SKRIPSI

PERANCANGAN DAN PEMBUATAN MODUL *SMARTCARD* MENGGUNAKAN RENESAS R8C13/TINY UNTUK AKSES REKAM MEDIS MELALUI USB

Disusun Oleh :

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JURUSAN TEKNIK ELEKTRO S -1
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FAKULTAS TEKNOLOGI INDUSTRI
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LEMBAR PERSETUJUAN

PERANCANGAN DAN PEMBUATAN MODUL *SMARTCARD* MENGGUNAKAN RENESAS R8C13/TINY UNTUK AKSES REKAM MEDIS MELALUI USB

SKRIPSI

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KATA PENGANTAR

Puji syukur kehadirat Allah SWT dan Nabi Muhammad SAW yang telah memberikan rahmat dan hidayahnya sehingga saya dapat menyelesaikan Laporan Akhir dengan judul **"PERANCANGAN DAN PEMBUATAN MODUL *SMARTCARD* MENGGUNAKAN RENESAS R8C13/TINY UNTUK AKSES REKAM MEDIS MELALUI USB ".**

Laporan Akhir ini disusun sebagai salah satu syarat penilaian mata kuliah tugas akhir di Program Studi Teknik Elektronika S-1.

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Malang, Maret 2008

Penulis

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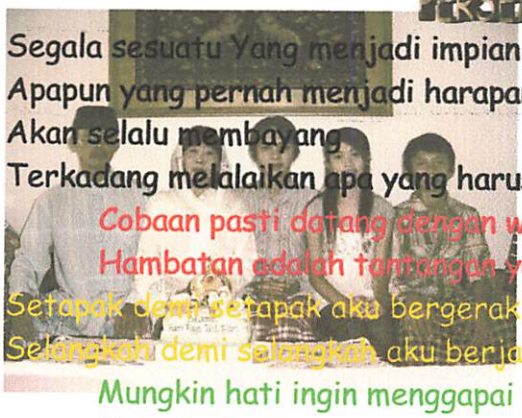

Segala sesuatu Yang menjadi impian
Apapun yang pernah menjadi harapan
Akan selalu membayang
Terkadang melalaikan apa yang harus didahulukan
Cobaan pasti datang dengan wajah-wajah menyenangkan
Hambatan adalah tantangan yang tidak bisa didiamkan
Setapak demi setapak aku bergerak melaluinya
Selangkah demi selangkah aku berjalan menghadapinya
Mungkin hati ingin menggapai sesuatu yang lebih tinggi
Meraih dan terus meraih
Akan tetapi tangan dan kaki sudah tak sampai lagi
Dan mungkin harus sampai disini

Keberhasilan tidak semestinya harus dipandang dari apa yang didapat
Melainkan perjuangan dikala harus berusaha untuk hadapi tantangan
Manusia dengan segala daya dan kemampuannya hanya
sekedar merencanakan, berusaha dan berdoa
Dan Allah menentukan hasil dari apa yang telah diusahakan
Senang ataupun tak senang yang pasti ada hikmah yang tersembunyikan
Lumpuhnya tangan dan kaki, tak akan bisa melumpuhkan keyakinan ini.

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ABSTRAKSI

PERANCANGAN DAN PEMBUATAN MODUL *SMARTCARD* MENGGUNAKAN RENESAS R8C13/TINY UNTUK AKSES REKAM MEDIS MELALUI USB

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Dalam kemajuan teknologi yang telah berkembang pesat diantara salah satunya adalah smartcard yang dapat diaplikasikan secara kompleks. Salah satunya untuk sistem aplikasi rekam medis yang digunakan oleh instansi Rumah Sakit, dimana data informasi riwayat kesehatan yang secara manual dikonversikan ke informasi digital.Dalam pembuatan modul smartcard memanfaatkan mikrocontroller Renesas R8C13/Tiny sebagai pemroses utama.

Alat ini bekerja dengan mendeteksi id card data pasien yang telah diakses pada database server yang dimana smartcard dapat digunakan secara portable pada instansi Rumah Sakit manapun yang mengaplikasikan sistem ini. Dimana smartcard mengakses data 8 bit dengan proses frame 1 start bit dan 1 stop bit yang dimana proses transmisi data I/O ketika pada smartcard ketika logika high untuk stop bit bersamaan dengan proses start bit. Pada proses transmisi untuk akses I/O dengan mengasumsikan panjang clock untuk lebar data I/O dan menggunakan komunikasi serial *UART* dengan mengasumsikan baudrate 9600bps untuk mensinkronisasikan komunikasi mikrocontroller dengan koneksi aplikasi pada PC.

BAB 1

PENDAHULUAN

1.1 Latar Belakang

Pada kemajuan teknologi yang semakin cepat dan perkembangan ilmu yang makin pesat dimana salah satunya adalah smartcard. Dari gagasan tersebut maka muncul suatu pemikiran untuk membuat sebuah modul smartcard. Maka pada sistim aplikasi yang memakai smartcard dapat lebih spesifik dan kompleks untuk sistim yang saya gunakan pada aplikasi Akses Rekam Medis (*Medical Record*) yang digunakan pada instansi Rumah Sakit. Dimana pada instansi Rumah Sakit pada sistim pendataan pasien masih diberikan pelayanan manual (tercatat) dalam beberapa tempo pemeriksaaan.

Apabila pendiagnosaan pasien terjadi kesalahan yang fatal yang disebabkan karena pergantian dokter atau pemindahan pemeriksaan kesehatan pada antar instansi Rumah Sakit baik di dalam kota maupun luarkota dapat diantisipasi oleh dokter terkait. Ketika pendiagnosaan terjadi kesalahan dan terjadinya Malpraktek dan akan memberikan dampak buruk bagi Instansi Rumah Sakit tersebut maka dengan gagasan sistem ini dapat memberikan kemudahan pendiagnosaan yang akan mengurangi dampak yang tidak diinginkan.. Berdasarkan perkembangan teknologi ini kita harus bisa memberikan informasi dengan cepat sesuai dengan data yang dibutuhkan dengan penyimpanan data medis secara digital yang menggunakan teknologi smartcard, yang menginterfacekan antara dokter dan pasien dengan melakukan rekam medis (*medical record*). Misalkan kita ingin memberikan informasi tentang data – data tiap pasien dengan terstuktur dalam

beberapa tempo dengan mengakses data proses gejala – gejala penyakit yang diderita oleh pasien pada beberapa jangka waktu telah dikonsultasikan dengan dokter dan pasien seperti memberitahukan jenis beberapa penyakit yang telah diderita oleh pasien, data riwayat kesehatan si pasien, waktu pemeriksaan, dan lain – lain secara digital dengan menggunakan teknologi smartcard.

Dari gagasan tersebut diatas maka muncul suatu pemikiran untuk membuat sebuah sistem yang dapat memberikan informasi secara digital yang dibutuhkan dengan cepat tanpa harus mengecek data – data yang ada di dalam arsip data Rumah Sakit secara manual. Dimana tujuan system tersebut dapat memberikan kemudahan interface pendiagnosaan antara dokter dengan pasien yang secara global dan kompleks dan memberikan data-data riwayat kesehatan si pasien dalam beberapa periode dan apabila terjadi kesalahan pada akses rekam medis pasien dapat disimulasikan oleh dokter diinstansi rumah sakit manapun yang mengaplikasikan sistem ini dengan mengakses data pasien melalui database admin. Apabila hasil malpraktek pasien yang diakibatkan ketidaksamaan diagnosa penyakit dan pemberian resep oleh beberapa dokter yang menggunakan sistem ini dapat diantisipasi oleh dokter sebelum melakukan akses medika yang bertahap jauh.Sistem kendali utamanya adalah sebuah mikrocontroller yang diberi masukan kartu smartcard yang diberi data – data informasi dari pasien tersebut yang kemudian disamakan dengan data yang ada pada database.

1.2 Rumusan Masalah

Mengacu pada permasalahan yang ada, maka dalam merencanakan dan pembuatan alat ini diutamakan pada hal-hal sebagai berikut :

1. Bagaimana merancang system akses rekam medis kesehatan Pasien di Instansi Rumah Sakit secara digital.
2. Bagaimana membuat modul smartcard untuk system akses rekam medis (*Medical Record*) yang menginterfacekan dokter dengan pasien.

1.3 Batasan Masalah

Dalam laporan akhir "Perancangan dan Pembuatan Modul Smartcard menggunakan Renesas R8C13/TINY untuk Akses Rekam Medis melalui USB", penulis akan memberikan batasan-batasan masalah agar tidak terjadi penyimpangan maksud dan tujuan utama penyusunan skripsi ini.

1. Mikrokontroller yang digunakan adalah R8C13/TINY.
2. Program aplikasi yang digunakan sebagai tampilan adalah Delphi.
3. Aplikasi alat hanya digunakan akses rekam medis (*Medical record*) yang hanya di komunikasikan antarmuka (*Interface*) antara pasien dengan dokter.
4. Tidak membahas jaringan komunikasi secara global.

1.4. Tujuan Penulisan

Tujuan menyusun tugas akhir ini antara lain :

1. Merancang system akses rekam medis kesehatan Pasien di Instansi Rumah Sakit secara digital.

2. Membuat modul smartcard untuk system akses rekam medis (*Medical Record*) yang menginterfacekan dokter dengan pasien.

1.5 Metodologi Penelitian

1. PERENCANAAN DAN PEMBUATAN ALAT

   Bertujuan untuk membuat diagram blok rangkaian yang sesuai dengan rencana kerja, kemudian direalisasikan dengan melaksanakan perencanaan dan pembuatan alat berdasarkan diagram blok rangkaian yang disusun.

2. STUDI ANALISA ALAT

   Dimaksudkan untuk melakukan analisa pengujian alat yang telah dirancang, apakah sesuai dengan fungsi kerja yang diharapkan atau tidak

3. PENYUSUNAN BUKU LAPORAN

   Bertujuan untuk menyusun data laporan berpedoman pada alat yang selesai dibuat beserta kesimpulan cara kerja dari alat tersebut.

1.6. Sistematika Pembahasan

Sistematika pembahasan dari skripsi ini terdiri dari pokok pembahasan yang saling berkaitan antara satu dengan lainnya, yaitu :

BAB I. Pendahuluan

Pada bab ini dibahas tentang latar belakang permasalahan, rumusan masalah, batasan masalah, sistematika pembahasan dari alat yang direncanakan.

BAB II. Landasan Teori

Pada bab ini dibahas tentang teori-teori yang mendukung dalam perencanaan dan pembuatan alat ini yang meliputi Smartcard, Sistem Smartcard Reader, Modul USB FT232BM dan Mikrokontroler Renesas R8C/13 TINY.

BAB III. Perencanaan Dan Pembuatan Alat

Pada bab ini dibahas tentang perencanaan dan pembuatan keseluruhan sistem perangkat keras (hardware) dan perangkat lunak (software).

BAB IV. Pengujian Alat

Pada bab ini dibahas tentang proses serta hasil dari pengujian alat, yang didasarkan oleh pengukuran-pengukuran.

BAB V. Penutup

Pada bab ini akan disampaikan kesimpulan dari perencanaan dan pembuatan sistem ini.

BAB II

LANDASAN TEORI

Landasan teori sangat membantu untuk dapat memahami suatu sistem. Landasan teori juga dapat digunakan sebagai acuan di dalam merencanakan suatu sistem. Dengan pertimbangan hal-hal tersebut, maka landasan teori merupakan bagian yang harus dipahami untuk pembahasan lebih lanjut. Dalam landasan teori ini akan dibahas teori dasar yang berhubungan dengan *Smart Card, Smart Card Reader ACR30, Max 232, Mikrokontroler Renesas R8C13/TINY dan FT232BM-USB.*

2.1 Smartcard

Untuk jenis kartu yang digunakan dalam penyusunan tugas akhir ini adalah type SLE 4442 dengan kapasaitas memory kartu 256 byte. Dimana smartcard merupakan sebuah kartu yang memiliki memory yang dapat menyimpan data-data. Kartu chip secara umum di golongkan menjadi dua macam berdasarkan penggunaanya yaitu :

- Kartu chip yang lebih berupa *memory.*
- Kartu chip yang mempunyai *microprocessor.*

Untuk jenis kartu chip pertama lebih sering digunakan sebagai kartu telpon, kartu internet dan fasilitas – fasilitas prabayar yang tidak memerlukan informasi penguna kartu. Kartu jenis ini fungsinya lebih ditekankan pada penyimpanan sejumlah kredit atau poin untuk transaksi-transaksi,contohnya pada kartu telpon chip. Pada beberapa jenis

kartu yang baru telah dilengkapi dengan enkripsi atau pin identifikasi yang seperti ini biasa disebut dengan *smart memorycard.*

Sedangkan untuk jenis kartu chip kedua adalah kartu yang lebih cangih yang dilengkapi mikroprosessor untuk fungsi-fungsi tertentu,selain menyimpan identitas pemilik kartu juga dapat memproses sejumlah data.Kartu jenis ini juga memiliki memory berupa ROM dan EEPROM,data dilindungi dengan algoritma enkripsi.jenis ini umum disebut dengan *smartcard* atau kartu cerdas (walau sebenarya *memorycard* adalah juga merupakan *smartcard*).

Spesifikasi kartu telpon chip generasi pertama :

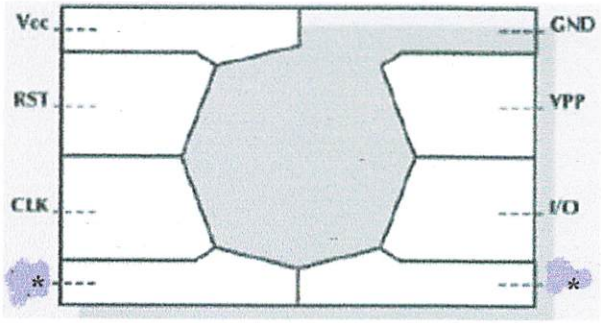
- Synchronous protocol
- Teknologi N-Mos atau CMOS untuk yang lebih baru.
- Organisasi memory 256 x 1 bit.
- 96 bit proteksi penulisan dengan clock out fuse.
- Pemakaian daya rendah 85 mW pada read mode.
- 21 volt programming voltage.
- Acces time 500 ms.
- Operating temperature range – 10°C sampai +70°C.
- Deteksi data hingga 10 thn.

Sedangkan untuk generasi kedua adalah

- ISO 7816 – ½ compatible protocol.
- Penggunaan tegangan supply tunggal 5 volt.
- Teknologi NMOS.
- Konsumsi daya rendah.

2.1.1 Posisi Pin pada Smartcard.

Posisi pin pada smartcard mengunakan standart ISO7816 dimana letaknya akan diperhatikan pada gambar berikut :



Gambar 2.1 Konfigurasi Pin *Smartcard* [2]

Tabel 2.1 Konfigurasi Pin Smartcard

Nama	deskripsi
Vcc	+ 5 volt
RST	Reset
CLK	Clock
*	NC
GND	Ground
*	NC
I/O	Input / Output
*	NC

2.1.2 System komunikasi Data Smartcard.

Komunikasi antara Smartcard dengan interface devais (reader) melalui beberapa proses yaitu :

- Kontak dan Aktivasi oleh reader.
- Reset dari smartcard.
- Answer to Reset (ATR) oleh smartcard.
- Pertukaran data antara smartcard dan reader.
- Deaktivasi kontak oleh reader.

2.1.2.1 kontak dan aktivasi oleh reader.

Untuk menghindari kerusakan yang mungkin terjadi pada kartu yang disebabkan oleh reader pada saat kartu dimasukan maka sirkuit diharapkan tidak diaktifkan dahulu sebelum pin - pin pada kartu benar – benar terhubung dengan readernya.adapun didalam mengaktifkan reader harus memperhatikan beberapa hal berikut yaitu :

- Reset berada pada status " low".
- Vcc telah diberikan tegangan tertentu.
- I/O pada reader berada pada reception mode.
- CLK harus diberikan clock yang sesuai dan stabil.

2.1.2.2 Reset Oleh Smartcard.

Setiap card reset dikenali oleh reader ,dimana kartu harus merespon dengan ATR seperti yang dijelaskan pada bagian berikut

Pada saat akhir aktivasi kontak oleh reader (RST berada pada state "low" ,Vcc telah diberi tegangan tertentu,I/O pada reader berada pada *reception mode*,Vpp harus dinaikan pada *idle state*,CLK harus diberi clock yang sesuai dan stabil),maka kartu akan merespon secara asinkron bahwa card siap di reset.

Jika kartu merespon secara sinkron,seperti pada kartu kredit misalnya maka semua pin berada pada posisi "low" Vcc telah diberikan pada tegangan tertentu,Vpp diset pada *idle state*,CLK dan RST berada tetap pada "Low",I/O berada pada *reception mode*,Reset harus berada pada kondisi "High" sekurang – kurangnya 50 us sebelum kembali kekondisi "Low".

2.1.2.3 *Answer To Reset* (ATR).

Terdapat dua buah tipe transmisi pengiriman data pada saat answer to reset yaitu :

- Pengiriman secara asinkron

  Karakter yang dikirim melalui I/O (half duplex) secara asinkron dimana setiap karakter berupa Byte (8 bit).

- Pengiriman secara Sinkron.

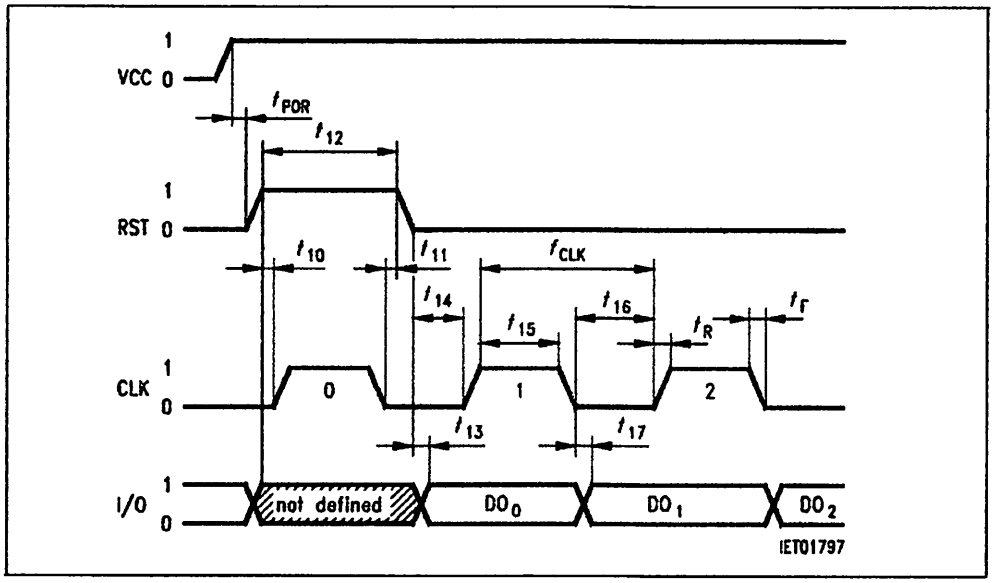
  Sekelompok bit yang dikirim secara half duplex melalui clock pada CLK.

Smartcard digunakan sebagai kartu GSM atau kartu telpon biasanya megunakan transmisi asinkron, sedangkan transmisi sinkron biasanya digunakan pada kartu kredit.

2.1.2.4 Deaktivasi Kontak oleh Reader.

Yaitu Jika pertukaran data putus atau dibatalkan yang disebabkan semisalnya oleh pengambilan kartu atau kartu yang tidak merespon maka kontak pada pin harus dinonaktifkan,adapun proses tersebut meliputi :

- RST pada kondisi "Low".
- CLK pada Kondisi "Low".
- Vpp tidak diberi tegangan.
- I/O berada pada kondisi "A"
- Vcc tidak diberi tegangan.



Gambar 2.2 Konfigurasi Timing Diagram *Smartcard* [2]

2.2 Smartcard Reader ACR30

Untuk smartcard reader yang digunakan dalam penyusunan tugas akhir ini adalah type ACR30 yang menginterfacekan antara pin smartcard dengan pin holder pada smartcard reader. Adapun gambar fisik dari smartcard type ACR30 dapat digambarkan sebagai berikut:

Gambar 2.3 Smartcard reader ACR30 [2]

Adapun perintah – perintah yang dikeluarkan reader dalam mengaakses kartu ini yaitu:

1. Reset

   Di dalam melaksanakan reset pada saat kartu dimasukkan ke dalam reader harus dapat dilakukan dengan cara mingikuti format berikut :

   Format perintah

Tabel 2.2 Format Reset [2]

Instruction Code	Data length
80_H	00_H

2.4 Smartcard Reader ACR30

Untuk smartcard reader yang digunakan dalam perancangan tugas akhir ini adalah tipe ACR30 yang menggunakan interface serial port dengan pin koneksi pada smartcard reader. Gambar 2.x dari smartcard type ACR30 dapat digambarkan sebagai berikut:

Gambar 2.x Smartcard reader ACR30

Ada beberapa command yang dapat digunakan dalam smartcard reader ini yaitu:

1. Reset

Perintah ini digunakan untuk mereset smartcard reader dan mengembalikan ke keadaan awal.

Format perintah:

Tabel 2. Format Reset

Instruction Code	Data length
30 H	00 H

2. Power_Off

Dalam mengakifkan reader pada saat kartu dimasukkan dapat mengunakan format sebagai berikut :

Format perintah

Tabel 2.3 Format Power_Off [2]

Instruction Code	Data length
81_H	00_H

3. Read_data

Pembacaan kartu dilakukan dengan jalan melakukan perintah pada saat kartu dimasukkan yaitu :

Format perintah

Tabel 2.4 Format Read Data [2]

Instruction Code	Data length	Data		
		ADDR		LEN
90_H	03_H			

ADDR : Alamat byte pada saat pembacaan kartu.

LEN : Jumlah data N yang dibaca dari kartu ($0 < N \leq MAX\_R$)

4. Write_Data

Pada saat kartu dimasukkan penulisan dilakukan pada alamat tertentu dengan format sebagai berikut :

Format perintah

Tabel 2.5 Format Write Data [2]

Instruction Code	Data length	Data					
	LEN	ADDR		BYTE 1	...	...	BYTE N
91_H							

LEN : Banyaknya byte data pada penulisan di kartu mulai dari awal data hinga akhir data.

ADDR : Alamat byte di dalam kartu pada saat memulai penulisan.

BYTE x : Nilai byte pada kartu mulai dari alamat ADDR dimana dimana BYTE 1 adalah penulisan alamat ADDR dan BYTE N adalah penulisan untuk alamat ADDR+N-1.

5. Present_Code

Memberikan kode rahasia dari dari kartu serta memungkinkan penulisan operasi dengan kartu SLE4442.

Berikut adalah tindakan yang dieksekusi oleh ACR30 yaitu

- Mencari "1" bit dalam pernyataan kesalahan proses dan menulisnya dengan bit "0".
- Memberikan spesifikasi kode yang ditetapkan kepada kartu.
- Mencoba untuk menghapus pernyataan kesalahan proses.

Format present code tersebut adalah :

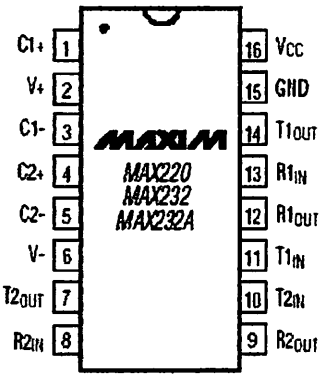
Tabel 2.6 Format Present Code [2]

Instruction Code	Data length	Data		
		CODE		
92_H	03_H			

CODE : Tiga byte rahasia code (PIN)

2.3 Komunikasi Serial

Berfungsi untuk hubungan komunikasi antara reader smartcard dengan mikrokontroler R8C/13 Tiny, digunakan RS-232, dimana pada RS232 ini terdapat fungsi-fungsi untuk Tx (pengiriman data), Rx (penerimaan data),CTS(Clear To Send) dan DTR. Untuk melakukan *transfer* data dari Reader Smartcard ke mikrokontroler digunakan IC MAX232, yang merupakan rangkaian terpadu untuk antarmuka komunikasi serial.



Gambar 2.4 RS 232 (MAXIM)

RS MAX232 tersusun dari 2 bagian yaitu *RS232 Line Driver* yang berfungsi mengubah level tegangan TTL ke level tegangan RS232 dan *RS232 Line Receiver* yang berfungsi mengubah level tegangan RS232 ke level tagangan TTL.

Alat ini merupakan standart yang dipakai untuk mengirimkan aliran bit seri antar *interface*. Komunikasi serial dapat dibagi menjadi dua sifat dasar pola komunikasi. Yang pertama adalah komunikasi asinkron, dimana pola-pola bit tertentu dipakai untuk memisahkan bit-bit karakter. yang kedua adalah komunikasi seri *sinkron*, yang memungkinkan karakter dikirim secara berurutan, namun membutuhkan karakter *sinkronisasi* khusus pada awal setiap karakter dan karakter semua khusus untuk dikirimkan ketika tidak ada informasi yang sedang dikirim.

2.3.1 Protokol Komunikasi pada RS 232

Beberapa protokol dalam interface RS 232 adalah:

- Start Bit

  Merupakan sebuah bit dengan logic "0" dimana bit ini yang menandakan bahwa akan ada karakter atau data yang mengikutinya. Bit ini langsung diberikan oleh sinyal device tanpa harus mensetnya terlebih dahulu.

- Data Bit

  Merupakan bit yang mewakili dari karakter yang diikutinya *data bit* ini dapat diset sepanjang antara 5 sampai 8 bit.

- Pariti Bit

  Merupakan bit yang digunakan sebagai *error checking* pada *receiver* , apabila terjadi kesalahan maka *receiver* akan menset *error flag* (parity error) pada special register. *Parity bit* ini menghitung jumlah data yang berlogic '1' pada data bit. Perhitungan jumlah data bit tersebut tergantung dari jenis *parity* yang diset. Untuk parity *EVEN* maka jumlah data bit yang berlogic '1' ditambah

dengan *parity bit* akan menghasilkan jumlah yang ganjil. Sedangkan untuk *parity MARK* merupakan *parity bit* selalu berlogic '1' begitu pula pada space, parity bit selalu berlogic ' 0' dan *parity NONE* disini *parity bit* yang diabaikan.

- Stop Bit

  Merupakan bit yang menandakan akhir dari suatu paket data (biasanya 1 byte data). Seperti pada start bit, bit ini langsung diberikan dari serial device. *Stop bit* ini dapat diset panjangnya menjadi satu bit, satu setengah dan dua bit.

- Baud Rate

  Sebenarnya *baut rate* berarti pergantian kondisi tiap detik *(State Change of the Line persecond)*, tetapi karena hanya ada 2 kondisi pada serial *(logic 0 dan 1)* maka dapat juga digunakan untuk menunjukkan kecepatan dari transmisi *(bits per second)*.

➢ Tx Buffer : berfungsi menampung dan menyimpan data yang akan dikirim keluar. Data ini dikirim oleh CPU ke Tx Buffer setelah memastikan diperolehkannya melakukan pengiriman.

➢ Rx Buffer : berfungsi menampung dan menyimpan data yang akan diterima. Data yang akan diterima lebih dahulu ditampung dalam Rx Buffer.

2.4 Mikrokontroler RENESAS R8C / Tiny

Renesas technology adalah produsen semikonduktor tingkat internasional.Renesas terbangun dari dua produsen semikonduktor,renesas juga mengeluarkan berbagai jenis keluarga mikrokontroler (MK).

Mikrokontroler RENESAS dibangun menggunakan proses gerbang silicon CMOS dengan kemampuan tinggi menggunakan CPU seri R8C/Tiny dan dikemas dalam modul plastic dengan jumlah pin sebanyak 32. Mikrokontroler ini beroperasi menggunakan perintah canggih khususnya efisiensi perintah dengan level tinggi. Mikrokontroler ini mempunyai 1 Mbytes kapasitas alamat, yang bisa digunakan untuk mengeksekusi perintah dengan kecepatan tinggi. Data flash ROM sebesar 2 KB x 2 blocks.

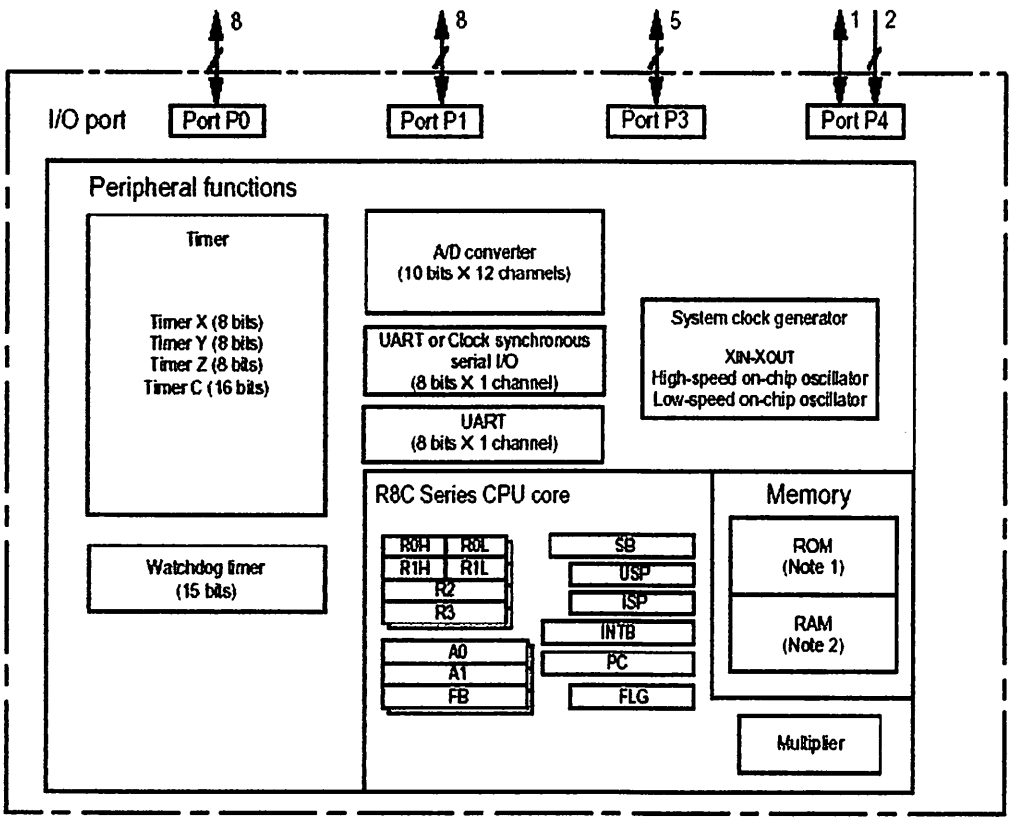
Renesas R8C adalah salah satu jenis keluarga MK M16C.CPU R8C sama dengan CPU CISC 16-bit M16C,hanya saja lebar jalur data R8C adalah 8-bit.Kerena menggunakan CPU yang sama maka R8C memiliki *instruction set* hamper sama dengan M16C.Perbadaanya hanya terletak pada 2 instruksi,yaitu R8C tidak memiliki instruksi JMPS (*Jump Special Page*) dan JSRS (*Jump Subroutine Special Page*).R8C/13 adalah salah satu tipe MK dalam seri R8C.MK ini memiliki kemasan 32-*pin* LQFP.dalam perancangan pada skripsi ini menggunakan MK MK seri R5F21134FP,yaitu R8C13 yang memiliki flash ROM 16KB(1000 E/W *cycles*) dan RAM sebesar 1KB.

2.4.1 Spesifikasi R8C/13Tiny

Berikut ini adalah spesifikasi R8C13/Tiny dengan peta peripheral dan memori – memorinya :

- Mempunyai CPU core (16-bit) 1-20 MHz, 3.0 – 5.5 Volt dan 1 – 10 MHz 2.7 – 5.5 Volt.
- Rangkaian Clock,kecepatan *low/high On-Chip Oscillator*.Clock utama dengan Xin/Xout.
- Memory (ROM/SRAM) 16Kbyte / 1 Kbyte, 2 x 2 Kbyte data flash pada R8C/13 Tiny.

- Kemasan 32 pin LQFP (7 mm x 7 m)

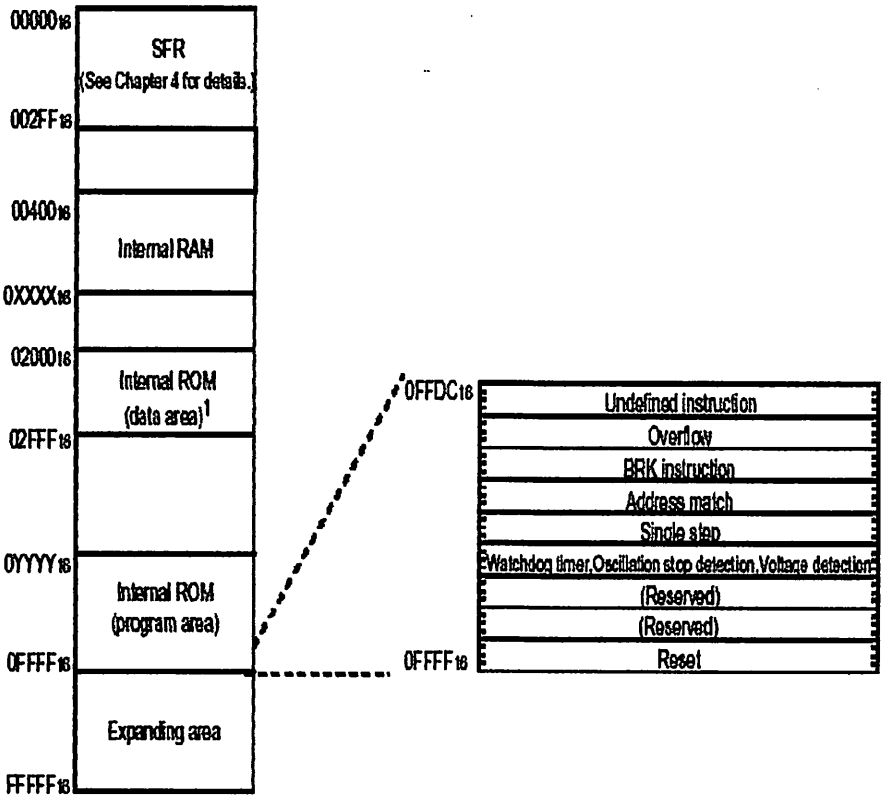


Gambar 2.5 Blok Diagram MCU Renesas [1]

Mikrokontroler Renesas R8C/Tiny mempunyai struktur memori yang terdiri atas :

- Space alamat hingga 1 Mbytes dari alamat 00000_{16} sampai $FFFFF_{16}$.
- ROM internal (*program area*) dialokasikan pada alamat terendah dimulai dari alamat $0FFFF_{16}$. Misalnya, 16 Kbyte ROM internal dialokasikan pada alamat yang dimulai dari $0C000_{16}$ sampai $0FFFF_{16}$.
- ROM internal untuk *data area* dialokasikan pada alamat 02000_{16} sampai $02FFF_{16}$.

- Sedangkan RAM internal dialokasikan pada arah alamat yang lebih tinggi dimulai dari alamat 00400_{16}.
- Special function register (SFR) dialokasikan pada alamat mulai dari 00000_{16} sampai $002FF_{16}$. Fungsi register control peripheral dialokasikan disini.



NOTES:

1. The data flash ROM block A (2K bytes) and block B (2K bytes) are shown.
2. Blank spaces are reserved. No access is allowed.

Type name	Internal ROM		Internal RAM	
	Size	Address 0YYYY₁₆	Size	Address 0XXXX₁₆
R5F21134FP, R5F21134DFP	16K bytes	0C000₁₆	1K bytes	007FF₁₆
R5F21133FP, R5F21133DFP	12K bytes	0D000₁₆	768 bytes	006FF₁₆
R5F21132FP, R5F21132DFP	8K bytes	0E000₁₆	512 bytes	005FF₁₆

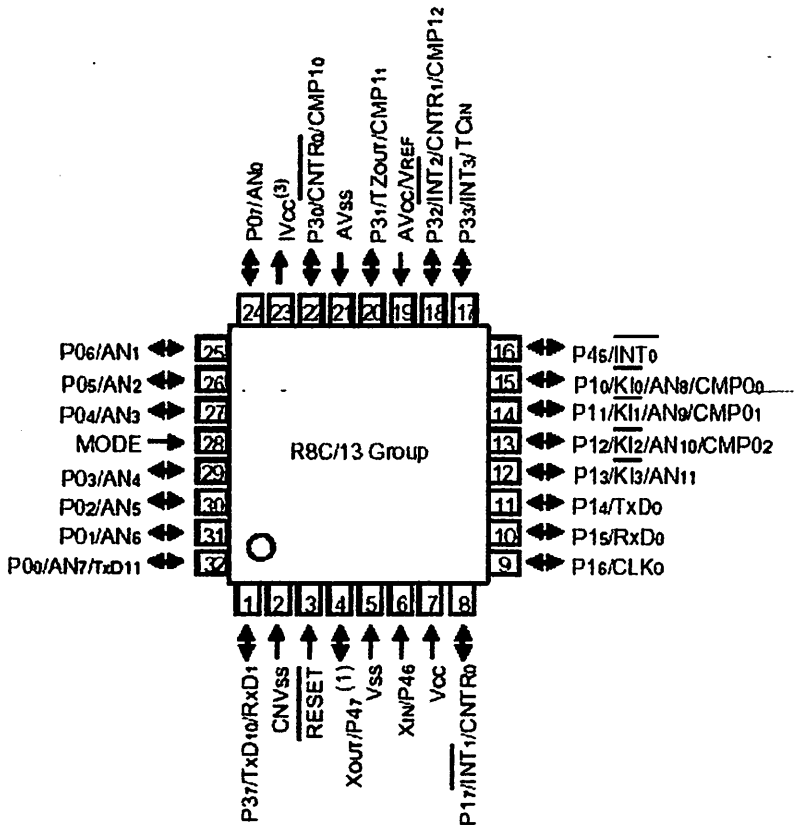
Gambar 2.6 Memory Map [1]

2.4.2 Kelebihan Kunci R8C/13 Tiny

Banyak kelebihan – kelebiha yang dimiliki R8C/13 Tiny diantaranya adalah :

- Kompatibel dengan M16C yaitu kompatibel dalam instruksi dan kode.
- *Peripheral* lebih terintegrasi jadi lebih hemat.
- *Electromagnetic Compatibility* (EMC) mempunyai EMI rendah,EMS tinggi.
- *Development Tool (Compiler dan Debugger)* didapat dengan murah dan difasilitasi *On-Chip Debugger.*
- Mempunyai *fitur fail – safe* yaitu pengamanan terhadap kegagalan system.
- Konsumsi daya rendah.
- 16-bit CISC CPU dengan kecepatan maksimal 20 MHz (1 : 1).
- 89 instruksi CISC lebih hemat ROM kira – kira 20 % RAM sampai 1 KB.
- Waktu konversi ADC 3 µS.

2.4.3 Konfigurasi Pin R8C/13 Tiny



Gambar 2.7 Konfigurasi Pin R8C/Tiny [1]

❖ Keterangan fungsi masing-masing pin R8C13/Tiny :

1. V_{CC}

   Digunakan untuk sumber tegangan dengan range nilai antara 2,7 – 5,5 Volt.

2. V_{SS}

   Range tegangan 0 Volt

3. IV_{CC}

   Pin ini digunakan untuk menyetabilkan sumber tegangan internal. Pin ini dihubungkan ke V_{SS} melalui kapasitor 0,1 μF.

4. AV_{CC}, AV_{SS}

   Pin ini merupakan input power supply untuk A/D Converter. Pin ini dihubungkan ke pin V_{CC}, sedangkan AV_{SS} dihubungkan ke V_{SS}. Hubungkan pin AV_{SS} dan AV_{CC} dengan kapasitor.

5. Reset

   Merupakan input reset pada MCU.

6. CNV_{SS}

   Pin ini dihubungkan ke V_{SS} melalui resistor.

7. Mode

   Pin ini dihubungkan ke V_{CC} melalui resistor.

8. X_{IN}, X_{OUT}

   Pin ini disediakan untuk pembangkitan rangkaian I/O pada clock utama. Hubungkan resonator keramik atau osilator kristal antara X_{IN} dan X_{OUT}. Untuk menggunakan clock derived external, masukkan ke pin X_{IN} dan pin X_{OUT} dibiarkan terbuka.

9. $INT_0 - INT_3$

   Merupakan pin input interupt

10. $KI_0 - KI_3$

    Merupakan pin Key Input interrupt.

11. $CNTR_0$ (I/O)

    Merupakan timer pin X I/O

12. $CNTR_0$ (O)

    Merupakan timer pin X output.

13. $CNTR_1$

    Merupakan timer pin Y I/O

14. TZ_{OUT}

    Merupakan timer pin Z output.

15. TC_{IN}

    Merupakan timer pin C input.

16. $CMPO_0$ – $CMPO_3$ dan $CMPO_{10}$ – $CMPO_{13}$

    Merupakan timer pin C output.

17. CLK_0

    Merupakan transfer clock untuk pin I/O.

18. RxD_0 dan RxD_1

    Pin serial data input.

19. TxD_0, TxD_{10} dan TxD_{11}

    Pin serial data output.

20. V_{REF}

    Referensi pin input tegangan untuk A/D Converter. Hubungkan V_{REF} ke V_{CC}.

21. AN_0 – AN_{11}

    Pin input analog untuk A/D Converter.

22. $P0_0 - P0_1$, $P1_0 - P1_7$, $P3_0 - P3_3$, $P3_7$ dan $P4_5$

Merupakan port 8 bit CMOS I/O. $P1_0 - P1_7$ juga berfungsi sebagai port LED driver.

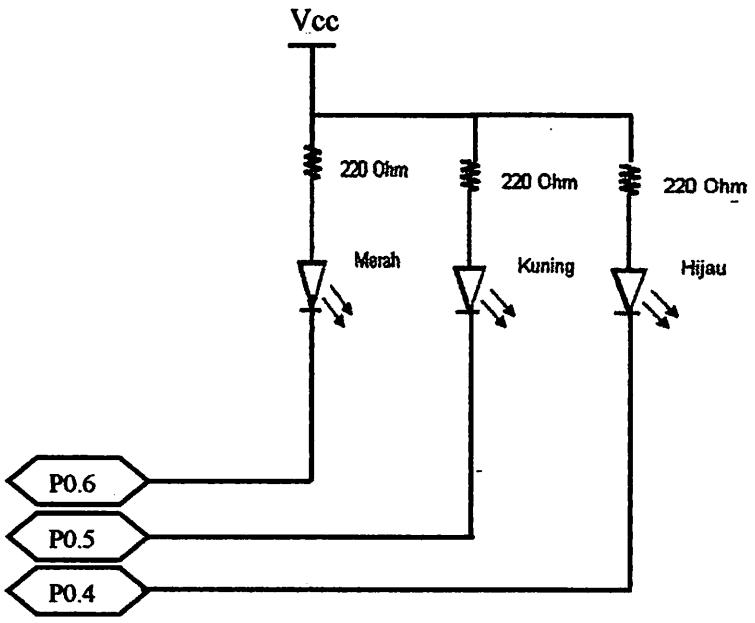
❖ **Rangkaian Osilator**

Pada osilator utama menggunakan Kristal luar sampai dengan 20MHz,dengan memiliki fitur Clock Stop Detect.kemudian untuk On Chip Osilator disediakan kecepatan Low 125 Khz dan High 8Mhz.saat setelah reset, default clock adalah kecepatan rendah On Chip osilator 125 KHz.

2.5 Rangkaian Indikator Smartcard

LED yang dipakai dalam perancangan ini adalah 3 buah Led indikator yang mempunyai fungsi untuk akses perintah interkoneksi smartcard reader dengan smartcard. Dimana 3 buah Led indikator yang digunakan yaitu :

- Led merah pada port 0.6 berfungsi sebagai indikator standby apabila koneksi antara smartcard belum terkoneksi dengan smartcard reader dan pada keadaan ON standby yang dikoneksikan pada Renesas R8C13/Tiny.
- Led kuning pada port 0.5 berfungsi sebagai indikator perintah write untuk smartcard melalui PC (Personal Computer) dengan melalui database yang diaplikasikan dimana terkoneksikan pada Renesas R8C13/Tiny.
- Led hijau pada port 0.4 berfungsi sebagai indikator read untuk smartcard melalui PC (Personal Computer) dengan melalui database yang diaplikasikan dimana terkoneksikan pada Renesas R8C13/Tiny.



Gambar 2.8 Rangkaian Indikator Smartcard

2.6 Modul FT232BM-USB

Perkembangan teknologi komputer dimana seiring dengan perkembangan ilmu pengetahuan yang semakin cepat pada PC atau Laptop – laptop untuk keluaran terbaru jumlah port serial RS232 semakin lama semakin berkurang, jika pada PC lama biasanya terdapat dua buah konektor RS232 maka sekarang hanya terdapat satu buah konektor saja sehingga keberadaan port serial RS232 sekarang telah digantikan oleh port USB yang mempunyai banyak kelebihan dibandingkan port serial RS232.adapun contoh pengiriman informasi secara serial melalui sebuah mikrokontroler yang dikirimkan ke PC melalui port USB seperti Modul FT232BM-USB yaitu modul interface yang digunakan untuk aplikasi dari mikrokontroller ke USB, hubungan ini dilakukan secara serial dengan kata lain sebuah modul yang dapat mengkonversikan data serial yang berasal dari mokrokontroller secara garis besar modul ini berfungsi untuk mengubah data USB yang

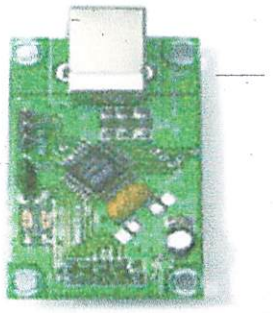
berasal dari port USB menjadi data serial dengan level tegangan TTL sehingga pengguna dapat melakukan komunikasi data serial (UART) melalui port USB. Keunggulan digunakannya modul ini adalah kemampuannya untuk mengirim data lebih cepat dibandingkan dengan komunikasi serial dengan mengunakan Port RS232 serta untuk kecepatan transfer data serial yang dapat di pakai oleh IC ini yaitu sebesar 300bps sampai 9600 bps.

Modul FT232BM-USB mempunyai spesifikasi sebagai berikut:

1. Memiliki tegangan kerja 4,4- 5,25 volt DC.
2. Tersedia 2 LED untuk indicator Tx dan Rx data pada komunikasi serial.
3. Memiliki boudrate 3Mbps (TTL), 1Mbps (RS-232), 3Mbps (RS-422/RS-485).
4. Pin sinyal kontrol (arah) untuk komunikasi RS-485 yang bekerja secara otomatis.
5. Kompatibel dengan USB 1.1 dan USB 2.0.

   Modul mengunakan konfigurasi daya Self Powered.
6. Memiliki output dengan level TTL 5 volt.
7. Memiliki EEPROM eksternal untuk menyimpan data PID,VID,nomor serial,dan deskripsi produk,pengisian datanya melalui USB.
8. Virtual COM port driver (VCP) dan D2xx (USB Direct Drivers + DLL S/W Interface) untuk windows 98,98SE,ME,2000 dan XP.
9. Mendukung format UART dengan 7/8 bit data , 1 / 2 stop bit dan Odd / Even / Mark / Space / No Parity.

Adapun gambar fisik dari modul FT232BM-USB dapat digambarkan sebagai berikut:

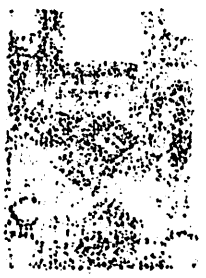


Gambar 2.9 Modul FT232BM-USB [4]

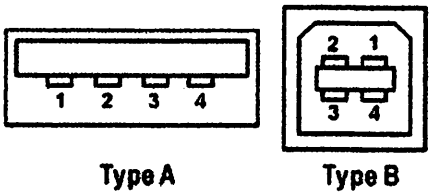
Gambar diatas merupakan modul dari FT232BM-USB secara fisik yang terdiri dari konektor USB TIPE B dan chip FT232BM sebagai komponen utama dari modul COM to USB tersebut serta komponen-komponen pendukung lainnya.

2.6.1. Kabel USB

Di dalam menghubungkan modul FT232BM-USB dengan komputer maka dibutuhkan kabel konektor USB dimana hanya terdapat ada 2 macam konektor yang digunakan dalam menghubungkan modul tersebut, yaitu konektor type A dan konektor type B seperti terlihat dalam Gambar 1. Konektor type A dipakai untuk menghubungkan kabel USB ke terminal USB yang ada pada bagian computer sedangkan Konektor type B dipakai untuk menghubungkan kabel USB ke terminal USB yang ada pada modul FT232BM-USB sedangkan untuk peralatan USB yang sederhana, misalnya mouse,



biasanya tidak pakai konektor B melainkan konektor tipe A hal ini dilakukan untuk menghemat biaya sehingga kabel langsung dihubungkan ke bagian dalam mouse.

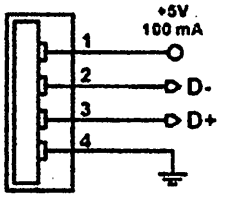


Gambar 2.10a Konektor USB [4]

Kabel USB terdiri dari 4 kabel ditambah konduktor pembungkus kabel seperti pelindung yang biasanya dijumpai dalam kabel audio.

Kabel nomor 1 dipakai untuk menyalurkan sumber daya dengan tegangan 5 Volt, jika diperlukan peralatan USB boleh mengambil daya dari saluran ini tidak lebih dari 100 mA. Komputer yang dilengkapi dengan kemampuan USB, wajib menyediakan daya sebesar 500 mA untuk keperluan ini. Peralatan USB yang memerlukan daya lebih dari ketentuan tersebut di atas, harus menyediakan sendiri sumber daya untuk keperluan kerja peralatan tersebut.

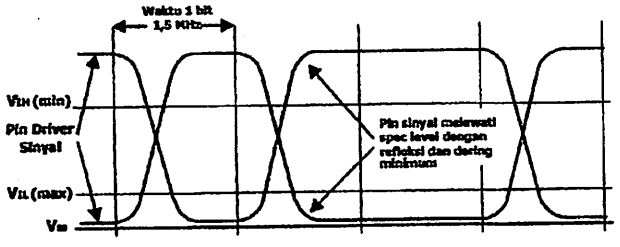
Kabel nomor 4 adalah ground sebagai saluran balik sumber tegangan 5 Volt.Kabel nomor 2 dan nomor 3 dipakai untuk pengiriman sinyal. Kabel nomor 2 bernama D- dan kabel nomor 3 bernama D+, tegangan pada dua saluran ini berubah antara 0 Volt dan 3,3 Volt seperti terlihat pada gambar 2 berikut:



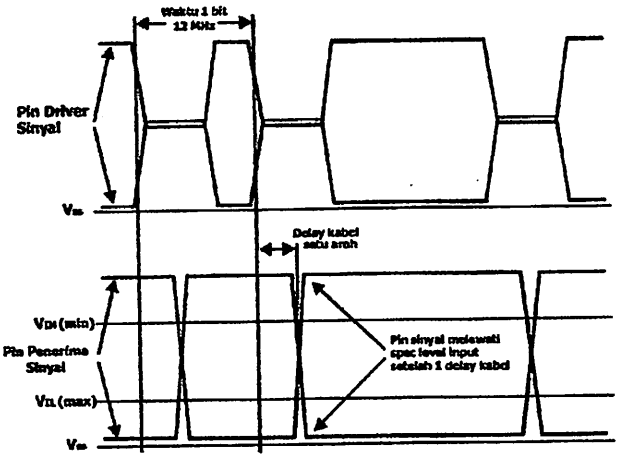
Gambar 2.10b Konektor Pin USB Tipe A [4]

2.6.2 Karakteristik USB (*Universal Serial Bus*).

Rentang tegangan USB adalah 0,3 volt hingga 3,6 volt (pada beban 1,5 kΩ).logika tinggi didapat jika tegangan sudah melebihi 2,8 volt terhadap ground pada beban 15kΩ.pada piranti USB yang berkecepatan rendah dan penuh untuk deferensial "1" dikirim dengan menarik D+ hingga lebih besar dari 2,8 volt dengan sebuah resistor 15 kΩ terhubung ke ground dan sekaligus menarik D- hinga dibawah 0,3 volt dengan dengan sebuah resistor 1,5kΩ terhubung ke 3,6 lebih rendah dari 0,3 volt dengan resistor pull-up dan pull-down yang sama.Di bagian penerima ,deferensial "1" dideferensialkan sebagai D+ lebih besar 200mV dari D-,dan deferensial "0" berarti D+ lebih kecil dari 200mV dibanding D-.Pada USB berkecepatan tinggi (480MBit/s) digunakan sumber arus tetap mA untuk mengurangi *noise*. Adapun bentuk sinyal gelombang pengiriman USB dengan kecepatan tinggi maupun rendah yang ditunjukkan pada gambar 2.4a dan 2.4b :



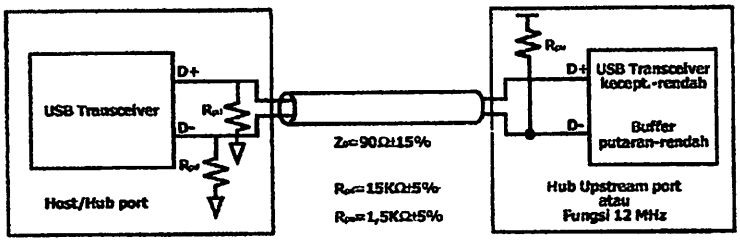
Gambar2.11a Gelombang sinyal USB 1,5 MHz[4]



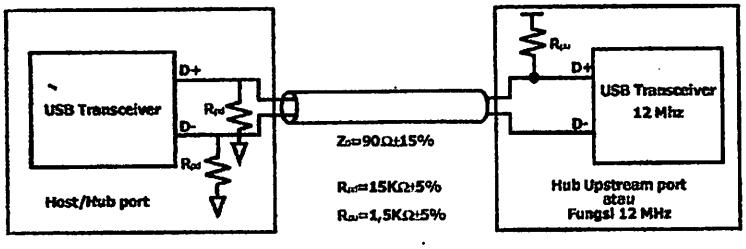
Gambar 2.11b Perkabelan USB Kecepatan tinggi 12MHz [4]

Kecepatan piranti USB dibagi menjadi dua yaitu kecepatan rendah (low-speed) dan kecepatan tinggi (full-speed) yang dihubungkan dengan cara koneksi resistor dan kabel USB oleh posisi resistor *pull-up* di ujung kabel *downstream* yaitu sebagai berikut :

- Piranti *full-speed* diterminalkan dengan resistor pull-up terhubung di D+ seperti gambar 2.5a.
- Piranti low-speed diterminalkan dengan resistor pull-up terhubung di D- ,seperti gambar 2.5b.
- Terminator pull-down di port down-stream adalah resistor 15kΩ ±5% terhubung ke ground.



Gambar 2.12a Perkabelan USB Kecepatan rendah [4]



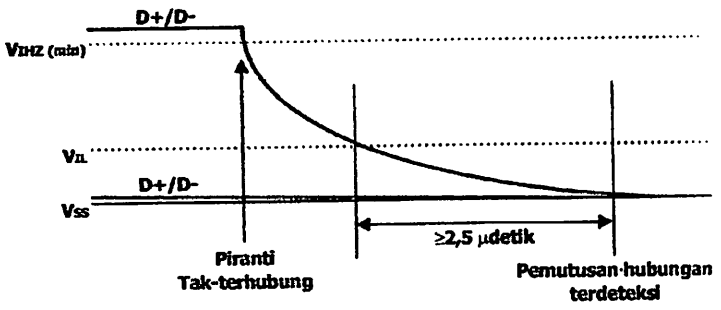
Gambar 2.12b Perkabelan USB kecepatan penuh [4]

2.6.3 Sinyal Penyambung dan Pemutusan

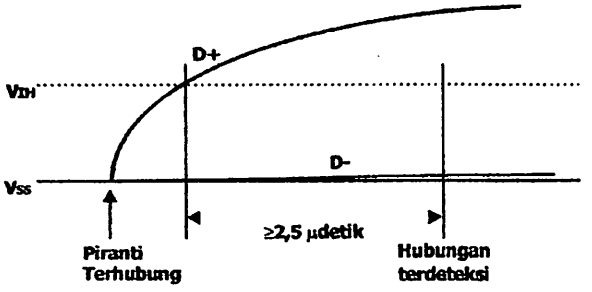
Pada sinyal penyambungan dan pemutusan USB yaitu ketika tidak ada piranti terhubung ke host atau komputer maka pull-down resistor yang ada akan menyebabkan D+ dan D- tertarik hingga di bawah ambang logika rendah host atau komputer ,hal ini menyebabkan munculnya keadaan SE0 (*singel-Ended 0*) di port downsteram.Kondisi tak-terhubungnya suatu piranti USB dari port akan dideteksi jika host atau komputer tidak mendrive *header* (di jalur data) selama lebih dari 2,5 µdetik.

Sedangkan jika sebuah piranti dihubungkan,maka host atau komputer akan mendeteksi bahwa salah satu jalur datanya tertarik hingan lebih besar dari ambang V_{IH} selama lebih dari 2,5µdetik.host kemudian bisa (option) mendeteksi kecepatan piranti yang baru terhubung dengan men-sempel keadaan bus segera sebelum men-drive SE0

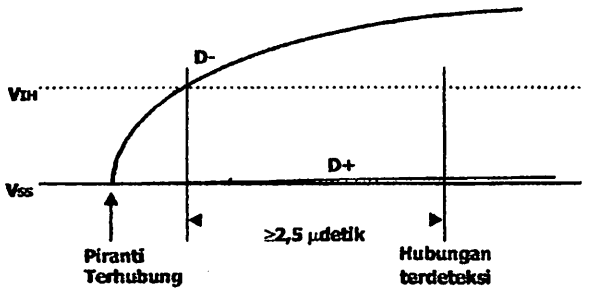
untuk mereset piranti.jika diinginkan,host dapat membuat bus mengambang sesudah meresetnya dan menjalankan evaluasi bus sesudah 2,5µdetik tersebut.lebih jelasnya seperti tampak pada gambar-gambar berikut :



Gambar 2.13 Sebuah piranti dilepas dari port USB [4].



Gambar 2.14a Sebuah piranti USB kecepatan tinggi dihubungkan ke port USB pada host/komputer [4].



Gambar 2.14b Sebuah piranti USB kecepatan rendah dihubungkan ke port USB pada host/komputer [4]

Untuk mengirimkan paket data,USB menerapkan enkode data NRZI (*Non Return to Zero Invert*). Dalam NRZI ini.logika "1" berarti tidak ada perubahan level tegangan dan logika "0" ditunjukkan dengan adanya perubahan level tegangan.Paket data dikirimkan ke bus USB berurutan dari bit yang berbobot paling rendah (LSB,*Least Significant Bit*),diikuti LSB berikutnya dan terakhir adalah bit yang berbobot paling tinggi (MSB,*Mos Significant Bit*).

2.7 Perangkat Lunak (*Software*)

Pada aplikasi sistem ini dibutuhkan program aplikasi tampilan pada PC yang mengakses aplikasi Delphi7 untuk tampilan. Dimana untuk mendukung pengakses database yang menggunakan database My-Sql dimana juga mendukung beberapa aplikasi program yang dimana antara lainnya :

1. Software Phptriad series 2.2.1

   Pada program ini untuk mengaktifkan koneksi database My-Sql dan pada localhost mengatur akses table yang telah disesuaikan. Koneksi aplikasi software Phptriad yang mengkoneksikan dengan database My-Sql adalah :

- Restart Apache

  Akses perintah ini adalah untuk mengatur ulang pengaktifan database MySql.

- Start Apache

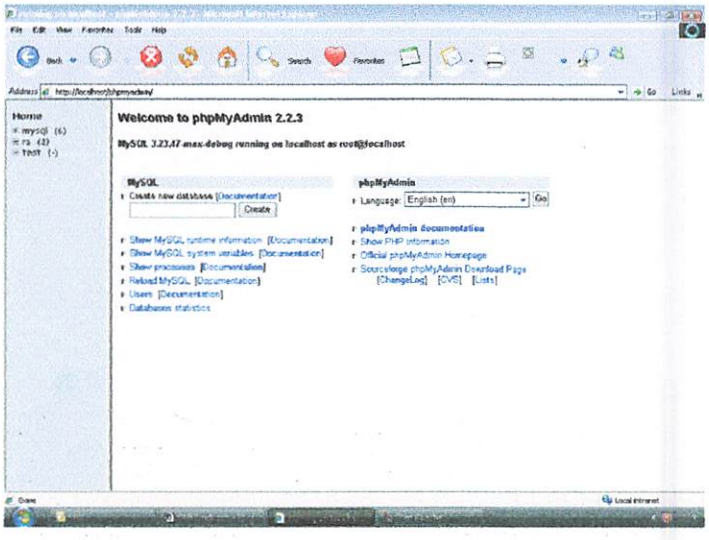
  Akses perintah ini adalah untuk memulai awal pengaktifan database MySql.

- Stop Apache

  Akses perintah ini adalah untuk menghentikan pengaktifan database MySql.

2. Software Mysql Connector ODBC series 3.51.12

   Pada program ini untuk mengaktifkan koneksi database My-Sql dan mengatur akses koneksi dengan aplikasi software dari Phptriad untuk menjalankan proses aktivasi database My-Sql.



Gambar 2.15 Form Database My-Sql

BAB III

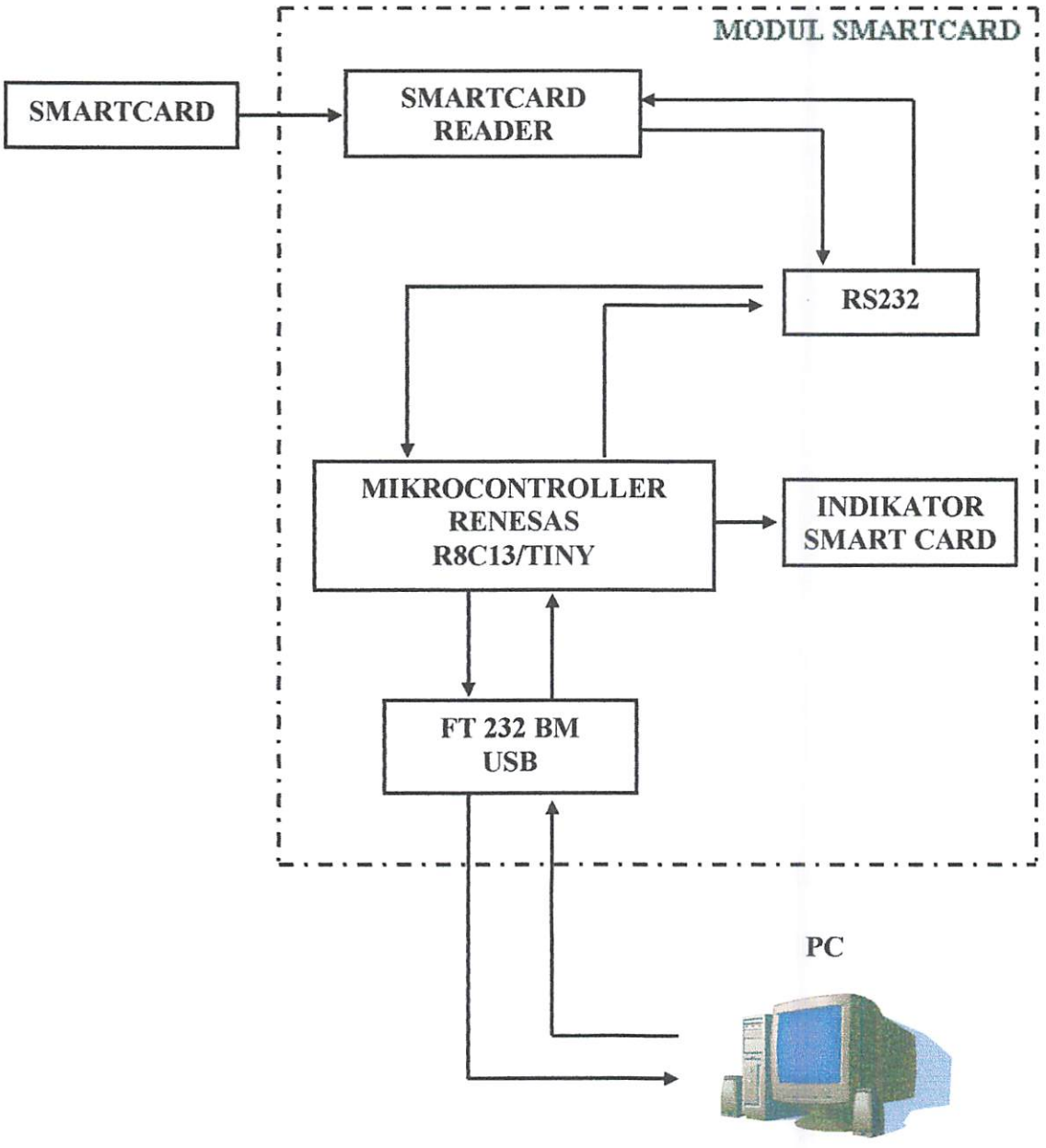
PERANCANGAN DAN PEMBUATAN ALAT

3.1. Pendahuluan

Pada dasarnya perencanaan alat yang dibuat dalam tugas akhir ini meliputi perencanaan perangkat keras dan perencanaan perangkat lunak. Komponen yang dipakai dalam perencanaan ini antara lain mikrokontroler Renesas R8C13/Tiny sebagai control utama, dengan komponen pendukung meliputi Smartcard, Smartcard Reader ACR30, Mikrocontroller Renesas R8C13/Tiny, Indikator Smartcard, FT232BM-USB , dan Delphi sebagai tampilan ke PC (*Personal Computer*).

3.2. Perancangan Perangkat Keras (*Hardware*)

Perancangan sistem akses rekam medis (*Medical Record*) juga dapat diaplikasikan akses melalui internet, sesuai dengan yang diinginkan berbasis web server yang dikendalikan dari database server sebagai kendali utama dan menggunakan komponen lain sebagai komponen pendukung. Sebelum membuat perangkat keras terlebih dahulu direncanakan blok diagram yang akan dibuat, dan membahasnya sesuai dengan blok diagram. Adapun blok diagram yang direncanakan adalah sebagai berikut :



Gambar3.1 Diagram Blok Akses Rekam Medis (Medical Record)

PC

3.2.1 Spesifikasi Blok Diagram Sistem :

1. **PC P4 Celeron 1.8GHz**

   Pada bagian ini berfungsi sebagai tampilan dengan menampilkan informasi yang ada pada Database.

2. **FT 232 BM - USB.**

   Merupakan bagian yang berfungsi sebagai modul penghubung komunikasi serial ke PC (Personal Computer) dan juga sebagai converter yang outputnya TTL dan RS 232.

3. **MIKROKONTROLLER RENESAS R8C13/TINY.**

   Merupakan bagian yang berfungsi sebagai pengolah data yang berasal dari Smartcard Sistem.

4. **INDIKATOR SMARTCARD**

   Merupakan bagian yang berfungsi untuk mengetahui proses keadaan system smartcard reader.

5. **RS232**

   Berfungsi sebagai interface antara mikrokontroler dengan Smartcard Reader.

6. **SMARTCARD READER.**

   Berfungsi sebagai penerima dan menulis data pada kartu smartcard.

7. **SMARTCARD.**

   Berfungsi sebagai kartu yang menyimpan data – data riwayat kesehatan pasien.

3.2.2. Cara Kerja Alat

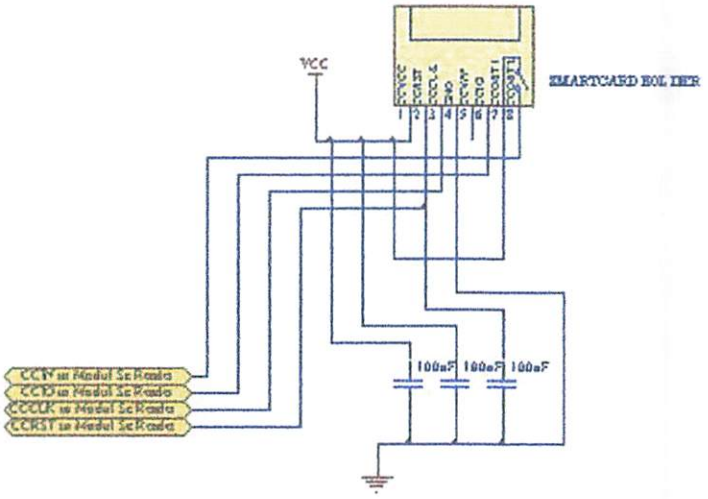
Cara kerja alat ini pada dasarnya adalah ketika power supply (Vcc) 12 Volt dicatukan reader maka pada holder reader terjadi proses pendeteksian sinyal kemudian CCDET1 port7 pada reader smartcard normaly close dengan CCDET2 port8 pada reader smartcard terkoneksi dengan P3.0 pada microcontroller yang berfungsi sebagai inisialisasi card sesuai dengan protocol modul yang mengakses data komunikasi serial UART. Ketika port8 pada smartcard reader logika high, maka microcontroller Renesas R8C13/Tiny mengetahui bahwa ada kartu yang dimasukkan dan kemudian microcontroller melanjutkan membaca kartu dimana pada proses pengiriman data input dan output (CCIO) yang dihubungkan pada port3.1 pada microcontroller Renesas R8C13/Tiny yang dimana pada proses pengolahan data mengasumsikan port3.2 pada renesas yang sebagai clock sesuai data yang diasumsikan dengan partisi clock.Dimana proses transmisi output tegangan dari reader dikonversikan level tegangan TTL oleh rs232 untuk akses transmisi ke mikrocontroller.Dan output data dari mikrocontroller dikirimkan melalui USB FT232BM yang dimana outputnya level TTL dan RS232 yang kemudian dihubungkan pada PC (*Personal Computer*) untuk akses tampilan aplikasi .

3.3 *Smartcard Reader*

Pada pembuatan skripsi ini, smartcard reader dapat dirancang dengan modul pengumpulan beberapa data sheet yang dimana harus disesuaikan dengan protokol yang mensupport pembacaan kartu jenis SLE442 dengan kapasitas memori 256 byte.di dalam melakukan komunikasi dengan mikrokontroler (R8C13/Tiny) dan komunikasi data

melalui Modul USB FT232-BM yang dikoneksikan ke PC, adapun pin – pin yang digunakan dalam komunikasi data pada sistem smartcard reader dengan mikrocontroller.

Smartcard reader terhubung dengan RS232, adapun pin – pin holder yang digunakan dalam modul yang akan terhubung dengan DB9/RS232.



Gambar 3.2 Pin pada holder yang digunakan pada Smartcard reader
(Sumber: Perancangan Alat)

❖ Pin – pin yang digunakan adalah :

➢ Pin 1

Pin ini merupakan pin CCVcc (Chip Card Voltage Supply) tegangan Vcc 3,3 Volt – 5Volt pada modul smartcard reader.

➢ Pin 2

Pin ini merupakan pin CCRST (Chip Card Reset) pada modul smartcard reader ke mikrocontroller Renesas R8C13/Tiny digunakan untuk mereset kartu.

- Pin 3

  Pin ini merupakan pin CCCLK (Chip Card Clock) pada modul smartcard reader yang oleh mikrocontroller Renesas R8C13/Tiny digunakan untuk memberi clock pada kartu.

- Pin 4

  Pin ini adalah pin CCGND (Chip Card Ground) pada modul smartcard reader ke mikrocontroller Renesas R8C13/Tiny digunakan untuk pentanahan/ ground.

- Pin 6

  Pin ini berfungsi sebagai CCIO (Chip Card Input Output) untuk komunikasi serial pada modul smartcard reader ke mikrocontroller Renesas R8C13/Tiny .

- Pin 8

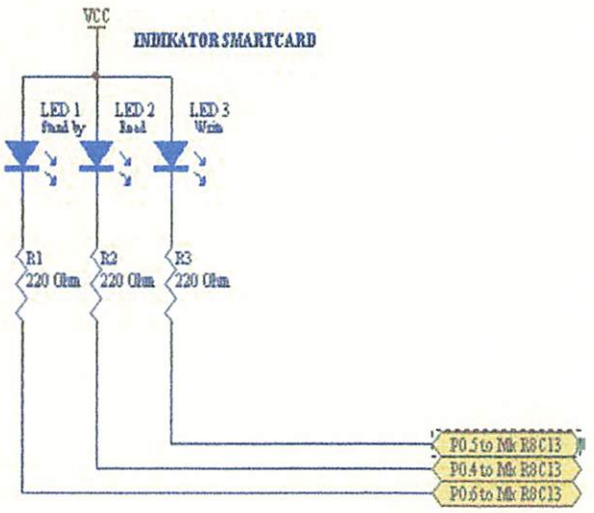
  Pin ini adalah pin CCIN pada modul smartcard reader ke mikrocontroller Renesas R8C13/Tiny berfungsi sebagai pendeteksian ada atau tidak adanya kartu.

3.4 Perancangan Rangkaian Indikator Smartcard

LED yang dipakai dalam perancangan ini adalah 3 buah Led indikator yang mempunyai fungsi untuk akses perintah interkoneksi smartcard reader dengan smartcard.Dimana 3 buah Led indikator yang digunakan yaitu:

- Led merah pada port 0.6 berfungsi sebagai indikator standby apabila koneksi antara smartcard belum terkoneksi dengan smartcard reader dan pada keadaan ON standby yang dikoneksikan pada Renesas R8C13/Tiny.

- Led kuning pada port 0.5 berfungsi sebagai indikator perintah write untuk smartcard melalui PC (Personal Computer) dengan melalui database yang diaplikasikan dimana terkoneksikan pada Renesas R8C13/Tiny.
- Led hijau pada port 0.4 berfungsi sebagai indikator read untuk smartcard melalui PC (Personal Computer) dengan melalui database yang diaplikasikan dimana terkoneksikan pada Renesas R8C13/Tiny.



Gambar 3.3 Rangkaian Indikator Smartcard

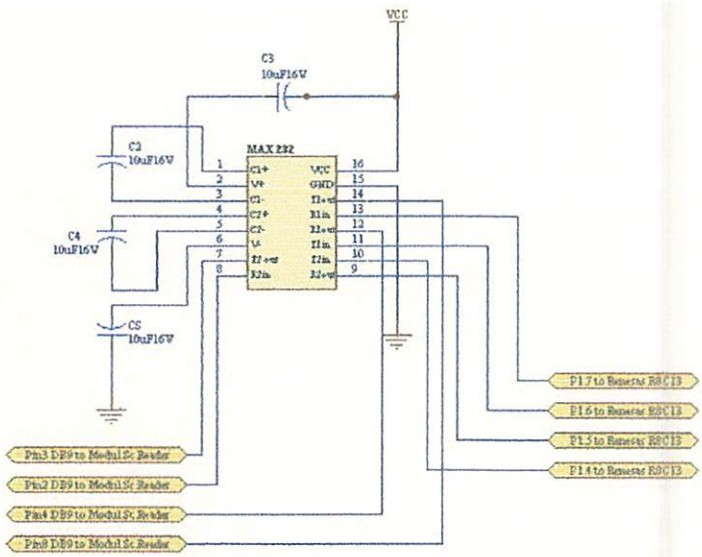
(Sumber: Perancangan Alat)

3.5 Rangkaian Antar Muka RS-232

Pada perencanaan hubungan antara *MCU* dan *Modul Smartcard ACR30* menggunakan komunikasi data secara *serial*. Adapun kaki/ pin-pin yang dipakai adalah

- pin 2 pada DB9 sebagai Rx.
- pin 3 pada DB9 sebagai Tx.
- Pin 4 pada DB9 Sebagai DTR
- Pin 5 pada DB9 sebagai ground
- Pin 8 pada DB9 sebagai CTS

Level tegangan dari RS-232 harus disesuaikan ke level tegangan TTL menggunakan IC MAX 232. Kecepatan transfer data per *bit* menggunakan 9600 Kbps. Rangkaian Interface RS-232 diperlihatkan pada gambar 3.4

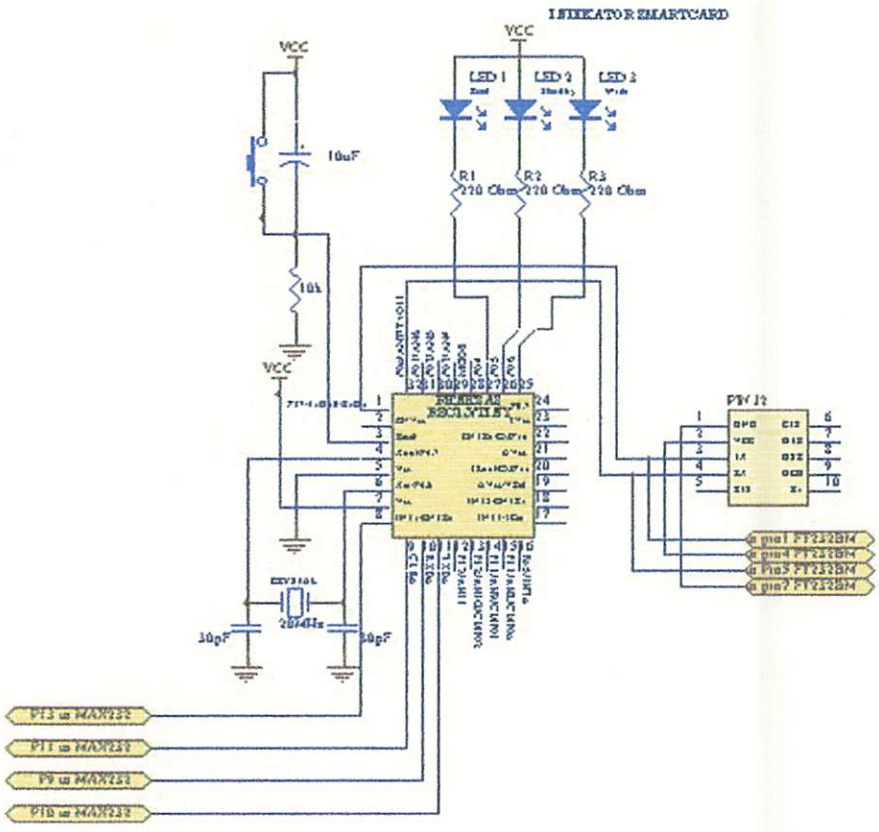


Gambar 3.4 Rangkaian Antar Muka RS-232.

(Sumber: Perancangan Alat)

3.6 Mikrokontroller Renesas R8C13/ TINY

Mikrokontroller Renesas R8C13/ TINY adalah suatu chip IC yang terdiri dari 32 pin, dalam perancangan alat ini pin-pin yang digunakan dapat dilihat dalam gambar dan dijelaskan sebagai berikut :



Gambar 3.5 Port pada MCU Renesas R8C13/Tiny yang dipakai pada sistem.

(Sumber: Perancangan Alat)

Fungsi port pada MCU yang digunakan pada alat adalah sebagai berikut :

- Port 0 memiliki fungsi sebagai berikut :
  - Port 0.0 digunakan sebagai input data (Rx) komunikasi Mikrocontroller Renesas R8C13/Tiny dengan Modul FT232BM.
  - Port 0.5 digunakan sebagai indikator write smartcard dengan nyala led kuning.
  - Port 0.6 digunakan sebagai indikator standby smartcard dengan nyala led merah.
  - Port 0.7 digunakan sebagai indikator read smartcard dengan nyala led hijau.
- Port 1 memiliki fungsi sebagai berikut :
  - Port 1.4 digunakan sebagai output data (Tx) komunikasi Mikrocontroller Renesas R8C13/Tiny dengan RS232.
  - Port 1.5 digunakan sebagai input data (Rx) komunikasi Mikrocontroller Renesas R8C13/Tiny dengan RS232.
  - Port 1.6 digunakan sebagai DTR komunikasi Mikrocontroller Renesas R8C13/Tiny dengan RS232.
  - Port 1.7 digunakan sebagai CTS komunikasi Mikrocontroller Renesas R8C13/Tiny dengan RS232.
- Port 3 memiliki fungsi sebagai berikut :
  - Port 3.7 digunakan sebagai output data (Tx) komunikasi Mikrocontroller Renesas R8C13/Tiny dengan Modul FT232BM.

- Port 4 memilki fungsi sebagai berikut :
  - Port 4.7 dengan port 4.6 disambungkan dengan rangkaian osilator.

3.6.1 Rangkaian Reset

Untuk me-*reset* mikrokontroler Renesas R8C13/Tiny, maka pin RST diberi logika tinggi selama sekurangnya dua siklus mesin (24 periode osilator). Untuk membangkitkan sinyal *reset* kapasitor dihubungkan dengan V_{CC} dan sebuah resistor yang dihubungkan ke *ground.*

Karena kristal yang digunakan mempunyai frekuensi sebesar 20 MHz, maka satu periode dapat dihitung dari persamaan :

$$T = \frac{1}{f_{XTAL}} = \frac{1}{20MHz} s = 5 \times 10^{-8} \text{s}$$

Sehingga waktu minimal logika tinggi yang dibutuhkan untuk me*reset* mikrokontroler dapat dihitung menggunakan persamaan :

$t_{reset(min)}$ = T x periode yang dibutuhkan

Jadi mikrokontroler membutuhkan waktu minimal 1.2 μs untuk me*reset.* Waktu minimal inilah yang dijadikan pedoman untuk menentukan nilai R dan C. Dari Persamaan dengan menentukan nilai R =10 kΩ, dan C = 10 μF, maka:

$$f_0 = \frac{1}{1,1.R.C}$$

$$f_o = \frac{1}{1{,}1.10.10^{3}.10.10^{-6}}$$

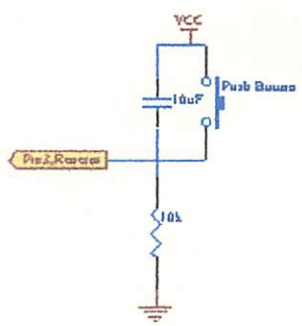
$f_o = 90{,}9$ Hz

Maka periode clock : $T = \frac{1}{f}$

$$T = \frac{1}{90{,}9}$$

T = 0,011 detik

Rangkaian reset ditunjukkan dalam gambar di bawah ini :



Gambar 3.6 Perencanaan Rangkaian Reset.

(Sumber: Perancangan Alat)

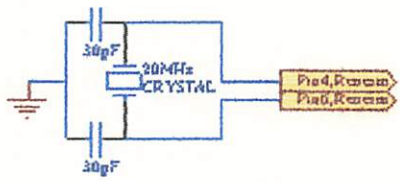
3.6.2 Rangkaian Clock

Kecepatan proses yang diperlukan oleh mikrokontroller Renesas R8C13/Tiny ditentukan oleh sumber *clock* yang mengendalikan mikrokontroller tersebut. Mikrokontroller Renesas R8C13/Tiny memiliki internal *clock* generator yang berfungsi sebagai sumber *clock* yang diperlukan. Untuk kristal *clock* dipasang Kristal dan resonator

keramik yang berfungsi sebagai pembangkit *clock* osilator yang ada pada mikrokontroller.

Rangkaian ini terdiri dari dua buah kapasitor dan sebuah kristal. Untuk mengendalikan frekuensi osilatornya cukup dengan menghubungkan Kristal pada pin 4 ($P4.7/X_{out}$) dan pin 6 ($P4.6/X_{in}$) serta dua buah kapasitor ke *ground.*

Dalam minimum kristal ini, menggunakan kristal 20 Mhz dan $C_1 = C_2$ yaitu sebesar 30 pF. Dengan rangkaian sebagai berikut :



Gambar 3.7 Perencanaan Rangkaian *Clock*.

(Sumber: Perancangan Alat)

Dengan menggunakan nilai kristal dan kapasitor di atas maka dapat dihitung waktu yang diperlukan untuk 1 siklus mesin yaitu :

Diketahui : F = 20 MHz

$$T = \frac{1}{f}$$

Maka $T = \frac{1}{20\ Mhz} = \frac{1}{20}$ µs

Maka untuk 1 siklus mesin dari mikrokontroller Renesas R8C13/Tiny adalah sebesar :

$$T_m = 12 \times T$$

$$= 12 \times \frac{1}{20}\ \mu s$$

$$= 0{,}6\ \mu s$$

3.7 Perencanaan Komunikasi Serial

Pada perencanaan komunikasi serial alat, digunakan sebuah modul FT232BM PC Link-USB sebagai *interface* komunikasi serial antara MCU dengan PC via port *USB*. Untuk melaksanakan proses komunikasi data antara keduanya diperlukan syarat-syarat yang harus dipenuhi yakni, pengaturan *baud rate* serta pengaturan secara *software*. Jenis data yang akan dikirim adalah dalam bentuk data biner (bit per bit transfer) dengan satuan *baud rate*. Serial kontrol (SCON) merupakan register khusus pengontrol kerja port serial, diset untuk mentransmisikan data 8 bit UART (*Universal Asynchronous Receiver Transmitter*) yang merupakan standart komunikasi data dengan *baud rate* yang dapat diatur. Penentuan *baud rate* tersebut dilakukan dengan pengesetan. Timer atau *counter* 1 high bit (TH1) bila diinginkan *baud rate* 9600 bps dan dimana *frekuensi eksternal* (fEXT) 20Mhz maka :

$$\text{Baud rate} = \frac{fEXT}{\text{Bit Rate} \times 16} - 1$$

$$\text{Baud rate} = \frac{20 \times 10^6}{9600 \times 16} - 1$$

$$\text{Baud rate} = \frac{20 \times 10^6}{153600} - 1$$

$$\text{Baud rate} = 130{,}21 - 1$$

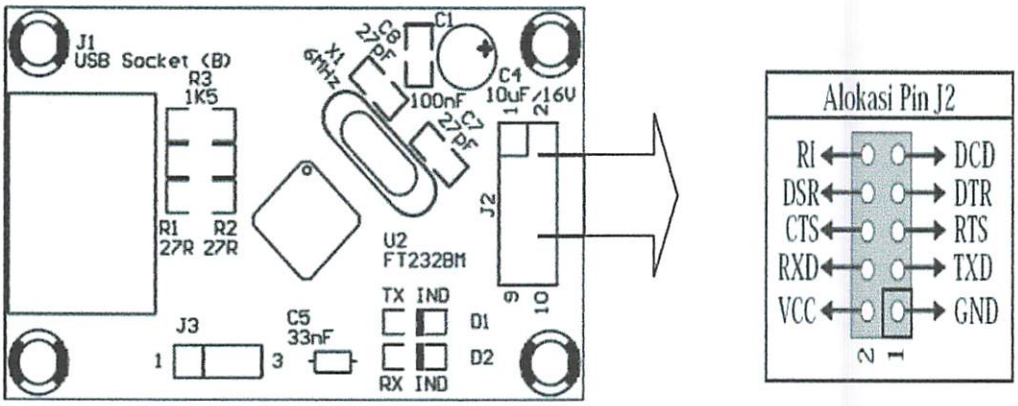
Baud rate = 129,21

BRG Seting Value = 129 (81_{16}) atau u1brg = 129 dan u1c1 = 0x05h

Jika *baud rate* besarnya adalah 9600 bps data membutuhkan waktu 0,05us. Karena satu karakter data terdiri atas 10 bit atau $10x0,05.10^{-6}$ = 0,5 ms. Sehingga kecepatan transfernya 1/0,5 us atau 2 karakter/us.

Antarmuka serial menggunakan modul FT232BM. Modul ini memungkinkan kita berkomunikasi serial melalui port USB. Karena saluran data keluaran dari modul ini menggunakan standart TTL maka kita tinggal menghubungkan port Rx dan Tx modul ini dengan Mikrokontroller. Hal ini dapat dilakukan karena port serial Renesas R8C13/Tiny juga menggunakan standart TTL yang sama. Dalam standart TTL logic 0 (low) dinyatakan sebagai tegangan antara 0 volt sampai 0.8 volt, dan logic 1 (high) dinyatakan sebagai tegangan antara 2.5 volt sampai 5 volt.

Tata letak komponen :



Gambar 3.8 Antarmuka dari modul USB menggunakan level TTL dan terhubung ke header dengan label J2.

(Sumber : www.innovativeelectronic.com)

Pin-pin yang digunakan dalam perancangan ini:

- Pin 1 GND (Ground)

  Pin 1 adalah pin yang digunakan sebagai ground sedangkan untuk Renesas R8C13/Tiny Gnd berada pada pin 5.

- Pin 2 VCC (+ 4,4 – 5,25 Volt)

  Modul FT 232 BM ini di operasikan dengan tegangan supply + 4,4— 5,25 Volt dan sedangkan untuk Renesas R8C13/Tiny Vcc berada pada pin 7.

- Pin TXD

  Pin TXD dialokasi pin J2 dan pada Renesas R8C13/Tiny Vcc berada pada pin 1,11,32 digunakan sebagai pengiriman data serial.

- Pin RXD

  Pin RXD dialokasi pin J2 dan pada Renesas R8C13/Tiny Vcc berada pada pin 1,10 digunakan sebagai penerima data serial.

3.8 Perancangan Perangkat Lunak

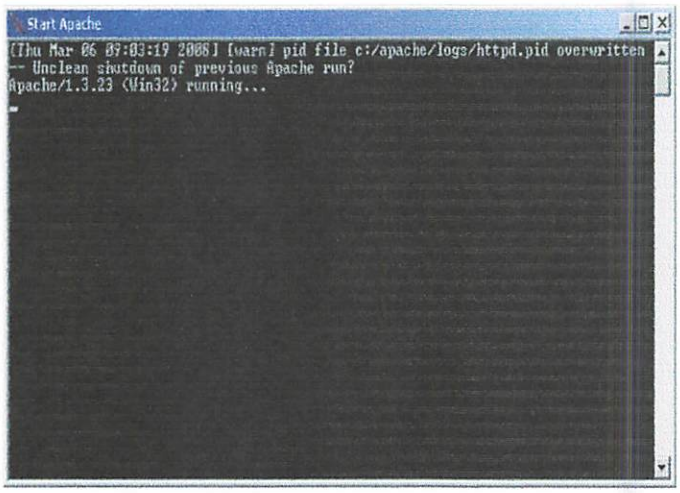
Setelah semua perangkat keras telah selesai dikerjakan pada tahap selanjutnya perangkat lunak (Sofware) yang akan menangani sistem rangkaian .Pada perangkat lunak inilah kita dapat menentukan bagaimana sistem rangkaian ini akan bekarja,pada bagian inilah semua tata kerja rangkaian ditentukan .dalam merancang perangkat lunak ini ,mengunakan dua buah sofware yaitu sofware pada mikrokontroler dan sofware pada delphi yaitu :

- Pada pemrograman di mikrokontroler mengunakan renesas R8C13/Tiny mengunakan bahasa C dengan compiler yang dipaket bersama pada suatu IDE yaitu HEW (High-Performance Embedded Workshop).
- Pada PC (komputer) mengunakan sefware delphi 7 di dalam delphi7 ini ada beberapa komponen yang di gunakan untuk mengakses/menghubungkan sofware pada mikrokontroler dengan PC baik itu dalam menampilkan data maupun dalam mengakses database. Komponen tersebut adalah :
    - Main menu : komponen ini terletak pada bagian standart yang fungsinya untuk mendesain dan menciptakan menu bar yang ada pada form.
    - Table : komponen ini terletak pada bagian BDE yang funsinya untuk menghubungkan tabel pada suatu database dengan program yang dibuat.
    - DataSource : komponen ini terletak pada bagian Data Access yang fungsinya untuk menghubungkan komponen Table atau Query dengan komponen tempat data akan ditampilkan.
    - Query : komponen ini terletak pada bagian BDE yang fungsinya untuk membuat dan mengeksekusi SQL query pada SQL Server Database atau Database lokal.
    - DBGrid : komponen ini terletak pada Data Controls yang fungsinya untuk menampilkan data-data dalam bentuk baris dan kolom.
    - DBNavigator : komponen ini terletak pada Data Controls yang fungsinya untuk membuat pengontrol yang bisa menavigasi database dan mempunyai kemampuan untuk mengubah data tersebut

- Timer : komponen ini terletak pada System yang fungsinya untuk mengaktifkan prosedur, fungsi, atau event dengan suatu internal waktu.
- Comport : komponen ini terletak pada CPortLib yang fungsinya untuk menyeting COM, Baud rate, Data bit, Stop bit, Parity dan Flowcontrol.

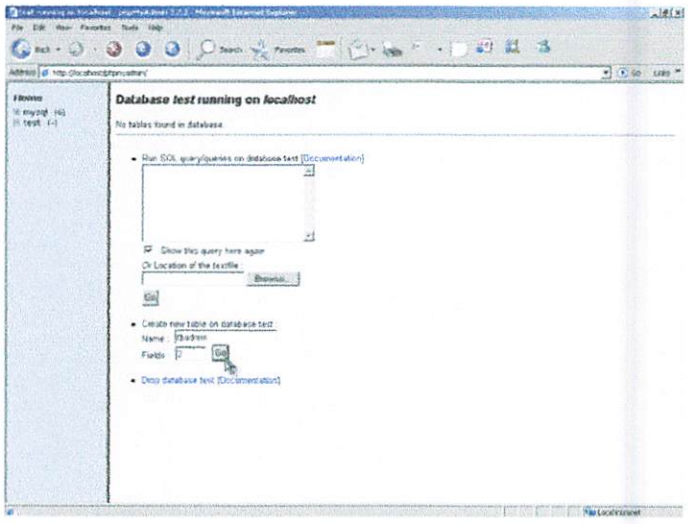
3.7.1 Perencanaan Form

Perencanaan form ini merupakan perencanaan tampilan program yang nantinya akan ditampilkan pada PC. Pada penyusunan tampilan ini membutuhkan beberapa komponen Borland Delphi 7. Diantaranya terdiri atas DBGrid, Table, Datasource, DBNavigator. DBNavigator digunakan untuk mengedit isi database yang ditampilkan oleh DBGrid. DBGrid digunakan untuk menampilkan database pada form Delphi yang dihubungkan dengan database dengan menggunakan komponen table dan datasource. Sedangkan komponen data source digunakan untuk menghubungkan sumber database dengan program yang mana dalam hal ini database di hubungkan dari MySQL ke program dengan menggunakan komponen connector ODBC. Pada perencanaan pembuatan website hasil pemungutan suara ini digunakan Apache 2.0.51 sebagai software untuk server dalam menyediakan semua isi web browser yang berupa halaman-halaman HTML. Apache yang digunakan untuk server ini terdapat pada software bundled yaitu XAMPP versi 1.4.8 yang juga memuat PHP dan MySQL.



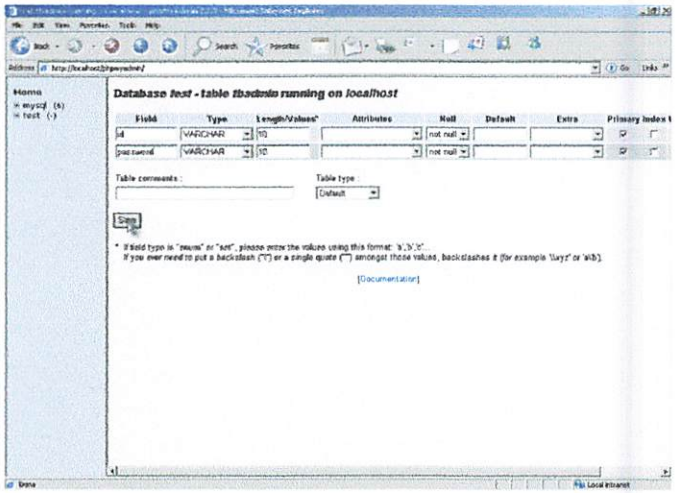
Gambar 3.9 Tampilan Start Apache

(Sumber : Perancangan Database)



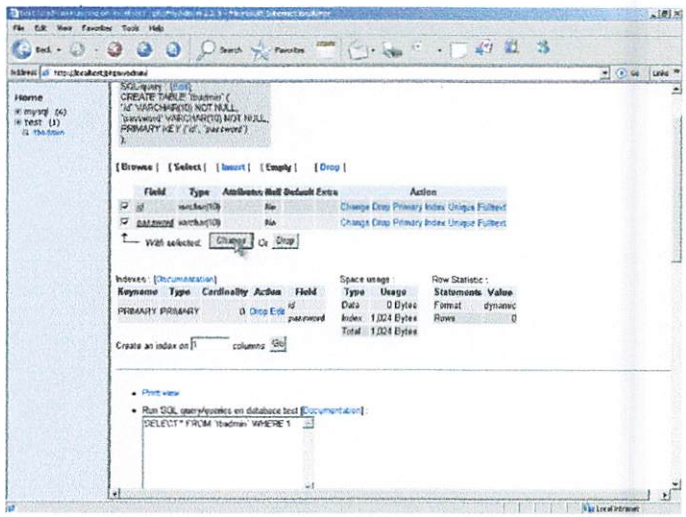
Gambar 3.10 Tampilan Pembuatan Table Database MySql

(Sumber : Perancangan Database)



Gambar 3.11 Tampilan Pengisian Table Database MySql

(Sumber : Perancangan Database)

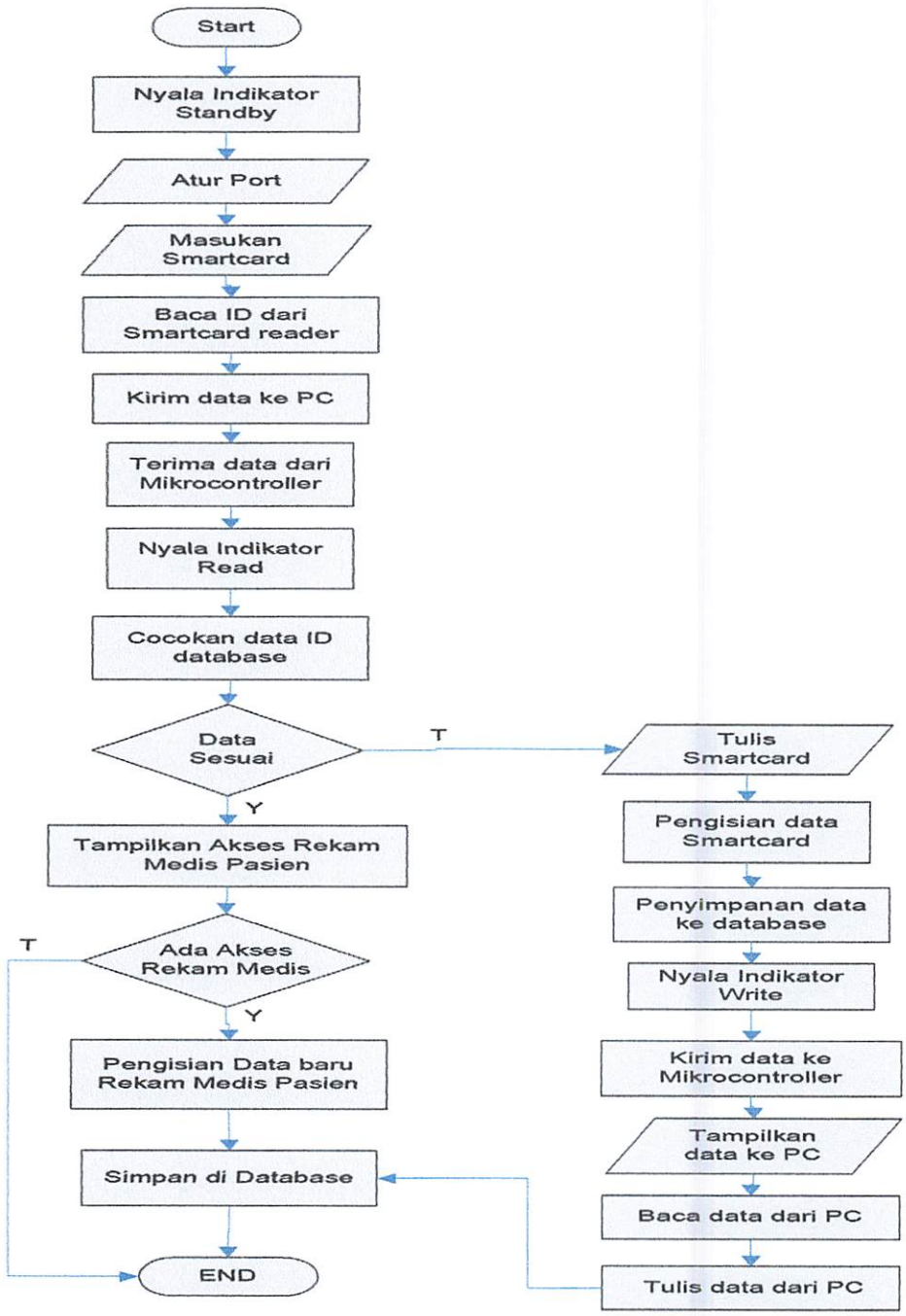


Gambar 3.12 Tampilan Hasil Pembuatan Table Database MySql

(Sumber : Perancangan Database)

3.9 Flow Chart

Cara kerja dari perangkat keras (*hardware*) sebagai berikut:



Gambar3.13 Flow Chart Keseluruhan Sistem

BAB IV

PENGUJIAN SISTEM DAN PEMBAHASAN

4.1 Pendahuluan

Pada bab ini dibahas tentang pengukuran dan pengujian alat yang dirancang, yang meliputi perangkat keras (*hardware*) dan perangkat lunak (*software*). Untuk mengetahui sistem yang dirancang sesuai dengan fungsi yang diharapkan, dilakukan pengujian terhadap sistem tersebut baik secara keseluruhan maupun subsistemnya. Berikut merupakan penjelasan mengenai prosedur pengukuran dan data hasil pengujian.

- Bagian-bagian perencanaan alat yang diuji meliputi perangkat keras (*hardware*) antara lain :

    1. Pengujian Akses *Smartcard* ke *Smartcard Reader*
    2. Pengujian Tegangan keluaran *Smartcard* reader ke Mikrocontroller
    3. Pengujian Indikator *Smartcard*
    4. Pengujian Modul USB

- Bagian-bagian perencanaan alat yang diuji meliputi perangkat lunak (*software*) antara lain :

    1. Pengujian Percobaan Transfer data antara Alat dengan PC (*Personal Computer*).
    2. Pengujian Tampilan Sistem Aplikasi Akses Rekam Medis.

Alat-alat bantu yang digunakan dalam pengujian adalah sebagai berikut:

1. Power supplier
2. Osiloskop
3. Multimeter digital.
4. Kartu Smartcard Type Siemens 4442
5. PC P4 Celeron 1.8GHz
6. Software Mysql connector odbc 3.51.12 win32
7. Software Phptriad2-2-1.exe
8. Perangkat Lunak Pemrograman Borland Delphi7

4.2 Pengujian Perangkat Keras (*Hardware*)

4.2.1 Pengujian Akses *Smartcard* ke *Smartcard reader*

Pengujian akses smartcard ke reader ini dilakukan untuk melihat adanya sinyal *clock* pada smartcard. Untuk melihat bentuk gelombang ini dilakukan dengan menggunakan osiloskop yang dimana ketika card telah terkoneksi dengan header dan pengiriman data dilakukan maka proses clockcard akan terjadi.Proses clockcard dapat dilihat pada lampiran gambar 1.a dan 1.b.

4.2.2 Pengukuran Tegangan

Pada pengujian pengukuran tegangan output dari smartcard reader ke mikrocontroller Renesas R8C13/Tiny digunakan multimeter digital untk mengetahui tegangan input dan output yang dimana ketika tegangan input dari power supply dialirkan pada reader dan menuju ke IC max232 dan tegangan dikonversikan ke mikrocontroller.

Hasil pengukuran tegangan dapat dilihat pada gambar 1.c yang dimana terdapat pada lembar lampiran. Proses tegangan input dan output yang dilakukan dapat didata sebagai berikut :

Tabel 4.1 Hasil pengukuran tegangan

Hasil pengukuran Tegangan	Tegangan pada Smartcard reader	Tegangan untuk Mikrocontroller
Vin	- 8,82 Volt	4,88 Volt
Vout	- 7,19 Volt	4,86 Volt

4.2.3 Pengujian Indikator *Smartcard*

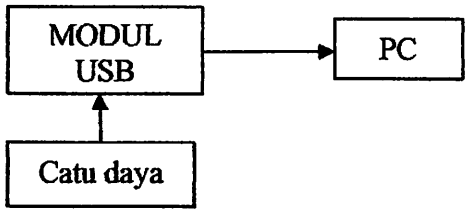
Pada pengujian Indikator smartcard diakses dari perintah smartcard reader ke mikrocontroller Renesas R8C13/Tiny dan dimana akses indikator diproses oleh mikrocontroller dari hardware pada proses koneksi smartcard dengan smartcard reader dan kemudian proses transmisi data yang dilakukan maka didapatkan data sebagai berikut:

Tabel 4.2 Hasil pengujian indikator smartcard

Kondisi	Indikator 1 Led merah	Indikator 2 Led kuning	Indikator 3 Led hijau	Kondisi lampu	Lama waktu
Standby	0	1	0	Nyala led Kuning	± 4 detik
Write	1	0	0	Nyala led merah	± 15detik
Read	0	0	1	Nyala led hijau	± 6 detik

4.2.4 Pengujian Modul USB (*Universal Serial Bus*)

Tujuan dari pengujian ini adalah untuk mengetahui apakah Modul USB bisa digunakan untuk mengirim dan menerima data atau tidak. Adapun cara pengujianya dilakukan dengan cara memilih com yang dideteksi oleh PC kemudian mencoba melakukan pengiriman data melalui program sederhana yang telah dibuat ,data akan dikirim melalui kabel USB menuju Modul USB dengan menggunakan indikator apabila data di kirim dari PC ke USB maka led indikator pada modul (Rx) akan nyala dan sebaliknya pada saat data dikirim kembali dari USB ke PC maka indikator pada modul (Tx) akan menyala,dengan prosedur pengujian seperti dibawah ini :



Gambar 4.1 Blok Pengujian Modul USB

1. Menghubungkan rangkaian Modul USB ke PC menggunakan kabel USB.
2. Menginstal driver modul USB.
3. Membuka program pada delphi

Setelah proses penginstallan selesai maka untuk melakukan pengujian terhadap modul USB, digunakan sebuah program simple delphi yang dibuat agar dapat digunakan untuk menguji modul USB tersebut yaitu :

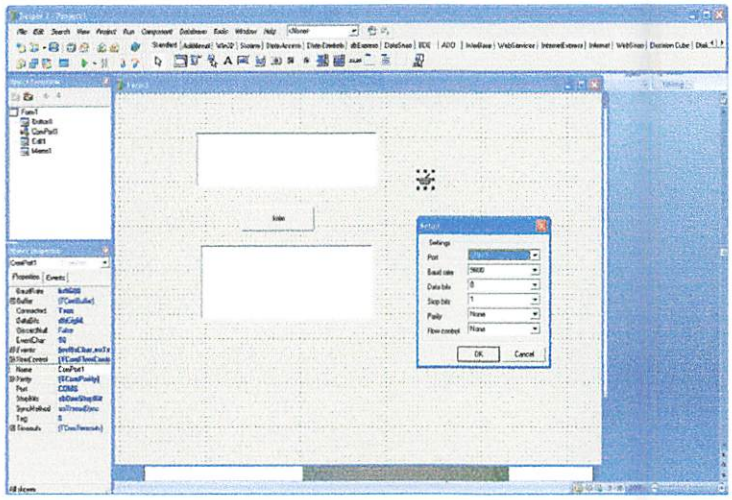
❖ Progam Uji Komunikasi Modul USB :

" Cuplikan program uji komunikasi serial di komputer menggunakan program Delphi 7.0 "

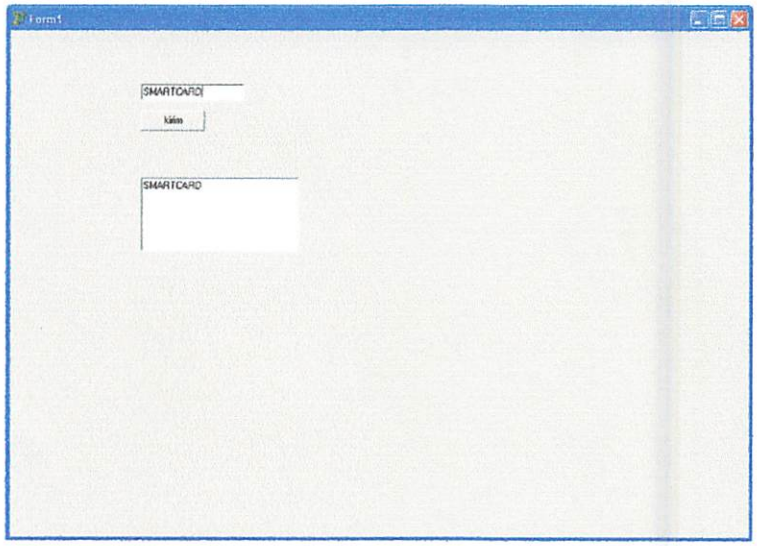
```
procedure TForm1.Button1Click(Sender: TObject);
begin
ComPort1.WriteStr('smartcard')
end;
procedure TForm1.ComPort1RxChar(Sender: TObject; Count:
Integer);
var data:string;
begin
ComPort1.ReadStr(data,count);
Memo1.Text:=Memo1.Text+data;
end;
end.
```

❖ Sebelum program dijalankan terlebih dahulu kita menyeting com yang dideteksi oleh PC seperti gambar 4.2 setelah itu program di runing tampilan pada saat program dijalankan seperti gambar 4.3 dan tampilan pada Modul USB pada saat data dikirim seperti gambar 4.4:

❖ Pada proses penjumperan Rx dan Tx pada Modul USB dapat dilihat pada halaman lampiran gambar.



Gambar 4.2 Tampilan Delphi pada saat Penyetinggan Komponen Comport.



Gambar 4.3 Tampilan Delphi pada saat Program dijalankan.

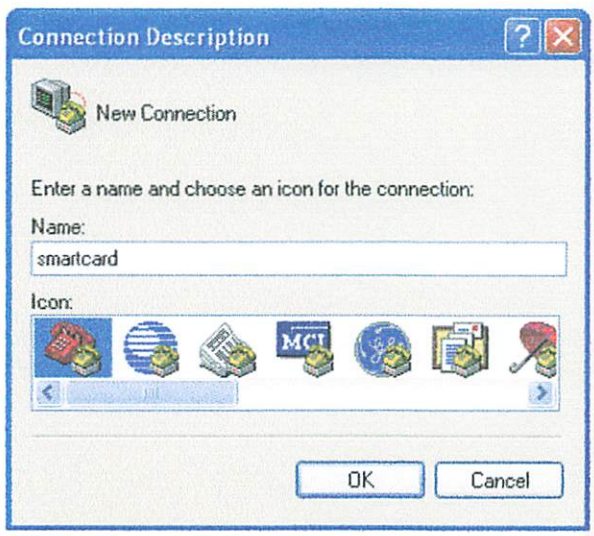
4.3 Pengujian Perangkat Lunak (*Software*)

4.3.1 Pengujian Percobaan Transfer data antara Alat dengan PC (*Personal Computer*).

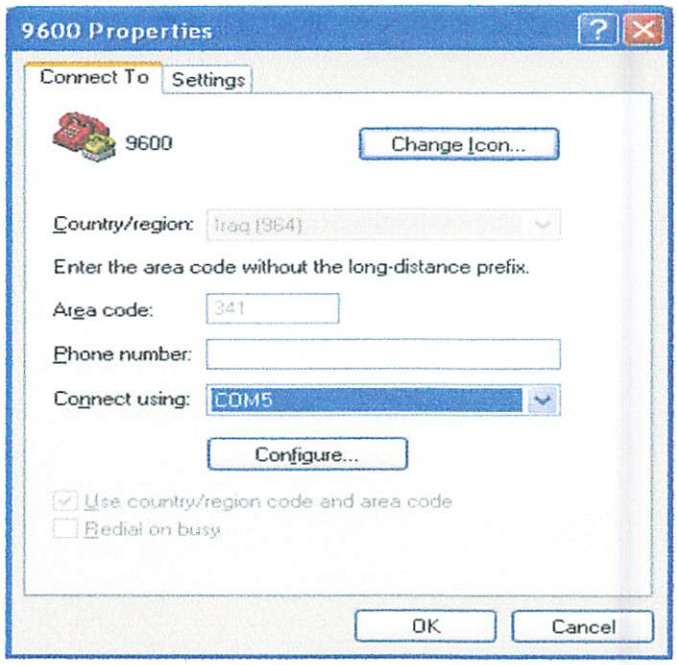
Pada pengujian percobaan transfer data antara *hardware* ke *software* dimana akses data pada pengisian smartcard harus sinkron dengan data Id pada program aplikasi *software* yang ketika jika akses data dari *smartcard* teridentifikasi dengan software maka akan terdeteksi secara automatis data input smartcard baik yang sudah terisi maupun yang belum terisi.

4.3.1.1 Prosedure pengujian transfer data antara lain :

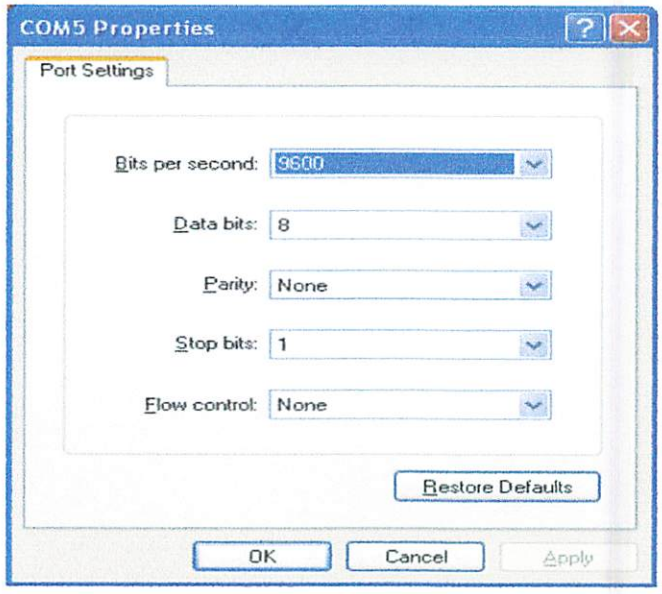
- Menghubungkan smartcard reader ⟶ Mikrokontroler ⟶ Indikator smartcard ⟶ Modul USB ⟶ PC.
- Membuka Hyper Terminal ⟶ (Start ⟶ AllProgram ⟶ accessories ⟶ Comunications ⟶ hyperterminal).
- Memberi nama dan memilih *icon* pada *Connection Desert.*



Gambar 4.4 Kotak Dialog *Connection Description*



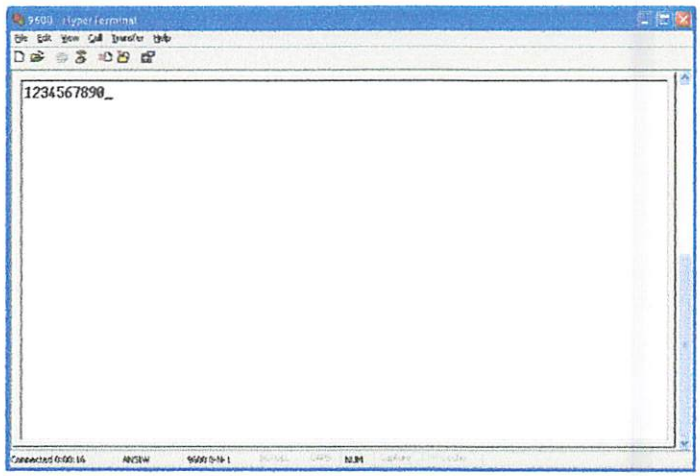
Gambar 4.5 Kotak *Dialog Connect To.*



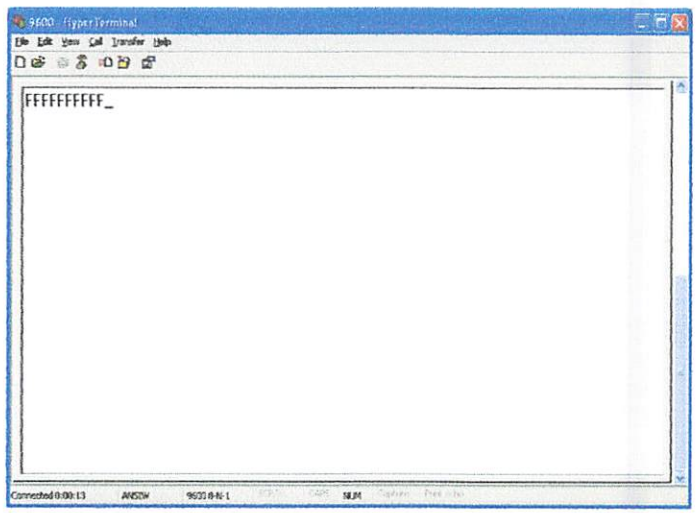
Gambar 4.6 Kotak Dialog COM 6 Properties

- Pada COM 5 *properties* mengubah *bits, rate per second* menjadi 9600 dan *flow control* menjadi *none*.

- Memasukkan 2 buah kartu smartcard seperti pada gambar 4.18 yang telah terisi data dan yang belum terisi data pada Reader :
- Tampilan Hyper Terminal pada baudrate 9600 antara lain :

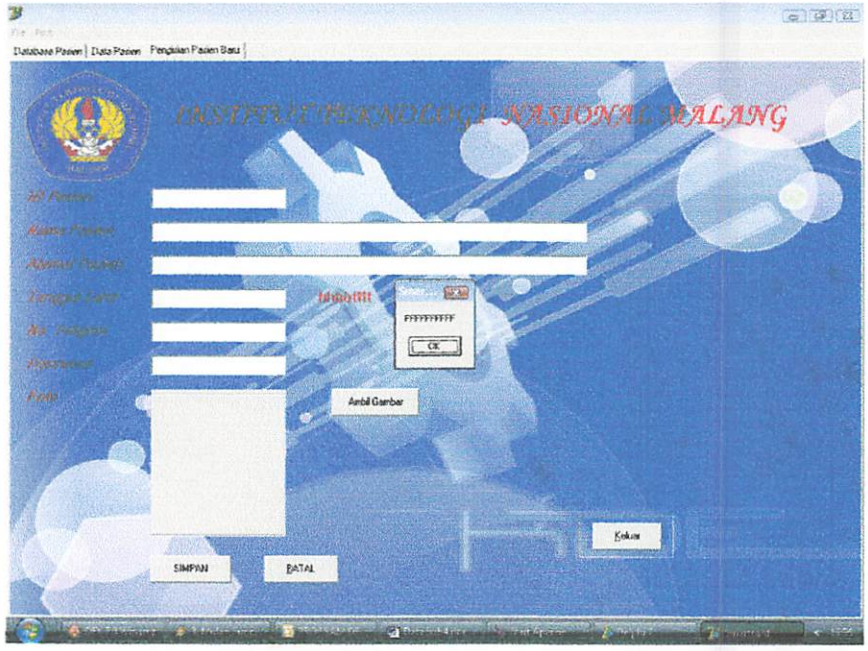


Gambar 4.7a Transmisi data *smartcard* yang telah terisi

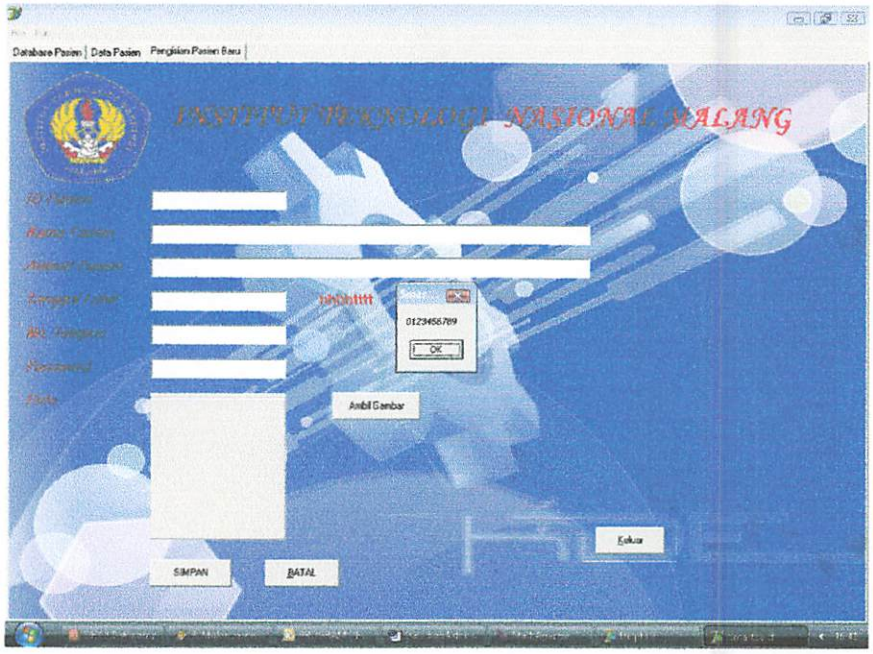


Gambar 4.7b Transmisi data *smartcard* yang kosong

➢ Tampilan *sinkronisasi software Delphi7* dengan hyper terminal :



Gambar 4.8a Transmisi data *smartcard* yang kosong



Gambar 4.8b Transmisi data *smartcard* yang telah terisi

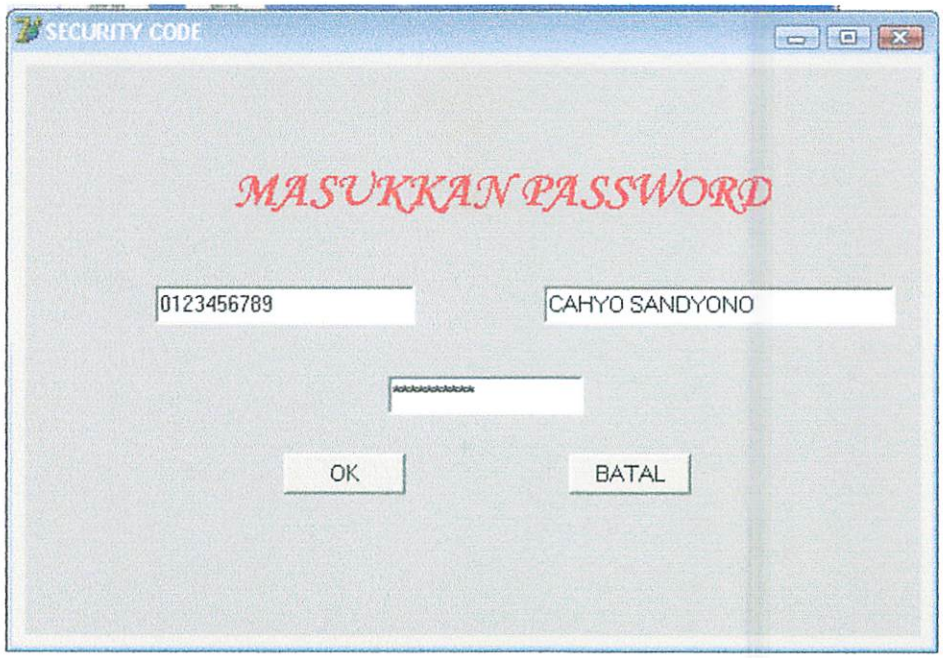
Tabel 4.3 Hasil Pengujian Sinkronisasi Transmisi data Smartcard

Pengujian Smartcard	Transmisi data id smartcard yang terkoneksi pada Hyperterminal	Transmisi data id smartcard yang terkoneksi pada PC
1	FFFFFFFFFF	FFFFFFFFFF
2	1234567890	1234567890
3	2345678901	2345678901
4	3456789012	3456789012
5	4567890123	4567890123

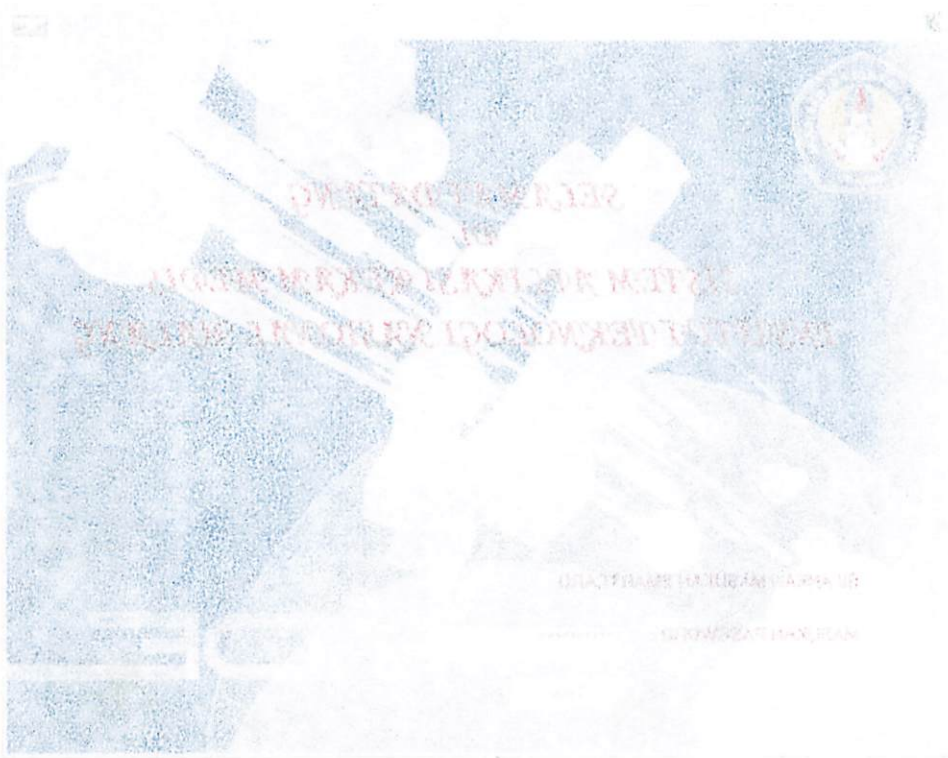
4.3.2 Pengujian Tampilan Form Sistem Aplikasi Akses Rekam Medis

Pada pengujian sistem aplikasi akses rekam medis digunakan program Delphi7 untuk akses programnya yang dimana pada hardware terkoneksikan dengan componen Cport yang mengakses komunikasi serial antara *hardware* dengan *software* Delphi7 yang dimana diaplikasikan ke Akses Rekam Medis. Dimana tampilan akses rekam medis terdapat beberapa form tampilan yang diaplikasikan pada sistem akses rekam medis yang dimana tampilan adalah sebagai berikut :

Gambar 4.9 Form Tampilan Utama

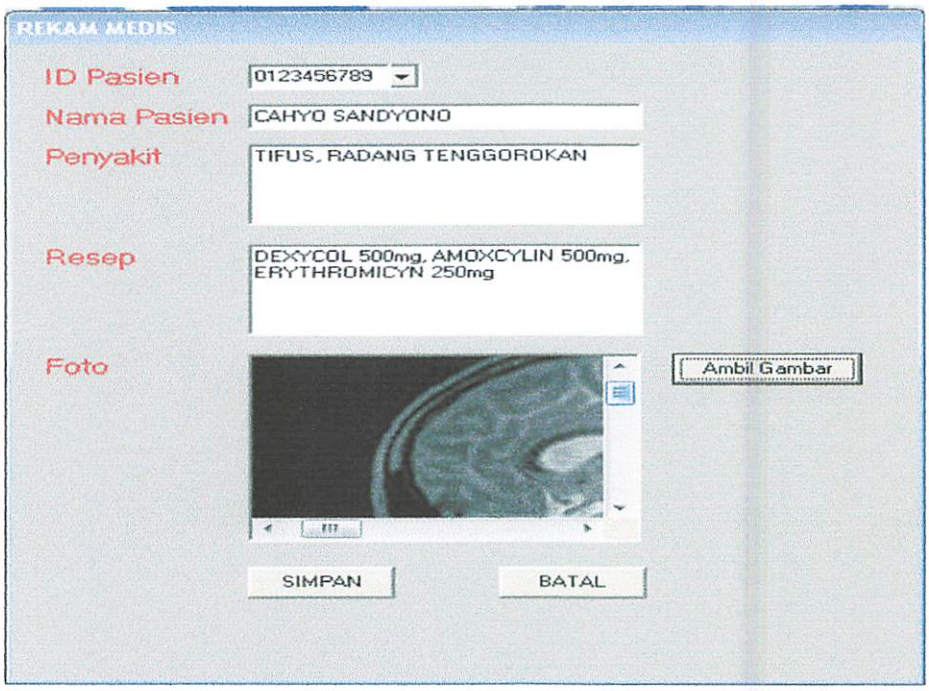


Gambar 4.10 Form Tampilan Kode Pengamanan ID

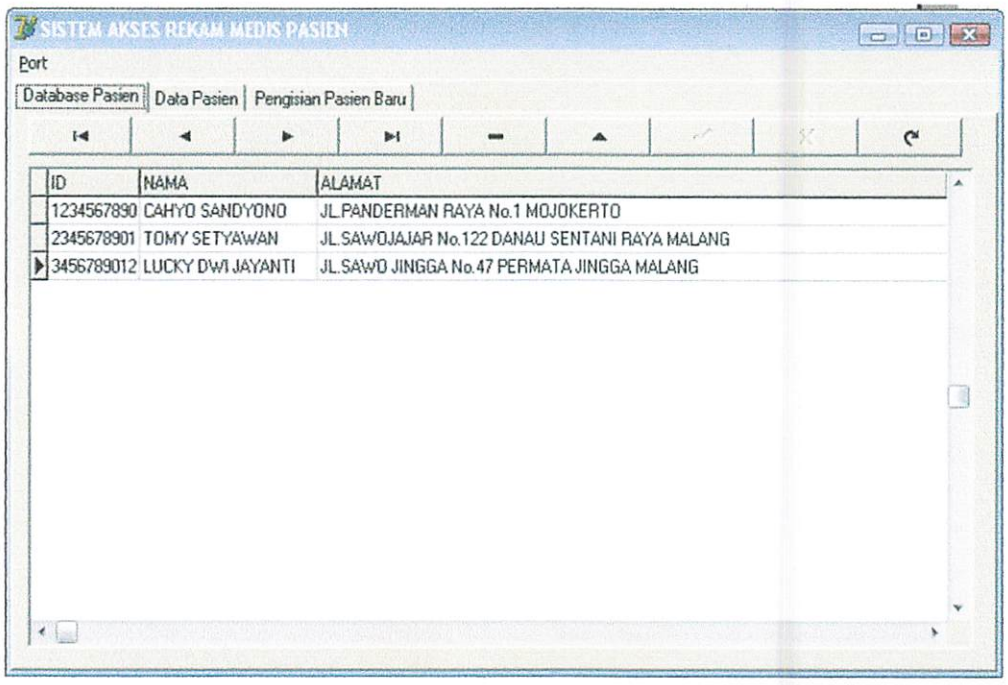


Gambar 4.11 Form Tampilan Pengisian Pasien Baru

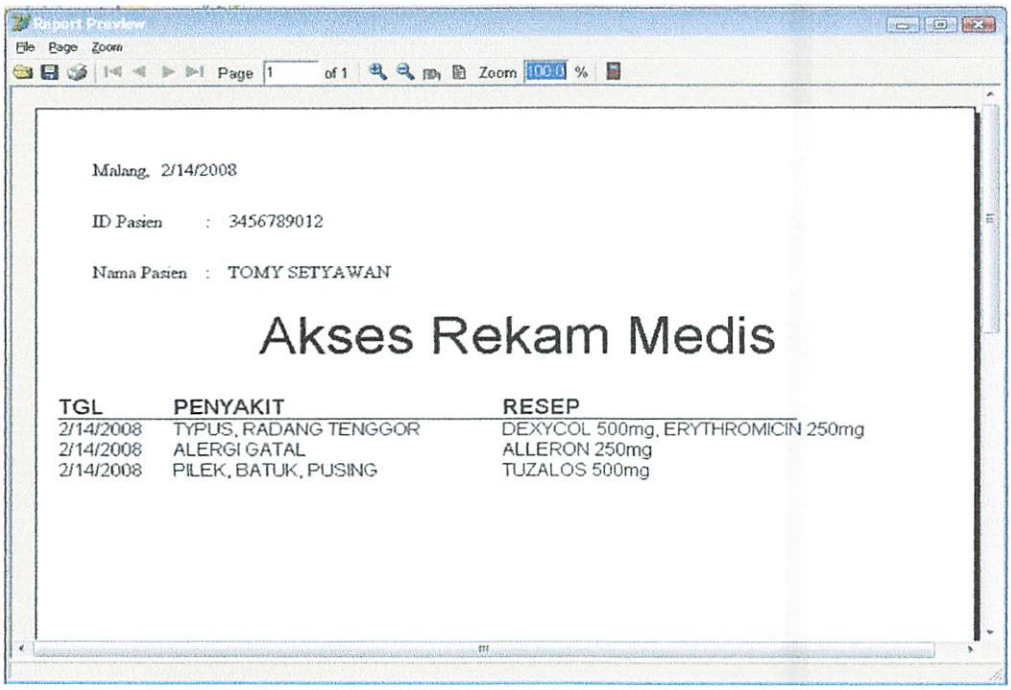
Gambar 4.12 Form Tampilan Data pasien



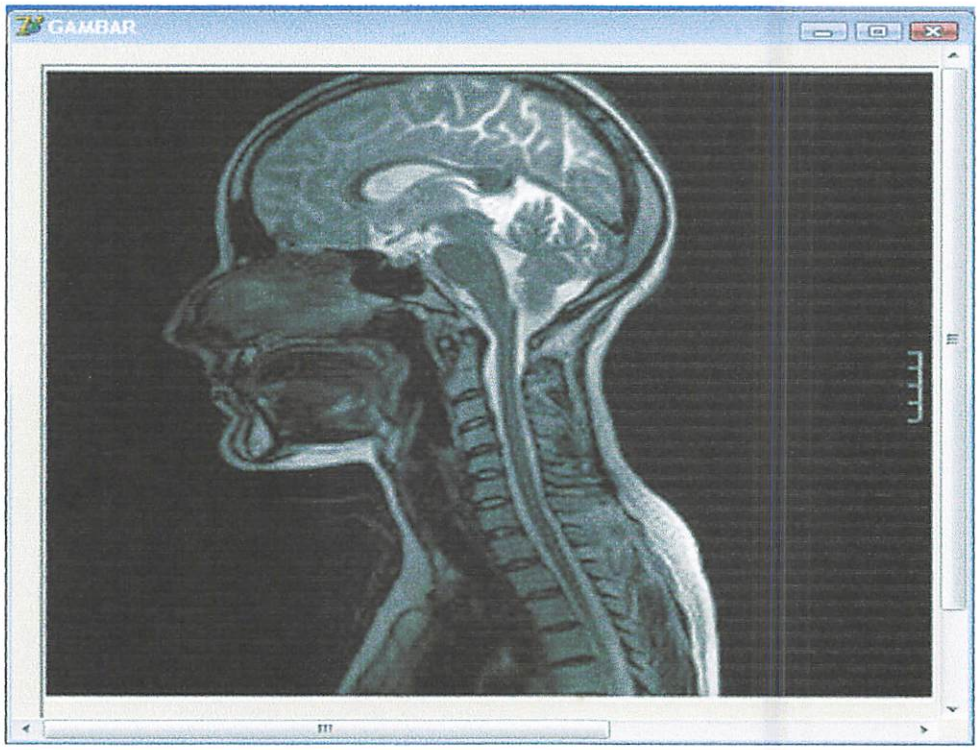
Gambar 4.13 Form Tampilan Akses Rekam Medis



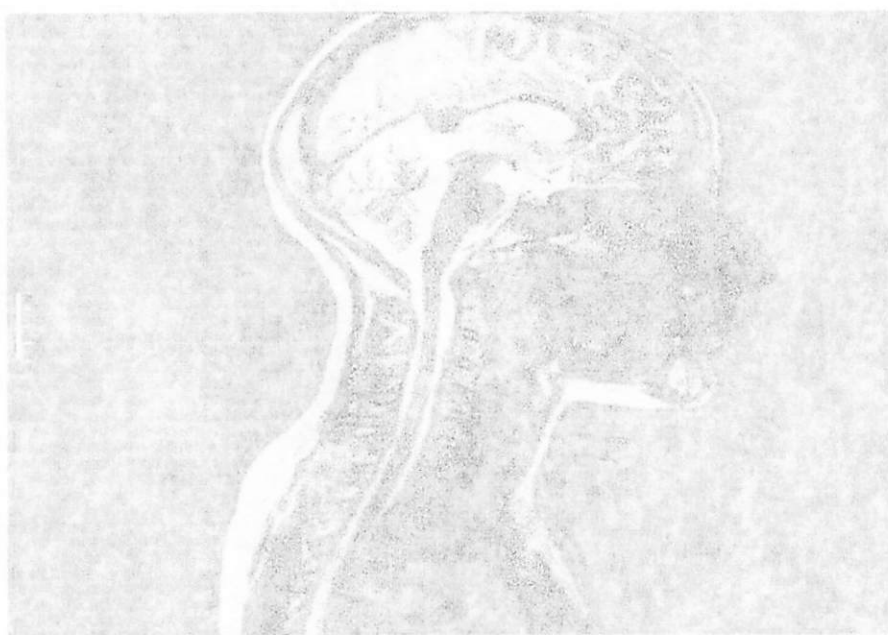
Gambar 4.14 Form Tampilan Database Pasien

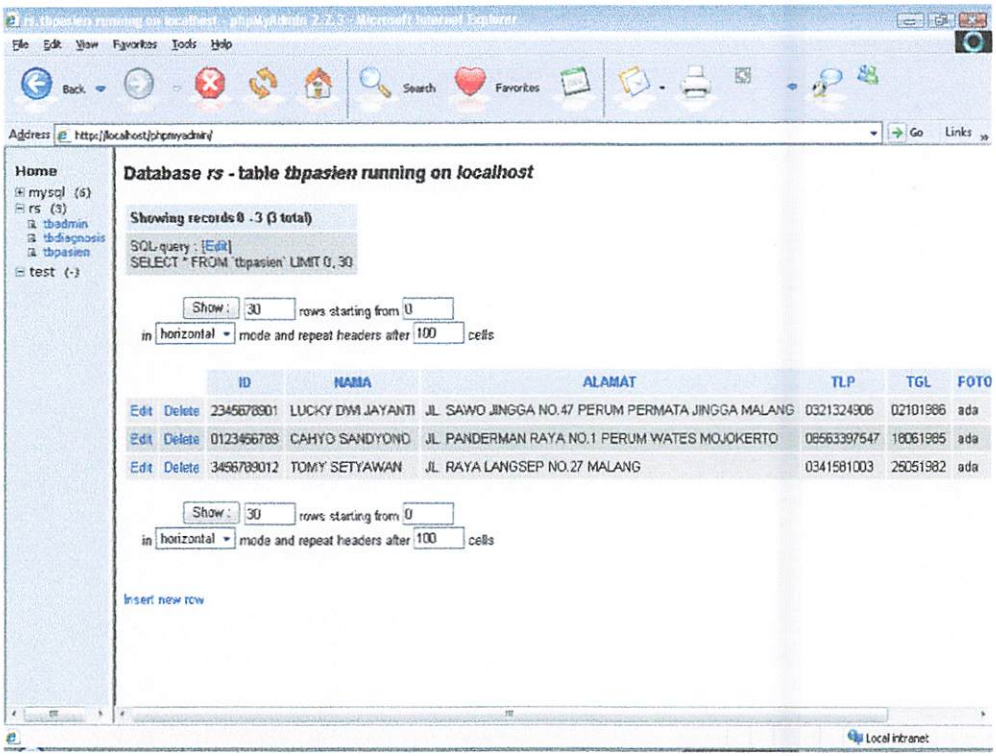


Gambar 4.15 Form Tampilan Print Report Database Pasien

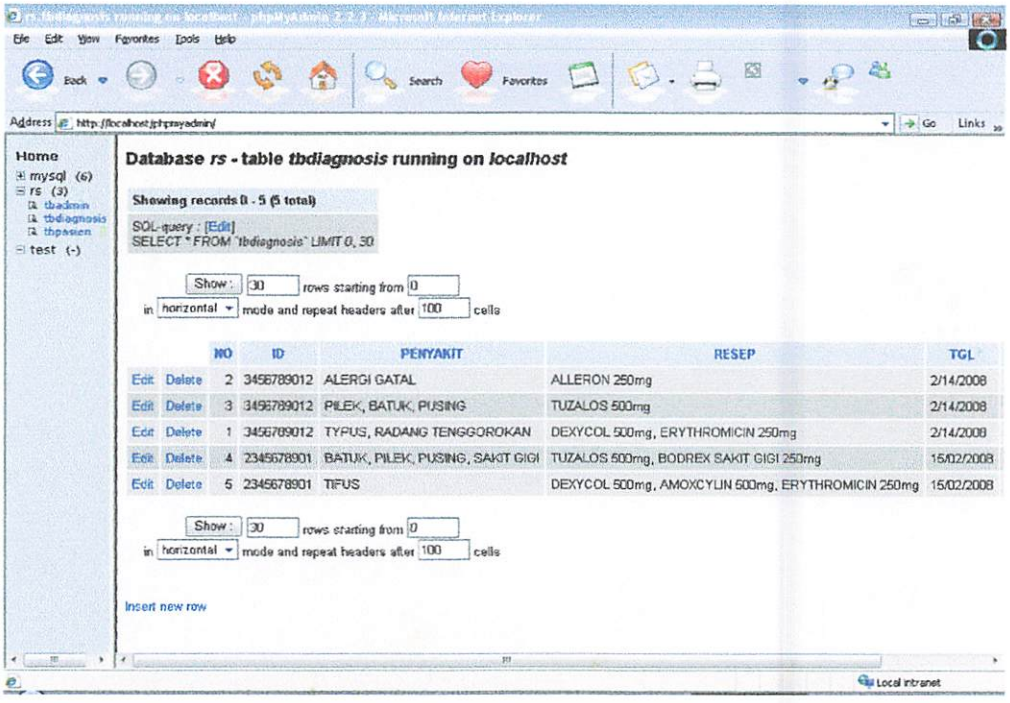


Gambar 4.16 Form Tampilan Pengisian Gambar Hasil Rontgen





Gambar 4.17 Form Tampilan Database Pasien



Gambar 4.18 Form Tampilan Database Akses Rekam Medis Pasien

BAB V

PENUTUP

5.1. Kesimpulan

Dari "Perancangan dan Pembuatan Modul Smartcard menggunakan Renesas R8C13/TINY untuk Akses Rekam Medis melalui USB" ini maka dapat diambil kesimpulan sebagai berikut:

1. Pada proses I/O smartcard mengasumsikan data 8 bit yang mengakses format standart card dan mampu mengirim dan menerima data, dan mengkonversikan data ID baru dengan 1 stop bit yang dimana proses transmisi data I/O ketika pada logika high untuk stop bit bersamaan dengan proses start bit pada proses protokol smartcard. Proses transmisi data menggunakan komunikasi serial UART dan proses I/O mengasumsikan clock sesuai panjang data I/O.
2. Pada saat pengiriman software koneksi PC harus menyesuaikan kecepatan baudrate pada 9600bps pengaturan port com yang digunakan pada PC agar dapat mensinkronisasikan komunikasi data pada mikrocontroller dengan aplikasi pada PC
3. Dari hasil pengujian, lamanya waktu pada saat proses indikator standby adalah ± 4 detik pengisian data (*write*) rekam medis adalah ± 15 detik serta waktu yang dibutuhkan dalam proses pembacaan kartu (*read*) adalah ± 6 detik.

4. Pada proses aplikasi penggunaan sistim rekam medis diberikan kode pengaman sistim yang dimana proses utama untuk mengaktifkan sistim rekam medis membutuhkan card administrator dan data ID admin yang telah disamakan dengan data yang sama dengan id card admin.

5.2. Saran

Aplikasi sistem dari Sistem Akses Rekam Medis yang dikendalikan oleh mikrokontroler Renesas R8C13/Tiny ini masih memiliki keterbatasan, nantinya diharapkan dapat dikembangkan untuk mengatasi keterbatasan itu.Untuk pengembangan database selain informasi mengenai sistim akses rekam medis bisa ditambahkan untuk informasi lain yang berkaitan pada proses akses medika lainnya yang dimana untuk mempermudah fasilitas interface medika yang secara kompleks dengan memanfaatkan teknologi smartcard.

DAFTAR PUSTAKA

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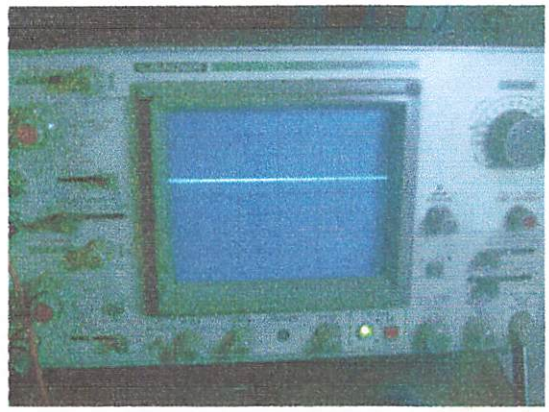
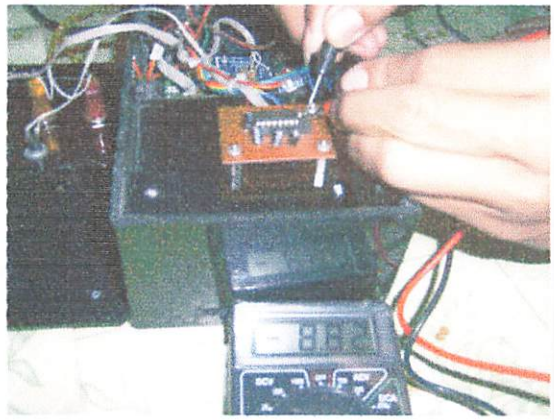
LAMPIRAN A

GAMBAR PENGUJIAN ALAT



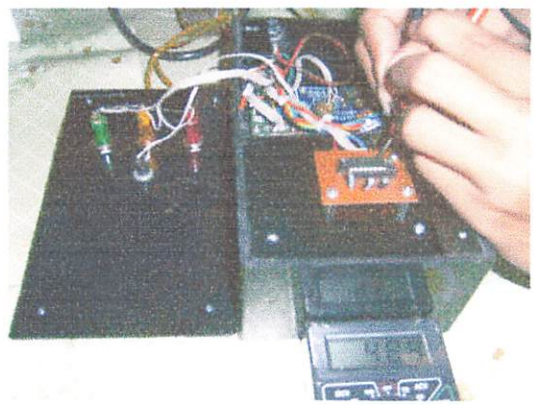
Gambar 1.a Gambar ketika belum ada masukan kartu

Gambar 1.b Gambar ketika setelah ada masukan kartu

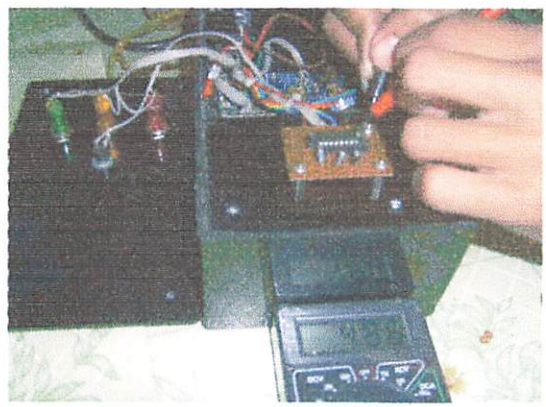


Gambar 1.c Gambar tegangan input pada smartcard reader

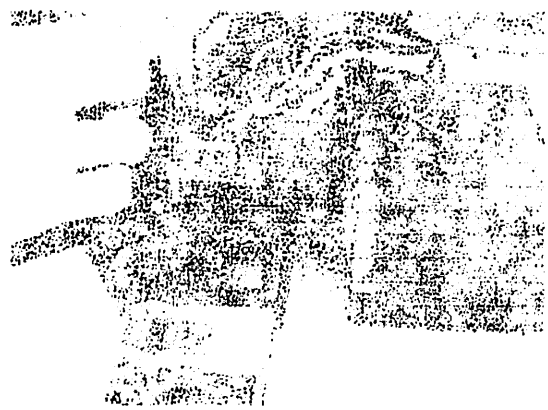
Gambar 1.d Gambar tegangan output pada smartcard reader

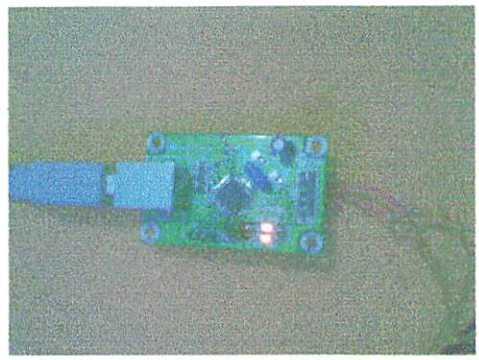


Gambar 1.e Gambar tegangan input proses ke mikrocontroller



Gambar 1.f Gambar tegangan output proses ke mikrocontroller

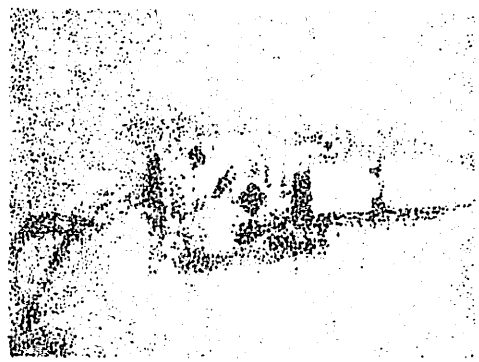


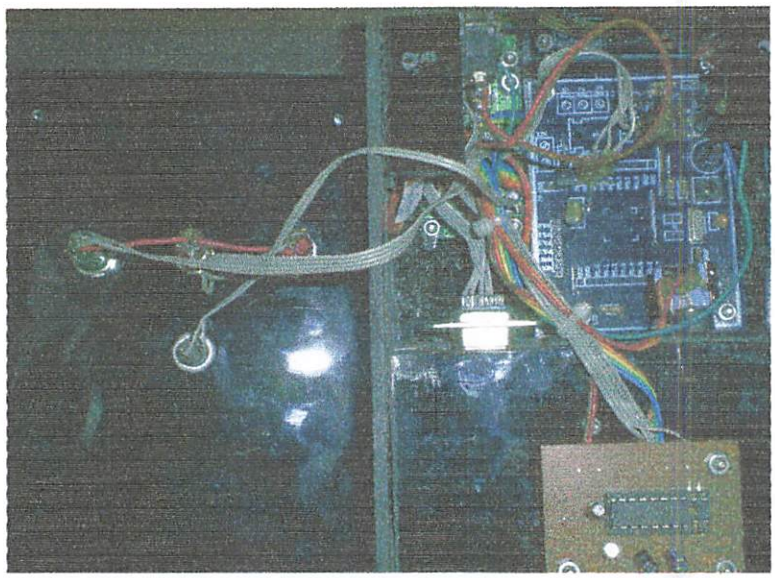


Gambar 1.g Pada proses penjumperan Rx dan Tx pada Modul USB

Spesifikasi Alat Keseluruhan :

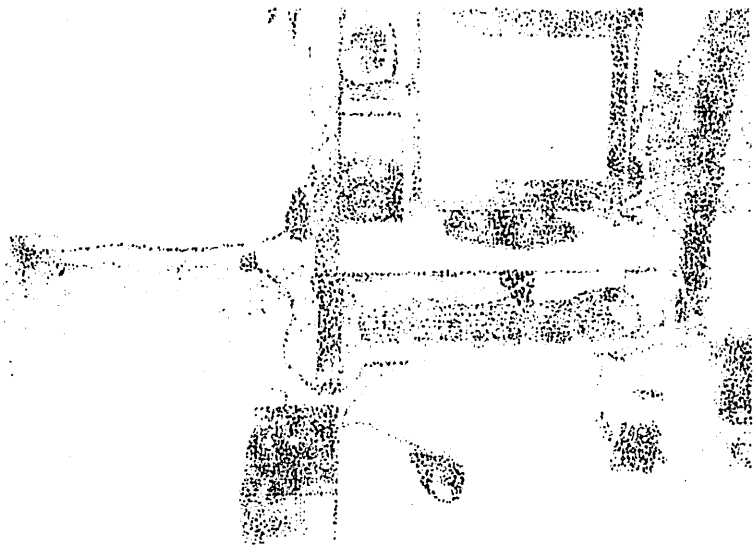
1. PC P4 Celeron 1.8GHz
2. Perangkat hardware keseluruhan terdiri dari :
    2.1 Dimensi : 16 x 11 x 6,5 cm
    2.2 Mikrokontroler R8C13/Tiny
    2.3 Indikator Smartcard
    2.4 Modul USB FT 232 BM
3. Power supplier
4. Kartu Smartcard Type Siemens SLE 4442
5. Software Mysql connector odbc 3.51.12 win32
6. Software Phptriad2-2-1.exe
7. Software Pemrograman Borland Delphi7

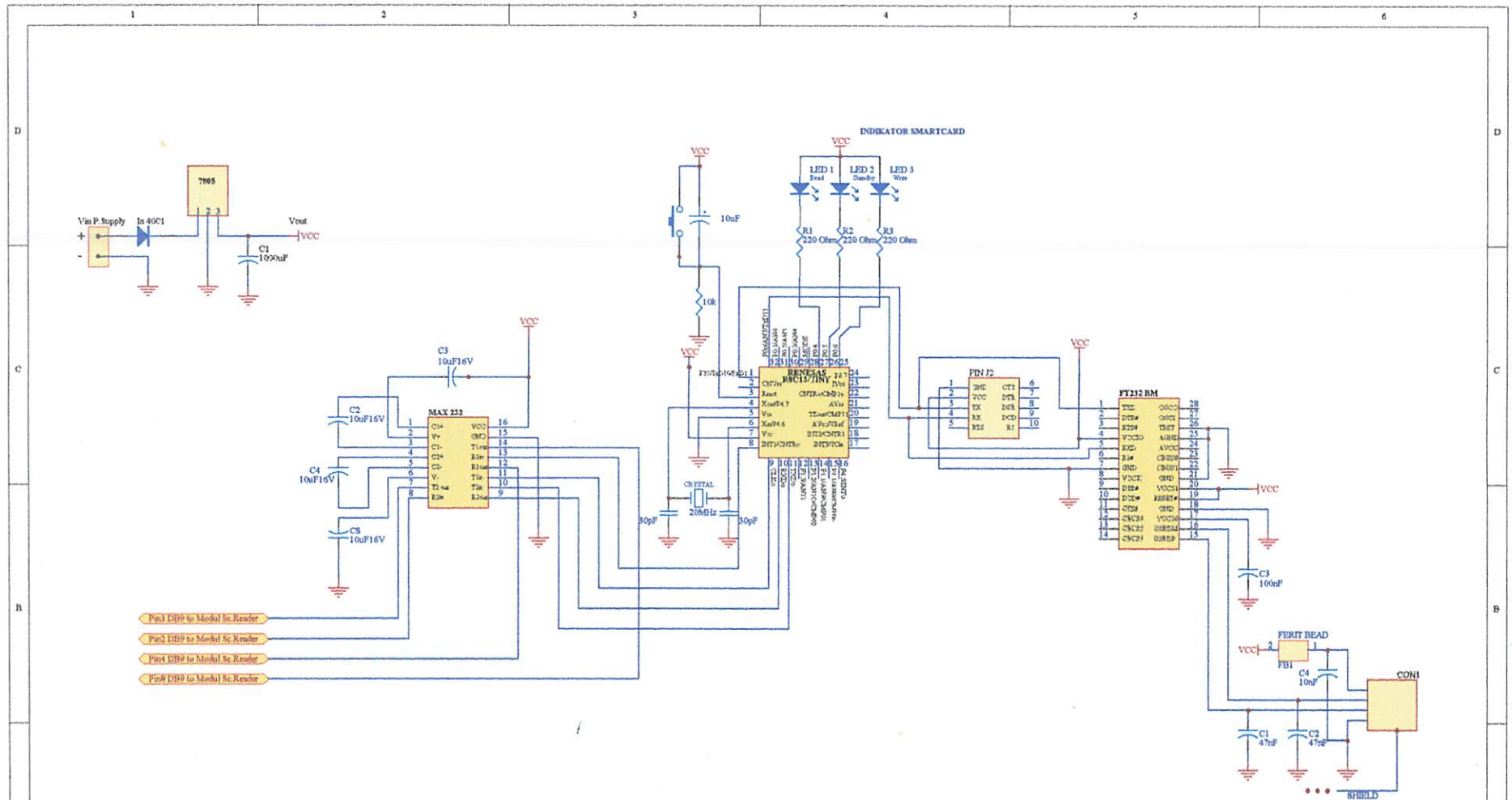




Gambar 1.h Perangkat hardware keseluruhan

Gambar 1.i Gambar Alat Keseluruhan.





Title :	PERANCANGAN DAN PEMBUATAN MODUL SMARTCARD MENGGUNAKAN RENESAS R8C13/TINY UNTUK AKSES REKAM MEDIS	
Size: B	Number : CAHYO SANDYONO TEKNIK ELEKTRONIKA S-1 ITN MALANG	Revision : 031*118
Date: 16-Mar-2008	Sheet of	
File: C:\PROGRAM FILES\DESIGN EXPLORER 99 SE\EXAMPLES\ACCPRO~1.DDB		

Text

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura – gura No.2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Cahyo Sandyono
Nim : 03.17.118
Masa Bimbingan : 07-November-2007 s/d 07-Mei-2008
Judul Skrips : Perencangan dan Pembuatan Modul *SMARTCARD* Menggunakan Renesas R8C13/Tiny Untuk Akses Rekam Medis Melalui USB

No	Tanggal	Uraian	Paraf Pembimbing
1	11/02/08	Bab I, II, III	
2	13/02/08	Perancangan System	
3	15/02/08	Bab IV	
4	15/02/08	pengujian Hardware	
5	15/02/08	pengujian Software	
6	15/02/08	Bab V	
7	17/02/08	Revisi tabel, gambar	
8	19/02/08	Makalah Seminar	
9		Acc Kompre	
10			

Malang, 6 Maret 2008
Dosen pembimbing I,

M Ashar, ST, MT
NIP.P.1030500408

Form S-4a

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura – gura No.2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Cahyo Sandyono
Nim : 03.17.118
Masa Bimbingan : 07-November-2007 s/d 07-Mei-2008
Judul Skrips : Perencangan dan Pembuatan Modul *SMARTCARD* Menggunakan Renesas R8C13/Tiny Untuk Akses Rekam Medis Melalui USB

No	Tanggal	Uraian	Paraf Pembimbing
1	11/08/02	BAB I, II, III	
2	13/08/02	PERANCANGAN SYSTEM	
3	05/08/02	BAB IV	
4	15/08/02	PENGUJIAN HARDWARE	
5	15/08/02	PENGUJIAN SOFTWARE	
6	15/08/02	BAB V	
7	15/08/02	Revisi TABEL, GAMBAR	
8	19/08/02	MAKALAH Seminar	
9	08/08/03	ACC KOMPRE	
10			

Malang, 6 MARET 2008

Dosen pembimbing II,

Sotyohadi, ST, MSc
NIP. Y

Form S-4a

LAMPIRAN B

PROGRAM

PROGRAM

```
#include <stdio.h>
#include "sfr_r813.h"
#include "timer.h"
#include "lcdku.h"
#include "serial.h"

#define fbreset     "0190000091"
#define fbmasuk  "01FF0100FF"
#define fbkeluar   "01FF0200FC"

//"00000"
#define dtr         p1_6
#define cts         p1_7
#define lmerah    p0_6
#define lhijau     p0_5
#define lkuning  p0_4


union byte_def tanda_addr;
#define   tanda    tanda_addr.byte
#define   tt   tanda_addr.bit.b0
#define   tsb   tanda_addr.bit.b1
#define   tkm   tanda_addr.bit.b2
#define   tcom   tanda_addr.bit.b3
unsigned char a,tangkap[100],i,i2,d[100],tangkap1[100];
long itimer;


unsigned char kon(unsigned char n)
  {
   if (n <10) return(n+0x30);
   else return(n+0x37);
  }

unsigned char nok(unsigned char n)
  {
   if (n < 0x3a) return(n-0x30);
   else return(n-0x37);
  }

void pindahdata()
{unsigned char aa;

for(i=0;i<10;i++) d[i]=tangkap1[i+1];
```

```
void rx(void)
{
while(ri_u1c1 == 0);
        ri_u1c1 =0;
        if(u1rb=='a') {tcom=1;i2=0;}
        else if(u1rb=='z') {tcom=0;}//pindahdata();tuliscard();}
        if(tcom==1) {tangkap1[i2]=u1rb;i2++;}
        u1c1 |= 1;
        }

#pragma INTERRUPT rx0//
void rx0(void)
{
while(ri_u0c1 == 0);
        ri_u0c1 =0;

        if(u0rb==2) {tt=1;i=0;}
        else if(u0rb==3) tt=0;
        if(tt==1) {tangkap[i]=u0rb;i++;}
        u0c1 |= 1;
        }

#pragma INTERRUPT tmx
void tmx(void)
{
        txund=0;
        itimer++;//kelip++;
        prex = 99;
        tx = 199;
}
void lampu(unsigned char la)//
{
if(la=='s') {lmerah=0;lhijau=1;lkuning=1;}
else if(la=='r') {lmerah=1;lhijau=0;lkuning=1;}
else if(la=='w') {lmerah=1;lhijau=1;lkuning=0;}
}
void main(void)
{
/* Inisialisasi Variable*/
        /* Inisialisasi Awal MK */
        asm("FCLR I"); // Interrupt disable
        prcr = 1;       // Protect off
        cm13 = 1;       // X-in X-out = Clock External
        cm15 = 1;           // XCIN-XCOUT drivecapacity select bit : HIGH
        cm05 = 0;           // X-in on
        cm16 = 0;           // Main clock = No division mode
```

```
        cm17 = 0;
        cm06 = 0;                   // CM16 and CM17 enable
        asm("nop");
        asm("nop");
        asm("nop");
        asm("nop");
        ocd2 = 0;                   // Main clock change (x-tal)
        prcr = 0;           // Protect on
        s1ric=2;
        s0ric=1;
        //txic=1;

/* p1 sebagai keluaran dan p0 sebagai masukan */
        pd1=0x80;
        pd1_4=1;
        pd0=0;
        prc2=1;pd0_5=1;
        prc2=1;pd0_4=1;
        prc2=1;pd0_6=1;
        pd3=0xff;
        pd3_7=0;
        pd1_6=1;pd1_7=0;
        asm("FSET I");
        initlcd();
        initSerial();
        tcom=0;
        for(i=0;i<60;i++) {d[i]='0';tangkap1[i]='0';}
        dtr=0;delay(100);dtr=1;delay(100);dtr=0;
        delay(100);
        milihcard();delay(100);
        oncard();delay(100);
        presetcode();delay(100);
        oncard();
        delay(2500);
        while (1) //
        {
        tsb=0;
        lampu('s');//lampu stand by
        while(tt==0)
        {
        if(tcom==1);while(tcom==1);
                        cetak(1,1,"proses transfer ");
                        lampu('w');//lampu write
                        pindahdata();tuliscard();
                        offcard();
                        }
```

```
                }
                while(tt==1);
                tsb=0;
                for(i=0;i<10;i++)
                {if(tangkap[i+1]!=fbmasuk[i]) tsb=1;}
                if(tsb==0) {busek();cetak(1,1,"deteksi masuk   ");
                                lampu('r');//lampu read
                                bacacard();tunggu();busek();
                                pos(1,1);

for(i=9;i<19;i++)kirim_serial(tangkap[i]);//
}
        offcard();
        tsb=0;
        for(i=0;i<10;i++)
        {if(tangkap[i+1]!=fbkeluar[i]) tsb=1;}
        if(tsb==0) ;delay(2000);

                }
}
void initSerial(void)
{
                /* parity disable, 1 stop bit */
                /* internal clock, UART mode 8 bits data length */
                u1mr = 0x05;u0mr=0x05;
                /* data dikirim LSB dulu,TxD is CMOS output, /*
                /* tidak ada data, prescaler dibagi 1 */
                u1c0 = 0x08;u0c0=0x08;
                /* baud rate 9600 at 20 MHz     */
                u1brg = 129;
                u0brg = 129;
                /* re = 1; enable reception */
                u1c1 |= 0x05; u0c1 |= 0x05;
                /* interupt at transmit completed, TXd11 activated */
                ucon |= 0x26;
}

void kirim_serial(char data)
{
                u1tb=data;
                while(txept_u1c0 == 0);
                //txept_u1c0 = 0;
                u1rb = data;
                u1c1 |= 1;
                delay(10);
                //delayx(20);
```

```
}
void kirim0(char data)
{
        u0tb=data;
        while(txept_u0c0 == 0);
        //txept_u1c0 = 0;
        u0rb = data;
        u0c1 |= 1;
        //delay(1);
        delay(10);
}
unsigned GetChar()
{
while(ri_u0c1 == 0);
        ri_u0c1 =0;
        //dataout(u0rb);
        //asu1=u0rb;
        u0c1 |= 1;
        return u0rb;
}
unsigned getsms()
{
while(ri_u1c1 == 0);
        ri_u1c1 =0;
        //dataout(u0rb);
        //asu1=u0rb;
        u1c1 |= 1;
        return u1rb;
}
void kirimgps(unsigned char *text)
{
        while( *text!=',' )        // while not end of text
        {
        kirim_serial(*text++);  // Write character and increment position
        }
return;
}
void kirimasli(unsigned char *text)
{
        while( *text!='?' )        // while not end of text
        {
          kirim_serial(*text++);// Write character and increment position
        }
return;
}
void enter()
```

```
{
        //kirimenter(0x0D);
        //kirimenter(0x0A);
        //kirim_serial(13);
        kirim_serial(10);
        kirim_serial(13);
        delay(100);
}
void ente()
{
        kirim_serial(10);
        kirim_serial(13);
        delay(10);
}
void Send_Text(unsigned char *text)
{
        while( *text )      // while not end of text
        {
        kirim_serial(*text++);  // Write character and increment position
        //delay(10);
        }
return;
}
void kirimt0(unsigned char *text)
{
        while( *text )      // while not end of text
        {
        kirim0(*text++);// Write character and increment position
        //delay(10);
        }
return;
}
void sendsms(unsigned char *CommandSMS, unsigned char *DataPDU)
{
        //send command SMS
        Send_Text(CommandSMS);
        delay(20)           ;
        enter()             ;
        delay(100)          ;
        //send DataPDU
        Send_Text(DataPDU);
        delay(20)           ;
  kirim_serial(0x1a);
        delay(500)          ;
        return;
}
```

```
void atcmg(unsigned char *CommandSMS)
{
        //send command SMS
        Send_Text(CommandSMS);
        delay(20)       ;
        enter()         ;
        //delay(100)    ;
        return;
}
void atcm(unsigned char *CommandSMS)
{
        //send command SMS
        Send_Text(CommandSMS);
        delay(20)       ;
        ente()          ;
        //delay(100)    ;
        return;
}
end;
```

LAMPIRAN C

DATA SHEET

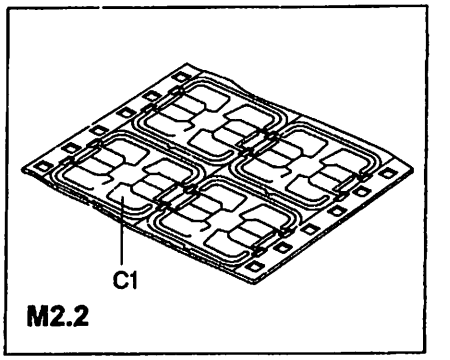
SIEMENS

Intelligent 256-Byte EEPROM with Write Protect Function — SLE 4432

Intelligent 256-Byte EEPROM with Write Protect Function and Programmable Security Code (PSC) — SLE 4442

Features

- 256 × 8-bit EEPROM organization
- Byte-wise addressing
- Irreversible byte-wise write protection of lowest 32 addresses (Byte 0 ... 31)
- 32 × 1-bit organization of protection memory
- Two-wire link protocol
- End of processing indicated at data output
- Answer-to-Reset acc. to ISO standard 7816-3
- Programming time 2.5 ms per byte for both erasing and writing
- Minimum of 10^4 write/erase cycles[1)]
- Data retention for minimum of ten years[1)]
- Contact configuration and serial interface in accordance with ISO standard 7816 (synchronous transmission)



M2.2

Additional Feature of SLE 4442

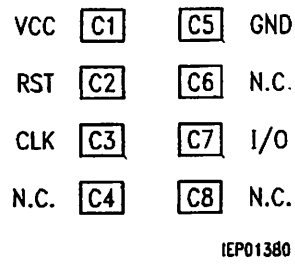
- Data can only be changed after entry of the correct 3-byte programmable security code (security memory)

Type	Ordering Code	Package
SLE 4432 M2.2	on request	Wire-Bonded Module M2.2
SLE 4432 C	on request	Chip
SLE 4442 M2.2	on request	Wire-Bonded Module M2.2
SLE 4442 C	on request	Chip

1) Values are temperature dependent, for further information please refer to your Siemens sales office.

1 Pin Configuration

(top view)



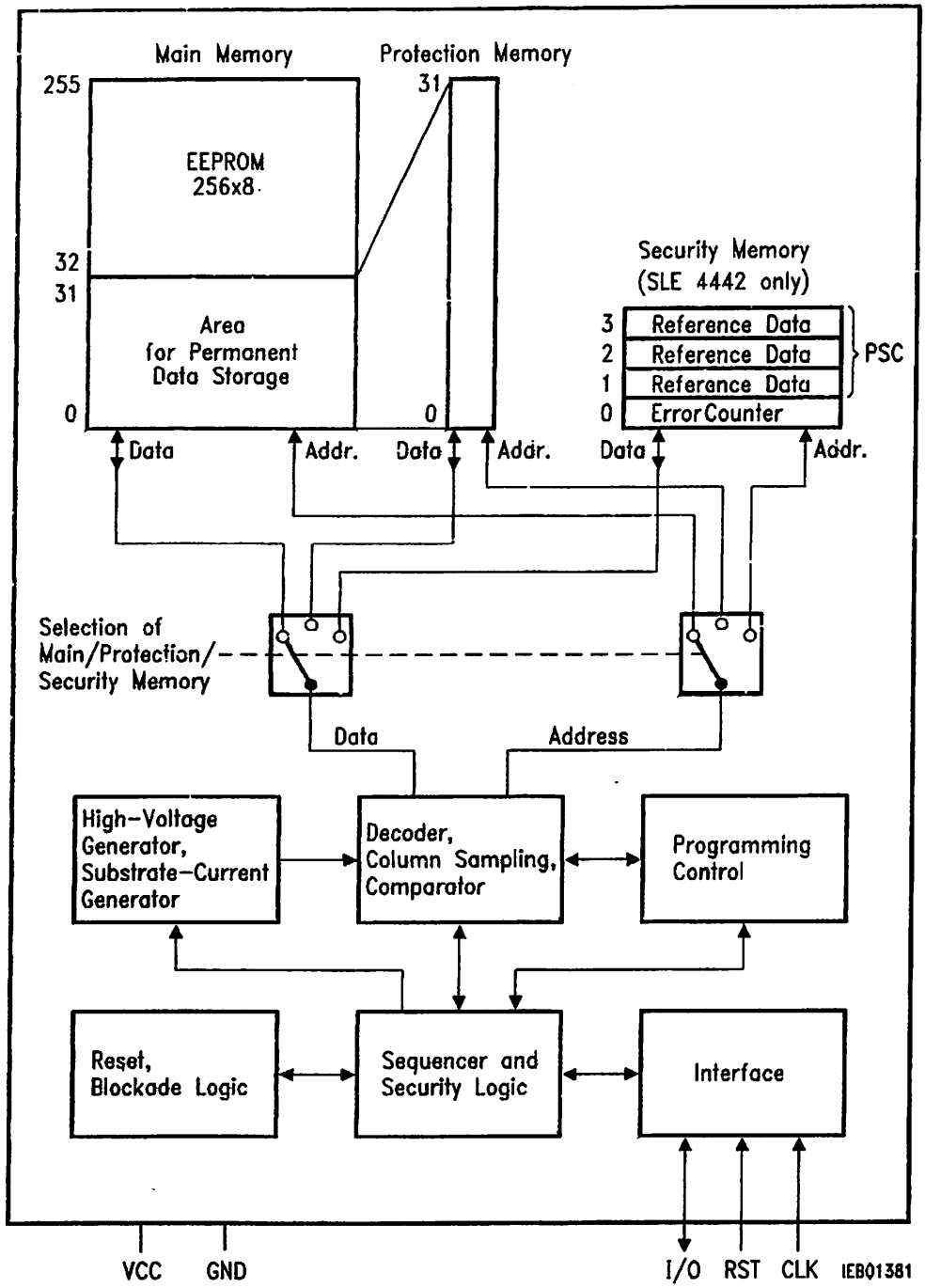
M2.2 (Card Contacts)

Pin Definitions and Functions

Card Contact	Symbol	Function
C1	VCC	Supply voltage
C2	RST	Reset
C3	CLK	Clock input
C4	N.C.	Not connected
C5	GND	Ground
C6	N.C.	Not connected
C7	I/O	Bidirectional data line (open drain)
C8	N.C.	Not connected

SLE 4432/SLE 4442 comes as a M2.2 wire-bonded module for embedding in plastic cards or as a die for customer packaging.

2 Functional Description



Block Diagram

2.1 Memory Overview

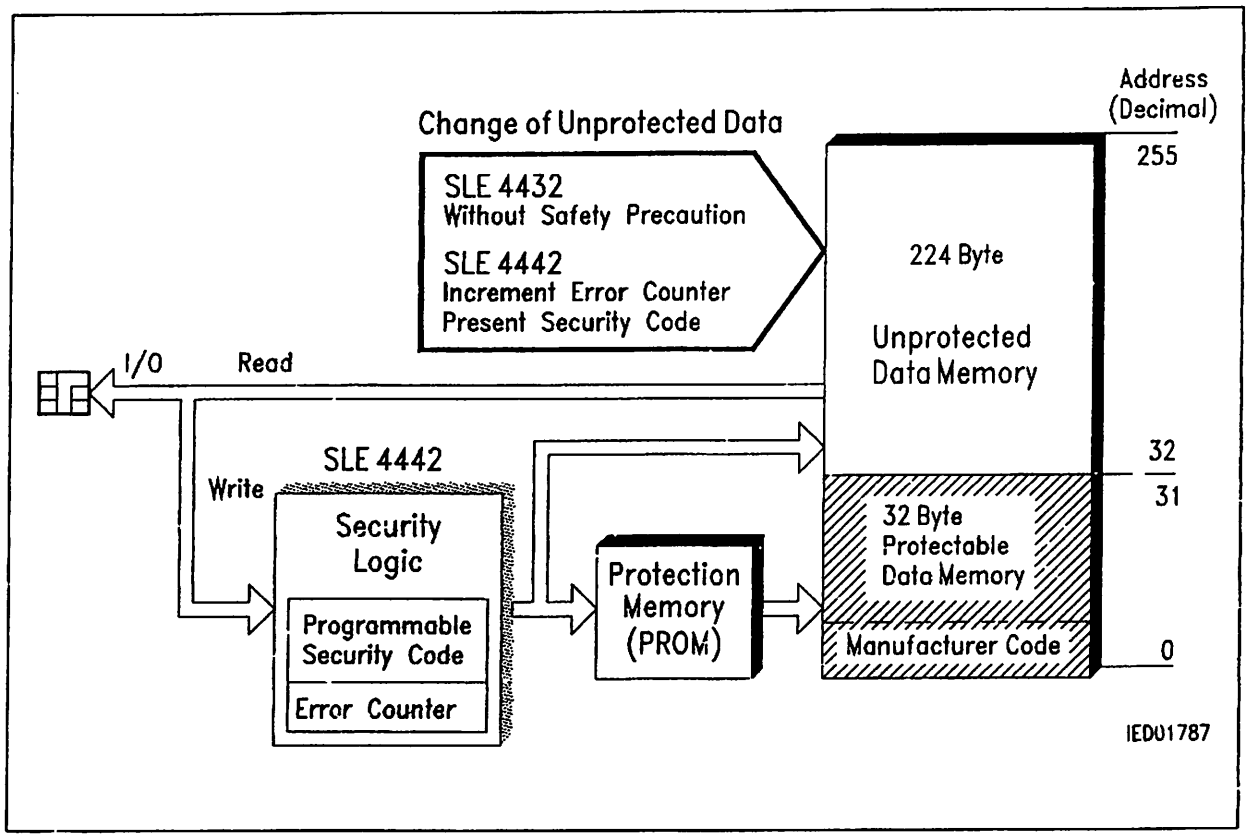


Figure 1
Memory Overwiew

SLE 4432

The SLE 4432 consists of 256 x 8 bit EEPROM main memory and a 32-bit protection memory with PROM functionality. The main memory is erased and written byte by byte. When erased, all 8 bits of a data byte are set to logical one. When written, the information in the individual EEPROM cells is, according to the input data, altered bit by bit to logical zeros (logical AND between the old and the new data in the EEPROM). Normally a data change consists of an erase and write procedure. It depends on the contents of the data byte in the main memory and the new data byte whether the EEPROM is really erased and/or written. If none of the 8 bits in the addressed byte requires a zero-to-one transition the erase access will be suppressed. Vice versa the write access will be suppressed if no one-to-zero transition is necessary. The write and the erase operation takes at least 2.5 ms each.

Each of the first 32 bytes can be irreversibly protected against data change by writing the corresponding bit in the protection memory. Each data byte in this address range is assigned to one bit of the protection memory and has the same address as the data byte in the main memory which it is assigned to. Once written the protection bit cannot be erased (PROM).

SLE 4442

Additionally to the above functions the SLE 4442 provides a security code logic which controls the write/erase access to the memory. For this purpose the SLE 4442 contains a 4-byte security memory with an Error Counter EC (bit 0 to bit 2) and 3 bytes reference data. These 3 bytes as a whole are called Programmable Security Code (PSC). After power on the whole memory, except for the reference data, can only be read. Only after a successful comparison of verification data with the internal reference data the memory has the identical access functionality of the SLE 4432 until the power is switched off. After three successive unsuccessful comparisons the Error Counter blocks any subsequent attempt, and hence any possibility to write and erase.

2.2 Transmission Protocol

The transmission protocol is a two wire link protocol between the interface device IFD and the integrated circuit IC. It is identical to the protocol type "S = A". All data changes on I/O are initiated by the falling edge on CLK.

The transmission protocol consists of the 4 modes:

- Reset and Answer-to-Reset
- Command Mode
- Outgoing Data Mode
- Processing Mode

} Operational modes

Note: The I/O pin is open drain and therefore requires an external pull up resistor to achieve a high level.

2.2.1 Reset and Answer-to-Reset

Answer-to-Reset takes place according to ISO standard 7816-3 (ATR). The reset can be given at any time during operation. In the beginning, the address counter is set to zero together with a clock pulse and the first data bit (LSB) is output to I/O when RST is set from level H to level L. Under a continuous input of additional 31 clock pulses the contents of the first 4 EEPROM addresses is read out. The 33rd clock pulse switches I/O to high impedance Z and finishes the ATR procedure.

Answer-to-Reset (Hex)	Byte 1	Byte 2	Byte 3	Byte 4
	$DO_7 \ldots DO_0$	$DO_{15} \ldots DO_8$	$DO_{23} \ldots DO_{16}$	$DO_{31} \ldots DO_{24}$

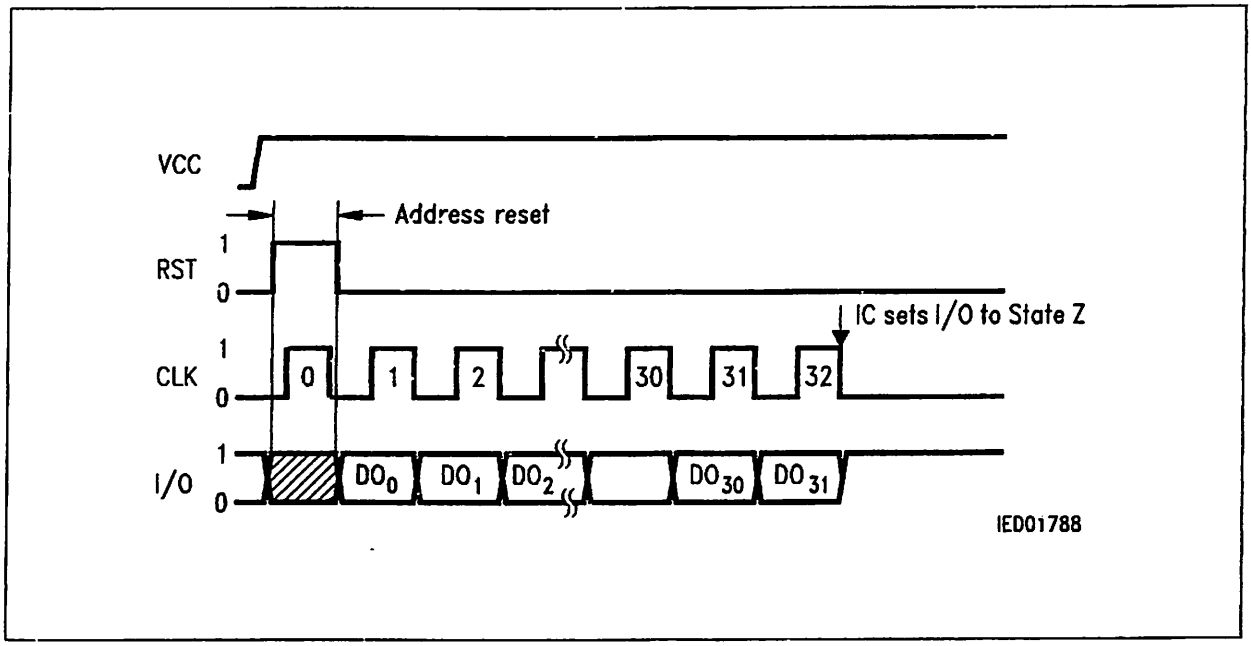


Figure 2
Reset and Answer-to-Reset

2.2.2 Operational Modes

Command Mode

After the Answer-to-Reset the chip waits for a command. Every command begins with a start condition, includes a 3 bytes long command entry followed by an additional clock pulse and ends with a stop condition.

- Start condition: Falling edge on I/O during CLK in level H
- Stop condition: Rising edge on I/O during CLK in level H

After the reception of a command there are two possible modes:

- Outgoing data mode for reading
- Processing mode for writing and erasing

Outgoing Data Mode

In this mode the IC sends data to the IFD. The first bit becomes valid on I/O after the first falling edge on CLK. After the last data bit an additional clock pulse is necessary in order to set I/O to high impedance Z and to prepare the IC for a new command entry. During this mode any start and stop condition is discarded.

Processing Mode

In this mode the IC processes internally. The IC has to be clocked continuously until I/O, which was switched to level L after the first falling edge of CLK, is set to high impedance level Z. Any start and stop condition is discarded during this mode.

Note: The RST line is low during the modes mentioned above. If RST is set to high during the CLK low level any operation is aborted and I/O is switched to high impedance Z (Break).

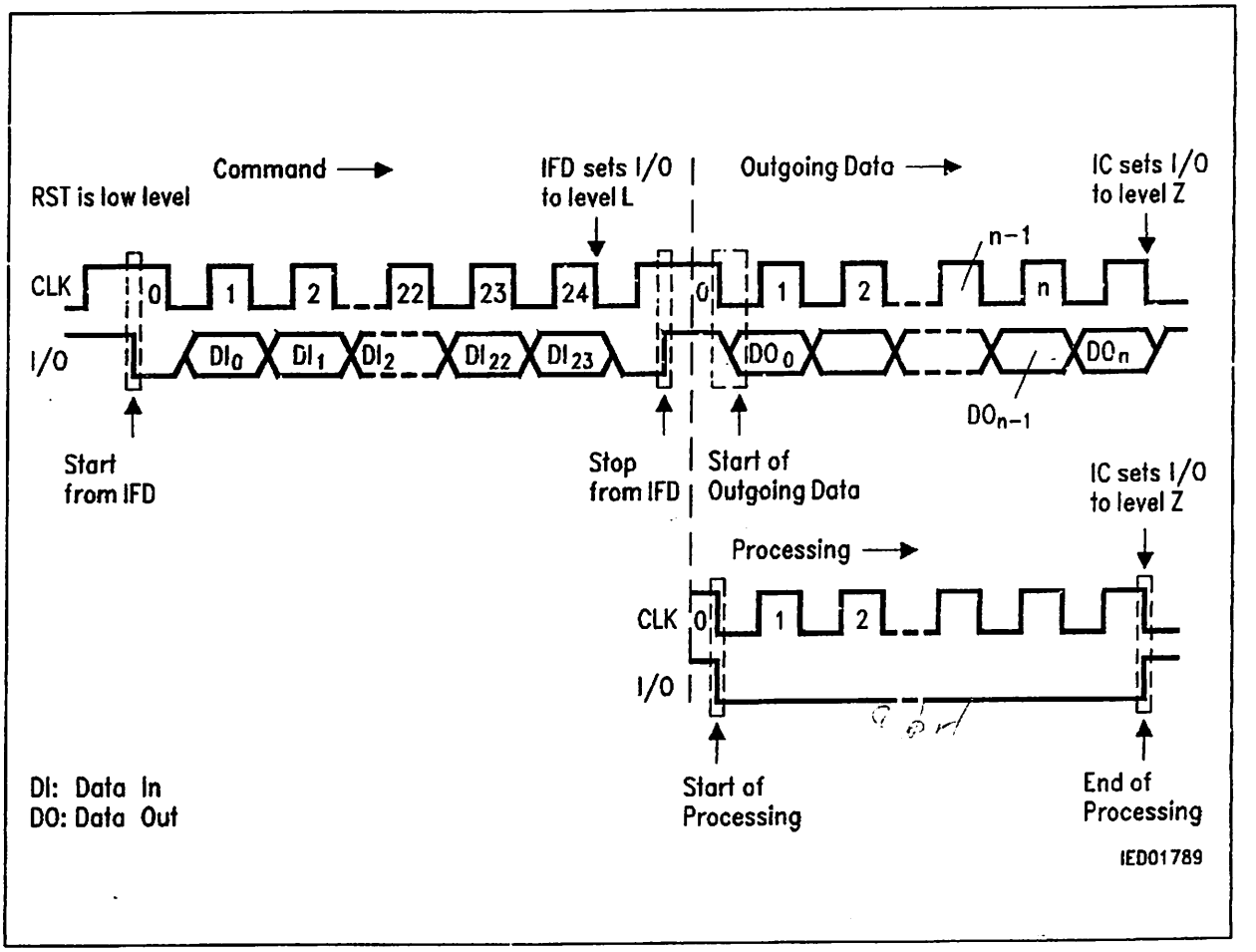


Figure 3
Operational Modes

2.3 Commands

Command Format

Each command consists of three bytes:

MSB			Control				LSB	MSB			Address				LSB	MSB			Data				LSB
B7	B6	B5	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Beginning with the control byte LSB is transmitted first.

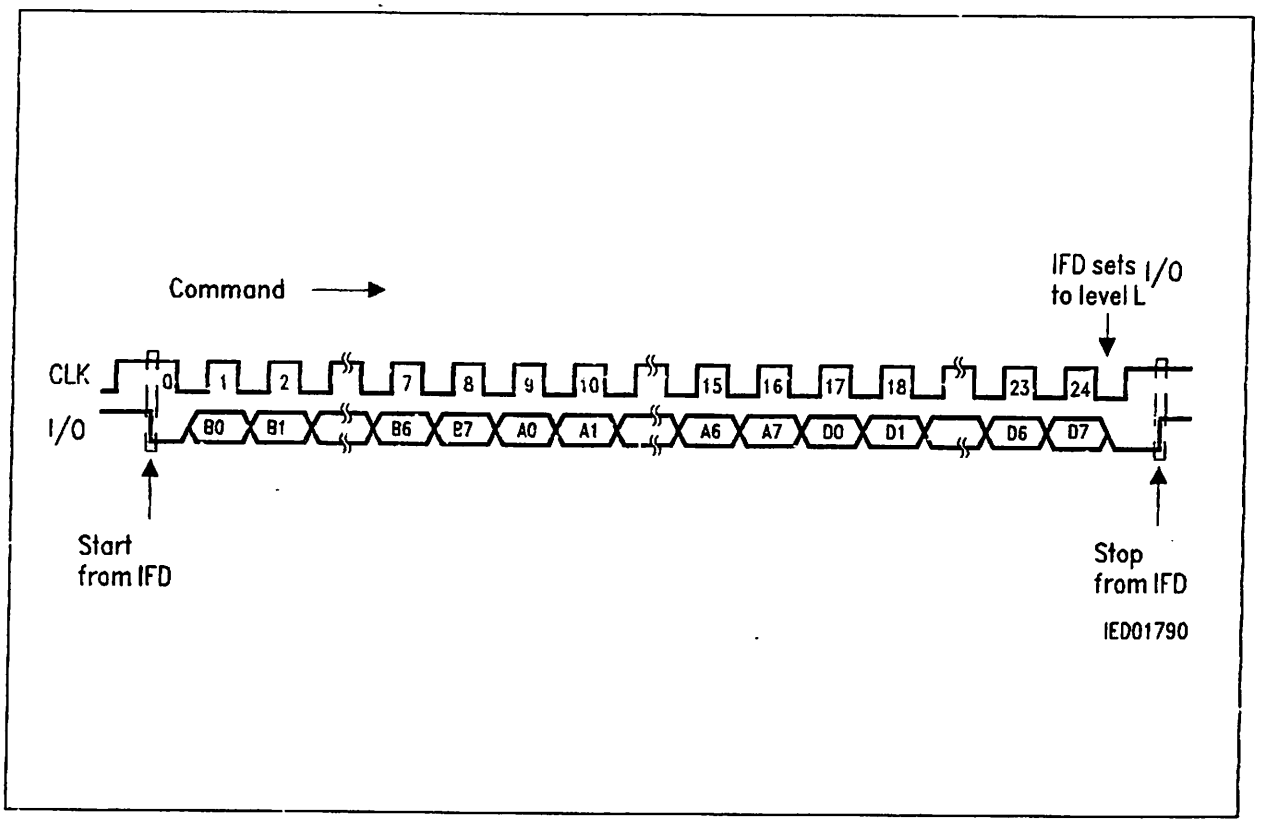


Figure 4
Command Mode

The SLE 4432 provides 4 commands which are listed in **table 1**. Additionally to these commands the SLE 4442 provides 3 commands which can be found in **table 2**.

Table 1

Byte 1 Control								Byte 2 Address	Byte 3 Data	Operation	Mode
B7	B6	B5	B4	B3	B2	B1	B0	A7-A0	D7-D0		
0	0	1	1	0	0	0	0	address	no effect	READ MAIN MEMORY	outgoing data
0	0	1	1	1	0	0	0	address	input data	UPDATE MAIN MEMORY	processing
0	0	1	1	0	1	0	0	no effect	no effect	READ PROTECTION MEMORY	outgoing data
0	0	1	1	1	1	0	0	address	input data	WRITE PROTECTION MEMORY	processing

Table 2
SLE 4442 only

0	0	1	1	0	0	0	1	no effect	no effect	READ SECURITY MEMORY	outgoing data
0	0	1	1	1	0	0	1	address	input data	UPDATE SECURITY MEMORY	processing
0	0	1	1	0	0	1	1	address	input data	COMPARE VERIFICATION DATA	processing

2.3.1 Read Main Memory (SLE 4432 and SLE 4442)

The command reads out the contents of the main memory (with LSB first) starting at the given byte address (N = 0...255) up to the end of the memory. After the command entry the IFD has to supply sufficient clock pulses. The number of clocks is m = (256 – N) × 8 + 1. The read access to the main memory is always possible.

Address (decimal)	Main Memory	Protection Memory	Security Memory (only SLE 4442)
255	Data Byte 255 (D7 ... D0)	–	–
:	:	–	–
32	Data Byte 32 (D7 ... D0)	–	--
31	Data Byte 31 (D7 ... D0)	Protection Bit 31 (D31)	–
:	:	:	–
3	Data Byte 3 (D7 ... D0)	Protection Bit 3 (D3)	Reference Data Byte 3 (D7 ... D0)
2	Data Byte 2 (D7 ... D0)	Protection Bit 2 (D2)	Reference Data Byte 2 (D7 ... D0)
1	Data Byte 1 (D7 ... D0)	Protection Bit 1 (D1)	Reference Data Byte 1 (D7 ... D0)
0	Data Byte 0 (D7 ... D0)	Protection Bit 0 (D0)	Error Counter

Command: READ MAIN MEMORY

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7...A0	D7...D0
Binary	0	0	1	1	0	0	0	0	Address	No effect
Hexadecimal	30_H								00_H...FF_H	No effect

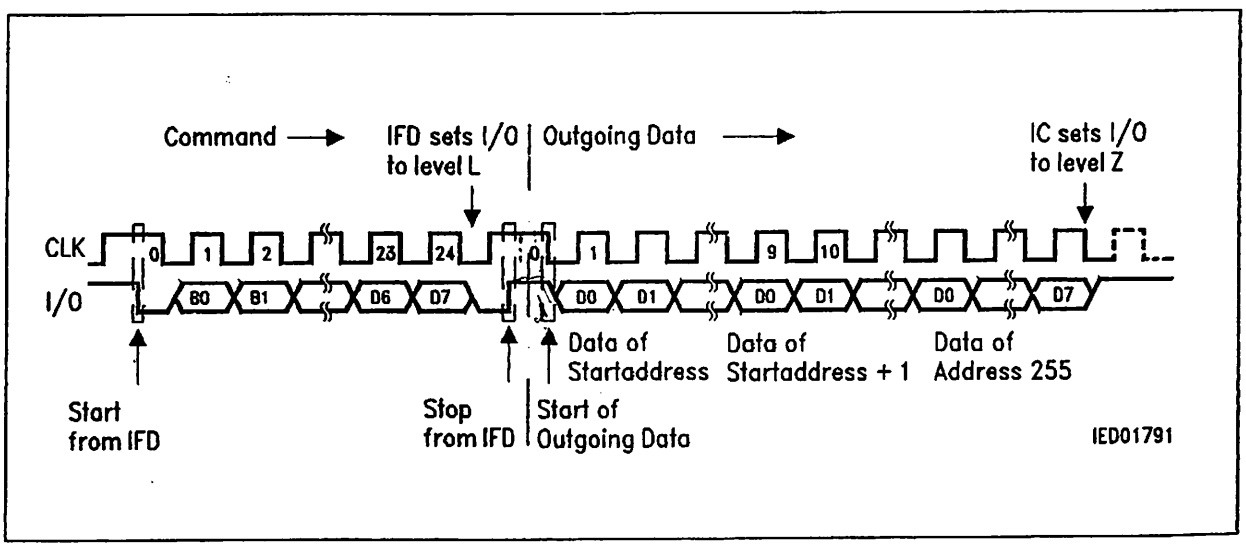


Figure 5
Read Main Memory

2.3.2 Read Protection Memory (SLE 4432 and SLE 4442)

The command transfers the protection bits under a continuous input of 32 clock pulses to the output. I/O is switched to high impedance Z by an additional pulse. The protection memory can always be read, and indicates the data bytes of the main memory protected against changing.

Address (decimal)	Main Memory	Protection Memory	Security Memory (only SLE 4442)
255	Data Byte 255 (D7 ... D0)	–	–
:	:	–	–
32	Data Byte 32 (D7 ... D0)	–	–
31	Data Byte 31 (D7 ... D0)	Protection Bit 31 (D31)	–
:	:	:	–
3	Data Byte 3 (D7 ... D0)	Protection Bit 3 (D3)	Reference Data Byte 3 (D7 ... D0)
2	Data Byte 2 (D7 ... D0)	Protection Bit 2 (D2)	Reference Data Byte 2 (D7 ... D0)
1	Data Byte 1 (D7 ... D0)	Protection Bit 1 (D1)	Reference Data Byte 1 (D7 ... D0)
0	Data Byte 0 (D7 ... D0)	Protection Bit 0 (D0)	Error Counter

Command: READ PROTECTION MEMORY

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7...A0	D7...D0
Binary	0	0	1	1	0	1	0	0	No effect	No effect
Hexadecimal	34_H								No effect	No effect

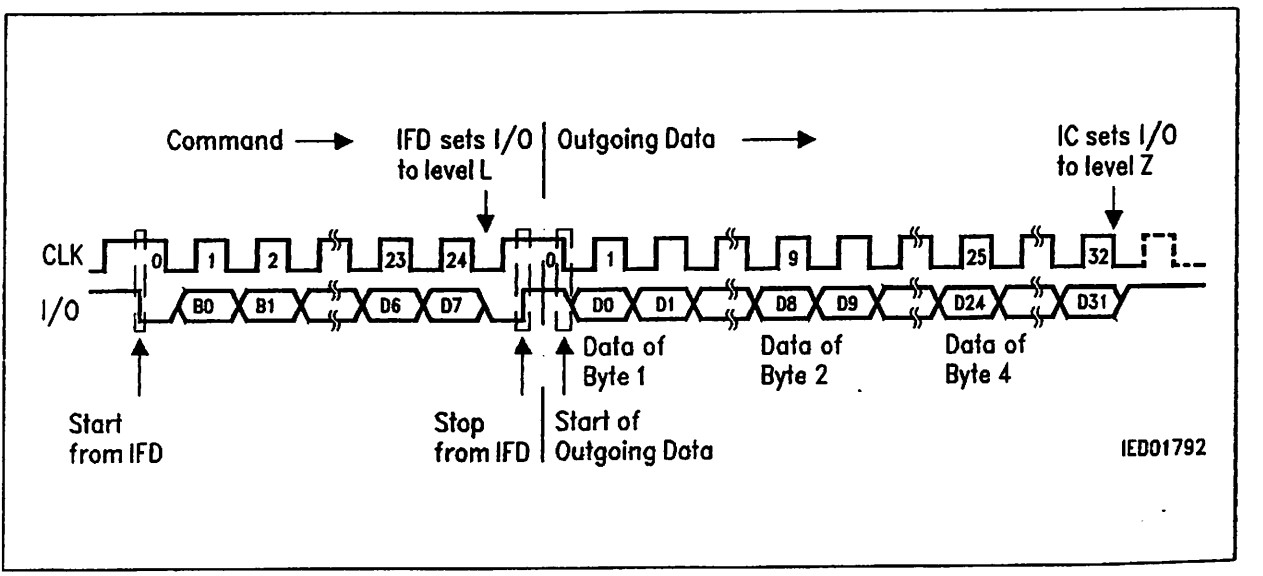


Figure 6
Read Protection Memory

2.3.3 Update Main Memory (SLE 4432 and SLE 4442)

The command programs the addressed EEPROM byte with the data byte transmitted. Depending on the old and new data, one of the following sequences will take place during the processing mode:

- erase and write (5 ms) corresponding to m = 255 clock pulses
- write without erase (2.5 ms) corresponding to m = 124 clock pulses
- erase without write (2.5 ms) corresponding to m = 124 clock pulses

(All values at 50 kHz clock rate.)

Address (decimal)	Main Memory	Protection Memory	Security Memory (only SLE 4442)
255	Data Byte 255 (D7 ... D0)	–	–
:	:	–	–
32	Data Byte 32 (D7 ... D0)	–	–
31	Data Byte 31 (D7 ... D0)	Protection Bit 31 (D31)	–
:	:	:	–
3	Data Byte 3 (D7 ... D0)	Protection Bit 3 (D3)	Reference Data Byte 3 (D7 ... D0)
2	Data Byte 2 (D7 ... D0)	Protection Bit 2 (D2)	Reference Data Byte 2 (D7 ... D0)
1	Data Byte 1 (D7 ... D0)	Protection Bit 1 (D1)	Reference Data Byte 1 (D7 ... D0)
0	Data Byte 0 (D7 ... D0)	Protection Bit 0 (D0)	Error Counter

Command: UPDATE MAIN MEMORY

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7...A0	D7...D0
Binary	0	0	1	1	1	0	0	0	Address	Input data
Hexadecimal	38_H								00_H...FF_H	Input data

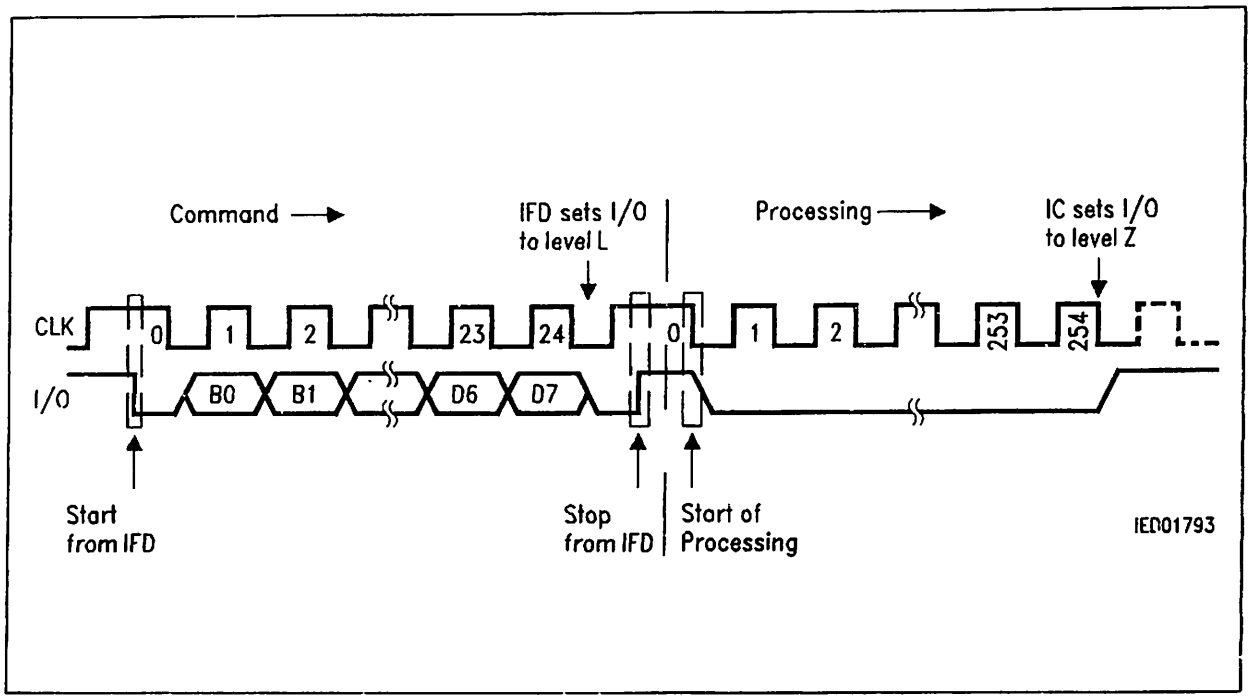


Figure 7
Erase and Write Main Memory

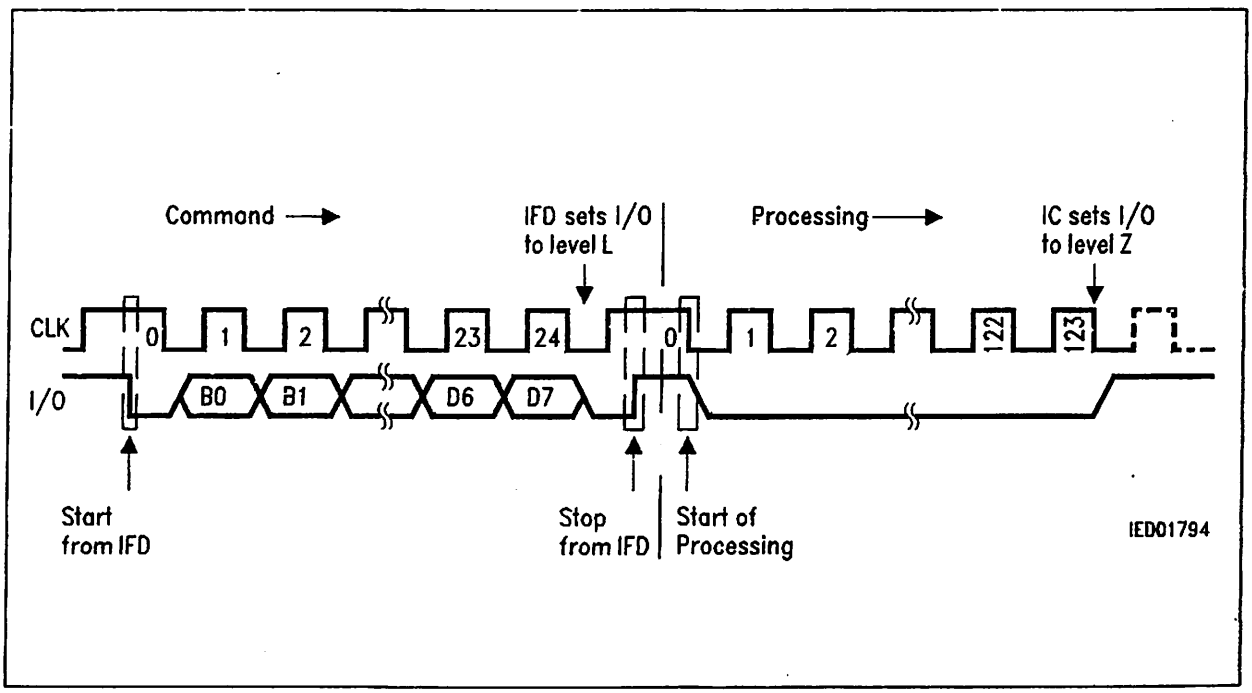


Figure 8
Erase or Write Main Memory

If the addressed byte is protected against changes (indicated by the associated written protection bit) the I/O is set to high impedance after the clock number 2 of the processing.

2.5 Reset Modes

Reset and Answer-to-Reset (compare 2.2.1)

Power on Reset

After connecting the operating voltage to VCC, I/O is high impedance Z. By all means, a read access to any address or an Answer-to-Reset must be carried out before data can be altered.

2.6 Break

If RST is set to high during CLK in state L any operation is aborted and I/O is switched to high impedance Z. Minimum duration of t_{RES} = 5 µs is necessary to trigger a defined valid reset. After Break the chip is ready for further operations.

2.7 Failures

Behavior in case of failures:

In case of one of the following failures, the chip sets the I/O to high impedance Z after 8 clock pulses at the latest.

Possible failures:

- Comparison unsuccessful
- Wrong command
- Wrong number of command clock pulses
- Write/erase access to already protected bytes
- Rewriting and erasing of a bit in the protection memory

2.8 Coding of the Chip

Due to security purposes every chip is irreversibly coded by a scheme. By this way fraud and misuse is excluded. The relevant data are programmed in the memory area from address 0 to 31. Afterwards the associated protection bits are programmed. As an example, **figures 12** and **13** show ATR and Directory Data of Structure 1. When delivered, ATR header, ICM and ICT are programmed. Siemens programs also the AID. The AID (Application IDentifier) consists of 5 byte RID (Registered application provider IDentifier) administered by a national registration authority and of up to 11 byte PIX (Proprietary application Identifier eXtension). There are two possibilities: the customers AID or Siemens AID (only for sample quantities). Depending on the agreement between the customer and Siemens ICCF can be also programmed before delivery.

3.3 Timing Diagrams

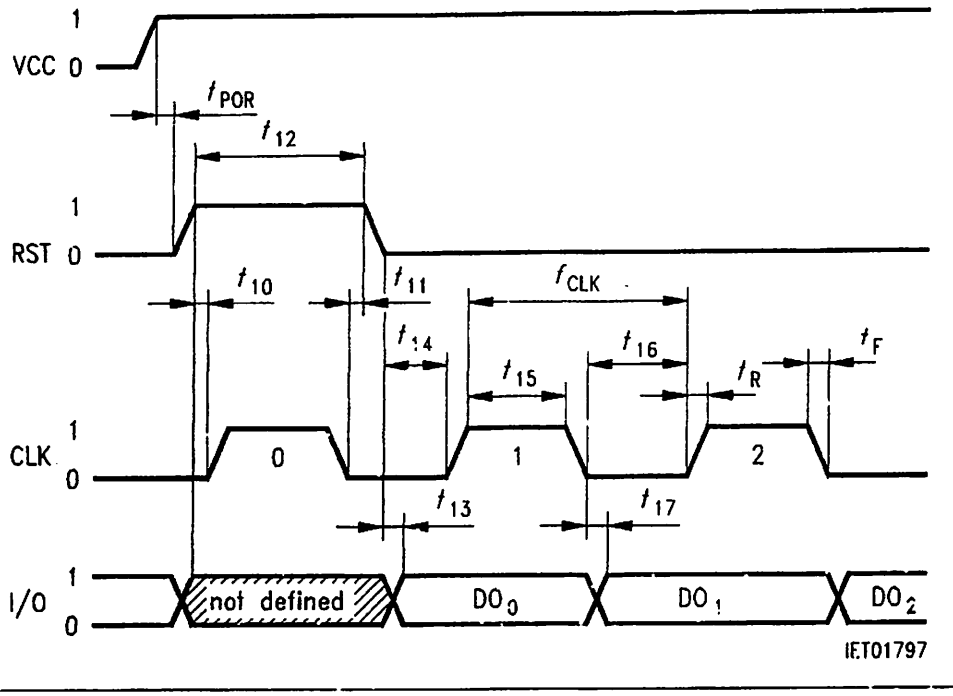


Figure 14
Reset and Answer-to-Reset

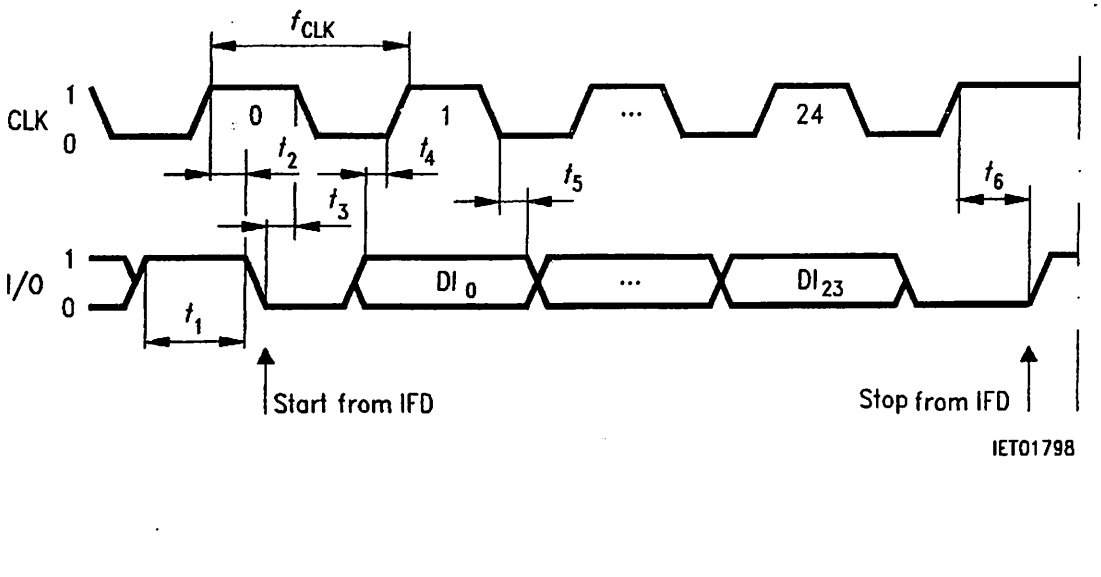
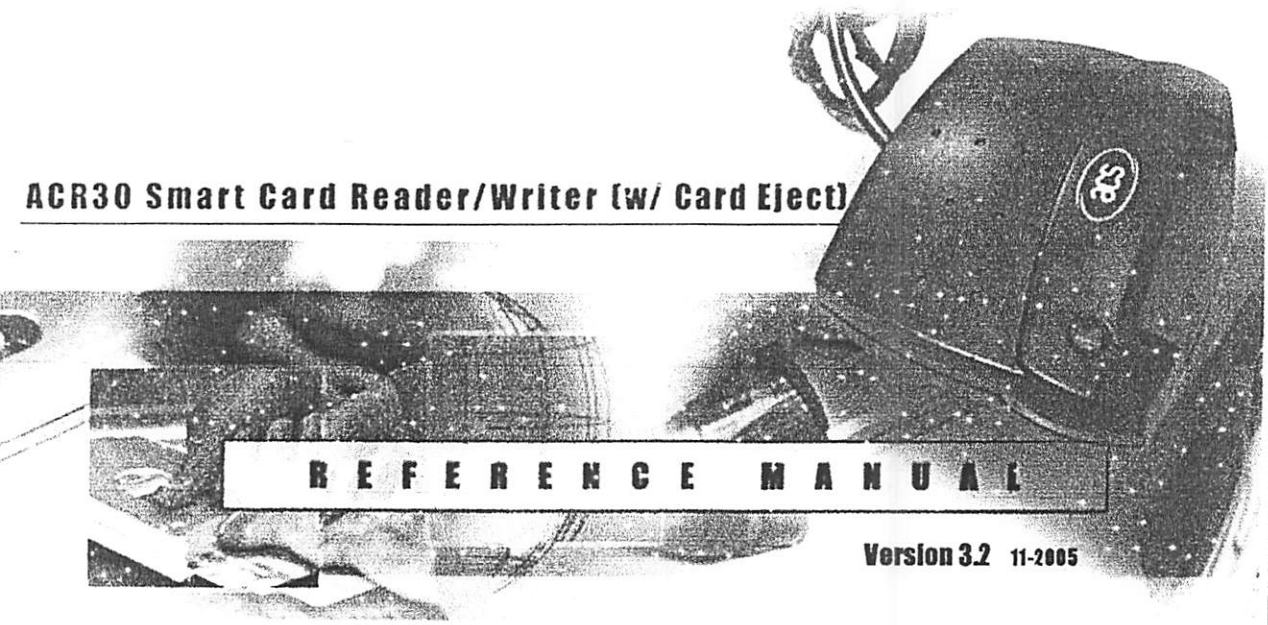


Figure 15
Command Mode

Advanced Card Systems Ltd.

ACR30 Smart Card Reader/Writer (w/ Card Eject)



REFERENCE MANUAL

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Contents

Note:
(*) – SAM Reader does not support for memory cards
(**) – SAM Reader only

1. Introduction

The ACS Smart Card Reader/Writer ACR30 is an interface for the communication between a computer (for example, a PC) and a smart card. Different types of smart cards have different commands and different communication protocols. This prevents in most cases the direct communication between a smart card and a computer. The ACR30 Reader/Writer establishes a uniform interface from the computer to the smart card for a wide variety of cards. By taking care of the card specific particulars, it releases the computer software programmer of getting involved with the technical details of the smart card operation, which are in many cases not relevant for the implementation of a smart card system.

The ACR30 Smart Card Reader/Writer is connected to the computer through a serial asynchronous interface (RS-232) or USB interface. The reader accepts commands from the computer, carries out the specified function at the smart card and returns the requested data or status information.

NOTE - Although the ACR30 is a true *card reader/writer* as it can read and write smart cards, the terms *card reader* or *reader* will be used indifferently to refer to the ACR30, for the sake of readability and because these designations are commonly in use for this kind of devices.

2. Features

- ISO7816-1/2/3 compatible smart card interface
- Supports CPU-based cards with T=0 and/or T=1 protocol
- (*) Supports commonly used memory cards (I2C, SLE4406, SLE4418/28, SLE4432/42)
- Support PPS (Protocol and Parameters Selection) with 9600 – 96000 bps in reading and writing smart cards
- RS-232 interface or USB interface to PC with simple command structure
- Supports memory cards SLE4436 and SLE5536 (firmware 2.10 onwards)
- Security application modules (SAM) inside the reader supporting CPU-based cards with T=0 and/or T=1 protocol (SAM Reader only)

Note (*) – SAM Reader does not support for memory cards

3. Supported Card Types

The ACR30 can operate MCU card with T=0 and T=1 protocol. The table presented in Appendix A explains which card type selection value must be specified for the various card types supported by the reader.

3.1 *Memory-based smart cards (synchronous interface) (*)*

- '104' type EEPROM non-reloadable token counter cards, including:
  Gemplus GPM103,
  Siemens SLE 4406
  Siemens SLE4436 and SLE5536 (firmware 2.10 onwards)
- Cards following the I^2C bus protocol (free memory cards) with memory capacity up to 16 Kbit and minimum 4 bytes page write capability, including:
  Atmel AT24C01/02/04/08/16
  Gemplus GFM2K, GFM4K
  SGS-Thomson ST14C02C,14C04C
- Siemens SLE4432/4442 intelligent 256 bytes EEPROM with write protect function:
  SLE 4432, SLE 4442
- Siemens SLE 4418/4428 intelligent 1K bytes EEPROM with write-protect function:
  SLE 4418, SLE 4428

NOTE (*) – SAM READER DOES NOT SUPPORT FOR MEMORY-BASED SMART CARD

3.2 *Microcontroller-based smart cards (asynchronous interface)*

The ACR30 supports EEPROM microcontroller-based cards with internal programming voltage (VPP) generation and the following programming parameters transmitted in the ATR:

PI1 = 0 or 5
I = 25 or 50

The ACR30 performs the Protocol and Parameters Selection (PPS) procedure as specified *in ISO7816-3:1997.*

When the card ATR indicates the specific operation mode (TA_2 present; bit b5 of TA_2 must be 0) and that particular mode is not supported by the ACR30, the reader will reset the card to set it to negotiable mode. If the card cannot be set to negotiable mode, the reader will reject the card.

When the card ATR indicates the negotiable mode (TA_2 not present) and communication parameters other than the default parameters, the ACR30 will execute the PPS and try to use the communication parameters

that the card suggested in its ATR. If the card does not accept the PPS, the reader will use the default parameters (F=372, D=1).
For the meaning of the aforementioned parameters, please refer to *ISO7816, part 3.*

4. Smart Card Interface

The interface between the ACR30 and the inserted smart card follows the specifications of *ISO7816-3* with certain restrictions or enhancements to increase the practical functionality of the ACR30.

4.1 Smart Card Power Supply VCC (C1)

The current consumption of the inserted card must not be higher than **50mA**.

4.2 Programming Voltage VPP (C6)

According to ISO 7816-3, the smart card contact C6 (VPP) supplies the programming voltage to the smart card. Since all common smart cards in the market are EEPROM based and do not require the provision of an external programming voltage, the contact C6 (VPP) has been implemented as a normal control signal in the ACR30. The electrical specifications of this contact are identical to those of the signal RST (at contact C2).

4.3 Card Type Selection

The controlling PC has to always select the card type through the proper command sent to the ACR30 prior to activating the inserted card. This includes both the memory cards and MCU-based cards.
For MCU-based cards the reader allows to select the preferred protocol, T=0 or T=1. However, this selection is only accepted and carried out by the reader through the PPS when the card inserted in the reader supports both protocol types. Whenever an MCU-based card supports only one protocol type, T=0 or T=1, the reader automatically uses that protocol type, regardless of the protocol type selected by the application.

4.4 Interface for Microcontroller-based Cards

For microcontroller-based smart cards only the contacts C1 (VCC), C2 (RST), C3 (CLK), C5 (GND) and C7 (I/O) are used. A frequency of 3.6864 / 4 MHz is applied to the CLK signal (C3).

4.5 Card Tearing Protection

The ACR30 provides a mechanism to protect the inserted card when it is suddenly withdrawn while it is powered up. The power supply to the card and the signal lines between the ACR30 and the card are immediately deactivated when the card is being removed. As a general rule, however, to avoid any electrical damage, **a card should only be removed from the reader while it is powered down.**

NOTE - The ACR30 does never by itself switch on the power supply to the inserted card. This must explicitly be done by the controlling computer through the proper command sent to the reader.

5. Power Supply

The ACR30 requires a voltage of 5V DC, 100mA regulated power supply. The ACR30 gets the power supply from PC (through the cable supplied along with each type of reader).

Status LEDs

Green LED on the front of the reader indicate the activation status of the smart card interface:

Green LED - Indicates power supply to the smart card is switched on, i.e., the smart card is activated.

6. Serial Interface

The ACR30 is connected to a computer through a serial asynchronous interface following the RS-232 standard.

6.1 Communication Parameters

The following communication parameters are used by the ACR30 and cannot be modified by the host computer:

Transmission protocol	:	serial asynchronous
Parity	:	none
Data Bits	:	8
Stop Bits	:	1
Handshake	:	through CTS

The ACR30 provides two means to select the transmission speed (baud rate) used by the reader in the normal operation, by hardware and/or by software.

6.1.1 Hardware Baud Rate

The default hardware baud rate setting is 9600 bps.

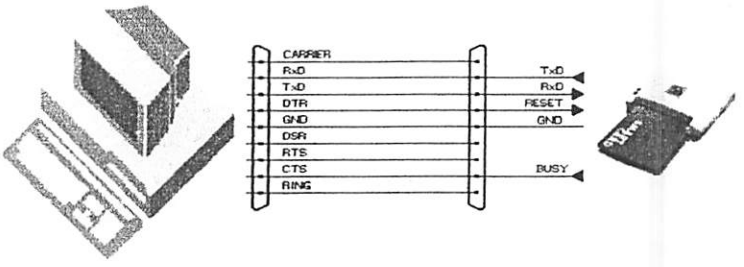
6.1.2 Software Baud Rate Selection

The *SET_PROTOCOL* command allows setting the transmission speed (baud rate) and a delay time inserted between the bytes transmitted by the reader to the PC.

Please note that the setting made with this command is volatile and will be lost when the reader is being reset or powered up next time.

6.2 Interface Wiring

For the communication between the ACR30 and a computer, five lines of the RS-232 interface are used: RxD, TxD, CTS, DTR and GND.



RS-232 Interface Wiring

Pin	PC	Cyber-mouse	Function
2	RxD	TxD	Data transmitted from PC to ACR30.
3	TxD	RxD	Data transmitted from ACR30 to PC.
4	DTR	RESET	RESET input signal. Allows performing hardware reset of the reader module through the RS-232 interface. Applying a logic '1' signal (negative voltage according to the RS-232 convention) to this pin causes a hardware reset of the ACR30.
5	GND	GND	Reference voltage level for power supply and serial interface.
8	CTS	BUSY	CTS (Clear To Send) signal to the PC. Indicates to the PC whether the ACR30 is ready to receive the next command. A logic '0' signal (positive voltage according to the RS-232 convention) is applied to this pin while the ACR30 is executing a command. Only when a '1' signal (negative voltage according to the RS-232 convention) is present at this pin can the PC send a command to the ACR30.

NOTE - Communication problems between the ACR30 and a PC can occur if a 25 pin to 9 pin RS-232 adapter or a cable is used in which not all 9 signal lines are connected. Adapters supplied with computer mouse frequently have not all lines connected. For the correct operation of the reader, use only a 9 pin to 25pin adapter and a serial interface cable in which all 9 signal lines are connected!

NOTE - To prevent any radio interference between the ACR30 and other electrical and electronic equipment, do not use an RS-232 cable longer than 3 meters!

7. USB Interface

The ACR30 is connected to a computer through a USB following the USB standard.

7.1 Communication Parameters

The ACR30 is connected to a computer through USB as specified in the USB Specification.

The ACR30 is working in low speed mode, i.e. 1.5 Mbps.

USB Interface Wiring

Pin	Signal	Function
1	V_{BUS}	+5V power supply for the reader
2	D-	Differential signal transmits data between ACR30 and PC.
3	D+	Differential signal transmits data between ACR30 and PC.
4	GND	Reference voltage level for power supply

NOTE - In order for the ACR30 functioning properly through USB interface, either ACS proprietary device drive or ACS PC/SC device driver has to be installed. Please refer to the *Device Driver Installation Guide* for more detail.

8. Communication protocol

In the normal operation, the ACR30 acts as a slave device with regard to the communication between a computer and the reader. The communication is carried out in the form of successive command-response exchanges. The computer transmits a command to the reader and receives a response from the reader after the command has been executed. A new command can be transmitted to the ACR30 only after the response to the previous command has been received.

There are two cases where the reader transmits data without having received a command from the computer, namely, the Reset Message of the reader and the Card Status Message.

8.1 Command

8.1.1 Normal Command (Length < 255 bytes)

A command consists of four protocol bytes and a variable number of data bytes and has the following structure:

byte	1	2	3	4 ... N+3 (0<N<255)	N+4
	Header	Instruction	Data length = N	Data	Checksum

Header Always 01_H to indicate the start of a command.

Instruction The instruction code of the command to be carried out by the ACR30

Data Length Number of subsequent data bytes. (0 < N < 255)

Data Data contents of the command.

For a READ command, for example, the data bytes would specify the start address and the number of bytes to be read. For a WRITE command, the data bytes would specify the start address and the data to be written to the card.

The data bytes can represent values to be written to a card and/or command parameters such as an address, a counter, etc.

Checksum The checksum is computed by XORing all command bytes including header, instruction, data length and all data bytes.

The following example shows the structure of a command with instruction code = 91_H and three data bytes with the values 11_H, 22_H and 33_H, respectively:

byte	1	2	3	4	5	6	7
	01_H	91_H	03_H	11_H	22_H	33_H	93_H

8.1.2 Extended Command

A command consists of six protocol bytes and a variable number of data bytes and has the following structure:

byte	1	2	3	4	5	6 ... N+5 (N>0)	N+6
	Header	Instruction	Data Length = N			Data	Checksum
			FF_H	Data Length N			

Header Always 01_H to indicate the start of a command.

Instruction The instruction code of the command to be carried out by the ACR30.

Data Length Number of subsequent data bytes, and is encoded in 3 bytes. The first byte is FF_H. The second byte and the third byte represent data length N.

Data Data contents of the command.

For a READ command, for example, the data bytes would specify the start address and the number of bytes to be read. For a WRITE command, the data bytes would specify the start address and the data to be written to the card.

The data bytes can represent values to be written to a card and/or command parameters such as an address, a counter, etc.

Checksum The checksum is computed by XORing all command bytes including header, instruction, data length and all data bytes.

8.2 Response

The response from the ACR30 to any command depends if the command where received by the reader without error (e.g., checksum error).

8.2.1 No transmission error with normal response (Length < 255 bytes)

The response by the ACR30 to a correctly received command consists of three protocol bytes, two status bytes and a variable number of data bytes and has the following structure:

byte	1	2	3	4	5 ... N+4 (0<N<255)	N+5
	Header	SW1	SW2	Data length = N	Data	Checksum

Header Always 01_H to indicate the start of the response.

SW1 Indicates the command execution status:

90_H = command successfully executed

60_H = error in command data; command cannot be executed

67_H = error detected in command execution

FF_H = status message initiated by the reader

SW2 Further qualification of the command execution status.

A table listing the possible values of the status bytes SW1 and SW2 and the corresponding meaning is given in Appendix B.

Data Length Number of subsequent data bytes (0 < N < 255)

Data Data contents of the command.

For a *READ_DATA* command, for example, the data bytes would contain the contents of the memory addresses read from the card. The data bytes can represent values read from the card and/or status information.

Checksum The checksum is computed by XORing all response bytes including header, status bytes, data length and all data bytes.

The following example shows the structure of the response to a command which has successfully been executed and which returns three data bytes with the values 11_H, 22_H and 33_H, respectively:

byte	1	2	3	4	5	6	7	8
	01_H	90_H	00_H	03_H	11_H	22_H	33_H	92_H

8.2.2 No transmission error with extended response

The response by the ACR30 to a correctly received command consists of three protocol bytes, two status bytes and a variable number of data bytes and has the following structure:

byte	1	2	3	4	5	6	7 ... N+6 (N>0)	N+7
	Header	SW1	SW2	Data length = N			Data	Checksum
				FF_H	Data Length N			

Header Always 01_H to indicate the start of the response.

SW1 Indicates the command execution status:

90_H = command successfully executed

60_H = error in command data; command cannot be executed

67_H = error detected in command execution

FF_H = status message initiated by the reader

SW2 Further qualification of the command execution status.

A table listing the possible values of the status bytes SW1 and SW2 and the corresponding meaning is given in Appendix B.

Data Length Number of subsequent data bytes, and is encoded in 3 bytes. The first byte is FF_H. The second byte and the third byte represent data length N.

Data Data contents of the command.

For a *READ_DATA* command, for example, the data bytes would contain the contents of the memory addresses read from the card. The data bytes can represent values read from the card and/or status information.

Checksum The checksum is computed by XORing all response bytes including header, status bytes, data length and all data bytes.

8.2.3 Transmission error

If the receiving party of a command (i.e., the ACR30) or a response (i.e., the computer) detects an error in the data length or the checksum of a command, it disregards the received data and sends a "NOT ACKNOWLEDGE" message to the transmitting party upon completion of the faulty transmission. The "NOT ACKNOWLEDGE" message consists of two bytes:

byte	1	2
	05_H	05_H

If the ACR30 responds with a 'NOT ACKNOWLEDGE' message to a command from the computer, the computer would normally transmit the command again. If the computer detects a transmission error in a response from the ACR30, it can send the 'NOT ACKNOWLEDGE' to the reader upon which the reader will transmit the most recent response again.

8.3 Reset Message

A reset of the reader occurs automatically whenever the reader is being powered up. A reset can also be actuated through the RS-232/USB interface. In either case the reader transmits **one time** a Reset Message, which has the same structure as the normal response to a command and the following contents:

byte	1	2	3	4	5	6
	Header	**SW1**	**SW2**	**Data length**	**Data**	**Checksum**
	01_H	FF_H	00_H	01_H	BAUD=12_H	

BAUD Indicates the hardware baud rate setting (default baud rate), which is set to 9600 bps (this is only valid in the RS232 reader).

The reader does not expect an acknowledge signal from the computer. After transmitting the Reset Message the reader is waiting for the first command from the computer.

8.4 Card Status Message

When a card is being inserted into the reader or an inserted card is being removed from the reader while the reader is idle, i.e., not executing a command, the reader transmits a Card Status Message to notify the host computer of the change in the card insertion status.

In a system where these unsolicited messages from the reader to the computer are not desired, they can be disabled with the *SET_NOTIFICATION* command. Please note that the setting made with this command is

volatile and will be lost with the next reader reset or power up. By default, the Card Status Message will be transmitted by the reader after a reset.

The Card Status Messages have the following structure and contents:

Card Status Message for Card Insertion

byte	1	2	3	4	5
	Header	SW1	SW2	Data length	Checksum
	01_H	FF_H	01_H	00_H	FF_H

Card Status Message for Card Removal

byte	1	2	3	4	5
	Header	SW1	SW2	Data length	Checksum
	01_H	FF_H	02_H	00_H	FC_H

A card status message is transmitted only **once** for every card insertion or removal event. The reader does not expect an acknowledge signal from the computer. After transmitting a status message, the reader waits for the next command from the computer.

NOTE - If the card is being removed from the reader while a card command is being executed, the reader will transmit a normal response to the computer with the response status bytes indicating the card removal during command execution (see *Appendix B: Response Status Codes*).

8.5 Transmission Protocol

The start of a command (to the reader) or a response (from the reader, including the Reset Message and Card Status Messages) is indicated by the respective party through the transmission of the single byte Start-of-Text (STX) character with the value 02_H.
The end of a command or response is indicated through the single byte End-of-Text (ETX) character with the value 03_H.

Within the command and response transmission only ASCII characters representing the hexadecimal (hex) digits 0...F are used. Each byte of a command or response is splitted into its upper and lower halfbyte (nibble). For each halfbyte is transmitted the ASCII character representing the respective hex digit value. For example, to transmit the data byte $3A_H$, two bytes are actually sent on the interface, namely, 33_H (ASCII code for '3') followed by 41_H (ASCII code for 'A'):

Data byte value	$3A_H$	
Transmitted values	33_H = '3'	41_H = 'A'

The following example shows the transmission of a command with instruction code $A2_H$ and one data byte with the value $3D_H$. The command has the following structure:

byte	1	2	3	4	5
	Header	Instruction	Data length	Data	Checksum
	01_H	$A2_H$	01_H	$3D_H$	$9F_H$

This command is transmitted on the serial interface in 12 bytes as follows:

byte	1	2	3	4	5	6	7	8	9	10	11	12
	STX	'0'	'1'	'A'	'2'	'0'	'1'	'3'	'D'	'9'	'F'	ETX
	02_H	30_H	31_H	41_H	32_H	30_H	31_H	33_H	44_H	39_H	46_H	03_H

For the representation of the hex halfbyte values as the corresponding ASCII characters in commands, the ACR30 accepts both upper case characters 'A' ... 'F' (41_H ... 46_H) and lower case characters 'a' ... 'f' (61_H ... 66_H):

byte	1	2	3	4	5	6	7	8	9	10	11	12
	STX	'0'	'1'	'A'	'2'	'0'	'1'	'3'	'D'	'9'	'F'	ETX
	02_H	30_H	31_H	41_H	32_H	30_H	31_H	33_H	44_H	39_H	46_H	03_H

... is equivalent to:

byte	1	2	3	4	5	6	7	8	9	10	11	12
	STX	'0'	'1'	'a'	'2'	'0'	'1'	'3'	'd'	'9'	'f'	ETX
	02_H	30_H	31_H	61_H	32_H	30_H	31_H	33_H	64_H	39_H	66_H	03_H

In its response messages, the ACR30 uses upper case characters 'A' ... 'F'.

9. Commands

The commands executed by the ACR30 can generally be divided into two categories, namely, Control Commands and Card Commands.

Control Commands control the internal operation of the ACR30. They do not directly affect the card inserted in the reader and are therefore independent of the selected card type.

Card Commands are directed toward the card inserted in the ACR30. The structure of these commands and the data transmitted in the commands and responses depend on the selected card type.

9.1 Control Commands

9.1.1 GET_ACR_STAT

This command returns relevant information about the particular ACR30 model and the current operating status, such as, the firmware revision number, the maximum data length of a command and response, the supported card types, and whether a card is inserted and powered up.

Command format

Instruction Code	Data length
01_H	00_H

Response data format

INTERNAL	MAX_C	MAX_R	C_TYPE	C_SEL	C_STAT

INTERNAL 10 bytes data for internal use only

MAX_C The maximum number of command data bytes.

MAX_R The maximum number of data bytes that can be requested to be transmitted in a response.

C_TYPE The card types supported by the ACR30. This data field is a bitmap with each bit representing a particular card type. A bit set to '1' means the corresponding card type is supported by the reader and can be selected with the *SELECT_CARD_TYPE* command. The bit assignment is as follows:

byte	1								2							
card type	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

See Appendix A for the correspondence between these bits and the respective card types.

C_SEL The currently selected card type as specified in a previous *SELECT_CARD_TYPE* command. A value of 00_H means that no card type has been selected.

C_STAT Indicates whether a card is physically inserted in the reader and whether the card is powered up:

00_H : no card inserted

01_H : card inserted, not powered up

03_H : card powered up

9.1.2 SET_PROTOCOL

This command is used to control the line speed of the communication channel between ACR30 reader and host device. The line speed of the communication is controlled by two factors, namely, the Delay Factor and the Baud Rate.

Command format

Instruction Code	Data length	Data
		DELAY N
03_H	01_H	

to change only the Delay Factor (for RS232 reader only), or

Instruction Code	Data length	Data	
		DELAY N	BAUD RATE
03_H	02_H		

to change the Delay Factor and the Baud Rate (for RS232 reader only).

DELAY Determines the time delay inserted by the ACR30 between two consecutive bytes sent in order to adapt to slower host system speeds. The time delay is given by N * 0.1msec, with N ranging from 0 ... 255 (00 - FF_H). The default value is N = 0 (delay changes only valid on RS232 reader).

BAUD RATE Selects the baud rate (bps) of the serial interface between reader and host system. The default hardware baud rate is 9600 bps. (baud rate changes only valid on RS232 reader).

BAUD RATE	Serial baud rate (bps)
12_H	9600
11_H	19200
10_H	38400
03_H	14400
02_H	28800
01_H	57600
00_H	115200

Response data format

No response data

The new protocol becomes effective by the completion of the *SET_PROTOCOL* command, immediately **after the ACR30 has sent out the response string to the *SET_PROTOCOL* command.**

9.1.3 SELECT_CARD_TYPE

This command sets the required card type. The firmware in the ACR30 adjusts the communication protocol between reader and the inserted card according to the selected card type.

Command format

Instruction Code	Data length	Data
		TYPE
02_H	01_H	

TYPE See Appendix A for the value to be specified in this command for a particular card to be used.

Response data format

No response data

9.1.4 RESET

This section describes the *RESET* command only for the case when no card type is selected or when the card type 00_H is selected. For all other cases, please refer to the specific section described for each individual card type.

Command format

Instruction Code	Data length
80_H	00_H

Response data format

ATR			

ATR The answer-to-reset string returned by the card.

The return status code for this command is 90 00_H when the inserted card is a T=0 card, 90 01_H when the inserted card is a T=1 card, and 90 10_H when the inserted card is a memory card; otherwise the status code is 60 20_H.

9.1.5 SET_NOTIFICATION

This command disables / enables the Card Status Messages transmitted by the reader to notify the host computer of the insertion or removal of a card.

Command format

Instruction Code	Data length	Data
		NOTIFY
06_H	01_H	

NOTIFY Specifies whether the Card Status Message shall be transmitted to notify the host computer of card insertion / removal

01_H : transmit Card Status Message

02_H : do not transmit Card Status Message

Response data format

No response data

9.1.6 SET_OPTION

This command selects the options for the reader.

Command format

Instruction Code	Data length	Data
		Option
07_H	01_H	

Option Bit 0 (LSB bit): Select for PPS mode

Specifies reader ⇔ card communication speed

0 : baud rate to/from the card is from 9600 bps to 96000 bps (default)

1 : baud rate to/from the card is at 9600 bps only

Bit 4 : Select for EMV mode

Specifies whether the reader is in EMV mode

0 : reader not in EMV mode (default)

1 : reader in EMV mode

Bit 2, 3, 5, 6 and 7

Reserved

Response data format

No response data

9.2 Card Commands

The available commands and the parameters specified in the card commands as well as the data transmitted in the response from the ACR30 depend on the selected card type.

9.2.1 '104' - type non-reloadable Token Counter Cards (*)

9.2.1.1 RESET (*)

This command powers up the card inserted in the card reader and performs a card reset.

If the card is powered up when the command is being issued, only a reset of the card is carried out; the power supply to the card is not switched off.

Command format

Instruction Code	Data length
80 H	00 H

Response data format

ATR			

ATR Four bytes Answer-To-Reset read from the card.
The ATR bytes are read from the card with LSB first, i.e., the first bit read from the card is the LSB of the first ATR byte.

9.2.1.2 POWER_OFF (*)

This command powers off the card inserted in the card reader.

Command format

Instruction Code	Data length
81 H	00 H

Response data format

No response data

9.2.1.3 READ_DATA (*)

To read the specified number of bytes from the specified address of the card inserted. The bytes are read from the card with LSB first, i.e., the bit at card address 0 is regarded as the LSB of byte 0.

Command format

Instruction Code	Data length	Data		
			ADDR	LEN
90 H	03 H	00 H		

ADDR Byte address of first byte to be read from the card

LEN Number N of data bytes to be read from the card
(0 < N ≤ MAX_R)

Response data format

BYTE 1	BYTE 2	BYTE 3	...	...	BYTE N

BYTE x Data bytes read from the card memory

9.2.1.4 WRITE_DATA (*)

To write one byte to the specified address of the card inserted. The byte is written to the card with LSB first, i.e., the bit at card address 0 is regarded as the LSB of byte 0.

Two different WRITE modes are available for this card type, which are distinguished by a flag in the command data field:

a) **Write**

The byte value specified in the command is written to the specified address. This command can be used for writing personalization data and counter values to the card.

b) **Write with carry**

The byte value specified in the command is written to the specified address and the command is sent to the card to erase the next lower counter stage. This write-mode can therefore only be used for updating the counter value in the card.

With either write mode, the byte at the specified card address is not erased prior to the write operation and, hence, memory bits can only be programmed from '1' to '0'.
The backup mode available in the SLE4436 card can be enabled or disabled in the write operation.

Command format

Instruction Code	Data length	Data			
			ADDR	MODE	BYTE
91_H	04_H	00_H			

ADDR Byte address of byte to be written

MODE Specifies the write mode and backup option (SLE4436)

00_H : write

01_H : write with carry

02_H : write with backup enabled

03_H : write with carry and with backup enabled

BYTE Byte value to be written to the card

Response data format

No response data

9.2.1.5 PRESENT_TRANSPORT_CODE (*)

To submit the transport code to the card in order to enable the card personalization mode. The following actions are executed by the ACR30:

- search a '1' bit in the presentation counter and write the bit to '0'
- present the specified code to the card

The ACR30 does not try to erase the presentation counter after the code submission! The application software through a separate 'Write with carry' command must do this.

Command format

Instruction Code	Data length	Data					
	LEN	ADDR	BYTE 1	BYTE 2	...	...	BYTE N
92_H							

LEN Number of transport code bytes, N, + 1

ADDR Byte address of the presentation counter in the card

BYTE x Transport code

Response data format

No response data

9.2.1.6 AUTHENTICATE_CARD_SLE4436 (firmware 2.10 onwards) (*)

To read a card authentication certificate from SLE4436 card. The following actions are executed by the ACR30:

- select Key 1 or Key 2 in the card as specified in the command
- present the challenge data specified in the command to the card
- generate the specified number of CLK pulses for each bit of authentication data computed by the card
- read 16 bits of authentication data from the card
- reset the card to normal operation mode

The ACR30 returns the 16 bits of authentication data calculated by the card in the response.

Command format

Instruction Code	Data length	Data					
		KEY	CLK_CNT	BYTE 1	...	...	BYTE 6
96_H	08_H						

KEY Key to be used for the computation of the authentication certificate:
00_H : key 1
01_H : key 2

CLK_CNT Number of CLK pulses to be supplied to the card for the computation of each bit of the authentication certificate.

BYTE 1...6 Card challenge data

Response data format

CERT	

CERT 16 bits of authentication data computed by the card. The LSB of BYTE 1 is the first authentication bit read from the card.

9.2.1.7 AUTHENTICATE_CARD_SLE5536 (firmware 2.10 onwards) (*)

To read a card authentication certificate from SLE5536 card. The following actions are executed by the ACR30:

- select Key 1 or Key 2 in the card as specified in the command
- present the challenge data specified in the command to the card
- generate the specified number of CLK pulses for each bit of authentication data computed by the card
- read 16 bits of authentication data from the card
- reset the card to normal operation mode

The ACR30 returns the 16 bits of authentication data calculated by the card in the response.

Command format

Instruction Code	Data length	Data					
		KEY	CLK_CNT	BYTE 1	...	...	BYTE 6
96_H	08_H						

KEY Key to be used for the computation of the authentication certificate:
00_H : key 1 with no cipher block chaining
01_H : key 2 with no cipher block chaining
80_H : key 1 with cipher block chaining
81_H : key 2 with cipher block chaining

CLK_CNT Number of CLK pulses to be supplied to the card for the computation of each bit of the authentication certificate.

BYTE 1...6 Card challenge data

Response data format

CERT	

CERT 16 bits of authentication data computed by the card. The LSB of BYTE 1 is the first authentication bit read from the card.

Note (*) – SAM Reader does not support for memory cards

9.2.2 I2C-Bus cards (standard and extended addressing) (*)

9.2.2.1 RESET (*)

This command powers up the card inserted in the card reader. No action is taken if the card is powered up when the command is being issued.

Command format

Instruction Code	Data length
80_H	00_H

Response data format

No response data

9.2.2.2 POWER_OFF (*)

This command powers off the card inserted in the card reader.

Command format

Instruction Code	Data length
81_H	00_H

Response data format

No response data

9.2.2.3 READ_DATA (*)

To read the specified number of bytes from the specified address of the card inserted.

Command format

Instruction Code	Data length	Data		
		ADDR		LEN
90_H	03_H			

ADDR Byte address of first byte to be read from the card. The high byte of the address is specified as the first byte of ADDR.

LEN Number N of data bytes to be read from the card

(0 < N ≤ MAX_R)

Response data format

BYTE 1	BYTE 2	BYTE 3	...	...	BYTE N

BYTE x Data bytes read from the card memory

9.2.2.4 WRITE_DATA (*)

To write the specified data bytes to the specified address of the card inserted.

Command format

Instruction Code	Data length	Data					
	LEN	ADDR		BYTE 1	...	...	BYTE N
91_H							

LEN Number of data bytes to be written to the card, N, + 2

ADDR Byte address in the card of the first byte to be written. The high byte of the address is specified as the first byte of ADDR.

BYTE x Byte values to be written to the card starting at address ADDR. BYTE 1 is written to address ADDR; BYTE N is written to address ADDR+N-1.

Response data format

No response data

Note (*) – SAM Reader does not support for memory cards

9.2.3 Siemens SLE 4432/4442 intelligent 256 Byte Memory Card (*)

9.2.3.1 RESET (*)

This command powers up the card inserted in the card reader and performs a card reset.

If the card is powered up when the command is being issued, only a reset of the card is carried out, the power supply to the card is not switched off.

Command format

Instruction Code	Data length
80 H	00 H

Response data format

ATR			

ATR Four bytes Answer-To-Reset read from the card.
The ATR bytes are read from the card with LSB first, i.e., the first bit read from the card is the LSB of the first ATR byte.

9.2.3.2 POWER_OFF (*)

This command powers off the card inserted in the card reader.

Command format

Instruction Code	Data length
81 H	00 H

Response data format

No response data

9.2.3.3 READ_DATA (*)

To read the specified number of bytes from the specified address of the card inserted.

Command format

Instruction Code	Data length	Data		
		ADDR		LEN
90 H	03 H			

ADDR Byte address of first byte to be read from the card. The high byte of the address is specified as the first byte of ADDR.

LEN Number N of data bytes to be read from the card (0 < N ≤ MAX_R)

Response data format

BYTE 1	BYTE 2	BYTE 3	...	BYTE N	PROT 1	...	PROT L

BYTE x Data bytes read from the card memory

PROT y Bytes containing the protection bits of the data bytes read (0...4 bytes)

The protection bits are only returned in the response data if the start address ADDR specified in the command is < 20_H, i.e., it is lying within the first 32 bytes of card memory which can be write protected.

Accordingly, the number of PROT bytes returned depends on how many of the data bytes read lie within the protectable area. If all data bytes read are outside the protectable area, only the data bytes read from the card are returned in the response, no PROT bytes are returned.

The arrangement of the protection bits in the PROT bytes is as follows:

PROT 1								PROT 2								....							
P8	P7	P6	P5	P4	P3	P2	P1	P16	P15	P14	P13	P12	P11	P10	P9	..	..	..	..	..	..	P18	P17
													1										

Px is the protection bit of BYTE x in the response data

'0' : byte is write protected

'1' : byte can be written

9.2.3.4 WRITE_DATA (*)

To write the specified data bytes to the specified address of the card inserted.

Command format

Instruction Code	Data length	Data					
	LEN	ADDR		BYTE 1	...	...	BYTE N
91_H							

LEN Number of data bytes to be written to the card, N, + 2

ADDR Byte address in the card of the first byte to be written. The high byte of the address is specified as the first byte of ADDR.

BYTE x Byte values to be written to the card starting at address ADDR. BYTE 1 is written to address ADDR; BYTE N is written to address ADDR+N-1.

Response data format

No response data

9.2.3.5 WRITE_PROTECTION (*)

To write the protection bits for the specified addresses in the card.

Each of the bytes specified in the command is internally in the card compared with the byte stored at the specified address and if the data match, the corresponding protection bit is irreversibly programmed to '0'.

Command format

Instruction Code	Data length	Data					
	LEN	ADDR		BYTE 1	...	...	BYTE N
94_H							

LEN Number of data bytes to be write protected, N, + 2

ADDR Byte address in the card of the first byte to be write protected. The high byte of **the address is specified as the first byte of ADDR.**

BYTE x Byte values to be compared with the data in the card starting at address ADDR. BYTE 1 is compared with the data at address ADDR; BYTE N is compared with the data at address ADDR+N-1.

Response data format

No response data

9.2.3.6 PRESENT_CODE (only SLE 4442) (*)

To submit the secret code to the card to enable the write operation with the SLE 4442 card.

The following actions are executed by the ACR30:

- search a '1' bit in the presentation error counter and write the bit to '0'
- present the specified code to the card
- try to erase the presentation error counter

Command format

Instruction Code	Data length	Data		
		CODE		
92_H	03_H			

CODE Three bytes secret code (PIN)

Response data format

ERRCNT	CODE		

ERRCNT The value of the presentation error counter after the code presentation.

CODE · The three bytes secret code read from the card.
If the correct code has been presented to the card, the value of ERRCNT is 07_H and the value of CODE is identical to the code data specified in the command.

9.2.3.7 CHANGE_CODE (only SLE 4442) (*)

To write the specified data as new secret code in the card.

The current secret code must have been presented to the card with the *PRESENT_CODE* command prior to the execution of this command!

Command format

Instruction Code	Data length	Data		
		CODE		
93_H	03_H			

CODE The three bytes new secret code (PIN)

Response data format

No response data

Note (*) – SAM Reader does not support for memory cards

8. Application Example (For serial port interface)

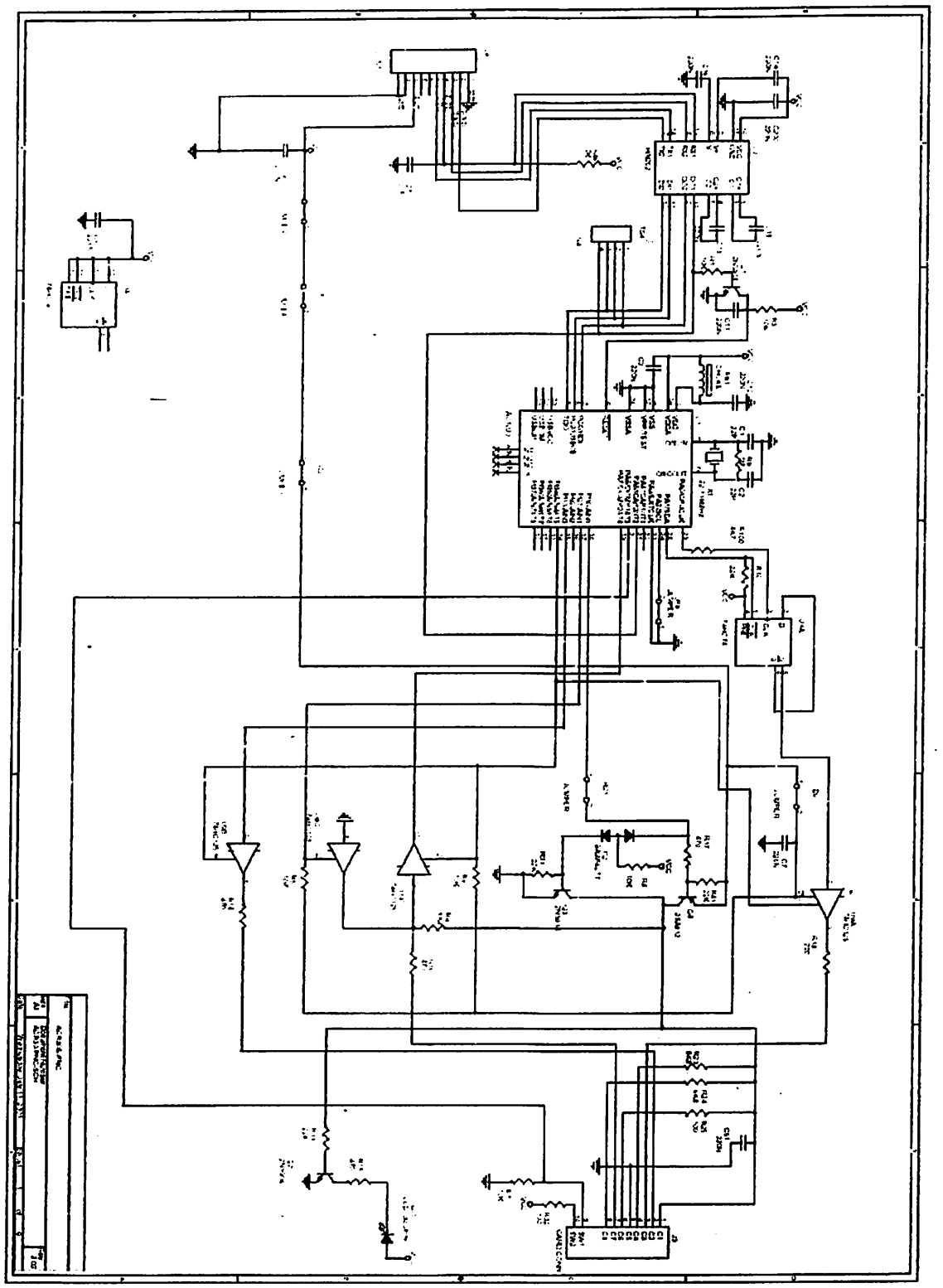


Figure 2. Card Reader Application of AC1030 (Serial connection)

19-0175; Rev 3; 5/96

MAXIM

±15kV ESD-Protected, +5V RS-232 Transceivers

General Description

The MAX202E–MAX213E, MAX232E/MAX241E line drivers/receivers are designed for RS-232 and V.28 communications in harsh environments. Each transmitter output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. The various combinations of features are outlined in the *Selection Guide*. The drivers and receivers for all ten devices meet all EIA/TIA 232E and CCITT V.28 specifications at data rates up to 120kbps, when loaded in accordance with the EIA/TIA-232E specification.

The MAX211E/MAX213E/MAX241E are available in 28-pin SO packages, as well as a 28 pin SSOP that uses 60% less board space. The MAX202E/MAX232E come in 16-pin narrow SO, wide SO, and DIP packages. The MAX203E comes in a 20-pin DIP/SO package, and needs no external charge-pump capacitors. The MAX205E comes in a 24-pin wide DIP package, and also eliminates external charge-pump capacitors. The MAX206E/MAX207E/MAX208E come in 24-pin SO, SSOP, and narrow DIP packages. The MAX232E/MAX241E operate with four 1µF capacitors, while the MAX202E/MAX206E/MAX207E/MAX208E/MAX211E/MAX213E operate with four 0.1µF capacitors, further reducing cost and board space.

Applications

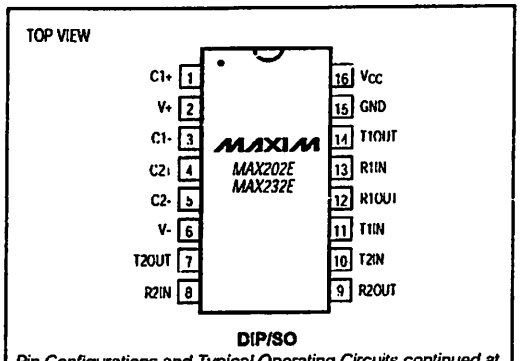
Notebook, Subnotebook, and Palmtop Computers
Battery-Powered Equipment
Hand-Held Equipment

Ordering Information appears at end of data sheet.

Features

- **ESD Protection for RS-232 I/O Pins:**
  ±15kV—Human Body Model
  ±8kV—IEC1000-4-2, Contact Discharge
  ±15kV—IEC1000-4-2, Air-Gap Discharge
- **Latchup Free (unlike bipolar equivalents)**
- **Guaranteed 120kbps Data Rate—LapLink™ Compatible**
- **Guaranteed 3V/µs Min Slew Rate**
- **Operate from a Single +5V Power Supply**

Pin Configurations



DIP/SO

Pin Configurations and Typical Operating Circuits continued at end of data sheet.

Selection Guide

PART	No. of RS-232 DRIVERS	No. of RS-232 RECEIVERS	RECEIVERS ACTIVE IN SHUTDOWN	No. of EXTERNAL CAPACITORS	LOW-POWER SHUTDOWN	TTL THREE-STATE
MAX202E	2	2	0	4 (0.1µF)	No	No
MAX203E	2	2	0	None	No	No
MAX205E	5	5	0	None	Yes	Yes
MAX206E	4	3	0	4 (0.1µF)	Yes	Yes
MAX207E	5	3	0	4 (0.1µF)	No	No
MAX208E	4	4	0	4 (0.1µF)	No	No
MAX211E	4	5	0	4 (0.1µF)	Yes	Yes
MAX213E	4	5	2	4 (0.1µF)	Yes	Yes
MAX232E	2	2	0	4 (1µF)	No	No
MAX241E	4	5	0	4 (1µF)	Yes	Yes

LapLink is a registered trademark of Traveling Software, Inc.

±15kV ESD-Protected, +5V RS-232 Transceivers

ABSOLUTE MAXIMUM RATINGS

VCC ..... -0.3V to +6V
V+ ..... (VCC - 0.3V) to +14V
V- ..... -14V to +0.3V
Input Voltages
T_IN ..... -0.3V to (V+ + 0.3V)
R_IN ..... ±30V
Output Voltages
T_OUT ..... (V- - 0.3V) to (V+ + 0.3V)
R_OUT ..... -0.3V to (VCC + 0.3V)
Short-Circuit Duration, T_OUT ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin SO (derate 10.00mW/°C above +70°C) 800mW
24-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) 1.07W
24-Pin Wide Plastic DIP
(derate 14.29mW/°C above +70°C) 1.14W
24-Pin SO (derate 11.76mW/°C above +70°C) 941mW
24-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
28-Pin SO (derate 12.50mW/°C above +70°C) 1W
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX2__EC_ _ ..... 0°C to +70°C
MAX2__EE_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; VCC = +5V ±5% for MAX203E/205E/207E; C1–C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1–C4 = 1µF for MAX232E/241E, T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
VCC Supply Current	ICC	No load, T_A = +25°C	MAX202E/203E		8	15	mA
			MAX205E–208E		11	20	
			MAX211E/213E		14	20	
			MAX232E		5	10	
			MAX241E		7	15	
Shutdown Supply Current		T_A = +25°C, Figure 1	MAX205E/206E		1	10	µA
			MAX211E/241E		1	10	
			MAX213E		15	50	
LOGIC							
Input Pull-Up Current		T_IN = 0V (MAX205E–208E/211E/213E/241E)			15	200	µA
Input Leakage Current		T_IN = 0V to VCC (MAX202E/203E/232E)				±10	µA
Input Threshold Low	VIL	T_IN; EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX205E–208E/211E/241E)				0.8	V
Input Threshold High	VIH	T_IN		2.0			V
		EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX205E–208E/211E/241E)		2.4			
Output Voltage Low	VOL	R_OUT; IOUT = 3.2mA (MAX202E/203E/232E) or IOUT = 1.6mA (MAX205E/208E/211E/213E/241E)				0.4	V
Output Voltage High	VOH	R_OUT; IOUT = -1.0mA		3.5	VCC - 0.4		V
Output Leakage Current		$\overline{EN}$ = VCC, EN = 0V, 0V ≤ ROUT ≤ VCC, MAX205E–208E/211E/213E/241E outputs disabled			±0.05	±10	µA

ELECTRICAL CHARACTERISTICS (continued)

(VCC = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; VCC = +5V ±5% for MAX203E/205E/207E; C1–C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1–C4 = 1µF for MAX232E/241E; TA = TMIN to TMAX; unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EIA/TIA-232E RECEIVER INPUTS							
Input Voltage Range				-30		30	V
Input Threshold Low		TA = +25°C, VCC = 5V	All parts, normal operation	0.8	1.2		V
			MAX213E, $\overline{SHDN}$ = 0V, EN = VCC	0.6	1.5		
Input Threshold High		TA = +25°C, VCC = 5V	All parts, normal operation		1.7	2.4	V
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = VCC		1.5	2.4	
Input Hysteresis		VCC = 5V, no hysteresis in shutdown		0.2	0.5	1.0	V
Input Resistance		TA = +25°C, VCC = 5V		3	5	7	kΩ
EIA/TIA-232E TRANSMITTER OUTPUTS							
Output Voltage Swing		All drivers loaded with 3kΩ to ground (Note 1)		±5	±9		V
Output Resistance		VCC = V+ = V- = 0V, VOUT = ±2V		300			Ω
Output Short-Circuit Current					±10	±60	mA
TIMING CHARACTERISTICS							
Maximum Data Rate		RL = 3kΩ to 7kΩ, CL = 50pF to 1000pF, one transmitter switching		120			kbps
Receiver Propagation Delay	tPLHR, tPHLR	CL = 150pF	All parts, normal operation		0.5	10	µs
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = VCC		4	40	
Receiver Output Enable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2			600		ns
Receiver Output Disable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2			200		ns
Transmitter Propagation Delay	tPLHT, tPHLT	RL = 3kΩ, CL = 2500pF, all transmitters loaded			2		µs
Transition-Region Slew Rate		TA = +25°C, VCC = 5V, RL = 3kΩ to 7kΩ, CL = 50pF to 1000pF, measured from +3V to -3V or -3V to +3V, Figure 3		3	6	30	V/µs
ESD PERFORMANCE: TRANSMITTER OUTPUTS, RECEIVER INPUTS							
ESD-Protection Voltage		Human Body Model			±15		kV
		IEC1000-4-2, Contact Discharge			±8		
		IEC1000-4-2, Air-Gap Discharge			±15		

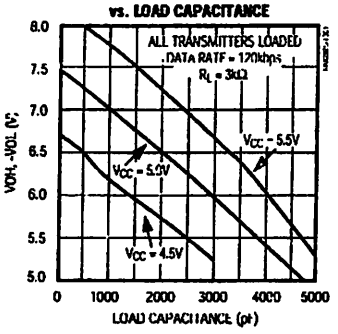
Note 1: MAX211EE_ _ tested with VCC = +5V ±5%.

±15kV ESD-Protected, +5V RS-232 Transceivers

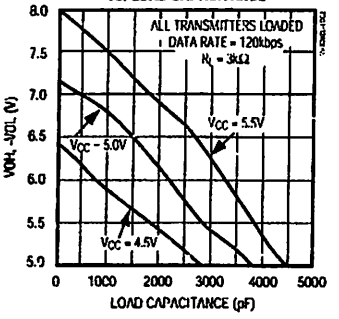
Typical Operating Characteristics

(Typical Operating Circuits, V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

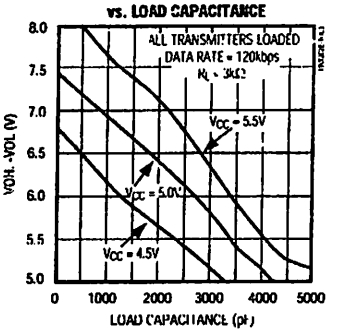
MAX232E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



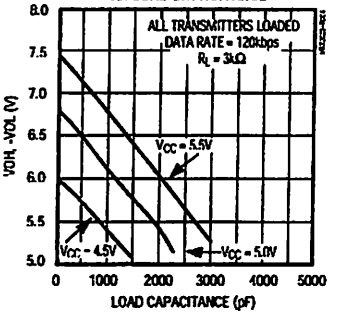
MAX202E/MAX203E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



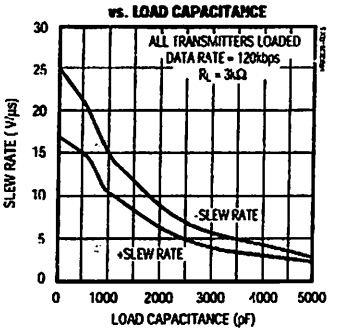
MAX241E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



MAX211E/MAX213E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



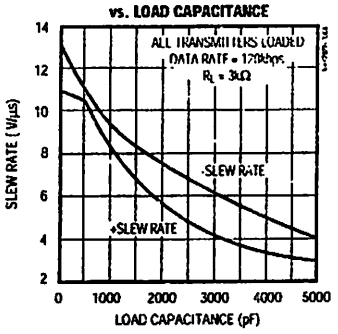
MAX211E/MAX213E/MAX241E
TRANSMITTER SLEW RATE
vs. LOAD CAPACITANCE



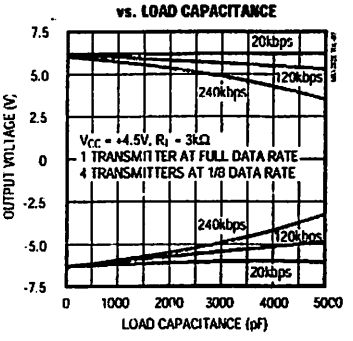
Typical Operating Characteristics (continued)

(Typical Operating Circuits, V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

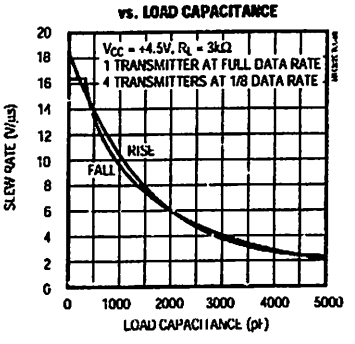
MAX202E/MAX203E/MAX232E TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



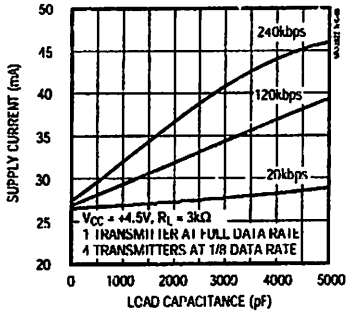
MAX205E–MAX208E TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



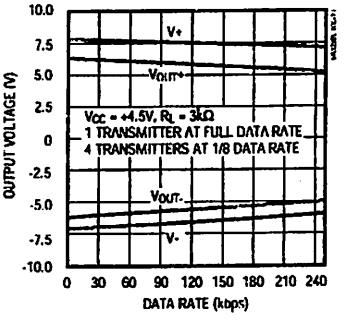
MAX205E–MAX208E TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



MAX205E–MAX208E SUPPLY CURRENT vs. LOAD CAPACITANCE



MAX205E–MAX208E OUTPUT VOLTAGE vs. DATA RATE



±15kV ESD-Protected, +5V RS-232 Transceivers

Pin Descriptions

MAX202E/MAX232E

PIN		NAME	FUNCTION
DIP/SO	LCC		
1, 3	2, 4	C1+, C1-	Terminals for positive charge-pump capacitor
2	3	V+	+2Vcc voltage generated by the charge pump
4, 5	5, 7	C2+, C2-	Terminals for negative charge-pump capacitor
6	8	V-	-2Vcc voltage generated by the charge pump
7, 14	9, 18	T_OUT	RS-232 Driver Outputs
8, 13	10, 17	R_IN	RS-232 Receiver Outputs
9, 12	12, 15	R_OUT	RS-232 Receiver Outputs
10, 11	13, 14	T_IN	RS-232 Driver Inputs
15	19	GND	Ground
16	20	Vcc	+4.5V to +5.5V Supply-Voltage Input
—	1, 6, 11, 16	N.C.	No Connect—not internally connected.

MAX203E

PIN		NAME	FUNCTION
DIP	SO		
1, 2	1, 2	T_IN	RS-232 Driver Inputs
3, 20	3, 20	R_OUT	RS-232 Receiver Outputs
4,19	4, 19	R_IN	RS-232 Receiver Inputs
5,18	5, 18	T_OUT	RS-232 Transmitter Outputs
6, 9	6, 9	GND	Ground
7	7	Vcc	+4.5V to +5.5V Supply-Voltage Input
8	13	C1+	Make no connection to this pin.
10, 16	11, 16	C2-	Connect pins together.
12, 17	10, 17	V-	-2Vcc voltage generated by the charge pump. Connect pins together.
13	14	C1-	Make no connection to this pin.
14	8	V+	+2Vcc voltage generated by the charge pump
11, 15	12, 15	C2+	Connect pins together.

MAX205E

PIN	NAME	FUNCTION
1–4, 19	T_OUT	RS-232 Driver Outputs
5, 10, 13, 18, 24	R_IN	RS-232 Receiver Inputs
6, 9, 14, 17, 23	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
7, 8, 15, 16, 22	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to Vcc.
11	GND	Ground
12	Vcc	+4.75V to +5.25V Supply Voltage
20	$\overline{EN}$	Receiver Enable—active low
21	SHDN	Shutdown Control—active high

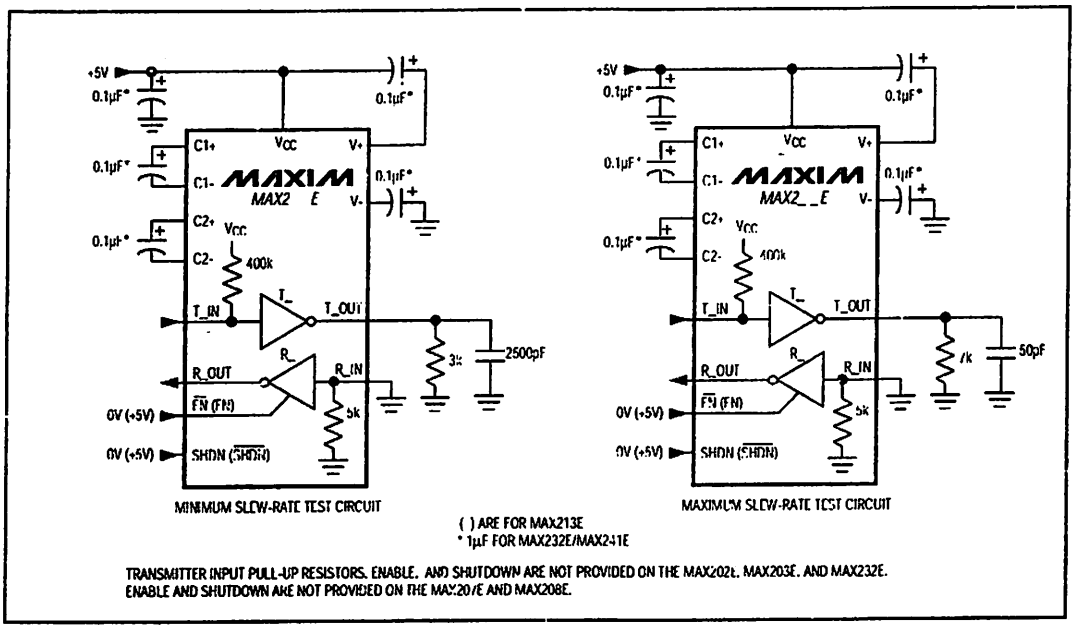


Figure 3. Transition Slew-Rate Circuit

Detailed Description

The MAX202E–MAX213E, MAX232E/MAX241E consist of three sections: charge pump voltage converters, drivers (transmitters), and receivers. These E versions provide extra protection against ESD. They survive ±15kV discharges to the RS-232 inputs and outputs, tested using the Human Body Model. When tested according to IEC1000-4-2, they survive ±8kV contact-discharges and ±15kV air-gap discharges. The rugged E versions are intended for use in harsh environments or applications where the RS-232 connection is frequently changed (such as notebook computers). The standard (non-"E") MAX202, MAX203, MAX205–MAX208, MAX211, MAX213, MAX232, and MAX241 are recommended for applications where cost is critical.

+5V to ±10V Dual Charge-Pump Voltage Converter

The +5V to ±10V conversion is performed by dual charge-pump voltage converters (Figure 4). The first charge pump converter uses capacitor C1 to double the +5V into +10V, storing the +10V on the output filter capacitor, C3. The second uses C2 to invert the +10V into -10V, storing the -10V on the V- output filter capacitor, C4.

In shutdown mode, V+ is internally connected to VCC by a 1kΩ pull-down resistor, and V- is internally connected to ground by a 1kΩ pull-up resistor.

RS-232 Drivers

With VCC = 5V, the typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver. The output swing is guaranteed to meet EIA/TIA-232E and V.28 specifications that call for ±5V minimum output levels under worst-case conditions. These include a 3kΩ load, minimum VCC, and maximum operating temperature. The open-circuit output voltage swings from (V+ - 0.6V) to V-.

Input thresholds are CMOS/TTL compatible. The unused drivers' inputs on the MAX205E–MAX208E, MAX211E, MAX213E, and MAX241E can be left unconnected because 400kΩ pull-up resistors to VCC are included on-chip. Since all drivers invert, the pull-up resistors force the unused drivers' outputs low. The MAX202E, MAX203E, and MAX232E do not have pull-up resistors on the transmitter inputs.

±15kV ESD-Protected, +5V RS-232 Transceivers

When in low-power shutdown mode, the MAX205E/MAX206E/MAX211E/MAX213E/MAX241E driver outputs are turned off and draw only leakage currents—even if they are back-driven with voltages between 0V and 12V. Below -0.5V in shutdown, the transmitter output is diode-clamped to ground with a 1kΩ series impedance.

RS-232 Receivers

The receivers convert the RS-232 signals to CMOS-logic output levels. The guaranteed 0.8V and 2.4V receiver input thresholds are significantly tighter than the ±3V thresholds required by the EIA/TIA-232E specification. This allows the receiver inputs to respond to TTL/CMOS-logic levels, as well as RS 232 levels.

The guaranteed 0.8V input low threshold ensures that receivers shorted to ground have a logic 1 output. The 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

Receiver inputs have approximately 0.5V hysteresis. This provides clean output transitions, even with slow rise/fall-time signals with moderate amounts of noise and ringing.

In shutdown, the MAX213E's R4 and R5 receivers have no hysteresis.

Shutdown and Enable Control (MAX205E/MAX206E/MAX211E/MAX213E/MAX241E)

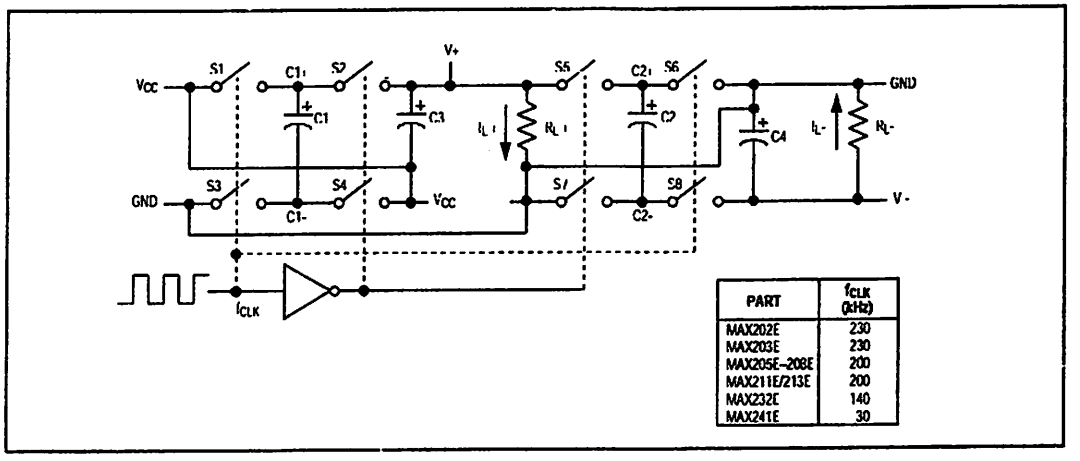
In shutdown mode, the charge pumps are turned off, V+ is pulled down to VCC, V- is pulled to ground, and the transmitter outputs are disabled. This reduces supply current typically to 1µA (15µA for the MAX213E). The time required to exit shutdown is under 1ms, as shown in Figure 5.

Receivers

All MAX213E receivers, except R4 and R5, are put into a high-impedance state in shutdown mode (see Tables 1a and 1b). The MAX213E's R4 and R5 receivers still function in shutdown mode. These two awake in shutdown receivers can monitor external activity while maintaining minimal power consumption.

The enable control is used to put the receiver outputs into a high-impedance state, to allow wire-OR connection of two EIA/TIA-232E ports (or ports of different types) at the UART. It has no effect on the RS-232 drivers or the charge pumps.

Note: The enable control pin is active low for the MAX211E/MAX241E (EN), but is active high for the MAX213E (EN). The shutdown control pin is active high for the MAX205E/MAX206E/MAX211E/MAX241E (SHDN), but is active low for the MAX213E (SHDN).



PART	fCLK (kHz)
MAX202E	230
MAX203E	230
MAX205E–208E	200
MAX211E/213E	200
MAX232E	140
MAX241E	30

Figure 4. Charge-Pump Diagram

The MAX213E's receiver propagation delay is typically 0.5µs in normal operation. In shutdown mode, propagation delay increases to 4µs for both rising and falling transitions. The MAX213E's receiver inputs have approximately 0.5V hysteresis, except in shutdown, when receivers R4 and R5 have no hysteresis.

When entering shutdown with receivers active, R4 and R5 are not valid until 80µs after $\overline{SHDN}$ is driven low. When coming out of shutdown, all receiver outputs are invalid until the charge pumps reach nominal voltage levels (less than 2ms when using 0.1µF capacitors).

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's E versions keep working without latchup, whereas competing RS-232 products can latch and must be powered down to remove latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ±8kV using the contact-discharge method specified in IEC1000-4-2
3) ±15kV using IEC1000-4-2's air-gap method.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 6a shows the Human Body Model, and Figure 6b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

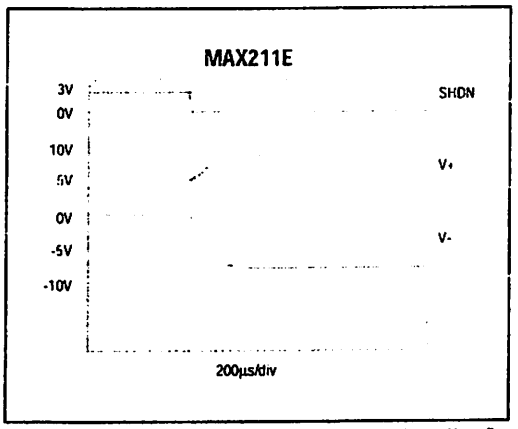


Figure 5. MAX211E V+ and V- when Exiting Shutdown (0.1µF capacitors)

Table 1a. MAX205E/MAX206E/MAX211E/MAX241E Control Pin Configurations

SHDN	EN	OPERATION STATUS	Tx	Rx
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All High-Z
1	X	Shutdown	All High-Z	All High-Z

X = Don't Care

Table 1b. MAX213E Control Pin Configurations

$\overline{SHDN}$	EN	OPERATION STATUS	Tx 1–4	Rx	
				1–3	4, 5
0	0	Shutdown	All High-Z	High-Z	High-Z
0	1	Shutdown	All High-Z	High-Z	Active*
1	0	Normal Operation	All Active	High-Z	High-Z
1	1	Normal Operation	All Active	Active	Active

**Active = active with reduced performance*

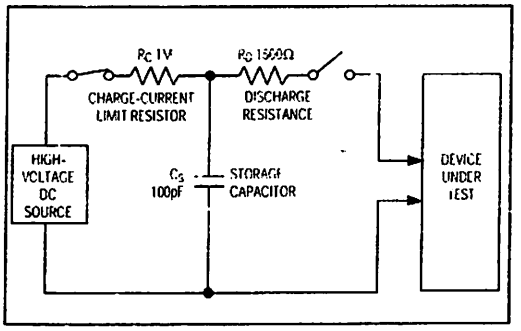


Figure 6a. Human Body ESD Test Model

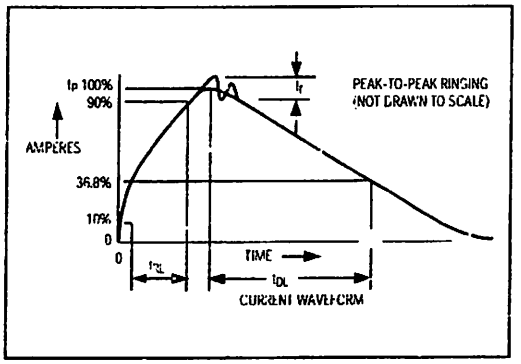


Figure 6b. Human Body Model Current Waveform

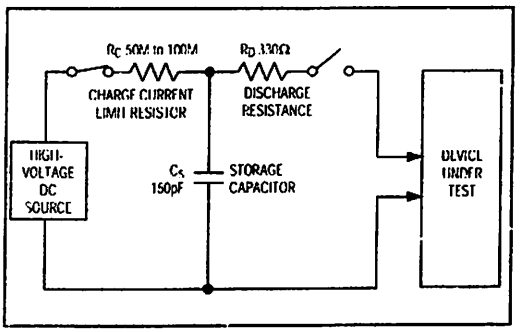


Figure 7a. IEC1000-4-2 ESD Test Model

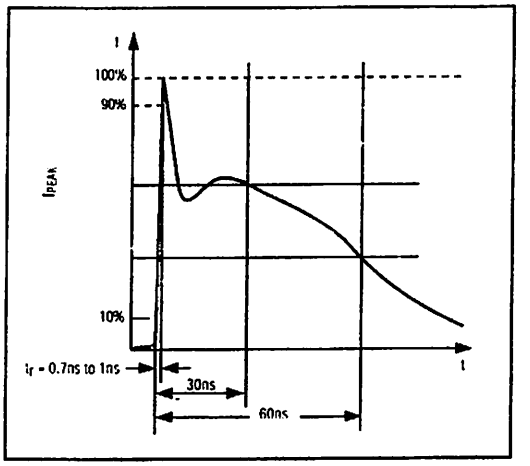


Figure 7b. IEC1000-4-2 ESD Generator Current Waveform

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX202E/MAX203E–MAX213E, MAX232E/MAX241E help you design equipment that meets level 4 (the highest level) of IEC1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2, because series resistance is lower in the IEC1000 4 2 model. Hence, the ESD withstand voltage measured to IEC1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7b shows the current waveform for the 8kV IEC1000-4-2 level-four ESD contact-discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just RS 232 inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The MAX202E, MAX206–MAX208E, MAX211E, and MAX213E require 0.1µF capacitors, and the MAX232E and MAX241E require 1µF capacitors, although in all cases capacitors up to 10µF can be used without harm. Ceramic, aluminum-electrolytic, or tantalum capacitors are suggested for the 1µF capacitors, and ceramic dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2x) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Use larger capacitors (up to 10µF) to reduce the output impedance at V+ and V-. This can be useful when "stealing" power from V+ or from V-. The MAX203E and MAX205E have internal charge-pump capacitors.

Bypass V_{CC} to ground with at least 0.1µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce both driver output swing and noise margins. Increasing the value of the charge-pump capacitors (up to 10µF) helps maintain performance when power is drawn from V+ or V-.

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple receivers.

Driver Outputs when Exiting Shutdown

The driver outputs display no ringing or undesirable transients as they come out of shutdown.

High Data Rates

These transceivers maintain the RS-232 ±5.0V minimum driver output voltages at data rates of over 120kbps. For data rates above 120kbps, refer to the Transmitter Output Voltage vs. Load Capacitance graphs in the *Typical Operating Characteristics*. Communication at these high rates is easier if the capacitive loads on the transmitters are small; i.e., short cables are best.

Table 2. Summary of EIA/TIA-232E, V.28 Specifications

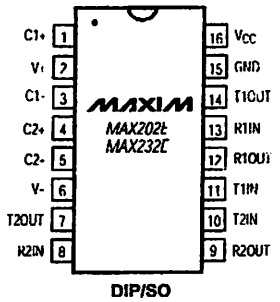
PARAMETER		CONDITIONS	EIA/TIA-232E, V.28 SPECIFICATIONS
Driver Output Voltage	0 Level	3kΩ to 7kΩ load	+5V to +15V
	1 Level	3kΩ to 7kΩ load	-5V to -15V
Driver Output Level, Max		No load	±25V
Data Rate		3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	Up to 20kbps
Receiver Input Voltage	0 Level		+3V to +15V
	1 Level		-3V to -15V
Receiver Input Level			±25V
Instantaneous Slew Rate, Max		3kΩ ≤ R_I ≤ 7kΩ, C_I ≤ 2500pF	30V/µs
Driver Output Short-Circuit Current, Max			100mA
Transition Rate on Driver Output		V.28	1ms or 3% of the period
		EIA/TIA-232E	4% of the period
Driver Output Resistance		-2V < V_{OUT} < +2V	300Ω

Table 3. DB9 Cable Connections Commonly Used for EIA/TIAE-232E and V.24 Asynchronous Interfaces

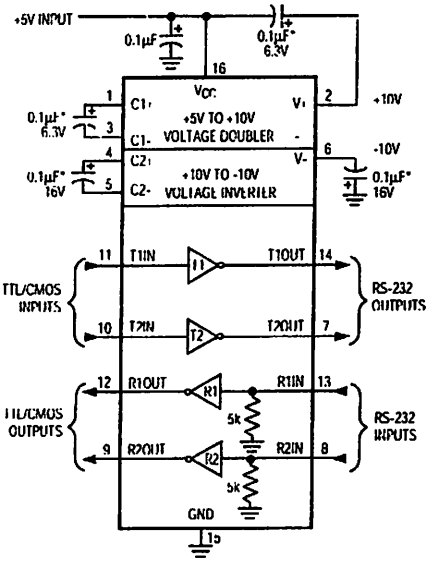
PIN	CONNECTION	
1	Received Line Signal Detector (sometimes called Carrier Detect, DCD)	Handshake from DCE
2	Receive Data (RD)	Data from DCE
3	Transmit Data (TD)	Data from DTE
4	Data Terminal Ready	Handshake from DTE
5	Signal Ground	Reference point for signals
6	Data Set Ready (DSR)	Handshake from DCE
7	Request to Send (RTS)	Handshake from DTE
8	Clear to Send (CTS)	Handshake from DCE
9	Ring Indicator	Handshake from DCE

Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



DIP/SO



PIN NUMBERS ON TYPICAL OPERATING CIRCUIT REFER TO DIP/SO PACKAGE, NOT LCC.
* 1.0µF CAPACITORS, MAX232E ONLY.

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX202ECPE	0°C to +70°C	16 Plastic DIP
MAX202ECSE	0°C to +70°C	16 Narrow SO
MAX202ECWE	0°C to +70°C	16 Wide SO
MAX202EC/D	0°C to +70°C	Dice*
MAX202EEPE	-40°C to +85°C	16 Plastic DIP
MAX202EESE	-40°C to +85°C	16 Narrow SO
MAX202EEWE	-40°C to +85°C	16 Wide SO
MAX203ECPP	0°C to +70°C	20 Plastic DIP
MAX203ECWP	0°C to +70°C	20 SO
MAX203EEPP	-40°C to +85°C	20 Plastic DIP
MAX203EEWP	-40°C to +85°C	20 SO
MAX205ECPG	0°C to +70°C	24 Wide Plastic DIP
MAX205EEPG	-40°C to +85°C	24 Wide Plastic DIP
MAX206ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX206ECWG	0°C to +70°C	24 SO
MAX206ECAG	0°C to +70°C	24 SSOP
MAX206EFNG	-40°C to +85°C	24 Narrow Plastic DIP
MAX206EFWG	-40°C to +85°C	24 SO
MAX206EEAG	-40°C to +85°C	24 SSOP
MAX207ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX207ECWG	0°C to +70°C	24 SO
MAX207ECAG	0°C to +70°C	24 SSOP
MAX207EENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX207EEWG	-40°C to +85°C	24 SO
MAX207EEAG	-40°C to +85°C	24 SSOP

PART	TEMP. RANGE	PIN-PACKAGE
MAX208ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX208ECWG	0°C to +70°C	24 SO
MAX208ECAG	0°C to +70°C	24 SSOP
MAX208EFNG	-40°C to +85°C	24 Narrow Plastic DIP
MAX208EEWG	-40°C to +85°C	24 SO
MAX208EEAG	-40°C to +85°C	24 SSOP
MAX211ECWI	0°C to +70°C	28 SO
MAX211ECAI	0°C to +70°C	28 SSOP
MAX211EEWI	-40°C to +85°C	28 SO
MAX211EEAI	-40°C to +85°C	28 SSOP
MAX213ECWI	0°C to +70°C	28 SO
MAX213ECAI	0°C to +70°C	28 SSOP
MAX213EEWI	-40°C to +85°C	28 SO
MAX213EEAI	-40°C to +85°C	28 SSOP
MAX232ECPE	0°C to +70°C	16 Plastic DIP
MAX232ECSE	0°C to +70°C	16 Narrow SO
MAX232ECWE	0°C to +70°C	16 Wide SO
MAX232EC/D	0°C to +70°C	Dice*
MAX232EFPE	-40°C to +85°C	16 Plastic DIP
MAX232EESE	-40°C to +85°C	16 Narrow SO
MAX232EEWE	-40°C to +85°C	16 Wide SO
MAX241ECWI	0°C to +70°C	28 SO
MAX241ECAI	0°C to +70°C	28 SSOP
MAX241EEWI	-40°C to +85°C	28 SO
MAX241EEAI	-40°C to +85°C	28 SSOP

*Dice are specified at T_A = +25°C.

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.
The data flash ROM (2 KB X 2 blocks) is embedded.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Outline

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Shortest instruction execution time	50 ns (f(XIN) = 20 MHz, Vcc = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, Vcc = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2.
Peripheral function	Interrupt	Internal: 11 factors, External: 5 factors, Software: 4 factors, Priority level: 7 levels
	Watchdog timer	15 bits x 1 (with prescaler) Reset start function selectable
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel Circuits of input capture and output compare.
	Serial interface	•1 channel Clock synchronous, UART •1 channel UART
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •On-chip oscillator (high-speed, low-speed) On high-speed on-chip oscillator the frequency adjustment function is usable.
	Oscillation stop detection function	Stop detection of main clock oscillation
	Voltage detection circuit	Included
	Power on reset circuit	Included
	Port	Input/Output: 22 (including LED drive port), Input: 2 (LED drive I/O port: 8)
Electrical characteristics	Power supply voltage	Vcc = 3.0 to 5.5V (f(XIN) = 20MHz) Vcc = 2.7 to 5.5V (f(XIN) = 10MHz)
	Power consumption	Typ.9 mA (Vcc = 5.0V, (f(XIN) = 20MHz,High-speed mode) Typ.5 mA (Vcc = 3.0V, (f(XIN) = 10MHz,High-speed mode) Typ.35 µA (Vcc = 3.0V, Wait mode, Peripheral clock stops) Typ.0.7 µA (Vcc = 3.0V, Stop mode)
Flash memory	Program/erase voltage	Vcc = 2.7 to 5.5 V
	Number of program/erase	10,000 times (Data area)
		1,000 times (Program area)
Operating ambient temperature		-20 to 85°C -40 to 85°C (D-version)
Package		32-pin plastic mold LQFP

1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

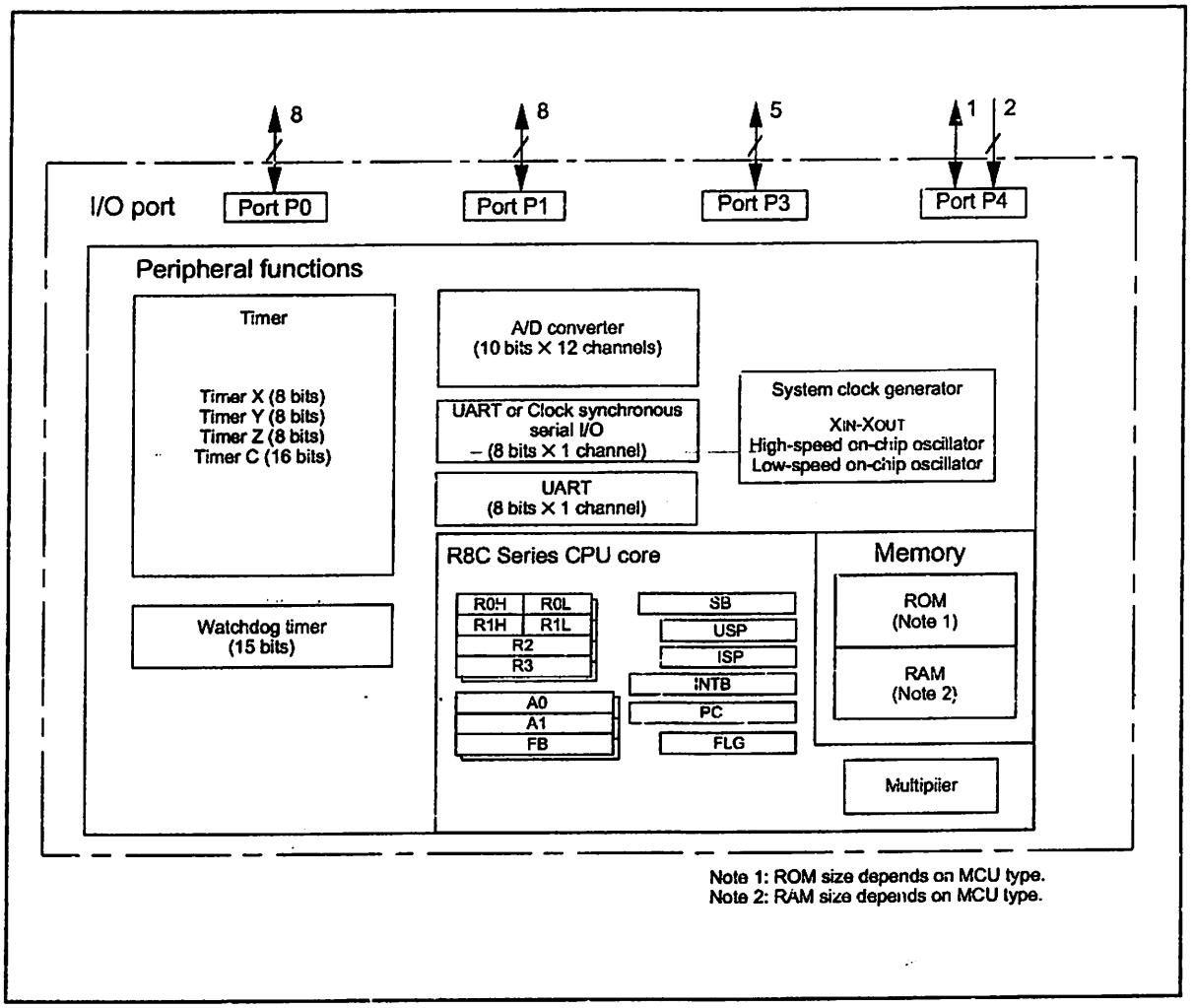


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.2 lists the products.

Table 1.2 Product List

As of April 2005

Type No.	ROM capacity		RAM capacity	Package type	Remarks
	Program area	Data area			
R5F21132FP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	Flash memory version
R5F21133FP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134FP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	
R5F21132DFP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	D version
R5F21133DFP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134DFP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	

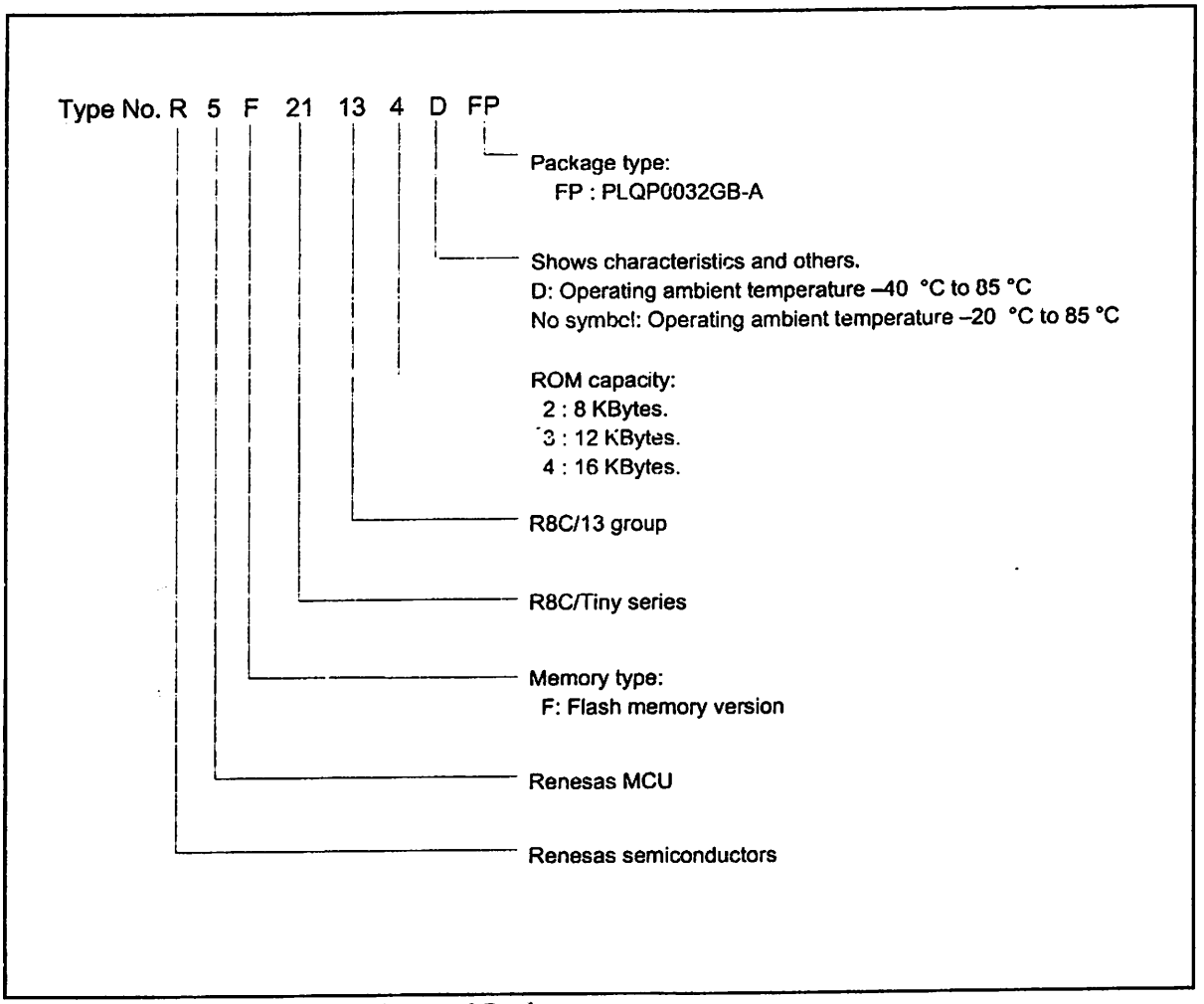


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Assignments

Figure 1.3 shows the pin configuration (top view).

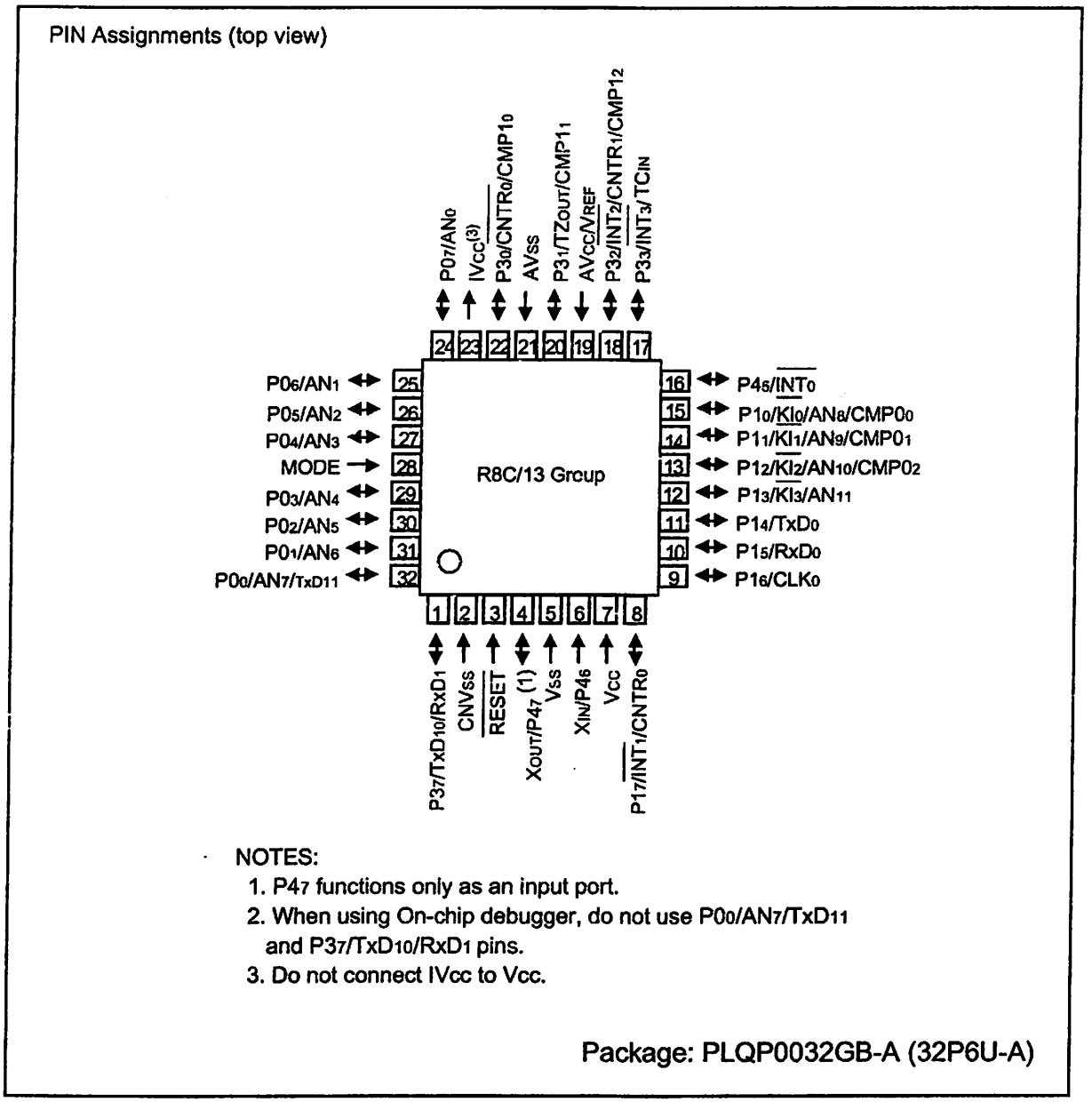


Figure 1.3 Pin Assignments (Top View)

1.6 Pin Description

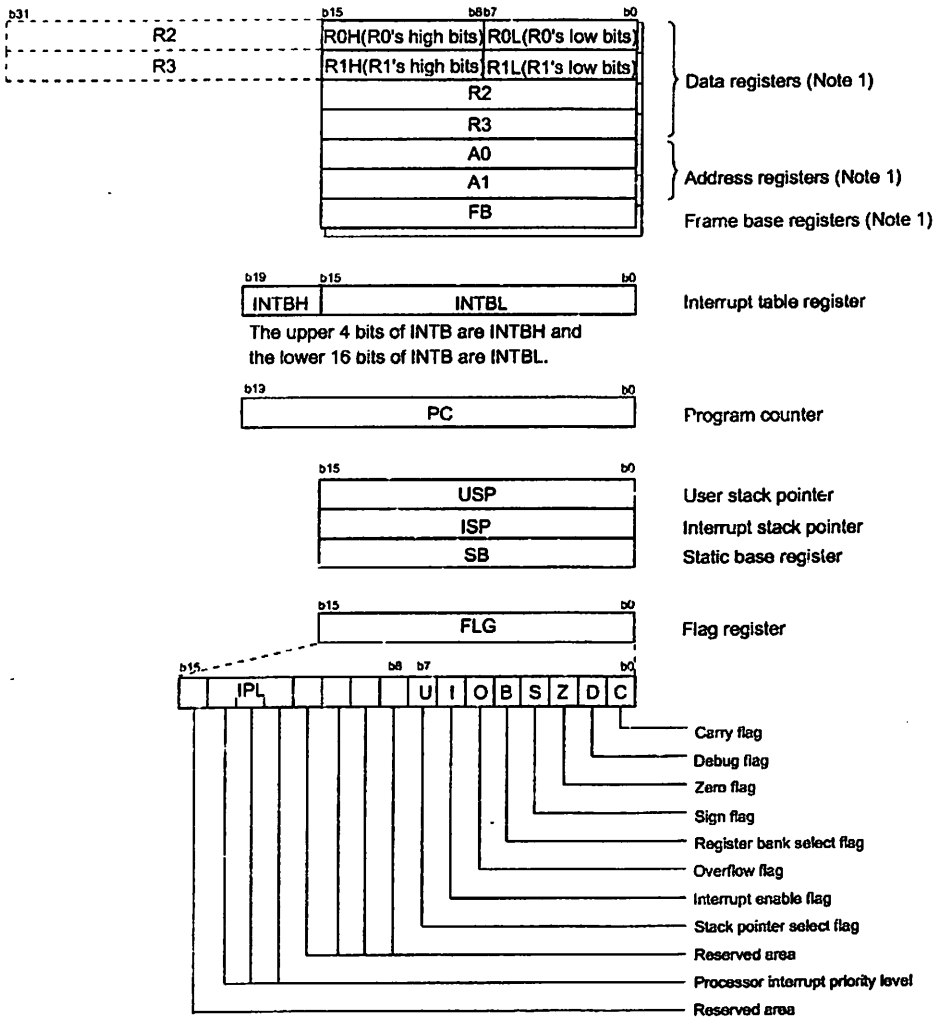
Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply Connect this pin to Vss via a capacitor (0.1 μF) Do not connect to Vcc
Analog power supply input	AVcc, AVss	I	These are power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	$\overline{\text{RESET}}$	I	"L" on this input resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor(1)
MODE	MODE	I	Connect this pin to Vcc via a resistor
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	These are $\overline{\text{INT}}$ interrupt input pins.
Key input interrupt input	KI0 to KI3	I	These are key input interrupt pins.
Timer X	CNTR0	I/O	This is the timer X I/O pin.
	$\overline{\text{CNTR0}}$	O	This is the timer X output pin.
Timer Y	CNTR1	I/O	This is the timer Y I/O pin.
Timer Z	TZOUT	O	This is the timer Z output pin.
Timer C	TCIN	I	This is the timer C input pin.
	CMP00 to CMP03, CMP10 to CMP13	O	These are the timer C output pins.
Serial interface	CLK0	I/O	This is a transfer clock I/O pin.
	RxD0, RxD1	I	These are serial data input pins.
	TxD0, TxD10, TxD11	O	These are serial data output pins.
Reference voltage input	VREF	I	This is a reference voltage input pin for A/D converter. Connect the VREF pin to Vcc.
A/D converter	AN0 to AN11	I	These are analog input pins for A/D converter.
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	I/O	These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	I	These are input only pins.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.



Note 1: These registers comprise a register bank. There are two register banks.

Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0" ; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of this MCU. The address space extends the 1M bytes from address 0000016 to FFFFF16.

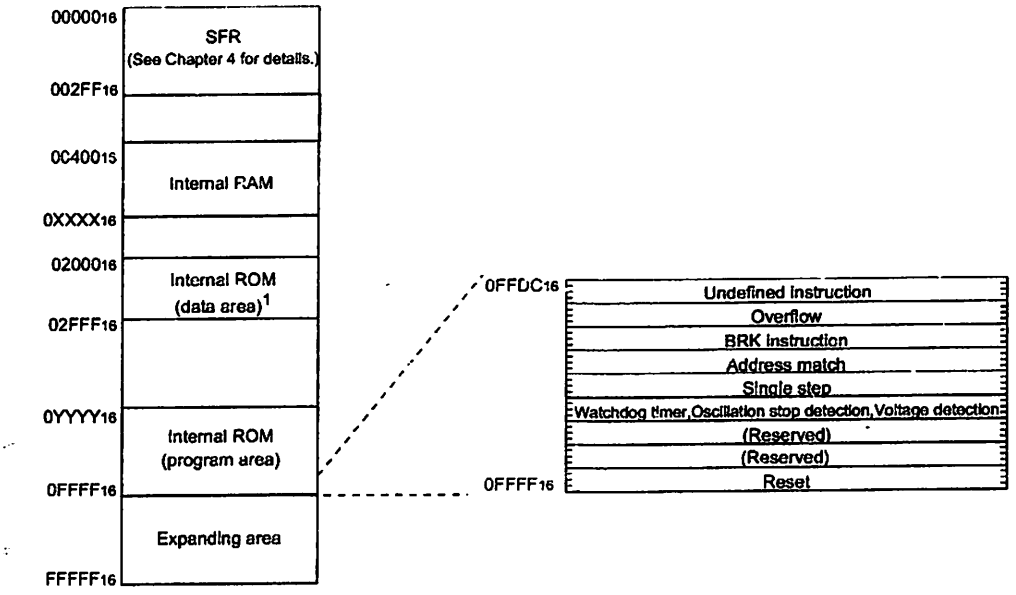
The internal ROM (program area) is allocated in a lower address direction beginning with address 0FFFF16. For example, a 16-Kbyte internal ROM is allocated to the addresses from 0C00016 to 0FFFF16.

The fixed interrupt vector table is allocated to the addresses from 0FFDC16 to 0FFFF16. Therefore, store the start address of each interrupt routine here.

The internal ROM (data area) is allocated to the addresses from 0200016 to 02FFF16.

The internal RAM is allocated in an upper address direction beginning with address 0040016. For example, a 1-Kbyte internal RAM is allocated to the addresses from 0040016 to 007FF16. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

Special function registers (SFR) are allocated to the addresses from 0000016 to 002FF16. Peripheral function control registers are located here. Of the SFR, any space which has no functions allocated is reserved for future use and cannot be used by users.



NOTES:
1. The data flash ROM block A (2K bytes) and block B (2K bytes) are shown.
2. Blank spaces are reserved. No access is allowed.

Type name	Internal ROM		Internal RAM	
	Size	Address 0YYYY16	Size	Address 0XXXX16
R5F21134FP, R5F21134DFP	16K bytes	0C00016	1K bytes	007FF16
R5F21133FP, R5F21133DFP	12K bytes	0D00016	768 bytes	006FF16
R5F21132FP, R5F21132DFP	8K bytes	0E00016	512 bytes	005FF16

Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)[1]

Address	Register	Symbol	After reset
000016			
000116			
000216			
000316			
000416	Processor mode register 0 [1]	PM0	0016
000516	Processor mode register 1	PM1	0016
000616	System clock control register 0	CM0	011010002
000716	System clock control register 1	CM1	001000002
000816	High-speed on-chip oscillator control register 0	HR0	0016
000916	Address match interrupt enable register	AIER	XXXXXX002
000A16	Protect register	PRCR	00XXX0002
000B16	High-speed on-chip oscillator control register 1	HR1	4016
000C16	Oscillation stop detection register	OCD	000001002
000D16	Watchdog timer reset register	WDTR	XX16
000E16	Watchdog timer start register	WDTS	XX16
000F16	Watchdog timer control register	WDC	000111112
001016 001116 001216	Address match interrupt register 0	RMAD0	0016 0016 X016
001316			
001416 001516 001616	Address match interrupt register 1	RMAD1	0016 0016 X016
001716			
001816			
001916	Voltage detection register 1 [2]	VCR1	000010002
001A16	Voltage detection register 2 [2]	VCR2	0016 [3] 100000002 [4]
001B16			
001C16			
001D16			
001E16	INT0 input filter select register	INT0F	XXXXX0002
001F16	Voltage detection interrupt register [2]	D4INT	0016 [3] 010000012 [4]
002016			
002116			
002216			
002316			
002416			
002516			
002616			
002716			
002816			
002916			
002A16			
002B16			
002C16			
002D16			
002E16			
002F16			
003016			
003116			
003216			
003316			
003416			
003516			
003616			
003716			
003816			
003916			
003A16			
003B16			
003C16			
003D16			
003E16			
003F16			

X : Undefined

NOTES:

1. Blank columns are all reserved space. No access is allowed.
2. Software reset or the watchdog timer reset does not affect this register.
3. Owing to Reset Input.
4. In the case of RESET pin = H retaining.

Table 4.2 SFR Information(2)[1]

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆			
0049₁₆			
004A₁₆			
004B₁₆			
004C₁₆			
004D₁₆	Key input interrupt control register	KUPIC	XXXXX0002
004E₁₆	AD conversion interrupt control register	ADIC	XXXXX0002
004F₁₆			
0050₁₆	Compare 1 interrupt control register	CMP1IC	XXXXX0002
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055₁₆	INT2 interrupt control register	INT2IC	XXXXX0002
0056₁₆	Timer X interrupt control register	TXIC	XXXXX0002
0057₁₆	Timer Y interrupt control register	TYIC	XXXXX0002
0058₁₆	Timer Z interrupt control register	TZIC	XXXXX0002
0059₁₆	INT1 interrupt control register	INT1IC	XXXXX0002
005A₁₆	INT3 interrupt control register	INT3IC	XXXXX0002
005B₁₆	Timer C interrupt control register	TCIC	XXXXX0002
003C₁₆	Compare 0 interrupt control register	CMP0IC	XXXXX0002
005D₁₆	INT0 interrupt control register	INT0IC	XX00X0002
005E₁₆			
005F₁₆			
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

X : Undefined

NOTES:

1. Blank columns are all reserved space. No access is allowed.

Table 4.3 SFR Information(3)[1]

Address	Register	Symbol	After reset
0080₁₆	Timer Y, Z mode register	TYZMR	00₁₆
0081₁₆	Prescaler Y	PREY	FF₁₆
0082₁₆	Timer Y secondary	TYSC	FF₁₆
0083₁₆	Timer Y primary	TYPR	FF₁₆
0084₁₆	Timer Y, Z waveform output control register	PUM	00₁₆
0085₁₆	Prescaler Z	PREZ	FF₁₆
0086₁₆	Timer Z secondary	TZSC	FF₁₆
0087₁₆	Timer Z primary	TZPR	FF₁₆
0088₁₆			
0089₁₆			
008A₁₆	Timer Y, Z output control register	TYZOC	00₁₆
008B₁₆	Timer X mode register	TXMR	00₁₆
008C₁₆	Prescaler X	PREX	FF₁₆
008D₁₆	Timer X register	TX	FF₁₆
008E₁₆	Count source set register	TCSS	00₁₆
008F₁₆			
0090₁₆	Timer C register	TC	00₁₆
0091₁₆			00₁₆
0092₁₆			
0093₁₆			
0094₁₆			
0095₁₆			
0096₁₆	External input enable register	INTEN	00₁₆
0097₁₆			
0098₁₆	Key input enable register	KIEN	00₁₆
0099₁₆			
009A₁₆	Timer C control register 0	TCC0	00₁₆
009B₁₆	Timer C control register 1	TCC1	00₁₆
009C₁₆	Capture, compare 0 register	TM0	00₁₆
009D₁₆			00₁₆2
009F₁₆	Compare 1 register	TM1	FF₁₆
009F₁₆			FF₁₆
00A0₁₆	UART0 transmit/receive mode register	U0MR	00₁₆
00A1₁₆	UART0 bit rate register	U0BRG	XX₁₆
00A2₁₆	UART0 transmit buffer register	U0TB	XX₁₆
00A3₁₆			XX₁₆
00A4₁₆	UART0 transmit/receive control register 0	U0C0	000010002
00A5₁₆	UART0 transmit/receive control register 1	U0C1	000000102
00A6₁₆	UART0 receive buffer register	U0RB	XX₁₆
00A7₁₆			XX₁₆
00A8₁₆	UART1 transmit/receive mode register	U1MR	00₁₆
00A9₁₆	UART1 bit rate register	U1BRG	XX₁₆
00AA₁₆	UART1 transmit buffer register	U1TB	XX₁₆
00AB₁₆			XX₁₆
00AC₁₆	UART1 transmit/receive control register 0	U1C0	000010002
00AD₁₆	UART1 transmit/receive control register 1	U1C1	000000102
00AE₁₆	UART1 receive buffer register	U1RB	XX₁₆
00AF₁₆			XX₁₆
00B0₁₆	UART transmit/receive control register 2	UCON	00₁₆
00B1₁₆			
00B2₁₆			
00B3₁₆			
00B4₁₆			
00B5₁₆			
00B6₁₆			
00B7₁₆			
00B8₁₆			
00B9₁₆			
00BA₁₆			
00BB₁₆			
00BC₁₆			
00BD₁₆			
00BE₁₆			
00BF₁₆			

X : Undefined

NOTES:

1. Blank columns are all reserved space. No access is allowed.
2. When the output compare mode is selected (the TCC13 bit in the TCC1 register = 1), the value is set to FFFF16.

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After reset
00C016	AD register	AD	XX16
00C116			XX16
00C216			
00C316			
00C416			
00C516			
00C616			
00C716			
00C816			
00C916			
00CA16			
00CB16			
00CC16			
00CD16			
00CE16			
00CF16			
00D016			
00D116			
00D216			
00D316			
00D416	AD control register 2	ADCON2	0016
00D516			
00D616	AD control register 0	ADCON0	00000XXX2
00D716	AD control register 1	ADCON1	0016
00D816			
00D916			
00DA16			
00DB16			
00DC16			
00DD16			
00DE16			
00DF16			
00E016	Port P0 register	P0	XX16
00E116	Port P1 register	P1	XX16
00E216	Port P0 direction register	PD0	0016
00E316	Port P1 direction register	PD1	0016
00E416			
00E516	Port P3 register	P3	XX16
00E616			
00E716	Port P3 direction register	PD3	0016
00E816	Port P4 register	P4	XX16
00E916			
00EA16	Port P4 direction register	PD4	0016
00EB16			
00EC16			
00ED16			
00EE16			
00EF16			
00F016			
00F116			
00F216			
00F316			
00F416			
00F516			
00F616			
00F716			
00F816			
00F916			
03FA16			
00FB16			
00FC16	Pull-up control register 0	PUR0	00XX00002
00FD16	Pull-up control register 1	PUR1	XXXXXX0X2
00FE16	Port P1 drive capacity control register	DRR	0016
00FF16	Timer C output control register	TCOUT	0016
≈			≈
01B316	Flash memory control register 4	FMR4	010000002
01B416			
01B516	Flash memory control register 1	FMR1	1000000X2
01B616			
01B716	Flash memory control register 0	FMR0	000000012
0FFFF16	Option function select register (2)	OFS	Note 2

X : Undefined

NOTES:

1. The blank areas, 010016 to 01B216 and 01B816 to 02FF16 are reserved and cannot be used by users.
2. The watchdog timer control bit is assigned. Refer to "Figure11.2 OFS, WDC, WDTR and WDTS registers" of Hardware Manual for details

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
Vcc	Supply voltage	Vcc=AVcc	-0.3 to 6.5	V
AVcc	Analog supply voltage	Vcc=AVcc	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to Vcc+0.3	V
Vo	Output voltage		-0.3 to Vcc+0.3	V
Pd	Power dissipation	Topr=25 °C	300	mW
T_{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard Min.	Standard Typ.	Standard Max.	Unit
Vcc	Supply voltage			2.7		5.5	V
AVcc	Analog supply voltage				Vcc[3]		V
Vss	Supply voltage				0	—	V
AVss	Analog supply voltage				0		V
V_{IH}	"H" input voltage			0.8Vcc		Vcc	V
V_{IL}	"L" input voltage			0		0.2Vcc	V
$I_{OH\ (sum)}$	"H" peak all output currents	Sum of all pins' IOH (peak)				-60.0	mA
$I_{OH\ (peak)}$	"H" peak output current					-10.0	mA
$I_{OH\ (avg)}$	"H" average output current					-5.0	mA
$I_{OL\ (sum)}$	"L" peak all output currents	Sum of all pins' IOL (peak)				60	mA
$I_{OL\ (peak)}$	"L" peak output current	Except P10 to P17				10	mA
		P10 to P17	Drive ability HIGH			30	mA
			Drive ability LOW			10	mA
$I_{OL\ (avg)}$	"L" average output current	Except P10 to P17				5	mA
		P10 to P17	Drive ability HIGH			15	mA
			Drive ability LOW			5	mA
f(XIN)	Main clock input oscillation frequency		3.0V ≤ Vcc ≤ 5.5V	0		20	MHz
			2.7V ≤ Vcc < 3.0V	0		10	MHz

Note
1: Referenced to Vcc = AVcc = 2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2: The mean output current is the mean value within 100ms.
3: Set Vcc=AVcc

Table 5.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} =Vcc			10	Bit
–	Absolute accuracy	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V			±3	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V			±2	LSB
		10 bit mode	øAD=10 MHz, Vref=Vcc=3.3V[3]			±5	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=3.3V[3]			±2	LSB
R_{LADDER}	Ladder resistance		V_{REF}=Vcc	10		40	kΩ
t_{CONV}	Conversion time	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	3.3			µs
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	2.8			µs
V_{REF}	Reference voltage				Vcc[4]		V
V_{IA}	Analog input voltage			0		V_{ref}	V
–	A/D operation clock frequency[2]	Without sample & hold		0.25		10	MHz
		With sample & hold		1.0		10	MHz

Note
1: Referenced to Vcc=AVcc=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2: When f_{AD} is 10 MHz more, divide the f_{AD} and make A/D operation clock frequency ($Ø_{AD}$) lower than 10 MHz.
3: When the AVcc is less than 4.2V, divide the f_{AD} and make A/D operation clock frequency ($Ø_{AD}$) lower than $f_{AD}/2$.
4: Set Vcc=Vref

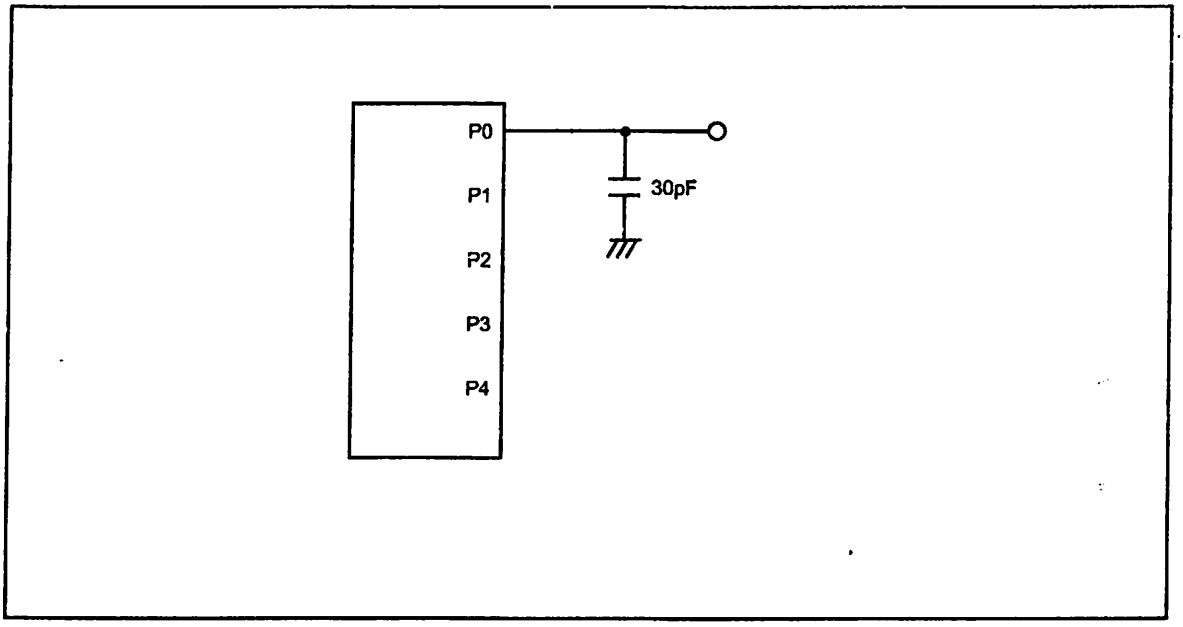


Figure 5.1 Port P0 to P4 measurement circuit

Table 5.4 Flash Memory (Program area) Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase cycle [2]		1000[3]	—	—	cycle
–	Byte program time	Vcc = 5.0 V at Topr = 25 °C	—	50	—	µs
–	Block erase time	Vcc = 5.0 V at Topr = 25 °C	—	0.4	—	s
td(SR-ES)	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
–	Erase Suspend Request Interval		10	—	—	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program, Erase Temperature		0	—	60	°C
–	Data-retention duration	Topr = 55 °C	20	—	—	year

Table 5.5 Flash Memory (Data area Block A, Block B) Electrical Characteristics [4]

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase endurance[2]		10000 [3]	—	—	times
–	Byte program time(program/erase endurance ≤1000 times)	Vcc = 5.0 V at Topr = 25 °C	—	50	400	µs
–	Byte program time(program/erase endurance >1000 times)	Vcc = 5.0 V at Topr = 25 °C	—	65	—	µs
–	Block erase time(program/erase endurance ≤1000 times)	Vcc = 5.0 V at Topr = 25 °C	—	0.2	9	s
–	Block erase time(program/erase endurance >1000 times)	Vcc = 5.0 V at Topr = 25 °C	—	0.3	—	s
td(SR-ES)	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
–	Erase Suspend Request Interval		10	—	—	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program/Erase Temperature		-20(-40)[8]	—	85	°C
–	Data-retention duration	Topr = 55 °C	20	—	—	year

Note
1: Referenced to Vcc=AVcc=2.7 to 5.5V at Topr = 0°C to 60°C unless otherwise specified.
2: Definition of Program/Erase
The cycle of Program/Erase shows a cycle for each block.
If the program/erase number is "n" (n = 1000, 10000), "n" times erase can be performed for each block.
For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.
However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).
3: Maximum numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.
4: Table 16.5 applies for Block A or B when the Program/Erase cycles are more than 1000. The byte program time up to 1000 cycles are the same as that of the program area (see Table 5.4).
5: To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.
6: If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.
7: Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
8: -40 °C for D version.

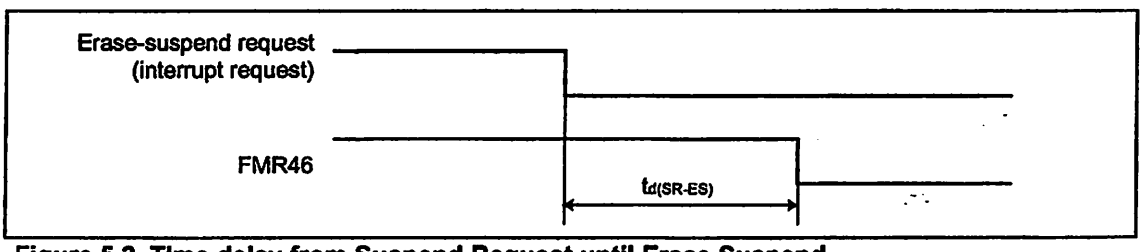


Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet	Voltage detection level		3.3	3.8	4.3	V
	Voltage detection interrupt request generating time[2]			40		µs
	Voltage detection circuit self consumption current	VC27=1, VCC=5.0V		600		nA
td(E-A)	Waiting time until voltage detection circuit operation starts[3]				20	µs
Vccmin	Microcomputer operation voltage minimum value		2.7			V

NOTES:
1. The measuring condition is Vcc=AVcc=2.7V to 5.5V and Topr=-40°C to 85°C.
2. This shows the time until the voltage detection interrupt request is generated since the voltage passes Vdet.
3. This shows the required time until the voltage detection circuit operates when setting to "1" again after setting the VC27 bit in the VCR2 register to "0".

Table 5.7 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2[1, 3])

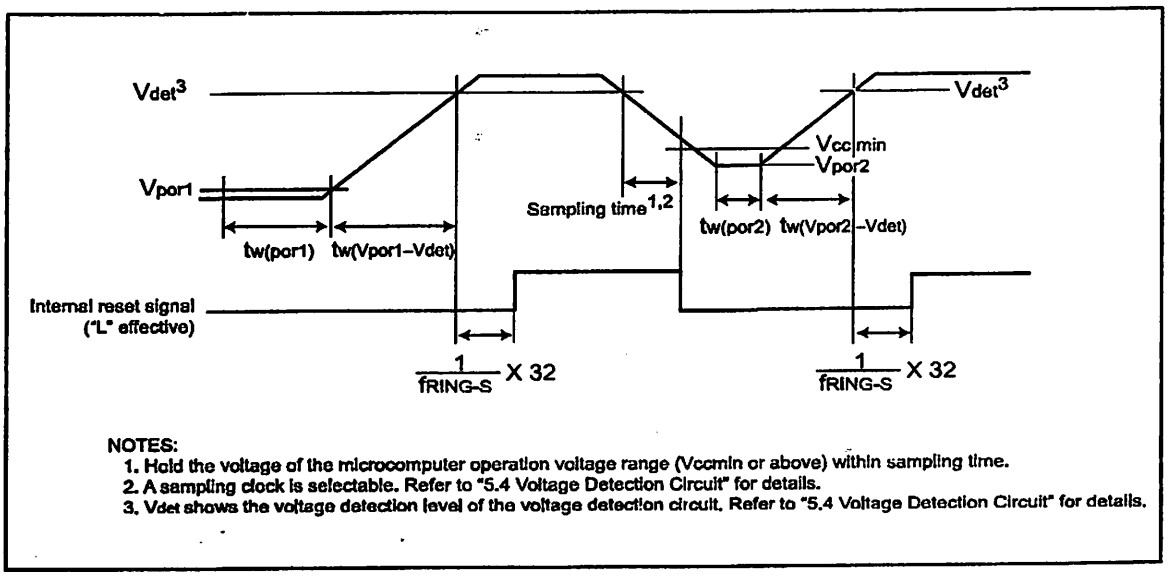
Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor2	Power-on reset valid voltage	-20°C ≤ Topr < 85°C			Vdet	V
tw(Vpor2-Vdet)	Supply voltage rising time when power-on reset is canceled[2]	-20°C ≤ Topr < 85°C, tw(por2) ≥ 0s[4]	—	—	100	ms

NOTES:
1. The voltage detection circuit which is embedded in a microcomputer is a factor to generate the hardware reset 2. Refer to 5.1.2 Hardware Reset 2.
2. This condition is not applicable when using Vcc ≥ 1.0V.
3. When turning power on after the external power has been held below the valid voltage for greater than 10 seconds, refer to Table 16.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2).
4. tw(por2) is time to hold the external power below effective voltage (Vpor2).

Table 5.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vpor1	Power-on reset valid voltage	-20°C ≤ Topr < 85°C			0.1	V
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 10s[2]	—	—	100	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	-20°C ≤ Topr < 0°C, tw(por1) ≥ 30s[2]			100	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	-20°C ≤ Topr < 0°C, tw(por1) ≥ 10s[2]	—	—	1	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C < Topr < 85°C, tw(por1) > 1s[2]	—	—	0.5	ms

NOTES:
1. When not using hardware reset 2, use with Vcc ≥ 2.7V.
2. tw(por1) is time to hold the external power below effective voltage (Vpor1).



NOTES:
1. Hold the voltage of the microcomputer operation voltage range (Vccmin or above) within sampling time.
2. A sampling clock is selectable. Refer to "5.4 Voltage Detection Circuit" for details.
3. Vdet shows the voltage detection level of the voltage detection circuit. Refer to "5.4 Voltage Detection Circuit" for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.9 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency 1 / {td(HRoffset)+td(HR)} when the reset is released	VCC=5.0V, Topr=25 °C Set "40$_{16}$" in the HR1 register		8	—	MHz
td(HRoffset)	Settable high-speed on-chip oscillator minimum period	VCC=5.0V, Topr=25 °C Set "00$_{16}$" in the HR1 register	—	61	—	ns
td(HR)	High-speed on-chip oscillator period adjusted unit	Differences when setting "01$_{16}$" and "00$_{16}$" in the HR register	—	1	—	ns
—	High-speed on-chip oscillator temperature dependence(1)	Frequency fluctuation in temperature range of -10 °C to 50 °C	—	±5	—	%
—	High-speed on-chip oscillator temperature dependence(2)	Frequency fluctuation in temperature range of -40 °C to 85 °C		±10	—	%

NOTES:
1. The measuring condition is Vcc=AVcc=5.0 V and Topr=25 °C.

Table 5.10 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on[2]		1		2000	µs
td(R-S)	STOP release time[3]				150	µs

Note
1: The measuring condition is Vcc=AVcc=2.7 to 5.5 V and Topr=25 °C.
2: This shows the wait time until the internal power supply generating circuit is stabilized during power-on.
3: This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

Table 5.11 Electrical Characteristics (1) [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-5mA		Vcc-2.0	—	Vcc	V
			I_{OH}=-200µA		Vcc-0.3	—	Vcc	V
		X_{OUT}	Drive capacity HIGH	I_{OH}=-1 mA	Vcc-2.0	—	Vcc	V
			Drive capacity LOW	I_{OH}=-500µA	Vcc-2.0	—	Vcc	V
V_{OL}	"L" output voltage	P10 to P17 Except X_{OUT}	I_{OL}= 5 mA		—	—	2.0	V
			I_{OL}= 200 µA		—	—	0.45	V
		P10 to P17	Drive capacity HIGH	I_{OL}= 15 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}= 5 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}= 200 µA	—	—	0.45	V
		X_{OUT}	Drive capacity HIGH	I_{OL}= 1 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}=500 µA	—	—	2.0	V
V_{T+}-V_{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, T_{CIN}, RxD0, RxD1, P45			0.2	—	1.0	V
		$\overline{RESET}$			0.2	—	2.2	V
I_{IH}	"H" input current		V_I=5V		—	—	5.0	µA
I_{IL}	"L" input current		V_I=0V		—	—	-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	X_{IN}			—	1.0	—	MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

Note
1 : Referenced to Vcc=AVcc=4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Table 5.12 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter	Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
Icc	Power supply current (Vcc=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are Vss	High-speed mode	Xin=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		9	15	mA
			Xin=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		8	14	mA
			Xin=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		5		mA
		Medium-speed mode	Xin=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		4		mA
			Xin=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		3		mA
			Xin=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		2		mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division		4	8	mA
			Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8		1.5		mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		470	900	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation VC27="0"		40	80	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off VC27="0"		38	76	µA
		Stop mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0"		0.8	3.0	µA

NOTES
1: The power supply current measuring is executed using the measuring program on frash memory.
2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: Vcc = 5V, Vss = 0V at Ta = 25 °C) [Vcc=5V]

Table 5.13 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(XIN)	XIN input cycle time	50		ns
twH(XIN)	XIN input HIGH pulse width	25		ns
twL(XIN)	XIN input LOW pulse width	25		ns

Table 5.14 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CNTR0)	CNTR0 input cycle time	100		ns
twH(CNTR0)	CNTR0 input HIGH pulse width	40		ns
twL(CNTR0)	CNTR0 input LOW pulse width	40		ns

Table 5.15 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TCIN)	TCIN input cycle time	400 [1]		ns
twH(TCIN)	TCIN input HIGH pulse width	200 [2]		ns
twL(TCIN)	TCIN input LOW pulse width	200 [2]		ns

NOTES
1 :When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).
2 : When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.16 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input HIGH pulse width	100		ns
tw(CKL)	CLKi input LOW pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	35		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.17 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INT0}$ input HIGH pulse width	250 [1]		ns
tw(INL)	$\overline{INT0}$ input LOW pulse width	250 [2]		ns

NOTES
1 : When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2 : When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

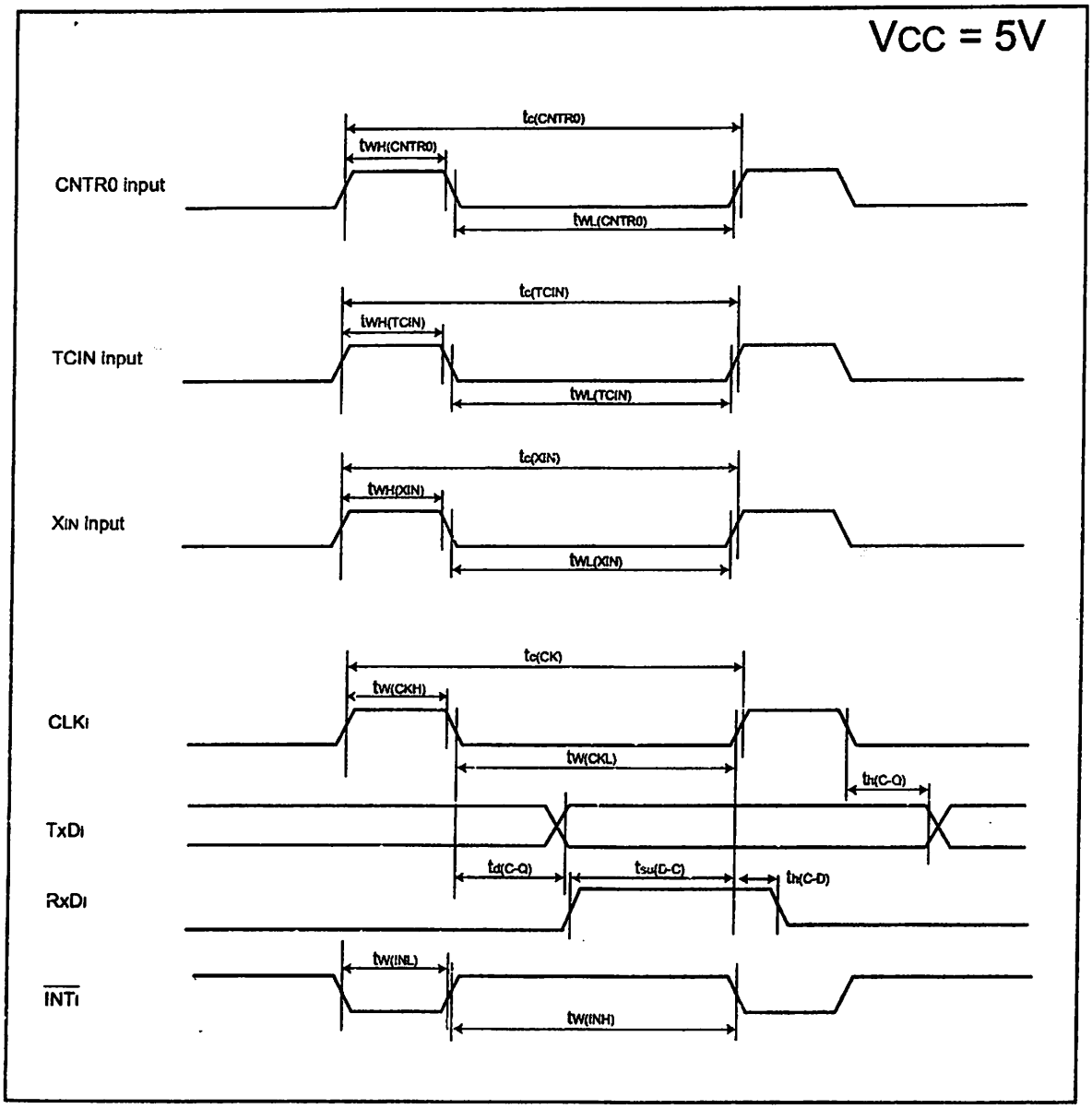


Figure 5.4 Vcc=5V timing diagram

Table 5.18 Electrical Characteristics (3) [Vcc=3V]

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-1mA		Vcc-0.5	—	Vcc	V
		X_{OUT}	Drive capacity HIGH	I_{OH}=-0.1 mA	Vcc-0.5	—	Vcc	V
			Drive capacity LOW	I_{OH}=-50 µA	Vcc-0.5		Vcc	V
V_{OL}	"L" output voltage	P10 to P17 Except X_{OUT}	I_{OL}= 1 mA		—		0.5	V
		P10 to P17	Drive capacity HIGH	I_{OL}= 2 mA	—	—	0.5	V
			Drive capacity LOW	I_{OL}= 1 mA	—	—	0.5	V
		X_{OUT}	Drive capacity HIGH	I_{OL}= 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I_{OL}=50 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	INTo, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, T_{CIN}, RxD0, RxD1, P45			0.2	—	0.8	V
		$\overline{RESET}$			0.2	—	1.8	V
I_{IH}	"H" input current		V_I=3V			—	4.0	µA
I_{IL}	"L" input current		V_I=0V		—	—	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V		66	160	500	kΩ
R_{XIN}	Feedback resistance	X_{IN}			—	3.0	—	MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

Note
1 : Referenced to Vcc=AVcc=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

Table 5.19 Electrical Characteristics (4) [Vcc=3V]

Symbol	Parameter	Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
Icc	Power supply current (Vcc=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are Vss	High-speed mode	Xin=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		8	13	mA
			Xin=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		7	12	mA
			Xin=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		5		mA
		Medium-speed mode	Xin=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		3		mA
			Xin=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		2.5		mA
			Xin=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		1.6		mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division	—	3.5	7.5	mA
			Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8		1.5		mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		420	800	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation VC27="0"		37	74	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off VC27="0"		35	70	µA
		Stop mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0"		0.7	3.0	µA

NOTES
1: The power supply current measuring is executed using the measuring program on flash memory.
2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: Vcc = 3V, Vss = 0V at Ta = 25 °C) [Vcc=3V]

Table 5.20 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	100		ns
tWH(XIN)	XIN input HIGH pulse width	40		ns
tWL(XIN)	XIN input LOW pulse width	40		ns

Table 5.21 CNTR0 input, CNTR1 input, INT2 input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	300		ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	120		ns
tWL(CNTR0)	CNTR0 input LOW pulse width	120		ns

Table 5.22 TCIN input, INT3 input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	1200 [1]		ns
tWH(TCIN)	TCIN input HIGH pulse width	600 [2]		ns
tWL(TCIN)	TCIN input LOW pulse width	600 [2]		ns

NOTES
1 :When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).
2 : When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.23 Serial Interface

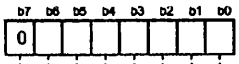
Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	300		ns
tW(CKH)	CLKi input HIGH pulse width	150		ns
tW(CKL)	CLKi input LOW pulse width	150		ns
td(C-Q)	TxDi output delay time		160	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	55		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.24 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	$\overline{INT0}$ input HIGH pulse width	380 [1]		ns
tW(INL)	$\overline{INT0}$ input LOW pulse width	380 [2]		ns

NOTES
1 : When selecting the digital filter by the INT0 input filter select bit, use the INT0 input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2 : When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

UARTi transmit/receive mode register (i=0, 1)

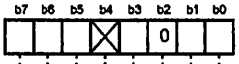


Symbol	Address	After reset
U0MR	00A0₁₆	00₁₆
U1MR	00A8₁₆	00₁₆

Bit symbol	Bit name	Function	RW
SMD0	Serial interface mode select bit[2]	b2 b1 b0 0 0 0 : Serial interface disabled 0 0 1 : Clock synchronous serial I/O mode 1 0 0 : UART mode transfer data 7 bits long 1 0 1 : UART mode transfer data 8 bits long 1 1 0 : UART mode transfer data 9 bits long Must not be set except above	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit[3]	0 : Internal clock 1 : External clock[1]	RW
STPS	Stop bit length select bit	0 : 1 stop bit 1 : 2 stop bits	RW
PRY	Odd/even parity select bit	Effective when PRYE = 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
——— (b7)	Reserved bit	Must set to "0"	RW

Notes:
1. Must set the P1_6 bit in the PD1 register to "0" (input).
2. For the U1MR register, the SMD2 to SMD0 bits must not be set except the followings: "000₂", "100₂", "101₂", or "110₂".
3. Must set the CKDIR bit to "0" (internal clock) in UART1.

UARTi transmit/receive control register 0 (i=0, 1)

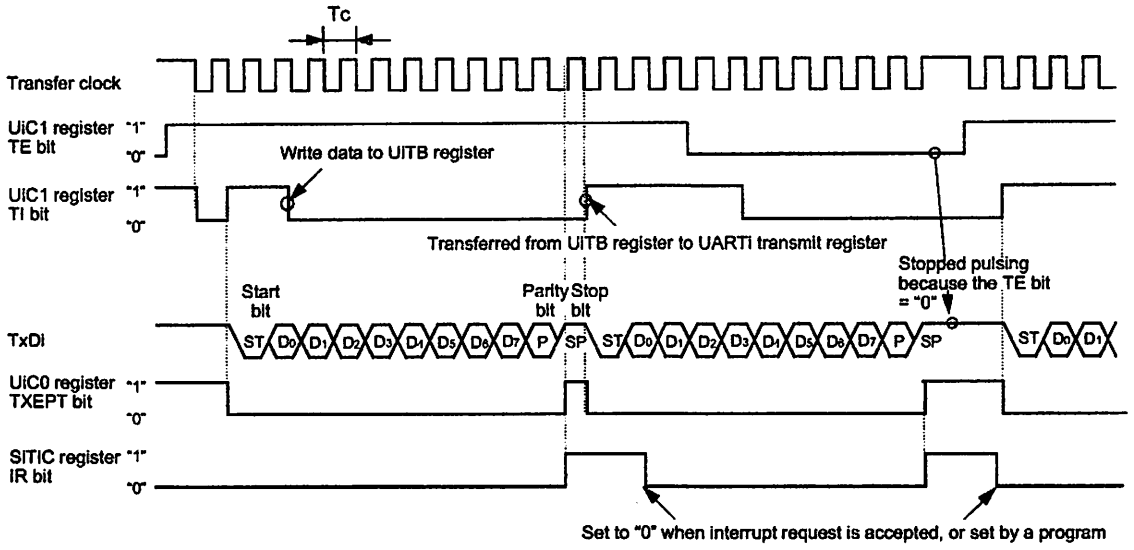


Symbol	Address	After reset
U0C0	00A4₁₆	08₁₆
U1C0	00AC₁₆	08₁₆

Bit symbol	Bit name	Function	RW
CLK0	BRG count source select bit	b1 b0 0 0 : f1SIO is selected 0 1 : fSIO is selected 1 0 : f2SIO is selected 1 1 : Avoid this setting	RW
CLK1			RW
——— (b2)	Reserved bit	Set to "0"	RW
TXEPT	Transmit register empty flag	0 : Data present in transmit register (during transmission) 1 : No data present in transmit register (transmission completed)	RO
——— (b4)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
NCH	Data output select bit	0 : TxDi pin is a pin of CMOS output 1 : TxDi pin is a pin of N-channel open-drain output	RW
CKPOL	CLK polarity select bit	0 : Transmit data is output at falling edge of transfer clock and receive data is input at rising edge 1 : Transmit data is output at rising edge of transfer clock and receive data is input at falling edge	RW
UFORM	Transfer format select bit	0 : LSB first 1 : MSB first	RW

gure 13.4 U0MR and U1MR Registers and U0C0 and U1C0 Registers

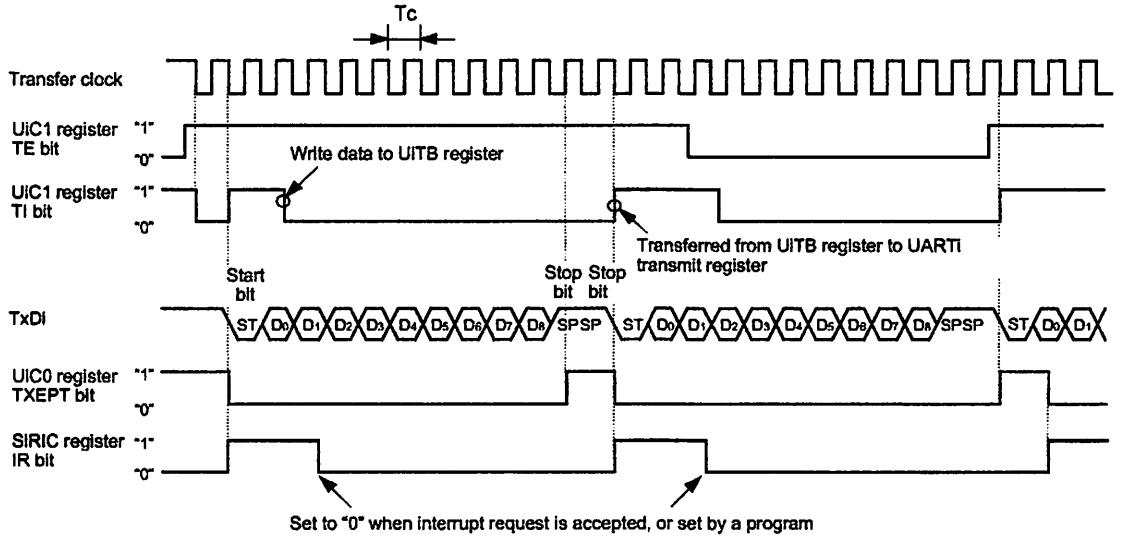
• Example of transmit timing when transfer data is 8 bits long (parity enabled, one stop bit)



The above timing diagram applies to the case where the register bits are set as follows:
- UiMR register PRYE bit = 1 (parity enabled)
- UiMR register STPS bit = 0 (1 stop bit)
- UiIRS bit = 1 (an interrupt request occurs when transmit completed):

$Tc = 16 (n + 1) / fj$ or $16 (n + 1) / f_{EXT}$
fj: frequency of UiBRG count source (f1SIO, f8SIO, f32SIO)
fEXT: frequency of UiBRG count source (external clock)
n: value set to UiBRG
i: 0, 1

• Example of transmit timing when transfer data is 9 bits long (parity disabled, two stop bits)



The above timing diagram applies to the case where the register bits are set as follows:
- UiMR register PRYE bit = 0 (parity disabled)
- UiMR register STPS bit = 1 (2 stop bits)
- UiIRS bit = 0 (an interrupt request occurs when transmit buffer becomes empty)

$Tc = 16 (n + 1) / fj$ or $16 (n + 1) / f_{EXT}$
fj: frequency of UiBRG count source (f1SIO, f8SIO, f32SIO)
fEXT: frequency of UiBRG count source (external clock)
n: value set to UiBRG
I: 0, 1

igure 13.9 Transmit Operation

13.2.3 Bit Rate

Divided-by-16 of frequency by the UiBRG (i=0 to 1) register in UART mode is a bit rate.

<UART Mode>

• When selecting internal clock

$$\text{Setting value to the UiBRG register} = \frac{fj}{\text{Bit Rate} \times 16} - 1$$

fj : Count source frequency of the UiBRG register (f1SIO, f8SIO and f32SIO)

• When selecting external clock

$$\text{Setting value to the UiBRG register} = \frac{fEXT}{\text{Bit Rate} \times 16} - 1$$

fEXT : Count source frequency of the UiBRG register (external clock)

igure 13.11 Calculation Formula of UiBRG (i=0 to 1) Register Setting Value

able 13.7 Bit Rate Setting Example in UART Mode

Bit Rate (bps)	BRG Count Source	System Clock = 20MHz			System Clock = 8MHz		
		BRG Setting Value	Actual Time(bps)	Error(%)	BRG Setting Value	Actual Time(bps)	Error(%)
1200	f8	129 (81_{16})	1201.92	0.16	51 (33_{16})	1201.92	0.16
2400	f8	64 (40_{16})	2403.85	0.16	25 (19_{16})	2403.85	0.16
4800	f8	32 (20_{16})	4734.85	–1.36	12 ($0C_{16}$)	4807.69	0.16
9600	f1	129 (81_{16})	9615.38	0.16	51 (33_{16})	9615.38	0.16
14400	f1	86 (56_{16})	14367.82	–0.22	34 (22_{16})	14285.71	–0.79
19200	f1	64 (40_{16})	19230.77	0.16	25 (19_{16})	19230.77	0.16
28800	f1	42 ($2A_{16}$)	29069.77	0.94	16 (10_{16})	29411.76	2.12
31250	f1	39 (27_{16})	31250.00	0.00	15 ($0F_{16}$)	31250.00	0.00
38400	f1	32 (20_{16})	37878.79	–1.36	12 ($0C_{16}$)	38461.54	0.16
51200	f1	23 (17_{16})	52083.33	1.73	9 (09_{16})	50000.00	–2.34

FT232BM is the 2nd generation of FTDI's popular USB UART i.c. This device not only adds extra functionality 's FT8U232AM predecessor and reduces external component count, but also maintains a high degree of pin npatibility with the original, making it easy to upgrade or cost reduce existing designs as well as increasing the ential for using the device in new application areas.

Features

RDWARE FEATURES

- Single Chip USB ⇔Asynchronous Serial Data Transfer
- Full Handshaking & Modem Interface Signals
- UART I/F Supports 7 / 8 Bit Data, 1 / 2 Stop Bits and Odd/Even/Mark/Space/No Parity
- Data rate 300 => 3M Baud (TLL)
- Data rate 300 => 1M Baud (RS232)
- Data rate 300 => 3M Baud (RS422/RS485)
- 384 Byte Receive Buffer / 128 Byte Transmit Buffer for high data throughput
- Adjustable RX buffer timeout
- Full hardware assisted hardware or X-On / X-Off handshaking
- In-built support for event characters and line break condition
- Auto Transmit Buffer control for RS485
- Support for USB Suspend / Resume through SLEEP# and RI# pins
- Support for high power USB Bus powered devices through PWREN# pin
- Integrated level converter on UART and control signals for interfacing to 5v and 3.3v logic
- Integrated 3.3v regulator for USB IO
- Integrated Power-On-Reset circuit
- Integrated 6MHz – 48Mhz clock multiplier PLL
- USB Bulk or Isocronous data transfer modes
- 4.4v to 5.25v single supply operation
- UHCI / OHCI / EHCI host controller compatible
- USB 1.1 and USB 2.0 compatible
- USB VID, PID , Serial Number and Product Description strings in external EEPROM
- EEPROM programmable on-board via USB

VIRTUAL COM PORT (VCP) DRIVERS for

- Windows 98 and Windows 98 SE
- Windows 2000 / ME / XP
- Windows CE **
- MAC OS-8 and OS-9
- MAC OS-X **
- Linux 2.40 and greater

D2XX (USB Direct Drivers + DLL S/W Interface)

- Windows 98 and Windows 98 SE
- Windows 2000 / ME / XP

APPLICATION AREAS

- USB ⇔RS232 Converters
- USB ⇔ RS422 / RS485 Converters
- Upgrading RS232 Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- PDA ⇔ USB data transfer
- USB Smart Card Readers
- Set Top Box (S.T.B.) PC - USB interface
- USB Hardware Modems
- USB Wireless Modems
- USB Instrumentation
- USB Bar Code Readers

[** = In planning or under development]

Enhancements

; section summarises the enhancements of the 2nd generation device compared to it's FT8U232AM predecessor. further details, consult the device pin-out description and functional descriptions.

Integrated Power-On-Reset (POR) Circuit
The device now incorporates an internal POR function. The existing RESET# pin is maintained in order to allow external logic to reset the device where required. however for many applications this pin can now be either left N/C or hard wired to VCC. In addition, a new reset output pin (RSTO#) is provided in order to allow the new POR circuit to provide a stable reset to external MCU and other devices. RSTO# was the TEST pin on the previous generation of devices.

Integrated RCCLK Circuit
In the previous devices, an external RC circuit was required to ensure that the oscillator and clock multiplier PLL frequency was stable prior to enabling the clock internal to the device. This circuit is now embedded on-chip – the pin assigned to this function is now designated as the TEST pin and should be tied to GND for normal operation.

Integrated Level Converter on UART interface and control signals
The previous devices would drive the UART and control signals at 5v CMOS logic levels. The new device has a separate VCC-IO pin allowing the device to directly interface to 3.3v and other logic families without the need for external level converter i.c.'s

- **Improved Power Management control for USB Bus Powered, high current devices**
  The previous devices had a USBEN pin, which became active when the device was enumerated by USB. To provide power control, this signal had to be externally gated with SLEEP# and RESET#. This gating is now done on-chip - USBEN has now been replaced with the new PWREN# signal which can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. A new EEPROM based option makes the device pull gently down it's UART interface lines when the power is shut off (PWREN# is High). In this mode, any residual voltage on external circuitry is bled to GND when power is removed thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored.
- **Lower Suspend Current**
  Integration of RCCLK within the device and internal design improvements reduce the suspend current of the FT232BM to under 200uA (excluding the 1.5k pull-up on USB DP) in USB suspend mode. This allows greater margin for peripherals to meet the USB Suspend current limit of 500uA.
- **Support for USB Isocronous Transfers**
  Whilst USB Bulk transfer is usually the best choice for data transfer, the scheduling time of the data is not guaranteed. For applications where scheduling latency takes priority over data integrity such as transferring audio and low bandwidth video data, the new device now offers an option of USB Isocronous transfer via an option bit in the EEPROM.

Programmable Receive Buffer Timeout

In the previous device, the receive buffer timeout used to flush remaining data from the receive buffer was fixed at 16ms timeout. This timeout is now programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the device to be better optimised for protocols requiring faster response times from short data packets.

TXDEN Timing fix

TXDEN timing has now been fixed to remove the external delay that was previously required for RS485 applications at high baud rates. TXDEN now works correctly during a transmit send-break condition.

Relaxed VCC Decoupling

The 2nd generation devices now incorporate a level of on-chip VCC decoupling. Though this does not eliminate the need for external decoupling capacitors, it significantly improves the ease of pcb design requirements to meet FCC,CE and other EMI related specifications.

Improved PreScaler Granularity

The previous version of the Prescaler supported division by (n + 0), (n + 0.125), (n + 0.25) and (n + 0.5) where n is an integer between 2 and 16,384 (2^{14}). To this we have added (n + 0.375), (n + 0.625), (n + 0.75) and (n+ 0.875) which can be used to improve the accuracy of some baud rates and generate new baud rates which were previously impossible (especially with higher baud rates).

- **Bit Bang Mode**

The 2nd generation device has a new option referred to as "Bit Bang" mode. In Bit Bang mode, the eight UART interface control lines can be switched between UART interface mode and an 8-bit Parallel IO port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by the prescaler setting. As well as allowing the device to be used stand-alone as a general purpose IO controller for example controlling lights, relays and switches, some other interesting possibilities exist. For instance, it may be possible to connect the device to an SRAM configurable FPGA as supplied by vendors such as Altera and Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use Bit Bang Mode to download configuration data to the FPGA which would define it's hardware function, then after the FPGA device is configured the FT232BM can switch back into UART interface mode to allow the programmed FPGA device to communicate with the PC over USB. This approach allows a customer to create a "generic" USB peripheral who's hardware function can be defined under control of the application software. The FPGA based hardware can be easily upgraded or totally changed simply by changing the FPGA configuration data file. Application notes, software and development modules for this application area will be available from FTDI and other 3rd parties.

PreScaler Divide By 1 Fix

The previous device had a problem when the integer part of the divisor was set to 1. In the 2nd generation device setting the prescaler value to 1 gives a baud rate of 2 million baud and setting it to zero gives a baud rate of 3 million baud. Non-integer division is not supported with divisor values of 0 and 1.

Less External Support Components

As well as eliminating the RCCLK RC network, and for most applications the need for an external reset circuit, we have also eliminated the requirement for a 100k pull-up on EECS to select 6MHz operation. When the FT232BM is being used without the configuration EEPROM, EECS, EESK and EEDATA can now be left n/c. For circuits requiring a long reset time (where the device is reset externally using a reset generator i.c., or reset is controlled by the IO port of a MCU, FPGA or ASIC device) an external transistor circuit is no longer required as the 1k5 pull-up resistor on USB DP can be wired to the RESETO# pin instead of to 3.3v. Note : RESETO# drives out at 3.3v level, not at 5v VCC level. This is the preferred configuration for new designs. In some other configurations, RSTO# can be used to reset external logic / MCU circuitry.

Extended EEROM Support

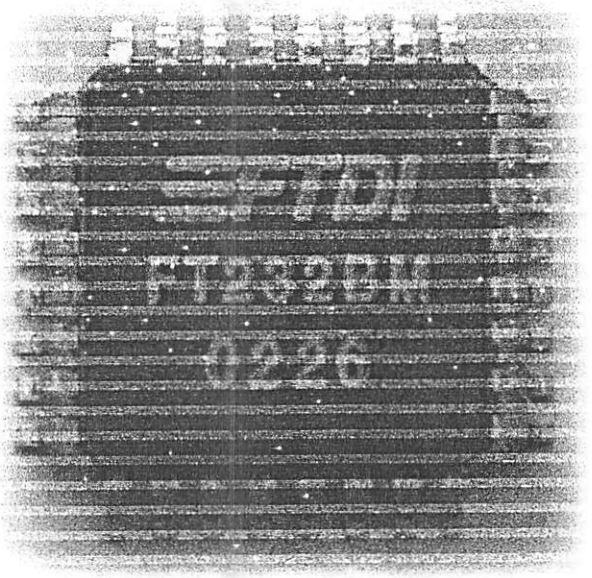
The previous generation of devices only supported EEPROM of type 93C46 (128 x 16 bit). The new devices will also work with EEPROM type 93C56 (256 x 16 bit) and 93C66 (512 x 16 bit). The extra space is not used by the device, however it is available for use by other external MCU / logic whilst the FT232BM is being held in reset.

- **USB 2.0 (full speed option)**

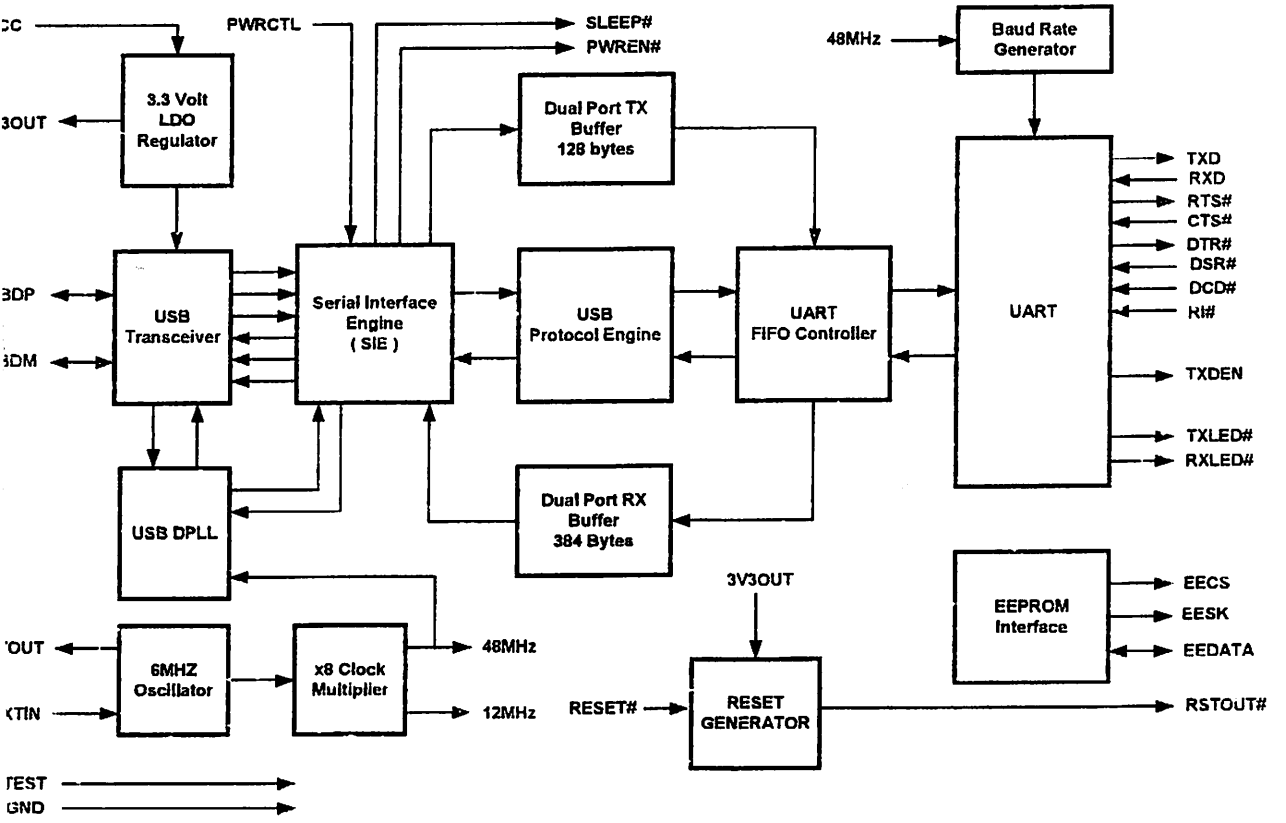
  A new EEPROM based option allows the FT232BM to return a USB 2.0 device descriptor as opposed to USB 1.1. Note : The device would be a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).

- **Multiple Device Support without EEPROM**

  When no EEPROM (or a blank or invalid EEPROM) is attached to the device, the FT232BM no longer gives a serial number as part of it's USB descriptor. This allows multiple devices to be simultaneously connected to the same PC. However, we still highly recommend that EEPROM is used, as without serial numbers a device can only be identified by which hub port in the USB tree it is connected to which can change if the end user re-plugs the device into a different port.



Block Diagram (simplified)



Functional Block Descriptions

3.3V LDO Regulator

The 3.3V LDO Regulator generates the 3.3 volt reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides 3.3v power to the RSTOUT# pin. The main function of this block is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, external circuitry requiring 3.3v nominal at a current of not greater than 5mA could also draw it's power from the 3V3OUT pin if required.

USB Transceiver

The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide 3.3 volt level slew rate control signalling, whilst a differential receiver and two single ended receivers provide USB data in, SEO and USB Reset condition detection.

USB DPLL

The USB DPLL cell locks on to the incoming NRZI USB data and provides separate recovered clock and data signals to the SIE block.

6MHz Oscillator

The 6MHz Oscillator cell generates a 6MHz reference clock input to the X8 Clock multiplier from an external 6MHz crystal or ceramic resonator.

x8 Clock Multiplier

The x8 Clock Multiplier takes the 6MHz input from the Oscillator cell and generates a 12MHz reference clock for the SIE, USB Protocol Engine and UART FIFO controller blocks. It also generates a 48MHz reference clock for the USB DPPL and the Baud Rate Generator blocks.

Serial Interface Engine (SIE)

The Serial Interface Engine (SIE) block performs the Parallel to Serial and Serial to Parallel conversion of the USB data. In accordance to the USB 1.1 specification, it performs bit stuffing / un-stuffing and CRC5 / CRC16 generation / checking on the USB data stream.

USB Protocol Engine

The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol (Chapter 9) requests generated by the USB host controller and the commands for controlling the functional parameters of the UART.

Dual Port TX Buffer (128 bytes)

Data from the USB data out endpoint is stored in the Dual Port TX buffer and removed from the buffer to the UART transmit register under control of the UART FIFO controller.

Dual Port RX Buffer (384 bytes)

Data from the UART receive register is stored in the Dual Port RX buffer prior to being removed by the SIE on a USB request for data from the device data in endpoint.

UART FIFO Controller

The UART FIFO controller handles the transfer of data between the Dual Port RX and TX buffers and the UART transmit and receive registers.

UART

The UART performs asynchronous 7 / 8 bit Parallel to Serial and Serial to Parallel conversion of the data on the RS232 (RS422 and RS485) interface. Control signals supported by the UART include RTS, CTS, DSR , DTR, DCD and RI. The UART provides a transmitter enable control signal (TXDEN) to assist with interfacing to RS485 transceivers. The UART supports RTS/CTS, DSR/DTR and X-On/X-Off handshaking options. Handshaking, where required, is handled in hardware to ensure fast response times. The UART also supports the RS232 BREAK setting and detection conditions.

Baud Rate Generator

The Baud Rate Generator provides a x16 clock input to the UART from the 48MHz reference clock and consists of a 14 bit prescaler and 3 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 3 million baud.

RESET Generator

The Reset Generator Cell provides a reliable power-on reset to the device internal circuitry on power up. An additional RESET# input and RSTOUT# output are provided to allow other devices to reset the FT232BM or the FT232BM to reset other devices respectively. During reset, RSTOUT# is high-impedance otherwise it drives out at the 3.3v provided by the onboard regulator. RSTOUT# can be used to control the 1k5 pull-up on USB DP directly where delayed USB enumeration is required. It can also be used to reset other devices. RSTOUT# will stay high-impedance for approximately 5ms after VCC has risen above 3.5v AND the device oscillator is running AND RESET# is high. RESET# should be tied to VCC unless it is a requirement to reset the device from external logic or an external reset generator i.c.

EEPROM Interface

Though the FT232BM will work without the optional EEPROM, an external 93C46 (93C56 or 93C66) EEPROM can be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT232BM for OEM applications. The EEPROM is also required for applications where multiple FT232BM's are connected to a single PC as the drivers rely on a unique serial number for each device to bind a unique virtual COM port to each individual device. Other parameters controlled by the EEPROM include Remote Wake Up, Isochronous Transfer Mode, Soft Pull Down on Power-Off and USB 2.0 descriptor modes. The EEPROM should be a 16 bit wide configuration such as a MicroChip 93LC46B or equivalent capable of a 1Mb/s clock rate at VCC = 4.4v to 5.25v. The EEPROM is programmable-on board over USB using a utility available from FTDI's web site (http://www.ftdichip.com). This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process.

If no EEPROM is connected (or the EEPROM is blank), the FT232BM will use it's built-in default VID, PID Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

Device Pin-Out

Figure 1

'in-Out (LQFP-32 Package)

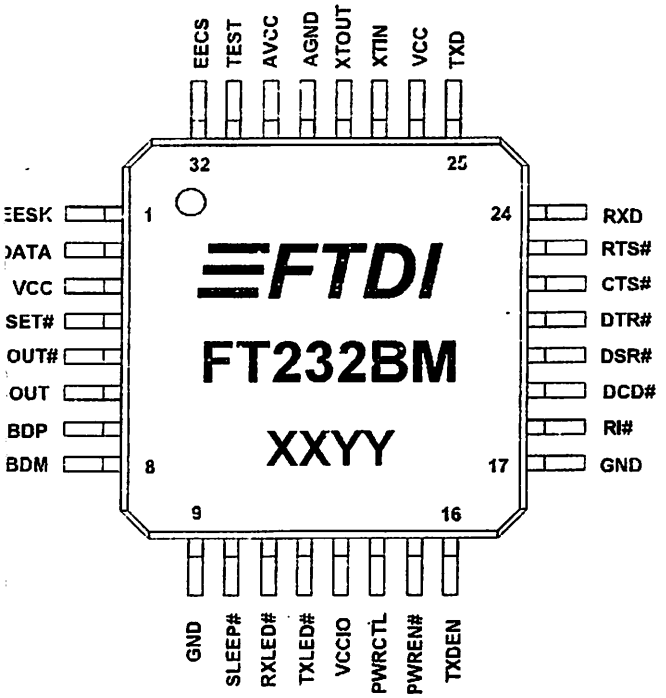
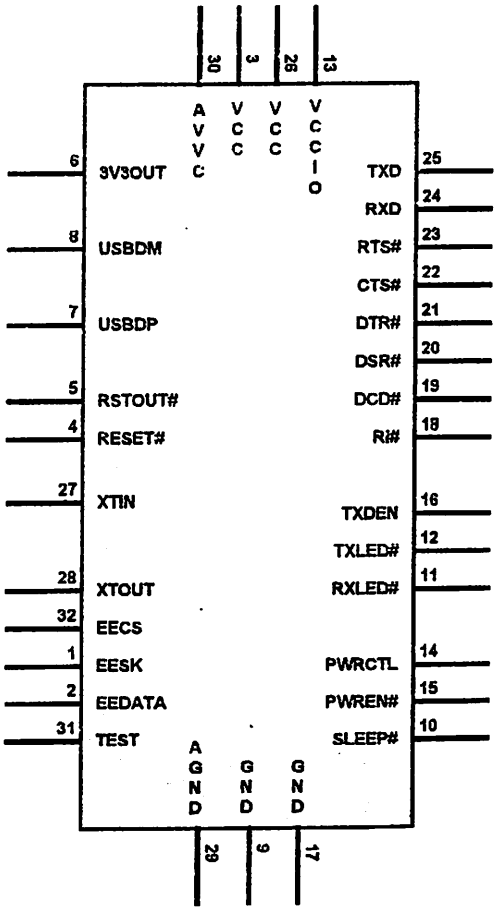


Figure 2

Pin-Out (Schematic Symbol)



Signal Descriptions

ble 1 - FT232BM - PINOUT DESCRIPTION

RT INTERFACE GROUP

#	Signal	Type	Description
	TXD	OUT	Transmit Asynchronous Data Output
	RXD	IN	Receive Asynchronous Data Input
	RTS#	OUT	Request To Send Control Output / Handshake signal
	CTS#	IN	Clear To Send Control Input / Handshake signal
	DTR#	OUT	Data Terminal Ready Control Output / Handshake signal
	DSR#	IN	Data Set Ready Control Input / Handshake signal
	DCD#	IN	Data Carrier Detect Control Input
	RI#	IN	Ring Indicator Control Input. When the Remote Wakeup option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend.
	TXDEN	OUT	Enable Transmit Data for RS485

INTERFACE GROUP

#	Signal	Type	Description
	USBDP	I/O	USB Data Signal Plus (Requires 1.5k pull-up to 3V3OUT or RSTOUT#)
	USBDM	I/O	USB Data Signal Minus

ROM INTERFACE GROUP

#	Signal	Type	Description
	EECS	I/O	EEPROM – Chip Select. For 48MHz operation pull EECS to GND using a 10k resistor. For 6MHz operation no resistor is required. Tri-State during device reset.
	EESK	OUT	Clock signal to EEPROM. Tri-State during device reset, else drives out.
	EEDATA	I/O	EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2k2 resistor. Also pull Data-Out of the EEPROM to VCC via a 10k resistor for correct operation. Tri-State during device reset.

VER CONTROL GROUP

#	Signal	Type	Description
	SLEEP#	OUT	Goes Low during USB Suspend Mode. Typically used to power-down an external TTL to RS232 level converter i.c. in USB -> RS232 converter designs.
	PWREN#	OUT	Goes Low after the device is configured via USB, then high during USB suspend. Can be used to control power to external logic using a P-Channel Logic Level MOSFET switch. Enable the Interface Pull-Down Option in EEPROM when using the PWREN# pin in this way.
	PWRCTL	IN	Bus Powered – Tie Low / Self Powered – Tie High

CELLANEOUS SIGNAL GROUP

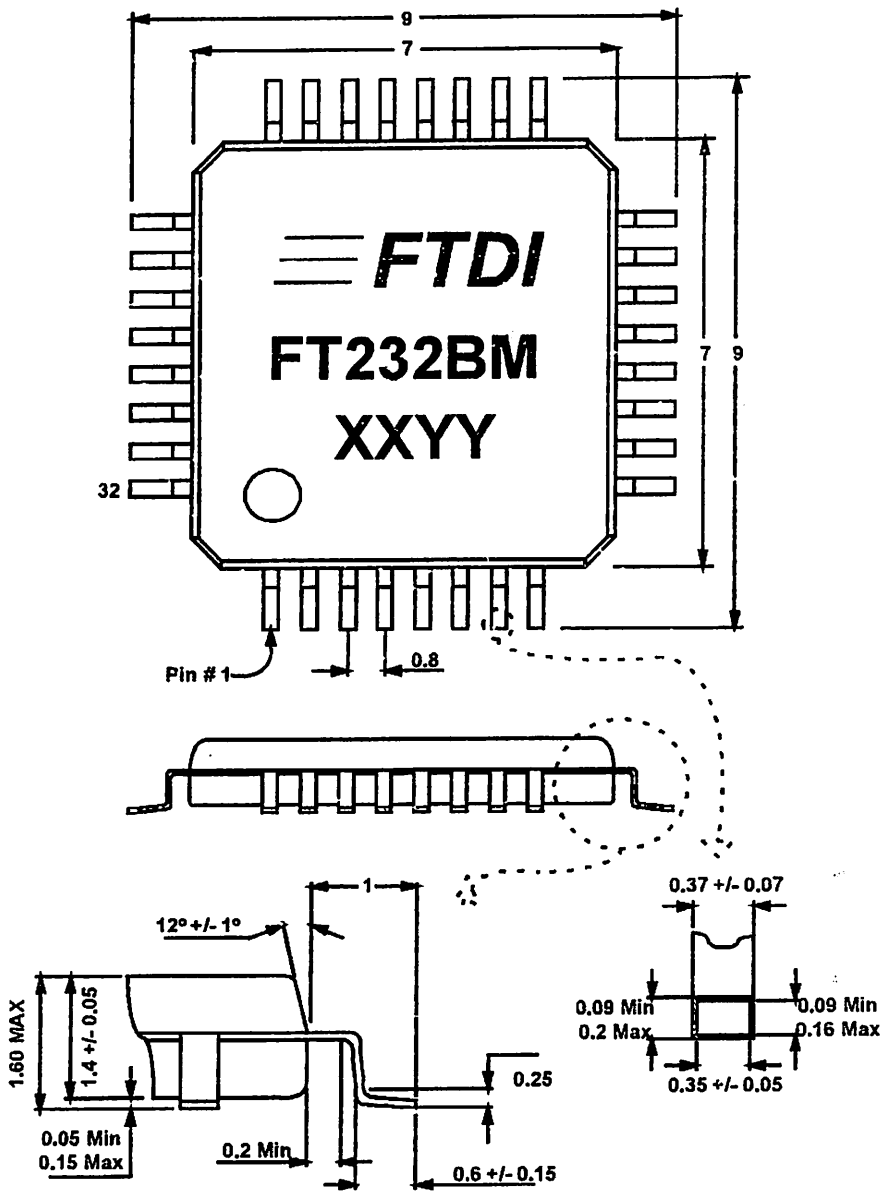
n#	Signal	Type	Description
	RESET#	IN	Can be used by an external device to reset the FT232BM. If not required, tie to VCC.
	RSTOUT#	OUT	Output of the internal Reset Generator. Stays high impedance for ~ 2ms after VCC > 3.5v and the internal clock starts up, then clamps it's output to the 3.3v output of the internal regulator. Taking RESET# low will also force RSTOUT# to go high impedance. RSTOUT# is NOT affected by a USB Bus Reset.
	TXLED#	O.C.	LED Drive - Pulses Low when Transmitting Data via USB
	RXLED#	O.C.	LED Drive - Pulses Low when Receiving Data via USB
	XTIN	IN	Input to 6MHz Crystal Oscillator Cell. This pin can also be driven by an external 6MHz clock if required. Note : Switching threshold of this pin is VCC/2, so if driving from an external source, the source must be driving at 5V CMOS level or a.c. coupled to centre around VCC/2.
	XTOUT	OUT	Output from 6MHz Crystal Oscillator Cell. XTOUT stops oscillating during USB suspend, so take care if using this signal to clock external logic.
	TEST	IN	Puts device in i.c. test mode – must be tied to GND for normal operation.

VER AND GND GROUP

#	Signal	Type	Description
	3V3OUT	OUT	3.3 volt Output from the integrated L.D.O. regulator This pin should be decoupled to GND using a 33nF ceramic capacitor in close proximity to the device pin. It's prime purpose is to provide the internal 3.3v supply to the USB transceiver cell and the RSTOUT# pin. A small amount of current (<= 5mA) can be drawn from this pin to power external 3.3v logic if required.
5	VCC	PWR	+4.4 volt to +5.25 volt VCC to the device core, LDO and and none-UART interface pins.
	VCCIO	PWR	+3.0 volt to +5.25 volt VCC to the UART interface pins 10..12, 14..16 and 18..25. When interfacing with 3.3v external logic connect VCCIO to the 3.3v supply of the external logic, otherwise connect to VCC to drive out at 5v CMOS level.
7	GND	PWR	Device– Ground Supply Pins
	AVCC	PWR	Device - Analog Power Supply for the internal x8 clock multiplier
	AGND	PWR	Device - Analog Ground Supply for the internal x8 clock multiplier

Package Outline

ure 3 – 32 LD LQFP Package Dimensions



he FT232BM is supplied in a 32 LD LQFP package as standard. This package has a 7mm x 7mm body (9mm 9mm including leads) with leads on a 0.8mm pitch. An alternative 5mm x 5mm leadless chip scale package is available on special request for projects where package area is critical.

The above drawing shows the LQFP-32 package – all dimensions are in millimetres.

XXYY = Date Code (XX = 2 digit year number, YY = 2 digit week number.

Absolute Maximum Ratings

se are the absolute maximum ratings for the FT232BM device in accordance with the Absolute Maximum Rating System : 60134). Exceeding these may cause permanent damage to the device.

Storage Temperature ..... –65°C to + 150°C
Ambient Temperature (Power Applied) ..... 0°C to + 70°C
VCC Supply Voltage ..... -0.5v to +6.00v
DC Input Voltage - Inputs ..... -0.5v to VCC + 0.5v
DC Input Voltage - High Impedance Bidirectionals ..... -0.5v to VCC + 0.5v
DC Output Current – Outputs 24mA
DC Output Current – Low Impedance Bidirectionals 24mA
Power Dissipation (VCC = 5.25v) 500mW
Electrostatic Discharge Voltage (I < 1uA) ..... +/- 2000v
Latch Up Current (Vi < 0 or Vi > Vcc) 100mA

D.C. Characteristics

Characteristics (Ambient Temperature = 0 .. 70°C)

rating Voltage and Current

ameter	Description	Min	Typ	Max	Units	Conditions
:1	VCC Operating Supply Voltage	4.4	5.0	5.25	V	
:2	VCCIO Operating Supply Voltage	3.0	-	5.25	V	
1	Operating Supply Current	-	25	-	mA	Normal Operation
2	Operating Supply Current	-	180	200	uA	USB Suspend ** Note 1

1 – Supply current excludes the 200uA nominal drawn by the external pull-up resistor on USB DP.

T IO Pin Characteristics (VCCIO = 5.0v)

ameter	Description	Min	Typ	Max	Units	Conditions
)	Output Voltage High	4.4	-	4.9	V	I source = 2mA
	Output Voltage Low	0.1	-	0.7	V	I sink = 4 mA
	Input Switching Threshold	1.1	1.5	1.9	V	Note 2
/s	Input Switching Hysteresis		200		mV	

T IO Pin Characteristics (VCCIO = 3.3v)

ameter	Description	Min	Typ	Max	Units	Conditions
	Output Voltage High	2.7	-	3.2	V	I source = 2mA
	Output Voltage Low	0.1	-	0.7	V	I sink = 4 mA
	Input Switching Threshold	1.0	1.4	1.8	V	Note 2
/s	Input Switching Hysteresis		200		mV	

2 – Inputs have an internal 200k pull-up resistor to VCCIO.

N / XTOUT Pin Characteristics

rameter	Description	Min	Typ	Max	Units	Conditions
h	Output Voltage High	4.0	-	5.0	V	Fosc = 6MHz
l	Output Voltage Low	0.1	-	1.0	V	Fosc = 6MHz
	Input Switching Threshold	1.8	2.5	3.2	V	

SET#, TEST, EECS, EESK, EEDATA, IO Pin Characteristics

rameter	Description	Min	Typ	Max	Units	Conditions
h	Output Voltage High	4.4	-	4.9	V	I source = 2mA
l	Output Voltage Low	0.1	-	0.7	V	I sink = 4 mA
	Input Switching Threshold	1.1	1.5	1.9	V	Note 3
ys	Input Switching Hysteresis		200		mV	

3 – EECS and EEDATA pins have an internal 200k pull-up resistor to VCC

OUT Pin Characteristics

ameter	Description	Min	Typ	Max	Units	Conditions
	Output Voltage High	3.0	-	3.6	V	I source = 2mA
	Leakage Current Tri-State	-	-	5	uA	

IO Pin Characteristics

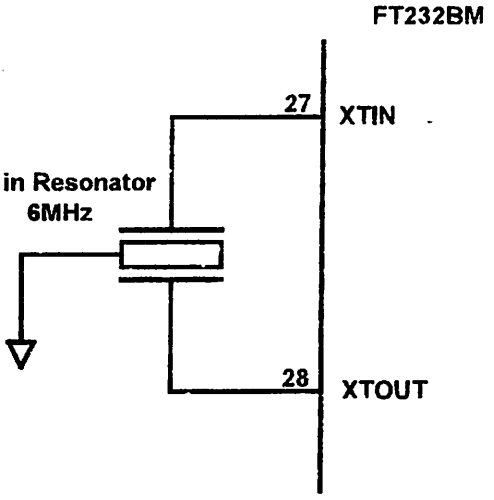
ameter	Description	Min	Typ	Max	Units	Conditions
oh	IO Pins Static Output (High)	2.8		3.6v	V	RI = 1k5 to 3V3Out (D+) RI = 15k to GND (D-)
ol	IO Pins Static Output (Low)	0		0.3	V	RI = 1k5 to 3V3Out (D+) RI = 15k to GND (D-)
se	Single Ended Rx Threshold	0.8		2.0	V	
om	Differential Common Mode	0.8		2.5	V	
oif	Differential Input Sensitivity	0.2			V	
vZ	Driver Output Impedance	29		44	ohm	Note 4

4 – Driver Output Impedance includes the external 27R series resistors on USBDP and USBDM pins.

Device Configuration Examples

Oscillator Configurations

ure 4
'in Ceramic Resonator
nfiguration



'e 4 illustrates how to use the FT232BM with
'in Ceramic Resonator such as Murata Part #
_S6M00G53 or equivalent. 3-Pin resonators have
)ad capacitors built into the resonator so no external
ng capacitors are required. This makes for an
omical configuration. Though the typical accuracy of
a resonator is +/- 0.5% and is technically out-with
SB specification, it has been calculated that using
a device will work satisfactorily in practice with the
2BM design.

Figure 5
Crystal or 2-Pin Ceramic Resonator Configuration

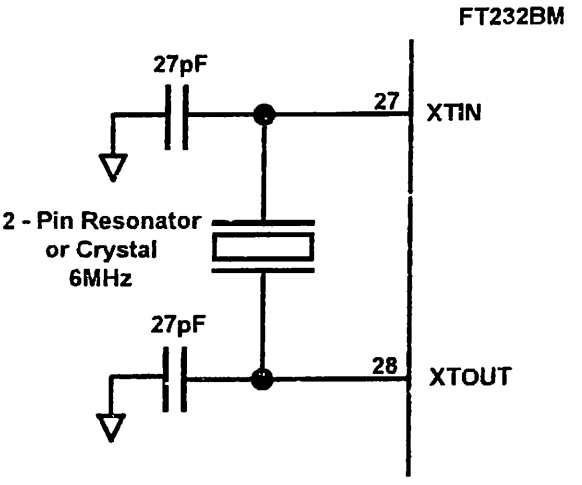


Figure 5 illustrates how to use the FT232BM with a 6MHz Crystal or 2-Pin Ceramic Resonator. In this case, these devices do not have in-built loading capacitors so these have to be added between XTIN, XTOUT and GND as shown. A value of 27pF is shown as the capacitor in the example – this will be good for many crystals and some resonators but do select the value based on the manufacturers recommendations wherever possible. If using a crystal, use a parallel cut type. If using a resonator, see the previous note on frequency accuracy.

EEPROM Configuration

jure 6
Prom Configuration

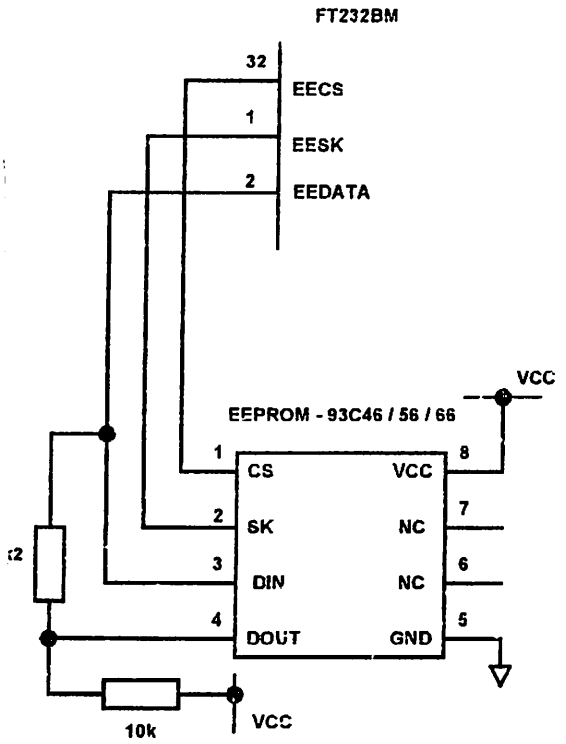


Figure 6 illustrates how to connect the FT232BM to the 93C46 (93C56 or 93C66) EEPROM. EECS (pin 32) is directly connected to the chip select (CS) pin of the EEPROM. EESK (pin 1) is directly connected to the clock (SK) pin of the EEPROM. EEDATA (pin 2) is directly connected to the Data In (Din) pin of the EEPROM. There is a potential condition whereby both the Data Output (Dout) of the EEPROM can drive out at the same time as the EEDATA pin of the FT232BM. To prevent potential data clash in this situation, the Dout of the EEPROM is connected to EEDATA of the FT232BM via a 2k2 resistor.

Following a power-on reset or a USB reset, the FT232BM will scan the EEPROM to find out a) if an EEPROM is attached to the Device and b) if the data in the device is valid. If both of these are the case, then the FT232BM will use the data in the EEPROM, otherwise it will use it's built-in default values. When a valid command is issued to the EEPROM from the FT232BM, the EEPROM will acknowledge the command by pulling it's Dout pin low. In order to check for this condition, it cessary to pull Dout high using a 10k resistor. If the command acknowledge doesn't happen then EEDATA will illed high by the 10k resistor during this part of the cycle and the device will detect an invalid command or no ROM present.

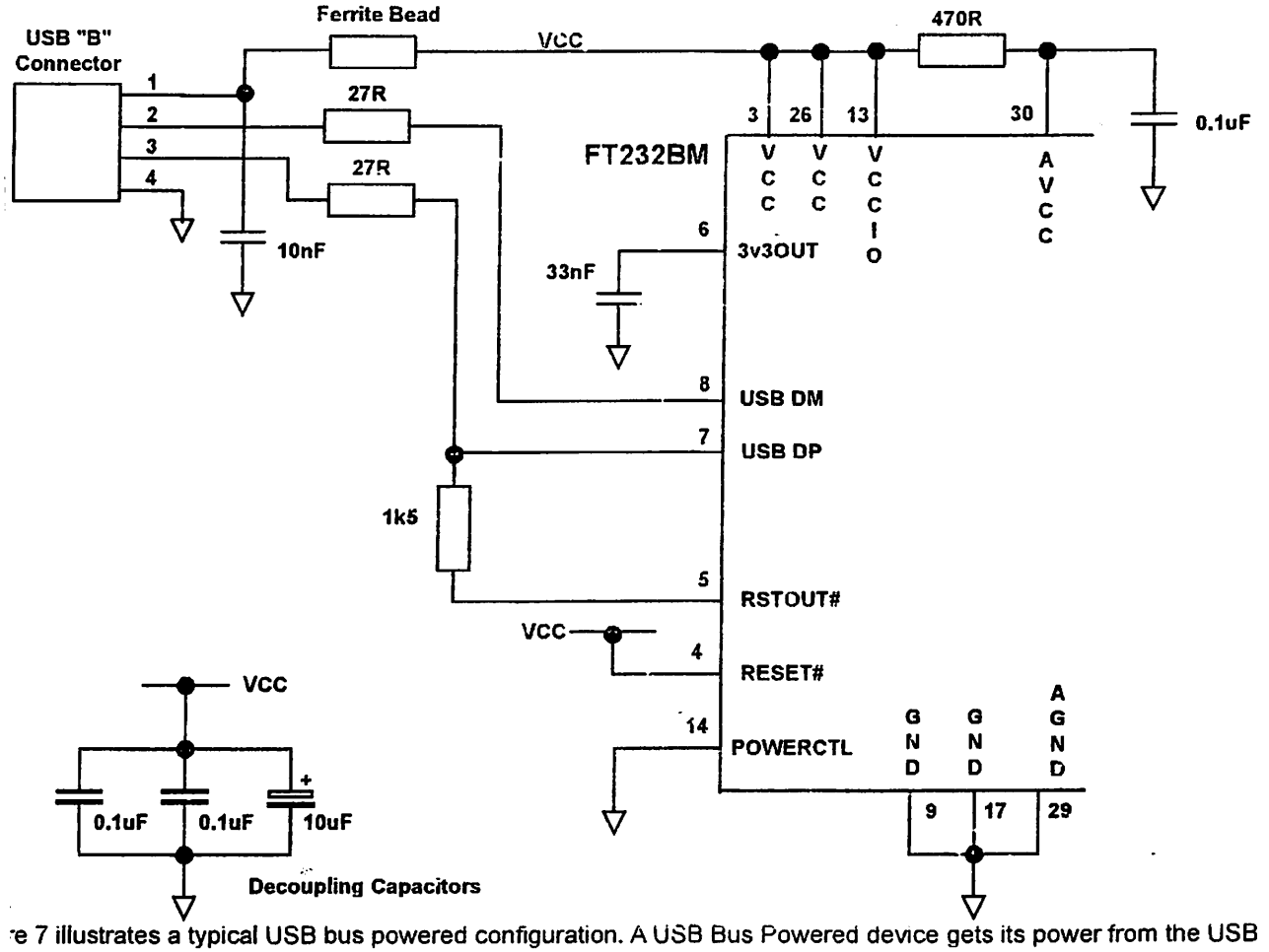
e are two varieties of these EEPROMs on the market – one is configured as being 16 bits wide, the other nfigured as being 8 bits wide. These are available from many sources such as Microchip, ST, SIS etc. The 2BM requires EEPROMs with a 16-bit wide configuration such as the Microchip 93LC46B device. The EEPROM be capable of reading data at a 1Mb clock rate at a supply voltage of 4.4v to 5.25v. Most available parts are ole of this.

k the manufacturers data sheet to find out how to connect pins 6 and 7 of the EEPROM. Some devices specify as no-connect, others use them for selecting 8 / 16 bit mode or for test functions. Some other parts have their t rotated by 90° so please select the required part and it's options carefully.

ossible to "share" the EEPROM between the FT232BM and another external device such as an MCU. However, an only be done when the FT232BM is in it's reset condition as it tri-states it's EEPROM interface at that time. cal configuration would use four bit's of an MCU IO Port. One bit would be used to hold the FT232BM reset (RESET#) on power-up, the other three would connect to the EECS, EESK and EEDATA pins of the FT232BM er to read / write data to the EEPROM at this time. Once the MCU has read / written the EEPROM, it would take T# high to allow the FT232BM to configure itself and enumerate over USB.

USB Bus Powered and Self Powered Configuration

ure 7
B Bus Powered Configuration



e 7 illustrates a typical USB bus powered configuration. A USB Bus Powered device gets its power from the USB
Basic rules for USB Bus power devices are as follows –

On plug-in, the device must draw no more than 100mA

On USB Suspend the device must draw no more than 500uA.

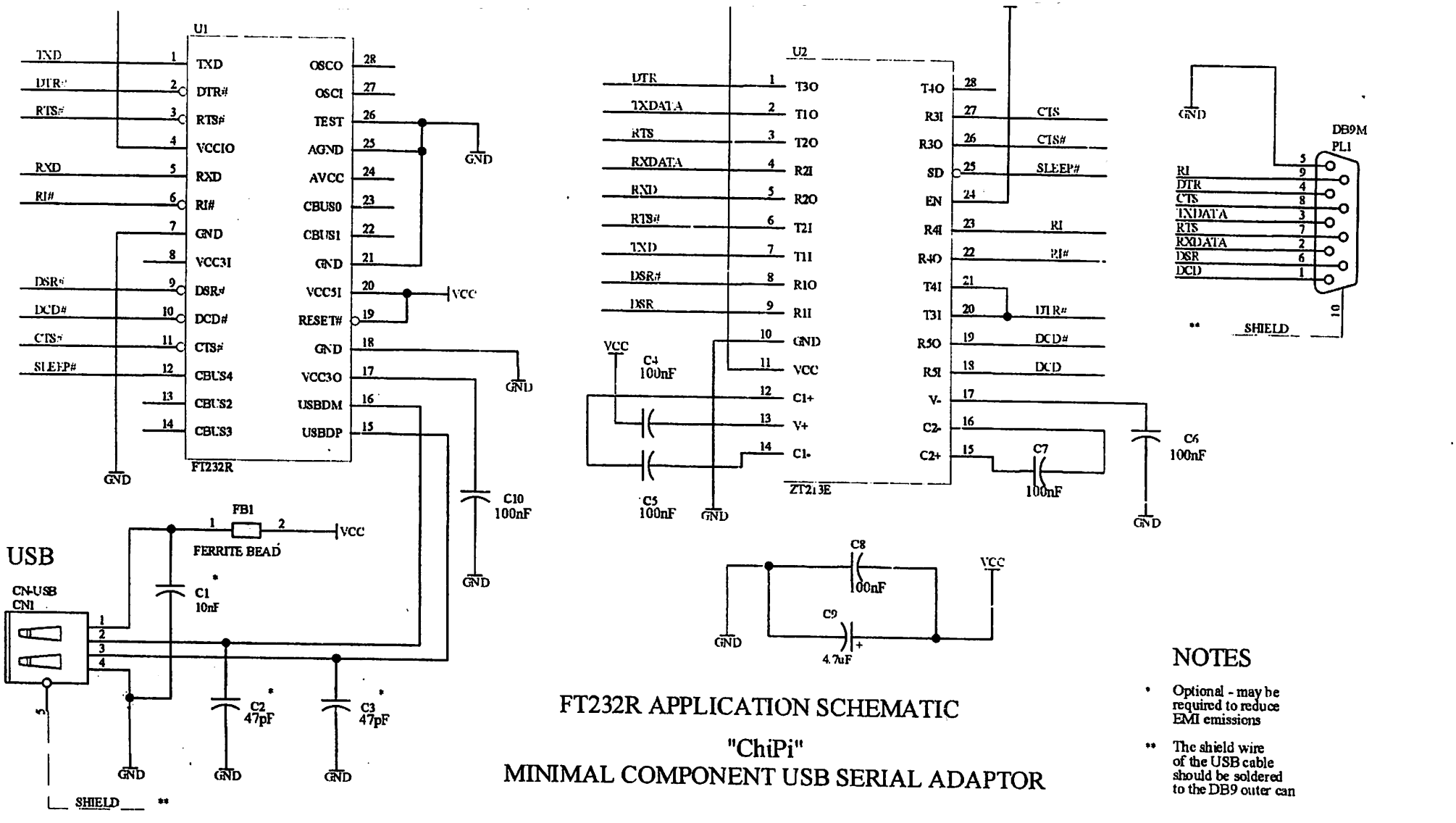
A Bus Powered High Power Device (one that draws more than 100mA) should use the PWREN# pin to keep the urrent below 100mA on plug-in and 500uA on USB suspend.

A device that consumes more than 100mA can not be plugged into a USB Bus Powered Hub

lo device can draw more that 500mA from the USB Bus.

'ERCTL (pin 14) is pulled low to tell the device to use a USB Bus Power descriptor. The power descriptor in the ROM should be programmed to match the current draw of the device.

rite Bead is connected in series with USB power to prevent noise from the device and associated circuitry (EMI g radiated down the USB cable to the Host. The value of the Ferrite Bead depends on the total current required e circuit – a suitable range of Ferrite Beads is available from Steward (www.steward.com) for example Steward **MI0805K400R-00 also available as DigiKey Part #** 240-1035-1.



FT232R APPLICATION SCHEMATIC

"ChiPi"
MINIMAL COMPONENT USB SERIAL ADAPTOR

NOTES

* Optional - may be required to reduce EMI emissions

** The shield wire of the USB cable should be soldered to the DB9 outer can