INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

PERENCANAAN DAN PEMBUATAN ALAT OTOMATIS PEMBERSIH PADA LANTAI DATAR MENGGUNAKAN TEKNOLOGI MIKROKONTROLLER AT89S51

SKRIPSI

Disusun oleh :
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98.17.050

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PERPUSTAKAAN
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PERENCANAAN DAN PEMBUATAN ALAT OTOMATIS PEMBERSIH PADA LANTAI DATAR MENGGUNAKAN TEKNOLOGI MIKROKONTROLLER AT89S51

SKRIPSI

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ABSTRAKSI

PERENCANAAN DAN PEMBUATAN ALAT OTOMATIS PEMBERSIH PADA LANTAI DATAR MENGGUNAKAN TEKNOLOGI MIKROKONTROLER AT89S51

(Bayu Krisdianto, 98.17.050, Teknik Elektro / T. Elektronika S - 1)
(Dosen Pembimbing : Ir. Erfan A Dahlan Dan M Ibrahim Ashari ,ST)

Kata Kunci : Mikrokontroller, Sensor Putaran, Driver Motor, Motor DC Keypad, dan LCD.

Teknologi dibuat dan diciptakan untuk membantu pekerjaan manusia atau untuk membuat suatu pekerjaan menjadi lebih mudah dan efisien, penerapan teknologi dimanfaatkan oleh semua bidang salah satunya adalah bidang kebersihan, khususnya pada sistem kebersihan pada lantai datar, dimana selama ini sistem kebersihan pada lantai datar masih menggunakan sistem manual yaitu dengan menggunakan tenaga manusia sebagai media pembersihnya, sehingga banyak tenaga manusia yang terbuang.

Untuk merancang atau pembuat alat pembersih pada lantai datar digunakan teknologi sistem kontrol teknologi lainnya. Salah satunya dengan menggunakan Mikrokontroller AT89S51, dengan menambahkan komponen luar sebagai piranti pendukung sehingga dapat dibuat suatu alat pembersih pada lantai datar yang mampu membersihkan lantai datar secara otomatis.

Prinsip kerja dari sistem ini pertama kita memasukkan luas wilayah yang akan dibersihkan melalui keypad, luas wilayah ini akan ditampilkan ke LCD dengan bantuan mikrokontroller AT89S51. setelah luas wilayah diketahui, maka alat akan mulai bergerak dengan sistem scanning vertical sesuai dengan luas wilayahnya. Untuk mengetahui berapa jarak yang telah ditempuh dapaty diketahui dengan memasang sensor putaran (optoisolator)yang dipasang pada tiap sisi roda penggerak. IC AT89S51 akan menghitung jumlah pulsa dari tiap-ntiap sensor putaran. Untuk menggerakkan roda kiri dan kanan digunakan dua buah motor dc yanag dikendalikan melalui driver motor dc. Komponen utama driver motor dc ini adalah IC L298 Dan pada saat pembersih mulai diaktifkan, secara terus menerus vacuum akan bekerja. Dengan adanya alat ini diharapkan sistem pembersihan pada lantai datar dapat dilakukan secara otomatis dan lebih efisien.

KATA PENGANTAR

Puji syukur kehadirat Allaw SWT yang senantiasa memberikan taufik dan hidayah-Nya sehingga penyusun dapat menyelesaikan tugas akhir yang berjudul:

"PERENCANAAN DAN PEMBUATAN ALAT OTOMATIS PEMBERSIH PADA LANTAI DATAR MENGGUNAKAN TEKNOLOGI MIKROKONTROLER AT 89S51 "

Pembuatan tugas akhir ini disusun guna memenuhi syarat akhir kelulusan pendidikan jenjang Strata-1 di Institut Teknologi Nasional Malang. Laporan tugas akhir ini merupakan tanggung jawab tertulis atas ilmu pengetahuan yang didapat selama penyusun mengikuti kuliah.

Atas selesainya tugas akhir ini, penyusun mengucapkan ucapan terimakasih kepada :

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- Nabi Muhammad SAW, penerang jalan hidupku.
- Ayahanda, ibunda serta keluargaku tercinta yang selalu memberikan dukungan moral dan material.
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- Bapak Ir. Wayan Sujana, MT, selaku Dekan Fakultas Teknologi Institut Teknologi Nasional Malang.
- Rekan-rekan seperjuangan yang selalu mendukungku.
- Rekan-rekan instruktur Laboratorium Elektronika ITN Malang

Penyusun menyadari bahwa laporan ini masih banyak yang perlu disempurnakan. Oleh sebab itu kritik dan saran yang membangun sangat diharapkan.

Akhir kata, penyusun mohan maaf kepada semua pihak bilamana selama penyusunan skripsi ini penyusun membuat kesalahan secara tidak sengaja dan semoga skripsi ini dapat bermanfaat bagi kita semua.

Malang, Oktober 2005

Penyusun

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BAB I

1.1 LATAR BELAKANG

Dalam penggunaan dan pemanfaatan teknologi dibidang elektronika peranan elektronika cukup besar dan mendominasi kemajuan yang ada , salah satunya adalah penggunaan sistem elektronika pada kebersihan lingkungan.

Sistem elektonika pada kebersihan lingkungan banyak digunakan diantaranya pengaturan pergerakan pembersih . Pengaturan pergerakan alat pembersih disini tergantung dari panjang dan lebar area yang akan di bersihkan , sehingga berkurangnya penggunaan tenaga manusia yang mempunyai banyak resiko .

Pada pengatur pergerakan pembersih yang biasa digunakan pada umumnya hanya secara manual sehingga banyak menggunakan tenaga manusia. Tetapi pada alat ini dapat menyesuaikan dengan kondisi yang telah ditentukan luas area yang akan dibersihkan.

Pada alat ini menggunakan inputan berupa frekuensi pulsa yang ditimbulkan dari photo transitor , serta keluaran berupa arus listrik yang digunakan menjalankan motor DC. Motor DC ini berfungsi sebagai penggerak alat pembersih. Jadi pada alat ini apabila kita memasukkan luas area yang diinginkan untuk dibersihkan maka secara otomatis alat akan berjalan sesuai yang dikehendaki

1.1 RUMUSAN MASALAH

Dalam perancangan dan pembuatan alat pembersih lantai dengan teknologi mikrokontroller ini dapat dirumuskan masalah sebagai berikut :

1. Bagaimana merancang pembuatan alat pembersih lantai dengan menggunakan IC AT89S51 dengan tepat serta bagaimana cara membuat alat ini bekerja berdasarkan kontrol-kontrol yang sesuai.
2. Bagaimana cara mengimplementasikan suatu sistem kontrol AT89S51 yang dapat mengendalikan suatu alat, sehingga alat alat yang dibuat dapat berfungsi dengan baik.
3. Bagaimana membuat perangkat lunak untuk mendukung kerja alat tersebut.

Sehubungan dengan rumusan masalah tersebut maka judul makalah skripsi tersebut adalah:

"PERANCANGAN DAN PEMBUATAN ALAT OTOMATIS PEMBERSIH PADA LANTAI DATAR MENGGUNAKAN TEKNOLOGI MIKROKONTROLER AT89S51"

1.2 TUJUAN

Tujuan yang ingin dicapai oleh penulis dari pembuatan dan penyusunan tugas akhir ini adalah :

1. Mempelajari implementasi sistem kontrol dengan menggunakan IC AT89S51
2. Mengaplikasikan sistem kontrol dengan menggunakan AT89S51 pada pembuatan alat pembersih yang dibuat sehingga dapat berfungsi sempurna.
3. Untuk memenuhi salah satu syarat kelulusan pada kurikulum program S-1 Teknik Elektronika ITN Malang.

1.3 BATASAN MASALAH

Dalam pembuatan laporan akhir ini diberikan batasan-batasan tertentu, supaya tidak terjadi penyimpangan dari maksud dan tujuan semula dari pembuatan laporan akhir ini.

Batasan batasan masalah tersebut antara lain :

1. Pembahasan hanya pada penunjang alat yang bisa secara otomatis dapat membersihkan sesuai dengan luas area yang ditentukan.
2. Luas area maksimal yang bisa dibersihkan kurang dari 9m x 9m
3. Luas area mininum yang bisa dibersihkan lebih dari 1m x 1m
4. Area yang dibersihkan merupakan area bebas hambatan dari benda apapun.
5. Adapun hal-hal diluar lingkup batasan masalah ini tidak dibahas dalam tugas akhir ini.

1.4 METODOLOGI

Adapun metodologi yang dipakai dalam perencanaan pembuatan alat ini meliputi :

1. Study leteratur

   Dengan mencari referensi-referensi yang berhubungan dengan perencanaan dan pembuatan alat, terutama referensi yang berhubungan dengan kontrol dan sensor.
2. Field Research

   Dari hasil percobaan data berdasarkan kondisi dan keadaan yang sesungguhnya dilapangan, yang merupakan data primer sebagai pembuktian kebenaran dari data sekunder hasil study literature.

1.6 . SISTEMATIKA PENULISAN

Penulisan Tugas Akhir dibagi menjadi lima bab :

BAB I : PENDAHULUAN

Meliputi beberapa uraian tentang latar belakang permasalahan, rumusan masalah, tujuan, batasan masalah, metodologi pembahasan, dan sistematika penulisan.

BAB II : LANDASAN TEORI

Membahas dasar-dasar teori penunjang dan pendukung, antara lain mengenai Mikrokontoller AT89S51 dan komponen yang bersangkutan dengan masalah yang dibahas.

BAB III : PERENCANAAN DAN PEMBUATAN ALAT

Membahas tentang perencanaan alat, uraian dasar perencanaan secara elektronik, dan membahas tentang program pembuatan.

BAB IV : PENGUJIAN ALAT

Membahas mengenai uji coba sistem, pengamatan, pengukuran dan analisa, serta kemungkinan pengembangan dari sistem yang telah dibuat.

BAB V : KESIMPULAN DAN SARAN

Merupakan bagian penutup yang berisi kesimpulan dan saran yang bermanfaat bagi pengembangan lebih lanjut.

BAB II

LANDASAN TEORI

2.1. Mikrokontroller AT89S51

2.1.1. Pendahuluan

Mikrokontroller bisa dipandang sebagai sebuah mini komputer yang terintegrasi dalam sebuah chip. Didalam satu chip mikrokontroller sudah terdapat bagian-bagian seperti dalam sebuah komputer. Bagian-bagian itu antara lain ; ALU (*Arithmetic Logic Unit*), PC (*Program Counter*), SP (*Stack Pointer*), Register, ROM (*Read Only Memory*), RAM (*Random Acces Memory*), Paralel I/O, Serial I/O, *Counter* dan sebuah rangkaian *Clock*.

Seperti sebuah mikroprosessor, mikrokontroller adalah sebuah perangkat serbaguna, yang fungsi kerjanya dapat ditentukan melalui sebuah perangkat lunak yang mendeskripsikan sebuah sistem yang diinginkan.

Pada saat ini terdapat banyak keluarga mikrokontroller salah satunya adalah keluarga MCS51. Salah satu tipe mikrokontroller yang termasuk dalam keluarga MCS51 adalah AT89S51 buatan Atmel.

AT89S51 adalah mikrokontroler keluaran atmel dengan 4K byte Flash PEROM (*Programmable and Erasable Read Only Memory*), AT89S51 merupakan memori dengan teknologi nonvolatile memori, artinya isi memori tersebut dapat diisi ulang ataupun dihapus berulang kali.

Memori ini biasa digunakan untuk menyimpan instruksi (Perintah) berstandar MCS – 51 code sehingga memungkinkan mikrokontroler ini untuk bekerja dalam mode *Single Chip Operation* (Mode Operasi Keping Tunggal) yang

Sumber : Perancangan Alat

IC ATMEL AT89S51 menyediakan standart berikut:

⇒ 4K Bytes memori yang dapat diprogram ulang

⇒ 128 Bytes internal RAM

⇒ 32 jalur I/O (Input dan Output) yang dapat diprogram

⇒ Sepasang 16 bit Timer dan Counter

⇒ Dual data Pointer (DPTR)

⇒ Watchdog Timer

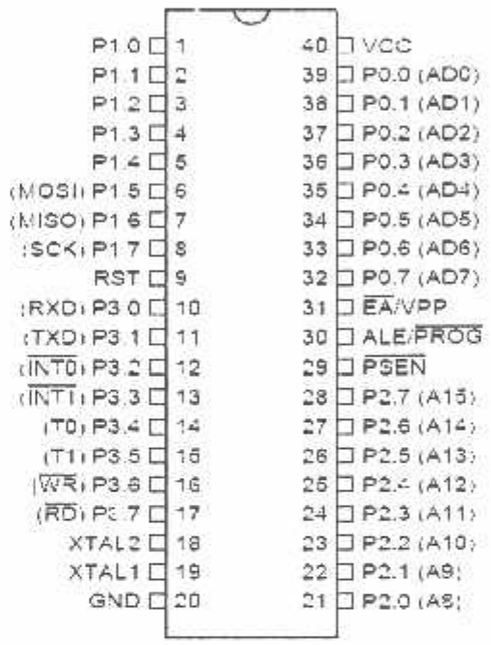
⇒ ISP Port

⇒ Mendukung serial Port secara penuh

⇒ Waktu Pemrograman yang singkat

Sebagai tambahan AT89S51 dirancang menggunakan logika yang statis untuk mode pengoperasian yang menuju ke frekwensi dasar dan pendukungan terhadap dua Software, serta dapat memilih model Power Savingnya. Mode idle akan berhenti ketika CPU sedang menjalankan RAM, Timer/Counter, Serial Port dan Interrupt System untuk terus melanjutkan fungsinya. Model power down akan menyimpan isi dari RAM tapi akan memberhentikan ossilator dan akan menghentikan semua chip lain yang sedang berfungsi sampai terdapat adanya gangguan dari luar atau hardware di reset.

Untuk konfigurasi pari pin-pin kaki IC AT89S51 dapat dilihat pada gambar 2.2



Gambar 2.2 Pin – Pin AT89S51

Sumber : perancangan Alat

2.1.3. Pin Deskripsi

VCC : Power Supply

GND : Ground

Port 0 : Port 0 berfungsi sebagai 8 bit I/O bertipe *open drain bi-directional.* Sebagai port keluaran masing – masing pin dapat menyerap arus sebesar 8 masukan TTL (sekitar 3,8 mA). Ketika diberikan logika '1' pada pin port 0 ini maka pin – pin port 0 ini akan dapat digunakan sebagai inputan berimpedansi tinggi. Port 0 juga dapat dikonfigurasikan pada sebagai bus alamat/data selama proses pengaksesan data memori dan program eksternal. Jika digunakan dalam mode ini port 0 memiliki internal Pull Up.

Port 0 juga menerima kode – kode data yang diberkan padanya selama proses pemrograman dan memberikan kode – kode selama proses verifikasi program yang telah tersimpan didalam memori. Dalam hal ini dibutuhkan eksternal Pull Up selama proses verifikasi program.

Port 1 : Port 1 berfungsi sebagai 8 bit I/O Bi-directional yang dilengkapi dengan internal Pull Up. Ketika diberikan logika '1' pin ini akan di Pull Up secara internal sehingga dapat digunakan sebagai input. Sebagai inputan jika pin – pin ini dihubungkan ke ground maka masing – masing pin ini dapat menghantarkan arus karena di Pull High secara internal. Port 1 juga menerima *Low Order Address Bytes* selama melakukan verifikasi program.

Pada port 1 di AT89S51 pin ini mempunyai alternatif seperti pada tabel 2.1

Tabel 2-1 Fungsi – Fungsi Alternative Port 1

Port Pin	Alternate Funtions
P1.5	MOSI (Master Output Slave Input)
P1.6	MISO (Master Input Slave Output)
P1.7	SCK (Serial Clock)

Port 2 : Port 2 berfungsi sebagai 8 bit I/O Bi-directional yang dilengkapi dengan internal Pull Up Penyangga keluaran port 2 dapat memberikan atau menyerap arus empat masukan TTL (sekitar 1,6 mA)

Jika diberikan logika '1' pada pin – pin port 2, maka masing – masing pin akan di Pull High secara internal sehingga dapat digunakan sebagai inputan. Sebagai inputan jika pin – pin port 2 dihubungkan ke ground (di Pull Low), maka , masing – masing pin dapat menghantarkan arus karena di Pull High secara internal.

Port 2 akan memberikan byte alamat bagian tinggi (High Byte) selama pengambilan instruksi dari memori program eksternal dan selama pengaksesan memori data eksternal yang menggunakan perintah dengan alamat 16 bit (misalkan **MOVX@DPTR**). Dalam aplikasi ini , jika ingin mengirimkan '1', maka digunakan Pull Up internal yang sudah disediakan. Selama pengaksesan memori data eksternal yang menggunaka perintah 8 bit (misalkan **MOVX@RI**), port 2 akan

mengirimkan isi dari SFR P2 (*Special Function Register Port 2*). Port 2 juga menerima alamat bagian tinggi (High Order Address) selama pemrograman dan verifikasi memori.

Port 3 : Port 3 sebagai 8 bit I/O Bi-directional yang dilengkapi dengan Pull Up Internal. Penyangga keluaran port 3 daqpat memberkan atau menyerap arus empat masukan TTL (sekitar 1,6 mA).

Jika diberikan logika '1' pada pin pin port 3, maka masing – masing pin akan di Pull High oleh Pull Up internal sehingga dapat digunakan sebagai inputan. Sebagai inputan, jika pin – pin port 3 dihubungkan ke ground, maka masing – masing kaki akan memberikan arus karena di Pull High secara internal.

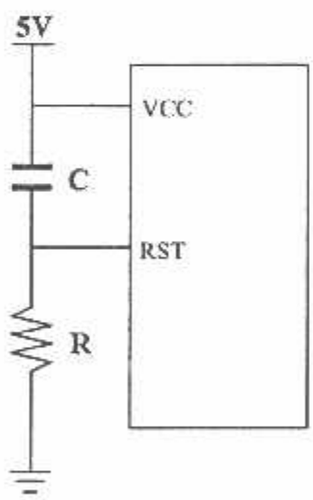
Seperti Port 1, port 3 juga mempunyai fungsi – fungsi alternatif yang diberikan oleh AT89S51 seperti pada tabel 2-2

Tabel 2-2 Fungsi – Fungsi Alternatif Port 3

Port Pin	Fungsi Alternatif
P3.0	RXD (Serial Input Port)
P3.1	TXD (Serial Output Port)
P3.2	INT0 (Eksternal Interrupt 0)
P3.3	INT1 (Eksternal Interrupt 1)
P3.4	T0 (Timer 0 Eksternal Input)
P3.5	T1 (Timer 1 Eksternal Input)

P3.6	WR (Eksternal Data Memory Write Strobe)
P3.7	RD (Eksternal Data Memory Read Strobe)

Reset : Inputan Reset akan memberikan logika High '1' pada pin ini dengan jangka waktu yang ditentukan oleh lamanya pengosongan data muatan kapasitor. Jangka waktu minimal adalah 2 siklus mesin (24 periode frekwensi clock) ditambah waktu start On Osilator. Dan gambar rangkaian power on reset dapat dilihat pada gambar 2.3



Gambar 2.3 Rangkaian Power On Reset

Sumber : Perancangan Alat

ALE/$\overline{\text{PROG}}$: Keluaran ALE (*Address Latch Enable*) menghasilkan pulsa – pulsa untuk menutup byte rendah (*Low Byte*) alamat selama mengakses memori eksternal. Pin ini juga berfungsi sebagai inputan pulsa program (*The Program Pulse Input*) atau PROG selama melakukan Flash Program. Pada operasi normal, ALE akan berpulsa dengan laju 1/6 dari frekwensi kristal dan dapat digunakan sebagai pewaktuan (*Timing*) atau pendetakan (*Clocking*) rangkaian eksternal. Sebagai catatan ada sebuah pulsa yang dilewati selama pengaksesan memori data eksternal. Jika dikehendaki operasi ALE dapat di nonaktifkan dengan cara mengatur bit 0 dari SFR (*Special Function Register*) lokasi 8Eh. Jika diberi logika '1' ALE hanya akan aktif selama menemui instruksi **MOVX** atau **MOVC**. Selain itu, pin ini secara perlahan akan di Pull High. Mematikan bit ALE tidak akan ada efeknya jika mikrokontroller mengeksekusi program secara eksternal.

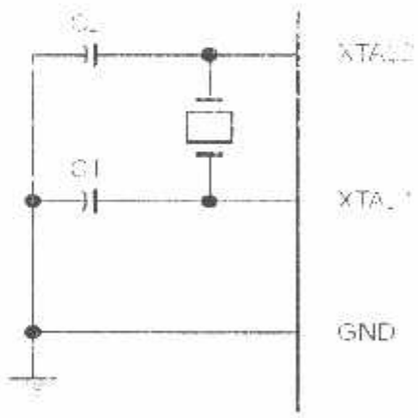
$\overline{\text{PSEN}}$: $\overline{\text{PSEN}}$ (*Program Store Enable*) merupakan sinyal baca untuk memori program eksternal. Ketika mikrokontroller AT89S51 menjalankan kode dari program eksternal, $\overline{\text{PSEN}}$ akan diaktifkan sebanyak 2 kali per siklusnya, kecuali dua aktivasi $\overline{\text{PSEN}}$ dilompati (Diabaikan) saat mengakses memori data eksternal.

$\overline{EA}$/VPP : $\overline{EA}$/VPP (*External Access Enable*). $\overline{EA}$ harus selalu dihubungkan ke Ground karena digunakan untuk mengakses eksternal memori dengan lokasi 0000H sampai FFFFH. Catatan sekalipun bit '1' sudah terkunci dan terprogram, maka EA akan terkunci pada reset. **EA** juga harus dihubungkan ke **Vcc** untuk melakukan menjalankan program secara internal. Pada saat Flash Programming pin ini mendapatkan tegangan sebesar 12 Volt.

XTAL1 : Merupakan input ke penguat pembalik osilator dan ke rangkaian operasi Clock internal.

XTAL2 : Keluaran dari penguat pembalik osilator.

Dan gambar rangkaian cristal dapat dilihat pada gambar 2.4



Gambar 2.4 Rangkaian Cristal

Sumber : Perancangan Alat

Mikrokontroler AT89S51 memiliki rangkaian osilator internal dengan mengacu pada frekwensi referensi pada pin XTAL1 dan XTAL2.

Waetlidog Timer (WDT)

Fungsi dari WDT sebenarnya adalah untuk melakukan peresetan secara otomatis. Dimana dia akan me – reset mikrokontroler jika mikrokontroler hang. Oleh sebab itu user harus selalu me – reset WDT sebelum WDT mereset mikrokontroler jika WDT tidak direset oleh mikrokontroler dalam jangka waktu yang telah ditentukan maka secara otomatis WDT – lah yang akan mereset mikrokontroler. WDT terdiri dari suatu 14-bit counter dan Watchdog Timer Reset (WDTRST) SFR. WDT diset default untuk menonaktifkan reset yang ada. Tidak ada jalan lain untuk menonaktifkan WDT kecuali melalui Reset (baik Hardware reset atau WDT Overflow reset). Jika WDT Overflow, itu akan membuat suatu keluaran Reset High di pin RST.

Untuk mengaktifkannya user harus menulis 01EH dan 0E1H di dalam daftar urutan WDTRST (alamat SFR-nya 0A6H). Ketika WDT aktif, pemakai harus mengisinya dengan menuliskan 01EH dan 0E1H ke WDTRST untuk menghindari suatu WDT Overflow. 14-Bit Counter akan Overflow jika mencapai angka 16383 (3FFFH), dan ini akan me – reset mikrokontroler. Disaat WDT aktif, dia akan menaikan tiap-tiap siklus mesin ketika osilator sedang menjalankannya. Dan ini artinya

pemakai harus mereset WDT sedikitnya tiap-tiap 16383 (3FFFH) siklus mesin. Untuk me-reset WDT pemakai harus menulis 01EH dan 0E1H ke WDTRST, WDTRST adalah suatu write-only register. WDT counter tidak bisa dibaca atau ditulis. Ketika WDT Overflow, itu akan menghasilkan suatu keluaran RESET di pin RST. Jangka waktu Reset adalah 98xTOSC, dimana TOSC = 1/FOSC. Untuk membuat penggunaan terbaik dari WDT adalah user harus mengisikan bagian dari kode – kode itu yang akan mereset WDT sebelum WDT mereset Mikrokontroler.

Dual DPTR (Data Pointer Register)

DPTR sebenarnya digunakan untuk melakukan transaksi dengan memori eksternal. Ini dikarenakan dalam keluarga MCS – 51 tidak dapat melakukan pemindahan data secara langsung dari RAM Internal dengan memori Eksternal. Pemindahan data semacam ini memerlukan DPTR untuk memberitahukan dimana alamat tepatnya data akan dipindahkan dari RAM Internal atau dari RAM Internal ke Memori Eksternal. Perbedaan antara AT89S51 dengan AT89S51 adalah bahwa AT89S51 diberikan Dual DPTR sedangkan di AT89S51 hanya sebuah, jadi untuk pengaksesan dari RAM Internal atau sebaliknya akan lebih cepat jika menggunaka AT89S51.

2.2. Ram Internal

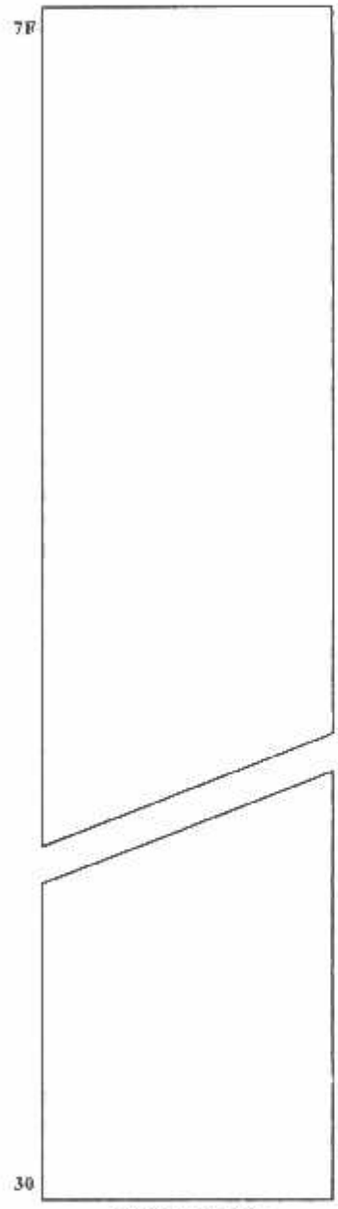
Untuk gambar ilustrasi pembagian ruang RAM AT89S51 dapat dilihat pada gambar 2.5

BANK3	1F	R7
	1E	R6
	1	R5
	1	R4
	1B	R3
	1	R2
	19	R1
	18	R0
BANK2	17	R7
	16	R6
	15	R5
	14	R4
	13	R3
	12	R2
	11	R1
	10	R0
BANK1	0F	R7
	0E	R6
	0	R5
	0	R4
	0B	R3
	0	R2
	09	R1
	08	R0
BANK0	07	R7
	06	R6
	05	R5
	04	R4
	03	R3
	02	R2
	01	R1
	00	R0

Working Register

2F	7F
2E	77
2	6F
2	67
2B	5F
2	57
29	4F
28	47
27	3F
26	37
25	2F
24	27
23	1F
22	17
21	0F
20	07

Bit Adressable



RGeneral Purpose

Gambar 2.5 Ilustrasi Pembagian Ruang RAM AT89S51

Sumber : Perancangan Alat

⇒ RAM Internal, memori sebesar 128 byte yang biasanya digunakan untuk menyimpan variabel atau data yang bersifat sementara atau data akan hilang saat catu daya dimatikan.

⇒ *Special Function Register* (Register Fungsi Khusus), memori yang berisi register – register yang mempunyai fungsi – fungsi khusus yang disediakan oleh mikrokontroler tersebut, seperti timer, serial dan lain – lain.

⇒ *Flash PEROM*, memori yang digunakan untuk menyimpan instruksi – instruksi MCS – 51.

AT89S51 mempunyai struktur memori yang terpisah antara RAM Internal dan Flash PEROM – nya. RAM Internal dialamati oleh RAM *Address Register* (Register Alamat RAM) sedangkan Flash PEROM yang menyimpan perintah – perintah MCS – 51 dialamati oleh *Program Address Register* (Register Alamat Program). Dengan adanya struktur memori yang terpisah tersebut, walaupun RAM Internal dan Flash PEROM, mempunyai alamat awal yang sama, yaitu 00, namun secara fisik kedua memori tersebut tidak saling berhubungan.

RAM Internal terdiri atas:

⇒ Register BANKS

8951 mempunyai delapan buah register yang terdiri atas R0 hingga R7. Kedelapan buah register ini selalu terletak pada alamat 00H hingga 07H pada setiap kali sistem direset. Namun, posisi R0 hingga R7 dapat dipindah ke BANK 1 (08 hingga 0FH), BANK 2 (10H hingga 17H), atau BANK 3 (18H hingga 1FH) dengan mengatur bit RS0 dan RS1.

⇒ Bit Addressable RAM

RAM pada alamat 20H hingga 2FH dapat diakses secara pengalamatan bit (*Bit Addressable*) sehingga hanya dengan sebuah instruksi saja setiap bit dalam area ini dapat diset, clear, AND dan OR. Sebagai contoh, pada saat terjadi instruksi Setb 67H, hal ini sama dengan menset bit MSB dari alamat 2C yaitu:

```
MOV     A,2CH          ; Pindahkan data dari alamat 2CH ke Acc
A
Orl     A,#10000000B   ; Set MSB Acc A
```

terjadi instruksi Setb 67H, hal ini sama dengan menset bit MSB dari alamat 2C yaitu:

Dengan adanya sistem bit addressable RAM, proses yang seharusnya dijalankan dengan tiga cycle seperti listing diatas dapat digantikan dengan sebuah instruksi yang hanya membutuhkan satu instruksi saja.

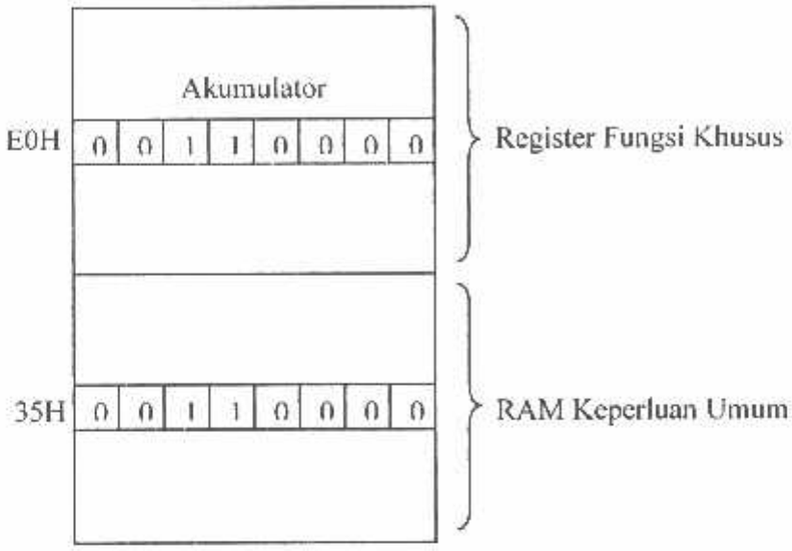
Dalam aplikasinya, lokasi yang dapat diakses dengan pengalamatan bit ini dapat juga digunakan untuk menandai suatu lokasi bit tertentu baik berupa Register Fungsi Khusus yang dapat dialamati secara bit (termasuk Register I/O) ataupun lokasi – lokasi tertentu yang dapat dialamati secara bit.

⇒ RAM Keperluan Umum

RAM keperluan umum dapat dimulai dari alamat 30H hingga 7FH dan dapat diakses dengan pengalamatan langsung maupun tak langsung. Pengalamatan langsung dilakukan ketika salah satu operand merupakan bilangan yang menunjukan lokasi yang dialamati seperti pada contoh gambar 2-6

MOV A,35H ; Baca data dari alamat 35H dan disimpan di Accumulator.

Alamat yang
ditunjuk langsung



Gambar 2.6 Pengalamatan Secara Langsung

Sumber : Perancangan Alat

Sedangkan pengalamatan secara tak langsung pada lokasi dari RAM Internal ini adalah akses dari data memori ketika alamat memori tersebut tersimpan dalam suatu register R0 atau R1. R0 dan R1 adalah dua buah register pada mikrokontroler berarsitertur MCS – 51 yang dapat digunakan sebagai pointer dari sebuah lokasi memori pada RAM Internal.

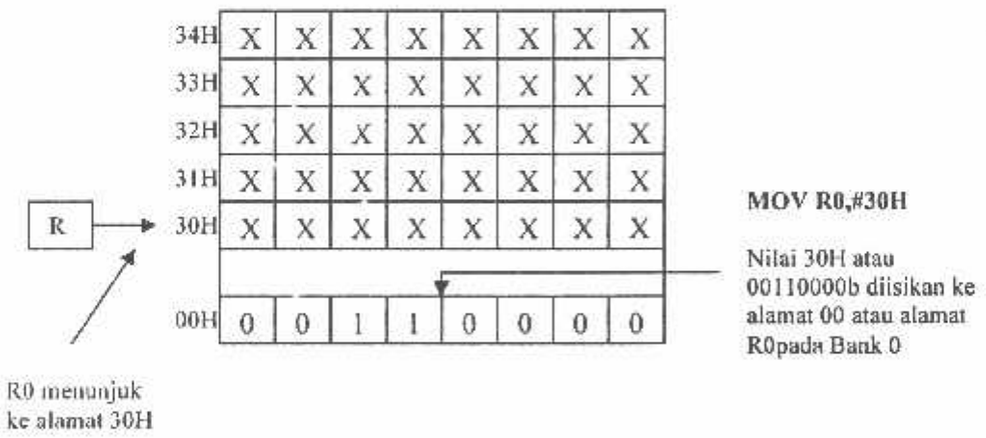
Sebagai Contoh:

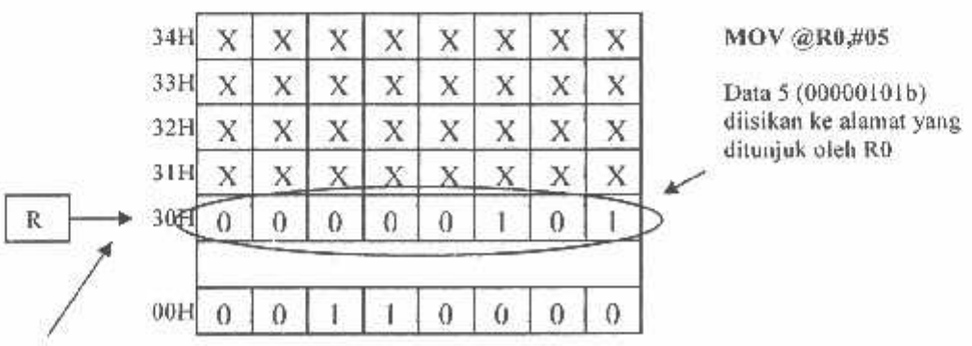
```
MOV  R0,#35H      ; R0 diisi dengan data 35H
MOV  A,@R0        ; Baca data di alamat yang dijuntuk oleh R0
```

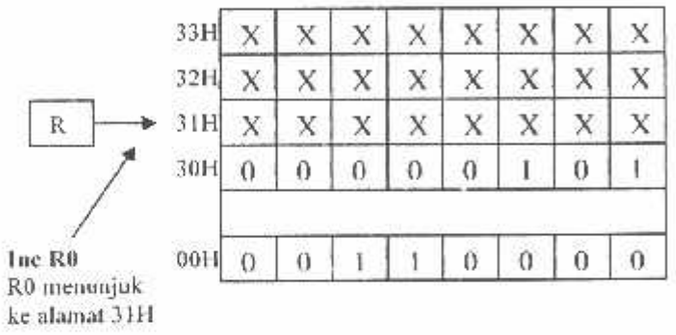
Pengalamatan secara tak langsung biasa digunakan untuk mengakses beberapa lokasi memori dengan letak yang beraturan seperti pada contoh berikut:

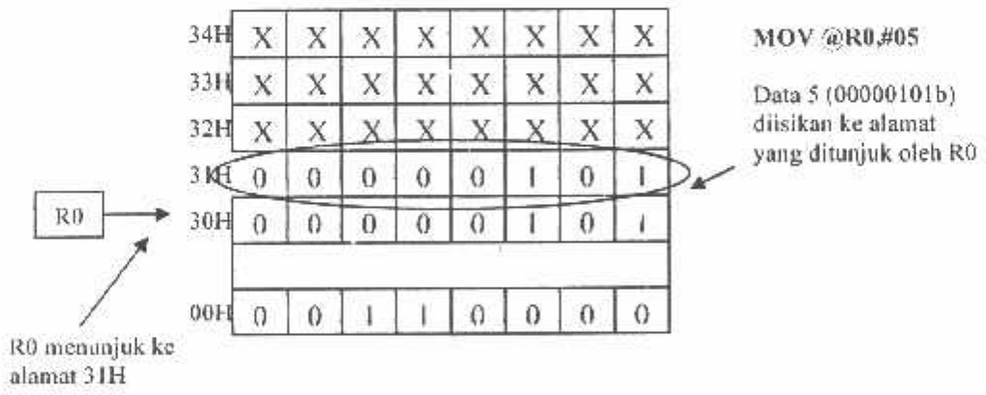
```
MOV      R0,#30H     ; R0 diisi dengan data 30H
Loop:
MOV      @R0,#05     ; Data 5 diisikan ke alamat yang
ditunjuk
                     ; oleh R0

Inc      R0          ; R0 menunjuk ke alamat selanjutnya
```

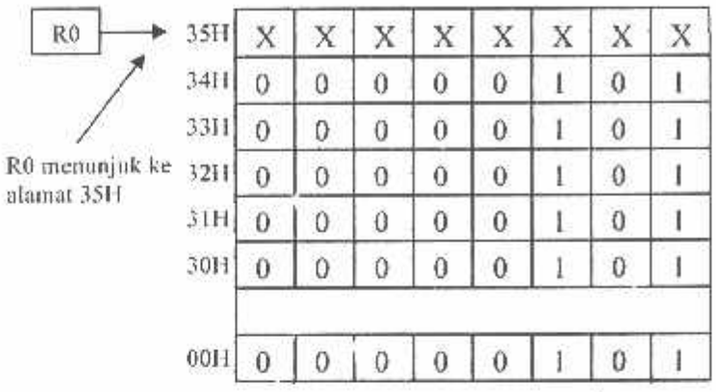
Pada gambar 2.4 yang merupakan step – step proses yang terjadi pada contoh program di atas, proses pemindahan data 5 ke alamat – alamat yang ditunjuk oleh R0 dilakukan berulang – ulang hingga R0, register yang berfungsi penyimpan nilai dari alamat yang diakses atau sebagai *pointer* (penunjuk) alamat yang diakses mencapai 35H, seperti pada gambar 2-7






33H X X X X X X X X
32H X X X X X X X X
R
31H X X X X X X X X
30H 0 0 0 0 0 1 0 1
00H 0 0 1 1 0 0 0 0
Inc R0
R0 menunjuk
ke alamat 31H


34H X X X X X X X X
33H X X X X X X X X
32H X X X X X X X X
31H 0 0 0 0 0 1 0 1
R0
30H 0 0 0 0 0 1 0 1
00H 0 0 1 1 0 0 0 0
MOV @R0,#05
Data 5 (00000101b)
diisikan ke alamat
yang ditunjuk oleh R0
R0 menunjuk ke
alamat 31H



Gambar 2.7 Step – Step Yang Terjadi Pada Pemindahan Data 5 ke Alamat 30H hingga 34H

Sumber : Perancangan Alat

Langkah kerjanya: Pertama R0 diisi dengan data 30H sehingga register ini menunjuk ke alamat 30H dari RAM Internal. Kemudian data 5 diisikan alamat yang ditunjukkan oleh R0 sehingga alamat 30H (alamat yang ditunjuk oleh R0 saat itu) akan berisi data 5. Perintah Inc R0 menyebabkan nilai dalam R0 bertambah 1 menjadi 31H sehingga register ini menunjuk ke alamat 31H. Oleh karena R0 belum mencapai 35H (Cjne R0,#05). Demikian berlangsung seterusnya hingga pada saat R0 menunjuk ke alamat 35H proses pemindahan data 5 tersebut tidak dilakukanlagi sehingga alamat 30H hingga 34H terisi dengan data 5.

2.2.1. Register Fungsi Khusus

89S51 mempunyai 21 ***Special Function Registers*** (Register Fungsi Khusus) yang terletak pada antara alamat 80H hingga FFH. Beberapa dari register – register ini juga bisa dialamati dengan pengalamatan bit sehingga dapat dioperasikan seperti yang ada pada RAM yang lokasinya dapat dialamati dengan pengalamatan bit.

⇒ Accumulator

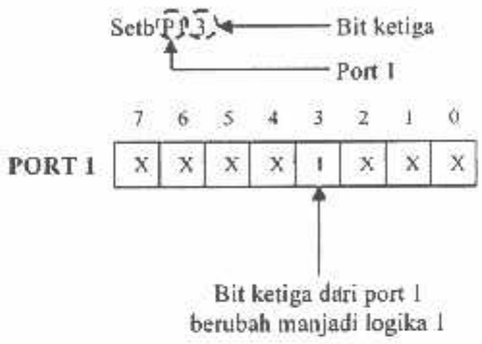
Register ini terletak pada alamat E0H. Hampir semua operasi aritmatik dan operasi logika selalu menggunakan register ini. Untuk proses pengambilan dan pengiriman data ke memori eksternal juga diperlukan register ini.

⇒ Port

89S51 mempunyai empat buah Port, yaitu Port 0, Port 1, Port 2 dan Port 3 yang terletak pada alamat 80H, 90H, A0H dan B0H. Namun, jika digunakan eksternal memoriataupun fungsi – fungsi special, seperti Eksternal Interrupt, Serial ataupun Eksternal Timer, Port 0, Port 2 dan Port 3 tidak dapat digunakan sebagai Port dengan fungsi umum. Untuk itu Port 1 yang dikhususkan untuk port dengan fungsi umum.

Semua Port ini dapat diakses dengan pengalamatan secara bit sehingga dapat dilakukan perubahan output pada tiap – tiap pin dari port ini tanpa mempengaruhi port – port yang lainnya.

Sebagai contoh, jika dilakukan instruksi Setb P1.3, maka bit ketiga dari port 1 akan berkondisi high (5V) tanpa mempengaruhi bit – bit yang lain pada port ini. Seperti yang dapat dilihat pada gambar 2-8



Gambar 2.8 Bit – Bit Port

Sumber : Perancangan Alat

Seperti yang tampak pada gambar 2.7, bit ketiga dari port 1 terletak pada alamat 93H oleh karena itu instruksi Setb P1.3 dapat diganti dengan instruksi Setb 93H.

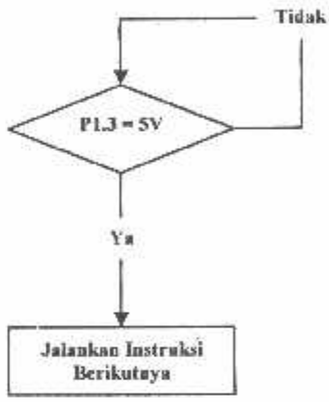
Port ini digunakan untuk menunggu sinyal yang dikirim oleh komponen lain yang merupakan sinyal positif (5V) misalnya, dengan instruksi

```
Tunggu:
        Jnb     P1.3, tunggu
```

Selama kondisi pada port 1 pin ketiga masih low (0V), program akan terus melompat ke alamat yang ditunjukkan oleh label "tunggu" sehingga dapat diartikan bahwa program berhenti di alamat tersebut hingga terjadi sinyal

positif (5V). Setelah sinyal positif (5V) muncul di bit ketiga dari port 1; program akan menuju ke alamat yang berikutnya.

Dan gambar diagram alir deteksi bit ketiga port 1 dapat dilihat pada gambar 2.9



Gambar 2.9 Diagram Alir Deteksi Bit Ketiga Port 1
Sumbewr : Perancangan Alat

⇒ PSW (*Program Status Word*)

Program status word atau PSW terletak pada alamat D0H yang terdiri atas beberapa bit sebagai berikut:

PSW	PSW.7	PSW.6	PSW.5	PSW.4	PSW.3	PSW.2	PSW.1	PSW.0
D0H	CY	AC	F0	RS1	RS0	OV	-	P

- Flag Carry

Flag Carry (terletak pada alamat D7H) mempunyai fungsi sebagai pendeteksi terjadinya kelebihan pada operasi penjumlahan atau terjadi

pinjam (*borrow*) pada operasi pengurangan. Misalnya jika data pada accumulator adalah FFH dan dijumlahkan dengan bilangan satu atau lebih, akan terjadi kelebihan dan membuat carry menjadi Set, sedangkan jika data pada accumulator adalah 00H dan dikurangkan dengan bilanagan satu atau lebih, akan terjadi pemimjaman dan membuat carry juga menjadi set.

- Flag Auxilary Carry

  Flag Auxilary Carry akan selalu Set pada saat proses penjumlahan terjadi carry dari bit ketiga hingga bit keempat.

- Flag 0

  Flag 0 digunakan untuk tujuan umum bergantung pada kebutuhan pemakai.

- Bit Pemilih Register Bank

  Register Bank Select Bits (RS0 dan RS1) atau Bit Pemilih Register Bank digunakan untuk menentukan lokasi dari Register Bank (R0 hingga R7) pada memori. RS0 dan RS1 selalu bernilai nol setiap kali system diresct sehingga lokasi dari R0 hingga R7 akan berada di alamat 00H hingga 07H.

- Flag Overflow

  Flag Overflow akan diset jika pada operasi aritmatik menghasilkan bilangan yang lebih besar dari pada 128 atau lebih kecil dari – 128.

Contoh:

```
MOV     A,#80h   ; A = 128
Add     A,#10H   ; A = 128 + 16, A = 144 ATAU 90H
```

Hasil dari operasi aritmatikdi atas adalah lebih besar dari 128, yaitu 144 atau 90H maka bit Overflow akan Set.

- Bit Pariti

Bit Pariti akan diset jika jumlah bit 1 dalam accumulator adalah ganjil dan akan clear jika jumlah bit 1 dalam accumulator genap. Jika data dalam accumulator adalah 10101110b atau AEH pariti akan diset. Data AEH mempunyai lima bit yang berkondisi 1 atau dapat disebut mempunyai bit 1 dalam jumlah yang ganjil. Bit pariti ini digunakan untuk proses yang berhubungan dengan serial port yaitu sebagai *Check sum*.

⇒ Register B

Register B digunakan bersama accumulator untuk proses aritmatik selain dapat juga difungsikan sebagai register biasa. Register ini juga bersifat *Bit Addressable*.

⇒ Stack Pointer

Stack Pointer merupakan sebuah register 8 bit yang terletak di alamat 81H. Isi dari Stack Pointer ini merupakan alamat dari data yang disimpan di stack. Stack Pointer dapat diedit atau dibiarkan saja mengikuti standart sesudah terjadi reset. Jika Stack Pointer diisi data 5FH, area untuk proses penyimpanan dan pengambilan data dari dan

ke stack adalah sebesar 32 byte, yaitu antara 60H hingga 7FH karena 89S51 mempunyai Internal RAM sebesar 128 byte.

⇒ Data Pointer Two Byte Register (DPTR)

Data Pointer Two Byte Register atau DPTR merupakan register 16 bit dan terletak pada alamat 82H untuk DPL (Data Pointer Low) dan 83H untuk DPH (Data Pointer High). DPTR biasa digunakan untuk mengakses source code ataupun data yang terletak di memori eksternal.

Contoh:

```
MOV     A, #01h
MOV     DPTR, #2000H
MOVX    @Dptr,A
```

2000H. Pertama, data 01H diisikan ke accumulator. Kemudian, DPTR yang berfungsi untuk menunjukan alamat penyimpanan data diisi dengan 2000H. terakhir, isi dari accumulator A disimpan ke lokasi memori yang ditunjukan oleh DPTR (*Indirect Addressing*).

⇒ Register Timer

AT89S51 mempunyai dua buah 16 bit Timer/Counter, yaitu Timer 0 dan Timer 1. Timer 0 terletak pada alamat 8AH untuk TL0 dan 8CH untuk TH0 dan Timer 1 terletak pada alamat 8BH untuk TL1 dan 8DH untuk TH1.

⇒ Register Port Serial

AT89S51 mempunyai sebuah *on chip serial port* (serial port dalam keping) yang dapat digunakan untuk berkomunikasi dengan peralatan

lain yang menggunakan serial port juga seperti modem, shift register dan lain – lain.

Buffer (Penyangga) untuk proses pengiriman maupun pengambilan data terletak pada register SBUF, yaitu pada alamat 99H. Sedangkan untuk mengatur mode serial dapat dilakukan dengan mengubah isi dari SCON yang terletak pada alamat 98H.

⇒ Register Interupt

89S51 mempunyai lima buah interupsi dengan sua level prioritas interupsi. Interupsi akan selalu nonaktif setiap kali system di – reset. Register – register yang berhubungan dengan interrupt adalah *Interrupt Enable Register* (IE) atau Register Pengaktif Interupsi pada alamat A8H untuk mengatur keaktifan tiap – tiap interrupt dan Interrupt Priority Register (IP) atau Register Prioritas Interupsi pada alamat B8H.

⇒ Register Kontrol Power

Register ini terdiri atas SMOD yang digunakan untuk melipat dua baud rate dari port serial, dua buah bit untuk flag fungsi umum pada bit ketiga dan bit kedua, power Down (PD) bit dan idle (IDL) bit.

Pada mode idle hubungan antara CPU dan internal clock terputus, namun kondisi port tetap pada kondisi terakhir, ALE dan PSEN menjadi high, timermasih tetap bekerja. Mode idle berakhir pada saat terjadi interupsi, reset atau kondisi – kondisi lain yang mereset IDL bit.

Pada Mode Power Down oscillator dan semua fungsi berhenti, RAM tetap pada kondisi terakhir, begitupula dengan port dan ALE maupun PSEN akan berkondisi 0. Mode Power Down berakhir pada saat terjadi reset.

⇒ Time Counter Control (TCON)

TCON merupakan suatu register yang berisi bit – bit untuk memulai atau menghentikan pencacah/pewaktu.

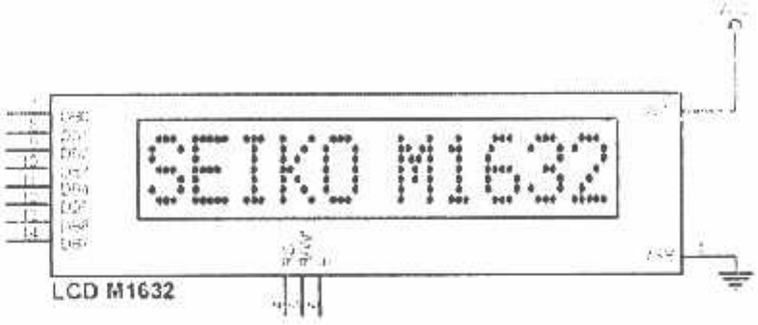
⇒ Serial Control Buffer (SBUFF)

Register ini digunakan untuk menampung data masukan (SBUFF IN) ataupun keluaran (SBUFF OUT) dari serial port.

2.3. LCD (Liquid Crystal Display)

LCD *Display Module* M1632 buatan *Seiko Instrument Inc.* terdiri dari dua bagian, yang pertama merupakan panel LCD sebagai media penampil informasi dalam bentuk huruf/angka dua baris, masing-masing baris bisa menampung 16 huruf/angka.

Bagian kedua merupakan sebuah sistem yang dibentuk dengan mikrokontroler yang ditempelkan dibalik panel LCD, berfungsi mengatur tampilan informasi serta berfungsi mengatur komunikasi M1632 dengan mikrokontroler yang memakai tampilan LCD itu. Dengan demikian pemakaian M1632 menjadi sederhana, sistem lain yang menggunakan M1632 cukup mengirimkan kode-kode ASCII dari informasi yang ditampilkan seperti layaknya memakai sebuah printer.untuk gambar LCD modul dapat dilihat pada gambar 2.10



Gambar 2-10 LCD Modul Seiko M1632

Sumber : *Datasheet* Seiko M1632

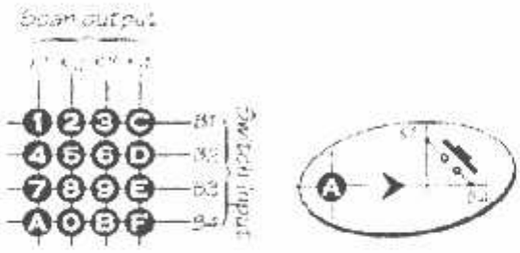
Untuk berhubungan dengan mikrokontroler pemakai, M1632 dilengkapi dengan 8 jalur data (DB0..DB7) yang dipakai untuk menyalurkan kode ASCII maupun perintah pengatur kerjanya M1632. Selain itu dilengkapi pula dengan E, R/W dan RS seperti layaknya komponen yang kompatibel dengan mikroprosesor. Kombinasi sinyal E dan R/W merupakan sinyal standard pada komponen buatan Motorola. Sebaliknya sinyal-sinyal dari kontroller merupakan sinyal khas Intel dengan kombinasi sinyal WR dan RD.

RS, singkatan dari *Register Select*, dipakai untuk membedakan jenis data yang dikirim ke M1632, kalau RS=0 data yang dikirim adalah perintah untuk mengatur kerja M1632, sebaliknya kalau RS=1 data yang dikirim adalah kode ASCII yang ditampilkan.

Demikian pula saat pengambilan data, saat RS=0 data yang diambil dari M1632 merupakan data status yang mewakili aktivitas M1632, dan saat RS=1 maka data yang diambil merupakan kode ASCII dari data yang ditampilkan.

2.4. Keypad

Matrik *keypad* 4x4 merupakan susunan 16 tombol membentuk *keypad* sebagai sarana *input* ke mikrokontroler, meskipun jumlah tombol ada 16 tapi hanya memerlukan 8 jalur port paralel, seperti terlihat dalam Gambar 2-11



Gambar 2-11 Matrik Keypad 4x4

Sumber : www.alds.stts.edu

Dalam gambar 2-11 masing-masing tombol menghubungkan sebuah jalur *output* (K1; K2; K3 atau K4) ke sebuah jalur *input* (B1; B2; B3 atau B4), seperti yang digambarkan secara rinci dalam bulatan bagian kanan gambar, tombol "A" menghubungkan jalur K1 ke jalur B4.

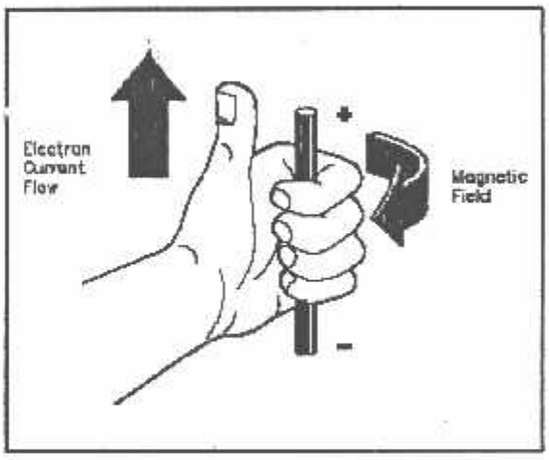
Semua tombol mekanis yang biasa dipakai untuk *keypad*, saat ditekan atau saat tekanan pada tombol dilepas akan bergetar selama lebih kurang 30 sampai 50 mili-detik, sifat ini akan mengakibatkan sub-rutin pembacaan *keypad* merasakan adanya penekanan tombol secara berulang-ulang, meskipun sesungguhnya tombol hanya ditekan sekali saja. Gejala ini biasanya disebut sebagai *bounce*.

Untuk mengatasi masalah ini, setelah berhasil membaca nilai tombol yang ditekan, kontroller dipaksa "istirahat" berapa saat sampai tombol tidak bergetar, sebelum membaca tombol berikutnya.

2.5. Pengendali Arah Putaran Motor DC

2.5.1. Teori Dasar Motor DC

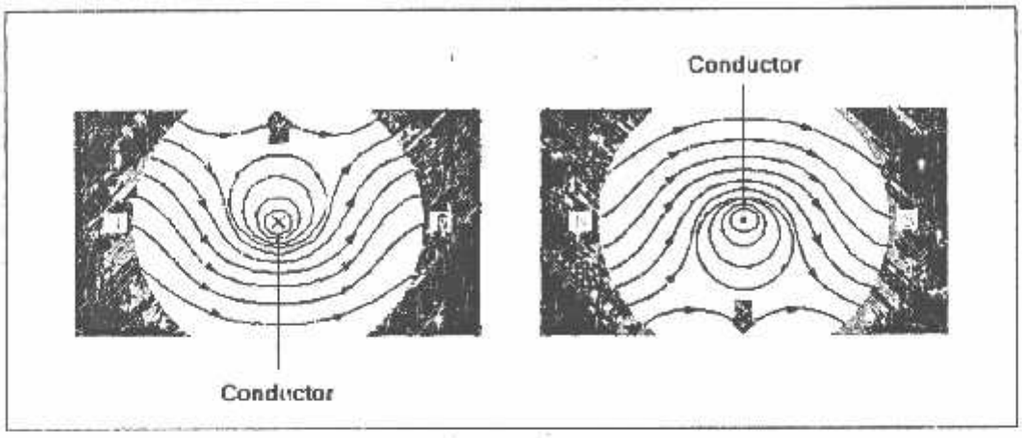
Setiap arus yang mengalir melalui sebuah konduktor akan menimbulkan medan magnet. Arah medan magnet dapat ditentukan dengan kaidah tangan kiri. Ibu jari tangan menunjukkan arah aliran arus listrik sedangkan jari-jari yang lain menunjukkan arah medan magnet yang timbul, seperti yang ditunjukkan oleh gambar 2-12



Gambar 2-12 Kaidah Tangan Kiri

Jika suatu konduktor yang dialiri arus listrik ditempatkan dalam sebuah medan magnet, kombinasi medan magnet akan ditunjukkan oleh gambar 2-13. Arah aliran arus listrik dalam konduktor ditunjukkan dengan tanda "x" atau ".". Tanda "x" menunjukkan arah arus listrik

mengalir menjauhi pembaca gambar, tanda "." menunjukkan arah arus listrik mengalir mendekati pembaca gambar. Seperti pada gambar 2-13



Gambar 2-13 Konduktor Berarus Listrik Dalam Medan Magnet

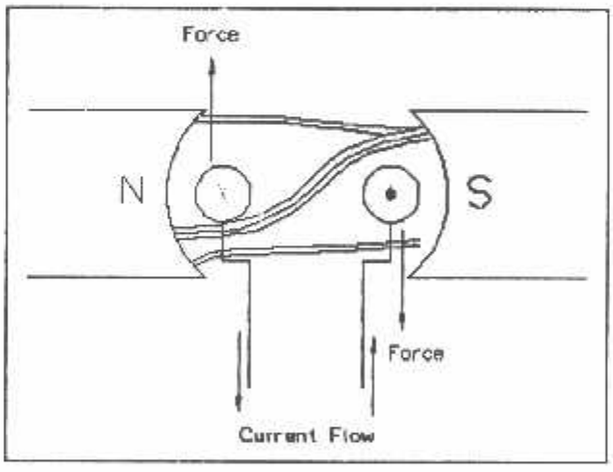
Pada gambar sebelah kiri, arah medan magnet pada sisi atas yang dihasilkan oleh konduktor berlawanan dengan arah medan magnet yang dihasilkan oleh magnet permanen. Sementara pada sisi sebelah bawah, arah medan magnet yang dihasilkan oleh konduktor searah dengan arah medan magnet yang dihasilkan oleh magnet permanen. Dengan kata lain, pada sisi sebelah atas kerapatan fluks magnet lebih sedikit dari pada sisi sebelah bawah. Sebuah gaya dorong akan menyebabkan konduktor bergerak ke sisi sebelah atas.

Pada gambar sebelah kanan, arah medan magnet pada sisi atas yang dihasilkan oleh konduktor searah dengan arah medan magnet yang dihasilkan oleh magnet permanen. Sementara pada sisi sebelah bawah, arah medan magnet yang dihasilkan oleh konduktor berlawanan dengan

arah medan magnet yang dihasilkan oleh magnet permanen. Dengan kata lain, pada sisi sebelah bawah kerapatan fluks magnet lebih sedikit dari pada sisi sebelah atas. Sebuah gaya dorong akan menyebabkan konduktor bergerak ke sisi sebelah bawah.

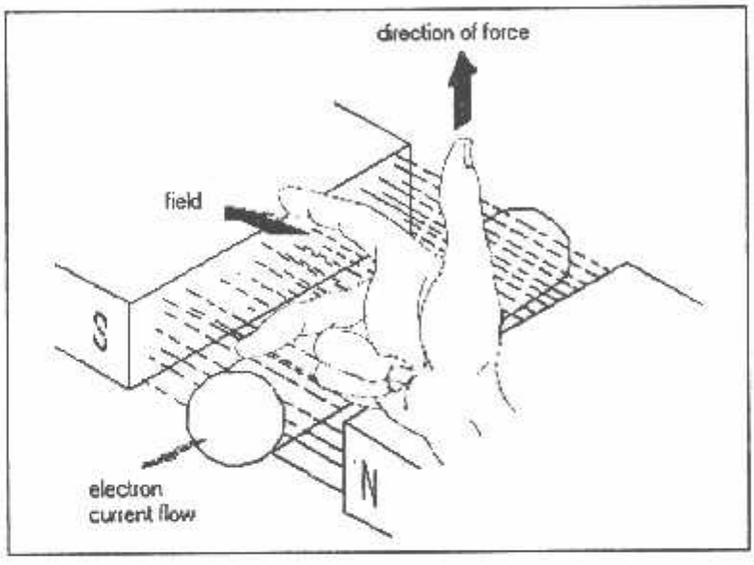
Pada sebuah motor dc, konduktor dibentuk menjadi sebuah loop sehingga ada dua bagian konduktor yang berada didalam medan magnet pada saat yang sama, seperti diperlihatkan pada gambar 2-14.

Konfigurasi konduktor seperti ini akan menghasilkan distorsi pada medan magnet utama dan menghasilkan gaya dorong pada masing-masing konduktor. Pada saat konduktor di tempatkan pada rotor, gaya dorong yang timbul akan menyebabkan rotor berputar searah dengan jarum jam, seperti diperlihatkan pada gambar 2-14



Gambar 2-14 Bergeraknya Sebuah Motor

Sebuah cara lagi untuk menunjukkan hubungan antara arus listrik yang mengalir didalam sebuah konduktor, medan magnet dan arah gerak, adalah kaidah tangan kanan untuk motor seperti yang diperlihatkan pada gambar 2-15



Gambar 2-15 Kaidah Tangan Kanan Untuk Motor

Kaidah tangan kanan untuk motor menunjukkan arah arus yang mengalir didalam sebuah konduktor yang berada dalam medan magnet. Jari tengah menunjukkan arah arus yang mengalir pada konduktor, jari telunjuk menunjukkan arah medan magnet dan ibu jari menunjukkan arah gaya putar. Adapun besarnya gaya yang bekerja pada konduktor tersebut dapat dirumuskan dengan :

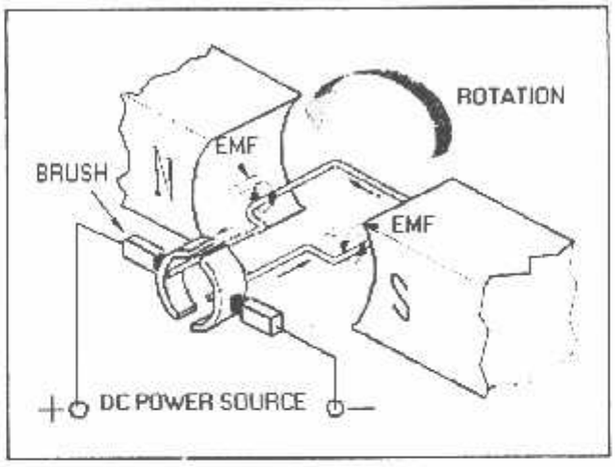
$$F = B.L.I \quad \text{(Newton)}$$

Dimana : B = kerapatan fluks magnet (weber)

L = panjang konduktor (meter)

I = arus listrik (ampere)

Dan gambar kontruksi dasar motor DC dapat dilihat pada gambar 2-16



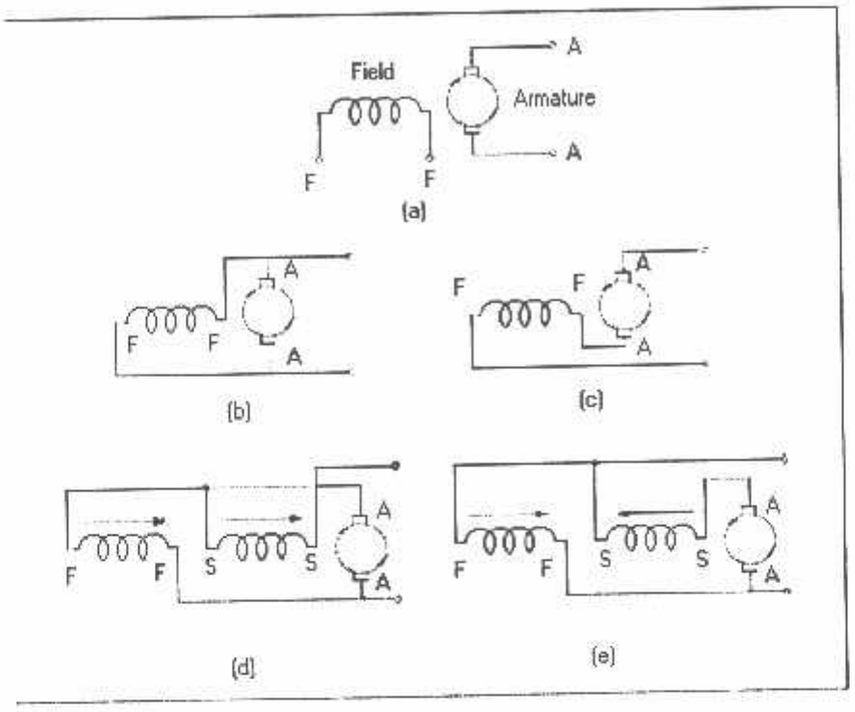
Gambar 2-16 Konstruksi Dasar Motor DC

Pada gambar diatas terlihat bahwa pada saat terminal motor diberi tegangan dc, maka arus elektron akan mengalir melalui konduktor dari terminal negatif menuju ke terminal positif. Karena konduktor berada diantara medan magnet, maka akan timbul medan magnet juga pada konduktor yang arahnya seperti terlihat pada gambar 2-16 diatas. Arah garis gaya medan magnet yang dihasilkan oleh magnet permanen adalah dari kutub utara menuju ke selatan. Sementara pada konduktor yang dekat dengan kutub selatan, arah garis gaya magnet disisi sebelah bawah searah dengan garis gaya magnet permanen sedangkan di sisi sebelah atas arah garis gaya magnet berlawanan arah dengan garis gaya magnet permanen. Ini menyebabkan medan magnet disisi sebelah bawah lebih rapat daripada

sisi sebelah atas. Dengan demikian konduktor akan terdorong ke arah atas. Sementara pada konduktor yang dekat dengan kutub utara, arah garis gaya magnet disisi sebelah atas searah dengan garis gaya magnet permanen sedangkan di sisi sebelah bawah arah garis gaya magnet berlawanan arah dengan garis gaya magnet permanen. Ini menyebabkan medan magnet disisi sebelah atas lebih rapat daripada sisi sebelah bawah. Dengan demikian konduktor akan terdorong ke arah bawah. Pada akhirnya konduktor akan membentuk gerakan berputar berlawanan dengan jarum jam seperti terlihat pada gambar 2-15 diatas.

2.5.2. Tipe Motor DC

Gambar 2-17 menunjukkan secara skematik beberapa metode pemasangan antara kumparan medan dengan armatur pada motor dc. Simbol lingkaran menunjukkan armatur motor dan simbol kotak disisi lingkaran menunjukkan sikat komutator *(brush)*. Arah anak panah menunjukkan arah medan magnet. Dan gambar dari tipe-tipe motor DC dapat dilihat pada gambar 2-17



Gambar 2-17 Tipe Motor DC

Gambar 2-16.a menunjukkan motor dc dengan penguatan terpisah. Pada tipe motor dc ini kumparan medannya tidak terhubung langsung dengan armaturnya.

Gambar 2-17.b menunjukkan motor dc *shunt*. Motor ini disebut motor *shunt* karena kumparan medan dipasang paralel dengan armatur.

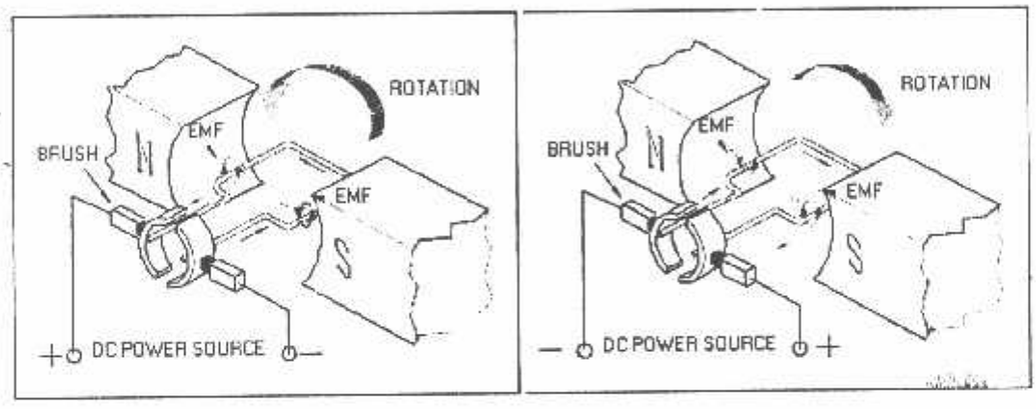
Gambar 2-17.c menunjukkan motor dc seri. Kumparan medannya dipasang seri dengan armatur.

Gambar 2-17.d dan 2-17.e menunjukkan motor dc kompon. Motor tipe ini adalah gabungan antara tipe motor dc shunt dan tipe motor dc seri. Gambar 2-17.d disebut motor dc *"cumulatively-compounded"*

karena satu kumparan medannya dipasang seri dengan armatur dan satu kumparan lagi dipasang seri dengan armatur sehingga arah medan magnetnya satu arah. Gambar 2-17.e disebut motor dc *"differentially-compounded"* karena dipasang sedemikian rupa sehingga arah medan magnetnya saling berlawanan.

2.5.3. Pengendalian Arah Putaran Motor DC

Agar putaran motor DC berubah, maka polaritas tegangan pada terminal motor harus di balik,seperti pada gambar 2-18



Gambar 2-18Arah Putaran Motor DC

BAB III

PERANCANGAN DAN PEMBUATAN ALAT

Perencanaan skripsi ini terdiri dari dua bagian, yaitu : perencanaan perangkat keras dan perencanaan perangkat lunak.

Perancangan perangkat keras terdiri dari beberapa bagian. Secara garis besar dapat dikategorikan sebagai berikut:

a. Perangkat pemroses utama

   Perangkat pemroses utama adalah mikrokontroller AT89S51

b. Perangkat masukan keluaran

   Perangkat masukan yang dibutuhkan berupa data tombol *keypad*, rangkaian sensor logam, rangkaian sensor putaran roda. Sementara perangkat keluaran yang dibutuhkan adalah rangkaian pengendali motor dc yang dapat mengendalikan putaran dari motor dc, rangkaian alarm dan sebuah LCD yang difungsikan sebagai tampilan data.

c. Perangkat pendukung

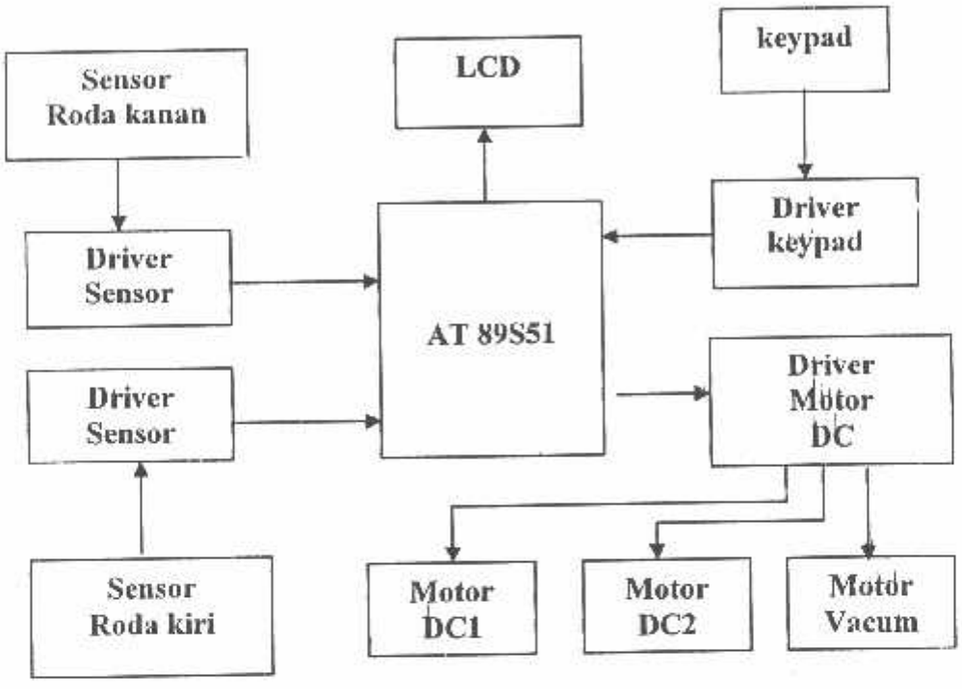
   Perangkat pendukung yang digunakan berupa mekanik pendeteksi logam.

Perencanaan perangkat lunak meliputi diagram alir dan urutan kerja programnya.

3.1. Perencanaan Perangkat Keras

3.1.1. Diagram Blok

Untuk gambar diagram blok alat pembersih lantai otomatis dapat dilihat pada gambar 3.1 dibawah ini.



Gambar 3-1 Diagram Blok Alat Pembersih Lantai Otomatis

Dari blok diagram diatas dapat dijelaskan fungsi dari masing-masing blok:

AT89S51 - Sebagai kontrol utama yang memproses data masukan dari sensor kemudian diolah dan dikeluarkan menjadi beberapa keluaran.

LCD - Berfungsi sebagai tampilan data inputan yang diinputkan melalui keypat.

Sensor Roda - Sensor Roda meliputi roda kiri dan Roda kanan rangkaian sensor menggunakan optoisolator, yang berfungsi sebagai sensor dari putaran roda untuk mendeteksi berpa kali putar tiap roda

Driver Sensor - Driver sensor dipasang pada masing masing sensor baik kiri maupun kanan , tujuan dari driver sensor itu sendiri yaitu berfungsi sebagai penguat arus dan pembalih logik dari keluaran sensor agar pdapat dibaca oleh mikrokontroller.

Keypad - Merupakan rangkaian yang berfungsi sebagai masukan dari alat ini yang berupa masukan panjang dan lebar dari lantai yang akan dibersihkan.

Driver keypad - Merupakan dekoder dari keluaran keypad 8 bit menjadi 4 bit yang kemudian diproses oleh mikrokontroller.

Driver motor - Merupakan rangkaian pengendali motor dan juga penguat arus yang dikeluarkan oleh mikrokontrollerdan juga penguat tegangan, agar motor dapat bekerja sesuai dengan arus dan tegangan yang dibutuhkan.

Motor DC - Merupakan alat penggerak dari roda kiri maupun roda kanan

Motor Vacum - Merupakan motor yang menggerakkan baling-baling dari penghisap debu

Ukuran Fisik Alat

Ukuran badan alat : Lebar badan alat = 28 cm

Panjang badan alat = 40cm

Tinggi badan alat = 20cm

Ukuran Roda penggerak

Roda kiri/kanan keliling = 20cm

Jumlah lobang pada roda = 20 lobang

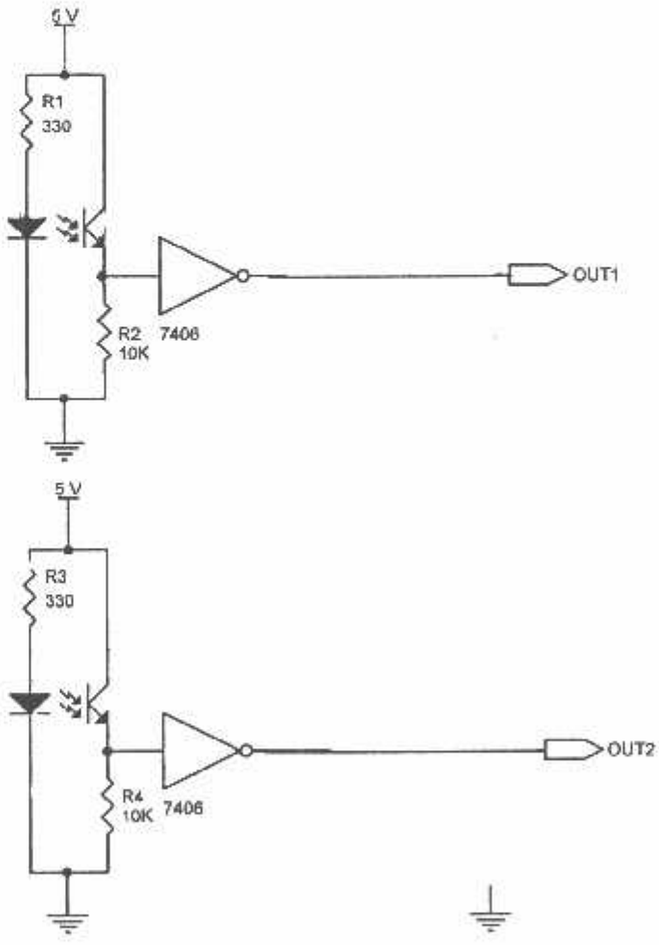
Dari blok diagram diatas dapat dijelaskan prinsip kerja dari alat pembersih lantai otomatis sebagai berikut :

1. Luas wilayah yang akan dideteksi dimasukkan melalui keypad. Luas wilayah ini akan ditampilkan juga ke LCD.
2. Agar mudah dalam penerimaan data dari keypad digunakan enkoder keypad yang akan menghasilkan kombinasi data 4 bit yang mengindikasikan penekanan masing-masing tombol. Komponen utama dekoder keypad adalah IC 74LS922.
3. Setelah luas wilayah diketahui, maka alat pendeteksi akan mulai bergerak dengan sistem scanning vertikal sesuai dengan luas wilayahnya. Untuk mengetahui berapa jarak yang telah ditempuh dapat diketahui dengan memasang sensor putaran (optocoupler) yang dipasang pada tiap sisi roda penggerak. IC AT89S51 akan menghitung jumlah pulsa dari tiap-tiap sensor putaran.
4. Untuk menggerakkan roda penggerak kiri dan kanan digunakan dua buah motor dc yang dikendalikan melalui driver motor dc. Komponen utama driver motor dc ini adalah IC L298.
5. Pada saat alat pembersih mulai diaktifkan, secara terus menerus vacum akan bekerja. Dan vacum akan berhenti sesuai area yang diinputkan.

3.1.2. Rangkaian Driver dan Sensor Putaran

Untuk mendeteksi jarak tempuh roda, dipasang sensor putaran yang terdiri dari sebuah optoisolator pada masing-masing roda. Pada roda juga dipasang sebuah piringan dengan lubang sebanyak 20 buah. Piringan ini dipasang sedemikian rupa sehingga posisi lubang berada diantara celah optoisolator.

Keliling roda dibuat sepanjang 20 cm, sehingga untuk menempuh jarak sejauh 1 m maka roda harus bergerak sebesar 5 X 360^0 atau menghasilkan 5 X 20 pulsa pada keluaran rangkaian sensor putaran. gambar 3-2 Berikut ini adalah rangkaian sensor putaran yang digunakan dalam perancangan ini.



Gambar 3-2 Rangkaian Driver danSensor Putaran

Dari lembar datasheet, diketahui

- Optoisolator :

I_F = 10 mA

V_F = 1,5 V

V_{CC} = 5 V

Dari data tersebut dapat dihitung besarnya R_1 :

$$Vin = V_{R1} + V_F$$

$$5 = (I_F . R_1) + 1,5$$

$$5 = (10 . 10^{-3} . R_1) + 1,5$$

$$5 - 1,5 = 10 . 10^{-3} R_1$$

maka : $R_1 = \frac{3,5}{10 \cdot 10^{-3}}$

$R_1 = 350\ \Omega$ (Pada perancangan ini digunakan $R_1 = 330\ \Omega$)

R2 dan R4 adalah sebuah resistor *pull-down* yang dipasang dengan maksud untuk menjaga kondisi keluaran agar tidak ada kondisi mengambang (antara logika 1 dan 0). Pada saat transistor optoisolator dalam keadaan saturasi maka tegangan di keluaran (yang akan masuk ke AT89S51), sebesar 5 V, tetapi pada saat transistor optoisolator dalam keadaan cut-off, diharapkan tegangan keluaran mendekati 0 Volt. Ini dapat dicapai dengan pertimbangan sebagai berikut

Diketahui :

Tegangan supply (V_{CC}) = 5 Volt

Arus (I) = 0,01mA (ini adalah arus yang dibutuhkan oleh masukan

AT89S51) Tegangan keluaran (V_{OUT}) ≈ 5 Volt (atau 4,9 Volt)

$$V_{CC} = I \cdot R + V_{OUT}$$
$$5 = (0{,}01 \cdot 10^{-3} \cdot R) + 4{,}9$$
$$R = \frac{0{,}1}{0{,}01 \cdot 10^{-3}}$$
$$R = 10000\Omega$$

maka nilai $R = R_2 = R_4 = 10\ K\Omega$

3.1.3. Rangkaian Keypad

Rangkaian *keypad* dibentuk dari sebuah *encoder keyboard* yaitu IC MM74C922 yang dapat menghubungkan *keypad* 4 X 4 dengan suatu sistem digital. Enkoder *keyboard* MM74C922 akan mengkonversi suatu tombol *keyboard* menjadi 4 bit data digital. Kecepatan *scan keyboard* dapat ditentukan dengan merubah nilai kapasitor C_{OSC} (*oscillator capacitor*).

Perioda *debounce keyboard* dapat ditentukan dengan mengubah nilai kapasitor C_{MSK} (*mask capacitor*). MM74C922 dapat diaplikasikan untuk beberapa jenis *keyboard* atau dapat juga diaplikasikan untuk *keypad*. Enkoder *keyboard* MM74C922 ini bisa dihubungkan dengan *keypad* dengan konfigurasi 4 kolom dan 4 baris.

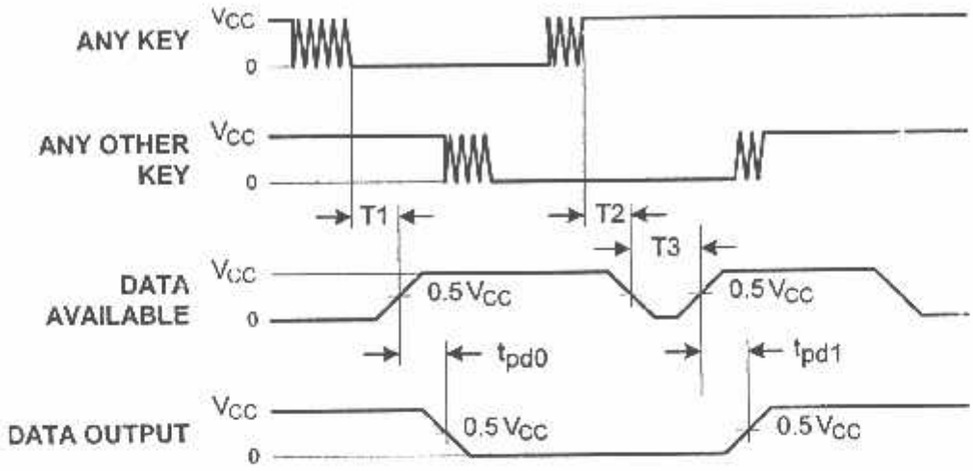
Saat tidak ada penekanan tombol, *input* baris dikonndisikan pull high (berlogika 1) oleh resistor *pull-up* internal dan *output* kolom selalu mengeluarkan logika 0 secara bergantian dengan sistem *scan* kolom. Kecepatan *scan* kolom ini tergantung dari besarnya frekuensi osilator yang dapat ditentukan dengan memasang kapasitor C_{OSC} pada kaki OSC MM74C922. Didalam MM74C922

sendiri sudah terdapat osilator *schmitt trigger, counter* 2 bit dan *decoder* 2 bit ke 4 bit.

Pada saat sebuah tombol ditekan, misalnya tombol 0, kondisi *input* Y1 tidak berubah jika *output* X1 *high*. Pada saat *output* X1 berlogika 0 maka *input* Y1 juga akan berlogika 0. Kondisi ini akan membuat *counter* berhenti bekerja dan menyebabkan *output* X1 tetap berlogika 0. Kondisi *low* pada Y1 ini juga akan membuat rangkaian pewaktu *key bounce* bekerja dan mengunci *input* Y yang lain. Kode *keypad* yang dihasilkan, nilainya sesuai dengan nilai *counter* yang tadi dihentikan. Ketika rangkaian pewaktu *key bounce* telah melampaui konstanta waktunya, maka data akan ditahan (*latch*) dan kaki *Data Available* (DA) akan mengeluarkan logika 1.

Jika ada penekanan tombol lain, maka *input* Y1 akan kembali berlogika 1, proses *scan* akan di ulang (*restart*) dan akan mereset rangkaian pewaktu *key bounce*. Pada saat pelepasan tombol *keypad* mungkin saja terjadi *bounce*. Agar *bounce* ini tidak dianggap oleh *encoder* sebagai adanya penekanan tombol *keypad*, maka rangkaian pewaktu *key bounce* harus melampaui konstanta waktunya sebelum terjadi *bounce* tersebut. Berikut ini adalah diagram waktu dari MM74C922 yang diambil dari lembaran *data sheet*.

Untuk penunjuk waktu IC MM74C922 dapat dilihat pada gambar 3.3 dibawah ini.



Gambar 3-3 Diagram Waktu MM74C922

Sumber: *Datasheet* MM74C22, Fairchild Semiconductor

Dari lembaran *datasheet* disebutkan bahwa T1 = T2 = RC, T3 = 0,7 RC dimana R adalah resistor *pull up* internal 10 KΩ dan C adalah kapasitor C_{MSK} yang dipasang di kaki KBM. Besarnya nilai C_{MSK} adalah 10 kali besarnya C_{OSC}.

Jika *bounce keypad* dianggap selama 30 mS dan jarak antara *bounce* penekanan dan *bounce* pelepasan *keypad* dianggap selama 30 mS, maka besarnya T1 dan T2 harus lebih besar dari 30 mS tapi harus lebih kecil dari 60 mS. Misalnya dianggap minimal T1 = T2 = 40 mS dan maksimal 50 mS. Dengan demikian dapat dihitung besarnya C_{MSK} sebagai berikut :

Minimal : $T1 = T2 = 40.10^{-3} = 10.10^{3} . C_{MSK}$

$C_{MSK} = 40.10^{-3} / 10.10^{3}$

$C_{MSK} = 4.10^{-5} = 4$ uF

Maksimal : $T1 = T2 = 50.10^{-3} = 10.10^{3} . C_{MSK}$

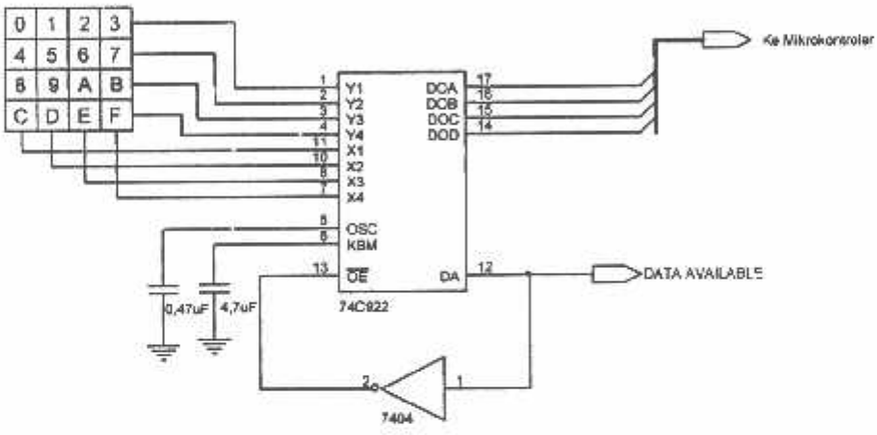
$C_{MSK} = 50.10^{-3} / 10.10^{3}$

$C_{MSK} = 5.10^{-5} = 5$ uF

Pada perancangan ini digunakan C_{MSK} sebesar 4,7uF. Sedangkan C_{OSC} dapat dihitung dari rumus :

$C_{MSK} = 10.C_{OSC}$ maka $C_{OSC} = 4,7$ uF / 10 = 0,47 uF.

Dengan mengacu pada uraian diatas, maka dapat disusun rangkaian *keypad* seperti terlihat pada gambar 3-4 berikut.



Gambar 3-4 Rangkaian *Keypad*

Sumber : Perancangan Alat

Berikut ini adalah tabel kebenaran dari MM74C922 :

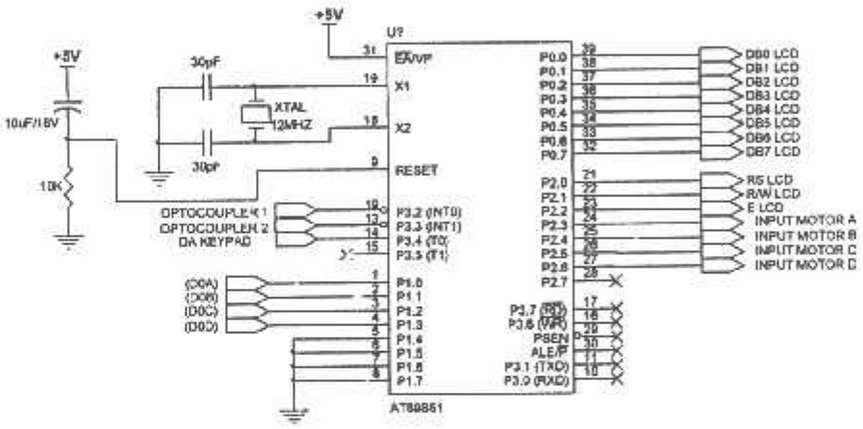
Tabel 3-1 Tabel Kebenaran MM74C922

	POSISI SWITCH	Y1,X1	Y1,X2	Y1,X3	Y1,X4	Y2,X1	Y2,X2	Y2,X3	Y2,X4
O	A	0	1	0	1	0	1	0	1
U	B	0	0	1	1	0	0	1	1
T	C	0	0	0	0	1	1	1	1
	D	0	0	0	0	0	0	0	0
	DA	0	0	0	0	0	0	0	0

	POSISI SWITCH	Y3,X1	Y3,X2	Y3,X3	Y3,X4	Y4,X1	Y4,X2	Y4,X3	Y4,X4
O	A	0	1	0	1	0	1	0	1
U	B	0	0	1	1	0	0	1	1
T	C	0	0	0	0	1	1	1	1
	D	1	1	1	1	1	1	1	1
	DA	0	0	0	0	0	0	0	0

3.1.4. Minimum Sistem Mikrokontroller AT89S51

Untuk gambar rangkaian minimum sistem mikrokontroller AT89S51 dapat dilihat pada gambar 3.5 dibawah ini.



Gambar 3-5 Minimum Sistem Mikrokontroller AT89S51

Sumber : Perancangan alat

Penggunaan port Mikrokontroller AT89S51 pada rancangan ini adalah sebagai berikut :

- P0.0 sampai P0.7 : data LCD
- P2.0 sampai P2.2 : kontrol LCD
- P1.0 sampai P1.3 : input keypad

- P3.2 : input optocoupler 1
- P3.3 . input optocoupler2
- P3.4 : DA keypad
- P2.3 sampai P2.6 : Output motor DC

3.1.5. Rangkaian LCD

Pada lembaran *datasheet* modul LCD M1632 SEIKO INSTRUMENT INC. disebutkan bahwa :

- *Power supply* LCD meliputi :

  Vss = 0 V (GND)

  Vcc = 5 V ± 10% (2mA)

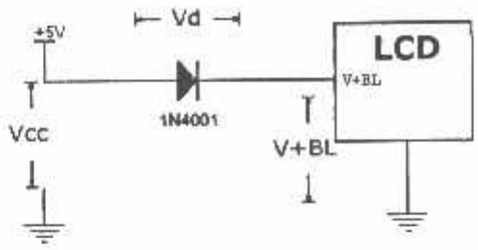
  Vee = Vcc-13,5 V sampai Vcc + 0,3 V (1mA pada Vee = 0,25 V)

- *Power supply Back Light* :

  V+BL = 4 V sampai 4,2 V (50 sampai 200mA)

  V-BL = 0 V (GND)

Untuk memenuhi ketentuan diatas, maka digunakan sebuah variabel resistor dengan tujuan membuat tegangan variabel untuk *input* Vee.seperti yang ditunjukkan pada gambar 3.6



Gambar 3-6 Pemasangan Dioda Pada LCD

Sumber : Perancangan alat

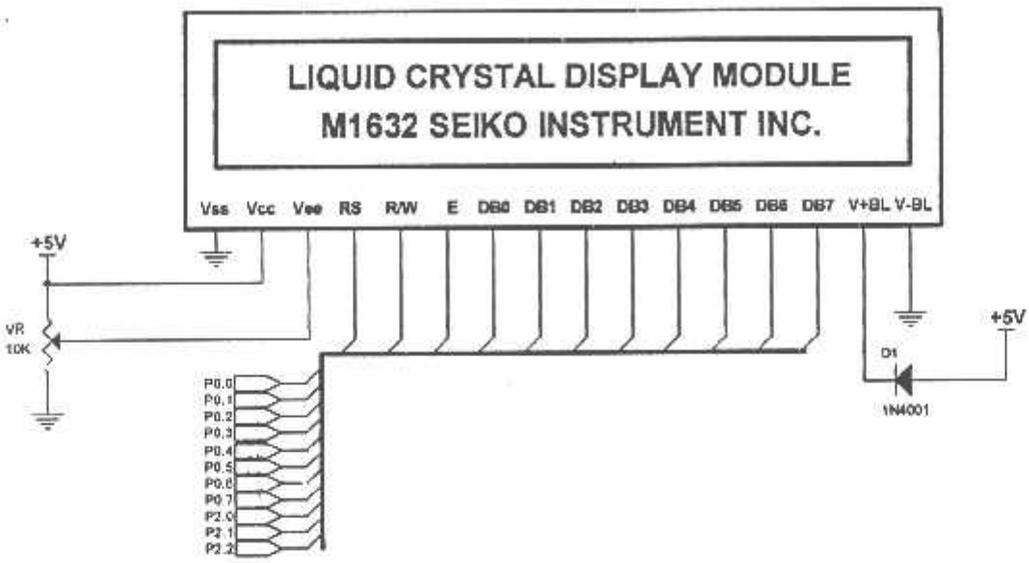
Pada *input* V+BL dipasang sebuah dioda 1N4001 (bahan silicon dengan Vd = 0,65 V sampai 0,7 V). Tujuannya adalah didapatkan tegangan V+BL sebesar 4,3 V dengan perhitungan sebagai berikut :

$$Vcc = Vd + (V+BL)$$

$$5 = 0,7 + (V+BL)$$

$$(V+BL) = 5 - 0,7 = 4,3\ V$$

Dipilih dioda 1N4001 karena arus maksimum yang bisa dilewatkan oleh dioda ini sebesar 1A. Berikut ini adalah rangkaian lengkap modul LCD yang digunakan dalam perancangan.seperti yang ditunjukkan pada gambar 3.7

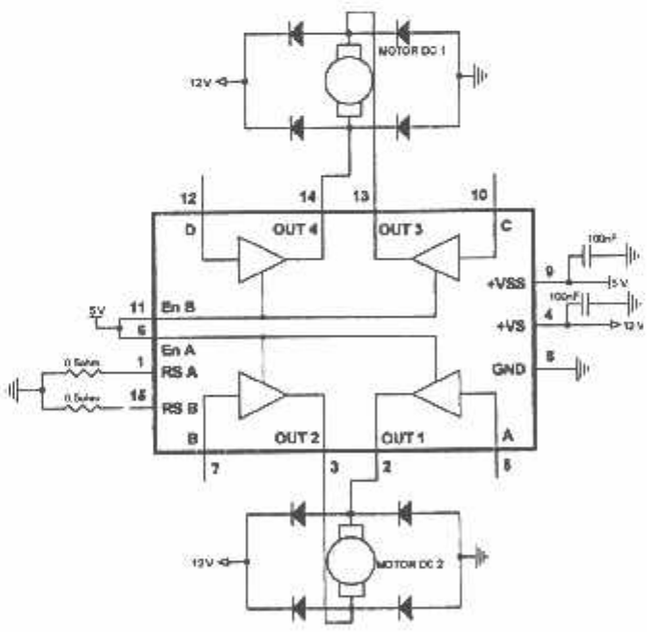


Gambar 3-7 Rangkaian LCD

Sumber : Perancangan Alat

3.1.6. Pengendali Motor DC

Rangkaian dari pangandali Motor DC dapat dilihat pada gambar 3.8 dibawai ini.



Gambar 3-8 Rangkaian Pengendali Motor DC

Sumber : Perancangan Alat

Pada IC_1 L298 kaki 1 dan 15 adalah kaki *Sensing Voltage*. Kaki ini akan mengendalikan besarnya arus beban. Dalam keadaan tidak terhubung ke ground, *tegangan sensing (V_{sens})* pada kaki ini sebesar 3 Volt. Agar motor dapat berputar, tegangan pada kaki 1 dan 15 harus sebesar -1 Volt sampai +2 Volt. Apabila diinginkan arus yang mengalir pada beban sebesar 4 A (dari baterai 12V/4Ah), maka :

$$I = \frac{Vsens}{Rs}$$

$$4 = \frac{2}{Rs}$$

$$Rs = \frac{2}{4}$$

$$Rs = 0{,}5\Omega$$

Komponen utama rangkaian penggerak motor dc ini adalah IC L298N yang merupakan IC yang dirancang khusus untuk keperluan pengendalian motor dc. IC L298N didalamnya terdapat empat penggerak push-pull yang dapat mengalirkan arus pada keluarannya sampai sebesar 4A tiap jalurnya. Masing-masing jalur dikendalikan oleh sebuah sebuah TTL yang kompatibel. Tegangan yang bisa dikendalikan untuk supply motor mencapai 46 V.

Cara kerja rangkaian adalah sebagai berikut:

Agar motor 2 dapat berputar, maka dibutuhkan tegangan supply motor (Vc). Tegangan Vc ini diumpankan ke IC L298N pada kaki 4 dan akan dikeluarkan ke kaki 13 (output 3) dan ke kaki 14 (output 4). Keluar atau tidaknya tegangan Vc dapat ke output 3 atau ke output 4 akan ditentukan oleh kondisi kaki 10 (D) dan kaki 12 (C) serta kondisi kaki 11 (*Enable B*).

Apabila pada input C terdapat logika *high*, pada input D terdapat logika *low* dan pada *Enable B* terdapat logika *high*, maka tegangan Vc akan keluar ke kaki 13 sedangkan dikaki 14 tidak akan ada tegangan. Dengan kondisi seperti ini maka satu terminal motor akan mendapat tegangan sebesar Vc dan satu terminal lainnya akan mendapat tegangan sebesar 0 V. Dengan demikian motor dc 1 akan berputar ke kanan.

Apabila pada input C terdapat logika *low*, pada input D terdapat logika *high* dan pada *Enable B* terdapat logika *high*, maka tegangan Vc akan keluar ke kaki 14 sedangkan dikaki 13 tidak akan ada tegangan. Dengan kondisi seperti ini maka satu terminal motor akan mendapat tegangan sebesar Vc dan satu terminal lainnya akan mendapat tegangan sebesar 0 V. Dengan demikian motor dc 1 akan berputar ke kiri.

Apabila kedua input C dan D terdapat logika yang sama dan pada *Enable B* terdapat logika *high*, maka tegangan Vc akan keluar ke kaki 13 dan 14. Dengan kondisi seperti ini maka kedua terminal motor akan mendapat tegangan sebesar Vc. Dengan demikian motor dc 1 akan berhenti secara cepat karena disertai pengereman.

Apabila pada *Enable B* terdapat logika *low*, apapun kondisi pada input C dan D, maka tegangan Vc tidak akan keluar ke kaki 13 dan 14. Dengan kondisi seperti ini maka kedua terminal motor akan mendapat tegangan sebesar 0 V. Dengan demikian motor dc 1 akan berhenti tanpa disertai pengereman. Dan data dapat dilihat pada tabel 3.2 .

Pada skema rangkaian terlihat ada 8 buah dioda 4A (1N4004) yang dipasang dengan konfigurasi jembatan dioda. Maksud dari pemasangan jembatan dioda ini adalah menghilangkan gelombang osilasi yang timbul akibat adanya beban induktif yaitu kumparan motor.

Tabel 3-2 Tabel Kebenaran IC L298N

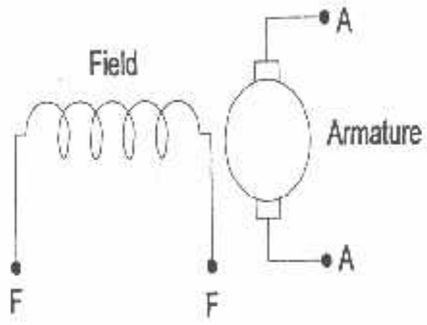
INPUT		FUNGSI MOTOR
EN A = H	A = H ; B = L	Motor 2 Berputar ke kanan
	A = L ; B = H	Motor 2 Berputar ke kiri
	A = B	Motor 2 Berhenti dengan cepat
EN A = L	A = X ; B = X	Motor 2 Berhenti tanpa ada pengereman
EN B = H	C = H ; D = L	Motor 1 Berputar ke kanan
	C = L ; D = H	Motor 1 Berputar ke kiri
	C = D	Motor 1 Berhenti dengan cepat
EN B = L	A = X ; B = X	Motor 1 Berhenti tanpa ada pengereman

Keterangan :
H = *High* L = *Low* X = *Don't Care*

3.1.7. Motor DC

Motor dc yang dipakai dalam alat ini merupakan motor dc dengan penguatan terpisah. Pada tipe motor dc ini kumparan medannya tidak terhubung langsung dengan armaturnya seperti yang ditunjukkan pada gambar 3.9

Gambar 3.9 Tipe Motor Dc Dengan Penguat Terpisah



Gambar 3.9 Tipe Motor Dc Dengan Penguat Terpisah

Motor DC yang digunakan memerlukan Arus sebesar 1 Ampere dimana daya yang dihasilkan sebesar:

W = V . I

W = 12 . 1

W = 12 Watt

Sedangkan 1HP = 735 Watt

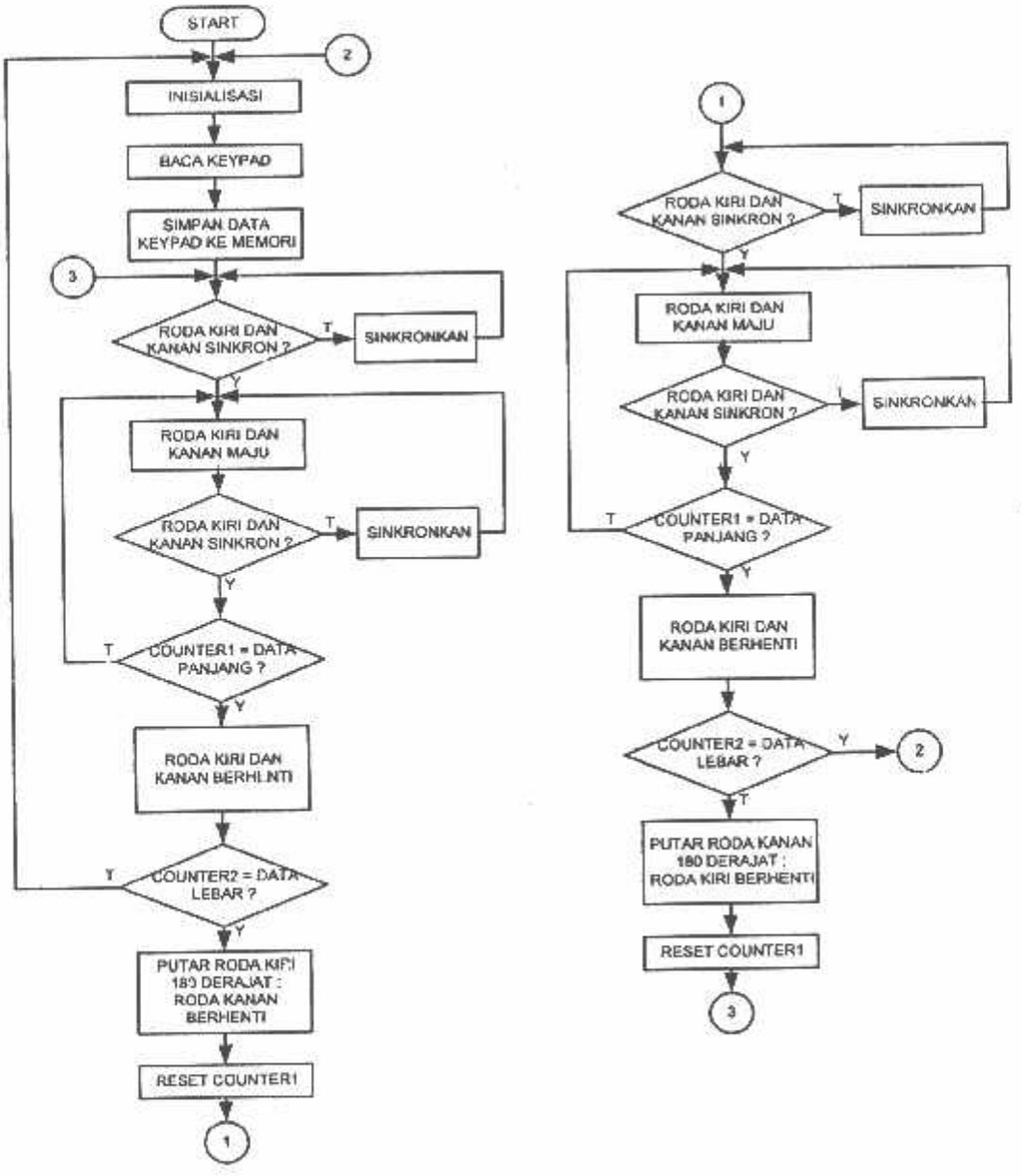
Jadi daya motor sebesar 0,016 HP

Untuk motor DC sebagai penggerak Roda dibutuhkan Transmisi kecepatan yang sangat besar maka dibutuhkan sebuah gir boks yang memiliki perbandingan 96 : 1 . Dimana 96 kali putaran motor DC menghasilkan 1 kali Putaran dari gir boks sehingga kecepatan dari alat dapat dilihat dan pelan . Sedangkan Motor DC untuk Penggerak Vacum memerlukan kecepatan putaran yang tinggi dimana berfungsi sebagai penghisap debu.

3.2. Perancangan Perangkat Lunak

3.2.1. Diagram Alir

Untuk cara kerja dari keseluruhan alat dapat dilihat dari diagram alir seperti yang ditunjukkan pada gambar3.10 berikut ini.



Gambar 3-10 Diagram Alir Program Utama Alat Pembersih Lantai

Dari diagram alir diatas dapat dijelaskan sistematika eksekusi program sebagai berikut :

- Inisialisasi

  Pada proses inisialisasi, mikrokontroller akan melakukan proses inisialisasi LCD agar siap digunakan.

- Baca keypad

  Pada saat terdapat logika 1 pada pin DA IC MM74C922 maka pada saat itu menandakan adanya penekanan tombol keypad. Data pertama yang masuk (data 4 bit) dianggap sebagai digit pertama panjang area pencarian. Data ini dimasukkan kedalam register 8 bit didalam AT89S51 yang dinamakan D_Pjg. Data tersebut diisikan pada byte atas sedangkan byte bawahnya diisikan data keypad selanjutnya. Untuk data lebar dimasukkan kedalam register D_Lbr.

- Simpan data keypad ke memori

  Data panjang dimasukkan ke register D_Pjg sedangkan data lebar dimasukkan ke register D_Lbr.

- Roda kiri dan kanan sinkron ?

  Pada roda kiri dan kanan terdapat piringan dengan jumlah lubang sebanyak 20 buah. Pada piringan ini dipasang sensor putaran yang akan menghasilkan 1 pulsa setiap 1 lubang. Pulsa pada roda kiri dihitung oleh counter0 sedangkan pulsa pada roda kanan dihitung oleh counter1 pada mikrokontroller.

- Sinkronkan

Agar detektor tetap bergerak lurus maka nilai counter untuk roda kiri dan kanan harus sama. Misalnya, counter roda kiri bernilai 20 sedangkan counter roda kanan bernilai 19, maka AT89S51 akan memerintahkan driver motor dc agar menghentikan roda kiri dan tetap memutar roda kanan. Jika nilai counter pada roda kanan telah bernilai 20, maka roda kiri baru boleh berputar.

- Roda kiri dan kanan maju

  Pada driver motor dc terdapat 4 buah masukan yaitu ABCD. Agar motor dc2 untuk roda kiri bergerak maka masukan A diberi logika 0 dan B harus diberi logika 1. Demikian pula untuk motor dc1 masukan C diberi logika 0 dan masukan D diberi logika 1.

- Counter1 = Data Panjang ?

  Apakah isi Counter1 dengan data Panjang ?

- Roda kiri dan kanan berhenti

  Agar roda kiri dan kanan berhenti maka masukan A, B, C dan D diberi logika 0.

- Counter2 = Data Lebar ?

  Apakah isi Counter2 dengan data Lebar ?

- Putar roda kiri 180^0 roda kanan berhenti

  Agar roda kiri berputar 180^0 maka masukan A diberi logika 0 dan masukan B diberi logika 1 selama nilai counter1 = 63. Sedangkan masukan C dan D diberi logika 0.

- Reset counter1

  Mengembalikan isi counter1 pada nilai 0.

- Putar roda kanan 180^0 roda kiri berhenti

  Agar roda kanan berputar 180^0 maka masukan C diberi logika 0 dan masukan D diberi logika 1 selama nilai counter1 = 63. Sedangkan masukan A dan B diberi logika 0.

3.2.2. Proses Pembuatan Program

Sedangkan untuk memprogram mikrokontroller AT89S51 diperlukan sebuah file dengan ekstensi .HEX atau .BIN. Untuk dapat menghasilkan file ini digunakan software HB2000 dengan urutan kerja sebagai berikut:

- Membuat listing program di lembar kerja notepad dan disimpan dengan nama file bayu.H51.
- Melakukan kompilasi file bayu.H51 dengan menggunakan software HB2000 sampai menghasilkan file bayu.BIN.
- Melakukan download file bayu.BIN ke Mikrokontroller AT89S51 dengan menggunakan module HB2000C.

BAB IV

PENGUJIAN ALAT

Secara umum, pengujian ini bertujuan untuk mengetahui apakah alat dapat bekerja sesuai dengan spesifikasi perencanaan yang telah ditetapkan. Pengujian dibagi menjadi dua bagian, yaitu pengujian perangkat keras dan pengujian perangkat lunak. Pertama-tama akan dilakukan pengujian unjuk kerja perangkat keras. Pengujian dilakukan pada masing-masing blok rangkaian penyusun sistem.

4.1. Pengujian Perangkat Keras

Tujuan pengujian yang dilakukan terhadap sistem adalah sebagai berikut:

- Mengetahui unjuk kerja rangkaian sensor putaran
- Mengetahui unjuk kerja rangkaian keypad.
- Mengetahui unjuk kerja rangkaian driver motor DC.

4.1.1. Pengujian Rangkaian Sensor Putaran

- **Tujuan**

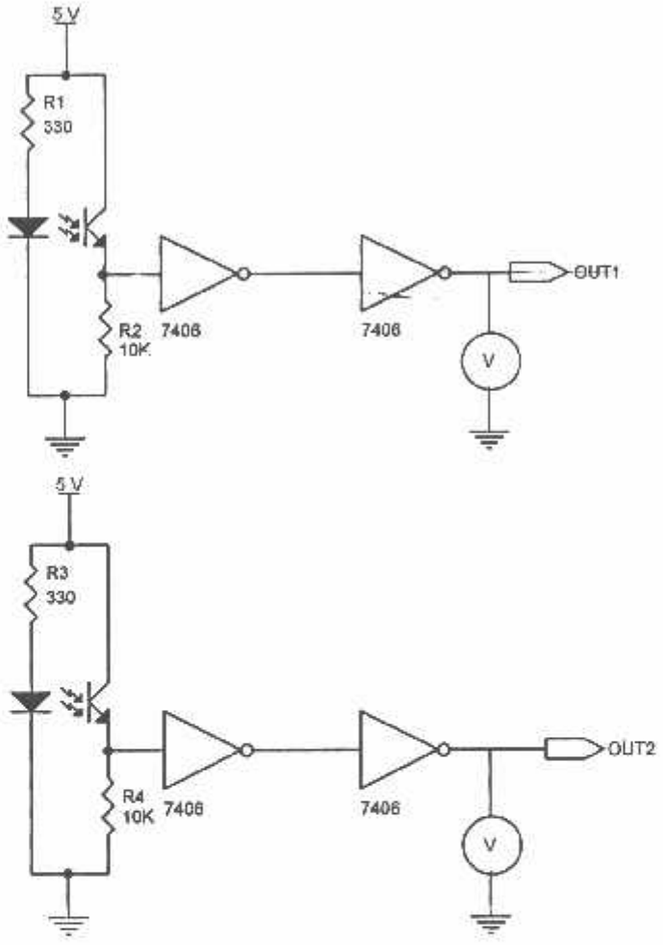
Untuk mengetahui apakah rangkaian sensor infra merah bekerja dengan baik dan mampu mengkondisikan keluarannya menjadi dua kondisi *high* dan *low*.

- **Peralatan yang digunakan**

1. Multimeter digital SANWA CD800.
2. Rangkaian sensor putaran yang akan diuji.
3. Catu daya 5 volt.

- **Prosedur pengujian**

1. Membuat rangkaian sensor putaran sesuai dengan perancangan. Dan gambar pengujian sensor putaran dapat dilihat pada gambar 4-1



Gambar 4-1 Pengujian Sensor Putaran

Sumber : Perancangan Alat

2. Menghubungkan rangkaian sensor putaran dengan catu daya 5 volt.
3. Menutup celah antara dioda infra merah dengan phototransistor.
4. Melakukan pengukuran tegangan pada masing-masing keluaran 74LS06, dan memasukkan hasil pengukuran ke tabel 4-1.

5. Membuka celah antara dioda infra merah dengan phototransistor.
6. Melakukan pengukuran tegangan pada masing-masing keluaran 74LS06, dan memasukkan hasil pengukuran ke tabel 4-1.

- **Data Hasil Pengujian**

Tabel 4-1 Hasil Pengujian Tegangan Sensor Putaran

No.	Tegangan				Unit
	Terhalang		Tidak Terhalang		
	Vout 1	Vout 2	Vout 1	Vout 2	
1.	0,30	0,30	5,15	5,15	Volt

- **Analisa Hasil Pengujian**

Dari hasil pengujian sensor putaran pada saat celah antara dioda infra merah dengan phototransistor terhalang diperoleh tegangan keluaran gerbang NOT sebesar 5,15 volt. Tegangan sebesar ini oleh AT89S51 dibaca sebagai logika *high*. pada saat celah antara dioda infra merah dengan phototransistor terhalang diperoleh tegangan keluaran gerbang NOT sebesar 0,45 volt. Tegangan sebesar ini oleh AT89S51 dibaca sebagai logika *low*.

4.1.2. Pengujian Rangkaian Driver Keypad

- **Tujuan**

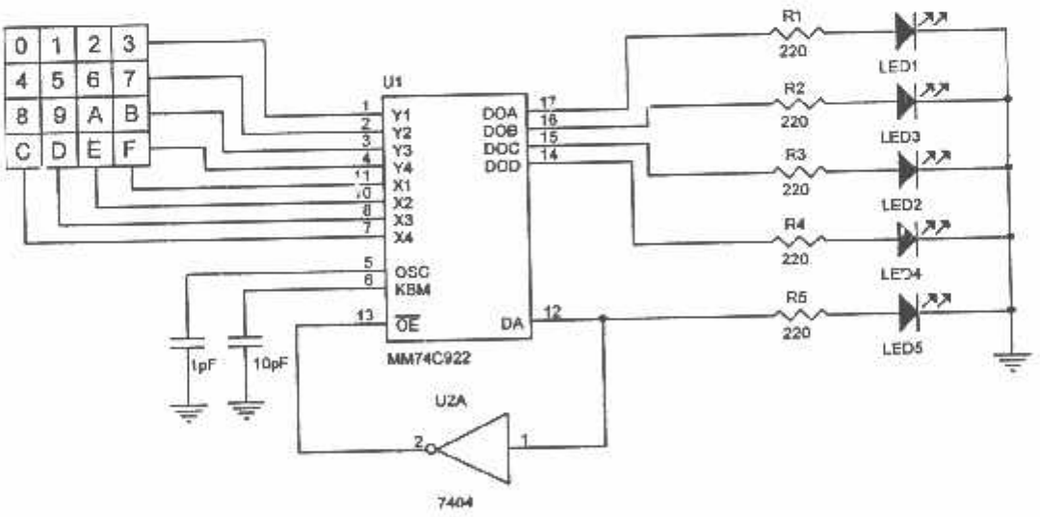
Untuk menguji apakah rangkaian driver keypad dapat bekerja sebagai mana mestinya.

- **Perlatan Yang Digunakan**

1. Multimeter digital SANWA CD800.
2. Rangkaian driver keypad.
3. Catu daya 5 volt.

- **Prosedur Pengujian**

1. menyusun rangkaian pengujian driver keypad seperti pada gambar 4-2.



Gambar 4-2 Pengujian Driver Keypad

Sumber : Perancangan Alat

2. Menghubungkan rangkaian driver keypad dengan catu daya 5V

3. Memberikan kombinasi masukan dengan menekan tombol-tombol keypad sesuai dengan data pada tabel 4-2

4. Mengamati hasil keluaran berupa nyala LED. Kemudian mencatat hasil pengamatan pada tabel 4.2.

Tabel 4-2 Hasil Pengujian Driver Keypad

No	TOMBOL YANG DITEKAN	OUTPUT				
		LED1	LED2	LED3	LED4	LED5
1	0	0	0	0	0	1
2	1	1	0	0	0	1
3	2	0	1	0	0	1
4	3	1	1	0	0	1
5	4	0	0	1	0	1
6	5	1	0	1	0	1
7	6	0	1	1	0	1
8	7	1	1	1	0	1
9	8	0	0	0	1	1
10	9	1	0	0	1	1
11	A	0	1	0	1	1
12	B	1	1	0	1	1
13	C	0	0	1	1	1
14	D	1	0	1	1	1
15	E	0	1	1	1	1
16	F	1	1	1	1	1

Keterangan :

0 = LED mati

1 = LED nyala

- **Analisa Hasil Pengujian**

dari gambar rangkaian pengujian *driver keypad* pada gambar 4-2 digunakan lima buah LED yang difungsikan sebagai pendeteksi pada tegangan output. Dari tabel 4-2 tampak bahwa saat penekanan tombol "0" pada keypad, maka keluaran pada LED 1 sampai dengan LED 4 akan berkondisi low (lampu mati) sedangkan pada Led 5 akan berkondisi high (lampu nyala) hal ini dikarenakan LED 1 sampai LED 4 terhubung dengan output data keypad, sedangkan untuk LED 5 terhubung dengan output indikator, jadi Led ini akan aktif apabila ada penekanan tombol keypad. Pada penekanan tomol "2", maka LED 1 dan LED 5 akan menyala, sedangkan LED 2 sampai LED 4 akan mati, hal ini harus sesuai dengan konversi dari bilangan desimal ke bilangan heksadesimal . demikian pula untuk penekanan pada to mbol-tombol lainnya seperti yang terlihat pada tabel 4-2 diatas.

4.1.3. Pengujian Rangkaian Driver Motor DC

- **Tujuan**

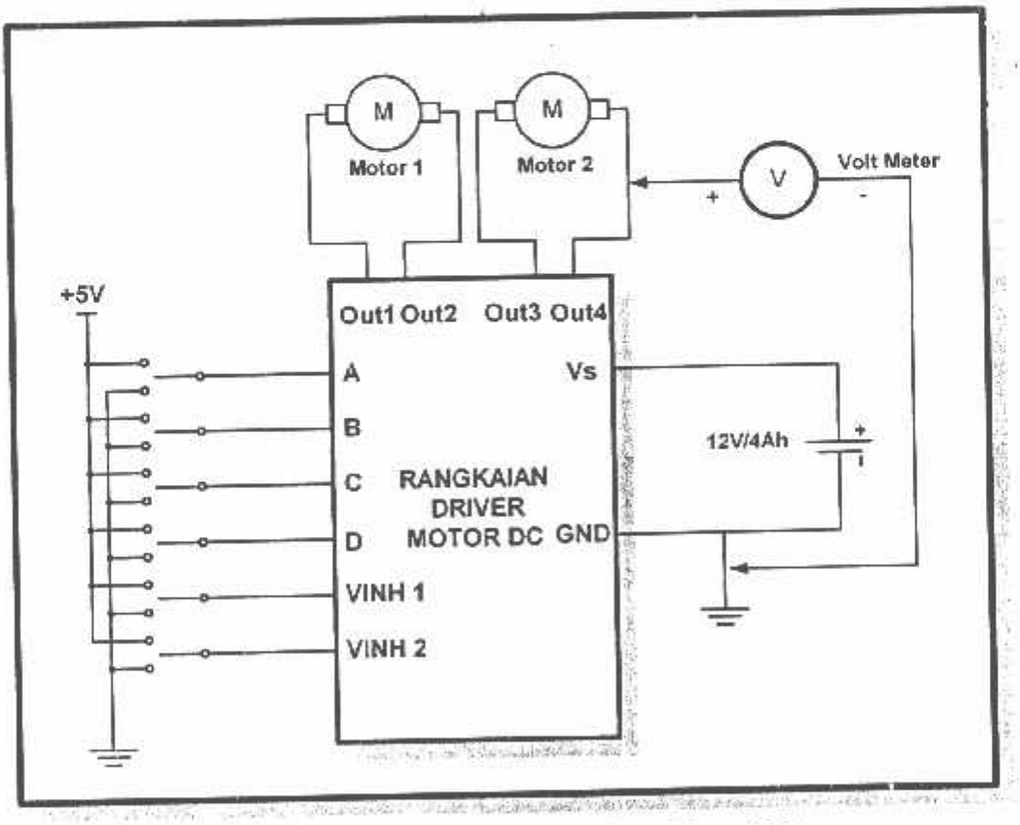
Untuk mengetahui apakah rangkaian driver motor dc dapat bekerja sebagaimana mestinya.

- **Peralatan yang digunakan**

1. Multimeter digital SANWA CD800.
2. Rangkaian driver motor dc.
3. Catu daya 5 volt.
4. Catu daya 12 volt.

- **Prosedur pengujian**

Menyusun rangkaian pengujian driver motor DC seperti dalam gambar 4-3.



Gambar 4-3 Pengujian Driver Motor DC

1. Menghubungkan rangkaian driver motor dc dengan catu daya 5 volt dan 12 volt.
2. Memberikan kombinasi masukan pada A, B, C, D, VINH1 dan VINH2 sesuai dengan kombinasi data pada tabel 4-3.
3. Mengukur tegangan pada tiap terminal motor terhadap ground. Kemudian mencatat hasil pengukuran pada tabel 4-3.

Tabel 4-3 Hasil Pengujian Driver Motor DC

No.	INPUT						OUTPUT				UNIT
	A	B	C	D	VINH1	VINH2	Out 1	Out 2	Out 3	Out 4	
1.	0	0	0	0	1	0	0,76	0,78	-	-	V
2.	0	1	0	1	1	0	0,75	10,31	-	-	V
3.	1	0	1	0	1	0	10,31	0,78	-	-	V
4.	1	1	1	1	1	0	10,30	10,30	-	-	V
5.	0	0	0	0	0	1	-	-	0,78	0,77	V
6.	0	1	0	1	0	1	-	-	0,79	10,31	V
7.	1	0	1	0	0	1	-	-	10,31	0,78	V
8.	1	1	1	1	0	1	-	-	10,30	10,30	V

Keterangan :

0 = *Low*

1 = *High*

- = Tidak ada tegangan

- **Analisa Hasil Pengujian**

Dari hasil pengukuran tegangan diatas, terlihat bahwa pada kondisi input A = 0, B = 1 dan VINH1 = 1, didapatkan tegangan pada out1 = 0,75 V dan out2 = 10,31 V. Pada kondisi ini motor 1 akan berputar searah dengan jarum jam.

Pada kondisi input A = 1, B = 0 dan VINH1 = 1, didapatkan tegangan pada out1 = 10,31 V dan out2 = 0,78 V. Pada kondisi ini motor 1 akan berputar berlawanan arah dengan jarum jam.

Pada kondisi input A = 1, B = 1 dan VINH1 = 1, didapatkan tegangan pada out1 = 10,30 V dan out2 = 10,30 V. Pada kondisi ini motor 1 akan berhenti disertai pengereman.

Pada kondisi input A = 0, B = 0 dan VINH1 = 1, didapatkan tegangan pada out1 = 0,76 V dan out2 = 0,78 V. Pada kondisi ini motor 1 akan berhenti disertai pengereman.

Pada kondisi input A = * (0 atau 1), B = * (0 atau 1) dan VINH1 = 0, tidak terdapat tegangan pada out1 maupun out2. Pada kondisi ini motor 1 akan berhenti tanpa disertai pengereman. Kondisi-kondisi diatas berlaku juga pada motor 2 dan motor 3.

BAB V

5 KESIMPULAN DAN SARAN

5.1. Kesimpulan

Dari proses perancangan seperti yang diterangkan diatas, dapat diambil kesimpulan sebagai berikut :

- Pada sensor roda menggunakan optoisolator
- Pada driver sensor roda nilai resistansi sebesar 10 k ohm sebagai resistansi poll down dan menggunakan gerbang NOT sebagai inferter.
- Pada rangkaian mikrokontroller AT89S51 digunakan P3.2 dan P3.3 sebagai port counter sebagai penghitung jumlah pulsa yang dihasilkan oleh rangkaian sensor roda.
- Pada rangkaian driver keypad menggunakan IC 74LS922 dimana hanya untuk mempermudah dalam pengerjaan program dalam mikrokontroller
- Pada rangkaian driver motor DC menggunakan IC L298 dimana pada IC ini hanya mengeluarkan arus maksimal sebesar 4 Ampere dan lebih simple dalam pembuatannya.

5.2. Saran

Pada alat ini masih dapat dikembangkan lebih jauh lagi antara lain penambahan sensor penghalang dimana tidak hanya ditempatkan pada kondisi datar tanpa penghalang tetapi pada apa saja

DAFTAR PUSTAKA

1. John F. Wakerly, DIGITAL DESIGN PRINCIPLES & PRACTICES, Prentice Hall, 2001
2. Kennet J. Ayala, THE 8051 MICROCONTROLLER ARCHITECTURE, PROGRAMMING AND APPLICATION, Pseudo Corp, 1990
3. Malvino, PRINSIP – PRINSIP ELEKTRONIKA, Erlangga, 1994
4. Moh. Ibnu Malik & Anistardi, BEREKSPERIMEN DENGAN MIKROKONTROLER 8031, PT Elex Media Komputindo, 1997

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI T.ELEKTRONIKA

LEMBAR BIMBINGAN SKRIPSI

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3. Jurusan	: T. Elektro S-1
4. Konsentrasi	: T. Elektronika
5. Judul Skripsi	: Perencanaan Dan Pembuatan Alat Otomatis Pembersih Pada Lantai Datar Menggunakan Teknologi Mikrokontroller AT 89S51
6. Tanggal Pengajuan Skripsi	: 26 Februari 2005
7. Selesai Pengajuan Skripsi	: 29 Agustus 2005
8. Pembimbing	: 1. Ir. Erfan A Dahlan 2. M Ibrahim Ashari,ST
9. Telah Dievaluasi Dengan Nilai	: 1. Pembimbing I : 80 : 2. Pembimbing II : 90

Dosen Pembimbing I

Ir. Erfan A Dahlan

Dosen Pembimbing II

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Mengetahui,
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INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGURA-GURA 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Bayu Krisdianto
Nim : 9817050
Masa Bimbingan : 26-Feb-2005 s/d 29-Aug-2005
Judul Skripsi : Perancangan dan pembuatan alat otomatis pembersih pada lantai datar menggunakan teknologi Mikrokontroller AT89S51

NO	Tanggal	Uraian	Paraf Pembimbing
1.	14/07/05	- [illegible]	
2.		- [illegible]	
3.		- [illegible]	
4.		[illegible]	
5.	-	[illegible]	
6.		[illegible]	
7.		- [illegible]	
8.		[illegible]	
9.			
10.			

Malang, 29 - Juli - 2005
Dosen Pembimbing

Ir. Erfan A. Dahlan

Form. S-4a

INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGURA-GURA 2
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FORMULIR BIMBINGAN SKRIPSI

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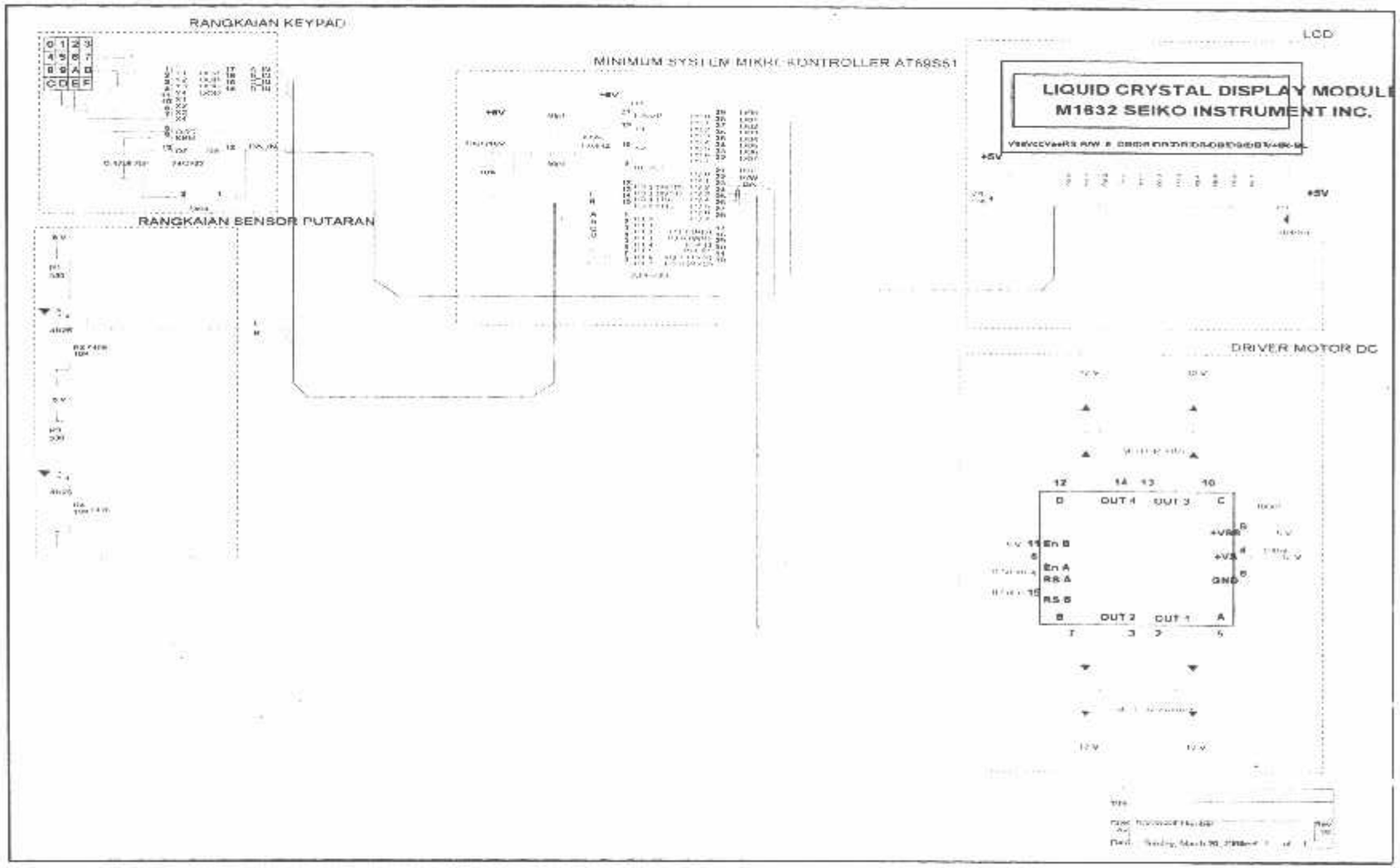
Judul Skripsi : Perancangan dan pembuatan alat otomatis pembersih pada lantai datar menggunakan teknologi Mikrokontroller AT89S51

NO	Tanggal	Uraian	Paraf Pembimbing
1.	4 Juli '05	acc Bab I	
2.	8/07 '05	acc Bab II	
3.	20/07 '05	Revisi Bab III	
4.	20/07 '05	acc bab III	
5.	20/07 '05	acc Bab IV.	
6.	10-8-05	acc makalah Seminar	
7.			
8.			
9.			
10.			

Malang, 29 Sept 2005
Dosen Pembimbing

M. Ibrahim Ashari, ST

Form. S-4a


RANGKAIAN KEYPAD
MINIMUM SYSTEM MIKRO KONTROLLER AT89S51
LCD
LIQUID CRYSTAL DISPLAY MODULE
M1832 SEIKO INSTRUMENT INC.
RANGKAIAN SENSOR PUTARAN
DRIVER MOTOR DC
OUT 4
OUT 3
OUT 2
OUT 1
En B
En A
RS A
RS B
GND
+5V

```
-----------------------------------------
THE CUTTER
P0.0 s/d P0.7 : P2.2ta Bus LCD
P1.0 s/d P1.3 : P2.2ta Keypad (DCBA)
P2.2 : Data Available Keypad
P2.0 : RS
P2.1 : EN
P2.3 : Motor Kanan
P2.4 : Motor Kiri
P2.5 : Motor Pemotong
-----------------------------------------
rg   00h
     RS    bit   P2.0
     EN    bit   P2.1
     PJG   equ   30h
     LBR   equ   31h
     Lcnt  equ   32h
     Rcnt  equ   33h
     KonvL equ   34h
     KonvP equ   35h
*************************************************
art:      clr   P2.7
     sjmp  Lanjut
     org   03h
     clr   P2.3        ;Motor Stop
     clr   P2.4        ;
     clr   P2.5        ;Motor Stop
     clr   P2.6
     setb  P2.7
iam:      nop
     sjmp  Diam
     reti
anjut:
     mov   IE,#81h
     mov   IP,#01h
     call  initLCD
     jnb   P2.2,Start
     mov   R4,#2       ;Tampilan Entry Data
     mov   dptr,#Entry ;keypad
     call  barisa
     call  Keypad
     sjmp  Start

*************************************************
ub  Program Baca Keypad
*************************************************
ypad:     jnb   P2.2,$
     mov   PJG,P1
     mov   A,PJG
     add   A,#030h
     mov   R1,#8Bh
     call  write_inst
     mov   R1,A
     call  write_data
     jb    P2.2,$
     jnb   P2.2,$
```

```
      mov    LBR,P1
      mov    A,LBR
      mov    R6,LBR              ; Init Counter Untuk Lebar
      add    A,#030h
      mov    R1,#0CBh
      call   write_inst
      mov    R1,A
      call   write_data
agi:  jb     P2.2,$
      jnb    P2.2,$
      mov    A,P1
      cjne   A,#0Eh,Cancel
      call   Konversi
      call   Process
      ret
ancel:       cjne  A,#0Ch,Lagi
      jb     P2.2,$
      ajmp   Keypad
      ret
*************************************************
 Sub Program Konversi meter ke pulsa
*************************************************
onversi:
      mov    B,#50h
      mov    A,PJG
      mul    AB
      mov    KonvP,A
      mov    B,#03h
      mov    A,LBR
      mul    AB
      mov    KonvL,A
      ret
*************************************************
  PROCESSING
*************************************************
ocess:
      mov    R4,#1        ;Tampilan Processing
      mov    dptr,#Proc
      call   barisa

gi2:        mov    TMOD,#66h
      setb   TR0
      setb   TR1
      mov    A,TL1
      mov    Rcnt,TL0
      mov    Lcnt,TL1
      cjne   A,35h,Call_Maju    ;KonvP = 35h
      call   Stop
      call   Reset_Counter
nan_Lagi:
      call   Kanan
      mov    A,TL0
      cjne   A,#4Bh,Kanan_Lagi
      call   Stop
      call   Reset_Counter
```

```
agi3:       mov   A,TL1
     mov    Rcnt,TL0
     mov    Lcnt,TL1
     cjne   A,35h,Call_Maju2  ;KonvP = 35h
     call   Stop
     call   Reset_Counter
iri_Lagi:
     call   Kiri
     mov    A,TL1
     cjne   A,#4Bh,Kiri_Lagi
     call   Stop
     call   Reset_Counter

agi4:       mov   A,TL1
     mov    Rcnt,TL0
     mov    Lcnt,TL1
     cjne   A,35h,Call_Maju3  ;KonvP = 35h
     call   Stop
     call   Reset_Counter
anan_Lagi2:
     call   Kanan
     mov    A,TL0
     cjne   A,#4Bh,Kanan_Lagi2
     call   Stop
     call   Reset_Counter

gi5:        mov   A,TL1
     mov    Rcnt,TL0
     mov    Lcnt,TL1
     cjne   A,35h,Call_Maju4   ;KonvP = 35h
     call   Stop
     call   Reset_Counter
ri_Lagi2:
     call   Kiri
     mov    A,TL1
     cjne   A,#4Bh,Kiri_Lagi2
     call   Stop
     call   Reset_Counter
     djnz   R6,Sambung
     ret
mbung:ajmp      Lagi2
ll_Maju:
     call   Sinkron
     call   Maju
     ajmp   Lagi2
ll_Maju2:
     call   Sinkron
     call   Maju
     sjmp   Lagi3
ll_Maju3:
     call   Sinkron
     call   Maju
     sjmp   Lagi4
ll_Maju4:
     call   Sinkron
     call   Maju
```

```
    sjmp  Lagi5
*************************************************
Sub Program Aksi Motor
*************************************************
iju: setb  P2.3          ;Motor Kanan Maju
     setb  P2.4          ;Motor Kiri Maju
     setb  P2.5          ;Motor Pemotong Aktif
     setb  P2.6
     ret
nan:       clr   P2.3          ;Motor Kanan Stop
     setb  P2.4          ;Motor Kiri Maju
     setb  P2.5          ;Motor Pemotong Aktif
     setb  P2.6
     ret
ri: setb  P2.3          ;Motor Kanan Maju
     clr   P2.4          ;Motor Kiri Stop
     setb  P2.5          ;Motor Pemotong Aktif
     setb  P2.6
     ret
op: clr   P2.3          ;Motor Kanan Stop
     clr   P2.4          ;Motor Kiri Stop
     clr   P2.5          ;Motor Pemotong Stop
     clr   P2.6
     ret
set_Counter:
     mov   Lcnt,#00h
     mov   Rcnt,#00h
     mov   TL1,#00h
     mov   TL0,#00h
     ret
inkron:
     mov   A,Lcnt             ;Lcnt = 32h
     cjne  A,33h,Check
     call  Maju
     ret
heck:      subb  A,33h
     jc    Belok_Kanan
     call  Belok_Kiri
     ljmp  Lagi2
elok_Kanan:
     clr   P2.3          ;Motor Kanan Maju
     clr   P2.4          ;
     clr   P2.5          ;Motor Stop
     setb  P2.6
     ljmp  Lagi2
elok_Kiri:
     setb  P2.3          ;Motor Kanan Maju
     clr   P2.4          ;
     clr   P2.5          ;Motor Stop
     clr   P2.6
     ret
*****************************************************
itLCD:
     mov   R1,#03Fh
     acall write_inst
     acall write_inst
```

```
    mov   R1,#0Dh
    acall write_inst
    mov   R1,#06h
    acall write_inst
    mov   R1,#01h
    acall write_inst
    mov   R1,#0Ch
    acall write_inst
    acall tulis
    mov   R1,#8Bh           ;Blinking
    acall write_inst
    mov   R1,#00001101b
    acall write_inst
    ret
ite_inst:
    clr   RS    ;untuk memuliskan
    mov   P0,R1 ;intruksi ke LCD
    setb  EN    ;module
    clr   EN
    acall delay
    ret

ite_data:
    setb  RS    ;untuk memuliskan
    mov   P0,R1 ;data ke LCD
    setb  EN    ;module
    clr   EN
    acall delay
    ret

lay:      mov   R0,#0
lay1: mov R5,#50h
    djnz  R5,$
    djnz  R0,delay1
    ret

elay: mov R2,#030h
1:  acall delay
    djnz  R2,Ld1
    ret

lis:      mov   R4,#2
    mov   DPTR,#CUTTER
risa:     mov   R3,#16
    mov   R1,#80h
    acall write_inst
lis1: clr A
    movc  A,@A+DPTR
    mov   R1,A
    inc   DPTR
    acall write_data
    djnz  R3,Tulis1

risb:     mov   R3,#16
    mov   R1,#0C0h
    acall write_inst
```

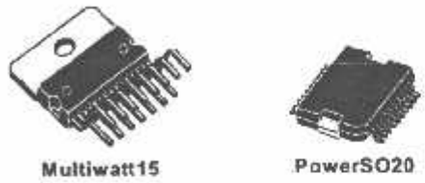
```
ulis2: clr A
     movc  A,@A+DPTR
     mov   R1,A
     Inc   DPTR
     acall write_data
     djnz  R3,Tulis2
     acall Ldelay
     djnz  R4,barisa
     ret

JTTER:      DB    '   THE CUTTER    '
     DB     '   APPLICATION   '
     DB       'T.ELEKTRONIKA S1'
     DB     '    ITN MALANG    '
ıtry:       DB    ' MASUKKAN  LUAS '
     DB     ' AREA  SCANNING '
     DB     ' PANJANG =    mt '
     DB     ' LEBAR   =    mt '
oc: DB      ' AWAS MAU JALAN '
     DB     ' NTAR  KETABRAK '
d
```

L298

DUAL FULL-BRIDGE DRIVER

- OPERATING SUPPLY VOLTAGE UP TO 46 V
- TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)



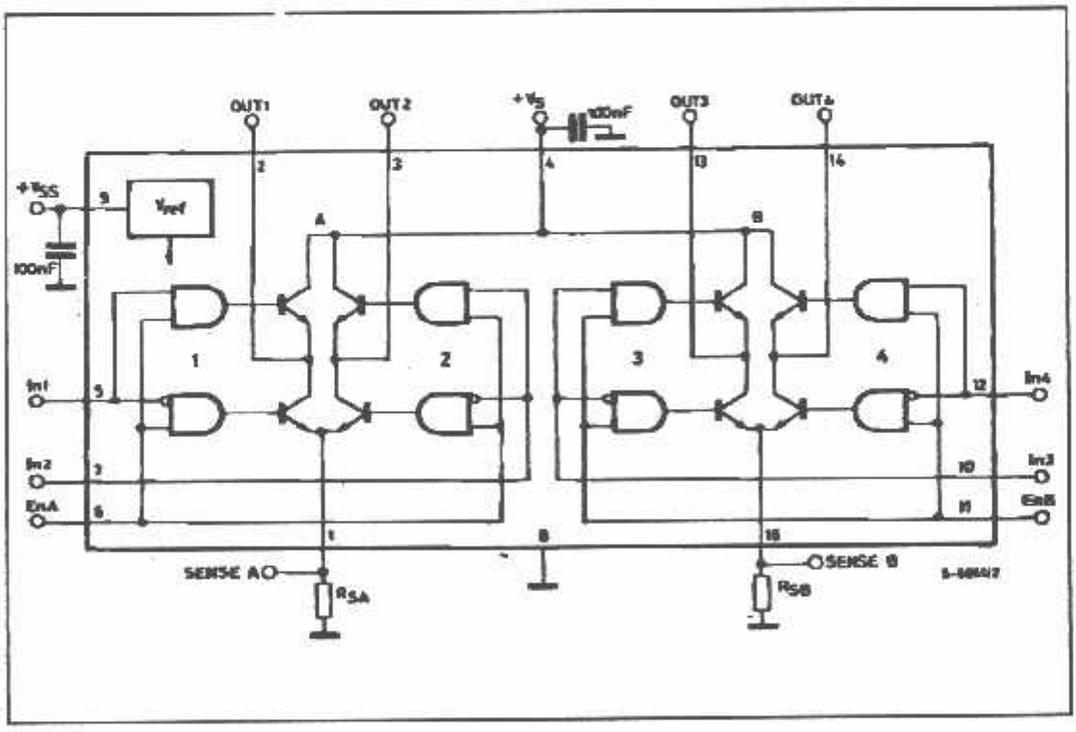
Multiwatt15 PowerSO20

ORDERING NUMBERS : L298N (Multiwatt Vert.)
L298HN (Multiwatt Horiz.)
L298P (PowerSO20)

DESCRIPTION

The L298 is an integrated monolithic circuit in a 15-lead Multiwatt and PowerSO20 packages. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

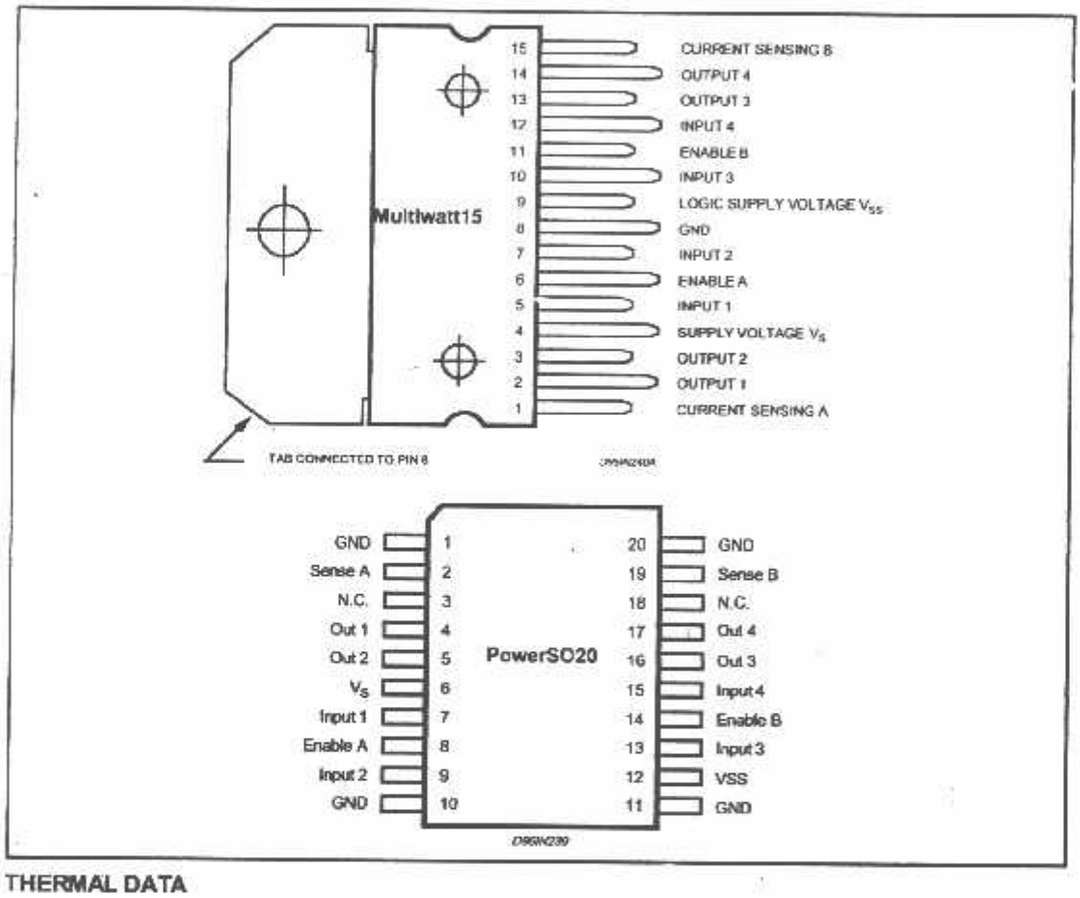
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply	50	V
V_{SS}	Logic Supply Voltage	7	V
V_i, V_{en}	Input and Enable Voltage	–0.3 to 7	V
I_O	Peak Output Current (each Channel) – Non Repetitive (t = 100µs) –Repetitive (80% on –20% off; t_{on} = 10ms) –DC Operation	 3 2.5 2	 A A A
V_{sens}	Sensing Voltage	–1 to 2.3	V
P_{tot}	Total Power Dissipation (T_{case} = 75°C)	25	W
T_{op}	Junction Operating Temperature	–25 to 130	°C
T_{stg}, T_j	Storage and Junction Temperature	–40 to 150	°C

PIN CONNECTIONS (top view)



THERMAL DATA

Symbol	Parameter		PowerSO20	Multiwatt15	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	–	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	13 (*)	35	°C/W

(*) Mounted on aluminum substrate

PIN FUNCTIONS (refer to the block diagram)

MW.15	PowerSO	Name	Function
1;15	2;19	Sense A; Sense B	Between this pin and ground is connected the sense resistor to control the current of the load.
2;3	4;5	Out 1; Out 2	Outputs of the Bridge A; the current that flows through the load connected between these two pins is monitored at pin 1.
4	6	V_S	Supply Voltage for the Power Output Stages. A non-inductive 100nF capacitor must be connected between this pin and ground.
5;7	7;9	Input 1; Input 2	TTL Compatible Inputs of the Bridge A.
6;11	8;14	Enable A; Enable B	TTL Compatible Enable Input: the L state disables the bridge A (enable A) and/or the bridge B (enable B).
8	1,10,11,20	GND	Ground.
9	12	VSS	Supply Voltage for the Logic Blocks. A100nF capacitor must be connected between this pin and ground.
10; 12	13;15	Input 3; Input 4	TTL Compatible Inputs of the Bridge B.
13; 14	16;17	Out 3; Out 4	Outputs of the Bridge B. The current that flows through the load connected between these two pins is monitored at pin 15.
–	3;18	N.C.	Not Connected

ELECTRICAL CHARACTERISTICS (V_S = 42V; V_{SS} = 5V, T_j = 25°C; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 4)	Operative Condition	V_{IH} +2.5		46	V
V_{SS}	Logic Supply Voltage (pin 9)		4.5	5	7	V
I_S	Quiescent Supply Current (pin 4)	V_{en} = H; I_L = 0 V_i = L V_i = H		13 50	22 70	mA mA
		V_{en} = L V_i = X			4	mA
I_{SS}	Quiescent Current from V_{SS} (pin 9)	V_{en} = H; I_L = 0 V_i = L V_i = H		24 7	36 12	mA mA
		V_{en} = L V_i = X			6	mA
V_{iL}	Input Low Voltage (pins 5, 7, 10, 12)		–0.3		1.5	V
V_{iH}	Input High Voltage (pins 5, 7, 10, 12)		2.3		VSS	V
I_{iL}	Low Voltage Input Current (pins 5, 7, 10, 12)	V_i = L			–10	µA
I_{iH}	High Voltage Input Current (pins 5, 7, 10, 12)	V_i = H ≤ V_{SS} –0.6V		30	100	µA
V_{en} = L	Enable Low Voltage (pins 6, 11)		–0.3		1.5	V
V_{en} = H	Enable High Voltage (pins 6, 11)		2.3		V_{SS}	V
I_{en} = L	Low Voltage Enable Current (pins 6, 11)	V_{en} = L			–10	µA
I_{en} = H	High Voltage Enable Current (pins 6, 11)	V_{en} = H ≤ V_{SS} –0.6V		30	100	µA
$V_{CEsat(H)}$	Source Saturation Voltage	I_L = 1A I_L = 2A	0.95	1.35 2	1.7 2.7	V V
$V_{CEsat(L)}$	Sink Saturation Voltage	I_L = 1A (5) I_L = 2A (5)	0.85	1.2 1.7	1.6 2.3	V V
V_{CEsat}	Total Drop	I_L = 1A (5) I_L = 2A (5)	1.80		3.2 4.9	V V
V_{sens}	Sensing Voltage (pins 1, 15)		–1 (1)		2	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_1 (V_i)	Source Current Turn-off Delay	0.5 V_i to 0.9 I_L (2); (4)		1.5		µs
T_2 (V_i)	Source Current Fall Time	0.9 I_L to 0.1 I_L (2); (4)		0.2		µs
T_3 (V_i)	Source Current Turn-on Delay	0.5 V_i to 0.1 I_L (2); (4)		2		µs
T_4 (V_i)	Source Current Rise Time	0.1 I_L to 0.9 I_L (2); (4)		0.7		µs
T_5 (V_i)	Sink Current Turn-off Delay	0.5 V_i to 0.9 I_L (3); (4)		0.7		µs
T_6 (V_i)	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3); (4)		0.25		µs
T_7 (V_i)	Sink Current Turn-on Delay	0.5 V_i to 0.9 I_L (3); (4)		1.6		µs
T_8 (V_i)	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3); (4)		0.2		µs
fc (V_i)	Commutation Frequency	I_L = 2A		25	40	KHz
T_1 (V_{en})	Source Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (2); (4)		3		µs
T_2 (V_{en})	Source Current Fall Time	0.9 I_L to 0.1 I_L (2); (4)		1		µs
T_3 (V_{en})	Source Current Turn-on Delay	0.5 V_{en} to 0.1 I_L (2); (4)		0.3		µs
T_4 (V_{en})	Source Current Rise Time	0.1 I_L to 0.9 I_L (2); (4)		0.4		µs
T_5 (V_{en})	Sink Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (3); (4)		2.2		µs
T_6 (V_{en})	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3); (4)		0.35		µs
T_7 (V_{en})	Sink Current Turn-on Delay	0.5 V_{en} to 0.9 I_L (3); (4)		0.25		µs
T_8 (V_{en})	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3); (4)		0.1		µs

1) 1)Sensing voltage can be −1 V for t ≤ 50 µsec; in steady state V_{sens} min ≥ −0.5 V
2) See fig. 2
3) See fig. 4.
4) The load must be a pure resistor.

Figure 1 : Typical Saturation Voltage vs. Output Current.

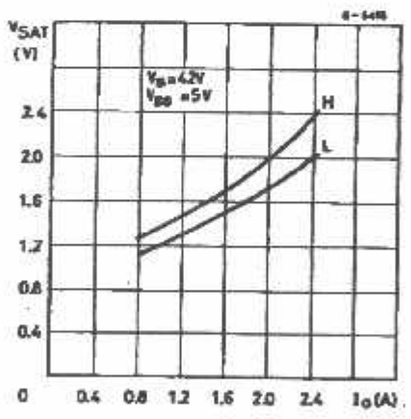
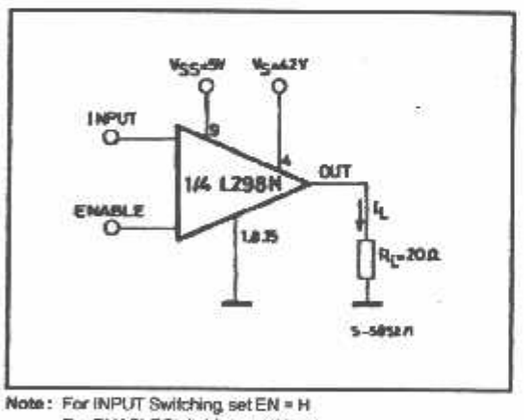


Figure 2 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = H

Figure 3 : Source Current Delay Times vs. Input or Enable Switching.

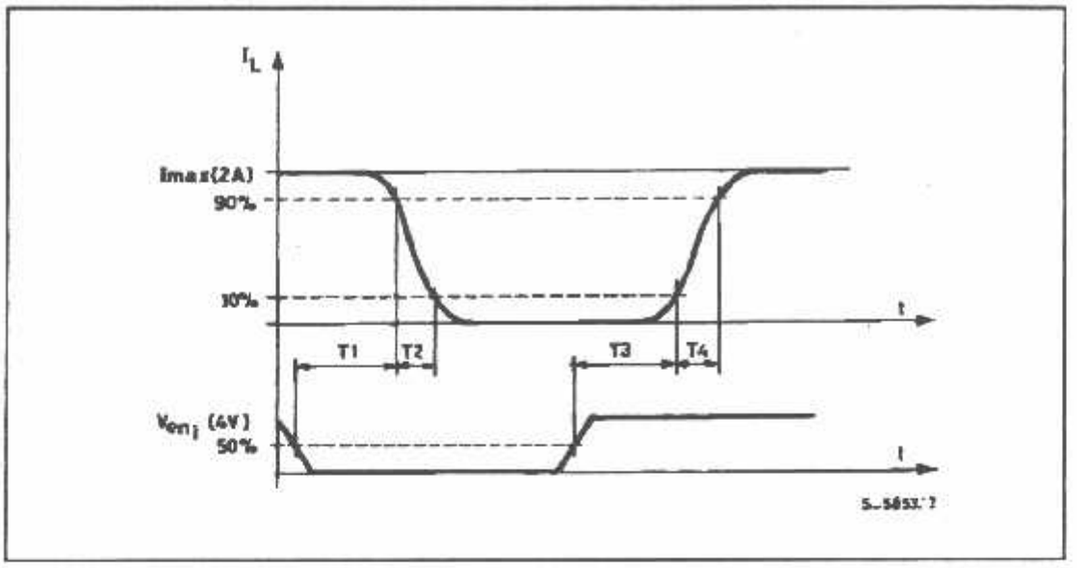
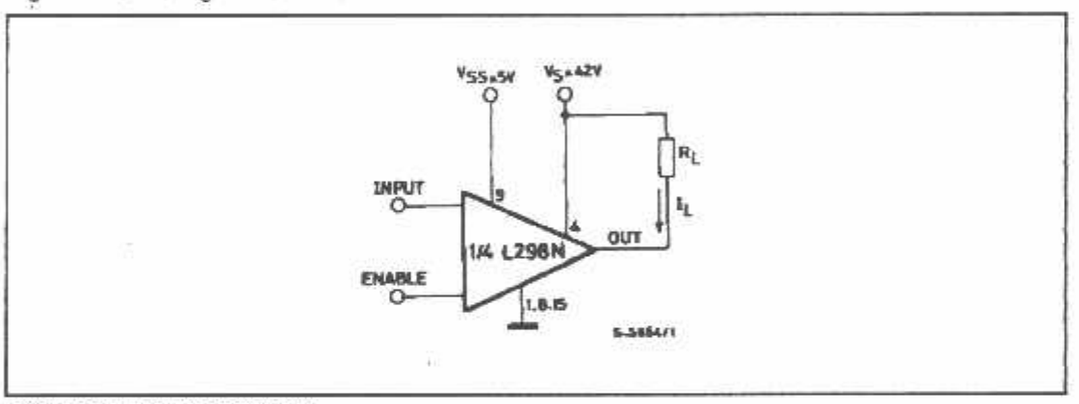


Figure 4 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = L

Figure 5 : Sink Current Delay Times vs. Input 0 V Enable Switching.

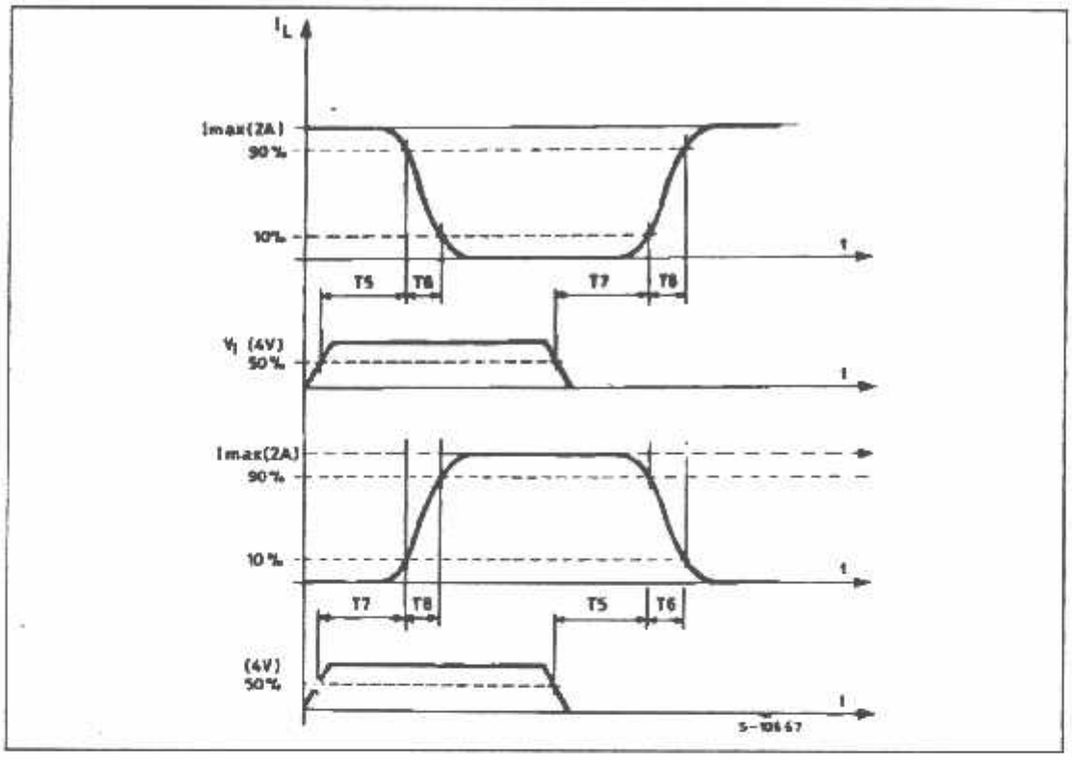
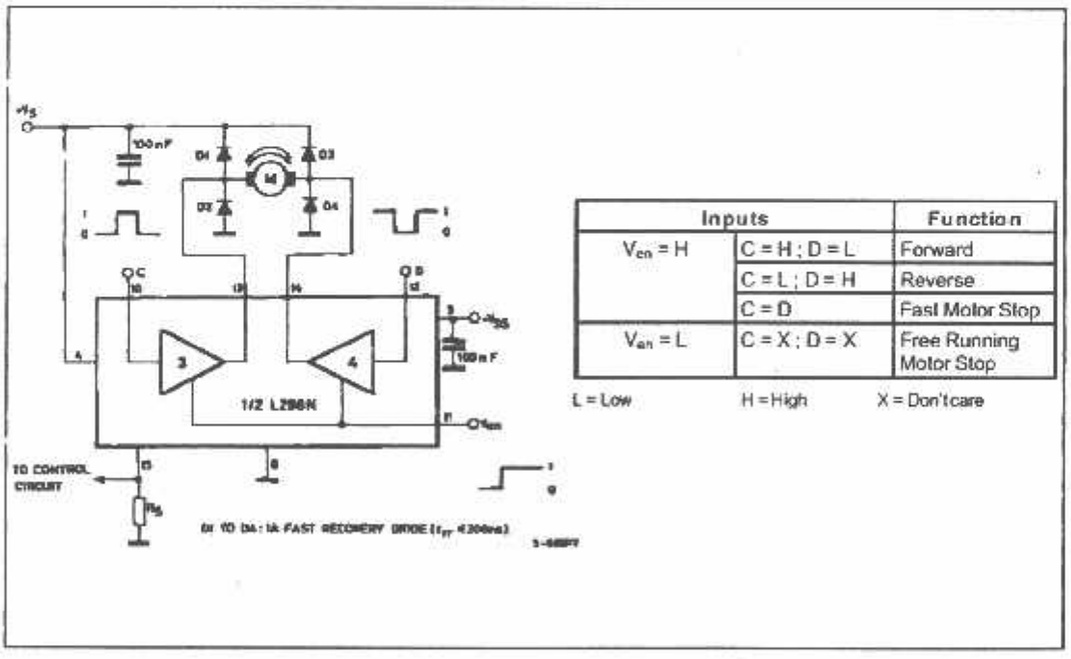


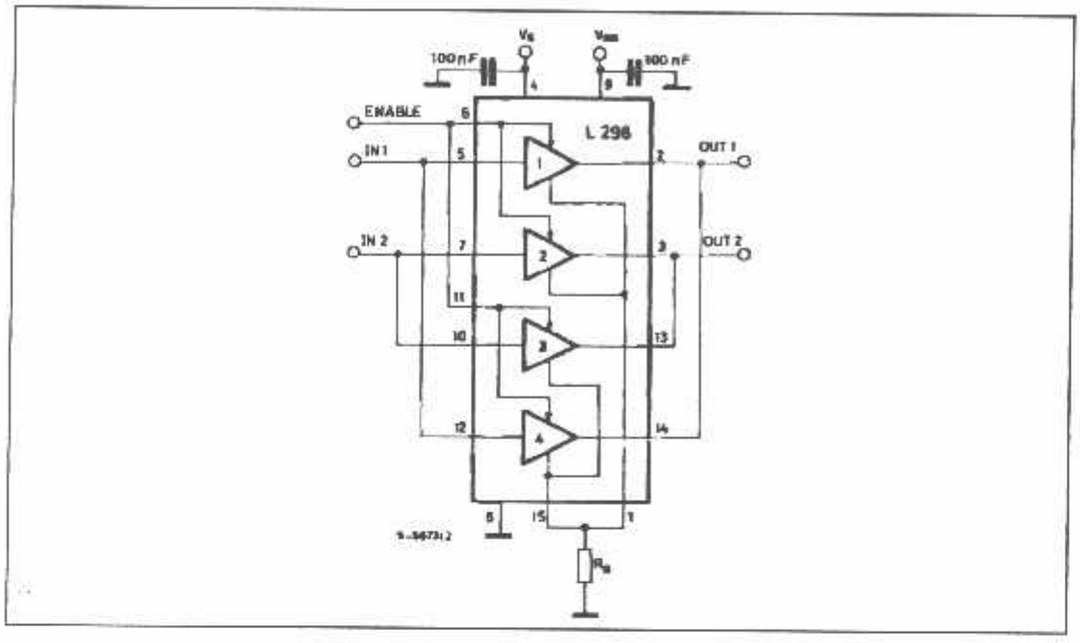
Figure 6 : Bidirectional DC Motor Control.



Inputs		Function
V_{en} = H	C = H ; D = L	Forward
	C = L ; D = H	Reverse
	C = D	Fast Motor Stop
V_{en} = L	C = X ; D = X	Free Running Motor Stop

L = Low H = High X = Don't care

Figure 7 : For higher currents, outputs can be paralleled. Take care to parallel channel 1 with channel 4 and channel 2 with channel 3.



APPLICATION INFORMATION (Refer to the block diagram)

1.1. POWER OUTPUT STAGE

The L298 integrates two power output stages (A ; B). The power output stage is a bridge configuration and its outputs can drive an inductive load in common or differenzial mode, dependingon the state of the inputs. The current that flows through the load comes out from the bridge at the sense output : an external resistor (R_{SA} ; R_{SB}.) allows to detect the intensity of this current.

1.2. INPUT STAGE

Each bridge is driven by means of four gates the input of which are In1 ; In2 ; EnA and In3 ; In4 ; EnB. The In inputs set the bridge state when The En input is high ; a low state of the En input inhibits the bridge. All the inputs are TTL compatible.

2. SUGGESTIONS

A non inductive capacitor, usually of 100 nF, must be foreseen between both Vs and Vss, to ground, as near as possible to GND pin. When the large capacitor of the power supply is too far from the IC, a second smaller one must be foreseen near the L298.

The sense resistor, not of a wire wound type, must be grounded near the negative pole of Vs that must be near the GND pin of the I.C.

Each input must be connected to the source of the driving signals by means of a very short path.

Turn-On and Turn-Off : Before to Turn-ON the Supply Voltage and before to Turn it OFF, the Enable input must be driven to the Low state.

3. APPLICATIONS

Fig 6 shows a bidirectional DC motor control Schematic Diagram for which only one bridge is needed. The external bridge of diodes D1 to D4 is made by four fast recovery elements ($t_{rr} \leq 200$ nsec) that must be chosen of a VF as low as possible at the worst case of the load current.

The sense output voltage can be used to control the current amplitude by chopping the inputs, or to provide overcurrent protection by switching low the enable input.

The brake function (Fast motor stop) requires that the Absolute Maximum Rating of 2 Amps must never be overcome.

When the repetitive peak current needed from the load is higher than 2 Amps, a paralleled configuration can be chosen (See Fig.7).

An external bridge of diodes are required when inductive loads are driven and when the inputs of the IC are chopped ; Shottky diodes would be preferred.

This solution can drive until 3 Amps In DC operation and until 3.5 Amps of a repetitive peak current.

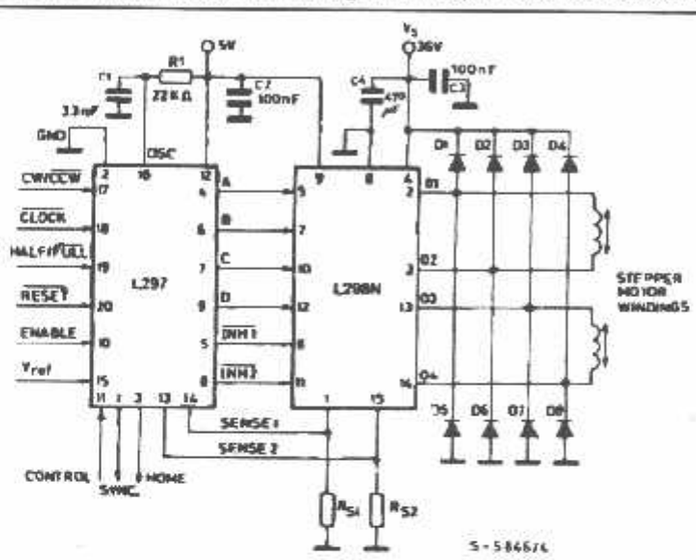
On Fig 8 it is shown the driving of a two phase bipolar stepper motor ; the needed signals to drive the inputs of the L298 are generated, in this example, from the IC L297.

Fig 9 shows an example of P.C.B. designed for the application of Fig 8.

Fig 10 shows a second two phase bipolar stepper motor control circuit where the current is controlled by the I.C. L6506.

Figure 8 : Two Phase Bipolar Stepper Motor Circuit.

This circuit drives bipolar stepper motors with winding currents up to 2 A. The diodes are fast 2 A types.



$R_{S1} = R_{S2} = 0.5\,\Omega$

D1 to D8 = 2 A Fast diodes { $V_F \leq 1.2$ V @ I = 2 A ; trr ≤ 200 ns }

Figure 9 : Suggested Printed Circuit Board Layout for the Circuit of fig. 8 (1:1 scale).

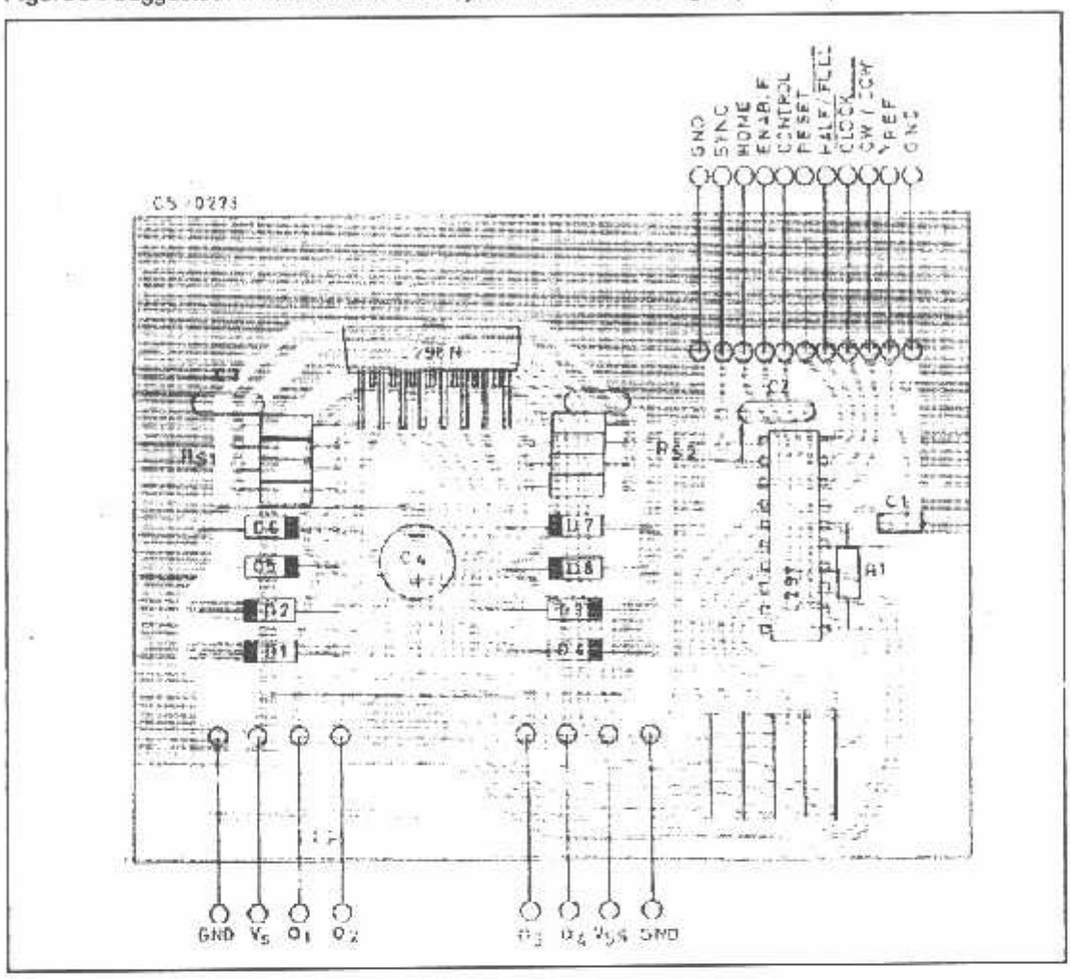
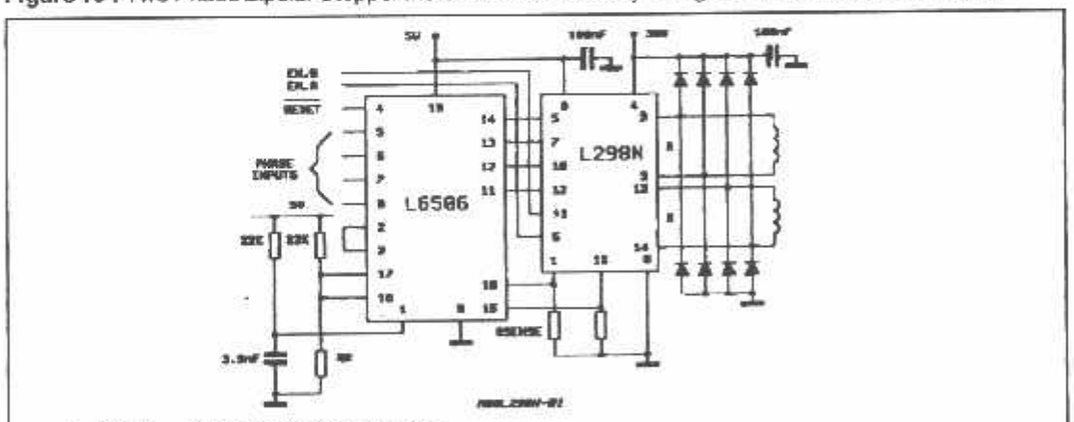


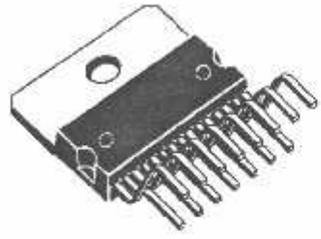
Figure 10 : Two Phase Bipolar Stepper Motor Control Circuit by Using the Current Controller L6506.



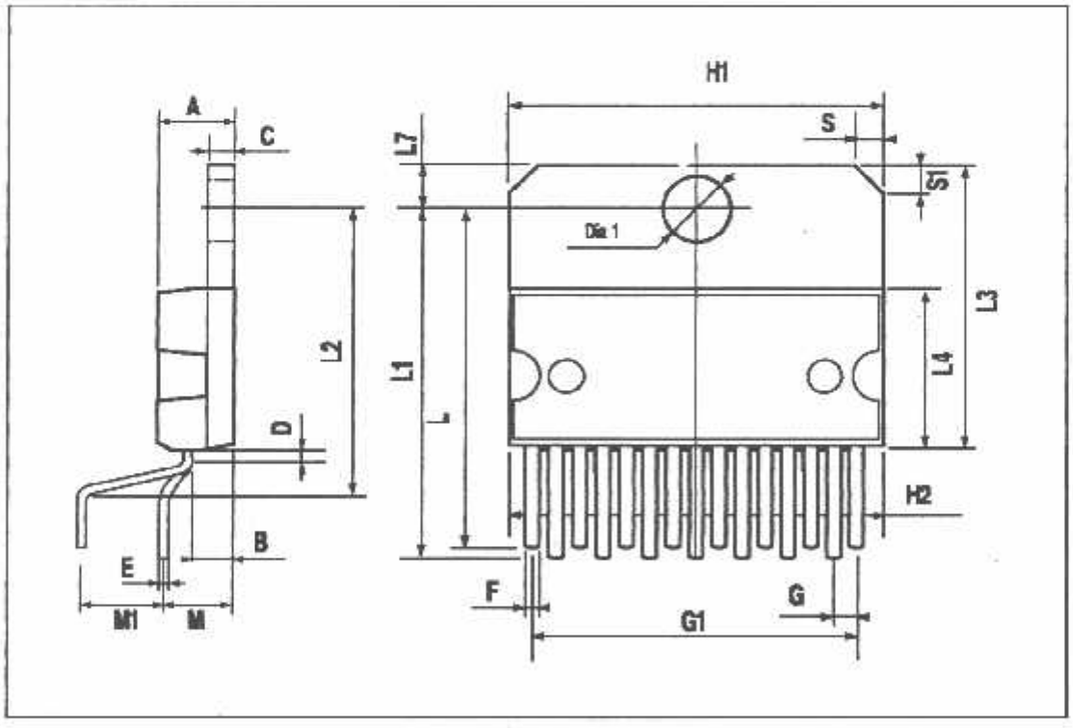
R_R and R_{sense} depend from the load current

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.870	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.63	5.08	5.53	0.182	0.200	0.218
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA

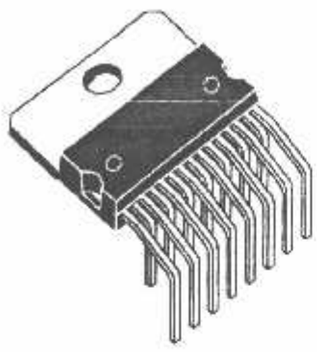


Multiwatt15 V

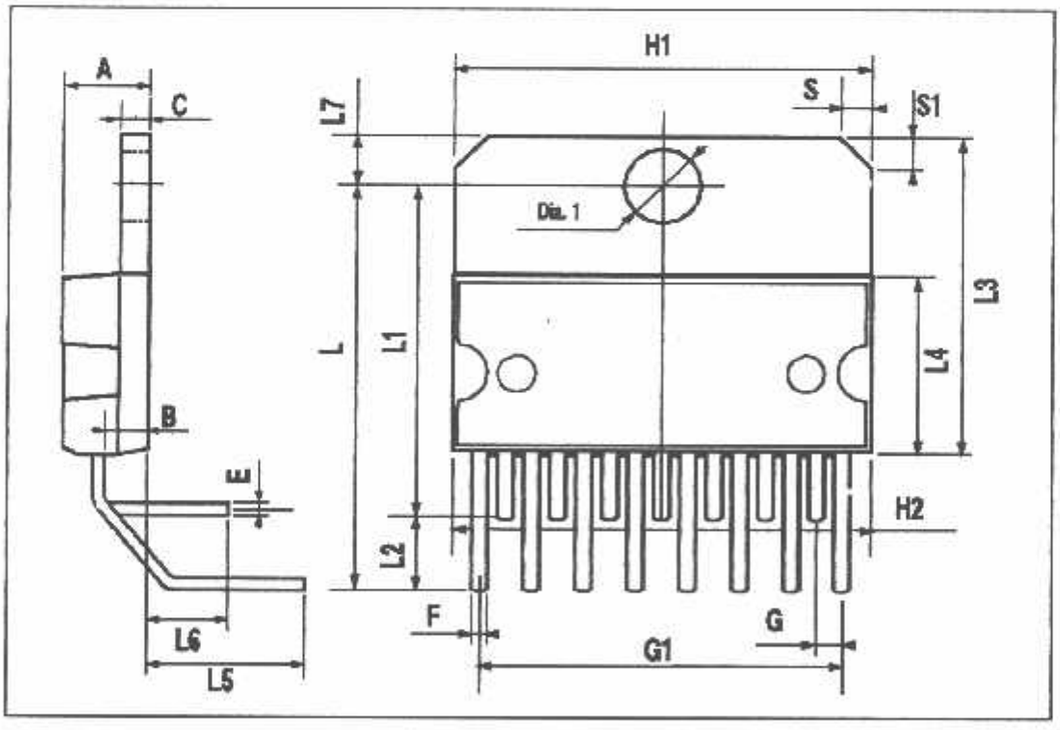


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L		20.57			0.810	
L1		18.03			0.710	
L2		2.54			0.100	
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L5		5.28			0.208	
L6		2.38			0.094	
L7	2.65		2.9	0.104		0.114
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



Multiwatt15 H



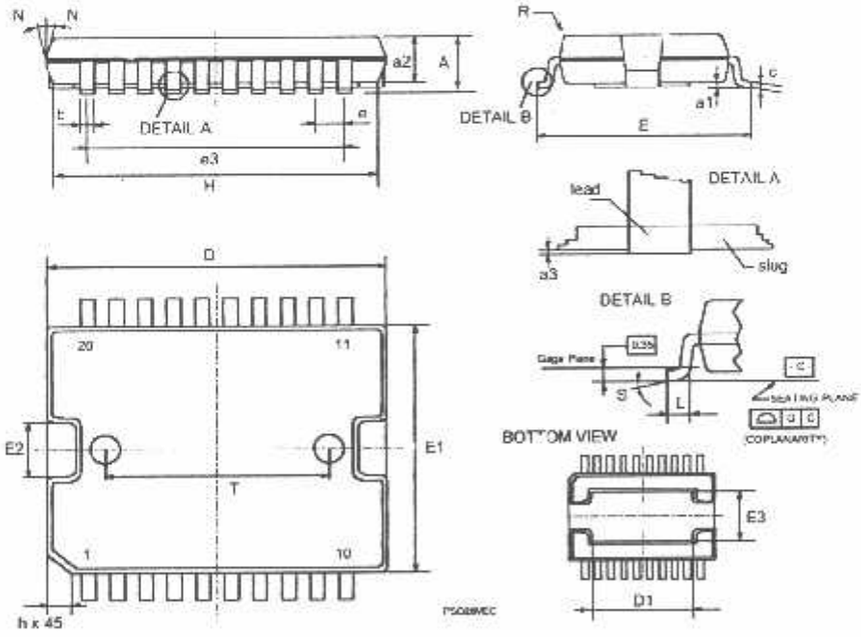
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	10° (max.)					
S	8° (max.)					
T		10			0.394	

(1) "D and E" do not include mold flash or protrusions.
- Mold flash or protrusions shall not exceed 0.15 mm (0.006").
- Critical dimensions: "E", "G" and "a3".

OUTLINE AND MECHANICAL DATA

JEDEC MO-166

PowerSO20



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FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

MM74C922 • MM74C923
16-Key Encoder • 20-Key Encoder

General Description

The MM74C922 and MM74C923 CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key roll-over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The 3-STATE outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- 3-STATE output LPTTL compatible
- Wide supply range: 3V to 15V
- Low power consumption

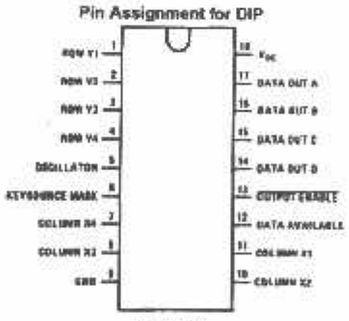
Ordering Code:

Order Number	Package Number	Package Description
MM74C922N	N18A	18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C922WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

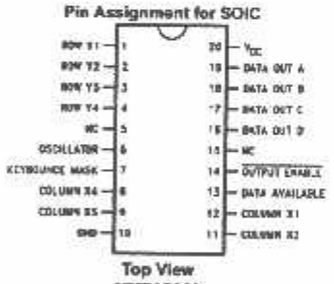
Connection Diagrams

Pin Assignment for DIP



Top View
MM94C922

Pin Assignment for SOIC



Top View
MM74C922

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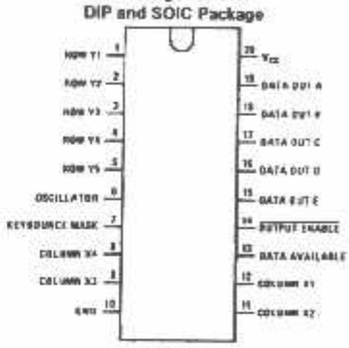
Connection Diagrams (Continued)

Pin Assignment for DIP and SOIC Package



Top View
MM74C923

Truth Tables

(Pins 0 through 11)

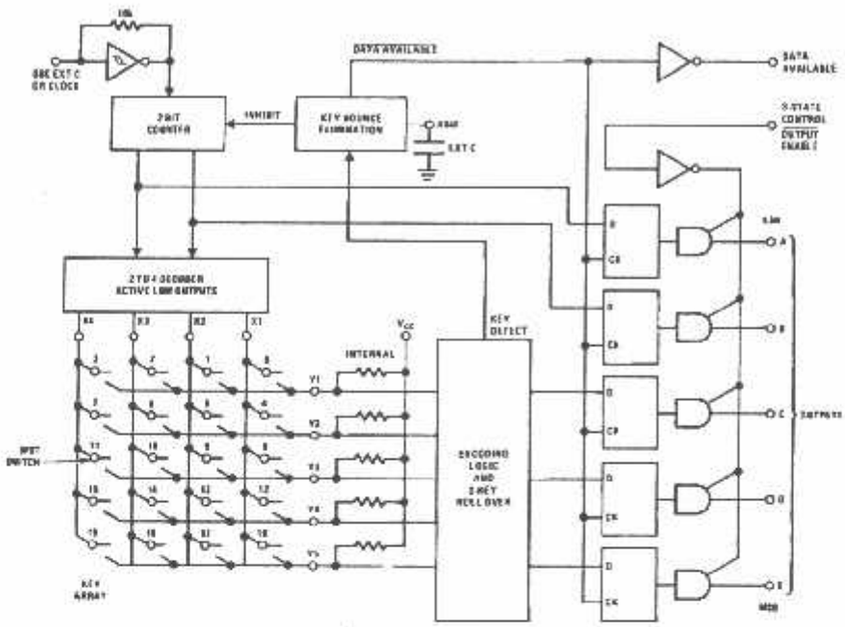
Switch Position		0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4
DATA OUT	A	0	1	0	1	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1	0	0	1	1
	C	0	0	0	0	1	1	1	1	0	0	0	0
	D	0	0	0	0	0	0	0	0	1	1	1	1
	E (Note 1)	0	0	0	0	0	0	0	0	0	0	0	0

(Pins 12 through 19)

Switch Position		12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5(Note 1), X1	17 Y5 (Note 1), X2	18 Y5 (Note 1), X3	19 Y5 (Note 1), X4
DATA OUT	A	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1
	C	1	1	1	1	0	0	0	0
	D	1	1	1	1	0	0	0	0
	E (Note 1)	0	0	0	0	1	1	1	1

Note 1: Omit for MM74C922

Block Diagram



Absolute Maximum Ratings (Note 2)

Voltage at Any Pin	V_{CC} − 0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM74C922, MM74C923	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	260°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, I_{IN} ≥ 0.7 mA	2.0	3.6	4.3	V
		V_{CC} = 10V, I_{IN} ≥ 1.4 mA	6.0	6.8	8.6	V
		V_{CC} = 15V, I_{IN} ≥ 2.1 mA	9.0	10	12.9	V
V_{T-}	Negative-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, I_{IN} ≥ 0.7 mA	0.7	1.4	2.0	V
		V_{CC} = 10V, I_{IN} ≥ 1.4 mA	1.4	3.2	4.0	V
		V_{CC} = 15V, I_{IN} ≥ 2.1 mA	2.1	5	6.0	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V	3.5	4.5		V
		V_{CC} = 10V	8.0	9		V
		V_{CC} = 15V	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V		0.5	1.5	V
		V_{CC} = 10V		1	2	V
		V_{CC} = 15V		1.5	2.5	V
I_{IN}	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	V_{CC} = 5V, V_{IN} = 0.1 V_{CC}		−2	−5	μA
		V_{CC} = 10V		−10	−20	μA
		V_{CC} = 15V		−22	−45	μA
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA	4.5			V
		V_{CC} = 10V, I_O = −10 μA	9			V
		V_{CC} = 15V, I_O = −10 μA	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 μA			0.5	V
		V_{CC} = 10V, I_O = 10 μA			1	V
		V_{CC} = 15V, I_O = 10 μA			1.5	V
R_{ON}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	V_{CC} = 5V, V_O = 0.5V		500	1400	Ω
		V_{CC} = 10V, V_O = 1V		300	700	Ω
		V_{CC} = 15V, V_O = 1.5V		200	500	Ω
I_{CC}	Supply Current Osc at 0V, (one Y low)	V_{CC} = 5V		0.55	1.1	mA
		V_{CC} = 10V		1.1	1.9	mA
		V_{CC} = 15V		1.7	2.8	mA
$I_{IN(1)}$	Logical "1" Input Current at Output Enable	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current at Output Enable	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Except Osc and KBM Inputs	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Except Osc and KBM Inputs	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA, V_{CC} = 4.75V, I_O = −360 μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = −360 μA, V_{CC} = 4.75V, I_O = −360 μA			0.4	V

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8	15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8	16		mA

AC Electrical Characteristics (Note 3)

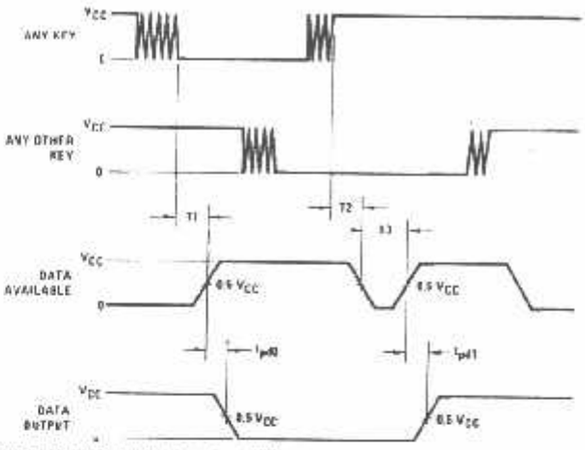
T_A = 25°C, C_L = 50 pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "0" or Logical "1" from D,A	C_L = 50 pF (Figure 1)				
		V_{CC} = 5V		60	150	ns
		V_{CC} = 10V		35	80	ns
		V_{CC} = 15V		25	60	ns
t_{pz0}, t_{pz1}	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	R_L = 10k, C_L = 10 pF (Figure 2)				
		V_{CC} = 5V, R_L = 10k		80	200	ns
		V_{CC} = 10V, C_L = 10 pF		65	150	ns
		V_{CC} = 15V		50	110	ns
t_{p0z}, t_{p1z}	Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	R_L = 10k, C_L = 50 pF (Figure 2)				
		V_{CC} = 5V, R_L = 10k		100	250	ns
		V_{CC} = 10V, C_L = 50 pF		55	125	ns
		V_{CC} = 15V		40	90	ns
C_{IN}	Input Capacitance	Any Input (Note 4)		5	7.5	pF
C_{OUT}	3-STATE Output Capacitance	Any Output (Note 4)		10		pF

Note 3: AC Parameters are guaranteed by DC correlated testing.

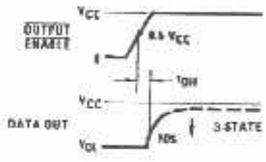
Note 4: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms



T1 = T2 = RC, T3 = 0.7 RC, where R = 10k and C is external capacitor at KBM input.

FIGURE 1.



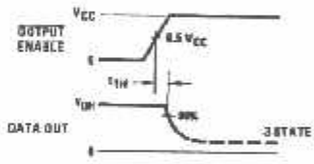
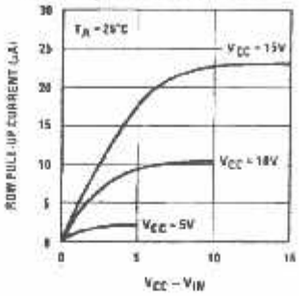


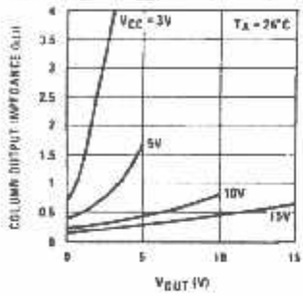
FIGURE 2.

Typical Performance Characteristics

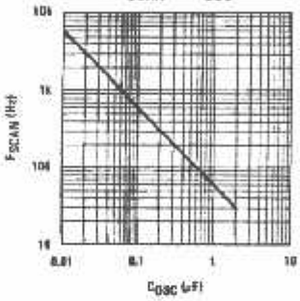
Typical I_{rp} vs V_{IN} at Any Y Input



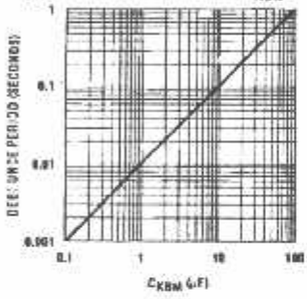
Typical R_{on} vs V_{OUT} at Any X Output



Typical F_{SCAN} vs C_{OSC}

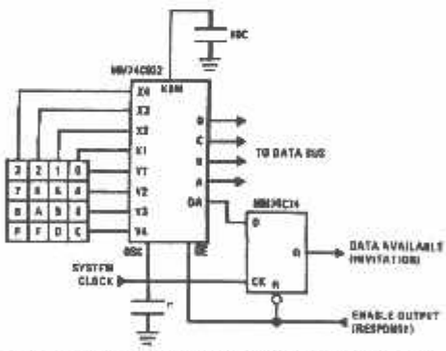


Typical Debounce Period vs C_{KBN}



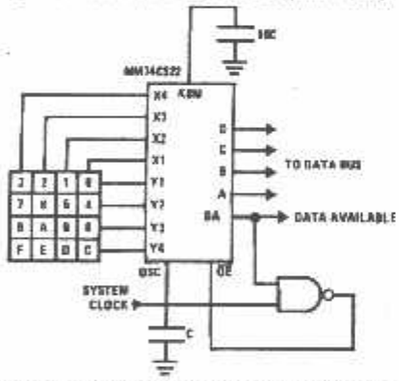
Typical Applications

Synchronous Handshake (MM74C922)



The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz.

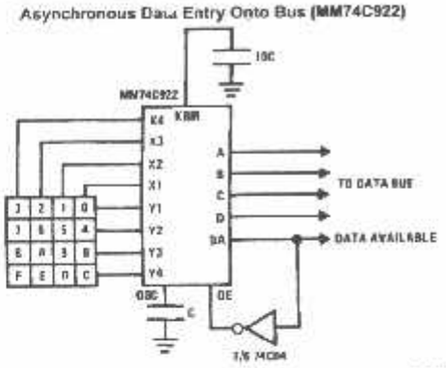
Synchronous Data Entry Onto Bus (MM74C922)



Outputs are enabled when valid entry is made and go into 3-STATE when key is released.

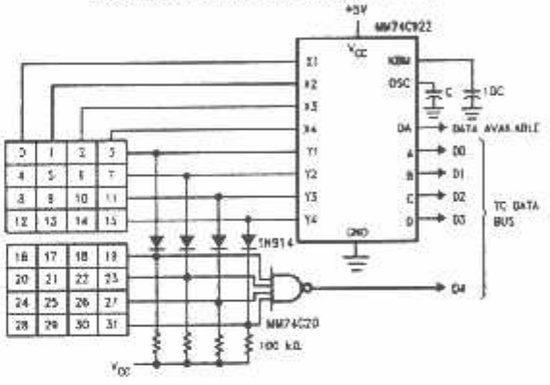
The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz.

Asynchronous Data Entry Onto Bus (MM74C922)



Outputs are in 3-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to 3-STATE.

Expansion to 32 Key Encoder (MM74C922)



Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closer to a 4(MM74C922) or 5(MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor, C_{OSE}, and the key bounce mask capacitor, C_{MSK}. Thus, the MM74C922/MM74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2-4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be output is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

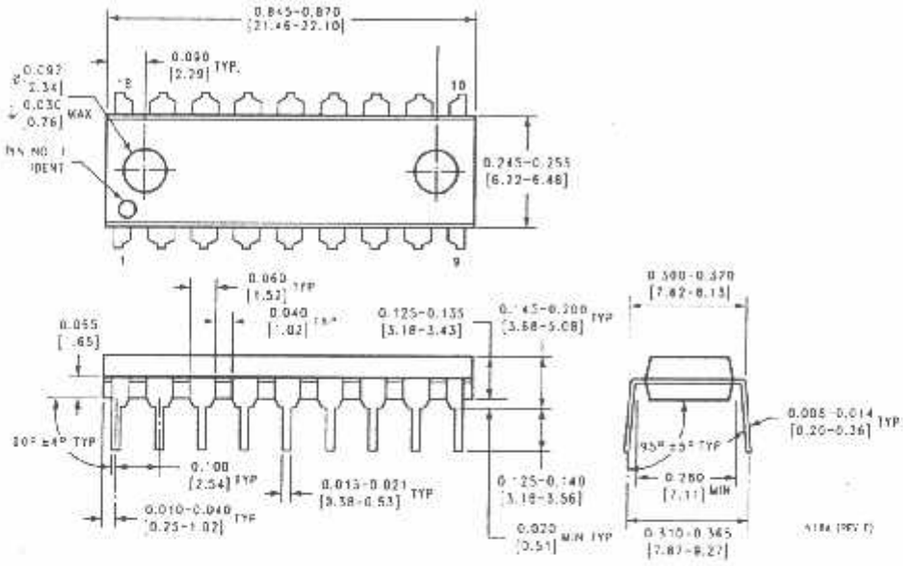
If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

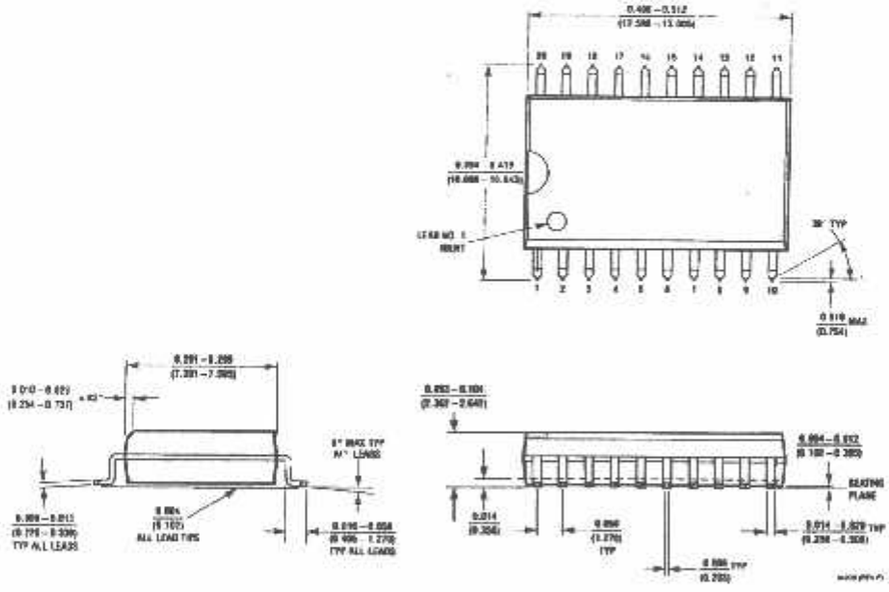
The two-key roll-over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches feed 3-STATE, which is enabled when the Output Enable ($\overline{OE}$) input is taken low.

Physical Dimensions inches (millimeters) unless otherwise noted

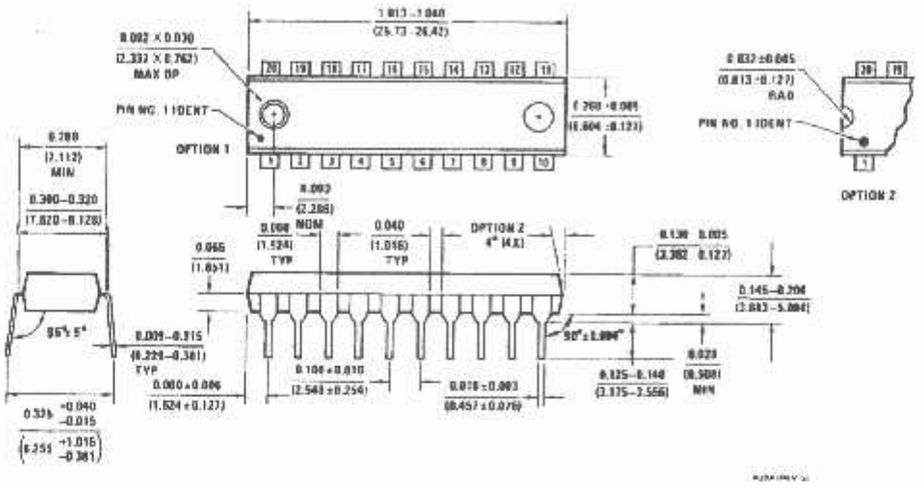


16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16A



20-Lead Plastic Small Outline I.C. Package (M)
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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MOTOROLA

SCHMITT TRIGGERS DUAL GATE/HEX INVERTER

SN54/74LS13 SN54/74LS14

SCHMITT TRIGGERS DUAL GATE/HEX INVERTER

LOW POWER SCHOTTKY

The SN54LS/74LS13 and SN54LS/74LS14 contain logic gates/inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

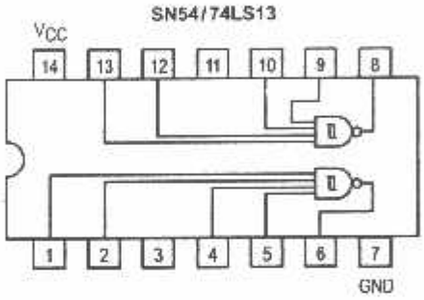
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

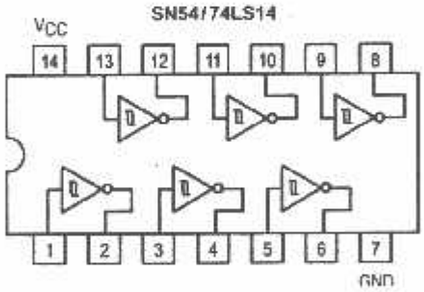
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC AND CONNECTION DIAGRAMS

SN54/74LS13



SN54/74LS14



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

C CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
$'_{T+}$	Positive-Going Threshold Voltage		1.5		2.0	V	V_{CC} = 5.0 V
$'_{T-}$	Negative-Going Threshold Voltage		0.6		1.1	V	V_{CC} = 5.0 V
$_{T+}-V_{T-}$	Hysteresis		0.4	0.8		V	V_{CC} = 5.0 V
$_{IK}$	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
$_{OH}$	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4		V	
$_{OL}$	Output LOW Voltage	54, 74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
$_{+}$	Input Current at Positive-Going Threshold			−0.14		mA	V_{CC} = 5.0 V, V_{IN} = V_{T+}
$_{-}$	Input Current at Negative-Going Threshold			−0.18		mA	V_{CC} = 5.0 V, V_{IN} = V_{T-}
$_{I}$	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
$_{S}$	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
	Power Supply Current						
	Total, Output HIGH	LS13		2.9	6.0	mA	V_{CC} = MAX
		LS14		8.6	16		
	Total, Output LOW	LS13		4.1	7.0		
		LS14		12	21		

1: Not more than one output should be shorted at a time, nor for more than 1 second.

CHARACTERISTICS (T_A = 25°C)

mbol	Parameter	Max LS13	Max LS14	Unit	Test Conditions
$_{H}$	Propagation Delay, Input to Output	22	22	ns	V_{CC} = 5.0 V C_L = 15 pF
$_{L}$	Propagation Delay, Input to Output	27	22	ns	

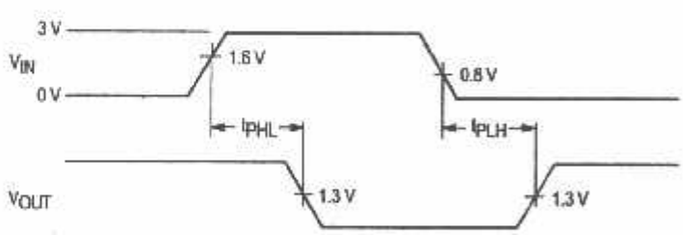


Figure 1. AC Waveforms

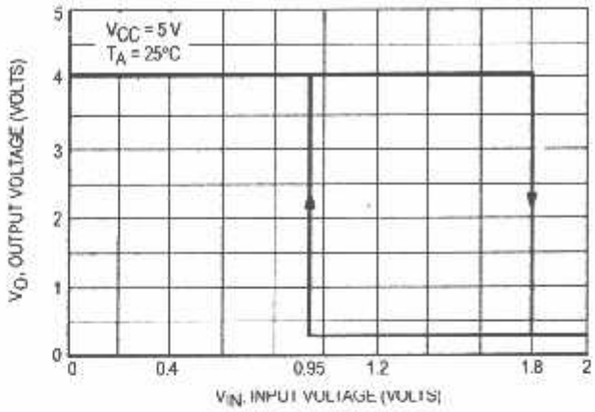


Figure 2. V_{IN} versus V_{OUT} Transfer Function

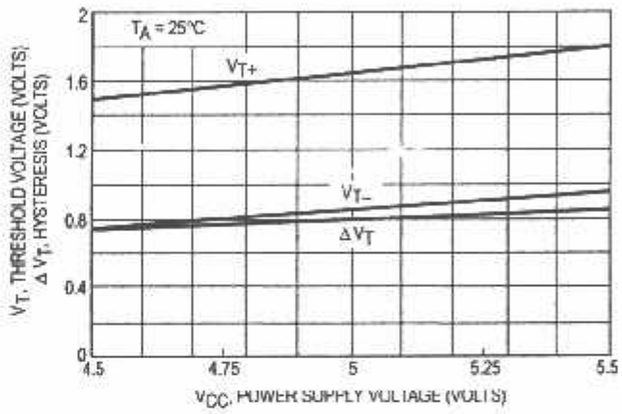


Figure 3. Threshold Voltage and Hysteresis versus Power Supply Voltage

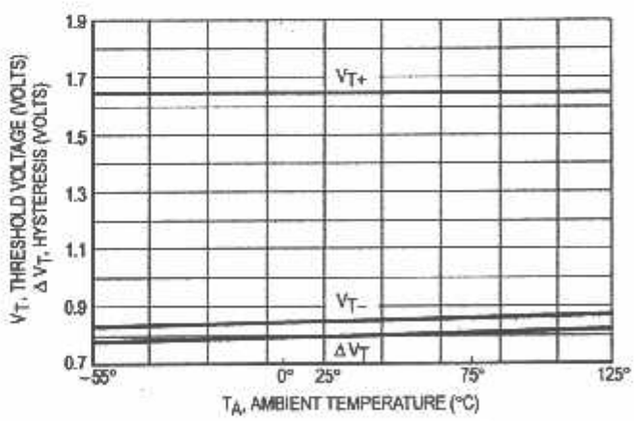


Figure 4. Threshold Voltage Hysteresis versus Temperature

Photodiode/Phototransistor Application Circuit

FUNDAMENTAL PHOTODIODE CIRCUITS

Figures 1 and 2 show the fundamental photodiode circuits.

The circuit shown in Figure 1 transforms a photocurrent produced by a photodiode without bias into a voltage. The output voltage (V_{OUT}) is given as $V_{OUT} = I_P \times R_L$. It is more or less proportional to the amount of incident light when $V_{OUT} < V_{OC}$. It can also be compressed logarithmically relative to the amount of incident light when V_{OUT} is near V_{OC}. (V_{OC} is the open-terminal voltage of a photodiode).

Figure 1 (B) shows the operating point for a load resistor (R_L) without application of bias to the photodiode.

Figure 2 shows a circuit in which the photodiode is reverse-biased by V_{CC} and a photocurrent (I_P) is transformed into an output voltage. Also in this arrangement, the V_{OUT} is given as $V_{OUT} = I_P \times R_L$. An output voltage proportional to the amount of incident light is obtained. The proportional region is expanded by the amount of V_{CC} {proportional region: $V_{OUT} < (V_{OC} + V_{CC})$}. On the other hand, application of reverse bias to the photodiode causes the dark current (I_d) to increase, leaving a voltage of $Id \times R_L$ when the light is interrupted, and this point should be noted in designing the circuit.

Figure 2 (B) shows the operating point for a load resistor R_L with reverse bias applied to the photodiode.

Features of a circuit used with a reverse-biased photodiode are:

- High-speed response
- Wide-proportional-range of output

Therefore, this circuit is generally used.

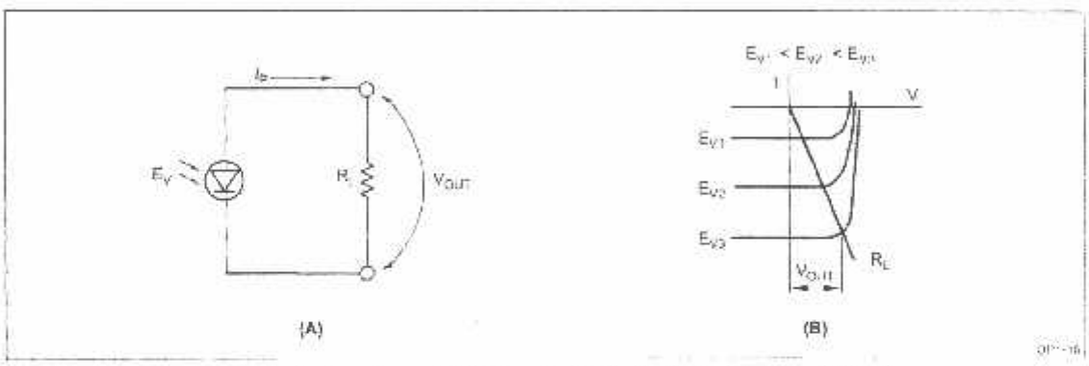


Figure 1. Fundamental Circuit of Photodiode (Without Bias)

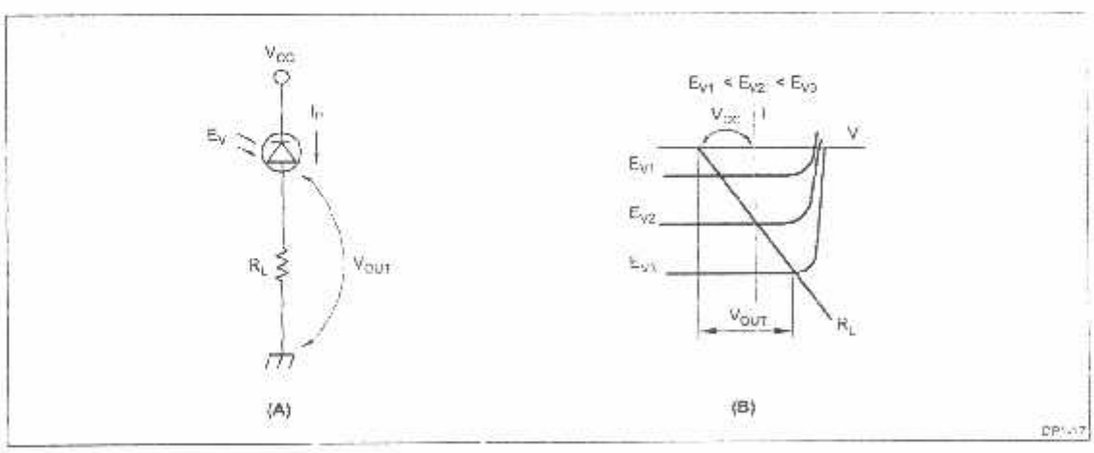


Figure 2. Fundamental Circuit of Photodiode (With Bias)

The response time is inversely proportional to the reverse bias voltage and is expressed as follows:

$r = C_j \times R_L$

$C_j = A(V_D - V_R) - \frac{1}{n}$

C_j: junction capacitance of the photodiode

R_L: load resistor

V_D: diffusion potential (0.5 V - 0.9 V)

V_R: Reverse bias voltage (negative value)

n: 2 - 3

PHOTOCURRENT AMPLIFIER CIRCUIT USING THE TRANSISTOR OF PHOTODIODE

Figures 3 and 4 show photocurrent amplifiers using transistors.

The circuit shown in Figure 3 are most basic combinations of a photodiode and an amplifying transistor. In the arrangement of Figure 3 (A), the photocurrent produced by the photodiode causes the transistor (Tr_1) to decrease its output (V_{OUT}) from high to low. In the arrangement of Figure 3 (B), the photocurrent causes the V_{OUT} to increase from low to high. Resistor R_{BE} in the circuit is effective for suppressing the influence of dard current (I_d) and is chosen to meet the following conditions:

$R_{BE} < V_{ED}/I_d$

$R_{BE} > V_{BE}/\{I_P - V_{CC}/(R_L \times h_{FE})\}$

Figure 4 shows simple amplifiers utilizing negative feedback.

In the circuit of Figure 4 (A), the output (V_{OUT}) is given as:

$V_{OUT} = I_P \times R_1 + I_B \times R_1 + V_{BE}$

This arrangement provides a large output and relatively fast response.

The circuit of Figure 4 (B) has an additional transistor (Tr_2) to provide a larger output current.

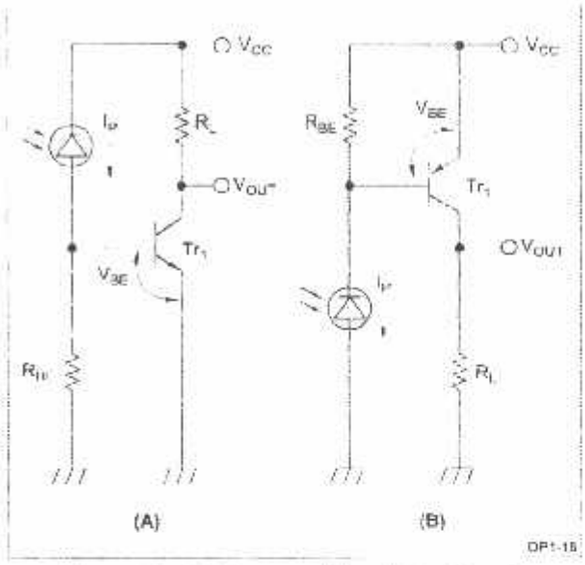


Figure 3. Photocurrent Amplifier Circuit using Transistor

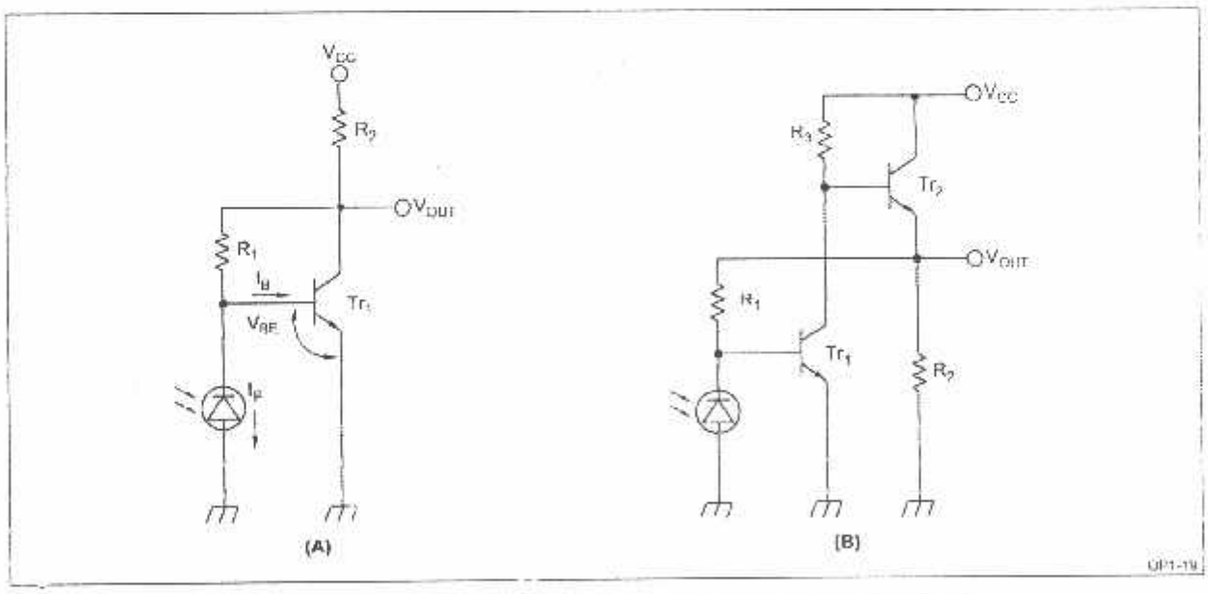


Figure 4. Photocurrent Amplifier Circuit with Negative Feedback

AMPLIFIER CIRCUIT USING OPERATIONAL AMPLIFIER

Figure 6 shows a photocurrent-voltage conversion circuit using an operational amplifier. The output voltage (V_{OUT}) is given as $V_{OUT} = I_F \times R_1$ ($I_P \equiv I_{SC}$). The arrangement utilizes the characteristics of an operational amplifier with two input terminals at about zero voltage to operate the photodiode without bias. The circuit provides an ideal short-circuit current (I_{SC}) in a wide operating range.

Figure 6 (B) shows the output voltage vs. radiant intensity characteristics. An arrangement with no bias and high impedance loading to the photodiode provides the following features:

- Less influence by dark current
- Wide linear range of the photocurrent relative to the radiant intensity.

Figure 5 shows a logarithmic photocurrent amplifier using an operating amplifier. The circuit uses a logarithmic diode for the logarithmic conversion of photocurrent into an output voltage. In dealing with a very wide irradiation intensity range, linear amplification results in a saturation of output because of the limited linear region of the operational amplifier, whereas logarithmic compression of the photocurrent prevents the saturation of output. With its wide measurement range, the logarithmic photocurrent amplifier is used for the exposure meter of cameras.

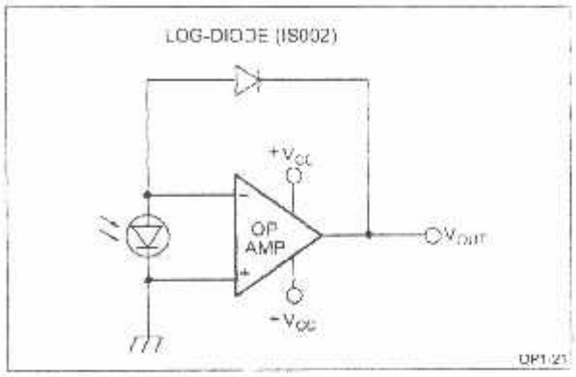


Figure 5. Logarithmic Photocurrent Amplifier using an Operational Amplifier

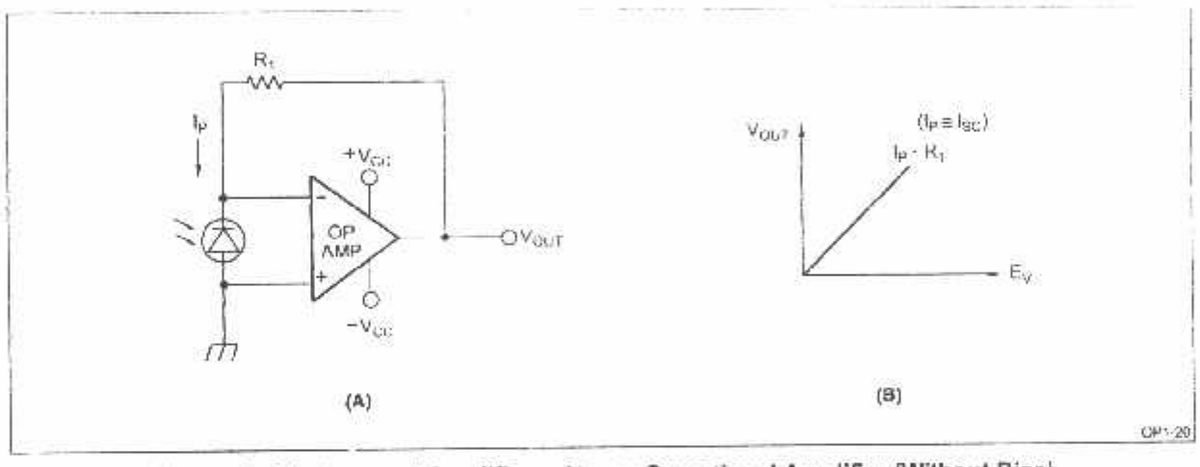


Figure 6. Photocurrent Amplifier using an Operational Amplifier (Without Bias)

LIGHT DETECTING CIRCUIT FOR MODULATED LIGHT INPUT

Figure 7 shows a light detecting circuit which uses an optical remote control to operate a television set, air conditioner, or other devices. Usually, the optical remote control is used in the sunlight or the illumination of a fluorescent lamp. To alleviate the influence of such a disturbing light, the circuit deals with pulse-modulation signals.

The circuit shown in Figure 7 detects the light input by differentiating the rising and falling edges of a pulse signal. To amplify a very small input signal, an FET providing a high input impedance is used.

COLOR SENSOR AMPLIFIER CIRCUIT

Figure 8 shows a color sensor amplifier using a semiconductor color sensor. Two short circuit currents (I_{SC1}, I_{SC2}) conducted by two photodiodes having different spectral sensitivities are compressed logarithmically and applied to a subtraction circuit which produces a differential output (V_{OUT}). The output voltage (V_{OUT}) is formulated as follows:

$$V_{OUT} = \frac{kT}{q} \times \log\left(\frac{I_{SC2}}{I_{SC1}}\right) \times A$$

Where A is the gain of the differential amplifier. The gain becomes $A = R_2/R_1$ when $R_1 = R_3$ and $R_2 = R_4$, then:

$$V_{OUT} = \frac{kT}{q} \times \log\left(\frac{I_{SC2}}{I_{SC1}}\right) \times \frac{R_2}{R_1}$$

The output signal of the semiconductor color sensor is extremely low level. Therefore, great care must be taken in dealing with the signal. For example, low-biased, low-drift operational amplifiers must be used, and possible current leaks of the surface of P.W.B. must be taken into account.

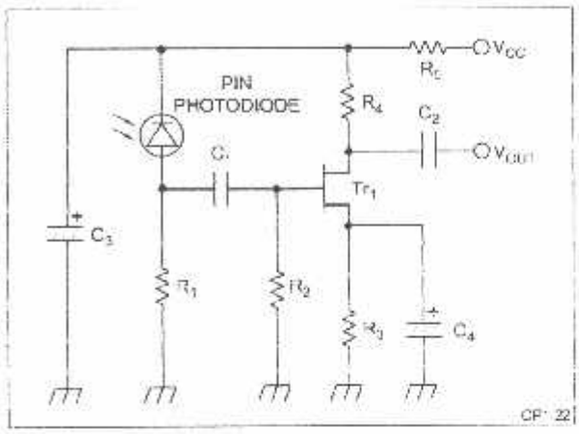


Figure 7. Light Detecting Circuit for Modulated Light Input PIN Photodiode

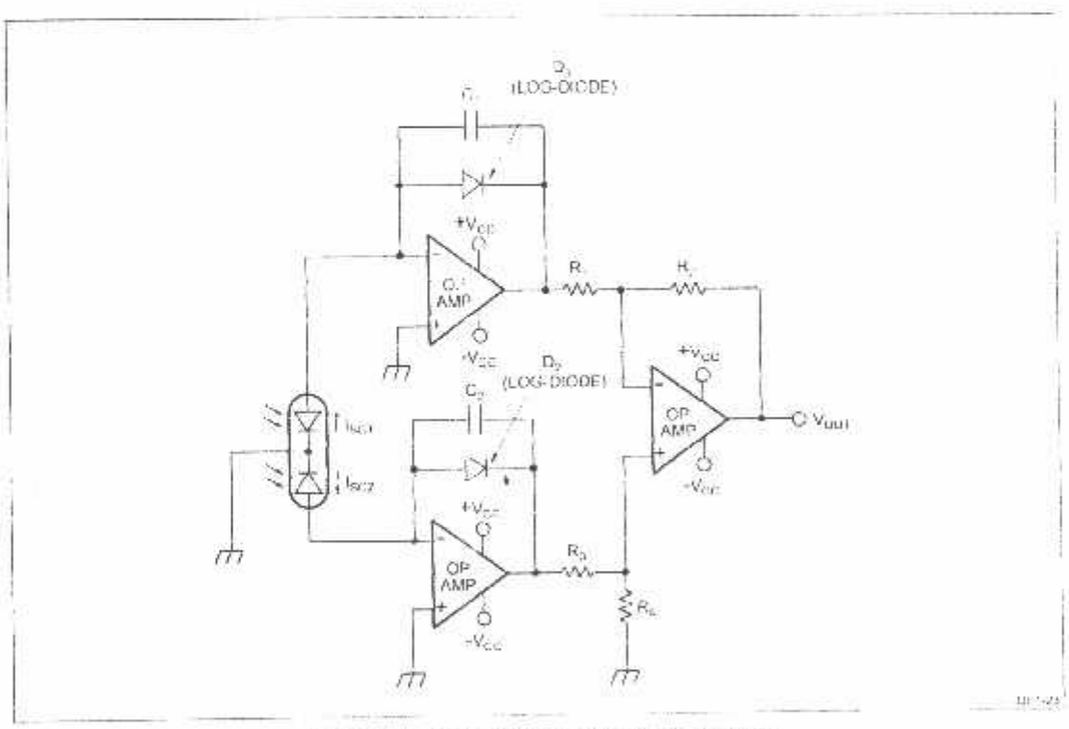


Figure 8. Color Sensor Amplifier Circuit

FUNDAMENTAL PHOTOTRANSISTOR CIRCUITS

Figures 9 and 10 show the fundamental phototransistor circuits. The circuit shown in Figure 9 (A) is a common-emitter amplifier. Light input at the base causes the output (V_{OUT}) to decrease from high to low. The circuit shown in Figure 9 (B) is a common-collector amplifier with an output (V_{OUT}) increasing from low to high in responce to light input. For the circuits in Figure 9 to operate in the switching mode, the load resistor (R_L) should be set in relation with the collector current (I_C) as $V_{CC} < R_L \times I_C$.

The circuit shown Figure 10 (A) uses a phototransistor with a base terminal. A R_{BE} resistor connected between the base and emitter alleviates the influence of a dark current when operating at a high temperature. The circuit shown in Figure 10 (B) features a cascade connection of the grounded-base transistor (Tr_1) so that the phototransistor is virtually less loaded, thereby improving the response.

AMPLIFIER CIRCUIT USING TRANSISTOR

Figure 11 shows the transistor amplifiers used to amplify the collector current of the phototransistor using a transistor (Tr_1). The circuit in Figure 11 (A) increases the output from high to low in response to a light input. The value of resistor R_1 depends on the input light intensity, ambient temperature, response speed, etc., to meet the following conditions:

$R_1 < V_{BE}/I_{CEO}, R_1 > V_{BE}/I_C$

Where I_{CBO} is the dark current of phototransistor and I_C is the collector current.

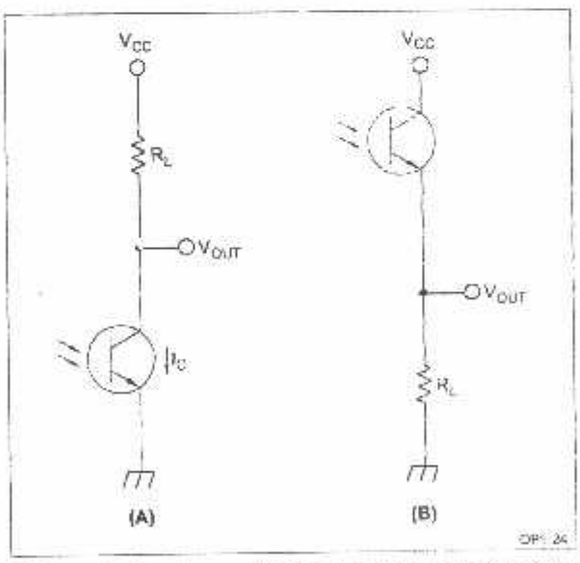


Figure 9. Fundamental Phototransistor Circuit (I)

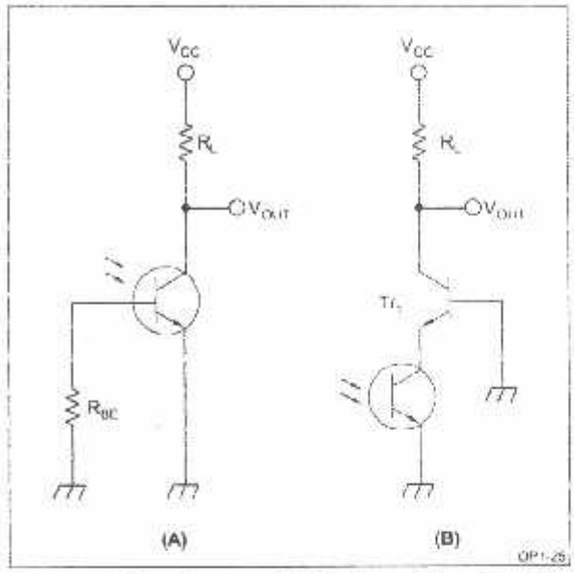


Figure 10. Fundamental Phototransistor Circuit (II)

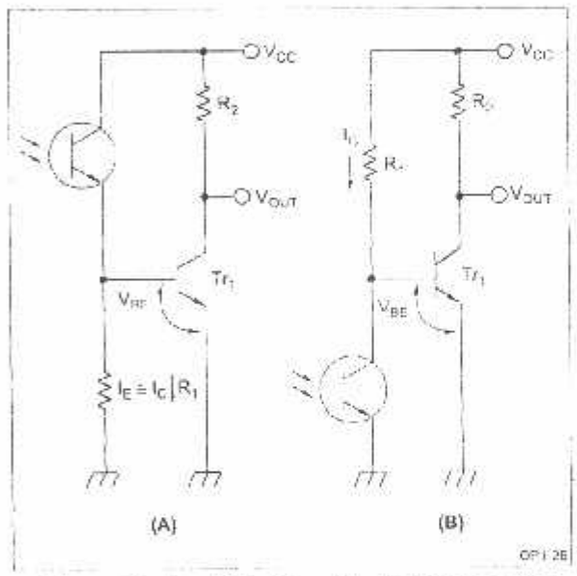


Figure 11. Amplifier Circuit using Transistor

MODULATED SIGNAL DETECTION CIRCUIT

Figure 12 shows the circuits used to detect a modulated signal such as an AC or pulse signal. The phototransistor has a base terminal with a fixed bias through resistors R_1 and R_2. An R_4 emitter resistor maintains the DC output voltage constant. A modulated signal provides a base current through bypass capacitor C causing current amplification so that the signal is greatly amplified.

AMPLIFIER CIRCUIT USING OPERATIONAL AMPLIFIER

Figure 13 shows a current-voltage conversion circuit using an operational amplifier. Its output voltage (V_{OUT}) is expressed as $V_{OUT} = I_C \times R_1$.

The current-voltage conversion circuit for the phototransistor is basically identical to that of the photodiode, except that the phototransistor requires a bias. The circuit shown if Figure 13 (A) has a negative bias (-V) for the emitter against the virtually grounded collector potential. Figure 13 (B) shows the output voltage vs. irradiation intensity characteristics.

AUTO-STROBOSCOPE CIRCUIT

Figure 14 shows the auto-stroboscope circuit of the current cut type. This circuit is most frequently used because of advantages such as continuous light emission and lower battery power consumption.

When the switch is in the ON-state, the SCR_2 and SCR_3 turn on to discharge capacitor C_4 so that the xenon lamp is energized to emit light. The anode of the SCR_2 is then reverse-biased, causing it to turn off and light emission of the xenon lamp ceases. The irradiation time is set automatically in response to variations in the collector current of the phototransistor. This follows the intensity of reflected light from the object and the value of C_1 in the circuit. In other words, the irradiation time is long for a distant object, and short for a near object.

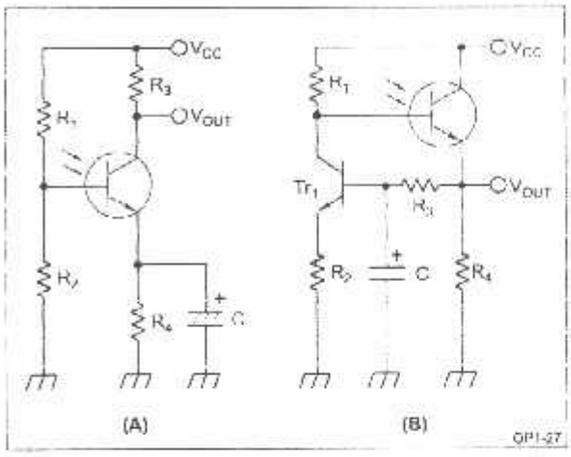


Figure 12. Modulated Signal Detection Circuit

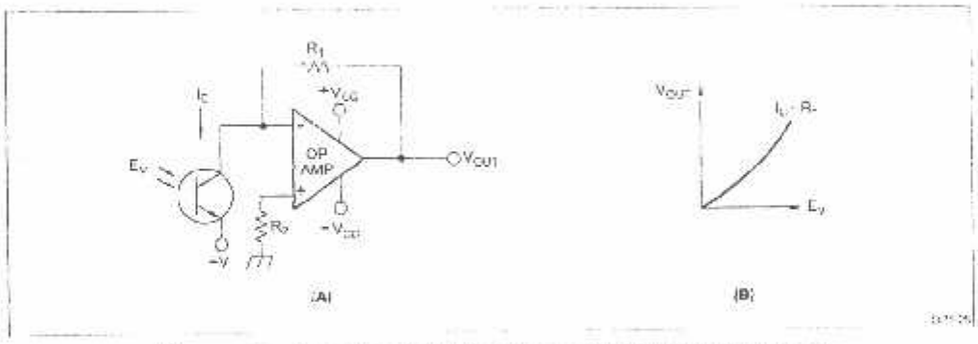


Figure 13. Amplifier Circuit using an Operational Amplifier

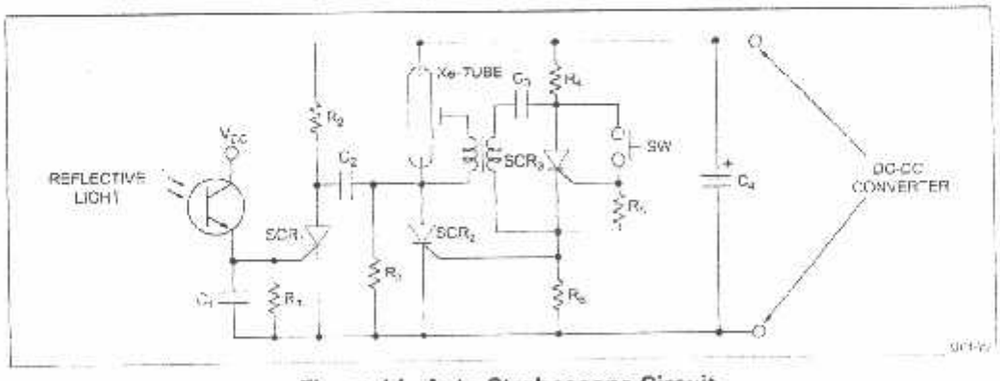


Figure 14. Auto-Stroboscope Circuit

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Photodiode Linearity and Optical Filter Transmission

Introduction

The purpose of this experiment is to demonstrate the operating characteristics of a photodiode detector and the properties of commonly-used optical filters. A very useful property of a detector is linearity, i.e. an output signal that is proportional to the intensity of light falling on the detector. Photodiodes are found to be linear over a wide range of intensities (about 10^7). Your first task in this experiment will be to verify the linearity of the photodiode, although over a smaller range of intensities. The second part of the experiment is a measurement the transmission properties of a set of optical filters, i.e. the fraction of light that each filter lets through as a function of wavelength. You will be using standard U, B, V, R, and I filters which are widely used in optical photometry.

Experimental Setup and Procedure

Photodiode Linearity

The detector is a PIN silicon photodiode (United Detector Technology Model 020A) mounted in a small rectangular box which is in turn mounted on a metal plate for mechanical stability. The diode mount resides inside a large, rectangular wooden box (3′ × 1′ × 1′). The box is painted black on the inside and has a lid so that it can isolate the apparatus from stray light in the room. When the photodiode is illuminated it produces a current which is measured with a Keithley electrometer (a fancy ammeter). The diode is connected to the electrometer through a pair of bulkhead connectors at the end of the box. At the other end another set of bulkhead connectors allow the quartz lamp to draw power from a transformer that sits outside the box. The arrangement is shown schematically in Figure 1.

After making checking that everything is connected properly, turn on the quartz lamp with the switch located on the transformer outside the box. Set the electrometer to read current in the μA (10^{-6} A) range. Adjust the multiplier knob so that when the quartz lamp is up close to the photodiode, the electrometer reads close to the maximum value that it can read. In the course of making measurements do not change the Ampère range switch to nA or anything else. This will change the input impedance of the electrometer and shift it to a different part of the current *vs* voltage curve. **All measurements of current should be made with the lid firmly closed. The current may take a few seconds to reach its final value after the lid is closed; wait for it to settle down before reading it off the meter.**

To adjust the intensity of light illuminating the photodiode move the lamp back and forth and measure its distance with the ruler. In addition to moving the lamp back and forth you can also insert neutral density filters in front of the lamp to reduce the intensity even further. There are three different filters available which produce an attenuation of 10^{-1}, 10^{-2}, and 10^{-4}. You should verify the attenuation produced by each filter experimentally, to be on the safe side. By combining these two techniques you can illuminate the photodiode with light spanning a fairly wide range of intensities.

When making measurements you should take proper account of any background current. Background current is current produced by the photodiode which does not result from direct illumination by the lamp. It could result from thermal noise in the material of the photodiode or from scattered light within the box. Any shiny, metal objects inside the box will scatter light and increase the background, so you should not keep any optical components in the box other than what you are using. To measure the background current you can put something between the lamp and the photodiode to stop direct light from reaching the photodiode. Then close the lid and read off any residual current produced by the photodiode. This background measurement must be made every time to change the configuration by moving the lamp or adding a neutral density filter.

Make 10 to 15 measurements of the current produced in the photodiode trying to sample as wide a range of light intensities as possible. Make sure to measure the background current *each time* and subtract it from the final current. Also, estimate the uncertainty in the intensity and in the current for each measurement. Of course, you cannot know the *absolute* intensity of the light falling on the photodiode but you should be able to determine the *relative* intensity. In your report you should explain how you determined the relative intensity (i.e., what is it relative to?). Make a plot of the current *vs* the relative intensity with error bars and check if you can fit a straight line through it by eye and measure its slope.

You should also try a quantitative assessment of the linearity of the photodiode using the χ^2 test. To simplify this exercise, ignore the errors in the intensity and use only the errors in the current. If the relationship between the current, I, and the illuminating flux, F, is of the form $I = aF + b$, then the coefficients can be determined by a least squared method through the formulae:

$$a = \frac{1}{\Delta}\left\{\left(\sum_{i=1}^{n}\frac{1}{\sigma_i^2}\right)\left(\sum_{i=1}^{n}\frac{F_iI_i}{\sigma_i^2}\right) - \left(\sum_{i=1}^{n}\frac{F_i}{\sigma_i^2}\right)\left(\sum_{i=1}^{n}\frac{I_i}{\sigma_i^2}\right)\right\}$$

and

$$b = \frac{1}{\Delta}\left\{\left(\sum_{i=1}^{n}\frac{F_i^2}{\sigma_i^2}\right)\left(\sum_{i=1}^{n}\frac{I_i}{\sigma_i^2}\right) - \left(\sum_{i=1}^{n}\frac{F_i}{\sigma_i^2}\right)\left(\sum_{i=1}^{n}\frac{F_iI_i}{\sigma_i^2}\right)\right\},$$

where

$$\Delta = \left(\sum_{i=1}^{n}\frac{1}{\sigma_i^2}\right)\left(\sum_{i=1}^{n}\frac{F_i^2}{\sigma_i^2}\right) - \left(\sum_{i=1}^{n}\frac{F_i}{\sigma_i^2}\right)^2.$$

In the above formulae, n is the number data points and F_i, I_i and σ_i denote the illuminating flux, current, and error bar on the current in the ith measurement. Once the coefficients a and b have been determined, you can apply the χ^2 test to see if the best-fitting straight line is indeed consistent with the data. The definition of the reduced χ^2 for this particular straight-line fit is

$$\chi_r^2 = \frac{1}{D}\sum_{i=1}^{n}\frac{(I_i - aF_i - b)^2}{\sigma_i^2},$$

where D is the number of degrees of freedom (number of data points minus the number of free parameters). How many free parameters are there in this case? What values of χ^2 or χ^2_r would indicate to you that a straight line is consistent with the data?

The above sums may be somewhat tedious to perform with a calculator, so you may have to resort to a computer. If you need to use a computer in the department talk to your instructor or T.A.

Optical Filter Transmission

Now that you have verified that the photodiode responds linearly to the intensity of illuminating light you can use it as a tool to measure the transmission through a set of filters as a function of wavelength. The basic principle behind this measurement is that when a filter is inserted into the beam it attenuates the light that reaches the photodiode. By measuring the intensity of the light with and without the filter in the beam the transmission properties of the filter can be determined. The transmission as a function of wavelength can be studied with the help of a monochromator, a device which uses a curved grating to select only light of a specific wavelength, which is allowed to exit the device. There is a crank on the side of the monochromator box that is used to select the wavelength. The selected wavelength is displayed on the top of the box in nanometers (1 nm = 10 Å).

The same wooden box used in the previous part of the experiment is used in this part too. However the arrangement of the apparatus inside the box is different. The new arrangement is shown in Figure 2. Light from the quartz lamp is focused by a lens onto the slit at the entrance of the monochromator. The next lens takes the light from the exit slit of the monochromator and focuses it onto the photodiode. An aluminum filter holder, which also acts as a colimator, is mounted in front of the quartz lamp housing. The purpose of the assembly of lenses is to direct all the light from the lamp to the monochromator entrance aperture and from the monochromator exit aperture to the photodiode.

You should take extra care when setting up the apparatus. Make sure that the light beam is well-aligned and well-focussed at the entrance aperture of the monochromator and at the face of the photodiode. You can use a piece of paper as a screen to trace the light path and verify the alignment. Whenever you make any change to the setup (e.g., when you change filters) there is a chance that the alignment is disturbed, so check it again before making any measurements. Since the whole point of this experiment is to measure the attenuation of light by the filters, any loss of light for other reasons, such as misalignment or poor focus, will introduce an error in the results.

Another potential source of error is the background current in the photodiode. The discussion of background current given in the photodiode linearity experiment applies here as well. Make sure to measure the background every time you change the filter (there is no need to re-measure the background if you are only adjusting the wavelength setting of the monochromator).

The first set of measurements you need to make are of the intensity of the unfiltered light from the lamp as a function of wavelength. Make measurements every 30 nm, starting at 300 nm and going up to 1020 nm. Follow all of the precautions mentioned above and in the previous section (as well as any other precautions that may seem reasonable) and try to estimate the typical uncertainty in your measurements.

When you finish the first set of measurements insert a filter into the filter holder, check the beam alignment, measure the background and repeat the whole series of measurements all over again *at the exact same wavelengths*. Measure as many filters as time permits, in the order I, R, V, B, U. If you get as far as the B and U filters you should exercise extra care with them because their transmission efficiency is low and so is the apparent intensity of the unfiltered light at those wavelengths. As a result, good measurements of the background are very important.

Construct transmission curves for the filters that you measured by dividing the filtered intensity by the unfiltered intensity, wavelength by wavelength. Plot the transmission curves *and their error bars*. From the plots determine the full width at half maximum of the filter passband. Use the measured transmission efficiencies to determine a transmission-weighted mean wavelength for each filter. The transmission-weighted mean wavelength is the first moment of the transmission curve (recall the definition of the first moment of a *properly normalized* distribution). Finally, contemplate the following questions and write your thoughts in the report

(a) Do the transmission curves that you determined depend in any way on the spectrum of the quartz lamp or the detection efficiency of the photodiode? Explain.

(b) Does the measured intensity of the unfiltered light as a function of wavelength represent the spectrum of the quartz lamp? Explain.

Lab Report

Your lab report should contain a *brief* summary of the experimental setup and procedure and a clear presentation of the results. You should answer all the little questions that are scattered around in the text and carry out all the exercises associated with the analysis of the data. The accuracy of the measurements is a major issue in this experiment so you should include a discussion of the potential sources of error, what you did to minimize their impact, and an assessment of the uncertainty in your results.

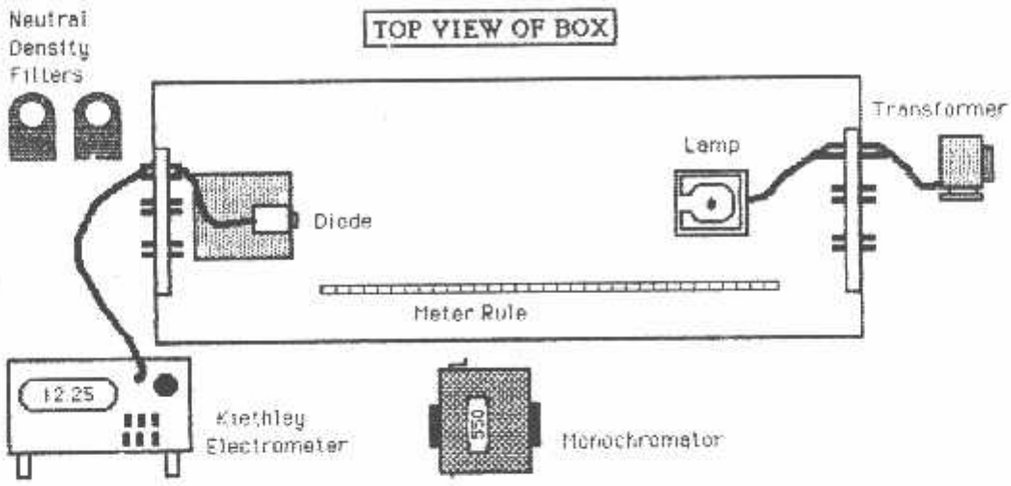

Figure 1: – Schematic arrangement of the apparatus for the photodiode linearity experiment. The quartz lamp and photodiode assembly reside inside the box. The neutral density filters are used for some of the measurements.

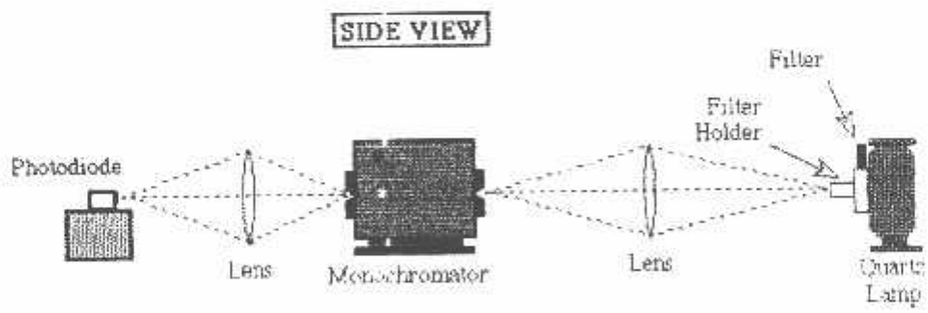

Figure 2: – Schematic arrangement of the apparatus for the filter transmission measurement. This entire setup resides inside the wooden box with connections to exterior devices as shown in **Figure 1**. Notice the filter holder mounted in front of the lamp housing.

Photodiode-Based Detector Operates at 60 GHz

Careful design of device structure and drive circuitry yield high speed photodetector for optical detection

By: Andrew Davidson, Focused Research Inc. and Kathy Li Dessau, New Focus Inc.

With the recent advancement of gigabit fiber communication and the photonic distribution of microwave signals, there is a growing need to characterize the high-speed optical signals found in such systems. This task is typically accomplished with a high-speed photodetector followed by an instrument such as a sampling oscilloscope, a radio frequency (RF) spectrum analyzer, or a vector network analyzer. For the measurement to be a true representation of the actual signal, the speed or bandwidth of the combined measurement system should exceed that of the signal under test. The high speed photodetector is thus an essential part of the system.

Designing a high-speed detector

Two types of photodetectors commonly used for high speed applications are *p-i-n* and Schottky photodiodes (see Figure 1). In both devices, photon absorption in the depletion region of a reverse-biased junction creates electron-hole pairs. These carriers are swept out of the high-field region to create a current in an external circuit.

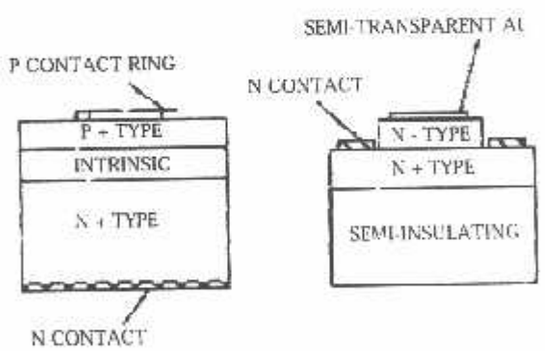

FIGURE 1: The high-field region is the intrinsic layer in the p-i-n photodiode (left) and the n-region in the Schottky photodiode (right).

The speed of these photodiodes is limited by depletion region transit time and capacitance. Transit time refers to the time required for the electrons and holes to drift across the high-field depletion region. It is determined by carrier velocity, which is constant ($\sim 3 \times 10^{7}$ cm/s) and the depletion region thickness t, which can vary. Depletion region thickness is thus the design parameter controlling transit time, and should be made inversely proportional to the desired bandwidth.

Capacitance slows the device via an RC time constant where the resistance is that of the device load impedance. The capacitance is proportional to the active area and inversely proportional to depletion region thickness. For high-speed operation, then, both the active area and depletion region thickness should be minimized. A small active area, however, places demanding requirements on the focusing optics for the detector. A thin depletion region means only a fraction of the incident photons will be absorbed. To optimize speed while maintaining performance, designers generally make the active area and depletion region thickness just small enough to satisfy the speed requirements; transit time is typically made comparable to the RC time constant. Using this simple approach, engineers at New Focus have designed high-speed Schottky detectors that can achieve bandwidths as high as 60 GHz.

The design team chose a Schottky configuration because it is the faster of the two designs — in the case of a *p-i-n* diode, if the top *p*-layer is absorbing, the carriers generated in this undepleted, low-field region must diffuse out at slow speeds. Schottky photodiodes also offer lower parasitic resistance. The *n*-type Schottky diode, for example, has only an *n*-layer and no *p*-layer. In a top-illuminated *n*-type diode, the carriers are created near the top metal contact; the holes, which are the slower carriers,

travel just a short distance to the metal.

The detectors have been designed for both back-side and front-side illumination. For back side illumination, light is incident through the transparent indium phosphide (InP) substrate and absorbed in the indium gallium arsenide (InGaAs) active region, permitting detection of wave lengths from 950 nm to 1650 nm. The top Schottky contact serves as a mirror, allowing a double-pass through the absorbing layer to enhance quantum efficiency.

The front-illuminated devices are fabricated with both InGaAs and gallium arsenide (GaAs) absorbing layers and have a thin, semi-transparent gold (Au) Schottky metal. The sheet resistance of the gold is detrimental to the high-speed performance, so a current-collecting ring of thick gold is added to the periphery of the active area to minimize this resistance (see Figure 2). The devices are sensitive for wavelengths ranging from 400 nm to 1650 nm.

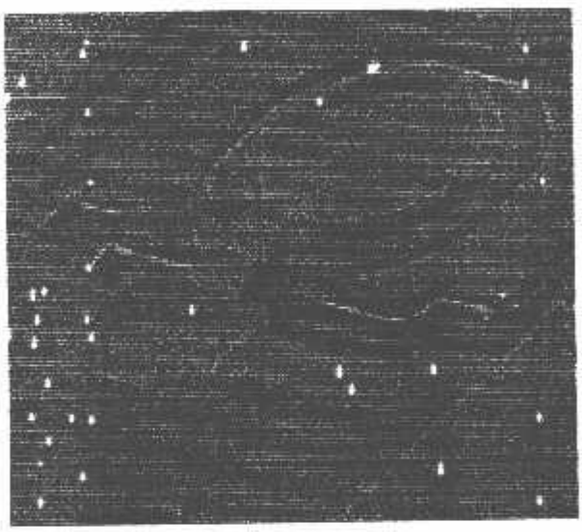

FIGURE 2: SEM of a front-illuminated InGaAs Schottky photodiode. Photo Courtesy of New Focus

Flat frequency response and ring-free impulse response detectors

An intrinsic photodiode designed for high-speed operation is necessary, but not sufficient, for high-speed optical detection. The bias circuitry and the high-speed connection to the 50-ohm output transmission line must also be carefully designed to produce the desired response. This response is dictated by the application and is generally either a flat frequency response, with the responsivity varying only slightly across the operating bandwidth, or a fast, ring-free impulse response. Fourier transform techniques show

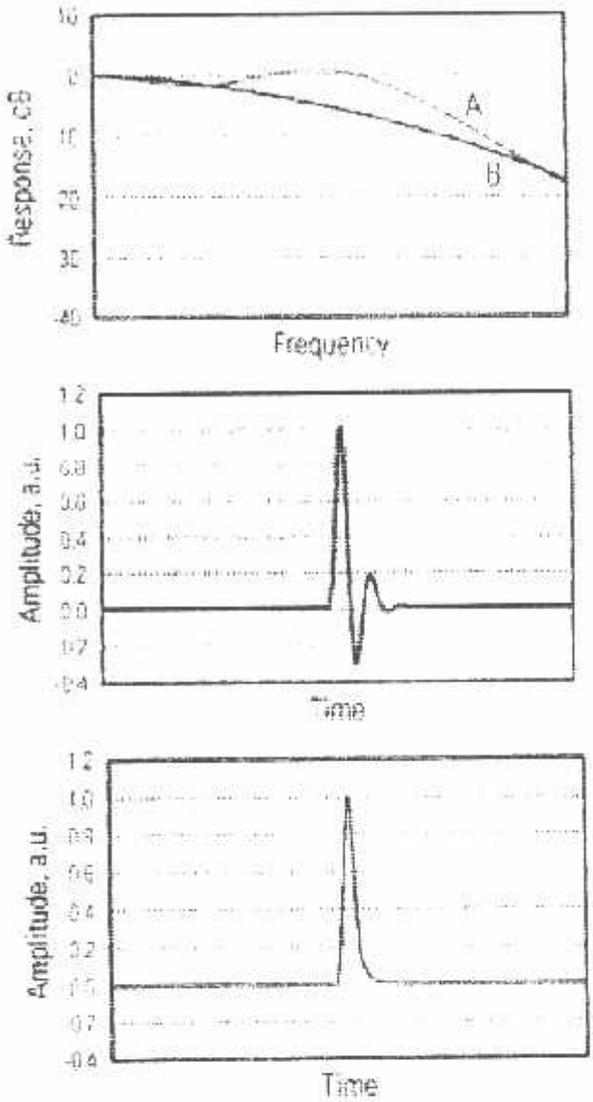

FIGURE 3: Detector designed for enhanced responsivity at high frequencies provides a nearly flat frequency response (top, curve A), but suffers from ringing in the temporal domain (middle). Detector with a clean, ring free impulse response in the temporal domain (bottom) experiences roll off in the frequency domain, reducing the 3-dB frequency.

that the flat frequency response suffers from controlled ringing in the temporal domain (impulse response, see Figure 3). The ring-free impulse response, on the other hand, corresponds to a characteristic roll-off in the frequency domain and a corresponding reduction in the 3-dB frequency.

Recently developed time-domain optimized detectors with a fast, minimal-ringing impulse response are especially useful for digital com-

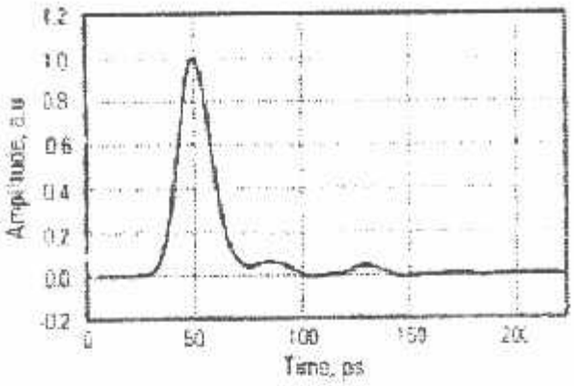

FIGURE 4: Impulse response of the Model 1444 measured with a 50-GHz scope and a 150-fs full-width-at-half-maximum input pulse at 1.06 μm shows only slight amounts on ringing.

munications applications in which spurious ringing can degrade an eye diagram and bit error rate (BER). These detectors have been designed with a resistive matching network that presents the diodes with a constant 50 ohm impedance to eliminate unwanted reflections, and also terminates the detector so that its impedance is 50 ohms. The internal 50-ohm termination makes the detectors directly compatible with BER testing using switched digital hierarchy and SONET filters. The detectors are also fabricated with on chip bias circuitry, such as integrated bypass capacitors which provide near-ideal performance to well beyond 60 GHz.

The impulse response of a detector with an 18-ps full-width-at-half-maximum shows only a slight amount of ringing (see Figure 4). The measurement has been made with a 50 GHz sampling oscilloscope and short (less than 200 fs) pulses from a diode-pumped neodymium-doped glass (Nd:glass) laser operating at 1.06 μm. Connecting the detector module directly to the input of the oscilloscope eliminates RF cables, and the detector's fiber optic input then receives signals from the system under test.

Detectors with a flat frequency response can be implemented with some slight inductive peaking to enhance the responsivity at higher frequencies. Such detectors are useful for applications involving the optical transmission of microwave and millimeter wave RF signals, such as wireless cellular networks or antenna remoting in military or commercial communication satellite systems.

High-speed detectors are an important component in characterizing high-bandwidth optical communications. By optimizing the photodiode for high-speed operation, and by designing the microwave circuitry to produce either a ring-free impulse response or a flat frequency response, a wide range of measurement needs can be addressed.

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Edited by Kristin Lewotsky

Features

- Compatible with MCS®-51 Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-Down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)

Description

The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of In-System Programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

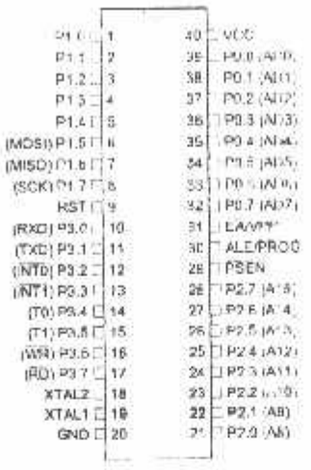
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

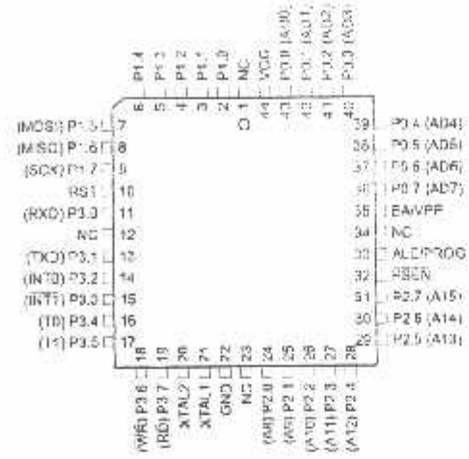
2487B-MICRO-12/03

Pin Configurations

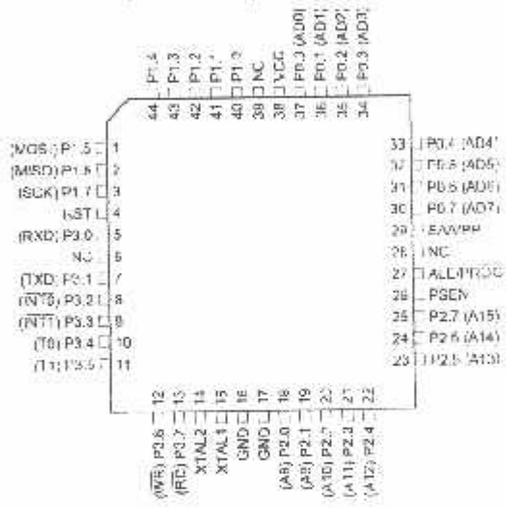
PDIP



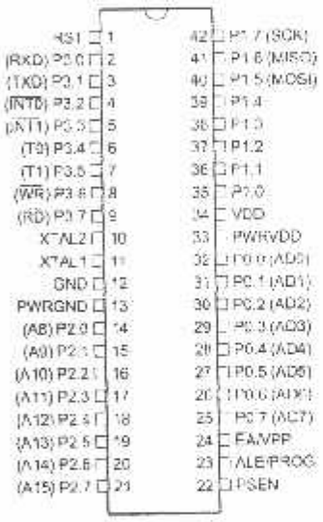
PLCC



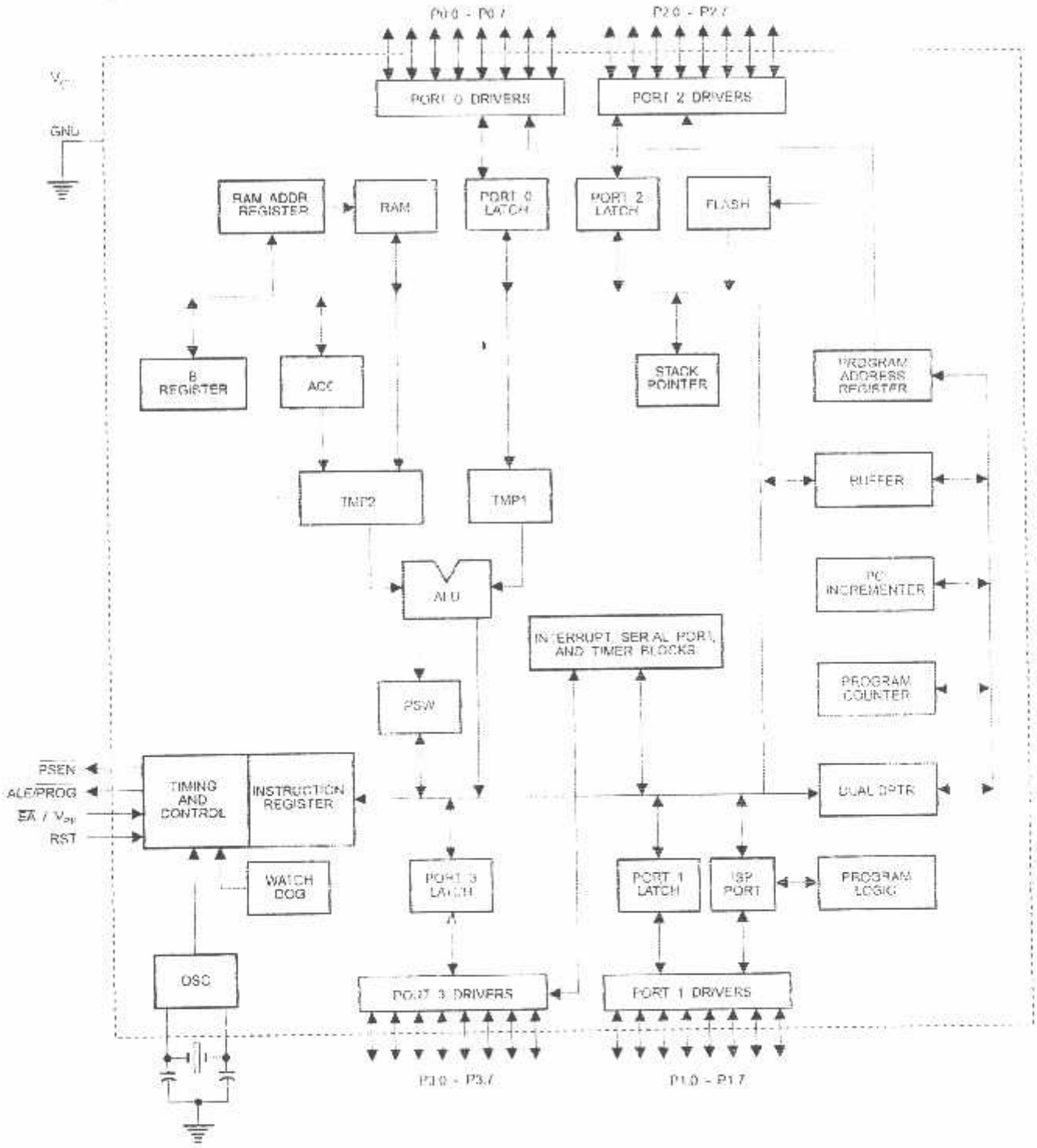
TQFP



PDIP



Block Diagram



Pin Description

VCC Supply voltage (all packages except 42-PDIP).

GND Ground (all packages except 42-PDIP; for 42-PDIP GND connects only the logic core and the embedded program memory).

VDD Supply voltage for the 42-PDIP which connects only the logic core and the embedded program memory.

PWRVDD Supply voltage for the 42-PDIP which connects only the I/O Pad Drivers. The application board **MUST** connect both VDD and PWRVDD to the board supply voltage.

PWRGND Ground for the 42-PDIP which connects only the I/O Pad Drivers. PWRGND and GND are weakly connected through the common silicon substrate, but not through any metal link. The application board **MUST** connect both GND and PWRGND to the board ground.

Port 0 Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1 Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2 Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 1. AT89S51 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H									0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset-out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1 Address = A2H Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Data Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

Watchdog Timer One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the Atmel Web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture", then "Documentation", and "Other Documents". Open the Adobe® Acrobat® file "AT89 Series Hardware Description".

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the Atmel Web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture", then "Documentation", and "Other Documents". Open the Adobe Acrobat file "AT89 Series Hardware Description".

Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit positions IE.6 and IE.5 are unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

Table 4. Interrupt Enable (IE) Register

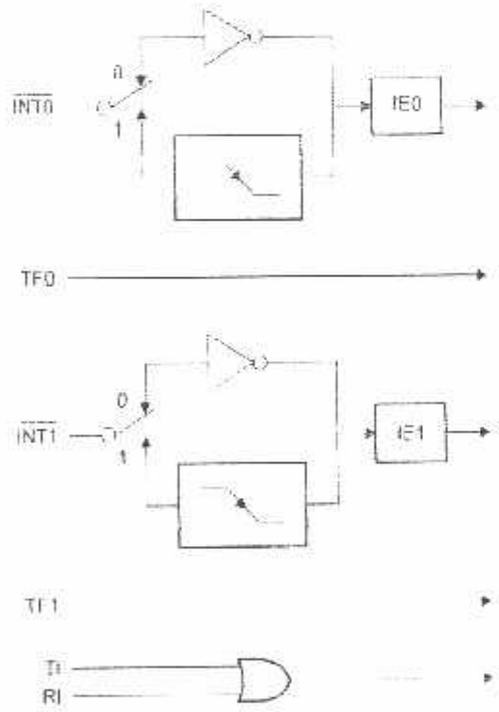
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

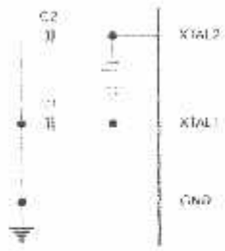
Figure 1. Interrupt Sources



Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ±10 pF for Crystals
= 40 pF ±10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt ($\overline{INT0}$ or $\overline{INT1}$). Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Programming the Flash – Parallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash Programming Modes table (Table 7) and Figures 4 and 5. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. **The status of the individual lock bits can be verified directly by reading them back.**

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates AT89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL 1 or a crystal needs to be connected across pins XTAL 1 and XTAL 2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 35 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

Serial Programming Algorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8.

Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer worldwide support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 7. Flash Programming Modes

Mode	V_{CC}	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

Notes:
1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/BSY signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

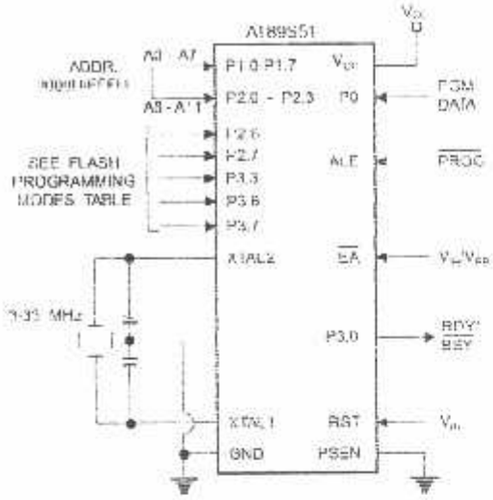
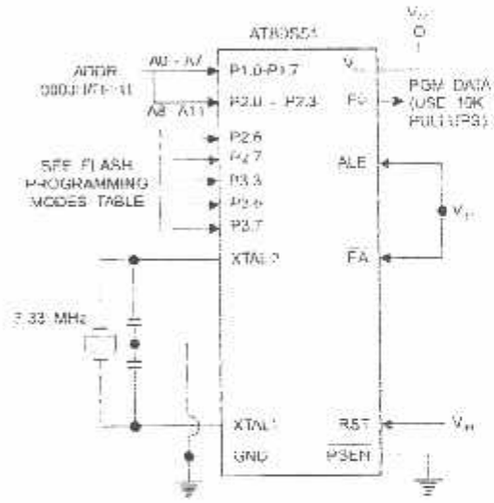


Figure 5. Verifying the Flash Memory (Parallel Mode)



Flash Programming and Verification Characteristics (Parallel Mode)

T_A = 20°C to 30°C, V_{CC} = 4.5 to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	0.2	1	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		50	µs

Figure 6. Flash Programming and Verification Waveforms – Parallel Mode

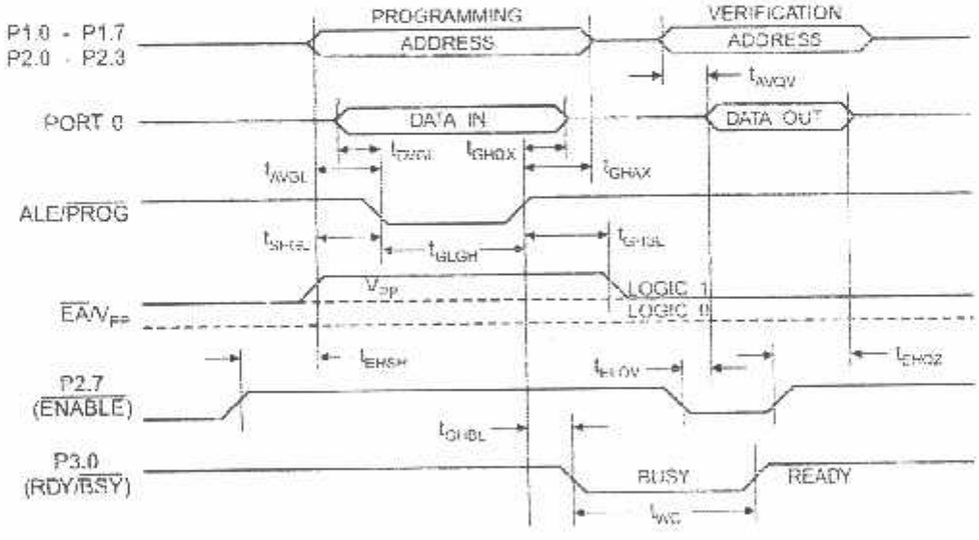
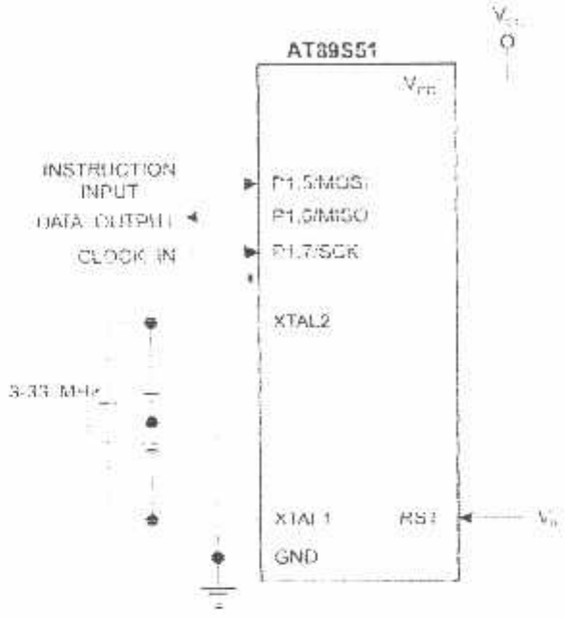


Figure 7. Flash Memory Serial Downloading



Flash Programming and Verification Waveforms – Serial Mode

Figure 8. Serial Programming Waveforms

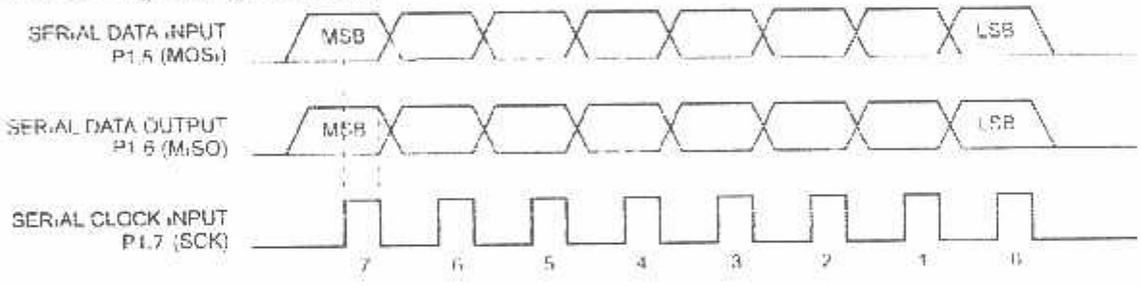


Table 3. Serial Programming Instruction Set

Instruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Write Lock Bits[1]	1010 1100	1110 00B2B1	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xxxx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Read Signature Bytes	0010 1000	xxxx A11 A10 A9 A8	A7 xxx xxx0	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Note: 1. B1 = 0, B2 = 0 → Mode 1, no lock protection
B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
B1 = 1, B2 = 1 → Mode 4, lock bit 3 activated

Each of the lock bit modes need to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Serial Programming Characteristics

Figure 9. Serial Programming Timing

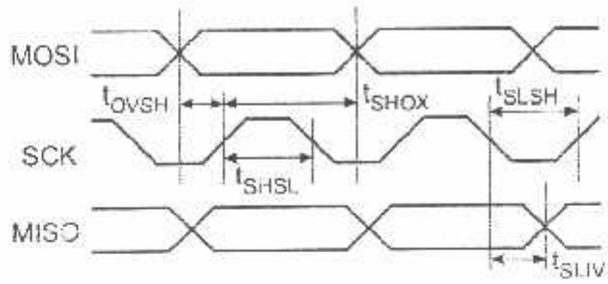


Table 9. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	3		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	8 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	8 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage(1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage(1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode(2)	V_{CC} = 5.5V		50	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

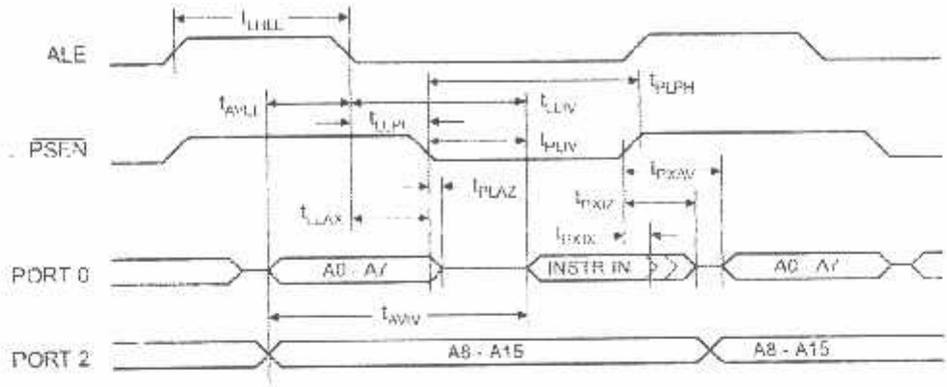
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

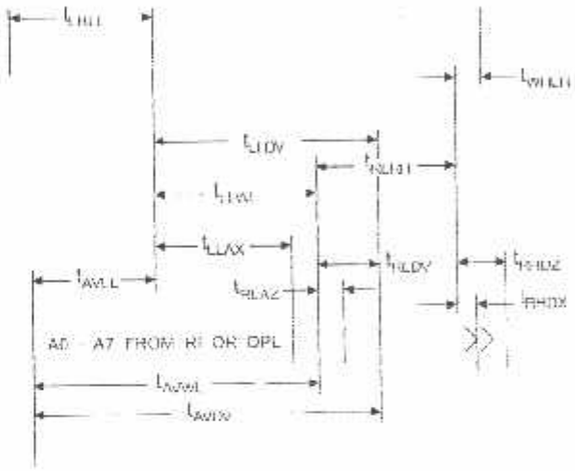
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-25		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-25		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

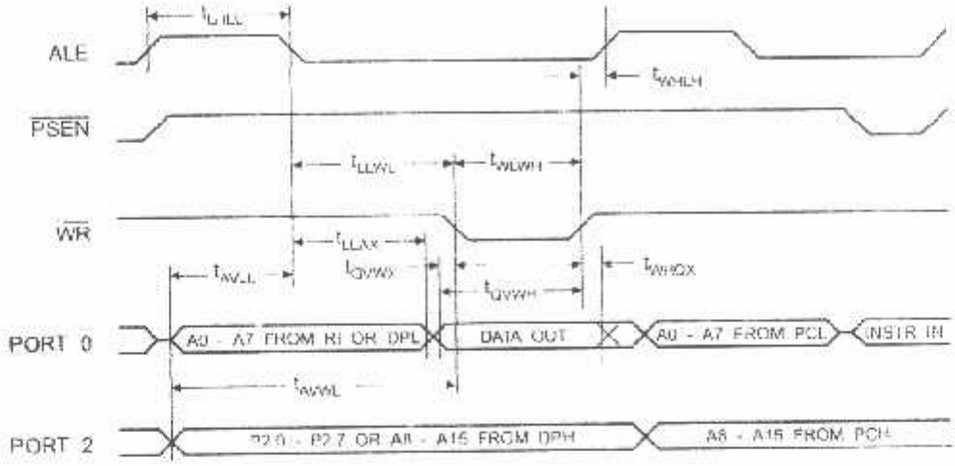
External Program Memory Read Cycle



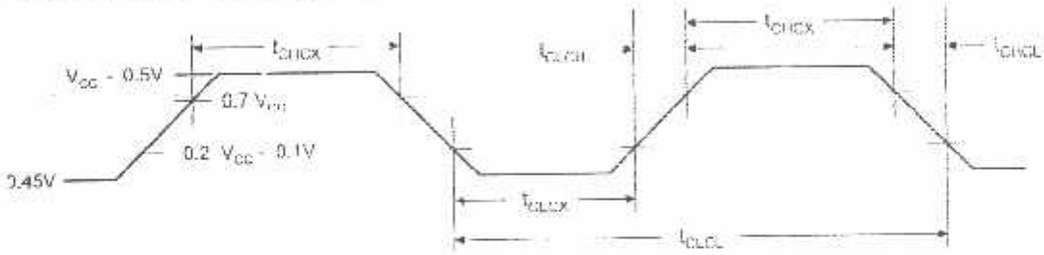
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

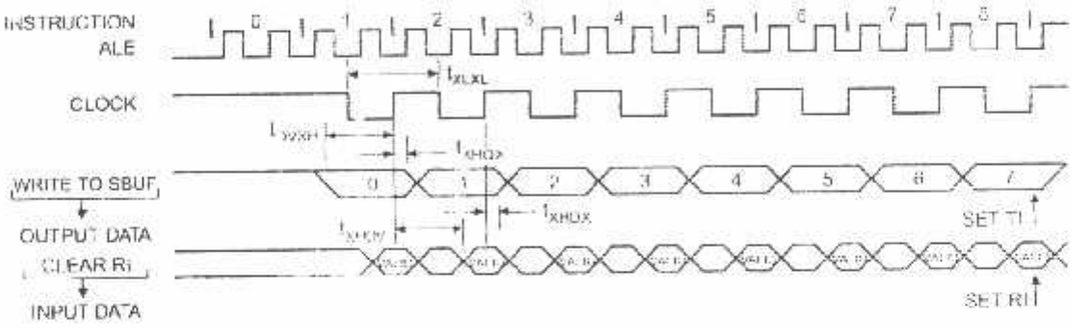
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	33	MHz
t_{CLCL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

Serial Port Timing: Shift Register Mode Test Conditions

The values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms



AC Testing Input/Output Waveforms[1]

Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]

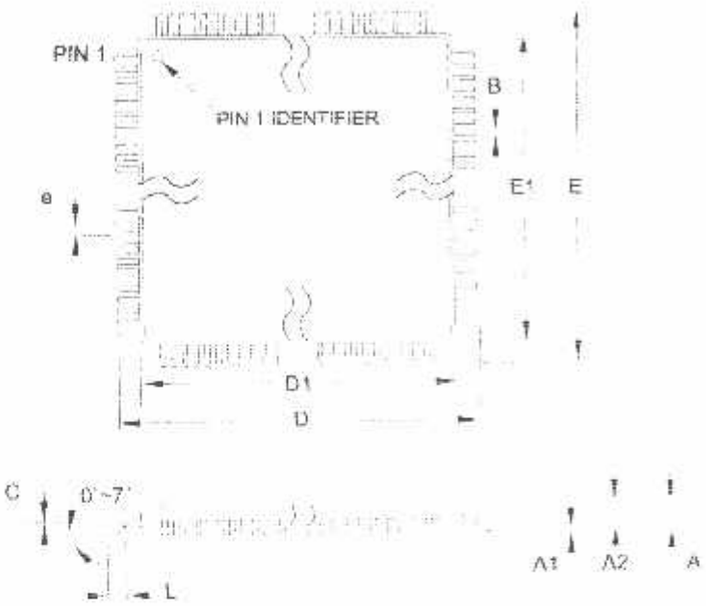
Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC AT89S51-24SC	44A 44J 40P6 42PS6	Commercial (0° C to 70° C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI AT89S51-24SI	44A 44J 40P6 42PS6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC AT89S51-33SC	44A 44J 40P6 42PS6	Commercial (0° C to 70° C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
42PS6	42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

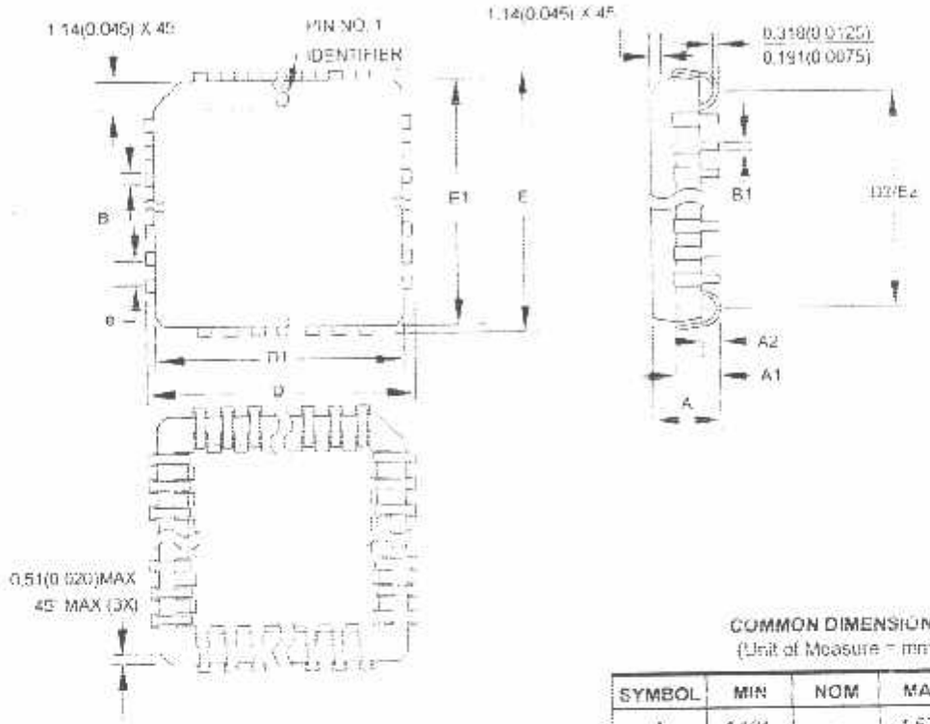
SYMBOL	MIN	NOM	MAX	NOTE
A			1.20	
A1	0.05		0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09		0.20	
L	0.45		0.75	
e		0.80 TYP		

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A**, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

4J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

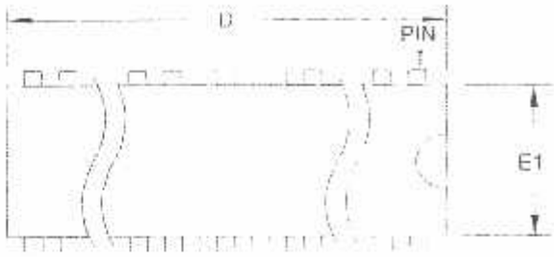
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286		2.048	
A2	0.508		–	
D	17.399		17.653	
D1	16.510	–	16.662	Note 2
E	17.399		17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330		0.533	
e	1.270 TYP			

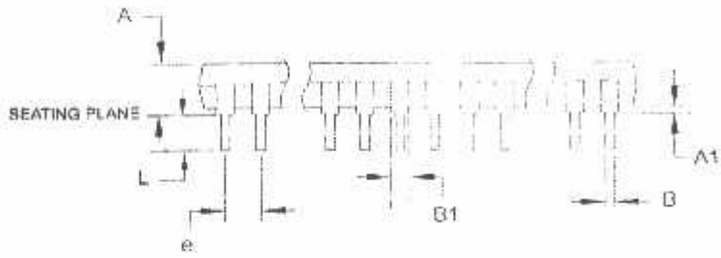
Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

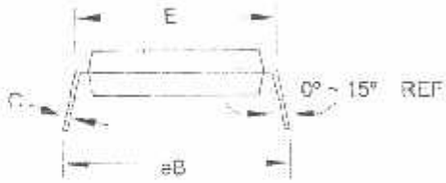
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

40P6 – PDIP







COMMON DIMENSIONS
(Unit of Measure = mm)

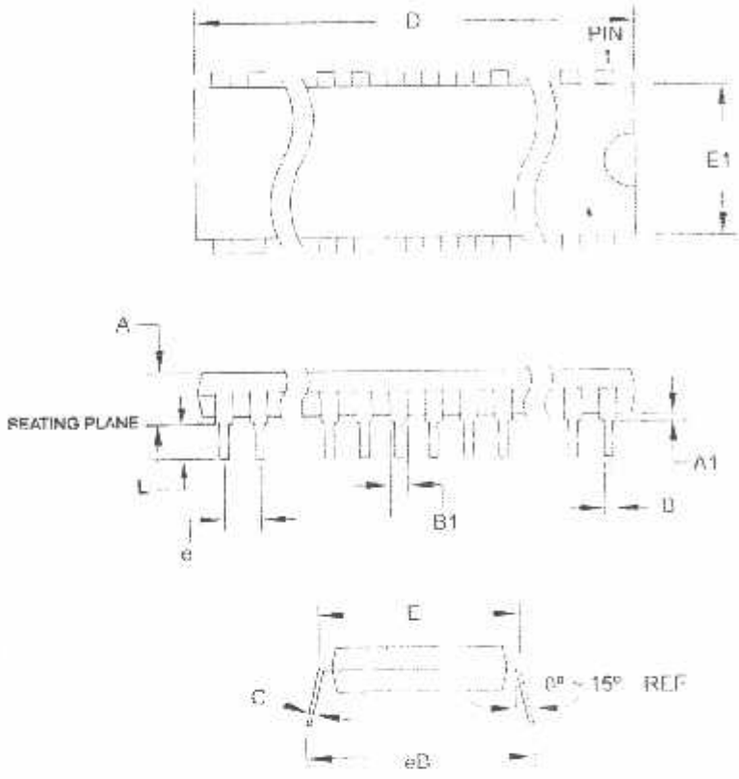
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–		
D	52.070	–	52.578	Note 2
E	15.240		15.875	
E1	13.462		13.970	Note 2
B	0.356		0.559	
B1	1.041		1.651	
L	3.048	–	3.556	
C	0.203		0.381	
eB	15.494		17.526	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

2PS6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A		–	4.83	
A1	0.51	–	–	
D	36.70	–	36.96	Note 2
E	15.24	–	15.88	
E1	13.46	–	13.97	Note 2
B	0.38	–	0.56	
B1	0.76	–	1.27	
L	3.05		3.43	
C	0.20	–	0.30	
eB		–	18.55	
e	1.78 TYP			

Notes:
1. This package conforms to JEDEC Reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/6/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**42PS6**, 42-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	42PS6	A

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