TUGAS AKHIR

PERENCANAAN DAN PEMBUATAN ALAT PENGATURAN KECEPATAN KIPAS ANGIN MENGGUNAKAN MIKROKONTROLER AT89S51

Disusun Oleh :

I Putu Agus Suwardana
01. 57. 107

KONSENTRASI ELEKTRONIKA
PROGRAM STUDI TEKNIK ELEKTRO D -III
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
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LEMBAR PERSETUJUAN

Perencanaan dan Pembuatan Alat Pengaturan Kecepatan Kipas Angin Menggunakan Mikrokontroler AT89S51

TUGAS AKHIR

Diajukan Guna Memenuhi Salah Satu Syarat Untuk Memperoleh Gelar Pada Jurusan Teknik Elektro D-III Konsentrasi Elektronika.

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ABSTRAK

Perencanaan dan Pembuatan Alat Pengaturan Kecepatan Kipas Angin Menggunakan Mikrokontroler AT89S51, I Putu Agus Suwardana, 0157107, Konsentrasi Elektronika, Jurusan Teknik Elektro DIII, Fakultas Teknologi Industri, Bambang Prio Hartono, ST, MT, Institut Teknologi Nasional Malang, 2007.

Kata Kunci : Mikrokontroler AT89S51, Hardware, Software, Sensor Suhu, Kipas.

Penggunaan mikrokontroler sebagai unit-unit kendali sudah sangat luas. Mengacu dengan adanya penelitian Hardianto Rochman (2007), kipas angin disempurnakan dengan menggunakan remote control sehingga dalam menghidupkan ataupun mematikan kipas angin tidak lagi dengan harus menekan tombol manual. Hal ini merupakan suatu kemajuan yang sangat membantu sekali bagi para penggunanya dengan tidak lagi menekan tombol manual melainkan sudah bisa mengoperasikan kipas angin tersebut dari jarak jauh. Tetapi dalam hal ini penemuan tersebut masih memiliki kelemahan yakni masih adanya ketergantungan terhadap remote control.Untuk itu dibuatlah sebuah alat pengaturan suhu rungan dengan kipas angin berbasis mikrokontroller AT89S51.

Dalam penelitian ini peneliti menggunakan beberapa metodologi penelitian diantaranya: Pertama metoda kepustakaan, yaitu penulis melakukan studi literatur tentang permasalahan yang ada melalui perpustakaan, dan internet. Kedua metoda percobaan, yaitu penulis melakukan berbagai percobaan yang berkaitan dengan peralatan. Ketiga metoda perencanaan dan perancangan alat, yaitu penulis membuat alat dengan menggabungkan berbagai data dan rangkaian yang penulis dapatkan. Keempat metoda pengujian, yaitu penulis melakukan pengujian alat dan kemudian dapat mengambil kesimpulan dari hasil pengujian tersebut.

Dari hasil analisa data yang dilakukan dapat dibuktikan dengan langkah Pengujian *hardware* dan *software* dapat dikatakan bekerja dengan baik. Sensor suhu diaplikasikan untuk pendeteksian derajat suhu pada suhu ruangan. Kipas angin disetting untuk bekerja sesuai dengan perubahan tegangan input dari sensor suhu, dimana setiap ada perubahan tegangan inputan maka akan berpengaruh pula pada kerja kipas angin

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Puji syukur kehadirat Tuhan Yang Maha Esa telah memberikan rahmat dan hidayah-Nya, sehingga dapat menyelesaikan Tugas Akhir yang berjudul " Perencanaan dan Pembuatan Alat Pengaturan Kecepatan Kipas Angin Menggunakan Mikrokontroler AT89S51 " ini dengan lancar. Tugas Akhir ini merupakan persyaratan kelulusan Studi di Jurusan Teknik Elektro D-III Konsentrasi Teknik Elektronika ITN Malang.

Keberhasilan penyelesaian laporan Tugas Akhir ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terima kasih kepada :

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Malang, Maret 2008

Penyusun

DAFTAR ISI

DAFTAR GAMBAR

DAFTAR TABEL

DAFTAR GRAFIK

BAB I
PENDAHULUAN

1.1. Latar Belakang

Pada saat sekarang ini kemajuan dalam bidang teknologi sangatlah pesat. Hal ini sangat mempengaruhi dalam pembuatan alat-alat canggih dimana alat-alat canggih tersebut dapat bekerja secara otomatis serta memiliki tingkat ketelitian yang sangat tinggi.

Penggunaan mikrokontroler sebagai unit-unit kendali sudah sangat luas. Hal ini dikarenakan peralatan-peralatan yang terkontrol dengan menggunakan mikrokontroler telah banyak memberikan kemudahan-kemudahan dalam penggunaannya.

Mengacu dengan adanya penelitian Hardianto Rochman (2007), kipas angin disempurnakan dengan menggunakan remote control sehingga dalam menghidupkan ataupun mematikan kipas angin tidak lagi dengan harus menekan tombol manual. Hal ini merupakan suatu kemajuan yang sangat membantu sekali bagi para penggunanya dengan tidak lagi menekan tombol manual melainkan sudah bisa mengoperasikan kipas angin tersebut dari jarak jauh. Tetapi dalam hal ini penemuan tersebut masih memiliki kelemahan yakni masih adanya ketergantungan terhadap remote control.

Dengan adanya permasalahan tersebut maka munculah ide dimana dengan menggunakan mikrokontroller, diharapkan tercipta suatu alat pengaturan suhu ruangan dengan kipas angin yang dapat beroperasi secara otomatis hanya dengan control suhu pada sekeliling ruangan tersebut, sehingga untuk penggunanya tidak lagi bergantung sepenuhnya terhadap remote control.

Untuk itu dibuatlah sebuah alat pengatur kecepatan kipas angin berbasis mikrokontroller AT89S51.

1.2. Rumusan Masalah

Berdasarkan hal tersebut diatas maka timbul permasalahan seperti :

1. Bagaimana merencanakan dan membuat alat pengaturan kecepatan kipas angin menggunakan Mikrokontroler.
2. Bagaimana pengaturan suhu dengan menggunakan sensor.
3. Bagaimana mengimplementasikan Mikrokontroller dengan menggunakan AT89S51

1.3. Tujuan

Merencanakan dan membuat alat pengaturan kecepatan kipas angin menggunakan mikrokontroller AT89S51.

1.4. Batasan Masalah

Mengingat masalah yang terkait dengan alat ini cukup luas serta keterbatasan pengetahuan dan kemampuan yang penulis miliki, maka penulis merasa perlu untuk membatasi masalah yang akan dibahas dalam penulisan ini.

Untuk itu penulis membatasi hanya pada hal-hal berikut :

1. Alat ini menggunakan mikrokontroller AT89S51 sebagai unit pemrosesnya.
2. Sensor suhu yang digunakan adalah IC LM35
3. Hanya membahas perangkat kerasnya, sedangkan perangkat lunaknya hanya dibahas secara garis besar.

4. Tidak membahas tentang power supply.

1.5. Metodologi Penelitian

Metodologi penelitian alat ini dilakukan melalui beberapa tahap :

1. Study literature tentang sensor suhu, ADC, LCD dan mikrokontroller.
2. Perancangan dan pembuatan alat sensor suhu, ADC, LCD dan mikrokontroller.
3. Pelaksanaan uji coba alat sensor suhu, ADC, LCD, driver triac diac dan mikrokontroller.
4. Analisa data.
5. Pembahasan.
6. Kesimpulan dan saran.

1.6. Sistematika Penulisan

Sistematika penulisan dalam tugas akhir ini terdiri dari 5 bab, yaitu :

BAB I : PENDAHULUAN

Berisi tentang latar belakang permasalahan, tujuan pembahasan, metodologi pembahasan, batasan masalah, sistematika penulisan dan relevansi dari penulisan tugas akhir ini.

BAB I : TEORI DASAR

Membahas mengenai teori dasar yang menunjang dari perencanaan dan pembuatan alat serta teori dasar alat-alat pendukung lainnya.

BAB III : PERENCANAAN DAN PEMBUATAN ALAT

Membahas tentang perencanaan dan pembuatan alat secara keseluruhan.

BAB IV : PENGUJIAN ALAT

Membahas tentang uji coba alat yang telah dibuat, cara pengoperasiannya, serta spesifikasi alat itu sendiri.

BAB V : PENUTUP

Berisi tentang kesimpulan dari pembahasan pada bab-bab sebelumnya dan kemungkinan pengembangan alat tersebut.

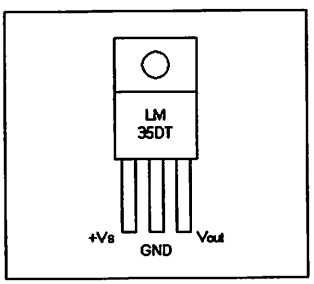
BAB II
DASAR TEORI

2.1. Sensor Suhu

Sensor suhu harus mempunyai kepekaan terhadap perubahan suhu yang akan diukur. Sensor suhu berfungsi sebagai transduser yang mengubah besaran suhu menjadi besaran listrik dalam bentuk tegangan.

Salah satu sensor suhu yang mudah digunakan adalah sensor suhu tipe IC LM35 adalah sensor temperatur tipe IC yang memiliki tegangan keluaran yang linier terhadap skala temperatur Celcius (*Centigrade*) dengan skala 10 mV / °C. Dengan demikian sensor ini juga linier terhadap skala temperatur Kelvin. Sensor ini dapat digunakan dengan catu daya tunggal atau dengan catu daya positif dan negatif.

Dengan menyerap daya sebasar 60μA dari catu daya, LM35 menghasilkan efek *self heating* kurang dari 0,1°C pada udara diam. Tegangan operasi yang umum digunakan adalah dari 4 hingga 20 volt. Keluarannya memiliki impedansi rendah, yaitu 0,1 Ω untuk beban 1 mA.



Gambar 2.1 Salah satu LM35 yang umum digunakan.
Sumber: Datasheet IC LM35

Dalam pemakaian, LM35 dapat direkatkan pada permukaan yang temperaturnya akan diukur jika menganggap temperatur udara sekitar hampir sama dengan temperatur permukaan. Jika temperatur udara jauh lebih tinggi atau lebih rendah dari pada temperatur permukaan, maka temperatur LM35 dapat berada diantara temperatur permukaan dan udara.

2.2. A/D Converter

Sinyal analog dapat dikodekan dalam bentuk bilangan biner menggunakan pengubah analog ke digital. Pengubahan analog ke digital ini dilakukan karena banyak sistem atau peralatan digital yang memerlukan masukkan berupa sinyal-sinyal analog atau digunakan untuk pemrosesan sinyal analog yang akan lebih mudah dan akurat jika dilakukan secara digital oleh peralatan digital.

Hal yang perlu diperhatikan dalam penggunaan ADC ini adalah :

- Waktu konversi

Waktu yang diperlukan ADC untuk menghasilkan suatu kode biner yang tepat untuk tegangan masukan yang diberikan. Sebuah konverter disebut berkecepatan tinggi jika mempunyai waktu konversi yang rendah.

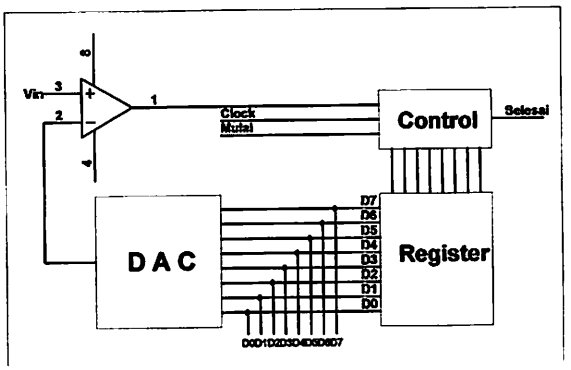
- Resolusi

Perubahan terkecil yang terjadi pada keluaran analog sebagai suatu hasil dari perubahan pada masukan digital. Resolusi selalu sama dengan bobot dari LSB (step size), karena step size merupakan besarnya perubahan tegangan keluaran pada saat kode masukan berubah dari satu step ke step berikutnya.

- Akurasi

Perbedaan antara tegangan masukan secara ideal yang dibutuhkan untuk menghasilkan suatu kode biner tertentu terhadap tegangan masukan sebenarnya.

Dalam pengubahan sinyal analog ke digital ada tiga metode, yakni metode pembandingan langsung, metode pencacah dan metode pendekatan beruntun. Pada sistem ADC, ada dua macam sinyal yang harus diukur atau dibangkitkan. Metode pendekatan beruntun adalah metode yang paling banyak digunakan. Diagram kotak metode ini diberikan dalam Gambar 2.4. Data hasil konversi ADC didapat bila tegangan dari DAC sama dengan tegangan masukan ADC. Rangkaian ADC dengan pendekatan beruntun ditunjukkan dalam Gambar 2.2.



Gambar 2.2 ADC dengan pendekatan beruntun
Sumber: National Data Book

Prinsip kerja :

1. Bila sinyal mulai diberi logika rendah, Vout akan menjadi nol. Ketika sinyal mulai kembali tinggi terjadi konversi. Pada metode ini pencacahan tidak naik satu per satu.
2. Dengan kecepatan yang ditentukan oleh clock, unit kontrol secara terus-menerus memodifikasi bilangan biner yang disimpan didalam register.
3. Mula-mula bit MSB (*Most Significant Bit*) dibuat tinggi sehingga menghasilkan keluaran 1000 0000_B. Nilai biner ini akan diubah oleh rangkaian DAC.
4. Komparator akan membandingkan keluaran DAC dengan tegangan masukan. Jika tegangan masukan lebih tinggi, keluaran pembanding akan membuat rangkaian kontrol tetap mengaktifkan MSB, sedangkan jika masukan lebih rendah, keluaran pembanding akan membuat rangkaian kontrol me-*reset* MSB. Kejadian tersebut akan diulang untuk bit-bit berikutnya.
5. Apabila konversi telah selesai, unit kontrol akan mengirimkan sinyal selesai konversi yang menjadi rendah. Sehingga data digital pada bus data merupakan data digital yang mewakili tegangan analog pada sisi masukan.

2.3. Mikrokontroler AT89S51

2.3.1. Pendahuluan

Perbedaan mendasar antara mikrokontroller dan mikroprosesor terletak pada kelengkapan isinya yaitu mikrokontroller sudah dilengkapi dengan berbagai macam alat kontrol selain memiliki CPU juga dilengkapi memori(ROM & RAM)

maupun input output yang merupakan kelengkapan minimum sistem sedangkan mikroprosesor kesemuanya itu tidak dimiliki secara internal melainkan terpisah sebuah mikrokontroller dapat dikatakan sebagai mikrokomputer dalam keping tunggal (Singgle Chip Microcomputer) yang dapat berdiri sendiri.

Mikrokontroller AT89S51 adalah mikrokontroller buatan ATMEL yang kompatibel penuh dengan mikrokontroler keluarga MCS - 51, hanya membutuhkan daya rendah, memiliki performance yang tinggi dan merupakan mikrokomputer 8 bit yang dilengkapi 4Kbyte EEPROM *(Electrical Erasable and Programmable Read Only Memory)* dan 128 Byte RAM internal. Program memori dapat diprogram dalam sistem atau menggunakan programmer *Nonvolatile* Memory konvensional. Dalam sistem mikrokontroller terdapat dua hal yang mendasar, yaitu: perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

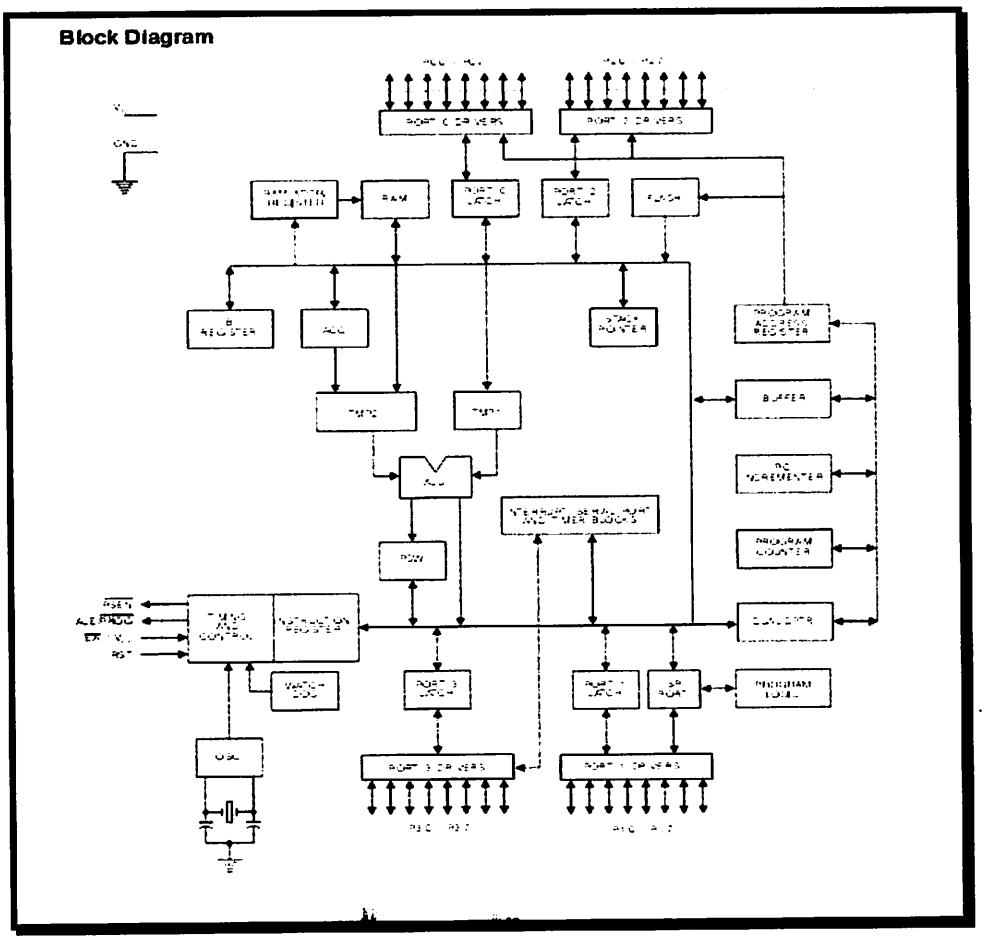
2.3.2. Perangkat keras mikrokontroler AT89S51

Secara umum Mikrokontroller AT89S51 memiliki :

- CPU 8 bit termasuk keluarga MCS-S I
- 4 Kb Flash memory
- 128 byte Internal RAM
- 32 buah Port I/O,masing - masing terdiri atas 8 jalur I/O
- 2 Timer / counter 16 bit
- 2 Serial Port Full Duplex
- 2 DPTR *(Data pointer)*

- *System Interrupt* dengan 2 sumber *Interrupt* eksternal dan 4 sumber *Interrupt* internal.
- Fleksibel ISP Programming

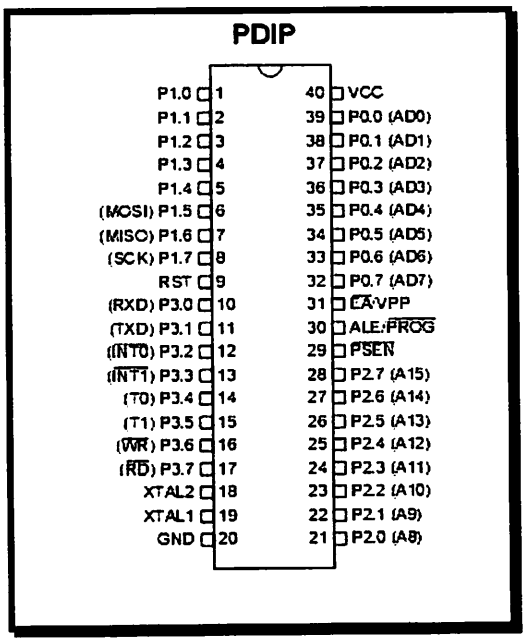
Dengan keistimewaan diatas pembuatan alat menggunakan AT89S51 menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak. Adapun blok diagram dari Mikrokontroller AT89S51 adalah sebagai berikut:



Gambar 2.3 Diagram Blok Mikrokontroller AT89S51
Sumber: Datasheet IC AT89S51

2.3.3. Konfigurasi Pena-Pena Mikrokontroller AT89S51

Mikrokontroller AT89S51 terdiri dari 40 pin dengan konfigurasi sebagai Berikut :



Gambar 2.4 Konfigurasi Pin AT89S51
Sumber: Datasheet IC AT89S51

Fungsi tiap-tiap pin-nya adalah sebagai berikut :

- VCC (Supply tegangan), pin 40
- GND (*Ground*), pin 20
- Port 0, pin 32 – 39

  Merupakan port input-output dua arah, tanpa internal pull-up dan dikonfigurasikan sebagai multipleks bus alamat rendah (A_0 - A7) dan data

selama pengaksesan memory eksternal. Setiap pin-nya dapat mengendalikan langsung 8 beban TTL. Port0 juga menerima dan mengeluarkan *code byte* selama proses pemrograman dan verifikasi ROM/EEPROM internal.

- Port 1, pin 1 - 8

Merupakan port input-output dua arah dengan internal pull-up yang dapat mengendalikan beban 4 TTL secara langsung dan mempunyai kegunaan lain yaitu sebagai port ISP header.

Tabel 2.1
Port ISP Header

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

- Port 2, pin 21 - 28

Merupakan port input-output dengan internal pull-up. Mengeluarkan alamat tinggi selama pengambilan program memory external.

- Port 3, pin 10 - 17

Merupakan port input-output dengan internal pull-up, dimana Port 3 juga memiliki fungsi khusus dan dapat dilihat pada tabel berikut ini

Tabel 2-2
Fungsi Khusus Pada Port 1

Simbol	Posisi	Nama dan arti
/RD	P3.7	*External data memori read strobe*
/WR	P3.6	*External data memori write strobe*
T1	P3.5	*Timer / counter 1 external input*
T0	P3.4	*Timer / counter 0 external input*
/INT1	P1.3	*External interrupt 1*
/INT0	P1.2	*External interrupt 0*
TXD	P1.1	*Serial data output port*
RXD	P1.0	*Serial data input port*

- RST *(Reset)*, pin 9

  Input Reset merupakan reset master untuk AT89S51.

- ALE/ Prog *(Address Latch Enable)*, pin 30

  Digunakan untuk memberikan sinyal *latch* pada alamat rendah pada multipleks *bus addres* dan data.

- PSEN (*Program Store Enable)*, pin 29

  Merupakan sinyal pengontrol yang memperbolehkan program memori eksternal masuk ke dalam bus.

- EA / VPP *(External Access)*, pin 31

Dapat diberikan logika rendah *(Ground)* atau logika tinggi (+5V). Jika diberikan logika tinggi maka mikrokontroller akan mengakses program dari *ROM* internal *(EEPROM / Flash Memory),* dan jika diberikan logika rendah maka mikrokontroller akan mengakses program dari memori eksternal.

- X-TAL 1 dan X-TAL 2, pin 19,18

  Kaki ini dihubungkan dengan kristal bila menggunakan *osilator internal.* XTAL 1 merupakan *input inverting osilator amplifier* sedangkan XTAL 2 merupakan *output inverting osilator amplifier.*

2.3.4. Organisasi Memory.

Mikrokontoller AT89S51 memiliki ruang alamat memori data dan memori program yang terpisah. Pemisahan memori program dan memori data tersebut membolehkan memori data diakses dengan alamat 8-bit, sehingga dapat dengan cepat dan mudah disimpan dan dimanipulasi oleh CPU 8-bit. Namun demikian, alamat memori data 16-bit bisa juga dihasilkan melalui register DPTR.

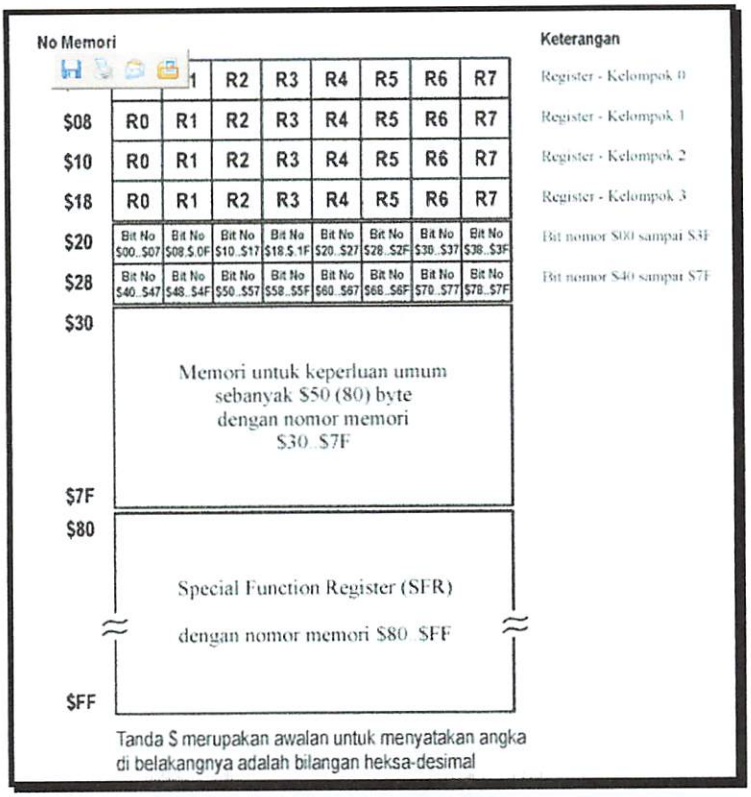
2.3.4.1. Program Memory

Program memori hanya dapat dibaca, tidak dapat ditulis. Disini tersimpan program yang akan dijalankan oleh AT89S51 dan data-data konstanta. Sinyal pembacaan EPROM eksternal adalah dari pin-PSEN. Pada AT89S51 ada dua tipe organisasi memori dari program memori, yaitu :

- Pengaksesan program memori sebagian berasal dari internal EPROM yang menempati alamat terendah dan alamat berikutnya dari EPROM eksternal. Sebagai contoh alamat 4 Kbyte program memori terendah adalah ROM internal dan alamat berikutnya adalah pada EPROM.
- Pengaksesan program memori yang semuanya dari eksternal EPROM.

2.3.4.2. Data Memori

Data memori menempati alamat yang terpisah dari program memori.Data memori merupakan tempat penyimpanan data variabel, operasi *stack* dan sebagainya. Data memori dapat dibaca dan ditulis. Sinyal pembacaan untuk emsternal RAM berasal dari pin –RD dan untuk penulisan berasal dari pin –RW. Peta data memori digambarkan sebagai berikut :



Gambar 2.5 Denah Memori Data AT89S51
Sumber: Data Memori MCS-51. www.alds.edu.com

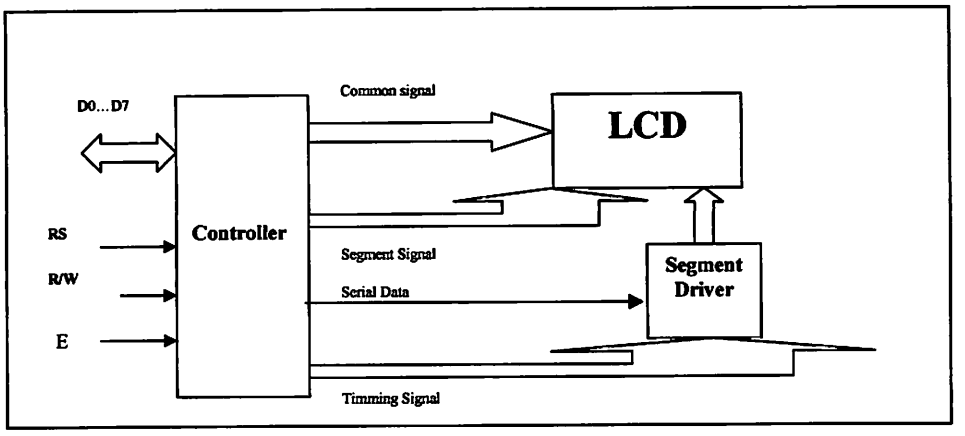
Alamat 00H-FFH merupakan alamat dari internal RAM yang dapat dialamati dalam dua mode. Pada alamat 00H-7FH dapat dialamati dalam *mode direct* maupun *indirect addressing.* Alamat 80H-FFH hanya dapat dialamati dalam *mode direct addressing.* Diluar alat tersebut merupakan alamat eksternal RAM. 32 byte terendah data memori terbagi atas 4 buah bank yang masing-masing terdiri aas 8 buah register. Kombinasi dari bank ini ditentukan oleh register PSW. Register-register tersebut adalah R0 sampai R7 yang menempati alamat 00H-1FH. Diatasnya merupakan segmen bit *addresable* yang besarnya 16 byte, menempati alamat 20H sampai 2FH. Alamat berikutnya yaitu mulai 30H sampai 7FH dapat dipakai sebagai data RAM.

Setelah kondisi reset, kondisi baku register SP (*stack pointer)* akan menuju alamat 07H dan begitu program dijalankan isi register SP akan ditambah 1 (menunjuk ke alamat 08H). Dan ini merupakan register bank 1 register R0. Bila memakai lebih dari satu bank register maka SP harus diinisialisasikan kelokasi yang lain.

2.4 Liquid Crystal Display (LCD)

Modul peraga yang digunakan dalam aplikasi ini adalah LCD modul M1632. modul LCD ini membutuhkan daya yang kecil dan dilengkapi dengan panel LCD dengan tingkat kontras yang cukup tinggi serta pengendali LCD CMOS yang terpasang dalam modul tersebut. Pengendali mempunyai pembangkit karakter ROM/RAM dan display data RAM. Semua fungsi display diatur oleh instruksi-instruksi, sehingga modul LCD ini dapat dengan dihubungkan dengan unit mikroprosesor. LCD tipe ini tersusun sebanyak dua baris dengan 16 karakter.

Masukan yang diperlukan untuk mengendalikan modul berupa bus data yang masih termultiplek dengan bus alamat serta tiga sinyal control. Sementara pengendalian LCD dilakukan secara internal oleh kontroler yang sudah terpasang dalam modul LCD. Diagram blok untuk LCD dapat dilihat dalam gambar 2.5.



Gambar 2.6 Diagram Blok LCD M1632
Sumber: Datasheet LCD M1632

LCD modul M1632 mempunyai spesifikasi perangkat keras sebagai berikut :

1. 16 kareakter dan 2 baris tampilan yang terdiri dari 5 x 7 dot matrik ditambah kursor
2. Pembangkit karakter ROM untuk 192 jenis karakter
3. Pembangkit karakter RAM untuk 8 jenis karakter
4. 80 x 8 display data RAM (maksimum 8 karakter)
5. Osilator internal
6. Catu daya +5 volt
7. Secara otomatis akan reset saat catu daya dinyalakan

LCD M1632 mempunyai 16 pin atau penyemat yang mempunyai fungsi-fungsi seperti yang ditunjukkan dalam Table 2.3.

Tabel 2.3.

Fungsi pin-pin LCD M1632

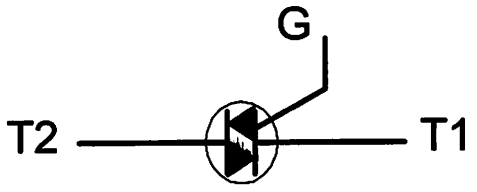
No	Nama Penyemat	Fungsi
1	Vss	Terminal Ground
2	Vcc	Tegangan catu +5 volt
3	Vee	Drive LCD
4	RS	Sinyal pemilih register 0: Instruksi register (tulis) 1: Data Register (tulis dan baca)
5	R/W	Sinyal seleksi tulis dan baca 0: Tulis 1:Baca
6	E	Sinyal operasi awal,sinyal ini mengaktifkan data dan baca
7-14	DB0-DB7	Merupakan saluran data, berisi perintah dan data yang akan ditampilkan
15	V+ BL	Pengendali kecerahan latar belakang LCD 4-4,42 dan 50-500mA
16	V- BL	Pengendali kecerahan latar belakang LCD 0V

2.5. TRIAC

Triac adalah sebuah semikonduktor arus bolak-balik yang akan menghantar jika diberi sinyal energi rendah ke bagian gerbangnya (gate). Triac menghantar dalam dua arah. Triac dapat disulut oleh arus searah, arus bolak-balik ataupun pulsa.

Karena Triac mampu dilalui arus bolak-balik maka penamaan terminalnya T1, T2, G dengan ketentuan T1 dan T2 adalah terminal pembawa arus dan G adalah terminal pemicu triac. Telah menjadi standar praktek yaitu dengan memakai T1 sebagai titik referensi untuk arus dan tegangan yang diberikan kepada triac.

Perancangan ini menggunakan sumber AC dari jala-jala PLN yang memiliki tegangan sebesar 220V, agar dalam proses pemanasan diperoleh suhu yang stabil yaitu 80 ^{0}C maka digunakan Triac *(triode alternating current)*. Simbol triac ditunjukkan dalam Gambar 2.6.



Gambar 2.7 Simbol TRIAC
Sumber: Prinsip-prinsip Elektronika jilid 1. Malvino

Kelebihan triac dari saklar mekanik dan relay adalah tidak adanya bunga api dan mempunyai kecepatan operasi yang tinggi sehingga menghasilkan kontrol arus yang teliti.

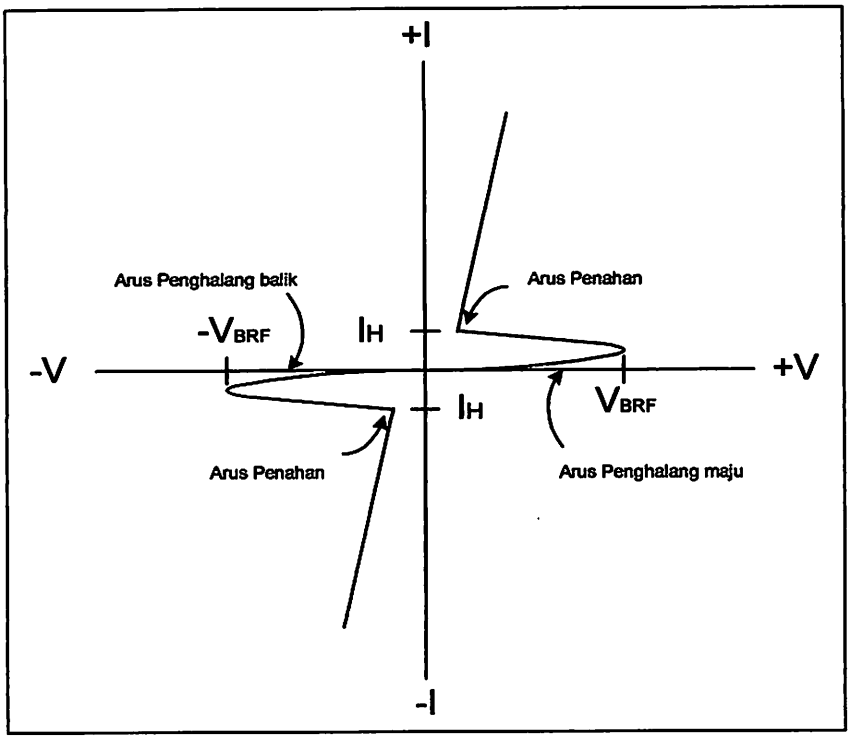
Triac mempunyai dua karakteristik penting, yaitu :

1. Suatu triac akan tetap dalam keadaan tidak menghantar meskipun di bias maju sampai V_{BRF} (tegangan *breakover*) majunya tercapai.
2. Nilai V_{BRF} ini dapat dikontrol dengan merubah besarnya arus gerbang I_G, sehingga memberikan kemampuan pada triac untuk mengontrol arus beban yang sangat besar dengan mengatur arus gerbang yang sangat kecil.

Ketika triac di bias dengan suatu tegangan V/-V, arus I/-I akan tetap kecil, disebut arus penghalang maju, sampai V_{BRF} tercapai. Bila ini terjadi, arusnya akan meningkat tajam dan jatuh tegangan pada triac menjadi sangat kecil.

Triac akan tetap on selama arusnya berada di atas arus penahan, I_H (*holding current).*

Karakteristik arus-tegangan triac dengan gerbang terbuka diperlihatkan dalam Gambar 2.7.



Gambar 2.8 Karakteristik Arus-Tegangan Triac Dengan Gerbang Terbuka
Sumber: Prinsip-prinsip Elektronika jilid 1. Malvino

2.5.1. Cara kerja TRIAC

T1 sebagai titik referensi Vdrm adalah batas tegangan maksimum dimana TRIAC masih dapat menahan dimana konduksi dari kedua arah. Jika tegangan yang diberikan pada TRIAC melebihi tegangan maksimum, maka TRIAC akan berkonduksi walaupun tidak ada penyulutan pada terminal gerbang (gate). Dalam keadaan ini TRIAC tidak akan rusak karena arusnya tetap dibatasi,

tetapi TRIAC akan kehilangan kemampuan kendalinya. Aplikasi jenis TRIAC yang baik adalah mempunyai tegangan Vdrm yang sama dengan tegangan puncak dari gelombang AC, sehingga diperoleh pengendalian yang baik. Arus genggam (I_H) adalah arus minimum yang dibutuhkan TRIAC arar tetap berkonduksi. Pada saat arus gate menurun di bawah I_H, maka TRIAC berhenti berkonduksi dan menuju keadaan menyumbat. Idrm adalah arus bocor yang timbul pada saat Vdrm diberikan pada saat Vdrm pada terminal T1 dan T2.

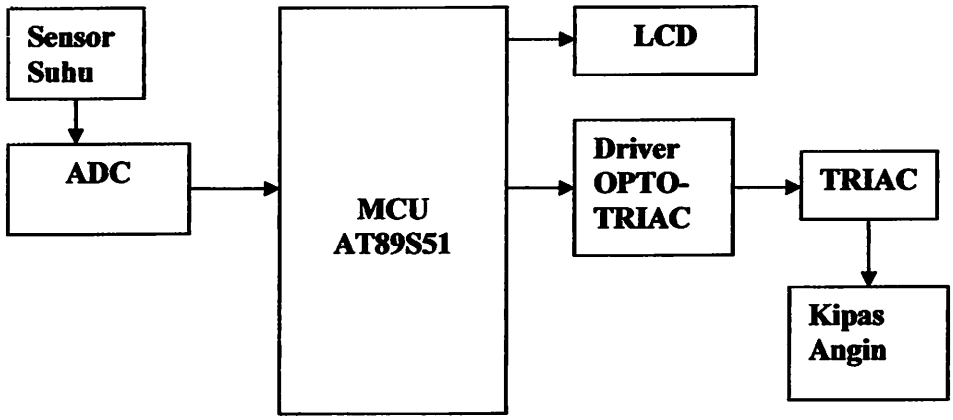
Untuk beban induktif, pergeseran fasa antara arus dan tegangan berarti bahwa pada saat arus turun di bawah I_H dan TRIAC menyumbat, akan ada tegangan yang melintas di antara TRIAC. Jika tegangan ini muncul terlalu cepat dan lebih besar daripada tegangan *breakdown* maksimal, maka TRIAC akan tetapi konduksi walau tidak ada penyulutan, sehingga TRIAC jadi tidak terkendali. Untuk dapat mengendalikan, maka derajat kenaikan tegangan terhadap waktu (dv/dt) harus dibatasi oleh rangkaian RC melintasi di antaraT1 dan T2. Kapasitor akan membatasi kenaikan arus yang mendadak pada saat TRIAC disulut. Pada alat ini digunakan TRIAC Q4004. TRIAC ini mampu menahan arus maju hingga 4A pada tegangan maksimal 400V, daya maksimumnya 1600W. Arus penyulutan maksimal adalah 15 mA. TRIAC ini dirangkai dengan optoisolator membentuk rangkaian saklar elektronik.

BAB III
PERENCANAAN DAN PEMBUATAN ALAT

Bab ini membahas pembuatan alat pengaturan kecepatan dengan kipas angin berbasis mikrokontroller AT89S51. Pembuatan alat disini dibagi dalam beberapa blok perangkat yang mempunyai fungsi sendiri-sendiri. Pembuatan sistem meliputi pembuatan perangkat keras dan perangkat lunak.

3.1. Perencanaan Perangkat Keras

Diagram blok sistem pengaturan kecepatan kipas angin berbasis mikrokontroller AT89S51 dapat dilihat dalam Gambar 3.1.



Gambar 3.1 Blok Diagram Blok Diagram Pengaturan Kecepatan Kipas Angin Menggunakan Mikrokontroler AT89S51

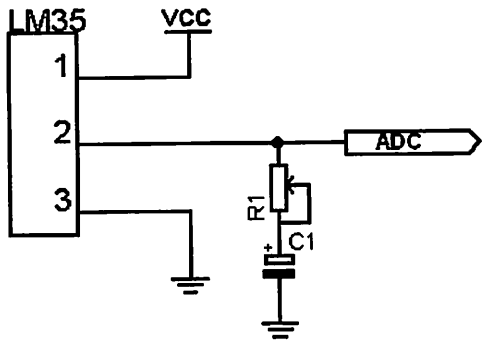
Penjelasan dari masing-masing blok adalah sebagai berikut :

1. Sensor suhu, berfungsi untuk mengubah suhu dari sensor yang ada di ruangan menjadi tegangan.
2. Rangkaian ADC, rangkaian ADC akan mendekodekan tegangan analog ke biner.
3. Mikrokontroller AT89S51 sebagai pengolah data dari keseluruhan sistem. Mikrokontroller ini mempunyai internal ROM 4kbyte sehingga tidak memerlukan memory program external, mempunyai 4 port I/O 8bit dan bekerja dengan tegangan catu single suply 5 volt.
4. Driver Triac Diac ini dimanfaatkan sebagai *triac driver* sekaligus sebagai isolasi antara rangkaian mikrokontroler dengan beban AC.
5. Triac, Triac ini digunakan untuk mengendalikan daya beban yaitu kipas angin.
6. Kipas angin sebagai target pengaturan kecepatan putaran.
7. LCD digunakan untuk menampilkan data suhu dari Mikrokontroler.

3.1.1 Perencanaan Sensor Suhu

Sensor suhu yang digunakan pada perencanaan alat ini adalah IC LM 35. LM 35 merupakan pengindera suhu yang memberikan tegangan keluaran berbanding langsung dengan suhu yang diukurnya, dalam derajat Celcius. Ini berarti bahwa kalau suhu 0°C, tegangan keluarannya adalah 0 Volt.

Adapun gambar dari rangkaian sensor suhu adalah sebagai berikut :



Gambar 3.2 Rangkaian Sensor Suhu

Dimana : Pin 1 sebagai Vcc dengan catu daya sebesar +5V

Pin 2 merupakan keluaran dari sensor suhu

Pin 3 sebagai Ground

Tegangan keluaran yang diberikan sensor ketika proses pengindraan temperatur adalah :

$$Vout = Temp \times 10mV/°C$$

Dimana : Vout adalah tegangan ouput dari sensor LM 35 (Volt)

Temp adalah besaran suhu yang dibaca (°C)

Misalnya suhu mencapai 25°C maka tegangan output dari sensor adalah :

$$Vout = 25 \times 10mV/°C$$

$$Vout = 250\ mV = 0{,}25\ V$$

Fungsi dari R dan C yang dipasang seri ke ground pada output sensor LM 35 adalah menyesuaikan impedansi dengan rangkaian selanjutnya.

3.1.2. Perencanaan rangkaian ADC *(Analog to Digital Converter)*

Rangkaian ADC ini berfungsi sebagai untuk merubah besaran analog menjadi besaran digital agar nantinya dapat diperoleh data masukan bagi mikrokontroler. Jadi sinyal keluaran dari sensor adalah sinyal analog yang harus diubah menjadi sinyal digital agar dapat diinterfacekan, sehingga dapat dibaca oleh program mikrokontroler.

Untuk rangkaian pengkonversi data analog ke digital (ADC) digunakan IC ADC 0804. Dengan sebuah masukan yaitu Vin + (pin 6) dan delapan buah keluaran yaitu DB0-DB7 (pin 18-pin 11). ADC bekerja dengan tegangan referensi sebesar 2,5 V pada Vref/2 atau pin 9 yang didapat dari resistor pembagi tegangan (sesuai data sheet). Fungsi dari rangkaian referensi ini adalah untuk mendapatkan resolusi 1 bit yang dinginkan.

ADC ini mempunyai range antara 0 sampai 5 Volt dengan menggunakan pencatu daya +5 Volt. ADC 0804 telah dilengkapi dengan clock internal yang secara runing dan dapat diaktifkan dengan menghubungkan komponen resistor eksternal dan komponen capasitor eksternal pada clock R dan clock IN. Untuk menghasilkan sinyal clock nilai R ditentukan sebesar 10 K dan nilai C sebesar 150 pF sehingga memberikan frekuensi clock sebesar :

$$Fclk = \frac{1}{1{,}1xRC}$$

$$= \frac{1}{1{,}1x10K\Omega x150pF}$$

$$= 606{,}6 \text{ KHz}$$

Dari perhitungan diatas dapat dilihat bahwa harga frekuensi yand didapatkan sudah memenuhi harga yang diminta ADC 0804 berdasarkan data sheetnya yaitu 640 KHz.

ADC ini dirancang dapat menerima masukan 0 Volt sampai 5 Volt. Tegangan referensi Vref/2 diset 2,5 Volt sesuai dengan data sheet, maka untuk perhitungan resolusi setiap 1 bitnya berbobot :

$$\text{Resolusi 1 bit} = \frac{Vref}{2^n - 1} = (\text{n = banyaknya data per bit } 2^8 = 256)$$

$$= \frac{5}{255} = 0{,}02 \text{ Volt}$$

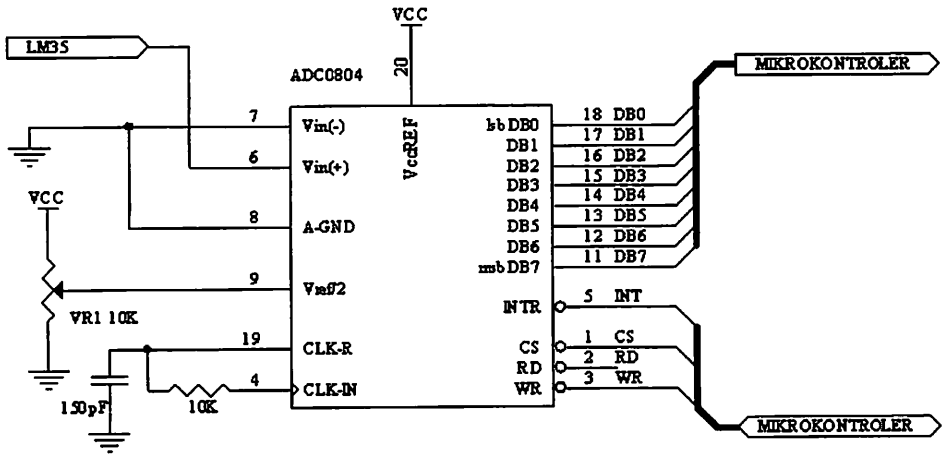
Untuk perhitungan pada suhu 25°C maka keluaran tegangan yang dihasilkan oleh sensor suhu adalah 0,25 Volt. Sehingga output digital bilangan Hex dari ADC 0804 adalah :

$$\text{ADC output} = \frac{Vin}{\text{Re}solusi}$$

$$= \frac{0{,}25}{0{,}02}$$

$$= 12{,}5 \text{ atau } 0\text{C H}$$

Gambar dari rangkaian ADC ditunjukkan pada gambar berikut :



Gambar 3.3 Rangkaian ADC 0804

3.1.3. Perencanaan Port Mikrokontroler AT89S51

Dalam hal ini perencanaan port pada minimum sistem AT89S51 adalah sebagai berikut :

1. EA/Vpp

   Dihubungkan dengan sumber +5 Volt.

2. Port 0

   Merupakan Bus alamat rendah (A0-A6), Digunakan sebagai data LCD.

3. Port 1

   Merupakan port I/O dua arah dengan internal pull-up digunakan sebagai data input dari ADC.

4. Port 3

Merupakan port dengan alamat tinggi. Disini hanya menggunakan alamat port 3.1 sebagai output mengatur kecepatan kipas angin melaui driver TRIAC.

5. Port 2

   Digunakan sebagai pengontrol ADC dan LCD.

6. RST *(Reset)*

   Sebagai input reset master AT89S51.

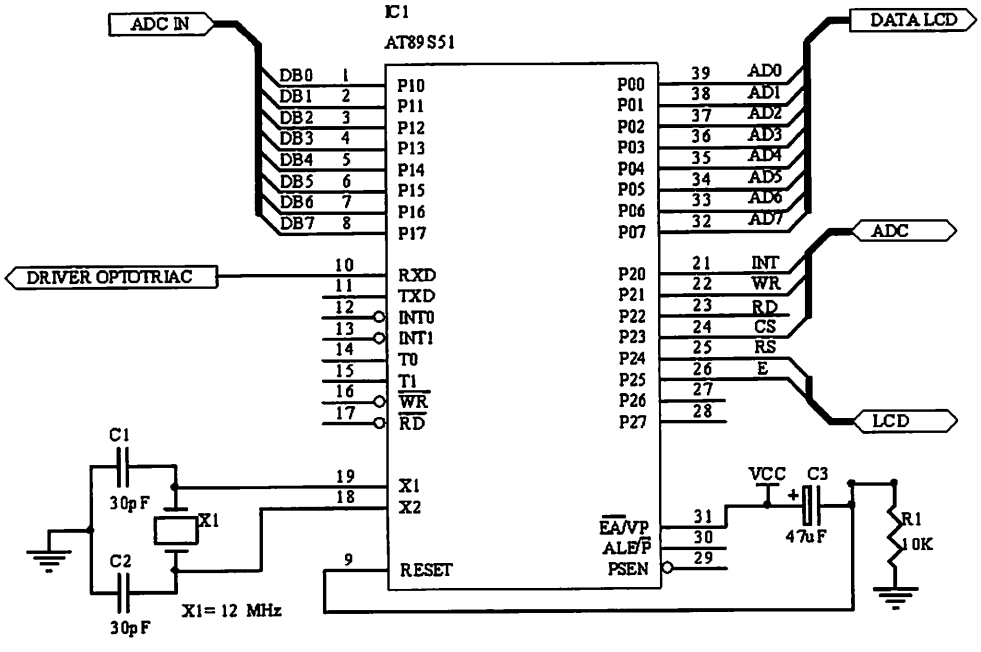
7. X_1 dan X_2

   Dihubungkan dengan rangkaian clock minimum sistem.

8. GND *(Ground)*

   Dihubungkan dengan negatif dari supply tegangan.

Gambar dari perencanaan port-port pada mikrokontroler adalah sebagai berikut :

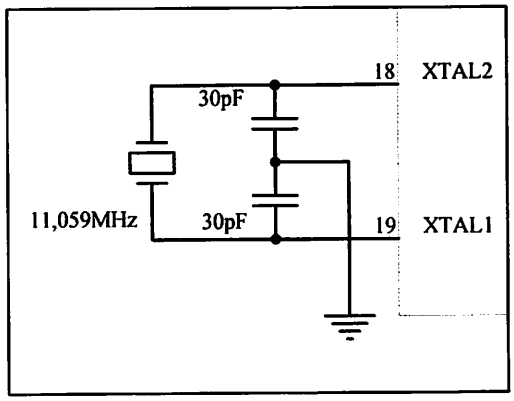


Gambar 3.4 Rangkaian Mikrokontroler

- **Sistem Pewaktuan Mikrokontroller**

Kecepatan proses yang dilakukan oleh mikrokontroler ditentukan oleh sumber *clock* (pewaktuan) yang mengendalikan mikrokontroler tersebut. Sistem yang dirancang ini seperti terlihat pada Gambar 4.10 akan menggunakan osilator internal yang sudah tersedia di dalam chip mikrokontroller. Untuk menentukan frekuensi osilatornya cukup dengan cara menghubungkan kristal pada pin XTAL1 dan XTAL2 serta dua buah kapasitor ke ground. Besar kapasitansinya disesuaikan dengan spesifikasi pada lembar data mikrokontroller yaitu 30 pF.

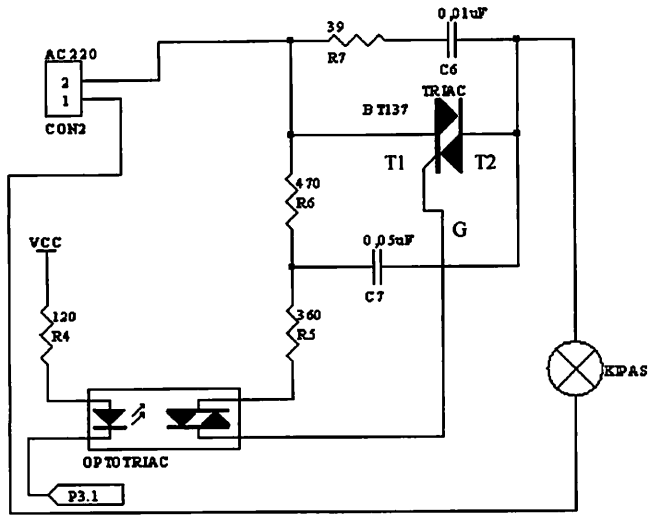
Pemilihan besar frekuensi kristal disesuaikan dengan pemilihan kecepatan yang diharapkan untuk transfer data melalui pin *serial interface* mikrokontroller tersebut. Dengan memakai kristal 11,059 MHz, maka satu siklus mesin membutuhkan waktu selama 1,08 mikrodetik atau 1/11,059 MHz x 12 periode.



Gambar 3.5 Rangkaian Pewaktuan

3.1.4 Rangkaian Optotriac dan Triac

Untuk mengendalikan daya beban kipas digunakan triac BT317 sebagai drivernya. Sedangkan sebagai driver triac digunakan optotriac MOC 3020 yang juga berfungsi sebagai isolasi antara rangkaian mikrokontroler dengan beban analog (lampu infra merah). Rangkaian optotriac dan triac ini dapat dilihat dalam Gambar 3.6.



Gambar 3.6 Rangkaian optotriac dan triac

Dari karakteristik elektrik optotriac diketahui bahwa dan pada saat arus majunya 30mA maka besar tegangan maju pada LED adalah 1,5V. Dengan menggunakan tegangan catu (Vcc) = 5V, maka besar R_4 adalah :

$$Vcc = VR_4 + V_{DI}$$

$$5 = VR_4 + 1,5$$

$$VR4 = 3,5V$$

$$R4 = \frac{VR5}{Ir} = \frac{3,5V}{30.10^{-3}} = 120\,\Omega$$

Terminal 1 (MT1) dan terminal 2 (MT2) merupakan saklar yang aliran arus beban yang mengalir dari sumber tegangan AC. Jika tidak ada arus penyulutan (*trigger*) pada gate TRIAC (Igate) maka MT1 dan MT2 tidak terhubung. Saat ada arus gate yang mengalir, maka kedua terminal ini akan terhubung meskipun tidak ada ada arus gate lagi.

Daya yang disalurkan ke beban tergantung pada lamanya MT1 terhubung dengan MT2 setiap setengah periode tegangan AC yakni bagian yang diarsir. Bagian yang diarsir ini menunjukkaan bahwa daya tersalurkan ke beban. Besarnya daya yang disalurkan ini dapat diatur melalui sudut perlambatan (*delay angle*) yang dimulai ketika detektor nol sudah memberikan sinyal bahwa saat itu sedang melintasi titik nol.

3.1.5 Display LCD 16x2

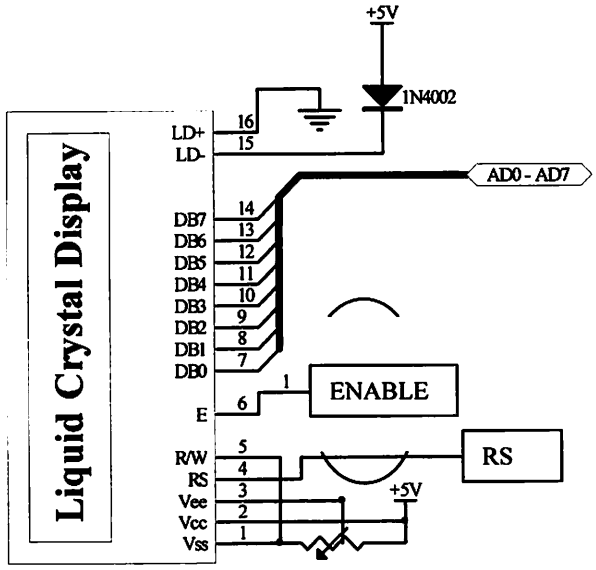
Dalam aplikasi ini menggunakan sebuah layar LCD (*Liquid Crystal Display*) yaitu jenis TM202A yang merupakan LCD dua baris dengan setiap barisnya terdiri atas 20 karakter. Penyemat LCD dan fungsinya ditunjukkan dalam Tabel 3.1.

Masukan yang diperlukan untuk mengendalikan modul ini berupa bus data yang masih termultiplek dengan bus alamat serta 3 bit sinyal kontrol. Sementara pengendalian dot matrik LCD dilakukan secara internal oleh kontroler yang sudah terpasang pada modul LCD.

Tabel 3.1
Fungsi penyemat LCD

Penyemat	Fungsi
DB0-DB7	Merupakan saluran data, berisi perintah dan data yang akan ditampilkan di LCD
Enable	Sinyal operasi awal, sinyal ini mengaktifkan data tulis atau baca
R/W	Sinyal seleksi tulis atau baca 0 : tulis 1 : baca
RS	Sinyal pemilih register 0 : instruksi register (tulis) 1 : data register (baca dan tulis)

Rangkaian display ditunjukkan dalam Gambar 3.10. Saluran data DB_0-DB_7 dihubungan pada *port* 0 Mikrokontroler AT89C51. Sedangkan penyemat R/W dihubungkan ke ground dan RS ke *port* 2.4 mikrokontroler AT89S51. Penyemat V_{ee} dihubungkan pada potensiometer 1 kΩ, untuk mengatur kecerahan LCD.



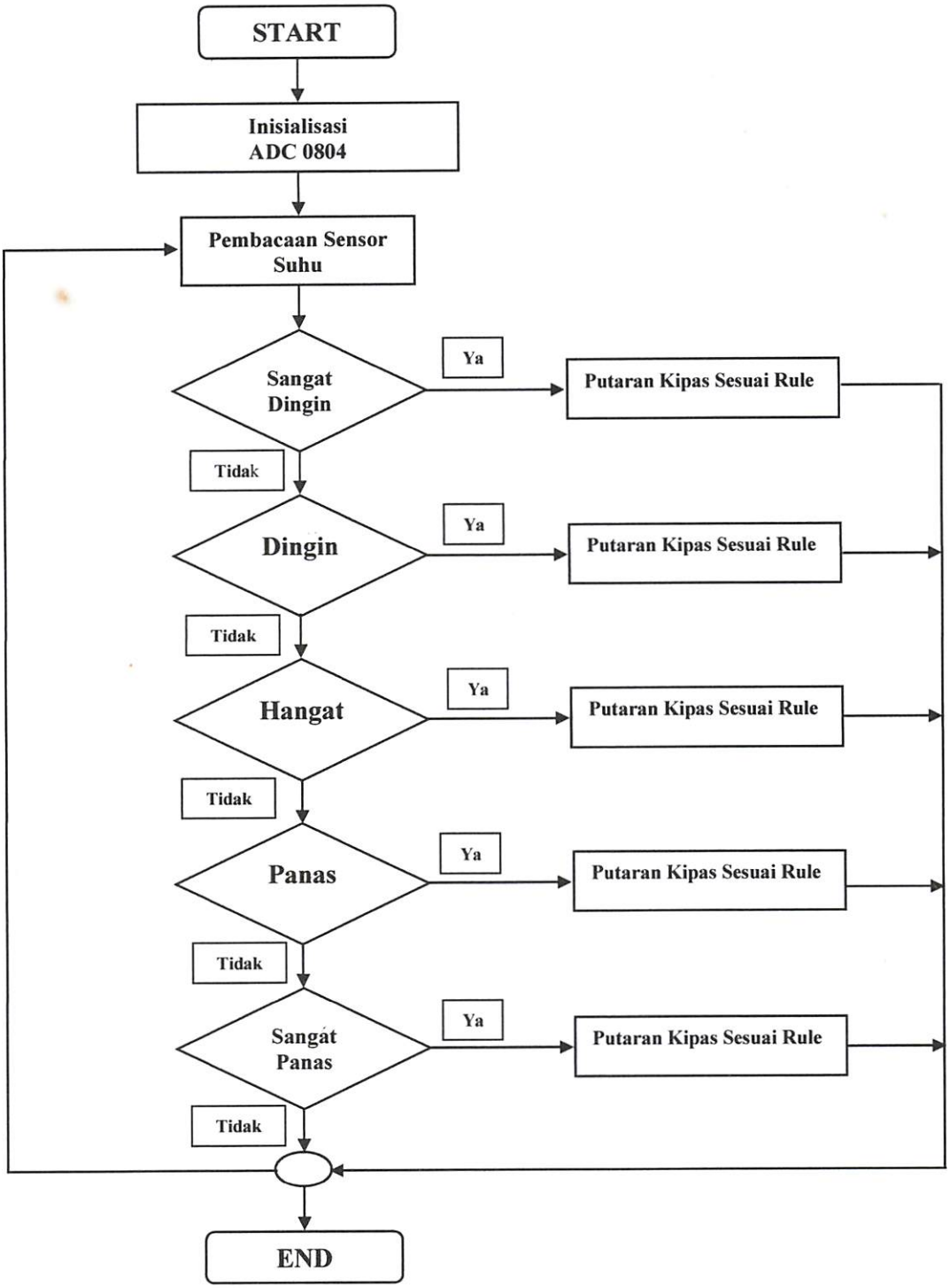
Gambar 3.7 Rangkaian LCD (*Liquid Crystal Display*)

3.2. Perencanaan Perangkat Lunak

Pada tahap ini kita akan melewati beberapa langkah yaitu :

1. Mendesain Crisp Input dan Crisp Output. Disini kita menentukan nama dan nilai (min dan max) dari input dan output sesuai dengan yang kita butuhkan.
2. Mendesain Input dan Output Membership Function. Pada langkah ini kita dapat menentukan bentuk membership function dari crisp input dan crisp output
3. Mendesain rule. Tujuan dari mendesain rule adalah untuk menentukan aturan-aturan yang akan diperlakukan pada hardware yang telah kita buat.

Secara garis besar program dalam pembuatan alat control pengaturan kecepatan kipas angin dapat dilihat pada gambar berikut :



Gambar 3.8 Flowchart Sistem Pengaturan Putaran Kipas Angin

BAB IV
PENGUJIAN ALAT

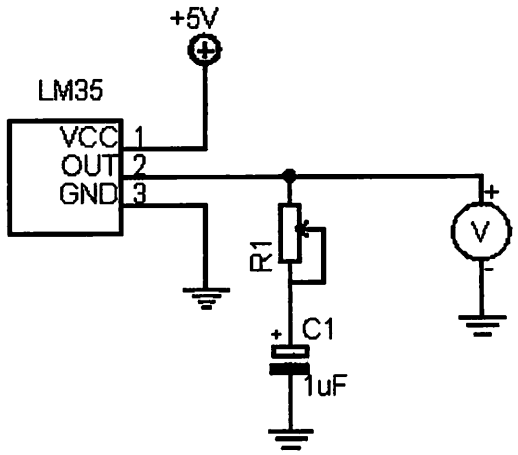
4.1. Pengujian *Hardware*

Dalam bab ini akan dibahas mengenai pengujian terhadap peralatan yang dibuat, guna untuk mengetahui kinerja atau proses dari peralatan tersebut. Setelah tahap pengujian kemudian dilanjutkan dengan tahap pengambilan data terhadap rangkaian – rangkaian dalam per blok.

Pengujian alat meliputi pengujian *Hardware* yang berupa pengujian sensor suhu, pengujian ADC 0804, rangkaian *Driver Optotriac* dan *Triac* dan pengujian LCD .Pengujian *hardware* bertujuan untuk mengetahui kinerja sistem dalam tiap bloknya. Selain itu untuk mengetahui apakah kinerja sistem maksimal atau tidak apabila dihubungkan dengan program.

4.1.1. Pengujian Rangkaian Sensor Suhu

Pengujian rangkaian sensor suhu ini dilakukan untuk mengetahui berapa tegangan output dari sensor suhu pada setiap perubahan suhu. Berikut ini merupakan gambar pengujian dari rangkaian sensor suhu.



Gambar 4.1 Pengujian Rangkaian Sensor Suhu

Pengujian suhu yang akan diukur adalah 20°C - 50°C. Berikut ini merupakan tabel hasil dari pengujian dan pengukuran alat.

Tabel 4.1.
Hasil Pengujian Pada Rangkaian Sensor Suhu

No	Pembacaan Suhu		Error
	Pengukuran (°C)	Alat (Tampilan LCD)	
1.	20	20	0
2.	25	25	0
3.	30	30	0
4.	35	35	0
5.	40	40	0
6.	45	45	0
7.	50	50	0
		Jumlah Error	0

$$\text{Eror rata-rata} = \frac{\Sigma_{Error}}{n}$$

$$= \frac{0}{7}$$

$$= 0$$

= 350mV = 0,35V

- Vo = 40°C X 10mV/°C

= 400mV = 0,4V

- Vo = 45°C X 10mV/°C

= 450mV = 0,45V

- Vo = 50°C X 10mV/°C

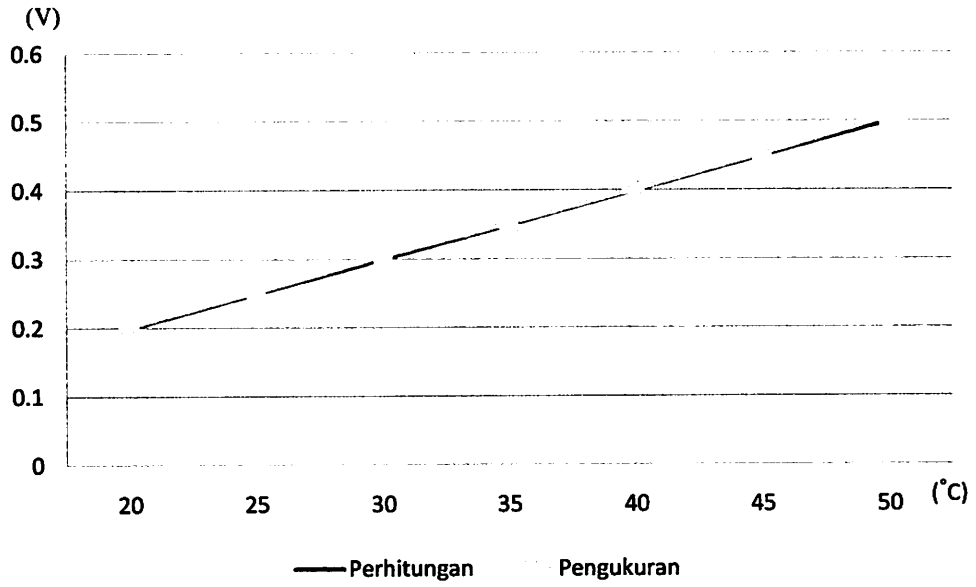
= 500mV = 0,5V

Dari pengukuran maupun perhitungan maka dapat dibuat suatu tabel hasil :

Tabel 4.2.
Perbandingan Hasil Pengukuran maupun Perhitungan Sensor Suhu

No.	Sensor	Pengukuran	Perhitungan
		Vo sensor (Volt)	Vo sensor (Volt)
1.	20°C	0,202	0,2
2.	25°C	0,252	0,25
3.	30°C	0,305	0,30
4.	35°C	0,352	0,35
5.	40°C	0,401	0,40
6.	45°C	0,452	0,45
7.	50°C	0,506	0,50

Grafik 4.2.
Hasil Pengukuran dan Perhitungan Sensor Suhu



Dari tabel perhitungan dan pengukuran, maka dapat dicari besar kesalahannya dengan menggunakan rumus :

$$E = \frac{Perhitungan - Pengukuran}{Perhitungan} X\,100\%$$

Dimana :

E (error) = Kesalahan relatif

Analisa data error hasil pengukuran dan perhitungan sensor suhu sebagai berikut :

- $E = \frac{0{,}2 - 0{,}202}{0{,}2} X100\%$

  $= 1\,\%$

- $E = \frac{0{,}25 - 0{,}252}{0{,}25} X100\%$

  $= 0{,}8\,\%$

$$- \text{ E } = \frac{0,3 - 0,305}{0,3} X100\%$$

$$= 1,6\ \%$$

$$- \text{ E } = \frac{0,35 - 0,352}{0,35} X100\%$$

$$= 0,5\ \%$$

$$- \text{ E } = \frac{0,4 - 0,401}{0,4} X100\%$$

$$= 0,2\ \%$$

$$- \text{ E } = \frac{0,45 - 0,452}{0,45} X100\%$$

$$= 0,4\ \%$$

$$- \text{ E } = \frac{0,50 - 0,506}{0,5} X100\%$$

$$= 1,2\ \%$$

Tabel 4.3.
Error Hasil Pengukuran dan Perhitungan Sensor Suhu

No	Suhu (°C)	Vo sensor Perhitungan (V)	Vo sensor Pengukuran (V)	Error (%)
1.	20	0,2	0,202	1
2.	25	0,25	0,252	0,8
3.	30	0,30	0,305	1,6
4.	35	0,35	0,352	0,5
5.	40	0,40	0,401	0,2
6.	45	0,45	0,452	0,4
7.	50	0,50	0,506	1,2
		Jumlah Error		5,7

$$\text{Error rata-rata} = \frac{\sum error}{X}$$

Dimana ,

Σerror = Jumlah error

X = Banyaknya data

Error rata-rata pada output sensor suhu adalah

Σerror = 1 + 0.8 + 1,6 + 0.5 +0.2 + 0.4 + 1,2

= 5,7 %

X = 7

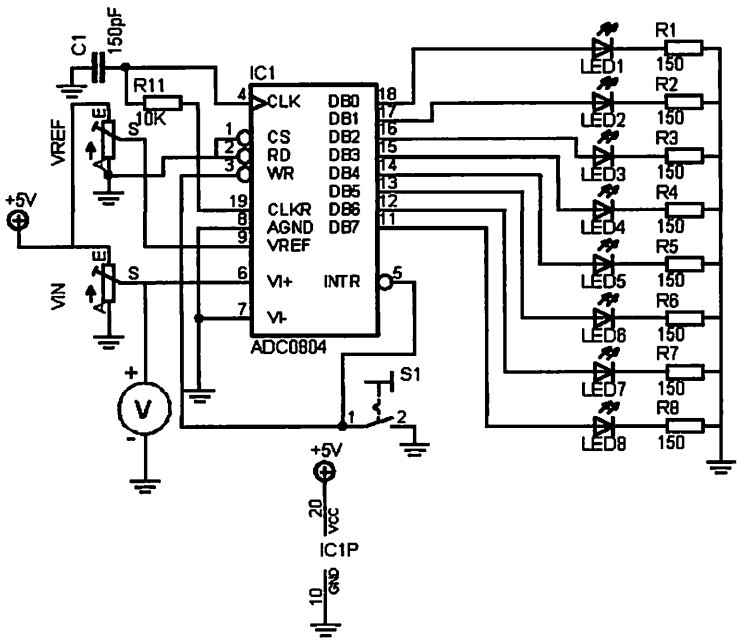
$$Error\ rata-rata = \frac{5,7}{7}$$

= 0,814 %

Hasil error rata-rata dari perbandingan antara pengukuran dan perhitungan pada output LM35 adalah 0,814.

4.1.2. Pengujian IC ADC 0804

Tujuan pengujian ADC adalah untuk mengetahui level tegangan ADC dan keluaran kelinieran hasil konversi ADC. Peralatan yang digunakan dalam pengujian ADC antara lain : Modul ADC, LED Display, Sumber tegangan DC variabel dengan besarnya tegangan input 5 Volt. Proses pengujiannya seperti pada gambar dibawah ini :



Gambar 4.2. Pengujian Rangkaian ADC0804

Data hasil pengujian ADC 0804 dapat ditunjukan pada tabel berikut ini

:

Tabel 4.4.
Hasil Pengujian Rangkaian ADC 0804

V Input	Output ADC								Vout Dec	Vout Hex
	D0	D1	D2	D3	D4	D5	D6	D7		
0.00	0	0	0	0	0	0	0	0	0	0
0.50	0	0	0	1	1	0	0	1	25	19
0.92	0	0	1	1	0	0	1	0	50	32
1.52	0	1	0	0	1	0	1	1	75	4B
2.04	0	1	1	0	0	1	0	0	100	64
2.52	0	1	1	1	1	1	0	1	125	7B
3.04	1	0	0	1	0	1	1	0	150	96
3.54	1	0	1	0	1	1	1	1	175	AF
4.00	1	1	0	0	1	0	0	0	200	C8
4.47	1	1	1	0	0	0	0	1	225	E1
4.98	1	1	1	1	1	0	1	0	250	F8

Keterangan alat yang digunakan:

- LED display
- Catu daya 5 volt DC
- Multimeter Digital
- Vref diatur 2.50 Volt

Dari tabel diatas akan dicari tegangan keluaran sehingga dapat diketahui karakteristik output dari rangkaian ADC. Untuk mendapatkan nilai Vout dapat digunakan persamaan sebagai berikut :

$$Vout = \frac{Vin}{Vref}(2^n - 1)$$

Dimana :$2^n = 256$ dengan Vref = 5 volt

Contoh datanya adalah 0.5V maka :

$$Vout = \frac{0.5}{5}(256 - 1)$$

$$= 25.5 \text{ Desimal}$$

Dan presentase kesalahannya dapat dihitung dengan persamaan dibawah ini :

$$\%\ error = \frac{Vout\ uji - Vout\ Hitung}{Vout\ Hitung} X100\%$$

Jika Vin = 0.5 Volt maka :

$$= \frac{25 - 25.5}{25.5} x100\%$$

$$= 1{,}96\%$$

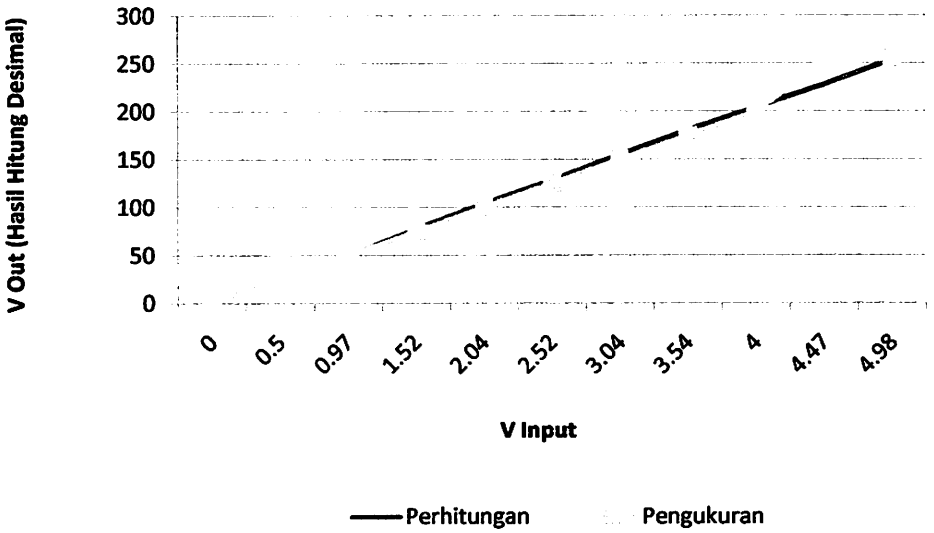
Dengan cara yang sama untuk masing-masing masukan dapat diketahui prosentase kesalahannya.

Tabel 4.5.
Kesalahan (Tingkat Error) dari pengujian ADC

V input (Volt)	DATA		%Error
	Vout (hasil uji)	Vout (hasil hitung) (Desimal)	
0.00	0	0.00	0.00
0.50	25	25.50	1.96
0.97	50	49.47	1.07
1.52	75	77.52	3.74
2.04	100	104.04	3.86
2.52	125	128.52	2.73
3.04	150	155.04	3.25
3.54	175	180.54	3.06
4.00	200	204.00	1.96
4.47	250	227.97	1.30
4.98	255	253.98	1.56
Total Error			24,49
Rata-rata Error			2,23

Grafik 4.5.

Hasil Kesalahan (Tingkat Error) dari pengujian ADC



Dari hasil pengujian dapat dianalisis bahwa keluaran tegangan ADC berbeda beda untuk tiap masukannya (Vinput) yang diberikan, dimana ADC diberi tegangan 0 Volt – 5 Volt mendekati dengan nilai biner atau hex. Setelah diuji dengan beberapa keadaan didapatkan % *error* sebesar 2.23%. Penggunaan ADC harus disesuaikan dengan tingkat resolusi bitnya dimana besarnya resolusi bit dari ADC 0804 tersebut adalah = $Vref/2^{nbit}$ dengan n bit = 8 bit.

4.1.3 Pengujian Rangkaian Optotriac dan Triac

Pengujian rangkaian optotriac dan triac ini dilakukan dengan perangkat lunak yang diprogram ke dalam mikrokontroler. Pengujian ini bertujuan untuk mengetahui apakah tingkat kecerahan lampu infra merah dapat dikendalikan oleh mikrokontroler. Dengan adanya tingkat kecerahan lampu infra merah yang berbeda-beda, maka besar tegangan dan daya heater juga akan berbeda-beda. Besar frekuensi dari tegangan jala-jala PLN adalah 50Hz, sehingga periodenya 20ms. Karena pengaturan waktu tunda perlambatan dilakukan setiap setengah gelombang, maka periode maksimalnya adalah 10ms. Jika dikonversikan ke dalam besar sudut perlambatan, maka 10ms senilai dengan 180°. Dalam perancangan alat ini sudut perlambatan akan dibagi dalam 30 tingkat dengan kenaikan perstep adalah 6°.

- **Peralatan yang Diperlukan**

1. Mikrokontroler
2. Lampu infra merah
3. Catu tegangan AC 220V
4. Multimeter

- **Prosedur Pengujian**

1. Membuat rangkaian pengujian seperti pada Gambar 4.3.
2. Membuat pulsa pada port mikrokontroler untuk penyalaan optotriac yang akan memicu triac konduksi.
3. Mengaktifkan catu AC.
4. Mengubah ubah tingkat kecerahan lampu dengan mengubah lebar pulsa mikrokontroler.

Pengujian untuk rangkaian optotriac dan triac ditunjukkan dalam Gambar 4.3.

Gambar 4.3. Pengujian rangkaian optotriac dan triac

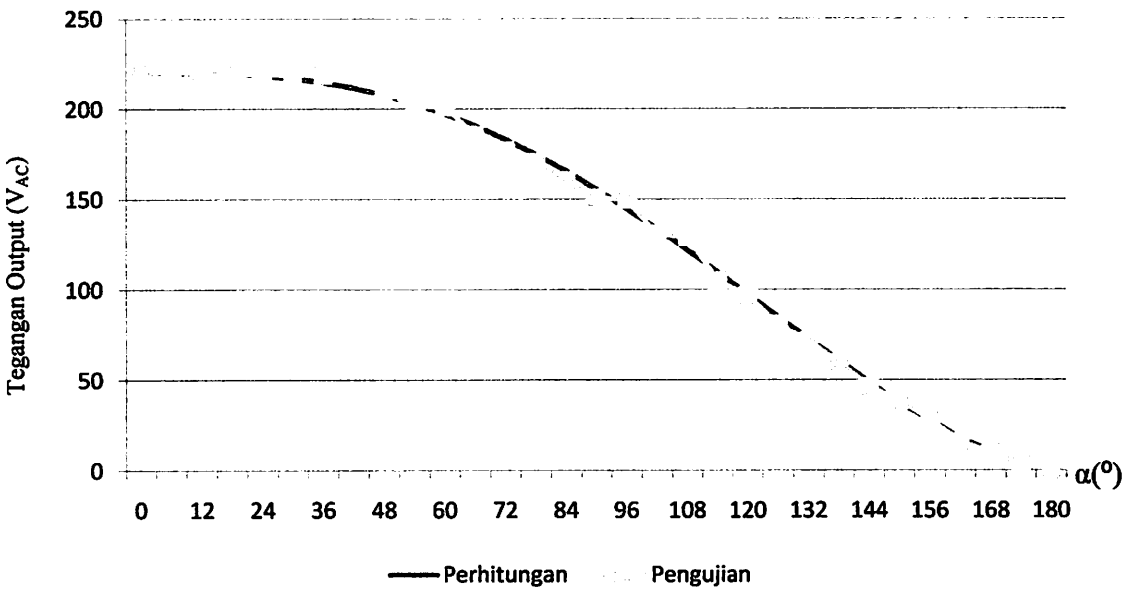
- **Hasil Pengujian**

Hasil pengujian menunjukkan bahwa dengan mengatur lebar pulsa mikrokontroller (waktu tunda perlambatan triac untuk konduksi), maka akan didapatkan tingkat kecerahan lampu yang berbeda-beda. Tingkat kecerahan lampu yang berbeda menunjukkan perubahan tegangan dan daya lampu infra merah.

Tabel 4.6.
Hasil pengujian tegangan pada Heater

No.	α (°)	t (ms)	Hasil perhitungan tegangan Heater (V)	Hasil pengujian tegangan Heater (V)	Error (%)
1.	0	0	220	219,9	0,000455
2.	6	0,33	219,9	220,2	0,001364
3.	12	0,67	219,7	219,5	0,00091
4.	18	1	219,3	219,1	0,000912
5.	24	1,33	218,38	219,0	0,002839
6.	30	1,67	216,8	218,6	0,008303
7.	36	2	214,6	218,6	0,018639
8.	42	2,33	211,6	218,7	0,033554
9.	48	2,67	207,7	210,2	0,012037
10.	54	3	202,9	200,9	0,009857
11.	60	3,33	197,37	201,3	0,019912
12.	66	3,67	190,8	185,4	0,028302
13.	72	4	183,2	176,8	0,034934
14.	78	4,33	174,8	170,4	0,025172
15.	84	4,67	165,6	160,2	0,032609
16.	90	5	155,6	150,9	0,030206
17.	96	5,33	144,9	149,8	0,033816
18.	102	5,67	1336	130,6	0,902246
19.	108	6	121,8	128,9	0,058292
20.	114	6,33	109,7	104,9	0,043756
21.	120	6,67	97,17	96,6	0,005866
22.	126	7	84,8	80,7	0,048349
23.	132	7,33	72,6	71,5	0,015152
24.	138	7,67	60,6	59,6	0,016502
25.	144	8	48,7	46,1	0,053388
26.	150	8,33	37,5	38,7	0,032
27.	156	8,67	27,8	28,0	0,007194
28.	162	9	17,6	15,8	0,102273
29.	168	9,33	10,3	10,0	0,029126
30.	174	9,67	3,1	3,5	0,129032
31.	180	10	0	0	0

Grafik 4.6.
Hasil Perhitungan dan Pengujian Tegangan Pada Heater



- **Analisis Hasil Pengujian**

  Untuk menghitung persentase kesalahan digunakan persamaan :

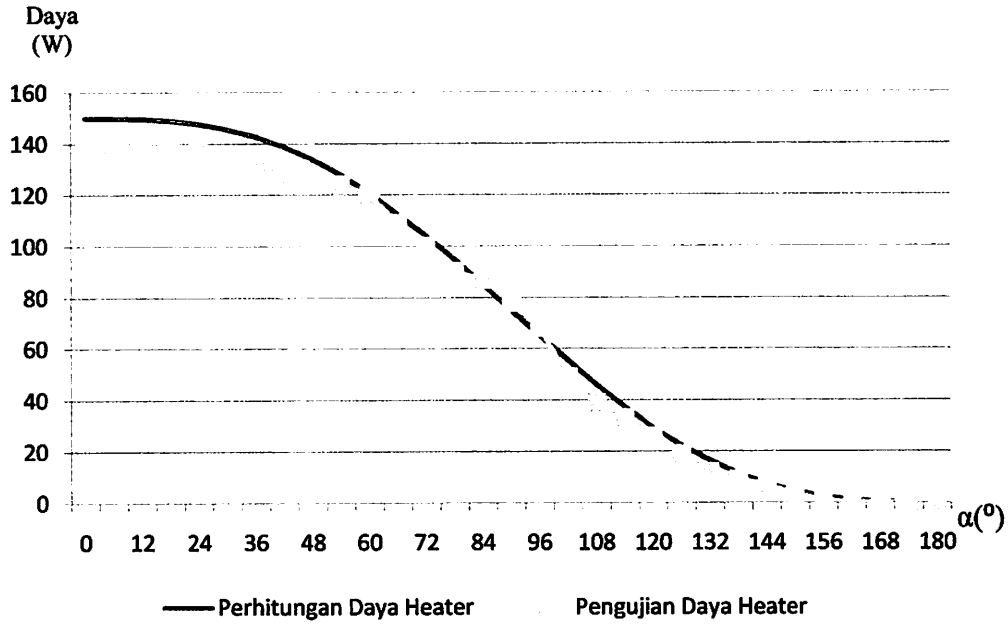
$$\text{Penyimpangan} = \left| \frac{\text{Data tegangan perhitungan - Data tegangan pengujian}}{\text{Data tegangan perhitungan}} \right| \times 100\%$$

Kesalahan rata-ratanya adalah 0,056032 %.

Tabel 4.6
Hasil Pengujian Daya Heater

No.	α (°)	t (ms)	Hasil perhitungan daya Heater (W)	Hasil pengujian daya Heater (W)	Error (%)
1.	0	0	150	140	0,066667
2.	6	0,33	149.9	139	0,072715
3.	12	0,67	149,7	139	0,071476
4.	18	1	149,0	139	0,067114
5.	24	1,33	147,8	137	0,073072
6.	30	1,67	145,6	135	0,072802
7.	36	2	142,7	133	0,067975
8.	42	2,33	138,8	128	0,07781
9.	48	2,67	133,8	126	0,058296
10.	54	3	127,7	124	0,028974
11.	60	3,33	120,7	120	0,0058
12.	66	3,67	112,3	109	0,029386
13.	72	4	104,0	100	0,038462
14.	78	4,33	94,7	90	0,04963
15.	84	4,67	85,0	87	0,023529
16.	90	5	75,0	78	0,04
17.	96	5,33	65,0	68	0,046154
18.	102	5,67	55,3	49	0,113924
19.	108	6	45,9	39	0,150327
20.	114	6,33	37,3	33	0,115282
21.	120	6,67	29,3	26	0,112628
22.	126	7	22,3	19	0,147982
23.	132	7,33	16,4	12	0,268293
24.	138	7,67	11,4	9	0,210526
25.	144	8	7,4	7	0,054054
26.	150	8,33	4,4	3	0,318182
27.	156	8,67	2,4	1	0,583333
28.	162	9	1,0	0	1
29.	168	9,33	0,3	0	1
30.	174	9,67	0,1	0	1
31.	180	10	0	0	0

Grafik 4.6
Hasil Analisa Pengujian Daya Heater



- **Analisis Hasil Pengujian**

Untuk menghitung persentase kesalahan digunakan persamaan :

$$\text{Penyimpangan} = \left| \frac{\text{Data daya perhitungan - Data daya pengujian}}{\text{Data daya perhitungan}} \right| \times 100\%$$

Kesalahan rata-ratanya adalah 0,19239977 %.

4.1.4. Pengujian Rangkaian Tampilan LCD

- **Tujuan**

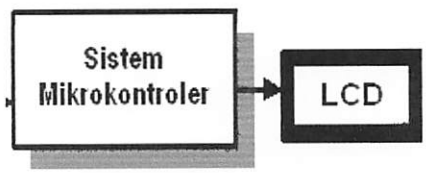
Untuk mengetahui kemampuan rangkaian tampilan yang sudah dibuat apakah dapat mendukung sistem yang direncanakan untuk memampilkan data pada LCD.

- **Peralatan yang dibutuhkan**

1. Power Supply 5 volt
2. Sistem Mikrokontroler dan LCD TM202A

- **Prosedur Pengujian**

1. Menyusun rangkaian seperti ditunjukkan dalam Gambar 4.4.
2. Menjalankan program untuk menampilkan tulisan "Suhu Ruang" ke LCD programnya terlampir
3. Mengamati keluaran pada LCD



Gambar 4.4. Diagram blok Pengujian Rangkaian Tampilan

- **Hasil dan Analisis Pengujian**

Dari hasil Pengujian dapat dilihat bahwa rangkaian tampilan dapat bekerja dengan baik.

4.2. Pengujian Perangkat Lunak

4.2.1. Tujuan

- ✓ Mengetahui kerja softrware dalam mengakses MCU AT89S51 dalam melakukan pemantauan suhu ruangan.

4.2.2. Peralatan yang digunakan

- ✓ PC (Personal Komputer).
- ✓ Rangkaian yang sudah jadi
- ✓ Box Alat
- ✓ Kebel penghubung.

4.2.3. Langkah Pengujian

- ✓ Menghubungkan koneksi antara softwere komputer dengan MCU AT89S51.
- ✓ Mengaktifkan power .
- ✓ Mengamati perubahan suhu

4.2.4. Hasil Pengujian

- ✓ Hasil pengujian pada kenaikan setiap perubahan suhu antara keluaran sensor dan display sesuai dengan yang direncanakan, jadi ini menandakan software yang dibuat sudah memenuhi ketentuan yang telah dibuat

4.3. Pengujian Sistem Secara Keseluruhan

4.3.1. Tujuan

- ✓ Mengetahui apakah sistem dapat bekerja dengan baik sesuai dengan yang direncanakan atau tidak..

4.3.2. Peralatan yang digunakan

- ✓ Keseluruhan sistem

4.3.3. Langkah Pengujian

- ✓ Mengaktifkan power.
- ✓ Membaca suhu ruangan.

✓ Mengamati apakah perubahan pada suhu akan merubah kecepatan kipas angin.

4.3.4. Hasil Pengujian

✓ Hasil pengujian keseluruhan sistem dapat di jelaskan sebagai berikut :

NO	SUHU	RPM	PUTARAN 1 DETIK
1	27	300	5
2	28	360	6
3	29	420	7
4	30	480	8
5	31	540	9
6	32	600	10
7	33	660	11
8	34	720	12
9	35	780	13
10	36	840	14
11	37	900	15
12	38	960	16
13	39	1020	17
14	40	1080	18
15	41	1140	19
16	42	1200	20
17	43	1260	21
18	44	1320	22
19	45	1380	23
20	46	1440	24
21	47	1500	25
22	48	1560	26
23	49	1620	27
24	50	1680	28

Dari hasil pengujian lama waktu dari suhu maksimal (50°C) ke suhu minimal (27°C) bekisar 20 detik.

BAB V

PENUTUP

5.1. Kesimpulan

Kesimpulan yang dapat diambil dari Pembuatan Sistem Pengaturan Kecepatan Kipas Angin Menggunakan Mikrokontroller ini adalah :

1. Hasil error rata-rata dari perbandingan antara pengukuran dan perhitungan pada output LM35 adalah 0,814 %, pada ADC memiliki error 2,23 %. Pada rangkaian driver triac diac memiliki error yaitu sebesar 0,056032 %.
2. Kipas angin disetting untuk bekerja sesuai dengan perubahan tegangan input dari sensor suhu, dimana setiap ada perubahan tegangan inputan maka akan berpengaruh pula pada kerja kipas angin

5.2. Saran

1. Penempatan sensor suhu di tempatkan pada tempat yang tepat agar suhu yang di deteksi sesuai dengan suhu ruangan sebenarnya.
2. Adanya kelemahan-kelemahan pada penulisan tugas akhir maka penulisan ini tidak dapat di jadikan bahan acuan satu-satunya, maka diperlukan pembanding dengan penulisan sejenis.
3. Sebaiknya pada layar LCD menampilkan angka di belakang koma.

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INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III

LEMBAR ASISTENSI BIMBINGAN TUGAS AKHIR

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Waktu Bimbingan : 04/02/2008 s/d 04/07/2008
Judul : Perencanaan dan Pembuatan Alat Pengaturan Kecepatan Kipas Angin Menggunakan MK AT89S51

No	Tanggal	Materi	Paraf
1.		BAB I	
2.		BAB II	
3.		BAB III	
4.		BAB IV, Perbaiki	
5.		BAB V	
6.		Acc maju	
7.			

Malang, 2008

Mengetahui
Dosen Pembimbing

(Bambang Prio Hartono, ST,MT)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III
PROGRAM STUDI TEKNIK ELEKTRONIKA
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NIM	: 01.57.107.
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Program Studi	: Teknik Elektronika.
Judul Tugas Ahkir	: Perencanaan dan Pembuatan Alat Pengaturan Kecepatan Kipas Angin Menggunakan Mikrokontroler AT89S51.

Dipertahankan di hadapan Team penguji Tugas Akhir Jenjang Diploma (D-III) :

Pada Hari	: Senin
Tanggal	: 24 Maret 2008
Dengan nilai	: 79.00 (B+)

Panitia Ujian Tugas Akhir

INSTITUT TEKNOLOGI NASIONAL MALANG

(Ir. Mochtar Asroni, MSME)
Ketua Majelis Penguji

(Ir. H Choirul Saleh, MT)
Sekretaris Majelis Penguji

Anggota Penguji

(Ir. M. Abdul Hamid, MT)
Pertama

(Ir. Taufik Hidayat, MT)
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LEMBAR PERBAIKAN TUGAS AKHIR

Telah dilakukan perbaikan oleh:

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NIM	: 01.57.107.
Jurusan	: Teknik Elektro D-III.
Program Studi	: Teknik Elektronika.
Hari/Tanggal	: Senin / 24 Maret 2008

No.	Materi Perbaikan	Paraf
1.	Validasi	
2.	Tujuan	
3.	Misal Setting Untuk Suhu yang dikehendaki 27°C, RPM kipas berapa?	
4.	Suhu naik >27°C, RPM berapa?	
5.	Kembali ke Normal waktunya berapa (lampirkan di bab IV)	

Telah Diperiksa/Disetujui:

Anggota Penguji I

(Ir. M. Abdul Hamid, MT)

Anggota Penguji II

(Ir. Taufik Hidayat, MT)

Mengetahui :
Dosen Pembimbing

(Bambang Prio H, ST, MT)

LAMPIRAN - LAMPIRAN

National Semiconductor

November 2000

LM35
Precision Centigrade Temperature Sensors

General Description

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to +110°C range (−10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full −55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 µA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ω for 1 mA load

Typical Applications

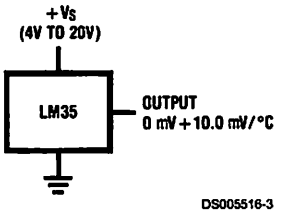
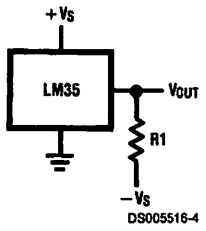


FIGURE 1. Basic Centigrade Temperature Sensor (+2°C to +150°C)

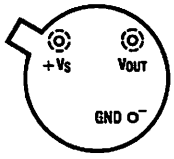


Choose $R_1 = -V_S/50\ \mu A$
V_{OUT}=+1,500 mV at +150°C
= +250 mV at +25°C
= −550 mV at −55°C

FIGURE 2. Full-Range Centigrade Temperature Sensor

Connection Diagrams

TO-46
Metal Can Package*

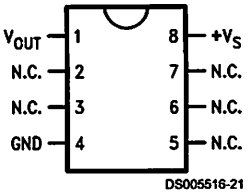


BOTTOM VIEW
DS005516-1

*Case is connected to negative pin (GND)

Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

SO-8
Small Outline Molded Package



DS005516-21

N.C. = No Connection

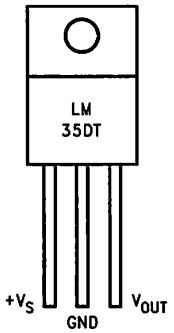
Top View
Order Number LM35DM
See NS Package Number M08A

TO-92
Plastic Package

BOTTOM VIEW
DS005516-2

Order Number LM35CZ, LM35CAZ or LM35DZ
See NS Package Number Z03A

TO-220
Plastic Package*



DS005516-24

*Tab is connected to the negative pin (GND).
Note: The LM35DT pinout is different than the discontinued LM35DP.

Order Number LM35DT
See NS Package Number TA03F

ɔlute Maximum Ratings (Note 10)

ary/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ ıtors for availability and specifications.

Voltage	+35V to −0.2V
Voltage	+6V to −1.0V
Current	10 mA
Temp.;	
6 Package,	−60°C to +180°C
2 Package,	−60°C to +150°C
Package,	−65°C to +150°C
20 Package,	−65°C to +150°C
ɛmp.:	
6 Package, ıldering, 10 seconds)	300°C
TO-92 and TO-220 Package, (Soldering, 10 seconds)	260°C
SO Package (Note 12)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	2500V
Specified Operating Temperature Range: T_{MIN} to T_{MAX} (Note 2)	
LM35, LM35A	−55°C to +150°C
LM35C, LM35CA	−40°C to +110°C
LM35D	0°C to +100°C

trical Characteristics

, 6)

ameter	Conditions	LM35A			LM35CA			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
	T_A=+25°C	±0.2	±0.5		±0.2	±0.5		°C
	T_A=−10°C	±0.3			±0.3		±1.0	°C
	T_A=T_{MAX}	±0.4	±1.0		±0.4	±1.0		°C
	T_A=T_{MIN}	±0.4	±1.0		±0.4		±1.5	°C
ity	T_{MIN}≤T_A≤T_{MAX}	**±0.18**		**±0.35**	**±0.15**		**±0.3**	°C
ain Slope)	T_{MIN}≤T_A≤T_{MAX}	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°C
ulation	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		mV/mA
)≤I_L≤1 mA	T_{MIN}≤T_A≤T_{MAX}	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
ulation	T_A=+25°C	±0.01	±0.05		±0.01	±0.05		mV/V
	4V≤V_S≤30V	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
t Current	V_S=+5V, +25°C	56	67		56	67		µA
	V_S=+5V	**105**		**131**	**91**		**114**	µA
	V_S=+30V, +25°C	56.2	68		56.2	68		µA
	V_S=+30V	**105.5**		**133**	**91.5**		**116**	µA
of t Current	4V≤V_S≤30V, +25°C	0.2	1.0		0.2	1.0		µA
	4V≤V_S≤30V	**0.5**		**2.0**	**0.5**		**2.0**	µA
ture nt of t Current		**+0.39**		**+0.5**	**+0.39**		**+0.5**	µA/°C
Temperature Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
m Stability	T_J=T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Electrical Characteristics

(Notes 1, 6)

Parameter	Conditions	LM35			LM35C, LM35D			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy, LM35, LM35C (Note 7)	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		°C
	T_A=−10°C	±0.5			±0.5		±1.5	°C
	T_A=T_{MAX}	±0.8	±1.5		±0.8		±1.5	°C
	T_A=T_{MIN}	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D (Note 7)	T_A=+25°C				±0.6	±1.5		°C
	T_A=T_{MAX}				±0.9		±2.0	°C
	T_A=T_{MIN}				±0.9		±2.0	°C
Nonlinearity (Note 8)	T_{MIN}≤T_A≤T_{MAX}	**±0.3**		**±0.5**	**±0.2**		**±0.5**	°C
Sensor Gain (Average Slope)	T_{MIN}≤T_A≤T_{MAX}	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°C
Load Regulation (Note 3) 0≤I_L≤1 mA	T_A=+25°C	±0.4	±2.0		±0.4	±2.0		mV/mA
	T_{MIN}≤T_A≤T_{MAX}	**±0.5**		**±5.0**	**±0.5**		**±5.0**	mV/mA
Line Regulation (Note 3)	T_A=+25°C	±0.01	±0.1		±0.01	±0.1		mV/V
	4V≤V_S≤30V	**±0.02**		**±0.2**	**±0.02**		**±0.2**	mV/V
Quiescent Current (Note 9)	V_S=+5V, +25°C	56	80		56	80		µA
	V_S=+5V	**105**		**158**	**91**		**138**	µA
	V_S=+30V, +25°C	56.2	82		56.2	82		µA
	V_S=+30V	**105.5**		**161**	**91.5**		**141**	µA
Change of Quiescent Current (Note 3)	4V≤V_S≤30V, +25°C	0.2	2.0		0.2	2.0		µA
	4V≤V_S≤30V	**0.5**		**3.0**	**0.5**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.7**	**+0.39**		**+0.7**	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	T_J=T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Note 1: Unless otherwise noted, these specifications apply: −55°C≤T_J≤+150°C for the LM35 and LM35A; −40°≤T_J≤+110°C for the LM35C and LM35CA; and 0°≤T_J≤+100°C for the LM35D. V_S=+5Vdc and I_{LOAD}=50 µA, in the circuit of *Figure 2*. These specifications also apply from +2°C to T_{MAX} in the circuit of *Figure 1*. Specifications in **boldface** apply over the full rated temperature range.

Note 2: Thermal resistance of the TO-46 package is 400°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient. Thermal resistance of the small outline molded package is 220°C/W junction to ambient. Thermal resistance of the TO-220 package is 90°C/W junction to ambient. For additional thermal resistance information see table in the Applications section.

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in **boldface** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

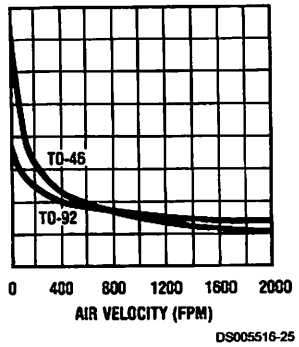
Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 12: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

;al Performance Characteristics

ıl Resistance
ın to Air



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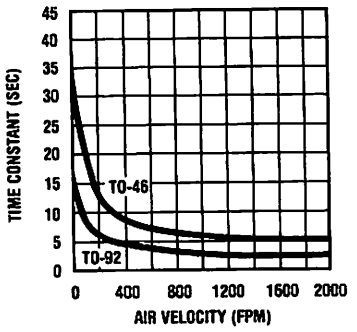
Thermal Time Constant



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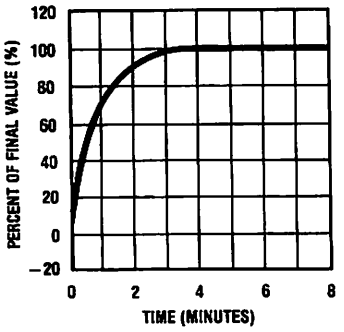
Thermal Response in Still Air



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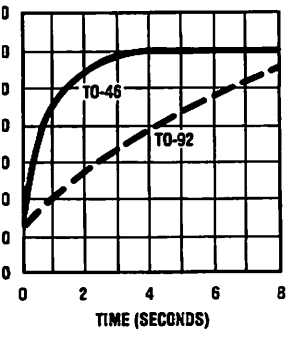
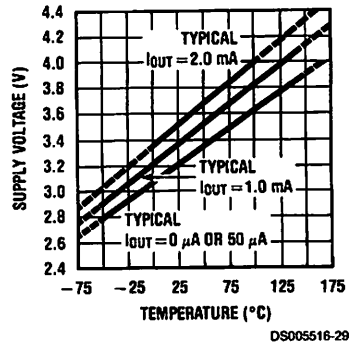
ıl Response in
Oil Bath



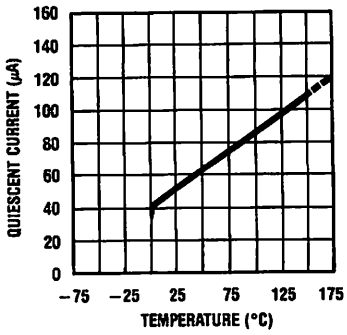
DS005516-28

Minimum Supply Voltage vs. Temperature



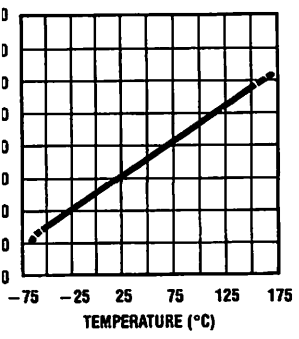
DS005516-29

Quiescent Current vs. Temperature (In Circuit of *Figure 1*.)



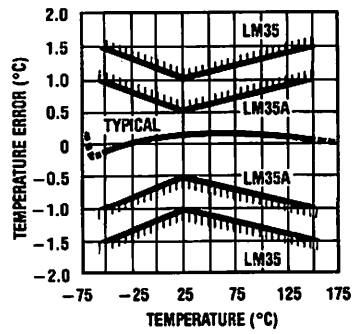
DS005516-30

ent Current
nperature
cuit of *Figure 2*.)



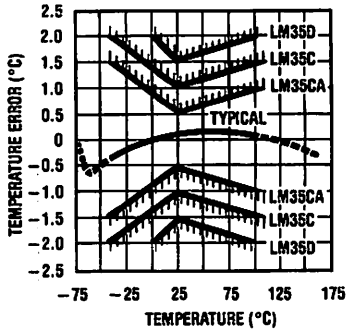
DS005516-31

Accuracy vs. Temperature (Guaranteed)



DS005516-32

Accuracy vs. Temperature (Guaranteed)



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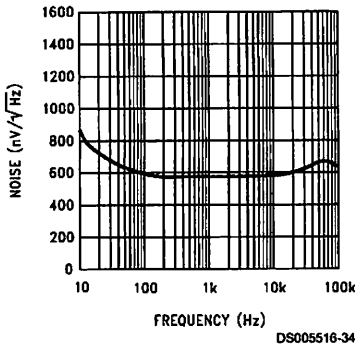
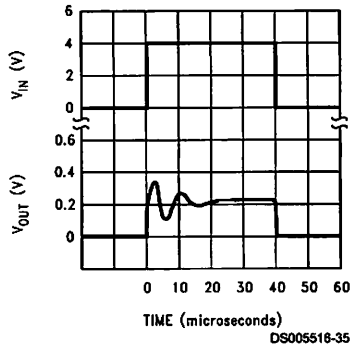
Typical Performance Characteristics (Continued)

Noise Voltage



Start-Up Response



Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01°C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM35 die would be at an intermediate temperature between the surface temperature and the air temperature. This is expecially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM35, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM35 die's temperature will not be affected by the air temperature.

The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course, in that case the V− terminal of the circuit will be grounded to that metal. Alternatively, the LM35 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM35 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM35 or its connections.

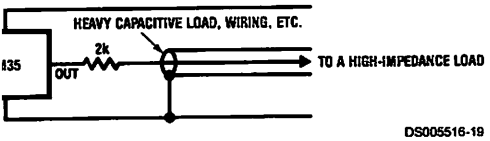
These devices are sometimes soldered to a small light-weight heat fin, to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor, to give the steadiest reading despite small deviations in the air temperature.

Temperature Rise of LM35 Due To Self-heating (Thermal Resistance, θ_{JA})

	TO-46, no heat sink	TO-46*, small heat fin	TO-92, no heat sink	TO-92**, small heat fin	SO-8 no heat sink	SO-8** small heat fin	TO-220 no heat sink
Still air	400°C/W	100°C/W	180°C/W	140°C/W	220°C/W	110°C/W	90°C/W
Moving air	100°C/W	40°C/W	90°C/W	70°C/W	105°C/W	90°C/W	26°C/W
Still oil	100°C/W	40°C/W	90°C/W	70°C/W			
Stirred oil	50°C/W	30°C/W	45°C/W	40°C/W			
(Clamped to metal, Infinite heat sink)	(24°C/W)				(55°C/W)		

*Wakefield type 201, or 1" disc of 0.020" sheet brass, soldered to case, or similar.
**TO-92 and SO-8 packages glued and leads soldered to 1" square of 1/16" printed circuit board with 2 oz. foil or similar.

cal Applications



E 3. LM35 with Decoupling from Capacitive Load

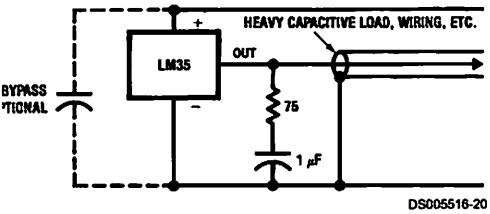
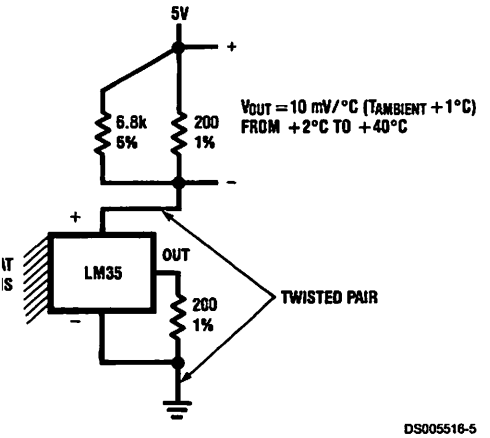


FIGURE 4. LM35 with R-C Damper

ITIVE LOADS

ıst micropower circuits, the LM35 has a limited ability heavy capacitive loads. The LM35 by itself is able to) pf without special precautions. If heavier loads are ited, it is easy to isolate or decouple the load with a ; see *Figure 3.* Or you can improve the tolerance of ance with a series R-C damper from output to see *Figure 4.*

he LM35 is applied with a 200Ω load resistor as n *Figure 5*, *Figure 6* or *Figure 8* it is relatively immune g capacitance because the capacitance forms a by- om ground to input, not on the output. However, as y linear circuit connected to wires in a hostile envi- t, its performance can be affected adversely by in- lectromagnetic sources such as relays, radio trans- motors with arcing brushes, SCR transients, etc, as ıg can act as a receiving antenna and its internal ıs can act as rectifiers. For best results in such cases, ss capacitor from V_{IN} to ground and a series R-C such as 75Ω in series with 0.2 or 1 µF from output to are often useful. These are shown in *Figure 13*, *14*, and *Figure 16.*



URE 5. Two-Wire Remote Temperature Sensor (Grounded Sensor)

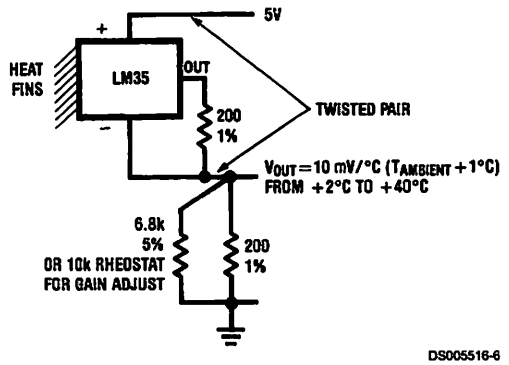


FIGURE 6. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

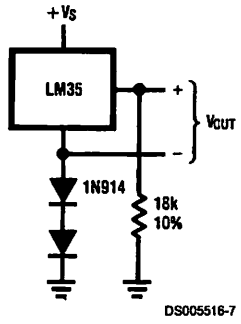


FIGURE 7. Temperature Sensor, Single Supply, −55° to +150°C

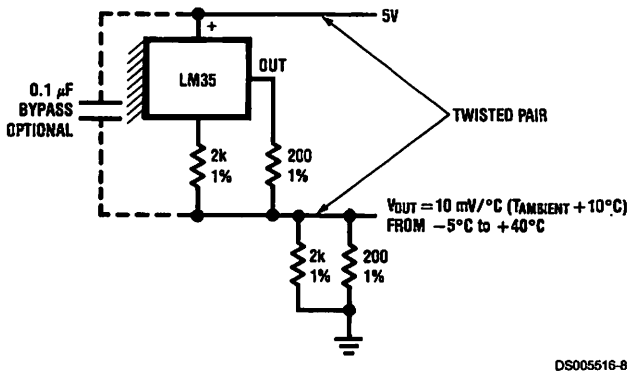


FIGURE 8. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

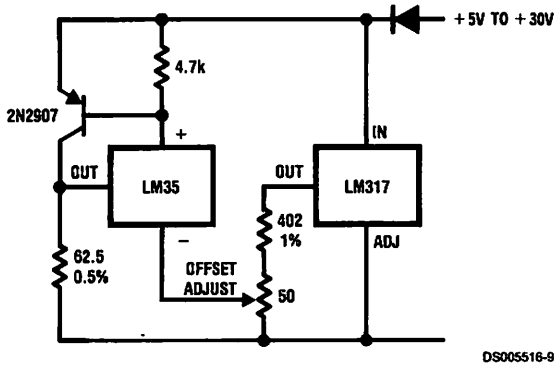


FIGURE 9. 4-To-20 mA Current Source (0°C to +100°C)

Typical Applications (Continued)

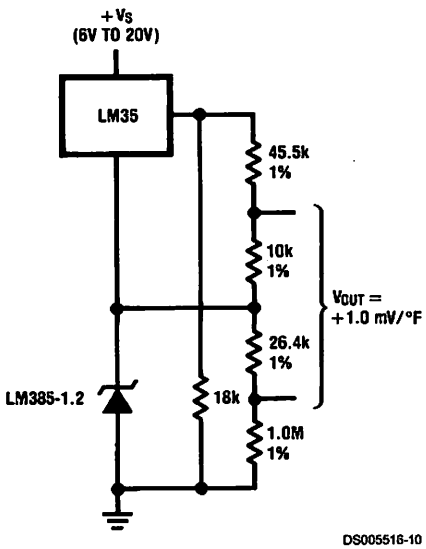


FIGURE 10. Fahrenheit Thermometer

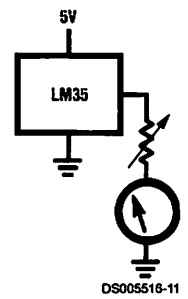


FIGURE 11. Centigrade Thermometer (Analog Meter)

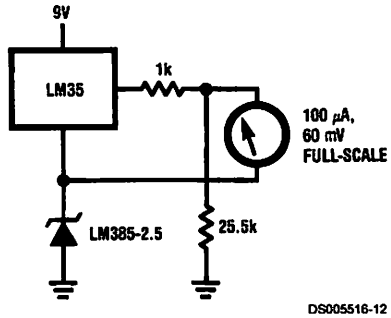


FIGURE 12. Fahrenheit ThermometerExpanded Scale Thermometer
(50° to 80° Fahrenheit, for Example Shown)

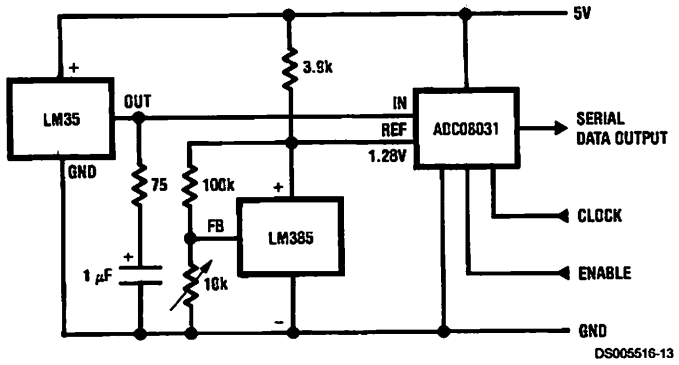


FIGURE 13. Temperature To Digital Converter (Serial Output) (+128°C Full Scale)

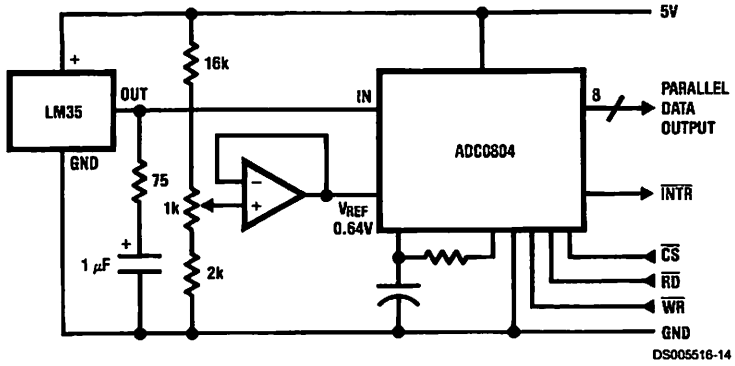
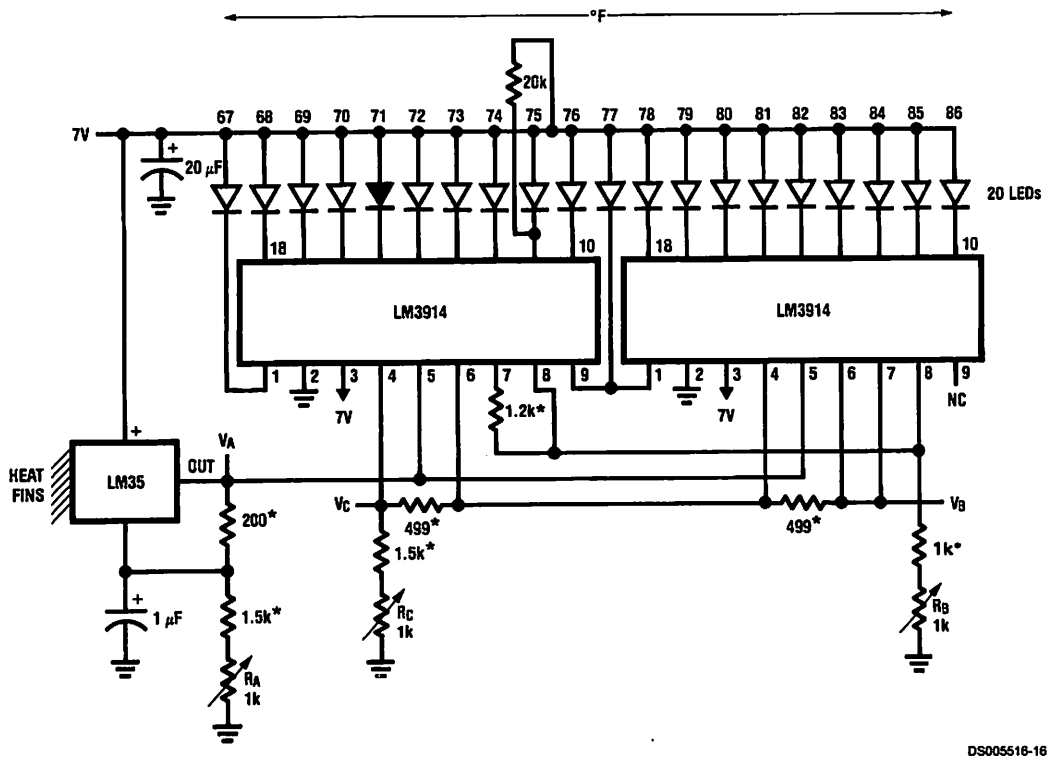


FIGURE 14. Temperature To Digital Converter (Parallel TRI-STATE™ Outputs for Standard Data Bus to µP Interface) (128°C Full Scale)

cal Applications (Continued)



2% film resistor
or V_B=3.075V
or V_C=1.955V
or V_A=0.075V + 100mV/°C x $T_{ambient}$
V_A=2.275V at 22°C

FIGURE 15. Bar-Graph Temperature Display (Dot Mode)

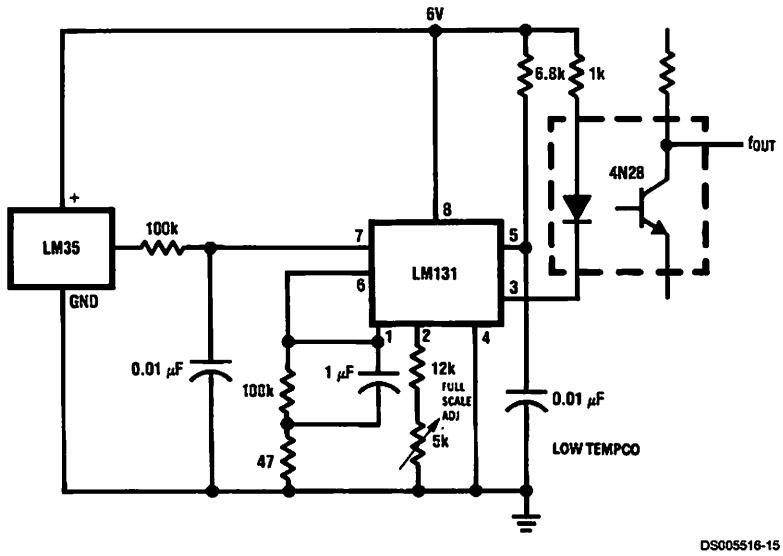
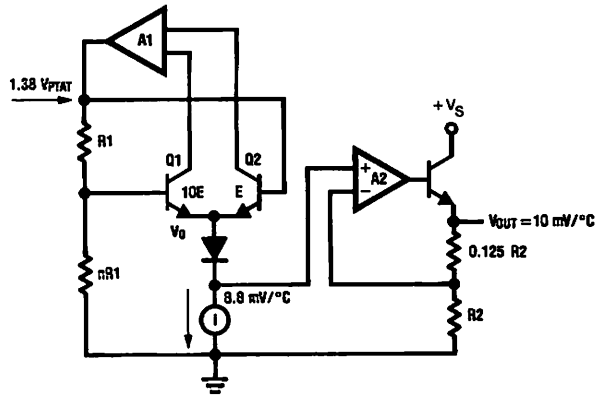


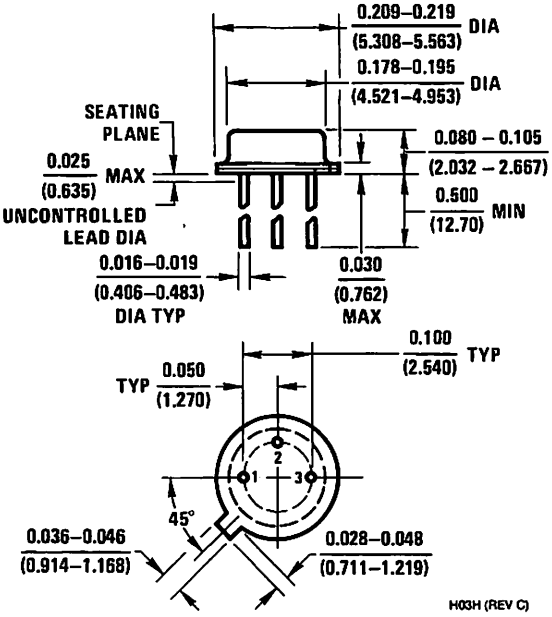
FIGURE 16. LM35 With Voltage-To-Frequency Converter And Isolated Output (2°C to +150°C; 20 Hz to 1500 Hz)

Block Diagram

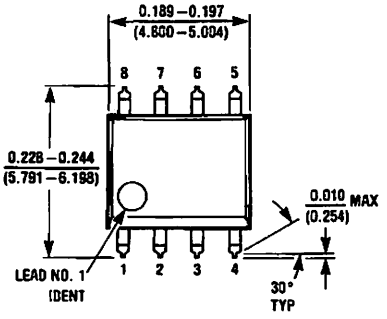


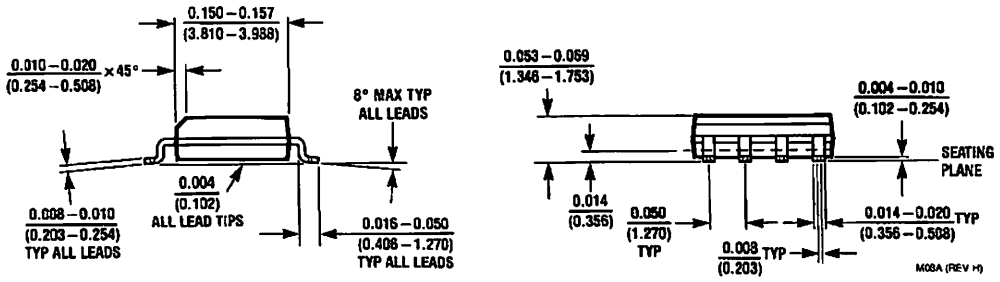
DS005516-23

sical Dimensions inches (millimeters) unless otherwise noted



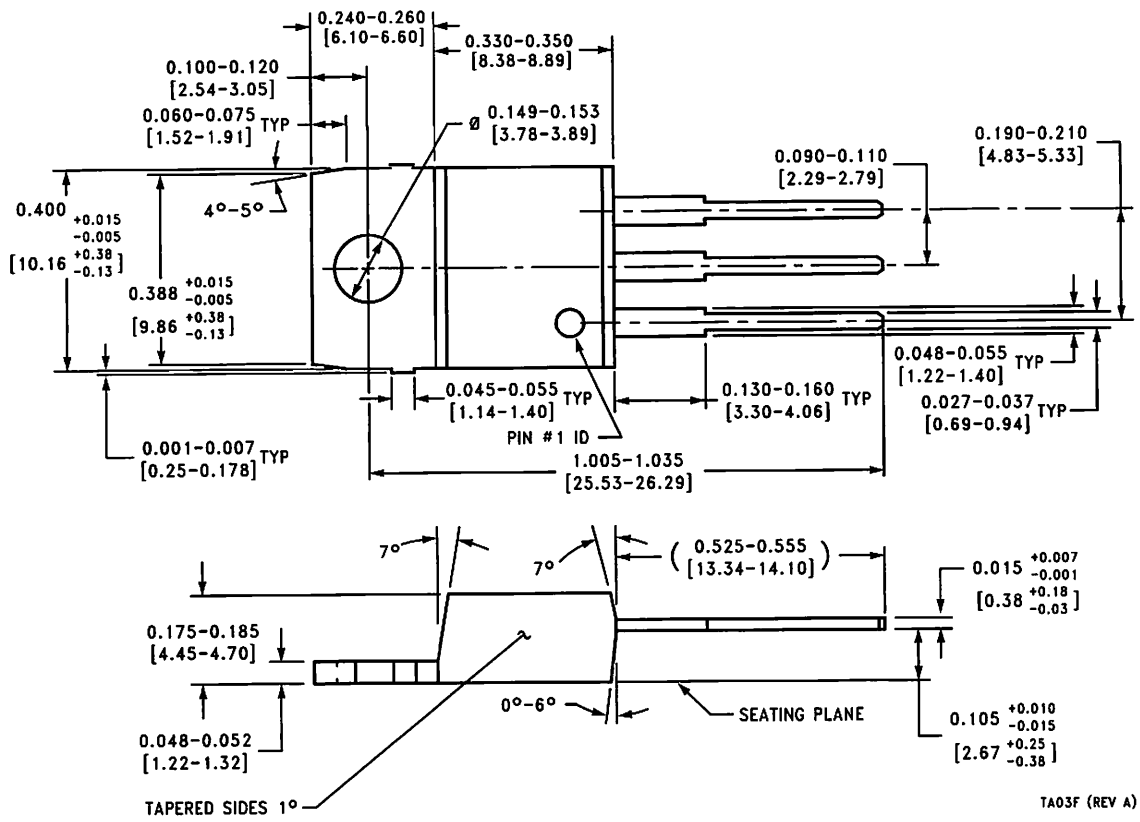
TO-46 Metal Can Package (H)
Order Number LM35H, LM35AH, LM35CH, LM35CAH, or LM35DH
NS Package Number H03H





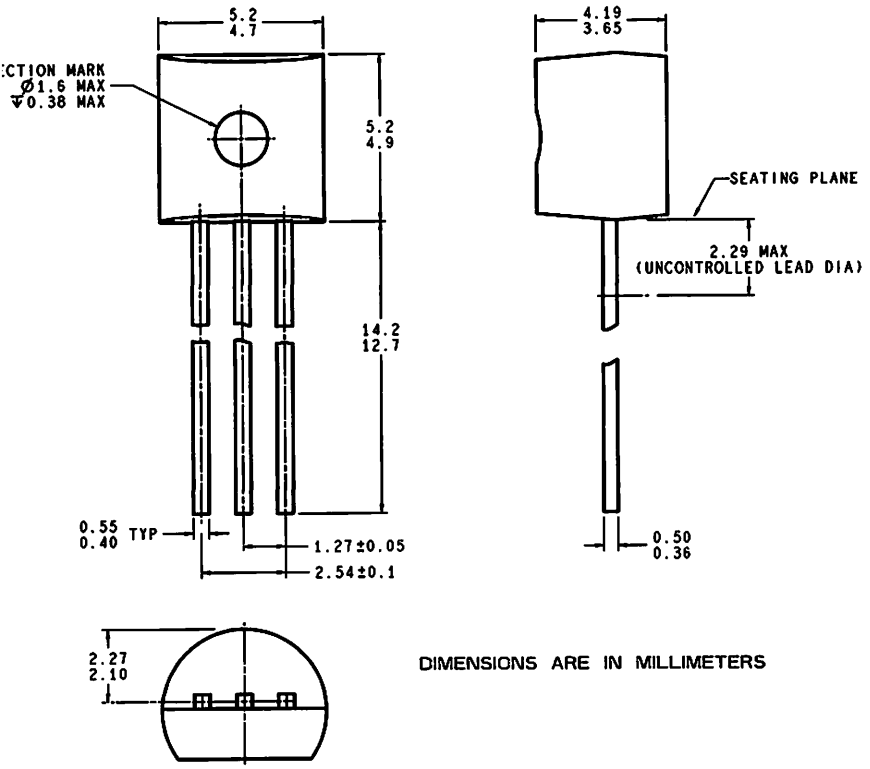
SO-8 Molded Small Outline Package (M)
Order Number LM35DM
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Power Package TO-220 (T)
Order Number LM35DT
NS Package Number TA03F

;ical Dimensions inches (millimeters) unless otherwise noted (Continued)



Z03A (Rev G)

TO-92 Plastic Package (Z)
Order Number LM35CZ, LM35CAZ or LM35DZ
NS Package Number Z03A

;UPPORT POLICY

NAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT ES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL SEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

support devices or systems are devices or tems which, (a) are intended for surgical implant the body, or (b) support or sustain life, and se failure to perform when properly used in ordance with instructions for use provided in the eling, can be reasonably expected to result in a ificant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

December 1994

C0801/ADC0802/ADC0803/ADC0804/ADC0805
ìit μP Compatible A/D Converters

ıeral Description

ADC0801, ADC0802, ADC0803, ADC0804 and 305 are CMOS 8-bit successive approximation A/D rters that use a differential potentiometric ladder— to the 256R products. These converters are de- l to allow operation with the NSC800 and INS8080A tive control bus with TRI-STATE® output latches di- driving the data bus. These A/Ds appear like memory ıns or I/O ports to the microprocessor and no inter- logic is needed.

ıntial analog voltage inputs allow increasing the com- ıode rejection and offsetting the analog zero input e value. In addition, the voltage reference input can usted to allow encoding any smaller analog voltage o the full 8 bits of resolution.

tures

ıpatible with 8080 μP derivatives—no interfacing c needed - access time - 135 ns

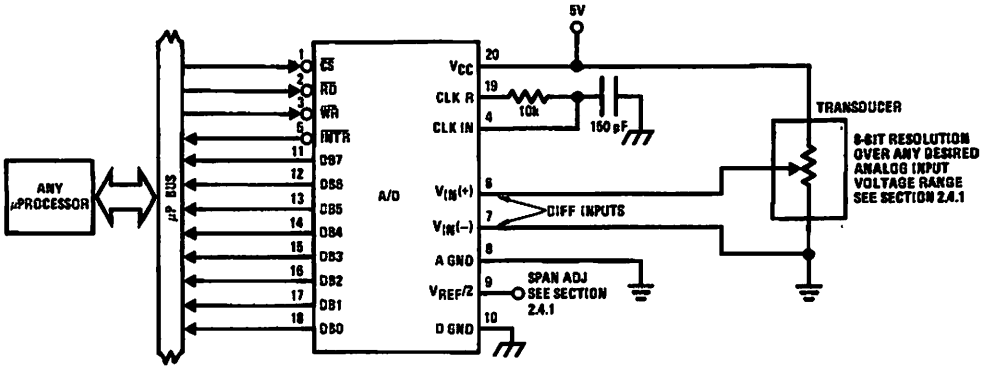
y interface to all microprocessors, or operates ınd alone"

- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution — 8 bits
- Total error — ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time — 100 μs

ical Applications



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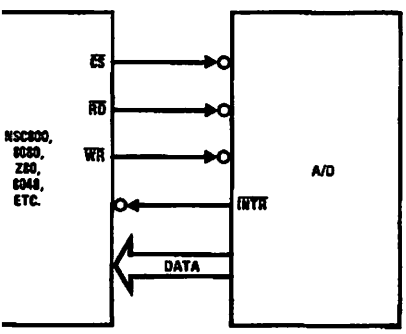
8080 Interface



TL/H/5671–31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

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bsolute Maximum Ratings (Notes 1 & 2)

Military/Aerospace specified devices are required, ıase contact the National Semiconductor Sales ffice/Distributors for availability and specifications.

ɔply Voltage (V_{CC}) (Note 3)	6.5V
ltage	
.ogic Control Inputs	−0.3V to +18V
٨t Other Input and Outputs	−0.3V to (V_{CC} + 0.3V)
ad Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ, ADC0802LJ/883	$-55°C \le T_A \le +125°C$
ADC0801/02/03/04LCJ	$-40°C \le T_A \le +85°C$
ADC0801/02/03/05LCN	$-40°C \le T_A \le +85°C$
ADC0804LCN	$0°C \le T_A \le +70°C$
ADC0802/03/04LCV	$0°C \le T_A \le +70°C$
ADC0802/03/04LCWM	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

ectrical Characteristics

ɔ following specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
C0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
C0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±½	LSB
C0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
C0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±1	LSB
C0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			±1	LSB
ɛF/2 Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
ılog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC} + 0.05	V_{DC}
Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
ver Supply Sensitivity	V_{CC} = 5 V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±⅛	LSB

C Electrical Characteristics

ɔ following specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

nbol	Parameter	Conditions	Min	Typ	Max	Units
	Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	μs
	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
K	Clock Frequency Clock Duty Cycle	V_{CC} = 5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz	8770		9708	conv/s
$\overline{WR})_L$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
C	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		135	200	ns
, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
I	Input Capacitance of Logic Control Inputs			5	7.5	pF
UT	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
NTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
I (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}

C Electrical Characteristics (Continued)

e following specifications apply for V_{CC} = 5V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

mbol	Parameter	Conditions	Min	Typ	Max	Units
NTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
(0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 4.75 V_{DC}			0.8	V_{DC}
(1)	Logical "1" Input Current (All Inputs)	V_{IN} = 5 V_{DC}		0.005	1	μA_{DC}
(0)	Logical "0" Input Current (All Inputs)	V_{IN} = 0 V_{DC}	−1	−0.005		μA_{DC}
OCK IN AND CLOCK R						
+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
−	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
UT (0)	Logical "0" CLK R Output Voltage	I_O = 360 μA V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
UT (1)	Logical "1" CLK R Output Voltage	I_O = −360 μA V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
TA OUTPUTS AND $\overline{INTR}$						
UT (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT} = 1.6 mA, V_{CC} = 4.75 V_{DC} I_{OUT} = 1.0 mA, V_{CC} = 4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
UT (1)	Logical "1" Output Voltage	I_O = −360 μA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
UT (1)	Logical "1" Output Voltage	I_O = −10 μA, V_{CC} = 4.75 V_{DC}	4.5			V_{DC}
T	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT} = 0 V_{DC} V_{OUT} = 5 V_{DC}	−3		 3	μA_{DC} μA_{DC}
URCE		V_{OUT} Short to Gnd, T_A = 25°C	4.5	6		mA_{DC}
IK		V_{OUT} Short to V_{CC}, T_A = 25°C	9.0	16		mA_{DC}
WER SUPPLY						
	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	f_{CLK} = 640 kHz, $V_{REF}/2$ = NC, T_A = 25°C and $\overline{CS}$ = 5V		 1.1 1.9	 1.8 2.5	 mA mA

e 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating device beyond its specified operating conditions.

e 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

e 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

e 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward duct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), igh level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. The s allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output e will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature ations, initial tolerance and loading.

e 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be nded so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

e 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The t request is internally latched, see *Figure 2* and section 2.0.

e 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

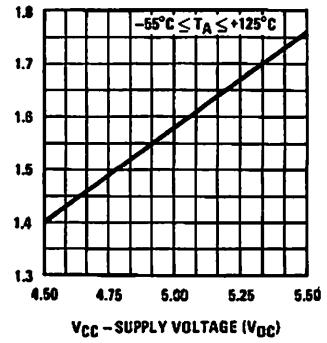
e 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

e 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and C0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

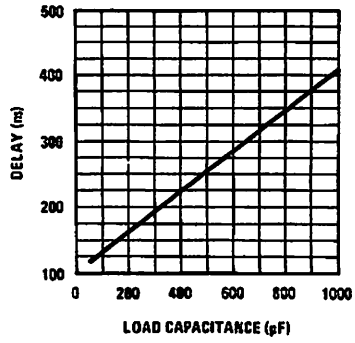
e 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

ypical Performance Characteristics

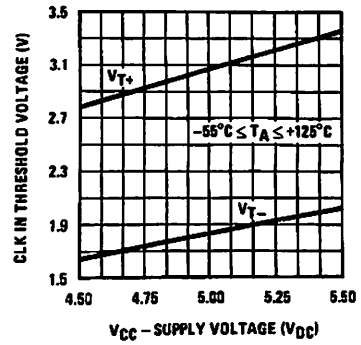
Logic Input Threshold Voltage vs. Supply Voltage



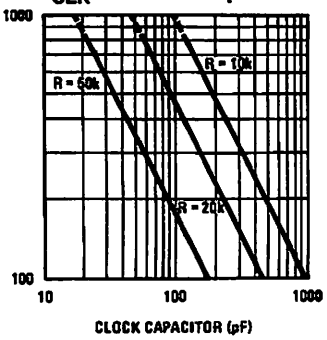
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



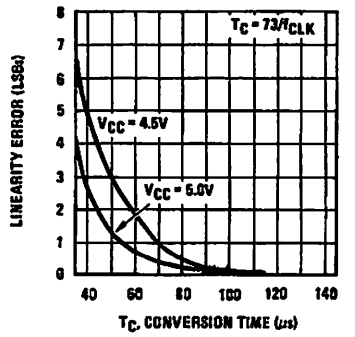
CLK IN Schmitt Trip Levels vs. Supply Voltage



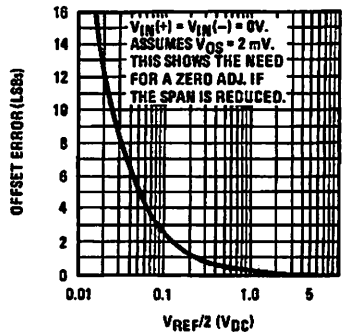
f_{CLK} vs. Clock Capacitor



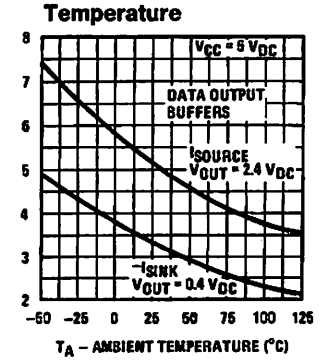
Full-Scale Error vs Conversion Time



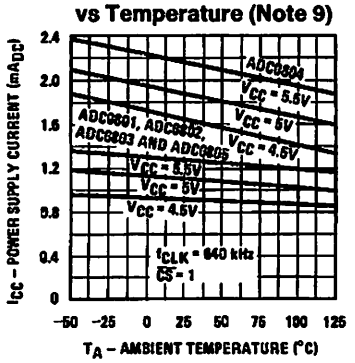
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



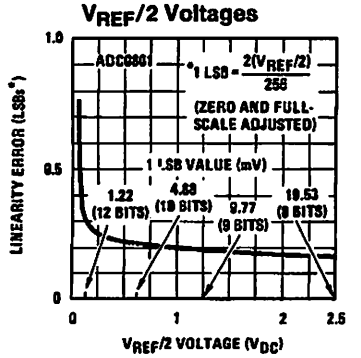
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)

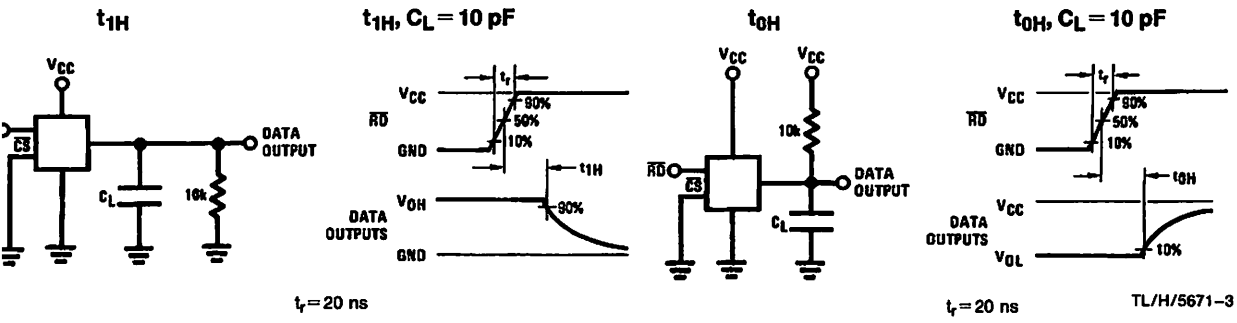


Linearity Error at Low $V_{REF}/2$ Voltages

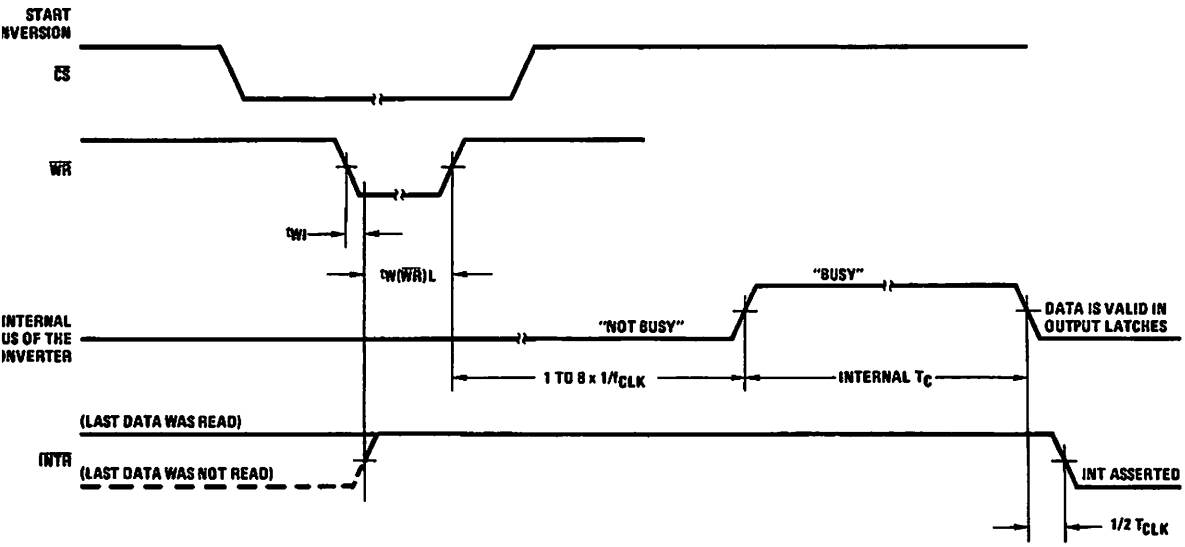


TL/H/5671–2

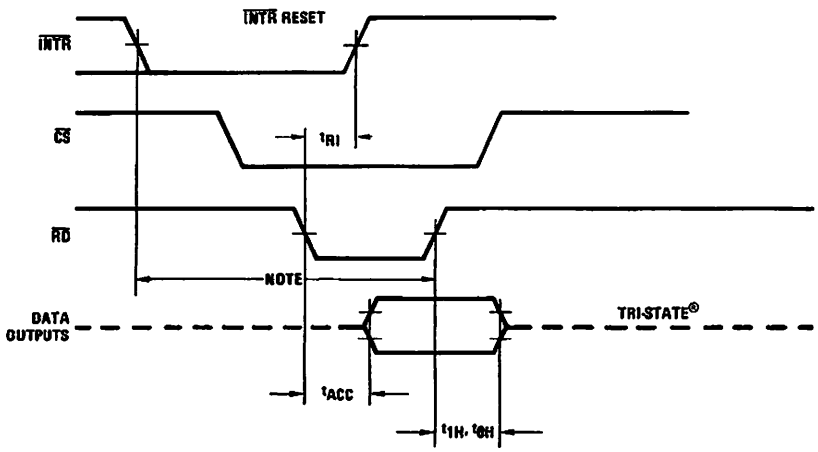
RI-STATE Test Circuits and Waveforms



ming Diagrams (All timing is measured from the 50% voltage points)



Output Enable and Reset INTR

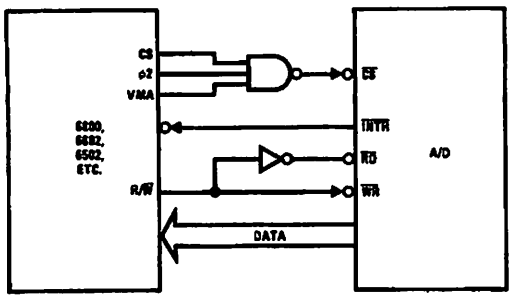


Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

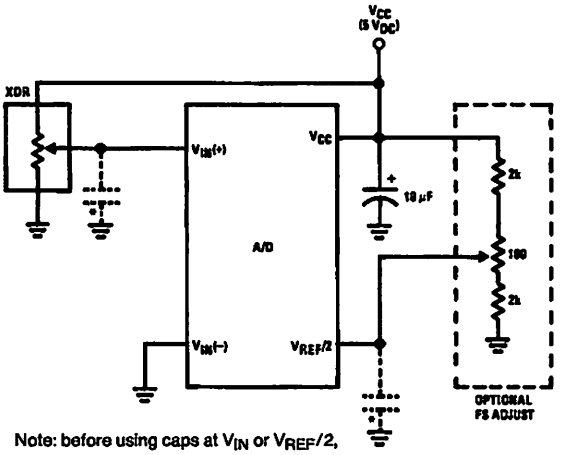
TL/H/5671–4

ypical Applications (Continued)

6800 Interface

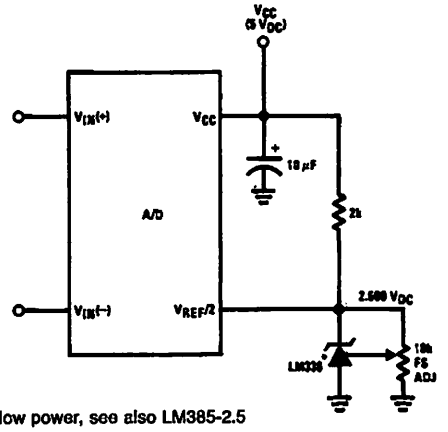


Ratiometric with Full-Scale Adjust



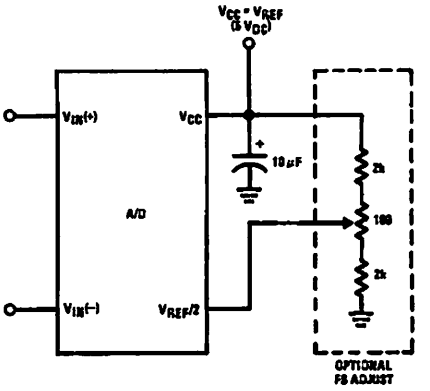
Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

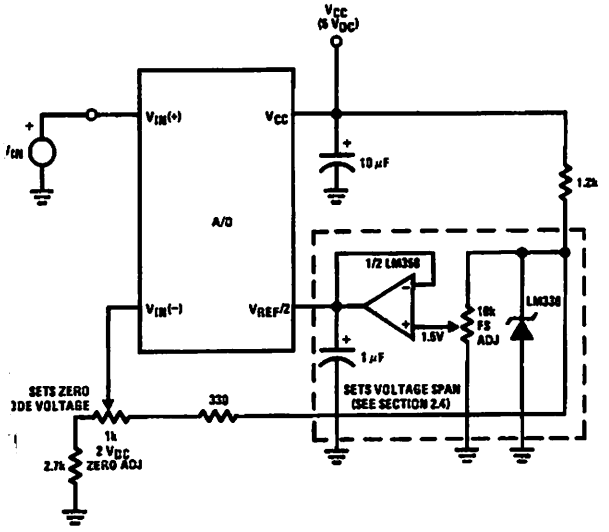


*For low power, see also LM385-2.5

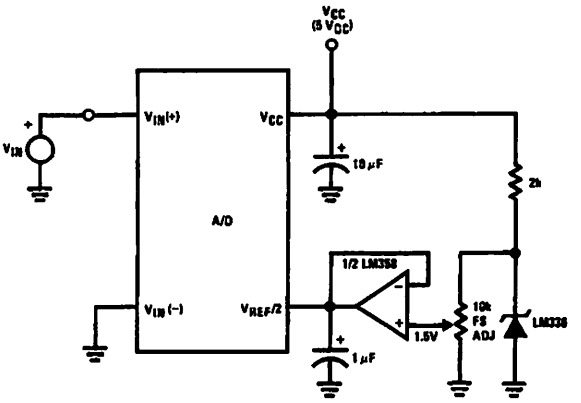
Absolute with a 5V Reference



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



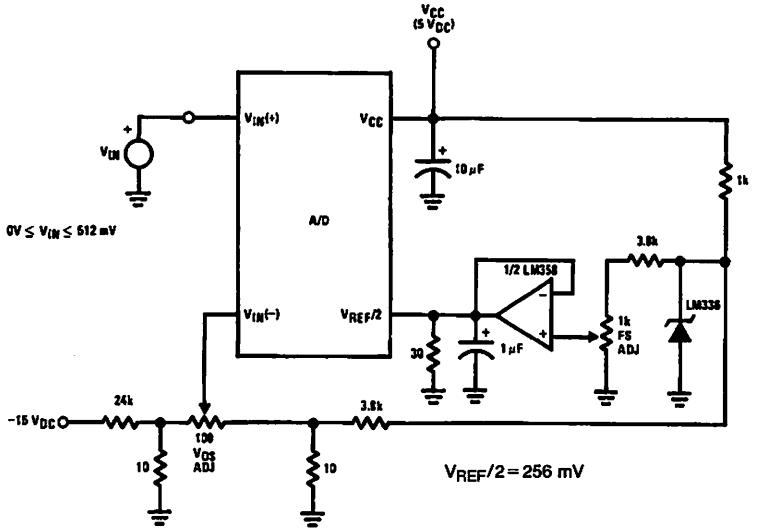
Span Adjust: $0V \leq V_{IN} \leq 3V$



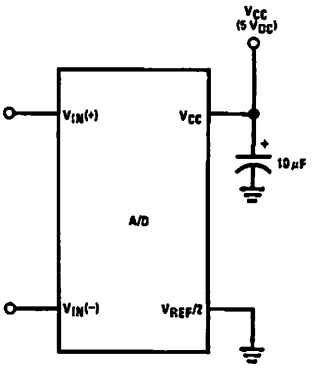
TL/H/5671–5

ypical Applications (Continued)

Directly Converting a Low-Level Signal



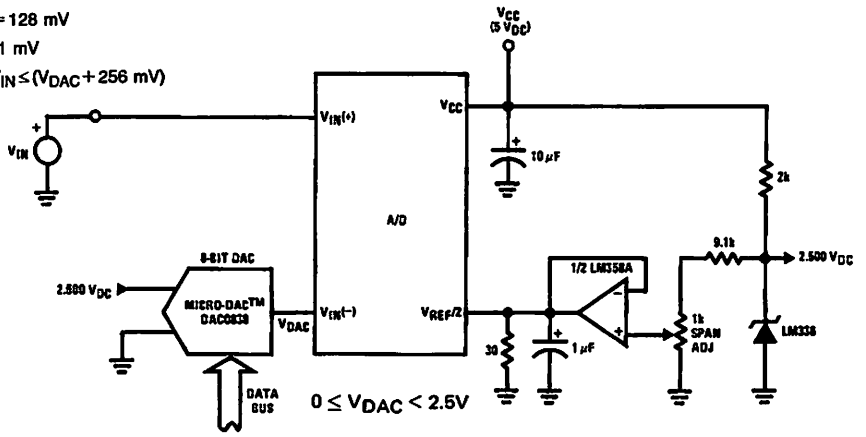
A µP Interfaced Comparator



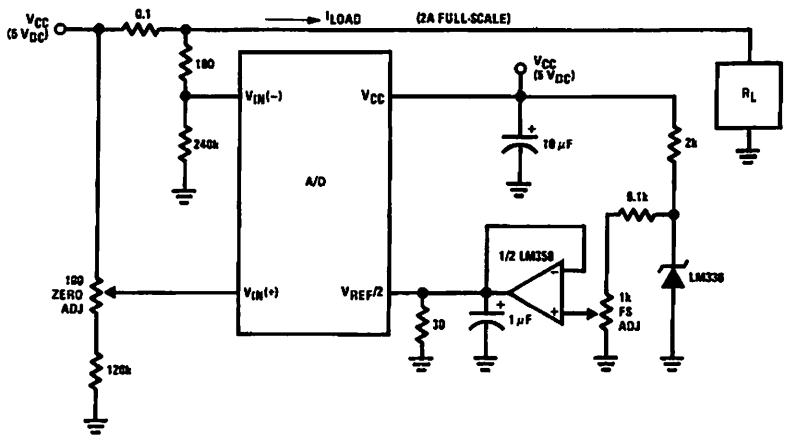
For: $V_{IN}(+) > V_{IN}(-)$
Output = FF_{HEX}
For: $V_{IN}(+) < V_{IN}(-)$
Output = 00_{HEX}

1 mV Resolution with µP Controlled Range

$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC} + 256$ mV)



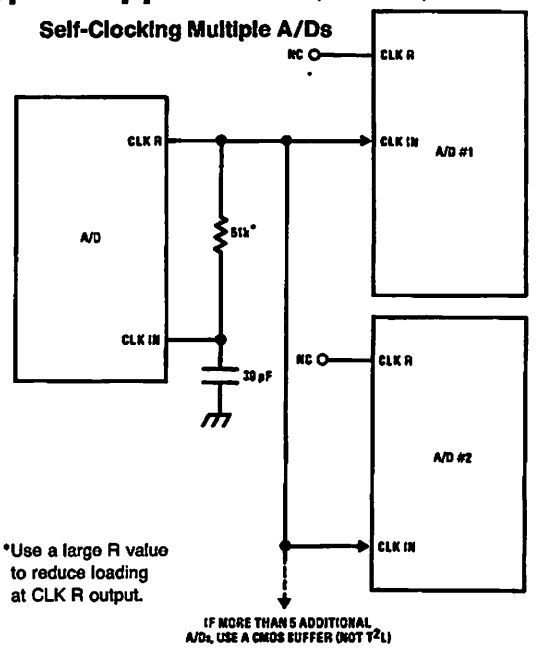
Digitizing a Current Flow



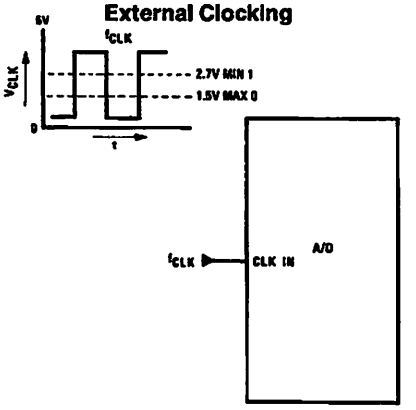
TL/H/5871–6

ypical Applications (Continued)

Self-Clocking Multiple A/Ds

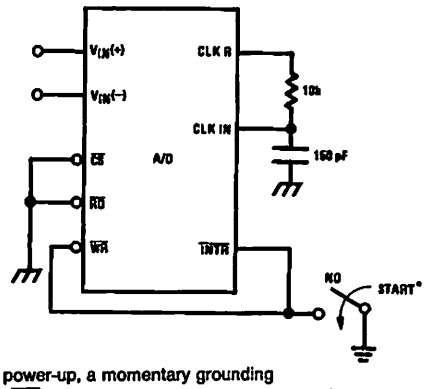


External Clocking



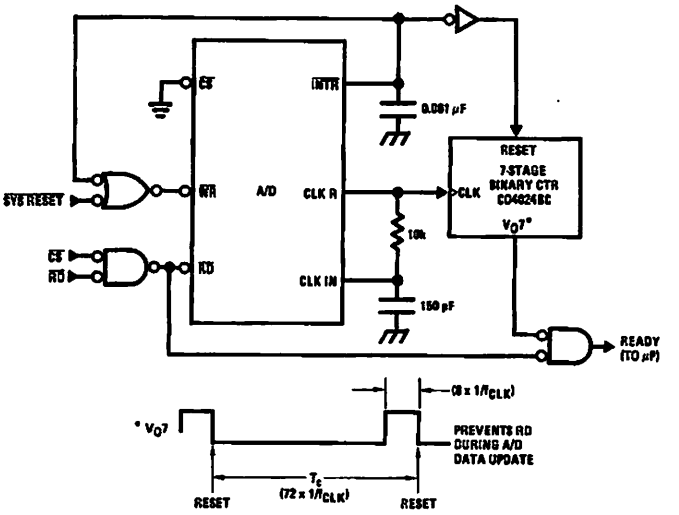
100 kHz ≤ f_{CLK} ≤ 1460 kHz

Self-Clocking in Free-Running Mode

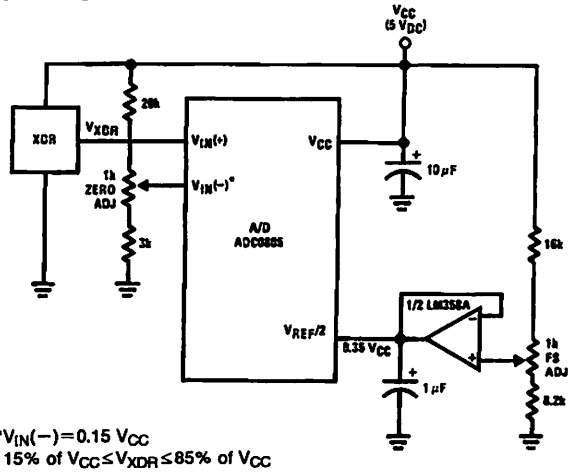


ter power-up, a momentary grounding
the $\overline{WR}$ input is needed to guarantee operation.

µP Interface for Free-Running A/D

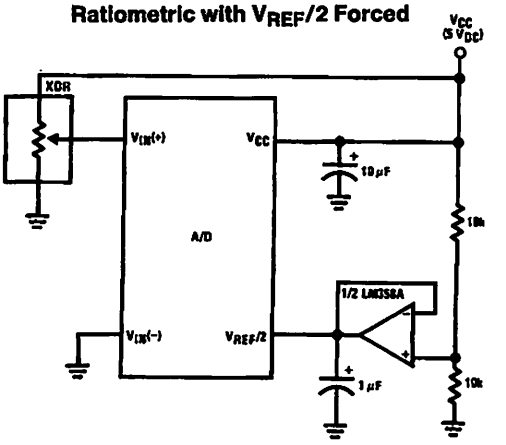


Operating with "Automotive" Ratiometric Transducers



*$V_{IN}(-)$ = 0.15 V_{CC}
15% of V_{CC} ≤ V_{XDR} ≤ 85% of V_{CC}

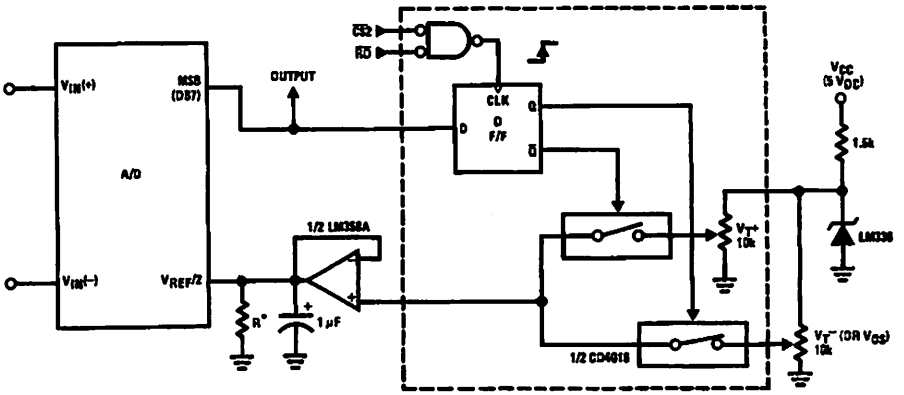
Ratiometric with $V_{REF}/2$ Forced



TL/H/5671–7

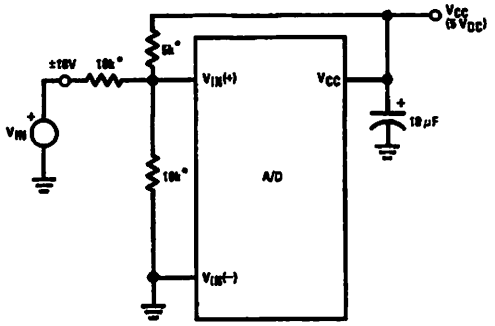
ypical Applications (Continued)

μP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)



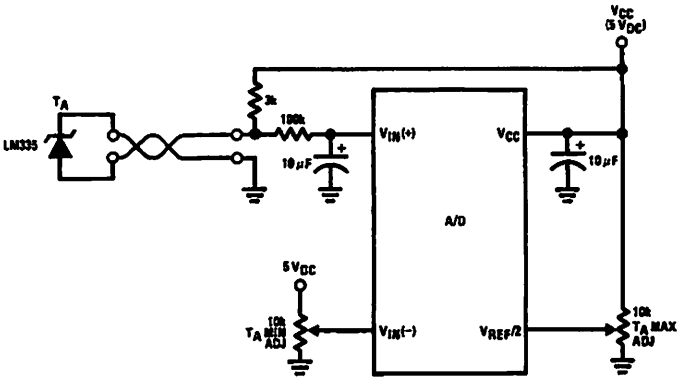
*See *Figure 5* to select R value
DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

Handling ±10V Analog Inputs

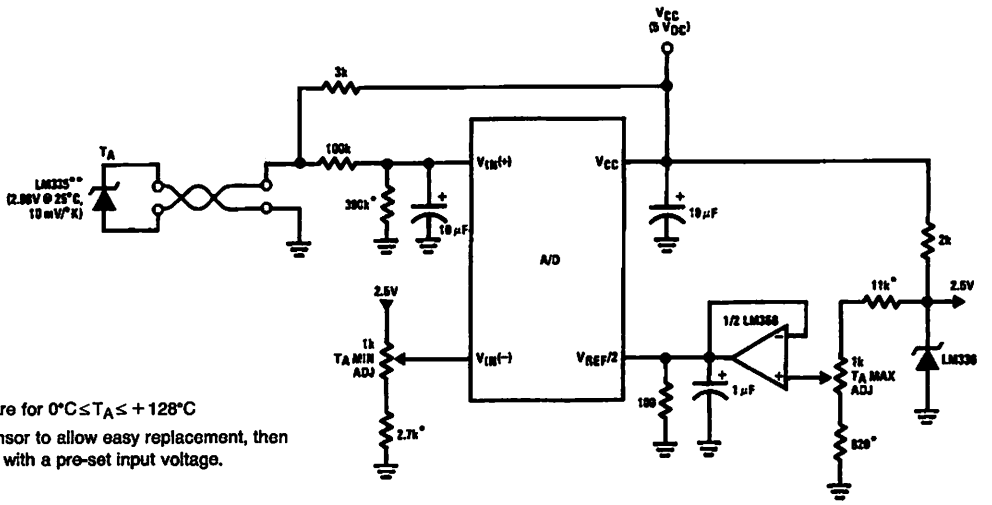


eckman Instruments #694-3-R10K resistor array

Low-Cost, μP Interfaced, Temperature-to-Digital Converter



μP Interfaced Temperature-to-Digital Converter

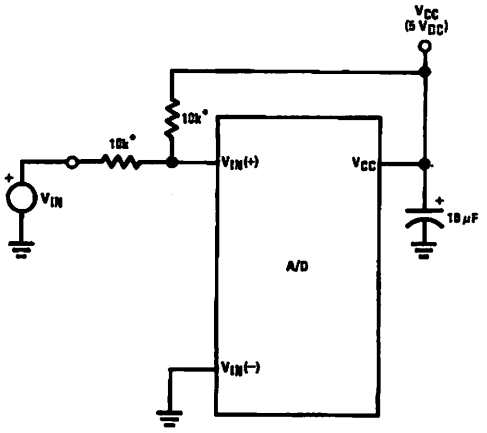


uit values shown are for $0°C \leq T_A \leq +128°C$
1 calibrate each sensor to allow easy replacement, then
) can be calibrated with a pre-set input voltage.

TL/H/5671–8

ypical Applications (Continued)

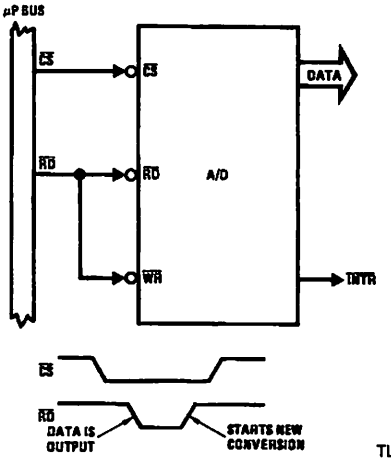
Handling ±5V Analog Inputs



TL/H/5671–33

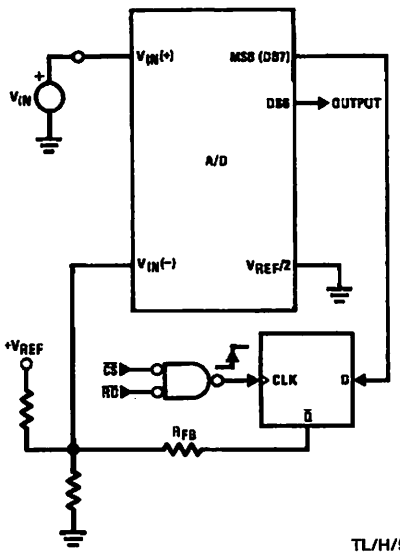
*Beckman Instruments #694-3-R10K resistor array

Read-Only Interface



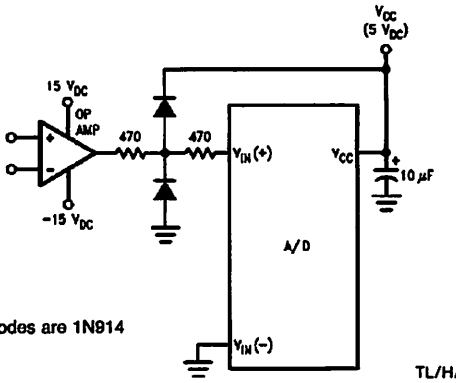
TL/H/5671–34

µP Interfaced Comparator with Hysteresis



TL/H/5671–35

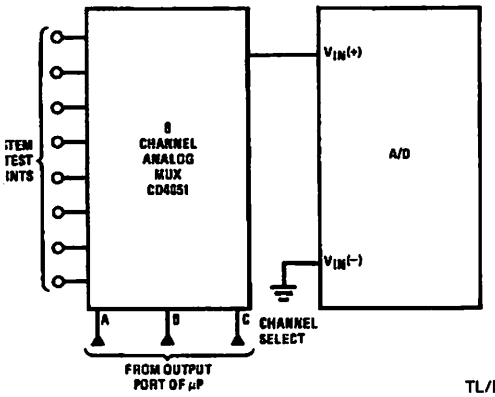
Protecting the Input



Diodes are 1N914

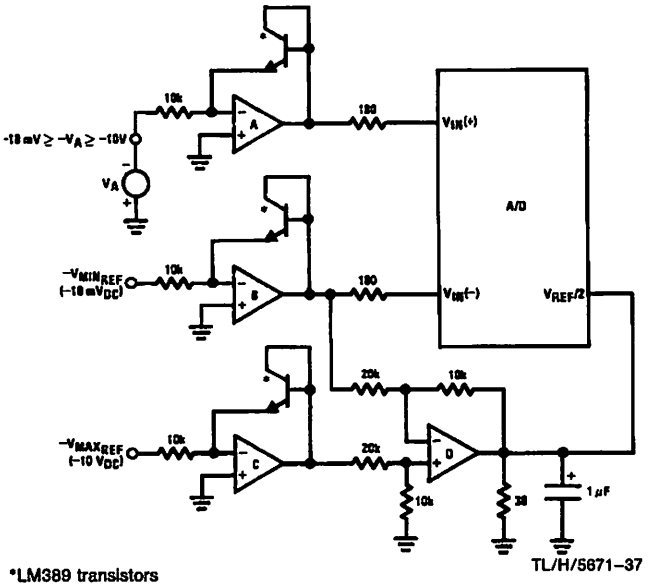
TL/H/5671–9

Analog Self-Test for a System



TL/H/5671–36

A Low-Cost, 3-Decade Logarithmic Converter



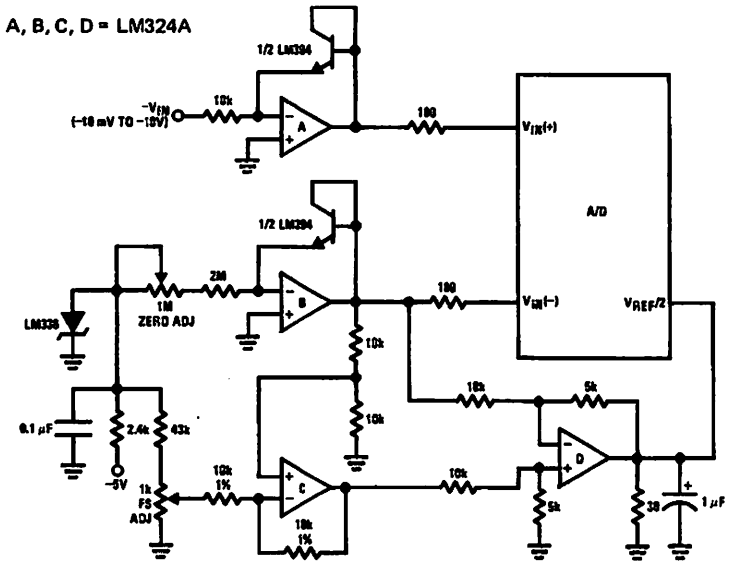
TL/H/5671–37

*LM389 transistors

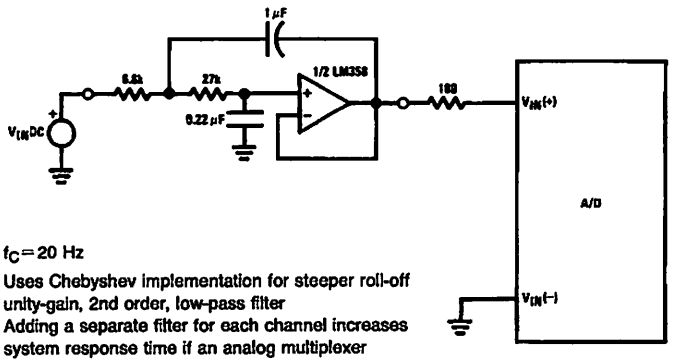
A, B, C, D = LM324A quad op amp

ypical Applications (Continued)

3-Decade Logarithmic A/D Converter



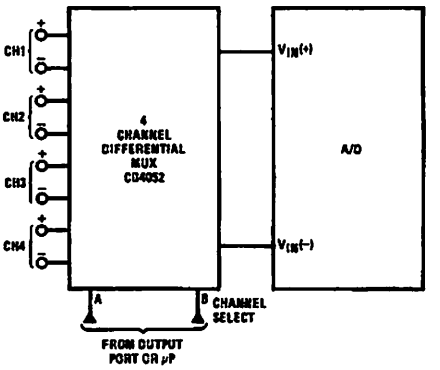
Noise Filtering the Analog Input



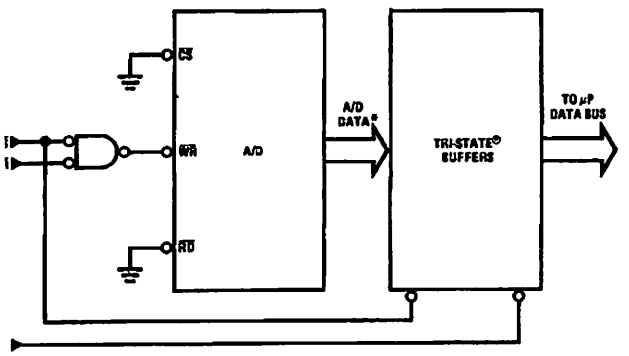
$f_C = 20$ Hz

Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

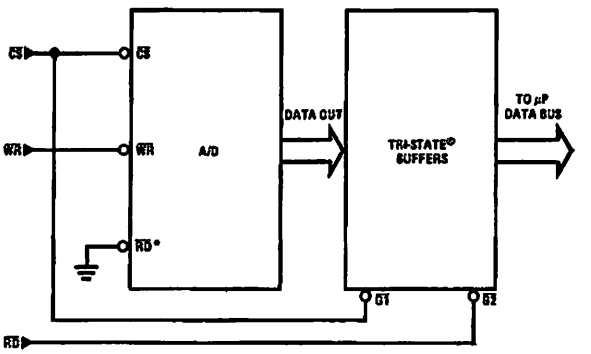


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

Increasing Bus Drive and/or Reducing Time on Bus

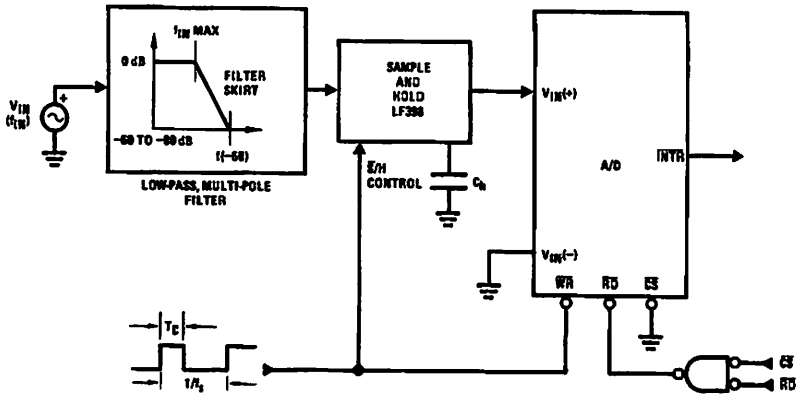


TL/H/5671–10

*Allows output data to set-up at falling edge of $\overline{CS}$

ypical Applications (Continued)

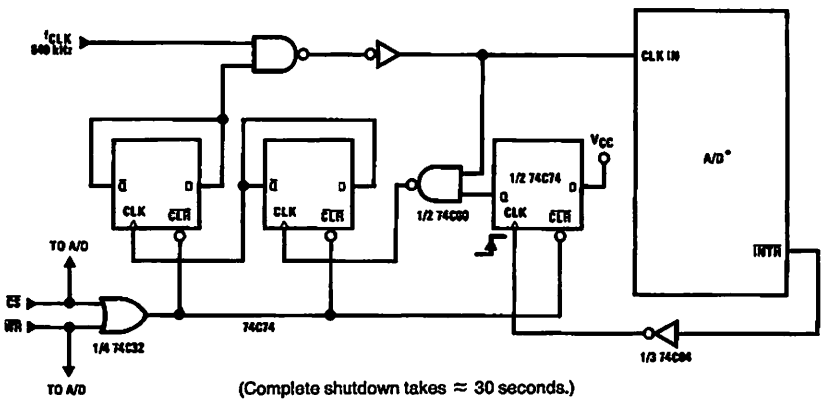
Sampling an AC Input Signal



Note 1: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

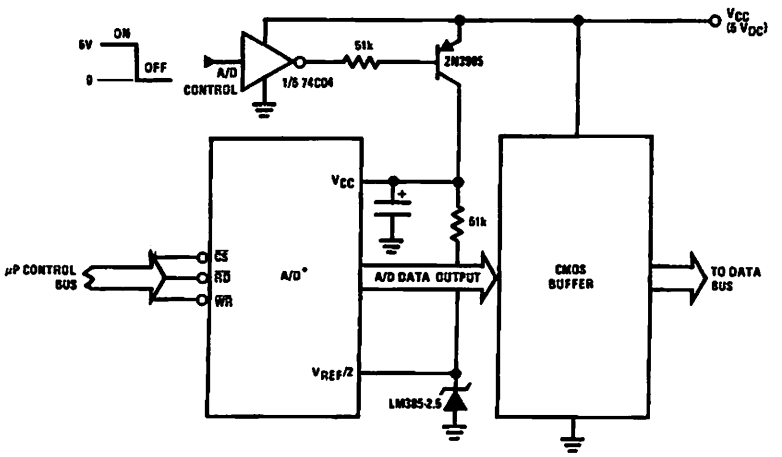
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



TL/H/5671–11

*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

unctional Description

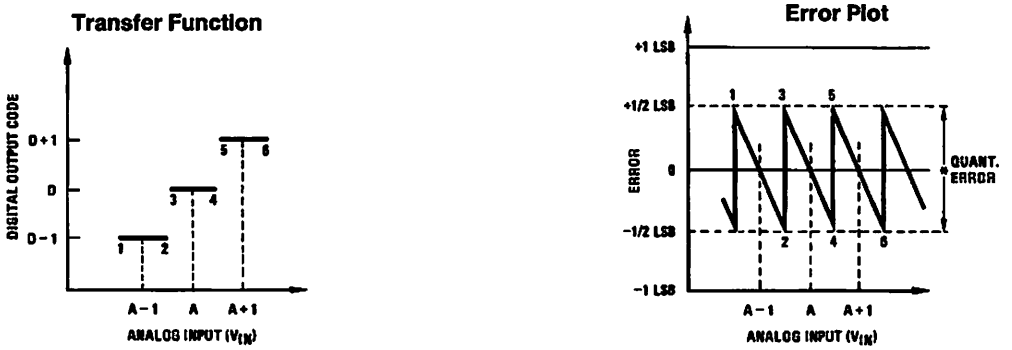
ɔ UNDERSTANDING A/D ERROR SPECS

perfect A/D transfer characteristic (staircase waveform) is ıown in *Figure 1a*. The horizontal scale is analog input ɪltage and the particular points labeled are in steps of 1 ɜB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital ıtput codes that correspond to these inputs are shown as −1, D, and D+1. For the perfect A/D, not only will center-ılue (A−1, A, A+1, ...) analog inputs produce the cor-ıct output ditigal codes, but also each riser (the transitions ətween adjacent output codes) will be located ±½ LSB ıay from each center-value. As shown, the risers are ideal ıd have no width. Correct digital output codes will be pro-ded for a range of analog input voltages that extend ±½ ɜB from the ideal center-values. Each tread (the range of ıalog input voltage that provides the same digital output ɔde) is therefore 1 LSB wide.

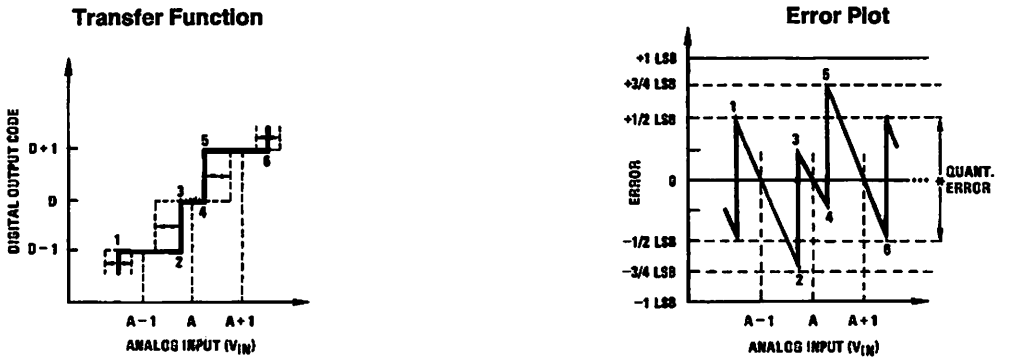
gure 1b shows a worst case error plot for the ADC0801. ll center-valued inputs are guaranteed to produce the cor-ıct output codes and the adjacent risers are guaranteed to ə no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

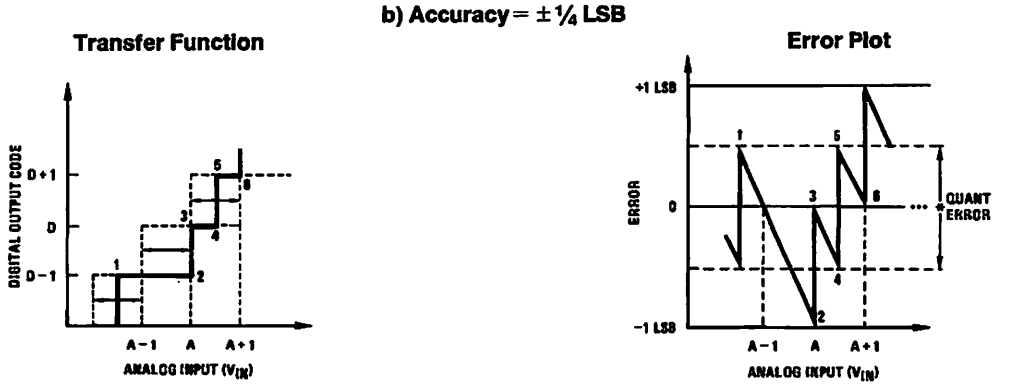
Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.



a) Accuracy = ±0 LSB: A Perfect A/D



b) Accuracy = ±¼ LSB



c) Accuracy = ±½ LSB

TL/H/5671–12

FIGURE 1. Clarifying the Error Specs of an A/D Converter

unctional Description (Continued)

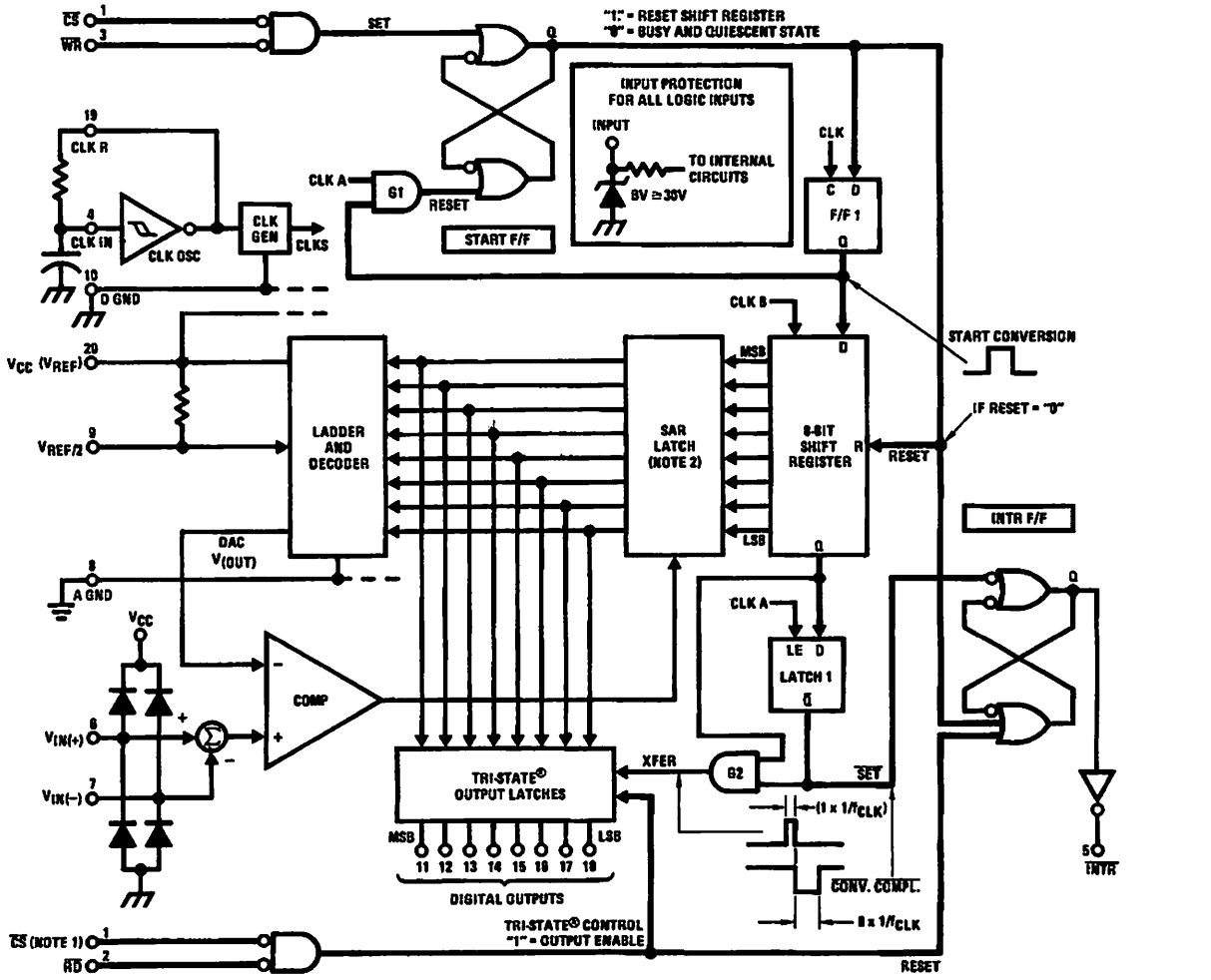
) FUNCTIONAL DESCRIPTION

ıe ADC0801 series contains a circuit equivalent of the ;6R network. Analog switches are sequenced by succes- ve approximation logic to match the analog difference in- ıt voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on e R network. The most significant bit is tested first and ter 8 comparisons (64 clock cycles) a digital 8-bit binary ıde (1111 1111 = full-scale) is transferred to an output tch and then an interrupt is asserted ($\overline{INTR}$ makes a high- -low transition). A conversion in process can be interrupt- l by issuing a second start command. The device may be ıerated in the free-running mode by connecting $\overline{INTR}$ to e $\overline{WR}$ input with $\overline{CS}=0$. To ensure start-up under all pos- ıle conditions, an external $\overline{WR}$ pulse is required during the st power-up cycle.

n the high-to-low transition of the $\overline{WR}$ input the internal AR latches and the shift register stages are reset. As long ; the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will re- ain in a reset state. *Conversion will start from 1 to 8 clock ıriods after at least one of these inputs makes a low-to- gh transition.*

A functional diagram of the A/D converter is shown in *Figure 2*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.



TL/H/5671–13

Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

unctional Description (Continued)

ter the "1" is clocked through the 8-bit shift register hich completes the SAR search) it appears as the input to e D-type latch, LATCH 1. As soon as this "1" is output)m the shift register, the AND gate, G2, causes the new gital word to transfer to the TRI-STATE output latches. hen LATCH 1 is subsequently enabled, the Q output akes a high-to-low transition which causes the INTR F/F set. An inverting buffer then supplies the $\overline{INTR}$ input sig-al.

ote that this $\overline{SET}$ control of the INTR F/F remains low for of the external clock periods (as the internal clocks run at of the frequency of the external clock). If the data output continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{TR}$ output will still signal the end of conversion (by a high-low transition), because the $\overline{SET}$ input can control the Q itput of the INTR F/F even though the RESET input is nstantly at a "1" level in this operating mode. This $\overline{INTR}$ itput will therefore stay low for the duration of the $\overline{SET}$ gnal, which is 8 periods of the external clock frequency ssuming the A/D is not started during this interval).

hen operating in the free-running or continuous conver-on mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see so section 2.8), the START F/F is SET by the high-to-low insition of the $\overline{INTR}$ signal. This resets the SHIFT REGIS-ER which causes the input to the D-type latch, LATCH 1, go low. As the latch enable input is still present, the $\overline{Q}$ itput will go high, which then allows the INTR F/F to be ESET. This reduces the width of the resulting $\overline{INTR}$ output lse to only a few propagation delays (approximately 300).

hen data is to be read, the combination of both $\overline{CS}$ and $\overline{D}$ being low will cause the INTR F/F to be reset and the RI-STATE output latches will be enabled to provide the 8-t digital outputs.

1 Digital Control Inputs

ne digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard L logic voltage levels. These signals have been renamed nen compared to the standard A/D Start and Output En-le labels. In addition, these inputs are active low to allow easy interface to microprocessor control busses. For n-microprocessor based applications, the $\overline{CS}$ input (pin 1) n be grounded and the standard A/D Start function is tained by an active low pulse applied at the $\overline{WR}$ input (pin and the Output Enable function is caused by an active v pulse at the $\overline{RD}$ input (pin 2).

2 Analog Differential Voltage Inputs and Common-Mode Rejection

is A/D has additional applications flexibility due to the alog differential voltage input. The $V_{IN}(-)$ input (pin 7) n be used to automatically subtract a fixed voltage value m the input reading (tare correction). This is also useful in nA–20 mA current loop conversion. In addition, common-de noise can be reduced by use of the differential input.

e time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)}$$

which gives

$V_P \cong 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

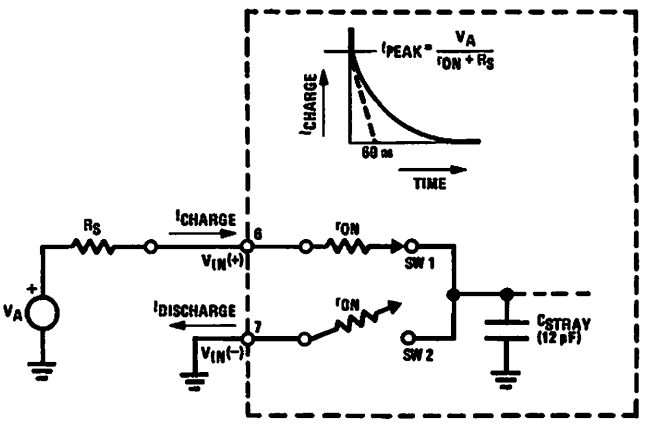
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



TL/H/5671–14

r_{ON} of SW 1 and SW 2 ≅ 5 kΩ

$r = r_{ON} C_{STRAY} \cong 5\ k\Omega \times 12\ pF = 60\ ns$

FIGURE 3. Analog Input Impedance

ınctional Description (Continued)

e voltage on this capacitance is switched and will result in rents entering the $V_{IN}(+)$ input pin and leaving the ı(−) input which will depend on the analog differential ut voltage levels. These current transients occur at the ding edge of the internal clocks. They rapidly decay and *not cause errors* as the on-chip comparator is strobed at end of the clock period.

ult Mode

he voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin ceeds the allowed operating range of $V_{CC}+50$ mV, large ut currents can flow through a parasitic diode to the V_{CC} . If these currents can exceed the 1 mA max allowed ec, an external diode (1N914) should be added to bypass s current to the V_{CC} pin (with the current bypassed with s diode, the voltage at the $V_{IN}(+)$ pin can exceed the c voltage by the forward voltage of this diode).

.2 Input Bypass Capacitors

pass capacitors at the inputs will average these charges d cause a DC current to flow through the output resistces of the analog signal sources. This charge pumping ion is worse for continuous conversions with the $V_{IN}(+)$ ut voltage at full-scale. For continuous conversions with 40 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog uts or the $V_{REF}/2$ pin* for high resistance sources (> 1). If input bypass capacitors are necessary for noise filter- and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop ross this input resistance, which is due to the average lue of the input current, can be eliminated with a full-scale justment while the given source resistor and input bypass pacitor are both in place. This is possible because the erage value of the input current is a precise linear function of the differential input voltage.

.3 Input Source Resistance

rge values of source resistance where an input bypass pacitor is not used, *will not cause errors* as the input curits settle out prior to the comparison time. If a low pass er is required in the system, use a low valued series resis- (≤ 1 kΩ) for a passive RC section or add an op amp RC tive low pass filter. For low source resistance applicans, (≤ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will event noise pickup due to series lead inductance of a long e. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback op—from the output of an op amp, if used.

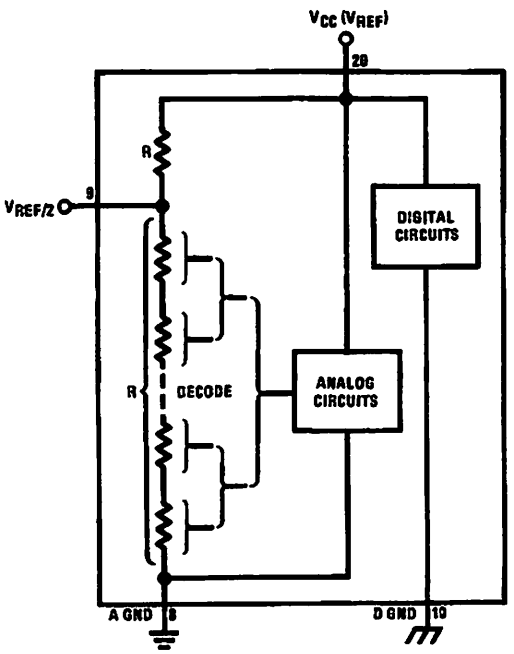
.4 Noise

ie leads to the analog inputs (pin 6 and 7) should be kept short as possible to minimize input noise coupling. Both ise and undesired digital clock coupling to these inputs n cause system errors. The source resistance for these uts should, in general, be kept below 5 kΩ. Larger values source resistance can cause undesired system noise kup. Input bypass capacitors, placed from the analog ints to ground, will eliminate system noise pickup but can ate analog scale errors as these capacitors will average transient input switching currents of the A/D (see sec- 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.



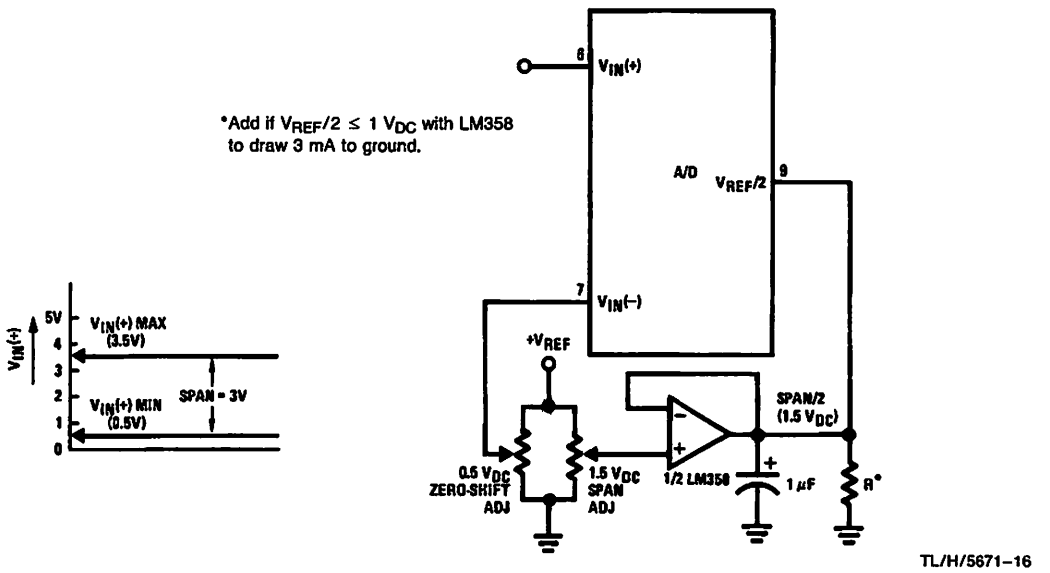
TL/H/5671–15

FIGURE 4. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

unctional Description (Continued)



TL/H/5671–16

a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5V (Digital Out = = 00_{HEX}) to 3.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

4.2 Reference Accuracy Requirements

ıe converter can be operated in a ratiometric mode or an ›solute mode. In ratiometric converter applications, the agnitude of the reference voltage is a factor in both the ıtput of the source transducer and the output of the A/D ›nverter and therefore cancels out in the final digital output ›de. The ADC0805 is specified particularly for use in ratio- etric applications with no adjustments required. In abso- le conversion applications, both the initial value and the mperature stability of the reference voltage are important ›tors in the accuracy of the A/D converter. For $V_{REF}/2$ ltages of 2.4 V_{DC} nominal value, initial errors of ±10 $/_{DC}$ will cause conversion errors of ±1 LSB due to the in of 2 of the $V_{REF}/2$ input. In reduced span applications, › initial value and the stability of the $V_{REF}/2$ input voltage come even more important. For example, if the span is ıuced to 2.5V, the analog input LSB voltage value is cor- ›pondingly reduced from 20 mV (5V span) to 10 mV and _SB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, s reduces the allowed initial tolerance of the reference ltage and requires correspondingly less absolute change ıh temperature variations. Note that spans smaller than ›V place even tighter requirements on the initial accuracy d stability of the reference source.

general, the magnitude of the reference voltage will re- ire an initial adjustment. Errors due to an improper value reference voltage appear as full-scale errors in the A/D nsfer function. IC voltage regulators may be used for ref- ›nces if the ambient temperature changes are not exces- e. The LM336B 2.5V IC reference diode (from National ›niconductor) has a temperature stability of 1.8 mV typ mV max) over $0°C \leq T_A \leq +70°C$. Other temperature ›ge parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

unctional Description (Continued)

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

the analog zero voltage of the A/D is shifted away from ound (for example, to accommodate an analog input sig- l that does not go to ground) this new zero reference ould be properly adjusted first. A $V_{IN}(+)$ voltage that uals this desired zero reference plus ½ LSB (where the B is calculated for the desired analog span, 1 LSB = ana- span/256) is applied to pin 6 and the zero reference ltage at pin 7 should then be adjusted to just obtain the $_{HEX}$ to 01_{HEX} code transition.

ie full-scale adjustment should then be made (with the pper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $_N(+)$ input which is given by:

$$V_{IN}(+) \text{ fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

ere:

V_{MAX} = The high end of the analog input range

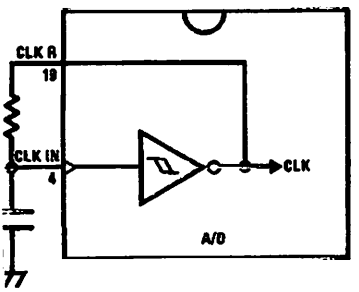
d

V_{MIN} = the low end (the offset zero) of the analog range. oth are ground referenced.)

ie $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a de change from FE_{HEX} to FF_{HEX}. This completes the ad- stment procedure.

5 Clocking Option

ie clock for the A/D can be derived from the CPU clock or external RC can be added to provide self-clocking. The .K IN (pin 4) makes use of a Schmitt trigger as shown in *gure 6.*



$$f_{CLK} \cong \frac{1}{1.1\,RC}$$

$R \cong 10\ k\Omega$

TL/H/5671–17

FIGURE 6. Self-Clocking the A/D

avy capacitive or DC loading of the clock R pin should be oided as this will disturb normal converter operation. ads less than 50 pF, such as driving up to 7 A/D convert- clock inputs from a single clock R pin of 1 converter, are owed. For larger clock line loading, a CMOS or low power L buffer or PNP input logic should be used to minimize loading on the clock R pin (do not use a standard TTL ffer).

Restart During a Conversion

he A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) ring a conversion, the converter is reset and a new con- sion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

nctional Description (Continued)

ngle point analog ground that is separate from the logic ınd points should be used. The power supply bypass acitor and the self-clocking capacitor (if used) should ı be returned to digital ground. Any $V_{REF}/2$ bypass ca-itors, analog input filter capacitors, or input signal shield-should be returned to the analog ground point. A test for ɔer grounding is to measure the zero error of the A/D verter. Zero errors in excess of ¼ LSB can usually be ed to improper board layout and wiring (see section 1 for measuring the zero error).

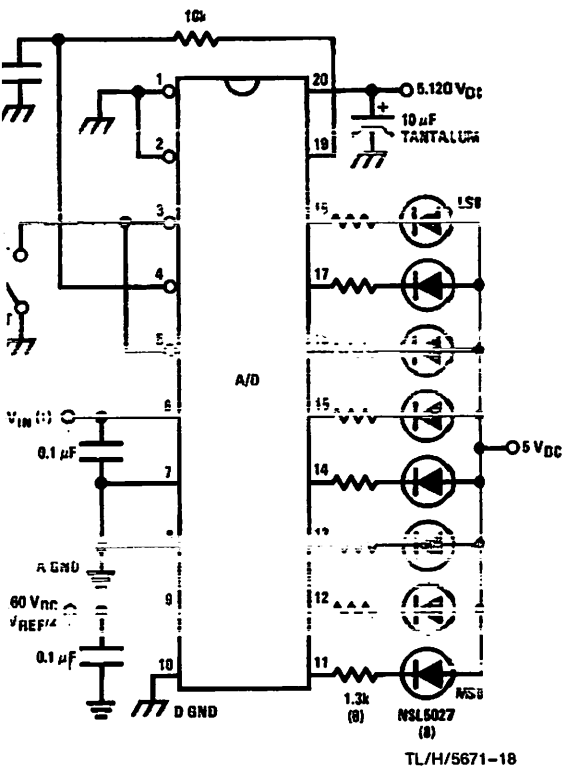
TESTING THE A/D CONVERTER

re are many degrees of complexity associated with test-an A/D converter. One of the simplest tests is to apply a wn analog input voltage to the converter and use LEDs isplay the resulting digital output code as shown in *Fig-7.*

ase of testing, the $V_{REF}/2$ (pin 9) should be supplied 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} uld be used. This provides an LSB value of 20 mV.

full-scale adjustment is to be made, an analog input age of 5.090 V_{DC} (5.120−1½ LSB) should be applied to $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of $V_{REF}/2$ input voltage should then be adjusted until the al output code is just changing from 1111 1110 to 1111 1. This value of $V_{REF}/2$ should then be used for all the s.

digital output LED display can be decoded by dividing 8 bits into 2 hex characters, the 4 most significant (MS) the 4 least significant (LS). Table I shows the fractional ıry equivalent of these two 4-bit groups. By adding the ages obtained from the "VMS" and "VLS" columns in le I, the nominal value of the digital display (when



TL/H/5671–18

FIGURE 7. Basic A/D Tester

$V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A−C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be [illegible] memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 may also be used — same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10*.

ctional Description (Continued)

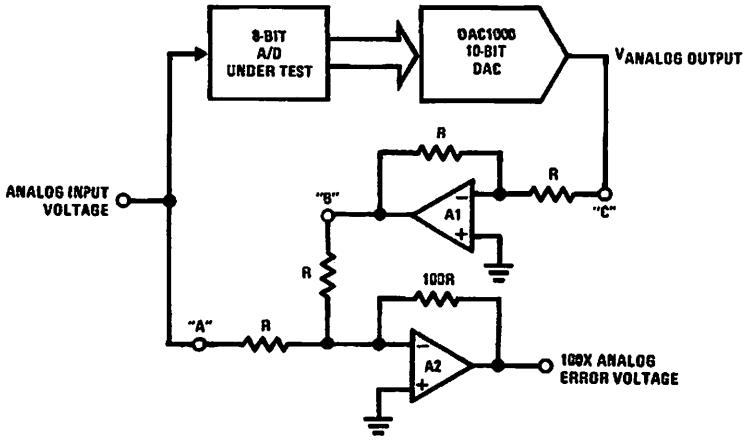
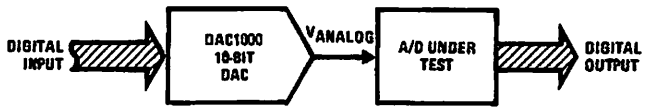


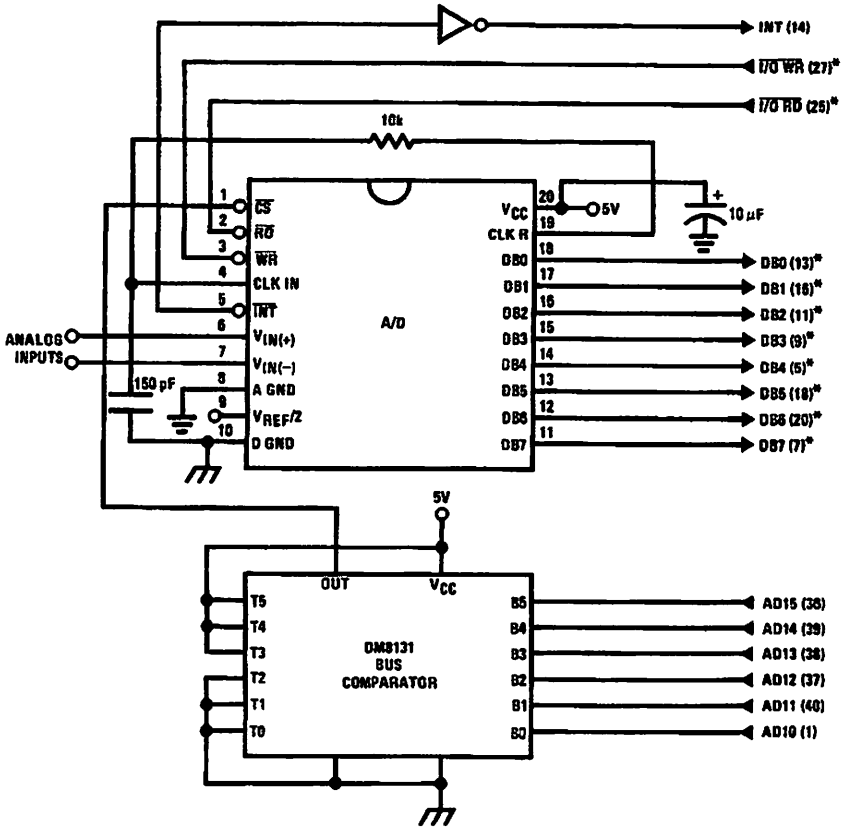
FIGURE 8. A/D Tester with Analog Error Output



TL/H/5671–19

FIGURE 9. Basic "Digital" A/D Tester

unctional Description (Continued)



TL/H/5671–20

Note 1: *Pin numbers for the DP8228 system controller, others are INS8080A.

Note 2: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 10. ADC0801–INS8080A CPU Interface

SAMPLE PROGRAM FOR *FIGURE 10* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:          JMP     LD DATA
  •       •           •
  •       •           •
0100    21 00 02    START:          LXI H 0200H         ; HL pair will point to
                                                        ; data storage locations
0103    31 00 04    RETURN:         LXI SP 0400H        ; Initialize stack pointer (Note 1)
0106    7D                          MOV A, L            ; Test # of bytes entered
0107    FE 0F                       CPI 0F H            ; If # = 16. JMP to
0109    CA 13 01                    JZ CONT             ; user program
010C    D3 E0                       OUT E0 H            ; Start A/D
010E    FB                          EI                  ; Enable interrupt
010F    00          LOOP:           NOP                 ; Loop until end of
0110    C3 0F 01                    JMP LOOP            ; conversion
0113      •         CONT:             •
  •       •           •               •
  •       •         (User program to  •
  •       •         process data)     •
  •       •           •               •
  •       •           •               •
0300    DB E0       LD DATA:        IN E0 H             ; Load data into accumulator
0302    77                          MOV M, A            ; Store data
0303    23                          INX H               ; Increment storage pointer
0304    C3 03 01                    JMP RETURN
```

e 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

te 2: All address used were arbitrarily chosen.

unctional Description (Continued)

ıe standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{R}$) can be directly wired to the digital control inputs of the 'D and the bus timing requirements are met to allow both arting the converter and outputting the data onto the data ıs. A bus driver should be used for larger microprocessor stems where the data bus leaves the PC board and/or ust drive capacitive loads larger than 100 pF.

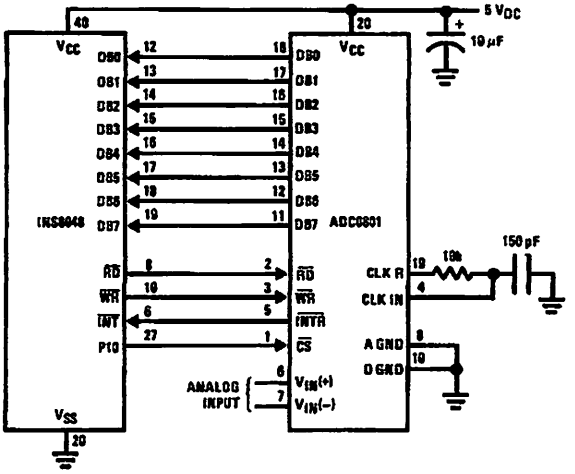
1.1 Sample 8080A CPU Interfacing Circuitry and Program

ıe following sample program and associated hardware own in *Figure 10* may be used to input data from the nverter to the INS8080A CPU chip set (comprised of the S8080A microprocessor, the INS8228 system controller d the INS8224 clock generator). For simplicity, the A/D is ntrolled as an I/O device, specifically an 8-bit bi-direction- port located at an arbitrarily chosen port address, E0. The RI-STATE output capability of the A/D eliminates the need r a peripheral interface device, however address decoding still required to generate the appropriate $\overline{CS}$ for the con- rter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 11*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.



TL/H/5671–21

FIGURE 11. INS8048 Interface

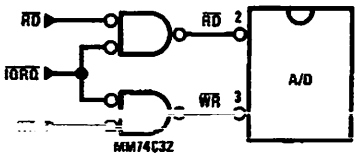
SAMPLE PROGRAM FOR *FIGURE 11* INS8048 INTERFACE

```
04 10                JMP     10H          ;Program starts at addr 10
                     ORG     3H
04 50                JMP     50H          ;Interrupt jump vector
                     ORG     10H          ;Main program
99 FE                ANL     P1, #0FEH    ;Chip select
81                   MOVX    A, @R1       ;Read in the 1st data
                                          ;to reset the intr
89 01      START:    ORL     P1, #1       ;Set port pin high
B8 20                MOV     R0, #20H     ;Data address
B9 FF                MOV     R1, #0FFH    ;Dummy address
BA 10                MOV     R2, #10H     ;Counter for 16 bytes
23 FF      AGAIN:    MOV     A, #0FFH     ;Set ACC for intr loop
99 FE                ANL     P1, #0FEH    ;Send CS (bit 0 of P1)
91                   MOVX    @R1, A       ;Send WR out
05                   EN      I            ;Enable interrupt
96 21      LOOP:     JNZ     LOOP         ;Wait for interrupt
EA 1B                DJNZ    R2, AGAIN    ;If 16 bytes are read
00                   NOP                  ;go to user's program
00                   NOP
                     ORG     50H
81         INDATA:   MOVX    A, @R1       ;Input data, CS still low
A0                   MOV     @R0, A       ;Store in memory
18                   INC     R0           ;Increment storage counter
89 01                ORL     P1, #1       ;Reset CS signal
27                   CLR     A            ;Clear ACC to get out of
93                   RETR                 ;the interrupt loop
```

unctional Description (Continued)

? Interfacing the Z-80

- Z-80 control bus is slightly different from that of the 80. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the general d strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is at the CPU will automatically insert one wait state (the $\overline{RD}$ d $\overline{WR}$ strobes are extended one clock period) to allow ore time for the I/O devices to respond. Logic to map the D in I/O space is shown in *Figure 13*.



TL/H/5671–23

FIGURE 13. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

ldditional I/O advantages exist as softwa... DMA ... e available and use can be made of the output data trans- which exists on the upper 8 address lines (A8 to A15) ring I/O input instructions. For example, MUX channel lection for the A/D can be accomplished with this operat- mode.

? Interfacing 6800 Microprocessor Derivatives (6502, etc.)

ıe control bus for the 6800 microprocessor derivatives es not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it em- ys a single R/$\overline{W}$ line and additional timing, if needed, can derived from the φ2 clock. All I/O devices are memory apped in the 6800 system, and a special signal, VMA, dicates that the current address is valid. *Figure 14* shows interface schematic where the A/D is memory mapped in e 6800 system. For simplicity, the $\overline{CS}$ decoding is shown ing ½ DM8092. Note that in many 6800 systems, an al- ready decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 15* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

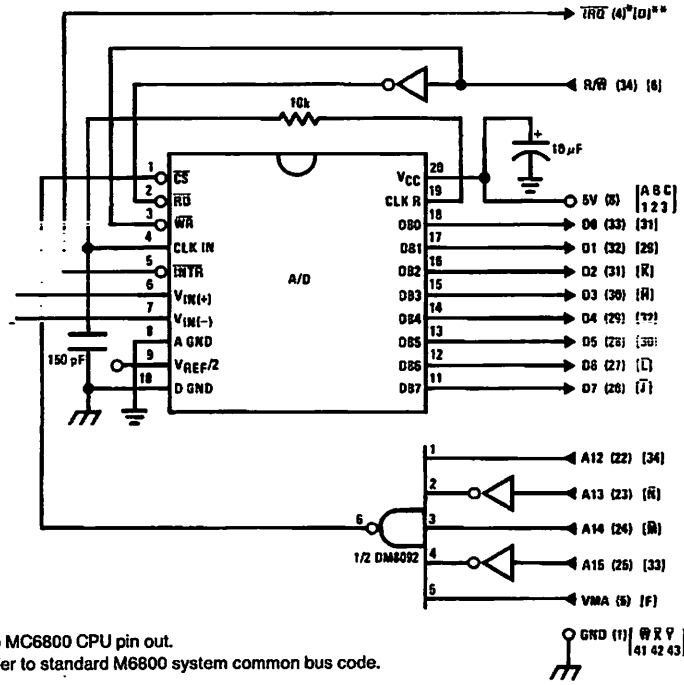
A sample interface program equivalent to the previous one is shown below *Figure 15*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexed single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels simultaneously. This scheme is shown in *Figure 15*.



e 1: Numbers in parentheses refer to MC6800 CPU pin out.
e 2: Number or letters in brackets refer to standard M6800 system common bus code.

TL/H/5671–24

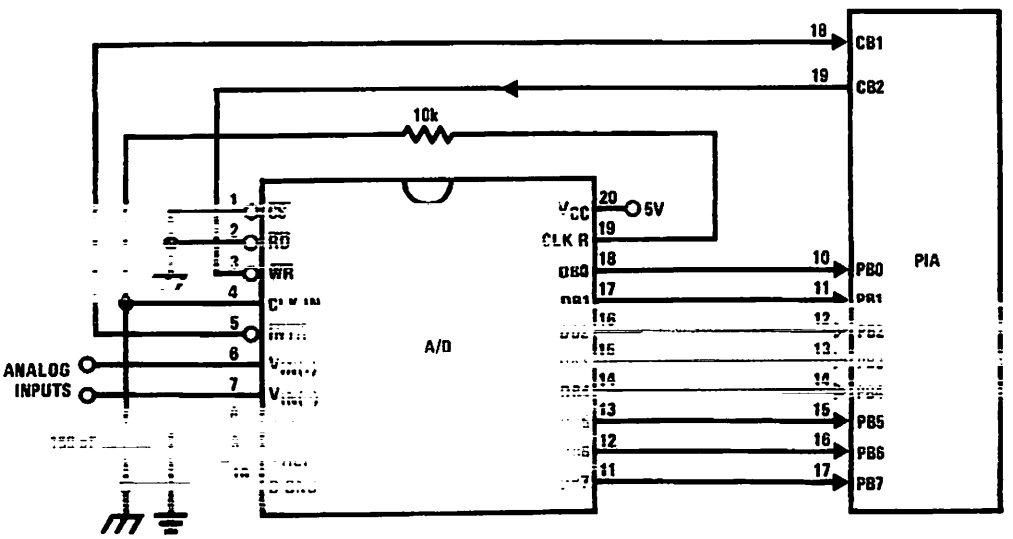
FIGURE 14. ADC0801-MC6800 CPU Interface

unctional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 14* ADC0801-MC6800 CPU INTERFACE

```
0010    DF 36       DATAIN   STX    TEMP2     ; Save contents of X
0012    CE 00 2C             LDX    #$002C    ; Upon IRQ low CPU
0015    FF FF F8             STX    $FFF8     ; jumps to 002C
0018    B7 50 00             STAA   $5000     ; Start ADC0801
001B    0E                   CLI
001C    3E          CONVRT   WAI               ; Wait for interrupt
001D    DE 34                LDX    TEMP1
001F    8C 02 0F             CPX    #$020F    ; Is final data stored?
0022    27 14                BEQ    ENDP
0024    B7 50 00             STAA   $5000     ; Restarts ADC0801
0027    08                   INX
0028    DF 34                STX    TEMP1
002A    20 F0                BRA    CONVRT
002C    DE 34       INTRPT   LDX    TEMP1
002E    B6 50 00             LDAA   $5000     ; Read data
0031    A7 00                STAA   X          ; Store it at X
0033    3B                   RTI
0034    02 00       TEMP1    FDB    $0200     ; Starting address for
                                               ; data storage
0036    00 00       TEMP2    FDB    $0000
0038    CE 02 00    ENDP     LDX    #$0200    ; Reinitialize TEMP1
003B    DF 34                STX    TEMP1
003D    DE 36                LDX    TEMP2
003F    39                   RTS               ; Return from subroutine
                                               ; To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.



TL/H/5671–25

FIGURE 15. ADC0801–MC6820 PIA Interface

unctional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 15* ADC0801–MC6820 PIA INTERFACE

```
0010   CE 00 38    DATAIN   LDX    #$0038    ; Upon IRQ low CPU
0013   FF FF F8             STX    $FFF8     ; jumps to 0038
0016   B6 80 06             LDAA   PIAORB    ; Clear possible IRQ flags
0019   4F                   CLRA
001A   B7 80 07             STAA   PIACRB
001D   B7 80 06             STAA   PIAORB    ; Set Port B as input
0020   0E                   CLI
0021   C6 34                LDAB   #$34
0023   86 3D                LDAA   #$3D
0025   F7 80 07    CONVRT   STAB   PIACRB    ; Starts ADC0801
0028   B7 80 07             STAA   PIACRB
002B   3E                   WAI               ; Wait for interrupt
002C   DE 40                LDX    TEMP1
002E   8C 02 0F             CPX    #$020F    ; Is final data stored?
0031   27 0F                BEQ    ENDP
0033   08                   INX
0034   DF 40                STX    TEMP1
0036   20 ED                BRA    CONVRT
0038   DE 40    INTRPT   LDX    TEMP1
003A   B6 80 06             LDAA   PIAORB    ; Read data in
003D   A7 00                STAA   X         ; Store it at X
003F   3B                   RTI
0040   02 00    TEMP1    FDB    $0200     ; Starting address for
                                           ; data storage
0042   CE 02 00    ENDP     LDX    #$0200    ; Reinitialize TEMP1
0045   DF 40                STX    TEMP1
0047   39                   RTS               ; Return from subroutine
               PIAORB   EQU    $8006     ; To user's program
               PIACRB   EQU    $8007
```

ıe following schematic and sample subroutine (DATA IN) ay be used to interface (up to) 8 ADC0801's directly to the C6800 CPU. This scheme can easily be extended to allow

nverters are (arbitrarily) located at HEX address 5000 in a MC6800 memory space. To save components, the ock signal is derived from just one RC pair on the first nverter. This output drives the other A/Ds.

the converters are started simultaneously with a STORE ıstruction at HEX address 5000. Note that any other HEX

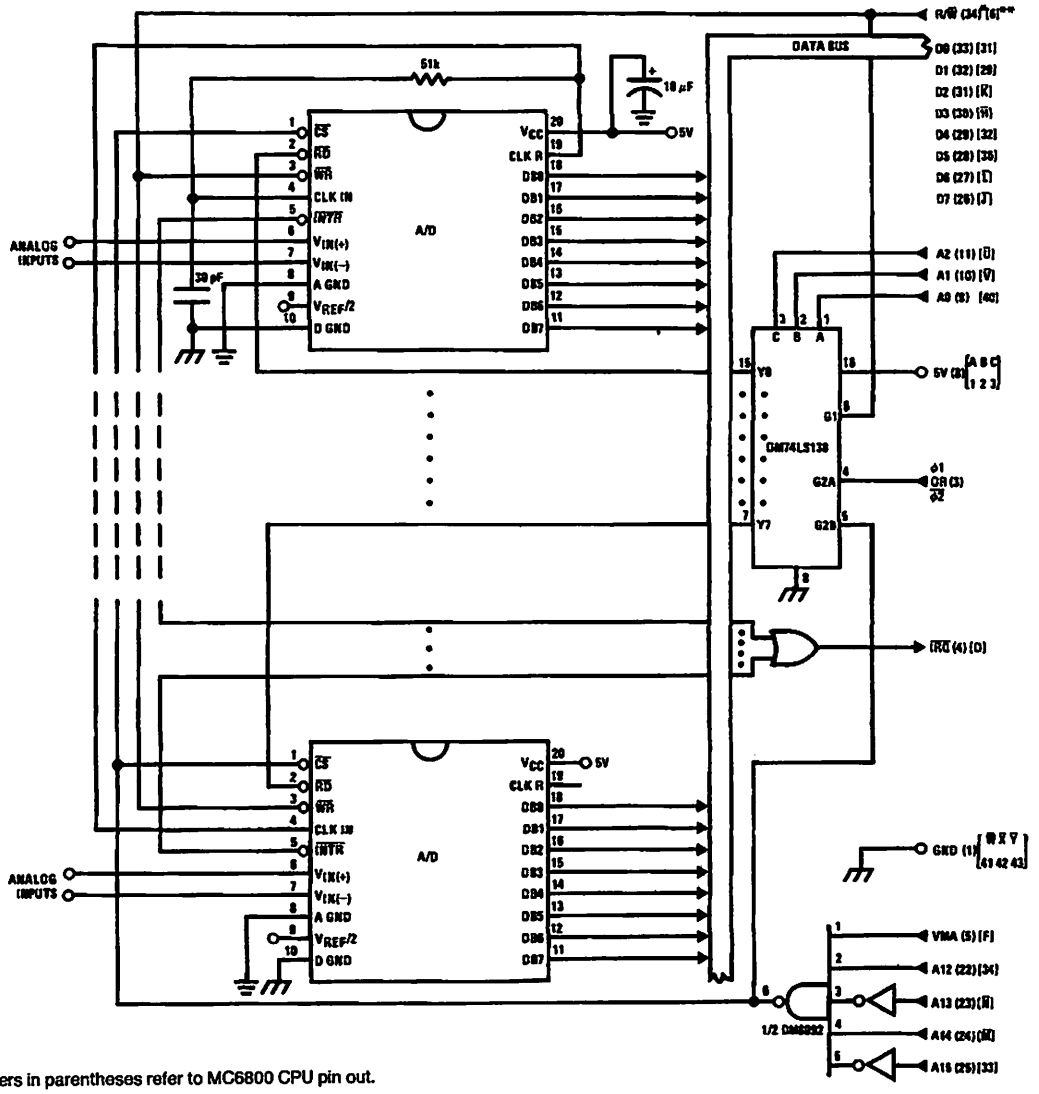
ıll the CS inputs low. This can easily be avoided by ing a more definitive address decoding scheme. All the errupts are ORed together to insure that all A/Ds have mpleted their conversion before the microprocessor rupted.

ıe subroutine, DATA IN, may be called from anywhere in e user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data temporarily at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before sending DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

unctional Description (Continued)



ote 1: Numbers in parentheses refer to MC6800 CPU pin out.

ote 2: Numbers of letters in brackets refer to standard M6800 system common bus code.

TL/H/5671–26

FIGURE 16. Interfacing Multiple A/Ds in an MC6800 System

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE	MNEMONICS			COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

ınctional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

te 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

ır amplification of DC input signals, a major system error is ə input offset voltage of the amplifiers used for the əamp. *Figure 17* is a gain of 100 differential preamp ıose offset voltage errors will be cancelled by a zeroing broutine which is performed by the INS8080A microproc-sor system. The total allowable input offset voltage error r this preamp is only 50 μV for ¼ LSB error. This would ıviously require very precise amplifiers. The expression for ə differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

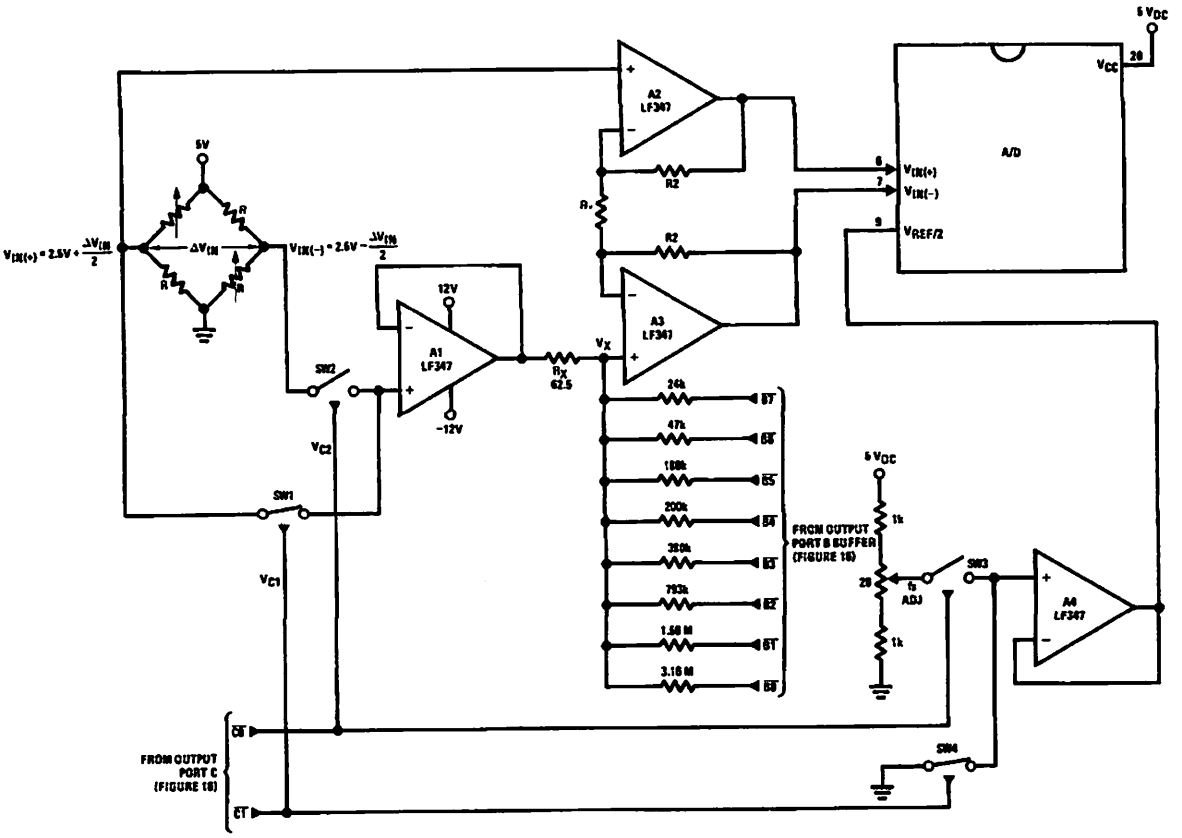
$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

here I_X is the current through resistor R_X. All of the offset *ror terms can be cancelled by making* $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing :heme.

ıe INS8080A uses the 3 I/O ports of an INS8255 Pro-amable Peripheral Interface (PPI) to control the auto zero-g and input data from the ADC0801 as shown in *Figure 18*. ıe PPI is programmed for basic I/O operation (mode 0) th Port A being an input port and Ports B and C being ıtput ports. Two bits of Port C are used to alternately open close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_X increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 μV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.

unctional Description (Continued)

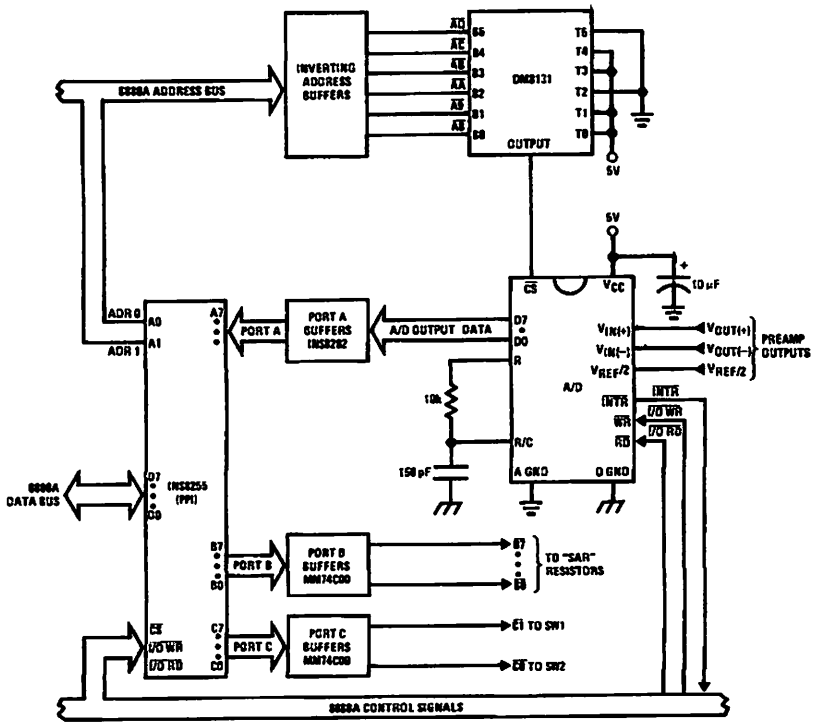


ote 1: R2 = 49.5 R1

ote 2: Switches are LMC13334 CMOS analog switches.

ote 3: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 17. Gain of 100 Differential Transducer Preamp



TL/H/5671–27

FIGURE 18. Microprocessor Interface Circuitry for Differential Preamp

flow chart for the zeroing subroutine is shown in *Figure* . It must be noted that the ADC0801 series will output an zero code when it converts a negative input [$V_{IN}(-) \geq$ $_{1}(+)$]. Also, a logic inversion exists as all of the I/O ports) buffered with inverting gates.

sically, if the data read is zero, the differential output volt- e is negative, so a bit in Port B is cleared to pull V_X more gative which will make the output more positive for the xt conversion. If the data read is not zero, the output volt- e is positive so a bit in Port B is set to make V_X more sitive and the output more negative. This continues for 8 proximations and the differential output eventually con- rges to within 5 mV of zero.

e actual program is given in *Figure 20*. All addresses ed are compatible with the BLC 80/10 microcomputer stem. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

data acquisition systems where more than one A/D con- rter (or other peripheral device) will be interrupting pro- am execution of a microprocessor, there is obviously a ied for the CPU to determine which device requires servic-). *Figure 21* and the accompanying software is a method determining which of 7 ADC0801 converters has com- ated a conversion ($\overline{INTR}$ asserted) and is requesting an errupt. This circuit allows starting the A/D converters in y sequence, but will input and store valid data from the nverters with a priority sequence of A/D 1 being read first, D 2 second, etc., through A/D 7 which would have the west priority for data being read. Only the converters ose INT is asserted will be read.

e key to decoding circuitry is the DM74LS373, 8-bit D pe flip-flop. When the Z-80 acknowledges the interrupt, e program is vectored to a data input Z-80 subroutine. is subroutine will read a peripheral status word from the M74LS373 which contains the logic state of the $\overline{INTR}$ out- uts of all the converters. Each converter which initiates an terrupt will place a logic "0" in a unique bit position in the atus word and the subroutine will determine the identity of e converter and execute a data read. An identifier word hich indicates which A/D the data came from) is stored in e next sequential memory location above the location of e data so the program can keep track of the identity of the ata entered.

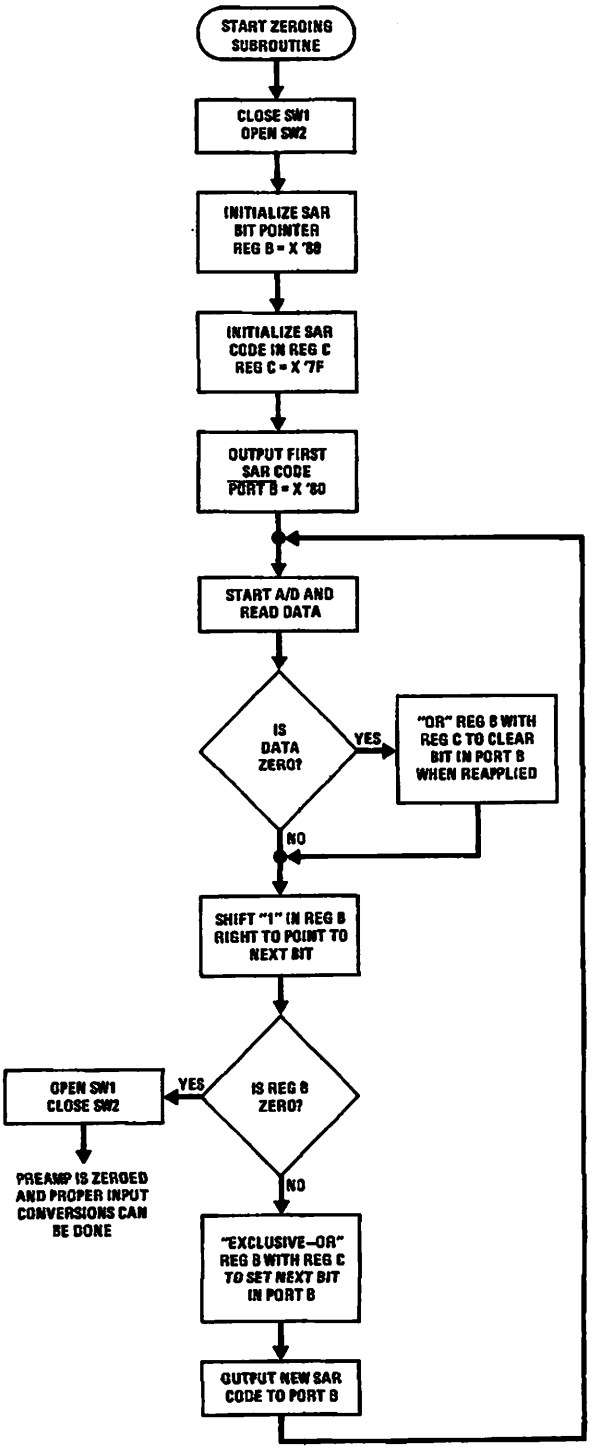


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FIGURE 19. Flow Chart for Auto-Zero Routine

```
3D00  3E90    MVI 90
3D02  D3E7    Out Control Port                    ;Program PPI
3D04  2601    MVI H 01          Auto-Zero Subroutine
3D06  7C      MOV A,H
3D07  D3E6    OUT C                              ;Close SW1 open SW2
3D09  0680    MVI B 80                           ;Initialize SAR bit pointer
3D0B  3E7F    MVI A 7F                           ;Initialize SAR code
3D0D  4F      MOV C,A           Return
3D0E  D3E5    OUT B                              ;Port B = SAR code
3D10  31AA3D  LXI SP 3DAA       Start            ;Dimension stack pointer
3D13  D3E4    OUT A                              ;Start A/D
3D15  FB      IE
3D16  00      NOP               Loop             ;Loop until INT asserted
3D17  C3163D  JMP Loop
3D1A  7A      MOV A,D           Auto-Zero
3D1B  C600    ADI 00
3D1D  CA2D3D  JZ Set C                           ;Test A/D output data for zero
3D20  78      MOV A,B           Shift B
3D21  F600    ORI 00                             ;Clear carry
3D23  1F      RAR                                ;Shift "1" in B right one place
3D24  FE00    CPI 00                             ;Is B zero? If yes last
3D26  CA373D  JZ Done                            ;approximation has been made
3D29  47      MOV B,A
3D2A  C3333D  JMP New C
3D2D  79      MOV A,C           Set C
3D2E  B0      ORA B                              ;Set bit in C that is in same
3D2F  4F      MOV C,A                            ;position as "1" in B
3D30  C3203D  JMP Shift B
3D33  A9      XRA C             New C            ;Clear bit in C that is in
3D34  C30D3D  JMP Return                         ;same position as "1" in B
3D37  47      MOV B,A           Done             ;then output new SAR code.
3D38  7C      MOV A,H                            ;Open SW1, close SW2 then
3D39  EE03    XRI 03                             ;proceed with program. Preamp
3D3B  D3E6    OUT C                              ;is now zeroed.
3D3D          •                 Normal
              •
              •
              Program for processing
              proper data values
3C3D  DBE4    IN A              Read A/D Subroutine  ;Read A/D data
3C3F  EEFF    XRI FF                             ;Invert data
3C41  57      MOV D,A
3C42  78      MOV A,B                            ;Is B Reg = 0? If not stay
3C43  E6FF    ANI FF                             ;in auto zero subroutine
3C45  C21A3D  JNZ Auto-Zero
3C48  C33D3D  JMP Normal
```

ote: All numerical values are hexadecimal representations.

FIGURE 20. Software for Auto-Zeroed Differential A/D

3 Multiple A/D Converters in a Z-80® Interrupt Driven Mode (Continued)

ne following notes apply:

It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

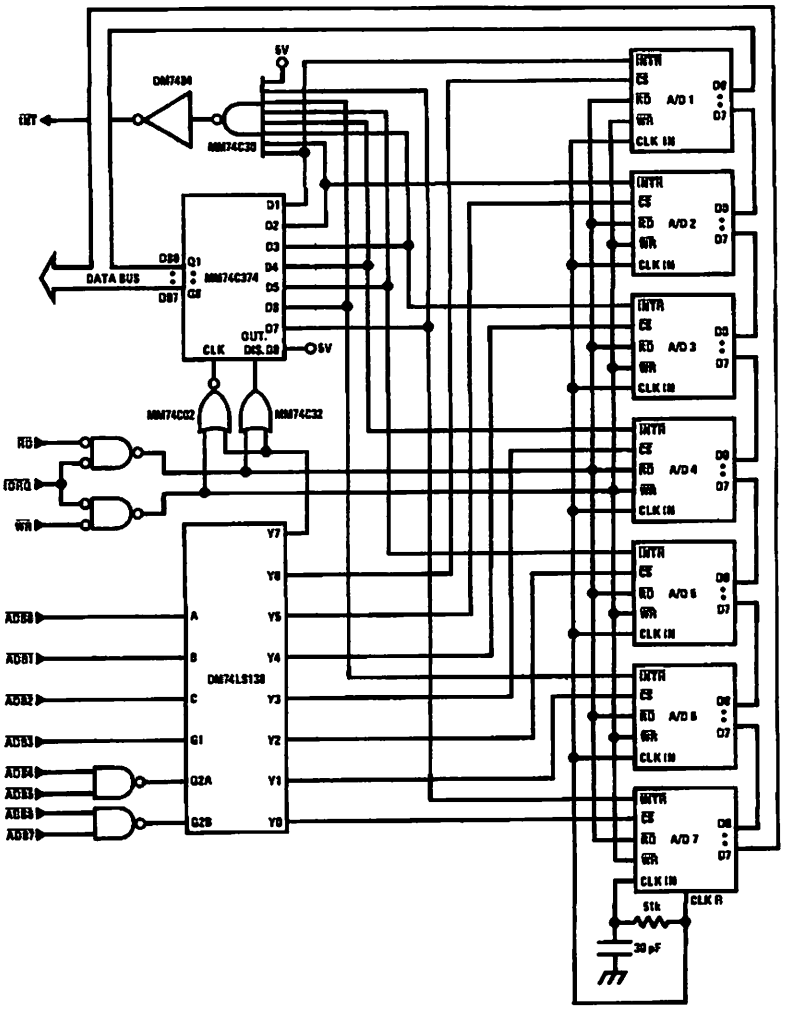
A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.



TL/H/5671–29

FIGURE 21. Multiple A/Ds with Z-80 Type Microprocessor

INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE		SOURCE STATEMENT	COMMENT
0038	E5		PUSH HL	;Save contents of all registers affected by
0039	C5		PUSH BC	;this subroutine.
003A	F5		PUSH AF	;Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL),X3E00	;Initialize memory pointer where data will be stored.
003E	0E 01		LD C, X01	;C register will be port ADDR of A/D converters.
0040	D300		OUT X00, A	;Load peripheral status word into 8-bit latch.
0042	DB00		IN A, X00	;Load status word into accumulator.
0044	47		LD B,A	;Save the status word.
0045	79	TEST	LD A,C	;Test to see if the status of all A/D's have
0046	FE 08		CP, X08	;been checked. If so, exit subroutine
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	;Test a single bit in status word by looking for
004C	1F		RRA	;a "1" to be rotated into the CARRY (an $\overline{INT}$
004D	47		LD B,A	;is loaded as a "1"). If CARRY is set then load
004E	DA 5500		JPC, LOAD	;contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	;If CARRY is not set, increment C register to point
0052	C3 4500		JP,TEST	;to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	;Read data from interrupting A/D and invert
0057	EE FF		XOR FF	;the data.
0059	77		LD (HL),A	;Store the data
005A	2C		INC L	
005B	71		LD (HL),C	;Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP,NEXT	;Test next bit in status word.
0060	F1	DONE	POP AF	;Re-establish all registers as they were
0061	C1		POP BC	;before the interrupt.
0062	E1		POP HL	
0063	C9		RET	;Return to original program

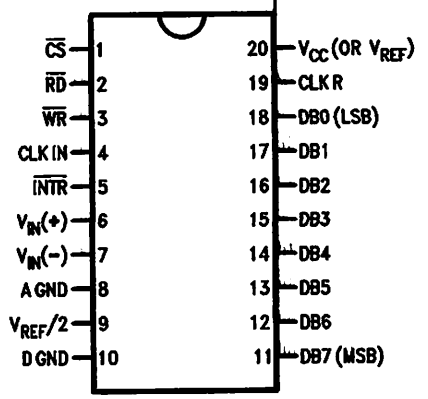
rdering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
RROR	±¼ Bit Adjusted				ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM	ADC0802LCV		ADC0802LCN
	±½ Bit Adjusted	ADC0803LCWM	ADC0803LCV		ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCV	ADC0804LCN	ADC0805LCN
PACKAGE OUTLINE		M20B—Small Outline	V20A—Chip Carrier	N20A—Molded DIP	

TEMP RANGE		−40°C TO +85°C	−55°C TO +125°C
ERROR	±¼ Bit Adjusted	ADC0801LCJ	ADC0801LJ
	±½ Bit Unadjusted	ADC0802LCJ	ADC0802LJ,
	±½ Bit Adjusted	ADC0803LCJ	ADC0802LJ/883
	±1Bit Unadjusted	ADC0804LCJ	
PACKAGE OUTLINE		J20A—Cavity DIP	J20A—Cavity DIP

onnection Diagrams

ADC080X
Dual-In-Line and Small Outline (SO) Packages



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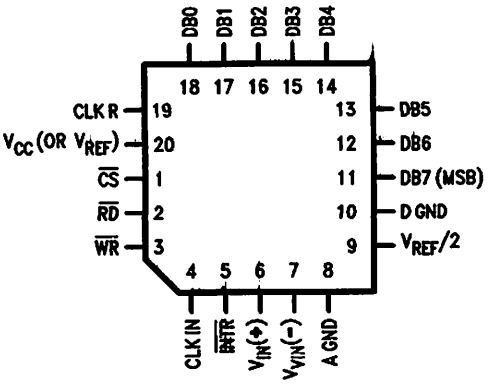
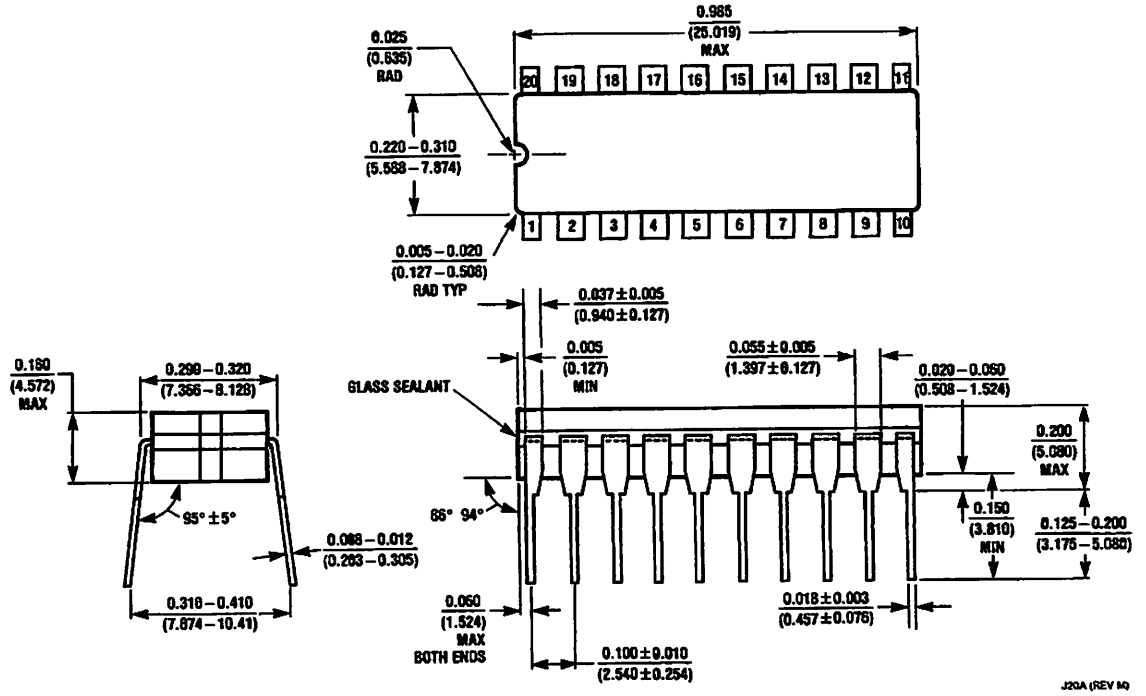
ADC080X
Molded Chip Carrier (PCC) Package



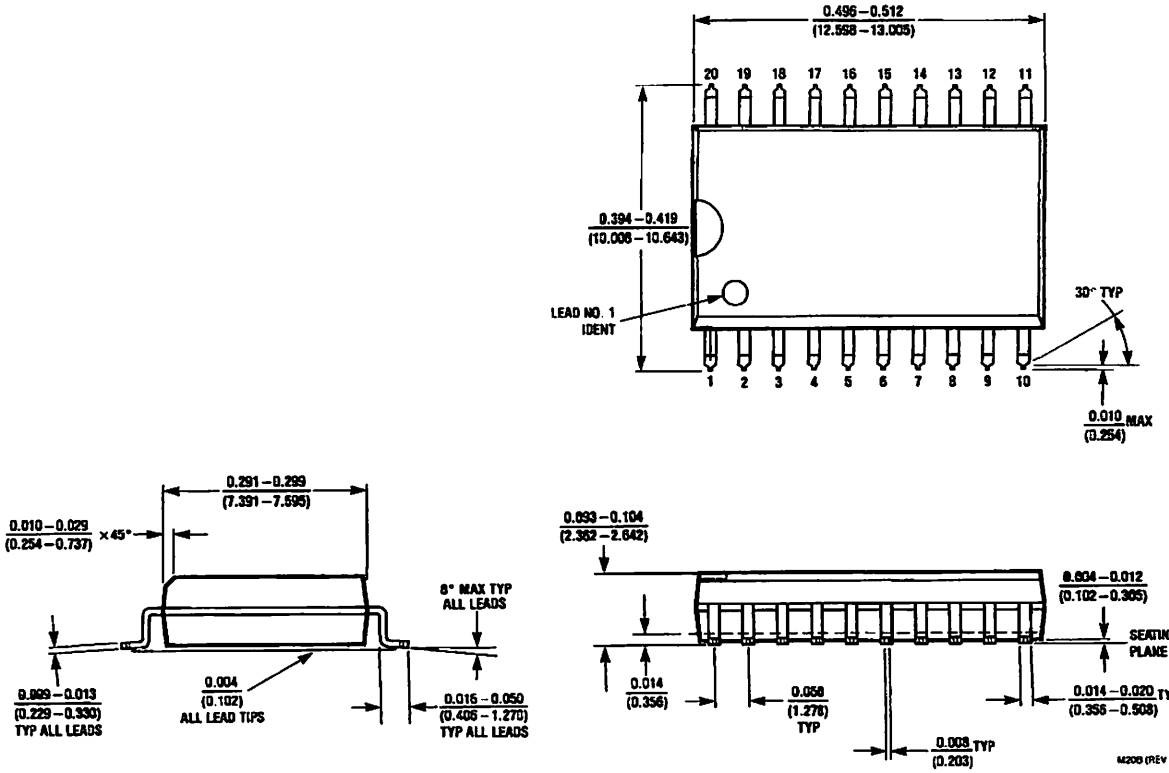
TL/H/5671–32

See Ordering Information

hysical Dimensions inches (millimeters)

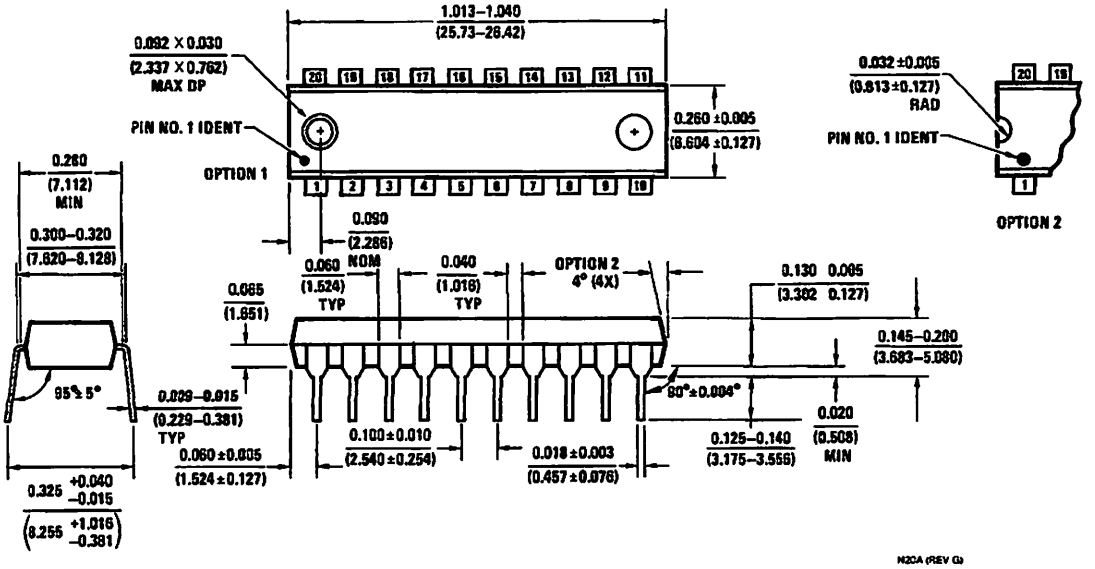


Dual-In-Line Package (J)
Order Number ADC0801LJ, ADC0802LJ, ADC0801LCJ,
ADC0802LCJ, ADC0803LCJ or ADC0804LCJ
ADC0802LJ/883 or 5962-9096601MRA
NS Package Number J20A



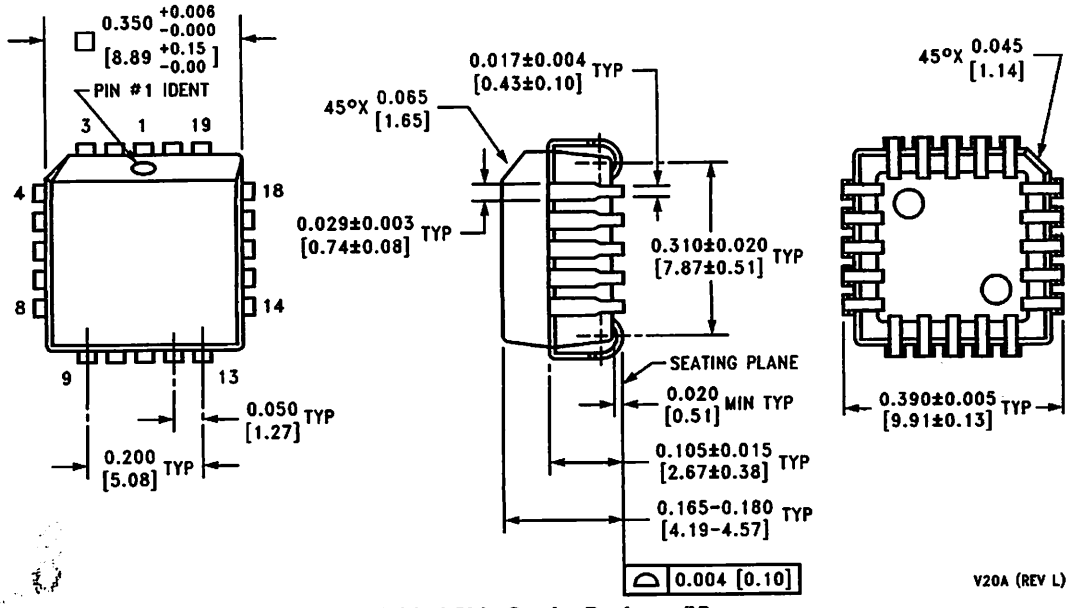
SO Package (M)
Order Number ADC0802LCWM, ADC0803LCWM or ADC0804LCWM
NS Package Number M20B

hysical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number ADC0801LCN, ADC0802LCN, ADC0803LCN, ADC0804LCN or ADC0805LCN
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



Molded Chip Carrier Package (V)
Order Number ADC0802LCV, ADC0803LCV or ADC0804LCV
NS Package Number V20A

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es

- ible with MCS-51® Products
- s of In-System Programmable (ISP) Flash Memory
- lurance: 1000 Write/Erase Cycles
- 5.5V Operating Range
- atic Operation: 0 Hz to 33 MHz
- evel Program Memory Lock
- bit Internal RAM
- rammable I/O Lines
- bit Timer/Counters
- rrupt Sources
- plex UART Serial Channel
- wer Idle and Power-down Modes
- ot Recovery from Power-down Mode
- log Timer
- ata Pointer
- off Flag
- ogramming Time
- ISP Programming (Byte and Page Mode)

iption

9S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K in-system programmable Flash memory. The device is manufactured using igh-density nonvolatile memory technology and is compatible with the indus-ard 80C51 instruction set and pinout. The on-chip Flash allows the program to be reprogrammed in-system or by a conventional nonvolatile memory pro-. By combining a versatile 8-bit CPU with in-system programmable Flash on a ic chip, the Atmel AT89S51 is a powerful microcontroller which provides a xible and cost-effective solution to many embedded control applications.

9S51 provides the following standard features: 4K bytes of Flash, 128 bytes of I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-o-level interrupt architecture, a full duplex serial port, on-chip oscillator, and cuitry. In addition, the AT89S51 is designed with static logic for operation zero frequency and supports two software selectable power saving modes. Mode stops the CPU while allowing the RAM, timer/counters, serial port, and system to continue functioning. The Power-down mode saves the RAM con-freezes the oscillator, disabling all other chip functions until the next external or hardware reset.

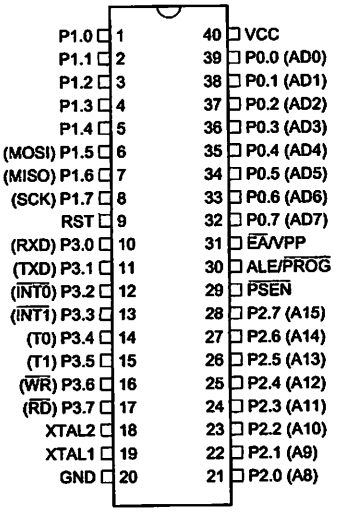
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

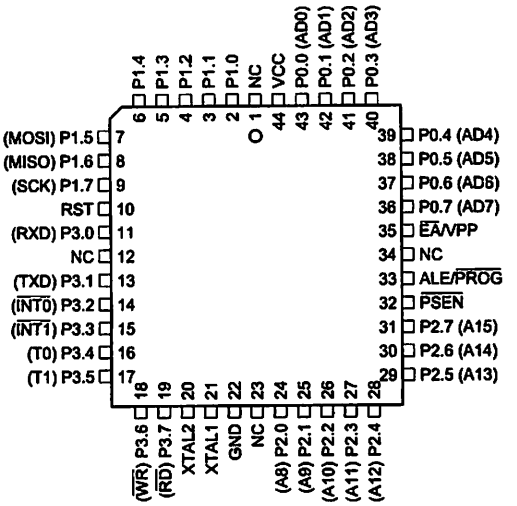
Rev. 2487A–10/01

nfigurations

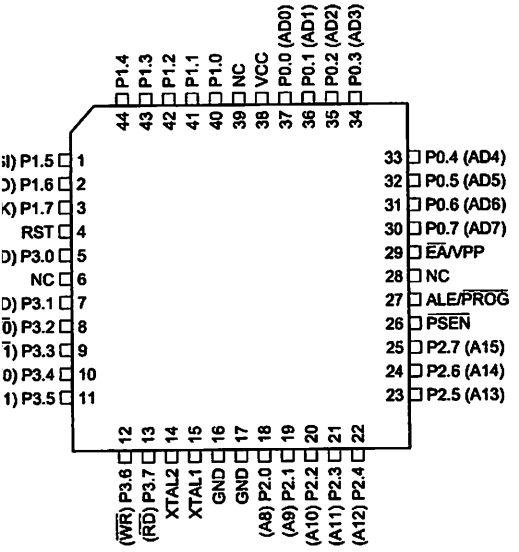
PDIP



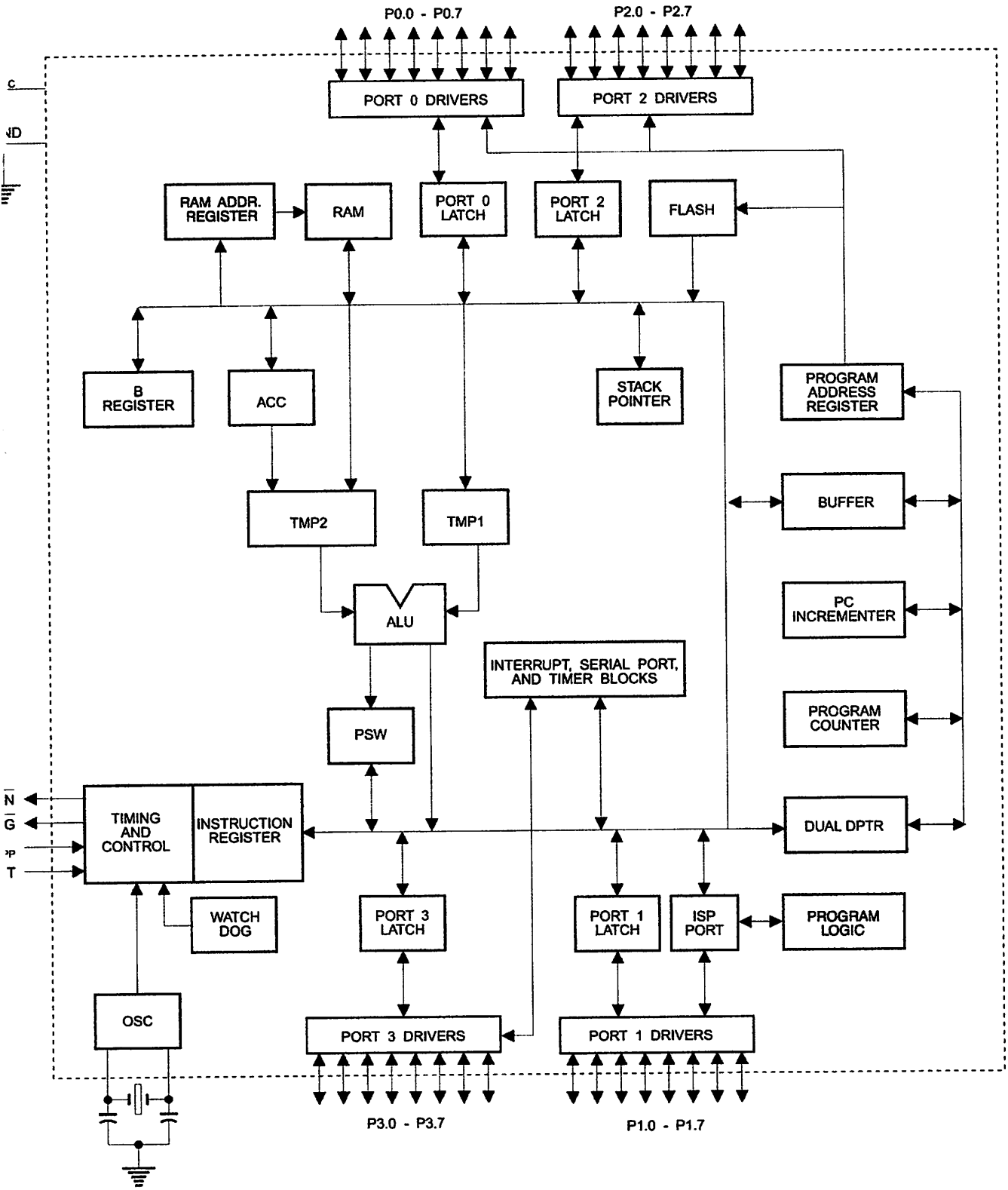
PLCC



TQFP



Diagram


P0.0 - P0.7
P2.0 - P2.7
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
ISP PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

scription

Supply voltage.

Ground.

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

Output from the inverting oscillator amplifier

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

AT89S51 SFR Map and Reset Values

								0FFH
B 00000000								0F7H
								0EFH
ACC 00000000								0E7H
								0DFH
PSW 00000000								0D7H
								0CFH
								0C7H
IP XX000000								0BFH
P3 11111111								0B7H
IE 0X000000								0AFH
P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
SCON 00000000	SBUF XXXXXXXX							9FH
P1 11111111								97H
TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

ry ization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

m Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

emory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

ıdog

time ed with -out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

)uring -down le

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

ıpts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

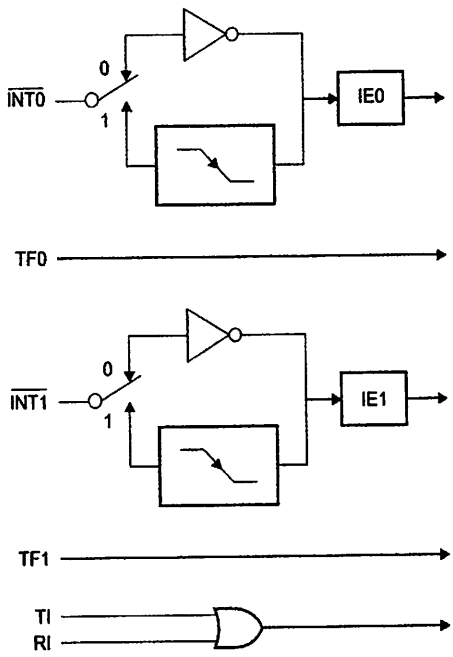
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

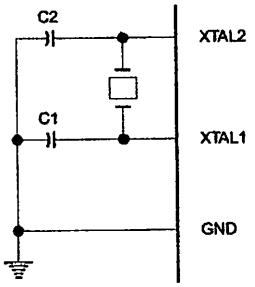
Figure 1. Interrupt Sources



tor :teristics

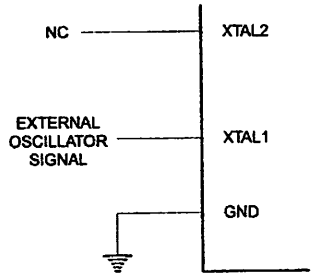
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



ode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

-down

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{INT0}$ or $\overline{INT1}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

ım ry Lock

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

ıamming ash – el Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

ımming ısh – Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

mming hm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

$\overline{\text{Data}}$ Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

ıming ion Set

mming ce – l Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

	V_{CC}	RST	$\overline{\text{PSEN}}$	ALE/ $\overline{\text{PROG}}$	$\overline{\text{EA}}$/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
e Data	5V	H	L	~ (2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
e Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
: Bit 1	5V	H	L	~ (3)	12V	H	H	H	H	H	X	X	X
Bit 2	5V	H	L	~ (3)	12V	H	H	H	L	L	X	X	X
Bit 3	5V	H	L	~ (3)	12V	H	L	H	H	L	X	X	X
Bits	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
s	5V	H	L	~ (1)	12V	H	L	H	L	L	X	X	X
ıl ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
ice ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
ice ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

1. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{\text{BSY}}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

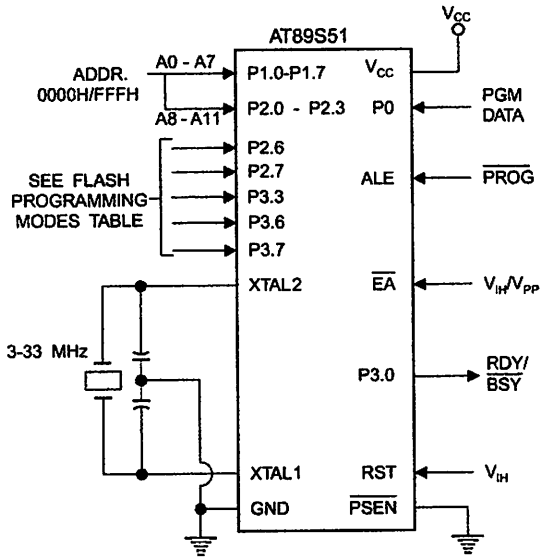
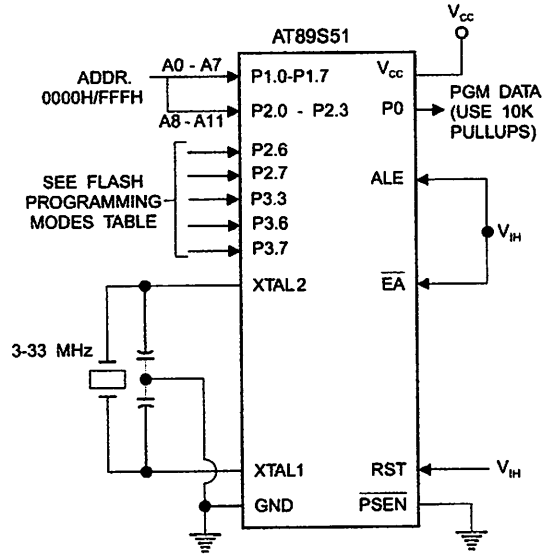


Figure 5. Verifying the Flash Memory (Parallel Mode)

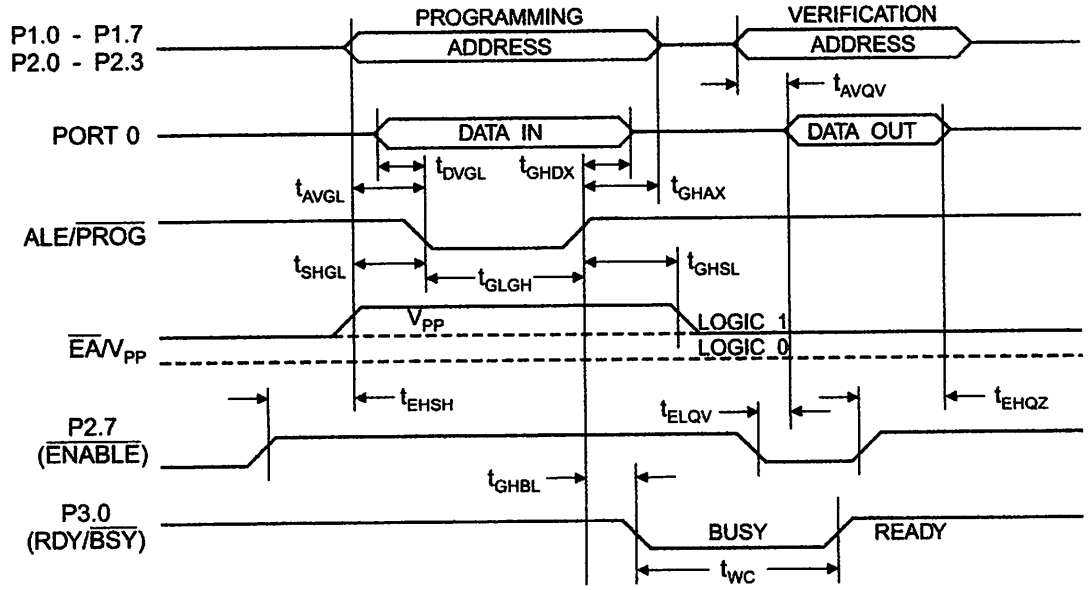


Programming and Verification Characteristics (Parallel Mode)

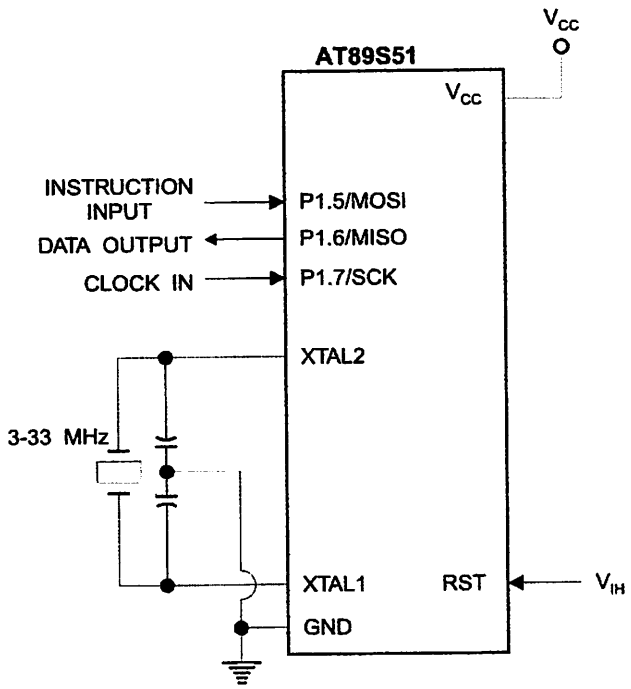
to 30°C, V_{CC} = 4.5 to 5.5V

	Parameter	Min	Max	Units
	Programming Supply Voltage	11.5	12.5	V
	Programming Supply Current		10	mA
	V_{CC} Supply Current		30	mA
	Oscillator Frequency	3	33	MHz
	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
	V_{PP} Hold After $\overline{PROG}$	10		µs
	$\overline{PROG}$ Width	0.2	1	µs
	Address to Data Valid		$48t_{CLCL}$	
	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		50	µs

Flash Programming and Verification Waveforms – Parallel Mode

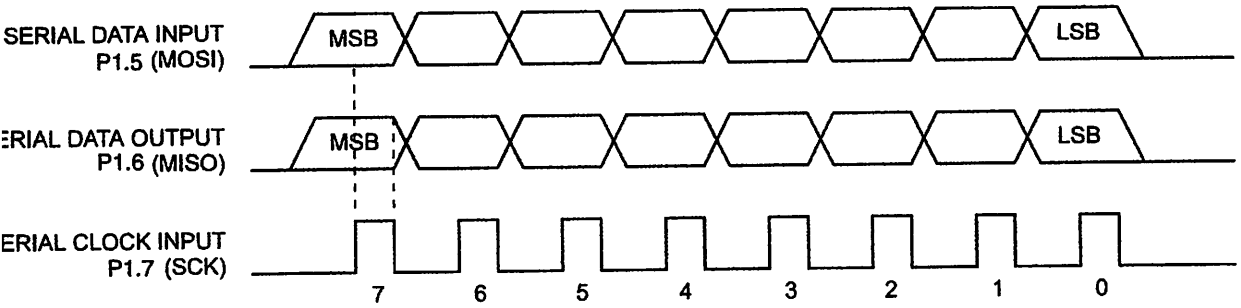


Flash Memory Serial Downloading



Programming and Verification Waveforms – Serial Mode

Serial Programming Waveforms



erial Programming Instruction Set

n	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
ing Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
e	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
gram Memory e)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
gram Memory e)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
ature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
gram Memory de)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
gram Memory de)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

The signature bytes are not readable in Lock Bit Modes 3 and 4.

B1 = 0, B2 = 0 → Mode 1, no lock protection
B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
B1 = 1, B1 = 1 → Mode 4, lock bit 3 activated

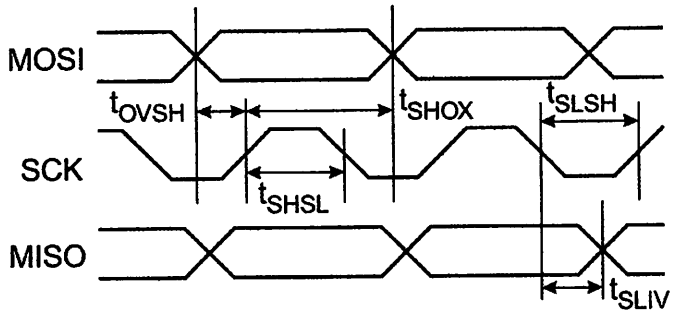
} Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Programming Characteristics

I. Serial Programming Timing



Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

	Parameter	Min	Typ	Max	Units
	Oscillator Frequency	0		33	MHz
	Oscillator Period	30			ns
	SCK Pulse Width High	8 t_{CLCL}			ns
	SCK Pulse Width Low	8 t_{CLCL}			ns
	MOSI Setup to SCK High	t_{CLCL}			ns
	MOSI Hold after SCK High	2 t_{CLCL}			ns
	SCK Low to MISO Valid	10	16	32	ns
	Chip Erase Instruction Cycle Time			500	ms
	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

ıte Maximum Ratings*

Temperature	-55°C to +125°C
emperature	-65°C to +150°C
n Any Pin ect to Ground	-1.0V to +7.0V
Operating Voltage	6.6V
ıt Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

aracteristics

s shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
	Reset Pulldown Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
. Minimum V_{CC} for Power-down is 2V.

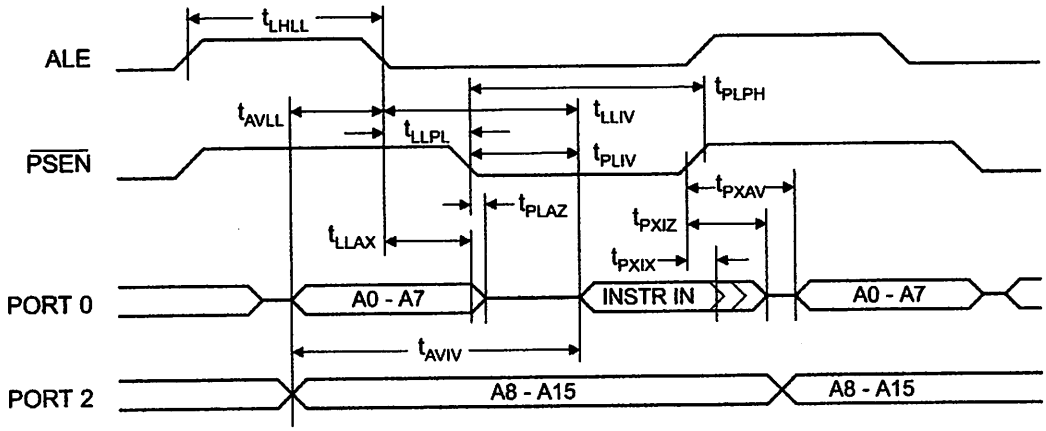
ıracteristics

rating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other 30 pF.

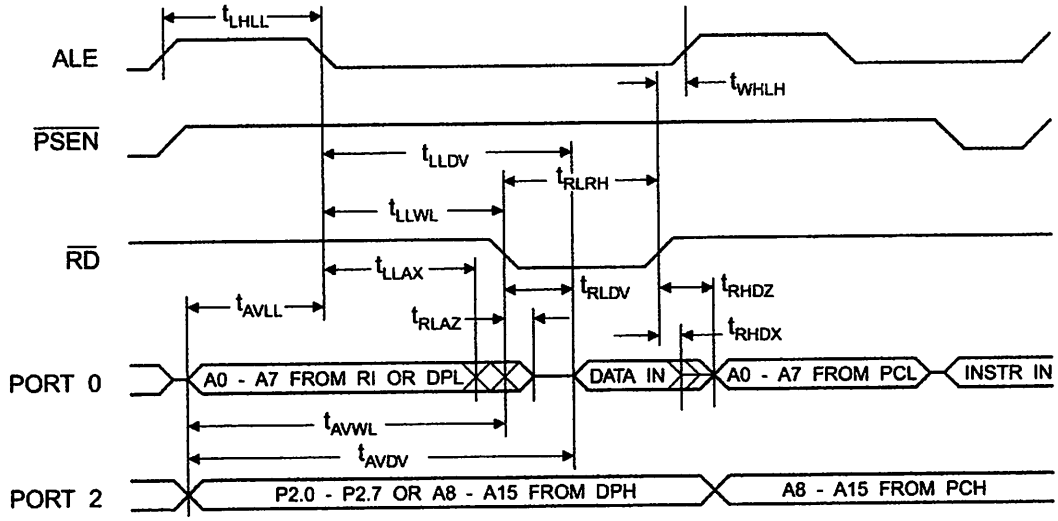
al Program and Data Memory Characteristics

Parameter	12 MHz Oscillator		Variable Oscillator		Units
	Min	Max	Min	Max	
Oscillator Frequency			0	33	MHz
ALE Pulse Width	127		$2t_{CLCL}$-40		ns
Address Valid to ALE Low	43		t_{CLCL}-25		ns
Address Hold After ALE Low	48		t_{CLCL}-25		ns
ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
Input Instruction Hold After $\overline{PSEN}$	0		0		ns
Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
$\overline{PSEN}$ Low to Address Float		10		10	ns
$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
Data Hold After $\overline{RD}$	0		0		ns
Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
Address to Valid Data In		585		$9t_{CLCL}$-165	ns
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
$\overline{RD}$ Low to Address Float		0		0	ns
$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

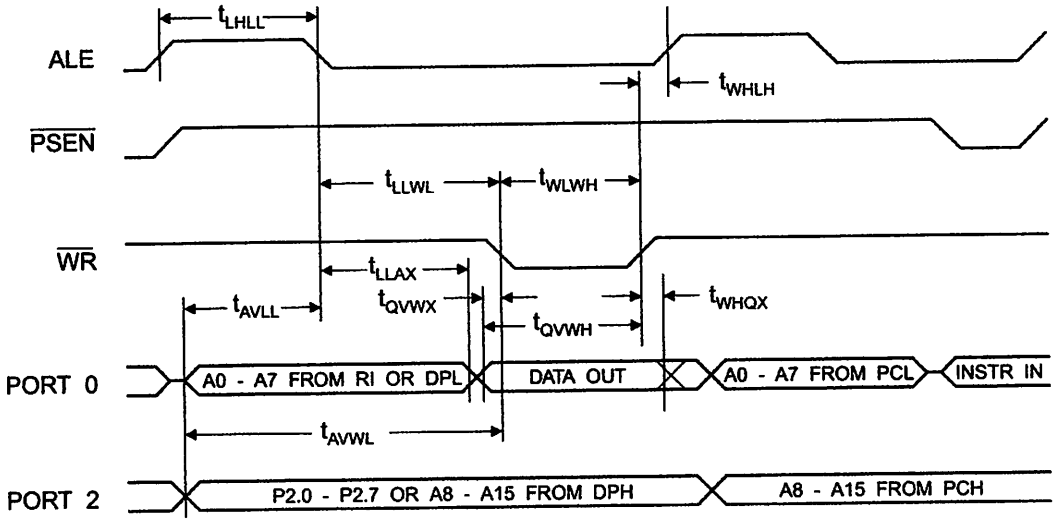
al Program Memory Read Cycle



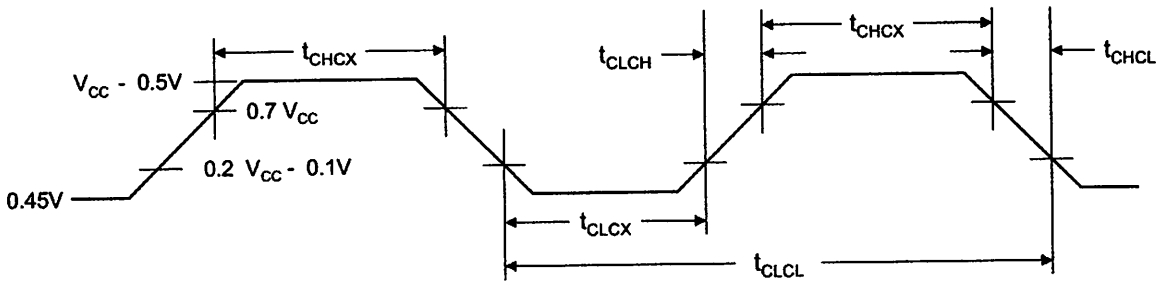
al Data Memory Read Cycle



al Data Memory Write Cycle



al Clock Drive Waveforms



al Clock Drive

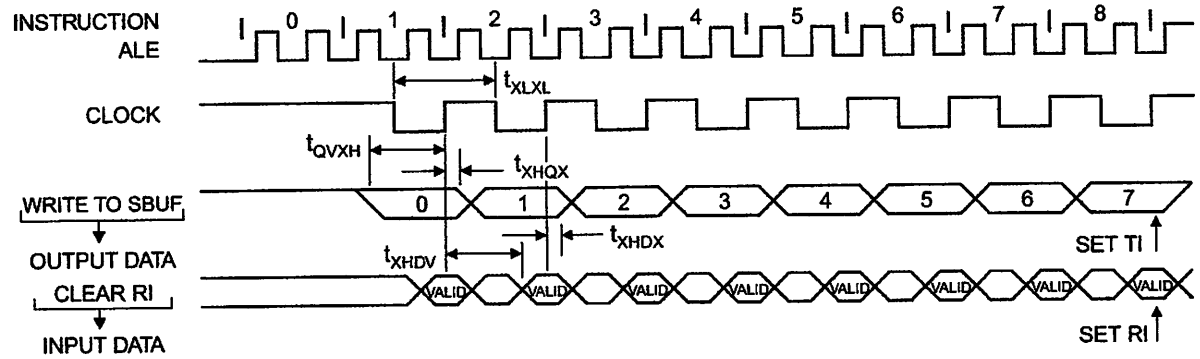
	Parameter	Min	Max	Units
	Oscillator Frequency	0	33	MHz
	Clock Period	30		ns
	High Time	12		ns
	Low Time	12		ns
	Rise Time		5	ns
	Fall Time		5	ns

ort Timing: Shift Register Mode Test Conditions

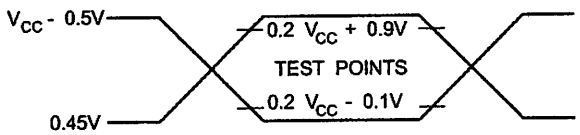
in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
	Input Data Hold After Clock Rising Edge	0		0		ns
	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

egister Mode Timing Waveforms

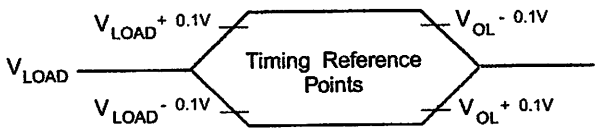


sting Input/Output Waveforms(1)



AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Waveforms(1)



. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

ıg Information

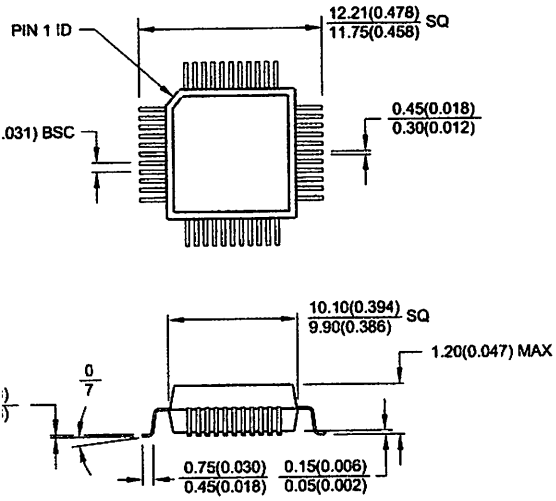
	Power Supply	Ordering Code	Package	Operation Range
	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC	44A 44J 40P6	Commercial (0° C to 70° C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI	44A 44J 40P6	Industrial (-40° C to 85° C)
	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC	44A 44J 40P6	Commercial (0° C to 70° C)

= Preliminary Availability

	Package Type
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

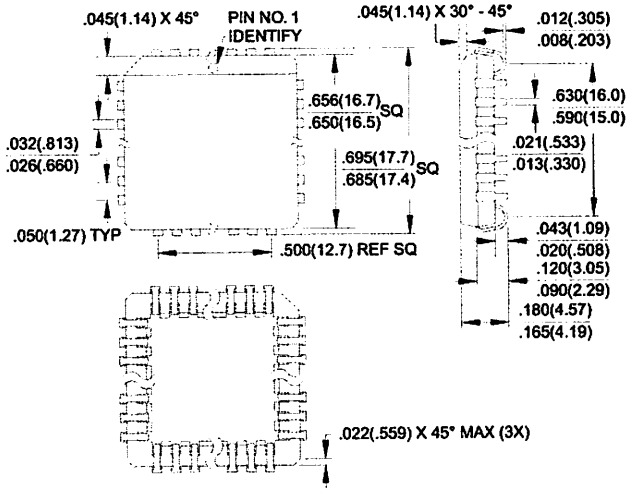
ing Information

4-lead, Thin (1.0 mm) Plastic Gull Wing Quad
ackage (TQFP)
sions in Millimeters and (Inches)*

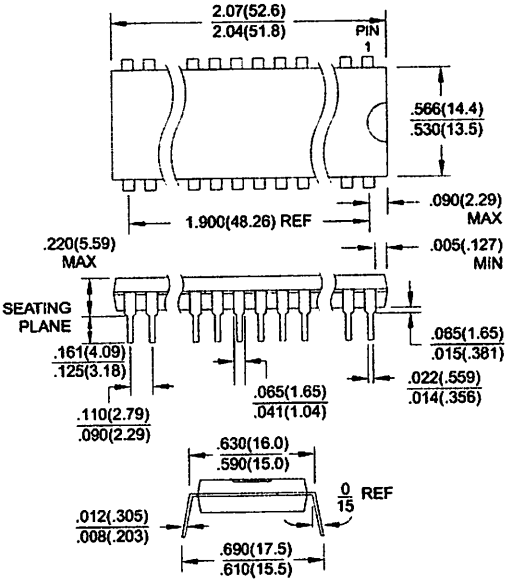


rolling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



, 40-pin, 0.600" Wide, Plastic Dual Inline
ge (PDIP)
nsions in Inches and (Millimeters)
: STANDARD MS-011 AC



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2487A–10/01/xM

AN.No.1632-711E

LIQUID CRYSTAL DISPLAY MODULE

M 1 6 3 2

USER MANUAL

Seiko Instruments Inc.

PREFACE

This manual describes technical informations on functions and instructions of M1632 from Seiko Instruments Inc. Please read this instruction manual carefully to understand all the module functions and make the best use of them. Description details may be changed without notice.

Revision Record

Edition	Revision	Date
1	Original	April 1985
2	Completely revised	Jan. 1987

ENERAL

1 General

The M1632 is a low-power-consumption dot-matrix liquid crystal display (LCD) module with a high-contrast wide-view TN LCD panel and a CMOS LCD drive controller built in. The controller has a built-in character generator ROM/RAM, and display data RAM. All the display functions are controlled by instructions and the module can easily be interfaced with an MPU. This makes the module applicable to a wide range of purposes including terminal display units for microcomputers and display units for measuring gages.

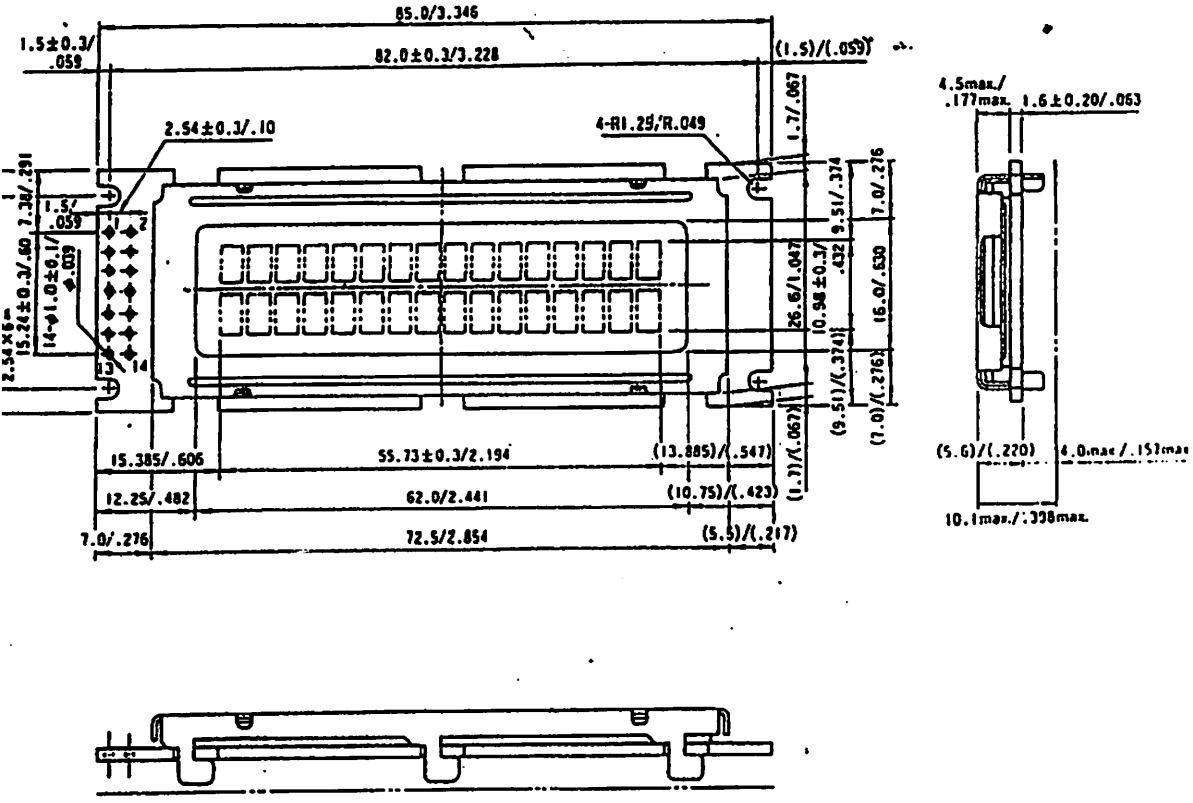
2 Features

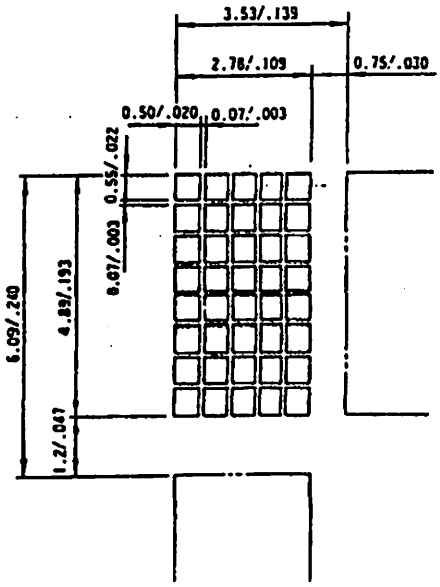
- 16-character, two-line TN liquid crystal display of 5 x 7 dot matrix + cursor
- Duty ratio: 1/16
- Character generator ROM for 192 character types (character font: 5 x 7 dot matrix)
- Character generator RAM for eight character types (program write) (character font: 5 x 7 dot matrix)
- 80 x 8 bit display data RAM (80 characters maximum)
- Interface with four-bit and eight-bit MPUs possible
- Display data RAM and character generator RAM readable from MPU
- Many instruction functions

  Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, and Display Shift

- Built-in oscillator circuit
- +5 V single power supply
- Built-in automatic reset circuit at power-on
- CMOS process
- Operating temperature range: 0°C to 50°C

Dimensions Diagram



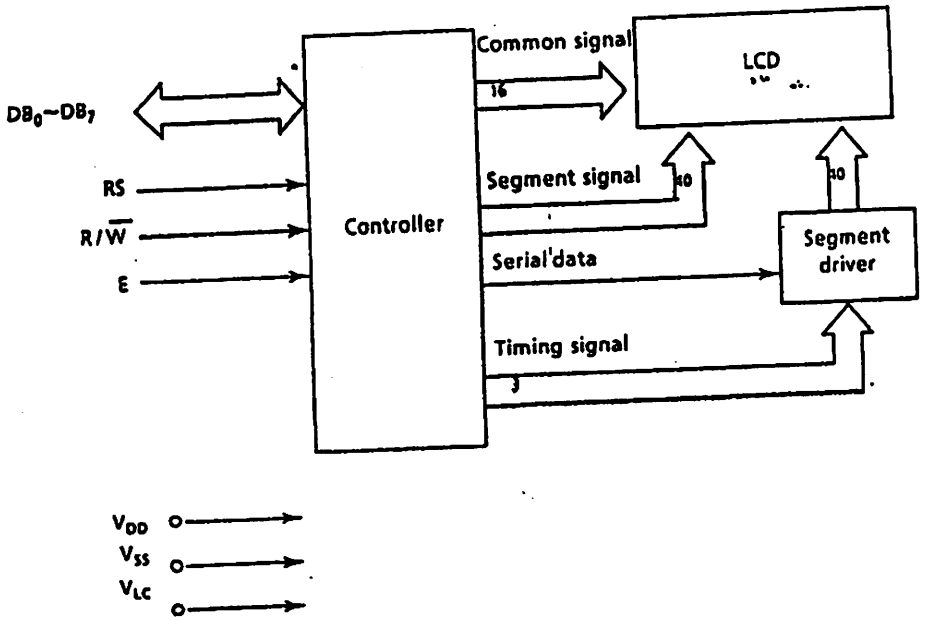


Unit : mm/inch
General tolerance : ± 0.5 mm

No.	Symbol	Level	Function	
1	Vss	-	Power Supply	0V (GND)
2	Vcc	-		5V ±10%
3	Vee	-		for LCD Drive
4	RS	H/L	H: Data Input L: Instruction Input	
5	R/W	H/L	H:READ L:WRITE	
6	E	H, ↓	Enable Signal	
7	DB0	H/L	Data Bus	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+ BL	-	Back Light Supply	4 - 4.2V 50-200mA
16	V- BL	-		0V (GND)

Figure 1 Dimensions diagran

Block Diagram



Absolute Maximum Ratings

V_{SS} = 0 V

Item	Symbol	Standard	Unit	Remarks
Power supply voltage	V_{DD}	− 0.3 to + 7.0	V	
	V_{LC}	V_{DD} − 13.5 to V_{DD} + 0.3	V	
Input voltage	V_{in}	− 0.3 to V_{DD} + 0.3,	V	
Operating temperature	T_{opr}	0 to + 50	°C	
Storage temperature	T_{stg}	− 20 to + 60	°C	At 50% RH

Electrical Characteristics

V_{DD} = 5 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Conditions	Standard			Unit
				Min.	Typ.	Max.	
Input voltage	High	V_{IH1}		2.2	−	V_{DD}	V
	Low	V_{IL1}		0	−	0.6	V
Output voltage (TTL)	High	V_{OH1}	$-I_{OH}$ = 0.205 mA	2.4	−	−	V
	Low	V_{OL1}	I_{OL} = 1.2 mA	−	−	0.4	V
Output voltage (CMOS)	High	V_{OH2}	$-I_{OH}$ = 0.04 mA	0.9V_{DD}	−	−	V
	Low	V_{OL2}	I_{OL} = 0.04 mA	−	−	0.1V_{DD}	V
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		V_{LC}	V_{DD} = 5 V, T_A = 25°C	−	0.25	−	V
Current consumption		I_{DD}		−	2.0	3.0	mA
		I_{LC}	V_{LC} = 0.25V	−	−	1.0	mA
Clock oscillation freq.		f_{osc}	Resistance oscillation	190	270	350	kHz

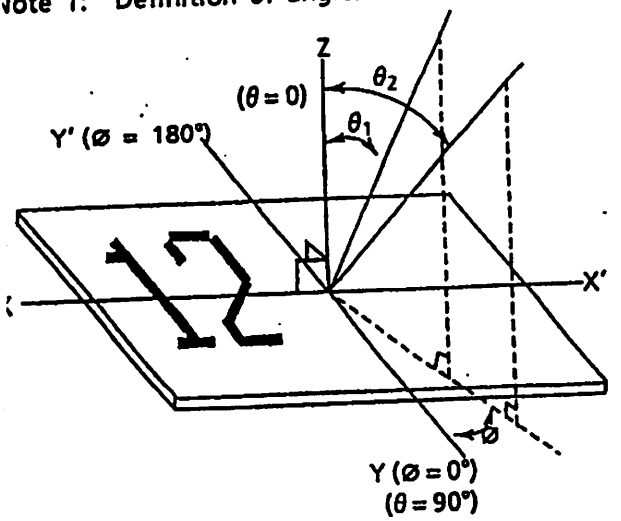
Optical Characteristics

1.7.1 Optical characteristics

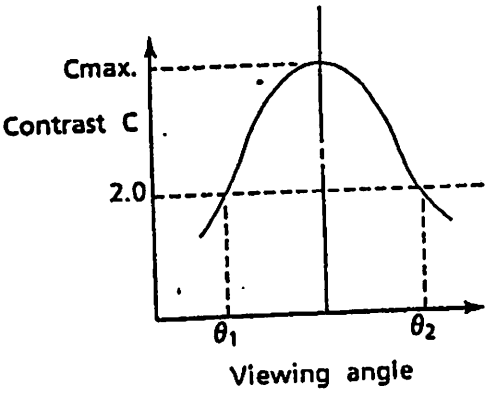
Maximum viewing angle: 6 o'clock (ϕ = 0°)
T_A = 25°C, V_{opr} = 4.75 V

Item	Symbol	Conditions	Min.	Typ.	Max.	Remarks
Viewing angle	$\theta_2 - \theta_1$	$C \geq 2.0$, $\phi = 0°$	35	–	–	See Notes 1 and 2.
Contrast	C	$\theta = 25°$, $\phi = 0°$	5	8	–	See Note 3.
Rise time	t_{on}	$\theta = 25°$, $\phi = 0°$	–	60 ms	70 ms	See Note 4.
Fall time	t_{off}	$\theta = 25°$, $\phi = 0°$	–	150 ms	170 ms	See Note 4.

Note 1: Definition of angles ϕ and θ

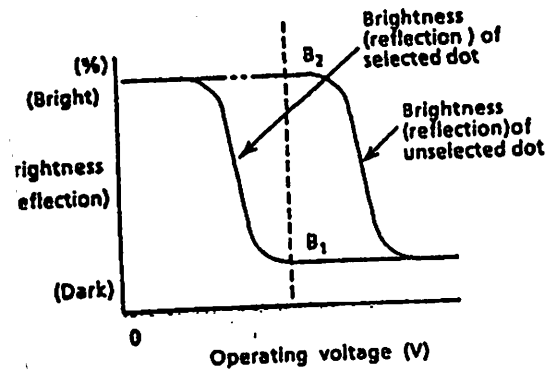


Note 2: Definition of viewing angles θ_1 and θ_2

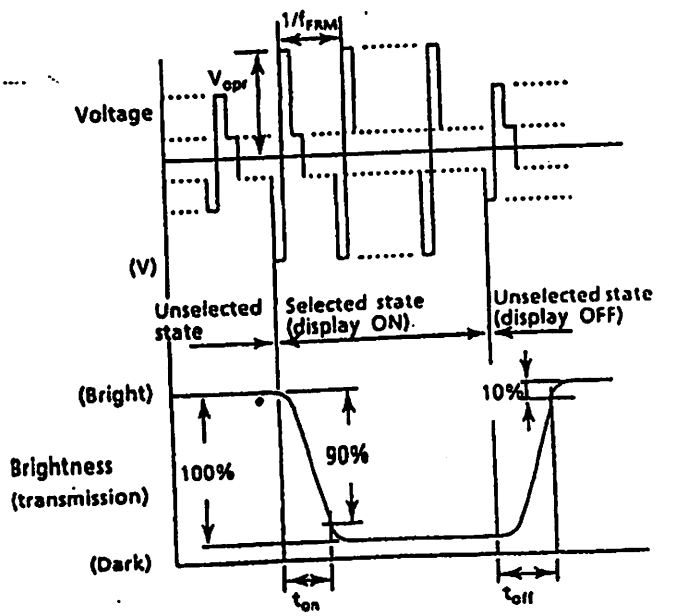


Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



V_{opr} : Operating voltage (V)
f_{FRM} : Frame frequency (Hz)
t_{on} : Response time (rise)(ms)
t_{off} : Response time (fall)(ms)

7.2 Recommended operating voltage

The viewing angle and screen contrast of the LCD panel can be varied by changing the liquid crystal operating voltage (V_{opr}), that is V_{LC}.

The optical characteristics is influenced by an ambient temperature. The recommended value of V_{opr} for an ambient temperatures are shown below.

Temperature (℃)	0	10	25	40	50
Voltage V_{opr} (V)	5.00	4.90	4.75	4.60	4.50

$V_{opr} = V_{DD} - V_{LC}$

ERATING INSTRUCTIONS

Terminal Functions

Table 1 Terminal functions

ıal name	No. of terminals	I/O	Destination	Function
$_0$ to DB_3	4	I/O	MPU	Tristate bidirectional lower four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. If the interface data is 4 bits, the signals are not used.
$_4$ to DB_7	4	I/O	MPU	Tristate bidirectional upper four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. DB_7 is also used as a busy flag.
E	1	Input	MPU	Operation start signal: The signal activates data write or read.
R/$\overline{W}$	1	Input	MPU	Read (R) and Write ($\overline{W}$) selection signals 0 : Write 1 : Read
RS	1	Input	MPU	Register selection signals 0 : Instruction register (Write) Busy flag and address counter (Read) 1 : Data register (Write and Read)
V_{LC}	1	–	Power supply	Power supply terminal for driving liquid crystal display: The screen contrast can be varied by changing V_{LC}.
V_{DD}	1	–	Power supply	+5 V
V_{SS}	1	–	Power supply	Ground terminal: 0 V

Basic Operations

2.1 Registers

The controller has two kinds of eight-bit registers: the instruction register (IR) and the data register (DR). They are selected by the register select (RS) signal as shown in Table 2.

The IR stores instruction codes such as Display Clear and Cursor Shift, and the address information of display data RAM (DD RAM) and character generator RAM (CG RAM). They can be written from the MPU, but cannot be read to the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM, or read from DD RAM or CG RAM. When data is written into DD RAM or CG RAM from the MPU, the data in the DR is automatically written into DD RAM or CG RAM by internal operation. However, when data is read from DD RAM or CG RAM, the necessary data address is written into the IR. The specified data is read out to the DR and then the MPU reads it from the DR. After the read operation, the next address is set and DD RAM or CG RAM data at the address is read into the DR for the next read operation.

Table 2 Register selection

RS	R/$\overline{W}$	Operation
0	0	IR selection, IR write. Internal operation : Display clear
0	1	Busy flag (DB_7) and address counter (DB_0 to DB_6) read
1	0	DR selection, DR write. Internal operation : DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation : DD RAM or CG RAM to DR

2.2.2 Busy flag (BF)

The flag indicates whether the module is ready to accept the next instruction. As shown in Table 2, the signal is output to DB_7 if RS = 0 and R/$\overline{W}$ = 1. If the value is 1, the module is working internally and the instruction cannot be accepted. If the value is 0, the next instruction can be written. Therefore, the flag status needs to be checked before executing an instruction. If an instruction is executed without checking the flag status, wait for more than the execution time shown by 2.4 Instruction Outline.

2.3 Address counter (AC)

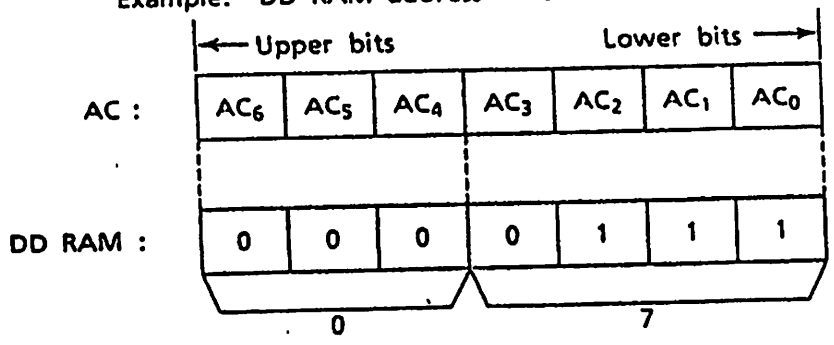
The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB_0 to DB_6 as shown in Table 2 if RS = 0 and $R/\overline{W}$ = 1.

2.4 Display data RAM (DD RAM)

DD RAM has a capacity of up to 80 × 8 bits and stores display data of 80 eight-bit character codes. Some storage areas of DD RAM which are not used for display can be used as general data RAM.

A DD RAM address to be set in the AC is expressed in hexadecimal form as follows.

Example: DD RAM address = 07



00_H to $0F_H$ of the DD RAM address is set in the line 1, and 40_H to $4F_H$ in the line 2.

Note : The addresses in the digit 16 of line 1 and the digit 1 of line 2 are not consecutive.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
ine 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM address
ine 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

If the display is shifted, DD RAM address 00_H to 27_H are displayed in line 1 and 40_H to 67_H in line 2. The following figures are examples of display shifts.

*Left shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
ine 1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	DD RAM address
ne 2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	

*Right shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
ne 1	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	DD RAM address
ne 2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

Character generator ROM (CG ROM)

Character generator ROM generates 192 types of 5 x 7 dot-matrix character patterns from eight-bit character codes.

Table 3 shows the correspondence between the CG ROM character codes and character patterns.

Character generator RAM (CG RAM)

CG RAM is used to create character patterns freely by programming. Eight types of character patterns can be written.

Table 4 shows the character patterns created from CG RAM addresses and data. To display a created character pattern, the character code in the left column of the table is written into DD RAM corresponding to the display position (digit). The areas not used for display are available as general data RAM.

Table 3 Correspondence between character codes and character patterns

er bit / 4 bit	0 0000	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	1010	1011	1100	1101	1110	1111
×0000	CG RAM (1)												
×0001	(2)												
×0010	(3)												
×0011	(4)												
×0100	(5)												
×0101	(6)												
×0110	(7)												
×0111	(8)												
××1000	(1)												
××1001	(2)												
××1010	(3)												
××1011	(4)												
××1100	(5)												
××1101	(6)												
××1110	(7)												
××1111	(8)												

Table 4 Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data)

Character code (DD RAM data)	CG RAM address	Character pattern (CG RAM data)
6 5 4 3 2 1 0 ← per bit Lower bit →	5 4 3 ← Upper bit	2 1 0 Lower bit →
0 0 0 * 0 0 0	0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1
0 0 0 * 0 0 1	0 0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1
		0 0 0 0 0 1
0 0 0 * 1 1 1	1 1 1	1 0 0 1 0 1 1 1 0 1 1 1

Example of character pattern (R)

← Cursor position

Example of character pattern (¥)

Notes: • In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display.

- Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).
- CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is changed to 1, one bit lights, regardless of the cursor.

The character pattern column positions correspond to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.

When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00_H and 08_H select the same character.

Timing Characteristics

1.1 Write timing characteristics

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		t_{CYCE}	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er},t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$ — E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data setup time		t_{DSW}	195	–	ns
Data hold time		t_H	10	–	ns

Write operation

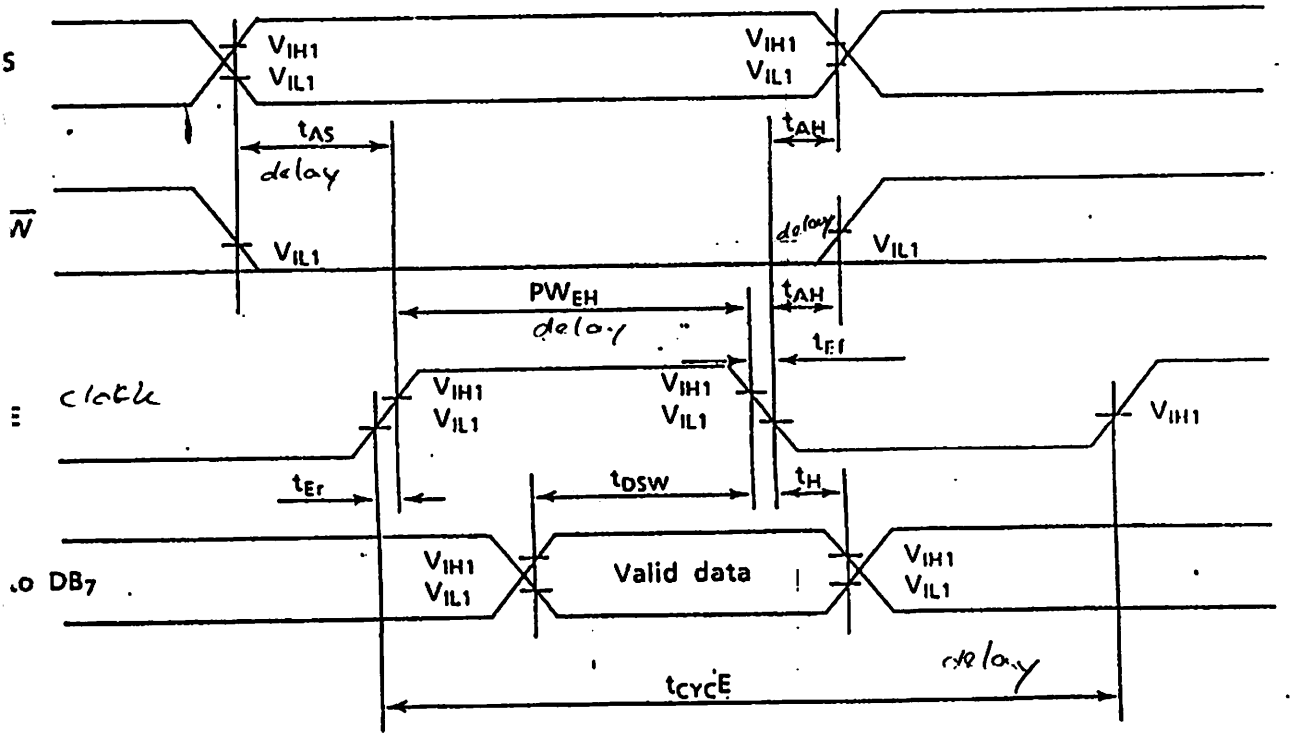


Figure 3 Data write from MPU to module

.2 Read timing characteristics

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		$t_{CYC}E$	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er}, t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$—E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data delay time		t_{DDR}	–	320	ns
Data hold time		t_{H}	20	–	ns

ead operation

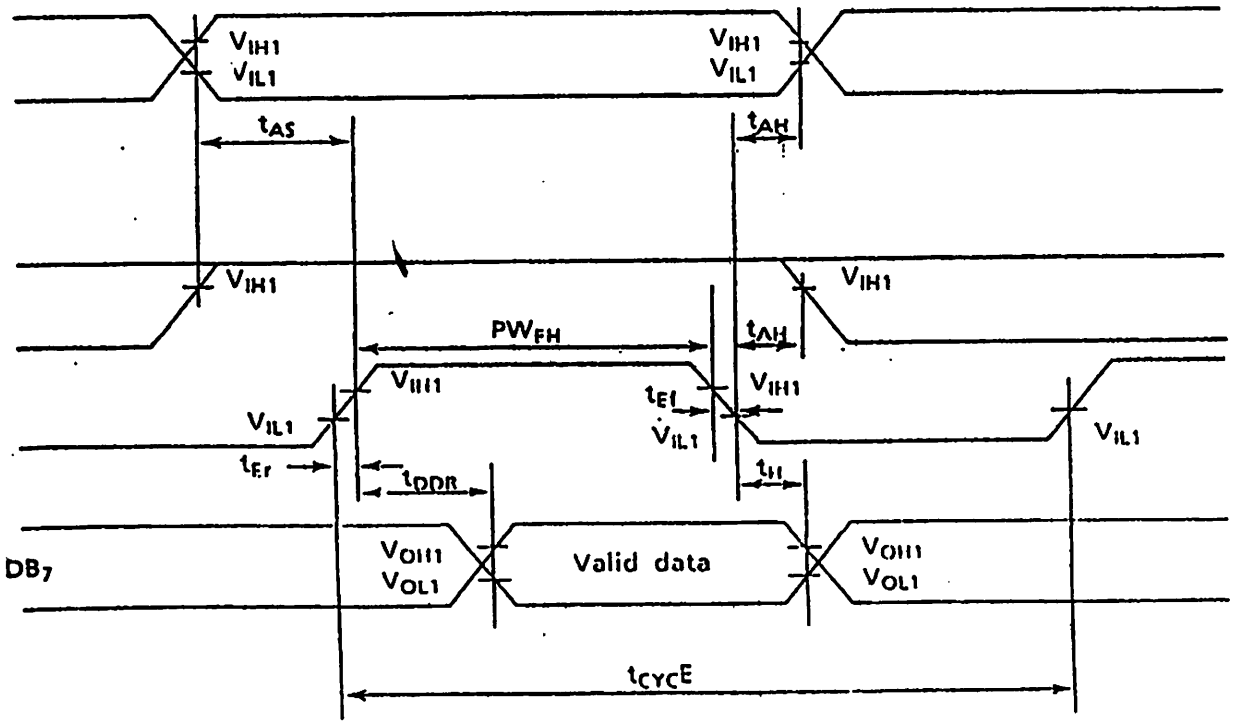


Figure 4 Data read from module to MPU

Instruction Outline

Table 5 List of instructions

Instruction	Code										Function	Execution time
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
lay clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns cursor to home position (address 0)	1.64 ms
or Home	0	0	0	0	0	0	0	0	1	•	Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change.	1.64 ms
y Mode Set	0	0	0	0	0	0	0	1	I/D 1	S 0	Sets direction of cursor movement and whether display will be shifted when data is written or read	40 µs
lay. ON / OFF trol	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)	40 µs
sor/Display Shift	0	0	0	0	0	1	S/C	R/L	•	•	Moves cursor and shifts display without changing DD RAM contents	40 µs
ction Set	0	0	0	0	1	DL	1	•	•	•	Sets interface data length (DL)	40 µs
RAM Address	0	0	0	1	A_{CG}						Sets CG RAM address to start transmitting or receiving CG RAM data	40 µs
RAM Address	0	0	1	A_{DD}							Sets DD RAM address to start transmitting or receiving DD RAM data	40 µs
Address Read	0	1	BF	AC							Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM)	0 µs
ta Write to CG M or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	40 µs
ta Read from RAM or DD M	1	1	Read Data								Reads data from DD RAM or CG RAM	40 µs

valid bit
CG RAM address
DD RAM address

I/D = 1 : Increment
I/D = 0 : Decrement

S = 1 : Display shift
S = 0 : No display shift

D = 1 : Display ON
D = 0 : Display OFF

C = 1 : Cursor ON
C = 0 : Cursor OFF

B = 1 : Blink ON
B = 0 : Blink OFF

S/C = 1 : Display shift
S/C = 0 : Cursor movement

R/L = 1 : Right shift
R/L = 0 : Left shift

DL = 1 : 8 bits
DL = 0 : 4 bits

BF = 1 : Internal operation in progress
BF = 0 : Instruction can be accepted

ruction Details

)isplay Clear

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Display Clear clears all display and returns cursor to home position (address 0).

Space code 20 (hexadecimal) is written into all the addresses of DD RAM, and DD RAM address 0 is set to the AC. If shifted, the display returns to the original position. After execution of the Display Clear instruction, the entry mode is incremented.

Note : When executing the Display Clear instruction, follow the restrictions listed in Table 6.

Cursor Home

	RS	R/$\overline{W}$	DB_7							DB_0	
Code	0	0	0	0	0	0	0	0	1.	*	* : Invalid bit

Cursor Home returns cursor to home position (address 0).

DD RAM address 0 is set to the AC. The cursor returns to the home position. If shifted, the display returns to the original position. The DD RAM contents do not change. If the cursor or blinking is ON, it returns to the left side.

Note : When executing the Cursor Home instruction, follow the restrictions listed in Table 6.

Table 6 Restrictions on execution of Display Clear and Cursor Home instructions

Conditions of use	Restrictions
When executing the Display Clear or Cursor Home instruction when the display is shifted (after execution of Display Shift instruction)	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{osc}$* second after the first execution. Example: 1.5 ms, 3 ms, 4.5 ms for f_{osc} = 270 kHz *f_{osc}: Oscillation frequency
When 23_H, 27_H, 63_H, or 67_H is used as a DD RAM address to execute Cursor Home instruction	Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)

Entry Mode Set

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry Mode Set sets the direction of cursor movement and whether display will be shifted.

I/D : The DD RAM address is incremented or decremented by one when a character code is written into or read from DD RAM. This is also true for writing into or reading from CG RAM.

When I/D = 1, the address is incremented by one and the cursor or blink moves to the right.

When I/D = 0, the address is decremented by one and the cursor or blink moves to the left.

S : If S = 1, the entire display is shifted either to the right or left for writing into DD RAM. The cursor position does not change, only the display moves. There is no display shift for reading from DD RAM.

When S = 1 and I/D = 1, the display shifts to the left.
When S = 1 and I/D = 0, the display shifts to the right.

If S = 0, the display does not shift.

Display ON/OFF Control

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display ON/OFF Control turns the total display and the cursor ON and OFF, and makes the cursor position start blinking. Cursor ON/OFF and blinking is done at the column indicated by the specified DD RAM address by the AC.

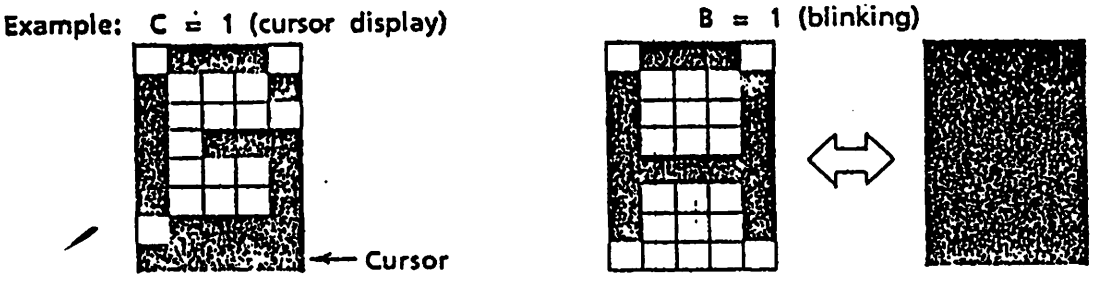
D : When D = 1, the display is turned ON.
When D = 0, the display is turned OFF.
If D = 0 is used, display data remains in DD RAM. Change 0 to 1 to display data.

C : When C = 1, the cursor is displayed.
When C = 0, the cursor is not displayed.

The cursor is displayed in the dot line below the 5 x 7 dot-matrix character fonts. If the cursor is OFF, display data is written into DD RAM in the order specified by I/D.

B : When B = 1, the character at the cursor position starts blinking.
When B = 0, it does not blink.

For blinking, all-black dots and the character are switched about every 0.4 seconds. The cursor and blinking can be set at the same time.



Cursor/Display Shift

	RS	R/$\overline{W}$	DB_7						DB_0	
Code	0	0	0	0	0	1	S/C	R/L	*	*

* :Invalid bit

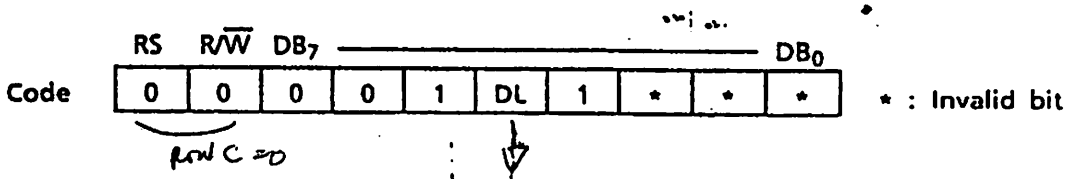
Cursor/Display Shift moves the cursor and shifts the display without changing the DD RAM contents.

The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. Since the DD RAM capacity is 40-character and two lines, the cursor is shifted from digit 40 of line 1 to digit 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. Therefore, the display pattern of line 2 is not shifted to line 1.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one).
0	1	The cursor position is shifted to the right (the AC increments one).
1	0	The entire display is shifted to the left with the cursor.
1	1	The entire display is shifted to the right with the cursor.

Note: If only display shift is done, the AC contents do not change.

Function Set



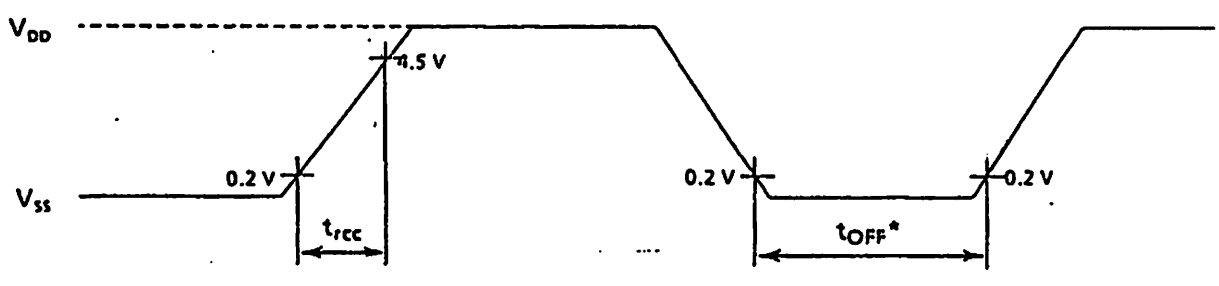
Function Set sets the interface data length.

DL : Interface data length
When DL = 1, the data length is set at eight bits (DB_7 to DB_0).
When DL = 0, the data length is set at four bits (DB_7 to DB_4).
The upper four bits are transferred first, then the lower four bits follow.

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

Remarks: Initialization

The system is automatically initialized at power-on if the following power supply conditions are satisfied.



0.1 ms ≤ t_{rcc} ≤ 10 ms $\qquad$ t_{OFF} ≥ 1 ms

*t_{OFF}: Time when power supply is OFF if cut instantaneously or turned ON and OFF repeatedly

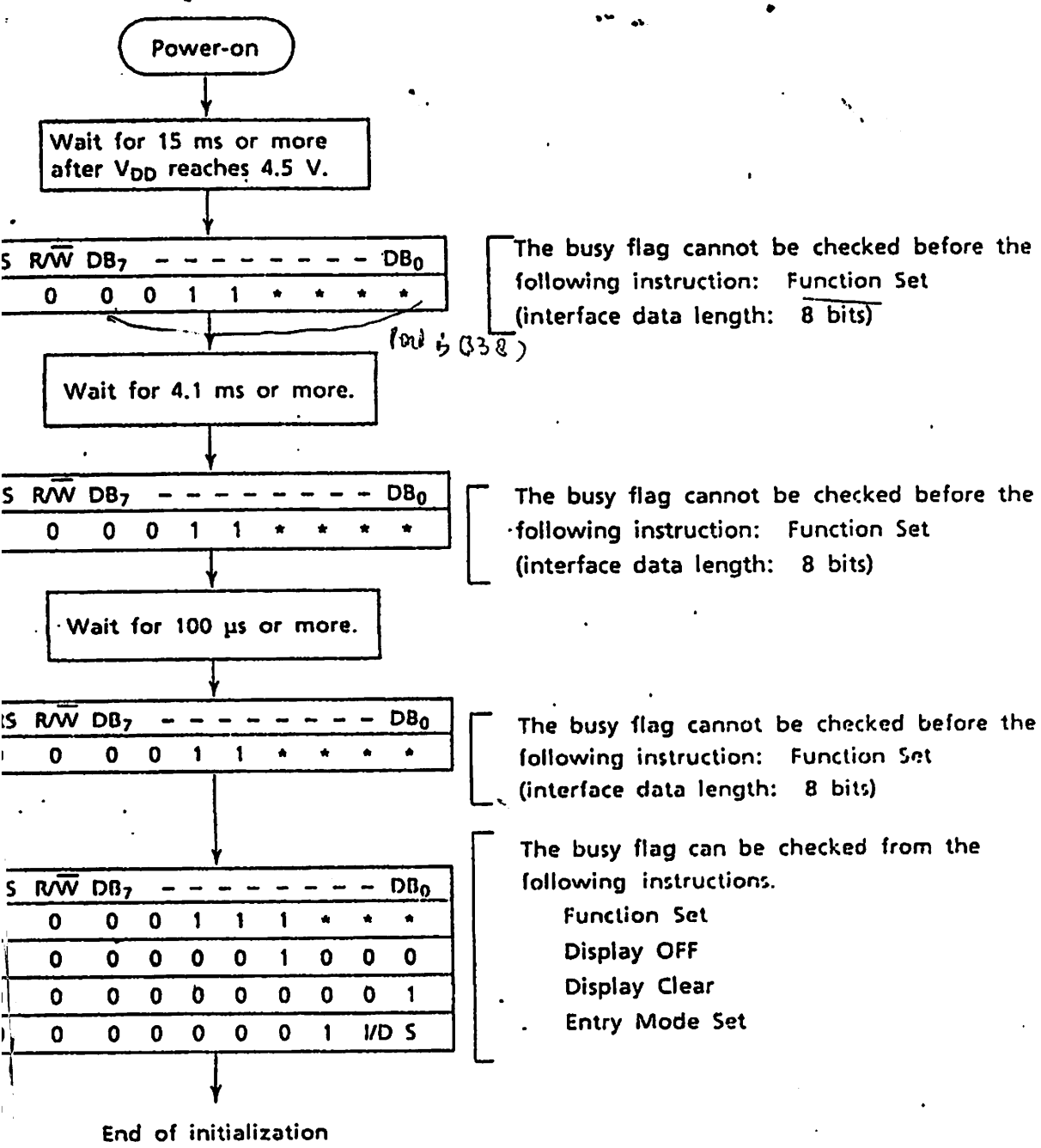
e following instructions are executed for initialization.

- 5 x 7 dot-matrix character font: 1/8 duty
- Display clear
- Function Set — DL = 1: Interface data length: 8 bits
- Display ON/OFF Control — D = 0: Display OFF; C = 0: Cursor OFF; B = 0: Blink OFF
- Entry mode — I/O = 1: Increment; S = 0: No display shift

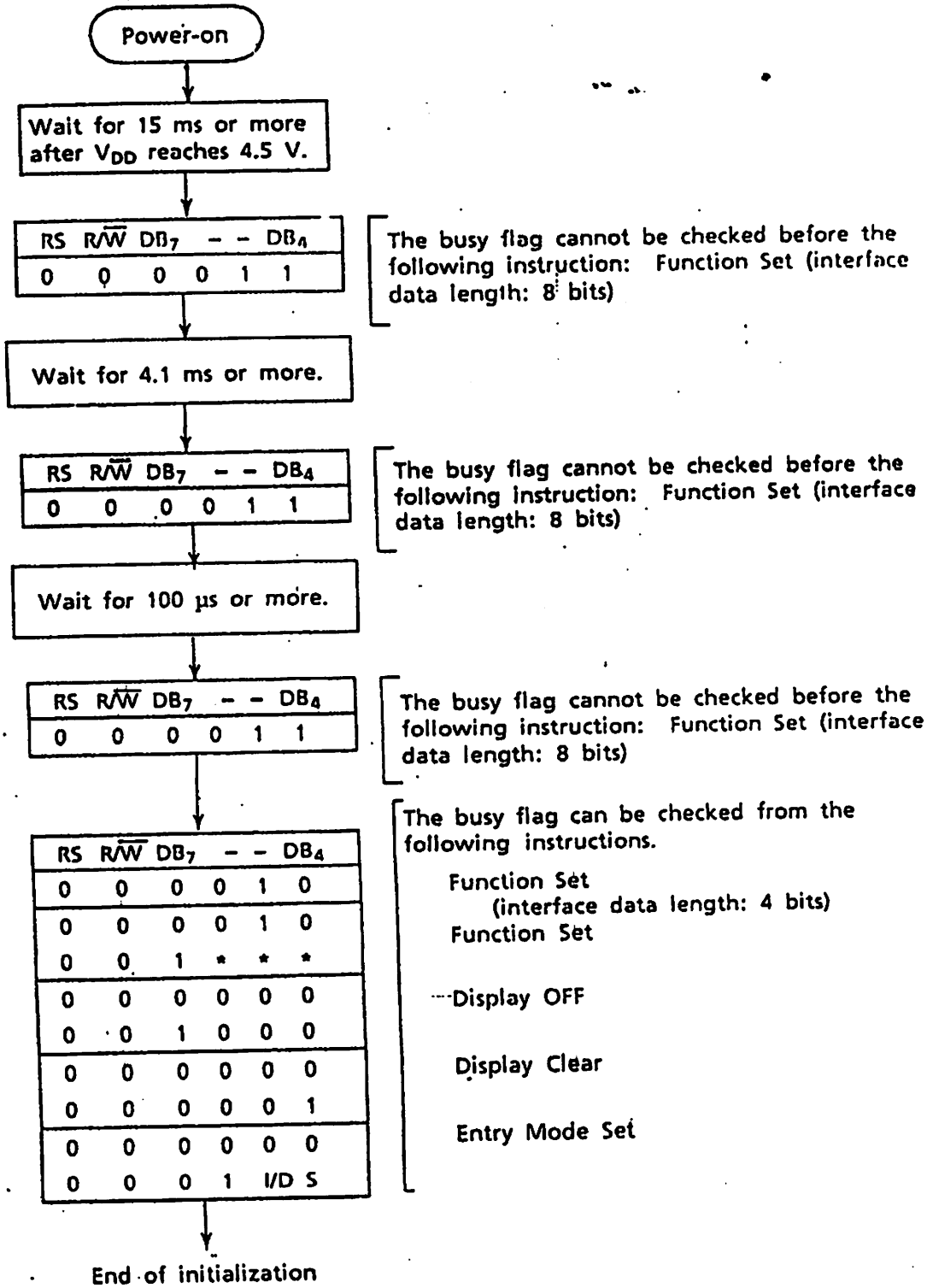
Since the condition is not suitable for the M1632, further function setting is ecessary.

If automatic initialization is not executed because the above power supply onditions are not satisfied, use the instruction from next page on.

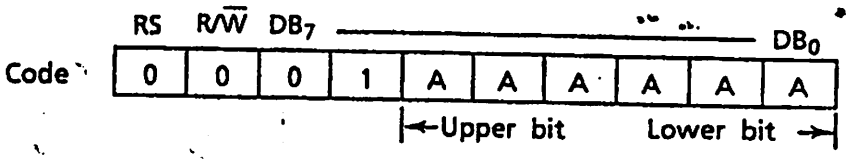
Interface data length : Eight bits



nterface data length: Four bits

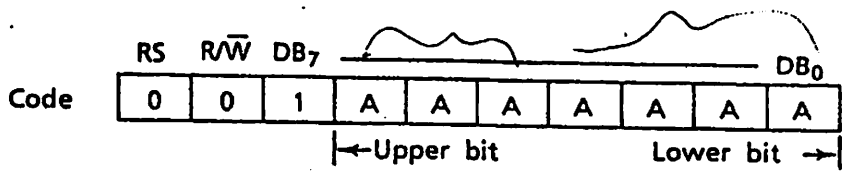


CG RAM Address Set



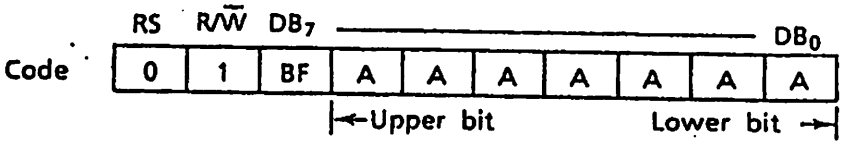
CG RAM addresses expressed as binary AAAAAA are set to the AC. Then data in CG RAM is written from or read to the MPU.

DD RAM Address Set



DD RAM addresses expressed as binary AAAAAAA are set to the AC. Then data n DD RAM is written from or read to the MPU. The addresses used for display in ine 1 (AAAAAAA) are 00_H to 27_H and those for line 2 (AAAAAAA) are 40_H to 67_H.

lusy Flag/Address Read



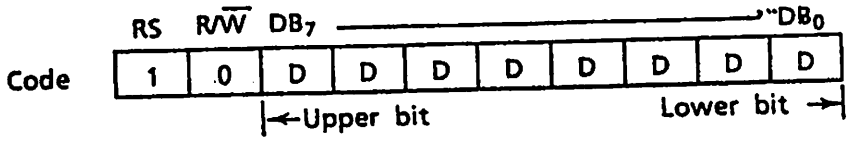
The BF signal is read out, indicating that the module is working internally because the previous instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

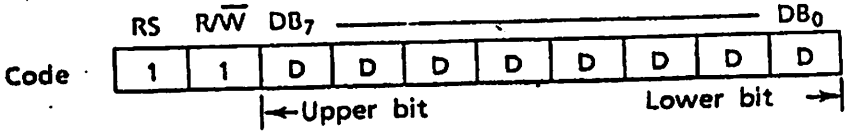
Therefore, make sure that BF = 0 before writing the next instruction. The AC alues of binary AAAAAAA are read out at the same time as reading the busy flag. he AC addresses are used for both CG RAM and DD RAM but the address set :fore execution of the instruction determines which address is to be used.

ata Write to CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is written into CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

Data Read from CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. In addition, either instruction (7) or (8) must be executed immediately before this instruction. If no address set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.
After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

Note : The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

Correct data is read out under the following conditions.

- An address set instruction is executed immediately before readout.
- For DD RAM, the Cursor Shift instruction is executed immediately before readout.
- The second, or later, instruction is executed in consecutive execution of read instructions.

Examples of Instruction Use

Interface data length: Eight bits

Instruction	Display	Operation
Power-on RS: —, R/W: —, DB_7 —— DB_0: —		The built-in reset circuit initializes the module.
Function Set ✓ RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 1 1 1 * * *		The interface data length is set to 8 bits. The character format becomes 5 x 7 dot-matrix at 1/16 duty cycle.
Display ON/OFF Control RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 0 0 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
Entry Mode Set RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 0 0 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 0 1 1 0 0	L_	L is written. The AC is incremented by one and the cursor shifts to the right.
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 0 0 0 1 1	LC_	C is written.
⋮	⋮	
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 0 1 1 0 0 1 0	LCD MODULE M1632	2 is written in digit 16. Cursor disappears.

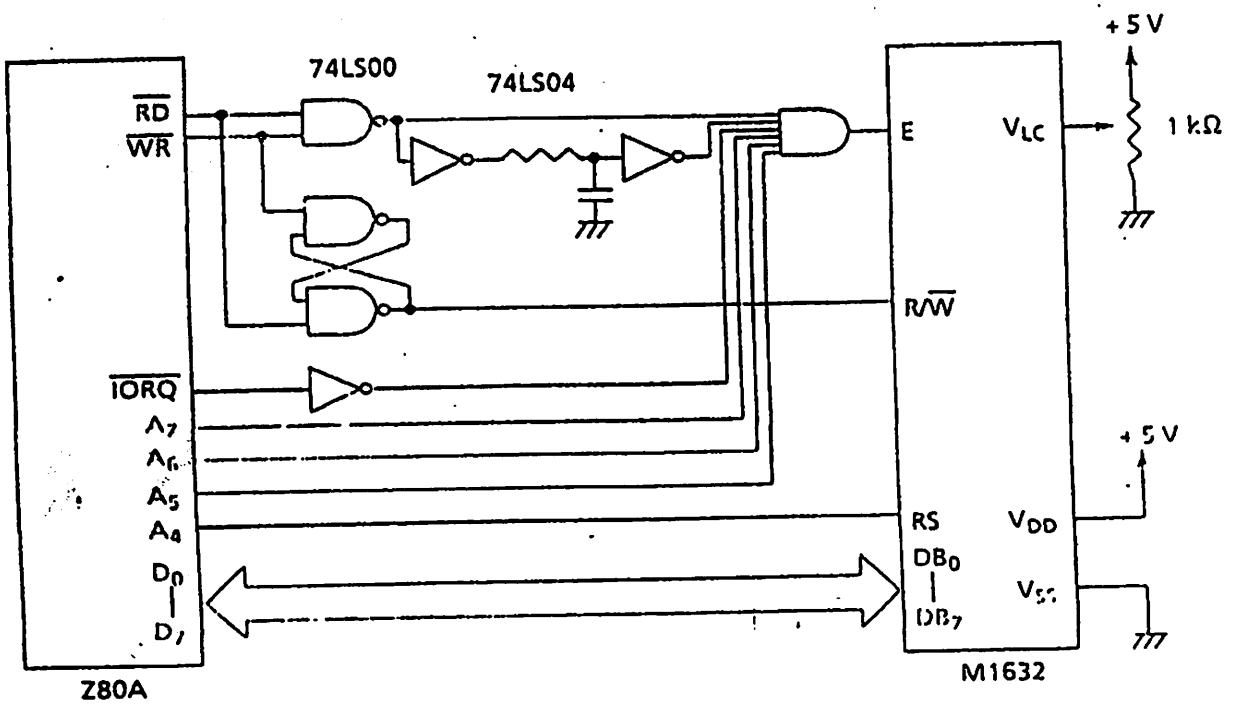
Instruction	Display	Operation
DD RAM address set RS: 0, R/W: 0, DB_7 —— DB_0: 1 1 0 0 0 0 0 0	LCD MODULE M1632 _	The DD RAM address is set so that the cursor appears at digit 1 of line 2.
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 0 1 1 0 0 0 1	LCD MODULE M1632 1_	1 is written.
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 0 1 1 0 1 1 0	LCD MODULE M1632 16_	6 is written.
⋮	⋮	
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 1 0 0 1 1	LCD MODULE M1632 16DIGITS,2LINES	S is written.
DD RAM address set RS: 0, R/W: 0, DB_7 —— DB_0: 1 0 0 0 0 0 0 0	LCD MODULE M1632 16DIGITS,2LINES	The cursor returns to the home position.
Display clear RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 0 0 0 0 0 1	_	All the display disappears and the cursor remains at the home position.
⋮	⋮	

Interface data length: Four bits

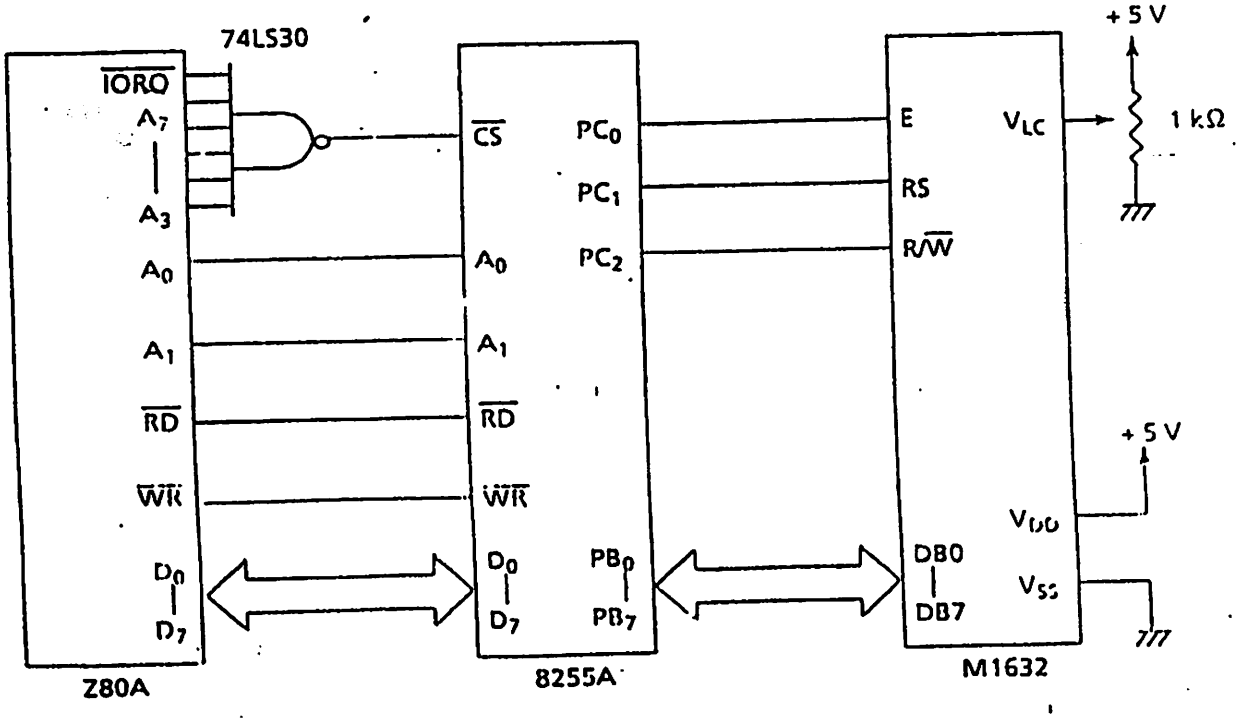
Instruction	Display	Operation
Power-on RS | R/W | DB7 — DB4		The built-in reset circuit initializes the module.
Function Set RS | R/W | DB7 — DB4 0 | 0 | 0 0 1 0		Four-bit operation mode is set. *Eight-bit operation mode is set by initialization, and the instruction is executed only once.
Function Set RS | R/W | DB7 — DB4 0 | 0 | 0 0 1 0 0 | 0 | 1 * * *		The 4-bit operation mode, 1/16 duty cycle, and 5 x 7 dot-matrix character format are selected. Then 4-bit operation mode starts.
Display ON/OFF Control RS | R/W | DB7 — DB4 0 | 0 | 0 0 0 0 0 | 0 | 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
Entry Mode Set RS | R/W | DB7 — DB4 0 | 0 | 0 0 0 0 0 | 0 | 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
Write to CG RAM or DD RAM. RS | R/W | DB7 — DB4 1 | 0 | 0 1 0 0 1 | 0 | 1 1 0 0	L_	L is written, the AC is incremented by one and the cursor shifts to the right.

PU Connection Diagrams

1 Z80A



.2 Z80A and 8255A



GlobalOptoisolator™

VDE	UL	CSA	SETI	SEMKO	DEMKO	NEMKO	BABT

# **MOC3021**
[IFT = 15 mA Max]
# **MOC3022**
[IFT = 10 mA Max]
# **MOC3023***
[IFT = 5 mA Max]

*Motorola Preferred Device

Pin DIP Random-Phase toisolators Triac Driver Output
Volts Peak)

MOC3020 Series consists of gallium arsenide infrared emitting diodes, ly coupled to a silicon bilateral switch.

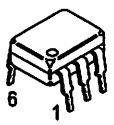
order devices that are tested and marked per VDE 0884 requirements, the fix "V" must be included at end of part number. VDE 0884 is a test option.

/ are designed for applications requiring isolated triac triggering.

nmended for 115/240 Vac(rms) Applications:

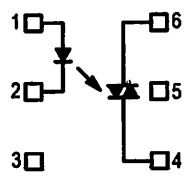
- enoid/Valve Controls
- np Ballasts
- rfacing Microprocessors to 115 Vac Peripherals
- or Controls
- Static ac Power Switch
- Solid State Relays
- Incandescent Lamp Dimmers

STYLE 6 PLASTIC



STANDARD THRU HOLE
CASE 730A–04

SCHEMATIC



1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE
   DO NOT CONNECT
6. MAIN TERMINAL

IUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RED EMITTING DIODE			
se Voltage	V_R	3	Volts
ard Current — Continuous	I_F	60	mA
Power Dissipation @ T_A = 25°C gligible Power in Triac Driver e above 25°C	P_D	100 1.33	mW mW/°C
T DRIVER			
tate Output Terminal Voltage	V_{DRM}	400	Volts
Repetitive Surge Current W = 1 ms, 120 pps)	I_{TSM}	1	A
Power Dissipation @ T_A = 25°C rate above 25°C	P_D	300 4	mW mW/°C
DEVICE			
tion Surge Voltage(1) eak ac Voltage, 60 Hz, 1 Second Duration)	V_{ISO}	7500	Vac(pk)
Power Dissipation @ T_A = 25°C rate above 25°C	P_D	330 4.4	mW mW/°C
ion Temperature Range	T_J	−40 to +100	°C
ent Operating Temperature Range(2)	T_A	−40 to +85	°C
ge Temperature Range(2)	T_{stg}	−40 to +150	°C
ering Temperature (10 s)	T_L	260	°C

tion surge voltage, V_{ISO}, is an internal device dielectric breakdown rating.
this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.
r to Quality and Reliability Section in Opto Data Book for information on test conditions.

d devices are Motorola recommended choices for future use and best overall value.
ptoisolator is a trademark of Motorola, Inc.

MOTOROLA

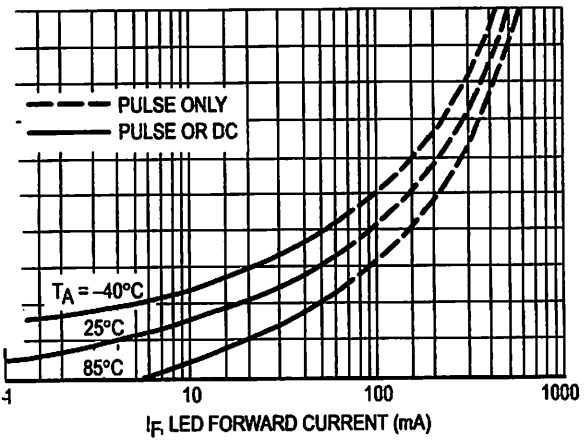
TRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
LED						
se Leakage Current = 3 V)		I_R	—	0.05	100	μA
ard Voltage = 10 mA)		V_F	—	1.15	1.5	Volts
IT DETECTOR (I_F = 0 unless otherwise noted)						
Blocking Current, Either Direction ited V_{DRM}(1))		I_{DRM}	—	10	100	nA
On–State Voltage, Either Direction M = 100 mA Peak)		V_{TM}	—	1.8	3	Volts
al Rate of Rise of Off–State Voltage (Figure 7, Note 2)		dv/dt	—	10	—	V/μs
LED						
Trigger Current, Current Required to Latch Output ain Terminal Voltage = 3 V(3))	MOC3021 MOC3022 MOC3023	I_{FT}	— — —	8 — —	15 10 5	mA
ing Current, Either Direction		I_H	—	100	—	μA

voltage must be applied within dv/dt rating.
is static dv/dt. See Figure 7 for test circuit. Commutating dv/dt is a function of the load–driving thyristor(s) only.
levices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max (15 mA for MOC3021, 10 mA for MOC3022, 5 mA for MOC3023) and absolute max I_F (60 mA).

TYPICAL ELECTRICAL CHARACTERISTICS

T_A = 25°C



ure 1. LED Forward Voltage versus Forward Current

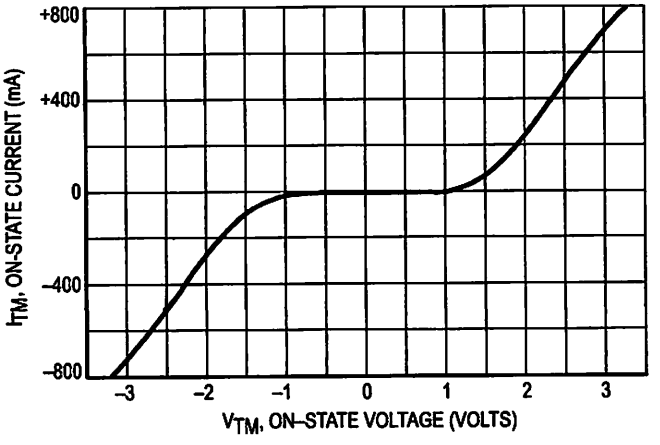


Figure 2. On–State Characteristics

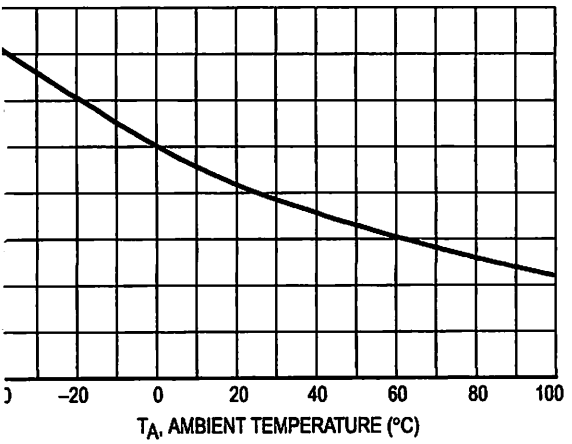


Figure 3. Trigger Current versus Temperature

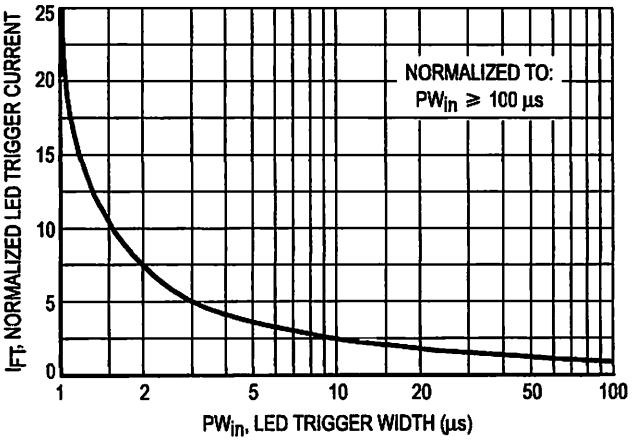


Figure 4. LED Current Required to Trigger versus LED Pulse Width

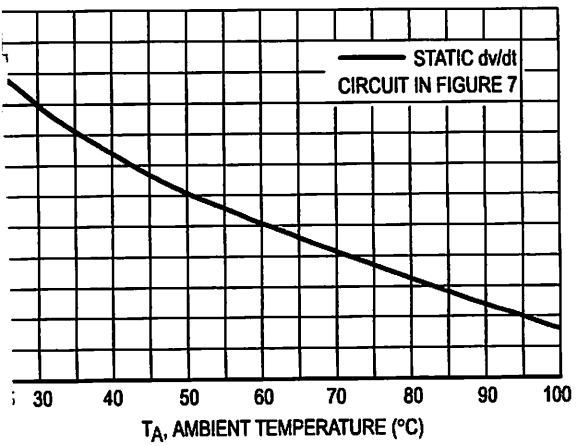


Figure 5. dv/dt versus Temperature

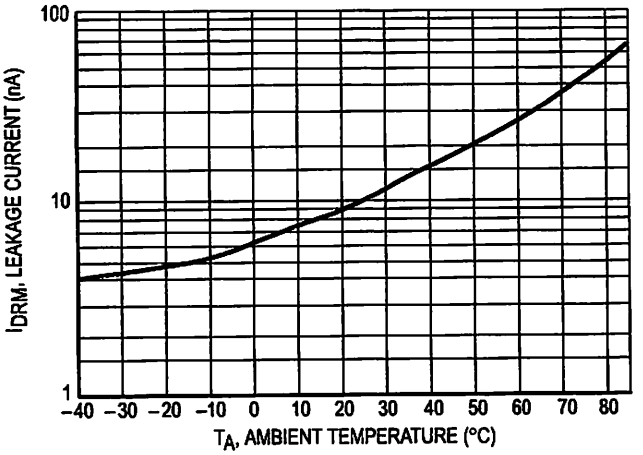
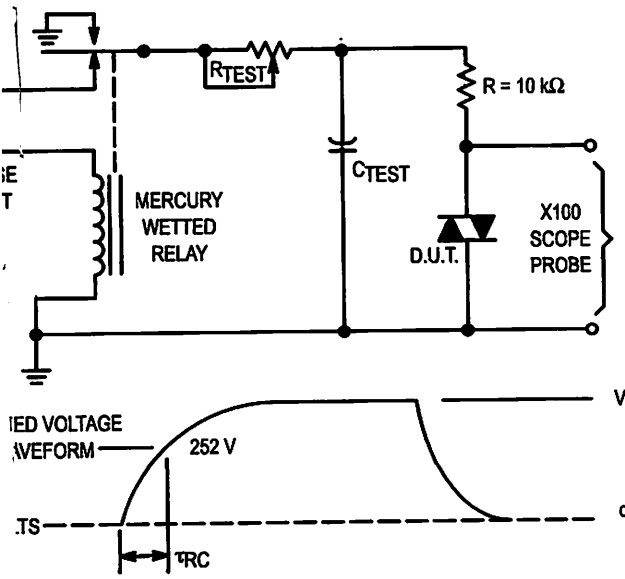
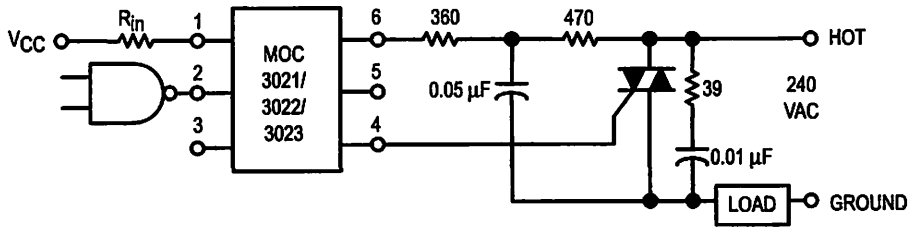


Figure 6. Leakage Current, I_{DRM} versus Temperature



1. The mercury wetted relay provides a high speed repeated pulse to the D.U.T.
2. 100x scope probes are used, to allow high speeds and voltages.
3. The worst–case condition for static dv/dt is established by triggering the D.U.T. with a normal LED input current, then removing the current. The variable R_{TEST} allows the dv/dt to be gradually increased until the D.U.T. continues to trigger in response to the applied voltage pulse, even after the LED current has been removed. The dv/dt is then decreased until the D.U.T. stops triggering. τ_{RC} is measured at this point and recorded.

Figure 7. Static dv/dt Test Circuit



ɔtoisolator should not be used to drive a load directly. It is in- l to be a trigger device only.

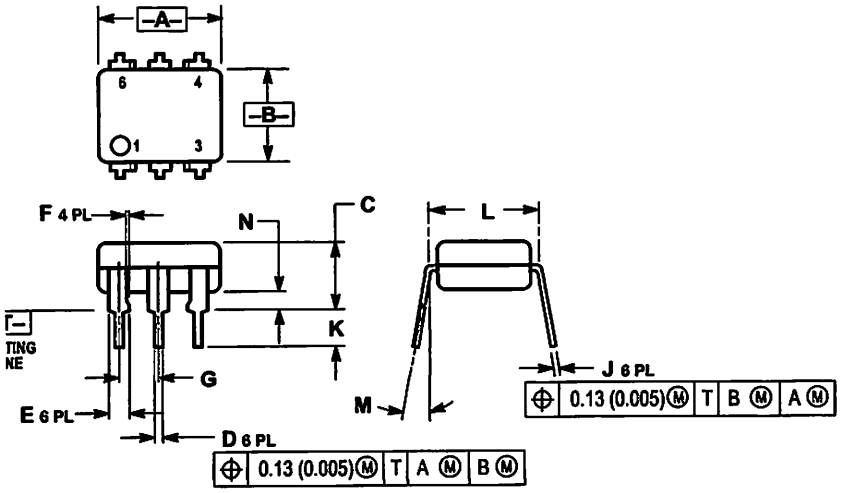
ıal information on the use of optically coupled triac s available in Application Note AN–780A.

In this circuit the "hot" side of the line is switched and the load connected to the cold or ground side.

The 39 ohm resistor and 0.01 µF capacitor are for snubbing of the triac, and the 470 ohm resistor and 0.05 µF capacitor are for snubbing the coupler. These components may or may not be necessary depending upon the particular triac and load used.

Figure 8. Typical Application Circuit

PACKAGE DIMENSIONS

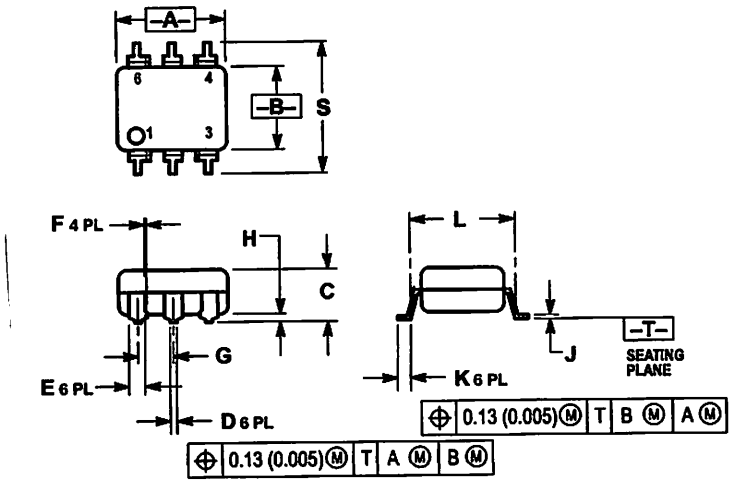


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.015	0.100	0.38	2.54

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE
6. MAIN TERMINAL

CASE 730A–04
ISSUE G



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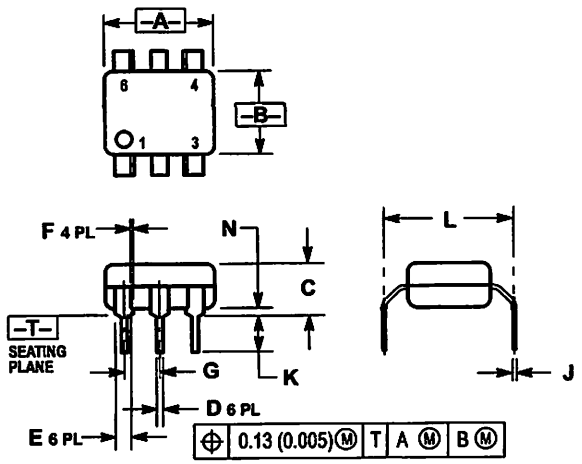
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
H	0.020	0.025	0.51	0.63
J	0.008	0.012	0.20	0.30
K	0.006	0.035	0.16	0.88
L	0.320 BSC		8.13 BSC	
S	0.332	0.390	8.43	9.90

***Consult factory for leadform option availability**

CASE 730C–04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.400	0.425	10.16	10.80
N	0.015	0.040	0.38	1.02

***Consult factory for leadform option availability**

CASE 730D–05
ISSUE D

›each us:
JROPE: Motorola Literature Distribution;
20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
ET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

AL DESCRIPTION

ssivated triacs in a plastic , intended for use in ons requiring high nal transient and blocking capability and high thermal performance. Typical ons include motor control, l and domestic lighting, and static switching.

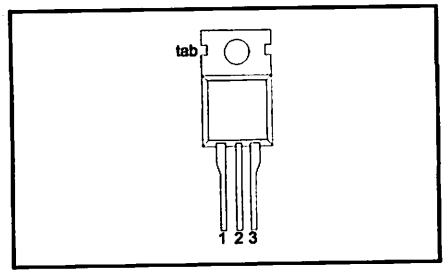
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BT136-	500	600	800	
	BT136-	500F	600F	800F	
	BT136-	500G	600G	800G	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	4	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	25	A

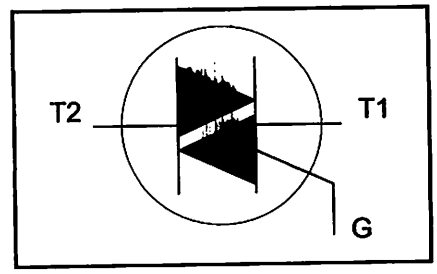
IG - TO220AB

DESCRIPTION
main terminal 1
main terminal 2
gate
main terminal 2

PIN CONFIGURATION



SYMBOL

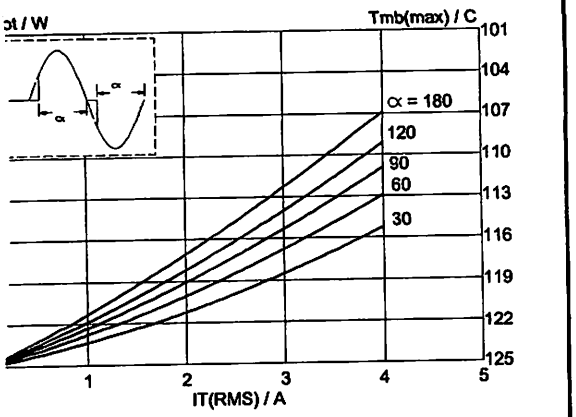


NG VALUES

values in accordance with the Absolute Maximum System (IEC 134).

OL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500	-600	-800	
	Repetitive peak off-state voltages		-	500[1]	600[1]	800	V
	RMS on-state current	full sine wave; $T_{mb} \leq 107$ °C	-		4		A
	Non-repetitive peak on-state current	full sine wave; $T_j = 25$ °C prior to surge					
		t = 20 ms	-		25		A
		t = 16.7 ms	-		27		A
	I^2t for fusing	t = 10 ms	-		3.1		A^2s
	Repetitive rate of rise of on-state current after triggering	I_{TM} = 6 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs					
		T2+ G+	-		50		A/µs
		T2+ G-	-		50		A/µs
		T2- G-	-		50		A/µs
		T2- G+	-		10		A/µs
	Peak gate current		-		2		A
	Peak gate voltage		-		5		V
	Peak gate power		-		5		W
	Average gate power	over any 20 ms period	-		0.5		W
	Storage temperature		-40		150		°C
	Operating junction temperature		-		125		°C

ugh not recommended, off-state voltages up to 800V may be applied without damage, but the triac may to the on-state. The rate of rise of current should not exceed 3 A/µs.



Maximum on-state dissipation, P_{tot}, versus rms e current, $I_{T(RMS)}$, where α = conduction angle.

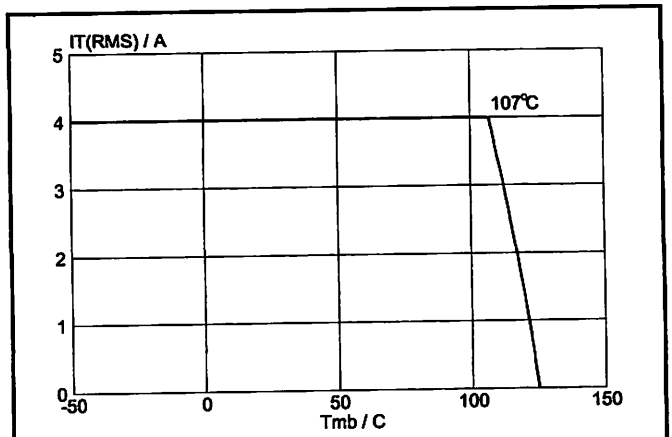
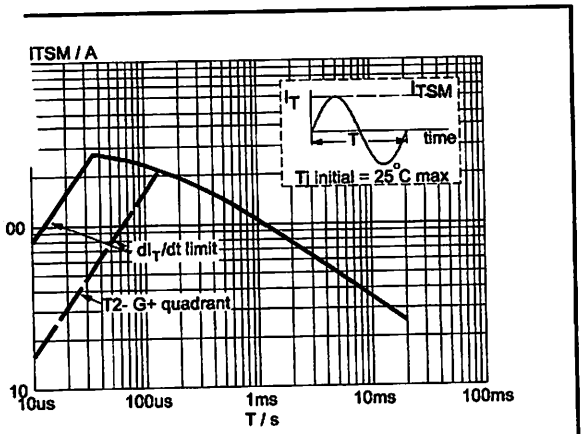


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.



2. Maximum permissible non-repetitive peak -state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

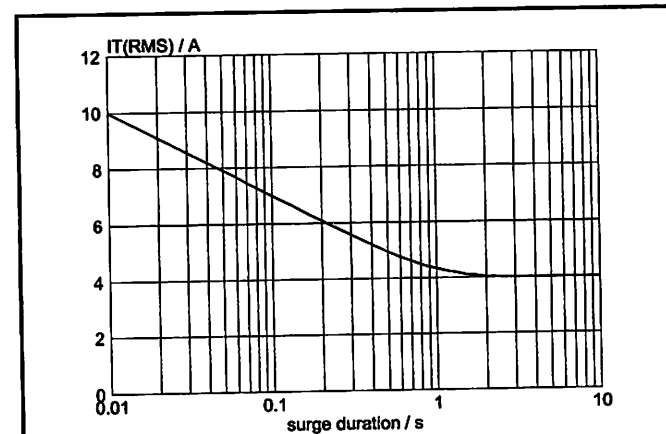
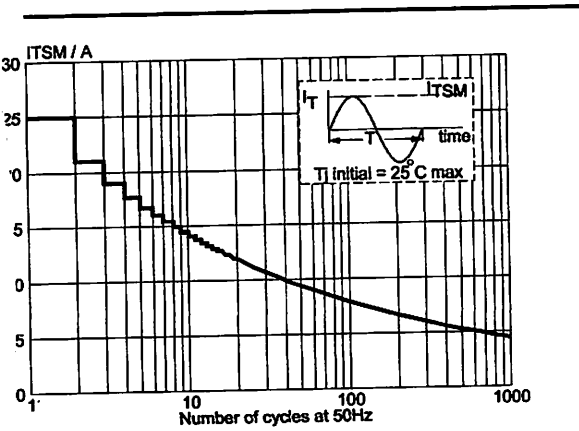


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.



.3. Maximum permissible non-repetitive peak state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

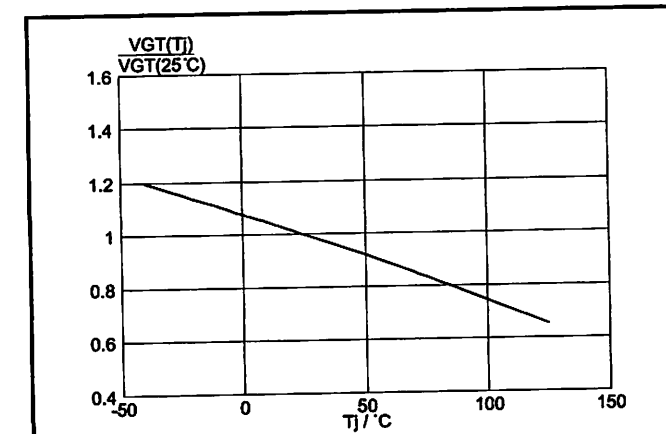


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature T_j.

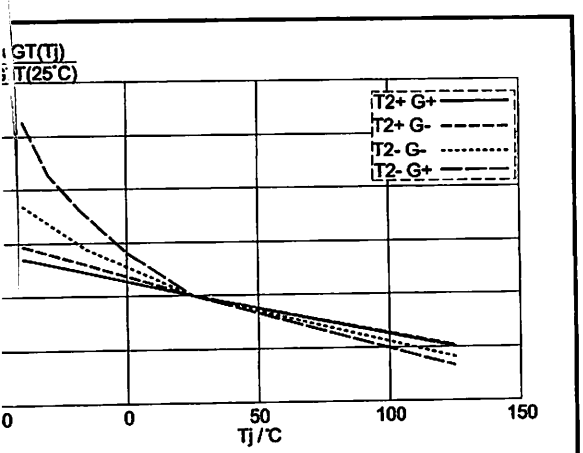
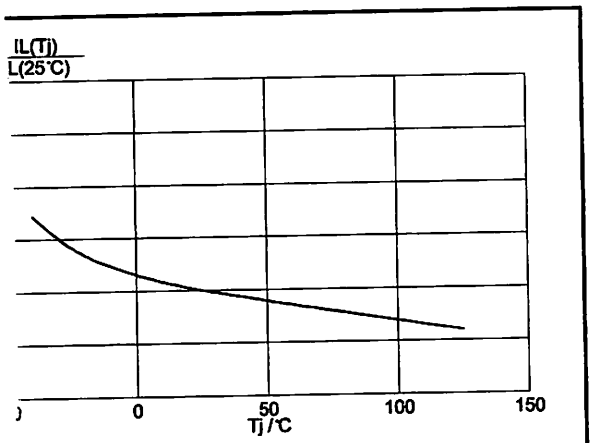
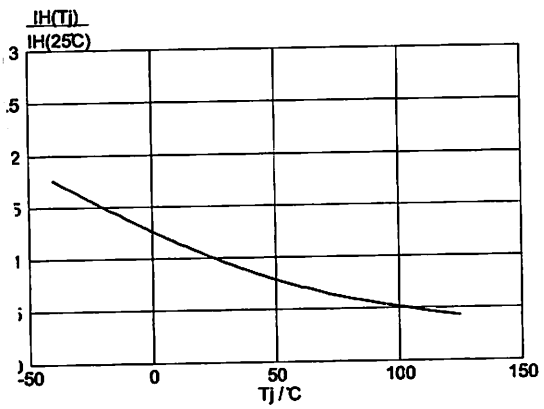


Fig.7. Normalised gate trigger current $(T_j)/ I_{GT}(25°C)$, versus junction temperature T_j.



8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature T_j.



9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature T_j.

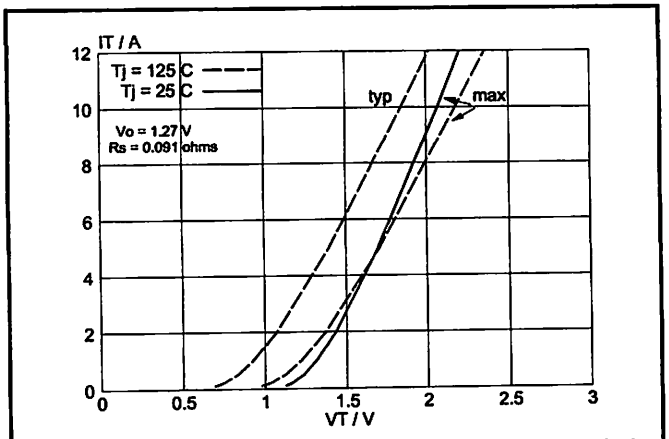


Fig.10. Typical and maximum on-state characteristic.

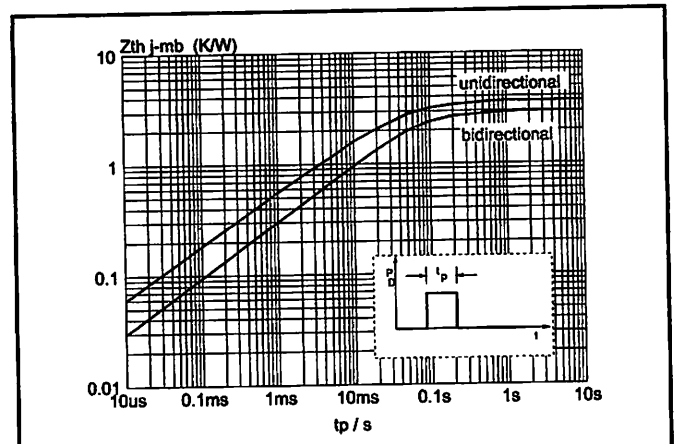


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

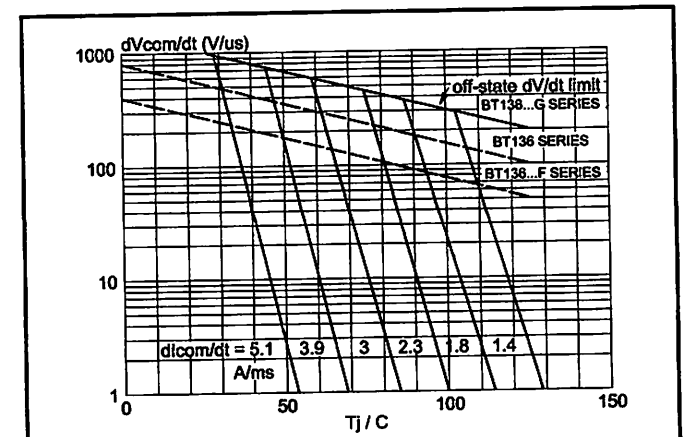


Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation dI_T/dt.

IANICAL DATA

ɪsions in mm

'ass: 2 g

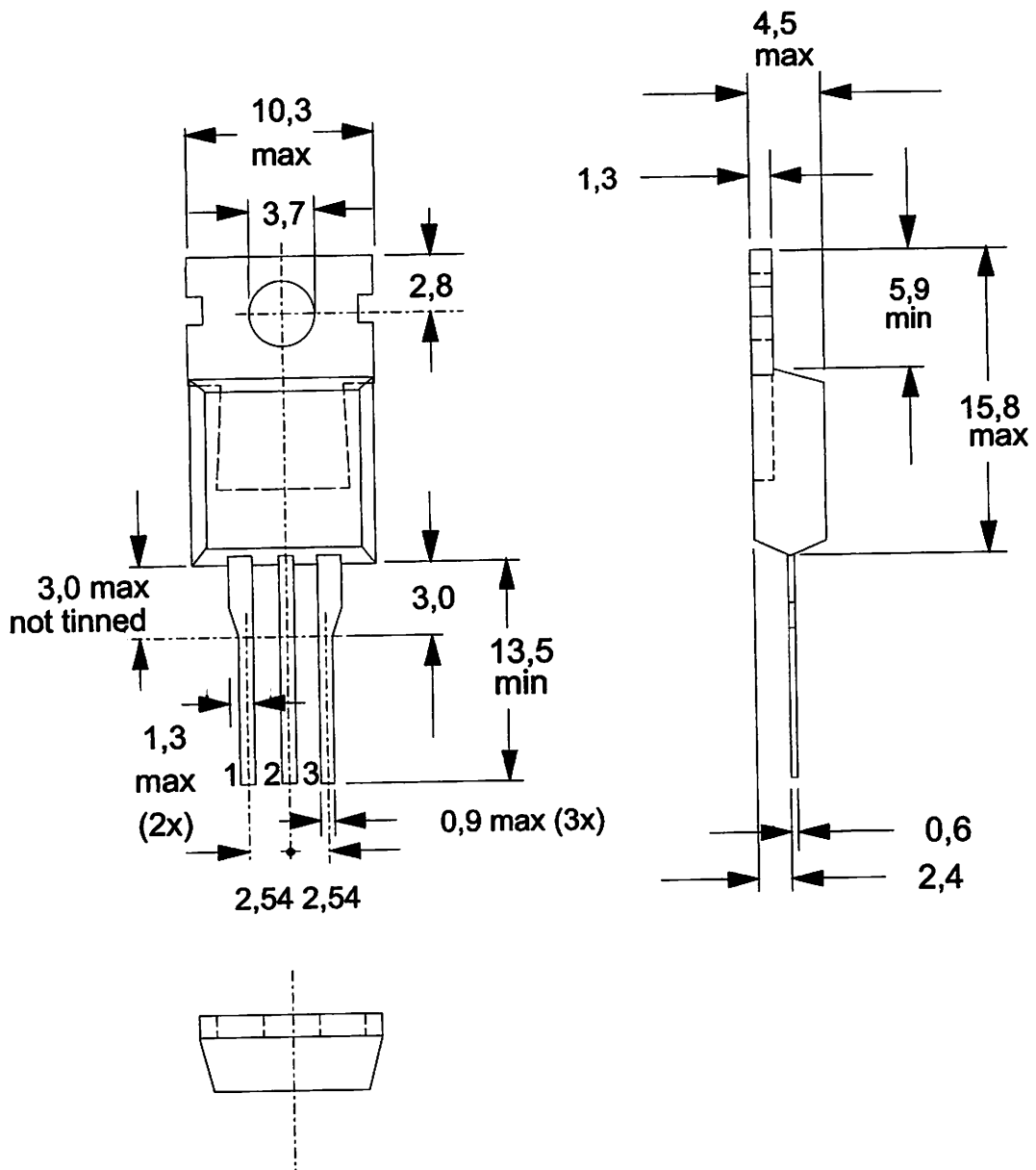


Fig.13. TO220AB; pin 2 connected to mounting base.

ɜr to mounting instructions for TO220 envelopes.
xy meets UL94 V0 at 1/8".

IITIONS

sheet status	
tive specification	This data sheet contains target or goal specifications for product development.
inary specification	This data sheet contains preliminary data; supplementary data may be published later.
of specification	This data sheet contains final product specifications.

ing values

ng values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one re of the limiting values may cause permanent damage to the device. These are stress ratings only and tion of the device at these or at any other conditions above those given in the Characteristics sections of pecification is not implied. Exposure to limiting values for extended periods may affect device reliability.

cation information

Where application information is given, it is advisory and does not form part of the specification.

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