INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S -1
KONSENTRASI ELEKTRONIKA

SKRIPSI

PERANCANGAN DAN PEMBUATAN SISTEM KONTROL *TRAFFIC LIGHT* JARAK JAUH DENGAN MENGGUNAKAN RADIO HT (*HANDY TALKY*)

Disusun Oleh **:**
ARDHIATAMA KUSUMAPUTRA
NIM. 02.17.056

MARET 2007

LEMBAR PERSETUJUAN

PERANCANGAN DAN PEMBUATAN
SISTEM KONTROL TRAFFIC LIGHT JARAK JAUH
DENGAN MENGGUNAKAN RADIO HT (HANDY TALKY)

SKRIPSI

Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik
Program Studi Teknik Elektronika

Disusun Oleh :

ARDHIATAMA KUSUMAPUTRA

NIM : 02.17.056

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Judul Skripsi	:	**Perancangan Dan Pembuatan Sistem Kontrol Traffic Light Dengan Menggunakan Radio HT (Handy Talky)**

Dipertahankan dihadapan Team Penguji Skripsi Jenjang Strata Satu (S-1) Pada :

Hari	:	**Sabtu**
Tanggal	:	**17 Maret 2007**
Dengan Nilai	:	**88,05 (A)**

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ABSTRAKSI

PERENCANAAN DAN PEMBUATAN SISTEM KONTROL *TRAFFIC LIGHT* DENGAN MENGGUNAKAN RADIO HT (*HANDY TALKY*)

(Ardhiatama Kusumaputra, 0217056, Teknik Elektro/Elektronika S-1)

(Dosen Pembimbing : Ir. Sidik Noertjahjono, MT)

Kata Kunci : Kontrol, Traffic Light, HT

Pada skripsi ini dirancang sebuah sistem kontrol *traffic light* jarak jauh dengan menggunakan radio HT (*Handy Talky*) dengan menitikberatkan permasalahan yang timbul pada kondisi *traffic light* yang tak tentu (*unusually condition*) dan pada waktu yang tak terduga, misal *ambulance* lewat (*emergency*), pejabat teras lewat, pemadam kebakaran atau konvoi kendaraan/demonstrasi. Perangkat HT (*Handy Talky*) digunakan sebagai alat pengesetan dari sistem kerja *traffic light* sesuai dengan permasalahan yang ada pada kondisi *traffic light* secara langsung dan di saat itu juga.

Kerja dari sistem kontrol *traffic light (sistem traffic light standalone)* ini adalah mengubah keadaan lampu lalu lintas disesuaikan dengan keadaan *traffic light*. Sistem yang telah ada, akan terhubung dengan sebuah HT (*Handy Talky*) penerima yang akan berfungsi sebagai media penerima perintah, sehingga keadaan lampu berubah sesuai dengan permasalahan yang timbul di saat itu secara cepat, tepat dan langsung. HT (*Handy Talky*) pengirim akan masuk terlebih dahulu pada sistem keamanan (*password)*, kemudian kirim kode akses sistem kontrol sesuai dengan kondisi *traffic light* yang dihadapi, khususnya keadaan darurat (*emergency*)

Pengujian SNR (*Signal to Noise Ratio*) rata-rata, didapat pada hasil pengukuran sebeasar 41,92 dB. Prosentase *error* dari sinyal input yang masuk ke dalam rangkaian DTMF *Decoder* paling besar adalah 0,41%. Waktu yang diperlukan untuk dapat mengendalikan sisten *traffic light* adalah ± 13 detik dengan jarak jangkauan ± 1000 m (dengan keadaan *power* HT adalah *low*).

KATA PENGANTAR

Assalamu'alaikum Wr. Wb

Segala puji syukur hanya milik Alloh SWT seru sekalian alam, karena atas hidayah dan rahmat-Nya, sehingga penyusunan Laporan Skripsi yang berjudul "Perancangan Dan Pembuatan Sistem Kontrol *Traffic Light* Jarak Jauh Dengan Menggunakan Radio HT (*Handy Talky*)" ini dapat diselesaikan dengan lancar. Skripsi ini merupakan persyaratan kelulusan Studi di Jurusan Teknik Elektro S-1 Konsentrasi Teknik Elektronika Institut Teknologi Nasional Malang dan untuk mencapai gelar Sarjana Teknik.

Keberhasilan peyelesaian Laporan Skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terima kasih kepada :

1. Bapak Prof. DR. Ir. Abraham Lomi, MSEE selaku Rektor Institut Teknologi Nasional Malang.
2. Bapak Ir. F. Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro S-1.
3. Bapak Ir. Sidik Noertjahjono, MT selaku Dosen Pembimbing.
4. Seluruh Dosen Institut Teknologi Nasional Malang, yang telah membantu.

5. Ayah dan Ibu serta saudara-saudara Kami yang telah memberikan do'a restu, dorongan dan semangat.
6. Rekan-rekan Elka 2 serta Instruktur di Laboratorium.
7. Semua pihak yang telah membantu dalam penyelesaian penyusunan skripsi ini.

Kami menyadari bahwa dalam penyusunan Laporan ini masih ada lebih dan kurangnya, untuk itu saran dan kritik yang akan Kami terima dengan senang hati dan penghargaan yang sebesar-besarnya, demi membangun hasil laporan yang lebih baik.

Semoga laporan ini berguna para pembaca sekalian, khususnya mahasiswa Teknik Elektro di Institut Teknologi Nasional Malang dan perkembangan dunia ilmu pengetahuan. Aamiin.....

Wassalamu'alaikum Wr.Wb

Malang, Maret 2007

Penyusun

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BAB I
PENDAHULUAN

1.1. Latar Belakang

Dengan berkembangnya pola pikir manusia terhadap ilmu pengetahuan dan teknologi, ternyata mengalami kemajuan secara terus menerus. Pengembangan terhadap teknologi yang telah tercipta terus dilakukan untuk mendapatkan teknologi yang terbaru, sehingga mampu untuk mengatasi berbagai macam masalah yang semakin meningkat. Bidang teknologi yang mengalami perkembangan antara lain ; teknologi komputer, robotika dan telekomunikasi, yang berkembang pesat dan kontinyu seiring dengan tuntutan dari perkembangan jaman. Suatu sistem yang bekerja berbasiskan komputer akan sangat membantu sekali didalam pekerjaan manusia sehingga semula yang pekerjaan dilakukan secara manual dapat dikerjakan secara otomatis.

Banyak media yang dapat digunakan sebagai media untuk mengirimkan data ke dalam suatu sistem yang ada, misalnya : telepon, sms, jaringan internet, dan sebagainya, namum dengan menggunakan media tersebut dirasakan kurang ekonomis. Hal ini dikarenakan faktor biaya yang dikeluarkan dalam mengkontrol suatu sistem yang bekerja secara kontinyu.

Penulis mengamati suatu permasalahan yang muncul dalam bekerjanya sistem kontrol *traffic light* yang telah ada, yaitu timbulnya kemacetan, yang dikarenakan sesuatu hal di luar dari kondisi yang normal, misalnya ; *ambulance* lewat, pejabat teras lewat, mobil pemadam kebakaran atau konvoi kendaraan/demonstrasi (*emergency condition*). Oleh karena itu, penulis

bermaksud untuk merancang suatu sistem kontrol jarak jauh pada sistem lampu lalu lintas (*traffic light*) dengan menggunakan metode *Radio Communication.*

Salah satu media komunikasi yang dapat digunakan dengan pertimbangan cepat, tepat dan langsung adalah HT (*Handy Talky*). Dengan adanya sistem kontrol *traffic light* dengan media HT (*Handy Talky*), maka pengontrolan sistem tidak lagi tergantung pada tempat, dikarenakan mudah dibawa kemanapun tanpa adanya hubungan kabel jaringan (sistem *nirkabel*) pada jarak tertentu dan pada kondisi tertentu. Selain itu, sistem pengontrolan *traffic light* dapat dilakukan kapanpun bahkan dengan melihat kondisi lapangan secara langsung.

1.2. Rumusan Masalah

Dalam perancangan dan pembuatan sistem kontrol *traffic light* jarak jauh dengan menggunakan radio HT, dapat dirumuskan beberapa permasalahan yang akan dibahas, yaitu :

1. Bagaimana memanfaatkan radio HT (*Handy Talky*) sebagai media komunikasi, yang akan berfungsi sebagai pengirim perintah (informasi) sehingga sistem *traffic light* berjalan sesuai dengan kondisi yang diharapkan.
2. Bagaimana merancang dan membuat perangkat keras (*hardware*) serta perangkat lunak (*software*) pada mikrokontroler yang akan mengendalikan semua kerja sistem, agar dapat bekerja sesuai dengan yang perintah (informasi) yang dikirim.

1.3. Tujuan

Penulisan skripsi ini bertujuan merancang alat kontrol *traffic light* jarak jauh dengan menggunakan HT (*Handy Talky*) sebagai media komunikasinya. Dalam hal ini, menitikberatkan pada permasalahan yang timbul pada kondisi *traffic light* yang tak terduga, misalnya ; kondisi darurat (*ambulance* lewat, pejabat teras lewat, mobil pemadam kebakaran atau konvoi kendaraan/demonstrasi dan sebagainya).

1.4. Batasan Masalah

Untuk memberikan pembahasan yang jelas maka diberikan ruang lingkup pembatasan masalah sebagai berikut :

- Perancangan dan pembuatan alat ini, hanya berupa prototipe.
- Perancangan dan pembuatan sistem ini, dimisalkan hanya untuk mengatur 1 kondisi *traffic light* dengan tiap jalan terdapat 2 jalur.
- Perancangan dan pembuatan sistem ini, digunakan pada kontrol sistem *traffic light standalone*.
- Tidak membahas jenis HT (*Handy Talky*) yang dipakai secara detail.
- Tidak memperhitungkan gangguan frekuensi dari luar.
- Tidak membahas catu daya.

1.5. Sistematika Penulisan

Adapun sistematika dari penyusunan Laporan Skripsi ini adalah :

BAB I PENDAHULUAN

Berisi latar belakang, rumusan masalah, tujuan, batasan masalah, serta sistematika penyusunan dan pembuatan alat.

BAB II TEORI PENUNJANG

Berisi tentang teori – teori dasar yang memiliki relevansi sebagai dasar perencanan dan pembuatan.

BAB III PERENCANAAN DAN PEMBUATAN

Berisi tentang perencanaan *hardware* dan *software*.

BAB IV PENGUJIAN ALAT

Berisi tentang data hasil pengujian peralatan yang telah dibuat secara keseluruhan.

BAB V PENUTUP

Berisi kesimpulan dan saran dari tugas akhir ini

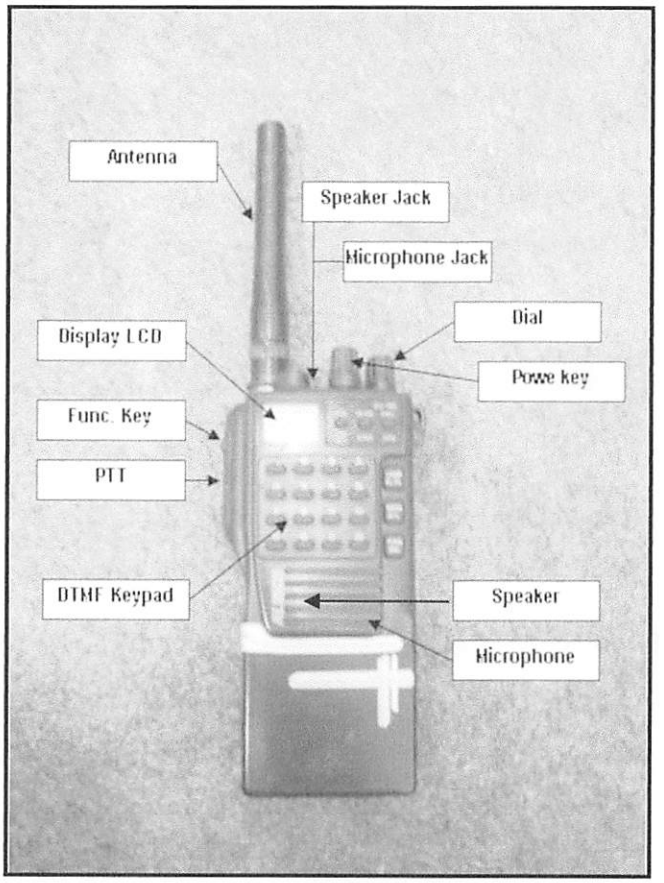
LAMPIRAN

BAB II

TEORI PENUNJANG

2.1 HT (*Handy Talky*)

Radio panggil atau yang lebih dikenal dengan HT (*Handy Talky*), merupakan sebuah alat komunikasi dua arah (*Halfduplex*). Dengan kata lain, merupakan sistem komunikasi yang dapat dilakukan dengan berbicara secara bergantian antara orang pertama dan orang kedua, bahkan lebih pada satu jalur frekuensi yang sama dengan cara menekan tombol PTT (*Push To Talk*)



Gambar 2-1 HT (*Handy Talky*)

Fungsi dan bagian – bagian dari HT adalah ;

1. Display LCD

   Untuk menampilkan frekuensi dan indikator lainnya pada saat digunakan.

2. Dial

   Digunakan untuk menaikkan atau menurunkan frekuensi secara bertahap (manual).

3. Microphone Jack

   Digunakan sebagai microphone eksternal apabila microphone internal tidak digunakan.

4. Speaker Jack

   Digunakan sebagai speaker eksternal apabila speaker internal tidak digunakan.

5. Power Key

   Digunakan untuk menghidupkan atau mematikan HT.

6. Func Key

   Digunakan untuk mengakses fungsi-fungsi yang ada pada HT.

7. Microphone

   Internal microphone.

8. DTMF Keypad dan tombol lain

   Tombol 1 - 9, dapat menghasilkan nada tone DTMF, yang apabila ditekan akan dapat mengahasilkan nada *tone* tertentu.

9. PTT (Push To Talk)

   Tekan PTT pada saat Tx dan dilepas pada saat Rx.

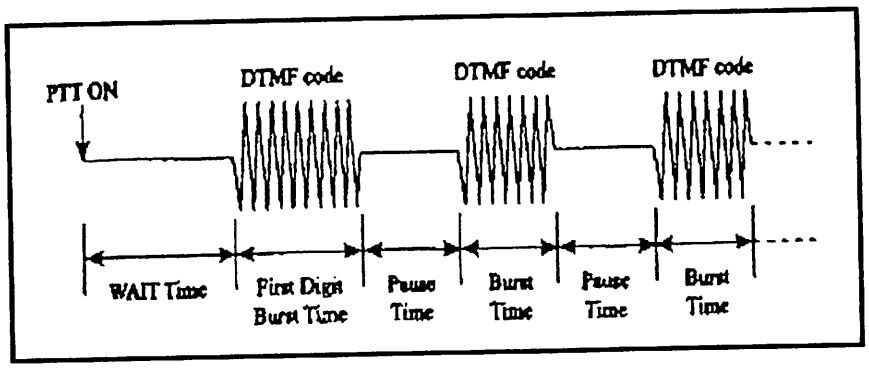
10. Speaker

    Internal speaker.

11. Antena Connector

    Dihubungkan dengan antena.

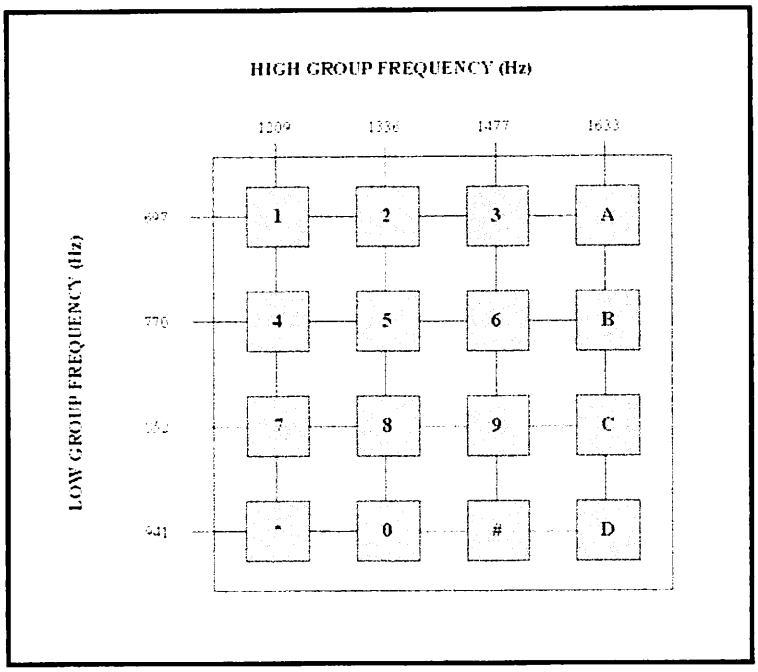
Selain sebagai media komunikasi penghantar suara untuk komunikasi, HT juga dapat menghasilkan sinyal DTMF (*Dual Tone Multi Frequency*).



Gambar 2-2 Bentuk Sinyal DTMF yang Dikeluarkan HT (*Handy Talky*)

Sistem DTMF (*Dual Tone Multi Frequency*) *keypad* pada radio HT memiliki prinsip kerja yang sama dengan *keypad* pada sistem telepon ataupun *handphone* (HP), yaitu sistem *signaling* (*Touch Tone*). Dalam sistem ini tersusun atas sebuah kombinasi dari dua frekuensi (frekuensi rendah dan frekuensi tinggi) yang dihubungkan (dikodekan) dengan angka (0 – 9) dan karakter (*, #, A, B, C, D). Prinsip kerjanya adalah setiap penekanan tombol, maka akan dikeluarkan sinyal DTMF yang terdiri atas kombinasi dua sinyal, yang kemudian akan ditransmisikan melalui media radio. Misal tombol *keypad* yang ditekan adalah

digit 8, maka sinyal yang ditransmisikan adalah kombinasi antara sinyal 852 Hz dengan 1336 Hz.



Gambar 2-3 *Keypad* HT (*Handy Talky*)

2.2 Mikrokontroler Renesas R8C/13 Tiny (R5F21134FP)

Renesas Technology adalah produsen semikonduktor tingkat internasional. Renesas tercipta dari gabungan dua produsen semikonduktor, yaitu Mitsubishi dan Hitachi. Sebagai produsen semikonduktor, renesas juga mengeluarkan berbagai jenis keluarga mikrokontroler (MK).

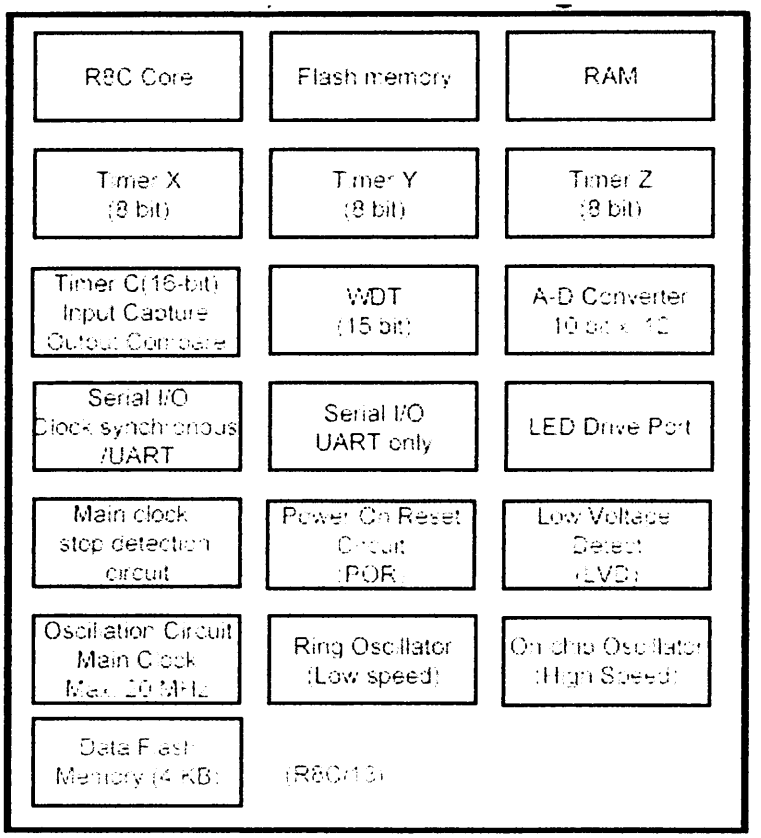
Renesas R8C adalah salah satu jenis seri dalam keluarga MK M16C. CPU R8C sama dengan CPU CISC 16-*bit* M16C, hanya saja lebar jalur data R8C adalah 8-*bit*. Karena menggunakan CPU yang sama maka R8C memiliki

instruction set hampir sama dengan M16C. Perbedaannya hanya terletak pada 2 instruksi, yaitu R8C tidak memiliki instruksi JMPS *(Jump Special Page)* dan JSRS *(Jump Subroutine Special Page).* R8C/13 adalah salah satu tipe MK dalam seri R8C. MK ini memiliki kemasan 32-*pin* LQFP. Dalam perancangan pada skripsi ini menggunakan menggunakan MK seri R5F21134, yaitu R8C/13 yang memiliki Flash ROM 16 KB (1000 E/W *cycles*) dan RAM sebesar 1 KB.

2.2.1 Spesifikasi R5F21134FP

Berikut ini adalah spesifikasi *R5F21134FP* dengan peta peripheral dan memori-memorinya.

- Mempunyai *CPU Core* (16-bit) 1 – 20 MHz, 3.0 – 5.5 Volt dan 1 – 10 MHz 2.7 – 5.5 Volt.
- Rangkaian Clock, kecepatan *Low/High On-Chip Oscillator. Clock* utama dengan Xin/Xout.
- Memory (ROM/SRAM) 16 Kbytes / 1 Kbytes, 2 x 2 KBytes Data Flash pada R8C/12, 13.
- Kemasan 32 pin LQFP (7mm x 7mm)



Gambar 2-4 Blok Diagram R8C/11, 13 dan Peta *Peripheral*-nya

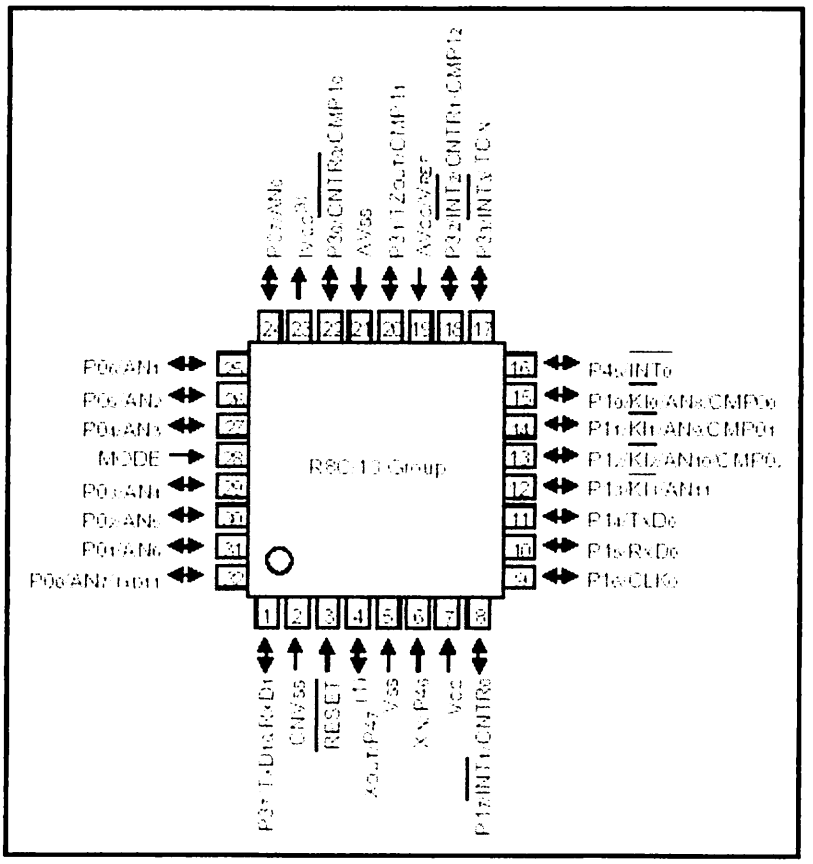
2.2.2 Kelebihan Kunci R8C/Tiny

Banyak kelebihan-kelebihan yang dimiliki R8C/Tiny diantaranya adalah :

- Kompatibel dengan M16C yaitu kompatibel dalam instruksi dan kode.
- *Peripheral* lebih terintegrasi jadi lebih hemat.
- *Electromagnetic Compatibility* (EMC) mempunyai EMI rendah, EMS tinggi.
- *Development Tool* (*Compiler* dan *Debugger*) didapat dengan murah dan difasilitasi *On-Chip Debugger.*
- Mempunyai fitur *fail-safe* yaitu pengamanan terhadap kegagalan sistem.

- Konsumsi daya rendah.
- 16-bit CISC CPU dengan kecepatan maksimal 20 MHz (1:1).
- 89 instruksi CISC lebih hemat ROM kira-kra 20 %, RAM sampai 1 KB.
- Waktu konversi ADC hanya 3 uS.

2.2.3 Konfigurasi Pin R8C R5F21134FP



Gambar 2-5 Konfigurasi Pin R8C/Tiny

Gambar diatas adalah kofigurasi pin-pin dari *R8C R5F21134FP* untuk lebih jelasnya dapat diamati pada tabel dekripsi pin-pin berikut ini :

Tabel 2-1 Konfigurasi Pin-Pin dari R8C R5F21134FP

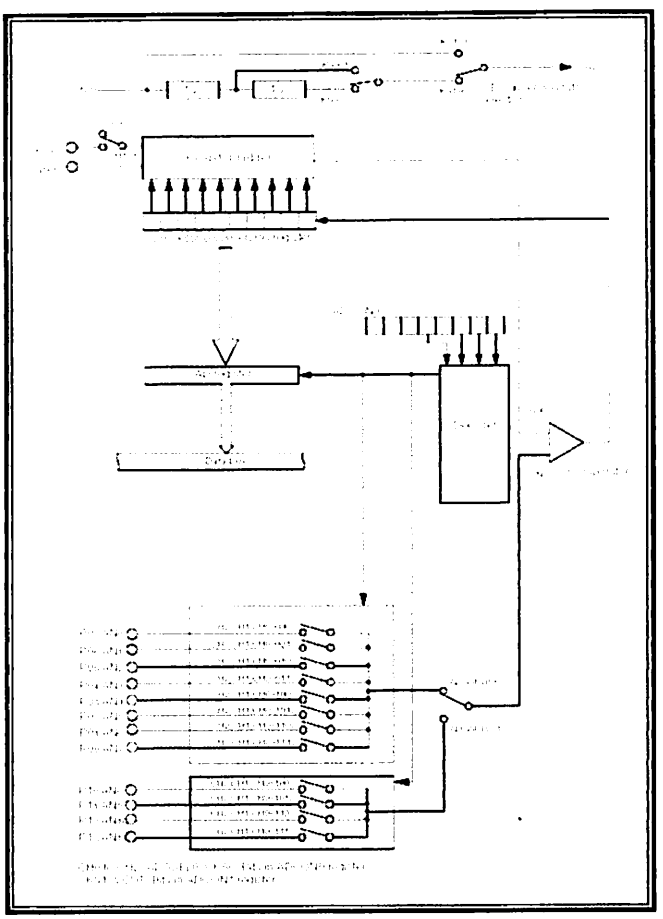
Nama Sinyal	Nama Pin	Type I/O	Fungsi
Masukan Catu Daya	Vcc, Vss	I	Tegangan 2.7 V – 5.5 V pada pin Vcc. Tegangan 0 V pada Vss pin
I Vcc	Ivcc	O	Pin ini untuk men-stabilkan catu daya *internal,* pin ini dihubungkan pada Vss melalui kapasitor 100nF. Jangan dihubungkan pada Vcc.
Input Catu Daya Analog	Avcc, Avss	I	Ini adalah untuk catu daya pada ADC. Avcc dihubungkan pada Vcc, A Vss dihubungkan ke Vss. Dianjurkan untuk menghubungkan kapasitor diantara pin A Vcc dan A Vss.
Input Reset	RESET	I	"L" untuk masukan ini mereset MCU
CNVss	CNVss	I	Pin ini dihubungkan pada Vss melalui sebuah resistor.
MODE	MODE	I	Pin ini dihubungkan pada Vcc melalui sebuah resistor.
Input Clock Utama	Xin	I	Pin-pin ini disediakan untuk membangkitkan rangkaian I/O Clock Utama. Dihubungkan dengan sebuah keramik resonator atau kristal diantara pin Xin dan Xout. Jika digunakan clock internal maka pin Xin dan Xout dalam keadaan terbuka.
Output Clock Utama	Xout	O	
Input Interupsi	INT0 – INT3	I	Pin ini sebagai masukan interupsi.
Input Kunci Interupsi	KI0 – KI3	I	Pin ini sebagai masukan kunci interupsi.
Timer X	CNTR 0	I/O	Pin I/O ini adalah untuk Timer X .
	CNTR 0	O	Pin Ouput untuk Timer X.
Timer Y	CNTR 1	I/O	Pin I/O untuk Timer Y.
Timer Z	TZout	O	Pin Ouput untuk Timer Z.
Timer C	TC in	I	Pin Input untuk Timer C.
	CMP00 CMP03 CMP10 CMP13	O	Pin Output untuk Timer C.
Serial Interface	CLK 0	I/O	Pin I/O untuk memindahkan Clock.
	RXD0, RXD1	I	Pin input untuk data Serial.

	TXD0, TXD10, TXD11	O	Pin output untuk data Serial.
Input Tegangan Referensi	Vref	I	Tegangan referensi input ini untuk ADC. Vref pin dihubungkan ke Vcc.
ADC, pengubah dari analog ke digital	AN0– AN11	I	Pin analog input pada ADC.
Port I/O	P00-P07, P10-P17, P30-P33, P37, P45	I/O	Merupakan port I/O CMOS 8-bit . Setiap port mempunyai pilihan register pengarah sebagai input atau output. Tiap Port dapat dialamati per bit. Dapat di-set menggunakan pull up resistor dengan program. P10 – P17 mempunyai driver transistor.
Port Input	P46, P47	I	Pin ini hanya bisa digunakan sebagai input.

2.2.4 Peripheral R8C/Tiny

Mikrokontroler R8C R5F21134FP mempunyai beberapa *peripheral-peripheral* yang banyak digunakan pada beberapa aplikasi-aplikasi penting, diantaranya adalah sebagai berikut :

- ***Analog To Digital Converter*** **(ADC)**



Gambar 2-6 Diagram Blok ADC

Dengan 12 SAR ADC S/H yang mempunyai resolusi 8-bit atau 10-bit. Mode Operasinya menggunakan *One-Shot dan Repeat* dengan waktu konversi 2.8 uS (pada clock 10 MHz). Berikut gambar diagram blok ADC *built in* pada mikrokontroler ini :

- ***Timer Mode***

  Mempunyai timer sebanyak 4 yaitu timer X, Y, Z, C. Berikut adalah mode-mode timernya :

Tabel 2-2 Mode-mode Timer

Item		Timer X	Timer Y	Timer Z	Timer C
Configuration		8-bit timer with 8-bit prescaler	8-bit timer with 8-bit prescaler	8-bit timer with 8-bit prescaler	16-bit timer
Count		Down	Down	Down	Up
Count source		•f1 •f2 •f8 •f32	•f1 •f8 •TRING •Input from CNTR1 pin	•f1 •f2 •f8 •Timer Y underflow	•f1 •f8 •f32
Function	Timer mode	provided	provided	provided	not provided
	Pulse output mode	provided	not provided	not provided	not provided
	Event counter mode	provided	provided[1]	not provided	not provided
	Pulse width measurement mode	provided	not provided	not provided	not provided
	Pulse period measurement mode	provided	not provided	not provided	not provided
	Programmable square-wave generation mode	not provided	provided	provided	not provided
	Programmable one-shot generation mode	not provided	not provided	provided	not provided
	Programmable one-shot one-shot generation mode	not provided	not provided	provided	not provided
	Capture	not provided	not provided	not provided	provided
Input pin		CNTR0	CNTR1	$\overline{INT0}$	TCIN
Output pin		CNTR0 $\overline{CNTR0}$	CNTR1	TZOUT	not provided
Related interrupt		Timer X int $\overline{INT1}$ int	Timer Y int $\overline{INT2}$ int	Timer Z int $\overline{INT0}$ int	Timer C int $\overline{INT3}$ int
Timer stop		provided	provided	provided	provided

- ***Low Voltage Detect*** **(LVD)**

  LVD adalah untuk mendeteksi Vcc kurang dari 3.8 V (± 0.5 V).

- ***Watchdog Timer***

  Watchdog berfungsi untuk mendeteksi ketika program diluar kontrol.

- ***On Chip Debugger***

  Fasilitas ini mempunyai fungsi untuk dapat di-*debug* pada waktu mikro sedang berjalan. Antara PC dan MK dapat berkomunikasi, PC akan mengetahui aktivitas MK saat itu. Syarat-syarat *On Chip Debugger* adalah

  - Vektor *Address Match interrupt* harus dihindari.
  - *Single step interrupt* tidak dapat digunakan bersamaan interrupt lain.
  - *UART1* tidak boleh dipakai.
  - Instruksi BRK tidak boleh dipakai.
  - Flash Address C000H – C7FFH.
  - PD 3.7 harus "0".
  - B5 FMR 0 harus "1"
  - Menyiapkan 8 Byte untuk Stack.
  - *On Chip Debugger* berpengaruh pada *timing run.*

- **Rangkaian Osilator**

  Pada osilator utama menggunakan kristal luar sampai dengan 20 MHz, dengan memiliki fitur *Clock Stop Detect*. Kemudian untuk *On Chip* Osilator disediakan kecepatan *Low* 125 KHz dan *High* 8 MHz. Saat setelah reset, default clock adalah kecepatan rendah *On Chip* osilator 125 KHz.

2.3 Mikrokontroler AT89S51

Perbedaan mendasar antara mikrokontroler dan mikroprosesor adalah mikrokontroler selain memiliki CPU juga dilengkapi memori dan input output yang merupakan kelengkapan sebagai sistem minimum mikrokomputer sehingga sebuah mikrokontroler dapat dikatakan sebagai mikrokomputer dalam keping tunggal *(Single Chip Microcomputer)* yang dapat berdiri sendiri.

Mikrokontroler AT89S51 adalah mikrokontroler ATMEL yang kompatibel penuh dengan mikrokontroler keluarga MCS – 51, membutuhkan daya rendah, memiliki *performance* yang tinggi dan merupakan mikrokomputer 8 bit yang dilengkapi 4 Kbyte EEPROM *(Electrical Erasable and Programmable Read Only Memory)* dan 128 Byte RAM internal. Program memori yang dapat diprogram ulang dalam sistem atau menggunakan programmer *Nonvolalite Memory* konvensional.

Dalam sistem mikrokontroler terdapat dua hal yang mendasar, yaitu: perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

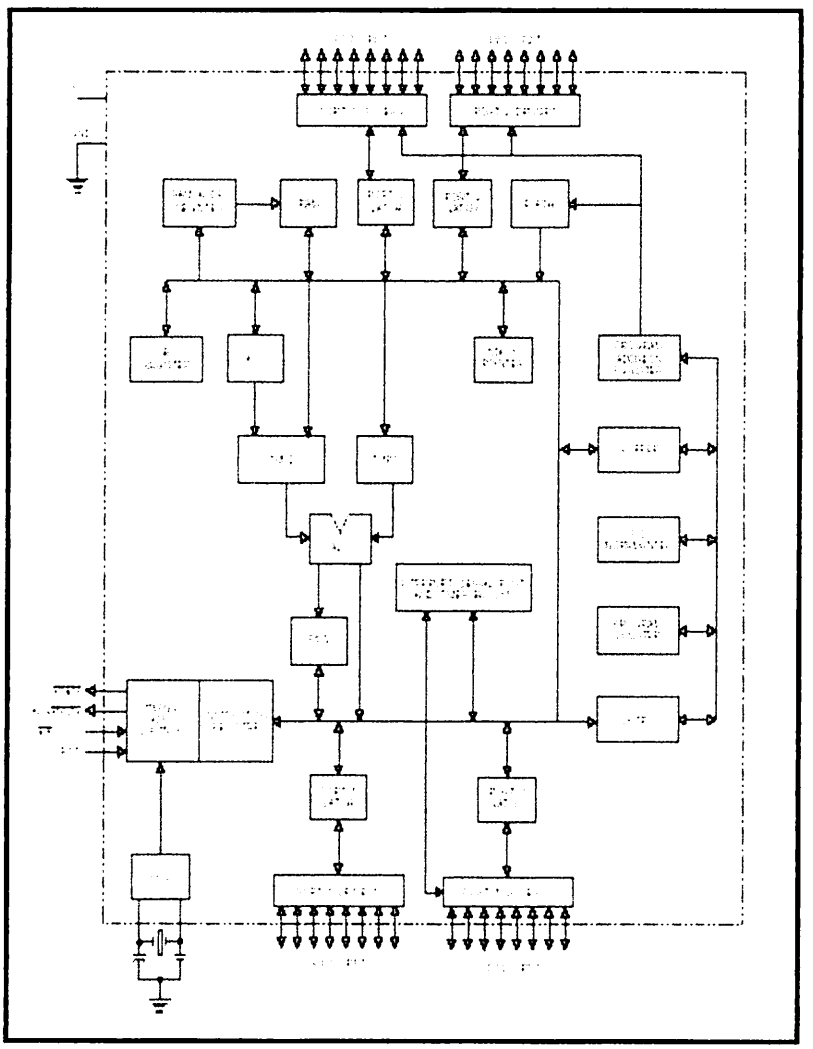
2.3.1 Perangkat keras mikrokontroler AT89S51

Secara umum Mikrokontroler AT89S51 memiliki :

- CPU 8 bit termasuk keluarga MCS-51
- 4 Kb Flash memory
- 128 byte Internal RAM
- 4 buah Port I/O, masing – masing terdiri atas 8 jalur I/O

- 2 Timer/ counter 16 bit
- 1 Serial Port Full Duplex
- Kecepatan pelaksanaan intruksi per siklus 1 us pada frekuensi clock 2 Mhz

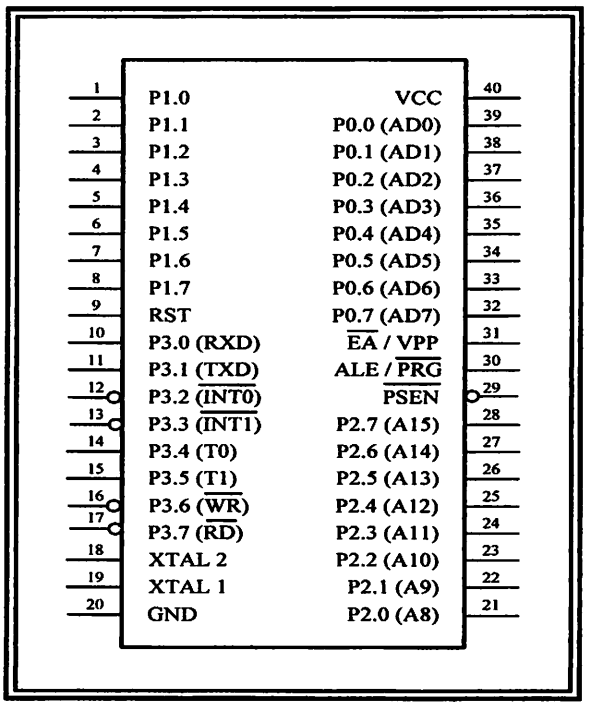
Dengan keistimewaan diatas pembuatan alat menggunakan AT89S51 menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak. Adapun Blok Diagram dari Mikrokontroler AT89S51 adalah sebagai berikut:



Gambar 2-7 Blok Diagram Mikrokontroler AT89S51

2.3.2 Konfigurasi Pena-Pena Mikrokontroler AT89S51

Mikrokontroler AT89C51 terdiri dari 40 pin dengan konfigurasi sebagai berikut:



Gambar 2-8 Konfigurasi Pena-Pena AT89S51

Fungsi tiap pin-nya adalah sebagai berikut :

- VCC (Supply tegangan), *pin 40*
- GND (*Ground*), *pin 20*
- Port 0, *pin 32 – 39*

  Merupakan port input-output dua arah, port ini digunakan sebagai multipleks bus alamat rendah (A0 – A7) dan data selama pengaksesan program memory dan data memory eksternal
- Port 1, *pin 1 – 8*

  Merupakan port input-output dua arah dengan internal pull-up

- Port 2, *pin 21 - 28*

  Merupakan port input-output dengan internal pull-up. Mengeluarkan alamat tinggi selama pengambilan program memori external.

- Port 3, *pin 10 – 17*

  Merupakan port input-output dengan internal pull-up, dimana Port 3 juga memiliki fungsi khusus dan dapat dilihat pada tabel berikut ini:

Tabel 2-3. Fungsi Khusus Pada Port 3

Nama Penyemat	Fungsi Khusus
Port 3.0	RxD (Port masukan serial)
Port 3.1	TxD (Port keluaran Serial)
Port 3.2	/INTO (Masukan Interupsi Eksternal 0)
Port 3.3	/INT1 (Masukan Interupsi Eksternal 1)
Port 3.4	T0 (masukan pewaktu eksternal 0)
Port 3.5	T1 (masukan pewaktu eksternal 1)
Port 3.6	/WR (sinyal tulis memori data eksternal)
Port 3.7	/RD (sinyal baca memori data eksternal)

- RST (Reset), *pin 9*

  Input Reset merupakan reset master untuk AT89S51.

- ALE / Prog (*Address Latch Enable*), *pin 30*

  Digunakan untuk menahan alamat memori eksternal selama pelaksanaan intruksi.

- PSEN (*Program Strobe Enable*), *pin 29*

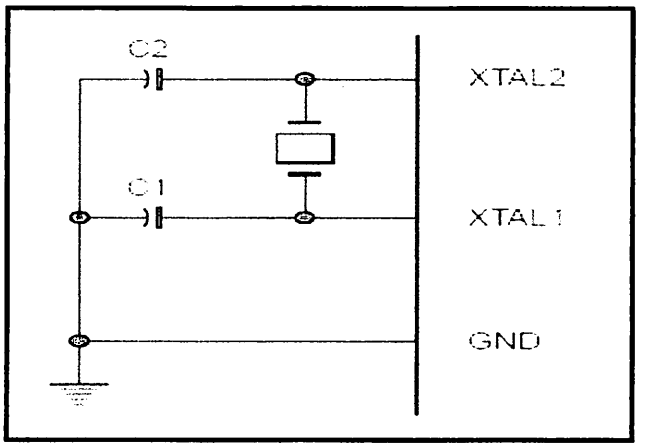
Merupakan sinyal pengontrol yang memperbolehkan program memori eksternal masuk kedalam bus.

- EA / VPP (*External Access*), *pin 31*

  Dapat diberikan logika rendah (Ground) atau logika tinggi (+5V). Jika diberikan logika tinggi maka mikrokontroler akan mengakses program dari ROM internal (EEPROM/Flash Memori), dan jika diberikan logika rendah maka mikrokontroler akan mengakses program dari memori eksternal.

- X-TAL 1 dan X-TAL 2, *pin 19, 18*

  Pin ini dihubungkan dengan kristal bila menggunakan osilator internal. X-TAL 1 merupakan masukan ke rangkaian osilator internal sedangkan X-TAL 2 keluaran dari rangkaian osilator internal. Untuk keperluan ini diperlukan kapasitor penstabil sebesar 30pF. Dan nilai dari X-TAL tersebut antara 4 – 24 Mhz. Untuk lebih jelasnya dapat dilihat gambar pemasangan X-TAL serta kapasitor yang digunakannya.



Gambar 2-9 Osilator Eksternal AT89S51

2.3.3 Organisasi Memory

Organisasi memori pada mikrokontroler AT89S51 dapat dibagi menjadi dua bagian besar yaitu memori program dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpanan data maupun program. Memori program digunakan untuk menyimpan instruksi-instruksi yang akan dijalankan oleh mikrokontroler, sedangkan memori data digunakan sebagai tempat yang sedang diolah mikrokontroler.

Program mikrokontroler disimpan dalam memori program berupa ROM. Mikrokontroler AT89S51 dilengkapi dengan ROM internal, sehingga untuk menyimpan program tidak digunakan ROM eksternal yang terpisah dari mikrokontroler. Agar tidak menggunakan memori program eksternal, penyemat/EA dihubungkan dengan Vcc (logika 1).

Memori program mikrokontroler menggunakan alamat 16 bit mulai 0000_H-$0FFF_H$, sehingga kapasitas penyimpanan program maksimal adalah 4Kb. Sinyal /PSEN (*Program Store Enable*) tidak digunakan jika digunakan memori program internal.

Selain program, mikrokontroler AT89S51 juga memiliki data internal 128 *byte* dan mampu mengakses memori data eksternal sebesar 64 Kb. Semua memori data internal dapat dialamati dengan data langsung atau tidak langsung. Ciri dari pengalamatan langsung adalah *operand* adalah alamat *register* yang berisi alamat data yang akan diolah. Sebagian memori tersebut dapat dialamati dengan pengalamatan register, dan sebagian lagi dapat dialamati dengan memori satu bit.

Untuk membaca data digunakan sinyal /RD sedangkan untuk menulis digunakan sinyal /WR.

2.3.4 SFR (*Special Function Register*)

Register Fungsi Khusus (*Special Function Register*) terletak pada 128 byte bagian atas memori data internal dan berisi register-register untuk pelayanan latch port, timer, program status words, control peripheral dan sebagainya.

Tabel 2-4. *Special Function Register*

Simbol	Nama Register	Alamat
ACC	Accumulator	$E0_H$
B	Register B	$F0_H$
PSW	Program Status Word	$D0_H$
SP	Stack Pointer	81_H
DPTR	Data Pointer 2 Byte	
DPL	Bit rendah	82_H
DPH	Bit Tinggi	83_H
P0	Port 0	80_H
P1	Port 1	90_H
P2	Port 2	$A0_H$
P3	Port 3	$B0_H$
IP	Interupt Periority Control	$D8_H$
IE	Interupt Enable Control	$A8_H$
TMOD	Timer/Counter Mode Control	89_H
TCON	Timer/Counter Control	88_H
TH0	Timer/Counter 0 High Control	$8A_H$
TL0	Timer/Counter 0 Low Control	$8B_H$
TH1	Timer/Counter 1 High Control	$8C_H$
TL1	Timer/Counter 1 Low Control	$8D_H$
SCON	Serial Control	98_H
SBUF	Serial Data Buffer	99_H
PCON	Power Control	87_H

Beberapa macam register fungsi khusus yang sering digunakan adalah sebagai berikut ini :

- *Accumulator* (Acc) merupakan register untuk penambahan dan pengurangan. Perintah *mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register B* merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Stack Pointer* (SP) merupakan register 8 bit yang dapat diletakkan di alamat manapun pada RAM internal.
- *Data Pointer* (DPTR) terdiri dari dua register, yaitu untuk byte tinggi (Data Pointer High, DPH) dan byte rendah (Data Pointer Low, DPL) yang berfungsi untuk mengunci alamat 16 bit.
- *Port 0* sampai *Port 3* merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada port 0, 1, 2, 3. Masing-masing register ini dapat dialamati per-port maupun per-bit.
- *Control Register* terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua register khusus, yaitu register IP (*Interupt Priority*) dan register IE (*Interupt Enable*). Untuk mengontrol pelayanan timer/counter terdapat register khusus, yaitu register TCON (*timer/counter control*) serta pelayanan port serial menggunakan register SCON (*Serial Port Contro*).

2.3.5 Sistem Interupsi

Mikrokontroler AT89S51 mempunyai 5 buah sumber interupsi yang dapat membangkitkan permintaan interupsi, yaitu : INT0, INT1, T1, T2 dan Port Serial.

Saat terjadinya interupsi mikrokontroler secara otomatis akan menuju ke subrutin pada alamat tersebut. Setelah interupsi selesai dikerjakan, mikrokontroler akan mengerjakan program semula. Tiap-tiap sumber interupsi dapat enable atau disable secara *software*.

Tingkat prioritas semua sumber *interupt* dapat diprogram sendiri-sendiri dengan *set* atau *clear* bit pada (*Interupt Priority*). Jika dua permintaan interupsi dengan tingkat prioritas yang berbeda diterima secara bersamaan, permintaan interupsi dengan prioritas tertinggi yang akan dilayani. Jika permintaan interupsi dengan prioritas yang sama diterima bersamaan, akan dilakukan polling untuk menentukan mana yang akan dilayani. Bit-bit pada IP adalah sebagai berikut:

Tabel 2-5. Prioritas Interupsi

Prioritas	Jenis Interupsi
1	Interupsi Eksternal 0
2	Interupsi Timer 0
3	Interupsi Eksternal 1
4	Interupsi Timer 1
5	Interupsi Serial

IP.7	IP.6	IP.5	IP.4	IP.3	IP.2	IP.1	IP.0
–	–	–	**PS**	**PT1**	**PX1**	**PT0**	**PX0**

Gambar 2-10 Register Interupt

Priority bit = 1 menandakan prioritas tinggi

Priority bit = 0 menandakan prioritas rendah

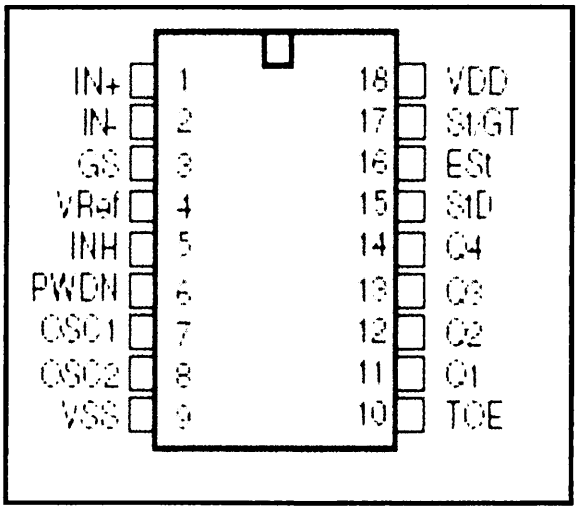
Simbol	**Posisi**	**Fungsi**
–	IP.7	Kosong
–	IP.6	Kosong
–	IP.5	Kosong
PS	IP.4	Bit prioritas interupsi port serial
PT1	IP.3	Bit prioritas interupsi Timer 1
PX1	IP.2	Bit prioritas interupsi $\overline{INT1}$
PT0	IP.1	Bit prioritas interupsi Timer 0
PX0	IP.0	Bit prioritas interupsi $\overline{INT0}$

Tabel 2-6 Alamat Sumber Interupsi

Sumber interupsi	**Alamat Awal**
Interupt Luar 0 (INT 0)	0003_H
Pewaktu / pencacah 0 (T0)	$000B_H$
Interupt Luar 1 (INT 1)	0013_H
Pewaktu / pencacah 1 (T1)	$001B_H$
Port Serial	0023_H

2.4 *Decoder* DTMF (*Dual Tone Multi Frequency*)

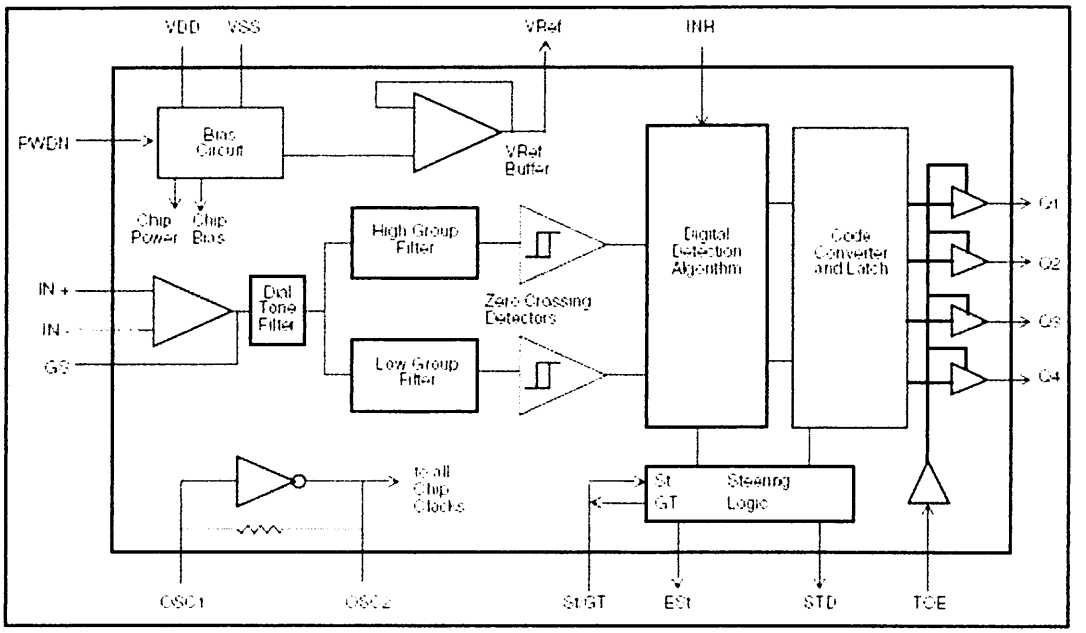
Decoder DTMF digunakan untuk mengkodekan nada *tone* DTMF ke dalam bentuk biner 4 bit. *Decoder* DTMF mempunyai beberapa masukan atau M input dimana salah satu masukan tersebut akan menghasilkan keluaran dengan N-bit output. Konfigurasi 2^N=M menyatakan untuk input desimal M akan dihasilkan output biner sebanyak N-bit. Sebagai contoh, 2^4=16 maka untuk 16 input desimal dihasilkan 4 output biner. Dapat dilihat dari gambar 2-11 bentuk IC dari *decoder* DTMF dibawah:



Gambar 2-11 Konfigurasi Pin IC MT8870

Sebagai contoh apabila *decoder* DTMF memiliki satu masukan aktif yaitu 8 maka akan menghasilkan keluaran biner 1000, yang berarti biner Q1 aktif. Salah satu contoh aplikasi adalah IC MT 8870 yang mempunyai ukuran kecil dengan kebutuhan power yang rendah dan *performance* yang tinggi. Memiliki dua fungsi yaitu sebagai *bandsplit filter* dan *dekoder digital*. Pada bagian filter menggunakan teknik *switching* kapasitor untuk *high pass filter* dan *low pass filter*. Sedang *decoder* menggunakan teknik perhitungan digital untuk mendeteksi dan

mendekodekan semua pasangan 16 sinyal DTMF menjadi sebuah kode 4 bit. Perhitungan komponen luar diminimumkan oleh *on chip provision* dari sebuah *differential input amplifier*, *clock oscillator* dan rangkaian *latched three state bus*. Berikut adalah blok diagram dari *decoder*DTMF :



Gambar 2-12 Diagram Blok *Decoder* DTMF MT8870

Bila suatu sinyal telah dideteksi, kemudian keluaran dari filter akan dideteksi oleh *"Digital Detection Algorithm"* dan kemudian diubah oleh *"Code Converter And Latch"*, maka setiap masukan akan keluar sesuai dengan yang telah ditentukan. Dapat dilihat pada tabel 2.7 berikut:

Tabel 2-7. Tabel Kombinasi *Decoder* DTMF

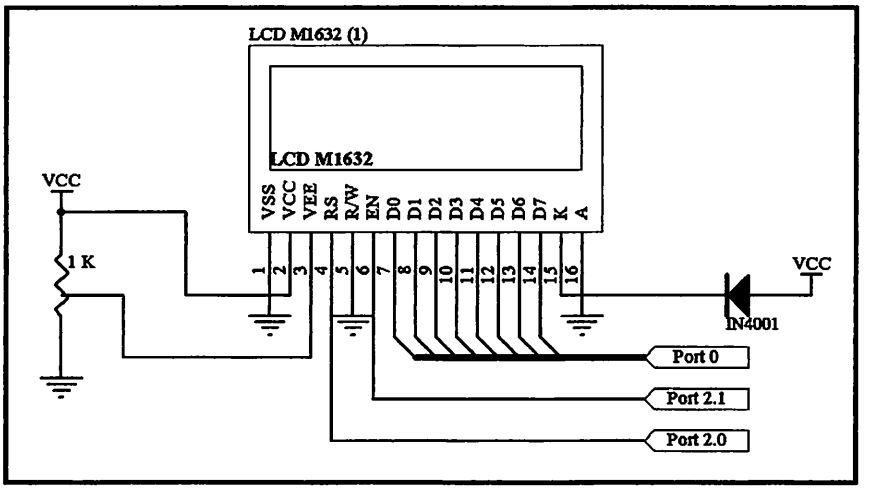
TOMBOL	FREK BAWAH	TOE	INH	FREK ATAS	Q_1 Q_2 Q_3 Q_4
1	697	H	X	1209	0 0 0 1
2	697	H	X	1336	0 0 1 0
3	697	H	X	1477	0 0 1 1
4	770	H	X	1209	0 1 0 0
5	770	H	X	1336	0 1 0 1
6	770	H	X	1477	0 1 1 0
7	852	H	X	1206	0 1 1 1
8	852	H	X	1336	1 0 0 0
9	852	H	X	1477	1 0 0 1
0	941	H	X	1209	1 0 1 0
*	941	H	X	1336	1 0 1 1
#	941	H	X	1477	1 1 0 0
A	697	H	L	1633	1 1 0 1
B	770	H	L	1633	1 1 1 0
C	852	H	L	1633	1 1 1 1
D	941	H	L	1633	0 0 0 0

2.5 LCD (*Liquid Crystal Display*)

Liquid Crystal Display adalah modul tampilan yang mempunyai konsumsi daya yang relatif rendah dan terdapat sebuah *controller* CMOS didalamnya. *Controller* tersebut sebagai pembangkit ROM/RAM dan display data RAM. Semua fungsi tampilan di kontrol oleh suatu instruksi modul LCD dapat dengan mudah diinterfacekan dengan MPU. Ciri-ciri dari LCD M1632 :

- Terdiri dari 32 karakter yang dibagi menjadi 2 baris dengan display dot matrik 5 X 7 ditambah cursor.
- Karakter generator ROM dengan 192 karakter.
- Karakter generator RAM dengan 8 tipe karakter.
- 80 X 8 bit display data RAM.

- Dapat diinterfacekan dengan MPU 8 atau 4 bit.
- Dilengkapi fungsi tambahan : Display clear, cursor home, display ON/OFF, cursor ON/ OFF, display character blink, cursor shift dan display shift.
- Internal data.
- Internal otomatis dan reset pada power ON.
- +5 V *power supply* tunggal.



Gambar 2-13 LCD (*Liquid Crystal Display*)

Berikut ini merupakan pin-pin LCD berserta konfigurasinya:

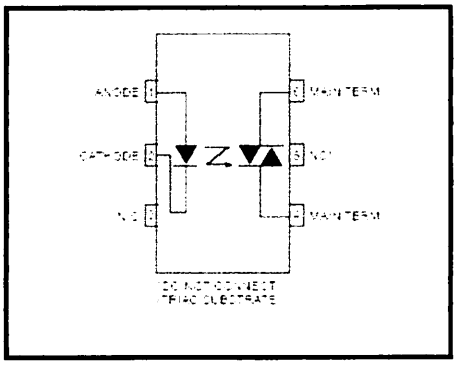
Tabel 2-8. Pin-Pin LCD Dan Konfigurasinya

NAMA PIN	JUMLAH	I/O	TUJUAN	FUNGSI
DB0-DB3	4	I/O	MPU	Tri state bidirectional lower data bus: data dibaca dari modul ke MPU atau dari MPU ditulis ke modul melalui bus
DB4-DB7	4	I/O	MPU	Tri state bidirectional upper fourdata bus: data dibaca dari modul ke MPU atau dari MPU ditulis ke modul melalui bus
E	1	Input	MPU	Sinyal operasi dimulai: sinyal aktif baca/tulis
R/W	1	Input	MPU	Sinyal pilih data dan tulis (0:tulis,1:baca)
RS	1	-	Power supply	Sinyal pilih register 0: Instruction register (write) Busy flag dan addess counter (read) 1: Data register (write dan read)
VLC	1	-	Power supply	Penyetelan kontras pada tampilan LCD
VDD	1	-	Power supply	+ 5V
VSS	1	-	Power supply	Ground 0V

2.6 TRIAC

2.6.1 Optotriac

Berfungsi untuk mengisolasi anatara suatu bagian/rangkaian dengan bagian rangkaian lain. Tujuan pengsolasian adalah untuk mencegah agar tidak terjadi kerusakan komponen pada suatu bagian sebagai akibat dari munculnya tegangan tinggi yang tidak diinginkan pada suatu bagian lainnya. Digunakan optotriac MOC 3021, yang membias diac, jika terdapat arus masuk sebesar 10 mA – 30mA.

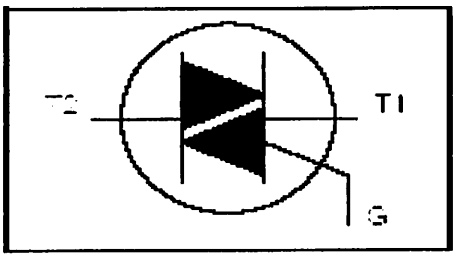


Gambar 2-14. Optotriac MOC 3021

2.6.2 Triac

Transistor Active Current (TRIAC) adalah komponen semikonduktor yang beroperasi seperti dua SCR dengan anoda-katoda terhubung. Sebuah triac terdiri atas dua dioda paralel yang dihubungkan pada arah yang berbeda dengan sebuah gerbang. Perbedaan utama antara triac dan SCR adalah dapat mengahantarkan arus tanpa memperhatikan polaritas tegangan dan keadaan bias pemicu yang diberikan pada gerbang. Karena tidak ada lagi terminal anoda dan katoda maka terminal pada triac disebut dengan terminal utama *(main terminal)* MTI dan MT2.

Triac menjadi aktif dengan memberikan teganan positif atau negatif pada gerbangnya. Seperti SCR, jika sebuah triac telah menjadi aktif, gerbang tidak dapat mematikan triac. Triac juga dikomutasi dengan menurunkan arus penahan dibawah nilai minimumnya. Kerugian yang utama pada triac dibanding dengan SCR adalah kemampuan menghantarkan arus yang kecil. Kebanyakan triac hanya dapat mengalirkan arus maksimum kurang dari 40A dan tegangan maksimum sebesar 600V.



Gambar 2-15 Simbol TRIAC

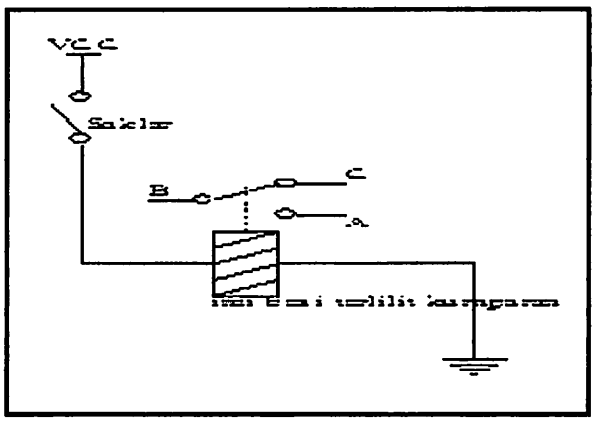
Dalam penggunaannya TRIAC memiliki beberapa keunggulan antara lain sebagai berikut :

- TRIAC lebih sederhana dalam pemakaiannya.
- Banyak ragam terapannya, termasuk pengemudian daya AC
- Triac memungkinkan pengemudian arus yang relatif besar, dari sumber berdaya kecil.
- Tidak terjadi bentuk kontak
- Daerah langsung antara MT1 dan MT2 berupa jajaran sekelar p-n-p-n dan n-p-n-p.
- Lambang terdiri dari lambang SCR yang dikombinasi dengan lambang SCR komplementer.
- Triac tidak kenal istilah "anoda" dan "katoda" melainkan dengan angka-angka: MT2 dan MT1 (*MT= Main terminal*)

2.7 Relay

Relay merupakan sebuah alat yang berfungsi sebagai saklar yang dikemudikan oleh koil yang ada didalamnya. Untuk dapat mengaktifkan *relay* ini, hanya perlu memberikan tegangan dan arus sebesar tegangan yang diperlukan

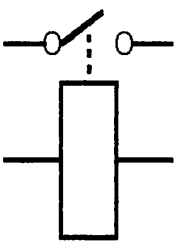
oleh koil. Prinsip kerja dari sebuah *relay* adalah adanya gaya magnetik pada inti besi yang dililit oleh koil pada saat diberi tegangan. Dengan adanya gaya magnetik ini, maka tuas besi besi akan tertarik dan bergerak. Dengan tertariknya tuas besi ini, tuas kontaktor akan terdorong dan saling menempel. Maka terjadilah aliran listrik antara kedua kontaktor tersebut. Kontaktor tersebut berfungsi seperti sebuah *switch.*



Gambar 2-16 Cara Kerja *Relay*

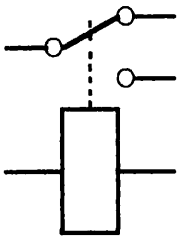
Ada beberapa macam relay, antara lain:

- SPST *(Single Pin Single Terminal)*



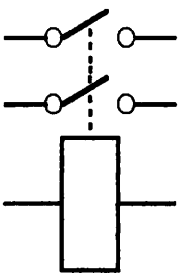
Relay SPST

- SPDT *(Single Pin Dual Terminal)*



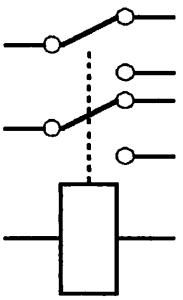
Relay SPDT

- DPST *(Dual Pin Single Terminal)*



Relay DPST

- DPDT *(Dual Pin Dual Terminal)*

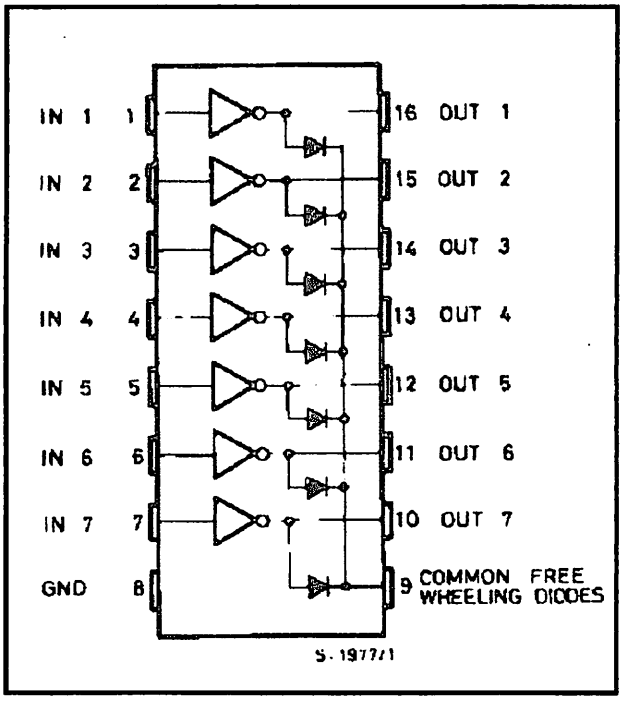


Relay DPDT

2.8 Driver *Relay*

Masalah yang muncul adalah ketika suatu rangkaian yang arus *output*-nya terlalu kecil sehingga tidak mampu untuk mengemudikan *relay*. Hal tersebut memerlukan ditambahnya *driver relay*. *Driver relay* ini merupakan penguat arus dan tegangan, yaitu menguatkan arus dan tegangan yang terlampau kecil menjadi cukup kuat untuk dapat mengaktifkan koil *relay* sehingga *relay* dapat bekerja.

Driver relay yang sering digunakan adalah menggunakan transistor sebagai penguat. Menggunakan transistor agak rumit digunakan karena harus memperhitungkan besarnya arus dan rangkaian yang digunakan kurang effisien; terdapat resistor, transistor dan diperlukan dioda sebagai proteksi transistor terhadap tegangan *kick-back* dari beban induktif yaitu koil dari *relay*.



Gambar 2-17 ULN 2003A

Fungsi dari transistor sekarang dapat digantikan oleh sebuah IC yang berisi *darlington array*. IC ini mampu mengemudikan beban induktif dangan kapasitas arus dan tegangan yang besar hingga 500 mA, 30V. Tipe dari IC ini adalah ULN2003AN. Kelebihan yang dimilikinya adalah :

- Praktis dalam penggunaannya, dibandingkan dengan menggunakan transistor.
- Arus beban outputnya masing-masing mampu hingga 500 mA.
- Tegangan outputnya dapat mencapai 30 volt.
- Outputnya telah dilengkapi oleh *clamp dioda* sebagai proteksi terhadap tegangan kick-back dari beban induktif.
- Kemampuan menge-drive relay dan motor.
- Inputnya mampu menerima semua jenis logic dengan arus yang kecil.
- Dalam satu IC ULN2003AN, terdapat 7 buah rangkaian *darlington array* yang dapat digunakan secara bersamaan,.

BAB III

PERANCANGAN DAN PEMBUATAN ALAT

Dalam bab ini akan dibahas perancangan dan pembuatan alat. Pembahasan akan dilakukan pada setiap blok rangkaian, cara kerja masing-masing blok rangkaian dan fungsi masing-masing blok rangkaian tersebut. Secara garis besar terdapat dua bagian perangkat yang ada yaitu :

1. Perancangan perangkat keras *(Hardware).*
2. Perancangan perangkat lunak *(Software).*

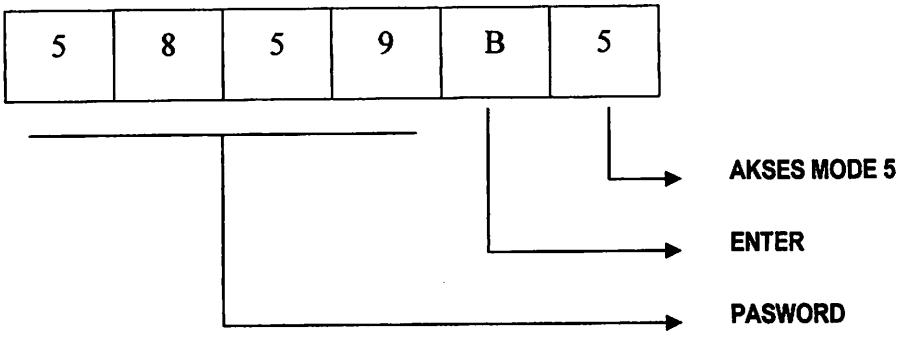
Pada perancangan perangkat keras akan meliputi seluruh *peripheral* yang digunakan pada sistem ini. Pada perancangan perangkat lunak akan meliputi diagram alir dan *software* secara umum. Akan tetapi kedua perangkat ini dalam kerjanya akan saling menunjang satu sama lain.

Perancangan dan pembuatan sistem kontrol *traffic light* jarak jauh dengan memanfaatkan radio HT (*Handy Talky*), ini meliputi beberapa tahapan perencanaan yang nantinya diharapkan akan terwujud sesuai dengan hasil yang dikehendaki dengan menitikberatkan segi daya guna, estetika dan kemungkinan pengembangan.

Dalam bab ini, akan membahas perencanaan perangkat keras yang digunakan sebagai penunjang sistem kontrol *traffic light* dengan menggunakan media radio HT (*Handy Talky*) dan pembahasan mengenai perangkat lunak yang berperan sebagai pengatur kerja sistem secara keseluruhan.

Konsep pengaturan yang ditetapkan pada sistem kontrol *traffic light* jarak jauh dengan menggunakan radio HT (*Handy Talky*) adalah sebagai berikut; Direncanakan terdapat 1 (satu) perempatan, dengan terdapat 2 (dua) jalur berlawanan pada tiap sisi jalan dan sistem yang dikendalikan adalah sistem *traffic light standalone.* Sistem kontrol terlebih dahulu akan masuk ke dalam sistem keamanan (*security*), kemudian masuk ke dalam sistem akses kondisi lampu *traffic light*. Pada sistem keamanannya, digunakan 4 (empat) kombinasi angka.

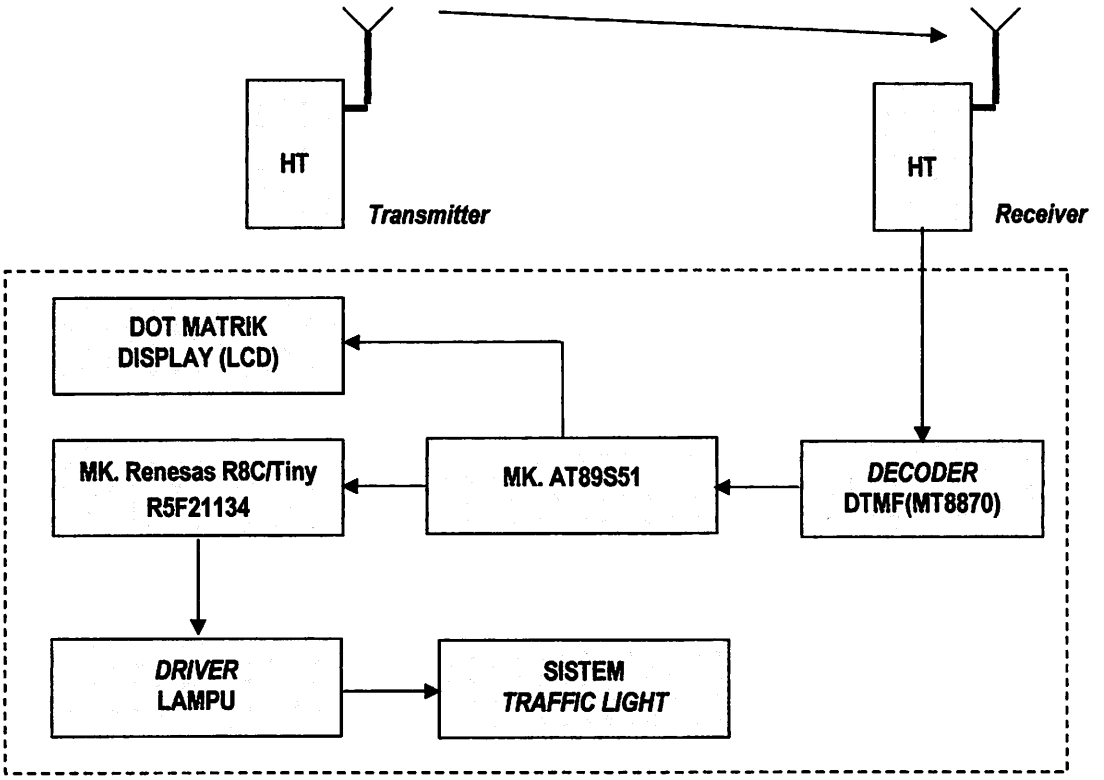
Kombinasi angka yang dimasukkan ke dalam sistem kontrol *traffic light* jarak jauh ini adalah 4 (empat) angka, sebagai pasword, 1 (satu) karakter sebagai akses masuk (enter) dan 1 (satu) angka sebagai pilihan dari akses kondisi lampu *traffic light*.



Tugas untuk sistem yang direncanakan adalah ;

1. Pada kondisi awal, sistem *traffic light* bekerja pada kondisi normal.
2. Sistem menunggu perintah (lewat radio HT), dimana perintah ini berupa nada *tone* DTMF, yang dipakai untuk mengendalikan sistem *traffic light* pada keadaan atau kondisi tertentu.

3.1 Diagram Blok Perangkat Keras



Gambar 3-1 Diagram Blok Keseluruhan Sistem

Fungsi dari tiap-tiap blok diagram dijelaskan sebagai berikut :

- **HT (*Handy Talky*)**

  Berfungsi sebagai media penghubung antara sistem kontrol dengan sistem kerja *traffic light*. Terdapat 2 (dua) HT (Handy Talky) yang digunakan, yaitu HT Alinco DJ-180 sebagai HT *Transmiiter* (pengirim sinyal *tone* DTMF) dan HT ICOM IC-2N sebagai HT *Receiver* (penerima sinyal DTMF).

- ***Decoder* DTMF**

  Berfungsi untuk mengubah data *tone* DTMF yang diterima oleh HT *received*, menjadi kode biner 4 bit yang kemudian data biner tersebut akan dieksekusi oleh mikrokontroler. *Decoder* DTMF yang digunakan adalah *Decoder* DTMF MT 8870.

- **Mikrokontroler Renesas R8C/Tiny**

  Berfungsi sebagai pengatur dari sistem kerja kondisi lampu *traffic light*.

- **Mikrokontroler AT89S51**

  Berfungsi sebagai pengendali utama dan proses pengiriman data berupa pesan ke dalam bentuk display LCD dot matrik.

- **LCD Dot matrik *display***

  Berfungsi menampilkan sistem keamanan (pasword), petunjuk arah dan pesan pada kondisi *traffic light* tertentu.

- **Driver Lampu**

  Berfungsi sebagai *driver* untuk mengatur sistem *traffic light*.

3.2 Perencanaan Perangkat Keras (*Hardware*)

Bagian ini, menguraikan perancanaan perangkat keras yang meliputi ;

a. Sistem *Decoder* DTMF.

b. Mikrokontroler Renesas R8C/Tiny.

c. Mikrokontroler AT89S51.

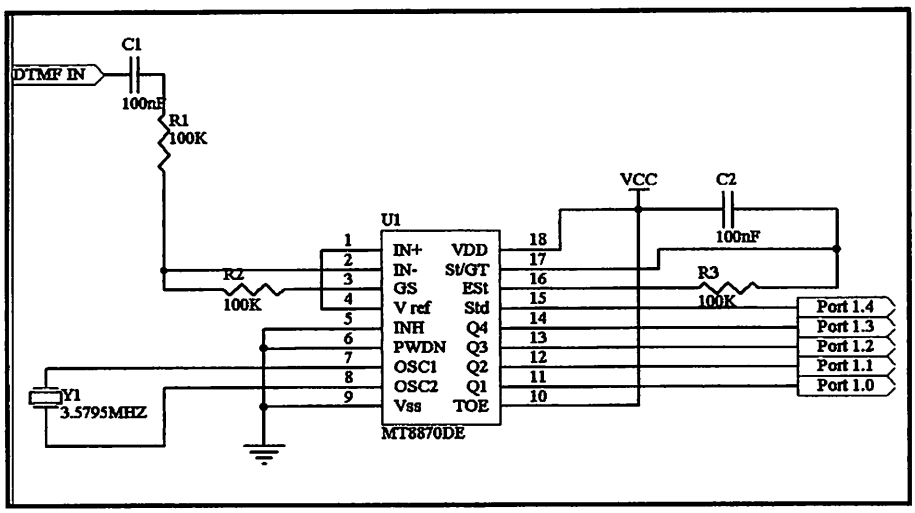
d. Triac (Sistem saklar /driver lampu).

e. LCD (*Liquid Crystal Display*)

f. *Relay* dan *Drive Relay*.

3.2.1 Rangkaian *Decoder* DTMF

Rangkaian *decoder* DTMF ini berfugsi untuk merubah sinyal nada *tone* yang dikirimkan menjadi bilangan biner 4 bit agar dapat diproses oleh mikrokontroler. Dalam perancangan ini dipilih rangkaian *decoder*, dengan menggunakan IC MT 8870 karena hanya memerlukan rangkaian eksternal yang sedikit.



Gambar 3-2 Rangkaian *Decoder* DTMF MT 8870

Kapasitor pada masukan IC berfungsi sebagai kopling dan penahan sinyal DC agar tidak masuk ke dalam rangkaian, R_2 merupakan resistor umpan balik akan menentukan penguatan dari rangkaian penerima DTMF sama dengan 1. Besar nilai R_2 sama dengan nilai R_1 untuk menghasilkan penguatan tegangan 1

Besarnya nilai $R_2 = R_1$ sesuai dengan karakteristik IC MT 8870 adalah 100 KΩ. Penguatan tegangan IC MT 8870 adalah :

$$A_V = R_2 / R_1$$

$$= 100\ K\Omega / 100K\Omega$$

$$= 1 \text{ kali}$$

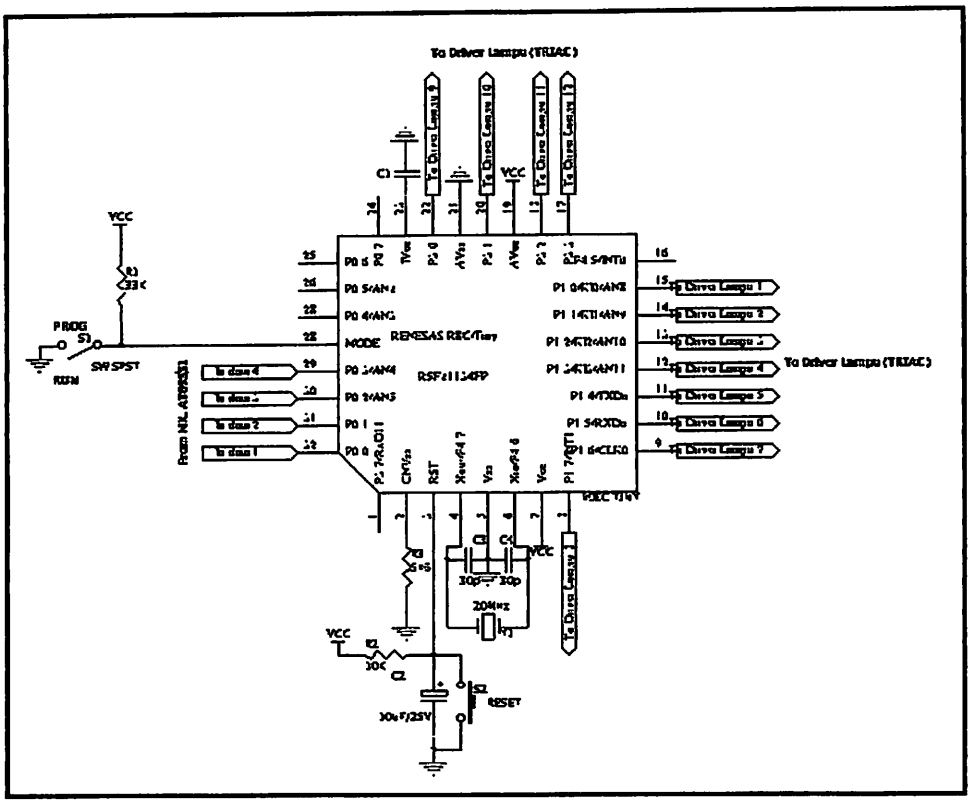
Jadi penguatan yang digunakan adalah sebesar 1 kali

Tabel 3-1. Tabel Kombinasi *Decoder* DTMF MT 8870

DIGIT	TOE	INH	Est	Q4	Q3	Q2	Q1
ANY	L	X	H	Z	Z	Z	Z
1	H	X	H	0	0	0	1
2	H	X	H	0	0	1	0
3	H	X	H	0	0	1	1
4	H	X	H	0	1	0	0
5	H	X	H	0	1	0	1
6	H	X	H	0	1	1	0
7	H	X	H	0	1	1	1
8	H	X	H	1	0	0	0
9	H	X	H	1	0	0	1
0	H	X	H	1	0	1	0
*	H	X	H	1	0	1	1
#	H	X	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMPEDANCE, X = DON'T CARE

3.2.2 Rangkaian Minimum Sistem Mikrokontroler Renesas R8C/Tiny



Gambar 3-3 Rangkaian Minimum Sistem Renesas R8C/Tiny

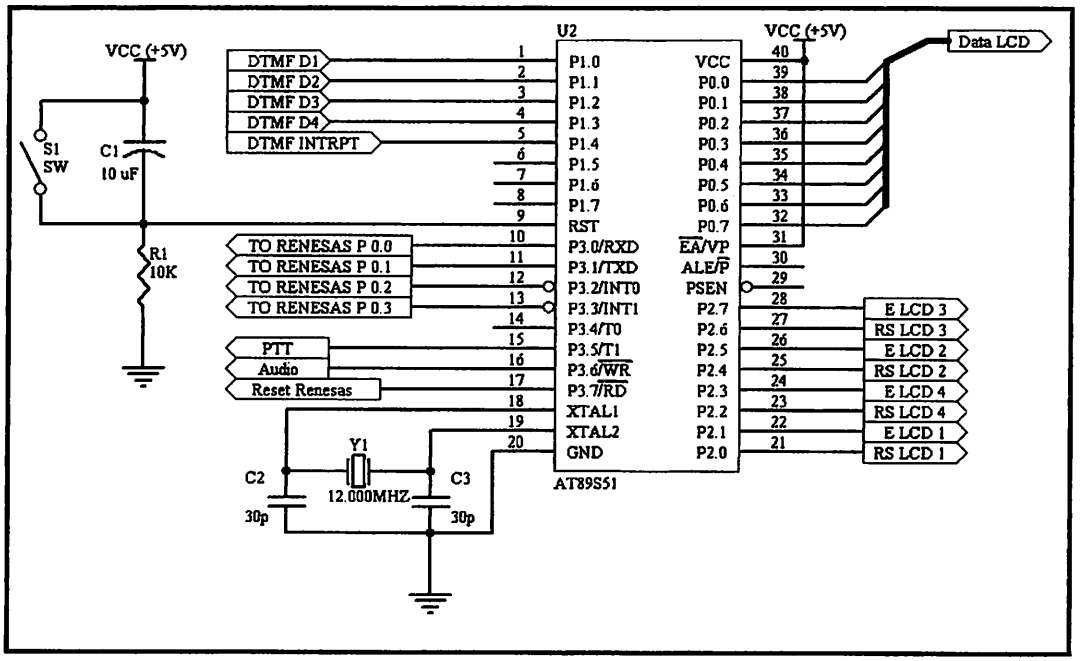
Mikrokontroler Renesas *R8C/Tiny* merupakan mikrokontroler yang berfungsi sebagai pengendali sistem lampu (kondisi lampu) *traffic light.* Mikrokontroler ini mempunyai I/O Port yaitu P0.0 – P0.7, P1.0 – P1.7, P3.0 – P3.3, P3.7 dan P4.5 sedangkan P4.6, P4.7 hanya bisa digunakan sebagai *input* saja, bila konfigurasi kristal memakai kristal *internal.* Dalam hal ini yang digunakan Port I/O saja. Berikut adalah konfigurasi pin-pin mikrokontroler R8C/Tiny:

- Port 0.0 – port 0.4 digunakan sebagai masukan data 4 bit dari mikrokontroler pengendali AT89S51 (port 3.0 – port 3.3).

- Port 1.0 – port 1.7 dan port 3.0 - port 3.3 digunakan sebagai masukan untuk mengaktifkan kerja sistem lampu *traffic light.*

3.2.3 Rangkaian Minimum Sistem Mikrokontroler AT89S51

Pada sistem kontrol ini digunakan mikrokontroler (AT89S51) sebagai pusat dari pengolah data dan pengendali seluruh kerja rangkaian. Sebagai otak dari pengolah data dan pengkontrol alat, pin-pin AT89S51 dihubungkan pada rangkaian pendukung membentuk suatu minimum sistem seperti dalam Gambar 3-4.



Gambar 3-4 Rangkaian Minimum Sistem AT89S51

Pin - pin pada keping mikrokontroler AT89S51 pada perancangan alat ini dialokasikan penggunaannya sebagai berikut:

a. Port I/O mikrokontroler AT89S51

- Port 0
  - Port 0.3 - Port 0.7 digunakan sebagai data LCD.
- Port 1
  - Port 1.0-Port 1.3 digunakan sebagai data input 4 bit dari d*ecoder* DTMF
  - Port 1.4 digunakan sebagai data interupt dari d*ecoder* DTMF.
- Port 2
  - Port 2.0 digunakan sebagai data input ke RS LCD 1.
  - Port 2.1 digunakan sebagai data input ke E LCD 1.
  - Port 2.2 digunakan sebagai data input ke RS LCD 4.
  - Port 2.3 digunakan sebagai data input ke E LCD 4.
  - Port 2.4 digunakan sebagai data input ke RS LCD 2.
  - Port 2.5 digunakan sebagai data input ke E LCD 2.
  - Port 2.6 digunakan sebagai data input ke RS LCD 3.
  - Port 2.7 digunakan sebagai data input ke E LCD 3.
- Port 3
  - Port 3.0 – Port 3.3 digunakan sebagai jalur input ke mikrokontroler Renesas.
  - Port 3.5 digunakan sebagai jalur untuk mengaktifkan sistem umpan balik, berupa *tone* suara (PTT).
  - Port 3.6 digunakan sebagai bit sinyal audio jika pasword sistem salah dimasukkan.

- Port 3.7 digunakan sebagai jalur untuk mengaktifkan reset mikrokontroler Renesas.

b. Pin RST (Reset, Pin 9) dihubungkan dengan keluaran rangkaian reset.

c. Pin XTAL1 dan XTAL2 (Pin 19 dan 18) dihubungkan dengan sebuah rangkaian penggerak osilator internal yang dimiliki AT89S51.

d. Pin $\overline{EA}$ (Pin 31) dihubungkan ke Vcc agar mikrokontroler mengakses program dari EPROM internal.

e. Pin Vcc (Pin 40) dihubungkan dengan rangkaian catu daya +5V.

f. Pin GND (Pin 20) dihubungkan dengan Ground rangkaian catu daya.

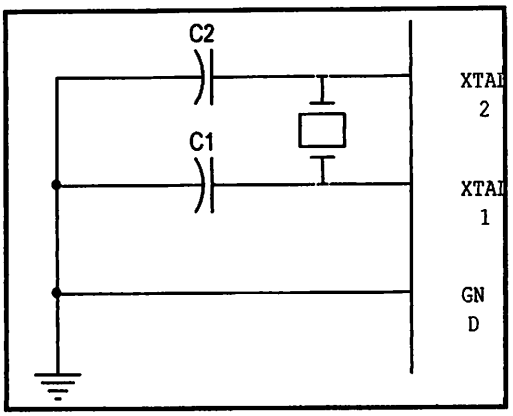
3.2.3.1 Rangkaian Osilator

Mikrokontroler AT89S51 ini memiliki internal *clock generator* yang berfungsi sebagai sumber *clock*, tetapi masih diperlukan rangkaian tambahan untuk membangkitkan *clock* tersebut. Rangkaian ini terdiri dari 2 buah kapasitor dan sebuah kristal dengan ketentuan:

C1 dan C2 = 20 pF – 40 pF untuk kristal

= 30 pF – 50 pF untuk keramik resonator

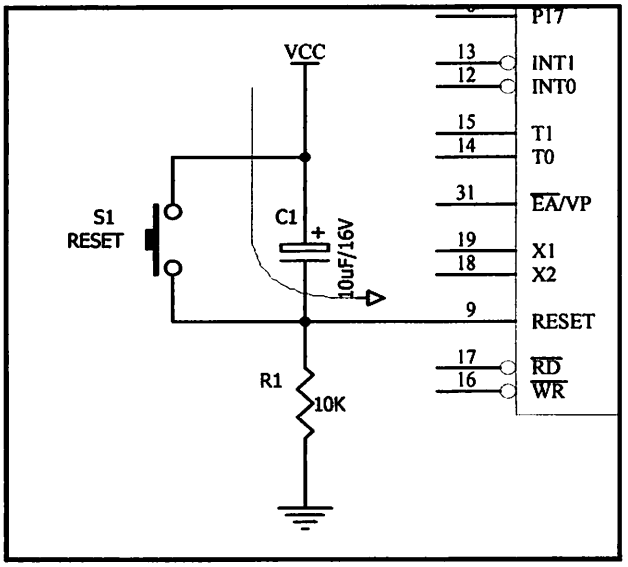
Dalam perencanaan rangkaian mikrokontroler ini digunakan kapasitor sebesar 30 pF.



Gambar 3-5 Rangkaian Clock

3.2.3.2 Rangkaian Reset

Mikrokontroler AT89S51 dapat bekerja jika ada rangkaian resetnya. AT89S51 memakai reset aktif *high* sehingga *input* reset harus tinggi minimal selama 2 siklus mesin (24 periode osilator) saat pertama kali mikrokontroler AT89S51 dijalankan. Rangkaian reset terdiri atas resistor dan kapasitor yang dihubungkan ke kaki 9 pada mikrokontroler AT89S51.



Gambar 3-6 Rangkaian Reset

Karena kristal yang digunakan mempunyai frekuensi sebesar 12 MHz maka satu periode membutuhkan waktu sebesar :

$$T = \frac{1}{f_{XTALL}} = \frac{1}{12\,MHz} s = 8.333 \cdot 10^{-8} s$$

Sehingga waktu minimal logika tinggi yang dibutuhkan untuk m*ereset* mikrokontroler adalah :

$$\begin{aligned} t_{reset(\min)} &= T \times \text{ periode yang dibutuhkan} \\ &= 8{,}333 \cdot 10^{-8} \times 24 \\ &= 2\,\mu S \end{aligned}$$

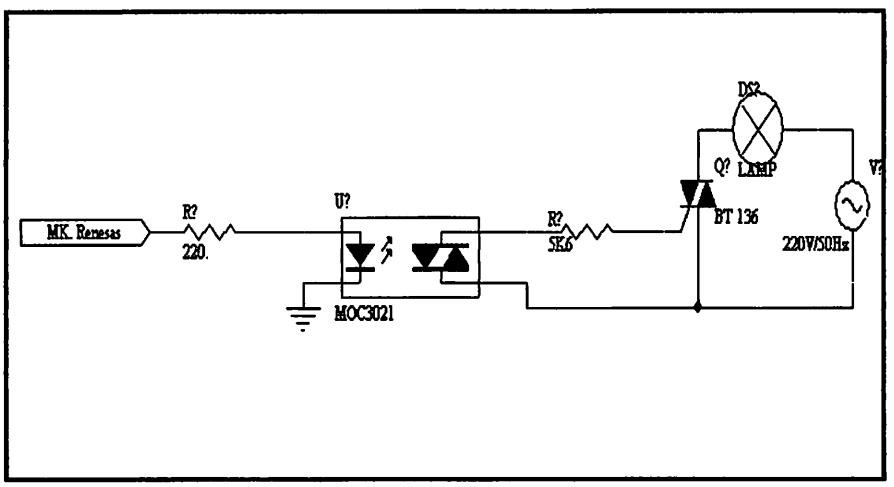
Jadi mikrokontroler membutuhkan waktu minimal 2 μs untuk m*ereset.* Waktu minimal inilah yang dijadikan pedoman untuk menentukan nilai R dan C. Dengan menentukan nilai R = 10 KΩ dan *t* sebesar 0,035detik. Nilai *t* lebih besar daripada 2 × 10^{-6} detik sehingga rangkaian tersebut dapat digunakan untuk me-*reset* mikrokontroler. Tombol tekan *push-button* digunakan untuk me-*reset* mikrokontroler tanpa perlu melepaskan catu daya.

$$\begin{aligned} t &= 0{,}357 \cdot R \cdot C \\ 35 \cdot 10^{-3} &= 0{,}357 \cdot 10 \cdot 10^{3} C \\ C &= 9{,}8 \cdot 10^{-6} F \end{aligned}$$

Jadi dengan nilai komponen R = 10 KΩ nilai kapasitor yang dapat memenuhi syarat untuk m*ereset* mikrokontroler harus diatas 9,8 μF. Untuk kemudahan perancangan dipilih C = 10 μF.

3.2.4 *Driver* Lampu

Driver lampu pada rancangan ini, difungsikan sebagai penyambung antara mikrokontroler dengan peralatan luar. Secara langsung mikrokonroler sebagai rangkaian digital dengan tegangan DC maksimal sebesar ± 5 volt, tidak mampu mengendalikan output beban besar dengan tegangan sumber AC 220 volt. Penggunaan driver ini membantu mikrokontroler dalam mengendalikan beban dengan sumber tegangan AC dengan tepat. Rangkaian driver ini disusun dari sebuah komponen optotriac dengan tipe MOC 3021 sebagai isolator antara tegangan tinggi 220 volt AC dengan tegangan DC 5 volt dari mikrokontroler dan triac tipe BT 136 sebagai saklar yang menghubungkan beban dengan tegangan 220 volt. MOC 3021 dipicu oleh output dari mikrokontroler ±5 volt sehingga mampu mengaktifkan triac BT 136 sebagai saklar pada tegangan 220 volt.



Gambar 3-7 Rangkaian *Driver* Lampu

Tegangan output maksimal dari mikrokontroler adalah 5 Volt sedangkan untuk lampu *traffic light* digunakan *supply* $220V_{AC}$, maka diperlukan rangkaian *driver* untuk mengendalikannya. Rangkaian *driver* yang dipakai berupa optotriac MOC 3021 dan Triac BT 136, untuk analisa data yang digunakan:

Vin = 5 Volt

Untuk mengaktifkan MOC 3021:

V_F (tegangan forward dioda) = 1,5 Volt

I_{FT} (arus forward Trigger) = 15 mA

Maka untuk mengaktifkan optotriac, resistor yang dipasang:

$$R = \frac{V_{in} - V_F}{I_{FT}}$$

$$R = \frac{5V - 1{,}5V}{15mA}$$

$$R = \frac{3{,}5V}{15mA}$$

$$R = 233\ \Omega$$

Karena nilai resistor 233 Ω tidak ada dipasaran, maka digunakan resistor yang mendekati yaitu 220 Ω.

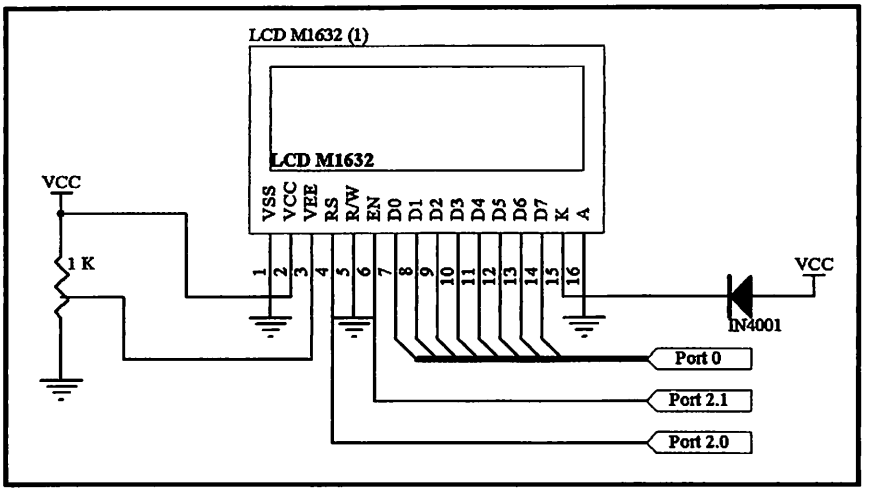
Karena tegangan jaringan yang digunakan adalah 220V dan arus gate maksimum (I_{GTM}) adalah 35 mA, maka total nilai R adalah :

$$R = \frac{V_{jaringan}}{I_{GTM}} = \frac{220}{35.10^{-3}} = 6{,}3K\Omega$$

Karena nilai resistor 6,3 KΩ tidak ada dipasaran, maka digunakan resistor yang mendekati yaitu 5,6 KΩ.

3.2.5 Rangkaian LCD (*Liquid Crystal Display*)

LCD dalam perencanaan sistem kontrol ini digunakan sebagai penampil sistem keamanan (password), penunjuk arah dan penampil pesan pada kondisi *traffic light* tertentu. Gambar rangkaian LCD ditunjukkan pada gambar berikut :



Gambar 3-8 Rangkaian LCD (Liquid Crystal Display)

Untuk tampilan dipergunakan LCD Dot Matrik 2 x 16 karakter. Sinyal-sinyal yang diperlukan oleh LCD adalah RS dan Enable, sinyal RS dan Enable dipergunakan sebagai input yang outputnya dipakai untuk mengaktifkan LCD. LCD akan aktif apabila mikrokontroler memberikan instruksi tulis pada LCD. Saat kondisi RS don't care dan Enable 0 maka LCD tetap pada kondisi semula, pengiriman data ke LCD dilakukan saat RS berlogika 0 dan enable berlogika 1. Instruksi dikirim pada LCD bila keadaan RS 1 dan Enable 1. Pin LCD ini untuk data terkoneksi pada Port 0 mikrokontoler AT89S51. Kemudian untuk RS dihubungkan pada Port 2.0, tulis/baca (*Read/Write)* diberikan logika *low* karena

disini LCD bersifat menulis data, dan yang terakhir *Enable* (E) dikendalikan dengan Port 1.1. Gambar rangkaian LCD ditunjukkan pada gambar 3-8.

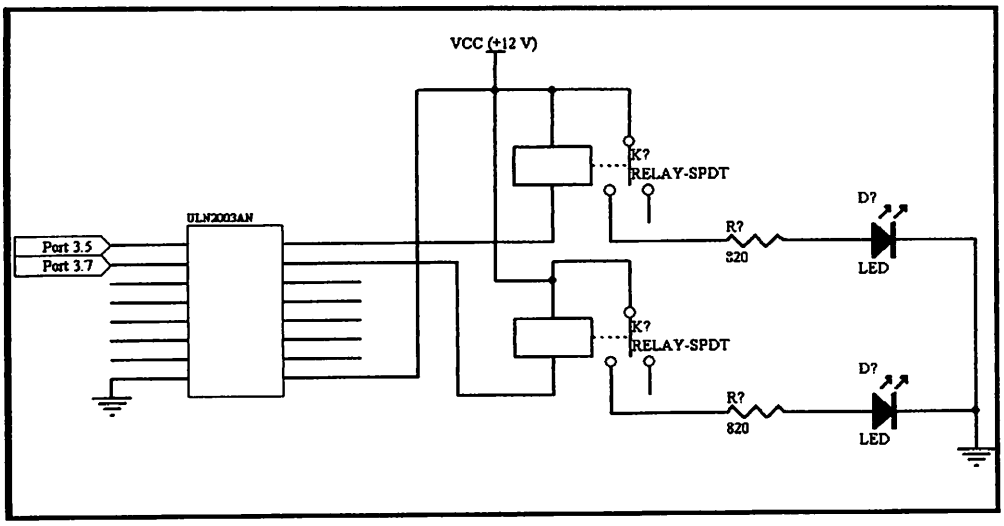
3.2.6 *Relay* dan *Driver Relay*

Untuk rangkaian *driver relay* digunakan IC ULN 2003A sebagai pengendali *relay* pada sistem reset dan PTT. Pada IC ULN 2003A dapat dipicu dengan tegangan 5 Volt dan arus maksimum sebesar 500mA dengan suhu kerja dari -20°C sampai 80°C. IC ULN2003A mampu menghidupkan dan mematikan *relay* yang hanya memiliki tegangan maksimal sebesar 12 Volt dengan resistansi kumparan sebesar 400 Ω jadi dapat diketahui arus *relay* sebesar :

$$\text{Dimana : } I_{relay} = \frac{V_{CC}}{R.relay}$$

$$= \frac{12}{400} = 30 \text{ mA}$$

Dengan adanya arus relay sebesar 30 mA maka IC ULN2003A dapat menggerakan *relay* tersebut karena ULN 2003A memiliki arus maksimum sebesar 500 mA sesuai dengan *data sheet*. Adapun rangkaian *driver relay* dapat dilihat pada gambar 3-9.

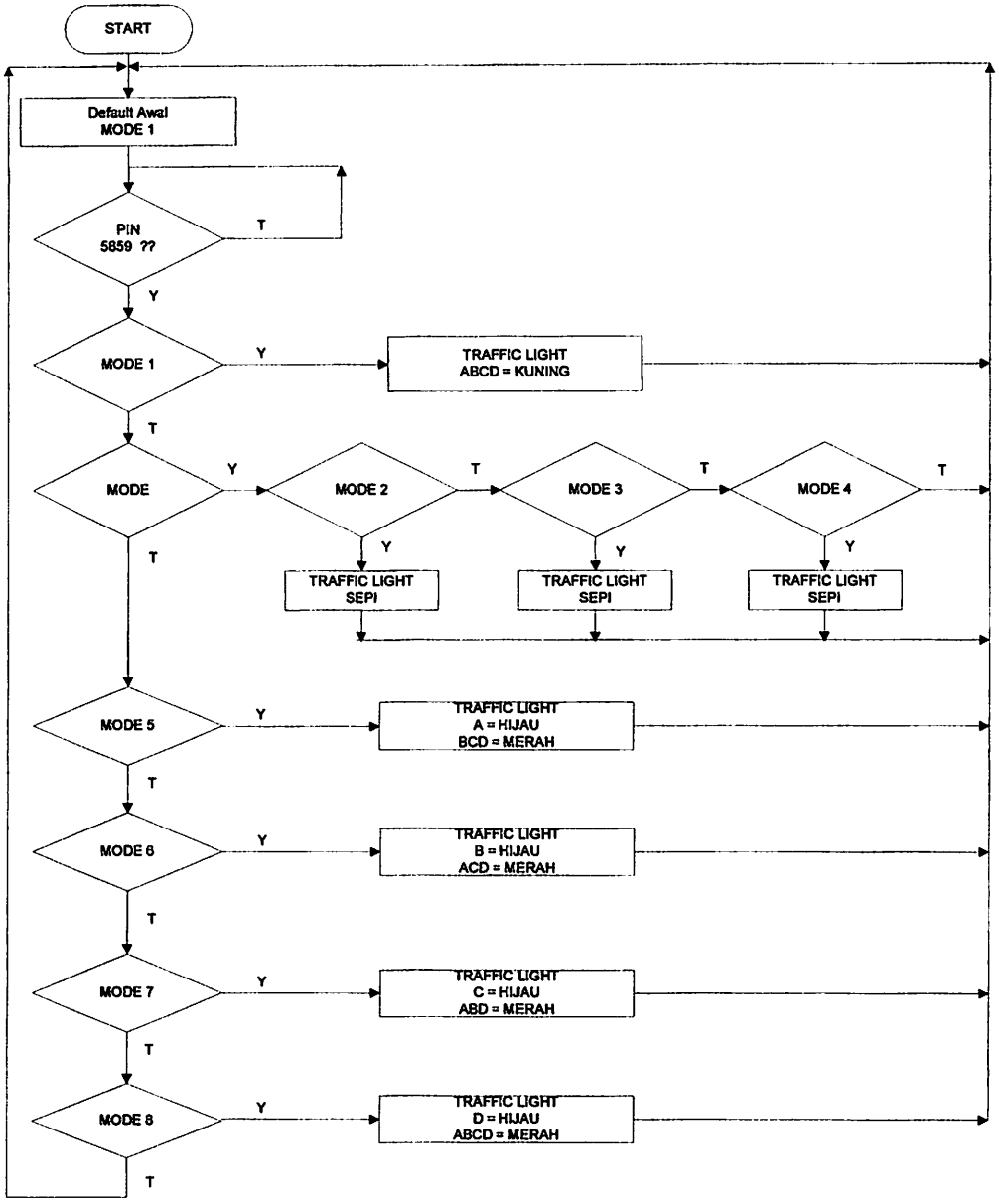


Gambar 3-9 Rangkaian ULN 2003A sebagai *driver relay*

Cara kerja dari rangkaian di atas adalah sebagai berikut :

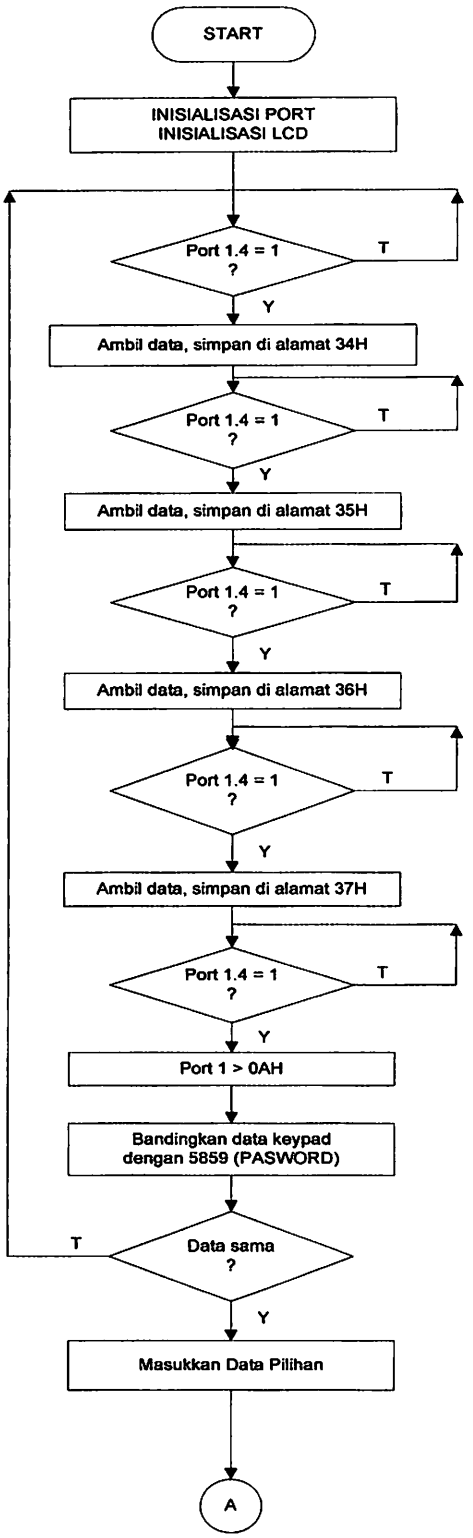
- Pin no 1 mendapat logika *high* (1), maka output IC ULN pada pin no 16 akan menjadi *low* (0). Akibatnya *relay* akan tercatu daya sehingga *relay* dalam keadaan ON.
- Pin no 1 mendapat logika *low* (0), maka output IC ULN pada pin no 16 akan menjadi *high* (1). Akibatnya *relay* tidak tercatu daya sehingga *relay* dalam keadaan OFF.

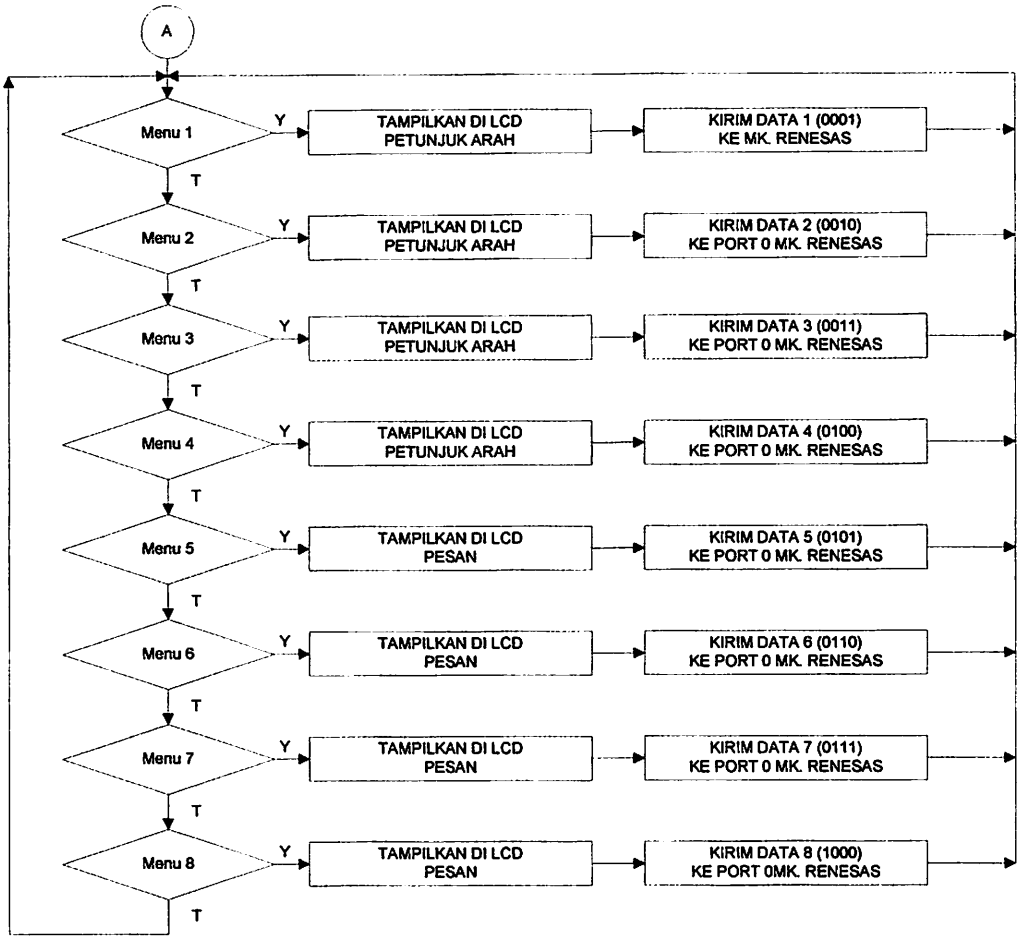
3.3.1 Diagram Alir Keseluruhan Sistem



Gambar 3-10 Flowchart Sistem Model Sistem Kontrol Traffic Light Sederhana

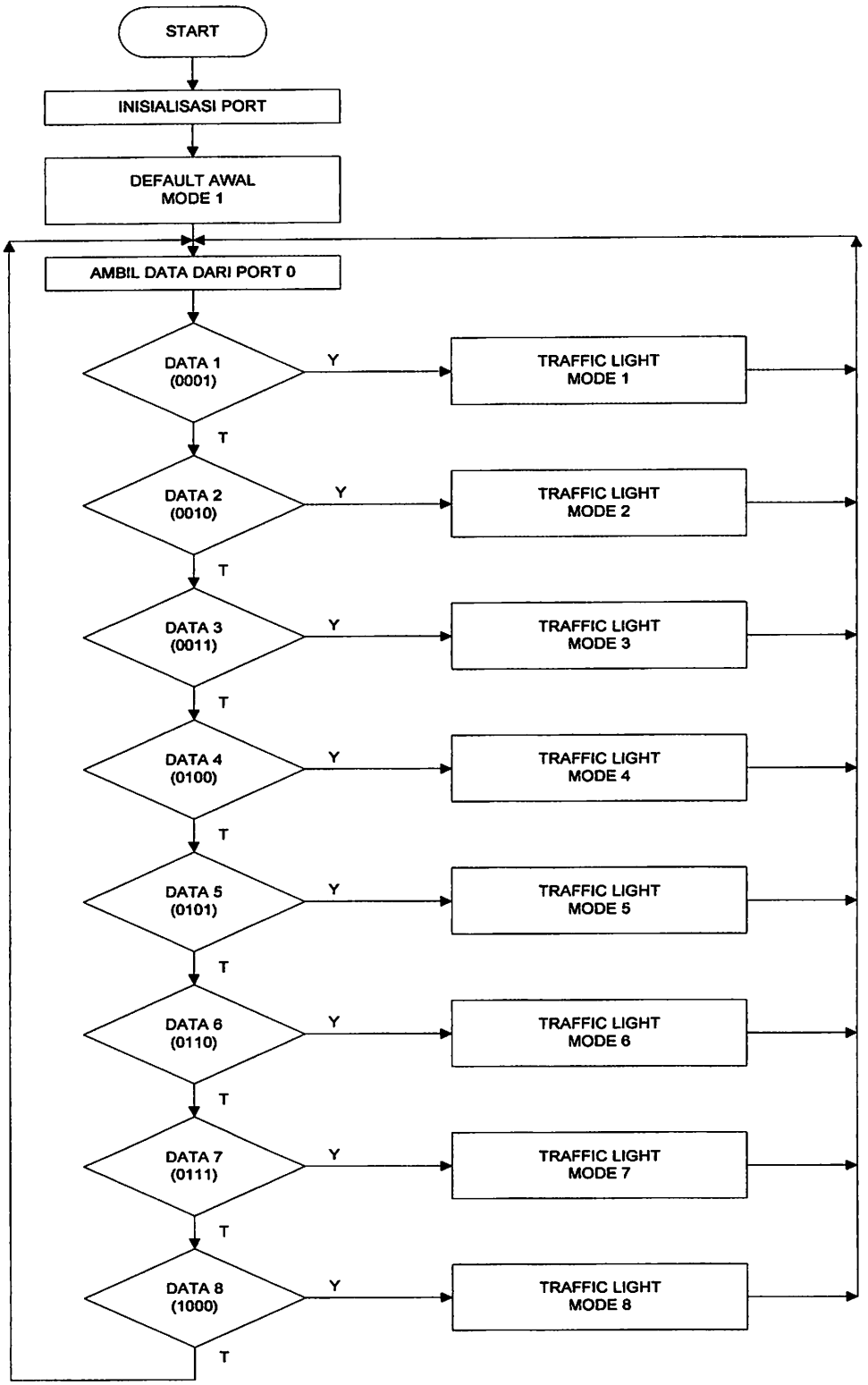
3.3.2 Diagram Alir Software Mikrokontroler AT89S51





Gambar 3-11 Flowchart Sistem Program Alur Utama MK. AT89S51

3.3.3 Diagram Alir Software Mikrokontroler Renesas R8C/Tiny



Gambar 3-12 Flowchart Sistem Program Alur Utama MK. Renesas R8C/Tiny

BAB IV

PENGUJIAN ALAT

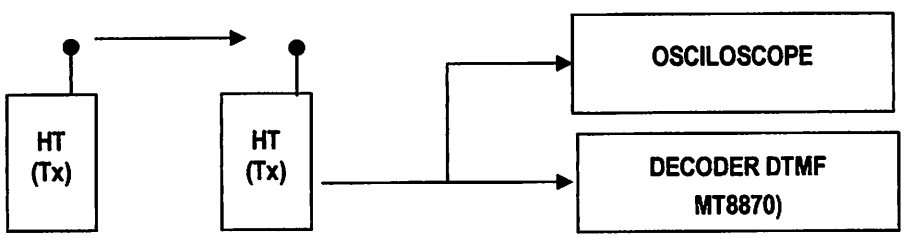
Tujuan dari pengujian ini adalah untuk mengetahui kerja dari sistem kontrol *traffic light* jarak jauh sesuai dengan perencanaan dan perancangan. Pengujian dilakukan melalui beberapa tahapan, yakni pengujian pada setiap blok serta pengujian pada sistem kontrol secara keseluruhan.

Pada tugas akhir ini pengujian alat dilakukan pada sub sistem meliputi ;

1. Pengujian Sinyal Input *Decoder* DTMF dan *Signal to Noise Ratio* (SNR).
2. Pengujian Output *Decoder* DTMF.
3. Pengujian Keseluruhan Sistem Kontrol.

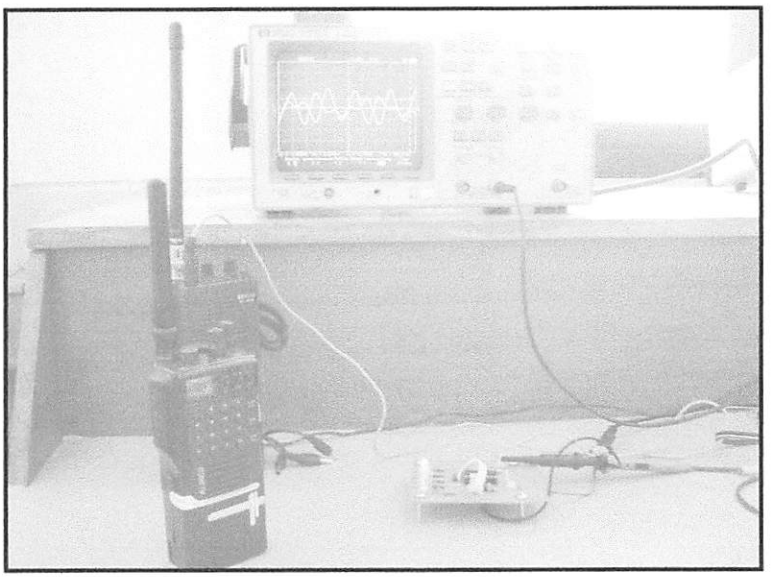
4.1 Pengujian Sinyal Input *Decoder* DTMF

Pengujian pada bagian ini bertujuan untuk mengetahui bentuk sinyal dan *error* penerimaan sinyal yang masuk ke dalam *decoder* DTMF MT 8870 serta nilai dari *Signal to Noise Ratio* (SNR).



Gambar 4-1 Blok Diagram Pengujian Sinyal Input *Decoder* DTMF

Pengujian yang dilakukan adalah seperti gambar 4-1, dimana informasi yang dikirim (*tone* DTMF) dari HT *Transmitter* (HT Alinco DJ-180) yang didalamnya terdapat proses *enkoder* dari *keypad* HT (*Touch Tone Signaling*) ke dalam sistem HT *Received* (HT ICOM IC-2N), kemudian masuk ke dalam rangkaian *decoder* DTMF MT 8870. Untuk mengamati sinyal dan *error* frekuensi yang masuk ke dalam *decoder* DTMF, maka digunakan *osciloscope*, sehingga dapat diperoleh bentuk sinyal input *decoder* DTMF dan frekuensi DTMF yang dikirimkan.



Gambar 4-2 Pengujian Sinyal Input *Decoder* DTMF

Tabel 4-1 Hasil Pengujian Sinyal Input *Decoder* DTMF

INPUT ENCODER	FREKUENSI KELUARAN				OUTPUT DECODER				ERROR (%)	
	STANDART DTMF (Hz)		PENGUKURAN (Hz)							
	F-High	F-Low	F-High	F-Low	D4	D3	D2	D1	F-High	F-Low
1	1209	697	1205	699,3	0	0	0	1	0,33	0,33
2	1336	697	1333	694,3	0	0	1	0	0,23	0,39
3	1477	697	1471	699,3	0	0	1	1	0,41	0,33
4	1209	770	1205	769,2	0	1	0	0	0,33	0,10
5	1336	770	1333	769,2	0	1	0	1	0,23	0,10
6	1477	770	1471	769,2	0	1	1	0	0,41	0,10
7	1209	852	1205	854,7	0	1	1	1	0,33	0,32
8	1336	852	1333	854,7	1	0	0	0	0,23	0,32
9	1477	852	1471	854,7	1	0	0	1	0,41	0,32
0	1336	941	1333	943,3	1	0	1	0	0,23	0,24
*	1209	941	1205	943,3	1	0	1	1	0,33	0,24
#	1477	941	1471	943,3	1	1	0	0	0,41	0,24
A	1633	697	1639	694,4	1	1	0	1	0,38	0,39
B	1633	770	1639	769,2	1	1	1	0	0,38	0,10
C	1633	852	1639	943,3	1	1	1	1	0,38	0,32
D	1633	941	1639	943,3	0	0	0	0	0,38	0,24

V/div = 500 mV
T/div = 500 µV
Volume HT (ICOM IC-2N) = ± 60 %

$$\% \; Error = \left| \frac{f.s\tan dart - f.pengukuran}{f.s\tan dart} \right| \times 100\%$$

$$\% \; Error_{(1)} = \left| \frac{1209 - 1205}{1209} \right| \times 100\% = 0{,}33\%$$

$$\% \; Error_{(1)} = \left| \frac{697 - 699.3}{697} \right| \times 100\% = 0{,}33\%$$

Signal to Noise Ratio (SNR) adalah perbandingan sinyal data yang ditransmisikan terhadap sinyal *noise* yang terjadi pada radio penerima (*receiver*).

Tabel 4-2 Hasil Pengujian *Signal to Noise Ratio* (SNR)

DIGIT	INPUT				PENGUKURAN V_{P-P} (volt)	PERHITUNGAN SNR (dB)
	D4	D3	D2	D1		
1	0	0	0	1	2,375	43,00
2	0	0	1	0	2,547	43,61
3	0	0	1	1	2,156	42,17
4	0	1	0	0	2,266	42,60
5	0	1	0	1	2,188	42,30
6	0	1	1	0	2,078	41,85
7	0	1	1	1	2,156	42,17
8	1	0	0	0	2,063	41,80
9	1	0	0	1	1,984	41,44
0	1	0	1	0	1,969	41,38
*	1	0	1	1	2,063	41,80
#	1	1	0	0	1,953	41,31
A	1	1	0	1	2,078	41,85
B	1	1	1	0	2,047	41,71
C	1	1	1	1	1,875	40,95
D	0	0	0	0	1,828	40,73
Σ						670,67

V_{RMS} (V_{NOISE}) = 5,940 mV (pengukuran saat sinyal *OFF*)

V/div = 500 mV

T/div = 1 mS

Volume HT (ICOM IC-2N) = ± 60 %

$$SNR = 20\log\left(\frac{V_S}{V_N}\right) dB$$

$$SNR = \left(\frac{0.707 \,.\, V_P}{V_N}\right) dB \qquad V_P = \frac{V_{P-P}}{2}$$

$$V_{P(1)} = \frac{V_{P-P}}{2} = \frac{2.375}{2} = 1{,}1875\ V$$

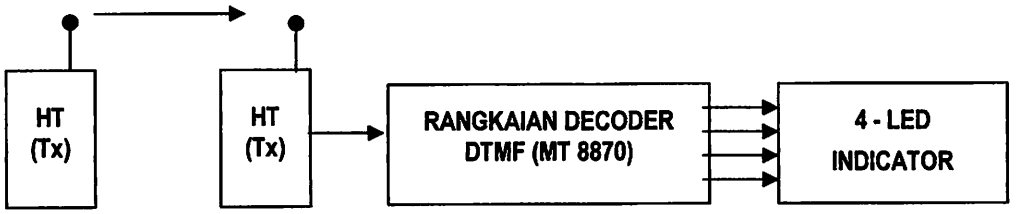
$$SNR_{(1)} = \left(\frac{0.707 \,.\, 1.1875}{5.940 \,.10^{-3}} \right) dB = 43 \; dB$$

$$SNR = \frac{\sum SNR}{\sum percobaan}$$

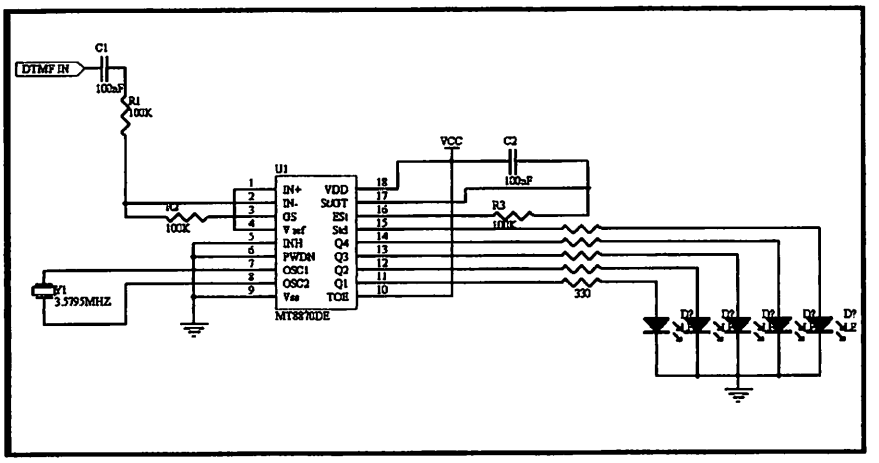
$$SNR_{RATA-RATA} = \frac{670.67}{16} = 41{,}92 \, dB$$

4.2 Pengujian Output *Decoder* DTMF.

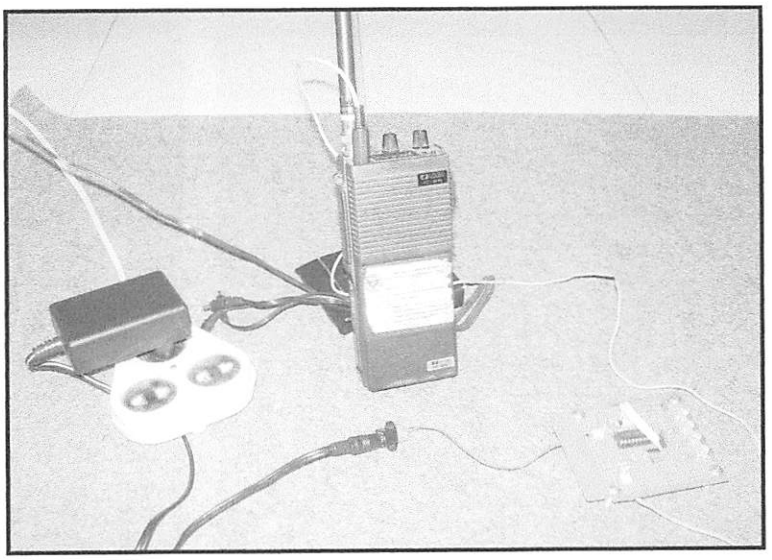
Pengujian pada bagian ini untuk mengetahui kerja rangkaian *decoder* DTMF MT 8870, sehingga dapat menerima *tone* dari HT (*Handy Talky*) pengirim informasi (berupa *tone* DTMF) dan menterjemahkan dalam bentuk data biner 4 bit (ditampilkan oleh *indicator* LED)



Gambar 4-3 Blok Diagram Pengujian Output *Decoder* DTMF



Gambar 4-4 Rangkaian Pengujian Output *Decoder* DTMF



Gambar 4-5 Pengujian Output *Decoder* DTMF

Tabel 4-3 Hasil Pengujian Rangkaian Output *Decoder* DTMF

DATA INPUT							DATA OUTPUT			
KEY	F_{HIGH}	F_{LOW}	D4	D3	D2	D1	D4	D3	D2	D1
1	1209	697	0	0	0	1	0	0	0	1
2	1336	697	0	0	1	0	0	0	1	0
3	1477	697	0	0	1	1	0	0	1	1
4	1209	770	0	1	0	0	0	1	0	0
5	1336	770	0	1	0	1	0	1	0	1
6	1477	770	0	1	1	0	0	1	1	0
7	1209	852	0	1	1	1	0	1	1	1
8	1336	852	1	0	0	0	1	0	0	0
9	1477	852	1	0	0	1	1	0	0	1
0	1336	941	1	0	1	0	1	0	1	0
*	1209	941	1	0	1	1	1	0	1	1
#	1477	941	1	1	0	0	1	1	0	0
A	1633	697	1	1	0	1	1	1	0	1
B	1633	770	1	1	1	0	1	1	1	0
C	1633	852	1	1	1	1	1	1	1	1
D	1633	941	0	0	0	0	0	0	0	0

Keterangan ;
LED menyala = 1 ; LED mati = 0

4.3 Pengujian Keseluruhan Sistem Kontrol

Setelah blok-blok sistem diuji dan menunjukkan unjuk kerja sesuai dengan data perintah yang dikirim dan berfungsi dengan baik, maka akan diuji kan keseluruhan dari sistem kontrol *traffic light* jarak jauh dengan menggunakan media HT (*Handy Talky*), baik secara *hardware* serta *software*-nya, meliputi;

1. Pengujian untuk sistem pengamanan (*security*).
2. Pengujian fungsi dari pengendalian (sistem kontrol).
3. Pengujian jarak kontrol sistem.

Alat harus dapat mengeksekusi perintah dari HT *Transmitter* (HT Alinco DJ-180) dan diterima oleh *HT Receiver* (HT ICOM IC-2N), yang kemudian dieksekusi dalam bentuk perubahan pada kondisi lampu *traffic light*.

Sistem kerja dari sistem kontrol *traffic light* ini adalah ;

a. HT Alinco DJ 180 digunakan sebagai input utama (perintah) dari sistem pengontrolan, dengan mengunakan sistem pengiriman *tone* DTMF.
b. HT ICOM IC-2N digunakan sebegai media penerima dari input (perintah), yang akan menghubungkan dengan rangkaian sebagai hasilnya ditunjukkan oleh perubahan kondisi sistem *traffic light*.
c. Data yang diterima akan di-cek kesesuaiannya dengan pasword yang telah ditentukan (sebagai sistem kendali keamanan) untuk masuk dalam sistem kontrol *traffic light* tersebut ; jika benar maka sistem akan bekerja dan masuk ke dalam sistem kode akses *traffic light* yang akan diinginkan, dan jika pasword yang dimasukkan salah maka sistem akan memberikan

umpan balik berupa *tone* suara sebagai tanda bahwa sistem menolak untuk mengeksekusi perintah serta sistem akan bekerja pada kondisi sebelum pasword dimasukan.

d. Jalur frekuensi yang digunakan pada kontrol sistem *traffic light* jarak jauh dengan menggunakan radio HT (*Handy Talky*) ini adalah 143,40 MHz

Tabel 4-4 Hasil Pengujian Sistem Kontrol Pengamanan Traffic Light

No.	KODE YANG DIKIRIM	RESPON
1.	Kondisi awal	Default pada mode 1 Jalur A – B – C – D = nyala kuning
2.	**5859 B 5**	Sistem telah terbuka, sistem dapat dikontrol sesuai dengan MODE 5
3.	**5858 A**	Sistem tetap tertutup, sistem tidak dapat mengeksekusi perintah yang dikirim.
4.	**2228 C**	Sistem tetap tertutup, sistem tidak dapat mengeksekusi perintah yang dikirim.

Tabel 4-5 Hasil Pengujian Sistem Kontrol Traffic Light

No.	KODE YANG DIKIRIM	RESPON
1.	**1**	Sistem mengeksekusi MODE 1
2.	**2**	Sistem mengeksekusi MODE 2
3.	**3**	Sistem mengeksekusi MODE 3
4.	**4**	Sistem mengeksekusi MODE 4
5.	**5**	Sistem mengeksekusi MODE 5
6.	**6**	Sistem mengeksekusi MODE 6
7.	**7**	Sistem mengeksekusi MODE 7
8.	**8**	Sistem mengeksekusi MODE 8

Tabel 4-6 Hasil Pengujian Waktu Sistem Kontrol Traffic Light

No.	PERCOBAAN	WAKTU (s)	KETERANGAN
1.	Password – benar **Password – benar + kode akses**	09 . 424 **13 . 730**	Sistem masuk
2.	Password – benar **Password – benar + kode akses**	08 . 575 **12 . 710**	Sistem masuk

Tabel 4-7. Hasil Pengujian Jarak Sistem Kontrol Traffic Light

NO.	JARAK (m)	POWER HT (H/L)	KETERANGAN
1.	± 5	L	Kirim : 5 kali Terima : 5 kali
2.	± 10	L	Kirim : 5 kali Terima : 5 kali
3.	± 50	L	Kirim : 5 kali Terima : 5 kali
4.	± 400	L	Kirim : 5 kali Terima : 5 kali
5.	± 1000	H/L	Kirim : 5 kali Terima : 3 kali

Dari hasil pengujian keseluruhan sistem kontrol *traffic light* jarak jauh dengan menggunakan media HT (*Handy Talky*), disimpulkan bahwa sistem kontrol ;

1. Waktu yang diperlukan untuk dapat mengendalikan sistem *traffic light* adalah ± 13 detik, sehingga sistem dapat bekerja sesuai dengan kondisi *traffic light* yang sedang terjadi.

2. Jarak yang dapat dicapai untuk dapat mengkontrol sistem *traffic light* adalah ± 1000 m (dengan keadaan *power HT* adalah *low*).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BAB V

PENUTUP

5.1 Kesimpulan

Penyusunan tugas akhir ini telah melalui tahapan perencanaan, pembuatan dan pengujian terhadap kerja dari kontrol sistem *traffic light*. Dalam pengujian tersebut disusun metode-metode pengujian yang terencana dan sistematis, sehingga didapatkan hasil pengujian yang dapat memberikan gambaran mengenai unjuk kerja sistem kontrol *traffic light* sesungguhnya.

Setelah melalui tahapan pengujian didapatkan kesimpulan ;

1. Pengujian SNR (*Signal to Noise Ratio*), didapat hasil pengukuran pada digit 1 yaitu tegangan output dengan sinyal V_{P-P} sebesar 2,375 V, sedangkan tegangan output tanpa sinyal sebesar 5,940 mV, sehingga nilai SNR pada digit 1 adalah sebesar 43 dB. SNR rata-rata dari keseluruhan pengujian adalah 41,92 dB.
2. Prosentase *error* dari sinyal input yang masuk ke dalam rangkaian *decoder* DTMF paling besar adalah 0,41%
3. Waktu yang diperlukan untuk dapat mengendalikan sistem *traffic light* adalah ± 13 detik.
4. Jarak yang dapat dicapai untuk dapat mengkontrol sistem *traffic light* adalah ± 1000 m (dengan keadaan power HT adalah low).

5.2 Saran

Dalam pembuatan skripsi ini masih terdapat beberapa kekurangan, sehingga untuk mencapai hasil yang lebih baik dan pengembangan lebih lanjut maka dapat diberikan saran – saran sebagai berikut :

1. Sebaiknya untuk pengembangan lebih lanjut, sistem kontrol *traffic light* dapat digunakan untuk lebih dari satu persimpangan jalan.
2. Dapat digunakan sistem *networking traffic light*, sehingga sistem dapat dikontrol secara tepusat.

LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

FORMULIR BIMBINGAN SKRIPSI

NAMA : ARDHIATAMA KUSUMAPUTRA
NIM : 02.17.056
Masa Bimbingan : 19 Juli 2006 – 19 Januari 2007
Judul Skripsi : Perancangan dan Pembuatan Sistem Kontrol *Traffic Light* Jarak Jauh Dengan Menggunakan Radio HT (*Handy Talky*).

No.	Tanggal	Uraian	Paraf Pembimbing
1.	5/6 06.	Pengidentifikasian masalah, pilih judul yg. lepas	
2.	11/7 06.	Lakukan pengujian Decoder & Encoder DTMF	
3.	25/7 06.	koordinasikan decoder DTMF & microcontroller.	
4.	14/8 06.	Bab IV, lakukan uji coba, kemudian tulis dlm Bab V	
5.	20/9 06.	Dari Bab IV & Bab V, tulis makalah seminar hasil.	
6.	11/10 06.	Bab III, menjelaskan secara detail ttg DTMF decoder.	
7.	24/11 06.	Uji ulang jarak terjauh utk low Power Radio HT	
8.	8/12 06.	Bab II, tambahkan teori ttg Sistem Elektronika.	
9.	29/01 07.	Bab I, tinjau kembali latar blk. batasan masalah.	
10.	14/3 07.	Persiapkan ujian komprehensif	

Malang, ...
Dosen Pembimbing

14/3 07.

Ir. Sidik Noertjahjono, MT
NIP. 1028700167

Form S- 4A

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Dari hasil ujian komprehensif jenjang Strata Satu (S-1) Jurusan Teknik Elektro, Konsentrasi Elektronika yang diselenggarakan pada:

Hari : **Sabtu**
Tanggal : **17 Maret 2007**

Telah dilakukan perbaikan skripsi oleh :

Nama : **Ardhiatama Kusumaputra**
N.I.M : **02.17.056**
Masa Bimbingan : **19 Juli 2006 – 19 Januari 2007**
Judul : **Perancangan Dan Pembuatan Sistem Kontrol Traffic Light Dengan Menggunakan Radio HT (Handy Talky)**

Perbaikan Meliputi :

No.	MATERI PERBAIKAN	PARAF DOSEN PENGUJI
1.	Rangkaian untuk kontrol reset Renesas dengan menggunakan relay	
2.	Spec. dari komunikasi HT yang dibuat	

Disetujui Oleh:

Dr. Cahyo Crysdian, MSc
Penguji Pertama

Mengetahui
Dosen Pembimbing

Ir. Sidik Noertjahjono, MT
NIP. 1028700167

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : ARDHIATAMA KUSUMA P.
N I M : 0217056.
Perbaikan meliputi :

(1) Ubah penulisan ~~[illegible]~~ unit kontrol ~~reset~~ [illegible] yg menggunakan relay

(2) Sebutkan spec dr komunikasi HT yg dibaca..

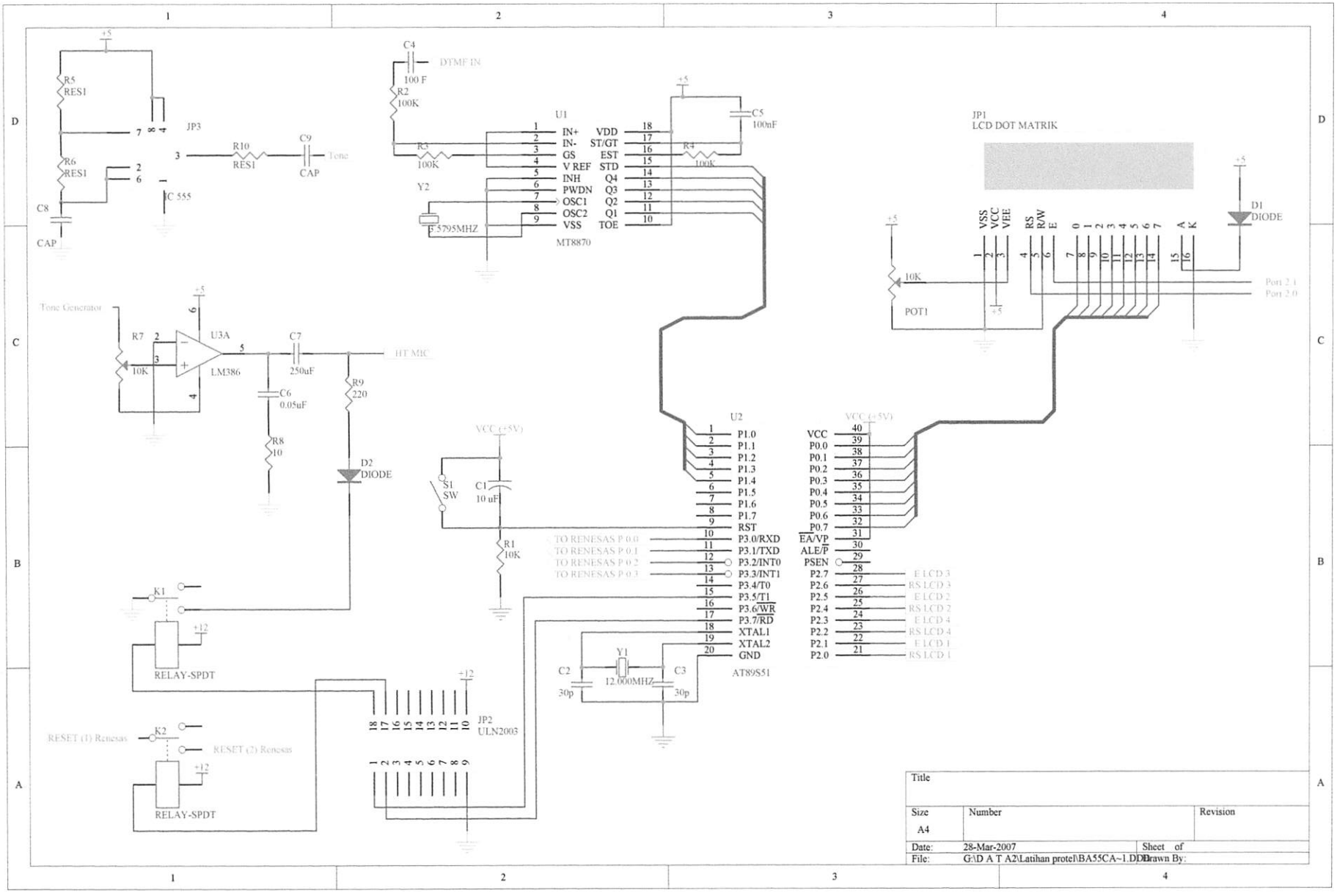
Malang, 17/3 - 2007.

(Dr. Cahyo Crysdian, MSc.)

Perancangan Dan Pembuatan Sistem Kontrol Traffic Light Jarak Jauh Dengan Menggunakan Radio HT (Handy Talky)

Spesifikasi :

1.	HT *Transmitter (Tx)*	Alinco DJ 180 Range Frequency : 137.00 – 173.99 MHz
2.	HT *Received (Rx)*	ICOM IC2N Range Frequency : 140.00 – 149.99 MHz
3.	Sistem Komunikasi HT $_{(Tx)}$→ HT$_{(Rx)}$	Sinyal DTMF (*Dual Tone Multifrequency*) + FM (*Frequency Modulation*)
4.	Jalur frekuensi yang digunakan	143,40 MHz
5.	Komunikasi HT$_{(Rx)}$ → Sistem *Traffic Light*	Sinyal DTMF (*Dual Tone Multifrequency*)
6.	*Decoder* Sinyal DTMF	MT 8870 ; sinyal DTMF → data biner (4 bit)
7.	Kontrol Sistem	MK. AT89S51 ; pusat kontrol MK. Renesas R8C/tiny ; *timer* lampu TL
8.	*Driver* Lampu *Traffic Light*	Optotriac : MOC 3021 Triac : BT 136
9.	Waktu pengendalian	± 13 detik
10.	Jarak jangkauan kendali	± 1000 m (pada kondisi power HT *Transmitter* adalah *low level*)



Title		
Size A4	Number	Revision
Date: 28-Mar-2007	Sheet of	
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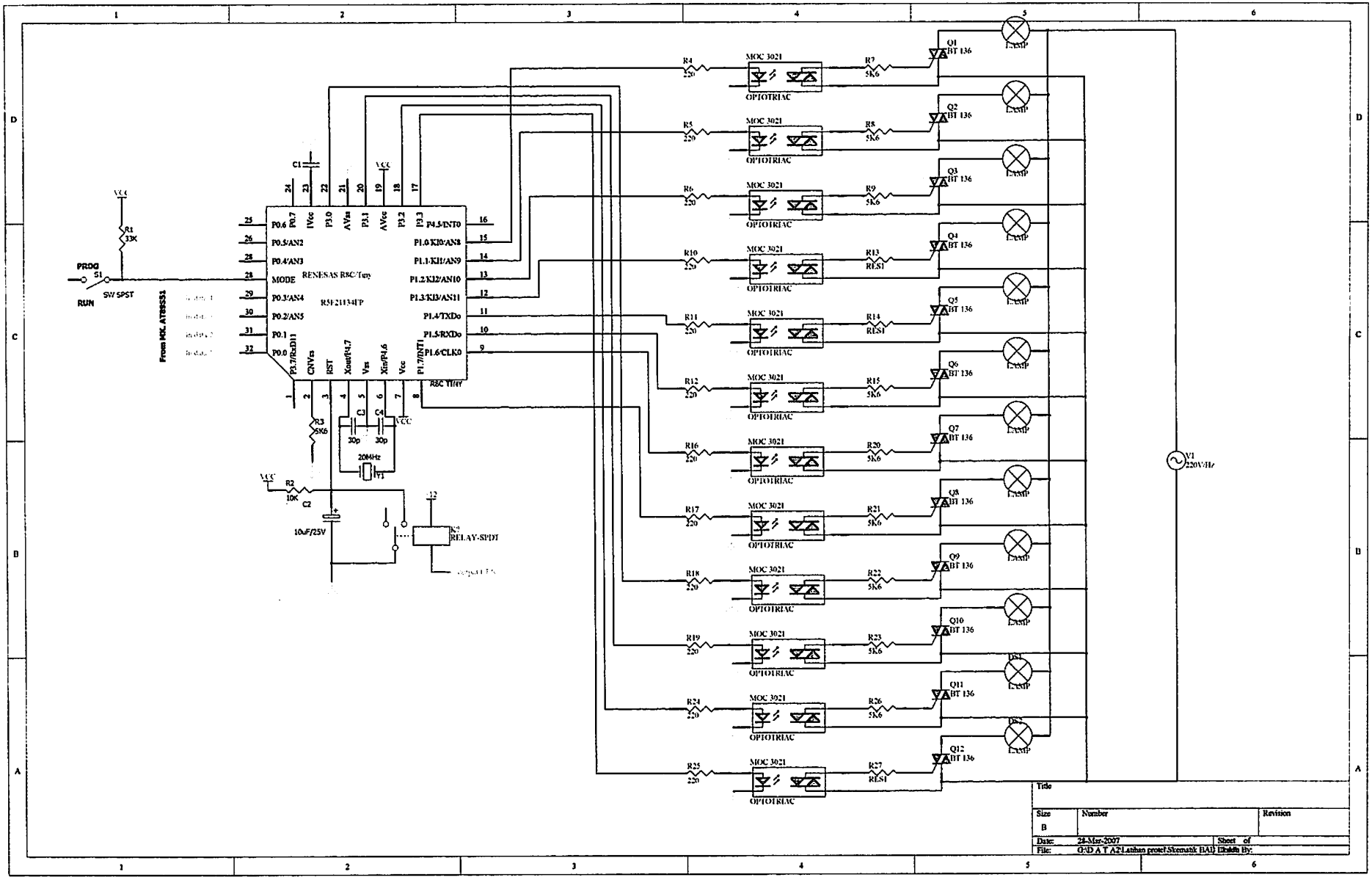
RENESAS R8C/Tiny
R5F21134FP
R8C Tiny
MOC 3021
OPTOTRIAC
BT 136
LAMP
RELAY-SPDT
20MHz
SW SPST
PROG
RUN
From MSC ATB8S51
Title
Size
B
Number
Revision
Date: 24-Mar-2007
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File: G:\D A T A\2\Lathan proef\Skematik BAU.DSN
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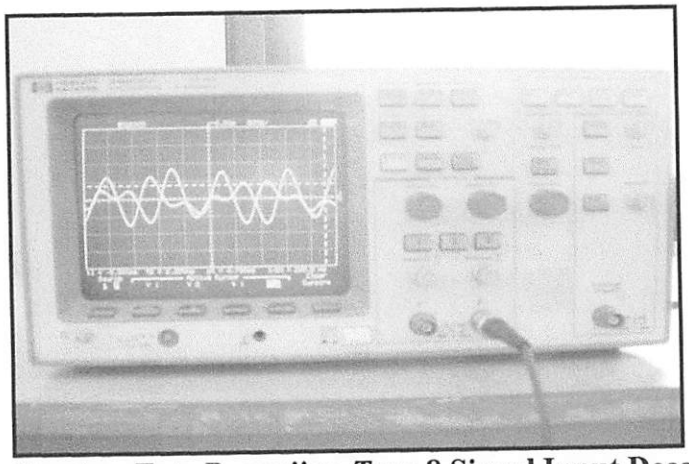
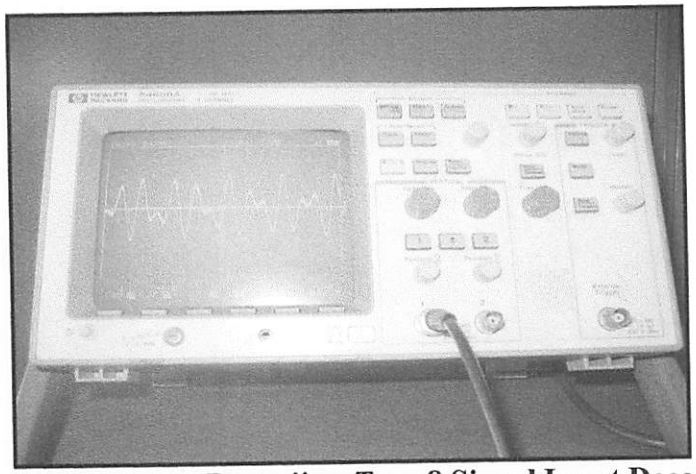


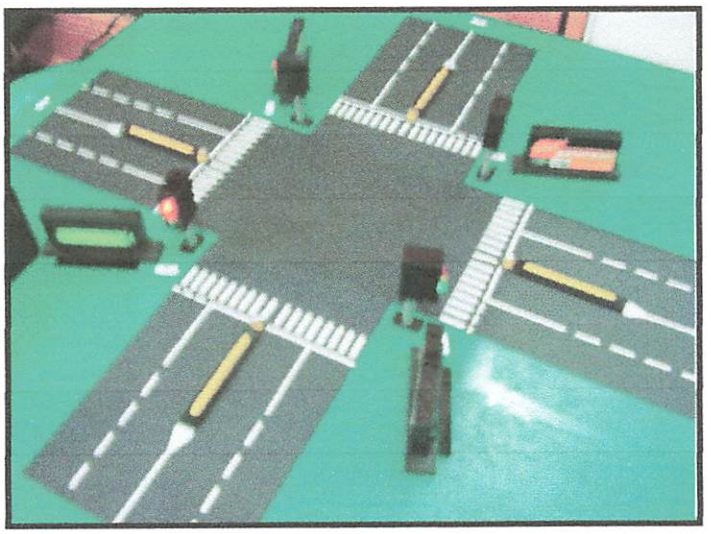
Data yang dikirim = digit 8
V/div = 500 mV
T/div = 500 µS
Volume HT (ICOM IC-2N) = ± 60 %

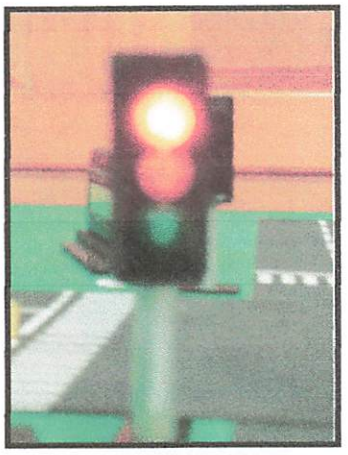
Gambar Foto Pengujian *Tone* 8 Sinyal Input Decoder DTMF

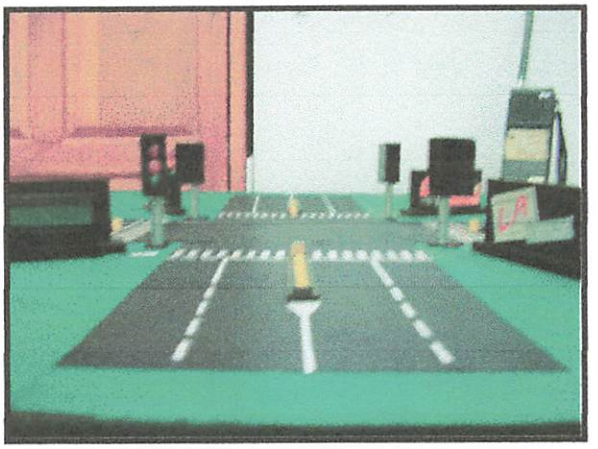


Data yang dikirim = digit 8
V/div = 500 mV
T/div = 1 mS
Volume HT (ICOM IC-2N) = ± 60 %

Gambar Foto Pengujian *Tone* 8 Sinyal Input Decoder DTMF







Sistem Kontrol Traffic Light Jarak Jauh
Dengan Menggunakan Radio HT (Handy Talky)

```
/*****************************************************************
:  FILE        : ardhie
:
:*****************************************************************/

/*****************************************************************
:   Tempat deklarasi include
:*****************************************************************/
#include    <stdio.h>
#include        "sfr_r813.h"                    /* Definition of the R8C/13 SFR
*/
#include        "TombolLED.h"

unsigned char waktu;
unsigned char a, b ,c, d;

/*****************************************************************************
*       Function : main()
*       program section
*****************************************************************************/
void delay(long tunggu)
{
        while(tunggu--);
}

void inittimer()
{
        txmr= 0x00;
        tcss= 0x02;
        prex= 249;
        tx  = 1;
.

void delay_1detik()
:
        waktu = 0;
        while (waktu < 10)
        {
                if(prex==0 && tx==0)
                {
                        waktu++;
                }
        }
}

void mode1(void)
{           LEDM1 = 0;
                        LEDK1 = 1;
                        LEDH1 = 0;

                        LEDM2 = 0;
                        LEDK2 = 1;
                        LEDH2 = 0;

                        LEDM3 = 0;
                        LEDK3 = 1;
                        LEDH3 = 0;

                        LEDM4 = 0;
                        LEDK4 = 1;
                        LEDH4 = 0;

                        delay_1detik ();


                        LEDM1 = 0;
                        LEDK1 = 0;
```

```
                LEDH1 = 0;

                LEDM2 = 0;
                LEDK2 = 0;
                LEDH2 = 0;

                LEDM3 = 0;
                LEDK3 = 0;
                LEDH3 = 0;

                LEDM4 = 0;
                LEDK4 = 0;
                LEDH4 = 0;

                delay_1detik ();



mode2(void)
        LEDM1 = 0;
                LEDK1 = 0;
                LEDH1 = 1;

                LEDM2 = 1;
                LEDK2 = 0;
                LEDH2 = 0;

                LEDM3 = 1;
                LEDK3 = 0;
                LEDH3 = 0;

                LEDM4 = 1;
                LEDK4 = 0;
                LEDH4 = 0;
                a = 0;
                while (a < 20)
                {
                        delay_1detik();
                        a++;
                }
                LEDK1 = 1;
            LEDH1 = 0;
                delay(50000);
                LEDK1 = 0;
                delay(50000);
                LEDK1 = 1;
                delay(50000);
                LEDK1 = 0;
                delay(50000);
                LEDK1 = 1;
                delay(50000);
                LEDM1 = 1;
                LEDK1 = 0;
                LEDH1 = 0;

                LEDM2 = 0;
                LEDK2 = 0;
                LEDH2 = 1;

                LEDM3 = 1;
                LEDK3 = 0;
                LEDH3 = 0;

                LEDM4 = 1;
                LEDK4 = 0;
                LEDH4 = 0;
```

```
    b = 0;
    while (b < 20)
    {
            delay_1detik();
            b++;
    }
    LEDK2 = 1;
LEDH2 = 0;
    delay(50000);
    LEDK2 = 0;
    delay(50000);
    LEDK2 = 1;
    delay(50000);
    LEDK2 = 0;
    delay(50000);
    LEDK2 = 1;
    delay(50000);
    LEDM1 = 1;
    LEDK1 = 0;
    LEDH1 = 0;

    LEDM2 = 1;
    LEDK2 = 0;
    LEDH2 = 0;

    LEDM3 = 0;
    LEDK3 = 0;
    LEDH3 = 1;

    LEDM4 = 1;
    LEDK4 = 0;
    LEDH4 = 0;
    c = 0;
    while (c < 20)
    {
            delay_1detik();
            c++;
    }
    LEDK3 = 1;
LEDH3 = 0;
    delay(50000);
    LEDK3 = 0;
    delay(50000);
    LEDK3 = 1;
    delay(50000);
    LEDK3 = 0;
    delay(50000);
    LEDK3 = 1;
    delay(50000);
    LEDM1 = 1;
    LEDK1 = 0;
    LEDH1 = 0;

    LEDM2 = 1;
    LEDK2 = 0;
    LEDH2 = 0;

    LEDM3 = 1;
    LEDK3 = 0;
    LEDH3 = 0;

    LEDM4 = 0;
    LEDK4 = 0;
    LEDH4 = 1;
    d = 0;
    while (d<20)
    {
```

```
                delay_1detik();
                d++;
            }
            LEDK4 = 1;
        LEDH4 = 0;
            delay(50000);
            LEDK4 = 0;
            delay(50000);
            LEDK4 = 1;
            delay(50000);
            LEDK4 = 0;
            delay(50000);
            LEDK4 = 1;
            delay(50000);

mode3(void)
        LEDM1 = 0;
            LEDK1 = 0;
            LEDH1 = 1;

            LEDM2 = 1;
            LEDK2 = 0;
            LEDH2 = 0;

            LEDM3 = 1;
            LEDK3 = 0;
            LEDH3 = 0;

            LEDM4 = 1;
            LEDK4 = 0;
            LEDH4 = 0;
            a = 0;
            while (a<15)
            {
                    delay_1detik();
                    a++;
            }
            LEDK1 = 1;
         LEDH1 = 0;
            delay(50000);
            LEDK1 = 0;
            delay(50000);
            LEDK1 = 1;
            delay(50000);
            LEDK1 = 0;
            delay(50000);
            LEDK1 = 1;
            delay(50000);
            LEDM1 = 1;
            LEDK1 = 0;
            LEDH1 = 0;

            LEDM2 = 0;
            LEDK2 = 0;
            LEDH2 = 1;

            LEDM3 = 1;
            LEDK3 = 0;
            LEDH3 = 0;

            LEDM4 = 1;
            LEDK4 = 0;
            LEDH4 = 0;
            b = 0;
            while (b<15)
            {
                    delay_1detik();
```

```
            b++;
    }
    LEDK2 = 1;
LEDH2 = 0;
    delay(50000);
    LEDK2 = 0;
    delay(50000);
    LEDK2 = 1;
    delay(50000);
    LEDK2 = 0;
    delay(50000);
    LEDK2 = 1;
    delay(50000);
    LEDM1 = 1;
    LEDK1 = 0;
    LEDH1 = 0;

    LEDM2 = 1;
    LEDK2 = 0;
    LEDH2 = 0;

    LEDM3 = 0;
    LEDK3 = 0;
    LEDH3 = 1;

    LEDM4 = 1;
    LEDK4 = 0;
    LEDH4 = 0;
    c = 0;
    while (c<15)
    {
            delay_1detik();
            c++;
    }

    LEDK3 = 1;
 LEDH3 = 0;
    delay(50000);
    LEDK3 = 0;
    delay(50000);
    LEDK3 = 1;
    delay(50000);
    LEDK3 = 0;
    delay(50000);
    LEDK3 = 1;
    delay(50000);
    LEDM1 = 1;
    LEDK1 = 0;
    LEDH1 = 0;

    LEDM2 = 1;
    LEDK2 = 0;
    LEDH2 = 0;

    LEDM3 = 1;
    LEDK3 = 0;
    LEDH3 = 0;

    LEDM4 = 0;
    LEDK4 = 0;
    LEDH4 = 1;
    d = 0;
    while (d<15)
    {
            delay_1detik();
            d++;
    }
```

```
        LEDK4 = 1;
    LEDH4 = 0;
        delay(50000);
        LEDK4 = 0;
        delay(50000);
        LEDK4 = 1;
        delay(50000);
        LEDK4 = 0;
        delay(50000);
        LEDK4 = 1;
        delay(50000);

oid mode4(void)
    LEDM1 = 0;
        LEDK1 = 0;
        LEDH1 = 1;

        LEDM2 = 1;
        LEDK2 = 0;
        LEDH2 = 0;

        LEDM3 = 1;
        LEDK3 = 0;
        LEDH3 = 0;

        LEDM4 = 1;
        LEDK4 = 0;
        LEDH4 = 0;
        a = 0;
        while (a<10)
        {
                delay_1detik();
                a++;
        }
        LEDK1 = 1;
    LEDH1 = 0;
        delay(50000);
        LEDK1 = 0;
        delay(50000);
        LEDK1 = 1;
        delay(50000);
        LEDK1 = 0;
        delay(50000);
        LEDK1 = 1;
        delay(50000);
        LEDM1 = 1;
        LEDK1 = 0;
        LEDH1 = 0;

        LEDM2 = 0;
        LEDK2 = 0;
        LEDH2 = 1;

        LEDM3 = 1;
        LEDK3 = 0;
        LEDH3 = 0;

        LEDM4 = 1;
        LEDK4 = 0;
        LEDH4 = 0;

        b = 0;
        while (b<10)
        {
                delay_1detik();
                b++;
        }
```

```
    LEDK2 = 1;
LEDH2 = 0;
    delay(50000);
    LEDK2 = 0;
    delay(50000);
    LEDK2 = 1;
    delay(50000);
    LEDK2 = 0;
    delay(50000);
    LEDK2 = 1;
    delay(50000);
    LEDM1 = 1;
    LEDK1 = 0;
    LEDH1 = 0;

    LEDM2 = 1;
    LEDK2 = 0;
    LEDH2 = 0;

    LEDM3 = 0;
    LEDK3 = 0;
    LEDH3 = 1;

    LEDM4 = 1;
    LEDK4 = 0;
    LEDH4 = 0;

    c = 0;
    while (c<10)
    {
            delay_1detik();
            c++;
    }
    LEDK3 = 1;
LEDH3 = 0;
    delay(50000);
    LEDK3 = 0;
    delay(50000);
    LEDK3 = 1;
    delay(50000);
    LEDK3 = 0;
    delay(50000);
    LEDK3 = 1;
    delay(50000);
    LEDM1 = 1;
    LEDK1 = 0;
    LEDH1 = 0;

    LEDM2 = 1;
    LEDK2 = 0;
    LEDH2 = 0;

    LEDM3 = 1;
    LEDK3 = 0;
    LEDH3 = 0;

    LEDM4 = 0;
    LEDK4 = 0;
    LEDH4 = 1;

    d =  0;
    while (d<10)
    {
            delay_1detik();
            d++;
    }
    LEDK4 = 1;
```

```
                LEDH4 = 0;
                    delay(50000);
                    LEDK4 = 0;
                    delay(50000);
                    LEDK4 = 1;
                    delay(50000);
                    LEDK4 = 0;
                    delay(50000);
                    LEDK4 = 1;
                    delay(50000);

oid mode5(void)
        LEDM1 = 0;
                    LEDK1 = 0;
                    LEDH1 = 1;

                    LEDM2 = 1;
                    LEDK2 = 0;
                    LEDH2 = 0;

                    LEDM3 = 1;
                    LEDK3 = 0;
                    LEDH3 = 0;

                    LEDM4 = 1;
                    LEDK4 = 0;
                    LEDH4 = 0;
                    delay_1detik ();
                    delay_1detik ();



oid mode6(void)
        LEDM1 = 1;
                    LEDK1 = 0;
                    LEDH1 = 0;

                    LEDM2 = 0;
                    LEDK2 = 0;
                    LEDH2 = 1;

                    LEDM3 = 1;
                    LEDK3 = 0;
                    LEDH3 = 0;

                    LEDM4 = 1;
                    LEDK4 = 0;
                    LEDH4 = 0;
                    delay_1detik ();
                    delay_1detik ();


oid mode7(void)
        LEDM1 = 1;
                    LEDK1 = 0;
                    LEDH1 = 0;

                    LEDM2 = 1;
                    LEDK2 = 0;
                    LEDH2 = 0;

                    LEDM3 = 0;
                    LEDK3 = 0;
                    LEDH3 = 1;

                    LEDM4 = 1;
```

```
        if (p0==0xF1)
        {delay(50);
                mode1();
                        }else
        if (p0==0xF2)
        {delay(50);
        mode2();

                        }else
        if (p0==0xF3)
        {delay(50);
        mode3();
                        }else
        if (p0==0xF4)
        {delay(500);
        mode4();
                        }else
        if (p0==0xF5)
        {delay(50);
        mode5();
                        }else
        if (p0==0xF6)
        {delay(500);
        mode6();
                        }else
        if (p0==0xF7)
        {delay(50);
        mode7();
                        }else
        if (p0==0xF8)
        {delay(50);
        mode8();
                        }
        }
}
```

```
.CD CONSTANTA
;PCLR    EQU 00000001B
:NK      EQU 00001101B
'RMOD    EQU 00000110B
;PON     EQU 00001100B
:SOR     EQU 00011100B
ICSET    EQU 00111000B

:VICE ADDRESS [LCD]
         bit P2.0    ;LCD
         bit P2.1    ;LCD
         bit P2.2    ;LCD
         bit P2.3    ;LCD
         bit P2.4    ;LCD
         bit P2.5    ;LCD
         bit P2.6    ;LCD
         bit P2.7    ;LCD

.asi1    EQU 22H
;IL1     EQU 23H
;IL2     EQU 24H
;IL3     EQU 25H
)1       EQU 26H
)2       EQU 27H
)3       EQU 28H
)4       EQU 29H
'AKEY0   EQU 34H
'AKEY1   EQU 35H
'AKEY2   EQU 36H
'AKEY3   EQU 37H
.1       EQU 20H
.2       EQU 21H
.3       EQU 22H
.4       EQU 38H
.5       EQU 39H
.6       EQU 40H
      ORG     0000H
      JMP     MULAI

.AI:

      MOV      P3,#01H
      LCALL    INIT_LCD

SIALISASI:

************************
 INISIALISASI LCD      *
************************
AY_INIT_LCD:
      MOV R6,#20H

_LCD_LP:

      MOV     R7,#0
      DJNZ    R7,$
      DJNZ    R6,DLY_LCD_LP
      RET

T_LCD:
      SETB RS
      ;SETB RW
      CLR E

      MOV A,#DISPCLR
      LCALL CONTROLOUT
      LCALL DELAY_INIT_LCD
```

```
      MOV     A,#FUNCSET
      LCALL   CONTROLOUT
      MOV     A,#DISPON
      LCALL   CONTROLOUT
      MOV     A,#ENTRMOD
      LCALL   CONTROLOUT
      MOV     DPTR,#itn1
      LCALL   PRINTSTRING1
      MOV     DPTR,#itn2
      LCALL   PRINTSTRING2

****************************************
IT_LCD1:

      SETB RS2
      ;SETB RW1
      CLR E1
      MOV A,#DISPCLR

      LCALL CONTROLOUT1
      LCALL DELAY_INIT_LCD

      MOV     A,#FUNCSET
      LCALL   CONTROLOUT1
      MOV     A,#DISPON
      LCALL   CONTROLOUT1
      MOV     A,#ENTRMOD
      LCALL   CONTROLOUT1
      MOV     DPTR,#DT1
      LCALL   PRINTSTRING11
      MOV     DPTR,#DT2
      LCALL   PRINTSTRING21
****************************************
IT_LCDB:

      SETB RSB
      ;SETB RWB
      CLR EB
      MOV A,#DISPCLR

      LCALL CONTROLOUTB
      LCALL DELAY_INIT_LCD

      MOV     A,#FUNCSET
      LCALL   CONTROLOUTB
      MOV     A,#DISPON
      LCALL   CONTROLOUTB
      MOV     A,#ENTRMOD
      LCALL   CONTROLOUTB
      MOV     DPTR,#brw1
      LCALL   PRINTSTRING1B
      MOV     DPTR,#brw2
      LCALL   PRINTSTRING2B
      ;CALL   DELAY
****************************************
IT_LCDC:
      SETB RSC
      ;SETB RWC
      CLR EC
      MOV A,#DISPCLR

      LCALL CONTROLOUTC
      LCALL DELAY_INIT_LCD

      MOV     A,#FUNCSET
      LCALL   CONTROLOUTC
      MOV     A,#DISPON
```

```
        MOV     @R0,A
        DEC     R0

        MOV     A,LOKASI1
        INC     A
        MOV     LOKASI1,A
.01:
        CJNE    A,#00000001B,PIL.L11
        MOV A,#7
        LCALL POSISI2
        JMP     TAMPILL1
.L11:
        CJNE    A,#00000010B,PIL21
        MOV A,#8
        LCALL POSISI2
        JMP     TAMPILL1
.21:
        CJNE    A,#00000011B,PIL31
        MOV A,#9
        LCALL POSISI2
        JMP     TAMPILL1
.31:
        CJNE    A,#00000100B,PIL41
        MOV LOKASI1,#00H
        MOV A,#10
        LCALL POSISI2
        JMP     TAMPILL1
.41:
        LJMP    PIL01
        RET
MPILL1:
        MOV A,#2AH
        LCALL   DATAOUT
        ACALL PTT
        ACALL PTT
        JMP     KEYLOOP
        RET

)PKEY:
        MOV     DPTR,#PASW2
        LCALL   PRINTSTRING1
        MOV     DPTR,#ESEK
        LCALL   PRINTSTRING2

        CALL    DELAY

'ER1:

        MOV A,COD2
        SWAP A
        ORL A,COD1
        MOV HASIL1,A
        MOV A,KAR4
        XRL A,HASIL1
        MOV R0,A
        CLR A
        CLR COD2
        MOV A,COD4
        SWAP A
        ORL A,COD3
        MOV HASIL2,A
        MOV A,KAR5
        XRL A,HASIL2
        ORL A,R0
        CJNE A,#00H,MALING1
        AJMP JALAN
```

```
LING1:

        MOV     DPTR,#pasc
        LCALL   PRINTSTRING1
        MOV     DPTR,#pasd
        LCALL   PRINTSTRING2
        CALL    DELAY
        MOV     DPTR,#itn1
        LCALL   PRINTSTRING1
        MOV     DPTR,#itn2
        LCALL   PRINTSTRING2
        MOV     P3,R2
        SETB    P3.7
        ACALL   PTT
        CLR     P3.7
        setb    p3.5
        ACALL   PTT
        ACALL   PTT
        ACALL   PTT
        ACALL   PTT
        CALL    SUARA
        CALL    SUARA
        CALL    SUARA
        clr     p3.5
lik2:
        JNB     P1.4,BALIK2
        AJMP    PUTT1

TA1:
        CLR     P3.6
        mov     R0,#200
L1:     djnz    R0,KEL1

        SETB    P3.6
        mov     R0,#200
L2:     djnz    R0,KEL2
        ret

ARA:
        call    data1
        call    data1
        call    data1
        call    data1
        call    data1
        call    data1
        call    data1
        call    data1
        call    data1
        call    data1
        call    data1
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        call    data1
        call    data1
```

```
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
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    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    RET
N:

    MOV     DPTR,#pasa
    LCALL   PRINTSTRING1
    MOV     DPTR,#pasb
    LCALL   PRINTSTRING2
    setb    p3.5
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    call    data1
    clr     p3.5

    JB      P1.4,$
    JNB     P1.4,$
    MOV     A,P1
    ANL     A,#0FH
    MOV     B,A
    CALL    DELAY
    MOV     A,B


    CJNE    A,#01H,TIDAK1
    MOV     P3,B
    JMP     PILIHAN_NORMAL

K1:
    CJNE    A,#02H,TIDAK2
```

```
        MOV     P3,B
        JMP     PILIHAN_NORMAL
)AK2:
        CJNE    A,#03H,TIDAK3
        MOV     P3,B
        JMP     PILIHAN_NORMAL
)AK3:
        CJNE    A,#04H,TIDAK4
        MOV     P3,B
        JMP     PILIHAN_NORMAL
)AK4:
        CJNE    A,#05H,TIDAK5
        MOV     P3,B
        JMP     PILIHAN_SIBUK
)AK5:
        CJNE    A,#06H,TIDAK6
        MOV     P3,B
        JMP     PILIHAN_SIBUK
)AK6:
        CJNE    A,#07H,TIDAK7
        MOV     P3,B
        JMP     PILIHAN_SIBUK
)AK7:
        CJNE    A,#08H,TIDAK8
        MOV     P3,B
        JMP     PILIHAN_SIBUK
)AK8:


LIHAN_NORMAL:
        SETB    P3.7
        ACALL   PTT
        CLR     P3.7
        MOV     DPTR,#itn1
        LCALL   PRINTSTRING1
        MOV     DPTR,#itn2
        LCALL   PRINTSTRING2
lik3:
        JNB     P1.4,BALIK3
        AJMP    PUTT1

LIHAN_SIBUK:
        SETB    P3.7
        ACALL   PTT
        CLR     P3.7
LIHAN_SIBUK1:
        MOV     DPTR,#SB1
        LCALL   PRINTSTRING1
        MOV     DPTR,#SB2
        LCALL   PRINTSTRING2
        MOV     DPTR,#SB1
        LCALL   PRINTSTRING1B
        MOV     DPTR,#SB2
        LCALL   PRINTSTRING2B
        MOV     DPTR,#SB1
        LCALL   PRINTSTRING11
        MOV     DPTR,#SB2
        LCALL   PRINTSTRING21
        MOV     DPTR,#SB1
        LCALL   PRINTSTRING1C
        MOV     DPTR,#SB2
        LCALL   PRINTSTRING2C
        JNB     P1.4,PILIHAN_SIBUK1

        MOV     DPTR,#itn1
        LCALL   PRINTSTRING1
        MOV     DPTR,#itn2
```

```
      LCALL   PRINTSTRING2
      ACALL   PTT
      MOV     DPTR,#brw1
      LCALL   PRINTSTRING1B
      MOV     DPTR,#brw2
      LCALL   PRINTSTRING2B
      ACALL   PTT
      MOV     DPTR,#DT1
      LCALL   PRINTSTRING11
      MOV     DPTR,#DT2
      LCALL   PRINTSTRING21
      ACALL   PTT
      MOV     DPTR,#SS1
      LCALL   PRINTSTRING1C
      MOV     DPTR,#SS2
      LCALL   PRINTSTRING2C
      ACALL   PTT
      AJMP    BALIK

LAY:
      MOV     R7,#100
OP2:  MOV     R6,#100
OP1:  MOV     R5,#100
      DJNZ    R5,$
      DJNZ    R6,LOOP1
      DJNZ    R7,LOOP2

      MOV     R7,#100
OP4:  MOV     R6,#100
OP3:  MOV     R5,#100
      DJNZ    R5,$
      DJNZ    R6,LOOP3
      DJNZ    R7,LOOP4
      RET
T:
      MOV     50H,#50
NDAL:
      MOV     51H,#250
      DJNZ    51H,$
      DJNZ    50H,TUNDAL
      RET
      JMP     $


*********************************
 KUMPULAN RUTIN PELAYANAN LCD1 *
*********************************

SISI2_1:
      MOV     A,#1
SISI2:
      ADD     A,#11000000B
      SJMP    POSISI_SUB

SISI1_1:
      MOV     A,#1
SISI1:
      ADD     A,#10000000B
SISI_SUB:
      DEC     A
      LCALL   CONTROLOUT
      RET

INTSTRING2:
      LCALL   POSISI2_1
      SJMP    PRINTSTRING
```

```
INTSTRING1:
      LCALL   POSISI1_1

INTSTRING:
      SJMP    OUTSTRING
INTSTRINGLOOP:
      LCALL   DATAOUT
      INC     DPTR

TSTRING:
      CLR     A
      MOVC    A,@A+DPTR
      JNZ     PRINTSTRINGLOOP
      RET

NTROLOUT:
      CPL RS
      CPL E
      MOV P0,A
      CPL E
      CPL RS
      MOV P0,#0FFH
      SJMP LCD_OUT

TAOUT:

      CPL E
      MOV P0,A
      CPL E


D_OUT:
      MOVX    @DPTR,A

LAY_LCD:
      PUSH ACC
      MOV     A,#250
      DJNZ    ACC,$
      POP ACC
      RET
********************************
 KUMPULAN RUTIN PELAYANAN LCD2 *
********************************

ISI2_11:
      MOV     A,#1
ISI21:
      ADD     A,#11000000B
      SJMP    POSISI_SUB1

ISI1_11:
      MOV     A,#1
ISI11:
      ADD     A,#10000000B
ISI_SUB1:
      DEC     A
      LCALL   CONTROLOUT1
      RET

NTSTRING21:
      LCALL   POSISI2_11
      SJMP    PRINTSTRINGa

NTSTRING11:
      LCALL   POSISI1_11

NTSTRINGa:
```

```
    SJMP    OUTSTRING1
STRINGLOOP1:
    LCALL   DATAOUT1
    INC     DPTR

RING1:
    CLR     A
    MOVC    A,@A+DPTR
    JNZ     PRINTSTRINGLOOP1
    RET

OLOUT1:

    CPL RS2
    CPL E1
    MOV P0,A
    CPL E1
    CPL RS2
    MOV P0,#0FFH
    SJMP LCD_OUT1

UT1:


    CPL E1
    MOV P0,A
    CPL E1


UT1:
    MOVX    @DPTR,A

Y_LCD1:
    PUSH ACC
    MOV     A,#250
    DJNZ    ACC,$
    POP ACC
    RET
*****************************
UMPULAN RUTIN PELAYANAN LCD3 *
*****************************

SI2_1B:
    MOV     A,#1
SI2B:
    ADD     A,#11000000B
    SJMP    POSISI_SUBB

SI1_1B:
    MOV     A,#1
SI1B:
    ADD     A,#10000000B
SI_SUBB:
    DEC     A
    LCALL   CONTROLOUTB
    RET

TSTRING2B:
    LCALL   POSISI2_1B
    SJMP    PRINTSTRINGB

TSTRING1B:
    LCALL   POSISI1_1B

ITSTRINGB:
    SJMP    OUTSTRINGB
ITSTRINGLOOPB:
```

```
        LCALL   DATAOUTB
        INC     DPTR

TSTRINGB:
        CLR     A
        MOVC    A,@A+DPTR
        JNZ     PRINTSTRINGLOOPB
        RET

NTROLOUTB:

        CPL RSB
        CPL EB
        MOV P0,A

        CPL EB
        CPL RSB
        MOV P0,#0FFH
        SJMP LCD_OUTB

TAOUTB:

        CPL EB
        MOV P0,A
        CPL EB

D_OUTB:
        MOVX    @DPTR,A

LAY_LCDB:
        PUSH ACC
        MOV     A,#250
        DJNZ    ACC,$
        POP ACC
        RET

*********************************
 KUMPULAN RUTIN PELAYANAN LCD3 *
*********************************

SISI2_1C:
        MOV     A,#1
SISI2C:
        ADD     A,#11000000B
        SJMP    POSISI_SUBC

SISI1_1C:
        MOV     A,#1
SISI1C:
        ADD     A,#10000000B
SISI_SUBC:
        DEC     A
        LCALL   CONTROLOUTC
        RET

INTSTRING2C:
        LCALL   POSISI2_1C
        SJMP    PRINTSTRINGC

INTSTRING1C:
        LCALL   POSISI1_1C

INTSTRINGC:
        SJMP    OUTSTRINGC
INTSTRINGLOOPC:
        LCALL   DATAOUTC
        INC     DPTR
```

```
STRINGC:
     CLR    A
     MOVC   A,@A+DPTR
     JNZ    PRINTSTRINGLOOPC
     RET

TROLOUTC:

     CPL RSC
     CPL EC
     MOV P0,A

     CPL EC
     CPL RSC
     MOV P0,#0FFH
     SJMP LCD_OUTC

AOUTC:

     CPL EC
     MOV P0,A
     CPL EC

_OUTC:
     MOVX   @DPTR,A

AY_LCDC:
     PUSH ACC
     MOV    A,#250
     DJNZ   ACC,$
     POP ACC
     RET
W:     DB 'MASUKKAN PASWORD',0
W1:    DB 'PSW  :           ',0
US:    DB '                 ',0
W2:    DB 'ANALISA  PASWORD',0
K:     DB ' WAIT A MINUTE  ',0
DI:    DB 'PASWORD DITERIMA',0


d:   DB ' PASWORD DITOLAK ',0
c:   DB '      MAAF       ',0

a:    DB '    PASWORD     ',0
b:    DB '    DITERIMA    ',0

:      DB 'PCK DIENG   --> ',0
:      DB '<-- ARAH DINOYO ',0
1:     DB 'ARAH DINOYO --> ',0
2:     DB '<-- PCK DIENG   ',0
:      DB 'ARAH KOTA   --> ',0
:      DB '<- ARAH ITN KMP1',0
1:     DB 'ARAH ITN KMP1 ->',0
2:     DB '<-- ARAH KE KOTA',0
:      DB 'MAAF  PERJALANAN',0
:      DB ' ANDA TERGANGGU ',0
      END
```

ISO²-CMOS MT8870D/MT8870D-1

Integrated DTMF Receiver

ISSUE 3 May1995

Features

- Complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Backward compatible with MT8870C/MT8870C-1

Applications

- Receiver system for British Telecom (BT) or CEPT Spec (MT8870D-1)
- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote control
- Personal computers
- Telephone answering machine

Ordering Information

MT8870DE/DE-1	18 Pin Plastic DIP
MT8870DC/DC-1	18 Pin Ceramic DIP
MT8870DS/DS-1	18 Pin SOIC
MT8870DN/DN-1	20 Pin SSOP
MT8870DT/DT-1	20 Pin TSSOP

-40 °C to +85 °C

Description

The MT8870D/MT8870D-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

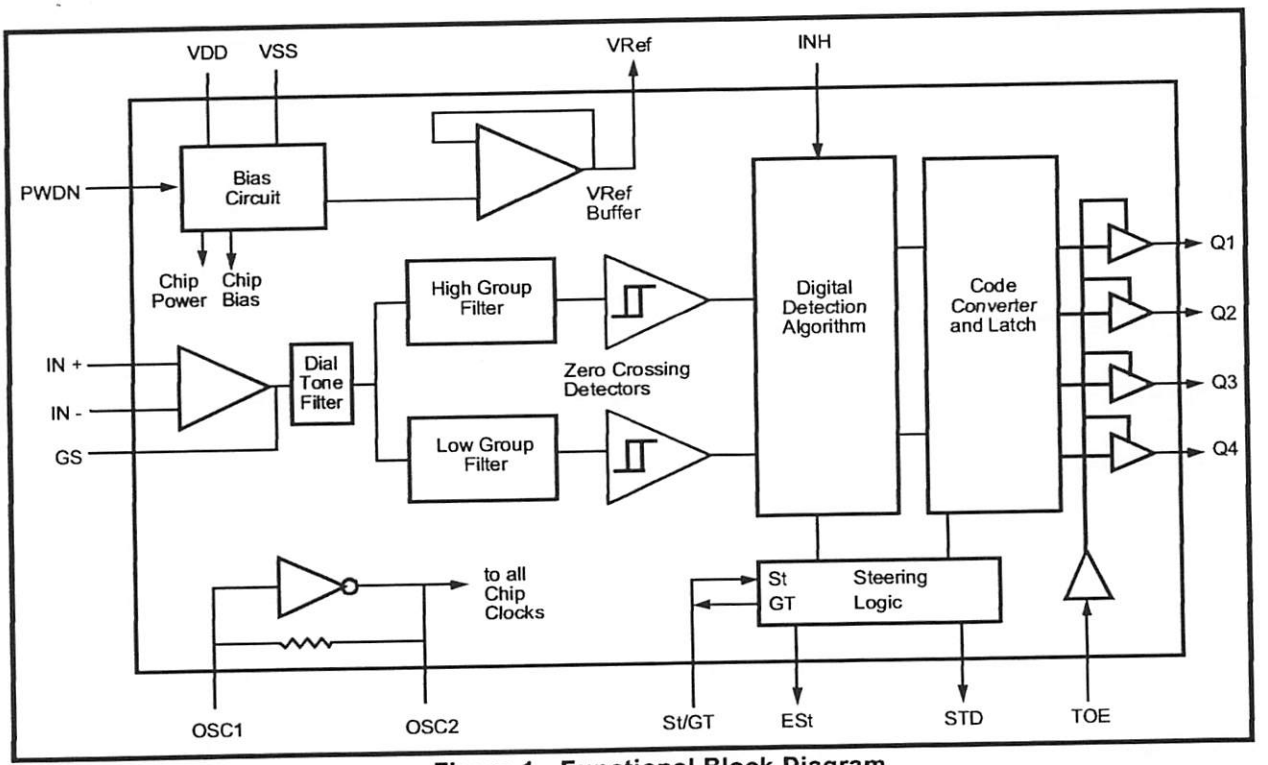


Figure 1 - Functional Block Diagram

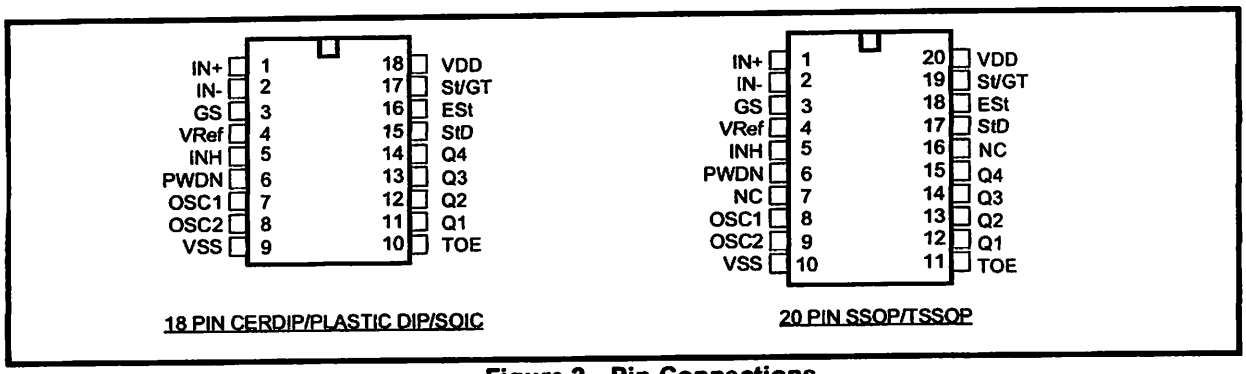


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
18	20		
1	1	IN+	**Non-Inverting Op-Amp (Input).**
2	2	IN-	**Inverting Op-Amp (Input).**
3	3	GS	**Gain Select.** Gives access to output of front end differential amplifier for connection of feedback resistor.
4	4	V_{Ref}	**Reference Voltage (Output).** Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig. 6 and Fig. 10).
5	5	INH	**Inhibit (Input).** Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
6	6	PWDN	**Power Down (Input).** Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down.
7	8	OSC1	**Clock (Input).**
8	9	OSC2	**Clock (Output).** A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9	10	V_{SS}	**Ground (Input).** 0V typical.
10	11	TOE	**Three State Output Enable (Input).** Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	12-15	Q1-Q4	**Three State Data (Output).** When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
15	17	StD	**Delayed Steering (Output).** Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}.
16	18	ESt	**Early Steering (Output).** Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
17	19	St/GT	**Steering Input/Guard time (Output) Bidirectional.** A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	20	V_{DD}	**Positive power supply (Input).** +5V typical.
	7, 16	NC	No Connection.

Functional Description

The MT8870D/MT8870D-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Figure 3). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while

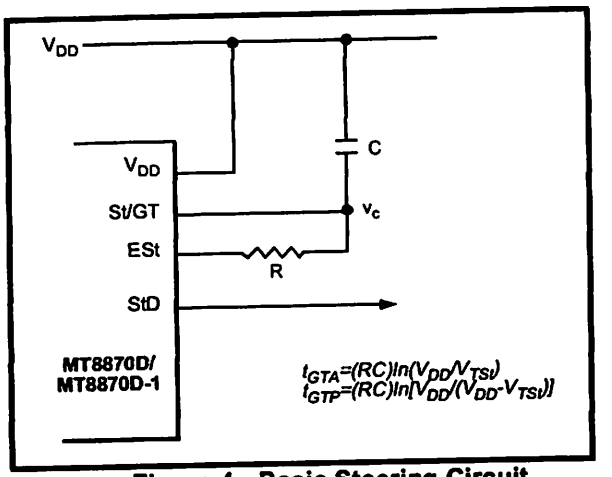


Figure 4 - Basic Steering Circuit

providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 4) to rise as the capacitor discharges. Provided signal

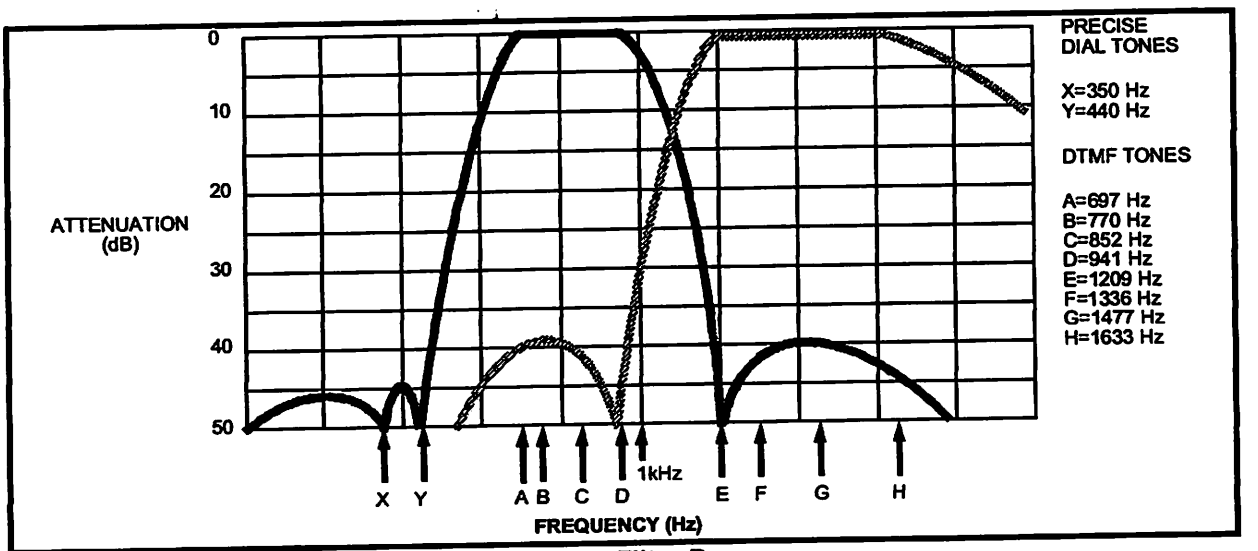


Figure 3 - Filter Response

dition is maintained (ESt remains high) for the dation period (t_{GTP}), v_c reaches the threshold s_t) of the steering logic to register the tone pair, hing its corresponding 4-bit code (see Table 1) the output latch. At this point the GT output is vated and drives v_c to V_{DD}. GT continues to drive as long as ESt remains high. Finally, after a rt delay to allow the output latch to settle, the ayed steering output flag (StD) goes high, alling that a received tone pair has been istered. The contents of the output latch are made ilable on the 4-bit output bus by raising the three e control input (TOE) to a logic high. The ering circuit works in reverse to validate the rdigit pause between signals. Thus, as well as cting signals too short to be considered valid, the eiver will tolerate signal interruptions (dropout) short to be considered a valid pause. This facility, ether with the capability of selecting the steering e constants externally, allows the designer to or performance to meet a wide variety of system uirements.

ard Time Adjustment

many situations not requiring selection of tone ation and interdigital pause, the simple steering uit shown in Figure 4 is applicable. Component ues are chosen according to the formula:

$$t_{REC}=t_{DP}+t_{GTP}$$
$$t_{ID}=t_{DA}+t_{GTA}$$

e value of t_{DP} is a device parameter (see Figure and t_{REC} is the minimum signal duration to be ognized by the receiver. A value for C of 0.1 µF is recommended for most applications, leaving R to be selected by the designer.

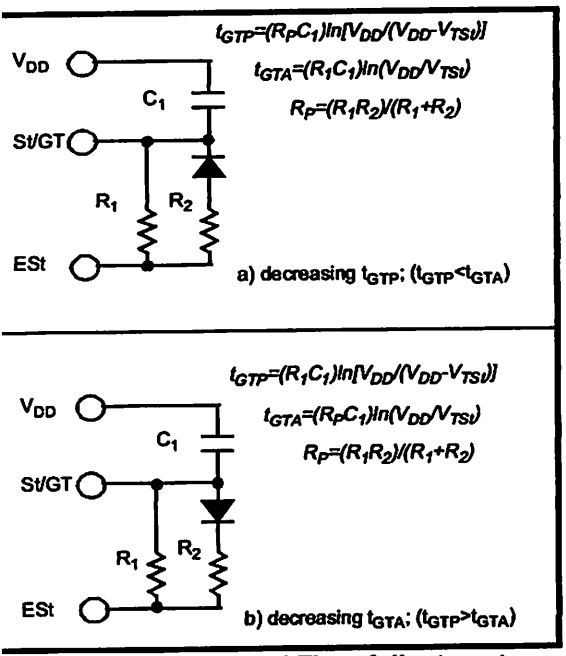


Figure 5 - Guard Time Adjustment

Digit	TOE	INH	ESt	Q_4	Q_3	Q_2	Q_1
ANY	L	X	H	Z	Z	Z	Z
1	H	X	H	0	0	0	1
2	H	X	H	0	0	1	0
3	H	X	H	0	0	1	1
4	H	X	H	0	1	0	0
5	H	X	H	0	1	0	1
6	H	X	H	0	1	1	0
7	H	X	H	0	1	1	1
8	H	X	H	1	0	0	0
9	H	X	H	1	0	0	1
0	H	X	H	1	0	1	0
*	H	X	H	1	0	1	1
#	H	X	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0
A	H	H	L	undetected, the output code will remain the same as the previous detected code			
B	H	H	L				
C	H	H	L				
D	H	H	L				

Table 1. Functional Decode Table

L=LOGIC LOW, H=LOGIC HIGH, Z=HIGH IMPEDANCE
X = DON'T CARE

Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 5.

Power-down and Inhibit Mode

A logic high applied to pin 6 (PWDN) will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones representing characters A, B, C, and D. The output code will remain the same as the previous detected code (see Table 1).

Differential Input Configuration

The input arrangement of the MT8870D/MT8870D-1 provides a differential-input operational amplifier as well as a bias source (V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 10 with the op-amp connected for unity gain and V_{Ref} biasing the input at $^1/_2V_{DD}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5.

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally connected as shown in Figure 10 (Single-Ended Input Configuration). However, it is possible to configure several MT8870D/MT8870D-1 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Figure 7 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, i.e., precision balancing capacitors are not required.

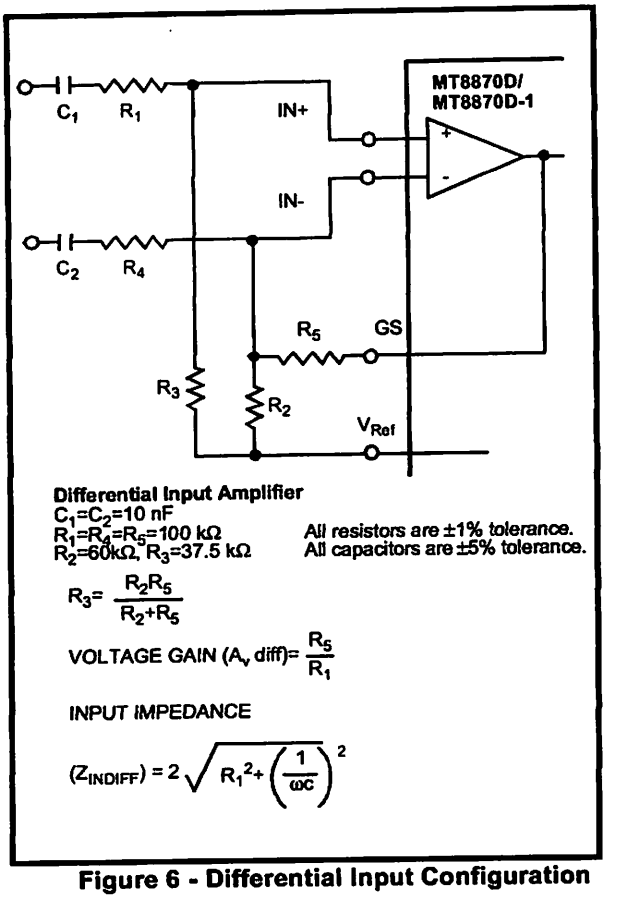


Figure 6 - Differential Input Configuration

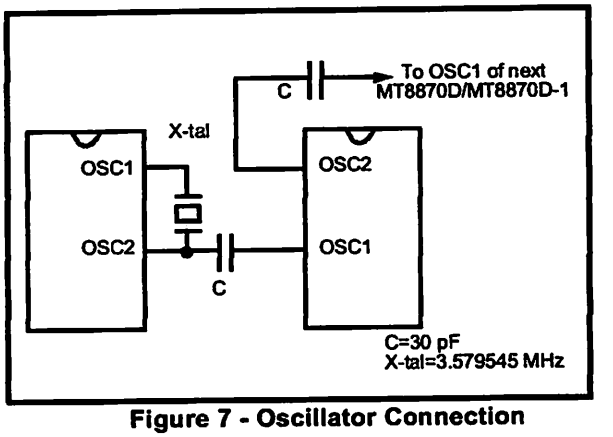


Figure 7 - Oscillator Connection

Parameter	Unit	Resonator
R1	Ohms	10.752
L1	mH	.432
C1	pF	4.984
C0	pF	37.915
Qm	-	896.37
Δf	%	±0.2%

Table 2. Recommended Resonator Specifications

Note: Qm=quality factor of RLC model, i.e., $1/2\Pi fR1C1$.

Applications

RECEIVER SYSTEM FOR BRITISH TELECOM SPEC POR 1151

The circuit shown in Fig. 9 illustrates the use of MT8870D-1 device in a typical receiver system. BT Spec defines the input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing a suitable values of R_1 and R_2 to provide 3 dB attenuation, such that -34 dBm input signal will correspond to -37 dBm at the gain setting pin GS of MT8870D-1. As shown in the diagram, the component values of R_3 and C_2 are the guard time requirements when the total component tolerance is 6%. For better performance, it is recommended to use the non-symmetric guard time circuit in Fig. 8.

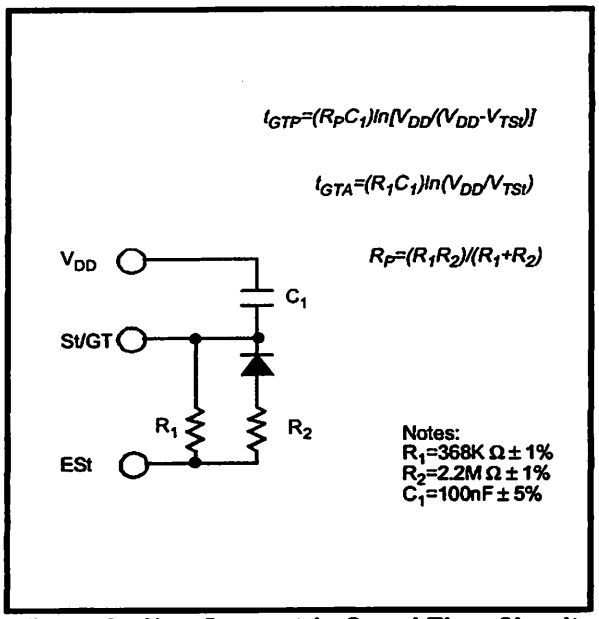


Figure 8 - Non-Symmetric Guard Time Circuit

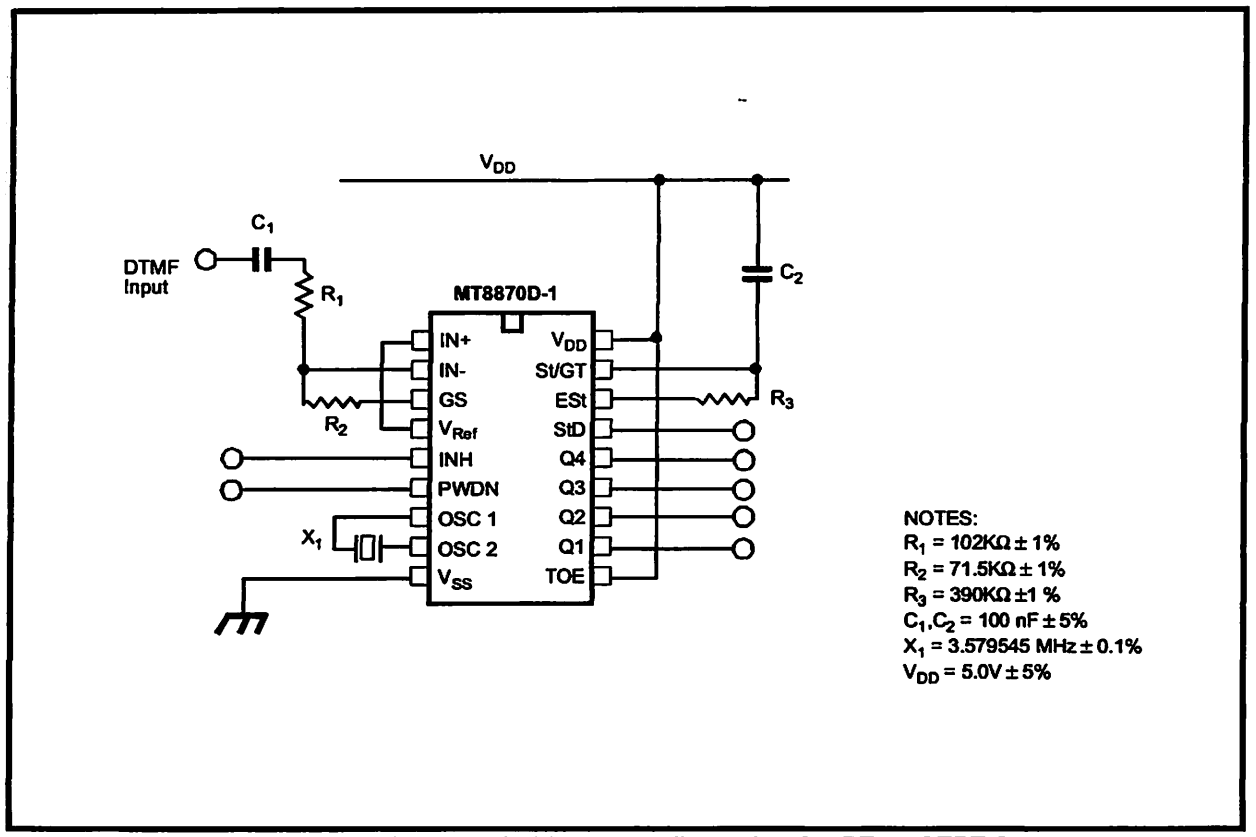


Figure 9 - Single-Ended Input Configuration for BT or CEPT Spec

Absolute Maximum Ratings†

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage	V_{DD}		7	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin (other than supply)	I_I		10	mA
4	Storage temperature	T_{STG}	-65	+150	°C
5	Package power dissipation	P_D		500	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75 °C at 16 mW / °C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DC Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Operating Temperature	T_O	-40		+85	°C	
3	Crystal/Clock Frequency	fc		3.579545		MHz	
4	Crystal/Clock Freq.Tolerance	Δfc		±0.1		%	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - V_{DD}=5.0V± 5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUPPLY	Standby supply current	I_{DDQ}		10	25	μA	PWDN=V_{DD}
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_O		15		mW	fc=3.579545 MHz
4	INPUTS	High level input	V_{IH}	3.5			V	V_{DD}=5.0V
5		Low level input voltage	V_{IL}			1.5	V	V_{DD}=5.0V
6		Input leakage current	I_{IH}/I_{IL}		0.1		μA	V_{IN}=V_{SS} or V_{DD}
7		Pull up (source) current	I_{SO}		7.5	20	μA	TOE (pin 10)=0, V_{DD}=5.0V
8		Pull down (sink) current	I_{SI}		15	45	μA	INH=5.0V, PWDN=5.0V, V_{DD}=5.0V
9		Input impedance (IN+, IN-)	R_{IN}		10		MΩ	@ 1 kHz
10		Steering threshold voltage	V_{TSt}	2.2	2.4	2.5	V	V_{DD} = 5.0V
11	OUTPUTS	Low level output voltage	V_{OL}			V_{SS}+0.03	V	No load
12		High level output voltage	V_{OH}	V_{DD}-0.03			V	No load
13		Output low (sink) current	I_{OL}	1.0	2.5		mA	V_{OUT}=0.4 V
14		Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT}=4.6 V
15		V_{Ref} output voltage	V_{Ref}	2.3	2.5	2.7	V	No load, V_{DD} = 5.0V
16		V_{Ref} output resistance	R_{OR}		1		kΩ	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

rating Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C ,unless otherwise stated.

Setting Amplifier

Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
Input leakage current	I_{IN}			100	nA	$V_{SS} \le V_{IN} \le V_{DD}$
Input resistance	R_{IN}	10			MΩ	
Input offset voltage	V_{OS}			25	mV	
Power supply rejection	PSRR	50			dB	1 kHz
Common mode rejection	CMRR	40			dB	0.75 V ≤ V_{IN} ≤ 4.25 V biased at V_{Ref}=2.5 V
DC open loop voltage gain	A_{VOL}	32			dB	
Unity gain bandwidth	f_C	0.30			MHz	
Output voltage swing	V_O	4.0			V_{pp}	Load ≥ 100 kΩ to V_{SS} @ GS
Maximum capacitive load (GS)	C_L			100	pF	
Resistive load (GS)	R_L			50	kΩ	
Common mode range	V_{CM}	2.5			V_{pp}	No Load

3870D AC Electrical Characteristics - V_{DD}=5.0V ±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C , using Test Circuit shown in Figure 10.

Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
Valid input signal levels (each tone of composite signal)		-29		+1	dBm	1,2,3,5,6,9
		27.5		869	mV_{RMS}	1,2,3,5,6,9
Negative twist accept				8	dB	2,3,6,9,12
Positive twist accept				8	dB	2,3,6,9,12
Frequency deviation accept		±1.5% ± 2 Hz				2,3,5,9
Frequency deviation reject		±3.5%				2,3,5,9
Third tone tolerance			-16		dB	2,3,4,5,9,10
Noise tolerance			-12		dB	2,3,4,5,7,9,10
Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

ical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

TES
3m= decibels above or below a reference power of 1 mW into a 600 ohm load.
git sequence consists of all DTMF tones.
ne duration= 40 ms, tone pause= 40 ms.
gnal condition consists of nominal DTMF frequencies.
th tones in composite signal have an equal amplitude.
ne pair is deviated by ±1.5 %± 2 Hz.
andwidth limited (3 kHz) Gaussian noise.
e precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
r an error rate of better than 1 in 10,000.
eferenced to lowest level frequency component in DTMF signal.
eferenced to the minimum valid accept level.
uaranteed by design and characterization.

MT8870D-1 AC Electrical Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C , using Test Circuit shown in Figure 10.

	Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	Valid input signal levels (each tone of composite signal)		-31		+1	dBm	Tested at V_{DD}=5.0V 1,2,3,5,6,9
			21.8		869	mV_{RMS}	
2	Input Signal Level Reject		-37			dBm	Tested at V_{DD}=5.0V 1,2,3,5,6,9
			10.9			mV_{RMS}	
3	Negative twist accept				8	dB	2,3,6,9,13
4	Positive twist accept				8	dB	2,3,6,9,13
5	Frequency deviation accept		±1.5%± 2 Hz				2,3,5,9
6	Frequency deviation reject		±3.5%				2,3,5,9
7	Third zone tolerance			-18.5		dB	2,3,4,5,9,12
8	Noise tolerance			-12		dB	2,3,4,5,7,9,10
9	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

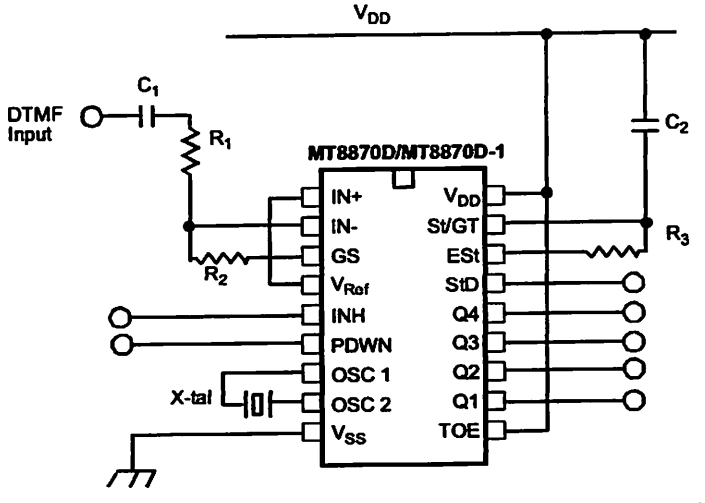
*NOTES
1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5 %± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Referenced to Fig. 10 input DTMF tone level at -25dBm (-28dBm at GS Pin) interference frequency range between 480-3400Hz.
13. Guaranteed by design and characterization.

Electrical Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ To ≤ +85°C , using Test Circuit shown in Figure 10.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
TIMING	Tone present detect time	t_{DP}	5	11	14	ms	Note 1
	Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 1
	Tone duration accept	t_{REC}			40	ms	Note 2
	Tone duration reject	$t_{\overline{REC}}$	20			ms	Note 2
	Interdigit pause accept	t_{ID}			40	ms	Note 2
	Interdigit pause reject	t_{DO}	20			ms	Note 2
OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	µs	TOE=V_{DD}
	Propagation delay (St to StD)	t_{PStD}		12	16	µs	TOE=V_{DD}
	Output data set up (Q to StD)	t_{QStD}		3.4		µs	TOE=V_{DD}
	Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	load of 10 kΩ, 50 pF
	Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	load of 10 kΩ, 50 pF
PDWN	Power-up time	t_{PU}		30		ms	Note 3
	Power-down time	t_{PD}		20		ms	
CLOCK	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
	Clock input rise time	t_{LHCL}			110	ns	Ext. clock
	Clock input fall time	t_{HLCL}			110	ns	Ext. clock
	Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
	Capacitive load (OSC2)	C_{LO}			30	pF	

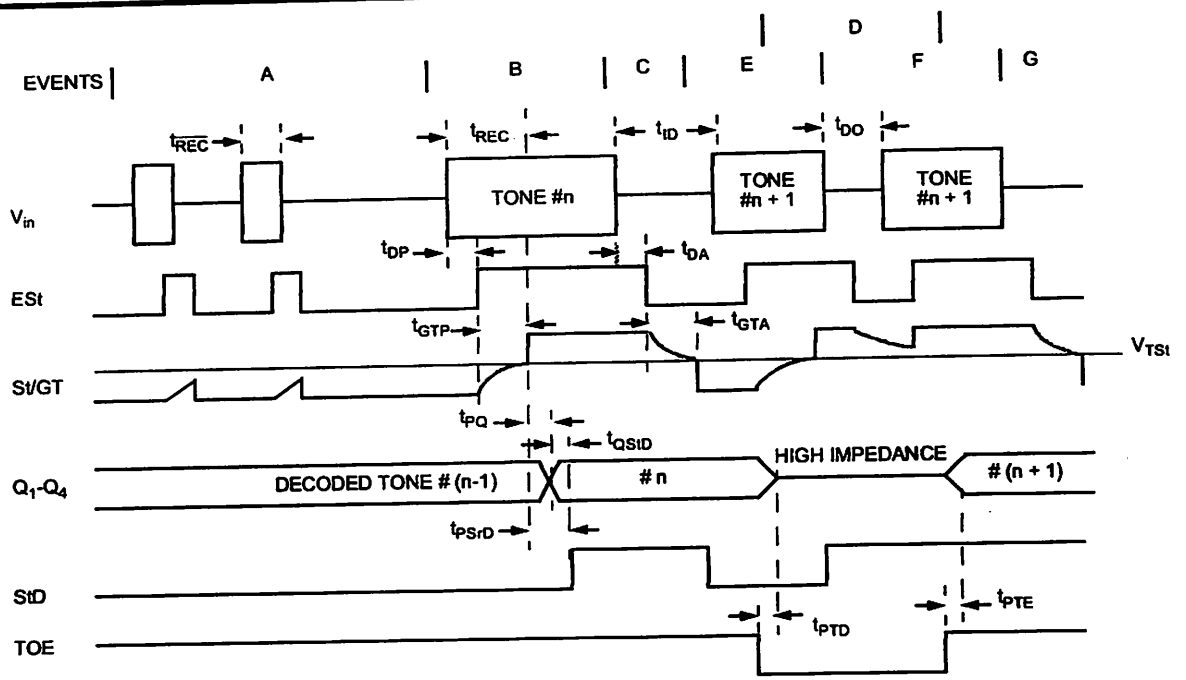
ical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

ES:
Used for guard-time calculation purposes only.
These, user adjustable parameters, are not device specifications. The adjustable settings of these minimums and maximums are recommendations based upon network requirements.
With valid tone present at input, t_{PU} equals time from PDWN going low until ESt going high.



NOTES:
R_1,R_2=100KΩ ± 1%
R_3=300KΩ ± 1%
C_1,C_2=100 nF ± 5%
X-tal=3.579545 MHz ± 0.1%

Figure 10 - Single-Ended Input Configuration



EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.

B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS

C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMIAN LATCHED UNTIL NEXT VALID TONE.

D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.

E) TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE).

F) ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED.

G) END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

EXPLANATION OF SYMBOLS

V_{in} DTMF COMPOSITE INPUT SIGNAL.

ESt EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.

St/GT STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.

Q_1-Q_4 4-BIT DECODED TONE OUTPUT.

StD DELAYED STEERING OUTPUT. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL.

TOE TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE.

$\overline{t_{REC}}$ MAXIMUM DTMF SIGNAL DURATION NOT DETECED AS VALID

t_{REC} MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION

t_{ID} MAXIMUM TIME BETWEEN VALID DTMF SIGNALS.

t_{DO} MAXIMUM ALLOWABLE DROP OUT DURING VALID DTMF SIGNAL.

t_{DP} TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS.

t_{DA} TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS.

t_{GTP} GUARD TIME, TONE PRESENT.

t_{GTA} GUARD TIME, TONE ABSENT.

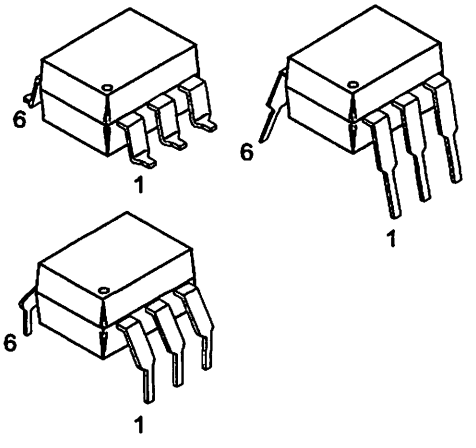
Figure 11 - Timing Diagram

FAIRCHILD
SEMICONDUCTOR®

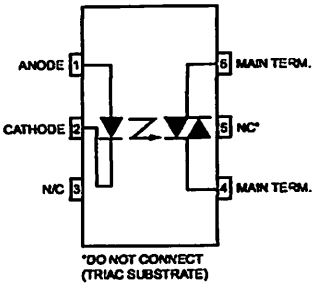
6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

)C3010M MOC3011M MOC3012M MOC3020M MOC3021M MOC3022M MOC3023M

PACKAGE



SCHEMATIC



ESCRIPTION

MOC301XM and MOC302XM series are optically isolated triac driver devices. These devices contain a GaAs infrared tting diode and a light activated silicon bilateral switch, which functions like a triac. They are designed for interfacing between ctronic controls and power triacs to control resistive and inductive loads for 115 VAC operations.

EATURES

- Excellent I_{FT} stability—IR emitting diode has low degradation
- High isolation voltage—minimum 5300 VAC RMS
- Underwriters Laboratory (UL) recognized—File #E90700
- Peak blocking voltage
  - 250V-MOC301XM
  - 400V-MOC302XM
- VDE recognized (File #94766)
  - Ordering option V (e.g. MOC3023VM)

PPLICATIONS

- Industrial controls
- Traffic lights
- Vending machines
- Solid state relay
- Lamp ballasts
- Solenoid/valve controls
- Static AC power switch
- Incandescent lamp dimmers
- Motor control

6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

\BSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

arameters	Symbol	Device	Value	Units
OTAL DEVICE				
torage Temperature	T_{STG}	All	-40 to +150	°C
perating Temperature	T_{OPR}	All	-40 to +85	°C
ead Solder Temperature	T_{SOL}	All	260 for 10 sec	°C
unction Temperature Range	T_J	All	-40 to +100	°C
olation Surge Voltage[1] eak AC voltage, 60Hz, 1 sec duration)	V_{ISO}	All	7500	Vac(pk)
otal Device Power Dissipation @ 25°C	P_D	All	330	mW
erate above 25°C			4.4	mW/°C
MITTER				
ontinuous Forward Current	I_F	All	60	mA
everse Voltage	V_R	All	3	V
otal Power Dissipation 25°C Ambient	P_D	All	100	mW
erate above 25°C			1.33	mW/°C
ETECTOR				
ff-State Output Terminal Voltage	V_{DRM}	MOC3010M/1M/2M MOC3020M/1M/2M/3M	250 400	V
eak Repetitive Surge Current (PW = 1 ms, 120 pps)	I_{TSM}	All	1	A
otal Power Dissipation @ 25°C Ambient	P_D	All	300	mW
erate above 25°C			4	mW/°C

te

Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

LECTRICAL CHARACTERISTICS (T_A = 25°C Unless otherwise specified)

NDIVIDUAL COMPONENT CHARACTERISTICS

Parameters	Test Conditions	Symbol	Device	Min	Typ	Max	Units
MITTER							
put Forward Voltage	I_F = 10 mA	V_F	All		1.15	1.5	V
everse Leakage Current	V_R = 3 V, T_A = 25°C	I_R	All		0.01	100	µA
ETECTOR							
eak Blocking Current,Either Direction	Rated V_{DRM}, I_F = 0 (note 1)	I_{DRM}	All		10	100	nA
eak On-State Voltage,Either Direction	I_{TM} = 100 mA peak, I_F = 0	V_{TM}	All		1.8	3	V

RANSFER CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

C Characteristics	Test Conditions	Symbol	Device	Min	Typ	Max	Units
ED Trigger Current	Voltage = 3V (note 3)	I_{FT}	MOC3020M			30	mA
			MOC3010M			15	
			MOC3021M				
			MOC3011M			10	
			MOC3022M				
			MOC3012M			5	
			MOC3023M				
lolding Current, Either Direction		I_H	All		100		µA

ote

Test voltage must be applied within dv/dt rating.

This is static dv/dt. See Figure 5 for test circuit. Commutating dv/dt is a function of the load-driving thyristor(s) only.

All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (30 mA for MOC3020M, 15 mA for MOC3010M and MOC3021M, 10 mA for MOC3011M and MOC3022M, 5 mA for MOC3012M and MOC3023M) and absolute max I_F (60 mA).

6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

MOC3010M MOC3011M MOC3012M MOC3020M MOC3021M MOC3022M MOC3023M

Fig. 1 LED Forward Voltage vs. Forward Current

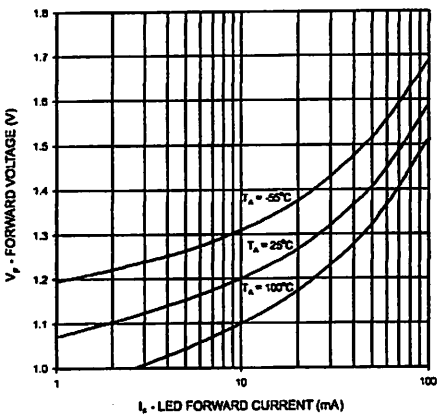


Fig. 2 On-State Characteristics

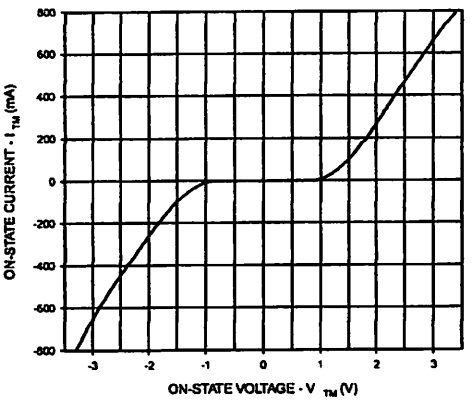


Fig. 3 Trigger Current vs. Ambient Temperature

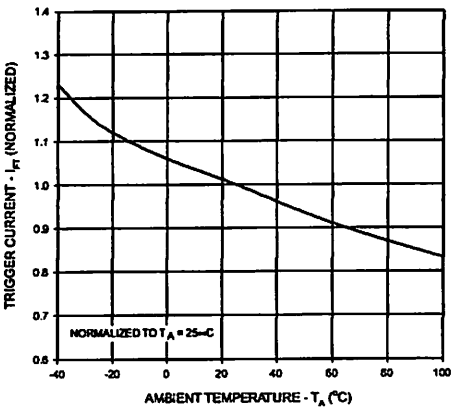


Fig. 4 LED Current Required to Trigger vs. LED Pulse Width

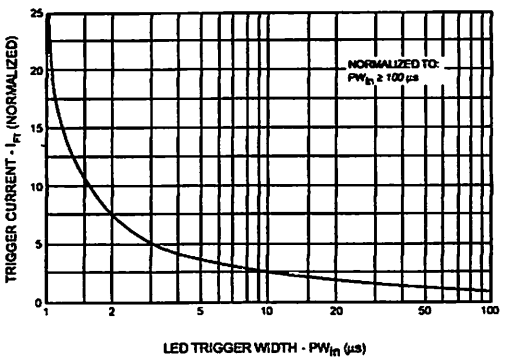


Fig. 5 dv/dt vs. Temperature

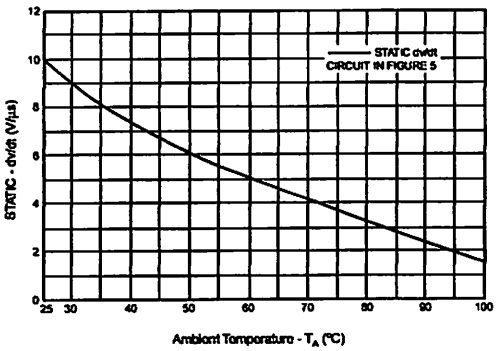
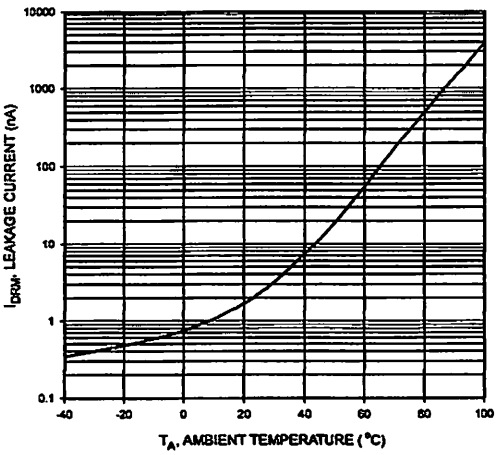
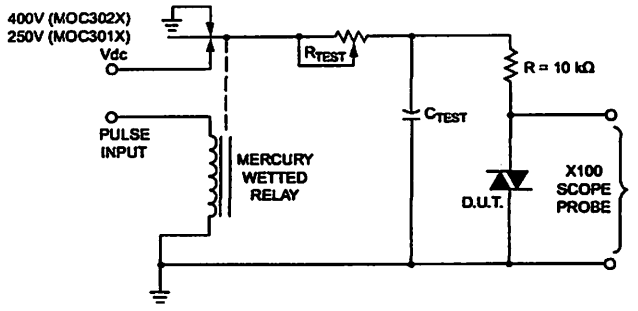


Fig. 6 Leakage Current, I_{DRM} vs. Temperature





1. The mercury wetted relay provides a high speed repeated pulse to the D.U.T.
2. 100x scope probes are used, to allow high speeds and voltages.
3. The worst-case condition for static dv/dt is established by triggering the D.U.T. with a normal LED input current, then removing the current. The variable R_{TEST} allows the dv/dt to be gradually increased until the D.U.T. continues to trigger in response to the applied voltage pulse, even after the LED current has been removed. The dv/dt is then decreased until the D.U.T. stops triggering. τ_{RC} is measured at this point and recorded.

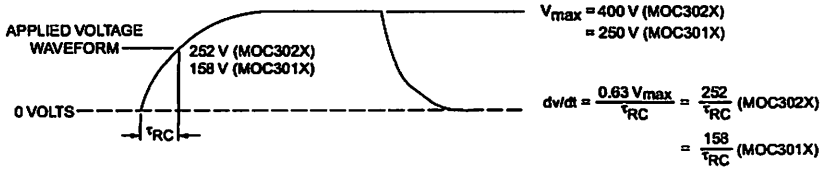


Figure 5. Static dv/dt Test Circuit

Note: This optoisolator should not be used to drive a load directly. It is intended to be a trigger device only.

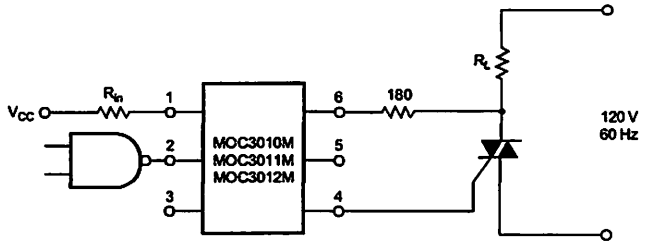


Figure 6. Resistive Load

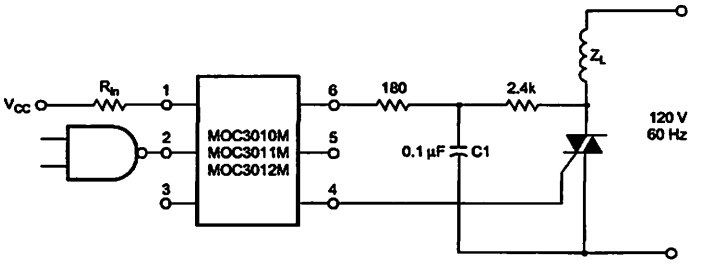


Figure 7. Inductive Load with Sensitive Gate Triac ($I_{GT} \leq 15$ mA)

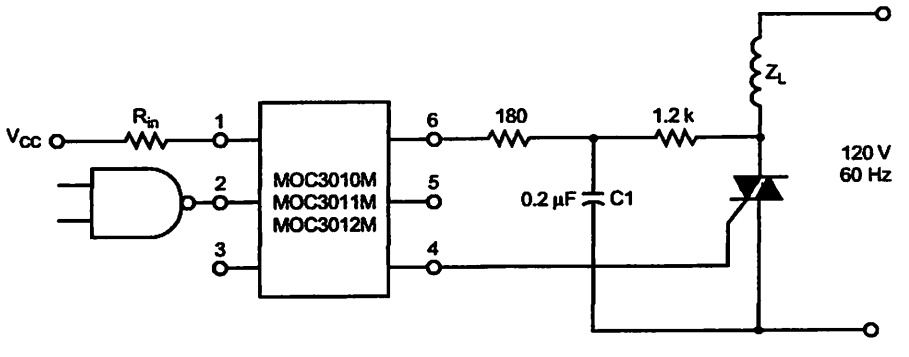
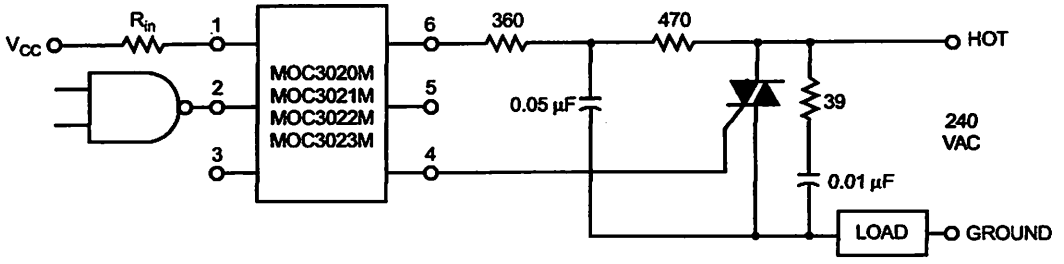


Figure 8. Inductive Load with Sensitive Gate Triac ($I_{GT} \leq 15$ mA)



In this circuit the "hot" side of the line is switched and the load connected to the cold or ground side.

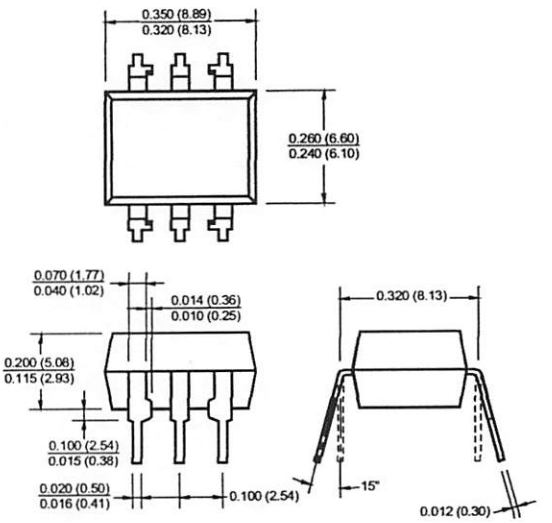
The 39 ohm resistor and 0.01µF capacitor are for snubbing of the triac, and the 470 ohm resistor and 0.05 µF capacitor are for snubbing the coupler. These components may or may not be necessary depending upon the particular and load used.

Figure 9. Typical Application Circuit

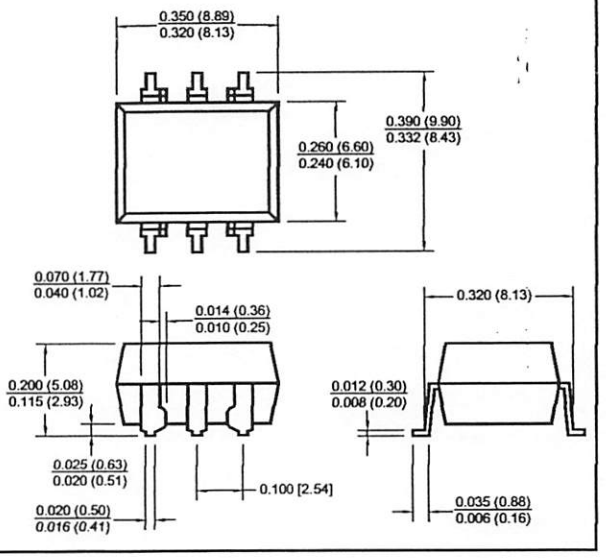
6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

MOC3010M MOC3011M MOC3012M MOC3020M MOC3021M MOC3022M MOC3023M

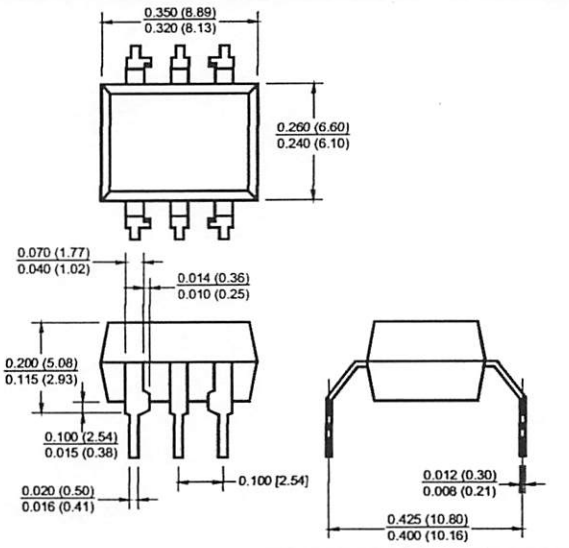
Package Dimensions (Through Hole)



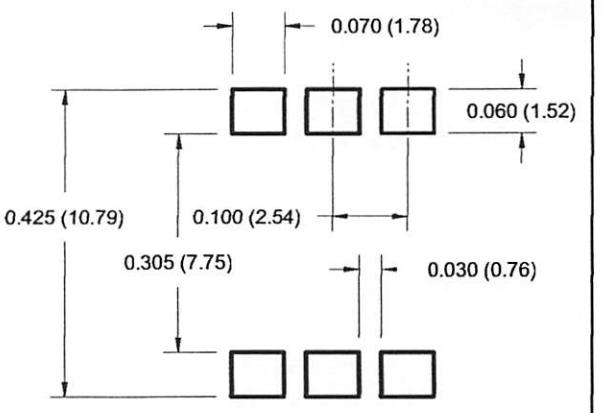
Package Dimensions (Surface Mount)



Package Dimensions (0.4" Lead Spacing)



Recommended Pad Layout for Surface Mount Leadform

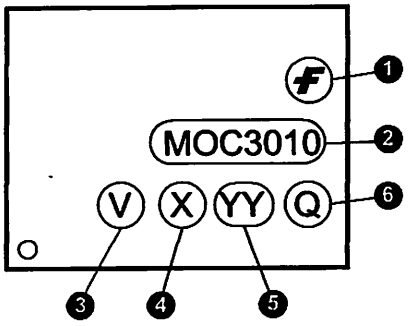


NOTE
All dimensions are in inches (millimeters)

ORDERING INFORMATION

Option	Order Entry Identifier	Description
S	S	Surface Mount Lead Bend
SR2	SR2	Surface Mount; Tape and reel
T	T	0.4" Lead Spacing
V	V	VDE 0884
TV	TV	VDE 0884, 0.4" Lead Spacing
SV	SV	VDE 0884, Surface Mount
SR2V	SR2V	VDE 0884, Surface Mount, Tape & Reel

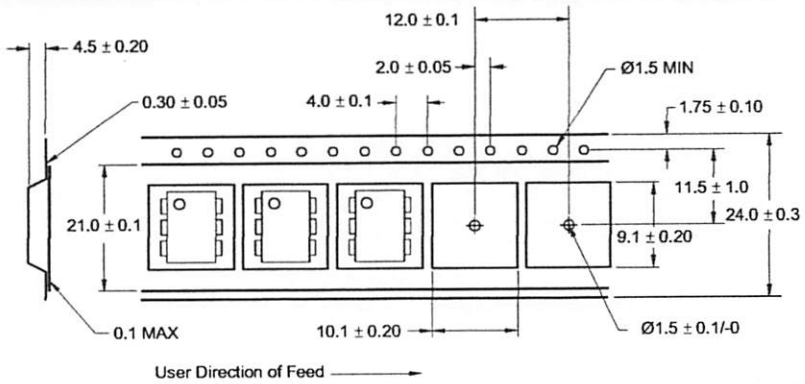
MARKING INFORMATION



Definitions	
1	*Fairchild logo*
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., '3'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

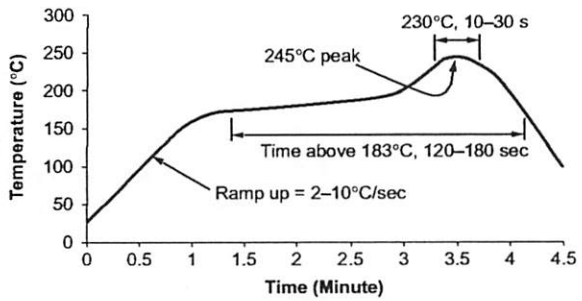
*Note – Parts that do not have the 'V' option (see definition 3 above) that are marked with date code '325' or earlier are marked in portrait format.

Carrier Tape Specifications



NOTE
All dimensions are in inches (millimeters)

Reflow Profile (White Package, -M Suffix)



- Peak reflow temperature: 245°C (package surface temperature)
- Time of temperature higher than 183°C for 120–180 seconds
- One time soldering reflow is recommended

GENERAL DESCRIPTION

Passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

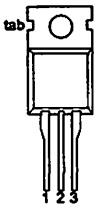
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
	BT136- BT136-	600 600F	
V_{DRM}	Repetitive peak off-state voltages	600	V
$I_{T(RMS)}$	RMS on-state current	4	A
I_{TSM}	Non-repetitive peak on-state current	25	A

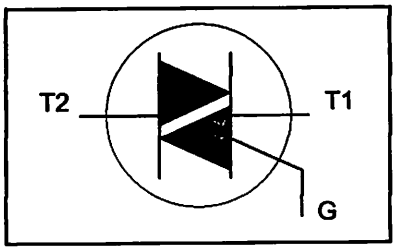
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{DRM}	Repetitive peak off-state voltages			-	600[1]	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ °C		-	4	A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25$ °C prior to surge				
		t = 20 ms		-	25	A
		t = 16.7 ms		-	27	A
I^2t	I^2t for fusing	t = 10 ms		-	3.1	A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs				
			T2+ G+	-	50	A/µs
			T2+ G-	-	50	A/µs
			T2- G-	-	50	A/µs
			T2- G+	-	10	A/µs
I_{GM}	Peak gate current			-	2	A
V_{GM}	Peak gate voltage			-	5	V
P_{GM}	Peak gate power			-	5	W
$P_{G(AV)}$	Average gate power	over any 20 ms period		-	0.5	W
T_{stg}	Storage temperature			-40	150	°C
T_j	Operating junction temperature			-	125	°C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	3.0	K/W
		half cycle	-	-	3.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.		UNIT
		BT136-			...	...F	
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A					
		T2+ G+	-	5	35	25	mA
		T2+ G-	-	8	35	25	mA
		T2- G-	-	11	35	25	mA
		T2- G+	-	30	70	70	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A					
		T2+ G+	-	7	20	20	mA
		T2+ G-	-	16	30	30	mA
		T2- G-	-	5	20	20	mA
		T2- G+	-	7	30	30	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	5	15	15	mA
V_T	On-state voltage	I_T = 5 A	-	1.4	1.70		V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5		V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C	0.25	0.4	-		V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 °C	-	0.1	0.5		mA

DYNAMIC CHARACTERISTICS

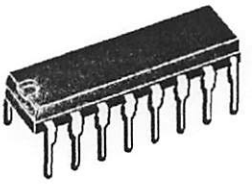
T_j = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.		TYP.	MAX.	UNIT
		BT136-	...	...F			
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 °C; exponential waveform; gate open circuit	100	50	250	-	V/µs
dV_{com}/dt	Critical rate of change of commutating voltage	V_{DM} = 400 V; T_j = 95 °C; $I_{T(RMS)}$ = 4 A; dI_{com}/dt = 1.8 A/ms; gate open circuit	-	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	2	-	µs

ULN2001A-ULN2002A
ULN2003A-ULN2004A

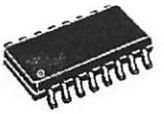
SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500mA PER DRIVER (600mA PEAK)
- OUTPUT VOLTAGE 50V
- INTEGRATED SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT



DIP16

ORDERING NUMBERS: ULN2001A/2A/3A/4A



SO16

ORDERING NUMBERS: ULN2001D/2D/3D/4D

DESCRIPTION

The ULN2001A, ULN2002A, ULN2003 and ULN2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel rated at 500mA and can withstand peak currents of 600mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

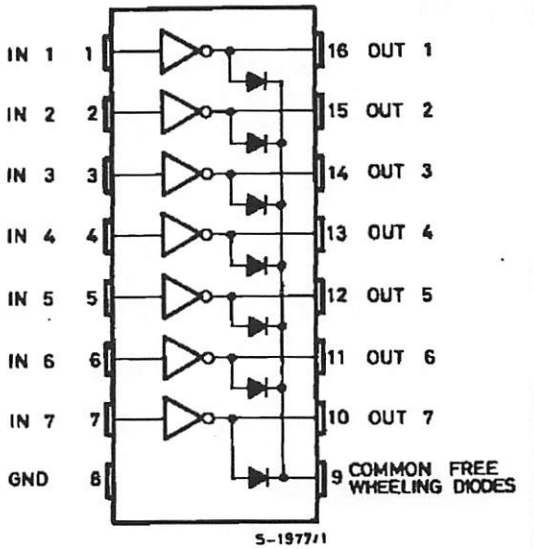
The four versions interface to all common logic families :

ULN2001A	General Purpose, DTL, TTL, PMOS, CMOS
ULN2002A	14-25V PMOS
ULN2003A	5V TTL, CMOS
ULN2004A	6–15V CMOS, PMOS

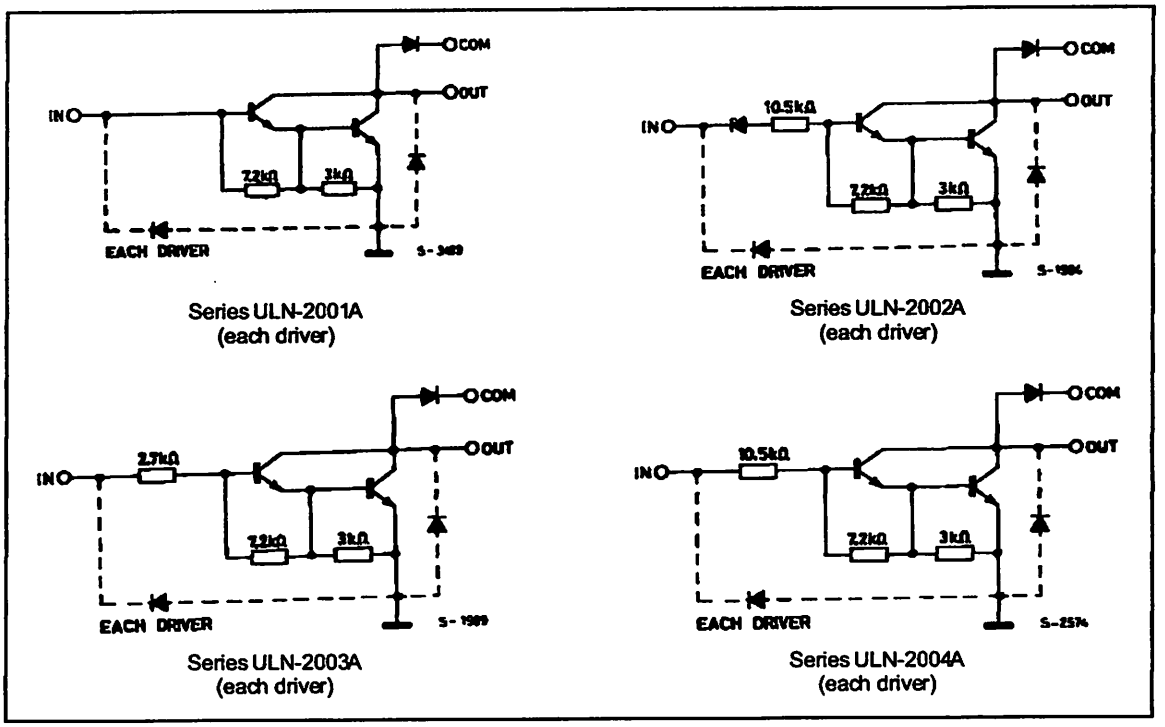
These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal printheads and high power buffers.

The ULN2001A/2002A/2003Aand 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D/2002D/2003D/2004D.

PIN CONNECTION



SCHEMATIC DIAGRAM



Series ULN-2001A (each driver)

Series ULN-2002A (each driver)

Series ULN-2003A (each driver)

Series ULN-2004A (each driver)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULN2002A/D - 2003A/D - 2004A/D)	30	V
I_c	Continuous Collector Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
T_j	Junction Temperature	150	°C

THERMAL DATA

Symbol	Parameter		DIP16	SO16	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	70	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50V			50	µA	1a
		T_{amb} = 70°C, V_{CE} = 50V			100	µA	1a
		T_{amb} = 70°C for ULN2002A V_{CE} = 50V, V_i = 6V			500	µA	1b
		for ULN2004A V_{CE} = 50V, V_i = 1V			500	µA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100mA, I_B = 250µA		0.9	1.1	V	2
		I_C = 200 mA, I_B = 350µA		1.1	1.3	V	2
		I_C = 350mA, I_B = 500µA		1.3	1.6	V	2
$I_{i(on)}$	Input Current	for ULN2002A, V_i = 17V		0.82	1.25	mA	3
		for ULN2003A, V_i = 3.85V		0.93	1.35	mA	3
		for ULN2004A, V_i = 5V		0.35	0.5	mA	3
		V_i = 12V		1	1.45	mA	3
$I_{i(off)}$	Input Current	T_{amb} = 70°C, I_C = 500µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	V_{CE} = 2V for ULN2002A I_C = 300mA			13	V	5
		for ULN2003A I_C = 200mA			2.4		
		I_C = 250mA			2.7		
		I_C = 300mA			3		
		for ULN2004A I_C = 125mA			5		
		I_C = 200mA			6		
		I_C = 275mA			7		
		I_C = 350mA			8		
h_{FE}	DC Forward Current Gain	for ULN2001A V_{CE} = 2V, I_C = 350mA	1000				2
C_i	Input Capacitance			15	25	pF	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	
I_R	Clamp Diode Leakage Current	V_R = 50V			50	µA	6
		T_{amb} = 70°C, V_R = 50V			100	µA	6
V_F	Clamp Diode Forward Voltage	I_F = 350mA		1.7	2	V	7

TEST CIRCUITS

Figure 1a.

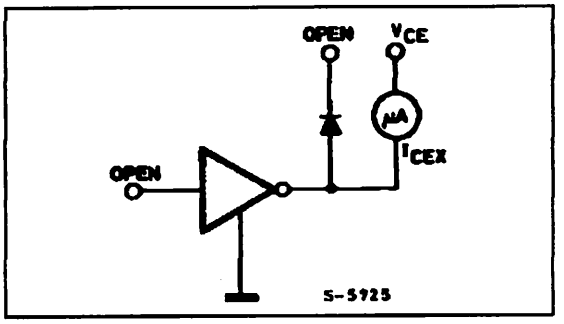


Figure 1b.

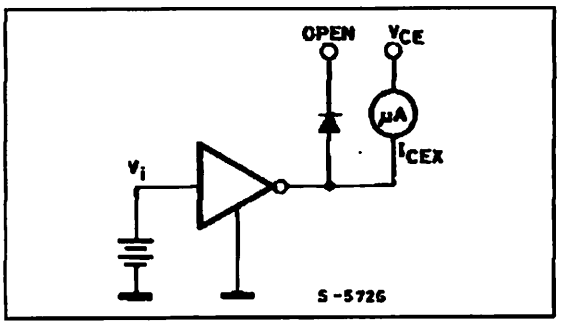


Figure 2.

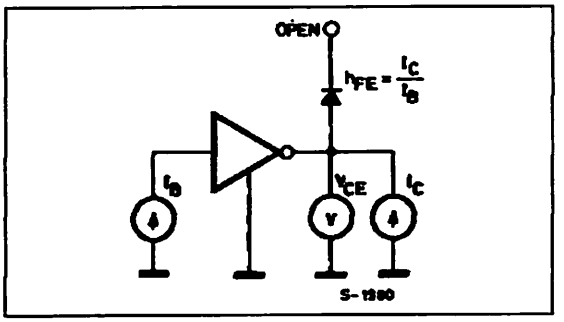


Figure 3.

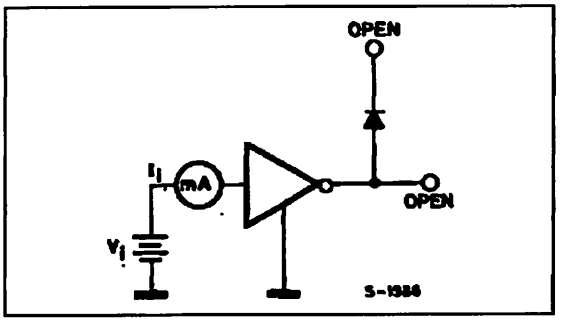


Figure 4.

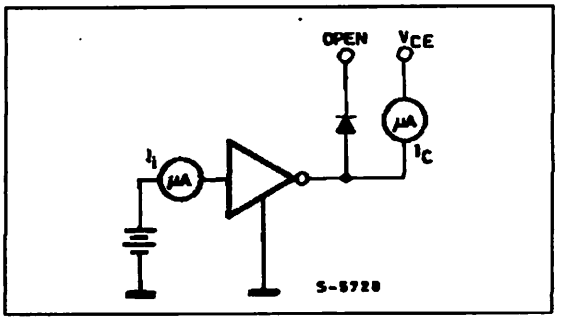


Figure 5.

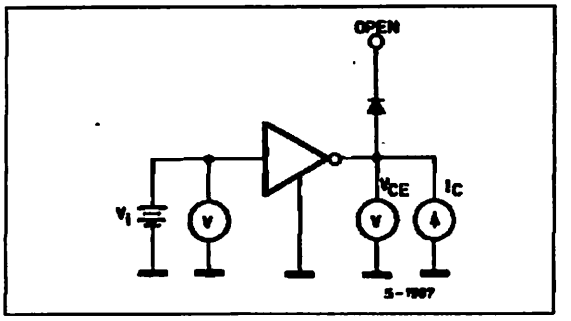


Figure 6.

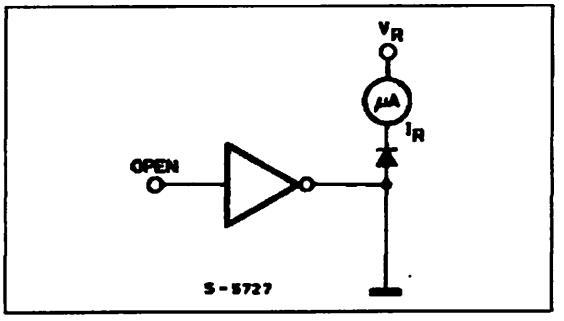


Figure 7.

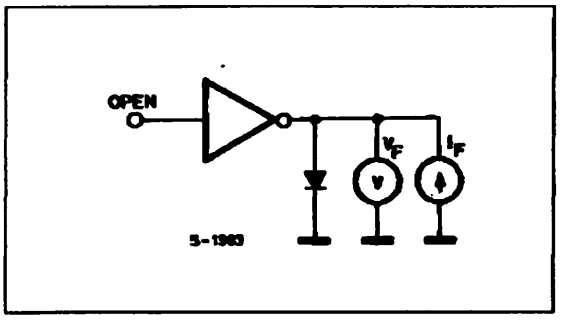


Figure 8: Collector Current versus Input Current

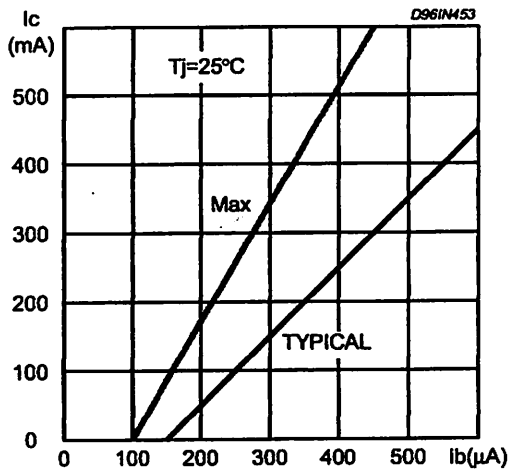


Figure 9: Collector Current versus Saturation Voltage

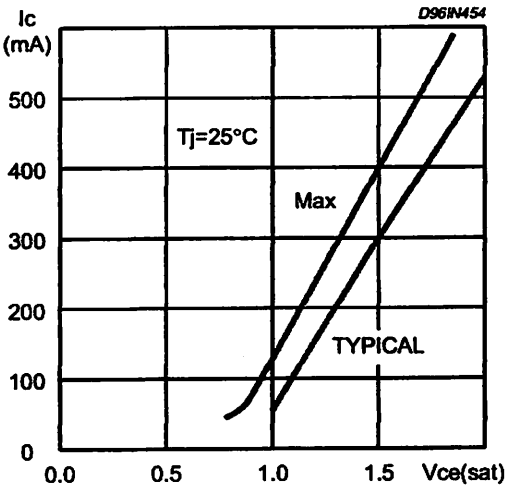


Figure 10: Peak Collector Current versus Duty Cycle

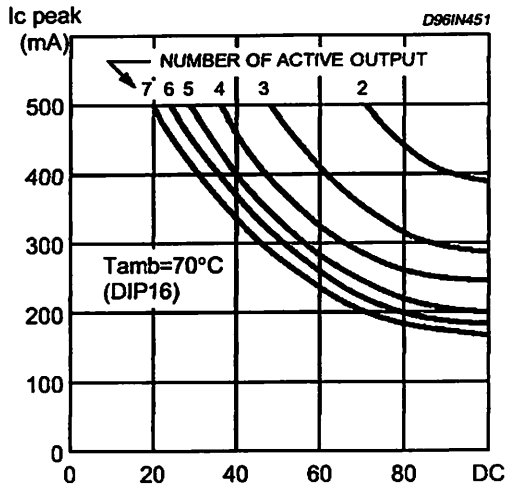
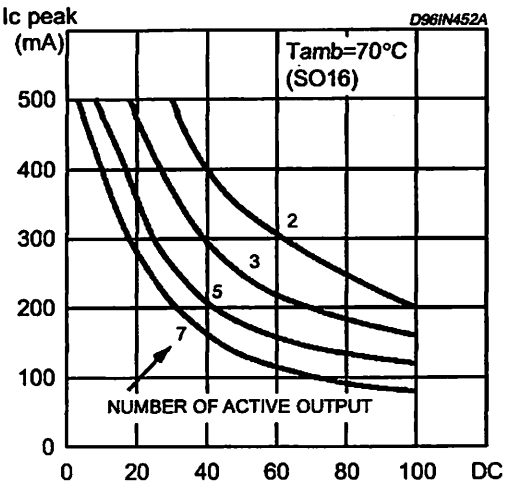
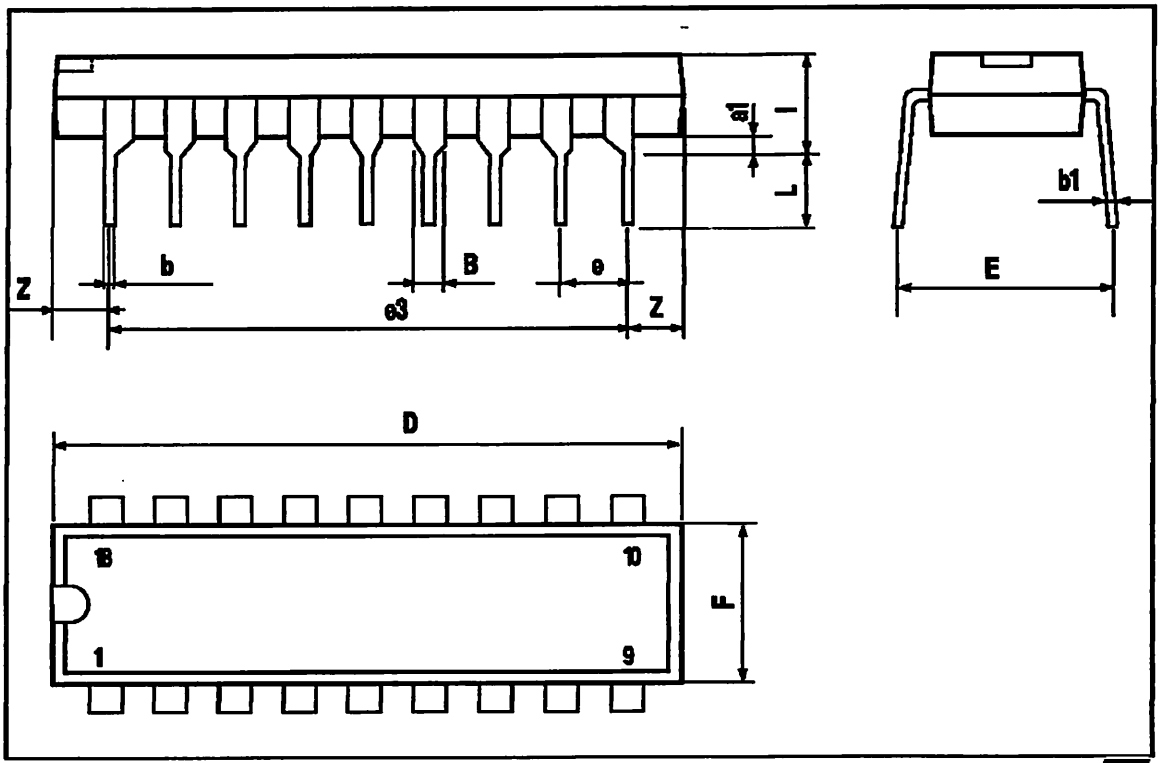


Figure 11: Peak Collector Current versus Duty Cycle



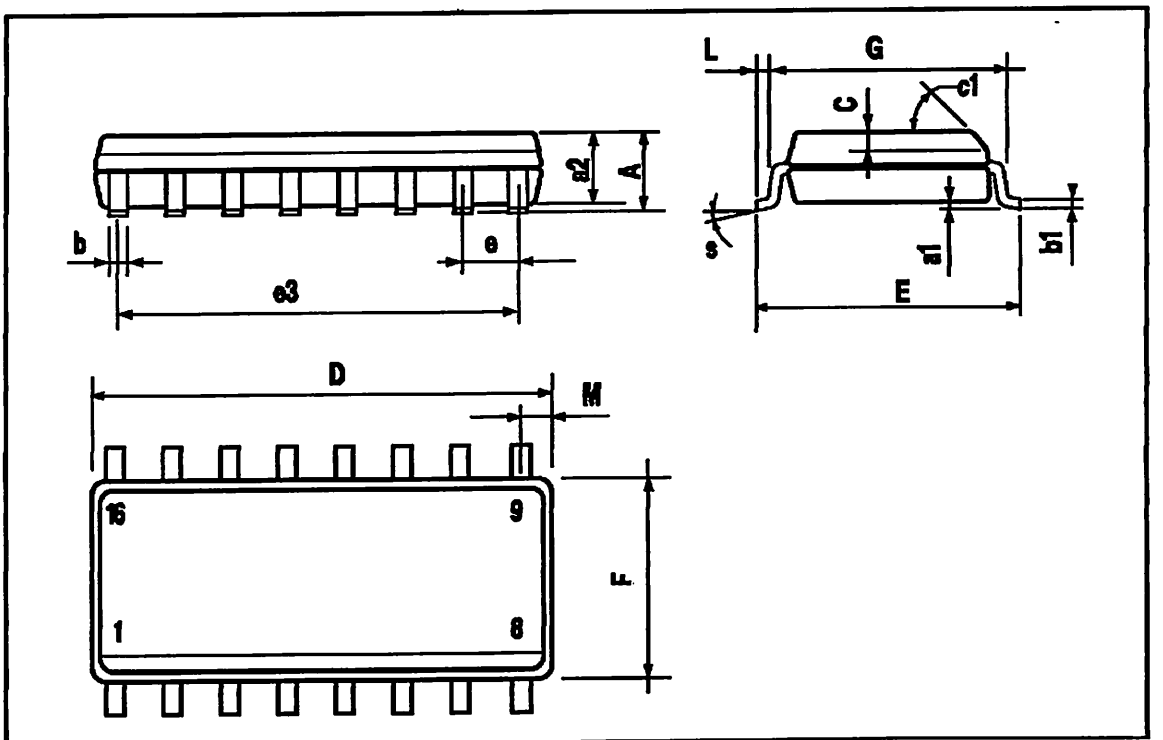
DIP16 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO16 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45 (typ.)					
D	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.62			0.024
S	8 (max.)					



Features

- Compatible with MCS®-51 Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)
- Green (Pb/Halide-free) Packaging Option

8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

1. Description

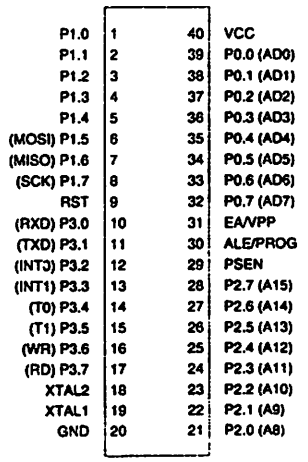
The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of In-System Programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

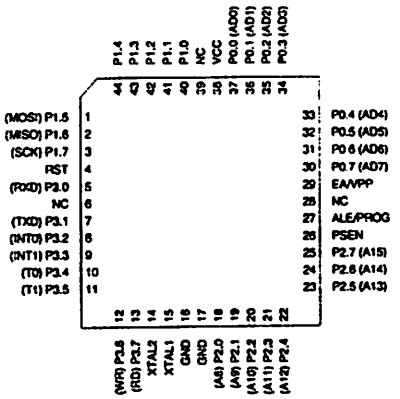
2487C–MICRO–03/05

2. Pin Configurations

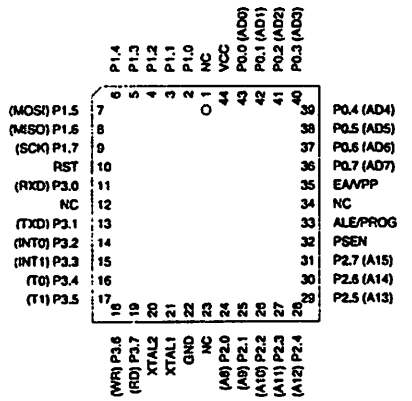
2.1 40-lead PDIP



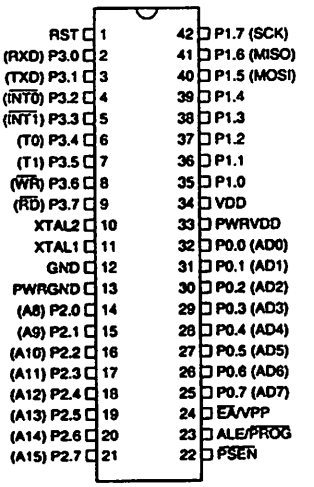
2.2 44-lead TQFP



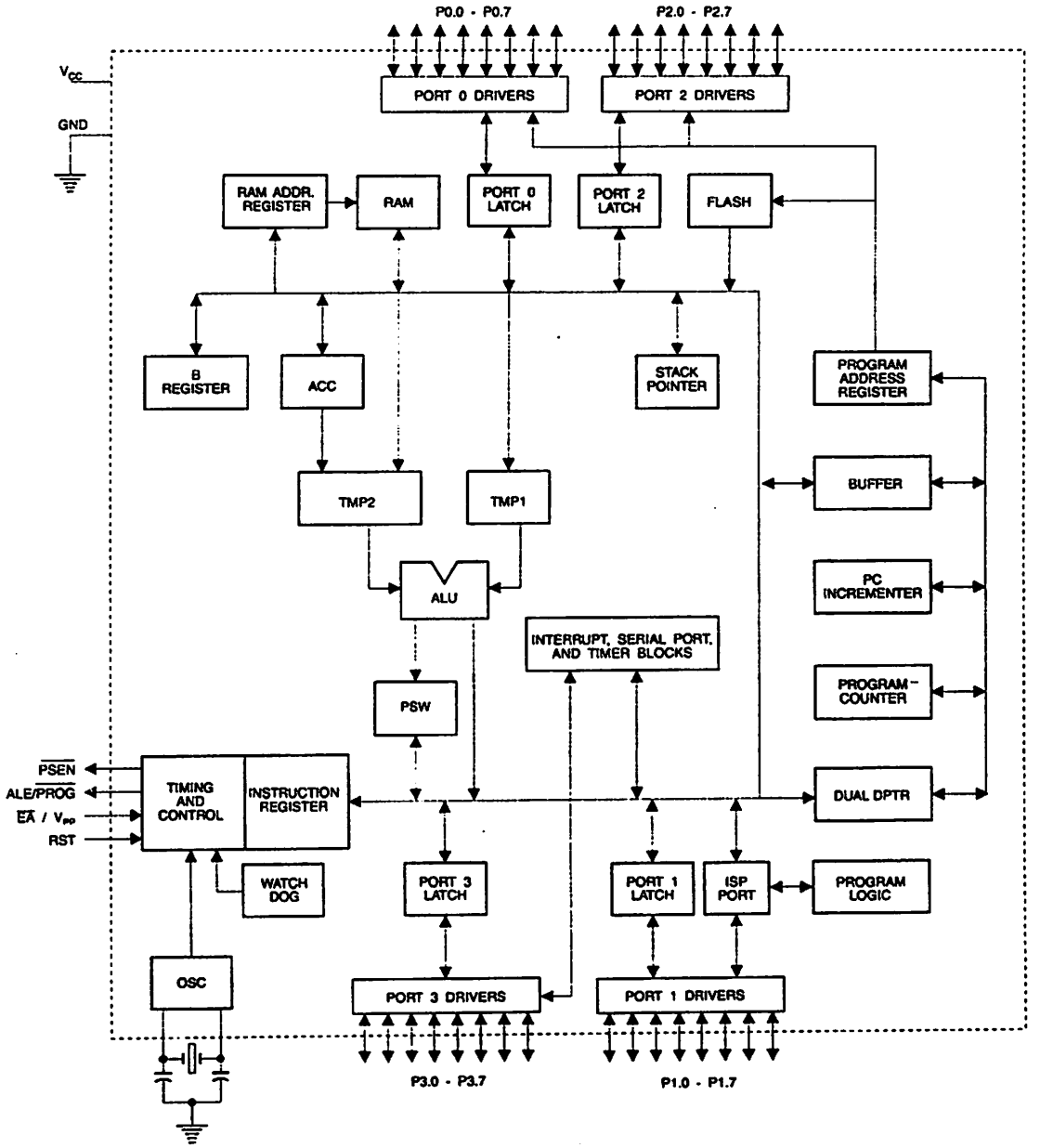
2.3 44-lead PLCC



2.4 42-lead PDIP



3. Block Diagram



4. Pin Description

4.1 VCC

Supply voltage (all packages except 42-PDIP).

4.2 GND

Ground (all packages except 42-PDIP; for 42-PDIP GND connects only the logic core and the embedded program memory).

4.3 VDD

Supply voltage for the 42-PDIP which connects only the logic core and the embedded program memory.

4.4 PWRVDD

Supply voltage for the 42-PDIP which connects only the I/O Pad Drivers. The application board **MUST** connect both VDD and PWRVDD to the board supply voltage.

4.5 PWRGND

Ground for the 42-PDIP which connects only the I/O Pad Drivers. PWRGND and GND are weakly connected through the common silicon substrate, but not through any metal link. The application board **MUST** connect both GND and PWRGND to the board ground.

4.6 Port 0

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

4.7 Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

4.8 Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

4.9 Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

4.10 RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

4.11 ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

4.12 $\overline{\text{PSEN}}$

Program Store Enable ($\overline{\text{PSEN}}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

4.13 $\overline{\text{EA}}$/VPP

External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

4.14 XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

4.15 XTAL2

Output from the inverting oscillator amplifier

5. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 5-1. AT89S51 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H									0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 5-2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

–	Reserved for future expansion
DISALE	Disable/Enable ALE
	DISALE Operating Mode
	0 ALE is emitted at a constant rate of 1/6 the oscillator frequency
	1 ALE is active only during a MOVX or MOVC instruction
DISRTO	Disable/Enable Reset-out
	DISRTO
	0 Reset pin is driven High after WDT times out
	1 Reset pin is input only
WDIDLE	Disable/Enable WDT in IDLE mode
WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 5-3. AUXR1: Auxiliary Register 1

AUXR1 Address = A2H — Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

6. Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

6.1 Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

6.2 Data Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

7. Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

7.1 Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least

every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

7.2 WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

8. UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

9. Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

10. Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 10-1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10-1 shows that bit positions IE.6 and IE.5 are unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

Table 10-1. Interrupt Enable (IE) Register

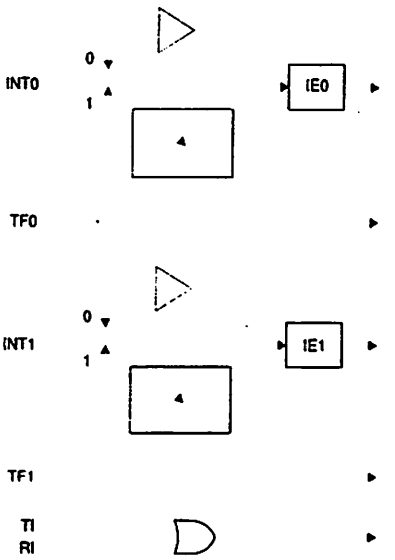
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

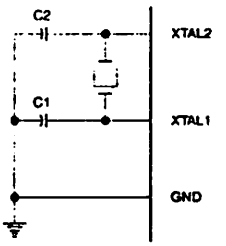
Figure 10-1. Interrupt Sources



11. Oscillator Characteristics

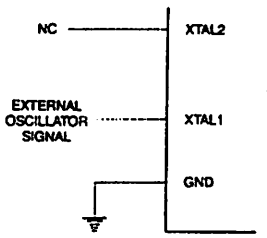
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11-1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 11-2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11-1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 11-2. External Clock Drive Configuration



12. Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

13. Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt ($\overline{INT0}$ or $\overline{INT1}$). Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 13-1. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

14. Program Memory Lock Bits

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in Table 14-1.

Table 14-1. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

15. Programming the Flash – Parallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash Programming Modes table (Table 17-1) and Figure 17-1 and Figure 17-2. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. **The status of the individual lock bits can be verified directly by reading them back.**

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates AT89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

16. Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

16.1 Serial Programming Algorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   a. Apply power between VCC and GND pins.
   b. Set RST pin to "H".

If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.

5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

1. Set XTAL1 to "L" (if a crystal is not used).
2. Set RST to "L".
3. Turn V_{CC} power off.

Data Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

16.2 Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in the "Serial Programming Instruction Set" on page 20.

17. Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer worldwide support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 17-1. Flash Programming Modes

Mode	V_{CC}	RST	$\overline{\text{PSEN}}$	ALE/ $\overline{\text{PROG}}$	$\overline{\text{EA}}$/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

Notes:
1. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{\text{BSY}}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 17-1. Programming the Flash Memory (Parallel Mode)

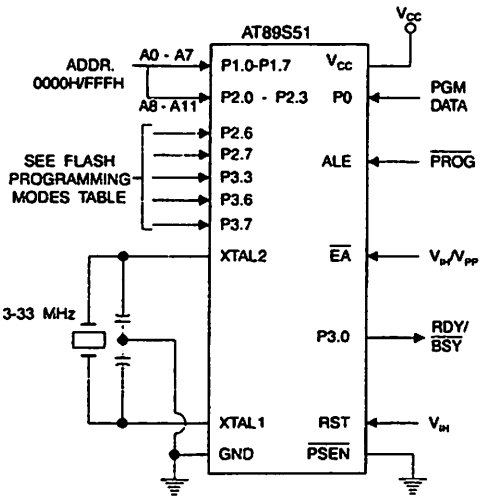
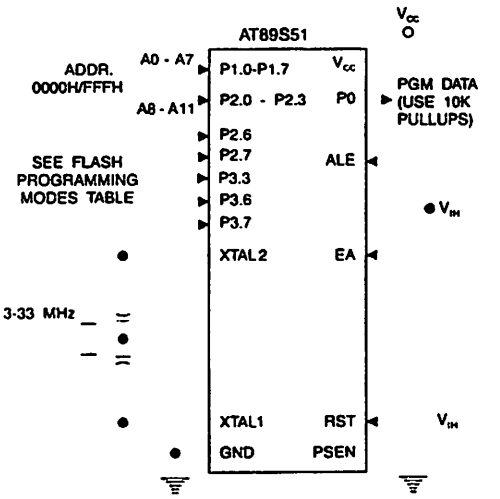


Figure 17-2. Verifying the Flash Memory (Parallel Mode)



18. Flash Programming and Verification Characteristics (Parallel Mode)

T_A = 20°C to 30°C, V_{CC} = 4.5 to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
t_{GHAX}	Address Hold After $\overline{PROG}$	48 t_{CLCL}		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
t_{GHDX}	Data Hold After $\overline{PROG}$	48 t_{CLCL}		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48 t_{CLCL}		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	0.2	1	µs
t_{AVQV}	Address to Data Valid		48t_{CLCL}	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		48t_{CLCL}	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	48t_{CLCL}	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		50	µs

Figure 18-1. Flash Programming and Verification Waveforms – Parallel Mode

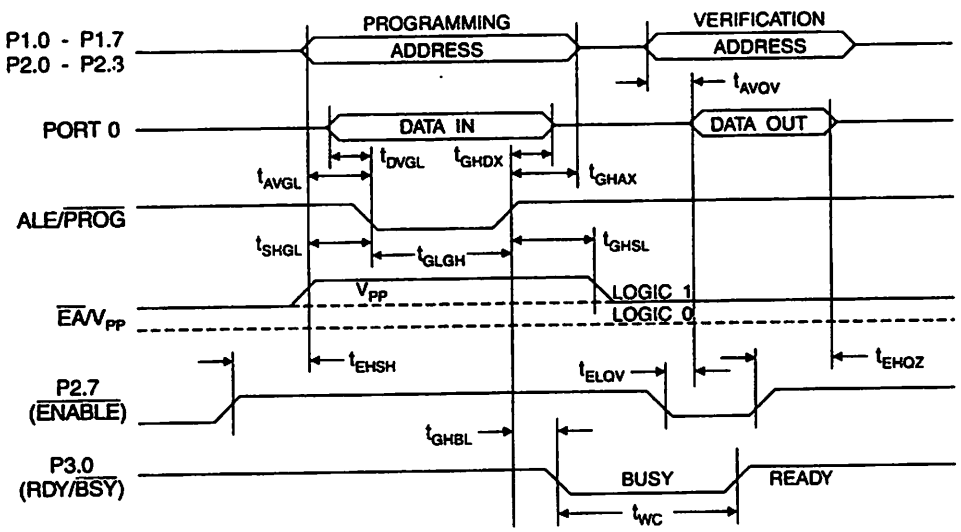
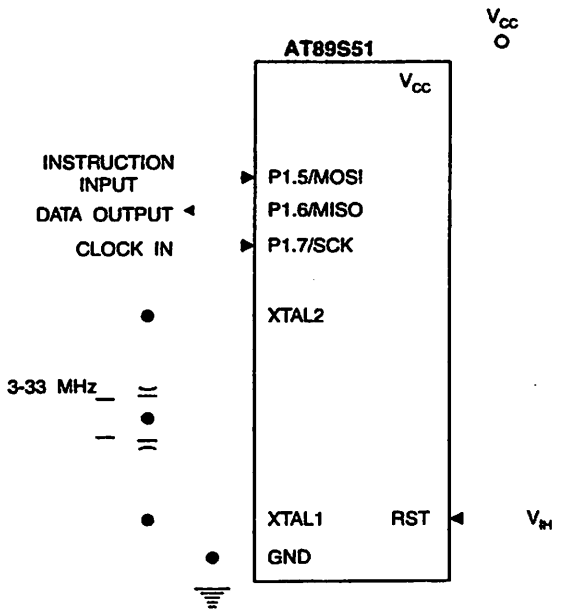
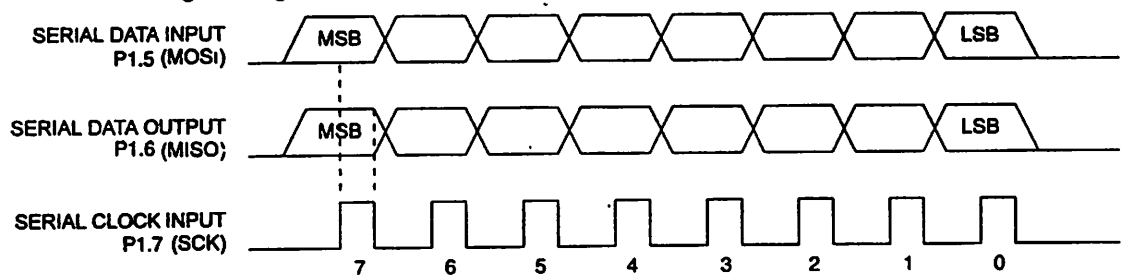


Figure 18-2. Flash Memory Serial Downloading



19. Flash Programming and Verification Waveforms – Serial Mode

Figure 19-1. Serial Programming Waveforms



20. Serial Programming Instruction Set

Instruction	Instruction Format				Operation
	Byte 1	Byte 2	Byte 3	Byte 4	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Write Lock Bits[1]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Read Signature Bytes	0010 1000	xxxx A11 A10 A9 A8	A7 xxx xxx0	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Note: 1. B1 = 0, B2 = 0 → Mode 1, no lock protection
B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
B1 = 1, B2 = 1 → Mode 4, lock bit 3 activated

} Each of the lock bit modes need to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

21. Serial Programming Characteristics

Figure 21-1. Serial Programming Timing

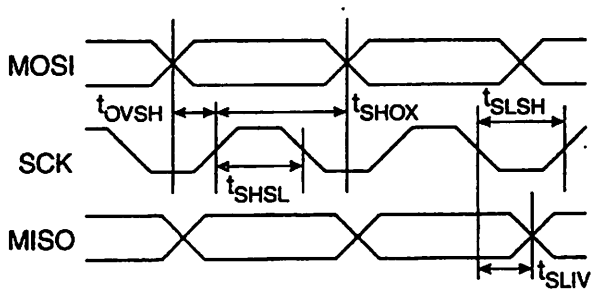


Table 21-1. Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	3		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	8 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	8 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

22. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

23. DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-300	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power-down is 2V.

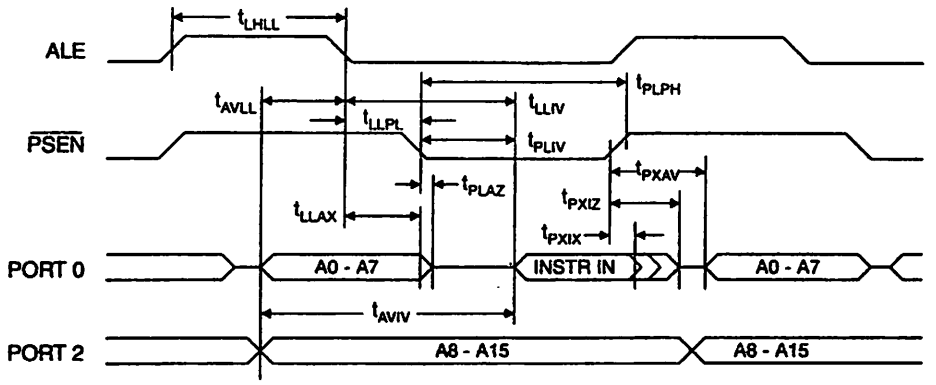
24. AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

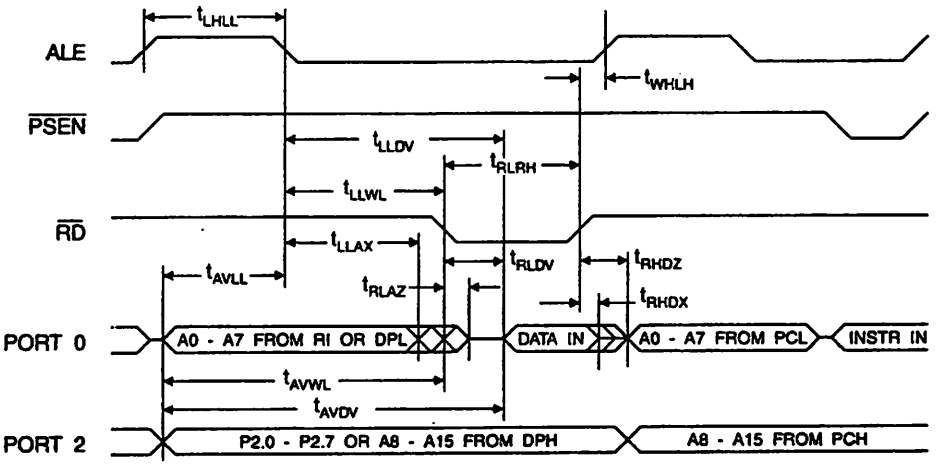
24.1 External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2\,t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-25		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-25		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4\,t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3\,t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3\,t_{CLCL}$-60	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5\,t_{CLCL}$-80	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6\,t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6\,t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5\,t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2\,t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8\,t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9\,t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3\,t_{CLCL}$-50	$3\,t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4\,t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7\,t_{CLCL}$-130		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

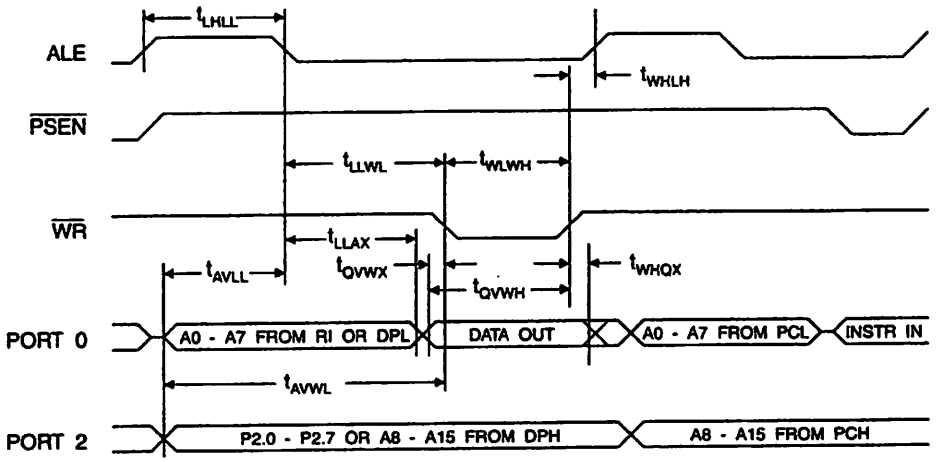
25. External Program Memory Read Cycle



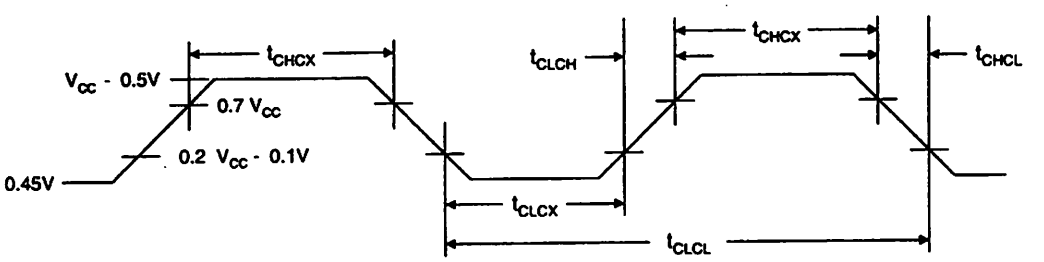
26. External Data Memory Read Cycle



27. External Data Memory Write Cycle



28. External Clock Drive Waveforms



29. External Clock Drive

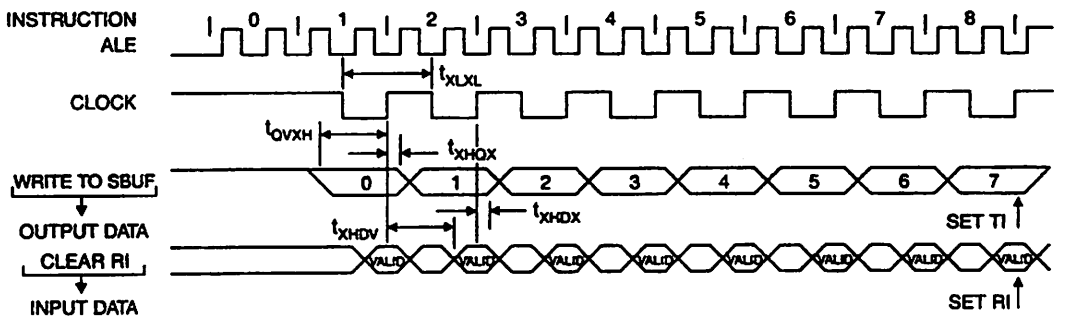
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	33	MHz
t_{CLCL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

30. Serial Port Timing: Shift Register Mode Test Conditions

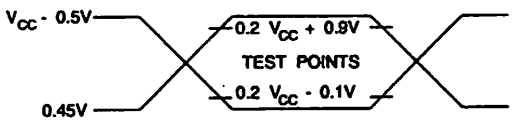
The values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		12 t_{CLCL}		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		10 t_{CLCL}-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		2 t_{CLCL}-80		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		10 t_{CLCL}-133	ns

31. Shift Register Mode Timing Waveforms

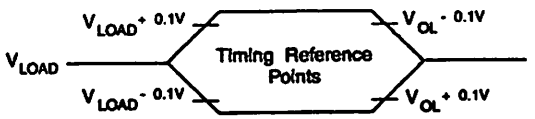


32. AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

33. Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

34. Ordering Information

34.1 Standard Package

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC AT89S51-24SC	44A 44J 40P6 42PS6	Commercial (0°C to 70°C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI AT89S51-24SI	44A 44J 40P6 42PS6	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC AT89S51-33SC	44A 44J 40P6 42PS6	Commercial (0°C to 70°C)

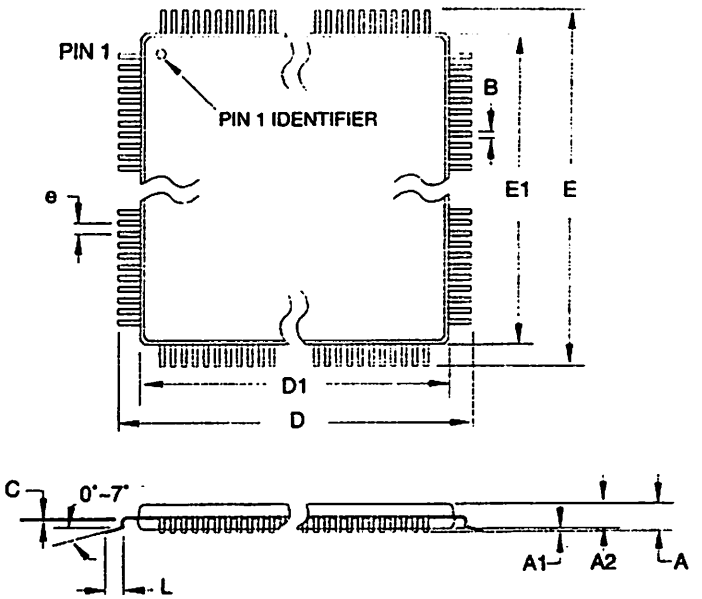
34.2 Green Package Option (Pb/Halide-free)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AU AT89S51-24JU AT89S51-24PU	44A 44J 40P6	Industrial (-40°C to 85°C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
42PS6	42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

35. Packaging Information

35.1 44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

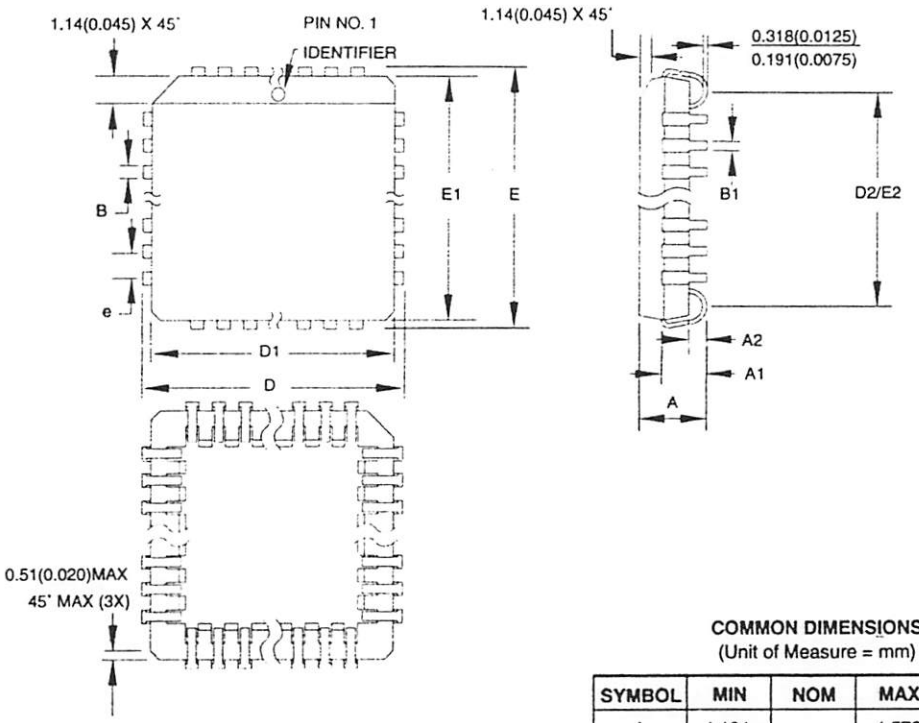
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	44A, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

35.2 44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

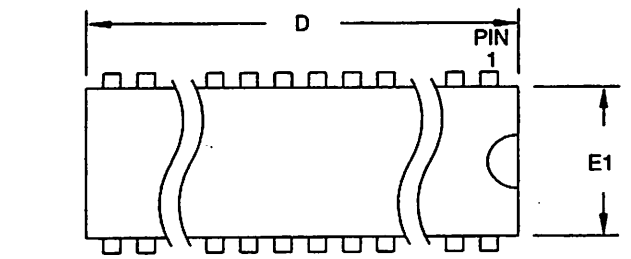
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

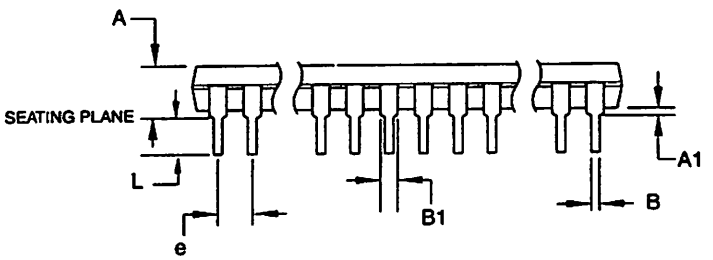
Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

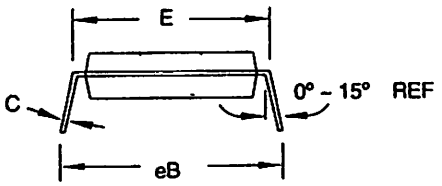
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

35.3 40P6 – PDIP







COMMON DIMENSIONS
(Unit of Measure = mm)

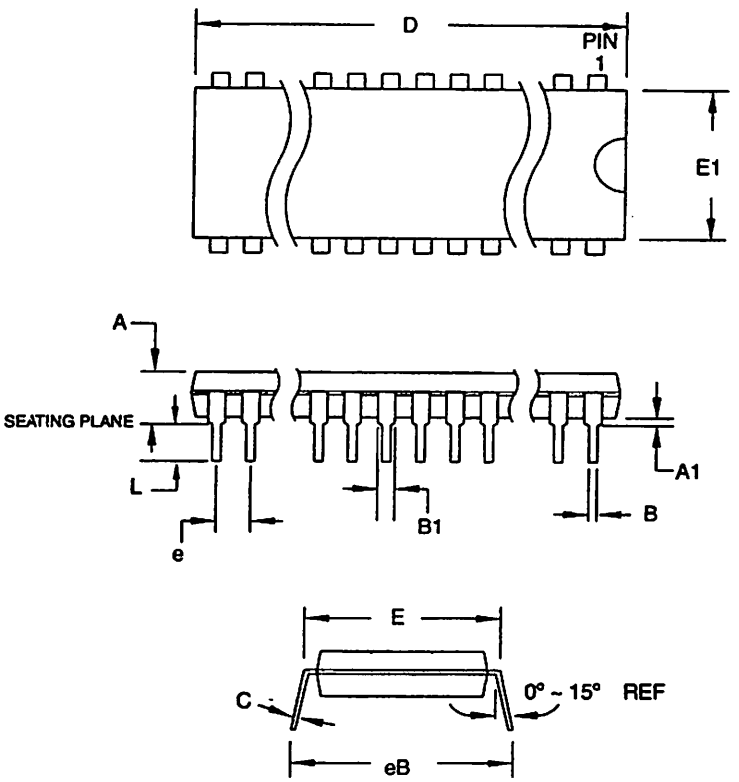
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	40P6, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

35.4 42PS6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.83	
A1	0.51	–	–	
D	36.70	–	36.96	Note 2
E	15.24	–	15.88	
E1	13.46	–	13.97	Note 2
B	0.38	–	0.56	
B1	0.76	–	1.27	
L	3.05	–	3.43	
C	0.20	–	0.30	
eB	–	–	18.55	
e	1.78 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/6/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	42PS6, 42-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	42PS6	A

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2487C–MICRO–03/05 /xM

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.
The data flash ROM (2 KB X 2 blocks) is embedded.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Outline

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Shortest instruction execution time	50 ns (f(XIN) = 20 MHz, Vcc = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, Vcc = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2.
Peripheral function	Interrupt	Internal: 11 factors, External: 5 factors, Software: 4 factors, Priority level: 7 levels
	Watchdog timer	15 bits x 1 (with prescaler) Reset start function selectable
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel Circuits of input capture and output compare.
	Serial interface	•1 channel Clock synchronous, UART •1 channel UART
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •On-chip oscillator (high-speed, low-speed) On high-speed on-chip oscillator the frequency adjustment function is usable.
	Oscillation stop detection function	Stop detection of main clock oscillation
	Voltage detection circuit	Included
	Power on reset circuit	Included
	Port	Input/Output: 22 (including LED drive port), Input: 2 (LED drive I/O port: 8)
Electrical characteristics	Power supply voltage	Vcc = 3.0 to 5.5V (f(XIN) = 20MHz) Vcc = 2.7 to 5.5V (f(XIN) = 10MHz)
	Power consumption	Typ.9 mA (Vcc = 5.0V, (f(XIN) = 20MHz,High-speed mode) Typ.5 mA (Vcc = 3.0V, (f(XIN) = 10MHz,High-speed mode) Typ.35 µA (Vcc = 3.0V, Wait mode, Peripheral clock stops) Typ.0.7 µA (Vcc = 3.0V, Stop mode)
Flash memory	Program/erase voltage	Vcc = 2.7 to 5.5 V
	Number of program/erase	10,000 times (Data area)
		1,000 times (Program area)
Operating ambient temperature		-20 to 85°C -40 to 85°C (D-version)
Package		32-pin plastic mold LQFP

1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

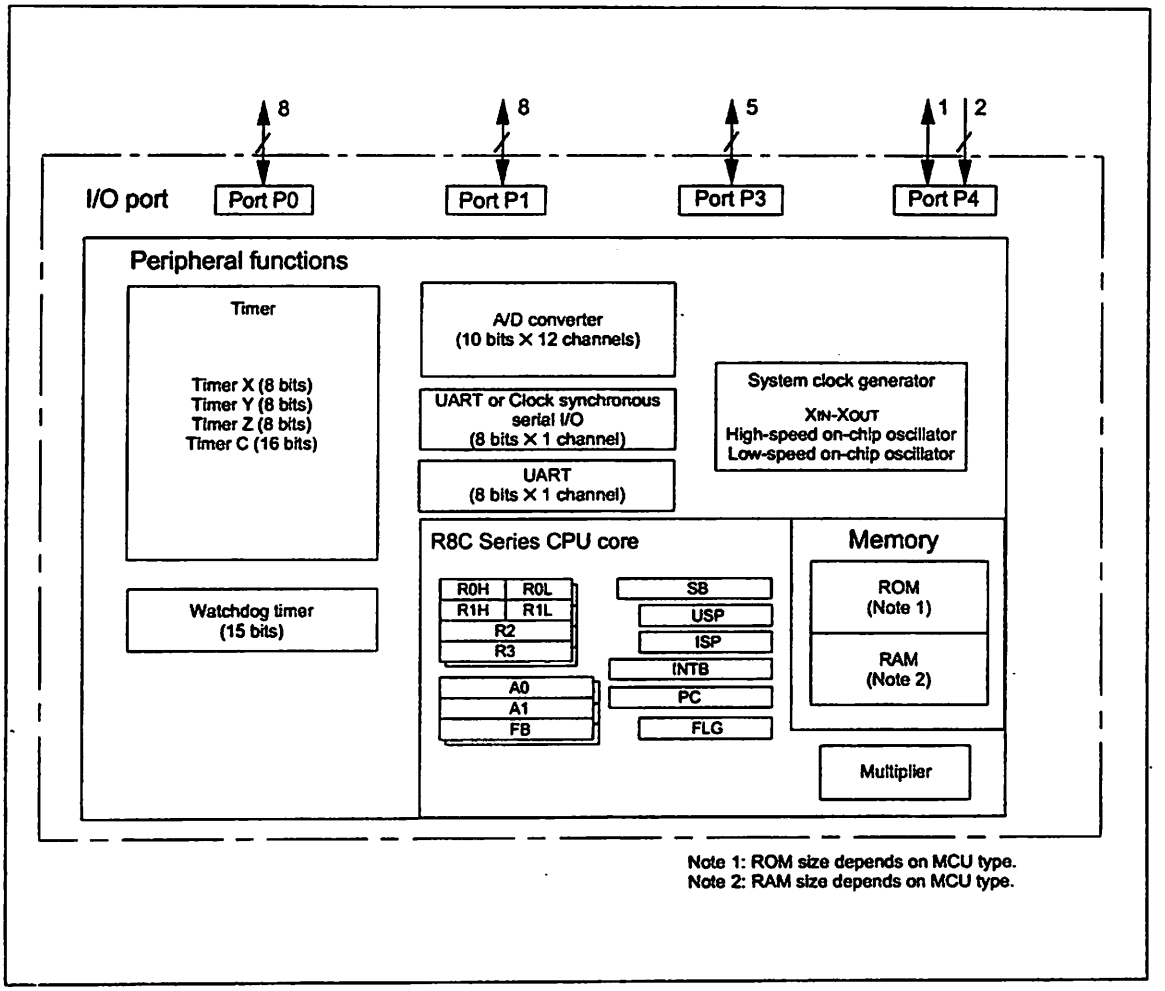


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.2 lists the products.

Table 1.2 Product List

As of April 2005

Type No.	ROM capacity		RAM capacity	Package type	Remarks
	Program area	Data area			
R5F21132FP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	Flash memory version
R5F21133FP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134FP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	
R5F21132DFP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	D version
R5F21133DFP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21134DFP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	

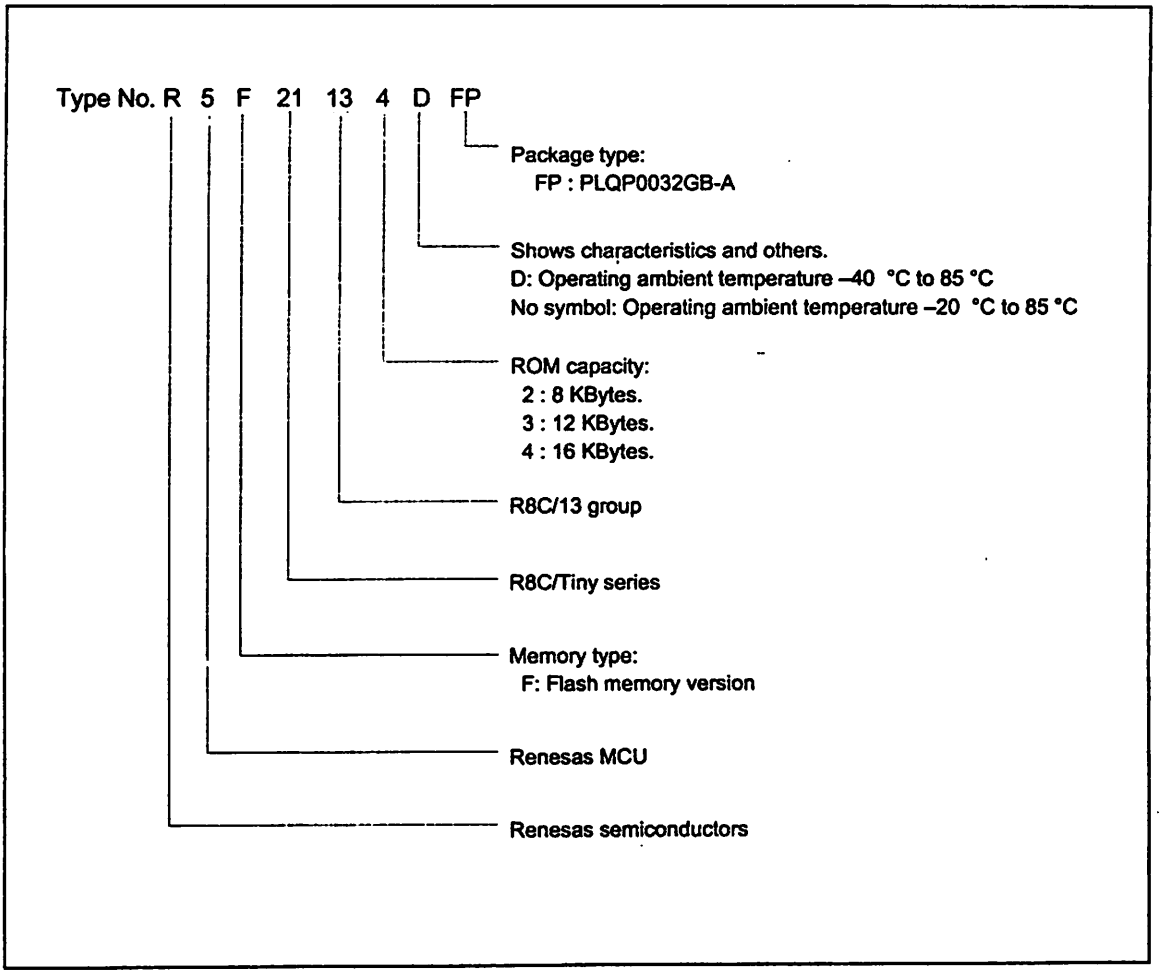


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Assignments

Figure 1.3 shows the pin configuration (top view).

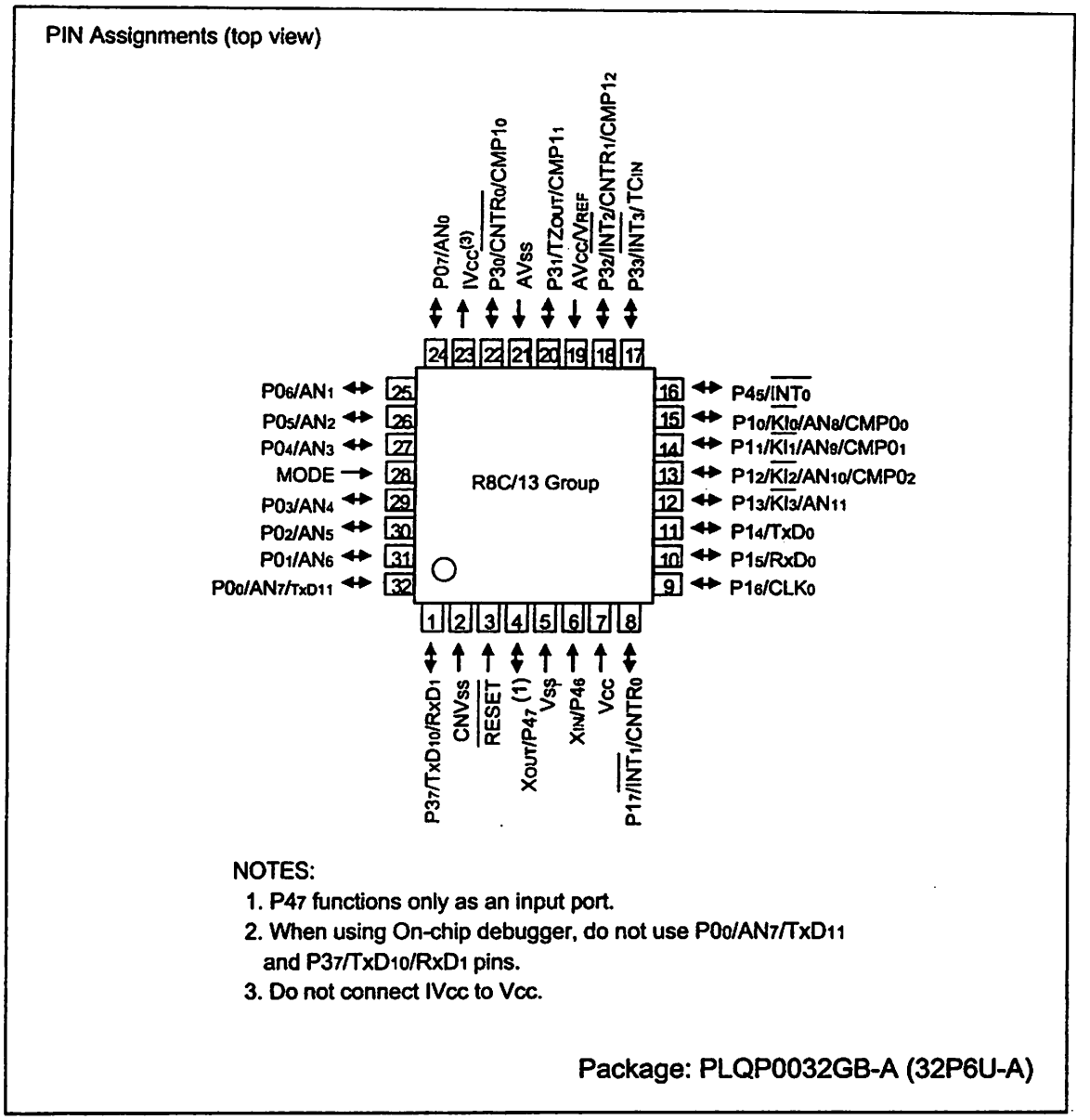


Figure 1.3 Pin Assignments (Top View)

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply Connect this pin to Vss via a capacitor (0.1 µF) Do not connect to Vcc
Analog power supply input	AVcc, AVss	I	These are power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	$\overline{\text{RESET}}$	I	"L" on this input resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor(1)
MODE	MODE	I	Connect this pin to Vcc via a resistor
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	These are $\overline{\text{INT}}$ interrupt input pins.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	These are key input interrupt pins.
Timer X	CNTR0	I/O	This is the timer X I/O pin.
	$\overline{\text{CNTR0}}$	O	This is the timer X output pin.
Timer Y	CNTR1	I/O	This is the timer Y I/O pin.
Timer Z	TZOUT	O	This is the timer Z output pin.
Timer C	TCIN	I	This is the timer C input pin.
	CMP00 to CMP03, CMP10 to CMP13	O	These are the timer C output pins.
Serial interface	CLK0	I/O	This is a transfer clock I/O pin.
	RxD0, RxD1	I	These are serial data input pins.
	TxD0, TxD10, TxD11	O	These are serial data output pins.
Reference voltage input	VREF	I	This is a reference voltage input pin for A/D converter. Connect the VREF pin to Vcc.
A/D converter	AN0 to AN11	I	These are analog input pins for A/D converter.
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	I/O	These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	I	These are input only pins.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

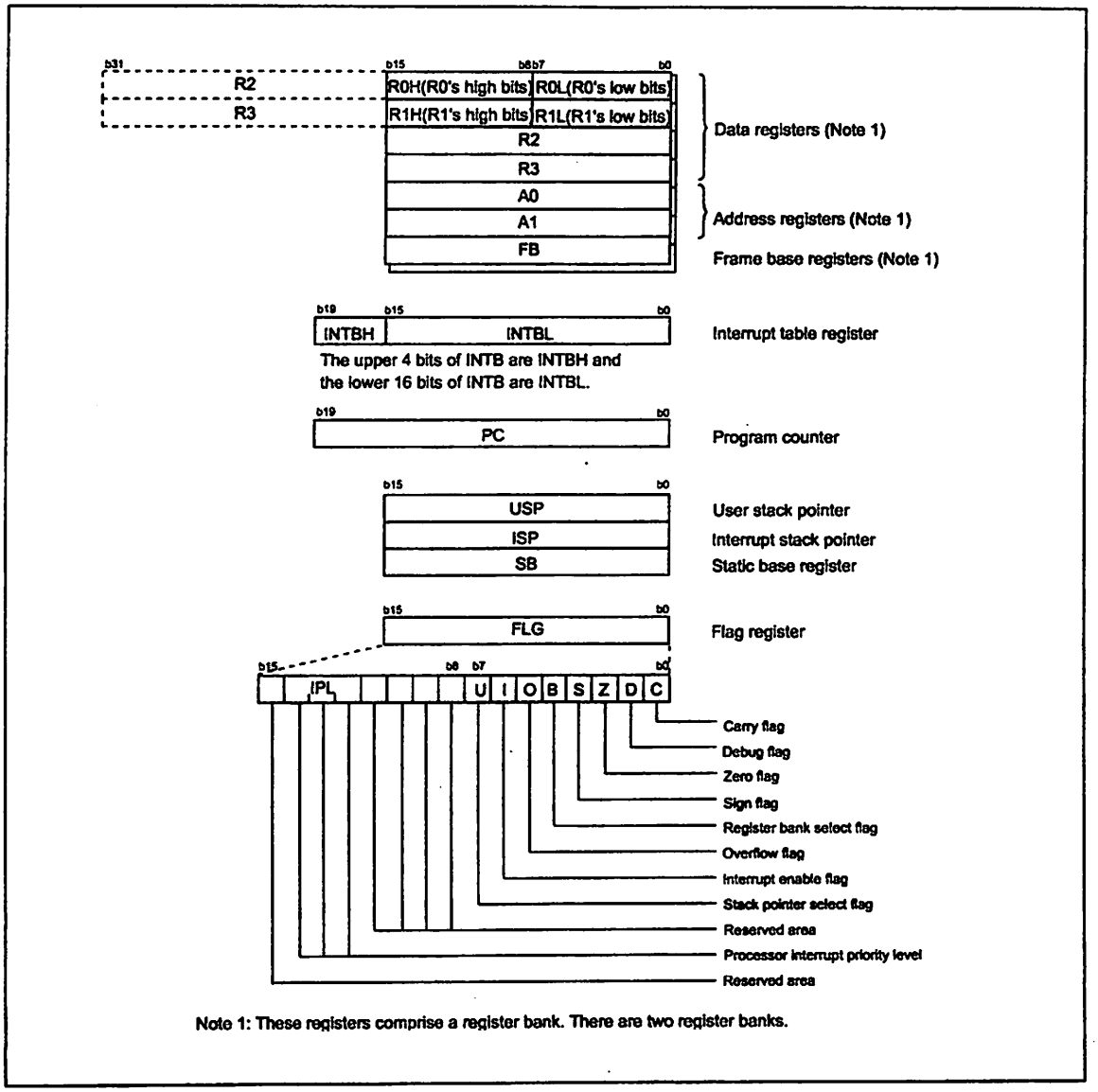


Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0" ; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of this MCU. The address space extends the 1M bytes from address 0000016 to FFFFF16.

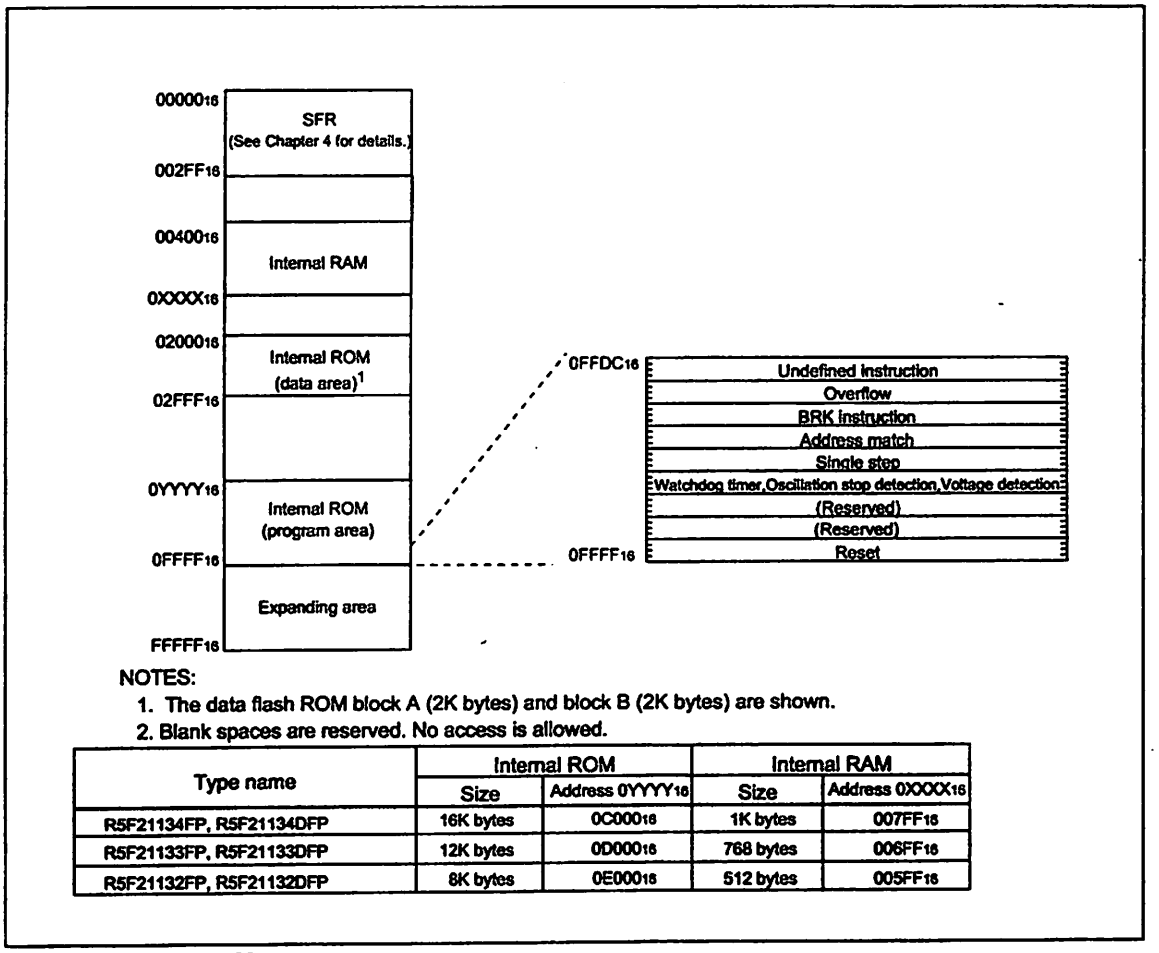
The internal ROM (program area) is allocated in a lower address direction beginning with address 0FFFF16. For example, a 16-Kbyte internal ROM is allocated to the addresses from 0C00016 to 0FFFF16.

The fixed interrupt vector table is allocated to the addresses from 0FFDC16 to 0FFFF16. Therefore, store the start address of each interrupt routine here.

The internal ROM (data area) is allocated to the addresses from 0200016 to 02FFF16.

The internal RAM is allocated in an upper address direction beginning with address 0040016. For example, a 1-Kbyte internal RAM is allocated to the addresses from 0040016 to 007FF16. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

Special function registers (SFR) are allocated to the addresses from 0000016 to 002FF16. Peripheral function control registers are located here. Of the SFR, any space which has no functions allocated is reserved for future use and cannot be used by users.



NOTES:
1. The data flash ROM block A (2K bytes) and block B (2K bytes) are shown.
2. Blank spaces are reserved. No access is allowed.

Type name	Internal ROM		Internal RAM	
	Size	Address 0YYYY16	Size	Address 0XXXX16
R5F21134FP, R5F21134DFP	16K bytes	0C00016	1K bytes	007FF16
R5F21133FP, R5F21133DFP	12K bytes	0D00016	768 bytes	006FF16
R5F21132FP, R5F21132DFP	8K bytes	0E00016	512 bytes	005FF16

Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)[1]

Address	Register	Symbol	After reset
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor mode register 0 [1]	PM0	0016
0005₁₆	Processor mode register 1	PM1	0016
0006₁₆	System clock control register 0	CM0	011010002
0007₁₆	System clock control register 1	CM1	001000002
0008₁₆	High-speed on-chip oscillator control register 0	HR0	0016
0009₁₆	Address match interrupt enable register	AIER	XXXXXX002
000A₁₆	Protect register	PRCR	00XXX0002
000B₁₆	High-speed on-chip oscillator control register 1	HR1	4016
000C₁₆	Oscillation stop detection register	OCD	000001002
000D₁₆	Watchdog timer reset register	WDTR	XX16
000E₁₆	Watchdog timer start register	WDTS	XX16
000F₁₆	Watchdog timer control register	WDC	000111112
0010₁₆	Address match interrupt register 0	RMAD0	0016
0011₁₆			0016
0012₁₆			X016
0013₁₆			
0014₁₆	Address match interrupt register 1	RMAD1	0016
0015₁₆			0016
0016₁₆			X016
0017₁₆			
0018₁₆			
0019₁₆	Voltage detection register 1 [2]	VCR1	000010002
001A₁₆	Voltage detection register 2 [2]	VCR2	0016 [3] 100000002 [4]
001B₁₆			
001C₁₆			
001D₁₆			
001E₁₆	INT0 input filter select register	INT0F	XXXXX0002
001F₁₆	Voltage detection interrupt register [2]	D4INT	0016 [3] 010000012 [4]
0020₁₆			
0021₁₆			
0022₁₆			
0023₁₆			
0024₁₆			
0025₁₆			
0026₁₆			
0027₁₆			
0028₁₆			
0029₁₆			
002A₁₆			
002B₁₆			
002C₁₆			
002D₁₆			
002E₁₆			
002F₁₆			
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆			
0039₁₆			
003A₁₆			
003B₁₆			
003C₁₆			
003D₁₆			
003E₁₆			
003F₁₆			

X : Undefined
NOTES:
1. Blank columns are all reserved space. No access is allowed.
2. Software reset or the watchdog timer reset does not affect this register.
3. Owing to Reset input.
4. In the case of RESET pin = H retaining.

REVISION HISTORY	R8C/13 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Oct 28, 2003		First edition issued
0.20	Dec05, 2003	5	Figure 1.3 revised
		10	Chapter 4, NOTES revised
		16	Table 5.4 revised Table 5.5 revised
		17	Table 5.6 revised Figure 5.3 added
		18	Table 5.8 revised Table 5.10 revised
		21	Figure 5.3 revised to Figure 5.4
		22	Table 5.17 revised
		25	Figure 5.4 revised to Figure 5.5
1.00	Sep 30, 2004	All pages	Words standardized (on-chip oscillator, serial interface, A/D)
		2	Table 1.1 revised
		5	Figure 1.3, NOTES 3 added
		6	Table 1.3 revised
		9	Figure 3.1, NOTES added
		10-13	One body sentence in chapter 4 added ; Titles of Table 4.1 to 4.4 added
		12	Table 4.3 revised ; Table 4.4 revised
		14	Table 5.2 revised
		15	Table 5.3 revised
		16	Table 5.4 and Table 5.5 revised
		17	Table 5.6, 5.7 and 5.8 revised ; Figure 5.3 revised
		18	Table 5.9 and 5.11 revised
		19	Table 5.12 revised
		20	Table 5.13 revised
		22	Table 5.18 revised
		23	Table 5.19 revised
		24	Table 5.20 and Table 5.24 revised
1.10	Apr.27.2005	4	Table 1.2, Figure 1.2 package name revised
		5	Figure 1.3 package name revised
		10	Table 4.1 revised
		12	Table 4.3 revised
		15	Table 5.3 partly revised
		16	Table 5.4, Table 5.5 partly added

Rev.	Date	Description	
		Page	Summary
1.10	Apr.27.2005	17	Table 5.7, 5.8 revised
		18	Table 5.10, Table 5.11 partly revised
		22	Table 5.18 partly revised
		26	Package Dimensions revised

AN.No.1632-711E

LIQUID CRYSTAL DISPLAY MODULE

M 1 6 3 2

USER MANUAL

Seiko Instruments Inc.

PREFACE

This manual describes technical informations on functions and instructions of M1632 from Seiko Instruments Inc. Please read this instruction manual carefully to understand all the module functions and make the best use of them. Description details may be changed without notice.

Revision Record

Edition	Revision	Date
1	Original	April 1985
2	Completely revised	Jan. 1987

CONTENTS

1. GENERAL

1.1 General

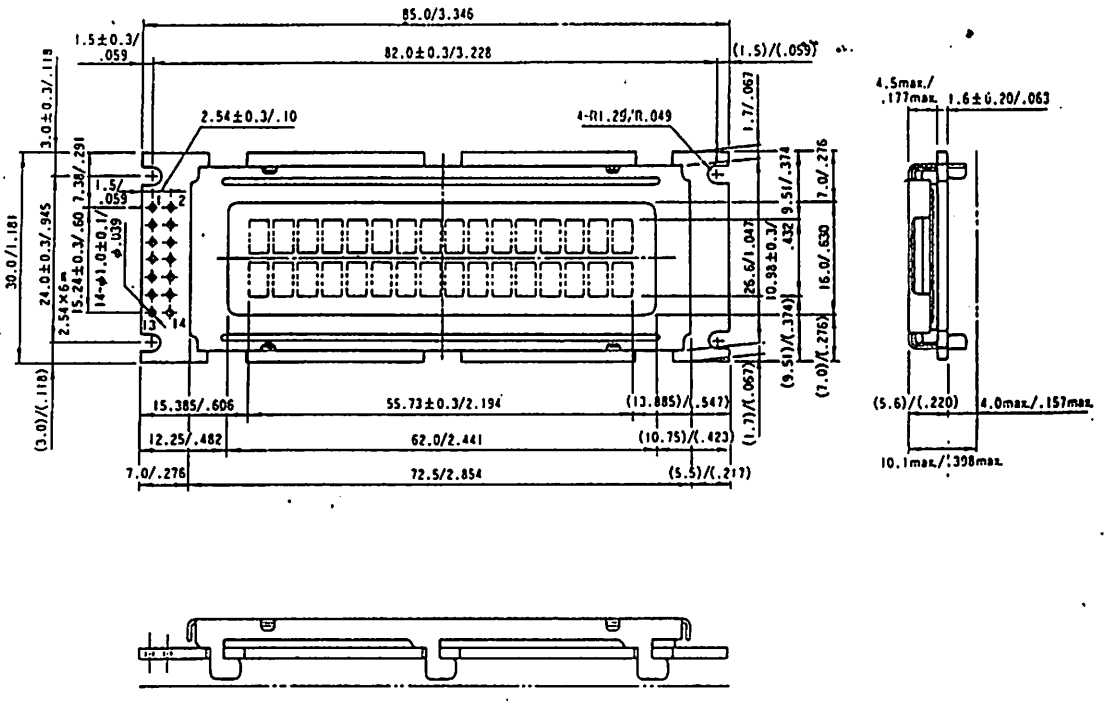
The M1632 is a low-power-consumption dot-matrix liquid crystal display (LCD) module with a high-contrast wide-view TN LCD panel and a CMOS LCD drive controller built in. The controller has a built-in character generator ROM/RAM, and display data RAM. All the display functions are controlled by instructions and the module can easily be interfaced with an MPU. This makes the module applicable to a wide range of purposes including terminal display units for microcomputers and display units for measuring gages.

1.2 Features

- 16-character, two-line TN liquid crystal display of 5 x 7 dot matrix + cursor
- Duty ratio: 1/16
- Character generator ROM for 192 character types
  (character font: 5 x 7 dot matrix)
- Character generator RAM for eight character types (program write)
  (character font: 5 x 7 dot matrix)
- 80 x 8 bit display data RAM (80 characters maximum)
- Interface with four-bit and eight-bit MPUs possible
- Display data RAM and character generator RAM readable from MPU
- Many instruction functions

  Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, and Display Shift
- Built-in oscillator circuit
- +5 V single power supply
- Built-in automatic reset circuit at power-on
- CMOS process
- Operating temperature range: 0°C to 50°C

1.3 Dimensions Diagram



Unit : mm/inch
General tolerance : ±0.5 mm

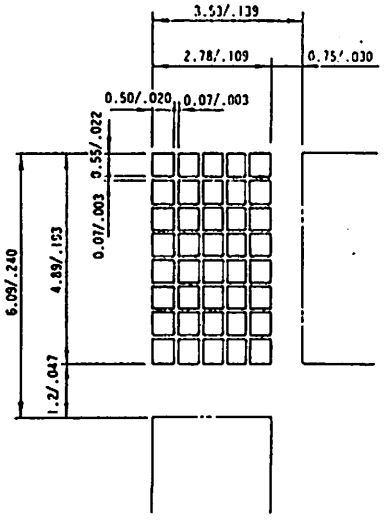
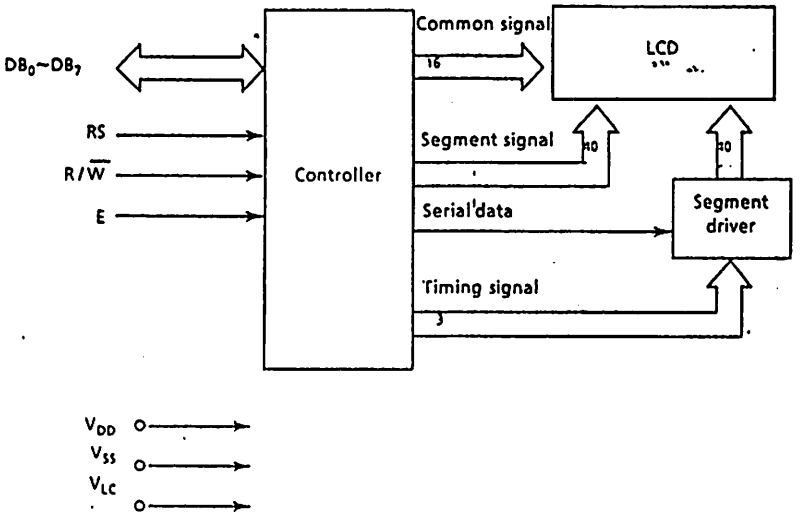


Figure 1 Dimensions diagram

I/O terminal symbol

No.	Symbol	Level	Function	
1	Vss	-	Power Supply	0V (GND)
2	Vcc	-		5V ±10%
3	Vee	-		for LCD Drive
4	RS	H/L	H: Data Input L: Instruction Input	
5	R/W	H/L	H:READ L:WRITE	
6	E	H,↴	Enable Signal	
7	DB0	H/L	Data Bus	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+ BL	-	Back Light Supply	4 - 4.2V 50-200mA
16	V- BL	-		0V (GND)

1.4 Block Diagram



1.5 Absolute Maximum Ratings

V_{SS} = 0 V

Item	Symbol	Standard	Unit	Remarks
Power supply voltage	V_{DD}	− 0.3 to + 7.0	V	
	V_{LC}	V_{DD} − 13.5 to V_{DD} + 0.3	V	
Input voltage	V_{in}	− 0.3 to V_{DD} + 0.3,	V	
Operating temperature	T_{opr}	0 to + 50	°C	
Storage temperature	T_{stg}	− 20 to + 60	°C	At 50% RH

1.6 Electrical Characteristics

V_{DD} = 5 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Conditions	Standard			Unit
				Min.	Typ.	Max.	
Input voltage	High	V_{IH1}		2.2	−	V_{DD}	V
	Low	V_{IL1}		0	−	0.6	V
Output voltage (TTL)	High	V_{OH1}	$-I_{OH}$ = 0.205 mA	2.4	−	−	V
	Low	V_{OL1}	I_{OL} = 1.2 mA	−	−	0.4	V
Output voltage (CMOS)	High	V_{OH2}	$-I_{OH}$ = 0.04 mA	0.9V_{DD}	−	−	V
	Low	V_{OL2}	I_{OL} = 0.04 mA	−	−	0.1V_{DD}	V
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		V_{LC}	V_{DD} = 5 V, T_A = 25°C	−	0.25	−	V
Current consumption		I_{DD}		−	2.0	3.0	mA
		I_{LC}	V_{LC} = 0.25V	−	−	1.0	mA
Clock oscillation freq.		f_{osc}	Resistance oscillation	190	270	350	kHz

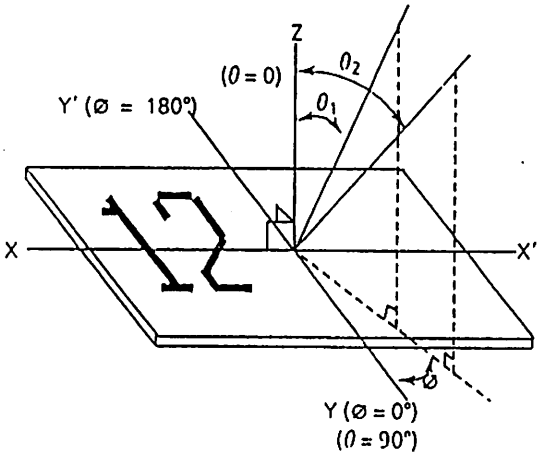
1.7 Optical Characteristics

1.7.1 Optical characteristics

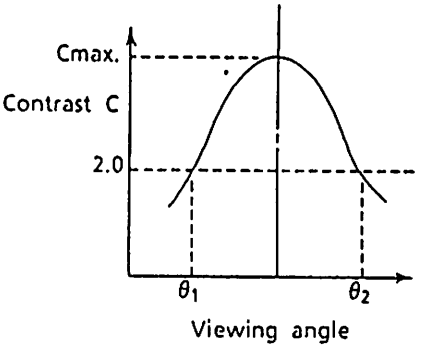
Maximum viewing angle: 6 o'clock ($\varnothing$ = 0°)
T_A = 25°C, V_{opr} = 4.75 V

Item	Symbol	Conditions	Min.	Typ.	Max.	Remarks
Viewing angle	$\theta_2 - \theta_1$	$C \geq 2.0$, $\varnothing$ = 0°	35	–	–	See Notes 1 and 2.
Contrast	C	θ = 25° , $\varnothing$ = 0°	5	8	–	See Note 3.
Rise time	t_{on}	θ = 25° , $\varnothing$ = 0°	–	60 ms	70 ms	See Note 4.
Fall time	t_{off}	θ = 25° , $\varnothing$ = 0°	–	150 ms	170 ms	See Note 4.

Note 1: Definition of angles ø and θ

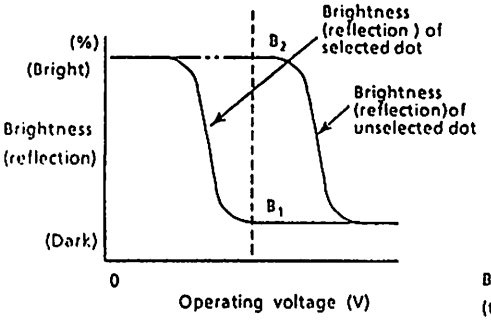


Note 2: Definition of viewing angles θ_1 and θ_2

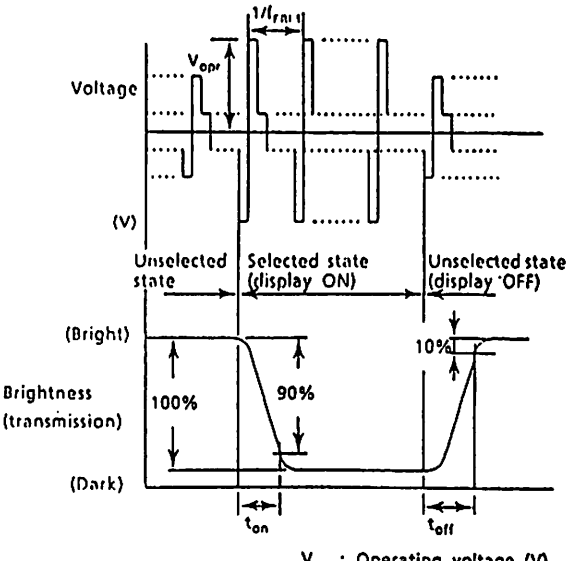


Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



V_{opr} : Operating voltage (V)
f_{FRM} : Frame frequency (Hz)
t_{on} : Response time (rise)(ms)
t_{off} : Response time (fall)(ms)

1.7.2 Recommended operating voltage

The viewing angle and screen contrast of the LCD panel can be varied by changing the liquid crystal operating voltage (V_{opr}), that is V_{LC}.

The optical characteristics is influenced by an ambient temperature. The recommended value of V_{opr} for an ambient temperatures are shown below.

Temperature (℃)	0	10	25	40	50
Voltage V_{opr} (V)	5.00	4.90	4.75	4.60	4.50

$V_{opr} = V_{DD} - V_{LC}$

2. OPERATING INSTRUCTIONS

2.1 Terminal Functions

Table 1 Terminal functions

Signal name	No. of terminals	I/O	Destination	Function
DB_0 to DB_3	4	I/O	MPU	Tristate bidirectional lower four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. If the interface data is 4 bits, the signals are not used.
DB_4 to DB_7	4	I/O	MPU	Tristate bidirectional upper four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. DB_7 is also used as a busy flag.
E	1	Input	MPU	Operation start signal: The signal activates data write or read.
$R/\overline{W}$	1	Input	MPU	Read (R) and Write ($\overline{W}$) selection signals 0 : Write 1 : Read
RS	1	Input	MPU	Register selection signals 0 : Instruction register (Write) Busy flag and address counter (Read) 1 : Data register (Write and Read)
V_{LC}	1	–	Power supply	Power supply terminal for driving liquid crystal display: The screen contrast can be varied by changing V_{LC}.
V_{DD}	1	–	Power supply	+5 V
V_{SS}	1	–	Power supply	Ground terminal: 0 V

2.2 Basic Operations

2.2.1 Registers

The controller has two kinds of eight-bit registers: the instruction register (IR) and the data register (DR). They are selected by the register select (RS) signal as shown in Table 2.

The IR stores instruction codes such as Display Clear and Cursor Shift, and the address information of display data RAM (DD RAM) and character generator RAM (CG RAM). They can be written from the MPU, but cannot be read to the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM, or read from DD RAM or CG RAM. When data is written into DD RAM or CG RAM from the MPU, the data in the DR is automatically written into DD RAM or CG RAM by internal operation. However, when data is read from DD RAM or CG RAM, the necessary data address is written into the IR. The specified data is read out to the DR and then the MPU reads it from the DR. After the read operation, the next address is set and DD RAM or CG RAM data at the address is read into the DR for the next read operation.

Table 2 Register selection

RS	R/$\overline{W}$	Operation
0	0	IR selection, IR write. Internal operation : Display clear
0	1	Busy flag (DB_7) and address counter (DB_0 to DB_6) read
1	0	DR selection, DR write. Internal operation : DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation : DD RAM or CG RAM to DR

2.2.2 Busy flag (BF)

The flag indicates whether the module is ready to accept the next instruction. As shown in Table 2, the signal is output to DB_7 if RS = 0 and R/$\overline{W}$ = 1. If the value is 1, the module is working internally and the instruction cannot be accepted. If the value is 0, the next instruction can be written. Therefore, the flag status needs to be checked before executing an instruction. If an instruction is executed without checking the flag status, wait for more than the execution time shown by 2.4 Instruction Outline.

2.2.3 Address counter (AC)

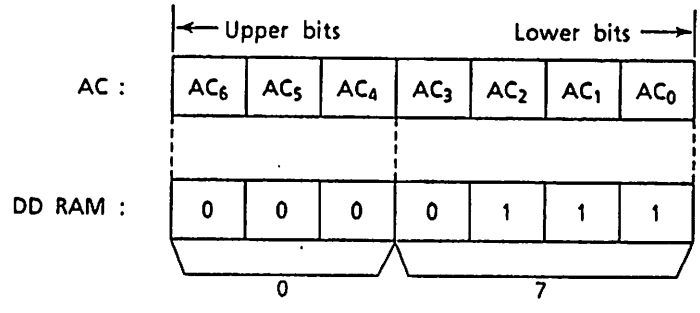
The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB_0 to DB_6 as shown in Table 2 if RS = 0 and $R/\overline{W} = 1$.

2.2.4 Display data RAM (DD RAM)

DD RAM has a capacity of up to 80 × 8 bits and stores display data of 80 eight-bit character codes. Some storage areas of DD RAM which are not used for display can be used as general data RAM.

A DD RAM address to be set in the AC is expressed in hexadecimal form as follows.

Example: DD RAM address = 07



00_H to $0F_H$ of the DD RAM address is set in the line 1, and 40_H to $4F_H$ in the line 2.

Note : The addresses in the digit 16 of line 1 and the digit 1 of line 2 are not consecutive.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM address
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

If the display is shifted, DD RAM address 00_H to 27_H are displayed in line 1 and 40_H to 67_H in line 2. The following figures are examples of display shifts.

*Left shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	DD RAM address
Line 2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	

*Right shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	DD RAM address
Line 2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

2.2.5 Character generator ROM (CG ROM)

Character generator ROM generates 192 types of 5 x 7 dot-matrix character patterns from eight-bit character codes.

Table 3 shows the correspondence between the CG ROM character codes and character patterns.

2.2.6 Character generator RAM (CG RAM)

CG RAM is used to create character patterns freely by programming. Eight types of character patterns can be written.

Table 4 shows the character patterns created from CG RAM addresses and data. To display a created character pattern, the character code in the left column of the table is written into DD RAM corresponding to the display position (digit). The areas not used for display are available as general data RAM.

Table 3 Correspondence between character codes and character patterns

Upper bit 4 bit / Lower bit 4 bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
×××0000	CG RAM (1)												
×××0001	(2)												
×××0010	(3)												
×××0011	(4)												
×××0100	(5)												
×××0101	(6)												
×××0110	(7)												
×××0111	(8)												
×××1000	(1)												
×××1001	(2)												
×××1010	(3)												
×××1011	(4)												
×××1100	(5)												
×××1101	(6)												
×××1110	(7)												
×××1111	(8)												

Table 4 Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data)

Character code (DD RAM data) 7 6 5 4 3 2 1 0 ←Upper bit Lower bit→	CG RAM address 5 4 3 2 1 0 ←Upper bit Lower bit→	Character pattern (CG RAM data) 7 6 5 4 3 2 1 0 ←Upper bit Lower bit→
0 0 0 0 * 0 0 0	0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1
0 0 0 0 * 0 0 1	0 0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1
		0 0 0 0 0 1
0 0 0 0 * 1 1 1	1 1 1	1 0 0 1 0 1 1 1 0 1 1 1

Example of character pattern (R)

← Cursor position

Example of character pattern (¥)

Notes: • In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display.

• Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).

• CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is changed to 1, one bit lights, regardless of the cursor.

The character pattern column positions correspond to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.

When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00H and 08H select the same character.

2.3 Timing Characteristics

2.3.1 Write timing characteristics

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		t_{CYCE}	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er},t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$ → E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data setup time		t_{DSW}	195	–	ns
Data hold time		t_H	10	–	ns

Write operation

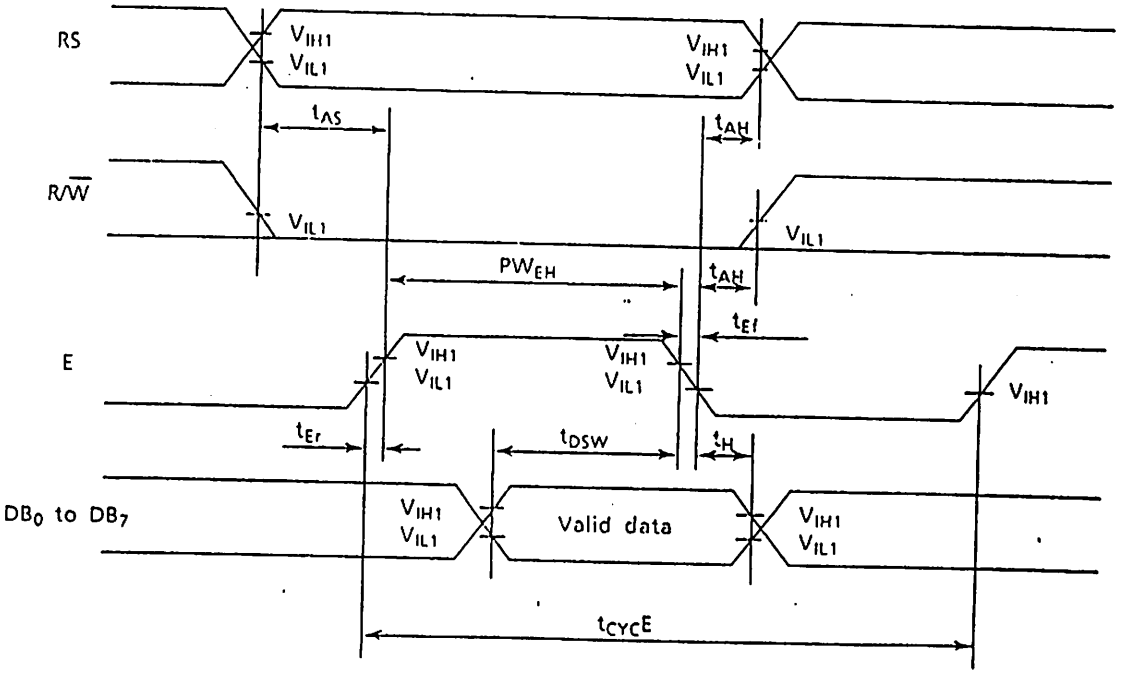


Figure 3 Data write from MPU to module

2.3.2 Read timing characteristics

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		$t_{CYC}E$	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er},t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$—E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data delay time		t_{DDR}	–	320	ns
Data hold time		t_H	20	–	ns

Read operation

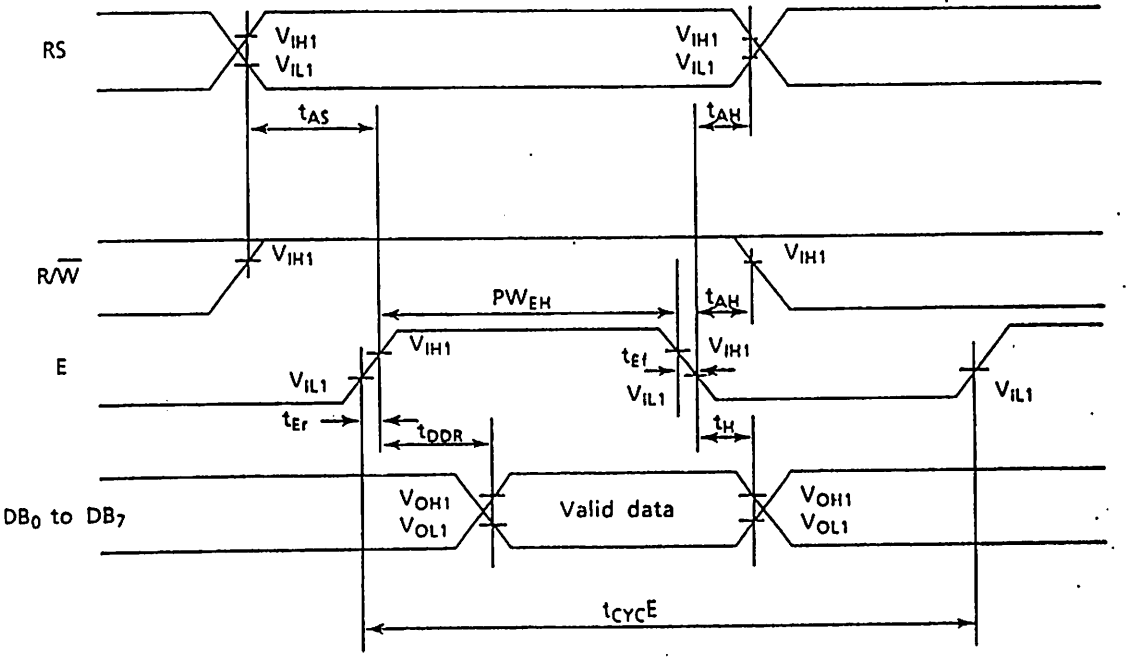


Figure 4 Data read from module to MPU

2.4 Instruction Outline

Table 5 List of instructions

Instruction	Code										Function	Execution time
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
(1) Display clear 4	0	0	0	0	0	0	0	0	0	1	Clears all display and returns cursor to home position (address 0)	1.64 ms
(2) Cursor Home	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change.	1.64 ms
(3) Entry Mode Set 3	0	0	0	0	0	0	0	1	I/D	S	Sets direction of cursor movement and whether display will be shifted when data is written or read	40 µs
(4) Display ON / OFF control 2	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)	40 µs
(5) Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents	40 µs
(6) Function Set 1	0	0	0	0	1	DL	1	*	*	*	Sets interface data length (DL)	40 µs
(7) CG RAM Address Set	0	0	0	1	A_{CG}						Sets CG RAM address to start transmitting or receiving CG RAM data	40 µs
(8) DD RAM Address Set	0	0	1	A_{DD}							Sets DD RAM address to start transmitting or receiving DD RAM data	40 µs
(9) BF/Address Read	0	1	BF	AC							Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM)	0 µs
(10) Data Write to CG RAM or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	40 µs
(11) Data Read from CG RAM or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM	40 µs

* : Invalid bit
A_{CG} : CG RAM address
A_{DD} : DD RAM address

I/D = 1 : Increment
I/D = 0 : Decrement

S = 1 : Display shift
S = 0 : No display shift

D = 1 : Display ON
D = 0 : Display OFF

C = 1 : Cursor ON
C = 0 : Cursor OFF

B = 1 : Blink ON
B = 0 : Blink OFF

S/C = 1 : Display shift
S/C = 0 : Cursor movement

R/L = 1 : Right shift
R/L = 0 : Left shift

DL = 1 : 8 bits
DL = 0 : 4 bits

BF = 1 : Internal operation in progress
BF = 0 : Instruction can be accepted

E = Enable clock.

2.5 Instruction Details

(1) Display Clear

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Display Clear clears all display and returns cursor to home position (address 0).

Space code 20 (hexadecimal) is written into all the addresses of DD RAM, and DD RAM address 0 is set to the AC. If shifted, the display returns to the original position. After execution of the Display Clear instruction, the entry mode is incremented.

Note : When executing the Display Clear instruction, follow the restrictions listed in Table 6.

(2) Cursor Home

	RS	R/$\overline{W}$	DB_7							DB_0	
Code	0	0	0	0	0	0	0	0	1	*	* : Invalid bit

Cursor Home returns cursor to home position (address 0).

DD RAM address 0 is set to the AC. The cursor returns to the home position. If shifted, the display returns to the original position. The DD RAM contents do not change. If the cursor or blinking is ON, it returns to the left side.

Note : When executing the Cursor Home instruction, follow the restrictions listed in Table 6.

Table 6 Restrictions on execution of Display Clear and Cursor Home instructions

Conditions of use	Restrictions
When executing the Display Clear or Cursor Home instruction when the display is shifted (after execution of Display Shift instruction)	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{osc}$* second after the first execution. Example: 1.5 ms, 3 ms, 4.5 ms for f_{osc} = 270 kHz *f_{osc}: Oscillation frequency
When 23_H, 27_H, 63_H, or 67_H is used as a DD RAM address to execute Cursor Home instruction	Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)

(3) Entry Mode Set

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry Mode Set sets the direction of cursor movement and whether display will be shifted.

I/D : The DD RAM address is incremented or decremented by one when a character code is written into or read from DD RAM. This is also true for writing into or reading from CG RAM.

When I/D = 1, the address is incremented by one and the cursor or blink moves to the right.

When I/D = 0, the address is decremented by one and the cursor or blink moves to the left.

S : If S = 1, the entire display is shifted either to the right or left for writing into DD RAM. The cursor position does not change, only the display moves. There is no display shift for reading from DD RAM.

When S = 1 and I/D = 1, the display shifts to the left.
When S = 1 and I/D = 0, the display shifts to the right.

If S = 0, the display does not shift.

(4) Display ON/OFF Control

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display ON/OFF Control turns the total display and the cursor ON and OFF, and makes the cursor position start blinking. Cursor ON/OFF and blinking is done at the column indicated by the specified DD RAM address by the AC.

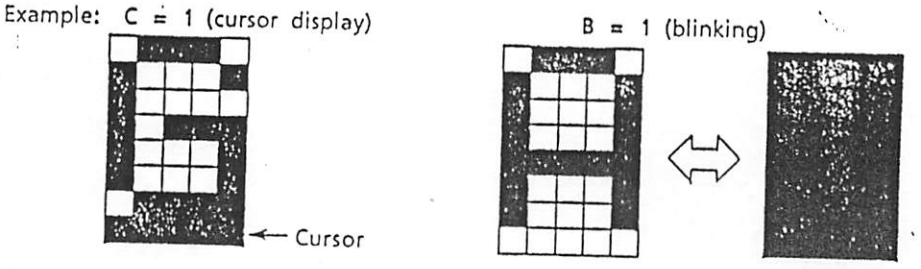
D : When D = 1, the display is turned ON.
When D = 0, the display is turned OFF.
If D = 0 is used, display data remains in DD RAM. Change 0 to 1 to display data.

C : When C = 1, the cursor is displayed.
When C = 0, the cursor is not displayed.

The cursor is displayed in the dot line below the 5 x 7 dot-matrix character fonts. If the cursor is OFF, display data is written into DD RAM in the order specified by I/D.

B : When B = 1, the character at the cursor position starts blinking.
When B = 0, it does not blink.

For blinking, all-black dots and the character are switched about every 0.4 seconds. The cursor and blinking can be set at the same time.



(5) Cursor/Display Shift

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* :Invalid bit

Cursor/Display Shift moves the cursor and shifts the display without changing the DD RAM contents.

The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. Since the DD RAM capacity is 40-character and two lines, the cursor is shifted from digit 40 of line 1 to digit 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. Therefore, the display pattern of line 2 is not shifted to line 1.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one).
0	1	The cursor position is shifted to the right (the AC increments one).
1	0	The entire display is shifted to the left with the cursor.
1	1	The entire display is shifted to the right with the cursor.

Note: If only display shift is done, the AC contents do not change.

(6) Function Set

	RS	R/$\overline{W}$	DB_7							DB_0	
Code	0	0	0	0	1	DL	1	*	*	*	* : Invalid bit

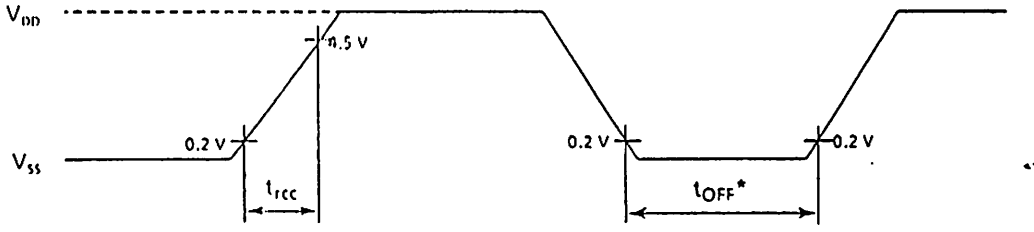
Function Set sets the interface data length.

DL : Interface data length
When DL = 1, the data length is set at eight bits (DB_7 to DB_0).
When DL = 0, the data length is set at four bits (DB_7 to DB_4).
The upper four bits are transferred first, then the lower four bits follow.

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

Remarks: Initialization

The system is automatically initialized at power-on if the following power supply conditions are satisfied.



0.1 ms ≦ t_{rcc} ≦ 10 ms $\qquad$ t_{OFF} ≧ 1 ms

*t_{OFF}: Time when power supply is OFF if cut instantaneously or turned ON and OFF repeatedly

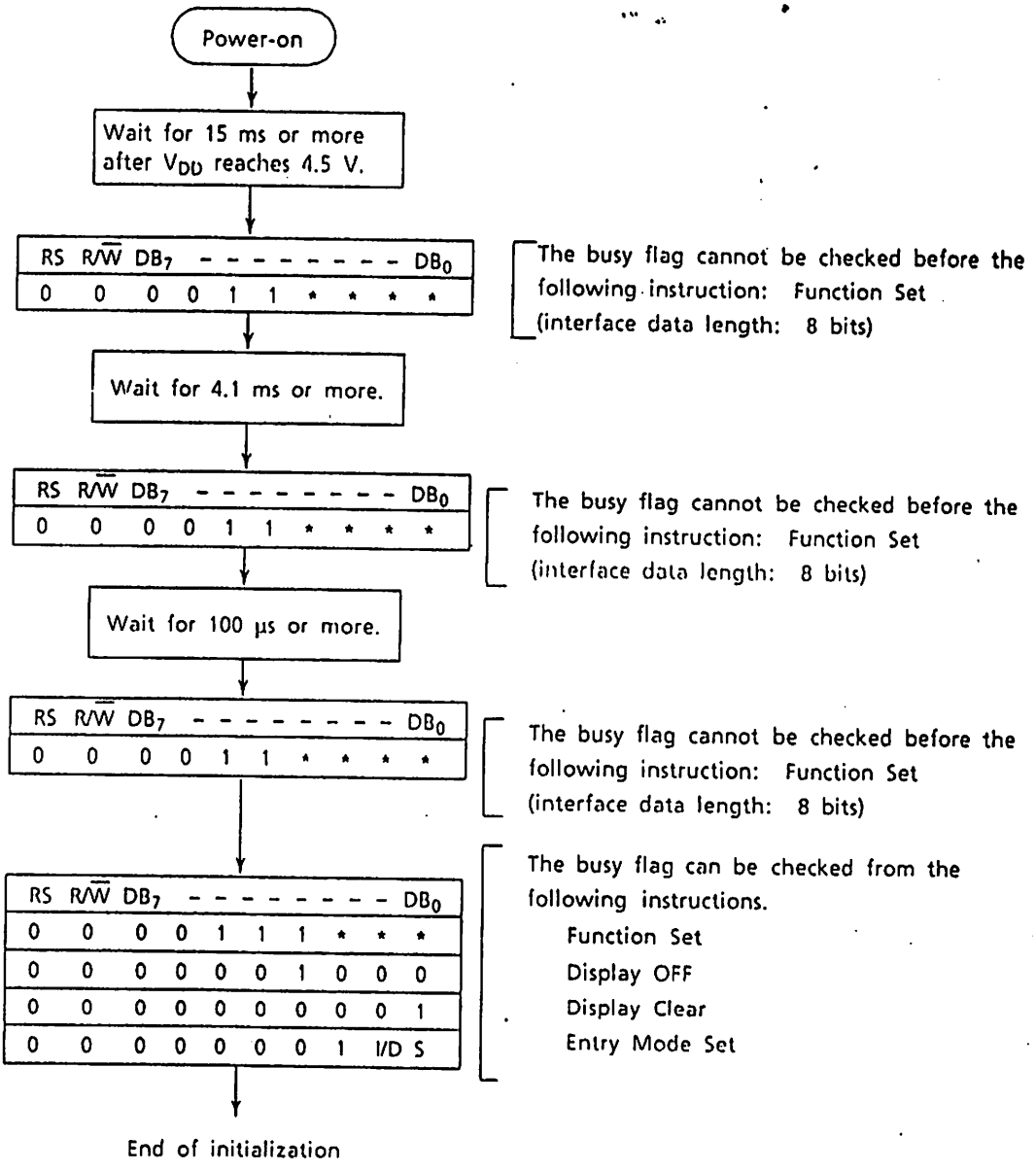
The following instructions are executed for initialization.

- 5 x 7 dot-matrix character font: 1/8 duty
- Display clear
- Function Set — DL = 1: Interface data length: 8 bits
- Display ON/OFF Control — D = 0: Display OFF; C = 0: Cursor OFF; B = 0: Blink OFF
- Entry mode — I/O = 1: Increment; S = 0: No display shift

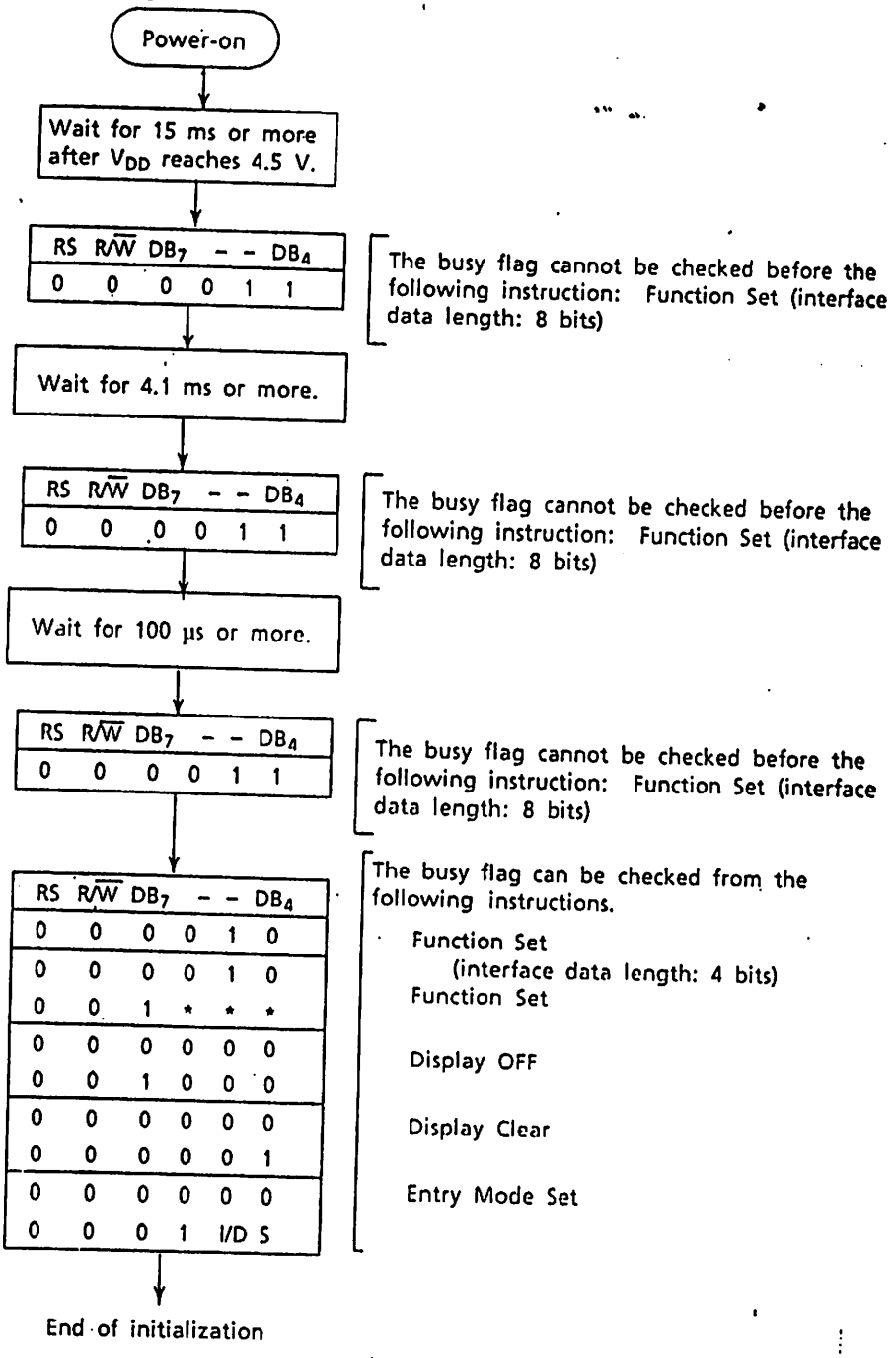
Since the condition is not suitable for the M1632, further function setting is necessary.

If automatic initialization is not executed because the above power supply conditions are not satisfied, use the instruction from next page on.

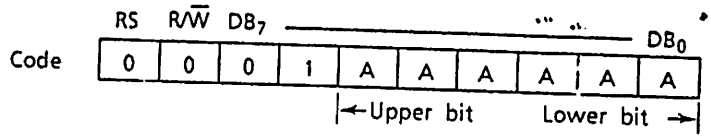
(a) Interface data length : Eight bits



(b) Interface data length: Four bits

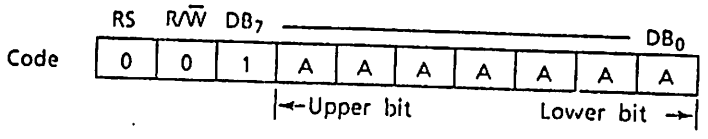


(7) CG RAM Address Set



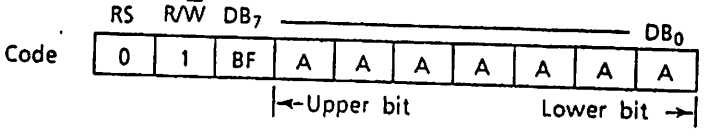
CG RAM addresses expressed as binary AAAAAA are set to the AC. Then data in CG RAM is written from or read to the MPU.

(8) DD RAM Address Set



DD RAM addresses expressed as binary AAAAAAA are set to the AC. Then data in DD RAM is written from or read to the MPU. The addresses used for display in line 1 (AAAAAAA) are 00_H to 27_H and those for line 2 (AAAAAAA) are 40_H to 67_H.

(9) Busy Flag/Address Read



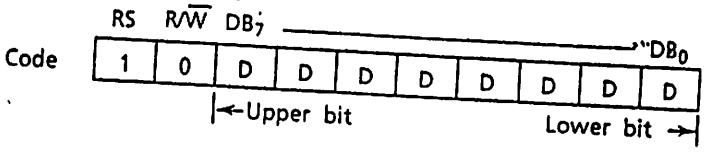
The BF signal is read out, indicating that the module is working internally because of the previous instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

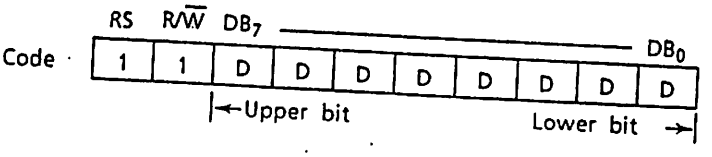
Therefore, make sure that BF = 0 before writing the next instruction. The AC values of binary AAAAAAA are read out at the same time as reading the busy flag. The AC addresses are used for both CG RAM and DD RAM but the address set before execution of the instruction determines which address is to be used.

(10) Data Write to CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is written into CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

(11) Data Read from CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. In addition, either instruction (7) or (8) must be executed immediately before this instruction. If no address set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.

After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

Note : The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

Correct data is read out under the following conditions.

- An address set instruction is executed immediately before readout.
- For DD RAM, the Cursor Shift instruction is executed immediately before readout.
- The second, or later, instruction is executed in consecutive execution of read instructions.

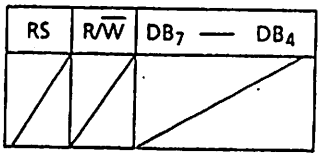
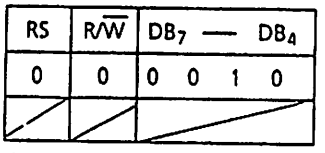
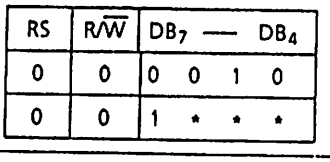
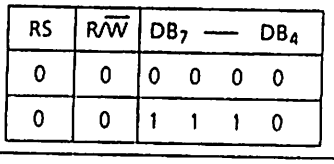
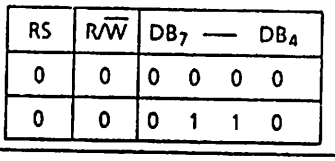
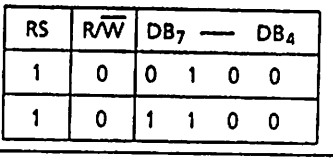
2.6 Examples of Instruction Use

(1) Interface data length: Eight bits

No.	Instruction	Display	Operation
1	Power-on RS: —, R/W: —, DB7 — DB0: —		The built-in reset circuit initializes the module.
2	Function Set RS: 0, R/W: 0, DB7 — DB0: 0 0 1 1 1 * * *		The interface data length is set to 8 bits. The character format becomes 5 x 7 dot-matrix at 1/16 duty cycle.
3	Display ON/OFF Control RS: 0, R/W: 0, DB7 — DB0: 0 0 0 0 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
4	Entry Mode Set RS: 0, R/W: 0, DB7 — DB0: 0 0 0 0 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
5	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 — DB0: 0 1 0 0 1 1 0 0	L_	L is written. The AC is incremented by one and the cursor shifts to the right.
6	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 — DB0: 0 1 0 0 0 0 1 1	LC_	C is written.
7	⋮	⋮	
8	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 — DB0: 0 0 1 1 0 0 1 0	LCD MODULE M1632	2 is written in digit 16. Cursor disappears.

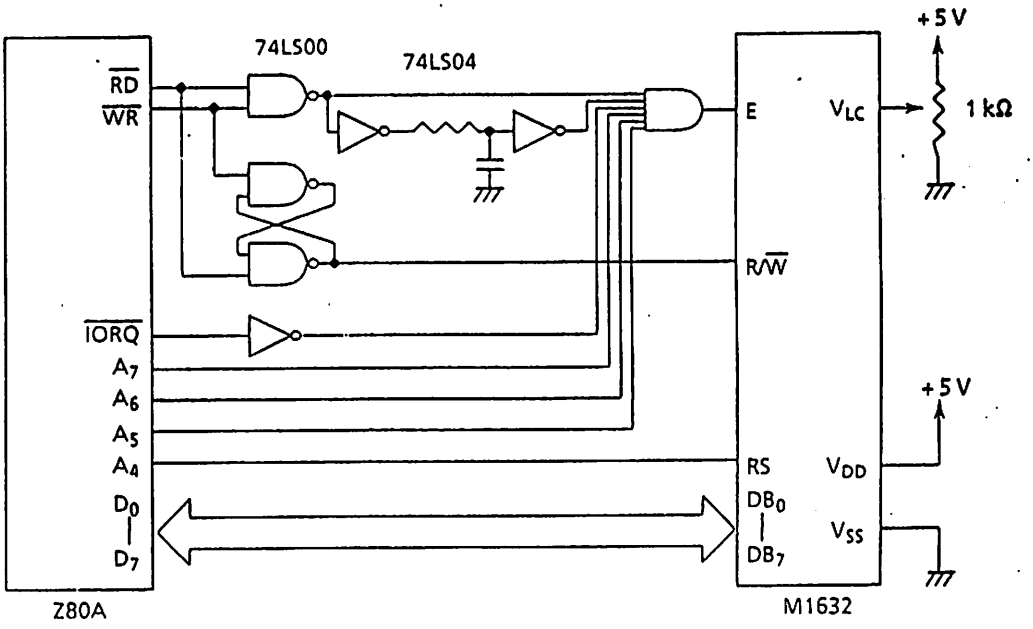
No.	Instruction	Display	Operation
9	DD RAM address set RS: 0, R/W: 0, DB7 —— DB0: 1 1 0 0 0 0 0 0	LCD MODULE M1632 _	The DD RAM address is set so that the cursor appears at digit 1 of line 2.
10	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 —— DB0: 0 0 1 1 0 0 0 1	LCD MODULE M1632 1_	1 is written.
11	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 —— DB0: 0 0 1 1 0 1 1 0	LCD MODULE M1632 16_	6 is written.
12	⋮	⋮	
13	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 —— DB0: 0 1 0 1 0 0 1 1	LCD MODULE M1632 16DIGITS,2LINES	S is written.
14	DD RAM address set RS: 0, R/W: 0, DB7 —— DB0: 1 0 0 0 0 0 0 0	LCD MODULE M1632 16DIGITS,2LINES	The cursor returns to the home position.
15	Display clear RS: 0, R/W: 0, DB7 —— DB0: 0 0 0 0 0 0 0 1	_	All the display disappears and the cursor remains at the home position.
16	⋮	⋮	

(2) Interface data length: Four bits

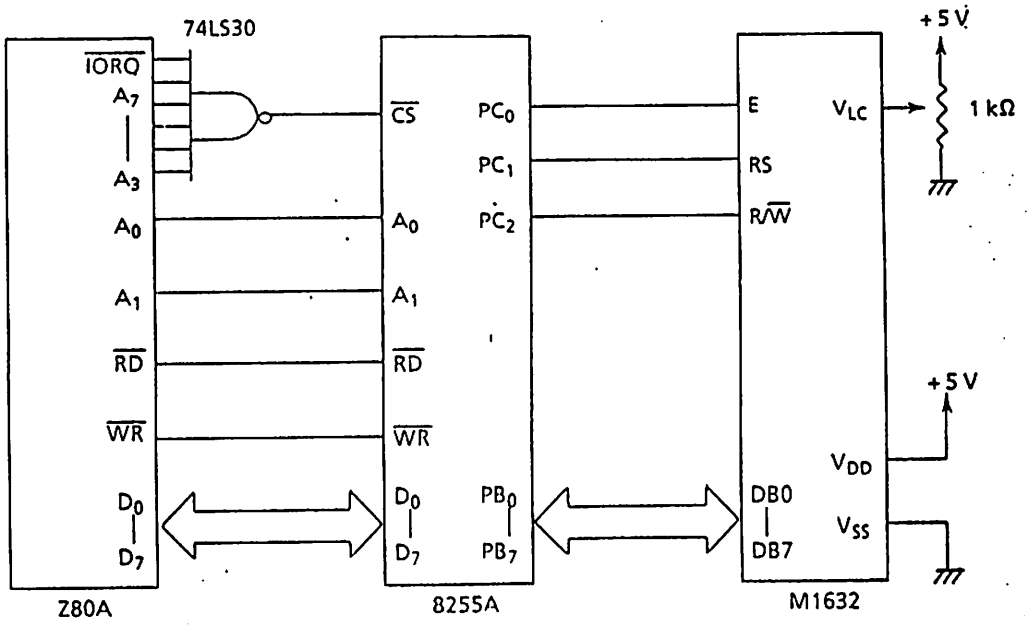
No.	Instruction	Display	Operation
1	Power-on 		The built-in reset circuit initializes the module.
2	Function Set 		Four-bit operation mode is set. *Eight-bit operation mode is set by initialization, and the instruction is executed only once.
3	Function Set 		The 4-bit operation mode, 1/16 duty cycle, and 5 x 7 dot-matrix character format are selected. Then 4-bit operation mode starts.
4	Display ON/OFF Control 	_	The display and cursor are turned ON, but nothing is displayed.
5	Entry Mode Set 	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
6	Write to CG RAM or DD RAM 	L_	L is written. the AC is incremented by one and the cursor shifts to the right.

2.7 MPU Connection Diagrams

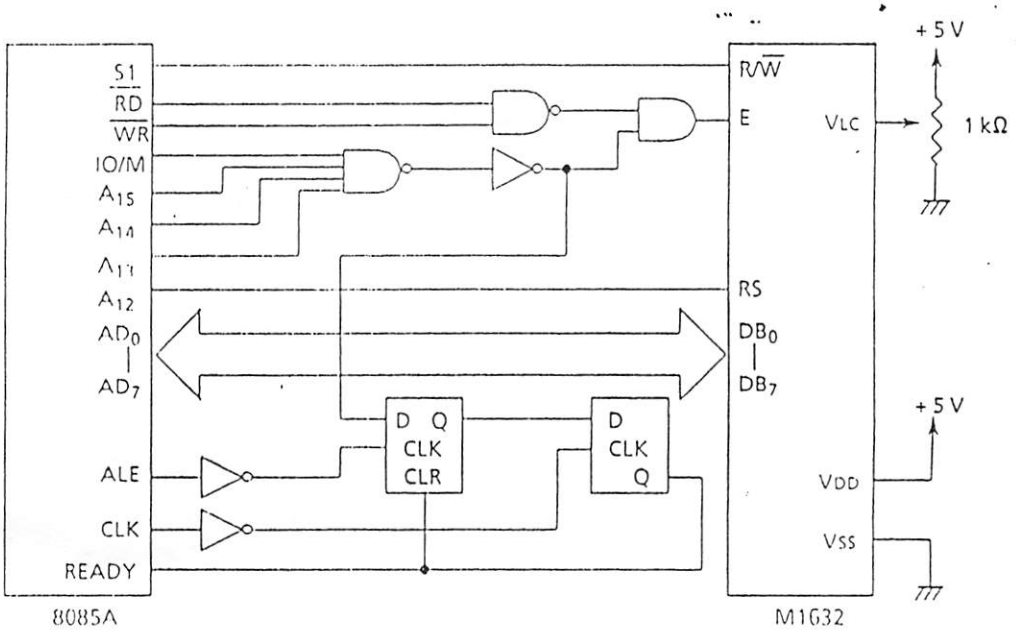
2.7.1 Z80A



2.7.2 Z80A and 8255A



2.7.3 8085A


S1
RD
WR
IO/M
A15
A14
A13
A12
AD0
AD7
ALE
CLK
READY
8085A
D Q
CLK
CLR
D
CLK
Q
R/W
E
RS
DB0
DB7
VLC
VDD
VSS
+5 V
1 kΩ
+5 V
M1632

3. NOTES

Safety

- If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

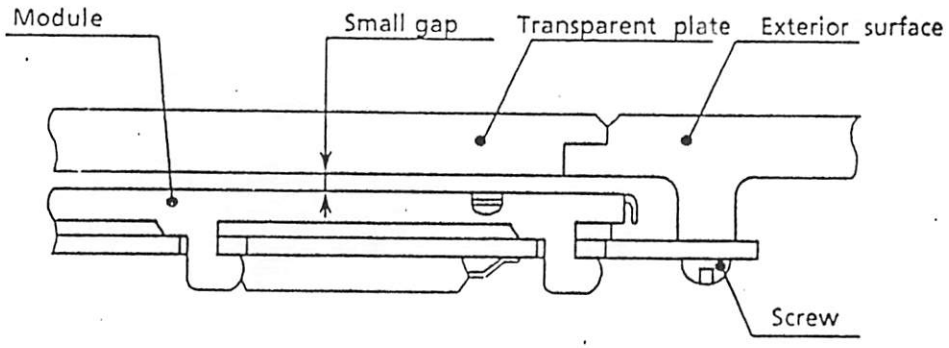
Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizing plate of the display is very fragile; handle it very carefully

Mounting and Design

- Mount the module by using the specified mounting part and holes.
- Connect a 10-μF capacitor between the power supply terminals to eliminate noise.
- To protect the module from external pressure, place a transparent plates (e.g. acrylic or glass), leaving a small gap, over the display surface, frame, and polarizing plate.

☆Example



- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)[1]

Address	Register	Symbol	After reset
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor mode register 0 [1]	PM0	00₁₆
0005₁₆	Processor mode register 1	PM1	00₁₆
0006₁₆	System clock control register 0	CM0	01101000₂
0007₁₆	System clock control register 1	CM1	00100000₂
0008₁₆	High-speed on-chip oscillator control register 0	HR0	00₁₆
0009₁₆	Address match interrupt enable register	AIER	XXXXXX00₂
000A₁₆	Protect register	PRCR	00XXX000₂
000B₁₆	High-speed on-chip oscillator control register 1	HR1	40₁₆
000C₁₆	Oscillation stop detection register	OCD	00000100₂
000D₁₆	Watchdog timer reset register	WDTR	XX₁₆
000E₁₆	Watchdog timer start register	WDTS	XX₁₆
000F₁₆	Watchdog timer control register	WDC	00011111₂
0010₁₆	Address match interrupt register 0	RMAD0	00₁₆
0011₁₆			00₁₆
0012₁₆			X0₁₆
0013₁₆			
0014₁₆	Address match interrupt register 1	RMAD1	00₁₆
0015₁₆			00₁₆
0016₁₆			X0₁₆
0017₁₆			
0018₁₆			
0019₁₆	Voltage detection register 1 [2]	VCR1	00001000₂
001A₁₆	Voltage detection register 2 [2]	VCR2	00₁₆ [3] 10000000₂ [4]
001B₁₆			
001C₁₆			
001D₁₆			
001E₁₆	INT0 input filter select register	INT0F	XXXXX000₂
001F₁₆	Voltage detection interrupt register [2]	D4INT	00₁₆ [3] 01000001₂ [4]
0020₁₆			
0021₁₆			
0022₁₆			
0023₁₆			
0024₁₆			
0025₁₆			
0026₁₆			
0027₁₆			
0028₁₆			
0029₁₆			
002A₁₆			
002B₁₆			
002C₁₆			
002D₁₆			
002E₁₆			
002F₁₆			
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆			
0039₁₆			
003A₁₆			
003B₁₆			
003C₁₆			
003D₁₆			
003E₁₆			
003F₁₆			

X : Undefined

NOTES:

1. Blank columns are all reserved space. No access is allowed.
2. Software reset or the watchdog timer reset does not affect this register.
3. Owing to Reset input.
4. In the case of RESET pin = H retaining.

Table 4.2 SFR Information(2)(1)

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆			
0049₁₆			
004A₁₆			
004B₁₆			
004C₁₆			
004D₁₆	Key input interrupt control register	KUPIC	XXXXX000₂
004E₁₆	AD conversion interrupt control register	ADIC	XXXXX000₂
004F₁₆			
0050₁₆	Compare 1 interrupt control register	CMP1IC	XXXXX000₂
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX000₂
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX000₂
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX000₂
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX000₂
0055₁₆	INT2 interrupt control register	INT2IC	XXXXX000₂
0056₁₆	Timer X interrupt control register	TXIC	XXXXX000₂
0057₁₆	Timer Y interrupt control register	TYIC	XXXXX000₂
0058₁₆	Timer Z interrupt control register	TZIC	XXXXX000₂
0059₁₆	INT1 interrupt control register	INT1IC	XXXXX000₂
005A₁₆	INT3 interrupt control register	INT3IC	XXXXX000₂
005B₁₆	Timer C interrupt control register	TCIC	XXXXX000₂
005C₁₆	Compare 0 interrupt control register	CMP0IC	XXXXX000₂
005D₁₆	INT0 interrupt control register	INT0IC	XX00X000₂
005E₁₆			
005F₁₆			
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

X : Undefined

NOTES:

1. Blank columns are all reserved space. No access is allowed.

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After reset
0080₁₆	Timer Y, Z mode register	TYZMR	00₁₆
0081₁₆	Prescaler Y	PREY	FF₁₆
0082₁₆	Timer Y secondary	TYSC	FF₁₆
0083₁₆	Timer Y primary	TYPR	FF₁₆
0084₁₆	Timer Y, Z waveform output control register	PUM	00₁₆
0085₁₆	Prescaler Z	PREZ	FF₁₆
0086₁₆	Timer Z secondary	TZSC	FF₁₆
0087₁₆	Timer Z primary	TZPR	FF₁₆
0088₁₆			
0089₁₆			
008A₁₆	Timer Y, Z output control register	TYZOC	00₁₆
008B₁₆	Timer X mode register	TXMR	00₁₆
008C₁₆	Prescaler X	PREX	FF₁₆
008D₁₆	Timer X register	TX	FF₁₆
008E₁₆	Count source set register	TCSS	00₁₆
008F₁₆			
0090₁₆ 0091₁₆	Timer C register	TC	00₁₆ 00₁₆
0092₁₆			
0093₁₆			
0094₁₆			
0095₁₆			
0096₁₆	External input enable register	INTEN	00₁₆
0097₁₆			
0098₁₆	Key input enable register	KIEN	00₁₆
0099₁₆			
009A₁₆	Timer C control register 0	TCC0	00₁₆
009B₁₆	Timer C control register 1	TCC1	00₁₆
009C₁₆ 009D₁₆	Capture, compare 0 register	TM0	00₁₆ 00₁₆(2)
009E₁₆ 009F₁₆	Compare 1 register	TM1	FF₁₆ FF₁₆
00A0₁₆	UART0 transmit/receive mode register	U0MR	00₁₆
00A1₁₆	UART0 bit rate register	U0BRG	XX₁₆
00A2₁₆ 00A3₁₆	UART0 transmit buffer register	U0TB	XX₁₆ XX₁₆
00A4₁₆	UART0 transmit/receive control register 0	U0C0	000010002
00A5₁₆	UART0 transmit/receive control register 1	U0C1	000000102
00A6₁₆ 00A7₁₆	UART0 receive buffer register	U0RB	XX₁₆ XX₁₆
00A8₁₆	UART1 transmit/receive mode register	U1MR	00₁₆
00A9₁₆	UART1 bit rate register	U1BRG	XX₁₆
00AA₁₆ 00AB₁₆	UART1 transmit buffer register	U1TB	XX₁₆ XX₁₆
00AC₁₆	UART1 transmit/receive control register 0	U1C0	000010002
00AD₁₆	UART1 transmit/receive control register 1	U1C1	000000102
00AE₁₆ 00AF₁₆	UART1 receive buffer register	U1RB	XX₁₆ XX₁₆
00B0₁₆	UART transmit/receive control register 2	UCON	00₁₆
00B1₁₆			
00B2₁₆			
00B3₁₆			
00B4₁₆			
00B5₁₆			
00B6₁₆			
00B7₁₆			
00B8₁₆			
00B9₁₆			
00BA₁₆			
00BB₁₆			
00BC₁₆			
00BD₁₆			
00BE₁₆			
00BF₁₆			

X : Undefined

NOTES:

1. Blank columns are all reserved space. No access is allowed.
2. When the output compare mode is selected (the TCC13 bit in the TCC1 register = 1), the value is set to FFFF16.

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After reset
00C016	AD register	AD	XX16
00C116			XX16
00C216			
00C316			
00C416			
00C516			
00C616			
00C716			
00C816			
00C916			
00CA16			
00CB16			
00CC16			
00CD16			
00CE16			
00CF16			
00D016			
00D116			
00D216			
00D316			
00D416	AD control register 2	ADCON2	0016
00D516			
00D616	AD control register 0	ADCON0	00000XXX2
00D716	AD control register 1	ADCON1	0016
00D816			
00D916			
00DA16			
00DB16			
00DC16			
00DD16			
00DE16			
00DF16			
00E016	Port P0 register	P0	XX16
00E116	Port P1 register	P1	XX16
00E216	Port P0 direction register	PD0	0016
00E316	Port P1 direction register	PD1	0016
00E416			
00E516	Port P3 register	P3	XX16
00E616			
00E716	Port P3 direction register	PD3	0016
00E816	Port P4 register	P4	XX16
00E916			
00EA16	Port P4 direction register	PD4	0016
00EB16			
00EC16			
00ED16			
00EE16			
00EF16			
00F016			
00F116			
00F216			
00F316			
00F416			
00F516			
00F616			
00F716			
00F816			
00F916			
00FA16			
00FB16			
00FC16	Pull-up control register 0	PUR0	00XX00002
00FD16	Pull-up control register 1	PUR1	XXXXXX0X2
00FE16	Port P1 drive capacity control register	DRR	0016
00FF16	Timer C output control register	TCOUT	0016
≈			≈
01B316	Flash memory control register 4	FMR4	010000002
01B416			
01B516	Flash memory control register 1	FMR1	1000000X2
01B616			
01B716	Flash memory control register 0	FMR0	000000012
0FFFF16	Option function select register (2)	OFS	Note 2

X : Undefined

NOTES:

1. The blank areas, 010016 to 01B216 and 01B816 to 02FF16 are reserved and cannot be used by users.
2. The watchdog timer control bit is assigned. Refer to "Figure11.2 OFS, WDC, WDTR and WDTS registers" of Hardware Manual for details

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
Vcc	Supply voltage	Vcc=AVcc	-0.3 to 6.5	V
AVcc	Analog supply voltage	Vcc=AVcc	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to Vcc+0.3	V
Vo	Output voltage		-0.3 to Vcc+0.3	V
P_d	Power dissipation	Topr=25 °C	300	mW
Topr	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
Tstg	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter	Conditions	Standard Min.	Standard Typ.	Standard Max.	Unit
Vcc	Supply voltage		2.7		5.5	V
AVcc	Analog supply voltage			Vcc[3]		V
Vss	Supply voltage			0		V
AVss	Analog supply voltage			0		V
V_{IH}	"H" input voltage		0.8Vcc		Vcc	V
V_{IL}	"L" input voltage		0		0.2Vcc	V
$I_{OH\ (sum)}$	"H" peak all output currents: Sum of all pins' IOH (peak)				-60.0	mA
$I_{OH\ (peak)}$	"H" peak output current				-10.0	mA
$I_{OH\ (avg)}$	"H" average output current				-5.0	mA
$I_{OL\ (sum)}$	"L" peak all output currents: Sum of all pins' IOL (peak)				60	mA
$I_{OL\ (peak)}$	"L" peak output current: Except P1o to P17				10	mA
	P1o to P17	Drive ability HIGH			30	mA
		Drive ability LOW			10	mA
$I_{OL\ (avg)}$	"L" average output current: Except P1o to P17				5	mA
	P1o to P17	Drive ability HIGH			15	mA
		Drive ability LOW			5	mA
f(XIN)	Main clock input oscillation frequency	3.0V ≤ Vcc ≤ 5.5V	0		20	MHz
		2.7V ≤ Vcc < 3.0V	0		10	MHz

Note
1: Referenced to Vcc = AVcc = 2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2: The mean output current is the mean value within 100ms.
3: Set Vcc=AVcc

Table 5.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} =Vcc			10	Bit
–	Absolute accuracy	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V			±3	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V			±2	LSB
		10 bit mode	øAD=10 MHz, Vref=Vcc=3.3V[3]			±5	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=3.3V[3]			±2	LSB
R_{LADDER}	Ladder resistance		V_{REF}=Vcc	10		40	kΩ
t_{CONV}	Conversion time	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	3.3			µs
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	2.8			µs
V_{REF}	Reference voltage				Vcc[4]		V
V_{IA}	Analog input voltage			0		V_{ref}	V
–	A/D operation clock frequency[2]	Without sample & hold		0.25		10	MHz
		With sample & hold		1.0		10	MHz

Note
1: Referenced to Vcc=AVcc=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2: When f_{AD} is 10 MHz more, divide the f_{AD} and make A/D operation clock frequency ($Ø_{AD}$) lower than 10 MHz.
3: When the AVcc is less than 4.2V, divide the f_{AD} and make A/D operation clock frequency ($Ø_{AD}$) lower than $f_{AD}/2$.
4: Set Vcc=Vref

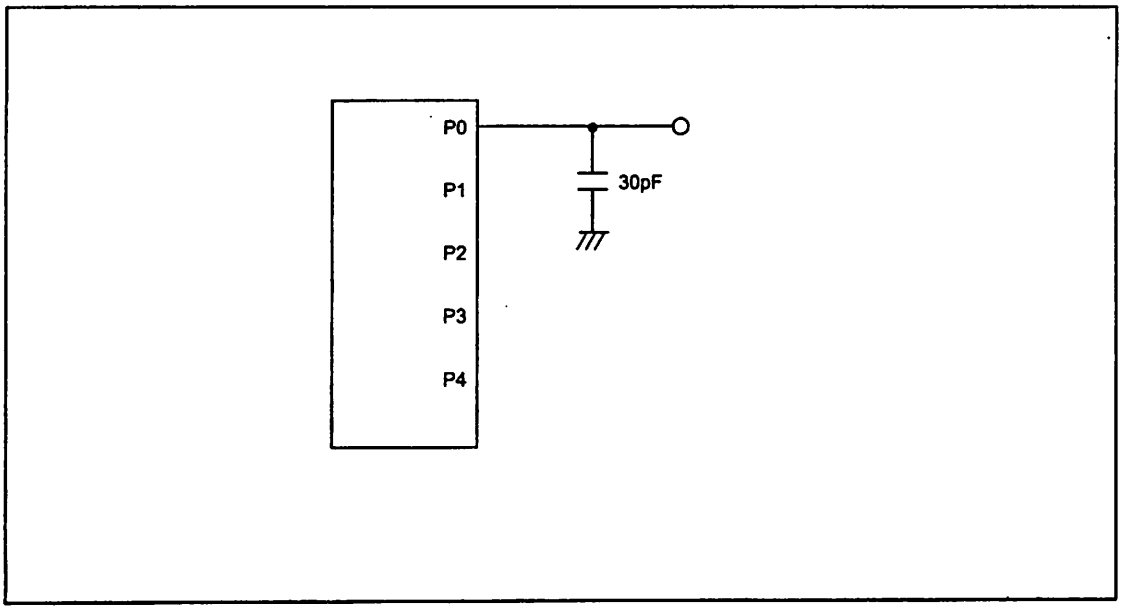


Figure 5.1 Port P0 to P4 measurement circuit

Table 5.4 Flash Memory (Program area) Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase cycle [2]		1000[3]	—	—	cycle
–	Byte program time	Vcc = 5.0 V at Topr = 25 °C	—	50	—	µs
–	Block erase time	Vcc = 5.0 V at Topr = 25 °C	—	0.4	—	s
$t_{d(SR-ES)}$	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
–	Erase Suspend Request Interval		10	—	—	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program, Erase Temperature		0	—	60	°C
–	Data-retention duration	Topr = 55 °C	20	—	—	year

Table 5.5 Flash Memory (Data area Block A, Block B) Electrical Characteristics [4]

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase endurance[2]		10000 [3]	—	—	times
–	Byte program time(program/erase endurance ≤1000 times)	Vcc = 5.0 V at Topr = 25 °C	—	50	400	µs
–	Byte program time(program/erase endurance >1000 times)	Vcc = 5.0 V at Topr = 25 °C	—	65	—	µs
–	Block erase time(program/erase endurance ≤1000 times)	Vcc = 5.0 V at Topr = 25 °C	—	0.2	9	s
–	Block erase time(program/erase endurance >1000 times)	Vcc = 5.0 V at Topr = 25 °C	—	0.3	—	s
$t_{d(SR-ES)}$	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
–	Erase Suspend Request Interval		10	—	—	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program/Erase Temperature		-20(-40)[8]	—	85	°C
–	Data-retention duration	Topr = 55 °C	20	—	—	year

Note
1: Referenced to Vcc=AVcc=2.7 to 5.5V at Topr = 0°C to 60°C unless otherwise specified.
2: Definition of Program/Erase
The cycle of Program/Erase shows a cycle for each block.
If the program/erase number is "n" (n = 1000, 10000), "n" times erase can be performed for each block.
For example, If performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.
However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).
3: Maximum numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.
4: Table 16.5 applies for Block A or B when the Program/Erase cycles are more than 1000. The byte program time up to 1000 cycles are the same as that of the program area (see Table 5.4).
5: To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.
6: If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.
7: Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
8: -40 °C for D version.

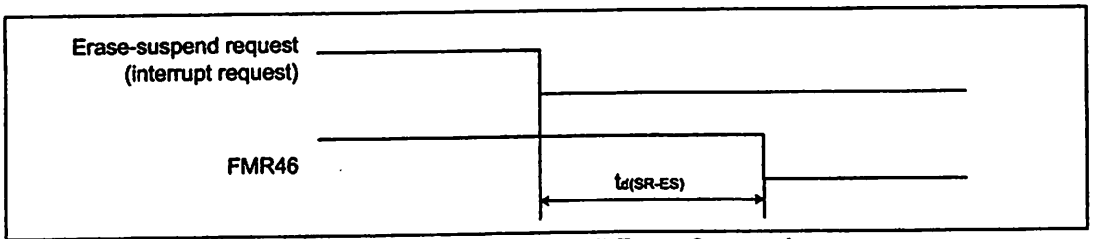


Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard Min.	Standard Typ.	Standard Max.	Unit
Vdet	Voltage detection level		3.3	3.8	4.3	V
	Voltage detection interrupt request generating time[2]			40		µs
	Voltage detection circuit self consumption current	VC27=1, VCC=5.0V		600		nA
td(E-A)	Waiting time until voltage detection circuit operation starts[3]				20	µs
Vccmin	Microcomputer operation voltage minimum value		2.7			V

NOTES:
1. The measuring condition is Vcc=AVcc=2.7V to 5.5V and Topr=-40°C to 85°C.
2. This shows the time until the voltage detection interrupt request is generated since the voltage passes Vdet.
3. This shows the required time until the voltage detection circuit operates when setting to "1" again after setting the VC27 bit in the VCR2 register to "0".

Table 5.7 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2[1, 3])

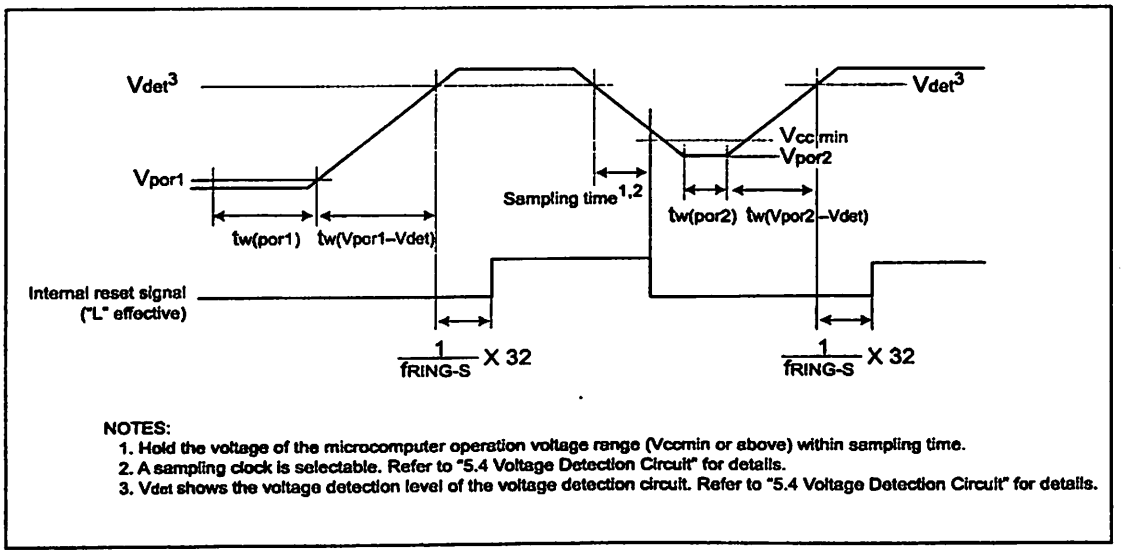
Symbol	Parameter	Measuring condition	Standard Min.	Standard Typ.	Standard Max.	Unit
Vpor2	Power-on reset valid voltage	-20°C ≤ Topr < 85°C	—	—	Vdet	V
tw(Vpor2-Vdet)	Supply voltage rising time when power-on reset is canceled[2]	-20°C ≤ Topr < 85°C, tw(por2) ≥ 0s[4]	—	—	100	ms

NOTES:
1. The voltage detection circuit which is embedded in a microcomputer is a factor to generate the hardware reset 2. Refer to 5.1.2 Hardware Reset 2.
2. This condition is not applicable when using Vcc ≥ 1.0V.
3. When turning power on after the external power has been held below the valid voltage for greater than 10 seconds, refer to Table 16.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2).
4. tw(por2) is time to hold the external power below effective voltage (Vpor2).

Table 5.8 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2)

Symbol	Parameter	Measuring condition	Standard Min.	Standard Typ.	Standard Max.	Unit
Vpor1	Power-on reset valid voltage	-20°C ≤ Topr < 85°C	—	—	0.1	V
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 10s[2]	—	—	100	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	-20°C ≤ Topr < 0°C, tw(por1) ≥ 30s[2]	—	—	100	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	-20°C ≤ Topr < 0°C, tw(por1) ≥ 10s[2]			1	ms
tW(Vpor1-Vdet)	Supply voltage rising time when power-on reset is canceled	0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 1s[2]			0.5	ms

NOTES:
1. When not using hardware reset 2, use with Vcc ≥ 2.7V.
2. tw(por1) is time to hold the external power below effective voltage (Vpor1).



NOTES:
1. Hold the voltage of the microcomputer operation voltage range (Vccmin or above) within sampling time.
2. A sampling clock is selectable. Refer to "5.4 Voltage Detection Circuit" for details.
3. Vdet shows the voltage detection level of the voltage detection circuit. Refer to "5.4 Voltage Detection Circuit" for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.9 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
-	High-speed on-chip oscillator frequency 1 / {td(HRoffset)+td(HR)} when the reset is released	VCC=5.0V, Topr=25 °C Set "40₁₆" in the HR1 register		8	- -	MHz
td(HRoffset)	Settable high-speed on-chip oscillator minimum period	VCC=5.0V, Topr=25 °C Set "00₁₆" in the HR1 register		61		ns
td(HR)	High-speed on-chip oscillator period adjusted unit	Differences when setting "01₁₆" and "00₁₆" in the HR register	-	1	- -	ns
	High-speed on-chip oscillator temperature dependence(1)	Frequency fluctuation in temperature range of -10 °C to 50 °C		±5		%
-	High-speed on-chip oscillator temperature dependence(2)	Frequency fluctuation in temperature range of -40 °C to 85 °C	- -	±10	- -	%

NOTES:
1. The measuring condition is Vcc=AVcc=5.0 V and Topr=25 °C.

Table 5.10 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on[2]		1		2000	µs
td(R-S)	STOP release time[3]				150	µs

Note
1: The measuring condition is Vcc=AVcc=2.7 to 5.5 V and Topr=25 °C.
2: This shows the wait time until the internal power supply generating circuit is stabilized during power-on.
3: This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

Table 5.11 Electrical Characteristics (1) [Vcc=5V]

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-5mA	Vcc-2.0	- -	Vcc	V
			I_{OH}=-200µA	Vcc-0.3	- -	Vcc	V
		X_{OUT}	Drive capacity HIGH I_{OH}=-1 mA	Vcc-2.0	- -	Vcc	V
			Drive capacity LOW I_{OH}=-500µA	Vcc-2.0	-	Vcc	V
V_{OL}	"L" output voltage	P10 to P17 Except X_{OUT}	I_{OL}= 5 mA	- -		2.0	V
			I_{OL}= 200 µA	- -	- -	0.45	V
		P10 to P17	Drive capacity HIGH I_{OL}= 15 mA	- -	- -	2.0	V
			Drive capacity LOW I_{OL}= 5 mA	- -	-	2.0	V
			Drive capacity LOW I_{OL}= 200 µA	-		0.45	V
		X_{OUT}	Drive capacity HIGH I_{OL}= 1 mA	-		2.0	V
			Drive capacity LOW I_{OL}=500 µA	- -	- -	2.0	V
V_{T+}-V_{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, T_{CIN}, RxD0, RxD1, P4S		0.2		1.0	V
		RESET		0.2		2.2	V
I_{IH}	"H" input current		V_I=5V			5.0	µA
I_{IL}	"L" input current		V_I=0V	- -		-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V	30	50	167	kΩ
R_{XIN}	Feedback resistance	X_{IN}		- -	1.0	- -	MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency			40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode	2.0			V

Note
1 : Referenced to Vcc=AVcc=4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Table 5.12 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter	Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
Icc	Power supply current (Vcc=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are Vss	High-speed mode	XIN=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		9	15	mA
			XIN=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		8	14	mA
			XIN=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		5		mA
		Medium-speed mode	XIN=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		4		mA
			XIN=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		3		mA
			XIN=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		2		mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division		4	8	mA
			Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8		1.5		mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		470	900	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation VC27="0"		40	80	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off VC27="0"		38	76	µA
		Stop mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0"		0.8	3.0	µA

NOTES
1: The power supply current measuring is executed using the measuring program on frash memory.
2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: Vcc = 5V, Vss = 0V at Ta = 25 °C) [Vcc=5V]

Table 5.13 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(XIN)	XIN input cycle time	50		ns
twH(XIN)	XIN input HIGH pulse width	25		ns
twL(XIN)	XIN input LOW pulse width	25		ns

Table 5.14 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CNTR0)	CNTR0 input cycle time	100		ns
twH(CNTR0)	CNTR0 input HIGH pulse width	40		ns
twL(CNTR0)	CNTR0 input LOW pulse width	40		ns

Table 5.15 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TCIN)	TCIN input cycle time	400 [1]		ns
twH(TCIN)	TCIN input HIGH pulse width	200 [2]		ns
twL(TCIN)	TCIN input LOW pulse width	200 [2]		ns

NOTES
1 :When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).
2 : When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.16 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input HIGH pulse width	100		ns
tw(CKL)	CLKi input LOW pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	35		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.17 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INT0}$ input HIGH pulse width	250 [1]		ns
tw(INL)	$\overline{INT0}$ input LOW pulse width	250 [2]		ns

NOTES
1 : When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2 : When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

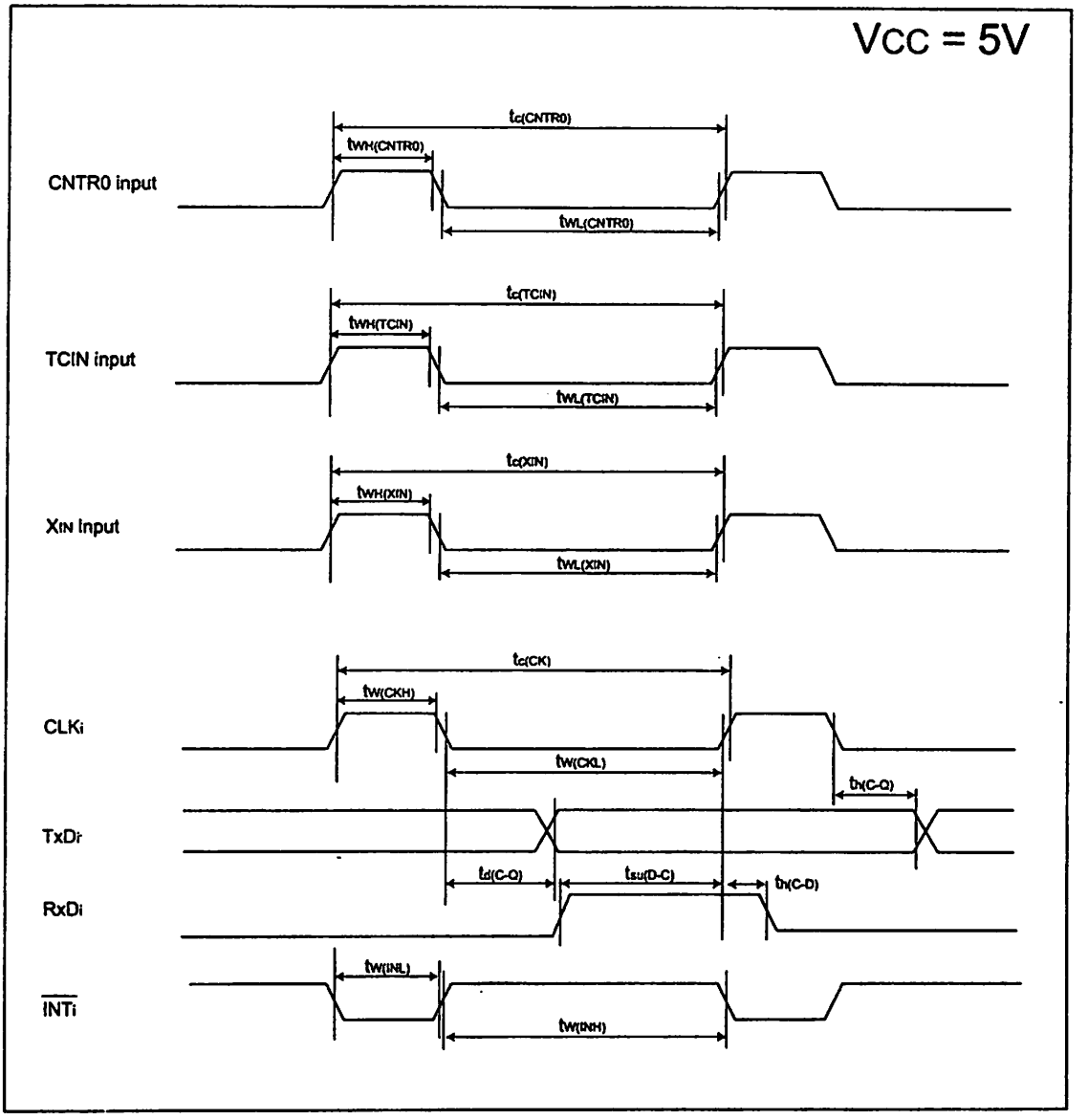


Figure 5.4 Vcc=5V timing diagram

Table 5.18 Electrical Characteristics (3) [Vcc=3V]

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-1mA	Vcc-0.5	---	Vcc	V
		X_{OUT}	Drive capacity HIGH I_{OH}=-0.1 mA	Vcc-0.5	---	Vcc	V
			Drive capacity LOW I_{OH}=-50 µA	Vcc-0.5	---	Vcc	V
V_{OL}	"L" output voltage	P10 to P17 Except X_{OUT}	I_{OL}= 1 mA	---	---	0.5	V
		P10 to P17	Drive capacity HIGH I_{OL}= 2 mA	---	---	0.5	V
			Drive capacity LOW I_{OL}= 1 mA	---	---	0.5	V
		X_{OUT}	Drive capacity HIGH I_{OL}= 0.1 mA	---	---	0.5	V
			Drive capacity LOW I_{OL}=50 µA	---	---	0.5	V
V_{T+}-V_{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, T_{CIN}, RxD0, RxD1, P45		0.2	---	0.8	V
		RESET		0.2	---	1.8	V
I_{IH}	"H" input current		V_I=3V	---	---	4.0	µA
I_{IL}	"L" input current		V_I=0V	---	---	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V	66	160	500	kΩ
R_{fXIN}	Feedback resistance	X_{IN}		---	3.0	---	MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency			40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode	2.0	---	---	V

Note
1 : Referenced to Vcc=AVcc=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

Table 5.19 Electrical Characteristics (4) [Vcc=3V]

Symbol	Parameter	Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
Icc	Power supply current (Vcc=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are Vss	High-speed mode	XIN=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		8	13	mA
			XIN=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		7	12	mA
			XIN=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division		5		mA
		Medium-speed mode	XIN=20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		3		mA
			XIN=16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		2.5		mA
			XIN=10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		1.6	---	mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division		3.5	7.5	mA
			Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8		1.5		mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8		420	800	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock operation VC27="0"		37	74	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed[2] Peripheral clock off VC27="0"		35	70	µA
		Stop mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0"		0.7	3.0	µA

NOTES
1: The power supply current measuring is executed using the measuring program on frash memory.
2: Timer Y is operated with timer mode.

Timing requirements (Unless otherwise noted: Vcc = 3V, Vss = 0V at Ta = 25 °C) [Vcc=3V]

Table 5.20 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(XIN)	XIN input cycle time	100		ns
twH(XIN)	XIN input HIGH pulse width	40		ns
twL(XIN)	XIN input LOW pulse width	40		ns

Table 5.21 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CNTR0)	CNTR0 input cycle time	300		ns
twH(CNTR0)	CNTR0 input HIGH pulse width	120		ns
twL(CNTR0)	CNTR0 input LOW pulse width	120		ns

Table 5.22 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TCIN)	TCIN input cycle time	1200 [1]		ns
twH(TCIN)	TCIN input HIGH pulse width	600 [2]		ns
twL(TCIN)	TCIN input LOW pulse width	600 [2]		ns

NOTES
1 :When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).
2 : When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.23 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	300		ns
tw(CKH)	CLKi input HIGH pulse width	150		ns
tw(CKL)	CLKi input LOW pulse width	150		ns
td(C-Q)	TxDi output delay time		160	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	55		ns
th(C-D)	RxDi input hold time	90		ns

Table 5.24 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tw(INH)	$\overline{INT0}$ input HIGH pulse width	380 [1]		ns
tw(INL)	$\overline{INT0}$ input LOW pulse width	380 [2]		ns

NOTES
1 : When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2 : When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

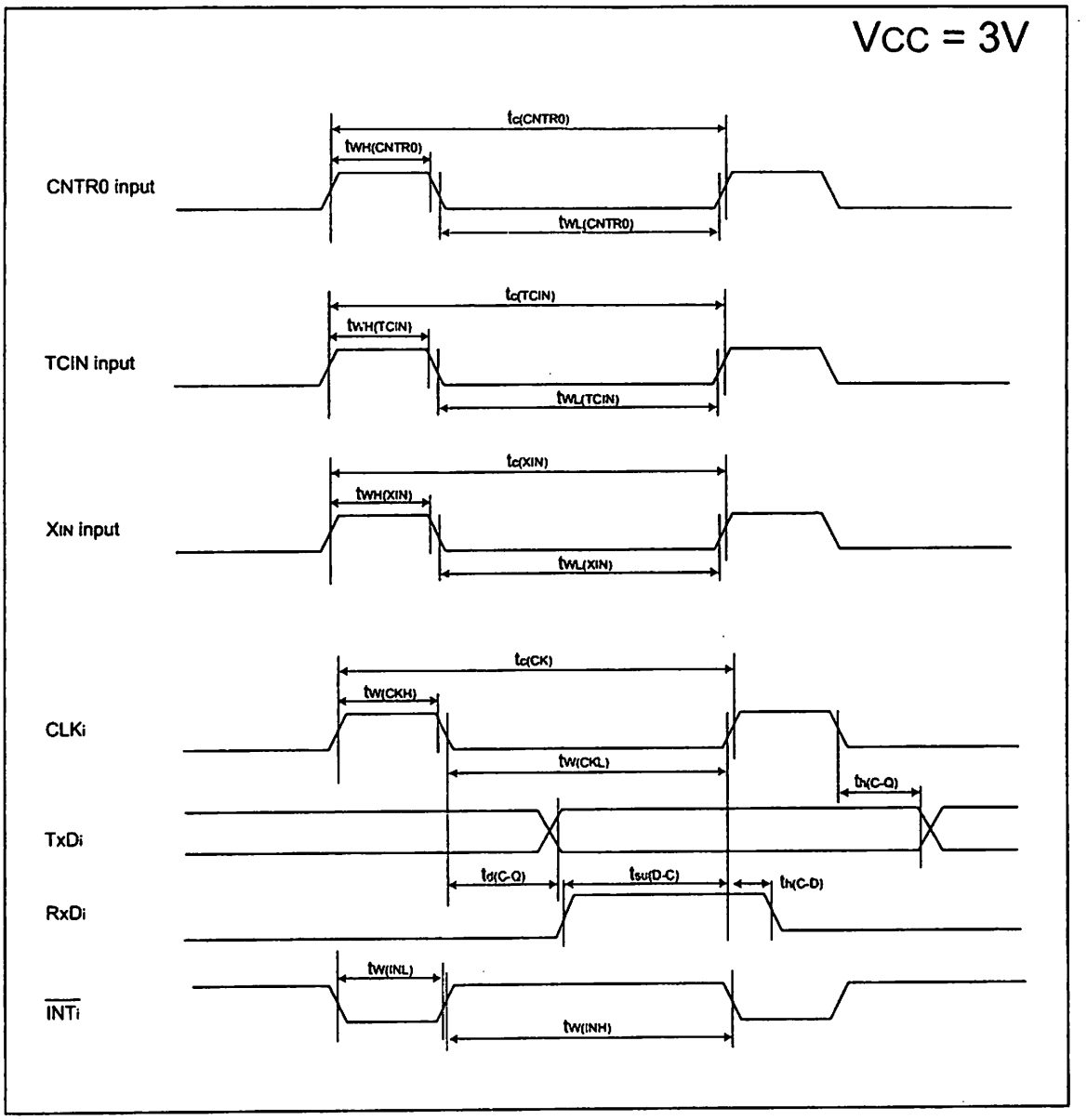
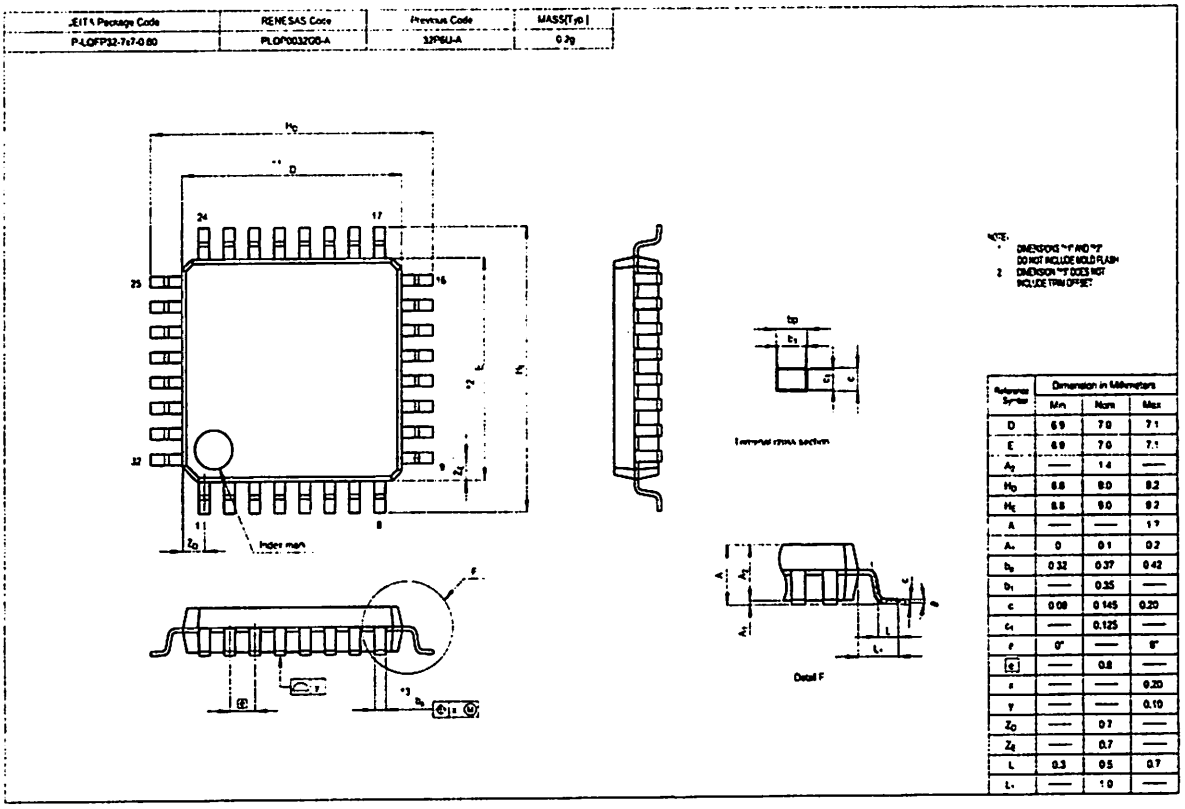


Figure 5.5 Vcc=3V timing diagram

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS(Typ.)
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
x	—	0.8	—
y	—	—	0.20
Y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—