SKRIPSI

PERENCANAAN DAN PEMBUATAN MODULATOR FSK

DENGAN MENGGUNAKAN METODE

DDS (Direct Digital Synthesis)

Disusun Oleh :

BUDI ARTONO

NIM: 03.17.094

KONSENTRASI TEKNIK ELEKTRONIKA
JURUSAN TEKNIK ELEKTRO S-1
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
SEPTEMBER 2007

LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN MODULATOR FSK

DENGAN MENGGUNAKAN METODE DDS *(Direct Digital Synthesis)*

SKRIPSI

Disusun dan diajukan sebagai salah satu syarat untuk memperoleh gelar sarjana Teknik Elektronika Strata Satu (S-1)

Disusun oleh :

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2007

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Judul Skripsi	: Perencanaan dan Pembuatan Modulator FSK dengan Menggunakan Metode DDS (Direct Digital Synthesis)

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Hari : Senin

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Alhamdulillah,…3X

Puji syukur kehadirat Allah SWT atas karunia dan hidayahNya. Engkau telah memberiku semangat bertahan untuk tidak mundur.

Tak lupa saya ucapkan terimakasih kepada pihak pihak yang telah membantu terselesaikannya TAku terutama kepada kedua Orang tuaku, yang selalu mendo'akanku juga Adikku2 Siti dan Ayu. Skalian Sedulur-dulurku Bude-Pakpoh, sekeluarga,juga Ning Fifin sekeluarga.

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Aku pesan aja buat yang mau membaca ini terutama yang belum pernah mengalami TA yaitu adik kelas

"Kerjakan,... apa yang dapat kamu kerjakan sekarang"

jangan bermain main dengan waktu karena kalau kamu mempermainkan waktu, maka waktupun dapat membuatmu menangis menyesal.

Wes ngono tok ae aku gak iso ngarang akeh-akeh. Pokok'e matur sembah nuwun kaleh ngapunten'ne kagem sedoyo engkang dereng kecatet teng kertak niki.

ABSTRAK

PERENCANAAN DAN PEMBUATAN MODULATOR FSK DENGAN MENGUNAKAN METODE DDS (*Direct Digital Synthesizer*)

Budi Artono, 0317094, Jurusan Teknik Elektronika S-1

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Sinyal digital tidak dapat ditransmisikan begitu saja, karena bandwidth (lebar pita) terlalu lebar. Pada makalah ini direalisasikan sebuah sistem yang dapat memodifikasikan sinyal digital agar dapat ditransmisikan. Salah satu metode modulasi sinyal digital adalah Frekuensi shift keying (FSK). Caranya dengan menggunakan mikrokontroler sebagai pemrosesan data sesuai dengan metode DDS (Direct Digital Synthesis) dimana keluaran dari Mikrokontroler berupa sinyal digital menjadi masukan untuk DAC (Digital to Analog Converter), Output dari DAC merupakan sample bentuk gelombang analog yang kemudian akan difilter untuk menghasilkan sinyal sinusoidal yang sempurna. Untuk mendemodulasikan sinyal FSK ke bentuk data digunakan MT8841 sebagai demodulator. Dengan cara ini maka dapat dihasilkan frekuensi dalam bentuk FSK dengan akurasi tinggi dan biaya rendah. Pada pengujian sistem secara keseluruhan boudrate maksimal yang bisa dicapai adalah 1200 bps apabila pengaturannya lebih dari 1200 bps maka data yang diterima oleh PC mengalami kerusakan beberapa buah karakter.

Kata kunci: modulasi, FSK, DDS, mikrokontroller, DAC, filter.

KATA PENGANTAR

Dengan memanjatkan puji syukur kehadirat Allah SWT. Akhirnya penyusun dapat menyelesaikan laporan skripsi yang berjudul **"PERENCANAAN DAN PEMBUATAN MODULATOR FSK DENGAN MENGGUNAKAN METODE DDS (Direct Digital Synthesis)"** ini dengan baik. Skripsi ini merupakan salah satu syarat dalam menyelesaikan studi di program strata 1 (satu) Teknik Elektronika Di Institut Teknologi Nasional Malang.

Dengan terselesainya penyusunan skripsi ini, penulis mengucapkan terima kasih atas bimbingan, petunjuk, saran, serta kesempatan pada semua pihak yang turut membantu dalam penyelesaian skripsi ini. Ucapan terima kasih tersebut penyusun tunjukan kepada :

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5. Bapak Joseph Dedy Irawan, ST, MT, selaku Dosen Pembimbing II

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Malang, 29 Agustus 2007

Penyusun

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BAB I

PENDAHULUAN

1.1.Latar Belakang

Seiring dengan perkembangan teknologi di segala bidang. Perkembangan dibidang elektronika juga mengalami kemajuan yang sangat pesat sehingga hampir setiap peralatan yang digunakan manusia tidak lepas dari penggunaan berbagai macam peralatan elektronika yang ada. Pada perkembangannya, teknologi elektronika menuntut manusia untuk menciptakan suatu peralatan elektronika yang tepat guna dan praktis sehingga dapat membantu semua kegiatan menjadi lebih mudah. Salah satu perkembangan yang paling menonjol saat ini adalah perkembangan di bidang komunikasi,Kemampuan dan ketelitian menghasilkan serta mengendalikan bentuk gelombang berbagai frekuensi telah menjadi suatu kebutuhan kunci yang umum bagi sejumlah industri.

Hal tersebut yang mendasari untuk mengaplikasikan suatu metode *direct digital synthesis* (DDS) untuk memodulasikan *Frequency Shift Keying (FSK)* pada skripsi ini. Seperti diketahui banyak sekali sistem atau metoda memproduksi suatu sinyal sinus ke dalam format digital dan kemudian melakukan suatu konversi digital-ke-analog. Tetapi, sistem yang dapat menawarkan kecepatan tinggi terhadap frekuensi keluaran, resolusi frekuensi bagus dan dengan kemajuan dalam disain teknologi, serta sangat ringkas dan membutuhkan sedikit daya sangat sedikit. Dalam sistem ini semua yang dibutuhkan dapat terpenuhi oleh penggunaan *direct digital synthesis (DDS).*

Dalam skripsi ini penulis mencoba untuk membuat modulator FSK *(Frequency Shift Keying)* dengan menggunakan metode DDS (*Direct Digital Synthesis*).

Adapun prinsip kerjanya adalah sebagai berikut, ketika tombol pada keyboard ditekan maka data dikirim ke mikrokontroler secara serial. Mikrokontroler sebagai pengolah data akan memproses inputan data (kode ASCII dikonversi ke bentuk biner dimana 0 mewakili frekuensi pada nilai f1=1200HZ dan 1 mewakili frekuensi f2=2200HZ) untuk dijadikan proses pada keluaran sesuai dengan perencanaan program. Kemudian dikeluarkan ke DAC, *Output* frekuensi adalah modulasi FSK. *Output* dari DAC merupakan sample bentuk gelombang analog yang kemudian akan dikirim melalui filter sebelum dikeluarkan. Untuk mengetahui apakah data yang dikrim sesuai dengan data yang diterima maka didemodulasikan menggunakan MT8841.

1.2.Tujuan

Tujuan dari skripsi ini adalah untuk memudahkan menghasilkan suatu modulasi frekuensi dalam bentuk FSK dengan akurasi tinggi dan biaya rendah.

1.3.Rumusan Masalah

Dalam perencanaan dan pembuatan modulator FSK dengan mengunakan metode DDS (*Direct Digital Synthesis*) maka permasalahannya adalah bagaimana menghasilkan sinyal sinus dengan akurasi tinggi, membuat suatu alat yang dapat menghasilkan suatu modulasi frekuensi dalam bentuk FSK, dan bagaimana mendemodulasikan frekuensi FSK ke bentuk karakter/data.

1.4.Batasan Masalah

Dalam menyusun skripsi ini diperlukan suatu batasan masalah agar tidak menyimpang dari ruang lingkup yang akan dibahas. Adapun batasan masalahnya adalah sebagai berikut :

a) Membahas tentang sistem dan proses alat.

b) Menggunakan MT8841 sebagai demodulator FSK

c) Menggunakan mikrokontroller ATmega untuk pemrosesan data.

1.5.Metodologi Penulisan

Metodologi yang dipakai dalam pembuatan skripsi ini adalah:

1. Studi Literatur

   Dengan mencari referensi-referensi yang berhubungan dengan perencanaan dan pembuatan alat yang akan dibuat.

2. *Field Research*

   Dengan melakukan penelitian secara langsung mengenai objek-objek yang berhubungan langsung dengan perencanaan alat yang akan dibuat.

3. Pengujian Alat

   Dengan melakukan pengujian perblok rangkaian dan kerja seluruh sistem pada alat tersebut.

1.6.Sistematika Pembahasan

Penulisan skripsi ini terbagi menjadi lima bab dengan sistematika sebagai berikut:

BAB I PENDAHULUAN

Membahas tentang latar belakang, rumusan masalah, tujuan, batasan masalah, metodologi dan sistematika penulisan pada penulisan skripsi ini.

BAB II LANDASAN TEORI

Berisikan tentang penjelasan dan teori-teori yang berhubungan denagn komponen-komponen yang digunakan dalan perancangan alat.

BAB III PERENCANAAN DAN PEMBUATAN ALAT

Membahas tentang perancangan alat yang terdiri dari perancangan perangkat keras dan perancangan perangkat lunak.

BAB IV PENGUJIAN ALAT

Membahas tentang pengujian peralatan secara keseluruhan dan analisa hasil pengujian.

BAB V PENUTUP

Berisikan kesimpulan yang didapat selama perancangan dan pembuatan alat serta saran-saran.

BAB II

DASAR TEORI

2.1 Pendahuluan

Bab ini membahas sistem DDS (*Direct Digital Synthesis*), FSK (Frequency Shift Keying), mikrokontroler ATmega8, DAC (*Digital To Analog Converter*), Filter, Op Amp dan MT8841 sebagai demodulator.

2.2 Latar Belakang DDS

System DDS (*Direct Digital Synthesis*) merupakan salah satu cara untuk menghasilkan sinyal sinusodial secara langsung. Inti dari system ini adalah arsitektur akumulator dengan resolusi mencapai mili Hertz dan frekuensi sinyal yang dihasilkan dapat diatur tergantung dari sinyal frekuensi referensi dan metode perancangan. Keluaran sistem DDS yang diproses oleh Mikrokontroler berupa sinyal digital kemudian menjadi masukan untuk DAC *(D/A converter)* dan LPF *(Low Pass Filter)* untuk menghasilkan sinyal sinusoidal yang sempurna.

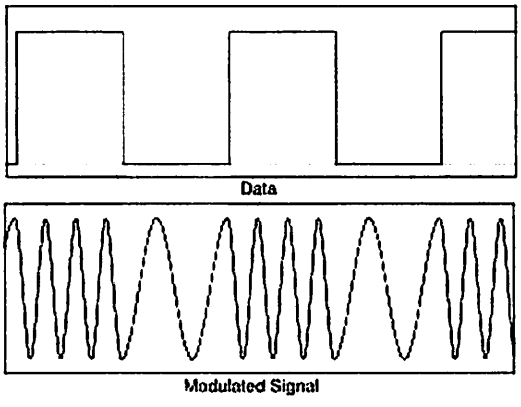
Semua parameter kontrol sistem DDS berada dalam bentuk besaran digital. Sistem DDS pada dasarnya terdiri atas akumulator phasa, LUT (Look Up Table), dan osilator sebagai pembangkit frekuensi referensi (clock). Sedangkan DAC (digital to Analog Converter) dan LPF (Low Pass Filter) merupakan komponen-komponen penunjang sistem DDS.

2.2.1 Kelebihan Dan Fleksibilitas DDS

Kelebihan penggunaan Sistem DDS adalah Karakteristik sistem DDS itu sendiri, dimana keutamaan dari sistem ini adalah memiliki *settling time/*kecepatan yang cepat dan memiliki resolusi frekuensi yang halus terhadap frekuensi keluaran, operasi atas suatu spektrum frekuensi yang lebar dan dengan kemajuan dalam disain teknologi proses. serta sangat ringkas dan sedikit membutuhkan pemakain daya. sehingga sangat memungkinkan sistem DDS bisa lebih dikembangkan untuk desain alat yang berkaitan dengan aplikasi-aplikasi frequency hopping serta system-sistem yang berkaiatan dengan peralatan pemancar radio,TV, peralatan test, dll.

2.3 FSK (Frequency Shift Keying)

Frequency Shift Keying (FSK) adalah modulasi yang menyatakan sinyal digital 1 sebagai suatu nilai tegangan dengan frekuensi (f1 = 2200 Hz), sementara sinyal digital 0 dinyatakan sebagai suatu nilai tegangan dengan frekuensi (f2 = 1200 Hz).pada modulasi frekuensi dapat dilakukan pada beberapa frekuensi sekaligus agar pengiriman data menjadi lebih effisien.



Gambar 2.1

FSK modulation[1]

spektrum secara keseluruhan terdiri dari superposisi 2 spektra FSK dengan frekuensi f1 dan f2.

2.4 Mikrokontroler AVR Atmega8

2.4.1. Arsitektur

AVR Atmega8 adalah mikrokontroler 8-bit CMOS, low-power yang berdasarkan pada bentuk arsitektur AVR RISC (*Reduced Instruction Set Computer*), yang hampir semua instruksinya selesai dikerjakan dalam satu siklus clock. AVR ATmega8 menggunakan instruksi tunggal (*Single Clock Cycle*), yaitu sistem mikrokontroler yang frekuensi kerja dalam chip sama dengan frekuensi kristal untuk osilator tanpa memerlukan rangkaian pembagi frekuensi setelah osilator yang diperlukan untuk memperoleh perbedaan fase dari clock, sehingga AVR 12 kali lebih cepat dibanding MCS51.

Berbagai karakteristik yang tersedia dalam IC ATmega8 adalah sebagai berikut:

- 8K bytes In-System Programable Flash
- 512 bytes EEPROM (*Electrical Erasable Programable Read Only Memory*)
- 512 bytes SRAM (*Static Random Access Memory*)
- 23 jalur I/O general-purpose
- 32 x 8 general-purpose working register
- Timer/Counter yang fleksibel dengan mode pembanding
- Interupsi internal dan eksternal
- Pemrograman serial UART (*Universal Asynchronous Receiver and Transmitter)*
- Serial Port SPI (*Serial Peripheral Interface*)

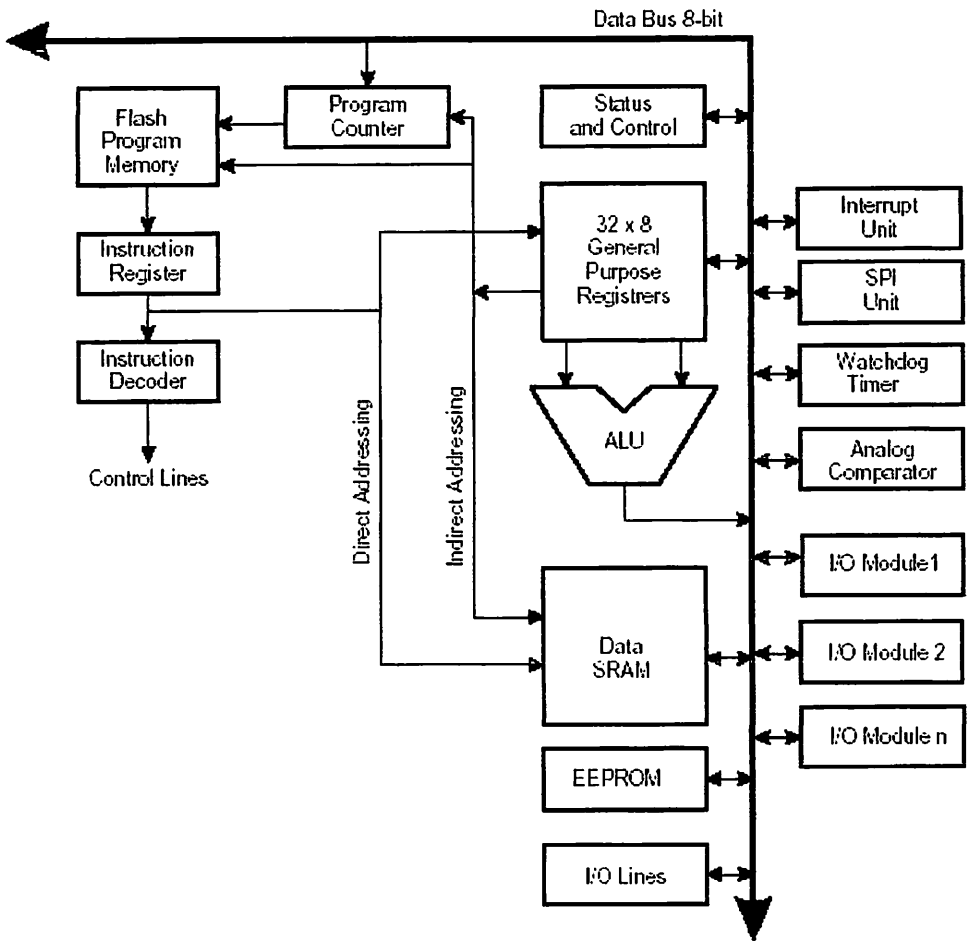
ATmega 8 mempunyai dua buah power-save mode yang dapat diatur melalui software, yaitu:

a. Idle Mode

   Menghentikan CPU sementara SRAM, Timer/ Counter, port SPI, dan sistem tetap berfungsi.

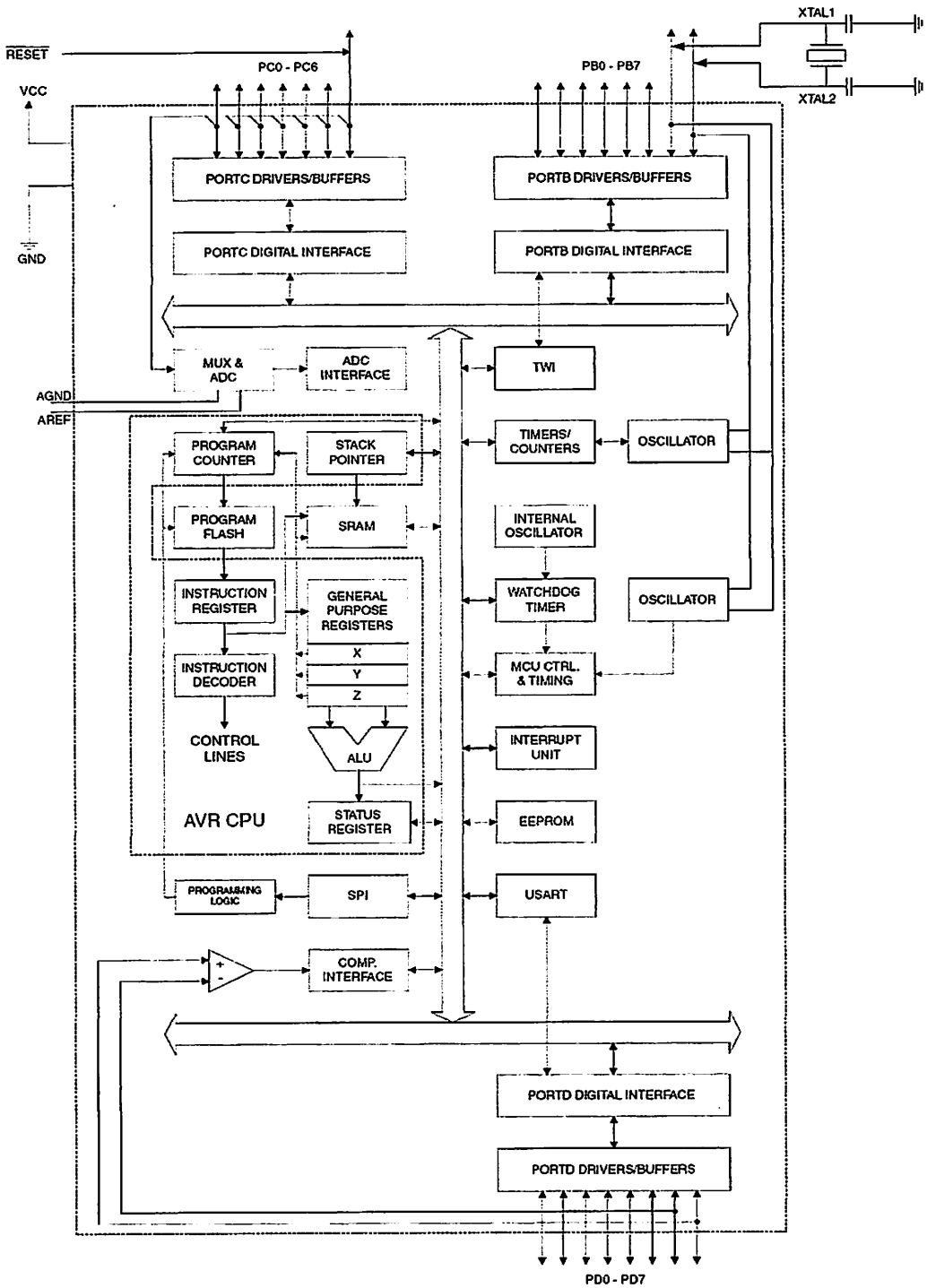
b. Power-Down Mode

   Menyimpan isi register dan menahan osilator untuk tidak mengaktifkan fungsi-fungsi chip yang lain sampai terjadi reset atau interupsi dari luar.



Gambar 2.2

Arsitektur AVR ATmega8[2]

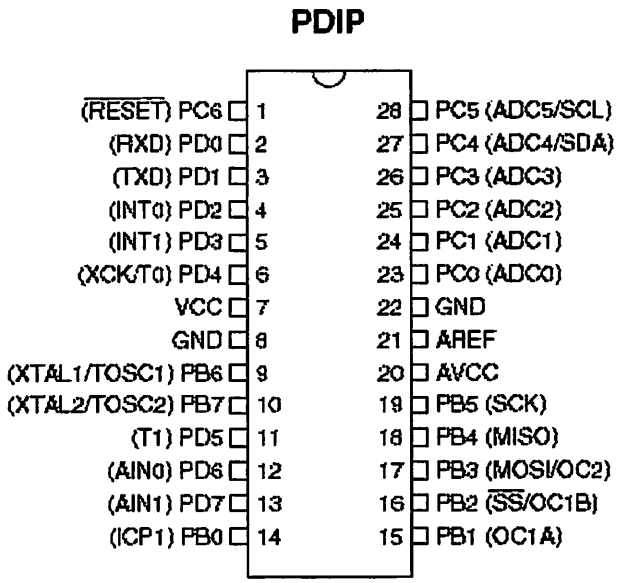


Gambar 2.3

Blok Diagram AVR ATmega8[2]

2.4.2. Konfigurasi Pin-Pin Mikrokontroller ATmega8

Mikrokontroller ATmega8 mempunyai 28 pin seperti pada gambar di bawah ini:



Gambar 2.4 Konfigurasi Pin ATmega8[2]

Fungsi tiap pin-nya adalah sebagai berikut:

a. Vcc: Tegangan Supply

b. Gnd: Ground

c. Port A (PA0-PA7): Port dua arah I/O 8-bit, kaki portnya dapat menyediakan resistor pull-up internal (dipilih untuk masing-masing bit). Port A juga dapat mengendalikan tampilan LED secara langsung.

d. Port B (PB0-PB7: Port dua arah I/O 8-bit dengan resistor pull-up internal, digunakan pada fungsi-fungsi khusus dari karakteristik ATmega8.

e. Port C (PC0-PC7): Port dua arah I/O 7-bit dengan resistor pull-up internal.

f. PC6/$\overline{\text{RESET}}$: Jika fuse RSTDISBL sudah diprogram, PC6 digunakan sebagai suatu pin I/O. Jika fuse RSTDISBL belum diprogram, PC6 digunakan sebagai

inputan Reset dimana level low dari pin ini lebih panjang dari pulsa minimum yang dihasilkan Reset.

g. Port D (PD0-PD7): Port dua arah /O 7-bit dengan resistor pull-up internal. Sebagai input, port D menggunakan eksternal pull low dengan sumber arus jika pull up resistor diaktifkan.

h. $\overline{\text{RESET}}$: Input reset. Level low-nya untuk lebih panjang dari pulsa minimum yang dihasilkan reset, meskipun clock tidak bekerja.

i. AV_{CC}: sebagai suplay tegangan untuk A/D converter port C (3..0), dan ADC (7..6). Pin ini harus dihubungkan dengan V_{CC} melalui low-pass filter.

j. AREF: Pin analog referensi untuk A/D converter.

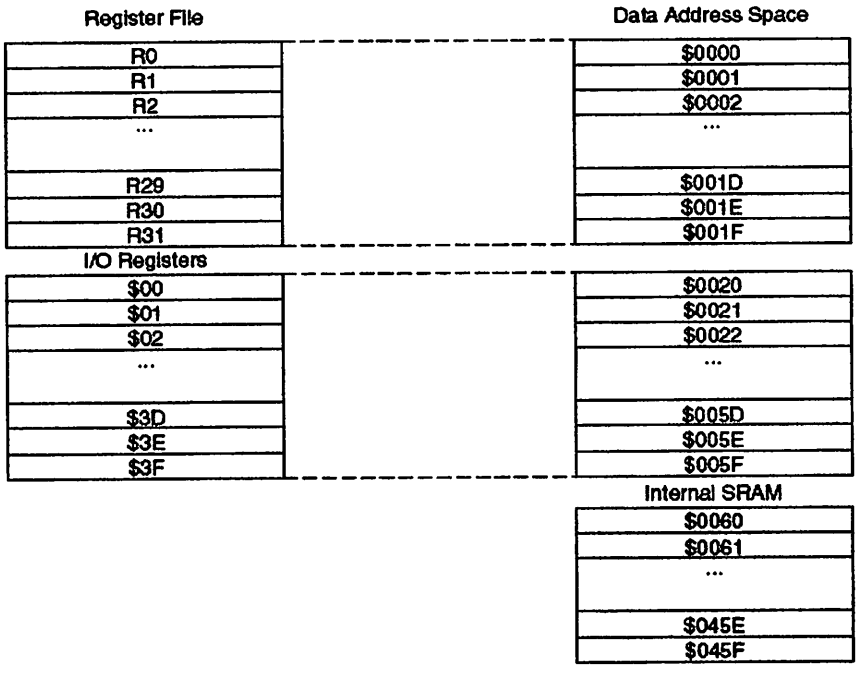
k. ADC 7..6 (TQFT and MLF): Pada TQFP dan MLP, ADC 7..6 bekerja sebagai input analog untuk A/D converter. Pin-pinnya mendapat daya dari power supplay analog dan dapat melayani 10 bit saluran ADC.

2.4.3 Peta Memori

AVR ATmega8 memiliki ruang pengalamatan memori data dan memori program yang terpisah. Memori data terbagi menjadi 3 bagian, yaitu 32 register umum, 64 buah register I/O, dan 1024 byte SRAM *Internal.*

Register keprluan umum menempati *space* data pada alamat terbawah, yaitu $00 sampai$1F. Sementara itu, register khusus unutk menangani I/O dan control terhadap mikrokontroler menempati 64 alamat berikutnya, yaitu mulai dari $20 hingga $5F. register tersebut merupakan register yang khusus digunakan untuk mengatur fungsi terhadap peripheral mikrokontroler, seperti control register, timer/ counter, fungsi-fungsi I/O, dan sebagainya. Alamat memori berikutnya digunakan untuk SRAM 1024 byte,

yaitu pada lokasi $60 sampai dengan $45F. Konfigurasi memori data ditunjukkan pada gambar dibawah ini.

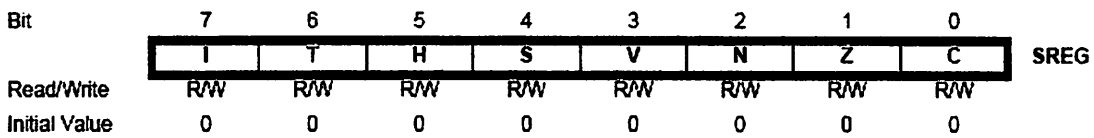


Gambar 2.5. Data Memory Map[2]

Memori program yang terletak dalam *Flash* System Reprogrammable Flash mempunyai 8K byte karena setiep instruksi memiliki lebar 16-bit atau 32-bit. AVR ATmega memiliki 4K byte x 16-bit *Flash* dengan alamat mulai dari $00 sampai $FFF. AVR tersebut memiliki 12-bit *Program Counter* sehingga mampu mengalamati isi *Flash.* Selain itu,AVR ATnega8 juga memiliki memory data berupa EEPROM 8-bit sebanyak 512 byte. Alamt EEPROM dimulai dari $000 sampai $1FF.

2.4.4. Status Register (SREG)

Status register adalah register berisis status yang dihasilkan pada setioap operasi yang dilakukan ketika suatu instruksi dieksekusi. SREG merupakan bagian dari inti CPU mikrokontroler.



Gambar 2.6. Status Register AVR ATmega8[2]

Keterangan dari bit SREG adalah:

a. Bit7 - I: *Global Interrupt Enable*

Bit harus diset untuk meng-enable interupsi. Setelah itu, baru dapat mengaktifkan interupsi mana yang akan digunakan dengan cara meng-enable bit control register yang bersangkutan secara individu. Bit akan di-clear apabila terjadi suatu interupsi, serta akan diset kembali oleh intruksi RETI.

b. Bit 6 – T: *Bit Copy Storage*

Intruksi BLD dan BST menggunakan bit-T sebagai sumber atau tujuan dalam operasi bit. Suatu bit dalam suatu register GPR dapat disalin ke bit T menggunakan instrusi BST, dan sebaliknya bit T dapat disalin kembali ke suatu bit dengan register GPR menggunakan instruksi BLD.

c. Bit 5 – H: *Half Carry Flag*

d. Bit 4 – S: *Sign* Bit, $S = N \oplus V$

Bit-S merupakan hasil operasi *EOR* antara *flag*-N (negative) dan *flag* V (komplemen dua *overflow*).

e. Bit 3 – V:*Two's Complement Overflow Flag*

Bit berguna untuk mendukung operasi aritmatika.

f. Bit 2 – N: Ne*gative Flag*

Apabila suatu operasi menghasilkan bilangan negative, maka *flag*-N akan diset.

g. Bit 1 – Z: *Zero Flag*

Bit akan diset bila hasil operasi yang diperoleh adlah nol.

h. Bit 0 – C: *Carry Flag*

Apabila suatu operasi menghasilkan *carry*, maka bit akan diset.

2.4.5. Register I/O

Semua port pada AVR memiliki kebenaran fungsional *read-modify-write* ketika digunakan sebagai port I/O umum. Ini berarti bahwa arah dari satu pin port dapat diubah tanpa bermaksud mengubah arah dari pin yang lain. Logika port I/O dapat diubah-ubah dalam program secara byte atau hanya bit tertentu. Mengubah sebuah keluaran bit I/O dapat dilakukan menggunakan perintah cbi (clear bit I/O) untuk menhasilkan output low dan perintah sbi (set bit I/O) untuk menghasilkan output haig. Pengubahan secara byte dilakukan dengan perintah in atu out yang menggunakan register bantu.

a. Port A

Tiga lokasi alamat memori I/O dilokasikan pada port A, masing-masing adalah register data-Port A, $1B ($3B), register data *direction* (register pengrah data)-DDRA, $1A ($3A), dan pin input port A-PIN A, $19 ($39). Pin-pin port A memiliki fungsi alternatif yang terhubung pada plihan data eksternal SRAM. Port A dapat dikonfigurasikan menjadi multiplexed low order alamat/data bus selama akses ke data memori eksternal. (blok diagram dapat dilihat pada lampiran).

I

b. Port B

Tiga lokasi alamat memori I/O yang dilokasikan pada port D, masing-masing adalah register data-PORTB, $18 ($38), register pengarah data-DDRB, $17 ($37), dan pin input port B-PINB, $16 ($36). (Blok diagram port B dan fungsi alternative pinnya dapat dilihat pada lampiran).

c. Port C

Tiga lokasi alamat memori I/O yang dilokasikan pada port C, masing-masing adalah register data-PORTC, $15 ($35), register pengarah data-DDRC, $14 ($34), dan pin input port C-PINC, $13 ($33). (Blok diagram skematik dapat dilihat pada lampiran).

d. Port D

Tiga lokasi alamat memori I/O yang dilokasikan pada port D, masing-masing adalah register data-PORTD, $12 ($32), register pengarah data-DDRD, $11 ($31), dan pin input port D-PIND, $10 ($30). (Blok diagram skematik port D dan fungsi alternatif pinnya dapat dilihat pada lampiran).

2.4.6. Osilator

Sumber clock dapat diatur dengan dua cara yaitu osilator internal dan osilator eksternal. Pengaturan osilator eksternal dilakukan dengan menambahan kristal keramik sesuai kebutuhan. Untuk osilator internal Atmega8 memiliki 4 nilai yaitu 1, 2, 4, 8 MHz. Penggunaan osilator internal menggunakan register OSCCAL, untuk 1 MHz alamat regiternya adalah 0X0000, untuk 2 MHz alamat regiternya adalah 0X0001, untuk 4 MHz alamat regiternya adalah 0X0002, untuk 8 MHz alamat regiternya adalah 0X0003

b. Port B

Tiga lokasi alamat memori I/O yang dilokasikan pada port D, masing-masing adalah register data-PORTB, $18 ($38), register pengarah data-DDRB, $17 ($37), dan pin input port B-PINB, $16 ($36). (Blok diagram port B dan fungsi alternative pinnya dapat dilihat pada lampiran).

c. Port C

Tiga lokasi alamat memori I/O yang dilokasikan pada port C, masing-masing adalah register data-PORTC, $15 ($35), register pengarah data-DDRC, $14 ($34), dan pin input port C-PINC, $13 ($33). (Blok diagram skematik dapat dilihat pada lampiran).

d. Port D

Tiga lokasi alamat memori I/O yang dilokasikan pada port D, masing-masing adalah register data-PORTD, $12 ($32), register pengarah data-DDRD, $11 ($31), dan pin input port D-PIND, $10 ($30). (Blok diagram skematik port D dan fungsi alternatif pinnya dapat dilihat pada lampiran).

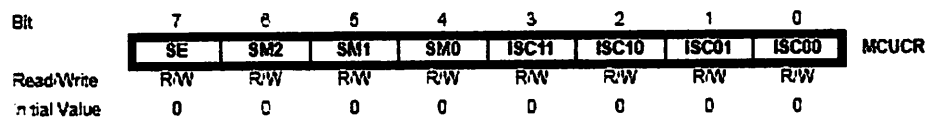
2.4.6. Oskilator

Sumber clock dapat diatur dengan dua cara yaitu oskilator internal dan oskilator eksternal. Pengaturan oskilator eksternal dilakukan dengan menambahkan kristal keramik sesuai kebutuhan. Untuk oskilator internal Atmega8 memiliki 4 nilai yaitu 1, 2, 4, 8 MHz. Penggunaan oskilator internal menggunakan register OSCCAL, untuk 1 MHz alamat registernya adalah 0X0000, untuk 2 MHz alamat registernya adalah 0X0001, untuk 4 MHz alamat registernya adalah 0X0002, untuk 8 MHz alamat registernya adalah 0X0003

2.4.7 Interupsi

Interupsi adalah kondisi yang membuat CPU berhenti dari rutinitas yang sedang dikerjakan (rutin utama) untuk mengerjakan rutin lain (rutin intrupsi). AVR ATMega8 memiliki 19 sumber interupsi.

a. Pada AVR terdapat 3 pin untuk interupsi eksternal, yaitu INT0, INT1 ,INT2. Interupsi eksternal dapat dibangkitkan apabila terdapat perubahan logika atau logika 0 pada pin interupsi. pengatuiran kondisi keadaan yang menyebabkan terjadinya interupsi eksternal diatur oleh register MCUCR(MCU Control Register). Yang terilihat pada tabel dibawah ini:



Gambar 2.7

Register MCUCR[2]

Bit penyusunya dapat dijelaskan sebagai berikut:

b. Bit ISC11 dan ISC10 bersama-sama menentukan kondisi yang dapat menyebabkan interupsi eksternal pada pin INT1.keadaan selengkapnya dapat dilihat pada tabel dibawah ini:

Tabel 2.1 beberapa setting kondisi yang menyebabkan interupsi eksternal I[2]

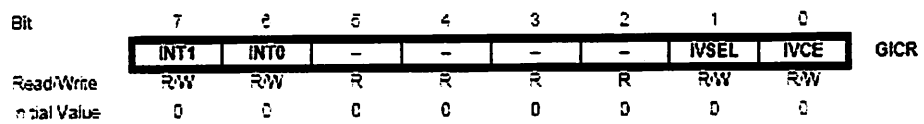
ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Any logical change on INT1 generates an interrupt request.
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.

c. Bit ISC01 dan ISC00 bersama-sama menentukan kondisi yang dapat menyebabkan interupsi eksternal pada pin INT0. keadaan selengkapnya dapat dilihat pada tabel dibawah ini:

Tabel 2.2 beberapa setting kondisi yang menyebabkan interupsi eksternal 0[2]

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Any logical change on INT0 generates an interrupt request.
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

Pemilihan pengaktifan interupsi eksternal diatur oleh register GICR (General Interupsi Control Register) yang terlihat seperti gambar berikut:



Gambar 2.8

General Interrupt Control Register[2]

Bit penyusun dapat dijelaskan sebagai berikut:

a. Bit INT1 adalah bit untuk mengaktifkan intrupsi ekternal 1. apabila bit tersebut diberi logika 1 dan bit-I pada SREG (stataus register) juga satu, maka interupsi eksternal 1 akan aktif.

b. Bit INT0 adalah bit untuk mengaktifkan intrupsi eksternal 0. apabiala bit tersebut diberi logika 1 dan bit-I pada SREG (status register) juga satu, maka interupsi eksternal 0 akan aktif.

c. Bit INT2 adalah bit untuk mengaktifkan interupsi ekternal 2 apabila bit tersebut diberi logika 1 dan bit-I pada SREG (status register) juga satu, maka ekternal 2 akan aktif.

Program interupsi dari masing-masing jenis interupsi eksternal akan dimulai dari vektor interupsi pada masing-masing jenis. Alamatnya dapat dilihat pada tabel:

Tabel 2.3 Macam Sumber Interupsi pada AVR Atmega8[2]

Vector No.	Program Address(2)	Source	Interrupt Definition
1	0x000(1)	RESET	External Pin, Power-on Reset, Brown-out Reset, and Watchdog Reset
2	0x001	INT0	External Interrupt Request 0
3	0x002	INT1	External Interrupt Request 1
4	0x003	TIMER2 COMP	Timer/Counter2 Compare Match
5	0x004	TIMER2 OVF	Timer/Counter2 Overflow
6	0x005	TIMER1 CAPT	Timer/Counter1 Capture Event
7	0x006	TIMER1 COMPA	Timer/Counter1 Compare Match A
8	0x007	TIMER1 COMPB	Timer/Counter1 Compare Match B
9	0x008	TIMER1 OVF	Timer/Counter1 Overflow
10	0x009	TIMER0 OVF	Timer/Counter0 Overflow
11	0x00A	SPI, STC	Serial Transfer Complete
12	0x00B	USART, RXC	USART, Rx Complete
13	0x00C	USART, UDRE	USART Data Register Empty
14	0x00D	USART, TXC	USART, Tx Complete
15	0x00E	ADC	ADC Conversion Complete
16	0x00F	EE_RDY	EEPROM Ready
17	0x010	ANA_COMP	Analog Comparator
18	0x011	TWI	Two-wire Serial Interface
19	0x012	SPM_RDY	Store Program Memory Ready

Untuk inisialiasasi awal interupsi, perlu dituliskan terlebih dahulu vektor interupsi dari interupsi yang terdapat pada sistem. Vektor interupsi adalah nilai yang disimpan ke *program counter* pada saat terjadi interupsi sehingga program akan menuju ke alamat yang ditunjukkan oleh *program counter*. alamat interupsi eksternal 0 pada alamat 001H

dan interupsi terima serial pada alamat 00B masing-masing alamat vektor memililki jarak yang berdekatan sehingga akan timbul masalah jika dperlukan rutin layanan interupsi yang panjang oleh sebab itu layanan interupsi ekternal 0 akan melompat ke alamat *ext_int0* dan inetrupsi terima serial pada alamat USART_RXC.

Pengaktifan interupsi eksternal dilakukan dengan memberikan logika satu pada register GICR. Dengan demikian, pada pengaktifan interupsi ekternal 0, akan diberikan logika satu pada bit ke 6 register GICR. pengaktifan interupsi terima serial dilakukan dengan memberikan logika 1 pada bit ke 7 register UCSRA. Terakhir, berikan perintah *sei* untuk menagaktifkan *global interupt.*

Interupsi dapat muncul kapan pun (kecuali jika bit *enable interupsi* dalam SREG *clear*) dengan demikian, interupsi juga dapat mencul ketika program sedang melakukan kalkulasi. Kalkulasi tersebut merubah flags dalam status register yang digunakan untuk *next step* dari kalkulasi atau untuk beberapa percabangan program. Jika ISR mengubah flags dalam SREG, maka kalkulasi yang sedang ditempatkan dalam program yang berjalan normal dapat di-corupt. Oleh sebab itu, perlu pengamanan SREG pada setiap subrutin interupsi.

2.4.8. Timer/Counter 2

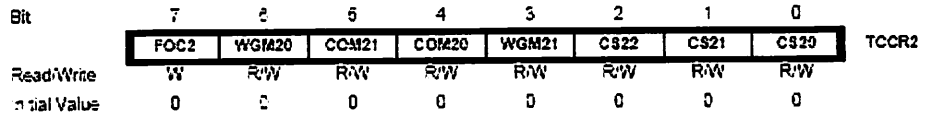
Timer/counter 2 adalah 8 bit Timer/Counter yang multifungsi. Deskripsi untuk Timer/Conuter 2 pada ATMega8 adalah sebagai berikut:

a. Sebagai Counter 1 kanal
b. Timer dinolkan saat *match compare (auto reload)*
c. Dapat menghasilkan gelombannng PWM dengan *glitch-free*
d. Frekuensi generator

e. Prescaler 10 bit untuk timer

f. Ineterupsi timer yang disebabakan timer *averflow* dan *match compare*

Pengaturan timer/counter 2 diatur oleh TCCR2 (Timer/Conuter control register 0) yang dapat dilihat pada gambar berikut:



Gambar 2.9

Register TCCR2[2]

Penjelasan untuk tiap bit adalah:

a. Bit 7 – FOC2 : Force Output Compare

b. Bit 6,3 – WGM21 : WGM20: Waveform genertion unit

Bit tersebut mengontrol kenaikan counter, sumber dari nilai maksimum counter, dan tipe dari jenis Timer/Counter yang dihasilkan, yaitu mode normal, clear timer mode compare match, dan dua tipe dari PWM (Pulse Width Modulation) berikut tabel setting pada bit untuk menghailkan mode tertentu:

Tabel 2.4 Konfigurasi Bit WGM21 dan WGM20[2]

Mode	WGM21 (CTC2)	WGM20 (PWM2)	Timer/Counter Mode of Operation[1]	TOP	Update of OCR2	TOV2 Flag Set
0	0	0	Normal	0xFF	Immediate	MAX
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	1	0	CTC	OCR2	Immediate	MAX
3	1	1	Fast PWM	0xFF	TOP	MAX

c. Bit 5,4 – COM01:COM00:Compare Match Output Mode

Bit mengontrol pin OC0(Output Compare pin) apalagi kedua bit tersebut nol atua clear, maka pin OC0 berfungsi sebagai pin biasa namun, jika salah satu bit set,

maka fungsi pin tergantung pada setting bit pada WGM00 dan WGM01 berikut daftar tabel setting bit sesuai setting pada WGM00 adan WGM01.

Tabel 2.5 Konfigurasi Bit COM21 dan COM20 Compare Output Mode non PWM[3]

COM21	COM20	Description
0	0	Normal port operation, OC2 disconnected.
0	1	Toggle OC2 on Compare Match
1	0	Clear OC2 on Compare Match
1	1	Set OC2 on Compare Match

Tabel 2.6 Konfigurasi Bit COM21 dan COM20 Compare Output Mode fast PWM[2]

COM21	COM20	Description
0	0	Normal port operation, OC2 disconnected.
0	1	Reserved
1	0	Clear OC2 on Compare Match, set OC2 at TOP
1	1	Set OC2 on Compare Match, clear OC2 at TOP

Tabel 2.7 Konfigurasi Bit COM21 dan COM20 Compare Output Mode Phase Correct PWM[2]

COM21	COM20	Description
0	0	Normal port operation, OC2 disconnected.
0	1	Reserved
1	0	Clear OC2 on Compare Match when up-counting. Set OC2 on Compare Match when downcounting.
1	1	Set OC2 on Compare Match when up-counting. Clear OC2 on Compare Match when downcounting.

d. Bit 2, 1, 0-CS22;CS21,CS20 : Clock Select

Ketiga bit tersebut memillih sumber clock yang akan digunakan oleh timer/counter Berikut list tabelnya:

Tabel 2.8 Konfigurasi Bit Clock Select untuk Memilih Sumber Clock[2]

CS22	CS21	CS20	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	clk_{T2S}/(No prescaling)
0	1	0	clk_{T2S}/8 (From prescaler)
0	1	1	clk_{T2S}/32 (From prescaler)
1	0	0	clk_{T2S}/64 (From prescaler)
1	0	1	clk_{T2S}/128 (From prescaler)
1	1	0	clk_{T2S}/256 (From prescaler)
1	1	1	clk_{T2S}/1024 (From prescaler)

2.3.9. Register TIMSK

Selain register di atas terdapat pula register TIMSK (Timer/Counter Interrupt Mask Register).

Bit	7	6	5	4	3	2	1	0	
	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	–	TOIE0	TIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Gambar 2.10. Register TIMSK[2]

Penjelasan Untuk setiap bit adalah:

a. Bit 0 – TOIE0: Timer/Counter 0 Overflow Interrup Enable

   Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka dilakukan enable interupsi Overflow Timer/Counter 0.

b. Bit 1 – OCIE0: Timer/Counter 0, Output Compare Match Interrupt Enable

   Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka bias dilakukan enable interupsi Output Compare Match Timer/Counter 0.

c. Bit 2 – TOIE1: Timer/Counter 1 Overflow Interrup Enable

   Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka dilakukan enable interupsi Overflow Timer/Counter 1.

d. Bit 3 – OCIE1B: Timer/Counter 1, Output Compare B Match Interrupt Enable

Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka dilakukan enable interupsi Overflow Compare Match B Timer/Counter 1.

e. Bit 4 – OCIE1A: Timer/Counter 1, Output Compare A Match Interrupt Enable

Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka dilakukan enable interupsi Overflow Compare Match A Timer/Counter 1.

f. Bit 5 – TICIE1: Timer/Counter 1 Input Capture Interrupt Enable

g. Bit 6 – TOIE2: Timer/Counter 2, Overflow Interrupt Enable

Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka dilakukan enable interupsi Overflow Timer/Counter 2.

h. Bit 7 – OCIE2: Timer/Counter 2, Output Compare Match Interurpt Enable

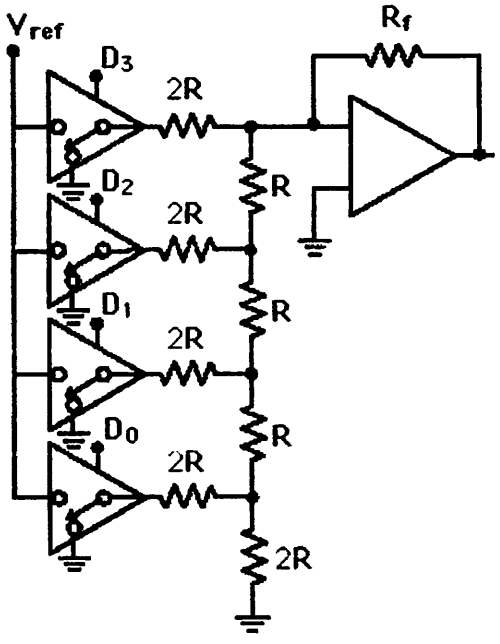
Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka bias dilakukan enable interupsi Output Compare Match Timer/Counter 2.

2.5. Digital To Analog Converter (DAC)

Keluaran-keluaran yang berbentuk sinyal analog dari suatu system computer dapat diperoleh dengan menggunakan converter digital ke analog, yang luas dikenal dengan istilah DAC *(Digital to Analoque Converter)*. DAC akan mengkonversi sebuah sinyal digital menjadi bentuk sinyal analog.

Salah satu susunan rangkaian *converter* digital ke analog adalah DAC dengan pembobotan biner (R-2R). dalam implementasi pembobotan biner kedua, hanya dua nilai resistor yang berbeda yang digunakan untuk memperoleh arus-arus pembobotan biner. Seperti tampak pada gambar 2.10 implementasi DAC pembobotan biner dapat dilakukan dengan menggunakan rangkaian R-2R bersama-sama dengan sebuah komponen penguat dan saklar CMOS. bergantung pada posisi saklar CMOS, arus-arus pembobotan biner

dapat mengalir ke resistor umpan balik atau ke terminal *ground.* arus yang mengalir ke resistor umpan balik akan berkontriibusi pada tegangan keluaran rangkaian.



Gambar 2.11. Rangkaian R-2R[3]

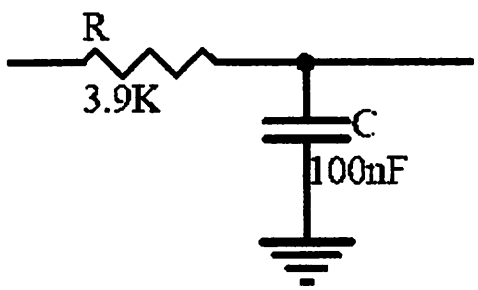
Nilai-nilai bit dari sinyal digital akan menentukan posisi saklar. sebuah logika yang bernilai 1 pada bit yang paling signifikan akan mengakibatkan saklar CMOS yang berkorespondensi, d_4, terhubung ke terminal masukan pembalik buffer. arus $V_{ref}/2$ akan mengalir ke titik penjumlahan buffer yang akan membangkitkan sebuah tegangan keluaran. logika yang bernilai 1 pada bit yang paling signifikan berikutnya akan mengoperasikan saklar CMOS d_3 dan mengakibatkan arus $V_{ref}/4R$ mengalir menuju ke titik penjumlahan buffer. dengan demikian besar arus yang mengalir akan bernilai setengah untuk setiap nilai biner bit yang bernilai setengah dari nilai sebelumnya, sehingga tegangan keluaran rangkaian akan berbanding lurus terhadap nilai sinyal digital.

Keuntungan dari rangkaian R-2R adalah hanya memerlukan dua nilai resistor. pencapaian kondisi matching di antara sejumlah resistor yang memiliki nilai R dan 2R akan lebih mudah.

2.6. Filter

Filter (tapis atau penyaring) didefinisikan sebagai rangkaian listrik yang dirancang untuk melewatkan atau meloloskan arus bolak-balik yang dibangkitkan pada frekuensi tertentu serta memperlemah semua arus bolak-balik yang dibangkitkan dengan frekuensi-frekuensi yang lain. (*George Clayton dan Steve Winder, 250*).

Suatu rangkaian filter LPF*(Low Passs Filter)* sederhana yang terdiri dari komponen kapasitor (C) dan resistor (R). Rangkaian diatas pada intinya merupakan sebuah rangkaian pembagi tegangan yang terdiri atas sebuah komponen resistif (resistor) yang terhubung secara seri dengan sebuah kapasitor.



Gambar 2.12. Rangkain Low Pass Filter[4]

tegangan keluaran rangkaian, e_o, diambil pada titik ujung dari komponen kapasitor. tegangan keluaran ini berelasi dengan tegangan masukan, e_i, sesuai persamaan:

$e_o = -jX_c\, e_i/(R-jX_c)$

Persamaan bilangan kompleks di atas memperlihatkan bahwa amplitude tegangan keluaran, e_o, dapat dinyatakan dalam persamaan:

$$|e_1| = \frac{e_i X_c}{\left(\sqrt{R^2 + X_c^{\,2}}\right)}$$

Meskipun tegangan masukan , e_i, dapat dijaga konstan sepanjang kisaran dari frekuensi-frekuensi masukan, *amplitude* tegangan keluaran, e_o, akan tetap berkurang jika frekuensi sinyal masukan bertambah. Hal ini terjadi oleh karena *reaktansi kapasitif kapasitor* $X_c = 1/2\pi fC$, bervariasi secara berkebalikan terhadap frekuensi, f, serta memiliki kecenderungan untuk bernilai tak terhingga pada frekuensi yang sama dengan nol dan bernilai nol pada frekuensi yang sangat tinggi (tak terhingga). dengan demikian pada frekuensi-frekuensi yang sangat tinggi, secara efektif tidak akan terdapat tegangan keluaran rangkaian.

Pada frekuensi-frekuensi rendah *rasio voltase* keluaran terhadap *voltase* masukan tetap berada level yang konstan hingga mencapai frekuensi f_c. frekuensi ini dikenal sebagai frekuensi *cutt-off* yaitu frekuensi di mana *reaktansi kapasitor* memiliki *magnitude* yang sama dengan *resisitansi* rangkaian, yang dirumuskan oleh persamaan:

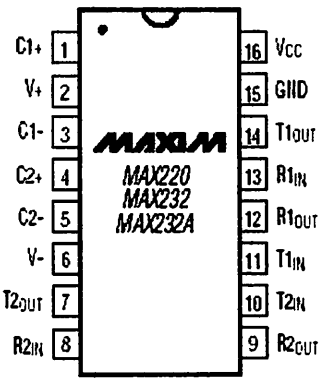
$$f_c = \frac{1}{2\pi RC} Hz$$

Untuk frekuensi-frekuensi yang lebih rendah dari f_c, gain rangkaian adalah konstan dan pada frekuensi-frekuensi yang lebih besar daripada f_c, *gain* rangkaian dapat dianggap sangat rendah sehingga sinyal-sinyal dengan frekuensi ini akan diredam oleh rangkaian.

2.7 Komunikasi Serial

Untuk mengirimkan kode ASCII dari PC (*Personal Computer*) dan untuk menerima data dari demodulator, digunakan port serial RS-232, dimana pada port ini terdapat fungsi-fungsi untuk Tx (pengiriman data), Rx (penerimaan data) dan TX/RX (pemilihan mode Tx atau Rx). Untuk melakukan *transfer* kode ASCII dari PC ke mikrokontroler

digunakan IC MAX232, yang merupakan rangkaian terpadu untuk antarmuka komunikasi serial.



Gambar 2-13
RS 232 (MAXIM) [5]

RS MAX232 tersusun dari 2 bagian yaitu *RS232 Line Driver* yang berfungsi mengubah level tegangan TTL ke level tegangan RS232 dan *RS232 Line Receiver* yang berfungsi mengubah level tegangan RS232 ke level tagangan TTL.

Alat ini merupakan standart yang dipakai untuk mengirimkan aliran bit seri antar *interface*. Komunikasi serial dapat dibagi menjadi dua sifat dasar pola komunikasi. Yang pertama adalah komunikasi asinkron, dimana pola-pola bit tertentu dipakai untuk memisahkan bit-bit karakter. yang kedua adalah komunikasi seri *sinkron,* yang memungkinkan karakter dikirim secara berurutan, namun membutuhkan karakter *sinkronisasi* khusus pada awal setiap karakter dan karakter semua khusus untuk dikirimkan ketika tidak ada informasi yang sedang dikirim.

2.7.1 Protokol Komunikasi pada RS 232

Beberapa protokol dalam interface RS 232 adalah:

- Start Bit

  Merupakan sebuah bit dengan logic "0" dimana bit ini yang menandakan bahwa akan ada karakter atau data yang mengikutinya. Bit ini langsung diberikan oleh sinyal device tanpa harus mensetnya terlebih dahulu.

- Data Bit

  Merupakan bit yang mewakili dari karakter yang diikutinya *data bit* ini dapat diset sepanjang antara 5 sampai 8 bit.

- Pariti Bit

  Merupakan bit yang digunakan sebagai *error checking* pada *receiver* , apabila terjadi kesalahan maka *receiver* akan menset *error flag* (parity error) pada special register. *Parity bit* ini menghitung jumlah data yang berlogic '1' pada data bit. Perhitungan jumlah data bit tersebut tergantung dari jenis *parity* yang diset. Untuk parity *EVEN* maka jumlah data bit yang berlogic '1' ditambah dengan *parity bit* akan menghasilkan jumlah yang ganjil. Sedangkan untuk *parity MARK* merupakan *parity bit* selalu berlogic '1' begitu pula pada space, parity bit selalu berlogic ' 0' dan *parity NONE* disini *parity bit* yang diabaikan.

- Stop Bit

  Merupakan bit yang menandakan akhir dari suatu paket data (biasanya 1 byte data). Seperti pada start bit, bit ini langsung diberikan dari serial device. *Stop bit* ini dapat diset panjangnya menjadi satu bit, satu setengah dan dua bit.

- Baut Rate

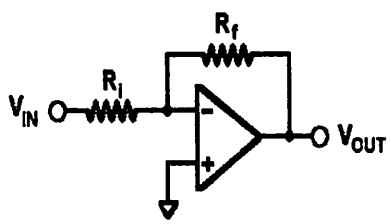
  Sebenarnya *baut rate* berarti pergantian kondisi tiap detik *(State Change of the Line persecond),* tetapi karena hanya ada 2 kondisi pada serial *(logic* 0 *dan 1)*

maka dapat juga digunakan untuk menunjukkan kecepatan dari transmisi *(bits per second).*

- Tx Buffer : berfungsi menampung dan menyimpan data yang akan dikirim keluar. Data ini dikirim oleh CPU ke Tx Buffer setelah memastikan diperolehkannya melakukan pengiriman.
- Rx Buffer : berfungsi menampung dan menyimpan data yang akan diterima. Data yang akan diterima lebih dahulu ditampung dalam Rx Buffer.

2.8 Op Amp Inverting

Pada penguat inverting tegangan input diberikan pada tegangan terminal input negatif sedangakan terminal positifnya dihubungkan dengan ground dasra gamabar inverting diperlihatkan pada gambar berikut



Gambar 2.14

Rangkaian Op Amp Inverting[6]

Teganagn keluaran (Vout) pada penguat tak membalik dapat diperhitungkan dengan persamaan sebagai beriikut:

$$Vout = \left(1 + \frac{Rf}{Rin}\right) Vin$$

Sedangakan penguatanya dapat diperoleh dengan persammaan di bawah ini:

$$A = \frac{Vout}{Vin}$$

$$A = \frac{\left(1 + \frac{Rf}{Rin}\right) Vin}{Vin}$$

$$A = \left(1 + \frac{Rf}{Rin}\right)$$

2.9 MT8841

MT8841 adalah sebuah IC CMOS dengan devais yang kompatibel dimana fungsinya adalah untuk mendemodulasikan sinyal FSK ke bentuk kode biner.

Gambar IC-nya adalah sebagai berikut:

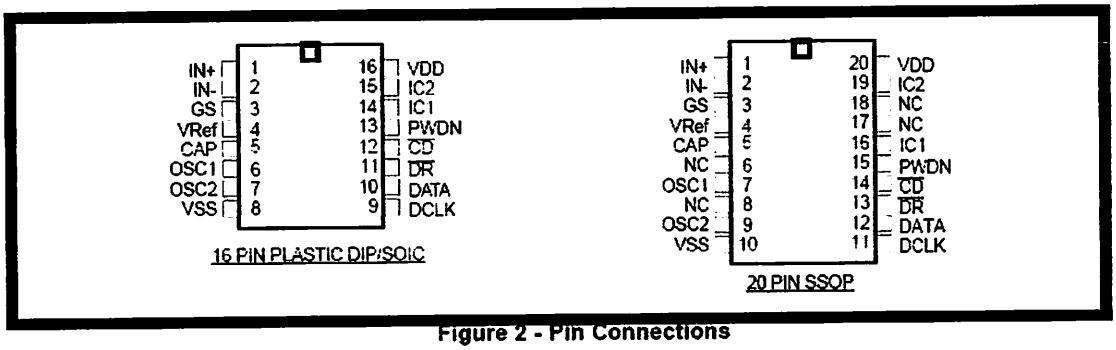


Figure 2 - Pin Connections

Gambar 2.15

Konfigurasi Pin MT8841[7]

Berbagai karakteristik yang tersedia dalam IC MT8841 adalah sebagai berikut:

- 1200 baud BELL 202 demodulasi *Frequency Shift Keying* (FSK)
- Sensitvitas input tinggi: -36dBm
- *Mode power down*
- Penguatan internal amplifier yang dapat disetel
- Memakai resonator crystal atau ceramic 3.579545 MHz
- *Single* 5V power supply

- *Low power CMOS technology*

MT8841 menyediakan sebuah data ready signal untuk mengindukasikan penerimaan setiap karakter 8-bit yang dikirim dari modulator.

Deskripsi Pin :

- IN+ : *Non-inverting Op-Amp (Input).*sinyal masuk melalui kaki ini apabila tidak diperlukan pembalikan fasa.
- IN- : *Inverting Op-Amp (Input).*sinyal masuk melalui kaki ini apabila diperlukan pembalikan fasa.
- GS : *Gain Select (Output).*memberikan akses ke *output op-amp* untuk koneksi resistor *feedback.*atau sebagai pemilihan penguatan sinyal apabila memerlukan penguatan maka diperlukan sebuah resistor yang dihubungkan ke kaki ini.
- Vref : *Voltage Reference (Output).*tegasngan referensi,nominalnya VDD/2 dipakai untuk mengarahkan input op-amp/sebagai bias input.
- CAP : *Capacitor.*sebagai kaki yang dihubungkan kapasitor 0.1uF ke VSS.
- OSC1 : *Oscillator (Input).*koneksi resonator Crystal atau ceramic sebesar 3,759545MHZ.pin ini dapat dikendalikan langsung dari sumber *clock eksternal.*
- OSC2 : *Oscillator (Output).*koneksi resonator Crystal atau ceramic. Saat OSC1 dikendalikan oleh *clock eksternal,* pin ini dibiarkan terbuka.
- VSS : *Power supply ground.*
- DATA : *Data (Output).*serial data output menyesuaikan dengan input dan *switching* FSK pada *input baud rate.*frekuensi tanda pada input sesuai dengan

logika *high,* sementara frekuensi *delay* sesuai dengan logia *low* pada DATA output. dengan tidak adanya input FSK, DATA berlogika *high.output* ini bertahan sampai CD(*Carrier Detect)* aktif.

- DR : *Data Ready (Open Drain Output). Output* ini menjadi *low* setelah pulsa DCLK terakhir tiap *word.* Ini dapat digunakan untuk mengidentifikasi batasan data (8-bit word) pada serial *output stream.* Secara khusus, DR digunakan untuk menghalangi kedelapan data bit dari *serial-to-parallel converter* kedalam sebuah microcontroller.
- CD : *Carrier Detect (Open Drain Output).*sebuah logika low mengindentasikan bahwa sebuah data telah diberikan untuk waktu tertentu pada line. Sebuah *hysteresis* waktu disediakan untuk membolehkan *diskontinyu data* sesaat.
- IC1 : *Internal Connection 1.* hubungkan ke VSS.
- VDD : *positive power supply voltage.*

BAB III

PERANCANGAN DAN PEMBUATAN ALAT

3.1. Pendahuluan

Dalam bab II telah dijelaskan bahwa Modulator FSK dengan menggunakan Metode DDS mempunyai spesifikasi frekuensi yang telah ditentukan. Oleh sebab itu setiap peralatan tambahan pada sistem DDS harus mengikuti spesifikasi yang telah ditentukan. Bab ini membahas tentang aplikasi mikrokontroler ATmega8 sebagai alat memproses data-data masukan dan mengolahnya untuk dijadikan proses pada keluaran sesuai dengan perencanaan program(sebagai Sebagai pengolah data). Aplikasi tersebut meliputi spesifikasi alat, dan blok-blok rangkaian penyusun sistem

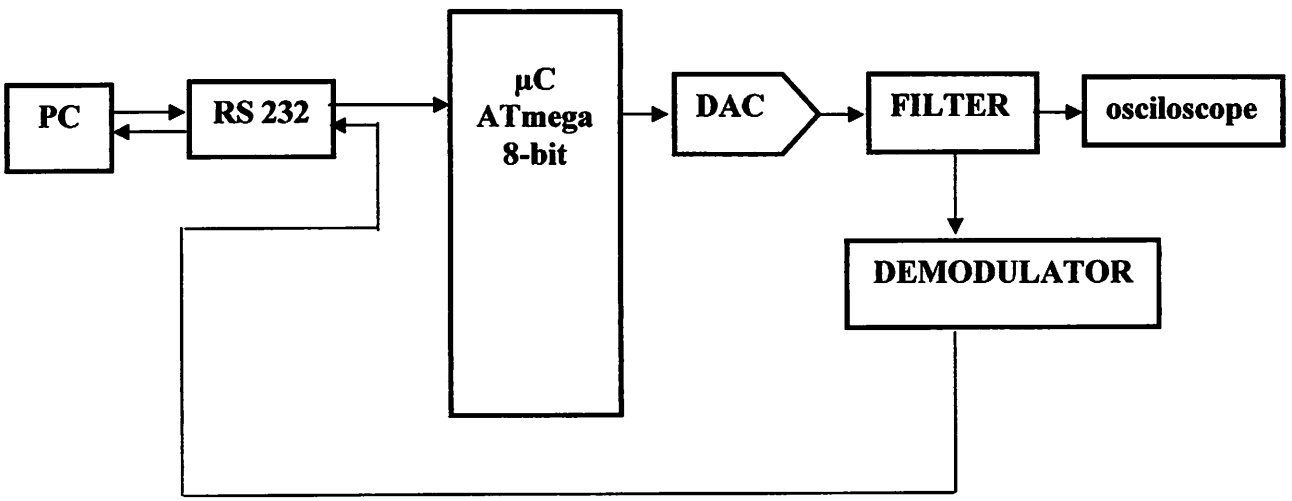
Spesifikasi rangkaian secara global ditetapkan terlebih dahulu untuk acuan dalam perencanaan selanjutnya. Spesifikasi yang direncanakan adalah sebagai berikut:

- Digunakan sebagai Modulator FSK dengan menggunakan sistem DDS
- Menggunakan mikrokontroler ATMEL AVR ATmega8 sebagai pengolah utama
- Menggunakan IC MT8841 buatan MITEL sebagai demodulator

Sistem alat terdiri atas mikrokontroler ATmega8 dan komponen pendukung seperti Komunikasi Serial,DAC (Digital to Analog Converter), Filter dan Demodulator.

3.2. Perancangan Perangkat Keras

Diagram blok rangkaian Metode Direct Digital Synthesis (DDS) Modulator FSK yang direncanakan ditunjukkan dalam Gambar 3.1



Gambar 3.1

Blok Diagram Metode Direct Digital Synthesis (DDS) Modulator FSK

Sistem piranti yang akan direalisasikan mempunyai blok diagram seperti terlihat pada gambar 3.1 di atas.

Fungsi dari masing-masing rangkaian subsistem dalam gambar di atas adalah sebagai berikut:

- Mikrokontroler ATmega8 sebagai pengendali utama, akan direalisasikan dengan menggunakan perangkat lunak sesuai dengan bahasa pemrograman pada AVR ATmega8.
- DAC R-2R(Digital to Analog Converter)

  Berfungsi untuk mengubah sinyal digital dari output mikrokontroller menjadi output analog berupa tegangan.

- Filter LPF(Low Pass Filter)

  Berfungsi untuk memfilter signal outputan dari DAC R-2R, agar output yang dihasilkan sesuai dengan yang diinginkan.

- keyboard

  Berfungsi sebagai pemberi inputan data ke Mikrokontroler berupa inputan kode bentuk hekhza yang kemudian di konversi ke bentuk biner dimana 0 mewakili frekuensi pada nilai f1=1200HZ dan 1 mewakili frekuensi pada nilai f2=2200HZ.

- Demodulator MT8841

  Berfungsi sebagai Dekoder yang akan mengkodekan data yang dikirim dari PC.

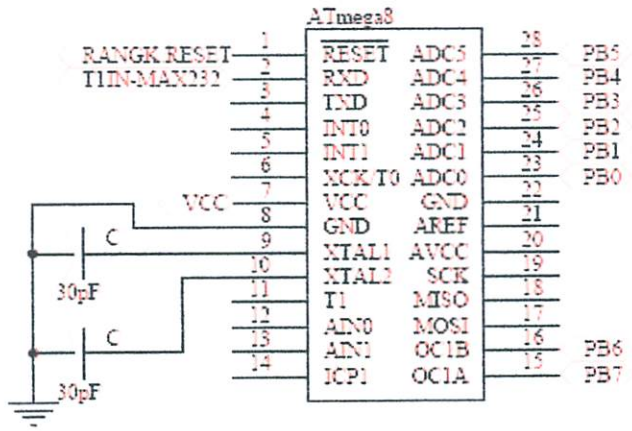
- RS 232

  Berfungsi sebagai komunikasi serial untuk mengirimkan kode ASCII dari PC (*Personal Computer*) dan untuk menerima data dari Demodulator.

3.2.1. Perancangan Rangkaian Mikrokontroler ATmega8

3.2.1.1. Sistem Minimum ATmega8

Pada rangkaian ini komponen utamanya adalah unit Mikrokontroler ATmega8. Komponen ini merupakan sebuah *chip* tunggal sebagai pengolah data dan pengontrolan alat. Sebagai pengolah data dan pengontrolan sistem, pin-pin mikrokontroler ATmega8 dihubungkan pada rangkaian pendukung membentuk suatu *minimum* sistem, yang ditunjukkan pada Gambar 3.2 di bawah ini:

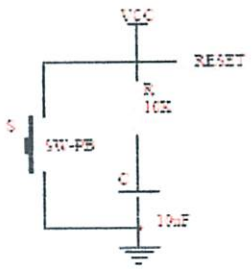


Gambar 3.2

Minimum Sistem Mikrokontroler ATmega8

3.2.1.2. Perancangan Rangkaian Reset

Untuk melakukan reset sistem pada mikrokontroler Atmega8 dapat memanfaatkan pin reset. Pin tersebut dihubungkan dengan rangkaian reset eksternal yang ditunjukkan Gambar 3.4 di bawah ini:



Gambar 3.3

Perancangan Rangkaian Reset ATmega8

Untuk membangkitkan sinyal *reset* kapasitor dihubungkan dengan V_{CC} dan sebuah resistor yang dihubungkan ke *ground.*

Sesuai dengan data sheet Atmega8 telah dicantumkan bahwa $t_{reset(min)}$ adalah sebesar 1,5 µs.

3.2.2. Perancangan Rangkaian Komunikasi Serial RS232

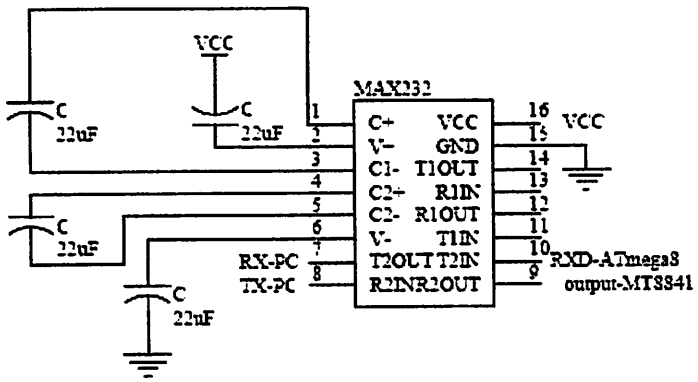
Sebelum diinputkan ke PC dibutuhkan rangkaian converter tegangan. Mikrokontroller mempunyai output logika high dihasilkan dari tegangan 5 volt dan logika low sebesar 0 volt, tegangan ini akan sering mengakibatkan terjadinya kesalahan didalam pengiriman data dikarenakan rugi-rugi dari kabel. RS 232 berfungsi untuk memperlebar range tegangan karena berada dikisaran +10V dan -10V, dengan range yang lebar ini kesalahan karena rugi-rugi sistem komunikasi dari PC ke mikrokontroller tidak mempengaruhi nilai data yang dikirim.

Pada proses penerimaan data pada perancangan alat digunakan RS 232 sebagai penghubung antara PC dengan Demodulator MT8841. ini berfungsi untuk mengurangi terjadinya kesalahan pada proses penerimaan data, dikarenakan rugi-rugi dari kabel. RS 232 berfungsi untuk memperlebar range tegangan karena berada dikisaran +10V dan -10V setelah MT8841 menerima masukan data, maka data yang dibaca akan dikirim ke RS232 untuk ditampilkan sebagai tampilan visual pada PC.

Untuk koneksi ke PC digunakan DB9, dimana pin 5 dihubungkan dengan ground, pin 2 dan pin 3 dihubungkan dengan relay yang akan memilih data yang diterima dari Demodulator atau data yang akan dikirim ke PC.

Rangkaian komunikasi serial MAX232 yang gambar lengkapnya dapat dilihat pada Gambar 3.5, berfungsi sebagai komunikasi serial untuk mengirimkan kode ASCII dari PC (*Personal Computer*) dan untuk menerima data dari Demodulator.

Rangkaian komunikasi serial MAX232 ditunjukkan dalam Gambar 3.5 ini.



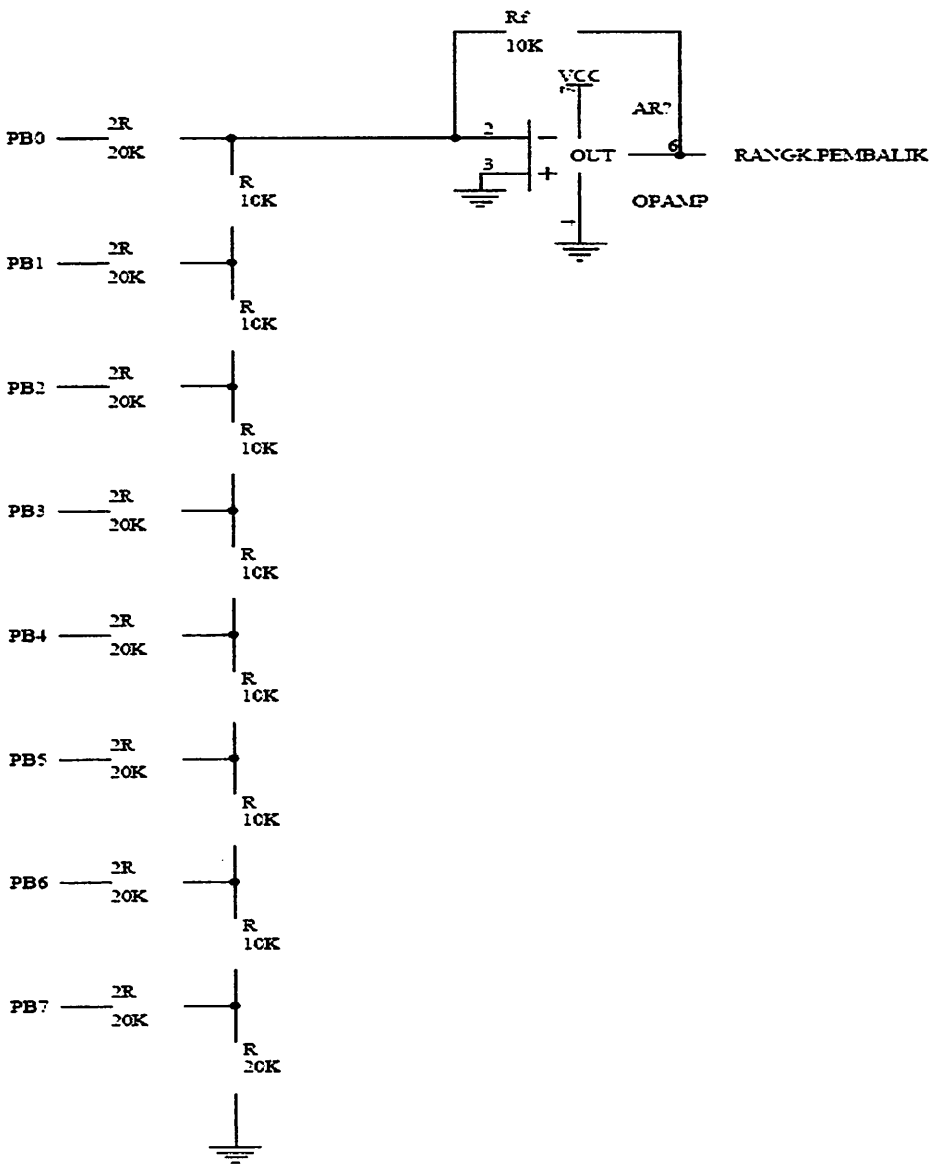
Gambar 3.4

Rangkaian RS232 Komunikasi Serial

Komponen utama rangkaian komunikasi serial ini adalah IC MAX232 dan beberapa komponen pendukung. Untuk memperlebar range tegangan karena berada dikisaran +10V dan -10V, dengan range yang lebar ini kesalahan karena rugi-rugi sistem komunikasi tidak mempengaruhi nilai data yang dikirim.

3.2.3. Perancangan Rangkaian DAC(Digital/Analog Converter)

Rangkaian DAC *(Digital/Analog Converter)* berfungsi untuk mengubah sinyal digital dari output mikrokontroller menjadi output analog berupa tegangan. DAC R-2R Ladder.



Gambar 3.5

Rangkaian DAC (Digital/Analog Converter)

Adapun Rangkaian DAC R-2R ditunjukkan dalam Gambar 3.6 di atas. dengan nilai komponen R=10K dan 2R=20K.

3.2.4. Perancangan Rangkaian Filter (LPF)

Sinyal yang keluar dari DAC di teruskan ke filter LPF*(Low Pass Filter).* LPF ini berfungsi untuk memperhalus bentuk gelombang sinus keluaran

DAC.nilai komponen R dan C pada frekuensi cutt off dapat ditentukan dengan rumus:

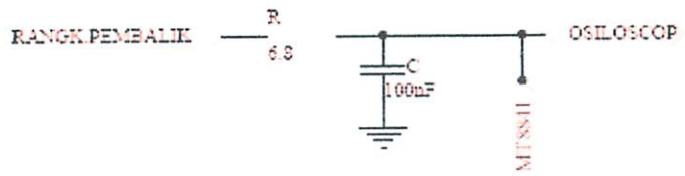
$$Fc = \frac{1}{2\pi RC}$$

$$2200 = \frac{1}{2\pi * R * 100nF}$$

$$R = 7{,}2\Omega$$

R yang digunakan adalah nilai yang mandekati dan tersedia di pasaran yaitu $6{,}8\,\Omega$.

Rangkaian Filter ditunjukkan dalam Gambar 3.7 di bawah ini.



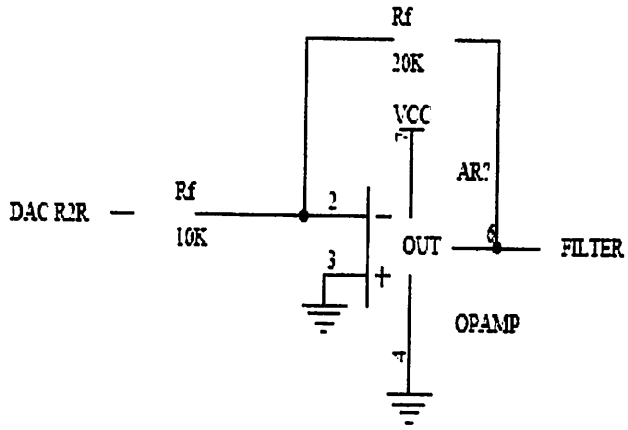
Gambar 3.6

Rangkaian Filter(Low Pass Filter)

3.2.5. Perancangan Rangkaian Op Amp

Digunakan Op Amp inverting sebagai pembalik sinyal keluaran dari DAC dengan penguatan sebesar 1x dimana digunakan feedback Rf =R=10k.

Gambar rangkaian Op Amp Inverting seperti tampak di bawah ini.

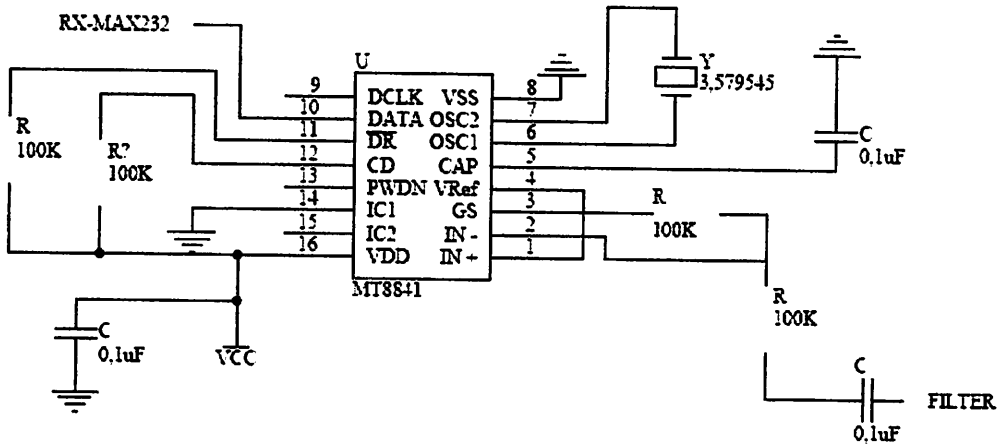


Gambar 3.7

Rangkaian Op Amp Inverting

3.2.6. Perancangan Rangkaian Demodulator MT8841

Rangkaian demodulator ini digunakan IC MT8841 buatan MITEL untuk mendemodulasikan sinyal FSK ke bentuk kode biner



Gambar 3.8

Rangkaian Demodulator MT8841

Pada input rangkaian diatas dihubungkan langsung dengan modulator FSK karena inputnya adalah kode yang sudah termodulasi bentuk FSK

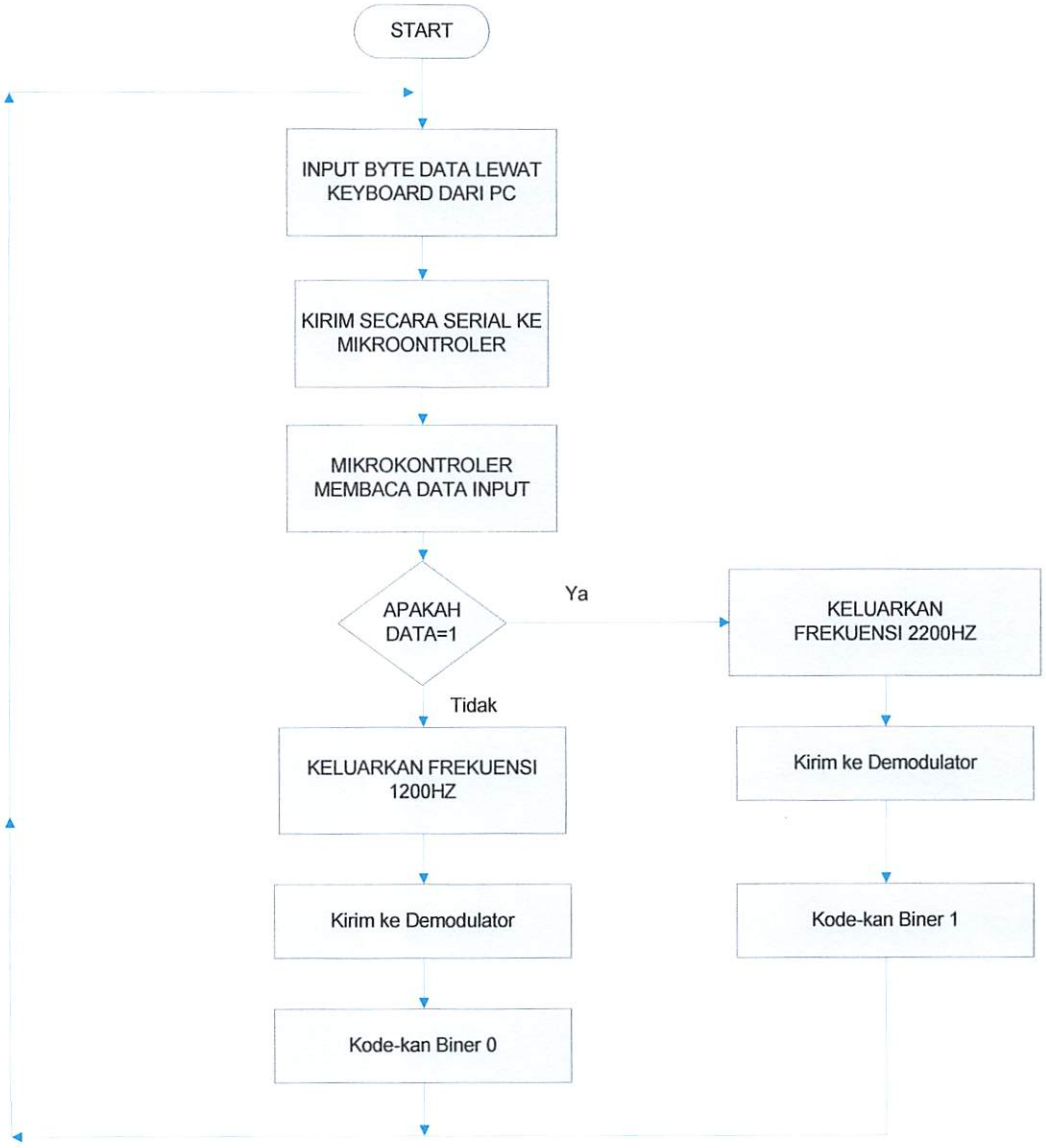
3.3. Perancangan Perangkat Lunak

Perangkat lunak ini berdasarkan pengendali utama yaitu mikrokontroller ATmega8. Pembuatan perangkat lunak sistem aplikasi berdasarkan pada semua kejadian yang harus dikerjakan perangkat keras.

Dalam perancangan alat ini perangkat lunak yang digunakan adalah bahasa pemrograman C dan perangkat lunak bahasa pemrograman Delphi7. untuk mikrokontroller ATmega8 bahasa yang digunakan adalah bahasa pemrograman C. sedangkan sebagai tampilan visual pada PC digunakan bahasa pemrograman delphi7. pembuatan perangkat lunak harus melalui proses-proses uji coba secara *software* maupun secara *hardware*.

Secara garis besar, sistem kerja dari Modulator dan Demodulator FSK seperti Gambar 3.9 di bawah ini:

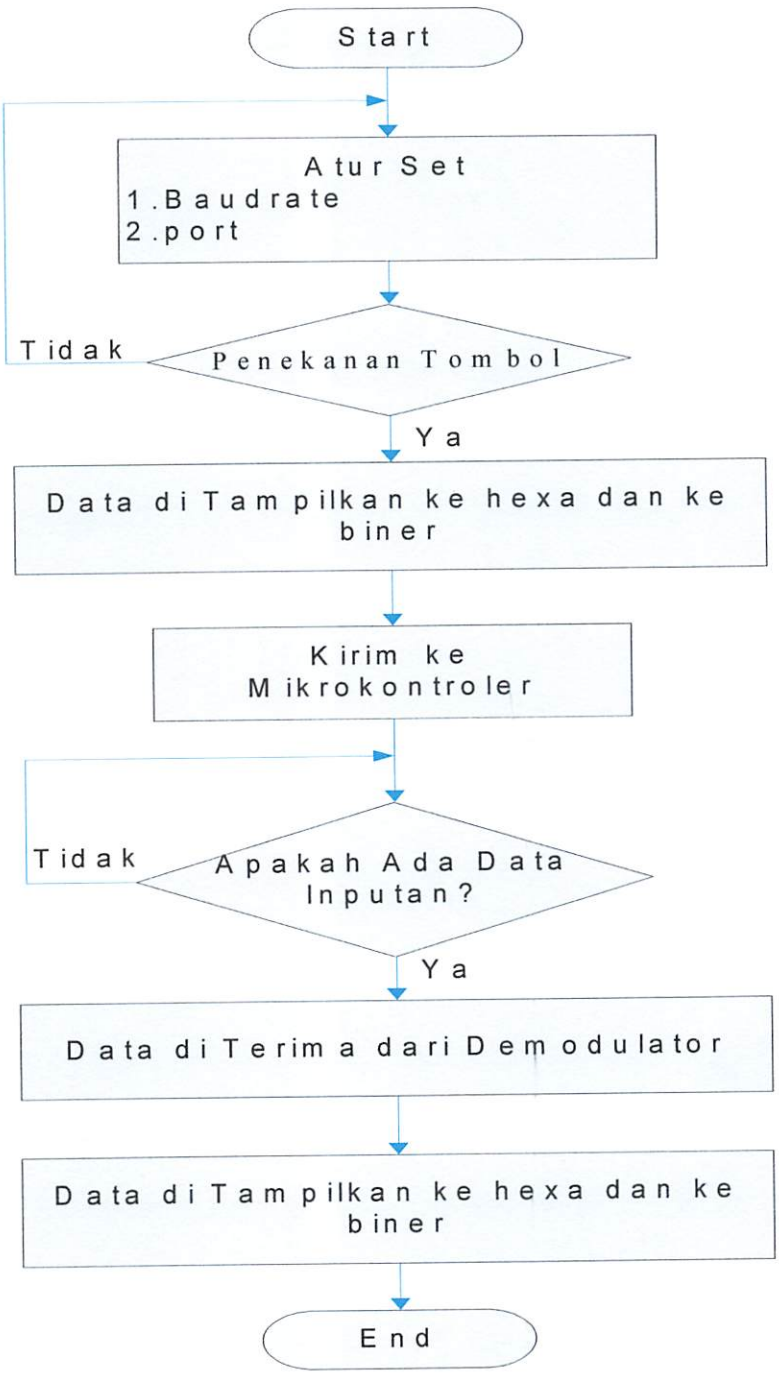
3.3.1 Flowchart Sistem



Gambar 3.9
Flowchart Sistem

Sedangkan untuk flowchart perancangan software-nya seperti pada gambar di bawah ini.

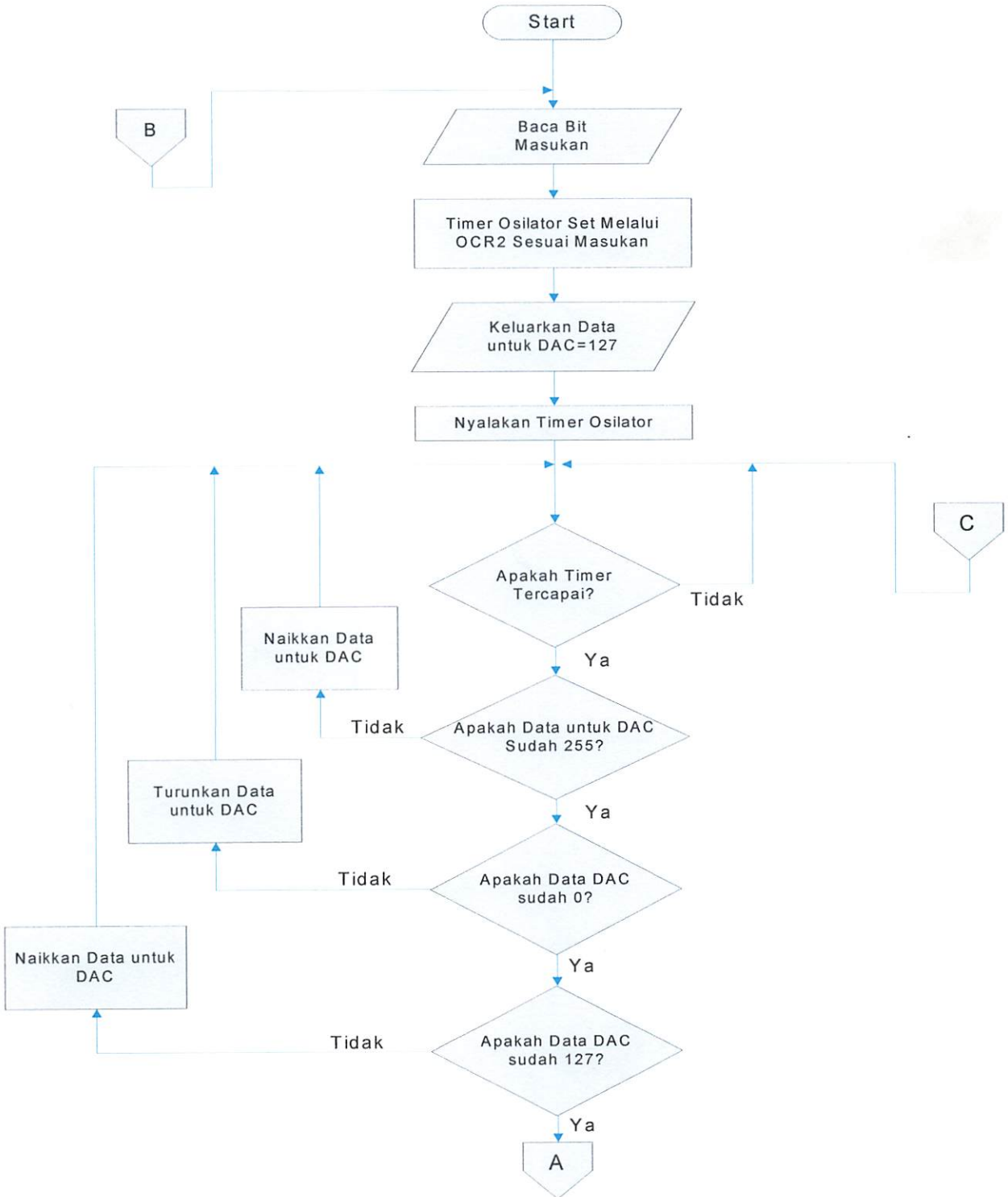
3.3.2 Flowchart Pada Delphi

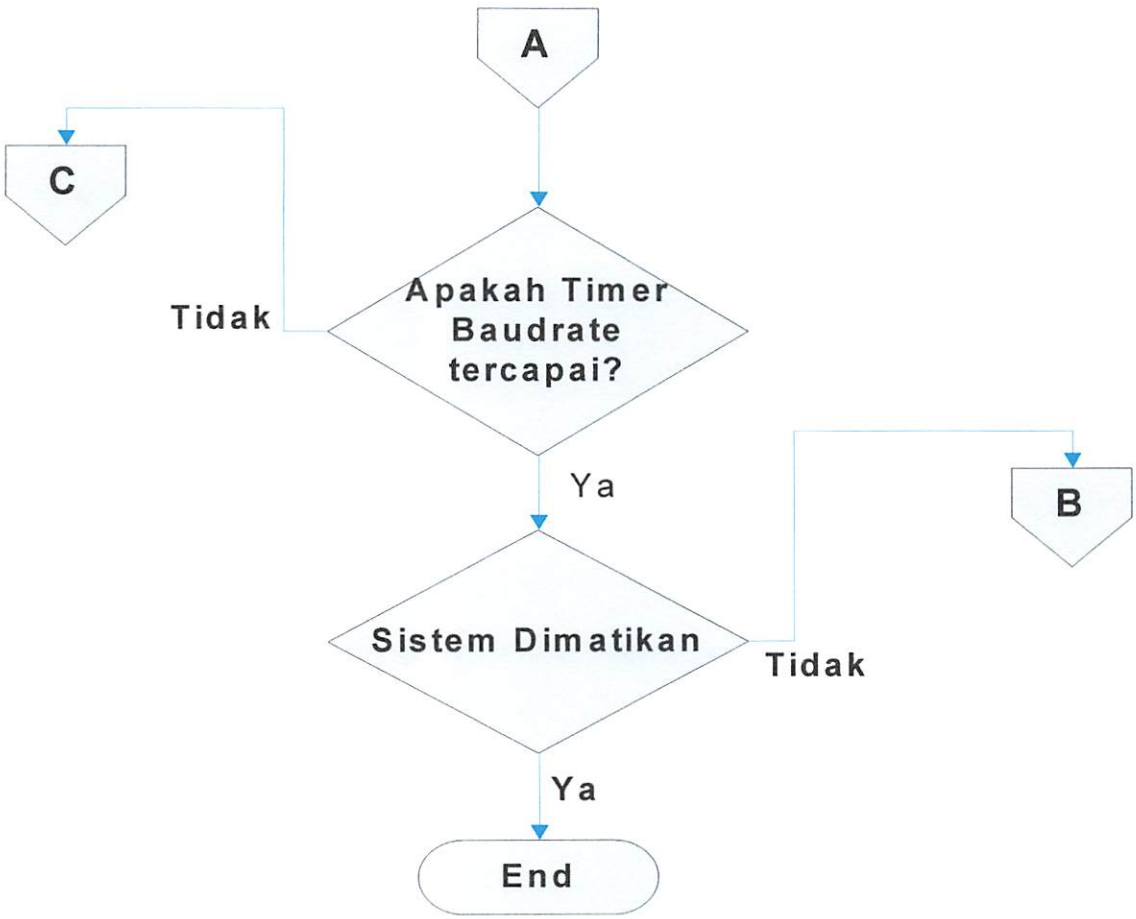


Gambar 3.10

Flowchart Pada Delphi

3.3.3 Flowchart Pada Mikrokontroler





Gambar 3.11

Flowchart Pada Mikrokontroler

BAB IV

PENGUKURAN DAN PENGUJIAN

Untuk memastikan sistem aplikasi modulator dan demodulator FSK dapat bekerja sesuai dengan spesifikasi perencanaan, diperlukan serangkaian pengujian dan pengukuran.

Bab pengujian dan pengukuran ini menguraikan tentang bagian alat yang diuji, tujuan pengujian, langkah-langkah pengujian dan hasil pengujian yang menunjukkan unjuk kerja dari tiap-tiap bagian alat. Pembahasan dalam bab ini dibagi menurut pembagian alat yang diuji untuk mengetahui unjuk kerja sistem secara keseluruhan.

Untuk mengetahui kemampuan alat dan sistem kerja sesuai dengan program yang telah dibuat maka dilakukan pengujian pada alat dan sistem kerja alat.

Pengujian dilakukan pada tiap-tiap blok system aadapun blok-blok yang di uji adalah:

1. Rangkaian RS 232
2. Rangkaian DAC R2R
3. Rangkaian op amp
4. Rangkaian modulator
5. Rangkain demodulator

4.1 Pengujian Komunikasi Serial Interface

a. Tujuan

Untuk mengetahui fungsi pin Tx (pengiriman data) dan Rx(penerimaan data) pada MAX232 sudah berfungsi dengan baik. Dengan cara mengirimkan data dari PC ke

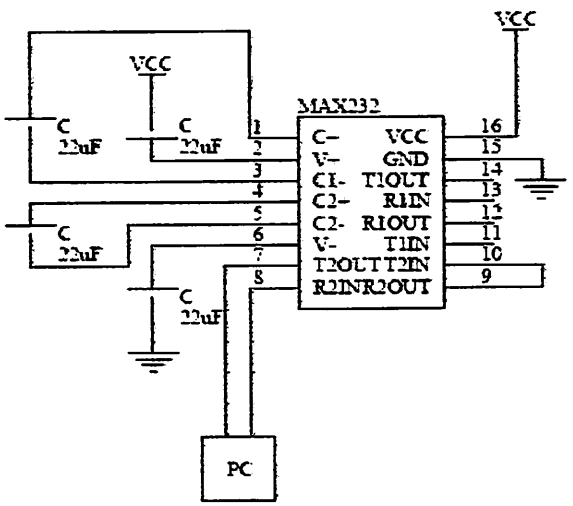
Mikrokontroller melalui rangkaian MAX232 dan pada pin9 dan 10 (Rx dan Tx) dijumper, sehingga data yang akan dikirimkan oleh PC ke Mikrokontroller akan dibalikkan lagi ke PC.

b. Peralatan yang digunakan

- Rangkaian MAX232
- Kabel Serial (DB 9)
- Power Supply +5 volt
- Jumper

c. Langkah-langkah Pengujian

1. Merangkai rangkaian driver seperti pada gambar dibawah ini:



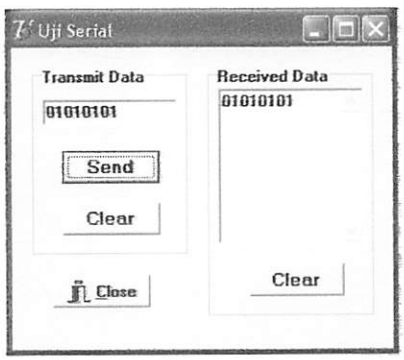
Gambar 4 -1

Rangkaian Pengujian Serial Interface

2. Pada gambar di atas, output MAX232 (Pin T_X) dihubungkan dengan input (Pin R_X), dengan demikian semua data yang dikirim melalui PC akan diumpan-balikkan ke PC lagi.

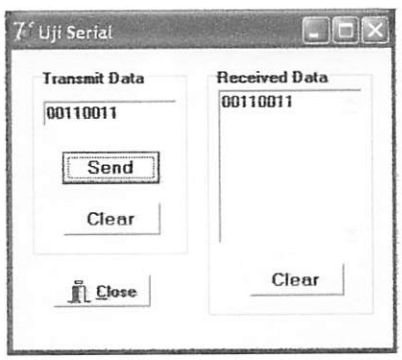
d. Analisa

Data yang dikirim PC 01010101 maka data yang diterima oleh PC pun sama 01010101.



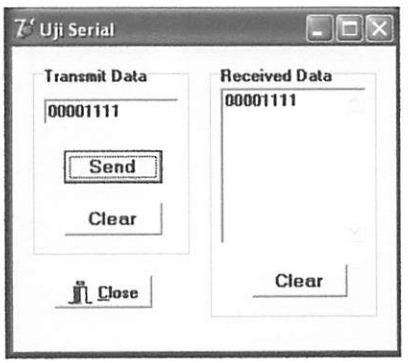
Gambar 4-2
Pengujian Komunikasi Serial Data 1

Data yang dikirim PC 00110011 maka data yang diterima oleh PC pun sama 00110011.



Gambar 4-3
Pengujian Komunikasi Serial Data 2

Data yang dikirim PC 00001111 maka data yang diterima oleh PC pun sama 00001111.



Gambar 4-4
Pengujian Komunikasi Serial Data 3

4.2 Pengujian Rangkaian DAC R2R

a. Tujuan

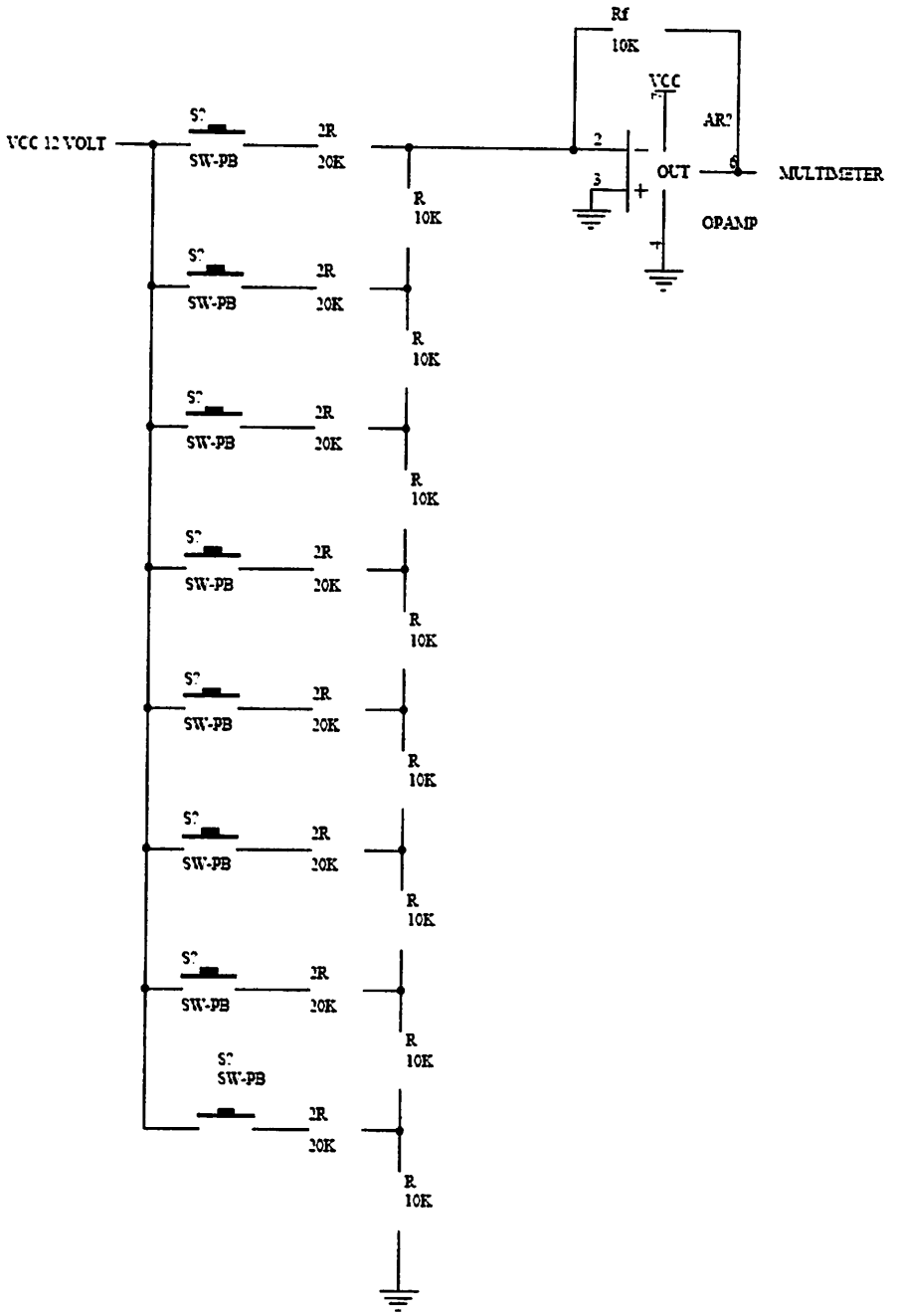
Penggujian rangkaian DAC bertujuan untuk mengetahui apakah DAC berfungsi dengan baik sekaligus untuk mengetahui kelancaran proses konversi atau perubahan sinyal digital ke sinyal analog

b. Peralatan yang digunakan

- Rangkaian DAC R2R
- Sumber tegangan +12 Volt
- Switch 8 Buah
- Multimeter digital (DT9205B)

c. Langkah Pengujian

1. Merangkai rangkaian seperti pada gambar dibawah ini:



Gambar 4-5
Rangkaian Pengujian DAC R2R

2. Menghubungkan kutub positif multimeter digital (multimeter diset pada skala 20 Volt DC) pada outputan DAC, sedangkan kutub negative ke ground.

3. Mengamati perubahan nilai tegangan pada multimeter dan mencatat hasilnya pada tabel 4-1.

d. Analisa

Untuk mengetahui keluaran DAC R2R dapat dicari dengan menggunakan rumus berikut:

$$V_{out} = \frac{R_f}{R} x V_{ref} \left[\frac{D_0}{256} + \frac{D_1}{128} + \frac{D_2}{64} + \frac{D_3}{32} + \frac{D_4}{16} + \frac{D_5}{8} + \frac{D_6}{4} + \frac{D_7}{2} \right]$$

Dimana:

V_{ref} = 12 Volt

- Jika diketahui inputan= 00010000_B. Maka berapakah keluaran DAC R2R ?

  Penyelesaian:

$$V_{out} = -\frac{R_f}{R} x V_{ref} \left[\frac{D_7}{2} + \frac{D_6}{4} + \frac{D_5}{8} + \frac{D_4}{16} + \frac{D_3}{32} + \frac{D_2}{64} + \frac{D_1}{128} + \frac{D_0}{256} \right]$$

$$V_{out} = -\frac{10}{10} x 12 \left[\frac{0}{2} + \frac{0}{4} + \frac{0}{8} + \frac{1}{16} + \frac{0}{32} + \frac{0}{64} + \frac{0}{128} + \frac{0}{256} \right]$$

= -0,75 Volt

Out_{DAC} = -0,75 Volt

- Jika diketahui inputan= 11111111_B. Maka berapakah keluaran DAC R2R ?

  Penyelesaian:

$$V_{out} = -\frac{R_f}{R} x V_{ref} \left[\frac{D_7}{2} + \frac{D_6}{4} + \frac{D_5}{8} + \frac{D_4}{16} + \frac{D_3}{32} + \frac{D_2}{64} + \frac{D_1}{128} + \frac{D_0}{256} \right]$$

$$V_{out} = -\frac{10}{10} x 12 \left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256} \right]$$

= -11,95 Volt

Out_{DAC} = -11,95 Volt

Berikut merupakan tabel perbandingan tegangan output antara hasil pengukuran dan hasil perhitungan dari keluaran DAC R2R:

Tabel 4-1

Data Hasil Pengujian Rangkaian Konversi DAC R2R

NO	Bit Masukan	Keluaran DAC R2R Tegangan V_O (Volt)		
		Perhitungan	Pengukuran	% kesalahan
1	00010000	-0,75	-0,74	0,132
2	00100000	-1,5	-1,52	-0,131
3	00110000	-2,25	-2,22	0,135
4	01000000	-3	-2,90	0,345
5	01010000	-3,75	-3,61	0,388
6	01100000	-4,5	-4,38	0,273
7	01110000	-5,25	-5,17	0,154
8	10000000	-6	-6,12	-0,196
9	11111111	-11,95	-11,50	-0,391

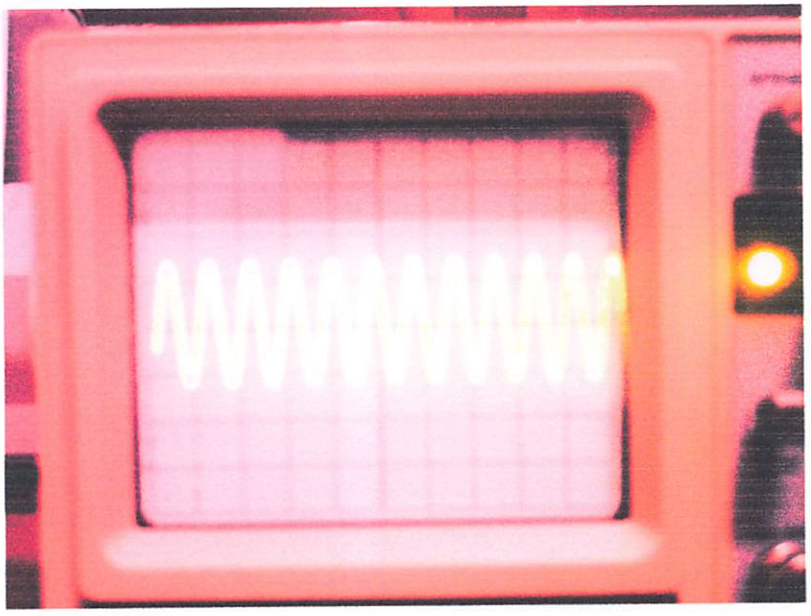
Untuk % kesalahan dapat dihitung dari hasil pengukuran dan perhitungan sebagai berikut :

$$\%\ \text{kesalahan} = \frac{(perhitungan - pengukuran)}{perhitungan} \times 100\%$$

Contoh : V_0 perhitungan = -0,75 Volt

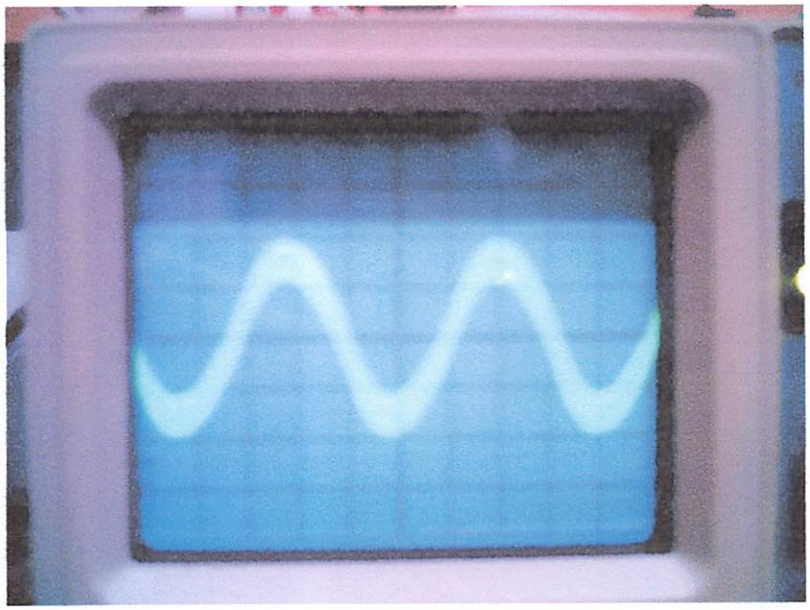
V_0 pengukuran = -0,74 Volt

$$\%\ \text{kesalahan} = \frac{(-0,75) - (-0,74)}{(-0,74)} \times 100\% \quad \text{jadi } \%\ \text{kesalahan} = 0,132\ \%$$



Gambar 4-6
Sinyal Output DAC Sebelum di Filter

Hasil pengujian DAC dapat dilihat dari gambar 4-6, V_{p-p} sebesar 6 V pada Volt / div sebesar 0,2 V dan Time/ div sebesar 0,2 ms. bahwa gambar sinyal yang dihasilkan masih terputus-putus hal ini terjadi karena input yang masuk kedalam DAC berupa data digital sehingga output dari DAC pun masih berupa data 8 bit = 256 langkah. Dari data yang dianalogkan untuk mencapai hasil yang diinginkan maka perlu ditambahkan filter pada output rangkaian DAC sehingga akan dihasilkan sinyal output yang lebih baik seperti gambar 4.7, V_{p-p} sebesar 6 V pada Volt / div sebesar 0,2 V dan Time/ div sebesar 0,5 ms



Gambar 4-7
Sinyal Output DAC Setelah di Filter

4.3 Pengujian Rangkaian Op Amp

a. Tujuan

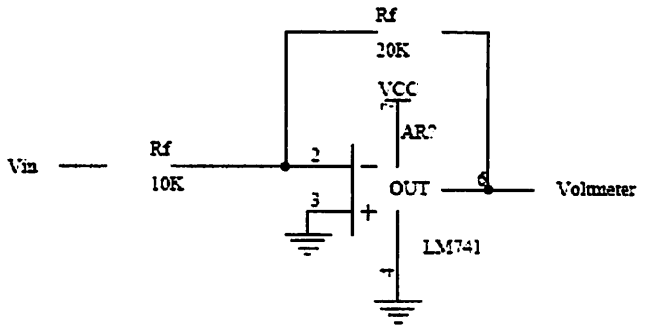
Pengujian rangkaian penguat (op amp) bertujuan untuk mengetahui karakteristik penguatan sinyal output sehingga sesuai dengan yang direncanakan.

b. Peralatan yang digunakan

- Rangkaian op amp
- Sumber tegangan ±5 Volt
- Voltmeter digital (DT9205B)

c. Langkah Pengujian

1. Merangkai rangkaian seperti pada gambar dibawah ini:



Gambar 4-8
Rangkaian Pengujian Op Amp

2. Menghubungkan kutub positif multimeter digital (multimeter diset pada skala 10 Volt DC) pada pin 1 dari IC LM 741, sedangkan kutub negative ke ground.
3. Mengamati perubahan nilai tegangan pada multimeter dan mencatat hasilnya pada tabel 4-2.

Tabel 4.2.

Data Hasil Perhitungan dan Pengukuran Rangkaian Op Amp

NO	Tegangan input (mV)	Tegangan Output (mV)		Gain (A)	% Kesalahan
		Perhitungan	Pengukuran		
1	100	200	197	2	0,15
2	200	400	399	2	0,025
3	300	600	600	2	0
4	400	800	798	2	0,025
5	500	1000	996	2	0,040

d. Analisa

Untuk perhitungan tegangan output op amp dapat dicari dengan menggunakan rumus berikut:

$$V_{OUT} = -V_{IN}\frac{R_f}{R_i}$$ Dimana: $V_{IN} = 100$

Maka:

$$V_{OUT} = -V_{IN}\frac{R_f}{R_i}; V_{OUT} = -100\frac{2R_f}{R_f}; V_{OUT} = -200mV$$

Sedangkan penguatannya (A_{CL}) seperti persamaan dibawah ini:

$$A_{CL} = \frac{V_{OUT}}{V_{IN}} = -\frac{R_f}{Ri}\ A_{CL} = \frac{200}{100}$$

$$A_{CL} = 2kali$$

Untuk % kesalahan dapat dihitung dari hasil pengukuran dan perhitungan sebagai berikut : $$\%\ \text{kesalahan} = \frac{(perhitungan - pengukuran)}{perhitungan} \times 100\%$$

Contoh : V_0 perhitungan = 200 mVolt

V_0 pengukuran = 197 mVolt

$$\%\ \text{kesalahan} = \frac{200-197}{197} \times 100\%$$ jadi % kesalahan = 0,15 %

4.4 Pengujian Rangkaian Modulator FSK

a. Tujuan

Untuk mengetahui bentuk sinyal dan besar frekuensi yang dibangkitkan oleh rangkaian modulator FSK apakah telah sesuai dengan frekuensi FSK yang direncanakan yaitu 1200Hz dan 2200Hz.

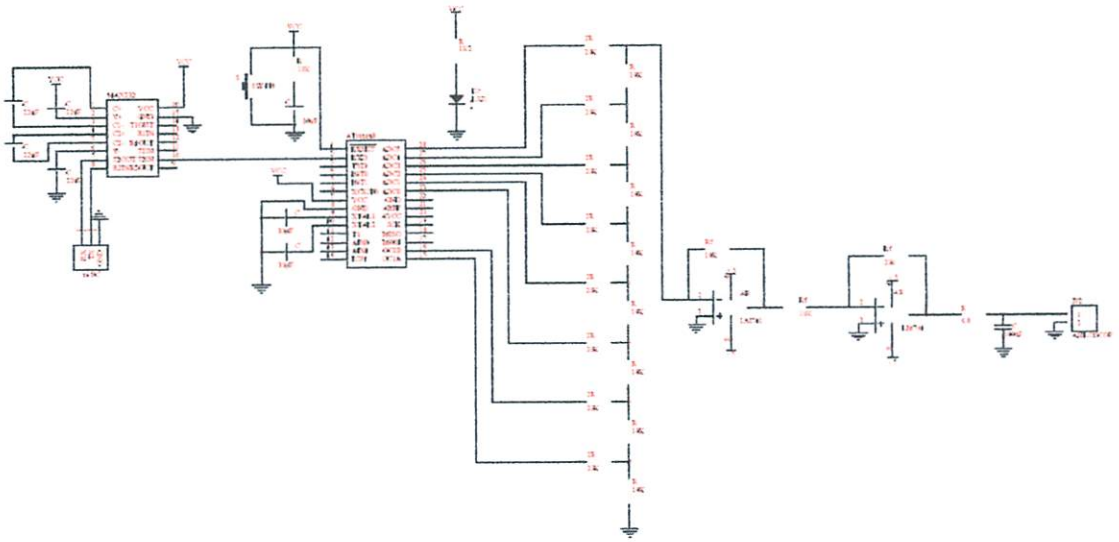
b. Peralatan yang digunakan

- Rangkaian modulator FSK

- Oscilloscope (HEWLETT PACKARD 54601A)

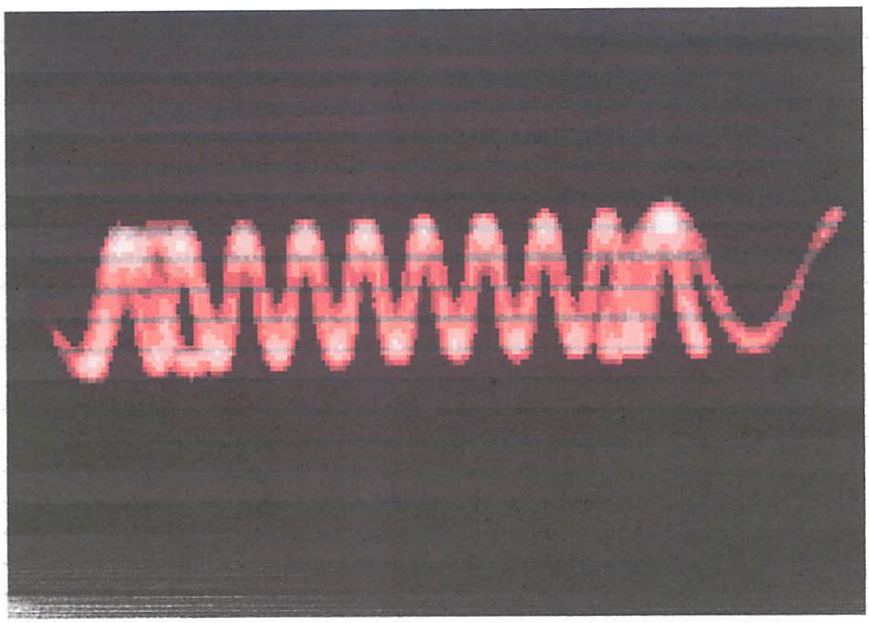
c. Langkah pengujian

Pengujian dilakukan dengan cara melihat sinyal output modulator, yaitu pada pin output filter. *Osiloscope* diset pada 500 V / div dan 1.00 ms /div, Probe merah pada *Osiloscope* dipasang pada output filter dan probe hitam *Osiloscope* dipasang pada *ground.*



Gambar 4-9
Rangkaian Pengujian Modulator FSK

Sinyal yang dihasilkan oleh modulator FSK tersebut terlihat seperti pada gambar 4-10 dengan frekuensi yang dihasilkan sebesar 1200 Hz dan 2200Hz dengan V_{p-p} sebesar 4,4 V pada Volt / div sebesar 0,1 V dan Time / div sebesar 0,5 ms.



Gambar 4-10
Sinyal Output Modulator FSK

4.5 Pengujian Demodulator MT8841

a. Tujuan

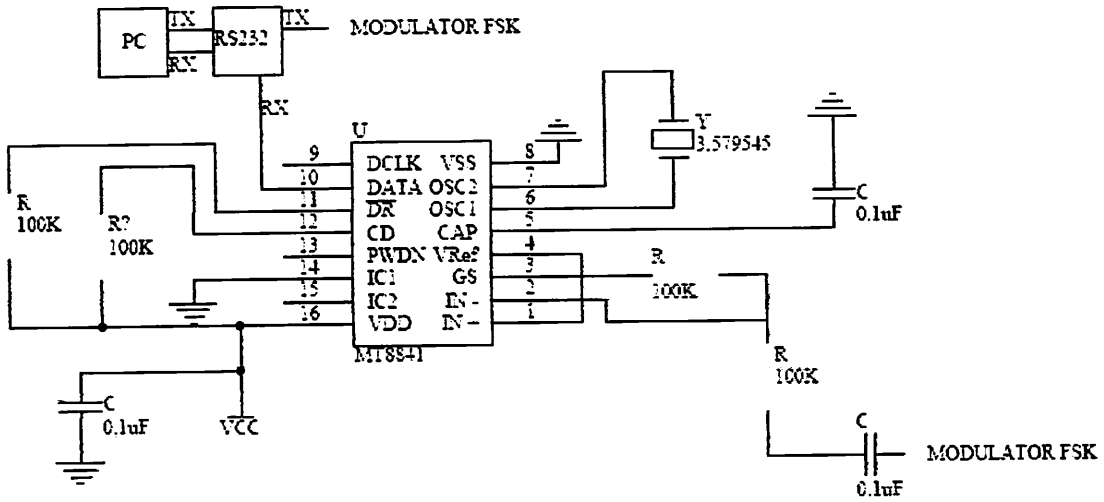
Untuk mengetahui pengkodean pada MT8841 sudah berfungsi dengan baik. Dengan cara mengirimkan data dari PC ke Modulator melalui rangkaian MAX232 pada pin 10 dan pin 9 dihubungkan ke Demodulator, sehingga data yang akan dikirimkan oleh PC ke Modulator akan dibalikkan lagi ke PC.

b. Peralatan yang digunakan

- Rangkaian MT8841
- Modulator FSK
- Kabel Serial (DB 9)
- Power Supply +5 volt
- Rangkaian MAX232

c. Langkah-langkah Pengujian

1. Merangkai rangkaian seperti pada gambar dibawah ini:



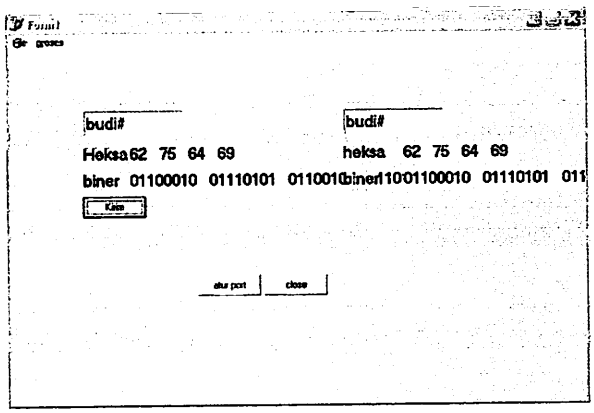
Gambar 4 -11

Rangkaian Pengujian Demodulator MT8841

2. Pada gambar di atas, output MT8841 (Pin DATA) dihubungkan dengan PC dan diberikan input dari rangkaian Modulator, dengan demikian semua data yang dikirim melalui PC akan diumpan-balikkan ke PC lagi.

d. Analisa

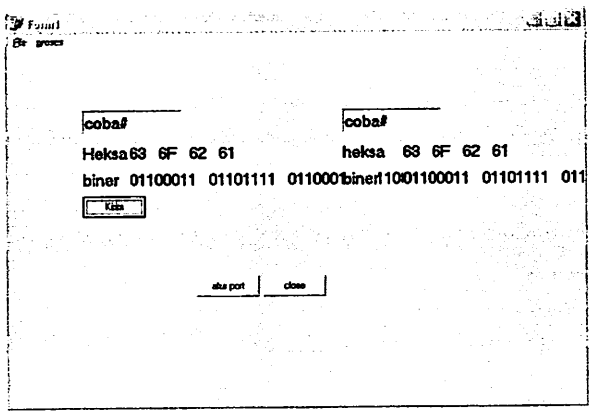
Data yang dikirim PC budi maka data yang diterima oleh PC pun sama budi.



Gambar 4-12

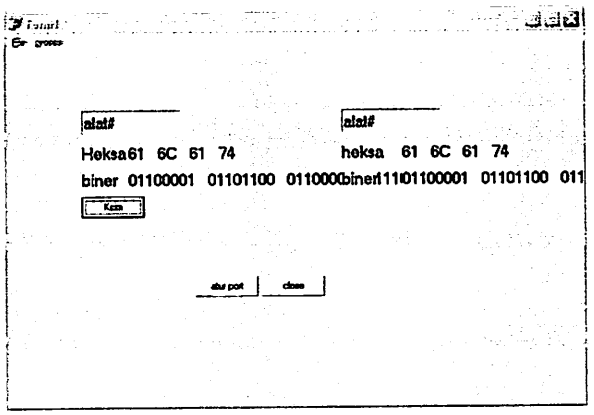
Pengujian Demodulator dari PC Data 1

Data yang dikirim PC coba maka data yang diterima oleh PC pun sama coba.



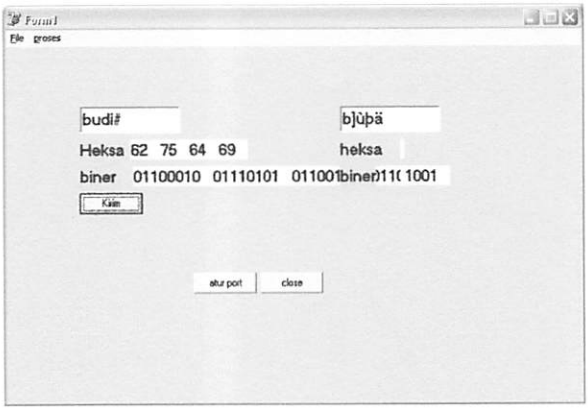
Gambar 4-13
Pengujian Demodulator dari PC Data 2

Data yang dikirim PC alat maka data yang diterima oleh PC pun sama alat.



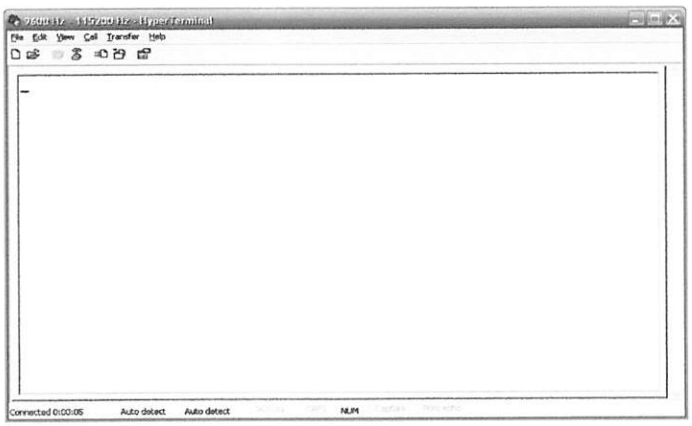
Gambar 4-14
Pengujian Demodulator dari PC Data 3

Apabila boudrate disetting lebih dari 1200 bps maka data yang diterima oleh PC mengalami kerusakan karakter.



Gambar 4-15
Pengujian Demodulator dari PC dengan Boudrate +1200 bps

Apabila boudrate disetting lebih dari 9600 bps maka data tidak bisa ditampilkan



Gambar 4-16
Pengujian Demodulator dari PC dengan Boudrate +9600 bps

BAB V

PENUTUP

5.1. Kesimpulan

Berdasarkan semua kegiatan yang telah dilakukan berkaitan dengan penyusunan skripsi ini yang meliputi orientasi pustaka, perencanaan sistem, pembuatan alat dan pengujian alat, dapat diambil kesimpulan sebagai berikut:

1. Dari hasil pengujian rangkaian modulator dan demodulator FSK, dalam proses pengiriman dan penerimaan data, dari 100 kali pengiriman data yang karakternya berbeda, rata-rata terjadi kesalahan akibat penyimpangan waktu antara waktu pengiriman dan penerimaan sebesar 0.98 % yaitu dari 100 kali data dikirim, 98 data dapat diterima oleh penerima sesuai dengan data yang dikirim, dua data mengalami kerusakan berupa kerusakan karakter.
2. Pada pengujian sistem secara keseluruhan boudrate maksimal yang bisa dicapai adalah 1200 bps apabila pengaturannya lebih dari 1200 bps maka data yang diterima oleh PC mengalami kerusakan beberapa buah karakter.
3. Kecepatan pengiriman data yang relatif masih rendah (1200 bps) sebagai akibat dari kualitas penerima yang tidak terlalu baik.

5.2. Saran

Alat Modulator FSK dengan metode DDS ini dapat dikembangkan lagi agar lebih sempurna dalam penggunaannya diantaranya dapat dilakukan dengan;

1. Dari alat ini sangat ideal dikembangkang untuk aplikasi-aplikasi frequency hopping, walaupun demikian sistem DDS juga dapat digunakan pada peralatan pemancar radio dan TV, peralatan test, dll.

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The Application Engineer—33
out Direct Digital Synthesis

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is Direct Digital Synthesis?

digital synthesis (DDS) is a method of producing an analog waveform—usually a sine wave enerating a time-varying signal in digital form and then performing a digital-to-analog sion. Because operations within a DDS device are primarily digital, it can offer fast ing between output frequencies, fine frequency resolution, and operation over a broad m of frequencies. With advances in design and process technology, today's DDS devices are ompact and draw little power.

vould one use a direct digital synthesizer (DDS)? Aren't there other methods for easily ting frequencies?

ility to accurately produce and control waveforms of various frequencies and profiles has e a key requirement common to a number of industries. Whether providing agile sources of ase-noise variable-frequencies with good spurious performance for communications, or generating a frequency stimulus in industrial or biomedical test equipment applications, ience, compactness, and low cost are important design considerations.

possibilities for frequency generation are open to a designer, ranging from *phase-locked-loop* based techniques for very high-frequency synthesis, to dynamic programming of *digital-to- converter* (DAC) outputs to generate arbitrary waveforms at lower frequencies. But the DDS ue is rapidly gaining acceptance for solving frequency- (or waveform) generation ments in both communications and industrial applications because single-chip IC devices erate programmable analog output waveforms simply and with high resolution and y.

nore, the continual improvements in both process technology and design have resulted in l power consumption levels that were previously unthinkably low. For example, the 3, a DDS-based programmable waveform generator (Figure 1), operating at 5.5 V with a 25- ock, consumes a maximum power of 30 *milliwatts*.

Figure 1. The AD9833—a one-chip waveform generator.

are the main benefits of using a DDS?

evices like the AD9833 are programmed through a high speed *serial peripheral-interface* nd need only an external clock to generate simple sine waves. DDS devices are now le that can generate frequencies from less than 1 Hz up to 400 MHz (based on a 1-GHz The benefits of their low power, low cost, and single small package, combined with their t excellent performance and the ability to digitally program (and reprogram) the output rm, make DDS devices an extremely attractive solution—preferable to less-flexible ns comprising aggregations of discrete elements.

kind of outputs can I generate with a typical DDS device?

evices are not limited to purely sinusoidal outputs. Figure 2 shows the square-, triangular-, usoidal outputs available from an AD9833.

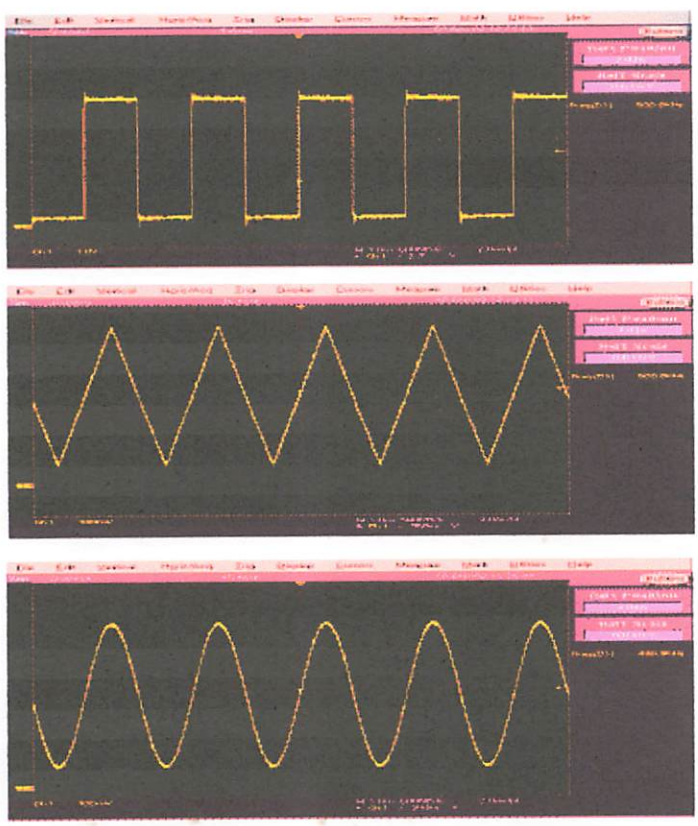


Figure 2. Square-, triangular-, and sinusoidal outputs from a DDS.

oes a DDS device create a sine wave?

a breakdown of the internal circuitry of a DDS device: its main components are a *phase lator*, a means of *phase-to-amplitude conversion* (often a sine look-up table), and a DAC. locks are represented in Figure 3.

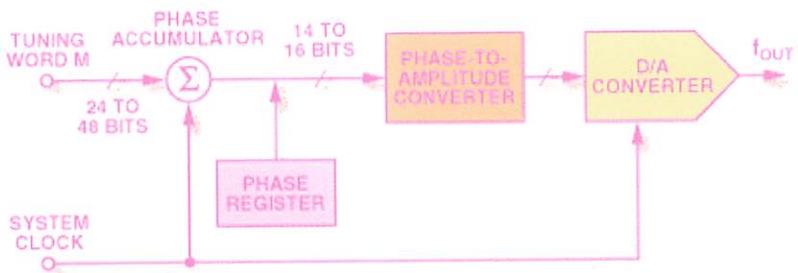


Figure 3. Components of a direct digital synthesizer.

produces a sine wave at a given frequency. The frequency depends on two variables, the *ce-clock* frequency and the binary number programmed into the frequency register (*tuning*

ary number in the frequency register provides the main input to the phase accumulator. If a ok-up table is used, the phase accumulator computes a phase (angle) address for the look-up which outputs the digital value of amplitude—corresponding to the sine of that phase angle—DAC. The DAC, in turn, converts that number to a corresponding value of analog voltage or . To generate a fixed-frequency sine wave, a constant value (the phase increment—which is ined by the binary number) is added to the phase accumulator with each clock cycle. If the ncrement is large, the phase accumulator will step quickly through the sine look-up table s generate a high frequency sine wave. If the phase increment is small, the phase ulator will take many more steps, accordingly generating a slower waveform.

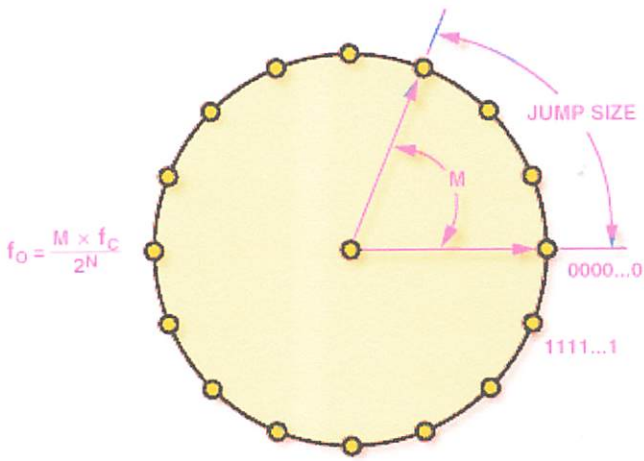
do you mean by a *complete* DDS?

egration of a D/A converter and a DDS onto a single chip is commonly known as a complete olution, a property common to all DDS devices from ADI.

alk some more about the phase accumulator. How does it work?

uous-time sinusoidal signals have a repetitive angular phase range of 0 to 2π. The digital nentation is no different. The counter's carry function allows the phase accumulator to act as e wheel in the DDS implementation.

lerstand this basic function, visualize the sine-wave oscillation as a vector rotating around a circle (see Figure 4). Each designated point on the phase wheel corresponds to the equivalent n a cycle of a sine wave. As the vector rotates around the wheel, visualize that the sine of le generates a corresponding output sine wave. One revolution of the vector around the vheel, at a constant speed, results in one complete cycle of the output sine wave. The phase ulator provides the equally spaced angular values accompanying the vector's linear rotation the phase wheel. The contents of the phase accumulator correspond to the points on the f the output sine wave.



n	NUMBER OF POINTS
8	256
12	4096
16	65535
20	1048576
24	16777216
28	268435456
32	4294967296
48	281474976710656

Figure 4. Digital phase wheel.

ase accumulator is actually a modulo-*M* counter that increments its stored number each time ves a clock pulse. The magnitude of the increment is determined by the binary-coded input *M*). This word forms the phase step size between reference-clock updates; it effectively sets any points to skip around the phase wheel. The larger the jump size, the faster the phase ulator overflows and completes its equivalent of a sine-wave cycle. The number of discrete oints contained in the *wheel* is determined by the resolution of the phase accumulator (*n*), determines the tuning resolution of the DDS. For an $n = 28$-bit phase accumulator, an *M* f 0000...0001 would result in the phase accumulator overflowing after 2^{28} reference-clock (increments). If the *M* value is changed to 0111...1111, the phase accumulator will overflow nly 2 reference-clock cycles (the minimum required by Nyquist). This relationship is found in ic tuning equation for DDS architecture:

$$f_{OUT} = \frac{M \times f_C}{2^n}$$

output frequency of the DDS

nary tuning word

ternal reference clock frequency (system clock)

gth of the phase accumulator, in bits

es to the value of M result in immediate and *phase-continuous* changes in the output ncy. No loop settling time is incurred as in the case of a phase-locked loop.

output frequency is increased, the number of samples per cycle decreases. Since sampling dictates that at least two samples per cycle are required to reconstruct the output waveform, ximum fundamental output frequency of a DDS is $f_C/2$. However, for practical applications,

ut frequency is limited to somewhat less than that, improving the quality of the ucted waveform and permitting filtering on the output.

enerating a constant frequency, the output of the phase accumulator increases linearly, so log waveform it generates is inherently a ramp.

ow is that linear output translated into a sine wave?
e-to-amplitude lookup table is used to convert the phase-accumulator's instantaneous output 28 bits for AD9833)—with unneeded less-significant bits eliminated by truncation—into the ave amplitude information that is presented to the (10-bit) D/A converter. The DDS cture exploits the symmetrical nature of a sine wave and utilizes mapping logic to synthesize lete sine wave from one-quarter-cycle of data from the phase accumulator. The phase-to-ude lookup table generates the remaining data by reading forward then back through the table. This is shown pictorially in Figure 5.

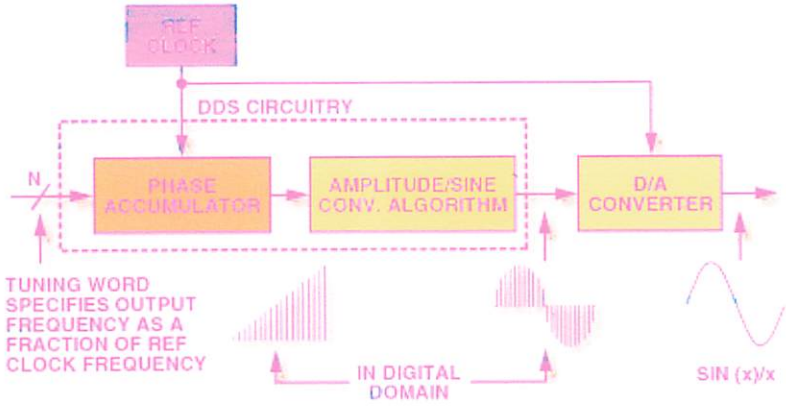


Figure 5. Signal flow through the DDS architecture.

are popular uses for DDS?
ations currently using DDS-based waveform generation fall into two principal categories: ers of communications systems requiring agile (i.e., immediately responding) frequency s with excellent phase noise and low spurious performance often choose DDS for its nation of spectral performance and frequency-tuning resolution. Such applications include a DDS for modulation, as a reference for a PLL to enhance overall frequency tunability, as a scillator (LO), or even for direct RF transmission.

atively, many industrial and biomedical applications use a DDS as a programmable rm generator. Because a DDS is digitally programmable, the phase and frequency of a rm can be easily adjusted without the need to change the external components that would ly need to be changed when using traditional analog-programmed waveform generators. ermits simple adjustments of frequency in real time to locate resonant frequencies or nsate for temperature drift. Such applications include using a DDS in adjustable frequency to measure impedance (for example in an impedance-based sensor), to generate pulse-wave ted signals for micro-actuation, or to examine attenuation in LANs or telephone cables.

lo you consider to be the key advantages of DDS to designers of real-world equipment stems?
s cost-competitive, high-performance, functionally integrated DDS ICs are becoming

n in both communication systems and sensor applications. The advantages that make them ve to design engineers include:

igitally controlled micro-hertz frequency-tuning and sub-degree phase-tuning capability, xtremely fast *hopping speed* in tuning output frequency (or phase); phase-continuous requency hops with no overshoot/undershoot or analog-related loop settling-time anomalies, he digital architecture of DDS eliminates the need for the manual tuning and tweaking elated to component aging and temperature drift in analog synthesizer solutions, and he digital control interface of the DDS architecture facilitates an environment where systems an be remotely controlled and optimized with high resolution under processor control.

ould I use a DDS device for FSK encoding?

frequency-shift keying (usually referred to simply as FSK) is one of the simplest forms of coding. The data is transmitted by shifting the frequency of a continuous carrier to one of crete frequencies (hence *binary*). One frequency, f_1, (perhaps the higher) is designated as the requency (binary one) and the other, f_0, as the *space* frequency (binary zero). Figure 6 shows mple of the relationship between the mark-space data and the transmitted signal.

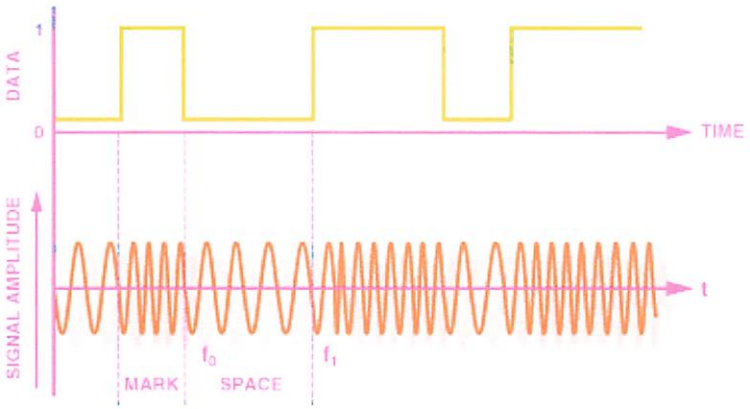


Figure 6. FSK modulation.

coding scheme is easily implemented using a DDS. The DDS frequency tuning word, nting the output frequencies, is set to the appropriate values to generate f_0 and f_1 as they n the pattern of 0s and 1s to be transmitted. The user programs the two required tuning words e device before transmission. In the case of the AD9834, two frequency registers are le to facilitate convenient FSK encoding. A dedicated pin on the device (FSELECT) accepts dulating signal and selects the appropriate tuning word (or frequency register). The block n in Figure 7 demonstrates a simple implementation of FSK encoding.

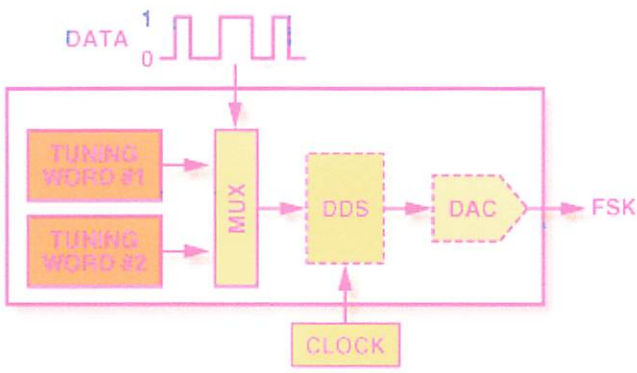


Figure 7. A DDS-based FSK encoder.

w about PSK coding?

hift keying (PSK) is another simple form of data encoding. In PSK, the frequency of the emains constant and the *phase* of the transmitted signal is varied to convey the information.

schemes to accomplish PSK, the simplest-known as binary PSK (BPSK)—uses just two hases: 0 degrees and 180 degrees. BPSK encodes 0° phase shift for a logic 1 input and 180° hift for a logic 0 input. The state of each bit is determined according to the state of the ng bit. If the phase of the wave does not change, the signal state stays the same (low or high) phase of the wave reverses (changes by 180 degrees), then the signal state changes (from igh, or from high to low).

coding is easily implemented with DDS ICs. Most of the devices have a separate input (a *phase register*) that can be loaded with a phase value. This value is directly added to the f the carrier without changing its frequency. Changing the contents of this register tes the phase of the carrier, thus generating a PSK output signal. For applications that high speed modulation, the AD9834 allows the preloaded phase registers to be selected dedicated toggling input pin (PSELECT), which alternates between the registers and tes the carrier as required.

ophisticated forms of PSK employ four- or eight- wave phases. This allows binary data to be tted at a faster rate per phase change than is possible with BPSK modulation. In four-phase tion (*quadrature* PSK or QPSK), the possible phase angles are 0, +90, –90, and 180 degrees; ase shift can represent two signal elements. The AD9830, AD9831, AD9832, and AD9835 four phase registers to allow complex phase modulation schemes to be implemented by ously updating different phase offsets to the registers.

ultiple DDS devices be synchronized for, say, I-Q capability?

ssible to use two single DDS devices that operate on the same master clock to output two whose phase relationship can then be directly controlled. In Figure 8, two AD9834s are nmed using one reference clock, with the same reset pin being used to update both parts. his setup, it is possible to do I-Q modulation.

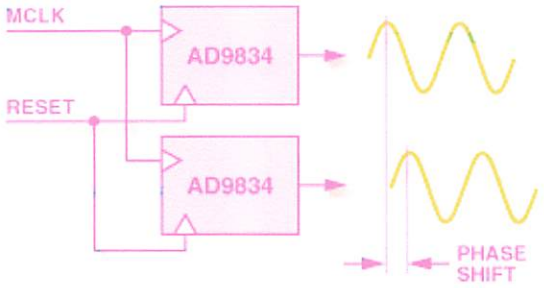


Figure 8. Multiple DDS ICs in synchronous mode.

must be asserted after power-up and prior to transferring any data to the DDS. This sets the utput to a known phase, which serves as the common reference point that allows onization of multiple DDS devices. When new data is sent simultaneously to multiple DDS coherent phase relationship can be maintained, and their relative phase offset can be ably shifted by means of the phase-offset register. The AD9833 and AD9834 have 12 bits of esolution, with an effective resolution of 0.1 degree. [For further details on synchronizing e DDS units please see Application Note AN-605.]

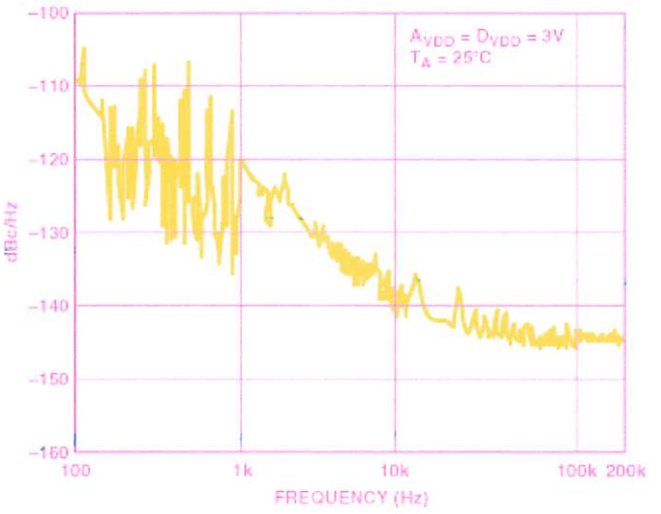
are the key performance specs of a DDS based system?

noise, jitter, and spurious-free dynamic range (SFDR).

noise is a measure (dBc/Hz) of the short-term frequency instability of the oscillator. It is ed as the single-sideband noise resulting from changes in frequency (in decibels below the ude at the operating frequency of the oscillator using a 1-Hz bandwidth) at two or more ncy displacements from the operating frequency of the oscillator. This measurement has lar application to performance in the analog communications industry.

S devices have good phase noise?

n a sampled system depends on many factors. Reference-clock jitter can be seen as phase n the fundamental signal in a DDS system; *and phase truncation* may introduce an error to the system, depending on the code word chosen. For a ratio that can be exactly expressed ncated binary-coded word, there is no truncation error. For ratios requiring more bits than ilable, the resulting phase noise truncation error results in spurs in a spectral plot. Their udes and distribution depends on the code word chosen. The DAC also contributes to noise ystem. DAC quantization or linearity errors will result in both noise and harmonics. Figure 9 a phase noise plot for a typical DDS device—in this case an AD9834.



9. Typical output phase noise plot for the AD9834. Output frequency is 2 MHz and M clock is 50 MHz.

bout jitter?

the dynamic displacement of digital signal edges from their long-term average positions, ed in degrees rms. A perfect oscillator would have rising and falling edges occurring at y regular moments in time and would never vary. This, of course, is impossible, as even the illators are constructed from real components with sources of noise and other ctions. A high-quality, low-phase-noise crystal oscillator will have jitter of less than 35 onds (ps) of period jitter, accumulated over many millions of clock edges

oscillators is caused by thermal noise, instabilities in the oscillator electronics, external ence through the power rails, ground, and even the output connections. Other influences external magnetic or electric fields, such as RF interference from nearby transmitters, an contribute jitter affecting the oscillator's output. Even a simple amplifier, inverter, or ill contribute jitter to a signal.

e output of a DDS device will add a certain amount of jitter. Since every clock will already intrinsic level of jitter, choosing an oscillator with low jitter is critical to begin with. g down the frequency of a high-frequency clock is one way to reduce jitter. With frequency , the same amount of jitter occurs within a longer period, reducing its percentage of system

al, to reduce essential sources of jitter and avoid introducing additional sources, one should able reference clock, avoid using signals and circuits that slew slowly, and use the highest reference frequency to allow increased oversampling.

s-Free Dynamic Range (SFDR) refers to the ratio (measured in decibels) between the level of the fundamental signal and the highest level of any spurious, signal—including nd harmonically related frequency components—in the spectrum. For the very best SFDR, ential to begin with a high-quality oscillator.

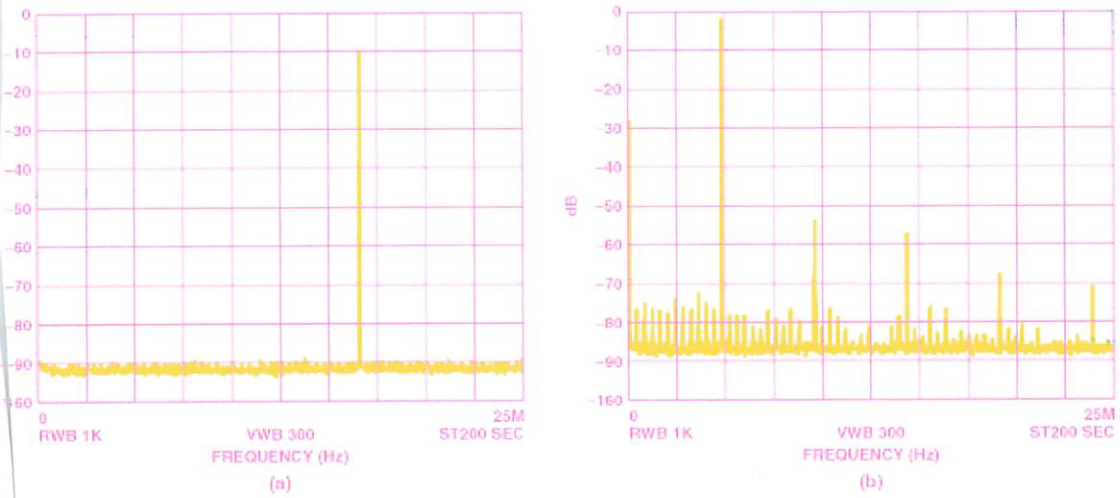


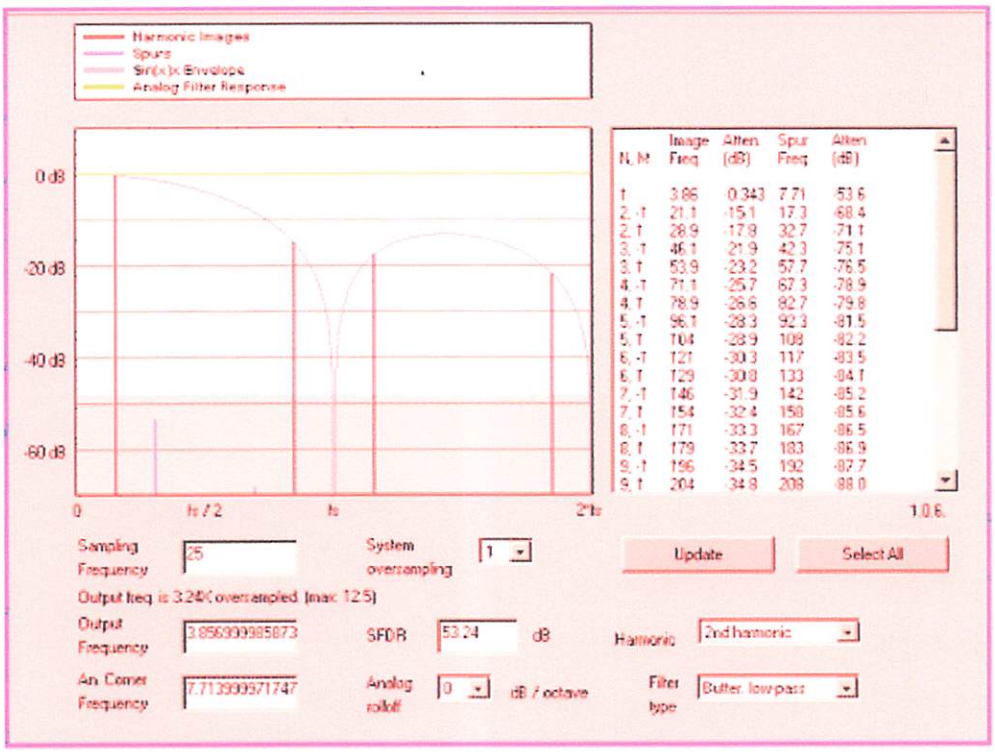
Figure 10. Output of an AD9834 with a 50-MHz master clock and (a) f_{out} = 16.667 MHz (i.e., MCLK/3); (b) f_{out} = 4.8 MHz.

s an important specification in an application where the frequency spectrum is being shared her communication channels and applications. If a transmitter's output sends spurious into other frequency bands, they can corrupt, or interrupt neighboring signals.

output plots taken from an AD9834 (10-bit DDS) with a 50-MHz master clock are shown re 10. In (a), the output frequency is exactly 1/3 of the master clock frequency (MCLK). e of the judicious choice of frequencies, there are no harmonic frequencies in the 25-MHz , aliases are minimized, and the spurious behavior appears excellent, with all spurs at least elow the signal (SFDR = 80 dB). The lower frequency setting in (b) has more points to he waveform (but not enough for a really clean waveform), and gives a more realistic the largest spur, at the second-harmonic frequency, is about 50 dB below the signal = 50 dB).

have tools that make it easier to program and predict the performance of the DDS?

-line *interactive design tool* is an assistant for selecting tuning words, given a reference nd desired output frequencies and/or phases. The required frequency is chosen, and idealized harmonics are shown after an external reconstruction filter has been applied. An example is in Figure 11. Tabular data is also provided for the major images and harmonics.



re 11. Screen presentation provided by an interactive design tool. A sin*x*/*x* presentation of a typical device output.

vill these tools help me program the DDS?

ıt's needed is the required frequency output and the system's reference clock frequency. The tool will output the full programming sequence required to program the part. In the example ıre 12, the MCLK is set to 25 MHz and the desired output frequency is set to 10 MHz. Once date button is pressed, the full programming sequence to program the part is contained in the quence register.

Figure 12. Typical display of programming sequence.

ın I evaluate your DDS devices?

S devices have an evaluation board available for purchase. They come with dedicated

e, allowing the user to test/evaluate the part easily within minutes of receiving the board. A al note accompanying each evaluation board contains schematic information and shows best ıended board-design and layout practice.

can I find more information on DDS devices?
in DDS homepage is located at www.analog.com/dds

o design tools are provided at http://www.analog.com/en/DCDesignToolsDisplay/ .00.html

lepth tutorial on DDS technology can be found at http://www.analog.com/UploadedFiles/ ls/450968421DDS_Tutorial_rev12-2-99.pdf

5 can be found at http://www.analog.com/UploadedFiles/Application_Notes/ 2853519044414816844 7035AN605_0.pdf

est DDS selection guide can be found at http://www.analog.com/IST/ onTable/?selection_table_id=27

TOP OF PAGE

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ormance, Low-power AVR® 8-bit Microcontroller
RISC Architecture
owerful Instructions – Most Single-clock Cycle Execution
General Purpose Working Registers
Static Operation
16 MIPS Throughput at 16 MHz
ip 2-cycle Multiplier
e Program and Data Memories
tes of In-System Self-Programmable Flash
lurance: 10,000 Write/Erase Cycles
nal Boot Code Section with Independent Lock Bits
System Programming by On-chip Boot Program
e Read-While-Write Operation
ytes EEPROM
durance: 100,000 Write/Erase Cycles
te Internal SRAM
amming Lock for Software Security
l Features
3-bit Timer/Counters with Separate Prescaler, one Compare Mode
16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture
Time Counter with Separate Oscillator
e PWM Channels
nnel ADC in TQFP and MLF package
ht Channels 10-bit Accuracy
nnel ADC in PDIP package
ht Channels 10-bit Accuracy
oriented Two-wire Serial Interface
rammable Serial USART
er/Slave SPI Serial Interface
rammable Watchdog Timer with Separate On-chip Oscillator
hip Analog Comparator
Microcontroller Features
er-on Reset and Programmable Brown-out Detection
nal Calibrated RC Oscillator
rnal and Internal Interrupt Sources
Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, and
dby
ackages
rogrammable I/O Lines
ad PDIP, 32-lead TQFP, and 32-pad MLF
g Voltages
5.5V (ATmega8L)
5.5V (ATmega8)
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MHz (ATmega8L)
5 MHz (ATmega8)
onsumption at 4 Mhz, 3V, 25°C
ve: 3.6 mA
Mode: 1.0 mA
er-down Mode: 0.5 µA

ATMEL®

8-bit AVR® with 8K Bytes In-System Programmable Flash

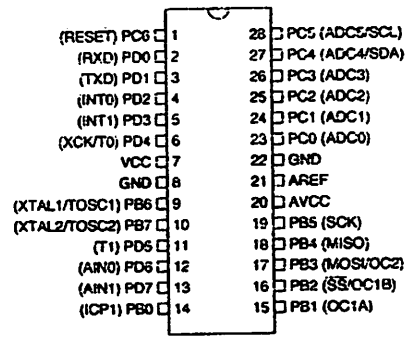
ATmega8
ATmega8L

2486O–AVR–10/04

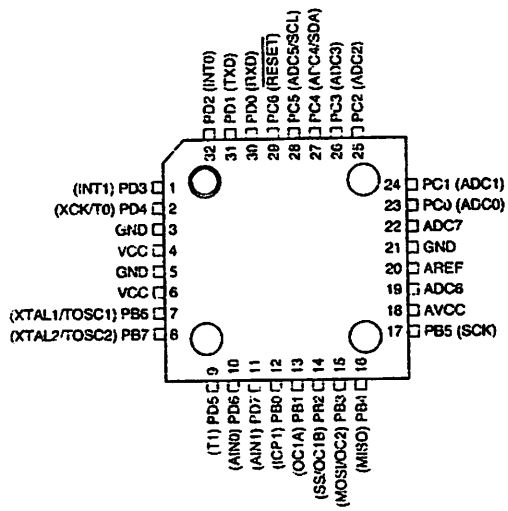
ATMEL

figurations

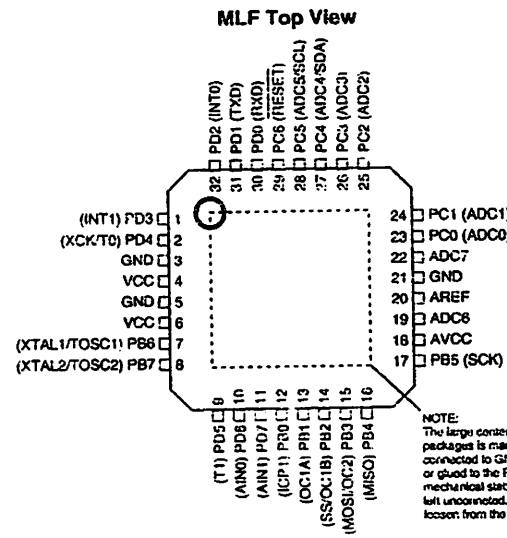
PDIP



TQFP Top View



MLF Top View



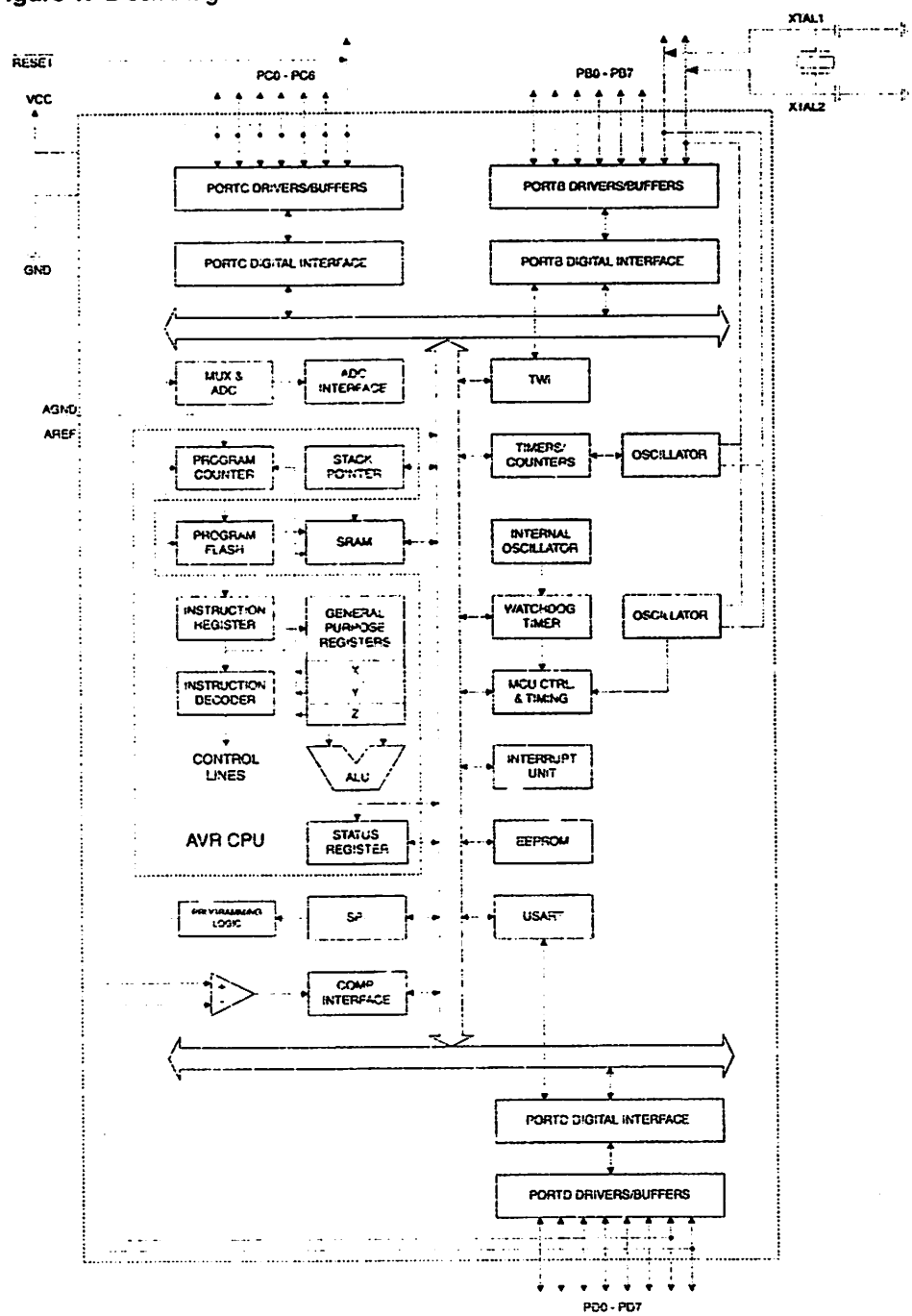
NOTE:
The large center pad underneath the MLF packages is made of metal and internally connected to GND. It should be soldered or glued to the PCB to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the PCB.

ew

The ATmega8 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8 achieves throughputs approaching 1 MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

iagram

Figure 1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8 provides the following features: 8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes of EEPROM, 1K byte of SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, a 6-channel ADC (eight channels in TQFP and MLF packages) with 10-bit accuracy, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next Interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The Flash Program memory can be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash Section will continue to run while the Application Flash Section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega8 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega8 AVR is supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, In-Circuit Emulators, and evaluation kits.

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

criptions

	Digital supply voltage.
	Ground.
37..PB0) AL2/TOSC1/TOSC2	Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running. Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit. Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier. If the Internal Calibrated RC Oscillator is used as chip clock source, PB7..6 is used as TOSC2..1 input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set. The various special features of Port B are elaborated in "Alternate Functions of Port B" on page 56 and "System Clock and Clock Options" on page 23.
C5..PC0)	Port C is an 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.
$\overline{\text{ET}}$	If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C. If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 36. Shorter pulses are not guaranteed to generate a Reset. The various special features of Port C are elaborated on page 59.
D7..PD0)	Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port D also serves the functions of various special features of the ATmega8 as listed on page 61.
	Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 36. Shorter pulses are not guaranteed to generate a reset.

AV_{CC} is the supply voltage pin for the A/D Converter, Port C (3..0), and ADC (7..6). It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. Note that Port C (5..4) use digital supply voltage, V_{CC}.

AREF is the analog reference pin for the A/D Converter.

TQFP and MLF Only)

In the TQFP and MLF package, ADC7..6 serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

Code les

This datasheet contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

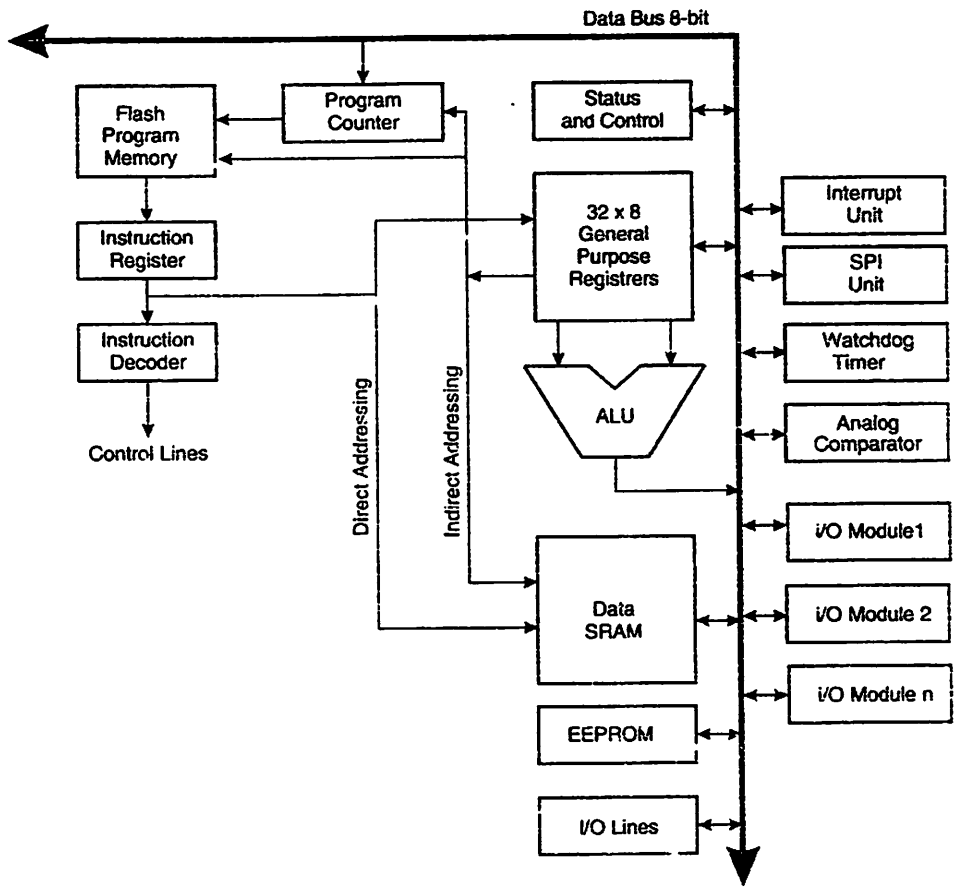
'U Core

tion

This section discusses the AVR core architecture in general. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals, and handle interrupts.

tural Overview

Figure 2. Block Diagram of the AVR MCU Architecture



In order to maximize performance and parallelism, the AVR uses a Harvard architecture – with separate memories and buses for program and data. Instructions in the Program memory are executed with a single level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the Program memory. This concept enables instructions to be executed in every clock cycle. The Program memory is In-System Reprogrammable Flash memory.

The fast-access Register File contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing – enabling efficient address calculations. One of the these address pointers can also be used as an address pointer for look up tables in Flash Program memory. These added function registers are the 16-bit X-, Y-, and Z-register, described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the Status Register is updated to reflect information about the result of the operation.

The Program flow is provided by conditional and unconditional jump and call instructions, able to directly address the whole address space. Most AVR instructions have a single 16-bit word format. Every Program memory address contains a 16- or 32-bit instruction.

Program Flash memory space is divided in two sections, the Boot program section and the Application program section. Both sections have dedicated Lock Bits for write and read/write protection. The SPM instruction that writes into the Application Flash memory section must reside in the Boot program section.

During interrupts and subroutine calls, the return address Program Counter (PC) is stored on the Stack. The Stack is effectively allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The Stack Pointer SP is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the Status Register. All interrupts have a separate Interrupt Vector in the Interrupt Vector table. The interrupts have priority in accordance with their Interrupt Vector position. The lower the Interrupt Vector address, the higher the priority.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, SPI, and other I/O functions. The I/O Memory can be accessed directly, or as the Data Space locations following those of the Register File, 0x20 - 0x5F.

'mega8 ies

This section describes the different memories in the ATmega8. The AVR architecture has two main memory spaces, the Data memory and the Program Memory space. In addition, the ATmega8 features an EEPROM Memory for data storage. All three memory spaces are linear and regular.

m ammable Flash ı Memory

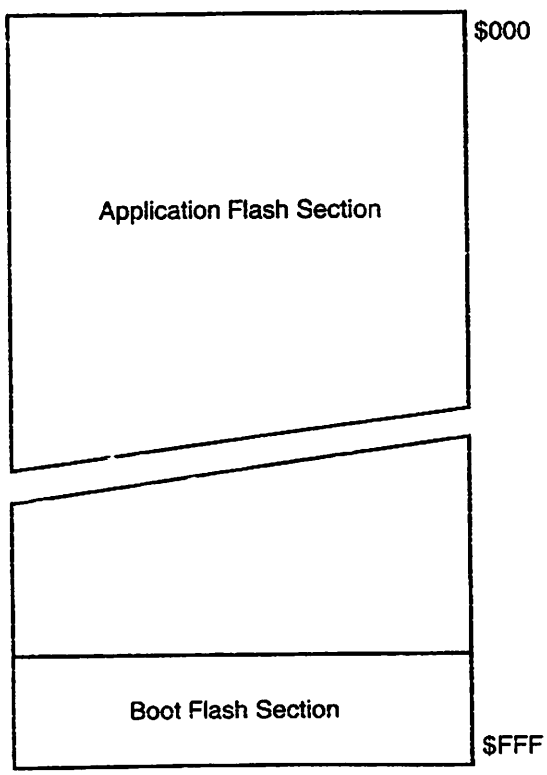
The ATmega8 contains 8K bytes On-chip In-System Reprogrammable Flash memory for program storage. Since all AVR instructions are 16- or 32-bits wide, the Flash is organized as 4K x 16 bits. For software security, the Flash Program memory space is divided into two sections, Boot Program section and Application Program section.

The Flash memory has an endurance of at least 10,000 write/erase cycles. The ATmega8 Program Counter (PC) is 12 bits wide, thus addressing the 4K Program memory locations. The operation of Boot Program section and associated Boot Lock Bits for software protection are described in detail in "Boot Loader Support – Read-While-Write Self-Programming" on page 206. "Memory Programming" on page 219 contains a detailed description on Flash Programming in SPI- or Parallel Programming mode.

Constant tables can be allocated within the entire Program memory address space (see the LPM – Load Program memory instruction description).

Timing diagrams for instruction fetch and execution are presented in "Instruction Execution Timing" on page 12.

Figure 7. Program Memory Map



ta Memory

Figure 8 shows how the ATmega8 SRAM Memory is organized.

The lower 1120 Data memory locations address the Register File, the I/O Memory, and the internal data SRAM. The first 96 locations address the Register File and I/O Memory, and the next 1024 locations address the internal data SRAM.

The five different addressing modes for the Data memory cover: Direct, Indirect with Displacement, Indirect, Indirect with Pre-decrement, and Indirect with Post-increment. In the Register File, registers R26 to R31 feature the indirect addressing pointer registers.

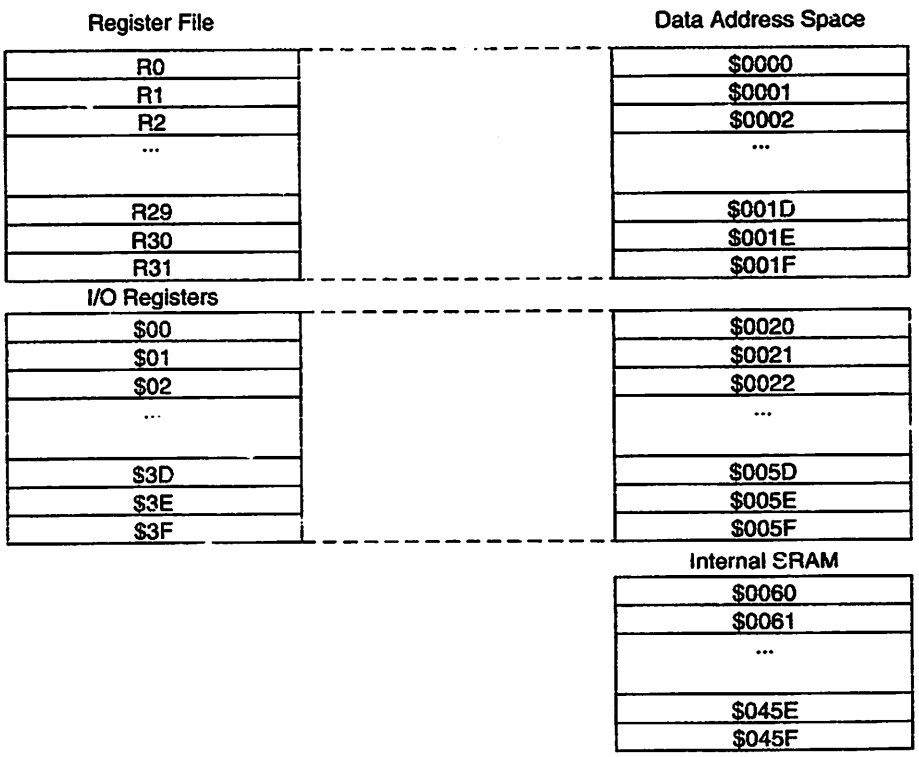
The direct addressing reaches the entire data space.

The Indirect with Displacement mode reaches 63 address locations from the base address given by the Y- or Z-register.

When using register indirect addressing modes with automatic pre-decrement and post-increment, the address registers X, Y and Z are decremented or incremented.

The 32 general purpose working registers, 64 I/O Registers, and the 1024 bytes of internal data SRAM in the ATmega8 are all accessible through all these addressing modes. The Register File is described in "General Purpose Register File" on page 10.

Figure 8. Data Memory Map



tic Logic Unit –

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed. The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions. Some implementations of the architecture also provide a powerful multiplier supporting both signed/unsigned multiplication and fractional format. See the "Instruction Set" section for a detailed description.

Register

The Status Register contains information about the result of the most recently executed arithmetic instruction. This information can be used for altering program flow in order to perform conditional operations. Note that the Status Register is updated after all ALU operations, as specified in the Instruction Set Reference. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt. This must be handled by software.

The AVR Status Register – SREG – is defined as:

Bit	7	6	5	4	3	2	1	0	
	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – I: Global Interrupt Enable**

The Global Interrupt Enable bit must be set for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers. If the Global Interrupt Enable Register is cleared, none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred, and is set by the RETI instruction to enable subsequent interrupts. The I-bit can also be set and cleared by the application with the SEI and CLI instructions, as described in the Instruction Set Reference.

- **Bit 6 – T: Bit Copy Storage**

The Bit Copy instructions BLD (Bit LoaD) and BST (Bit STore) use the T-bit as source or destination for the operated bit. A bit from a register in the Register File can be copied into T by the BST instruction, and a bit in T can be copied into a bit in a register in the Register File by the BLD instruction.

- **Bit 5 – H: Half Carry Flag**

The Half Carry Flag H indicates a Half Carry in some arithmetic operations. Half Carry is useful in BCD arithmetic. See the "Instruction Set Description" for detailed information.

- **Bit 4 – S: Sign Bit, S = N ⊖ V**

The S-bit is always an exclusive or between the Negative Flag N and the Two's Complement Overflow Flag V. See the "Instruction Set Description" for detailed information.

- **Bit 3 – V: Two's Complement Overflow Flag**

The Two's Complement Overflow Flag V supports two's complement arithmetics. See the "Instruction Set Description" for detailed information.

- **Bit 2 – N: Negative Flag**

The Negative Flag N indicates a negative result in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

- **Bit 1 – Z: Zero Flag**

The Zero Flag Z indicates a zero result in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

- **Bit 0 – C: Carry Flag**

The Carry Flag C indicates a Carry in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

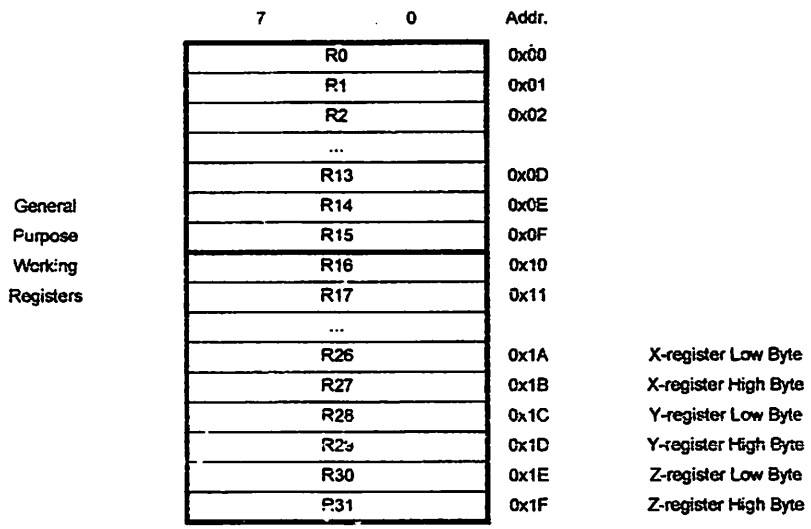
Purpose r File

The Register File is optimized for the AVR Enhanced RISC instruction set. In order to achieve the required performance and flexibility, the following input/output schemes are supported by the Register File:

- One 8-bit output operand and one 8-bit result input.
- Two 8-bit output operands and one 8-bit result input.
- Two 8-bit output operands and one 16-bit result input.
- One 16-bit output operand and one 16-bit result input.

Figure 3 shows the structure of the 32 general purpose working registers in the CPU.

Figure 3. AVR CPU General Purpose Working Registers



Most of the instructions operating on the Register File have direct access to all registers, and most of them are single cycle instructions.

As shown in Figure 3, each register is also assigned a Data memory address, mapping them directly into the first 32 locations of the user Data Space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y-, and Z-pointer Registers can be set to index any register in the file.

Keep the AVR RESET active (low) during periods of insufficient power supply voltage. This can be done by enabling the internal Brown-out Detector (BOD). If the detection level of the internal BOD does not match the needed detection level, an external low V_{CC} Reset Protection circuit can be used. If a reset occurs while a write operation is in progress, the write operation will be completed provided that the power supply voltage is sufficient.

ory

The I/O space definition of the ATmega8 is shown in "" on page 284.

All ATmega8 I/Os and peripherals are placed in the I/O space. The I/O locations are accessed by the IN and OUT instructions, transferring data between the 32 general purpose working registers and the I/O space. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Refer to the instruction set section for more details. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses.

For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

Some of the Status Flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

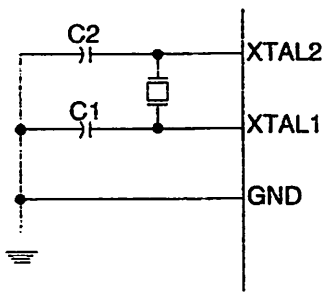
The I/O and Peripherals Control Registers are explained in later sections.

Oscillator

XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier which can be configured for use as an On-chip Oscillator, as shown in Figure 11. Either a quartz crystal or a ceramic resonator may be used. The CKOPT Fuse selects between two different Oscillator amplifier modes. When CKOPT is programmed, the Oscillator output will oscillate a full rail-to-rail swing on the output. This mode is suitable when operating in a very noisy environment or when the output from XTAL2 drives a second clock buffer. This mode has a wide frequency range. When CKOPT is unprogrammed, the Oscillator has a smaller output swing. This reduces power consumption considerably. This mode has a limited frequency range and it cannot be used to drive other clock buffers.

For resonators, the maximum frequency is 8 MHz with CKOPT unprogrammed and 16 MHz with CKOPT programmed. C1 and C2 should always be equal for both crystals and resonators. The optimal value of the capacitors depends on the crystal or resonator in use, the amount of stray capacitance, and the electromagnetic noise of the environment. Some initial guidelines for choosing capacitors for use with crystals are given in Table 4. For ceramic resonators, the capacitor values given by the manufacturer should be used.

Figure 11. Crystal Oscillator Connections



The Oscillator can operate in three different modes, each optimized for a specific frequency range. The operating mode is selected by the fuses CKSEL3..1 as shown in Table 4.

Table 4. Crystal Oscillator Operating Modes

CKOPT	CKSEL3..1	Frequency Range(MHz)	Recommended Range for Capacitors C1 and C2 for Use with Crystals (pF)
1	101[1]	0.4 - 0.9	–
1	110	0.9 - 3.0	12 - 22
1	111	3.0 - 8.0	12 - 22
0	101, 110, 111	1.0 ≤	12 - 22

Note: 1. This option should not be used with crystals, only with ceramic resonators.

The CKSEL0 Fuse together with the SUT1..0 Fuses select the start-up times as shown in Table 5.

Table 5. Start-up Times for the Crystal Oscillator Clock Selection

CKSEL0	SUT1..0	Start-up Time from Power-down and Power-save	Additional Delay from Reset (V_{CC} = 5.0V)	Recommended Usage
0	00	258 CK[1]	4.1 ms	Ceramic resonator, fast rising power
0	01	258 CK[1]	65 ms	Ceramic resonator, slowly rising power
0	10	1K CK[2]	–	Ceramic resonator, BOD enabled
0	11	1K CK[2]	4.1 ms	Ceramic resonator, fast rising power
1	00	1K CK[2]	65 ms	Ceramic resonator, slowly rising power
1	01	16K CK	–	Crystal Oscillator, BOD enabled
1	10	16K CK	4.1 ms	Crystal Oscillator, fast rising power
1	11	16K CK	65 ms	Crystal Oscillator, slowly rising power

Notes: 1. These options should only be used when not operating close to the maximum frequency of the device, and only if frequency stability at start-up is not important for the application. These options are not suitable for crystals.
2. These options are intended for use with ceramic resonators and will ensure frequency stability at start-up. They can also be used with crystals when not operating close to the maximum frequency of the device, and if frequency stability at start-up is not important for the application.

quency Crystal tor

To use a 32.768 kHz watch crystal as the clock source for the device, the Low-frequency Crystal Oscillator must be selected by setting the CKSEL Fuses to "1001". The crystal should be connected as shown in Figure 11. By programming the CKOPT Fuse, the user can enable internal capacitors on XTAL1 and XTAL2, thereby removing the need for external capacitors. The internal capacitors have a nominal value of 36 pF.

When this Oscillator is selected, start-up times are determined by the SUT Fuses as shown in Table 6.

Table 6. Start-up Times for the Low-frequency Crystal Oscillator Clock Selection

SUT1..0	Start-up Time from Power-down and Power-save	Additional Delay from Reset (V_{CC} = 5.0V)	Recommended Usage
00	1K CK[1]	4.1 ms	Fast rising power or BOD enabled
01	1K CK[1]	65 ms	Slowly rising power
10	32K CK	65 ms	Stable frequency at start-up
11	Reserved		

Note: 1. These options should only be used if frequency stability at start-up is not important for the application.

ed Internal RC or

The calibrated internal RC Oscillator provides a fixed 1.0, 2.0, 4.0, or 8.0 MHz clock. All frequencies are nominal values at 5V and 25°C. This clock may be selected as the system clock by programming the CKSEL Fuses as shown in Table 9. If selected, it will operate with no external components. The CKOPT Fuse should always be unprogrammed when using this clock option. During reset, hardware loads the 1 MHz calibration byte into the OSCCAL Register and thereby automatically calibrates the RC Oscillator. At 5V, 25°C and 1.0 MHz Oscillator frequency selected, this calibration gives a frequency within ± 3% of the nominal frequency. Using run-time calibration methods as described in application notes available at www.atmel.com/avr it is possible to achieve ± 1% accuracy at any given V_{CC} and Temperature. When this Oscillator is used as the chip clock, the Watchdog Oscillator will still be used for the Watchdog Timer and for the Reset Time-out. For more information on the pre-programmed calibration value, see the section "Calibration Byte" on page 222.

Table 9. Internal Calibrated RC Oscillator Operating Modes

CKSEL3..0	Nominal Frequency (MHz)
0001[1]	1.0
0010	2.0
0011	4.0
0100	8.0

Note: 1. The device is shipped with this option selected.

When this Oscillator is selected, start-up times are determined by the SUT Fuses as shown in Table 10. PB6 (XTAL1/TOSC1) and PB7(XTAL2/TOSC2) can be used as either general I/O pins or Timer Oscillator pins..

Table 10. Start-up Times for the Internal Calibrated RC Oscillator Clock Selection

SUT1..0	Start-up Time from Power-down and Power-save	Additional Delay from Reset (V_{CC} = 5.0V)	Recommended Usage
00	6 CK	–	BOD enabled
01	6 CK	4.1 ms	Fast rising power
10[1]	6 CK	65 ms	Slowly rising power
11	Reserved		

Note: 1. The device is shipped with this option selected.

Management ep Modes

Sleep modes enable the application to shut down unused modules in the MCU, thereby saving power. The AVR provides various sleep modes allowing the user to tailor the power consumption to the application's requirements.

To enter any of the five sleep modes, the SE bit in MCUCR must be written to logic one and a SLEEP instruction must be executed. The SM2, SM1, and SM0 bits in the MCUCR Register select which sleep mode (Idle, ADC Noise Reduction, Power-down, Power-save, or Standby) will be activated by the SLEEP instruction. See Table 13 for a summary. If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU wakes up. The MCU is then halted for four cycles in addition to the start-up time, it executes the interrupt routine, and resumes execution from the instruction following SLEEP. The contents of the Register File and SRAM are unaltered when the device wakes up from sleep. If a reset occurs during sleep mode, the MCU wakes up and executes from the Reset Vector.

Note that the Extended Standby mode present in many other AVR MCUs has been removed in the ATmega8, as the TOSC and XTAL inputs share the same physical pins.

Figure 10 on page 23 presents the different clock systems in the ATmega8, and their distribution. The figure is helpful in selecting an appropriate sleep mode.

trol Register –

The MCU Control Register contains control bits for power management.

Bit	7	6	5	4	3	2	1	0	
	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	MCUCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – SE: Sleep Enable**

The SE bit must be written to logic one to make the MCU enter the sleep mode when the SLEEP instruction is executed. To avoid the MCU entering the sleep mode unless it is the programmer's purpose, it is recommended to set the Sleep Enable (SE) bit just before the execution of the SLEEP instruction.

- **Bits 6..4 – SM2..0: Sleep Mode Select Bits 2, 1, and 0**

These bits select between the five available sleep modes as shown in Table 13.

Table 13. Sleep Mode Select

SM2	SM1	SM0	Sleep Mode
0	0	0	Idle
0	0	1	ADC Noise Reduction
0	1	0	Power-down
0	1	1	Power-save
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Standby(1)

Note: 1. Standby mode is only available with external crystals or resonators.

ts

This section describes the specifics of the interrupt handling performed by the ATmega8. For a general explanation of the AVR interrupt handling, refer to "Reset and Interrupt Handling" on page 12.

Vectors in

Table 18. Reset and Interrupt Vectors

Vector No.	Program Address[2]	Source	Interrupt Definition
1	0x000[1]	RESET	External Pin, Power-on Reset, Brown-out Reset, and Watchdog Reset
2	0x001	INT0	External Interrupt Request 0
3	0x002	INT1	External Interrupt Request 1
4	0x003	TIMER2 COMP	Timer/Counter2 Compare Match
5	0x004	TIMER2 OVF	Timer/Counter2 Overflow
6	0x005	TIMER1 CAPT	Timer/Counter1 Capture Event
7	0x006	TIMER1 COMPA	Timer/Counter1 Compare Match A
8	0x007	TIMER1 COMPB	Timer/Counter1 Compare Match B
9	0x008	TIMER1 OVF	Timer/Counter1 Overflow
10	0x009	TIMER0 OVF	Timer/Counter0 Overflow
11	0x00A	SPI, STC	Serial Transfer Complete
12	0x00B	USART, RXC	USART, Rx Complete
13	0x00C	USART, UDRE	USART Data Register Empty
14	0x00D	USART, TXC	USART, Tx Complete
15	0x00E	ADC	ADC Conversion Complete
16	0x00F	EE_RDY	EEPROM Ready
17	0x010	ANA_COMP	Analog Comparator
18	0x011	TWI	Two-wire Serial Interface
19	0x012	SPM_RDY	Store Program Memory Ready

Notes: 1. When the BOOTRST Fuse is programmed, the device will jump to the Boot Loader address at reset, see "Boot Loader Support – Read-While-Write Self-Programming" on page 206.

2. When the IVSEL bit in GICR is set, Interrupt Vectors will be moved to the start of the boot Flash section. The address of each Interrupt Vector will then be the address in this table added to the start address of the boot Flash section.

Table 19 shows reset and Interrupt Vectors placement for the various combinations of BOOTRST and IVSEL settings. If the program never enables an interrupt source, the Interrupt Vectors are not used, and regular program code can be placed at these locations. This is also the case if the Reset Vector is in the Application section while the Interrupt Vectors are in the boot section or vice versa.

al Interrupts

The external interrupts are triggered by the INT0, and INT1 pins. Observe that, if enabled, the interrupts will trigger even if the INT0..1 pins are configured as outputs. This feature provides a way of generating a software interrupt. The external interrupts can be triggered by a falling or rising edge or a low level. This is set up as indicated in the specification for the MCU Control Register – MCUCR. When the external interrupt is enabled and is configured as level triggered, the interrupt will trigger as long as the pin is held low. Note that recognition of falling or rising edge interrupts on INT0 and INT1 requires the presence of an I/O clock, described in "Clock Systems and their Distribution" on page 23. Low level interrupts on INT0/INT1 are detected asynchronously. This implies that these interrupts can be used for waking the part also from sleep modes other than Idle mode. The I/O clock is halted in all sleep modes except Idle mode.

Note that if a level triggered interrupt is used for wake-up from Power-down mode, the changed level must be held for some time to wake up the MCU. This makes the MCU less sensitive to noise. The changed level is sampled twice by the Watchdog Oscillator clock. The period of the Watchdog Oscillator is 1 µs (nominal) at 5.0V and 25°C. The frequency of the Watchdog Oscillator is voltage dependent as shown in "Electrical Characteristics" on page 239. The MCU will wake up if the input has the required level during this sampling or if it is held until the end of the start-up time. The start-up time is defined by the SUT Fuses as described in "System Clock and Clock Options" on page 23. If the level is sampled twice by the Watchdog Oscillator clock but disappears before the end of the start-up time, the MCU will still wake up, but no interrupt will be generated. The required level must be held long enough for the MCU to complete the wake up to trigger the level interrupt.

ıtrol Register –

The MCU Control Register contains control bits for interrupt sense control and general MCU functions.

Bit	7	6	5	4	3	2	1	0	
	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	MCUCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 3, 2 – ISC11, ISC10: Interrupt Sense Control 1 Bit 1 and Bit 0**

The External Interrupt 1 is activated by the external pin INT1 if the SREG I-bit and the corresponding interrupt mask in the GICR are set. The level and edges on the external INT1 pin that activate the interrupt are defined in Table 31. The value on the INT1 pin is sampled before detecting edges. If edge or toggle interrupt is selected, pulses that last longer than one clock period will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt. If low level interrupt is selected, the low level must be held until the completion of the currently executing instruction to generate an interrupt.

Table 31. Interrupt 1 Sense Control

ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Any logical change on INT1 generates an interrupt request.
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.

- **Bit 1, 0 – ISC01, ISC00: Interrupt Sense Control 0 Bit 1 and Bit 0**

The External Interrupt 0 is activated by the external pin INT0 if the SREG I-flag and the corresponding interrupt mask are set. The level and edges on the external INT0 pin that activate the interrupt are defined in Table 32. The value on the INT0 pin is sampled before detecting edges. If edge or toggle interrupt is selected, pulses that last longer than one clock period will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt. If low level interrupt is selected, the low level must be held until the completion of the currently executing instruction to generate an interrupt.

Table 32. Interrupt 0 Sense Control

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Any logical change on INT0 generates an interrupt request.
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

Interrupt Control – GICR

Bit	7	6	5	4	3	2	1	0	
	INT1	INT0	–	–	–	–	IVSEL	IVCE	GICR
Read/Write	R/W	R/W	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – INT1: External Interrupt Request 1 Enable**

When the INT1 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the external pin interrupt is enabled. The Interrupt Sense Control1 bits 1/0 (ISC11 and ISC10) in the MCU general Control Register (MCUCR) define whether the external interrupt is activated on rising and/or falling edge of the INT1 pin or level sensed. Activity on the pin will cause an interrupt request even if INT1 is configured as an output. The corresponding interrupt of External Interrupt Request 1 is executed from the INT1 Interrupt Vector.

- **Bit 6 – INT0: External Interrupt Request 0 Enable**

When the INT0 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the external pin interrupt is enabled. The Interrupt Sense Control0 bits 1/0 (ISC01 and ISC00) in the MCU general Control Register (MCUCR) define whether the external interrupt is activated on rising and/or falling edge of the INT0 pin or level sensed. Activity on the pin will cause an interrupt request even if INT0 is configured as an output. The corresponding interrupt of External Interrupt Request 0 is executed from the INT0 Interrupt Vector.

terrupt Flag
· GIFR

Bit	7	6	5	4	3	2	1	0	
	INTF1	INTF0	–	–	–	–	–	–	GIFR
Read/Write	R/W	R/W	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – INTF1: External Interrupt Flag 1**

When an event on the INT1 pin triggers an interrupt request, INTF1 becomes set (one). If the I-bit in SREG and the INT1 bit in GICR are set (one), the MCU will jump to the corresponding Interrupt Vector. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical one to it. This flag is always cleared when INT1 is configured as a level interrupt.

- **Bit 6 – INTF0: External Interrupt Flag 0**

When an event on the INT0 pin triggers an interrupt request, INTF0 becomes set (one). If the I-bit in SREG and the INT0 bit in GICR are set (one), the MCU will jump to the corresponding Interrupt Vector. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical one to it. This flag is always cleared when INT0 is configured as a level interrupt.

imer/Counter2 WM and hronous tion

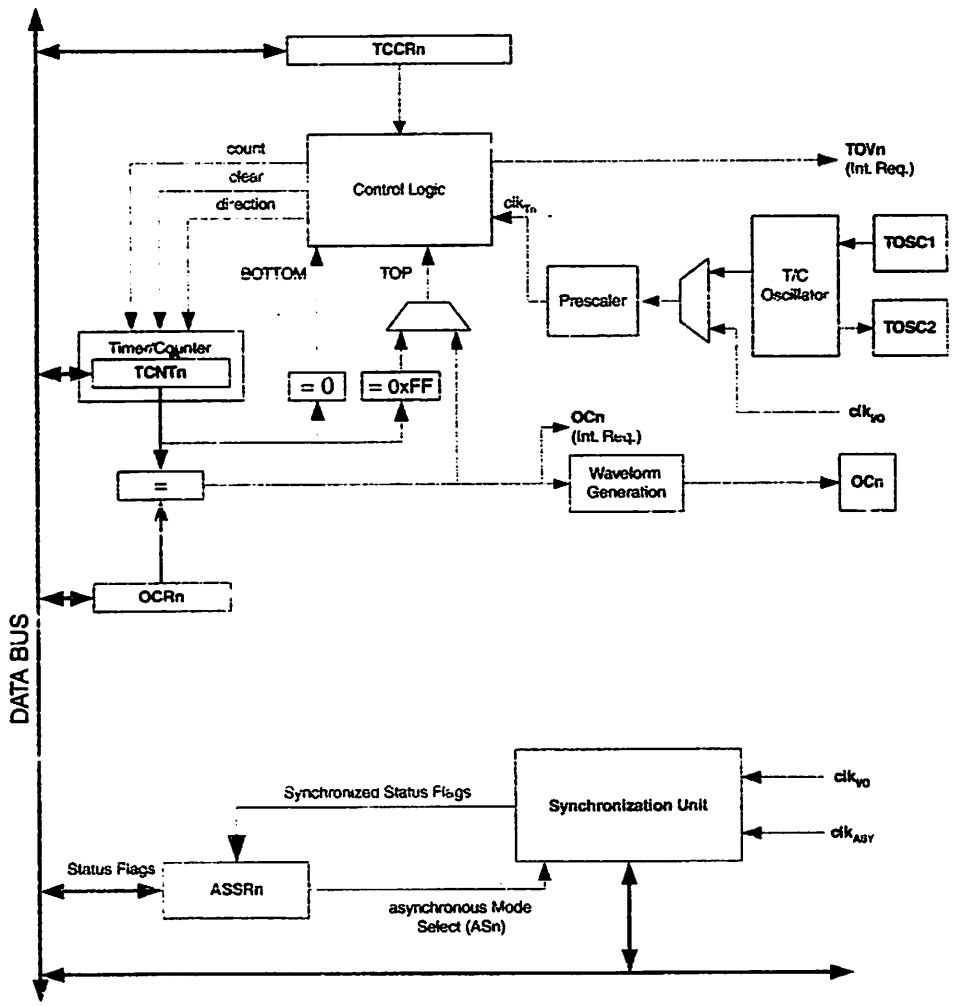
Timer/Counter2 is a general purpose, single channel, 8-bit Timer/Counter module. The main features are:

- **Single Channel Counter**
- **Clear Timer on Compare Match (Auto Reload)**
- **Glitch-free, phase Correct Pulse Width Modulator (PWM)**
- **Frequency Generator**
- **10-bit Clock Prescaler**
- **Overflow and Compare Match Interrupt Sources (TOV2 and OCF2)**
- **Allows Clocking from External 32 kHz Watch Crystal Independent of the I/O Clock**

ew

A simplified block diagram of the 8-bit Timer/Counter is shown in Figure 45. For the actual placement of I/O pins, refer to "Pin Configurations" on page 2. CPU accessible I/O Registers, including I/O bits and I/O pins, are shown in bold. The device-specific I/O Register and bit locations are listed in the "8-bit Timer/Counter Register Description" on page 115.

Figure 45. 8-bit Timer/Counter Block Diagram



The Timer/Counter (TCNT2) and Output Compare Register (OCR2) are 8-bit registers. Interrupt request (shorten as Int.Req.) signals are all visible in the Timer Interrupt Flag Register (TIFR). All interrupts are individually masked with the Timer Interrupt Mask Register (TIMSK). TIFR and TIMSK are not shown in the figure since these registers are shared by other timer units.

The Timer/Counter can be clocked internally, via the prescaler, or asynchronously clocked from the TOSC1/2 pins, as detailed later in this section. The asynchronous operation is controlled by the Asynchronous Status Register (ASSR). The Clock Select logic block controls which clock source the Timer/Counter uses to increment (or decrement) its value. The Timer/Counter is inactive when no clock source is selected. The output from the clock select logic is referred to as the timer clock (clk_{T2}).

The double buffered Output Compare Register (OCR2) is compared with the Timer/Counter value at all times. The result of the compare can be used by the waveform generator to generate a PWM or variable frequency output on the Output Compare Pin (OC2). For details, see "Output Compare Unit" on page 105. The Compare Match event will also set the Compare Flag (OCF2) which can be used to generate an Output Compare interrupt request.

Many register and bit references in this document are written in general form. A lower case "n" replaces the Timer/Counter number, in this case 2. However, when using the register or bit defines in a program, the precise form must be used (i.e., TCNT2 for accessing Timer/Counter2 counter value and so on).

The definitions in Table 41 are also used extensively throughout the document.

Table 41. Definitions

BOTTOM	The counter reaches the BOTTOM when it becomes zero (0x00).
MAX	The counter reaches its MAXimum when it becomes 0xFF (decimal 255).
TOP	The counter reaches the TOP when it becomes equal to the highest value in the count sequence. The TOP value can be assigned to be the fixed value 0xFF (MAX) or the value stored in the OCR2 Register. The assignment is dependent on the mode of operation.

unter Clock

The Timer/Counter can be clocked by an internal synchronous or an external asynchronous clock source. The clock source clk_{T2} is by default equal to the MCU clock, $clk_{I/O}$. When the AS2 bit in the ASSR Register is written to logic one, the clock source is taken from the Timer/Counter Oscillator connected to TOSC1 and TOSC2. For details on asynchronous operation, see "Asynchronous Status Register – ASSR" on page 117. For details on clock sources and prescaler, see "Timer/Counter Prescaler" on page 121.

ıer/Counter
· Description

ınter Control
- TCCR2

Bit	7	6	5	4	3	2	1	0	
	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	TCCR2
Read/Write	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – FOC2: Force Output Compare**

The FOC2 bit is only active when the WGM bits specify a non-PWM mode. However, for ensuring compatibility with future devices, this bit must be set to zero when TCCR2 is written when operating in PWM mode. When writing a logical one to the FOC2 bit, an immediate Compare Match is forced on the waveform generation unit. The OC2 output is changed according to its COM21:0 bits setting. Note that the FOC2 bit is implemented as a strobe. Therefore it is the value present in the COM21:0 bits that determines the effect of the forced compare.

A FOC2 strobe will not generate any interrupt, nor will it clear the timer in CTC mode using OCR2 as TOP.

The FOC2 bit is always read as zero.

- **Bit 6,3 – WGM21:0: Waveform Generation Mode**

These bits control the counting sequence of the counter, the source for the maximum (TOP) counter value, and what type of waveform generation to be used. Modes of operation supported by the Timer/Counter unit are: Normal mode, Clear Timer on Compare Match (CTC) mode, and two types of Pulse Width Modulation (PWM) modes. See Table 42 and "Modes of Operation" on page 108.

Table 42. Waveform Generation Mode Bit Description

Mode	WGM21 (CTC2)	WGM20 (PWM2)	Timer/Counter Mode of Operation[1]	TOP	Update of OCR2	TOV2 Flag Set
0	0	0	Normal	0xFF	Immediate	MAX
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	1	0	CTC	OCR2	Immediate	MAX
3	1	1	Fast PWM	0xFF	TOP	MAX

Note: 1. The CTC2 and PWM2 bit definition names are now obsolete. Use the WGM21:0 definitions. However, the functionality and location of these bits are compatible with previous versions of the timer.

- **Bit 5:4 – COM21:0: Compare Match Output Mode**

These bits control the Output Compare Pin (OC2) behavior. If one or both of the COM21:0 bits are set, the OC2 output overrides the normal port functionality of the I/O pin it is connected to. However, note that the Data Direction Register (DDR) bit corresponding to OC2 pin must be set in order to enable the output driver.

When OC2 is connected to the pin, the function of the COM21:0 bits depends on the WGM21:0 bit setting. Table 43 shows the COM21:0 bit functionality when the WGM21:0 bits are set to a normal or CTC mode (non-PWM).

Table 43. Compare Output Mode, Non-PWM Mode

COM21	COM20	Description
0	0	Normal port operation, OC2 disconnected.
0	1	Toggle OC2 on Compare Match
1	0	Clear OC2 on Compare Match
1	1	Set OC2 on Compare Match

Table 44 shows the COM21:0 bit functionality when the WGM21:0 bits are set to fast PWM mode.

Table 44. Compare Output Mode, Fast PWM Mode[1]

COM21	COM20	Description
0	0	Normal port operation, OC2 disconnected.
0	1	Reserved
1	0	Clear OC2 on Compare Match, set OC2 at TOP
1	1	Set OC2 on Compare Match, clear OC2 at TOP

Note: 1. A special case occurs when OCR2 equals TOP and COM21 is set. In this case, the Compare Match is ignored, but the set or clear is done at TOP. See "Fast PWM Mode" on page 110 for more details.

Table 45 shows the COM21:0 bit functionality when the WGM21:0 bits are set to phase correct PWM mode.

Table 45. Compare Output Mode, Phase Correct PWM Mode[1]

COM21	COM20	Description
0	0	Normal port operation, OC2 disconnected.
0	1	Reserved
1	0	Clear OC2 on Compare Match when up-counting. Set OC2 on Compare Match when downcounting.
1	1	Set OC2 on Compare Match when up-counting. Clear OC2 on Compare Match when downcounting.

Note: 1. A special case occurs when OCR2 equals TOP and COM21 is set. In this case, the Compare Match is ignored, but the set or clear is done at TOP. See "Phase Correct PWM Mode" on page 111 for more details.

- **Bit 2:0 – CS22:0: Clock Select**

The three clock select bits select the clock source to be used by the Timer/Counter, see Table 46.

Table 46. Clock Select Bit Description

CS22	CS21	CS20	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	clk_{T2S}/(No prescaling)
0	1	0	clk_{T2S}/8 (From prescaler)
0	1	1	clk_{T2S}/32 (From prescaler)
1	0	0	clk_{T2S}/64 (From prescaler)
1	0	1	clk_{T2S}/128 (From prescaler)
1	1	0	clk_{T2S}/256 (From prescaler)
1	1	1	clk_{T2S}/1024 (From prescaler)

nter Register –

Bit	7	6	5	4	3	2	1	0	
	TCNT2[7:0]								TCNT2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Timer/Counter Register gives direct access, both for read and write operations, to the Timer/Counter unit 8-bit counter. Writing to the TCNT2 Register blocks (removes) the Compare Match on the following timer clock. Modifying the counter (TCNT2) while the counter is running, introduces a risk of missing a Compare Match between TCNT2 and the OCR2 Register.

npare Register –

Bit	7	6	5	4	3	2	1	0	
	OCR2[7:0]								OCR2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Output Compare Register contains an 8-bit value that is continuously compared with the counter value (TCNT2). A match can be used to generate an Output Compare interrupt, or to generate a waveform output on the OC2 pin.

ɔnous Operation ner/Counter

ous Status ASSR

Bit	7	6	5	4	3	2	1	0	
	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	ASSR
Read/Write	R	R	R	R	R/W	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 3 – AS2: Asynchronous Timer/Counter2**

When AS2 is written to zero, Timer/Counter 2 is clocked from the I/O clock, $clk_{I/O}$. When AS2 is written to one, Timer/Counter 2 is clocked from a crystal Oscillator connected to the Timer Oscillator 1 (TOSC1) pin. When the value of AS2 is changed, the contents of TCNT2, OCR2, and TCCR2 might be corrupted.

- **Bit 2 – TCN2UB: Timer/Counter2 Update Busy**

When Timer/Counter2 operates asynchronously and TCNT2 is written, this bit becomes set. When TCNT2 has been updated from the temporary storage register, this bit is cleared by hardware. A logical zero in this bit indicates that TCNT2 is ready to be updated with a new value.

- **Bit 1 – OCR2UB: Output Compare Register2 Update Busy**

When Timer/Counter2 operates asynchronously and OCR2 is written, this bit becomes set. When OCR2 has been updated from the temporary storage register, this bit is cleared by hardware. A logical zero in this bit indicates that OCR2 is ready to be updated with a new value.

- **Bit 0 – TCR2UB: Timer/Counter Control Register2 Update Busy**

When Timer/Counter2 operates asynchronously and TCCR2 is written, this bit becomes set. When TCCR2 has been updated from the temporary storage register, this bit is cleared by hardware. A logical zero in this bit indicates that TCCR2 is ready to be updated with a new value.

If a write is performed to any of the three Timer/Counter2 Registers while its update busy flag is set, the updated value might get corrupted and cause an unintentional interrupt to occur.

The mechanisms for reading TCNT2, OCR2, and TCCR2 are different. When reading TCNT2, the actual timer value is read. When reading OCR2 or TCCR2, the value in the temporary storage register is read.

ıous Operation of inter2

When Timer/Counter2 operates asynchronously, some considerations must be taken.

- Warning: When switching between asynchronous and synchronous clocking of Timer/Counter2, the Timer Registers TCNT2, OCR2, and TCCR2 might be corrupted. A safe procedure for switching clock source is:
  1. Disable the Timer/Counter2 interrupts by clearing OCIE2 and TOIE2.
  2. Select clock source by setting AS2 as appropriate.
  3. Write new values to TCNT2, OCR2, and TCCR2.
  4. To switch to asynchronous operation: Wait for TCN2UB, OCR2UB, and TCR2UB.
  5. Clear the Timer/Counter2 Interrupt Flags.
  6. Enable interrupts, if needed.
- The Oscillator is optimized for use with a 32.768 kHz watch crystal. Applying an external clock to the TOSC1 pin may result in incorrect Timer/Counter2 operation. The CPU main clock frequency must be more than four times the Oscillator frequency.
- When writing to one of the registers TCNT2, OCR2, or TCCR2, the value is transferred to a temporary register, and latched after two positive edges on TOSC1. The user should not write a new value before the contents of the temporary register have been transferred to its destination. Each of the three mentioned registers have their individual temporary register, which means that e.g. writing to TCNT2 does not disturb an OCR2 write in progress. To detect that a transfer to the destination register has taken place, the Asynchronous Status Register – ASSR has been implemented.
- When entering Power-save mode after having written to TCNT2, OCR2, or TCCR2, the user must wait until the written register has been updated if Timer/Counter2 is used to wake up the device. Otherwise, the MCU will enter sleep mode before the

changes are effective. This is particularly important if the Output Compare2 interrupt is used to wake up the device, since the Output Compare function is disabled during writing to OCR2 or TCNT2. If the write cycle is not finished, and the MCU enters sleep mode before the OCR2UB bit returns to zero, the device will never receive a Compare Match interrupt, and the MCU will not wake up.

- If Timer/Counter2 is used to wake the device up from Power-save mode, precautions must be taken if the user wants to re-enter one of these modes: The interrupt logic needs one TOSC1 cycle to be reset. If the time between wake-up and re-entering sleep mode is less than one TOSC1 cycle, the interrupt will not occur, and the device will fail to wake up. If the user is in doubt whether the time before re-entering Power-save or Extended Standby mode is sufficient, the following algorithm can be used to ensure that one TOSC1 cycle has elapsed:
  1. Write a value to TCCR2, TCNT2, or OCR2.
  2. Wait until the corresponding Update Busy Flag in ASSR returns to zero.
  3. Enter Power-save or Extended Standby mode.
- When the asynchronous operation is selected, the 32.768 kHZ Oscillator for Timer/Counter2 is always running, except in Power-down and Standby modes. After a Power-up Reset or Wake-up from Power-down or Standby mode, the user should be aware of the fact that this Oscillator might take as long as one second to stabilize. The user is advised to wait for at least one second before using Timer/Counter2 after Power-up or Wake-up from Power-down or Standby mode. The contents of all Timer/Counter2 Registers must be considered lost after a wake-up from Power-down or Standby mode due to unstable clock signal upon start-up, no matter whether the Oscillator is in use or a clock signal is applied to the TOSC1 pin.
- Description of wake up from Power-save or Extended Standby mode when the timer is clocked asynchronously: When the interrupt condition is met, the wake up process is started on the following cycle of the timer clock, that is, the timer is always advanced by at least one before the processor can read the counter value. After wake-up, the MCU is halted for four cycles, it executes the interrupt routine, and resumes execution from the instruction following SLEEP.
- Reading of the TCNT2 Register shortly after wake-up from Power-save may give an incorrect result. Since TCNT2 is clocked on the asynchronous TOSC clock, reading TCNT2 must be done through a register synchronized to the internal I/O clock domain. Synchronization takes place for every rising TOSC1 edge. When waking up from Power-save mode, and the I/O clock ($clk_{I/O}$) again becomes active, TCNT2 will read as the previous value (before entering sleep) until the next rising TOSC1 edge. The phase of the TOSC clock after waking up from Power-save mode is essentially unpredictable, as it depends on the wake-up time. The recommended procedure for reading TCNT2 is thus as follows:
  1. Write any value to either of the registers OCR2 or TCCR2.
  2. Wait for the corresponding Update Busy Flag to be cleared.
  3. Read TCNT2.
- During asynchronous operation, the synchronization of the Interrupt Flags for the asynchronous timer takes three processor cycles plus one timer cycle. The timer is therefore advanced by at least one before the processor can read the timer value causing the setting of the Interrupt Flag. The Output Compare Pin is changed on the timer clock and is not synchronized to the processor clock.

ıter Interrupt Mask TIMSK

Bit	7	6	5	4	3	2	1	0	
	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	–	TOIE0	TIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – OCIE2: Timer/Counter2 Output Compare Match Interrupt Enable**

When the OCIE2 bit is written to one and the I-bit in the Status Register is set (one), the Timer/Counter2 Compare Match interrupt is enabled. The corresponding interrupt is executed if a Compare Match in Timer/Counter2 occurs (i.e., when the OCF2 bit is set in the Timer/Counter Interrupt Flag Register – TIFR).

- **Bit 6 – TOIE2: Timer/Counter2 Overflow Interrupt Enable**

When the TOIE2 bit is written to one and the I-bit in the Status Register is set (one), the Timer/Counter2 Overflow interrupt is enabled. The corresponding interrupt is executed if an overflow in Timer/Counter2 occurs (i.e., when the TOV2 bit is set in the Timer/Counter Interrupt Flag Register – TIFR).

nter Interrupt Flag TIFR

Bit	7	6	5	4	3	2	1	0	
	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	–	TOV0	TIFR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – OCF2: Output Compare Flag 2**

The OCF2 bit is set (one) when a Compare Match occurs between the Timer/Counter2 and the data in OCR2 – Output Compare Register2. OCF2 is cleared by hardware when executing the corresponding interrupt Handling Vector. Alternatively, OCF2 is cleared by writing a logic one to the flag. When the I-bit in SREG, OCIE2 (Timer/Counter2 Compare Match Interrupt Enable), and OCF2 are set (one), the Timer/Counter2 Compare Match Interrupt is executed.

- **Bit 6 – TOV2: Timer/Counter2 Overflow Flag**

The TOV2 bit is set (one) when an overflow occurs in Timer/Counter2. TOV2 is cleared by hardware when executing the corresponding interrupt Handling Vector. Alternatively, TOV2 is cleared by writing a logic one to the flag. When the SREG I-bit, TOIE2 (Timer/Counter2 Overflow Interrupt Enable), and TOV2 are set (one), the Timer/Counter2 Overflow interrupt is executed. In PWM mode, this bit is set when Timer/Counter2 changes counting direction at 0x00.

Digital-to-Analog Conversion

lata is in binary form, the 0's and 1's may be of several forms such TL form where the logic zero may be a value up to 0.8 volts and ay be a voltage from 2 to 5 volts. The data can be converted to clean orm using gates which are designed to be on or off depending on ıe of the incoming signal. Data in clean binary digital form can be ed to an analog form by using a summing amplifier. For example, a 4-bit D/A converter can be made with a four-input summing er. More practical is the R-2R Network DAC.

Weighted Summing Amplifier | R-2R Network Approach

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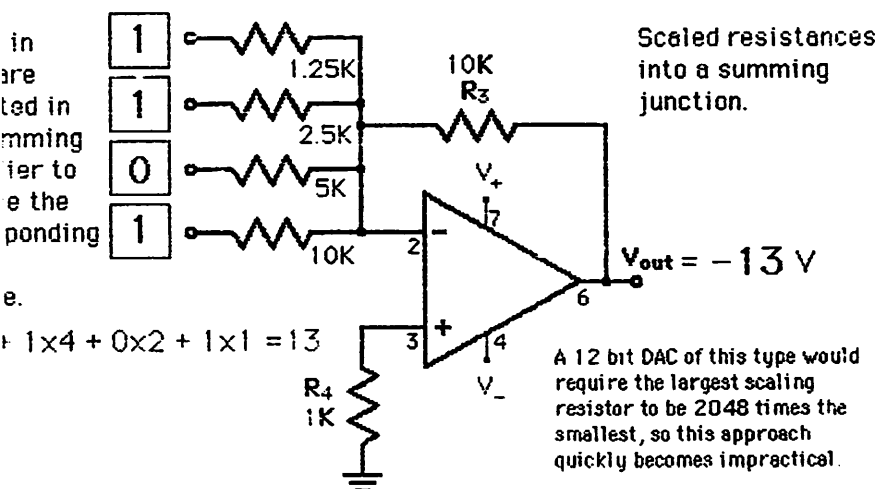
Four-Bit D/A Converter

ıy to achieve D/A conversion is to use a summing amplifier.



proach is not satisfactory for a large number of bits because it s too much precision in the summing resistors. This problem is ne in the R-2R network DAC.

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Reference Horowitz & Hill Digital Systems, Sec 9-16.

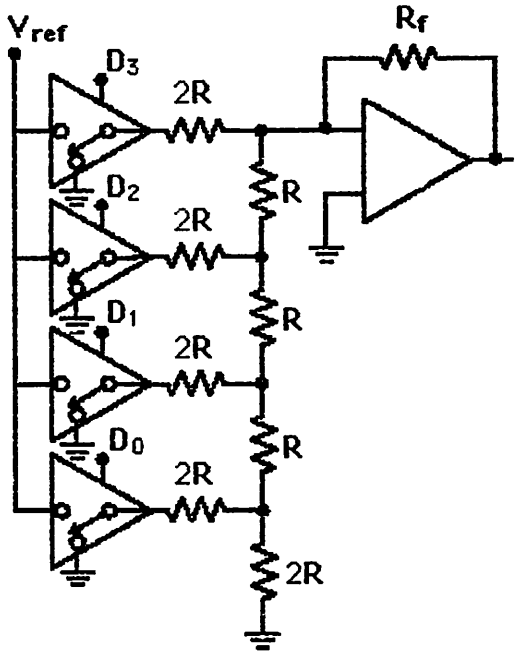
R-2R Ladder DAC

imming amplifier with the R-2R of resistances shown produces tput

$$_t = \frac{R_f}{R} V_{ref}\left[\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2}\right]$$

the D's take the value 0 or 1. The inputs could be TTL voltages close the switches on a logical 1 ave it grounded for a logical 0. s illustrated for 4 bits, but can be led to any number with just the nce values R and 2R.

More Detail



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Reference Horowitz & Hill Sec 9-16. Tocci Digital Systems, Sec 10-3. Simpson Sec 15.2.3.

R-2R Ladder DAC Details

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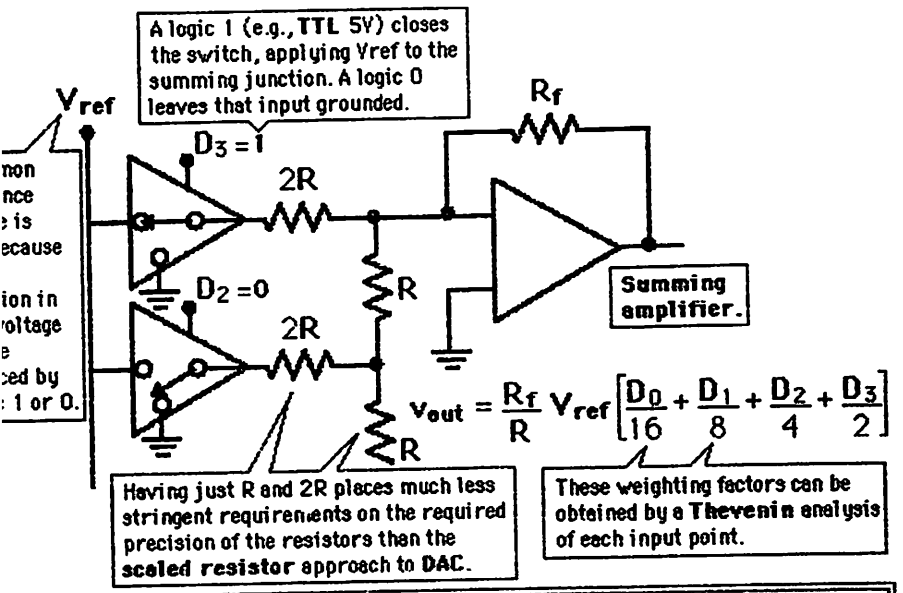

L | Scaled Resistor | Thevenin analysis | Digital-to-Analog Conversion

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Diode varieties

Reference Horowitz & Hill Sec 9-16. Tocci Digital Systems, Sec 10-3. Simpson Sec 15.2.3.

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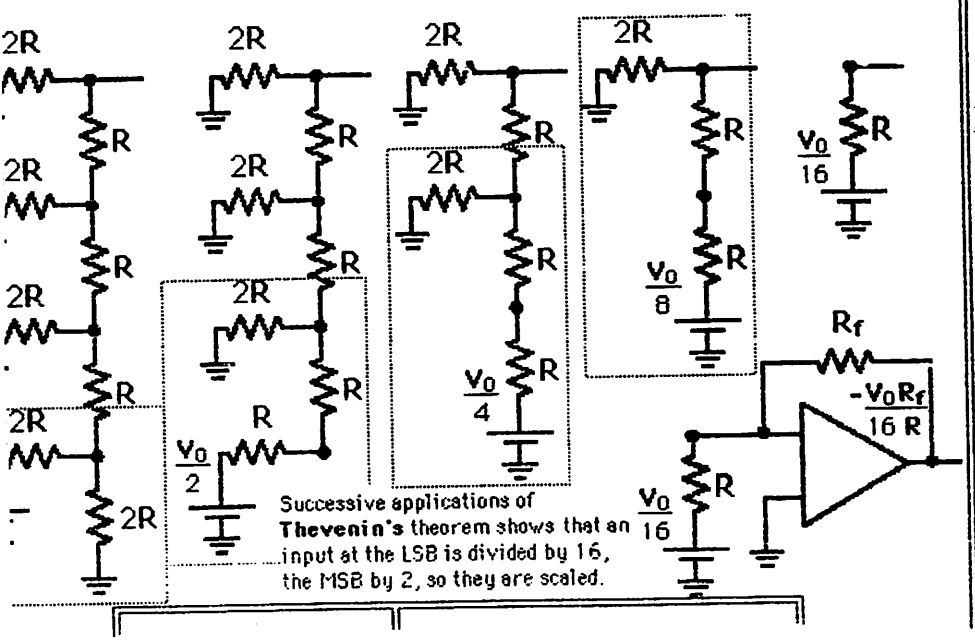
Thevenin Example: R-2R Ladder



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Reference Simpson Sec 15.2.3.

Thevenin's Theorem | Digital-to-Analog Conversion

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R2R DIGITAL TO ANALOG CONVERTER

Deskripsi:

DAC - R - 2R Ladder ini memiliki kelebihan-kelebihan antara lain

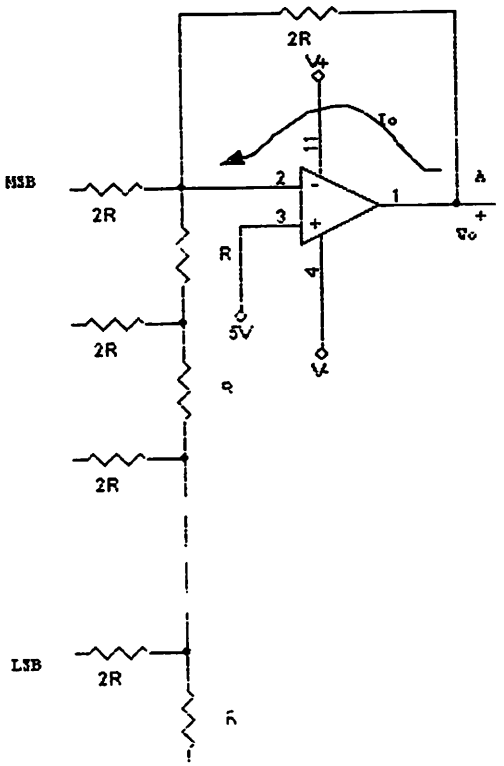
- Tegangan output analog yang dapat diatur antara 5V sampai 34V sesuai yang diinginkan
- Arus output yang lebih besar daripada IC DAC yang lain.

Hal ini disebabkan DAC ini menggunakan OP-AMP. Secara umum rangkaian DAC - R - 2R Ladder ini dapat dibagi menjadi 2 bagian utama, yaitu :

1. Blok R-2R Ladder
2. Blok Penguat Tegangan

Blok R-2R Ladder

Rangkaian R-2R Ladder mengkkonversikan 8 bit data digital dari mikrokontroler menjadi tegangan analog yang bersesuaian

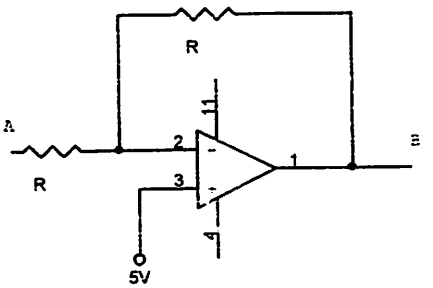


Apabila semua bit data berlogika 1 (FFH) maka tidak ada arus Io yang mengalir sehingga tegangan output (Vo) = 5V

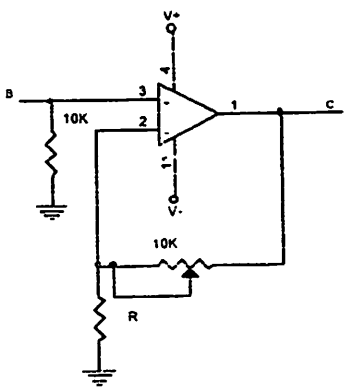
Apabila semua bit data = 0 (0H) maka mengalir arus Io dan tegangan output = 10V

Pada bagian ini ada suatu level DC 5V yang harus dihilangkan agar output DAC berayun antara 0 sampai 5V.

Untuk itu, output DAC ini diinputkan lagi ke sebuah penguat membalik yang mana akan menghasilkan tegangan output DAC 0-5V saja.



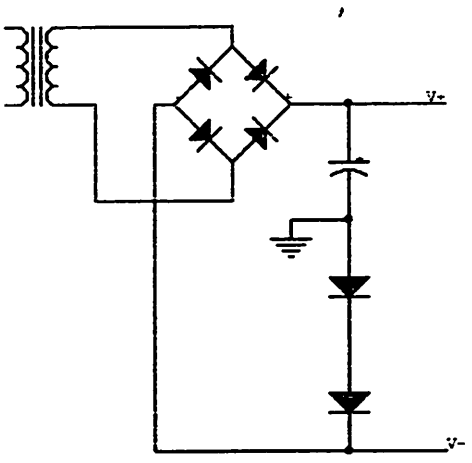
Bagian Penguat Tegangan



Output DAC ini masih dapat dinaikkan ke level yang lebih besar tergantung dari besar tegangan supply yang digunakan. Tegangan output ini maksimal 1,5V dibawah tegangan supply positifnya. Rangkaian dasar penguat tegangan adalah penguat tegangan tidak membalik seperti dalam gambar berikut

$$V_O = V_C = (1+Rf/R)\ V_B$$

Supply DAC



Pada bagian ini, tegangan –V dibutuhkan untuk menghasilkan respon yang lebih linier dari Op Amp yang digunakan.

19-0175; Rev 3; 5/96

MAXIM

±15kV ESD-Protected, +5V RS-232 Transceivers

General Description

The MAX202E–MAX213E, MAX232E/MAX241E line drivers/receivers are designed for RS-232 and V.28 communications in harsh environments. Each transmitter output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. The various combinations of features are outlined in the *Selection Guide*. The drivers and receivers for all ten devices meet all EIA/TIA-232E and CCITT V.28 specifications at data rates up to 120kbps, when loaded in accordance with the EIA/TIA-232E specification.

The MAX211E/MAX213E/MAX241E are available in 28-pin SO packages, as well as a 28-pin SSOP that uses 60% less board space. The MAX202E/MAX232E come in 16-pin narrow SO, wide SO, and DIP packages. The MAX203E comes in a 20-pin DIP/SO package and needs no external charge-pump capacitors. The MAX205E comes in a 24-pin wide DIP package, and also eliminates external charge-pump capacitors. The MAX206E/MAX207E/MAX208E come in 24-pin SO, SSOP, and narrow DIP packages. The MAX232E/MAX241E operate with four 1µF capacitors, while the MAX202E/MAX206E/MAX207E/MAX208E/MAX211E/MAX213E operate with four 0.1µF capacitors, further reducing cost and board space.

Applications

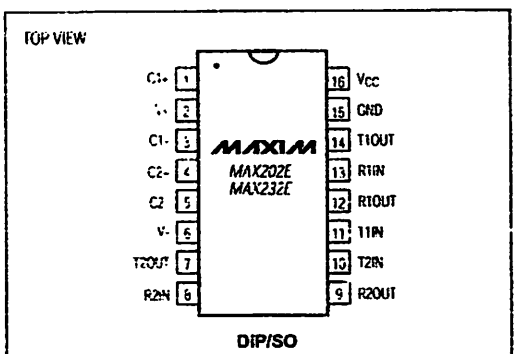
Notebook, Subnotebook, and Palmtop Computers
Battery-Powered Equipment
Hand-Held Equipment

Ordering Information appears at end of data sheet.

Features

- **ESD Protection for RS-232 I/O Pins:**
  ±15kV—Human Body Model
  ±8kV—IEC1000-4-2, Contact Discharge
  ±15kV—IEC1000-4-2, Air-Gap Discharge
- **Latchup Free (unlike bipolar equivalents)**
- **Guaranteed 120kbps Data Rate—LapLink™ Compatible**
- **Guaranteed 3V/µs Min Slew Rate**
- **Operate from a Single +5V Power Supply**

Pin Configurations



DIP/SO

Pin Configurations and Typical Operating Circuits continued at end of data sheet

Selection Guide

PART	No. of RS-232 DRIVERS	No. of RS-232 RECEIVERS	RECEIVERS ACTIVE IN SHUTDOWN	No. of EXTERNAL CAPACITORS	LOW-POWER SHUTDOWN	TTL THREE-STATE
MAX202E	2	2	0	4 (0.1µF)	No	No
MAX203E	2	2	0	None	No	No
MAX205E	5	5	0	None	Yes	Yes
MAX206E	4	3	0	4 (0.1µF)	Yes	Yes
MAX207E	5	3	0	4 (0.1µF)	No	No
MAX208E	4	4	0	4 (0.1µF)	No	No
MAX211E	4	5	0	4 (0.1µF)	Yes	Yes
MAX213E	4	5	2	4 (0.1µF)	Yes	Yes
MAX232E	2	2	0	4 (1µF)	No	No
MAX241E	4	5	0	4 (1µF)	Yes	Yes

LapLink is a registered trademark of Traveling Software, Inc.

±15kV ESD-Protected, +5V RS-232 Transceivers

ABSOLUTE MAXIMUM RATINGS

VCC ..... -0.3V to +6V
V+ ..... (VCC - 0.3V) to +14V
V- ..... -14V to +0.3V
Input Voltages
T_IN ..... -0.3V to (V+ + 0.3V)
R_IN ..... ±30V
Output Voltages
T_OUT ..... (V- - 0.3V) to (V+ + 0.3V)
R_OUT ..... -0.3V to (VCC + 0.3V)
Short-Circuit Duration, T_OUT ..... Continuous
Continuous Power Dissipation (TA = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) ... 842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ... 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin SO (derate 10.00mW/°C above +70°C) ... 800mW
24-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) ... 1.07W
24-Pin Wide Plastic DIP
(derate 14.29mW/°C above +70°C) ... 1.14W
24-Pin SO (derate 11.76mW/°C above +70°C) ... 941mW
24-Pin SSOP (derate 8.00mW/°C above +70°C) ... 640mW
28-Pin SO (derate 12.50mW/°C above +70°C) ... 1W
28-Pin SSOP (derate 9.52mW/°C above +70°C) ... 762mW
Operating Temperature Ranges
MAX2_ _EC_ _ ... 0°C to +70°C
MAX2_ _EE_ _ ... -40°C to +85°C
Storage Temperature Range ... -65°C to +165°C
Lead Temperature (soldering, 10sec) ... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; VCC = +5V ±5% for MAX203E/205E/207E; C1–C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1–C4 = 1µF for MAX232E/241E; TA = TMIN to TMAX; unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
VCC Supply Current	ICC	No load, TA = +25°C	MAX202E/203E		8	15	mA
			MAX205E–208E		11	20	
			MAX211E/213E		14	20	
			MAX232E		5	10	
			MAX241E		7	15	
Shutdown Supply Current		TA = +25°C, Figure 1	MAX205E/206E		1	10	µA
			MAX211E/241E		1	10	
			MAX213E		15	50	
LOGIC							
Input Pull-Up Current		T_IN = 0V (MAX205E–208E/211E/213E/241E)			15	200	µA
Input Leakage Current		T_IN = 0V to VCC (MAX202E/203E/232E)				±10	µA
Input Threshold Low	VIL	T_IN; EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX205E–208E/211E/241E)				0.8	V
Input Threshold High	VIH	T_IN		2.0			V
		EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX205E–208E/211E/241E)		2.4			
Output Voltage Low	VOL	R_OUT; IOUT = 3.2mA (MAX202E/203E/232E) or IOUT = 1.6mA (MAX205E/208E/211E/213E/241E)				0.4	V
Output Voltage High	VOH	R_OUT; IOUT = -1.0mA		3.5	VCC - 0.4		V
Output Leakage Current		$\overline{EN}$ = VCC, EN = 0V, 0V ≤ ROUT ≤ VCC, MAX205E–208E/211E/213E/241E outputs disabled			±0.05	±10	µA

ELECTRICAL CHARACTERISTICS (continued)

(VCC = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; VCC = +5V ±5% for MAX203E/205E/207E, C1–C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1–C4 = 1µF for MAX232E/241E; TA = TMIN to TMAX unless otherwise noted. Typical values are at TA = +25°C.)

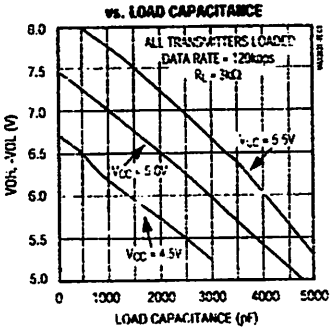
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EIA/TIA-232E RECEIVER INPUTS							
Input Voltage Range				-30		30	V
Input Threshold Low		TA = +25°C, VCC = 5V	All parts, normal operation	0.8	1.2		V
			MAX213E, $\overline{SHDN}$ = 0V, EN = VCC	0.6	1.5		
Input Threshold High		TA = +25°C, VCC = 5V	All parts, normal operation		1.7	2.4	V
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = VCC		1.5	2.4	
Input Hysteresis		VCC = 5V, no hysteresis in shutdown		0.2	0.5	1.0	V
Input Resistance		TA = +25°C, VCC = 5V		3	5	7	kΩ
EIA/TIA-232E TRANSMITTER OUTPUTS							
Output Voltage Swing		All drivers loaded with 3kΩ to ground (Note 1)		±5	±9		V
Output Resistance		VCC = V+ = V- = 0V, VOUT = ±2V		300			Ω
Output Short-Circuit Current					±10	±60	mA
TIMING CHARACTERISTICS							
Maximum Data Rate		RL = 3kΩ to 7kΩ, CL = 50pF to 1000pF, one transmitter switching		120			kbps
Receiver Propagation Delay	tPLHR, tPHLR	CL = 150pF	All parts, normal operation		0.5	10	µs
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = VCC		4	40	
Receiver Output Enable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2			600		ns
Receiver Output Disable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2			200		ns
Transmitter Propagation Delay	tPLHT, tPHLT	RL = 3kΩ, CL = 2500pF, all transmitters loaded			2		µs
Transition-Region Slew Rate		TA = +25°C, VCC = 5V, RL = 3kΩ to 7kΩ, CL = 50pF to 1000pF, measured from -3V to +3V or +3V to -3V, Figure 3		3	6	30	V/µs
ESD PERFORMANCE: TRANSMITTER OUTPUTS, RECEIVER INPUTS							
ESD-Protection Voltage		Human Body Model			±15		kV
		IEC1000-4-2, Contact Discharge			±8		
		IEC1000-4-2, Air-Gap Discharge			±15		

Note 1: MAX211EE_ _ tested with VCC = +5V ±5%.

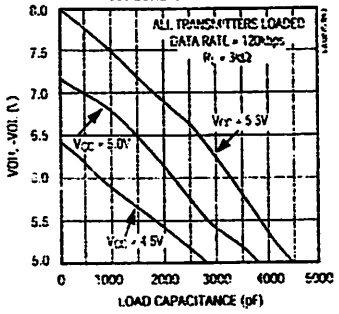
Typical Operating Characteristics

(Typical Operating Circuits. V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

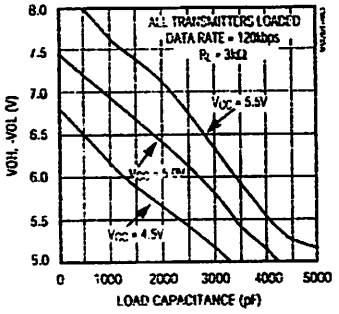
MAX232E
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



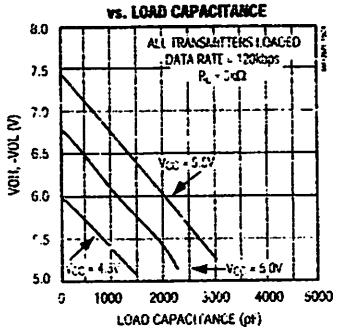
MAX202E/MAX203E
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



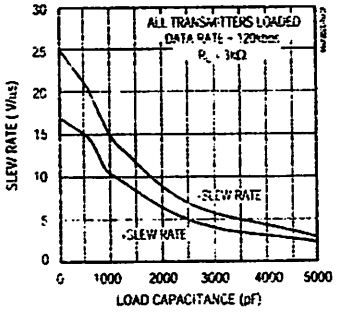
MAX241E
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



MAX211E/MAX213E
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



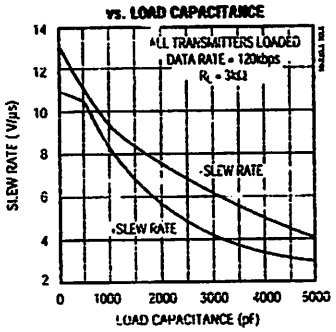
MAX211E/MAX213E/MAX241E
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



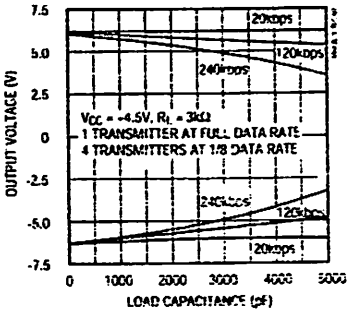
Typical Operating Characteristics (continued)

(Typical Operating Circuits, V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

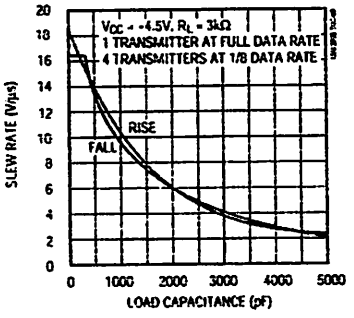
MAX202E/MAX203E/MAX232E
TRANSMITTER SLEW RATE
vs. LOAD CAPACITANCE



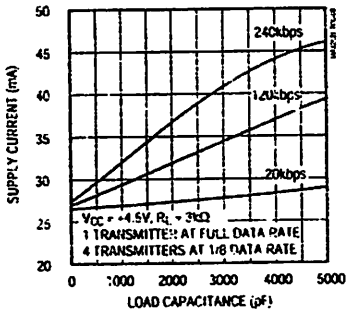
MAX205E–MAX208E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



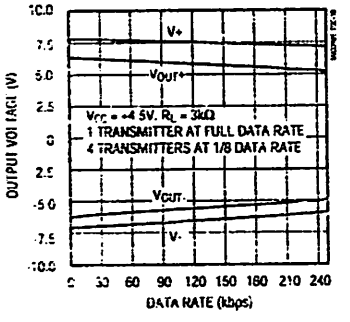
MAX205E–MAX208E
TRANSMITTER SLEW RATE
vs. LOAD CAPACITANCE



MAX205E–MAX208E
SUPPLY CURRENT
vs. LOAD CAPACITANCE



MAX205E–MAX208E
OUTPUT VOLTAGE vs. DATA RATE



Pin Descriptions

MAX202E/MAX232E

PIN		NAME	FUNCTION
DIP/SO	LCC		
1, 3	2, 4	C1+, C1-	Terminals for positive charge-pump capacitor
2	3	V+	+2VCC voltage generated by the charge pump
4, 5	5, 7	C2+, C2-	Terminals for negative charge-pump capacitor
6	8	V-	-2VCC voltage generated by the charge pump
7, 14	9, 18	T_OUT	RS-232 Driver Outputs
8, 13	10, 17	R_IN	RS-232 Receiver Outputs
9, 12	12, 15	R_OUT	RS-232 Receiver Outputs
10, 11	13, 14	T_IN	RS-232 Driver Inputs
15	19	GND	Ground
16	20	VCC	+4.5V to +5.5V Supply-Voltage Input
—	1, 6, 11, 16	N.C.	No Connect—not internally connected.

MAX203E

PIN		NAME	FUNCTION
DIP	SO		
1, 2	1, 2	T_IN	RS-232 Driver Inputs
3, 20	3, 20	R_OUT	RS-232 Receiver Outputs
4,19	4, 19	R_IN	RS-232 Receiver Inputs
5,18	5, 18	T_OUT	RS-232 Transmitter Outputs
6, 9	6, 9	GND	Ground
7	7	VCC	+4.5V to +5.5V Supply-Voltage Input
8	13	C1+	Make no connection to this pin.
10, 16	11, 16	C2-	Connect pins together.
12, 17	10, 17	V-	-2VCC voltage generated by the charge pump. Connect pins together.
13	14	C1-	Make no connection to this pin.
14	8	V+	+2VCC voltage generated by the charge pump
11, 15	12, 15	C2+	Connect pins together.

MAX205E

PIN	NAME	FUNCTION
1–4, 1[illegible]	T_OUT	RS-232 Driver Outputs
5, 10, 1[illegible]4	R_IN	RS-232 Receiver Inputs
6, 9, 14, 1[illegible]3	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
7, 8, 15, 1[illegible]2	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to VCC.
11	GND	Ground
12	VCC	+4.75V to +5.25V Supply Voltage
20	$\overline{EN}$	Receiver Enable—active low
21	SHDN	Shutdown Control—active high

Pin Descriptions (continued)

MAX206E

PIN	NAME	FUNCTION
1, 2, 3, 24	T_OUT	RS-232 Driver Outputs
4, 16, 23	R_IN	RS-232 Receiver Inputs
5, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
6, 7, 18, 19	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.5V to +5.5V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	$-2V_{CC}$ generated by the charge pump
13, 14	C2-, C2-	Terminals for negative charge-pump capacitor
15	V-	$-2V_{CC}$ generated by the charge pump
20	$\overline{EN}$	Receiver Enable—active low
21	SHDN	Shutdown Control—active high

MAX207E

PIN	NAME	FUNCTION
1, 2, 3, 20, 24	T_OUT	RS-232 Driver Outputs
4, 16, 23	R_IN	RS-232 Receiver Inputs
5, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
6, 7, 18, 19, 21	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.75V to +5.25V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	$-2V_{CC}$ generated by the charge pump
13, 14	C2-, C2-	Terminals for negative charge-pump capacitor
15	V-	$-2V_{CC}$ generated by the charge pump

MAX208E

PIN	NAME	FUNCTION
1, 2, 20, 24	T_OUT	RS-232 Driver Outputs
3, 7, 16, 23	R_IN	RS-232 Receiver Inputs
4, 6, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
5, 18, 19, 21	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V_{CC}.
8	GND	Ground
9	V_{CC}	+4.5V to +5.5V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	$-2V_{CC}$ generated by the charge pump
13, 14	C2-, C2-	Terminals for negative charge-pump capacitor
15	V-	$-2V_{CC}$ generated by the charge pump

±15kV ESD-Protected, +5V RS-232 Transceivers

Pin Descriptions (continued)

MAX211E/MAX213E/MAX241E

PIN	NAME	FUNCTION
1, 2, 3, 26	T_OUT	RS-232 Driver Outputs
4, 9, 18, 23, 27	R_IN	RS-232 Receiver Inputs
5, 8, 19, 22, 26	R_OUT	TTL/CMOS Receiver Outputs. For the MAX213E, receivers R4 and R5 are active in shutdown mode when EN = 1. For the MAX211E and MAX241E, all receivers are inactive in shutdown.
6, 7, 20, 21	T_IN	TTL/CMOS Driver Inputs. Only the MAX211E, MAX213E, and MAX241E have internal pull-ups to Vcc
10	GND	Ground
11	Vcc	+4.5V to +5.5V Supply Voltage
12, 14	C1+, C1-	Terminals for positive charge-pump capacitor
13	V-	-2Vcc voltage generated by the charge pump
15, 16	C2+, C2-	Terminals for negative charge-pump capacitor
17	V-	-2Vcc voltage generated by the charge pump
24	$\overline{EN}$	Receiver Enable—active low (MAX211E, MAX241E)
	EN	Receiver Enable—active high (MAX213E)
25	SHDN	Shutdown Control—active high (MAX211E, MAX241E)
	$\overline{SHDN}$	Shutdown Control—active low (MAX213E)

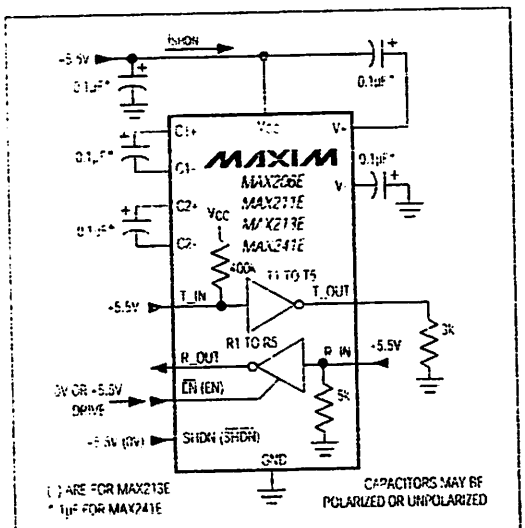


Figure 1. Shutdown-Current Test Circuit (MAX206E, MAX211E/MAX213E/MAX241E)

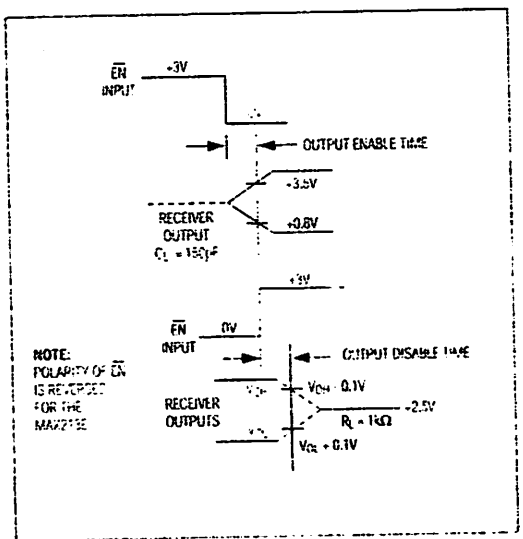


Figure 2. Receiver Output Enable and Disable Timing (MAX205E, MAX206E/MAX211E/MAX213E/MAX241E)

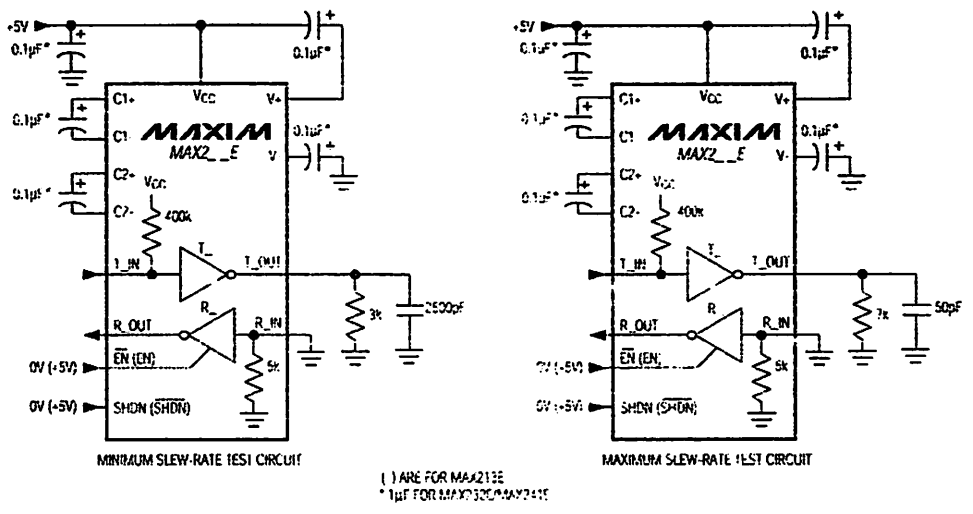


Figure 3. Transition Slew-Rate Circuit

Detailed Description

The MAX202E–MAX213E, MAX232E/MAX241E consist of three sections: charge-pump voltage converters, drivers (transmitters), and receivers. These E versions provide extra protection against ESD. They survive ±15kV discharges to the RS-232 inputs and outputs, tested using the Human Body Model. When tested according to IEC1000-4-2, they survive ±8kV contact-discharges and ±15kV air-gap discharges. The rugged E versions are intended for use in harsh environments or applications where the RS-232 connection is frequently changed (such as notebook computers). The standard (non-"E") MAX202, MAX203, MAX205–MAX208, MAX211, MAX213, MAX232, and MAX241 are recommended for applications where cost is critical.

+5V to ±10V Dual Charge-Pump Voltage Converter

The +5V to ±10V conversion is performed by dual charge-pump voltage converters (Figure 4). The first charge-pump converter uses capacitor C1 to double the +5V into +10V, storing the +10V on the output filter capacitor, C3. The second uses C2 to invert the +10V into -10V, storing the -10V on the V- output filter capacitor C4.

In shutdown mode, V- is internally connected to VCC by a 1kΩ pull-down resistor, and V- is internally connected to ground by a 1kΩ pull-up resistor.

RS-232 Drivers

With VCC = 5V, the typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver. The output swing is guaranteed to meet EIA/TIA-232E and V.28 specifications that call for ±5V minimum output levels under worst-case conditions. These include a 3kΩ load, minimum VCC, and maximum operating temperature. The open-circuit output voltage swings from (V+ - 0.6V) to V-.

Input thresholds are CMOS/TTL compatible. The unused drivers' inputs on the MAX205E–MAX208E, MAX211E, MAX213E, and MAX241E can be left unconnected because 400kΩ pull-up resistors to VCC are included on-chip. Since all drivers invert, the pull-up resistors force the unused drivers' outputs low. The MAX202E, MAX203E, and MAX232E do not have pull-up resistors on the transmitter inputs.

When in low-power shutdown mode, the MAX205E/MAX206E/MAX211E/MAX213E/MAX241E driver outputs are turned off and draw only leakage currents—even if they are back-driven with voltages between 0V and 12V. Below -0.5V in shutdown, the transmitter output is diode-clamped to ground with a 1kΩ series impedance.

RS-232 Receivers

The receivers convert the RS-232 signals to CMOS-logic output levels. The guaranteed 0.8V and 2.4V receiver input thresholds are significantly tighter than the ±3V thresholds required by the EIA/TIA-232E specification. This allows the receiver inputs to respond to TTL/CMOS-logic levels, as well as RS-232 levels.

The guaranteed 0.8V input low threshold ensures that receivers shorted to ground have a logic 1 output. The 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

Receiver inputs have approximately 0.5V hysteresis. This provides clean output transitions, even with slow rise/fall-time signals with moderate amounts of noise and ringing.

In shutdown, the MAX213E's R4 and R5 receivers have no hysteresis.

Shutdown and Enable Control (MAX205E/MAX206E/MAX211E/MAX213E/MAX241E)

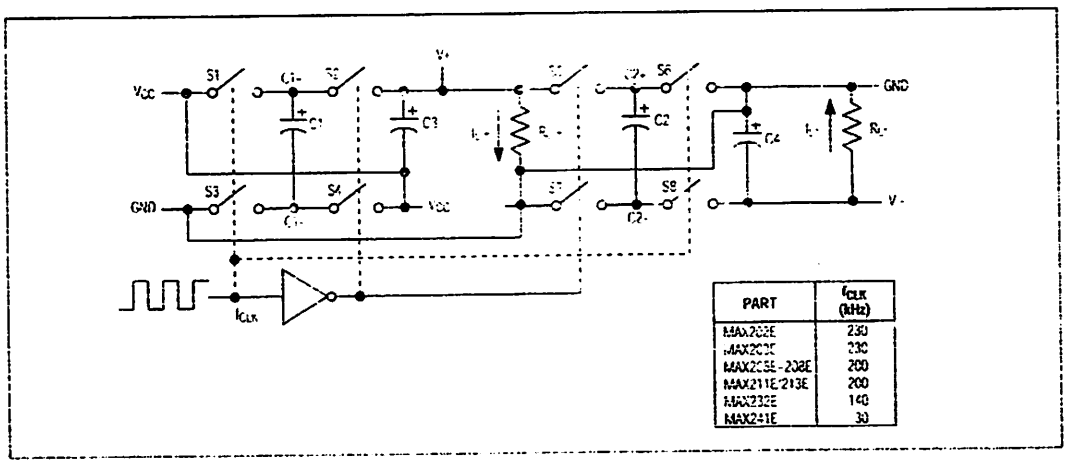
In shutdown mode, the charge pumps are turned off, V+ is pulled down to VCC, V- is pulled to ground, and the transmitter outputs are disabled. This reduces supply current typically to 1µA (15µA for the MAX213E). The time required to exit shutdown is under 1ms, as shown in Figure 5.

Receivers

All MAX213E receivers, except R4 and R5, are put into a high-impedance state in shutdown mode (see Tables 1a and 1b). The MAX213E's R4 and R5 receivers still function in shutdown mode. These two awake-in-shutdown receivers can monitor external activity while maintaining minimal power consumption.

The enable control is used to put the receiver outputs into a high-impedance state, to allow wire-OR connection of two EIA/TIA-232E ports (or ports of different types) at the UART. It has no effect on the RS-232 drivers or the charge pumps.

Note: The enable control pin is active low for the MAX211E/MAX241E (EN), but is active high for the MAX213E (EN). The shutdown control pin is active high for the MAX205E/MAX206E/MAX211E/MAX241E (SHDN), but is active low for the MAX213E (SHDN).



PART	f_{CLK} (kHz)
MAX202E	250
MAX203E	230
MAX205E-208E	200
MAX211E-213E	200
MAX232E	140
MAX241E	30

Figure 4. Charge-Pump Diagram

The MAX213E's receiver propagation delay is typically 0.5µs in normal operation. In shutdown mode, propagation delay increases to 4µs for both rising and falling transitions. The MAX213E's receiver inputs have approximately 0.5V hysteresis, except in shutdown, when receivers R4 and R5 have no hysteresis.

When entering shutdown with receivers active, R4 and R5 are not valid until 80µs after $\overline{SHDN}$ is driven low. When coming out of shutdown, all receiver outputs are invalid until the charge pumps reach nominal voltage levels (less than 2ms when using 0.1µF capacitors).

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's E versions keep working without latchup, whereas competing RS-232 products can latch and must be powered down to remove latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ±8kV using the contact-discharge method specified in IEC1000-4-2
3) ±15kV using IEC1000-4-2's air-gap method.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 6a shows the Human Body Model, and Figure 6b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

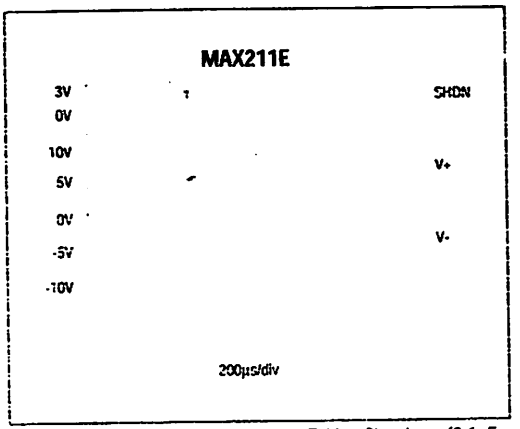


Figure 5. MAX211E V+ and V- when Exiting Shutdown (0.1µF capacitors)

Table 1a. MAX205E/MAX206E/MAX211E/ MAX241E Control Pin Configurations

SHDN	EN	OPERATION STATUS	Tx	Rx
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All High-Z
1	X	Shutdown	All High-Z	All High-Z

X = Don't Care

Table 1b. MAX213E Control Pin Configurations

SHDN	EN	OPERATION STATUS	Tx 1–4	Rx	
				1–3	4, 5
0	0	Shutdown	All High-Z	High-Z	High-Z
0	1	Shutdown	All High-Z	High-Z	Active*
1	0	Normal Operation	All Active	High-Z	High-Z
1	1	Normal Operation	All Active	Active	Active

*Active = active with reduced performance

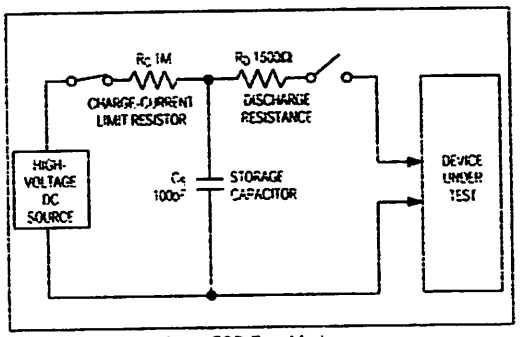


Figure 6a. Human Body ESD Test Model

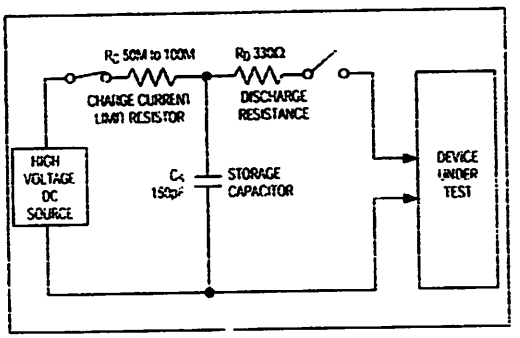


Figure 7a. IEC1000 4-2 ESD Test Model

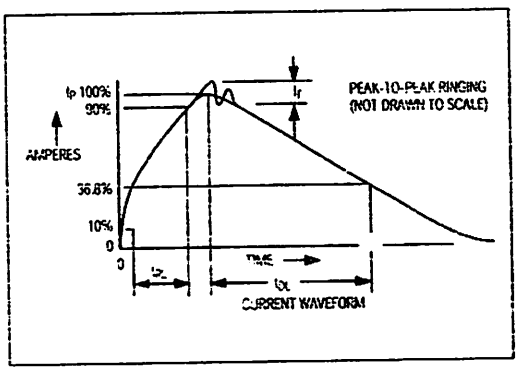


Figure 6b. Human Body Model Current Waveform

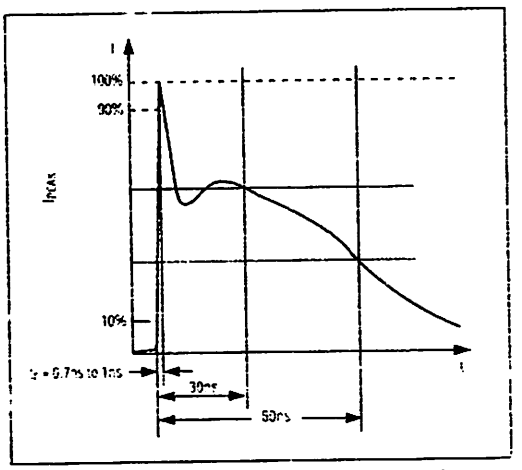


Figure 7b. IEC1000-4-2 ESD Generator Current Waveform

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX202E/MAX203E–MAX213E, MAX232E/MAX241E help you design equipment that meets level 4 (the highest level) of IEC1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2 because series resistance is lower in the IEC1000-4-2 model. Hence, the ESD withstand voltage measured to IEC1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7b shows the current waveform for the 8kV IEC1000-4-2 level-four ESD contact-discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just RS-232 inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The MAX202E, MAX206–MAX208E, MAX211E, and MAX213E require 0.1µF capacitors, and the MAX232E and MAX241E require 1µF capacitors, although in all cases capacitors up to 10µF can be used without harm. Ceramic, aluminum-electrolytic, or tantalum capacitors are suggested for the 1µF capacitors, and ceramic dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2x) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Use larger capacitors (up to 10µF) to reduce the output impedance at V+ and V-. This can be useful when "stealing" power from V+ or from V-. The MAX203E and MAX205E have internal charge-pump capacitors.

Bypass V_{CC} to ground with at least 0.1µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce both driver output swing and noise margins. Increasing the value of the charge-pump capacitors (up to 10µF) helps maintain performance when power is drawn from V+ or V-.

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple receivers.

Driver Outputs when Exiting Shutdown

The driver outputs display no ringing or undesirable transients as they come out of shutdown.

High Data Rates

These transceivers maintain the RS-232 ±5.0V minimum driver output voltages at data rates of over 120kbps. For data rates above 120kbps, refer to the Transmitter Output Voltage vs. Load Capacitance graphs in the *Typical Operating Characteristics*. Communication at these high rates is easier if the capacitive loads on the transmitters are small; i.e., short cables are best.

Table 2. Summary of EIA/TIA-232E, V.28 Specifications

PARAMETER		CONDITIONS	EIA/TIA-232E, V.28 SPECIFICATIONS
Driver Output Voltage	0 Level	3kΩ to 7kΩ load	+5V to +15V
	1 Level	3kΩ to 7kΩ load	-5V to -15V
Driver Output Level, Max		No load	±25V
Data Rate		$3k\Omega \le R_L \le 7k\Omega$, $C_L \le 2500pF$	Up to 20kbps
Receiver Input Voltage	0 Level		+3V to +15V
	1 Level		-3V to -15V
Receiver Input Level			±25V
Instantaneous Slew Rate, Max		$3k\Omega \le R_L \le 7k\Omega$, $C_L \le 2500pF$	30V/µs
Driver Output Short-Circuit Current, Max			100mA
Transition Rate on Driver Output		V.28	1ms or 3% of the period
		EIA/TIA-232E	4% of the period
Driver Output Resistance		$-2V < V_{OUT} < +2V$	300Ω

National Semiconductor

August 2000

M741
perational Amplifier

neral Description

LM741 series are general purpose operational amplifi- vhich feature improved performance over industry stan- s like the LM709. They are direct, plug-in replacements ie 709C, LM201, MC1439 and 748 in most applications.

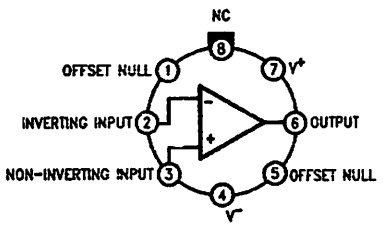
amplifiers offer many features which make their appli- n nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Features

nnection Diagrams

Metal Can Package

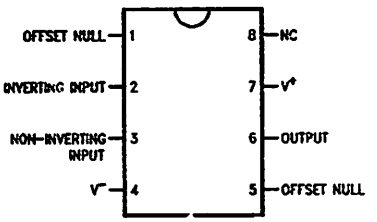


00934102

1: LM741H is available per JM38510/10101

Order Number LM741H, LM741H/883 (Note 1), LM741AH/883 or LM741CH
See NS Package Number H08C

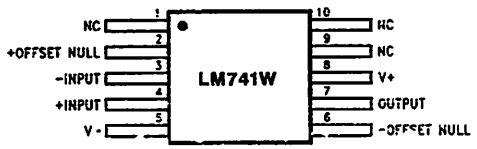
Dual-In-Line or S.O. Package



00934103

Order Number LM741J, LM741J/883, LM741CN
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak

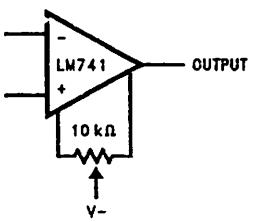


00934106

Order Number LM741W/883
See NS Package Number W10A

pical Application

Offset Nulling Circuit



00934107

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 7)

	LM741A	LM741	LM741C
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V
Input Voltage (Note 4)	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	150°C	100°C
Soldering Information			
N-Package (10 seconds)	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C
M-Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.			
ESD Tolerance (Note 8)	400V	400V	400V

Electrical Characteristics (Note 5)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$										
	$R_S \le 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \le 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 50\Omega$			4.0							mV
	$R_S \le 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							µV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	$T_A = 25°C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V

ical Characteristics (Note 5) (Continued)

arameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
al Voltage Gain	T_A = 25°C, $R_L \geq 2$ kΩ										
	V_S = ±20V, V_O = ±15V	50									V/mV
	V_S = ±15V, V_O = ±10V				50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $R_L \geq 2$ kΩ,										
	V_S = ±20V, V_O = ±15V	32									V/mV
	V_S = ±15V, V_O = ±10V				25			15			V/mV
	V_S = ±5V, V_O = ±2V	10									V/mV
tage Swing	V_S = ±20V										
	$R_L \geq 10$ kΩ	±16									V
	$R_L \geq 2$ kΩ	±15									V
	V_S = ±15V										
	$R_L \geq 10$ kΩ				±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ				±10	±13		±10	±13		V
ort Circuit	T_A = 25°C	10	25	35		25			25		mA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Mode	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
Ratio	$R_S \leq 10$ kΩ, V_{CM} = ±12V				70	90		70	90		dB
	$R_S \leq 50$Ω, V_{CM} = ±12V	80	95								dB
ltage Rejection	$T_{AMIN} \leq T_A \leq T_{AMAX}$, V_S = ±20V to V_S = ±5V										
	$R_S \leq 50$Ω	86	96								dB
	$R_S \leq 10$ kΩ				77	96		77	96		dB
Response	T_A = 25°C, Unity Gain										
ne			0.25	0.8		0.3			0.3		µs
ot			6.0	20		5			5		%
(Note 6)	T_A = 25°C	0.437	1.5								MHz
	T_A = 25°C, Unity Gain	0.3	0.7			0.5			0.5		V/µs
rrent	T_A = 25°C					1.7	2.8		1.7	2.8	mA
nsumption	T_A = 25°C										
	V_S = ±20V		80	150							mW
	V_S = ±15V					50	85		50	85	mW
	V_S = ±20V										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
	V_S = ±15V										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is , but do not guarantee specific performance limits.

Electrical Characteristics (Note 5) (Continued)

Note 3: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	25°C/W	N/A

Note 4: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

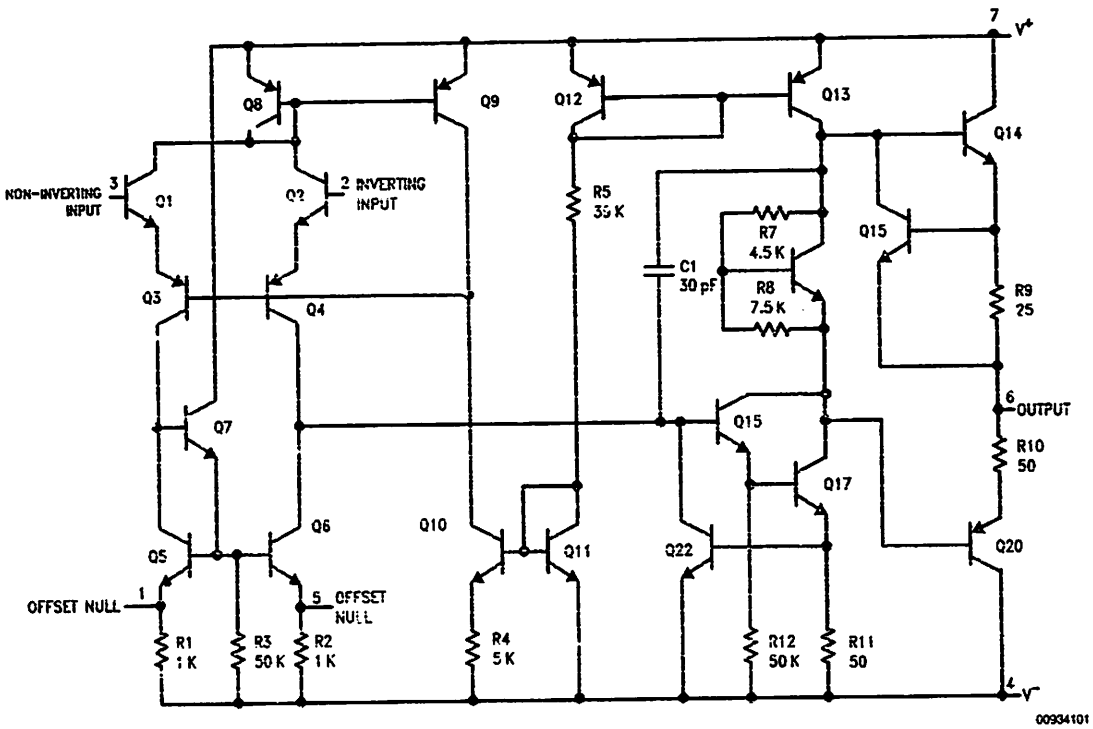
Note 5: Unless otherwise specified, these specifications apply for V_S = ±15V, $-55°C \leq T_A \leq +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \leq T_A \leq +70°C$.

Note 6: Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

Note 7: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Schematic Diagram



CMOS MT8841
Calling Number Identification Circuit

ISSUE 4 May 1995

Ordering Information

MT8841AE	16 Pin Plastic DIP
MT8841AS	16 Pin SOIC
MT8841AN	20 Pin SSOP

-40 °C to +85 °C

eatures

- 1200 baud BELL 202 and CCITT V.23 Frequency Shift Keying (FSK) demodulation
- Compatible with Bellcore TR-NWT-000030 and SR-TSV-002476
- High input sensitivity: -36dBm
- Simple serial 3-wire data interface eliminating the need for a UART
- Power down mode
- Internal gain adjustable amplifier
- Carrier detect status output
- Uses 3.579545 MHz crystal or ceramic resonator
- Single 5V power supply
- Low power CMOS technology

pplications

- Calling Number Delivery (CND), Calling Name Delivery (CNAM) and Calling Identity on Call Waiting (CIDCW) features of Bellcore CLASS℠ service
- Feature phones
- Phone set adjunct boxes
- FAX machines
- Telephone Answering machines
- Database query systems

Description

The MT8841 Calling Number Identification Circuit (CNIC) is a CMOS integrated circuit providing an interface to various calling line information delivery services that utilize 1200 baud BELL 202 or CCITT V.23 FSK voiceband data transmission schemes. The CNIC receives and demodulates the signal and outputs data into a simple 3-wire serial interface.

Typically, the FSK modulated data containing information on the calling line is sent before alerting the called party or during the silent interval between the first and second ring using either CCITT V.23 recommendations or Bell 202 specifications.

The CNIC accepts and demodulates both CCITT V.23 and BELL 202 signals. Along with serial data and clock, the CNIC provides a data ready signal to indicate the reception of every 8-bit character sent from the Central Office. The received data can be processed externally by a microcontroller, stored in memory, or displayed as is, depending on the application.

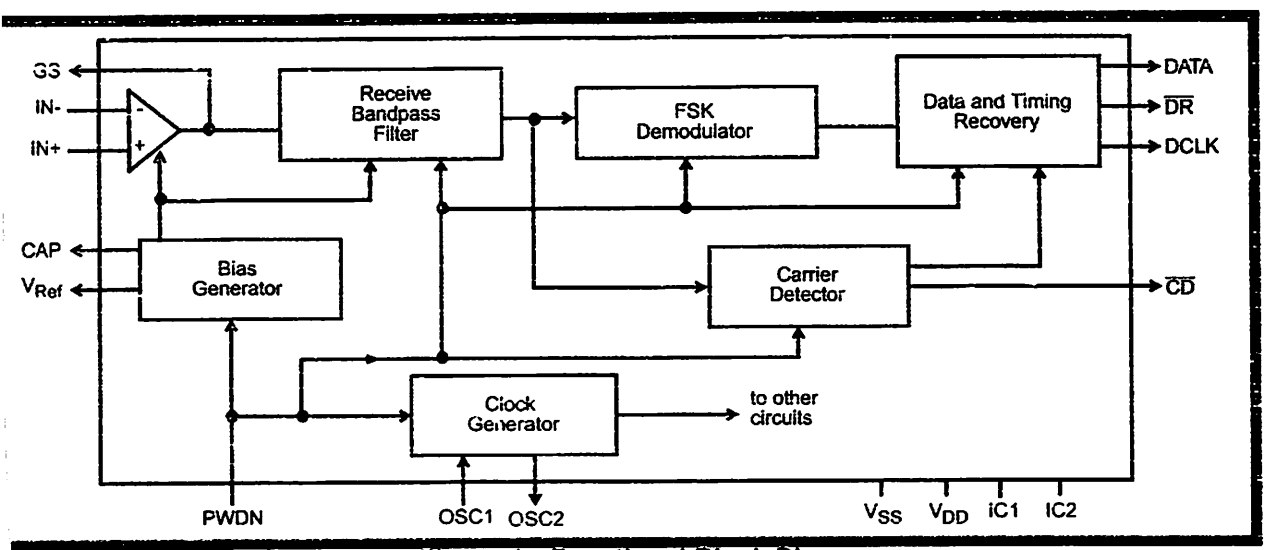


Figure 1 - Functional Block Diagram

.ASS℠ is a service mark of Bellcore

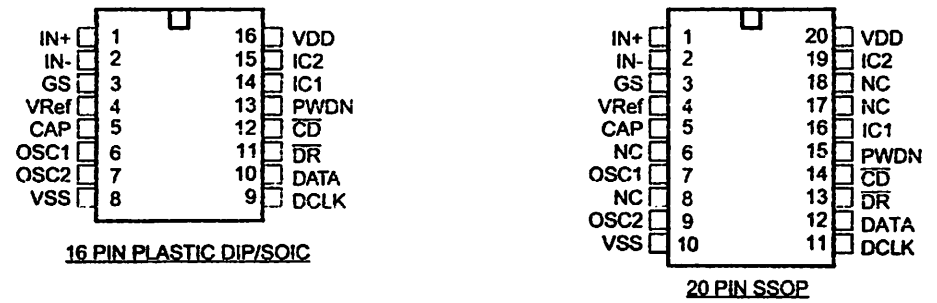


Figure 2 - Pin Connections

scription

Name	Description
IN+	**Non-inverting Op-Amp (Input).**
IN-	**Inverting Op-Amp (Input).**
GS	**Gain Select (Output).** Gives access to op-amp output for connection of feedback resistor.
V_{Ref}	**Voltage Reference (Output).** Nominally $V_{DD/2}$. This is used to bias the op-amp inputs.
CAP	**Capacitor.** Connect a 0.1µF capacitor to V_{SS}.
OSC1	**Oscillator (Input).** Crystal or ceramic resonator connection. This pin can be driven directly from an external clocking source.
OSC2	**Oscillator (Output).** Crystal or ceramic resonator connection. When OSC1 is driven by an external clock, this pin should be left open.
V_{SS}	Power supply ground.
DCLK	**Data Clock (Output).** Outputs a clock burst of 8 low going pulses at 1202.8Hz (3.5795MHz divided by 2976). Every clock burst is initiated by the DATA stop bit start bit sequence. When the input DATA is 1202.8 baud, the positive edge of each DCLK pulse coincides with the middle of the data bits output at the DATA pin. No DCLK pulses are generated during the start or stop bits. Typically, DCLK is used to clock the eight data bits from the 10 bit data word into a serial-to-parallel converter.
DATA	**Data (Output).** Serial data output corresponding to the FSK input and switching at the input baud rate. Mark frequency at the input corresponds to a logic high, while space frequency corresponds to a logic low at the DATA output. With no FSK input, DATA is at logic high. This output stays high until $\overline{CD}$ has become active.
$\overline{DR}$	**Data Ready (Open Drain Output).** This output goes low after the last DCLK pulse of each word. This can be used to identify the data (8-bit word) boundary on the serial output stream. Typically, $\overline{DR}$ is used to latch the eight data bits from the serial-to-parallel converter into a microcontroller.
$\overline{CD}$	**Carrier Detect (Open Drain Output).** A logic low indicates that a carrier has been present for a specified time on the line. A time hysteresis is provided to allow for momentary discontinuity of carrier.
PWDN	**Power Down (Input).** Active high, Schmitt Trigger input. Powers down the device including the input op-amp and the oscillator.
IC1	**Internal Connection 1.** Connect to V_{SS}.
IC2	**Internal Connection 2.** Internally connected, leave open circuit.
V_{DD}	Positive power supply voltage.
NC	No Connection.

inctional Description

e MT8841 Calling Number Identification Circuit NIC) is a device compatible with the Bellcore)posal (TR-NWT-000030) on generic requirements transmitting asynchronous voiceband data to stomer Premises Equipment (CPE) from a serving)red Program Controlled Switching System PCS) or a Central Office (CO). This data nsmission technique is applicable in a variety of rvices like Calling Number Delivery (CND), Calling me Delivery (CNAM) or Calling Identity Delivery Call Waiting (CIDCW) as specified in Custom cal Area Signalling Service (CLASS℠) calling ormation delivery features by Bellcore.

th CND, CNAM and CIDCW service, the called bscriber has the capability to display or to store information on the calling party which is sent by CO and received by the CNIC.

the CND service, information about a calling party embedded in the silent interval between the first d second ring. During this period, the CNIC ceives and demodulates the 1200 baud FSK signal)mpatible with Bell-202 specification) and outputs ta into a 3-wire serial interface.

the CIDCW service, information about a second lling party is sent to the subscriber, while they are gaged in another call. During this period, the CNIC ceives and demodulates the FSK signal as in the ND case.

ie CNIC is designed to provide the data nsmission interface required for the above service

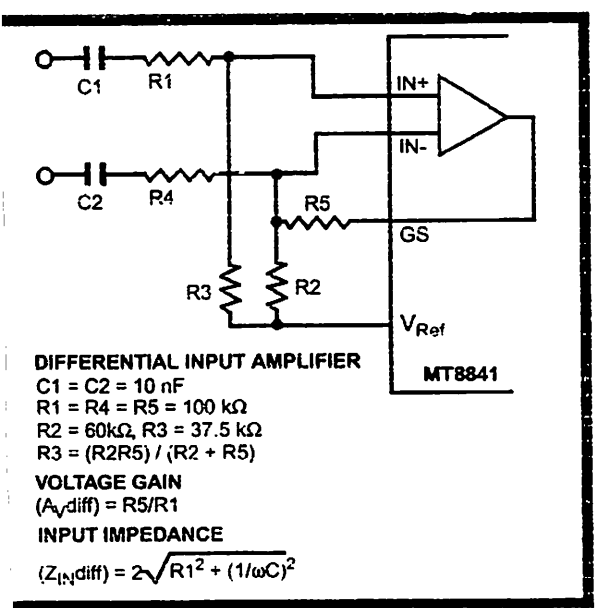


Figure 3 - Differential Input Configuration

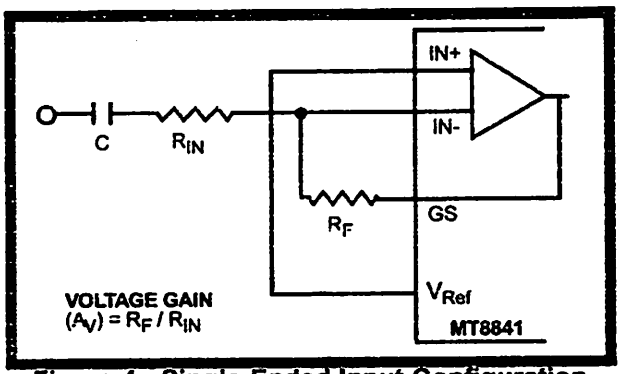


Figure 4 - Single-Ended Input Configuration

at the called subscriber location either in the on-hook case as in CND, or the off-hook case, as in CIDCW. The functional block diagram of the CNIC is shown in Figure 1. Note however, for CIDCW applications, a separate CAS (CPE Alerting Signal) detector is required.

In Europe, Caller ID and CIDCW services are being proposed. These schemes may be different from their North American counterparts. In most cases. 1200 baud CCITT V.23 FSK is used instead of Bell 202. Because the CNIC can also demodulate 1200 baud CCITT V.23 with the same performance, it is suitable for these applications.

Although the main application of the CNIC is to support CND and CIDCW service, it may also be used in any application where 1200 baud Bell 202 and/or CCITT V.23 FSK data reception is required.

Input Configuration

The input arrangement of the MT8841 provides an operational amplifier, as well as a bias source (V_{Ref}) which is used to bias the inputs at $V_{DD/2}$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 4.

Figure 3 shows the necessary connections for a differential input configuration.

User Interface

The CNIC provides a powerful 3-pin interface which can reduce the external hardware and software requirements. The CNIC receives the FSK signal demodulates it, and outputs the extracted data to the DATA pin. For each received stop bit start bit sequence, the CNIC outputs a fixed frequency clock string of 8 pulses at the DCLK pin. Each clock rising

sponds to the centre of each DATA bit cell
the incoming baud rate matches the DCLK
K is not generated for the stop and start
equently, DCLK will clock only valid data
pheral device such as a serial to parallel
ter or a micro-controller. The CNIC also
end of word pulse (data ready) at the $\overline{DR}$
ata ready signal indicates the reception of
it word sent from the Central Office. This
pically used to interrupt a micro-controller.
outputs together, eliminate the need for a
(Universal Asynchronous Receiver
r) or the high software overhead of
the UART function (asynchronous serial
tion).

the 3-pin interface may also output data
by voice since these frequencies are in
frequency detection band of the device.
may choose to ignore these outputs when
is not expected, or force the CNIC into its
n mode.

wn Mode

plications requiring reduced power
ion, the CNIC can be forced into power
n it is not needed to receive FSK data. This
y pulling the PWDN pin high. In powerdown
e crystal oscillator, op-amp and internal
re all disabled and the CNIC will not react
ut signal. DATA and DCLK are at logic high,
and $\overline{CD}$ are at high impedance or at logic
n pulled up with resistors.The CNIC can be
d for reception of the FSK signal by pulling
N pin to ground (see Figure 9).

Detect

ence of the FSK signal is indicated by a
at the carrier detect ($\overline{CD}$) output. This
as built in hysteresis to prevent toggling
received signal is shortly interrupted. Note
$\overline{CD}$ output is also activated by voice since
equencies are in the input frequency
band of the device. The user may choose
this output when FSK data is not expected,
he CNIC into its powerdown mode.

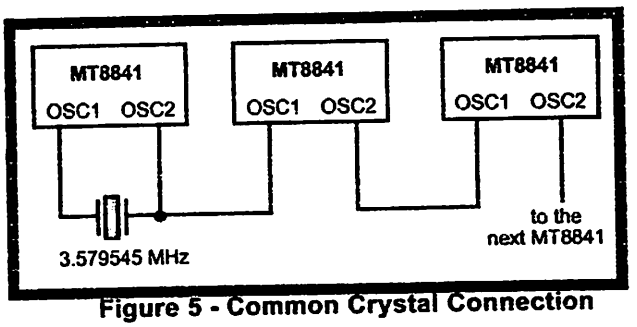


Figure 5 - Common Crystal Connection

Crystal Oscillator

The CNIC uses a crystal oscillator as the master timing source for filters and the FSK demodulator. The crystal specification is as follows:

Frequency:	3.579545 MHz
Frequency tolerance:	±0.1%(-40°C+85°C)
Resonance mode:	Parallel
Load capacitance:	18 pF
Maximum series resistance:	150 ohms
Maximum drive level (mW):	2 mW

e.g. CTS MP036S

A number of MT8841 devices can be connected as shown in Figure 5 such that only one crystal is required. The connection between OSC2 and OSC1 can be D.C. coupled as shown, or A.C. coupled using 30pF capacitors. Alternatively, the OSC1 inputs on all devices can be driven from a CMOS buffer (dc coupled) with the OSC2 outputs left unconnected.

VRef and CAP Inputs

V_{Ref} is the output of a low impedance voltage source equal to $V_{DD/2}$ and is used to bias the input op-amp. A 0.1µF capacitor is required between CAP and V_{SS} to suppress noise on V_{Ref}.

ıplications

ɜ circuit shown in Figure 6 illustrates the use of MT8841 device in a typical FSK receiver system. llcore Special Report SR-TSV-002476 specifies t the FSK receiver should be able to receive FSK nal levels as follows:

ceived Signal Level at 1200Hz:
-32dBm to -12dBm

ceived Signal Level at 2200Hz:
-36dBm to -12dBm

s condition can be attained by choosing suitable ues of R1 and R2. The MT8841 configured in a ty gain mode as shown in Fig. 6 meets the above el requirements.

· applications requiring detection of lower FSK nal level, the input op amp may be configured to ıvide adequate gain.

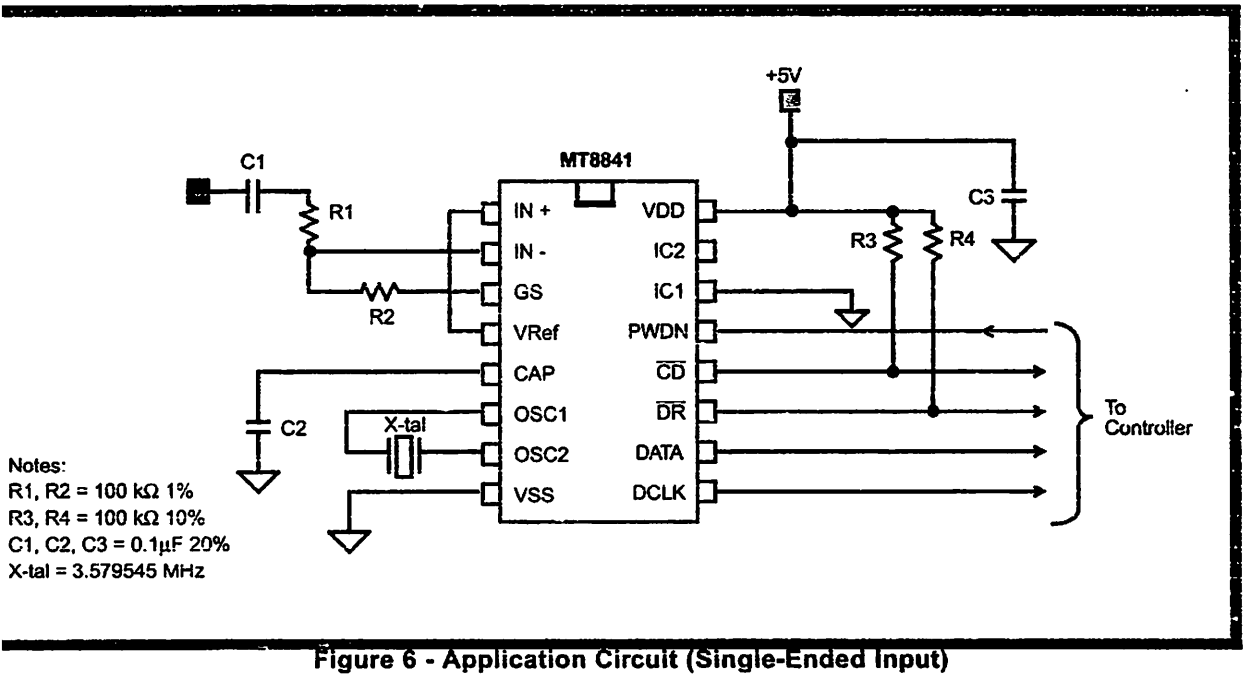


Figure 6 - Application Circuit (Single-Ended Input)

e Maximum Ratings* - Voltages are with respect to V_{SS} unless otherwise stated.

Parameter	Symbol	Min	Max	Units
Power Supply Voltage V_{DD} to V_{SS}	V_{DD}	-0.3	6	V
ige on any pin	V_P	-0.3	V_{DD}+0.3	V
ent at any pin (except V_{DD} and V_{SS})	$I_{I/O}$		±10	mA
age Temperature	T_{ST}	-65	+150	°C
tage Power Dissipation	P_D		500	mW

these values may cause permanent damage. Functional operation under these conditions is not implied.

nended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
k Frequency	f_{OSC}		3.579545		MHz	
rance on Clock Frequency	Δfc			±0.2	%	
rating Temperature		-40		+85	°C	

trical Characteristics†

Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
Standby Supply Current	IDDQ		15	100	µA	PWDN=V_{DD}
Operating Supply Current	I_{DD}		3	5	mA	PWDN=V_{SS}
Power Consumption	PO			28	mW	
Low Level Output Voltage High Level Output Voltage	V_{OL} V_{OH}	 V_{DD}-0.4		0.4	V V	I_{OL}=2.5mA I_{OH}=0.8mA
Sink Current	I_{OL}	2.5			mA	V_{OL}=0.4V
Low Level Input Voltage High Level Input Voltage	V_{IL} V_{IH}	 V_{DD}-1.2		1.2	V V	
Input Current	I_{IN}			10	µA	$V_{SS} \le V_{IN} \le V_{DD}$
Output Voltage	V_{Ref}	2.45	2.5	2.55	V	V_{DD}=5.0V No Load
Output Resistance	R_{Ref}			2	kΩ	

cal Characteristics are over recommended operating conditions unless otherwise stated.
ires are at 25°C and are for design aid only.

ectrical Characteristics† - Gain Setting Amplifier

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input Leakage Current	I_{IN}			1	µA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input Resistance	R_{in}	5			MΩ	
3	Input Offset Voltage	V_{OS}			25	mV	
4	Power Supply Rejection Ratio	PSRR	30	40		dB	1kHz ripple on V_{DD}
5	Common Mode Rejection	CMRR	30	40		dB	$V_{CMmin} \le V_{IN} \le V_{CMmax}$
6	DC Open Loop Voltage Gain	A_{VOL}	30	32		dB	
7	Unity Gain Bandwidth	f_C	.2	0.3		MHz	
8	Output Voltage Swing	V_O	0.5		V_{DD}-0.5	V_{pp}	Load ≥ 50kΩ
9	Maximum Capacitive Load (GS)	C_L			100	pF	
10	Maximum Resistive Load (GS)	R_L	50			kΩ	
11	Common Mode Range Voltage	V_{CM}	1.0		V_{DD}-1.0	V	

Electrical characteristics are over recommended operating conditions, unless otherwise stated.
Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

C Electrical Characteristics† - FSK Detection

	Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	Input Detection Level		-36 12.3		-9 275	dBm mV	1, 2, 3 1, 2, 3
2	Input Baud Rate		1188	1200	1212	baud	7
3	Input Frequency Detection Bell 202 1 (Mark) Bell 202 0 (Space) CCITT V.23 1 (Mark) CCITT V.23 0 (Space)		 1188 2178 1280.5 2068.5	 1200 2200 1300 2100	 1212 2222 1319.5 2131.5	 Hz Hz Hz Hz	 }7 BELL 202 Frequencies }7 CCITT V.23 Frequencies
4	Input Noise Tolerance $20 \log(\frac{signal}{noise})$	SNR	20			dB	2, 3, 4, 5

AC Electrical Characteristics are over recommended operating conditions, unless otherwise stated.
Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

rical Characteristics† - Timing

	Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
DN	Power-up time	t_{PU}		35	50	ms	
C1	Power-down time	t_{PD}		100	1000	µs	11
	Input FSK to $\overline{CD}$ low delay	t_{IAL}			25	ms	
D	Input FSK to $\overline{CD}$ high delay	t_{IAH}	8			ms	
	Hysteresis		8			ms	
TA	Rate		1188	1200	1212	bps	6,12
	Input FSK to DATA delay	t_{IDD}		1	5	ms	
	Rise time	t_R			200	ns	8
TA	Fall time	t_F			200	ns	8
LK	DATA to DCLK delay	t_{DCD}	6	416		µs	6, 7, 10
	DCLK to DATA delay	t_{CDD}	6	416		µs	6, 7, 10
	Frequency		1200	1202.8	1205	Hz	7
LK	High time	t_{CH}	415	416	417	µs	7
	Low time	t_{CL}	415	416	417	µs	7
LK R	DCLK to $\overline{DR}$ delay	t_{CRD}	415	416	417	µs	7
	Rise time	t_{RR}			10	µs	9
R	Fall time	t_{FF}			200	ns	9
	Low time	t_{RL}	415	416	417	µs	7

cal Characteristics are over recommended operating conditions unless otherwise stated.
ures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.

dBm=decibels above or below a reference power of 1mW into 600Ω.
Using unity gain test circuit shown in Figure 6.
Mark and Space frequencies have the same amplitude.
Band limited random noise (200-3200Hz).
Referenced to the minimum input detection level.
FSK input data at 1200 ±12 baud.
OSC1 at 3.579545 MHz ±0.2%.
10k to V_{SS}, 50pF to V_{SS}.
10k to V_{DD}, 50pF to V_{SS}.
Function of signal condition.
The device will stop functioning within this time, but more time may be required to reach I_{DDQ}.
For a repeating mark space sequence, the data stream will typically have equal 1 and 0 bit durations.

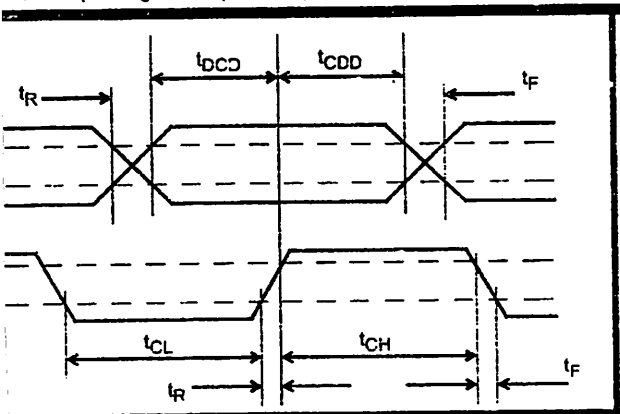


Figure 7 - DATA and DCLK Output Timing

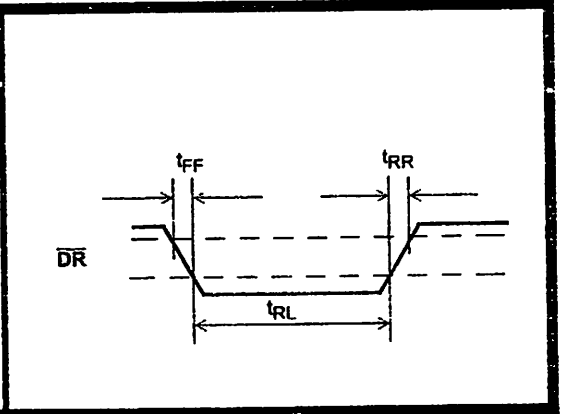


Figure 8 - $\overline{DR}$ Output Timing

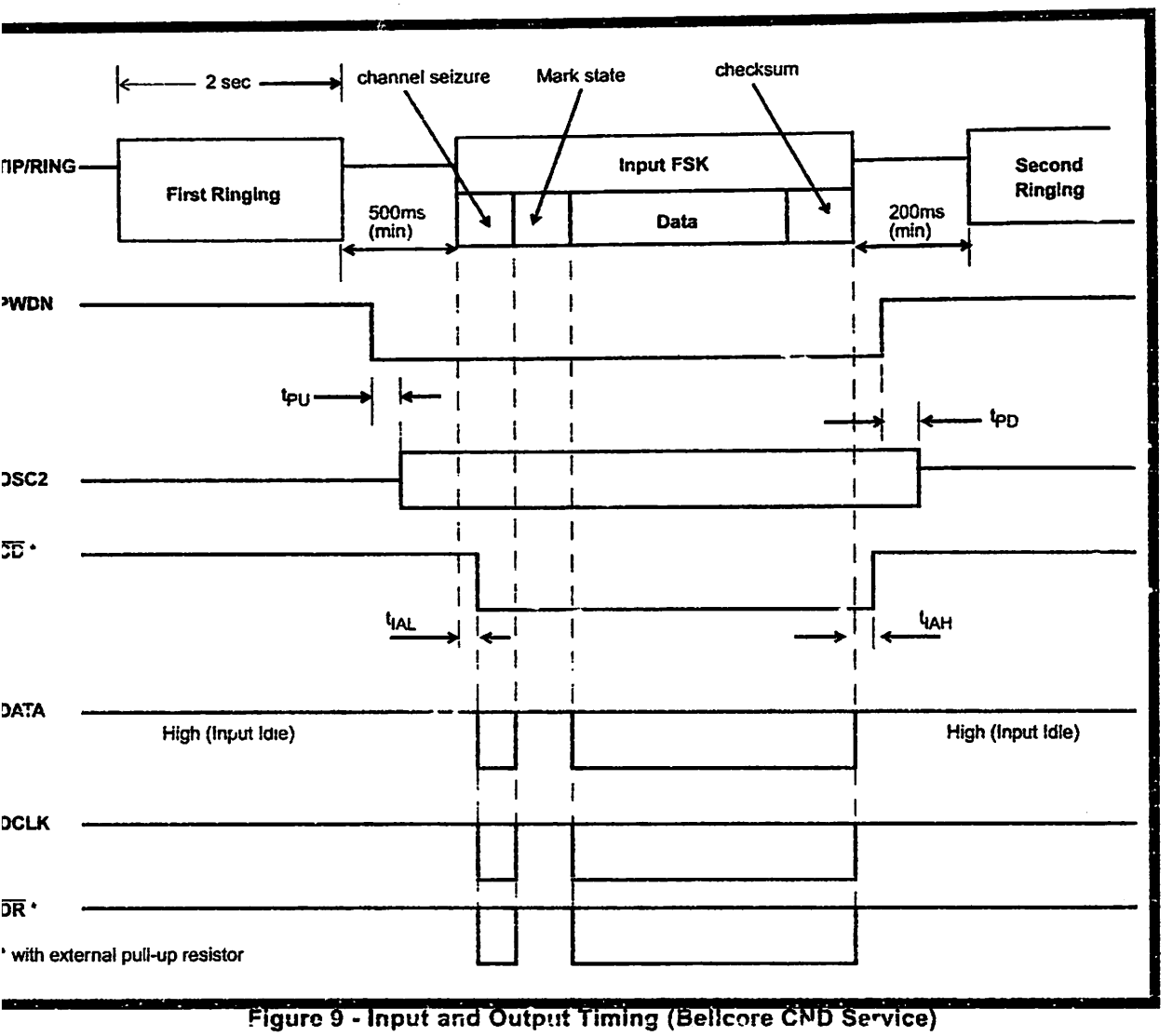


Figure 9 - Input and Output Timing (Bellcore CND Service)

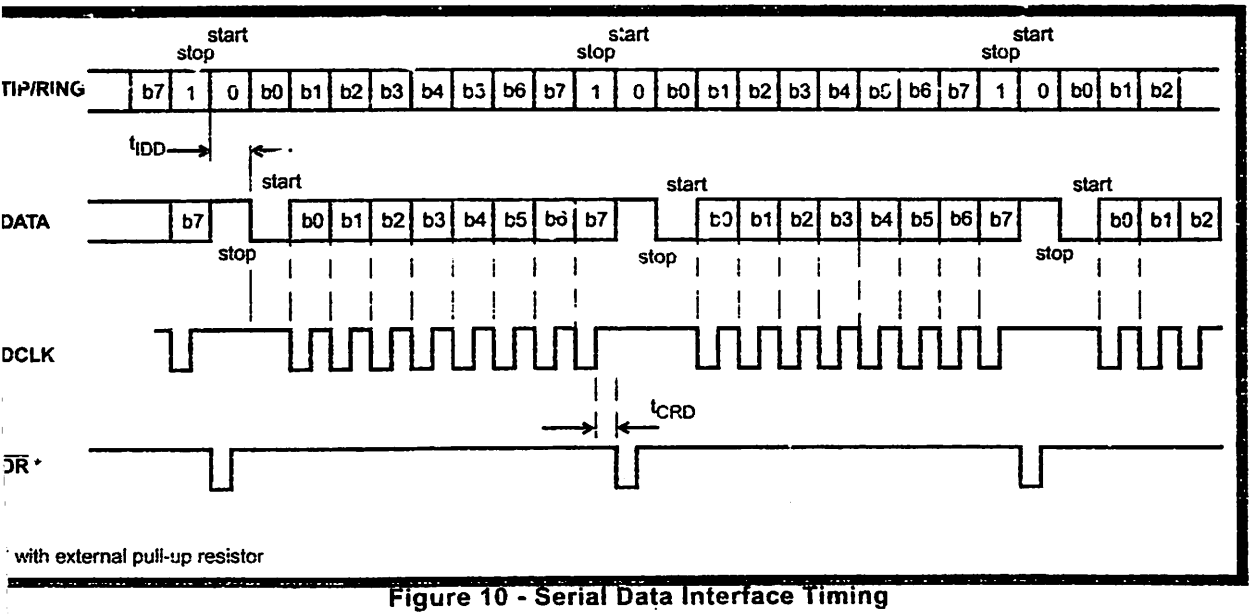


Figure 10 - Serial Data Interface Timing

```
unit Unit1;

interface

uses
  Windows, Messages, SysUtils, Variants, Classes, Graphics, Controls, Forms,
  Dialogs, DB, ADODB, Menus, ExtCtrls, StdCtrls, CPort;

type
  TForm1 = class(TForm)
    Notebook1: TNotebook;
    MainMenu1: TMainMenu;
    File1: TMenuItem;
    close1: TMenuItem;
    ADOConnection1: TADOConnection;
    ADOQuery1: TADOQuery;
    ADOConnection2: TADOConnection;
    ADOQuery2: TADOQuery;
    lbcipta: TLabel;
    button: TImage;
    GroupBox1: TGroupBox;
    Label1: TLabel;
    edbt: TEdit;
    buton: TButton;
    lbpasscipta: TLabel;
    Label2: TLabel;
    kirim1: TMenuItem;
    edtkirimdata: TEdit;
    btnkirimdata: TButton;
    Label3: TLabel;
    lblkirimdataHeksa: TLabel;
    ComPort1: TComPort;
    Label4: TLabel;
    lblkirimdatabiner: TLabel;
    Button3: TButton;
    Edtdtserial: TEdit;
    Lblterimaheksa: TLabel;
    lblterimabiner: TLabel;
    Label5: TLabel;
    Label6: TLabel;
    Button1: TButton;
    procedure close1Click(Sender: TObject);
    procedure butonClick(Sender: TObject);
    procedure buttonClick(Sender: TObject);
    procedure FormCreate(Sender: TObject);
    procedure kirim1Click(Sender: TObject);
```

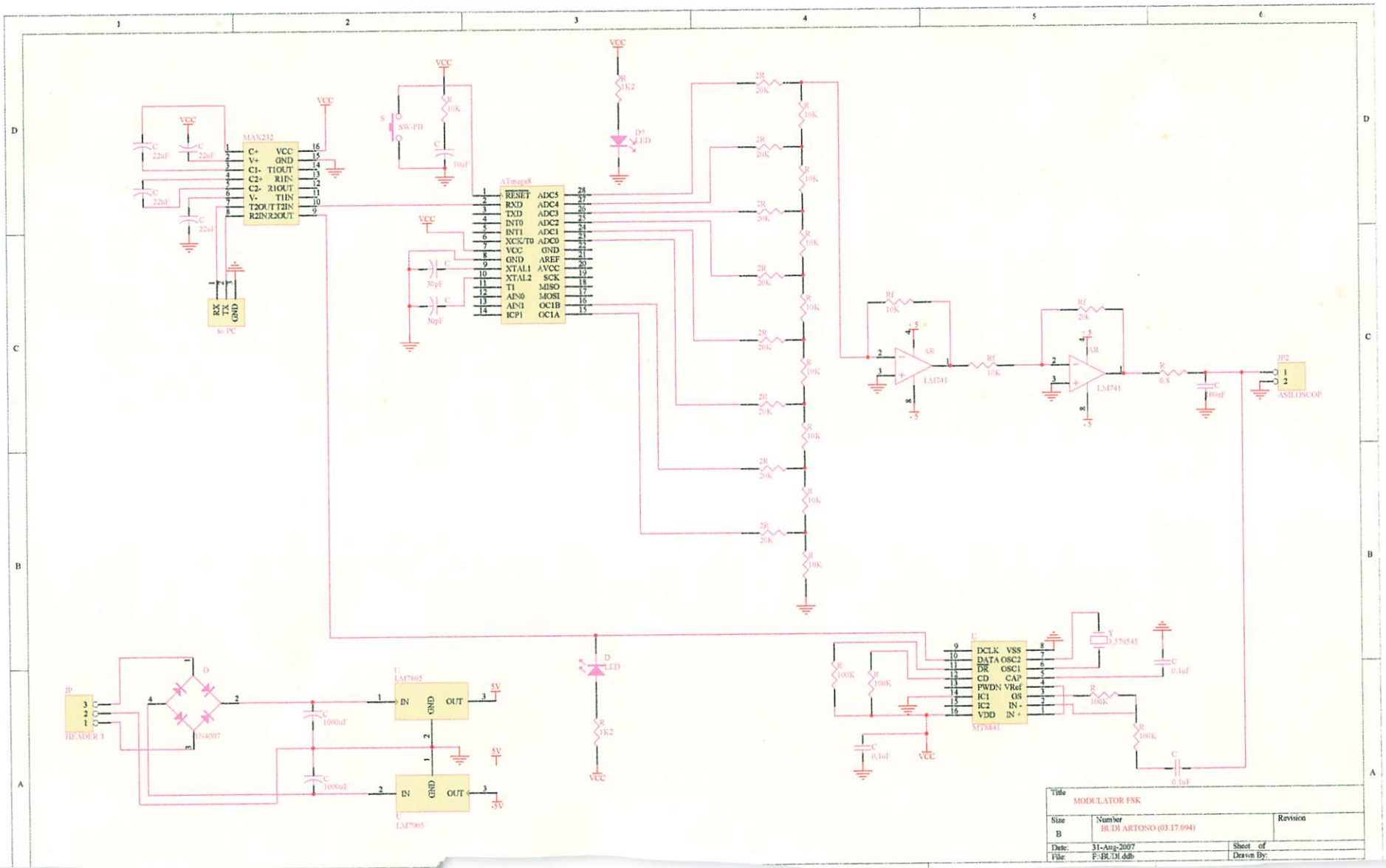
```
    procedure btnkirimdataClick(Sender: TObject);
    procedure heksa(ldtheksa:string);
    procedure biner(ldtbiner:string);
    procedure kirimmk(data:string);
    procedure ComPort1RxChar(Sender: TObject; Count: Integer);
    procedure terima1Click(Sender: TObject);
    procedure Button3Click(Sender: TObject);
    procedure Button1Click(Sender: TObject);

  private
    { Private declarations }
  public
    { Public declarations }
  end;
var
  Form1: TForm1;
  dtheksa,dtbiner,dtserial:string;

implementation

uses Unit5, Unit3;

{$R *.dfm}

procedure TForm1.kirimmk(data:string);
begin
ComPort1.WriteStr(data);

end;

procedure TForm1.heksa(ldtheksa:string);
begin
dtheksa:=IntToHex(Ord(ldtheksa[1]),2)+'  ';
end;

procedure TForm1.biner(ldtbiner:string);
var lintdt,lintmod,bt0,bt1,bt2,bt3,bt4,bt5,bt6,bt7:integer;
begin
lintdt:=Ord(ldtbiner[1]);
 //lintdt:=StrToInt(Edit5.Text);
bt0:=(lintdt div 1) mod 2;
bt1:=(lintdt div 2) mod 2;
bt2:=(lintdt div 4) mod 2;
bt3:=(lintdt div 8) mod 2;
bt4:=(lintdt div 16) mod 2;
bt5:=(lintdt div 32) mod 2;
```

```
bt6:=(lintdt div 64) mod 2;
bt7:=(lintdt div 128) mod 2;
dtbiner:=IntToStr(bt7)+IntToStr(bt6)+IntToStr(bt5)+IntToStr(bt4)+IntToStr(bt3)+IntToS
tr(bt2)+IntToStr(bt1)+IntToStr(bt0)+'  ';
//Edit5.Text:=Edit5.Text+IntToStr(lintdt);
end;

procedure TForm1.close1Click(Sender: TObject);
begin
close;
end;

procedure TForm1.butonClick(Sender: TObject);
begin
DM5.g;
end;

procedure TForm1.buttonClick(Sender: TObject);
begin
DM3.a;
end;

procedure TForm1.FormCreate(Sender: TObject);
begin
Notebook1.ActivePage:='utama';
dtheksa:='';
dtserial:='';
end;

procedure TForm1.kirim1Click(Sender: TObject);
begin
Notebook1.ActivePage:='kirim';
end;

procedure TForm1.btnkirimdataClick(Sender: TObject);
var lstr:string;
li:integer;
begin
Edtdtserial.Text:='';
lstr:=edtkirimdata.Text;
kirimmk(lstr);
lblkirimdataHeksa.Caption:='';
lblkirimdatabiner.Caption:='';
Lblterimaheksa.Caption:='';
lblterimabiner.Caption:='';
for li := 1 to length(lstr)-1 do
```

```
begin
heksa(lstr[li]);
lblkirimdataHeksa.Caption:=lblkirimdataHeksa.Caption+dtheksa;
biner(lstr[li]);
lblkirimdatabiner.Caption:=lblkirimdatabiner.Caption+dtbiner;

end;

end;

procedure TForm1.ComPort1RxChar(Sender: TObject; Count: Integer);
var ldtserial,lstr:string;
li:integer;
begin
ComPort1.ReadStr(ldtserial,Count);

Edtdtserial.Text:=Edtdtserial.Text+ldtserial;
dtserial:=Edtdtserial.Text;
if dtserial[Length(dtserial)]='#' then
begin
for li := 1 to length(dtserial)-1 do
begin
heksa(dtserial[li]);
Lblterimaheksa.Caption:=Lblterimaheksa.Caption+dtheksa;
biner(dtserial[li]);
lblterimabiner.Caption:=lblterimabiner.Caption+dtbiner;
end;
end;
end;

procedure TForm1.terima1Click(Sender: TObject);
begin
Notebook1.ActivePage:='terima';
end;

procedure TForm1.Button3Click(Sender: TObject);
begin
ComPort1.ShowSetupDialog;
end;

procedure TForm1.Button1Click(Sender: TObject);
begin
Application.Terminate;
end;

end.
```

```
/* File include */
#include <mega8.h>
#include <delay.h>


/* Pendefinisian */
#define DAC_low      PORTC       //PORTC.5-PORTC.0
#define DAC_high     PORTB       //PORTB.2-PORTB.1
#define masukan      PIND.0


/* Inisialisasi variabel global */
unsigned char index_data_keluaran;
flash unsigned char
data_keluaran_low[33]={63,25,48,7,26,41,53,60,63,60,53,41,26,7,48,25,63,38,15,56,37,
22,10,3,0,3,10,22,37,56,15,38};
flash unsigned char
data_keluaran_high[33]={2,4,4,6,6,6,6,6,6,6,6,6,6,6,4,4,2,2,2,0,0,0,0,0,0,0,0,0,0,2,2};


void init_port()
{
    DDRC=0b00111111;
    DDRB=0b00000110;
    DDRD=0b11111110;
}


void init_timer2()
{
    /* Timer ini akan digunakan sebagai oscillator */
    /* Mode yang digunakan adalah Clear Timer On Compare dengan interrupt */
    /* Mula-mula OCR0 diset untuk frekuensi 1200 Hz, 17 langkah, frekuensi clock 8
MHz */
    TCCR2=0x08;
    TIMSK=TIMSK|0x80;
    TCNT2=0;
    OCR2=203;
}


/* Fungsi saat terjadi timer 2 compare match interrupt */
/* Turn registers saving off */
#pragma savereg-
/* interrupt handler */
interrupt [4] void timer2_match(void)
```

```
{
    /* Pemanasan */
    #asm
    push r30
    push r31
    in   r30,SREG
    push r30
    #endasm

    /* Inti */
    if (index_data_keluaran!=31)index_data_keluaran++;
    else index_data_keluaran=0;

    DAC_high=data_keluaran_high[index_data_keluaran];
    DAC_low=data_keluaran_low[index_data_keluaran];

    /* Pendinginan */
    #asm
    pop r30
    out SREG,r30
    pop r31
    pop r30
    #endasm

}
/* re-enable register saving for the other interrupts */
#pragma savereg+


/* Program Utama */
void main()
{
    /* Inisialisasi */
    init_port();
    init_timer2();

    /* lets go */
    DAC_low=63;
    DAC_high=2;
    index_data_keluaran=0;
    #asm("sei");
    TCCR2=TCCR2|0x01;
    do
      {
        OCR2=masukan==0 ? 109:200;//168 : 84;
    }while(1);
```


MAX232
ATmega8
SW-PB
LED
LM741
LM7805
LM7905
1N4007
HEADER 3
ASILOSCOP
MT8841
MODULATOR FSK
BUDI ARTONO (03.17.094)
31-Aug-2007
F:\BUDI.ddb

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura – gura No.2
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Masa Bimbingan : 05-Juni-2007 s/d 05-Desember-2007
Judul Skripsi : Perencanaan dan Pembuatan Modulator FSK dengan Menggunakan Metode DDS Berbasis Mikrokontroler ATmega 8-bit.

No	Tanggal	Uraian	Paraf Pembimbing
1	2/8 2007	Bab I – III Perbaiki	
2	3/8 2007	Bab IV	
3	6/8 2007	Bab IV (diuji Gelombang) Bab V (diperbaiki)	
4	27/8 2007	Bab VI Abstraksi	
5	30/8 2007	Bab V Revisi	
6	30/8 2007	Acc ujian	
7			
8			
9			
10			

Malang,

Dosen pembimbing I

Ir.F.Yudi Limpraptono,MT
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Form S-4a

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No	Tanggal	Uraian	Paraf Pembimbing
1	2/8 2007	BAB I - III perbaiki	
2	3/8 2007	BAB I - III * sumber ditambahkan * penulisan	
3	6/8 2007	BAB III * revisi	
4	10/8 2007	BAB IV * pengujian ditambahkan	
5	13/8 2007	BAB IV (uji spektrum) V (revisi)	
6	14/8 2007	BAB V (dibetulkan)	
7	27/8 2007	dilengkapi	
8	29/8 2007	ACC KOMPRE	
9			
10			

Malang,

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Form S-4a