SKRIPSI

ALAT PENURUNAN KADAR AIR DALAM MADU DENGAN METODE PEMANAS AIR

Disusun oleh :

MUHAMMMAD YUSUF
NIM : 04.12.230

MILIK
PERPUSTAKAAN
ITN MALANG

JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI

APRIL 2009

SKRIPSI

ALAT PENGUKUR KADAR AIR DALAM MADU DENGAN METODE PEMANAS AIR

Disusun oleh :

MUHAMMAD YUSUF
NIM : 04.12.250

PERPUSTAKAAN
ITN MALANG

JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI

APRIL 2009

LEMBAR PERSETUJUAN

ALAT PENURUN KADAR AIR DALAM MADU DENGAN METODE PEMANAS AIR

SKRIPSI

Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh
Gelar Sarjana Teknik Elektronika Strata Satu (S-I)

Disusun Oleh :

MUHAMMAD YUSUF
NIM : 04.12.230

Diperiksa dan Disetujui

Dosen Pembimbing I	Dosen Pembimbing II
M.Ibrahim Ashari, ST, MT	Irmalia Suryani Faradisa,ST MT
Nip. 1030100358	Nip. 1030100365

Mengetahui
Ketua Jurusan Teknik Elektro S-I

(Ir. F. Yudi Limpraptono, MT.)
NIP.Y. 1039500274

JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
2009

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

Nama	:	Muhammad Yusuf
NIM	:	04.12.230
Jurusan	:	Teknik Elektro S-1
Konsentrasi	:	Teknik Elektronika
Judul Skripsi	:	Alat Penurun Kadar Air Dalam Madu Dengan Metode Pemanas Air

Dipertahankan di hadapan majelis penguji Skripsi jenjang Strata satu (S-1) pada :

Hari	:	Selasa
Tanggal	:	17 Maret 2009
Dengan Nilai	:	84,55(A)

Ketua Majelis Penguji

(Ir. H.Sidik Noertjahjono, MT)
NIP.Y.1028700163

Sekretaris Majelis Penguji

(Ir. F. Yudi Limpraptono, MT)
NIP.Y.1039500274

Penguji I

(Sotyohadi, ST, MSc)
NIP.Y.1039700309

Penguji II

(Joseph Dedy Irawan, ST, MT.)
NIP. 132315178

KATA PENGANTAR

Alhamdulillah telah memberikan rahmat dan hidayah-Nya, sehingga dapat menyelesaikan skripsi yang berjudul "Alat penurun kadar air menggunakan metode pemanas air" ini dengan lancar. Skripsi ini merupakan persyaratan kelulusan Studi di Jurusan Teknik Elektro S-1 Konsentrasi Teknik Elektronika ITN Malang dan untuk mencapai gelar Sarjana Teknik.

Keberhasilan peyelesaian laporan skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terima kasih kepada :

1. Bapak Ir. F. Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro S-1.
2. Bapak M.Ibrahim Ashari,ST, MT selaku Dosen Pembimbing I.
3. Ibu Irmalia Suryani Faradisa,ST MT selaku Dosen Pembimbing II.
4. Ayah dan Ibu serta saudara-saudara kami yang telah memberikan do'a restu, dorongan, semangat, dan biaya.
5. Rekan-rekan Mahasiswa jurusan Elektronika S-1 senasib seperjuanga, tdak lupa pula temen-temen kos semuanya.
6. Semua yang telah membantu dalam penyelesaian penyusunan skripsi.

Penyusun telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam menyelasaikan laporan ini. Untuk itu penyusun mengharapkan saran dan kritik yang membangun dari pembaca demi kesempurnaan laporan ini.

Harapan penyusun semoga laporan skripsi ini memberikan manfaat bagi perkembangan ilmu pengetahuan dan pembaca.

Malang, Maret 2009

Penyusun

DAFTAR ISI

LEMBAR PERSETUJUAN i

ABSTRAKSI ii

KATA PENGANTAR iii

DAFTAR ISI v

DAFTAR GAMBAR xi

DAFTAR TABEL xiv

BAB I PENDAHULUAN 1

1.1. Latar Belakang 1

1.2. Rumusan Masalah 2

1.3. Batasan Masalah 3

1.4. Tujuan 3

1.5. Metodologi 3

1.6. Sistematika Pembahasan 4

BAB II TEORI DASAR 5

2.1. Sensor kadar air 6

2.2. Sensor suhu 7

2.3. LCD (*Liquid Crystal Display*) M1632 8

2.4. *Transistor* 12

2.4.1. Transistor sebagai saklar 16

2.5. *Triac (Triode Alternatif Current)* 18

2.5.1. Karakteristik *Triac* 19

2.6. Mikrokontroler ATMEGA 8535 21

2.6.1. Konfigurasi Pin ATMega 8535 23

2.6.2. Organisasi memori 27

BAB III PERANCANGAN DAN PEMBUATAN ALAT 30

3.1. Pendahuluan 30

3.1.1 Blok Diagram Keseluruhan Sistem 30

3.2. Prinsip Kerja Alat 32

3.3. Perancangan Perangkat Keras (*Hardware*) 33

3.3.1. RangkaianSensor Kadar Air 33

3.3.2. Key pad 35

3.3.3. LCD (*Liquid Crystal Display*) 36

3.3.4. Driver motor 37

3.3.5. Driver heater 38

3.3.6. Perancangan minimum sistem ATMega8535 39

3.4. Perancangan Perangkat Lunak (*Software*) 43

3.4.1. Diagram alir (*flow chart*) 44

BAB IV PENGUJIAN DAN HASIL ANALISA 46

4.1. Pengujian mokrokontroler ATMega 8535 46

4.1.1. Tujuan 46

4.1.2. Peralatan yang digunakan 47

4.1.3. Prosedur pengujian 47

4.1.4. Hasil Pengujian 48

4.2. Pengujian sensor kadar air 49

4.2.1. Tujuan 49

4.2.2. Peralatan yang digunakan 49

4.2.3. Prosedur pengujian 50

4.2.4. Hasil Pengujian 50

4.3. Pengujian sensor suhu 51

4.3.1. Tujuan 51

4.3.2. Peralatan yang digunakan 51

4.3.3. Prosedur pengujian 51

4.3.4. Hasil Pengujian 52

4.4. Pengujian LCD (*Liquid Crystal Display*) 53

4.4.1. Tujuan 53

4.4.2. Peralatan yang digunakan 54

4.4.3. Prosedur pengujian 54

4.4.4. Hasil Pengujian 55

4.5. Pengujian driver motor AC 56

4.5.1. Tujuan 56

4.5.2. Peralatan yang digunakan 56

4.5.3. Prosedur pengujian..... 56

4.5.4. Hasil pengujian 57

4.6. Pengujian driver Heater 57

4.6.1. Tujuan 57

4.6.2. Peralatan yang digunakan 57

4.6.3. Prosedur pengujian..... 58

4.6.4. Hasil pengujian 58

4.7. Spesifikasi alat 59

BAB V PENUTUP 60

5.1. Kesimpulan 60

5.2. Saran 61

DAFTAR PUSTAKA 62

LAMPIRAN-LAMPIRAN

DAFTAR GAMBAR

2.1. Konstruksi sensor kadar air 6

2.2. Sensor suhu LM35 7

2.3. Diagram blok LCD 8

2.4. Rankaian transistor sebagai switching 13

2.5. Strutur dan simbol NPN 14

2.6. Struktur dan simbol PNP 14

2.7. Transistor bias aju dan balik 14

2.8. Karakteristik Transistor 16

2.9. Rangkaian transistor sebagai saklar 17

2.10. Triac 18

2.11. Bias Forward dan Bias reverse Triac 18

2.12. Rangkaian Percobaan Karakteristik Forward dan Reverse 19

2.13. Kurva karkteristik triac 19

2.14. Rangkaian dasar kontrol 20

2.15. Bentuk gelombang tegangan triac 20

2.16. Blok diagram ATMEGA8535 22

2.17. Konfigurasi pin ATMega8535 23

2.18. Map Memori Program Flash Memori 27

2.19. Memori Map Program Data Memori 28

2.20. Logika reset mikrokontroller 29

3.1. Diagram Blok Keseluruhan Sistem 31

3.2. Konstruksi sensor kadar air 34

3.3. Rangkaian sensor kadar air 34

3.4. Rangkaian Keypad 35

3.5. Perancangan Rangkaian LCD (*Liquid Crystal Display*) 76

3.6. Rangkaian driver motor 37

3.7. Rangkaian driver heater 38

3.8. Rangkaian minium system ATMega8535 40

3.9. Rangkaian Reset 41

3.10. Rangkaian clok 42

3.11. Flowchart total sistem 44

4.1. Diagram Blok Pengujian Mikrokontroler 47

4.2. Hasil pengujian tampilan LED 48

4.3. Diagram blok pengujian Sensor kadar air 50

4.4. Diagram blok pengujian sensor suhu 51

4.5. Grafik perbandingan tegangan out LM35 dengan temperatur 53

4.6. Rangkaian LCD (*Liquid Crystal Display*) 54

4.7. Tampilan hasil pengujian LCD 55

4.8. Diagram blok pengujian driver motor 56

4.9. Diagram blok pengujian driver heater 58

DAFTAR TABEL

2.1. Konfigurasi pin-pin LCD 9

2.2. Fungsi alternatif dar pin port A..... 24

2.3. Fungsi alternatif dar pin port C..... 25

2.4. Fungsi alternatif dar pin port D..... 26

4.1. Hasil Pengujian Sistem Mikrokontroler 49

4.2. Data ADC yang ditampilkan LCD 50

4.3. Hasil pengujian tegangan output 52

4.4. Hasil pengujian rangkaian driver motor 57

4.5. Hasil pengujian rangkaian driver heater 58

ABSTRAKSI

ALAT PENURUN KADAR AIR DALAM MADU DENGAN METODE PEMANAS AIR

Muhammad Yusuf
04.12.230
Fakultas Teknologi Industri, Jurusan Teknik Elektro S1,
Konsentrasi Teknik Elektronika, Institut Teknologi Nasional Malang
Jln. Raya Karanglo Km 2 Malang
Email: iyus.hudi@gmail.com

Dosen Pembimbing : **I. M.Ibrahim Ashari, ST, MT**
II. Irmalia Suryani Faradisa,ST MT

Kata Kunci : Penurun Kadar Air Metode Pemanas Air

Pada Laporan Tugas Akhir ini telah dirancang sebuah alat penurun kadar air pada madu yang dilengakapi dengan sistem pemanas air. Alat ini memiliki sensor kadar air yang berupa penghatar listrik dan memiliki sensor suhu sebagai pemeriksa suhu, agar pada waktu proses penurunan kadar air dengan system pemanasan tidak melebihi 65°C. Output dari sensor kadar air yang berupa tegangan yang kemudian diperkuat oleh buffer LF351 agar dapat dibaca oleh ADC. Data untuk menurunkan kadar air pada alat ini di masukkan melalui keypad matrik 4x4 dimana data yang dimasukkan adalah data dengan satuan % kadar air. Sistem ini juga dilengkapi dengan LCD untuk tampilannya.

BAB I
PENDAHULUAN

1.1. Latar Belakang

Madu menjadi salah satu komoditi ekspor bagi Indonesia. Namun pada setiap madu mempunyai kandungan air yang beragam. Tinggi rendah kadar air dalam madu sangat dipengaruhi sumber nectar, jenis tanah, cara pemanenan, tahun pemanenan, iklim, dan cuaca di lokasi penggembalaan lebah. Sesuai ketetapan SNI (Standar Nasional Indonesia), bahwa madu yang diekspor adalah madu dengan kadar air di bawah 22%.

Indonesia sangat potensial dalam pengembangan produksi madu. Tidak hanya karena wilayahnya yang sangat cocok karena termasuk daerah tropis tetapi juga jumlah peternaknya yang kian bertambah dari waktu ke waktu. Pemerintah pun tidak tinggal diam menanggapi kemajuan ini, melalui Dinas Kehutanan, Pemerintah memberikan penyuluhan dan berbagai macam fasilitas. Salah satu fasilitas yang diberikan adalah sentra penurunan kadar air madu. Di sentra ini terdapat alat penurun kadar air yang disebut *dehumidifier*. Alat ini memiliki kelemahan yaitu pada biaya proses penurunan kadar air akan sangat mahal bila madu yang diproses kurang dari 1 kuintal. Padahal tidak semua peternak madu panen dalam jumlah banyak. Selain itu membutuhkan daya listrik yang besar dan ruangan khusus untuk mengoperasikannya.

Selain pada penurunan kadar air, pengukuran kadar air juga menjadi masalah tersendiri bagi para peternak lebah. Alat pengukur kadar air disebut

refraktometer. Alat ini mahal harganya, sehingga jarang sekali peternak lebah yang memilikinya.

Untuk itu dibuat alat penurun kadar air madu ini yang diharapkan bisa membantu para peternak lebah yang mempunyai jumlah hasil panen sedikit sehingga diharapkan biaya proses akan menjadi lebih rendah. Alat penurun ini juga dilengkapi dengan pengukur kadar air pada madu, sehingga peternak dapat melakukan pengukuran terhadap madu hasil panennya, untuk nantinya dapat menentukan madu tersebut akan diturunkan kadar airnya atau tidak.

Dengan alat ini diharapkam tidak ada lagi peternak lebah terutama peternak yang mempunyai hasil panen sedikit yang merasa rugi dan diharapkan juga tidak ada madu yang beredar dengan kualitas rendah .

1.2. Rumusan Masalah

Mengacu pada permasalahan yang ada dan sering terjadi maka rumusan masalah ditekankan pada:

1. Bagaimana merancang sebuah alat penurun kadar air dalam madu dengan metode pemanas air menggunakan mikrocontroller AVR ATMega8535.
2. Bagaimana mengatur suhu dalam batas yang diinginkan saat pemanasan yaitu antara 60° C – 65° C dan mengatur kesetabilan putaran dalam pengadukan dengan waktu yang dikehendaki.

1.3. Batasan Masalah

Agar pembahasan tidak terlalu meluas maka penyusun perlu membuat batasan-batasan masalah yang meliputi:

1. Alat ini menggunakan komponen sensor kadar air (Konduktor).
2. Untuk pengolahan data menggunakan mikrokontroller AVR ATMega8535.
3. Untuk tampilan menggunakan LCD.
4. Menggunakan 1 Liter madu Untuk sampel percobaan.
5. Tiga jenis madu yang di uji coba.

1.4. Tujuan

Tujuan kami membuat proposal skripsi ini adalah untuk merancang dan membuat alat penurun kadar air dalam madu dengan metode pemanas air, agar dapat bermanfaat oleh peternak lebah sekala kecil.

1.5. Metodologi

Metodologi yang dipakai dalam pembuatan skripsi ini adalah:

1. Studi Literatur

   Mencari referensi-referensi yang berhubungan dengan perencanaan dan pembuatan alat yang akan dibuat.

2. Penelitian Lapangan

   Melakukan penelitian secara langsung mengenai objek-objek yang berhubungan langsung dengan perencanaan alat yang akan dibuat.

3. Pengolahan Data

   Mengolah Data dengan jalan membuat analisa dan menarik kesimpulan dari hasil pengujian yang ada.

1.6. Sistematika Pembahasan

Sistematika pembahasan dari skripsi ini terdiri dari pokok pembahasan yang saling berkaitan antara satu dengan lainnya, yaitu :

BAB I Pendahuluan

Pada bab ini dibahas tentang latar belakang permasalahan, rumusan masalah, batasan masalah, sistematika pembahasan dari alat yang direncanakan.

BAB II Landasan Teori

Pada bab ini dibahas tentang teori-teori yang mendukung dalam perencanaan dan pembuatan alat ini yang meliputi sensor kadar air, pengadukan, pemanasan antara 60°C - 65°C.

BAB III Perencanaan Dan Pembuatan Alat

Pada bab ini dibahas tentang perencanaan dan pembuatan keseluruhan sistem perangkat keras (hardware) dan perangkat lunak (software).

BAB IV Pengujian Alat

Pada bab ini dibahas tentang proses serta hasil dari pengujian alat, yang didasarkan oleh pengukuran-pengukuran.

BAB V Penutup

Pada bab ini akan disampaikan kesimpulan dari perencanaan dan pembuatan sistem ini.

BAB II

LANDASAN TEORI

Penurunan kadar air pada madu yang selama ini sering dilakukan oleh pada peternak lebah adalah menggunakan teknik pencampuran madu dan penggunaan *dehumidifier.*

Teknik pencampuran madu maksudnya adalah dengan cara mencampur madu berkadar air tinggi dengan berkadar air rendah dengan perbandingan tertentu. Teknik pencampuran ini mempunyai kelemahan antara lain:

a. Adanya madu berkadar air rendah yang dikorbankan. Padahal selain telah bernilai mahal, madu berkadar air rendah diperoleh dari waktu penggembalaan yang lama.
b. Persentase perbandingan antar jenis madu yang sulit.

Penggunaan Dehumidifier memiliki kelemahan:

a. Biaya proses relatif mahal, terutama untuk hasil madu dibawah 1kuintal.
b. Memerlukan daya listrik yang besar yaitu 3000 Watt.
c. Memerlukan ruangan khusus.
d. Harga alat mahal.

2.1. Sensor Kadar Air

Pada alat ini menggunakan sensor berupa dua buah logam sejenis. Logam sejenis digunakan untuk meminimalisasi adanya proses elektrokimia, dimana dengan jenis logam yang sama maka tidak ada beda potensial antar kutub sehingga tidak ada partikel yang terbawa arus listrik untuk melapisi kutub lainnya.

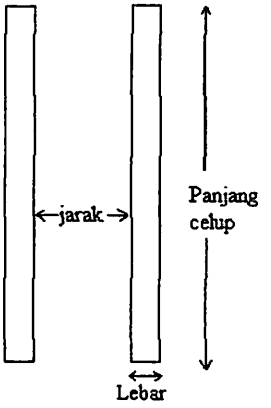
Sensor kadar air terbuat dari bahan terlapis logam Krom. Pemilihan jenis ini adalah karena anti karat. Selain itu juga memiliki lapisan yang licin atau halus sehingga madu juga tidak mudah menempel, sensor mudah dibersihkan.

Rumus resistifitas adalah:

$$R = \rho \frac{L}{A}$$

ρ = massa jenis; L = panjang; A = luas penampang

Dengan melihat rumus, dapat disimpulkan bahwa dalam sensor kadar air, resistivitas dipengaruhi oleh luas permukaan sensor dan konduktivitas media perantara diantara sensor. Media dalam hal ini adalah madu yaitu pada kadar airnya. Karena air dalam madu memiliki resistivitas yang dominan daripada bahan lainnya. Makin lebar permukaan sensor, makin tinggi kadar airnya maka makin rendah resistansinya, begitu juga sebaliknya. Gambar 2.1 merupakan konstruksi sensor kadar air.



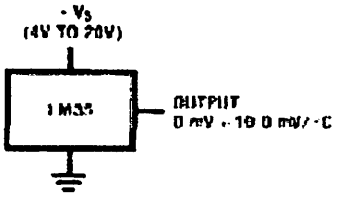
Gambar 2.1. Konstruksi Sensor Kadar Air.

Lebar permukaan yang tercelup madu untuk setiap bilah sensor adalah :
L = Panjang x Lebar
= 15mm x 7mm
= 105 mm^2

2.2. Sensor Suhu

Pada pembuatan alat ini digunakan sensor temperatur LM35 karena mempunyai keluaran linear, murah, dan mudah dalam perencanaannya. Pada dasarnya IC ini merupakan jenis IC yang output tegangannya sensitif terhadap temperatur.

Salah satu jenis IC ini adalah produksi Nasional semikonduktor yaitu LM35, yang memiliki jangkauan dari -55°C sampai +150°C. Gambar 2.2 merupakan sensor panas LM35 :



Gamabar 2.2.Sensor Panas LM35

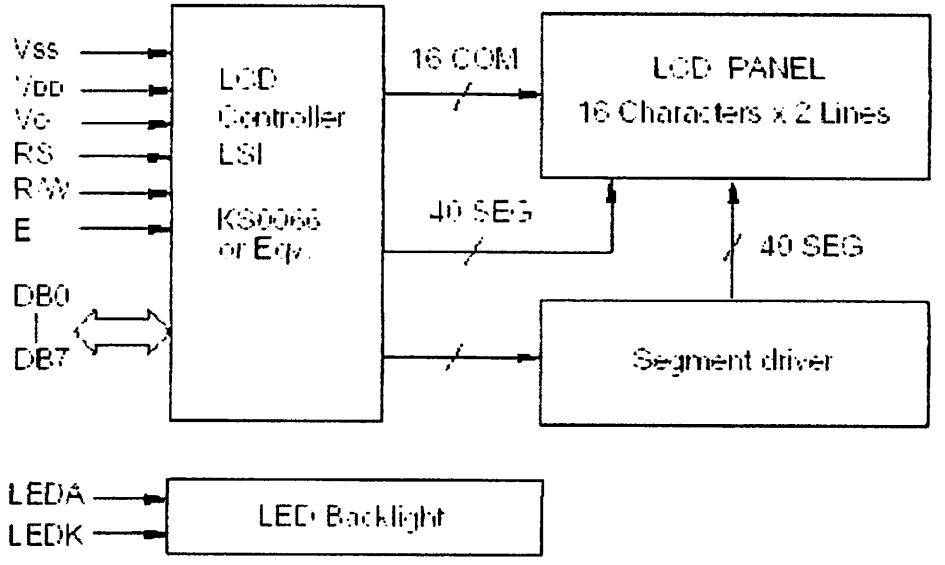
*(National Semiconductor,1994).

Rangkaian IC sensor ini mampu mengeliminasi kesalahan linear, tetapi kelemahan sensor ini adalah timbulnya kesalahan akibat *self heating*. Untuk mengurangi efek ini adalah dengan cara mengoperasikan IC pada arus minimum dan cukup mengatur sensor dan tahanan (potensiometer) dikalibrasi pada temperatur kerja maksimum. IC ini memiliki resolusi sebesar 10mV/°C. Artinya setiap kenaikan suhu 1°C maka tegangannya bertambah 10mV atau sebaliknya.

2.3. LCD

Liquid Crystal Display (LCD) merupakan suatu bentuk kristal cair yang akan beremulsi apabila dikenakan tegangan padanya. Bagian ini berupa *dot matrix* 5x7 LCD sehingga jenis huruf yang mampu ditampilkan akan lebih banyak dan lebih baik resolusinya jika dibandingkan dengan *seven segment* atau 16 *segment.*

Liquid adalah modul tampilan yang mempunyai konsumsi daya yang relatif rendah dan terdapat sebuah modul *controller* CMOS di dalamnya. Kontroller tersebut sebagai pembangkit dari karakter ROM / RAM dan *display* data RAM. Semua fungsi tampilan dikontrol oleh suatu unit mikrokontroller. Masukan yang diperlukan untuk mengendalikan modul ini berupa data *bus* yang masih termultipleks dengan *bus* alamat serta 3 bit sinyal kontrol. Sementara pengendalian *dot matrix* LCD dilakukan secara internal oleh kontroller yang sudah ada pada modul LCD. Gambar diagram blok LCD seperti ditunjukkan pada gambar 2.3



Gambar 2.3. Diagram Blok LCD

Sedangkan konfigurasi pin-pin dari LCD ditunjukkan pada tabel 2-1 :

Tabel 2-1. Konfigurasi Pin-pin LCD

Pin No.	Symbol	Level	Function
1	Vss	-	Ground
2	VDD	-	Power Supply for Logic (+5V)
3	Vo	-	Power Supply for LCD
4	RS	H/L	Register Selection H: Display Data L: Instruction Code
5	R/W	H/L	Read/Write Selection H: Read Operation L: Write Operation
6	E	H, H->L	Enable Signal. Read data when E is "H", write data at the falling edge of E.
7	DB0	H/L	In 8-bit mode, used as low order bi-directional data bus. In 4-bit mode, open these terminals.
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	In 8-bit mode, used as high order bi-directional data bus. In 4 bit mode, used as both high and low order data bus.
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	
15	LEDA	-	LED Power Supply (+5V)
16	LEDK	-	LED Power Supply (0v)

Operasi-operasi dasar pada LCD:

a) *Register*

Kontroller dari LCD mempunyai dua buah register 8 bit yaitu register instruksi (IR) dan register data (DR). Kedua register tersebut dipilih melalui register select (SR). IR menyimpan instruksi seperti *display clear, cursor shift* dan *display data* (DD RAM) serta *character generatot* (CG RAM). DR menyimpan data untuk dituliskan ke DD RAM atau CG RAM ataupun membaca data dari DD RAM atau CG RAM. Ketika data ditulis ke DD RAM atau CG RAM, maka DR secara otomatis menulis data ke DD RAM atau CG RAM. Ketika data dari DD

RAM atau CG RAM akan dibaca, maka alamat data ditulis pada IR, sedangkan data akan dimasukkan melalui DR dan mikroprosessor membaca data dari DR

b) *Busy Flag*

Busy flag menunjukkan bahwa modul siap untuk menerima instruksi selanjutnya. Sebagaimana terlihat pada tabel register seleksi sinyal akan melalui DB7, jika RS=0 R/W=1. Jika bernilai 1, maka modul siap melakukan kerja internal dan instruksi tidak akan diterima. Oleh karena itu status dari *flag* harus diperiksa sebelum melaksanakan selanjutnya.

c) *Address Counter* (AC)

AC menunjukkan lokasi dalam modul LCD. Pemilihan lokasi alamat diberikan lewat register instruksi (IR). Ketika data pada A, maka AC secara otomatis menaikkan atau menurunkan alamat tergantung dari *entry mode set.*

d) *Display Data* (DD)

Pada LCD masing-masing *line* mempunyai *range* alamat tersendiri. Alamat itu dienkripsikan dengan bilangan heksadesimal. Untuk *line* 1 *range* alamat berkisar antar 00h-0Fh, sedangkan untuk *line* 2 *range* alamat berkisar antara 40h-41h.

e) *Character Generator Rom* (CG ROM)

CG ROM mempunyai tipe *dot matrix* 5x7, yang pada LCD telah tersedia ROM sebagai karakter dalam kode ASCII

f) *Character Generator Ram* (CG RAM)

CG RAM dipakai untuk pembuatan karakter tersendiri melalui program.

Inisialisasi pada LCD dijelaskan sebagai berikut:

1) *Display Clear*

Membersihkan semua tampilan yang ada pada LCD serta menyimpan, sedangkan kursor kembali ke posisi semula.

2) *Cursor Home*

Hanya membersihkan semua tampilan dan kursor kembali ke posisi semula

3) *Entry Mode Set*

Layar beraksi sebagai tampilan karakter tulis:

S = I/O: menggeser layar

I/O = 1: kursor bergerak ke kanan dan layar bergerak ke kiri

I/O = 0: kursor bergeser ke kiri dan layar bergerak ke kanan.

4) *Display On Off Control*

D = 1: Layar On

D = 0: Layar Off

C = 1: Kursor On

C = 0: Kursor Off

B = 1: Layar berkedip-kedip

B = 0: Layar Tidak Berkedip-kedip

5) *Cursor Display Shift*

S/C = 1: LCD diidentifikasikan sebagai layar

S/C = 0: LCD diidentifikasikan sebagai kursor

R/L = 1: menggeser 1 spasi ke kanan

R/L = 0: menggeser 1 spasi ke kiri.

6) *Function Set*

DL = 1: panjang data LCD pada mode 8 bit (DB7-DB0)

DL =0: panjang data LCD pada mode 4 bit (DB7-DB4) 4 bit upper ditransfer terlebih dahulu kemudian 4 bit lower

N = 1/0: LCD menggunakan 2 atau 1 baris karakter

F = 1/0: LCD menggunakan 5x10 atau 5x7 *dot* per karakter.

7) CG RAM *Address set*

Menulis alamat RAM ke karakter

8) DD RAM

Menulis alamat RAM ke tampilan

9) BF / *Address Read*

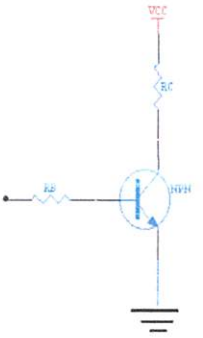
B/F = 1/0: LCD dalam keadaan sibuk atau tidak sibuk

10) *Data Read From* DD RAM *Or* CG RAM

Membaca byte dari alamat terakhir RAM yang dipilih.

2.4. Transistor

Rangkaian transistor sebagai switching adalah mengerjakan transistor pada daerah saturasi ketika mendapat sinyal saat melakukan *transmitter*. Oleh karena itu, diperlukan hfe dari transistor saturasi. Rangkaian lengkap transistor sebagai switching dapat dilihat pada gambar 2.4 :



Gambar 2.4. Rangkaian Transistor sebagai Switching

Persamaan yang dapat diperoleh dari rangkaian di atas adalah :

$$Ib = Vbb - \frac{Vbe}{Rb}$$

Keterangan :

Vcc = Tegangan inputan pada kolektor

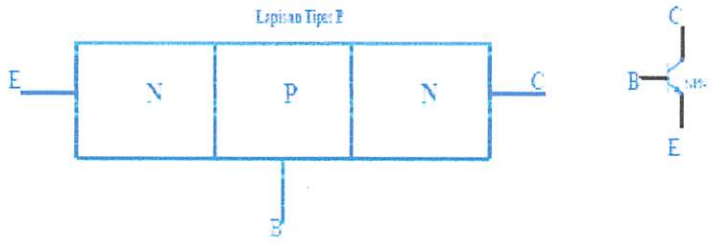
Vbb = tegangan inputan pada basis

Ic = arus kolektor

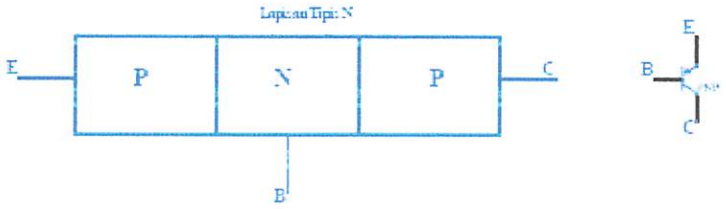
Ib = arus basis

Rb = resistansi pada basis

Transistor adalah suatu komponen semikonduktor yang pada dasarnya seperti 2 buah dioda sebab mempunyai 2 junction yaitu yang pertama adalah antara emitor dan basis, sedangkan yang kedua adalah antara basis dan kolektor. Selain itu transistor disebut juga suatu monokristal semikonduktor dimana terjadi pertemuan antara P-N dan N-P yang dapat dibuat menjadi dua kemungkinan. Transistor disebut juga sebagai junction transistor atau transistor bipolar tang memiliki tiga pin basis, kolektor, emitor.



Gambar 2.5. Struktur dan Simbol NPN

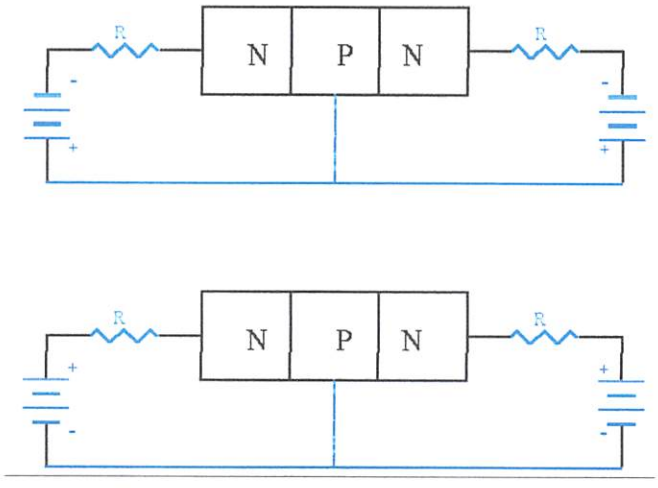


Gambar 2.6. Struktur dan Simbol PNP

Cara membias transistor adalah :

1) Pertemuan emitor basis diberi polaritas arah maju (forward).

2) Pertemuan basis kolektor diberi polaritas mundur (reverse).



Gambar 2.7. a) Kedua sambungan dibias maju

b) Kedua sambungan dibias balik

Pada gambar 2.7(a) baterai yang terletak di sebelah dibias maju (forward) dioda emitor dan baterai yang terletak di sebelah kanan membias maju dioda kolektor. Elektron bebas masuk ke dalam emitor dan kolektor transistor, bergabung dengan basis menuju polaritas positif.

Pada gambar 2.7(b) menunjukkan cara lain untuk membias transistor. Kedua dioda dibias balik (reverse). Untuk keadaan ini arus kecil dan hanya terdiri dari 2 jenis pembawa muatan minoritas, yang keluar dari kaki kolektor dan kaki emitor.

Transistor mempunyai 2 keadaan yaitu keadaan kerja penuh (saturasi) dan keadaan tidak bekerja (cut off). Perubahannya dapat berupa arus atau tegangan. Pada keadaan kerja penuh (saturasi) tegangan kolektor akan menjadi rendah atau mendekati nol, dengan demikian arus kolektor akan menjadi sangat besar dan arus yang menuju beban kecil. Pada keadaan tidak bekerja (cut off) tegangan kolektor akan menjadi besar, dengan demikian arus kolektor akan menuju beban. Pada kondisi normal masukannya tidak dibias sehingga titik kerjanya berada pada kondisi cut-off dan tidak ada arus yang menuju beban. Apabila transistor masukannya diberi bias maka arus yang mengalir adalah :

$$Ib = \frac{Ic}{hfe}$$

Keterangan :

Ib = arus basis

Ic = arus kolektor

hfe= penguatan transistor

Sedangkan untuk mencari nilai tahanan basis transistor Rb yang berfungsi sebagai pembatas arus maka harga Rb dapat ditentukan dengan rumus :

$$Rb = \frac{(Vbb - Vbe)}{Ib}$$

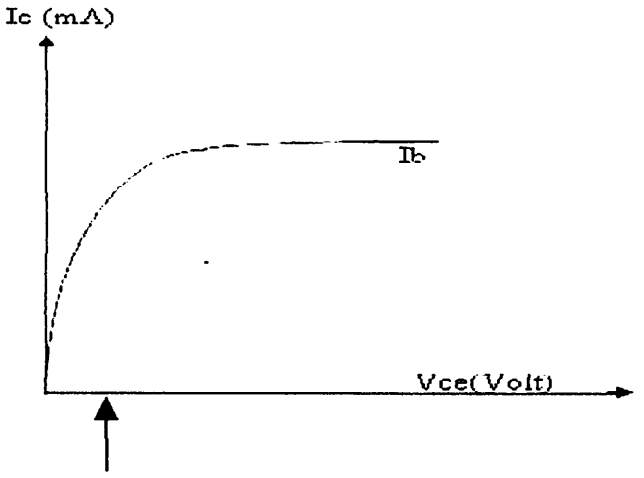
Keterangan :

Rb = tahanan basis

Vbb = tegangan inputan basis

Vbe = tegangan basis emitor

Ib = arus basis



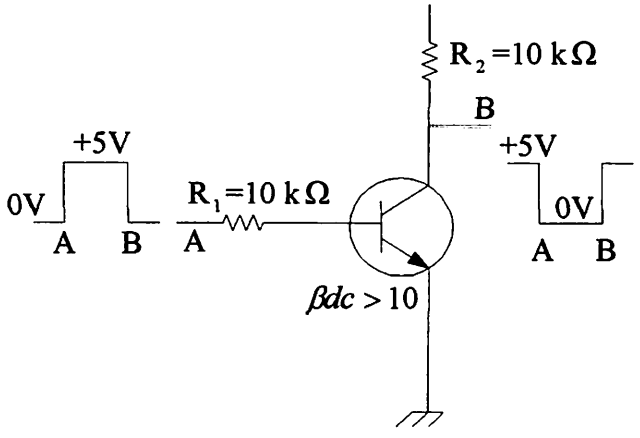
Gambar 2.8. Karakteristik Transistor

Transistor dapat dibuat sebagai saklar elektronik yang memiliki kelebihan-kelebihan dibandingkan dengan saklar mekanik biasa antara lain tidak ada bagian yang bergerak tanpa adanya sobekan (aus), tidak ada pengapian kontak bekerja dengan kecepatan tinggi serta biaya yang relative murah.

2.4.1. Transistor sebagai saklar

Keluaran suatu rangkaian logika adalah salah satu diantara tegangan rendah atau tinggi. Sebagai contoh, Gambar 2-9 memperlihatkan sebuah rangkaian logika sederhana yang menggunakan transistor dengan βdc lebih besar dari 10. Sebelum titik waktu A, tegangan masukan adalah nol dan transistor terpancung (cut off), oleh karenanya tegangan keluaran adalah +5V. Pada titik

waktu A, tegangan waktu masukan berpindah dari 0V ke +5V, cukup untuk mendorong transistor kekeadaan jenuh secara ideal, tegangan keluaran langsung jatuh dari +5V ke 0V. Selanjutnya pada titik waktu B, tegangan masukan jatuh kembali ke 0V, dan tegangan keluaran kembali ke +5V. hal yang penting untuk diingat adalah : keluaran rangkaian logika adalah salah satu diantara tegangan rendah atau tinggi.



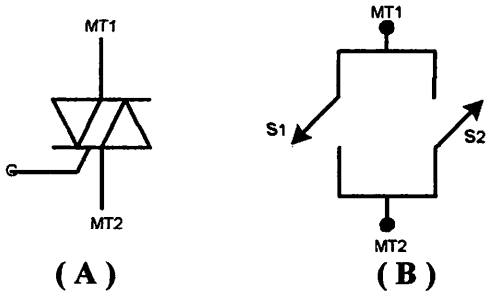
Gambar 2-9 Rangkaian Transistor sebagai saklar

Tegangan diatas dan dibawah 0,6 Volt, kedua tegangan ini disebut sebagai logika 1 untuk on dan logika 0 untuk off.

Jika kedua tingkatan tegangan ini terlalu dekat bedanya, misalnya 0,5 Volt dan 0,7 Volt maka ada kemungkinan bahwa transistor tidak akan selalu switch on dan off, karena adanya toleransi dan perubahan temperatur. Jadi biasanya tingkatan logika dibuat tidak terlalu dekat logika 1 mungkin 6 Volt dan logika 0 dibawah 0,25 Volt dengan tidak ada apa - apa diantaranya.

2.5. Triac (Triode Alternating Current)

Triac adalah saklar triode untuk arus bolak-balik. Berdasarkan gambar 2.10 triac tersusun oleh 2 buah SCR secara paralel. Simbol triac dan rangkaian pengganti sebagai saklar seperti gambar 2.10.



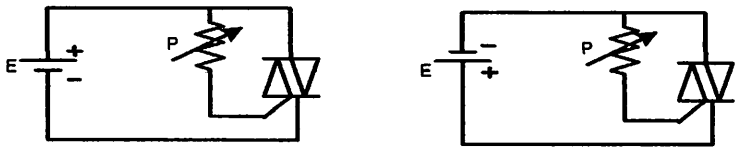
GAMBAR 2.10

(A) Simbol Triac

(B) Rangkaian Penggantinya Sebagai Saklar

Pada gambar 2.10 triac terdiri dari 3 kaki yaitu: Gate; MT_1; MT2, dengan prinsip kerja apabila MT1 diberi *forward* bias, maka saklar S_1 menutup (ON), dan sebaliknya jika MT1 diberi *reverse* bias menyebabkan saklar S_2 menutup, dengan kata lain triac bekerja secara bergantian.

Skema pemberian *forward* bias maupun *reverse* bias adalah seperti gambar 2.10.



GAMBAR 2.11

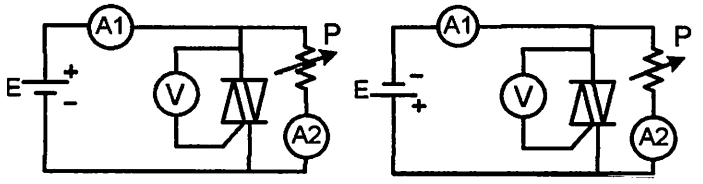
(A) Forward Bias

(B) Reverse Bias

Triac dapat dipakai untuk alat kontrol rangkaian arus bolak-balik (AC) pada beban atau juga untuk pengatur daya pada beban.

2.5.1. Karakteristik Triac

Rangkaian percobaan untuk karakteristik triac, seperti pada gambar 2.12



(A) (B)

GAMBAR 2.12. Rangkaian Percobaan Karakteristik Triac

(A) Rangkaian Untuk Karakteristik Forward

(B) Rangkaian Untuk Karakteristik Reverse

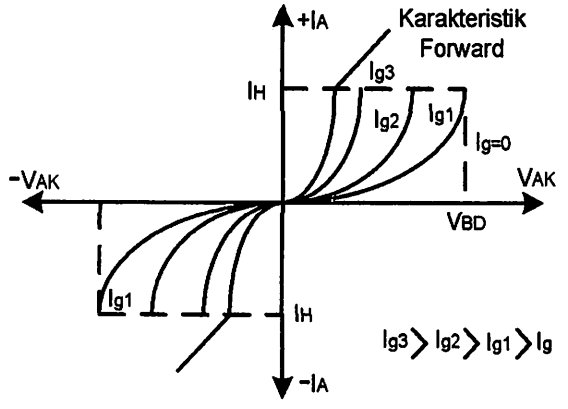
A1 = Amperemeter Untuk Mengukur Arus Melalui Triac

A2 = Amperemeter Untuk Mengukur Arus Gate

V = Voltmeter Untuk Mengukur V Breakdown antara MT1 dan MT2

E = Sumber *Arus*

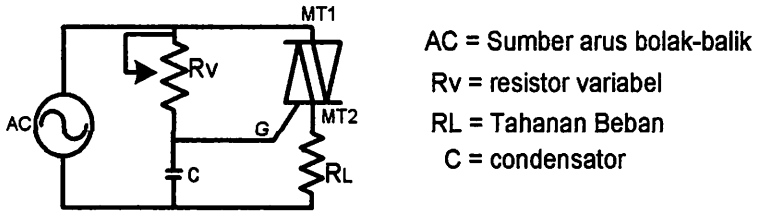
Kurva karakteristik triac seperti terlihat pada gambar 2.13



Gambar 2.13. Kurva Karakteristik Triac.Tidak Ada Perbedaan Antara Karakteristik Forward Dan Reverse-nya

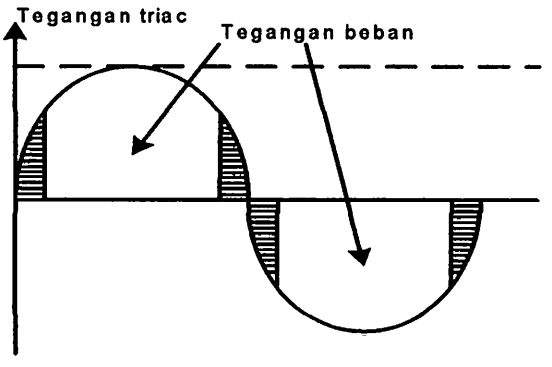
V_{BD} = *Tegangan BreakDown* I_g = *Arus Gate*
I_H = *Arus Holding* V_{AK} = *Tegangan MT1 Triac*

Rangkain dasarnya dapat dijelaskan pada gambar 2.14



GAMBAR 2.14 Rangkaian Dasar Kontrol

Jika resistor (Tahanan) variable (Rv) diatur pada posisi minimum, maka kerugian tegangan pada Rv besar dibandingkan dengan pada *gate*. sekarang jika Rv diatur pada posisi maksimum maka tegangan pada *gate* akan bertambah besar. Apabila tegangan *trigger* diperbesar maka pada saat tegangan tertentu triac akan menghantar sehingga ada arus melalui beban. Oleh karena itu pada beban terdapat daya. Bentuk gelombang yang terdapat pada beban seperti pada gambar 2.15.



GAMBAR 2.15. *Bentuk Gelombang Pada Beban Rangkaian Dasar Kontrol*

Dari gambar 2.15 dapat dilihat bahwa tegangan yang terdapat pada beban tidak gelombang penuh, tetapi dikurangi tegangan pada triac itu sendiri.

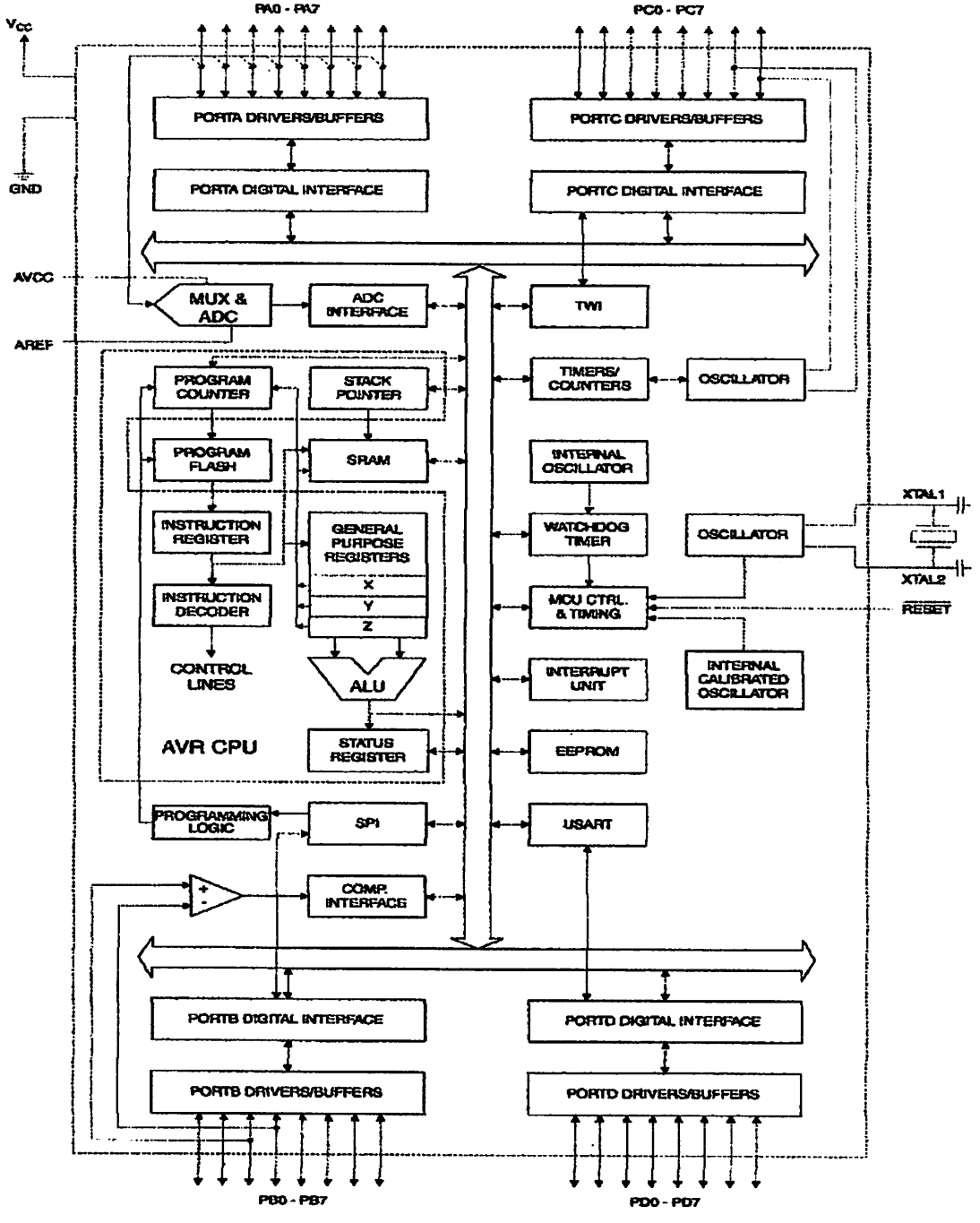
2.6. Mikrokontroler ATMEGA 8535

Secara sederhana mikrokontroler merupakan suatu IC yang didalamnya berisi CPU, ROM, RAM dan port I/O yang merupakan kelengkapan sebagai sistem minimum mikrokomputer sehingga sebuah mikrokontroler dapat dikatakan sebagai mikrokomputer dalam kepingan tunggal (*single chip microcomputer*) yang dapat berdiri sendiri.

Mikrokontroler ATMEGA 8535 merupakan mikrokontroler buatan ATMEL *Inc* yang merupakan mikrokontroler tipe terbaru buatan ATMEL dan memiliki beberapa kelebihan dari pada yang lainnya. Fitur-fitur yang ada pada ATMEGA 8535 antara lain :

- 8 bit CPU (Cental Proccessing Unit).
- 8 Kbyte self-programming flash program memory.
- *SRAM* berukuran 512 *bytes.*
- *EEPROM* berkapasitas 512 *bytes.*
- Memiliki 32 pin *I/O.*
- Memiliki 8 channel ADC 10 bit.
- Eksternal dan Internal sumber interrupt.
- Programming lock for software security.
- Tegangan operasi 2.7 – 5.5 Volt.
- Programmable serial USART.

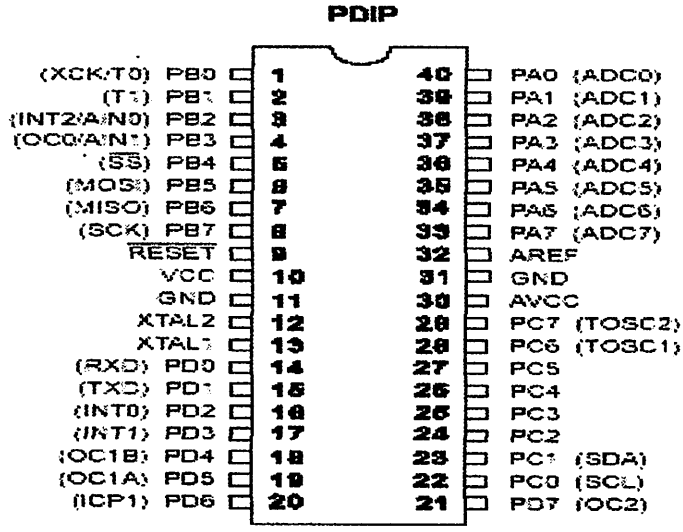
Arsitektur dasar dari mikrokontrller ATMEGA 8535 dapat dilihat pada gambar 2.16 :



Gambar 2.16. Blok Diagram ATMEGA 8535 [1]

2.6.1. Konfigurasi pin ATMEGA 8535

Berikut ini adalah bentuk fisik dan susunan pin – pin dari ATMEGA8535 yang dapat dilihat pada gambar 2.17 :



Gambar 2.17. Konfigurasi pin ATMEGA 8535 [1]

Adapun fungsi dari tiap – tiap pin pada ATMEGA 8535 berdasarkan gambar diatas adalah sebagai berikut :

1. VCC

   Pin – pin ini merupakan pin catu daya dengan level tegangan + 2.7 – 5.5 Volt DC untuk VCC.

2. GND

   Merupakan ground.

3. Port A (PA7 – PA0)

   Port A merupakan input analog untuk ADC, jika ADC tidak digunakan maka port A dapat berfungsi sebagai port I/O dua jalur. Port A merupakan

port I/O 8 bit yang dapat menyediakan *internal pull up resistors* dan *buffer* pada outputnya mempunyai *symmetrical drive characteristics.*

Jika PA_0 - PA_7 digunakan sebagai input dan *internal pull up resistors* dalam keadaan aktif maka *external pull low* port ini akan mengalirkan arus.

Selain fungsi diatas, port B juga mempunyai fungsi khusus yang lain seperti Tabel 2-2 :

Tabel 2-2. Fungsi Alternatif dari Pin Port A

Pin	Fungsi Alternatif
PA7	ADC7 (ADC Input Channel 7)
PA6	ADC6 (ADC Input Channel 6)
PA5	ADC5 (ADC Input Channel 5)
PA4	ADC4 (ADC Input Channel 4)
PA3	ADC3 (ADC Input Channel 3)
PA2	ADC2 (ADC Input Channel 2)
PA1	ADC1 (ADC Input Channel 1)
PA0	ADC0 (ADC Input Channel 0)

4. Port B (PB7 – PB0)

Port B merupakan *bi-directional* port I/O 8 bit dengan *internal pull up resistors, buffer* pada output port ini juga memiliki *symmetrical drive characteristics.* Jika digunakan sebagai input dan jika resistor *pull up* dalam keadaan aktif, maka *external pull low* akan mengalirkan arus.

Selain fungsi diatas, port B juga mempunyai fungsi khusus yang lain seperti Tabel 2-3 :

Tabel 2-3. Fungsi Alternatif dari pin port B

Pin	Fungsi Alternatif
PB7	SCK (SPI Bus Serial Clock)
PB6	MISO (SPI Bus Master Input / Slave Output)
PB5	MOSI (SPI Bus Master Output / Slave Input)
PB4	SS (SPI Slave Select Input)
PB3	AIN1 (Analog Comparator Negative Input)
	OC0 (Time/Counter 0 Output Compare Match Output)
PB2	AIN0 (Analog Comparator Positive Input)
	INT1 (External Interrupt 2 Input)
PB1	T1 (Timer / Counter 1 External Counter Input)
	T0 (Timer / Counter 0 External Counter Input)
PB0	XCK (USART External Clock Input / Output)

5. Port C (PC7 – PC0)

   Port C merupakan port I/O 8 bit dengan *internal pull up resistor*. *buffer* pada output port ini juga memiliki *symmetrical drive characteristics*. Jika digunakan sebagai input, maka *external pull low* akan mengalirkan arus jika resistor *pull up* dalam keadaan aktif.

6. Port D (PD7 – PD0)

   Port D merupakan port I/O 8 bit dengan *internal pull up resistor*. *buffer* pada output port ini juga memiliki *symmetrical drive characteristics*. Jika

digunakan sebagai input, maka *external pull low* akan mengalirkan arus jika resistor *pull up* dalam keadaan aktif.

Selain fungsi diatas, port B juga mempunyai fungsi khusus yang lain seperti Tabel 2-4 :

Tabel 2-4. Fungsi Khusus Dari Port D

Pin	Alternative Function
PD7	OC2 (Timer/Counter2 Output Compare Match Output)
PD6	ICP1 (Timer/Counter1 Input Capture pin)
PD5	OC1A (Timer/Counter1 Output Compare A Match Output)
PD4	OC1B (Timer/Counter1 Output Compare B Match Output)
PD3	INT1 (External Interrupt 1 Input)
PD2	INT0 (External Interrupt 0 Input)
PD1	TXD (USART Output Pin)
PD0	RXD (USART Input Pin)

7. RESET

   Pin ini adalah untuk input RESET,

8. XTAL1

   Merupakan input untuk oscillator *inverting amplifier* dan input untuk *clock* internal pada operasi rangkaian.

9. XTAL2

   Output dari oscillator *inverting amplifier.*

10. AVCC

    Merupakan pin tegangan untuk port A dan ADC. Tegangan ini harus berbeda dengan tegangan VCC, jika ADC tidak digunakan. Dan jika ADC digunakan maka tegangan ini harus disambunga dengan tegangan VCC melalui sebuah *low-pass filter.*

11. AREF

    Merupakan pin referensi untuk ADC

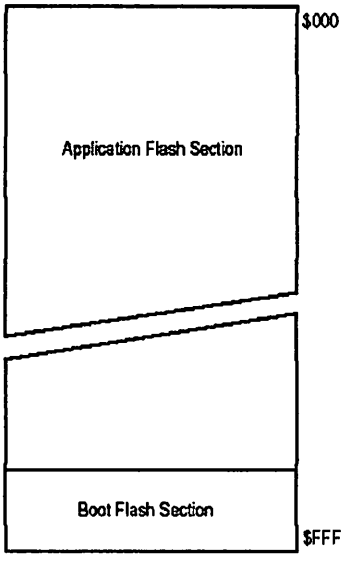
2.6.2. Organisasi Memori

Organisasi memori pada mikrokontroler ATMEGA 8535 dibagi menjadi dua bagian utama yaitu memori program *(Flash Memori)* dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpangan data maupun program. Mikrokontroler ATMEGA 8535 telah dilengkapi dengan EEPROM yang digunakan sebagai media penyimpanan data.

Berikut ini adalah penjelasan memori pada mikrokontroler ATMEGA 8535 :

- Flash Memory

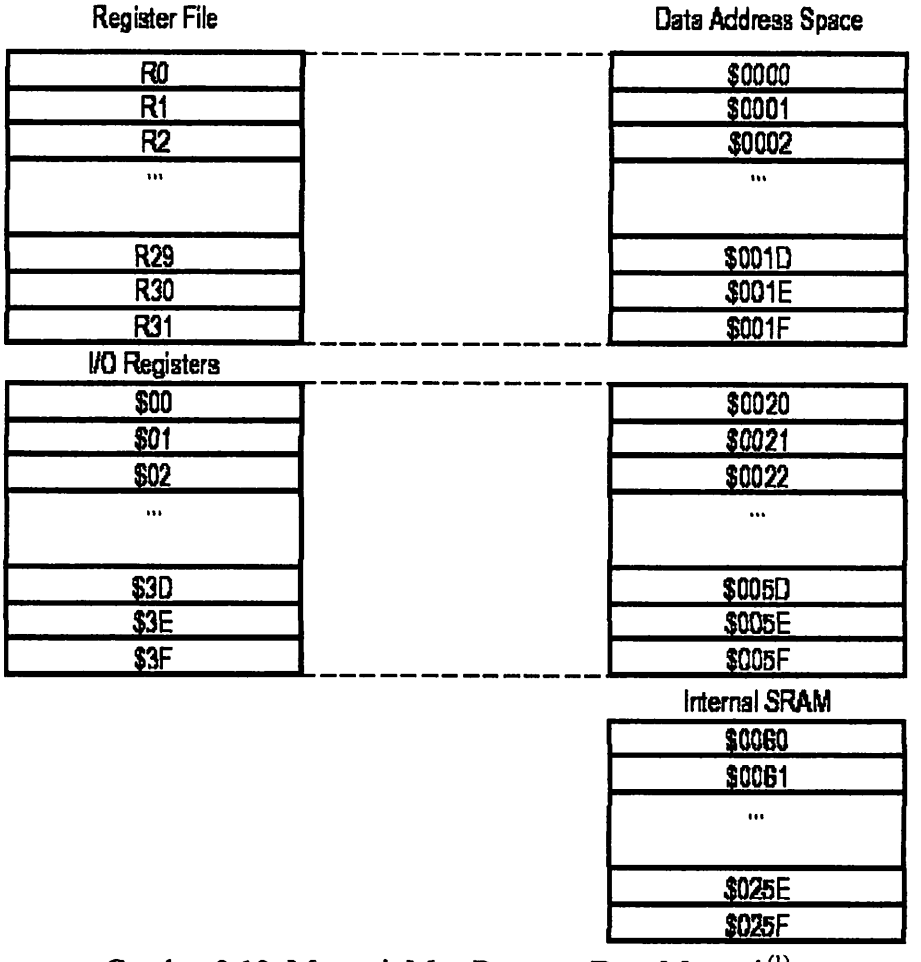
  Mikrokontroler ATMEGA 8535 memiliki 8Kb *System Reprogrammable Flash Memory* untuk penyimpanan data, selama semua instruksi pada MCU ini menggunakan data 16 atau 32 bit maka *Flash Memory* terorganisasi atas 4K x 16. Untuk pengamanan program, *Flash Memory* ini terbagi menjadi 2 bagian yaitu *Boot Program* dan *Application Program.* Gambar 2.18 menunjukkan Map Memori Program Flash Memori



Gambar 2.18. Map Memori Program Flash Memori [1]

❖ Data Memory

Terdapat 608 lokasi data memori yang dialamatkan pada *register file, I/O memory* dan *internal data SRAM*, 96 lokasi memori tersebut terletak pada *register file* dan *I/O memory* sedangkan sisanya terdapat pada *internal data SRAM.* Gambar 2.19 menunjukkan Memori Map Program Data Memori.



Gambar 2.19. Memori Map Program Data Memori [1]

2.6.3. Sistem Reset

Mikrokontroler ATMEGA 8535 mempunyai empat sumber reset baik internal maupun eksternal, berikut ini adalah sumber reset dari ATMEGA 8535 :

1. Eksternal Reset

MCU dalam kondisi reset apabila pin *reset* pada pin 9 diberikan sebuah input berupa pulsa low dalam waktu lama.

2. Power-On Reset

   MCU akan mereset jika tegangan power supply menurun atau berada dibawah tegangan power-on reset.

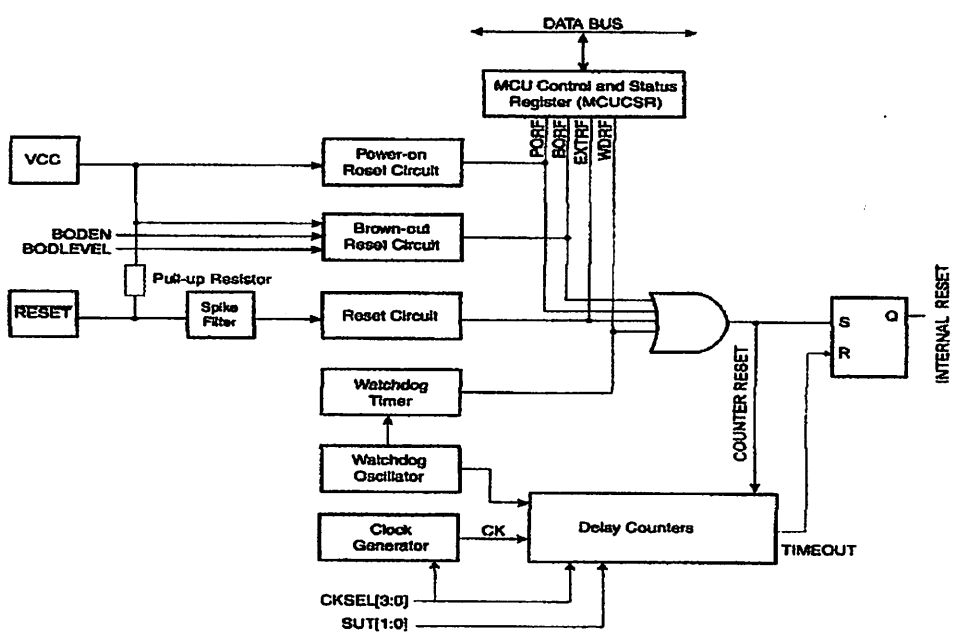
3. Watchdog Reset

   MCU akan mereset apabila watchdog timer dalam kondisi enable dan periodenya telah habis.

4. Brown-Out Reset

   MCU akan mereset apabila tegangan power supply Vcc berada dibawah atau mendekati tegangan brown-out reset dan ketika detector brown-out dalam keadaan enable.

Gambar 2.20 menunjukan logika pe-reset-an mikrokontroler ATMEGA 8535 :



Gamabar 2.20. Logika Reset Mikrokontroler ATMEGA 8535 [1]

BAB III

PERANCANGAN DAN PEMBUATAN ALAT

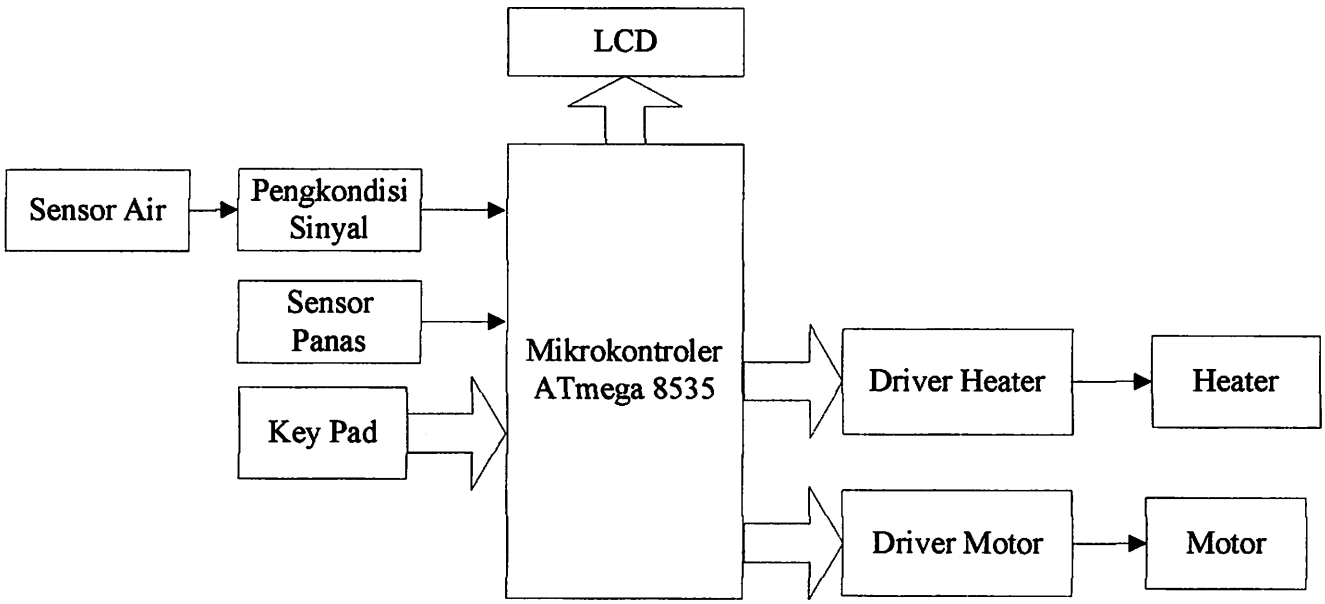
3.1. Pendahuluan

Pada bab ini akan dibahas tentang perencanaan dan pembuatan alat penurun kadar air pada madu dengan metode penangas air beserta *flowchart dan software*.

Alat ini dibuat bertujuan untuk dapat menurunkan kadar air yang ada di dalam madu, terlebih dahulu madu tersebut diukur kadar airnya dengan menggunakan sensor kadar air kemudian data tersebut diolah oleh mikrokontroler dan hasilnya ditampilkan melalui display, lalu pemrosesan penurunan kadar air dengan menggunakan heater dimana pemanasannya tidak boleh melebihi 65°C sesuai ketetapan SNI, agar pemanasannya merata digunakan motor untuk mengaduk madu tersebut.

3.1.1. Blok Diagram Keseluruhan Sistem

Perancangan dan pembuatan alat ditunjukkan dengan gambar blok diagram pada gambar 3-1 :



Gambar 3.1 Diagram Blok Keseluruhan Sistem

Keterangan fungsi dari masing-masing blok diagram diatas sebagai berikut :

1. Sensor Suhu :

   Berfungsi untuk mendeteksi suhu madu yang diproses.

2. Pengkondisi Sinyal :

   Berfungsi untuk menyesuaikan antara tegangan keluaran pada sensor suhu dengan tegangan masukan ADC.

3. Sensor Kadar Air :

   Berfungsi untuk mengukur kadar air yang ada pada madu.

4. MCU :

   Mikrontroler keluarga AVR ini berfungsi sebagai pengontrol atau pengendali semua sistem yang ada.

5. LCD :

   Berfungsi sebagai penampil data yang telah diproses oleh MCU.

6. Driver Heater :

Berfungsi menghidupkan dan mematikan heater.

7. Heater :

Berfungsi untuk menghasilkan panas yang digunakan untuk memanaskan air yang ada dalam madu.

8. Driver Motor :

Berfungsi untuk menghidupkan dan mematikan motor.

9. Motor :

Berfungsi sebagai pengaduk madu saat proses pemanasan, dimaksudkan agar proses pemanasan dapat merata.

10. KeyPad

Berfungsi sebagai inputan kadar air dalam bentuk % untuk memproses lebih lanjut.

3.2. Prinsip kerja alat

Inisialisasi port pada MCU dan madu sudah di tuang ke wadah. Memulai pengambilan data kadar air dengan cara motor mengaduk madu agar air yang terdapat pada madu menajadi rata dan sensor kadar air aktif. Data yang diambil oleh sensor kadar air diolah oleh MCU dan terus ditampilkan oleh LCD dalam satuan %. Lalu memasukan data dalam satuan % untuk proses penurunan kadar air melalui keypad.

Mulailah penurunan kadar air dengan cara Heater aktif, motor mengaduk madu agar pemanasan merata (pemanasan tidak melebihi 65°C) dan sensor kadar

air aktif selama penurunan kadar air, agar selama proses penurunan kadar air pada madu sesuai yang diinginkan, hasilnya akan ditampilkan ke LCD.

Lalu motor dan sensor kadar air aktif kembali untuk mendeteksi kadar air yang baru pada madu dan kadar air pada madu yang terbaru ditampilkan ke LCD begitu pula pertanyaan (apakah masih perlu penurunan kembali kadar air?)

Jika ya maka kembali lagi memasukkan data penurunan kadar air seperti yang diatas. Jika tidak maka selesailah proses ini.

3.3. Perancangan perangkat keras (*hardware*)

3.3.1. Sensor Kadar Air

Pada alat ini menggunakan sensor berupa dua buah logam sejenis. Logam sejenis digunakan untuk meminimalisasi adanya proses elektrokimia, dimana dengan jenis logam yang sama maka tidak ada beda potensial antar kutub sehingga tidak ada partikel yang terbawa arus listrik untuk melapisi kutub lainnya.

Sensor kadar air terbuat dari bahan terlapis logam Krom. Pemilihan jenis ini adalah karena anti karat. Selain itu juga memiliki lapisan yang licin atau halus sehingga madu juga tidak mudah menempel, sensor mudah dibersihkan.

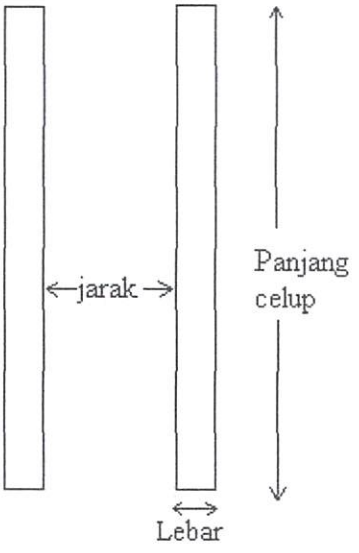
Rumus resistifitas adalah:

$$R = \rho \frac{L}{A}$$

ρ = massa jenis; L = panjang; A = luas penampang

Dengan melihat rumus, dapat disimpulkan bahwa dalam sensor kadar air, resistivitas dipengaruhi oleh luas permukaan sensor dan konduktivitas media perantara diantara sensor. Media dalam hal ini adalah madu yaitu pada kadar airnya. Karena air dalam madu memiliki resistivitas yang dominan daripada bahan lainnya. Makin lebar permukaan sensor, makin tinggi kadar airnya maka makin

rendah resistansinya, begitu juga sebaliknya. Gambar 3.2 merupakan konstruksi sensor kadar air



Gambar 3.2 Konstruksi Sensor Kadar Air.

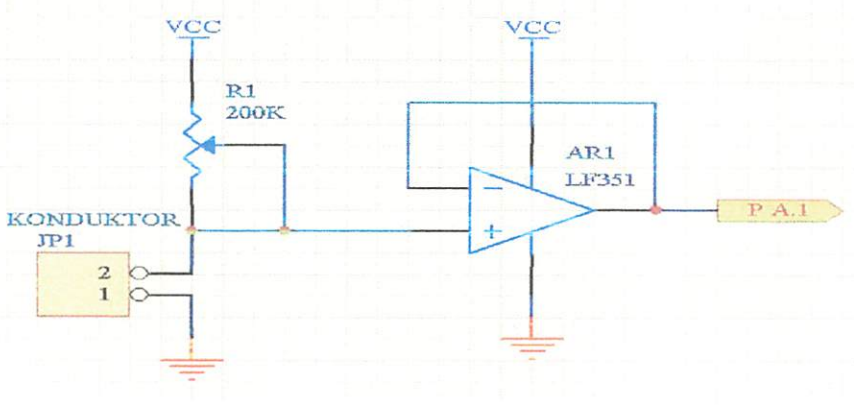
Lebar permukaan yang tercelup madu untuk setiap bilah sensor adalah :

L = Panjang x Lebar

= 15mm x 7mm

= 105 mm^2

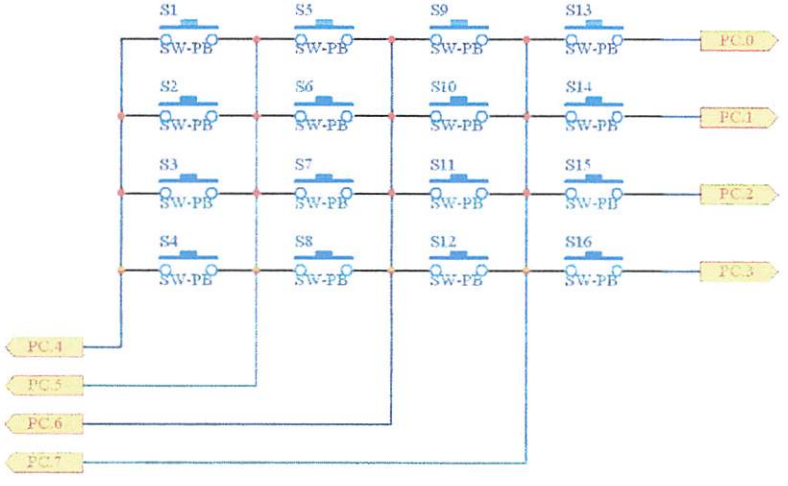
Gambar 3.3 merupakan rangkaian sensor kadar air:



Gambar 3.3 Rangkaian sensor kadar air

3.3.2. Keypad

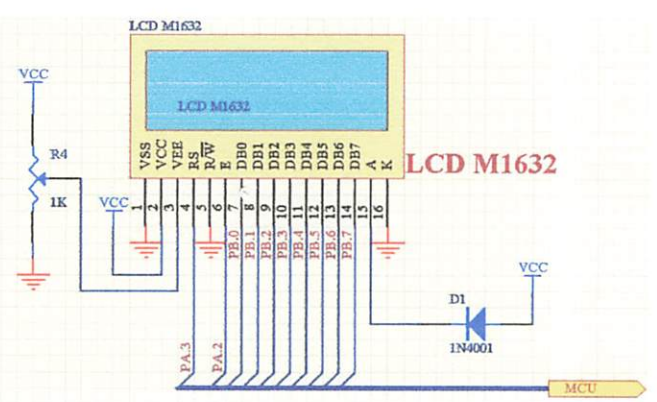
Keypad ini berfungsi untuk memberikan nilai input pada mikrokontroler yang digunakan untuk merubah dan memasukkan data nilai Kp, Ti dan Td pada program PID kontrol. Pada perancangan ini digunakan keypad 4x4 yang berarti papan tombol ini mempunyai matrik 4 baris dan 4 kolom. Deretan kolom dan baris dari keypad ini dihubungkan dengan *port* C yang difungsikan sebagai masukan dan keluaran. Deretan kolom dihubungkan dengan *ground* (berlogika 0) dan *port* C (PC4 - PC7) yang difungsikan sebagai input mkrokontroller. Sedangkan deretan baris dihubungkan ke *port* C (PC0 - PC3) yang telah diberi data 0001 dan secara kontinyu data tersebut bergeser satu bit ke kiri. Pergeseran data satu bit ini dimaksudkan untuk menentukan posisi tombol yang ditekan dalam satu kolom. Port ini difungsikan sebagai output dari mikrokontroller. Dengan demikian kalau tombol tidak ditekan maka masukan *port* C (PC4 - PC7) di pin yang terhubung tombol tersebut berlogika 0 dan bila tombol ditekan akan berlogika 1. Rangkaian papan tombol tersebut dapat terlihat pada Gambar 3.4.



Gambar 3.4 Rangkaian Keypad

3.3.3. LCD (*Liquid Crystal Display*)

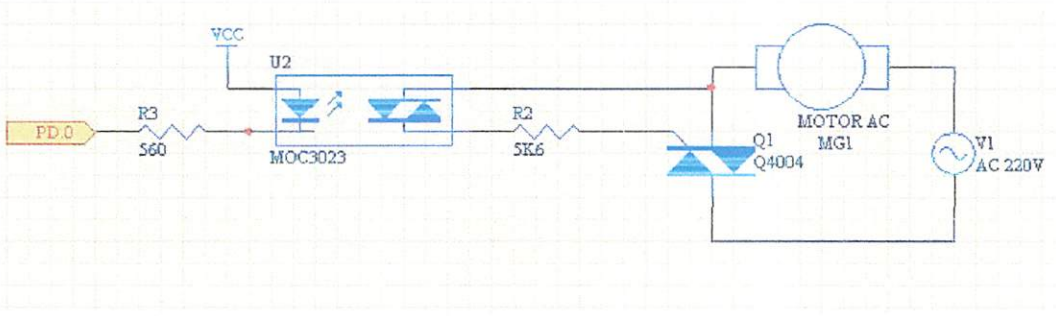
Pada perancangan ini digunakan LCD *dot matrix* 2 x 16 karakter yaitu M1632. Sinyal-sinyal yang diperlukan oleh LCD adalah RS dan *Enable*, sinyal RS dan Enable dipergunakan sebagai input yang outputnya dipakai untuk mengaktifkan LCD. LCD akan aktif apabila mikrokontroler memberikan instruksi tulis pada LCD. Saat kondisi RS *don't care* dan *Enable* 0 maka LCD tetap pada kondisi semula, pengiriman data ke LCD dilakukan saat RS berlogika 0 dan enable berlogika 1. Instruksi dikirim pada LCD bila keadaan RS 1 dan *Enable* 1. Pin LCD ini untuk data terkoneksi pada *Port* B.3 mikrokontoler ATMega 8535. Kemudian untuk RS dihubungkan pada *Port* B.0, tulis/baca (*Read/Write)* diberikan logika *low* karena disini LCD bersifat menulis data, dan yang terakhir *Enable* (E) dikendalikan dengan *Port* B.1. Gambar rangkaian LCD ditunjukkan pada gambar 3.5.



Gambar 3.5 Perancangan Rangkaian LCD (*Liquid Crystal Display*)

3.3.4. Rangkaian Driver Motor

Untuk perancangan driver heater digunakan triac karena Motor disini disupply dengan tegangan 220V AC, Gambar 3-6 menunjukkan rangkaian driver motor.



Gambar 3.6 Rangkaian Driver Motor

Tegangan output maksimum dari Mikro adalah 5 V sedangkan untuk Motor memerlukan catu daya 220V AC,maka diperlukan rangkaian driver untuk mengendalikannya. Rangkaian driver yang dipakai berupa optoisolator triac MOC3023 dan triac Q4004,untuk analisa data yang digunakan.:

Vin = 5 V (Max)

Data sheet untuk mengaktifkan MOC3023:

V_F (tegangan forward dioda) = 1,5 Volt

I_{FT} (Arus forward Trigger) = 10 mA

Maka untuk mengaktifkan optocoupler R yang dipasang :

$$R = \frac{V_{in} - V_F}{I_{FT}}$$

$$R = \frac{5v - 1{,}5v}{15mA}$$

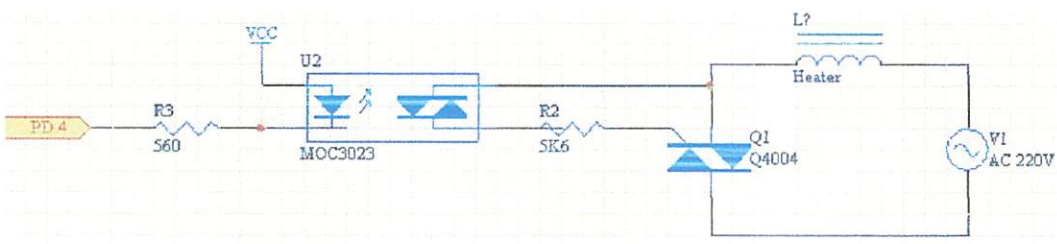
$$R = \frac{3{,}5v}{10mA}$$

$$R = 350\Omega$$

Untuk rangkaiannya menggunakan resistor 560 Ω.

3.3.5. *Rangkaian Driver Heater*

Untuk perancangan driver heater digunakan triac karena Heater disini disupply dengan tegangan 220V AC. Gambar 3-7 menunjukkan rangkaian driver heater



Gambar 3.7 Rangkaian Driver Heater

Tegangan output maksimum dari Mikro adalah 5 V sedangkan untuk Heater memerlukan catu daya 220V AC,maka diperlukan rangkaian driver untuk mengendalikannya. Rangkaian driver yang dipakai berupa optoisolator triac MOC3023 dan triac Q4004,untuk analisa data yang digunakan.:

Vin = 5 V (Max)

Data sheet untuk mengaktifkan MOC3023:

V_F (tegangan forward dioda) = 1,5 Volt

I_{FT} (Arus forward Trigger) = 10 mA

Maka untuk mengaktifkan optocoupler R yang dipasang :

$$R = \frac{V_{in} - V_F}{I_{FT}}$$

$$R = \frac{5v - 1{,}5v}{15mA}$$

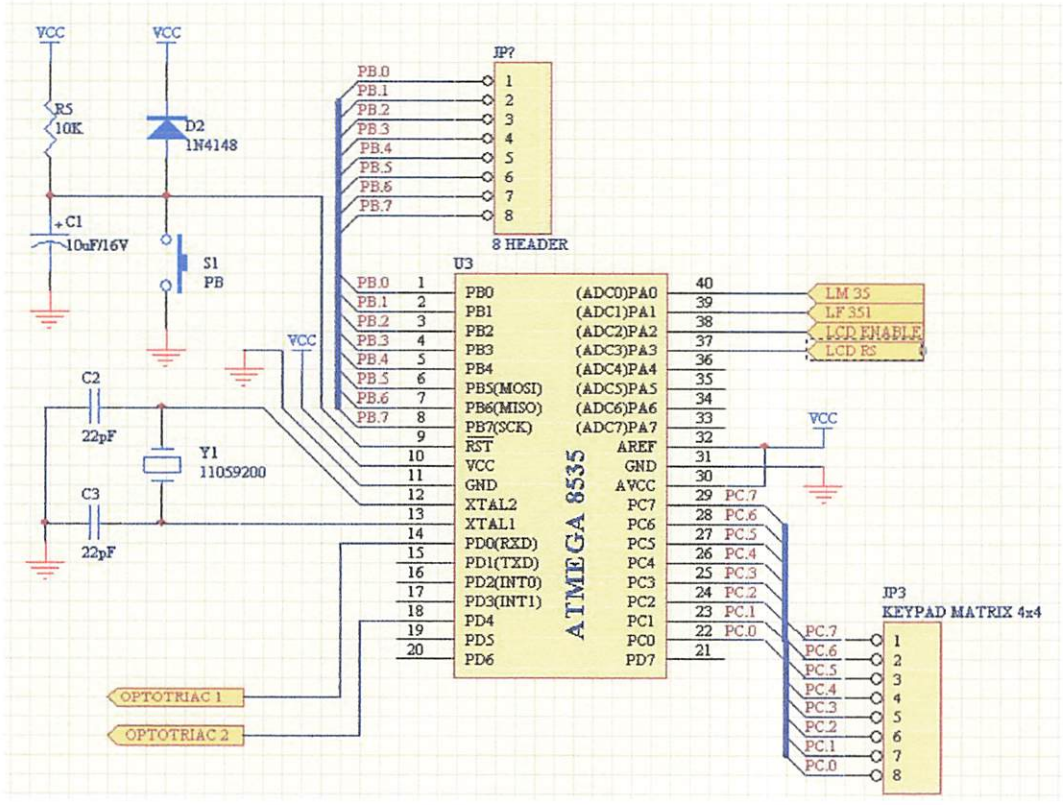
$$R = \frac{3{,}5v}{10mA}$$

$R = 350\Omega$

Untuk rangkaiannya menggunakan resistor 560 Ω.

3.3.6. Perancangan minimum sistem Atmega8535

Mikrokontroler yang digunakan adalah mikrokontroler keluarga AVR ATMega 8535 yang mempunyai arsitektur *RISC(Reduce Instruction Set)*. ATMega 8535 mempunyai 4 *channels* PWM, 8 *channels* ADC 10-bit, dan juga ATMega 8535 mempunyai kemampuan PWT (*Programmable Watchdog Timer*) dengan osilator yang terpisah, sehingga memungkinkan untuk mengaplikasikannya sebagai MCU yang cukup handal. Selain itu dengan adanya fitur-fitur tersebut, system hardware juga makin simpel karena tidak perlu lagi membuat rangkaian ADC dan PWM sehingga biaya pembuatan juga dapat lebih ekonomis. Gambar berikut menunjukkan rangkaian minimum sistem Atmega8535



Gambar 3.8 Rangkaian minimum system ATMega 8535

Alokasi penggunaan pin mikrokontroler :

- PA.0 digunakan sebagai *port* input data analog dari *Sensor Suhu* dan PA.1 digunakan sebagai *port* input data analog dari *Sensor Kadar Air*. *Port* A merupakan *port* khusus yang didalamnya memiliki ADC sehingga data analog dari *Sensor Suhu* dan *Sensor Kadar Air* diubah oleh ADC di *port* A menjadi data digital.

- PB.1 terhubung dengan kaki *Enable* (E) pada LCD dan PB.0 terhubung dengan kaki RS pada LCD.

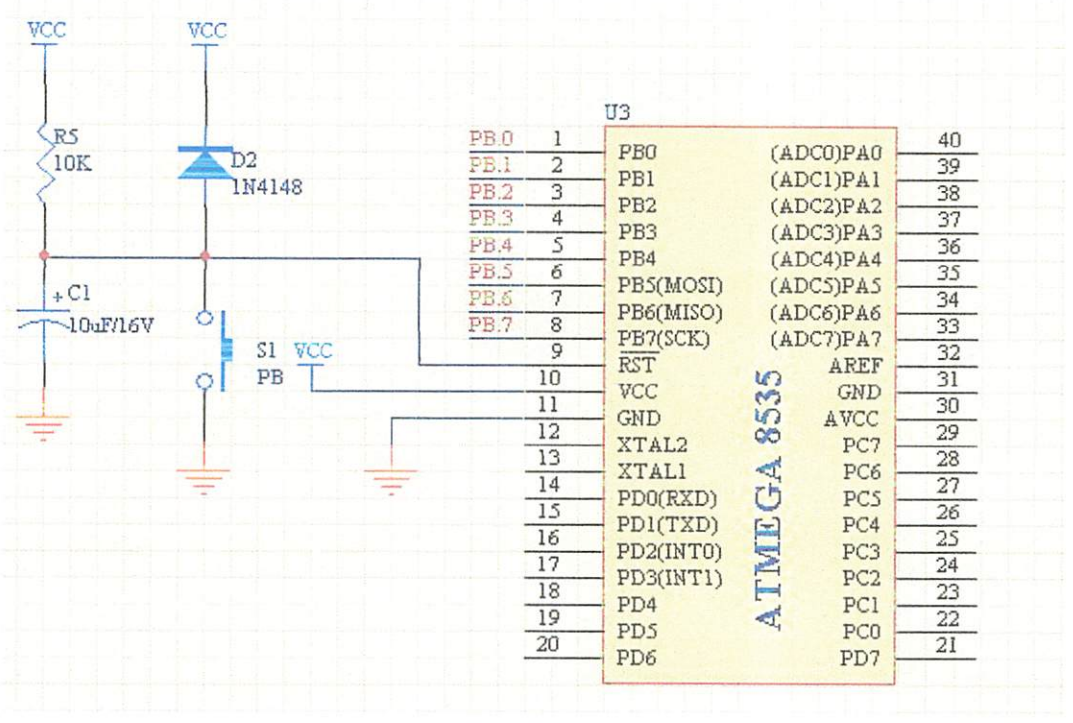
- *Port* B.3 digunakan sebagai *port* input dan output data LCD serial.

- *Port* C (PC.0 – PC.7) digunakan sebagai *port* input data dari *keypad.*

- PD.0 dan PD.4 digunakan untuk rangkaian driver Motor dan Heater

- PD.2 digunakan sebagai *Zero Crossing*.
- PD.4 dan PD.7 digunakan sebagai *port* output data PWM yang terhubung dengan driver motor.

Perancangan rangkaian reset pada mikrokontroler ATMega 8535 ialah dengan memberikan logika low pada pin reset mikrokontroler ATMega 8535. Rangkaian reset ini diperoleh dari *application note AVR Design Consideration* dari ATMEL. Gambar 3-9 merupakan rancangan rangkaian reset pada ATMega 8535 :



Gambar 3.9 Rangkaian reset

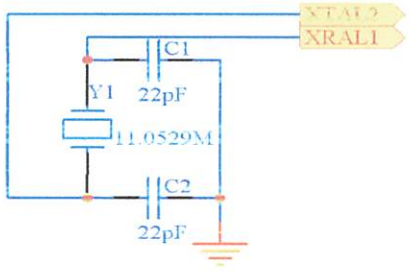
Osilator pada rangkaian minimum sistem ATMega 8535 menggunakan kristal 11,0592 MHz dan kapasitor 22 pF. Nilai kapasitor ini diperoleh dari tabel datasheet tentang penggunaan kapasitor untuk rangkaian osilator / sistem clock

pada ATMega 8535. Penggunaan kristal 11,0592 MHz ini bertujuan agar berhitungan bautrate tidak mengalami error yang disebabkan karena selisih perhitungan. Perhitungan bautrate pada ATMega 8535 dengan menggunakan kristal 11,0592 MHz :

Bautrate yang diinginkan ialah 38400 bps, maka nilai pada *UBRR(USART Baut Rate Register)* dapat ditentukan dengan perhitungan :

$$UBRR = \frac{fosc}{16.Baud} - 1$$
$$UBRR = \frac{11059200}{16.38400} - 1$$
$$UBRR = \frac{11059200}{614400} - 1$$
$$UBRR = 18 - 1 = 17 = 11H$$

Penggunaan kristal 11,0592 MHz memungkinkan hasil perhitungan *baudrate* tidak sisa dan *error* dari selisih perhitungan tidak ada. Gambar 3-10 menunjukkan rangkaian clock

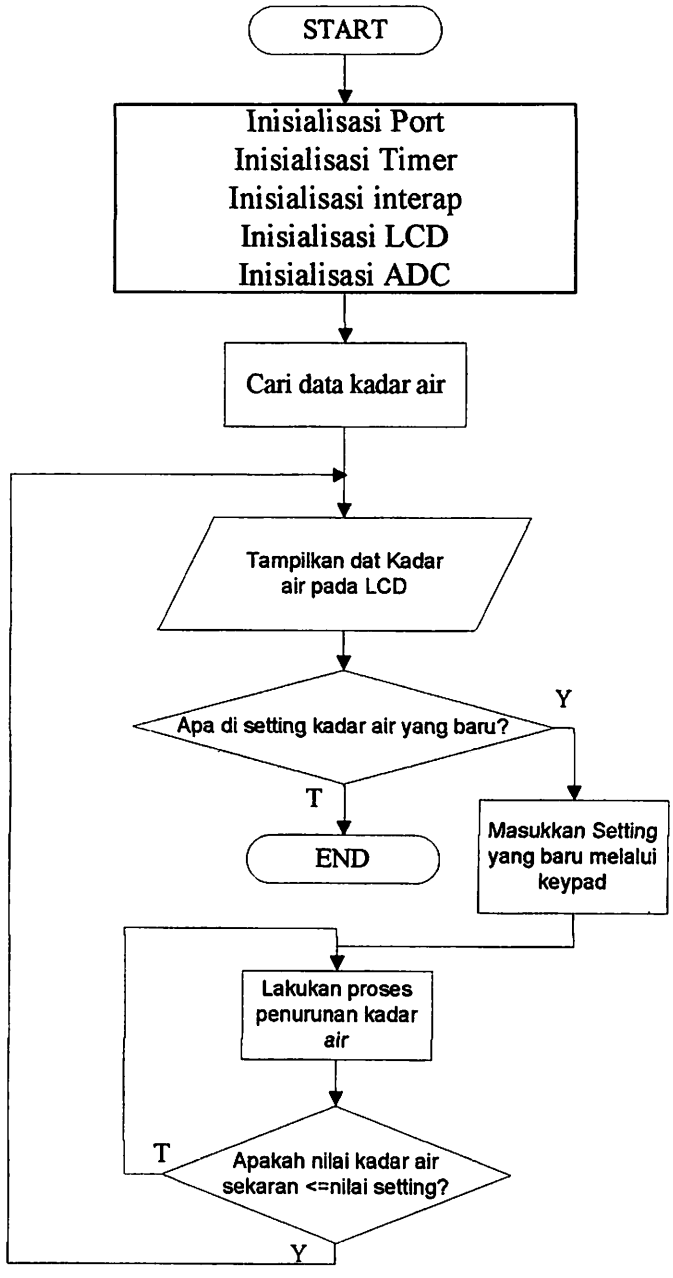


Gambar 3.10 Rangkaian clock

3.4. Perancangan perangkat lunak (*Software*)

Perancangan perangkat lunak (*software*) yang digunakan dalam perancangan sistem penurun kadar air pada madu berbasis mikrokontroller ATMega 8535 akan dipaparkan dalam *flowchart* sistem secara keseluruhan. Sistematika jalannya program yang dibuat didasarkan pada sistem *hardware* yang telah dirancang. Pembuatan *software* hanya dilakukan pada mikrokontroler menggunakan bahasa C.

3.4.1. Diagram Alir (*Flow Chart*)



Gambar 3.11 Flow chart total sistem

➢ Penjelasan *flowchart* secara keseluruhan :

1. Pertama kali *software* akan melakukan pengenalan terhadap mikrokontroller dan kristal yang digunakan, pada perancangan *software* ini menggunakan mikrokontroller ATMega 8535 dan kristal 11.0592MHz. Selanjutnya program mengkonfigurasi pin-pin LCD, jenis LCD yang dipakai, dan juga mendefinisikan karakter baru yang dipakai. Kemudian program mengkonfigurasi timer agar timer pada mikrokontroller ATMega 8535 dikenali dan dapat digunakan.
2. Pengambilan data kadar air melalui sensor kadar air yang pertama kerja ialah motor megaduk madu agar air pada madu mencampur merata dengan madu lalu sensor air mengambil data kadar air pada madu.
3. Menampilkan kadar air yang baru melalui LCD.
4. Memutuskan apakah kadar air perlu penurunan, jika tidak maka selesai prosesnya, jika ya maka memasukkan nilai dalam bentuk satuan % yang kita hendaki melalui keypad.
5. Memulai proses penurunan kadar air yang meliputi Motor dan Heater aktif dimana panasnya heater tidak boleh melebihi 65°C, setelah beberapa detik sensor air mendetksi kandungan air apakah kandungan air sesuai data yang dimasukkan, jika tidak maka proses terus berlanjut hingga ter penuhi.
6. Menampilkan data kadar air yang baru saja di proses, lalu pertanyaan kembali apakah masih perlu diturunkan lagi? Jika ya kembali ke point 4, jika tidak proses selesai.

BAB IV

PENGUJIAN DAN HASIL ANALISA

Pengujian dilakukan untuk mengetahui sejauh mana perlatan dapat bekerja sesuai dengan perencanaan.Langkah pengujian dilakukan melalui 2 tahap, yakni pengujian pada setiap blok dan pengujian pada sistem keseluruhan. Tahap pertama dimaksudkan untuk mengetahui sejauh mana blok-blok rangkaian dapat berjalan, sedangkan tahap kedua dilakukan setelah diperoleh kepastian bahwa tiap blok rangkaian telah berjalan sesuai rencana. Pada tahap ini setiap blok rangkaian diintegrasikan menjadi sebuah sistem pangendalian motor AC dan Heater yang kemudian dilakukan pengujian secara menyeluruh.

4.1. Pengujian Mikrokontroller ATMega 8535

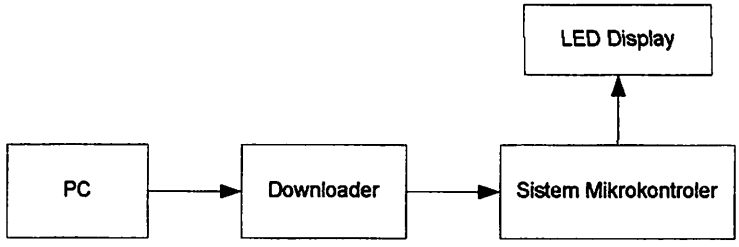
4.1.1. Tujuan

Untuk mengetahui kondisi awal dari Mikrokontroler apakah sudah sesuai yang direncanakan.

4.1.2. Peralatan yang digunakan

1. Catu daya 5V.
2. Komputer.
3. *Downloader.*
4. Minimum sistem mikrokontroler ATMega8535.

4.1.3. Prosedur pengujian



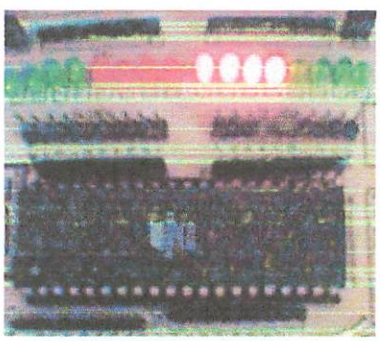
Gambar 4.1. Diagram Blok Pengujian Mikrokontroler

1. Rangkaian dibuat seperti gambar 4.1.
2. Memberikan catu daya 5 volt.
3. Membuat program yang digunakan untuk menguji mikrokontroler. Program yang digunakan dalam pengujian mikrokontroler ini merupakan program yang sederhana yang meletakkan $F0_H$ dan $0F_H$ secara bergantian pada *PortC* ATMega 8535. Program yang dibuat adalah sebagai berikut :

```
$regfile = "m16def.dat"

$crystal = 11059200

Config Portc = Output

Do

    Portc = &HF0

    Wait 3

    Portc = &H0F

    Wait 3

Loop
```

4. Mengamati keluaran pada LED Display.

4.1.4. Hasil pengujian



Gambar 4.2. Hasil pengujian tampilan LED

Tabel 4.1. Hasil Pengujian Sistem Mikrokontroler

Kondisi	Keluaran pada LED *Display*							
	Bit 0	*Bit 1*	*Bit 2*	*Bit 3*	*Bit 4*	*Bit 5*	*Bit 6*	*Bit 7*
Satu	0	0	0	0	1	1	1	1
Dua	1	1	1	1	0	0	0	0

Keterangan :

- Kondisi bit *low* (0) = LED menyala
- Kondisi bit *height* (1) = LED mati

Dari hasil pengujian pada tabel 4–1 dapat dilihat bahwa *port C* memberikan logika $0F_H$ dan $F0_H$ secara bergantian sesuai dengan isi program.

4. 2. Pengujian sensor kadar air

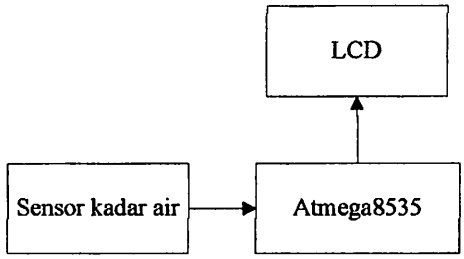
4.2.1. Tujuan

Untuk mengetahui apakah sensor dapat bekerja sesuai dengan rancangan.

4.2.2. Peralatan yang digunakan

1. Sensor kadar air.
2. *Rangkaian Atmega8535.*
3. LCD untuk tampilan.

4.2.3. Prosedur pengujian



Gambar 4.3. Diagram blok pengujian Sensor kadar air

1. Memberi catu daya 5V.

Melihat data keluaran *Sensor kadar air* yang di tampilkan oleh *LCD.*

4.2.4. Hasil pengujian

Sensor kadar air merupakan dua batang konduktor yang dirancang untuk mengambil reisistansi pada madu. Berdasarkan data yang diperoleh dari uji coba alat didapat

Table 4.2. data *ADC* yang ditampilkan *LCD.*

Kadar air %	Keluaran ADC
24 %	243
23 %	245
22 %	247
21 %	248-249
20 %	250
19 %	252-253

4. 3. Pengujian sensor Suhu

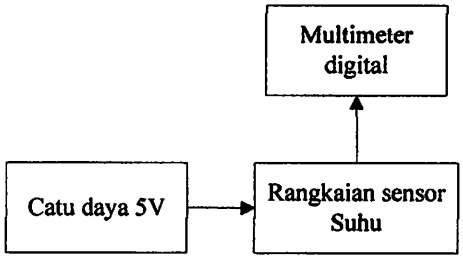
4.3.1. Tujuan

Untuk mengetahui apakah sensor dapat bekerja sesuai dengan rancangan.

4.3.2. Peralatan yang digunakan

1. Catu daya 5V.
2. Rangkaian sensor Suhu.
3. Multimeter digital.

4.3.3. Prosedur pengujian



Gambar 4.4. Diagram blok pengujian Sensor suhu

2. Memberi catu daya 5V.
3. Mengukur tegangan keluaran *Sensor suhu* dengan *AVO meter* apabila suhu dinaikkan atau di turunkan.

4.3.4. Hasil pengujian

Hasil pengujian sensor suhu ditunjukkan dalam Tabel 4.2. Dari data tersebut diperlihatkan hubungan nilai suhu, tegangan keluaran berdasarkan pengukuran, tegangan keluaran berdasarkan perhitungan, dan besar penyimpangan data pengukuran terhadap perhitungan

Table 4.3. Hasil pengujian tegangan *output.*

No	Suhu (°C)	Tegangan keluaran pengukuran (mvolt)	Tegangan keluaran perhitungan (mvolt)	Penyimpangan (%)
1	43	428	430	0,46
2	44	436	440	0,91
3	45	452	450	0,35
4	46	458	460	0,43
5	47	471	470	0,21
6	48	483	480	0,62
Penyimpangan rata-rata				0,49

Keterangan:

Dalam Tabel 4.2 bisa dilihat bahwa tegangan keluaran sensor suhu terhadap perubahan suhu adalah linier dan sesuai dengan spesifikasi sensor suhu tersebut. Persentase kesalahan dari hasil pengujian terhadap nilai yang diinginkan dalam perancangan bisa dihitung dengan:

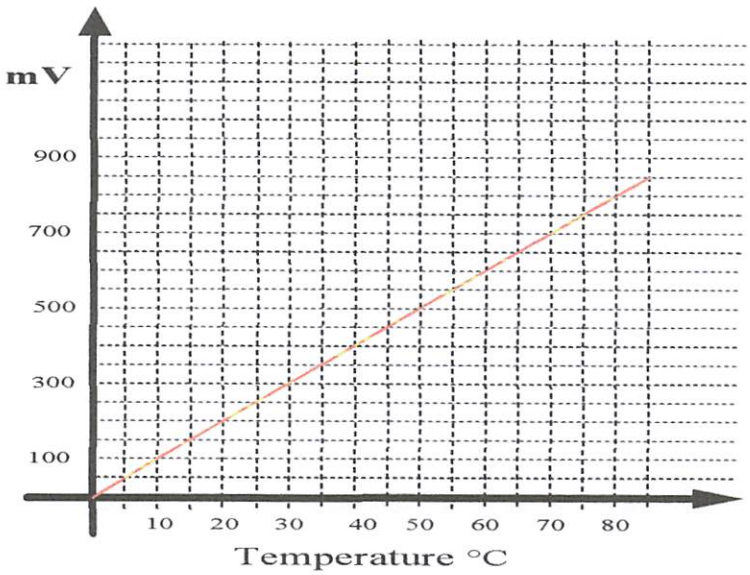
$$\text{Prosentase penyimpangan} = \frac{|V_o \text{ perhitungan} - V_o \text{ pengukuran}|}{V_0 \text{ perhitungan}} \times 100\%$$

$$\text{Penyimpangan rata-rata} = \frac{X}{Y}$$

$$= Z\%$$

Adanya penyimpangan dikarenakan:

- Pembacaan yang tidak tepat pada termometer
- Tidak presisinya multimeter sehingga menyebabkan kesalahan dalam pembacaan



Gambar 4-5. Grafik perbandingan tegangan out Lm35 dengan tempertur

4.4. Pengujian LCD

4.4.1. Tujuan

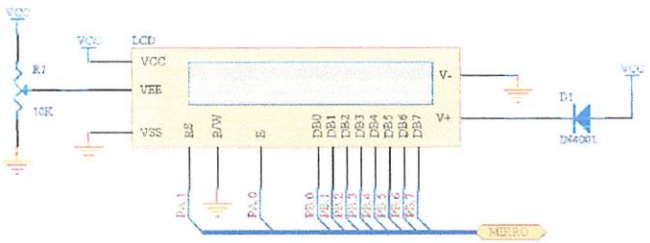
Untuk mengetahui apakah LCD dapat bekerja sesuai dengan rancangan.

4.4.2. Peralatan yang digunakan

1. Catu daya 5V.

2. Minimum sistem mikrokontroler dan LCD (*Liquid Crystal Display*).

4.4.3. *Prosedur pengujian*



Gambar 4.6. Rangkaian LCD (*Liquid Crystal Display*)

1. Rangkaian dibuat seperti gambar 4.3.

2. Memberi catu daya 5V.

3. Membuat program yang digunakan untuk menguji LCD. Program yang digunakan dalam pengujian LCD merupakan program yang sederhana yaitu menuliskan nama pada baris pertama dan menuliskan NIM pada baris ke dua. Program yang dibuat adalah sebagai berikut:

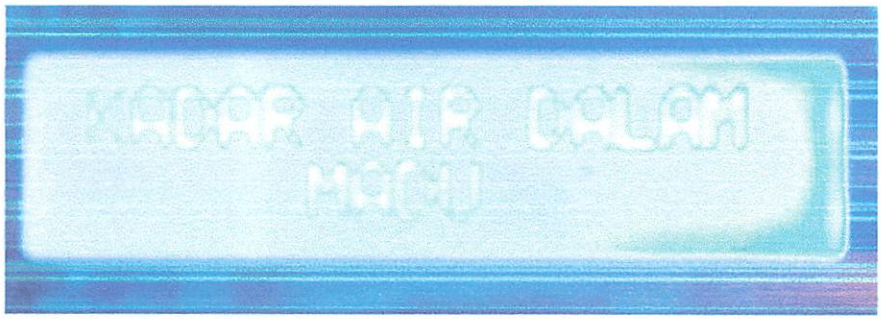
```
$regfile = "m16def.dat"

$crystal = 8000000
```

```
Dim A As Byte
Config Lcdpin = Pin , Db4 = Portb.4 , Db5 = Portb.5 , Db6 = Portb.6 ,
Db7 = Portb.7 , E = Porta.0 , Rs = Porta.1
Config Lcd = 16 * 2
Cursor Off
Cls
Do
   Locate 1 , 1 : Lcd "      Kadar Air Dalam      "
   Locate 2 , 1 : Lcd "     Madu    "
   Wait 2
   Cls
   Wait 3
Loop
```

4. Mengamati keluaran pada LCD.

4.4.4. Hasil pengujian

Setelah data diolah mikrokontroler maka hasil tampilan LCD berupa tulisan pada baris pertama "Kadar Air Dalam" dan baris ke dua "Madu".



Gambar 4.7. Tampilan hasil pengujian LCD

4.5. Pengujian driver motor AC

4.5.1. Tujuan

Untuk mengetahui apakah rangkaian ini dapat bekerja sebagaimana mestinya, yaitu dapat menggerakkan motor.

4.5.2. Peralatan yang digunakan

1. Catu daya Tegangan jala-jala.
2. Rangkaian driver motor.
3. Multimeter digital.

4.5.3. Prosedur pengujian

Gambar 4.8. Diagram blok pengujian driver motor

1. Rangkaian dibuat seperti gambar 4.8.
2. Memberi catu daya Tegangan jala-jala.
3. memberi logika pada inputan driver dan mengamati arah putaran motor AC pada keluarannya.

4.5.4. Hasil pengujian

Table 4.4. Hasil pengujian rangkaian driver motor

No.	*INPUT*	*OUTPUT* *Tegangan jala-jala = 205 volt*
1.	0	173
2.	1	0

Keterangan :

- Kondisi bit *low* (0) = Motor hidup
- Kondisi bit *height* (1) = Motor mati

4.6. Pengujian driver Heater

4.6.1. Tujuan

Untuk mengetahui apakah rangkaian ini dapat bekerja sebagaimana mestinya, yaitu dapat menghidupkan Heater sesuai yang di inginkan.

4.6.2. Peralatan yang digunakan

1. Catu daya Tegangan jala-jala.
2. Rangkaian driver Heater.
3. Multimeter digital.

4.6.3. Prosedur pengujian

Gambar 4.9. Diagram blok pengujian driver Heater

1. Rangkaian dibuat seperti gambar 4.8.

2. *Memberi Catu daya Tegangan jala-jala.*

3. memberi logika pada inputan driver dan mengamati hidup matinya Heater.

4.6.4. Hasil pengujian

Table 4.5. Hasil pengujian rangkaian driver Heater

No.	*INPUT*	*OUTPUT* *Tegangan jala-jala = 205 volt*
1.	0	173
2.	1	0

Keterangan :

- Kondisi bit *low* (0) = Heater hidup
- Kondisi bit *height* (1) = Heater mati

BAB V

PENUTUP

5.1. Kesimpulan

Dari rangkaian kegiatan perencanaan sampai dengan pengujian keseluruhan system yang telah dibuat maka dapat diambil beberapa kesimpulan sebagai berikut :

1. Berikut ini data kadar air yang di tampilkan *LCD* melalui uji kalibrasi.

Kadar air %	Keluaran ADC
24 %	243
23 %	245
22 %	247
21 %	248-249
20 %	250
19 %	252-253

   Hasil pengkalibrasian kurang dapat dipertanggung jawabkan, karena hasil ini merupakan pengujian alat yang di cocokan terhadap sempel kondisi saat itu.

2. Untuk pemanas, suhunya di buat stabil dengan cara mencacah frekwensi dari tegangan 220V melalui zero crossing.
3. Hasil kalibrasi belum mengacu pada hasil analisa dari lab. Kimia fakultas Mipa Unversitas brawijaya.
4. Persamaan untuk nilai resistansi terhadap jarak kedua elektroda tersebut belum dapat dituliskan dengan pasti sehingga mempengaruhi hasil.

5.2. Saran - saran

Ada beberapa saran yang dapat kami berikan kapada pembaca yang tertarik dengan skripsi ini bahkan ingin mengembangkannya.

- Pada pengambilan data kadar air diperlukan lebih dari 1 kali untuk mencapai data yang valid.
- Panas sangat berpengaruh pada Resistansi maka di perlukan suhu yang stabil untuk pengambilan data resistansi air.

DAFTAR PUSTAKA

[1]. *Frans Gunterus, Falsafah Dasar : Sistem Pengendalian Proses.*

[2]. *http://puslit.petra.ac.id/journals/electrical/pid.pdf*

[3]. *http://www.innovativeelectronics.com/innovative_electronics/download_files/artikel/AN27.pdf*

[4]. *http://elektronika-elektronika.blogspot.com*

[5]. *Lingga Warhana, Belajar Sendiri Mikrokontroler AVR Seri ATMega8535 Simulasi, Hardware, dan Aplikasi.*

[6]. *www.atmel.com , data sheet ATMega8535*

[7]. *www.parallax.com , LCD M1632*

LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika / T.Infokom, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : M Yusuf
NIM : 04 12230
Perbaikan meliputi : 8

*> Rumus nilai Resistansi ~~di~~ terhadap jarak ~~dan~~ antara 2 Konduktor terhadap kadar air dlm wadah ?

*> Perbaiki Gbr ? skematik yg tdk benar 1.

Malang, 17 - 3. 2009

(_____)

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika / T.Infokom, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : M Yusuf
NIM : 2412230
Perbaikan meliputi :

1) TEORI SNI

Malang, 200

( )

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama	:	Muhammad Yusuf
NIM	:	04.12.230
Jurusan	:	Teknik Elektro S-1
Konsentrasi	:	Teknik Elektronika
Judul	:	Alat Penurun Kadar Air Dalam Madu Dengan Metode Pemanas Air
Hari / Tanggal Ujian Skripsi	:	Selasa / 17 Maret 2009

No	Materi Perbaikan	Paraf
1	Hasil Pengujian yang di keluarkan Sensor kadar air melalui Pengkalibrasian	
2	Perbaiki Gambar sekematik yang tidak benar	

Disetujui,

Penguji I

(Sotyohadi, ST, MSc)
NIP.Y.1039700309

Mengetahui,

Dosen Pembimbing I

M.Ibrahim Ashari, ST, MT
Nip. 1030100358

Dosen Pembimbing II

Irmalia Suryani Faradisa,ST MT
Nip. 1030100365

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama	:	Muhammad Yusuf
NIM	:	04.12.230
Jurusan	:	Teknik Elektro S-1
Konsentrasi	:	Teknik Elektronika
Judul	:	Alat Penurun Kadar Air Dalam Madu Dengan Metode Pemanas Air
Hari / Tanggal Ujian Skripsi	:	Selasa / 17 Maret 2009

No	Materi Perbaikan	Paraf
1	SNI Madu	

Disetujui,

Penguji II

(Joseph Dedy Irawan, ST, MT.)
NIP. 132315178

Mengetahui,

Dosen Pembimbing I

M.Ibrahim Ashari, ST, MT
Nip. 1030100358

Dosen Pembimbing II

Irmalia Suryani Faradisa,ST MT
Nip. 1030100365

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura -- gura No.2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Muhammad Yusuf
Nim : 04.12.230
Masa Bimbingan : 16-January-2009 s/d 16-Juli-2009
Judul Skripsi : ALAT PENURUN KADAR AIR PADA MADU DENGAN METODE PEMANAS AIR

No	Tanggal	Uraian	Paraf Pembimbing
1		BAB I → rumus tambah.	
2		III → sensor air. → suhu? LM 35. GGL?	
3			
4		Gambar di lengkapi	
5			
6		Tambah kesimpulan Bab 5	
7		Revisi makalah Seminar	
8		Acc. Ujian.	
9			
10			

Malang, 14/03/03
Dosen pembimbing II

Irmalia Suryani Faradisa,ST MT
Nip. 1030100365

Form S-4a

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura – gura No.2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Muhammad Yusuf
Nim : 04.12.230
Masa Bimbingan : 16-January-2009 s/d 16-Juli-2009
Judul Skripsi : ALAT PENURUN KADAR AIR PADA MADU DENGAN METODE PEMANAS AIR

No	Tanggal	Uraian	Paraf Pembimbing
1	15 feb 09	Revisi Bab 1, Bab 2 dan Bab III	
2	19 feb 09	acc Bab 1, 2 dan 3.	
3	21 feb 09	Revisi Bab 4 dan Bab 5	
4	24 feb 09	Revisi makalah seminar	
5	2 mar 09	acc Bab 4 dan Bab 5.	
6	3 mar 09	acc makalah Seminar	
7			
8			
9			
10			

Malang,

Dosen pembimbing I

M.Ibrahim Ashari, ST, MT
Nip. 1030100358

Form S-4a

DEPARTEMEN PENDIDIKAN NASIONAL
UNIVERSITAS BRAWIJAYA MALANG
FAKULTAS MIPA JURUSAN KIMIA
JL. VETERAN TELP. (0341) 575838 MALANG 65145

LAPORAN HASIL ANALISA

Nomor : M.03 / RT.5 / T.1 / R.0 / TT. 150803 / 2009

1.Data konsumen :

Nama konsumen	: Yusuf.
Instansi	: Fakultas Teknik Jurusan Teknik Elektro ITN Malang.
Alamat	: Jalan Candi Panggung No.40 Malang
Telepon	: -
Status	: Mahasiswa
Keperluan analisis	: Penelitian
2.Sampling dilakukan	: Oleh konsumen
3.Identifikasi sampel	
Nama sampel	: ***Madu***
Wujud	: Cair
Warna	: Kuning
Bau	: Berbau
4.Prosedur analisa	: Dari Lab. Lingkungan Jurusan Kimia FMIPA Unibraw Malang.
5.Penyampaian Laporan hasil analisis	: Diambil sendiri/langsung
6.Tanggal terima sampel	: 28 Januari 2009
7. Data hasil analisa	:

Parameter	No.	Kode	Hasil Analisa		Metode Analisis	
			Kadar	Satuan	Pereaksi	Metode
Kadar Air	1.	A	18,38 ± 0,06	%	-	Gravimetri
	2.	B	16,02 ± 0,15	%	-	Gravimetri
	3.	C	19,20 ± 0,15	%	-	Gravimetri

Catatan :

1. Hasil analisa ini adalah nilai rata – rata pengerjaan analisis secara duplo.
2. Hasil analisa ini hanya berlaku untuk sampel yang kami terima dengan kondisi sampel saat itu.

Malang, 09 Pebruari 2009
Kalab. Lingkungan,

Mengetahui :

Dr. Sasangka Prasetyawan, MS.
NIP. 131 655 134

Ir. Bambang Ismuyanto, MS.
NIP. 131 616 317

PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL MALANG

INSTITUT TEKNOLOGI NASIONAL MALANG

FAKULTAS TEKNOLOGI INDUSTRI
FAKULTAS TEKNIK SIPIL DAN PERENCANAAN
PROGRAM PASCASARJANA MAGISTER TEKNIK

T. BNI (PERSERO) MALANG
BANK NIAGA MALANG

Kampus I : Jl. Bendungan Sigura-gura No. 2 Telp. (0341) 551431 (Hunting), Fax. (0341) 553015 Malang 65145
Kampus II : Jl. Raya Karanglo, Km 2 Telp. (0341) 417636 Fax. (0341) 417634 Malang

Malang, 9 Pebruari 2009

Nomor : ITN- 699/7/TA /2009
Lampiran :
Perihal : *Bimbingan Skripsi*

Kepada : Yth. Sdr. **M. IBRAHIM ASHARI, ST, MT**
Dosen Pembimbing
Jurusan Teknik Elektro S-1
di
Malang

Dengan hormat,
Sesuai dengan permohonan dan persetujuan dalam proposal skipsi untuk mahasiswa:

Nama	: **MUHAMMAD YUSUF**
Nim	: **04 12 230**
Fakultas	: **Teknologi Industri**
Jurusan	: **Teknik Elektro S-1**
Konsentrasi	: **Teknik Elektronika**

Maka dengan ini pembimbingan tersebut kami serahkan sepenuhnya kepada Saudara/i selama masa waktu 6 (enam) bulan, terhitung mulai tanggal:

16 JANUARI 2009 S/D 16 JULI 2009

Sebagai satu syarat untuk menempuh Ujian sarjana.
Demikian atas perhatian serta kerjasama yang baik kami ucapkan terima kasih

Ketua Jurusan
Teknik Elektro S-1

Ir. F. Yudi Limpraptono, MT
NIP. Y. 1039500274

Tindasan:
1. Mahasiswa yang Bersangkutan
2. Arsip

Form S-4a

PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL MALANG

INSTITUT TEKNOLOGI NASIONAL MALANG

FAKULTAS TEKNOLOGI INDUSTRI
FAKULTAS TEKNIK SIPIL DAN PERENCANAAN
PROGRAM PASCASARJANA MAGISTER TEKNIK

T. BNI (PERSERO) MALANG
BANK NIAGA MALANG

Kampus I : Jl. Bendungan Sigura-gura No. 2 Telp. (0341) 551431 (Hunting), Fax. (0341) 553015 Malang 65145
Kampus II : Jl. Raya Karanglo, Km 2 Telp. (0341) 417636 Fax. (0341) 417634 Malang

Malang, 9 Pebruari 2009

Nomor : ITN- 700/7/TA /2009
Lampiran :
Perihal : ***Bimbingan Skripsi***

Kepada : Yth. Sdr. **IRMALIA SURYANI F, ST, MT**
Dosen Pembimbing
Jurusan Teknik Elektro S-1
di
Malang

Dengan hormat,
Sesuai dengan permohonan dan persetujuan dalam proposal skipsi untuk mahasiswa:

Nama	: **MUHAMMAD YUSUF**
Nim	: **04 12 230**
Fakultas	: **Teknologi Industri**
Jurusan	: **Teknik Elektro S-1**
Konsentrasi	: **Teknik Elektronika**

Maka dengan ini pembimbingan tersebut kami serahkan sepenuhnya kepada Saudara/i selama masa waktu 6 (enam) bulan, terhitung mulai tanggal:

16 JANUARI 2009 S/D 16 JULI 2009

Sebagai satu syarat untuk menempuh Ujian sarjana.
Demikian atas perhatian serta kerjasama yang baik kami ucapkan terima kasih

Ketua Jurusan
Teknik Elektro S-1

Ir. F. Yudi Limpraptono, MT
NIP. Y. 1039500274

Tindasan:
1. Mahasiswa yang Bersangkutan
2. Arsip

Form S-4a

```
/* File include */
#include <mega8535.h>
#include <delay.h>
#include <math.h>
#include "lcdku.c"
#include "keypad.c"
//#include "i2c.c"


/* Pendefinisian */
#define triac   PORTD.0
#define motor   PORTD.4


/* Inisialisasi variabel global */
unsigned char a,hit;
long int time;
int i,ia,b,s,suhu,kental,p,pb;
bit t,trx;
float x;
//flash int
konstanta_timing[25]={1,666,333,111,167,133,112,96,84,74,66,60,56,52,48,44,42,40,
38,36,34,32,30,28,28};

/*Inisialisasi input output */
void init_port()
{
        DDRC=0b11110000;
        DDRB=0b00001111;
        DDRD=0b11010011;
        DDRA=0b00000000;
        PORTC=0b11111111;
        //scld=1;sdad=1;
}

void init_ADC()
{
        /* Referensi AVcc*/
        SFIOR=SFIOR&0x0f;
        ADMUX=0x40;
        ADCSRA=0x02;
}
void initser()
{
     UBRRL=25;
     UBRRH=0;
     UCSRA=0x80;//aslinya 0
     UCSRB=0x98; //Txd,Rxd Enabled aslinya 18
     UCSRC=0x86; //8 bit data
}

unsigned char terimaser()
{
     while((UCSRA & 0x80) == 0x00);
     return UDR;
}

void kirimser(char TxData)
{
     while((UCSRA & 0x20) == 0x00);
     //while ( !( UCSRA & (1<<UDRE)) );
     UDR = TxData;
     delay_ms(10);
}
void kirimtext(flash char *text)
{
```

```
        while(*text)
        {
                kirimser(*text++);
        }
}
unsigned int konversi(unsigned char channel)
{
        unsigned char high,low;
        int data_konversi;

        /* pilih channel dengan referensi AVcc */
        ADMUX=(ADMUX&0xe0)|channel;

         /* Nyalakan ADC dan Start Konversi */
        ADCSRA=ADCSRA|0b11000000;

        /* tunggu proses konversi selesai */
        while((ADCSRA&0b00010000)!=0x10);

        /* matikan ADC, reset ADIF */
        ADCSRA=(ADCSRA|0b00010000)&0b01111111;

        /* data hasil konversi */
        delay_ms(1);
        low=ADCL;
        high=ADCH&0x03;
        data_konversi=(high%2)*256;
        high/=2;
        data_konversi=(data_konversi+((high%2)*512))+low;
        return data_konversi;
}
/*inisialisasi timer 1*/
void inttim(char in)
{
if(in==0)TIMSK=TIMSK & 0xFE;
else TIMSK=TIMSK|0x1;
}
void init_timer0()
{
        /* Timer ini akan digunakan sebagai penghitung kecepatan */
        /* Mode yang digunakan adalah normal */
        TCCR0=0x04;
        //TIMSK=TIMSK|0x1;
        TCNT0=0;
        inttim(1);
}

void kon(long int n)
{
        int ascii;
         ascii=n/1000+0x30;
         if(ascii==0x30) dataout(' ',1);
         else dataout(ascii,1);
         ascii=n/100%10+48; dataout(ascii,1);
         ascii=n/10%10+48; dataout(ascii,1);
         dataout(',',1);
         ascii=n%10+48; dataout(ascii,1);
}


void tampil_angka_bulat_5digit(long int biner)
{
         long int ascii;

         ascii=biner; ascii=(ascii/10000)|0x30; dataout(ascii,1);
         ascii=biner; ascii=(ascii/1000)|0x30; dataout(ascii,1);
         ascii=biner; ascii=((ascii/100)%10)|0x30; dataout(ascii,1);
```

```
        ascii=biner; ascii=((ascii/10)%10)|0x30; dataout(ascii,1);
        ascii=biner; ascii=(ascii%10)|0x30; dataout(ascii,1);
}

void tampil(unsigned int biner)
{
        long int ascii;

      //  ascii=biner; ascii=(ascii/10000)|0x30; dataout(ascii,1);
       // ascii=biner; ascii=(ascii/1000)|0x30; dataout(ascii,1);
        ascii=biner; ascii=((ascii/100)%10)|0x30; dataout(ascii,1);
        ascii=biner; ascii=((ascii/10)%10)|0x30; dataout(ascii,1);
        ascii=biner; ascii=(ascii%10)|0x30; dataout(ascii,1);
}
void post(unsigned char po,unsigned char st,unsigned int dt)
{
pos(po,st);tampil(dt);
}
interrupt [10] void timer0_overflow(void)
{
        #asm
        push r30
        push r31
        in   r30,SREG
        push r30
        #endasm
        //b++;
        //pengali++;
        triac=0;
        #asm("nop")
        #asm("nop")
        #asm("nop")
        #asm("nop")
        #asm("nop")
        #asm("nop")
        #asm("nop")
        #asm("nop")

        //triac=1;
        //inttim(0);
        #asm
        pop r30
        out SREG,r30
        pop r31
        pop r30
        #endasm*


* Turn registers saving off */
pragma savereg-
* interrupt handler */
nterrupt [5] void timer2_overflow(void)

        #asm
        push r30
        push r31
        in   r30,SREG
        push r30
        #endasm

        #asm
        pop r30
        out SREG,r30
        pop r31
        pop r30
        #endasm*
```

```
/* re-enable register saving for the other interrupts */
#pragma savereg+


/* Turn registers saving off */
#pragma savereg-
/* interrupt handler */
interrupt [2] void external_int0(void)
{
        #asm
        push r30
        push r31
        in   r30,SREG
        push r30
        #endasm
        triac=0;
/*
if(hit==1){TCNT0=-116;inttim(1);}
else if(hit==2){TCNT0=-102;inttim(1);}
else if(hit==3){TCNT0=-93;inttim(1);}
else if(hit==4){TCNT0=-85;inttim(1);}
else if(hit==5){TCNT0=-78;inttim(1);}
else if(hit==5){TCNT0=-78;inttim(1);}
else if(hit==6){TCNT0=-71;inttim(1);}
else if(hit==7){TCNT0=-63;inttim(1);}
else if(hit==8){TCNT0=-53;inttim(1);}
else if(hit==9){TCNT0=-42;inttim(1);}
else
*/

if(hit==10){inttim(1);triac=1;}
else if(hit==0){inttim(0);triac=0;}
else {TCNT0=-(time/64);inttim(1);}
        #asm
        pop r30
        out SREG,r30
        pop r31
        pop r30
        #endasm
}
#pragma savereg+
interrupt [3] void external_int1(void)
{
        #asm
        push r30
        push r31
        in   r30,SREG
        push r30
        #endasm
       b++;
triac=1;
/*
if(hit==1){TCNT0=-116;inttim(1);}
else if(hit==2){TCNT0=-102;inttim(1);}
else if(hit==3){TCNT0=-93;inttim(1);}
else if(hit==4){TCNT0=-85;inttim(1);}
else if(hit==5){TCNT0=-78;inttim(1);}
else if(hit==5){TCNT0=-78;inttim(1);}
else if(hit==6){TCNT0=-71;inttim(1);}
else if(hit==7){TCNT0=-63;inttim(1);}
else if(hit==8){TCNT0=-53;inttim(1);}
else if(hit==9){TCNT0=-42;inttim(1);}
else
*/

if(hit==10){inttim(1);triac=0;}
else if(hit==0){inttim(0);triac=1;}
```

```
else {TCNT0=-(time/64);inttim(1);}
        #asm
        pop r30
        out SREG,r30
        pop r31
        pop r30
        #endasm
}
#pragma savereg-
/* interrupt handler */
interrupt [12] void interuptrx(void)
{

     while((UCSRA & 0x80) == 0x00);
     if(UDR=='a')trx=1;

}
#pragma savereg+
void init_ext_interrupt()
{
        /* Set untuk interupt 0 rising edge */
        MCUCR=0x03;
        GICR=GICR|0x40;
}
void init_ext_interrupt1()
{
        /* Set untuk interupt 0 rising edge */
        MCUCR=0x05;
        GICR=GICR|0x80;
}
unsigned int loopkonv(unsigned char ch,unsigned char n)
{
        unsigned int a1;
        unsigned long int a;
        a=0;
        for(i=0;i<n;i++)
        {
        a1=konversi(ch);
        a=a+a1;
        }
        a=a/n;
        return(a);


float keyhasil()

float ke,ii;
char yh,asi;
int tdot;
ke=0;tdot=0;ii=1;
while(1)

yh=rkey();
if(yh=='E')break;
else if(yh=='.') tdot=1;
else if(tdot==1) {asi=yh-48;ke=(ke*10+asi);ii=ii*10;}
else {asi=yh-48;ke=ke*10+asi;}
dataout(yh,1);

return ke/ii;


* Program Utama */
void main()


       /* Inisialisasi */
```

```
init_port();
init_timer0();
//init_timer1();
//init_timer2();
init_ext_interrupt1();
initlcd();
init_ADC();
//initser();
//i2c_init();
delay_ms(10);

 hit=0;motor=1;triac=1;
#asm("cli")
cetak(1,1,"KADAR AIR DALAM");
cetak(2,1,"     MADU");
motor=0;
delay_ms(30000);
motor=1;triac=1;
delay_ms(2000);busek();
kental=loopkonv(1,100);
//p=121-(21*kental/100);
p=115-(15*kental/100);
if(p<0)p=0;
else if(p>100)p=100;
cetak(1,1,"Kadar air:");
cetak(1,16,"%");
post(1,12,p);
cetak(2,1,"Perlu penurunan?");
a=rkey();

do
{

busek();
#asm("cli")
motor=1;triac=1;
post(2,12,p);
cetak(1,1,"Setting Nilai:");
pos(2,1);x=keyhasil();
s=x;



#asm("sei")

while(1)
{
busek();
cetak(1,1,"Pengadukan");
cetak(2,1,"Suhu :    C");
motor=0;
for(a=0;a<30;a++)
{
suhu=loopkonv(0,100)/2;
post(2,7,suhu);
if(suhu<60)hit=10;
else if(suhu>65)hit=0;
else {hit=1;time=7000;}//suhu*700-35000;}
delay_ms(900);
 }
 motor=1;
 busek();
cetak(1,1,"      Proses");
cetak(2,1,"     Berhenti");
 for(a=0;a<5;a++)
{
suhu=loopkonv(0,100)/2;
```

```
if(suhu<60)hit=10;
else if(suhu>65)hit=0;
else {hit=1;time=7000;}//suhu*700-35000;}
delay_ms(900);
 }
busek();
cetak(1,1,"Suhu :    C");
cetak(2,1,"Kadar:    %");
suhu=loopkonv(0,100)/2;
post(1,7,suhu);
kental=loopkonv(1,100);
//p=122-(22*kental/100);
p=115-(15*kental/100);
if(p<0)p=0;
else if(p>100)p=100;
post(2,7,p);
delay_ms(3000);
if(p<s){busek();cetak(1,1,"Tercapai");delay_ms(1000);break;}
}
/*
kental=loopkonv(1,100);
p=kental;//122-(22*kental/100);
post(2,7,p);
*/
}while(1);
```

SNI

Standar Nasional Indonesia

SNI 01-3545-2004

Madu

ICS 67.180.10

Badan Standardisasi Nasional

Daftar isi

Daftar isi i
Prakata ii
1 Ruang lingkup 1
2 Acuan normatif 1
3 Istilah dan definisi 1
4 Persyaratan 1
5 Pengambilan contoh 2
6 Cara uji 2
7 Syarat lulus uji 3
8 Higiene 3
9 Penandaan 3
10 Pengemasan 3
Lampiran A (normatif) Persiapan contoh 4
Lampiran B (normatif) Cara uji aktifitas enzim diastase 5
Lampiran C (normatif) Cara uji hidroksimetilfurfural 8
Lampiran D (normatif) Cara uji kadar air 10
Lampiran E (normatif) Cara uji keasaman 12
Bibliografi 13
Tabel 1 Persyaratan mutu madu 8
Tabel B.1 Hubungan antara titik akhir pencampuran (menit) dengan nilai absorban 6
Tabel D.1 Hubungan indeks bias dengan kadar air pada madu 10

Prakata

Standar Nasional Indonesia (SNI) madu merupakan Revisi SNI 01-3545-1994, *Madu*. Standar ini disusun oleh Panitia Teknis 93S, Makanan dan Minuman.

Maksud dan tujuan penyusunan standar adalah sebagai acuan sehingga madu yang beredar di pasaran dapat terjamin mutu dan keamanannya.

Panitia teknis dalam menyusun rumusan SNI ini telah memperhatikan hal-hal yang tertera dalam:

) Undang-undang RI No. 7 tahun 1996 tentang Pangan;

) Undang-undang RI No. 8 tahun 1999 tentang Perlindungan Konsumen;

) Peraturan Pemerintah No.69 tahun 1999 tentang Label dan Iklan Pangan;

) Kumpulan Peraturan Perundang-undangan di Bidang Makanan tahun 1993 – 1994 Dit.Jen.POM, Dep.Kes.RI.

andar ini telah dibahas melalui rapat konsensus nasional pada tangal 17 Desember 2002 Jakarta. Hadir dalam rapat tersebut wakil-wakil dari konsumen, produsen, lembaga ilmu ngetahuan dan teknologi dan instansi terkait lainnya.

Madu

1 Ruang lingkup

Standar ini meliputi acuan normatif, istilah dan definisi, persyaratan mutu, pengambilan contoh, cara uji, syarat lulus uji, higiene, penandaan dan pengemasan untuk madu.

2 Acuan normatif

SNI 19-0428-1998, *Petunjuk pengambilan contoh padatan.*

SNI 01-2891-1992, *Cara uji makanan dan minuman.*

SNI 01-2892-1992, *Cara uji gula.*

SNI 01-2896-1998, *Cara uji cemaran logam dalam makanan.*

SNI 01-4866-1998, *Cara uji cemaran arsen dalam makanan.*

Codex Standard for Honey 12-1981, Rev.1 (1987).

Codex Standards for Sugars (including honey). CAC /Vol.III-Ed 1,1981.

AOAC Official Method, 16 th Ed. 5 th Revision, Vol.II, 1999, Sugars and Sugar Products.

3 Istilah dan definisi

madu
cairan alami yang umumnya mempunyai rasa manis yang dihasilkan oleh lebah madu dari sari bunga tanaman (floral nektar) atau bagian lain dari tanaman (ekstra floral nektar) atau ekskresi serangga.

4 Persyaratan

Persyaratan madu seperti Tabel di bawah ini:

Tabel 1 Persyaratan mutu madu

No	Jenis uji	Satuan	Persyaratan
1	Aktifitas enzim diastase, min.	DN	3
2	Hidroksimetilfurfural (HMF), maks.	mg/kg	50
3	Air, maks.	% b/b	22
4	Gula pereduksi (dihitung sebagai glukosa), min.	% b/b	65
	Sukrosa, maks.	% b/b	5
5	Keasaman, maks.	ml NaOH 1 N/kg	50

Tabel 1 (lanjutan)

No	Jenis uji	Satuan	Persyaratan
7	Padatan yang tak larut dalam air, maks.	% b/b	0,5
8	Abu, maks.	% b/b	0,5
9	Cemaran logam Timbal (Pb), maks Tembaga (Cu), maks.	 mg/kg mg/kg	 1,0 5,0
10	Cemaran arsen (As), maks.	mg/kg	0,5

Pengambilan contoh

ara pengambilan contoh sesuai SNI 19-0428-1998, *Petunjuk pengambilan contoh* adatan.

Cara uji

1 Persiapan contoh

ersiapan contoh sesuai dengan AOAC *Official Method* 920.180-1999 (Lampiran A).

2 Aktifitas enzim diastase

ira uji aktifitas enzim diastase sesuai dengan AOAC *Official Method* 958.09-1999 ampiran B).

Hidroksimetilfurfural (HMF)

ra uji hidroksimetilfurfural (HMF) sesuai dengan AOAC *Official Method* 980.23-1999 mpiran C).

Kadar air

ra uji kadar air sesuai dengan AOAC *Official Method* 969.38-1999 (lampiran D).

Kadar gula pereduksi

a uji gula sesuai dengan SNI 01-2892-1992, *Cara uji gula*, butir 2.1.

Kadar sukrosa

a uji sukrosa sesuai dengan SNI 01-2892-1992, *Cara uji gula*, butir 3.1.

Keasaman

a uji keasaman sesuai dengan CAC/Vol.III-Ed 1. *Codex Standards for Sugars (including ey)* (Lampiran E).

6.8 Padatan tak larut dalam air

Cara uji padatan tak larut dalam air sesuai dengan SNI 01-2891-1992, *Cara uji makanan dan minuman,* butir 13.

6.9 Kadar abu

Cara uji kadar abu sesuai dengan SNI 01-2891-1992, *Cara uji makanan dan minuman.*

6.10 Cemaran logam dalam makanan

Cara uji cemaran logam sesuai dengan SNI 01-2896-1998, *Cara uji cemaran logam dalam makanan.*

6.11 Cemaran arsen

Cemaran arsen sesuai dengan SNI 01-4866-1998, *Cara uji cemaran arsen dalam makanan.*

7 Syarat lulus uji

Produk dinyatakan lulus uji apabila memenuhi syarat mutu.

8 Higiene

Madu harus di produksi secara higienis termasuk cara penyiapan dan penanganan yang mengacu pada peraturan Departemen Kesehatan RI yang berlaku tentang Pedoman cara produksi yang baik untuk makanan.

9 Penandaan

Penandaan dan pelabelan madu sesuai dengan Undang-undang RI No. 7 Tahun 1996 tentang Pangan dan Peraturan Pemerintah No.69 Tahun 1999 tentang Label dan Iklan Pangan.

10 Pengemasan

Madu dikemas dalam wadah yang tertutup rapat tidak dipengaruhi atau mempengaruhi isi, aman selama penyimpanan dan pengangkutan.

Lampiran A
(normatif)

Persiapan contoh

A.1 Acuan

AOAC Official Method 920.180-1999

A.2 Prinsip

Contoh yang dipersiapkan harus dalam kondisi siap pakai/dalam bentuk cairan (lolos ayakan *U. S Sieve* No.40) dan untuk mencegah kerusakan suhu madu tidak boleh melebihi 40°C.

A.3 Prosedur

A.3.1 Madu dalam bentuk cairan

Contoh untuk penetapan enzim diastase dan hidroksimetilfurfural (HMF) tidak boleh dipanaskan. Jadi, penetapan dilakukan langsung dari contoh asal, tanpa perlakuan lain kecuali penyaringan, pengadukan dan pengocokan. Jika contoh tidak mengandung bagian-bagian yang menggumpal maka contoh cukup dikocok atau diaduk dengan baik. Jika mengandung bagian-bagian yang menggumpal, contoh dipanaskan dalam wadah tertutup diatas penangas air 60°C–65°C selama 30 menit. Selama pemanasan, contoh digoyang/diaduk sewaktu-waktu dan didinginkan setelah mencair seluruhnya. Jika madu mengandung bahan asing seperti lilin lebah, partikel sarang lebah dan bahan-bahan asing lainnya maka madu harus dipanaskan sampai 40°C diatas penangas air dan disaring dengan kain saring melalui corong yang dilengkapi dengan pemanasan oleh aliran air panas.

A.3.2 Madu masih dalam sarang lebah

Jika contoh yang diterima masih dalam tempat madu sarang lebah, maka tempat madu mula-mula dipotong melintang pada bagian atasnya kemudian saring melalui saringan mesh *U.S. Sieve* No.40). Jika partikel-partikel sarang lebah dan lilin ikut melalui saringan, maka lakukan perlakuan pemanasan seperti pada butir A.3.1 dan saring dengan kain saringan. Jika madunya menggumpal dalam tempat madu, maka hangatkan sampai lilinnya mencair, aduk, dinginkan dan pisahkan lilinnya.

Lampiran B
(normatif)

Cara uji aktifitas enzim diastase

B.1 Acuan

AOAC Official Method 958.09-1999

B.2 Prinsip

Larutan pati yang ditambahkan iod akan menghasilkan warna biru. Enzim diastase akan mengubah pati menjadi gula. Dengan adanya aktifitas enzim diastase warna biru pada larutan pati akan hilang. Semakin tinggi aktifitas enzim semakin cepat hilangnya warna biru dari pati.

B.3 Pereaksi

a) **Larutan stock iod**
Larutkan 8,80 g resublimisi (p.a) dalam 30ml - 40ml air yang mengandung 22,0 g KI (p.a) dan encerkan dengan air sampai volume 1 liter.

b) **Larutan iod 0,0007 N**
Larutkan 20 g KI (p.a) dan 5,0 ml larutan stock iod dalam labu ukur 500 ml, encerkan dan tepatkan sampai tanda tera dengan air suling. Larutan harus diperbaharui setiap 2 hari sekali.

c) **Larutan dapar asetat pH 5,3 (1,59 M)**
Larutkan 87 g CH_3 COONa., $3H_2O$ dalam 400 ml air, kemudian tambahkan kira-kira 10,5 ml larutan asam asetat dalam air. Tepatkan volumenya sampai 500 ml dengan penambahan air. Atur larutan sampai pH 5,3 dengan penambahan air, natrium asetat atau asam asetat jika perlu.

d) **Larutan natrium klorida 0,5 M**
Larutkan 14,5 g natrium klorida (p.a) dalam air suling yang telah dididihkan dan volumenya dibuat 500 ml. Larutan ini perlu sering diperbaharui karena mudah berjamur.

e) **Larutan pati**
Timbang 2,000 g pati dapat larut (dengan spesifikasi khusus untuk penetapan daya diastase dapat diperoleh dari *Thomas Scientific*, cat No. C733-L51; *Pfanstichl Laboratories, Inc.*, 1219. *Glen Rock Ave, Waukegan*, IL60085-0439, atau yang setara) dan campurkan dengan 90 ml air suling dalam erlenmeyer 250 ml. Didihkan segera sambil sering diaduk. Kurangi pemanasan dan lanjutkan pendidihan secara hati-hati selama 3 menit, tutup dan biarkan dingin sampai suhu kamar. Pindahkan kedalam labu ukur 100 ml, encerkan dan tepatkan hingga tanda tera. Perhatikan dengan seksama keragaman nilai absorban blanko iod-pati.

f) **Standardisasi**
Pipet 5 ml larutan pati kedalam 10 ml air dan campur baik-baik. Kemudian pipet 1 ml campuran tersebut kedalam beberapa wadah (piala gelas erlenmeyer) 50 ml yang mengandung 10 ml larutan iod encer. Campurkan baik-baik bila perlu encerkan dengan air suling untuk memperoleh nilai absorban 0,760 ± 0,02.

B.4 Peralatan

a) Fotometer fotoelektrik, pembacaan pada 660 nm (dengan filter merah) atau 600 nm (filterintervensi) dengan cell 1 cm.

b) Penangas air, suhu (40 ± 0,2) ^{0}C.

c) Tabung reaksi. Hubungkan lengan sampai yang tertutup berukuran 18 mm x 60 mm, dengan tabung reaksi ukuran 18 mm x 175 mm. Bagian bawah lengan sampai tertutup dihubungkan 100mm dari bagian bawah tabung dengan membentuk sudut 45^0 dengan bagian bawah tabung.

B.5 Prosedur

B.5.1 Persiapan contoh

Timbang 5 gram madu kedalam piala 20 ml, tambah 10 ml – 15 ml air dan 2,5 ml larutan dapar asetat. Dalam keadaan dingin larutan diaduk sampai contoh madu larut seluruhnya. Pindahkan larutan contoh ini kedalam labu ukur 25 ml yang berisi 1,5 ml larutan NaCl, epatkan sampai tanda tera dengan air (larutan harus didapatkan dahulu sebelum itambahkan larutan NaCl).

B.5.2 Penetapan absorban

Pipet 10 ml larutan contoh, masukkan kedalam tabung reaksi 50 ml dan letakkan dalam penangas air 40^0 ± 0,2^{0}C bersama dengan erlenmeyer berisi larutan pati. Setelah 15 menit, pipet 5 ml larutan pati dan masukan kedalam larutan contoh, kocok dan hidupkan stopwatch.Setiap interval waktu 5 menit, pipet 1 ml campuran contoh tersebut dan ambahkan kedalam 10,00 ml larutan iod. Campurkan, kemudian encerkan sampai volume seperti sebelumnya dan tetapkan nilai absorbannya pada panjang gelombang 660 nm. Catat waktu sejak pencampuran pati dengan madu sampai dengan pada penambahan cairan pada iod sebagai waktu reaksi (letakkan pipet 1 ml dalam tabung reaksi untuk digunakan embali apabila cairan diambil kembali). Lanjutkan pengambilan larutan dalam selang waktu tertentu sampai diperoleh nilai A< 0,235.

Tabel B.1 Hubungan antara titik akhir pencampuran (menit) dengan nilai absorban

Absorban	Titik akhir, menit
0,7	> 25
0,65	20 – 25
0,60	15 – 18
0,55	11 – 13
0,50	9 – 10
0,45	7 - 8

B.6 Perhitungan

Plotkan nilai absorban terhadap waktu (menit) diatas kertas millimeter. Garis lurus digambarkan melalui beberapa titik. Dari grafik ditetapkan waktu yang diperlukan untuk mencapai nilai absorban (A) = 0,235. Nilai ini jika dibagi 300 menunjukkan aktifitas enzim diastase (DN).

CATATAN Pembacaan waktu 5 menit cukup untuk memperkirakan titik akhir dari contoh yang memiliki nilai DN yang tinggi (> 35) apabila nilai lain diambil cukup cepat untuk mendapatkan A kira-kira 0,20. Guna memperoleh hasil yang teliti, ulangi penetapan dengan cara mengambil contoh setiap menit sejak awal. Bila contoh yang memiliki DN yang rendah, pembacaan dimulai pada saat 10 menit.

Lampiran C
(normatif)

Cara uji hidroksimetilfurfural (HMF)

C.1 Acuan

AOAC Official Method 980.23-1999.

C.2 Prinsip

Perbedaan absorbansi contoh pada panjang gelombang 284 nm dari 336 nm dengan larutan natrium bisulfit ($NaHSO_3$) sebagai pembanding.

C.3 Pereaksi

a) **Larutan Carrez I**
Timbang 15 g kalium feroksianida $K_4Fe(CN)_6\ 3H_2O$, larutkan dengan air dan encerkan sampai 100 ml.

b) **Larutan Carrez II**
Timbang 30 g seng asetat Zn $(CH_3COO)_2\ 2H_2O$, larutkan dengan air dan encerkan sampai 100ml.

c) **Natrium bisulfit ($NaHSO_3$) 0,20 %**
Timbang 0,20 g $NaHSO_3$, larutkan dengan air dan encerkan sampai 100 ml.

C.4 Peralatan

Spektrofotometer yang biasa dipakai harus mempunyai panjang gelombang 284 nm dan 336 nm, mempunyai sel 1 cm.

C.5 Prosedur

Timbang dengan teliti 5g madu (sampai ketelitian 1 mg) dalam piala gelas kecil, masukkan ke dalam labu ukur 50ml dan bilas dengan air sampai volume larutan 25 ml. Tambah 0,50 ml larutan Carrez I, kocok dan tambahkan 0,50ml larutan Carrez II, kocok kembali dan encerkan dengan air sampai dengan tanda garis. Tambahkan setetes alkohol untuk menghilangkan busa pada permukaan. Saring melalui kertas saring, dan buang 10ml saringan pertama.

Pipet 5ml saringan dan masing-masing masukkan kedalam tabung reaksi 18ml x 150ml. Pipet 5ml air dan masukan kedalam salah satu tabung (contoh) dan 5ml 0,20 % Natrium bisulfit kedalam tabung lainnya (pembanding). Kocok sampai tercampur sempurna (Vordex mixer) dan tetapkan absorban contoh terhadap reference (pembanding) dalam cell 1cm pada panjang gelombang 284nm dan 336nm. Bila absorban lebih tinggi dari 0,6 untuk memperoleh hasil yang teliti, larutan contoh diencerkan dengan air sesuai kebutuhan. Demikian juga dengan larutan pembanding (larutan referensi) encerkan dengan cara sama

dengan menggunakan larutan $NaHSO_3$ 0,1%, nilai absorban yang diperoleh dikalikan dengan faktor pengenceran sebelum perhitungan.

C.6 Perhitungan

$$\text{HMF (mg/100 g madu)} = \frac{(A284-A336) \times 14,97 \times 5}{\text{Bobot contoh (g)}}$$

$$\text{Faktor} : \frac{126}{16830} \times \frac{1000}{10} \times \frac{100}{5} = 14,97$$

Keterangan:

126 adalah bobot molekul HMF;
16830 adalah absorbansifitas moler HMF pada panjang gelombang 284nm;
1000 adalah mg/g;
10 adalah sentiliter/L;
100 adalah gram madu yang dilaporkan;
5 adalah bobot contoh yang diambil dalam gram.

Lampiran D
(normatif)

Cara uji kadar air

D.1 Acuan

AOAC Official Method 969.38-1999.

D.2 Prinsip

Pembacaan nilai indeks bias madu pada suhu 20°C, atau suhu pembacaan yang telah dikoreksi 20°C, menunjukkan besarnya kadar air dari contoh madu.

D.3 Peralatan

Refraktometer.

D.4 Prosedur

Tetapkan pembacaan nilai indeks bias contoh pada suhu 20°C dengan menggunakan alat refraktometer. Cari kandungan air dalam contoh dengan membandingkan nilai indeks bias dan air pada Tabel D.1 dibawah ini. Jika penetapan tidak dibulatkan pada suhu 20°C, hitung nilai koreksi suhu itu sebagaimana yang tertera dalam catatan kaki.

Tabel D.1 Hubungan indeks bias dengan kadar air pada madu [a)]

Indeks bias (20^0C)[b)]	Kadar air	Indeks bias	Kadar air ($20\ ^0C$)[b)]
1.5044	13.0	1.4890	19.0
1.5038	13.2	1.4885	19.2
1.5033	13.4	1.4880	19.4
1.5028	13.6	1.4875	19.6
1.5023	13.8	1.4870	19.8
1.5018	14.0	1.4865	20.0
1.5012	14.2	1.4860	20.2
1.5007	14.4	1.4855	20.4
1.5002	14.6	1.4850	20.6
1.4997	14.8	1.4845	20.8
1.4992	15.0	1.4840	21.0
1.4987	15.2	1.4835	21.2
1.4982	15.4	1.4830	21.4
1.4976	15.6	1.4825	21.6
1.4971	15.8	1.4820	21.8
1.4966	16.0	1.4815	22.0
1.4961	16.2	1.4810	22.2
1.4956	16.4	1.4805	22.4
1.4951	16.6	1.4800	22.6
1.4946	16.8	1.4795	22.8
1.4940	17.0	1.4790	23.0
1.4935	17.2	1.4785	23.2
1.4930	17.4	1.4780	23.4
1.4925	17.6	1.4775	23.6
1.4920	17.8	1.4770	23.8
1.4915	18.0	1.4765	24.0
1.4910	18.2	1.4760	24.2
1.4905	18.4	1.4755	24.4
1.4900	18.6	1.4750	24.6
1.4895	18.8	1.4745	24.8
		1.4740	25.0

a) *Nilai untuk 20^0C merupakan nilai perhitungan Wedmori's (Bee World* 36, 197 (1955). Nilai 22 % diperoleh dari FAO/WHO *Codex Committee on Methods of Analysis and Sampling* (1968).

b) Jika nilai indeks bias diukur pada suhu dibawah $20\ ^0C$ tambahkan $0{,}000023\ ^0$ C pada angka tabel, bila pengukuran dilakukan pada suhu diatas $20\ ^0$ C, kurangkan $0{,}00023/^0$ C dari angka tabel.

Lampiran E
(normatif)

Cara uji keasaman

E.1 Acuan

CAC/Vol.III-Ed.1,1981.

E.2 Prinsip

Netralisasi asam dengan basa.

E.3 Peralatan

a) neraca analitik terkalibrasi;
b) buret 10 ml, terkalibrasi;
c) erlenmeyer 250 ml.

E.4 Pereaksi

a) larutan natrium hidroksida, NaOH 0,1 N, bebas karbonat;
b) indikator fenoftalein, pp 1% dalam etanol, netral;
c) air suling, bebas CO_2.

E.5 Prosedur

a) Timbang dengan teliti 10,0 g madu, masukkan kedalam erlenmeyer 250 ml kemudian larutkan dengan 75 ml air suling dan tambahkan 4 - 5 tetes indikator PP.
b) Titar dengan larutan NaOH 0,1 N sampai titik akhir yang tetap selama 10 detik.
c) Catat volume NaOH 0,1 N yang digunakan untuk titrasi.
d) Sebagai alternatif, dapat digunakan pH meter dan contoh dititar sampai pH 8,3.
e) Hitung keasaman dalam madu.

E.6 Perhitungan

$$\text{Keasaman (ml N NaOH/kg)} = \frac{a \times b}{c} \times 1000$$

Keterangan:
a adalah volume NaOH 0,1 N yang digunakan dalam titrasi, ml.
b adalah normalitas NaOH 0,1 N.
c adalah bobot contoh, gram.

Bibliografi

Honey Quality and International Regulatory Standards: Review by The International Honey Commission.

tures

- ®– High-performance and Low-power RISC Architecture
- 118 Powerful Instructions – Most Single Clock Cycle Execution
- 32 x 8 General-purpose Working Registers
- Up to 8 MIPS Throughput at 8 MHz

a and Nonvolatile Program Memories

- *8K Bytes of In-System Programmable Flash*
  - SPI Serial Interface for In-System Programming
  - Endurance: 1,000 Write/Erase Cycles
- 512 Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- 512 Bytes Internal SRAM
- Programming Lock for Software Security

ipheral Features

- 8-channel, 10-bit ADC
- Programmable UART
- Master/Slave SPI Serial Interface
- Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
- One 16-bit Timer/Counter with Separate Prescaler, Compare and Capture Modes and Dual 8-, 9-, or 10-bit PWM
- *Programmable Watchdog Timer with On-chip Oscillator*
- On-chip Analog Comparator

ɔcial Microcontroller Features

- Power-on Reset Circuit
- Real-time Clock (RTC) with Separate Oscillator and Counter Mode
- External and Internal Interrupt Sources
- Three Sleep Modes: Idle, Power Save and Power-down

ver Consumption at 4 MHz, 3V, 20°C

- Active: 6.4 mA
- Idle Mode: 1.9 mA
- Power-down Mode: <1 µA

and Packages

- 32 Programmable I/O Lines
- 40-lead PDIP, 44-lead PLCC, 44-lead TQFP, and 44-pad MLF

ɜrating Voltages

- V_{CC}: 4.0 - 6.0V AT90S8535
- V_{CC}: 2.7 - 6.0V AT90LS8535

ɜed Grades:

- 0 - 8 MHz for the AT90S8535
- 0 - 4 MHz for the AT90LS8535

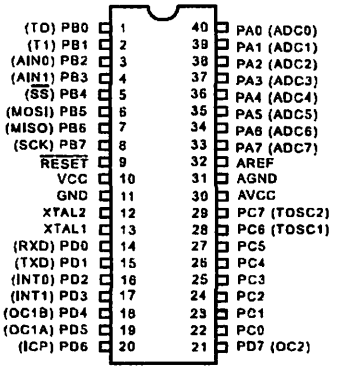
8-bit AVR® Microcontroller with 8K Bytes In-System Programmable Flash

AT90S8535
AT90LS8535

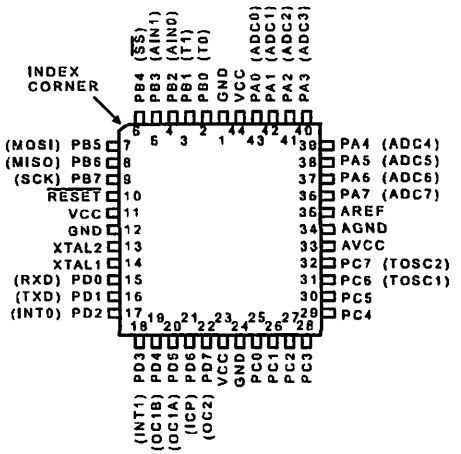
Rev. 1041H–11/01

Configurations

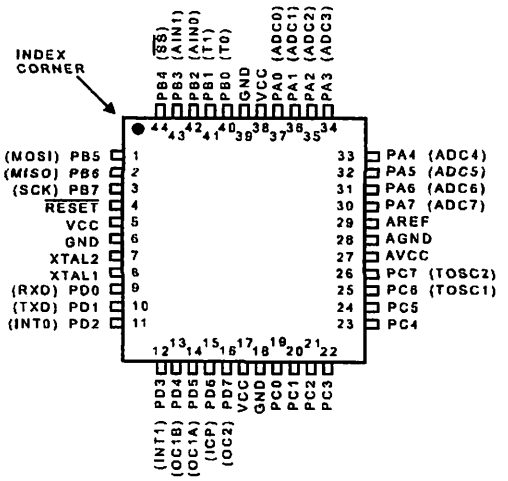
PDIP



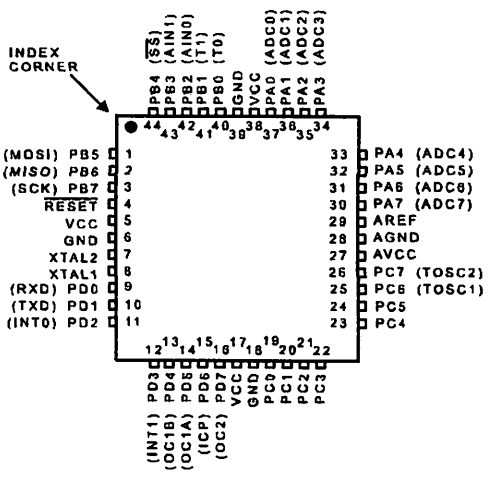
PLCC



TQFP



MLF

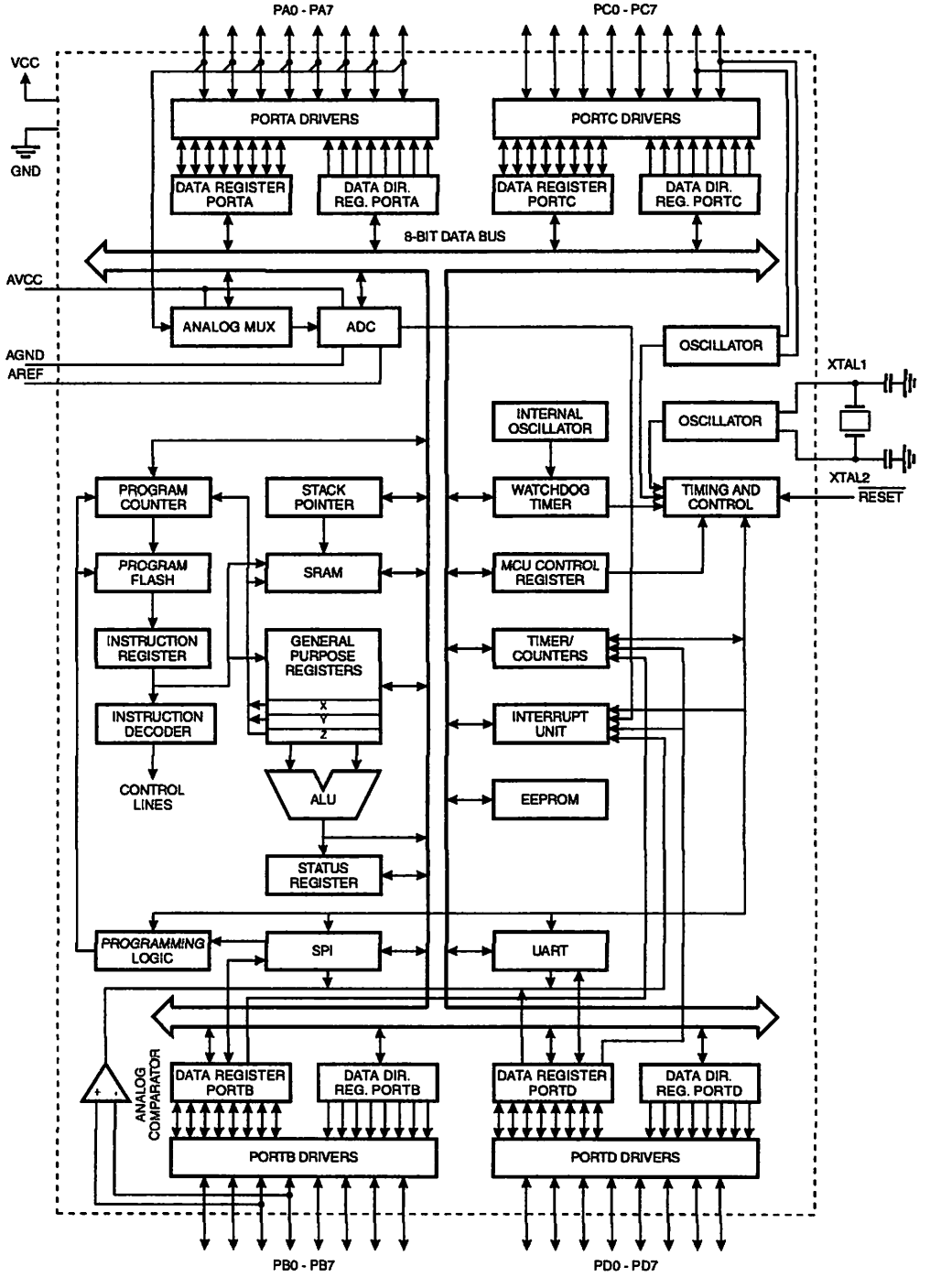


cription

The AT90S8535 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the AT90S8535 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

:k Diagram

Figure 1. The AT90S8535 Block Diagram



The AVR core combines a rich instruction set with 32 general-purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The AT90S8535 provides the following features: 8K bytes of In-System Programmable Flash, 512 bytes EEPROM, 512 bytes SRAM, 32 general-purpose I/O lines, 32 general-purpose working registers, Real-time Clock (RTC), three flexible timer/counters with compare modes, internal and external interrupts, a programmable serial UART, 8-channel, 10-bit ADC, programmable Watchdog Timer with internal oscillator, an SPI serial port and three software-selectable power-saving modes. The Idle Mode stops the CPU while allowing the SRAM, timer/counters, SPI port and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power Save Mode, the timer oscillator continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining an 8-bit RISC CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT90S8535 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The AT90S8535 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators and evaluation kits.

Descriptions

Digital supply voltage.

Digital ground.

A (PA7..PA0)

Port A is an 8-bit bi-directional I/O port. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers can sink 20 mA and can drive LED displays directly. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

Port A also serves as the analog inputs to the A/D Converter.

The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors. The Port B output buffers can sink 20 mA. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. Port B also serves the functions of various special features of the AT90S8535 as listed on page 78.

The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

C (PC7..PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors. The Port C output buffers can sink 20 mA. As inputs, Port C pins that are externally pulled low will source

current if the pull-up resistors are activated. Two Port C pins can alternatively be used as oscillator for Timer/Counter2.

The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors. The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated.

Port D also serves the functions of various special features of the AT90S8535 as listed on page 86.

The Port D pins are tri-stated when a reset condition becomes active, even if the clock is *not running.*

ET

Reset input. An external reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

.1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

.2

Output from the inverting oscillator amplifier.

C

AVCC is the supply voltage pin for Port A and the A/D Converter. If the ADC is not used, this pin must be connected to VCC. If the ADC is used, this pin must be connected to VCC via a low-pass filter. See page 68 for details on operation of the ADC.

F

AREF is the analog reference input for the A/D Converter. For ADC operations, a voltage in the range 2V to AV_{CC} must be applied to this pin.

D

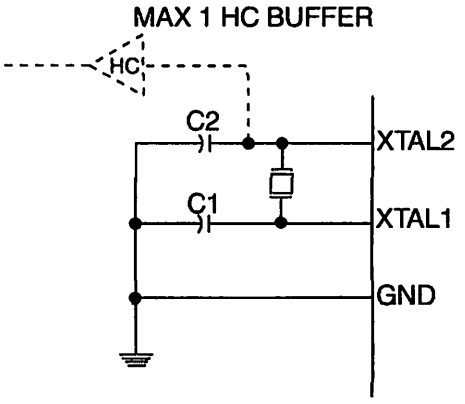
Analog ground. If the board has a separate analog ground plane, this pin should be connected to this ground plane. Otherwise, connect to GND.

:k Options

:al Oscillator

XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or a ceramic resonator may be used.

Figure 2. Oscillator Connections

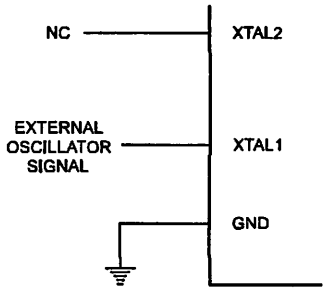


Note: When using the MCU Oscillator as a clock for an external device, an HC buffer should be connected as indicated in the figure.

'nal Clock

To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 3.

Figure 3. External Clock Drive Configuration



r Oscillator

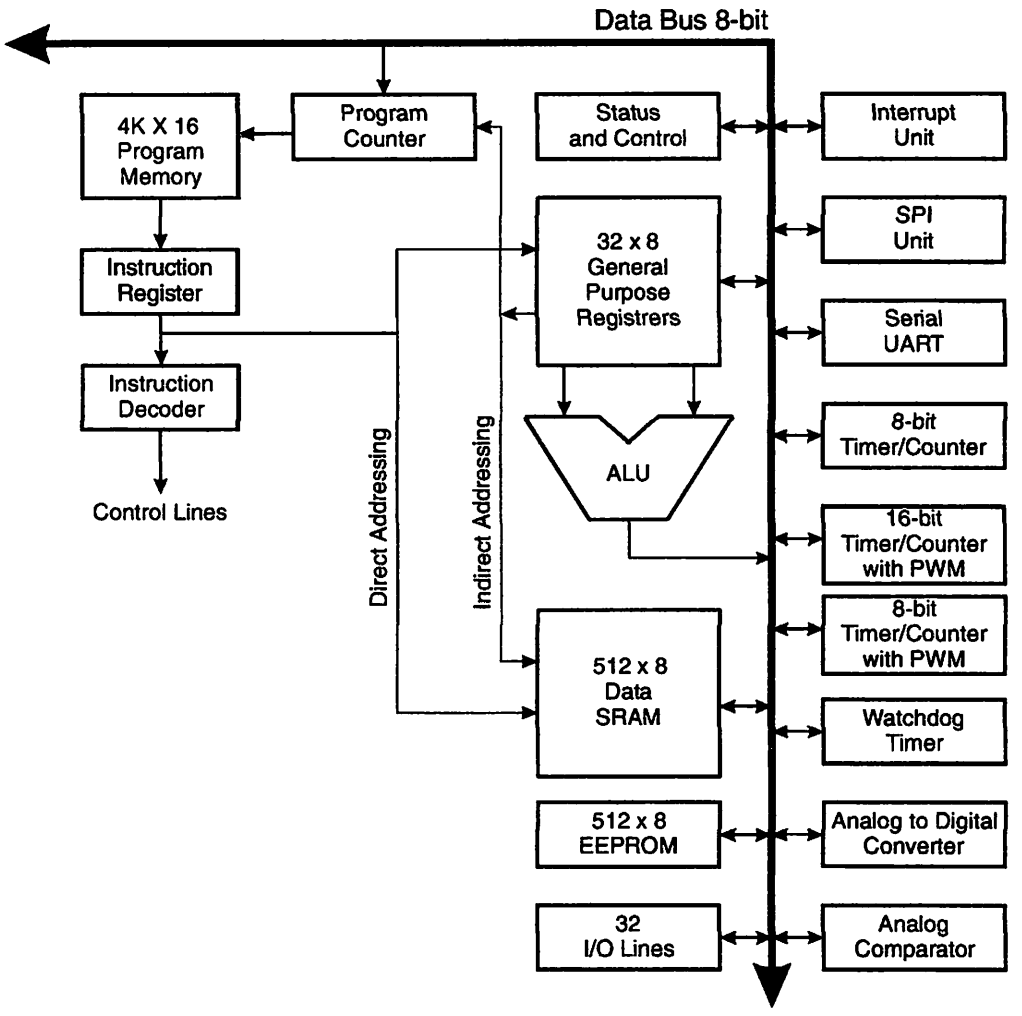
For the Timer Oscillator pins, TOSC1 and TOSC2, the crystal is connected directly between the pins. No external capacitors are needed. The oscillator is optimized for use with a 32,768 Hz watch crystal. Applying an external clock source to TOSC1 is not recommended.

hitectural rview

The fast-access register file concept contains 32 x 8-bit general-purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one Arithmetic Logic Unit (ALU) operation is executed. Two operands are output from the register file, the operation is executed and the result is stored back in the register file – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing, enabling efficient address calculations. One of the three address pointers is also used as the address pointer for the constant table look-up function. These added function registers are the 16-bit X-register, Y-register, and Z-register.

Figure 4. The AT90S8535 AVR RISC Architecture



The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 4 shows the AT90S8535 AVR RISC microcontroller architecture.

In addition to the register operation, the conventional memory addressing modes can be used on the register file as well. This is enabled by the fact that the register file is

assigned the 32 lowermost Data Space addresses ($00 - $1F), allowing them to be accessed as though they were ordinary memory locations.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, Timer/Counters, A/D converters and other I/O functions. The I/O memory can be accessed directly or as the Data Space locations following those of the register file, $20 - $5F.

The AVR uses a Harvard architecture concept – with separate memories and buses for program and data. The program memory is executed with a two-stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system downloadable Flash memory.

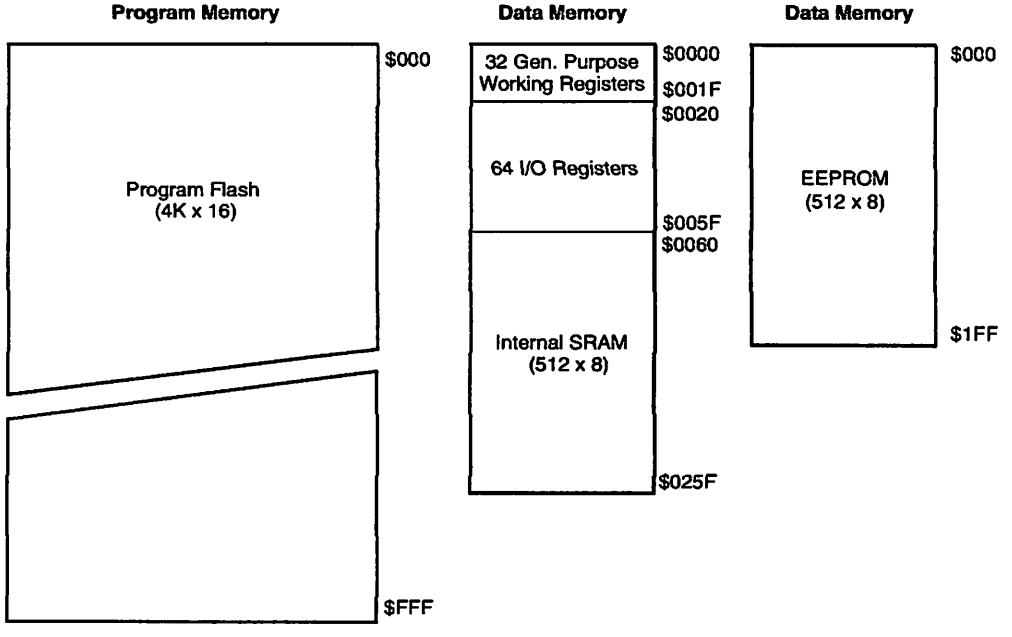
With the relative jump and call instructions, the whole 4K address space is directly accessed. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

During interrupts and subroutine calls, the return address Program Counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM and consequently, the stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The 10-bit stack pointer (SP) is read/write-accessible in the I/O space.

The 512 bytes data SRAM can be easily accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

Figure 5. Memory Maps



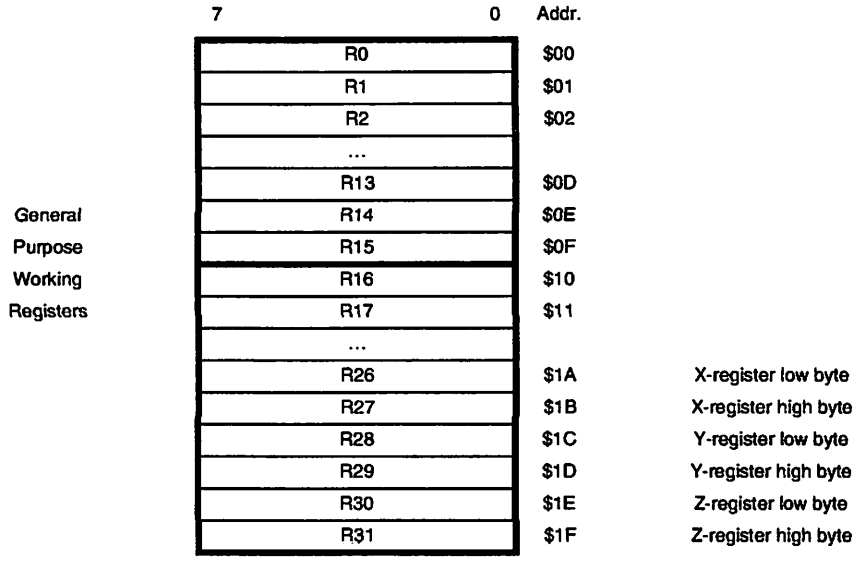
A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All the different interrupts have a separate interrupt vector in the interrupt vector table at the beginning of the program

memory. The different interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

eral-purpose ister File

Figure 6 shows the structure of the 32 general-purpose working registers in the CPU.

Figure 6. AVR CPU General-purpose Working Registers



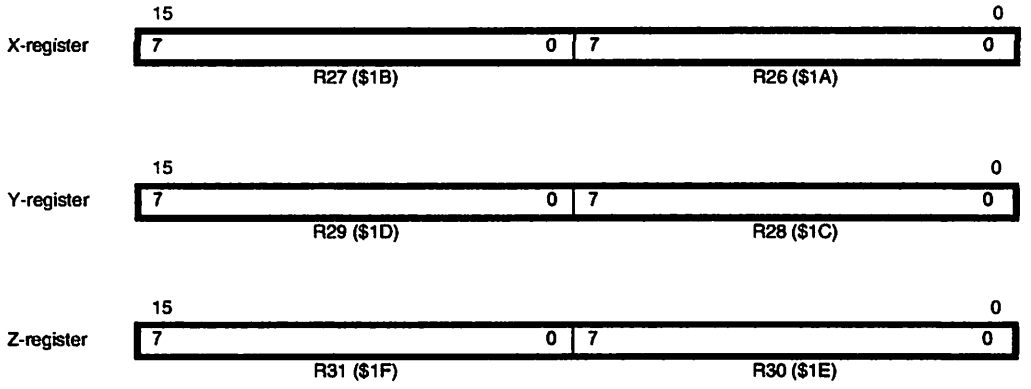
All the register operating instructions in the instruction set have direct and single-cycle access to all registers. The only exception is the five constant arithmetic and logic instructions SBCI, SUBI, CPI, ANDI and ORI between a constant and a register and the LDI instruction for load immediate constant data. These instructions apply to the second half of the registers in the register file (R16..R31). The general SBC, SUB, CP, AND, and OR and all other operations between two registers or on a single register apply to the entire register file.

As shown in Figure 6, each register is also assigned a data memory address, mapping them directly into the first 32 locations of the user Data Space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y-, and Z-registers can be set to index any register in the file.

ister, Y-register and Z-ter

The registers R26..R31 have some added functions to their general-purpose usage. These registers are address pointers for indirect addressing of the Data Space. The three indirect address registers, X, Y, and Z, are defined in Figure 7.

Figure 7. X-, Y-, and Z-register



In the different addressing modes, these address registers have functions as fixed displacement, automatic increment and decrement (see the descriptions for the different instructions).

– Arithmetic Logic

The high-performance AVR ALU operates in direct connection with all the 32 general-purpose working registers. Within a single clock cycle, ALU operations between registers in the register file are executed. The ALU operations are divided into three main categories: arithmetic, logical and bit functions.

ystem Programmable h Program Memory

The AT90S8535 contains 8K bytes On-chip, In-System Programmable Flash memory for program storage. Since all instructions are 16- or 32-bit words, the Flash is organized as 4K x 16. The Flash memory has an endurance of at least 1000 write/erase cycles. The AT90S8535 Program Counter (PC) is 12 bits wide, thus addressing the 4096 program memory addresses.

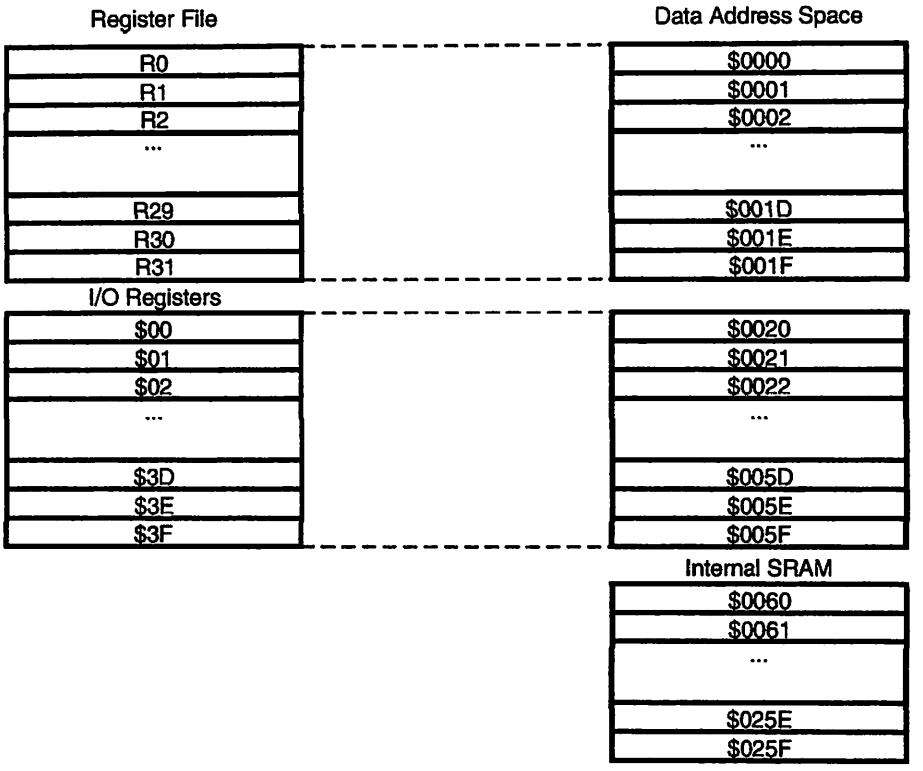
See page 99 for a detailed description on Flash data downloading.

See page 12 for the different program memory addressing modes.

M Data Memory

Figure 8 shows how the AT90S8535 SRAM memory is organized.

Figure 8. SRAM Organization



The lower 608 data memory locations address the Register file, the I/O memory and the internal data SRAM. The first 96 locations address the Register file + I/O memory, and the next 512 locations address the internal data SRAM.

The five different addressing modes for the data memory cover: Direct, Indirect with Displacement, Indirect, Indirect with Pre-decrement and Indirect with Post-increment. In the register file, registers R26 to R31 feature the indirect addressing pointer registers.

The direct addressing reaches the entire data space.

The Indirect with Displacement mode features 63 address locations reached from the base address given by the Y- or Z-registers.

When using register indirect addressing modes with automatic pre-decrement and post-increment, the address registers X, Y, and Z are decremented and incremented.

The 32 general-purpose working registers, 64 I/O registers and the 512 bytes of internal data SRAM in the AT90S8535 are all accessible through all these addressing modes.

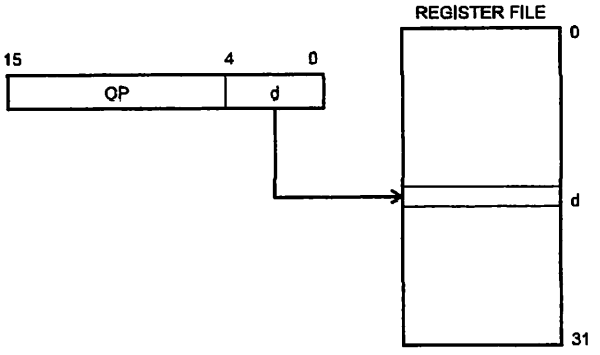
See the next section for a detailed description of the different addressing modes.

ıram and Data ressing Modes

The AT90S8535 AVR RISC microcontroller supports powerful and efficient addressing modes for access to the program memory (Flash) and data memory (SRAM, register file and I/O memory). This section describes the different addressing modes supported by the AVR architecture. In the figures, OP means the operation code part of the instruction word. To simplify, not all figures show the exact location of the addressing bits.

ster Direct, Single ster Rd

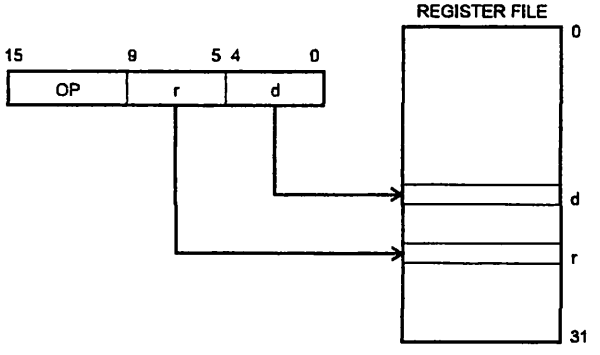
Figure 9. Direct Single Register Addressing



The operand is contained in register d (Rd).

ster Direct, Two Registers nd Rr

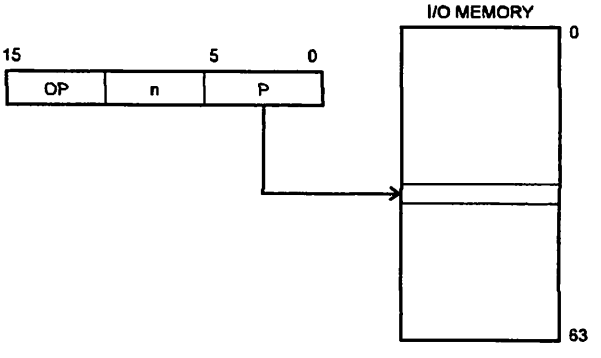
Figure 10. Direct Register Addressing, Two Registers



Operands are contained in register r (Rr) and d (Rd). The result is stored in register d (Rd).

irect

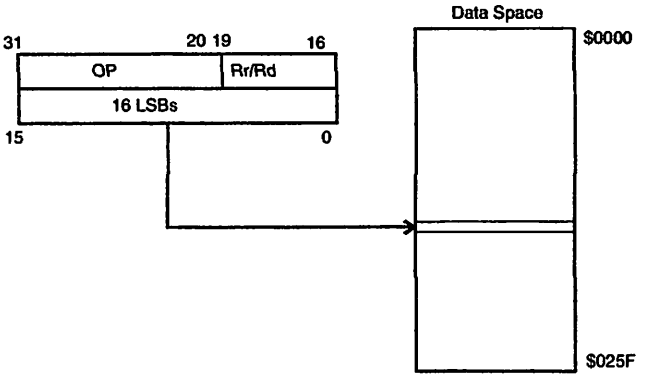
Figure 11. I/O Direct Addressing



Operand address is contained in six bits of the instruction word. n is the destination or source register address.

Direct

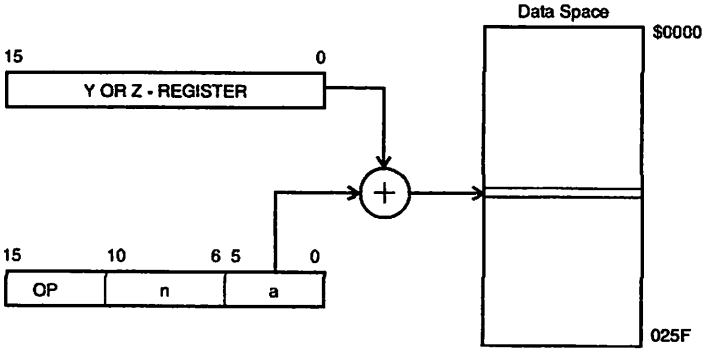
Figure 12. Direct Data Addressing



A 16-bit data address is contained in the 16 LSBs of a 2-word instruction. Rd/Rr specify the destination or source register.

Indirect with acement

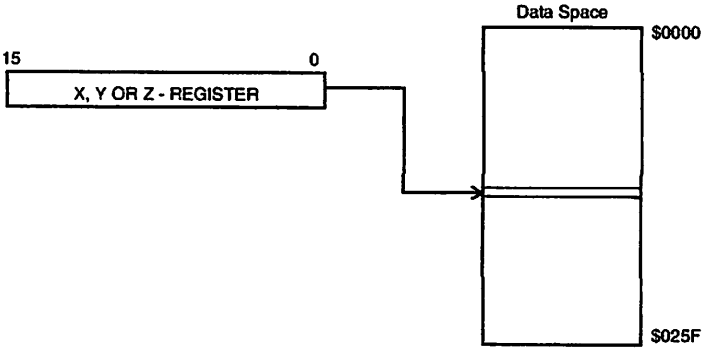
Figure 13. Data Indirect with Displacement



Operand address is the result of the Y- or Z-register contents added to the address contained in six bits of the instruction word.

Indirect

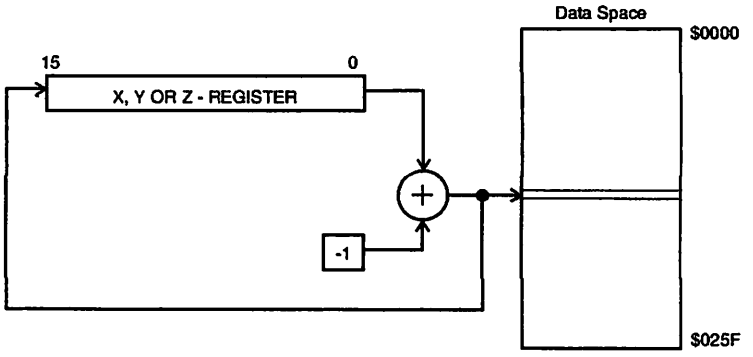
Figure 14. Data Indirect Addressing



Operand address is the contents of the X-, Y-, or the Z-register.

Indirect with Pre-ment

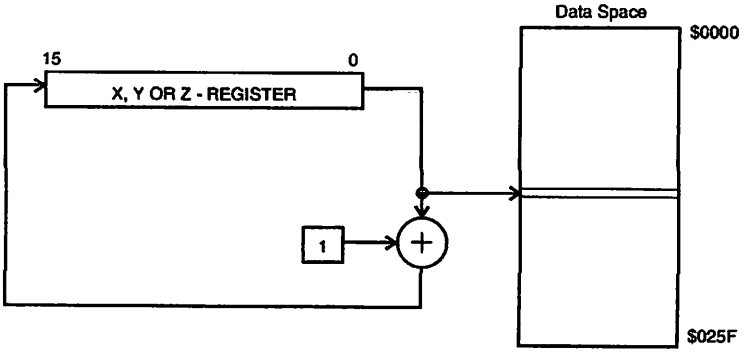
Figure 15. Data Indirect Addressing with Pre-decrement



The X-, Y-, or the Z-register is decremented before the operation. Operand address is the decremented contents of the X-, Y-, or the Z-register.

Indirect with Post-ment

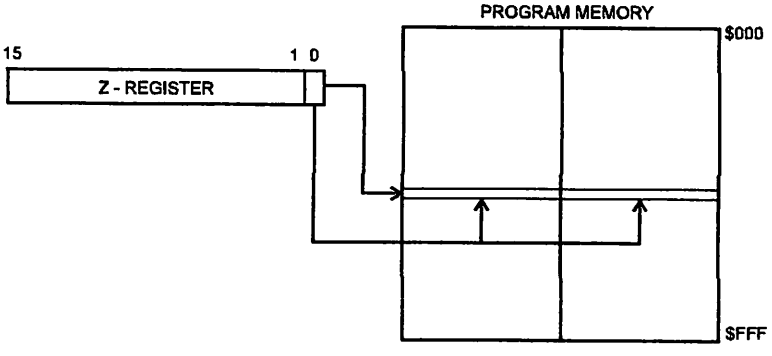
Figure 16. Data Indirect Addressing with Post-increment



The X-, Y-, or the Z-register is incremented after the operation. Operand address is the content of the X-, Y-, or the Z-register prior to incrementing.

tant Addressing Using PM Instruction

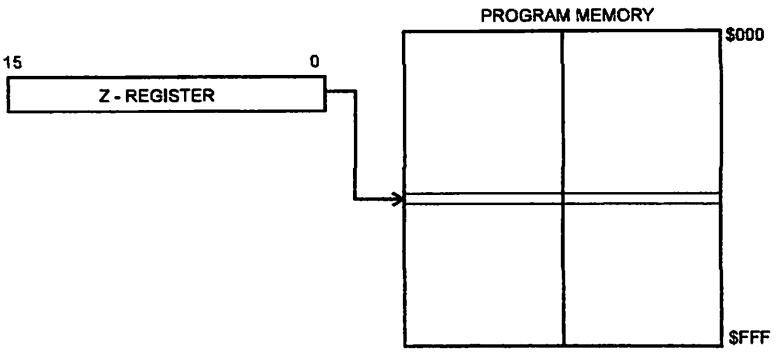
Figure 17. Code Memory Constant Addressing



Constant byte address is specified by the Z-register contents. The 15 MSBs select word address (0 - 4K), the LSB selects low byte if cleared (LSB = 0) or high byte if set (LSB = 1).

ect Program Addressing, and ICALL

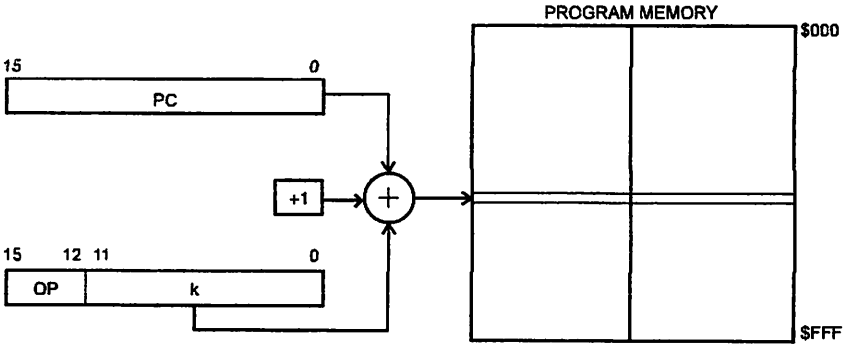
Figure 18. Indirect Program Memory Addressing



Program execution continues at address contained by the Z-register (i.e., the PC is loaded with the contents of the Z-register).

tive Program Addressing, P and RCALL

Figure 19. Relative Program Memory Addressing



Program execution continues at address PC + k + 1. The relative address k is from -2048 to 2047.

ROM Data Memory

The AT90S8535 contains 512 bytes of data EEPROM memory. It is organized as a separate data space, in which single bytes can be read and written. The EEPROM has an endurance of at least 100,000 write/erase cycles. The access between the EEPROM and the CPU is described on page 51 specifying the EEPROM address registers, the EEPROM data register and the EEPROM control register.

For the SPI data downloading, see page 99 for a detailed description.

ıory Access Times Instruction ːution Timing

This section describes the general access timing concepts for instruction execution and internal memory access.

The AVR CPU is driven by the System Clock Ø, directly generated from the external clock crystal for the chip. No internal clock division is used.

Figure 20 shows the parallel instruction fetches and instruction executions enabled by the Harvard architecture and the fast-access register file concept. This is the basic pipelining concept to obtain up to 1 MIPS per MHz with the corresponding unique results for functions per cost, functions per clocks and functions per power-unit.

Figure 20. The Parallel Instruction Fetches and Instruction Executions

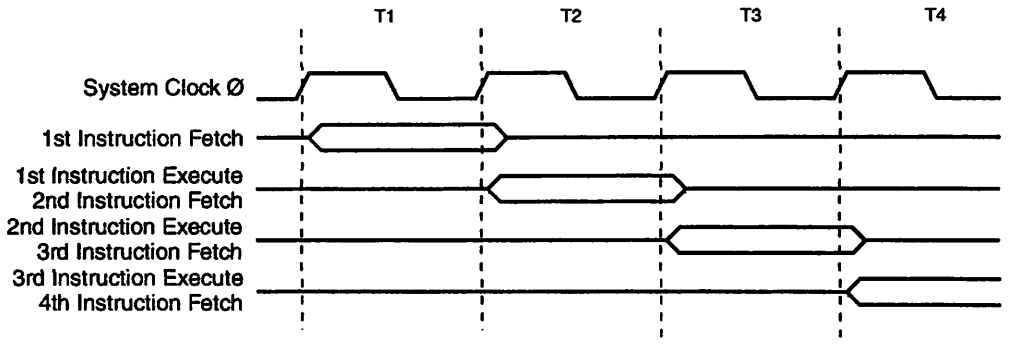
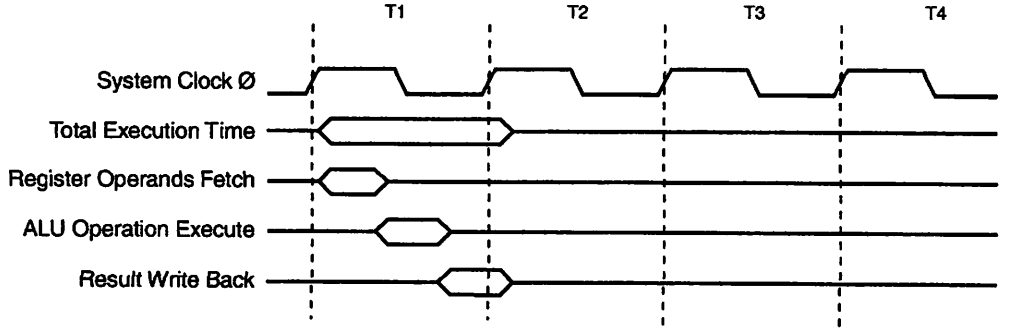


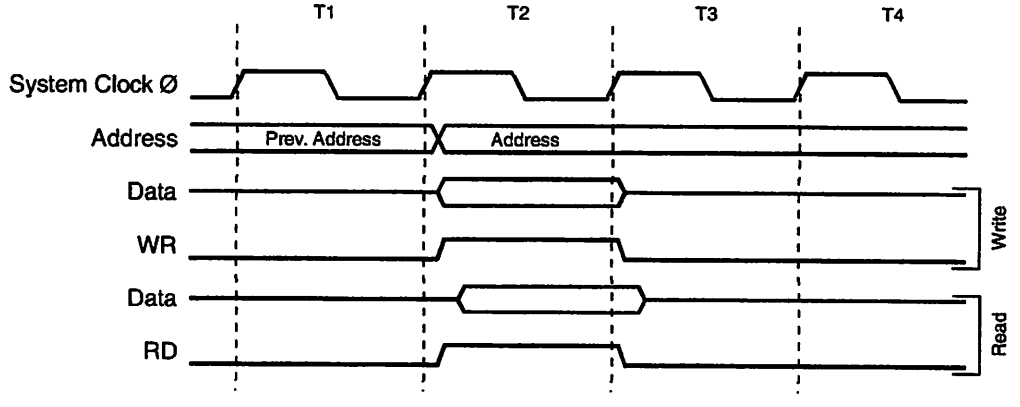
Figure 21 shows the internal timing concept for the register file. In a single clock cycle an ALU operation using two register operands is executed and the result is stored back to the destination register.

Figure 21. Single Cycle ALU Operation



The internal data SRAM access is performed in two System Clock cycles as described in Figure 22.

Figure 22. *On-chip Data SRAM Access Cycles*



Memory

The I/O space definition of the AT90S8535 is shown in Table 1.

Table 1. AT90S8535 I/O Space

I/O Address (SRAM Address)	Name	Function
$3F ($5F)	SREG	Status REGister
$3E ($5E)	SPH	Stack Pointer High
$3D ($5D)	SPL	Stack Pointer Low
$3B ($5B)	GIMSK	General Interrupt MaSK register
$3A ($5A)	GIFR	General Interrupt Flag Register
$39 ($59)	TIMSK	Timer/Counter Interrupt MaSK register
$38 ($58)	TIFR	Timer/Counter Interrupt Flag register
$35 ($55)	MCUCR	MCU general Control Register
$34 ($45)	MCUSR	MCU general Status Register
$33 ($53)	TCCR0	Timer/Counter0 Control Register
$32 ($52)	TCNT0	Timer/Counter0 (8-bit)
$2F ($4F)	TCCR1A	Timer/Counter1 Control Register A
$2E ($4E)	TCCR1B	Timer/Counter1 Control Register B
$2D ($4D)	TCNT1H	Timer/Counter1 High Byte
$2C ($4C)	TCNT1L	Timer/Counter1 Low Byte
$2B ($4B)	OCR1AH	Timer/Counter1 Output Compare Register A High Byte
$2A ($4A)	OCR1AL	Timer/Counter1 Output Compare Register A Low Byte
$29 ($49)	OCR1BH	Timer/Counter1 Output Compare Register B High Byte
$28 ($48)	OCR1BL	Timer/Counter1 Output Compare Register B Low Byte
$27 ($47)	ICR1H	T/C 1 Input Capture Register High Byte
$26 ($46)	ICR1L	T/C 1 Input Capture Register Low Byte
$25 ($45)	TCCR2	Timer/Counter2 Control Register
$24 ($44)	TCNT2	Timer/Counter2 (8-bit)
$23 ($43)	OCR2	Timer/Counter2 Output Compare Register
$22 ($42)	ASSR	Asynchronous Mode Status Register
$21 ($41)	WDTCR	Watchdog Timer Control Register
$1F ($3E)	EEARH	EEPROM Address Register High Byte
$1E ($3E)	EEARL	EEPROM Address Register Low Byte
$1D ($3D)	EEDR	EEPROM Data Register
$1C ($3C)	EECR	EEPROM Control Register
$1B ($3B)	PORTA	Data Register, Port A
$1A ($3A)	DDRA	Data Direction Register, Port A
$19 ($39)	PINA	Input Pins, Port A
$18 ($38)	PORTB	Data Register, Port B

Table 1. AT90S8535 I/O Space (Continued)

I/O Address (SRAM Address)	Name	Function
$17 ($37)	DDRB	Data Direction Register, Port B
$16 ($36)	PINB	Input Pins, Port B
$15 ($35)	PORTC	Data Register, Port C
$14 ($34)	DDRC	Data Direction Register, Port C
$13 ($33)	PINC	Input Pins, Port C
$12 ($32)	PORTD	Data Register, Port D
$11 ($31)	DDRD	Data Direction Register, Port D
$10 ($30)	PIND	Input Pins, Port D
$0F ($2F)	SPDR	SPI I/O Data Register
$0E ($2E)	SPSR	SPI Status Register
$0D ($2D)	SPCR	SPI Control Register
$0C ($2C)	UDR	UART I/O Data Register
$0B ($2B)	USR	UART Status Register
$0A ($2A)	UCR	UART Control Register
$09 ($29)	UBRR	UART Baud Rate Register
$08 ($28)	ACSR	Analog Comparator Control and Status Register
$07 ($27)	ADMUX	ADC Multiplexer Select Register
$06 ($26)	ADCSR	ADC Control and Status Register
$05 ($25)	ADCH	ADC Data Register High
$04 ($24)	ADCL	ADC Data Register Low

Note: Reserved and unused locations are not shown in the table.

All AT90S8535 I/Os and peripherals are placed in the I/O space. The I/O locations are accessed by the IN and OUT instructions transferring data between the 32 general-purpose working registers and the I/O space. I/O registers within the address range $00 - $1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Refer to the instruction set section for more details. When using the I/O specific commands IN and OUT, the I/O addresses $00 - $3F must be used. When addressing I/O registers as SRAM, $20 must be added to these addresses. All I/O register addresses throughout this document are shown with the SRAM address in parentheses.

For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

Some of the status flags are cleared by writing a logical "1" to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a "1" back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

The I/O and peripherals control registers are explained in the following sections.

is Register – SREG

The AVR Status Register (SREG) at I/O space location $3F ($5F) is defined as:

Bit	7	6	5	4	3	2	1	0	
$3F ($5F)	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – I: Global Interrupt Enable**

The global interrupt enable bit must be set (one) for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers. If the global interrupt enable register is cleared (zero), none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred and is set by the RETI instruction to enable subsequent interrupts.

- **Bit 6 – T: Bit Copy Storage**

The bit copy instructions BLD (Bit LoaD) and BST (Bit STore) use the T-bit as source and destination for the operated bit. A bit from a register in the register file can be copied into T by the BST instruction and a bit in T can be copied into a bit in a register in the register file by the BLD instruction.

- **Bit 5 – H: Half-carry Flag**

The half-carry flag H indicates a half-carry in some arithmetic operations. See the Instruction Set description for detailed information.

- **Bit 4 – S: Sign Bit, S = N ⊕ V**

The S-bit is always an exclusive or between the negative flag N and the two's complement overflow flag V. See the Instruction Set description for detailed information.

- **Bit 3 – V: Two's Complement Overflow Flag**

The two's complement overflow flag V supports two's complement arithmetics. See the Instruction Set description for detailed information.

- **Bit 2 – N: Negative Flag**

The negative flag N indicates a negative result from an arithmetical or logical operation. See the Instruction Set description for detailed information.

- **Bit 1 – Z: Zero Flag**

The zero flag Z indicates a zero result from an arithmetical or logic operation. See the Instruction Set description for detailed information.

- **Bit 0 – C: Carry Flag**

The carry flag C indicates a carry in an arithmetical or logical operation. See the Instruction Set description for detailed information.

Note that the Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt routine. This must be handled by software.

‹ Pointer – SP

The AT90S8535 Stack Pointer is implemented as two 8-bit registers in the I/O space locations $3E ($5E) and $3D ($5D). As the AT90S8535 data memory has $25F locations, 10 bits are used.

Bit	15	14	13	12	11	10	9	8	
$3E ($5E)	–	–	–	–	–	–	SP9	SP8	SPH
$3D ($5D)	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SPL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

The Stack Pointer points to the data SRAM stack area where the Subroutine and Interrupt stacks are located. This stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. The Stack Pointer must be set to point above $60. The Stack Pointer is decremented by 1 when data is pushed onto the stack with the PUSH instruction and it is decremented by 2 when an address is pushed onto the stack with subroutine calls and interrupts. The Stack Pointer is incremented by 1 when data is popped from the stack with the POP instruction and it is incremented by 2 when an address is popped from the stack with return from subroutine RET or return from interrupt RETI.

et and Interrupt dling

The AT90S8535 provides 16 different interrupt sources. These interrupts and the separate reset vector each have a separate program vector in the program memory space. All interrupts are assigned individual enable bits that must be set (one) together with the I-bit in the Status Register in order to enable the interrupt.

The lowest addresses in the program memory space are automatically defined as the Reset and Interrupt vectors. The complete list of vectors is shown in Table 2. The list also determines the priority levels of the different interrupts. The lower the address, the higher the priority level. RESET has the highest priority, and next is INT0 (the External Interrupt Request 0), etc.

Table 2. Reset and Interrupt Vectors

Vector No.	Program Address	Source	Interrupt Definition
1	$000	RESET	Hardware Pin, Power-on Reset and Watchdog Reset
2	$001	INT0	External Interrupt Request 0
3	$002	INT1	External Interrupt Request 1
4	$003	TIMER2 COMP	Timer/Counter2 Compare Match
5	$004	TIMER2 OVF	Timer/Counter2 Overflow
6	$005	TIMER1 CAPT	Timer/Counter1 Capture Event
7	$006	TIMER1 COMPA	Timer/Counter1 Compare Match A
8	$007	TIMER1 COMPB	Timer/Counter1 Compare Match B
9	$008	TIMER1 OVF	Timer/Counter1 Overflow
10	$009	TIMER0 OVF	Timer/Counter0 Overflow
11	$00A	SPI, STC	SPI Serial Transfer Complete
12	$00B	UART, RX	UART, Rx Complete

Table 2. Reset and Interrupt Vectors (Continued)

Vector No.	Program Address	Source	Interrupt Definition
13	$00C	UART, UDRE	UART Data Register Empty
14	$00D	UART, TX	UART, Tx Complete
15	$00E	ADC	ADC Conversion Complete
16	$00F	EE_RDY	EEPROM Ready
17	$010	ANA_COMP	Analog Comparator

The most typical and general program setup for the Reset and Interrupt vector addresses are:

```
Address Labels      Code              Comments
$000                rjmp    RESET       ; Reset Handler
$001                rjmp    EXT_INT0    ; IRQ0 Handler
$002                rjmp    EXT_INT1    ; IRQ1 Handler
$003                rjmp    TIM2_COMP   ; Timer2 Compare Handler
$004                rjmp    TIM2_OVF    ; Timer2 Overflow Handler
$005                rjmp    TIM1_CAPT   ; Timer1 Capture Handler
$006                rjmp    TIM1_COMPA  ; Timer1 CompareA Handler
$007                rjmp    TIM1_COMPB  ; Timer1 CompareB Handler
$008                rjmp    TIM1_OVF      ; Timer1 Overflow Handler
$009                rjmp    TIM0_OVF    ; Timer0 Overflow Handler
$00a                rjmp    SPI_STC;    ; SPI Transfer Complete Handler
$00b                rjmp    UART_RXC    ; UART RX Complete Handler
$00c                rjmp    UART_DRE    ; UDR Empty Handler
$00d                rjmp    UART_TXC    ; UART TX Complete Handler
$00e                rjmp    ADC         ; ADC Conversion Complete Interrupt
Handler
$00f                rjmp    EE_RDY      ; EEPROM Ready Handler
$010                rjmp    ANA_COMP    ; Analog Comparator Handler
$011    MAIN:       ldi     r16, high(RAMEND); Main program start
$012                out     SPH,r16
$013                ldi     r16, low(RAMEND) ;
$014                out     SPL,r16
$015            <instr> xxx
...       ...         ...       ...
```

t Sources

The AT90S8535 has three sources of reset:

- Power-on Reset. The MCU is reset when the supply voltage is below the Power-on Reset threshold (V_{POT}).
- External Reset. The MCU is reset when a low level is present on the $\overline{\text{RESET}}$ pin for more than 50 ns.
- Watchdog Reset. The MCU is reset when the Watchdog timer period expires and the Watchdog is enabled.

During reset, all I/O registers are set to their initial values and the program starts execution from address $000. The instruction placed in address $000 must be an RJMP (relative jump) instruction to the reset handling routine. If the program never enables an interrupt source, the interrupt vectors are not used and regular program code can be

placed at these locations. The circuit diagram in Figure 23 shows the reset logic. Table 3 defines the timing and electrical parameters of the reset circuitry.

Figure 23. Reset Logic

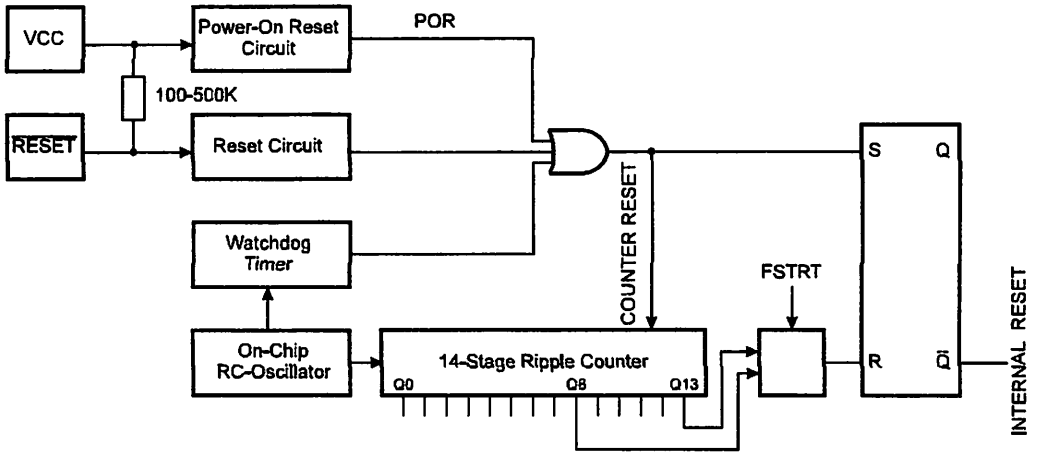


Table 3. Reset Characteristics (V_{CC} = 5.0V)

Symbol	Parameter	Min	Typ	Max	Units
V_{POT}[1]	Power-on Reset Threshold (rising)	1.0	1.4	1.8	V
	Power-on Reset Threshold (falling)	0.4	0.6	0.8	V
V_{RST}	$\overline{\text{RESET}}$ Pin Threshold Voltage		0.6 V_{CC}		V
t_{TOUT}	Reset Delay Time-out Period FSTRT Unprogrammed	11.0	16.0	21.0	ms
t_{TOUT}	Reset Delay Time-out Period FSTRT Programmed	1.0	1.1	1.2	ms

Note: 1. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling).

Table 4. Number of Watchdog Oscillator Cycles

FSTRT	Time-out at V_{CC} = 5V	Number of WDT Cycles
Programmed	1.1 ms	1K
Unprogrammed	*16.0 ms*	*16K*

r-on Reset

A Power-on Reset (POR) circuit ensures that the device is reset from power-on. As shown in Figure 23, an internal timer clocked from the Watchdog Timer oscillator prevents the MCU from starting until after a certain period after V_{CC} has reached the Power-on Threshold voltage (V_{POT}), regardless of the V_{CC} rise time (see Figure 24).

The user can select the start-up time according to typical oscillator start-up time. The number of WDT oscillator cycles is shown in Table 4. The frequency of the Watchdog oscillator is voltage-dependent as shown in "Typical Characteristics" on page 107.

If the built-in start-up delay is sufficient, $\overline{\text{RESET}}$ can be connected to V_{CC} directly or via an external pull-up resistor. By holding the pin low for a period after V_{CC} has been applied, the Power-on Reset period can be extended. Refer to Figure 25 for a timing example of this.

Figure 24. MCU Start-up, $\overline{\text{RESET}}$ Tied to V_{CC}.

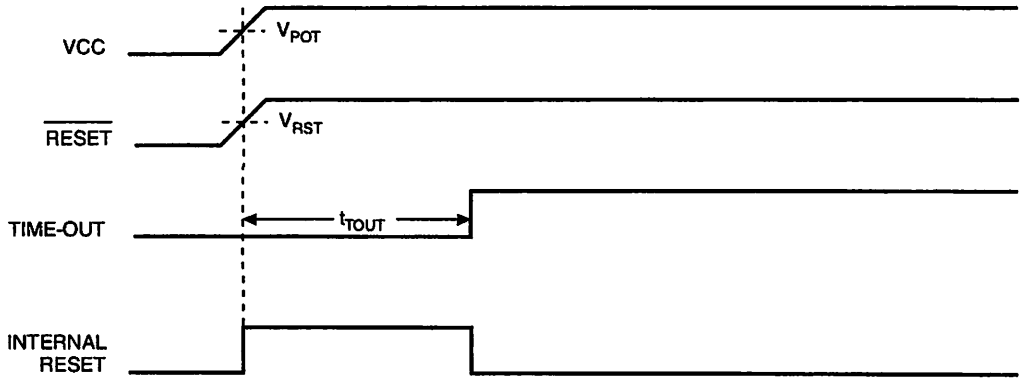
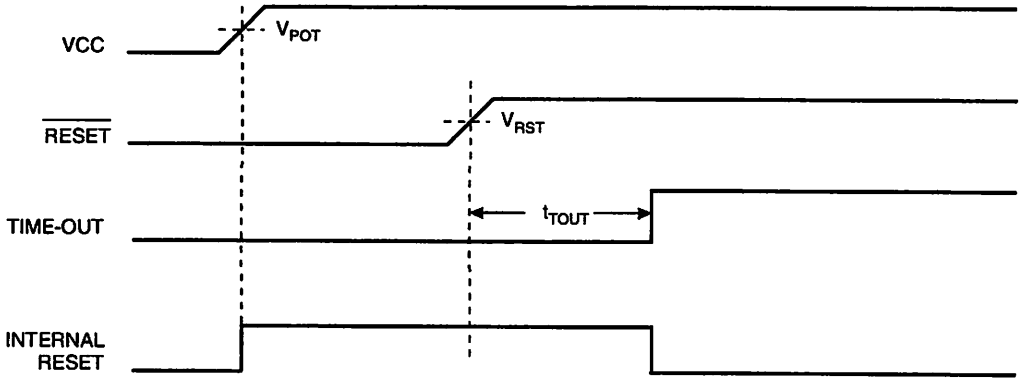


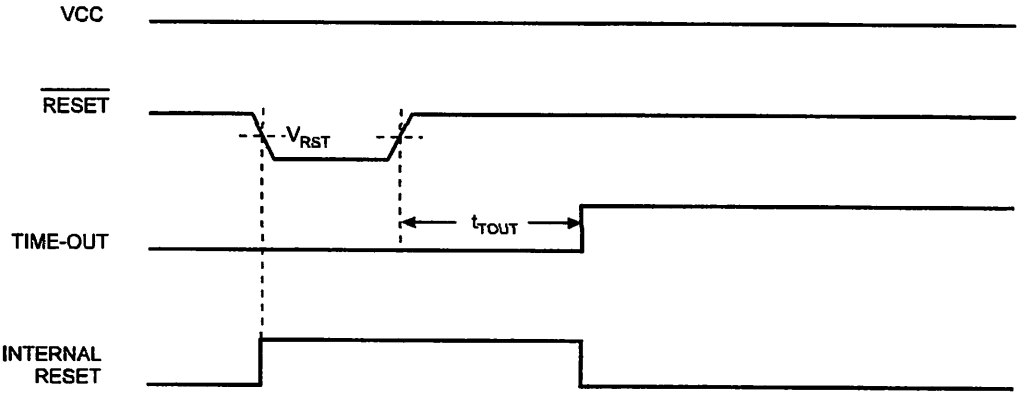
Figure 25. MCU Start-up, $\overline{\text{RESET}}$ Controlled Externally



nal Reset

An external reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset. When the applied signal reaches the Reset Threshold Voltage (V_{RST}) on its positive edge, the delay timer starts the MCU after the Time-out period t_{TOUT} has expired.

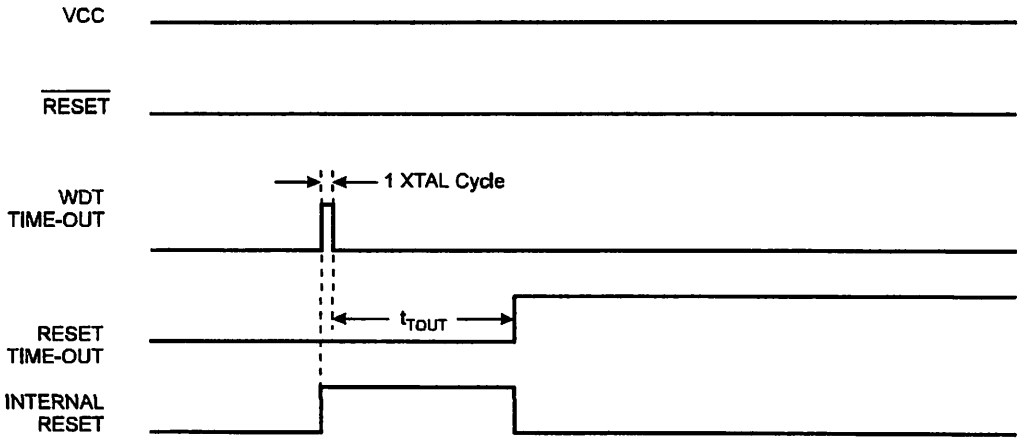
Figure 26. External Reset during Operation



hdog Reset

When the Watchdog times out, it will generate a short reset pulse of 1 XTAL cycle duration. On the falling edge of this pulse, the delay timer starts counting the Time-out period t_{TOUT}. Refer to page 49 for details on operation of the Watchdog.

Figure 27. Watchdog Reset during Operation



Status Register – SR

The MCU Status Register provides information on which reset source caused an MCU reset.

Bit	7	6	5	4	3	2	1	0	
$34 ($54)	–	–	–	–	–	–	EXTRF	PORF	MCUSR
Read/Write	R	R	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	See Bit Description		

- **Bits 7..2 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and always read as zero.

- **Bit 1 – EXTRF: External Reset Flag**

After a power-on reset, this bit is undefined (X). It can only be set by an External Reset. A Watchdog Reset will leave this bit unchanged. The bit is cleared by writing a logical zero to the bit.

- **Bit 0 – PORF: Power-on Reset Flag**

This bit is only set by a Power-on Reset. A Watchdog Reset or an External Reset will leave this bit unchanged. The bit is cleared by writing a logical zero to the bit.

To summarize, Table 5 shows the value of these two bits after the three modes of reset.

Table 5. PORF and EXTRF Values after Reset

Reset Source	EXTRF	PORF
Power-on Reset	Undefined	1
External Reset	1	Unchanged
Watchdog Reset	Unchanged	Unchanged

To make use of these bits to identify a reset condition, the user software should clear both the PORF and EXTRF bits as early as possible in the program. Checking the PORF and EXTRF values is done before the bits are cleared. If the bit is cleared before an External or Watchdog Reset occurs, the source of reset can be found by using Table 6.

Table 6. Reset Source Identification

EXTRF	PORF	Reset Source
0	0	Watchdog Reset
0	1	Power-on Reset
1	0	External Reset
1	1	Power-on Reset

rupt Handling

The AT90S8535 has two 8-bit interrupt mask control registers: GIMSK (General Interrupt Mask register) and TIMSK (Timer/Counter Interrupt Mask register).

When an interrupt occurs, the Global Interrupt Enable I-bit is cleared (zero) and all interrupts are disabled. The user software can set (one) the I-bit to enable nested interrupts. The I-bit is set (one) when a Return from Interrupt instruction (RETI) is executed.

When the Program Counter is vectored to the actual interrupt vector in order to execute the interrupt handling routine, hardware clears the corresponding flag that generated the interrupt. Some of the interrupt flags can also be cleared by writing a logical "1" to the flag bit position(s) to be cleared. If an interrupt condition occurs when the corresponding interrupt enable bit is cleared (zero), the interrupt flag will be set and remembered until the interrupt is enabled or the flag is cleared by software.

If one or more interrupt conditions occur when the global interrupt enable bit is cleared (zero), the corresponding interrupt flag(s) will be set and remembered until the global interrupt enable bit is set (one) and will be executed by order of priority.

Note that external level interrupt does not have a flag and will only be remembered for as long as the interrupt condition is active.

Note that the Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt routine. This must be handled by software.

ıral Interrupt Mask ster – GIMSK

Bit	7	6	5	4	3	2	1	0	
$3B ($5B)	INT1	INT0	–	–	–	–	–	–	GIMSK
Read/Write	R/W	R/W	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – INT1: External Interrupt Request 1 Enable**

When the INT1 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the external pin interrupt is enabled. The Interrupt Sense Control1 bits 1/0 (ISC11 and ISC10) in the MCU general Control Register (MCUCR) define whether the external interrupt is activated on rising or falling edge of the INT1 pin or level sensed. Activity on the pin will cause an interrupt request even if INT1 is configured as an output. The corresponding interrupt of External Interrupt Request 1 is executed from program memory address $002. *See also "External Interrupts."*

- **Bit 6 – INT0: External Interrupt Request 0 Enable**

When the INT0 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the external pin interrupt is enabled. The Interrupt Sense Control0 bits 1/0 (ISC01 and ISC00) in the MCU general Control Register (MCUCR) define whether the external interrupt is activated on rising or falling edge of the INT0 pin or level sensed. Activity on the pin will cause an interrupt request even if INT0 is configured as an output. The corre-

sponding interrupt of External Interrupt Request 0 is executed from program memory address $001. See also "External Interrupts."

- **Bits 5.0 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and always read as zero.

ral Interrupt Flag
ıter – GIFR

Bit	7	6	5	4	3	2	1	0	
$3A ($5A)	INTF1	INTF0	–	–	–	–	–	–	GIFR
Read/Write	R/W	R/W	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – INTF1: External Interrupt Flag1**

When an edge or logical change on the INT1 pin triggers an interrupt request, INTF1 becomes set (one). This flag is always cleared (0) when the pin is configured for low-level interrupts, as the state of a low-level interrupt can be determined by reading the PIN register.

If the I-bit in SREG and the INT1 bit in GIMSK are set (one), the MCU will jump to the interrupt address $002. For edge and logic change interrupts, this flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical "1" to it.

- **Bit 6 – INTF0: External Interrupt Flag0**

When an edge or logical change on the INT0 pin triggers an interrupt request, INTF0 becomes set (one). This flag is always cleared (0) when the pin is configured for low-level interrupts, as the state of a low-level interrupt can be determined by reading the PIN register.

If the I-bit in SREG and the INT0 bit in GIMSK are set (one), the MCU will jump to the interrupt address $001. For edge and logic change interrupts, this flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical "1" to it.

- **Bits 5..0 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and always read as zero.

'/Counter Interrupt Mask
ıter – TIMSK

Bit	7	6	5	4	3	2	1	0	
$39 ($59)	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	–	TOIE0	TIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – OCIE2: Timer/Counter2 Output Compare Match Interrupt Enable**

When the OCIE2 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter2 Compare Match interrupt is enabled. The corresponding interrupt (at vector $003) is executed if a compare match in Timer/Counter2 occurs (i.e., when the OCF2 bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

- **Bit 6 – TOIE2: Timer/Counter2 Overflow Interrupt Enable**

When the TOIE2 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter2 Overflow interrupt is enabled. The corresponding interrupt (at vector $004) is executed if an overflow in Timer/Counter2 occurs (i.e., when the TOV2 bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

- **Bit 5 – TICIE1: Timer/Counter1 Input Capture Interrupt Enable**

When the TICIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Input Capture Event Interrupt is enabled. The corresponding interrupt (at vector $005) is executed if a capture-triggering event occurs on pin 20, PD6 (ICP) (i.e., when the ICF1 bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

- **Bit 4 – OCIE1A: Timer/Counter1 Output CompareA Match Interrupt Enable**

When the OCIE1A bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 CompareA Match interrupt is enabled. The corresponding interrupt (at vector $006) is executed if a CompareA match in Timer/Counter1 occurs (i.e., when the OCF1A bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

- **Bit 3 – OCIE1B: Timer/Counter1 Output CompareB Match Interrupt Enable**

When the OCIE1B bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 CompareB Match interrupt is enabled. The corresponding interrupt (at vector $007) is executed if a CompareB match in Timer/Counter1 occurs (i.e., when the OCF1B bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

- **Bit 2 – TOIE1: Timer/Counter1 Overflow Interrupt Enable**

When the TOIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Overflow Interrupt is enabled. The corresponding interrupt (at vector $008) is executed if an overflow in Timer/Counter1 occurs (i.e., when the TOV1 bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

- **Bit 1 – Res: Reserved Bit**

This bit is a reserved bit in the AT90S8535 and always reads zero.

- ***Bit 0 – TOIE0: Timer/Counter0 Overflow Interrupt Enable***

When the TOIE0 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter0 Overflow Interrupt is enabled. The corresponding interrupt (at vector $009) is executed if an overflow in Timer/Counter0 occurs (i.e., when the TOV0 bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

r/Counter Interrupt Flag ıter – TIFR

Bit	7	6	5	4	3	2	1	0	
$38 ($58)	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	–	TOV0	TIFR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – OCF2: Output Compare Flag 2**

The OCF2 bit is set (one) when compare match occurs between the Timer/Counter2 and the data in OCR2 (Output Compare Register2). OCF2 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, OCF2 is cleared by writing a logical "1" to the flag. When the I-bit in SREG and OCIE2 (Timer/Counter2 Compare Match Interrupt Enable) and the OCF2 are set (one), the Timer/Counter2 Compare Match Interrupt is executed.

- **Bit 6 – TOV2: Timer/Counter2 Overflow Flag**

The TOV2 bit is set (one) when an overflow occurs in Timer/Counter2. TOV2 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, TOV2 is cleared by writing a logical "1" to the flag. When the SREG I-bit and TOIE2 (Timer/Counter2 Overflow Interrupt Enable) and TOV2 are set (one), the Timer/Counter2 Overflow Interrupt is executed. In up/down PWM mode, this bit is set when Timer/Counter1 advances from $0000.

- **Bit 5 – ICF1: Input Capture Flag 1**

The ICF1 bit is set (one) to flag an input capture event, indicating that the Timer/Counter1 value has been transferred to the Input Capture Register (ICR1). ICF1 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ICF1 is cleared by writing a logical "1" to the flag. When the SREG I-bit and TICIE1 (Timer/Counter1 Input Capture Interrupt Enable) and ICF1 are set (one), the Timer/Counter1 Capture Interrupt is executed.

- **Bit 4 – OCF1A: Output Compare Flag 1A**

The OCF1A bit is set (one) when compare match occurs between the Timer/Counter1 and the data in OCR1A (Output Compare Register 1A). OCF1A is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, OCF1A is cleared by writing a logical "1" to the flag. When the I-bit in SREG and OCIE1A (Timer/Counter1 Compare Match InterruptA Enable) and the OCF1A are set (one), the Timer/Counter1 Compare A Match Interrupt is executed.

- **Bit 3 – OCF1B: Output Compare Flag 1B**

The OCF1B bit is set (one) when compare match occurs between the Timer/Counter1 and the data in OCR1B (Output Compare Register 1B). OCF1B is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, OCF1B is cleared by writing a logical "1" to the flag. When the I-bit in SREG and OCIE1B (Timer/Counter1 Compare Match InterruptB Enable) and the OCF1B are set (one), the Timer/Counter1 Compare Match B Interrupt is executed.

- **Bit 2 – TOV1: Timer/Counter1 Overflow Flag**

The TOV1 is set (one) when an overflow occurs in Timer/Counter1. TOV1 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, TOV1 is cleared by writing a logical "1" to the flag. When the I-bit in SREG and TOIE1 (Timer/Counter1 Overflow Interrupt Enable) and TOV1 are set (one), the Timer/Counter1 Overflow Interrupt is executed. In up/down PWM mode, this bit is set when Timer/Counter1 advances from $0000.

- **Bit 1 – Res: Reserved Bit**

This bit is a reserved bit in the AT90S8535 and always reads zero.

- **Bit 0 – TOV0: Timer/Counter0 Overflow Flag**

The bit TOV0 is set (one) when an overflow occurs in Timer/Counter0. TOV0 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, TOV0 is cleared by writing a logical "1" to the flag. When the SREG I-bit and TOIE0 (Timer/Counter0 Overflow Interrupt Enable) and TOV0 are set (one), the Timer/Counter0 Overflow Interrupt is executed. In up/down PWM mode, this bit is set when Timer/Counter1 advances from $0000.

nal Interrupts

The external interrupts are triggered by the INT1 and INT0 pins. Observe that, if enabled, the interrupts will trigger even if the INT0/INT1 pins are configured as outputs. This feature provides a way of generating a software interrupt. The external interrupts can be triggered by a falling or rising edge or a low level. This is set up as indicated in the specification for the MCU Control Register (MCUCR). When the external interrupt is enabled and is configured as level-triggered, the interrupt will trigger as long as the pin is held low.

The external interrupts are set up as described in the specification for the MCU Control Register (MCUCR).

'upt Response Time

The interrupt execution response for all the enabled AVR interrupts is four clock cycles minimum. Four clock cycles after the interrupt flag has been set, the program vector address for the actual interrupt handling routine is executed. During this 4-clock-cycle period, the Program Counter (2 bytes) is pushed onto the stack and the Stack Pointer is decremented by 2. The vector is normally a relative jump to the interrupt routine and this jump takes two clock cycles. If an interrupt occurs during execution of a multi-cycle instruction, this instruction is completed before the interrupt is served.

A return from an interrupt handling routine (same as for a subroutine call routine) takes four clock cycles. During these four clock cycles, the Program Counter (2 bytes) is popped back from the stack, the Stack Pointer is incremented by 2 and the I-flag in SREG is set. When the AVR exits from an interrupt, it will always return to the main program and execute one more instruction before any pending interrupt is served.

Control Register – CR

The MCU Control Register contains control bits for general MCU functions.

Bit	7	6	5	4	3	2	1	0	
$35 ($55)	–	SE	SM1	SM0	ISC11	ISC10	ISC01	ISC00	MCUCR
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- ***Bit 7 – Res: Reserved Bit***

This bit is a reserved bit in the AT90S8535 and always reads zero.

- **Bit 6 – SE: Sleep Enable**

The SE bit must be set (one) to make the MCU enter the Sleep Mode when the SLEEP instruction is executed. To avoid the MCU entering the Sleep Mode unless it is the programmer's purpose, it is recommended to set the Sleep Enable (SE) bit just before the execution of the SLEEP instruction.

- **Bits 5, 4 – SM1/SM0: Sleep Mode Select Bits 1 and 0**

These bits select between the three available sleep modes as shown in Table 7.

Table 7. Sleep Mode Select

SM1	SM0	Sleep Mode
0	0	Idle
0	1	Reserved
1	0	Power-down
1	1	Power Save

- **Bits 3, 2 – ISC11, ISC10: Interrupt Sense Control 1 Bits 1 and 0**

The External Interrupt 1 is activated by the external pin INT1 if the SREG I-flag and the corresponding interrupt mask in the GIMSK is set. The level and edges on the external INT1 pin that activate the interrupt are defined in Table 8.

Table 8. Interrupt 1 Sense Control

ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Reserved
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.

The value on the INT pin is sampled before detecting edges. If edge interrupt is selected, pulses that last longer than one CPU clock period will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt. If low-level interrupt is selected, the low level must be held until the completion of the currently executing instruction to generate an interrupt. If enabled, a level-triggered interrupt will generate an interrupt request as long as the pin is held low.

- **Bit 1, 0 – ISC01, ISC00: Interrupt Sense Control 0 Bits 1 and 0**

The External Interrupt 0 is activated by the external pin INT0 if the SREG I-flag and the corresponding interrupt mask is set. The level and edges on the external INT0 pin that activate the interrupt are defined in Table 9.

Table 9. Interrupt 0 Sense Control

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Reserved
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

The value on the INT pin is sampled before detecting edges. If edge interrupt is selected, pulses that last longer than one CPU clock period will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt. If low-level interrupt is selected, the low level must be held until the completion of the currently executing instruction to generate an interrupt. If enabled, a level-triggered interrupt will generate an interrupt request as long as the pin is held low.

ıp Modes

To enter any of the three sleep modes, the SE bit in MCUCR must be set (one) and a SLEEP instruction must be executed. The SM0 and SM1 bits in the MCUCR register select which sleep mode (Idle, Power-down or Power Save) will be activated by the SLEEP instruction. See Table 7.

If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU wakes up, executes the interrupt routine and resumes execution from the instruction following SLEEP. The contents of the register file, SRAM and I/O memory are unaltered. If a reset occurs during Sleep Mode, the MCU wakes up and executes from the Reset vector.

Mode

When the SM1/SM0 bits are set to 00, the SLEEP instruction makes the MCU enter the Idle Mode, stopping the CPU but allowing SPI, UARTs, Analog Comparator, ADC, Timer/Counters, Watchdog and the interrupt system to continue operating. This enables the MCU to wake up from external triggered interrupts as well as internal ones like the Timer Overflow and UART Receive Complete interrupts. If wake-up from the Analog

Comparator Interrupt is not required, the Analog Comparator can be powered down by setting the ACD-bit in the Analog Comparator Control and Status Register (ACSR). This will reduce power consumption in Idle Mode. When the MCU wakes up from Idle Mode, the CPU starts program execution immediately.

ɪr-down Mode

When the SM1/SM0 bits are set to 10, the SLEEP instruction makes the MCU enter the *Power-down mode. In this mode, the external oscillator is stopped while the external* interrupts and the Watchdog (if enabled) continue operating. Only an external reset, a Watchdog reset (if enabled) or an external level interrupt can wake up the MCU.

Note that when a level-triggered interrupt is used for wake-up from power-down, the low level must be held for a time longer than the reset delay Time-out period t_{TOUT}.

When waking up from Power-down mode, a delay from the wake-up condition occurs until the wake-up becomes effective. This allows the clock to restart and become stable after having been stopped. The wake-up period is equal to the reset period, as shown in Table 3 on page 22.

If the wake-up condition disappears before the MCU wakes up and starts to execute, e.g., a low-level on is not held long enough, the interrupt causing the wake-up will not be executed.

ɪr Save Mode

When the SM1/SM0 bits are 11, the SLEEP instruction makes the MCU enter the Power Save Mode. This mode is identical to Power-down, with one exception: If Timer/Counter2 is clocked asynchronously, i.e., the AS2 bit in ASSR is set, Timer/Counter2 will run during sleep. In addition to the power-down wake-up sources, the device can also wake up from either a Timer Overflow or Output Compare event from Timer/Counter2 if the corresponding Timer/Counter2 interrupt enable bits are set in *TIMSK and the global interrupt enable bit in* SREG *is set.*

When waking up from Power Save Mode by an external interrupt, two instruction cycles are executed before the interrupt flags are updated. When waking up by the asynchronous timer, three instruction cycles are executed before the flags are updated. During these cycles, the processor executes instructions, but the interrupt condition is not readable and the interrupt routine has not started yet.

When waking up from Power Save Mode by an asynchronous timer interrupt, the part will wake up even if global interrupts are disabled. To ensure that the part executes the interrupt routine when waking up, also set the global interrupt enable bit in SREG.

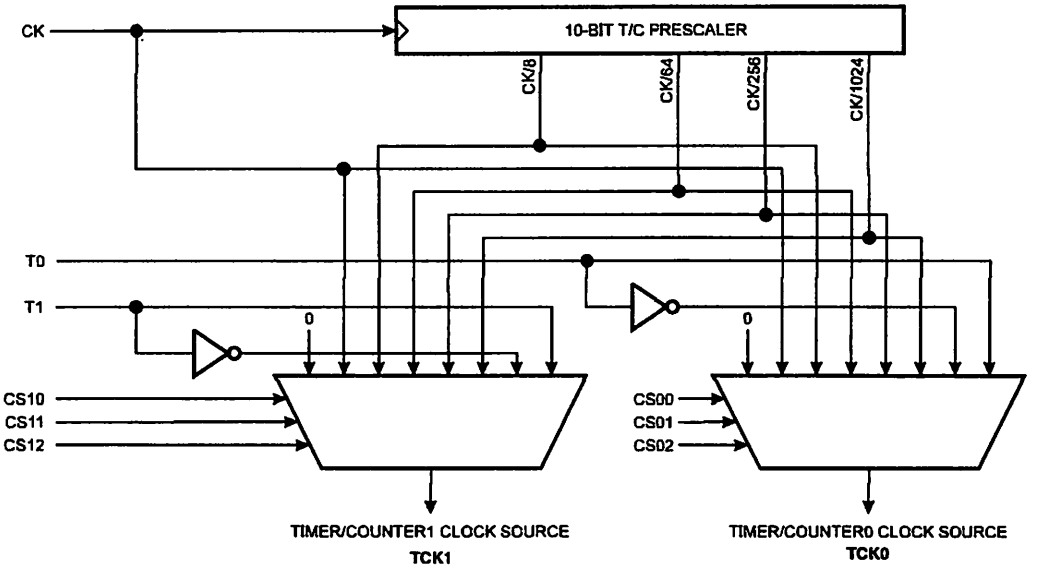
If the asynchronous timer is not clocked asynchronously, Power-down mode is recommended instead of Power Save Mode because the contents of the registers in the asynchronous timer should be considered undefined after wake-up in Power Save Mode, even if AS2 is 0.

er/Counters

The AT90S8535 provides three general-purpose Timer/Counters – two 8-bit T/Cs and one 16-bit T/C. Timer/Counter2 can optionally be asynchronously clocked from an external oscillator. This oscillator is optimized for use with a 32.768 kHz watch crystal, enabling use of Timer/Counter2 as a Real-time Clock (RTC). Timer/Counters 0 and 1 have individual prescaling selection from the same 10-bit prescaling timer. Timer/Counter2 has its own prescaler. These Timer/Counters can either be used as a timer with an internal clock time base or as a counter with an external pin connection that triggers the counting.

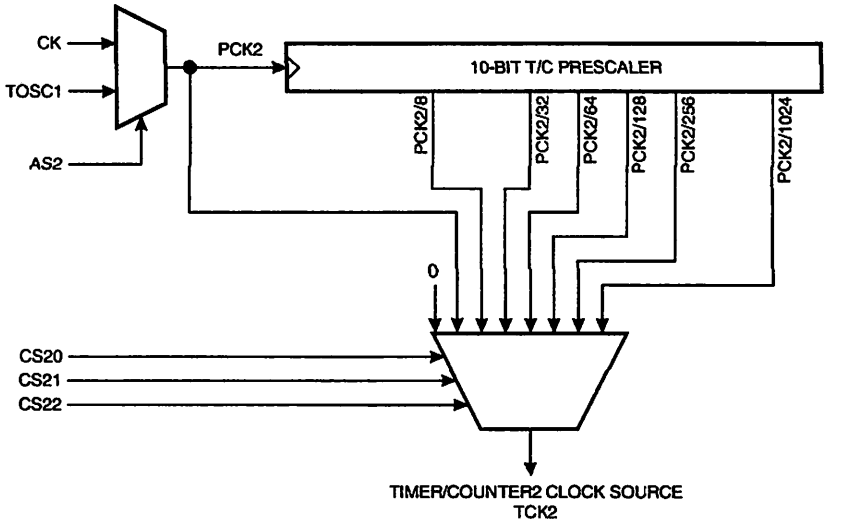
er/Counter scalers

Figure 28. Prescaler for Timer/Counter0 and 1



For Timer/Counters 0 and 1, the four different prescaled selections are: CK/8, CK/64, CK/256 and CK/1024, where CK is the oscillator clock. For the two Timer/Counters 0 and 1, CK, external source and stop can also be selected as clock sources.

Figure 29. Timer/Counter2 Prescaler



The clock source for Timer/Counter2 prescaler is named PCK2. PCK2 is by default connected to the main system clock (CK). By setting the AS2 bit in ASSR, Timer/Counter2 prescaler is asynchronously clocked from the PC6(TOSC1) pin. This enables use of Timer/Counter2 as a Real-time Clock (RTC). When AS2 is set, pins PC6(TOSC1) and PC7(TOSC2) are disconnected from Port C. A crystal can then be connected between the PC6(TOSC1) and PC7(TOSC2) pins to serve as an independent clock source for Timer/Counter2. The oscillator is optimized for use with a 32.768 kHz crystal. Applying an external clock source to TOSC1 is not recommended.

t Timer/Counter0

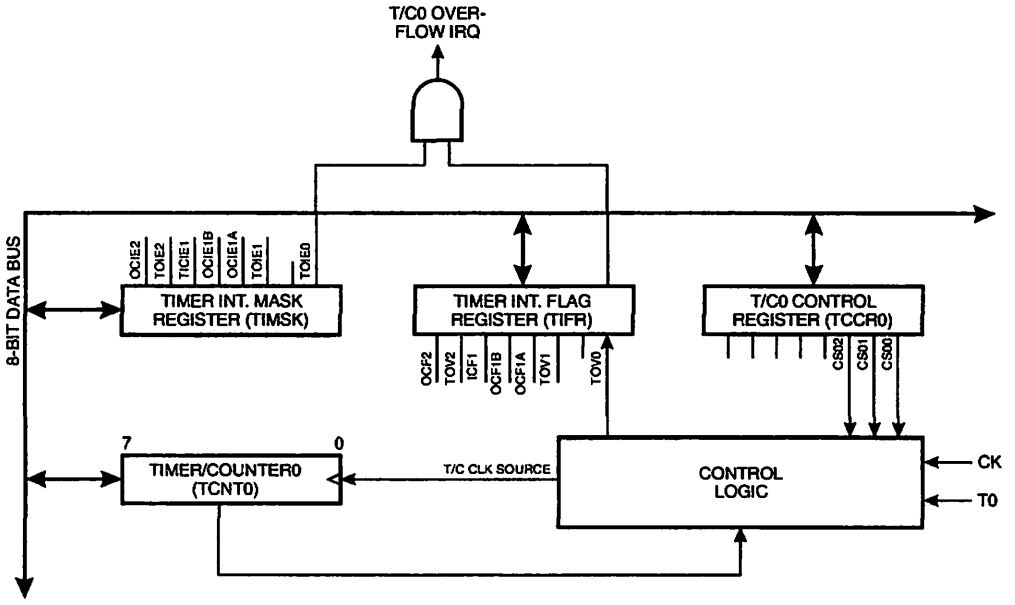
Figure 30 shows the block diagram for Timer/Counter0.

The 8-bit Timer/Counter0 can select clock source from CK, prescaled CK or an external pin. In addition, it can be stopped as described in the specification for the Timer/Counter0 Control Register (TCCR0). The overflow status flag is found in the Timer/Counter Interrupt Flag Register (TIFR). Control signals are found in the Timer/Counter0 Control Register (TCCR0). The interrupt enable/disable settings for Timer/Counter0 are found in the Timer/Counter Interrupt Mask Register (TIMSK).

When Timer/Counter0 is externally clocked, the external signal is synchronized with the oscillator frequency of the CPU. To assure proper sampling of the external clock, the minimum time between two external clock transitions must be at least one internal CPU clock period. The external clock signal is sampled on the rising edge of the internal CPU clock.

The 8-bit Timer/Counter0 features both a high-resolution and a high-accuracy usage with the lower prescaling opportunities. Similarly, the high prescaling opportunities make the Timer/Counter0 useful for lower speed functions or exact timing functions with infrequent actions.

Figure 30. Timer/Counter0 Block Diagram



r/Counter0 Control ster – TCCR0

Bit	7	6	5	4	3	2	1	0	
$33 ($53)	–	–	–	–	–	CS02	CS01	CS00	TCCR0
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7..3 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and always read zero.

- **Bits 2, 1, 0 – CS02, CS01, CS00: Clock Select0, Bits 2, 1 and 0**

The Clock Select0 bits 2,1 and 0 define the prescaling source of Timer/Counter0.

Table 10. Clock 0 Prescale Select

CS02	CS01	CS00	Description
0	0	0	Stop, Timer/Counter0 is stopped.
0	0	1	CK
0	1	0	CK/8
0	1	1	CK/64
1	0	0	CK/256
1	0	1	CK/1024
1	1	0	External Pin T0, falling edge
1	1	1	External Pin T0, rising edge

The Stop condition provides a Timer Enable/Disable function. The prescaled CK modes are scaled directly from the CK oscillator clock. If the external pin modes are used, the corresponding setup must be performed in the actual Data Direction Control Register (cleared to zero gives an input pin).

r Counter 0 – TCNT0

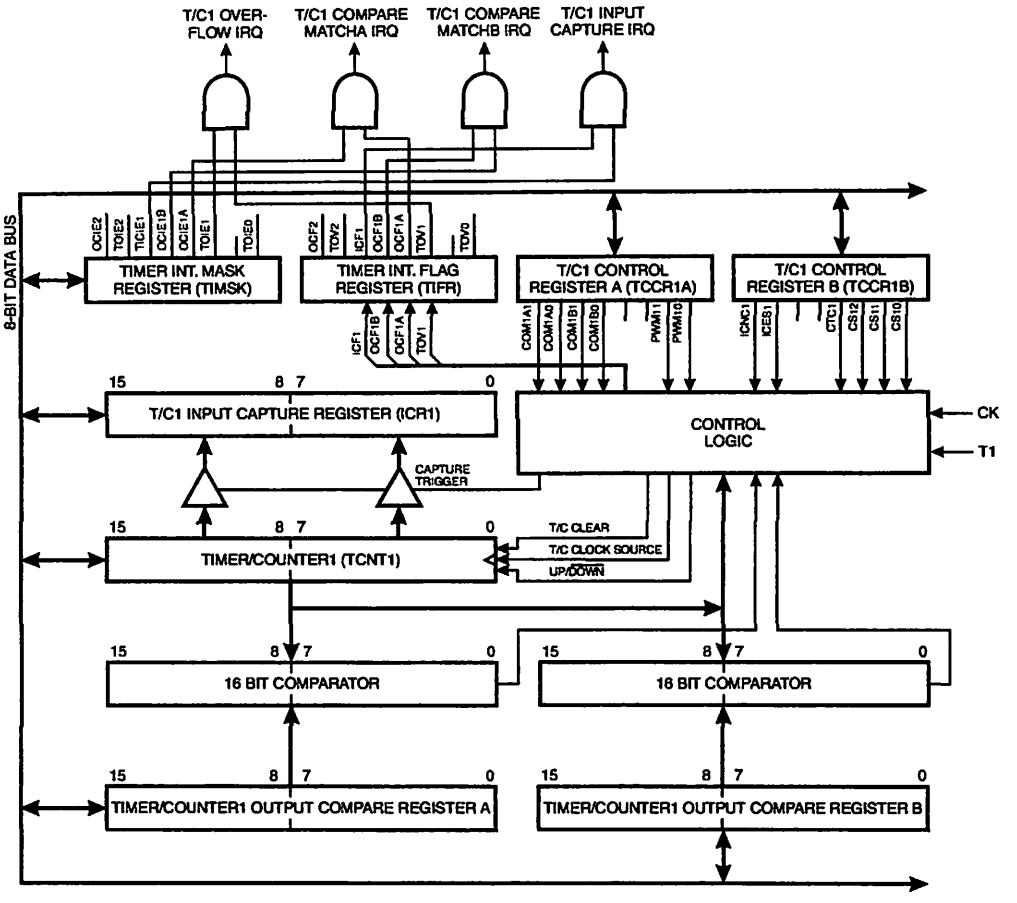
Bit	7	6	5	4	3	2	1	0	
$32 ($52)	MSB							LSB	TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Timer/Counter0 is realized as an up-counter with read and write access. If the Timer/Counter0 is written and a clock source is present, the Timer/Counter0 continues counting in the clock cycle following the write operation.

it Timer/Counter1

Figure 31 shows the block diagram for Timer/Counter1.

Figure 31. Timer/Counter1 Block Diagram



The 16-bit Timer/Counter1 can select clock source from CK, prescaled CK or an external pin. In addition, it can be stopped as described in the specification for the Timer/Counter1 Control Registers (TCCR1A and TCCR1B). The different status flags (Overflow, Compare Match and Capture Event) and control signals are found in the Timer/Counter1 Control Registers (TCCR1A and TCCR1B). The interrupt enable/disable settings for Timer/Counter1 are found in the Timer/Counter Interrupt Mask Register (TIMSK).

When Timer/Counter1 is externally clocked, the external signal is synchronized with the oscillator frequency of the CPU. To assure proper sampling of the external clock, the minimum time between two external clock transitions must be at least one internal CPU clock period. The external clock signal is sampled on the rising edge of the internal CPU clock.

The 16-bit Timer/Counter1 features both a high-resolution and a high-accuracy usage with the lower prescaling opportunities. Similarly, the high prescaling opportunities makes the Timer/Counter1 useful for lower speed functions or exact timing functions with infrequent actions.

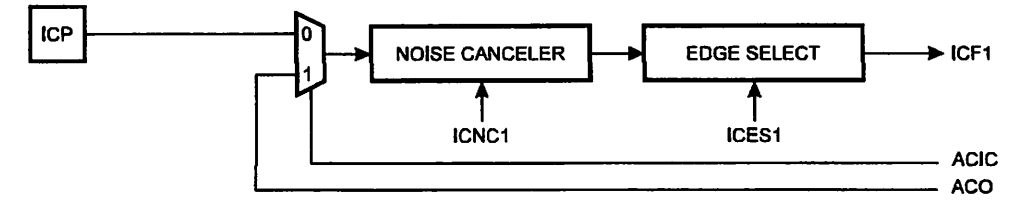
The Timer/Counter1 supports two Output Compare functions using the Output Compare Register 1A and B (OCR1A and OCR1B) as the data sources to be compared to the Timer/Counter1 contents. The Output Compare functions include optional clearing of

the counter on compareA match and actions on the Output Compare pins on both compare matches.

Timer/Counter1 can also be used as an 8-, 9- or 10-bit Pulse Width Modulator. In this mode the counter and the OCR1A/OCR1B registers serve as a dual glitch-free standalone PWM with centered pulses. Refer to page 40 for a detailed description of this function.

The Input Capture function of Timer/Counter1 provides a capture of the Timer/Counter1 contents to the Input Capture Register (ICR1), triggered by an external event on the Input Capture Pin (ICP). The actual capture event settings are defined by the Timer/Counter1 Control Register (TCCR1B). In addition, the Analog Comparator can be set to trigger the input capture. Refer to "Analog Comparator" on page 66 for details on this. The ICP pin logic is shown in Figure 32.

Figure 32. ICP Pin Schematic Diagram



ACIC: COMPARATOR IC ENABLE
ACO: COMPARATOR OUTPUT

If the Noise Canceler function is enabled, the actual trigger condition for the capture event is monitored over four samples and all four must be equal to activate the capture flag. The input pin signal is sampled at XTAL clock frequency.

ır/Counter1 Control ster A – TCCR1A

Bit	7	6	5	4	3	2	1	0	
$2F ($4F)	COM1A1	COM1A0	COM1B1	COM1B0	–	–	PWM11	PWM10	TCCR1A
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7, 6 – COM1A1, COM1A0: Compare Output Mode1A, Bits 1 and 0**

The COM1A1 and COM1A0 control bits determine any output pin action following a compare match in Timer/Counter1. Any output pin actions affect pin OC1A (Output CompareA pin 1). This is an alternative function to an I/O port and the corresponding direction control bit must be set (one) to control an output pin. The control configuration is shown in Table 11.

- **Bits 5, 4 – COM1B1, COM1B0: Compare Output Mode1B, Bits 1 and 0**

The COM1B1 and COM1B0 control bits determine any output pin action following a compare match in Timer/Counter1. Any output pin actions affect pin OC1B (Output CompareB). This is an alternative function to an I/O port and the corresponding direction control bit must be set (one) to control an output pin. The control configuration is given in Table 11.

Table 11. Compare 1 Mode Select

COM1X1	COM1X0	Description
0	0	Timer/Counter1 disconnected from output pin OC1X
0	1	Toggle the OC1X output line.
1	0	Clear the OC1X output line (to zero).
1	1	Set the OC1X output line (to one).

Note: X = A or B.

In PWM mode, these bits have a different function. Refer to Table 15 for a detailed description. When changing the COM1X1/COM1X0 bits, Output Compare Interrupt 1 must be disabled by clearing their Interrupt Enable bits in the TIMSK Register. Otherwise an interrupt can occur when the bits are changed.

- **Bits 3..2 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and always read zero.

- **Bits 1..0 – PWM11, PWM10: Pulse Width Modulator Select Bits**

These bits select PWM operation of Timer/Counter1 as specified in Table 12. This mode is described on page 40.

Table 12. PWM Mode Select

PWM11	PWM10	Description
0	0	PWM operation of Timer/Counter1 is disabled
0	1	Timer/Counter1 is an 8-bit PWM
1	0	Timer/Counter1 is a 9-bit PWM
1	1	Timer/Counter1 is a 10-bit PWM

r/Counter1 Control ster B – TCCR1B

Bit	7	6	5	4	3	2	1	0	
$2E ($4E)	ICNC1	ICES1	–	–	CTC1	CS12	CS11	CS10	TCCR1B
Read/Write	R/W	R/W	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – ICNC1: Input Capture1 Noise Canceler (4 CKs)**

When the ICNC1 bit is cleared (zero), the Input Capture Trigger Noise Canceler function is disabled. The input capture is triggered at the first rising/falling edge sampled on the ICP (input capture pin) as specified. When the ICNC1 bit is set (one), four successive samples are measured on the ICP (input capture pin), and all samples must be high/low according to the input capture trigger specification in the ICES1 bit. The actual sampling frequency is XTAL clock frequency.

- **Bit 6 – ICES1: Input Capture1 Edge Select**

While the ICES1 bit is cleared (zero), the Timer/Counter1 contents are transferred to the Input Capture Register (ICR1) on the falling edge of the input capture pin (ICP). While the ICES1 bit is set (one), the Timer/Counter1 contents are transferred to the Input Capture Register (ICR1) on the rising edge of the input capture pin (ICP).

- **Bits 5, 4 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and always read zero.

- **Bit 3 – CTC1: Clear Timer/Counter1 on Compare Match**

When the CTC1 control bit is set (one), the Timer/Counter1 is reset to $0000 in the clock cycle after a compareA match. If the CTC1 control bit is cleared, Timer/Counter1 continues counting and is unaffected by a compare match. Since the compare match is detected in the CPU clock cycle following the match, this function will behave differently when a prescaling higher than 1 is used for the timer. When a prescaling of 1 is used and the compareA register is set to C, the timer will count as follows if CTC1 is set:

... | C-2 | C-1 | C | 0 | 1 |...

When the prescaler is set to divide by 8, the timer will count like this:

... | C-2, C-2, C-2, C-2, C-2, C-2, C-2, C-2 | C-1, C-1, C-1, C-1, C-1, C-1, C-1, C-1 | C, 0, 0, 0, 0, 0, 0, 0 |1,1,1,1,1,1,1,1|...

In PWM mode, this bit has no effect.

- **Bits 2, 1, 0 – CS12, CS11, CS10: Clock Select1, Bits 2, 1 and 0**

The Clock Select1 bits 2, 1 and 0 define the prescaling source of Timer/Counter1.

Table 13. Clock 1 Prescale Select

CS12	CS11	CS10	Description
0	0	0	Stop, the Timer/Counter1 is stopped.
0	0	1	CK
0	1	0	CK/8
0	1	1	CK/64
1	0	0	CK/256
1	0	1	CK/1024
1	1	0	External Pin T1, falling edge
1	1	1	External Pin T1, rising edge

The Stop condition provides a Timer Enable/Disable function. The CK down divided modes are scaled directly from the CK oscillator clock. If the external pin modes are used, the corresponding setup must be performed in the actual Direction Control Register (cleared to zero gives an input pin).

r/Counter1 – TCNT1H
TCNT1L

Bit	15	14	13	12	11	10	9	8	
$2D ($4D)	MSB								TCNT1H
$2C ($4C)								LSB	TCNT1L
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

This 16-bit register contains the prescaled value of the 16-bit Timer/Counter1. To ensure that both the high and low bytes are read and written simultaneously when the CPU accesses these registers, the access is performed using an 8-bit temporary register (TEMP). This temporary register is also used when accessing OCR1A, OCR1B and ICR1. *If the main program and also interrupt routines perform access to registers using*

TEMP, interrupts must be disabled during access from the main program (and from interrupt routines if interrupts are allowed from within interrupt routines).

- TCNT1 Timer/Counter1 Write:
  When the CPU writes to the high byte TCNT1H, the written data is placed in the TEMP register. Next, when the CPU writes the low byte TCNT1L, this byte of data is combined with the byte data in the TEMP register, and all 16 bits are written to the TCNT1 Timer/Counter1 register simultaneously. Consequently, the high byte TCNT1H must be accessed first for a full 16-bit register write operation.
- TCNT1 Timer/Counter1 Read:
  When the CPU reads the low byte TCNT1L, the data of the low byte TCNT1L is sent to the CPU and the data of the high byte TCNT1H is placed in the TEMP register. When the CPU reads the data in the high byte TCNT1H, the CPU receives the data *in the TEMP register. Consequently, the low byte TCNT1L must be accessed first for* a full 16-bit register read operation.

The Timer/Counter1 is realized as an up or up/down (in PWM mode) counter with read and write access. If Timer/Counter1 is written to and a clock source is selected, the Timer/Counter1 continues counting in the timer clock cycle after it is preset with the written value.

r/Counter1 Output pare Register – OCR1AH OCR1AL

Bit	15	14	13	12	11	10	9	8	
$2B ($4B)	MSB								OCR1AH
$2A ($4A)								LSB	OCR1AL
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

r/Counter1 Output pare Register – OCR1BH OCR1BL

Bit	15	14	13	12	11	10	9	8	
$29 ($49)	MSB								OCR1BH
$28 ($48)								LSB	OCR1BL
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

The output compare registers are 16-bit read/write registers.

The Timer/Counter1 Output Compare registers contain the data to be continuously compared with Timer/Counter1. Actions on compare matches are specified in the Timer/Counter1 Control and Status registers. A compare match only occurs if Timer/Counter1 counts to the OCR value. A software write that sets TCNT1 and OCR1A or OCR1B to the same value does not generate a compare match.

A compare match will set the compare interrupt flag in the CPU clock cycle following the compare event.

Since the Output Compare Registers (OCR1A and OCR1B) are 16-bit registers, a temporary register (TEMP) is used when OCR1A/B are written to ensure that both bytes are updated simultaneously. When the CPU writes the high byte, OCR1AH or OCR1BH, the data is temporarily stored in the TEMP register. When the CPU writes the low byte,

OCR1AL or OCR1BL, the TEMP register is simultaneously written to OCR1AH or OCR1BH. Consequently, the high byte OCR1AH or OCR1BH must be written first for a full 16-bit register write operation.

The TEMP register is also used when accessing TCNT1 and ICR1. If the main program and interrupt routines perform access to registers using TEMP, interrupts must be disabled during access from the main program.

r/Counter1 Input Capture ster – ICR1H AND ICR1L

Bit	15	14	13	12	11	10	9	8	
$27 ($47)	MSB								ICR1H
$26 ($46)								LSB	ICR1L
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

The Input Capture Register is a 16-bit read-only register.

When the rising or falling edge (according to the input capture edge setting [ICES1]) of the signal at the input capture pin (ICP) is detected, the current value of the Timer/Counter1 is transferred to the Input Capture Register (ICR1). At the same time, the input capture flag (ICF1) is set (one).

Since the Input Capture Register (ICR1) is a 16-bit register, a temporary register (TEMP) is used when ICR1 is read to ensure that both bytes are read simultaneously. When the CPU reads the low byte ICR1L, the data is sent to the CPU and the data of the high byte ICR1H is placed in the TEMP register. When the CPU reads the data in the high byte ICR1H, the CPU receives the data in the TEMP register. Consequently, the low-byte ICR1L must be accessed first for a full 16-bit register read operation.

The TEMP register is also used when accessing TCNT1, OCR1A and OCR1B. If the main program and interrupt routines perform access to registers using TEMP, interrupts must be disabled during access from the main program.

r/Counter1 In PWM Mode

When the PWM mode is selected, Timer/Counter1, the Output Compare Register1A (OCR1A) and the Output Compare Register1B (OCR1B) form a dual 8-, 9- or 10-bit, free-running, glitch-free and phase-correct PWM with outputs on the PD5(OC1A) and PD4(OC1B) pins. Timer/Counter1 acts as an up/down counter, counting up from $0000 to TOP (see Table 14), where it turns and counts down again to zero before the cycle is repeated. When the counter value matches the contents of the 10 least significant bits of OCR1A or OCR1B, the PD5(OC1A)/PD4(OC1B) pins are set or cleared according to the settings of the COM1A1/COM1A0 or COM1B1/COM1B0 bits in the Timer/Counter1 Control Register (TCCR1A). Refer to Table 15 for details.

Table 14. Timer TOP Values and PWM Frequency

PWM Resolution	Timer TOP value	Frequency
8-bit	$00FF (255)	$f_{TCK1}/510$
9-bit	$01FF (511)	$f_{TCK1}/1022$
10-bit	$03FF(1023)	$f_{TCK1}/2046$

Note that if the Compare Register contains the TOP value and the prescaler is not in use (CS12..CS10 = 001), the PWM output will not produce any pulse at all, because the

up-counting and down-counting values are reached simultaneously. When the prescaler is in use (CS12..CS10 ≠ 001 or 000), the PWM output goes active when the counter reaches TOP value, but the down-counting compare match is not interpreted to be reached before the next time the counter reaches the TOP value, making a one-period PWM pulse.

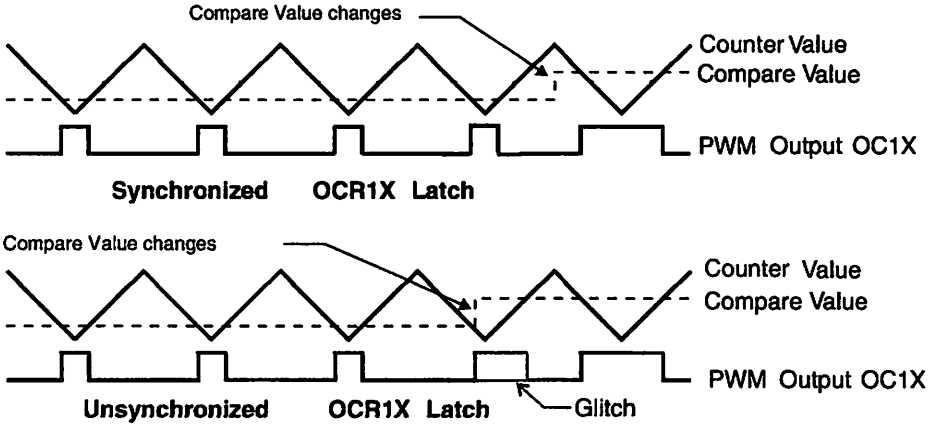
Table 15. Compare1 Mode Select in PWM Mode

COM1X1	COM1X0	Effect on OCX1
0	0	Not connected
0	1	Not connected
1	0	Cleared on compare match, up-counting. Set on compare match, down-counting (non-inverted PWM).
1	1	Cleared on compare match, down-counting. Set on compare match, up-counting (inverted PWM).

Note: X = A or B

Note that in the PWM mode, the 10 least significant OCR1A/OCR1B bits, when written, are transferred to a temporary location. They are latched when Timer/Counter1 reaches the value TOP. This prevents the occurrence of odd-length PWM pulses (glitches) in the event of an unsynchronized OCR1A/OCR1B write. See Figure 33 for an example.

Figure 33. Effects of Unsynchronized OCR1 Latching



Note: X = A or B

During the time between the write and the latch operations, a read from OCR1A or OCR1B will read the contents of the temporary location. This means that the most recently written value always will read out of OCR1A/B.

When the OCR1A/OCR1B contains $0000 or TOP, the output OC1A/OC1B is updated to low or high on the next compare match according to the settings of COM1A1/COM1A0 or COM1B1/COM1B0. This is shown in Table 16.

Table 16. PWM Outputs OCR1X = $0000 or TOP

COM1X1	COM1X0	OCR1X	Output OC1X
1	0	$0000	L

Table 16. PWM Outputs OCR1X = $0000 or TOP

COM1X1	COM1X0	OCR1X	Output OC1X
1	0	TOP	H
1	1	$0000	H
1	1	TOP	L

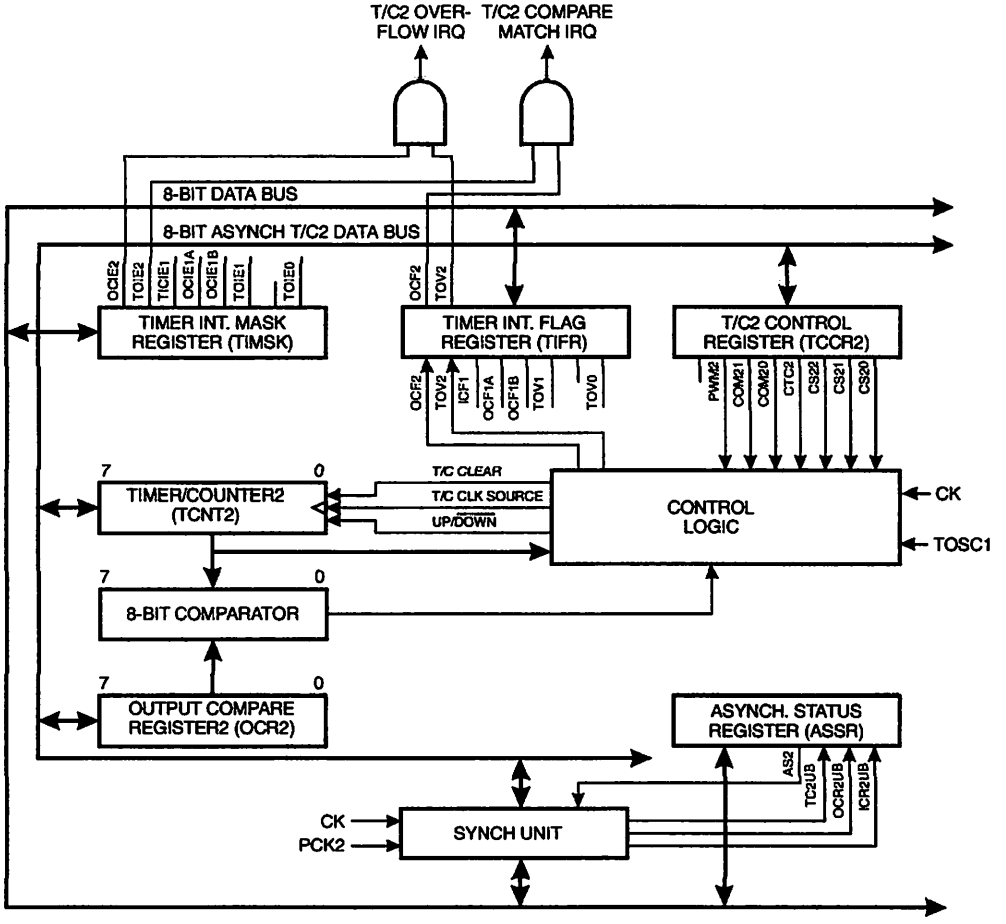
Note: X = A

In PWM mode, the Timer Overflow Flag1 (TOV1) is set when the counter advances from $0000. Timer Overflow Interrupt1 operates exactly as in normal Timer/Counter mode, i.e., it is executed when TOV1 is set, provided that Timer Overflow Interrupt1 and global interrupts are enabled. This also applies to the Timer Output Compare1 flags and interrupts.

t Timer/Counter2

Figure 34 shows the block diagram for Timer/Counter2.

Figure 34. Timer/Counter2 Block Diagram



The 8-bit Timer/Counter2 can select clock source from PCK2 or prescaled PCK2. It can also be stopped as described in the specification for the Timer/Counter Control Register (TCCR2).

The different status flags (Overflow and Compare Match) are found in the Timer/Counter Interrupt Flag Register (TIFR). Control signals are found in the

Timer/Counter Control Register (TCCR2). The interrupt enable/disable settings are found in the Timer/Counter Interrupt Mask Register (TIMSK).

This module features a high-resolution and a high-accuracy usage with the lower prescaling opportunities. Similarly, the high prescaling opportunities make this unit useful for lower speed functions or exact timing functions with infrequent actions.

The Timer/Counter supports an Output Compare function using the Output Compare Register (OCR2) as the data source to be compared to the Timer/Counter contents.The Output Compare function includes optional clearing of the counter on compare match and action on the Output Compare Pin, PD7(OC2), on compare match. Writing to PORTD7 does not set the OC2 value to a predetermined value.

Timer/Counter2 can also be used as an 8-bit Pulse Width Modulator. In this mode, Timer/Counter2 and the Output Compare Register serve as a glitch-free, stand-alone PWM with centered pulses. Refer to page 45 for a detailed description of this function.

ır/Counter2 Control ster – TCCR2

Bit	7	6	5	4	3	2	1	0	
$25 ($45)	–	PWM2	COM21	COM20	CTC2	CS22	CS21	CS20	TCCR2
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – Res: Reserved Bit**

This bit is a reserved bit in the AT90S8535 and always reads as zero.

- **Bit 6 – PWM2: Pulse Width Modulator Enable**

When set (one), this bit enables PWM mode for Timer/Counter2. This mode is described on page 45.

- **Bits 5, 4 – COM21, COM20: Compare Output Mode, Bits 1 and 0**

The COM21 and COM20 control bits determine any output pin action following a compare match in Timer/Counter2. Output pin actions affect pin PD7(OC2). This is an alternative function to an I/O port and the corresponding direction control bit must be set (one) to control an output pin. The control configuration is shown in Table 17.

Table 17. Compare Mode Select

COM21	COM20	Description
0	0	Timer/Counter disconnected from output pin OC2
0	1	Toggle the OC2 output line.
1	0	Clear the OC2 output line (to zero).
1	1	Set the OC2 output line (to one).

Note: In PWM mode, these bits have a different function. Refer to Table 19 for a detailed description.

- **Bit 3 – CTC2: Clear Timer/Counter on Compare Match**

When the CTC2 control bit is set (one), Timer/Counter2 is reset to $00 in the CPU clock cycle after a compare match. If the control bit is cleared, Timer/Counter2 continues counting and is unaffected by a compare match. Since the compare match is detected in the CPU clock cycle following the match, this function will behave differently when a prescaling higher than 1 is used for the timer. When a prescaling of 1 is used and the compare2 register is set to C, the timer will count as follows if CTC2 is set:

... I C-2 I C-1 I C I 0 I 1 I...

When the prescaler is set to divide by 8, the timer will count like this:

... I C-2, C-2, C-2, C-2, C-2, C-2, C-2, C-2 I C-1, C-1, C-1, C-1, C-1, C-1, C-1, C-1 I C, 0, 0, 0, 0, 0, 0, 0, 0 I 1, 1, 1,...

In PWM mode, this bit has no effect.

- **Bits 2, 1, 0 – CS22, CS21, CS20: Clock Select Bits 2, 1 and 0**

The Clock Select bits 2,1 and 0 define the prescaling source of Timer/Counter2.

Table 18. Timer/Counter2 Prescale Select

CS22	CS21	CS20	Description
0	0	0	Timer/Counter2 is stopped.
0	0	1	PCK2
0	1	0	PCK2/ 8
0	1	1	PCK2/ 32
1	0	0	PCK2/ 64
1	0	1	PCK2/128
1	1	0	PCK2/256
1	1	1	PCK2/1024

The Stop condition provides a Timer Enable/Disable function. The prescaled CK modes are scaled directly from the CK oscillator clock.

r/Counter2 – TCNT2

Bit	7	6	5	4	3	2	1	0	
$24 ($44)	MSB							LSB	TCNT2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

This 8-bit register contains the value of Timer/Counter2.

Timer/Counter2 is realized as an up or up/down (in PWM mode) counter with read and write access. If the Timer/Counter2 is written to and a clock source is selected, it continues counting in the timer clock cycle following the write operation.

r/Counter2 Output pare Register – OCR2

Bit	7	6	5	4	3	2	1	0	
$23 ($43)	MSB							LSB	OCR2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Output Compare Register is an 8-bit read/write register.

The Timer/Counter Output Compare Register contains the data to be continuously compared with Timer/Counter2. Actions on compare matches are specified in TCCR2. A *compare match only occurs if Timer/Counter2 counts to the OCR2 value. A software* write that sets TCNT2 and OCR2 to the same value does not generate a compare match.

A compare match will set the compare interrupt flag in the CPU clock cycle following the compare event.

r/Counter2 in PWM Mode

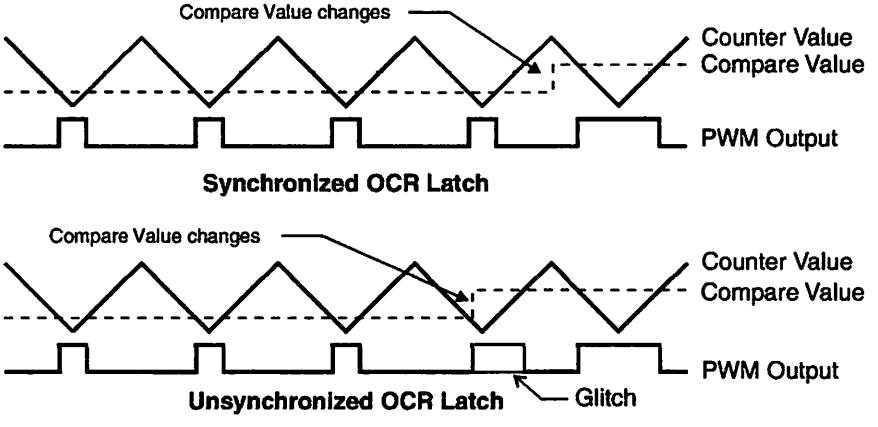
When the PWM mode is selected, Timer/Counter2 and the Output Compare Register (OCR2) form an 8-bit, free-running, glitch-free and phase correct PWM with outputs on the PD7(OC2) pin. Timer/Counter2 acts as an up/down counter, counting up from $00 to $FF, where it turns and counts down again to zero before the cycle is repeated. When the counter value matches the contents of the Output Compare Register, the PD7(OC2) pin is set or cleared according to the settings of the COM21/COM20 bits in the *Timer/Counter2 Control Register (TCCR2). Refer to Table 19 for details.*

Table 19. Compare Mode Select in PWM Mode

COM21	COM20	Effect on Compare Pin
0	0	Not connected
0	1	Not connected
1	0	Cleared on compare match, up-counting. Set on compare match, down-counting (non-inverted PWM).
1	1	Cleared on compare match, down-counting time-out. Set on compare match, up-counting (inverted PWM).

Note that in PWM mode, the Output Compare Register is transferred to a temporary location when written. The value is latched when the Timer/Counter reaches $FF. This prevents the occurrence of odd-length PWM pulses (glitches) in the event of an unsynchronized OCR2 write. See Figure 35 for an example.

Figure 35. Effects of Unsynchronized OCR Latching



During the time between the write and the latch operation, a read from OCR2 will read the contents of the temporary location. This means that the most recently written value always will read out of OCR2.

When the OCR register (not the temporary register) is updated to $00 or $FF, the PWM output changes to low or high immediately according to the settings of COM21/COM20. This is shown in Table 20.

Table 20. PWM Outputs OCR2 = $00 or $FF

COM21	COM20	OCR2	Output PWM2
1	0	$00	L

Table 20. PWM Outputs OCR2 = $00 or $FF

COM21	COM20	OCR2	Output PWM2
1	0	$FF	H
1	1	$00	H
1	1	$FF	L

In PWM mode, the Timer Overflow Flag (TOV2) is set when the counter advances from $00. Timer Overflow Interrupt2 operates exactly as in normal Timer/Counter mode, i.e., it is executed when TOV2 is set, provided that Timer Overflow Interrupt and global interrupts are enabled. This also applies to the Timer Output Compare flag and interrupt.

The frequency of the PWM will be Timer Clock Frequency divided by 510.

ıchronous Status ister – ASSR

Bit	7	6	5	4	3	2	1	0	
$22 ($22)	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	ASSR
Read/Write	R	R	R	R	R/W	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7..4 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and always read as zero.

- **Bit 3 – AS2: Asynchronous Timer/Counter2**

When AS2 is set (one), Timer/Counter2 is clocked from the TOSC1 pin. Pins PC6 and PC7 become connected to a crystal oscillator and cannot be used as general I/O pins. When cleared (zero), Timer/Counter2 is clocked from the internal system clock, CK. When the value of this bit is changed, the contents of TCNT2, OCR2 and TCCR2 might get corrupted.

- **Bit 2 – TCN2UB: Timer/Counter2 Update Busy**

When Timer/Counter2 operates asynchronously and TCNT2 is written, this bit becomes set (one). When TCNT2 has been updated from the temporary storage register, this bit is cleared (zero) by hardware. A logical "0" in this bit indicates that TCNT2 is ready to be *updated with a new value.*

- **Bit 1 – OCR2UB: Output Compare Register2 Update Busy**

When Timer/Counter2 operates asynchronously and OCR2 is written, this bit becomes set (one). When OCR2 has been updated from the temporary storage register, this bit is cleared (zero) by hardware. A logical "0" in this bit indicates that OCR2 is ready to be updated with a new value.

- **Bit 0 – TCR2UB: Timer/Counter Control Register2 Update Busy**

When Timer/Counter2 operates asynchronously and TCCR2 is written, this bit becomes set (one). When TCCR2 has been updated from the temporary storage register, this bit is cleared (zero) by hardware. A logical "0" in this bit indicates that TCCR2 is ready to be updated with a new value.

If a write is performed to any of the three Timer/Counter2 registers while its Update Busy flag is set (one), the updated value might get corrupted and cause an unintentional interrupt to occur.

The mechanisms for reading TCNT2, OCR2 and TCCR2 are different. When reading TCNT2, the actual timer value is read. When reading OCR2 or TCCR2, the value in the temporary storage register is read.

ıchronous Operation of r/Counter2

When Timer/Counter2 operates asynchronously, some considerations must be taken.

- Warning: When switching between asynchronous and synchronous clocking of Timer/Counter2, the timer registers TCNT2, OCR2 and TCCR2 might get corrupted. A safe procedure for switching clock source is:
  1. Disable the Timer/Counter2 interrupts OCIE2 and TOIE2.
  2. Select clock source by setting AS2 as appropriate.
  3. Write new values to TCNT2, OCR2 and TCCR2.
  4. To switch to asynchronous operation: Wait for TCN2UB, OCR2UB and TCR2UB.
  5. Clear the Timer/Counter2 interrupt flags.
  6. Clear the TOV2 and OCF2 flags in TIFR.
  7. Enable interrupts, if needed.
- When writing to one of the registers TCNT2, OCR2 or TCCR2, the value is transferred to a temporary register and latched after two positive edges on TOSC1. The user should not write a new value before the contents of the temporary register have been transferred to their destination. Each of the three mentioned registers have their individual temporary register. For example, writing to TCNT2 does not disturb an OCR2 write in progress. To detect that a transfer to the destination register has taken place, an Asynchronous Status Register (ASSR) has been implemented.
- When entering a Power Save Mode after having written to TCNT2, OCR2 or TCCR2, the user must wait until the written register has been updated if Timer/Counter2 is used to wake up the device. Otherwise, the MCU will go to sleep *before the changes have had any effect. This is extremely important if the Output* Compare2 interrupt is used to wake up the device; Output Compare is disabled during write to OCR2 or TCNT2. If the write cycle is not finished (i.e., the user goes to sleep before the OCR2UB bit returns to zero), the device will never get a compare match and the MCU will not wake up.
- If Timer/Counter2 is used to wake up the device from Power Save Mode, *precautions must be taken if the user wants to re-enter Power Save Mode:* The interrupt logic needs one TOSC1 cycle to be reset. If the time between wake up and re-entering Power Save Mode is less than one TOSC1 cycle, the interrupt will not occur and the device will fail to wake up. If the user is in doubt whether the time before re-entering Power Save is sufficient, the following algorithm can be used to ensure that one TOSC1 cycle has elapsed:
  1. Write a value to TCCR2, TCNT2 or OCR2.
  2. Wait until the corresponding Update Busy flag in ASSR returns to zero.
  3. Enter Power Save Mode.
- When the asynchronous operation is selected, the 32 kHz oscillator for Timer/Counter2 is always running, except in Power-down mode. After a power-up reset or wake-up from power-down, the user should be aware of the fact that this *oscillator might take as long as one second to stabilize. The user is advised* to wait for at least one second before using Timer/Counter2 after power-up or wake-up from power-down. The content of all Timer/Counter2 registers must be considered lost after a wake-up from power-down due to the unstable clock signal upon start-up, regardless of whether the oscillator is in use or a clock signal is applied to the TOSC pin.
- *Description of wake-up from Power Save Mode when the timer is clocked* asynchronously: When the interrupt condition is met, the wake-up process is started on the following cycle of the timer clock, that is, the timer is always advanced by at

least one before the processor can read the counter value. After wake-up, the MCU is halted for four cycles, it executes the interrupt routine, and resumes execution from the instruction following SLEEP.

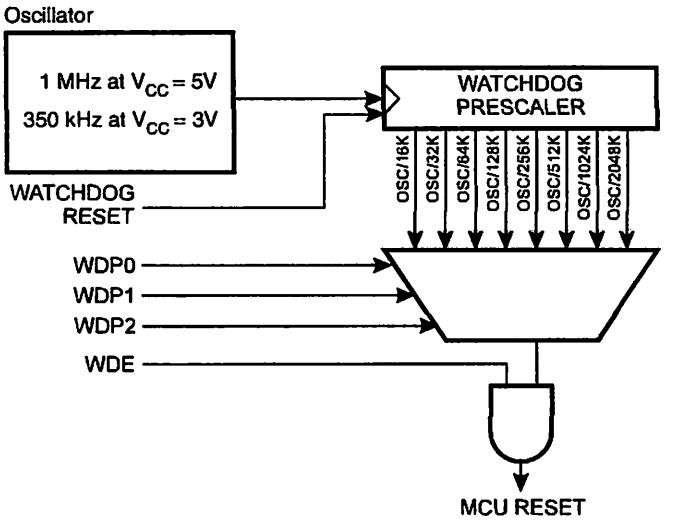
- During asynchronous operation, the synchronization of the interrupt flags for the asynchronous timer takes three processor cycles plus one timer cycle. The timer is therefore advanced by at least 1 before the processor can read the timer value causing the setting of the interrupt flag. The output compare pin is changed on the timer clock and is not synchronized to the processor clock.

tchdog Timer

The Watchdog Timer is clocked from a separate On-chip oscillator. By controlling the Watchdog Timer prescaler, the Watchdog reset interval can be adjusted as shown in Table 21. See characterization data for typical values at other V_{CC} levels. The WDR (Watchdog Reset) instruction resets the Watchdog Timer. Eight different clock cycle periods can be selected to determine the reset period. If the reset period expires without another Watchdog reset, the AT90S8535 resets and executes from the reset vector. For timing details on the Watchdog reset, refer to page 22.

To prevent unintentional disabling of the Watchdog, a special turn-off sequence must be followed when the Watchdog is disabled. Refer to the description of the Watchdog Timer Control Register for details.

Figure 36. Watchdog Timer



chdog Timer Control ister – WDTCR

Bit	7	6	5	4	3	2	1	0	
$21 ($41)	–	–	–	WDTOE	WDE	WDP2	WDP1	WDP0	WDTCR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7..5 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and will always read as zero.

- **Bit 4 – WDTOE: Watchdog Turn-off Enable**

This bit must be set (one) when the WDE bit is cleared. Otherwise, the Watchdog will not be disabled. Once set, hardware will clear this bit to zero after four clock cycles. Refer to the description of the WDE bit for a Watchdog disable procedure.

- **Bit 3 – WDE: Watchdog Enable**

When the WDE is set (one) the Watchdog Timer is enabled and if the WDE is cleared (zero) the Watchdog Timer function is disabled. WDE can only be cleared if the WDTOE bit is set (one). To disable an enabled Watchdog Timer, the following procedure must be followed:

1. In the same operation, write a logical "1" to WDTOE and WDE. A logical "1" must be written to WDE even though it is set to "1" before the disable operation starts.
2. Within the next four clock cycles, write a logical "0" to WDE. This disables the Watchdog.

- **Bits 2..0 – WDP2, WDP1, WDP0: Watchdog Timer Prescaler 2, 1 and 0**

The WDP2, WDP1 and WDP0 bits determine the Watchdog Timer prescaling when the Watchdog Timer is enabled. The different prescaling values and their corresponding time-out periods are shown in Table 21.

Table 21. Watchdog Timer Prescale Select

WDP2	WDP1	WDP0	Number of WDT Oscillator Cycles	Typical Time-out at V_{CC} = 3.0V	Typical Time-out at V_{CC} = 5.0V
0	0	0	16K cycles	47 ms	15 ms
0	0	1	32K cycles	94 ms	30 ms
0	1	0	64K cycles	0.19 s	60 ms
0	1	1	128K cycles	0.38 s	0.12 s
1	0	0	256K cycles	0.75 s	0.24 s
1	0	1	512K cycles	1.5 s	0.49 s
1	1	0	1,024K cycles	3.0 s	0.97 s
1	1	1	2,048K cycles	6.0 s	1.9 s

Note: The frequency of the Watchdog oscillator is voltage-dependent as shown in the Electrical *Characteristics section.*

The WDR (Watchdog Reset) instruction should always be executed before the Watchdog Timer is enabled. This ensures that the reset period will be in accordance with the Watchdog Timer prescale settings. If the Watchdog Timer is enabled without reset, the Watchdog Timer may not start to count from zero.

To avoid unintentional MCU resets, the Watchdog Timer should be disabled or reset before changing the Watchdog Timer Prescale Select.

²ROM Read/Write ːess

The EEPROM access registers are accessible in the I/O space.

The write access time is in the range of 2.5 - 4 ms, depending on the V_{CC} voltages. A self-timing function lets the user software detect when the next byte can be written. A special EEPROM Ready interrupt can be set to trigger when the EEPROM is ready to accept new data.

In order to prevent unintentional EEPROM writes, a specific write procedure must be followed. Refer to the description of the EEPROM Control Register for details on this.

When the EEPROM is read, the CPU is halted for four clock cycles before the next instruction is executed. When the EEPROM is written, the CPU is halted for two clock cycles before the next instruction is executed.

ROM Address Register – RH and EEARL

Bit	15	14	13	12	11	10	9	8	
$1F ($3F)	–	–	–	–	–	–	–	EEAR8	EEARH
$1E ($3E)	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	EEARL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	X	
	X	X	X	X	X	X	X	X	

The EEPROM address registers (EEARH and EEARL) specify the EEPROM address in the 512-byte EEPROM space. The EEPROM data bytes are addressed linearly between 0 and 511.

ROM Data Register – R

Bit	7	6	5	4	3	2	1	0	
$1D ($3D)	MSB							LSB	EEDR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7..0 – EEDR7.0: EEPROM Data**

For the EEPROM write operation, the EEDR register contains the data to be written to the EEPROM in the address given by the EEAR register. For the EEPROM read operation, the EEDR contains the data read out from the EEPROM at the address given by EEAR.

ROM Control Register – R

Bit	7	6	5	4	3	2	1	0	
$1C ($3C)	–	–	–	–	EERIE	EEMWE	EEWE	EERE	EECR
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7..4 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and will always read as zero.

- **Bit 3 – EERIE: EEPROM Ready Interrupt Enable**

When the I-bit in SREG and EERIE are set (one), the EEPROM Ready Interrupt is enabled. When cleared (zero), the interrupt is disabled. The EEPROM Ready Interrupt generates a constant interrupt when EEWE is cleared (zero).

- **Bit 2 – EEMWE: EEPROM Master Write Enable**

The EEMWE bit determines whether setting EEWE to "1" causes the EEPROM to be written. When EEMWE is set (one), setting EEWE will write data to the EEPROM at the selected address. If EEMWE is zero, setting EEWE will have no effect. When EEMWE has been set (one) by software, hardware clears the bit to zero after four clock cycles. See the description of the EEWE bit for a EEPROM write procedure.

- **Bit 1 – EEWE: EEPROM Write Enable**

The EEPROM Write Enable signal (EEWE) is the write strobe to the EEPROM. When address and data are correctly set up, the EEWE bit must be set to write the value into the EEPROM. The EEMWE bit must be set when the logical "1" is written to EEWE, otherwise no EEPROM write takes place. The following procedure should be followed when writing the EEPROM (the order of steps 2 and 3 is unessential):

1. Wait until EEWE becomes zero.
2. Write new EEPROM address to EEARL and EEARH (optional).
3. Write new EEPROM data to EEDR (optional).
4. Write a logical "1" to the EEMWE bit in EECR (to be able to write a logical "1" to the EEMWE bit, the EEWE bit must be written to "0" in the same cycle).
5. *Within four clock cycles after setting EEMWE, write a logical "1" to EEWE.*

Caution: An interrupt between step 4 and step 5 will make the write cycle fail, since the EEPROM Master Write Enable will time-out. If an interrupt routine accessing the EEPROM is interrupting another EEPROM access, the EEAR and EEDR registers will be modified, causing the interrupted EEPROM access to fail. It is recommended to have the global interrupt flag cleared during the four last steps to avoid these problems.

When the write access time (typically 2.5 ms at V_{CC} = 5V or 4 ms at V_{CC} = 2.7V) has elapsed, the EEWE bit is cleared (zero) by hardware. The user software can poll this bit and wait for a zero before writing the next byte. When EEWE has been set, the CPU is halted for two clock cycles before the next instruction is executed.

- **Bit 0 – EERE: EEPROM Read Enable**

The EEPROM Read Enable signal (EERE) is the read strobe to the EEPROM. When the correct address is set up in the EEAR register, the EERE bit must be set. When the EERE bit is cleared (zero) by hardware, requested data is found in the EEDR register. The EEPROM read access takes one instruction and there is no need to poll the EERE bit. When EERE has been set, the CPU is halted for four clock cycles before the next instruction is executed.

The user should poll the EEWE bit before starting the read operation. If a write operation is in progress when new data or address is written to the EEPROM I/O registers, the write operation will be interrupted and the result is undefined.

vent EEPROM ruption

During periods of low V_{CC}, the EEPROM data can be corrupted because the supply voltage is too low for the CPU and the EEPROM to operate properly. These issues are the same as for board level systems using the EEPROM and the same design solutions should be applied.

An EEPROM data corruption can be caused by two situations when the voltage is too low. First, a regular write sequence to the EEPROM requires a minimum voltage to operate correctly. Secondly, the CPU itself can execute instructions incorrectly, if the supply voltage for executing instructions is too low.

EEPROM data corruption can easily be avoided by following these design recommendations (one is sufficient):

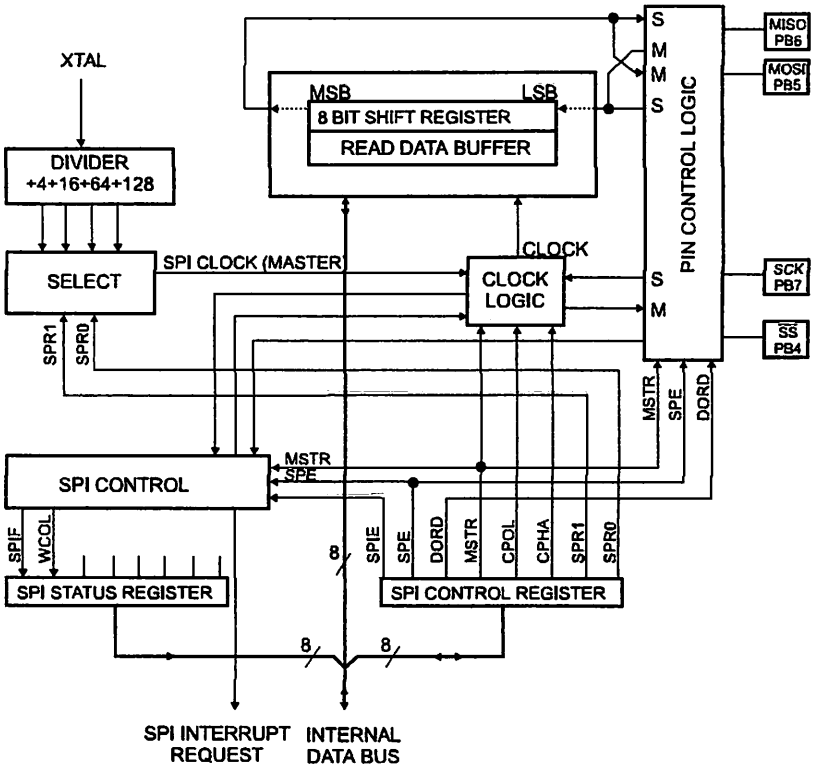
1. Keep the AVR RESET active (low) during periods of insufficient power supply voltage. This is best done by an external low V_{CC} Reset Protection circuit, often referred to as a Brown-out Detector (BOD). Please refer to application note AVR 180 for design considerations regarding power-on reset and low-voltage detection.
2. Keep the AVR core in Power-down Sleep Mode during periods of low V_{CC}. This will prevent the CPU from attempting to decode and execute instructions, effectively protecting the EEPROM registers from unintentional writes.
3. Store constants in Flash memory if the ability to change memory contents from software is not required. Flash memory cannot be updated by the CPU and will not be subject to corruption.

ial Peripheral
erface – SPI

The Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between the AT90S8535 and peripheral devices or between several AVR devices. The AT90S8535 SPI features include the following:

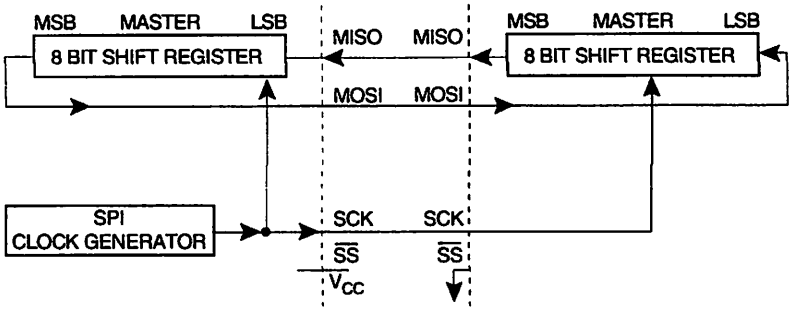
- **Full-duplex, 3-wire Synchronous Data Transfer**
- **Master or Slave Operation**
- **LSB First or MSB First Data Transfer**
- ***Four Programmable Bit Rates***
- **End-of-transmission Interrupt Flag**
- **Write Collision Flag Protection**
- **Wake-up from Idle Mode**

Figure 37. SPI Block Diagram



The interconnection between master and slave CPUs with SPI is shown in Figure 38. The PB7(SCK) pin is the clock output in the Master Mode and is the clock input in the Slave Mode. Writing to the SPI Data Register of the master CPU starts the SPI clock generator and the data written shifts out of the PB5(MOSI) pin and into the PB5(MOSI) pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end-of-transmission flag (SPIF). If the SPI interrupt enable bit (SPIE) in the SPCR register is set, an interrupt is requested. The Slave Select input, PB4(SS), is set low to select an individual slave SPI device. The two shift registers in the master and the slave can be considered as one distributed 16-bit circular shift register. This is shown in Figure 38. When data is shifted from the master to the slave, data is also shifted in the opposite direction, simultaneously. During one shift cycle, data in the master and the slave is interchanged.

Figure 38. SPI Master-slave Interconnection



The system is single-buffered in the transmit direction and double-buffered in the receive direction. This means that bytes to be transmitted cannot be written to the SPI Data Register before the entire shift cycle is completed. When receiving data, however, a received byte must be read from the SPI Data Register before the next byte has been completely shifted in. Otherwise, the first byte is lost.

When the SPI is enabled, the data direction of the MOSI, MISO, SCK and $\overline{SS}$ pins is overridden according to *Table 22.*

Table 22. SPI Pin Overrides

Pin	Direction, Master SPI	Direction, Slave SPI
MOSI	User Defined	Input
MISO	Input	User Defined
SCK	User Defined	Input
$\overline{SS}$	User Defined	Input

Note: See "Alternate Functions of Port B" on page 79 for a detailed description of how to define the direction of the user-defined SPI pins.

Pin Functionality

When the SPI is configured as a master (MSTR in SPCR is set), the user can determine the direction of the $\overline{SS}$ pin. If $\overline{SS}$ is configured as an output, the pin is a general output pin, which does not affect the SPI system. If $\overline{SS}$ is configured as an input, it must be held high to ensure master SPI operation. If the $\overline{SS}$ pin is driven low by peripheral circuitry when the SPI is configured as master with the $\overline{SS}$ pin defined as an input, the SPI system interprets this as another master selecting the SPI as a slave and starting to send data to it. To avoid bus contention, the SPI system takes the following actions:

1. The MSTR bit in SPCR is cleared and the SPI system becomes a slave. As a result of the SPI becoming a slave, the MOSI and SCK pins become inputs.
2. The SPIF flag in SPSR is set and if the SPI interrupt is enabled and the I-bit in SREG are set, the interrupt routine will be executed.

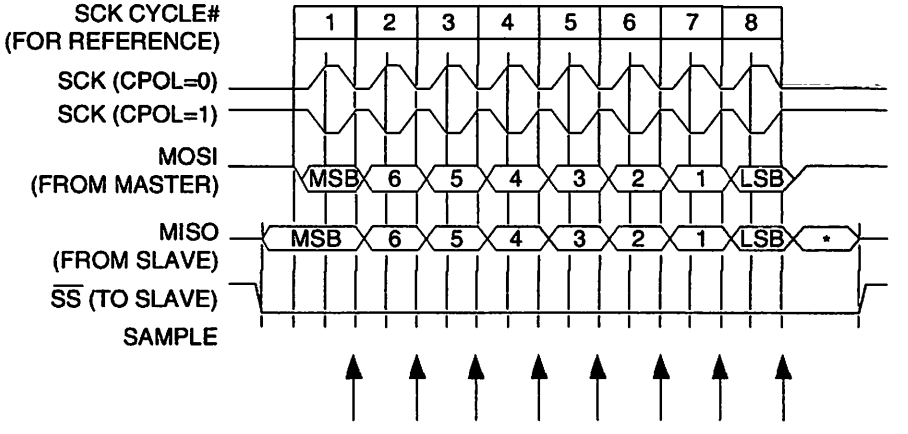
Thus, when interrupt-driven SPI transmission is used in Master Mode and there exists a possibility that $\overline{SS}$ is driven low, the interrupt should always check that the MSTR bit is still set. Once the MSTR bit has been cleared by a slave select, it must be set by the user to re-enable the SPI Master Mode.

When the SPI is configured as a slave, the $\overline{SS}$ pin is always input. When $\overline{SS}$ is held low, the SPI is activated and MISO becomes an output if configured so by the user. All other pins are inputs. When $\overline{SS}$ is driven high, all pins are inputs and the SPI is passive, which means that it will not receive incoming data. Note that the SPI logic will be reset once the $\overline{SS}$ pin is brought high. If the $\overline{SS}$ pin is brought high during a transmission, the SPI will stop sending and receiving immediately and both data received and data sent must be considered as lost.

a Modes

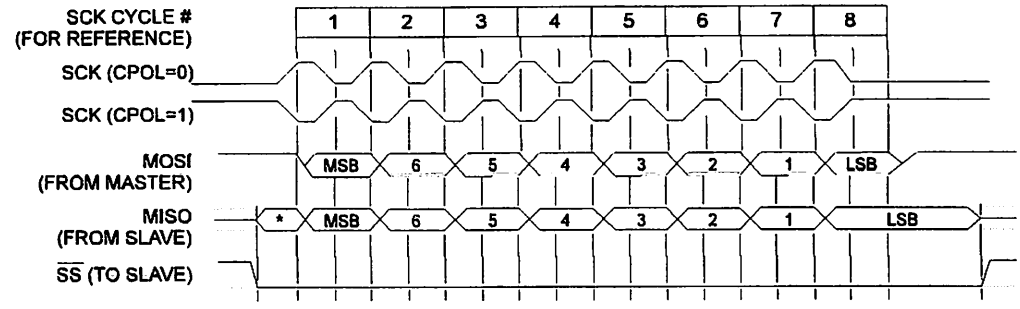
There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 39 and Figure 40.

Figure 39. SPI Transfer Format with CPHA = 0 and DORD = 0



*Not defined but normally MSB of character just received.

Figure 40. SPI Transfer Format with CPHA = 1 and DORD = 0



* Not defined but normally LSB of previously transmitted character

Control Register – SPCR

Bit	7	6	5	4	3	2	1	0	
$0D ($2D)	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – SPIE: SPI Interrupt Enable**

This bit causes the SPI interrupt to be executed if SPIF bit in the SPSR register is set and the global interrupts are enabled.

- **Bit 6 – SPE: SPI Enable**

When the SPE bit is set (one), the SPI is enabled. This bit must be set to enable any SPI operations.

- **Bit 5 – DORD: Data Order**

When the DORD bit is set (one), the LSB of the data word is transmitted first.

When the DORD bit is cleared (zero), the MSB of the data word is transmitted first.

- **Bit 4 – MSTR: Master/Slave Select**

This bit selects Master SPI Mode when set (one) and Slave SPI Mode when cleared (zero). If $\overline{SS}$ is configured as an input and is driven low while MSTR is set, MSTR will be cleared and SPIF in SPSR will become set. The user will then have to set MSTR to re-enable SPI Master Mode.

- **Bit 3 – CPOL: Clock Polarity**

When this bit is set (one), SCK is high when idle. When CPOL is cleared (zero), SCK is low when idle. Refer to Figure 39. and Figure 40. for additional information.

- **Bit 2 – CPHA: Clock Phase**

Refer to Figure 40 or Figure 41 for the functionality of this bit.

- **Bits 1,0 – SPR1, SPR0: SPI Clock Rate Select 1 and 0**

These two bits control the SCK rate of the device configured as a master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator clock frequency f_{cl} is shown in Table 23.

Table 23. Relationship between SCK and the Oscillator Frequency

SPR1	SPR0	SCK Frequency
0	0	$f_{cl}/4$
0	1	$f_{cl}/16$
1	0	$f_{cl}/64$
1	1	$f_{cl}/128$

Status Register – SPSR

Bit	7	6	5	4	3	2	1	0	
$0E ($2E)	SPIF	WCOL	–	–	–	–	–	–	SPSR
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – SPIF: SPI Interrupt Flag**

When a serial transfer is complete, the SPIF bit is set (one) and an interrupt is generated if SPIE in SPCR is set (one) and global interrupts are enabled. If $\overline{SS}$ is an input and is driven low when the SPI is in Master Mode, this will also set the SPIF flag. SPIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, the SPIF bit is cleared by first reading the SPI Status Register with SPIF set (one), then accessing the SPI Data Register (SPDR).

- **Bit 6 – WCOL: Write Collision flag**

The WCOL bit is set if the SPI Data Register (SPDR) is written during a data transfer. The WCOL bit (and the SPIF bit) are cleared (zero) by first reading the SPI Status Register with WCOL set (one) and then accessing the SPI Data Register.

- **Bit 5..0 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and will always read as zero.

The SPI interface on the AT90S8535 is also used for program memory and EEPROM downloading or uploading. See page 99 for serial programming and verification.

Data Register – SPDR

Bit	7	6	5	4	3	2	1	0	
$0F ($2F)	MSB							LSB	SPDR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	X	X	X	X	X	X	X	X	Undefined

The SPI Data Register is a read/write register used for data transfer between the register file and the SPI Shift Register. Writing to the register initiates data transmission. Reading the register causes the Shift Register Receive buffer to be read.

RT

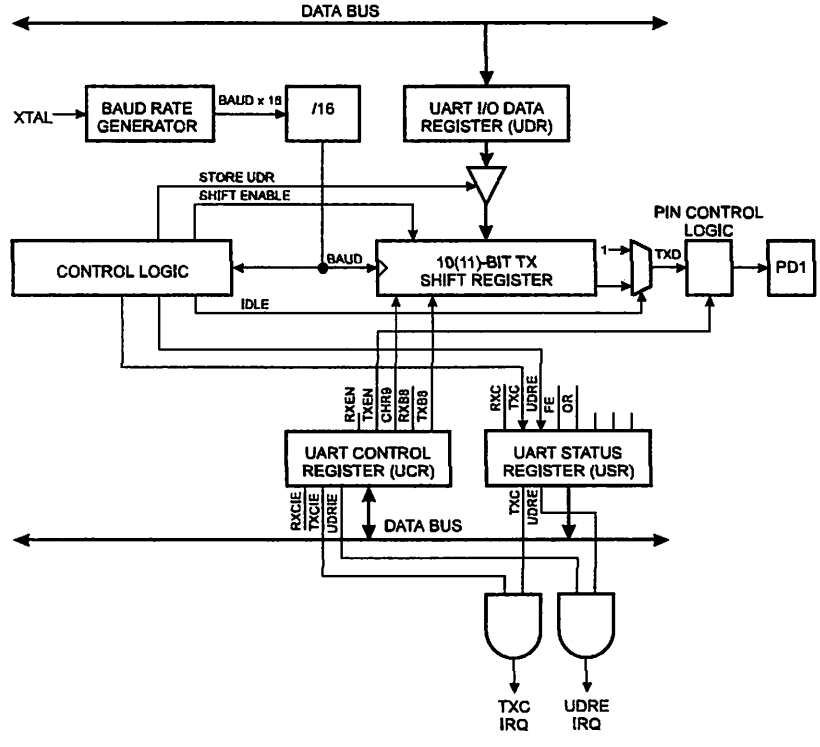
The AT90S8535 features a full duplex (separate receive and transmit registers) Universal Asynchronous Receiver and Transmitter (UART). The main features are:

- **Baud Rate Generator that can Generate a Large Number of Baud Rates (bps)**
- **High Baud Rates at Low XTAL Frequencies**
- **8 or 9 Bits Data**
- **Noise Filtering**
- **Overrun Detection**
- **Framing Error Detection**
- **False Start Bit Detection**
- **Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete**
- **Buffered Transmit and Receive**

a Transmission

A block schematic of the UART transmitter is shown in Figure 41.

Figure 41. UART Transmitter



Data transmission is initiated by writing the data to be transmitted to the UART I/O Data Register, UDR. Data is transferred from UDR to the Transmit shift register when:

- A new character is written to UDR after the stop bit from the previous character has been shifted out. The shift register is loaded immediately.
- A new character is written to UDR before the stop bit from the previous character has been shifted out. The shift register is loaded when the stop bit of the character currently being transmitted is shifted out.

If the 10(11)-bit Transmitter shift register is empty, data is transferred from UDR to the shift register. The UDRE (UART Data Register Empty) bit in the UART Status Register, USR, is set. When this bit is set (one), the UART is ready to receive the next character. At the same time as the data is transferred from UDR to the 10(11)-bit shift register, bit 0 of the shift register is cleared (start bit) and bit 9 or 10 is set (stop bit). If 9-bit data word

is selected (the CHR9 bit in the UART Control Register, UCR is set), the TXB8 bit in UCR is transferred to bit 9 in the Transmit shift register.

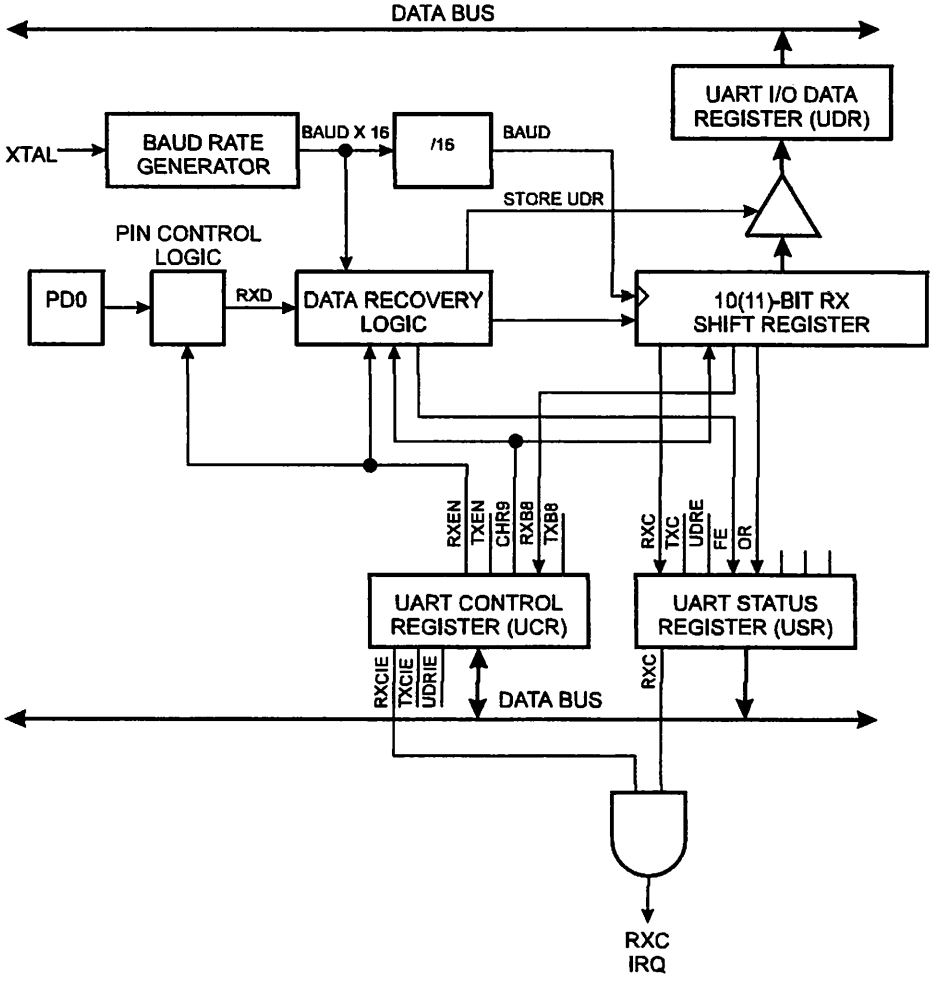
On the baud rate clock following the transfer operation to the shift register, the start bit is shifted out on the TXD pin. Then follows the data, LSB first. When the stop bit has been shifted out, the shift register is loaded if any new data has been written to the UDR during the transmission. During loading, UDRE is set. If there is no new data in the UDR register to send when the stop bit is shifted out, the UDRE flag will remain set until UDR is written again. When no new data has been written and the stop bit has been present on TXD for one bit length, the TX Complete flag (TXC) in USR is set.

The TXEN bit in UCR enables the UART Transmitter when set (one). When this bit is cleared (zero), the PD1 pin can be used for general I/O. When TXEN is set, the UART Transmitter will be connected to PD1, which is forced to be an output pin regardless of the setting of the DDD1 bit in DDRD.

a Reception

Figure 42 shows a block diagram of the UART Receiver.

Figure 42. UART Receiver



The receiver front-end logic samples the signal on the RXD pin at a frequency 16 times the baud rate. While the line is idle, one single sample of logical "0" will be interpreted as the falling edge of a start bit and the start bit detection sequence is initiated. Let sample

1 denote the first zero-sample. Following the 1-to-0 transition, the receiver samples the RXD pin at samples 8, 9 and 10. If two or more of these three samples are found to be logical "1"s, the start bit is rejected as a noise spike and the receiver starts looking for the next 1-to-0 transition.

If however, a valid start bit is detected, sampling of the data bits following the start bit is performed. These bits are also sampled at samples 8, 9 and 10. The logical value found in at least two of the three samples is taken as the bit value. All bits are shifted into the Transmitter Shift register as they are sampled. Sampling of an incoming character is shown in Figure 43.

Figure 43. Sampling Received Data

When the stop bit enters the receiver, the majority of the three samples must be one to accept the stop bit. If two or more samples are logical "0"s, the Framing Error (FE) flag in the UART Status Register (USR) is set. Before reading the UDR register, the user should always check the FE bit to detect framing errors.

Whether or not a valid stop bit is detected at the end of a character reception cycle, the data is transferred to UDR and the RXC flag in USR is set. UDR is in fact two physically separate registers, one for transmitted data and one for received data. When UDR is read, the Receive Data register is accessed and when UDR is written, the Transmit Data register is accessed. If 9-bit data word is selected (the CHR9 bit in the UART Control Register, UCR is set), the RXB8 bit in UCR is loaded with bit 9 in the Transmit Shift register when data is transferred to UDR.

If, after having received a character, the UDR register has not been read since the last receive, the OverRun (OR) flag in UCR is set. This means that the last data byte shifted into the shift register could not be transferred to UDR and has been lost. The OR bit is buffered and is updated when the valid data byte in UDR is read. Thus, the user should *always check the OR bit after reading the UDR register in order to detect any overruns if* the baud rate is high or CPU load is high.

When the RXEN bit in the UCR register is cleared (zero), the receiver is disabled. This means that the PD0 pin can be used as a general I/O pin. When RXEN is set, the UART Receiver will be connected to PD0, which is forced to be an input pin regardless of the setting of the DDD0 bit in DDRD. When PD0 is forced to input by the UART, the *PORTD0 bit can still be used to control the pull-up resistor on the pin.*

When the CHR9 bit in the UCR register is set, transmitted and received characters are 9 bits long, plus start and stop bits. The ninth data bit to be transmitted is the TXB8 bit in UCR register. This bit must be set to the wanted value before a transmission is initiated by writing to the UDR register. The ninth data bit received is the RXB8 bit in the UCR register.

RT Control

T I/O Data Register – UDR

Bit	7	6	5	4	3	2	1	0	
$0C ($2C)	MSB							LSB	UDR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The UDR register is actually two physically separate registers sharing the same I/O address. When writing to the register, the UART Transmit Data register is written. When reading from UDR, the UART Receive Data register is read.

T Status Register – USR

Bit	7	6	5	4	3	2	1	0	
$0B ($2B)	RXC	TXC	UDRE	FE	OR	–	–	–	USR
Read/Write	R	R/W	R	R	R	R	R	R	
Initial Value	0	0	1	0	0	0	0	0	

The USR register is a read-only register providing information on the UART status.

- **Bit 7 – RXC: UART Receive Complete**

This bit is set (one) when a received character is transferred from the Receiver Shift register to UDR. The bit is set regardless of any detected framing errors. When the RXCIE bit in UCR is set, the UART Receive Complete interrupt will be executed when RXC is set (one). RXC is cleared by reading UDR. When interrupt-driven data reception is used, the UART Receive Complete Interrupt routine must read UDR in order to clear RXC, otherwise a new interrupt will occur once the interrupt routine terminates.

- **Bit 6 – TXC: UART Transmit Complete**

This bit is set (one) when the entire character (including the stop bit) in the Transmit Shift register has been shifted out and no new data has been written to UDR. This flag is especially useful in half-duplex communications interfaces, where a transmitting application must enter receive mode and free the communications bus immediately after completing the transmission.

When the TXCIE bit in UCR is set, setting of TXC causes the UART Transmit Complete interrupt to be executed. TXC is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, the TXC bit is cleared (zero) by writing a logical "1" to the bit.

- **Bit 5 – UDRE: UART Data Register Empty**

This bit is set (one) when a character written to UDR is transferred to the Transmit Shift register. Setting of this bit indicates that the transmitter is ready to receive a new character for transmission.

When the UDRIE bit in UCR is set, the UART Transmit Complete interrupt to be executed as long as UDRE is set. UDRE is cleared by writing UDR. When interrupt-driven data transmission is used, the UART Data Register Empty Interrupt routine must write UDR in order to clear UDRE, otherwise a new interrupt will occur once the interrupt routine terminates.

UDRE is set (one) during reset to indicate that the transmitter is ready.

- **Bit 4 – FE: Framing Error**

This bit is set if a Framing Error condition is detected, i.e., when the stop bit of an incoming character is zero.

The FE bit is cleared when the stop bit of received data is one.

- **Bit 3 – OR: OverRun**

This bit is set if an Overrun condition is detected, i.e., when a character already present in the UDR register is not read before the next character has been shifted into the Receiver Shift register. The OR bit is buffered, which means that it will be set once the valid data still in UDR is read.

The OR bit is cleared (zero) when data is received and transferred to UDR.

- **Bits 2..0 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and will always read as zero.

T Control Register – UCR

Bit	7	6	5	4	3	2	1	0	
$0A ($2A)	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8	UCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	W	
Initial Value	0	0	0	0	0	0	1	0	

- **Bit 7 – RXCIE: RX Complete Interrupt Enable**

When this bit is set (one), a setting of the RXC bit in USR will cause the Receive Complete Interrupt routine to be executed provided that global interrupts are enabled.

- **Bit 6 – TXCIE: TX Complete Interrupt Enable**

When this bit is set (one), a setting of the TXC bit in USR will cause the Transmit Complete Interrupt routine to be executed provided that global interrupts are enabled.

- **Bit 5 – UDRIE: UART Data Register Empty Interrupt Enable**

When this bit is set (one), a setting of the UDRE bit in USR will cause the UART Data Register Empty Interrupt routine to be executed provided that global interrupts are enabled.

- **Bit 4 – RXEN: Receiver Enable**

This bit enables the UART receiver when set (one). When the receiver is disabled, the RXC, OR and FE status flags cannot become set. If these flags are set, turning off RXEN does not cause them to be cleared.

- **Bit 3 – TXEN: Transmitter Enable**

This bit enables the UART transmitter when set (one). When disabling the transmitter while transmitting a character, the transmitter is not disabled before the character in the shift register plus any following character in UDR has been completely transmitted.

- **Bit 2 – CHR9: 9 Bit Characters**

When this bit is set (one), transmitted and received characters are 9 bits long, plus start and stop bits. The ninth bit is read and written by using the RXB8 and TXB8 bits in UCR, respectively. The ninth data bit can be used as an extra stop bit or a parity bit.

- **Bit 1 – RXB8: Receive Data Bit 8**

When CHR9 is set (one), RXB8 is the ninth data bit of the received character.

- ***Bit 0 – TXB8: Transmit Data Bit 8***

When CHR9 is set (one), TXB8 is the ninth data bit in the character to be transmitted.

d Rate Generator

The baud rate generator is a frequency divider which generates baud rates according to the following equation:

$$BAUD = \frac{f_{CK}}{16(UBRR + 1)}$$

- BAUD = Baud rate
- f_{CK} = Crystal clock frequency
- UBRR = Contents of the UART Baud Rate register, UBRR (0 - 255)

For standard crystal frequencies, the most commonly used baud rates can be generated by using the UBRR settings in Table 24. UBRR values that yield an actual baud rate differing less than 2% from the target baud rate are boldface in the table. However, using baud rates that have more than 1% error is not recommended. High error ratings give less noise resistance.

Table 24. UBRR Settings at Various Crystal Frequencies (Examples)

Baud Rate	1 MHz		%Error	1.8432 MHz		%Error	2 MHz		%Error	2.4576 MHz		%Error
2400	UBRR=	**25**	**0.2**	UBRR=	**47**	**0.0**	UBRR=	**51**	**0.2**	UBRR=	**63**	**0.0**
4800	UBRR=	**12**	**0.2**	UBRR=	**23**	**0.0**	UBRR=	**25**	**0.2**	UBRR=	**31**	**0.0**
9600	UBRR=	6	7.5	UBRR=	**11**	**0.0**	UBRR=	**12**	**0.2**	UBRR=	**15**	**0.0**
14400	UBRR=	3	7.8	UBRR=	**7**	**0.0**	UBRR=	8	3.7	UBRR=	10	3.1
19200	UBRR=	2	7.8	UBRR=	**5**	**0.0**	UBRR=	6	7.5	UBRR=	**7**	**0.0**
28800	UBRR=	1	7.8	UBRR=	**3**	**0.0**	UBRR=	3	7.8	UBRR=	4	6.3
38400	UBRR=	1	22.9	UBRR=	**2**	**0.0**	UBRR=	2	7.8	UBRR=	**3**	**0.0**
57600	UBRR=	0	7.8	UBRR=	**1**	**0.0**	UBRR=	1	7.8	UBRR=	2	12.5
76800	UBRR=	0	22.9	UBRR=	1	33.3	UBRR=	1	22.9	UBRR=	**1**	**0.0**
115200	UBRR=	0	84.3	UBRR=	**0**	**0.0**	UBRR=	0	7.8	UBRR=	0	25.0

Baud Rate	3.2768 MHz		%Error	3.6864 MHz		%Error	4 MHz		%Error	4.608 MHz		%Error
2400	UBRR=	**84**	**0.4**	UBRR=	**95**	**0.0**	UBRR=	**103**	**0.2**	UBRR=	**119**	**0.0**
4800	UBRR=	**42**	**0.8**	UBRR=	**47**	**0.0**	UBRR=	**51**	**0.2**	UBRR=	**59**	**0.0**
9600	UBRR=	**20**	**1.6**	UBRR=	**23**	**0.0**	UBRR=	**25**	**0.2**	UBRR=	**29**	**0.0**
14400	UBRR=	**13**	**1.6**	UBRR=	**15**	**0.0**	UBRR=	16	2.1	UBRR=	**19**	**0.0**
19200	UBRR=	10	3.1	UBRR=	**11**	**0.0**	UBRR=	**12**	**0.2**	UBRR=	**14**	**0.0**
28800	UBRR=	**6**	**1.6**	UBRR=	**7**	**0.0**	UBRR=	8	3.7	UBRR=	**9**	**0.0**
38400	UBRR=	4	6.3	UBRR=	**5**	**0.0**	UBRR=	6	7.5	UBRR=	7	6.7
57600	UBRR=	3	12.5	UBRR=	**3**	**0.0**	UBRR=	3	7.8	UBRR=	**4**	**0.0**
76800	UBRR=	2	12.5	UBRR=	**2**	**0.0**	UBRR=	2	7.8	UBRR=	3	6.7
115200	UBRR=	1	12.5	UBRR=	**1**	**0.0**	UBRR=	1	7.8	UBRR=	2	20.0

Baud Rate	7.3728 MHz		%Error	8 MHz		%Error	9.216 MHz		%Error	11.059 MHz		%Error
2400	UBRR=	**191**	**0.0**	UBRR=	**207**	**0.2**	UBRR=	**239**	**0.0**	UBRR=	287	-
4800	UBRR=	**95**	**0.0**	UBRR=	**103**	**0.2**	UBRR=	**119**	**0.0**	UBRR=	**143**	**0.0**
9600	UBRR=	**47**	**0.0**	UBRR=	**51**	**0.2**	UBRR=	**59**	**0.0**	UBRR=	**71**	**0.0**
14400	UBRR=	**31**	**0.0**	UBRR=	**34**	**0.8**	UBRR=	**39**	**0.0**	UBRR=	**47**	**0.0**
19200	UBRR=	**23**	**0.0**	UBRR=	**25**	**0.2**	UBRR=	**29**	**0.0**	UBRR=	**35**	**0.0**
28800	UBRR=	**15**	**0.0**	UBRR=	16	2.1	UBRR=	**19**	**0.0**	UBRR=	**23**	**0.0**
38400	UBRR=	**11**	**0.0**	UBRR=	**12**	**0.2**	UBRR=	**14**	**0.0**	UBRR=	**17**	**0.0**
57600	UBRR=	**7**	**0.0**	UBRR=	8	3.7	UBRR=	**9**	**0.0**	UBRR=	**11**	**0.0**
76800	UBRR=	**5**	**0.0**	UBRR=	6	7.5	UBRR=	7	6.7	UBRR=	**8**	**0.0**
115200	UBRR=	**3**	**0.0**	UBRR=	3	7.8	UBRR=	**4**	**0.0**	UBRR=	**5**	**0.0**

Note: Maximum baud rate to each frequency.

T Baud Rate Register – R

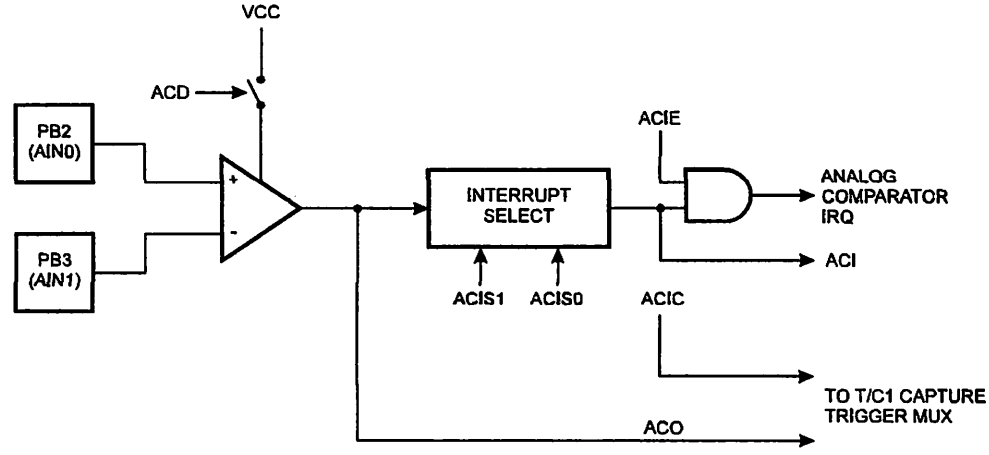
Bit	7	6	5	4	3	2	1	0	
$09 ($29)	MSB							LSB	UBRR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The UBRR register is an 8-bit read/write register that specifies the UART Baud Rate according to the equation on the previous page.

alog Comparator

The Analog Comparator compares the input values on the positive input PB2 (AIN0) and negative input PB3 (AIN1). When the voltage on the positive input PB2 (AIN0) is higher than the voltage on the negative input PB3 (AIN1), the Analog Comparator Output (ACO) is set (one). The comparator's output can be set to trigger the Timer/Counter1 Input Capture function. In addition, the comparator can trigger a separate interrupt, exclusive to the Analog Comparator. The user can select Interrupt triggering on comparator output rise, fall or toggle. A block diagram of the comparator and its surrounding logic is shown in Figure 44.

Figure 44. Analog Comparator Block Diagram



log Comparator Control Status Register – ACSR

Bit	7	6	5	4	3	2	1	0	
$08 ($28)	ACD	–	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	ACSR
Read/Write	R/W	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	N/A	0	0	0	0	0	

- **Bit 7 – ACD: Analog Comparator Disable**

When this bit is set (one), the power to the Analog Comparator is switched off. This bit can be set at any time to turn off the Analog Comparator. When changing the ACD bit, the Analog Comparator interrupt must be disabled by clearing the ACIE bit in ACSR. Otherwise an interrupt can occur when the bit is changed.

- **Bit 6 – Res: Reserved Bit**

This bit is a reserved bit in the AT90S8535 and will always read as zero.

- **Bit 5 – ACO: Analog Comparator Output**

ACO is directly connected to the comparator output.

- **Bit 4 – ACI: Analog Comparator Interrupt Flag**

This bit is set (one) when a comparator output event triggers the interrupt mode defined by ACI1 and ACI0. The Analog Comparator Interrupt routine is executed if the ACIE bit is set (one) and the I-bit in SREG is set (one). ACI is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ACI is cleared by writing a logical "1" to the flag.

- **Bit 3 – ACIE: Analog Comparator Interrupt Enable**

When the ACIE bit is set (one) and the I-bit in the Status Register is set (one), the Analog Comparator interrupt is activated. When cleared (zero), the interrupt is disabled.

- **Bit 2 – ACIC: Analog Comparator Input Capture Enable**

When set (one), this bit enables the Input Capture function in Timer/Counter1 to be triggered by the Analog Comparator. The comparator output is in this case directly connected to the Input Capture front-end logic, making the comparator utilize the noise canceler and edge select features of the Timer/Counter1 Input Capture interrupt. When cleared (zero), no connection between the Analog Comparator and the Input Capture function is given. To make the comparator trigger the Timer/Counter1 Input Capture interrupt, the TICIE1 bit in the Timer Interrupt Mask Register (TIMSK) must be set (one).

- **Bits 1,0 – ACIS1, ACIS0: Analog Comparator Interrupt Mode Select**

These bits determine which comparator events trigger the Analog Comparator interrupt. The different settings are shown in Table 25.

Table 25. ACIS1/ACIS0 Settings

ACIS1	ACIS0	Interrupt Mode
0	0	Comparator Interrupt on Output Toggle
0	1	Reserved
1	0	Comparator Interrupt on Falling Output Edge
1	1	Comparator Interrupt on Rising Output Edge

Note: When changing the ACIS1/ACIS0 bits, the Analog Comparator interrupt must be disabled by clearing its interrupt enable bit in the ACSR register. Otherwise an interrupt can occur when the bits are changed.

Caution: Using the SBI or CBI instruction on bits other than ACI in this register will write a "1" back into ACI if it is read as set, thus clearing the flag.

alog-to-Digital nverter

ture list

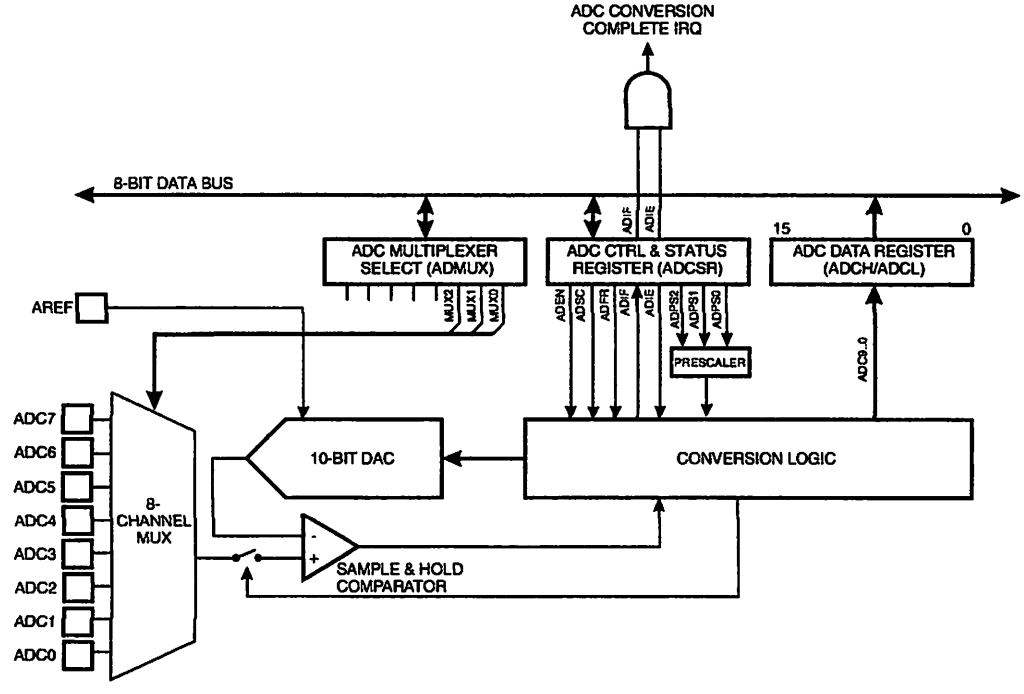
- **10-bit Resolution**
- **0.5 LSB Integral Non-linearity**
- **±2 LSB Absolute Accuracy**
- ***65 - 260 µs Conversion Time***
- **Up to 15 kSPS at Maximum Resolution**
- **8 Multiplexed Input Channels**
- **Rail-to-Rail Input Range**
- **Free Running or Single Conversion Mode**
- **Interrupt on ADC Conversion Complete**
- **Sleep Mode Noise Canceler**

The AT90S8535 features a 10-bit successive approximation ADC. The ADC is connected to an 8-channel Analog Multiplexer that allows each pin of Port A to be used as an input for the ADC. The ADC contains a Sample and Hold Amplifier that ensures that the input voltage to the ADC is held at a constant level during conversion. A block diagram of the ADC is shown in Figure 45.

The ADC has two separate analog supply voltage pins, AVCC and AGND. AGND must be connected to GND and the voltage on AV_{CC} must not differ more than ±0.3V from V_{CC}. See "ADC Noise Canceling Techniques" on page 74 on how to connect these pins.

An external reference voltage must be applied to the AREF pin. This voltage must be in the range 2V - AV_{CC}.

Figure 45. Analog-to-Digital Converter Block Schematic



ɪration

The ADC converts an analog input voltage to a 10-bit digital value through successive approximation. The minimum value represents AGND and the maximum value represents the voltage on the AREF pin minus one LSB. The analog input channel is selected by writing to the MUX bits in ADMUX. Any of the eight ADC input pins ADC7..0 can be selected as single-ended inputs to the ADC.

The ADC can operate in two modes – Single Conversion and Free Running. In Single Conversion Mode, each conversion will have to be initiated by the user. In Free Running Mode, the ADC is constantly sampling and updating the ADC Data Register. The ADFR bit in ADCSR selects between the two available modes.

The ADC is enabled by setting the ADC Enable bit, ADEN in ADCSR. Input channel selections will not go into effect until ADEN is set. The ADC does not consume power when ADEN is cleared, so it is recommended to switch off the ADC before entering power-saving sleep modes.

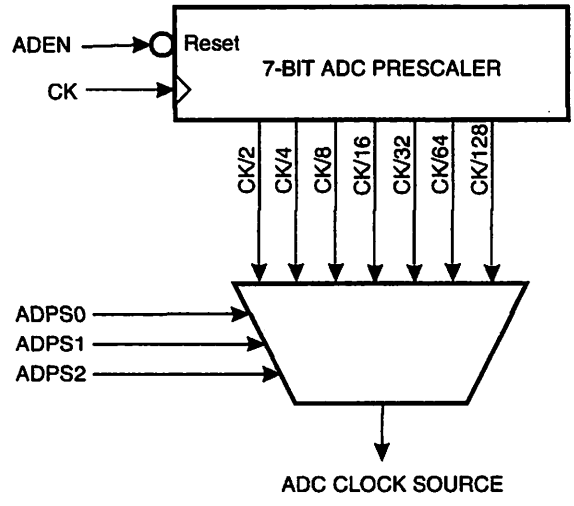
A conversion is started by writing a logical "1" to the ADC Start Conversion bit, ADSC. This bit stays high as long as the conversion is in progress and will be set to zero by hardware when the conversion is completed. If a different data channel is selected while a conversion is in progress, the ADC will finish the current conversion before performing the channel change.

The ADC generates a 10-bit result, which is presented in the ADC data register, ADCH and ADCL. When reading data, ADCL must be read first, then ADCH, to ensure that the content of the data register belongs to the same conversion. Once ADCL is read, ADC access to data register is blocked. This means that if ADCL has been read and a conversion completes before ADCH is read, neither register is updated and the result from the conversion is lost. Then ADCH is read, ADC access to the ADCH and ADCL register *is re-enabled.*

The ADC has its own interrupt that can be triggered when a conversion completes. When ADC access to the data registers is prohibited between reading of ADCH and ADCL, the interrupt will trigger even if the result is lost.

scaling

Figure 46. ADC Prescaler



The successive approximation circuitry requires an input clock frequency between 50 kHz and 200 kHz to achieve maximum resolution. If a resolution of lower than 10 bits is required, the input clock frequency to the ADC can be higher than 200 kHz to achieve a

higher sampling rate. See "ADC Characteristics" on page 75 for more details. The ADC module contains a prescaler, which divides the system clock to an acceptable ADC clock frequency.

The ADPS2..0 bits in ADCSR are used to generate a proper ADC clock input frequency from any CPU frequency above 100 kHz. The prescaler starts counting from the moment the ADC is switched on by setting the ADEN bit in ADCSR. The prescaler keeps running for as long as the ADEN bit is set and is continuously reset when ADEN is low.

When initiating a conversion by setting the ADSC bit in ADCSR, the conversion starts at the following rising edge of the ADC clock cycle.

A normal conversion takes 13 ADC clock cycles. In certain situations, the ADC needs more clock cycles for initialization and to minimize offset errors. Extended conversions take 25 ADC clock cycles and occur as the first conversion after the ADC is switched on (ADEN in ADCSR is set).

The actual sample-and-hold takes place 1.5 ADC clock cycles after the start of a normal conversion and 13.5 ADC clock cycles after the start of an extended conversion. When a conversion is complete, the result is written to the ADC data registers and ADIF is set. In Single Conversion Mode, ADSC is cleared simultaneously. The software may then set ADSC again and a new conversion will be initiated on the first rising ADC clock edge. In Free Running Mode, a new conversion will be started immediately after the conversion completes, while ADSC remains high. Using Free Running Mode and an ADC clock frequency of 200 kHz gives the lowest conversion time with a maximum resolution, 65 µs, equivalent to 15 kSPS. For a summary of conversion times, see Table 26.

Figure 47. ADC Timing Diagram, Extended Conversion (Single Conversion Mode)

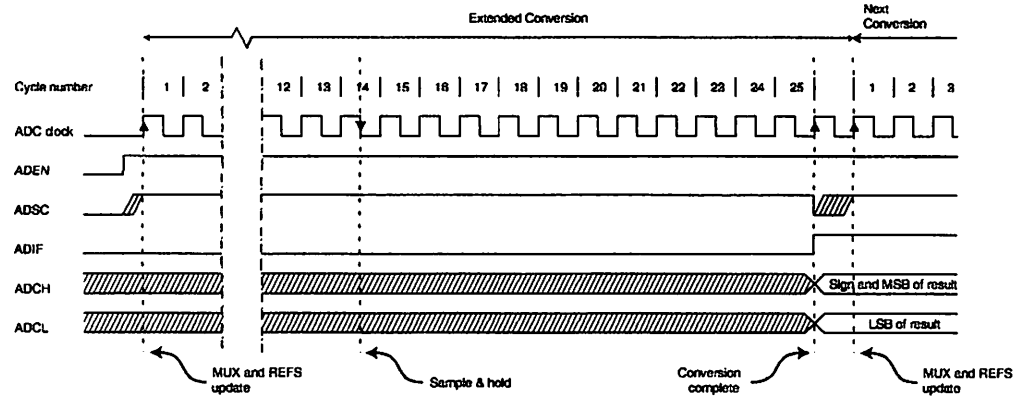


Figure 48. ADC Timing Diagram, Single Conversion

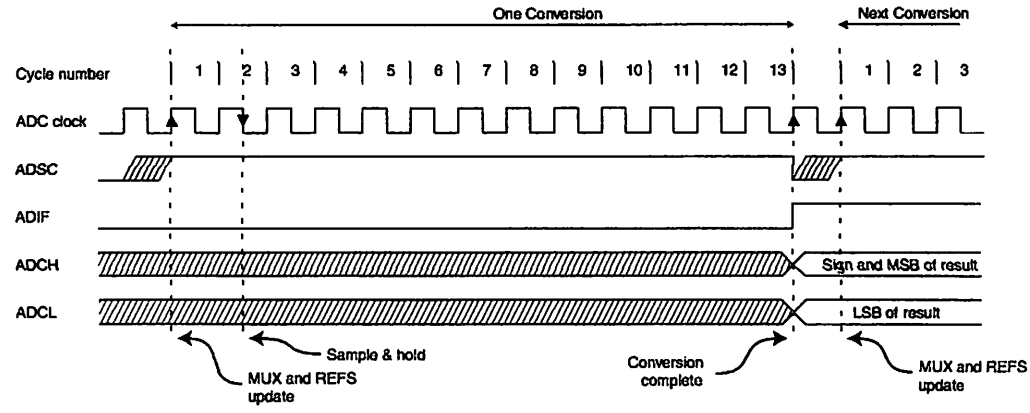


Figure 49. ADC Timing Diagram, Free Running Conversion

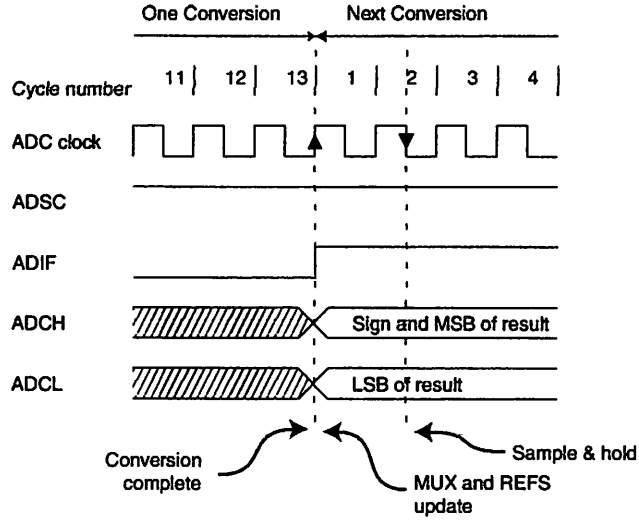


Table 26. ADC Conversion Time

Condition	Sample and Hold (Cycles from Start of Conversion)	Conversion Time (Cycles)	Conversion Time (µs)
Extended Conversion	14	25	125 - 500
Normal Conversion	14	26	130 - 520

C Noise Canceler ıction

The ADC features a noise canceler that enables conversion during Idle Mode to reduce noise induced from the CPU core. To make use of this feature, the following procedure should be used:

1. Make sure that the ADC is enabled and is not busy converting. Single Conversion Mode must be selected and the ADC conversion complete interrupt must be enabled.

   ADEN = 1

   ADSC = 0

   ADFR = 0

   ADIE = 1

2. Enter Idle Mode. The ADC will start a conversion once the CPU has been halted.
3. If no other interrupts occur before the ADC conversion completes, the ADC interrupt will wake up the MCU and execute the ADC Conversion Complete Interrupt routine.

; Multiplexer Select ister – ADMUX

Bit	7	6	5	4	3	2	1	0	
$07 ($27)	–	–	–	–	–	MUX2	MUX1	MUX0	ADMUX
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7..3 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and always read as zero.

- **Bits 2..0 – MUX2..MUX0: Analog Channel Select Bits 2-0**

The value of these three bits selects which analog input ADC7..0 is connected to the ADC. See Table 27 for details.

If these bits are changed during a conversion, the change will not go into effect until this conversion is complete (ADIF in ADCSR is set).

Table 27. Input Channel Selections

MUX2.0	Single-ended Input
000	ADC0
001	ADC1
010	ADC2
011	ADC3
100	ADC4
101	ADC5
110	ADC6
111	ADC7

; Control and Status ister – ADCSR

Bit	7	6	5	4	3	2	1	0	
$06 ($26)	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – ADEN: ADC Enable**

Writing a logical "1" to this bit enables the ADC. By clearing this bit to zero, the ADC is turned off. Turning the ADC off while a conversion is in progress will terminate this conversion.

- **Bit 6 – ADSC: ADC Start Conversion**

In Single Conversion Mode, a logical "1" must be written to this bit to start each conversion. In Free Running Mode, a logical "1" must be written to this bit to start the first conversion. The first time ADSC has been written after the ADC has been enabled or if ADSC is written at the same time as the ADC is enabled, an extended conversion will precede the initiated conversion. This extended conversion performs initialization of the ADC.

ADSC will read as one as long as a conversion is in progress. When the conversion is complete, it returns to zero. When a extended conversion precedes a real conversion, ADSC will stay high until the real conversion completes. Writing a "0" to this bit has no effect.

- **Bit 5 – ADFR: ADC Free Running Select**

When this bit is set (one), the ADC operates in Free Running Mode. In this mode, the ADC samples and updates the data registers continuously. Clearing this bit (zero) will terminate Free Running Mode.

- **Bit 4 – ADIF: ADC Interrupt Flag**

This bit is set (one) when an ADC conversion completes and the data registers are updated. The ADC Conversion Complete interrupt is executed if the ADIE bit and the I-bit in SREG are set (one). ADIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ADIF is cleared by writing a logical "1" to the flag. Beware that if doing a read-modify-write on ADCSR, a pending interrupt can be disabled. This also applies if the SBI and CBI instructions are used.

- **Bit 3 – ADIE: ADC Interrupt Enable**

When this bit is set (one) and the I-bit in SREG is set (one), the ADC Conversion Complete interrupt is activated.

- **Bits 2..0 – ADPS2..ADPS0: ADC Prescaler Select Bits**

These bits determine the division factor between the XTAL frequency and the input clock to the ADC.

Table 28. ADC Prescaler Selections

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

; Data Register – ADCL
) ADCH

Bit	15	14	13	12	11	10	9	8	
$05 ($25)	–	–	–	–	–	–	ADC9	ADC8	ADCH
$04 ($24)	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

When an ADC conversion is complete, the result is found in these two registers.

When ADCL is read, the ADC Data Register is not updated until ADCH is read. Consequently, it is essential that both registers are read and that ADCL is read before ADCH.

- **ADC9..0: ADC Conversion result**

These bits represent the result from the conversion. $000 represents analog ground and $3FF represents the selected reference voltage minus one LSB.

ınning Multiple annels

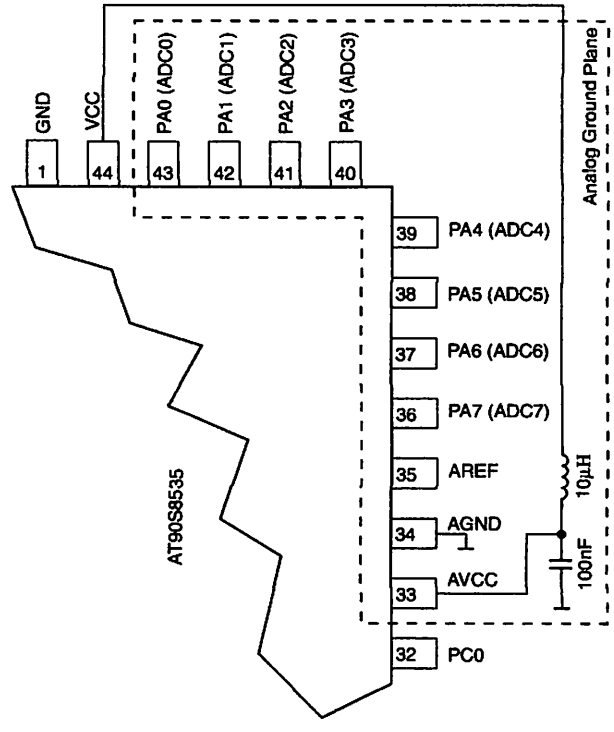
Since change of analog channel always is delayed until a conversion is finished, the Free Running Mode can be used to scan multiple channels without interrupting the converter. Typically, the ADC Conversion Complete interrupt will be used to perform the channel shift. However, the user should take the following fact into consideration: The interrupt triggers once the result is ready to be read. In Free Running Mode, the next conversion will start immediately when the interrupt triggers. If ADMUX is changed after the interrupt triggers, the next conversion has already started and the old setting is used.

C Noise Canceling hniques

Digital circuitry inside and outside the AT90S8535 generates EMI that might affect the accuracy of analog measurements. If conversion accuracy is critical, the noise level can be reduced by applying the following techniques:

1. The analog part of the AT90S8535 and all analog components in the application should have a separate analog ground plane on the PCB. This ground plane is connected to the digital ground plane via a single point on the PCB.
2. Keep analog signal paths as short as possible. Make sure analog tracks run over the analog ground plane and keep them well away from high-speed switching digital tracks.
3. The AV_{CC} pin on the AT90S8535 should be connected to the digital V_{CC} supply voltage via an LC network as shown in Figure 50.
4. Use the ADC noise canceler function to reduce induced noise from the CPU.
5. If some Port A pins are used as digital outputs, it is essential that these do not switch while a conversion is in progress.

Figure 50. ADC Power Connections



C Characteristics

-40°C to 85°C

mbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution			10		Bits
	Absolute accuracy	VREF = 4V ADC clock = 200 kHz		1	2	LSB
	Absolute accuracy	VREF = 4V ADC clock = 1 MHz		4		LSB
	Absolute accuracy	VREF = 4V ADC clock = 2 MHz		16		LSB
	Integral Non-linearity	V_{REF} > 2V		0.5		LSB
	Differential Non-linearity	V_{REF} > 2V		0.5		LSB
	Zero Error (Offset)			1		LSB
	Conversion Time		65		260	µs
	Clock Frequency		50		200	kHz
AV_{CC}	Analog Supply Voltage		V_{CC} - 0.3(1)		V_{CC} + 0.3(2)	V
V_{REF}	Reference Voltage		2		AV_{CC}	V
R_{REF}	Reference Input Resistance		6	10	13	kΩ
V_{IN}	Input Voltage		AGND		AREF	V
R_{AIN}	Analog Input Resistance			100		MΩ

s: 1. Minimum for AV_{CC} is 2.7V.
2. Maximum for AV_{CC} is 6.0V.

Ports

All AVR ports have true read-modify-write functionality when used as general digital I/O ports. This means that the direction of one port pin can be changed without unintentionally changing the direction of any other pin with the SBI and CBI instructions. The same applies for changing drive value (if configured as output) or enabling/disabling of pull-up resistors (if configured as input).

t A

Port A is an 8-bit bi-directional I/O port.

Three I/O memory address locations are allocated for Port A, one each for the Data Register – PORTA, $1B($3B), Data Direction Register – DDRA, $1A($3A) and the Port A Input Pins – PINA, $19($39). The Port A Input Pins address is read-only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port A output buffers can sink 20 mA and thus drive LED displays directly. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

Port A has an alternate function as analog inputs for the ADC. If some Port A pins are configured as outputs, it is essential that these do not switch when a conversion is in progress. This might corrupt the result of the conversion.

During Power-down mode, the Schmitt trigger of the digital input is disconnected. This allows analog signals that are close to $V_{CC}/2$ to be present during power-down without causing excessive power consumption.

A Data Register – PORTA

Bit	7	6	5	4	3	2	1	0	
$1B ($3B)	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	PORTA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

A Data Direction Register)RA

Bit	7	6	5	4	3	2	1	0	
$1A ($3A)	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

A Input Pins Address –

Bit	7	6	5	4	3	2	1	0	
$19 ($39)	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	PINA
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

The Port A Input Pins address (PINA) is not a register; this address enables access to the physical value on each Port A pin. When reading PORTA, the Port A Data Latch is read and when reading PINA, the logical values present on the pins are read.

A as General Digital I/O

All eight pins in Port A have equal functionality when used as digital I/O pins.

PAn, general I/O pin: The DDAn bit in the DDRA register selects the direction of this pin. If DDAn is set (one), PAn is configured as an output pin. If DDAn is cleared (zero), PAn is configured as an input pin. If PORTAn is set (one) when the pin is configured as an input pin, the MOS pull-up resistor is activated. To switch the pull-up resistor off, the PORTAn has to be cleared (zero) or the pin has to be configured as an output pin.The port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Table 29. DDAn Effects on Port A Pins

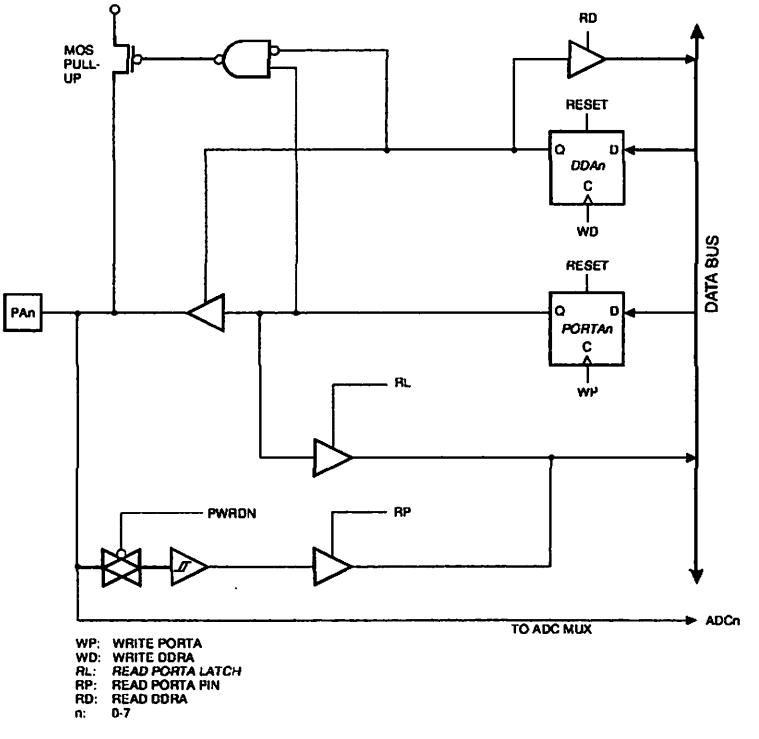
DDAn	PORTAn	I/O	Pull-up	Comment
0	*0*	*Input*	*No*	*Tri-state (high-Z)*
0	1	Input	Yes	PAn will source current if ext. pulled low
1	0	Output	No	Push-pull Zero Output
1	1	Output	No	Push-pull One Output

Note: n: 7,6...0, pin number.

A Schematics

Note that all port pins are synchronized. The synchronization latch is, however, not shown in the figure.

Figure 51. Port A Schematic Diagrams (Pins PA0 - PA7)



t B

Port B is an 8-bit bi-directional I/O port.

Three I/O memory address locations are allocated for the Port B, one each for the Data Register – PORTB, $18($38), Data Direction Register – DDRB, $17($37) and the Port B Input Pins – PINB, $16($36). The Port B Input Pins address is read-only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port B output buffers can sink 20 mA and thus drive LED displays directly. When pins PB0 to PB7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

The Port B pins with alternate functions are shown in Table 30.

Table 30. Port B Pin Alternate Functions

Port Pin	Alternate Functions
PB0	T0 (Timer/Counter0 External Counter Input)
PB1	T1 (Timer/Counter1 External Counter Input)
PB2	AIN0 (Analog Comparator Positive Input)
PB3	AIN1 (Analog Comparator Negative Input)
PB4	$\overline{SS}$ (SPI Slave Select Input)
PB5	MOSI (SPI Bus Master Output/Slave Input)
PB6	MISO (SPI Bus Master Input/Slave Output)
PB7	SCK (SPI Bus Serial Clock)

When the pins are used for the alternate function, the DDRB and PORTB registers have to be set according to the alternate function description.

B Data Register – PORTB

Bit	7	6	5	4	3	2	1	0	
$18 ($38)	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	PORTB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

B Data Direction Register)RB

Bit	7	6	5	4	3	2	1	0	
$17 ($37)	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

B Input Pins Address – 3

Bit	7	6	5	4	3	2	1	0	
$16 ($36)	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	PINB
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

The Port B Input Pins address (PINB) is not a register and this address enables access to the physical value on each Port B pin. When reading PORTB, the Port B Data Latch is read and when reading PINB, the logical values present on the pins are read.

: B As General Digital I/O

All eight pins in Port B have equal functionality when used as digital I/O pins.

PBn, general I/O pin: The DDBn bit in the DDRB register selects the direction of this pin. If DDBn is set (one), PBn is configured as an output pin. If DDBn is cleared (zero), PBn is configured as an input pin. If PORTBn is set (one) when the pin is configured as an input pin, the MOS pull-up resistor is activated. To switch the pull-up resistor off, the PORTBn has to be cleared (zero) or the pin has to be configured as an output pin. The port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Table 31. DDBn Effects on Port B Pins

DDBn	PORTBn	I/O	Pull-up	Comment
0	*0*	*Input*	*No*	*Tri-state (high-Z)*
0	1	Input	Yes	PBn will source current if ext. pulled low
1	0	Output	No	Push-pull Zero Output
1	1	Output	No	Push-pull One Output

Note: n: 7,6...0, pin number.

rnate Functions of Port B

The alternate pin configuration is as follows:

- **SCK – Port B, Bit 7**

SCK: Master clock output, slave clock input pin for SPI channel. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB7. When the SPI is enabled as a master, the data direction of this pin is controlled by DDB7. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB7 bit. See the description of the SPI port for further details.

- **MISO – Port B, Bit 6**

MISO: Master data input, slave data output pin for SPI channel. When the SPI is enabled as a master, this pin is configured as an input regardless of the setting of DDB6. When the SPI is enabled as a slave, the data direction of this pin is controlled by DDB6. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB6 bit. See the description of the SPI port for further details.

- **MOSI – Port B, Bit 5**

MOSI: SPI Master data output, slave data input for SPI channel. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB5. When the SPI is enabled as a master, the data direction of this pin is controlled by DDB5. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB5 bit. See the description of the SPI port for further details.

- **$\overline{SS}$ – Port B, Bit 4**

$\overline{SS}$: Slave port select input. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB4. As a slave, the SPI is activated when this pin is driven low. When the SPI is enabled as a master, the data direction of this pin is controlled by DDB4. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB4 bit. See the description of the SPI port for further details.

- **AIN1 – Port B, Bit 3**

AIN1, Analog Comparator Negative Input. When configured as an input (DDB3 is cleared [zero]) and with the internal MOS pull-up resistor switched off (PB3 is cleared [zero]), this pin also serves as the negative input of the on-chip Analog Comparator. During Power-down mode, the Schmitt trigger of the digital input is disconnected. This

allows analog signals that are close to $V_{CC}/2$ to be present during power-down without causing excessive power consumption.

- **AIN0 – Port B, Bit 2**

AIN0, Analog Comparator Positive Input. When configured as an input (DDB2 is cleared [zero]) and with the internal MOS pull-up resistor switched off (PB2 is cleared [zero]), this pin also serves as the positive input of the on-chip Analog Comparator. During Power-down mode, the Schmitt trigger of the digital input is disconnected. This allows analog signals that are close to $V_{CC}/2$ to be present during power-down without causing excessive power consumption.

- **T1 – Port B, Bit 1**

T1, Timer/Counter1 counter source. See the timer description for further details.

- **T0 – Port B, Bit 0**

T0: Timer/Counter0 counter source. See the timer description for further details.

B Schematics

Note that all port pins are synchronized. The synchronization latches are, however, not shown in the figures.

Figure 52. Port B Schematic Diagram (Pins PB0 and PB1)

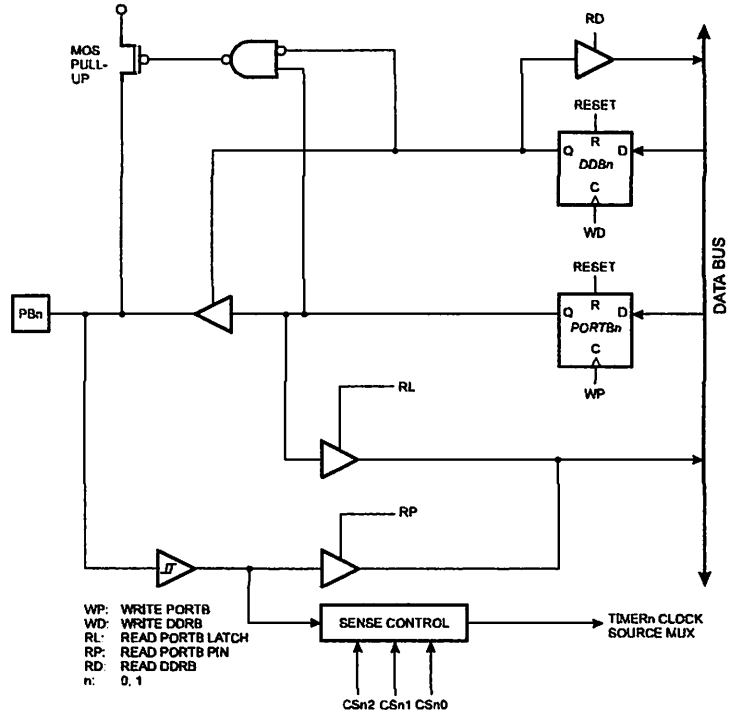


Figure 53. Port B Schematic Diagram (Pins PB2 and PB3)

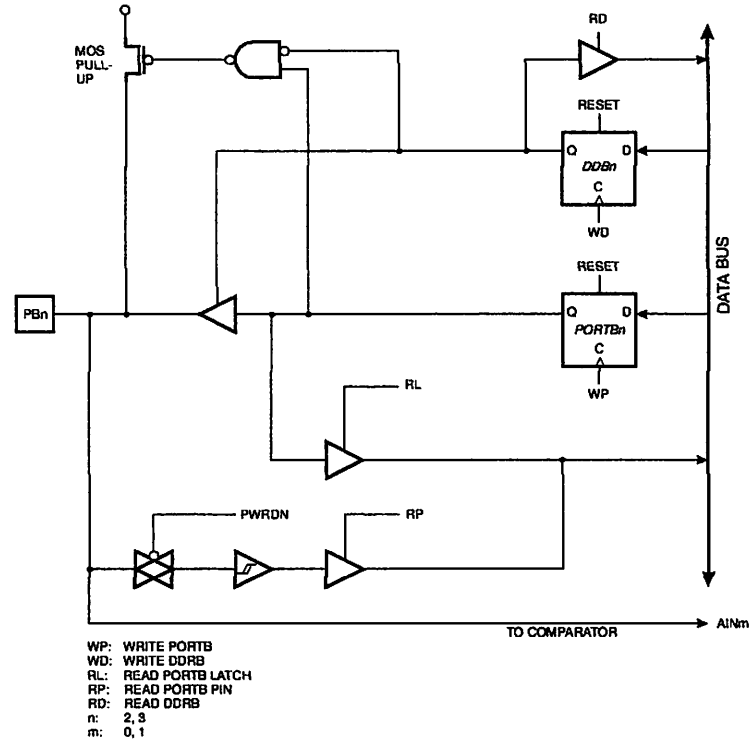


Figure 54. Port B Schematic Diagram (Pin PB4)

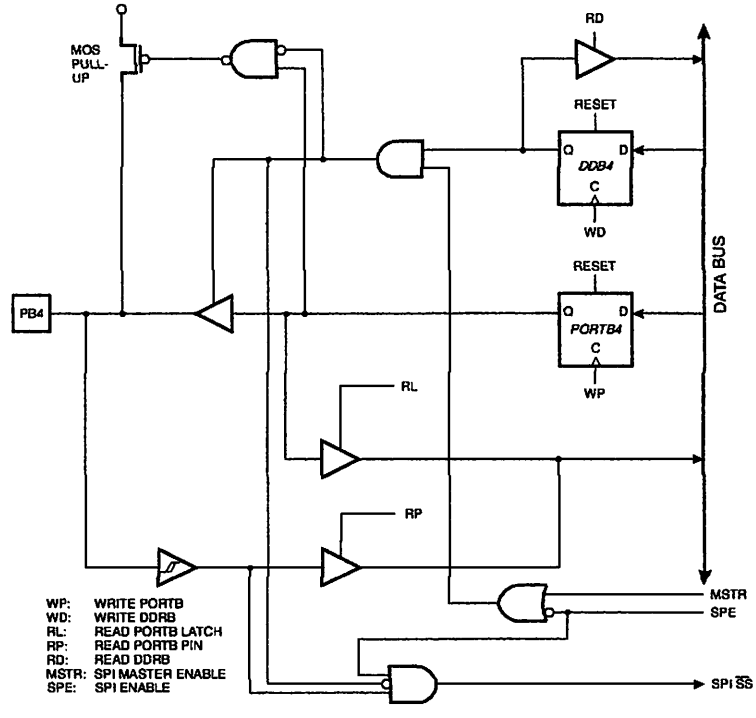


Figure 55. Port B Schematic Diagram (Pin PB5)

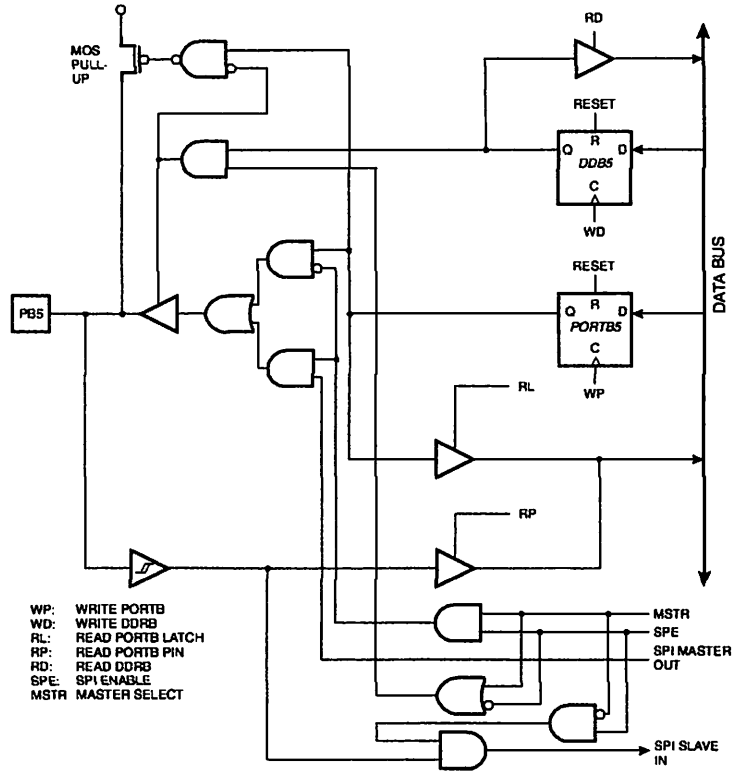


Figure 56. Port B Schematic Diagram (Pin PB6)

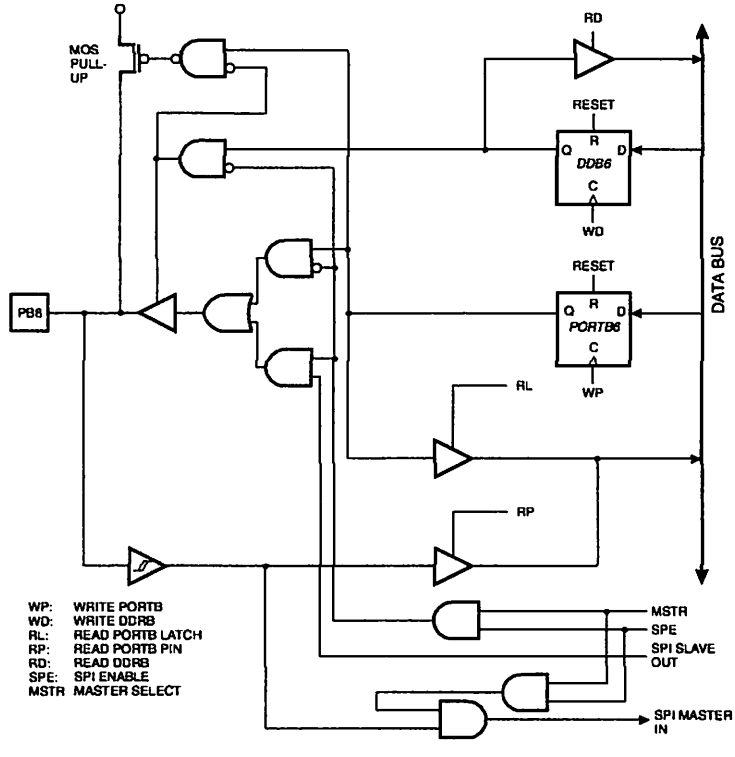
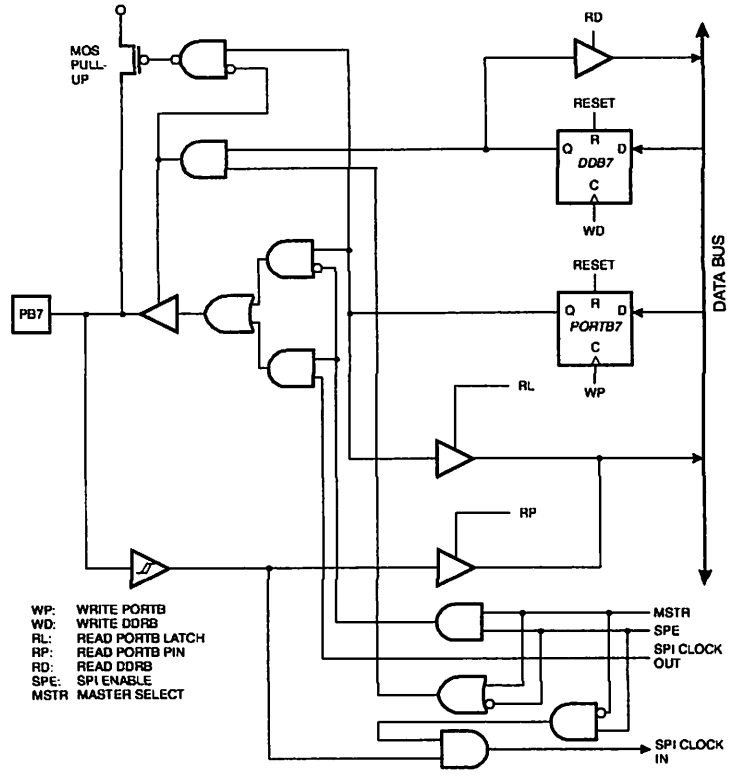


Figure 57. Port B Schematic Diagram (Pin PB7)



t C

Port C is an 8-bit bi-directional I/O port.

Three I/O memory address locations are allocated for the Port C, one each for the Data Register – PORTC, $15($35), Data Direction Register – DDRC, $14($34) and the Port C Input Pins – PINC, $13($33). The Port C Input Pins address is read-only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port C output buffers can sink 20 mA and thus drive LED displays directly. When pins PC0 to PC7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

: C Data Register – PORTC

Bit	7	6	5	4	3	2	1	0	
$15 ($35)	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	PORTC
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

: C Data Direction Register)RC

Bit	7	6	5	4	3	2	1	0	
$14 ($34)	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

: C Input Pins Address – C

Bit	7	6	5	4	3	2	1	0	
$13 ($33)	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	PINC
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

The Port C Input Pins address (PINC) is not a register; this address enables access to the physical value on each Port C pin. When reading PORTC, the Port C Data Latch is read and when reading PINC, the logical values present on the pins are read.

: C As General Digital I/O

All eight pins in Port C have equal functionality when used as digital I/O pins.

PCn, general I/O pin: The DDCn bit in the DDRC register selects the direction of this pin. If DDCn is set (one), PCn is configured as an output pin. If DDCn is cleared (zero), PCn is configured as an input pin. If PORTCn is set (one) when the pin is configured as an input pin, the MOS pull-up resistor is activated. To switch the pull-up resistor off, PORTCn has to be cleared (zero) or the pin has to be configured as an output pin.The port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Table 32. DDCn Effects on Port C Pins

DDCn	PORTCn	I/O	Pull-up	Comment
0	0	Input	No	Tri-state (high-Z)
0	1	Input	Yes	PCn will source current if ext. pulled low
1	0	Output	No	Push-pull Zero Output
1	1	Output	No	Push-pull One Output

Note: n: 7...0, pin number

rnate Functions of Port C

When the AS2 bit in ASSR is set (one) to enable asynchronous clocking of Timer/Counter2, pins PC6 and PC7 are disconnected from the port. In this mode, a crystal oscillator is connected to the pins and the pins cannot be used as I/O pins.

t C Schematics

Note that all port pins are synchronized. The synchronization latch is, however, not shown in the figure.

Figure 58. Port C Schematic Diagram (Pins PC0 - PC5)

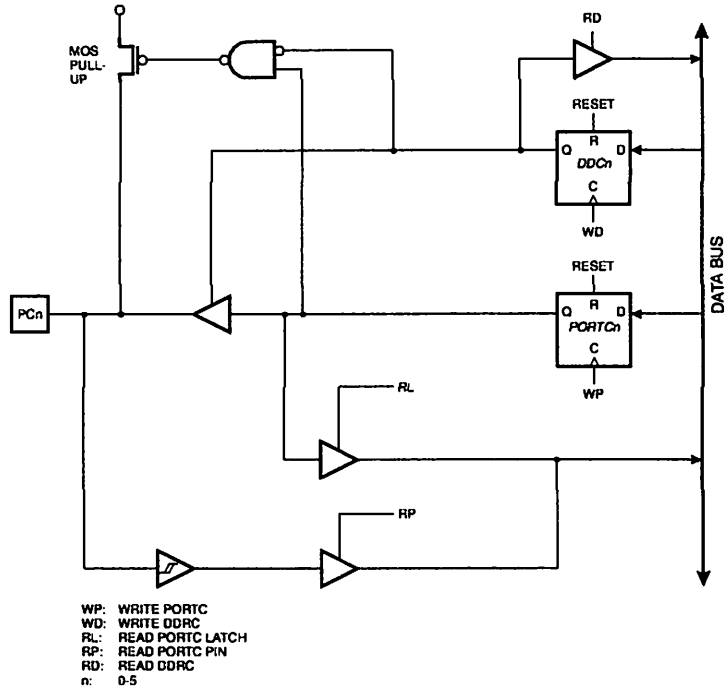


Figure 59. Port C Schematic Diagram (Pins PC6)

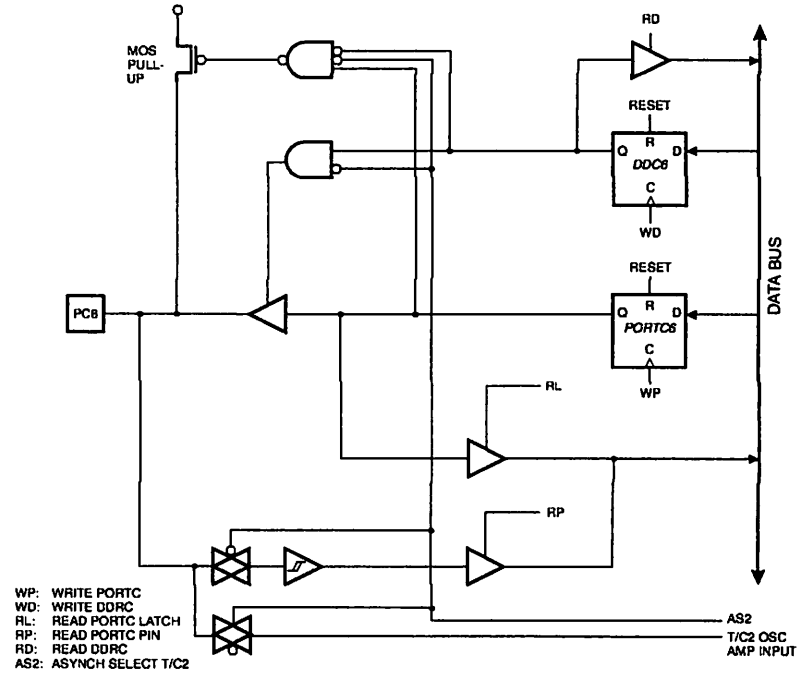
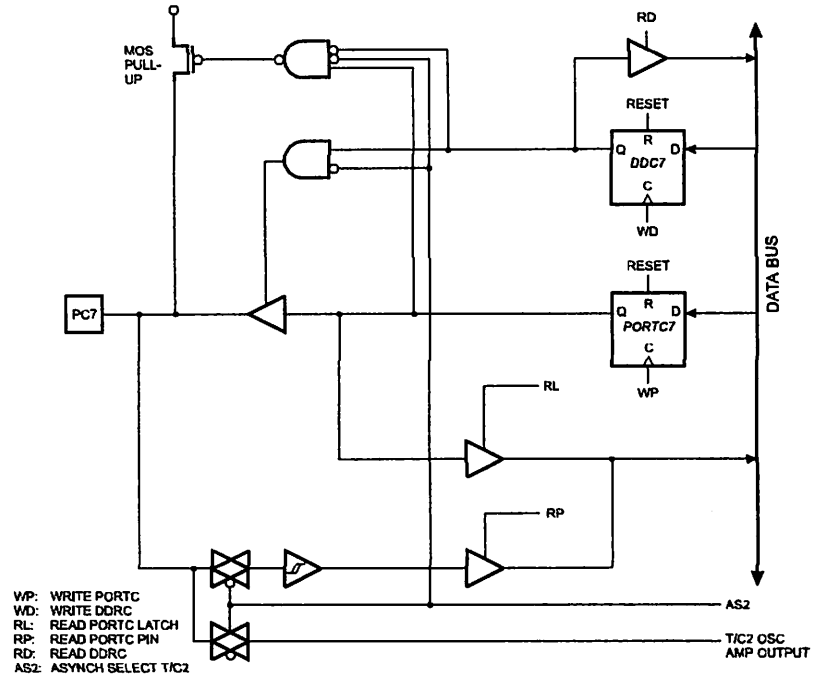


Figure 60. Port C Schematic Diagram (Pins PC7)



t D

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors.

Three I/O memory address locations are allocated for Port D, one each for the Data Register – PORTD, $12($32), Data Direction Register – DDRD, $11($31) and the Port D Input Pins – PIND, $10($30). The Port D Input Pins address is read-only, while the Data Register and the Data Direction Register are read/write.

The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. Some Port D pins have alternate functions as shown in Table 33.

Table 33. Port D Pin Alternate Functions

Port Pin	Alternate Function
PD0	RXD (UART Input line)
PD1	TXD (UART Output line)
PD2	INT0 (External interrupt 0 input)
PD3	INT1 (External interrupt 1 input)
PD4	OC1B (Timer/Counter1 output compareB match output)
PD5	OC1A (Timer/Counter1 output compareA match output)
PD6	ICP (Timer/Counter1 input capture pin)
PD7	OC2 (Timer/Counter2 output compare match output)

D Data Register – PORTD

Bit	7	6	5	4	3	2	1	0	
$12 ($32)	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	PORTD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

D Data Direction Register
)RD

Bit	7	6	5	4	3	2	1	0	
$11 ($31)	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

: D Input Pins Address –
)

Bit	7	6	5	4	3	2	1	0	
$10 ($30)	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	PIND
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

The Port D Input Pins address (PIND) is not a register; this address enables access to the physical value on each Port D pin. When reading PORTD, the Port D Data Latch is read and when reading PIND, the logical values present on the pins are read.

: D As General Digital I/O

PDn, general I/O pin: The DDDn bit in the DDRD register selects the direction of this pin. If DDDn is set (one), PDn is configured as an output pin. If DDDn is cleared (zero), PDn is configured as an input pin. If PDn is set (one) when configured as an input pin, the MOS pull-up resistor is activated. To switch the pull-up resistor off, the PDn has to be cleared (zero) or the pin has to be configured as an output pin.The port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Table 34. DDDn Bits on Port D Pins

DDDn	PORTDn	I/O	Pull-up	Comment
0	*0*	*Input*	*No*	*Tri-state (high-Z)*
0	1	Input	Yes	PDn will source current if ext. pulled low
1	0	Output	No	Push-pull Zero Output
1	1	Output	No	Push-pull One Output

Note: n: 7,6...0, pin number.

rnate Functions of Port D

- **OC2 – Port D, Bit 7**

OC2, Timer/Counter2 output compare match output: The PD7 pin can serve as an external output for the Timer/Counter2 output compare. The pin has to be configured as an output (DDD7 set [one]) to serve this function. See the timer description on how to enable this function. The OC2 pin is also the output pin for the PWM mode timer function.

- **ICP – Port D, Bit 6**

ICP – Input Capture Pin: The PD6 pin can act as an input capture pin for Timer/Counter1. The pin has to be configured as an input (DDD6 cleared [zero]) to serve this function. See the timer description on how to enable this function.

- **OC1A – Port D, Bit 5**

OC1A, Output compare matchA output: The PD5 pin can serve as an external output for the Timer/Counter1 output compareA. The pin has to be configured as an output (DDD5 set [one]) to serve this function. See the timer description on how to enable this function. The OC1A pin is also the output pin for the PWM mode timer function.

- **OC1B – Port D, Bit 4**

OC1B, Output compare matchB output: The PD4 pin can serve as an external output for the Timer/Counter1 output compareB. The pin has to be configured as an output (DDD4 set [one]) to serve this function. See the timer description on how to enable this function. The OC1B pin is also the output pin for the PWM mode timer function.

- **INT1 – Port D, Bit 3**

INT1, External Interrupt source 1: The PD3 pin can serve as an external interrupt source to the MCU. See the interrupt description for further details and how to enable the source.

- **INT0 – Port D, Bit 2**

INT0, External Interrupt source 0: The PD2 pin can serve as an external interrupt source to the MCU. See the interrupt description for further details and how to enable the source.

- **TXD – Port D, Bit 1**

Transmit Data (data output pin for the UART). When the UART Transmitter is enabled, this pin is configured as an output, regardless of the value of DDD1.

- **RXD – Port D, Bit 0**

Receive Data (data input pin for the UART). When the UART Receiver is enabled, this pin is configured as an input, regardless of the value of DDD0. When the UART forces this pin to be an input, a logical "1" in PORTD0 will turn on the internal pull-up.

D Schematics

Note that all port pins are synchronized. The synchronization latches are, however, not shown in the figures.

Figure 61. Port D Schematic Diagram (Pin PD0)

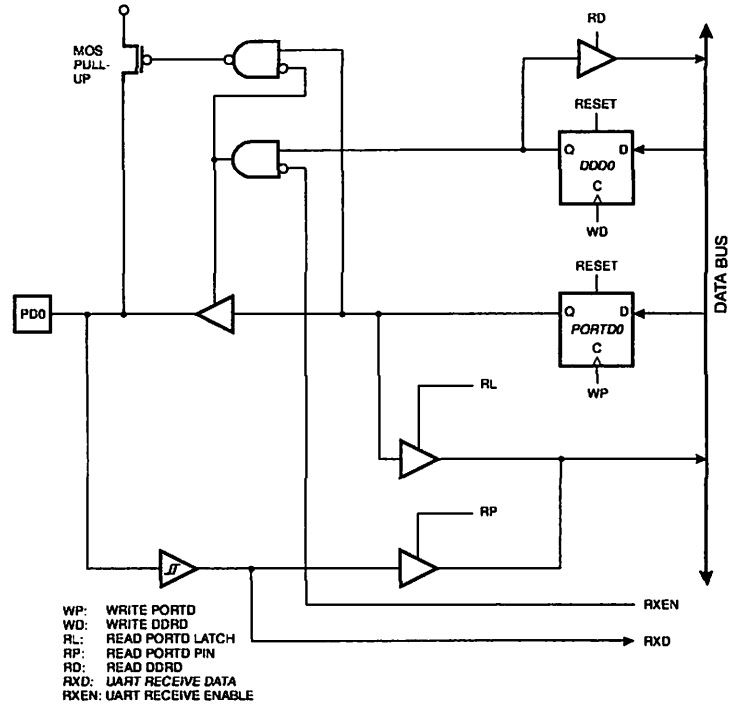


Figure 62. Port D Schematic Diagram (Pin PD1)

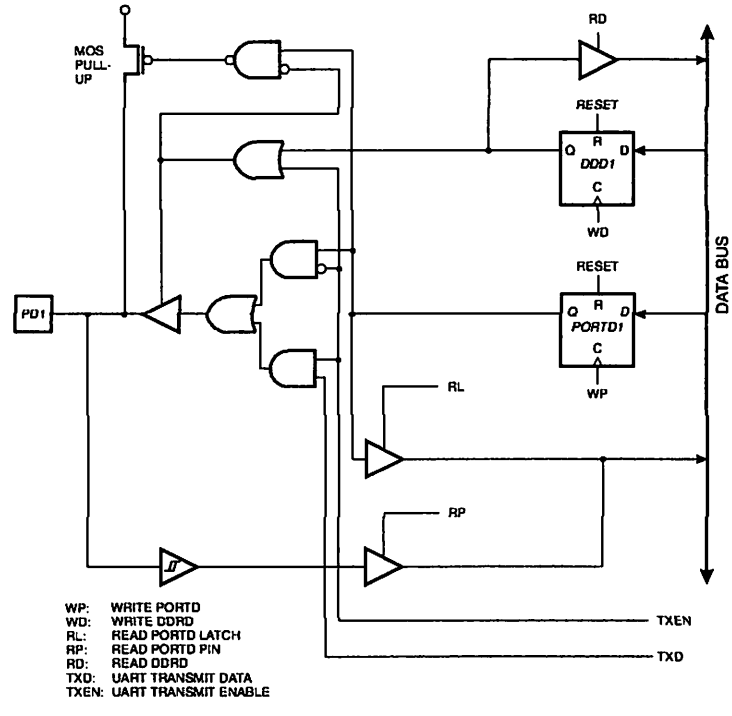


Figure 63. Port D Schematic Diagram (Pins PD2 and PD3)

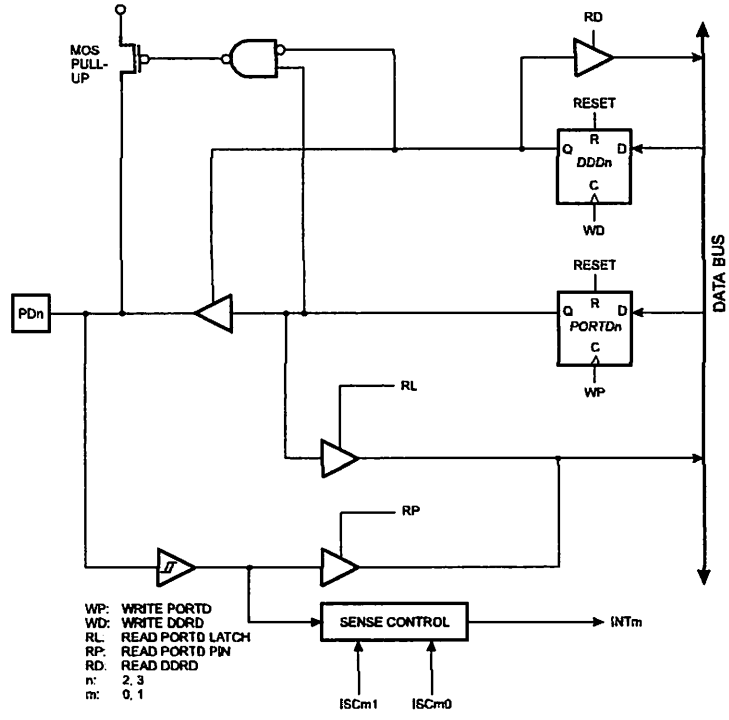


Figure 64. Port D Schematic Diagram (Pins PD4 and PD5)

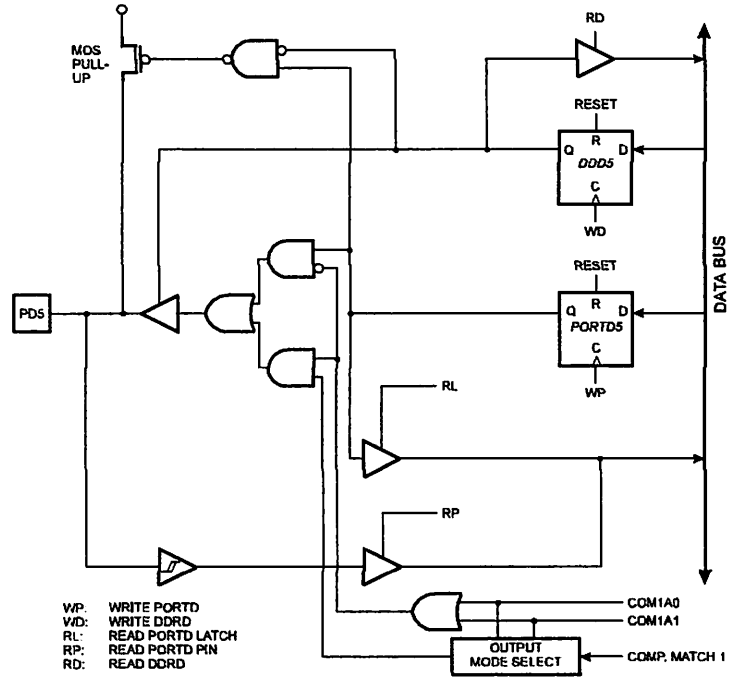


Figure 65. Port D Schematic Diagram (Pin PD6)

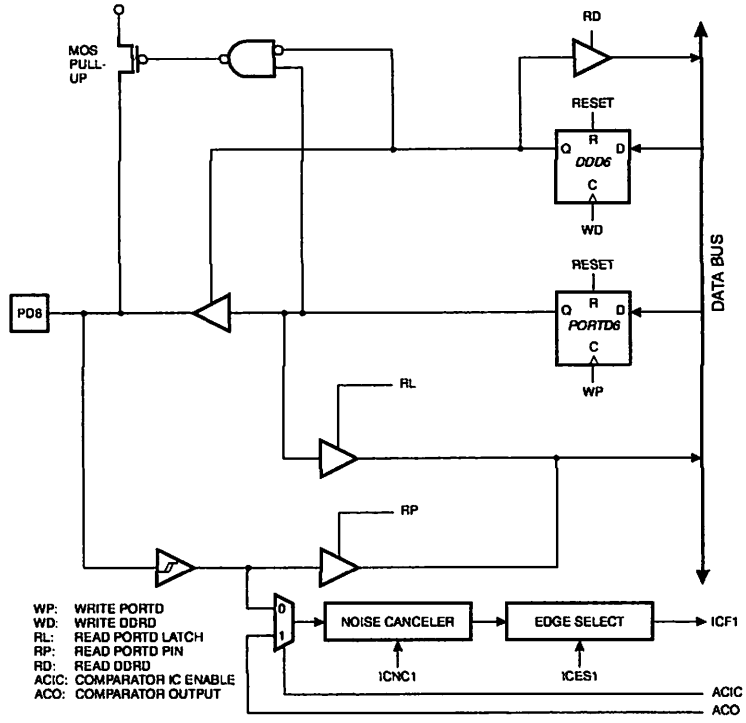
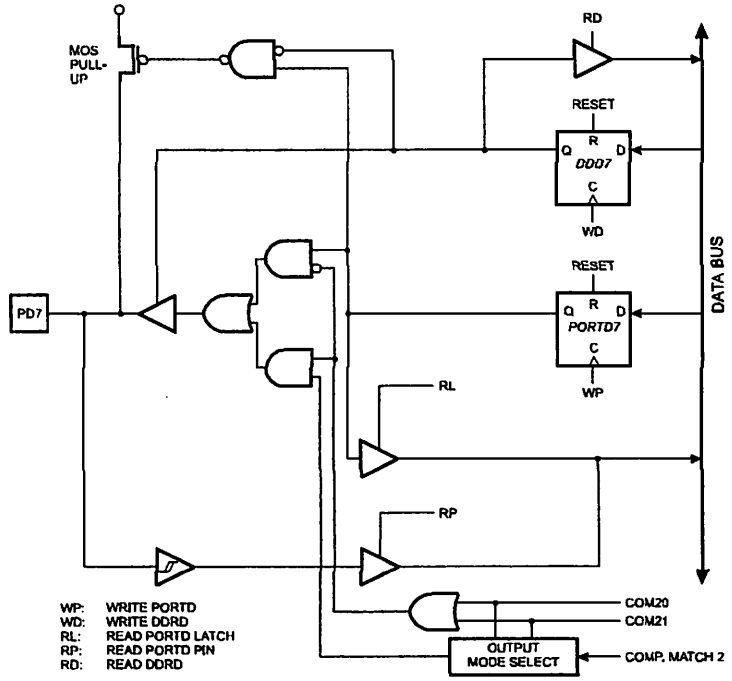


Figure 66. Port D Schematic Diagram (Pin PD7)



mory
›gramming

›gram and Data mory Lock Bits

The AT90S8535 MCU provides two Lock bits that can be left unprogrammed ("1") or can be programmed ("0") to obtain the additional features listed in Table 35. The Lock bits can only be erased with the Chip Erase command.

Table 35. Lock Bit Protection Modes

Memory Lock Bits			
Mode	**LB1**	**LB2**	**Protection Type**
1	1	1	No memory lock features enabled.
2	0	1	Further programming of the Flash and EEPROM is disabled.(1)
3	0	0	Same as mode 2 and verify is also disabled.

Note: 1. In Parallel Mode, further programming of the Fuse bits is also disabled. Program the Fuse bits before programming the Lock bits.

›e Bits

The AT90S8535 has two Fuse bits, SPIEN and FSTRT.

- When the SPIEN Fuse is programmed ("0"), Serial Program and Data Downloading is enabled. Default value is programmed ("0"). The SPIEN Fuse is not accessible in Serial Programming Mode.
- When the FSTRT Fuse is programmed ("0"), the short start-up time is selected. Default value is unprogrammed ("1").

The status of the Fuse bits is not affected by Chip Erase.

nature Bytes

All Atmel microcontrollers have a three-byte signature code that identifies the device. This code can be read in both Serial and Parallel modes. The three bytes reside in a separate address space.

1. $000: $1E (indicates manufactured by Atmel)
2. *$001: $93 (indicates 8K bytes Flash memory)*
3. $002: $03 (indicates AT90S8535 device when signature byte $001 is $93)

Note: 1. When both Lock bits are programmed (lock mode 3), the signature bytes cannot be read in Serial Mode. Reading the signature bytes will return: $00, $01 and $02.

›gramming the Flash ı EEPROM

Atmel's AT90S8535 offers 8K bytes of in-system reprogrammable Flash program memory and 512 bytes of EEPROM data memory.

The AT90S8535 is shipped with the On-chip Flash program and EEPROM data memory arrays in the erased state (i.e., contents = $FF) and ready to be programmed. This device supports a high-voltage (12V) Parallel Programming Mode and a low-voltage Serial Programming Mode. The +12V is used for programming enable only and no current of significance is drawn by this pin. The Serial Programming Mode provides a convenient way to download program and data into the AT90S8535 inside the user's system.

The program and data memory arrays on the AT90S8535 are programmed byte-by-byte in either programming mode. For the EEPROM, an auto-erase cycle is provided within the self-timed write instruction in the Serial Programming Mode.

During programming, the supply voltage must be in accordance with Table 36.

Table 36. Supply Voltage during Programming

Part	Serial Programming	Parallel Programming
AT90S8535	4.0 - 6.0V	4.5 - 5.5V
AT90LS8535	2.7 - 6.0V	4.5 - 5.5V

allel Programming

This section describes how to parallel program and verify Flash program memory, EEPROM data memory, Lock bits and Fuse bits in the AT90S8535.

ıal Names

In this section, some pins of the AT90S8535 are referenced by signal names describing their function during parallel programming. See Figure 67 and Table 37. Pins not described in Table 37 are referenced by pin name.

The XA1/XA0 pins determine the action executed when the XTAL1 pin is given a positive pulse. The bit coding are shown in Table 38.

When pulsing $\overline{WR}$ or $\overline{OE}$, the command loaded determines the action executed. The command is a byte where the different bits are assigned functions as shown in Table 39.

Figure 67. Parallel Programming

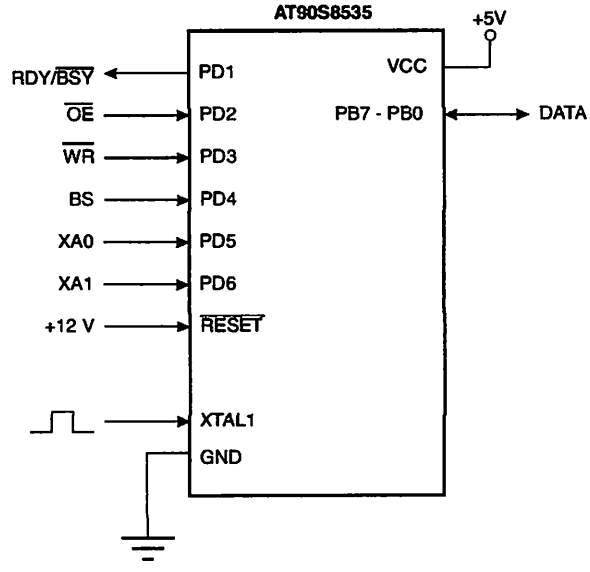


Table 37. Pin Name Mapping

Signal Name in Programming Mode	Pin Name	I/O	Function
RDY/$\overline{BSY}$	PD1	O	0: Device is busy programming, 1: Device is ready for new command
$\overline{OE}$	PD2	I	Output Enable (Active low)
$\overline{WR}$	PD3	I	Write Pulse (Active low)
BS	PD4	I	Byte Select ("0" selects low byte, "1" selects high byte)
XA0	PD5	I	XTAL Action Bit 0
XA1	PD6	I	XTAL Action Bit 1
DATA	PB7 - 0	I/O	Bi-directional Data Bus (Output when $\overline{OE}$ is low)

Table 38. XA1 and XA0 Coding

XA1	XA0	Action when XTAL1 is Pulsed
0	0	Load Flash or EEPROM Address (high or low address byte determined by BS)
0	1	Load Data (High or low data byte for Flash determined by BS)
1	0	Load Command
1	1	No Action, Idle

Table 39. Command Byte Bit Coding

Command Byte	Command Executed
1000 0000	Chip Erase
0100 0000	Write Fuse Bits
0010 0000	Write Lock Bits
0001 0000	Write Flash
0001 0001	Write EEPROM
0000 1000	Read Signature Bytes
0000 0100	Read Lock and Fuse Bits
0000 0010	Read Flash
0000 0011	Read EEPROM

ɐr Programming Mode

The following algorithm puts the device in Parallel Programming Mode:

1. Apply supply voltage according to Table 36, between V_{CC} and GND.
2. Set the $\overline{RESET}$ and BS pin to "0" and wait at least 100 ns.
3. Apply 11.5 - 12.5V to $\overline{RESET}$. Any activity on BS within 100 ns after +12V has been applied to $\overline{RESET}$, will cause the device to fail entering programming mode.

› Erase

The Chip Erase command will erase the Flash and EEPROM memories and the Lock bits. The Lock bits are not reset until the Flash and EEPROM have been completely erased. The Fuse bits are not changed. Chip Erase must be performed before the Flash or EEPROM is reprogrammed.

Load Command "Chip Erase":

1. Set XA1, XA0 to "10". This enables command loading.
2. Set BS to "0".
3. Set DATA to "1000 0000". This is the command for Chip Erase.
4. Give XTAL1 a positive pulse. This loads the command.
5. Give $\overline{WR}$ a t_{WLWH_CE}-wide negative pulse to execute Chip Erase. See Table 40 for t_{WLWH_CE} value. Chip Erase does not generate any activity on the RDY/$\overline{BSY}$ pin.

ɡramming the Flash

A: Load Command "Write Flash"

1. Set XA1, XA0 to "10". This enables command loading.
2. Set BS to "0".
3. Set DATA to "0001 0000". This is the command for Write Flash.
4. Give XTAL1 a positive pulse. This loads the command.

B: Load Address High Byte

1. Set XA1, XA0 to "00". This enables address loading.
2. Set BS to "1". This selects high byte.
3. Set DATA = Address high byte ($00 - $0F).
4. Give XTAL1 a positive pulse. This loads the address high byte.

C: Load Address Low Byte

1. Set XA1, XA0 to "00". This enables address loading.
2. Set BS to "0". This selects low byte.
3. Set DATA = Address low byte ($00 - $FF).
4. Give XTAL1 a positive pulse. This loads the address low byte.

D: Load Data Low Byte

1. Set XA1, XA0 to "01". This enables data loading.
2. Set DATA = Data low byte ($00 - $FF).
3. Give XTAL1 a positive pulse. This loads the data low byte.

E: Write Data Low Byte

1. Set BS to "0". This selects low data.
2. Give $\overline{WR}$ a negative pulse. This starts programming of the data byte. RDY/$\overline{BSY}$ goes low.
3. Wait until RDY/$\overline{BSY}$ goes high to program the next byte.

(See Figure 68 for signal waveforms.)

F: Load Data High Byte

1. Set XA1, XA0 to "01". This enables data loading.
2. Set DATA = Data high byte ($00 - $FF).
3. Give XTAL1 a positive pulse. This loads the data high byte.

G: Write Data High Byte

1. Set BS to "1". This selects high data.
2. Give $\overline{WR}$ a negative pulse. This starts programming of the data byte. RDY/$\overline{BSY}$ goes low.
3. Wait until RDY/$\overline{BSY}$ goes high to program the next byte.

(See Figure 69 for signal waveforms.)

The loaded command and address are retained in the device during programming. For efficient programming, the following should be considered:

- The command needs only be loaded once when writing or reading multiple memory locations.
- Address high byte needs only be loaded before programming a new 256-word page in the Flash.
- Skip writing the data value $FF, that is, the contents of the entire Flash and EEPROM after a Chip Erase.

These considerations also apply to EEPROM programming and Flash, EEPROM and signature byte reading.

Figure 68. Programming the Flash Waveforms

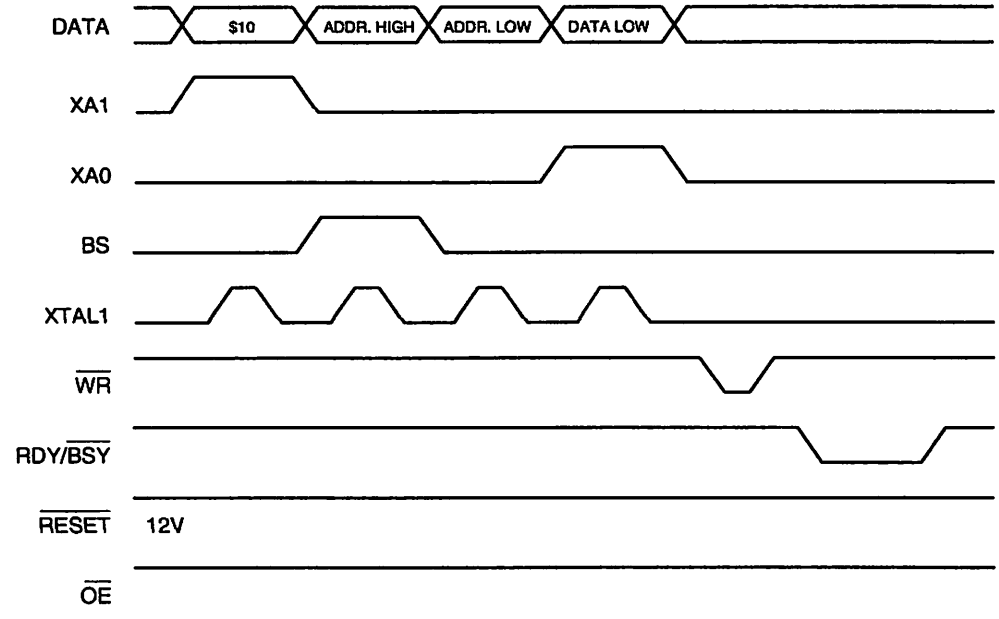
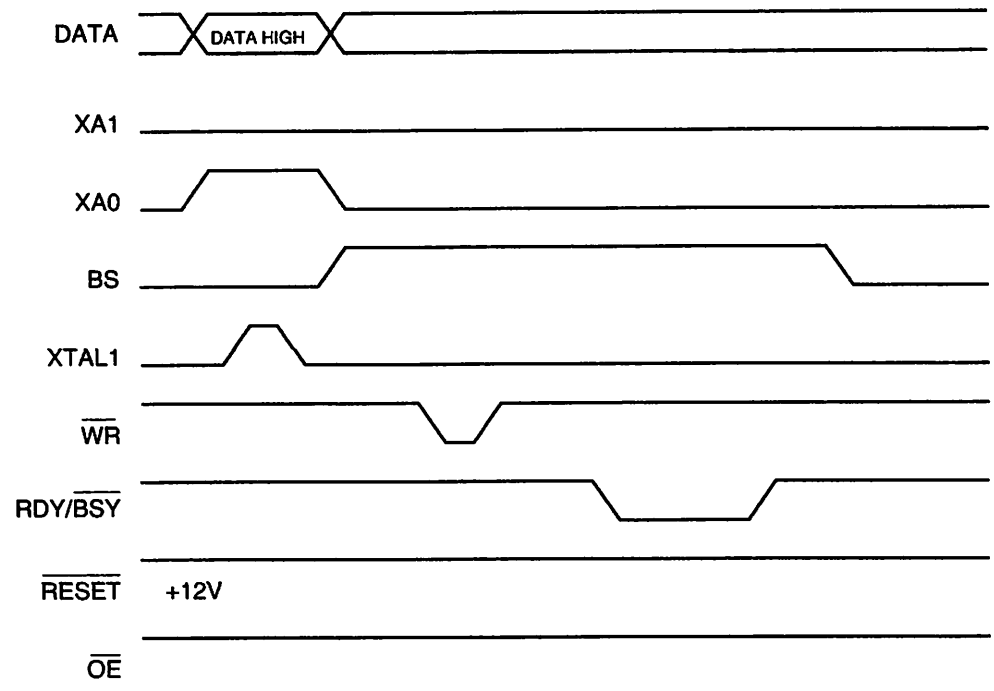


Figure 69. Programming the Flash Waveforms (Continued)



ding the Flash

The algorithm for reading the Flash memory is as follows (refer to "Programming the Flash" for details on command and address loading):

1. A: Load Command "0000 0010".
2. B: Load Address High Byte ($00 - $0F).
3. C: Load Address Low Byte ($00 - $FF).
4. Set $\overline{OE}$ to "0" and BS to "0". The Flash word low byte can now be read at DATA.
5. Set BS to "1". The Flash word high byte can now be read from DATA.
6. Set $\overline{OE}$ to "1".

gramming the EEPROM

The programming algorithm for the EEPROM data memory is as follows (refer to "Programming the Flash" for details on command, address and data loading):

1. A: Load Command "0001 0001".
2. B: Load Address High Byte ($00 - $01).
3. C: Load Address Low Byte ($00 - $FF).
4. D: Load Data Low Byte ($00 - $FF).
5. E: Write Data Low Byte.

ding the EEPROM

The algorithm for reading the EEPROM memory is as follows (refer to "Programming the Flash" for details on command and address loading):

1. A: Load Command "0000 0011".
2. B: Load Address High Byte ($00 - $01).
3. C: Load Address Low Byte ($00 - $FF).
4. Set $\overline{OE}$ to "0" and BS to "0". The EEPROM data byte can now be read at DATA.
5. Set $\overline{OE}$ to "1".

gramming the Fuse Bits

The algorithm for programming the Fuse bits is as follows (refer to "Programming the Flash" for details on command and data loading):

1. A: Load Command "0100 0000".
2. D: Load Data Low Byte. Bit n = "0" programs and bit n = "1" erases the Fuse bit.
   Bit 5 = SPIEN Fuse bit.
   Bit 0 = FSTRT Fuse bit.
   Bit 7-6,4-1 = "1". These bits are reserved and should be left unprogrammed ("1").
3. Give $\overline{WR}$ a t_{WLWH_PFB}-wide negative pulse to execute the programming, t_{WLWH_PFB} is found in Table 40. Programming the Fuse bits does not generate any activity on the RDY/$\overline{BSY}$ pin.

gramming the Lock Bits

The algorithm for programming the Lock bits is as follows (refer to "Programming the *Flash" on page 95 for details on command and data loading):*

1. A: Load Command "0010 0000".
2. D: Load Data Low Byte. Bit n = "0" programs the Lock bit.
   Bit 2 = Lock Bit2
   Bit 1 = Lock Bit1
   Bit 7-3,0 = "1". These bits are reserved and should be left unprogrammed ("1").
3. E: Write Data Low Byte.

The Lock bits can only be cleared by executing Chip Erase.

ding the Fuse and Lock

The algorithm for reading the Fuse and Lock bits is as follows (refer to "Programming the Flash" on page 95 for details on command loading):

1. A: Load Command "0000 0100".
2. Set $\overline{OE}$ to "0" and BS to "1". The status of the Fuse and Lock bits can now be read at DATA ("0" means programmed).
   Bit 7 = Lock Bit1
   Bit 6 = Lock Bit2
   Bit 5 = SPIEN Fuse bit
   Bit 0 = FSTRT Fuse bit
3. Set $\overline{OE}$ to "1".
   Observe that BS needs to be set to "1".

ding the Signature Bytes

The algorithm for reading the signature bytes is as follows (refer to "Programming the Flash" on page 95 for details on command and address loading):

1. A: Load Command "0000 1000".
2. C: Load Address Low Byte ($00 - $02).
   Set $\overline{OE}$ to "0" and BS to "0". The selected signature byte can now be read at DATA.
3. Set $\overline{OE}$ to "1".

allel Programming aracteristics

Figure 70. Parallel Programming Timing

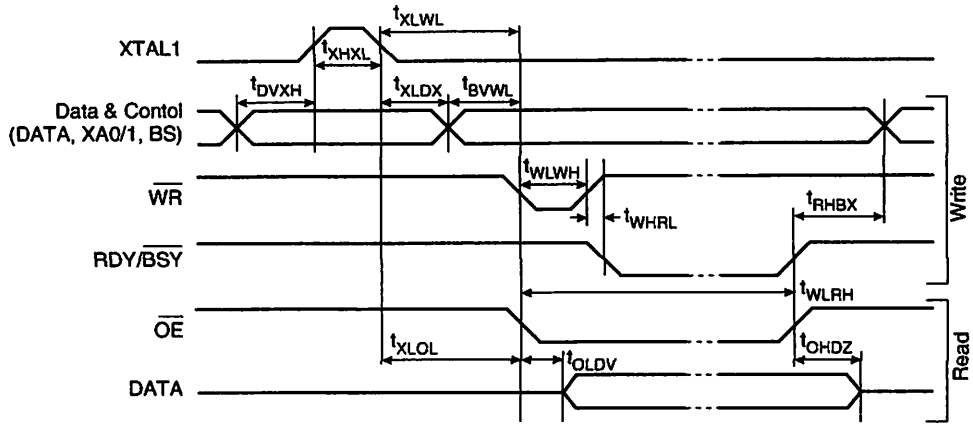


Table 40. Parallel Programming Characteristics, T_A = 25°C ± 10%, V_{CC} = 5V ± 10%

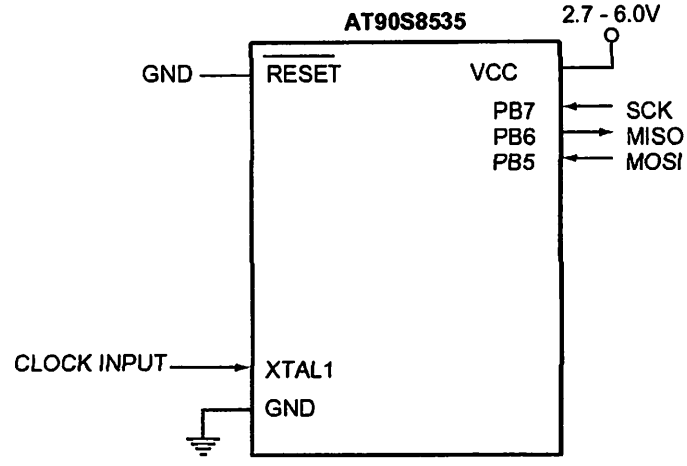
Symbol	Parameter	Min	Typ	Max	Units
V_{PP}	*Programming Enable Voltage*	11.5		12.5	V
I_{PP}	Programming Enable Current			250.0	µA
t_{DVXH}	Data and Control Setup before XTAL1 High	67.0			ns
t_{XHXL}	XTAL1 Pulse Width High	67.0			ns
t_{XLDX}	Data and Control Hold after XTAL1 Low	67.0			ns
t_{XLWL}	XTAL1 Low to $\overline{WR}$ Low	67.0			ns
t_{BVWL}	BS Valid to $\overline{WR}$ Low	67.0			ns
t_{RHBX}	BS Hold after RDY/$\overline{BSY}$ High	67.0			ns
t_{WLWH}	$\overline{WR}$ Pulse Width Low[1]	67.0			ns
t_{WHRL}	*$\overline{WR}$ High to RDY/$\overline{BSY}$ Low*[2]		*20.0*		*ns*
t_{WLRH}	$\overline{WR}$ Low to RDY/$\overline{BSY}$ High[2]	0.5	0.7	0.9	ms
t_{XLOL}	XTAL1 Low to $\overline{OE}$ Low	67.0			ns
t_{OLDV}	$\overline{OE}$ Low to DATA Valid		20.0		ns
t_{OHDZ}	$\overline{OE}$ High to DATA Tri-stated			20.0	ns
t_{WLWH_CE}	$\overline{WR}$ Pulse Width Low for Chip Erase	5.0	10.0	15.0	ms
t_{WLWH_PFB}	$\overline{WR}$ Pulse Width Low for Programming the Fuse Bits	1.0	1.5	1.8	ms

Notes: 1. Use t_{WLWH_CE} for Chip Erase and t_{WLWH_PFB} for programming the Fuse bits.
2. If t_{WLWH} is held longer than t_{WLRH}, no RDY/$\overline{BSY}$ pulse will be seen.

ial Downloading

Both the Flash and EEPROM memory arrays can be programmed using the serial SPI bus while $\overline{RESET}$ is pulled to GND. The serial interface consists of pins SCK, MOSI (input) and MISO (output), see Figure 71. After $\overline{RESET}$ is set low, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

Figure 71. Serial Programming and Verify



For the EEPROM, an auto-erase cycle is provided within the self-timed write instruction and there is no need to first execute the Chip Erase instruction. The Chip Erase instruction turns the content of every memory location in both the program and EEPROM arrays into $FF.

The program and EEPROM memory arrays have separate address spaces: $0000 to $0FFF for program memory and $0000 to $01FF for EEPROM memory.

Either an external clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The minimum low and high periods for the serial clock (SCK) input are defined as follows:

Low: > 2 XTAL1 clock cycles

High: > 2 XTAL1 clock cycles

ial Programming orithm

When writing serial data to the AT90S8535, data is clocked on the rising edge of SCK.

When reading data from the AT90S8535, data is clocked on the falling edge of SCK. See Figure 72, Figure 73 and Table 43 for timing details.

To program and verify the AT90SS8535 in the Serial Programming Mode, the following sequence is recommended (see 4-byte instruction formats in Table 42):

1. Power-up sequence:

   Apply power between V_{CC} and GND while $\overline{\text{RESET}}$ and SCK are set to "0". If a crystal is not connected across pins XTAL1 and XTAL2, apply a clock signal to the XTAL1 pin. In some systems, the programmer cannot guarantee that SCK is held low during power-up. In this case, $\overline{\text{RESET}}$ must be given a positive pulse of at least two XTAL1 cycles duration after SCK has been set to "0".
2. Wait for at least 20 ms and enable serial programming by sending the Programming Enable serial instruction to the MOSI (PB5) pin.
3. The serial programming instructions will not work if the communication is out of synchronization. When in sync, the second byte ($53) will echo back when issuing the third byte of the Programming Enable instruction. Whether the echo is correct or not, all four bytes of the instruction must be transmitted. If the $53 did not echo back, give SCK a positive pulse and issue a new Programming Enable instruction. If the $53 is not seen within 32 attempts, there is no functional device connected.

4. If a Chip Erase is performed (must be done to erase the Flash), wait t_{WD_ERASE} after the instruction, give $\overline{RESET}$ a positive pulse and start over from step 2. See Table 44 for t_{WD_ERASE} value.
5. The Flash or EEPROM array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. An EEPROM memory location is first automatically erased before new data is written. Use Data Polling to detect when the next byte in the Flash or EEPROM can be written. If polling is not used, wait t_{WD_PROG} before transmitting the next instruction. See Table 45 for t_{WD_PROG} value. In an erased device, no $FFs in the data file(s) needs to be programmed.
6. Any memory location can be verified by using the Read instruction that returns the content at the selected address at the serial output MISO (PB6) pin.
7. At the end of the programming session, $\overline{RESET}$ can be set high to commence normal operation.
8. Power-off sequence (if needed):

   Set XTAL1 to "0" (if a crystal is not used).

   Set $\overline{RESET}$ to "1".

   Turn V_{CC} power off.

a Polling EEPROM

When a byte is being programmed into the EEPROM, reading the address location being programmed will give the value P1 until the auto-erase is finished and then the value P2. See Table 41 for P1 and P2 values.

At the time the device is ready for a new EEPROM byte, the programmed value will read correctly. This is used to determine when the next byte can be written. This will not work for the values P1 and P2, so when programming these values, the user will have to wait for at least the prescribed time t_{WD_PROG} before programming the next byte. See Table 45 for t_{WD_PROG} value. As a chip-erased device contains $FF in all locations, programming of addresses that are meant to contain $FF can be skipped. This does not apply if the EEPROM is reprogrammed without first chip-erasing the device.

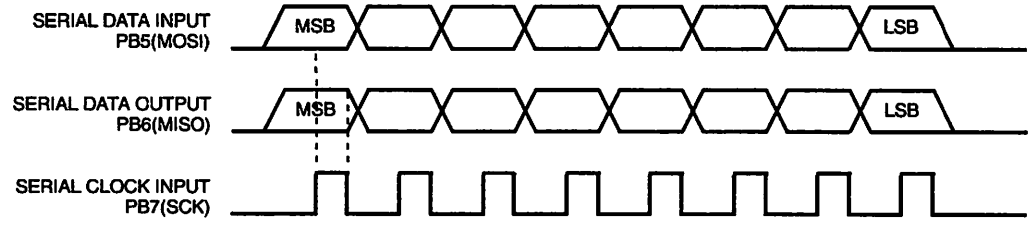
Table 41. *Read Back Value during EEPROM Polling*

Part	P1	P2
AT90S/LS8535	$00	$FF

a Polling Flash

When a byte is being programmed into the Flash, reading the address location being programmed will give the value $FF. At the time the device is ready for a new byte, the programmed value will read correctly. This is used to determine when the next byte can be written. This will not work for the value $FF, so when programming this value, the user will have to wait for at least t_{WD_PROG} before programming the next byte. As a chip-erased device contains $FF in all locations, programming of addresses that are meant to contain $FF can be skipped.

Figure 72. Serial Programming Waveforms



e 42. Serial Programming Instruction Set

truction	Instruction Format				Operation
	Byte 1	Byte 2	Byte 3	Byte4	
gramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx	Enable serial programming while $\overline{\text{RESET}}$ is low.
p Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash and EEPROM memory arrays.
ad Program Memory	0010 H000	xxxx aaaa	bbbb bbbb	oooo oooo	Read H (high or low) data o from program memory at word address a:b.
ite Program Memory	0100 H000	xxxx aaaa	bbbb bbbb	iiii iiii	Write H (high or low) data i to program memory at word address a:b.
ad EEPROM Memory	1010 0000	xxxx xxxa	bbbb bbbb	oooo oooo	Read data o from EEPROM memory at address a:b.
ite EEPROM Memory	1100 0000	xxxx xxxa	bbbb bbbb	iiii iiii	Write data i to EEPROM memory at address a:b.
ad Lock and Fuse Bits	0101 1000	xxxx xxxx	xxxx xxxx	*12S*x xxxF	Read Lock and Fuse bits. "0" = programmed "1" = unprogrammed
ite Lock Bits	1010 1100	1111 1*21*1	xxxx xxxx	xxxx xxxx	Write Lock bits. Set bits *1,2* = "0" to program Lock bits.
ad Signature Byte	0011 0000	xxxx xxxx	xxxx xxbb	oooo oooo	Read signature byte o at address b.(2)
ite FSTRT Fuse	1010 1100	1011 111F	xxxx xxxx	xxxx xxxx	Write FSTRT fuse. Set bit F = "0" to program, "1" to unprogram.

s: 1. **a** = address high bits
b = address low bits
H = 0 – Low byte, 1 – High Byte
o = data out
I = data in
x = don't care
1 = Lock Bit 1
2 = Lock Bit 2
F = FSTRT Fuse
S = SPIEN Fuse

2. The signature bytes are not readable in lock mode 3, i.e., both Lock bits programmed.

ial Programming aracteristics

Figure 73. Serial Programming Timing

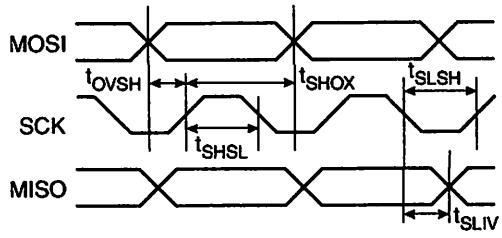


Table 43. Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 2.7 - 6.0V (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency (V_{CC} = 2.7 - 6.0V)	0		4.0	MHz
t_{CLCL}	Oscillator Period (V_{CC} = 2.7 - 4.0V)	250.0			ns
$1/t_{CLCL}$	Oscillator Frequency (V_{CC} = 4.0 - 6.0V)	0		8.0	MHz
t_{CLCL}	Oscillator Period (V_{CC} = 4.0 - 6.0V)	125.0			ns
t_{SHSL}	SCK Pulse Width High	2.0 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	2.0 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2.0 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10.0	16.0	32.0	ns

Table 44. Minimum Wait Delay after the Chip Erase instruction

Symbol	3.2V	3.6V	4.0V	5.0V
t_{WD_ERASE}	18 ms	14 ms	12 ms	8 ms

Table 45. Minimum Wait Delay after Writing a Flash or EEPROM Location

Symbol	3.2V	3.6V	4.0V	5.0V
t_{WD_PROG}	9 ms	7 ms	6 ms	4 ms

ctrical Characteristics

solute Maximum Ratings*

erating Temperature	-40°C to +105°C
rage Temperature	-65°C to +150°C
tage on Any Pin except $\overline{\text{RESET}}$ h Respect to Ground	-1.0V to V_{CC} + 0.5V
tage on $\overline{\text{RESET}}$ with Respect to Ground	-1.0V to +13.0V
ximum Operating Voltage	6.6V
Pin Maximum Current	40.0 mA
ximum Current V_{CC} GND (PDIP package)	200.0 mA
ximum Current V_{CC} GND (TQFP, PLCC package)	400.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and *functional operation of the device at these or* other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

-40°C to 85°C, V_{CC} = 2.7V to 6.0V (unless otherwise noted)

ymbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage		-0.5		$0.3V_{CC}$[1]	V
V_{IL1}	Input Low Voltage	XTAL	-0.5		$0.2\ V_{CC}$[1]	V
V_{IH}	Input High Voltage	Except (XTAL, RESET)	$0.6\ V_{CC}$[2]		V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	XTAL	$0.8\ V_{CC}$[2]		V_{CC} + 0.5	V
V_{IH2}	Input High Voltage	RESET	$0.9\ V_{CC}$[2]		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage[3] (Ports A, B, C, D)	I_{OL} = 20 mA, V_{CC} = 5V I_{OL} = 10 mA, V_{CC} = 3V			0.6 0.5	V V
V_{OH}	Output High Voltage[4] (Ports A, B, C, D)	I_{OH} = -3 mA, V_{CC} = 5V I_{OH} = -1.5 mA, V_{CC} = 3V	4.2 2.3			V V
I_{IL}	Input Leakage Current I/O Pin	V_{CC} = 6V, Vin = 0.45V (absolute value)			8.0	µA
I_{IH}	Input Leakage Current I/O Pin	V_{CC} = 6V, Vin = 6.0V (absolute value)			8.0	µA
RST	Reset Pull-up		100.0		500.0	kΩ
$R_{I/O}$	I/O Pin Pull-up Resistor		35.0		120.0	kΩ
I_{CC}	Power Supply Current	Active 4 MHz, V_{CC} = 3V			5.0	mA
		Idle 4 MHz, V_{CC} = 3V			3.0	mA
		Power-down, V_{CC} = 3V WDT enabled[5]			15.0	µA
		Power-down, V_{CC} = 3V WDT disabled[5]			5.0	µA
		Power Save, V_{CC} = 3V WDT disabled[5]			15.0	µA

Characteristics (Continued)

: -40°C to 85°C, V_{CC} = 2.7V to 6.0V (unless otherwise noted)

ymbol	Parameter	Condition	Min	Typ	Max	Units
V_{ACIO}	Analog Comparator Input Offset Voltage	V_{CC} = 5V V_{in} = V_{CC}/2			40.0	mV
I_{ACLK}	Analog Comparator Input Leakage A	V_{CC} = 5V V_{in} = V_{CC}/2	-50.0		50.0	nA
t_{ACPD}	Analog Comparator Propagation Delay	V_{CC} = 2.7V V_{CC} = 4.0V		750.0 500.0		ns

es:
1. "Max" means the highest value where the pin is guaranteed to be read as low (logical "0").
2. "Min" means the lowest value where the pin is guaranteed to be read as high (logical "1").
3. Although each I/O port can sink more than the test conditions (20 mA at V_{CC} = 5V, 10 mA at V_{CC} = 3V) under steady state conditions (non-transient), the following must be observed:
   PDIP Package:
   1] The sum of all I_{OL}, for all ports, should not exceed 200 mA.
   2] The sum of all I_{OL}, for port A0 - A7, should not exceed 100 mA.
   3] The sum of all I_{OL}, for ports B0 - B7, C0 - C7, D0 - D7 and XTAL2, should not exceed 100 mA.
   PLCC and TQFP Packages:
   1] The sum of all I_{OL}, for all ports, should not exceed 400 mA.
   2] The sum of all I_{OL}, for ports A0 - A7, should not exceed 100 mA.
   3] The sum of all I_{OL}, for ports B0 - B3, should not exceed 100 mA.
   4] The sum of all I_{OL}, for ports B4 - B7, should not exceed 100 mA.
   5] The sum of all I_{OL}, for ports C0 - C3, should not exceed 100 mA.
   6] The sum of all I_{OL}, for ports C4 - C7, should not exceed 100 mA.
   7] The sum of all I_{OL}, for ports D0 - D3 and XTAL2, should not exceed 100 mA.
   8] The sum of all I_{OL}, for ports D4 - D7, should not exceed 100 mA.
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
4. Although each I/O port can source more than the test conditions (3 mA at V_{CC} = 5V, 1.5 mA at V_{CC} = 3V) under steady state conditions (non-transient), the following must be observed:
   PDIP Package:
   1] The sum of all I_{OH}, for all ports, should not exceed 200 mA.
   2] The sum of all I_{OH}, for port A0 - A7, should not exceed 100 mA.
   3] The sum of all I_{OH}, for ports B0 - B7, C0 - C7, D0 - D7 and XTAL2, should not exceed 100 mA.
   PLCC and TQFP Packages:
   1] The sum of all I_{OH}, for all ports, should not exceed 400 mA.
   2] The sum of all I_{OH}, for ports A0 - A7, should not exceed 100 mA.
   3] The sum of all I_{OH}, for ports B0 - B3, should not exceed 100 mA.
   4] The sum of all I_{OH}, for ports B4 - B7, should not exceed 100 mA.
   5] The sum of all I_{OH}, for ports C0 - C3, should not exceed 100 mA.
   6] The sum of all I_{OH}, for ports C4 - C7, should not exceed 100 mA.
   7] The sum of all I_{OH}, for ports D0 - D3 and XTAL2, should not exceed 100 mA.
   8] The sum of all I_{OH}, for ports D4 - D7, should not exceed 100 mA.
   If I_{OH} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
5. *Minimum V_{CC} for power-down is 2V.*

ernal Clock Drive veforms

Figure 74. External Clock

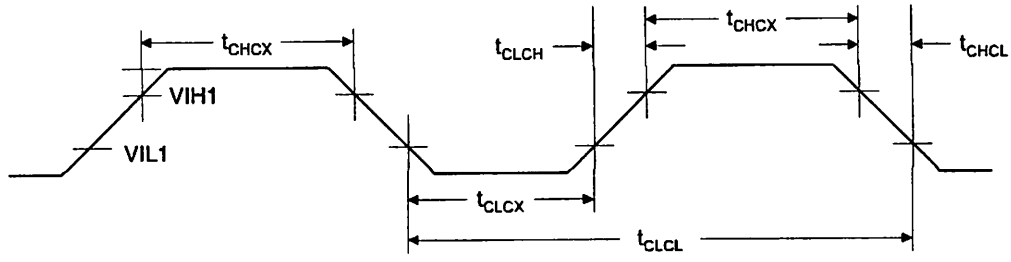


Table 46. External Clock Drive

Symbol	Parameter	V_{CC} = 2.7V to 6.0V		V_{CC} = 4.0V to 6.0V		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	4	0	8.0	MHz
t_{CLCL}	Clock Period	250.0		125.0		ns
t_{CHCX}	High Time	100.0		50.0		ns
t_{CLCX}	Low Time	100.0		50.0		ns
t_{CLCH}	Rise Time		1.6		0.5	µs
t_{CHCL}	Fall Time		1.6		0.5	µs

pical aracteristics

The following charts show typical behavior. These figures are not tested during manufacturing. All current consumption measurements are performed with all I/O pins configured as inputs and with internal pull-ups enabled. A sine wave generator with rail-to-rail output is used as clock source.

The power consumption in Power-down mode is independent of clock selection.

The current consumption is a function of several factors such as: operating voltage, operating frequency, loading of I/O pins, switching rate of I/O pins, code executed and ambient temperature. The dominating factors are operating voltage and frequency.

The current drawn from capacitive loaded pins may be estimated (for one pin) as $C_L \cdot V_{CC} \cdot f$ where C_L = load capacitance, V_{CC} = operating voltage and f = average switching frequency of I/O pin.

The parts are characterized at frequencies higher than test limits. Parts are not guaranteed to function properly at frequencies higher than the ordering code indicates.

The difference between current consumption in with Watchdog Timer enabled and Power-down mode with Watchdog Timer disabled represents the differential current drawn by the Watchdog Timer.

Figure 75. Active Supply Current vs. Frequency

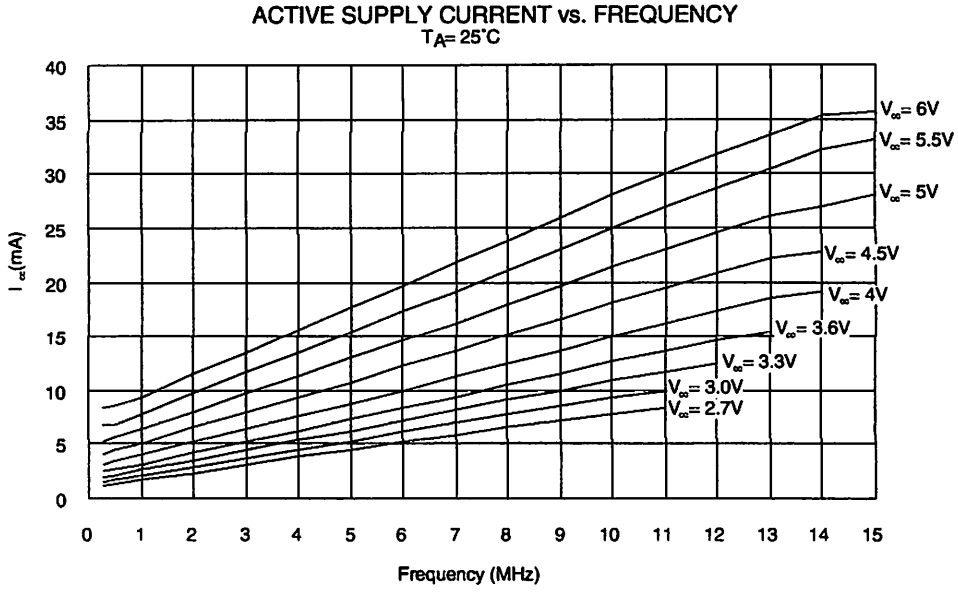


Figure 76. Active Supply Current vs. V_{CC}

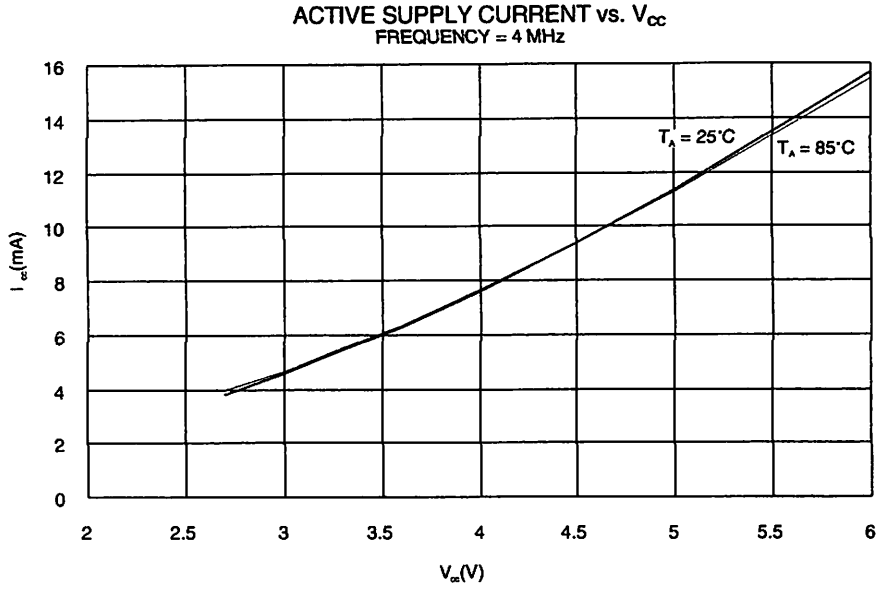


Figure 77. Idle Supply Current vs. Frequency

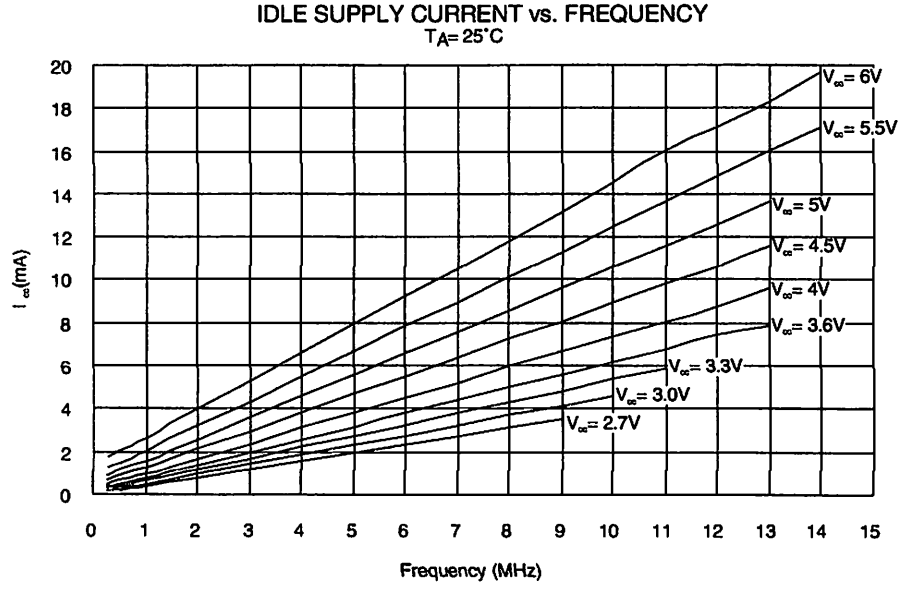


Figure 78. Idle Supply Current vs. V_{CC}

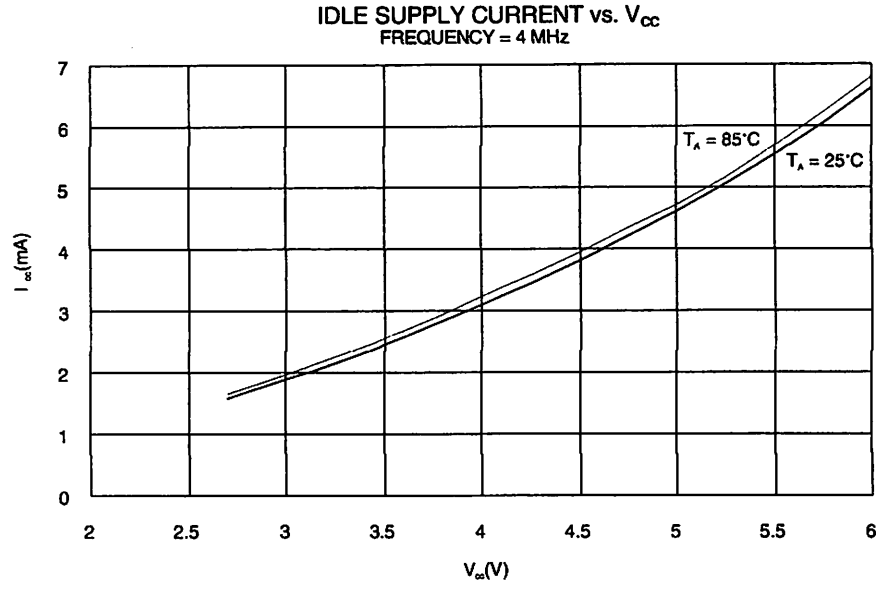


Figure 79. Power-down Supply Current vs. V_{CC}

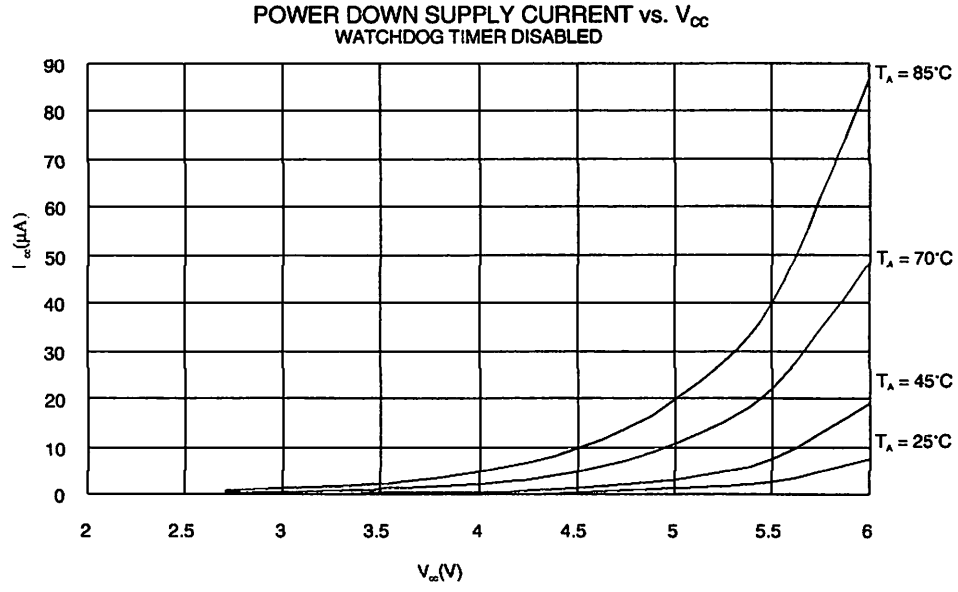


Figure 80. Power-down Supply Current vs. V_{CC}

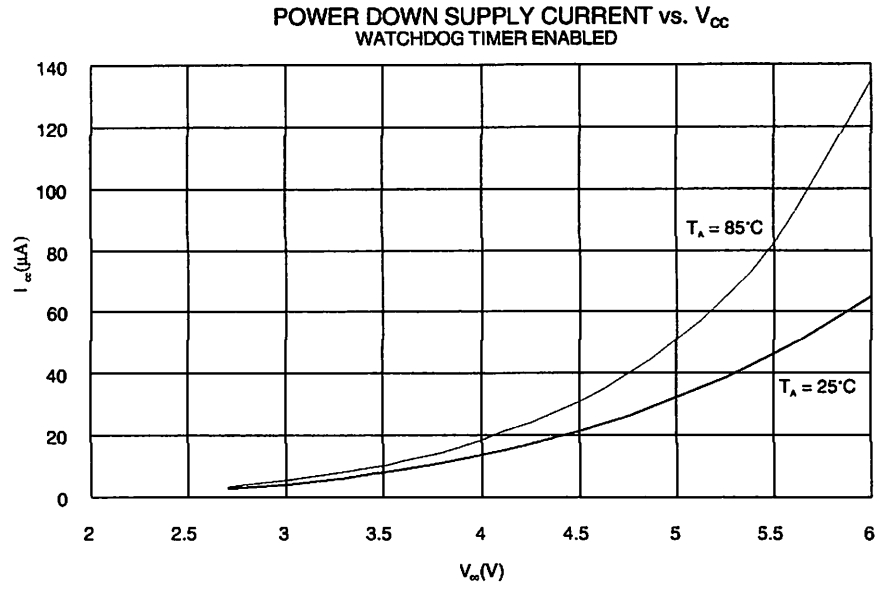


Figure 81. Power Save Supply Current vs. V_{CC}

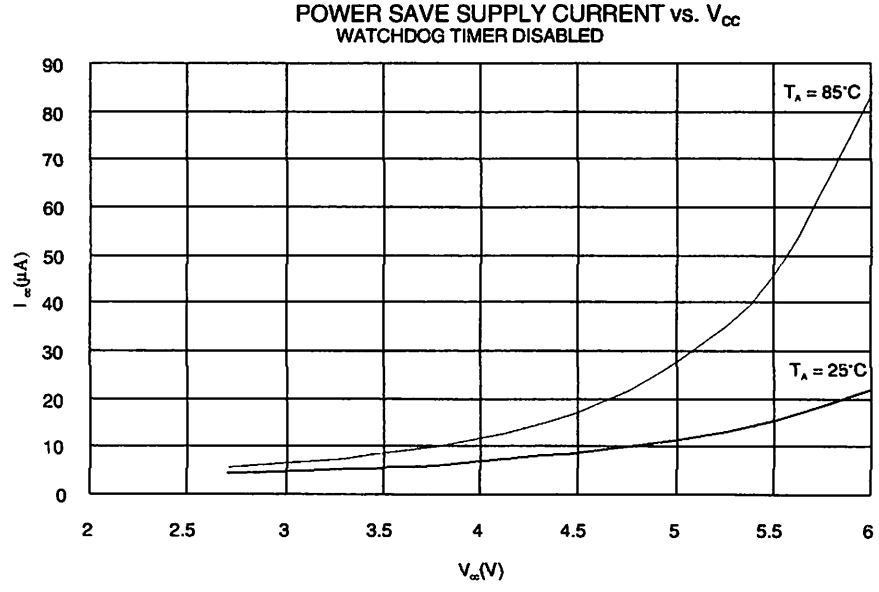
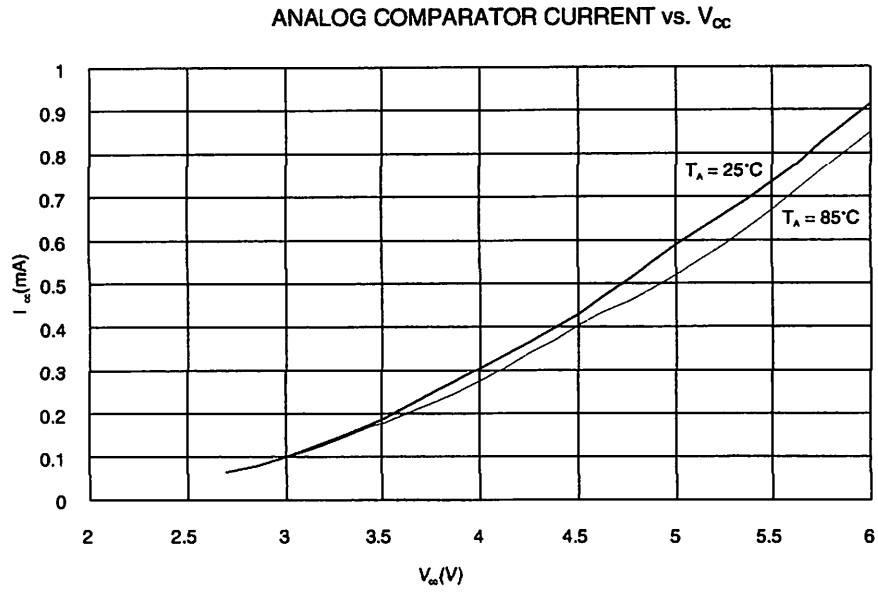


Figure 82. Analog Comparator Current vs. V_{CC}



Note: Analog comparator offset voltage is measured as absolute offset.

Figure 83. Analog Comparator Offset Voltage vs. Common Mode Voltage

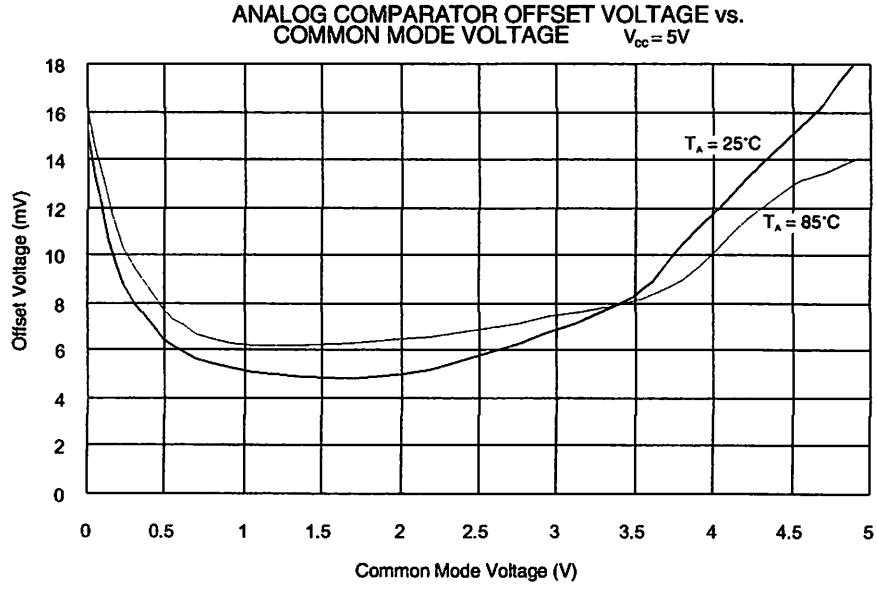


Figure 84. Analog Comparator Offset Voltage vs. Common Mode Voltage

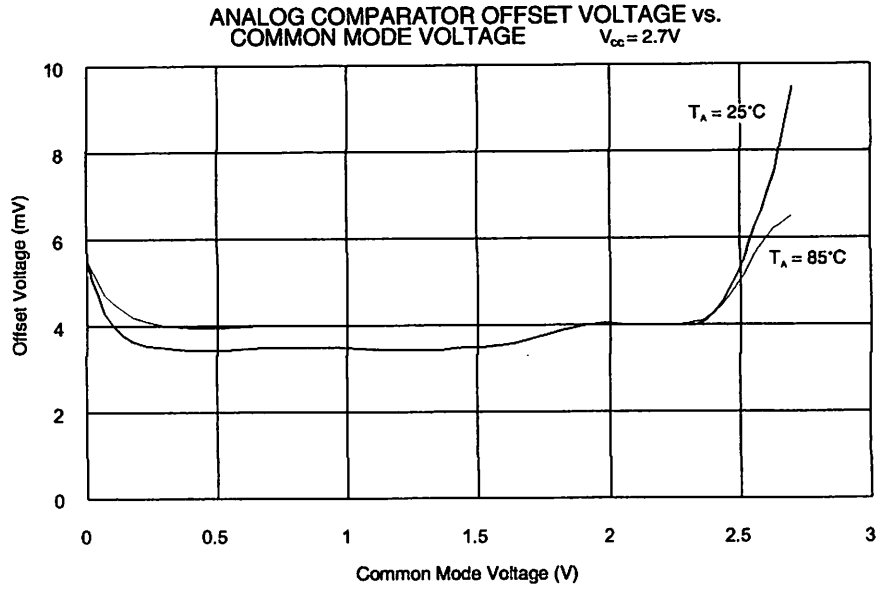


Figure 85. Analog Comparator Input Leakage Current

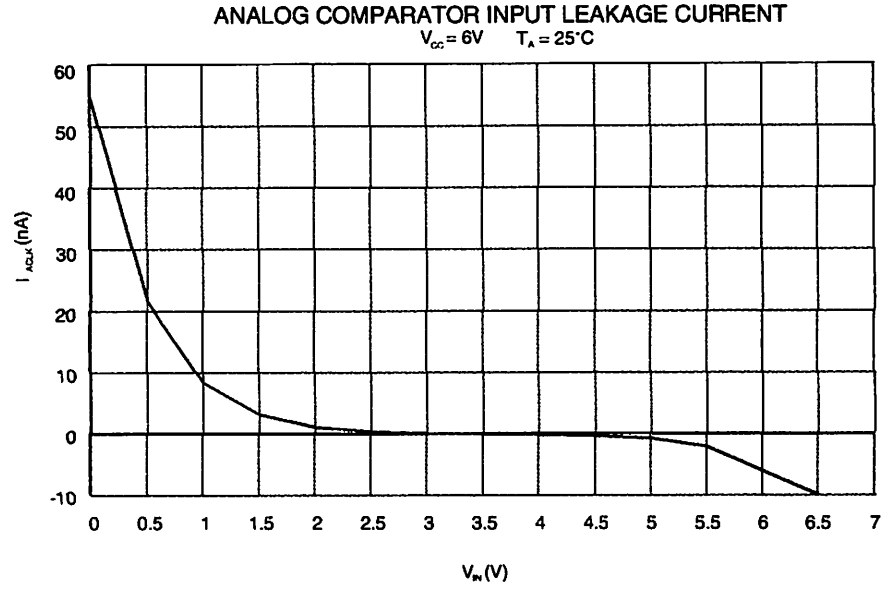
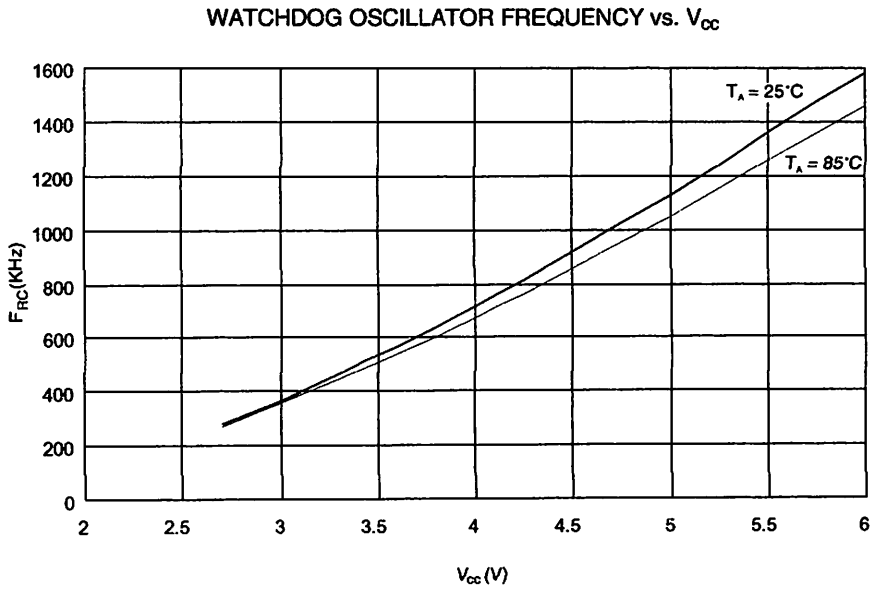


Figure 86. Watchdog Oscillator Frequency vs. V_{CC}



Note: Sink and source capabilities of I/O ports are measured on one pin at a time.

Figure 87. Pull-up Resistor Current vs. Input Voltage

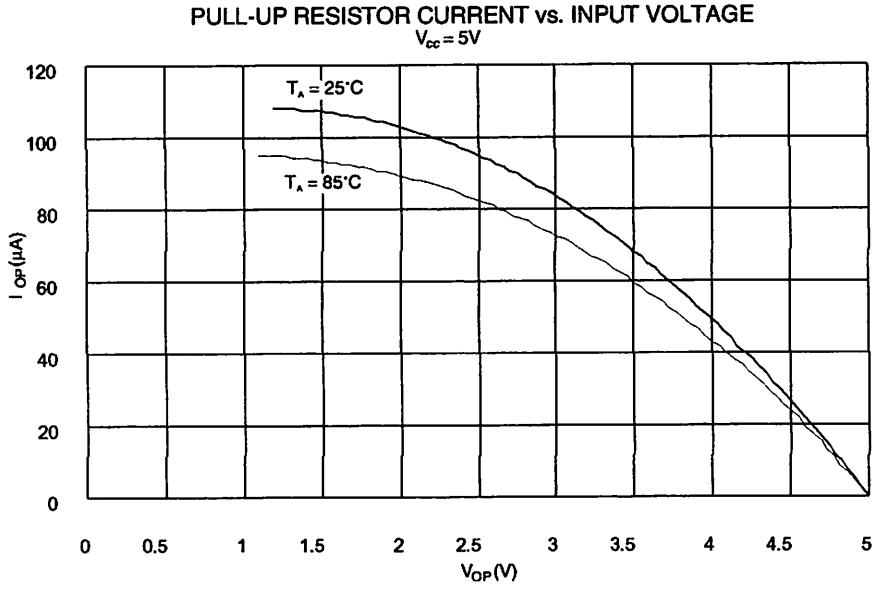


Figure 88. Pull-up Resistor Current vs. Input Voltage

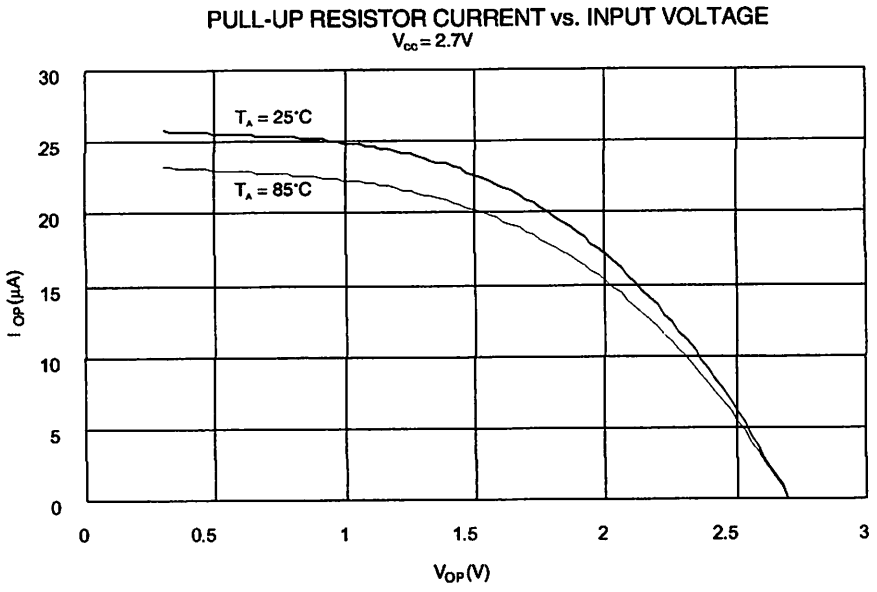


Figure 89. I/O Pin Sink Current vs. Output Voltage

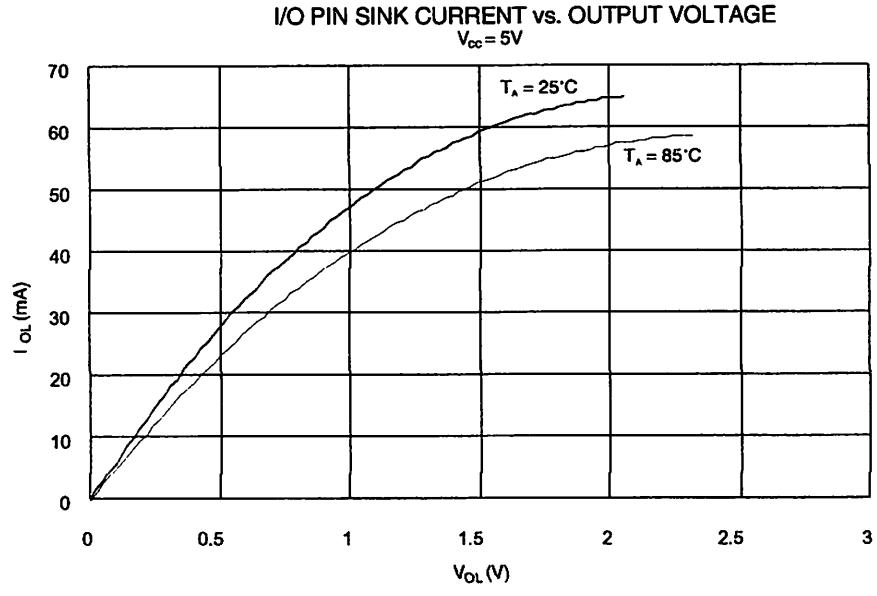


Figure 90. I/O Pin Source Current vs. Output Voltage

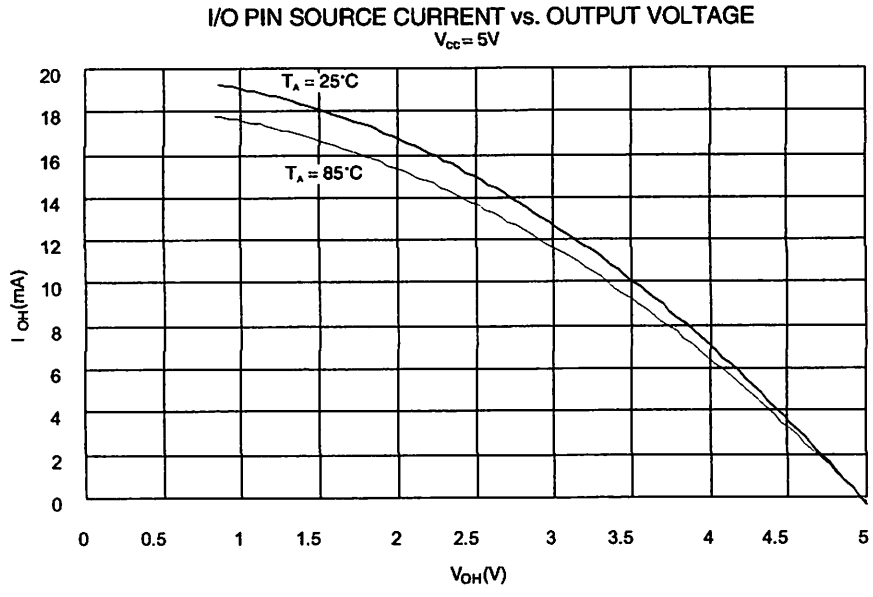


Figure 91. I/O Pin Sink Current vs. Output Voltage

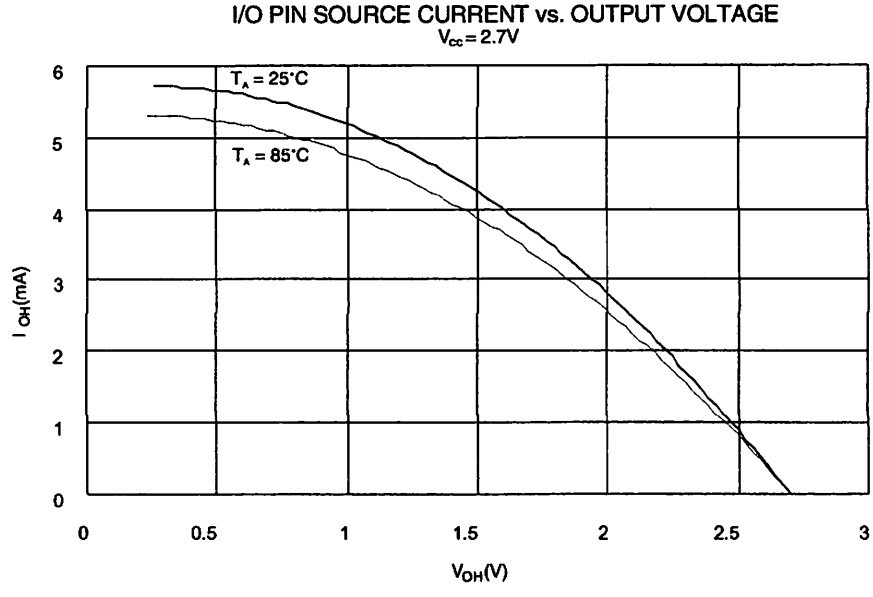


Figure 92. I/O Pin Source Current vs. Output Voltage

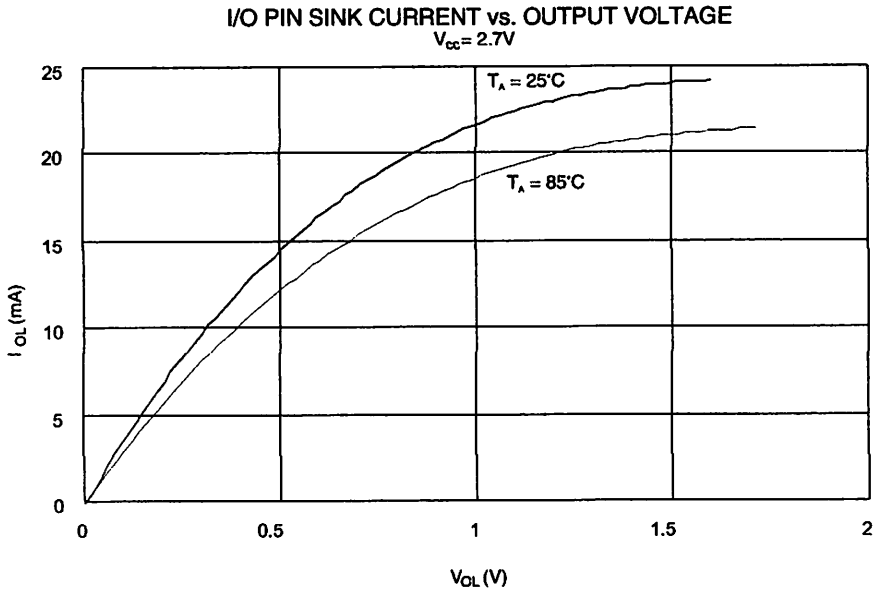


Figure 93. I/O Pin Input Threshold Voltage vs. V_{CC}

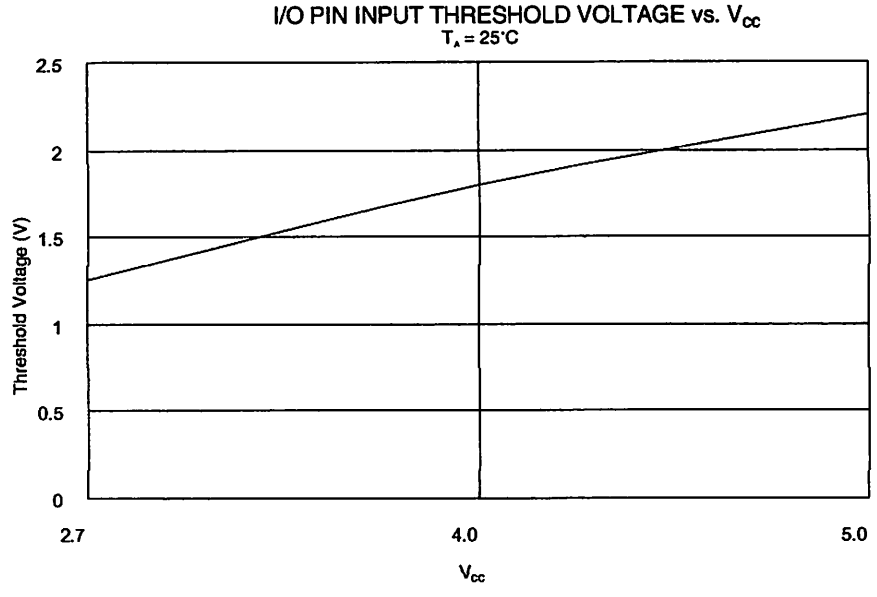
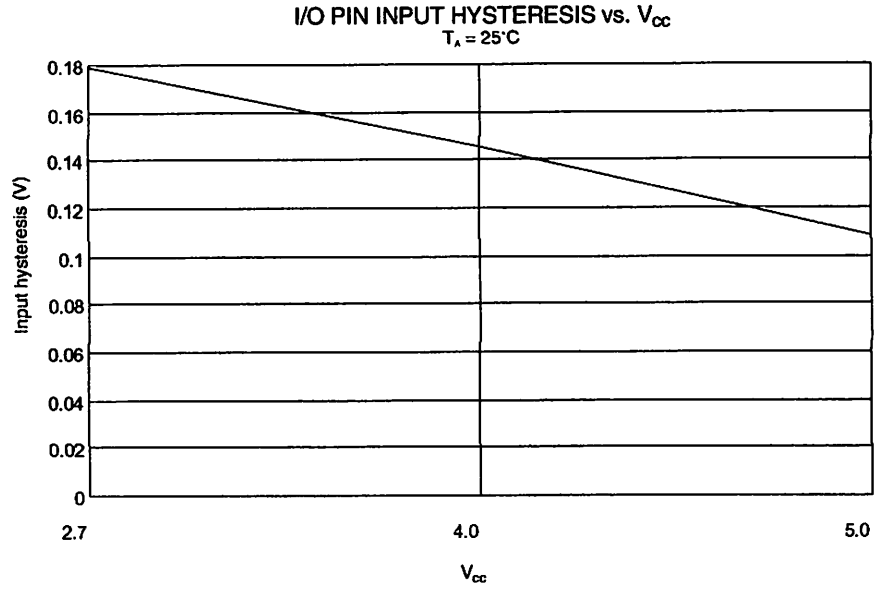


Figure 94. I/O Pin Input Hysteresis vs. V_{CC}



gister Summary

ddress	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
3F ($5F)	SREG	I	T	H	S	V	N	Z	C	page 19
3E ($5E)	SPH	-	-	-	-	-	-	SP9	SP8	page 20
3D ($5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	page 20
3C ($5C)	Reserved									
3B ($5B)	GIMSK	INT1	INT0	-	-	-	-	-	-	page 25
3A ($5A)	GIFR	INTF1	INTF0							page 26
39 ($59)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	-	TOIE0	page 26
38 ($58)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	-	TOV0	page 27
37 ($57)	Reserved									
36 ($56)	Reserved									
35 ($55)	MCUCR	-	SE	SM1	SM0	ISC11	ISC10	ISC01	ISC00	page 29
34 ($54)	MCUSR	-	-	-	-	-	-	EXTRF	PORF	page 24
33 ($53)	TCCR0	-	-	-	-	-	CS02	CS01	CS00	page 34
32 ($52)	TCNT0	Timer/Counter0 (8 Bits)								page 34
31 ($51)	Reserved									
30 ($50)	Reserved									
2F ($4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	-	-	PWM11	PWM10	page 36
2E ($4E)	TCCR1B	ICNC1	ICES1	-	-	CTC1	CS12	CS11	CS10	page 37
2D ($4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								page 38
2C ($4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								page 38
2B ($4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High Byte								page 39
2A ($4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low Byte								page 39
29 ($49)	*OCR1BH*	*Timer/Counter1 – Output Compare Register B High Byte*								*page 39*
28 ($48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low Byte								page 39
27 ($47)	ICR1H	Timer/Counter1 – Input Capture Register High Byte								page 40
26 ($46)	ICR1L	Timer/Counter1 – Input Capture Register Low Byte								page 40
25 ($45)	TCCR2	-	PWM2	COM21	COM20	CTC2	CS22	CS21	CS20	page 43
24 ($44)	TCNT2	Timer/Counter2 (8 Bits)								page 44
23 ($43)	*OCR2*	*Timer/Counter2 Output Compare Register*								page 44
22 ($42)	ASSR	-	-	-	-	AS2	TCN2UB	OCR2UB	TCR2UB	page 46
21 ($41)	WDTCR	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	page 49
20 ($40)	Reserved									
1F ($3F)	EEARH								EEAR8	page 51
1E ($3E)	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	page 51
1D ($3D)	EEDR	EEPROM Data Register								page 51
1C ($3C)	EECR	-	-	-	-	EERIE	EEMWE	EEWE	EERE	page 51
1B ($3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	page 76
1A ($3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	page 76
19 ($39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	page 76
18 ($38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	page 78
17 ($37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	page 78
16 ($36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 78
15 ($35)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	page 84
14 ($34)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	page 84
13 ($33)	*PINC*	*PINC7*	*PINC6*	*PINC5*	*PINC4*	*PINC3*	*PINC2*	*PINC1*	*PINC0*	*page 84*
12 ($32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	page 87
11 ($31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	page 87
10 ($30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	page 87
0F ($2F)	SPDR	SPI Data Register								page 58
0E ($2E)	SPSR	SPIF	WCOL	-	-	-	-	-	-	page 58
0D ($2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	page 57
0C ($2C)	UDR	UART I/O Data Register								page 62
0B ($2B)	USR	RXC	TXC	UDRE	FE	OR	-	-	-	page 62
0A ($2A)	UCR	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8	page 63
09 ($29)	UBRR	UART Baud Rate Register								page 65
08 ($28)	ACSR	ACD	-	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	page 66
07 ($27)	ADMUX	-	-	-	-	-	MUX2	MUX1	MUX0	page 72
06 ($26)	ADCSR	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	page 72
05 ($25)	ADCH	-	-	-	-	-	-	ADC9	ADC8	page 73
04 ($24)	ADCL	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	page 73
03 ($20)	Reserved									
02 ($22)	Reserved									
01 ($21)	Reserved									
00 ($20)	Reserved									

is: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. Some of the status flags are cleared by writing a logical "1" to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

ɨtruction Set Summary

emonic	Operands	Description	Operation	Flags	# Clocks
ΓHMETIC AND LOGIC INSTRUCTIONS					
)	Rd, Rr	Add Two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
:	Rd, Rr	Add with Carry Two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
W	Rdl, K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
;	Rd, Rr	Subtract Two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
I	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
:	Rd, Rr	Subtract with Carry Two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
I	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
W	Rdl, K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
)	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
I	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
R	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
M	Rd	One's Complement	Rd ← $FF – Rd	Z,C,N,V	1
G	Rd	Two's Complement	Rd ← $00 – Rd	Z,C,N,V,H	1
I	Rd, K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
R	Rd, K	Clear Bit(s) in Register	Rd ← Rd • ($FF - K)	Z,N,V	1
	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
;	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
I	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
I	Rd	Set Register	Rd ← $FF	None	1
ANCH INSTRUCTIONS					
IP	k	Relative Jump	PC ← PC + k + 1	None	2
P		Indirect Jump to (Z)	PC ← Z	None	2
ALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
LL		Indirect Call to (Z)	PC ← Z	None	3
-		Subroutine Return	PC ← STACK	None	4
T		Interrupt Return	PC ← STACK	I	4
PE	Rd, Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
	Rd, Rr	Compare	Rd – Rr	Z,N,V,C,H	1
;	Rd, Rr	Compare with Carry	Rd – Rr – C	Z,N,V,C,H	1
	Rd, K	Compare Register with Immediate	Rd – K	Z,N,V,C,H	1
RC	Rr, b	Skip if Bit in Register Cleared	If (Rr(b) = 0) PC ← PC + 2 or 3	None	1/2/3
RS	Rr, b	Skip if Bit in Register is Set	If (Rr(b) = 1) PC ← PC + 2 or 3	None	1/2/3
C	P, b	Skip if Bit in I/O Register Cleared	If (P(b) = 0) PC ← PC + 2 or 3	None	1/2/3
S	P, b	Skip if Bit in I/O Register is Set	If (P(b) = 1) PC ← PC + 2 or 3	None	1/2/3
BS	s, k	Branch if Status Flag Set	If (SREG(s) = 1) then PC ← PC + k + 1	None	1/2
BC	s, k	Branch if Status Flag Cleared	If (SREG(s) = 0) then PC ← PC + k + 1	None	1/2
EQ	k	Branch if Equal	If (Z = 1) then PC ← PC + k + 1	None	1/2
NE	k	Branch if Not Equal	If (Z = 0) then PC ← PC + k + 1	None	1/2
CS	k	Branch if Carry Set	If (C = 1) then PC ← PC + k + 1	None	1/2
CC	k	Branch if Carry Cleared	If (C = 0) then PC ← PC + k + 1	None	1/2
SH	k	Branch if Same or Higher	If (C = 0) then PC ← PC + k + 1	None	1/2
LO	k	Branch if Lower	If (C = 1) then PC ← PC + k + 1	None	1/2
MI	k	Branch if Minus	If (N = 1) then PC ← PC + k + 1	None	1/2
PL	k	Branch if Plus	If (N = 0) then PC ← PC + k + 1	None	1/2
GE	k	Branch if Greater or Equal, Signed	If (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
LT	k	Branch if Less Than Zero, Signed	If (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
HS	k	Branch if Half-carry Flag Set	If (H = 1) then PC ← PC + k + 1	None	1/2
HC	k	Branch if Half-carry Flag Cleared	If (H = 0) then PC ← PC + k + 1	None	1/2
TS	k	Branch if T-flag Set	If (T = 1) then PC ← PC + k + 1	None	1/2
TC	k	Branch if T-flag Cleared	If (T = 0) then PC ← PC + k + 1	None	1/2
VS	k	Branch if Overflow Flag is Set	If (V = 1) then PC ← PC + k + 1	None	1/2
VC	k	Branch if Overflow Flag is Cleared	If (V = 0) then PC ← PC + k + 1	None	1/2
IE	k	Branch if Interrupt Enabled	If (I = 1) then PC ← PC + k + 1	None	1/2
ID	k	Branch if Interrupt Disabled	If (I = 0) then PC ← PC + k + 1	None	1/2
TA TRANSFER INSTRUCTIONS					
V	Rd, Rr	Move between Registers	Rd ← Rr	None	1
	Rd, K	Load Immediate	Rd ← K	None	1
	Rd, X	Load Indirect	Rd ← (X)	None	2
	Rd, X+	Load Indirect and Post-inc.	Rd ← (X), X ← X + 1	None	2
	Rd, -X	Load Indirect and Pre-dec.	X ← X - 1, Rd ← (X)	None	2

truction Set Summary (Continued)

emonic	Operands	Description	Operation	Flags	# Clocks
	Rd, Y	Load Indirect	Rd ← (Y)	None	2
	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
	Rd, -Y	Load Indirect and Pre-dec.	Y ← Y - 1, Rd ← (Y)	None	2
	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
	Rd, Z	Load Indirect	Rd ← (Z)	None	2
	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z + 1	None	2
	Rd, -Z	Load Indirect and Pre-dec.	Z ← Z - 1, Rd ← (Z)	None	2
	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
	X, Rr	Store Indirect	(X) ← Rr	None	2
	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
	-X, Rr	Store Indirect and Pre-dec.	X ← X - 1, (X) ← Rr	None	2
	Y, Rr	Store Indirect	(Y) ← Rr	None	2
	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
	-Y, Rr	Store Indirect and Pre-dec.	Y ← Y - 1, (Y) ← Rr	None	2
	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
	Z, Rr	Store Indirect	(Z) ← Rr	None	2
	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
	-Z, Rr	Store Indirect and Pre-dec.	Z ← Z - 1, (Z) ← Rr	None	2
	Z+q, Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
		Load Program Memory	R0 ← (Z)	None	3
	Rd, P	In Port	Rd ← P	None	1
	P, Rr	Out Port	P ← Rr	None	1
H	Rr	Push Register on Stack	STACK ← Rr	None	2
	Rd	Pop Register from Stack	Rd ← STACK	None	2
AND BIT-TEST INSTRUCTIONS					
	P, b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
	P, b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
	Rd	Rotate Left through Carry	Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7)	Z,C,N,V	1
	Rd	Rotate Right through Carry	Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0)	Z,C,N,V	1
	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n = 0..6	Z,C,N,V	1
AP	Rd	Swap Nibbles	Rd(3..0) ← Rd(7..4), Rd(7..4) ← Rd(3..0)	None	1
T	s	Flag Set	SREG(s) ← 1	SREG(s)	1
R	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
	Rd, b	Bit Load from T to Register	Rd(b) ← T	None	1
		Set Carry	C ← 1	C	1
		Clear Carry	C ← 0	C	1
		Set Negative Flag	N ← 1	N	1
		Clear Negative Flag	N ← 0	N	1
		Set Zero Flag	Z ← 1	Z	1
		Clear Zero Flag	Z ← 0	Z	1
		Global Interrupt Enable	I ← 1	I	1
		Global Interrupt Disable	I ← 0	I	1
		Set Signed Test Flag	S ← 1	S	1
		Clear Signed Test Flag	S ← 0	S	1
		Set Two's Complement Overflow	V ← 1	V	1
		Clear Two's Complement Overflow	V ← 0	V	1
		Set T in SREG	T ← 1	T	1
		Clear T in SREG	T ← 0	T	1
		Set Half-carry Flag in SREG	H ← 1	H	1
		Clear Half-carry Flag in SREG	H ← 0	H	1
		No Operation		None	1
EP		Sleep	(see specific descr. for Sleep function)	None	1
R		Watchdog Reset	(see specific descr. for WDR/timer)	None	1

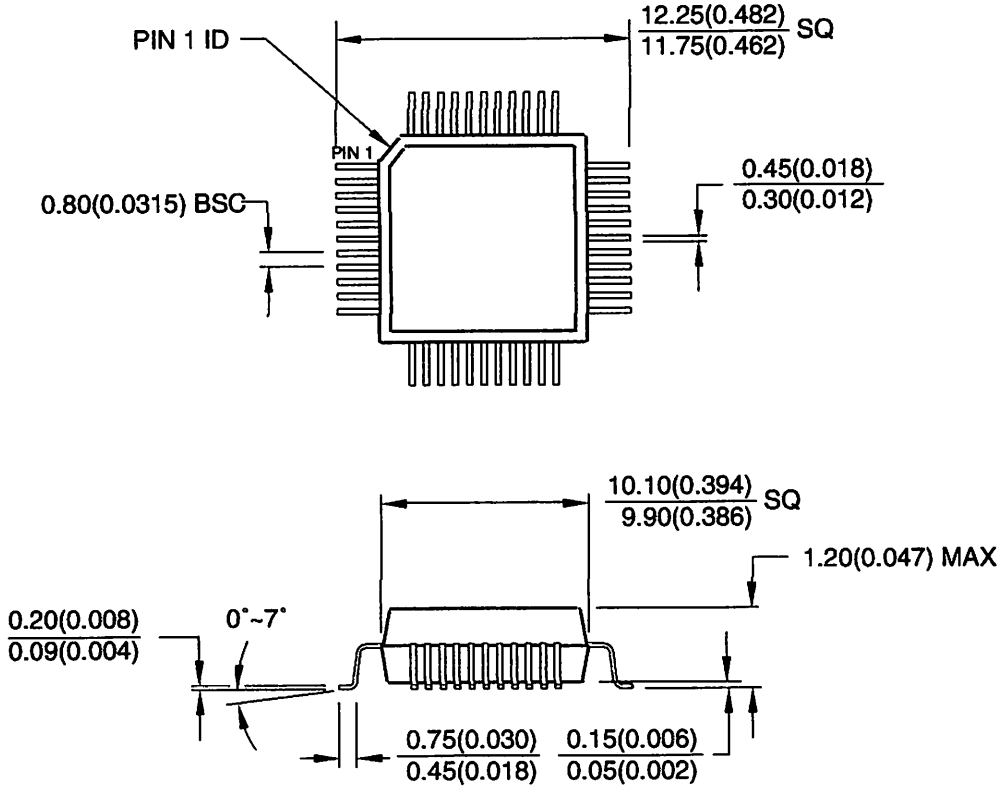
dering Information

Power Supply	Speed (MHz)	Ordering Code	Package	Operation Range
2.7 - 6.0V	4	AT90LS8535-4AC AT90LS8535-4JC AT90LS8535-4PC AT90LS8535-4MC	44A 44J 40P6 44M1	Commercial (0°C to 70°C)
		AT90LS8535-4AI AT90LS8535-4JI AT90LS8535-4PI AT90LS8535-4MI	44A 44J 40P6 44M1	Industrial (-40°C to 85°C)
4.0 - 6.0V	8	AT90S8535-8AC AT90S8535-8JC AT90S8535-8PC AT90LS8535-8MC	44A 44J 40P6 44M1	Commercial (0°C to 70°C)
		AT90S8535-8AI AT90S8535-8JI AT90S8535-8PI AT90LS8535-8MI	44A 44J 40P6 44M1	Industrial (-40°C to 85°C)

	Package Type
A	44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
M1	44-pad, 7 x 7 x 1.0 mm body, lead pitch 0.50 mm, Micro Lead Frame Package (MLF)

ckaging Information

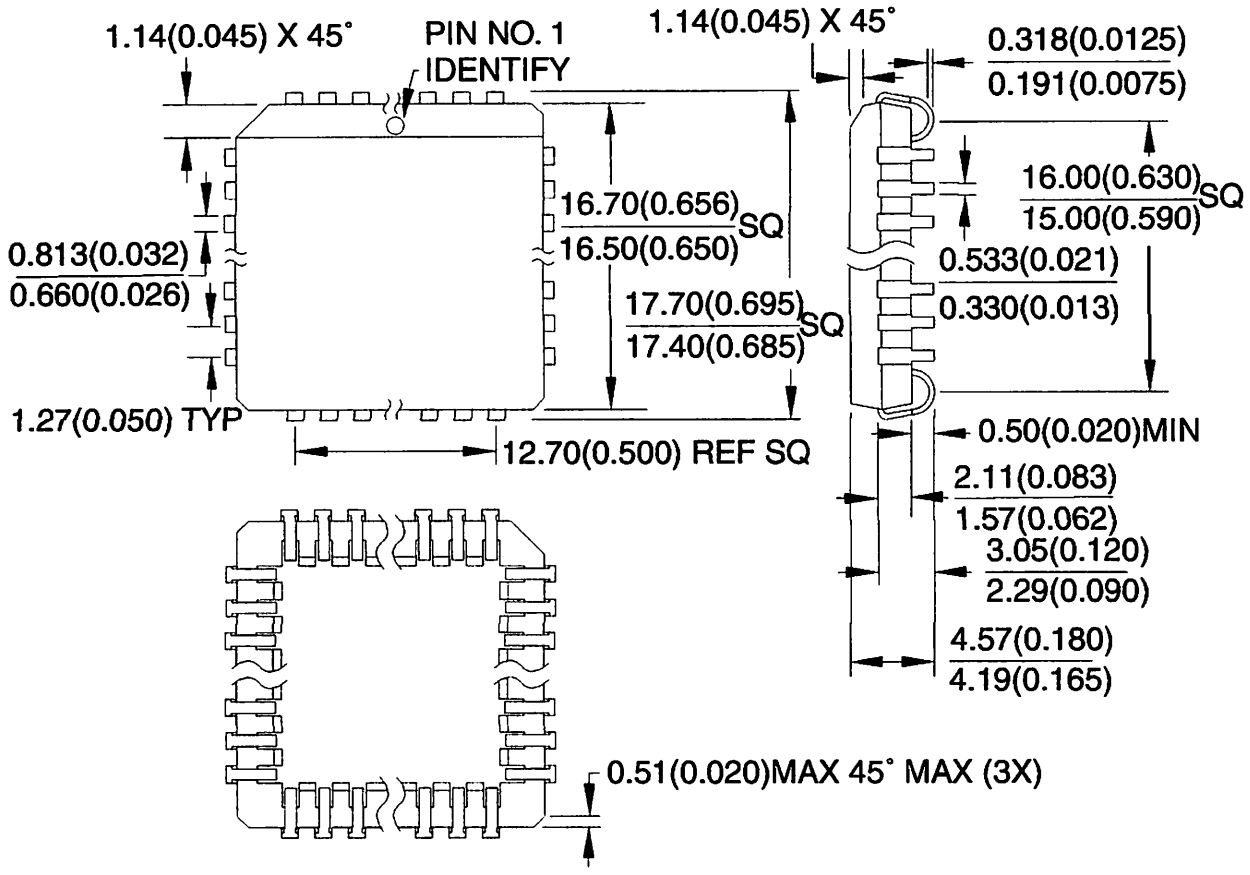
44-lead, Thin (1.0mm) Plastic Quad Flat Package
(TQFP), 10x10mm body, 2.0mm footprint, 0.8mm pitch.
Dimension in Millimeters and (Inches)*
JEDEC STANDARD MS-026 ACB



*Controlling dimension: millimetter

REV. A 04/11/2001

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Milimeters and (Inches)*
JEDEC STANDARD MS-018 AC

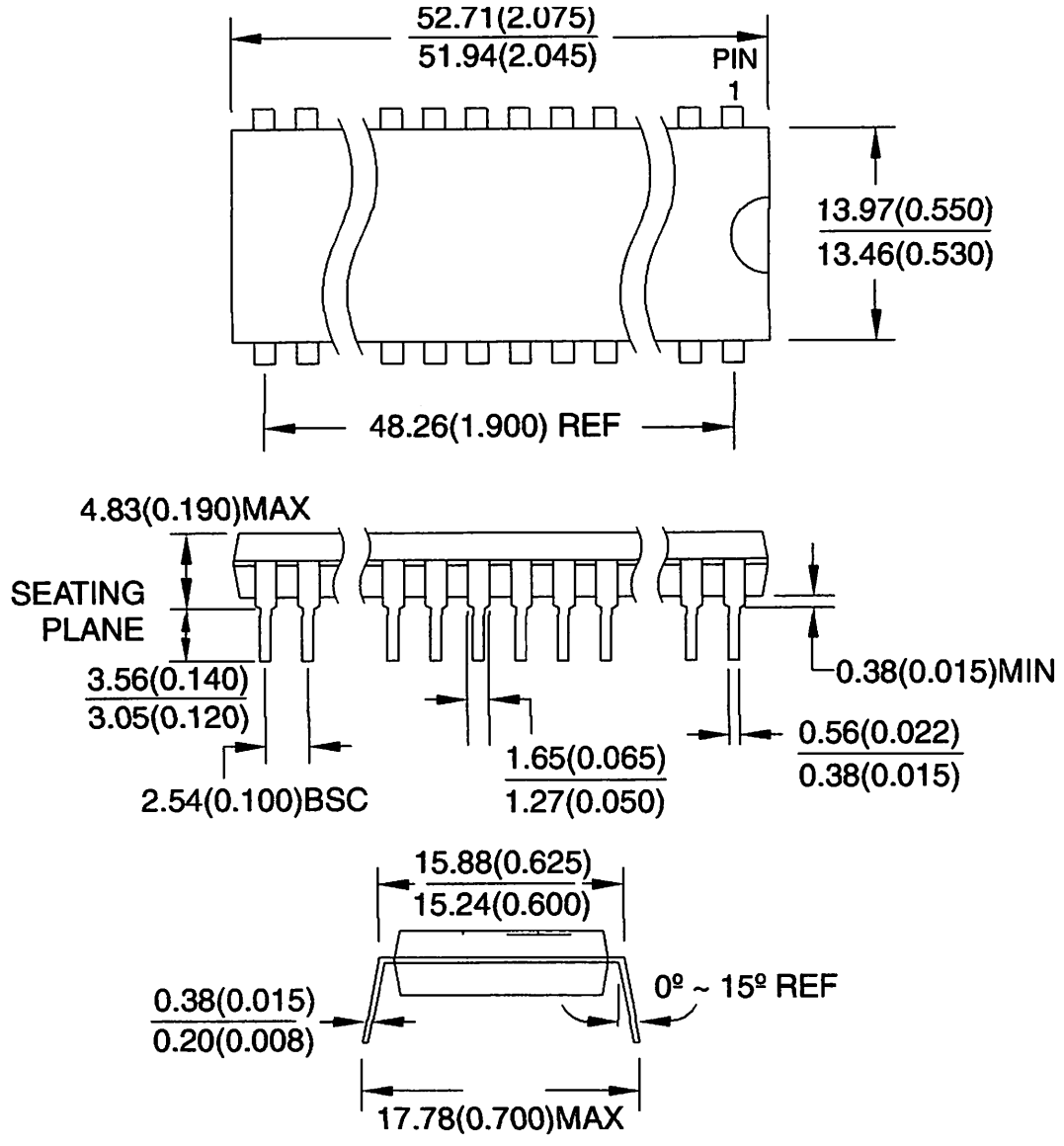


*Controlling dimensions: Inches

REV. A 04/11/2001

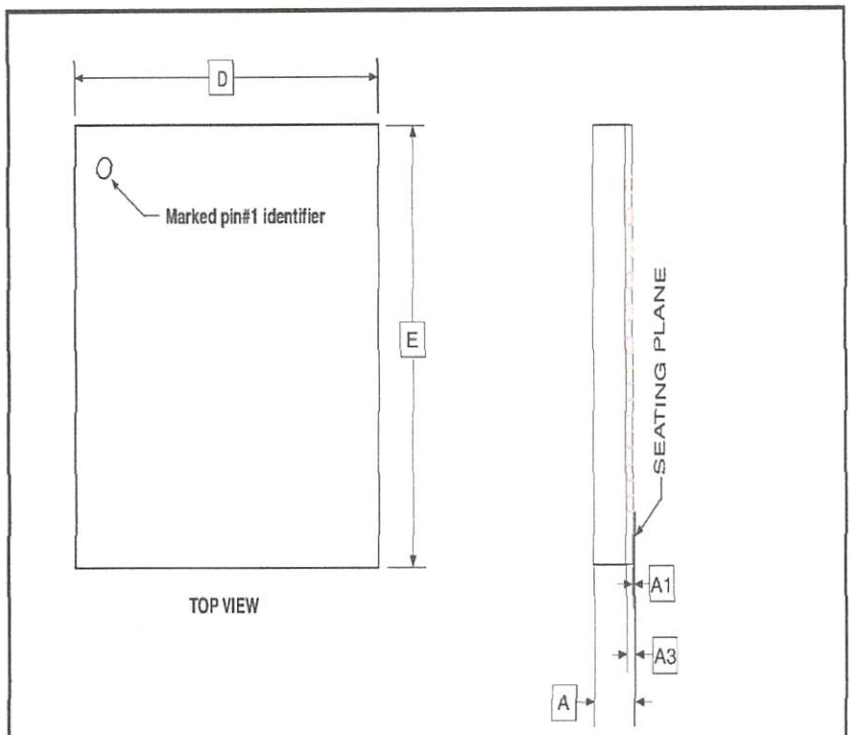
'6

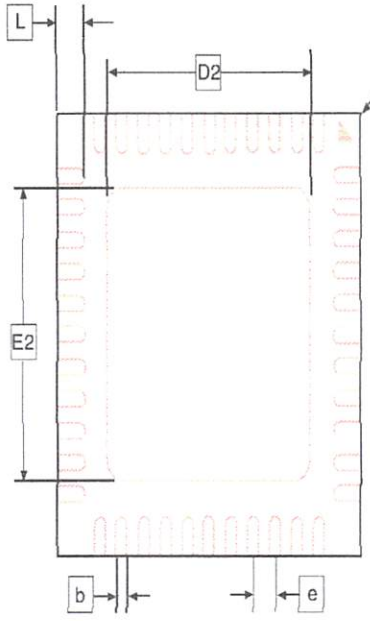
40-lead, Plastic Dual Inline
Parkage (PDIP), 0.600" wide
Demension in Millimeters and (Inches)*
JEDEC STANDARD MS-011 AC



*Controlling dimension: Inches

REV. A 04/11/2001





COMMON DIMENSIONS (*Unit of Measure = mm)				
SYMBOL	*MIN*	*NOM*	*MAX*	*NOTE*
A	*0.80*	*0.90*	*1.00*	
A1	0.00	0.02	0.05	
A3		0.25 REF		
b	0.18	0.23	0.30	
D		7.00 BSC		
D2	2.25	4.70	5.25	
E		7.00 BSC		
E2	2.25	4.70	5.25	
e		0.50 BSC		
L	0.35	0.55	0.75	

NOTE 1. JEDEC STANDARD MO-220, Fig 1 (Saw Singulation), VKKD-1

07/23/01

2325 Orchard Parkway San Jose, CA 95131	TITLE *44M1, 44-pad ,7 x 7 x 1.0 mm body, lead pitch 0.50mm Micro lead frame package (MLF)*	DRAWING NO. *44M1*	REV *A*

:mel Headquarters

rporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

rope
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

ia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

pan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Product Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-7658-3000
FAX (33) 4-7658-3480

Atmel Heilbronn
Theresienstrasse 2
POB 3535
D-74025 Heilbronn, Germany
TEL (49) 71 31 67 25 94
FAX (49) 71 31 67 24 23

Atmel Nantes
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 0 2 40 18 18 18
FAX (33) 0 2 40 18 19 60

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-357-000
FAX (44) 1355-242-743

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

tmel Corporation 2001.

el Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty :h is detailed in Atmel's Terms and Conditions located on the Company's web site. The Company assumes no responsibility for any errors :h may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does nake any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted ie Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical ponents in life support devices or systems.

IEL® and AVR® are the registered trademarks of Atmel.

er terms and product names may be the trademarks of others.

Printed on recycled paper.

1041H–11/01/0M

FAIRCHILD
SEMICONDUCTOR™

August 1986
Revised July 2001

DM7414
Hex Inverter with Schmitt Trigger Input

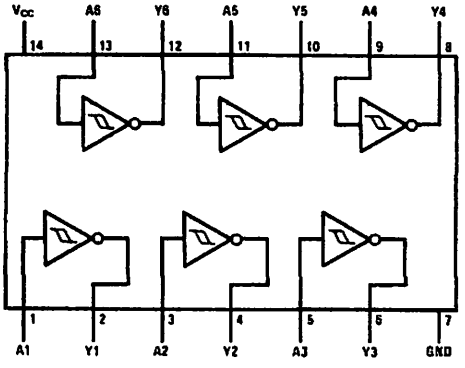
General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Ordering Code:

Order Number	Package Number	Package Description
DM7414N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

© 2001 Fairchild Semiconductor Corporation

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be *operated at these limits. The parametric values defined in the Electrical* Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 2)	1.5	1.7	2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 2)	0.6	0.9	1.1	V
HYS	Input Hysteresis (Note 2)	0.4	0.8		V
I_{OH}	High Level Output Current			−0.8	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Note 2: V_{CC} = 5V

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_I = V_{T-} Min	2.4	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_I = V_{T+} Max		0.2	0.4	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}		−0.43		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}		−0.56		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	−18		−55	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		22	36	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		39	60	mA

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

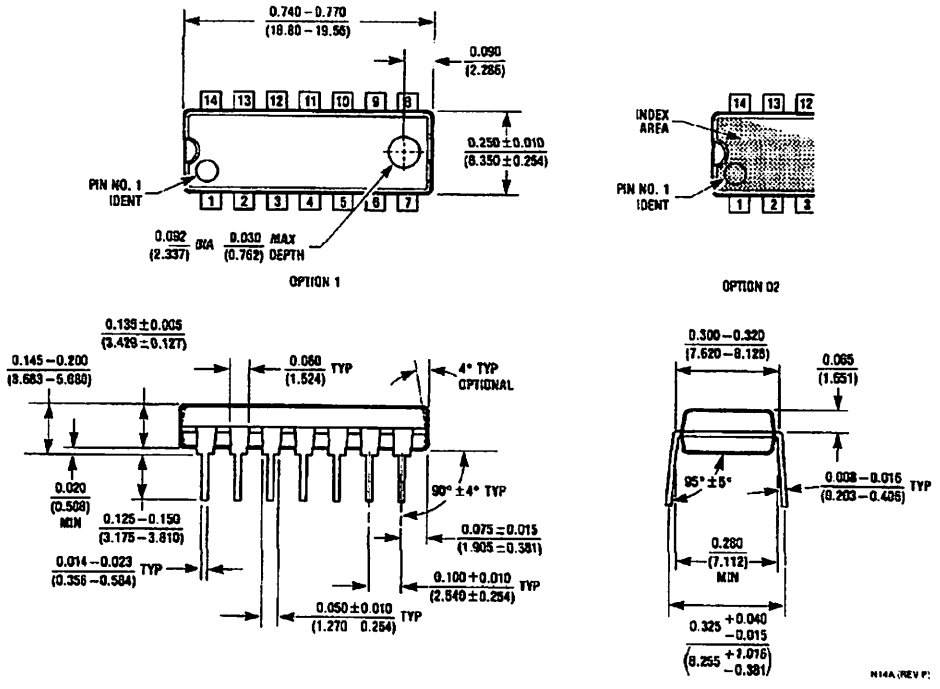
Note 4: Not more than one output should be shorted at a time.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF, R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			22	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

FAIRCHILD
SEMICONDUCTOR®

SS9014

Pre-Amplifier, Low Level & Low Noise

- High total power dissipation. (P_T=450mW)
- High h_{FE} and good linearity
- Complementary to SS9015

TO-92

1

1. Emitter 2. Base 3. Collector

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{CBO}	Collector-Base Voltage	50	V
V_{CEO}	Collector-Emitter Voltage	45	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current	100	mA
P_C	Collector Power Dissipation	450	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C=100μA, I_E=0	50			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C=1mA, I_B=0	45			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E=100μA, I_C=0	5			V
I_{CBO}	Collector Cut-off Current	V_{CB}=50V, I_E=0			50	nA
I_{EBO}	Emitter Cut-off Current	V_{EB}=5V, I_C=0			50	nA
h_{FE}	DC Current Gain	V_{CE}=5V, I_C=1mA	60	280	1000	
V_{CE} (sat)	Collector-Base Saturation Voltage	I_C=100mA, I_B=5mA		0.14	0.3	
V_{BE} (sat)	Base-Emitter Saturation Voltage	I_C=100mA, I_B=5mA		0.84	1.0	V
V_{BE} (on)	Base-Emitter On Voltage	V_{CE}=5V, I_C=2mA	0.58	0.63	0.7	V
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0 f=1MHz		2.2	3.5	pF
f_T	Current Gain Bandwidth Product	V_{CE}=5V, I_C=10mA	150	270		MHz
NF	Noise Figure	V_{CE}=5V, I_C=0.2mA f=1KHz, R_S=2KΩ		0.9	10	dB

h_{FE} Classification

Classification	A	B	C	D
h_{FE}	60 ~ 150	100 ~ 300	200 ~ 600	400 ~ 1000

©2002 Fairchild Semiconductor Corporation

Typical Characteristics

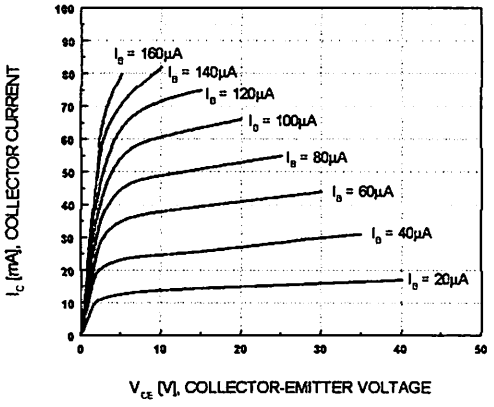


Figure 1. Static Characteristic

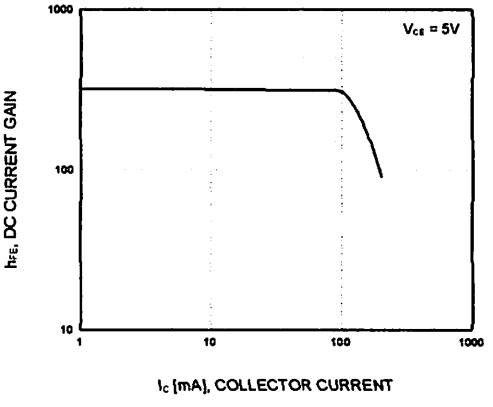


Figure 2. DC current Gain

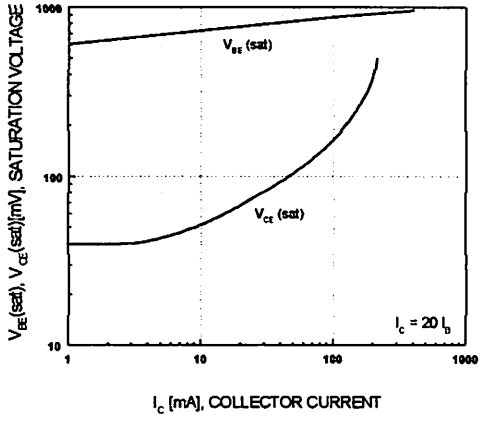


Figure 3. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

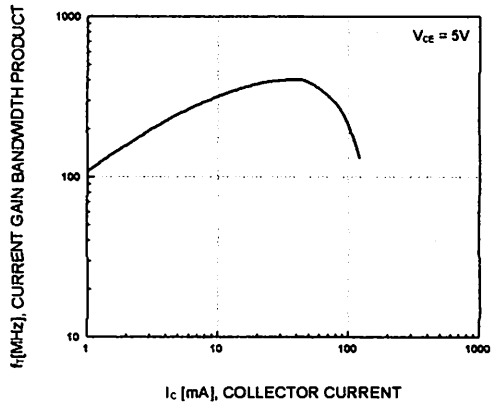
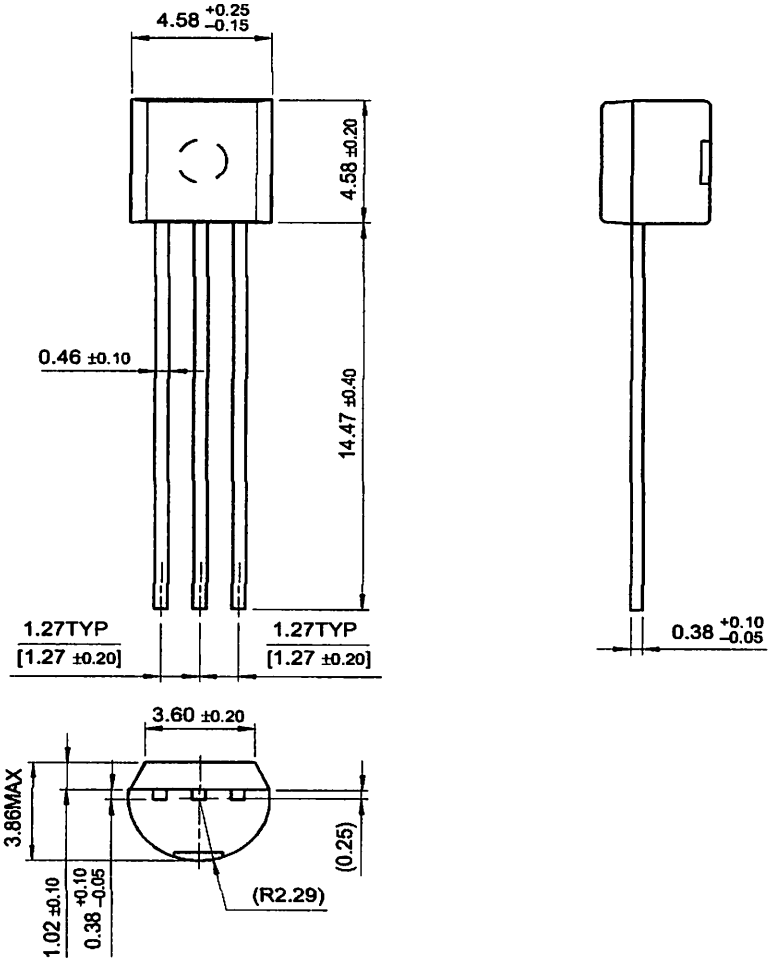


Figure 4. Current Gain Bandwidth Product

©2002 Fairchild Semiconductor Corporation

Package Demensions

TO-92



Dimensions in Millimeters

©2002 Fairchild Semiconductor Corporation

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	MICROWIRE™	SLIENT SWITCHER®	UHC™
Bottomless™	FASTr™	OPTOLOGIC™	SMART START™	UltraFET®
CoolFET™	FRFET™	OPTOPLANAR™	SPM™	VCX™
CROSSVOLT™	GlobalOptoisolator™	PACMAN™	STAR*POWER™	
DenseTrench™	GTO™	POP™	Stealth™	
DOME™	HiSeC™	Power247™	SuperSOT™-3	
EcoSPARK™	I^2C™	PowerTrench®	SuperSOT™-6	
E^2CMOS™	ISOPLANAR™	QFET™	SuperSOT™-8	
EnSigna™	LittleFET™	QS™	SyncFET™	
FACT™	MicroFET™	QT Optoelectronics™	TinyLogic™	
FACT Quiet Series™	MicroPak™	Quiet Series™	TruTranslation™	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	*First Production*	*This datasheet contains preliminary data, and* supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at *any time without notice in order to improve design.*
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

©2002 Fairchild Semiconductor Corporation

National Semiconductor

December 1995

LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

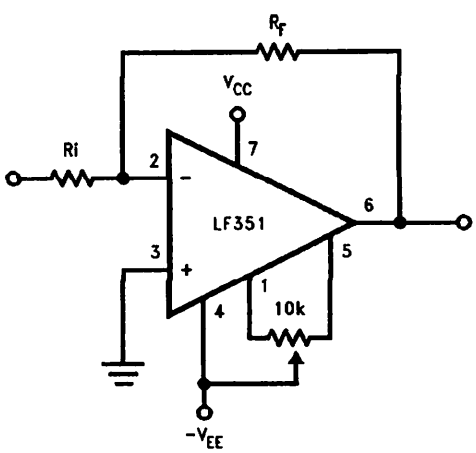
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

Features

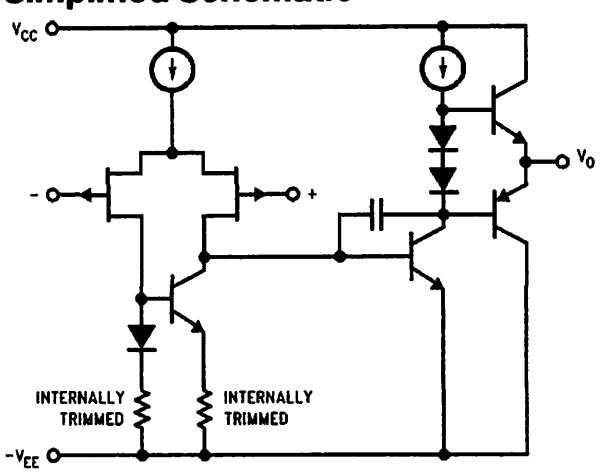
■ Internally trimmed offset voltage	10 mV
■ Low input bias current	50 pA
■ Low input noise voltage	25 nV/$\sqrt{Hz}$
■ Low input noise current	0.01 pA/$\sqrt{Hz}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



TL/H/5648–11

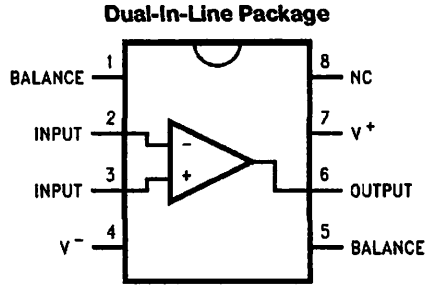
Simplified Schematic



TL/H/5648–12

Connection Diagrams

Dual-In-Line Package



TL/H/5648–13

Order Number LF351M or LF351N
See NS Package Number M08A or N08E

©1995 National Semiconductor Corporation

RRD-B30M125/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Notes 1 and 6)	670 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	
Metal Can	300°C
DIP	260°C
θ_{jA}	
N Package	120°C/W
M Package	TBD
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C *Over Temperature*		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		25	100 4	pA nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ ±70°C		50	200 8	pA nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	3.4	mA

AC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13		V/μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, $f = 1000$ Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, $f = 1000$ Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on the thermal resistance, θ_{JA}.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

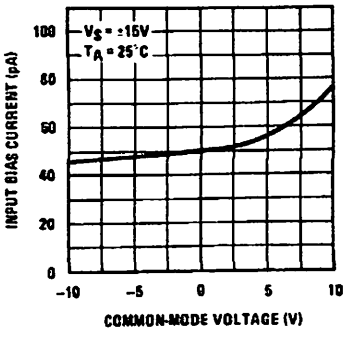
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From ±15V to ±5V.

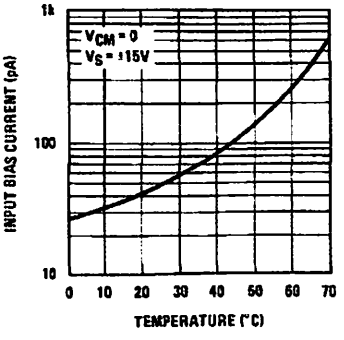
Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

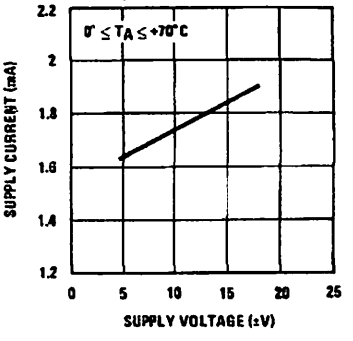
Input Bias Current



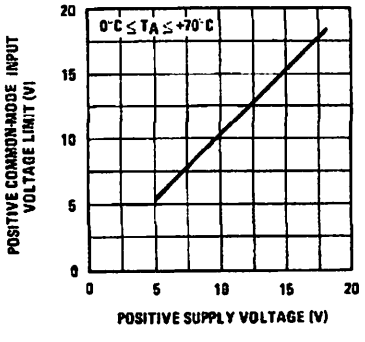
Input Bias Current



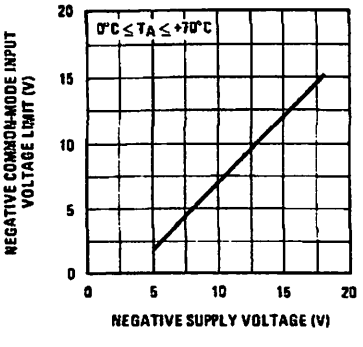
Supply Current



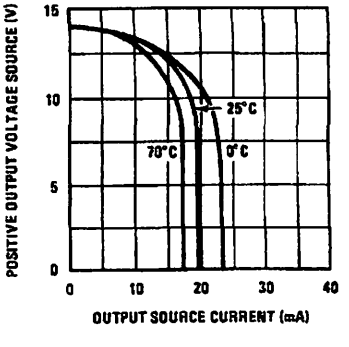
Positive Common-Mode Input Voltage Limit



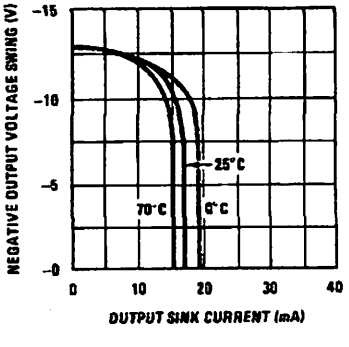
Negative Common-Mode Input Voltage Limit



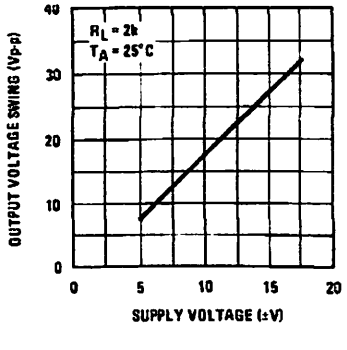
Positive Current Limit



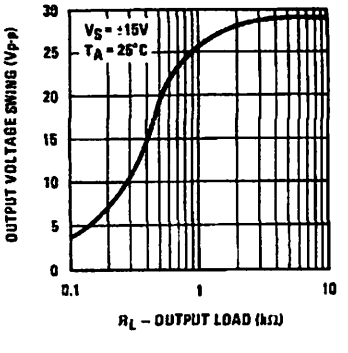
Negative Current Limit



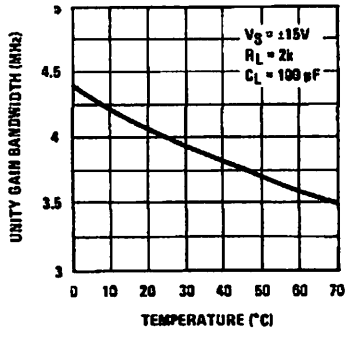
Voltage Swing



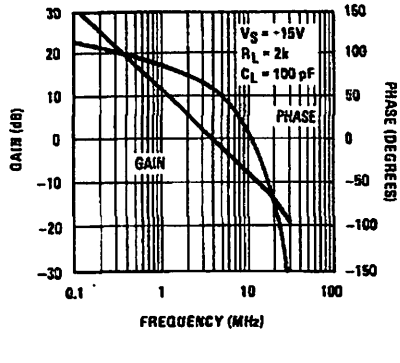
Output Voltage Swing



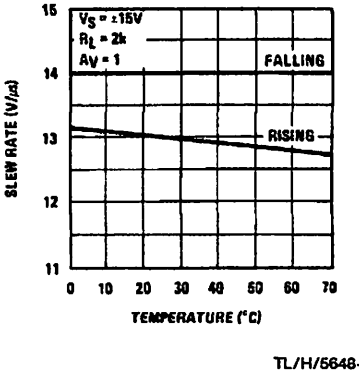
Gain Bandwidth



Bode Plot



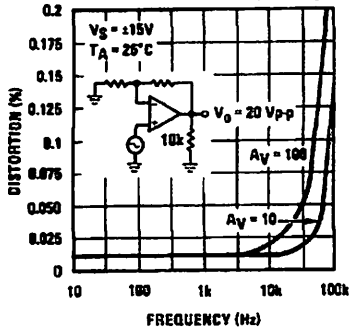
Slew Rate



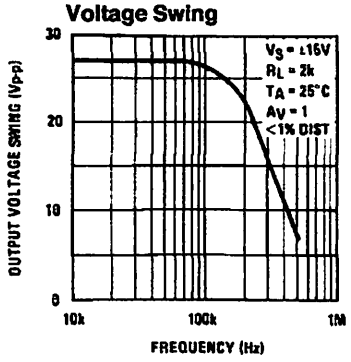
TL/H/5648–2

Typical Performance Characteristics (Continued)

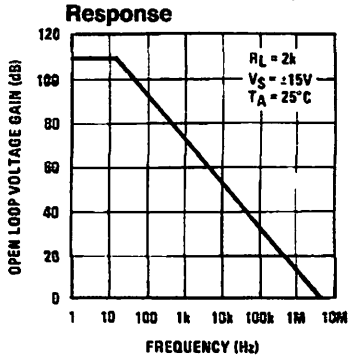
Distortion vs Frequency



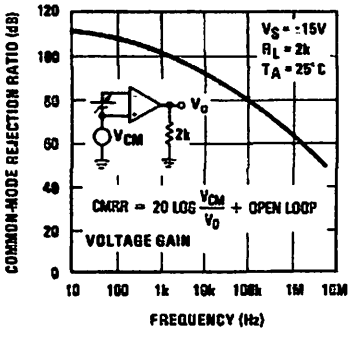
Undistorted Output Voltage Swing



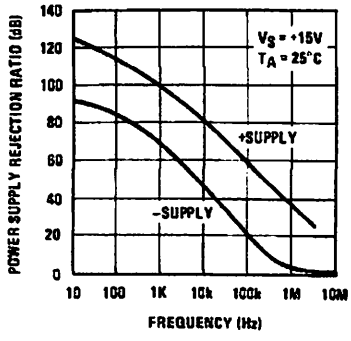
Open Loop Frequency Response



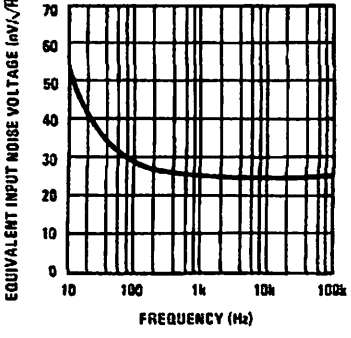
Common-Mode Rejection Ratio



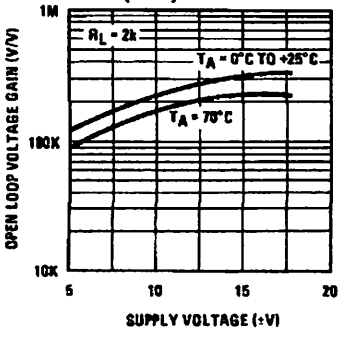
Power Supply Rejection Ratio



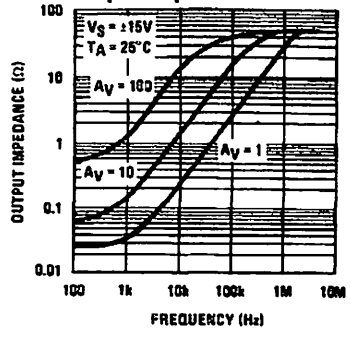
Equivalent Input Noise Voltage



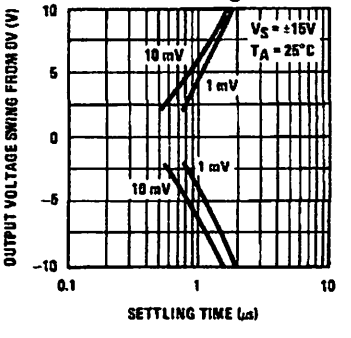
Open Loop Voltage Gain (V/V)



Output Impedance



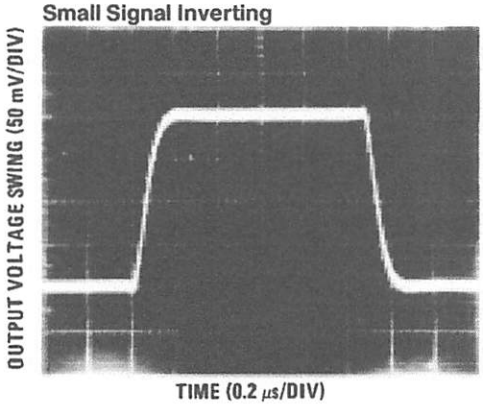
Inverter Settling Time



TL/H/5648–3

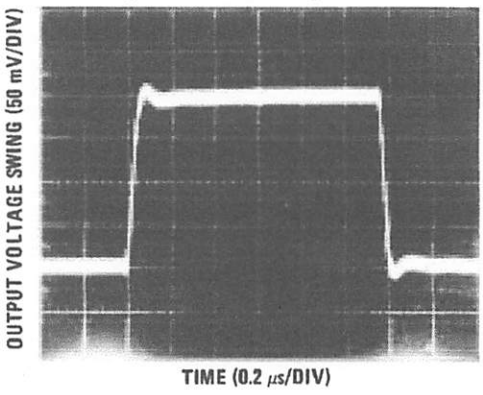
Pulse Response

Small Signal Inverting



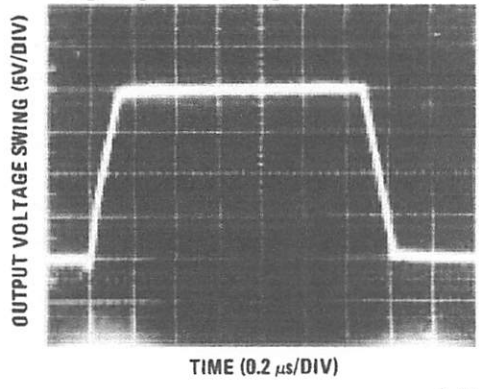
TL/H/5648–4

Small Signal Non-Inverting



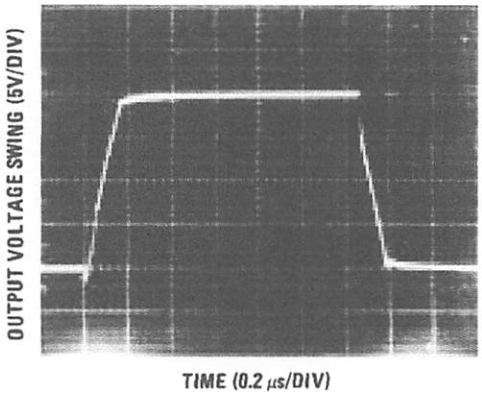
TL/H/5648–5

Large Signal Inverting



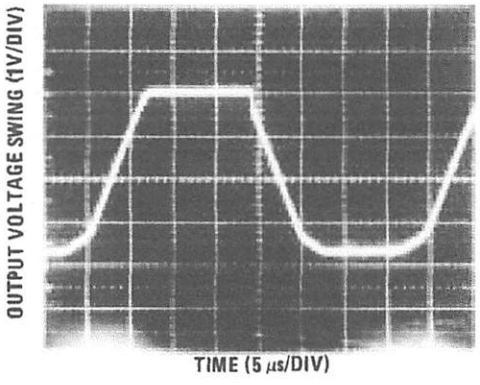
TL/H/5648–6

Large Signal Non-Inverting



TL/H/5648–7

Current Limit ($R_L = 100\Omega$)



TL/H/5648–8

Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

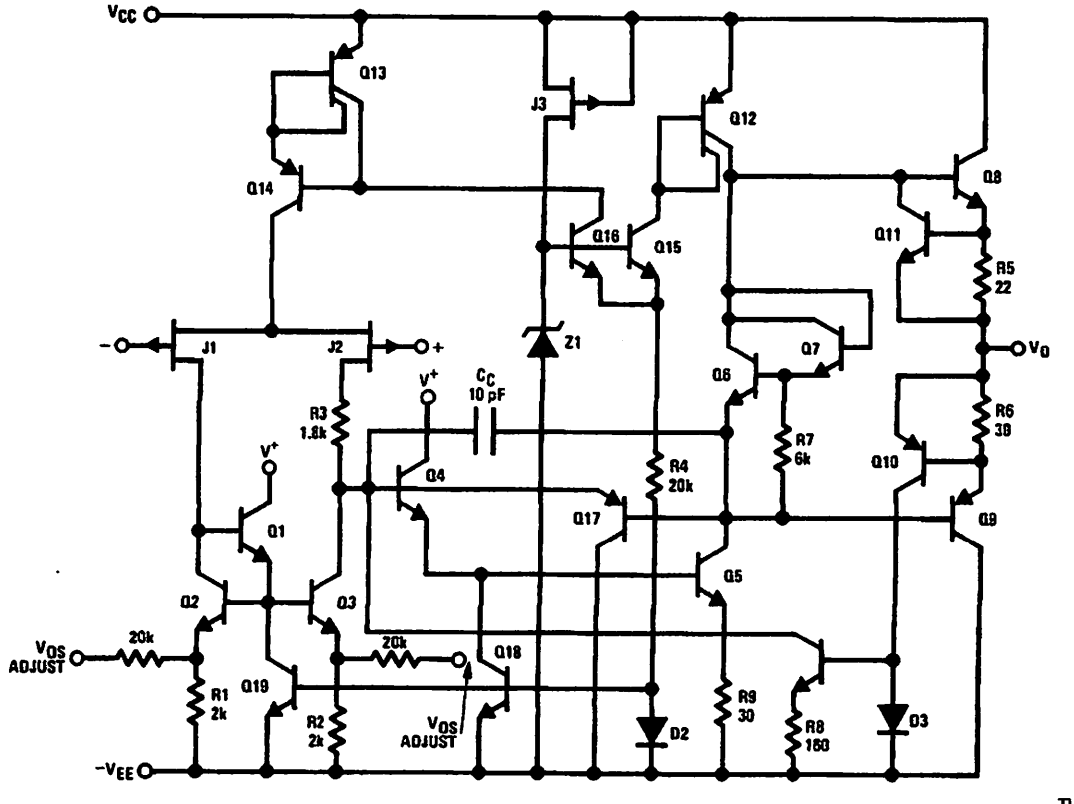
The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

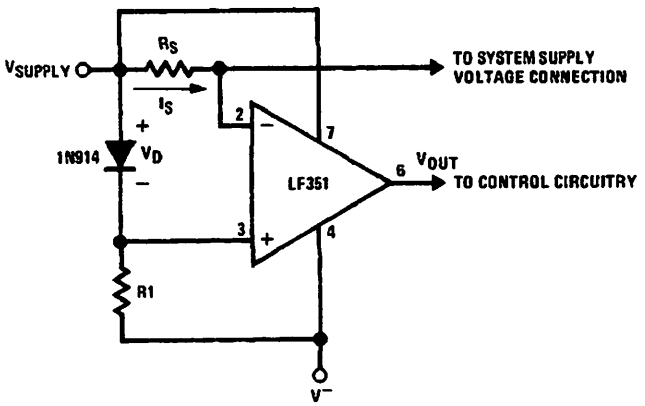
Detailed Schematic



TL/H/5648–9

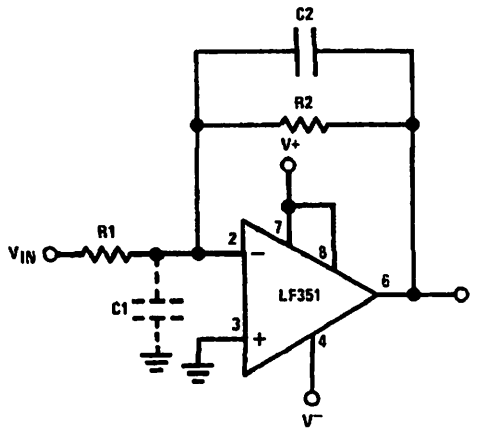
Typical Applications

Supply Current Indicator/Limiter



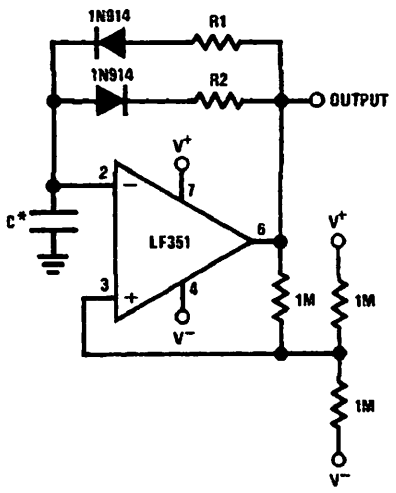
• V_{OUT} switches high when $R_S I_S > V_D$

Hi-Z_{IN} Inverting Amplifier



Parasitic input capacitance C1 ≃ (3 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≃ R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator



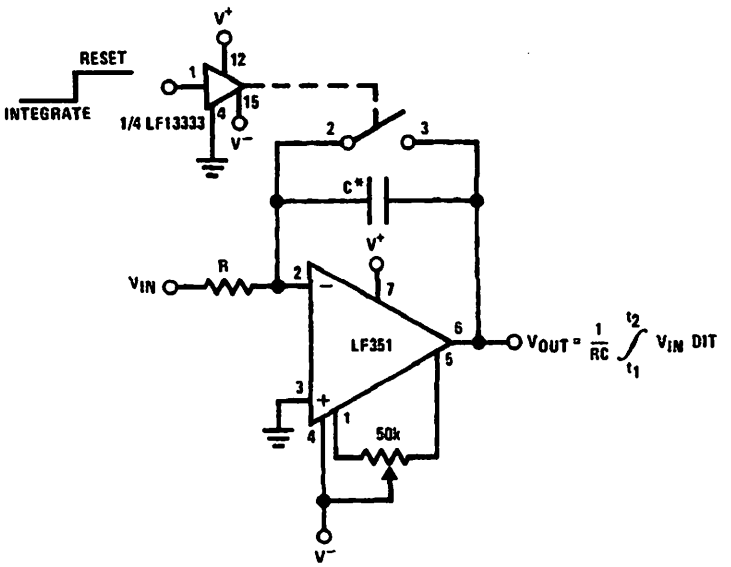
• $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \frac{4.8 - 2V_S}{4.8 - V_S}$

• $t_{OUTPUT\ LOW} \approx R2C\ \ell n \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

Long Time Integrator

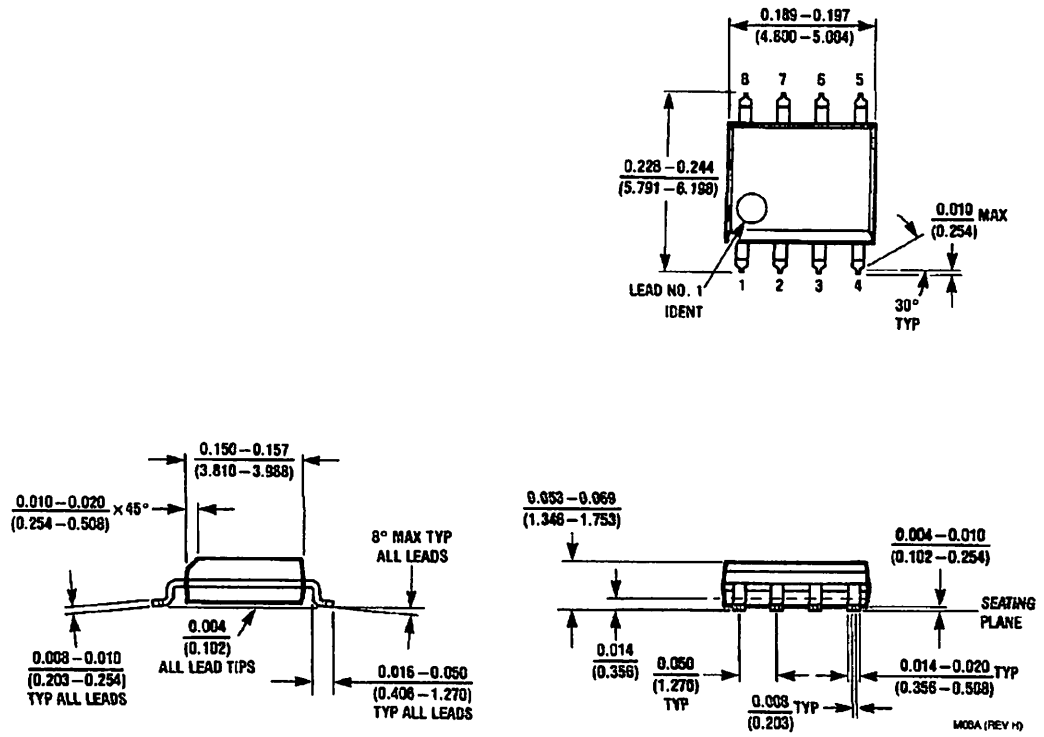


TL/H/5648–10

*Low leakage capacitor

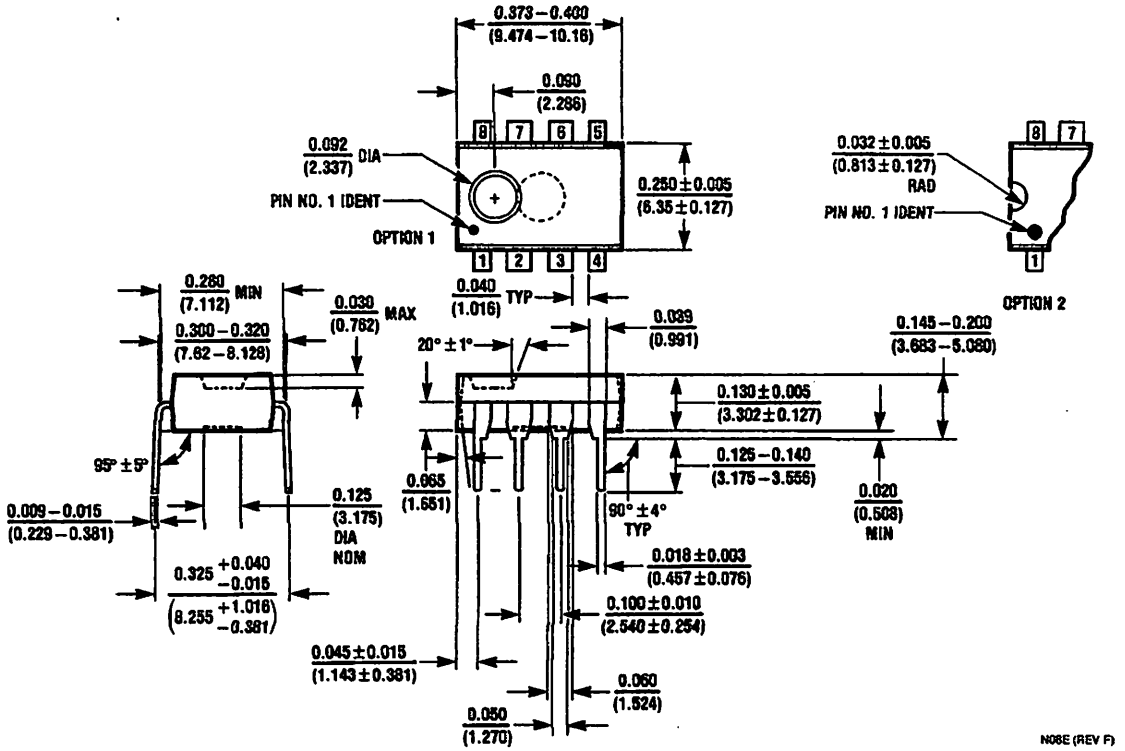
• 50k pot used for less sensitive V_{OS} adjust

Physical Dimensions inches (millimeters)



SO Package (M)
Order Number LF351M
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LF351N
NS Package Number N08E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

National Semiconductor

September 1997

LM35/LM35A/LM35C/LM35CA/LM35D Precision Centigrade Temperature Sensors

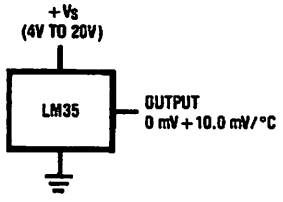
General Description

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to +110°C range (−10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.

Features

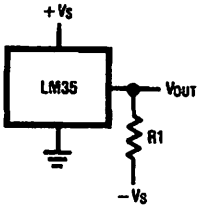
- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full −55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 µA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ω for 1 mA load

Typical Applications



DS005516-3

FIGURE 1. Basic Centirade Temperature Sensor (+2°C to +150°C)



DS005516-4

Choose $R_1 = -V_S/50\ \mu A$

V_{OUT} = +1,500 mV at +150°C
= +250 mV at +25°C
= −550 mV at −55°C

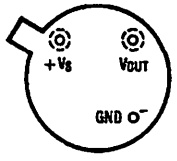
FIGURE 2. Full-Range Centigrade Temperature Sensor

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

© 1997 National Semiconductor Corporation

Connection Diagrams

TO-46
Metal Can Package*



BOTTOM VIEW
DS005516-1

*Case is connected to negative pin (GND)

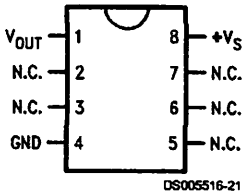
Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

TO-92
Plastic Package

BOTTOM VIEW
DS005516-2

Order Number LM35CZ, LM35CAZ or LM35DZ
See NS Package Number Z03A

SO-8
Small Outline Molded Package

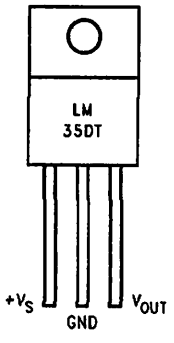


DS005516-21

N.C. = No Connection

Top View
Order Number LM35DM
See NS Package Number M08A

TO-220
Plastic Package*



DS005516-24

*Tab is connected to the negative pin (GND).
Note: The LM35DT pinout is different than the discontinued LM35DP.

Order Number LM35DT
See NS Package Number TA03F

Absolute Maximum Ratings (Note 10)

f Military/Aerospace specified devices are required,)lease contact the National Semiconductor Sales Office/)istributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temp.;	
TO-46 Package,	−60°C to +180°C
TO-92 Package,	−60°C to +150°C
SO-8 Package,	−65°C to +150°C
TO-220 Package,	−65°C to +150°C
Lead Temp.:	
TO-46 Package, (Soldering, 10 seconds)	300°C
TO-92 and TO-220 Package, (Soldering, 10 seconds)	260°C
SO Package (Note 12)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	2500V
Specified Operating Temperature Range: T_{MIN} to T_{MAX} (Note 2)	
LM35, LM35A	−55°C to +150°C
LM35C, LM35CA	−40°C to +110°C
LM35D	0°C to +100°C

Electrical Characteristics

(Notes 1, 6)

Parameter	Conditions	LM35A			LM35CA			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Curacy	T_A=+25°C	±0.2	±0.5		±0.2	±0.5		°C
)te 7)	T_A=−10°C	±0.3			±0.3		±1.0	°C
	T_A=T_{MAX}	±0.4	±1.0		±0.4	±1.0		°C
	T_A=T_{MIN}	±0.4	±1.0		±0.4		±1.5	°C
nlinearity	$T_{MIN} \le T_A \le T_{MAX}$	**±0.18**		**±0.35**	**±0.15**		**±0.3**	°C
)te 8)								
nsor Gain	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°C
erage Slope)								
ad Regulation	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		mV/mA
)te 3) 0≤I_L≤1 mA	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
e Regulation	T_A=+25°C	±0.01	±0.05		±0.01	±0.05		mV/V
)te 3)	4V≤V_S≤30V	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
iescent Current	V_S=+5V, +25°C	56	67		56	67		µA
)te 9)	V_S=+5V	**105**		**131**	**91**		**114**	µA
	V_S=+30V, +25°C	56.2	68		56.2	68		µA
	V_S=+30V	**105.5**		**133**	**91.5**		**116**	µA
ange of	4V≤V_S≤30V, +25°C	0.2	1.0		0.2	1.0		µA
iescent Current	4V≤V_S≤30V	**0.5**		**2.0**	**0.5**		**2.0**	µA
)te 3)								
nperature		**+0.39**		**+0.5**	**+0.39**		**+0.5**	µA/°C
efficient of								
iescent Current								
imum Temperature	In circuit of	+1.5		+2.0	+1.5		+2.0	°C
Rated Accuracy	*Figure 1*, I_L=0							
g Term Stability	T_J=T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Electrical Characteristics

(Notes 1, 6)

Parameter	Conditions	LM35			LM35C, LM35D			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy, LM35, LM35C (Note 7)	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		°C
	T_A=−10°C	±0.5			±0.5		±1.5	°C
	T_A=T_{MAX}	±0.8	±1.5		±0.8		±1.5	°C
	T_A=T_{MIN}	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D (Note 7)	T_A=+25°C				±0.6	±1.5		°C
	T_A=T_{MAX}				±0.9		±2.0	°C
	T_A=T_{MIN}				±0.9		±2.0	°C
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.3**		**±0.5**	**±0.2**		**±0.5**	°C
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°C
Load Regulation (Note 3) $0 \le I_L \le 1$ mA	T_A=+25°C	±0.4	±2.0		±0.4	±2.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±5.0**	**±0.5**		**±5.0**	mV/mA
Line Regulation (Note 3)	T_A=+25°C	±0.01	±0.1		±0.01	±0.1		mV/V
	$4V \le V_S \le 30V$	**±0.02**		**±0.2**	**±0.02**		**±0.2**	mV/V
Quiescent Current (Note 9)	V_S=+5V, +25°C	56	80		56	80		µA
	V_S=+5V	**105**		**158**	**91**		**138**	µA
	V_S=+30V, +25°C	56.2	82		56.2	82		µA
	V_S=+30V	**105.5**		**161**	**91.5**		**141**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +25°C	0.2	2.0		0.2	2.0		µA
	$4V \le V_S \le 30V$	**0.5**		**3.0**	**0.5**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.7**	**+0.39**		**+0.7**	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	T_J=T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Note 1: Unless otherwise noted, these specifications apply: $-55°C \le T_J \le +150°C$ for the LM35 and LM35A; $-40°C \le T_J \le +110°C$ for the LM35C and LM35CA; and $0°C \le T_J \le +100°C$ for the LM35D. V_S=+5Vdc and I_{LOAD}=50 µA, in the circuit of *Figure 2*. These specifications also apply from +2°C to T_{MAX} in the circuit of *Figure 1*. Specifications in **boldface** apply over the full rated temperature range.

Note 2: Thermal resistance of the TO-46 package is 400°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient. Thermal resistance of the small outline molded package is 220°C/W junction to ambient. Thermal resistance of the TO-220 package is 90°C/W junction to ambient. For additional thermal resistance information see table in the Applications section.

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in **boldface** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

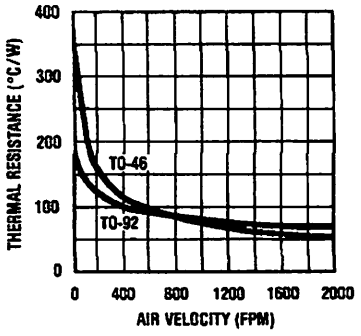
Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 12: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

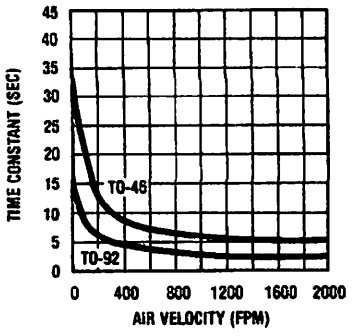
Typical Performance Characteristics

Thermal Resistance Junction to Air



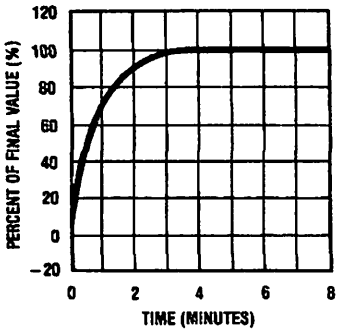
DS005516-25

Thermal Time Constant



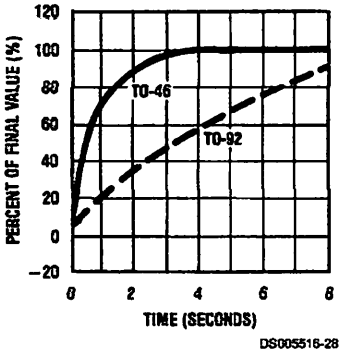
DS005516-26

Thermal Response in Still Air



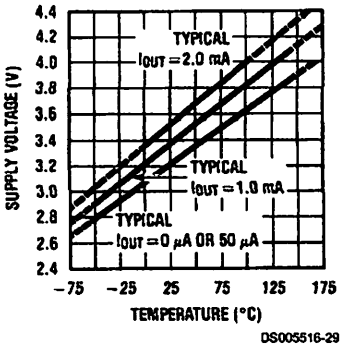
DS005516-27

Thermal Response in Stirred Oil Bath



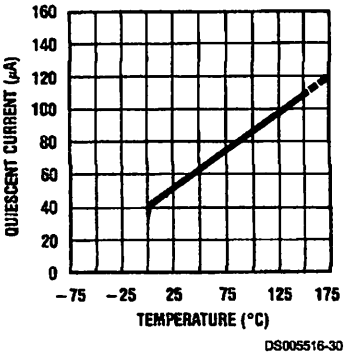
DS005516-28

Minimum Supply Voltage vs. Temperature



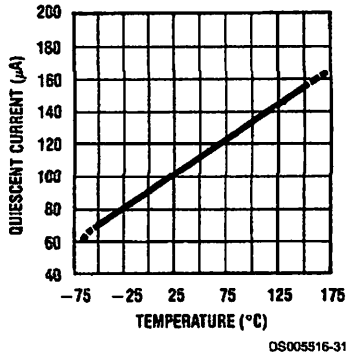
DS005516-29

Quiescent Current vs. Temperature (In Circuit of *Figure 1*.)



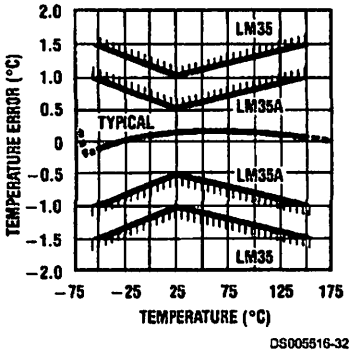
DS005516-30

Quiescent Current vs. Temperature (In Circuit of *Figure 2*.)



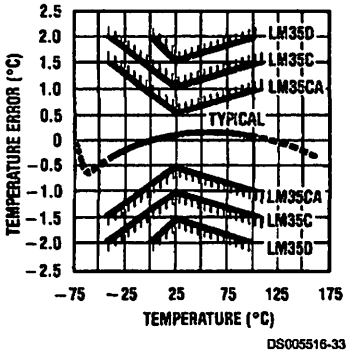
DS005516-31

Accuracy vs. Temperature (Guaranteed)



DS005516-32

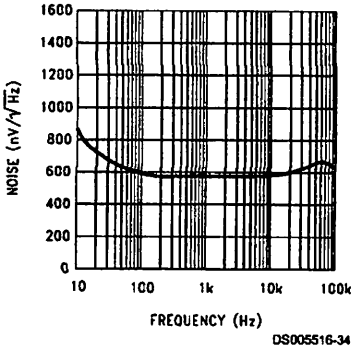
Accuracy vs. Temperature (Guaranteed)



DS005516-33

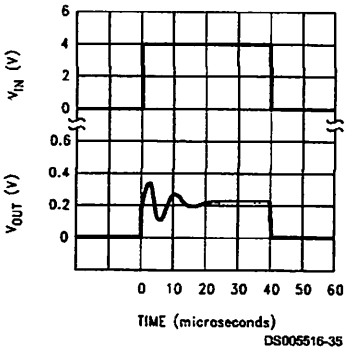
Typical Performance Characteristics (Continued)

Noise Voltage



DS005516-34

Start-Up Response



DS005516-35

Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01°C of the surface temperature.

This presumes that the ambient air temperature is almost the *same as the surface temperature; if the air temperature were* much higher or lower than the surface temperature, the actual temperature of the LM35 die would be at an intermediate temperature between the surface temperature and the air temperature. This is expecially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM35, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM35 die's temperature will not *be affected by the air temperature.*

The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course, in that case the V− terminal of the circuit will be grounded to that metal. Alternatively, the LM35 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM35 and accompanying wiring and circuits must be kept insulated and *dry, to avoid leakage and corrosion. This is especially true if* the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM35 or its connections.

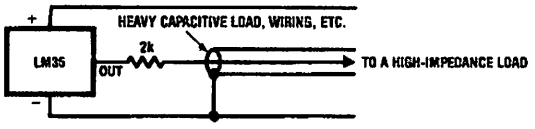
These devices are sometimes soldered to a small light-weight heat fin, to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor, to give the steadiest reading despite small deviations in the air temperature.

Temperature Rise of LM35 Due To Self-heating (Thermal Resistance, Θ_{JA})

	TO-46, no heat sink	TO-46*, small heat fin	TO-92, no heat sink	TO-92**, small heat fin	SO-8 no heat sink	SO-8** small heat fin	TO-220 no heat sink
Still air	400°C/W	100°C/W	180°C/W	140°C/W	220°C/W	110°C/W	90°C/W
Moving air	*100°C/W*	*40°C/W*	*90°C/W*	*70°C/W*	*105°C/W*	*90°C/W*	*26°C/W*
Still oil	100°C/W	40°C/W	90°C/W	70°C/W			
Stirred oil	50°C/W	30°C/W	45°C/W	40°C/W			
(Clamped to metal, Infinite heat sink)	(24°C/W)				(55°C/W)		

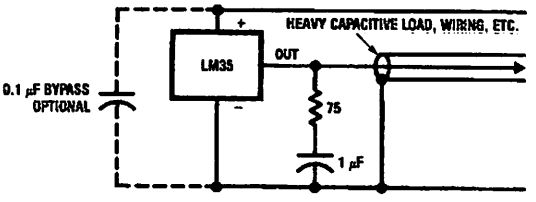
*Wakefield type 201, or 1" disc of 0.020" sheet brass, soldered to case, or similar.
**TO-92 and SO-8 packages glued and leads soldered to 1" square of 1/16" printed circuit board with 2 oz. foil or similar.

Typical Applications



DS005516-19

FIGURE 3. LM35 with Decoupling from Capacitive Load



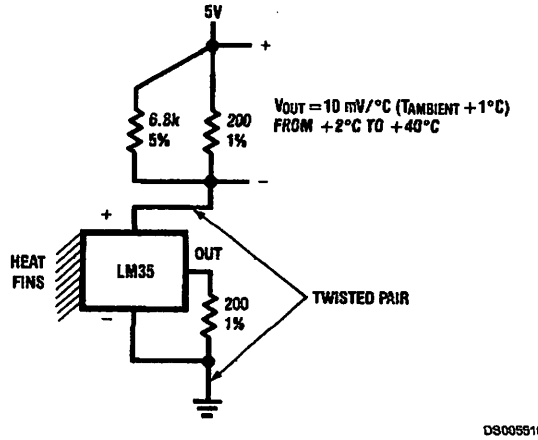
DS005516-20

FIGURE 4. LM35 with R-C Damper

CAPACITIVE LOADS

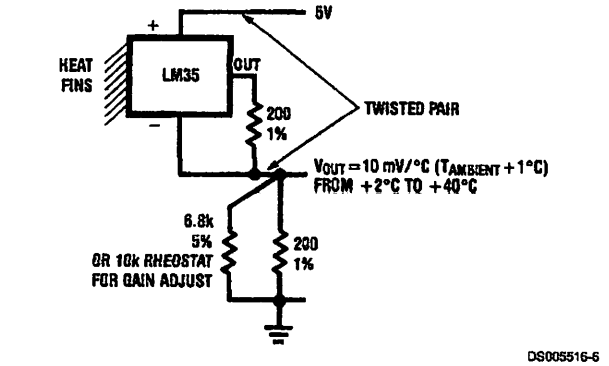
Like most micropower circuits, the LM35 has a limited ability to drive heavy capacitive loads. The LM35 by itself is able to drive 50 pf without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure 3*. Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure 4*.

When the LM35 is applied with a 200Ω load resistor as shown in *Figure 5*, *Figure 6* or *Figure 8* it is relatively immune to wiring capacitance because the capacitance forms a bypass from ground to input, not on the output. However, as with any linear circuit connected to wires in a hostile environment, its performance can be affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR transients, etc, as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from V_{IN} to ground and a series R-C damper such as 75Ω in series with 0.2 or 1 µF from output to ground are often useful. These are shown in *Figure 13*, *Figure 14*, and *Figure 16*.



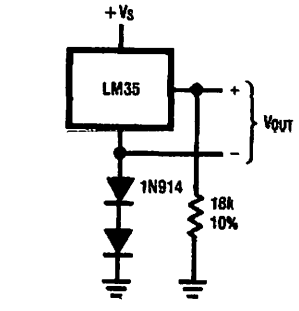
DS005516-5

FIGURE 5. Two-Wire Remote Temperature Sensor (Grounded Sensor)



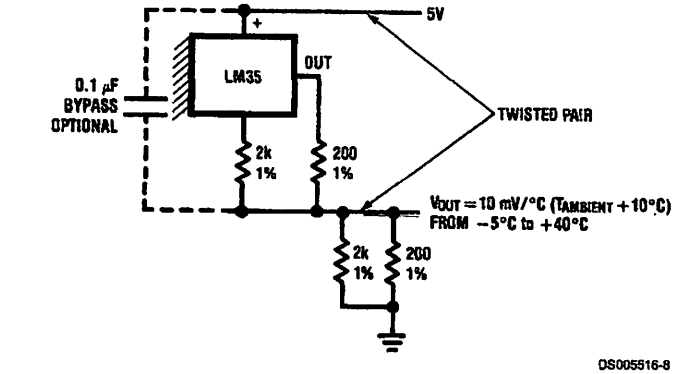
DS005516-6

FIGURE 6. Two-Wire Remote Temperature Sensor (Output Referred to Ground)



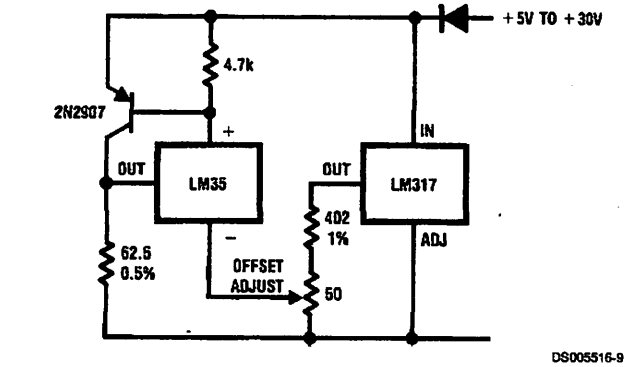
DS005516-7

FIGURE 7. Temperature Sensor, Single Supply, −55° to +150°C



DS005516-8

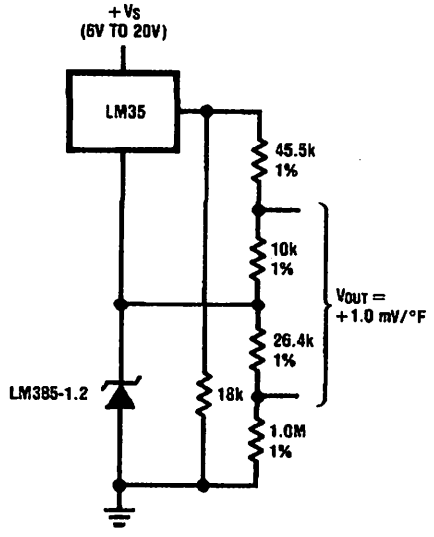
FIGURE 8. Two-Wire Remote Temperature Sensor (Output Referred to Ground)



DS005516-9

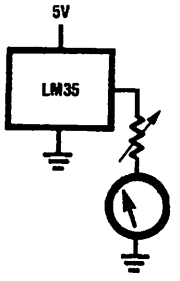
FIGURE 9. 4-To-20 mA Current Source (0°C to +100°C)

Typical Applications (Continued)



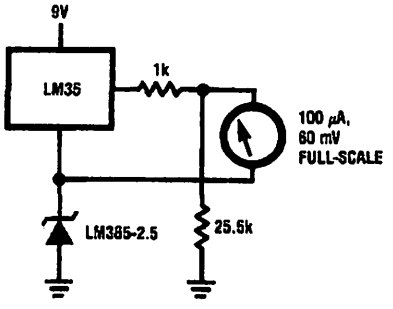
DS005516-10

FIGURE 10. Fahrenheit Thermometer



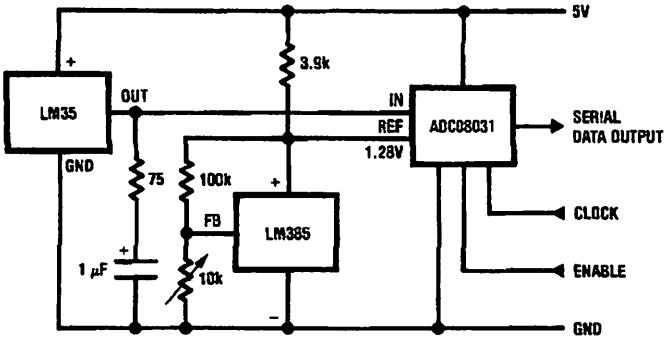
DS005516-11

FIGURE 11. Centigrade Thermometer (Analog Meter)



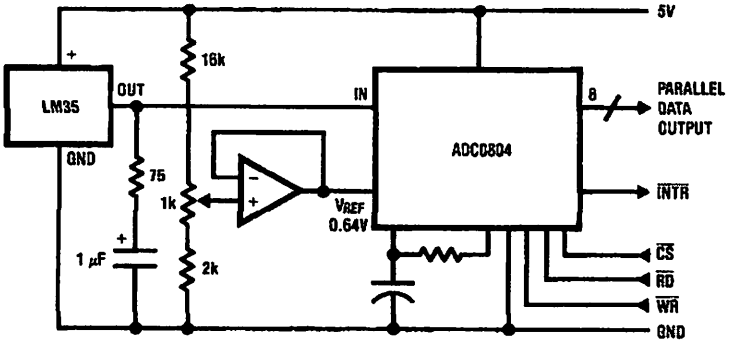
DS005516-12

FIGURE 12. Fahrenheit ThermometerExpanded Scale Thermometer
(50˚ to 80˚ Fahrenheit, for Example Shown)



DS005516-13

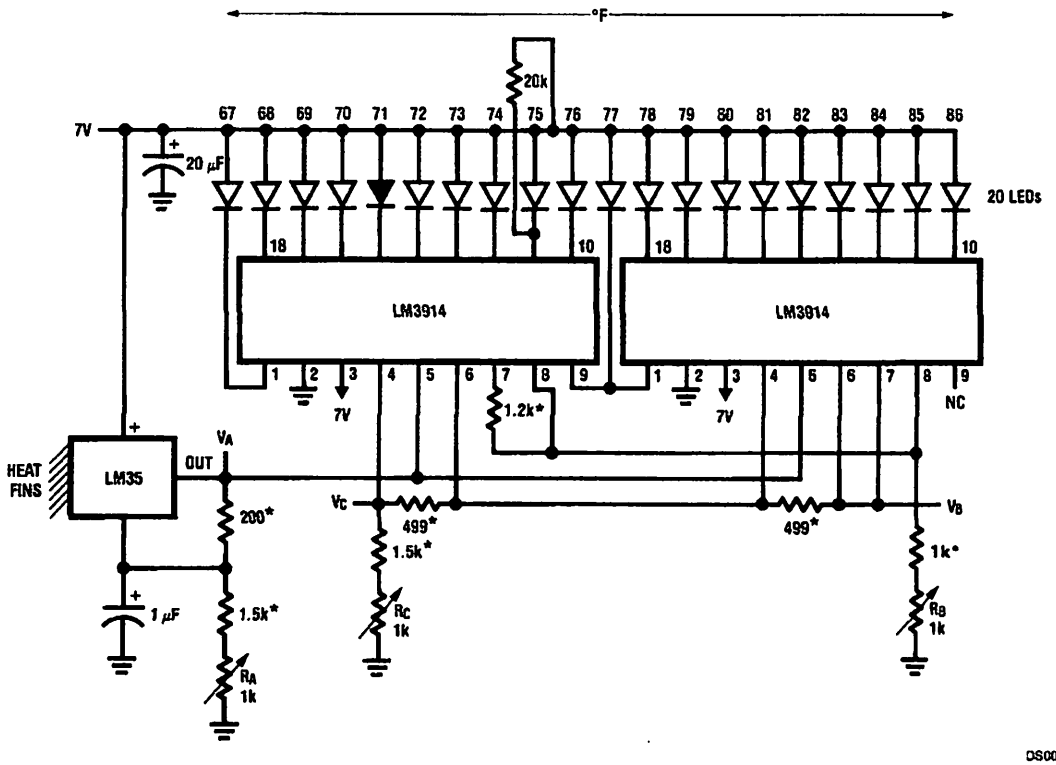
FIGURE 13. Temperature To Digital Converter (Serial Output) (+128˚C Full Scale)



DS005516-14

FIGURE 14. Temperature To Digital Converter (Parallel TRI-STATE® Outputs for *Standard Data Bus to µP Interface*) (128˚C Full Scale)

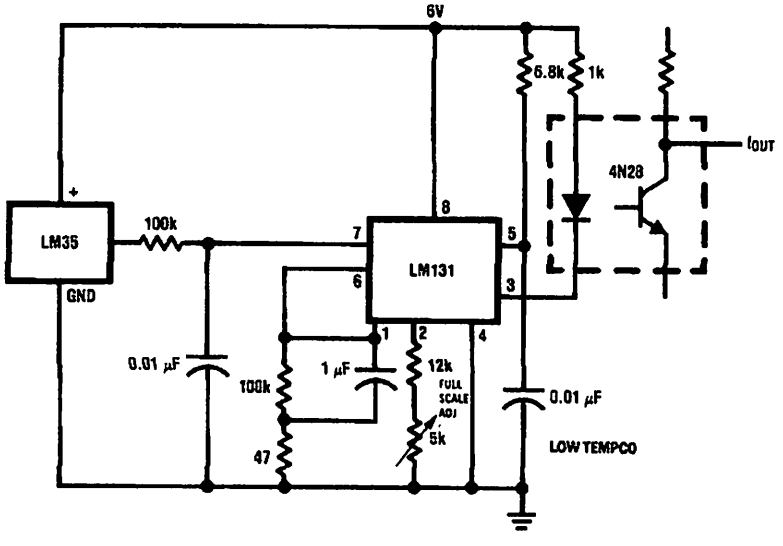
Typical Applications (Continued)



DS005516-16

*=1% or 2% film resistor
Trim R_B for V_B=3.075V
Trim R_C for V_C=1.955V
Trim R_A for V_A=0.075V + 100mV/°C x $T_{ambient}$
Example, V_A=2.275V at 22°C

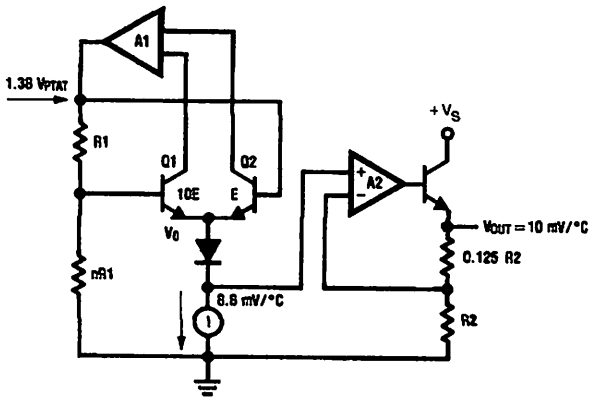
FIGURE 15. Bar-Graph Temperature Display (Dot Mode)



DS005516-15

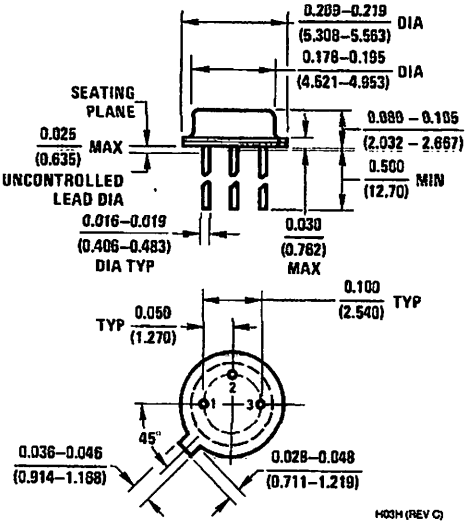
FIGURE 16. LM35 With Voltage-To-Frequency Converter And Isolated Output (2°C to +150°C; 20 Hz to 1500 Hz)

Block Diagram

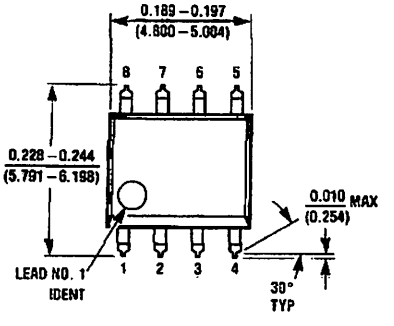


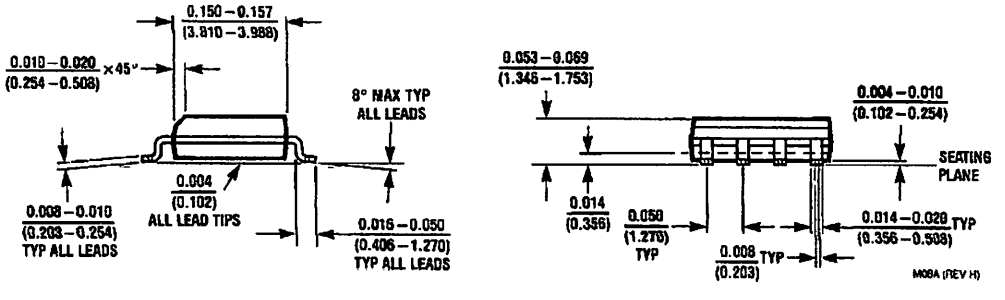
DS005516-23

Physical Dimensions inches (millimeters) unless otherwise noted



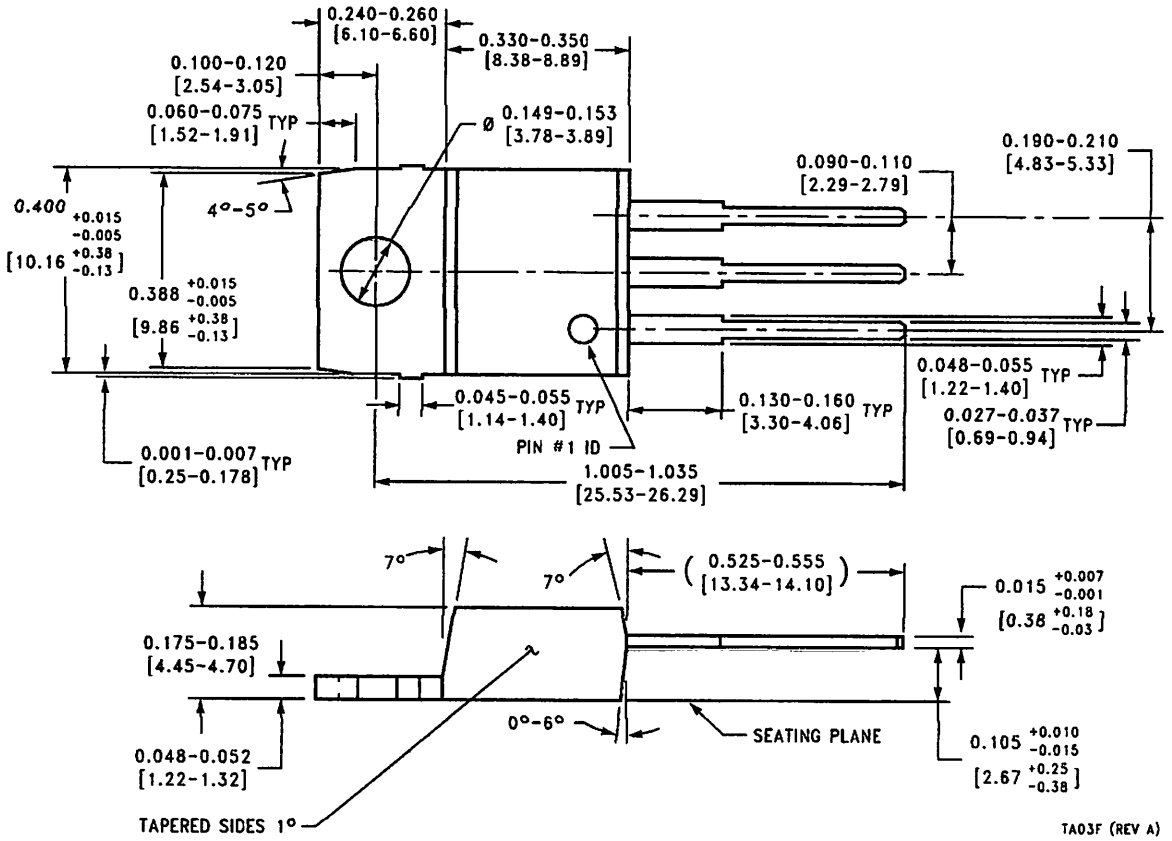
TO-46 Metal Can Package (H)
Order Number LM35H, LM35AH, LM35CH, LM35CAH, or LM35DH
NS Package Number H03H



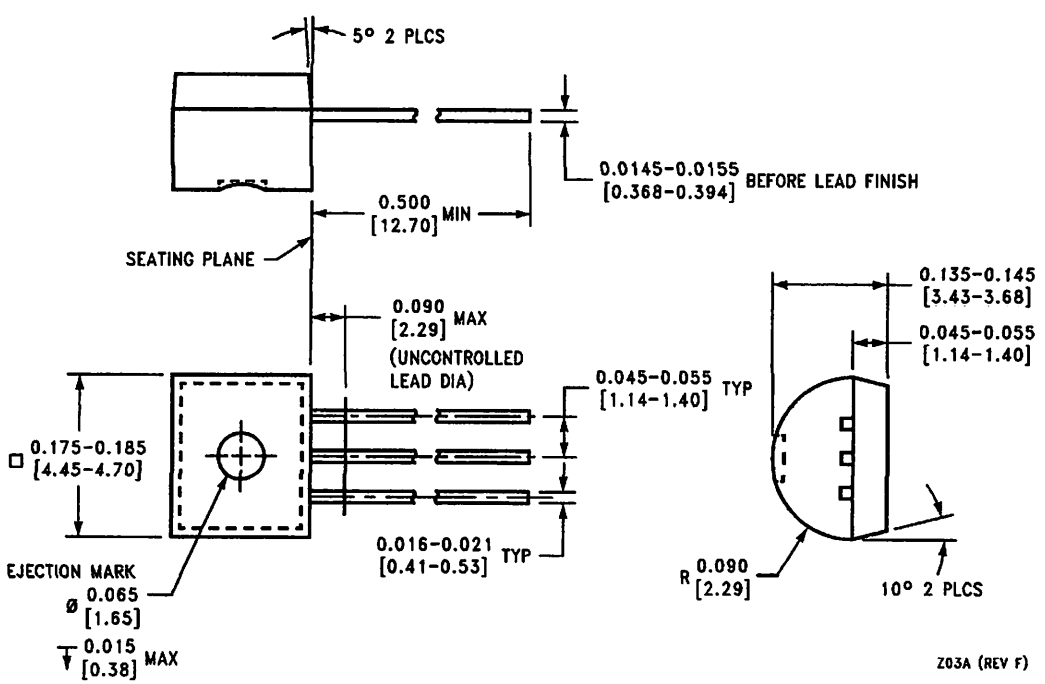


SO-8 Molded Small Outline Package (M)
Order Number LM35DM
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Power Package TO-220 (T)
Order Number LM35DT
NS Package Number TA03F



TO-92 Plastic Package (Z)
Order Number LM35CZ, LM35CAZ or LM35DZ
NS Package Number Z03A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

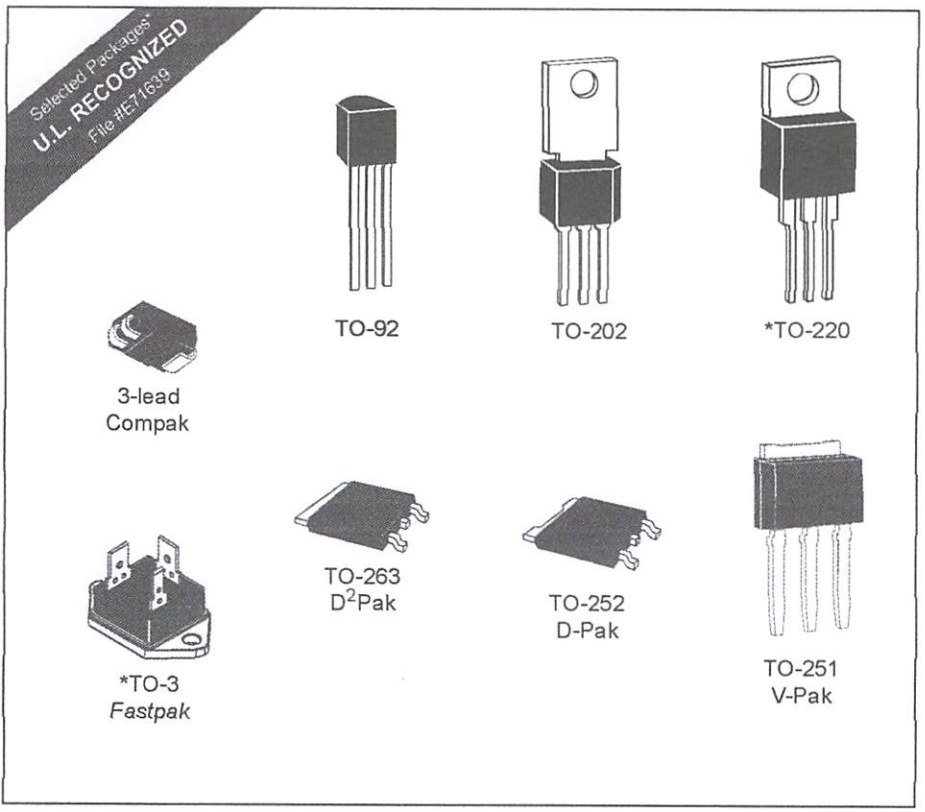
www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

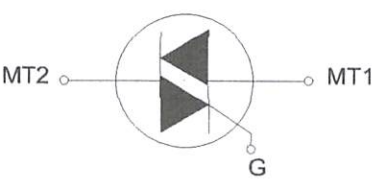
National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.



E2



Triacs

(0.8 A to 35 A)

General Description

These gated triacs from Teccor Electronics are part of a broad line of bidirectional semiconductors. The devices range in current ratings from 0.8 A to 35 A and in voltages from 200 V to 1000 V.

The triac may be gate triggered from a blocking to conduction state for either polarity of applied voltage and is designed for AC switching and phase control applications such as speed and temperature modulation controls, lighting controls, and static switching relays. The triggering signal is normally applied between the gate and MT1.

Isolated packages are offered with internal construction, having the case or mounting tab electrically isolated from the semiconductor chip. This feature facilitates the use of low-cost assembly and convenient packaging techniques. Tape-and-reel capability is available. See "Packing Options" section of this catalog.

All Teccor triacs have glass-passivated junctions to ensure long-term device reliability and parameter stability. Teccor's glass-passivated junctions offer a rugged, reliable barrier against junction contamination.

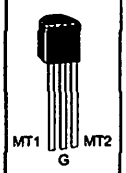
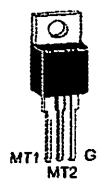
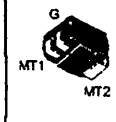
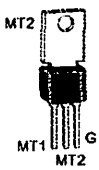
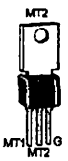
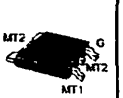
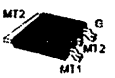
Variations of devices covered in this data sheet are available for custom design applications. Consult factory for more information.

Features

- **Electrically-isolated packages**
- **Glass-passivated junctions**
- **Voltage capability — up to 1000 V**
- **Surge capability — up to 200 A**

Compak Package

- **Surface mount package — 0.8 A and 1 A series**
- **New small profile three-leaded Compak package**
- **Packaged in embossed carrier tape with 2,500 devices per reel**
- **Can replace SOT-223**

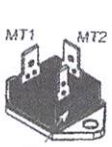
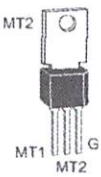
:MS) 4)	Part Number								V_{DRM} (1)	I_{GT} (3) (7) (15)				
	Isolated			Non-isolated										
									Volts	mAmps				
	TO-92	TO-220	Compak	TO-202	TO-220	TO-252 D-Pak	TO-251 V-Pak	TO-263 D^2Pak		QI	QII	QIII	QIV	QIV
AX	See "Package Dimensions" section for variations. (11)								MIN	MAX				TYP
A	Q2X8E3		Q2X3						200	10	10	10		25
	Q4X8E3		Q4X3						400	10	10	10		25
	Q6X8E3		Q8X3						600	10	10	10		25
	Q2X8E4		Q2X4						200	25	25	25		50
	Q4X8E4		Q4X4						400	25	25	25		50
	Q6X8E4		Q6X4						600	25	25	25		50
A	Q201E3		Q2N3						200	10	10	10		25
	Q401E3		Q4N3						400	10	10	10		25
	Q601E3		Q6N3						600	10	10	10		25
	Q201E4		Q2N4						200	25	25	25		50
	Q401E4		Q4N4						400	25	25	25		50
	Q601E4		Q6N4						600	25	25	25		50
A		Q2004L3		Q2004F31		Q2004D3	Q2004V3		200	10	10	10		25
		Q4004L3		Q4004F31		Q4004D3	Q4004V3		400	10	10	10		25
		Q6004L3		Q6004F31		Q6004D3	Q6004V3		600	10	10	10		25
		Q2004L4		Q2004F41		Q2004D4	Q2004V4		200	25	25	25		50
		Q4004L4		Q4004F41		Q4004D4	Q4004V4		400	25	25	25		50
		Q6004L4		Q6004F41		Q6004D4	Q6004V4		600	25	25	25		50
		Q8004L4				Q8004D4	Q8004V4		800	25	25	25		50
		QK004L4				QK004D4	QK004V4		1000	25	25	25		50
A		Q2006L4		Q2006F41	Q2006R4			Q2006N4	200	25	25	25		50
		Q4006L4		Q4006F41	Q4006R4			Q4006N4	400	25	25	25		50
		Q6006L5		Q6006F51	Q6006R5			Q6006N5	600	50	50	50		75
		Q8006L5			Q8006R5			Q8006N5	800	50	50	50		75
		QK006L5			QK006R5			QK006N5	1000	50	50	50		75
A		Q2008L4		Q2008F41	Q2008R4			Q2008N4	200	25	25	25		50
		Q4008L4		Q4008F41	Q4008R4			Q4008N4	400	25	25	25		50
		Q6008L5		Q6008F51	Q6008R5			Q6008N5	600	50	50	50		75
		Q8008L5			Q8008R5			Q8008N5	800	50	50	50		75
		QK008L5			QK008R5			QK008N5	1000	50	50	50		75

"General Notes" on page E2 - 4 and "Electrical Specification Notes" on page E2 - 5.

©2003 Teccor Electronics

I_{DRM} (1) (16) mAmps			V_{TM} (1) (5) Volts	V_{GT} (2) (6) (15) (18) (19) Volts	I_H (1) (8) (12)	I_{GTM} (14)	P_{GM} (14)	$P_{G(AV)}$	I_{TSM} (9) (13) Amps	dv/dt(c) (1) (4) (13)	dv/dt (1) Volts/µSec		t_{gt} (10)	I^2t	di/dt
T_C = 25 °C	T_C = 100 °C	T_C = 125 °C	T_C = 25 °C	T_C = 25 °C	mAmps	Amps	Watts	Watts	60/50 Hz	Volts/µSec	T_C= 100 °C	T_C= 125 °C	µSec	Amp^2Sec	Amps/µSec
MAX			MAX	MAX	MAX					TYP	MIN		TYP		
0.02	0.5	1	1.6	2	15	1	10	0.2	10/8.3	1	40	30	2.5	0.41	20
0.02	0.5	1	1.6	2	15	1	10	0.2	10/8.3	1	35	25	2.5	0.41	20
0.02	0.5	1	1.6	2	15	1	10	0.2	10/8.3	1	25	15	2.5	0.41	20
0.02	0.5	1	1.6	2.5	25	1	10	0.2	10/8.3	1	50	40	3	0.41	20
0.02	0.5	1	1.6	2.5	25	1	10	0.2	10/8.3	1	45	35	3	0.41	20
0.02	0.5	1	1.6	2.5	25	1	10	0.2	10/8.3	1	35	25	3	0.41	20
0.02	0.5	1	1.6	2	15	1	10	0.2	20/16.7	1	40	30	2.5	1.6	30
0.02	0.5	1	1.6	2	15	1	10	0.2	20/16.7	1	40	30	2.5	1.6	30
0.02	0.5	1	1.6	2	15	1	10	0.2	20/16.7	1	30	20	2.5	1.6	30
0.02	0.5	1	1.6	2.5	25	1	10	0.2	20/16.7	1	50	40	3	1.6	30
0.02	0.5	1	1.6	2.5	25	1	10	0.2	20/16.7	1	50	40	3	1.6	30
0.02	0.5	1	1.6	2.5	25	1	10	0.2	20/16.7	1	40	30	3	1.6	30
0.05	0.5	2	1.6	2	20	1.2	15	0.3	55/46	2	50	40	2.5	12.5	50
0.05	0.5	2	1.6	2	20	1.2	15	0.3	55/46	2	50	40	2.5	12.5	50
0.05	0.5	2	1.6	2	20	1.2	15	0.3	55/46	2	40	30	2.5	12.5	50
0.05	0.5	2	1.6	2.5	30	1.2	15	0.3	55/46	2	100	75	3	12.5	50
0.05	0.5	2	1.6	2.5	30	1.2	15	0.3	55/46	2	100	75	3	12.5	50
0.05	0.5	2	1.6	2.5	30	1.2	15	0.3	55/46	2	75	50	3	12.5	50
0.05	0.5	2	1.6	2.5	30	1.2	15	0.3	55/46	2	60	40	3	12.5	50
0.05	3		1.6	2.5	30	1.2	15	0.3	55/46	2	50		3	12.5	50
0.05	0.5	2	1.6	2.5	50	1.6	18	0.5	80/65	4	200	120	3	26.5	70
0.05	0.5	2	1.6	2.5	50	1.6	18	0.5	80/65	4	200	120	3	26.5	70
0.05	0.5	2	1.6	2.5	50	1.6	18	0.5	80/65	4	150	100	3	26.5	70
0.05	0.5	2	1.6	2.5	50	1.6	18	0.5	80/65	4	125	85	3	26.5	70
0.05	3		1.6	2.5	50	1.6	18	0.5	80/65	4	100		3	26.5	70
0.05	0.5	2	1.6	2.5	50	1.8	20	0.5	100/83	4	250	150	3	41	70
0.05	0.5	2	1.6	2.5	50	1.8	20	0.5	100/83	4	250	150	3	41	70
0.05	0.5	2	1.6	2.5	50	1.8	20	0.5	100/83	4	220	125	3	41	70
0.05	0.5	2	1.6	2.5	50	1.8	20	0.5	100/83	4	150	100	3	41	70
0.05	3		1.6	2.5	50	1.8	20	0.5	100/83	4	100		3	41	70

See "General Notes" on page E2 - 4 and "Electrical Specification Notes" on page E2 - 5.

RMS) (16)	Part Number					V_{DRM} (1)	I_{GT} (3) (7) (15)					I_{DRM} (1) (16)		
	Isolated		Non-isolated				mAmps					mAmps		
	 TO-3 Fastpak	TO-220	 TO-202	TO-220	TO-263 D^2Pak	Volts	QI	QII	QIII	QIV	QIV	T_C = 25 °C	T_C = 100 °C	T_C = 125 °C
AX	See "Package Dimensions" section for variations. (11)					MIN	MAX				TYP	MAX		
		Q2010L4		Q2010R4	Q2010N4	200	25	25	25	50		0.05	1	
		Q4010L4		Q4010R4	Q4010N4	400	25	25	25	50		0.05	1	
		Q6010L4		Q6010R4	Q6010N4	600	25	25	25	50		0.05	1	
		Q8010L4		Q8010R4	Q8010N4	800	25	25	25	50		0.1	1	
A		QK010L4		QK010R4	QK010N4	1000	25	25	25	50		0.1	3	
		Q2010L5	Q2010F51	Q2010R5	Q2010N5	200	50	50	50		75	0.05	0.5	2
		Q4010L5	Q4010F51	Q4010R5	Q4010N5	400	50	50	50		75	0.05	0.5	2
		Q6010L5	Q6010F51	Q6010R5	Q6010N5	600	50	50	50		75	0.05	0.5	2
		Q8010L5		Q8010R5	Q8010N5	800	50	50	50		75	0.1	0.5	2
		QK010L5		QK010R5	QK010N5	1000	50	50	50		75	0.1	3	
		Q2015L5		Q2015R5	Q2015N5	200	50	50	50			0.05	0.5	2
5 A		Q4015L5		Q4015R5	Q4015N5	400	50	50	50			0.05	0.5	2
		Q6015L5		*Q6015R5*	*Q6015N5*	*600*	*50*	*50*	*50*			*0.05*	*0.5*	2
		Q8015L5		Q8015R5	Q8015N5	800	50	50	50			0.1	1	3
		QK015L5		QK015R5	QK015N5	1000	50	50	50			0.1	3	
				Q2025R5	Q2025N5	200	50	50	50			0.1	1	3
				Q4025R5	Q4025N5	400	50	50	50			0.1	1	3
				Q6025R5	Q6025N5	600	50	50	50			0.1	1	3
5 A				Q8025R5	Q8025N5	800	50	50	50			0.1	1	3
				QK025R5	QK025N5	1000	50	50	50			0.1	3	
	Q6025P5					600	50	50	50		120	0.1		5
	Q8025P5					800	50	50	50		120	0.1		5
5 A	Q6035P5					600	50	50	50		120	0.1		5
	Q8035P5					800	50	50	50		120	0.1		5

ecific Test Conditions

— Maximum rate-of-change of on-state current; I_{GT} = 200 mA with ±0.1 µs rise time

t — Critical rate-of-rise of off-state voltage at rated V_{DRM} gate open

t(c) — Critical rate-of-rise of commutation voltage at rated V_{DRM} and $I_{T(RMS)}$ commutating di/dt = 0.54 rated $I_{T(RMS)}$/ms; gate unenergized

- RMS surge (non-repetitive) on-state current for period of 8.3 ms for fusing

— Peak off-state current, gate open; V_{DRM} = maximum rated value

- DC gate trigger current in specific operating quadrants; V_D = 12 V dc

— Peak gate trigger current

Holding current (DC); gate open

s) — RMS on-state current conduction angle of 360°

— Peak one-cycle surge

v) — Average gate power dissipation

— Peak gate power dissipation; $I_{GT} \le I_{GTM}$

- Gate controlled turn-on time; I_{GT} = 200 mA with 0.1 µs rise time

V_{DRM} — Repetitive peak blocking voltage

V_{GT} — DC gate trigger voltage; V_D = 12 V dc; R_L = 60 Ω

V_{TM} — Peak on-state voltage at maximum rated RMS current

General Notes

- All measurements are made at 60 Hz with a resistive load at an ambient temperature of +25 °C unless specified otherwise.
- *Operating temperature range (T_J) is -65 °C to +125 °C for TO-92, -25 °C to +125 °C for Fastpak, and -40 °C to +125 °C for all other devices.*
- Storage temperature range (T_S) is -65 °C to +150 °C for TO-92, -40 °C to +150 °C for TO-202, and -40 °C to +125 °C for all other devices.
- Lead solder temperature is a maximum of 230 °C for 10 seconds, *maximum; ≥1/16" (1.59 mm) from case.*
- The case temperature (T_C) is measured as shown on the dimensional outline drawings. See "Package Dimensions" section of this catalog.

©2003 Teccor Electronics

V_{TM}	V_{GT}	I_H	I_{GTM}	P_{GM}	$P_{G(AV)}$	I_{TSM}	dv/dt(c)	dv/dt		t_{gt}	I^2t	di/dt
(1) (5)	(2) (6) (15) (18) (19)	(1) (8) (12)	(14)	(14)		(9) (13)	(1) (4) (13)	(1)		(10) (17)		
Volts	Volts					Amps		Volts/µSec				
T_C = 25 °C	T_C = 25 °C	mAmps	Amps	Watts	Watts	60/50 Hz	Volts/µSec	T_C = 100 °C	T_C = 125 °C	µSec	$Amps^2Sec$	Amps/µSec
MAX	MAX	MAX					TYP	MIN		TYP		
1.6	2.5	35	1.8	20	0.5	120/100	2	150		3	60	70
1.6	2.5	35	1.8	20	0.5	120/100	2	150		3	60	70
1.6	2.5	35	1.8	20	0.5	120/100	2	100		3	60	70
1.6	2.5	35	1.8	20	0.5	120/100	2	75		3	60	70
1.6	2.5	35	1.8	20	0.5	120/100	2	50		3	60	70
1.6	2.5	50	1.8	20	0.5	120/100	4	350	225	3	60	70
1.6	2.5	50	1.8	20	0.5	120/100	4	350	225	3	60	70
1.6	2.5	50	1.8	20	0.5	120/100	4	300	200	3	60	70
1.6	2.5	50	1.8	20	0.5	120/100	4	250	175	3	60	70
1.6	2.5	50	1.8	20	0.5	120/100	4	150		3	60	70
1.6	2.5	70	2	20	0.5	200/167	4	400	275	4	166	100
1.6	2.5	70	2	20	0.5	200/167	4	400	275	4	166	100
1.6	2.5	70	2	20	0.5	200/167	4	350	225	4	166	100
1.6	2.5	70	2	20	0.5	200/167	4	300	200	4	166	100
1.6	2.5	70	2	20	0.5	200/167	4	200		4	166	100
1.8	2.5	100	2	20	0.5	200/167	5	400	275	4	166	100
1.8	2.5	100	2	20	0.5	200/167	5	400	275	4	166	100
1.8	2.5	100	2	20	0.5	200/167	5	350	225	4	166	100
1.8	2.5	100	2	20	0.5	200/167	5	300	200	4	166	100
1.8	2.5	100	2	20	0.5	200/167	5	200		4	166	100
1.4	2.75	50	2	20	0.5	250/220	5	550	475	3	260	100
1.4	2.75	50	2	20	0.5	250/220	5	450	400	3	260	100
1.5	2.75	50	2	20	0.5	350/300	5	550	475	3	508	100
1.5	2.75	50	2	20	0.5	350/300	5	450	400	3	508	100

Electrical Specification Notes

(1) For either polarity of MT2 with reference to MT1 terminal

(2) For either polarity of gate voltage (V_{GT}) with reference to MT1 terminal

(3) See Gate Characteristics and Definition of Quadrants.

(4) See Figure E2.1 through Figure E2.7 for current rating at specific operating temperature.

(5) See Figure E2.8 through Figure E2.10 for i_T versus v_T.

(6) See Figure E2.12 for V_{GT} versus T_C.

(7) See Figure E2.11 for I_{GT} versus T_C.

(8) See Figure E2.14 for I_H versus T_C.

(9) See Figure E2.13 for surge rating with specific durations.

(10) See Figure E2.15 for t_{gt} versus I_{GT}.

(11) See package outlines for lead form configurations. When ordering special lead forming, add type number as suffix to part number.

(12) Initial on-state current = 200 mA dc for 0.8 A to10 A devices, 400 mA dc for 15 A to 35 A devices

(13) See Figure E2.1 through Figure E2.6 for maximum allowable case temperature at maximum rated current.

(14) Pulse width ≤10 µs; $I_{GT} \leq I_{GTM}$

(15) R_L = 60 Ω for 0.8 A to10 A triacs; R_L = 30 Ω for 15 A to 35 A triacs

(16) $T_C = T_J$ for test conditions in off state

(17) I_{GT} = 300 mA for 25 A and 35 A devices

(18) Quadrants I, II, III only

(19) Minimum non-trigger V_{GT} at 125 °C is 0.2 V for all except 50 mA MAX QIV devices which are 0.2 V at 110 °C.

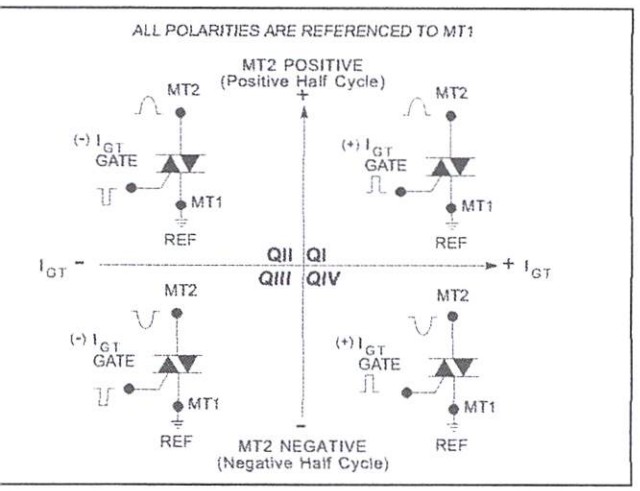
Gate Characteristics

Teccor triacs may be turned on between gate and MT1 terminals in the following ways:

- In-phase signals (with standard AC line) using Quadrants I and III
- Application of unipolar pulses (gate always positive or negative), using Quadrants II and III with negative gate pulses and Quadrants I and IV with positive gate pulses

  However, due to higher gate requirements for Quadrant IV, it is recommended that only negative pulses be applied. If positive pulses are required, see "Sensitive Triacs" section of this catalog or contact the factory. Also, see Figure AN1002.8, "Amplified Gate" Thyristor Circuit.

ll cases, if maximum surge capability is required, pulses uld be a minimum of one magnitude above I_{GT} rating with a ep rising waveform (≤1 µs rise time).



nition of Quadrants

Electrical Isolation

Teccor's isolated triac packages will withstand a minimum high potential test of 2500 V ac rms from leads to mounting tab or base, over the operating temperature range of the device. The following isolation table shows standard and optional isolation ratings.

Electrical Isolation from Leads to Mounting Tab *		
V AC RMS	TO-220 Isolated	Fastpak Isolated
2500	Standard	Standard
4000	Optional **	N/A

* UL Recognized File E71639

** For 4000 V isolation, use V suffix in part number.

Thermal Resistance (Steady State)
$R_{\theta JC}$ [$R_{\theta JA}$] (TYP.) °C/W

kage Code	P	E	C	F	F2	L	R	D	V	N
Type	TO-3 Fastpak	TO-92	Compak	TO-202 Type 1	TO-202 Type 2	TO-220 Isolated	TO-220 Non-isolated	TO-252 D-Pak	TO-251 V-Pak	TO-263 D^2Pak
0.8 A		60 [135]	60 *							
1 A		50 [95]	40 *							
4 A				3.5 [45]	6 [70]	3.6 [50]		3.5	6.0 [70]	
6 A				3.8		3.3	1.8 [45]			1.8
8 A				3.3		2.8	1.5			1.5
10 A				3.5		2.6	1.3			1.3
15 A						2.1	1.1			1.1
25 A	1.6						*0.89*			*0.89*
35 A	1.5									

unted on 1 cm^2 copper foil surface; two-ounce copper foil

©2003 Teccor Electronics

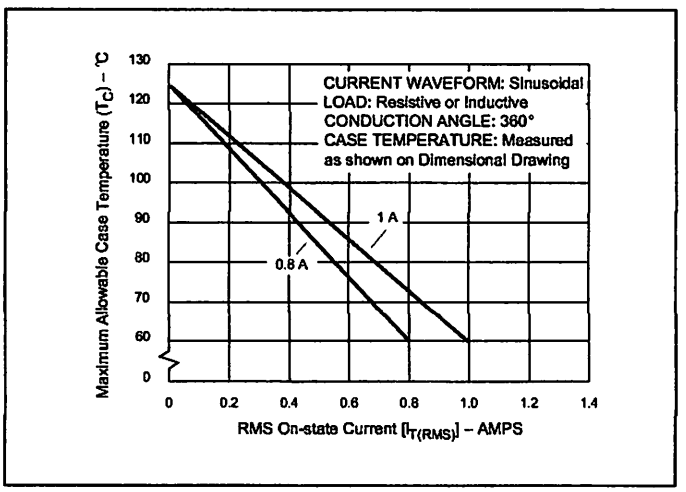


Figure E2.1 Maximum Allowable Case Temperature versus On-state Current (0.8 A and 1 A)

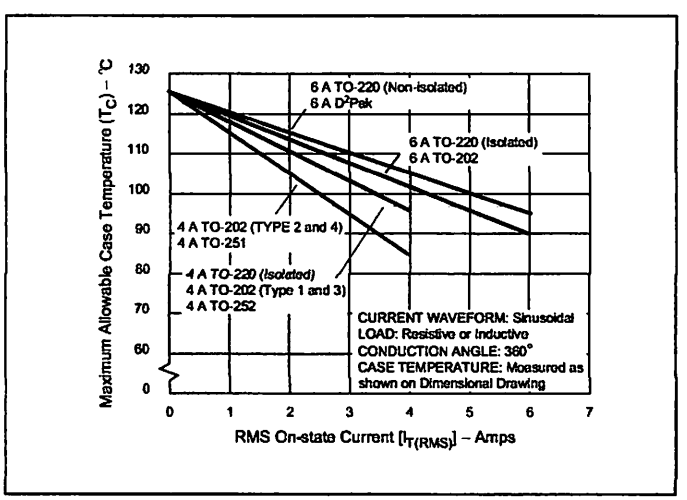


Figure E2.2 Maximum Allowable Case Temperature versus On-state Current (4 A and 6 A)

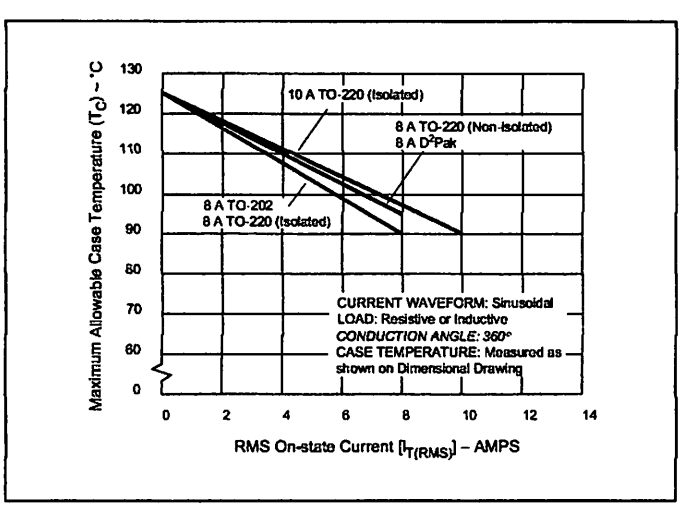


Figure E2.3 Maximum Allowable Case Temperature versus On-state Current (8 A and 10 A)

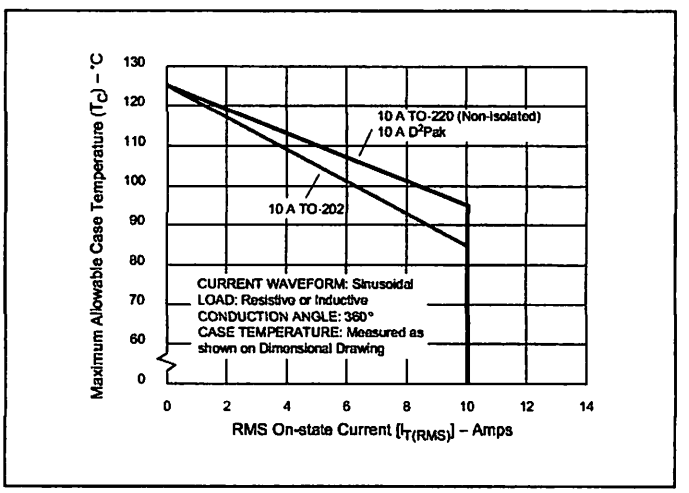


Figure E2.4 Maximum Allowable Case Temperature versus On-state Current (10 A)

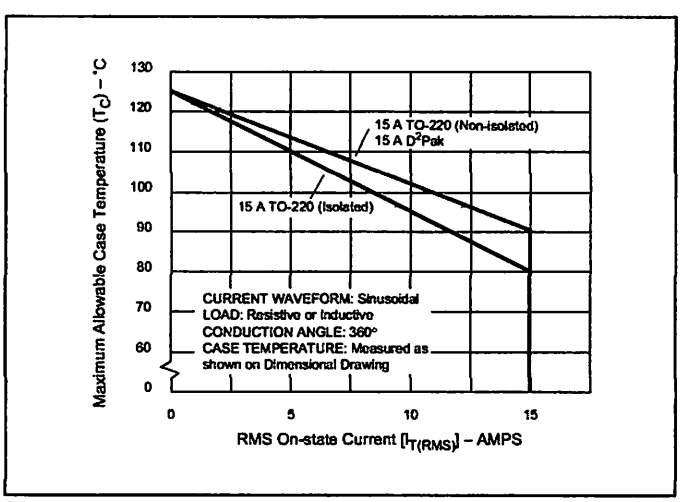


Figure E2.5 Maximum Allowable Case Temperature versus On-state Current (15 A)

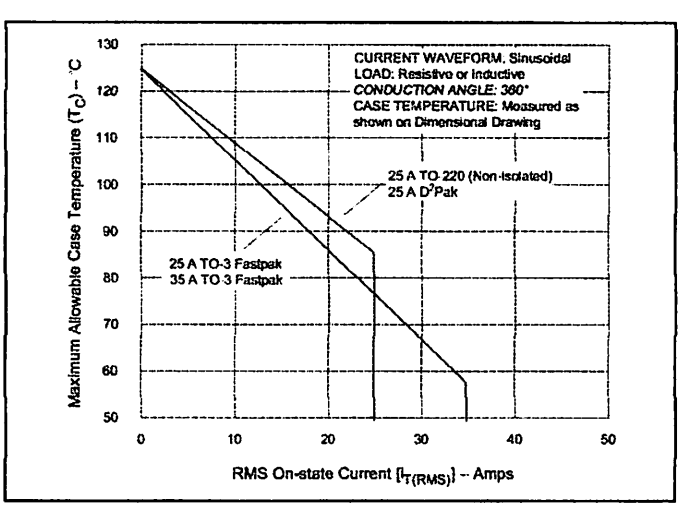
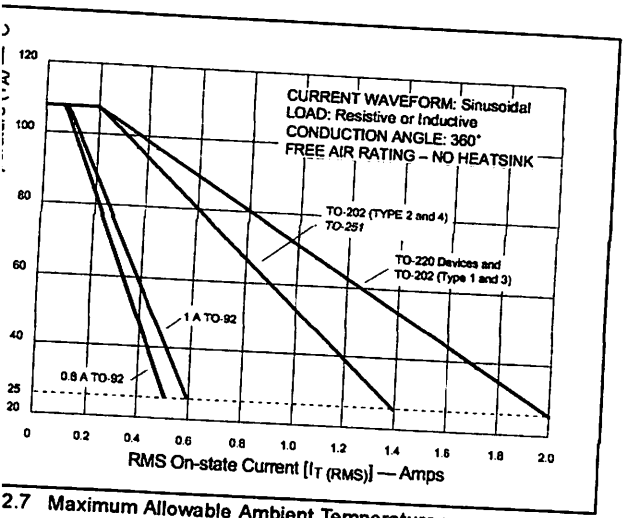
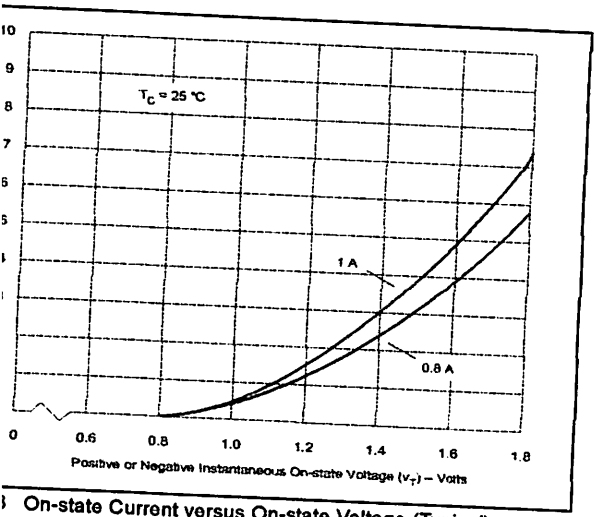


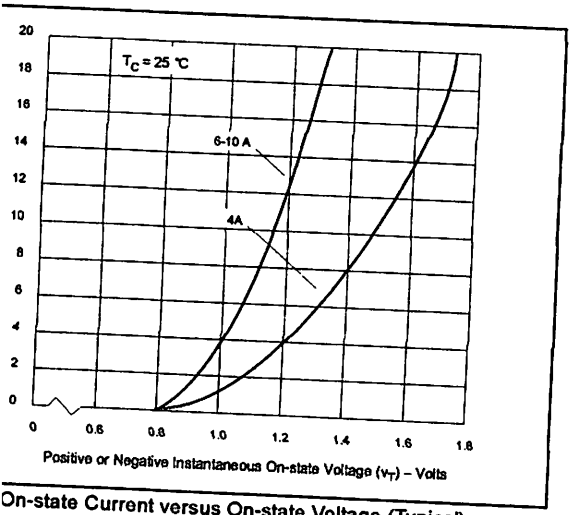
Figure E2.6 Maximum Allowable Case Temperature versus On-state Current (25 A and 35 A)



2.7 Maximum Allowable Ambient Temperature versus On-state Current



On-state Current versus On-state Voltage (Typical) (0.8 A and 1 A)



On-state Current versus On-state Voltage (Typical) (4 A, 6 A, 8 A, and 10 A)

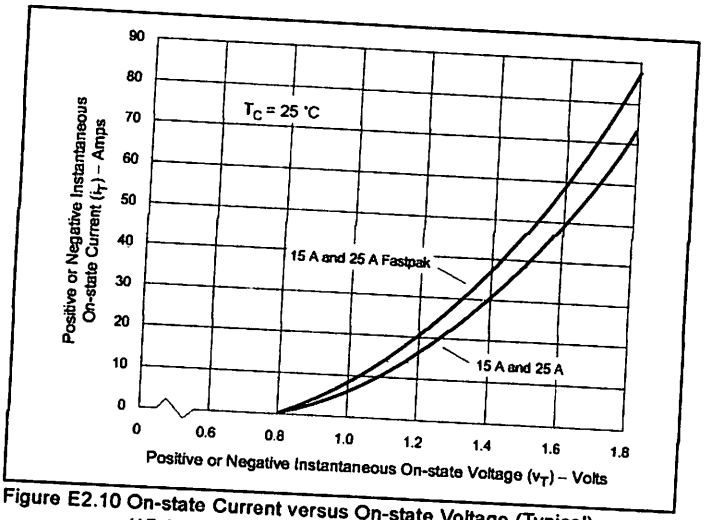


Figure E2.10 On-state Current versus On-state Voltage (Typical) (15 A and 25 A)

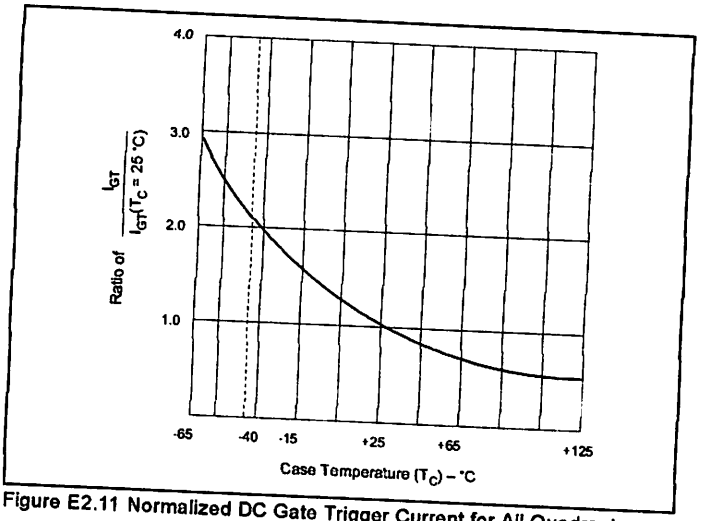


Figure E2.11 Normalized DC Gate Trigger Current for All Quadrants versus Case Temperature

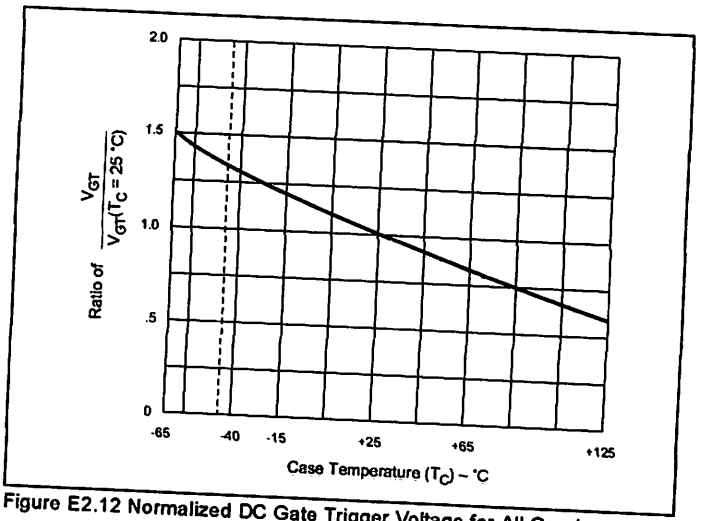
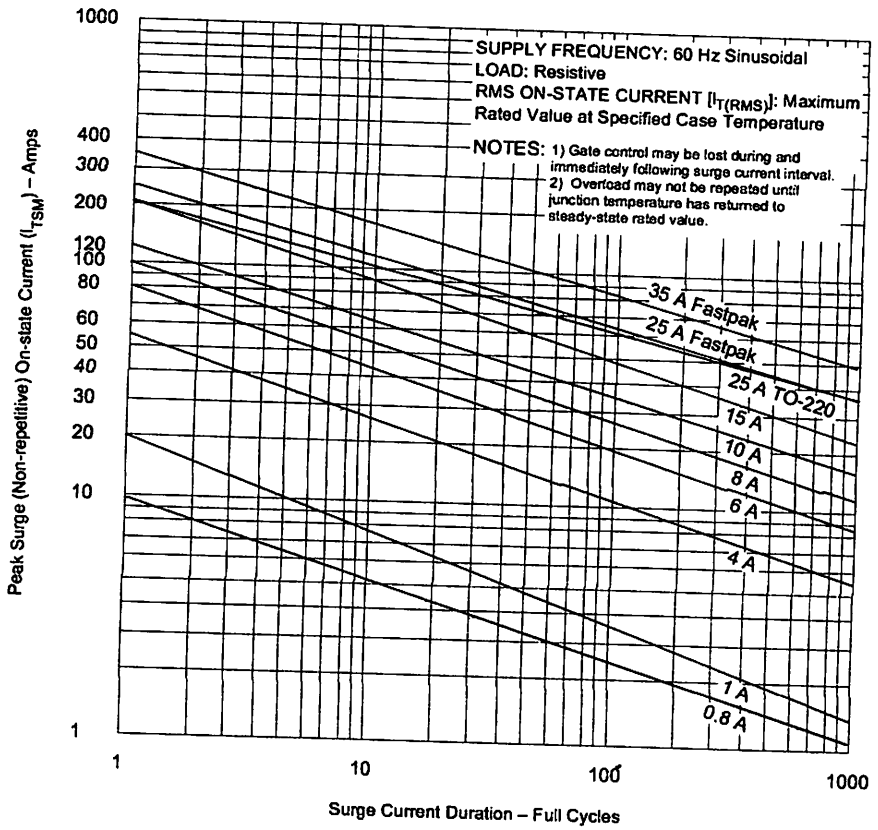
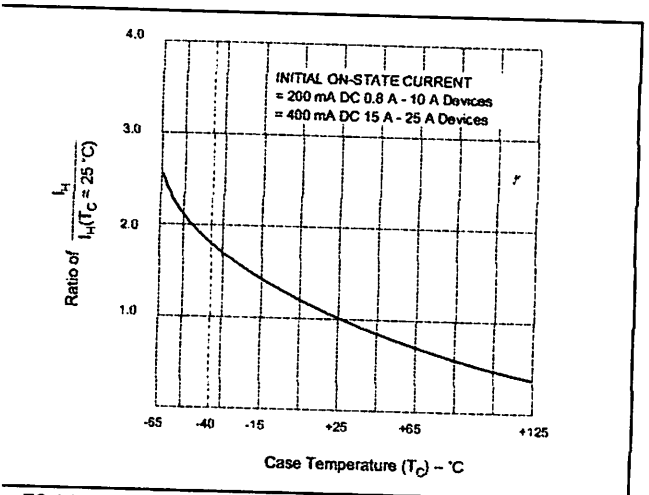


Figure E2.12 Normalized DC Gate Trigger Voltage for All Quadrants versus Case Temperature

©2003 Teccor Electronics
Thyristor Product Catalog



ure E2.13 Peak Surge Current versus Surge Current Duration



e E2.14 Normalized DC Holding Current versus Case Temperature

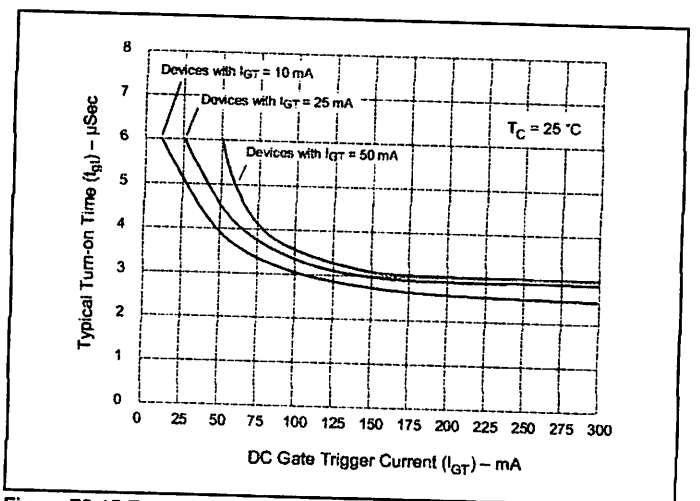
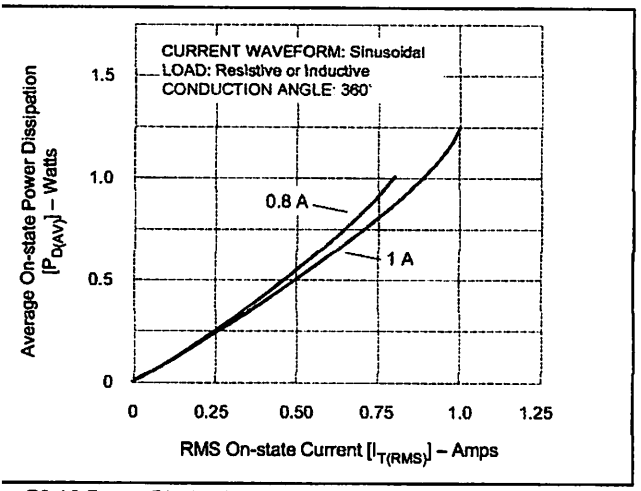


Figure E2.15 Turn-on Time versus Gate Trigger Current (Typical)



re E2.16 Power Dissipation (Typical) versus On-state Current (0.8 A and 1 A)

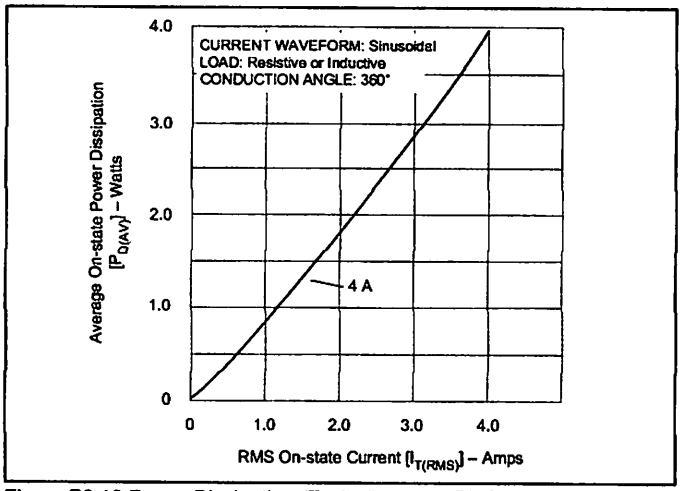
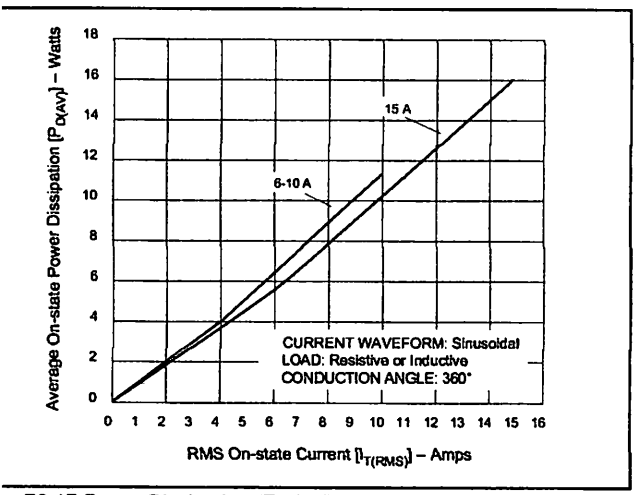
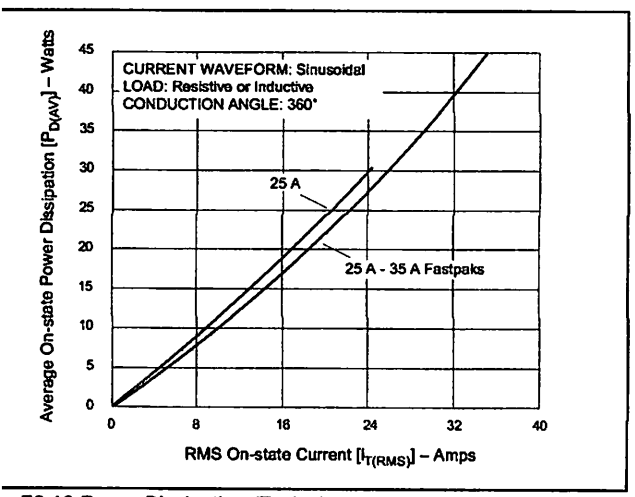


Figure E2.19 Power Dissipation (Typical) versus RMS On-state Current (4 A)



re E2.17 Power Dissipation (Typical) versus On-state Current (6 A to 10 A and 15 A)



e E2.18 Power Dissipation (Typical) versus On-state Current (25 A to 35 A)

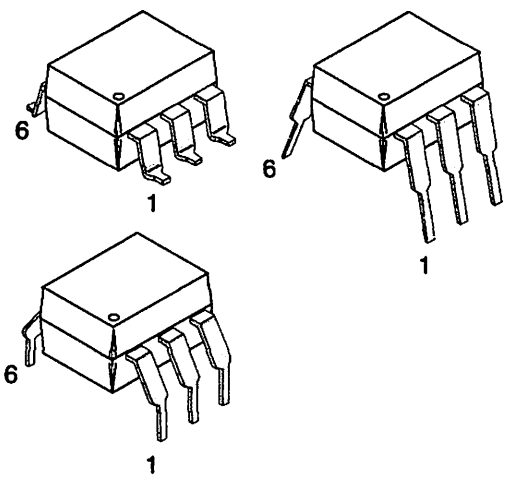
©2003 Teccor Electronics
Thyristor Product Catalog

FAIRCHILD
SEMICONDUCTOR®

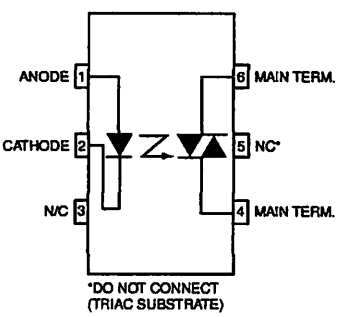
6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

MOC3010M MOC3011M MOC3012M MOC3020M MOC3021M MOC3022M MOC3023M

PACKAGE



SCHEMATIC



DESCRIPTION

The MOC301XM and MOC302XM series are optically isolated triac driver devices. These devices contain a GaAs infrared emitting diode and a light activated silicon bilateral switch, which functions like a triac. They are designed for interfacing between electronic controls and power triacs to control resistive and inductive loads for 115 VAC operations.

FEATURES

Excellent I_{FT} stability—IR emitting diode has low degradation
High isolation voltage—minimum 5300 VAC RMS
Underwriters Laboratory (UL) recognized—File #E90700
Peak blocking voltage
– 250V-MOC301XM
– 400V-MOC302XM
VDE recognized (File #94766)
– Ordering option V (e.g. MOC3023VM)

APPLICATIONS

Industrial controls
Traffic lights
Vending machines
Solid state relay
Lamp ballasts

- Solenoid/valve controls
- Static AC power switch
- Incandescent lamp dimmers
- Motor control

© 2003 Fairchild Semiconductor Corporation

6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameters	Symbol	Device	Value	Units
TOTAL DEVICE				
Storage Temperature	T_{STG}	All	-40 to +150	°C
Operating Temperature	T_{OPR}	All	-40 to +85	°C
Lead Solder Temperature	T_{SOL}	All	260 for 10 sec	°C
Junction Temperature Range	T_J	All	-40 to +100	°C
Isolation Surge Voltage[1] (peak AC voltage, 60Hz, 1 sec duration)	V_{ISO}	All	7500	Vac(pk)
Total Device Power Dissipation @ 25°C	P_D	All	330	mW
Derate above 25°C			4.4	mW/°C
EMITTER				
Continuous Forward Current	I_F	All	60	mA
Reverse Voltage	V_R	All	3	V
Total Power Dissipation 25°C Ambient	P_D	All	100	mW
Derate above 25°C			1.33	mW/°C
DETECTOR				
Off-State Output Terminal Voltage	V_{DRM}	MOC3010M/1M/2M MOC3020M/1M/2M/3M	250 400	V
Peak Repetitive Surge Current (PW = 1 ms, 120 pps)	I_{TSM}	All	1	V
Total Power Dissipation @ 25°C Ambient	P_D	All	300	mW
Derate above 25°C			4	mW/°C

Note

1. Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

© 2003 Fairchild Semiconductor Corporation

6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless otherwise specified)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameters	Test Conditions	Symbol	Device	Min	Typ	Max	Units
EMITTER							
Input Forward Voltage	I_F = 10 mA	V_F	All		1.15	1.5	V
Reverse Leakage Current	V_R = 3 V, T_A = 25°C	I_R	All		0.01	100	μA
DETECTOR							
Peak Blocking Current,Either Direction	Rated V_{DRM}, I_F = 0 (note 1)	I_{DRM}	All		10	100	nA
Peak On-State Voltage,Either Direction	I_{TM} = 100 mA peak, I_F = 0	V_{TM}	All		1.8	3	V

TRANSFER CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

DC Characteristics	Test Conditions	Symbol	Device	Min	Typ	Max	Units
LED Trigger Current	Voltage = 3V (note 3)	I_{FT}	MOC3020M			30	mA
			MOC3010M			15	
			MOC3021M				
			MOC3011M			10	
			MOC3022M				
			MOC3012M			5	
			MOC3023M				
Holding Current, Either Direction		I_H	All		100		μA

Note

1. *Test voltage must be applied within dv/dt rating.*
2. This is static dv/dt. See Figure 5 for test circuit. Commutating dv/dt is a function of the load-driving thyristor(s) only.
3. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (30 mA for MOC3020M, 15 mA for MOC3010M and MOC3021M, 10 mA for MOC3011M and MOC3022M, 5 mA for MOC3012M and MOC3023M) and absolute max I_F (60 mA).

© 2003 Fairchild Semiconductor Corporation

6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

Fig. 1 LED Forward Voltage vs. Forward Current

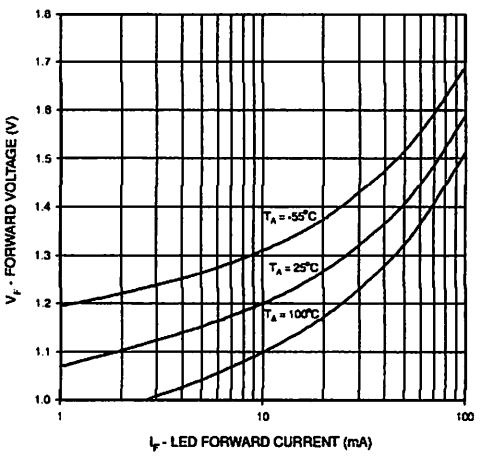


Fig. 2 On-State Characteristics

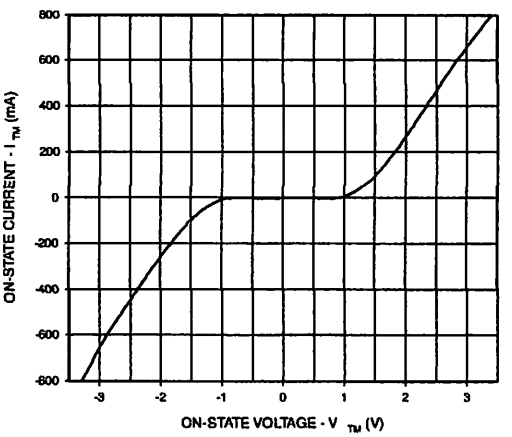


Fig. 3 Trigger Current vs. Ambient Temperature

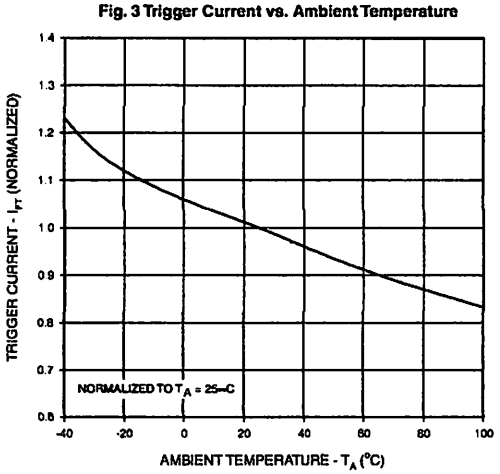


Fig. 4 LED Current Required to Trigger vs. LED Pulse Width

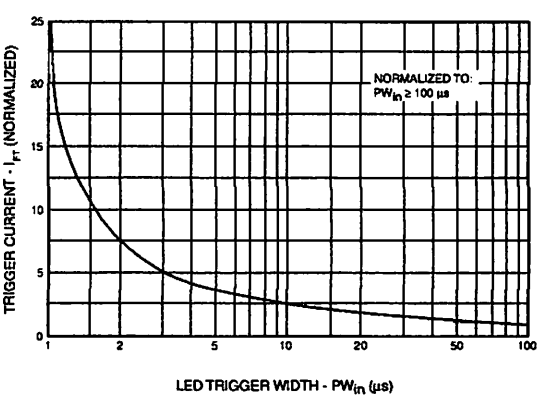


Fig. 5 dv/dt vs. Temperature

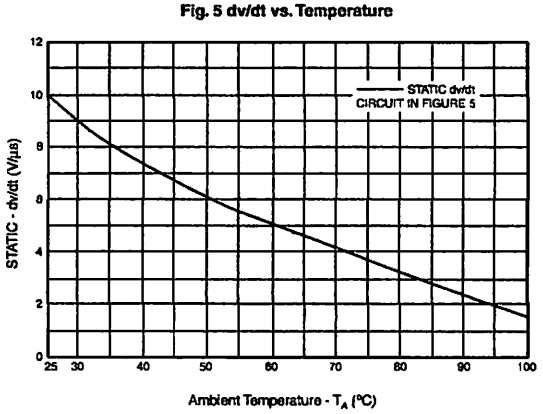
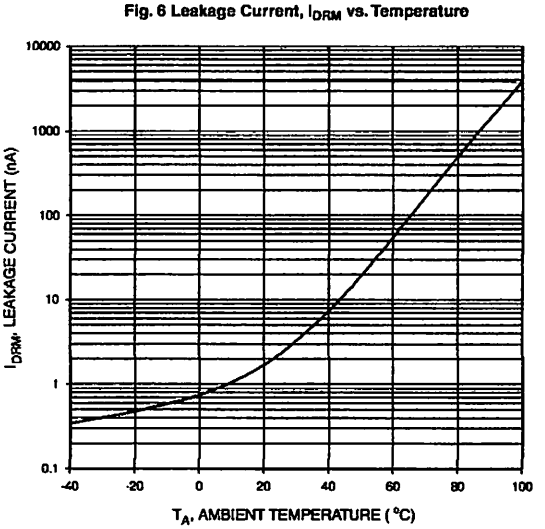
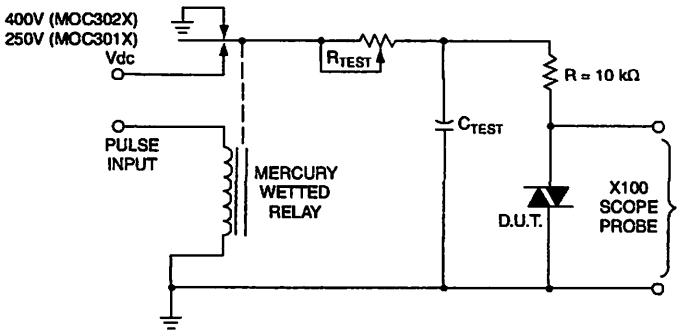


Fig. 6 Leakage Current, I_{DRM} vs. Temperature



© 2003 Fairchild Semiconductor Corporation



1. The mercury wetted relay provides a high speed repeated pulse to the D.U.T.
2. 100x scope probes are used, to allow high speeds and voltages.
3. The worst-case condition for static dv/dt is established by triggering the D.U.T. with a normal LED input current, then removing the current. The variable R_{TEST} allows the dv/dt to be gradually increased until the D.U.T. continues to trigger in response to the applied voltage pulse, even after the LED current has been removed. The dv/dt is then decreased until the D.U.T. stops triggering. τ_{RC} is measured at this point and recorded.

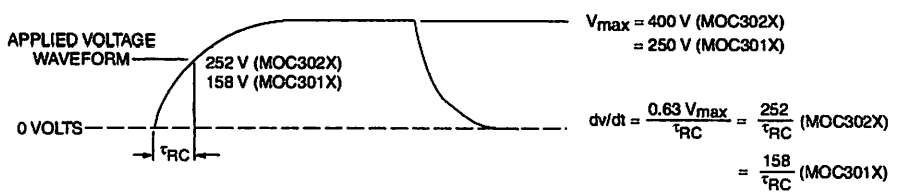


Figure 5. Static dv/dt Test Circuit

Note: This optoisolator should not be used to drive a load directly. It is intended to be a trigger device only.

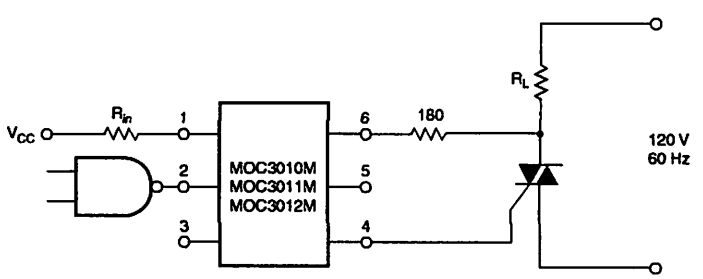


Figure 6. Resistive Load

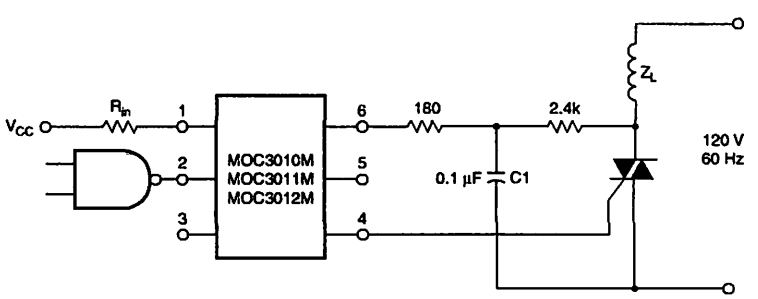


Figure 7. Inductive Load with Sensitive Gate Triac ($I_{GT} \leq 15$ mA)

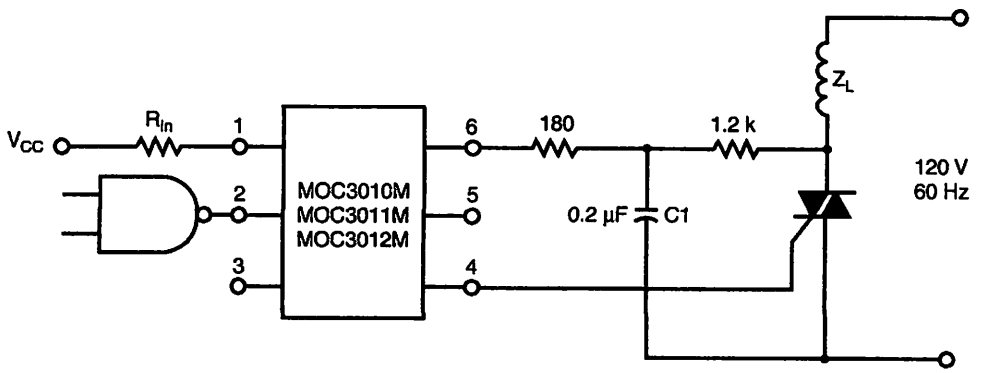
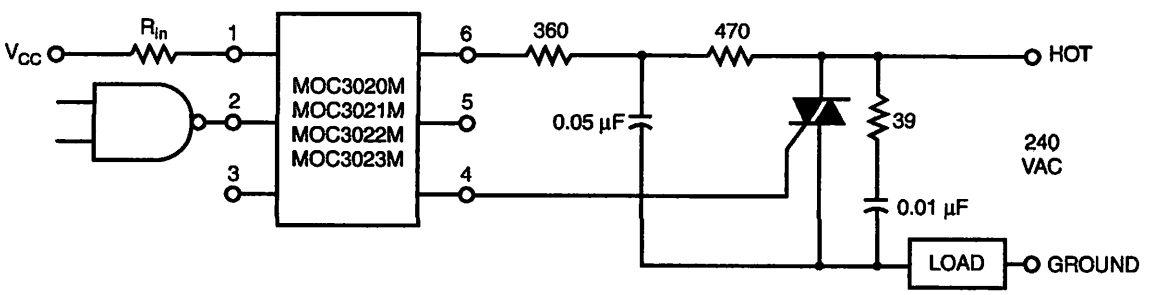


Figure 8. Inductive Load with Sensitive Gate Triac ($I_{GT} \leq 15$ mA)



In this circuit the "hot" side of the line is switched and the load connected to the cold or ground side.

The 39 ohm resistor and 0.01µF capacitor are for snubbing of the triac, and the 470 ohm resistor and 0.05 µF capacitor are for snubbing the coupler. These components may or may not be necessary depending upon the particular and load used.

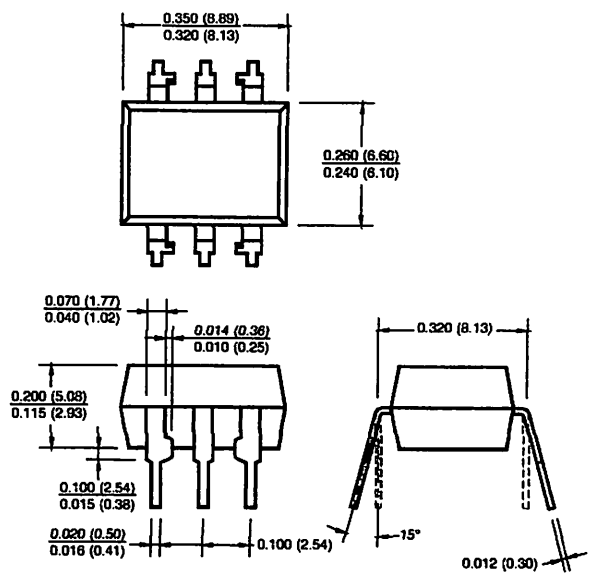
Figure 9. Typical Application Circuit

FAIRCHILD
SEMICONDUCTOR®

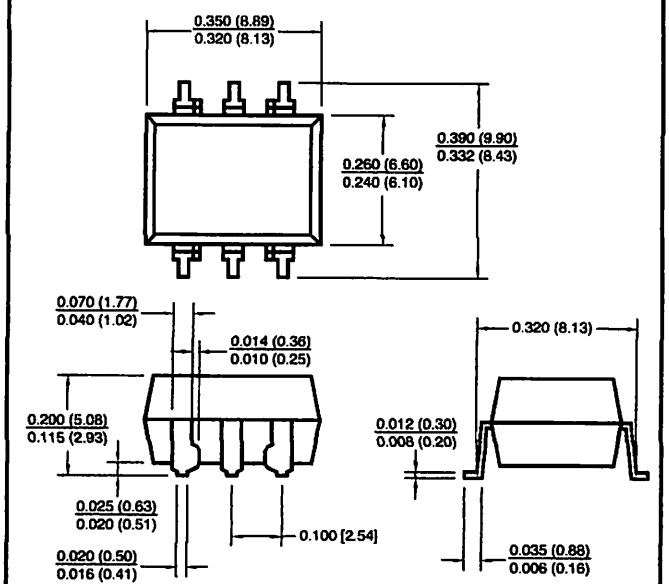
6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

MOC3010M MOC3011M MOC3012M MOC3020M MOC3021M MOC3022M MOC3023M

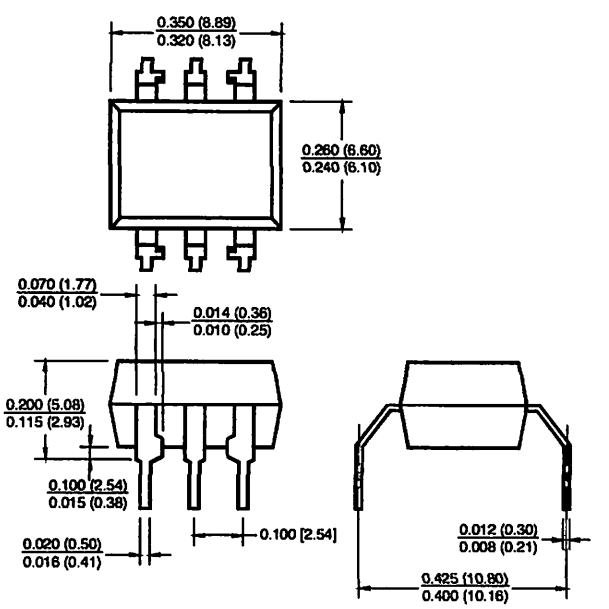
Package Dimensions (Through Hole)



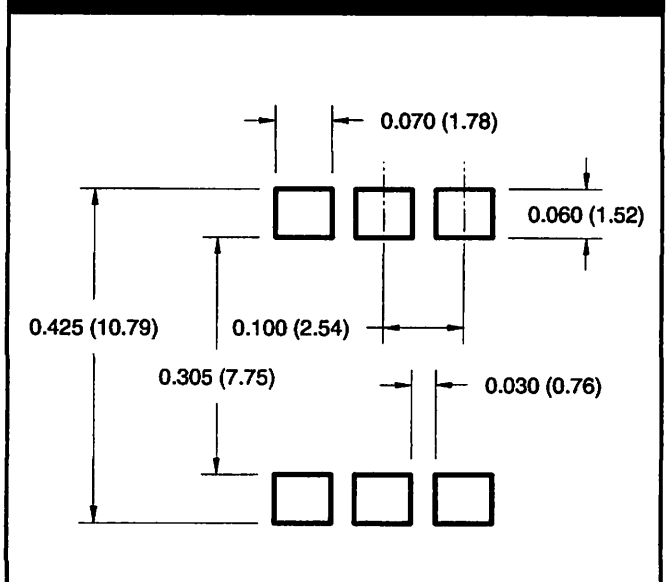
Package Dimensions (Surface Mount)



Package Dimensions (0.4" Lead Spacing)



Recommended Pad Layout for Surface Mount Leadform



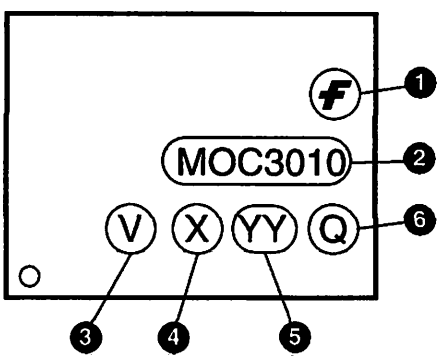
NOTE
All dimensions are in inches (millimeters)

6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

ORDERING INFORMATION

Option	Order Entry Identifier	Description
S	S	Surface Mount Lead Bend
SR2	SR2	Surface Mount; Tape and reel
T	T	0.4" Lead Spacing
V	V	VDE 0884
TV	TV	VDE 0884, 0.4" Lead Spacing
SV	SV	VDE 0884, Surface Mount
SR2V	SR2V	VDE 0884, Surface Mount, Tape & Reel

MARKING INFORMATION

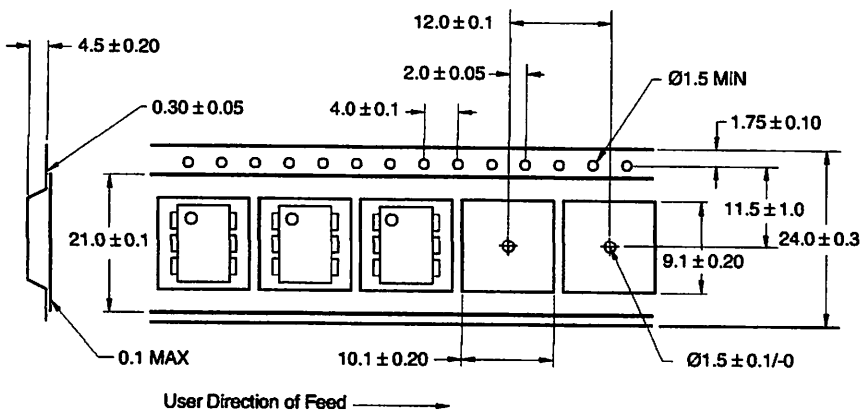


Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., '3'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

*Note – Parts that do not have the 'V' option (see definition 3 above) that are marked with date code '325' or earlier are marked in portrait format.

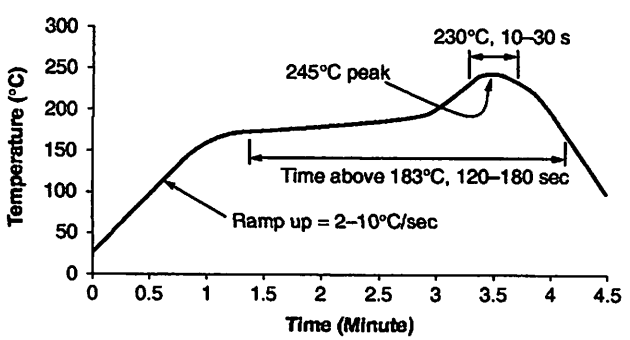
© 2003 Fairchild Semiconductor Corporation

Carrier Tape Specifications



NOTE
All dimensions are in inches (millimeters)

Reflow Profile (White Package, -M Suffix)



- Peak reflow temperature: 245°C (package surface temperature)
- Time of temperature higher than 183°C for 120–180 seconds
- One time soldering reflow is recommended

FAIRCHILD
SEMICONDUCTOR®

6-PIN DIP RANDOM-PHASE OPTOISOLATORS TRIAC DRIVER OUTPUT (250/400 VOLT PEAK)

MOC3010M MOC3011M MOC3012M MOC3020M MOC3021M MOC3022M MOC3023M

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

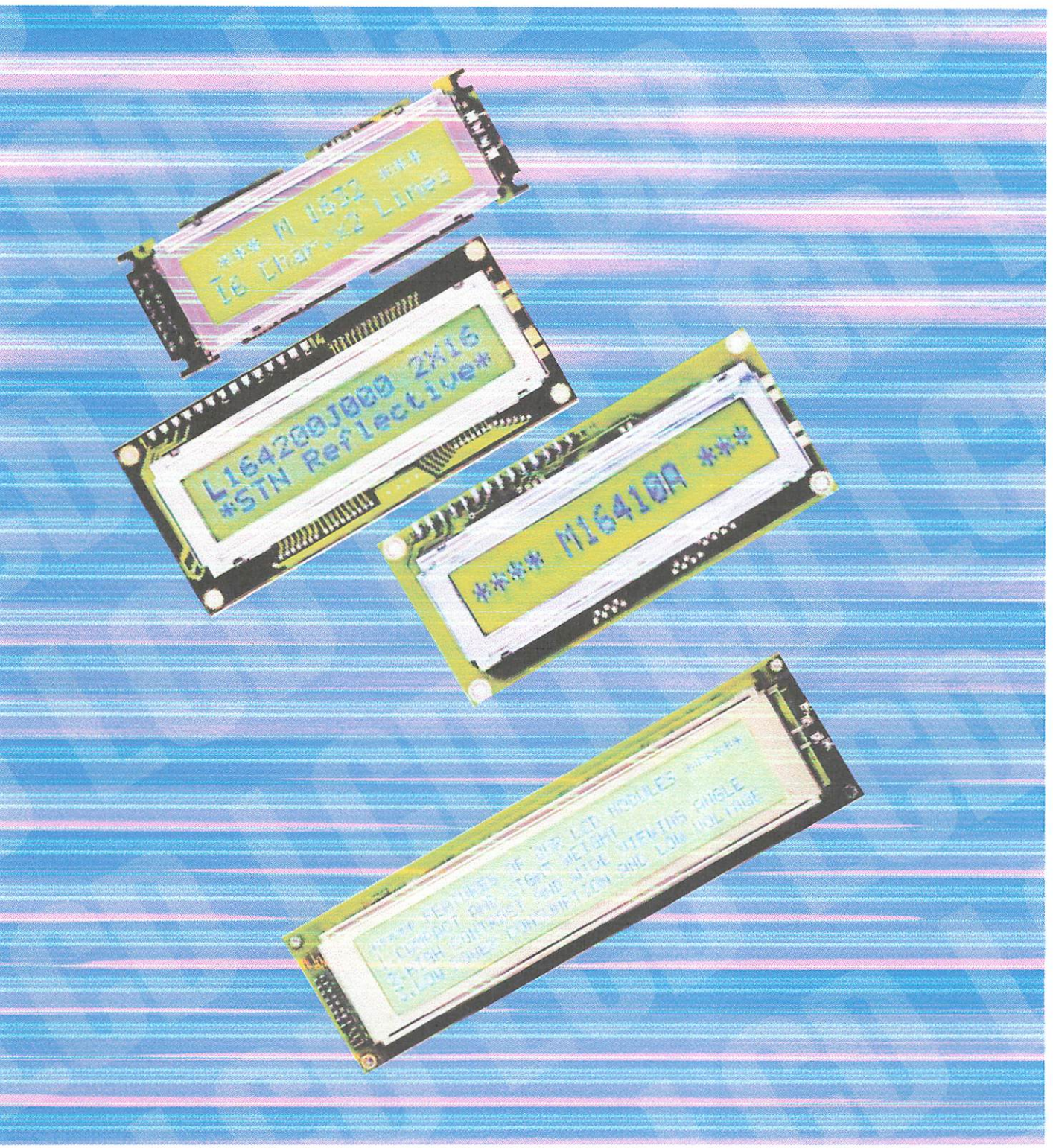
1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

© 2003 Fairchild Semiconductor Corporation

LCM

Liquid Crystal Display Modules

Seiko Instruments GmbH

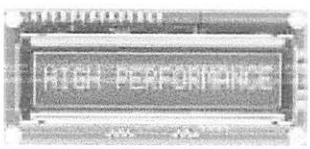


Dot Matrix Liquid Crystal Display Modules

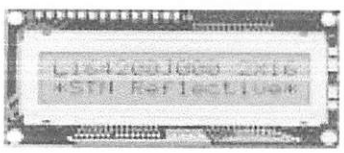
CHARACTER TYPE

• FEATURES :

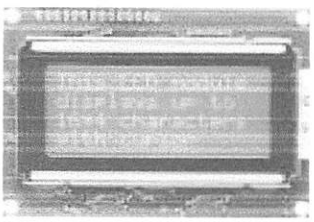
- Slim, light weight and low power consumption
- High contrast and wide viewing angle
- Built-in controller for easy interfacing
- LCD modules with built-in EL or LED backlight



M1641



L1642



L1614

M1632

L1652

L2012

• SPECIFICATIONS :

: Standard products : Products of optional specification

Character Format (character x line)			16 x 1	16 x 2	16 x 2	16 x 2	16 x 4	20 x 2
Model			M1641	M1632	L1642	L1652	L1614	L2012
Reflective			M16410AS	M16320AS	L164200J000S	L165200J200S	L161400J000S	L201200J000S
EL backlight			M16419DWS	M16329DWS	L164221J000S	L165221J200S	L161421J000S	L201221J000S
LED backlight			M16417DYS	M16327DYS	L1642B1J000S	L1652B1J200S	L1614B1J000S	L2012B1J000S
Reflective (wide temp)			M16410CS	M16320CS	L164200L000S	L165200L200S	L161400L000S	L201200L000S
LED backlight (wide temp)			M16417JYS	M16327JYS	L1642B1L000S	L1652B1L200S	L1614B1L000S	L2012B1L000S
Character font			5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor
Module size (HxVxT) mm		Reflective	80,0 x 36,0 x 11,3	85,0 x 30,0 x 10,1	80,0 x 36,0 x 11,3	122,0 x 44,0 x 11,3	87,0 x 60,0 x 11,6	116,0 x 37,0 x 11,3
		EL backlight	80,0 x 36,0 x 11,3	85,0 x 30,0 x 10,1	80,0 x 36,0 x 11,3	122,0 x 44,0 x 11,3	87,0 x 60,0 x 11,6	116,0 x 37,0 x 11,3
		LED backlight	80,0 x 36,0 x 15,8	80,0 x 30,0 x 15,8	80,0 x 36,0 x 15,8	122,0 x 44,0 x 15,8	87,0 x 60,0 x 15,8	116,0 x 37,0 x 15,8
Viewing area (HxV) mm			64,5 x 13,8	62,0 x 16,0	64,5 x 13,8	99,0 x 24,0	61,8 x 25,2	83,0 x 18,6
Character size (HxV) mm *1			3,07 x 5,73	2,78 x 4,27	2,95 x 3,80	4,84 x 8,06	2,95 x 4,15	3,20 x 4,85
Dot size (HxV) mm			0,55 x 0,75	0,50 x 0,55	0,50 x 0,55	0,92 x 1,10	0,55 x 0,55	0,60 x 0,65
Power supply voltage (VDD-VSS) V			+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V
Current consumption (mA,typ)		IDD	1,5	2,0	1,6	2,0	2,7	2,0
		ILC *4	0,2	0,2	0,3	0,4	1,1	0,4
Driving method (duty)			1/16	1/16	1/16	1/16	1/16	1/16
Built-in LSI			KS0066 or equivalent	KS0066 MSM5839 or equivalent	KS0066 MSM5839 or equivalent	KS0066 MSM5839 or equivalent	KS0066 KS0063 or equivalent	KS0066 KS0063 or equivalent
Operating temperature (°C)		normal temp.	0 to + 50	0 to + 50	0 to + 50	0 to + 50	0 to + 50	0 to + 50
		wide temp. *2	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70
Storage temperature (°C)		normal temp.	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60
		wide temp.	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80
Weight (g, typ.)	Reflective		25	25	25	50	50	40
	EL backlight		30	30	30	55	55	45
	LED backlight		35	40	35	65	65	60
Inverters for EL	Model		5S	5S	5S	5C	5A	5A
	Power supply (V)		+ 5.0	+ 5.0	+ 5.0	+ 5.0	+ 5.0	+ 5.0
	current consumption (mA) *3		10	10	10	35	45	45
LED backlight	Forward current consumption (mA)		100	112	100	240	200	154
	Forward input voltage (V,typ.)		+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1

*1 : Excluding cursor

H : Horizontal V : Vertical T : Thickness (max)

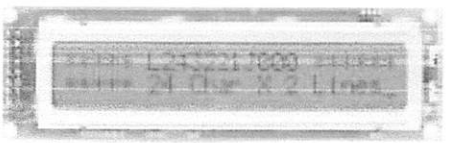
*2 : With external temperature compensation

*3 : Including EL backlight

*4 : Based on normal temperature range

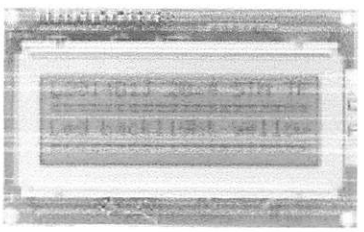
Since our policy is one of continues improvements we reserve the right to change the specifications for the products in the catalogue without notice.

L2022

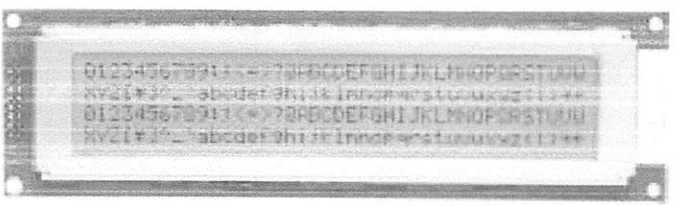


L2432

L4042



L2014



M4024

• SPECIFICATIONS :

: Standard products : Products of optional specification

Character Format (character x line)		20 x 2	20 x 4	24 x 2	40 x 2	40 x 4
Model		L2022	L2014	L2432	L4042	M4024
Reflective		-	L201400J000S	L243200J000S	L404200J000S	M40240AS
EL backlight		-	L201421J000S	L243221J000S	L404221J000S	M40249DWS
LED backlight		-	L2014B1J000S	L2432B1J000S	L4042B1J000S	M40247DYS
Reflective (wide temp)		L202200P000S	L201400L000S	L243200L000S	L404200L000S	M40240CS
LED backlight (wide temp)		L2022B1P000S	L2014B1L000S	L2432B1L000S	L4042B1L000S	M40247JYS
Character font		5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor	5x7 dots + cursor
Module size (HxVxT) mm	Reflective	180,0 x 40,0 x 10,5	98,0 x 60,0 x 11,6	118,0 x 36,0 x 11,3	182,0 x 33,5 x 11,3	190,0 x 54,0 x 10,1
	EL backlight	180,0 x 40,0 x 10,5	98,0 x 60,0 x 11,6	118,0 x 36,0 x 11,3	182,0 x 33,5 x 11,3	190,0 x 54,0 x 10,1
	LED backlight	180,0 x 40,0 x 14,8	98,0 x 60,0 x 15,8	118,0 x 36,0 x 15,8	182,0 x 33,5 x 16,3	190,0 x 54,0 x 16,3
Viewing area (HxV) mm		149,0 x 23,0	76,0 x 25,2	94,5 x 17,8	154,4 x 15,8	147,0 x 29,5
Character size (HxV) mm *1		6,00 x 9,66	2,95 x 4,15	3,20 x 4,85	3,20 x 4,85	2,78 x 4,27
Dot size (HxV) mm		1,12 x 1,12	0,55 x 0,55	0,60 x 0,65	0,60 x 0,65	0,50 x 0,55
Power supply voltage (VDD-VSS) V		+ 5 V	+ 5 V	+ 5 V	+ 5 V	+ 5 V
Current consumption (mA,typ)	IDD	4,2	2,9	2,5	3,0	8,0
	ILC *4	2,6	1,2	0,5	1,0	3,0
Driving method (duty)		1/16	1/16	1/16	1/16	1/16
Built-in LSI		KS0066 KS0063 or equivalent	KS0066 MSM5839 or equivalent	KS0066 KS0063 or equivalent	KS0066 KS0063 or equivalent	KS0066 MSM5839 or equivalent
Operating temperature (°C)	normal temp.	-	0 to + 50	0 to + 50	0 to + 50	0 to + 50
	wide temp. *2	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70	- 20 to + 70
Storage temperature (°C)	normal temp.	-	- 20 to + 60	- 20 to + 60	- 20 to + 60	- 20 to + 60
	wide temp.	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80	- 30 to + 80
Weight (g, typ.)	Reflective	80	55	40	70	90
	EL backlight	-	60	45	75	105
	LED backlight	110	70	60	95	140
Inverters for EL	Model	-	5A	5A	5C	5D
	Power supply (V)	+ 5.0	+ 5.0	+ 5.0	+ 5.0	+ 5.0
	current consumption (mA) *3	-	45	45	25	80
LED backlight	Forward current consumption (mA)	320	240	150	260	480
	Forward input voltage (V,typ.)	+ 4,1	+ 4,1	+ 4,1	+ 4,1	+ 4,1

*1 : Excluding cursor H : Horizontal V : Vertical T : Thickness (max)

*2 : With external temperature compensation

*3 : Including EL backlight

*4 : Based on normal temperature range

Dot Matrix Liquid Crystal Display Modules

GRAPHIC TYPE

- **FEATURES :**
  - •Wide viewing angle and high contrast
  - •Full dot configuration fits any application
  - •Slim, light weight and low power consumption
  - •Available in STN and FSTN

- **SPECIFICATIONS :**

Dot format (HxV,dot)			97 x 32	128 x 32	128 x 64	128 x 64
Model			Y97031	G1213	G1216	G1226
STN type (Gray mode)	Reflective	built-in RAM	-	-	-	-
	Reflective wide temp.	built-in RAM	-	G121300N000S	G121600N000S	-
	LED backlight	built-in RAM	-	-	-	G1226B1J000S
	LED backlight wide temp	built-in RAM	-	G1213B1N000S	G1216B1N000S	-
FSTN type (B&W mode)	Transmissive	-	-	-	-	-
	with CFL backlight	built-in controller	-	-	-	-
	Transflective	built-in RAM	Y97031LF60W	-	-	-
Module size (H x V x T) mm	Reflective (no backlight)		47,5 x 65,4 x 2,1	75,0 x 41,5 x 6,8	75,0 x 52,7 x 6,8	-
	LED backlight		-	75,0 x 41,5 x 8,9	75,0 x 52,7 x 8,9	93,0 x 70,0 x 11,4
	CFL backlight		-	-	-	-
Viewing area (HxV) mm			43,5 x 23,9	60,0 x 21,3	60,0 x 32,5	70,7 x 38,8
Dot size (H x V) mm			0,35 x 0,48	0,40 x 0,48	0,40 x 0,40	0,44 x 0,44
Dot pitch (H x V) mm			0,39 x 0,52	0,43 x 0,51	0,43 x 0,43	0,48 x 0,48
Power supply voltage (V)		(VDD - VSS)	+5,0	+5,0	+5,0	+5,0
		(VLC - VSS)	-	- 8,0	- 8,1	-8,2
Current consumption (mA, typ.)		IDD	0,10	2,0	2,0	3,0
		IDD (built-in controller)	-	-	-	-
		ILC	-	1,8	1,8	2,0
Driving method (duty)			1/33	1/64	1/64	1/64
Built-in LSI		Driver	SED1530 or equivalent	HD61202 HD61203 or equivalent	HD61202 HD61203 or equivalent	KS0107 KS0108 or equivalent
		Controller	-	-	-	-
Operating temperature range (°C)			- 20 to + 70	- 20 to + 70	- 20 to + 70	0 to + 50
Storage temperature range (°C)			- 30 to + 80	- 30 to + 80	- 30 to + 80	- 20 to + 60
Weight (g, typ.)	Reflective (Transflective no backlight)		10	23	35	-
	LED backlight		-	35	45	72
	CFL backlight		-	-	-	-
LED backlight	Forward current consumption (mA)		-	40	90	125
	Forward input voltage (V, typ.)		-	3,8	4,1	4,1
Inverter for CFL	Mode		-	-	-	-
	Power supply voltage (V)		-	-	-	-
	Current consumption (mA, typ.)		-	-	-	-

*1 : built-in DC/DC converter (single power source)

*2 : Use with external temperature compensation circuit

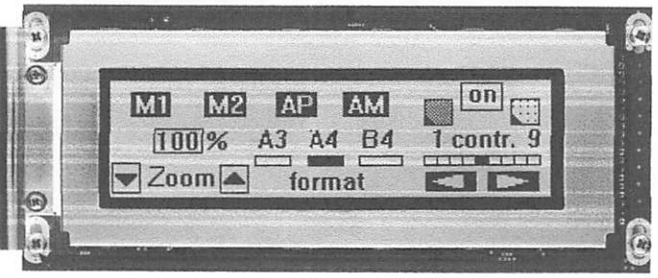
Since our policy is one of continues improvements we reserve the right to change the specifications of the products in the catalogue without notice.

Dot format (HxV,dot)			240 x 64	240 x 128	320 x 200	320 x 240	640 x 200
Model			G2446	G242C	G321D	G324E	G649D
STN type (Gray mode)	Reflective	built-in RAM	-	-	-	-	-
	Reflective wide temp.	built-in RAM	-	-	-	-	-
	LED backlight	built-in RAM	-	-	-	-	-
	LED backlight wide temp	built-in RAM	-	-	-	-	-
FSTN type (B&W mode)	Transmissive	-	G2446X5R1A0S	G242CX5R1ACS	G321DX5R1A0S	G324EX5R1A0S	G649DX5R010S
	with CFL backlight	built-in controller	G2446X5R1ACS	G242CX5R1A0S	G321DX5R1ACS	G324EX5R1ACS	-
	Transflective	built-in RAM	-	-	-	-	-
Module size (H x V x T) mm	Reflective (no backlight)			-	-	-	-
	LED backlight			-	-	-	-
	CFL backlight		191,0 x 79,0 x 15,1	180,0 x 110,0 x 15,1	166,0 x 134,0 x 15,1	166,0 x 134,0 x 15,1	260,0 x 122,0 x 15,7
Viewing area (HxV) mm			134,0 x 41,0	134,0 x 76,0	128,0 x 110,0	128,0 x 110,0	216,0 x 83,0
Dot size (H x V) mm			0,49 x 0,49	0,47 x 0,47	0,34 x 0,48	0,32 x 0,39	0,30 x 0,36
Dot pitch (H x V) mm			0,53 x 0,53	0,51 x 0,51	0,38 x 0,52	0,36 x 0,43	0,33 x 0,39
Power supply voltage (V)		(VDD - VSS)	+5,0	+5,0	+5,0	+5,0	+5,0
		(VLC - VSS)	*1	*1	-24,0	-24,0	-24,0
Current consumption (mA, typ.)		IDD	12	30	8	7,5	11
		IDD (built-in controller)	15	40	23	23	-
		ILC	-	-	6	6,5	9
Driving method (duty)			1/64	1/128	1/200	1/240	1/200
Built-in LSI		Driver	MSM5298 MSM5299 or equivalent	KS0103 KS0104 or equivalent	MSM5298 MSM5299 or equivalent	HD66204 HD66205 or equivalent	MSM5298 MSM5299 or equivalent
		Controller	SED1330FB	SED1330FB	SED1330FB	SED1330FB	-
Operating temperature range (°C)			0 to +50	0 to +50	0 to +50	0 to +50	0 to +50
Storage temperature range (°C)			- 20 to +60	- 20 to +60	- 20 to +60	- 20 to +60	- 20 to +60
Weight (g, typ.)	Reflective (Transflective no backlight)		-	-	-	-	-
	LED backlight		-	-	-	-	-
	CFL backlight		200	280	350	350	420
LED backlight	Forward current consumption (mA)		-	-	-	-	-
	Forward input voltage (V, typ.)		-	-	-	-	-
Inverter for CFL	Mode		4800210	4800210	4800210	4800210	4800120
	Power supply voltage (V)		+5,0	+5,0	+5,0	+5,0	+12,0
	Current consumption (mA, typ.)		250	350	365	365	390

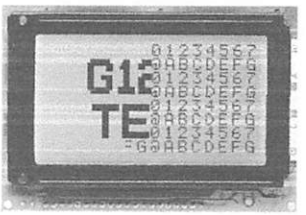
*1 : built-in DC/DC converter (single power source)

*2 : Use with external temperature compensation

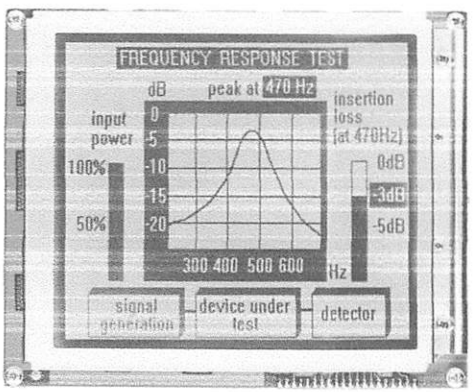
Since our policy is one of continous improvemets, we reserve the right to change the specifications of the products in the catalogue without notice.



G2446

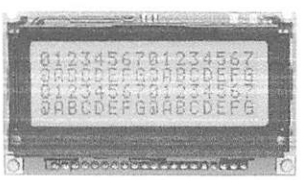


G1226

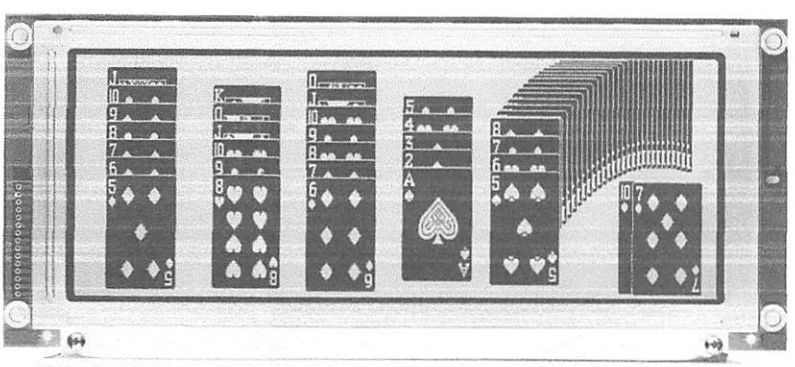


G321D

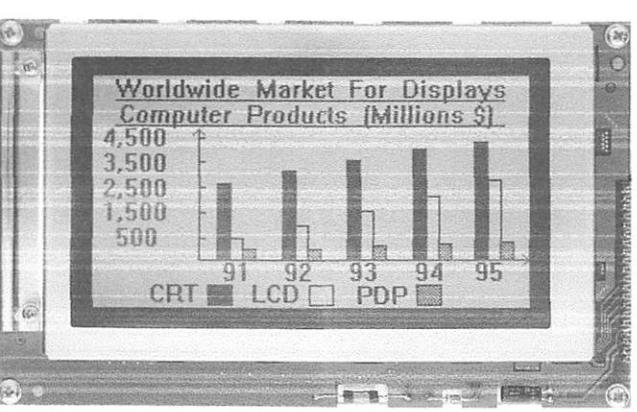
G1216



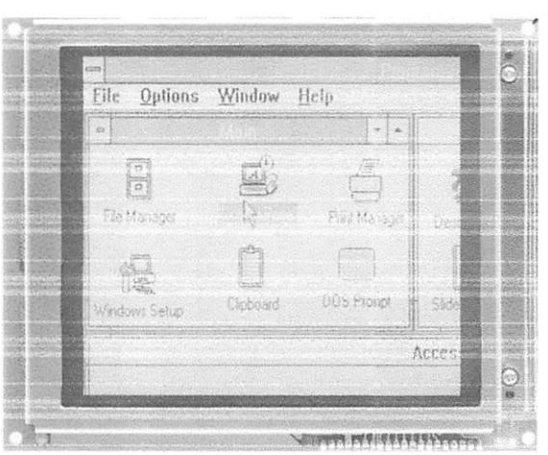
G1213



G649D



G242C



G324E

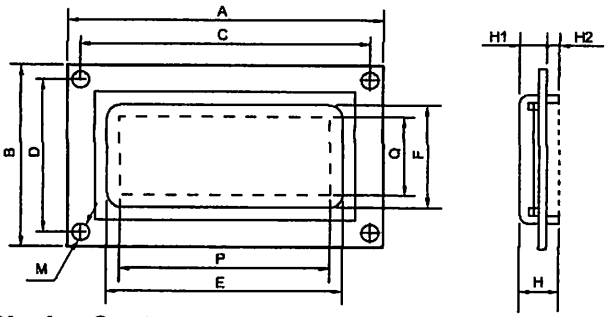
CHECK LIST FOR CUSTOM DESIGNED LCD MODULE

1. Company_____ **2. Application**_____ **3. Customer Specified Part No.**_____

4. Design

☐ New ☐ Modified : Manufacturer_____ , Part No._____ , Remarks _____
☐ Equivalent: Manufacturer_____, Part No._____, Remarks _____

5. LCM Dimensions



A x B : Module size _____ x _____ mm
E x F : Viewing area _____ x _____ mm
P x Q : Active display area _____ x _____ mm
C : Length between mounting holes _____ mm
D : Length between mounting holes _____ mm
M : Diameter of mounting hole _____ mm
H : Total thickness _____ mm
H1 : Upper thickness _____ mm
H2 : Lower thickness _____ mm

6. Display Contents

☐ Character type:_____characters_____lines
Character font_____x_____dots + cursor
Character pitch_____x_____mm
Dot pitch_____x_____mm
Dot size_____x_____mm
☐ Graphics (Full dot) type:_____x_____dots
Dot pitch_____x_____mm
Dot size_____x_____mm
☐ Segment type:_____digits_____lines
☐ Others_____

7. LCD Panel

Viewing angle: ☐6 o'clock ☐12 o'clock ☐____o'clock
Type: ☐ TN ☐ FSTN (Black and white)
☐ STN (☐ Yellow green ☐ Gray ☐ Blue)
Chromaticity coordinates
(_____ ≦ x ≦ _____ , _____ ≦ y ≦ _____)
☐ Positive type ☐ Negative type
☐ Reflective ☐ Transflective ☐ Transmissive
☐ Others_____
Gray scale: ☐ Yes_____ gray scale ☐ No
Preferential specifications:
☐ Response time t_{on} ____ ms (___ °C) t_{off} ____ ms (___ °C)
☐ Viewing angle____ deg. (___ °C) ☐ Contrast____ (___ °C)
☐ Others_____
LCD *surface finishing*:
☐ Normal ☐ Anti-glare ☐_____
Polarizer color: ☐ Normal (neutral gray) ☐ Red
☐ Green ☐ Blue ☐_____

8. Driving Method

Multiplexing:1/_____ duty, 1/_____ bias
Frame frequency: _____ Hz

9. IC

LCD driver: ☐ Specified ☐ Unspecified
Segment driver _____ (Manufacturer _____)
Common driver _____ (Manufacturer _____)
Controller: ☐ Internal ☐ External
Type No._____ (Manufacturer _____)
MPU: ☐ Internal ☐ External
Type No._____ (Manufacturer _____)
RAM: ☐ Internal ☐ External
Type No. /Memory size_____ (Kbit) (Manufacturer _____)

10. Power Supply

☐ Single power supply: ☐ 5V ☐_____V
☐ 2 power supplies
For logic: (V_{DD}-V_{SS}) : ☐ 5V ☐_____V
For LC drive: (V_{LC}-V_{SS}) : ☐_____V

11. Temperature Compensation Circuit

☐ Internal ☐ External ☐ Unnecessary
Compensation range: ☐ 0°C to 50°C ☐ ___°C to ___°C

12. Current Consumption

For logic: typ._____mA, max._____mA
For LC drive: typ._____mA, max._____mA
Others ( ) : typ._____mA, max._____mA

13. Contrast Adjustment

☐ Internal ☐ External ☐ Unnecessary
Method: ☐ Temp. compensation circuit ☐ Volume ☐____

14. Temperature Range

Operating temperature range: ☐ 0°C to 50°C ☐____°C to ___°C
Storage temperature range: ☐ - 20°C to 60°C ☐____°C to ___°C

15. Input/Output Terminals

Specifying allocation: ☐ Yes ☐ No
Specifying position: ☐ Yes ☐ No

16. Weight

typ.____ g, max.____ g

17. Connector

☐ Internal ☐ External ☐ Unnecessary
Type No._____ (Manufacturer _____)

18. Backlight

☐ Internal ☐ External ☐ Unnecessary
☐ EL: ☐ Green ☐ White ☐_____
☐ LED: ☐ Yellow green ☐ Amber ☐_____
☐ CFL: ☐ White ☐_____
☐ Incandescent lamp ☐ Others_____
☐ Backlight type ☐ Edge backlight type
Brightness:_____cd/m²
Inverter: ☐ Internal ☐ External ☐ Unnecessary
Power supply voltage_____V
Current consumption (backlight included)_____ mA
Brightness control: ☐ Yes ☐ No

19. Others

_____
_____
_____

20. Schedule

Estimate: _____
Sample: Delivery_____, Quantity:_____pcs
Mass production: Target price: _____
Delivery _____, Total quantity:_____pcs
Quantity per month_____pcs

CHECK LIST FOR CUSTOM DESIGNED LCD

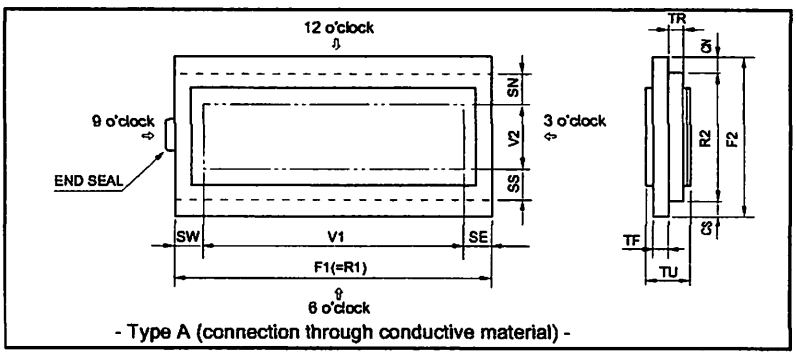
1. Company_____ **2. Application**_____ **3. Customer Specified Part No.**_____

4. Design

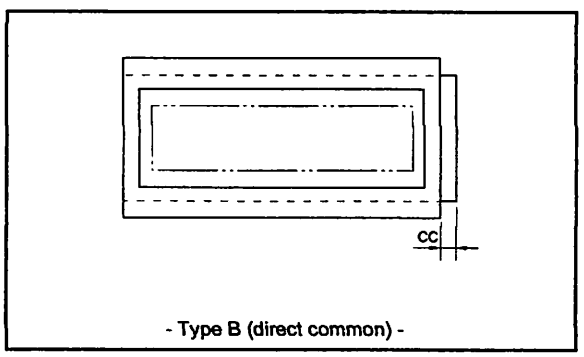
☐New ☐Modified: Manufacturer _____ , Part No._____ , Remarks_____

☐Equivalent: Manufacturer_____ , Part No._____ , Remarks_____

5. Panel Dimensions



- Type A (connection through conductive material) -



- Type B (direct common) -

F1: Horizontal length of upper glass _____mm

F2: Vertical length of upper glass_____mm

R1: Horizontal length of lower glass_____ the same as F1

R2*: Vertical length of lower glass_____mm

*R2 is generally longer than F2 when terminals are with pin.

TF, TR***: Thickness of glass_____mm

***Standard type: 1.1 mm or 0.7 mm

TU: Thickness of LCD_____mm

End seal:☐Right ☐Left ☐Right or Left

V1 :Horizontal length of viewing area _____mm

V2 :Vertical length of viewing area _____mm

CN**: Terminal length_____mm

CS**:Terminal length_____mm

**CN or CS=0 in case of one side terminal type.

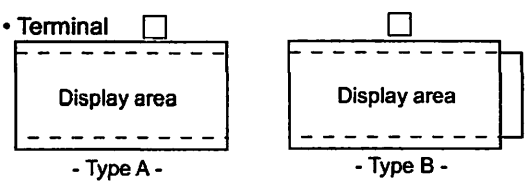
CC: Terminal length_____mm

SE,SW,SN,SS : Seal width

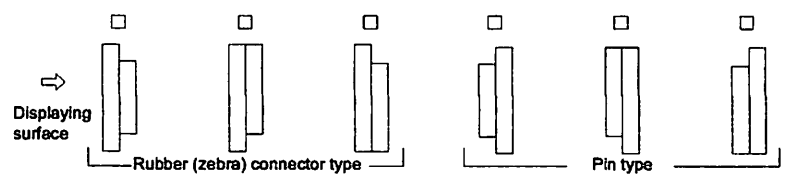
(According to design or manufacturing condition:
about 2.0 mm to 4.0 mm)

6. Panel Form

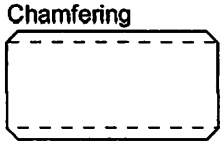
• Terminal ☐



- Type A - - Type B -

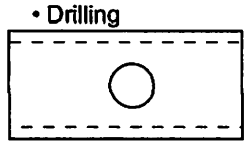


• Chamfering



☐ Yes ☐ No

• Drilling



☐ Yes ☐ No

7. Display Mode

Viewing angle : ☐6 o'clock ☐ 12 o'clock ☐_____o'clock

Type: ☐TN ☐FSTN (Black and white)

☐STN: (☐ Yellow green ☐ Gray ☐ Blue)

Chromaticity coordinates (____≦ x ≦ ____, ____≦ y ≦ ____)

☐Positive type ☐Negative type

☐Reflective ☐Transflective ☐Transmissive

Preferential specifications:

☐Response time t_{on} ____ ms (____ °C) t_{off} ____ ms (____ °C)

☐Viewing angle ____ deg. (____ °C) ☐Contrast ____ (____ °C)

☐Others_____

8. Polarizer

Surface finishing: ☐Normal ☐Anti-glare ☐_____

Color: ☐Normal (neutral gray) ☐Red ☐Green
☐Blue ☐_____

Front polarizer : ☐ Attached type ☐ Separate type

Rear polarizer : ☐Attached type ☐ Separate type

9. Driving Method

☐ Static ☐ Multiplexing: (1/_____duty, 1/_____bias)

Operating voltage (V_{opr}) :_____V

Frame frequency:_____Hz

Driving IC:_____(Manufacturer_____)

Current consumption:_____μA

10. Temperature Range

Operating temperature range

☐With temperature compensation circuit (or volume)
(☐ 0°C to 50°C ☐_____°C to_____°C)

☐Without temperature compensation circuit
(☐ 0°C to 50°C ☐_____°C to_____°C)

Storage temperature range
(☐ - 20°C to 60°C ☐_____°C to_____°C)

11. Terminal Connecting Method

☐Rubber connector (Zebra rubber)

☐Pin: ☐DIL ☐SIL ☐_____

Pitch (☐2.54 ☐_____mm) Length (_____mm)

☐Heat seal: ☐Equipped ☐Unnecessary

12. Others

Print (Characters, lines, masks etc.) : ☐Yes ☐ No

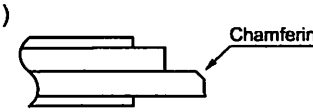
Protective film:

☐Yes (Color: ☐ Red ☐Translucent ☐Transparent) ☐No

Chamfering (for heat-seal connector) :

☐Yes (Position:_____)
(Quantity:_____)

☐No



13. Schedule

Estimate :_____

Sample : Delivery_____ , Quantity :_____pcs

Mass production : Target price :_____

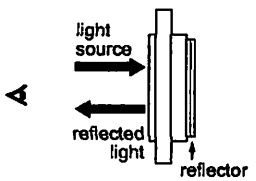
Delivery _____ , Total quantity:_____pcs

Quantity per month:_____pcs

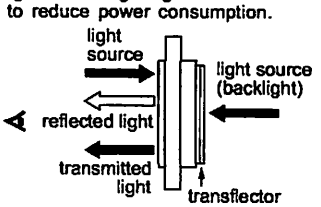
Liquid Crystal Display Modules

REFLECTIVE/TRANSFLECTIVE/TRANSMISSIVE LCD

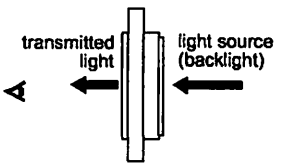
❶ Reflective LCD
Reflector bonded to the rear polarizer reflects the incoming ambient light. Low power consumption because no backlight is required.



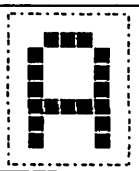
❷ Transflective LCD
Transflector bonded to the rear polarizer reflects light from the front as well as enabling lights to pass through the back. Used with backlight off in bright light and with it on in low light to reduce power consumption.

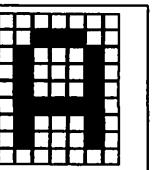


❸ Transmissive LCD
Without reflector or transflector bonded to the rear polarizer. Backlight required. Most common is transmissive negative image.



POSITIVE/NEGATIVE MODE

Positive type	

Negative type		Negative type (inverse image) (when data is inverted)	

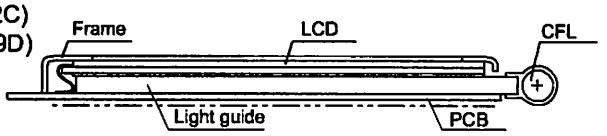
TN TYPE/STN TYPE/FSTN TYPE

TN	(Background/dot color) Gray/Black	TN(Twisted Nematic) type is most conventional and economical. It is used for static drive LCD and low-duty drive LCD (watch,calculator, etc.)
STN	Yellowgreen/Dark blue Gray/Dark blue White/Blue	STN (Super Twisted Nematic) type has a higher twist angle, and thus provides clear visibility and wider viewing angle. This is suitable especially for high-duty drive LCD.
FSTN	White/Black	FSTN (Film Super Twisted Nematic) type utilizes RCF (Retardation Control Film) to remove the coloring of STN LCD. Thus FSTN type provides easy-to-read black-and-white display.

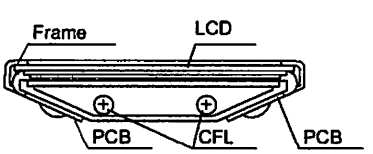
STRUCTURE AND FEATURE OF LCD MODULE WITH BACKLIGHT

CFL (Cold Cathode Fluorescent Lamp) backlight
Features: high brightness, long service life, inverter required

- Edge backlight type
  (G2446,G242C)
  (G321D,G649D)

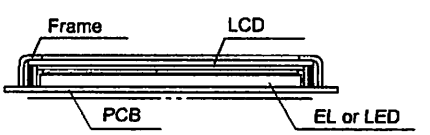


- Backlight type



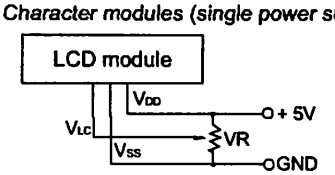
EL (Electroluminescent Lamp) backlight
LED (Light Emitting Diode) backlight

Features: EL: thin, inverter required
LED: long service life, low voltage driving, no inverter required

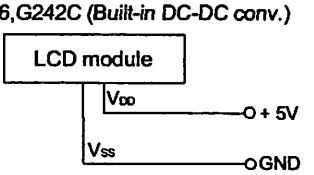


POWER SUPPLY

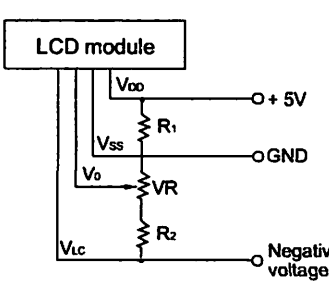
- *Character modules (single power supply)*



- *G2446,G242C (Built-in DC-DC conv.)*

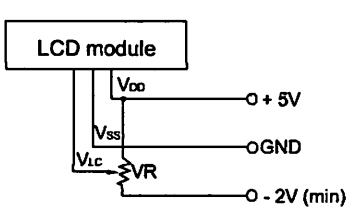


- *G321D, G324E and G649D*

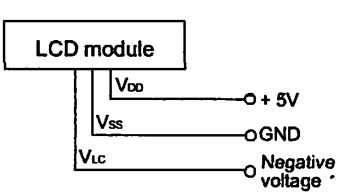


Note 1:Contrast can be adjusted by VR.
Note 2:For module with backlight, power supply for backlight is necessary.

- Character Modules(Dual power supply)



- Y1206 and G1226



·Negative voltage should be variable for contrast adjustment.

Precautions

Safety Instructions

- If the LCD panel is damaged, be careful not to get the liquid crystal in your mouth and not to be injured by crushed glasses.
- If you should swallow the liquid crystal, first, wash your mouth thoroughly with water, then, drink a lot of water and induce vomiting, and then, consult a physician.
- If the liquid crystal should get in your eye, flush your eye with running water for at least fifteen minutes.
- If the liquid crystal touches your skin or clothes, remove it and wash the affected part of your skin or clothes with soap and running water.
- EL or CFL backlight is driven by a high voltage with an inverter. Do not touch the connection part or the wiring pattern of the inverter.
- Do not use inverters without a load or in the short-circuit mode.
- Use the LCD module within the rated voltage to prevent overheating and/or damage. Also, take steps to ensure that the connector does not come off.

Handling Precautions

- Since the LCD panel has glass substrate, avoid applying mechanical shock or pressure on the module. Do not drop, bend, twist or press the module.
- Do not soil or damage LCD panel terminals.
- Since the polarizer is made of easily-scratched material, be careful not to touch or place objects on the display surface.
- Keep the display surface clean. Do not touch it with your skin.
- CMOS LSI is used in the LCD module. Be careful of static electricity.
- Do not disassemble the module or remove the liquid crystal panel or the panel frame.
- Do not damage the film surface of the EL lamp; otherwise the lamp will be damaged by humidity.
- To set an EL lamp in an LCD module, push the EL lamp with its emitting side up, without pushing the rubber connectors too hard. If you damage them, the LCD module may not work properly.

Mounting and Designing

- To protect the polarizer and the LCD panel, cover the display surface with a transparent plate (e.g., acrylic or glass) with a small gap between the transparent plate and the display surface.
- Keep the module dry. Avoid condensation to prevent the transparent electrodes from being damaged.
- Drive LCD panel with AC waveform in which DC element is not included to prevent deterioration in the LCD panel.
- Contrast of LCD varies depending on the ambient temperature. To offer the optimum contrast, LC drive voltage should be adjusted. LCD driven in a high duty ratio must be provided with drive voltage adjustment method.
- Mount a LCD module with the specified mounting part/ holes.
- Design the equipment so that input signal is not applied to the LCD module while power supply voltage is not applied to it.
- Do not locate the CFL tube and the lamp lead wire close to a metal plate or a plated part inside the equipment. Otherwise stray capacity causes a drop in voltage, decreasing the brightness and the ability to start-up.

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the LCD panel gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetone)or aromatic solvents (toluene and xylene), as they may damage the polarizer.

Storing

- Store the LCD panel in a dark place, where the temperature is 25°C±10°C and the relative humidity below 65%. If possible, store the LCD panel in the packaging situation when it was delivered.
- Do not store the module near organic solvents or corrosive gases.
- Keep the module (including accessories) safe from vibration, shock and pressure.
- Use an LCD module with built-in EL backlight within six months of delivery.
- EL backlight is easily affected by environmental conditions such as temperature and humidity; the quality may deteriorate if stored for an extended period of time. Contact Seiko Instruments GmbH for details.
- Some parts of the backlight and the inverter generate heat. Take care so that the heat does not affect the liquid crystal or any other parts.
- Dust particles attached to the surface of the LCD or the surface of the backlight degrade the display quality. Be careful to keep dust out in designing the structure as well as in handling the module.
- Black or white air-bubbles may be produced if the LCD panel is stored for long time in the lower temperature or mechanical shocks are applied onto the LCD panel.

On This Brochure

- Seiko Instruments GmbH reserves the right to make changes without notice to the specifications and materials contained herein.
- The colors of the products reproduced herein may be different from the actual colors. Check color on actual products before using the product.
- The information contained herein shall not be reproduced in whole or in part without the express written consent of Seiko Instruments GmbH
- The products described herein are designed for consumer equipment and cannot be used as part of any device or equipment which influences the human body or requires a significantly high reliability, such as physical exercise equipment, medical equipment, disaster prevention equipment, gas related equipment, vehicles, aircraft and equipment mounted on vehicles.

Notes :