TUGAS AKHIR

ALAT PENABUR PAKAN TERNAK OTOMATIS DENGAN PENGGERAK MOTOR DC BERBASIS MIKROKONTROLLER AT89C2051

Disusun oleh :

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05.52.017

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INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
PROGRAM STUDI TEKNIK ELEKTRO D-3
KONSENTRASI TEKNIK LISTRIK
MALANG 2009

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ALAT PENABUR PAKAN TERNAK OTOMATIS DENGAN PENGGERAK MOTOR DC BERBASIS MIKROKONTROLLER AT89C2051

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ABSTRAK

Dalam beternak sangatlah penting dalam hal pemberian pakan, namun dengan kesibukan seseorang maka sangat minim waktu dalam pemberian pakan pada hewan ternak, maka kita dapat memanfaatkan teknologi elektromekanik dalam membantu pekerjaan kita sehingga dapat mengefisien waktu

Dalam kesempatan ini, penulis mencoba untuk memaparkan perencanaan dan pembuatan alat yang dinamis dan otomatis dalam pemberian pakan pada hewan ternak dengan menggunakan mikrokontroller AT89C2051 yang akan memberikan kemudahan bagi masyarakat untuk dapat menyalurkan hobi beternaknya tanpa meninggalkan pekerjaannya

Hasil yang diperoleh dari perancangan alat ini adalah terciptanya sebuah alat yang otomatis dalam pemberian pakan pada ternak tanpa kehadiran pemiliknya dengan berbagai keunggulan yang dimiliki antara lain :

1. *Motor DC GearBox sebagai penggerak mekanik alat mempunyai kekuatan yang lebih dari cukup untuk menggerakan tabung penampung pakan serta menggerakkan penabur pakan.*
2. *Sensor Infra Merah mampu bekerja dengan baik pada jarak 1 Meter hingga 6 Meter.*
3. *Penggunaan transformator 5A pada rangkaian power supplay telah mencukupi untuk konsumsi daya alat dengan baik.*

KATA PENGANTAR

Puji syukur penyusun panjatkan kehadirat ALLAH SWT yang telah melimpahkan nikmat dan hidayah –Nya sehingga penyusun dapat menyelesaikan tugas akhir yang berjudul **"ALAT PENABUR PAKAN TERNAK OTOMATIS DENGAN PENGGERAK MOTOR DC BERBASIS MIKROKONTROLLER AT89C2051 "**

Tugas akhir ini diajukan sebagai syarat guna menempuh ujian Sarjana jenjang Diploma Tiga (D-III) di Jurusan Teknik Elektro Institut Teknologi Malang.

Atas terselesaikannya tugas akhir ini penyusun mengucapkan terima kasih kepada:

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12. Kakakku Nina yang mendukungku.
13. Istriku yang selalu mendukungku untuk menyelesaikan tugas akhir ini.
14. Rekan – rekan mahasiswa dan semua pihak yang membantu hingga terselesainya laporan tugas akhir ini.

Penyusun menyadari bahwa laporan tugas akhir ini jauh dari sempurna oleh karena itu penyusun mengharapkan kritik dan saran yang membangun dari semua pihak guna penyempurnaan laporan tugas akhir ini.

Malang, 24 MARET 2009

Penyusun

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BAB I

PENDAHULUAN

1.1 Latar Belakang.

Sebagian masyarakat menengah kebawah sangatlah suka dalam beternak, umumnya adalah berternak ayam atau bebek. Dengan banyaknya hewan ternak maka peternak haruslah rutin dalam meluangkan waktu guna pemberian pakan. Masalah perawatan dan pembersihan kandang masihlah bisa dilakukan 1 kali dalam seminggu, akan tetapi masalah pemberian pakan/makanan untuk ternak haruslah setiap hari. Hal ini terkadang sangat merepotkan bagi peternak. Dengan kesibukan sehari-hari atau rutinitas yang padat bisa membuat kelalaian dalam pemberian pakan. Bahkan sewaktu-waktu jika pemilik rumah pergi/bepergian keluar kota dengan waktu yang agak lama, maka hal ini sangatlah membahayakan bagi kehidupan ternak yang dipeliharanya.

Maka dengan masalah tersebut diatas peternak dapat memanfaatkan teknologi elektro mekanik yang saat ini sangat berkembang pesat guna mempermudah manusia. Teknologi elektro mekanik dapat mengefisiensi waktu dan pekerjaan dimana pekerjaan yang sifatnya rutin dapat diwakilkan dengan mengoperasikan suatu mesin yang dapat bekerja sesuai dengan yang kita harapkan. Sehingga beban pekerjaan masyarakat bisa terkurangi dan dapat meningkatkan efisiensi kerja untuk meningkatkan produktifitas usaha dalam beternak.

Alat ini mempunyai keunggulan yaitu alat ini dapat menaburkan pakan ternak secara otomatis jika pakan dalam tempat yang disediakan telah habis. Sensor pakan menggunakan sinar Infra Merah dengan jarak jangkau yang jauh sehingga memungkinkan tempat pakan dapat diperpanjang hingga 6 meter. Penggerak alat menggunakan motor DC GearBox dengan kekuatan yang besar dengan konsumsi daya yang kecil. Alat juga dapat dioperasikan dengan menggunakan catu daya eksternal dengan menggunakan aki 24V.

1.2 Rumusan Permasalahan

Permasalahan pada perancangan tugas akhir ini adalah bagaimana cara untuk ?

1. Merancang mekanik penabur pakan ternak yang digerakan oleh Motor DC.
2. Merancang Hardware yang dapat menggerakan Motor DC.
3. Merancang minimum sistem berbasis mikrokontroler AT89C2051.
4. Merancang software mikrokontroler dengan bahasa Assembler.

1.3 Tujuan

Tujuan tugas akhir ini adalah untuk merancang dan membuat alat penabur pakan ternak otomatis.

1.4 Batasan Permasalahan

Dalam tugas akhir ini permasalahan akan dibatasi pada pembahasan perancangan mekanik menggunakan bahan yang ringan sehingga beban pada motor DC tidak terlalu besar. Ukuran mekanik disesuaikan dengan kekuatan pergerakan motor DC yang digunakan. Perancangan perangkat keras dengan basis mikrokontroller AT89C2051. Bahasa pemrograman menggunakan Assembler.

1.5 Metode Perancangan dan Perakitan

Metode yang dipakai dalam perancangan dan perakitan alat menggunakan sensor infra merah berbasis mikrokontroler AT89C2051 adalah:

1. Metode Studi Literatur

   Meliputi kegiatan mengumpulkan bahan-bahan yang merupakan referensi dari beberapa buku yang berisikan tentang mikrokontroler, motor dc, dan infrared.

2. Metode Perancangan Sistem

   Melakukan perencanaan dalam pembuatan rancang bangun serta pemrograman robot berbasis mikrokontroler AT89C2051.

3. Metode Persiapan Bahan Dan Peralatan

   Mempersiapkan semua bahan komponen rangkaian dan peralatan yang akan digunakan dalam perakitan.

4. Metode Perakitan Sistem

   Merakit semua bahan yang telah dipersiapkan menjadi sebuah alat kendali baik perakitan rangkaian ataupun perakitan rancang bangun mekanik.

5. Metode Pengujian dan Pengambilan Data

   Metode ini dilakukan guna menguji mekanik dan pengendali yang telah dirakit, apakah bergerak sesuai dengan yang diinginkan.

6. Pembahasan

7. Kesimpulan

1.6 Sistematika Pembahasan

Sistematika pembahasan dan penulisan laporan tugas akhir ini adalah sebagai berikut :

Bab I : Menjelaskan tentang latar belakang permasalahan, rumusan masalah, batasan masalah serta metodologi.

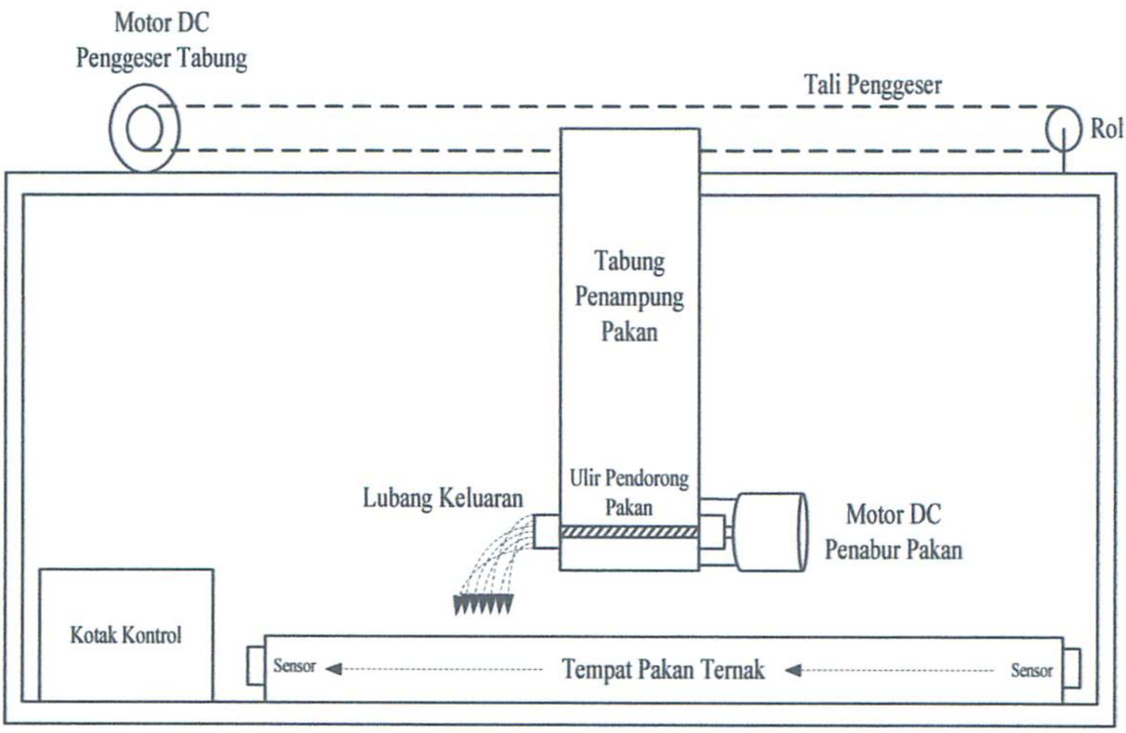
Bab II : Menjelaskan teori dasar yang menunjang dan berhubungan dengan perencanaan dan pembuatan alat.

Bab III : Menjelaskan tentang komponen-komponen dalam pembuatan tugas akhir, blok diagram sistem, perencanaan mekanik, perencanaan rangkaian hardware dan software, metode pengujian dan analisa.

Bab IV : Menjelaskan hasil pengujian dan analisa

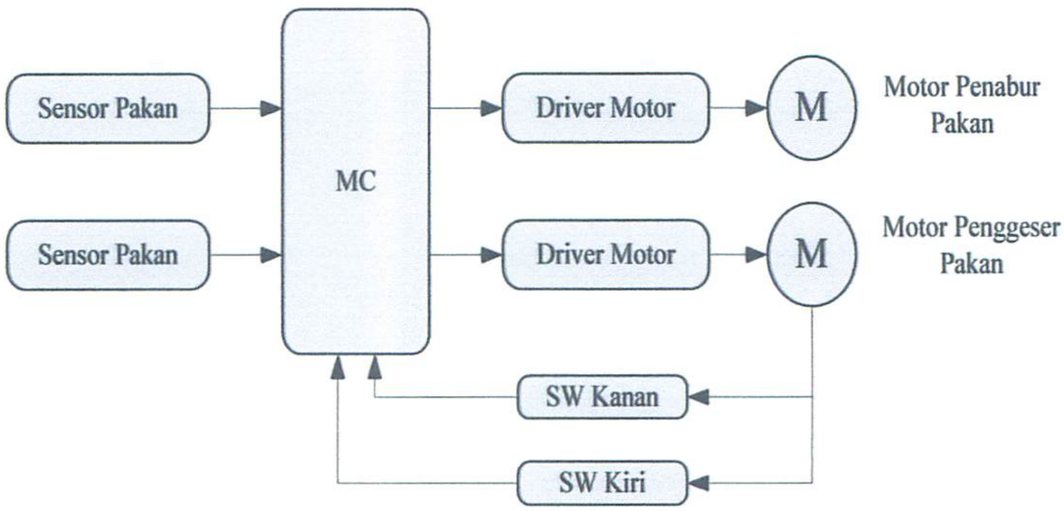
Bab V : Berisi kesimpulan dan saran untuk pengembangan alat yang di buat

1.7 Perencanaan Rancangan Mekanik Alat



Gambar 1.1
Rancangan Mekanik Alat

1. Jenis motor DC penabur pakan dan motor DC penggeser tabung adalah Motor DC Gear Box.
2. Rangka mekanik terbuat dari besi.
3. Tabung penampung pakan terbuat dari alumunium.
4. Penabur pakan menggunakan ulir besi yang terpasang pada lubang keluaran.
5. Rangkaian kontrol terkendali mikrokontroller ATMEL type AT89C2051.
6. Sensor kondisi pakan menggunakan infra red diameter 5mm yang terpasang pada tempat pakan.
7. Power Supply sebagai catu daya alat menggunakan transformator 5A.



Gambar 1.2
Diagram Blok Perancangan Alat

Pada perancangan alat sesuai diagram blok diatas dijelaskan bahwa, motor penggerak pada mekanik menggunakan jenis motor DC GearBox. Dimana motor DC tersebut akan dipasang pada rancangan mekanik. Motor DC penabur pakan berfungsi untuk mengeluarkan pakan dari tabung penampung. Sedangkan motor DC penggeser pakan berfungsi untuk meratakan penaburan dalam satu tempat pakan yang memanjang. Untuk menggerakkan motor DC digunakan rangkaian Driver sebagai penggerak motor yang nantinya akan mendapat signal dari Mikrokontroller. Penaburan pakan dilakukan secara otomatis dimana pada saat pakan habis maka mekanik penabur akan bekerja. Sebagai parameter kosong atau pakan telah habis digunakan sensor infra merah pada tempat pakan. Alat penabur pakan akan selalu bekerja secara otomatis jika pakan telah habis.

BAB II

LANDASAN TEORI

2.1. Mikrokontroler AT89C2051

Perbedaan mendasar antara mikrokontroler dengan mikroprosesor adalah mikrokontroler selain memiliki CPU juga dilengkapi memori dan input output yang merupakan kelengkapan sebagai sistem minimum mikrokomputer sehingga sebuah mikrokontroler dapat dikatakan sebagai mikrokomputer dalam keping tunggal (Singgle Chip Mikrokomputer) yang dapat berdiri sendiri.

Mikrokontroler AT89C2051 adalah mikrokontroler ATMEL yang kompatibel penuh dengan mikrokontroler keluarga MCS – 51 yang membutuhkan daya rendah, memiliki performan yang tinggi dan merupakan mikrokomputer 8 bit yang dilengkapi 4Kbyte EEPROM (Electrical Erasable and Programmable Read Only Memori) dan 128 Byte RAM internal. Program memori yang dapat diprogram ulang dalam sistem yang menggunakan programmer Nonvolalite Memori Konvensional.

Dalam sistem mikrokontroler terdapat dua hal yang mendasar, yaitu : perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

2.1.1. Perangkat keras mikrokontroler AT89C2051

Secara umum Mikrokontroler AT89C2051 memiliki :

- CPU 8 bit termasuk keluarga MCS – 51
- 2 Kb flash memori
- 128 internal RAM

- 2 buah port I/O, masing-masing terdiri atas 8 jalur I/O
- 2 Timer / counter 16 bit
- 1 Serial Port Full Duplex
- 15 I/O Lines
- 1 chip Oscilator

Dengan keistimewaan diatas pembuat alat menggunakan AT89C2051 menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak.

2.1.1.1. Arsitektur Mikrokontroller AT89C2051

Arsitektur mikrokontroller AT89C2051 sebagai berikut :

a. CPU (Centrl Procesing Unit)

Dengan 8 bit register A (accumulator) dan register B, yang optimal untuk aplikasi kontrol.

b. 16 bit program couter (PC) dan data pointer

c. 8 bit program status word (PSW)

d. 8 bit stack pointer (SP)

e. 128 byte internal RAM

- 4 bank register, masing-masing berisi 8 register
- 16 byte yang dapat dialamati pada bit level
- 80 byte genaral purpose memori data

f. 2 K byte internal EPROM

g. 15 pin Input – output tersusun atas P1 – P3, P1 (8 bit) dan P3 (7 bit)

h. 2 timer / counter

i. Receiver transmiter data serial full dupleks : SUBF

j. Control register : TCON, TMOD, SCON, PCON,IP dan IE

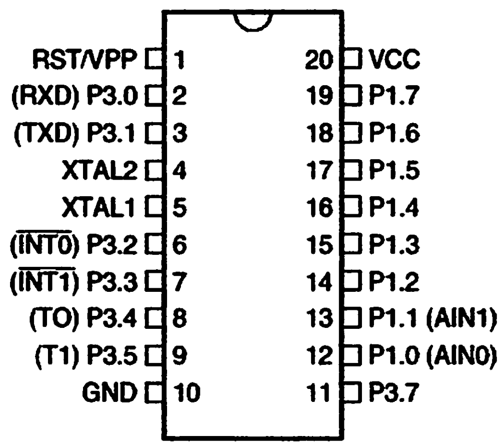
k. 5 buah sumber interrupt

2 buah sumber interupt eksternal dan 3 buah interupt internal

l. Oscilator dan Clock

2.1.1.2. Konfigurasi Pena –Pena Mikrokontroller AT89C2051

Mikrokontloller AT89C2051 terdiri dari 20 pin dengan konfigurasi segagai berikut :



Gambar 2.1
Konfigurasi Pena-Pena AT89C2051

Fungsi tiap pin sebagai berikut :

1. Gnd (ground)

   Dihubungkan dengan ground rangkaian

2. Vcc

Dihubungkan dengan sumber tegangan

3. Port 1 (P1.0 – P1.7)

Merupakan port Input-output dua arah dengan pull up. Port ini berfungsi sebagai Input atau output dan bekerja baik untuk operasi bit maupun byte, tergantung dari Pengaturan software.

4. Port (P3.0 – P3.7) Port 3 selain memiliki fungsi sebaai I/O juga mempunyai Fungsi khusus sebagai berikut :

- RD (P3.7) : Sinyal dataan memori data luar
- TI (P3.5) : Masukan dari pewakyu / pencacah I
- T0 (3.4) : Masukan dari pewaktu pencacah 0
- INT 1 (P3.3) : Interupt 1 eksternal
- INT 0 (P3.2) : Interupt 0 eksternal
- TXD (P3.1) : Keluaran pengiriman data untuk serial port (asinkron) atau sebagai keluaran clock (sinkron)
- RXD (P3.0) : Masukan penerimaan data serial (asinkron) atau sebagai masukan atau keluaran data (sinkron)

5. RST

Merupakan pin tinggi (high), pin ini aktif tinggi selama dua siklus mesin ketika osilator bekerja akan mereset peralatan. Selain berfungsi sebagai pin reset juga digunakan sebagai tegangan program dimana pada saat mikrokontroller dalam kondisi terprogram maka pin RST/VPP akan bertegangan 12 V.

6. XTAL 1 dan XTAL 2

Pin XTAL 1 merupakan pin input inverting oscilator amplifier dan input rangkaian internal clock operating. Sedangkan pin XTAL 2 merupakan pin output dari inverting oscilator amplifier.

7. EA / Vpp (External Access / Programming Supply Voltage)

Pin EA harus di-hold rendah secara external atau dihubungkan ke ground agar Mikrokontroller dapat dapat mengakses program memori eksternal dengan lokasi 0000H – FFFFH. Untuk mengakses memori internal pin ini dihubungkan ke Vcc.

2.1.1.3. SFR (Special Function Register)

Register fungsi khusus (Spesial Function Register) terletak pada 128 byte bagian atas memori data internal dan berisi register-register untuk pelayaan latch port, timer, program status words, control peripheral dan sebagainya. Alamat register fungsi khusus ditunjukkan pada tabel 2.1.

Tabel 2.1
Special Function Register

Simbol	Nama Register	Alamat
ACC		
B	Accumulator	$0E0_H$
PSW	Register B	$0F0_H$
SP	Program Status Word	0D0
DPTRT	Stack Pointer	81_H
DPL	Data Pointer 2 byte	-
DPH	Bit rendah	82_H
P0	Bit tinggi	83_H
P1	Port 0	80_H
P2	Port 1	90_H
P3	Port 2	$0A0_H$
IP	Port 3	$0B0_H$
IE	Interupt Periority Control	$0B8_H$
TMOD	Interupt Enable Control	$0A8_H$
TCON	Timer / Counter Mode Control	89_H
TH0	Timer / Counter Control	88_H
TL0	Timer / Counter 0 High Control	$8C_H$
TH1	Timer / Counter 0 Low Control	$8A_H$
TL1	Timer / Counter 1 High Control	$8D_H$
SCON	Timer / Counter 0 Low Control	$8B_H$
SBUF	Serial Control	98_H
PCON	Serial Data Buffer	99_H
	Power Control	87_H

Beberapa macam register fungsi khusus yang sering digunakan adalah sebagai berikut :

- Accumulator (ACC) merupakan register untuk penambahan dan pengurangan .Perintah mnemonic untuk mengakses akumulator disederhanakan sebagai A.
- Register B merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian.
- Stak Pointer (SP) merupakan register 8 bit yang dapat diletakkan dialamat manapun pada RAM internal.
- Data Pointer (DPTR) terdiri dari dua register, yaitu untuk byte tinggi (Data Pointer High, DPH) dan byte rendah (Data Pointer Low, DPL) yang berfungsi untuk mengunci alamat 16 bit.
- Port 0 sampai Port 3 merupakan register yang berfungsi untu membaca dan mengeluarkan data pada port 0, 1, 2, 3. Masing – masing register ini dapat dialamati per-byte.
- Control Register terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sitem interupsi, terdapat register IE (Interupt Enable). Untuk mengontrol pelayanan timer/counter terdapat register khusus, yaitu register TCON (Timer Counter Control) serta pelayanan port serial menggunakan register SCON (Serial Port Control).

2.1.1.4 Sistem Interupsi

Mikrokontroller AT89C2051 mempunyai 5 buah sumber interupsi yang dapat membangkitkan permintaan interupsi yaitu INT0, INT1, T1, T2 DAN Port serial.

Saat terjadinya interupsi mikrokontroller secara otomatis akan menuju ke sub rutin pada alamat tersebut. Setelah interupsi selesai dikerjakan, mikrokontroller akan mengerjakan program semula. Tiap-tiap interupsi dapat anable atau disable secara software.

Tingkat prioritas semua sumber interupt dapat diprogram sendiri-sendiri dengan set atau clear bit pada (Interupt Priority). Jika dua permintaan interupsi dengan tingkat prioritas yang berbeda diterima secara bersamaan, permintaan interusi dengan permintaan yang tertinggi yang akan dilayani. Jika permintan interupsi dengan prioritas yang sama diterima bersamaan, akan dilakukan polling untuk menentukan yang mana yang akan dilayani. Bit-bit pada IP adalah sebagai berikut :

-	-	-	PS	PT1	PX1	PT0	PX0

Priority byt = 1 menandakan prioritas tinggi

Priority byt = 0 menandakan rendah

Tabel 2.2
Permintaan interupsi

Simbol	Posisi	Fungsi
-	IP. 7	Kosong
-	IP. 6	Kosong
-	IP. 5	Kosong
PS	IP. 4	Bit prioritas interupsi port serial
PT1	IP. 3	Bit prioritas interpsi Timer
PX1	IP. 2	Bit prioritas interupsi INT1
PT0	IP. 1	Bit prioritas interupsi Timer 0
PX0	IP. 0	Bit prioritas interusi INT0

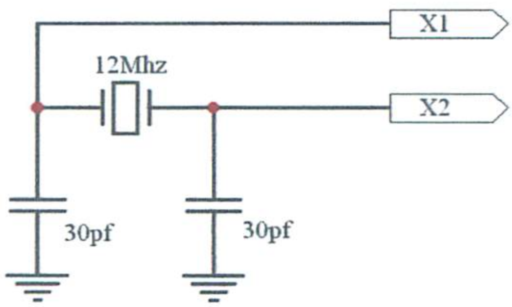
2.1.1.5 Rangkaian Clock

Mikrokontroller AT 89C2051 memiliki internal clock pada pin 5 (X1) dan pin 4 (X2) yang berfungsi sebagai sumber clock, tetapi masih diperlukan rangkaian tambahan untuk membangkitkan clock tersebut. Rangkaian clock ini merupakan jantung dari rangkaian minimum mikrokontroller AT 89C2051, yang terdapat oscillator sebagai pembangkit pulsa pada mikrokontroller AT 89C2051, mempunyai input XTAL 1 dan XTAL 22. Dimana XTAL1 adalah input yang dihubungkan dengan rangkaian osilasi dalam rangkaian mikrokontroller sedangkan XTAL 2 adalah output feedback untuk osilasi.

Rangkaian ini terdiri dari dua buah capacitor dan sebuah crystal, dengan ketentuan :

C1 dan C2 = 20 – 40 pF (digunakan untuk crystal)

= 30 – 40 pF (digunakan untuk keramik resonator)



Gambar 2.2
Rangkaian Clock
(Sumber : Data sheet ATMEL, 8-Bit Microcontroller With 4 Kbytes Flash AT 89C2051)

Perencanaan cristal berikut menggunakan 12 MHZ yang dimaksudkan untuk ketepatan perhitungan besar band rate pada system trasmisi pada serial, sedangkan nilai kapasitor yang digunakan adalah 30 pF sesuai dengan toleransi yang dispesifikasikan. Clock ini menghasilkan suatu interval pewaktu yang dinamakan pulsa, untuk sebuah intruksi program terkecil diperlukan beberapa pulsa yang dikelompokkan dalam bagian keadaan (state) menunjukkan dasar dari interval waktu untuk menandai suatu operasi, seperti penempatan Opcode Byte, Pengerjaan Opcode atau penulisan data byte. Rangkaian clock ini berfungsi untuk menentukan kecepatan kerja siklus program yang dibuat.

2.2. Motor DC

Motor DC adalah peralatan elektromekanis yang mengubah daya listrik menjadi daya mekanis dengan sumber arus sebagai supply energi listriknya.

Pada umumnya motor DC terdiri dari atas bagian yang diam dan bagian yang bergerak. Bagian yang diam biasa disebut stator dan bagian yang bergerak disebut rotor. Stator adalah kumparan medan yang berbentuk kutub sepatu untuk menghasilkan medan magnet. Rotor merupakan kumparan jangkar dengan belitan konduktor (kumparan) untuk mengimbaskan ggl (gaya gerak listrik) pada konduktor yang terletak pada alur-alur jangkar. Celah udara memungkinkan berputarnya jangkar dalam medan magnet.

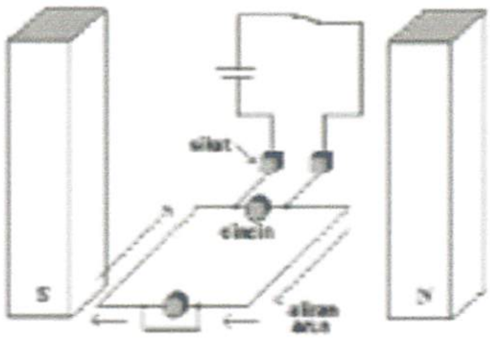
Pada stator dililitkan gulungan kawat untuk kumparan medan. Arus yang mengalir pada kumparan ini disebut arus medan (i_e) yang pada rangkaian motor DC menghasilkan fluks magnet utama (Φ_e) pada stator dan rotor. Kumparan jangkar adalah lilitan yang digulungkan secara aksial pada besi rotor dan dihubungkan ke batang-batang komutator. Kumparan ini lewati listrik melewati sikat-sikat dan komutator tersebut. Arus yang mengalir dalam kumparan ini dinamakan arus jangkar (i_a). arus ini menghasilkan ggm (gaya gerak magnet) yang memiliki arah tegak lurus terhadap fluks magnet utama yang ditimbulkan oleh arus pada kumparan stator *(Zuhal,1991)*.

Motor DC dibedakan menjadi 4 yaitu :

1. Motor Shunt
2. Motor Seri
3. Motor Kompon

Pada gambar 2.3 memperlihatkan gambar dasar motor DC. Motor ini menggunakan sikat dan cincin belah (komotator). Saat siklus pertama, arus mengalir dari kutub positif kekutub negative. Aliran arus yang melewati bagian kabel yang berada didekat kutub N magnet akan menimbulkan gaya Lorentz kebawah.

Sementara itu aliran arus yang melewati kabel yang berada didekat kutub S magnet akan menyebabkan gaya Lorentz keatas. Kedua perpaduan gaya Lorentz tersebut akan menyebabkan kawat berputar. Pada siklus berikutnya teerjadi hal yang serupa seperti pada siklus sebelumnya. Apabila arus terus-menerus dialirkan, maka kawat akan berputar secara terus-menerus pula. Pada aplikasi sesungguhnya, kawat adalah sebuah rotor yang akan dikopel dengan sebuah as dan akan memutar as tersebut terus-menerus seiring perputaran motor.



Gambar 2.3
Bagan motor DC
Sumber : www.elektroindonesia.com

Pada motor DC, kumparan medan yang dialiri arus listrik akan menghasilkan medan magnet yang melingkupi kumparan jangkar dengan arah tertentu. Konverter energi baik energi listrik menjadi energi mekanik (motor) maupun sebaliknya dari energi mekanik menjadi energi listrik (generator) berlangsung melalui medium medan magnet. Energi yang akan diubah dari suatu sistem ke sistem yang lain, sementara akan tersimpan pada medium medan magnet untuk kemudian dilepaskan menjadi energi sistem lainnya. Dengan demikian, medan magnet disini selain berfungsi sebagi tempat penyimpanan energi juga sekaligus proses perubahan energi, dimana proses perubahan energi pada motor arus searah dapat digambarkan pada gambar 2.4.

Energi Listrik	Medan Magnet	Energi Mekanik

Gambar 2.4
Proses Konversi Energi pada Motor DC`
Sumber : www.elektroindonesia.com

2.2.1. Prinsip Kerja Motor DC

Prinsip kerja motor DC berdasarkan pada penghantar yang menghantarkan arus ditempatkan dalam suatu medan magnet penghantar tersebut akan mengalami suatu gaya. Gaya tersebut akan menimbulkan torsi yang akan menimbulkan rotasi mekanik sehingga motor akan berputar. Motor DC ini akan menerima sumber arus searah dari jala-jala kemudian diubah menjadi energi mekanik berupa putaran yang akan digunakan oleh peralatan yang lain. Ada tiga hal pokok dari prinsip kerja motor DC antara lain:

- Adanya garis-garis gaya medan magnet (fluks) antar kutub-kutub yang berada dalam stator.
- Penghantar yang dilalui arus listrik ditempatkan pada jangkar yang berada dalam medan magnet.
- Pada penghantar timbul gaya yang menghasilkan torsi.

Arah dari garis-garis gaya (fluks) medan magnet yang dihasilkan oleh kutub, arah arus yang mengalir dan arah dari gaya saling tegak lurus satu sama yang lainya dan sesuai dengan kaidah tangan kiri yang berbunyi sebagai berikut :

“ Apabila tangan kiri dibiarkan terbuka dan diletakkan diantara kutub utara dan kutub selatan, sehingga garis-garis gaya yang keluar dari kutub Utara menembus telapak tangan kiri dan arus dalam kawat mengalir searah dengan keempat jari, maka kawat tersebut akan mendapat gaya yang jatuhnya sesuai dengan ibu jari ”.

Besarnya gaya yang dihasilkan adalah:

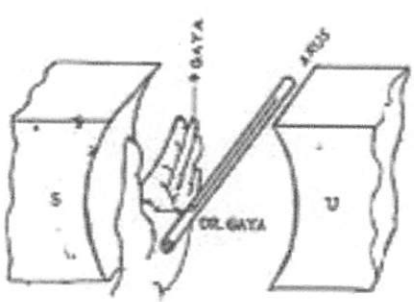
$F = B.\ I.\ \lambda$ (Newton)

Dimana:

B = kerapatan fluks (weber)

I = arus yang mengalir pada penghantar (ampere)

λ= panjang penghantar (meter)



Gambar 2.5
Kaidah tangan kiri
Sumber : www.elektroindonesia.com

2.2.2 Rumus Dasar Motor DC

Berdasarkan teori elektromagnetik, dapat diturunkan 3 rumus dasar untuk mesin arus searah ini adalah:

- Tegangan induksi

$$E_a = C.n.\Phi \quad \text{volt}$$

- Kecepatan

Rumus kecepatan ini sebenarnya diturunkan dari rumus tegangan induksi dan merupakan kecepatan motor tanpa beban:

$$n = \frac{Ea}{C.\Phi}$$

Pengaturan kecepatan dapat dilakukan dengan mengubah E_a atau Φ

- Kopel elektromagnetik

$$T = C.I_a.\Phi$$

Kopel elektromagnetik ini tidak sama dengan kopel yang terdapat pada sumbu. Dengan mengurangi kopel geser barulah didapat harga kopel pada sumbu. Hubungan lain antara kopel elektromagnetik dengan daya mekanik, yaitu:

$$E_a.I_a = T.W_m$$

$$W_m = \frac{2\pi.n}{60} = kecep \quad sudut$$

Keterangan:

Φ = fluks/kutub

n = putaran (rpm)

C = (p/a) x (Z/60) = konstanta

P = jumlah kutub

a = jalur parallel konduktor jangkar

Z = jumlah konduktor jangkar

I_a = arus jangkar

2.3 Relay (Reed Switch)

Dalam dunia elektronika, relay dikenal sebagai komponen yang dapat mengimplementasikan logika switching. Sebelum tahun 70an, relay merupakan "otak" dari rangkaian pengendali. Baru setelah itu muncul PLC yang mulai menggantikan posisi relay. Relay yang paling sederhana ialah relay elektromekanis yang memberikan pergerakan mekanis saat mendapatkan energi listrik. Secara sederhana relay elektromekanis ini didefinisikan sebagai berikut :

1. Alat yang menggunakan gaya elektromagnetik untuk menutup (atau membuka) kontak saklar.
2. Saklar yang digerakkan (secara mekanis) oleh daya / energi listrik.

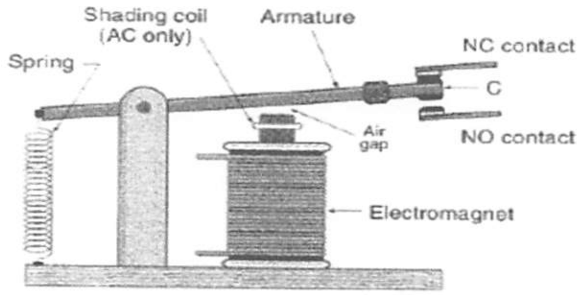
2.3.1. Prinsip Kerja Dan Simbol

Relay terdiri dari coil dan contact. Perhatikan gambar 2.6, coil adalah gulungan kawat yang mendapat arus listrik, sedang contact adalah sejenis saklar yang pergerakannya tergantung dari ada tidaknya arus listrik di coil.

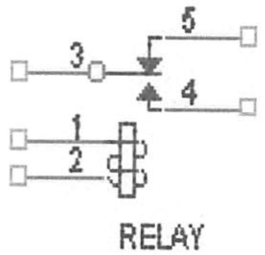
Contact ada 2 jenis :

a. Normally Open (kondisi awal sebelum diaktifkan open).
b. Normally Closed (kondisi awal sebelum diaktifkan close).

Secara sederhana berikut ini prinsip kerja dari relay : ketika Coil mendapat energi listrik (energized), akan timbul gaya elektromagnet yang akan menarik armature yang berpegas, dan contact akan menutup



Gambar 2.6
Skema relay elektromekanik
(Kilian, Christopher T, 1996)



Gambar 2.7
Simbol Relay (Kilian, Christopher T, 1996)

Bagian titik kontak dibagi menjadi 2 bagian yaitu bagian kontak utama dan kontak bantu yaitu :

1. Bagian kontak utama gunanya untuk menghubungkan dan memutuskan arus listrik bagian yang menuju beban /pemakai.
2. Bagian kontak bantu gunanya untuk menghubungkan dan memutuskan arus listrik ke bagian yang menuju bagian pengendali.

Kontak Bantu mempunyai 2 kontak yaitu kontak hubung (NC) dan kontak putus (NO) menandakan masing-masing kontak dan gulungan spool.

2.3.2. Jenis-Jenis Relay

Seperti saklar, relay juga dibedakan berdasar pole dan throw yang dimilikinya. Berikut definisi pole dan throw:

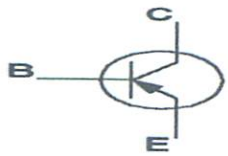
- Pole : banyaknya contact yang dimiliki oleh relay
- Throw : banyaknya kondisi (state) yang mungkin dimiliki contact

Berikut ini penggolongan relay berdasar jumlah pole dan throw :

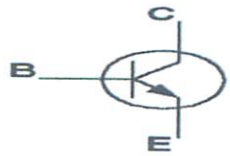
- SPST (Single Pole Single Throw)
- DPST (Double Pole Single Throw)
- SPDT (Single Pole Double Throw)
- DPDT (Double Pole Double Throw)
- 3PDT (Three Pole Double Throw)
- 4PDT (Four Pole Double Throw)

2.4. Transistor

Transistor adalah suatu komponen semikonduktor yang dibuat dari pertemuan PN, pada transitor terdapat tiga buah terminal yaitu : Emitor (E), Basis (B) dan Kolektor (C). Macam transistor dibagi menjadi dua tipe yaitu tipe PNP dan tipe NPN, seperti pada gambar berikut :



Gambar 2.8
Transistor jenis PNP



Gambar 2.9
Transistor jenis NPN

Pada gambar 2.8 menunjukan sebuah transistor PNP, dimana dioda emiter dan kolektor menunjuk arah yang berlawanan dengan arah pada transistor NPN, semua arus dan tegangan dibalik jika transistor PNP dibias forward. Dengan perkataan lain, untuk membias forward dioda emiter dari transistor PNP. Karena dioda emitor menunjuk kedalam, arus emiter konvensional mengalir kedalam transistor PNP, arus basis dan kolektor mengalir keluar.

Simbol skematik NPN ditunjukkan pada gambar 2.9. Emiter mempunyai tanda kepala panah tetapi kolektor tidak, yang penting khususnya yaitu kepala panah menunjukkan arah dari arus konvensional emiter. Arus konvensional emiter mengalir keluar dari basis, arus konvensional basis dan kolektor mengalir kedalam transistor NPN.

Ada tiga konfigurasi untuk menyambung transistor bila dipakai dalam rangkaian yaitu :

- konfigurasi Common Emitor (CE) dimana diumpankan antara basis dan emiter. Konfigurasi ini adalah yang paling banyak pemakaiannya karena fleksibelitas dan penguatannya.
- Konfigurasi Common Basis (CB) dimana basisnya milik bersama bagi input dan output.
- Konfigurasi Common Colector (CC) dimana kolektornya merupakan nilai bersama. Konfigurasi ini dikenal dengan pengikut emitor karena outputnya diambil di emitor.

Transistor mempunyai dua keadaan yaitu keadaan kerja jenuh (saturasi) dan keadaan tidak kerja (cut off). Perubahannya berupa arus atau tegangan. Pada keadaan kerja jenuh (saturasi) tegangan kolektor akan menjadi rendah (mendekati nol), dengan demikian arus kolektor akan menjadi sangat besar dan arus yang menuju beban akan kecil. Pada keadaan tidak bekerja (cut off) tegangan kolektor akan menjadi besar, dengan demikian arus kolektor akan mengalir menuju beban. Pada kondisi normal masukanya tidat di bias sehingga titik kerjanya berada pada kondisi cut off, sehingga tidak ada arus yang menuju beban (Pambudi,2002).

2.4.1. Transistor Sebagai Saklar

Untuk mengfungsikan transistor sebagai saklar elektronik, transistor dibuat dalam kondisi :

1. Transistor dalam kondisi jenuh (Saturasi)
2. Transistor dalam kondisi sumbat (Cut Off)

Transistor dalam kondisi jenuh (saturasi) terjadi apabila Ib lebih besar dari Ib (sat) dan arus kolektor Ic = maksimum. Pada daerah saturasi, Dioda kolektor menuju ke bias maju, karena hal ini transistor akan kehilangan kerja normalnya dan transistor bertindak sebagai suatu tahanan dengan Ohm yang kecil. Selanjutnya kenaikan pada arus basis tidak menghasilkan kenaikan pada arus kolektor. Tegangan Vce pada daerah saturasi biasanya hanya beberapa perpuluh Volt, tergantung berapa besar arus kolektor.

$$Ic(sat) = \frac{Vcc - Vce(jenuh)}{Rc}$$

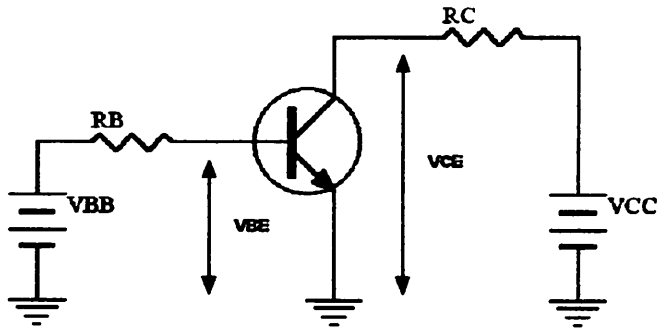
$$Ic(sat) = \frac{Vcc}{Rc}$$

Sedangkan arus basis yang dapat menimbulkan penjenuhan adalah :

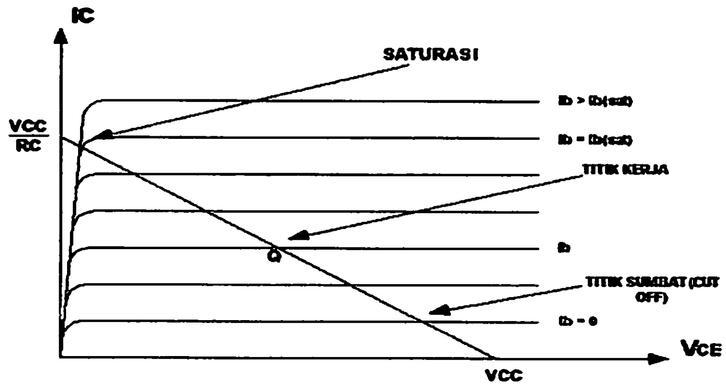
$$Ib(sat) = \frac{Ic(sat)}{\beta dc}$$

$$Ib(sat) = \frac{Vbb - Vbe}{Rb}$$

Transistor dalam kondisi Sumbat/Cut Off dimana titik garis beban memotong kurva Ib = 0 (titik sumbat/cut off), dimana Ib = 0 dan Ic sangat kecil sehingga dapat diabaiakan hanya ada arus bocor Iceo sehingga tegangan Vce (CutOff)



Gambar 2.10
Rangkaian Switching Transistor
(Sumber : Komunikasi Elektronika)

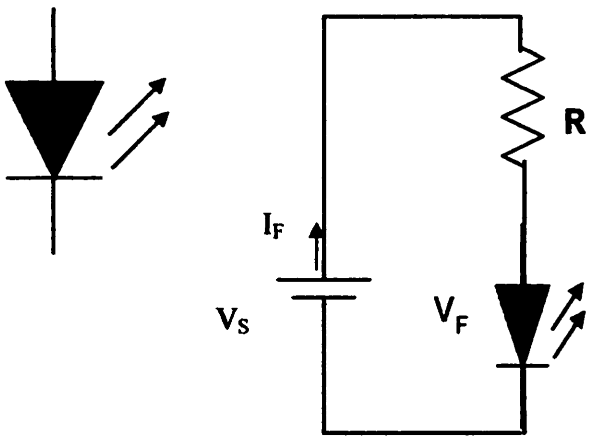


Gambar 2.11
Garis Beban DC
Sumber (Komunikasi Elektronika)

2.5 LED (Infra Merah)

Emitter semikonduktor adalah alat dengan sambungan P N yang menghasilkan cahaya kalau di biaskan dalam keadaan biasa (forward), yaitu positif ke jenis P (anode) dan negatif ke jenis N. Alat ini disebut LED (light Emiting Dioda), simbol LED diperlihatkan pada gambar 2.12.

Emiter cahaya semikonduktor di buat dalam berbagai ukuran panjang gelombang, sehingga secara teoritis dapat di beri tanda warna. Dalam kenyataan, warna dipabrik terbatas pada reaksi spectrum silicon, gallium arsenide, gallium fosfisida dan gallium arsanida fosfida. Warna yang sering di gunakan adalah merah, hijau, kuning, dan jingga. Dalam aplikasi elektronik LED merupakan diode yang mengeluarkan cahaya infra merah (infra red emiting diodes).



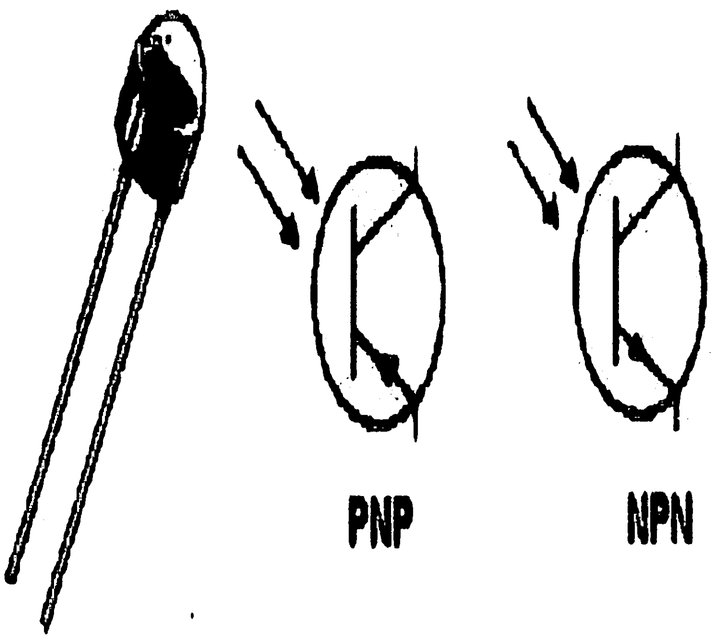
$$R = \frac{V_S - V_F}{I_F} \quad \text{............(2.1)}$$

Gambar 2.12.
simbol LED (infra merah)

Dioda penghasil cahaya yang terlihat banyak di pakai sebagai indikator dan sebagai display digital. Keuntungan LED di bandingkan lampu pijar yaitu umurnya lebih lama, tegangan rendah (1V sampai 2V) dan saklar ON/OFF-nya cepat (nano detik).

2.6 Fototransistor

Fototransistor adalah komponen semikonduktor yang istimewa yakni tanpa memiliki kaki basis akan tetapi mempunyai input yang dapat di operasikan dengan cahaya. Gambar di bawah ini menunjukkan bentuk dan simbol fototransistor.



Gambar 2.13.
Bentuk dan simbol fototransistor

2.7 Transformator

Transformator adalah suatu alat listrik yang dapat memindahkan dan mengubah energi listrik dari satu atau lebih rangkaian listrik ke rangkaian listrik yang lain melalui suatu gandengan magnet dan berdasarkan prinsip induksi elektromagnetik.
Transformator terdiri dari 2 bagian utama. Bagian pertama adalah primer dan kedua adalah sekunder, maka kumparannya dibagi menjadi dua bagian menurut keperluan mesin tersebut. Disini berlaku arus lisriknya di transfer dari kumparan pertama menuju kumparan kedua, oleh sebab itu dalam kumparannya dibagi dua bagian dengan fungsi sendiri-sendiri yang berbeda satu dengan lainnya, sebab fungsi yang pertama bekerja menerima sumber arus dan yang kedua meneruskan sumber arus yang sudah diolah menjadi arus yang sesuai dengan keperluannya. Maka kumparan yang kedua disebut sekunder dan yang menerima sumber arus listrik pertama disebut kumparan primer

2.7.1. Prinsip Dasar Transformator

Piranti transformator banyak digunakan untuk berbagai keperluan yang disesuaikan dengan kondisinya. Maka transformator bisa berfungsi apabila ada tegangan, bila tidak ada tegangan maka tidak akan berhasil melakukan perubahan tegangan yang lebih tinggi atau yang lebih rendah. Oleh sebab itu dalam system kerja transformator dibagi menjadi dua yaitu :

1. Transformator penaik tegangan (*Step Up*)
2. Transformator penurun tegangan (*Step Down*)

Pada transformator penaik tegangan tegangan (Step Up) lilitan tegangan rendahnya merupakan sisi primer, sedangkan lilitan tegangan tingginya merupakan sisi sekunder. Adapun transformator penurun tegangan tegangan (Step Down) lilitan tegangan tingginya merupakan sisi primer dan lilitan tegangan rendahnya merupakan sisi sekunder.

2.7.2. Prinsip Kerja Transformator

Pada dasarnya prinsip kerja transformator adalah menggunakan Induksi Elekromagnetik. Apabila sisi kumparan primer di hubungkan dengan sumber tegangan, maka arus mengalir pada kumparan primer, karena rangkaian tertutup sehingga timbul fluksi, dan fluksi tersebut menginduksi kumparan sekunder dimana kumparan sekunder tersebut akan timbul tegangan atau tegangan induksi.

2.8. Resistor

Sebagian orang menyebutnya dengan Restan. Artinya penahan sesuatu. Ada lagi yang menyebutnya Tahanan. Alat ini merupakan komponen terbanyak yang dipasang pada benda elektronika. Dinamakan demikian karena ia berfungsi sebagai penahan arus sementara sebelum diproses dan disalurkan pada komponen lainnya. Dalam penahanan sementara ini arus bisa diperkecil atau sebaliknya sesuai dengan besar kecilnya tahanan. Didalamnya masih banyak jenis tahanan, antara lain :

1. Fixed Restan (Tahanan Tetap)
2. Resistor Variabel
3. Potensiometer.

Pada dasarnya ketiga tahanan itu mempunyai sifat yang sama yakni menahan arus listrik sementara. Tetapi pada poin 2 dan 3, memiliki kelebihan karena tahanannya dapat diubah. Sedangkan pada poin 1 arus yang masuk tidak bisa diubah-ubah, tetap.

1. Fixed Restan (Tahanan Tetap)

Alat ini bentuknya kecil dan memiliki gelang bervariasi. Gelang-gelang warna ini adalah menunjukkan besar kecilnya nilai tahanan arus didalamnya. Warna-warna gelang tersebut sangat penting artinya bagi penggemar elektronika dan harus diketahui.
Resistor umumnya berbentuk kecil dengan dua kaki pada bagian dua ujungnya. Resistor tidak mempunyai kutub negative dan positif, sehingga pemasangannya boleh terbalik, asalkan nilainya sama dengan nilai yang tertera pada pcb .
Resistor terbuat dari bahan arang sehingga arus yang ada dalam resisitor tetap tidak bisa diubah ubah lagi. Bila nilai ohmnya tidak sesuai dengan arus yang masuk (lebih besar arus dari nilainya) maka komponen ini jadi terbakar dan tidak berfungsi lagi.

2. Resistor variable

Prinsip kegunaannya hampir sama dengan fixed restan. Komponen ini pun dapat menahan arus untuk sementara waktu. Ttetapi dapat diperbesar dan sebaliknya sesuai dengan nilai ohm yang ada. Bila kita ingin mengubah nilai ohm cukup dengan mengetrim (memutar) menggunakan obeng kekiri atau kekanan.

3. Potensiometer

Potensiometer masuk dalam komponen resistor sebab sifatnya menahan arus, tetapi dapat diubah ubah nilai ohmnya. Bisa dikatakan komponen ini mempunyai sifa adjustable manual resistor

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

3.1 Pendahuluan.

Didalam bab perencanaan dan pembuatan alat ini, kami akan membahas tentang bagaimana cara kerja rangkaian dari masing-masing blok. Komponen Utama dari alat yang akan di buat menggunakan mikrokontroller AT89C2051. Dimana Mikrokontroller akan memproses Input Output dari rangkaian pendukung.

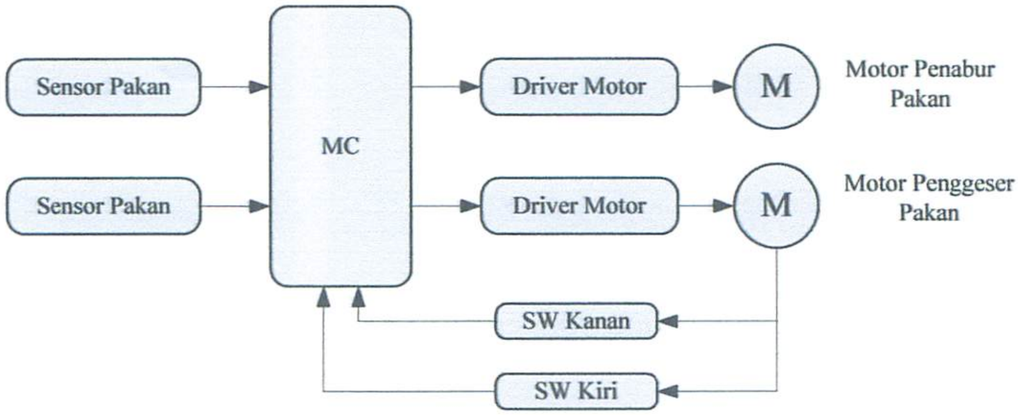
Sistem kerja rangkaian alat penabur pakan ini pertama akan membaca sensor infra merah yang terpasang pada tempat pakan ternak. Jika pakan ternak masih ada maka sinar infra merah akan terhalang oleh pakan ternak, sehingga sensor akan berlogika High dan mikrokontroller tidak akan memproses apa – apa atau dalam kondisi standby. Jika pakan ternak telah habis maka sensor atau sinar infra merah tidak terhalang sehingga sensor infra merah akan berlogika Low dan mikrokontroller akan menggerakkan motor penabur pakan dan motor penggerak tabung penampung pakan kekiri. Jika tabung penampung sudah bergerak dan sampai mengenai limit switch sebelah kiri maka motor penggerak tabung akan bergerak kembali kekanan. Jika sudah sampai kekanan dan mengenai limit switch sebelah kanan maka mikrokontroller akan membaca lagi sensor infra merah apakah pakan sudah penuh atau banyak. Jika pakan sudah penuh atau banyak maka motor penabur pakan dan penggerak tabung penampung akan di OFF kan, akan tetapi jika pakan belum penuh maka mikrokontroller akan menggerakkan kembali motor penabur dan penggerak pakan bergerak kekiri lagi hingga kembali lagi keposisi kanan.

3.2. Diagram Blok Rangkaian.

Dalam merancang suatu rangkaian ada bebera hal yang perlu diperhatikan, yaitu tentang perencanaan sistem kerja rangkaian dari masing-masing bagian yang mempunyai fungsi atau kerja yang di inginkan. Sehingga nantinya akan didapatkan suatu Blok-blok rangkaian yang disusun menjadi Diagram Blok. Apabila Diagram Blok sudah dibuat, maka untuk menentukan komponen-komponen apa saja yang dibutuhkan akan lebih mudah. Setelah rancangan Diagram Blok sudah terbuat maka pembuatan alat sudah bisa dimulai.

Didalam perencanaan pembuatan alat penabur pakan ternak otomatis ini terdapat beberapa bagian yang akan dibuat untuk menjadi rangkaian, antara lainnya adalah :

1. Perancangan Mekanik Penabur Pakan Ternak
2. Perancangan Rangkaian Kontrol
3. Perancangan Rangkaian Pensaklaran / Switch
4. Perancangan Rangkaian Sensor Infra Merah
5. Perancangan Rangkaian Driver Motor DC



Gambar 3.1
Blok Diagram Rangkaian Alat Penabur Pakan Ternak

3.3. Perencanaan Dan Pembuatan Rangkaian.

Pada perancangan dan pembuatan ini juga akan dibahas sistem Kontrol dengan menggunakan mikrokontroller AT89C2051 yang berfungsi sebagai otak dari seluruh rangkaian ini.

Berikut ini adalah penjelasan singkat dari masing-masing blok rangkaian sesuai dengan blok diagram diatas.

1. Mekanik Alat Penabur Pakan Ternak.

   Mekanik terbuat dari rangka besi kotak dengan dinding tabung terbuat dari bahan alumunium. Kapasistas tabung penampung pakan ternak diharapkan dapat menampung pakan hingga 5 - 7 Kg.

2. Rangkaian Kontrol Menggunakan Mikrokontroller AT89C2051.

   Rangkaian ini terdiri dari Komponen MikroKontroller AT89C2051 sebagai pengendali sistem utama dari keseluruhan rangkian. Mikrokontroller mengatur semua masukan/ Input dan keluaran/ Output dari setiap rangkaian pendukung.

3. Rangkaian Pensaklaran.

   Blok rangkaian pensaklaran disini terdiri dari komponen Limit Swicth. Limit Swicth berfungsi sebagai pengendali posisi tabung penampung pakan ternak. Limit Swicth terdiri dari Switch posisi kanan dan posisi kiri.

4. Rangkaian Sensor Infra Merah.

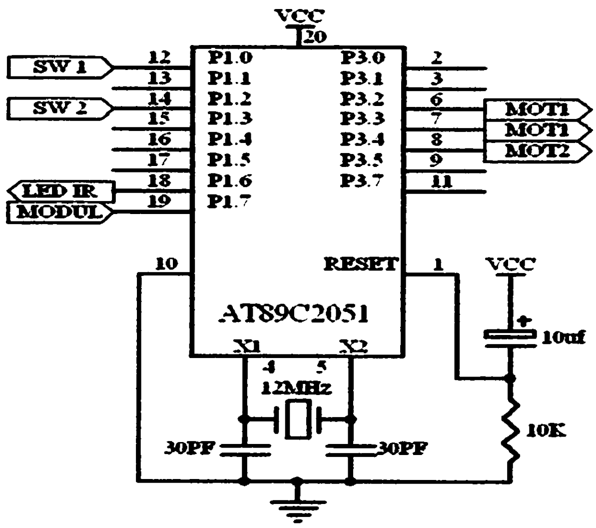
   Rangkaian Sensor Infra merah menggunakan LED IR sebagai transmitter gelombang cahaya infra merah dengan frekuensi 40Khz, sedangkan receivernya adalah module IR. Module IR akan mengeluarkan output berlogika High jika tidak menerima gelombang sinar IR dengan frekuensi 40Khz, dan apabila menerima gelombang sinar maka outputnya akan berlogika Low.

5. Rangkaian Driver Motor DC.

   Rangkaian driver motor DC sebagai penggerak mekanik penabur pakan dan penggerak tabung penampung pakan. Motor DC penabur pakan hanya berputar satu arah saja, sedangkan Motor DC penggerak tabung penampung pakan berputar kanan kiri.

3.3.1. Rangkaian Kontrol Menggunakan Mikrokontroller AT89C51.

Mikrokontroller AT89C2051 adalah suatu chip IC yang terdiri dari 20pin. Dalam perancangan dan pembuatan alat ini pin-pin yang dipergunakan adalah sebagai berikut :

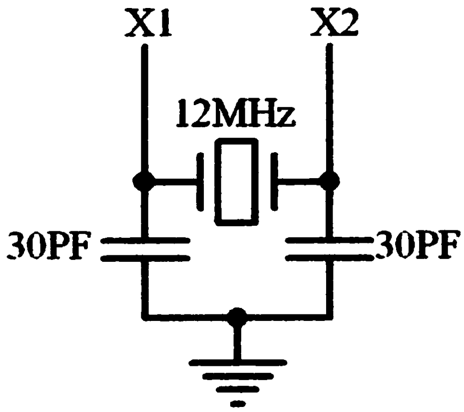


Gambar 3.2
Rangkaian Mikrokontroller AT89C2051.

Mikrokontroller AT89C2051 memiliki internal clock pada pin 5 (X1) dan pin 4 (X2) yang berfungsi sebagai sumber clock, tapi masih diperlukan rangkaian tambahan untuk membangkitkan clock tersebut. Rangkaian clock ini merupakan jantung dari rangkaian minimum mikrokontroller AT89C2051, yang terdapat oscilator sebagai pembangkit pulsa pada mikrokontroller AT89C2051, mempunyai input XTAL 1 dan output XTAL 2. Dimana XTAL 1 adalah input yang dihubungkan dengan rangkaian osilasi dalam rangkaian mikrokontroller sedangkan XTAL 2 adalah output feedback untuk osilasi.

Rangkaian ini terdiri dari 2 buah capasitor dan sebuah kristal, dengan ketentuan C1 dan C2 = 20 – 40 pF (digunakan untuk kristal).

= 30 – 50 pF (digunakan untuk keramik resonantor).

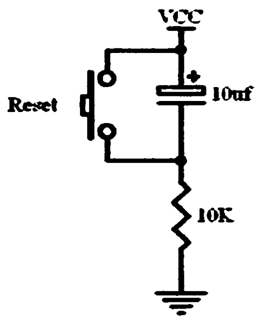


Gambar 3.3
Rangkaian Osilator Clock.

Perencanaan berikut menggunakan kristal 12,000 MHz yang dimaksudkan untuk ketepatan perhitungan besar baud rate pada sistem transmisi data serial sedangkan nilai kapasitor yang digunakan adalah 30 pF sesuai dengan toleransi yang dispesifikasikan. Clock ini menghasilkan suatu interval pewaktu yang dinamakan pulsa, untuk sebuah instruksi program terkecil diperlukan beberapa pulsa yang dikelompokkan dalam bagian keadaan (state) yang dinamakan satu siklus mesin. Sebuah keadaan (state) menunjukan dasar dari interval waktu untuk menandai suatu operasi, seperti penempatan opcode byte, pengerjaan opcode atau penulisan data byte. Jumlah suatu byte opcode telah ditentukan oleh pabrik berdasarkan bentuk perintah, misalkan penggunaan perintah, MOV A, R1, yang mempunyai 1 byte , maka waktu eksekusi suatu program dapat dicari sesuai dengan persamaan sebagai berikut :

$$t_{inst} = \frac{1 \times 12}{12{,}000 \times 10^6} = 1us$$

Rangkaian reset disini digunakan untuk mereset mikrokontroller AT89C2051, yaitu mengawali eksekusi program pada alamat paling rendah. Rangkaian ini direncanakan agar mempunyai kemampuan power on reset, yaitu reset terjadi pada saat power diaktifkan.



Gambar 3.4
Rangkaian Reset.

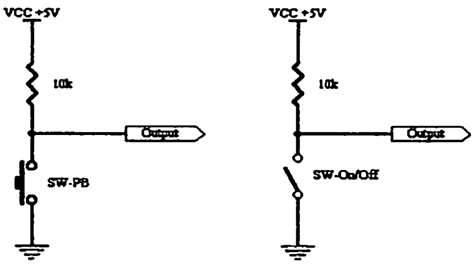
Dengan mengasumsikan lama waktu startup dari oscilasi pada waktu power di-on-kan adalah 10 μs dan kristal yang dipakai pada mikrokontroller adalah 12,000 Mhz. Maka lebar pulsa pada saat rest harus lebih besar dari :

$$T = \frac{2 \times 12}{12{,}000 \times 10^6} + 10 \times 10^{-6} = 12\mu 2$$

Tegangan tipikal dikaki reset adalah setengah dari Vcc yaitu 2,5 V. Untuk memenuhi kriteria diatas dalam perencanaan dipakai nilai R=10 kΩ dan C=10 μF, sehingga waktu pulsa pada reset adalah :

$T_{reset} = 10.10^3 \times 10.10^{-6} = 0{,}1$ s

3.3.2. Rangkaian Pensaklaran Limit Switch



Gambar 3.5
Rangkaian Pensaklaran

Rangkaian Pensaklaran disini terdapat 2 jenis saklar penghubung yaitu switch Puss Button dan Dip switch. Switch Puss Button dan Dip switch berfungsi sebagai media pengoperasian kerja alat dimana akan memberikan 2 kondisi yaitu kondisi terhubung dan kondisi terputus. Dengan menambahkan Resistor yang terhubung dengan Vcc dan salah satu kaki switch terhubung dengan ground maka 2 kondisi terhubung dan terputus pada switch akan diubah pada besaran logic sebagai masukan terhadap mikrokontroler. Untuk mencari nilai resistor yang sesuai dengan kebutuhan maka harus diketahui dahulu karakteristik dari masukan/input mikrokontroler.

Karakteristik Teknis Mikrokontroler :

Vin logic High = 2,0 – 5,0 Volt

Iin logic High = 650 μA Max

(*Sumber DataSheet Microcontroller AT89C2051*)

Dalam rangkaian ini mikrokontroler mendapat logic high dengan tegangan 5 Volt dengan Arus 500μA, maka dapat dicari nilai Resistornya.

$$R = \frac{V}{I} = \frac{5}{0.0005} = 10000\Omega \text{ atau sama dengan } 10K\Omega$$

3.3.3. Rangkaian Driver Motor DC

Di dalam perencanaan rangkaian ini hal utama yang perlu diperhatikan adalah pemilihan media penghubung yang dapat dikontrol melalui suatu rangkaian pengendali. Media penghubung yang digunakan dalam rangkaian ini berupa Relay SPDT (Single Pool Double Terminal) yang merupakan Relay dengan 1 masukan dan 2 keluaran.

Relay yang digunakan merupakan Relay 24 Volt dengan resistansi 168 Ohm. Untuk dapat mengetahui rangkaian ini bekerja sebagai mestinya dipergunakan sebuah LED (Light Emiting Diode) sebagai indikator. Led yang dipergunakan mempunyai arus bias maju (If) sebesar 10 mA dan tegangan sebesar 1,5 Volt. Supaya Led mampu bekerja dan tidak putus maka harus ditambahkan Tahanan yang dihubungkan secara seri.

$$Rled = \frac{Vcc - Vled - Vce(sat)}{If}$$

$$Rled = \frac{24 - 1.5 - 0.2V}{0.010A}$$

$$Rled = 2230\ \Omega \text{ atau yang ada tersedia 2K2}$$

Transistor BJT (Bipolar Juntion Transistor) yang harus mempunyai arus kolektor sebesar 68,8 mA untuk kondisi Saturasi (Jenuh).

Transistor yang dipilih merupakan karakteristik ßdc lebih dari 64, hal ini dikarenakan agar tidak terlalu kritis.

Transistor yang kita pilih merupakan transistor sederhana type NPN yang mempunyai ßdc 110. Selama transistor tersebut dapat menghubungkan Relay dan mempunyai rating tegangan lebih dari 24 Volt, type yang biasa digunakan adalah BD139. Diode yang dihubungkan melintasi Relay disini dimaksudkan untuk melindungi transistor dari bahaya tegangan balik EMF 'Spikes' pada kondisi transisi. Pada saat koil Relay mempunyai induktansi yang besar yang dapat secara mudah menyebabkan Spikes yang mungkin akan merusak transistor, maka dari itu untuk menghindari kerusakan pada transistor digunakan Diode.

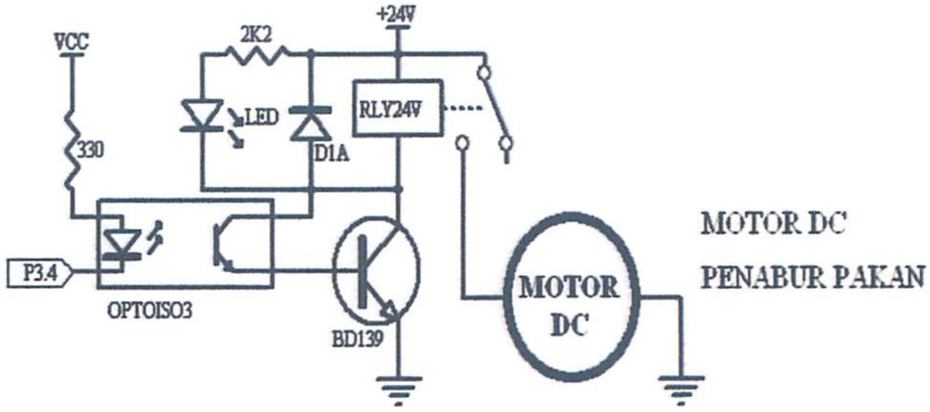
Hubungan antara rangkaian driver dengan mikrokontroller AT89C2051 terdapat OptoCoupler. Disini OptoCoupler dimaksudkan agar logic kendali dari mikrokontroller aman dari gangguan tegangan yang besar dari rangkaian driver. Logic dari mikrokontroller untuk mengendalikan rangkaian driver terhubung dengan Led IR pada OptoCoupler. Jadi agar rangkaian driver motor dapat bekerja maka mikrokontroller cukup menghidupkan Led IR di dalam OptoCoupler. Untuk menghidupkan Led IR pada OptoCoupler maka perlu digunakan resistor guna membatasi arus yang mengalir pada Led IR. Berikut adalah perhitungan guna mencari nilai resistansi untuk menyalakan Led IR.

$$ILed = 10 - 15mA$$

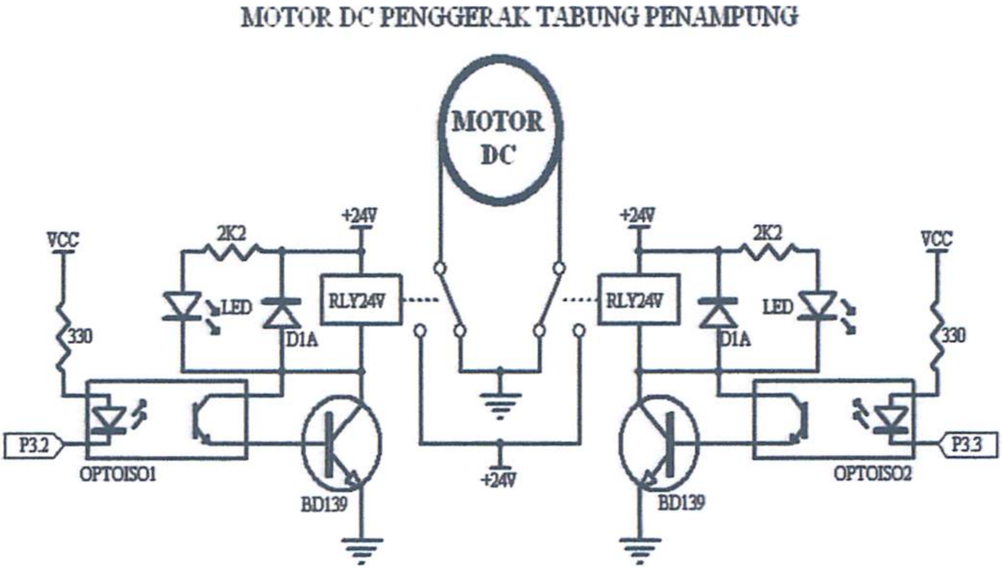
$$Rled = \frac{Vcc - Vled}{If}$$

$$Rled = \frac{5 - 1.5}{0.010A}$$

$$Rled = 350\ \Omega \text{ atau yang tersedia dipasaran } 330\Omega$$



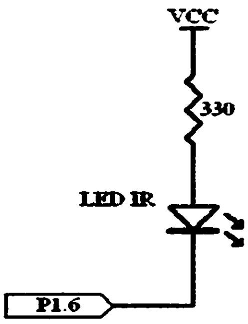
Gambar 3.6
Rangkaian Driver Motor DC Penabur Pakan



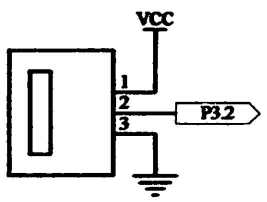
Gambar 3.7
Rangkaian Driver Motor DC Penggerak Tabung Penampung

3.4. Modul Infra Red (Pemancar Dan Penerima)

Modul pemancar dan penerima gelombang infra merah di tunjukan pada gambar 3.8. Penerima IR mengunakan GP 1 U 52x karena banyak tersedia di pasaran. Komponen ini akan menghasilkan logika 0 pada keluarannya jika terdeteksi adanya sinyal infra red dan sebaliknya akan berlogika 1 jika tidak terdeteksi sinyal infrared 40 kHz. Sedangkan bagian pemancar menggunakan LED IR yang terhubung dengan pin mikrokontroller. Pin output yang terhubung dengan LED IR akan mengeluarkan logic frekuensi 40Khz untuk dipancarkan ke Module IR receiver.



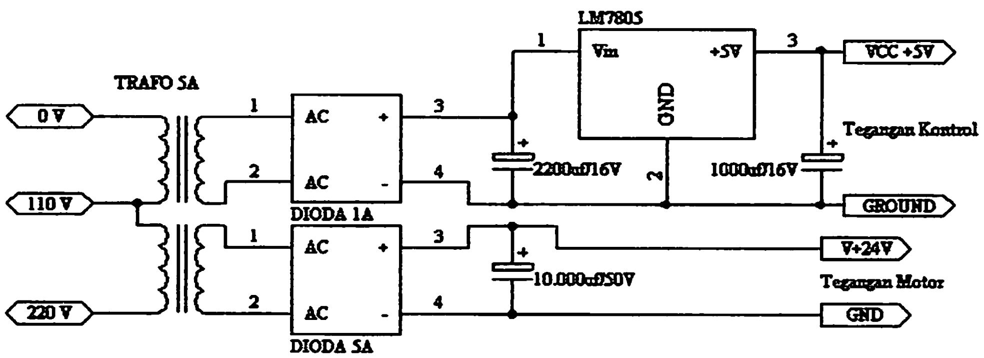
Gambar 3.8
LED IR



Gambar 3.9
Module Sensor IR Receiver

3.5. Catu Daya Rangkaian

Catu Daya Rangkaian disini menggunakan transformator 5Ampere dimana transformator digunakan untuk sunber tegangan Rangkaian Kontrol dan untuk sumber tegangan penggerak Motor DC. Pada tranformator mempunyai 2 belitan sekunder, yaitu dengan arus maksimal 500 mA dan arus maksimal 5A. sekunder dengan arus 500mA digunakan untuk sumber tegangan rangkaian control, sedangkan sekunder dengan arus 5A digunakan untuk sumber tegangan penggerak Motor DC. Pemisahan tegangan antara rangkaian control dan penggerak Motor DC dimaksudkan agar tidak terjadinya gangguan tegangan pada rangkaian control yang diakibatkan oleh kerja Motor DC. Berikut ini adalah gambar perancangan rangkaian power supplay yang dibuat.



Gambar 3.10
Rangkaian Catu Daya

3.6. Perancangan Software

Software merupakan perintah program yang akan dijalankan oleh MCU untuk mengendalikan proses kerja alat tersebut. Software atau program tersebut akan dimasukkan ke dalam EEPROM internal mikrokontroller AT89C2051 dan akan mengontrol Motor DC untuk berputar kekiri maupun kekanan baik motor penabur pakan dan motor penggerak tabung penampung serta proses proses input output untuk sensor infra merah. Software yang digunakan untuk menjalankan alat adalah bahasa pemrograman Assembler.

3.6.1. Struktur Dasar Bahasa Assembler

Struktur dasar bahasa assembler menganut satu baris untuk satu perintah seperti :Proses: MOV AX,BX ; Menyalin isi register BX kedalam register AX.

Proses adalah bagian label, MOV adalah bagian mnemonic, AX dan BX adalah bagian operand (AX yang berada disebelahkiri disebut operand tujuan atau Destination operand sedangkan BX yang berada disebelah kanan disebut operand sumber atau Source Operand hal ini berlaku untuk semua jenis operand yang lebih dari satu), sedangkan kalimat yang ada dibelakang tanda ';' adalah bagian komentar.

Bagian mnemonic merupakan singkatan perintah yang mudah diingat, bagian ini adalah bagian yang menginstruksikan suatu program untuk bekerja sesuai dengan perintah yang ditulisnya.

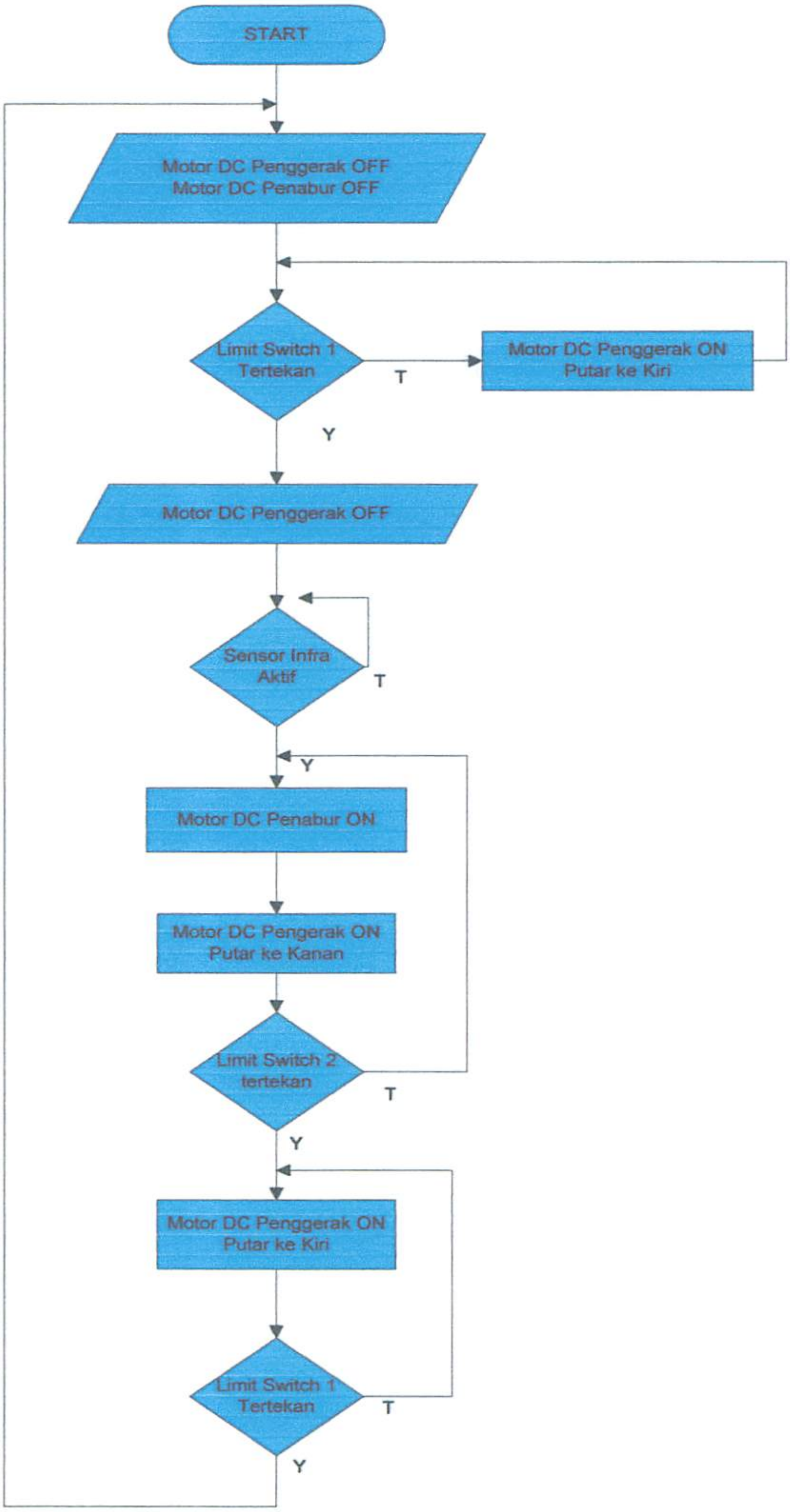
Bagian operand adalah bagian yang merupakan objek dari sebuah instruksi atau bagian yang harus dieksekusi oleh program assembler sesuai dengan perintah dari bagian mnemonic.

Bagian komentar tidak berpengaruh pada jalannya program assembler, tetapi sangat penting untuk mempermudah seseorang mengerti maksud dari program yang dibuatnya sehingga orang tersebut tahu akan guna dari sebuah instruksi.

3.6.2. Cara MengCompile Program Assembler

Untuk mengkompile sebuah program dengan bahasa Assembler diperlukan sebuah compiler yang disebut ASM51.EXE, yang akan membuat source code dengan file berektensi .A51 yang telah kita isi dengan program dengan bahasa assembler menjadi sebuah file dengan ekstensi .BIN. setelah itu file program berekstensi BIN akan dikompile lagi ke file berekstensi List, Hex. File yang nantinya akan di isikan kedalam mikrokontroller adalah file program yang berekstensi Hex melalui program Downloader.

3.7. FlowChart Sistem Kerja Alat



BAB IV

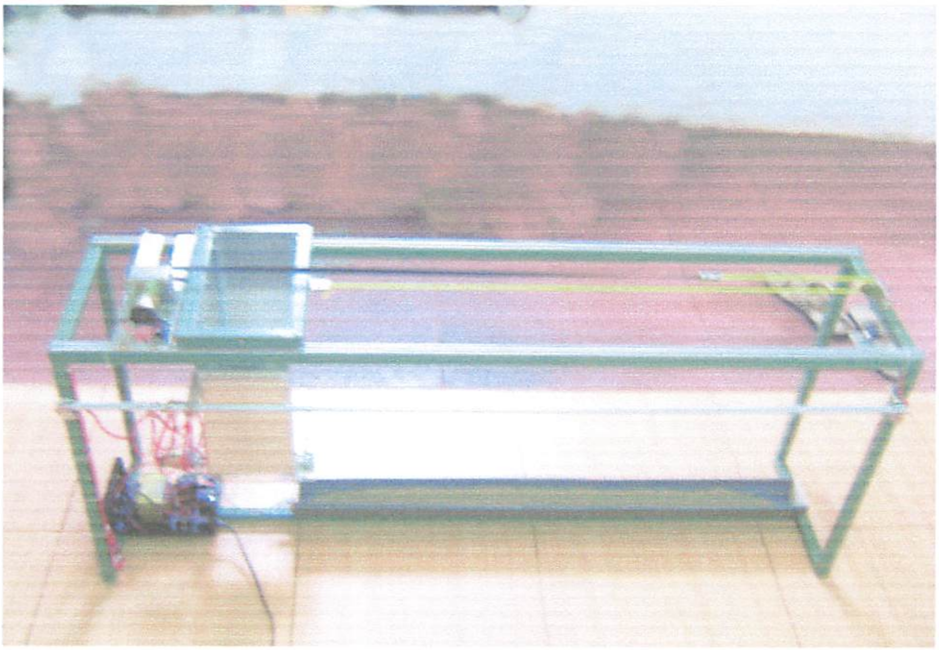
PENGUJIAN DAN PERCOBAAN

4.1. Pengujian Kerja Alat

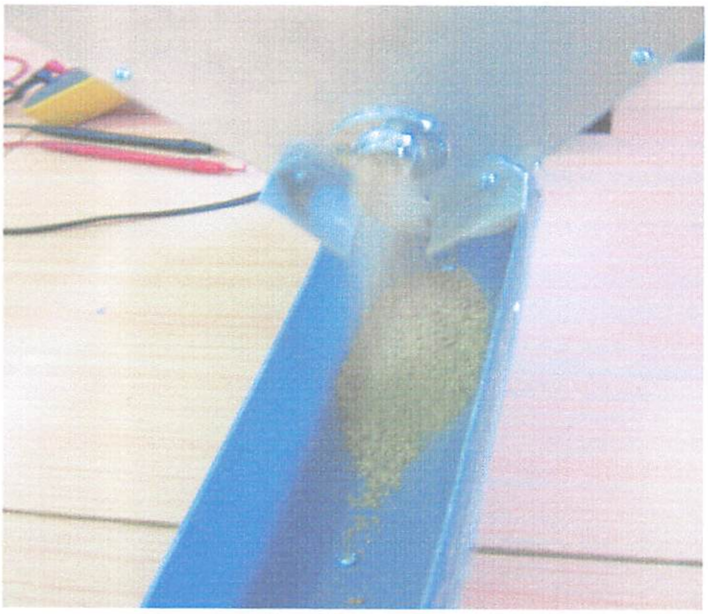
Untuk mengetahui bahwa mekanik mesin penabur pakan ternak telah berjalan dengan baik atau tidak, maka kita perlu melakukan pengujian. Yang mana pengujian ini dilakukan pada beberapa tahapan sebelum dilakukan pengujian secara keseluruhan.

Pengujian hardware bertujuan untuk mengetahui kinerja sistem yang telah dirancang berjalan sesuai dengan perencanaan dan analisa. Pada bab ini akan dibahas secara keseluruhan tahap-tahap dari pengujian hardware yang telah terintegrasi menjadi satu sistem control. Pada proses pengukuran hardware yang telah menjadi satu system control ini menggunakan multimeter digital untuk melihat tegangan dan pemakaian arus yang dihasilkan oleh setiap blok kontrol. Dalam pengujian hardware ini meliputi :

1. Pengujian Power Supply.
2. Pengujian Driver Motor.
3. Pengujian Sensor Infra Merah.
4. Pengujian Limit Switch Posisi Tabung Penampung
5. Pengujian Sistem dan Kerja Alat.



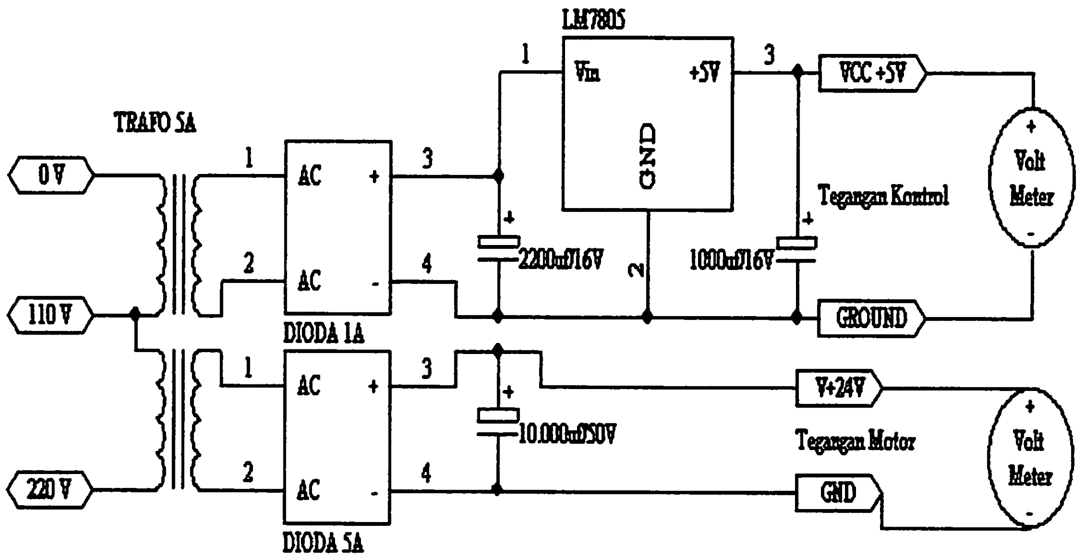
Gambar 4.1
Foto Alat Keseluruhan



Gambar 4.2
Foto Kondisi Alat Sedang Bekerja

4.1.1. Pengujian Power Supply.

Sebelum kita melakukan pengujian hasil secara keseluruhan, kita perlu melakukan pengetesan hardware terlebih dahulu. Hal ini bertujuan untuk menghindari terjadi kesalahan pada hasil data yang diproses nantinya. Pengujian hardware dilakukan sesuai urutan dari pada blok diagramnya. Yang pertama adalah memastikan bahwa supply PLN bertegangan 220 Volt. Kedua yaitu memastikan rectifier dan DC power supplay input dan output hasilnya seperti pada table 4.1. dengan ketentuan ini didapatkan hasil pengujian DC power supplay seperti berikut ini :



Gambar 4.3
Pengujian Power Supplay

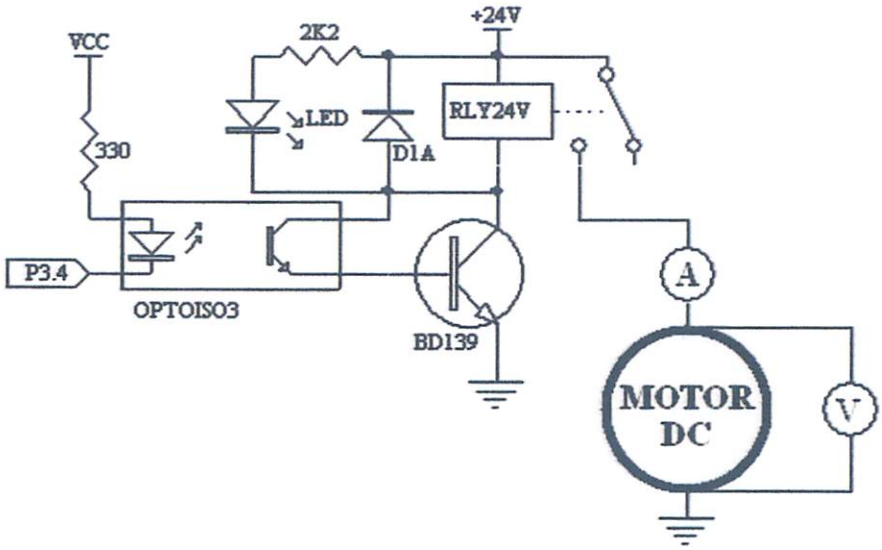
Tabel 4.1
Hasil Pengujian Power Supply pada Alat

Kondisi Alat	Catu Daya 5V Regulator LM7805	Catu Daya 24V
Standby	5,01	24,90
Motor Penggeser ON Motor Penabur OFF	4,99 4,99	24,50 24,49
Motor Penggeser ON Motor Penabur ON	4,99 4,99	24,25 24,20

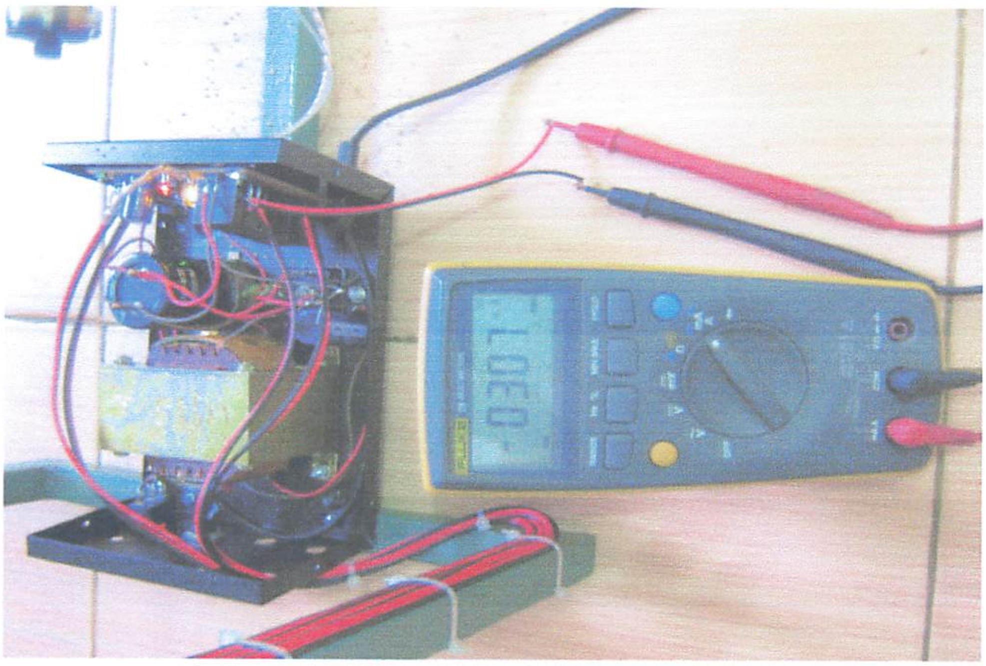
Dari pengujian power supplay pada table 4.1 dapat dianalisa bahwa untuk tegangan yang diinginkan sesuai dengan yang diharapkan. Untuk tegangan 24 V di gunakan untuk motor, sedangkan tegangan 5 V adalah untuk minimum sistem.

4.1.2. Pengujian Driver Motor

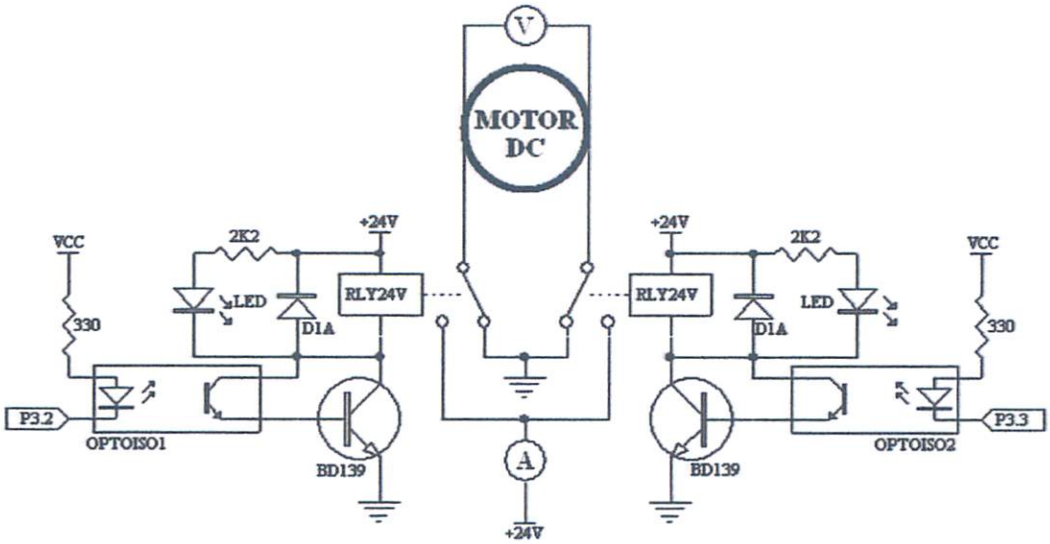
Penggerak mekanik penabur pakan ternak otomatis disini adalah motor DC GearBox 24V. Pengujian motor DC dilakukan dengan mengukur tegangan kerja motor DC serta mengamati pemakaian arus yang dibutuhkan. Selain itu juga mengukur kecepatan putar pada masing-masing motor DC. Pada pengujian berikut ini dilakukan pengukuran besaran tegangan dan arus pada motor DC terhadap tegangan 24V DC.



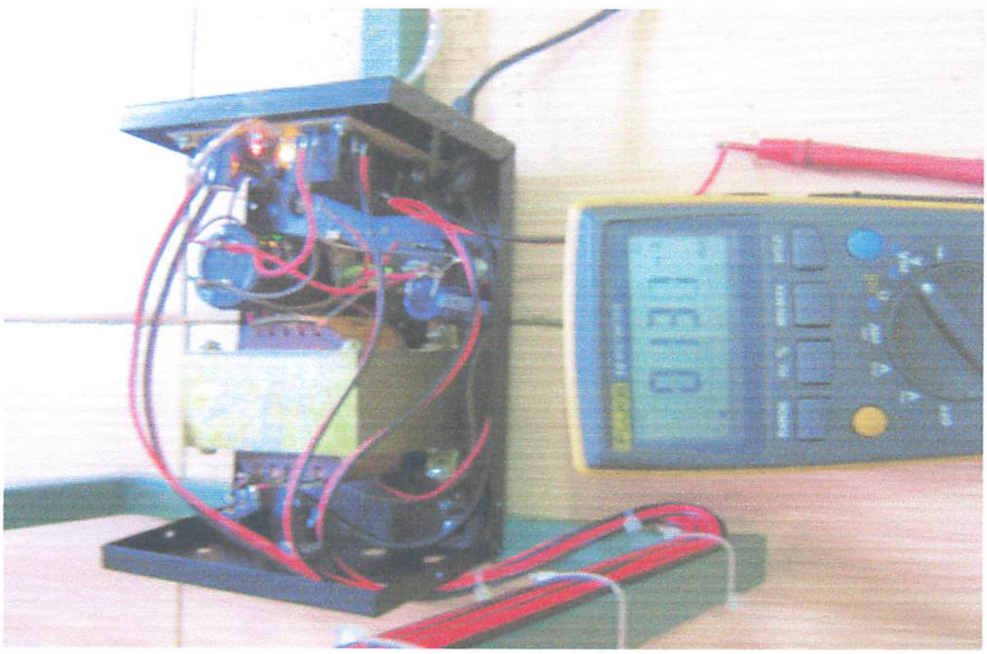
Gambar 4.4
Pengujian Rangkaian Driver Motor Penabur Pakan



Gambar 4.5
Foto Pengujian Arus Kerja Motor Penabur Pakan



Gambar 4.6
Pengujian Motor DC Penggerak Tabung Penampung



Gambar 4.7
Foto Pengujian Arus Kerja Motor Penggerak Tabung Pakan

Tabel 4.2
Data Pengujian Driver Motor

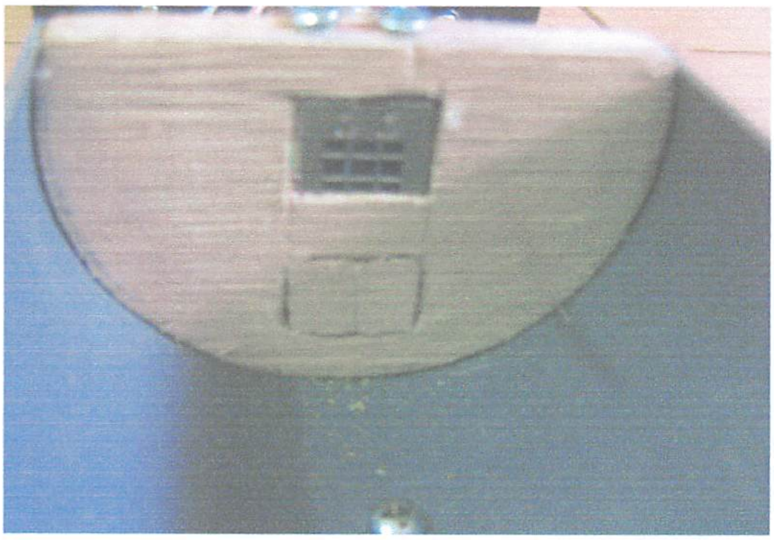
Motor DC GearBox	Tegangan Kerja	Arus Pemakaian
Motor Penabur Pakan ON	24V	0,307A
Motor Penggerak Tabung Putar Kanan	24V	0,130A
Motor Penggerak Tabung Putar Kiri	24V	0,131A

4.1.3. Pengujian Sensor Infra merah

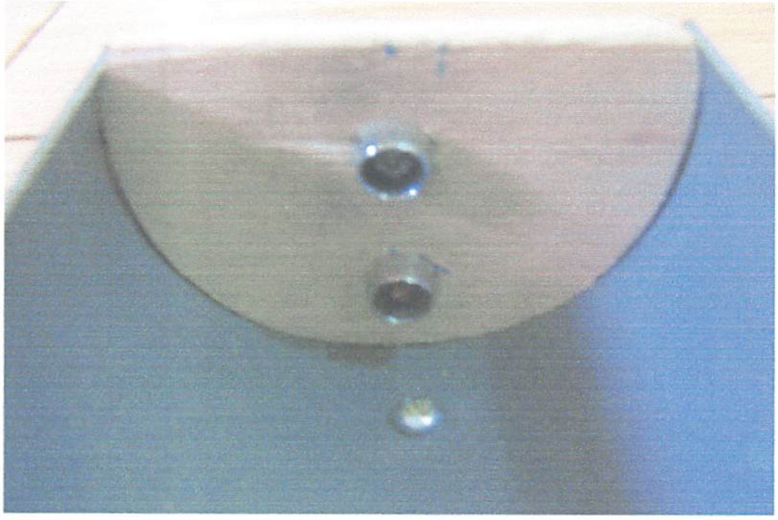
Pengujian sensor ini dilakukan untuk mengetahui tegangan keluaran dari module infra merah apakah bekerja dengan baik atau tidak. Pengujian sensor ini dilakukan dengan cara menghubungkan output module infra merah dengan multimeter. Output module infra merah mendapatkan input berupa cahaya infra merah. Jika module IR mendapatkan sinar infra merah maka outputnya akan berlogika Low (0). Dan sebaliknya jika tidak mendapatkan sinar infra merah maka outputnya akan berlogika High (1). Perubahan logic inilah yang nantinya akan dibaca oleh mikrokontroller untuk menggerakkan alat. Hasil pengujian untuk kinerja dari module infra merah terlihat pada table sebagai berikut :

Tabel 4.3
Pengujian pada module Infra Merah

Kondisi	Tegangan Keluaran
Terbuka Pakan Habis	0,03 Volt
Tertutup Pakan Penuh	2,50 Volt



Gambar 4.8
Foto Posisi Module Sensor Infra Red Pada Alat



Gambar 4.9
Foto Posisi Led Infra Merah Pada Alat

Dari hasil pengujian module infra merah menunjukkan bahwa module IR bekerja dengan baik, dimana terlihat bahwa ketika module IR mendapatkan sinar infra merah maka tegangan keluaran yang dihasilkan adalah *0 volt,* dan ketika tidak mendapatkan sinar infra merah maka tegangan keluaran yang dihasilkan adalah *5 volt.*

4.1.4. Pengujian Limit Switch

Pengujian sensor *Limit switch* pada posisi tabung penampung dilakukan dengan menggunakan Avo meter digital dengan tujuan mengetahui apakah sensor ini dapat mendeteksi posisi tabung sudah berada pada posisi maksimum dikanan dan posisi maksimum di kiri. Berikut adalah data pengujian kondisi limit switch tertekan dan tidak tertekan.

Tabel 4.4
Data limit switch pada posisi tabung penampung

Kondisi	Volt
Tertekan	0,0 V
Tidak tertekan	4.95 V

Setelah dilakukan beberapa kali pengujian didapat data seperti pada tabel. Pada saat sensor Limit tertekan oleh tabung penampung pakan maka kondisi tegangan output adalah 0,0V atau logik Low, dan jika sensor limit switch tidak tertekan maka kondisi tegangan adalah 4,95V atau logik High. Perubahan tegangan keluaran inilah yang akan diproses oleh mikrokontroller sebagai tanda posisi tabung penampung pakan sudah maksimal atau belum.

BAB V

PENUTUP

5.1. Kesimpulan

1. Motor DC GearBox sebagai penggerak mekanik alat mempunyai kekuatan yang lebih dari cukup untuk menggerakan tabung penampung pakan serta menggerakkan penabur pakan.
2. Sensor Infra Merah mampu bekerja dengan baik pada jarak 1 Meter hingga 6 Meter.
3. Pemakaian trafo 5A pada rangkaian catu daya telah sesuai dan mencukupi untuk konsumsi daya rangkaian. Hal ini didasarkan pada analisa pengukuran arus rangkaian.
4. Waktu pengisian tempat pakan sampai penuh adalah 2 menit 56 detik.
5. Tempat penampung pakan dapat menampung sebanyak 1,2 kg sekali pengisian.

5.2. Saran – Saran

Kami selaku penyusun sangat mengharapkan alat penabur pakan ternak otomatis ini dapat berguna dan meringankan pekerjaan manusia, yang dewasa ini semakin di tuntut keefisiensinya dalam lingkup kehidupan. Semoga alat ini dapat memberikan keuntungan bagi penggunanya.

Untuk pengembangan peningkatan kemampuan alat ini pengguna dapat melakukan hal-hal sebagai berikut :

- Kecepatan motor DC penabur pakan dapat di tingkatkan sehingga pakan yang keluar dari tabung penampung lebih banyak dan lebih cepat.
- Kapasitan tabung penampung pakan dapat diperbesar.
- Panjang tempat pakan ternak ditambah menyesuaikan dengan banyak ternak.

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2. Albert Paul Malvino, Ph.D./ Hanapi Gunawan, **Prinsip-Prinsip Elektronika,** Penerbit Erlangga, 1996
3. Data Sheet Atmel Corporation **AT89C2051** : 8-bit Microcontroler with 2 K byte flash 2000.
4. www.elektroindonesia.com
5. www.komunikasi elektronika.com

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III

LEMBAR ASISTENSI BIMBINGAN TUGAS AKHIR

Nama : **Harli Ariandono**
Nim : **05 52 017**
Waktu Bimbingan : **26/11/2008 s/d 26/03/2009**
Judul : **Alat Penabur Pakan Ternak Otomatis Dengan Penggerak Motor DC Berbasis Mikrokonroller AT89C2051**

No	Tanggal	Materi	Paraf
1			
2			
3			
4			
5			
6			
7			
8			
9		Acc maju ujian	
10			
11			
12			
13			
14			
15			

Malang,7 Maret 2009

Mengetahui
Dosen Pembimbing

(Bambang Prio Hartono,ST, MT)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO D-III
PROGRAM STUDI TEKNIK LISTRIK
MALANG

LEMBAR PERBAIKAN TUGAS AKHIR

Telah dilakukan perbaikan oleh :

Nama : Harli Ariandono

NIM : 05.52.017

Jurusan : Teknik Elektro D-III.

Program Studi : Teknik Listrik D-III.

Hari/Tanggal : Selasa / 24 Maret 2009

No.	Materi Perbaikan	Paraf
1.	Cantumkan hasil (waktu) untuk pengisian pakan sampai penuh	

Telah Diperiksa/Disetujui:

Anggota Penguji I

Ir. Eko Nurcahyo
NIP. Y. 1028700172

Anggota Penguji II

Ir. M. Abdul Hamid, MT
NIP. Y. 103 97 00309

Mengetahui :
Dosen Pembimbing

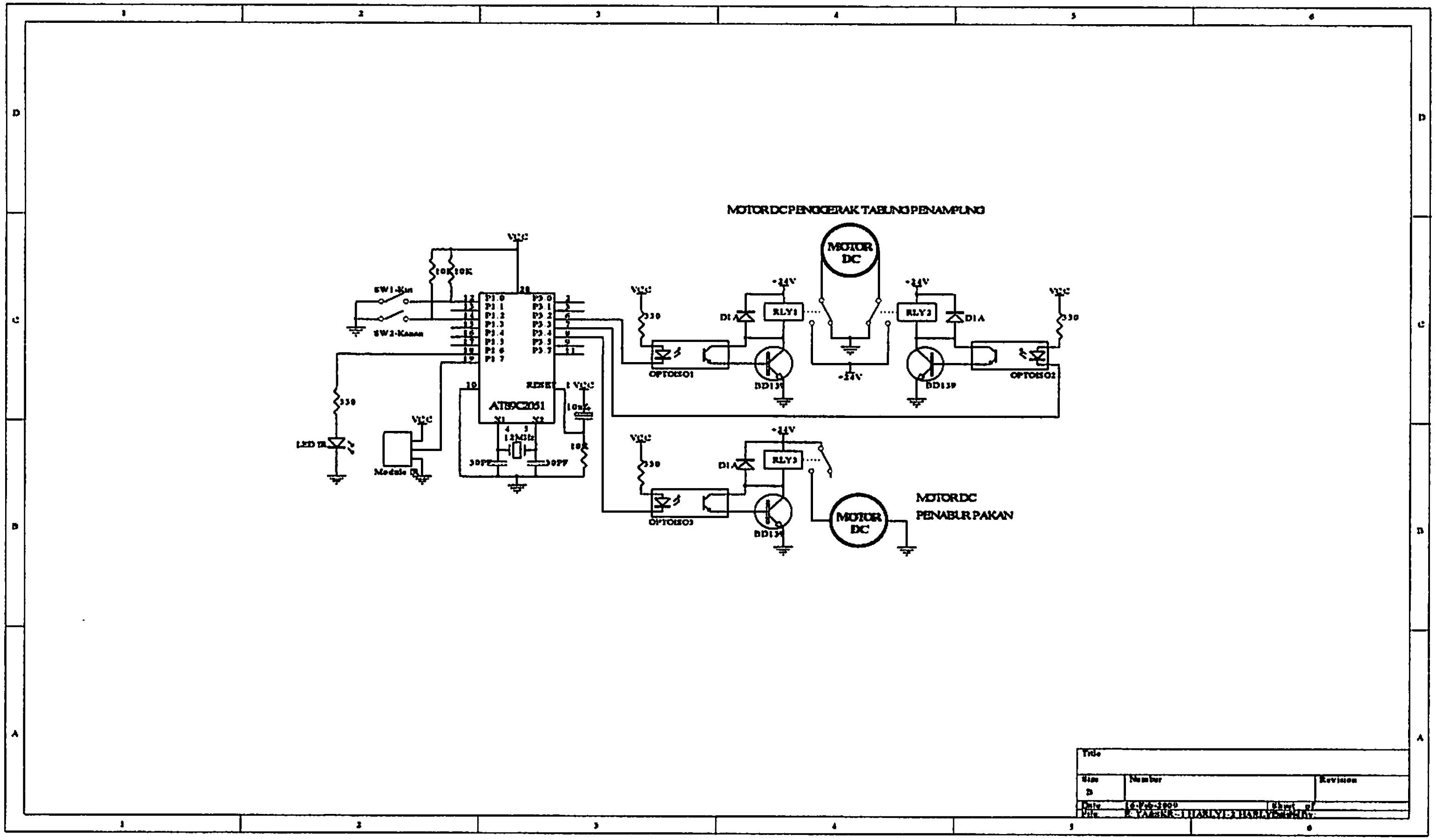
Bambang Prio Hartono, MT
NIP. Y. 102 84 00082

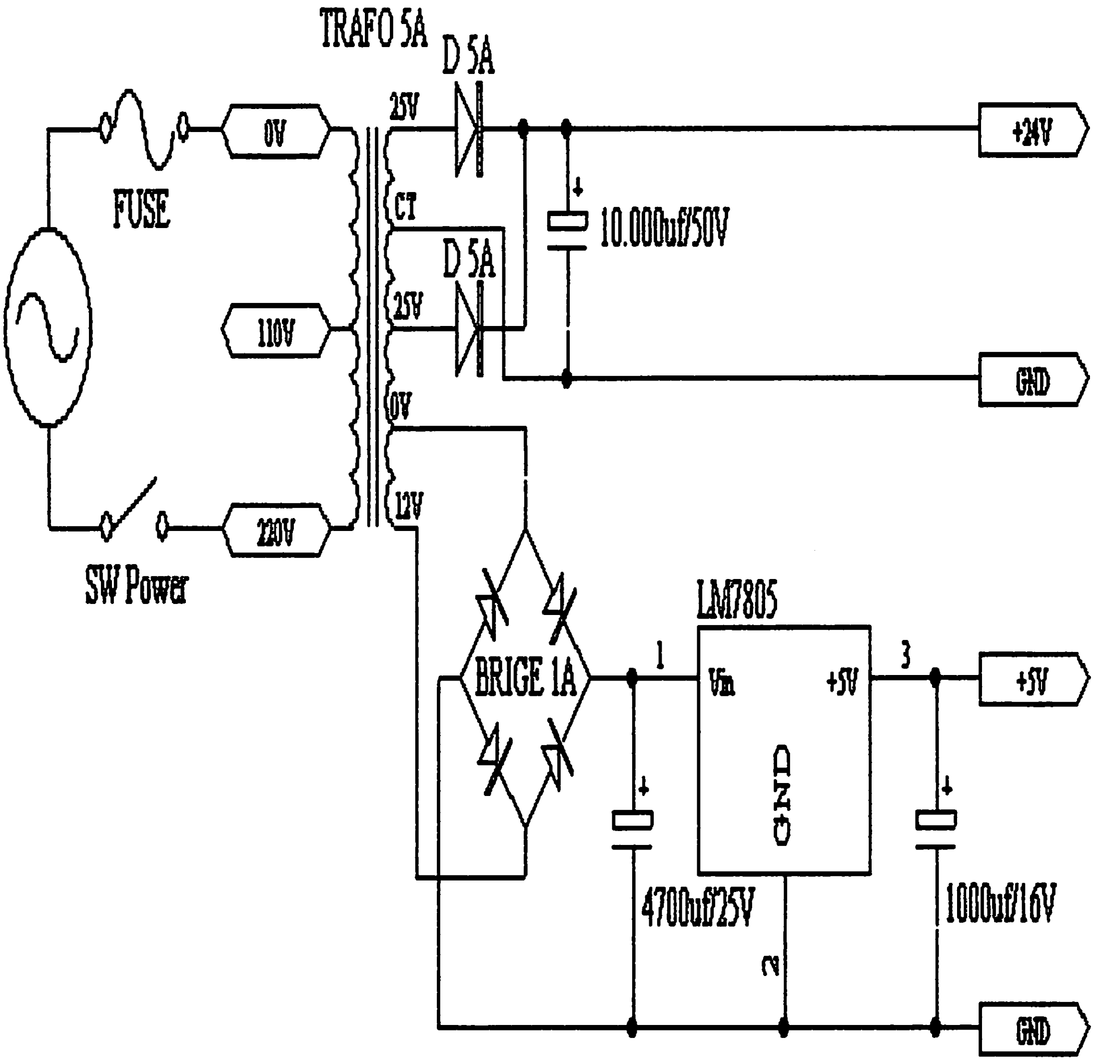
Lampiran

PROGRAM AT89C2051

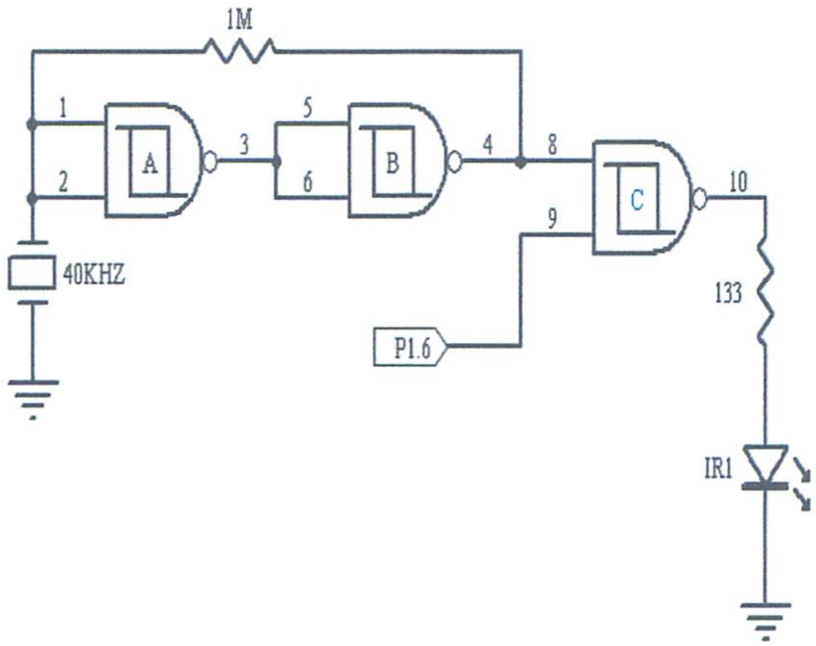
```
        Org     0000h

Mulai:  Setb    P3.2            ;Motor Penggerak Tabung Kiri OFF
        Setb    P3.3            ;Motor Penggerak Tabung Kanan OFF
        Setb    P3.4            ;Motor Penabur Pakan OFF
Mli1:   Jb      P1.2,Mli2       ;Periksa Posisi Tabung Di Kiri (Limit Switch 1)
        Sjmp    Mli3
Mli2:   Clr     P3.2            ;Motor Penggerak Tabung ON Kekiri
        Sjmp    Mli1
Mli3:   Setb    P3.2
        Setb    P3.3
        Setb    P3.4
        Setb    P1.7
        Clr     P1.7            ;Aktifkan Sensor
        Mov     R7,#02h
Mli4:   Mov     R6,#0FFh
Mli5:   Mov     R5,#0FFh
Mli6:   Jnb     P3.5,mli7       ;Baca Sensor
        Sjmp    Mli8
Mli7:   Djnz    R5,Mli6
```

```
        Djnz  R6,Mli5
        Djnz  R7,Mli4
        Sjmp  Mli3
Mli8:   Setb  P3.2
        Clr   P3.3         ;Motor Penggerak ON Kekanan
        Clr   P3.4         ;Motor Penabur ON Keluarkan Pakan
        Jb    P1.5,Mli8    ;Periksa Posisi Tabung Dikanan (Limit Switch 2)
        Setb  P3.2
        Setb  P3.3
Mli9:   Clr   P3.2         ;Motor Penggerak ON Kekiri
        Setb  P3.3
        Clr   P3.4
        Jb    P1.2,Mli9    Periksa Posisi Tabung Dikiri (Limit Switch 1)
        Sjmp  Mulai
```


MOTOR DC PENGGERAK TABUNG PENAMPUNG
MOTOR DC
AT89C2051
SW1-Kiri
SW2-Kanan
10K
10K
VCC
330
LED IR
Module IR
12MHz
30PF
30PF
10uF
10K
RESET
OPTOISO1
OPTOISO2
OPTOISO3
D1A
RLY1
RLY2
RLY3
BD139
+24V
MOTOR DC
PENABUR PAKAN
Title
Size
B
Number
Revision
Date
Sheet of
File



Rangkaian Power Supplay



Rangkaian Infra Merah

Features

- **Compatible with MCS-51™ Products**
- **2K Bytes of Reprogrammable Flash Memory**
  - **Endurance: 1,000 Write/Erase Cycles**
- **2.7V to 6V Operating Range**
- **Fully Static Operation: 0 Hz to 24 MHz**
- **Two-Level Program Memory Lock**
- **128 x 8-Bit Internal RAM**
- **15 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **Six Interrupt Sources**
- **Programmable Serial UART Channel**
- **Direct LED Drive Outputs**
- **On-Chip Analog Comparator**
- **Low Power Idle and Power Down Modes**

8-Bit Microcontroller with 2K Bytes Flash

AT89C2051

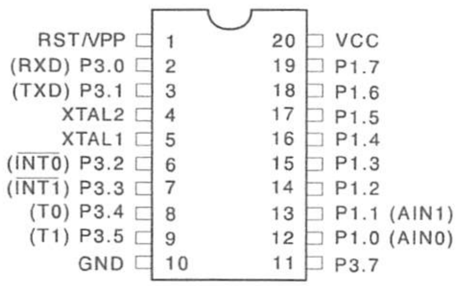
Description

The AT89C2051 is a low-voltage, high-performance CMOS 8-bit microcomputer with 2K Bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C2051 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

The AT89C2051 provides the following standard features: 2K Bytes of Flash, 128 bytes of RAM, 15 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, a precision analog comparator, on-chip oscillator and clock circuitry. In addition, the AT89C2051 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

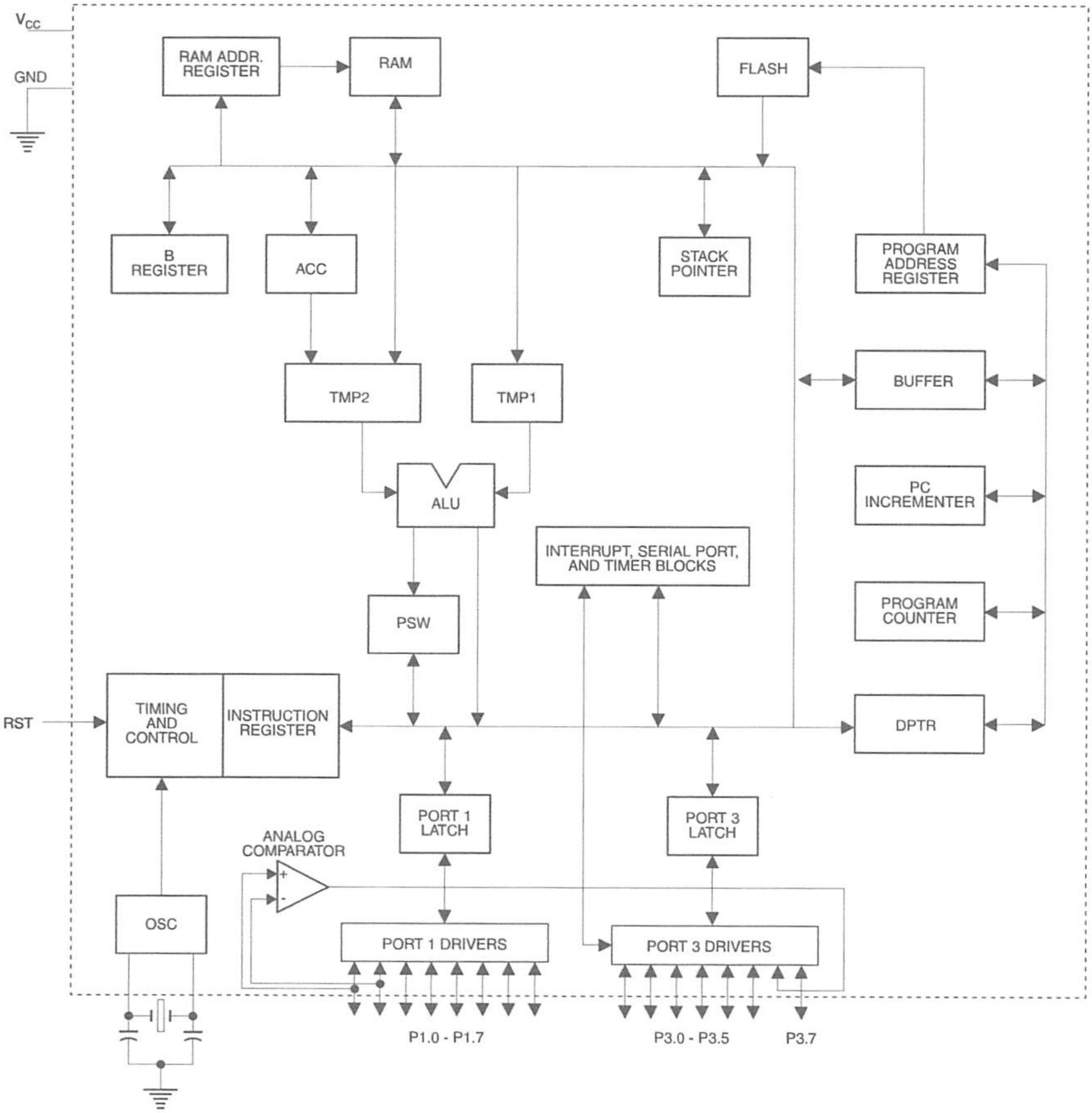
Pin Configuration

PDIP/SOIC



0368D-B–12/97

Block Diagram



Pin Description

V_{CC}

Supply voltage.

GND

Ground.

Port 1

Port 1 is an 8-bit bidirectional I/O port. Port pins P1.2 to P1.7 provide internal pullups. P1.0 and P1.1 require external pullups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. The Port 1 output buffers can sink 20 mA and can drive LED displays directly. When 1s are written to Port 1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs and are externally pulled low, they will source current (I_{IL}) because of the internal pullups.

Port 1 also receives code data during Flash programming and verification.

Port 3

Port 3 pins P3.0 to P3.5, P3.7 are seven bidirectional I/O pins with internal pullups. P3.6 is hard-wired as an input to the output of the on-chip comparator and is not accessible as a general purpose I/O pin. The Port 3 output buffers can sink 20 mA. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C2051 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. All I/O pins are reset to 1s as soon as RST goes high. Holding the RST pin high for two machine cycles while the oscillator is running resets the device.

Each machine cycle takes 12 oscillator or clock cycles.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

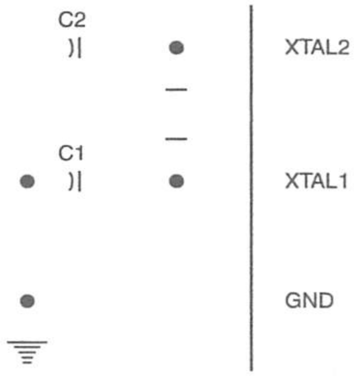
XTAL2

Output from the inverting oscillator amplifier.

Oscillator Characteristics

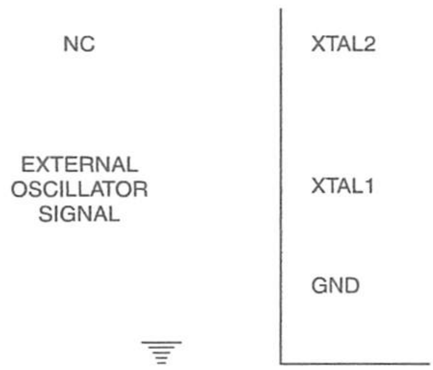
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in the table below.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Table 1. AT89C2051 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H									0CFH
0C0H									0C7H
0B8H	IP XXX00000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0XX00000								0AFH
0A0H									0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H		SP 00000111	DPL 00000000	DPH 00000000				PCON 0XXX0000	87H

Restrictions on Certain Instructions

The AT89C2051 and is an economical and cost-effective member of Atmel's growing family of microcontrollers. It contains 2K bytes of flash program memory. It is fully compatible with the MCS-51 architecture, and can be programmed using the MCS-51 instruction set. However, there are a few considerations one must keep in mind when utilizing certain instructions to program this device.

All the instructions related to jumping or branching should be restricted such that the destination address falls within the physical program memory space of the device, which is 2K for the AT89C2051. This should be the responsibility of the software programmer. For example, LJMP 7E0H would be a valid instruction for the AT89C2051 (with 2K of memory), whereas LJMP 900H would not.

1. Branching instructions:
LCALL, LJMP, ACALL, AJMP, SJMP, JMP @A+DPTR

These unconditional branching instructions will execute correctly as long as the programmer keeps in mind that the destination branching address must fall within the physical boundaries of the program memory size (locations 00H to 7FFH for the 89C2051). Violating the physical space limits may cause unknown program behavior.

CJNE [...], DJNZ [...], JB, JNB, JC, JNC, JBC, JZ, JNZ With these conditional branching instructions the same rule above applies. Again, violating the memory boundaries may cause erratic execution.

For applications involving interrupts the normal interrupt service routine address locations of the 80C51 family architecture have been preserved.

2. MOVX-related instructions, Data Memory:
The AT89C2051 contains 128 bytes of internal data memory. Thus, in the AT89C2051 the stack depth is limited to 128 bytes, the amount of available RAM. External DATA memory access is not supported in this device, nor is external PROGRAM memory execution. Therefore, no MOVX [...] instructions should be included in the program.

A typical 80C51 assembler will still assemble instructions, even if they are written in violation of the restrictions mentioned above. It is the responsibility of the controller user to know the physical features and limitations of the device being used and adjust the instructions used correspondingly.

Program Memory Lock Bits

On the chip are two lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

Lock Bit Protection Modes[1]

Program Lock Bits			
	LB1	LB2	Protection Type
1	U	U	No program lock features.
2	P	U	Further programming of the Flash is disabled.
3	P	P	Same as mode 2, also verify is disabled.

Note: 1. The Lock Bits can only be erased with the Chip Erase operation.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

P1.0 and P1.1 should be set to '0' if no external pullups are used, or set to '1' if external pullups are used.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

P1.0 and P1.1 should be set to '0' if no external pullups are used, or set to '1' if external pullups are used.

Programming The Flash

The AT89C2051 is shipped with the 2K bytes of on-chip PEROM code memory array in the erased state (i.e., contents = FFH) and ready to be programmed. The code memory array is programmed one byte at a time. *Once the array is programmed, to re-program any non-blank byte, the entire memory array needs to be erased electrically.*

Internal Address Counter: The AT89C2051 contains an internal PEROM address counter which is always reset to 000H on the rising edge of RST and is advanced by applying a positive going pulse to pin XTAL1.

Programming Algorithm: To program the AT89C2051, the following sequence is recommended.

1. Power-up sequence:
   Apply power between V_{CC} and GND pins
   Set RST and XTAL1 to GND
2. Set pin RST to 'H'
   Set pin P3.2 to 'H'
3. Apply the appropriate combination of 'H' or 'L' logic levels to pins P3.3, P3.4, P3.5, P3.7 to select one of the programming operations shown in the PEROM Programming Modes table.

To Program and Verify the Array:

4. Apply data for Code byte at location 000H to P1.0 to P1.7.
5. Raise RST to 12V to enable programming.
6. Pulse P3.2 once to program a byte in the PEROM array or the lock bits. The byte-write cycle is self-timed and typically takes 1.2 ms.
7. To verify the programmed data, lower RST from 12V to logic 'H' level and set pins P3.3 to P3.7 to the appropiate levels. Output data can be read at the port P1 pins.
8. To program a byte at the next address location, pulse XTAL1 pin once to advance the internal address counter. Apply new data to the port P1 pins.
9. Repeat steps 5 through 8, changing data and advancing the address counter for the entire 2K bytes array or until the end of the object file is reached.
10. Power-off sequence:
    set XTAL1 to 'L'
    set RST to 'L'
    Turn V_{CC} power off

$\overline{\text{Data}}$ Polling: The AT89C2051 features $\overline{\text{Data}}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P1.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The Progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. Pin P3.1 is pulled low after P3.2 goes High during programming to indicate BUSY. P3.1 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed code data can be read back via the data lines for verification:

1. Reset the internal address counter to 000H by bringing RST from 'L' to 'H'.
2. Apply the appropriate control signals for Read Code data and read the output data at the port P1 pins.
3. Pulse pin XTAL1 once to advance the internal address counter.
4. Read the next code data byte at the port P1 pins.
5. Repeat steps 3 and 4 until the entire array is read.

The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire PEROM array (2K bytes) and the two Lock Bits are erased electrically by using the proper combination of control signals and by holding P3.2 low for 10 ms. The code array is written with all "1"s in the Chip Erase operation and must be executed before any non-blank memory byte can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 001H, and 002H, except that P3.5 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(001H) = 21H indicates 89C2051

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST/VPP	P3.2/$\overline{\text{PROG}}$	P3.3	P3.4	P3.5	P3.7
Write Code Data(1)(3)		12V		L	H	H	H
Read Code Data(1)		H	H	L	L	H	H
Write Lock	Bit - 1	12V		H	H	H	H
	Bit - 2	12V		H	H	L	L
Chip Erase		12V	(2)	H	L	L	L
Read Signature Byte		H	H	L	L	L	L

Notes: 1. The internal PEROM address counter is reset to 000H on the rising edge of RST and is advanced by a positive pulse at XTAL 1 pin.

2. Chip Erase requires a 10-ms $\overline{\text{PROG}}$ pulse.

3. P3.1 is pulled Low during programming to indicate RDY/$\overline{\text{BSY}}$.

Figure 3. Programming the Flash Memory

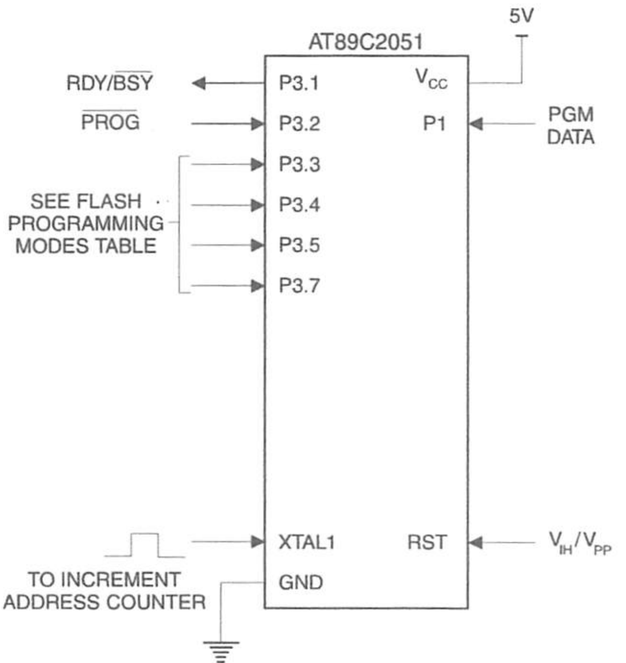
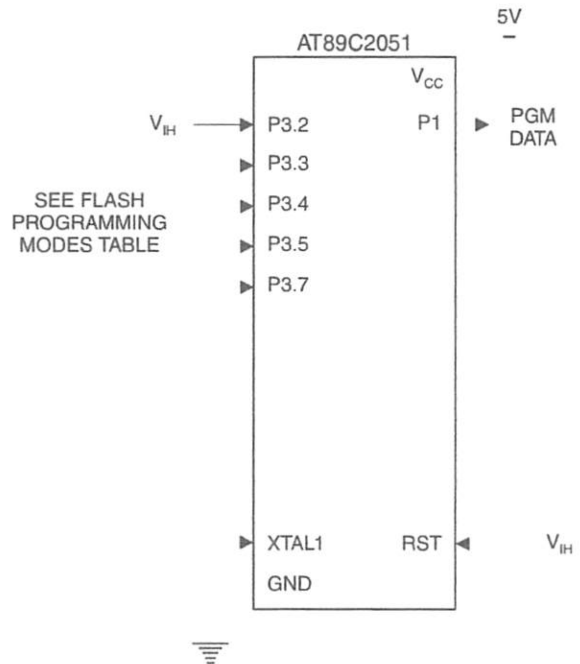


Figure 4. Verifying the Flash Memory



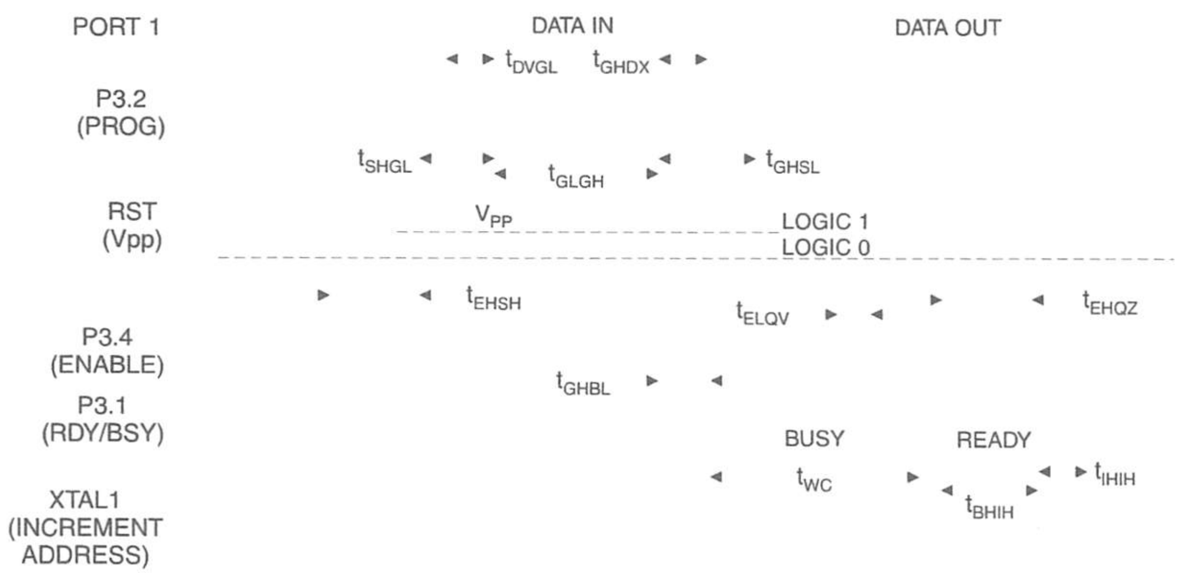
Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		250	µA
t_{DVGL}	Data Setup to $\overline{\text{PROG}}$ Low	1.0		µs
t_{GHDX}	Data Hold After $\overline{\text{PROG}}$	1.0		µs
t_{EHSH}	P3.4 ($\overline{\text{ENABLE}}$) High to V_{PP}	1.0		µs
t_{SHGL}	V_{PP} Setup to $\overline{\text{PROG}}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{\text{PROG}}$	10		µs
t_{GLGH}	$\overline{\text{PROG}}$ Width	1	110	µs
t_{ELQV}	$\overline{\text{ENABLE}}$ Low to Data Valid		1.0	µs
t_{EHQZ}	Data Float After $\overline{\text{ENABLE}}$	0	1.0	µs
t_{GHBL}	$\overline{\text{PROG}}$ High to $\overline{\text{BUSY}}$ Low		50	ns
t_{WC}	Byte Write Cycle Time		2.0	ms
t_{BHIH}	RDY/$\overline{\text{BSY}}$\ to Increment Clock Delay	1.0		µs
t_{IHIL}	Increment Clock High	200		ns

Note: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Waveforms



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	25.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

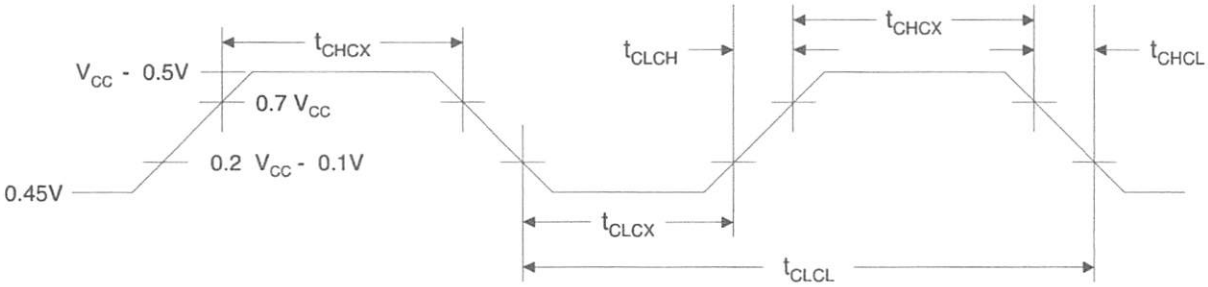
DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.0V to 6.0V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage		-0.5	0.2 V_{CC} - 0.1	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage(1) (Ports 1, 3)	I_{OL} = 20 mA, V_{CC} = 5V I_{OL} = 10 mA, V_{CC} = 2.7V		0.5	V
V_{OH}	Output High Voltage (Ports 1, 3)	I_{OH} = -80 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -30 µA	0.75 V_{CC}		V
		I_{OH} = -12 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1, 3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-750	µA
I_{LI}	Input Leakage Current (Port P1.0, P1.1)	$0 < V_{IN} < V_{CC}$		±10	µA
V_{OS}	Comparator Input Offset Voltage	V_{CC} = 5V		20	mV
V_{CM}	Comparator Input Common Mode Voltage		0	V_{CC}	V
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz, V_{CC} = 6V/3V		15/5.5	mA
		Idle Mode, 12 MHz, V_{CC} = 6V/3V P1.0 & P1.1 = 0V or V_{CC}		5/1	mA
	Power Down Mode(2)	V_{CC} = 6V P1.0 & P1.1 = 0V or V_{CC}		100	µA
		V_{CC} = 3V P1.0 & P1.1 = 0V or V_{CC}		20	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 20 mA
Maximum total I_{OL} for all output pins: 80 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power Down is 2V.

External Clock Drive Waveforms



External Clock Drive

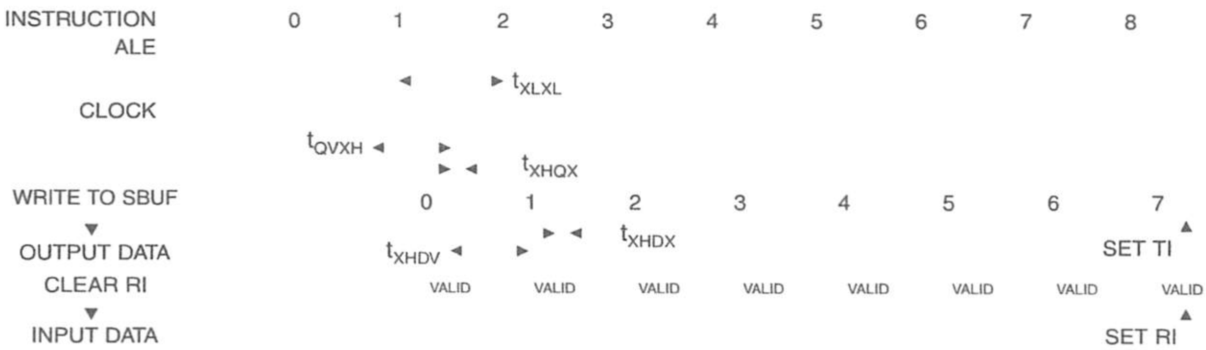
Symbol	Parameter	V_{CC} = 2.7V to 6.0V		V_{CC} = 4.0V to 6.0V		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	12	0	24	MHz
t_{CLCL}	Clock Period	83.3		41.6		ns
t_{CHCX}	High Time	30		15		ns
t_{CLCX}	Low Time	30		15		ns
t_{CLCH}	Rise Time		20		20	ns
t_{CHCL}	Fall Time		20		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

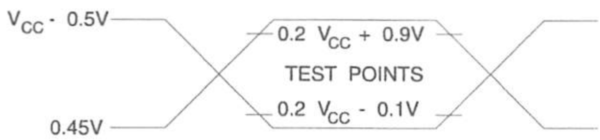
(V_{CC} = 5.0V ± 20%; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

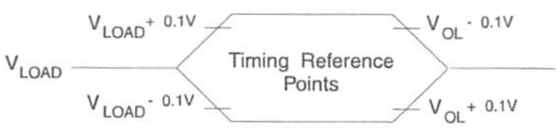


AC Testing Input/Output Waveforms(1)



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

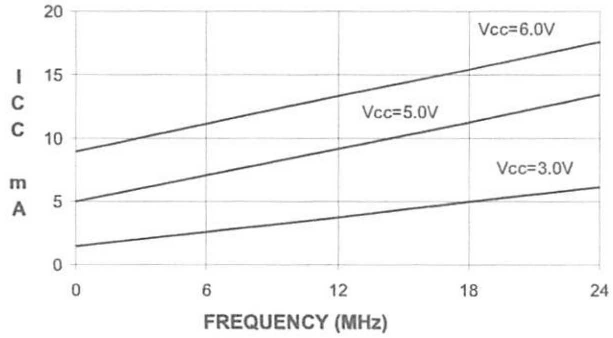
Float Waveforms(1)



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change frothe loaded V_{OH}/V_{OL} level occurs.

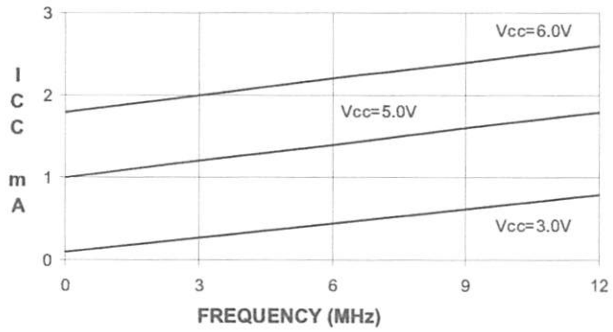
AT89C2051

TYPICAL ICC - ACTIVE (85°C)



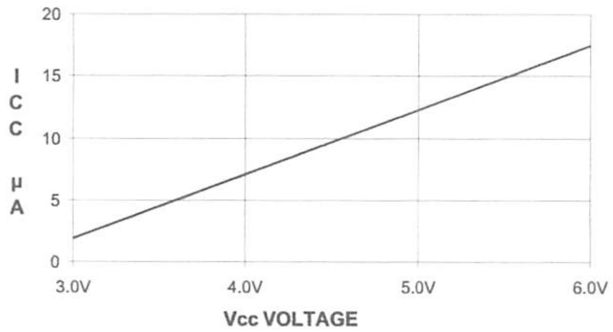
AT89C2051

TYPICAL ICC - IDLE (85°C)



AT89C2051

TYPICAL ICC vs. VOLTAGE- POWER DOWN (85°C)



Notes:
1. XTAL1 tied to GND for I_{CC} (power down)
2. P.1.0 and P1.1 = V_{CC} or GND
3. Lock bits programmed

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	2.7V to 6.0V	AT89C2051-12PC AT89C2051-12SC	20P3 20S	Commercial (0°C to 70°C)
		AT89C2051-12PI AT89C2051-12SI	20P3 20S	Industrial (-40°C to 85°C)
		AT89C2051-12PA AT89C2051-12SA	20P3 20S	Automotive (-40°C to 105°C)
24	4.0V to 6.0V	AT89C2051-24PC AT89C2051-24SC	20P3 20S	Commercial (0°C to 70°C)
		AT89C2051-24PI AT89C2051-24SI	20P3 20S	Industrial (-40°C to 85°C)

Package Type	
20P3	20 Lead, 0.300" Wide, Plastic Dual In-line Package (PDIP)
20S	20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

National Semiconductor

February 1995

LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expanded to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

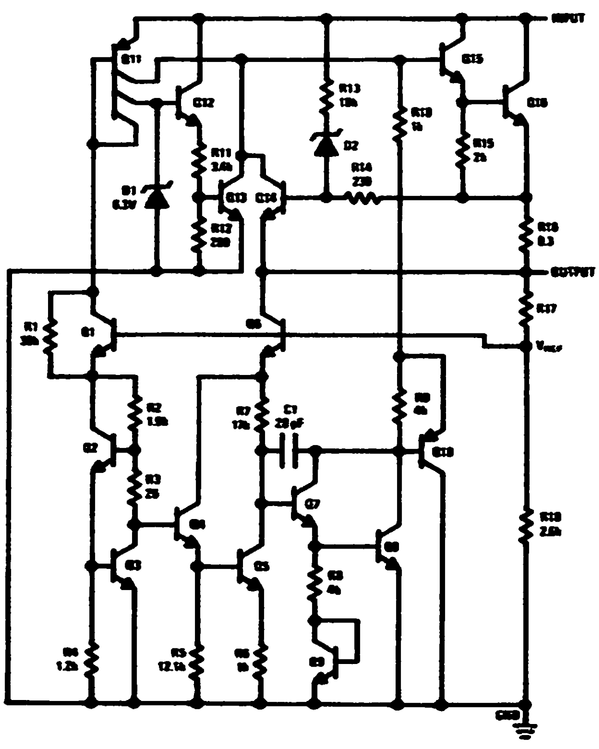
Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

Voltage Range

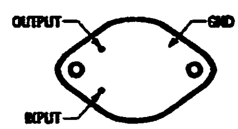
LM7805C	5V
LM7812C	12V
LM7815C	15V

Schematic and Connection Diagrams



TL/H/7746–1

Metal Can Package
TO-3 (K)
Aluminum

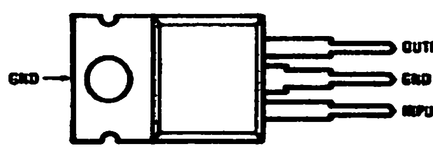


TL/H/7746–2

Bottom View

Order Number LM7805CK, LM7812CK or LM7815CK
See NS Package Number KC02A

Plastic Package
TO-220 (T)



TL/H/7746–3

Top View

Order Number LM7805CT, LM7812CT or LM7815CT
See NS Package Number T03B

 TL/H/7746 RRD-B30M115/Printed in U. S. A.

National Semiconductor

LM78XX Series Voltage Regulators

General Description

[illegible]

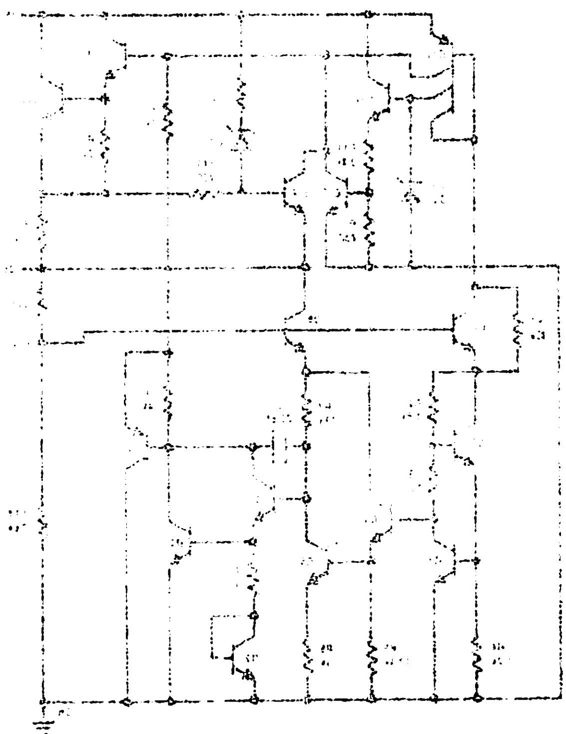
Features

[illegible]

Voltage Range

[illegible]

Schematic and Connection Diagrams

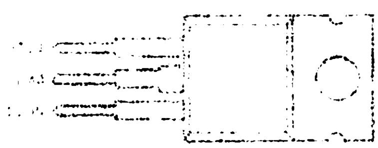


Metal Can Package
TO-3 (K)
Aluminum

Bottom View

Order Number LM7805CK,
LM7812CK or LM7815CK
See NS Package Number K02A

Plastic Package
TO-220 (T)



Top View

Order Number LM7805CT,
LM7812CT or LM7815CT
See NS Package Number T03B

LM78XX Series Voltage Regulators

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage (V_O = 5V, 12V and 15V)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	0°C to +70°C
Maximum Junction Temperature	
(K Package)	150°C
(T Package)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
TO-3 Package K	300°C
TO-220 Package T	230°C

Electrical Characteristics LM78XXC (Note 2) 0°C ≤ Tj ≤ 125°C unless otherwise noted.

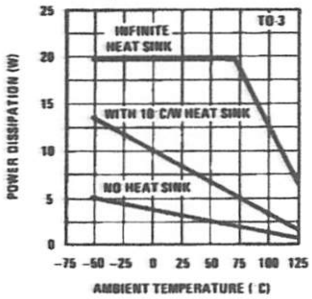
		Output Voltage		5V			12V			15V			
		Input Voltage (unless otherwise noted)		10V			19V			23V			Units
Symbol	Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	Tj = 25°C, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A		4.75		5.25	11.4		12.6	14.25		15.75	V
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			V
ΔV_O	Line Regulation	I_O = 500 mA	Tj = 25°C		3	50		4	120		4	150	mV
			ΔV_{IN}	(7 ≤ V_{IN} ≤ 25)			14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
			0°C ≤ Tj ≤ +125°C			50			120			150	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 20)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 1A	Tj = 25°C			50			120			150	mV
			ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)			V
			0°C ≤ Tj ≤ +125°C			25			60			75	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			V
ΔV_O	Load Regulation	Tj = 25°C	5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	mV
			250 mA ≤ I_O ≤ 750 mA			25			60			75	mV
		5 mA ≤ I_O ≤ 1A, 0°C ≤ Tj ≤ +125°C				50			120			150	mV
I_Q	Quiescent Current	I_O ≤ 1A	Tj = 25°C			8			8			8	mA
			0°C ≤ Tj ≤ +125°C			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A				0.5			0.5			0.5	mA
		Tj = 25°C, I_O ≤ 1A				1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			V
		I_O ≤ 500 mA, 0°C ≤ Tj ≤ +125°C				1.0			1.0			1.0	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
V_N	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40			75			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	I_O ≤ 1A, Tj = 25°C or	62	80		55	72		54	70		dB
			I_O ≤ 500 mA, 0°C ≤ Tj ≤ +125°C	62			55			54			dB
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			V
R_O	Dropout Voltage	Tj = 25°C, I_{OUT} = 1A			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			18			19		mΩ
	Short-Circuit Current	Tj = 25°C			2.1			1.5			1.2		A
	Peak Output Current	Tj = 25°C			2.4			2.4			2.4		A
	Average TC of V_{OUT}	0°C ≤ Tj ≤ +125°C, I_O = 5 mA			0.6			1.5			1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	Tj = 25°C, I_O ≤ 1A			7.5		14.6			17.7			V

Note 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

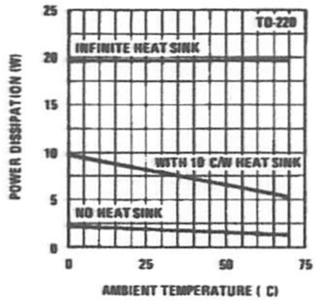
Note 2: All characteristics are measured with capacitor across the input of 0.22 µF, and a capacitor across the output of 0.1µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Characteristics

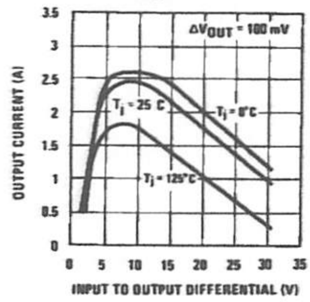
Maximum Average Power Dissipation



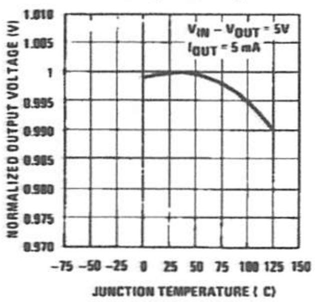
Maximum Average Power Dissipation



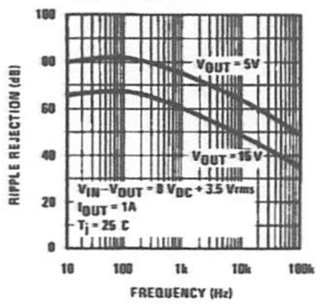
Peak Output Current



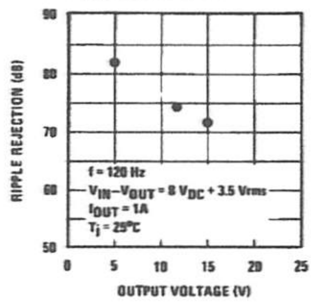
Output Voltage (Normalized to 1V at Tj = 25°C)



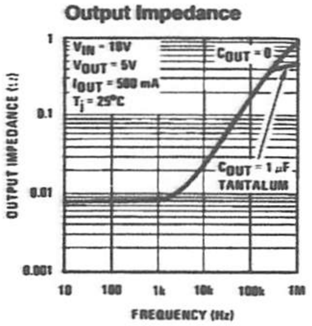
Ripple Rejection



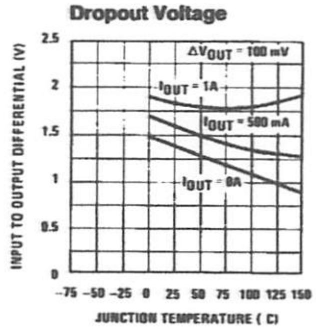
Ripple Rejection



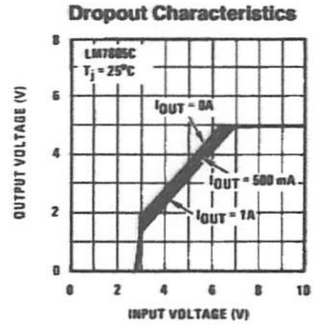
Output Impedance



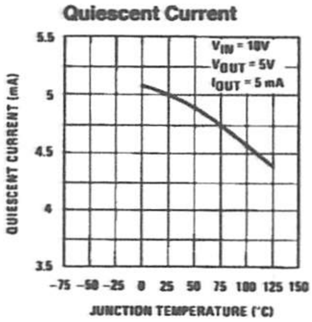
Dropout Voltage



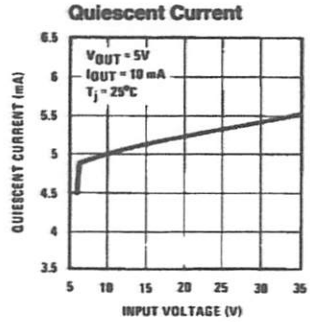
Dropout Characteristics



Quiescent Current

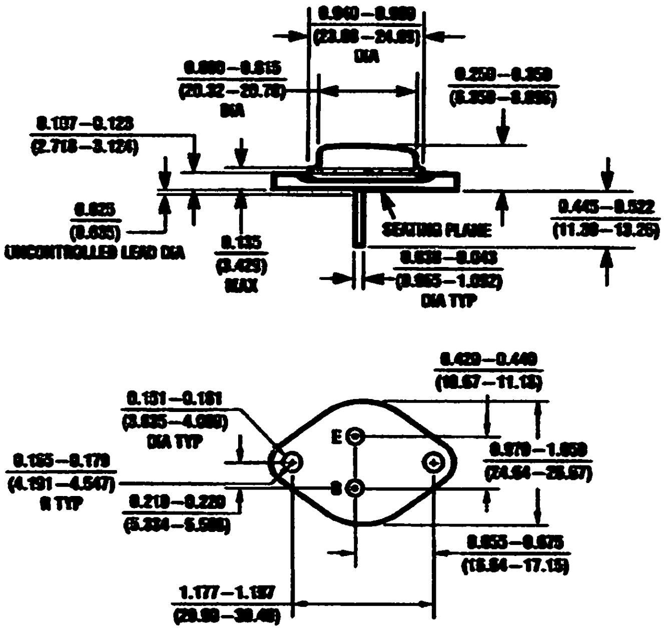


Quiescent Current



TL/H/7746–4

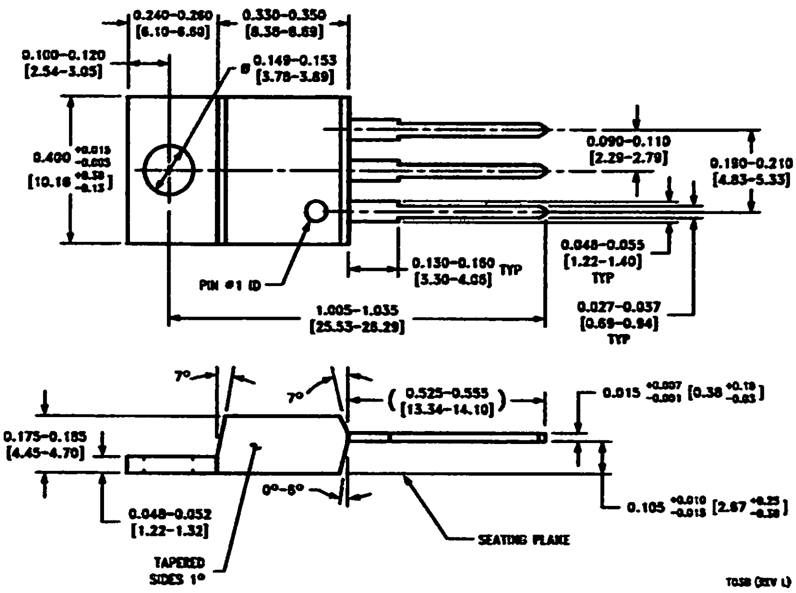
Physical Dimensions inches (millimeters)



KC02A (REV C)

Aluminum Metal Can Package (KC)
Order Number LM7805CK, LM7812CK or LM7815CK
NS Package Number KC02A

Physical Dimensions inches (millimeters) (Continued)



TO-220 Package (T)
Order Number LM7805CT, LM7812CT or LM7815CT
NS Package Number T03B

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Infrared Data Association
Serial Infrared
Physical Layer Link Specification

Version 1.1

October 17, 1995

Authors

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Peter Hortensius, Gregory Russell, Nathan Lee (IBM Corporation)
Hiroshi Uno, Yoshihiro Ohtani (Sharp Corporation)

Document Status and Current Changes

Version 1.0 was approved at the IrDA meeting on April 27, 1994.
Version 1.1a (Proposal) was presented at the IrDA meeting May 31-June 1, 1995.
This proposal is a draft of Version 1.1b.

Proposed Changes from 1.1b August 4, 1995

Proposal version number change from 1.1b to 1.1c.
Joe Tajnaiís email address is new.
Prefactory remarks added to Appendix A and Appendix B, stating informative rather than normative nature of the appendices.
Added CCITT & ITU-T definitions.
Revised Table 5 for 10^-8 BER.
Added text to cover jitter measurements at 1.152 Mb/s in A.2.3.
Corrected 4 Mb/s 4PPM pulse parameter definition: replaced ìbitî with ìsymbolî in text above Table 1 in Section 4.1.

Proposed Changes from 1.1c October 5, 1995

Proposal version number change from 1.1c to 1.1d.
Revised Cover from proposal to draft.
Revised Cover - deleted the names of the 3 companies
Hewlett Packard, IBM and Sharp.
Revised definition for 4 Mb/s 4 PPM pulse paramters in Table 1 and in text above Table 1 in Section 4.1.
Tolerance was changed to 2% of symbol to correctly identify the 10 nsecs specified.
In Table 1 a line was added to identify double pulse parameters for the 4 Mb/s rate.
In Table 2, changed Edge jitter for 115.2 kb/s and below from +/- 2.3 to 6.5%.
Revised section 5.3 to include the polynomial for the 16 bit CRC-CCITT.

Proposed Changes from 1.1d October 17, 1995

Proposal version number change from 1.1d to 1.1e.
In Section 1.4.2 - under Edge Jitter for .576 and 1.152 Mbps, replaced TBD with verbage.
In section 4.1 above Table 1 changed typo of .762 Mbps to .576.
In Section 5.3.1, added some verbage to clarify 16 bit CRC.
In Section 5.3.2.1 - changed 2K-3 bytes to 2045 = (2048 - 3) bytes.
In Appendix A removed 3 redundant paragrapghs talking about jitter measurement for .576 and 1.152 Mbps.

Table of Contents

Figures

Tables

1. Introduction

1.1. Scope

This physical specification is intended to facilitate the point-to-point communication between electronic devices (e.g., computers and peripherals) using directed half duplex serial infrared communications links through free space. This document specifies the optical media interfaces, and 0.576 Mb/s, 1.152 Mb/s and 4.0 Mb/s modulation and demodulation. It contains specifications for the Active Output Interface and the Active Input Interface, and for the overall link. It also contains Appendices covering test methods and implementation examples.

Over the past several years several optical link specifications have been developed. This activity has established the advantages of optical interface specifications to define optical link parameters needed to support the defined link performance. Optical interface specifications are independent of technology, apply over the life of the link and are readily testable for conformance. The IrDA serial infrared link specification supports low cost optoelectronic technology and is designed to support a link between two nodes from 0 to at least 1 metre apart as shown in Figure 1 (the two ports need not be perfectly aligned).

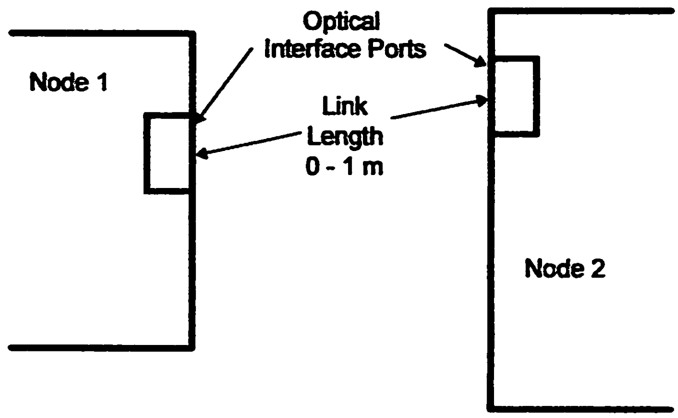


Figure 1. Schematic View of the Optical Interface Port Geometry

1.2. References

The following standards either contain provisions that, through reference in this text, constitute provisions of this proposed standard, or provide background information. At the time of publication of this document, the editions and dates of the referenced documents indicated were valid. However, all standards are subject to revision, and parties to agreements based on this proposed standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

IEC Standard Publication 801-3: Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment, Part 3: Radiated Electromagnetic Field Measurements.

IrDA (Infrared Data Association) Serial Infrared Link Access Protocol (IrLAP), Version 1.0, June 23, 1994.

IrDA (Infrared Data Association) Serial Infrared Link Management Protocol, Version 1.0, 12 August, 1994.

1.3. Abbreviations & Acronyms

4PPM = Four Pulse Position Modulation
A = Address field
Base = Number of pulse positions (chips) in each data symbol
BER = Bit Error Ratio
Bwr = Receiver Bandwidth
Bwrl = Receiver Band Lower Cutoff Frequency
Bwru = Receiver Band Upper Cutoff Frequency
C = Control field
CCITT = International Consultative Committee for Telephone and Telegraph; now ITU-T (CCITT is obsolete term). CCITT used in CRC codes.
Chip = One time slice in a PPM symbol
cm = centimetre(s)
CRC32 = 32 bit IEEE 802.x Cyclic Redundancy Check Field
Ct = Duration of one chip
dB = decibel(s)
DBP = Data Bit Pair
DD = PPM encoded data symbol
Dt = Duration of one data symbol
EIA = Electronic Industries Association
FCS = Frame Check Sequence
FIR = Fast (Serial) Infrared (obsolete term)
HDLC = High level Data Link Control
I = Information field
IEC = International Electrotechnical Commission
IR = Infrared
IRLAP = Infrared Link Access Protocol (document), also IrLAP
IRLMP = Infrared Link Management Protocol (document), also IrLMP
ITU-T = International Technical Union - Telecommunication (new name of old CCITT)
kBd = kilobaud
kb/s = kilobits per second
kHz = kilohertz
LSB = Least Significant Bit
m = metre(s)
mA = milliampere(s)
Mbd = Megabaud
Mb/s = Megabits per second
MHz = MegaHertz
mW = milliwatt(s)
ms = millisecond(s)
MSB = Most Significant Bit
nA = nanoampere(s)
ns = nanosecond(s)
pA = picoampere(s)
PA = Preamble
Payload Data = Real, unencoded data bytes transmitted in any packet
PLL = Phase Locked Loop
PPM = Pulse Position Modulation
RZ = Return-to-Zero
RZI = Return-to-Zero-Inverted
SCC = Serial Communication Controller
SIP = Serial Infrared Interaction Pulse
SIR = Serial Infrared
Sr = Steradian

STA = Start Flag
STO = Stop Flag
Tf = Fall Time
Tr = Rise Time
uA = microampere(s)
UART = Universal Asynchronous Receiver/Transmitter
Up = Peak Wavelength
uA = microampere(s)
us = microsecond(s)
uW = microwatt(s)
V = volt(s)

1.4. Definitions

1.4.1. Link Definitions

BER. Bit Error Ratio is the number of errors divided by the total number of bits. It is a probability, generally very small, and is often expressed as a negative power of 10 (e.g., 10^-8).

Angular Range is described by a cylindrical coordinate system (radial distance r, angular coordinate relative to a defined axis, distance along the axis z) whose axis is normal to the emitting and receiving surface of the optical port and intersects the optical port at the center. The angular range is a cone whose apex is at the intersection of the optical axis and the optical interface plane.

Half-Angle (degrees) is the half angle of the cone whose apex is at the center of the optical port and whose axis is normal to the surface of the port (see Angular Range above). The half angle value is determined by the minimum angle from the normal to the surface where the Minimum Intensity In Angular Range is encountered.

1.4.2. Active Output Interface Definitions

Maximum Intensity In Angular Range, power per unit solid angle (milliwatts per steradian), is the maximum allowable source intensity within the defined angular range (See Angular Range definition in Section 1.4.1.).

Minimum Intensity In Angular Range, power per unit solid angle (milliwatts or microwatts per steradian), is the minimum allowable source intensity within the defined angular range (See Angular Range definition in Section 1.4.1.).

Rise Time Tr, 10-90%, and Fall Time Tf, 90-10% (microseconds or nanoseconds). These are the time intervals for the pulse to rise from 10% to 90% of the 100% value (not the overshoot value), and to fall from 90% to 10% of the 100% value.

Optical Over Shoot, % of Full (or 100%), is the peak optical signal level above the steady state maximum, less the steady state maximum, expressed as a % of the steady state maximum.

Signaling Rate (also called **Bit Rate**), (kilobits per second or megabits per second). The rate at which information (data and protocol information) is sent or received.

Pulse Duration, % of bit period. This is the duration of the optical pulse, measured between 50% amplitude points (relative to the 100% value, not the overshoot value), divided by the duration of the bit or symbol period (depending on the modulation scheme), expressed as a percentage. This parameter is used in the duty factor conversion between average and peak power measurements.

Edge Jitter, %. For rates up to and including 115.2 kb/s, this is the maximum deviation within a frame of an actual leading edge time from the expected value. The expected value is an integer number of bit durations (reciprocal of the signaling rate) after the reference or start pulse leading edge. The jitter is expressed as a percentage of the bit duration.

For 0.576 Mb/s and 1.152 Mb/s rates, the jitter is defined as one half of the worst case deviation in time delay between any 2 edges within 32 bit durations of one another, from the nearest integer multiple of the average bit duration. In other words, at 1.151 Mbps (valid deviation from 1.152 Mbps), if two pulses can be found in a transmitted frame whose edges are separated by 25.10 micoseconds, this would be out of spec., since the nearest integer multiple of the bit duration is 25.195 microseconds, so the observed delay is more than twice 2.9% of a bit period (50.3 nanoseconds) different from the expected delay.

For 4.0 Mb/s, both leading and trailing edges are considered. From an eye diagram (see measurements section-Appendix A), the edge jitter is the spread of the 50% leading and trailing times. The jitter is expressed as a percentage of the symbol duration.

Peak Wavelength (nanometers). Wavelength at which the optical output source intensity is a maximum.

1.4.3. Active Input Interface Definitions

Maximum Irradiance In Angular Range, power per unit area (milliwatts per square centimetre). The optical power delivered to the detector by a source operating at the Maximum Intensity In Angular Range at **Minimum Link Length** must not cause receiver overdrive distortion and possible related link errors. If placed at the Active Output Interface reference plane of the transmitter, the receiver must meet its bit error ratio (BER) specification.

Minimum Irradiance In Angular Range, power per unit area (milliwatts or microwatts per square centimetre). The receiver must meet the BER specification while operating at the Minimum Intensity in Angular Range into the minimum Half-Angle Range at the maximum Link Length.

Half-Angle (degrees) is the half angle of the cone whose apex is at the center of the optical port and whose axis is normal to the surface of the port. The receiver must operate at the Minimum Irradiance In Angular Range from 0 angular degrees (normal to the optical port) to at least the minimum angular range value.

Receiver Latency Allowance (milliseconds or microseconds) is the maximum time after a node ceases transmitting before the nodeís receiver recovers its specified sensitivity.

Edge Jitter, %. The receiver must allow the link to operate within the specified BER for all possible combinations of output interface specs, except for non-allowed codes. No separate input interface jitter parameters are specified. The actual definitions for the various data rates are given in Section 1.4.2.

2. General Description

2.1. Point-to-Point Link Overview

The serial infrared link supports optical link lengths from zero to at least 1 metre for accurate (within specified bit error ratio), free space communication between two independent nodes (such as a calculator and a printer, or two computers).

2.2. Environment

The Optical Interface Specifications apply over the life of the product and over the applicable temperature range for the product. Background light and electric field test conditions are presented in Appendix A.

2.3. Modulation Schemes

For data rates up to and including 1.152 Mb/s, RZI modulation scheme is used, and a ì0î is represented by a light pulse. For rates up to and including 115.2 kb/s, the optical pulse duration is nominally 3/16 of a bit duration (or 3/16 of a 115.2 kb/s bit duration). For 0.576 Mb/s and 1.152 Mb/s, the optical pulse duration is nominally 1/4 of a bit duration.

For 4.0 Mb/s, the modulation scheme is 4PPM. In it, a pair of bits is taken together and called a data symbol. It is divided into 4 ìchipsî, only one of which contains an optical pulse. For 4.0 Mb/s, the nominal pulse duration (chip duration) is 125 ns. A ì1î is represented by a light pulse.

3. Media Interface Description

3.1. Physical Representation

A block diagram of one end of a serial infrared link is shown in Figure 2. Additional signal paths may exist. Because there are many implementation alternatives, this specification only defines the serially encoded optical output and input signals at [3].

In the diagram, the electrical signals to the left of the Encoder/Decoder at [1] are serial bit streams. For data rates up to and including 1.152 Mb/s, the optical signals at [3] are bit streams with a "0" being a pulse, and a "1" is a bit period with no pulse. For 4.0 Mb/s, a 4PPM encoding scheme is used, with a ì1î being a pulse and a ì0î being no a chip with no pulse.. A summary of pulse durations for all supported data rates appears in Table 1 in Section 4.1.

The electrical signals at [2] are the electrical analogs of the optical signals at [3]. For data rates up to and including 115.2 kb/s, in addition to encoding, the signal at [2] is organized into frames with a start bit, 8 data bits, and a stop bit. An implementation of this (up to 115.2 kb/s) is described in Appendix B. For data rates above 115.2 kb/s, data is sent in synchronous frames consisting of many data bytes. Detail of the frame format is found in Section 5.

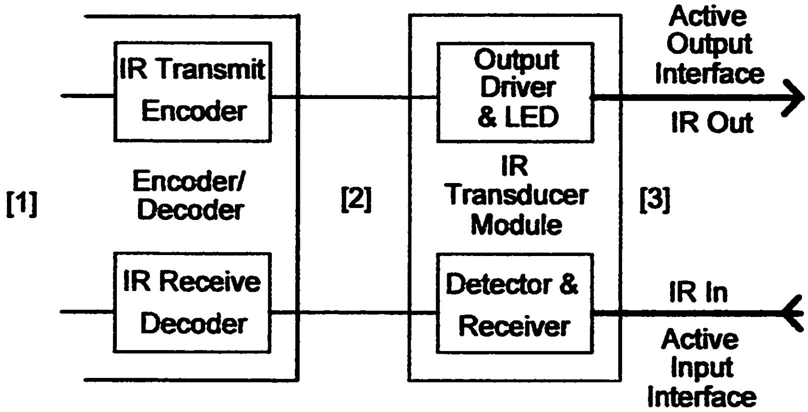


Figure 2. IR Transducer Module Interfaces

3.2. Optical Angle Definitions

The optical axis is assumed to be normal to the surface of the node's face that contains the optical port (See Figure 3). For convenience, the center of the optical port is taken as the reference point where the optical axis exits the port. If there is asymmetry, as long as the maximum half angle of the distribution is not greater than the allowable Half-Angle Range maximum, and the minimum half angle of the distribution is not less than the Half-Angle Range minimum, the Half-Angle Range specification is met.

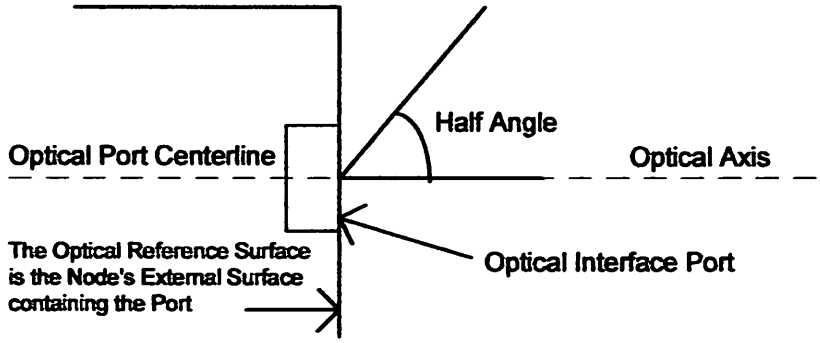


Figure 3. Optical Port Geometry

4. Media Interface Specifications

4.1. Overall Link

The **Link Length** is from 0 to at least 1 metre. The distance is measured between the optical reference surfaces. The link shall operate and meet the BER specification over this range.

The **Bit Error Ratio** (BER) shall be no greater than 10^-8.

Signaling Rate and Pulse Duration: An IrDA serial infrared interface must operate at 9.6 kb/second. Additional allowable rates listed below are optional. Signaling rate and pulse duration specifications are shown in Table 1.

For all signaling rates up to and including 115.2 kb/s the minimum pulse duration is the same (the specification allows both a 3/16 of bit duration pulse and a minimum pulse duration for the 115.2 kb/s signal (1.63 microseconds minus the 0.22 microsecond tolerance)). The maximum pulse duration is 3/16 of the bit duration, plus the greater of the tolerance of 2.5% of the bit duration and 0.60 microseconds.

For 0.576 Mb/s and 1.152 Mb/s, the maximum and minimum pulse durations are the nominal 25% of the bit duration plus 5% (tolerance) and minus 8% (tolerance) of the bit duration.

For 4.0 Mb/s, the maximum and minimum single pulse durations are the nominal 25% of the symbol duration plus and minus a tolerance of 2% of the symbol duration. For 4.0 Mb/s, the maximum and minimum double pulse durations are 50% of the symbol plus and minus a tolerance of 2% of the symbol duration. Double pulses may occur whenever two adjacent chips require a pulse.

The link must meet the BER specification over the link length range and meet the optical pulse constraints.

Signaling Rate	Modulation	Rate Tolerance % of Rate	Pulse Duration Minimum	Pulse Duration Nominal	Pulse Duration Maximum
2.4 kb/s	RZI	+/- 0.87	1.41 us	78.13 us	88.55 us
9.6 kb/s	RZI	+/- 0.87	1.41 us	19.53 us	22.13 us
19.2 kb/s	RZI	+/- 0.87	1.41 us	9.77 us	11.07 us
38.4 kb/s	RZI	+/- 0.87	1.41 us	4.88 us	5.96 us
57.6 kb/s	RZI	+/- 0.87	1.41 us	3.26 us	4.34 us
115.2 kb/s	RZI	+/- 0.87	1.41 us	1.63 us	2.23 us
0.576 Mb/s	RZI	+/- 0.1	295.2 ns	434.0 ns	520.8 ns
1.152 Mb/s	RZI	+/-0.1	147.6 ns	217.0 ns	260.4 ns
4.0 Mb/s (single pulse) (double pulse)	 4PPM 4PPM	 +/-0.01 +/-0.01	 115.0 ns 240.0 ns	 125.0 ns 250.0 ns	 135.0 ns 260.0 ns

Table 1. Signaling Rate and Pulse Duration Specifications

In order to guarantee non-disruptive coexistence with slower (115.2 kb/s and below) systems, once a higher speed (above 115.2 kb/s) connection has been established, the higher speed system must emit a **Serial Infrared Interaction Pulse (SIP)** at least once every 500 ms as long as the connection lasts to quiet slower systems that might interfere with the link. A SIP is defined as a 1.6 us optical pulse of the transmitter followed by a 7.1 us off time of the transmitter. It simulates a start pulse, causing the potentially interfering system to listen for at least 500 ms. See Section 5.2.

The specified values for **Rise Time Tr**, **Fall Time Tf**, and **Jitter** are listed in Table 2.

Receiver Latency Allowance and Conditioning: The receiver electronics can become biased (or even saturated) from optical power coupled from the adjacent transmitter LED in the node. If the link is operating near the minimum optical irradiance condition (see Table 3), there may be a significant period of time before the receiver relaxes to its specified sensitivity. This duration shall not exceed 10 milliseconds, and includes all aspects of a node changing from transmit to receive. See IrDA (Infrared Data Association) Serial Infrared Link Access Protocol (IrLAP) for negotiation of shorter latency times.

Receivers with gain control or other adaptive circuitry may require conditioning after durations of no optical input. The protocol allows for additional start flags (STAs) to be used for conditioning.

Media Access Control and Link Protocol are covered in separate specification documents (see Section 1.2., References).

4.2. Active Output Interface

At the Active Output Interface, an infrared signal is emitted. The specified Active Output Interface parameters appearing in Table 2 are defined in section 1.4 and the associated test methods are found in Appendix A.

SPECIFICATION	Data Rates	Minimum	Maximum
Peak Wavelength, Up, um	All	0.85	0.90
Maximum Intensity In Angular Range, mW/Sr	All	-	500
Minimum Intensity In Angular Range, mW/Sr	115.2 kb/s and below	40	-
	Above 115.2 kb/s	100	-
Half-Angle, degrees	All	+/-15	+/-30
Signaling Rate (also called Clock Accuracy)	All	See Table 1	See Table 1
Rise Time Tr, 10-90%, Fall Time Tf, 90-10% , ns	115.2 kb/s and below	-	600
	Above 115.2 kb/s	-	40
Pulse Duration	All	See Table 1	See Table 1
Optical Over Shoot, %	All	-	25
Edge Jitter, % of nominal bit duration	115.2 kb/s and below	-	+/-6.5
Edge Jitter Relative to Reference Clock, % of nominal bit duration	0.576 and 1.152 Mb/s	-	+/-2.9
Edge Jitter, % of nominal chip duration	4.0 Mb/s	-	+/-4.0

Table 2. Active Output Specifications

4.3. Active Input Interface

If a suitable infrared optical signal impinges upon the Active Input Interface, the signal is detected, conditioned by the receiver circuitry, and output to the IR Receive Decoder. The specified Active Input Interface parameters appearing in Table 3 are defined in section 1.4. The test methods for determining the values for a particular serial infrared interface are found in Appendix A.

SPECIFICATION	Data Rates	Minimum	Maximum
Maximum Irradiance In Angular Range, mW/cm^2	All	-	500
Minimum Irradiance In Angular Range, uW/cm^2	115.2 kb/s and below	4.0	-
	Above 115.2 kb/s	10.0	-
Half-Angle, degrees	All	+/-15	-
Receiver Latency Allowance, ms	All	-	10

Table 3. Active Input Specifications

There is no Half-Angle maximum value for the Active Input Interface. The link must operate at angles from 0 to at least 15 degrees.

There are no Active Input Interface Jitter specifications. The link must meet the BER specification for all negotiated and allowable combinations of Active Output Interface specifications, except for non-allowed codes (Negotiated latency and data rates, start and stop fields and other special sequences are to be avoided.). For rates up to and including 115.2 kb/s, the allowed codes are described in Infrared Data Association Serial Infrared Link Access Protocol (IrLAP), and Infrared Data Association Link Management Protocol. See Section 1.2, References. For 0.576 Mb/s and 1.152 Mb/s and 4.0 Mb/s, see Section 5 of this document.

5. 0.576, 1.152 and 4.0 Mb/s Modulation and Demodulation

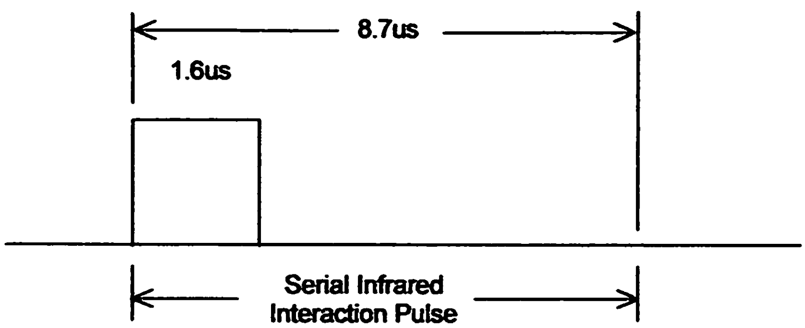
5.1. Scope

This section covers data modulation and demodulation at 0.576, 1.152 and 4.0 Mb/s data rates. The 0.576 and 1.152 Mb/s rates use an encoding scheme similar to 115.2 kb/s; the 4.0 Mb/s rate uses a pulse position modulation (PPM) scheme. Both cases specify packet format, data encoding, cyclic redundancy check, and frame format for use in communications systems based on the optical interface specification.

Systems operating at these higher rates are transparent to IrLAP and IrLMP as it is defined for the lower rates. Architecturally, it appears as an alternate modulation/demodulation (modem) path for data from IrLAP bound for the IR medium. These higher rates are negotiated during normal IrLMP discovery processes. For these and specific discovery bit field definitions of the higher rates, see documents referenced in Section 1.2.

5.2. Serial Infrared Interaction Pulses

In order to guarantee non-disruptive coexistence with slower (up to 115.2 kb/s) systems, once a higher speed (above 115.2 kb/s) connection has been established, the higher speed system must emit a **Serial Infrared Interaction Pulse (SIP)** at least once every 500 ms as long as the connection lasts to quiet slower systems that might interfere with the link (see Section 4.1). The pulse can be transmitted immediately after a packet has been transmitted. The pulse is shown below:



5.3. 0.576 and 1.152 Mb/s Rates

5.3.1. Encoding

The 0.576 and 1.152 Mb/s encoding scheme is similar to that of the lower rates except that it uses one quarter pulse duration of a bit cell instead of 3/16, and uses HDLC bit stuffing after five consecutive ones instead of byte insertion. The following illustrates the order of encoding.

1) The raw transmitted data is scanned from the least significant to the most significant bit of each byte sent and a 16 bit CRC-CCITT is computed for the whole frame except flags and appended at the end of data.

The CRC-CCITT polynomial is defined as follows:

$$CRC(x) = x^{16} + x^{12} + x^{5} + 1$$

(For an example refer to the 32 bit CRC calculation in section 5.4.2.5 and adjust the polynomial for the one indicated above and note the size will be 16 bits (2 bytes) instead of 32 bits (4 bytes), note preset to all 1ís and inversion of the outgoing crc value)

(The address and control field are considered as part of data in this example.) For example, say four bytes, ëCCÍhex, ÍF5Íhex, ÍF1Íhex, and ÍA7Íhex, are data to be sent out in sequence, then ë51DFÍhex is the CRC-CCITT.

	LSB	MSB
Raw Data	00110011 10101111 10001111 11100101	

	LSB	MSB
Data/CRC	00110011 10101111 10001111 11100101 11111011 10001010	

2) A ëZeroí is inserted after five consecutive ones are transmitted in order to distinguish the flag from data. Zero insertion is done on every field except the flags. Using the same data as an example;

	LSB	MSB
Data/CRC	00110011 10101111 10001111 11100101 11111011 10001010	

	First bit to be transmitted	Last bit to be transmitted
Transmit Data	0011001110101111100001111101100101111101011100010100	

(Note: Underlined zeros are inserted bits.)

3) The beginning and ending flags, ë7Eíhex, are appended at the beginning and end. Using the same example;

First bit to be transmitted Last bit to be transmitted

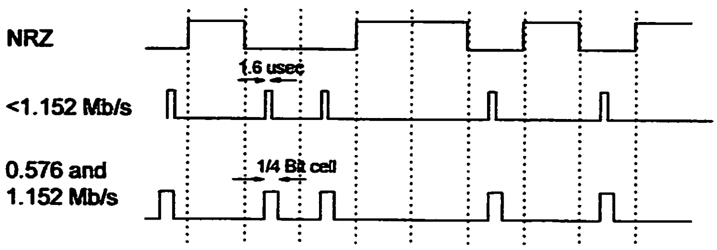
Transmit Data 0111111000110011101011111000011111011001011111010111000101001111110

4) An additional beginning flag is added at the beginning. Finally the whole frame to be sent out is:

First bit to be transmitted Last bit to be transmitted

Tx Frame 01111110011111100011001110101111100001111101100101111101011100010100111111 0

5) The transmitter sends out 1/4 bit cell length of infrared signal whenever data is zero. For example, the frame to be sent out is 0100110101 in binary in the order of being transmitted, then the following figure illustrates the actually transmitted signal for lower data rates and also for 0.576 and 1.152 Mb/s.



5.3.2. Frame Format

5.3.2.1. Frame Overview

The 0.576 and 1.152 Mb/s frame format follows the standard HDLC format except that it requires two beginning flags and consists of two beginning flags, an address field, a control field, an information field, a frame check sequence field and minimum of one ending flag. ë7Eíhex is used for the beginning flag as well as for the ending flag. The frame format is the same as for the lower rate-IrLAP frame with STA changed from ëC0íhex to ë7Eíhex and STO changed from ëC1íhex to ë7Eíhex.

STA	STA	ADDR	DATA	16b FCS	STO

STA:	Beginning Flag, 01111110 binary
ADDR:	8 bit Address Field
DATA:	8 bit Control Field plus up to 2045 = (2048 - 3) bytes Information Field
FCS:	CCITT 16 bit CRC
STO:	Ending Flag, 01111110 binary

Note 1: Minimum of three STO fields between back to back frames is required.
Note 2: Zero insertion after five consecutive 1's is used. CRC is computed before zero insertion is performed.
Note 3: Least significant bit is transmitted first.
Note 4: Abort sequence requires minimum of seven consecutive 1ís.
Note 5: 8 bits are used per character before zero insertion.

5.3.2.2. Beginning Flag (STA) and Ending Flag (STO) Definition

The 0.576 and 1.152 Mb/s links use the same physical layer flag, 01111110, for both STA and STO. It is required to have a minimum of two STAs and a minimum of one STO. The receiver treats multiple STAs or STOs as a single flag even if it receives more than one.

5.3.2.3. Address Field (ADDR) Definition

The 0.576 and 1.152 Mb/s links expect the first byte after STA to be the 8 bit address field. This address field should be used as specified in the IrLAP.

5.3.2.4. Data Field (DATA) Definition

The data field consists of Control field and optional information field as defined in the IrLAP.

5.3.2.5. Frame Check Sequence Field (FCS) Definition

The 0.576 and 1.152 Mb/s links use a 16 bit CRC-CCITT cyclic redundancy check to check received frames for errors that may have been introduced during frame transmission. The CRC is computed from the ADDR and Data fields using the same algorithm as specified in the IrLAP.

5.3.2.6. Frame Abort

A prematurely terminated frame is called an aborted frame. The frame can be aborted by blocking the IR transmission path in the middle of the frame, a random introduction of infrared noise, or intentional termination by the transmitter. Regardless what caused the aborted frame, the receiver treats a frame as an aborted frame when seven or more consecutive ones (no optical signal) are received. The abort terminates the frame immediately without the FCS field or an ending flag.

5.3.2.7. Frame Transmission Order

All fields are transmitted the least significant bit of each byte first.

5.3.2.8. Back to Back Frame Transmission

Back to back, or ìbrick-walledî frames are allowed with three or more flags, ë01111110íb, in between. If two consecutive frames are not back to back, the gap between the last ending flag of the first frame and the STA of the second frame should be separated by at least seven bit durations (abort sequence).

5.4. 4 Mb/s Rate

5.4.1. 4PPM Data Encoding Definition

Pulse Position Modulation (PPM) encoding is achieved by defining a data symbol duration (Dt) and subsequently subdividing Dt into a set of equal time slices called "chips." In PPM schemes, each chip position within a data symbol represents one of the possible bit combinations. Each chip has a duration of Ct given by:

Ct = Dt/Base

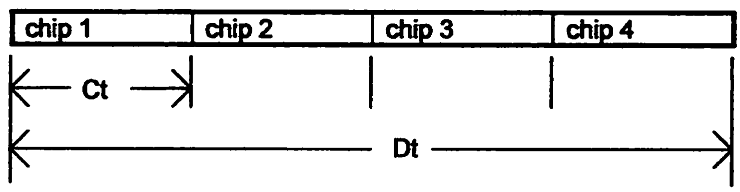
In this formula "Base" refers to the number of pulse positions, or chips, in each data symbol. The Base for IrDA PPM 4.0 Mb/s systems is defined as four, and the resulting modulation scheme is called "four pulse position modulation (4PPM)." The data rates of IrDA PPM systems are defined as 4.0 Mb/s. The resulting values for Ct and Dt are as follows:

Dt = 500 ns

Ct = 125 ns

The figure below describes a data symbol field and its enclosed chip durations for the 4PPM scheme.

ONE COMPLETE
SYMBOL



Because there are four unique chip positions within each symbol in 4PPM, four independent symbols exist in which only one chip is logically a "one" while all other chips are logically a "zero." We define these four unique symbols to be the only legal data symbols (DD) allowed in 4PPM. Each DD represents two bits of payload data, or a single "data bit pair (DBP)", so that a byte of payload data can be represented by four DDs in sequence. The following table defines the chip pattern representation of the four unique DDs defined for 4PPM.

Data Bit Pair (DBP)	4PPM Data Symbol (DD)
00	1000
01	0100
10	0010
11	0001

Logical ì1î represents a chip duration when the transmitting LED is emitting light, while logical ì0î represents a chip duration when the LED is off.

Data encoding for transmission is done LSB first. The following examples show how various data bytes would be represented after encoding for transmission. In these examples transmission time increases from left to right so that chips and symbols farthest to the left are transmitted first.

Data Byte	Resulting DBPs	Resulting DD Stream (chips and symbols transmitted from left to right for LSB first reception)
Xi1Bi	00 01 10 11	
		0001
		0010
		0100
		1000
		0001 0010 0100 1000
Xi0Bi	00 00 10 11	0001 0010 1000 1000
XiA4i	10 10 01 00	1000 0100 0010 0010

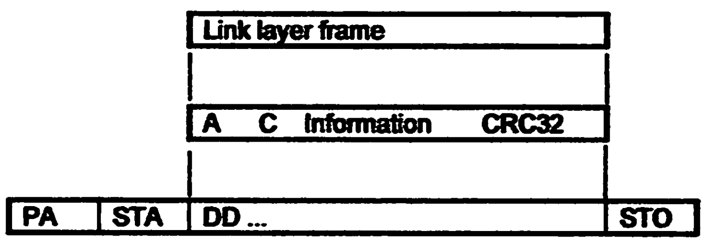
First chip delivered to/received by physical layer.

Last chip delivered to/received by physical layer.

5.4.2. PPM Packet Format

5.4.2.1. Packet Overview

For 4.0 Mb/s PPM packets the following packet format is defined:



In this packet format, the payload data is encoded as described in the 4PPM encoding above, and the encoded symbols reside in the DD field. Maximum packet length is negotiated by the same mechanism as for the slower rates. The preamble field (PA) is used by the receiver to establish bit synchronization. After PA, the receiver begins to search for the start flag (STA) to establish symbol synchronization. If STA is received correctly, the receiver can begin to interpret the data symbols in the DD field. The receiver continues to receive and interpret data until the stop flag (STO) is recognized. STO indicates the end of a frame. The chip patterns and symbols for PA, STA, FCS field, and STO are defined below. Only complete packets that contain the entire format defined above are guaranteed to be decoded at the receiver (note that, as for the lower rates, the information field, I, may be of zero length).

The 4PPM data encoding described above defines only the legal encoded payload data symbols. All other 4 chip combinations are by definition illegal symbols for encoded payload data. Some of these illegal symbols are used in the definition of the preamble, start flag, and stop flag fields because they are unambiguously not data.

Data Byte	Resulting DBPs	Resulting DD Stream (chips and symbols transmitted from left to right for LSB first reception)
0x1B	00 01 10 11	0001
		0010
		0100
		1000
		0001 0010 0100 1000
0x0E	00 00 10 11	0001 0010 1000 1000
0xAA	10 10 10 10	0010 0010 0010 0010

First chip delivered to/received by physical layer

Last chip delivered to/received by physical layer

5.4.2. PPM Packet Format

5.4.2.1. Packet Overview

For 4.0 Mb/s PPM packets the following packet format is used:

Link Layer Frame			
A	C	Information	CRC32

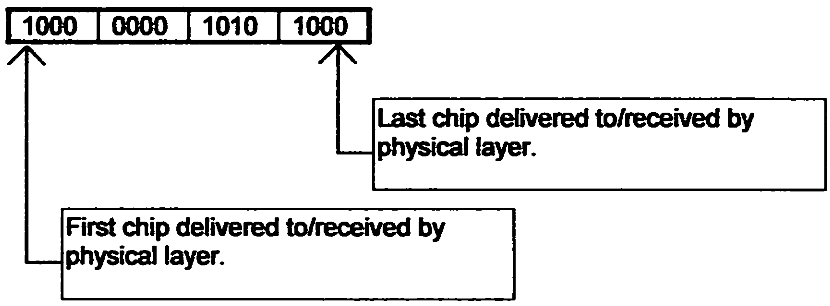
PA	STA	DD	STO

In this packet format, the payload data is encoded as described in the 4PPM encoding above, and the encoded symbols reside in the DD field. Maximum packet length is negotiated in the same mechanism as for the slower rates. The preamble field (PA) is used by the receiver to establish bit synchronization. After PA, the receiver begins to search for the start flag (STA) to establish symbol synchronization. If STA is received correctly, the receiver can begin to interpret the data symbols in the DD field. The receiver continues to receive and interpret data until the stop flag (STO) is recognized. STO indicates the end of a frame. The chip patterns and symbols for PA, STA, FCS field and STO are defined below. Only complete packets that contain the entire format defined above are guaranteed to be decoded at the receiver (note that, as for the lower rates, the information field may be of zero length).

The 4PPM data encoding described above defines only the legal encoded data symbols. All other 4 chip combinations are by definition illegal symbols for encoded payload data. Some of these illegal symbols are used in the definition of the preamble, start flag, and stop flag fields because they are unambiguously not data.

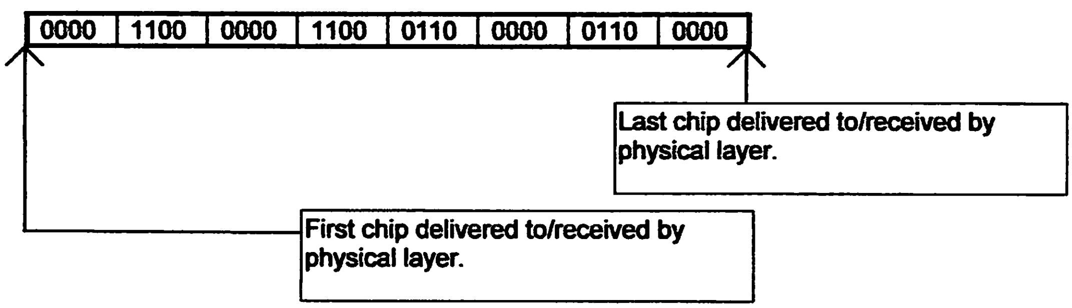
5.4.2.2. Preamble Field Definition

The preamble field (PA) consists of exactly sixteen repeated transmissions of the following stream of symbols. In the PA field, transmission time increases from left to right so that chips and symbols on the left are transmitted first.



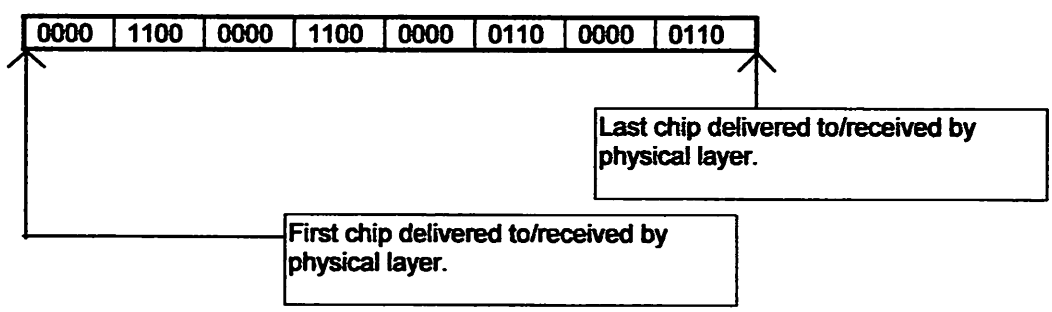
5.4.2.3. Start Flag Definition

The start flag (STA) consists of exactly one transmission of the following stream of symbols. In the STA field, transmission time increases from left to right so that chips and symbols on the left are transmitted first.



5.4.2.4. Stop Flag Definition

The stop flag (STO) consists of exactly one transmission of the following stream of symbols. In the STO field, transmission time increases from left to right so that chips and symbols on the left are transmitted first.



5.4.2.5 Frame Check Sequence Field Definition

Frame check sequence (FCS) field is a 32 bit field that contains a cyclic redundancy check (CRC) value. The CRC is a calculated, payload data dependent field. It consists of the 4PPM encoded data resulting from the IEEE 802 CRC32 algorithm for cyclic redundancy check as applied to the payload data contained in the packet. The CRC32 polynomial is defined as follows:

$$CRC(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x + 1$$

The CRC32 calculated result for each packet is treated as four data bytes, and each byte is encoded in the same fashion as is payload data. Payload data bytes are input to this calculation in LSB first format.

The 32 bit CRC register is preset to all "1's" prior to calculation of the CRC on the transmit data stream. When data has ended and the CRC is being shifted for transmission at the end of the packet, a "0" should
be shifted in so that the CRC register becomes a virtual shift register. Note: the inverse of the CRC register is what is shifted as defined in the polynomial. An example of a verilog implementation follows to describe the process.

```
module txcrc32(clrcrc,clk,txdin,nreset,crcndata,txdout,bdcrc);
/* ************************************************************************ */
// compute 802.X CRC x32 x26 x23 x22 x16 x12 x11 x10 x8 x7 x5 x4 x2 x + 1
// on serial bit stream.
/* ************************************************************************ */
/* bdcrc is input signal used to send a bad crc for test purposes */
/* note ^ is exclusive or function */

input clrcrc,clk,txdin,nreset,crcndata,bdcrc;
output txdout;
reg [31:0] nxtxcrc,txcrc;

/* ************************************************************************ */
// XOR data stream with output of CRC register and create input stream
// if crcndata is low, feed a 0 into input to create virtual shift reg
/* ************************************************************************ */

wire crcshin = (txcrc[31] ^ txdin) & ~crcndata;

/* ************************************************************************ */
// combinatorial logic to implement polynomial
/* ************************************************************************ */

always @ (txcrc or clrcrc or crcshin)
begin
if (clrcrc)
nxtxcrc <= 32'hffffffff;
else
begin
nxtxcrc[31:27] <= txcrc[30:26];
nxtxcrc[26] <= txcrc[25] ^ crcshin; // x26
nxtxcrc[25:24] <= txcrc[24:23];
nxtxcrc[23] <= txcrc[22] ^ crcshin; // x23
nxtxcrc[22] <= txcrc[21] ^ crcshin; // x22
nxtxcrc[21:17] <= txcrc[20:16];
nxtxcrc[16] <= txcrc[15] ^ crcshin; // x16
nxtxcrc[15:13] <= txcrc[14:12];
nxtxcrc[12] <= txcrc[11] ^ crcshin; // x12
nxtxcrc[11] <= txcrc[10] ^ crcshin; // x11
nxtxcrc[10] <= txcrc[9] ^ crcshin; // x10
nxtxcrc[9] <= txcrc[8];
```

```
nxtxcrc[8] <= txcrc[7] ^ crcshin; // x8
nxtxcrc[7] <= txcrc[6] ^ crcshin; // x7
nxtxcrc[6] <= txcrc[5];
nxtxcrc[5] <= txcrc[4] ^ crcshin; // x5
nxtxcrc[4] <= txcrc[3] ^ crcshin; // x4
nxtxcrc[3] <= txcrc[2];
nxtxcrc[2] <= txcrc[1] ^ crcshin; // x2
nxtxcrc[1] <= txcrc[0] ^ crcshin; // x1
nxtxcrc[0] <= crcshin; // +1
end

end
/* ************************************************************************** */
// infer 32 flops for strorage, include async reset asserted low
/* ************************************************************************** */
always @ (posedge clk or negedge nreset)
begin
if (!nreset)
txcrc <= 32'hffffffff;
else
txcrc <= nxtxcrc;     // load D input (nxtxcrc) into flops
end
/* ************************************************************************** */
// normally crc is inverted as it is sent out
// input signal badcrc is asserted to append bad CRC to packet for
// testing, this is an implied mux with control signal crcndata
// if crcndata = 0 , the data is passed by unchanged, if = 1 then
// the crc register is inverted and transmitted.
/* ************************************************************************** */

wire txdout = (crcndata) ? (~txcrc[31] ^ bdcrc) : txdin; // don't invert
                                                 // if bdcrc is 1
endmodule
/* ************************************************************************** */
```

The following shows a CRC calculation and how the results would be represented after encoding for transmission. The results of the CRC calculation (txcrc[31 - 0]) is shown in the next table when the contents of the DD field is Xí1Bí and XíA4í, where Xí1Bí is the first byte of the DD field. If the four bytes of CRC are counted as received data, then the resultant 6 bytes in order would be Xí1Bí, XíA4í, Xí94í, XíBEí, Xí54í and Xí39í.

	[31] [0]
txcrc[31-0]	1101 0110 1000 0010 1101 0101 0110 0011
~txcrc[31-0]	0010 1001 0111 1101 0010 1010 1001 1100

CRC Value	Resulting DBPs	Resulting DD Stream (chips and symbols transmitted from left to right for LSB first reception)
~txcrc[24-31]	10 01 01 00	
		1000
		0100
		0100
		0010
		1000 0100 0010 0001
~txcrc[16-23]	10 11 11 10	0010 0001 0001 0010
~txcrc[8-15]	01 01 01 00	1000 0100 0100 0100
~txcrc[0-7]	00 11 10 01	0100 0010 0001 1000

First chip delivered to/received by physical layer.

Last chip delivered to/received by physical layer.

5.4.3. Aborted Packets

Receivers may only accept packets that have valid STA, DD, FCS, and STO fields as defined in the PPM Packet Format section. The PA field need not be valid in the received packet. All other packets are aborted and ignored.

Any packet may be aborted at any time after a valid STA but before transmission of a complete STO flag by two or more repeated transmissions of the illegal symbol "0000." Also, any packet may be aborted at any time after a valid STA by reception of any illegal symbol which is not part of a valid STO field.

5.4.4. Back to Back Packet Transmission

Back to back, or "brick-walled" packets are allowed, but each packet must be complete (i.e., containing PA, STA, DD and STO fields). Brick-walled packets are illustrated below.

Packet 1				Packet 2			
PA	STA	DD	STO	PA	STA	DD	STO

Appendix A. Test Methods

(Note-Appendix A is Informative, not Normative {i.e., it does not contain requirements, but is for information only}.)

A.1. Background Light and Electromagnetic Field

There are four ambient interference conditions in which the receiver is to operate correctly. The conditions are to be applied separately:

1. Electromagnetic field: 3 V/m maximum (refer to IEC 801-3. severity level 3 for details)
2. Sunlight: 10 kilolux maximum at the optical port
   This is simulated with an IR source having a peak wavelength within the range 850 nm to 900 nm and a spectral width less than 50 nm biased to provide 490 uW/cm^2 (with no modulation) at the optical port. The light source faces the optical port.

   This simulates sunlight within the IrDA spectral range. The effect of longer wavelength radiation is covered by the incandescent condition.
3. Incandescent Lighting: 1000 lux maximum
   This is produced with general service, tungsten-filament, gas-filled, inside-frosted lamps in the 60 Watt to 150 Watt range to generate 1000 lux over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The source is expected to have a filament temperature in the 2700 to 3050 degrees Kelvin range and a spectral peak in the 850 nm to 1050 nm range.
4. Fluorescent Lighting : 1000 lux maximum
   This is simulated with an IR source having a peak wavelength within the range 850 nm to 900 nm and a spectral width of less than 50 nm biased and modulated to provide an optical square wave signal (0 uW/cm^2 minimum and 0.3 uW/cm^2 peak amplitude with 10% to 90% rise and fall times less than or equal to 100 ns) over the horizontal surface on which the equipment under test rests. The light sources are above the test area. The frequency of the optical signal is swept over the frequency range from 20 kHz to 200 kHz.

   Due to the variety of fluorescent lamps and the range of IR emissions, this condition is not expected to cover all circumstances. It will provide a common floor for IrDA operation.

A.2. Active Output Specifications

A.2.1. Peak Wavelength

The peak wavelength (Peak Wavelength, Up, um) is the wavelength of peak intensity and can be measured using an optical spectrum analyzer. The pulse shape and sequence can be the same as that used for the power measurements below and the measurement can be made on the optical axis.

A.2.2. Intensity and Angle

The following three specifications form a set that can be measured concurrently:

- Maximum Intensity In Angular Range, mW/Sr
- Minimum Intensity In Angular Range, mW/Sr
- Half-Angle, degrees

This intensity measurement requires means to measure optical power as well as the distance and angle from a reference point. Power measured in milliwatts (mW) or microwatts (uW) is converted to intensity in mW/Sr (or uW/Sr) or irradiance in mW/cm^2 (or uW/cm^2). In addition, if there are any cosmetic windows or filters that are part of the interface, they must be in place for all intensity and spatial distribution optical measurements

The primary reference point is the center point of the surface of the IrDA optical port and the port's optical axis is the line through the reference point and normal to the port surface. Link specifications are based on the assumption that the maximum intensity at the port surface is 500 mW/cm^2 due to a point source of 500 mW/Sr maximum intensity placed one centimetre behind the reference surface. Distance is measured radially from the reference point to the test head. Half-Angle is the angular deviation from the optical axis as shown in Figure 4. The plane of the detector at the Test Head is normal to the radial vector from the center of the optical port to the detector.

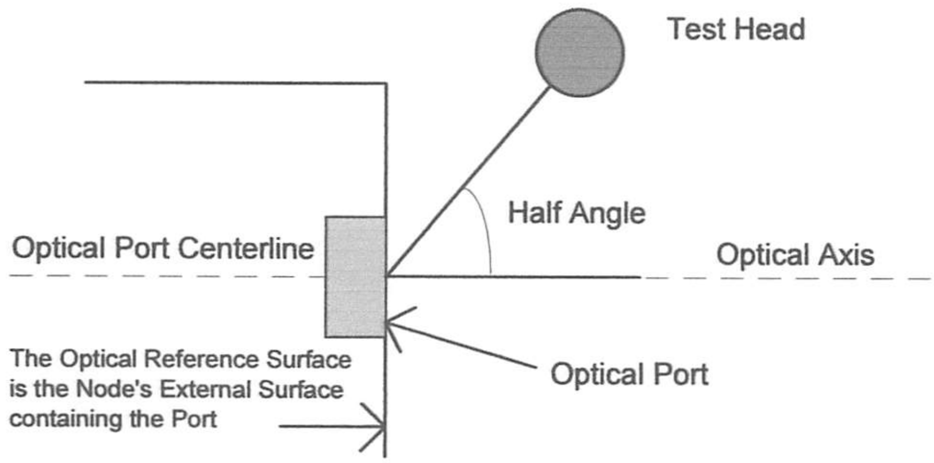


Figure 4. Optical Port Angle Measurement Geometry

The IrDA link specification is based on peak optical power levels. Power measurement can be made on a single pulse or by averaging a sequence of pulses and converting to peak levels. Averaging methods require knowledge of the pulse sequence and/or duty factor in order to calculate the peak power from the reported average. In addition, for short pulse durations, attention must be paid to the effect of the rise and fall times of the optical signal on the effective optical pulse duration.

The test head is to be calibrated to provide accurate results for signals within the appropriate ranges of wavelength, pulse and pulse sequence characteristics. The size of the photodetector in the test head must be known in order to translate the results from power (mW or uW) to irradiance (mW/cm^2 or uW/cm^2) and intensity (mW/Sr or uW/Sr). Finally, the test head should be aimed directly at the reference point, i.e., the test detector should be normal to the vector from the center of the optical port to the center of the test detector.

The power measurement should be made at a distance large enough to avoid near field optical effects but close enough to receive a robust signal. To test for an appropriate distance, make power measurements at half and double the chosen distance and check that the results are consistent with an inverse square relationship.

Resolution of spatial intensity variation should be as fine as the smallest detector. Unfortunately, because the detected signal intensity is averaged over the size of the test head, resolution becomes a tradeoff with signal strength. There is no size constraint for the detector in the IrDA receiver. Since it is impractical to test with an infinitesimal detector, spatial resolution will be measured to a resolution of 2 x 10^-5 steradians. This can be achieved with a detector having an effective area of 0.2 cm^2 (5 mm diameter) at 1.0 metre, which subtends a half-angle of 0.14 degrees.

Figure 5 contains a graphical representation of the serial infrared Active Output Interface specifications. The measured intensity must be less than or equal to "Maximum Intensity In Angular Range" in the angular region less than or equal to 30 degrees and less than or equal to "Minimum Intensity In Angular Range" in the angular region greater than 30 degrees. The measured intensity must be greater than or equal to "Minimum Intensity In Angular Range" in the angular region less than or equal to 15 degrees. The minimum allowable intensity value is indicated by ìminî in Figure 5, since the actual specified value is dependent upon data rate.

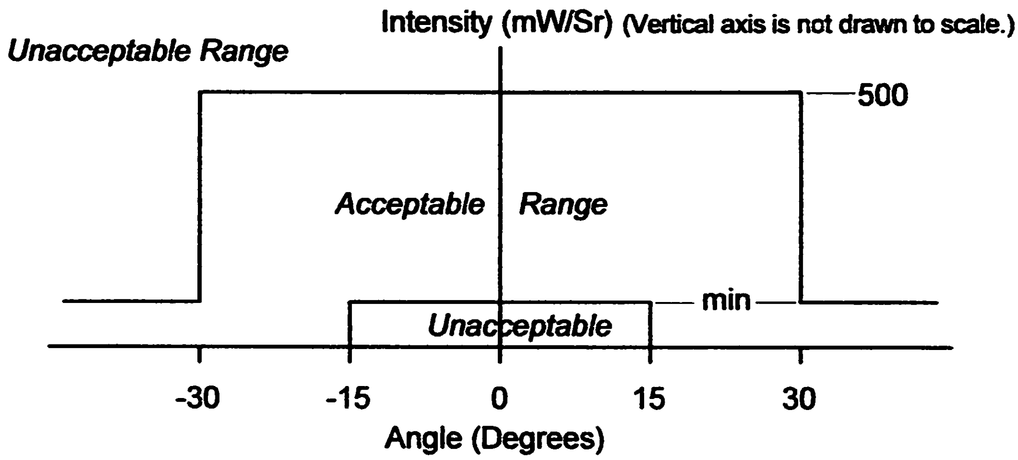


Figure 5. Acceptable Optical Output Intensity Range

The optical power measurements are converted to optical intensity across the +/- 30 degree region to verify both the maximum and minimum intensity specifications and sufficiently beyond +/- 30 degrees to verify the specification. Optical power is converted to intensity by the relationship

Intensity(mW/Sr) = [Power(mW)]/[Detector Solid Angle(Sr)].

The Detector Solid Angle in steradians is given by the relationship

Detector Solid Angle (Sr) = 2pi[1-cos(Half-Angle)],

where the Half-Angle is half the angle subtended by the detector, viewed from the reference point.

The Detector Solid Angle can be approximated with the relationship

Detector Solid Angle (Sr) ~ [Area of Detector]/[r^2],

where r is the distance between the test head and the reference point.

A.2.3. Pulse Parameters and Signaling Rate

The following six specifications form a set that can be measured with the same set-up:

- Rise Time Tr, 10-90%, us or ns
- Fall Time Tf, 90-10%, us or ns
- Pulse Duration, % of Bit or Symbol Period
- Optical Over Shoot, %
- Edge Jitter, us or ns
- Signaling Rate, kb/s or Mb/s

These measurements require means to measure optical power and an oscilloscope (or equivalent) with sufficient bandwidth to resolve jitter to better than 0.2 us (for data rates up to and including 115.2 kb/s). A minimum bandwidth of 5 MHz is recommended. The output of the test optical detector must be able to drive the oscilloscope input. For the data rates up to 4.0 Mb/s, jitter down to 10 ns must be resolved, so a minimum bandwidth of 100 MHz is recommended.

Definitions of the reference point, etc., are the same as for the Active Output Interface power measurements and the same considerations for test distance and signal strength apply. The test head should be positioned within +/- 15 degrees of the optical axis and aimed directly at the reference point.

Rise Time, Fall Time, Pulse Duration and Overshoot can be measured for a single optical pulse. Since overshoot is referenced to the pulse amplitude at the end of the pulse, the maximum duration pulses should be used in this test. For Rise Time, Fall Time, Pulse Duration and Overshoot, refer to Figure 6. It is critical to determine the 100% level, since all four of these parameters are dependent upon it. If there is uncertainty concerning the existence of the flat region that defines the 100% level (is there over shoot, or does the pulse have a long, rounded top?), measurements at a longer drive pulse duration will resolve this, and allow easier determination of the 100% level.

Jitter and Signaling Rate require a sequence of pulses for determination. For data rates up to and including 115.2 kb/s, the signal is asynchronous at the byte level (though typically less than 20ms {window=7, packet size=2k}), therefore Jitter and Signal Rate are only relevant within a byte. For 0.576 Mb/s, 1.152 Mb/s and 4.0 Mb/s, however, the optical bit stream is synchronous for up to 500 ms, though typically less than 20 ms (window = 7, packet size = 2k). Thus, the measurement requires the accumulation of data over a longer time interval.

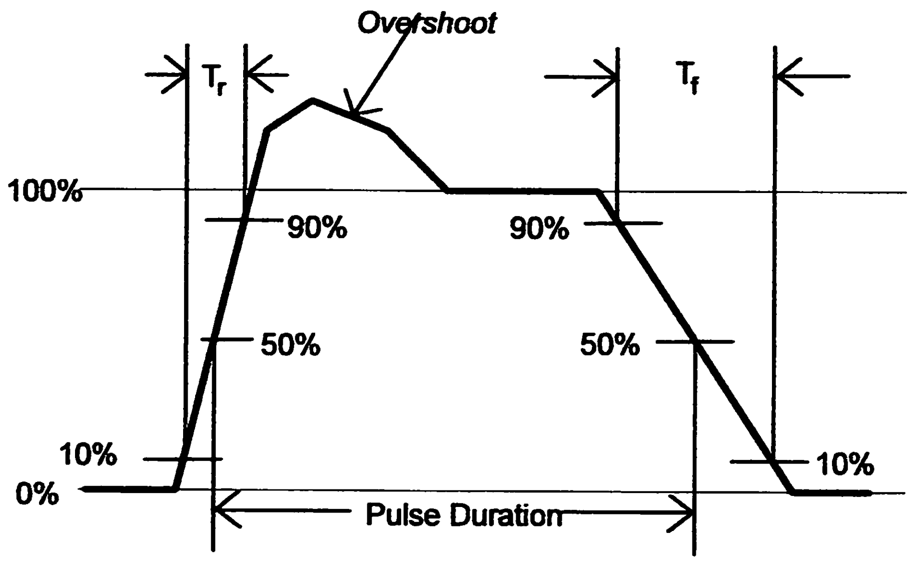


Figure 6. Pulse Parameter Definitions

For rates up to and including 115.2 kb/s, we can consider jitter to be the range of deviation between the leading edge of the optical pulse and a reference signal edge. Refer to Figure 7. For simplicity, the reference signal can be taken to be the leading edge of the first pulse in the byte (the ìStartî pulse). Using the nominal data rate, the arrival time of each pulse in the byte can be predicted. The jitter (in time units) is the maximum departure from predicted arrival time of the actual arrival time. Since jitter may be pattern dependent, various data should be used in the test signal.

The reciprocal of the mean of the absolute delay times between optical pulses is the data rate. Although some accuracy should be gained by the averaging, for only 1 asynchronous byte the tolerance requirement may be difficult to achieve with an oscilloscope. If UART frames are back to back (synchronous across bytes), use of an oscilloscope may be adequate. If access to an internal clock signal is available, a counter may be used.

For 0.576 and 1.152 Mb/s RZI and 4.0 Mb/s 4PPM, an entire packet can be used to determine jitter. The optical signal should be detected using a high speed optical detector (e.g., a reverse-biased, small silicon p-i-n diode). The detector output signal is displayed using a storage oscilloscope set to trigger as often as possible during a packet, the stored image displaying an eye diagram. Care should be taken to use time constants in any a.c. coupling which are much, much longer than the symbol times.. The jitter (in time units) is half of the horizontal ìsmearî of the eye signal at the 50% level, where the leading and trailing edges of the signal cross (see Figure 8). To determine data rate, a counter may be used at 4.0 Mb/s if a sufficiently long data transmission is available. For 0.576 and 1.152 Mb/s, an oscilloscope and back to back packets are recommended to determine data rate.

For 0.576 and 1.152 Mb/s, there may be some implementations which use a digital synthesizer to generate the transmitter clock. In this case, there may be jitter of up to +/- 25 ns relative to an idealized reference clock. Typically, with a 40 MHz primary clock, the jitter would be +/- 12.5 ns from the synthesizer, and another 5 ns or so from the driver and LED.

The jitter may be measured indirectly by using a high speed photodiode and a digitizing oscilloscope to measure the variance in edge to edge delay. Configure the transmitter to repetitively send large (2kb) packets of data (approximately 2 ms), and trigger the oscilloscope on any rising optical edge. Capture a section of the waveform delayed from the reference edge by 1 to 31 times the bit period. Capture several hundred repetitions at each delay, and measure the spread in the edge locations. It is necessary to measure at several delays since any one delay might be a multiple of the clock synthesis cycle, and show artificially small jitter. Measurements at several prime intervals should be sufficient, e.g., at 3, 7 ,13 ,19, and 31 times the bit period. The jitter relative to a "reference" clock is one half of the worst case spread in the rising edges at each delay.

The jitter may also be measured relative to a reference clock generated with an analog phase locked loop with a tracking bandwidth of about 10 kHz, locked to the optical signal edges. In this case, the oscilloscope should be triggered on the reference clock edge, and several hundred optical signal edges should be collected. Adequate time must be allowed for the PPL to settle before collecting edges, so the oscilloscope trigger should be gated for several PLL time constants after the beginning of a packet.

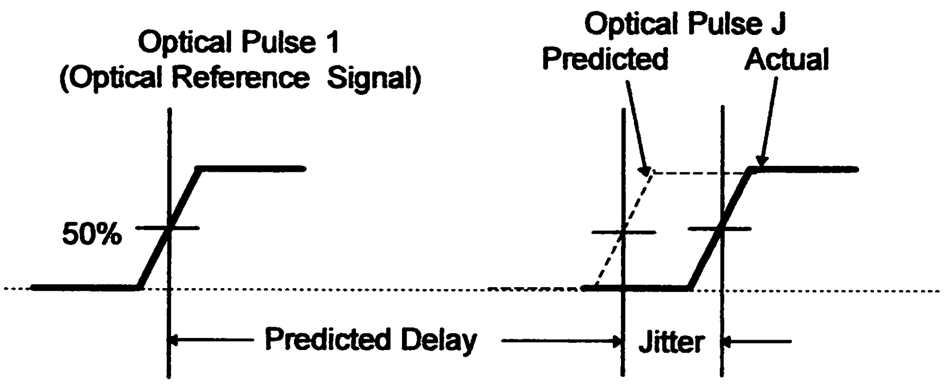


Figure 7. Pulse Delay and Jitter Definitions

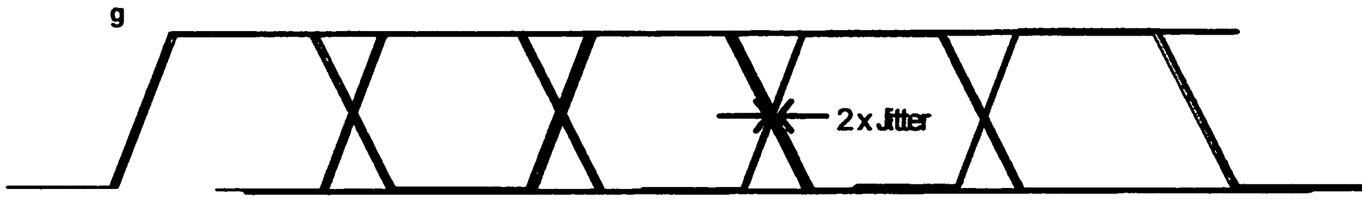


Figure 8. 4.0 Mb/s Jitter Definitions

A.3. Active Input Specifications

The following five specifications form a set which can be measured concurrently:

- Maximum Irradiance in Angular Range, mW/cm^2
- Minimum Irradiance in Angular Range, uW/cm^2
- Half-Angle, degrees
- Bit Error Ratio, (BER)
- Receiver Latency Allowance, ms

These measurements require an optical power source and means to measure angles and BERs. Since the optical power source must provide the specified characteristics of the Active Output, calibration and control of this source can use the same equipment as that required to measure the intensity and timing characteristics. BER measurements require access to the receiver's output. The latency test requires exercise of the node's transmitter to condition the receiver.

Definitions of the reference point, etc., are the same as for the Active Output Interface optical power measurements except that the test head is now an optical power source with the in-band characteristics (Peak Wavelength, Rise and Fall Times, Pulse Duration, Signaling Rate and Jitter) of the Active Output Interface. The optical power source also must be able to provide the maximum power levels listed in the Active Output Specifications. It is expected that the minimum levels can be attained by appropriately spacing the optical source from the reference point.

Figure 9 illustrates the region over which the Optical High State is defined. The receiver is operated throughout this region and BER measurements are made to verify the maximum and minimum requirements. The ambient conditions of A.1 apply during BER tests; BER measurements can be done with worst case signal patterns. Unless otherwise known, the test signal pattern should include maximum length sequences of "1"s (no light) to test noise and ambient, and maximum length sequences of "0"s (light) to test for latency and other overload conditions.

The minimum allowable intensity value is indicated by ìminimumî in Figure 9, since the actual specified value is dependent upon data rate.

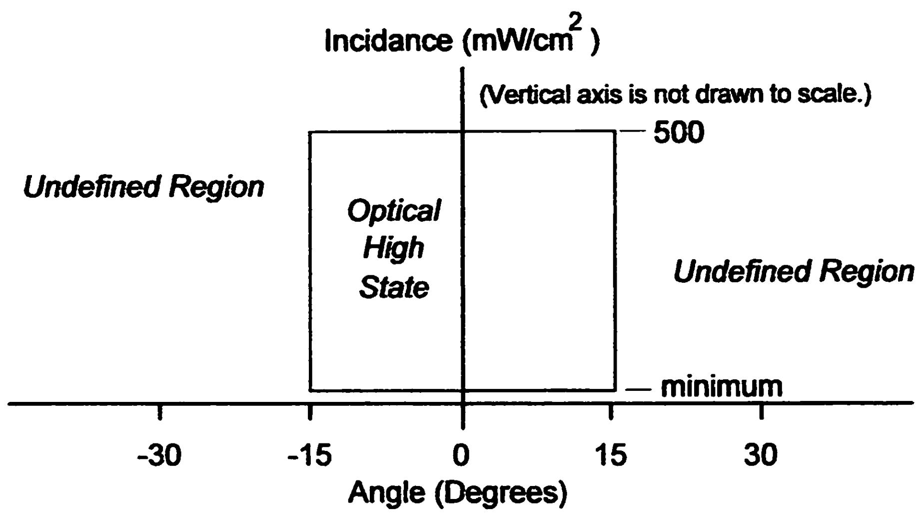


Figure 9. Optical High State Acceptable Range

Latency is tested at the Minimum Irradiance in Angular Range conditions. The receiver is conditioned by the exercise of its associated transmitter. For rates up to and including 1.152 Mb/s, the conditioning signal should include maximum length sequences of "0"s (light) permitted for this equipment. For 4.0 Mb/s 4PPM operation, various data strings should be used; the latency may be pattern dependent. The receiver is operated with the minimum irradiance levels and BER measurements are made after the specified latency period for this equipment to verify irradiance, half-angle, BER and latency requirements.

Appendix B. An Example of One End of a Link Implementation

(Note-Appendix B is Informative, not Normative {i.e., it does not contain requirements, but is for information only}. Specifications in Table 4 are derived from tables earlier in the document.

The link implementations in this appendix are examples only. All links must operate at 9.6 kb/s. The first example chosen is for a link which operates only up to 115.2 kb/s. Specifications are used as constraints, but all other parameters' values are calculated for the purpose of providing a more complete example. Operation at 1.152 Mb/s and 4.0 Mb/s are covered in Sections B.4.2. and B.4.3. respectively.

B.1. Definitions

UART - Universal Asynchronous Receiver/Transmitter: an electronic device/module that interfaces with a serial data channel.

B.2. Physical Representations

A block diagram of one end of an overall serial infrared link for data rates up to and including 115.2 kb/s is shown in Figure 10a. Figure 10b shows on overall configuration for a link supporting the lower speeds as well as 0.576 Mb/s, 1.152 Mb/s and 4.0 Mb/s.

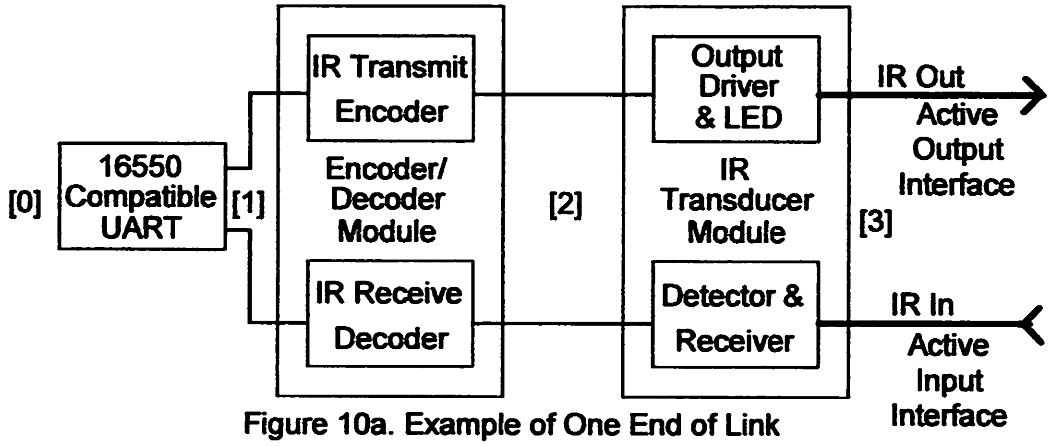


Figure 10a. Example of One End of Link
For Signaling Rates Up to & Including 115.2 kb/s

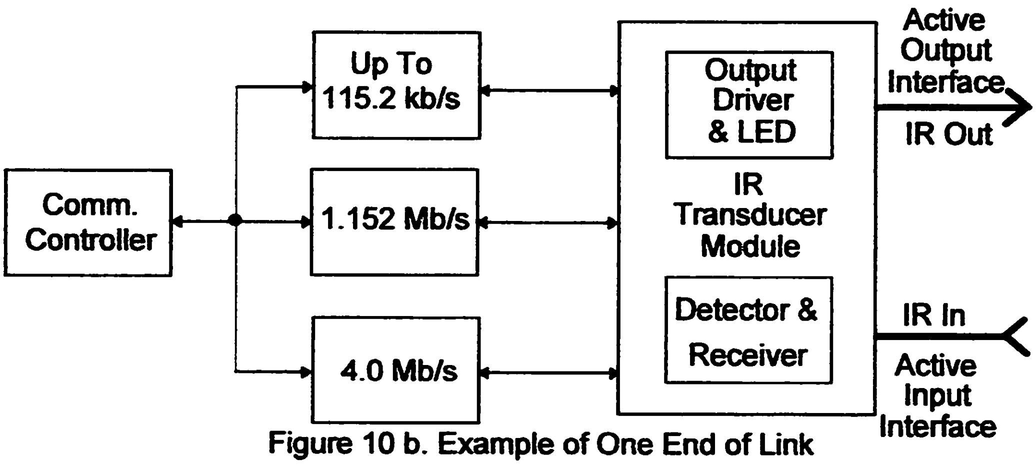


Figure 10 b. Example of One End of Link
For Signaling Rates Up to 4.0 Mb/s

B.3. Functionality & Electrical Waveforms-Data Rates Up to & Including 115.2 kb/s

In Figure 10a, the signal to the left of the UART [0] will not be discussed. The signal between the UART and the Encoder/Decoder [1] is a bit stream of pulses in a frame comprised a Start Bit, 8 Data Bits, no Parity Bit and ending with a Stop Bit, as shown in Figure 11a.

The signal at [2], between the Encoder/Decoder Module and the IR Transducer Module is shown in Figure 11b. The electrical pulses between the IR Transmit Encoder and the Output Driver & LED are 3/16 of a bit period in duration (or, for the slower signaling rates, as short as 3/16 of the bit period for 115.2 kb/s). Note that the IR Transmit Encoder and the Output Driver and LED pulses begin at the center of the bit period. The electrical pulses between the Detector & Receiver and the IR Receive Decoder are nominally of the same duration as those between the IR Transmit Encoder and the Output Driver & LED, but may be longer in some implementations. Thus, the electrical signals at [2] are analogs of the optical signals at [3]; an example of a nominal waveform is shown in Figure 11b. A "0" is represented by a pulse and a "1" is represented by no pulse.

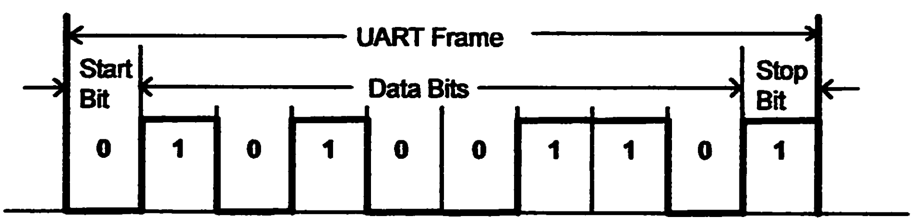


Figure 11a. UART Frame

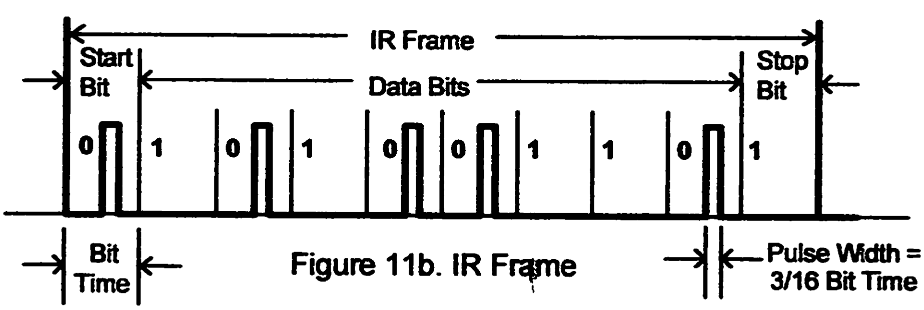


Figure 11b. IR Frame

B.4. Receiver Data and Calculated Performance

The definitions below refer to the parameters in Tables 4 through 7. The three segments of Table 4 appear in specifications in section 4 of the main body of this document. The analysis in Table 5 is for 115.2 kb/s operation, Table 6, for 1.152 Mb/s; Table 7 for 4.0 Mb/s.

LINK INTERFACE SPECIFICATIONS:

Signal Rate: The **Minimum** and **Maximum** limits define the acceptable limits for the clock.

Link Length: The link is specified to meet its **BER** specification within this specified **Minimum** to **Maximum** range. The assumption is that the source is positioned behind the **ACTIVE OUTPUT INTERFACE** by about 1.0 cm. Similarly, the detector is positioned behind the interface by about the same amount.

BER: This is the operating Bit Error Ratio for the overall link.

RECEIVER DATA (Not Interface Specifications):

Receiver Upper 3 dB Bandwidth, BWr: Used in the **Receiver Input Noise Current** and **Channel Response Time** calculations. The receiver will also have a Lower 3 dB Bandwidth limit to reduce interference from the sun and modulated fluorescent light optical noise sources.

Noise Current: Defines the receiver input noise current magnitude. This is calculated assuming an equivalent flat noise spectrum.

Detector Responsivity: Used to calculate the conversion of input optical **Irradiance** to the corresponding signal and noise currents.

Ambient Sunlight Irradiance: This is the sunlight level that is used in the calculation of Required Internal Detector Threshold Level. The sunlight causes a steady current to flow in the detector (e.g., a photodiode). The level of the current may be calculated using **Detector Responsivity**. As this current flows through the detector a shot noise is produced. This sunlight induced shot noise must be combined with the **Receiver Input Noise Current** to determine the **Required Internal Detector Threshold Level** for the specified **BER**.

Internal Threshold Level For EMI Immunity: Set high enough to avoid **BER** degradation due to a prescribed 3 V/m external EMI test level.

CALCULATED PERFORMANCE:

Receiver Input Noise Current and **Sunlight Ambient Noise Current** are rms added to give the **Total Receiver rms Noise Current**. This value is used with the specified link **BER** and the related Gaussian **Signal/Noise** ratio to calculate the **Required Internal Detector Threshold Level**. In general, the receiver frequency response will be shaped to minimize interference.

Specified Minimum Irradiance In Angular Range: This is the **MINIMUM** received optical irradiance level defined by the **ACTIVE INPUT INTERFACE** specification.

Received Minimum Irradiance Signal: Calculated from the **Minimum Intensity In Angular Range** and the **Link Optical Attenuation**. This value must be greater than the **Specified Minimum Irradiance In Angular Range**.

Received Minimum Detected Current: This is calculated from the product of the **Received Minimum Irradiance Signal** and the **MINIMUM Detector Responsivity**.

Defined Detection Threshold: This is the larger of the **Internal Threshold Level For EMI Immunity** and the **Required Internal Detector Threshold Level**.

Link Optical Loss Margin: The ratio in dB of the **Received Minimum Detected Current** and the **Defined Detection Threshold**. A viable technology implementation must yield a positive margin.

Detector Relative Loss At Wavelengths: This accounts for the roll-off in photo detector responsivity with increased wavelength. The **Link Optical Loss Margin** must exceed this value for a particular source wavelength.

Link Optical Attenuation: Calculated from the **Link Length** range.

Specified Receiver Optical Dynamic Range: Calculated from the ratio in dB of the **Maximum Irradiance In Angular Range** and the **Minimum Irradiance In Angular Range**.

Channel Response Times: Calculated from the **Optical Response Times** and the **Receiver Upper 3 dB Bandwidth**. These values are used in a Gaussian response time analysis to determine if there is a **Center-Of-The-Eye Penalty**.

ACTIVE OUTPUT SPECIFICATIONS	Data Rates	Minimum	Maximum
Peak Wavelength, Up, um	All	0.85	0.90
Maximum Intensity In Angular Range, mW/Sr	All	-	500
Minimum Intensity In Angular Range, mW/Sr	115.2 kb/s & below	40	-
	Above 115.2 kb/s	100	-
Half-Angle, degrees	All	+/-15	+/-30
Signaling Rate (also called Clock Accuracy)	All	See Table 1	See Table 1
Rise Time Tr & Fall Time Tf, 10-90% , ns	115.2 kb/s & below	-	600
	Above 115.2 kb/s	-	40
Optical Over Shoot, %	All	-	25
Pulse Duration	All	See Table 1	See Table 1
Edge Jitter, % of nominal bit duration	115.2 kb/s & below	-	+/-2.3
Jitter Relative to Reference Clock, % of nominal bit duration	0.576 &1.152 Mb/s	-	+/-2.9
Edge Jitter, % of nominal chip duration	4.0 Mb/s	-	+/-4.0
ACTIVE INPUT SPECIFICATIONS		-	-
Maximum Irradiance In Angular Range, mW/cm^2	All	-	500
Minimum Irradiance In Angular Range, uW/cm^2	115.2 kb/s & below	4.0	-
	Above 115.2 kb/s	10.0	-
Half-Angle, degrees	All	+/-15	-
Receiver Latency Allowance, ms	All	-	10
LINK INTERFACE SPECIFICATIONS			
Signaling Rate (also called Clock Accuracy)	All	See Table 1	See Table 1
Minimum Link Length, m	All	0	0
Maximum Link Length, m	All	1	-
Bit Error Ratio, BER	All	-	10^-8
Receiver Latency Allowance, ms	All	-	10

Table 4. Serial Infrared Specifications

B.4.1. 115.2 kb/s Implementation Example

RECEIVER DATA (Not Interface Specifications)	Minimum	Maximum
Receiver Upper 3 dB Bandwidth BWr, kHz	-	300
Receiver Input Noise Current, pA/(BWr)^0.5	-	11
Detector Responsivity, uA/(mW/cm^2)	100	160
Ambient Sunlight Irradiance, mW/cm^2	-	0.5
Ambient Fluorescent Irradiance, mW/cm^2	-	0.3
Set Detection Threshold For EMI Margin, nA	100	-
CALCULATED PERFORMANCE		
Receiver Input Noise Current, nA	-	6.02
Sunlight Ambient Noise Current, nA	-	2.19
Total Receiver rms Noise, nA	-	6.41
Specified Signal/Noise Ratio For BER	11.2	-
Required Detection Threshold With No EMI, nA	71.8	-
Received Minimum Detected Current, nA	400	-
Set Detection Threshold, nA	100	-
EMI Noise Threshold Margin, dB	1.44	-
Optical Loss Margin With No Eye Penalty, dB	6.02	-
Detector Relative Loss At Wavelengths, dB	0.33	1.24
Link Optical Attenuation, dB	-	40.0
Specified Receiver Optical Dynamic Range, dB	51.0	-
Channel Response Time, us	-	1.31
Center-Of-The-Eye Loss, dB	-	1.06
Total Optical Link Margin, dB	4.96	-

Table 5. Receiver Data and Calculated Performance
For Signaling Rates Up to and Including 115.2 kb/s

B.4.2. 1.152 Mb/s Implementation Example

RECEIVER DATA (Not Interface Specifications)	MIN	MAX
Receiver Lower & Upper 3 dB Bandwidth, BWrl & BWru, MHz	0.1	3.0
Receiver Input Noise Current, pA/(BWr)^0.5	-	10
Detector Responsivity, uA/(mW/cm^2)	75	-
Inband Ambient Sunlight Irradiance, mW/cm^2	-	0.5
Set Detection Threshold for EMI Margin, nA	200	-
CALCULATED PERFORMANCE		
Receiver Input Noise Current, nA	-	17.3
Sunlight Ambient Noise Current, nA	-	7.0
Total Receiver rms Noise, nA	-	18.7
Specified Signal/Noise Ratio For BER	12	-
Required Detection Threshold With No EMI, nA	224.2	-
Received Minimum Detected Current, nA	750	-
Set Detection Threshold, nA	400	-
EMI Noise Threshold Margin, dB	2.51	-
Optical Loss Margin With No Eye Penalty, dB	2.73	
Detector Relative Loss At Wavelengths, dB	-	1.24
Link Optical Attenuation, dB	-	40
Specified Receiver Optical Dynamic Range, dB	47	-
Channel Response Time, ns	-	171
Center-Of-The-Eye Loss, dB	-	0.6
Total Optical Link Margin, dB	1.37	-

Table 6. Receiver Data and Calculated Performance for 1.152 Mb/s

B.4.3. 4.0 Mb/s Implementation Example

RECEIVER DATA (Not Interface Specifications)	MIN	MAX
Receiver Lower & Upper 3 dB Bandwidth, BWrl & BWru, MHz	0.1	4.20
Receiver Input Noise Current, pA/(BWr)^0.5	-	10
Detector Responsivity, uA/(mW/cm^2)	75	116
Inband Ambient Sunlight Irradiance, mW/cm^2	-	0.5
Set Detection Threshold for EMI Margin, nA	400	-
CALCULATED PERFORMANCE		
Receiver Input Noise Current, nA	-	20.25
Sunlight Ambient Noise Current, nA	-	7.01
Total Receiver rms Noise, nA	-	21.43
Specified Signal/Noise Ratio For BER	11.2	-
Required Detection Threshold With No EMI, nA	240.1	-
Received Minimum Detected Current, nA	750	-
Set Detection Threshold, nA	400	-
EMI Noise Threshold Margin, dB	2.22	-
Optical Loss Margin With No Eye Penalty, dB	2.73	
Detector Relative Loss At Wavelengths, dB	0.33	1.24
Link Optical Attenuation, dB	-	40.0
Specified Receiver Optical Dynamic Range, dB	44.8	-
Channel Response Time, ns	-	92.4
Center-Of-The-Eye Loss, dB	-	0.75
Eye Opening Penalty, dB	-	0.61
Total Optical Link Margin, dB	1.37	-

Table 7. Receiver Data and Calculated Performance for 4.0 Mb/s