INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S - 1
KONSENTRASI TEKNIK ELEKTRONIKA

PERANCANGAN DAN PEMBUATAN ALAT PENDETEKSI LEVEL AIR RADIATOR DENGAN KELUARAN SUARA PADA MOBIL MENGGUNAKAN MIKROKONTROLLER AT89C51

SKRIPSI

Disusun oleh :

ANTON KUSWORO
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APRIL 2005

LEMBAR PERSETUJUAN

PERANCANGAN DAN PEMBUATAN ALAT PENDETEKSI LEVEL AIR RADIATOR DENGAN KELUARAN SUARA PADA MOBIL MENGGUNAKAN MIKROKONTROLLER AT89C51

SKRIPSI

Disusun dan Diajukan untuk Melengkapi dan Memenuhi Syarat Guna Mencapai Gelar Sarjana Teknik

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Dipertahankan di hadapan majelis penguji Skripsi jenjang Strata satu (S-1) pada :

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Salam damai dariku untuk : Persikmania (apapun kondisi Persik kita harus tetap dukung Persik 100%), **Interisti** (kita mengalami masa-masa sulit beberapa tahun ini, kita sedang diuji apakah kita ini merupakan Interisti sejati atau bukan), **Helloween mania** (pumpkin rule!!! mari kita nantikan Keeper 3, penasaran kan? aku juga) & **penggemar metal** (metal will never die!!!), **Otaku** (ada yang bisa buat manga dengan benar? ajarin donk), **komikus Indonesia** (maju terus kita hidupkan lagi komik Indonesia). Untuk **Duelist sejati** (siapkan deck terbaikmu aku menantimu hehehe)

Wassalamualaikum Wr. Wb.

ABSTRAKSI

Anton Kusworo, 2005, **Perancangan dan pembuatan alat pendeteksi level air radiator dengan keluaran suara pada mobil menggunakan mikrokontroller AT89C51,** Teknik Elektro S-1/ Teknik Elektronika, Fakultas Teknologi Industri, Institut Teknologi Nasional Malang.
Dosen Pembimbing I : Ir. F. Yudi Limpraptono, MT
Dosen Pembimbing II : I Komang Somawirata, ST

Kata Kunci : Radiator mobil, *Microcontroller AT89C51.*

Dalam skripsi ini dibahas suatu perancangan dan pembuatan alat pendeteksi air radiator dengan keluaran suara pada mobil menggunakan mikrokontroller AT89C51. Dengan menggunakan sistem pengontrolan digital mikrokontroller ini diharapkan dapat membuat suatu sistem pengontrolan yang otomatis dan efisien.

Mikrokontroler AT89C51 merupakan pengolah utama. Sistem akan membaca level air dengan elektrode (berlogika 1 jika terkena air dan 0 jika tidak terkena air) juga akan membaca kondisi suhu air. Sebagai keluaran adalah ISD yang mengeluarkan suara peringatan sesuai dengan level air yang dibaca. Saat level air 100% ISD mengeluarkan suara peringatan "air radiator penuh", saat level air 50% ISD mengeluarkan suara peringatan "air radiator berkurang banyak segera lakukan pengisian air" dan saat level air 40% sampai 0% ISD mengeluarkan suara peringatan "air radiator hampir habis segera lakukan pengisian air jika tidak dalam waktu 1 menit mesin mati". Untuk level air 90% sampai 60% tidak ada peringatan suara. Keluaran yang lain adalah LCD untuk menampilkan level air dan kondisi suhu air.

Dari hasil pengujian didapatkan bahwa sensor level, sensor suhu, penguat op –amp dan rangkaian ADC 0809 dapat bekerja dengan baik dan akurat. Hal ini dibuktikan dengan rata-rata kesalahan untuk sensor suhu tanpa penguatan sebesar 2,03%. Untuk rata-rata kesalahan penguat op-amp sebesar 1,13%. Dan untuk rata-rata kesalahan rangkaian ADC 0809 sebesar 0%. Dengan rata-rata kesalahan yang kecil alat dapat bekerja dengan baik dan menghasilkan keluaran sesuai dengan yang diinginkan.

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Penyusun

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BAB I

PENDAHULUAN

1.1 Latar Belakang

Perkembangan ilmu pengetahuan dan teknologi pada saat ini semakin berkembang dengan pesat seiring dengan perkembangan jarr an terutama dibidang elektronika. Salah satu perkembangan yang paling menonjol saat ini adalah perkembangan di bidang komputer selain itu adanya perkembangan teknologi *robotic*. Suatu sistem yang ditangani oleh komputer , semuanya akan terasa lebih cangih, lebih pintar, lebih otomatis dan lebih praktis serta efisien.

Sistem yang berkembang sekarang adalah sistem pengontrolan digital. Salah satu elemen sistem kontrol yang banyak dipakai yaitu *microcontroller*. Yaitu sebuah komponen elektronika yang dapat bekerja sesuai dengan program yang diisikan ke dalam memorinya seperti layaknya sebuah komputer yang sangat sederhana. Penggunaan *microcontroller* telah cukup meluas pada berbagai aplikasi mulai dari elektronik, *robotic*, kendali industri dan lain-lain.

Microcontroller digunakan untuk menggantikan pekerjaan manusia yang menggunakan cara manual dan tidak efisien. Misalnya pengisian radiator pada mobil sekarang ini masih menggunakan cara manual yaitu dengan mengecek radiator tersebut untuk melihat radiator tersebut sudah kosong atau masih penuh.

Jadi untuk keamanan, pengemudi setiap akan menggunakan mobil terlebih dahulu mengecek radiator tersebut.

Untuk mengatasi masalah di atas diperlukan suatu alat pendeteksi level air radiator secara otomatis dimana jika isi air pada radiator penuh (100%) maka alat akan bekerja yaitu megeluarkan suara (air radiator penuh), jika tinggal setengah (50%) maka alat akan bekerja yaitu mengeluarkan suara (air radiator berkurang banyak segera lakukan pengisian air pada radiator). Dan apabila isi radiator hampir habis sampai habis (40% sampai 0%) maka alat akan bekerja yaitu mengeluarkan suara (air radiator hampir habis segera lakukan pengisian air pada radiator jika tidak dalam waktu 1 menit mesin mati). Alat ini juga dilengkapi dengan pendeteksi suhu yang digunakan untuk mengetahui suhu air di dalam radiator. Dengan memanfaatkan teknologi elektronika, maka direncanakan suatu alat pendeteksi level radiator secara otomatis menggunakan mikrokontroller AT89C51.

1.2. Rumusan Masalah

Berdasarkan latar belakang yang telah diuraikan pada bagian sebelumnya, maka permasalahannya adalah :

- Bagaimana merencanakan dan membuat suatu alat yang dapat menggantikan cara *manual* untuk mendeteksi level radiator secara otomatis.
- Bagaimana membuat perangkat lunak yang dapat menghasilkan pengendalian yang mendukung perangkat keras sehingga diperoleh tujuan yang diinginkan.

Sehubungan dengan permasalaahan diatas, maka dalam skripsi ini dipilih judul :

"PERANCANGAN DAN PEMBUATAN ALAT PENDETEKSI LEVEL AIR RADIATOR DENGAN KELUARAN SUARA PADA MOBIL MENGGUNAKAN MIKROKONTROLLER AT89C51"

1.3. Tujuan

Penulisan Skripsi ini bertujuan untuk merancang dan membuat alat yang mampu mendeteksi level radiator dan akan mengeluarkan suara (peringatan). Juga dilengkapi dengan pendeteksi suhu radiator.

1.4. Batasan Masalah

Dalam menyusun tugas akhir ini diperlukan suatu batasan masalah agar tidak menyimpang dari ruang lingkup yang akan dibahas. Adapun batasan masalahnya:

1. Alat ini menggunakan sensor level yaitu elektrode dan sensor suhu yang dikendalikan oleh mikrokontroller AT89C51.
2. Tidak dapat mendeteksi kisi – kisi yang tersumbat.
3. Hanya membahas masalah perancangan perangkat kerasnya, sedangkan perangkat lunaknya hanya dibahas secara garis besarnya.
4. Alat yang dibuat nantinya hanya berupa model bukan barang yang sesungguhnya dan tidak membahas mekanisme mesin.
5. Tidak membahas catu daya.

1.5 Metodologi

Metodologi penelitian yang dipakai dalam pembuatan tugas akhir ini adalah:

1. Study literatur
2. Perancangan dan Pembuatan alat
3. Pelaksanaan uji coba alat
4. Penyusunan laporan tugas akhir

1.6 Sistematika Penulisan

Penulisan tugas akhir ini terbagi menjadi lima bab dengan sistematika sebagai berikut:

BAB I PENDAHULUAN

Berisi latar belakang, rumusan masalah, tujuan, batasan masalah, metodologi, dan sistematika penulisan.

BAB II TEORI PENUNJANG

Membahas teori – teori dasar penunjang perancangan dan pembuatan alat.

BAB III PERANCANGAN DAN PEMBUATAN ALAT

Membahas tentang perancangan alat baik perangkat keras maupun perangkat lunak dan cara kerja blok diagram.

BAB IV PENGUJIAN ALAT

Mencakup pembahasan tentang proses pengujian alat yang terdiri dari peralatan yang digunakan, langkah kerja, dan analisa hasil pengujian.

BAB V PENUTUP

Berisi kesimpulan dan saran.

BAB II

TEORI PENUNJANG

2.1. Mikrokontroler AT 89C51

Perbedaan mendasar antara mikrokontroler dan mikroprosesor adalah mikrokontroler selain memiliki CPU juga dilengkapi memori dan *input output* yang merupakan kelengkapan sebagai sistem minimum mikrokomputer sehingga sebuah mikrokontroler dapat dikatakan sebagai mikrokomputer dalam keping tunggal *(Singge Chip Microcomputer)* yang dapat berdiri sendiri.

Mikrokontroler AT89C51 adalah mikrokontroler *ATMEL* yang kompatibel penuh dengan mikrokontroler keluarga *MCS* – 51, membutuhkan daya rendah, memiliki *performance* yang tinggi dan merupakan mikrokomputer 8 *bit* yang dilengkapi 4 *Kbyte* EEPROM *(Electrical Erasable and Programmable Read Only Memory)* dan 128 *Byte RAM internal.* Program memori yang dapat diprogram ulang dalam sistem atau menggunakan *programmer Nonvolalite Memory* konvensional.

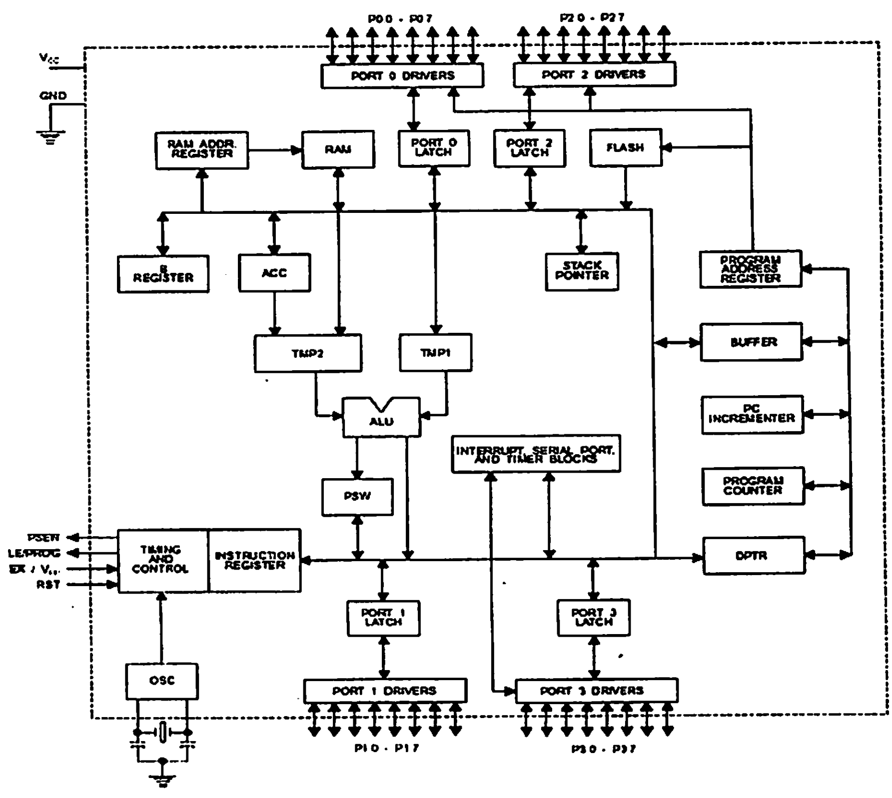
- **Spesifikasi Mikrokontroller AT89C51**

Mikrokontroler AT89C51 ini mempunyai spesifikasi yaitu sebagai berikut ini:

- CPU 8 bit yang dioptimasi untuk aplikasi kontrol
- *4Kbytes Flash Programmable and Erasable Read Only Memory* (PEROM)

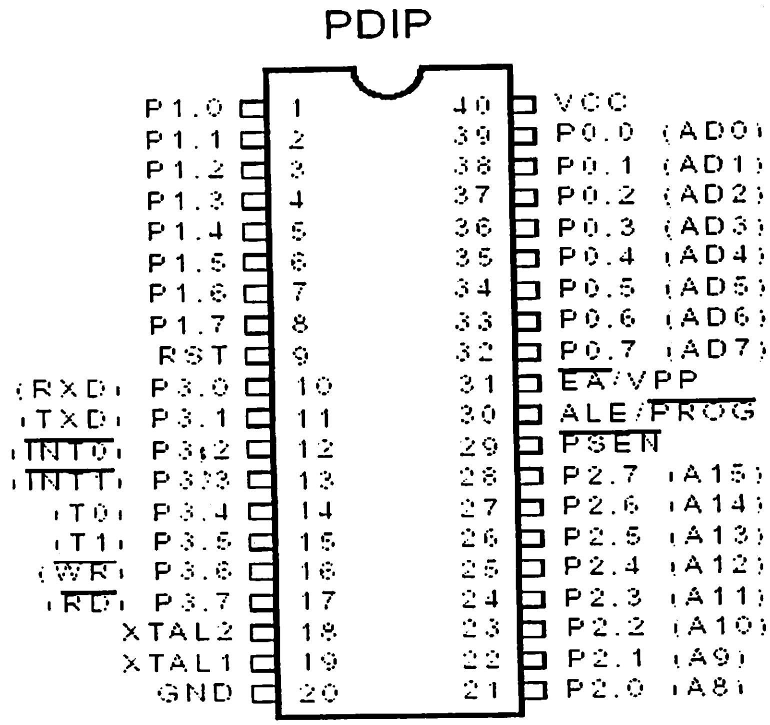
- 128 bytes *Internal* RAM
- 2 buah 16 bit *Timer / Counter*
- *Serial Port* yang dapat diprogram
- sumber *interupt* dengan 2 level prioritas
- *On-chip oscillator*
- 32 jalur *input output* yang dapat diprogram
- 64K Program *Memory*
- 64K Data *Memory*

Dengan keistimewaan diatas pembuatan alat menggunakan AT89C51 menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak. Adapun blok diagram dari Mikrokontroler AT89C51 adalah sebagai berikut :



Gambar 2-1. Blok Diagram Mikrokontroler AT89C51

- **Konfigurasi Pena-Pena Mikrokontroler AT89C51**



Gambar 2-2. Konfigurasi Pena-Pena AT89C51

Fungsi tiap *pin*-nya adalah sebagai berikut :

- VCC (Supply tegangan), *pin 40*
- GND (*Ground*), *pin 20*
- Port 0, *pin 32 – 39*

  Merupakan *port input-output* dua arah, tanpa *internal pull-up* dan konfigurasikan sebagai *multipleks bus* alamat rendah (A0 – A7) dan data selama pengaksesan program *memory* dan data *memory eksternal* *Port* 0 dapat berfungsi sebagai I/O biasa, *low order multiplex address/data* ataupun menerima kode *byte* pada saat *Flash Programming*

- Port 1, *pin 1 – 8*

  Merupakan *port input-output* dua arah dengan *internal pull-up. Port* 1 berfungsi sebagai I/O biasa atau menerima *low order address bytes* selama pada saat *Flash Programming. Port* ini mempunyai *internal pull up* dan berfungsi sebagai *input* dengan memberikan logika 1. Sebagai *output port* ini dapat memberikan *output sink* ke empat buah *input TTL.*

- Port 2, *pin 21 - 28*

  Merupakan *port input-output* dengan *internal pull-up.* Mengeluarkan alamat tinggi selama pengambilan program *memory external. Port* 2 berfungsi sebagai I/O biasa atau *high order address*, pada saat mengakses *memory* secara 16 *bit* (*Movx @Dptr*). Pada saat mengakses *memory* secara 8 *bit*, (*Mov @Rn*) port ini akan mengeluarkan isi dari *Port 2 Special Function Register. Port* ini mempunyai *internal pull up* dan berfungsi sebagai *input* dengan memberikan logika 1. Sebagai *output port* ini dapat memberikan *output sink* ke empat buah *input* TTL.

- Port 3, *pin 10 – 17*

  Merupakan *port input-output* dengan *internal pull-up*, dimana *Port* 3 juga memiliki fungsi khusus dan dapat dilihat pada tabel berikut ini:

Tabel 2-1.Fungsi Khusus Pada Port 3

Nama Penyemat	Fungsi Khusus
Port 3.0	RxD (Port masukan serial)
Port 3.1	TxD (Port keluaran Serial)
Port 3.2	/INTO (Masukan Interupsi Eksternal 0)
Port 3.3	/INT1 (Masukan Interupsi Eksternal 1)
Port 3.4	T0 (masukan pewaktu eksternal 0)
Port 3.5	T1 (masukan pewaktu eksternal 1)
Port 3.6	/WR (sinyal tulis memori data eksternal)
Port 3.7	/RD (sinyal baca memori data eksternal)

- RST (*Reset*), *pin 9*

  Input Reset merupakan *reset master* untuk AT89C51. *Reset* akan aktif dengan memberikan *input high* selama 2 *cycle*

- ALE / Prog (*Address Latch Enable*), *pin 30*

  Digunakan untuk menahan alamat memori *eksternal* selama pelaksanaan intruksi. *Pin* ini dapat berfungsi sebagai *Address Latch Enable* (ALE) yang me-*latch low byte address* pada saat mengakses memori eksternal. Sedangkan pada saat *Flash Programming* (PROG) berfungsi sebagai *pulse input* untuk. Pada operasi normal ALE akan mengeluarkan sinyal *clock* sebesar 1/16 frekwensi *oscillator* kecuali pada saat mengakses memori *eksternal*. Sinyal *clock* pada *pin* ini dapat pula di *disable* dengan men-set *bit* 0 dari Special *Function Register* di alamat 8EH. ALE hanya akan aktif pada saat mengakses memori *eksternal* (*MOVX & MOVC*).

- PSEN (*Program Strobe Enable*), *pin 29*

  Merupakan sinyal pengontrol yang memperbolehkan program memori *eksternal* masuk kedalam *bus*. *Pin* ini berfungsi pada saat mengeksekusi program yang terletak pada memori *eksternal*. *PSEN* akan aktif dua kali setiap *cycle*.

- EA / VPP (*External Access*), *pin 31*

  Dapat diberikan logika rendah (*Ground*) atau logika tinggi (+5V). Jika diberikan logika tinggi maka mikrokontroler akan mengakses program dari ROM *internal (EEPROM/Flash Memori)*, dan jika diberikan logika rendah maka mikrokontroler akan mengakses program dari memori *eksternal*. Pada saat *Flash Programming pin* ini akan mendapat tegangan 12 Volt (VP)

- X-TAL 1 dan X-TAL 2, *pin 19, 18*

  Pin ini dihubungkan dengan kristal bila menggunakan osilator *internal*. X-TAL 1 merupakan masukan ke rangkaian osilator *internal* sedangkan X-TAL 2 keluaran dari rangkaian osilator *internal* . Untuk keperluan ini diperlukan kapasitor penstabil sebesar 30pF. Dan nilai dari X-TAL tersebut antara 4 – 24 Mhz. Untuk lebih jelasnya dapat dilihat gambar pemasangan X-TAL serta kapasitor yang digunakannya.

alamat 8EH. ALE hanya akan aktif pada saat mengakses memori *eksternal* (*MOVX & MOVC*).

- PSEN (*Program Strobe Enable*), *pin 29*

  Merupakan sinyal pengontrol yang memperbolehkan program memori *eksternal* masuk kedalam *bus*. *Pin* ini berfungsi pada saat mengeksekusi program yang terletak pada memori *eksternal*. *PSEN* akan aktif dua kali setiap *cycle*.

- EA / VPP (*External Access*), *pin 31*

  Dapat diberikan logika rendah (*Ground*) atau logika tinggi (+5V). Jika diberikan logika tinggi maka mikrokontroler akan mengakses program dari ROM *internal (EEPROM/Flash Memori)*, dan jika diberikan logika rendah maka mikrokontroler akan mengakses program dari memori *eksternal*. Pada saat *Flash Programming pin* ini akan mendapat tegangan 12 Volt (VP)

- X-TAL 1 dan X-TAL 2, *pin 19, 18*

  Pin ini dihubungkan dengan kristal bila menggunakan osilator *internal*. X-TAL 1 merupakan masukan ke rangkaian osilator *internal* sedangkan X-TAL 2 keluaran dari rangkaian osilator *internal* . Untuk keperluan ini diperlukan kapasitor penstabil sebesar 30pF. Dan nilai dari X-TAL tersebut antara 4 – 24 Mhz. Untuk lebih jelasnya dapat dilihat gambar pemasangan X-TAL serta kapasitor yang digunakannya.

- **Struktur *Memory***

Organisasi memori pada mikrokontroler AT89C51 dapat dibagi menjadi dua bagian besar yaitu memori program dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpanan data maupun program. Memori program digunakan untuk menyimpan instruksi-instruksi yang akan dijalankan oleh mikrokontroler, sedangkan memori data digunakan sebagai tempat yang sedang di olah mikrokontroler.

Program mikrokontroler di simpan dalam memori program berupa *ROM.* Mikrokontroler 89C51 dilengkapi dengan *ROM internal*, sehingga untuk menyimpan program tidak digunakan *ROM eksternal* yang terpisah dari mikrokontroler. Agar tidak menggunakan memori program *eksternal*, penyemat/EA dihubungkan dengan *Vcc* (logika 1).

Memori program mikrokontroler menggunakan alamat 16 *bit* mulai 0000_H -$0FFF_H$, sehingga kapasitas penyimpanan program maksimal adalah 4Kb. Sinyal */PSEN* (*Program Store Enable*) tidak digunakan jika digunakan memori program *internal.*

Selain program mikrokontroler 89C51 juga memiliki data *internal* 128 *byte* dan mampu mengakses memori data *eksternal* sebesar 64 Kb. Semua memori data *internal* dapat dialamati dengan data langsung atau tidak langsung. Ciri dari pengalamatan langsung adalah *operand* adalah alamat *register* yang berisi alamat data yang akan diolah. Sebagian memori tersebut dapat dialamati dengan pengalamatan *register*, dan sebagian lagi dapat dialamati dengan memori satu *bit.*

Untuk membaca data digunakan sinyal /RD sedangkan untuk menulis digunakan sinyal /WR.

- **SFR (*Special Function Register*)**

Register Fungsi Khusus (*Special Function Register*) terletak pada 128 *byte* bagian atas memori data *internal* dan berisi *register-register* untuk pelayanan *latch port, timer*, program status *words*, kontrol *peripheral* dan sebagainya. Alamat *register* fungsi khusus ditunjukkan pada tabel 2-2.

Tabel 2-2. *Special Function Register*

Simbol	Nama Register	Alamat
ACC	Accumulator	$E0_H$
B	Register B	$F0_H$
PSW	Program Statut Word	$D0_H$
SP	Stack Pointer	81_H
DPTR	Data Pointer 2 Byte	
DPL	Bit rendah	82_H
DPH	Bit Tinggi	83_H
P0	Port 0	80_H
P1	Port 1	90_H
P2	Port 2	$A0_H$
P3	Port 3	$B0_H$
IP	Interupt Periority Control	$D8_H$
IE	Interupt Enable Control	$A8_H$
TMOD	Timer/Counter Mode Control	89_H
TCON	Timer/Counter Control	88_H
TH0	Timer/Counter 0 High Control	$8C_H$
TL0	Timer/Counter 0 Low Control	$8A_H$
TH1	Timer/Counter 1 High Control	$8D_H$
TL1	Timer/Counter 1 Low Control	$8B_H$
SCON	Serial Control	98_H
SBUF	Serial Data Buffer	99_H
PCON	Power Control	87_H

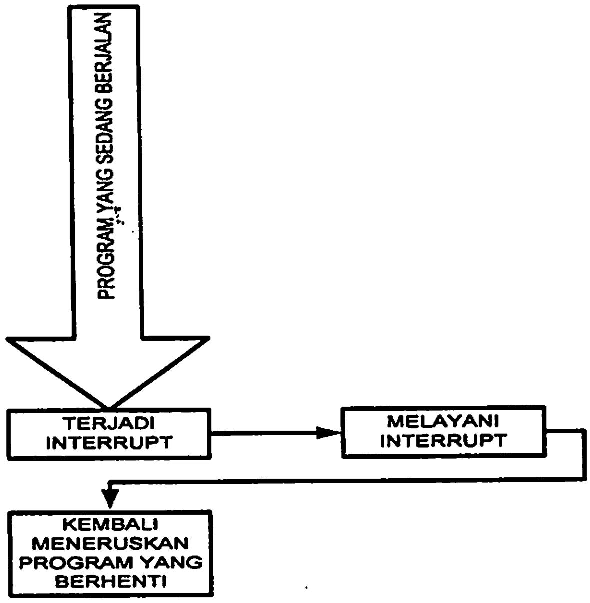
Beberapa macam *register* fungsi khusus yang sering digunakan adalah sebagai berikut ini :

- *Accumulator* (ACC) merupakan register untuk penambahan dan pengurangan. Perintah *mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register B* merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Stack Pointer* (SP) merupakan register 8 *bit* yang dapat diletakkan di alamat manapun pada *RAM internal*. Alamat *SP* ditambah / dinaikkan sebelum data disimpan pada eksekusi instruksi *PUSH* dan *CALL*. *SP* dapat diletakkan pada alamat manapun di *on-chip RAM*, *SP* diinisialisasi pada alamat 07H setelah *reset*. Hal ini mengakibatkan *stack* dimulai pada lokasi 08H.
- *Data Pointer* (DPTR) terdiri dari dua *register*, yaitu untuk *byte* tinggi (*Data Pointer High, DPH*) dan *byte* rendah (*Data Pointer Low, DPL*) yang berfungsi untuk mengunci alamat 16 *bit*.
- *Port 0* sampai *Port 3* merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada *port* 0, 1, 2, 3. Masing-masing *register* ini dapat dialamati per-*byte* maupun per-*bit*.
- *Control Register* terdiri dari *register* yang mempunyai fungsi kontrol. Untuk mengontrol sistem *interupsi*, terdapat dua *register* khusus, yaitu *register* IP (*Interupt Priority*) dan *register* IE (*Interupt Enable*). Untuk mengontrol pelayanan *timer/counter* terdapat *register* khusus, yaitu *register* TCON (*timer/counter control*) serta pelayanan *port serial* menggunakan *register* SCON (*Serial Port Control*).

- Sistem *Interupsi*

Interrupt adalah suatu kejadian atau peristiwa yang menyebabkan mikrokontroler berhenti sejenak untuk melayani interrupt tersebut. Program yang dijalankan pada saat melayani *interrupt* disebut *Interrupt Service Routine*. Analoginya adalah sebagai berikut, seseorang sedang mengetik laporan, mendadak telephone berdering dan menginterrupsi orang tersebut sehingga menghentikan pekerjaan mengetik dan mengangkat telephone. Setelah pembicaraan telephone yang dalam hal ini adalah merupakan analogi dari *Interrupt Service Routine* selesai maka orang tersebut kembali meneruskan pekerjaanya mengetik.

Demikian pula pada sistem mikrokontroler yang sedang menjalankan programnya, saat terjadi *interrupt*, program akan berhenti sesaat, melayani *interrupt* tersebut dengan menjalankan program yang berada pada alamat yang ditunjuk oleh vektor dari *interrupt* yang terjadi hingga selesai dan kembali meneruskan program yang terhenti oleh *interrupt* tadi. Seperti yang terlihat pada gambar 2-3. berikut ini :



Gambar 2-3. Proses *Interrupsi*

Proses yang dilakukan oleh mikrokontroler saat melayani *interrupt* adalah sebagai berikut:

- Instruksi terakhir yang sedang dijalankan diselesaikan terlebih dahulu
- Program *Counter* (alamat dari instruksi yang sedang berjalan) disimpan ke *stack*
- *Interrupt* Status disimpan secara *internal*
- *Interrupt* dilayani sesuai peringkat dari *interrupt* (lihat *Interrupt Priority*)
- Program *Counter* terisi dengan alamat dari vector *interrupt* (lihat *Interrupt Vector*) sehingga mikrokontroler langsung menjalankan program yang terletak pada *vector interrupt*

Program pada vector *interrupt* biasanya diakhiri dengan instruksi *RETI* di mana pada saat ini proses yang terjadi pada mikrokontroler adalah sebagai berikut:

- Program *Counter* diisi dengan alamat yang tersimpan dalam stack pada saat *interrupt* terjadi sehingga mikrokontroler kembali meneruskan program di lokasi saat *interrupt* terjadi
- *Interrupt* Status dikembalikan ke kondisi terakhir sebelum terjadi *interrupt*

■ ***Timer / Counter***

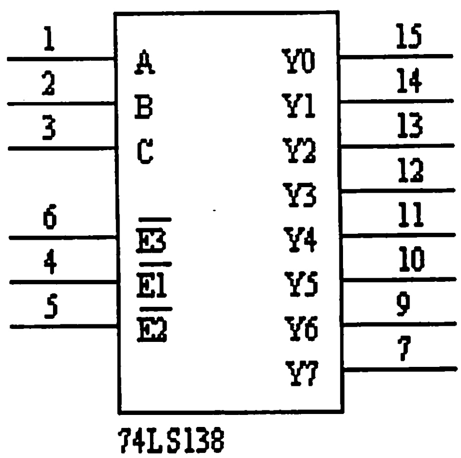
Mikrokontroler 89C51 mempunyai 2 buah *register timer / counter* 16 *bit* : *Timer* 0 dan *Timer* 1. Keduanya dapat beroperasi sebagai *timer* atau *counter.* Pada fungsi *'timer',* isi *register* ditambah satu setiap siklus mesin. Jadi, seperti menghitung siklus mesin. Karena satu siklus mesin terdiri dari 12 periode osilator, maka kecepatannya = 1/12 frekuensi osilator. Pada fungsi *'counter',* isi *register* ditambah satu setiap terjadi *transisi* 1 ke 0 pada pin *input* eksternal yang bersesuaian T0 atau T1. Untuk mengenali *transisi* 1 ke 0 ini dibutuhkan 2 siklus mesin (24 periode osilator), maka *input* maksimum ialah 1/24 frekuensi osilator. Tidak ada batasan untuk *duty cycle* sinyal *input. Timer* 0 dan *Timer* 1 mempunyai 4 mode operasi yang bisa dipilih.

2.2. Address Decoder

Sistem berbasis mikroprosesor atau mikrokontroler pada umumnya mempunyai lebih dari satu *device / peripheral* seperti memori, *input output, Analog to Digital Converter* (ADC), dan lain-lain. Masing-masing *device* ini perlu diberi alamat, sama seperti rumah kita yang mempunyai alamat unik untuk tiap-tiap rumah.. Demikian pula dengan mikrokontroler, supaya dapat mengakses suatu *device* maka mikrokontroler tersebut harus punya alamat *device* yang akan diakses. *Address decoder* akan memberikan alamat untuk tiap *device.*

- **IC 74LS138**

IC ini merupakan rangkaian *decoder* yang memiliki tiga masukan dan delapan keluaran. Dari *decoder* ini maka dapat ditemukan alamat *input decoder,* yaitu A15, A14, A13, gambar rangkaian *decoding* ditunjukan pada gambar dibawah. Tujuan dari IC *decoding* ini adalah untuk menghindari kemungkinan terjadinya pemakian *bus* dari sumber yang berbeda pada saat yang bersamaan. Sehingga dengan adanya IC *decoder* ini, memori atau komponen ya ıg lain dapat diaktifkan secara bergantian.

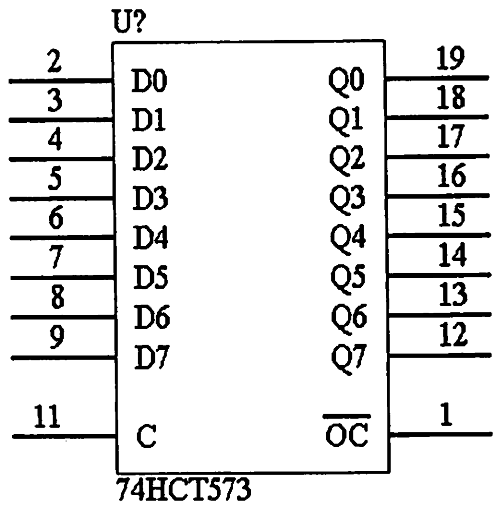


Gambar 2-4. IC 74LS138

2.3. IC 74HC573

IC 74HC573 ini berfungsi sebagai data *latch,* IC ini memiliki kecepatan yang tinggi dalam pengiriman data dan memerlukan daya yang rendah. IC ini memiliki dua puluh dua buah *pin* yang terdiri dari delapan buah *pin* masukan (D0-

D7), sebuah masukan *Latch Enable* (LE) yang aktif *high*, sebuah masukan *clock* (CP) yang aktif *high*, sebuah *output enable* (OE) yang aktif *low* dan delapan buah keluaran (O0-O7).



Gambar 2-5. IC 74HC573

2.4. Memori

Memori dalam suatu sistem mikrokontroler merupakan suatu piranti yang berfungsi untuk menyimpan program dan data yang dibutuhkan oleh mikrokontroler. Memori secara garis besar dibagi menjadi dua macam yaitu memori yang hanya dapat dibaca (*Read only memory*) dan memori yang dapat dibaca maupun ditulisi (*Random Access memory*).

a. Read Only Memory (ROM)

ROM adalah suatu bentuk memori yang hanya dapat dibaca isinya. Isi ROM tidak mudah dihapus atau tidak mudah hilang meskipun catu daya tidak diberikan padanya. Karena sifatnya yang tidak mudah dihapus tersebut ROM disebut juga memori *non volatile* (Tidak mudah menguap). Suatu program atau data statis yang diinginkan agar tidak mudah hilang dapat disimpan dalam ROM. Menurut sifatnya ROM dapat dibagi menjadi beberapa macam, yaitu :

- PROM (*Programmable Read Only Memory*) yaitu jenis ROM yang sekali ditulisi dan tidak dapat dihapus kembali.
- EPROM (*Erasable Programmable Read Only Memory*) yaitu jenis ROM yang dapat ditulisi maupun dihapus kembali. Menurut cara penghapusannya EPROM dapat dibagi menjadi dua yaitu UV-EPROM (*Ultra Violet* EPROM) dan EEPROM (*Electrically* EPROM).

b. RAM (*Random Access Memory*)

RAM adalah memori yang dapat dibaca maupun ditulisi. Menurut sifatnya RAM biasa disebut sebagai memori yang mudah menguap (*volatile*), yaitu bila catu daya yang diberikan pada RAM dihilangkan, maka data pada RAM akan hilang. Ada dua macam RAM yaitu :

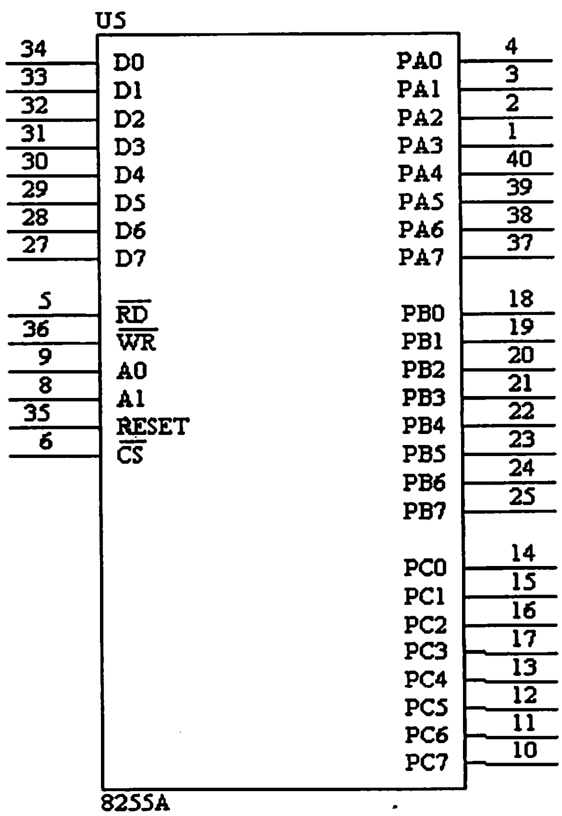
- RAM statik yaitu RAM yang tersusun atas flip-flop. Selama catu daya diberikan pada RAM, maka data akan tetap tersimpan.
- RAM dinamik yaitu RAM yang menggunakan kapasitor sebagai penyimpan data. RAM ini memerlukan penyegaran data karena sifat kapasitor dapat menurun muatannya.

2.5. PPI 8255

- **Blok Diagram**

Programmable Peripheral Interface (PPI) 8255 merupakan perangkat I/O multiguna yang dapat diprogram dan berfungsi untuk mengantarkan perangkat luar yang dikendalikan oleh *bus* sistem mikrokontroler

PPI 8255 ini memiliki 24 jalur I/O yang terbagi menjadi 3 *port* (*port* A, *port* B, dan *port* C) dan tiga jalur *mode* operasi (*mode* 0, *mode* 1, dan *mode* 2). Konfigurasi dari fungsi dari masing-masing *port* diprogram dengan perangkat lunak. Berikut ini adalah blok diagram dari PPI 8255.



Gambar 2-6. IC PPI 8255

Difinisi *Pin* dari PPI adalah :

D0 – D7 : *Bus* data yang berfungsi sebagai sarana berhubungan antara mikrokontroler dengan PPI.

$\overline{RD}$: *Pin* aktif rendah yang berfungsi untuk membaca data dari *port* PPI, yang kemudian ditransfer ke data *bus* mikrokontroler.

$\overline{WR}$: Berfungsi untuk menuliskan data dari *bus* mikrokontroler menuju ke *port* PPI.

A1, A0 : Merupakan alamat PPI, yang menentukan *port* PPI yang dipilih.

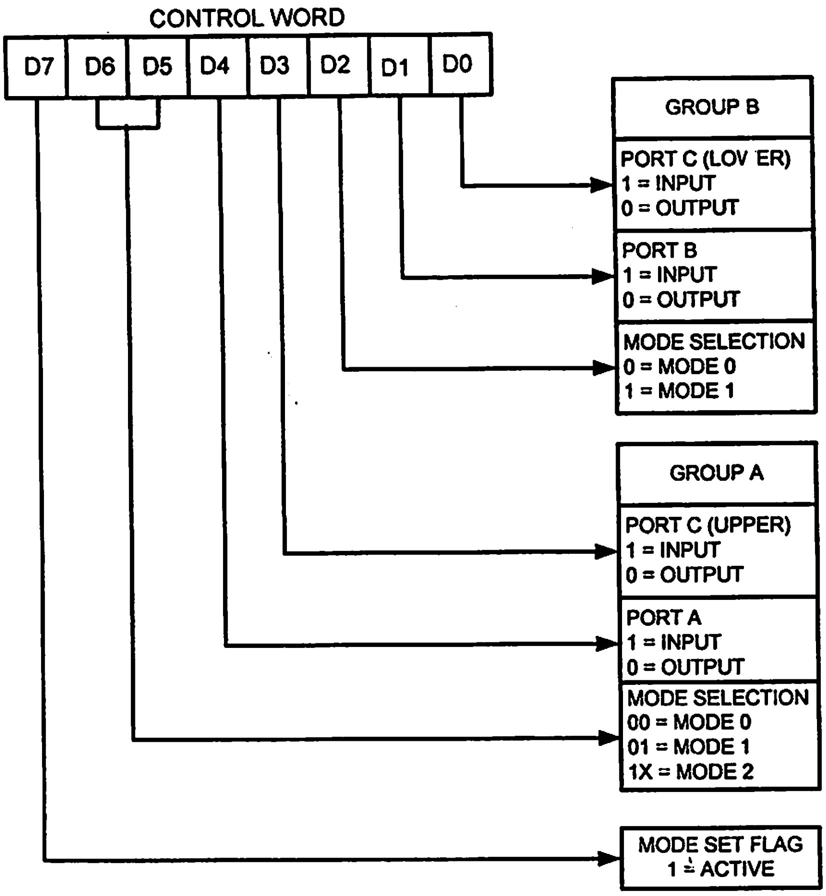
Reset : *Pin* yang berfungsi untuk mereset PPI.

$\overline{CS}$: *Pin* yang berfungsi untuk membuat aktif atau tidaknya PPI.

PA, PB, PC : 3 port parallel PPI, tiap-tiap *port* terdiri dari 8-*bit*, dan dapat digunakan sebagai *input* atau *output*.

- **Inisialisa PPI**

Sebelum dijalankan PPI harus diinisialisasi terlebih dahulu untuk bisa berkomunikasi dengan peralaatan yang lain. Berikut ini contoh suatu format dari mode kata kontrol jika A0 A1 = 11, maka fungsi dari setiap *bit* suatu kata kontrol terbagi seperti gambar berikut :



Gambar 2-7. Contoh Inisialisasi PPI 8255

2.6. ADC (*Analog To digital Converter*)

Mikrokontroler hanya dapat mengolah (memproses) data dalam bentuk *biner* saja, atau lebih sering disebut *digital*, oleh sebab itu setiap data *analog* yang akan diproses oleh mikrokontroler harus dirubah terlebih dahulu kedalam bentuk kode *biner* (*digital*). Jadi untuk menghubungkan sistem *analog* yang ada diluar mikrokontroler ke dalam mikrokontroler, dibutuhkan suatu pengubah atau konversi *analog* ke *digital*.

Fungsi dasar dari pengubah *analog* ke *digital* adalah mengubah tegangan *analog* kedalam bentuk kode-kode *biner* (*digital*) sehingga dapat diproses oleh mikrokontroler. Tegangan *analog* yang merupakan masukan dari ADC yang berasal dari pengondisi arus, rangkaian ini mempunyai *range* tertentu dan disebut *analog*. Kode *biner* hasil konversi ini dipakai data untuk diolah oleh mikrokontroler yang kemudian ditampilkan pada *output*.

Pengubah *analog* ke *digital* merupakan jantung dari sistem data akuisisi yang berfungsi mengubah data dalam bentuk kontinyu kedalam *digital* yang *diskrit*, sehingga cocok untuk diproses oleh mikrokontroler. ADC lebih banyak variasi bentuknya bila dibandingkan dengan DAC. Karena dalam ADC karakteristik yang dibutuhkan jauh lebih banyak.

Ada beberapa faktor yang perlu diperhatikan dalam pemilihan komponen ADC, antara lain :

- ***Resulotion* (Resolusi)**

Merupakan spesifikasi terpenting untuk ADC, yaitu jumlah langkah dari sinyal skala penuh yang dibagi dan juga ukuran dari langkah-langkah. Boleh juga dinyatakan dalam *bit* yang ada dalam satu *word*, ukuran LSB (angka terkecil) sebagai persen dari skala penuh atau dapat juga LSB dalam mV (untuk skala penuh yang diberikan).

- ***Accuracy* (Ketelitian)**

Adalah jumlah dari semua kesalahan, misalnya kesalahan *non linier*, skala penuh, skala *nol* dan lain-lain. Dapat juga menyatakan perbedaan antara tegangan *input analog* secara teoritis yang dibutuhkan untuk menghasilkan suatu kode *biner* tertentu terhadap tegangan *input* nyata yang menghasilkan tegangan kode *biner* tersebut.

- **Waktu Konversi**

Waktu yang dibutuhkan untuk mengkonversikan *analog* ke *digital* setiap sampel atau waktu yang diperlukan untuk menyelesaikan suatu konversi. Disini tidak akan dijelaskan keseluruhan dari jenis ADC, tetapi hanya dititik beratkan pada ADC jenis *Successive Approximation.* Karena dalam perencanaan pembuatan alat digunakan ADC jenis ini. *Successive Approximation* ADC merupakan golongan ADC *medium.* ADC tipe ini dapat dikatakan merupakan perpaduan yang baik antara kecepatan (kecepatan menegah) dan tingkat kerumitan rangkaian (menengah). Waktu konversi ADC ini selalu tetap, tidak tergantung pada besarnya sinyal *analog* (*input*), tetapnya waktu konversi ini merupakan keuntungan penggunaan ADC tipe ini.

- **ADC 0809**

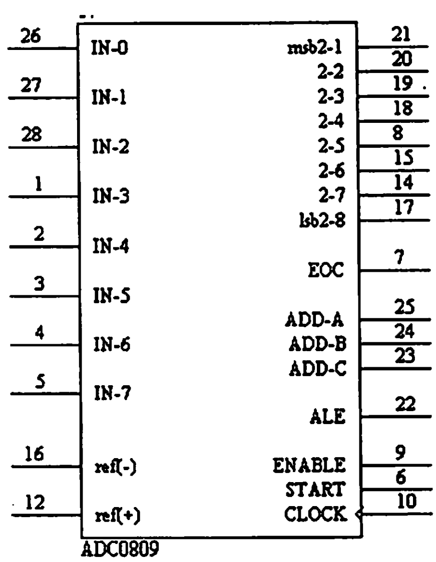
Analog To Digital Converter (ADC) 0809 dikemas dalam IC *monolitik,* ADC ini menggunakan metode pengubah berturut-turut (*Successive Approximation Register*) dengan 8 saluran *input analog* dan dilengkapi beberapa kontrol logika sesuai dengan standart mikroprosessor. Blok diagram ADC 0809 memperlihatkan bahwa ADC 0809 terdiri dari 3 (tiga) bagian utama yaitu :

- MUX *Analog* 8 Channel.
- *Analog To Digital Converter* (ADC) 8 *bit.*
- *Three-State Buffer* (Penyangga terkunci 3 kanal).

Multiplexer analog 8 *chanel* berfungsi untuk mengolah 8 *input* data *analog* secara bergantian. Untuk memilih *input* mana yang dikehendaki pada *output multiplexer* disediakan 3 *bit* kontrol pemilih saluran *input* A, B, C. *Analog To*

Digital Conventer (ADC) merupakan *Successive Approximation Register* 8 *bit* yang terdiri dari komparator, *SAR*, dan *Clok Tri-State Latch Buffer* berfungsi untuk menampung keluaran ADC 8 *bit*.

ADC ini merupakan level tegangan terbatas untuk sinyal *input*-nya yang tergantung pada *input referensi* yang digunakan. Dalam hal ini yang membatasi adalah tegangan *referensi* positif *Vref* (+) dan tegangan negatif *Vref* (-). Jika *input referensi* diberi tegangan negatif dan *input referensi* positif diberi tegangan positif sehingga tegangan *input analog* dapat berharga diantara kedua tegangan *referensi* tadi dan ini disebut *bipolar*, artinya kedua *input*-nya mempunyai polaritas positif dan negatif. Jika *input referensi* positif diberi tegangan positif dan *referensi* negatif diberi tegangan 0 volt, maka dapat disebut *unipolar* karena *analog*-nya berada diatas 0 Volt (berharga positif saja). ADC yang dipakai dalam sistem ini dirancang untuk jenis *unipolar*. Gambar struktur pin ADC 0809 dapat dilihat pada gambar dibawah ini.



Gambar 2-8. Struktur *Pin* IC ADC 0809

2.7. *Transducer*

Sistem instrumentasi elektronik terdiri dari sejumlah komponen yang secara bersama-sama digunakan untuk melakukan suatu pengukuran dan mencatat hasilnya. Sebuah sistem instrumentasi umumnya terdiri dari tiga elemen utama, yaitu : peralatan masukan, pengondisi sinyal (*signal conditioning*) atau peralatan pengolah, dan peralatan keluaran (*output*).

Besaran masukan pada kebanyakan sistem instrumentasi bukan besaran listrik. Untuk menggunakan metoda dan teknik listrik pada pengukuran, manipulasi atau pengontrolan, besaran yang bukan listrik ini dirubah menjadi suatu sinyal listrik oleh sebuah alat yang disebut dengan *tranducer*. Suatu definisi menyatakan bahwa *tranducer* adalah sebuah alat yang dapat digerakan oleh energi di dalam sebuah sistem tranmisi, menyalurkan energi dalam bentuk yang berlainan ke sistem tranmisi kedua. Transmisi energi ini dapat berupa listrik, mekanik, kimia, *optic* (radiasi) atau *termal* (panas).

Transducder dapat dikelompokkan berdasarkan pemakaianya. Metode pengubahan energi, sifat dasar dari sinyal keluaran, dan lain-lain. Semua pengelompokan ini biasanya memperlihatkan daerah yang saling melengkapi sedangkan pengelompokan *transducer* berdasarkan prinsip listrik adalah sebagai berikut :

a. *Transducer Pasif.*

Merupakan *transducer* yang memerlukan daya luar pada saat menghasilkan perubahan dalam sebuah parameter listrik seperti halnya tahanan, kapasitansi, dan sebagainya yang dapat diukur sebagai suatu perubahan tegangan atau arus.

b. Transducer Aktif.

Merupakan jenis *transducer* yang memiliki jenis pembangkit sendiri (*self generation type*), yang dapat menghasilkan suatu tegangan atau arus *analog* bila dirangsang dengan suatu bentuk *fisis* energi. *Transducer* ini tidak memerlukan daya luar pada saat berkerja.

Dengan demikian pemilihan *transducer* yang sesuai merupakan langkah pertama dan mungkin yang paling penting untuk memperoleh hasil-hasil yang teliti. Persyaratan ketelitian bagi sistem keseluruhan menentukan derajat terhadap masing-masing faktor yang terkontribusi terhadap ketelitian harus diperhitungkan. Sebagian faktor-faktor tersebut adalah :

- Parameter dasar *transducer*

  Merupakan jenis dan rangkuman pengukuran, sensitivitas, dan *eksitasi*

- Kondisi fisik

  Memperlihatkan sambungan-sambungan mekanis dan elektrik, perlengkapan-perlengkapan pemasaran, tahan korusi.

- Kondisi sekeliling

  Memperhatikaan efek ketidak *linier*-an, efek linieritas, respon frekuensi, resolusi.

- Kondisi lingkungan

  Merupakan pengaruh atau efek *temperature*, percepatan, guncangan, dan getaran.

- Kesesuaian peralatan yang disertakan.

Merupakan perlengkapan kesetimbangan nol, toleransi sensitivitas, penyesuaian impedansi.

2.7.1. *Transducer* Temperatur

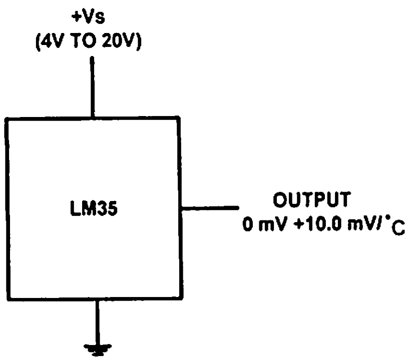
Pada Skripsi ini *transducer* yang digunakan untuk mendeteksi suhu adalah LM 35. LM 35 menghasilkan tegangan keluaran yang proposional *linier* dengan suhu yang dinyatakan dengan satuan derajat *celcius* (°C), selain itu LM 35 juga mempunyai keungulan dibandingkan dengan *sensor temperature* yang berkalibrasi dalam °K, sehingga di dalam penggunaannya tidak diperlukan pengurangan tegangan konstan yang besar dari *output*-nya untuk menghasilkan pengukuran *centigrade*. LM 35 tidak memerlukan kalibrasi ekternal atau *trimming* untuk menghasilkan tegangan.

LM 35 mempunyai impedansi keluaran yang rendah dan *output linier* yang dapat digunakan dalam *interfacing* dengan tampilan atau rangkaian pengontrol. *Sensor* ini dapat digunakan secara *single power supply* maupun *plus* dan *minus supply*.

Spesifikasi dari LM 35 adalah sebagai berikut :

- Kalibrasi secara langsung pada derajat *Celcius* (°C).
- Faktor skala *linier* sebesar 10mV / °C.
- Jaminan keakurasian sebesar 0,5 °C (pada suhu 25 °C).
- *Range temperature* -55 °C sampai +150 °C.
- Sesuai jika digunakan pada aplikasi pengontrolan.
- Beroperasi dari 4 Volt hingga 30 Volt.

- Arus drain kurang dari 60 μA.
- *Low self heating*, yaitu sebesar 0,08 °C pada hampa udara.
- Non linieritas tipikal sebesar $\frac{1}{4}$ °C
- Impedansi keluaran yang rendah, yaitu 0,1 Ω untuk muatan 1 mA.



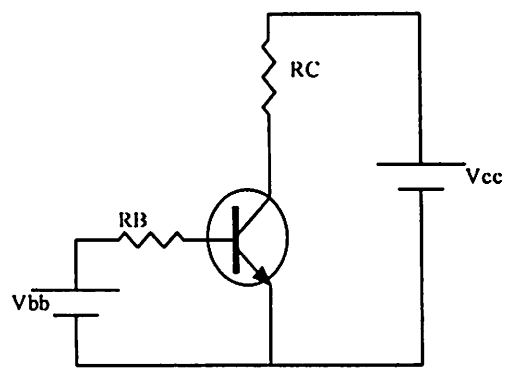
Gambar 2-9. *Sensor* Suhu LM 35

2.7.2. Sensor *Level*

Sensor *level* yang di gunakan dalam skripsi ini adalah *elektrode. Elektrode* di gunakan untuk menentukan *level* atau ketinggian air di dalam *radiator. Electrode* berupa dua jalur pada *PCB* yang sejajar dan berdekatan. Cara kerja *electrode* ini adalah pada saat kedua jalur ini tidak terkena air maka tidak akan ada arus yang mengalir. Tetapi saat kedua jalur ini terkena air maka ada arus yang mengalir dikarenakan sifat air sebagai *conductor* yang baik.

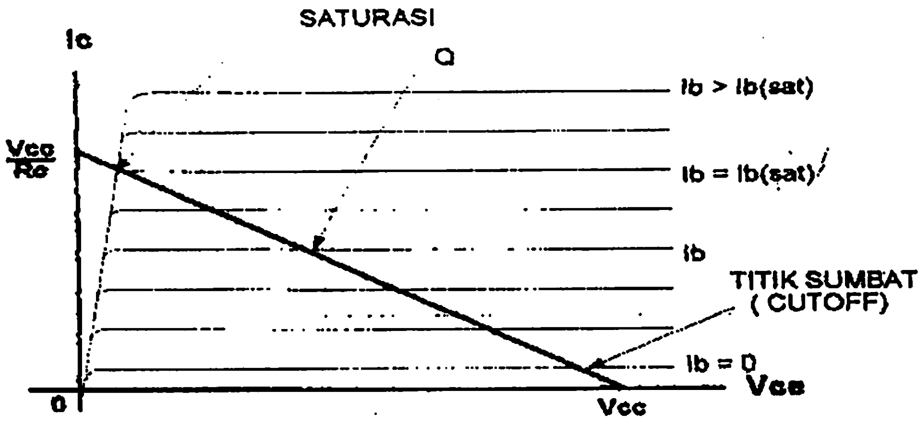
2.8. *Transistor*

Transistor merupakan salah satu dari komponen aktif yang banyak sekali digunakan. Beberapa fungsi dari *transistor* yaitu dapat digunakan sebagai rangkaian *driver* ataupun sebagai saklar. Rangkaian *driver* merupakan suatu rangkaian yang digunakan untuk mengerakan peralatan lain yang membutuhkan arus atau tegangan yang lebih besar. Asas kerja dari *transistor* adalah akan ada arus yang mengalir diantara terminal kolektor – emitor (Ic) hanya apabila ada arus yang mengalir diantara terminal *basis emitor* (I_B). Jadi *transistor* harus dioperasikan pada daerah *linier* agar diperoleh sinyal keluaran yang tidak cacat (*distorsi*). Untuk dapat mengoperasikan secara tepat maka pengertian tentang titik kerja transistor amatlah penting dan harus dipahami dan dimengerti dengan benar.



Gambar 2-10. Rangkaian *Switching* Transistor

Garis beban akan memotong sekelompok kurva arus *basis* konstan I_B tertentu (yang diatur rangkaian *bias*), garis beban akan memotong kurva I_B tersebut dititik Q yang disebut titik kerja *transistor*. Titik kerja ini menjadi kondisi awal dari pengoperasian *transistor* kelak dimana transistor tersebut mempunyai tiga daerah kerja yaitu aktif (*active*), jenuh (*saturasi*), dan tersumbat (cut-*off*)



Gambar 2-11. Karakteristik Ic – Vcc sebuah transistor *Bipolar*

Pada gambar 2-11 dapat dilihat, titik dimana garis beban memotong kurva $I_B = 0$ disebut sebagai titik sumbat (*cut-off*). Pada titik ini arus kolektor (Ic) sangat kecil (hanya arus bocor) sehingga dapat diabaikan, disini *transistor* kehilangan kerja normalnya. Disini dapat dikatakan bahwa tegangan kolektor *emitor* sama dengan ujung dari garis beban tersebut.

$$V_{CE(cut-off)} \cong Vcc$$

Perpotongan garis beban dengan kurva $I_B = I_{B\,(sat)}$ disebut titik jenuh (*saturasi*). Pada titik ini arus kolektor maksimum atau dapat dikatakan bahwa arus kolektor sama dengan ujung dari garis beban.

$$I_{C(sat)} \cong \frac{Vcc}{Rc}$$

Jika arus *basis* I_B lebih kecil dari $I_{B\,(sat)}$ maka *transistor* akan beroperasi pada daerah aktif, yaitu titik kerjanya terletak sepanjang garis beban.

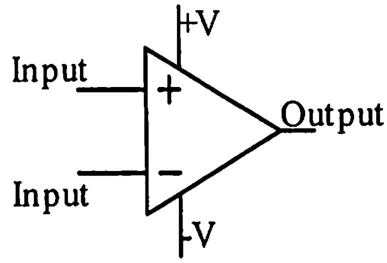
Jadi dapat disimpulkan bahwa *transistor bipolar* berkerja sebagai suatu sumber arus (penguat) dimana saja sepanjang garis beban, kecuali titik jenuh (*saturasi*) atau titik sumbat (*cut-off*) dimana *transistor* tidak lagi berkerja sebagai sumber arus (penguat) melainkan sebagai saklar (*swiching*).

2.9. Penguat Operasional (*Op – Amp*)

Amplifier atau lazimnya disebut penguat, dalam suatu rangkaian dapat difungsikan sebagai rangkaian penguat sinyal *input*, rangkaian penjumlahan tegangan *input*, rangkaian pembanding antara dua sinyal *input*, rangkaian *filter* dan sebagainya.

Rangkaian penguat ini sangat sederhana dalam pemakaian baik cara merangkainya maupun dalam penggunaannya. Rangkaian ini terdiri dari kombinasi antara Penguat Operasional (*Operasional amplifier Op-amp*) yang dirangkai bersama komponen *pasif* tahanan maupun kapasitor. Dengan kombinasi tersebut maka *Op-amp* dapat dikembangkan lagi menjadi rangkaian yang mempunyai spesifikasi khusus seperti rangkaian instrumentasi, rangkaian osilator dan lainnya.

Gambar 2-12 menujukkan simbol dari *op-amp* dengan lima terminal dasar yang terdiri dari 2 terminal catu daya, 2 terminal *input* atau masukan yaitu (+) dan (-) dan satu buah terminal *output* atau keluaran dari *Op-amp*.

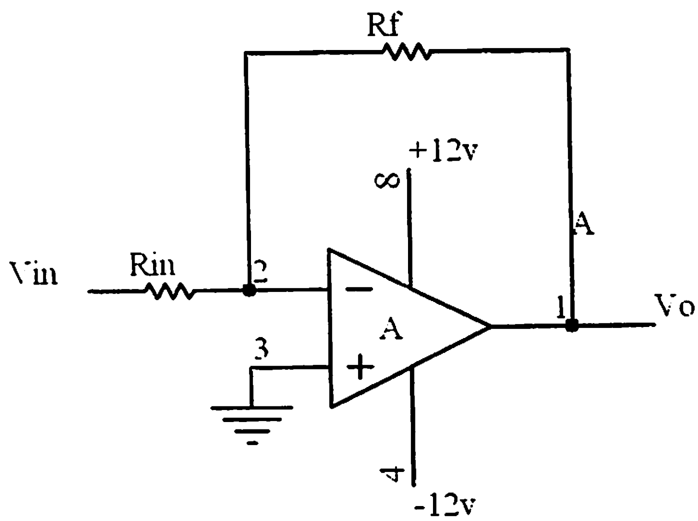


Gambar 2-12. Simbol *Op-Amp*

- ***Inverting Amplifier***

Inverting Amplifier merupakan penguat pembalik dimana polaritas input dibalik sehingga menghasilkan output dengan polaritas berbeda dari input. Besarnya nilai output tergantung dari penguatan yang direncanakan. Rumus untuk penguatan dari *Inverting Amplifier* adalah sebagai berikut :

$$Av = -\frac{Rf}{Rin}$$



Gambar 2-13. Simbol *Inverting Op-Amp*

2.10. IC *Information Storage Device* 2560

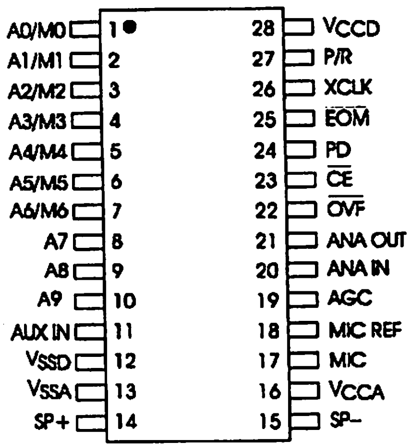
IC ISD (*Information Storage Device*) 2560 merupakan salah satu seri dari IC ISD 2500. IC penyimpan informasi ISD 2500 *chip corder series* memberikan kualitas yang tinggi sebagai *single chip record / playback* dengan jangka waktu durasi 60 – 120 detik penggunaan. Dan di dalamnya telah dilengkapi dengan *on chip oscilator, microphone preamplifier, automatic gain control, antiliasing filter,* *smoothing filter, speaker amplifier* dan penyimpanan dengan kepadatan tinggi. Selain itu ISD 2500 ini didesain sangat cocok atau sesuai dengan penggunaan *microcontroller*.

Perekam suara di simpan di dalam sel memori yang tidak mudah hilang. Di dalam proses perekaman menggunakan aktif *low* pada pin *rec.* pembuatan *Information Storage Device* ini di patenan secara langsung oleh *Direct Analogue Storage Technology* (DAST TM), yang mana sinyal suara dan audio dapat disimpan dalam bentuk aslinya secara analog, ke dalam *memory.* Penyimpanan ini adalah dalam bentuk natural atau alami sehingga akan memberikan kualitas yang tinggi dan kemampuan suara yang baik.

Tabel 2-3. Seri ISD 2500

Tipe	Waktu (detik)	*Sample rate* (kHz)	*Filter Pass Band* (Hz)
2560	60	8.0	3400
2575	75	6.4	2700
2590	90	5.3	2300
25120	120	4.0	1700

Dengan melihat pada tabel 2-3 (Seri ISD 2500) diatas, maka dapat diketahui bahwa IC penyimpanan suara ISD seri 2560 ini adalah merupakan jenis EEPROM (*Electrically Erasable Programable* ROM). EEPROM adalah jenis ROM yang dapat diprogram, dihapus dan diprogram ulang secara elektrik dan tidak menggunakan sinar ultraviolet. IC ISD 2560 ini dapat melakukan perekaman suara atau pesan dengan jangka waktu durasi maksimum selama 60 detik dengan *sample rate* 8.0 kHz. Dimana untuk *cell* penyimpanan ini terbagi dalam alamat yaitu dari 00H – 275H. pada saat *standby* arus yang diserap sekitar 1µA. Di dalam ISD 2560 ini dilengkapi dengan *preamplifier, internal Automatic Gain Control, filter antialising*. Susunan pin dari ISD 2560 ditunjukkan gambar 2-14.



Gambar 2-14. Pin ISD 2560

Keutamaan dari ISD 2560 ini adalah :

- Mudah dalam penggunaannya sebagai *single chip voice record / playback.*
- Mempunyai kualitas yang tinggi, menghasilkan kembali suara atau audio aslinya.
- Kompatible dengan penggunaan *microcontroller.*
- *Single chip* dengan lama penyimpanan 60 detik.
- *Power supply* +5V *single.*
- Dapat menyimpan pesan selama 100 tahun.

Selanjutnya untuk mengetahui dan untuk melakukan pengontrolan atau langkah – langkah cara penggunaan dari ISD 2560 ini maka dapat dilihat sesuai pada tabel 2-4 (Sinyal *control* ISD) yang mana pada tabel tersebut berisi langkah – langkah pemberian sinyal kontrol pada ISD 2560 yang dikondisikan dalam keadaan *record* maupun *playback* serta memulai atau mengakhiri suatu *record* atau *playback*. Untuk lebih jelasnya marilah kita perhatikan tabel berikut.

Tabel 2-4. Sinyal *control* ISD

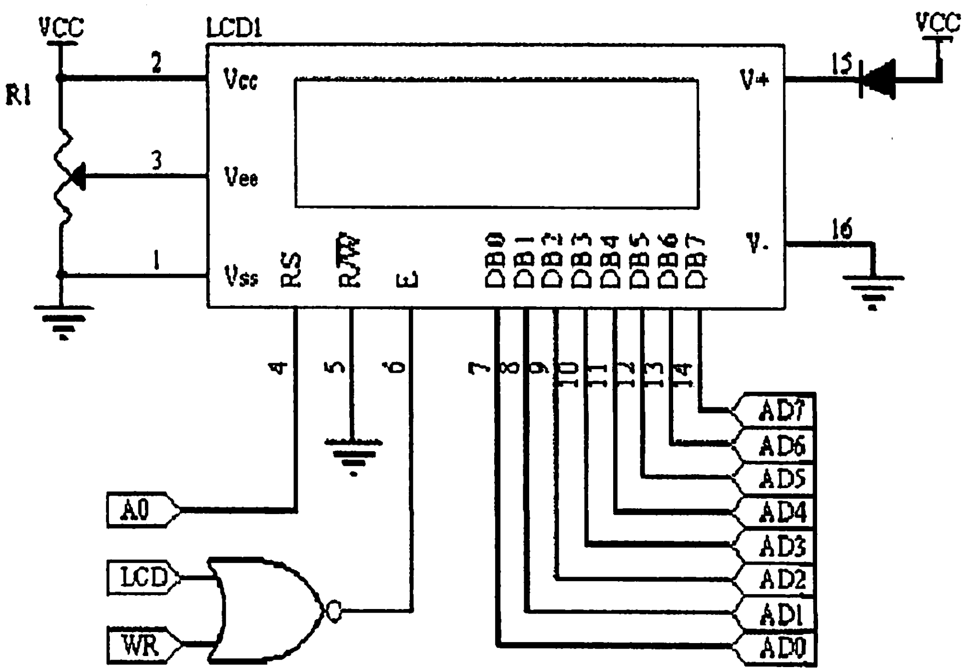
Langkah *control*	*Function*	*Action*
1	Pemilihan *rec/playback mode*	[1] /PD = *low* [2] P/R= *as desired*
2	*Set address* memulai *rec/playback*	Pemilihan alamat A0 – A9
3A	Mulai *playback*	P/R= *high*, $\overline{CE}$= *low*
3B	Mulai *record*	P/R = *low*, $\overline{CE}$= *low*
4A	Mengakhiri *playback*	Otomatis
4B	Mengakhiri *record*	PD atau $\overline{CE}$= *high*

2.11. LCD (*Liquid Crystal Display*)

Untuk menampilkan data yang telah diproses oleh mikrokontroler, maka dibutuhkan suatu perangkat yang dapat digunakan sebagai alat penampil data, sehingga pengguna dapat mengerti data-data hasil olahan dari mikrokontroler.

Suatu perangkat penampil siap pakai dan banyak dipakai adalah LCD *dot matrik* berukuran 2 x 16 *digit*.

Tampilan LCD sesuai dengan instruksi melalui *software* dan dengan mengontrol pada pin E, R/W dan RS yang dihubungkan dengan sistem mikrokontroler.



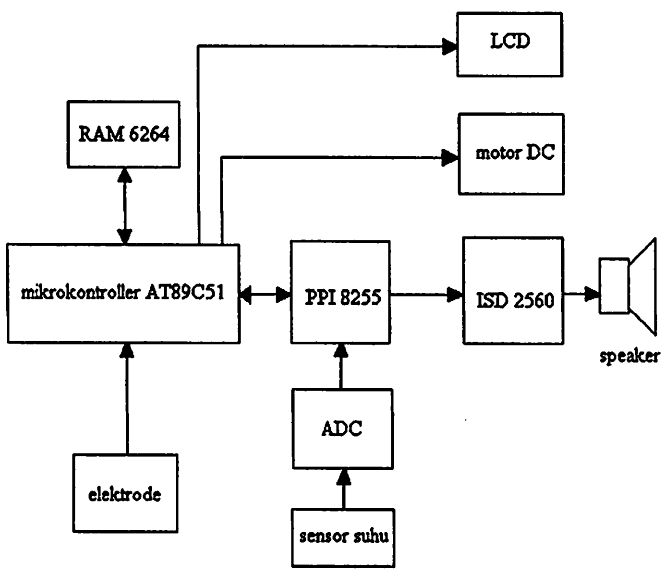
Gambar 2-15. Rangkaian LCD

BAB III

PERANCANGAN DAN PEMBUATAN ALAT

Alat yang direncanakan ini berfungsi untuk mendeteksi level air dan suhu dengan bantuan mikrokontroler Atmel dan antarmuka yang sengaja dirancang untuk keperluan tersebut.

Bab ini membahas tentang perencanaan dan realisasi perangkat keras dan perangkat lunak yang digunakan dalam sistem ini. Diagram skematiknya ditunjukkkan dalam Gambar 3-1.



Gambar 3-1. Blok Diagram Sistem

3.1. Perancangan Perangkat Keras

Perangkat keras sistem ini terdiri beberapa bagian , yaitu :

1. Sistem mikrokontroler 89C51, RAM 6264 dan PPI 8255.

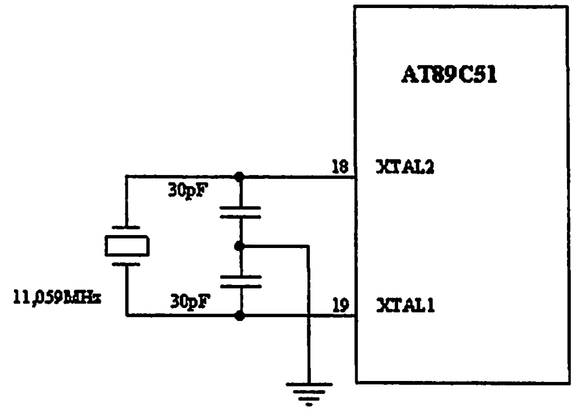
2. Sensor
3. Rangkaian penguat tegangan, rangkaian yang menguatkan tegangan dari sensor menjadi tegangan 0V sampai 5V agar dapat dibaca oleh ADC.
4. Rangkaian pengubah data analog ke data digital dengan ADC 0809.
5. *Liquid Crystal Display.*
6. ISD 2560.

3.1.1. Mikrokontroler 89C51

Mikrokontroler 89C51 harus didukung oleh beberapa rangkaian lain agar dapat melakukan prosesnya, yaitu berupa rangkaian clock dan reset. Selain itu juga harus ditentukan penggunaan port-portnya dan sinyal sinyal yang digunakan untuk mendukung proses yang akan dilakukan.

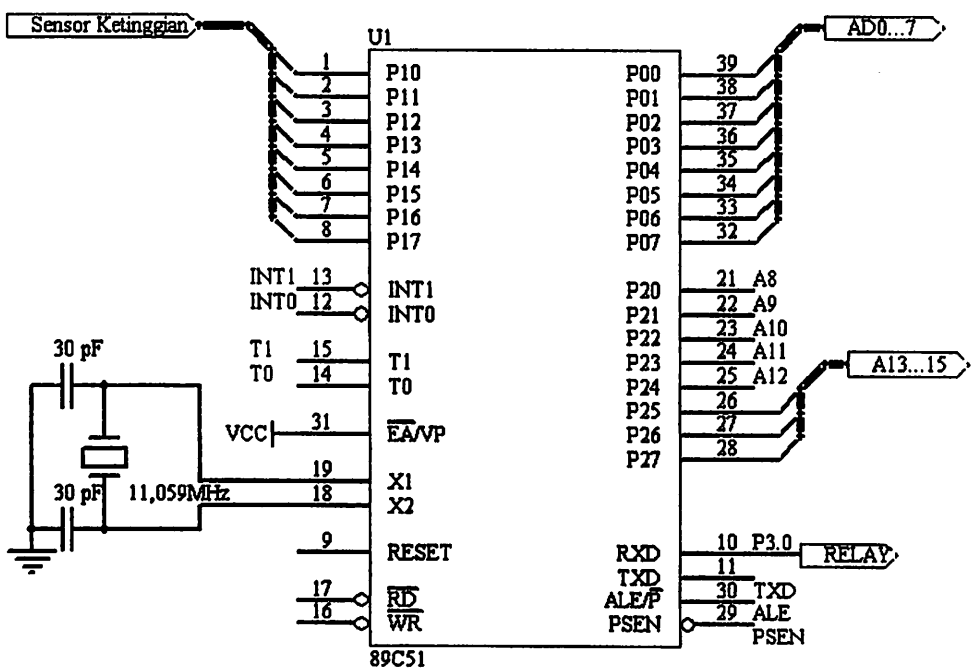
- *Clock*

Kecepatan proses yang dilakukan oleh mikrokontroler ditentukan oleh sumber *clock* (pewaktuan) yang mengendalikan mikrokontroler tersebut. Sistem yang dirancang ini akan menggunakan osilator internal yang sudah tersedia di dalam chip 89C51. Untuk menentukan frekuensi osilatornya cukup dengan cara menghubungkan kristal pada pin XTAL1 dan XTAL2 serta dua buah kapasitor ke ground. Besar kapasitansinya disesuaikan dengan spesifikasi pada lembar data 89C51 yaitu 30 pF. Pemilihan besar frekuensi kristal disesuaikan dengan pemilihan kecepatan yang diharapkan untuk transfer data melalui pin *serial interface* 89C51 tersebut. Sistem ini dirancang untuk memiliki kemampuan *baud rate* sebesar 9600 bps, sehingga dipilih kristal dengan nilai 11,059 MHz sesuai dengan spesifikasi pada lembar data 89C51. Gambar 3-2 memperlihatkan rangkaian pewaktu yang digunakan.



Gambar 3-2. Rangkaian Pewaktuan

- **Mikrokontroler AT89C51**



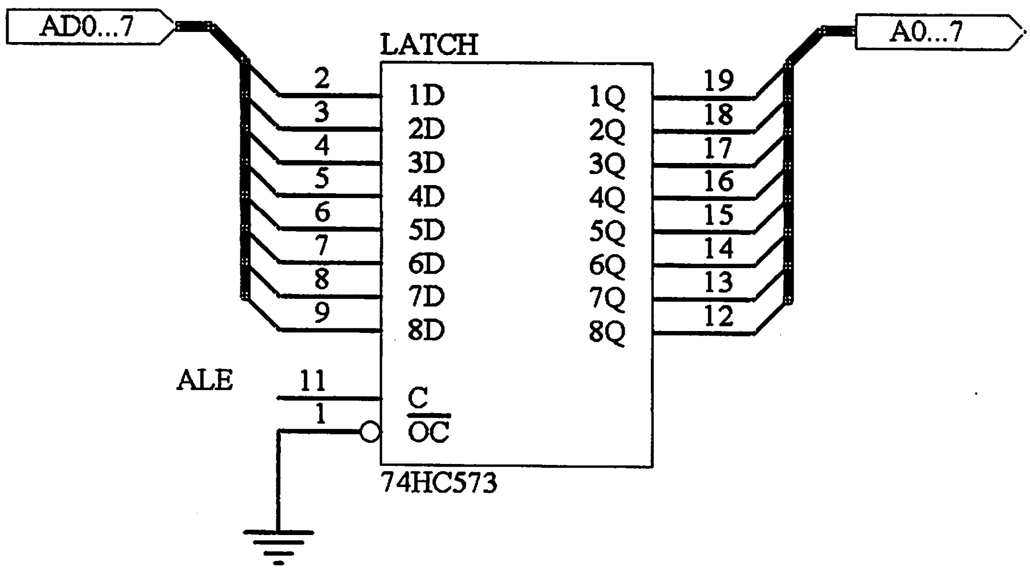
Gambar 3-3. Rangkaian Mikrokontroler AT89C51

Pada gambar 3-3 terlihat bahwa AT89C51 menggunakan *clok internal* dengan memasang sebuah *XTAL* yang mempunyai frekuensi 11.059 MHz dan dua buah kapasitor 30 pF sebagai stabilisator. *Port* 0 dari AT89C51 dihubungkan pada *Latch* 74HCT573 untuk memisahkan antara jalur data (*Data Bus*) dengan jalur alamat (*Address Bus*). *Port* 1 AT89C51 digunakan untuk sensor *level electrode*.. *Port* 2 AT89C51 A13,A14 dan A15) akan dihubungkan dengan IC dekoder 74LS138 yang digunakan sebagai pemetaan alamat untuk memilih komponen mana yang akan diakses.

3.1.2. Latch

Latch digunakan untuk memisahkan antara bit-bit data dengan bit-bit alamat rendah yang dikeluarkan pada port 0 oleh mikrokontroler 89C51. Tipe yang akan dipakai adalah tipe 74LS573. Pin enable C pada latch ini dihubungkan dengan sinyal ALE yang dikeluarkan oleh mikrokontroler. Sedangkan saluran masukan latch dihubungkan dengan port 0 yang mengeluarkan bit-bit data dan alamat rendah.

Sinyal ALE berlogika tinggi maka bit-bit yang dikeluarkan melalui port 0 adalah bit-bit alamat, dan 74LS573 akan meneruskan bit-bit ini ke keluarannya yang terhubung dengan saluran alamat komponen yang dituju. Apabila sinyal ALE dalam keadaan logika rendah maka 74LS573 menahan bit-bit tersebut sehingga bit-bit ini akan dibaca sebagai data oleh komponen yang terhubung. Address latch ditunjukkan pada gambar 3-4.



Gambar 3-4. *Address Latch*

3.1.3. Dekoder

Proses aliran data yang diperlukan oleh mikrokontroler tergantung dari pengalamatan yang dipilih mikrokontroler tersebut. Untuk memilih komponen mana yang diakses maka diperlukan suatu rangkaian dekoder. Dekoder ini akan dihubungkan dengan alamat tinggi yang dikeluarkan mikrokontroler. Sistem ini mempergunakan pengalamatan 16 bit untuk mengalamati LCD dan PPI.

Peta alamat pada sistem ini direncanakan dibagi per-delapan kilo byte, yang berarti bahwa alamat mikrokontroler yang tersedia sebesar 64 kilo byte dibagi menjadi 8 blok. Masing-masing blok dipilih dengan menggunakan 3 bit alamat tinggi yang dikeluarkan melalui port 2. Tabel 3.1. memperlihatkan pemetaan alamat pada sistem ini.

Tabel 3-1. Pemetaan Alamat

Chip Select	Alamat	Fungsi
CS0	0000-1FFF	
CS1	2000-3FFF	
CS2	4000-5FFF	
CS3	6000-7FFF	
CS4	8000-9FFF	
CS5	A000-BFFF	LCD
CS6	C000-DFFF	RAM
CS7	E000-FFFF	PPI 8255

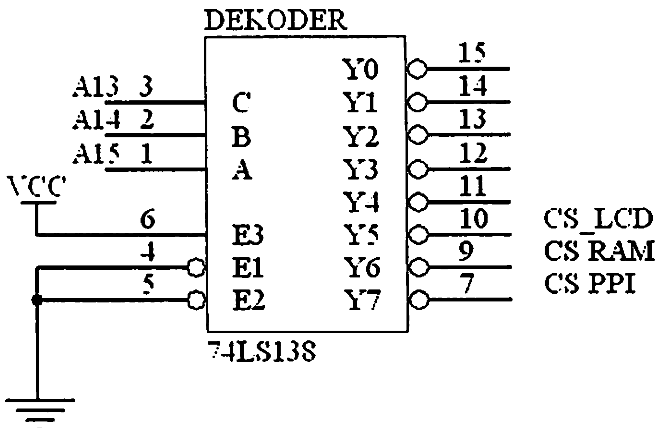
LCD diletakkan pada alamat A000H-BFFFH. RAM diletakkan pada alamat C000H-DFFFH. Sedangkan PPI 8255 diletakkan pada alamat E000-FFFF. Blok-blok yang masih kosong dapat dimanfaatkan untuk penambahan memori atau untuk keperluan lainnya. Pemilihan alamat-alamat ini disesuaikan dengan keperluan dan perencanaan yang dapat dilakukan untuk pengembangan berikutnya.

Dekoder yang dipergunakan adalah dekoder 74LS138, suatu dekoder 3 ke 8. Tabel fungsinya seperti terlihat dalam Tabel 3-2.

Tabel 3-2. Tabel dekoder 74LS138

INPUT					OUTPUT							
ENABLE		SELECT										
G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	H	H	H	H	H	L	H	H	H	H	H
H	L	H	H	H	H	H	H	L	H	H	H	H
H	L	H	H	H	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

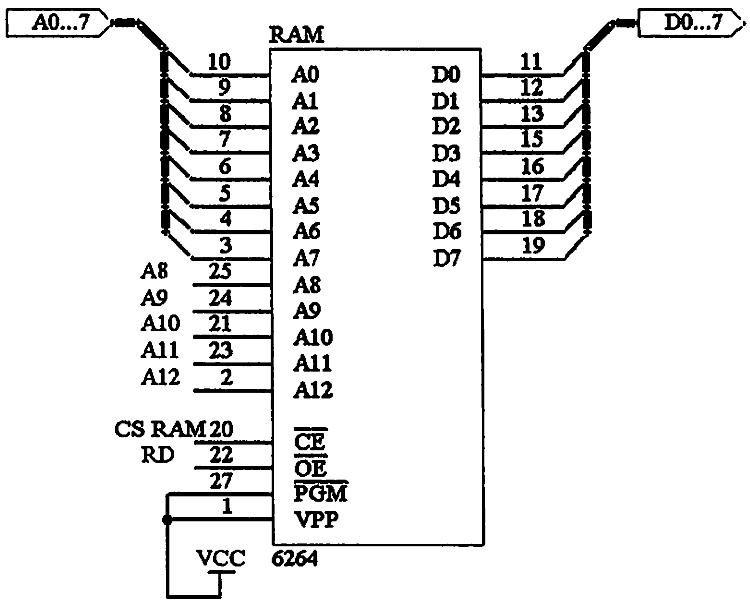
Dekoder ini dikondisikan selalu membaca data masukannya setiap saat, sehingga pin G1 diberi logika tinggi dan pin G2A, G2B dihubungkan dengan pentanahan. Saluran alamat yang digunakan untuk memilih alamat diambil dari mikrokontroler pada bit A13, A14 dan A15, dihubungkan dengan pin A, B dan C pada dekoder. Rangkaian dekoder ditunjukkan dalam Gambar 3-5.



Gambar 3-5. Rangkaian Dekoder Alamat

3.1.4. RAM

RAM yang digunakan untuk menyimpan data adalah jenis 6264 yang berkapasitas 8 kilobyte. Komponen ini tersusun atas 13 jalur alamt A0-A12, 8 jalur data D0-D7, dua saluran seleksi CS1 dan CS2 serta sinyal kontrol pembacaan dan penulisan OE dan WE. Rangkaian RAM pada rangkaian ini ditunjukkan dalam Gambar 3-6.

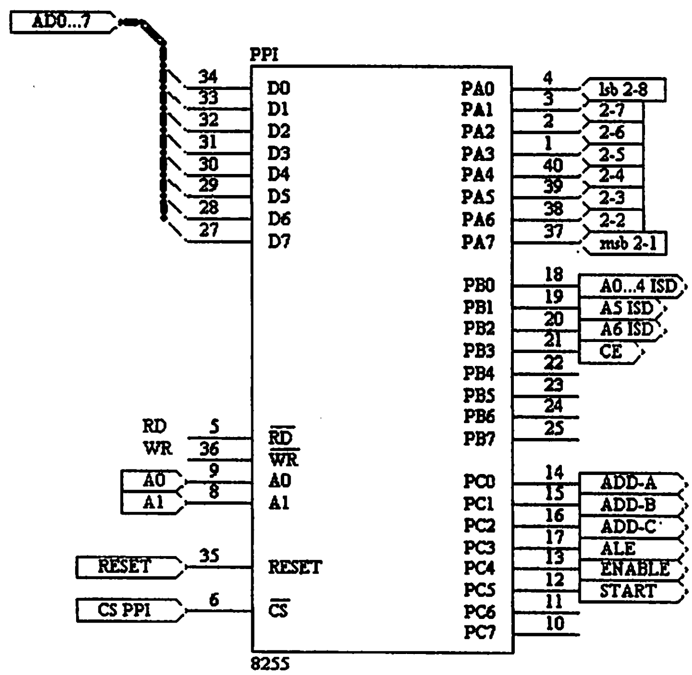


Gambar 3-6 Rangkaian RAM 6264

3.1.5. PPI 8255

Mikrokontroler 89C51 memiliki 4 buah port, yaitu port 0, port 1, port 2 dan port 3. Tetapi karena tidak mempunyai EPROM internal, maka untuk mengakses EPROM eksternal, port 0 dan port 2 difungsikan menjadi bus alamat dan bus data. Sementara itu beberapa bit dari port 3 juga memiliki fungsi lain yaitu sinyal RD, WR, TxD, RxD, INT0, INT1, T0 dan T1. Jadi port bebas yang tersisa adalah port 1. Untuk menambah jumlah port digunakanlah PPI 8255.

Dalam perencanaan, PPI 8255 ditempatkan pada alamat E000H-E003H. Pin A0 dan A1 PPI yang dipergunakan untuk memilih register yang diakses dihubungkan ke A0 dan A1 sistem mikrokontroler. Sementara pin CS IC 8255 dihubungkan ke CS7 (keluaran dari *address decoder* 74LS138). Rangkaian PPI 8255 seperti terlihat dalam Gambar 3-7.



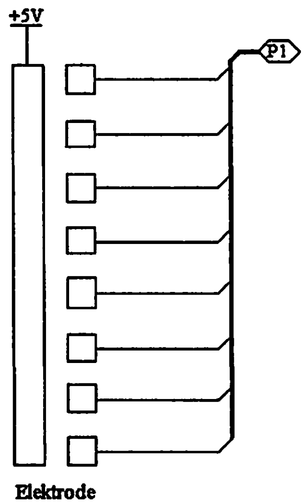
Gambar 3-7. Rangkaian PPI 8255

3.1.6 Sensor

3.1.6.1. Sensor level

Sensor *level* yang di gunakan dalam skripsi ini adalah *elektrode. Elektrode* di gunakan untuk menentukan *level* atau ketinggian air di dalam *radiator. Electrode* berupa dua jalur pada *PCB* yang sejajar dan berdekatan. Cara kerja *electrode* ini adalah pada saat kedua jalur ini tidak terkena air maka tidak akan ada arus yang mengalir. Tetapi saat kedua jalur ini terkena air maka ada arus yang mengalir dikarenakan sifat air sebagai *conductor* yang baik.

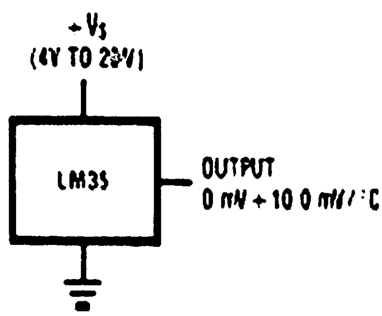
Disini sensor disupply dengan tengangan (Vs) 5V. Jadi jika sensor tidak terkena air maka output dari sensor yang masuk ke P1 mikrokontroler adalah sebesar 0V (dibaca sebagai data rendah). Dan saat sensor terkena air maka output dari sensor yang masuk ke P1 mikrokontroler adalah sebesar (Vs) sensor yaitu 5V (dibaca sebagai data tinggi).



Gambar 3-8. Sensor level air (*electrode*)

3.1.6.2. Sensor suhu

Pada perancangan dan pembuatan alat, *sensor* suhu yang digunakan adalah LM 35. *Sensor* ini memiliki *output* yang linier yaitu menghasilkan kenaikan tegangan *output* sebesar 10 mV untuk setiap kenaikan 1° C sehingga memudahkan dalam pengolahan datanya. *Output* dari LM 35 ini adalah *linier*, ini dibuktikan dengan semakin naiknya suhu maka semakin besar pula tegangan yang dihasilkan.



Gambar 3-9. Sensor Suhu LM35

Untuk menghitung tegangan *output* dari *sensor* ini pada saat membaca *temperature* adalah :

V_{out} = (Suhu) x 10mV/°C

Dimana :

- V_{out} : Tegangan *output* dari *sensor* LM 35 (volt)
- Temp : Besar suhu yang dibaca (°C)

Disini *sensor* disuplay dengan tegangan (Vs) 5 Volt DC.

3.1.7. Rangkaian Penguat Sinyal

Spesifikasi keluaran sensor yang diinginkan untuk diumpankan ke ADC 0809 dapat mengukur temperatur dari 0°C sampai 100°C. Dengan jangkauan temperatur tersebut maka sensor akan mengeluarkan tegangan dari 0 V sampai 1000mV (dianggap bahwa karakter sensor mengikuti spesifikasi sebagaimana yang dijelaskan dalam data sheet).

Keluaran sensor suhu tersebut perlu dikuatkan agar didapatkan ketelitian data yang lebih baik jika dimasukkan ke ADC. Penguatan diambil 5 kali oleh penguat LM 741. Penguat pertama berfungsi untuk menguatkan tegangan masukan dan penguat kedua berfungsi untuk membalik polaritas tegangan hasil penguatan penguat pertama. Untuk mencari nilai R2 dan R3 dapat dicari berdasarkan rumus:

Vout = - Av x Vin

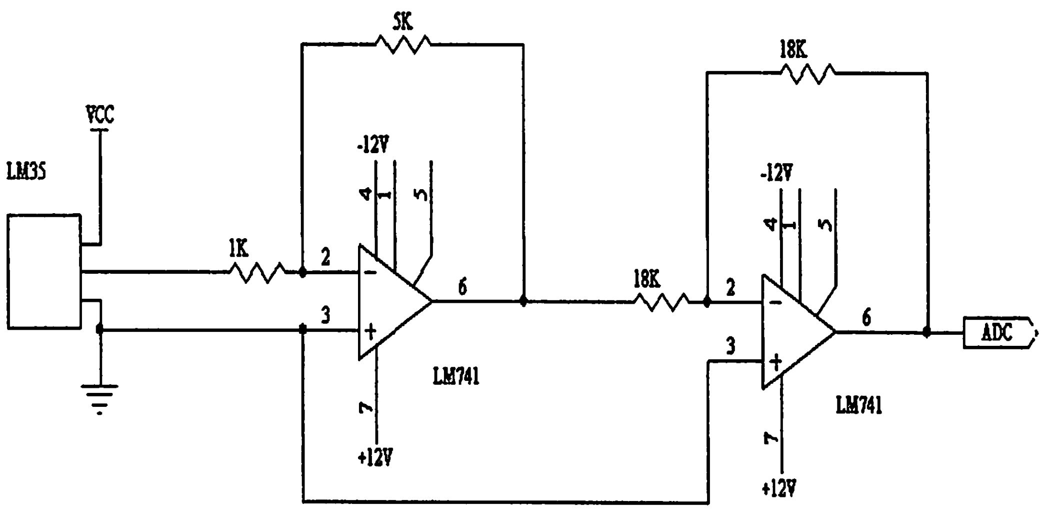
Av = R3/R2

5 = R3/R2

Bila ditentukan R3 = 5 KΩ, maka R2 = 1KΩ.

Karena penguatan kedua 1 kali (berfungsi sebagai pembalik polaritas tegangan saja) maka nilai Rf = Rin. Bila ditentukan Rf = 18kΩ maka Rin = 18kΩ.

Gambar rangkaian penguat dapat dilihat dalam Gambar 3-10.



Gambar 3-10. Penguat Tegangan

3.1.8. Rangkaian Pengubah Data Analog ke Digital (ADC)

Data suhu yang diperoleh dari sensor adalah berupa besaran tegangan analog, maka data suhu tersebut harus diubah ke bentuk data digital 8 bit agar dapat dibaca oleh mikrokontroler. Untuk itu digunakan konverter analog ke digital (ADC). *Type* yang dipakai dalam perancangan ini adalah *type* ADC 0809 yang merupakan ADC dengan 8 masukan analog yang dimultipleks menjadi data digital 8 bit.

Dikarenakan tegangan yang terukur cukup kecil maka tingkat resolusi dari ADC 0809 diharapkan cukup kecil, sehingga digunakan V_{ref} = 5 volt, dengan tingkat resolusi ADC 0809 adalah :

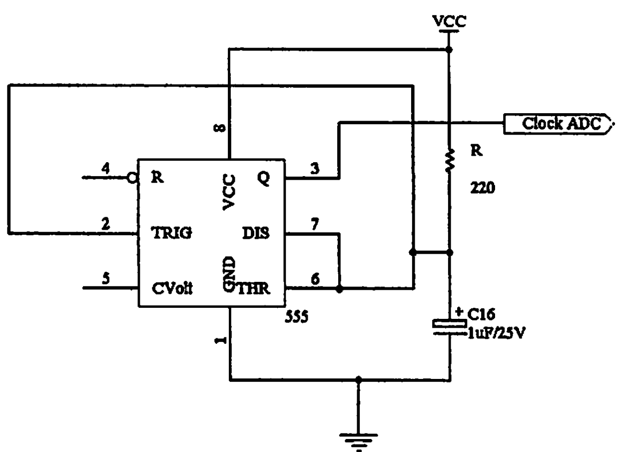
Resolusi = $V_{referensi} / (2^8 - 1)$

Resolusi = $5/(2^8 - 1)$

= 0,0196 V

Jadi besarnya resolusi adalah sebesar 0,0196 V ≈ 0,02 V

Untuk membuat ADC 0809 dapat bekerja, maka diperlukan sebuah clock. Pada data book yang ada, tertulis bahwa frekwensi clock pada umumnya adalah 640kHz. Pada perancangan ini digunakan IC timer 555. Rangkaian pembentuk pulsa dapat dilihat dalam Gambar 3-11.



Gambar 3-11. Pembangkit Clock

Frekuensi yang dihasilkan oleh rangkaian ini adalah sebesar :

F = 1 / t

T = 1,1RC

Dengan menentukan C yaitu sebesar 1μF dan frekwensi ditentukan sebesar 4kHz maka harga R sebesar :

$F = 1/(1,1 \times R \times 10^{-6})$

$4.10^3 = 1 / (1,1.10^{-6}.R)$

$R = 10^3 / 4,4$

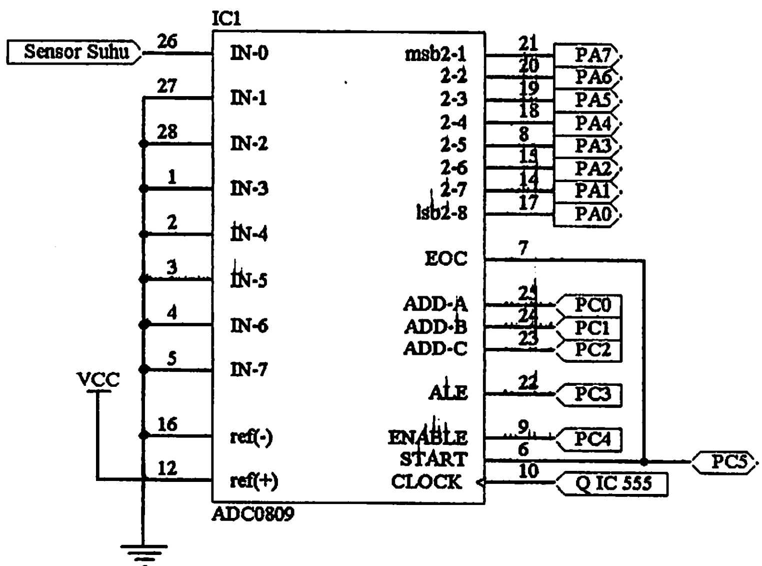
$R = 227,27\ \Omega$

$R = 220\ \Omega$

Frekwensi yang ditentukan kecil karena ADC mengatur suhu yang perubahan outputnya memerlukan waktu yang lama sehingga dibutuhkan pembacaan pengkonversian suhu lama pula untuk mendapatkan hasil pengkonversian yang sesuai.

Saluran keluaran data digital ADC 0809 dihubungkan pada *port* A PPI 8255, sedangkan alamat di ADC 0809 yang berfungsi untuk menyeleksi data masukan ADC.

Realisasi dari rangkaian ADC tersebut terlihat dalam Gambar 3-12.



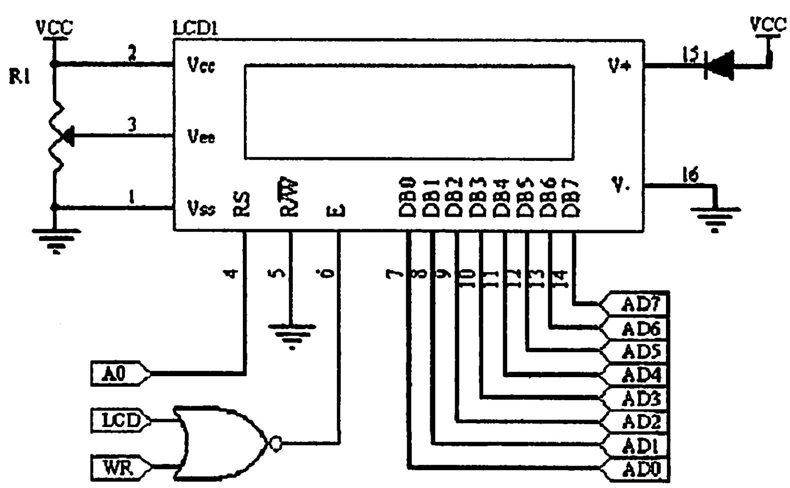
Gambar 3-12. Rangkaian ADC 0809

3.1.9. LCD

Pada sistem yang direncanakan akan digunakan LCD (Liquid Crystal Display) sebagai tampilan. LCD yang digunakan adalah jenis TM162ABC yang merupakan LCD dua baris dengan tiap barisnya terdiri dari 16 karakter.

LCD ini membutuhkan 3 sinyal kontrol, R/W (*read/write*) untuk menentukan apakah data akan dibaca atau ditulis, E (*Enable*) yang merupakan sinyal untuk meng-enable-kan dan RS (*Register Select*) untuk memilih register yang diakses. LCD TM162ABC memiliki 2 register yaitu register data dan register instruksi.

Dalam sistem ini, LCD menempati ruang alamat A000H-A001H. Pin R/W dihubungkan ke *ground* atau selalu berlogika 0 karena dalam perancangan LCD ini hanya selalu dalam operasi tulis dan pin RS dihubungkan ke pin A0 sistem mikrokontroler. Pengaktifan LCD ini selanjutnya tergantung pada pin E. Dimana pin E ini tergantung dari CS5 dari addres dekoder dan perintah write mikrokontroler. Rangkaian LCD seperti terlihat dalam Gambar 3-13.



Gambar 3-13. Rangkaian LCD

3.1.10. Unit Suara

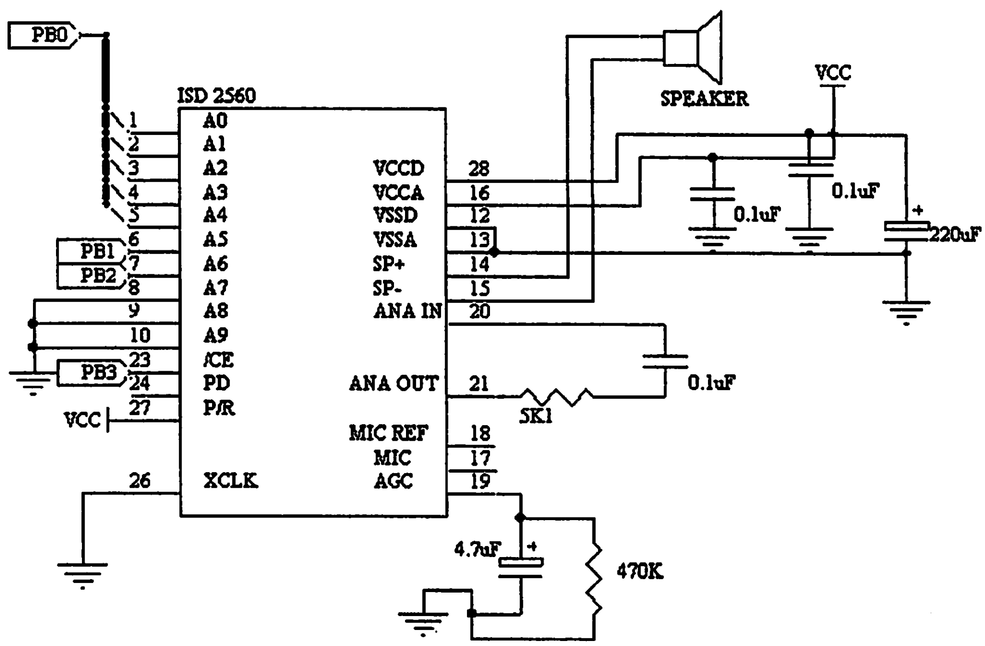
Rangkaian ISD 2560 dengan mikrokontroler 89C51 untuk memutar suara ditunjukkan dalam gambar 3-14. Pin alamat A0 – A4 ISD 2560 dihubungkan dengan PB0 PPI 8255, alamat A5, A6 dahubungkan dengan PB1, PB2 PPI 8255 dan alamat A7, A8, A9 dihubungkan dengan GND. Sebagai pin *control* untuk memutar suara, CE dihubungkan dengan PB3 PPI 8255.

Dalam perencanaan IC ISD 2560 yang mempunyai dua fungsi yaitu mode message address dan mode operasional. Dalam perencanaan berdasarkan data sheet ISD 2560 mampu merekam 60 detik.

Selanjutnya untuk mengetahui dan untuk melakukan pengontrolan atau langkah – langkah cara penggunaan dari ISD 2560 ini maka dapat dilihat sesuai pada tabel 3-4 (Sinyal *control* ISD) yang mana pada tabel tersebut berisi langkah – langkah pemberian sinyal kontrol pada ISD 2560 yang dikondisikan dalam keadaan *record* maupun *playback* serta memulai atau mengakhiri suatu *record* atau *playback*. Untuk lebih jelasnya marilah kita perhatikan tabel berikut.

Tabel 3-3. Sinyal *control* ISD

Langkah *control*	*Function*	*Action*
1	Pemilihan *rec/playback mode*	[1] /PD = *low* [2] P/R= *as desired*
2	*Set address* memulai *rec/playback*	Pemilihan alamat A0 – A9
3A	Mulai *playback*	P/R= *high*, $\overline{CE}$ = *low*
3B	Mulai *record*	P/R = *low*, $\overline{CE}$ = *low*
4A	Mengakhiri *playback*	Otomatis
4B	Mengakhiri *record*	PD atau $\overline{CE}$ = *high*

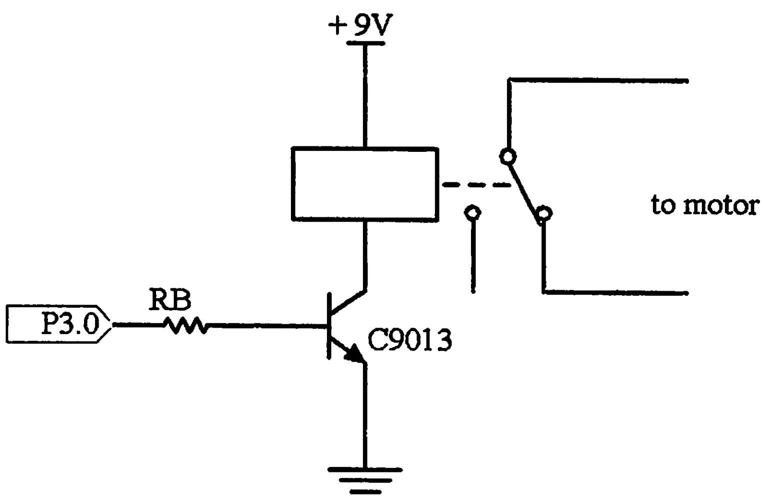


Gambar 3-14. Rangkaian ISD

3.1.11. Penggerak relay

Bagian ini digunakan untuk mengendalikan relay yang akan memutuskan dan menghubungkan mesin mobil (dalam perencanaan ini menggunakan motor DC).

Rangkaian penggerak relay ditunjukkan dalam gambar 3-15. Rangkaian penggerak relay diperlukan karena arus keluaran mikrokontroler terlalu kecil untuk menggerakkan relay. Untuk keperluan ini digunakan transistor C9013.



Gambar 3-15 Rangkaian penggerak relay

Apabila Vin=0, transistor bekerja dalam keadaan terputus. Dalam hal ini tidak ada arus mengalir melalui beban. Tetapi bila Vin cukup besar, titik operasi beralih dari keadaan putus ke keadaan jenuh.

Dari data sheet transistor (C9013) diketahui Hfe=64, Ic=100mA. Tegangan masukan basis merupakan keluaran mikrokontroler, sehingga masukan basis untuk level high minimum 2V, tegangan V_{BE}=0,7V. Maka untuk menghasilkan kejenuhan, besarnya R_B adalah :

$R_B = (V_{CC} - V_{BE}) / I_B$

Nilai I_B dapat dicari melalui rumus :

$I_B = I_C$ / Hfe

$= 100.10^{-3} / 64$

$I_B = 1{,}56$mA

Setelah I_B didapatkan maka nilai R_B dapat dicari :

$R_B = (5 - 0{,}7) / 1{,}56.10^{-3}$

$= 2{,}76.10^{3}$

$R_B = 2{,}76$ kΩ

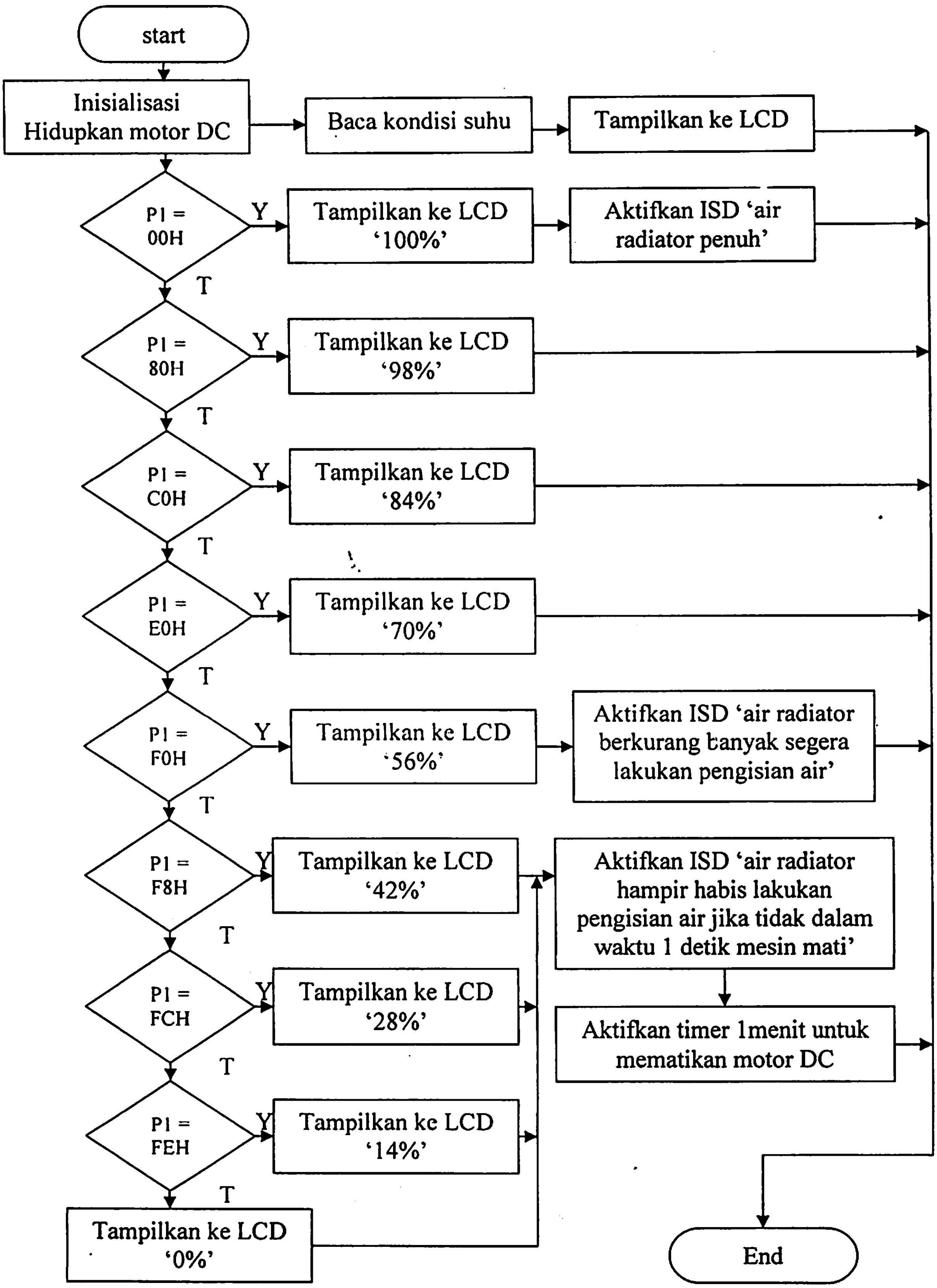
3.2. Perancanagan perangkat lunak

Untuk pemakaian mikrokontroler didalam suatau sistem, perlu direncanakan perangkat lunak mikrokontroler yang dapat mengatur sistem tersebut. Perangkat lunak disini adalah susunan perintah – perintah (program) didalam memori yang harus dilaksanakan oleh mikrokontroler.

Alamat dari memori program ini diatur oleh hubungan antara kaki EA dengan Vcc (kutub positif) atau Vss (kutub negatif) bila kaki EA dihubungkan dengan Vcc, maka program akan mengambil dari ROM dalam bentuk alamat 0000H samapai dengan 0FFFH. Sedangkan untuk alamat 1000H sampai FFFFH diambil dari ROM luar. Bila kaki EA dihubungkan dengan Vss maka seluruh program akan diambil dari luar. Dalam rancangan ini EA dihubungkan dengan Vcc.

Perangkat lunak untuk mengendalikan sistem ini terdiri dari proses pengambilan data dari unit masukan yaitu : sensor level dan suhu mengolahnya dan ditampilkan melalui LCD dan ISD.

Berikut ini *flowchart* program utama yang digunakan pada pendeteksian level air dan suhu pada radiator.



Gambar 3-16. *Flowchart* perangkat lunak

Gambar 3-17 *Flowchart* untuk mengaktifkan ISD

BAB IV

PENGUJIAN ALAT

4.1 Tujuan

Bab ini membahas tentang pengujian dan analisis alat yang telah dibuat. Secara umum, pengujian ini bertujuan untuk mengetahui apakah piranti yang telah direalisasikan dapat bekerja sesuai dengan spesifikasi perencanaan yang telah ditetapkan. Pengujian piranti ini dilakukan dalam dua tahap. Pertama, dilakukan pengujian terhadap perangkat keras pada masing-masing blok rangkaian penyusun sistem antara lain sensor, rangkaian ADC, LCD, dan ISD. Pengujian kedua dilakukan pada sistem secara keseluruhan dengan mengintegrasikan perangkat keras dan perangkat lunak untuk mengetahui unjuk kerja sistem dengan melakukan pengaturan suhu dan waktu sesuai dengan tabel yang telah dibuat. Adapun tujuan pengujian yang dilakukan terhadap sistem adalah sebagai berikut:

- Mengetahui unjuk kerja rangkaian sensor dan ADC.
- Mengetahui unjuk kerja rangkaian µC.
- Mengetahui unjuk kerja rangkaian ISD.
- Mengetahui unjuk kerja sistem secara keseluruhan dengan mengintegrasikan perangkat keras dan perangkat lunak.

4.2. Pengujian rangkaian sensor dan ADC

4.2.1. Pengujian sensor level

- Tujuan

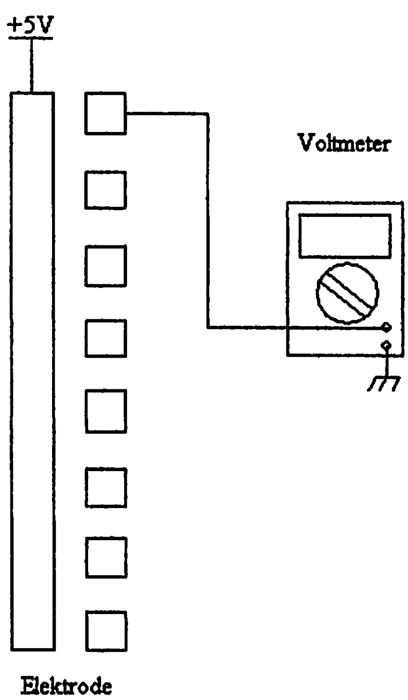
Untuk mengetahui apakah sensor level (*electrode*) dapat digunakan pada alat yang direncanakan.

- Peralatan yang digunakan

1. Power supply 5V DC
2. Voltmeter

- Prosedur pengujian

1. Membuat rangkaian seperti gambar 4-1 di bawah ini :



Gambar 4-1. Pengujian sensor level

2. Memasang power supply 5V DC pada input sensor level
3. Memasang multimeter pada output sensor level

4. membaca nilai output yang ditampilkan pada multimeter saat sensor level belum terkena air dan terkena air.

- Hasil pengujian

Hasil pengujian ditunjukkan dalam tabel 4-1.

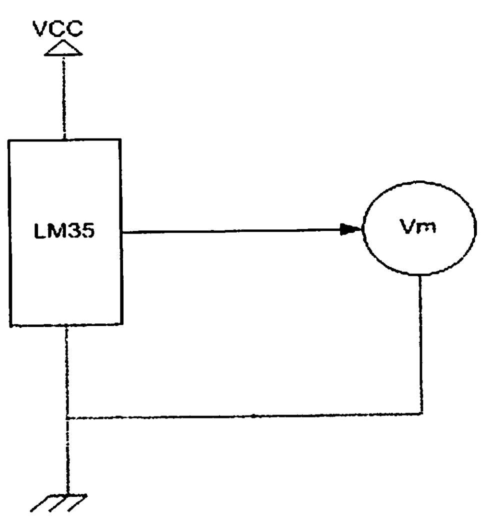
Tabel 4-5. Hasil Pengujian sensor level

V_{in} (volt)	Kondisi sensor	V_{out} (volt)
5	Saat belum terkena air	0
5	Saat terkena air	5

4.2.2. Pengujian Output Lm 35 Tanpa Penguat

Besarnya kenaikan tegangan pada LM35 tanpa penguatan adalah 10 mV/°C. Sehingga :

$$V = (\text{Suhu}) \times 10\ \text{mV/°C}$$



Gambar 4-2. Pengujian Rangkaian *Sensor* Suhu Tanpa Penguatan.

Dengan rumus diatas maka didapatkan tegangan keluaran (*output*) dari *sensor* suhu seperti pada table 4-2 berikut :

Tabel 4-2. Hasil Pengukuran dan Perhitungan *Sensor* Suhu Tanpa Penguatan

No	Suhu (°C)	Pengukuran (Volt)	Perhitungan (Volt)
1	25	0,26	0,25
2	30	0,31	0,3
3	34	0,33	0,34
4	35	0,34	0,35
5	37	0,36	0,37
6	38	0,37	0,38
7	40	0,39	0,4
8	42	0,41	0,42
9	43	0,42	0,43
10	44	0,43	0,44
11	45	0,45	0,45
12	48	0,47	0,48
13	50	0,5	0,5
14	54	0,53	0,54
15	55	0,56	0,55
16	58	0,57	0,58
17	60	0,59	0,6
18	63	0,62	0,63
19	65	0,64	0,65
20	68	0,67	0,68
21	70	0,69	0,7
22	72	0,71	0,72
23	75	0,75	0,75

Dari data diatas dapat maka dapat dianalisa kesalahan, yaitu sebagai berikut :

$$\% \text{ kesalahan} = \frac{\textit{Hasil Perhitungan} - \textit{Hasil Pengukuran}}{\textit{Hasil Pengukuran}} x 100\%$$

Dengan menggunakan rumus diatas maka dapat dihitung sebagai berikut :

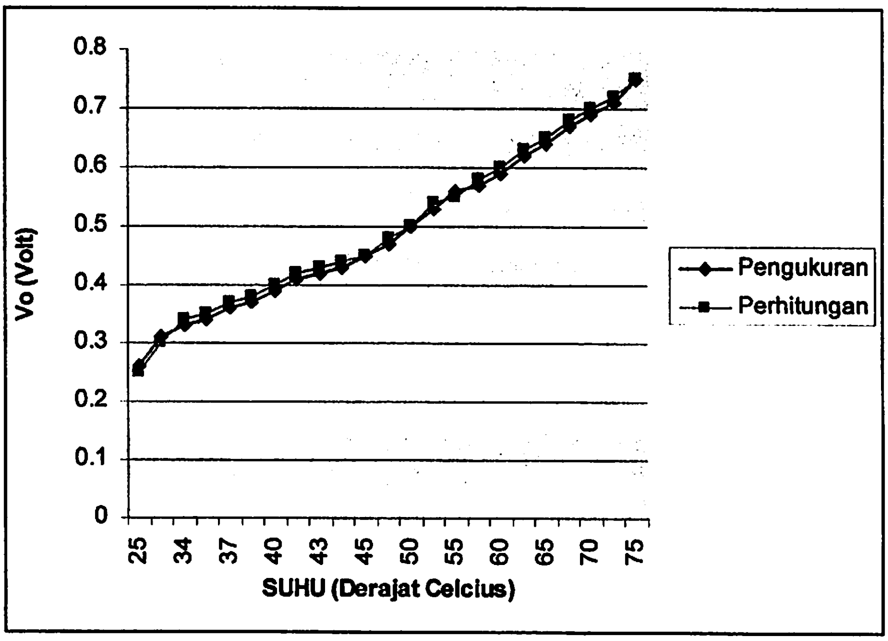
% kesalahan = (0,25-0,26) x 100% / 0,26

= 3,85%

Tabel 4-3. Hasil Kesalahan Sensor Suhu Tanpa Penguatan

No.	Suhu (°C)	V_{output} (volt)		Kesalahan (%)
		Pengukuran	Perhitungan	
1	25	0,26	0,25	3,85
2	30	0,31	0,3	3,23
3	34	0,33	0,34	3,03

4	35	0,34	0,35	2,94
5	37	0,36	0,37	2,78
6	38	0,37	0,38	2,7
7	40	0,39	0,4	2,56
8	42	0,41	0,42	2,44
9	43	0,42	0,43	2,38
10	44	0,43	0,44	2,33
11	45	0,45	0,45	0
12	48	0,47	0,48	2,13
13	50	0,5	0,5	0
14	54	0,53	0,54	1,89
15	55	0,56	0,55	1,79
16	58	0,57	0,58	1,75
17	60	0,59	0,6	1,69
18	63	0,62	0,63	1,61
19	65	0,64	0,65	1,56
20	68	0,67	0,68	1,49
21	70	0,69	0,7	1,45
22	72	0,71	0,72	1,41
23	75	0,75	0,75	0
				$\bar{X} = 2,03$

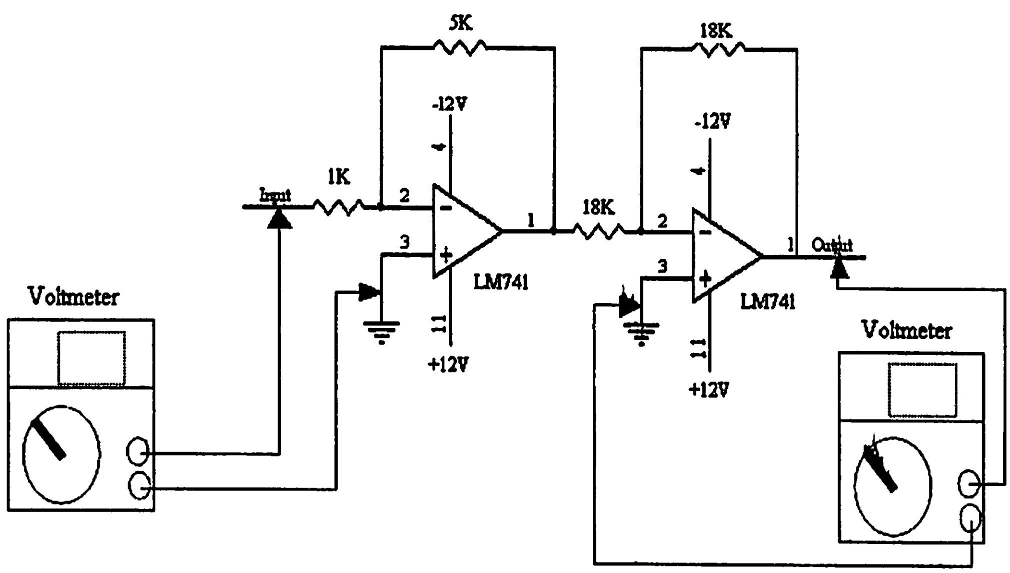


Grafik 4-1. Linieritas *Sensor* Suhu Tanpa Penguatan

4.2.3. Pengujian Penguat Sinyal

Tujuan pengujian penguat sinyal adalah untuk mengetahui tanggapan keluaran penguat sinyal LM 741 seperti dalam Gambar 4-3. apabila diberi sinyal masukan dengan penguatan (A_V) yang telah ditentukan yaitu 5 kali penguatan. Peralatan yang dipergunakan dalam pengujian ini antara lain catu daya dan Multimeter.

Pengujian penguatan Av dapat dilakukan dengan cara menggunakan Multimeter yang berfungsi untuk mengetahui besar nilai V_{Tout} , Vin, dan Vout dengan masukan dari sumber tegangan.



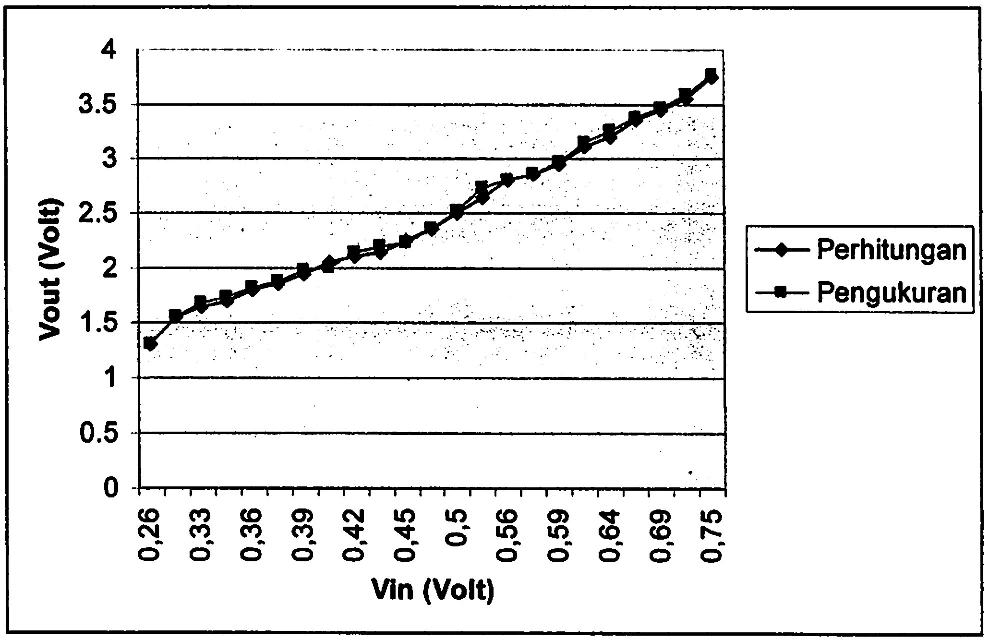
Gambar 4-3. Pengujian Penguatan Penguat Sinyal LM 741

Langkah-langkah pengujian penguatan penguat sinyal LM 741 dengan menggunakan *Multi meter* adalah sebagai berikut :

- Menyiapkan rangkaian penguat Sinyal seperti dalam Gambar 4-3, serta memastikan bahwa catu daya 12V dan –12V DC telah terpasang dan hubungan pada rangkaian telah benar.
- Menghubungkan sumber tegangan dengan masukan input dalam Gambar 4-2.
- Setelah susunan dan hubungan antar rangkaian telah benar aktifkan sumber tegangan dan rangkaian penguat sinyal.
- Selanjutnya mengukur tegangan pada V_{input} dan V_{output}.

Tabel 4-4 Hasil pengujian Penguat Sinyal dengan Multimeter

No.	V_{input} (volt)	V_{output} (volt)		Kesalahan (%)
		Perhitungan	Pengukuran	
1	0,26	1,3	1,3	0
2	0,31	1,55	1,55	0
3	0,33	1,65	1,67	1,2
4	0,34	1,7	1,74	2,3
5	0,36	1,8	1,82	1,1
6	0,37	1,85	1,87	1,07
7	0,39	1,95	1,98	1,52
8	0,41	2,05	2	2,5
9	0,42	2,1	2,15	2,33
10	0,43	2,15	2,2	2,27
11	0,45	2,25	2,23	0,9
12	0,47	2,35	2,36	0,42
13	0,5	2,5	2,51	0,4
14	0,53	2,65	2,74	3,28
15	0,56	2,8	2,8	0
16	0,57	2,85	2,86	0,35
17	0,59	2,95	2,97	0,67
18	0,62	3,1	3,15	1,59
19	0,64	3,2	3,25	1,54
20	0,67	3,35	3,37	0,59
21	0,69	3,45	3,47	0,58
22	0,71	3,55	3,59	1,11
23	0,75	3,75	3,76	0,27
				$\bar{X} = 1,13$



Grafik 4-2. Linieritas *Sensor* Suhu Dengan Penguatan

4.2.4. Pengujian Rangkaian ADC

- Tujuan

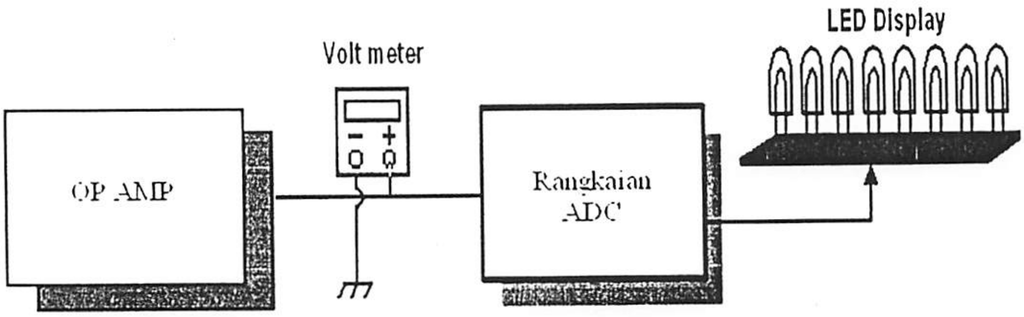
Tujuan dari pengujian rangkaian ADC adalah untuk mengetahui level tegangan keluaran ADC dan kelinieran hasil konversi ADC.

- Peralatan yang diperlukan

1. Voltmeter
2. Catu daya 5 volt
3. Led Display

- Prosedur Pengujian

1. Rangkaian dibuat seperti Gambar 4-4.



Gambar 4-4. Diagram blok Pengujian Rangkaian ADC

2. Memasang catu rangkaian sebesar 5 volt
3. Mengamati keluaran rangkaian pada LED Display dan tegangannya dengan Volt meter.
4. Mengulangi langkah 3 untuk tegangan yang berbeda.

- Analisa :

ADC menggunakankonversi sistem SAR (*Succesive Aprproximation Register*) yaitu konversi dengan pendekatan berturut-turut.

Diketahui :

V_{REF} = 5V

Vinput = 1,3V

Konversi data dari bit tertinggi :

1. Clock 1

   Data SAR = 10000000 = 128_D

   $V = (128 / 2^8 - 1)5$

   $= (128 / 256 - 1)5$

   $= (128 / 255)5$

   V = 2,5V

Karena V = 2,5V lebih besar dari Vin = 1,3V maka D_7 = 0

2. Clock 2

   Data SAR = 01000000 = 64_D

   V = (64 / 255)5

   V = 1,25V

   Karena V = 1,25V lebih kecil dari Vin = 1,3V maka D_6 = 1

3. Clock 3

   Data SAR = 01100000 = 96_D

   V = (96 / 255)5

   V = 1,88V

   Karena V = 1,88V lebih besar dari Vin = 1,3V maka D_5 = 0

4. Clock 4

   Data SAR = 01010000 = 80_D

   V = (80 / 255)5

   V = 1,56V

   Karena V = 1,56V lebih besar dari Vin = 1,3V maka D_4 = 0

5. Clock 5

   Data SAR = 01001000 = 72_D

   V = (72 / 255)5

   V = 1,41V

   Karena V = 1,41V lebih besar dari Vin = 1,3V maka D_3 = 0

6. Clock 6

   Data SAR = 01000100 = 68_D

$V = (68 / 255)5$

$V = 1,33V$

Karena $V = 1,33V$ lebih besar dari $Vin = 1,3V$ maka $D_2 = 0$

7. Clock 7

Data SAR = 01000010 = 66_D

$V = (66 / 255)5$

$V = 1,29V$

Karena $V = 1,29V$ lebih kecil dari $Vin = 1,3V$ maka $D_1 = 1$

8. Clock 8

Data SAR = 01000011 = 67_D

$V = (67 / 255)5$

$V = 1,31V$

Karena $V = 1,31V$ lebih besar dari $Vin = 1,3V$ maka $D_0 = 0$

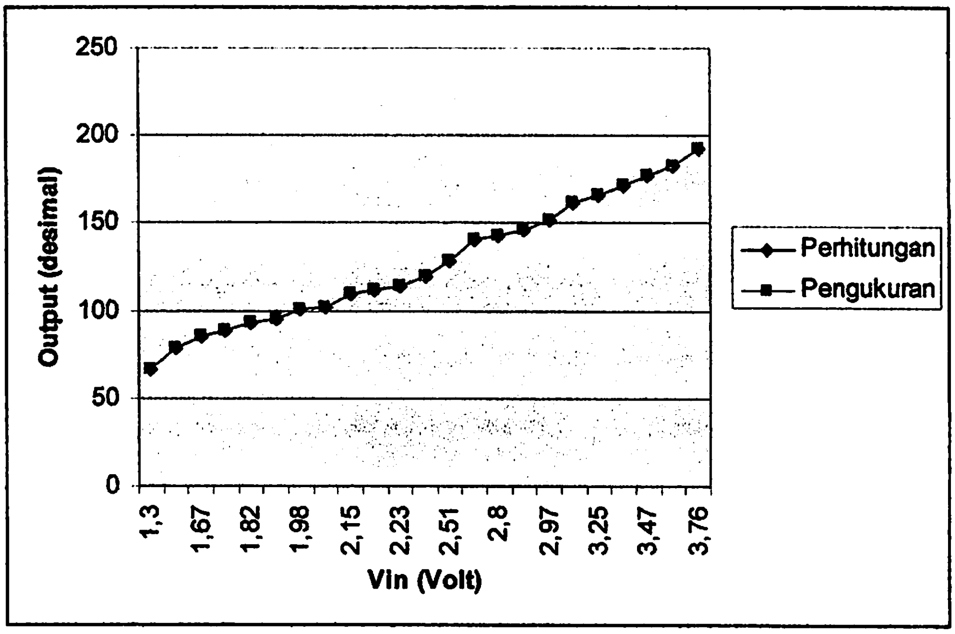
Dari perhitungan diatas didapatkan data output ADC = 01000010 = 66_D

Dengan perhitungan seperti diatas maka didapatkan data sebagai berikut :

Tabel 4-5. Hasil dan Analisis Pengujian Rangkaian ADC

No.	V_{input} (volt)	Output (desimal)		Kesalahan (%)
		Perhitungan	Pengukuran	
1	1,3	66	66	0
2	1,55	79	79	0
3	1,67	85	85	0
4	1,74	89	89	0
5	1,82	93	93	0
6	1,87	95	95	0
7	1,98	101	101	0
8	2	102	102	0
9	2,15	109	109	0
10	2,2	112	112	0
11	2,23	114	114	0
12	2,36	120	120	0

13	2,51	128	128	0
14	2,74	140	140	0
15	2,8	143	143	0
16	2,86	146	146	0
17	2,97	151	151	0
18	3,15	161	161	0
19	3,25	166	166	0
20	3,37	172	172	0
21	3,47	177	177	0
22	3,59	183	183	0
23	3,76	192	192	0
				$\bar{X} = 0$



Grafik 4-3. Linieritas Rangkaian ADC 0809

4.3. Pengujian Sistem Mikrokontroler

- Tujuan

Untuk mengetahui kondisi awal dari mikrokontroler apakah sudah sesuai dengan yang direncanakan.

- Peralatan yang dibutuhkan

1. Komputer
2. Downloader
3. Led Display

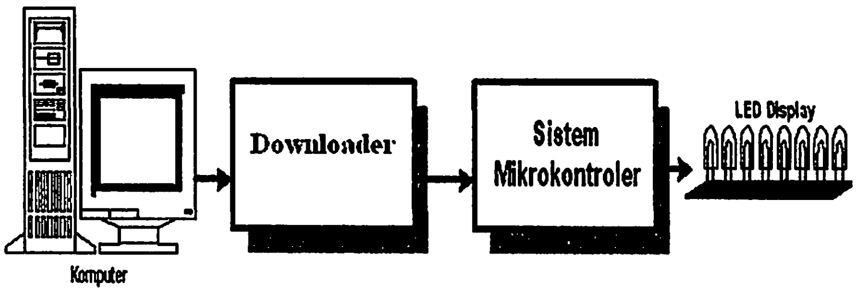
- Prosedur Pengujian

1. Membuat program yang digunakan dalam pengujian mikrokontroler.

   Program yang digunakan dalam pengujian mikrokontroler ini merupakan program sederhana yang meletakkan $0F_H$ dan $F0_H$ pada ACC secara bergantian kemudian memindahkannya pada *Port* 1 89C51. Program yang dibuat adalah sebagai berikut :

```
ORG      0000H
         JMP     START
START:   MOV     A,#0FH
         MOV     P1,A
         CALL    TUNDA
         MOV     A,#F0H
         MOV     P1,A
         CALL    TUNDA
         JMP     START
TUNDA:   MOV     R3,#0FFH
TUNDA1:  MOV     R2,#0FFH
         DJNZ    R2,$
         MOV     R1,#0FH
         DJNZ    R1,$
         DJNZ    R3,TUNDA1
         RET
         END
```

2. Rangkaian dibuat seperti Gambar 4-5
3. Memasang catu rangkaian sebesar 5 volt
4. Download program diatas .
5. Mengamati keluaran pada LED Display .



Gambar 4-5 Diagram blok Pengujian Mikrokontroler

- Hasil Pengujian

Hasil pengujian ditunjukkan dalam Tabel 4-6.

Tabel 4-6 Hasil Pengujian Sistem Mikrokontroler

Kondisi	Keluaran pada LED Display							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Satu	1	1	1	1	0	0	0	0
Dua	0	0	0	0	1	1	1	1

- Analisis Pengujian

Dari hasil pengujian dalam tabel 4-6 dapat dilihat bahwa *port* 1 memberikan logika $F0_H$ dan $0F_H$ secara bergantian sesuai dengan isi program.

4.4. Pengujian Rangkaian Tampilan

- Tujuan

Untuk mengetahui kemampuan rangkaian tampilan yang sudah dibuat apakah dapat mendukung sistem yang direncanakan untuk memampilkan data pada LCD.

- Peralatan yang dibutuhkan

1. Komputer
2. Downloader

3. Sistem Mikrokontroler
4. LCD

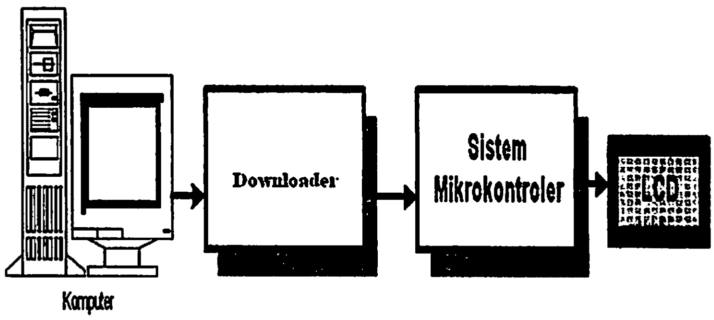
- Prosedur Pengujian

1. Menyusun rangkaian seperti dalam Gambar 4-6
2. Menjalankan program untuk menampilkan tulisan

```
              ORG OH
MULAI:        CALL INISIALISASI
              MOV DPTR,#TULISAN
              MOV R3,#16
              MOV A,#80H
              CALL TULIS_INST
TULIS:        CLR A
              MOVC A,@A+DPTR
              INC DPTR
              CALL TULIS_DATA
              DJNZ R3,TULIS
              SJMP  MULAI
INISIALISASI:
              CALL TUNDA
              MOV A,#3FH
              CALL TULIS_INST
              MOV A,#0EH
              CALL TULIS_INST
              MOV A,#06H
              CALL TULIS_INST
              MOV A,#01H
              CALL TULIS_INST
              RET
TULIS_INST:
              CLR P1.0
              MOV P0,A
              SETB P1.1
              CLR P1.1
              CALL TUNDA
              RET
TULIS DATA:
              SETB P1.0
              MOV P0,A
              SETB P1.1
              CLR P1.1
              CALL TUNDA
```

```
                RET
TUNDA:          MOV R0,#0FFH
TUNDA1:         MOV R1,#00H
                DJNZ R1,$
                DJNZ R0,TUNDA1
                RET
TULISAN:        DB 'ITN MALANG     '
                END
```

3. Mengamati keluaran pada LCD



Gambar 4-6 Diagram blok Pengujian Rangkaian Tampilan

4.5. Pengujian Penyimpan Suara

a. Tujuan

- Mengetahui apakah IC penyimpan suara dapat menyimpan suara yang telah direkam.

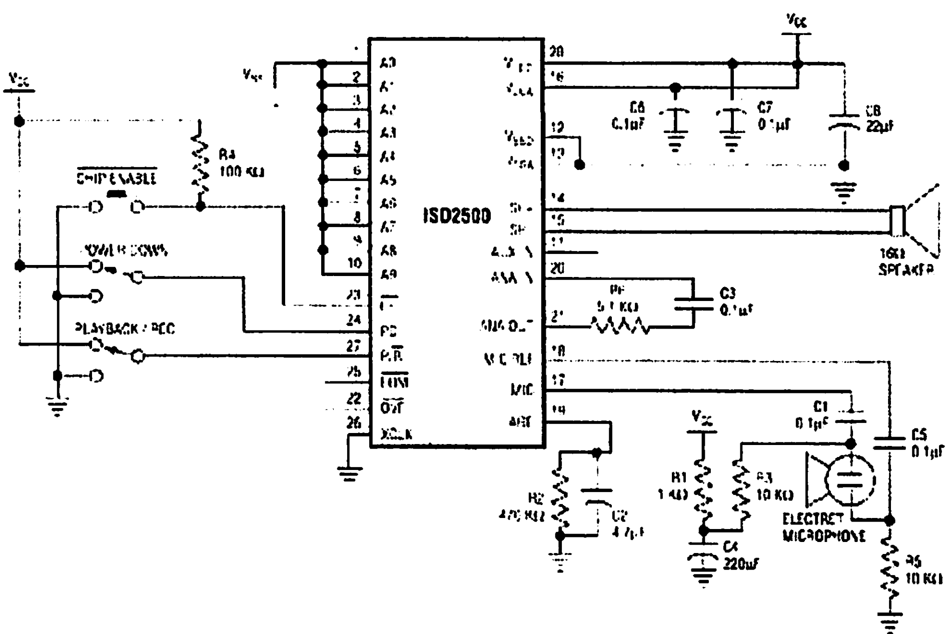
b. Peralatan yang digunakan

- Catu daya 5V DC.
- IC ISD
- Modul ISD

c. Prosedur pengujian

Pasang rangkaian penyimpan suara seperti gambar 4-7. Kemudian aktifkan rekam dan selanjutnya informasi suara dikeluarkan. Setelah beberapa detik, hentikan perekaman suara.

Untuk memutar ulang suara yang telah direkam, aktifkan *play*.



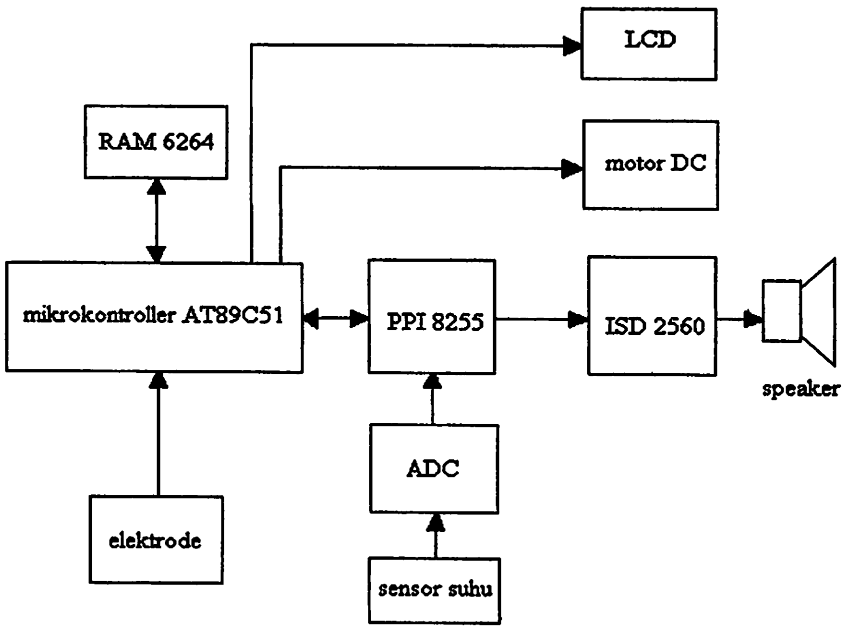
Gambar 4-7 Pengujian ISD2500

d. Hasil Pengujian

Dari hasil pengujian, maka didapatkan bahwa IC ISD dapat menyimpan suara seperti yang telah direncanakan.

4.6. Pengujian secara keseluruhan

Pengujian sistem secara keseluruhan dengan menggabungkan masing – masing rangkaian (blok) dan menjalankan perangkat lunak (software). Pengujian dimaksudkan untuk mengetahui apakah sistem yang telah dibuat mampu dioperasikan. Pertama – tama mengisi air pada radiator sampai penuh kemudian menghubungkan alat dengan sumber tegangan. Biarkan alat bekerja dan kurangi air pada radiator sampai habis. Jika tampilan pada LCD berubah – ubah sesuai dengan keadaan air pada radiator yaitu nilai suhu naik dan nilai level air turun juga jika ISD mengeluarkan suara peringatan sesuai dengan keadaan air pada radiator maka alat telah berfungsi dengan benar. Blok diagram alat ditunjukkan



Gambar 4-8. Blok Diagram Sistem

BAB V

PENUTUP

5.1. Kesimpulan

Berdasarkan perancangan *hardware* dan *software* dan pengujian alat pendeteksi level air radiator dilengkapi suhu dengan keluaran suara berbasis mikrokontroler AT89C51 dapat disimpulkan :

1. Pada percobaan pengujian sensor *electrode*, menyentuhnya air dengan *electrode* mengakibatkan pin – pin terhubung dengan Vcc (+5V) atau berlogika (1) dan akan berlogika (0) bila tidak tersentuh air, sehingga dapat dibaca posisi air dalam radiator.
2. Pada percobaan pengujian sensor suhu terdapat kesalahan antara perhitungan dan pengukuran dengan kesalahan rata – rata 2,03%, untuk pengujian penguatan output suhu terdapat kesalahan rata – rata 1,13% dan untuk pengujian ADC terdapat kesalahan rata –rata 0%.
3. Pada perancangan ini untuk tampilan suhu dibatasi 20°C sampai 100°C saja.
4. Pada ISD pengalamatannya tidak boleh masuk pada alamat berikutnya, karena suara yang telah direkam pada alamat berikutnya akan terpotong.
5. Tidak presisinya alat ukur menyebabkan selisih antara nilai perhitungan dan pengukuran.

5.2. Saran

1. Pada keluaran suara ISD dapat ditambahkan *amplifier* untuk menguatkan suara.
2. Sensor level air (*electrode*) masih mempunyai kelemahan pada aır yang tidak tenang terutama pada radiator jadi untuk sensor level air bisa dikembangkan atau diganti dengan sensor level air lainnya yang lebih baik.
3. Alat yang dirancang masih belum sempurna maka perlu dilakukan penelitian lebih lanjut.

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[3]. Paulus Andi Nalwan, "*Teknik Antar Muka dan Pemrograman Mikrokontroler AT89C5*", PT Elex Komputindo, Jakarta, 2003.

[4]. "*Pelatihan Microkontroller MCS-51 Programming and Interfacing*", Hafindo Electric & Education, Malang, 2001.

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LAMPIRAN

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MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Anton Kusworo
Nim : 0017168
Masa Bimbingan : 19-Nov-2004 s/d 22-May-2005
Judul Skripsi : Perancangan dan pembuatan slst pendeteksi level radiator dengan keluaran suara pada mobil menggunakan Mikrokontroller AT89C51

NO	Tanggal	Uraian	Paraf Pembimbing
1.	7/3 05	Bab I	[signature]
2.	7/3 05	Bab II	[signature]
3.	7/3 05	Bab III	[signature]
4.	7/3 05	Bab IV	[signature]
5.	10/3 05	Demo alat	[signature]
6.	18/3 05	Persiapan seminar	[signature]
7.	21/3 05	Bab V	[signature]
8.			
9.			
10.			

Malang, 21 Maret 2005
Dosen Pembimbing

[signature]

Ir. F. Yudi Limpraptono, MT

Form. S-4a

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JL. BENDUNGAN SIGURA-GURA 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Anton Kusworo
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Masa Bimbingan : 19-Nov-2004 s/d 22-May-2005
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NO	Tanggal	Uraian	Paraf Pembimbing
1.	5/12 04	Bab III, Konsep perancangan	[signature]
2.	10/1 05	Bab III, Sensor level	[signature]
3.	24/1 05	Bab I, Bab II, Bab III	[signature]
4.	5/2 05	Bab IV Analisa ADC SAR	[signature]
5.	10/3 05	[illegible] seminar.	[signature]
6.	20/3 05	Acc Laporan SKRIPSI	[signature]
7.			
8.			
9.			
10.			

Malang, 20 Maret 2005
Dosen Pembmbing

[signature]

I Komang Somawirata,ST

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KONSENTRASI TEKNIK ELEKTRONIKA

LEMBAR BIMBINGAN SKRIPSI

Nama	: Anton Kusworo
NIM	: 00.17168
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Judul Skripsi	: Perancangan dan Pembuatan Alat Pendeteksi Level Air Radiator dengan Keluaran Suara pada Mobil Menggunakan Mikrokontroller AT89C51
Tanggal Pengajuan Skripsi	: 19 Mei 2004
Selesai Penulisan Skripsi	: 22 Mei 2005
Dosen Pembimbing I	: Ir. F. Yudi Limpraptono, MT
Dosen Pembimbing II	: I Komang Somawirata, ST
Telah Dievaluasi Dengan Nilai	: Dosen Pembimbing I : 90 (A)
	Dosen Pembimbing II : 90 (A)

Diperiksa Dan Disetujui,
Dosen Pembimbing I

(Ir. F. Yudi Limpraptono, MT)
NIP. P. 1039500274

Diperiksa Dan Disetujui,
Dosen Pembimbing II

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Mengetahui
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NAMA :
N I M :
Perbaikan meliputi :

Malang, 200

(____________________)

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JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

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NAMA :
N I M :
Perbaikan meliputi :

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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama : Anton Kusworo

NIM : 00.17168

Masa Bimbingan : 19 Mei 2004 s/d 22 Mei 2005

Judul : Perancangan dan Pembuatan Alat Pendeteksi Level Air Radiator dengan Keluaran Suara pada Mobil Menggunakan Mikrokontroller AT89C51

No	Tanggal	Uraian	Paraf
1	8 April 2005	Perbaiki gambar dan keterangan pada gambar	
2	8 April 2005	Grafik untuk pengujian alat	

Disetujui

Penguji I

(Ir. Usman Djuanda, MM)

Penguji II

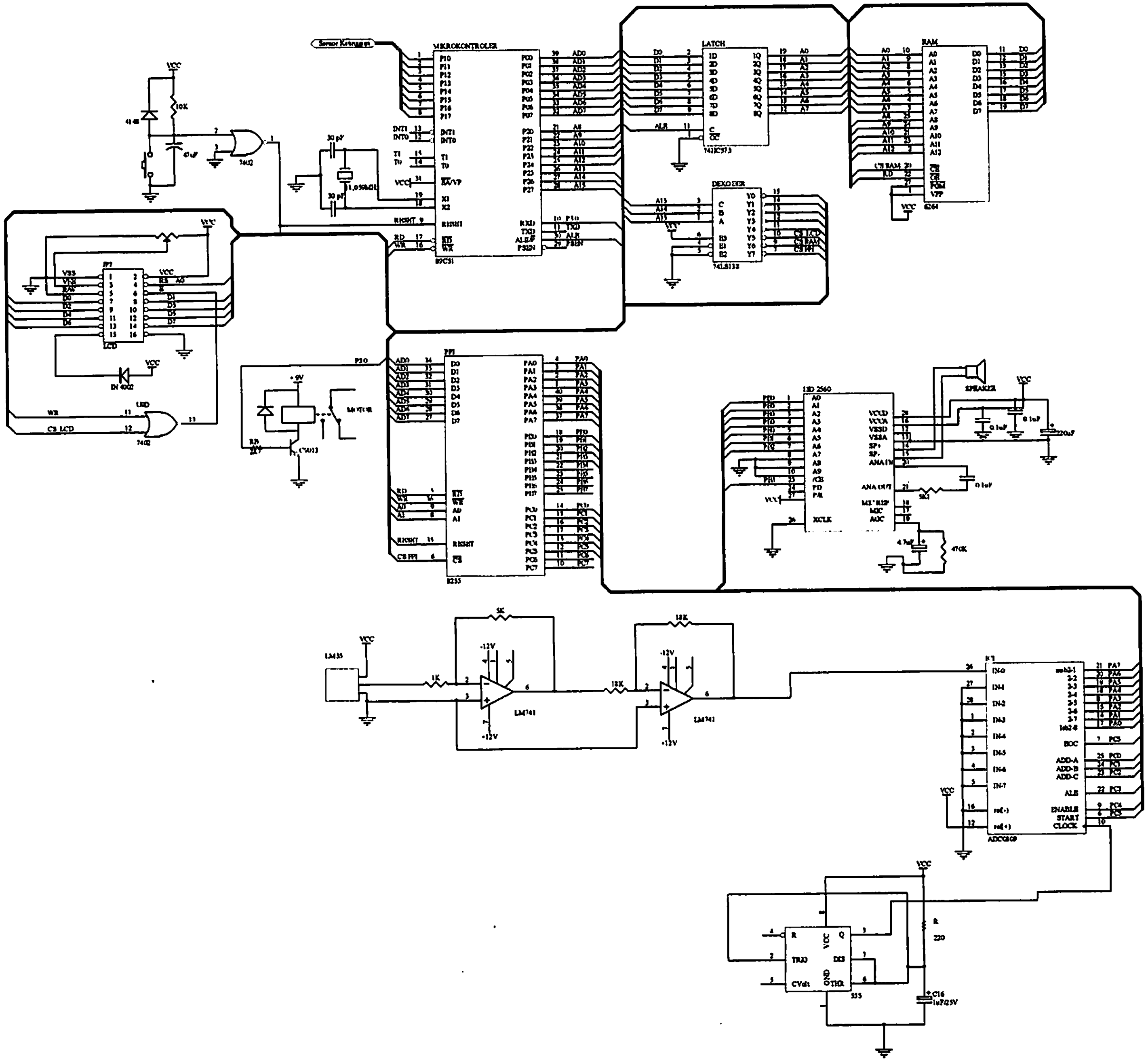
(Ir. Mimien Mustikawati)

Mengetahui
Dosen Pembimbing I

(Ir. F. Yudi Limpraptono, MT)
NIP. P. 1039500274

Mengetahui
Dosen Pembimbing II

(I Komang Somawirata, ST)
NIP. P. 1030100361



Title
Size
C
Number
Revision

```
dphh            Data    20h
dpll            Data    21h
Suhu            Data    27h
ADC             Data    28h
TmpLevel        Data    2Eh
TmpLevelOld     Data    2Fh
TmpRelay        Data    30h
CntWaktu        Data    31h
Motor           Bit     P3.0

        Mov     CntWaktu,#60
        Mov     TmpLevelOld,#0FFh
        Mov     SP,#40h

        Setb    Motor

        Mov     A,#90h
        Call    PPI_Initialization
        Mov     A,#90h
        Call    PPI_Initialization

        Mov     A,#0FFh
        Call    PPI_Send_Port_C

        Mov     A,#0FFh
        Call    PPI_Send_Port_B

        Call    LCD_Initialization
        Call    LCD_Clrscr
        Call    LCD_Clrscr
        Call    LCD_Clrscr
        Call    Delay_Fix_100ms
        Call    LCD_Line1
        Mov     DPTR,#txt_Suhu1
        Call    LCD_String

        Call    LCD_Line2
        Mov     DPTR,#txt_Tinggi1
        Call    LCD_String
        Mov     TmpRelay,#0h

start:
;       Call    AmbilSuhu

        Mov     R0,#15h
        Call    LCD_Cursor_Position
        Mov     R0,#15h
        Call    LCD_Cursor_Position

        Call    AmbilSuhu
        Mov     Suhu,ADC
        Mov     A,Suhu

        Call    ShowSuhu

        Mov     R0,#27h
```

```
        Call    LCD_Cursor_Position
        Mov     R0,#27h
        Call    LCD_Cursor_Position
        Call    AmbilTinggi

        Call    ProsesISD

;------------

        Mov     A,TmpRelay
        Cjne    A,#00,KurangiWaktuRelay
        Mov     CntWaktu,#60
        Jmp     TampilWaktuRelay
KurangiWaktuRelay:
        Mov     A,CntWaktu
        Cjne    A,#0,KurangiWaktuRelay1
        Jmp     TampilWaktuRelay
KurangiWaktuRelay1:
        Dec     CntWaktu
TampilWaktuRelay:
        Mov     R0,#2Dh
        Call    LCD_Cursor_Position
        Mov     R0,#2Dh
        Call    LCD_Cursor_Position
        Mov     A,CntWaktu
        Call    Conversion_Hexa_to_Bcd
        Mov     A,CntWaktu
        Cjne    A,#0,MatiMotor
        Clr     Motor
        Jmp     Mbalik
MatiMotor:
        Setb    Motor
Mbalik:
        Call    Delay_Fix_1s
        Jmp     start

Subroutine Conversion_Hexa_to_Bcd:
        Push    B
        Mov     R0,A
        Mov     A,#10
        Xch     A,B
        Div     AB
        Swap    A
        Add     A,B
        Mov     R1,A
        Pop     B
EndSub

Subroutine ProsesISD:
        Mov     A,TmpLevel
        Cjne    A,TmpLevelOld,ProsesISDNext
        Ret
ProsesISDNext:
        Mov     A,TmpLevel
        Cjne    A,#8,ProsesISDNext1
        Mov     A,#0FFh
```

```
        Call     PPI_Send_Port_B ; Full

        Mov      A,#11111000b
        Call     PPI_Send_Port_B
        Call     Delay_Fix_100ms
        Call     Delay_Fix_100ms

        Mov      A,#11110000b
        Call     PPI_Send_Port_B

        Mov      R0,#25
        Call     Delay_Var_100ms

        Mov      A,#0FFh
        Call     PPI_Send_Port_B ; Full

        Mov      TmpLevelOld,TmpLevel
        Ret
ProsesISDNext1:
        Cjne     A,#4,ProsesISDNext3

        Mov      A,#0FFh
        Call     PPI_Send_Port_B ; Full
        Mov      A,#11111010b

        Call     PPI_Send_Port_B
        Call     Delay_Fix_100ms
        Call     Delay_Fix_100ms

        Mov      A,#11110000b
        Call     PPI_Send_Port_B

        Mov      R0,#57
        Call     Delay_Var_100ms

        Mov      A,#0FFh
        Call     PPI_Send_Port_B ; Full

        Mov      TmpLevelOld,TmpLevel
        Ret

ProsesISDNext3:
        Cjne     A,#5,ProsesISDNext4

        Mov      TmpLevelOld,TmpLevel
        Ret
ProsesISDNext4:
        Cjne     A,#6,ProsesISDNext5

        Mov      TmpLevelOld,TmpLevel
        Ret
ProsesISDNext5:
        Cjne     A,#7,ProsesISDNext6

        Mov      TmpLevelOld,TmpLevel
        Ret
```

```
ProsesISDNext6:

        Mov     A,#0FFh
        Call    PPI_Send_Port_B ; Full

        Mov     A,#11111101b
        Call    PPI_Send_Port_B
        Call    Delay_Fix_100ms
        Call    Delay_Fix_100ms

        Mov     A,#11110000b
        Call    PPI_Send_Port_B

        Mov     R0,#95
        Call    Delay_Var_100ms

        Mov     A,#0FFh
        Call    PPI_Send_Port_B ; Full

        Mov     TmpLevelOld,TmpLevel
        Ret
EndSub

Subroutine AmbilTinggi:
        Mov     A,P1
        Cjne    A,#11111111b,Lepel2
        Mov     TmpLevel,#0
        Mov     DPTR,#txt_level0
        Call    LCD_String
        Mov     TmpRelay,#0ffh
        Ret
Lepel2:
        Cjne    A,#11111110b,Lepel3
        Mov     TmpLevel,#1
        Mov     DPTR,#txt_level1
        Call    LCD_String
        Mov     TmpRelay,#0ffh
        Ret
Lepel3:
        Cjne    A,#11111100b,Lepel4
        Mov     TmpLevel,#2
        Mov     DPTR,#txt_level2
        Call    LCD_String
        Mov     TmpRelay,#0ffh
        Ret
Lepel4:
        Cjne    A,#11111000b,Lepel5
        Mov     TmpLevel,#3
        Mov     DPTR,#txt_level3
        Call    LCD_String
        Mov     TmpRelay,#0ffh
        Ret
Lepel5:
        Cjne    A,#11110000b,Lepel6
        Mov     TmpLevel,#4
        Mov     DPTR,#txt_level4
```

```
        Call    LCD_String
        Mov     TmpRelay,#0ffh
        Ret
Lepel6:
        Cjne    A,#11100000b,Lepel7
        Mov     TmpLevel,#5
        Mov     DPTR,#txt_level5
        Call    LCD_String
        Ret
Lepel7:
        Cjne    A,#11000000b,Lepel8
        Mov     TmpLevel,#6
        Mov     DPTR,#txt_level6
        Call    LCD_String
        Mov     TmpRelay,#0h
        Ret
Lepel8:
        Cjne    A,#10000000b,Lepel9
        Mov     TmpLevel,#7
        Mov     DPTR,#txt_level7
        Call    LCD_String
        Mov     TmpRelay,#0h
        Ret
Lepel9:
        Cjne    A,#00000000b,Lepel10
        Mov     TmpLevel,#8
        Mov     DPTR,#txt_level8
        Call    LCD_String
        Mov     TmpRelay,#0h
        Ret
Lepel10:
EndSub

Subroutine ShowSuhu:
        Mov     B,A
        Call    Get_DPTR_Suhu
        Call    LCD_String
EndSub

Subroutine AmbilSuhu:
        Mov     A,#00000000b    ;alamat
        Call    PPI_Send_Port_C
        Nop
        Nop
        Nop
        Nop
        Mov     A,#00001000b    ;ale
        Call    PPI_Send_Port_C
        Nop
        Nop
        Nop
        Mov     A,#00100000b    ;alamat+ale
        Call    PPI_Send_Port_C
        Nop
        Nop
        Nop
```

```
        Nop
        Nop
        Nop
        Nop
        Nop
        Nop
        Nop
        Nop
        Nop
        Nop
        Nop'
        Mov     A,#00110000b    ;ena
        Call    PPI_Send_Port_C
        Nop

        Nop
        Nop
        Nop
        Lcall   PPI_Get_Port_A
        Mov     ADC,A
        Mov     A,#00000000b    ;ena+alamat
        Call    PPI_Send_Port_C
        Nop

        Nop
        Nop
EndSub
;******************************
; subrutin clear lcd1
;******************************
Subroutine LCD_Clrscr:
        Push    ACC
        Mov     A,#01h
        Call    LCD_Command
        Pop     ACC
EndSub
;******************************
; subrutin menempatkan kursor
;******************************
Subroutine LCD_Cursor_Position:
        Push    ACC
        Mov     A,R0
        Anl     A,#0F0h
        Cjne    A,#10h,lcd_cursor_position1
        Mov     A,R0
        Orl     A,#80h
        Call    LCD_Command
        Jmp     lcd_cursor_position_end
lcd_cursor_position1:
        Cjne    A,#20h,lcd_cursor_position_end
        Mov     A,R0
        Anl     A,#0Fh
        Orl     A,#0C0h
        Call    LCD_Command
lcd_cursor_position_end:
        Pop     ACC
```

```
EndSub
;*******************************************
; kirim data ke lcd1
;*******************************************
Subroutine LCD_Data:
        Push    DPL
        Push    DPH
        Push    ACC
        Mov     DPTR,#lcd1
        Movx    @DPTR,A
        Call    LCD_Delay
        Lcall   LCD_Delay
        Lcall   LCD_Delay
        Lcall   LCD_Delay
        Pop     ACC
        Pop     DPH
        Pop     DPL
EndSub
;*********************************************
; kirim instruksi ke lcd1
;*********************************************
lcd0    Equ     0a000h      ;lcd control operation
lcd1    Equ     lcd0+1      ;lcd data operation
Subroutine LCD_Command:
        Push    DPL
        Push    DPH
        Mov     DPTR,#lcd0
        Movx    @DPTR,A
        Lcall   LCD_Delay
        Lcall   LCD_Delay
        Pop     DPH
        Pop     DPL
        Ret
EndSub
Subroutine LCD_Delay:
        Push    01h
        Push    02h
        Push    03h
        Mov     3,#5
tunda1qqqa:
        Mov     1,#30
        Djnz    1,$
        Mov     2,#40
        Djnz    2,$
        Mov     2,#1
        Djnz    2,$
        Djnz    3,tunda1qqqa
        Pop     03h
        Pop     02h
        Pop     01h
EndSub
Subroutine LCD_Initialization:
        Mov     A,#38h      ;function set 8 bit
        Lcall   LCD_Command
        Mov     A,#0Ch      ;display on, cursor off, blink off
        Lcall   LCD_Command
```

```
        Mov     A,#06h      ;increment, no display shift
        Lcall   LCD_Command
        Mov     A,#01h      ;clear display
        Lcall   LCD_Command
EndSub
Subroutine LCD_Line1:
        Push    ACC
        Mov     A,#80h
        Lcall   LCD_Command
        Pop     ACC
EndSub
Subroutine LCD_Line2:
        Push    ACC
        Mov     A,#0C0h
        Lcall   LCD_Command
        Pop     ACC
EndSub
;-----
Subroutine LCD_String:
        Push    ACC
        Push    DPL
        Push    DPH
getcar1:
        Clr     A           ; mengambil data dari eprom
        Movc    A,@A+DPTR
        Cjne    A,#0,tammpil1    ; tes apakah data habis?
        Ljmp    mettul
tammpil1:               ; keluarkan data ke lcd

        Call    LCD_Data
        Inc     DPTR        ; naikkan dptr
        Ljmp    getcar1
mettul:
        Pop     DPH
        Pop     DPL
        Pop     ACC
EndSub
ppi_porta       Equu    0e000h
ppi_portb       Equ     0e001h
ppi_portc       Equ     0e002h
ppi_portcw      Equ     0e003h

Subroutine PPI_Get_Port_A:
        Push    DPH
        Push    DPL
        Mov     DPTR,#ppi_porta
        Movx    A,@DPTR
        Pop     DPL
        Pop     DPH
EndSub
Subroutine PPI_Get_Port_B:
        Push    DPH
        Push    DPL
        Mov     DPTR,#ppi_portb
        Movx    A,@DPTR
        Pop     DPL
```

```
        Pop     DPH
EndSub
Subroutine PPI_Get_Port_C:
        Push    DPH
        Push    DPL
        Mov     DPTR,#ppi_portc
        Movx    A,@DPTR
        Pop     DPL
        Pop     DPH
EndSub
Subroutine PPI_Initialization:
        Push    DPH
        Push    DPL
        Mov     DPTR,#ppi_portcw
        Movx    @DPTR,A         ; kirim ke port control ppi 8255
        Pop     DPL
        Pop     DPH
EndSub
Subroutine PPI_Send_Port_A:
        Push    DPH
        Push    DPL
        Mov     DPTR,#ppi_porta
        Movx    @DPTR,A
        Pop     DPL
        Pop     DPH
EndSub
Subroutine PPI_Send_Port_B:
        Push    DPH
        Push    DPL
        Mov     DPTR,#ppi_portb
        Movx    @DPTR,A
        Pop     DPL
        Pop     DPH
EndSub
Subroutine PPI_Send_Port_C:
        Push    DPH
        Push    DPL
        Mov     DPTR,#ppi_portc
        Movx    @DPTR,A
        Pop     DPL
        Pop     DPH
EndSub
;================== DELAY ===============================
Subroutine Delay_Var_1ms:
        Call    Delay_Fix_1ms
        Djnz    R0,Delay_Var_1ms
EndSub
Subroutine Delay_Var_10ms:
        Call    Delay_Fix_10ms
        Djnz    R0,Delay_Var_10ms
EndSub
Subroutine Delay_Var_100ms:
        Call    Delay_Fix_100ms
        Djnz    R0,Delay_Var_100ms
EndSub
Subroutine Delay_Var_1s:
```

```
        Call    Delay_Fix_1s
        Djnz    R0,Delay_Var_1s
EndSub
Subroutine Delay_Var_10s:
        Call    Delay_Fix_10s
        Djnz    R0,Delay_Var_10s
EndSub
Subroutine Delay_Var_10us:
        Call    Delay_Fix_10us
        Djnz    R0,Delay_Var_10us
EndSub
Subroutine Delay_Fix_10us:
        Push    1
        Mov     1,#20
        Djnz    1,$
        Pop     1
EndSub
Subroutine Delay_Fix_10s:
        Push    1
        Mov     1,#100
delay_fix_10s_1:
        Call    Delay_Fix_100ms
        Djnz    1,delay_fix_10s_1
        Pop     1
EndSub
Subroutine Delay_Fix_1s:
        Push    1
        Mov     1,#100
delay_fix_1000ms_1:
        Call    Delay_Fix_10ms
        Djnz    1,delay_fix_1000ms_1
        Pop     1
EndSub
Subroutine Delay_Fix_100ms:
        Push    1
        Mov     1,#10
delay_fix_100ms_1:
        Call    Delay_Fix_10ms
        Djnz    1,delay_fix_100ms_1
        Pop     1
EndSub
Subroutine Delay_Fix_10ms:
        Mov     TMOD,#00000001b   ; Timer 1 bekerja pada mode 1
        Mov     TL0,#3Dh    ; siapkan waktu tunda 50 mili-detik
        Mov     TH0,#0B0h
        Clr     TF0               ; me-nol-kan bit limpahan
        Setb    TR0               ; timer mulai bekerja
        Jnb     TF0,$             ; tunggu di sini sampai melimpah
        Clr     TR0               ; timer berhenti kerja
        Ret
EndSub
Subroutine Delay_Fix_1ms:
        Mov     TMOD,#00000001b   ; Timer 1 bekerja pada mode 1
        Mov     TL0,#0EDh   ; siapkan waktu tunda 50 mili-detik
        Clr     TF0               ; me-nol-kan bit limpahan
        Setb    TR0               ; timer mulai bekerja
```

```
        Jnb     TF0,$               ; tunggu di sini sampai melimpah
        Clr     TR0                 ; timer berhenti kerja
        Ret
EndSub

Subroutine Get_DPTR_Suhu:
        Push    B
        Mul     AB                  ; kalikan a dengan b
        Add     A,DPL               ; jumlahkan a dengan dpl
        Mov     DPL,A               ; simpan ke dpl
        Mov     A,B                 ; ambil b
        Addc    A,DPH
        Mov     DPH,A
        Pop     B
        Ret
EndSub

db_Suhu0:       Db      '00,0',0DFh,'C',0
db_Suhu1:       Db      '0,40',0DFh,'C',0
db_Suhu2:       Db      '0,80',0DFh,'C',0
db_Suhu3:       Db      '1,20',0DFh,'C',0
db_Suhu4:       Db      '1,60',0DFh,'C',0
db_Suhu5:       Db      '2,00',0DFh,'C',0
db_Suhu6:       Db      '2,40',0DFh,'C',0
db_Suhu7:       Db      '2,70',0DFh,'C',0
db_Suhu8:       Db      '3,10',0DFh,'C',0
db_Suhu9:       Db      '3,50',0DFh,'C',0
db_Suhu10:      Db      '3,90',0DFh,'C',0
db_Suhu11:      Db      '4,30',0DFh,'C',0
db_Suhu12:      Db      '4,70',0DFh,'C',0
db_Suhu13:      Db      '5,10',0DFh,'C',0
db_Suhu14:      Db      '5,50',0DFh,'C',0
db_Suhu15:      Db      '5,90',0DFh,'C',0
db_Suhu16:      Db      '6,30',0DFh,'C',0
db_Suhu17:      Db      '6,70',0DFh,'C',0
db_Suhu18:      Db      '7,10',0DFh,'C',0
db_Suhu19:      Db      '7,50',0DFh,'C',0
db_Suhu20:      Db      '7,80',0DFh,'C',0
db_Suhu21:      Db      '8,20',0DFh,'C',0
db_Suhu22:      Db      '8,60',0DFh,'C',0
db_Suhu23:      Db      '9,00',0DFh,'C',0
db_Suhu24:      Db      '9,40',0DFh,'C',0
db_Suhu25:      Db      '9,80',0DFh,'C',0
db_Suhu26:      Db      '10,2',0DFh,'C',0
db_Suhu27:      Db      '10,6',0DFh,'C',0
db_Suhu28:      Db      '11,0',0DFh,'C',0
db_Suhu29:      Db      '11,4',0DFh,'C',0
db_Suhu30:      Db      '11,8',0DFh,'C',0
db_Suhu31:      Db      '12,2',0DFh,'C',0
db_Suhu32:      Db      '12,5',0DFh,'C',0
db_Suhu33:      Db      '12,9',0DFh,'C',0
db_Suhu34:      Db      '13,3',0DFh,'C',0
db_Suhu35:      Db      '13,7',0DFh,'C',0
db_Suhu36:      Db      '14,1',0DFh,'C',0
db_Suhu37:      Db      '14,5',0DFh,'C',0
db_Suhu38:      Db      '14,9',0DFh,'C',0
```

```
db_Suhu39:      Db      '15,3',0DFh,'C',0
db_Suhu40:      Db      '15,7',0DFh,'C',0
db_Suhu41:      Db      '16,1',0DFh,'C',0
db_Suhu42:      Db      '16,5',0DFh,'C',0
db_Suhu43:      Db      '16,9',0DFh,'C',0
db_Suhu44:      Db      '17,3',0DFh,'C',0
db_Suhu45:      Db      '17,6',0DFh,'C',0
db_Suhu46:      Db      '18,0',0DFh,'C',0
db_Suhu47:      Db      '18,4',0DFh,'C',0
db_Suhu48:      Db      '18,8',0DFh,'C',0
db_Suhu49:      Db      '19,2',0DFh,'C',0
db_Suhu50:      Db      '19,6',0DFh,'C',0
db_Suhu51:      Db      '20,0',0DFh,'C',0
db_Suhu52:      Db      '20,4',0DFh,'C',0
db_Suhu53:      Db      '20,8',0DFh,'C',0
db_Suhu54:      Db      '21,2',0DFh,'C',0
db_Suhu55:      Db      '21,6',0DFh,'C',0
db_Suhu56:      Db      '22,0',0DFh,'C',0
db_Suhu57:      Db      '22,4',0DFh,'C',0
db_Suhu58:      Db      '22,7',0DFh,'C',0
db_Suhu59:      Db      '23,1',0DFh,'C',0
db_Suhu60:      Db      '23,5',0DFh,'C',0
db_Suhu61:      Db      '23,9',0DFh,'C',0
db_Suhu62:      Db      '24,3',0DFh,'C',0
db_Suhu63:      Db      '24,7',0DFh,'C',0
db_Suhu64:      Db      '25,1',0DFh,'C',0
db_Suhu65:      Db      '25,5',0DFh,'C',0
db_Suhu66:      Db      '25,9',0DFh,'C',0
db_Suhu67:      Db      '26,3',0DFh,'C',0
db_Suhu68:      Db      '26,7',0DFh,'C',0
db_Suhu69:      Db      '27,1',0DFh,'C',0
db_Suhu70:      Db      '27,5',0DFh,'C',0
db_Suhu71:      Db      '27,8',0DFh,'C',0
db_Suhu72:      Db      '28,2',0DFh,'C',0
db_Suhu73:      Db      '28,6',0DFh,'C',0
db_Suhu74:      Db      '29,0',0DFh,'C',0
db_Suhu75:      Db      '29,4',0DFh,'C',0
db_Suhu76:      Db      '29,8',0DFh,'C',0
db_Suhu77:      Db      '30,2',0DFh,'C',0
db_Suhu78:      Db      '30,6',0DFh,'C',0
db_Suhu79:      Db      '31,0',0DFh,'C',0
db_Suhu80:      Db      '31,4',0DFh,'C',0
db_Suhu81:      Db      '31,8',0DFh,'C',0
db_Suhu82:      Db      '32,2',0DFh,'C',0
db_Suhu83:      Db      '32,5',0DFh,'C',0
db_Suhu84:      Db      '32,9',0DFh,'C',0
db_Suhu85:      Db      '33,3',0DFh,'C',0
db_Suhu86:      Db      '33,7',0DFh,'C',0
db_Suhu87:      Db      '34,1',0DFh,'C',0
db_Suhu88:      Db      '34,5',0DFh,'C',0
db_Suhu89:      Db      '34,9',0DFh,'C',0
db_Suhu90:      Db      '35,3',0DFh,'C',0
db_Suhu91:      Db      '35,7',0DFh,'C',0
db_Suhu92:      Db      '36,1',0DFh,'C',0
db_Suhu93:      Db      '36,5',0DFh,'C',0
db_Suhu94:      Db      '36,9',0DFh,'C',0
```

```
db_Suhu95:     Db     '37,3',0DFh,'C',0
db_Suhu96:     Db     '37,6',0DFh,'C',0
db_Suhu97:     Db     '38,0',0DFh,'C',0
db_Suhu98:     Db     '38,4',0DFh,'C',0
db_Suhu99:     Db     '38,8',0DFh,'C',0
db_Suhu100:    Db     '39,2',0DFh,'C',0
db_Suhu101:    Db     '39,6',0DFh,'C',0
db_Suhu102:    Db     '40,0',0DFh,'C',0
db_Suhu103:    Db     '40,4',0DFh,'C',0
db_Suhu104:    Db     '40,8',0DFh,'C',0
db_Suhu105:    Db     '41,2',0DFh,'C',0
db_Suhu106:    Db     '41,6',0DFh,'C',0
db_Suhu107:    Db     '42,0',0DFh,'C',0
db_Suhu108:    Db     '42,4',0DFh,'C',0
db_Suhu109:    Db     '42,7',0DFh,'C',0
db_Suhu110:    Db     '43,1',0DFh,'C',0
db_Suhu111:    Db     '43,5',0DFh,'C',0
db_Suhu112:    Db     '43,9',0DFh,'C',0
db_Suhu113:    Db     '44,3',0DFh,'C',0
db_Suhu114:    Db     '44,7',0DFh,'C',0
db_Suhu115:    Db     '45,1',0DFh,'C',0
db_Suhu116:    Db     '45,5',0DFh,'C',0
db_Suhu117:    Db     '45,9',0DFh,'C',0
db_Suhu118:    Db     '46,3',0DFh,'C',0
db_Suhu119:    Db     '46,7',0DFh,'C',0
db_Suhu120:    Db     '47,1',0DFh,'C',0
db_Suhu121:    Db     '47,5',0DFh,'C',0
db_Suhu122:    Db     '47,8',0DFh,'C',0
db_Suhu123:    Db     '48,2',0DFh,'C',0
db_Suhu124:    Db     '48,6',0DFh,'C',0
db_Suhu125:    Db     '49,0',0DFh,'C',0
db_Suhu126:    Db     '49,4',0DFh,'C',0
db_Suhu127:    Db     '49,8',0DFh,'C',0
db_Suhu128:    Db     '50,2',0DFh,'C',0
db_Suhu129:    Db     '50,6',0DFh,'C',0
db_Suhu130:    Db     '51,0',0DFh,'C',0
db_Suhu131:    Db     '51,4',0DFh,'C',0
db_Suhu132:    Db     '51,8',0DFh,'C',0
db_Suhu133:    Db     '52,2',0DFh,'C',0
db_Suhu134:    Db     '52,5',0DFh,'C',0
db_Suhu135:    Db     '52,9',0DFh,'C',0
db_Suhu136:    Db     '53,3',0DFh,'C',0
db_Suhu137:    Db     '53,7',0DFh,'C',0
db_Suhu138:    Db     '54,1',0DFh,'C',0
db_Suhu139:    Db     '54,5',0DFh,'C',0
db_Suhu140:    Db     '54,9',0DFh,'C',0
db_Suhu141:    Db     '55,3',0DFh,'C',0
db_Suhu142:    Db     '55,7',0DFh,'C',0
db_Suhu143:    Db     '56,1',0DFh,'C',0
db_Suhu144:    Db     '56,5',0DFh,'C',0
db_Suhu145:    Db     '56,9',0DFh,'C',0
db_Suhu146:    Db     '57,3',0DFh,'C',0
db_Suhu147:    Db     '57,6',0DFh,'C',0
db_Suhu148:    Db     '58,0',0DFh,'C',0
db_Suhu149:    Db     '58,4',0DFh,'C',0
db_Suhu150:    Db     '58,8',0DFh,'C',0
```

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db_Suhu151:    Db    '59,2',0DFh,'C',0
db_Suhu152:    Db    '59,6',0DFh,'C',0
db_Suhu153:    Db    '60,0',0DFh,'C',0
db_Suhu154:    Db    '60,4',0DFh,'C',0
db_Suhu155:    Db    '60,8',0DFh,'C',0
db_Suhu156:    Db    '61,2',0DFh,'C',0
db_Suhu157:    Db    '61,6',0DFh,'C',0
db_Suhu158:    Db    '62,0',0DFh,'C',0
db_Suhu159:    Db    '62,4',0DFh,'C',0
db_Suhu160:    Db    '62,7',0DFh,'C',0
db_Suhu161:    Db    '63,1',0DFh,'C',0
db_Suhu162:    Db    '63,5',0DFh,'C',0
db_Suhu163:    Db    '63,9',0DFh,'C',0
db_Suhu164:    Db    '64,3',0DFh,'C',0
db_Suhu165:    Db    '64,7',0DFh,'C',0
db_Suhu166:    Db    '65,1',0DFh,'C',0
db_Suhu167:    Db    '65,5',0DFh,'C',0
db_Suhu168:    Db    '65,9',0DFh,'C',0
db_Suhu169:    Db    '66,3',0DFh,'C',0
db_Suhu170:    Db    '66,7',0DFh,'C',0
db_Suhu171:    Db    '67,1',0DFh,'C',0
db_Suhu172:    Db    '67,5',0DFh,'C',0
db_Suhu173:    Db    '67,8',0DFh,'C',0
db_Suhu174:    Db    '68,2',0DFh,'C',0
db_Suhu175:    Db    '68,6',0DFh,'C',0
db_Suhu176:    Db    '69,0',0DFh,'C',0
db_Suhu177:    Db    '69,4',0DFh,'C',0
db_Suhu178:    Db    '69,8',0DFh,'C',0
db_Suhu179:    Db    '70,2',0DFh,'C',0
db_Suhu180:    Db    '70,6',0DFh,'C',0
db_Suhu181:    Db    '71,0',0DFh,'C',0
db_Suhu182:    Db    '71,4',0DFh,'C',0
db_Suhu183:    Db    '71,8',0DFh,'C',0
db_Suhu184:    Db    '72,2',0DFh,'C',0
db_Suhu185:    Db    '72,5',0DFh,'C',0
db_Suhu186:    Db    '72,9',0DFh,'C',0
db_Suhu187:    Db    '73,3',0DFh,'C',0
db_Suhu188:    Db    '73,7',0DFh,'C',0
db_Suhu189:    Db    '74,1',0DFh,'C',0
db_Suhu190:    Db    '74,5',0DFh,'C',0
db_Suhu191:    Db    '74,9',0DFh,'C',0
db_Suhu192:    Db    '75,3',0DFh,'C',0
db_Suhu193:    Db    '75,7',0DFh,'C',0
db_Suhu194:    Db    '76,1',0DFh,'C',0
db_Suhu195:    Db    '76,5',0DFh,'C',0
db_Suhu196:    Db    '76,9',0DFh,'C',0
db_Suhu197:    Db    '77,3',0DFh,'C',0
db_Suhu198:    Db    '77,6',0DFh,'C',0
db_Suhu199:    Db    '78,0',0DFh,'C',0
db_Suhu200:    Db    '78,4',0DFh,'C',0
db_Suhu201:    Db    '78,8',0DFh,'C',0
db_Suhu202:    Db    '79,2',0DFh,'C',0
db_Suhu203:    Db    '79,6',0DFh,'C',0
db_Suhu204:    Db    '80,0',0DFh,'C',0
db_Suhu205:    Db    '80,4',0DFh,'C',0
db_Suhu206:    Db    '80,8',0DFh,'C',0
```

```
db_Suhu207:     Db      '81,2',0DFh,'C',0
db_Suhu208:     Db      '81,6',0DFh,'C',0
db_Suhu209:     Db      '82,0',0DFh,'C',0
db_Suhu210:     Db      '82,4',0DFh,'C',0
db_Suhu211:     Db      '82,7',0DFh,'C',0
db_Suhu212:     Db      '83,1',0DFh,'C',0
db_Suhu213:     Db      '83,5',0DFh,'C',0
db_Suhu214:     Db      '83,9',0DFh,'C',0
db_Suhu215:     Db      '84,3',0DFh,'C',0
db_Suhu216:     Db      '84,7',0DFh,'C',0
db_Suhu217:     Db      '85,1',0DFh,'C',0
db_Suhu218:     Db      '85,5',0DFh,'C',0
db_Suhu219:     Db      '85,9',0DFh,'C',0
db_Suhu220:     Db      '86,3',0DFh,'C',0
db_Suhu221:     Db      '86,7',0DFh,'C',0
db_Suhu222:     Db      '87,1',0DFh,'C',0
db_Suhu223:     Db      '87,5',0DFh,'C',0
db_Suhu224:     Db      '87,8',0DFh,'C',0
db_Suhu225:     Db      '88,2',0DFh,'C',0
db_Suhu226:     Db      '88,6',0DFh,'C',0
db_Suhu227:     Db      '89,0',0DFh,'C',0
db_Suhu228:     Db      '89,4',0DFh,'C',0
db_Suhu229:     Db      '89,8',0DFh,'C',0
db_Suhu230:     Db      '90,2',0DFh,'C',0
db_Suhu231:     Db      '90,6',0DFh,'C',0
db_Suhu232:     Db      '91,0',0DFh,'C',0
db_Suhu233:     Db      '91,4',0DFh,'C',0
db_Suhu234:     Db      '91,8',0DFh,'C',0
db_Suhu235:     Db      '92,2',0DFh,'C',0
db_Suhu236:     Db      '92,5',0DFh,'C',0
db_Suhu237:     Db      '92,9',0DFh,'C',0
db_Suhu238:     Db      '93,3',0DFh,'C',0
db_Suhu239:     Db      '93,7',0DFh,'C',0
db_Suhu240:     Db      '94,1',0DFh,'C',0
db_Suhu241:     Db      '94,5',0DFh,'C',0
db_Suhu242:     Db      '94,9',0DFh,'C',0
db_Suhu243:     Db      '95,3',0DFh,'C',0
db_Suhu244:     Db      '95,7',0DFh,'C',0
db_Suhu245:     Db      '96,1',0DFh,'C',0
db_Suhu246:     Db      '96,5',0DFh,'C',0
db_Suhu247:     Db      '96,9',0DFh,'C',0
db_Suhu248:     Db      '97,3',0DFh,'C',0
db_Suhu249:     Db      '97,6',0DFh,'C',0
db_Suhu250:     Db      '98,0',0DFh,'C',0
db_Suhu251:     Db      '98,4',0DFh,'C',0
db_Suhu252:     Db      '98,8',0DFh,'C',0
db_Suhu253:     Db      '99,2',0DFh,'C',0
db_Suhu254:     Db      '99,6',0DFh,'C',0
db_Suhu255:     Db      '100',0DFh,'C ',0

txt_Suhu1:        Db      'Suhu:',0
txt_Tinggi1:      Db      'Tinggi:',0

txt_level0:       Db      '0%  ',0
txt_level1:       Db      '14% ',0
txt_level2:       Db      '28% ',0
```

```
txt_level3:     Db      '42% ',0
txt_level4:     Db      '56% ',0
txt_level5:     Db      '70% ',0
txt_level6:     Db      '84% ',0
txt_level7:     Db      '98% ',0
txt_level8:     Db      '100%',0
```

DATA SHEET

atures

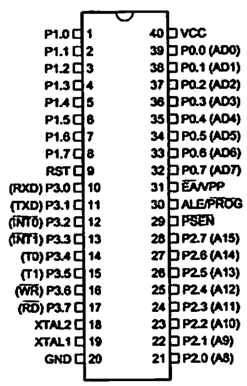
- ompatible with MCS-51™ Products
- ‹ Bytes of In-System Reprogrammable Flash Memory
  - – Endurance: 1,000 Write/Erase Cycles
- ully Static Operation: 0 Hz to 24 MHz
- hree-level Program Memory Lock
- 28 x 8-bit Internal RAM
- 2 Programmable I/O Lines
- wo 16-bit Timer/Counters
- ix Interrupt Sources
- rogrammable Serial Channel
- ow-power Idle and Power-down Modes

escription

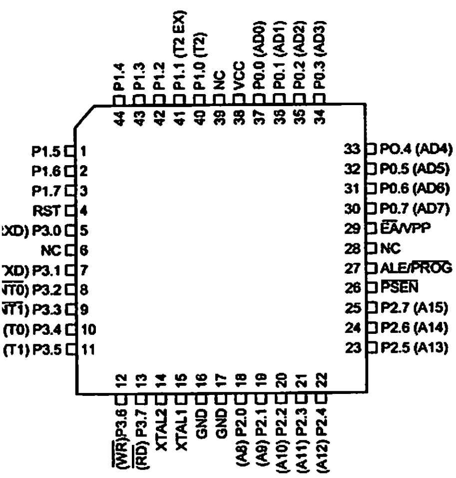
e AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K es of Flash programmable and erasable read only memory (PEROM). The device nanufactured using Atmel's high-density nonvolatile memory technology and is npatible with the industry-standard MCS-51 instruction set and pinout. The on-chip sh allows the program memory to be reprogrammed in-system or by a conven-ial nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides ighly-flexible and cost-effective solution to many embedded control applications.

n Configurations

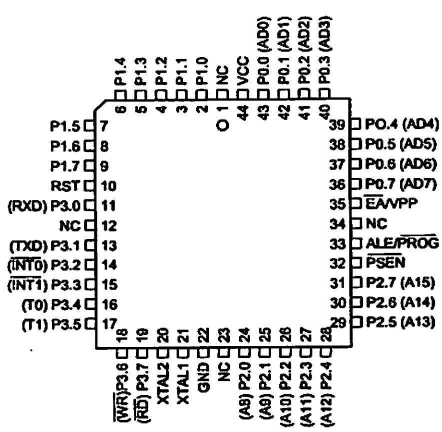
PDIP



PQFP/TQFP



PLCC



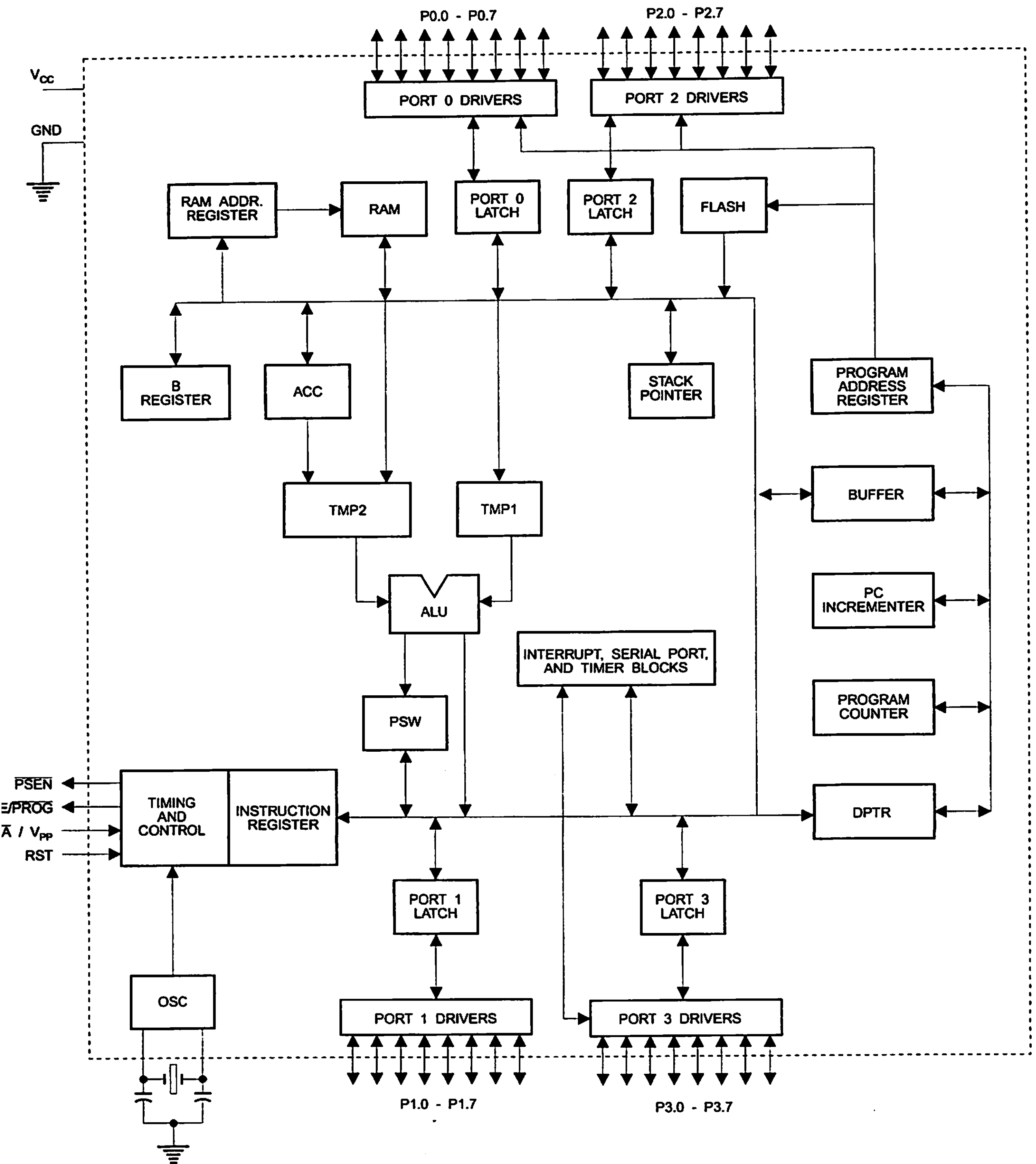
8-bit Microcontroller with 4K Bytes Flash

AT89C51

Not Recommended for New Designs. Use AT89S51.

Rev. 0265G–02/00

lock Diagram



ɪ AT89C51 provides the following standard features: 4K ɜs of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit ɜr/counters, a five vector two-level interrupt architecture, ɪll duplex serial port, on-chip oscillator and clock cir- ɪy. In addition, the AT89C51 is designed with static logic operation down to zero frequency and supports two tware selectable power saving modes. The Idle Mode ps the CPU while allowing the RAM, timer/counters, ial port and interrupt system to continue functioning. The wer-down Mode saves the RAM contents but freezes oscillator disabling all other chip functions until the next dware reset.

n Description

C

ɔply voltage.

ID

ɔund.

rt 0

rt 0 is an 8-bit open-drain bi-directional I/O port. As an ɪput port, each pin can sink eight TTL inputs. When 1s ɪ written to port 0 pins, the pins can be used as high- ɔedance inputs.

rt 0 may also be configured to be the multiplexed low- ler address/data bus during accesses to external pro- ɪm and data memory. In this mode P0 has internal lups.

rt 0 also receives the code bytes during Flash program- ng, and outputs the code bytes during program ification. External pullups are required during program ification.

rt 1

rt 1 is an 8-bit bi-directional I/O port with internal pullups. e Port 1 output buffers can sink/source four TTL inputs. ɪen 1s are written to Port 1 pins they are pulled high by ɪ internal pullups and can be used as inputs. As inputs, rt 1 pins that are externally being pulled low will source rrent (I_{IL}) because of the internal pullups.

rt 1 also receives the low-order address bytes during ɪsh programming and verification.

rt 2

rt 2 is an 8-bit bi-directional I/O port with internal pullups. e Port 2 output buffers can sink/source four TTL inputs. ɪen 1s are written to Port 2 pins they are pulled high by ɪ internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{\text{PROG}}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE se is skipped during each access to external Data mory.

esired, ALE operation can be disabled by setting bit 0 of R location 8EH. With the bit set, ALE is active only dur- a MOVX or MOVC instruction. Otherwise, the pin is akly pulled high. Setting the ALE-disable bit has no ect if the microcontroller is in external execution mode.

EN

ogram Store Enable is the read strobe to external pro- m memory.

ien the AT89C51 is executing code from external pro- im memory, PSEN is activated twice each machine :le, except that two PSEN activations are skipped during ch access to external data memory.

/VPP

ernal Access Enable. EA must be strapped to GND in ler to enable the device to fetch code from external pro- im memory locations starting at 0000H up to FFFFH. te, however, that if lock bit 1 is programmed, EA will be ernally latched on reset.

should be strapped to V_{CC} for internal program ecutions.

is pin also receives the 12-volt programming enable volt- e (V_{PP}) during Flash programming, for parts that require -volt V_{PP}.

AL1

out to the inverting oscillator amplifier and input to the ernal clock operating circuit.

AL2

tput from the inverting oscillator amplifier.

scillator Characteristics

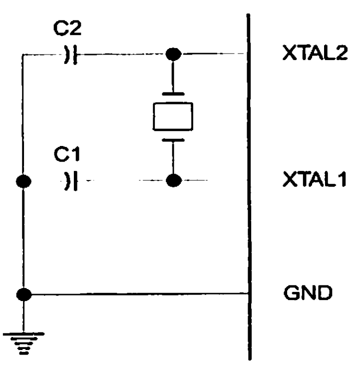
AL1 and XTAL2 are the input and output, respectively, an inverting amplifier which can be configured for use as on-chip oscillator, as shown in Figure 1. Either a quartz ystal or ceramic resonator may be used. To drive the vice from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

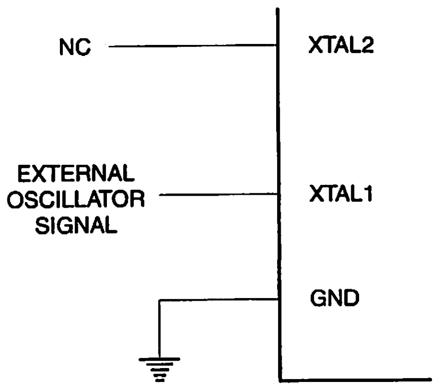


Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

tatus of External Pins During Idle and Power-down Modes

lode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
lle	Internal	1	1	Data	Data	Data	Data
ile	External	1	1	Float	Data	Address	Data
ower-down	Internal	0	0	Data	Data	Data	Data
ower-down	External	0	0	Float	Data	Data	Data

ure 2. External Clock Drive Configuration



›wer-down Mode

:he power-down mode, the oscillator is stopped, and the truction that invokes power-down is the last instruction ›cuted. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

›ck Bit Protection Modes

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled
3	P	P	U	Same as mode 2, also verify is disabled
4	P	P	P	Same as mode 3, also external execution is disabled

›gramming the Flash

AT89C51 is normally shipped with the on-chip Flash nory array in the erased state (that is, contents = FFH) ready to be programmed. The programming interface epts either a high-voltage (12-volt) or a low-voltage ;) program enable signal. The low-voltage program- g mode provides a convenient way to program the 9C51 inside the user's system, while the high-voltage jramming mode is compatible with conventional third- y Flash or EPROM programmers.

AT89C51 is shipped with either the high-voltage or -voltage programming mode enabled. The respective side marking and device signature codes are listed in following table.

	V_{PP} = 12V	V_{PP} = 5V
p-side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
jnature	(030H) = 1EH (031H) = 51H (032H) =F FH	(030H) = 1EH (031H) = 51H (032H) = 05H

AT89C51 code memory array is programmed byte-by- e in either programming mode. *To program any non- nk byte in the on-chip Flash Memory, the entire memory st be erased using the Chip Erase Mode.*

›gramming Algorithm: Before programming the 39C51, the address, data and control signals should be up according to the Flash programming mode table and ure 3 and Figure 4. To program the AT89C51, take the owing steps.

Input the desired memory location on the address lines.

Input the appropriate data byte on the data lines.

Activate the correct combination of control signals.

Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.

Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms.

Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{\text{Data}}$ Polling: The AT89C51 features $\overline{\text{Data}}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

ısh Programming Modes

ıde		RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7
ite Code Data		H	L		H/12V	L	H	H	H
ıad Code Data		H	L	H	H	L	L	H	H
ite Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
ıip Erase		H	L	(1)	H/12V	H	L	L	L
ıad Signature Byte		H	L	H	H	L	L	L	L

ɔ: 1. Chip Erase requires a 10 ms PROG pulse.

ure 3. Programming the Flash

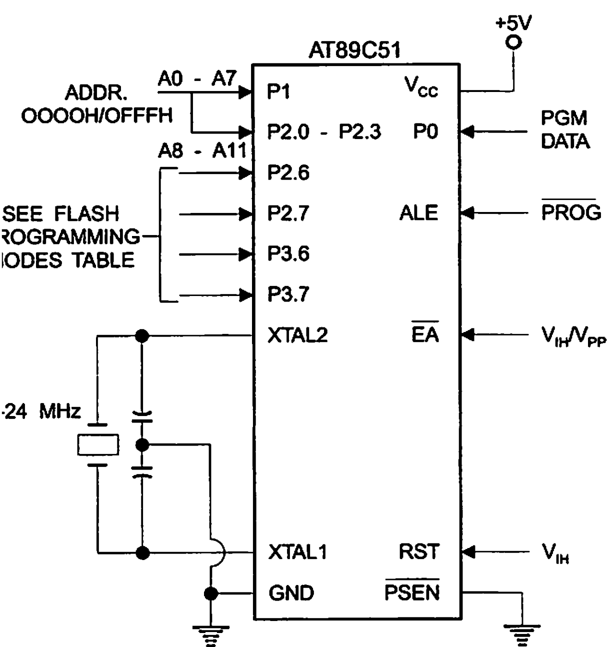
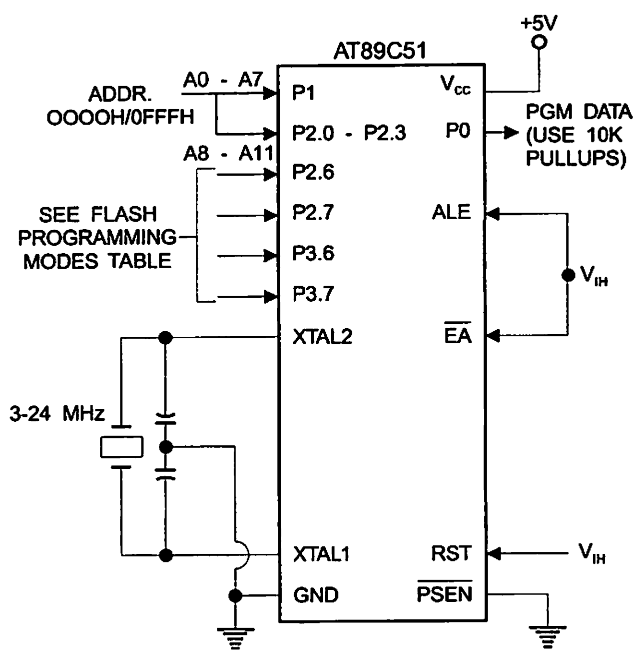
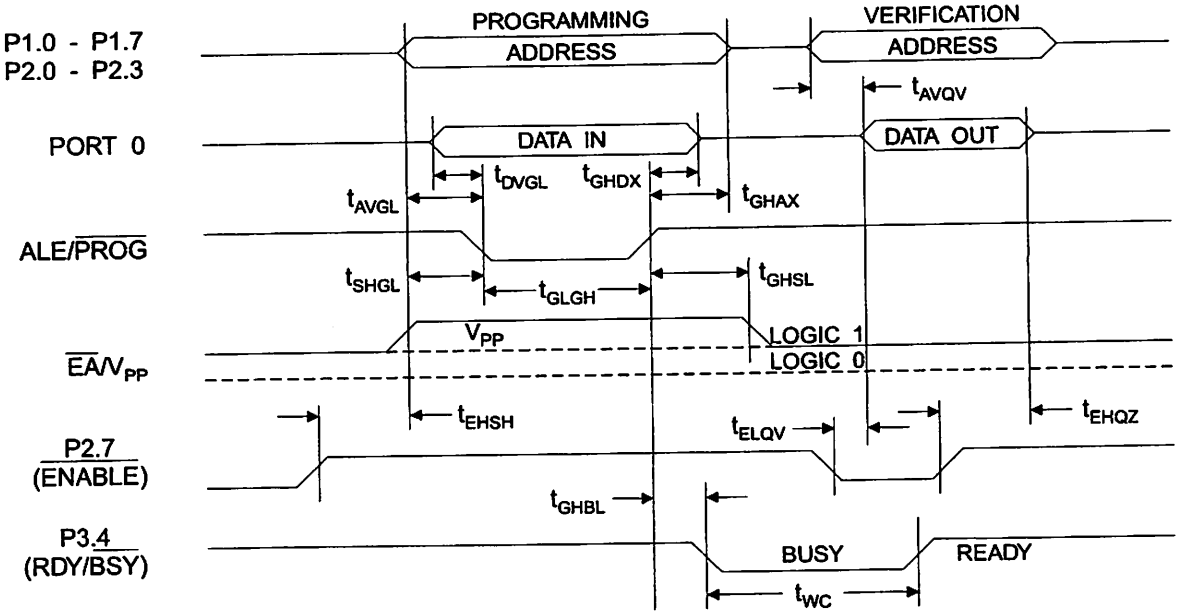


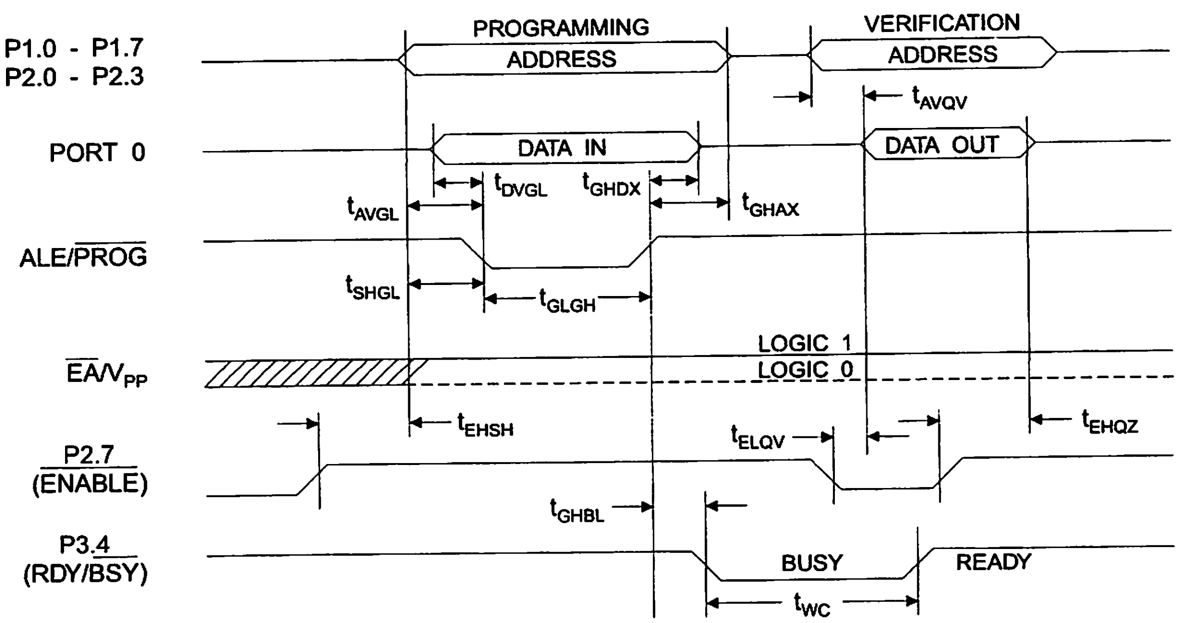
Figure 4. Verifying the Flash



ash Programming and Verification Waveforms - High-voltage Mode (V_{PP} = 12V)



lash Programming and Verification Waveforms - Low-voltage Mode (V_{PP} = 5V)



ash Programming and Verification Characteristics

= 0°C to 70°C, V_{CC} = 5.0 ± 10%

ymbol	Parameter	Min	Max	Units
$_{PP}$(1)	Programming Enable Voltage	11.5	12.5	V
$_P$(1)	Programming Enable Current		1.0	mA
t_{CLCL}	Oscillator Frequency	3	24	MHz
$_{VGL}$	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
$_{HAX}$	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
$_{VGL}$	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
$_{HDX}$	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
$_{HSH}$	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
$_{HGL}$	V_{PP} Setup to $\overline{PROG}$ Low	10		μs
$_{HSL}$(1)	V_{PP} Hold after $\overline{PROG}$	10		μs
$_{LGH}$	$\overline{PROG}$ Width	1	110	μs
$_{VQV}$	Address to Data Valid		$48t_{CLCL}$	
$_{LQV}$	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
$_{HQZ}$	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
$_{HBL}$	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	μs
$_{C}$	Byte Write Cycle Time		2.0	ms

e: 1. Only used in 12-volt programming mode.

solute Maximum Ratings*

perating Temperature	-55°C to +125°C
orage Temperature	-65°C to +150°C
ltage on Any Pin th Respect to Ground	-1.0V to +7.0V
aximum Operating Voltage	6.6V
C Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C Characteristics

= -40°C to 85°C, V_{CC} = 5.0V ±20% (unless otherwise noted)

mbol	Parameter	Condition	Min	Max	Units
L	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
L1	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
H	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
H1	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
OL	Output Low-voltage[(1)] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
OL1	Output Low-voltage[(1)] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
OH	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 μA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 μA	0.75 V_{CC}		V
		I_{OH} = -10 μA	0.9 V_{CC}		V
OH1	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 μA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 μA	0.75 V_{CC}		V
		I_{OH} = -80 μA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	μA
L	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	μA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	μA
RST	Reset Pull-down Resistor		50	300	KΩ
IO	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
C	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power-down Mode[(2)]	V_{CC} = 6V		100	μA
		V_{CC} = 3V		40	μA

tes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

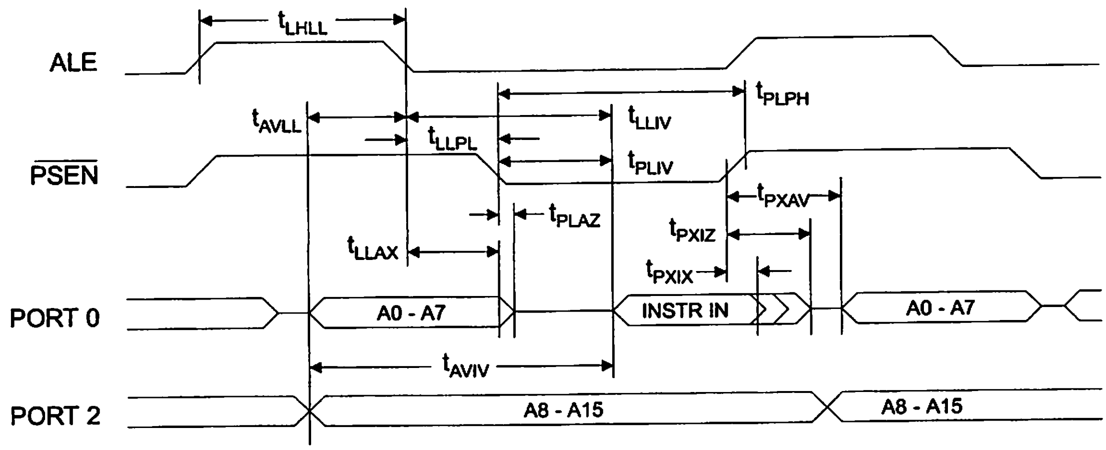
C Characteristics

ler operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other puts = 80 pF.

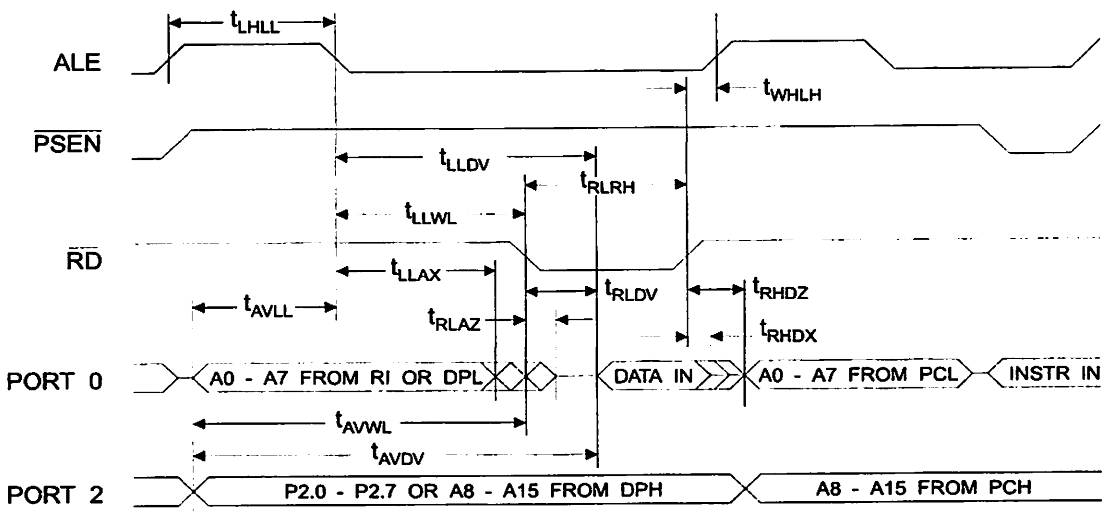
:ternal Program and Data Memory Characteristics

ymbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
t_{CLCL}	Oscillator Frequency			0	24	MHz
HLL	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
VLL	Address Valid to ALE Low	43		t_{CLCL}-13		ns
LAX	Address Hold after ALE Low	48		t_{CLCL}-20		ns
LIV	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
LPL	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
LPH	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
LIV	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
XIX	Input Instruction Hold after $\overline{PSEN}$	0		0		ns
XIZ	Input Instruction Float after $\overline{PSEN}$		59		t_{CLCL}-10	ns
XAV	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
VIV	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
LAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
LRH	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
WLWH	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
LDV	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
HDX	Data Hold after $\overline{RD}$	0		0		ns
HDZ	Data Float after $\overline{RD}$		97		$2t_{CLCL}$-28	ns
LDV	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
VDV	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
LWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
VWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
QVWX	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
QVWH	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
WHQX	Data Hold after $\overline{WR}$	33		t_{CLCL}-20		ns
RLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
WHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

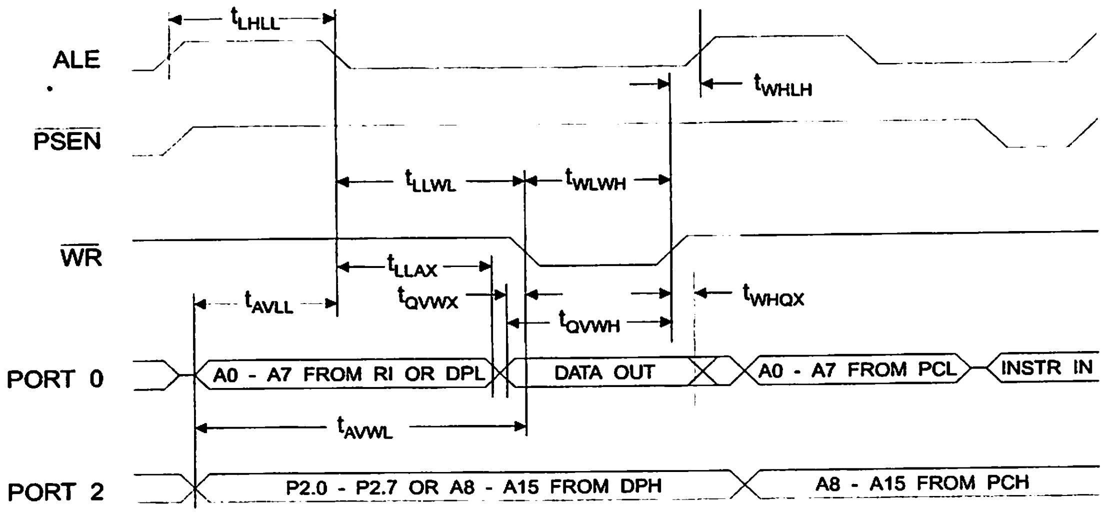
:ternal Program Memory Read Cycle



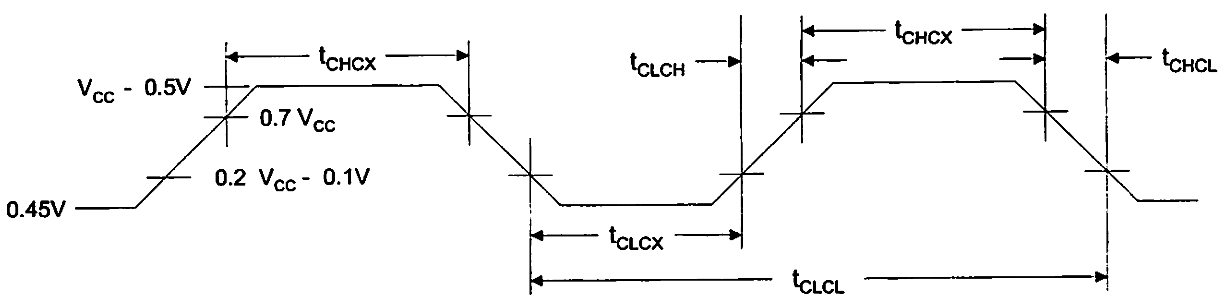
:ternal Data Memory Read Cycle



ternal Data Memory Write Cycle



xternal Clock Drive Waveforms



xternal Clock Drive

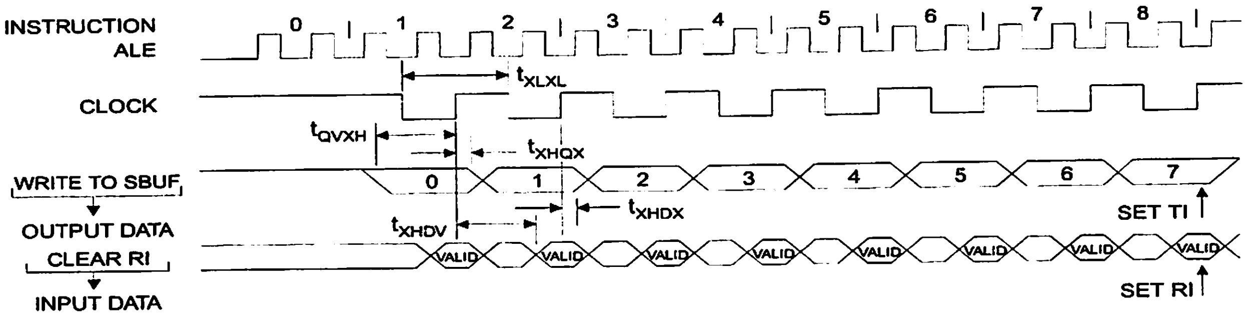
ymbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
$_{LCL}$	Clock Period	41.6		ns
$_{HCX}$	High Time	15		ns
$_{LCX}$	Low Time	15		ns
$_{LCH}$	Rise Time		20	ns
$_{HCL}$	Fall Time		20	ns

rial Port Timing: Shift Register Mode Test Conditions

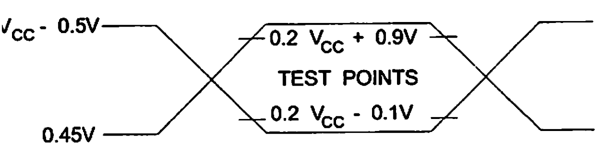
; = 5.0 V ±20%; Load Capacitance = 80 pF)

'mbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
XL	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
/XH	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
IQX	Output Data Hold after Clock Rising Edge	50		$2t_{CLCL}$-117		ns
IDX	Input Data Hold after Clock Rising Edge	0		0		ns
IDV	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

iift Register Mode Timing Waveforms

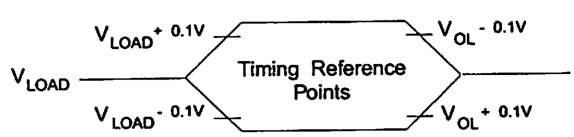


C Testing Input/Output Waveforms(1)



te: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms(1)



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

SN74LS138

1-of-8 Decoder/ Demultiplexer

The LSTTL/MSI SN74LS138 is a high speed 1-of-8 Decoder/ Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138s and one inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Typical Power Dissipation of 32 mW
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

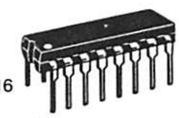
GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA

ON Semiconductor™

http://onsemi.com

LOW POWER SCHOTTKY



16

1

PLASTIC
N SUFFIX
CASE 648

16

1

SOIC
D SUFFIX
CASE 751B

16

1

SOEIAJ
M SUFFIX
CASE 966

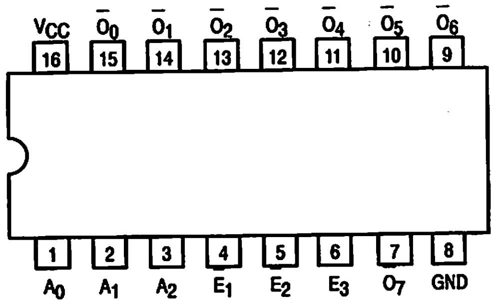
ORDERING INFORMATION

Device	Package	Shipping
SN74LS138N	16 Pin DIP	2000 Units/Box
SN74LS138D	SOIC–16	38 Units/Rail
SN74LS138DR2	SOIC–16	2500/Tape & Reel
SN74LS138M	SOEIAJ–16	See Note 1
SN74LS138MEL	SOEIAJ–16	See Note 1

1. For ordering information on the EIAJ version of the SOIC package, please contact your local ON Semiconductor representative.

SN74LS138

CONNECTION DIAGRAM DIP (TOP VIEW)



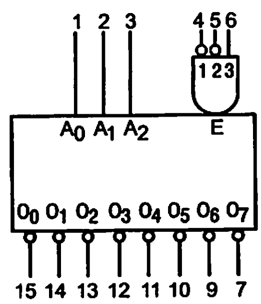
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$A_0 - A_2$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_1, \overline{E}_2$	Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
E_3	Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_7$	Active LOW Outputs	10 U.L.	5 U.L.

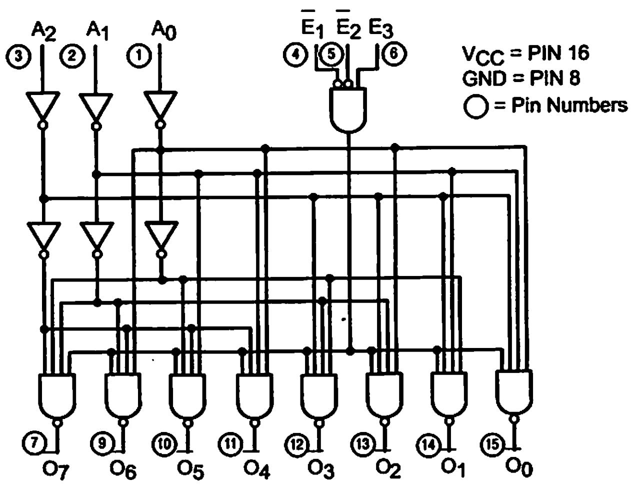
NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW Outputs ($\overline{O}_0$–$\overline{O}_7$). The LS138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LS138s and one inverter. (See Figure a.)

The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

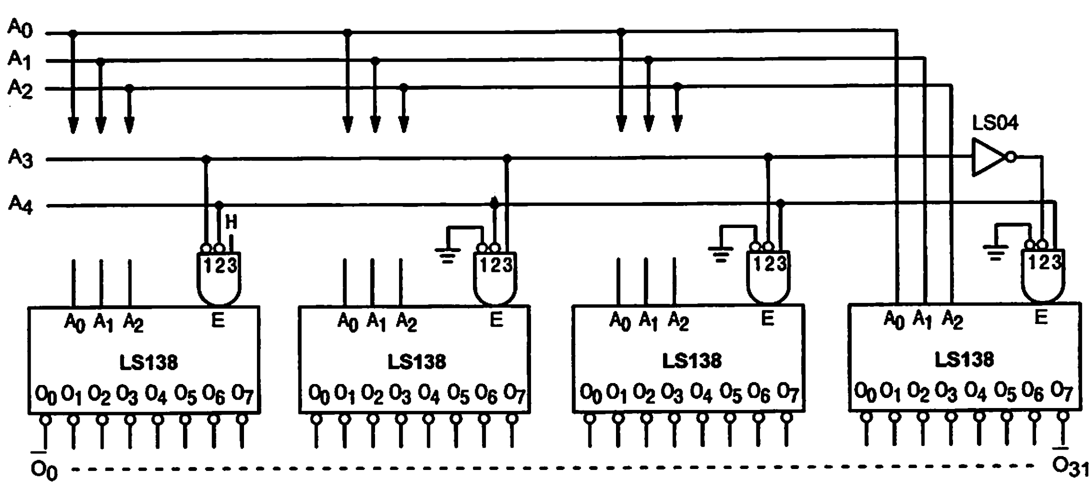


Figure a

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current			–0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 2)	–20		–100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current			10	mA	V_{CC} = MAX	

2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Levels of Delay	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH} t_{PHL}	Propagation Delay Address to Output	2 2		13 27	20 41	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Address to Output	3 3		18 26	27 39	ns	
t_{PLH} t_{PHL}	Propagation Delay E_1 or E_2 Enable to Output	2 2		12 21	18 32	ns	
t_{PLH} t_{PHL}	Propagation Delay E_3 Enable to Output	3 3		17 25	26 38	ns	

AC WAVEFORMS

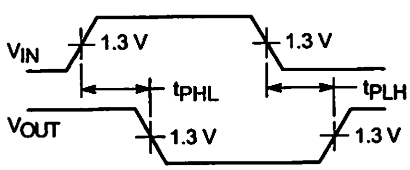


Figure 1.

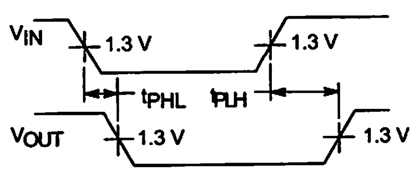


Figure 2.

intel®

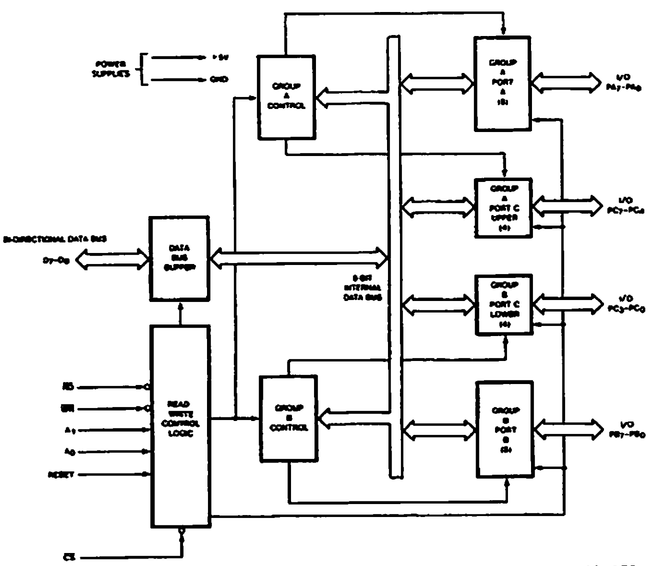
82C55A
CHMOS PROGRAMMABLE PERIPHERAL INTERFACE

- **Compatible with all Intel and Most Other Microprocessors**
- **High Speed, "Zero Wait State" Operation with 8 MHz 8086/88 and 80186/188**
- **24 Programmable I/O Pins**
- **Low Power CHMOS**
- **Completely TTL Compatible**
- **Control Word Read-Back Capability**
- **Direct Bit Set/Reset Capability**
- **2.5 mA DC Drive Capability on all I/O Port Outputs**
- **Available in 40-Pin DIP and 44-Pin PLCC**
- **Available in EXPRESS**
  - **—Standard Temperature Range**
  - **—Extended Temperature Range**

The Intel 82C55A is a high-performance, CHMOS version of the industry standard 8255A general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The 82C55A is pin compatible with the NMOS 8255A and 8255A-5.

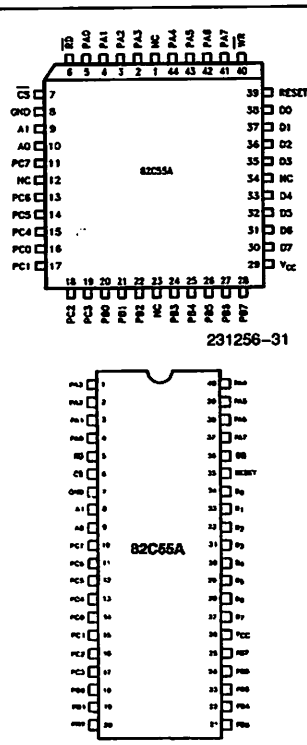
In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

The 82C55A is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The 82C55A is available in 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC) packages.



231256–1

Figure 1. 82C55A Block Diagram



231256–2

Figure 2. 82C55A Pinout

Diagrams are for pin reference only. Package sizes are not to scale.

Table 1. Pin Description

Symbol	Pin Number Dip	Pin Number PLCC	Type	Name and Function
PA_{3-0}	1–4	2–5	I/O	**PORT A, PINS 0–3:** Lower nibble of an 8-bit data output latch/buffer and an 8-bit data input latch.
$\overline{RD}$	5	6	I	**READ CONTROL:** This input is low during CPU read operations.
$\overline{CS}$	6	7	I	**CHIP SELECT:** A low on this input enables the 82C55A to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and WR are ignored otherwise.
GND	7	8		**System Ground**
A_{1-0}	8–9	9–10	I	**ADDRESS:** These input signals, in conjunction $\overline{RD}$ and $\overline{WR}$, control the selection of one of the three ports or the control word registers.

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (Read)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Control Word - Data Bus
					Output Operation (Write)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control
					Disable Function
X	X	X	X	1	Data Bus - 3 - State
X	X	1	1	0	Data Bus - 3 - State

Symbol	Pin Number Dip	Pin Number PLCC	Type	Name and Function
PC_{7-4}	10–13	11,13–15	I/O	**PORT C, PINS 4–7:** Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.
PC_{0-3}	14–17	16–19	I/O	**PORT C, PINS 0–3:** Lower nibble of Port C.
PB_{0-7}	18–25	20–22, 24–28	I/O	**PORT B, PINS 0–7:** An 8-bit data output latch/buffer and an 8-bit data input buffer.
V_{CC}	26	29		**SYSTEM POWER:** + 5V Power Supply.
D_{7-0}	27–34	30–33, 35–38	I/O	**DATA BUS:** Bi-directional, tri-state data bus lines, connected to system data bus.
RESET	35	39	I	**RESET:** A high on this input clears the control register and all ports are set to the input mode.
$\overline{WR}$	36	40	I	**WRITE CONTROL:** This input is low during CPU write operations.
PA_{7-4}	37–40	41–44	I/O	**PORT A, PINS 4–7:** Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input latch.
NC		1, 12, 23, 34		No Connect

82C55A FUNCTIONAL DESCRIPTION

General

The 82C55A is a programmable peripheral interface device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 82C55A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7–C4)
Control Group B - Port B and Port C lower (C3–C0)

The control word register can be both written and read as shown in the address decode table in the pin descriptions. Figure 6 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A. One 8-bit data output latch/buffer and one 8-bit input latch buffer. Both "pull-up" and "pull-down" bus hold devices are present on Port A.

Port B. One 8-bit data input/output latch/buffer. Only "pull-up" bus hold devices are present on Port B.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only "pull-up" bus hold devices are present on Port C.

See Figure 4 for the bus-hold circuit configuration for Port A, B, and C.

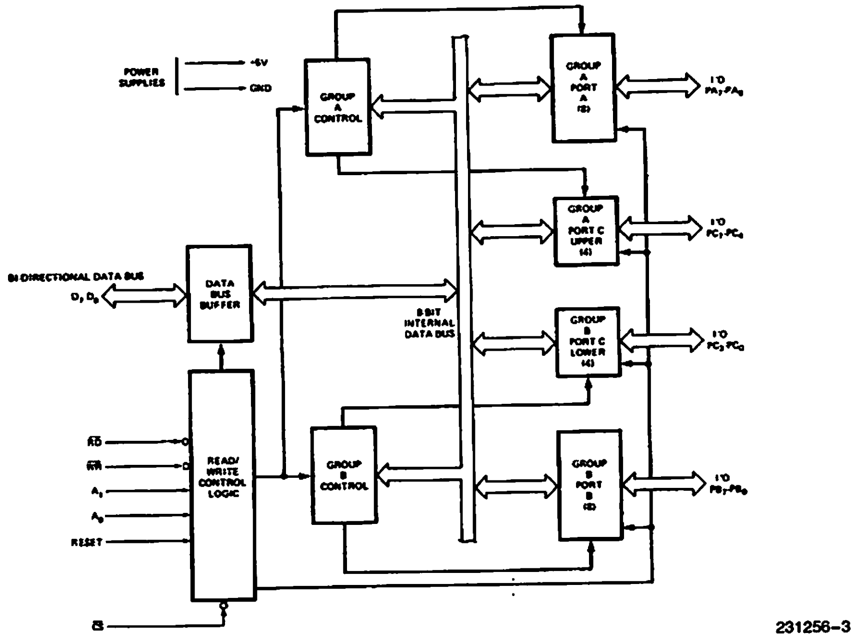
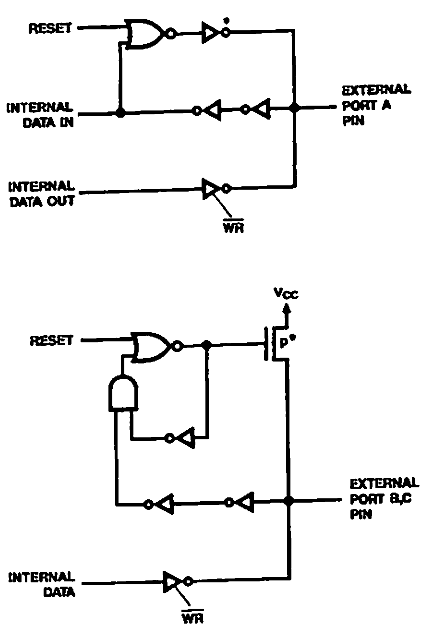


Figure 3. 82C55A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions



*NOTE:
Port pins loaded with more than 20 pF capacitance may not have their logic level guaranteed following a hardware reset.

Figure 4. Port A, B, C, Bus-hold Configuration

82C55A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 — Basic input/output
Mode 1 — Strobed Input/output
Mode 2 — Bi-directional Bus

When the reset input goes "high" all ports will be set to the input mode with all 24 port lines held at a logic "one" level by the internal bus hold devices (see Figure 4 Note). After the reset is removed the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown devices in "all CMOS" designs. During the execution of the system program, any of the other modes may be selected by using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

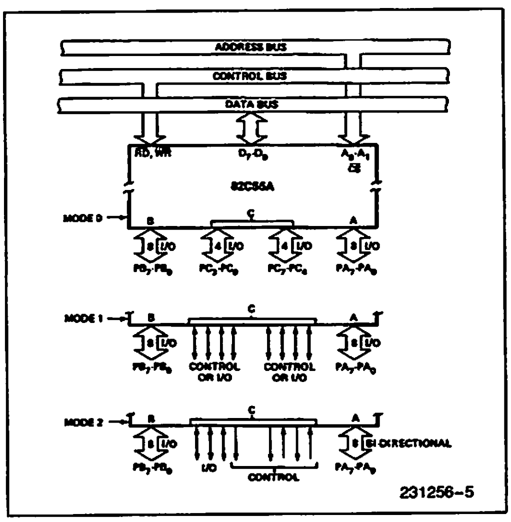


Figure 5. Basic Mode Definitions and Bus Interface

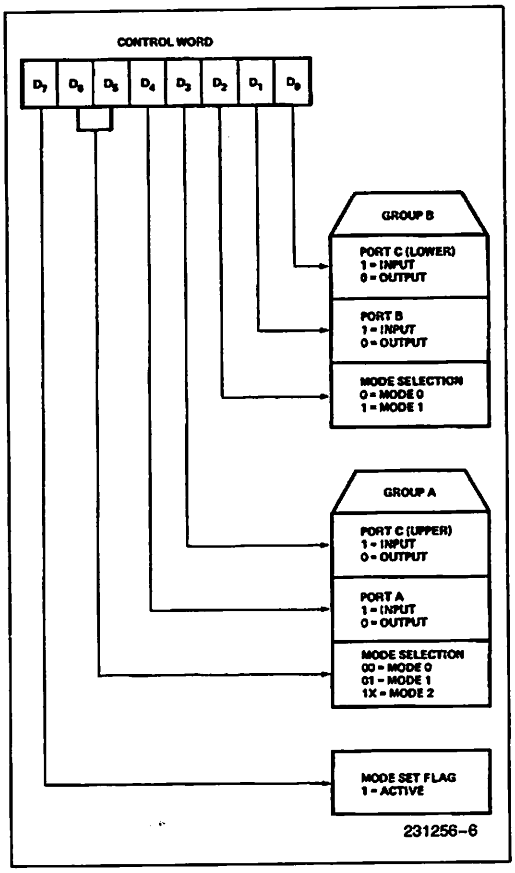


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

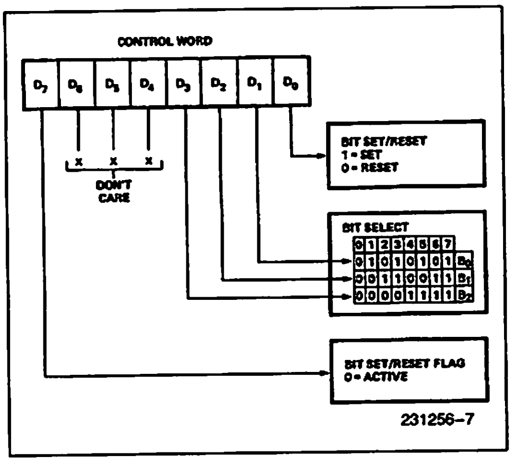


Figure 7. Bit Set/Reset Format

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET)—INTE is SET—Interrupt enable
(BIT-RESET)—INTE is RESET—Interrupt disable

Note:
All Mask flip-flops are automatically reset during mode selection and device Reset.

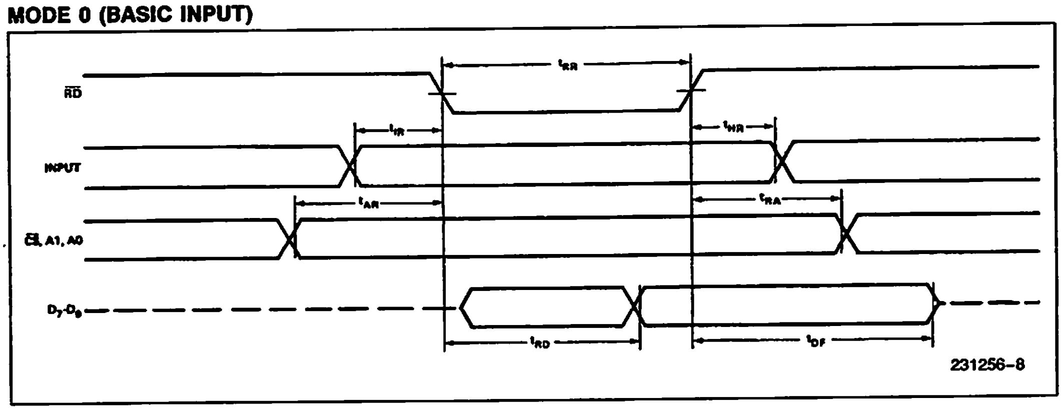
Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

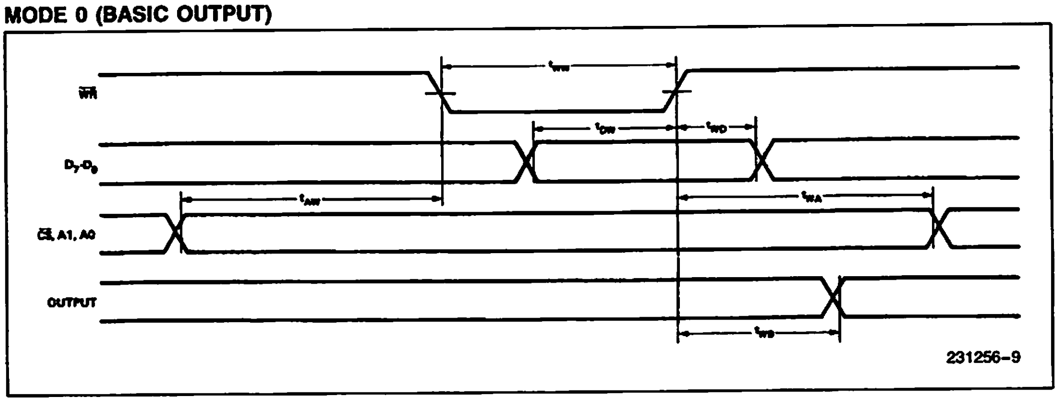
- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

MODE 0 (BASIC INPUT)



231256-8

MODE 0 (BASIC OUTPUT)



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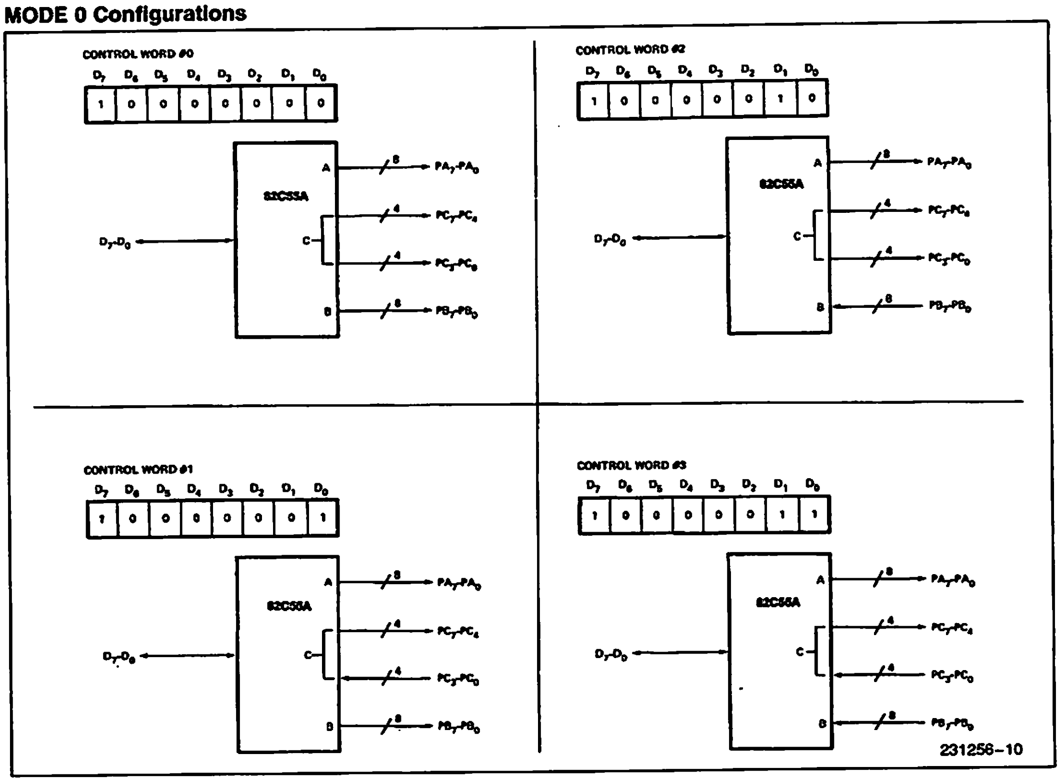
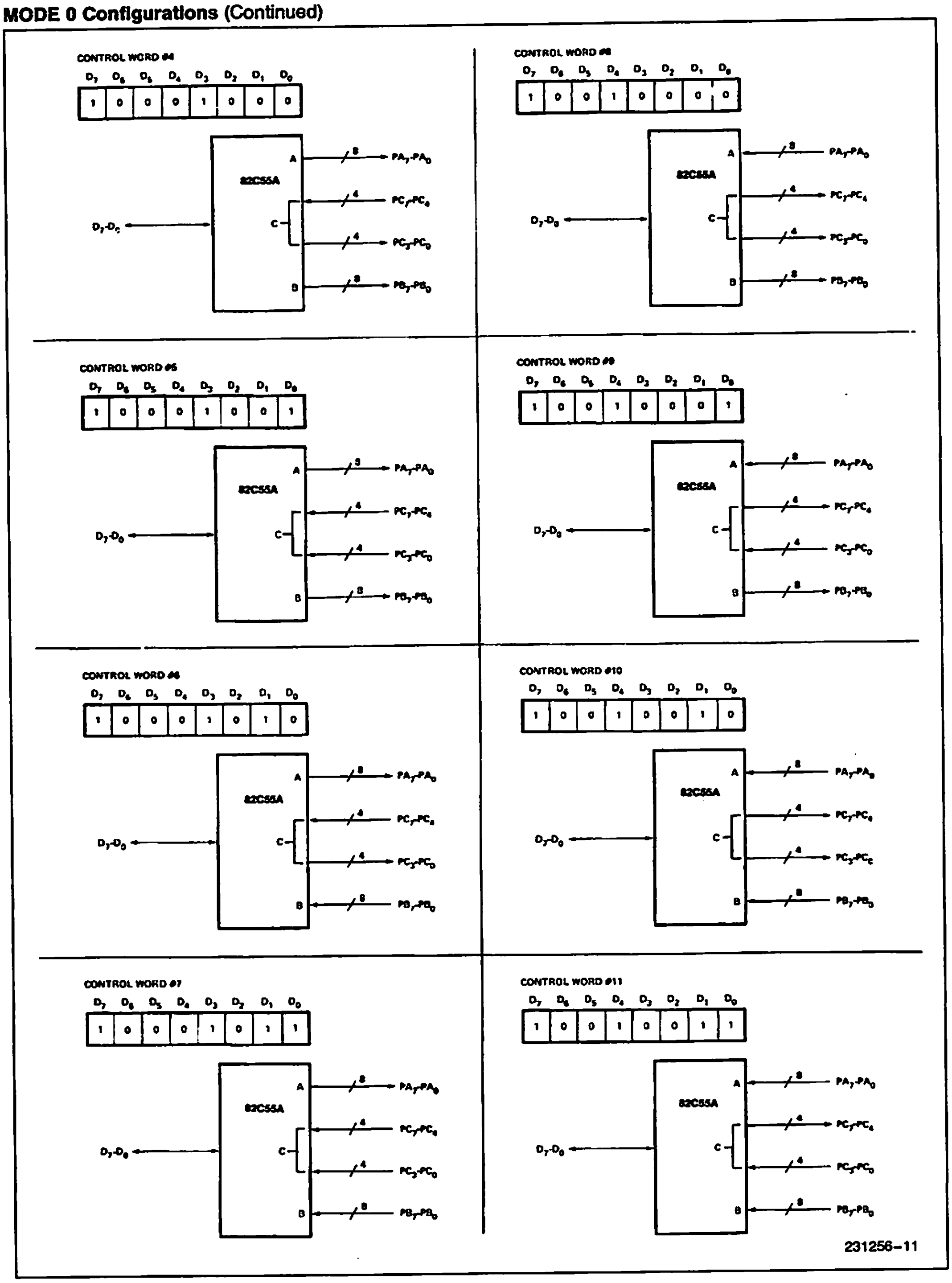
MODE 0 Port Definition

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations

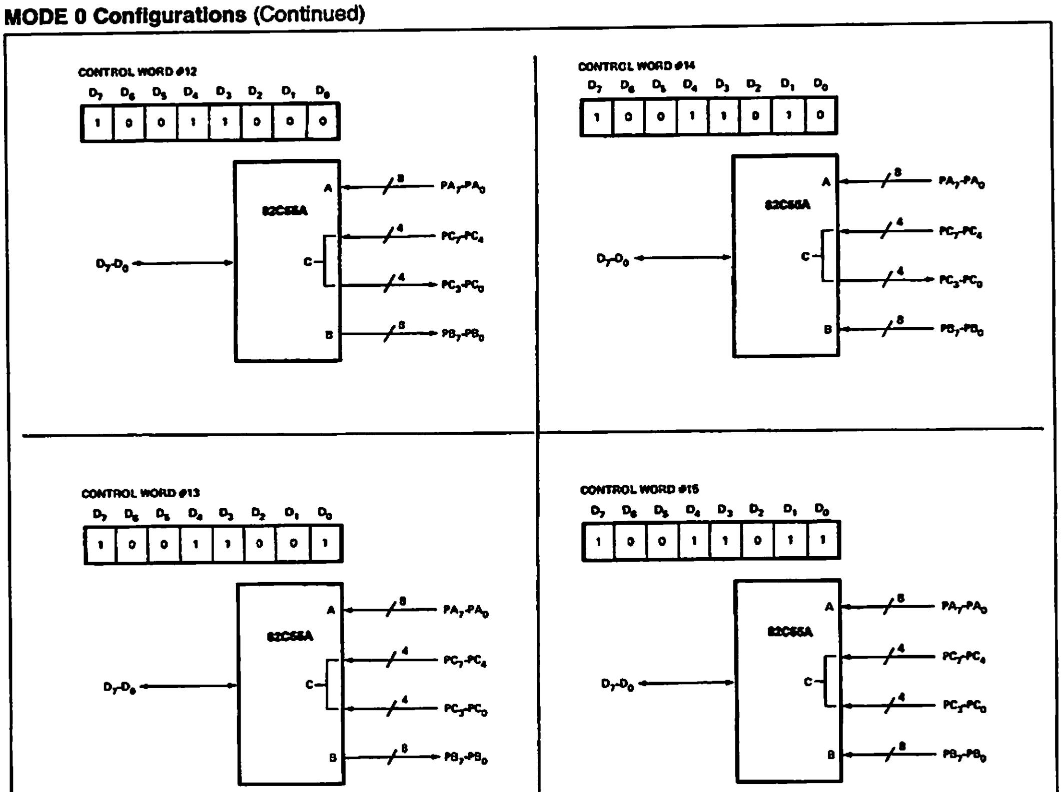


MODE 0 Configurations (Continued)



231256-11

MODE 0 Configurations (Continued)



231256–12

Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic functional Definitions:

- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias....0°C to + 70°C
Storage Temperature ....− 65°C to + 150°C
Supply Voltage ....− 0.5 to + 8.0V
Operating Voltage ....+ 4V to + 7V
Voltage on any Input..........GND−2V to + 6.5V
Voltage on any Output ..GND−0.5V to V_{CC} + 0.5V
Power Dissipation ....1 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

***WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, GND = 0V (T_A = −40°C to +85°C for Extended Temperture)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output High Voltage	3.0 V_{CC} − 0.4		V V	I_{OH} = −2.5 mA I_{OH} = −100 μA
I_{IL}	Input Leakage Current		±1	μA	V_{IN} = V_{CC} to 0V (Note 1)
I_{OFL}	Output Float Leakage Current		±10	μA	V_{IN} = V_{CC} to 0V (Note 2)
I_{DAR}	Darlington Drive Current	±2.5	(Note 4)	mA	Ports A, B, C R_{ext} = 500Ω V_{ext} = 1.7V
I_{PHL}	Port Hold Low Leakage Current	+50	+300	μA	V_{OUT} = 1.0V Port A only
I_{PHH}	Port Hold High Leakage Current	−50	−300	μA	V_{OUT} = 3.0V Ports A, B, C
I_{PHLO}	Port Hold Low Overdrive Current	−350		μA	V_{OUT} = 0.8V
I_{PHHO}	Port Hold High Overdrive Current	+350		μA	V_{OUT} = 3.0V
I_{CC}	V_{CC} Supply Current		10	mA	(Note 3)
I_{CCSB}	V_{CC} Supply Current-Standby		10	μA	V_{CC} = 5.5V V_{IN} = V_{CC} or GND Port Conditions If I/P = Open/High O/P = Open Only With Data Bus = High/Low $\overline{CS}$ = High Reset = Low Pure Inputs = Low/High

NOTES:
1. Pins A_1, A_0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, Reset.
2. Data Bus; Ports B, C.
3. Outputs open.
4. Limit output current to 4.0 mA.

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	Input Capacitance		10	pF	Unmeasured pins returned to GND f_c = 1 MHz(5)
$C_{I/O}$	I/O Capacitance		20	pF	

NOTE:
5. Sampled not 100% tested.

A.C. CHARACTERISTICS

T_A = 0° to 70°C, V_{CC} = +5V ±10%, GND = 0V
T_A = −40°C to +85°C for Extended Temperature

BUS PARAMETERS

READ CYCLE

Symbol	Parameter	82C55A-2		Units	Test Conditions
		Min	Max		
t_{AR}	Address Stable Before $\overline{RD}$ ↓	0		ns	
t_{RA}	Address Hold Time After $\overline{RD}$ ↑	0		ns	
t_{RR}	$\overline{RD}$ Pulse Width	150		ns	
t_{RD}	Data Delay from $\overline{RD}$ ↓		120	ns	
t_{DF}	$\overline{RD}$ ↑ to Data Floating	10	75	ns	
t_{RV}	Recovery Time between $\overline{RD}/\overline{WR}$	200		ns	

WRITE CYCLE

Symbol	Parameter	82C55A-2		Units	Test Conditions
		Min	Max		
t_{AW}	Address Stable Before $\overline{WR}$ ↓	0		ns	
t_{WA}	Address Hold Time After $\overline{WR}$ ↑	20		ns	Ports A & B
		20		ns	Port C
t_{WW}	$\overline{WR}$ Pulse Width	100		ns	
t_{DW}	Data Setup Time Before $\overline{WR}$ ↑	100		ns	
t_{WD}	Data Hold Time After $\overline{WR}$ ↑	30		ns	Ports A & B
		30		ns	Port C

OTHER TIMINGS

Symbol	Parameter	82C55A-2		Units Conditions	Test
		Min	Max		
t_{WB}	$\overline{WR}$ = 1 to Output		350	ns	
t_{IR}	Peripheral Data Before $\overline{RD}$	0		ns	
t_{HR}	Peripheral Data After $\overline{RD}$	0		ns	
t_{AK}	$\overline{ACK}$ Pulse Width	200		ns	
t_{ST}	$\overline{STB}$ Pulse Width	100		ns	
t_{PS}	Per. Data Before $\overline{STB}$ High	20		ns	
t_{PH}	Per. Data After $\overline{STB}$ High	50		ns	
t_{AD}	$\overline{ACK}$ = 0 to Output		175	ns	
t_{KD}	$\overline{ACK}$ = 1 to Output Float	20	250	ns	
t_{WOB}	$\overline{WR}$ = 1 to $\overline{OBF}$ = 0		150	ns	
t_{AOB}	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1		150	ns	
t_{SIB}	$\overline{STB}$ = 0 to IBF = 1		150	ns	
t_{RIB}	$\overline{RD}$ = 1 to IBF = 0		150	ns	
t_{RIT}	$\overline{RD}$ = 0 to INTR = 0		200	ns	
t_{SIT}	$\overline{STB}$ = 1 to INTR = 1		150	ns	
t_{AIT}	$\overline{ACK}$ = 1 to INTR = 1		150	ns	
t_{WIT}	$\overline{WR}$ = 0 to INTR = 0		200	ns	see note 1
t_{RES}	Reset Pulse Width	500		ns	see note 2

NOTE:
1. INTR ↑ may occur as early as $\overline{WR}$ ↓.
2. Pulse width of initial Reset pulse after power on must be at least 50 μSec. Subsequent Reset pulses may be 500 ns minimum. The output Ports A, B, or C may glitch low during the reset pulse but all port pins will be held at a logic "one" level after the reset pulse.

November 2000

National Semiconductor

LM35
Precision Centigrade Temperature Sensors

General Description

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ˚ Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼˚C at room temperature and ±¾˚C over a full −55 to +150˚C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1˚C in still air. The LM35 is rated to operate over a −55˚ to +150˚C temperature range, while the LM35C is rated for a −40˚ to +110˚C range (−10˚ with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.

Features

- Calibrated directly in ˚ Celsius (Centigrade)
- Linear + 10.0 mV/˚C scale factor
- 0.5˚C accuracy guaranteeable (at +25˚C)
- Rated for full −55˚ to +150˚C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 µA current drain
- Low self-heating, 0.08˚C in still air
- Nonlinearity only ±¼˚C typical
- Low impedance output, 0.1 Ω for 1 mA load

Typical Applications

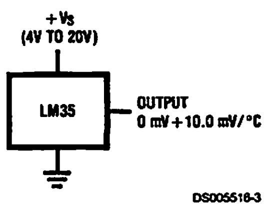
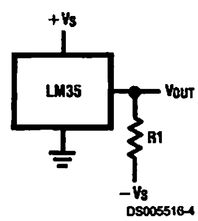


FIGURE 1. Basic Centigrade Temperature Sensor (+2˚C to +150˚C)



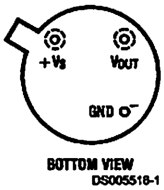
Choose $R_1 = -V_S/50\ \mu A$
V_{OUT}=+1,500 mV at +150˚C
= +250 mV at +25˚C
= −550 mV at −55˚C

FIGURE 2. Full-Range Centigrade Temperature Sensor

 DS005516 www.national.com

Connection Diagrams

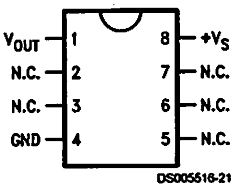
TO-46
Metal Can Package*



*Case is connected to negative pin (GND)

Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

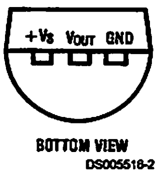
SO-8
Small Outline Molded Package



N.C. = No Connection

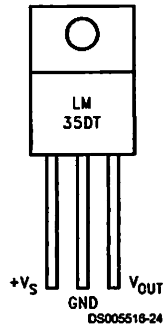
Top View
Order Number LM35DM
See NS Package Number M08A

TO-92
Plastic Package



Order Number LM35CZ, LM35CAZ or LM35DZ
See NS Package Number Z03A

TO-220
Plastic Package*



*Tab is connected to the negative pin (GND).
Note: The LM35DT pinout is different than the discontinued LM35DP.

Order Number LM35DT
See NS Package Number TA03F

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temp.;	
TO-46 Package,	−60°C to +180°C
TO-92 Package,	−60°C to +150°C
SO-8 Package,	−65°C to +150°C
TO-220 Package,	−65°C to +150°C
Lead Temp.:	
TO-46 Package, (Soldering, 10 seconds)	300°C
TO-92 and TO-220 Package, (Soldering, 10 seconds)	260°C
SO Package (Note 12)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	2500V

Specified Operating Temperature Range: T_{MIN} to T_{MAX} (Note 2)

LM35, LM35A	−55°C to +150°C
LM35C, LM35CA	−40°C to +110°C
LM35D	0°C to +100°C

Electrical Characteristics

Notes 1, 6)

Parameter	Conditions	LM35A			LM35CA			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
curacy	T_A=+25°C	±0.2	±0.5		±0.2	±0.5		°C
ote 7)	T_A=−10°C	±0.3			±0.3		±1.0	°C
	T_A=T_{MAX}	±0.4	±1.0		±0.4	±1.0		°C
	T_A=T_{MIN}	±0.4	±1.0		±0.4		±1.5	°C
onlinearity lote 8)	T_{MIN}≤T_A≤T_{MAX}	±0.18		±0.35	±0.15		±0.3	°C
ensor Gain verage Slope)	T_{MIN}≤T_A≤T_{MAX}	+10.0	+9.9, +10.1		+10.0		+9.9, +10.1	mV/°C
ad Regulation	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		mV/mA
lote 3) 0≤I_L≤1 mA	T_{MIN}≤T_A≤T_{MAX}	±0.5		±3.0	±0.5		±3.0	mV/mA
ne Regulation	T_A=+25°C	±0.01	±0.05		±0.01	±0.05		mV/V
lote 3)	4V≤V_S≤30V	±0.02		±0.1	±0.02		±0.1	mV/V
uiescent Current	V_S=+5V, +25°C	56	67		56	67		µA
lote 9)	V_S=+5V	105		131	91		114	µA
	V_S=+30V, +25°C	56.2	68		56.2	68		µA
	V_S=+30V	105.5		133	91.5		116	µA
hange of	4V≤V_S≤30V, +25°C	0.2	1.0		0.2	1.0		µA
uiescent Current lote 3)	4V≤V_S≤30V	0.5		2.0	0.5		2.0	µA
emperature oefficient of uiescent Current		+0.39		+0.5	+0.39		+0.5	µA/°C
inimum Temperature r Rated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
ong Term Stability	T_J=T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Electrical Characteristics

(Notes 1, 6)

Parameter	Conditions	LM35			LM35C, LM35D			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy, LM35, LM35C (Note 7)	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		°C
	T_A=−10°C	±0.5			±0.5		±1.5	°C
	$T_A=T_{MAX}$	±0.8	±1.5		±0.8		±1.5	°C
	$T_A=T_{MIN}$	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D (Note 7)	T_A=+25°C				±0.6	±1.5		°C
	$T_A=T_{MAX}$				±0.9		±2.0	°C
	$T_A=T_{MIN}$				±0.9		±2.0	°C
Nonlinearity (Note 8)	$T_{MIN}\le T_A\le T_{MAX}$	**±0.3**		**±0.5**	**±0.2**		**±0.5**	°C
Sensor Gain (Average Slope)	$T_{MIN}\le T_A\le T_{MAX}$	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°C
Load Regulation (Note 3) $0\le I_L\le 1$ mA	T_A=+25°C	±0.4	±2.0		±0.4	±2.0		mV/mA
	$T_{MIN}\le T_A\le T_{MAX}$	**±0.5**		**±5.0**	**±0.5**		**±5.0**	mV/mA
Line Regulation (Note 3)	T_A=+25°C	±0.01	±0.1		±0.01	±0.1		mV/V
	$4V\le V_S\le 30V$	**±0.02**		**±0.2**	**±0.02**		**±0.2**	mV/V
Quiescent Current (Note 9)	V_S=+5V, +25°C	56	80		56	80		μA
	V_S=+5V	**105**		**158**	**91**		**138**	μA
	V_S=+30V, +25°C	56.2	82		56.2	82		μA
	V_S=+30V	**105.5**		**161**	**91.5**		**141**	μA
Change of Quiescent Current (Note 3)	$4V\le V_S\le 30V$, +25°C	0.2	2.0		0.2	2.0		μA
	$4V\le V_S\le 30V$	**0.5**		**3.0**	**0.5**		**3.0**	μA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.7**	**+0.39**		**+0.7**	μA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	$T_J=T_{MAX}$, for 1000 hours	±0.08			±0.08			°C

Note 1: Unless otherwise noted, these specifications apply: −55°C≤T_J≤+150°C for the LM35 and LM35A; −40°≤T_J≤+110°C for the LM35C and LM35CA; and 0°≤T_J≤+100°C for the LM35D. V_S=+5Vdc and I_{LOAD}=50 μA, in the circuit of *Figure 2.* These specifications also apply from +2°C to T_{MAX} in the circuit of *Figure 1.* Specifications in **boldface** apply over the full rated temperature range.

Note 2: Thermal resistance of the TO-46 package is 400°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient. Thermal resistance of the small outline molded package is 220°C/W junction to ambient. Thermal resistance of the TO-220 package is 90°C/W junction to ambient. For additional thermal resistance information see table in the Applications section.

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in **boldface** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1.*

Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 12: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Typical Applications

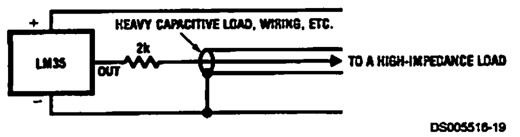


FIGURE 3. LM35 with Decoupling from Capacitive Load

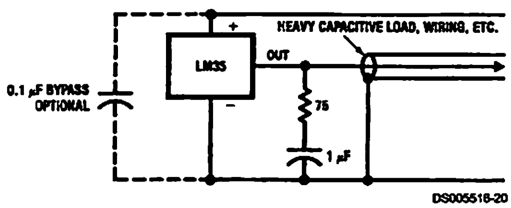


FIGURE 4. LM35 with R-C Damper

CAPACITIVE LOADS

Like most micropower circuits, the LM35 has a limited ability to drive heavy capacitive loads. The LM35 by itself is able to drive 50 pf without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure 3*. Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure 4*.

When the LM35 is applied with a 200Ω load resistor as shown in *Figure 5*, *Figure 6* or *Figure 8* it is relatively immune to wiring capacitance because the capacitance forms a bypass from ground to input, not on the output. However, as with any linear circuit connected to wires in a hostile environment, its performance can be affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR transients, etc, as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from V_{IN} to ground and a series R-C damper such as 75Ω in series with 0.2 or 1 μF from output to ground are often useful. These are shown in *Figure 13*, *Figure 14*, and *Figure 16*.

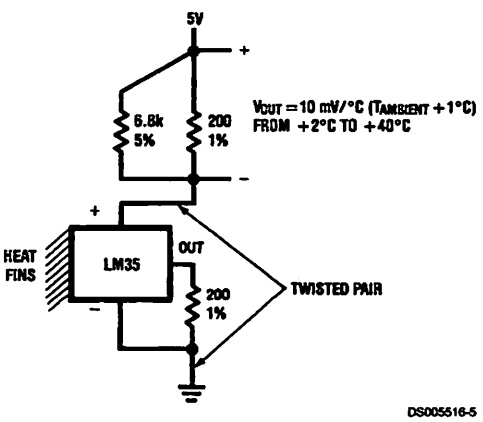


FIGURE 5. Two-Wire Remote Temperature Sensor (Grounded Sensor)

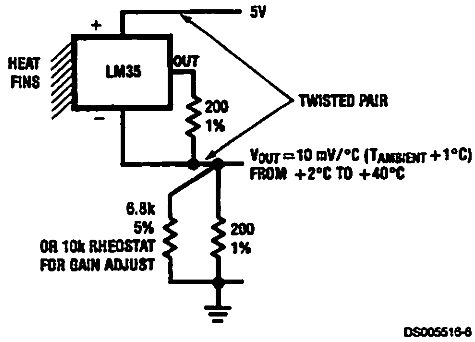


FIGURE 6. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

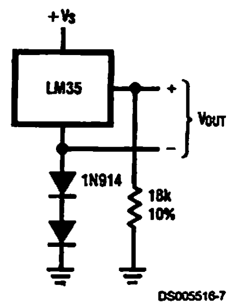


FIGURE 7. Temperature Sensor, Single Supply, −55° to +150°C

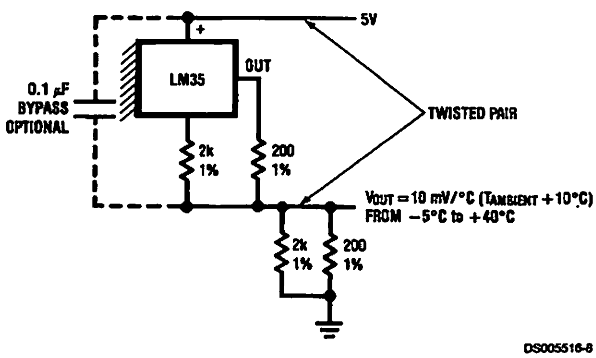


FIGURE 8. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

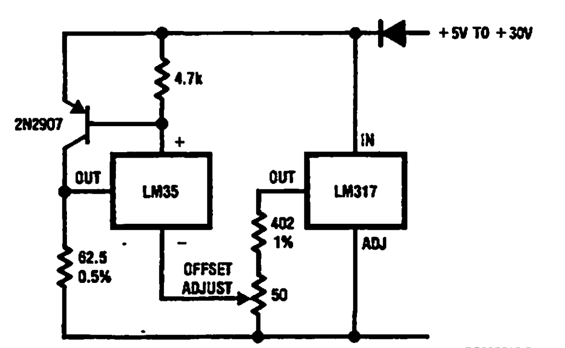


FIGURE 9. 4-To-20 mA Current Source (0°C to +100°C)

Typical Applications (Continued)

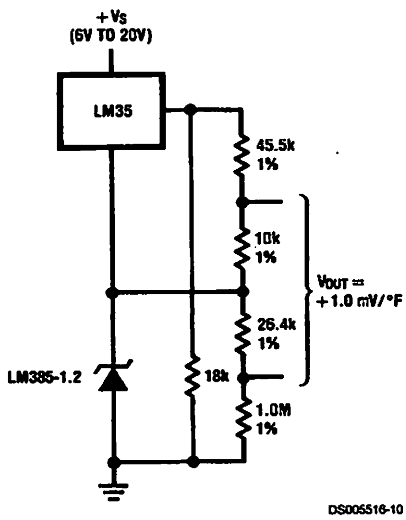


FIGURE 10. Fahrenheit Thermometer

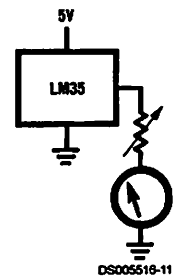


FIGURE 11. Centigrade Thermometer (Analog Meter)

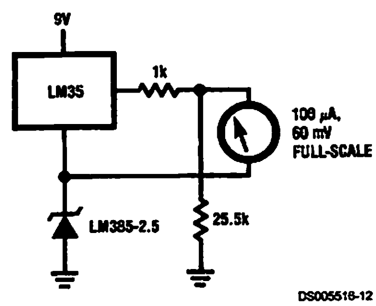


FIGURE 12. Fahrenheit ThermometerExpanded Scale Thermometer
(50° to 80° Fahrenheit, for Example Shown)

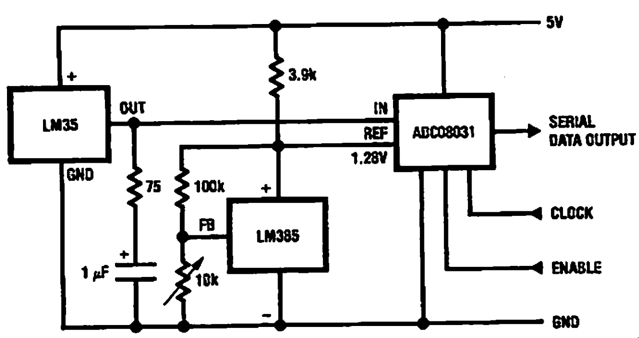


FIGURE 13. Temperature To Digital Converter (Serial Output) (+128°C Full Scale)

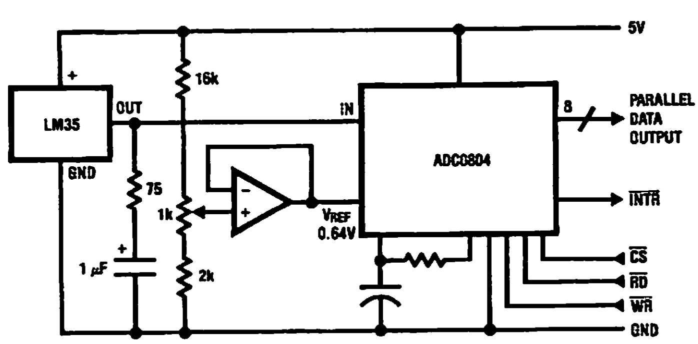
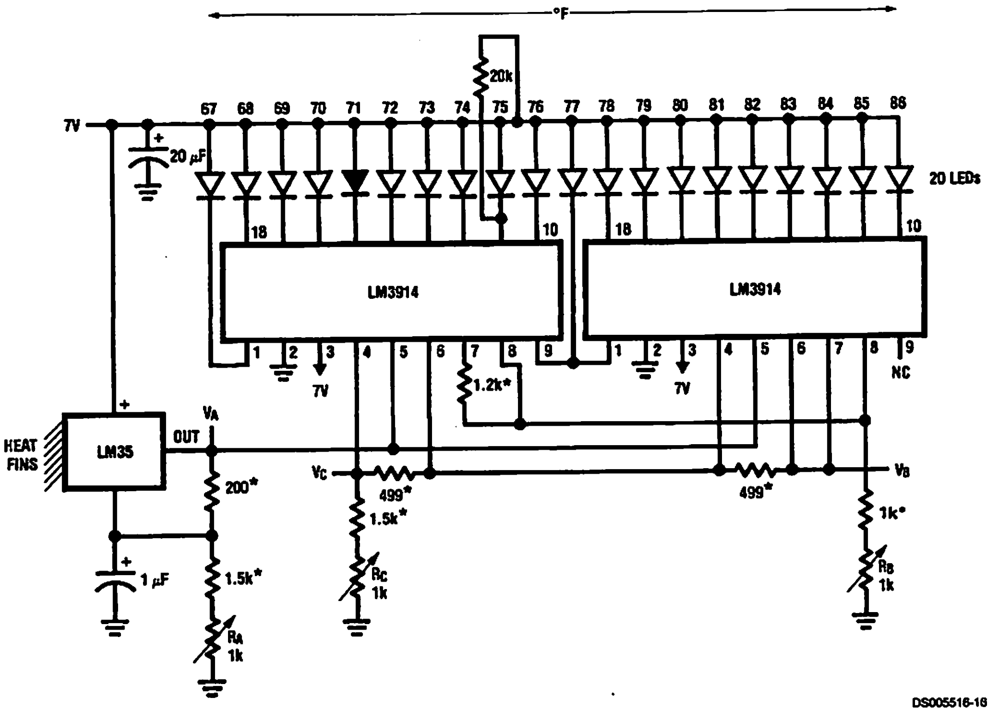


FIGURE 14. Temperature To Digital Converter (Parallel TRI-STATE™ Outputs for Standard Data Bus to µP Interface) (128°C Full Scale)

Typical Applications (Continued)



*=1% or 2% film resistor
Trim R_B for V_B=3.075V
Trim R_C for V_C=1.955V
Trim R_A for V_A=0.075V + 100mV/°C x $T_{ambient}$
Example, V_A=2.275V at 22°C

FIGURE 15. Bar-Graph Temperature Display (Dot Mode)

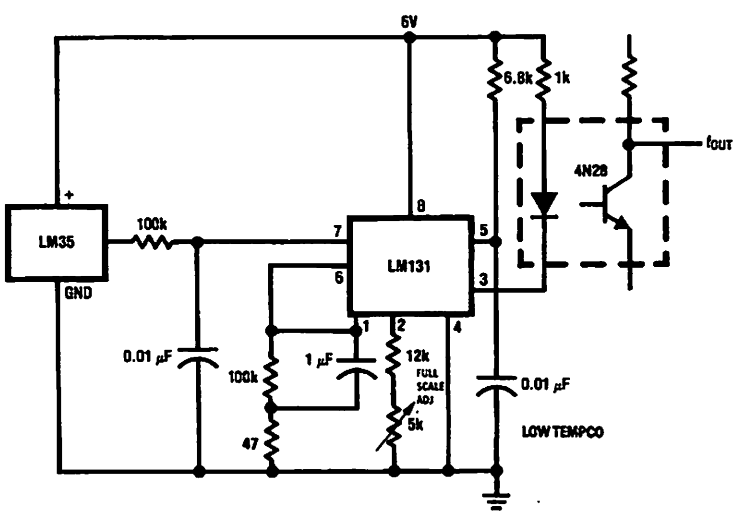
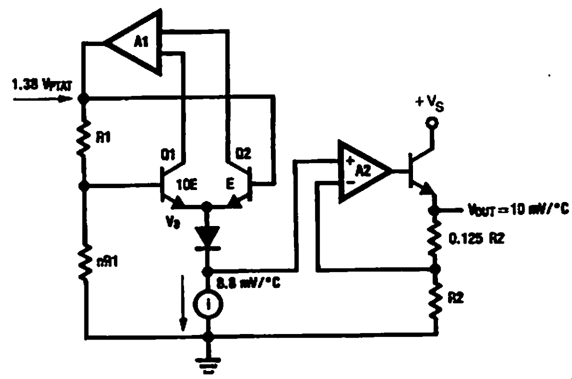


FIGURE 16. LM35 With Voltage-To-Frequency Converter And Isolated Output (2°C to +150°C; 20 Hz to 1500 Hz)

Block Diagram



DS005516-23

August 2000

National Semiconductor

LM741
Operational Amplifier

General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

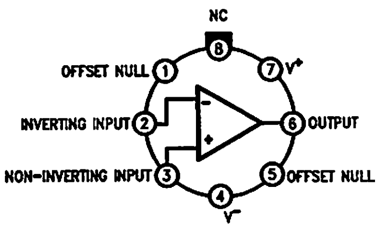
The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Features

Connection Diagrams

Metal Can Package

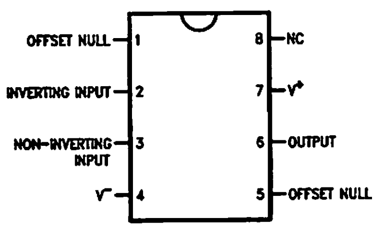


00934102

Note 1: LM741H is available per JM38510/10101

Order Number LM741H, LM741H/883 (Note 1), LM741AH/883 or LM741CH
See NS Package Number H08C

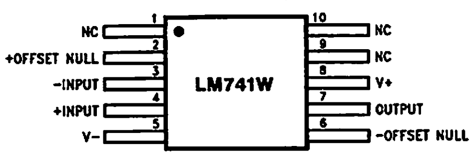
Dual-In-Line or S.O. Package



00934103

Order Number LM741J, LM741J/883, LM741CN
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak

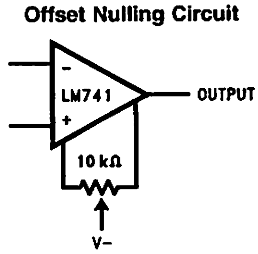


00934106

Order Number LM741W/883
See NS Package Number W10A

Typical Application

Offset Nulling Circuit



00934107

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 7)

	LM741A	LM741	LM741C
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V
Input Voltage (Note 4)	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	150°C	100°C
Soldering Information			
N-Package (10 seconds)	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C
M-Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering
surface mount devices.

	LM741A	LM741	LM741C
ESD Tolerance (Note 8)	400V	400V	400V

Electrical Characteristics (Note 5)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$										
	$R_S \le 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \le 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 50\Omega$			4.0							mV
	$R_S \le 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							μV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	μA
Input Resistance	$T_A = 25°C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V

Electrical Characteristics (Note 5) (Continued)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
rge Signal Voltage Gain	$T_A = 25°C$, $R_L \geq 2\ k\Omega$										
	$V_S = \pm 20V$, $V_O = \pm 15V$	50									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
	$R_L \geq 2\ k\Omega$,										
	$V_S = \pm 20V$, $V_O = \pm 15V$	32									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				25			15			V/mV
	$V_S = \pm 5V$, $V_O = \pm 2V$	10									V/mV
utput Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	±16									V
	$R_L \geq 2\ k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$				±10	±13		±10	±13		V
utput Short Circuit	$T_A = 25°C$	10	25	35		25			25		mA
urrent	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
ommon-Mode	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
ejection Ratio	$R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\Omega$, $V_{CM} = \pm 12V$	80	95								dB
upply Voltage Rejection	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
atio	$V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10\ k\Omega$				77	96		77	96		dB
ransient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
andwidth (Note 6)	$T_A = 25°C$	0.437	1.5								MHz
lew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/µs
upply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
ower Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Electrical Characteristics (Note 5) (Continued)

Note 3: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100˚C/W	100˚C/W	170˚C/W	195˚C/W
θ_{jC} (Junction to Case)	N/A	N/A	25˚C/W	N/A

Note 4: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

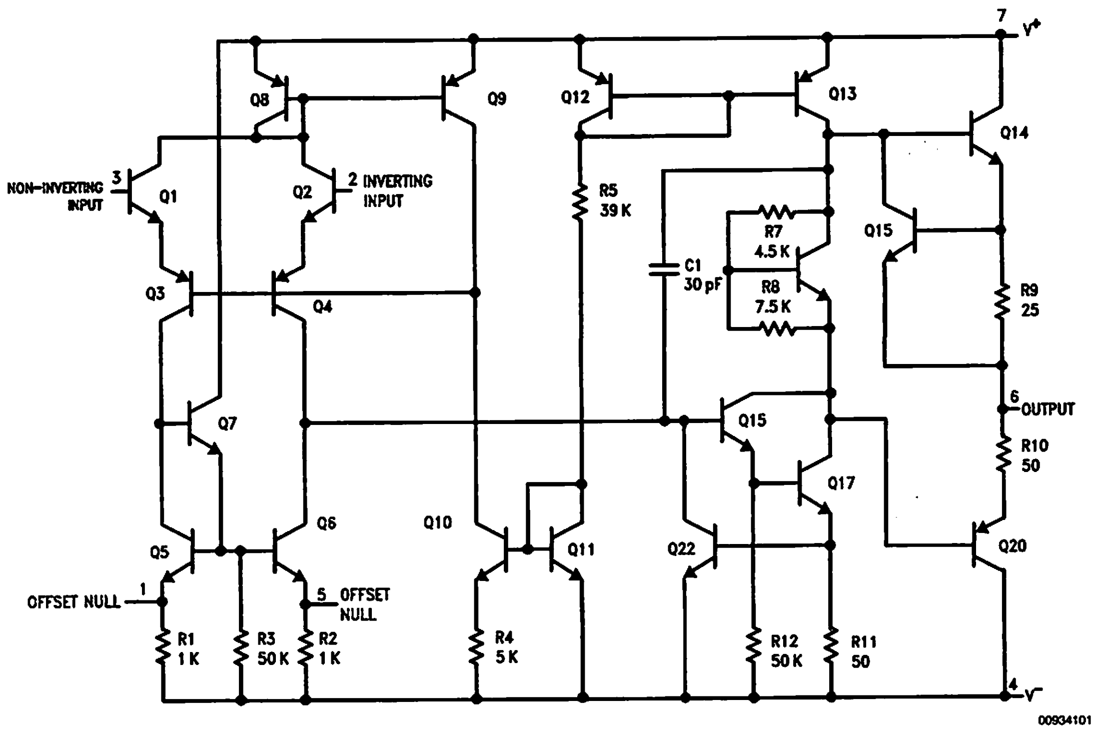
Note 5: Unless otherwise specified, these specifications apply for V_S = ±15V, −55˚C ≤ T_A ≤ +125˚C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0˚C ≤ T_A ≤ +70˚C.

Note 6: Calculated value from: BW (MHz) = 0.35/Rise Time(µs).

Note 7: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Schematic Diagram



February 2000

National Semiconductor

LM555
Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

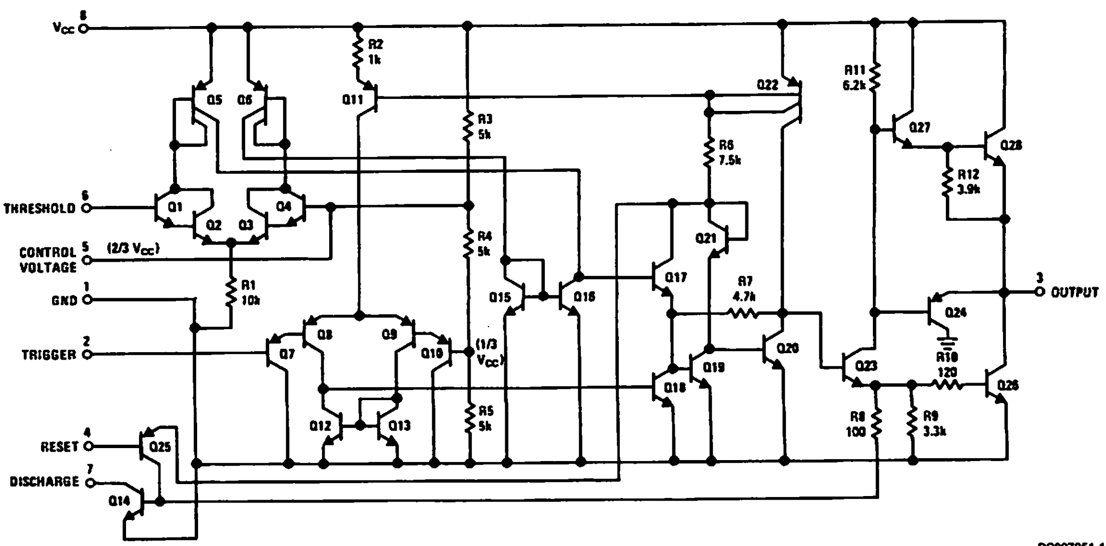
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram

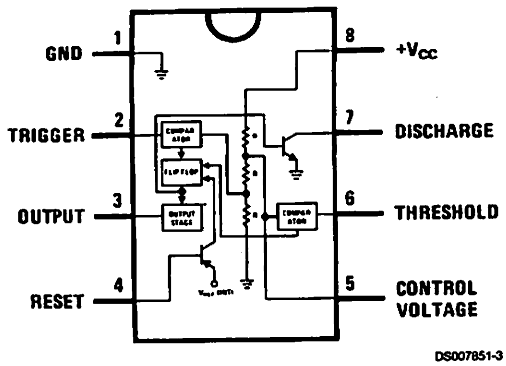


DS007851-1

 DS007851

Connection Diagram

Dual-In-Line, Small Outline and Molded Mini Small Outline Packages



Top View

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Packages (SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

(T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits LM555C Min	Limits LM555C Typ	Limits LM555C Max	Units
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞ (Low State) (Note 4)		3 10	6 15	mA
Timing Error, Monostable					
Initial Accuracy			1		%
Drift with Temperature	R_A = 1k to 100kΩ, C = 0.1µF, (Note 5)		50		ppm/°C
Accuracy over Temperature			1.5		%
Drift with Supply			0.1		%/V
Timing Error, Astable					
Initial Accuracy			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100kΩ, C = 0.1µF, (Note 5)		150		ppm/°C
Accuracy over Temperature			3.0		%
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V		5		V
	V_{CC} = 5V		1.67		V
Trigger Current			0.5	0.9	µA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V V_{CC} = 5V	9 2.6	10 3.33	11 4	V
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat (Note 7)					
Output Low	V_{CC} = 15V, I_7 = 15mA		180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5mA		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V				
	I_{SINK} = 10mA		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.75	V
	I_{SINK} = 100mA		2	2.5	V
	I_{SINK} = 200mA		2.5		V
	V_{CC} = 5V				
	I_{SINK} = 8mA				V
	I_{SINK} = 5mA		0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200mA, V_{CC} = 15V		12.5		V
	I_{SOURCE} = 100mA, V_{CC} = 15V	12.75	13.3		V
	V_{CC} = 5V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 106°C/W (DIP), 170°C/W (S0-8), and 204°C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20MΩ.

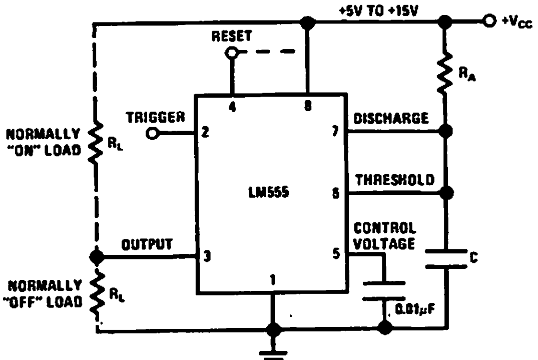
Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

∖pplications Information

∕IONOSTABLE OPERATION

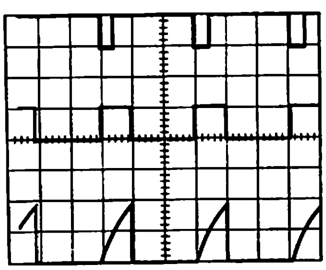
n this mode of operation, the timer functions as a one-shot *Figure 1*). The external capacitor is initially held discharged ›y a transistor inside the timer. Upon application of a negaive trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is ;et which both releases the short circuit across the capacitor ınd drives the output high.



DS007851-5

FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



DS007851-6

V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 9.1kΩ
C = 0.01μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

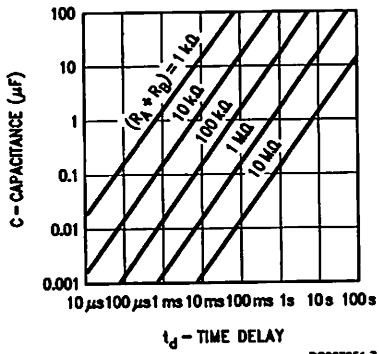
FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

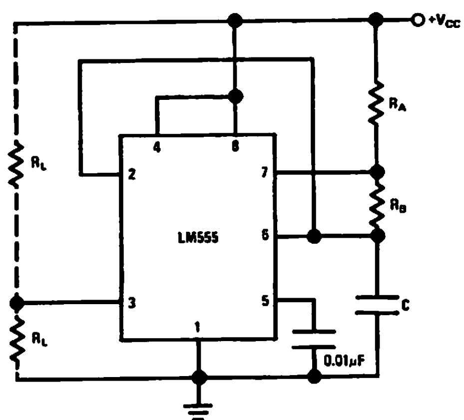


DS007851-7

FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.



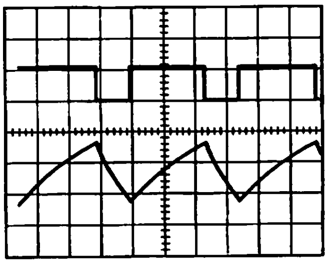
DS007851-8

FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



DS007851-9

V_{CC} = 5V
TIME = 20µs/DIV.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

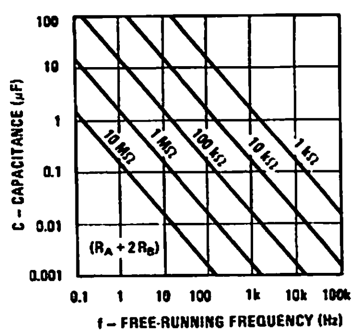
The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

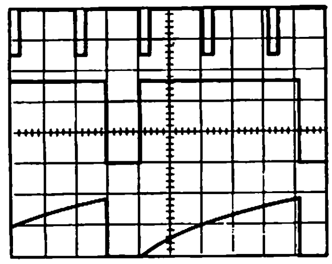


DS007851-10

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



DS007851-11

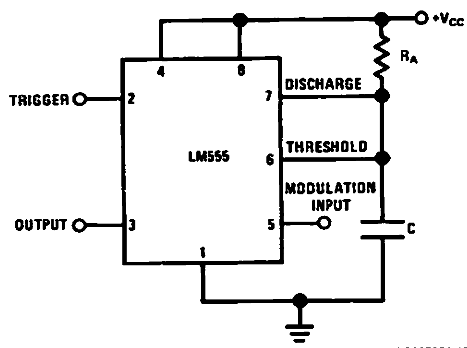
V_{CC} = 5V
TIME = 20µs/DIV.
R_A = 9.1kΩ
C = 0.01µF

Top Trace: Input 4V/Div.
Middle Trace: Output 2V/Div.
Bottom Trace: Capacitor 2V/Div.

FIGURE 7. Frequency Divider

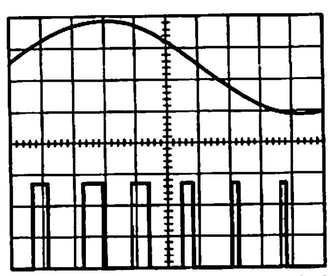
PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.



DS007851-12

FIGURE 8. Pulse Width Modulator



DS007851-13

V_{CC} = 5V
TIME = 0.2 ms/DIV.
R_A = 9.1kΩ
C = 0.01µF

Top Trace: Modulation 1V/Div.
Bottom Trace: Output Voltage 2V/Div.

FIGURE 9. Pulse Width Modulator

\pplications Information (Continued)

'ULSE POSITION MODULATOR

'his application uses the timer connected for astable opera- on, as in *Figure 10,* with a modulating signal again applied ɔ the control voltage terminal. The pulse position varies with ne modulating signal, since the threshold voltage and hence he time delay is varied. *Figure 11* shows the waveforms jenerated for a triangle wave modulation signal.

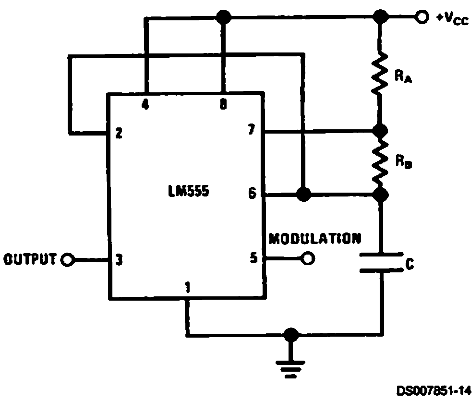
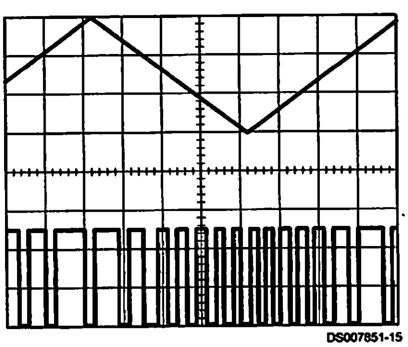


FIGURE 10. Pulse Position Modulator



V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output 2V/Div.

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.

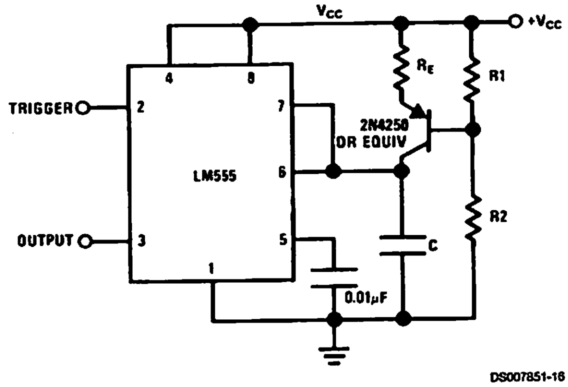


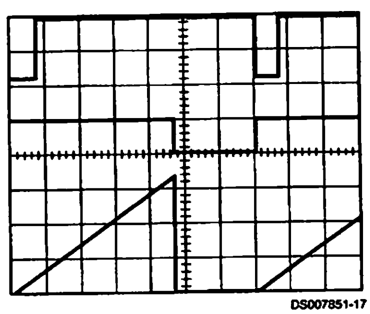
FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$

$$V_{BE} \cong 0.6V$$



V_{CC} = 5V
TIME = 20µs/DIV.
R_1 = 47kΩ
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 µF

Top Trace: Input 3V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 13. Linear Ramp

Applications Information (Continued)

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$

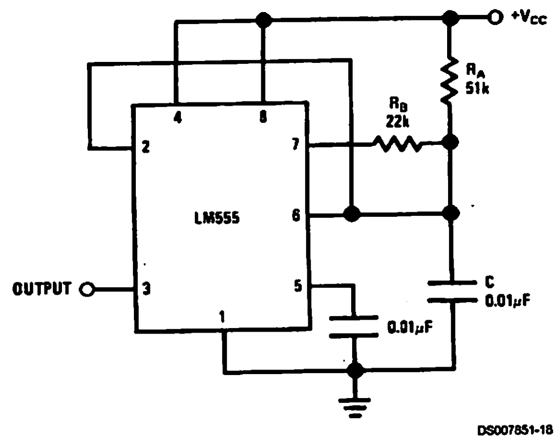


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

Lower comparator storage time can be as long as 10µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10µs minimum.

Delay time reset to output is 0.47µs typical. Minimum reset pulse width must be 0.3µs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

October 1999

National Semiconductor

ADC0808/ADC0809
8-Bit µP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

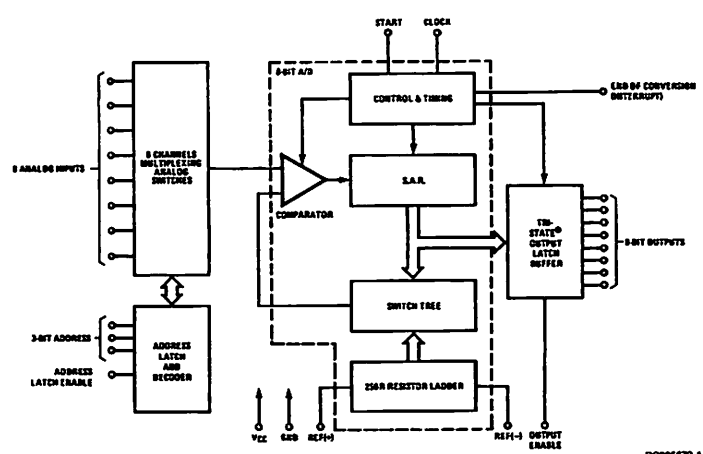
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 µs

Block Diagram



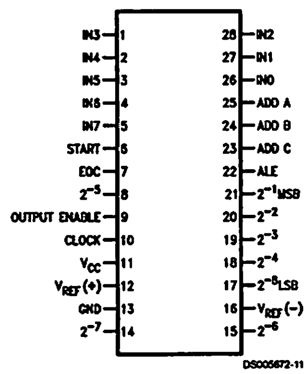
DS005672-1

See Ordering Information

TRI-STATE® is a registered trademark of National Semiconductor Corp.

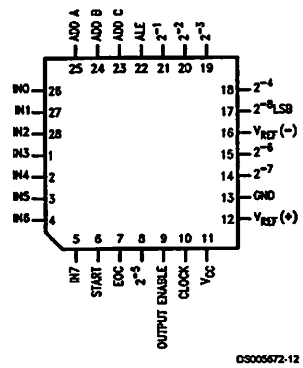
Connection Diagrams

Dual-In-Line Package



Order Number ADC0808CCN or ADC0809CCN
See NS Package J28A or N28A

Molded Chip Carrier Package



Order Number ADC0808CCV or ADC0809CCV
See NS Package V28A

Ordering Information

TEMPERATURE RANGE		−40˚C to +85˚C			−55˚C to +125˚C
Error	±½ LSB Unadjusted	ADC0808CCN	ADC0808CCV	ADC0808CCJ	ADC0808CJ
	±1 LSB Unadjusted	ADC0809CCN	ADC0809CCV		
Package Outline		N28A Molded DIP	V28A Molded Chip Carrier	J28A Ceramic DIP	J28A Ceramic DIP

Absolute Maximum Ratings (Notes 2, 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin	−0.3V to (V_{CC}+0.3V)
Except Control Inputs	
Voltage at Control Inputs	−0.3V to +15V
(START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 8)	400V

Operating Conditions (Notes 1, 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CCN,ADC0809CCN	−40°C≤T_A≤+85°C
ADC0808CCV, ADC0809CCV	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: V_{CC}=5 V_{DC}=V_{REF+}, $V_{REF(-)}$=GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			±½	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±¾	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			±1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±1¼	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2-0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
I_{IN}	Comparator Input Current	f_c=640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75≤V_{CC}≤5.25V, −40°C≤T_A≤+85°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=5V,				
		T_A=25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=0,				
		T_A=25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN}=15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN}=0	−1.0			μA
I_{CC}	Supply Current	f_{CLK}=640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, $4.75\le V_{CC}\le 5.25V$, $-40^\circ C\le T_A\le +85^\circ C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V I_{OUT} = −360µA I_{OUT} = −10µA		2.4 4.5		V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O=1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O=1.2 mA			0.45	V
I_{OUT}	TRI-STATE Output Current	V_O=5V V_O=0	 −3		3 	µA µA

Electrical Characteristics

Timing Specifications $V_{CC}=V_{REF(+)}=5V$, $V_{REF(-)}=GND$, $t_r=t_f=20$ ns and $T_A=25^\circ C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	(*Figure 5*)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(*Figure 5*)		100	200	ns
t_s	Minimum Address Set-Up Time	(*Figure 5*)		25	50	ns
t_H	Minimum Address Hold Time	(*Figure 5*)		25	50	ns
t_D	Analog MUX Delay Time From ALE	R_S=0Ω (*Figure 5*)		1	2.5	µs
t_{H1}, t_{H0}	OE Control to Q Logic State	C_L=50 pF, R_L=10k (*Figure 8*)		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	C_L=10 pF, R_L=10k (*Figure 8*)		125	250	ns
t_c	Conversion Time	f_c=640 kHz, (*Figure 5*) (Note 7)	90	100	116	µs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(*Figure 5*)	0		8+2 µS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless othewise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC}n supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0V_{DC} to 5V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (*Figure 6*). See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. *Table 1* shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1.

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (*Figure 1*) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

Functional Description (Continued)

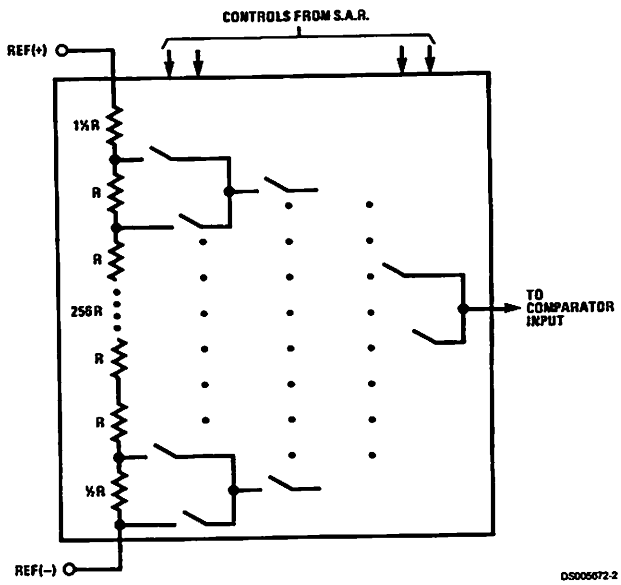


FIGURE 1. Resistor Ladder and Switch Tree

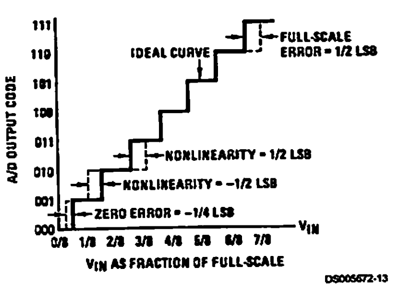


FIGURE 2. 3-Bit A/D Transfer Curve

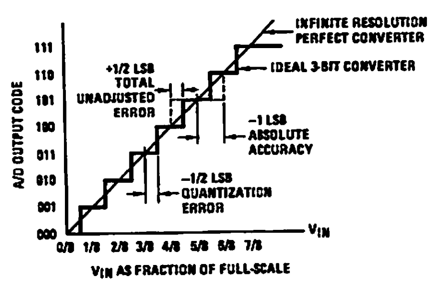


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

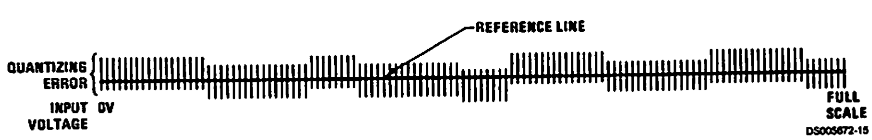


FIGURE 4. Typical Error Curve

Timing Diagram

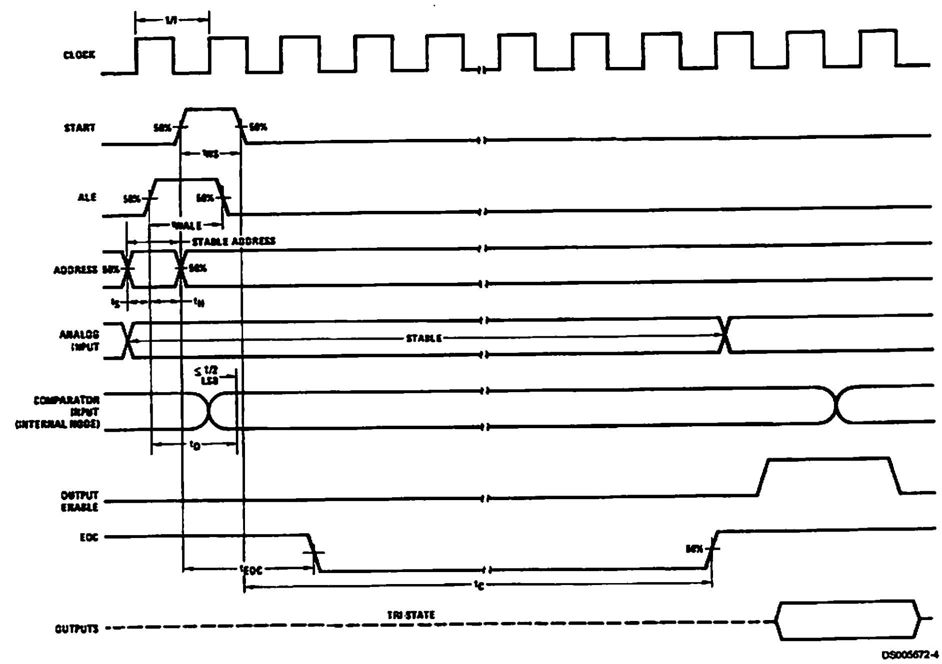


FIGURE 5.

Typical Performance Characteristics

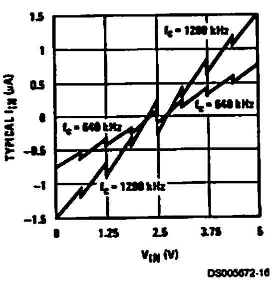


FIGURE 6. Comparator I_{IN} vs V_{IN} (V_{CC}=V_{REF}=5V)

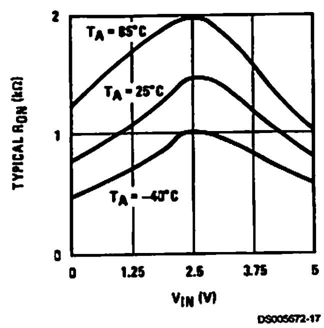


FIGURE 7. Multiplexer R_{ON} vs V_{IN} (V_{CC}=V_{REF}=5V)

TRI-STATE Test Circuits and Timing Diagrams

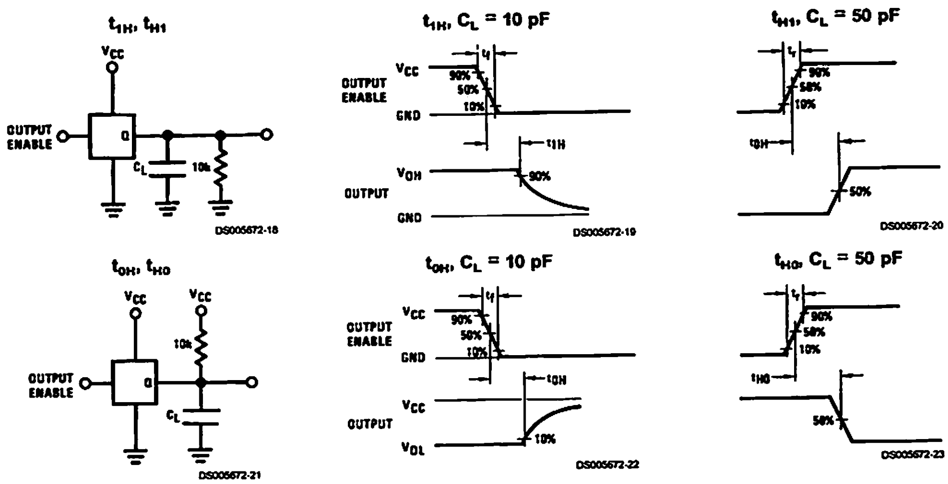


FIGURE 8.

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \qquad (1)$$

V_{IN}=Input voltage into the ADC0808

V_{fs}=Full-scale voltage

V_Z=Zero voltage

D_X=Data point being measured

D_{MAX}=Maximum data limit

D_{MIN}=Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (*Figure 9*).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a sys-

Applications Information (Continued)

tem reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC}=V_{REF}=5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

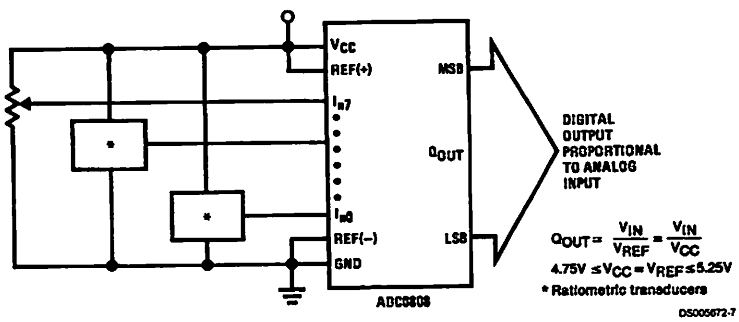
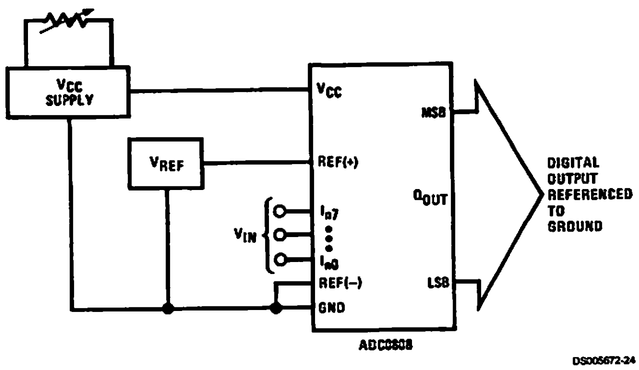


FIGURE 9. Ratiometric Conversion System

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 µF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

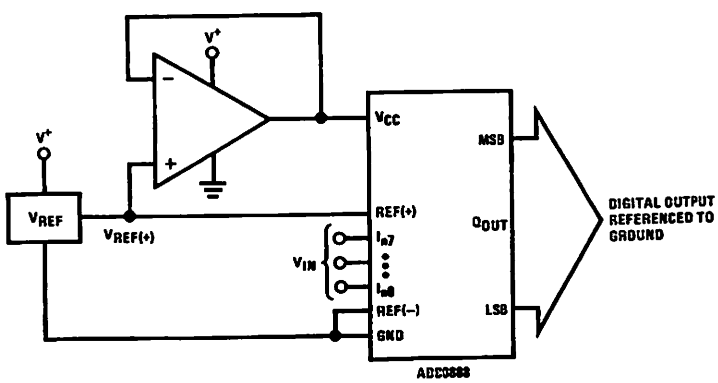
Applications Information (Continued)



$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply



$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

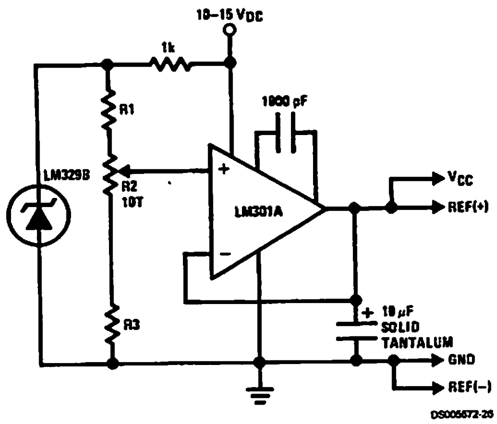
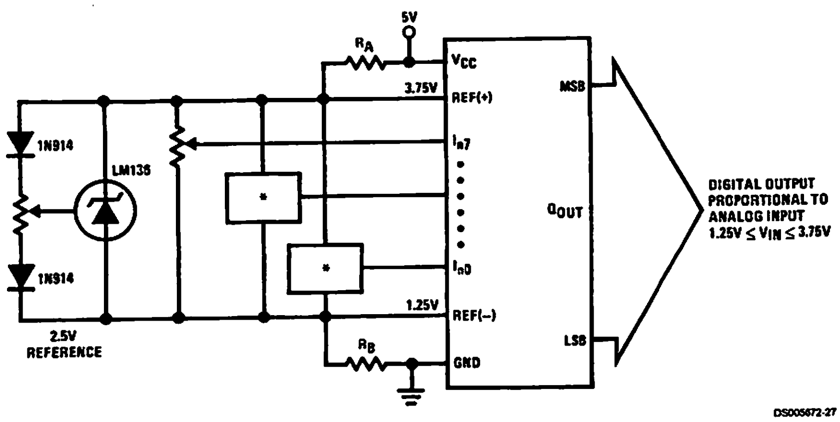


FIGURE 12. Typical Reference and Supply Circuit



$R_A = R_B$

*Ratiometric transducers

FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

Where: V_{IN}=Voltage at comparator input

$V_{REF(+)}$=Voltage at Ref(+)

$V_{REF(-)}$=Voltage at Ref(−)

V_{TUE}=Total unadjusted error voltage (typically $V_{REF(+)}$÷512)

Applications Information (Continued)

4.0 ANALOG COMPARATOR INPUTS

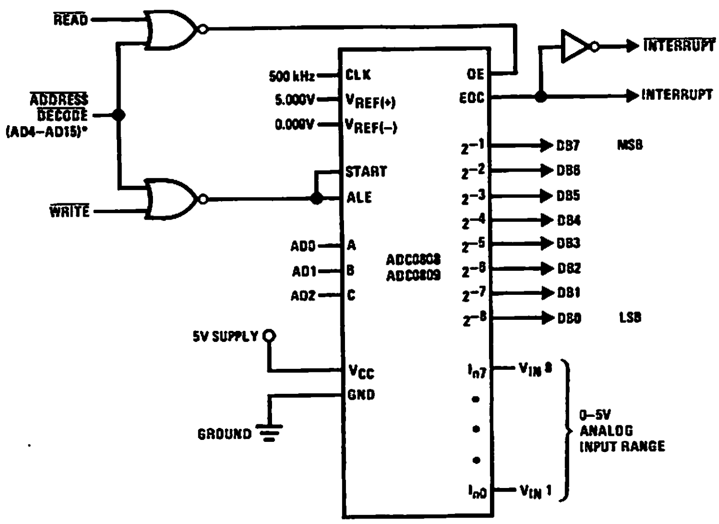
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Typical Application



DS005672-10

*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

TABLE 2. Microprocessor Interface Table

PROCESSOR	$\overline{READ}$	$\overline{WRITE}$	INTERRUPT (COMMENT)
8080	$\overline{MEMR}$	$\overline{MEMW}$	INTR (Thru RST Circuit)
8085	$\overline{RD}$	$\overline{WR}$	INTR (Thru RST Circuit)
Z-80	$\overline{RD}$	$\overline{WR}$	$\overline{INT}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•ϕ2•R/W	VMA•ϕ•$\overline{R/W}$	$\overline{IRQA}$ or $\overline{IRQB}$ (Thru PIA)

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APPLICATION INFORMATION FOR ALL ISD ChipCorder PRODUCTS

Address Segment Resolution

	Address Inputs											Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		1016A 1416 2532 2560	1110 1210 1020A 1420 2540 2575	1212 2548 2590	2564 25120	33060 33120	33075 33150	33090 33180	33120-4 33240
0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1	0 1	0.1	0.125	0.15	0.2	0.15	0.1875	0.225	0.3
2	0	0	0	0	0	0	0	0	1	0	0 2	0.2	0.25	0.3	0.4	0.3	0.375	0.45	0.6
3	0	0	0	0	0	0	0	0	1	1	0 3	0.3	0.375	0.45	0.6	0.45	0.5625	0.675	0.9
4	0	0	0	0	0	0	0	1	0	0	0 4	0.4	0.5	0.6	0.8	0.6	0.75	0.9	1.2
5	0	0	0	0	0	0	0	1	0	1	0 5	0.5	0.625	0.75	1	0.75	0.9375	1.125	1.5
6	0	0	0	0	0	0	0	1	1	0	0 6	0.6	0.75	0.9	1.2	0.9	1.125	1.35	1.8
7	0	0	0	0	0	0	0	1	1	1	0 7	0.7	0.875	1.05	1.4	1.05	1.3125	1.575	2.1
8	0	0	0	0	0	0	1	0	0	0	0 8	0.8	1	1.2	1.6	1.2	1.5	1.8	2.4
9	0	0	0	0	0	0	1	0	0	1	0 9	0.9	1.125	1.35	1.8	1.35	1.6875	2.025	2.7
10	0	0	0	0	0	0	1	0	1	0	0 A	1	1.25	1.5	2	1.5	1.875	2.25	3
11	0	0	0	0	0	0	1	0	1	1	0 B	1.1	1.375	1.65	2.2	1.65	2.0625	2.475	3.3
12	0	0	0	0	0	0	1	1	0	0	0 C	1.2	1.5	1.8	2.4	1.8	2.25	2.7	3.6
13	0	0	0	0	0	0	1	1	0	1	0 D	1.3	1.625	1.95	2.6	1.95	2.4375	2.925	3.9
14	0	0	0	0	0	0	1	1	1	0	0 E	1.4	1.75	2.1	2.8	2.1	2.625	3.15	4.2
15	0	0	0	0	0	0	1	1	1	1	0 F	1.5	1.875	2.25	3	2.25	2.8125	3.375	4.5
16	0	0	0	0	0	1	0	0	0	0	1 0	1.6	2	2.4	3.2	2.4	3	3.6	4.8
17	0	0	0	0	0	1	0	0	0	1	1 1	1.7	2.125	2.55	3.4	2.55	3.1875	3.825	5.1
18	0	0	0	0	0	1	0	0	1	0	1 2	1.8	2.25	2.7	3.6	2.7	3.375	4.05	5.4
19	0	0	0	0	0	1	0	0	1	1	1 3	1.9	2.375	2.85	3.8	2.85	3.5625	4.275	5.7
20	0	0	0	0	0	1	0	1	0	0	1 4	2	2.5	3	4	3	3.75	4.5	6
21	0	0	0	0	0	1	0	1	0	1	1 5	2.1	2.625	3.15	4.2	3.15	3.9375	4.725	6.3
22	0	0	0	0	0	1	0	1	1	0	1 6	2.2	2.75	3.3	4.4	3.3	4.125	4.95	6.6
23	0	0	0	0	0	1	0	1	1	1	1 7	2.3	2.875	3.45	4.6	3.45	4.3125	5.175	6.9

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs											1016A 1416 2532 2560	1110 1210 1020A 1420 2540 2575	1212 2548 2590	2564 25120	33060 33120	33075 33150	33090 33180	33120-4 33240
EC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0									
24	0	0	0	0	0	1	1	0	0	0	1 8	2.4	3	3.6	4.8	3.6	4.5	5.4	7.2
25	0	0	0	0	0	1	1	0	0	1	1 9	2.5	3.125	3.75	5	3.75	4.6875	5.625	7.5
26	0	0	0	0	0	1	1	0	1	0	1 A	2.6	3.25	3.9	5.2	3.9	4.875	5.85	7.8
27	0	0	0	0	0	1	1	0	1	1	1 B	2.7	3.375	4.05	5.4	4.05	5.0625	6.075	8.1
28	0	0	0	0	0	1	1	1	0	0	1 C	2.8	3.5	4.2	5.6	4.2	5.25	6.3	8.4
29	0	0	0	0	0	1	1	1	0	1	1 D	2.9	3.625	4.35	5.8	4.35	5.4375	6.525	8.7
30	0	0	0	0	0	1	1	1	1	0	1 E	3	3.75	4.5	6	4.5	5.625	6.75	9
31	0	0	0	0	0	1	1	1	1	1	1 F	3.1	3.875	4.65	6.2	4.65	5.8125	6.975	9.3
32	0	0	0	0	1	0	0	0	0	0	2 0	3.2	4	4.8	6.4	4.8	6	7.2	9.6
33	0	0	0	0	1	0	0	0	0	1	2 1	3.3	4.125	4.95	6.6	4.95	6.1875	7.425	9.9
34	0	0	0	0	1	0	0	0	1	0	2 2	3.4	4.25	5.1	6.8	5.1	6.375	7.65	10.2
35	0	0	0	0	1	0	0	0	1	1	2 3	3.5	4.375	5.25	7	5.25	6.5625	7.875	10.5
36	0	0	0	0	1	0	0	1	0	0	2 4	3.6	4.5	5.4	7.2	5.4	6.75	8.1	10.8
37	0	0	0	0	1	0	0	1	0	1	2 5	3.7	4.625	5.55	7.4	5.55	6.9375	8.325	11.1
38	0	0	0	0	1	0	0	1	1	0	2 6	3.8	4.75	5.7	7.6	5.7	7.125	8.55	11.4
39	0	0	0	0	1	0	0	1	1	1	2 7	3.9	4.875	5.85	7.8	5.85	7.3125	8.775	11.7
40	0	0	0	0	1	0	1	0	0	0	2 8	4	5	6	8	6	7.5	9	12
41	0	0	0	0	1	0	1	0	0	1	2 9	4.1	5.125	6.15	8.2	6.15	7.6875	9.225	12.3
42	0	0	0	0	1	0	1	0	1	0	2 A	4.2	5.25	6.3	8.4	6.3	7.875	9.45	12.6
43	0	0	0	0	1	0	1	0	1	1	2 B	4.3	5.375	6.45	8.6	6.45	8.0625	9.675	12.9
44	0	0	0	0	1	0	1	1	0	0	2 C	4.4	5.5	6.6	8.8	6.6	8.25	9.9	13.2
45	0	0	0	0	1	0	1	1	0	1	2 D	4.5	5.625	6.75	9	6.75	8.4375	10.125	13.5
46	0	0	0	0	1	0	1	1	1	0	2 E	4.6	5.75	6.9	9.2	6.9	8.625	10.35	13.8
47	0	0	0	0	1	0	1	1	1	1	2 F	4.7	5.875	7.05	9.4	7.05	8.8125	10.575	14.1
48	0	0	0	0	1	1	0	0	0	0	3 0	4.8	6	7.2	9.6	7.2	9	10.8	14.4
49	0	0	0	0	1	1	0	0	0	1	3 1	4.9	6.125	7.35	9.8	7.35	9.1875	11.025	14.7
50	0	0	0	0	1	1	0	0	1	0	3 2	5	6.25	7.5	10	7.5	9.375	11.25	15
51	0	0	0	0	1	1	0	0	1	1	3 3	5.1	6.375	7.65	10.2	7.65	9.5625	11.475	15.3
52	0	0	0	0	1	1	0	1	0	0	3 4	5.2	6.5	7.8	10.4	7.8	9.75	11.7	15.6
53	0	0	0	0	1	1	0	1	0	1	3 5	5.3	6.625	7.95	10.6	7.95	9.9375	11.925	15.9
54	0	0	0	0	1	1	0	1	1	0	3 6	5.4	6.75	8.1	10.8	8.1	10.125	12.15	16.2
55	0	0	0	0	1	1	0	1	1	1	3 7	5.5	6.875	8.25	11	8.25	10.3125	12.375	16.5
56	0	0	0	0	1	1	1	0	0	0	3 8	5.6	7	8.4	11.2	8.4	10.5	12.6	16.8
57	0	0	0	0	1	1	1	0	0	1	3 9	5.7	7.125	8.55	11.4	8.55	10.6875	12.825	17.1
58	0	0	0	0	1	1	1	0	1	0	3 A	5.8	7.25	8.7	11.6	8.7	10.875	13.05	17.4
59	0	0	0	0	1	1	1	0	1	1	3 B	5.9	7.375	8.85	11.8	8.85	11.0625	13.275	17.7
60	0	0	0	0	1	1	1	1	0	0	3 C	6	7.5	9	12	9	11.25	13.5	18

	Address Inputs											Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		1016A 1416 2532 2560	1110 1210 1020A 1420 2540 2575	1212 2548 2590	2564 25120	33060 33120	33075 33150	33090 33180	33120-4 33240
61	0	0	0	0	1	1	1	1	0	1	3 D	6.1	7.625	9.15	12.2	9.15	11.4375	13.725	18.3
62	0	0	0	0	1	1	1	1	1	0	3 E	6.2	7.75	9.3	12.4	9.3	11.625	13.95	18.6
63	0	0	0	0	1	1	1	1	1	1	3 F	6.3	7.875	9.45	12.6	9.45	11.8125	14.175	18.9
64	0	0	0	1	0	0	0	0	0	0	4 0	6.4	8	9.6	12.8	9.6	12	14.4	19.2
65	0	0	0	1	0	0	0	0	0	1	4 1	6.5	8.125	9.75	13	9.75	12.1875	14.625	19.5
66	0	0	0	1	0	0	0	0	1	0	4 2	6.6	8.25	9.9	13.2	9.9	12.375	14.85	19.8
67	0	0	0	1	0	0	0	0	1	1	4 3	6.7	8.375	10.05	13.4	10.05	12.5625	15.075	20.1
68	0	0	0	1	0	0	0	1	0	0	4 4	6.8	8.5	10.2	13.6	10.2	12.75	15.3	20.4
69	0	0	0	1	0	0	0	1	0	1	4 5	6.9	8.625	10.35	13.8	10.35	12.9375	15.525	20.7
70	0	0	0	1	0	0	0	1	1	0	4 6	7	8.75	10.5	14	10.5	13.125	15.75	21
71	0	0	0	1	0	0	0	1	1	1	4 7	7.1	8.875	10.65	14.2	10.65	13.3125	15.975	21.3
72	0	0	0	1	0	0	1	0	0	0	4 8	7.2	9	10.8	14.4	10.8	13.5	16.2	21.6
73	0	0	0	1	0	0	1	0	0	1	4 9	7.3	9.125	10.95	14.6	10.95	13.6875	16.425	21.9
74	0	0	0	1	0	0	1	0	1	0	4 A	7.4	9.25	11.1	14.8	11.1	13.875	16.65	22.2
75	0	0	0	1	0	0	1	0	1	1	4 B	7.5	9.375	11.25	15	11.25	14.0625	16.875	22.5
76	0	0	0	1	0	0	1	1	0	0	4 C	7.6	9.5	11.4	15.2	11.4	14.25	17.1	22.8
77	0	0	0	1	0	0	1	1	0	1	4 D	7.7	9.625	11.55	15.4	11.55	14.4375	17.325	23.1
78	0	0	0	1	0	0	1	1	1	0	4 E	7.8	9.75	11.7	15.6	11.7	14.625	17.55	23.4
79	0	0	0	1	0	0	1	1	1	1	4 F	7.9	9.875	11.85	15.8	11.85	14.8125	17.775	23.7

"End of Message Storage Space for ISD1110, ISD1210, and ISD1212 Devices"

EC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		Sample Rates: 8.0 KHz / ISD Part Numbers: 1016A 1416 2532 2560	6.4 KHz / 1020A 1420 2540 2575	5.3 KHz / 2548 2590	4.0 KHz / 2564 25120	8.0 KHz / 33060 33120	6.4 KHz / 33075 33150	5.3 KHz / 33090 33180	4.0 KHz / 33120-4 33240
80	0	0	0	1	0	1	0	0	0	0	5 0	8	10	12	16	12	15	18	24
81	0	0	0	1	0	1	0	0	0	1	5 1	8.1	10.125	12.15	16.2	12.15	15.1875	18.225	24.3
82	0	0	0	1	0	1	0	0	1	0	5 2	8.2	10.25	12.3	16.4	12.3	15.375	18.45	24.6
83	0	0	0	1	0	1	0	0	1	1	5 3	8.3	10.375	12.45	16.6	12.45	15.5625	18.675	24.9
84	0	0	0	1	0	1	0	1	0	0	5 4	8.4	10.5	12.6	16.8	12.6	15.75	18.9	25.2
85	0	0	0	1	0	1	0	1	0	1	5 5	8.5	10.625	12.75	17	12.75	15.9375	19.125	25.5
86	0	0	0	1	0	1	0	1	1	0	5 6	8.6	10.75	12.9	17.2	12.9	16.125	19.35	25.8
87	0	0	0	1	0	1	0	1	1	1	5 7	8.7	10.875	13.05	17.4	13.05	16.3125	19.575	26.1
88	0	0	0	1	0	1	1	0	0	0	5 8	8.8	11	13.2	17.6	13.2	16.5	19.8	26.4
89	0	0	0	1	0	1	1	0	0	1	5 9	8.9	11.125	13.35	17.8	13.35	16.6875	20.025	26.7
90	0	0	0	1	0	1	1	0	1	0	5 A	9	11.25	13.5	18	13.5	16.875	20.25	27
91	0	0	0	1	0	1	1	0	1	1	5 B	9.1	11.375	13.65	18.2	13.65	17.0625	20.475	27.3
92	0	0	0	1	0	1	1	1	0	0	5 C	9.2	11.5	13.8	18.4	13.8	17.25	20.7	27.6
93	0	0	0	1	0	1	1	1	0	1	5 D	9.3	11.625	13.95	18.6	13.95	17.4375	20.925	27.9
94	0	0	0	1	0	1	1	1	1	0	5 E	9.4	11.75	14.1	18.8	14.1	17.625	21.15	28.2
95	0	0	0	1	0	1	1	1	1	1	5 F	9.5	11.875	14.25	19	14.25	17.8125	21.375	28.5
96	0	0	0	1	1	0	0	0	0	0	6 0	9.6	12	14.4	19.2	14.4	18	21.6	28.8
97	0	0	0	1	1	0	0	0	0	1	6 1	9.7	12.125	14.55	19.4	14.55	18.1875	21.825	29.1
98	0	0	0	1	1	0	0	0	1	0	6 2	9.8	12.25	14.7	19.6	14.7	18.375	22.05	29.4
99	0	0	0	1	1	0	0	0	1	1	6 3	9.9	12.375	14.85	19.8	14.85	18.5625	22.275	29.7
100	0	0	0	1	1	0	0	1	0	0	6 4	10	12.5	15	20	15	18.75	22.5	30
101	0	0	0	1	1	0	0	1	0	1	6 5	10.1	12.625	15.15	20.2	15.15	18.9375	22.725	30.3
102	0	0	0	1	1	0	0	1	1	0	6 6	10.2	12.75	15.3	20.4	15.3	19.125	22.95	30.6
103	0	0	0	1	1	0	0	1	1	1	6 7	10.3	12.875	15.45	20.6	15.45	19.3125	23.175	30.9
104	0	0	0	1	1	0	1	0	0	0	6 8	10.4	13	15.6	20.8	15.6	19.5	23.4	31.2
105	0	0	0	1	1	0	1	0	0	1	6 9	10.5	13.125	15.75	21	15.75	19.6875	23.625	31.5
106	0	0	0	1	1	0	1	0	1	0	6 A	10.6	13.25	15.9	21.2	15.9	19.875	23.85	31.8
107	0	0	0	1	1	0	1	0	1	1	6 B	10.7	13.375	16.05	21.4	16.05	20.0625	24.075	32.1
108	0	0	0	1	1	0	1	1	0	0	6 C	10.8	13.5	16.2	21.6	16.2	20.25	24.3	32.4
109	0	0	0	1	1	0	1	1	0	1	6 D	10.9	13.625	16.35	21.8	16.35	20.4375	24.525	32.7
110	0	0	0	1	1	0	1	1	1	0	6 E	11	13.75	16.5	22	16.5	20.625	24.75	33
111	0	0	0	1	1	0	1	1	1	1	6 F	11.1	13.875	16.65	22.2	16.65	20.8125	24.975	33.3
112	0	0	0	1	1	1	0	0	0	0	7 0	11.2	14	16.8	22.4	16.8	21	25.2	33.6
113	0	0	0	1	1	1	0	0	0	1	7 1	11.3	14.125	16.95	22.6	16.95	21.1875	25.425	33.9
114	0	0	0	1	1	1	0	0	1	0	7 2	11.4	14.25	17.1	22.8	17.1	21.375	25.65	34.2
115	0	0	0	1	1	1	0	0	1	1	7 3	11.5	14.375	17.25	23	17.25	21.5625	25.875	34.5
116	0	0	0	1	1	1	0	1	0	0	7 4	11.6	14.5	17.4	23.2	17.4	21.75	26.1	34.8

	Address Inputs											Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
												1016A 1416 2532 2560	1020A 1420 2540 2575	2548 2590	2564 25120	33060 33120	33075 33150	33090 33180	33120-4 33240
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0									
117	0	0	0	1	1	1	0	1	0	1	7 5	11.7	14.625	17.55	23.4	17.55	21.9375	26.325	35.1
118	0	0	0	1	1	1	0	1	1	0	7 6	11.8	14.75	17.7	23.6	17.7	22.125	26.55	35.4
119	0	0	0	1	1	1	0	1	1	1	7 7	11.9	14.875	17.85	23.8	17.85	22.3125	26.775	35.7
120	0	0	0	1	1	1	1	0	0	0	7 8	12	15	18	24	18	22.5	27	36
121	0	0	0	1	1	1	1	0	0	1	7 9	12.1	15.125	18.15	24.2	18.15	22.6875	27.225	36.3
122	0	0	0	1	1	1	1	0	1	0	7 A	12.2	15.25	18.3	24.4	18.3	22.875	27.45	36.6
123	0	0	0	1	1	1	1	0	1	1	7 B	12.3	15.375	18.45	24.6	18.45	23.0625	27.675	36.9
124	0	0	0	1	1	1	1	1	0	0	7 C	12.4	15.5	18.6	24.8	18.6	23.25	27.9	37.2
125	0	0	0	1	1	1	1	1	0	1	7 D	12.5	15.625	18.75	25	18.75	23.4375	28.125	37.5
126	0	0	0	1	1	1	1	1	1	0	7 E	12.6	15.75	18.9	25.2	18.9	23.625	28.35	37.8
127	0	0	0	1	1	1	1	1	1	1	7 F	12.7	15.875	19.05	25.4	19.05	23.8125	28.575	38.1
128	0	0	1	0	0	0	0	0	0	0	8 0	12.8	16	19.2	25.6	19.2	24	28.8	38.4
129	0	0	1	0	0	0	0	0	0	1	8 1	12.9	16.125	19.35	25.8	19.35	24.1875	29.025	38.7
130	0	0	1	0	0	0	0	0	1	0	8 2	13	16.25	19.5	26	19.5	24.375	29.25	39
131	0	0	1	0	0	0	0	0	1	1	8 3	13.1	16.375	19.65	26.2	19.65	24.5625	29.475	39.3
132	0	0	1	0	0	0	0	1	0	0	8 4	13.2	16.5	19.8	26.4	19.8	24.75	29.7	39.6
133	0	0	1	0	0	0	0	1	0	1	8 5	13.3	16.625	19.95	26.6	19.95	24.9375	29.925	39.9
134	0	0	1	0	0	0	0	1	1	0	8 6	13.4	16.75	20.1	26.8	20.1	25.125	30.15	40.2
135	0	0	1	0	0	0	0	1	1	1	8 7	13.5	16.875	20.25	27	20.25	25.3125	30.375	40.5
136	0	0	1	0	0	0	1	0	0	0	8 8	13.6	17	20.4	27.2	20.4	25.5	30.6	40.8
137	0	0	1	0	0	0	1	0	0	1	8 9	13.7	17.125	20.55	27.4	20.55	25.6875	30.825	41.1
138	0	0	1	0	0	0	1	0	1	0	8 A	13.8	17.25	20.7	27.6	20.7	25.875	31.05	41.4
139	0	0	1	0	0	0	1	0	1	1	8 B	13.9	17.375	20.85	27.8	20.85	26.0625	31.275	41.7
140	0	0	1	0	0	0	1	1	0	0	8 C	14	17.5	21	28	21	26.25	31.5	42
141	0	0	1	0	0	0	1	1	0	1	8 D	14.1	17.625	21.15	28.2	21.15	26.4375	31.725	42.3
142	0	0	1	0	0	0	1	1	1	0	8 E	14.2	17.75	21.3	28.4	21.3	26.625	31.95	42.6
143	0	0	1	0	0	0	1	1	1	1	8 F	14.3	17.875	21.45	28.6	21.45	26.8125	32.175	42.9
144	0	0	1	0	0	1	0	0	0	0	9 0	14.4	18	21.6	28.8	21.6	27	32.4	43.2
145	0	0	1	0	0	1	0	0	0	1	9 1	14.5	18.125	21.75	29	21.75	27.1875	32.625	43.5
146	0	0	1	0	0	1	0	0	1	0	9 2	14.6	18.25	21.9	29.2	21.9	27.375	32.85	43.8
147	0	0	1	0	0	1	0	0	1	1	9 3	14.7	18.375	22.05	29.4	22.05	27.5625	33.075	44.1
148	0	0	1	0	0	1	0	1	0	0	9 4	14.8	18.5	22.2	29.6	22.2	27.75	33.3	44.4
149	0	0	1	0	0	1	0	1	0	1	9 5	14.9	18.625	22.35	29.8	22.35	27.9375	33.525	44.7
150	0	0	1	0	0	1	0	1	1	0	9 6	15	18.75	22.5	30	22.5	28.125	33.75	45
151	0	0	1	0	0	1	0	1	1	1	9 7	15.1	18.875	22.65	30.2	22.65	28.3125	33.975	45.3
152	0	0	1	0	0	1	1	0	0	0	9 8	15.2	19	22.8	30.4	22.8	28.5	34.2	45.6
153	0	0	1	0	0	1	1	0	0	1	9 9	15.3	19.125	22.95	30.6	22.95	28.6875	34.425	45.9

											Sample Rates							
											8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
											ISD Part Numbers							
	Address Inputs										1016A 1416 2532 2560	1020A 1420 2540 2575	2548 2590	2564 25120	33060 33120	33075 33150	33090 33180	33120-4 33240
EC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0								
54	0	0	1	0	0	1	1	0	1	0	9 A	15.4	19.25	23.1	30.8	23.1	28.875	34.65	46.2
55	0	0	1	0	0	1	1	0	1	1	9 B	15.5	19.375	23.25	31	23.25	29.0625	34.875	46.5
56	0	0	1	0	0	1	1	1	0	0	9 C	15.6	19.5	23.4	31.2	23.4	29.25	35.1	46.8
57	0	0	1	0	0	1	1	1	0	1	9 D	15.7	19.625	23.55	31.4	23.55	29.4375	35.325	47.1
58	0	0	1	0	0	1	1	1	1	0	9 E	15.8	19.75	23.7	31.6	23.7	29.625	35.55	47.4
59	0	0	1	0	0	1	1	1	1	1	9 F	15.9	19.875	23.85	31.8	23.85	29.8125	35.775	47.7

"End of Message Storage Space for ISD1416, ISD1420, ISD1016A, and ISD1020A Devices"

											Sample Rates							
											8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
											ISD Part Numbers							
	Address Inputs										2532 2560	2540 2575	2548 2590	2564 25120	33060 33120	33075 33150	33090 33180	33120-4 33240
EC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0								
160	0	0	1	0	1	0	0	0	0	0	A 0	16	20	24	32	24	30	36	48
161	0	0	1	0	1	0	0	0	0	1	A 1	16.1	20.125	24.15	32.2	24.15	30.1875	36.225	48.3
162	0	0	1	0	1	0	0	0	1	0	A 2	16.2	20.25	24.3	32.4	24.3	30.375	36.45	48.6
163	0	0	1	0	1	0	0	0	1	1	A 3	16.3	20.375	24.45	32.6	24.45	30.5625	36.675	48.9
164	0	0	1	0	1	0	0	1	0	0	A 4	16.4	20.5	24.6	32.8	24.6	30.75	36.9	49.2
165	0	0	1	0	1	0	0	1	0	1	A 5	16.5	20.625	24.75	33	24.75	30.9375	37.125	49.5
166	0	0	1	0	1	0	0	1	1	0	A 6	16.6	20.75	24.9	33.2	24.9	31.125	37.35	49.8
167	0	0	1	0	1	0	0	1	1	1	A 7	16.7	20.875	25.05	33.4	25.05	31.3125	37.575	50.1
168	0	0	1	0	1	0	1	0	0	0	A 8	16.8	21	25.2	33.6	25.2	31.5	37.8	50.4
169	0	0	1	0	1	0	1	0	0	1	A 9	16.9	21.125	25.35	33.8	25.35	31.6875	38.025	50.7
170	0	0	1	0	1	0	1	0	1	0	A A	17	21.25	25.5	34	25.5	31.875	38.25	51
171	0	0	1	0	1	0	1	0	1	1	A B	17.1	21.375	25.65	34.2	25.65	32.0625	38.475	51.3
172	0	0	1	0	1	0	1	1	0	0	A C	17.2	21.5	25.8	34.4	25.8	32.25	38.7	51.6
173	0	0	1	0	1	0	1	1	0	1	A D	17.3	21.625	25.95	34.6	25.95	32.4375	38.925	51.9
174	0	0	1	0	1	0	1	1	1	0	A E	17.4	21.75	26.1	34.8	26.1	32.625	39.15	52.2
175	0	0	1	0	1	0	1	1	1	1	A F	17.5	21.875	26.25	35	26.25	32.8125	39.375	52.5
176	0	0	1	0	1	1	0	0	0	0	B 0	17.6	22	26.4	35.2	26.4	33	39.6	52.8
177	0	0	1	0	1	1	0	0	0	1	B 1	17.7	22.125	26.55	35.4	26.55	33.1875	39.825	53.1
178	0	0	1	0	1	1	0	0	1	0	B 2	17.8	22.25	26.7	35.6	26.7	33.375	40.05	53.4
179	0	0	1	0	1	1	0	0	1	1	B 3	17.9	22.375	26.85	35.8	26.85	33.5625	40.275	53.7
180	0	0	1	0	1	1	0	1	0	0	B 4	18	22.5	27	36	27	33.75	40.5	54
181	0	0	1	0	1	1	0	1	0	1	B 5	18.1	22.625	27.15	36.2	27.15	33.9375	40.725	54.3

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs											2532	2540	2548	2564	33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
182	0	0	1	0	1	1	0	1	1	0	B 6	18.2	22.75	27.3	36.4	27.3	34.125	40.95	54.6
183	0	0	1	0	1	1	0	1	1	1	B 7	18.3	22.875	27.45	36.6	27.45	34.3125	41.175	54.9
184	0	0	1	0	1	1	1	0	0	0	B 8	18.4	23	27.6	36.8	27.6	34.5	41.4	55.2
185	0	0	1	0	1	1	1	0	0	1	B 9	18.5	23.125	27.75	37	27.75	34.6875	41.625	55.5
186	0	0	1	0	1	1	1	0	1	0	B A	18.6	23.25	27.9	37.2	27.9	34.875	41.85	55.8
187	0	0	1	0	1	1	1	0	1	1	B B	18.7	23.375	28.05	37.4	28.05	35.0625	42.075	56.1
188	0	0	1	0	1	1	1	1	0	0	B C	18.8	23.5	28.2	37.6	28.2	35.25	42.3	56.4
189	0	0	1	0	1	1	1	1	0	1	B D	18.9	23.625	28.35	37.8	28.35	35.4375	42.525	56.7
190	0	0	1	0	1	1	1	1	1	0	B E	19	23.75	28.5	38	28.5	35.625	42.75	57
191	0	0	1	0	1	1	1	1	1	1	B F	19.1	23.875	28.65	38.2	28.65	35.8125	42.975	57.3
192	0	0	1	1	0	0	0	0	0	0	C 0	19.2	24	28.8	38.4	28.8	36	43.2	57.6
193	0	0	1	1	0	0	0	0	0	1	C 1	19.3	24.125	28.95	38.6	28.95	36.1875	43.425	57.9
194	0	0	1	1	0	0	0	0	1	0	C 2	19.4	24.25	29.1	38.8	29.1	36.375	43.65	58.2
195	0	0	1	1	0	0	0	0	1	1	C 3	19.5	24.375	29.25	39	29.25	36.5625	43.875	58.5
196	0	0	1	1	0	0	0	1	0	0	C 4	19.6	24.5	29.4	39.2	29.4	36.75	44.1	58.8
197	0	0	1	1	0	0	0	1	0	1	C 5	19.7	24.625	29.55	39.4	29.55	36.9375	44.325	59.1
198	0	0	1	1	0	0	0	1	1	0	C 6	19.8	24.75	29.7	39.6	29.7	37.125	44.55	59.4
199	0	0	1	1	0	0	0	1	1	1	C 7	19.9	24.875	29.85	39.8	29.85	37.3125	44.775	59.7
200	0	0	1	1	0	0	1	0	0	0	C 8	20	25	30	40	30	37.5	45	60
201	0	0	1	1	0	0	1	0	0	1	C 9	20.1	25.125	30.15	40.2	30.15	37.6875	45.225	60.3
202	0	0	1	1	0	0	1	0	1	0	C A	20.2	25.25	30.3	40.4	30.3	37.875	45.45	60.6
203	0	0	1	1	0	0	1	0	1	1	C B	20.3	25.375	30.45	40.6	30.45	38.0625	45.675	60.9
204	0	0	1	1	0	0	1	1	0	0	C C	20.4	25.5	30.6	40.8	30.6	38.25	45.9	61.2
205	0	0	1	1	0	0	1	1	0	1	C D	20.5	25.625	30.75	41	30.75	38.4375	46.125	61.5
206	0	0	1	1	0	0	1	1	1	0	C E	20.6	25.75	30.9	41.2	30.9	38.625	46.35	61.8
207	0	0	1	1	0	0	1	1	1	1	C F	20.7	25.875	31.05	41.4	31.05	38.8125	46.575	62.1
208	0	0	1	1	0	1	0	0	0	0	D 0	20.8	26	31.2	41.6	31.2	39	46.8	62.4
209	0	0	1	1	0	1	0	0	0	1	D 1	20.9	26.125	31.35	41.8	31.35	39.1875	47.025	62.7
210	0	0	1	1	0	1	0	0	1	0	D 2	21	26.25	31.5	42	31.5	39.375	47.25	63
211	0	0	1	1	0	1	0	0	1	1	D 3	21.1	26.375	31.65	42.2	31.65	39.5625	47.475	63.3
212	0	0	1	1	0	1	0	1	0	0	D 4	21.2	26.5	31.8	42.4	31.8	39.75	47.7	63.6
213	0	0	1	1	0	1	0	1	0	1	D 5	21.3	26.625	31.95	42.6	31.95	39.9375	47.925	63.9
214	0	0	1	1	0	1	0	1	1	0	D 6	21.4	26.75	32.1	42.8	32.1	40.125	48.15	64.2
215	0	0	1	1	0	1	0	1	1	1	D 7	21.5	26.875	32.25	43	32.25	40.3125	48.375	64.5
216	0	0	1	1	0	1	1	0	0	0	D 8	21.6	27	32.4	43.2	32.4	40.5	48.6	64.8
217	0	0	1	1	0	1	1	0	0	1	D 9	21.7	27.125	32.55	43.4	32.55	40.6875	48.825	65.1
218	0	0	1	1	0	1	1	0	1	0	D A	21.8	27.25	32.7	43.6	32.7	40.875	49.05	65.4
219	0	0	1	1	0	1	1	0	1	1	D B	21.9	27.375	32.85	43.8	32.85	41.0625	49.275	65.7
220	0	0	1	1	0	1	1	1	0	0	D C	22	27.5	33	44	33	41.25	49.5	66

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs											2532	2540	2548	2564	33060	33075	33090	33120-4
EC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
221	0	0	1	1	0	1	1	1	0	1	D D	22.1	27.625	33.15	44.2	33.15	41.4375	49.725	66.3
222	0	0	1	1	0	1	1	1	1	0	D E	22.2	27.75	33.3	44.4	33.3	41.625	49.95	66.6
223	0	0	1	1	0	1	1	1	1	1	D F	22.3	27.875	33.45	44.6	33.45	41.8125	50.175	66.9
224	0	0	1	1	1	0	0	0	0	0	E 0	22.4	28	33.6	44.8	33.6	42	50.4	67.2
225	0	0	1	1	1	0	0	0	0	1	E 1	22.5	28.125	33.75	45	33.75	42.1875	50.625	67.5
226	0	0	1	1	1	0	0	0	1	0	E 2	22.6	28.25	33.9	45.2	33.9	42.375	50.85	67.8
227	0	0	1	1	1	0	0	0	1	1	E 3	22.7	28.375	34.05	45.4	34.05	42.5625	51.075	68.1
228	0	0	1	1	1	0	0	1	0	0	E 4	22.8	28.5	34.2	45.6	34.2	42.75	51.3	68.4
229	0	0	1	1	1	0	0	1	0	1	E 5	22.9	28.625	34.35	45.8	34.35	42.9375	51.525	68.7
230	0	0	1	1	1	0	0	1	1	0	E 6	23	28.75	34.5	46	34.5	43.125	51.75	69
231	0	0	1	1	1	0	0	1	1	1	E 7	23.1	28.875	34.65	46.2	34.65	43.3125	51.975	69.3
232	0	0	1	1	1	0	1	0	0	0	E 8	23.2	29	34.8	46.4	34.8	43.5	52.2	69.6
233	0	0	1	1	1	0	1	0	0	1	E 9	23.3	29.125	34.95	46.6	34.95	43.6875	52.425	69.9
234	0	0	1	1	1	0	1	0	1	0	E A	23.4	29.25	35.1	46.8	35.1	43.875	52.65	70.2
235	0	0	1	1	1	0	1	0	1	1	E B	23.5	29.375	35.25	47	35.25	44.0625	52.875	70.5
236	0	0	1	1	1	0	1	1	0	0	E C	23.6	29.5	35.4	47.2	35.4	44.25	53.1	70.8
237	0	0	1	1	1	0	1	1	0	1	E D	23.7	29.625	35.55	47.4	35.55	44.4375	53.325	71.1
238	0	0	1	1	1	0	1	1	1	0	E E	23.8	29.75	35.7	47.6	35.7	44.625	53.55	71.4
239	0	0	1	1	1	0	1	1	1	1	E F	23.9	29.875	35.85	47.8	35.85	44.8125	53.775	71.7
240	0	0	1	1	1	1	0	0	0	0	F 0	24	30	36	48	36	45	54	72
241	0	0	1	1	1	1	0	0	0	1	F 1	24.1	30.125	36.15	48.2	36.15	45.1875	54.225	72.3
242	0	0	1	1	1	1	0	0	1	0	F 2	24.2	30.25	36.3	48.4	36.3	45.375	54.45	72.6
243	0	0	1	1	1	1	0	0	1	1	F 3	24.3	30.375	36.45	48.6	36.45	45.5625	54.675	72.9
244	0	0	1	1	1	1	0	1	0	0	F 4	24.4	30.5	36.6	48.8	36.6	45.75	54.9	73.2
245	0	0	1	1	1	1	0	1	0	1	F 5	24.5	30.625	36.75	49	36.75	45.9375	55.125	73.5
246	0	0	1	1	1	1	0	1	1	0	F 6	24.6	30.75	36.9	49.2	36.9	46.125	55.35	73.8
247	0	0	1	1	1	1	0	1	1	1	F 7	24.7	30.875	37.05	49.4	37.05	46.3125	55.575	74.1
248	0	0	1	1	1	1	1	0	0	0	F 8	24.8	31	37.2	49.6	37.2	46.5	55.8	74.4
249	0	0	1	1	1	1	1	0	0	1	F 9	24.9	31.125	37.35	49.8	37.35	46.6875	56.025	74.7
250	0	0	1	1	1	1	1	0	1	0	F A	25	31.25	37.5	50	37.5	46.875	56.25	75
251	0	0	1	1	1	1	1	0	1	1	F B	25.1	31.375	37.65	50.2	37.65	47.0625	56.475	75.3
252	0	0	1	1	1	1	1	1	0	0	F C	25.2	31.5	37.8	50.4	37.8	47.25	56.7	75.6
253	0	0	1	1	1	1	1	1	0	1	F D	25.3	31.625	37.95	50.6	37.95	47.4375	56.925	75.9
254	0	0	1	1	1	1	1	1	1	0	F E	25.4	31.75	38.1	50.8	38.1	47.625	57.15	76.2
255	0	0	1	1	1	1	1	1	1	1	F F	25.5	31.875	38.25	51	38.25	47.8125	57.375	76.5
256	0	1	0	0	0	0	0	0	0	0	10 0	25.6	32	38.4	51.2	38.4	48	57.6	76.8
257	0	1	0	0	0	0	0	0	0	1	10 1	25.7	32.125	38.55	51.4	38.55	48.1875	57.825	77.1
258	0	1	0	0	0	0	0	0	1	0	10 2	25.8	32.25	38.7	51.6	38.7	48.375	58.05	77.4
259	0	1	0	0	0	0	0	0	1	1	10 3	25.9	32.375	38.85	51.8	38.85	48.5625	58.275	77.7

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs											2532 2560	2540 2575	2548 2590	2564 25120	33060 33120	33075 33150	33090 33180	33120-4 33240
EC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0									
299	0	1	0	0	1	0	1	0	1	1	12 B	29.9	37.375	44.85	59.8	44.85	56.0625	67.275	89.7
300	0	1	0	0	1	0	1	1	0	0	12 C	30	37.5	45	60	45	56.25	67.5	90
301	0	1	0	0	1	0	1	1	0	1	12 D	30.1	37.625	45.15	60.2	45.15	56.4375	67.725	90.3
302	0	1	0	0	1	0	1	1	1	0	12 E	30.2	37.75	45.3	60.4	45.3	56.625	67.95	90.6
303	0	1	0	0	1	0	1	1	1	1	12 F	30.3	37.875	45.45	60.6	45.45	56.8125	68.175	90.9
304	0	1	0	0	1	1	0	0	0	0	13 0	30.4	38	45.6	60.8	45.6	57	68.4	91.2
305	0	1	0	0	1	1	0	0	0	1	13 1	30.5	38.125	45.75	61	45.75	57.1875	68.625	91.5
306	0	1	0	0	1	1	0	0	1	0	13 2	30.6	38.25	45.9	61.2	45.9	57.375	68.85	91.8
307	0	1	0	0	1	1	0	0	1	1	13 3	30.7	38.375	46.05	61.4	46.05	57.5625	69.075	92.1
308	0	1	0	0	1	1	0	1	0	0	13 4	30.8	38.5	46.2	61.6	46.2	57.75	69.3	92.4
309	0	1	0	0	1	1	0	1	0	1	13 5	30.9	38.625	46.35	61.8	46.35	57.9375	69.525	92.7
310	0	1	0	0	1	1	0	1	1	0	13 6	31	38.75	46.5	62	46.5	58.125	69.75	93
311	0	1	0	0	1	1	0	1	1	1	13 7	31.1	38.875	46.65	62.2	46.65	58.3125	69.975	93.3
312	0	1	0	0	1	1	1	0	0	0	13 8	31.2	39	46.8	62.4	46.8	58.5	70.2	93.6
313	0	1	0	0	1	1	1	0	0	1	13 9	31.3	39.125	46.95	62.6	46.95	58.6875	70.425	93.9
314	0	1	0	0	1	1	1	0	1	0	13 A	31.4	39.25	47.1	62.8	47.1	58.875	70.65	94.2
315	0	1	0	0	1	1	1	0	1	1	13 B	31.5	39.375	47.25	63	47.25	59.0625	70.875	94.5
316	0	1	0	0	1	1	1	1	0	0	13 C	31.6	39.5	47.4	63.2	47.4	59.25	71.1	94.8
317	0	1	0	0	1	1	1	1	0	1	13 D	31.7	39.625	47.55	63.4	47.55	59.4375	71.325	95.1
318	0	1	0	0	1	1	1	1	1	0	13 E	31.8	39.75	47.7	63.6	47.7	59.625	71.55	95.4
319	0	1	0	0	1	1	1	1	1	1	13 F	31.9	39.875	47.85	63.8	47.85	59.8125	71.775	95.7
"End of Message Storage Space for ISD2532, ISD2540, ISD2548, and ISD2564 Devices"																			

												Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs															33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
320	0	1	0	1	0	0	0	0	0	0	14 0	32	40	48	64	48	60	72	96
321	0	1	0	1	0	0	0	0	0	1	14 1	32.1	40.125	48.15	64.2	48.15	60.1875	72.225	96.3
322	0	1	0	1	0	0	0	0	1	0	14 2	32.2	40.25	48.3	64.4	48.3	60.375	72.45	96.6
323	0	1	0	1	0	0	0	0	1	1	14 3	32.3	40.375	48.45	64.6	48.45	60.5625	72.675	96.9
324	0	1	0	1	0	0	0	1	0	0	14 4	32.4	40.5	48.6	64.8	48.6	60.75	72.9	97.2
325	0	1	0	1	0	0	0	1	0	1	14 5	32.5	40.625	48.75	65	48.75	60.9375	73.125	97.5
326	0	1	0	1	0	0	0	1	1	0	14 6	32.6	40.75	48.9	65.2	48.9	61.125	73.35	97.8
327	0	1	0	1	0	0	0	1	1	1	14 7	32.7	40.875	49.05	65.4	49.05	61.3125	73.575	98.1

	Address Inputs											Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
																33060	33075	33090	33120-4
EC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
366	0	1	0	1	1	0	1	1	1	0	16 E	36.6	45.75	54.9	73.2	54.9	68.625	82.35	109.8
367	0	1	0	1	1	0	1	1	1	1	16 F	36.7	45.875	55.05	73.4	55.05	68.8125	82.575	110.1
368	0	1	0	1	1	1	0	0	0	0	17 0	36.8	46	55.2	73.6	55.2	69	82.8	110.4
369	0	1	0	1	1	1	0	0	0	1	17 1	36.9	46.125	55.35	73.8	55.35	69.1875	83.025	110.7
370	0	1	0	1	1	1	0	0	1	0	17 2	37	46.25	55.5	74	55.5	69.375	83.25	111
371	0	1	0	1	1	1	0	0	1	1	17 3	37.1	46.375	55.65	74.2	55.65	69.5625	83.475	111.3
372	0	1	0	1	1	1	0	1	0	0	17 4	37.2	46.5	55.8	74.4	55.8	69.75	83.7	111.6
373	0	1	0	1	1	1	0	1	0	1	17 5	37.3	46.625	55.95	74.6	55.95	69.9375	83.925	111.9
374	0	1	0	1	1	1	0	1	1	0	17 6	37.4	46.75	56.1	74.8	56.1	70.125	84.15	112.2
375	0	1	0	1	1	1	0	1	1	1	17 7	37.5	46.875	56.25	75	56.25	70.3125	84.375	112.5
376	0	1	0	1	1	1	1	0	0	0	17 8	37.6	47	56.4	75.2	56.4	70.5	84.6	112.8
377	0	1	0	1	1	1	1	0	0	1	17 9	37.7	47.125	56.55	75.4	56.55	70.6875	84.825	113.1
378	0	1	0	1	1	1	1	0	1	0	17 A	37.8	47.25	56.7	75.6	56.7	70.875	85.05	113.4
379	0	1	0	1	1	1	1	0	1	1	17 B	37.9	47.375	56.85	75.8	56.85	71.0625	85.275	113.7
380	0	1	0	1	1	1	1	1	0	0	17 C	38	47.5	57	76	57	71.25	85.5	114
381	0	1	0	1	1	1	1	1	0	1	17 D	38.1	47.625	57.15	76.2	57.15	71.4375	85.725	114.3
382	0	1	0	1	1	1	1	1	1	0	17 E	38.2	47.75	57.3	76.4	57.3	71.625	85.95	114.6
383	0	1	0	1	1	1	1	1	1	1	17 F	38.3	47.875	57.45	76.6	57.45	71.8125	86.175	114.9
384	0	1	1	0	0	0	0	0	0	0	18 0	38.4	48	57.6	76.8	57.6	72	86.4	115.2
385	0	1	1	0	0	0	0	0	0	1	18 1	38.5	48.125	57.75	77	57.75	72.1875	86.625	115.5
386	0	1	1	0	0	0	0	0	1	0	18 2	38.6	48.25	57.9	77.2	57.9	72.375	86.85	115.8
387	0	1	1	0	0	0	0	0	1	1	18 3	38.7	48.375	58.05	77.4	58.05	72.5625	87.075	116.1
388	0	1	1	0	0	0	0	1	0	0	18 4	38.8	48.5	58.2	77.6	58.2	72.75	87.3	116.4
389	0	1	1	0	0	0	0	1	0	1	18 5	38.9	48.625	58.35	77.8	58.35	72.9375	87.525	116.7
390	0	1	1	0	0	0	0	1	1	0	18 6	39	48.75	58.5	78	58.5	73.125	87.75	117
391	0	1	1	0	0	0	0	1	1	1	18 7	39.1	48.875	58.65	78.2	58.65	73.3125	87.975	117.3
392	0	1	1	0	0	0	1	0	0	0	18 8	39.2	49	58.8	78.4	58.8	73.5	88.2	117.6
393	0	1	1	0	0	0	1	0	0	1	18 9	39.3	49.125	58.95	78.6	58.95	73.6875	88.425	117.9
394	0	1	1	0	0	0	1	0	1	0	18 A	39.4	49.25	59.1	78.8	59.1	73.875	88.65	118.2
395	0	1	1	0	0	0	1	0	1	1	18 B	39.5	49.375	59.25	79	59.25	74.0625	88.875	118.5
396	0	1	1	0	0	0	1	1	0	0	18 C	39.6	49.5	59.4	79.2	59.4	74.25	89.1	118.8
397	0	1	1	0	0	0	1	1	0	1	18 D	39.7	49.625	59.55	79.4	59.55	74.4375	89.325	119.1
398	0	1	1	0	0	0	1	1	1	0	18 E	39.8	49.75	59.7	79.6	59.7	74.625	89.55	119.4
399	0	1	1	0	0	0	1	1	1	1	18 F	39.9	49.875	59.85	79.8	59.85	74.8125	89.775	119.7

"End of Message Storage Space for ISD33060, ISD33075, ISD33090, and ISD33120-4 Devices"

												Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs															33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
400	0	1	1	0	0	1	0	0	0	0	19 0	40	50	60	80	60	75	90	120
401	0	1	1	0	0	1	0	0	0	1	19 1	40.1	50.125	60.15	80.2	60.15	75.1875	90.225	120.3
402	0	1	1	0	0	1	0	0	1	0	19 2	40.2	50.25	60.3	80.4	60.3	75.375	90.45	120.6
403	0	1	1	0	0	1	0	0	1	1	19 3	40.3	50.375	60.45	80.6	60.45	75.5625	90.675	120.9
404	0	1	1	0	0	1	0	1	0	0	19 4	40.4	50.5	60.6	80.8	60.6	75.75	90.9	121.2
405	0	1	1	0	0	1	0	1	0	1	19 5	40.5	50.625	60.75	81	60.75	75.9375	91.125	121.5
406	0	1	1	0	0	1	0	1	1	0	19 6	40.6	50.75	60.9	81.2	60.9	76.125	91.35	121.8
407	0	1	1	0	0	1	0	1	1	1	19 7	40.7	50.875	61.05	81.4	61.05	76.3125	91.575	122.1
408	0	1	1	0	0	1	1	0	0	0	19 8	40.8	51	61.2	81.6	61.2	76.5	91.8	122.4
409	0	1	1	0	0	1	1	0	0	1	19 9	40.9	51.125	61.35	81.8	61.35	76.6875	92.025	122.7
410	0	1	1	0	0	1	1	0	1	0	19 A	41	51.25	61.5	82	61.5	76.875	92.25	123
411	0	1	1	0	0	1	1	0	1	1	19 B	41.1	51.375	61.65	82.2	61.65	77.0625	92.475	123.3
412	0	1	1	0	0	1	1	1	0	0	19 C	41.2	51.5	61.8	82.4	61.8	77.25	92.7	123.6
413	0	1	1	0	0	1	1	1	0	1	19 D	41.3	51.625	61.95	82.6	61.95	77.4375	92.925	123.9
414	0	1	1	0	0	1	1	1	1	0	19 E	41.4	51.75	62.1	82.8	62.1	77.625	93.15	124.2
415	0	1	1	0	0	1	1	1	1	1	19 F	41.5	51.875	62.25	83	62.25	77.8125	93.375	124.5
416	0	1	1	0	1	0	0	0	0	0	1A 0	41.6	52	62.4	83.2	62.4	78	93.6	124.8
417	0	1	1	0	1	0	0	0	0	1	1A 1	41.7	52.125	62.55	83.4	62.55	78.1875	93.825	125.1
418	0	1	1	0	1	0	0	0	1	0	1A 2	41.8	52.25	62.7	83.6	62.7	78.375	94.05	125.4
419	0	1	1	0	1	0	0	0	1	1	1A 3	41.9	52.375	62.85	83.8	62.85	78.5625	94.275	125.7
420	0	1	1	0	1	0	0	1	0	0	1A 4	42	52.5	63	84	63	78.75	94.5	126
421	0	1	1	0	1	0	0	1	0	1	1A 5	42.1	52.625	63.15	84.2	63.15	78.9375	94.725	126.3
422	0	1	1	0	1	0	0	1	1	0	1A 6	42.2	52.75	63.3	84.4	63.3	79.125	94.95	126.6
423	0	1	1	0	1	0	0	1	1	1	1A 7	42.3	52.875	63.45	84.6	63.45	79.3125	95.175	126.9
424	0	1	1	0	1	0	1	0	0	0	1A 8	42.4	53	63.6	84.8	63.6	79.5	95.4	127.2
425	0	1	1	0	1	0	1	0	0	1	1A 9	42.5	53.125	63.75	85	63.75	79.6875	95.625	127.5
426	0	1	1	0	1	0	1	0	1	0	1A A	42.6	53.25	63.9	85.2	63.9	79.875	95.85	127.8
427	0	1	1	0	1	0	1	0	1	1	1A B	42.7	53.375	64.05	85.4	64.05	80.0625	96.075	128.1
428	0	1	1	0	1	0	1	1	0	0	1A C	42.8	53.5	64.2	85.6	64.2	80.25	96.3	128.4
429	0	1	1	0	1	0	1	1	0	1	1A D	42.9	53.625	64.35	85.8	64.35	80.4375	96.525	128.7
430	0	1	1	0	1	0	1	1	1	0	1A E	43	53.75	64.5	86	64.5	80.625	96.75	129
431	0	1	1	0	1	0	1	1	1	1	1A F	43.1	53.875	64.65	86.2	64.65	80.8125	96.975	129.3
432	0	1	1	0	1	1	0	0	0	0	1B 0	43.2	54	64.8	86.4	64.8	81	97.2	129.6
433	0	1	1	0	1	1	0	0	0	1	1B 1	43.3	54.125	64.95	86.6	64.95	81.1875	97.425	129.9
434	0	1	1	0	1	1	0	0	1	0	1B 2	43.4	54.25	65.1	86.8	65.1	81.375	97.65	130.2
435	0	1	1	0	1	1	0	0	1	1	1B 3	43.5	54.375	65.25	87	65.25	81.5625	97.875	130.5
436	0	1	1	0	1	1	0	1	0	0	1B 4	43.6	54.5	65.4	87.2	65.4	81.75	98.1	130.8
437	0	1	1	0	1	1	0	1	0	1	1B 5	43.7	54.625	65.55	87.4	65.55	81.9375	98.325	131.1

												Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs															33060	33075	33090	33120-4
EC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
438	0	1	1	0	1	1	0	1	1	0	1B 6	43.8	54.75	65.7	87.6	65.7	82.125	98.55	131.4
439	0	1	1	0	1	1	0	1	1	1	1B 7	43.9	54.875	65.85	87.8	65.85	82.3125	98.775	131.7
440	0	1	1	0	1	1	1	0	0	0	1B 8	44	55	66	88	66	82.5	99	132
441	0	1	1	0	1	1	1	0	0	1	1B 9	44.1	55.125	66.15	88.2	66.15	82.6875	99.225	132.3
442	0	1	1	0	1	1	1	0	1	0	1B A	44.2	55.25	66.3	88.4	66.3	82.875	99.45	132.6
443	0	1	1	0	1	1	1	0	1	1	1B B	44.3	55.375	66.45	88.6	66.45	83.0625	99.675	132.9
444	0	1	1	0	1	1	1	1	0	0	1B C	44.4	55.5	66.6	88.8	66.6	83.25	99.9	133.2
445	0	1	1	0	1	1	1	1	0	1	1B D	44.5	55.625	66.75	89	66.75	83.4375	100.125	133.5
446	0	1	1	0	1	1	1	1	1	0	1B E	44.6	55.75	66.9	89.2	66.9	83.625	100.35	133.8
447	0	1	1	0	1	1	1	1	1	1	1B F	44.7	55.875	67.05	89.4	67.05	83.8125	100.575	134.1
448	0	1	1	1	0	0	0	0	0	0	1C 0	44.8	56	67.2	89.6	67.2	84	100.8	134.4
449	0	1	1	1	0	0	0	0	0	1	1C 1	44.9	56.125	67.35	89.8	67.35	84.1875	101.025	134.7
450	0	1	1	1	0	0	0	0	1	0	1C 2	45	56.25	67.5	90	67.5	84.375	101.25	135
451	0	1	1	1	0	0	0	0	1	1	1C 3	45.1	56.375	67.65	90.2	67.65	84.5625	101.475	135.3
452	0	1	1	1	0	0	0	1	0	0	1C 4	45.2	56.5	67.8	90.4	67.8	84.75	101.7	135.6
453	0	1	1	1	0	0	0	1	0	1	1C 5	45.3	56.625	67.95	90.6	67.95	84.9375	101.925	135.9
454	0	1	1	1	0	0	0	1	1	0	1C 6	45.4	56.75	68.1	90.8	68.1	85.125	102.15	136.2
455	0	1	1	1	0	0	0	1	1	1	1C 7	45.5	56.875	68.25	91	68.25	85.3125	102.375	136.5
456	0	1	1	1	0	0	1	0	0	0	1C 8	45.6	57	68.4	91.2	68.4	85.5	102.6	136.8
457	0	1	1	1	0	0	1	0	0	1	1C 9	45.7	57.125	68.55	91.4	68.55	85.6875	102.825	137.1
458	0	1	1	1	0	0	1	0	1	0	1C A	45.8	57.25	68.7	91.6	68.7	85.875	103.05	137.4
459	0	1	1	1	0	0	1	0	1	1	1C B	45.9	57.375	68.85	91.8	68.85	86.0625	103.275	137.7
460	0	1	1	1	0	0	1	1	0	0	1C C	46	57.5	69	92	69	86.25	103.5	138
461	0	1	1	1	0	0	1	1	0	1	1C D	46.1	57.625	69.15	92.2	69.15	86.4375	103.725	138.3
462	0	1	1	1	0	0	1	1	1	0	1C E	46.2	57.75	69.3	92.4	69.3	86.625	103.95	138.6
463	0	1	1	1	0	0	1	1	1	1	1C F	46.3	57.875	69.45	92.6	69.45	86.8125	104.175	138.9
464	0	1	1	1	0	1	0	0	0	0	1D 0	46.4	58	69.6	92.8	69.6	87	104.4	139.2
465	0	1	1	1	0	1	0	0	0	1	1D 1	46.5	58.125	69.75	93	69.75	87.1875	104.625	139.5
466	0	1	1	1	0	1	0	0	1	0	1D 2	46.6	58.25	69.9	93.2	69.9	87.375	104.85	139.8
467	0	1	1	1	0	1	0	0	1	1	1D 3	46.7	58.375	70.05	93.4	70.05	87.5625	105.075	140.1
468	0	1	1	1	0	1	0	1	0	0	1D 4	46.8	58.5	70.2	93.6	70.2	87.75	105.3	140.4
469	0	1	1	1	0	1	0	1	0	1	1D 5	46.9	58.625	70.35	93.8	70.35	87.9375	105.525	140.7
470	0	1	1	1	0	1	0	1	1	0	1D 6	47	58.75	70.5	94	70.5	88.125	105.75	141
471	0	1	1	1	0	1	0	1	1	1	1D 7	47.1	58.875	70.65	94.2	70.65	88.3125	105.975	141.3
472	0	1	1	1	0	1	1	0	0	0	1D 8	47.2	59	70.8	94.4	70.8	88.5	106.2	141.6
473	0	1	1	1	0	1	1	0	0	1	1D 9	47.3	59.125	70.95	94.6	70.95	88.6875	106.425	141.9
474	0	1	1	1	0	1	1	0	1	0	1D A	47.4	59.25	71.1	94.8	71.1	88.875	106.65	142.2
475	0	1	1	1	0	1	1	0	1	1	1D B	47.5	59.375	71.25	95	71.25	89.0625	106.875	142.5
476	0	1	1	1	0	1	1	1	0	0	1D C	47.6	59.5	71.4	95.2	71.4	89.25	107.1	142.8

												Sample Rating							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
	Address Inputs															33060	33075	33090	33120-4
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		2560	2575	2590	25120	33120	33150	33180	33240
477	0	1	1	1	0	1	1	1	0	1	1D D	47.7	59.625	71.55	95.4	71.55	89.4375	107.325	143.1
478	0	1	1	1	0	1	1	1	1	0	1D E	47.8	59.75	71.7	95.6	71.7	89.625	107.55	143.4
479	0	1	1	1	0	1	1	1	1	1	1D F	47.9	59.875	71.85	95.8	71.85	89.8125	107.775	143.7
480	0	1	1	1	1	0	0	0	0	0	1E 0	48	60	72	96	72	90	108	144
481	0	1	1	1	1	0	0	0	0	1	1E 1	48.1	60.125	72.15	96.2	72.15	90.1875	108.225	144.3
482	0	1	1	1	1	0	0	0	1	0	1E 2	48.2	60.25	72.3	96.4	72.3	90.375	108.45	144.6
483	0	1	1	1	1	0	0	0	1	1	1E 3	48.3	60.375	72.45	96.6	72.45	90.5625	108.675	144.9
484	0	1	1	1	1	0	0	1	0	0	1E 4	48.4	60.5	72.6	96.8	72.6	90.75	108.9	145.2
485	0	1	1	1	1	0	0	1	0	1	1E 5	48.5	60.625	72.75	97	72.75	90.9375	109.125	145.5
486	0	1	1	1	1	0	0	1	1	0	1E 6	48.6	60.75	72.9	97.2	72.9	91.125	109.35	145.8
487	0	1	1	1	1	0	0	1	1	1	1E 7	48.7	60.875	73.05	97.4	73.05	91.3125	109.575	146.1
488	0	1	1	1	1	0	1	0	0	0	1E 8	48.8	61	73.2	97.6	73.2	91.5	109.8	146.4
489	0	1	1	1	1	0	1	0	0	1	1E 9	48.9	61.125	73.35	97.8	73.35	91.6875	110.025	146.7
490	0	1	1	1	1	0	1	0	1	0	1E A	49	61.25	73.5	98	73.5	91.875	110.25	147
491	0	1	1	1	1	0	1	0	1	1	1E B	49.1	61.375	73.65	98.2	73.65	92.0625	110.475	147.3
492	0	1	1	1	1	0	1	1	0	0	1E C	49.2	61.5	73.8	98.4	73.8	92.25	110.7	147.6
493	0	1	1	1	1	0	1	1	0	1	1E D	49.3	61.625	73.95	98.6	73.95	92.4375	110.925	147.9
494	0	1	1	1	1	0	1	1	1	0	1E E	49.4	61.75	74.1	98.8	74.1	92.625	111.15	148.2
495	0	1	1	1	1	0	1	1	1	1	1E F	49.5	61.875	74.25	99	74.25	92.8125	111.375	148.5
496	0	1	1	1	1	1	0	0	0	0	1F 0	49.6	62	74.4	99.2	74.4	93	111.6	148.8
497	0	1	1	1	1	1	0	0	0	1	1F 1	49.7	62.125	74.55	99.4	74.55	93.1875	111.825	149.1
498	0	1	1	1	1	1	0	0	1	0	1F 2	49.8	62.25	74.7	99.6	74.7	93.375	112.05	149.4
499	0	1	1	1	1	1	0	0	1	1	1F 3	49.9	62.375	74.85	99.8	74.85	93.5625	112.275	149.7
500	0	1	1	1	1	1	0	1	0	0	1F 4	50	62.5	75	100	75	93.75	112.5	150
501	0	1	1	1	1	1	0	1	0	1	1F 5	50.1	62.625	75.15	100.2	75.15	93.9375	112.725	150.3
502	0	1	1	1	1	1	0	1	1	0	1F 6	50.2	62.75	75.3	100.4	75.3	94.125	112.95	150.6
503	0	1	1	1	1	1	0	1	1	1	1F 7	50.3	62.875	75.45	100.6	75.45	94.3125	113.175	150.9
504	0	1	1	1	1	1	1	0	0	0	1F 8	50.4	63	75.6	100.8	75.6	94.5	113.4	151.2
505	0	1	1	1	1	1	1	0	0	1	1F 9	50.5	63.125	75.75	101	75.75	94.6875	113.625	151.5
506	0	1	1	1	1	1	1	0	1	0	1F A	50.6	63.25	75.9	101.2	75.9	94.875	113.85	151.8
507	0	1	1	1	1	1	1	0	1	1	1F B	50.7	63.375	76.05	101.4	76.05	95.0625	114.075	152.1
508	0	1	1	1	1	1	1	1	0	0	1F C	50.8	63.5	76.2	101.6	76.2	95.25	114.3	152.4
509	0	1	1	1	1	1	1	1	0	1	1F D	50.9	63.625	76.35	101.8	76.35	95.4375	114.525	152.7
510	0	1	1	1	1	1	1	1	1	0	1F E	51	63.75	76.5	102	76.5	95.625	114.75	153
511	0	1	1	1	1	1	1	1	1	1	1F F	51.1	63.875	76.65	102.2	76.65	95.8125	114.975	153.3
512	1	0	0	0	0	0	0	0	0	0	20 0	51.2	64	76.8	102.4	76.8	96	115.2	153.6
513	1	0	0	0	0	0	0	0	0	1	20 1	51.3	64.125	76.95	102.6	76.95	96.1875	115.425	153.9
514	1	0	0	0	0	0	0	0	1	0	20 2	51.4	64.25	77.1	102.8	77.1	96.375	115.65	154.2

EC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
	Address Inputs											Sample Rating							
												ISD Part Numbers							
																33060	33075	33090	33120-4
												2560	2575	2590	25120	33120	33150	33180	33240
592	1	0	0	1	0	1	0	0	0	0	25 0	59.2	74	88.8	118.4	88.8	111	133.2	177.6
593	1	0	0	1	0	1	0	0	0	1	25 1	59.3	74.125	88.95	118.6	88.95	111.1875	133.425	177.9
594	1	0	0	1	0	1	0	0	1	0	25 2	59.4	74.25	89.1	118.8	89.1	111.375	133.65	178.2
595	1	0	0	1	0	1	0	0	1	1	25 3	59.5	74.375	89.25	119	89.25	111.5625	133.875	178.5
596	1	0	0	1	0	1	0	1	0	0	25 4	59.6	74.5	89.4	119.2	89.4	111.75	134.1	178.8
597	1	0	0	1	0	1	0	1	0	1	25 5	59.7	74.625	89.55	119.4	89.55	111.9375	134.325	179.1
598	1	0	0	1	0	1	0	1	1	0	25 6	59.8	74.75	89.7	119.6	89.7	112.125	134.55	179.4
599	1	0	0	1	0	1	0	1	1	1	25 7	59.9	74.875	89.85	119.8	89.85	112.3125	134.775	179.7

"End of Message Storage Space for ISD2560, ISD2575, ISD2590, and ISD25120 Devices"

DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
	Address Inputs											Sample Rates							
												ISD Part Numbers							
																33120	33150	33180	33240
600	1	0	0	1	0	1	1	0	0	0	25 8					90	112.5	135	180
601	1	0	0	1	0	1	1	0	0	1	25 9					90.15	112.6875	135.225	180.3
602	1	0	0	1	0	1	1	0	1	0	25 A					90.3	112.875	135.45	180.6
603	1	0	0	1	0	1	1	0	1	1	25 B					90.45	113.0625	135.675	180.9
604	1	0	0	1	0	1	1	1	0	0	25 C					90.6	113.25	135.9	181.2
605	1	0	0	1	0	1	1	1	0	1	25 D					90.75	113.4375	136.125	181.5
606	1	0	0	1	0	1	1	1	1	0	25 E					90.9	113.625	136.35	181.8
607	1	0	0	1	0	1	1	1	1	1	25 F					91.05	113.8125	136.575	182.1
608	1	0	0	1	1	0	0	0	0	0	26 0					91.2	114	136.8	182.4
609	1	0	0	1	1	0	0	0	0	1	26 1					91.35	114.1875	137.025	182.7
610	1	0	0	1	1	0	0	0	1	0	26 2					91.5	114.375	137.25	183
611	1	0	0	1	1	0	0	0	1	1	26 3					91.65	114.5625	137.475	183.3
612	1	0	0	1	1	0	0	1	0	0	26 4					91.8	114.75	137.7	183.6
613	1	0	0	1	1	0	0	1	0	1	26 5					91.95	114.9375	137.925	183.9
614	1	0	0	1	1	0	0	1	1	0	26 6					92.1	115.125	138.15	184.2
615	1	0	0	1	1	0	0	1	1	1	26 7					92.25	115.3125	138.375	184.5
616	1	0	0	1	1	0	1	0	0	0	26 8					92.4	115.5	138.6	184.8
617	1	0	0	1	1	0	1	0	0	1	26 9					92.55	115.6875	138.825	185.1
618	1	0	0	1	1	0	1	0	1	0	26 A					92.7	115.875	139.05	185.4
619	1	0	0	1	1	0	1	0	1	1	26 B					92.85	116.0625	139.275	185.7
620	1	0	0	1	1	0	1	1	0	0	26 C					93	116.25	139.5	186
621	1	0	0	1	1	0	1	1	0	1	26 D					93.15	116.4375	139.725	186.3

	Address Inputs											Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
												ISD Part Numbers							
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0						33120	33150	33180	33240
702	1	0	1	0	1	1	1	1	1	0	2B E					105.3	131.625	157.95	210.6
703	1	0	1	0	1	1	1	1	1	1	2B F					105.45	131.8125	158.175	210.9
704	1	0	1	1	0	0	0	0	0	0	2C 0					105.6	132	158.4	211.2
705	1	0	1	1	0	0	0	0	0	1	2C 1					105.75	132.1875	158.625	211.5
706	1	0	1	1	0	0	0	0	1	0	2C 2					105.9	132.375	158.85	211.8
707	1	0	1	1	0	0	0	0	1	1	2C 3					106.05	132.5625	159.075	212.1
708	1	0	1	1	0	0	0	1	0	0	2C 4					106.2	132.75	159.3	212.4
709	1	0	1	1	0	0	0	1	0	1	2C 5					106.35	132.9375	159.525	212.7
710	1	0	1	1	0	0	0	1	1	0	2C 6					106.5	133.125	159.75	213
711	1	0	1	1	0	0	0	1	1	1	2C 7					106.65	133.3125	159.975	213.3
712	1	0	1	1	0	0	1	0	0	0	2C 8					106.8	133.5	160.2	213.6
713	1	0	1	1	0	0	1	0	0	1	2C 9					106.95	133.6875	160.425	213.9
714	1	0	1	1	0	0	1	0	1	0	2C A					107.1	133.875	160.65	214.2
715	1	0	1	1	0	0	1	0	1	1	2C B					107.25	134.0625	160.875	214.5
716	1	0	1	1	0	0	1	1	0	0	2C C					107.4	134.25	161.1	214.8
717	1	0	1	1	0	0	1	1	0	1	2C D					107.55	134.4375	161.325	215.1
718	1	0	1	1	0	0	1	1	1	0	2C E					107.7	134.625	161.55	215.4
719	1	0	1	1	0	0	1	1	1	1	2C F					107.85	134.8125	161.775	215.7
720	1	0	1	1	0	1	0	0	0	0	2D 0					108	135	162	216
721	1	0	1	1	0	1	0	0	0	1	2D 1					108.15	135.1875	162.225	216.3
722	1	0	1	1	0	1	0	0	1	0	2D 2					108.3	135.375	162.45	216.6
723	1	0	1	1	0	1	0	0	1	1	2D 3					108.45	135.5625	162.675	216.9
724	1	0	1	1	0	1	0	1	0	0	2D 4					108.6	135.75	162.9	217.2
725	1	0	1	1	0	1	0	1	0	1	2D 5					108.75	135.9375	163.125	217.5
726	1	0	1	1	0	1	0	1	1	0	2D 6					108.9	136.125	163.35	217.8
727	1	0	1	1	0	1	0	1	1	1	2D 7					109.05	136.3125	163.575	218.1
728	1	0	1	1	0	1	1	0	0	0	2D 8					109.2	136.5	163.8	218.4
729	1	0	1	1	0	1	1	0	0	1	2D 9					109.35	136.6875	164.025	218.7
730	1	0	1	1	0	1	1	0	1	0	2D A					109.5	136.875	164.25	219
731	1	0	1	1	0	1	1	0	1	1	2D B					109.65	137.0625	164.475	219.3
732	1	0	1	1	0	1	1	1	0	0	2D C					109.8	137.25	164.7	219.6
733	1	0	1	1	0	1	1	1	0	1	2D D					109.95	137.4375	164.925	219.9
734	1	0	1	1	0	1	1	1	1	0	2D E					110.1	137.625	165.15	220.2
735	1	0	1	1	0	1	1	1	1	1	2D F					110.25	137.8125	165.375	220.5
736	1	0	1	1	1	0	0	0	0	0	2E 0					110.4	138	165.6	220.8
737	1	0	1	1	1	0	0	0	0	1	2E 1					110.55	138.1875	165.825	221.1
738	1	0	1	1	1	0	0	0	1	0	2E 2					110.7	138.375	166.05	221.4
739	1	0	1	1	1	0	0	0	1	1	2E 3					110.85	138.5625	166.275	221.7
740	1	0	1	1	1	0	0	1	0	0	2E 4					111	138.75	166.5	222
741	1	0	1	1	1	0	0	1	0	1	2E 5					111.15	138.9375	166.725	222.3

												Sample Rates							
												8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz	8.0 KHz	6.4 KHz	5.3 KHz	4.0 KHz
	Address Inputs											ISD Part Numbers							
DEC	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0						33120	33150	33180	33240
782	1	1	0	0	0	0	1	1	1	0	30 E					117.3	146.625	175.95	234.6
783	1	1	0	0	0	0	1	1	1	1	30 F					117.45	146.8125	176.175	234.9
784	1	1	0	0	0	1	0	0	0	0	31 0					117.6	147	176.4	235.2
785	1	1	0	0	0	1	0	0	0	1	31 1					117.75	147.1875	176.625	235.5
786	1	1	0	0	0	1	0	0	1	0	31 2					117.9	147.375	176.85	235.8
787	1	1	0	0	0	1	0	0	1	1	31 3					118.05	147.5625	177.075	236.1
788	1	1	0	0	0	1	0	1	0	0	31 4					118.2	147.75	177.3	236.4
789	1	1	0	0	0	1	0	1	0	1	31 5					118.35	147.9375	177.525	236.7
790	1	1	0	0	0	1	0	1	1	0	31 6					118.5	148.125	177.75	237
791	1	1	0	0	0	1	0	1	1	1	31 7					118.65	148.3125	177.975	237.3
792	1	1	0	0	0	1	1	0	0	0	31 8					118.8	148.5	178.2	237.6
793	1	1	0	0	0	1	1	0	0	1	31 9					118.95	148.6875	178.425	237.9
794	1	1	0	0	0	1	1	0	1	0	31 A					119.1	148.875	178.65	238.2
795	1	1	0	0	0	1	1	0	1	1	31 B					119.25	149.0625	178.875	238.5
796	1	1	0	0	0	1	1	1	0	0	31 C					119.4	149.25	179.1	238.8
797	1	1	0	0	0	1	1	1	0	1	31 D					119.55	149.4375	179.325	239.1
798	1	1	0	0	0	1	1	1	1	0	31 E					119.7	149.625	179.55	239.4
799	1	1	0	0	0	1	1	1	1	1	31 F					119.85	149.8125	179.775	239.7

ISD2560/75/90/120

SINGLE-CHIP, MULTIPLE-MESSAGES,

VOICE RECORD/PLAYBACK DEVICE

60-, 75-, 90-, AND 120-SECOND DURATION

Publication Release Date: May 2003
Revision 1.0

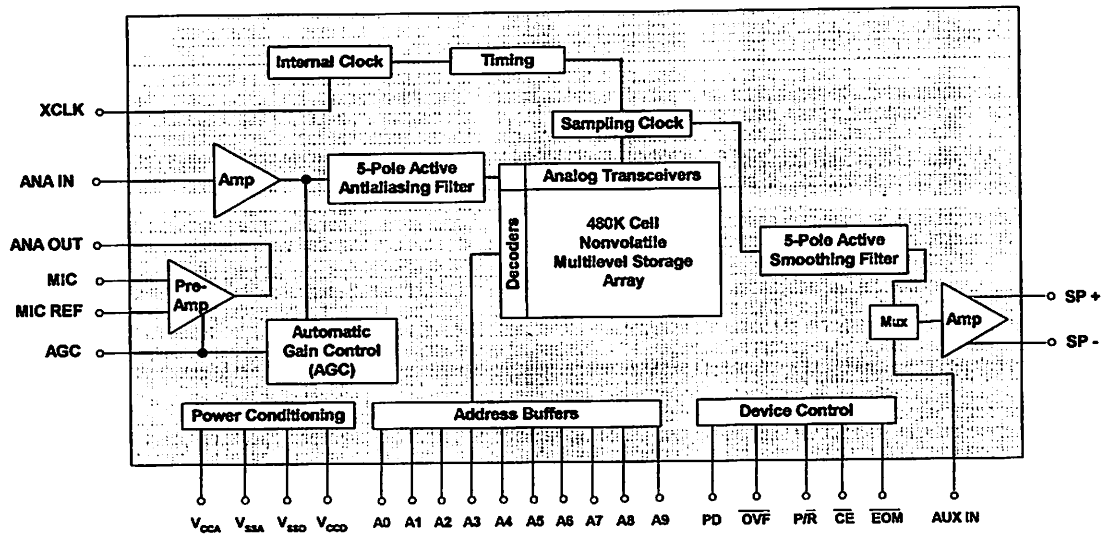
1. GENERAL DESCRIPTION

Winbond's ISD2500 ChipCorder® Series provide high-quality, single-chip, Record/Playback solutions for 60- to 120-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, speaker amplifier, and high density multi-level storage array. In addition, the ISD2500 is microcontroller compatible, allowing complex messaging and addressing to be achieved. Recordings are stored into on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through Winbond's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

2. FEATURES

- Easy-to-use single-chip, voice record/playback solution
- High-quality, natural voice/audio reproduction
- Single-chip with duration of 60, 75, 90, or 120 seconds.
- Manual switch or microcontroller compatible
- Playback can be edge- or level-activated
- Directly cascadable for longer durations
- Automatic power-down (push-button mode)
  - Standby current 1 μA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- Programmer support for play-only applications
- Single +5 volt power supply
- Available in die form, PDIP, SOIC and TSOP packaging
- Temperature = die (0°C to +50°C) and package (0°C to +70°C)

3. BLOCK DIAGRAM



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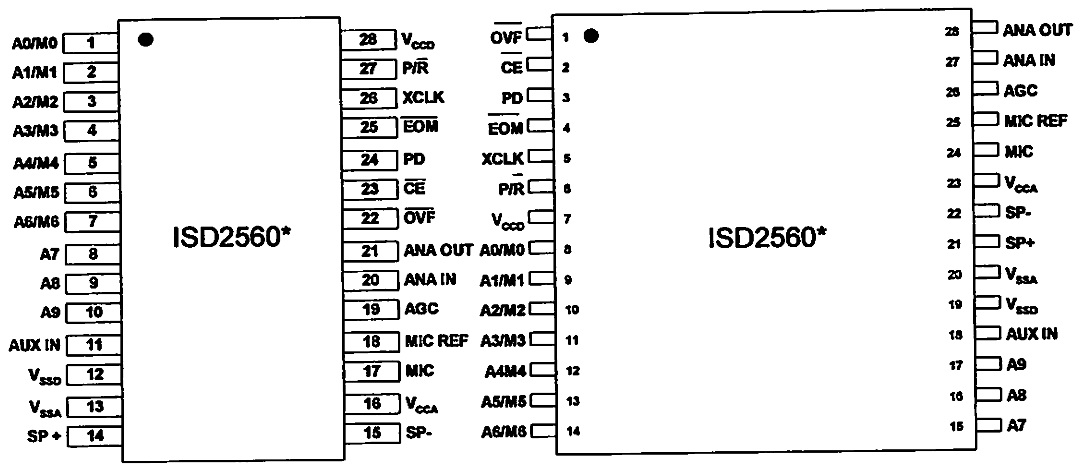
5. PIN CONFIGURATION



SOIC/PDIP TSOP

* Same pinouts for ISD2575 / 2590 / 25120 products

PIN NAME	PIN NO.		FUNCTION
	SOIC/ PDIP	TSOP	
V_{CCA}, V_{CCD}	16, 28	23, 7	**Supply Voltage**: To minimize noise, the analog and digital circuits in the ISD2500 series devices use separate power busses. These voltage busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.
MIC	17	24	**Microphone**: The microphone pin transfers input signal to the on-chip preamplifier. A built-in Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the ISD2500 series passband. See Winbond's Application Information for additional information on low-frequency cutoff calculation.
MIC REF	18	25	**Microphone Reference**: The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected to a differential microphone.
AGC	19	26	**Automatic Gain Control**: The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2 on the schematic of Figure 5 in section 11) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2) connected in parallel between the AGC pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases.
ANA IN	20	27	**Analog Input**: The analog input transfers analog signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.
ANA OUT	21	28	**Analog Output**: This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

PIN NAME	PIN NO.		FUNCTION
	SOIC/ PDIP	TSOP	
$\overline{OVF}$	22	1	**Overflow**: This signal pulses LOW at the end of memory array, indicating the device has been filled and the message has overflowed. The $\overline{OVF}$ output then follows the $\overline{CE}$ input until a PD pulse has reset the device. This pin can be used to cascade several ISD2500 devices together to increase record/playback durations.
$\overline{CE}$	23	2	**Chip Enable**: The $\overline{CE}$ input pin is taken LOW to enable all playback and record operations. The address pins and playback/record pin (P/$\overline{R}$) are latched by the falling edge of $\overline{CE}$. $\overline{CE}$ has additional functionality in the M6 (Push-Button) Operational Mode as described in the Operational Mode section.
PD	24	3	**Power Down**: When neither record nor playback operation, the PD pin should be pulled HIGH to place the part in standby mode (see I_{SB} specification). When overflow ($\overline{OVF}$) pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the memory array. The PD pin has additional functionality in the M6 (Push-Button) Operation Mode as described in the Operational Mode section.
$\overline{EOM}$	25	4	**End-Of-Message**: A nonvolatile marker is automatically inserted at the end of each recorded message. It remains there until the message is recorded over. The $\overline{EOM}$ output pulses LOW for a period of T_{EOM} at the end of each message. In addition, the ISD2500 series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5V. In this case, $\overline{EOM}$ goes LOW and the device is fixed in Playback-only mode. When the device is configured in Operational Mode M6 (Push-Button Mode), this pin provides an active-HIGH signal, indicating the device is currently recording or playing. This signal can conveniently drive an LED for visual indicator of a record or playback operation in process.

<table>
<tr><th rowspan="2">PIN NAME</th><th colspan="2">PIN NO.</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>SOIC/ PDIP</th><th>TSOP</th></tr>
<tr><td>XCLK</td><td>26</td><td>5</td><td>External Clock: The external clock input has an internal pull-down device. The device is configured at the factory with an internal sampling clock frequency centered to ±1 percent of specification. The frequency is then maintained to a variation of ±2.25 percent over the entire commercial temperature and operating voltage ranges. If greater precision is required, the device can be clocked through the XCLK pin as follows:
<table>
<tr><th>Part Number</th><th>Sample Rate</th><th>Required Clock</th></tr>
<tr><td>ISD2560</td><td>8.0 kHz</td><td>1024 kHz</td></tr>
<tr><td>ISD2575</td><td>6.4 kHz</td><td>819.2 kHz</td></tr>
<tr><td>ISD2590</td><td>5.3 kHz</td><td>682.7 kHz</td></tr>
<tr><td>ISD25120</td><td>4.0 kHz</td><td>512 kHz</td></tr>
</table>
These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. If the XCLK is not used, this input must be connected to ground.</td></tr>
<tr><td>P/$\overline{\text{R}}$</td><td>27</td><td>6</td><td>Playback/Record: The P/$\overline{\text{R}}$ input pin is latched by the falling edge of the $\overline{\text{CE}}$ pin. A HIGH level selects a playback cycle while a LOW level selects a record cycle. For a record cycle, the address pins provide the starting address and recording continues until PD or $\overline{\text{CE}}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a record cycle is terminated by pulling PD or $\overline{\text{CE}}$ HIGH, then End-Of-Message ($\overline{\text{EOM}}$) marker is stored at the current address in memory. For a playback cycle, the address inputs provide the starting address and the device will play until an $\overline{\text{EOM}}$ marker is encountered. The device can continue to pass an $\overline{\text{EOM}}$ marker if $\overline{\text{CE}}$ is held LOW in address mode, or in an Operational Mode. (See Operational Modes section)</td></tr>
</table>

Programming

The ISD2500 series is also ideal for playback-only applications, where single or multiple messages are referenced through buttons, switches, or a microcontroller. Once the desired message configuration is created, duplicates can easily be generated via a gang programmer.

7.2. Operational Modes

The ISD2500 series is designed with several built-in Operational Modes that provide maximum functionality with minimum external components. These modes are described in details as below. The Operational Modes are accessed via the address pins and mapped beyond the normal message address range. When the two Most Significant Bits (MSB), A8 and A9, are HIGH, the remaining address signals are interpreted as mode bits and not as address bits. Therefore, Operational Modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using Operational Modes. First, all operations begin initially at address 0 of its memory. Later operations can begin at other address locations, depending on the Operational Mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback, playback to record (except M6 mode), or when a Power-Down cycle is executed.

Second, Operational Modes are executed when $\overline{CE}$ goes LOW. This Operational Mode remains in effect until the next LOW-going $\overline{CE}$ signal, at which point the current mode(s) are sampled and executed.

TABLE 2: OPERATIONAL MODES

Mode [1]	Function	Typical Use	Jointly Compatible [2]
M0	Message cueing	Fast-forward through messages	M4, M5, M6
M1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	M3, M4, M5, M6
M2	Not applicable	Reserved	N/A
M3	Looping	Continuous playback from Address 0	M1, M5, M6
M4	Consecutive addressing	Record/playback multiple consecutive messages	M0, M1, M5
M5	$\overline{CE}$ level-activated	Allows message pausing	M0, M1, M3, M4
M6	Push-button control	Simplified device interface	M0, M1, M3

[1] Besides mode pin needed to be "1", A8 and A9 pin are also required to be "1" in order to enter into the related operational mode.

[2] Indicates additional Operational Modes which can be used simultaneously with the given mode.

7.2.1. Operational Modes Description

The Operational Modes can be used in conjunction with a microcontroller, or they can be hardwired to provide the desired system operation.

M0 – Message Cueing

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each $\overline{\text{CE}}$ LOW pulse causes the internal address pointer to skip to the next message. This mode is used for playback only, and is typically used with the M4 Operational Mode.

M1 – Delete $\overline{\text{EOM}}$ Markers

The M1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one $\overline{\text{EOM}}$ marker set at the end of the final message. When this Operational Mode is configured, messages recorded sequentially are played back as one continuous message.

M2 – Unused

When Operational Modes are selected, the M2 pin should be LOW.

M3 – Message Looping

The M3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message can completely fill the ISD2500 device and will loop from beginning to end without $\overline{\text{OVF}}$ going LOW.

M4 – Consecutive Addressing

During normal operation, the address pointer will reset when a message is played through an $\overline{\text{EOM}}$ marker. The M4 Operational Mode inhibits the address pointer reset on $\overline{\text{EOM}}$, allowing messages to be played back consecutively.

M5 - $\overline{\text{CE}}$-Level Activated

The default mode for ISD2500 devices is for $\overline{\text{CE}}$ to be edge-activated on playback and level-activated on record. The M5 Operational Mode causes the $\overline{\text{CE}}$ pin to be interpreted as level-activated as opposed to edge-activated during playback. This is especially useful for terminating playback operations using the $\overline{\text{CE}}$ signal. In this mode, $\overline{\text{CE}}$ LOW begins a playback cycle, at the beginning of the device memory. The playback cycle continues as long as $\overline{\text{CE}}$ is held LOW. When $\overline{\text{CE}}$ goes HIGH, playback will immediately end. A new $\overline{\text{CE}}$ LOW will restart the message from the beginning unless M4 is also HIGH.

2. The P/$\overline{R}$ pin is taken LOW.
3. The $\overline{CE}$ pin is pulsed LOW. Recording starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. When the $\overline{CE}$ pin is pulsed LOW. Recording pauses, $\overline{EOM}$ goes back LOW. The internal address pointers are not cleared, but the $\overline{EOM}$ marker is stored in memory to indicate as the message end. The P/$\overline{R}$ pin may be taken HIGH at this time. Any subsequent $\overline{CE}$ would start a playback at address 0.
5. The $\overline{CE}$ pin is pulsed LOW. Recording starts at the next address after the previous set $\overline{EOM}$ marker. $\overline{EOM}$ goes back HIGH.[3]
6. When the recording sequences are finished, the final $\overline{CE}$ pulse LOW will end the last record cycle, leaving a set $\overline{EOM}$ marker at the message end. Recording may also be terminated by a HIGH level on PD, which will leave a set $\overline{EOM}$ marker.

Playback in Push-Button Mode

1. The PD pin should be LOW.
2. The P/$\overline{R}$ pin is taken HIGH.
3. The $\overline{CE}$ pin is pulsed LOW. Playback starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. If the $\overline{CE}$ pin is pulsed LOW or an $\overline{EOM}$ marker is encountered during an operation, the part will pause. The internal address pointers are not cleared, and $\overline{EOM}$ goes back LOW. The P/$\overline{R}$ pin may be changed at this time. A subsequent record operation would not reset the address pointers and the recording would begin where playback ended.
5. $\overline{CE}$ is again pulsed LOW. Playback starts where it left off, with $\overline{EOM}$ going HIGH to indicate an operation in progress.
6. Playback continues as in steps 4 and 5 until PD is pulsed HIGH or overflow occurs.
7. If in overflow, pulling $\overline{CE}$ LOW will reset the address pointer and start playback from the beginning. After a PD pulse, the part is reset to address 0.

Note: Push-Button Mode can be used in conjunction with modes M0, M1, and M3.

[3] If the M1 Operational Mode pin is also HIGH, the just previously written $\overline{EOM}$ bit is erased, and recording starts at that address.

11. TYPICAL APPLICATION CIRCUIT

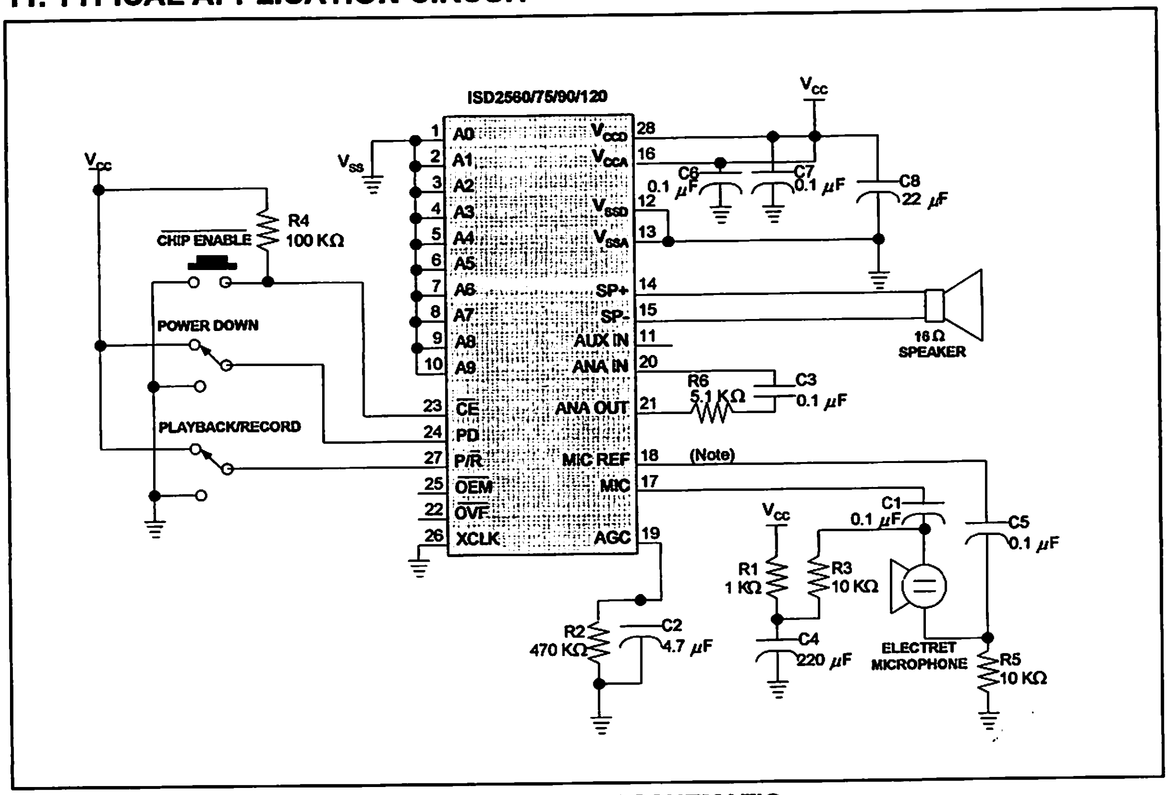


FIGURE 5: DESIGN SCHEMATIC

Note: If desired, pin 18 (PDIP package) may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage. Additional design example schematics are provided below.

TABLE 13: APPLICATION EXAMPLE – BASIC DEVICE CONTROL

Control Step	Function	Action
1	Power up chip and select Record/Playback Mode	1. PD = LOW, 2. P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0-A9
3A	Begin playback	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulse LOW
3B	Begin record	P/$\overline{R}$ = LOW, $\overline{CE}$ = LOW
4A	End playback	Automatic
4B	End record	PD or $\overline{CE}$ = HIGH

TABLE 14: APPLICATION EXAMPLE – PASSIVE COMPONENT FUNCTIONS

Part	Function	Comments
R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3, R5	Microphone biasing resistors	Provides biasing for microphone operation
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages
R6	Series limiting resistor	Reduces level to high supply voltages
C1, C5	Microphone DC-blocking capacitor Low-frequency cutoff	Decouples microphone bias from chip. Provides single-pole low-frequency cutoff and command mode noise rejection.
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
C4	Microphone power supply decoupling	Reduces power supply noise
C6, C7, C8	Power supply capacitors	Filter and bypass of power supply