INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

SKRIPSI

PERENCANAAN DAN PEMBUATAN ALAT PENGUKUR KETINGGIAN GELOMBANG AIR LAUT UNTUK INFORMASI PELAYARAN BERBASIS MIKROKONTROLLER AT89S8252

Disusun Oleh :
ERWIN NURPATRIA SAKTI
NIM : 0017179

SEPTEMBER 2006

LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN ALAT PENGUKUR KETINGGIAN GELOMBANG AIR LAUT UNTUK INFORMASI PELAYARAN BERBASIS MIKROKONTROLLER AT89S8252

SKRIPSI

Disusun dan Diajukan untuk Melengkapi dan Memenuhi Syarat Guna Mencapai Gelar Sarjana Teknik

Disusun Oleh :

ERWIN NUR PATRIA SAKTI

NIM : 0017179

Mengetahui

Ketua Jurusan T.Elektro S-1

Ir.F.Yudi Limpraptono.MT

NIP.Y.1039500274

Diperiksa dan Disetujui

Dosen Pembimbing

Joshep Dedy Irawan.ST,MT

NIP.132315178

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BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

Nama : ERWIN NURPATRIA SAKTI
Nim : 00.17.179
Jurusan : Teknik Elektro S-1
Konsentrasi : Teknik Elektronika
Judul Skripsi : PERENCANAAN DAN PEMBUATAN ALAT PENGUKUR KETINGGIAN GELOMBANG AIR LAUT UNTUK INFORMASI PELAYARAN BERBASIS MIKRONTROLLER AT89S8252

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Hari : KAMIS
Tanggal : 21 September 2006
Dengan Nilai : 80,85 (A)

Panitia Ujian Skripsi,

Ketua	Sekretaris
Ir. Mochtar Asroni, MSME	Ir. F. Yudi Limpraptono, MT

Anggota Penguji,

Penguji I	Penguji II
Ir. Usman Djuanda, MM	Sotyohadi, ST, MSc

ABSTRAKSI

PERENCANAAN DAN PEMBUATAN ALAT PENGUKUR KETINGGIAN GELOMBANG AIR LAUT UNTUK INFORMASI PELAYARAN BERBASIS MIKROKONTROLLER AT89S8252

(Erwin Nurpatria Sakti, 0017179, Teknik Elektronika S-1)
(Dosen Pembimbing :Joseph Dedy Irawan ST,MT)

Kata Kunci : Konsep Ketinggian, Sensor Tekanan.

Untuk mengurangi jumlah korban dalam aktifitas kelautan akibat kurangnya informasi tentang bahaya gelombang yang terjadi dilaut dibuat instrument dengan memanfaatkan fungsi dari mikrokontroller sebagai pengolah data. Sebuah alat dengan ukuran yang reatif kecil dan harganya pun relatif murah. Dengan dibuatnya alat ini diharapkan mampu menyelamatkan jiwa orang lain sebanyak mungkin.

Dalam pembuatan alat ukur ketinggian gelombang air laut digunakan sebuah metode untuk menentukan ketinggian yaitu dengan menggunakan tekanan udara. Untuk menentukan ketinggian tempat hal-hal yang perlu diperhatikan adalah perubahan tekanan udara dan suhu (temperatur) pada tempat tersebut. Semakin meningkatnya ketinggian dari permukaan laut maka tekanan udara dan suhu akan semakin menurun, demikian pula sebaliknya tekanan udara dan suhu akan semakin meningkat jika ketinggiannya menurun.

Pemakaian sensor tekanan ini mengacu pada *datasheet* yang telah ada sensor MPX4115AP memiliki jangkauan 3313 feet (994,11m) di bawah permukaan laut hingga 49902 feet (14970m) di atas permukaan laut, Dari spesifikasi alat ini dirancang dapat mengukur ketinggian 0m hingga 4095m dengan range tekanan udara 60kPa hingga 101,3kPa. Berdasarkan *datasheet* sensor MPX4115AP pada range tekanan udara tersebut, sensor MPX4115AP dapat menghasilkan tegangan keluaran pada kisaran 2,25 volt hingga 4,08 volt Berdasarkan spesifikasi alat yang dapat mengukur ketinggian 0 meter hingga 4095 meter dari permukaan laut, diharapkan dengan perubahan resolusi ADC 1mV alat ini mampu mendeteksi perubahan kenaikan ketinggian gelombang air laut setiap 1 meter untuk ditampilkan kedalam PC berupa grafik perubahan ketinggian terhadap waktu.

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Puji dan syukur penulis panjatkan kehadirat Tuhan yang maha esa, yang telah melimpahkan rahmat dan petunjuk-Nya sehingga penulis dapat menyelesaikan laporan skripsi yang berjudul "***Perencanaan dan Pembuatan Alat Pengukur Ketinggian Gelombang Air Laut Untuk Informasi Pelayaran Berbasis Mikrokontroller AT89S8252***". Penyusunan skripsi ini merupakan salah satu syarat dalam rangka menyelesaikan studi di Fakultas Teknologi Industri Institut Teknologi Nasional Malang.

Dalam kesempatan ini penulis ingin menyampaikan banyak terima kasih kepada :

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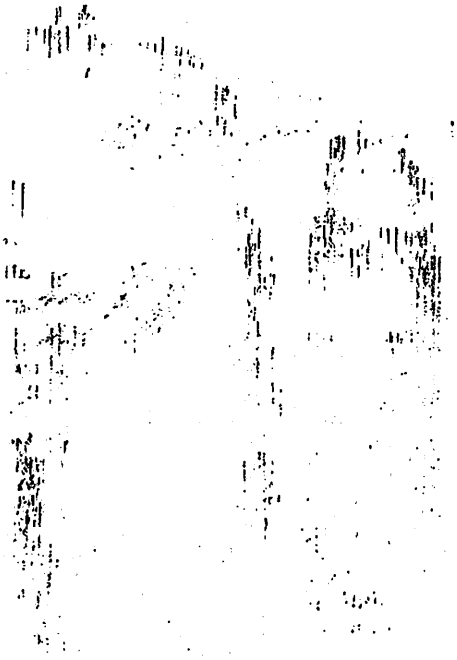
2. Joseph Dedy Irawan, ST, MT, selaku dosen pembimbing
3. Seluruh pihak yang telah membantu penulis untuk menyelesaikan laporan skripsi ini

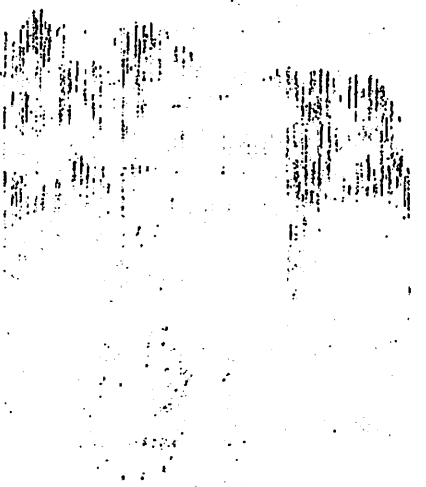
Penulis menyadari bahwa dalam laporan ini masih banyak terdapat kekurangan dan kesalahan. Oleh karena itu saran dan kritik guna memperbaiki laporan ini sangat diharapkan.

Akhir kata semoga laporan ini dapat berguna bagi semua pihak yang membutuhkan.

Malang, September 2006

Penulis





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BAB I

PENDAHULUAN

1.1. Latar Belakang

Pada era globalisasi yang makin maju telah memicu segala bidang ilmu pengetahuan dan dunia pendidikan untuk membuat inovasi-inovasi sehingga segala hal akan menjadi lebih mudah dan efisien. Elektronika merupakan salah satu ilmu pengetahuan yang sangat berpengaruh pada perkembangan teknologi sekarang ini.

Mikrokontroller sebagai suatu terobosan teknologi mikroprosessor dan mikrokontroller, hadir memenuhi kebutuhan pasar dan teknologi baru. Sebagai teknologi baru yaitu teknologi yang ada didalamnya dapat dikatakan sebagai komputer dalam chip, membutuhkan ruang yang kecil sedangkan fungsinya hampir sama dengan komputer. Dengan menambah beberapa rangkaian sensing dan memadukannya dengan pesawat HT, sebuah mikrokontroller sebagai pengolah data mampu mengontrol perangkat aplikatif sesuai dengan fungsi dari rangkaian pendukungnya dengan jarak yang sangat jauh.

Aktifitas penduduk tidak lepas dari bidang kelautan, pelayaran merupakan aktifitas utama dibidang kelautan diantaranya adalah para nelayan, transportasi laut, pengamanan laut, penelitian laut, bahkan untuk hiburan dan lain-lain. Mereka tidak tahu tentang keadaan sesungguhnya yang terjadi ditengah laut sangat membahayakan dirinya untuk melakukan pelayaran. Yang pasti adalah ketinggian gelombang air laut itu layak atau tidak untuk melakukan pelayaran.

Untuk mengurangi jumlah korban dalam aktifitas kelautan akibat kurangnya informasi tentang bahaya gelombang yang terjadi dilaut dibuat instrument dengan memanfaatkan fungsi dari mikrokontroller sebagai pengolah data. Sebuah alat dengan ukuran yang reatif kecil dan harganya pun relatif murah. Dengan dibuatnya alat ini diharapkan mampu menyelamatkan jiwa orang lain sebanyak mungkin.

1.2. Rumusan Masalah

Mengacu pada latar belakang diatas berkaitan dengan proses pembuatan alat pengukur ketinggian gelombang air laut untuk informasi pelayaran dapat disusun rumusan masalah sebagai berikut.

1) bagaimana merencanakan dan membuat alat yang berfungsi sebagai alat ukur yang dapat digunakan untuk mengukur ketinggian gelombang air laut
2) bagaimana merencanakan dan membuat perangkat-lunak untuk mengukur ketinggian gelombang air laut sebagai antarmuka dari mikrokontroler;

1.3. Batasan Masalah.

Dalam penulisan skripsi ini akan dibahas tentang rancang bangun alat pengukur ketinggian gelombang air laut dengan tampilan grafik pada PC, untuk mencegah meluasnya permasalahan dari fokus pembahasan, maka diperlukan pembatasan permasalahan yang meliputi:

1) Masalah perangkat-keras yang meliputi Mikrokontroller sebagai pengolah data yang akan dikirim melalui DTMF, sensor tekanan, ADC (Analog to

Digital Converter) sebagai pengkonversi data analog dari sensor menjadi data digital, dan PC sebagai penampil (Display).

2) Masalah perangkat-lunak yang meliputi diagram alur (*flow chart*) dan program
3) Tidak membahas catu daya pada alat yang dirancang. Kondisi catu daya diasumsikan nyala terus menerus.
4) Tidak membahas tata letak / penempatan alat di atas permukaan air laut.
5) Alat yang dibuat dalam bentuk simulasi (*prototype*).

1.4. Tujuan

Tujuan dari pembuatan dan perencanaan alat ini adalah:

1) Dapat membuat alat yang berfungsi sebagai alat ukur yang dapat digunakan untuk mengukur ketinggian gelombang air laut untuk Informasi Pelayaran.
2) Memudahkan pihak atau instansi terkait untuk memantau ketinggian gelombang air laut secara kontiyu.
3) Menghilangkan faktor keterbatasan jarak dan waktu dalam pamantauan ketinggian gelombang air laut.

1.5. Metodologi

Metodologi penelitian yang dipakai dalam pembuatan laporan skripsi ini adalah :

a. Studi literature.
b. Perencanaan dan pembuatan alat.

c. Pelaksanaan uji coba alat.

d. Penyusunan laporan skripsi.

1.6. Sistematika Penulisan

Sistem penulisan yang akan digunakan untuk membahas masalah dalam tugas akhir ini diperlukan gambaran susunan alat secara keseluruhan yang selanjutnya ditentukan komponen-komponen utama dan pendukung yang digunakan dan kemungkinan untuk disederhanakan baik untuk bentuk, biaya pembuatannya agar didapatkan susunan yang seefisien dan seefektif mungkin.

Adapun pembahasan Tugas Akhir ini dibagi menjadi beberapa bab sebagai berikut :

BAB I Pendahuluan

Pada pendahuluan ini dibahas latar belakang Perencanaan dan Pembuatan alat Pengukur Ketinggian Gelombang Air Laut Untuk Informasi Pelayaran berbasis Mikrokontroller AT89S8252., rumusan masalah , batasan masalah, tujuan pembuatan alat, metodologi dan sistematika penulisan.

BAB II Dasar Teori

Pada dasar teori ini akan dibahas mengenai teori-teori yang mendasari pembuatan alat ini.

BAB III Perencanaan Dan Pembuatan Alat

Memuat Perencanaan dan Pembuatan alat Pengukur Ketinggian Gelombang Air Laut Untuk Informasi Pelayaran berbasis Mikrokontroller AT89S8252

BAB IV Pengujian Alat

Memuat hasil pengujian Perencanaan dan Pembuatan alat Pengukur Ketinggian Gelombang Air Laut Untuk Informasi Pelayaran berbasis Mikrokontroller AT89S8252

BAB V Penutup

Berisi kesimpulan dari Perencanaan dan Pembuatan alat Pengukur Ketinggian Gelombang Air Laut Untuk Informasi Pelayaran berbasis Mikrokontroller AT89S8252 Serta saran-saran yang telah menyempurnakan alat yang telah dibuat

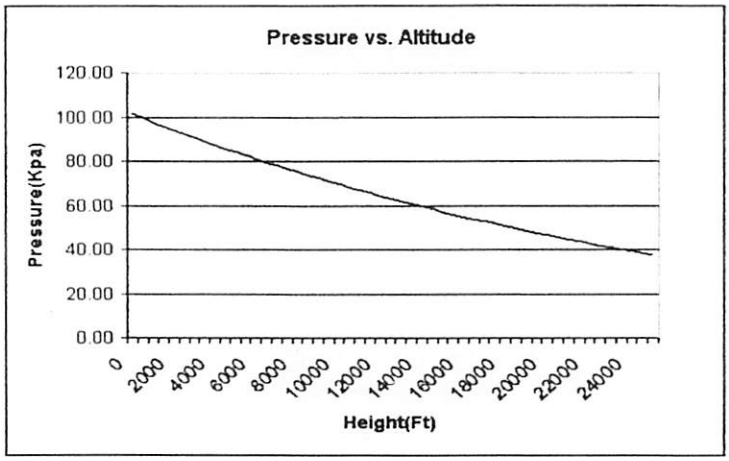
BAB II

DASAR TEORI

Dalam merencanakan dan merealisasikan sistem ini dibutuhkan pemahaman mengenai pengetahuan yang berhubungan dengan aplikasi tersebut. Pemahaman tersebut akan sangat bermanfaat dalam perancangan perangkat keras maupun perangkat lunak sistem. Adapun pengetahuan yang mendukung perencanaan dan realisasi alat antara lain, sensor MPX4115A, pengkondisi sinyal, ADC mikrokontroller AT89S8252 dan DTMF.

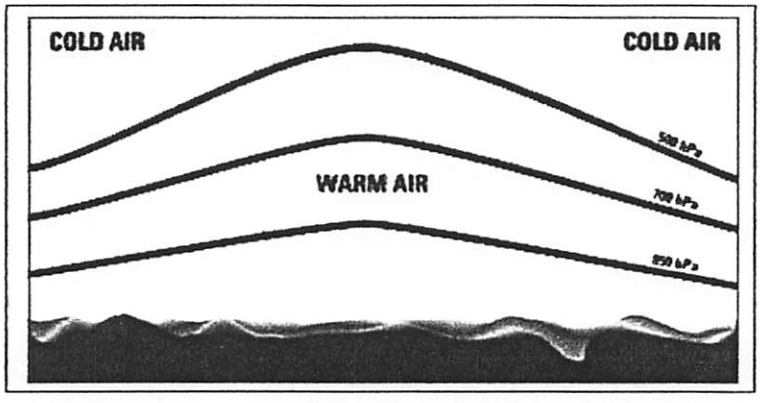
2.1 Konsep Ketinggian

Dalam pembuatan alat ukur ketinggian gelombang air laut digunakan sebuah metode untuk menentukan ketinggian yaitu dengan menggunakan tekanan udara. Di permukaan laut, tekanan udara berkisar pada angka 1013,25 milibar (1013hPa). Perbedaan ketinggian dan temperatur akan menyebabkan tekanan turun. Para ahli telah menetapkan bahwa setiap terjadi perubahan ketinggian sebesar 1000m, tekanan udara akan mengalami penurunan sekitar 100mb (100hPa). Hal ini terjadi karena semakin tinggi permukaan semakin tipis pula tingkat kerapatan udara, sehingga menyebabkan penurunan tekanan udara yang besarnya sekitar 100mb (100hPa) per 1000m. (Priyono, 2003:2). Hal tersebut dapat digambarkan dengan menggunakan sebuah grafik seperti yang ditunjukkan dalam Gambar 2.1 berikut:



Gambar 2.1 Grafik hubungan antara Tekanan Udara dan Ketinggian
Sumber : Halliday, 1985:560

Variasi tingkat ketinggian juga dipengaruhi oleh temperatur dan fluktuasi tekanan dari lapisan udara yaitu udara hangat (*warm air*) dan udara dingin (*cold air*). Karena udara terdingin lokasinya dekat kutub, level tekanan di sana umumnya lebih rendah dibandingkan level tekanan di atas garis katulistiwa. (Lane, 2004:8). Tekanan suatu gas dengan massa tertentu berbanding lurus dengan temperatur mutlak, bila volume tak berubah (Keenan dkk, 1992:258). Seperti terlihat dalam Gambar 2.2 berikut:



Gambar 2.2 Efek temperature dari level perubahan tekanan
Sumber: Lane, 2004:8

Dari gambar terlihat bahwa semakin besar tekanan udara, udara di sekitarnya akan semakin hangat. Demikian pula sebaliknya makin kecil tekanan udara, udara di sekitarnya juga akan semakin dingin. Fenomena ini sesuai dengan Hukum Gas Ideal yang menyatakan bahwa

$$PV = T \quad \text{.....(2.1)}$$

Sumber: Kleinfelter, 1992:263

dimana P = Tekanan dari gas, V = volume yang ditempati, dan T = temperatur.

Dalam bentuk sederhana, jika volume konstan, peningkatan pada temperature sebanding dengan peningkatan pada tekanan. Jika tekanan konstan, peningkatan pada temperature juga sebanding dengan peningkatan pada volume. Sebaliknya, jika volume menurun dan tekanan tetap konstan, temperatur juga ikut menurun. Hal terpenting adalah perubahan tekanan dan volume sebanding dengan perubahan temperatur.

Dari ilustrasi di atas dapat diambil kesimpulan bahwa dalam menentukan ketinggian tempat hal-hal yang perlu diperhatikan adalah perubahan tekanan udara dan suhu (temperatur) pada tempat tersebut. Semakin meningkatnya ketinggian dari permukaan laut maka tekanan udara dan suhu akan semakin menurun, demikian pula sebaliknya tekanan udara dan suhu akan semakin meningkat jika ketinggiannya menurun.

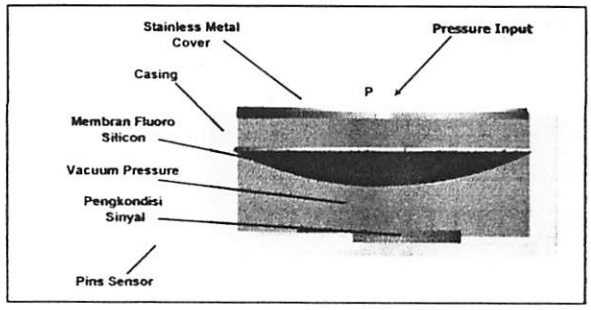
Untuk selanjutnya pada bagian ini membahas tentang sensor tekanan yang mengacu pada *datasheet* yang telah ada, penguat operasional sebagai pengkondisi sinyalnya, ADC dan mikrokontroller sebagai pengolah datanya.

2.2 Sensor Tekanan (*Pressure Sensor*)

Bagian pertama dan paling penting dari sistem ini adalah sensor yang digunakan untuk mendeteksi perubahan tekanan udara. Adalah sensor tekanan (*Integrated Silicon Pressure Sensor*) dengan tipe MPX4115AP yang diproduksi oleh Motorola. Inc. Sensor ini dipilih karena dapat menghasilkan sinyal keluaran analog berupa tegangan apabila terjadi perubahan tekanan udara pada suatu tempat. Menurut *datasheet* yang ada, keluaran yang dihasilkan sensor ini berada pada range 0,2 volt – 4,7 volt dengan range tekanan 15 kPa-115kPa dan memiliki sensitivitas sebesar 45,9mV/kPa.

Cara kerja sensor MPX4115AP sama dengan cara kerja sensor-sensor lainnya dimana bila terdeteksi perubahan besaran fisik yaitu perubahan tekanan udara, maka sensor akan bekerja dan menghasilkan tegangan. Besaran fisik yang dapat dideteksi sensor MPX4115AP dinyatakan dalam satuan hPa (*hectoPascal*). hPa disebut juga seratus Pascal (*newtons per square meter*) dan merupakan standar pengukuran tekanan satu atmosfir yaitu 1013,25hPa (101,325 kPa) (Halliday,1985:560). Sebagai perbandingan pada permukaan laut memiliki tekanan udara sekitar 76cmHg atau setara dengan satu atmosfir (101,325kPa).

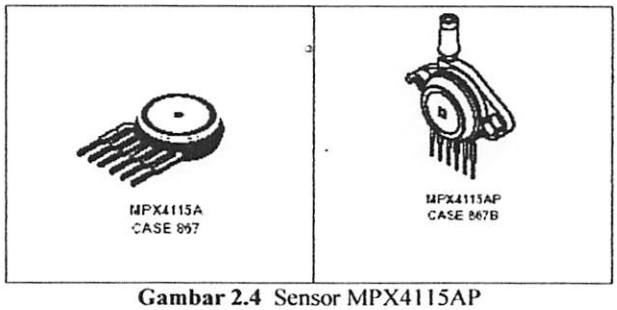
Secara garis besar sensor tekanan udara ini memiliki prinsip kerja sebagai berikut seperti ditunjukkan dalam Gambar 2.3;



Gambar 2.3 Bagian-bagian dari Sensor Tekanan
Sumber: *Anonymous*, 2001:3

Apabila ada tekanan udara yang masuk melalui lubang P, dimana tekanan tersebut lebih besar dari tekanan vacuum yang dipergunakan sebagai tekanan referensi, maka membran *fluoro silicon* akan melengkung ke bawah, dimana besar lengkungan ini sebanding dengan besar tekanan yang diterima. Lengkungan ini yang kemudian diolah oleh pengkondisi sinyal untuk kemudian dijadikan tegangan analog sebagai keluaran dari sensor melalui pin keluaran tegangan.

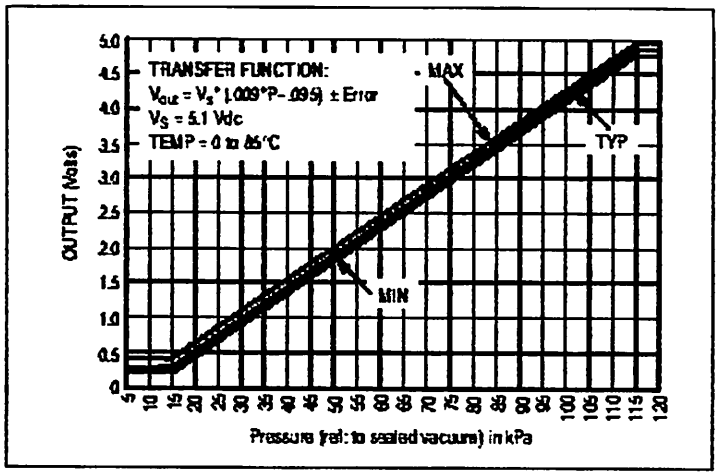
Sensor MPX4115AP memiliki bentuk yang kecil dengan kehandalan yang tinggi sehingga cocok dan ekonomis untuk digunakan seperti terlihat dalam Gambar 2.4:



Gambar 2.4 Sensor MPX4115AP
Sumber: *Anonymous*, 2001:1

Keluaran sensor yang berupa tegangan (volt) memiliki hubungan yang linier terhadap tekanan (kPa) di mana keluaran tegangan akan berubah dengan

perubahan tekanan udara, apabila tekanan semakin tinggi maka tegangan keluaran yang dihasilkan juga akan bertambah seperti terlihat dalam Gambar 2.5;



Gambar 2.5 Grafik Hubungan antara Output terhadap Tekanan
Sumber: *Anonymous*, 2001:3

Dari Gambar 2.5 terlihat bahwa pada tekanan 100kPa (1 atm), *pressure sensor* MPX4115AP akan menghasilkan tengangan keluaran sebesar 4,03 volt. Demikian pula untuk tekanan-tekanan berikutnya. Untuk mendapatkan perhitungan ketinggian digunakan persamaan

$$Z = -26126 * \ln\left(\frac{P(kPa)}{101{,}304}\right) \quad \text{.....(2.2)}$$

Sumber: Kerckhoff, 2001:1

dimana Z = ketinggian (feet)

P = Tekanan (kPa)

Berdasarkan *datasheet* sensor MPX4115AP, range tekanan 15kPa-115kPa dapat di prediksikan ketinggian dengan perhitungan sebagai berikut:

- 15kPa

$$Z = -26126 * \ln\left(\frac{15}{101,304}\right) = 49902 feet$$

dengan nilai 1 feet (ft) = 0,3048 meter maka

$$Z = 49902 * 0,3048 = 14970 meter$$

- 115kPa

$$Z = -26126 * \ln\left(\frac{115}{101,304}\right) = -3313 feet$$
$$= -994,11 meter$$

Sehingga sensor MPX4115AP memiliki jangkauan 3313 feet (994,11m) di bawah permukaan laut hingga 49902 feet (14970m) di atas permukaan laut. Sedangkan perhitungan untuk mendapatkan tegangan keluaran dari sensor adalah:

$$Vout = Vs * (0,009 * P(kPa) - 0,095) \pm error(datasheet) \quad \text{.....(2.3)}$$

Sumber: *Anonymous*, 2001:3

dimana Vout = Tegangan keluaran yang dihasilkan sensor (volt)

P = Tekanan (kPa)

Vs = Tegangan supply sensor tekanan (volt)

Dari spesifikasi alat ini dirancang dapat mengukur ketinggian 0m hingga 4095m dengan range tekanan udara 60kPa hingga 101,3kPa. Berdasarkan *datasheet* sensor MPX4115AP pada range tekanan udara tersebut, sensor MPX4115AP dapat menghasilkan tegangan keluaran pada kisaran 2,25 volt hingga 4,08 volt. Berikut perhitungannya:

- 60kPa

$$Vout = Vs * (0{,}009 * P(kPa) - 0{,}095)$$
$$= 5 * ((0{,}009 * 60) - 0{,}095) = 2{,}25volt$$

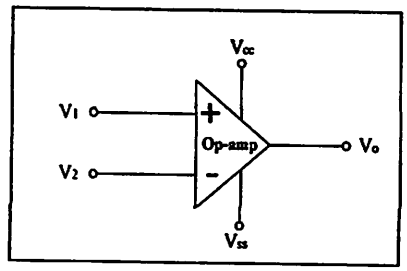
- 101,3kPa

$$Vout = Vs * (0{,}009 * P(kPa) - 0{,}095)$$
$$= 5 * ((0{,}009 * 101{,}3) - 0{,}095) = 4{,}08volt$$

Jadi pada range tekanan sebesar 60kPa hingga 101,3kPa, sensor MPX4115AP akan menghasilkan jangkauan tegangan 2,25 volt hingga 4,08 volt.

2.3 Penguat Operasional

Penguat operasional (op-amp) merupakan suatu komponen aktif yang terdiri dari rangkaian penguat gandengan langsung dengan penguatan tinggi yang dalam pengoperasiannya dilengkapi dengan umpan balik untuk memberikan tanggapan secara menyeluruh. Penguat ini mempunyai lima buah terminal dasar, diantaranya dua terminal untuk mencatu daya, dua terminal untuk isyarat masukan, dan satu terminal keluaran. Kedua terminal isyarat masukan masing-masing terminal masukan pembalik (*inverting input* (-)), dan terminal masukan tak membalik (*non-inverting input* (+)). Skematis dari op-amp diperlihatkan dalam Gambar 2.6



Gambar 2.6 Penguat operasional.
Sumber: Wasito, 1978: 128

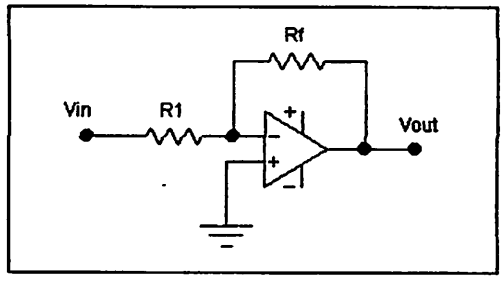
Jika pada kutub masukan tak membalik (V_1) diberi tegangan masukan, maka tegangan keluarannya akan sefasa dengan masukannya. Sebaliknya jika pada kutub masukan membalik (V_2) diberi tegangan masukan, maka tegangan keluarannya akan berlawan fasa dengan masukannya.

Suatu penguat operasional yang ideal mempunyai sifat-sifat sebagai berikut:

- Impedansi masukan = ~ (tak berhingga)
- Impendasi keluaran = 0 (nol)
- Penguatan = ~ (tak berhingga)
- Karakteristik tidak berubah tehadap suhu.
- Dapat menguatkan sinyal-sinyal DC.

2.3.1 Penguat Membalik (*Inverting*)

Berikut ini adalah merupakan salah satu contoh aplikasi dari penguat operasional (Op-amp) yang ditunjukkan dalam Gambar 2.7;



Gambar 2.7 Penguat *Inverting*
Sumber: Coughin, *1994: 33.*

Rangkaian penguat operasional di atas adalah rangkaian penguat *inverting*, yang mempunyai tegangan output sebesar:

$$Vout = -\left[\frac{Rf}{Ri}\right] x Vin \quad \text{.....(2.4)}$$

Sumber: Coughin, 1994: 34

Oleh karena harga faktor penguatan atau Av merupakan perbandingan antara tegangan keluaran dan tegangan masukan maka persamaan di atas dapat di sederhanakan menjadi:

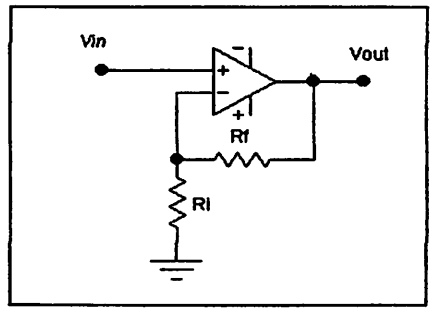
$$Av = \left[\frac{Vout}{Vin}\right] \quad \text{.....(2.5)}$$

Sumber: Coughin, 1994: 34

Berdasarkan persamaan di atas diketahui bahwa faktor penguatan atau Av adalah sangat besar dengan kemungkinan memiliki harga Av ≤ 1 dan Av ≥ 1.

2.3.2 Penguat Tak Membalik (*Non Inverting*)

Selain penguat *inverting* ada pula penguat *Non inverting* seperti ditunjukkan dalam Gambar 2.8 berikut ini;



Gambar 2.8 Penguat *Non Inverting*
Sumber: Coughin, 1994: 47

Dimana harga faktor penguatan atau Av memiliki persamaan sebagai berikut:

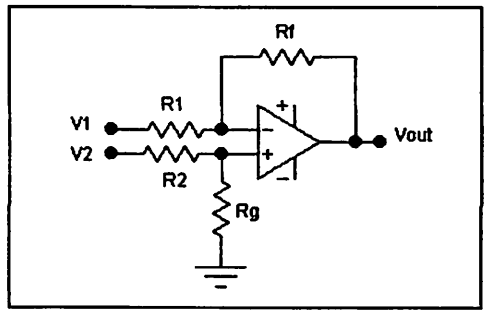
$$Av = \left[\frac{Rf}{Ri} + 1\right] \quad \text{.....(2.6)}$$

Sumber: Coughin, 1994: 46

Berdasarkan persamaan di atas dapat diketahui bahwa besarnya faktor penguatan atau Av dari penguat *non inverting* adalah selalu lebih besar dari satu atau dengan kata lain Av ≥ 1.

2.3.3 Penguat Selisih Tegangan dengan Penguatan (Penguat Differensial)

Penguat differensial memiliki keunggulan dibandingkan dengan penguat pembalik atau penguat tak membalik biasa. Penguat differensial bisa mengukur maupun memperkuat isyarat-isyarat kecil yang terbenam dalam isyarat-isyarat yang jauh lebih besar. (Coughin, 1994:161). Penguat ini dibuat dari sebuah penguat dengan empat tahanan. Terminal masukannya ada dua, masukan bertanda (-) dan masukan bertanda (+), dihubungkan dengan terminal op-amp yang terdekat. Seperti yang terlihat dalam Gambar 2.9.



Gambar 2.9 Penguat Selisih Tegangan
Sumber: Coughin, 1994: 162

Tegangan keluaran yang dihasilkan merupakan hasil kali penguatan dengan selisih tegangan diantara kedua masukan. Besarnya penguatan disesuaikan dengan nilai tahanan yang digunakan. Bila perbandingan *Rf* terhadap *R1* sama dengan perbandingan *Rg* terhadap *R2* maka tegangan keluaran dapat dihitung menggunakan Persamaan 2.9 sebagai berikut:

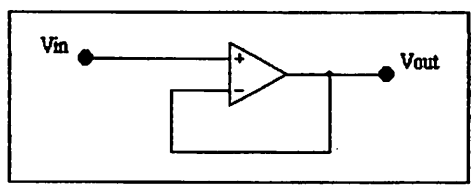
$$Vout = \frac{Rf}{R1}(V_2 - V_1) \quad \text{.....(2.9)}$$

Sumber: Coughin, 1994: 162

Penguat differensial ini memiliki keuntungan yakni kemampuan merasakan adanya tegangan diferensial kecil yang tersembunyi dalam tegangan sinyal besar. Namun, impedansi masukannya amat rendah, sehingga sering pada rangkaian ini perlu ditambahkan pengikut untuk penyangga atau mengisolasinya.

2.3.4 Rangkaian *Voltage Follower* (*Buffer*)

Rangkaian *voltage follower* atau sering dikenal sebagai rangkaian *buffer* adalah suatu rangkaian yang memiliki fungsi untuk mengisolasi masukan-masukannya supaya dihasilkan tegangan keluaran yang sama besarnya dengan tegangan masukan dengan kata lain polaritas tegangan keluaran sama dengan polaritas tegangan masukannya, seperti ditunjukkan dalam Gambar 2.10;



Gambar 2.10 Rangkaian *Voltage Follower*
Sumber: Coughin, 1994: 42

2.4 *Analog to Digital Coverter* (ADC)

Dalam sebuah pengukuran suatu variabel fisik yang pada umumnya bersifat analog dengan menggunakan piranti digital, diperlukan adanya pengubahan variabel digital yang nilainya proporsional dengan nilai variabel yang akan diukur. Hal-hal yang perlu diperhatikan dalam penggunaan ADC ini adalah metode pengubah sinyal analog ke sinyal digital yang digunakan, tegangan maksimum yang dapat dikonversikan oleh ADC dari rangkaian pengkondisi sinyal, resolusi, pewaktu eksternal ADC, tipe keluaran, ketepatan dan waktu konversinya.

Resolusi ADC adalah perubahan terkecil yang terjadi pada keluaran analog sebagai suatu hasil dari perubahan masukan digital. Resolusi selalu sama dengan bobot dari LSB atau disebut juga '*step size*' karena *step size* merupakan besarnya perubahan tegangan keluaran pada saat kode masukan berubah dari satu step ke step berikutnya. Adapun perhitungan resolusi ADC adalah sebagai berikut:

$$\Delta V_{OUT} = \frac{V_R}{2^n - 1} \qquad \text{.....(2.10)}$$

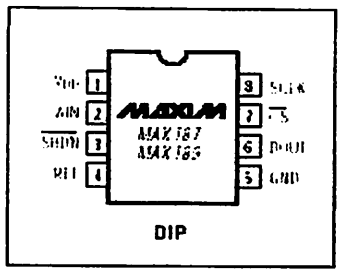
Sumber: Malvino, 1996: 337

dimana ΔV_{OUT} menyatakan perubahan tegangan terkecil pada keluaran analog (resolusi), V_R menyatakan tegangan referensi dan n menyatakan jumlah bit keluaran biner IC *analog to digital converter.*

Spesifikasi lain untuk ADC adalah waktu konversi (*conversion time*). Waktu konversi suatu ADC adalah waktu yang diperlukan ADC untuk menghasilkan kode biner yang valid untuk tegangan masukan yang diberikan.

Sebuah *converter* disebut berkecepatan tinggi jika memiliki waktu konversi yang pendek.

Dalam perencanaan dan pembuatan skripsi digunakan ADC MAX187 yang diproduksi oleh MAXIM Semiconductor. ADC ini digunakan untuk mengubah tegangan analog menjadi besaran digital 12-bit. MAX187 merupakan ADC yang memiliki keluaran serial 12-bit dengan konsumsi daya rendah dan beroperasi dengan menggunakan catu daya ±5 volt. Adapun konfigurasi pin ADC Serial 12-bit MAX187 ditunjukkan dalam Gambar 2.11.



Gambar 2.11 Konfigurasi pin ADC Serial 12-bit MAX187
Sumber: *Anonymous*, 1993:1

Fungsi dari masing-masing pin pada ADC serial 12-bit MAX187 dapat dilihat pada Tabel 2.1 di bawah ini;

Table 2.1. Fungsi PIN ADC Serial 12-bit

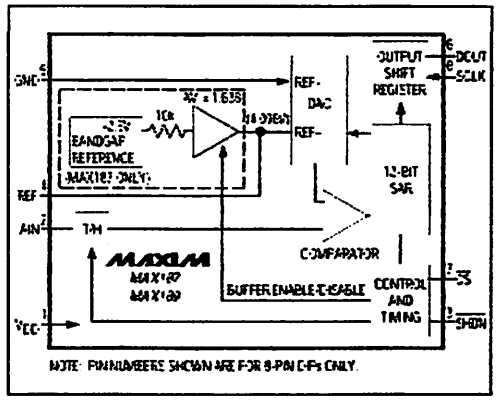
PIN	Nama	Fungsi
1	VDD	Tegangan supply 5 volt
2	AIN	Input analog
3	$\overline{SHDN}$	Input *shutdown* dimana untuk MAX187 SHDN *high* maka *enable* untuk referensi internal
4	REF	Tegangan referensi
5	GND	*Ground* digital dan analog
6	DOUT	Output data serial
7	$\overline{CS}$	*Chip select* aktif *low* yang akan memulai pengkonversian saat aktif turun
8	SCLK	Input serial *clock*

Sumber: Anonymous, 1993:7

ADC Serial 12-bit MAX187 ini memiliki beberapa karakteristik, yaitu:

1. Input analog yakni AIN. ADC ini beroperasi dengan tegangan Vcc = +5 volt dan input analognya mempunyai variasi range 0 sampai 5 volt.
2. Dapat mengkonversi tegangan masukan analog menjadi 12 bit tegangan keluaran digital, apabila menggunakan *referensi eksternal* sebesar 5 volt maka resolusinya adalah $\frac{5V}{2^{12}-1} = \frac{5V}{4095} = 1{,}22mV$ dan apabila menggunakan *referensi internal* sebesar 4,096 Volt maka resolusinya adalah $\frac{4{,}096}{2^{12}-1} = \frac{4{,}096V}{4095} = 1mV$
3. MAX187 merupakan *successive-approximation* ADC dengan waktu konversi (conversion time) 8,5 μs
4. Memiliki referensi internal V_{REF} = 4,096v dan dapat pula menggunakan referensi eksternal serta memiliki fasilitas internal clock f_{CLK} = 4,0 MHz.

Blok diagram dari ADC MAX187 ditunjukkan dalam Gambar 2.12.



Gambar 2.12 Blok Diagram ADC 12-bit MAX187
Sumber: *Anonymous*, 1993:1.

2.5 Minimum Sistem AT89S8252

2.5.1 Mikrokontroler AT89S8252

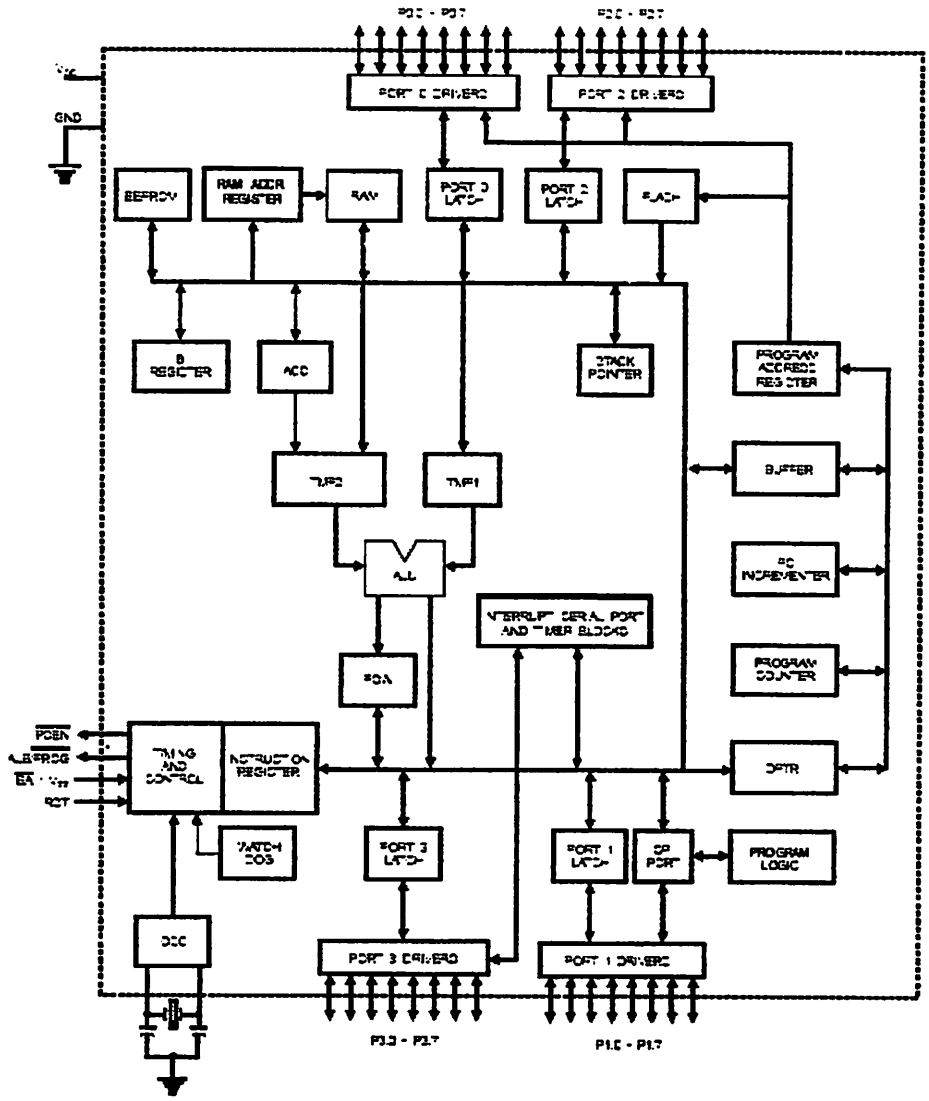
Pada dasarnya perbedaan antara mikroprosesor dan mikrokontroler adalah mikroprosesor adalah bagian CPU (Central Prosesing Unit) dari sebuah computer yang tidak dilengkapi dengan memori, I/O dan peripheral yang dibutuhkan oleh sistem yang lengkap, sedangkan mikrokontroler adalah kombinasi antara CPU dengan memori dan I/O dalam bentuk single chip. Keuntungan memakai mikrokontroler dibandingkan mikroprosesor adalah pada mikrokontroler terdapat RAM dan peralatan I/O pendukung.

Mikrokontroler AT89S8252 adalah mikrokrokontroller ATMEL yang kompatibel penuh dengan mikrokontroler keluarga 80C51, membutuhkan daya yang rendah, memiliki *performance* yang tinggi dan merupakan mikrokomputer 8 *bit* yang dilengkapi 2 Kbyte EEPROM (*Electrical Eraseable Programmable Read Only Memory*) dan 256 Byte RAM internal.

Adapun fasilitas yang dimiliki oleh mikrokontroler 80C51 ini antara lain:

1. *Central Processing Unit* (CPU) 8 *bit* dengan *register* A (Accumultor) dan *register* B
2. 16 *bit Program Counter* (PC) dan *Data Pointer* (DPTR)
3. 8 *bit Program Status Word* (PSW)
4. 2 K *byte internal* EEPROM
5. *256 byte internal* RAM
6. 32 pin input-output tersusun atas P0-P3, masing-masing 8 bit
7. 3 buah *timer / counter* 16 bit
8. *Receiver register data serial full duplex*: SBUF

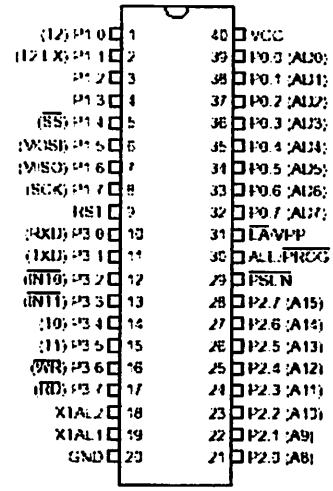
9. *Central Register* yaitu TCON, TMOP, SCON, PCON, IP dan IE
10. *Oscillator* dan *clock internal*
11. Dua buah *External interrupt*



Gambar 2.14 Blok Diagram Mikrokontroller Atmel AT89S8252

Sumber: *data sheet AT89S8252*

Susunan pin-pin mikrokontroler terdiri dari 40 pin, seperti pada gambar 2.15



Gambar 2.15. Konfigurasi pin AT89S8252

Sumber : Datasheet AT89S8252

1. *Vcc*

   Mikrokontroler AT89S8252 dioperasikan dengan tegangan supply +5V, yaitu pada pin 40.

2. *GND*

   Hubungan dengan ground adalah pin 20.

3. *Port 0*

   Port 0 (pin 32-39) merupakan saluran input/output yang bersifat dua arah Dalam rancangan sederhana, port ini digunakan sebagai port I/O dengan fungsi untuk berbagai keperluan. Sedangkan untuk rancangan yang lebih besar dimana ditambahkan memori dari luar, port ini berfungsi untuk memultipleks alamat memori dengan data.

4. *Port 1*

   Port 1 (pin 1-8) merupakan port I/O 8-bit yang bersifat dua arah. Port ini dapat digunakan untuk hubungan dengan peralatan luar bila diinginkan.

5. *Port 2*

   Port 2 (pin 21-28) merupakan port yang dapat digunakan untuk beberapa fungsi yaitu keperluan I/O, juga sebagai byte alamat selama penerimaan suatu data dari program memori eksternal dan saat akses ke data memori eksternal yang menggunakan alamat 16-bit (yaitu instruksi MOVX @ DPTR). Selama akses ke memori data eksternal yang menggunakan alamat (MOVX @ RI), maka port 2 akan mengeluarkan isi dari P2 *Special Function Register* (SPF).

6. *Port 3*

   Port 3 (pin 10-17) merupakan port paralel 8 bit yang bersifat dua arah dan mempunyai fungsi ganda, dimana setiap pin mempunyai keistimewaan yang dimiliki AT89S8252 seperti pada tabel 2-2

Tabel 2-2. Fugsi Pengganti Dari Port 3

IN	FUNGSI
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	*T0 (timer 0 external input)*
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

Sumber : Data Sheet Atmel 89S8252

7. *Reset (RST)*

   Reset input berada pada pin nomor 9. Piranti akan mengalami reset saat terdapat logika high '1' pada pin 9 dan osilator bekerja.

8. *ALE/$\overline{PROG}$*

   Pin ALE/$\overline{\text{PROG}}$ terdapat pada pin 30. ALE berfungsi untuk menahan alamat bit rendah selama berlangsungnya akses ke memori eksternal. Pin ini juga merupakan input dari sinyal program ($\overline{\text{PROG}}$) selama program Flash bekerja.

9. *$\overline{PSEN}$*

   Program Store Enable adalah sinyal kontrol dari memori program eksternal. Ketika AT89S8252 mengeksekusi kode dari memori program eksternal, $\overline{\text{PSEN}}$ diaktifkan dua kali setiap mesin aktif, kecuali bila diloncati selama akses ke memori data eksternal.

10. $\overline{EA}$ */ Vpp*

EA (*External Access Enable*) harus dihubungkan dengan GND untuk mengaktifkan program eksternal dan harus dihubungkan dengan V_{CC} saat terjadi eksekusi program secara internal. Pin ini juga menerima V_{PP} (programming enable voltage) selama pemrograman Flash, untuk komponen yang memerlukan 12 V_{PP}.

11. XTAL 1

Merupakan input dari penguat osilator dan clock internal untk pengoperasian rangkaian.

12.XTAL 2

Merupakan out put dari penguat pembalik osilator.

Keluarga MCS®51 yang diproduksi Intel mempunyai konfigurasi yang berbeda-beda sesuai dengan jenisnya. Masing-masing jenis saling kompatibel serta mempunyai kelebihan tersendiri. Misalnya mikrokontroler AT89S8252 merupakan padanan dari mikrokontroler 8051, tetapi tidak memiliki ROM internal. Tabel 2-3 memperlihatkan sebagian dari keluarga MCS®51.

Tabel 2-3. Keluarga MCS®51

Tipe	Tipe tanpa EPROM	Tipe ber-EPROM	Kapasitas ROM	Kapasitas RAM	*Port* I/O	Pewaktu
8051	8031	-	4K	128	4	2
8051AH	*8031AH*	*8751H*	4K	*128*	4	2
8052AH	8032AH	8752BH	8K	256	4	3
80C51BH	80C31BH	87C51	4K	128	4	2
80C52	80C32	-	8K	256	4	3
83C51FA	80C51BH	8751FA	8K	256	4	3
83C51FB	80C51FB	87C51FB	16K	256	4	3
83C152	80C152	-	8K	256	5	3

Sumber : Bereksperimen DenganMikrokontroller 8031, 5.

a). *Organisasi Memori*

Organisasi memori pada mikrokontroler AT89S8252 dapat dibagi menjadi dua bagian besar yaitu memori program dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpanan data maupun program. Memori program digunakan untuk menyimpan instruksi-instruksi yang akan dijalankan oleh mikrokontroler, sedangkan memori data digunakan sebagai tempat penyimpanan data yang sedang diolah mikrokontroller.

Program mikrokontroler disimpan dalam memori program berupa ROM. Mikrokontroler AT89S8252 dilengkapi dengan ROM internal namun untuk program yang besar digunakan ROM eksternal yang terpisah dari mikrokontroler.

Untuk dapat menggunakan memori program eksternal ini penyemat /EA dihubungkan dengan penyemat V_{SS} (logika 0).

Memori program mikrokontroler menggunakan alamat 16 *bit* mulai 0000_H-$FFFF_H$, sehingga kapasitas penyimpanan program maksimal adalah 2^{16} *byte* atau 64 Kb. Sinyal yang digunakan untuk membaca memori program eksternal adalah sinyal /PSEN (*program store enable*).

Selain memori program mikrokontroler AT89S8252 juga memiliki memori data internal berkapasitas 128 *byte* dan mampu mengakses memori data eksternal sebesar 64 Kb. Semua memori data internal dapat dialamati dengan pengalamatan langsung atau tidak langsung. Ciri dari pengalamatan langsung adalah *operand* berisi alamat data yang diolah. Sedangkan ciri dari pengalamatan tidak langsung adalah *operand* adalah alamat *register* yang berisi alamat data yang akan diolah. Sebagian memori tersebut dapat dialamati dengan pengalamatan register, dan sebagian lagi dapat dialamati dengan memori satu *bit*. Untuk membaca data digunakan sinyal /RD, sedangkan untuk menulis data digunakan sinyal /WR.

b). Register Fungsi Khusus

Mikrokontroler ini mendapat register tambahan antara lain T2CON (Timer 2 register dengan alamat 0C8H),T2MOD (Timer 2 mode dengan alamat 0C9H),WMCON (Watchdog and memory control register dengan alamt 96H), SPCR (SPI control register dengan alamt D5H), SPSR (SPI status register dengan alamat AAH), SFDR (SPI data register dengan alamat 86H) register fungsi khusus (*Special Function Register)* terletak pada 128 *byte* bagian atas memori data

internal dan berisi *register-register* untuk pelayanan *latch port, timer, program status words, control peripheral* dan sebagainya, seperti pada Tabel 2-4.

Register-register ini hanya dapat diakses dengan pengalamatan langsung. Enam belas alamat pada register fungsi khusus dapat dialamati per*bit* maupun per-*byte* dan terletak pada alamat 80_H-FF_H. Secara perangkat keras, register fungsi khusus ini dibedakan dengan memori data internal.

Tabel 2-4. Nama dan Alamat Register pada Register Fungsi Khusus

Simbol	Nama Register	Nilai pada saat reset	Alamat
ACC	*Accumulator*	0000_H	$0E0_H$
B	*Register B*	00_H	$0F0_H$
PSW	*Program Status Word*	00_H	$0D0_H$
SP	*Stack Pointer*	07_H	81_H
DPTR	*Data Pointer 2 bytes*		
DPL	*Low bytes*	0000_H	82_H
DPH	*High bytes*	0000_H	83_H
P0	*Port 0*	FF_H	80_H
P1	*Port 1*	FF_H	90_H
P2	*Port 2*	FF_H	$0A0_H$
P3	*Port 3*	FF_H	$0B0_H$
IP	*Interrupt priority control*	$XXX00000_B$	$0B8_H$
IE	*Interupt enable control*	$0XX00000_B$	$0A8_H$
TMOD	*Timer/counter mode control*	00_H	89_H
TCON	*Timer/counter control*	00_H	88_H
TH0	*Timer/counter 0 high byte*	00_H	$8C_H$
TL0	*Timer/counter 0 low byte*	00_H	$8A_H$
TH1	*Timer/counter 1 high byte*	00_H	$8D_H$
TL1	*Timer/counter 1 low byte*	00_H	$8B_H$
SCON	*Serial control*	00_H	98_H

SBUF PCON	*Serial data buffer* *Power control*	Independen HMOS $0XXXXXXX_B$ CHMOS $0XXX0000_B$	99_H 87_H
WMCON	*Memory control / timer*	$0000\ 0000_B$	96H
SPI	*SerialPeripheral inrerface*	$0000\ 0000_B$	AAH

Sumber : Bereksperimen Dengan Mikrokontroller AT89S8252.

Beberapa macam register fungsi khusus yang sering digunakan, dijelaskan sebagai berikut :

- *Accumulator* (ACC) merupakan *register* untuk penambahan dan pengurangan. Perintah *Mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register* B merupakan *register* khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Program Status Word* (PSW) terdiri dari beberapa *bit* status yang menggambarkan kejadian di akumulator sebelumnya. Yaitu *carry bit*, *auxiliary carry*, dua *bit* pemilih bank, bendera *overflow*, *parity bit*, dan dua bendera yang dapat didefinisikan sendiri oleh pemakai.
- *Stack pointer* (SP) merupakan *register* 8 *bit* yang dapat diletakkan di alamat manapun pada RAM internal. Isi *register* ini ditambah sebelum data disimpan, selama instruksi PUSH dan CALL. Pada saat *reset*, *register* SP diinisialisasi pada alamat 07_H, sehingga *stack* akan dimulai pada lokasi 08_H.

- *Data pointer* (DPTR) terdiri dari dua *register*, yaitu untuk *byte* tinggi (*Data pointer high*, DPH) dan *byte* rendah (*Data pointer Low*, DPL) yang berfungsi untuk mengunci alamat 16 *bit*.
- *Port* 0 sampai *port* 3 merupakan *register* yang berfungsi untuk membaca dan mengeluarkan data pada *port* 0, 1, 2, 3. Masing-masing *register* ini dapat dialamati per-*byte* maupun per-*bit*.
- *Serial data buffer* (SBUF) merupakan dua *register* yang terpisah, *register buffer* pengirim dan sebuah *register buffer* penerima. Meletakkan data pada SBUF berarti meletakkan pada *buffer* pengirim yang akan mengirimkan data melalui transmisi serial. Membaca data SBUF berarti menerima data dari *buffer* penerima.
- *Control register* terdiri dari *register* yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua register khusus, yaitu register IP (*interrupt priority*) dan *register* IE (*Interrupt Enable*). Untuk mengontrol pelayanan *timer/counter* terdapat *register* khusus, yaitu *register* TCON (*timer/counter control*) serta untuk pelayanan *port* serial menggunakan *register* SCON (*serial port control*)

c). Port Masukan dan Keluaran

Mikrokontroler AT89S8252 mempunyai 4 *port* dan masing-masing *port* terdiri dari 8 saluran *bit*. Keempat *port* ini bersifat *bidirectional* yaitu dapat digunakan sebagai masukan atau keluaran. *Port* 0 digunakan sebagai saluran data yang dimultipleks dengan saluran alamat rendah untuk mengakses memori eksternal, baik memori program maupun memori data. *Port* 2 mengeluarkan

bagian alamat tinggi untuk mode pengalamatan memori 16 *bit*. *Port* 1 dan 3 berfungsi sebagai saluran masukan dan keluaran multi fungsi.

d). Sistem Interupsi

Mikrokontroler AT89S8252 mempunyai dua sumber interupsi eksternal dan sumber interupsi internal yang dapat diprogram agar sensitif terhadap perubahan level atau transisi. Interupsi *timer* aktif saat *register timer* yang bersangkutan mengalami *rollover*, interupsi serial akan aktif pada saat mikrokontroler mengirim/menerima data. Setiap sumber interupsi dapat diaktifkan/dimatikan melalui perangkat lunak.

2.5.2 Memori

Memori dalam suatu sistem mikrokontroler merupakan suatu piranti yang berfungsi untuk menyimpan program dan data yang dibutuhkan oleh mikrokontroler. Memori secara garis besar dibagi menjadi dua macam yaitu memori yang hanya dapat dibaca (*Read Only Memory*) dan memori yang dapat dibaca maupun ditulisi (*Random Access Memory*).

a. Read Only Memory (*ROM*)

ROM adalah suatu bentuk memori yang hanya dapat dibaca isinya. Isi ROM tidak mudah dihapus atau tidak mudah hilang meskipun catu daya tidak diberikan padanya. Karena sifatnya yang tidak mudah dihapus tersebut ROM disebut juga memori *non volatile* (tidak mudah menguap). Suatu program atau data statis yang diinginkan agar tidak mudah hilang dapat disimpan dalam ROM. Menurut sifatnya ROM dapat dibagi menjadi beberapa macam, yaitu :

- PROM (*Programmable Read Only Memory*) yaitu jenis ROM yang sekali ditulisi dan tidak dapat dihapus kembali.
- EPROM (*Erasable Programmable Read Only Memory*) yaitu jenis ROM yang dapat ditulisi maupun dihapus kembali. Menurut cara penghapusannya EPROM dapat dibagi menjadi dua yaitu UV-EPROM (*Ultra Violet* EPROM) dan EEPROM (*Electrically* EPROM).

b. Random Access Memory (*RAM*)

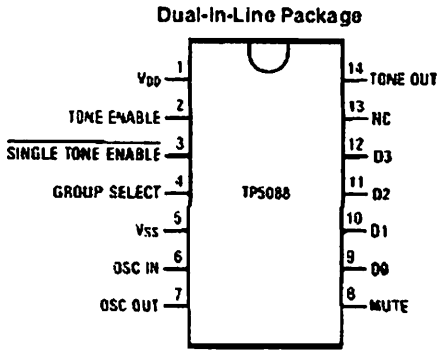
RAM adalah memori yang dapat dibaca maupun ditulisi. Menurut sifatnya RAM biasa disebut sebagai memori yang mudah menguap (*volatile*), yaitu bila catu daya yang diberikan pada RAM dihilangkan, maka data pada RAM akan hilang. Ada dua macam RAM yaitu :

- RAM statik yaitu RAM yang tersusun atas flip-flop. Selama catu daya diberikan pada RAM, maka data akan tetap tersimpan.
- RAM dinamik yaitu RAM yang menggunakan kapasitor sebagai penyimpan data. RAM ini memerlukan penyegaran data karena sifat kapasitor dapat menurun muatannya.

2.6 Encoder DTMF (TP5088).

IC TP 5088 merupakan jenis encoder DTMF yang merupakan perangkat CMOS yang dapat menghasilkan tone-dialing yang dalam aplikasinya yang dapat digunakan pada hubungan telpon. IC ini dapat dikontrol oleh microkontroler data input yang berupa 4 buah data biner akan dikodekan secra langsung tanpa memerlukan konversi untuk mensimulasikan input keyboard yang dibutuhkan

oleh pembangkit DTMF standart. Terdiri dari 14 pin dengan konfigurasi pin dapat dilihat pada gambar berikut :



Gambar 2.15 Konfigurasi Pin IC TP 5088
Sumber : *Data Sheet National Semikonduktor TP5088, hal 3.*

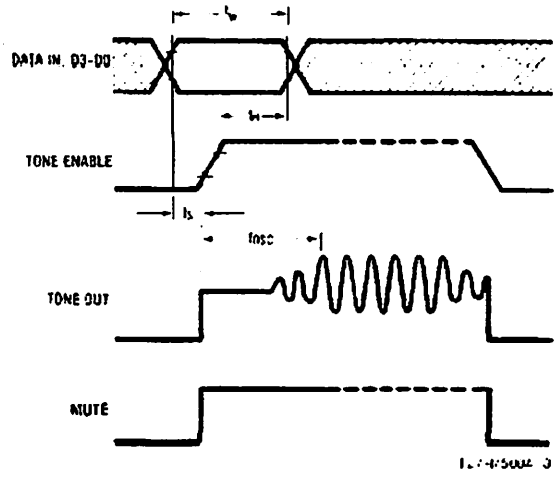
Fungsi pin-pin tersebut adalah :

Tabel 2.5 Diskripsi fungsi dari pin-pin TP5088

Pin	Nama	Keterangan
1,5	VDD & VSS	Merupakan penyemat catu daya, VDD dihubungkan dengan catu daya positif dan VSS pada ground.
6,7	OSC IN – OSC OUT	Kaki ini dihubungkan dengan kristal atau sumber osilator dari luar. Nilai kristal sebesar 3,579545 MHz
2	TONE ENABLE	*Input ini mempunyai sebuah resistor puul up* internal. Ketika Tone Enable dalam kondisi Low, osilator akan diberhentikan sehingga tone generator mati. Perubahan logika '0' ke logika '1' pada tone enable menahan data dari D0-D3. Osilator akan mulai bekerja dan tone generator kontinyu sampai Tone Enable ke keadaan low.
9,10,11,12	D0 – D3	Kaki ini merupakan input untuk data biner yang dikodekan, yang ditahan pada sisi naik oleh tone enable.
14	TONE OUT	Output ini merupakan open emitor dan transistor NPN, kolektor secara internal dihubungkan ke VDD. Ketika beban resisitor eksternal dihubungkan tone out ke VSS, maksimum tegangan pada kaki ini merupakan penjumlahan dari group tone low dan high. Pada saat tidak membangkitkan tone output, transistor ini akan mati.

Sumber: *Data Sheet National Semikonduktor.*

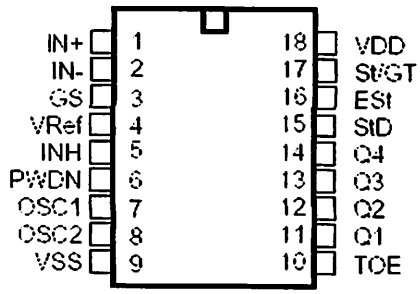
DIAGRAM WAKTU DARI TP5088



Gambar 2.16 diagram waktu operasi encoder DTMF
Sumber : *Data Sheet IC TP5088 National Semikonduktor, hal 4*

2.7 Decoder DTMF.

Decoder DTMF (Dual Tone Multi Frekwensi) adalah rangkaian yang dapat merespon kode-kode sinyal DTMF. IC jenis MT8870C adalah rangkaian decoder yang berfungsi menterjemahkan kode DTMF 16 digit sesuai standart DTMF menjadi keluaran kode biner 4 bit.gambar skema blok IC MT8870C diperlihatkan pada gambar berikut :



Gambar 2.17 Konfigurasi Pin IC MT8870
Sumber : *Data Sheet MITEL 8870,hal 2*

Keterangan pin-pin Decoder DTMF:

Table 2.6 diskripsi fungsi dari pin-pin MT8870

Pin	Nama	Keterangan
1	IN +	Non inverting input op-amp
2	IN -	Inverting input op-amp
3	GS	Pemilihan besarnya gain untuk sinyal dari luar
4	Vref	*Voltage referensi* biasanya besarnya VDD/2 *(output)*
7	OSC1	**Clock input**
8	OSC2	*Clock output*, frekuensi keluaran 3,579545 Mhz
9	VSS	*Ground*, Biasanya 0 Volt.
10	TOE	*Tristate Output Enable*, mengaktifkan atau tidak
11....14	Q0 – Q3	*Output* data yang dikeluarkan
15	STD	Jika logika tinggi pada pin ini maka data *output Valid*
16	Est	Saat nilai input benar maka keluaran logika tinggi.
17	St / Gt	*Streeung / guard time*, menentukan kecepatan nada.
18	VDD	*Supply* tegangan positif, biasanya 5 volt

Sumber : *Data Sheet MITEL*

STD merupakan output yang menandakan MT8870 mempunyai data baru yang bias diambil. STD akan bernilai '1' jika ada nada yang masuk dan akan tetap bertahan sampai nada tersebut masih ada. TOE merupakan input untuk mengatur data di D0...D3 jika TOE bernilai '1' data output bias diambil.

Berikut adalah konfigurasi penyemat MT8870C:

Table 2.7 konfigurasi penyemat MT8870C

Digi	TOE	INH	ESI	Q_4	Q_3	Q_2	Q_1
ANY	L	X	H	Z	Z	Z	Z
1	H	X	H	0	0	0	1
2	H	X	H	0	0	1	0
3	H	X	H	0	0	1	1
4	H	X	H	0	1	0	0
5	H	X	H	0	1	0	1
6	H	X	H	0	1	1	0
7	H	X	H	0	1	1	1
8	H	X	H	1	0	0	0
9	H	X	H	1	0	0	1
0	H	X	H	1	0	1	0
*	H	X	H	1	0	1	1
#	H	X	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0
A	H	H	L	undetected, the output code will remain the same as the previous detected code			
B	H	H	L				
C	H	H	L				
D	H	H	L				

Sumber : *data Sheet MT8870, hal 4*

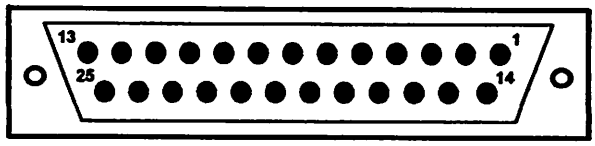
2.8. Paralel Port LPT1

Paralel port LPT1 dapat dijumpai pada CPU, yang biasanya digunakan sebagai port untuk mengendalikan printer. Port ini pada computer type lama biasanya merupakan suatu card tersendiri (I\O), dan pada computer generasi baru

sudah terintegrasi menjadi satu dengan mainboardnya. Port LPT1 ini berbentuk sebuah soket DB-25 yang terdapat pada bagian belakang sebuah komputer.

Paralel port LPT1 Data Port, Status Port dan Control Port yang masing-masing memiliki alamat 378H, 379H, 37AH dan terdapat dalam bentuk DB-25. Data port yang memiliki alamat 378H ini jika dioperasikan pada mode normal hanya dapat bersifat mengeluarkan data saja (out) sebanyak 8 bit dan tidak dapat digunakan sebagai port imput. Status Port yang beralamat pada 379H, terdiri dari 5 bit yang hanya sebagai port input saja. Sedangkan Control Port yang beralamatkan pada 37AH, terdiri dari 4 bit saja dan dapat bersifat sebagai input atau output (bidirectional). Untuk dapat menggunakan port ini, dalam program harus kita masuksn alamat untuk inisialisasinya, dan untuk mengaktifkan port LPT1 ini, sekaligus mengolah data yang diterima dari port LPT1 ini digunakan software.

Penggunaan port paralel pada PC identik dengan port printer, disebabkan karena port paralel yang tersedia memang dirancang untuk output ke printer. Port ini sebenarnya salah satu port paralel yang tersedia yaitu LPT0, LPT1 dan LPT2. yang dimaksud dengan port printer tersebut adalah LPT1. slot untuk port printer ini dengan mudah ditemukan disetiap computer dalam bentuik DB-25.



Gambar 2.18 DB25

Port paralel yang baru, distandarisasi dengan standar IEEE.1284 yang dikeluarkan pada tahun 1984. standar ini mendefinisikan 5 macam mode operasi sebagai beriku;

1. mode Kompabilitas
2. mode Nibel
3. mode Byte
4. Mode EPP (Enhanced Parallel Port),
5. Mode ECP (Extended Capabilities Port)

Tujuan standarisasi ini untuk membantu merancang penggerak (driver) dan piranti yang baru yang kompatibel antara satu dengan yang lainnya serta kompatibel mundur (backwards) dengan SPP (standar Parallel Port).

Dari lima macam mode operasi untuk LPT1 diatas, yang paling banyak dijumpai pada PC keluaran terbaru adalah mode EPP + ECP, sedangkan mode yang lain sudah diwakili dalam mode SPP (standar pParallel Port). Namun dalam mode EPP sendiri juga memuat alamat fisik dari mode SPP, sehingga pada seting bios dari PC umumnya diseting pada mode EPP atau EPP-ECP. EPP sebagai salah satu pilihan mode LPT1 banyak digunakan secara luas untuk peraltan yang sifatnya non-printer, seperti CD-ROM External, Tape Srive, Hard Drive dan lain-lain.

Register pada EPP tersusun dari 8 Byte alamat di memori (ofsfset), sehingga terdapat lebih banyak register pada EPP jika dibandingkan dengan SPP. Hal ini wajar mengingat lebih banyak peripheral yang dipasang pada EPP agar dapat bekerja dengan baik. Sebagian dari register EPP identik denganregister SPP,

yakni 3 byte awalnya (data, status, contol), sedangkan 5 byte berikutnya unik milik EPP. Table 2.8 berikut menyajikan register pada EPP.

Tabel 2.8 EPP software Register

Address	**Nama Port**	**Read/Write**
Base + 0	Data Port (SPP/EPP)	Write
Base + 1	Status Port (SPP/EPP)	Read
Base + 2	Control Port (SPP/EPP)	Write
Base + 3	Address Port (EPP)	Read/Write
Base + 4	Data Port (EPP)	Read/Write
Base + 5	Tak terdefinisi (16/32 bit transfer	----------
Base + 6	Tak terdefinisi (32 bit transfer)	----------
Base + 7	Tak terdefinisi (32 bit transfer)	----------

Tiga register yang tersisa yakni Base+5, Base+6 dan Base+7 dapat digunakan untuk operasi baca dan tulis (16 dan 32 bit) jika port yang ada memang support untuk itu. Parallel Port hanya dapat memuat 8 bit data dalam satu kali siklus proses, dengan demikian jika ada data 32 atau 16 bit yang dituliskan pada Parallel Port, data tersebut akan di split ke dalam ukuran byte untuk kemudian dikirim melalui 8 jalur data Parallal Port.

Sedangkan untuk pin-pin dari DB25, karena menggunakan mode EPP maka sangat perlu untuk mengerti definisi dari pin-pin DB25 dalam mode EPP. Pada saat mengginakan mode EPP, fungsi dan nama dari masing-masing jalur

didefinisikan ulang. Definisi dari pin-pin parallel port dapat dilihat pada table 2.9 berikut:

Tabel 2.9 Sinyal EPP dan SPP

Pin	SPP Signal	EPP Signal	In/Out	Function
1	Strobe	Write	Out	Kondisi Low berarti proses Write, High berarti proses Read
2-9	Data 0-7	Data0-7	In-Out	Data bus dua arah
10	Acknowledge	Interupt	In	INTERUPT Line. Interupt dijalankan pada saat menuju positif (Positif Rising Edge)
11	Busy	Wait	In	Untuk *handshaking*. Proses EPP dimulai bila kondisi Low dan selesai bila High
12	Paper Out/End	Spare	IN	Kosong. Tidak diginakan pada proses *handshake*
13	Select	Spare	In	Kosong. Tidak digunakan pada proses handshake
14	Auto Linefeed	Data Strobe	Out	Low berarti ditransfer
15	Error/Fault	Spare	In	Kosong. Tidak diginakan pada proses *handshake*
16	Initialize	Reset	Out	Reset. Aktif low
17	Select Printer	Address Strobe	Out	Saat low berarti Address di transfer
18-25	Ground	Ground	Gnd	Ground

Untuk pin *paper out*, *select* dan *Error* dalam proses EPP handshake tidak didefinisikan. Jalur-jalur tersebut masih dimanfaatkan oleh pemakai untuk keperlua yang lain. Status dari jalur-jalur tersebut dapat digunakan dengan melihat pada SPP Status Register.

Sebelum merancang hardware dan meng *–interface*-kannya dengan LPT1, perlu dilakukan pemahaman terhadap perangkat keras LPT1 itu sendiri. Chip dari parallel port pada umumnya sudah dalam satu IC ASIC (*Application Specific Integrated Circuit*) namun teori dan cara kerjanya sama.

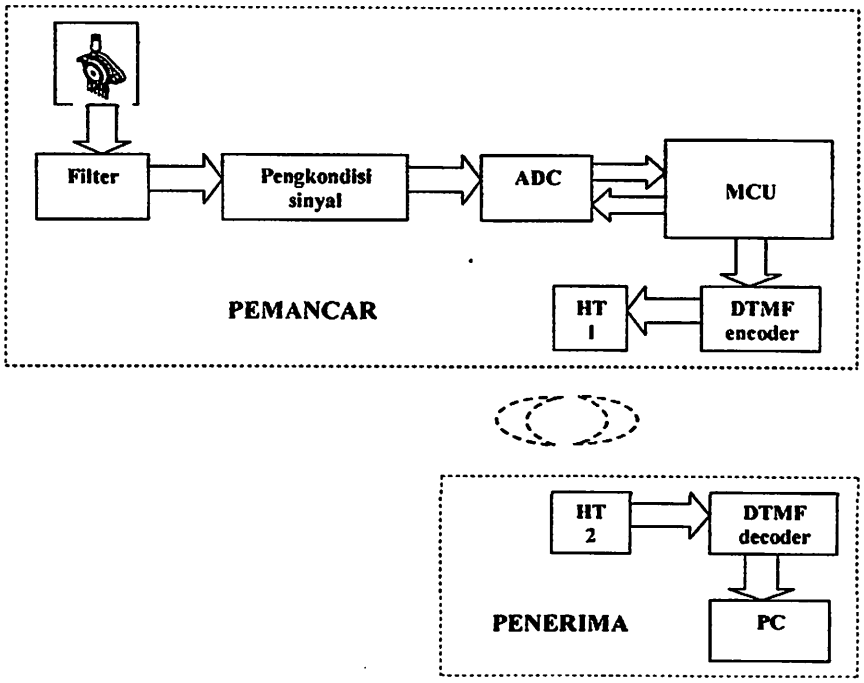
BAB III

PERENCANAAN DAN PEMBUATAN ALAT

3.1 Pendahuluan

Pada bab ini membahas tentang pengendalian peralatan yang dikendalikan dengan menggunakan mikrokontroler AT89S8252. Perencanaan ini meliputi perencanaan kerja sistem rangkaian pada blok diagram, perencanaan perangkat keras dan perencanaan perangkat lunak yang mengintegrasikan kerja seluruh sistem Perancangan ini dibuat tahap demi tahap sesuai dengan blok diagram seperti pada gambar 3.1.

3.2 Blok Diagram Rangkaian



Gambar 3.1 Diagram Blok Sistem

Dari Blok diagram diatas dapat dijelaskan mengenai bagian-bagian yang menyusun keseluruhan sistem dari alat ini di antaranya:

1) Sensor Tekanan

Sensor yang digunakan pada alat ini adalah sensor tekanan udara (*pressure sensor*) dengan tipe MPX4115A yang memiliki sensitivitas sebesar 45.9mV/kPa (*datasheet*). Sensor ini digunakan untuk mendeteksi setiap perubahan tekanan udara disekitar di mana akan menghasilkan sinyal-sinyal tegangan analog yang akan menjadi masukan bagi ADC, yang sebelumnya melewati rangkaian pengkondisi sinyal.

2) Filter

Filter ini berfungsi untuk mengurangi osilasi output dari sensor tekanan.

3) Pengkondisi Sinyal

Pengkondisi sinyal disini berupa rangkaian yang digunakan untuk mengkondisikan sinyal output dari filter agar kompatibel dengan ADC.

4) Analog to Digital Converter (ADC)

ADC disini berfungsi sebagai pengkonversi (*converter*) tegangan analog menjadi data-data digital agar dapat diproses oleh Mikrokontroller.

5) MCU (Mikrokontroller)

MCU yang digunakan disini memiliki beberapa fungsi diantaranya; memberikan instruksi pada ADC untuk mengkonversikan sinyal analog menjadi data digital, mengolah data output dari ADC, kemudian memberikan instruksi pada DTMF (Encoder) untuk mengubah data digital menjadi sinyal DTMF agar dapat dikrim oleh HT 1.

6) DTMF (Encoder)

Berfungsi menerjemahkan output mikro agar dapat dikrimkan oleh HT 1.

7) HT 1 dan HT 2

Digunakan sebagai media komunikasi pengirim dan penerima data

8) DTMF (Decoder)

Berfungsi menarjemahkan sinyal yang dikirim oleh HT 1 dan diterima oleh HT 2 agar dapat ditampilkan oleh PC.

9) PC

Menampilkan ketinggian gelombang air laut (display)

Metode yang digunakan dalam pengukuran ketinggian gelombang air laut ini adalah dengan mendeteksi perubahan tekanan udara pada tempat tersebut. Perubahan tekanan udara tersebut dapat dideteksi dengan menggunakan sebuah sensor yang diproduksi oleh Motorola Inc. MPX4115APP. Sensor tersebut dapat menghasilkan keluaran berupa tegangan yang sebanding dengan tekanan udara yang dideteksinya.

Tegangan yang dihasilkan dari sensor tersebut kemudian diumpankan ke sebuah rangkaian *low pass* RC (*Resistor Capacitor*) filter untuk mengurangi *noise* yang dihasilkan dari sensor itu sendiri. Kemudian keluaran dari filter tersebut dihubungkan dengan rangkaian pengkondisi sinyal agar keluaran dari sensor tekanan dapat di baca oleh ADC. Adapun fungsi ADC pada alat ini adalah untuk mengkonversikan perubahan sinyal-sinyal analog yang dihasilkan rangkaian pengkondisi sinyal menjadi data-data digital. Data-data digital tersebut kemudian langsung diumpankan ke mikrokontroller AT89S8252 untuk diolah, dikonversikan dan mikrokontroller akan memberikan instruksi DTMF (encoder)

untuk mengirimkan sinyal melalui HT1 dan diterima oleh HT2 kemudian dikonversikan kembali oleh DTMF (decoder) untuk ditampilkan ke PC berupa angka-angka desimal dalam satuan meter.

3.3 Perencanaan Bagian Perangkat Keras

Dari Gambar 3.1 blok diagram sistem dan uraian di atas maka perencanaan dari masing-masing bagian (blok) dapat diuraikan sebagai berikut:

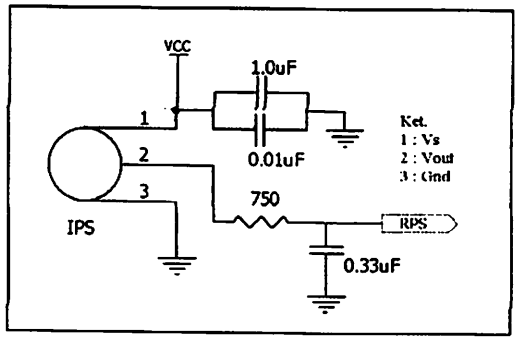
Perencanaan bagian perangkat keras (*hardware*), yaitu perencanaan;

- Bagian sensor dan filternya
- Bagian pengkondisi sinyal
- Bagian pengkonversi sinyal analog ke digital (ADC Serial 12-bit)
- Bagian kontrol dan pengolah data (mikrokontroller AT89S8252)
- Bagian Pengiriman (DTMF encoder TP5088)
- Bagian Penerima (DTMF decoder MT8870)

3.3.1 Perencanaan Bagian Sensor

Pada bagian sensor ini digunakan sensor MPX4115APP yang diproduksi oleh Motorola Inc. Sensor ini akan menghasilkan sinyal keluaran analog berupa tegangan apabila dideteksi tekanan udara pada tempat tersebut. Tegangan keluaran yang dihasilkan sensor ini berada pada range 0,2 volt – 4,8 volt dengan range tekanan 15 kPa – 115 kPa dan memiliki sensitivitas sebesar 45,9 mV/kPa (Anonymous: 2001:1).

Pada perencanaan sensor ini dilakukan berdasarkan *datasheet* sensor dan *application note* MPX4115AP seperti terlihat dalam Gambar 3.2.



Gambar 3.2 Rangkaian Sensor MPX4115AP

Dari Gambar 3.2 diatas terlihat bahwa keluaran dari *Integrated Pressure Sensor* (IPS) pada pin 3 langsung dihubungkan dengan rangkaian *low pass* RC filter. Menurut *datasheet* sensor MPX4115AP direkomendasikan untuk menggunakan *low pass* RC filter dengan frekuensi *cutoff* sebesar 650Hz (Anonymous: 2001:2), yang berfungsi untuk mengurangi *noise* yang dihasilkan oleh sensor itu sendiri. Sehingga perhitungan nilai yang digunakan adalah sebagai berikut:

Untuk mendapatkan nilai frekuensi, Nilai C = 0,33uF, maka:

$$fc = \frac{1}{2\pi RC} \rightarrow R = \frac{1}{2\pi \cdot C \cdot fc} = \frac{1}{2\pi \cdot 0{,}3uF \cdot 650Hz} = 742{,}35 \approx 750\Omega$$

Dari spesifikasi alat ini dirancang dapat mengukur ketinggian 0m hingga 4095m dengan range tekanan udara 60,5kPa hingga 101,3kPa. Berdasarkan *datasheet* sensor MPX4115AP pada range tekanan udara tersebut, sensor MPX4115AP dapat menghasilkan tegangan keluaran pada kisaran 2,25 volt hingga 4,08 volt. Berikut perhitungannya:

- 60,5kPa

$$Vout = Vs * (0{,}009 * P(kPa) - 0{,}095)$$
$$= 5 * ((0{,}009 * 60{,}5) - 0{,}095) = 2{,}25volt$$

- 101,3kPa

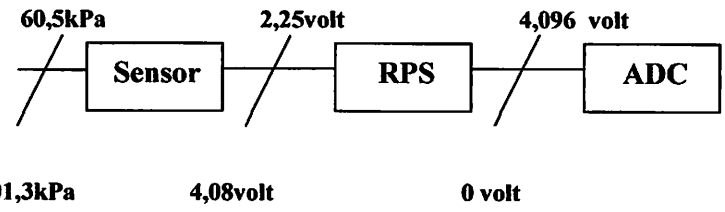
$$Vout = Vs * (0{,}009 * P(kPa) - 0{,}095)$$
$$= 5 * ((0{,}009 * 101{,}3) - 0{,}095) = 4{,}08volt$$

Jadi pada range tekanan sebesar 60,5kPa hingga 101,3kPa, sensor MPX4115AP akan menghasilkan jangkauan tegangan antara 2,25 volt hingga 4,08 volt. Range tegangan inilah yang akan menjadi tegangan masukan ke rangkaian pengkondisi sinyal.

3.3.2 Perencanaan Bagian Pengkondisi Sinyal

Pada bagian pengkondisi sinyal ini menggunakan rangkaian penguat selisih tegangan dengan penguatan dimana penguat ini digunakan sebagai penguat yang presisi untuk menguatkan sinyal-sinyal kecil. Rangkaian ini nantinya akan menjadi rangkaian penghubung dengan rangkaian ADC. Rangkaian pengkonsidi sinyal yang dirancang di sini merupakan gabungan dari rangkaian *voltage follower* (*buffer*) dan rangkaian penguat selisih tegangan. Yang mana keluaran dari masing-masing rangkaian *buffer* langsung diumpankan pada masing-masing masukan rangkaian penguat selisih tegangan.

Pada perencanaan bagian pengkondisi sinyal ini, direncanakan dengan range tegangan masukan 2,25 volt – 4,08 volt yang berasal dari rangkaian sensor MPX4115AP, rangkaian pengkondisi sinyal (RPS) akan menghasilkan tegangan keluaran sebesar 0 volt – 4,096 volt.



Dari ilustrasi di atas maka didapatkan persamaan sebagai berikut:

$$V_{OUT} = V_{IN} \cdot A + B \rightarrow 4{,}096 = 2{,}25 \cdot A + B \quad \text{.....a}$$

$$0 = 4{,}08 \cdot A + B \quad \text{.....b}$$

$$4{,}096 = -1{,}83A$$

$$A = -2{,}23 \ , \ B = 9{,}13$$

Dari hasil perhitungan di atas maka didapatkan persamaan baru sebagai berikut:

$$V_{OUT} = V_{IN} \cdot A + B \rightarrow V_{OUT} = 9{,}13 - 2{,}23 \cdot V_{IN}$$

$$V_{OUT} = 2{,}23 \times (4{,}09 - V_{IN}) \quad \text{.....(3.1)}$$

dimana Vout = Tegangan keluaran RPS (volt)

Vin = Tegangan masukan RPS = Tegangan keluaran sensor (volt)

$= V_1$

Hasil Persamaan 3.1 dijadikan acuan untuk merancang rangkaian pengkondisi sinyal yang akan menghasilkan tegangan keluaran 0 volt – 4,096 volt. Range tegangan keluaran dari rangkaian pengkondisi sinyal tersebut akan menjadi tegangan masukan ke rangkaian ADC.

Dari Persamaan 3.1 diketahui besarnya penguatan dari rangkaian pengkondisi sinyal sebesar 2,23 kali. Pada perencanaan ini digunakan rangkaian penguat selisih dengan penguatan, dimana rangkaian ini dapat membaca adanya tegangan differensial kecil. Karena penguatan yang dibutuhkan rangkaian penguat selisih dengan penguatan sebesar 2,23 kali, sedangkan harga Rf telah ditentukan sebesar 1 MΩ maka harga R1 dapat diperoleh yaitu:

$$Av = \frac{Rf}{R1} \rightarrow R1 = \frac{Rf}{Av}$$

$$R1 = \frac{1M\Omega}{2,23} = 448k\Omega$$

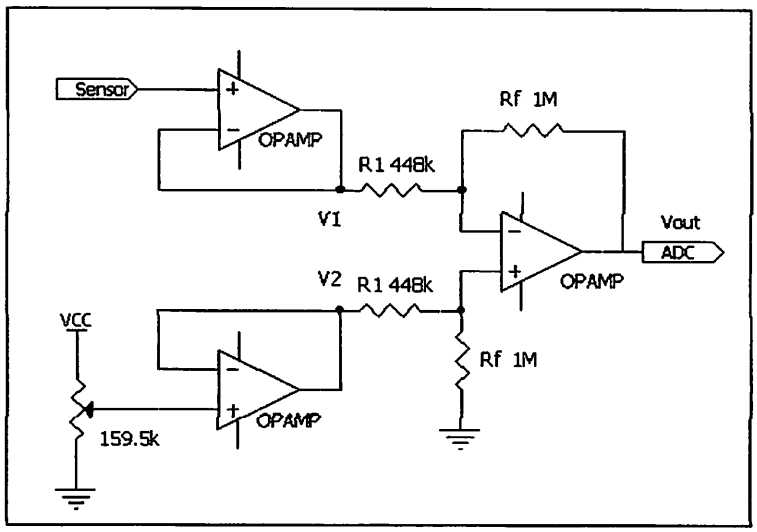
Dari perhitungan di atas digunakan nilai R1 sebesar 448k dengan menggunakan *multitune* sebesar 500k. Tegangan keluaran dari penguat ke dua akan menjadi tegangan masukan pada *Analog to Digital Converter* (ADC).

Tegangan referensi didapatkan dari tegangan keluaran sensor pada ketinggian nol meter dimana memiliki tekanan satu atm maka tekanan dalam kPa didapatkan sebesar 101,325 (diperoleh dari *Pressure Units Conversion Chart*), maka perhitungan tegangan referensi berdasarkan Persamaan 2.3 adalah:

$$Vref = V_2 = Vcc.(0,009.P - 0,095) \pm error \text{ (}data\ sheet\text{ sensor)}$$

$$= 5.(0,009 * 101,325 - 0,095) \pm 0,0675$$
$$= 4,08volt \pm 0,0675$$

maka didapatkan tegangan referensi (V_2) sebesar $4,08\ volt \pm 0,0675$. Untuk mengurangi impedansi masukan dari Vref maka digunakan rangkaian *voltage follower*. Gambar rangkaian pengkondisi sinyalnya ditunjukkan dalam Gambar 3.3.



Gambar 3.3 Rangkaian Pengkondisi Sinyal

Dari Gambar 3.3 diketahui bahwa penguat pertama berfungsi sebagai penyangga (*buffer*) sehingga tegangan keluaran yang dihasilkan sama besarnya dengan tegangan masukan. Tegangan masukan *buffer* ini berasal dari tegangan keluaran sensor dan tegangan referensi.. Kemudian tegangan keluaran dari *buffer* masuk ke penguat ke dua yaitu penguat selisih dengan penguatan (penguat differensial). Penguat ini yang akan menguatkan selisih tegangan antara tegangan keluaran dari sensor yang telah di*buffer* dengan tegangan referensi.

3.3.3. Perancangan Bagian *Analog to Digital Converter* (ADC)

Pada bagian ini digunakan ADC MAX187 yang diproduksi oleh MAXIM Semiconductor. ADC ini digunakan untuk mengubah tegangan analog menjadi data digital. ADC MAX187 merupakan ADC yang memiliki keluaran serial 12-bit

dengan konsumsi daya rendah dan dapat beroperasi dengan menggunakan catu daya 5 volt. Selain itu ADC ini memiliki dua mode tegangan referensi yaitu tegangan referensi internal (4,096 volt) dan tegangan referensi eksternal.

Karena keluaran dari rangkaian pengkondisi sinyal menghasilkan tegangan keluaran sebesar 0 volt – 4,096 volt, maka perencanaan rangkaian ADC MAX187 dipilih menggunakan tegangan referensi internal sebesar 4,096 volt. Adapun perhitungan resolusi dari ADC MAX 187 12-bit adalah sebagai berikut:

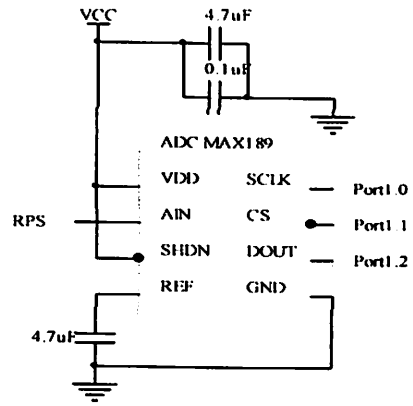
$$resolusi = \frac{Vref}{(2^n - 1)}$$

$$= \frac{4{,}096}{(2^{12} - 1)} = \frac{4{,}096}{4095}$$

$$= 1mV$$

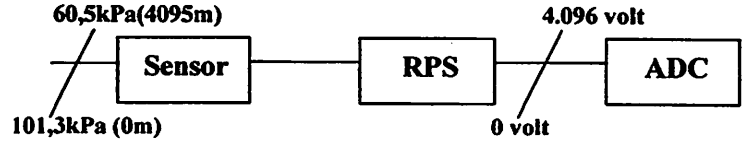
Jadi rangkaian ADC ini memiliki resolusi sebesar 1mV dengan tegangan referensi sebesar 4,096 volt. Untuk mengaktifkan tegangan referensi internal maka pin $\overline{SHDN}$ dihubungkan dengan Vcc (*high*) dan pada pin *REF* di*bypass* dengan kapasitor 4,7uF (Anonymous, 1993:7). Data-data analog yang dihasilkan rangkaian pengkondisi sinyal terhubung dengan pin AIN ADC.

ADC MAX187 ini menggunakan sumber clock eksternal sebesar 4Mhz, yang di*supply* oleh mikrokontroller melalui pin P1.0 yang terhubung dengan pin SCLK ADC. Sedangkan untuk mengaktifkan ADC MAX187 juga dikontrol melalui pin P1.1mikrokontroller yang terhubung dengan pin $\overline{CS}$ ADC. Sedangkan data serial ADC MAX187 dikeluarkan melalui pin DOUT yang terhubung dengan pin P1.2 mikrokontroller. Perencanaan rangkaian ADC ditunjukkan dalam Gambar 3.4.



Gambar 3.4 Rangkaian *Analog to Digital Converter* (ADC)

Berdasarkan spesifikasi alat yang dapat mengukur ketinggian 0 meter hingga 4095 meter dari permukaan laut, diharapkan dengan perubahan resolusi ADC 1mV alat ini mampu mendeteksi perubahan kenaikan ketinggian setinggi 1 meter. Perhitungan resolusi dari altimeter digital ini adalah sebagai berikut;



$$resolusi\_alat = \frac{\Delta Range\_ketinggian\_alat}{\Delta V_{IN}\ ADC}$$

$$= \frac{(4095-0)\,meter}{(4096-0)\,mV}$$

$$= 0,999 \approx 1\ meter/mV$$

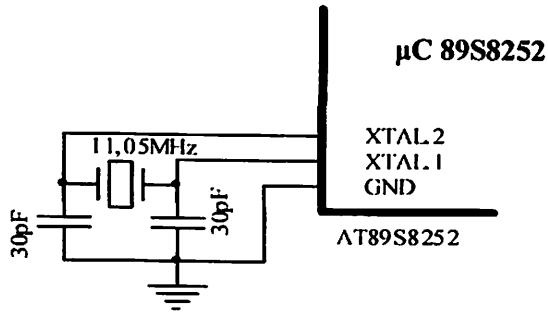
Jadi dengan resolusi 1mV dari ADC, alat ini mampu mendeteksi perubahan ketinggian setinggi 1 meter.

3.3.4 Perencanaan Bagian Kontrol dan Pengolah Data

Pada sistem ini komponen utamanya adalah mikrokontroller tipe AT89S8252 harus didukung oleh beberapa rangkaian lain agar dapat melakukan prosesnya, yaitu berupa rangkaian clock dan reset. Selain itu juga harus ditentukan penggunaan port-portnya dan sinyal-sinyal yang digunakan untuk mendukung proses yang akan dilakukan.

- ***Clock***

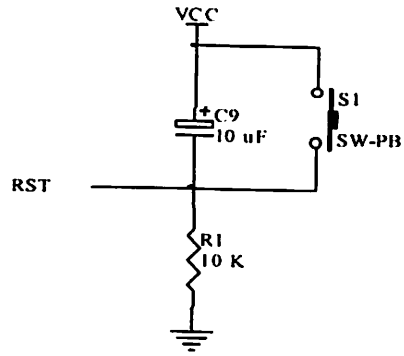
Kecepatan proses yang dilakukan oleh mikrokontroler ditentukan oleh sumber *clock* (pewaktuan) yang mengendalikan mikrokontroler tersebut. Sistem yang dirancang ini akan menggunakan osilator internal yang sudah tersedia di dalam chip AT89S8252. Untuk menentukan frekuensi osilatornya cukup dengan cara menghubungkan kristal pada pin XTAL1 dan XTAL2 serta dua buah kapasitor ke ground. Besar kapasitansinya disesuaikan dengan spesifikasi pada lembar data AT89S8252 yaitu 20 pF. Pemilihan besar frekuensi kristal disesuaikan dengan pemilihan kecepatan yang diharapkan untuk transfer data melalui pin *serial interface* AT89S8252 tersebut. Sistem ini dirancang untuk memiliki kemampuan *baud rate* sebesar 9600 bps, sehingga dipilih kristal dengan nilai 11,059 MHz sesuai dengan spesifikasi pada lembar data AT89S8252. Gambar 3.6. memperlihatkan rangkaian pewaktu yang digunakan.



Gambar 3.5. Rangkaian Pewaktuan

- ***Reset***

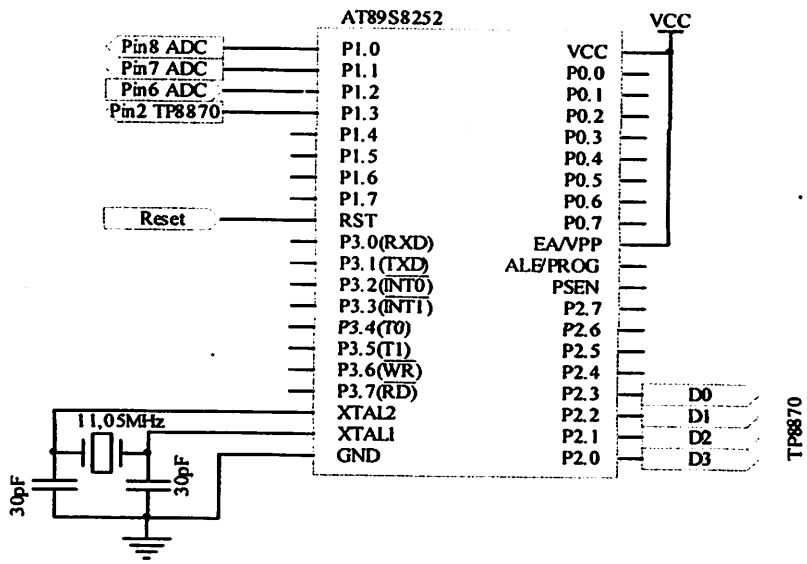
Untuk mereset mikrokontroler, pin RST harus diberi logika tinggi selama sekurangnya dua siklus mesin (24 periode osilator). Untuk membangkitkan sinyal reset pada saat awal catu daya dihidupkan, suatu reset otomatis dapat dilakukan dengan menghubungkan pin RST ke rangkaian *Power-On Reset*, seperti pada gambar 3.7. Ketika catu daya dinyalakan, rangkaian akan menahan pin RST dalam kondisi logika tinggi selama selang beberapa saat tergantung nilai kapasitor dan kecepatan pengisian muatannya. Pemberian catu daya pada mikrokontroler tanpa suatu sinyal reset dapat menyebabkan CPU memulai eksekusi instruksinya dari lokasi yang tak tertentu, ini disebabkan karena *Program Counter* tidak terinisialisasi.



Gambar 3.6. Rangkaian *Power-On Reset*

- **Pembagian Port**

Mikrokontroller AT89S8252 mempunyai 4 buah port yaitu port 0 (P0), port 1 (P1). port 2 (P2) dan port 3 (P3), maka port 0 digunakan untuk saluran data dan alamat bagian rendah yang dimultiplek (AD0-AD7) dan alamat bagian tinggi dikeluarkan pada port 2 (A8-A15). Port 3 digunakan sebagai pembangkit sinyal kontrol (Tx, Rx, RD dan WR).



Gambar 3.7. Rangkaian Mikrokontroler

Pin–pin yang digunakan pada IC AT89S8252 adalah sebagai berikut:

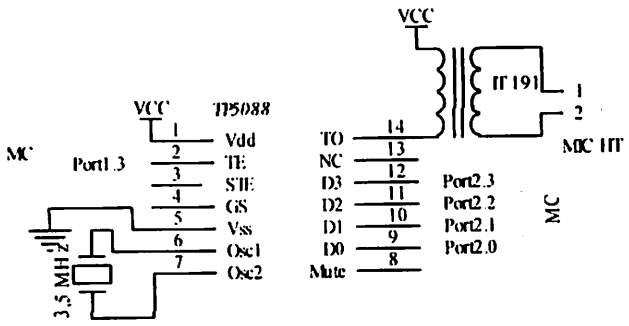
- P1.0 : digunakan untuk mengirimkan data *clock* ke *Serial Clock* (SCLK) ADC.
- P1.1 : digunakan untuk mengirim data kontrol ke *Chip Select* (CS) ADC.
- P1.2 : digunakan untuk menerima data dari ADC.
- P1.3 : untuk mengontrol *Tone Enable* pada *encoder* DTMF
- P 9 (reset) : reset aktif tinggi yang terhubung dengan rangkaian power on reset dan jika diaktifkan akan mereset mikrokontroler
- EA (*External Acces Enable*) : dihubungkan ke VCC karena program memori menggunakan memori program internal. X1 dan X2 digunakan sebagai input dari rangkaian osilator kristal. Rangkaian osilator kristal terdiri dari kristal osilator 11.0592 Mhz, kapasitor C1 dan C2 masing-masing 30 pF akan membangkitkan pulsa clock yang akan menjadi penggerak bagi sebuah operasi internal MCU. Jadi besarnya satu machine cycle dari rankaian ini dapat ditentukan dengan perhitungan sebagai berikut :

$$Tp = \frac{12}{fkristal} = \frac{12}{11.0592} \cong 1{,}0851\ \mu s$$

- P2.0 – P2.3 : merupakan input data untuk encoder DTMF (TP5088).

3.3.5 Perencanaan Bagian Pemancar (Encoder DTMF TP5088)

IC TP5088 ini menghasilkan tone dialing. Input dari TP5088 ini berupa 4 buah dari biner dan selanjutnya akan dikodekan menjadi sinyal DTMF tergantung kode yang dimasukkannya. IC ini akan bekerja apabila *Tone Enable* berlogika tinggi sehingga *clock* yang berasal dari *isolator Cristal 3.579545* Mhz akan aktif IC akan menghasilkan tone sampai *Tone Enable low* kembali. Jika pembacaan terhadap input akan dimulai pada saat transisi *Tone Enable* dari *Low* ke *High.*



Gambar 3.8 Rangkaian Encoder DTMF (TP5088)

Berikut konfigurasi pin-pinnya :

1. Pin 1 dihubungkan dengan Vcc
2. Pin 3 dihubungkan ke P.3 Mikrokontroller yang digunakan sebagai pengontrol pengiriman data.
3. Pin 5 dihubungkan dengan GND
4. Pin 6 dan Pin 7 dihubungkan dengan osilator yang digunakan sebagai input clock.
5. Pin 9 – Pin 12 merupakan input DTMF yang dihubungkan ke output Mikrokontroller pada P2.0 –P2.3 yang merupakan data biner yang akan dikonversi ke tone DTMF.

3.3.6 Perencanaan Bagian Penerima (Decoder DTMF MT8870)

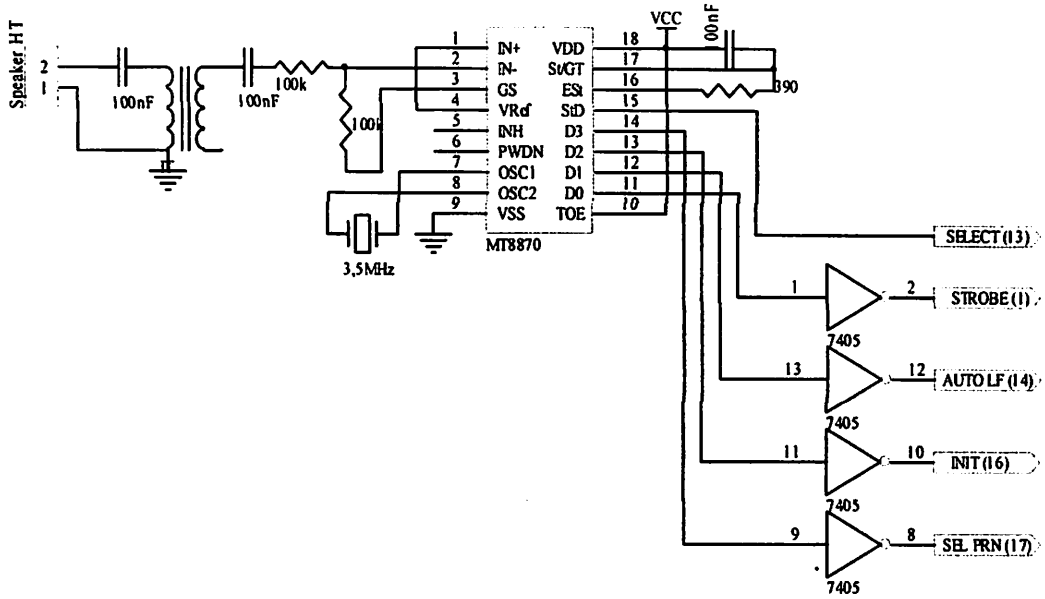
IC ini menghasilkan kode biner hasil tejemahan dari sinyal DTMF yang masuk. Rangkaian ini menggunakan *Osilator Crystal* 3,579545 Mhz sebagai *clocknya.* Sebagai sinyal pengaktif IC ini digunakan TOE, apabila dalam kondisi low maka IC akan mempunyai impedansi yang tinggi pada outputnya, sedanglan pada saat TOE dalam kondisi high maka IC akan aktif dan akan menterjemahkan sinyal DTMF yang masuk. Sedangkan input dimasukkan pada input inverting

4. Pin 10 dihubungkan dengan Vcc 5 volt.
5. Pin 11 – Pin 14 merupakan output decoder DTMF yang dihubungkan ke parallel port melalui inverter yang merupakan data konversi dari data ton DTMF yang diubah ke biner.
6. Pin 15 dihubungkan langsung dengan parallel port pin 13 tanpa melalui inverter yang digunakan sebagai indicator penerima data DTMF (STD).

3.4 Perencanaan Perangkat Lunak.

Perangkat lunak ini berdasarkan pengendali utama yaitu mikrokontroler AT 89S8252. Pembuatan perangkat lunak sistem aplikasi berdasarkan pada semua kejadian yang harus dikerjakan perangkat keras. Dalam system aplikasi ini menggunakan bahasa pemrograman *assembler* milik MCS-51.Secara garis besar, sistem kerja dari perangkat lunak dapat dilihat pada diagram alir seperti Gambar 3.11.

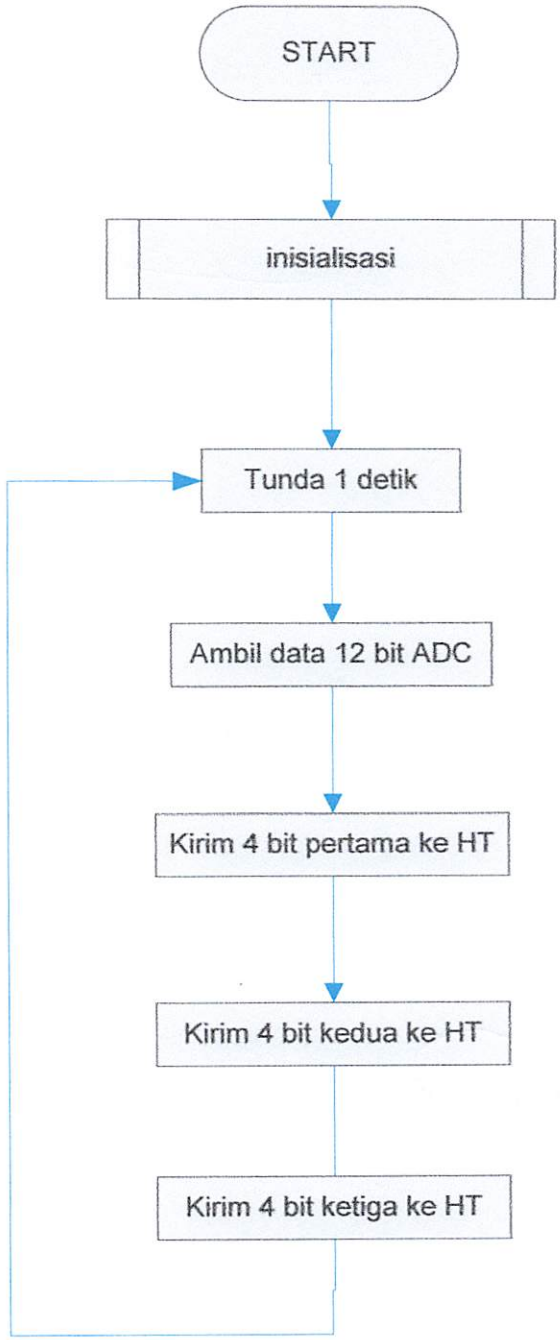
dengan penguatan satu kali, hal ini dapat diketahui dari nilai *Rin* an *Rf* yang dimasukkan ke pin GS sebagai *feedback*. Sebagai indicator adanya sinyal yang masuk maka Std akan berlogika tinggi dan akan low jika tidak ada sinyal yang masuk. Sebagai *interface* antara HT dengan rangkaian yang ada dalam system ini digunakan sebagai *transformator* (IT191) agar sinyal DC yang tidak diharapkan tidak ikut masuk dan juga sebagai penyesuai impedansi.



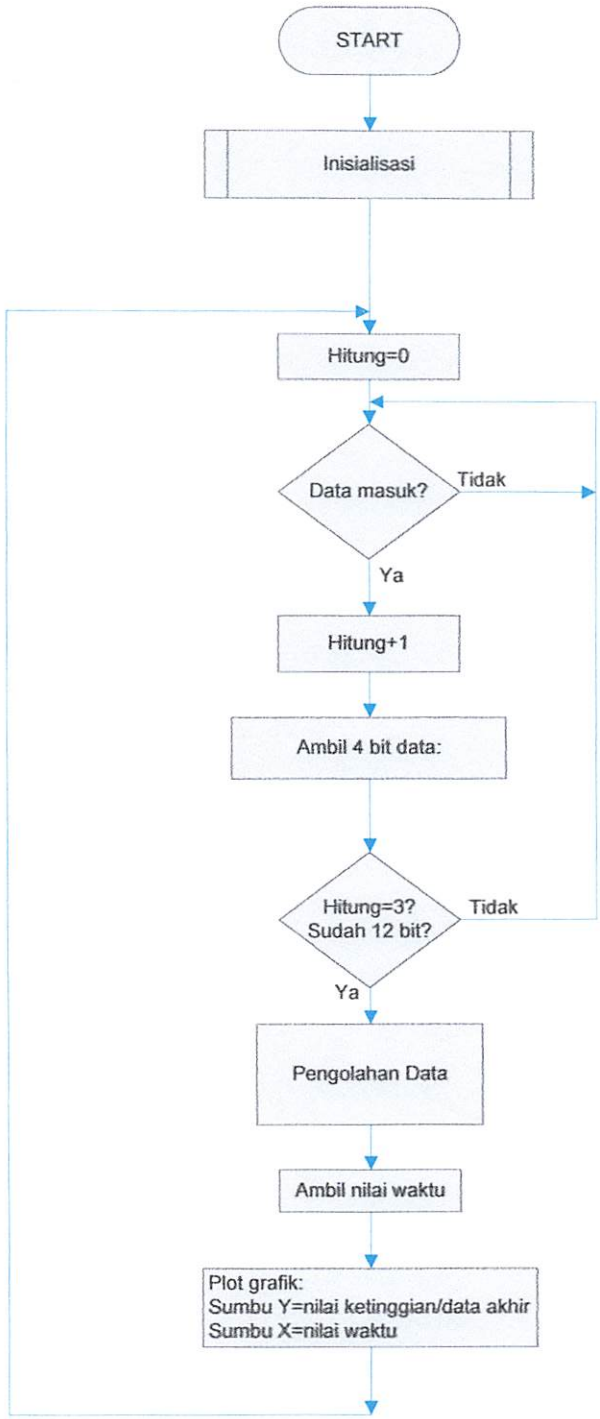
Gambar 3.9. Rangkaian *Decoder* DTMF (MT 8870)

Berikut konfigurasi pin-pinnya :

1. Pin 1 - P4 digunakan untuk menguatkan sinyal yang masuk yang dihubungkan dengan Travo.
2. Pin 7 dan Pin8 dihubungkan dengan osilator yang digunakan untuk input clock.
3. Pin 9 dihubungkan dengan GND.



Gambar 3.11 Diagram alir program utama pengirim



Gambar 3.12 Diagram Alir Program Penerima

BAB IV

PENGUJIAN ALAT

4.1 Umum

Tujuan pengujian alat ini adalah untuk menentukan apakah alat yang telah dibuat berfungsi dengan baik dan sesuai dengan perencanaan. Pengujian dilakukan dengan cara menguji rangkaian setiap blok secara terpisah. Pengujian setiap blok ini dilakukan untuk mempermudah analisis apabila alat ini tidak bekerja sesuai dengan perencanaan.

Dalam pelaksanaan pengujian dilakukan dengan dua cara yaitu secara perangkat keras dan perangkat lunak. Secara perangkat keras dilakukan melalui pemeriksaan sambungan pengawatan dan pengukuran dengan alat-alat ukur. Sedangkan pengujian perangkat lunak, pengujian dilakukan melalui pembuatan *software* dan hasilnya diamati dengan bantuan alat peraga atau melalui alat ukur.

4.2 Pengujian Sensor Tekanan

4.2.1 Tujuan

Untuk mengetahui hubungan antara ketinggian suatu tempat atau daerah dengan tegangan keluaran yang dihasilkan sensor tekanan dan mengetahui *noise* yang dihasilkan dari sensor tekanan tersebut..

4.2.2 Peralatan yang Digunakan

1) Rangkaian sensor tekanan MPX4115AP
2) Osiloskop.

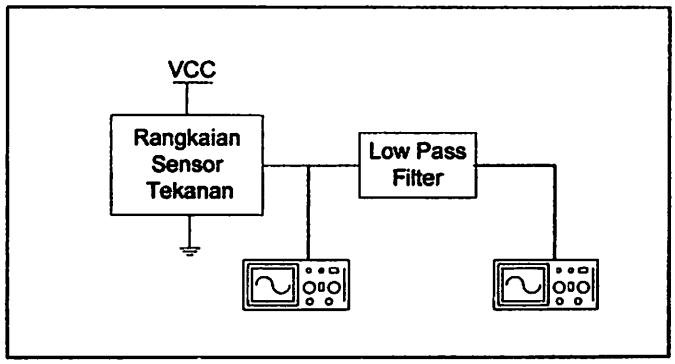
4) *Projectboard.*

5) Catu daya +5 volt.

4.2.3 Langkah Pengujian

Langkah-langkah pengujian adalah sebagai berikut:

Merangkai blok rangkaian pengujian sensor tekanan seperti dalam

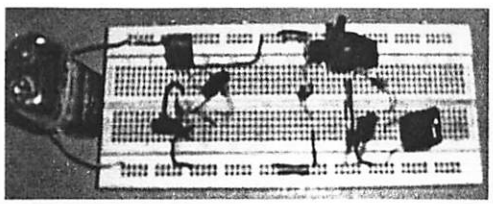


Gambar 4.1 Blok Pengujian Sensor Tekanan dengan Osiloskop

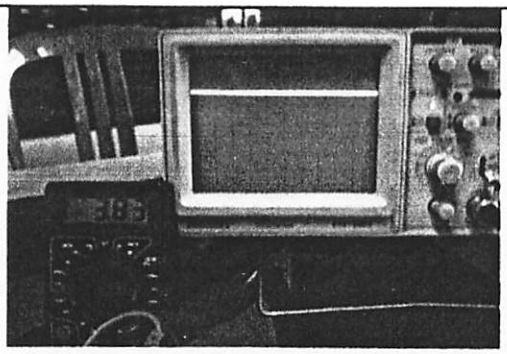
1) Memberikan catu daya +5 volt pada rangkaian sensor tekanan.
2) Menghubungkan osiloskop pada bagian keluaran dari rangkaian sensor sebelum dan sesudah melalui filter (Gambar 4.1), guna mengetahui *noise* yang dihasilkan dari sensor tekanan.
3) Hasil pengujian terdapat pada osiloskop.

4.2.4 Hasil Pengujian

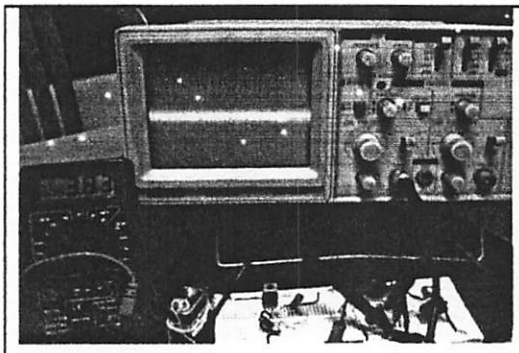
Gambar 4.2 menunjukkan hasil pengujian rangkaian sensor tekanan pada osiloskop



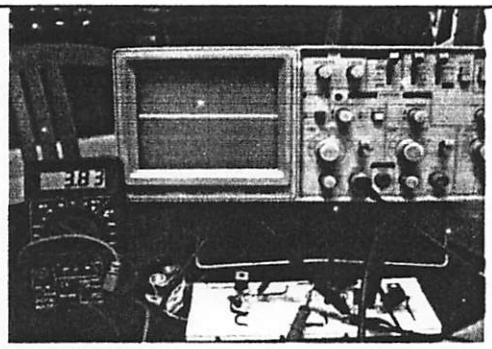
Gambar 4.2a Rangkaian Sensor Tekanan



Gambar 4.2b Tegangan Keluaran Sensor Tekanan (V_{DC})



Gambar 4.2c *Noise* yang dihasilkan Sensor Tekanan sebelum difilter



Gambar 4.2d *Noise* yang dihasilkan Sensor Tekanan setelah difilter

Tabel 4.1 Hasil Pengujian Sensor Tekanan dengan Multimeter Digital

No.	Tempat (stasiun) yang diukur	Ketinggian (m)	Vout Sensor (volt)
1	Malang Kota Baru	444	3,85
2	Malang Kota Lama	429	3,86
3	Pakisaji	386	3,87
4	Pantai Sendangbiru	0	4,08

4.3 Pengujian Rangkaian Pengkondisi Sinyal

4.3.1 Tujuan

Untuk mengetahui persentase rata-rata kesalahan tegangan keluaran pada rangkaian pengkondisi sinyal dalam melakukan pembacaan dari rangkaian sensor tekanan.

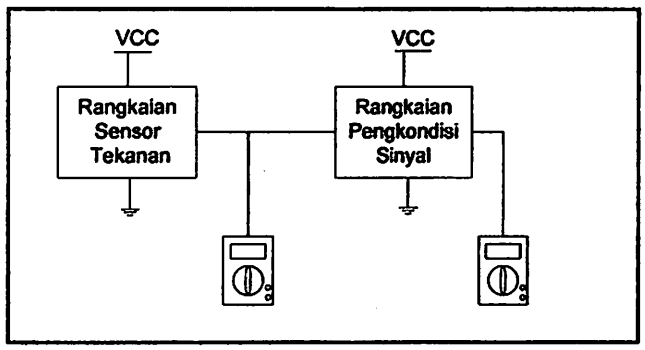
4.3.2 Peralatan yang Digunakan

1) Rangkaian pengkondisi sinyal.
2) Rangkaian sensor tekanan MPX4115AP.
3) Multimeter digital DT-830B No.11270.
4) *Projectboard.*
5) Catu daya +5 volt.

4.3.3 Langkah Pengujian

Langkah-langkah pengujian adalah sebagai berikut:

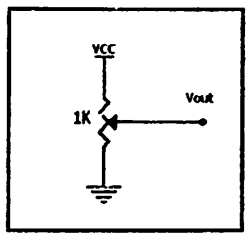
1) Merangkai blok rangkaian pengujian pengkondisi sinyal seperti dalam Gambar 4.3.



Gambar 4.3 Blok Pengujian Pengkondisi Sinyal

2) Menghubungkan blok rangkaian sensor tekanan sebagai masukan pada rangkaian pengkondisi sinyal.
3) Memberikan catu daya +5 volt pada rangkaian pengkondisi sinyal dan rangkaian sensor tekanan.
4) Menghubungkan multimeter digital pada bagian keluaran rangkaian sensor tekanan dan keluaran rangkaian pengkondisi sinyal.
5) Hasil pengujian terdapat pada multimeter digital.

Karena bekerjanya rangkaian sensor tekanan tergantung dari ketinggian suatu tempat, maka rangkaian sensor tersebut digantikan dengan rangkaian pembagi tegangan yang bekerjanya identik dengan rangkaian sensor tersebut, yaitu menghasilkan tegangan keluaran sesuai dengan tekanan udara yang dideteksinya. Dalam pengujian ini rangkaian pembagi tegangan tersebut menggunakan *multitune* sebesar 1k, yang menghasilkan range tegangan keluaran 2,25 volt – 4,08 volt. Adapun rangkaian pembagi tegangan ditunjukkan dalam Gambar 4.4.



Gambar 4.4 Rangkaian Pembagi Tegangan

4.3.4 Hasil Pengujian

Tabel 4.2 menunjukkan hasil pengujian Rangkaian Pengkondisi Sinyal (RPS).

Tabel 4.2 Hasil Pengujian Rangkaian Pengkondisi Sinyal

No.	Vout Sensor (*volt*)	Vout RPS(volt)	
		Pengujian	Perhitungan
1	4,00	0,20	0,2
2	3,82	0,61	0,6
3	3,58	1,14	1,13
4	3,35	1,67	1,65
5	3,13	2,15	2,14
6	2,90	2,68	2,65
7	2,68	3,14	3,14
8	2,45	3,70	3.66

4.4 Pengujian Rangkaian ADC

4.4.1 Tujuan

Untuk mengetahui presentase rata-rata kesalahan rangkaian ADC dalam melakukan pengkonversian tegangan analog yang berasal dari rangkaian pengkondisi sinyal menjadi data-data digital.

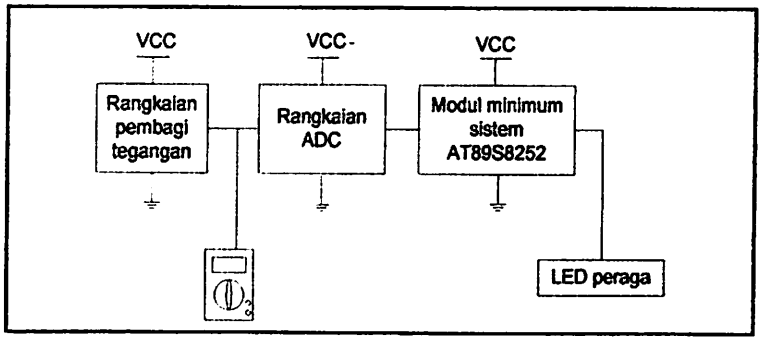
4.4.2 Peralatan yang Digunakan

1) Rangkaian ADC.
2) Modul minimum sistem mikrokontroller AT89S8252
3) Multimeter digital DT-830B No.11270.
4) *Light Emitting Dioda* (LED) peraga.
5) *Projectboard.*
6) Catu daya +5 volt.

4.4.3 Langkah Pengujian

Langkah-langkah pengujian adalah sebagai berikut:

1) Merangkai blok rangkaian pengujian ADC seperti dalam Gambar 4.5.



Gambar 4.5 Blok Pengujian ADC

2) Menghubungkan modul minimum sistem mikrokontroller AT89S8252 dengan blok rangkaian pengujian ADC.

3) Membuat program untuk membaca data dari blok ADC pada modul minimum sistem mikrokontroller AT89S8252, kemudian data yang dibaca oleh mikrokontroller dari blok ADC tersebut dikonversikan menjadi kode biner dan dikirimkan melalui port 0, port 3 menuju modul LED peraga.
4) Memberikan catu daya +5 volt pada rangkaian ADC dan modul minimum sistem mikrokontroller AT89S8252.
5) Memberikan masukan pada blok rangkaian pengujian ADC melalui pin 2 (AIN) berupa tegangan analog dari rangkaian pembagi tegangan.
6) Menghubungkan multimeter digital pada bagian keluaran rangkaian pembagi tegangan dan hasil pengujian terdapat pada LED peraga.

4.4.4 Hasil Pengujian

Tabel 4.3 menunjukkan hasil pengujian ADC.

Tabel 4.3 Hasil Pengujian ADC

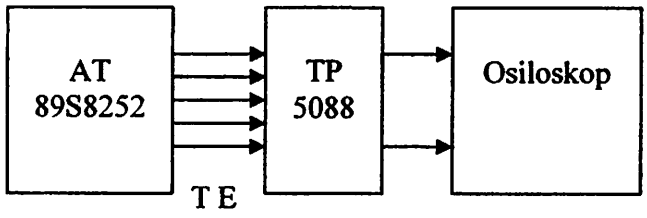
No.	Vin ADC (volt)	Data Keluaran Digital	
		Perhitungan (heksadesimal)	Pengujian ADC (heksadesimal)
1	0,5	1F3	1F5
2	1	3E7	3E8
3	1,5	5DB	5DD
4	2	7CF	7CD
5	2,5	9C3	9C1
6	3	BB7	BB6
7	3,5	DAB	DAC
8	4	F94	F96

4.5 Pengujian (encoder) DTMF

4.5.1 Tujuan

Tujuan dari pengujian ini adalah untuk mengetahui apakah (*encoder*) DTMF tersebut bekerja dengan apa yang diharapkan.

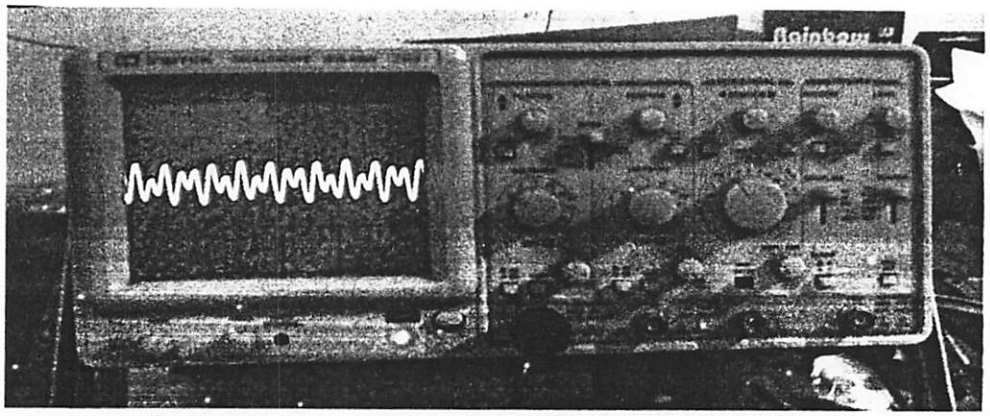
Rangkaian pemancar (encoder) DTMF dalam piranti ini menggunakan IC TP5088. IC ini dirancang untuk membangkitkan nada pilih yang digunakan telepon DTMF. Input dari IC ini berupa 5 bit, 4 bit data yang akan ditranmsika dan 1 bit sebagai control untuk pentranmisian (tone enable). Rangkaian pengujian ditunjukkan pada gambar 4.6 sebagai berikut :



Gambar. 4.6 Rangkaian pengujian pemancar DTMF

4.5.2 Hasil Pengujian

Hasil keluaran dari pemancarr DTMF berupa gambar sinyal pemancar seperti gambar dibawah ini.



Gambar 4.7 Gambar Keluaran pemancarr DTMF pada osiloskop.

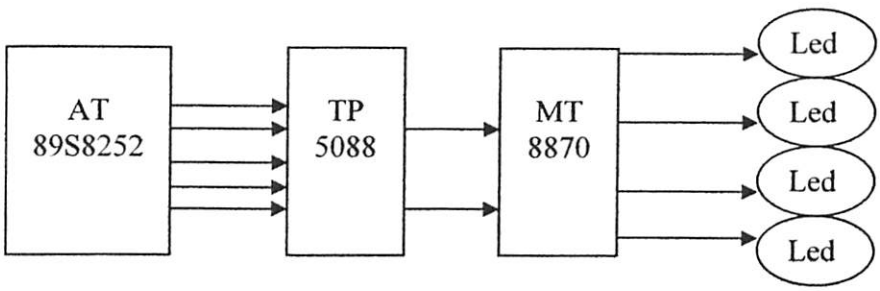
Hasil dari gambar diatas T/Div =10 ms dan V/Div = 5 Volt AC.

4.6 Pengujian penerima (decoder) DTMF

4.6.1 Tujuan

Tujuan dari pengujian ini adalah untuk mengetahui apakah (*encoder*) DTMF tersebut bekerja dengan apa yang diharapkan

Dalam piranti ini penerima (decoder) DTMF menggunakan IC MT 8870. untuk memudahkan pengujian rangkaian ini, maka digunakanpula rangkaian pengujian pemancar DTMF (pada Gambar 4.6). Ontput dari TP 5088 dihubungkan pada input MT 8870, seperti gambar 4.8 dibawah ini :



Gambar 4.8 Pengujian penerima (decoder) DTMF.

4.6.2 Hasil Pengujian

Keluaran MT8870 adalah sesuai degan table 4.4

Tabel 4.4 hasil keluaran penerima (decoder) DTMF MT8870

Pin		Q1	Q2	Q3	Q4
In TP 5088	TE = 1	1	0	0	0
Out MT8870	STD = 1	1	0	0	0

Dari hasil tabel diatas dapat dianalisa sebagai berikut data dari MCU AT89S8252.berupa bilangan biner kemudian masuk ke TP 5088 diubah menjadi tone DTMF kemudian masuk ke MT 8870 diubah lagi menjadi bilangan biner. Dan hasilnya tetap yaitu 1000 H.

Pada rangkaian ini pengkodean kembali terhadap sinyal DTMF akan dideteksi dengan pin STD inilah yang akan dikirimkan ke MCU. Port 1.5 sebagai tanda bahwa sinyal masuk. Bil pin STD berlogika Low maka MCU tidak akan menerima data dari penerima (decoder) DTMF.

4.5 Pengujian Alat

4.5.1 Tujuan

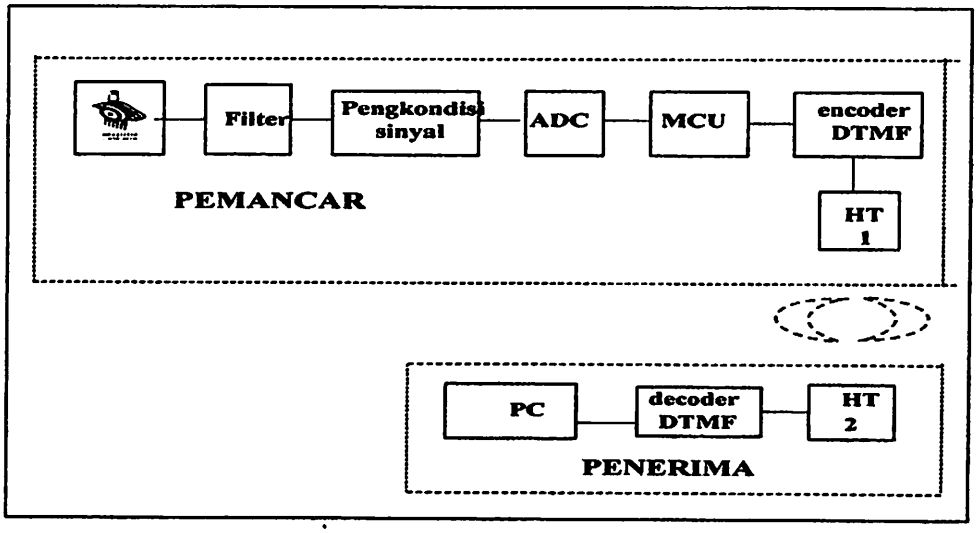
Pengujian alat bertujuan untuk mengetahui kinerja sistem secara keseluruhan, apakah sesuai dengan spesifikasi yang direncanakan di awal dan mengetahui persentasi rata-rata kesalahan pengukuran dari alat tesebut.

4.5.2 Peralatan yang Digunakan

1) Rangkaian sensor tekanan MPX4115AP.
2) Rangkaian pengkondisi sinyal.
3) Rangkaian ADC.
4) Modul mikrokontroller AT89S8252.
5) Rangkaian (Encoder) DTMF
6) Rangkaian DTMF (Decoder).

7) 1 Pasang HT
8) Perangkat Komputer
9) Catu daya +5 volt.

Pengujian keseluruhan rangkaian ini meliputi program dan alat yang telah direncanakan, bertujuan untuk mengetahui apakah sesuai dengan yang direncanakan pengujian ini bertujuan untuk mengetahui persentase *error* dari setiap pengukuran ketinggian.



Gambar 4.9 Rangkaian Blok keseluruhan

4.5.3 Hasil Pengujian

Pengujian I :

Tabel 4.5 Hasil Pengujian I
(lokasi : Sumber Sari Malang)

No.	Pengambilan sample ketinggian tempat		*Error*
	Pengukuran GPS (m)	Pengukuran alat (m)	
1.	502	503	1
2.	503	505	2
3.	504	507	2

❖ **Analisa Data**

$$\%Error = \frac{502-503}{502} x100\%$$

$$= \frac{1}{502} x100\%$$

$$= 0{,}19\%$$

$$\%ketelitian = 100\% - \%Error$$

$$= 100\% - 0{,}19\%$$

$$= 99{,}81\%$$

$$\%Error = \frac{503-505}{503} x100\%$$

$$= \frac{2}{503} x100\%$$

$$= 0{,}4\%$$

$$\%ketelitian = 100\% - \%Error$$

$$= 100\% - 0{,}4\%$$

$$= 99{,}6\%$$

$$\%Error = \frac{503-505}{503} x100\%$$

$$= \frac{2}{503} x100\%$$

$$= 0{,}4\%$$

$$\%ketelitian = 100\% - \%Error$$

$$= 100\% - 0{,}4\%$$

$$= 99{,}6\%$$

Tabel 4.6 Persentase *Error* Pengujian I

No.	Pengambilan sample ketinggian tempat		*Error* (%)	Ketelitian (%)
	Perencanaan	Pengukuran		
1.	502	503	0,19	99,81
2.	503	505	0,4	99,6
3.	504	507	0,4	99,6

$$\%Error rata-rata = \frac{\sum \%(Error)}{\sum Data}$$

$$= \frac{0,99\%}{3}$$

$$= 0.33\%$$

Pengujian II :

Tabel 4.7 Hasil Pengujian II
(lokasi : Sengkaling – Malang)

No.	Jumlah Pengambilan sample ketinggian tempat		*Error*
	Pengukuran GPS (m)	Pengukuran alat (m)	
1.	565	567	2
2.	566	569	3
3.	567	601	4

❖ **Analisa Data**

$$\%Error = \frac{565-567}{565} x100\%$$

$$= \frac{2}{565} x100\%$$

$$= 0{,}35\%$$

$$\%ketelitian = 100\% - \%Error$$

$$= 100\% - 0{,}35\%$$

$$= 99{,}65\%$$

$$\%Error = \frac{566-569}{566} x100\%$$

$$= \frac{3}{566} x100\%$$

$$= 0{,}53\%$$

$$\%ketelitian = 100\% - \%Error$$

$$= 100\% - 0{,}53\%$$

$$= 99{,}47\%$$

$$\%Error = \frac{567-601}{567} x100\%$$

$$= \frac{4}{567} x100\%$$

$$= 0{,}71\%$$

$$\%ketelitian = 100\% - \%Error$$

$$= 100\% - 0{,}71\%$$

$$= 99{,}29\%$$

Tabel 4.8 Persentase *Error* Pengujian II

No.	Pengambilan sample ketinggian tempat		*Error* (%)	Ketelitian (%)
	Perencanaan	Pengukuran		
1.	565	567	0,35	99,65
2.	566	569	0,53	99,47
3.	567	601	0,71	99,29

$$\%Errorrata-rata=\frac{\sum\%(Error)}{\sum Data}$$

$$=\frac{1{,}59\%}{3}$$

$$=0.53\%$$

BAB V

PENUTUP

5.1 Kesimpulan

Setelah mengkaji isi dari bab-bab sebelumnya mulai dari perencanaan, pembuatan hingga pengujian dari tugas akhir yang berjudul *"Perencanaan dan Pembuatan Alat Pengukur Ketinggian Gelombang Air Laut Untuk Informasi Pelayaran Berbasis Mikrokontroller AT89S8252"*, maka bisa diambil beberapa kesimpulan sebagai berikut :

1. *Error* yang diperoleh dari hasil pengukuran dengan pengujian pada pengambilan sampel ketinggian tempat menunjukkan bahwa semakin tinggi lokasi yang kita uji maka *error* semakin tinggi ini dikarenakan faktor suhu yang berlainan ini bisa dilihat pada tabel 4.5 sampai dengan Tabel 4.8.
2. Perubahan resolusi ADC 1mV alat ini mampu mendeteksi perubahan kenaikan ketinggian setinggi 1 meter

5.2 Saran

Dalam pembuatan skripsi ini masih ada kekurangannya, sehingga untuk mencapai hasil yang lebih sempurna maka dapat diberikan saran-saran sebagai berikut :

1. Tampilan dari alat ini bisa dikembangkan yaitu dengan menambah sensor-sensor lain sehingga tidak hanya menampilkan grafik ketinggian terhadap

waktu saja tetapi juga dapat mendeteksi keadaan cuaca , kecepatan angin,arah angin dan sebagainya.

2. Sebulum melakukan pengujian sebaiknya alat ini diset dengan ketinggian permukaan air laut sebenarnya, sehingga persentase rata-rata kesalahan pembacaan pada alat dapat dikurangi.

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Panduan' *praktikum Dasar elektronika* 'ITN malang

LAMPIRAN

A

INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGURA-GURA 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Erwin Nurpatria Sakti
Nim : 0017179
Masa Bimbingan : 17 Jun 2006 s/d 17 Dec 2006
Judul Skripsi : Perencanaan dan Pembuatan Alat Pengukur Ketinggian Gelombang Air Laut Untuk Informasi Pelayaran Berbasis Mikrokontroller AT89S8252

NO	Tanggal	Uraian	Paraf Pembimbing
1.	11-8-2006	Acc BAB I & II	
2.	24-8-2006	Revisi BAB III ADC.	
3.	26-8-2006	ACC BAB III.	
4.	4-9-2006	Revisi Hasil pengujian.	
5.	12-9-2006	ACC BAB IV & V	
6.	18-9-2006	Acc lompre	
7.			
8.			
9.			
10.			

Malang, 2006

Dosen Pembimbing

Joseph Dedy Irawan ST,MT
NIP. 132315178

Form S-4a

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KOSENTRASI T.ELEKTRONIKA

LEMBAR BIMBINGAN SKRIPSI

Nama Mahasiswa	: Erwin Nur Patria Sakti
Nim	: 0017179
Jurusan	: T.Elektro S-1
Kosentrasi	: T.Elektronika
Judul	: Perencanaan Dan Pembuatan Alat Pengukur Ketinggin Gelombang Air Laut Untuk Informasi Pelayaran Berbasis Mikrokontroler AT89S8252
Tanggal Pengajuan Skripsi	: 5 Juni 2006
Selesai Penulisan Skripsi	: September 2006
Dosen pembimbing	: Joshep Dedy Irawan ST,MT
Telah dievaluasi Dengan Nilai	: 87 (A)

Mengetahui
Ketua Jurusan Teknik Elektro S-1

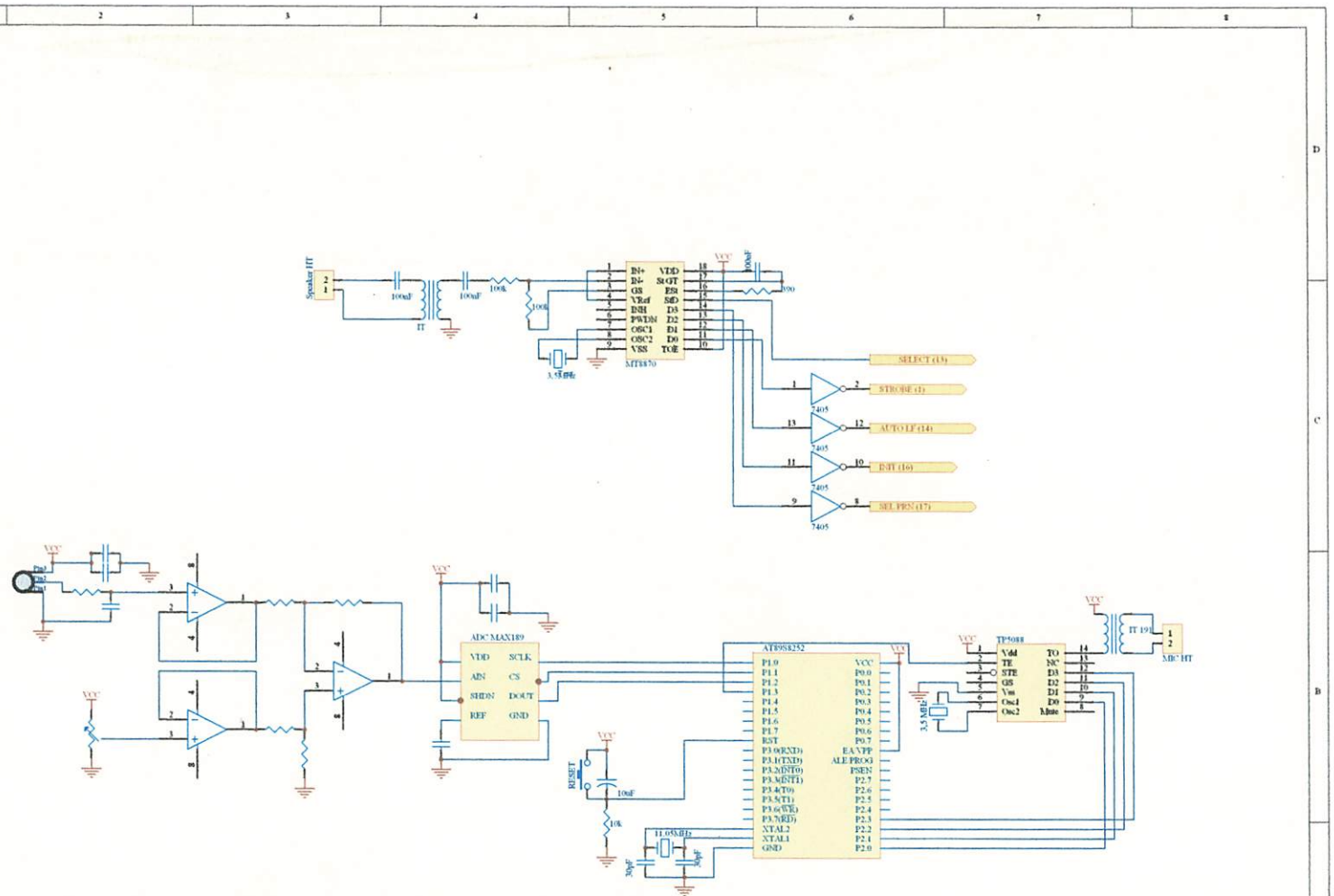
Ir.F.Yudi Limpraptono.MT
NIP.Y.1039500274

Diperiksa dan Disetujui
Dosen Pembimbing

Joshep Dedy Irawan.ST,MT
NIP.132315178

LAMPIRAN

B



Title			
Size: A3	Number		Revision
Date:	23-Sep-2006	Sheet of	
File:	H:\TA_KU\LENGKAP.SCH	Drawn By:	

```
MCS-51 Family Macro Assembler   A S E M - 5 1   V 1.3
=====================================================


 Source File:    H:\altimeter.a51
 Object File:    H:\altimeter.hex
 List File:      H:\altimeter.lst


 Line  I  Addr  Code            Source

    1:                         $TITLE          (Altimeter)
    2:                         $nosymbols
    3:          N      0000                    org     00h
    4:    0000  02 00 50                       ljmp    start
    5:
    6:          N      0050                    org     50h
    7:                         ;init hard ---------------------------------;
    8:                         ;kontrol TP5088
    9:          B        93    te              bit     p1.3    ;tone enable
   10:          D      00A0    tone            equ     P2      ;data out
   11:          B        94    lamp            bit     p1.4
   12:
   13:                         ;kontrol ADC serial
   14:          B        90    sclk            bit     p1.0
   15:          B        91    cs              bit     p1.1
   16:          B        92    dout            bit     p1.2
   17:
   18:                         ;ram data adc 12 bit
   19:          N      0030    temp_h          equ     30h     ;8 bit high order
   20:          N      0031    temp_l          equ     31h     ;4 bit low order
   21:
   22:                         ;program start
   23:    0050                 start:
   24:    0050  75 89 01               mov     tmod,#1
   25:    0053  C2 93                  clr     te
   26:    0055  D2 94                  setb    lamp
   27:    0057                 ss:
   28:    0057  C2 90                  clr     sclk
   29:    0059  D2 91                  setb    cs
   30:    005B  12 00 CB               call    timer1s
   31:    005E  12 00 66               call    ambil_data
   32:    0061  12 00 90               call    kirim
   33:    0064  80 F1                  sjmp    ss
   34:                         ;subzero
==========================================
   35:                         ;pengambilan data adc 12 bit
   36:    0066                 ambil_data:
   37:    0066  C2 30                  clr     temp_h
   38:    0068  C2 31                  clr     temp_l
   39:    006A  C2 91                  clr     cs
   40:    006C  78 14                  mov     r0,#20
   41:    006E  D8 FE                  djnz    r0,$
   42:    0070  D2 90                  setb    sclk
   43:    0072  00                     nop
```

```
 Line  I  Addr  Code            Source

   44:     0073  C2 90                 clr     sclk
   45:     0075  78 08                 mov     r0,#8           ;pengambilan 8
bit
   46:     0077                  pulse:
   47:     0077  D2 90                 setb    sclk
   48:     0079  A2 92                 mov     c,dout
   49:     007B  C2 90                 clr     sclk
   50:     007D  33                    rlc     a
   51:     007E  D8 F7                 djnz    r0,pulse
   52:     0080  F5 30                 mov     temp_h,a
   53:
   54:     0082  78 04                 mov     r0,#4           ;pengambilan 4
bit
   55:     0084                  pulse2:
   56:     0084  D2 90                 setb    sclk
   57:     0086  A2 92                 mov     c,dout
   58:     0088  C2 90                 clr     sclk
   59:     008A  33                    rlc     a
   60:     008B  D8 F7                 djnz    r0,pulse2
   61:     008D  F5 31                 mov     temp_l,a        ;xxxxdddd
   62:     008F  22                    ret
   63:
   64:                           ;pengiriman data 3 nibble ke tp5088
   65:                           ;method - (2nd) low order -> (1st) high order
   66:     0090                  kirim:
   67:                           ;       mov     a,temp_h
   68:                           ;       swap    a               ;high nibble from
high order send out first
   69:     0090  74 01                 mov     a,#1
   70:     0092  F5 A0                 mov     tone,a
   71:     0094  D2 93                 setb    te
   72:     0096  12 00 DF              call    t_50ms
   73:     0099  C2 93                 clr     te
   74:     009B  12 00 F3              call    t_25ms
   75:                           ;       swap    a               ;then low nibble
from high order send out
   76:     009E  74 08                 mov     a,#8
   77:     00A0  F5 A0                 mov     tone,a
   78:     00A2  D2 93                 setb    te
   79:     00A4  12 00 DF              call    t_50ms
   80:     00A7  C2 93                 clr     te
   81:     00A9  12 00 F3              call    t_25ms
   82:                           ;       mov     a,temp_l        ;last low nibble
from low order send out
   83:     00AC  74 0C                 mov     a,#0ch
   84:     00AE  F5 A0                 mov     tone,a
   85:     00B0  D2 93                 setb    te
   86:     00B2  12 00 DF              call    t_50ms
   87:     00B5  C2 93                 clr     te
   88:     00B7  12 00 F3              call    t_25ms
   89:     00BA  22                    ret
   90:
   91:     00BB                  timer1ms:
   92:                                                         ;timer 1 ms,xtal
11.05
   93:     00BB  75 8C FC              mov     th0,#0fch
   94:     00BE  75 8A 66              mov     tl0,#066h
   95:     00C1  D2 8C                 setb    tr0
   96:     00C3  30 8D FD              jnb     tf0,$
   97:     00C6  C2 8C                 clr     tr0
   98:     00C8  C2 8D                 clr     tf0
   99:     00CA  22                    ret
```

```
Line  I  Addr  Code            Source

 100:
 101:     00CB                 timer1s:
 102:     00CB  7C 14                  mov     r4,#20          ;timer 1s
 103:     00CD  75 8C 3A       ob1:    mov     th0,#03ah
 104:     00D0  75 8A EB               mov     tl0,#0ebh
 105:     00D3  D2 8C                  setb    tr0
 106:     00D5  30 8D FD               jnb     tf0,$
 107:     00D8  C2 8C                  clr     tr0
 108:     00DA  C2 8D                  clr     tf0
 109:     00DC  DC EF                  djnz    r4,ob1
 110:     00DE  22                     ret
 111:
 112:     00DF                 t_50ms:
 113:     00DF  7C 0A                  mov     r4,#10          ;timer 1/2 s
 114:     00E1  75 8C 3A       ob2:    mov     th0,#03ah
 115:     00E4  75 8A EB               mov     tl0,#0ebh
 116:     00E7  D2 8C                  setb    tr0
 117:     00E9  30 8D FD               jnb     tf0,$
 118:     00EC  C2 8C                  clr     tr0
 119:     00EE  C2 8D                  clr     tf0
 120:     00F0  DC EF                  djnz    r4,ob2
 121:     00F2  22                     ret
 122:
 123:     00F3                 t_25ms:
 124:     00F3  7C 05                  mov     r4,#5           ;timer 1/4 s
 125:     00F5  75 8C 3A       ob3:    mov     th0,#03ah
 126:     00F8  75 8A EB               mov     tl0,#0ebh
 127:     00FB  D2 8C                  setb    tr0
 128:     00FD  30 8D FD               jnb     tf0,$
 129:     0100  C2 8C                  clr     tr0
 130:     0102  C2 8D                  clr     tf0
 131:     0104  DC EF                  djnz    r4,ob3
 132:     0106  22                     ret
 133:                                 end
```

register banks used: ---

no errors

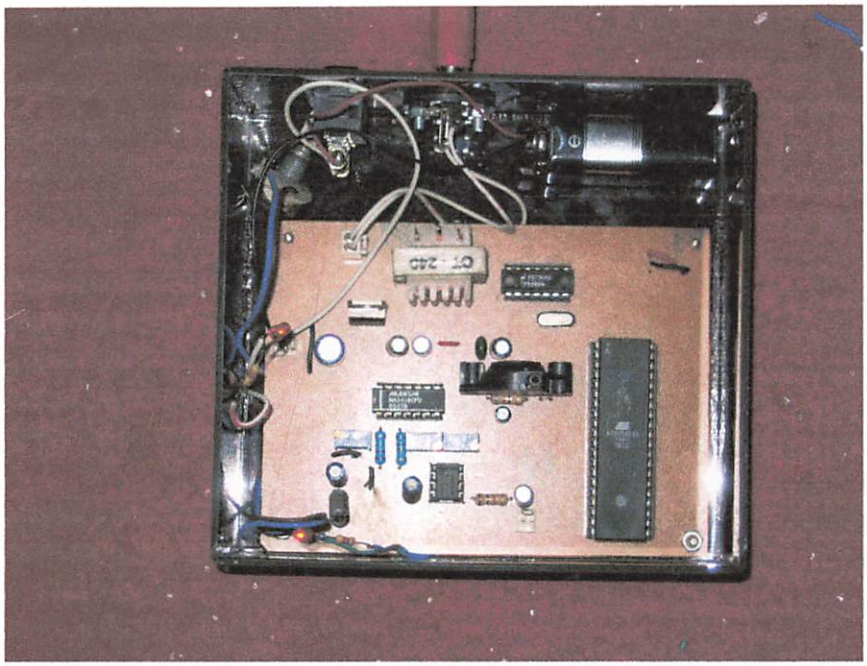
```
unit Umain;

interface

uses
  Windows, Messages, SysUtils, Variants, Classes, Graphics, Controls, Forms,
  Dialogs, SkinData, DynamicSkinForm, TeEngine, Series, ExtCtrls, TeeProcs,
  Chart, PortIO, TextFade, SkinCtrls, StdCtrls;

type
  TForm1 = class(TForm)
    spDynamicSkinForm1: TspDynamicSkinForm;
    spSkinData1: TspSkinData;
    spCompressedStoredSkin1: TspCompressedStoredSkin;
    Chart1: TChart;
    Series1: TFastLineSeries;
    p1: TDLPrinterPortIO;
    TextFader1: TTextFader;
    Timer1: TTimer;
    btstart: TspSkinButton;
    btstop: TspSkinButton;
    l1: TspSkinStdLabel;
    Timer2: TTimer;
    Label1: TLabel;
    procedure FormCreate(Sender: TObject);
    procedure Timer1Timer(Sender: TObject);
    procedure btstartClick(Sender: TObject);
    procedure btstopClick(Sender: TObject);
    procedure FormClose(Sender: TObject; var Action: TCloseAction);
    procedure Timer2Timer(Sender: TObject);
  private
    { Private declarations }
  public
    { Public declarations }
  end;

var
  Form1: TForm1;
  i:integer;
  mulai:boolean;
implementation

{$R *.dfm}

procedure TForm1.FormCreate(Sender: TObject);
begin
  textfader1.Active:=true;
  p1.OpenDriver;
  if (not p1.ActiveHW) then
    MessageDlg('LPT Port (378h) Error!', mtError, [mbOK], 0)

end;

procedure TForm1.Timer1Timer(Sender: TObject);
begin
  inc(i);
  if i=61 then
  begin
   i:=0;
   series1.Clear;
  end;
end;

procedure TForm1.btstartClick(Sender: TObject);
var
   dat:array [1..3] of integer;
   nilai:integer;
   a:byte;
```

```
begin
  btstart.Enabled:=false;
  btstop.Enabled:=true;
  mulai:=true;
  a:=0;
  i:=0;
  timer1.Enabled:=true;
while mulai=true do
begin
  if (p1.Port[$378+1] and $40) = $40 then
  begin
    inc(a);
    dat[a]:=p1.Port[$378+2] xor 11;
    dat[a]:=not dat[a];
    label1.Caption:=inttostr(dat[a]);
    while (p1.Port[$378+1] and $40) = $40 do
    begin
    application.ProcessMessages;
    if mulai=false then exit;
    end;
    if a=3 then
    begin
      dat[1]:=dat[1] shl 8;
      dat[2]:=dat[2] shl 4;
      nilai:=dat[1] or dat[2] or dat[3];
      a:=0;
      series1.AddXY(i,nilai);
    end;
  end;
  application.ProcessMessages;
end;
end;

procedure TForm1.btstopClick(Sender: TObject);
begin
  btstart.Enabled:=true;
  btstop.Enabled:=false;
  mulai:=false;
  timer1.Enabled:=false;
end;

procedure TForm1.FormClose(Sender: TObject; var Action: TCloseAction);
begin
  application.Terminate;
end;

procedure TForm1.Timer2Timer(Sender: TObject);
begin
  l1.Caption:=timetostr(now);
end;

end.
```

LAMPIRAN C

FOTO ALAT

Rangkaian Pemancar



Rangkaian Penerima

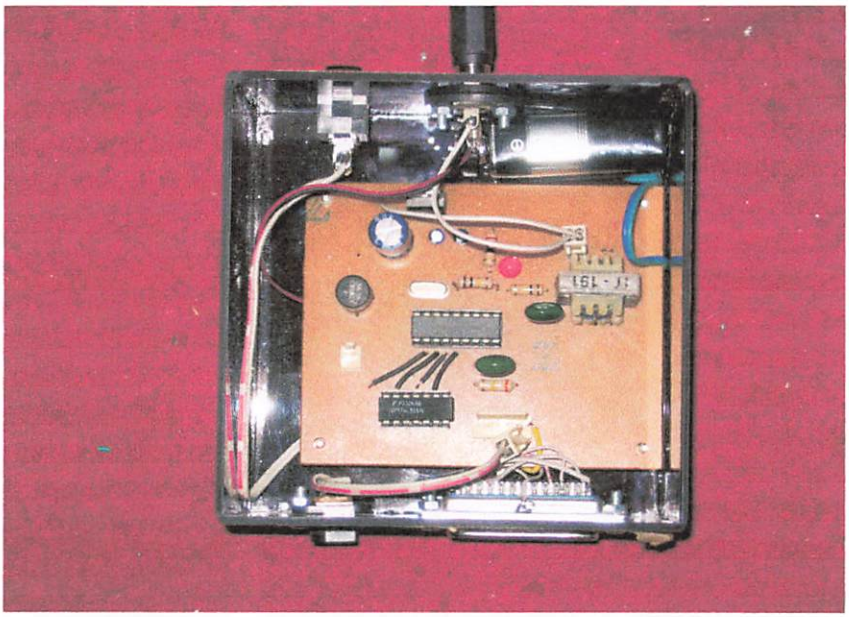
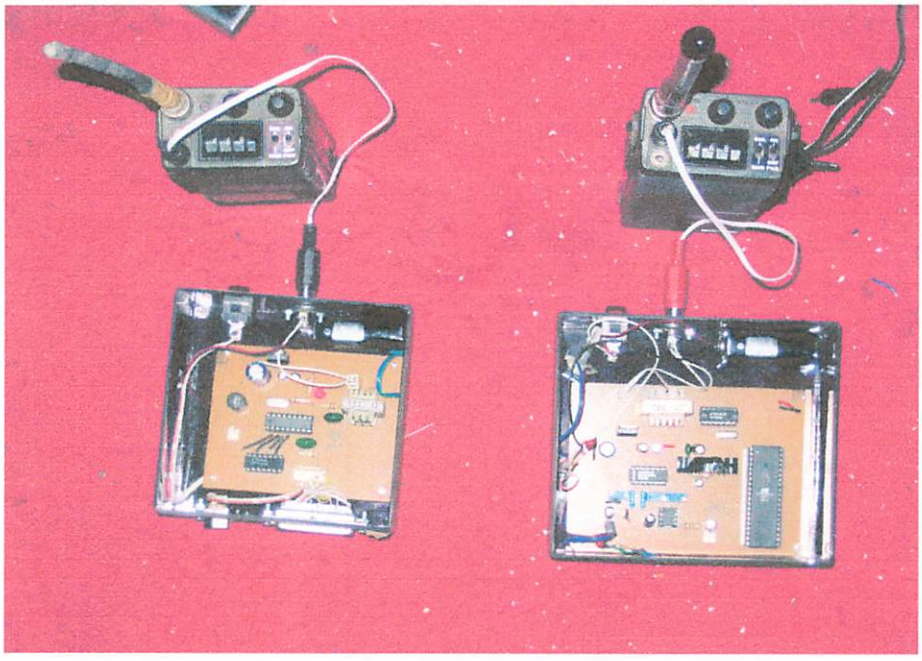
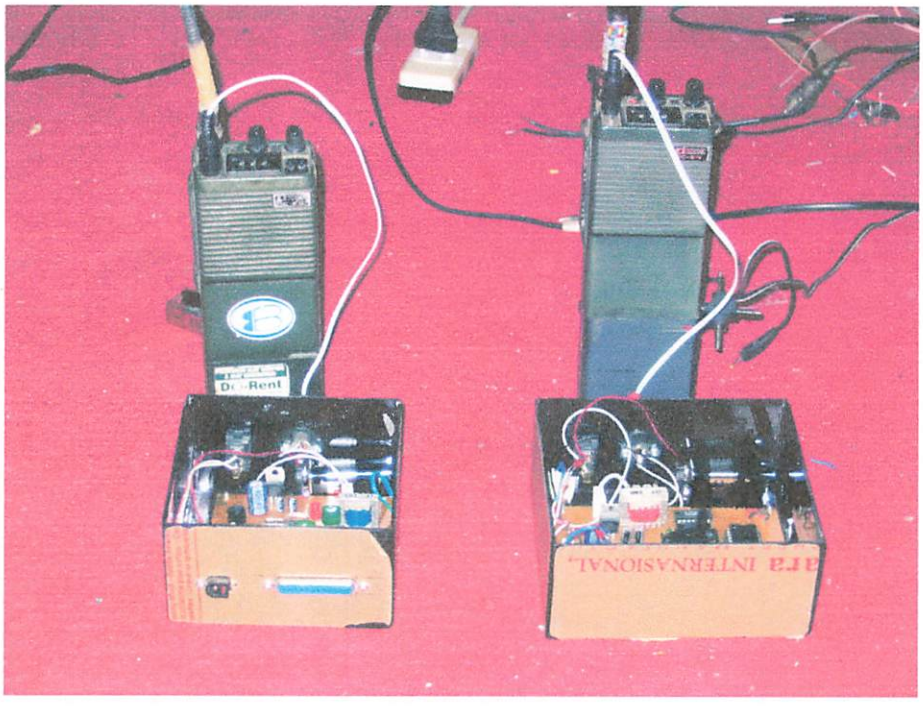


Foto Alat Keseluruhan

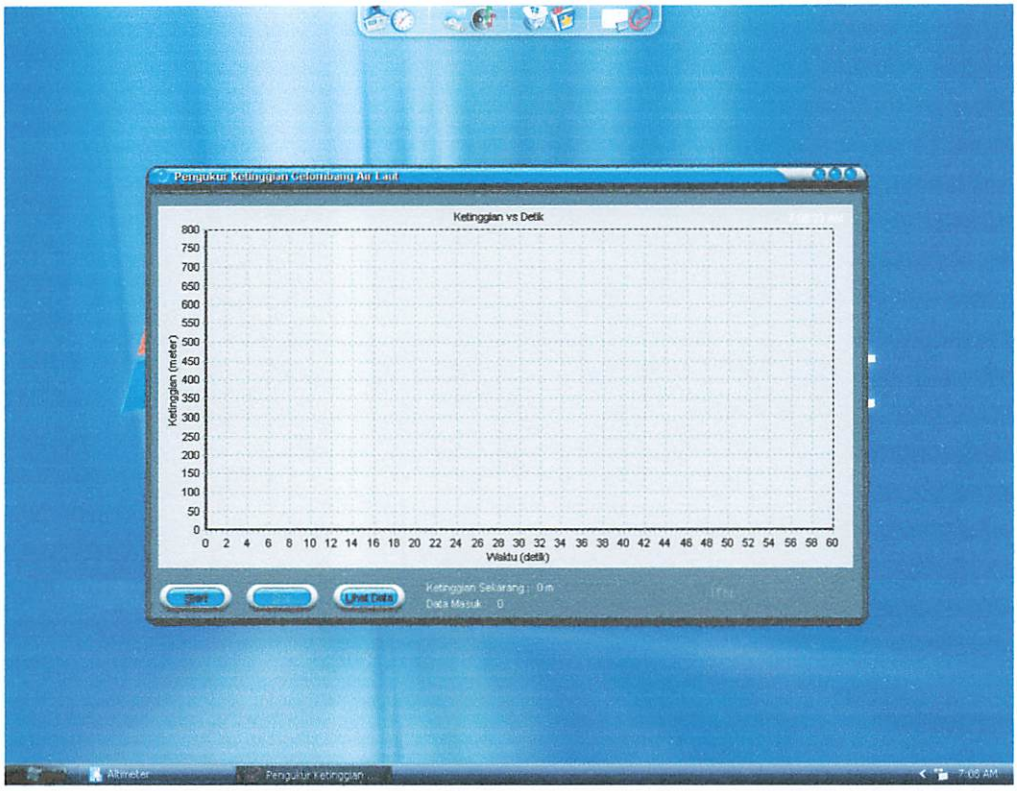
Tampak Atas



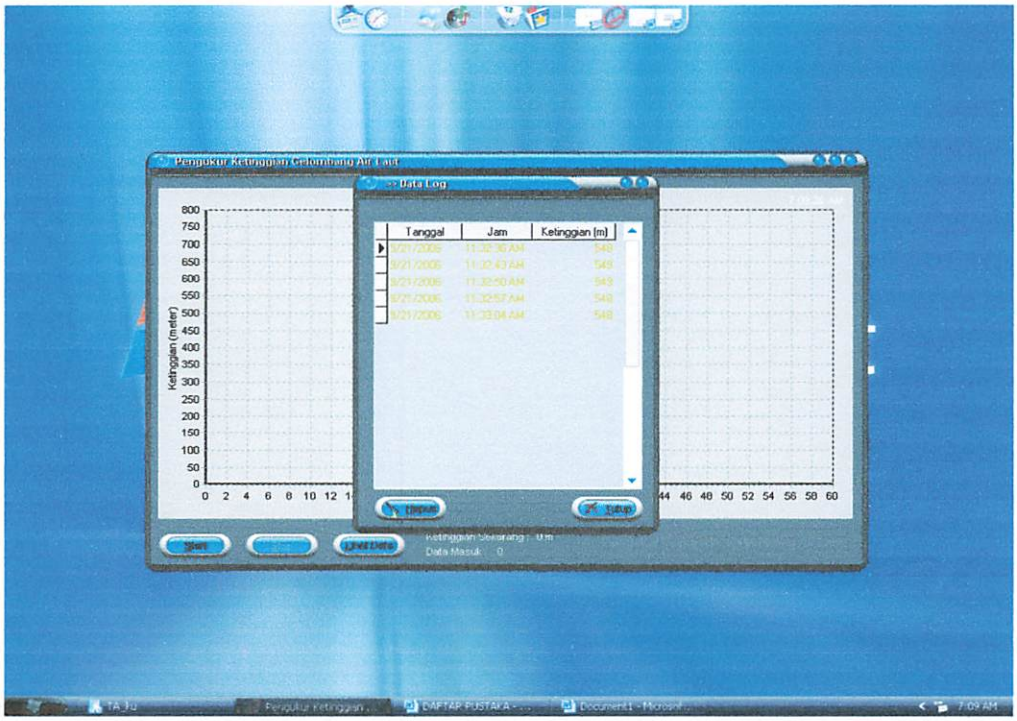
Tampak Samping



Tampilan grafik pengukur ketinggian gelombang air laut
Ketinggian (m) terhadap waktu (detik)



Tampilan data base hasil uji pengukuran ketinggian gelombang air laut
Ketinggian (m) terhadap waktu (detik)



DATA SHEET

Integrated Silicon Pressure Sensor for Manifold Absolute Pressure, Altimeter or Barometer Applications On-Chip Signal Conditioned, Temperature Compensated and Calibrated

MPX4115A
MPXA4115A
SERIES

INTEGRATED PRESSURE SENSOR
15 to 115 kPa (2.2 to 16.7 psi)
0.2 to 4.8 Volts Output

Motorola's MPX4115A/MPXA4115A series sensor integrates on–chip, bipolar op amp circuitry and thin film resistor networks to provide a high output signal and temperature compensation. The small form factor and high reliability of on–chip integration make the Motorola pressure sensor a logical and economical choice for the system designer.

The MPX4115A/MPXA4115A series piezoresistive transducer is a state–of–the–art, monolithic, signal conditioned, silicon pressure sensor. This sensor combines advanced micromachining techniques, thin film metallization, and bipolar semiconductor processing to provide an accurate, high level analog output signal that is proportional to applied pressure.

Figure 1 shows a block diagram of the internal circuitry integrated on a pressure sensor chip.

Features

- 1.5% Maximum Error over 0° to 85°C
- Ideally suited for Microprocessor or Microcontroller–Based Systems
- Temperature Compensated from –40° to +125°C
- Durable Epoxy Unibody Element or Thermoplastic (PPS) Surface Mount Package

Application Examples

- Aviation Altimeters
- Industrial Controls
- Engine Control
- Weather Stations and Weather Reporting Devices

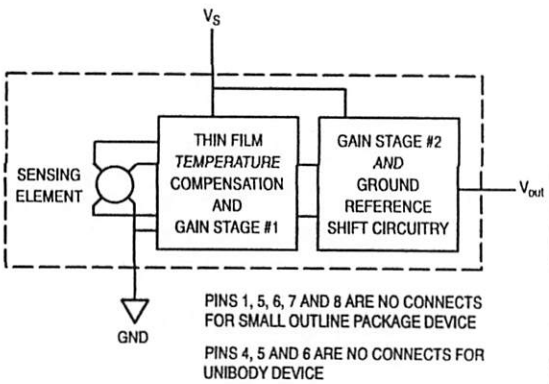
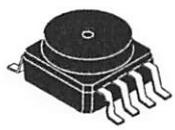
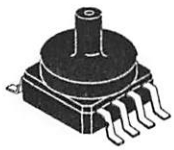


Figure 1. Fully Integrated Pressure Sensor Schematic

SMALL OUTLINE PACKAGE



MPXA4115A6U
CASE 482



MPXA4115AC6U
CASE 482A

PIN NUMBER			
1	N/C	5	N/C
2	V_S	6	N/C
3	Gnd	7	N/C
4	V_{out}	8	N/C

NOTE: Pins 1, 5, 6, 7, and 8 are internal device connections. Do not connect to external circuitry or ground. Pin 1 is noted by the notch in the lead.

UNIBODY PACKAGE

MPX4115A
CASE 867

MPX4115AP
CASE 867B

MPX4115AS
CASE 867E

PIN NUMBER			
1	V_{out}	4	N/C
2	Gnd	5	N/C
3	V_S	6	N/C

NOTE: Pins 4, 5, and 6 are internal device connections. Do not connect to external circuitry or ground. Pin 1 is noted by the notch in the lead.

REV 4

MAXIMUM RATINGS(NOTE)

Parametrics	Symbol	Value	Units
Maximum Pressure (P1 > P2)	P_{max}	400	kPa
Storage Temperature	T_{stg}	–40° to +125°	°C
Operating Temperature	T_A	–40° to +125°	°C

NOTE: Exposure beyond the specified limits may cause permanent damage or degradation to the device.

OPERATING CHARACTERISTICS (V_S = 5.1 Vdc, T_A = 25°C unless otherwise noted, P1 > P2. Decoupling circuit shown in Figure 3 required to meet Electrical Specifications.)

Characteristic		Symbol	Min	Typ	Max	Unit
Pressure Range		P_{OP}	15	—	115	kPa
Supply Voltage(1)		V_S	4.85	5.1	5.35	Vdc
Supply Current		I_o	—	7.0	10	mAdc
Minimum Pressure Offset(2) @ V_S = 5.1 Volts	(0 to 85°C)	V_{off}	0.135	0.204	0.273	Vdc
Full Scale Output(3) @ V_S = 5.1 Volts	(0 to 85°C)	V_{FSO}	4.725	4.794	4.863	Vdc
Full Scale Span(4) @ V_S = 5.1 Volts	(0 to 85°C)	V_{FSS}	4.521	4.590	4.659	Vdc
Accuracy(5)	(0 to 85°C)	—	—	—	±1.5	$\%V_{FSS}$
Sensitivity		V/P	—	45.9	—	mV/kPa
Response Time(6)		t_R	—	1.0	—	ms
Output Source Current at Full Scale Output		I_{o+}	—	0.1	—	mAdc
Warm–Up Time(7)		—	—	20	—	ms
Offset Stability(8)		—	—	*±0.5*	—	$\%V_{FSS}$

NOTES:

1. Device is ratiometric within this specified excitation range.
2. Offset (V_{off}) is defined as the output voltage at the minimum rated pressure.
3. Full Scale Output (V_{FSO}) is defined as the output voltage at the maximum or full rated pressure.
4. Full Scale Span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.
5. Accuracy is the deviation in actual output from nominal output over the entire pressure range and temperature range as a percent of span at 25°C due to all sources of error including the following:
   - Linearity: Output deviation from a straight line relationship with pressure over the specified pressure range.
   - Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to and from the minimum or maximum operating temperature points, with zero differential pressure applied.
   - Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from minimum or maximum rated pressure at 25°C.
   - TcSpan: Output deviation over the temperature range of 0° to 85°C, relative to 25°C.
   - TcOffset: Output deviation with minimum pressure applied, over the temperature range of 0° to 85°C, relative to 25°C.
6. Response Time is defined as the time for the incremental change in the output to go from 10% to 90% of its final value when subjected to a specified step change in pressure.
7. Warm–up Time is defined as the time required for the product to meet the specified output voltage after the pressure has been stabilized.
8. Offset Stability is the product's output deviation when subjected to 1000 cycles of Pulsed Pressure, Temperature Cycling with Bias Test.

MECHANICAL CHARACTERISTICS

Characteristics	Typ	Unit
Weight, Basic Element (Case 867)	4.0	grams
Weight, Small Outline Package (Case 482)	1.5	grams

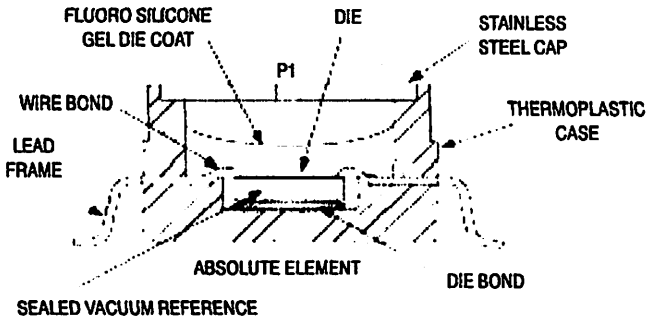


Figure 2. Cross Sectional Diagram SOP (not to scale)

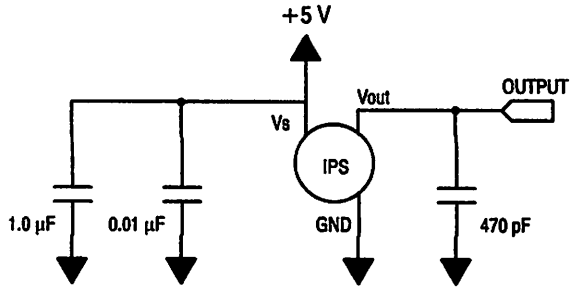


Figure 3. Recommended power supply decoupling and output filtering.
For additional output filtering, please refer to Application Note AN1646.

Figure 2 illustrates the absolute sensing chip in the basic chip carrier (Case 482).

Figure 3 shows the recommended decoupling circuit for interfacing the output of the integrated sensor to the A/D input of a microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

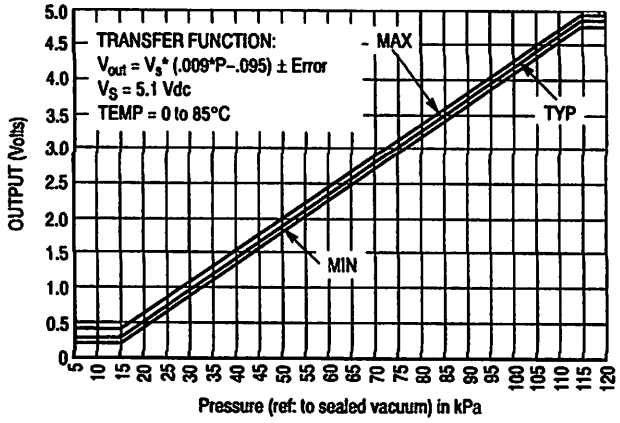


Figure 4. Output versus Absolute Pressure

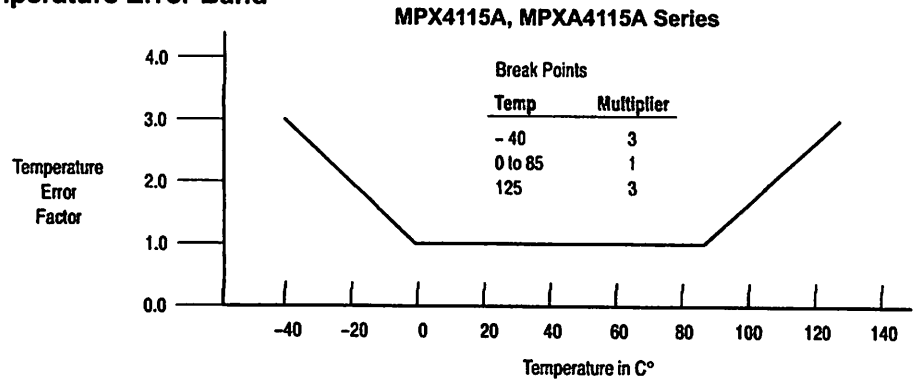
Figure 4 shows the sensor output signal relative to pressure input. Typical minimum and maximum output curves are shown for operation over 0 to 85°C temperature range. The output will saturate outside of the rated pressure range.

A fluorosilicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm. The MPX4115A/MPXA4115A series pressure sensor operating characteristics, internal reliability and qualification tests are based on use of dry air as the pressure media. Media other than dry air may have adverse effects on sensor performance and long-term reliability. Contact the factory for information regarding media compatibility in your application.

Transfer Function (MPX4115A, MPXA4115A)

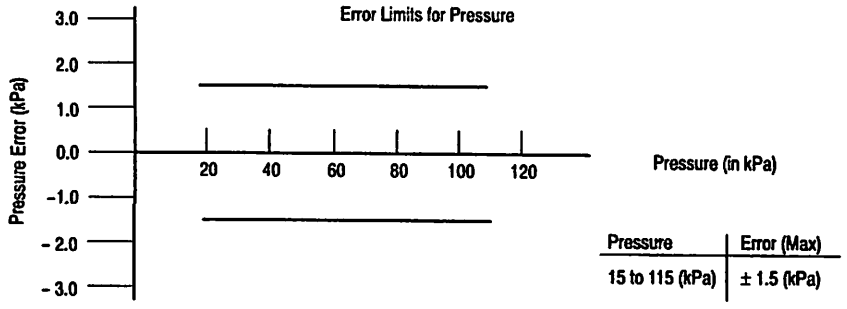
Nominal Transfer Value: $V_{out} = V_S \times (0.009 \times P - 0.095)$
$\pm$ (Pressure Error x Temp. Factor x 0.009 x V_S)
$V_S = 5.1 \pm 0.25$ Vdc

Temperature Error Band



NOTE: The Temperature Multiplier is a linear response from 0°C to –40°C and from 85°C to 125°C

Pressure Error Band



Pressure	Error (Max)
15 to 115 (kPa)	± 1.5 (kPa)

ORDERING INFORMATION — UNIBODY PACKAGE

Device Type	Options	Case No.	MPX Series Order No.	Marking
Basic Element	Absolute, Element Only	867	MPX4115A	MPX4115A
Ported Elements	Absolute, Ported	867B	MPX4115AP	MPX4115AP
	Absolute, Stove Pipe Port	867E	MPX4115AS	MPX4115A

ORDERING INFORMATION — SMALL OUTLINE PACKAGE

Device Type	Options	Case No.	MPX Series Order No.	Packing Options	Marking
Basic Element	Absolute, Element Only	482	MPXA4115A6U	Rails	MPXA4115A
	Absolute, Element Only	482	MPXA4115A6T1	Tape and Reel	MPXA4115A
Ported Element	Absolute, Axial Port	482A	MPXA4115AC6U	Rails	MPXA4115A
	Absolute, Axial Port	482A	MPXA4115AC6T1	Tape and Reel	MPXA4115A

INFORMATION FOR USING THE SMALL OUTLINE PACKAGE (CASE 482)

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct fottprint, the packages will self–align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

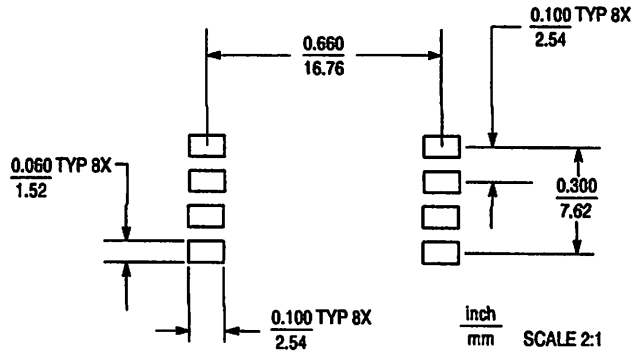
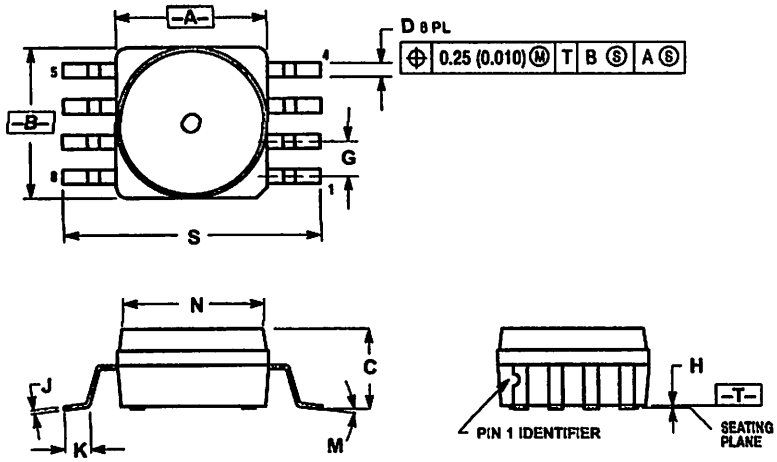


Figure 5. SOP Footprint (Case 482)

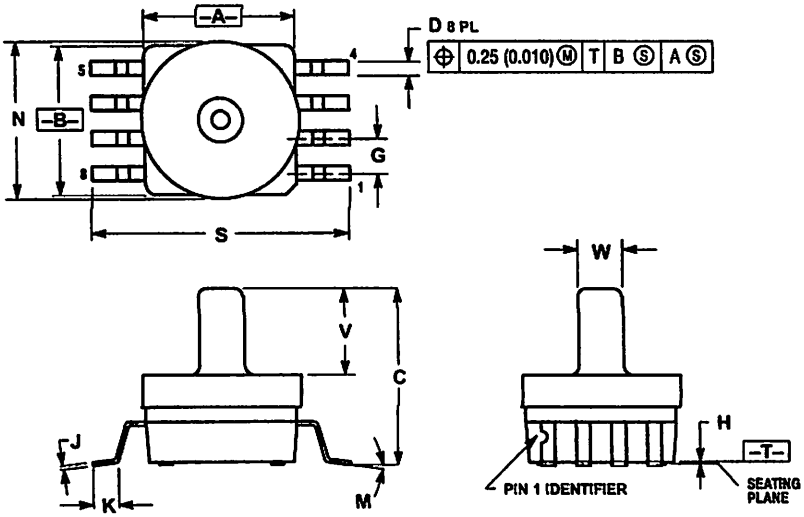
SMALL OUTLINE PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. *DIMENSION A AND B DO NOT INCLUDE MOLD* PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.212	0.230	5.38	5.84
D	0.038	0.042	0.96	1.07
G	0.100 BSC		2.54 BSC	
H	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0°	7°	0°	7°
N	0.405	0.415	10.29	10.54
S	0.709	0.725	18.01	18.41

CASE 482–01
ISSUE O

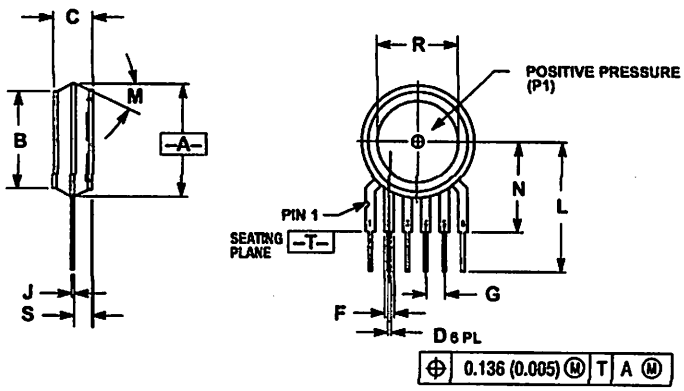


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.500	0.520	12.70	13.21
D	0.038	0.042	0.96	1.07
G	0.100 BSC		2.54 BSC	
H	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0°	7°	0°	7°
N	0.444	0.448	11.28	11.38
S	0.709	0.725	18.01	18.41
V	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

CASE 482A–01
ISSUE A

UNIBODY PACKAGE DIMENSIONS



NOTES:
9. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
10. CONTROLLING DIMENSION: INCH.
11. DIMENSION -A- IS INCLUSIVE OF THE MOLD STOP RING. MOLD STOP RING NOT TO EXCEED 16.00 (0.630).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.595	0.630	15.11	16.00
B	0.514	0.534	13.06	13.56
C	0.200	0.220	5.08	5.59
D	0.027	0.033	0.68	0.84
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.40
L	0.695	0.725	17.65	18.42
M	30 °NOM		30 °NOM	
N	0.475	0.495	12.07	12.57
R	0.430	0.450	10.92	11.43
S	0.090	0.105	2.29	2.66

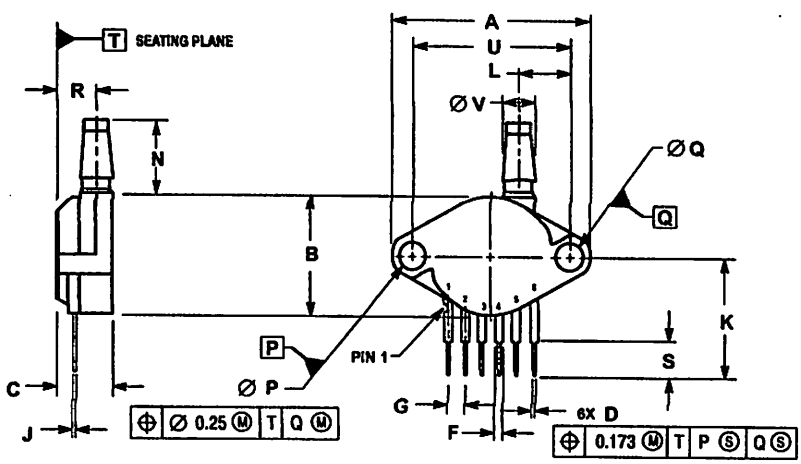
STYLE 1:
PIN 1. VOUT
2. GROUND
3. VCC
4. V1
5. V2
6. VEX

STYLE 2:
PIN 1. OPEN
2. GROUND
3. -VOUT
4. VSUPPLY
5. +VOUT
6. OPEN

STYLE 3:
PIN 1. OPEN
2. GROUND
3. +VOUT
4. +VSUPPLY
5. -VOUT
6. OPEN

CASE 867–08
ISSUE N

BASIC ELEMENT



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

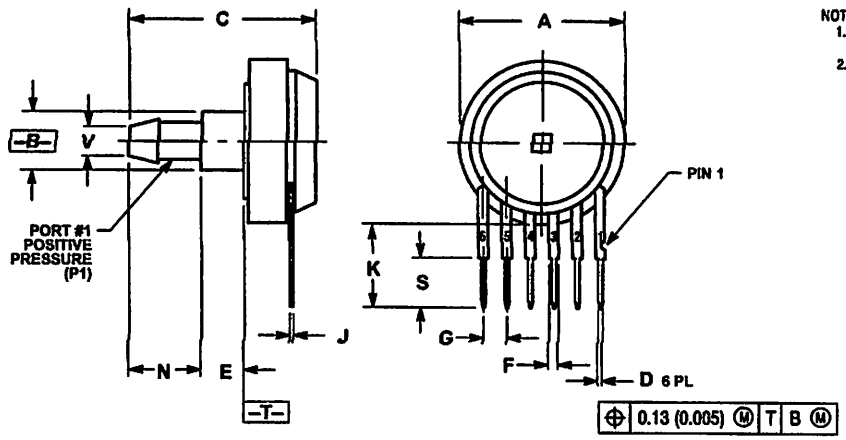
	MILLIMETERS	
DIM	MIN	MAX
A	29.08	29.65
B	17.4	18.16
C	7.75	8.26
D	0.68	0.84
F	1.22	1.63
G	2.54 BSC	
J	0.36	0.41
K	17.65	18.42
L	7.37	7.62
N	10.67	11.18
P	3.89	4.04
Q	3.89	4.04
R	5.84	6.35
S	5.59	6.1
U	23.11 BSC	
V	4.62	4.93

STYLE 1:
PIN 1. V_{OUT}
2. GROUND
3. V_{CC}
4. V1
5. V2
6. V_{EX}

CASE 867B–04
ISSUE F

PRESSURE SIDE PORTED (AP, GP)

UNIBODY PACKAGE DIMENSIONS—CONTINUED



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.690	0.720	17.53	18.28
B	0.245	0.255	6.22	6.48
C	0.780	0.820	19.81	20.82
D	0.027	0.033	0.69	0.84
E	0.178	0.186	4.52	4.72
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.41
K	0.345	0.375	8.76	9.53
N	0.300	0.310	7.62	7.87
S	0.220	0.240	5.59	6.10
V	0.182	0.194	4.62	4.93

STYLE 1:
PIN 1. V_{OUT}
2. GROUND
3. V_{CC}
4. V1
5. V2
6. V_{EX}

CASE 867E–03
ISSUE D

PRESSURE SIDE PORTED (AS, GS)

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19-1407; Rev 3; 8/99

MAXIM

SOT23, Rail-to-Rail, Fixed-Gain GainAmps/Open-Loop Op Amps

General Description

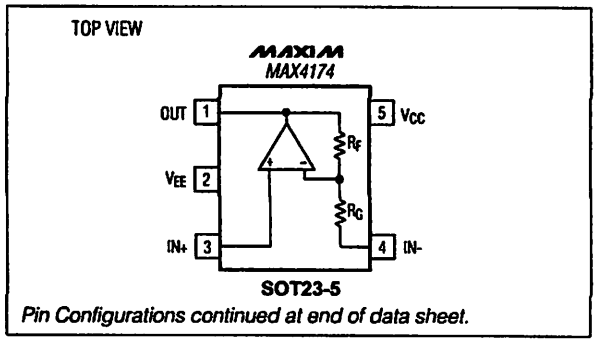
The MAX4174/MAX4175/MAX4274/MAX4275 GainAmp™ family combines a low-cost Rail-to-Rail® op amp with precision internal gain-setting resistors and VCC / 2 biasing. Factory-trimmed on-chip resistors decrease design size, cost, and layout, and provide 0.1% gain accuracy. Fixed inverting gains from -0.25V/V to -100V/V or noninverting gains from +1.25V/V to +101V/V are available. These devices operate from a single +2.5V to +5.5V supply and consume only 300µA. GainAmp amplifiers are optimally compensated for each gain version, achieving exceptional GBW products up to 23MHz (AV = +25V/V to +101V/V). High-voltage fault protection withstands ±17V at either input without excessive current draw.

Three versions are available in this amplifier family: single/dual/quad open-loop, unity-gain stable (MAX4281/MAX4282/MAX4284); single/dual fixed gain (MAX4174/MAX4274); and single/dual fixed gain plus internal VCC / 2 bias at the noninverting input (MAX4175/MAX4275), which simplifies input biasing in single-supply designs. The input common-mode voltage range of the open-loop amplifiers extends from 150mV below the negative supply to within 1.2V of the positive supply. The outputs can swing rail-to-rail and drive a 1kΩ load while maintaining excellent DC accuracy. The amplifier is stable for capacitive loads up to 470pF.

Applications

Portable Instruments	Smart-Card Readers
Instruments, Terminals, and Bar-Code Readers	Infrared Receivers for Remote Controls
Keyless Entry	Low-Side Current-Sense Amplifiers
Photodiode Preamps	

Pin Configurations



SOT23-5

Pin Configurations continued at end of data sheet.

Features

- ♦ **GainAmp Family Provides Internal Precision Gain-Setting Resistors in SOT23 (MAX4174/5)**
- ♦ **0.1% Gain Accuracy (RF/RG) (MAX4174/5, MAX4274/5)**
- ♦ **54 Standard Gains Available (MAX4174/5, MAX4274/5)**
- ♦ **Open-Loop Unity-Gain-Stable Op Amps (MAX4281/2/4)**
- ♦ ***Rail-to-Rail Outputs Drive 1kΩ Load***
- ♦ **Internal VCC / 2 Biasing (MAX4175/MAX4275)**
- ♦ **+2.5V to +5.5V Single Supply**
- ♦ **300µA Supply Current**
- ♦ **Up to 23MHz GBW Product**
- ♦ **Fault-Protected Inputs Withstand ±17V**
- ♦ **Stable with Capacitive Loads Up to 470pF with No Isolation Resistor**

Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX4174_EUK-T	-40°C to +85°C	5 SOT23-5	††
MAX4175_EUK-T	-40°C to +85°C	5 SOT23-5	††

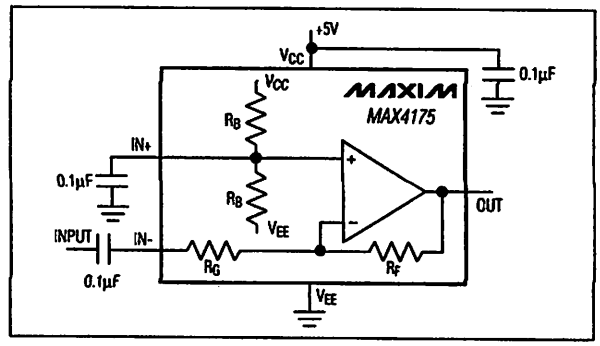
Ordering Information continued at end of data sheet.

* *Insert the desired gain code (from the Gain Selection Guide) in the blank to complete the part number.*

†† *Refer to the Gain Selection Guide for a list of preferred gains and SOT Top Marks.*

Selector Guide appears at end of data sheet.

Typical Operating Circuit



†*Patent pending*

GainAmp is a trademark of Maxim Integrated Products. Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

ELECTRICAL CHARACTERISTICS—MAX4174/MAX4175/MAX4274/MAX4275 Fixed-Gain Amplifiers (continued)

(V_{CC} = +2.5V to +5.5V, V_{EE} = 0, V_{IN+} = V_{IN-} = V_{CC} / 2, R_L to V_{CC} / 2, R_L = open, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Up Time		Output settling to 1%		1		ms
Slew Rate	SR	V_{CC} = 5V, V_{OUT} = 4V step		0.7		V/µs
Settling Time to Within 0.01%		V_{CC} = 5V, V_{OUT} = 4V step		7		µs
Input Noise Voltage Density	e_n	f = 10kHz (Note 5)		90		nV/√Hz
Input Noise Current Density	i_n	f = 10kHz		4		fA/√Hz
Capacitive Load Stability	C_{LOAD}	No sustained oscillations		470		pF
DC Gain Accuracy		(V_{EE} + 25mV) < V_{OUT} < (V_{CC} - 25mV), R_L = 100kΩ *(Note 6)*		0.1	0.5	%
-3dB Bandwidth	BW_{-3dB}	Gain = +1.25V/V		1700		kHz
		Gain = +3V/V		970		
		Gain = +5V/V		970		
		Gain = +10V/V		640		
		Gain = +25V/V		590		
		Gain = +51V/V		330		

ELECTRICAL CHARACTERISTICS—MAX4281/MAX4282/MAX4284 Open-Loop Op Amps

(V_{CC} = +2.5V to +5.5V, V_{EE} = 0, V_{IN+} = V_{IN-} = V_{CC} / 2, R_L to V_{CC} / 2, R_L = open, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Note 1)

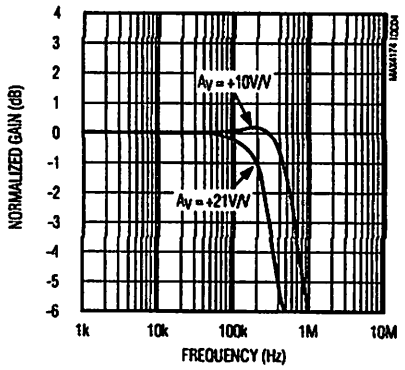
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Guaranteed by PSRR tests	2.5		5.5	V
Supply Current (per Amplifier)	I_{CC}	V_{CC} = 3V		290	450	µA
		V_{CC} = 5V		320	500	µA
Input Offset Voltage	V_{OS}	R_L = 100kΩ		±0.5	±2	mV
Input Offset Voltage Drift				±5		µV/°C
Input Bias Current	I_{BIAS}			±0.05	±10	nA
Input Offset Current	I_{OS}			±10	±1000	pA
Input Resistance	R_{IN}	Differential or common mode		1000		MΩ
Input Capacitance	C_{IN}			2.5		pF
Common-Mode Input Voltage Range	CMVR	Guaranteed by CMRR test	V_{EE} - 0.15		V_{CC} - 1.2	V
Common-Mode Rejection Ratio	CMRR	V_{EE} - 0.15V ≤ V_{CM} ≤ V_{CC} - 1.2V	60	90		dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.5V to 5.5V	70	90		dB
Closed-Loop Output Impedance	R_{OUT}	A_V = 1V/V		0.02		Ω

Typical Operating Characteristics (continued)

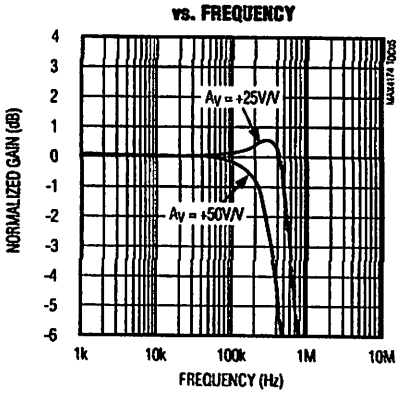
(V_{CC} = +5V, R_L = 100kΩ to V_{CC} / 2, small-signal V_{OUT} = 100mVp-p, large-signal V_{OUT} = 1Vp-p, T_A = +25°C, unless otherwise noted.)

MAX4174/MAX4175

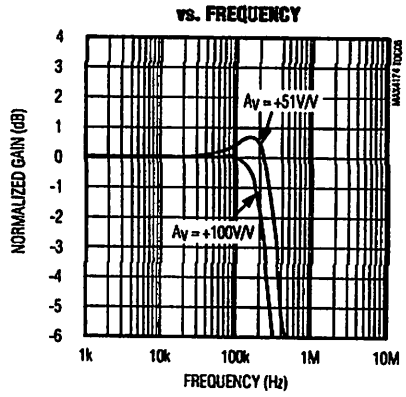
LARGE-SIGNAL GAIN vs. FREQUENCY



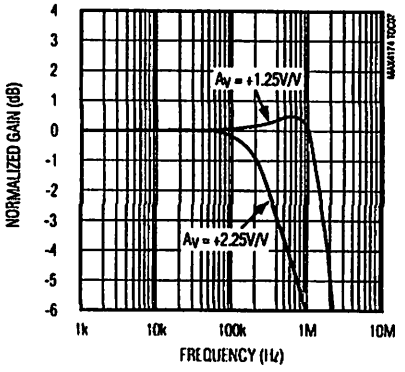
LARGE-SIGNAL GAIN vs. FREQUENCY



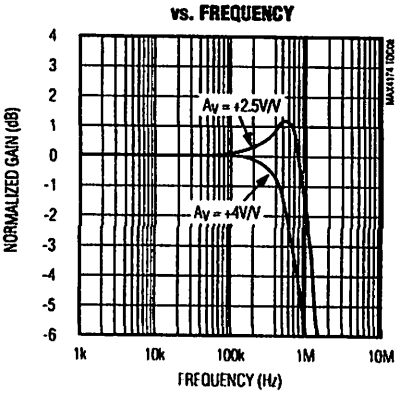
LARGE-SIGNAL GAIN vs. FREQUENCY



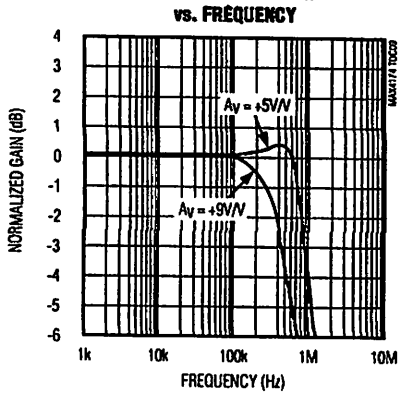
SMALL-SIGNAL GAIN vs. FREQUENCY



SMALL-SIGNAL GAIN vs. FREQUENCY



SMALL-SIGNAL GAIN vs. FREQUENCY



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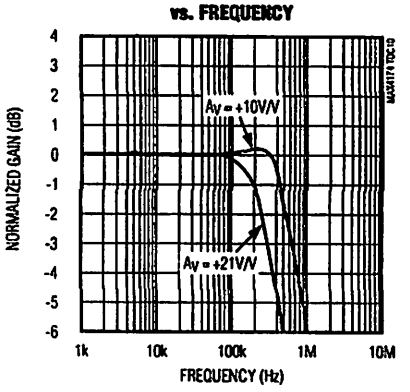

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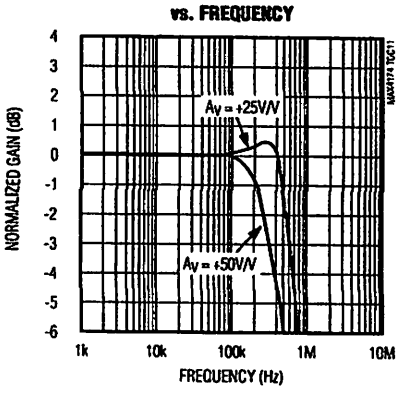
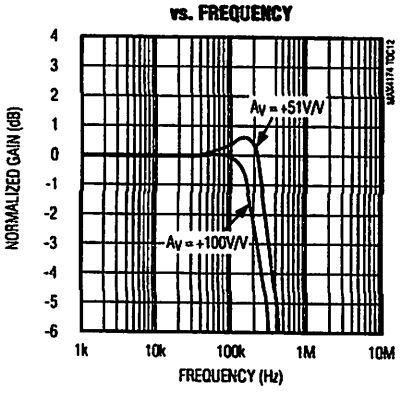


SMALL-SIGNAL GAIN vs. FREQUENCY

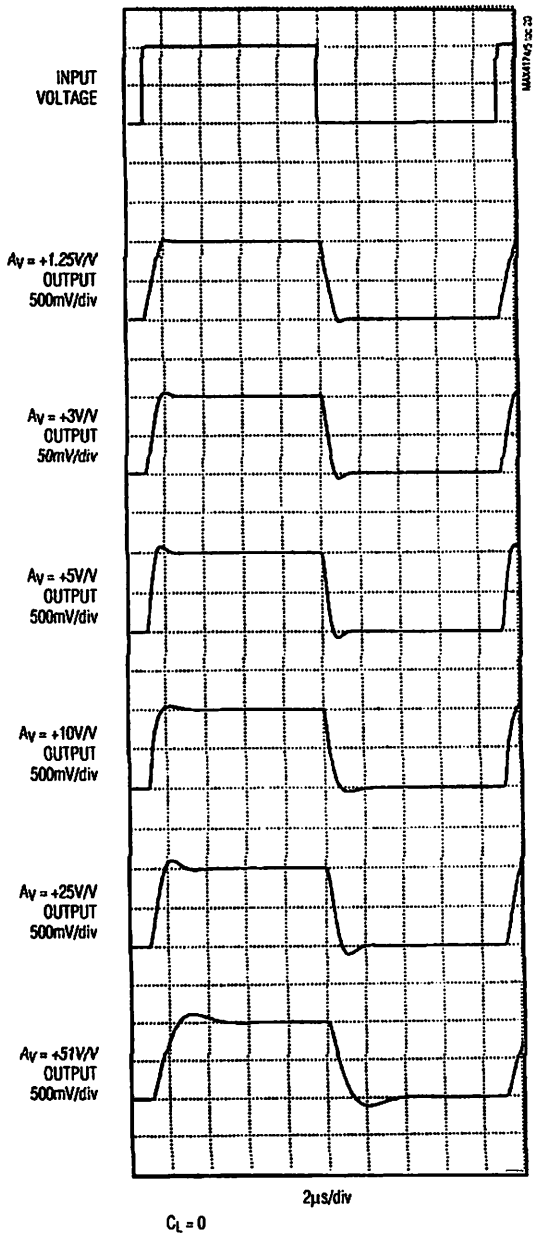


Typical Operating Characteristics (continued)

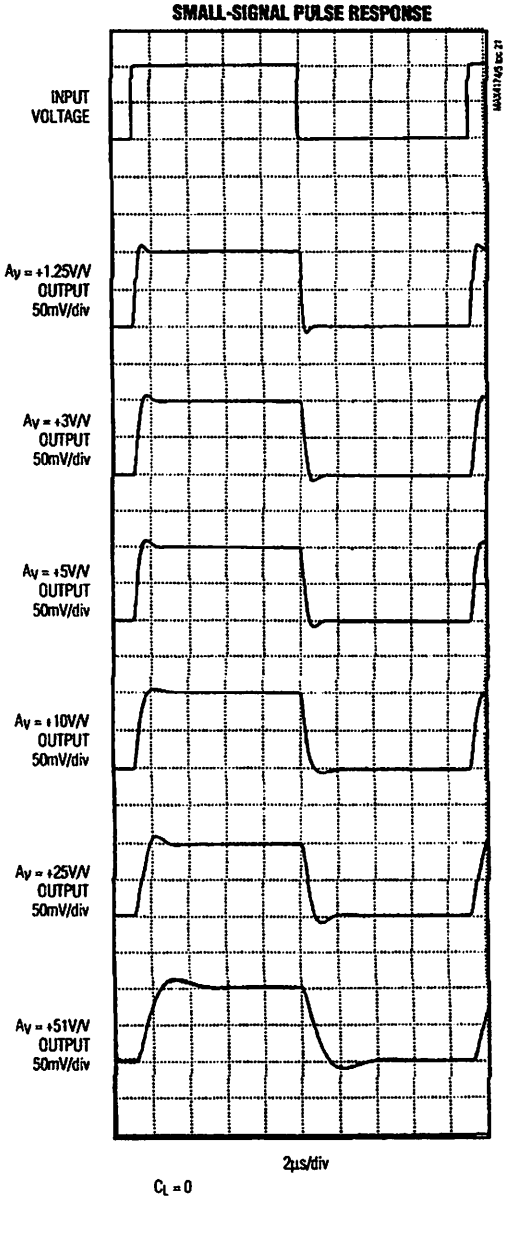
(V_{CC} = +5V, R_L = 100kΩ to V_{CC} / 2, small-signal V_{OUT} = 100mVp-p, large-signal V_{OUT} = 1Vp-p, T_A = +25°C, unless otherwise noted.)

MAX4174/MAX4175

LARGE-SIGNAL PULSE RESPONSE



SMALL-SIGNAL PULSE RESPONSE

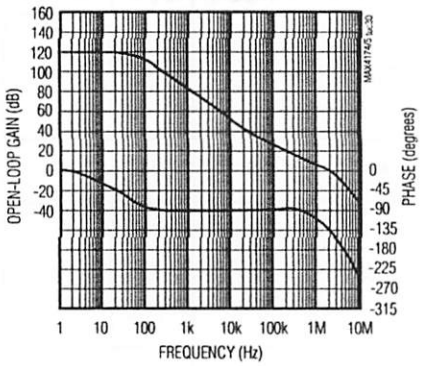


Typical Operating Characteristics

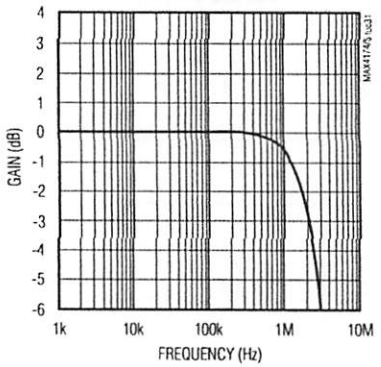
(V_{CC} = +5V, R_L = 100kΩ to V_{CC} / 2, small-signal V_{OUT} = 100mVp-p, large-signal V_{OUT} = 1Vp-p, T_A = +25°C, unless otherwise noted.)

MAX4281/MAX4282/MAX4284

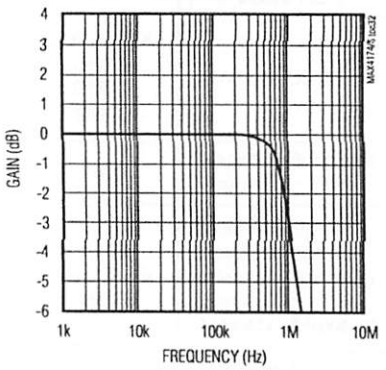
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



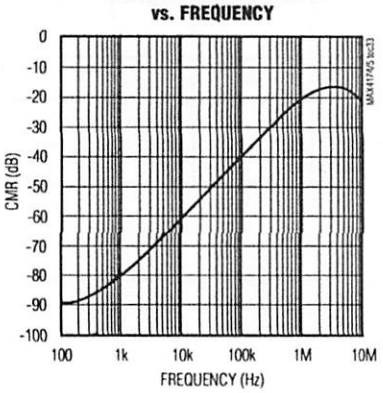
SMALL-SIGNAL GAIN vs. FREQUENCY



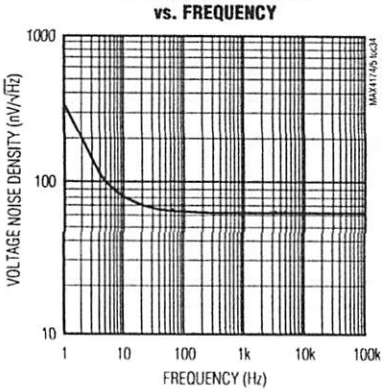
LARGE-SIGNAL GAIN vs. FREQUENCY



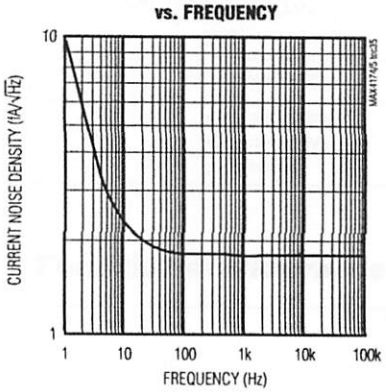
COMMON-MODE REJECTION vs. FREQUENCY



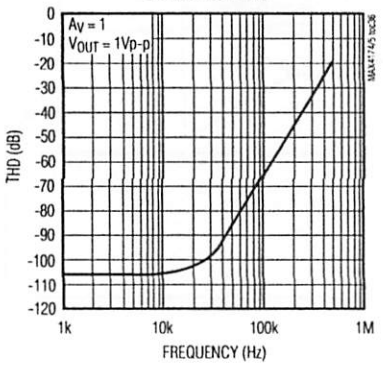
VOLTAGE NOISE DENSITY vs. FREQUENCY



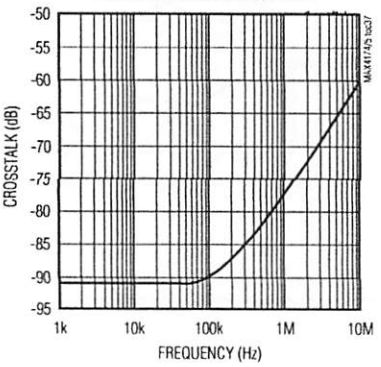
CURRENT NOISE DENSITY vs. FREQUENCY



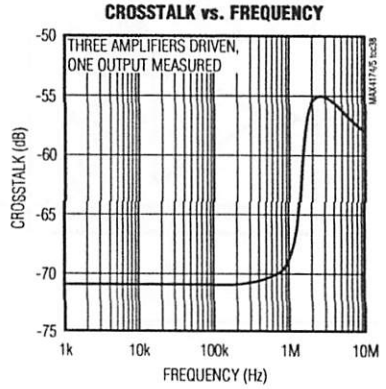
TOTAL HARMONIC DISTORTION vs. FREQUENCY



MAX4282 CROSSTALK vs. FREQUENCY



MAX4284 CROSSTALK vs. FREQUENCY



Detailed Description

Maxim's GainAmp fixed-gain amplifiers combine a low-cost rail-to-rail op amp with internal gain-setting resistors. Factory-trimmed on-chip resistors provide 0.1% gain accuracy while decreasing design size, cost, and layout. Three versions are available in this amplifier family: single/dual/quad open-loop, unity-gain-stable devices (MAX4281/MAX4282/MAX4284); single/dual fixed-gain devices (MAX4174/MAX4274); and single/dual devices with fixed gain plus internal V_{CC} / 2 bias at the noninverting input (MAX4175/MAX4275). All amplifiers feature rail-to-rail outputs and drive a 1kΩ load while maintaining excellent DC accuracy.

Open-Loop Op Amps

The single/dual/quad MAX4281/MAX4282/MAX4284 are high-performance, open-loop op amps with rail-to-rail outputs. These devices are compensated for unity-gain stability, and feature a gain bandwidth (GBW) of 2MHz. The op amps in these ICs feature an input common-mode range that extends from 150mV below the negative rail to within 1.2V of the positive rail. These high performance op amps serve as the core for this family of GainAmp fixed-gain amplifiers. Although the -3dB bandwidth will not correspond to that of a fixed-gain amplifier in higher gain configurations, these open-loop op-amps can be used to prototype designs.

Internal Gain-Setting Resistors

Maxim's proprietary laser trimming techniques produce the necessary R_F/R_G values (Figure 1), so many gain offerings are easily available. These GainAmp fixed-gain amplifiers feature a negative-feedback resistor network that is laser trimmed to provide a gain-setting feedback ratio (R_F/R_G) with 0.1% typical accuracy. The standard op amp pinouts allow the GainAmp fixed-gain amplifiers to drop in directly to existing board designs, easily replacing op-amp-plus-resistor gain blocks.

GainAmp Bandwidth

GainAmp fixed-gain amplifiers feature factory-trimmed precision resistors to provide fixed inverting gains from -0.25V/V to -100V/V or noninverting gains from +1.25V/V to +101V/V. The op-amp core is decompensated strategically over the gain-set options to maximize bandwidth. Open-loop decompensation increases GBW product, ensuring that usable bandwidth is maintained with increasing closed-loop gains. A GainAmp with a fixed gain of A_V = 100V/V has a -3dB bandwidth of 230kHz. By comparison, a unity-gain-stable op amp configured for A_V = 100V/V would yield a -3dB bandwidth of only 20kHz (Figure 2). Decompensation is performed at five intermediate gain sets, as shown in the *Gain Selection Guide*. Low gain decompensation greatly increases usable bandwidth, while decompensation above gains of +25V/V offers diminished returns.

V_{CC} / 2 Internal Bias

The MAX4175/MAX4275 GainAmp fixed-gain amplifiers with the V_{CC} / 2 bias option are identical to standard GainAmp fixed-gain amplifiers, with the added feature of V_{CC} / 2 internal bias at the noninverting inputs. Two 150kΩ resistors form a voltage-divider for self-biasing the noninverting input, eliminating external bias resistors for AC-coupled applications, and allowing maximum signal swing at the op amp's rail-to-rail output for single-supply systems (see *Typical Operating Circuit*). For DC-coupled applications, use the MAX4174/MAX4274.

High-Voltage (±17V) Input Fault Protection

The MAX4174/MAX4175/MAX4274/MAX4275 include ±17V input fault protection. For normal operation, see the input voltage range specification in the *Electrical Characteristics*. Overdriven inputs up to ±17V will not

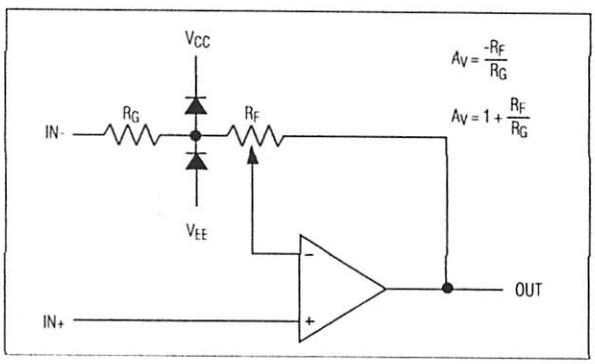


Figure 1. Internal Gain-Setting Resistors

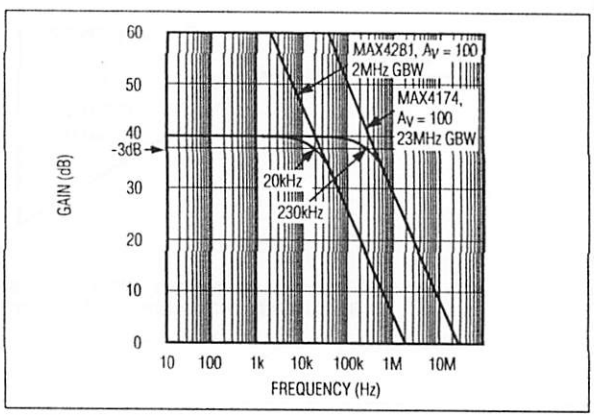


Figure 2. Gain-Bandwidth Comparison

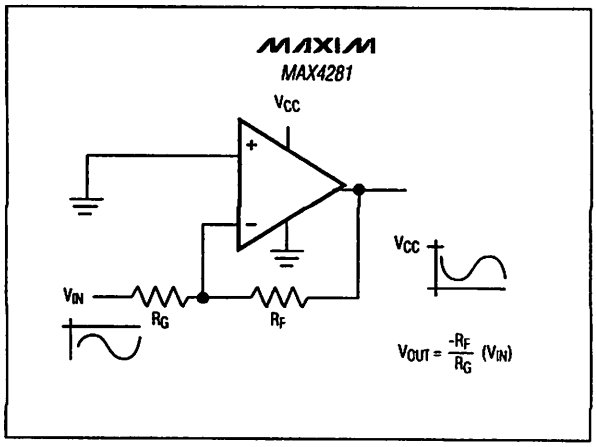


Figure 4. Single-Supply, DC-Coupled Inverting Amplifier with Negative Input Voltage

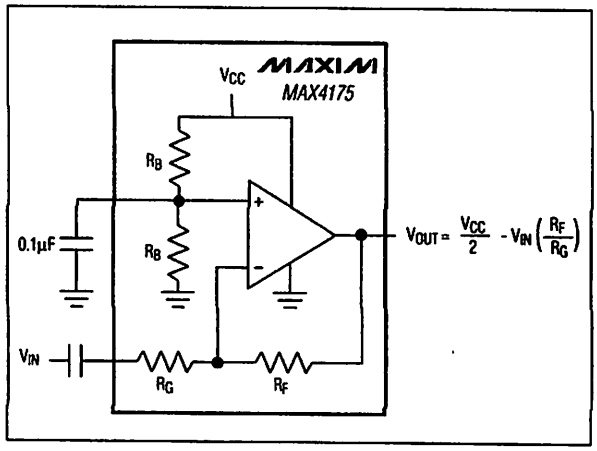


Figure 6. Single-Supply, AC-Coupled Inverting Amplifier

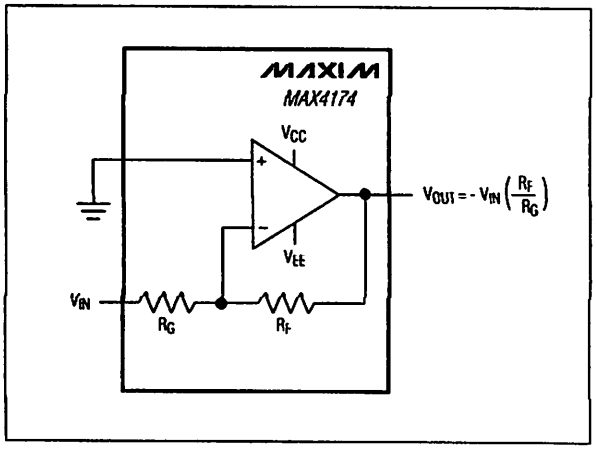


Figure 5. Dual-Supply, DC-Coupled Inverting Amplifier

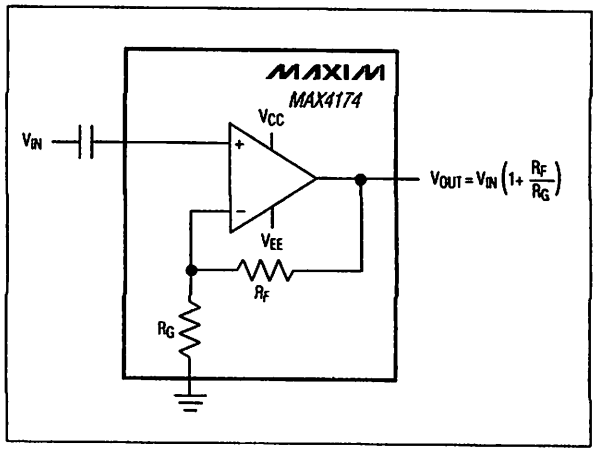


Figure 7. Dual-Supply, AC-Coupled Noninverting Amplifier

GainAmp Signal Coupling and Configurations

Common op-amp configurations include both noninverting and inverting amplifiers. Figures 5–8 show various single and dual-supply circuit configurations. Single-supply systems benefit from a midsupply bias on the noninverting input (provided internally on MAX4175/MAX4275), as this produces a quiescent DC level at the center of the rail-to-rail output stage signal swing. For dual-supply systems, ground-referenced signals may be DC-coupled into the inverting or noninverting inputs.

IN_+ Filter on MAX4175/MAX4275

Internal resistor biasing of the VCC / 2 bias options couples power-supply noise directly to the op amp's noninverting input. To minimize high-frequency power-supply noise coupling, add a 1µF to 0.1µF capacitor from IN+ to ground to create a lowpass filter (Figure 6). The lowpass filter resulting from the internal bias resistors and added capacitor can help eliminate higher frequency power-supply noise coupling through the noninverting input.

Supply Bypassing and Board Layout

All devices in the GainAmp family operate from a +2.5V to +5.5V single supply or from ±1.25V to ±2.75V dual supplies. For single-supply operation, bypass the power supply with a 0.1µF capacitor to ground. For dual supplies, bypass each supply to ground. Bypass with capacitors as close to the device as possible, to minimize lead inductance and noise. A printed circuit board with a low-inductance ground plane is recommended.

Capacitive-Load Stability

Driving large capacitive loads can cause instability in most low-power, rail-to-rail output amplifiers. The fixed-gain amplifiers of this GainAmp family are stable with capacitive loads up to 470pF. Stability with higher capacitive loads can be improved by adding an isolation resistor in series with the op-amp output, as shown in Figure 9. This resistor improves the circuit's phase margin by isolating the load capacitor from the amplifier's output. In Figure 10, a 1000pF capacitor is driven with a 100Ω isolation resistor exhibiting some overshoot but no oscillation. Figures 11 and 12 show the typical small-signal pulse responses of GainAmp fixed-gain amplifiers with 250pF and 470pF capacitive loads and no isolation resistor.

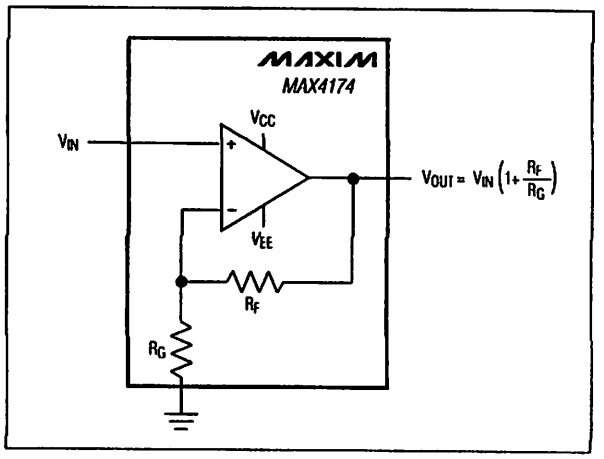


Figure 8. Dual-Supply, DC-Coupled Noninverting Amplifier

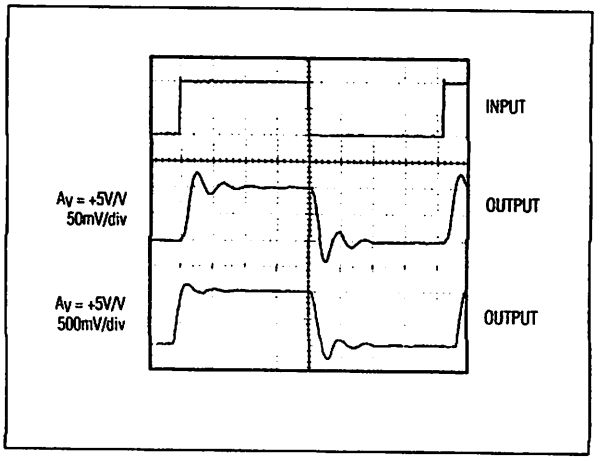


Figure 10. Small-Signal/Large-Signal Transient Response with Excessive Capacitive Load with Isolation Resistor

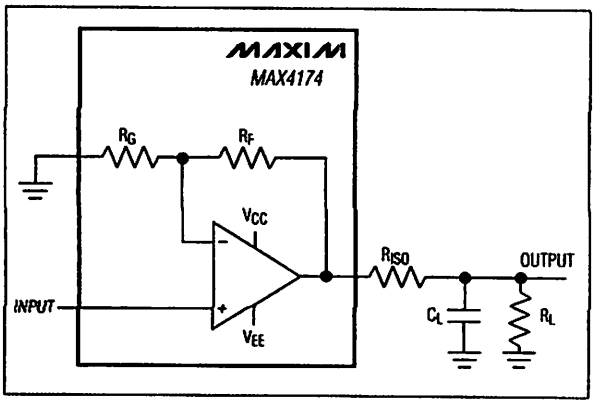


Figure 9. Dual-Supply, Capacitive-Load Driving Circuit

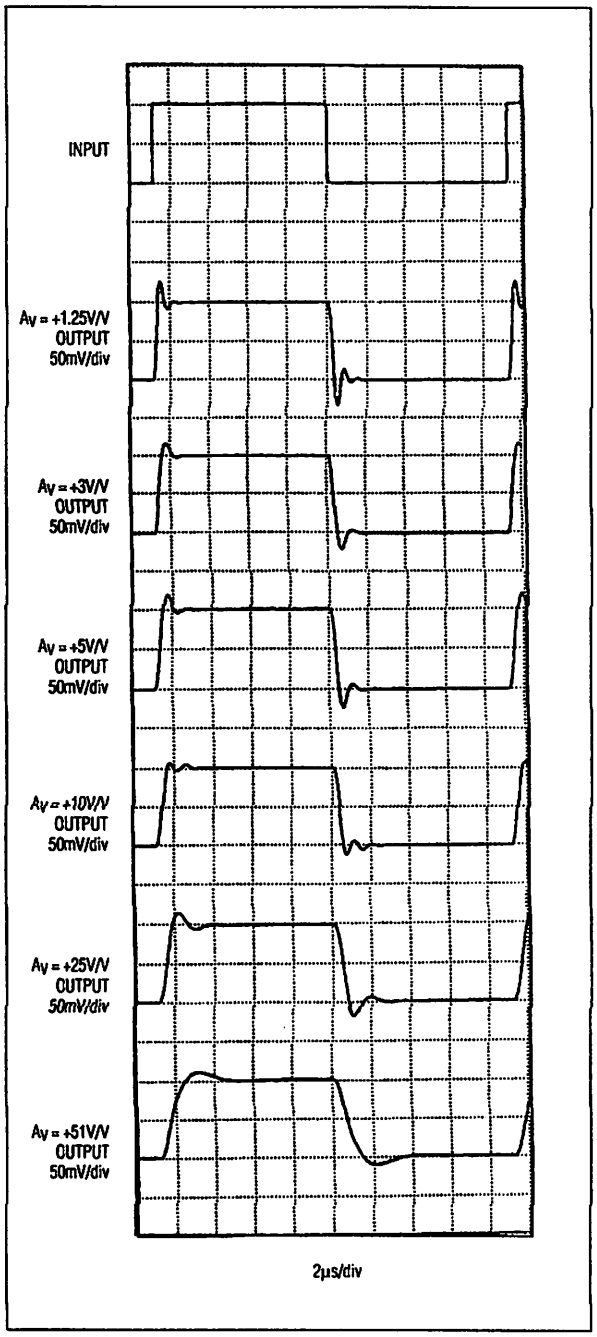


Figure 11. MAX4174/MAX4175 Small-Signal Pulse Response (C_L = 250pF, R_L = 100kΩ)

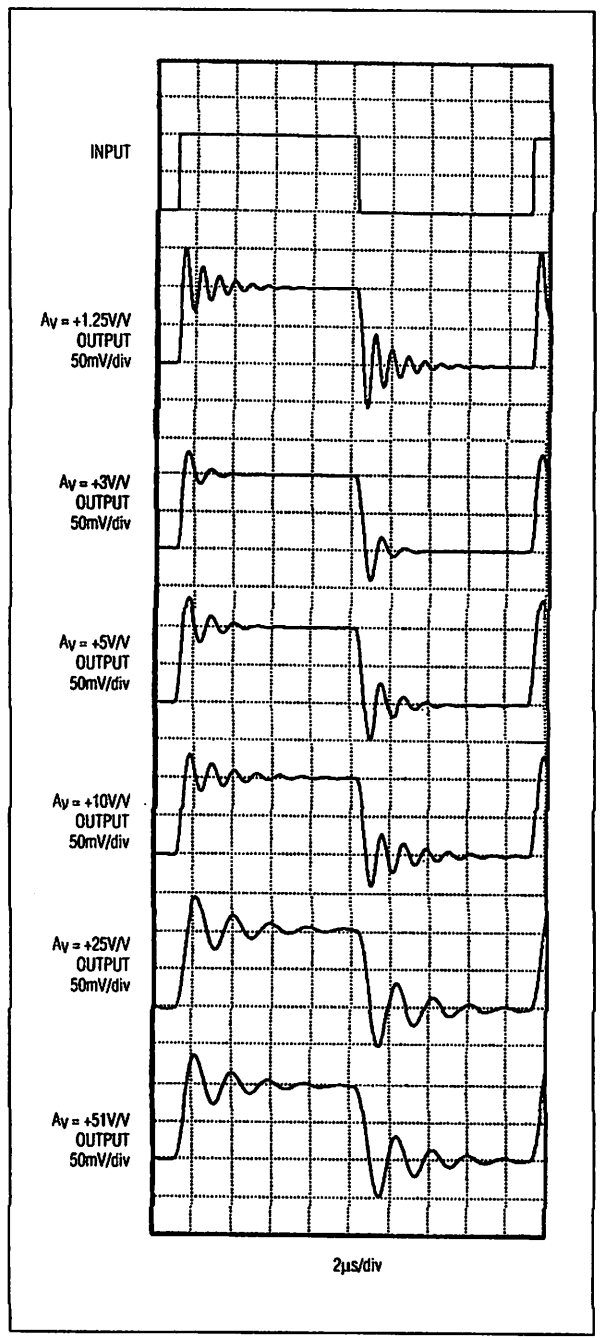


Figure 12. MAX4174/MAX4175 Small-Signal Pulse Response (C_L = 470pF, R_L = 100kΩ)

Gain Selection Guide

GAIN CODE	R_F/R_G INVERTING GAIN	1+ (R_F/R_G) NONINVERTING GAIN	-3dB BW (kHz)†	TOP MARK	
				MAX4174	MAX4175
AB*	0.25	1.25	1700	ACDS	ACET
AC	0.5	1.5	1280	ACDT	ACEU
AD*	1	2	590	ACDU	ACEV
AE	1.25	2.25	450	ACDV	ACEW
AF	1.5	2.5	1180	ACDW	ACEX
AG*	2	3	970	ACDX	ACEY
AH	2.5	3.5	820	ACDY	ACEZ
AJ	3	4	690	ACDZ	ACFA
AK*	4	5	970	ACEA	ACFB
AL	5	6	790	ACEB	ACFC
AM	6	7	640	ACEC	ACFD
AN	8	9	480	ACED	ACFE
AO*	9	10	640	ACEE	ACFF
BA*	10	11	560	ACEF	ACFG
BB	12.5	13.5	460	ACEG	ACFH
BC	15	16	390	ACEH	ACFI
BD	20	21	300	ACEI	ACFJ
BE*	24	25	590	ACEJ	ACFK
BF	25	26	580	ACEK	ACFL
BG	30	31	510	ACEL	ACFM
BH	40	41	390	ACEM	ACFN
BJ*	49	50	310	ACEN	ACFO
BK*	50	51	330	ACEO	ACFP
BL	60	61	310	ACEP	ACFQ
BM	80	81	260	ACEQ	ACFR
BN*	99	100	230	ACER	ACFS
CA*	100	101	230	ACES	ACFT

Note: *Gains in the noninverting configuration are 1+ (R_F/R_G) and range from +1.25V/V to +101V/V. For a +1V/V gain, use the MAX4281/MAX4282/MAX4284.*

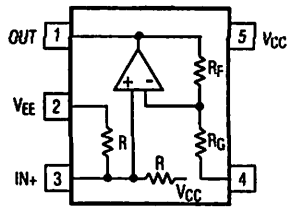
* *Preferred Gains. These gain versions are available as samples and in small quantities.*

† *The -3dB bandwidth is the same for inverting and noninverting configurations.*

Pin Configurations (continued)

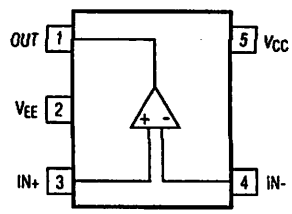
TOP VIEW

MAXIM MAX4175



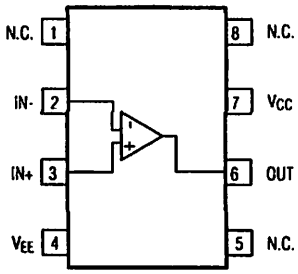
SOT23-5

MAXIM MAX4281



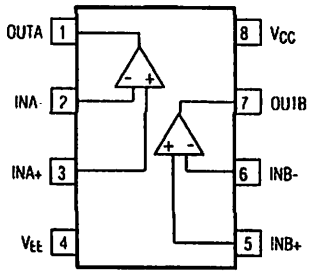
SOT23-5

MAXIM MAX4281



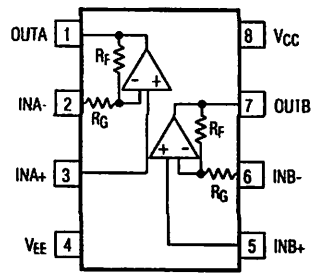
SO

MAXIM MAX4282



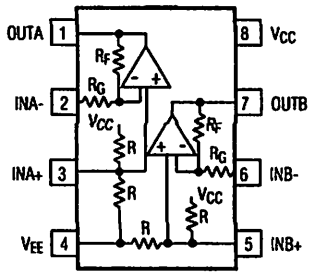
µMAX/SO

MAXIM MAX4274



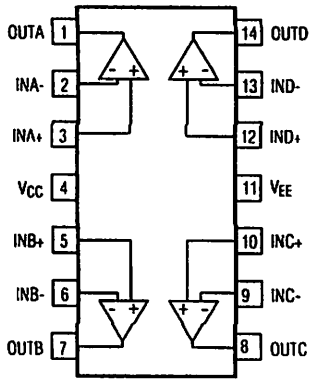
µMAX/SO

MAXIM MAX4275



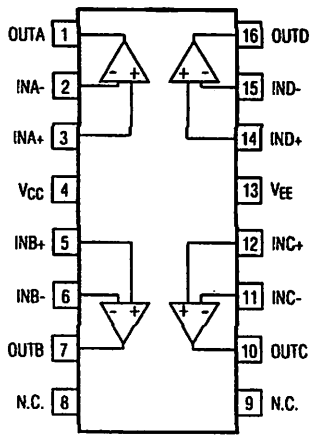
µMAX/SO

MAXIM MAX4284



SO/TSSOP

MAXIM MAX4284



QSOP

SOT23, Rail-to-Rail, Fixed-Gain GainAmps/Open-Loop Op Amps

Ordering Information (continued)

PART*	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX4274_EUA	-40°C to +85°C	8 µMAX	—
MAX4274_ESA	-40°C to +85°C	8 SO	—
MAX4275_EUA	-40°C to +85°C	8 µMAX	—
MAX4275_ESA	-40°C to +85°C	8 SO	—
MAX4281EUK-T	-40°C to +85°C	5 SOT23-5	ACDR
MAX4281ESA	-40°C to +85°C	8 SO	—
MAX4282EUA	-40°C to +85°C	8 µMAX	—
MAX4282ESA	-40°C to +85°C	8 SO	—
MAX4284EUD	-40°C to +85°C	14 TSSOP	—
MAX4284ESD	-40°C to +85°C	14 SO	—
MAX4284EEE	-40°C to +85°C	16 QSOP	—

Note: *Refer to Gain Selection Guide for SOT top marks.*

**Insert the desired gain code (from the Gain Selection Guide) in the blank to complete the part number. Refer to Gain Selection Guide for a list of preferred gains.*

Chip Information

TRANSISTOR COUNTS:

MAX4174: 178
MAX4175: 178
MAX4274: 332
MAX4275: 332
MAX4281: 178
MAX4282: 332
MAX4284: 328

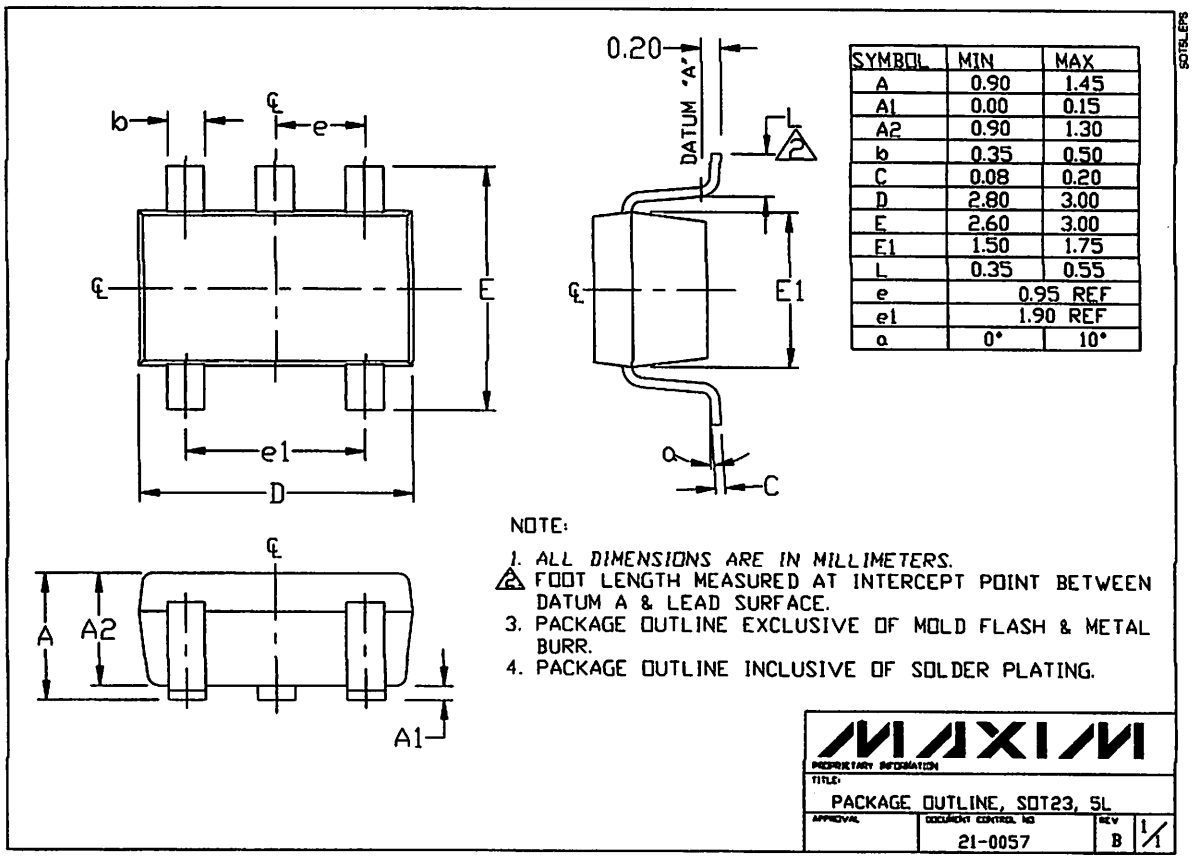
SUBSTRATE CONNECTED TO V_{EE}

Selector Guide

PART*	INVERTING GAINS AVAILABLE (V/V) (INVERTING, R_F/R_G)	NONINVERTING GAIN (V/V)	INTERNAL RESISTORS	INTERNAL $V_{CC}/2$ BIAS	NO. OF AMPS PER PACKAGE	PIN-PACKAGE
MAX4174_	-0.25 to -100	+1.25 to +101	Yes	No	1	5-pin SOT23
MAX4175_	-0.25 to -100	+1.25 to +101	Yes	Yes	1	5-pin SOT23
MAX4274_	-0.25 to -100	+1.25 to +101	Yes	No	2	8-pin µMAX/SO
MAX4275_	-0.25 to -100	+1.25 to +101	Yes	Yes	2	8-pin µMAX/SO
MAX4281_	Open Loop, Unity-Gain Stable		No	No	1	5-pin SOT23, 8-pin SO
MAX4282_	Open Loop, Unity-Gain Stable		No	No	2	8-pin µMAX/SO
MAX4284_	Open Loop, Unity-Gain Stable		No	No	4	14-pin SO/TSSOP, 16-pin QSOP

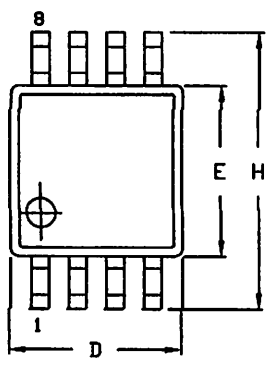
** Insert the desired gain code (from the Gain Selection Guide) in the blank to complete the part number.*

Package Information

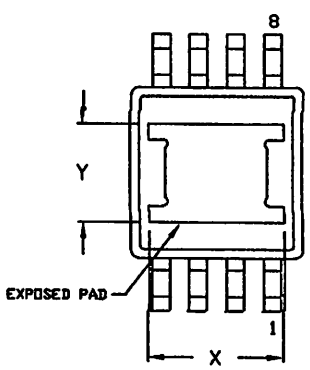


SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
e1	1.90 REF	
α	0°	10°

Package Information



TOP VIEW

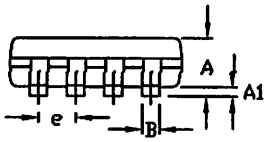


BOTTOM VIEW

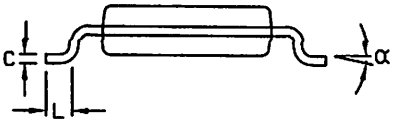
	INCHES		MILLIMETERS		JEDEC INCHES		JEDEC MILLIMETERS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10	---	0.043	---	1.10
A1	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15
B	0.010	0.014	0.25	0.36	0.010	0.016	0.25	0.40
C	0.005	0.007	0.13	0.18	0.005	0.009	0.13	0.23
D	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
e	0.0256 BSC		0.65 BSC		0.0256 BSC		0.64 BSC	
E	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
H	0.188	0.198	4.78	5.03	0.193 BSC		4.9 BSC	
L	0.016	0.026	0.41	0.66	0.016	0.027	0.40	0.70
α	0°	6°	0°	6°	0°	6°	0°	6°
*X	0.087	0.099	2.210	2.515				
*Y	0.062	0.074	1.575	1.880				

* EXPOSED PAD

8LUMAXD.EPS



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187.
5. DIMENSIONS X & Y APPLY TO EXPOSED PAD VERSIONS ONLY.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 8L uMAX

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0036	G	1/1

19-0196; Rev 0; 10/93

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

MAXIM

+5V, Low-Power, 12-Bit Serial ADCs

General Description

The MAX187/MAX189 serial 12-bit analog-to-digital converters (ADCs) operate from a single +5V supply and accept a 0V to 5V analog input. Both parts feature an 8.5µs successive-approximation ADC, a fast track/hold (1.5µs), an on-chip clock, and a high-speed 3-wire serial interface.

The MAX187/MAX189 digitize signals at a 75ksps throughput rate. An external clock accesses data from the interface, which communicates without external hardware to most digital signal processors and microcontrollers. The interface is compatible with SPI™, QSPI™, and Microwire™.

The MAX187 has an on-chip buffered reference, and the MAX189 requires an external reference. Both the MAX187 and MAX189 save space with 8-pin DIP and 16-pin SO packages. Power consumption is 7.5mW and reduces to only 10µW in shutdown.

Excellent AC characteristics and very low power consumption combined with ease of use and small package size make these converters ideal for remote DSP and sensor applications, or for circuits where power consumption and space are crucial.

Applications

Portable Data Logging

Remote Digital Signal Processing

Isolated Data Acquisition

High-Accuracy Process Control

Features

- **12-Bit Resolution**
- **±½ LSB Integral Nonlinearity (MAX187A/MAX189A)**
- **Internal Track/Hold, 75kHz Sampling Rate**
- **Single +5V Operation**
- **Low Power: 2µA Shutdown Current**
  1.5mA Operating Current
- **Internal 4.096V Buffered Reference (MAX187)**
- **3-Wire Serial Interface, Compatible with SPI, QSPI, and Microwire**
- **Small-Footprint 8-Pin DIP and 16-Pin SO**

Ordering Information

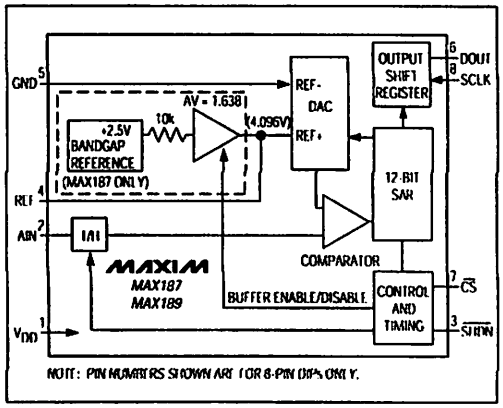
PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX187ACPA	0°C to +70°C	8 Plastic DIP	±½
MAX187BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX187CCPA	0°C to +70°C	8 Plastic DIP	±2
MAX187ACWE	0°C to +70°C	16 Wide SO	±½
MAX187BCWE	0°C to +70°C	16 Wide SO	±1
MAX187CCWE	0°C to +70°C	16 Wide SO	±2
MAX187BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued on last page.

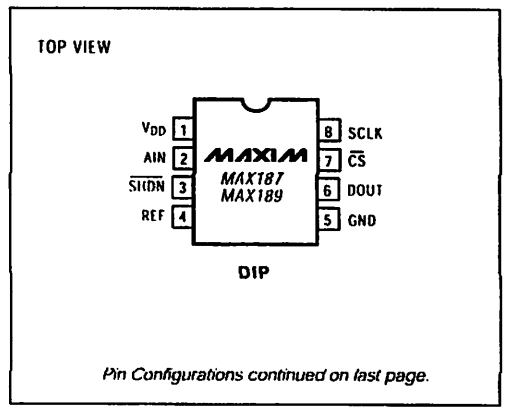
* *Dice are specified at T_A = +25°C, DC parameters only.*

** *Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configurations



Pin Configurations continued on last page.

+5V, Low-Power, 12-Bit Serial ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
AIN to GND .....-0.3V to (V_{DD} + 0.3V)
REF to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Outputs to GND .....-0.3V to (V_{DD} + 0.3V)
SHDN to GND .....-0.3V to (V_{DD} + 0.3V)
REF Load Current (MAX187) .....4.0mA Continuous
REF Short-Circuit Duration (MAX187) 20sec
DOUT Current .....+20mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ..500mW
16-Pin Wide SO (derate 8.70mW/°C above +70°C) ...478mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 440mW
Operating Temperature Ranges:
MAX187_C_ _/MAX189_C_ _ .....0°C to +70°C
MAX187_E_ _/MAX189_E_ _ .....-40°C to +85°C
MAX187_MJA/MAX189_MJA .....-55°C to +125°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%; GND = 0V; unipolar input mode; 75ksps, f_{CLK} = 4.0MHz, external clock (50% duty cycle); MAX187—internal reference: V_{REF} = 4.096V, 4.7µF capacitor at REF pin, or MAX189—external reference: V_{REF} = 4.096V applied to REF pin, 4.7µF capacitor at REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution					12	Bits
Relative Accuracy (Note 2)		MAX18_A			±½	LSB
		MAX18_B			±1	
		MAX18_C			±2	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX18_A			±1½	LSB
		MAX18_B/C			±3	
Gain Error (Note 3)		MAX187			±3	LSB
		MAX189A			±1	
		MAX189B/C			±3	
Gain Temperature Coefficient		External reference, 4.096V		±0.8		ppm/°C
DYNAMIC SPECIFICATIONS (10kHz sine wave input, 0V to 4.096V_{p-p}, 75ksps)						
Signal-to-Noise plus Distortion Ratio	SINAD		70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD				-80	dB
Spurious-Free Dynamic Range	SFDR		80			dB
Small-Signal Bandwidth		Rolloff -3dB		4.5		MHz
Full-Power Bandwidth				0.8		MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%; GND = 0V; unipolar input mode; 75ksps, f_{CLK} = 4.0MHz, external clock (50% duty cycle); MAX187—internal reference: V_{REF} = 4.096V, 4.7µF capacitor at REF pin, or MAX189—external reference: V_{REF} = 4.096V applied to REF pin, 4.7µF capacitor at REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CONVERSION RATE							
Conversion Time	t_{CONV}			5.5		8.5	µs
Track/Hold Acquisition Time	t_{ACQ}			1.5			µs
Throughput Rate		External clock, 4MHz, 13 clocks				75	ksps
Aperture Delay	t_{APR}				10		ns
Aperture Jitter					<50		ps
ANALOG INPUT							
Input Voltage Range						0 to V_{REF}	V
Input Capacitance (Note 4)					16		pF
INTERNAL REFERENCE (MAX187 only, reference buffer enabled)							
REF Output Voltage	V_{REF}	T_A = +25°C		4.076	4.096	4.116	V
		T_A = T_{MIN} to T_{MAX}	MAX187_C	4.060		4.132	
			MAX187_E	4.050		4.140	
			MAX187_M	4.040		4.150	
REF Short-Circuit Current						30	mA
REF Tempco		MAX187AC/BC			±30	±50	ppm/°C
		MAX187AE/BE			±30	±60	
		MAX187AM/BM			±30	±80	
		MAX187C			±30		
Load Regulation (Note 5)		0mA to 0.6mA output load			1		mV
EXTERNAL REFERENCE AT REF (Buffer disabled, V_{REF} = 4.096V)							
Input Voltage Range				2.50		V_{DD} + 50mV	V
Input Current					200	350	µA
Input Resistance				12	20		kΩ
Shutdown REF Input Current					1.5	10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%; GND = 0V; unipolar input mode; 75ksps, f_{CLK} = 4.0MHz, external clock (50% duty cycle); MAX187—internal reference: V_{REF} = 4.096V, 4.7µF capacitor at REF pin, or MAX189—external reference: V_{REF} = 4.096V applied to REF pin, 4.7µF capacitor at REF pin: T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, CS, SHDN)							
SCLK, CS Input High Voltage	V_{INH}			2.4			V
SCLK, CS Input Low Voltage	V_{INL}					0.8	V
SCLK, CS Input Hysteresis	V_{HYST}				0.15		V
SCLK, CS Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}				±1	µA
SCLK, CS Input Capacitance	C_{IN}	(Note 4)				15	pF
SHDN Input High Voltage	V_{INSH}			V_{DD} - 0.5			V
SHDN Input Low Voltage	V_{INSL}					0.5	V
SHDN Input Current	I_{INS}	SHDN = V_{DD} or 0V				±4.0	µA
SHDN Input Mid Voltage	V_{IM}			1.5		V_{DD} -1.5	V
SHDN Voltage, Floating	V_{FLT}	SHDN = open			2.75		V
SHDN Maximum Allowed Leakage, Mid Input		SHDN = open		-100		100	nA
DIGITAL OUTPUT (DOUT)							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
		I_{SINK} = 16mA			0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA		4			V
Three-State Leakage Current	I_L	CS = 5V				±10	µA
Three-State Output Capacitance	C_{OUT}	CS = 5V (Note 4)				15	pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.75		5.25	V
Supply Current	I_{DD}	Operating mode	MAX187		1.5	2.5	mA
			MAX189		1.0	2.0	
		Power-down mode			2	10	µA
Power-Supply Rejection	PSR	V_{DD} = +5V, +5%; external reference, 4.096V; full-scale input (Note 6)			±0.06	±0.5	mV

TIMING CHARACTERISTICS

(V_{DD} = +5.0V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Track/Hold Acquisition Time	t_{ACQ}	CS = high (Note 7)		1.5			µs
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD} = 100pF	MAX18_ _C/E	20		150	ns
			MAX18_ _M	20		200	
CS Fall to Output Enable	t_{DV}	C_{LOAD} = 100pF				100	ns
CS Rise to Output Disable	t_{TR}	C_{LOAD} = 100pF				100	ns
SCLK Clock Frequency	f_{SCLK}					5	MHz
SCLK Pulse Width High	t_{CH}			100			ns
SCLK Pulse Width Low	t_{CL}			100			ns
SCLK Low to CS Fall Setup Time	t_{CSO}			50			ns
CS Pulse Width	t_{CS}			500			ns

Note 1: Tested at V_{DD} = +5V.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.

Note 3: MAX187—internal reference, offset nulled; MAX189–external +4.096V reference, offset nulled. Excludes reference errors.

Note 4: Guaranteed by design. Not subject to production testing.

Note 5: External load should not change during conversion for specified ADC accuracy.

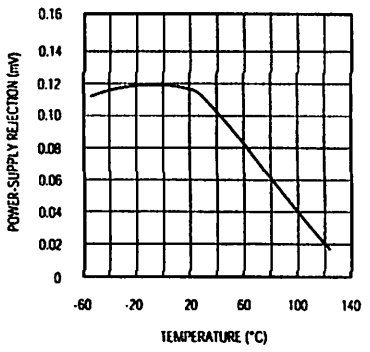
Note 6: DC test, measured at 4.75V and 5.25V only.

Note 7: *To guarantee acquisition time, t_{ACQ} is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired.*

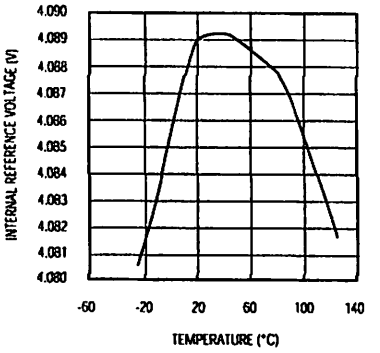
+5V, Low-Power, 12-Bit Serial ADCs

Typical Operating Characteristics

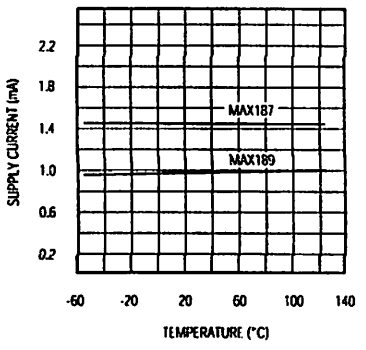
POWER-SUPPLY REJECTION vs. TEMPERATURE



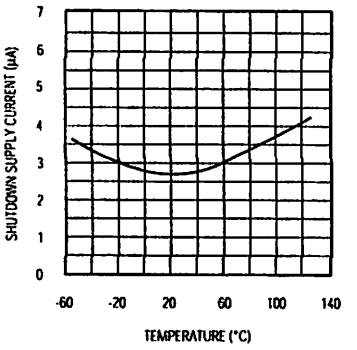
V_{REF} vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
DIP	WIDE SO		
1	1	V_{DD}	Supply voltage, +5V ±5%
2	3	AIN	Sampling analog input, 0V to V_{REF} range
3	6	SHDN	Three-level shutdown input. Pulling SHDN low shuts the MAX187/MAX189 down to 10µA (max) supply current. Both MAX187 and MAX189 are fully operational with either SHDN high or floating. For the MAX187, pulling SHDN high enables the internal reference, and letting SHDN float disables the internal reference and allows for the use of an external reference.
4	8	REF	Reference voltage—sets analog voltage range and functions as a 4.096V output for the MAX187 with enabled internal reference. REF also serves as a +2.5V to V_{DD} input for a precision reference for both MAX187 (disabled internal reference) and MAX189. Bypass with 4.7µF if internal reference is used, and with 0.1µF if an external reference is applied.
5	—	GND	Analog and digital ground
—	10	AGND	Analog ground
—	11	DGND	Digital ground
6	12	DOUT	Serial data output. Data changes state at SCLK's falling edge.
7	15	CS	Active-low chip select initiates conversions on the falling edge. When CS is high, DOUT is high impedance.
8	16	SCLK	Serial clock input. Clocks data out with rates up to 5MHz.
—	2,4,5,7,9,13,14	N.C.	Not internally connected. Connect to AGND for best noise performance.

Detailed Description

Converter Operation

The MAX187/MAX189 use input track/hold (T/H) and successive approximation register (SAR) circuitry to convert an analog input signal to a digital 12-bit output. No external hold capacitor is needed for the T/H. Figures 3a and 3b show the MAX187/MAX189 in their simplest configuration. The MAX187/MAX189 convert input signals in the 0V to V_{IN+} range in 10µs, including T/H acquisition time. The MAX187's internal reference is trimmed to 4.096V, while the MAX189 requires an external reference. Both devices accept external reference voltages from +2.5V to V_{DD}. The serial interface requires only three digital lines, SCLK, $\overline{CS}$, and DOUT, and provides easy interface to microprocessors (µPs).

Both converters have two modes: normal and shutdown. Pulling SHDN low shuts the device down and reduces supply current to below 10µA, while pulling SHDN high or leaving it floating puts the device into the operational mode. A conversion is initiated by $\overline{CS}$ falling. The conversion result is available at DOUT in unipolar serial format. A high bit, signaling the end of conversion (EOC), followed by the data bits (MSB first), make up the serial data stream.

The MAX187 operates in one of two states: (1) internal reference and (2) external reference. Select internal reference operation by forcing SHDN high, and external reference operation by floating SHDN.

Analog Input

Figure 4 illustrates the sampling architecture of the ADC's analog comparator. The full-scale input voltage depends on the voltage at REF.

REFERENCE	ZERO SCALE	FULL SCALE
Internal Reference (MAX187 only)	0V	+4.096V
External Reference	0V	V_{REF}

For specified accuracy, the external reference voltage range spans from +2.5V to V_{DD}.

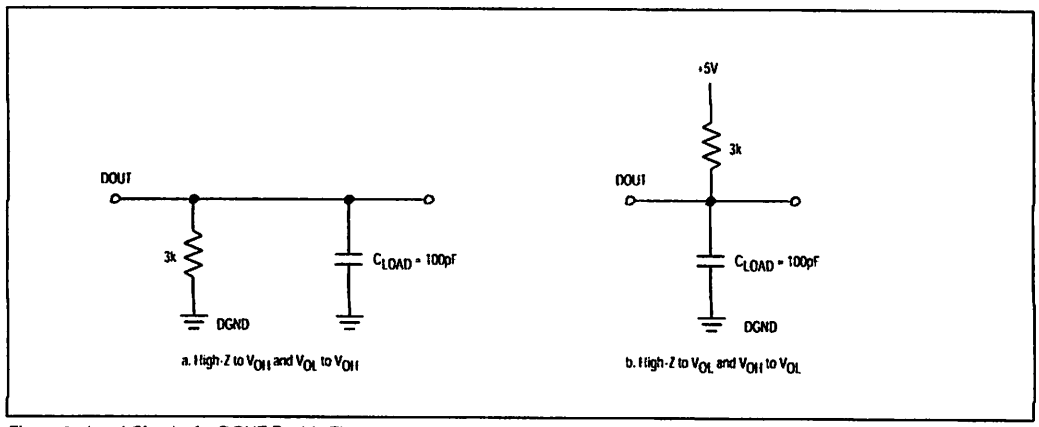


Figure 1. Load Circuits for DOUT Enable Time

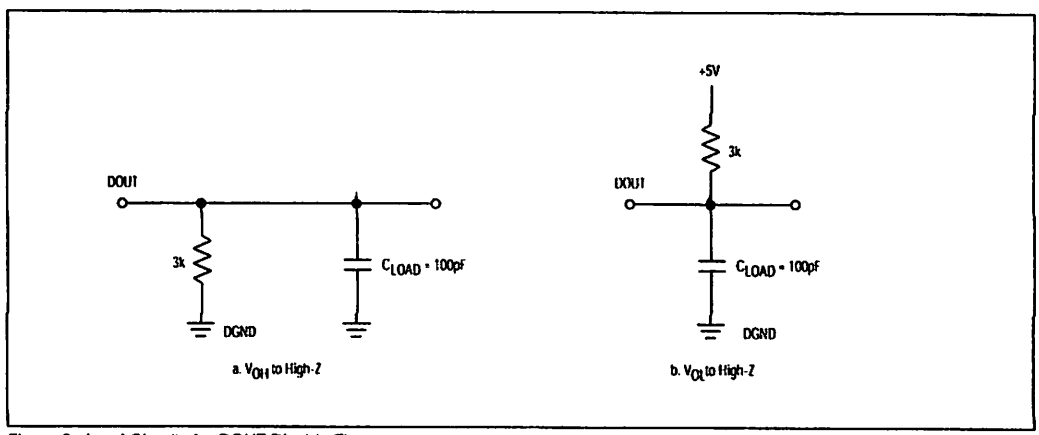


Figure 2. Load Circuits for DOUT Disable Time

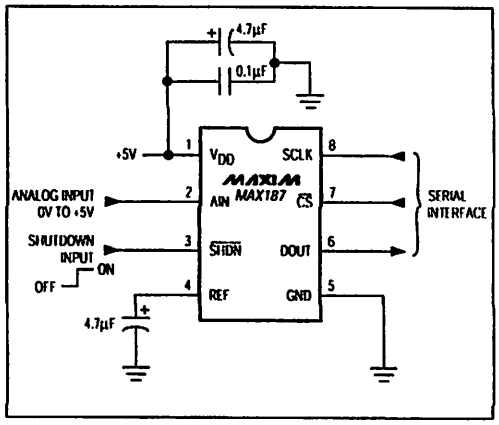


Figure 3a. MAX187 Operational Diagram

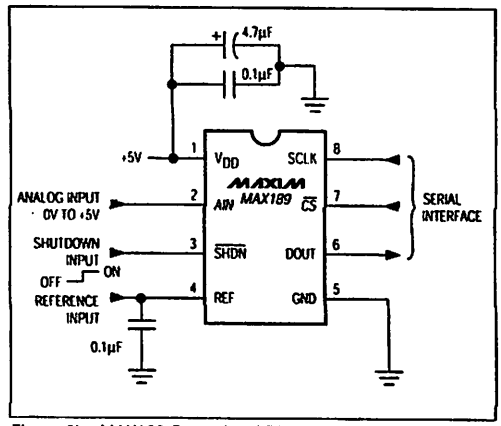


Figure 3b. MAX189 Operational Diagram

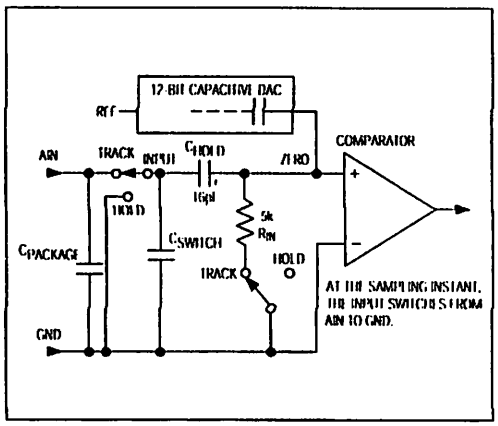


Figure 4. Equivalent Input Circuit

Track/Hold

In track mode, the analog signal is acquired and stored in the internal hold capacitor. In hold mode, the T/H switch opens and maintains a constant input to the ADC's SAR section.

During acquisition, the analog input AIN charges capacitor C_{HOLD}. Bringing CS low ends the acquisition interval. At this instant, the T/H switches the input side of C_{HOLD} to GND. The retained charge on C_{HOLD} represents a sample of the input, unbalancing the node ZERO at the comparator's input.

In hold mode, the capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of a 12-bit resolution. This action is equivalent to transferring a charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal. At the conversion's end, the input side of C_{HOLD} switches back to AIN, and C_{HOLD} charges to the input signal again.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{ACQ} = 9 (R_S + R_{IN}) 16pF,$$

where R_{IN} = 5kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Source impedances below 5kΩ do not significantly affect the AC performance of the ADC.

+5V, Low-Power, 12-Bit Serial ADCs

Input Bandwidth

The ADCs' input tracking circuitry has a 4.5MHz small-signal bandwidth, and an 8V/µs slew rate. It is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted high-frequency signals into the frequency band of interest, an anti-alias filter is recommended. See the MAX274/MAX275 continuous-time filters data sheet.

Input Protection

Internal protection diodes that clamp the analog input allow the input to swing from GND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the input must not exceed V_{DD} by more than 50mV, or be lower than GND by 50mV.

If the analog input exceeds the supplies by more than 50mV beyond the supplies, limit the input current to 2mA, since larger currents degrade conversion accuracy.

Driving the Analog Input

The input lines to AIN and GND should be kept as short as possible to minimize noise pickup. Shield longer leads. Also see the *Input Protection* section.

Because the MAX187/MAX189 incorporate a T/H, the drive requirements of the op amp driving AIN are less stringent than those for a successive-approximation ADC without a T/H. The typical input capacitance is 16pF. The amplifier bandwidth should be sufficient to handle the frequency of the input signal. The MAX400 and OP07 work well at lower frequencies. For higher-frequency operation, the MAX427 and OP27 are practical choices. The allowed input frequency range is limited by the 75ksps sample rate of the MAX187/MAX189. Therefore, the maximum sinusoidal input frequency allowed is 37.5kHz. Higher-frequency signals cause aliasing problems unless undersampling techniques are used.

Reference

The MAX187 can be used with an internal or external reference, while the MAX189 requires an external reference.

Internal Reference

The MAX187 has an on-chip reference with a buffered temperature-compensated bandgap diode, laser-trimmed to +4.096V ±0.5%. Its output is connected to REF and also drives the internal DAC. The output can be used as a reference voltage source for other components and can source up to 0.6mA. Decouple REF with a 4.7µF capacitor. The internal reference is enabled by pulling the $\overline{SHDN}$ pin high. Letting $\overline{SHDN}$ float disables the internal reference, which allows the use of an external reference, as described in the *External Reference* section.

External Reference

The MAX189 operates with an external reference at the REF pin. To use the MAX187 with an external reference, disable the internal reference by letting $\overline{SHDN}$ float. Stay within the voltage range +2.5V to V_{DD} to achieve specified accuracy. The minimum input impedance is 12kΩ for DC currents. During conversion, the external reference must be able to deliver up to 350µA DC load current and have an output impedance of 10Ω or less. The recommended minimum value for the bypass capacitor is 0.1µF. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor.

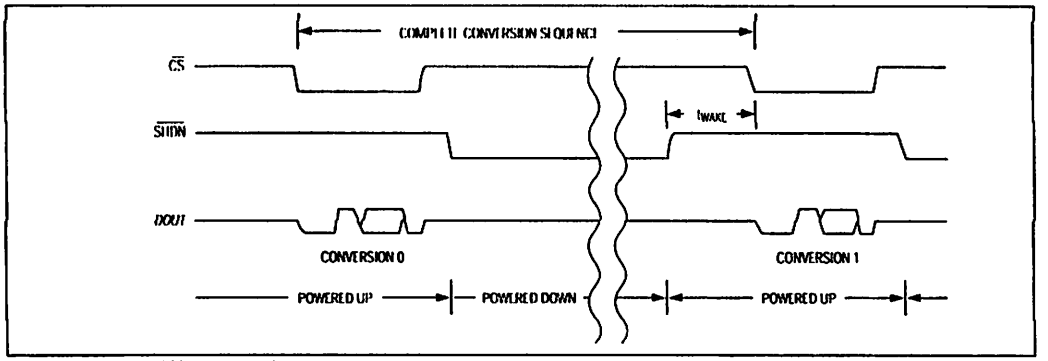


Figure 5. MAX187/MAX189 Shutdown Sequence

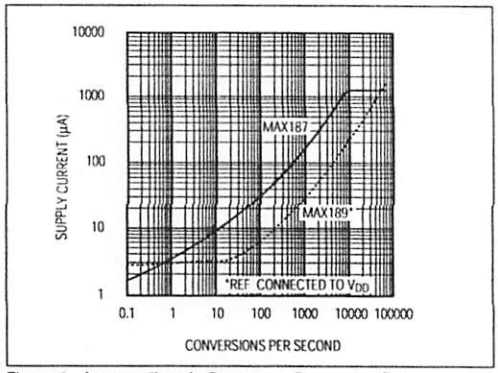


Figure 6. Average Supply Current vs. Conversion Rate

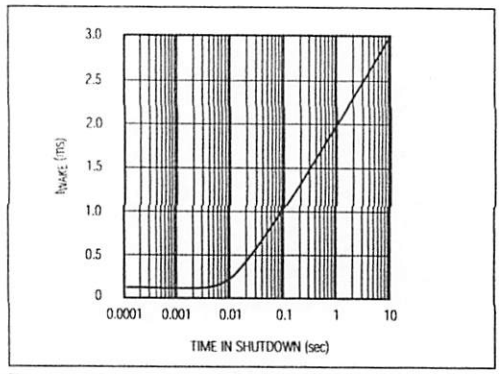


Figure 7. t_{WAKE} vs. Time in Shutdown (MAX187 only)

Serial Interface

Initialization After Power-Up and Starting a Conversion

When power is first applied, it takes the fully discharged 4.7µF reference bypass capacitor up to 20ms to provide adequate charge for specified accuracy. With $\overline{SHDN}$ not pulled low, the MAX187/MAX189 are now ready to convert.

To start a conversion, pull $\overline{CS}$ low. At $\overline{CS}$'s falling edge, the T/H enters its hold mode and a conversion is initiated. After an internally timed 8.5µs conversion period, the end of conversion is signaled by DOUT pulling high. Data can then be shifted out serially with the external clock.

Using *SHDN* to Reduce Supply Current

Power consumption can be reduced significantly by shutting down the MAX187/MAX189 between conversions. This is shown in Figure 6, a plot of average supply current vs. conversion rate. Because the MAX189 uses an external reference voltage (assumed to be present continuously), it "wakes up" from shutdown more quickly, and therefore provides lower average supply currents. The wakeup-time, t_{WAKE}, is the time from $\overline{SHDN}$ deasserted to the time when a conversion may be initiated. For the MAX187, this time is 2µs. For the MAX189, this time depends on the time in shutdown (see Figure 7) because the external 4.7µF reference bypass capacitor loses charge slowly during shutdown (see the specifications for shutdown, REF Input Current = 10µA max).

External Clock

The actual conversion does not require the external clock. This frees the µP from the burden of running the SAR conversion clock, and allows the conversion result to be read back at the µP's convenience at any clock rate from 0MHz to 5MHz. The clock duty cycle is unrestricted if each clock phase is at least 100ns. Do not run the clock while a conversion is in progress.

Timing and Control

Conversion-start and data-read operations are controlled by the $\overline{CS}$ and SCLK digital inputs. The timing diagrams of Figures 8 and 9 outline the operation of the serial interface.

A $\overline{CS}$ falling edge initiates a conversion sequence: The T/H stage holds input voltage, the ADC begins to convert, and DOUT changes from high impedance to logic low. SCLK must be kept inactive during the conversion. An internal register stores the data when the conversion is in progress.

End of conversion (EOC) is signaled by DOUT going high. DOUT's rising edge can be used as a framing signal. SCLK shifts the data out of this register any time after the conversion is complete. DOUT transitions on SCLK's falling edge. The next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits. Since there are 12 data bits and one leading high bit, at least 13 falling clock edges are needed to shift out these bits. Extra clock pulses occurring after the conversion result has been clocked out, and prior to a rising edge of $\overline{CS}$, produce trailing 0s at DOUT and have no effect on converter operation.

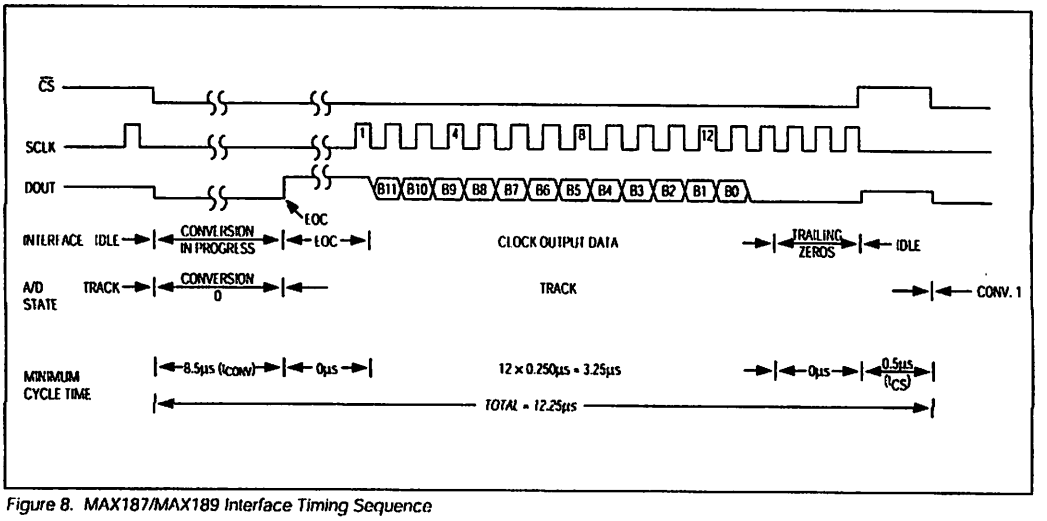


Figure 8. MAX187/MAX189 Interface Timing Sequence

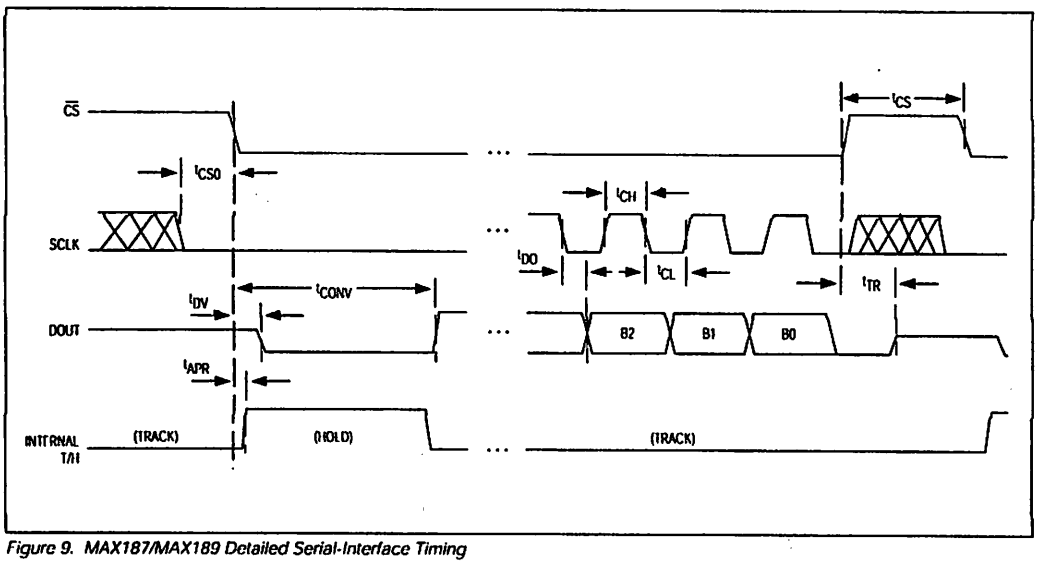


Figure 9. MAX187/MAX189 Detailed Serial-Interface Timing

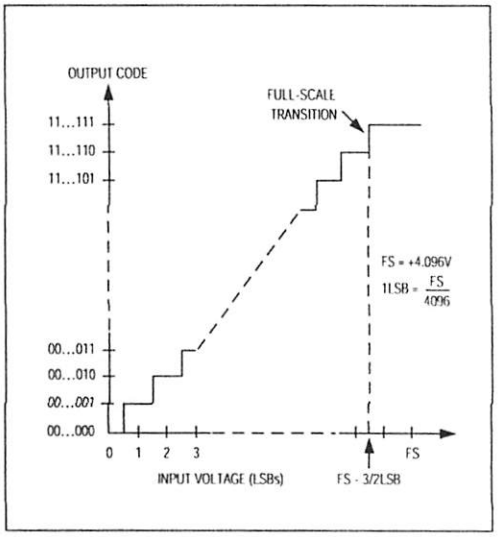


Figure 10. MAX187/MAX189 Unipolar Transfer Function, 4.096V = Full Scale

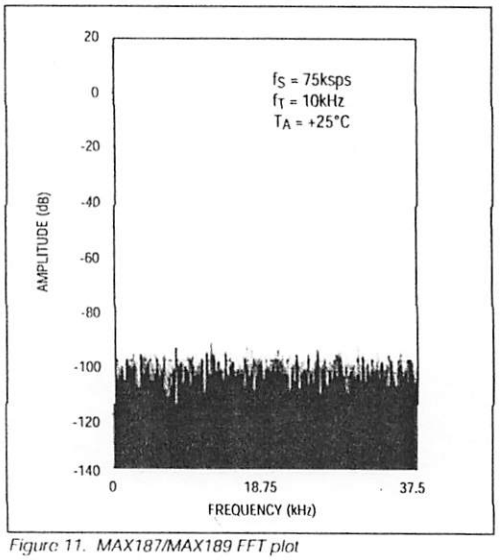


Figure 11. MAX187/MAX189 FFT plot

Minimum cycle time is accomplished by using DOUT's rising edge as the EOC signal. Clock out the data with 13 clock cycles at full speed. Raise CS after the conversion's LSB has been read. After the specified minimum time, t_{ACQ}, CS can be pulled low again to initiate the next conversion.

Output Coding and Transfer Function

The data output from the MAX187/MAX189 is binary, and Figure 10 depicts the nominal transfer function. Code transitions occur halfway between successive integer LSB values. If V_{REF} = +4.096V, then 1 LSB = 1.00mV or 4.096V/4096.

Dynamic Performance

High-speed sampling capability and a 75ksps throughput make the MAX187/MAX189 ideal for wideband signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm that determines its spectral content. Conversion errors are then seen as spectral elements outside of the fundamental *input frequency. ADCs have traditionally been evaluat*ed by specifications such as Zero and Full-Scale Error, Integral Nonlinearity (INL), and Differential Nonlinearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal-processing applications, where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so *different tests are required.*

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS amplitude of all other ADC output signals. The input bandwidth is limited to frequencies above DC and below one-half the ADC sample (conversion) rate.

*The theoretical minimum ADC noise is caused by quan*tization error and is a direct result of the ADC's resolution: SINAD = (6.02N + 1.76)dB, where N is the number of bits of resolution. An ideal 12-bit ADC can, therefore, do no better than 74dB. An FFT plot of the output shows the output level in various spectral bands. Figure 11 shows the result of sampling a pure 10kHz sine wave at a 75ksps rate with the MAX187/MAX189.

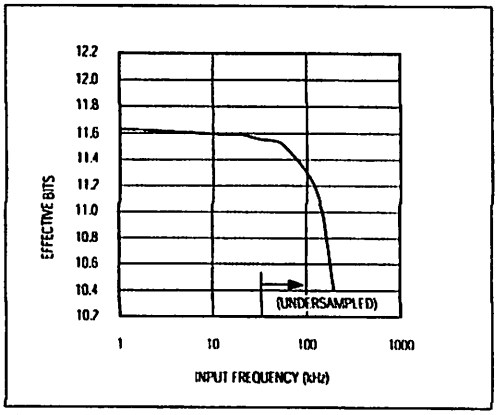


Figure 12. Effective Bits vs. Input Frequency

The effective resolution (effective number of bits) the ADC provides can be determined by transposing the above equation and substituting in the measured SINAD: N = (SINAD - 1.76)/6.02. Figure 12 shows the effective number of bits as a function of the input frequency for the MAX187/MAX189.

Total Harmonic Distortion

If a pure sine wave is sampled by an ADC at greater than the Nyquist frequency, the nonlinearities in the ADC's transfer function create harmonics of the input frequency present in the sampled output data.

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all the harmonics (in the frequency band above DC and below one-half the sample rate, but not including the DC component) to the RMS amplitude of the fundamental frequency. This is expressed as follows:

$$THD = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots V_N^2}}{V_1}$$

where V_1 is the fundamental RMS amplitude, and V_2 through V_N are the amplitudes of the 2nd through Nth harmonics. The THD specification in the *Electrical Characteristics* includes the 2nd through 5th harmonics.

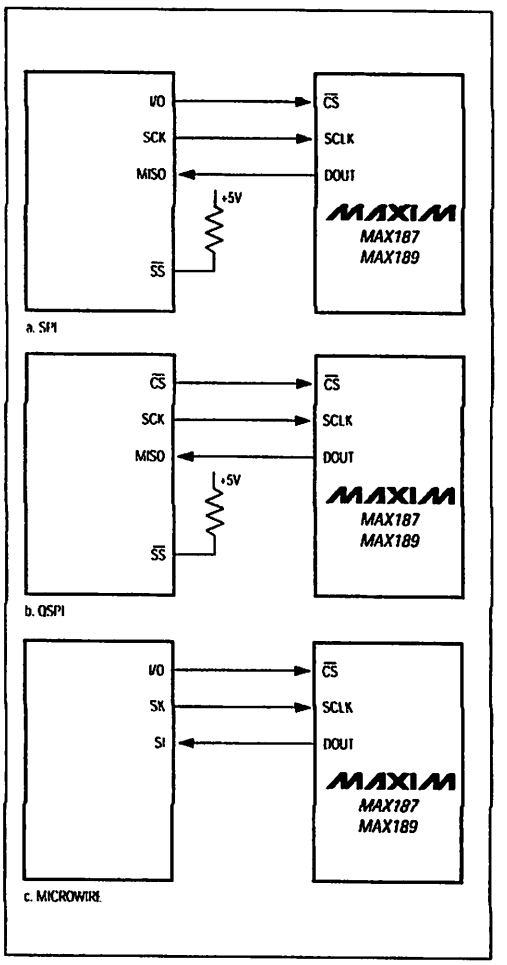


Figure 13. Common Serial-Interface Connections to the MAX187/MAX189

Applications Information

Connection to Standard Interfaces

The MAX187/MAX189 serial interface is fully compatible with SPI, QSPI, and Microwire standard serial interfaces.

If a serial interface is available, set the CPU's serial interface in master mode so the CPU generates the serial clock. Choose a clock frequency up to 2.5MHz.

1. Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low. Keep SCLK low.
2. Wait the for the maximum conversion time specified before activating SCLK. Alternatively, look for a DOUT rising edge to determine the end of conversion.
3. Activate SCLK for a minimum of 13 clock cycles. The first falling clock edge will produce the MSB of the DOUT conversion. DOUT output data transitions on SCLK's falling edge and is available in MSB-first format. Observe the SCLK to DOUT valid timing characteristic. Data can be clocked into the µP on SCLK's rising edge.
4. Pull CS high at or after the 13th falling clock edge. If $\overline{CS}$ remains low, trailing zeros are clocked out after the LSB.
5. With $\overline{CS}$ = high, wait the minimum specified time, t_{CS}, *before launching a new conversion by pulling* $\overline{CS}$ low. If a conversion is aborted by pulling $\overline{CS}$ high before the conversions end, wait for the minimum acquisition time, t_{ACQ}, before starting a new conversion.

Data can be output in 1-byte chunks or continuously, as shown in Figure 8. The bytes will contain the result of the conversion padded with one leading 1, and trailing 0s if SCLK is still active with $\overline{CS}$ kept low.

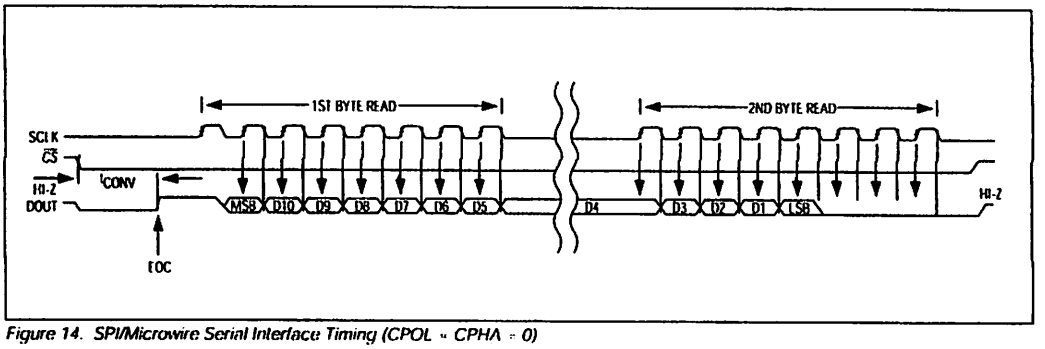


Figure 14. SPI/Microwire Serial Interface Timing (CPOL = CPHA = 0)

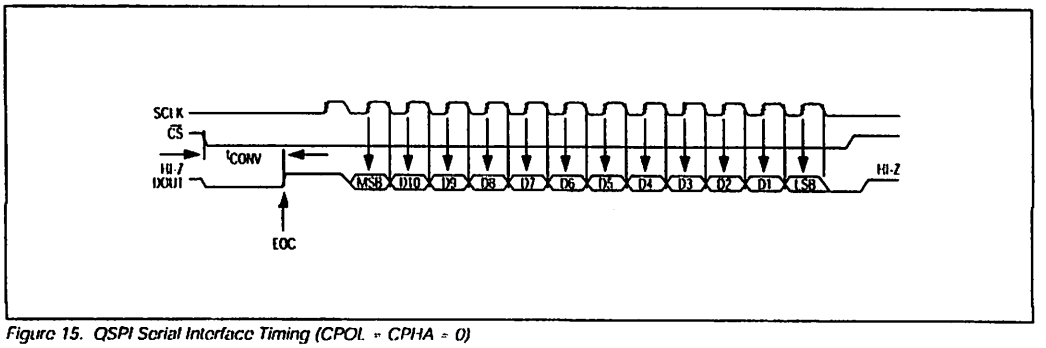


Figure 15. QSPI Serial Interface Timing (CPOL = CPHA = 0)

+5V, Low-Power, 12-Bit Serial ADCs

SPI and Microwire

When using SPI or QSPI, set CPOL = 0 and CPHA = 0. Conversion begins with a $\overline{CS}$ falling edge. DOUT goes low, indicating a conversion in progress. Wait until DOUT goes high or the maximum specified 8.5µs conversion time. Two consecutive 1-byte reads are required to get the full 12 bits from the ADC. DOUT output data transitions on SCLK's falling edge and is clocked into the µP on SCLK's rising edge.

The first byte contains a leading 1 and 7 bits of conversion result. The second byte contains the remaining 5 bits and 3 trailing 0s. See Figure 13 for connections and Figure 14 for timing.

QSPI

Set CPOL = CPHA = 0. Unlike SPI, which requires two 1-byte reads to acquire the 12 bits of data from the ADC, QSPI allows the minimum number of clock cycles necessary to clock in the data. The MAX187/MAX189 require 13 clock cycles from the µP to clock out the 12 bits of data with no trailing 0s (Figure 15). The maximum clock frequency to ensure compatibility with QSPI is 2.77MHz.

Opto-Isolated Interface, Serial-to-Parallel Conversion

Many industrial applications require electrical isolation to separate the control electronics from hazardous electrical conditions, provide noise immunity, or prevent excessive current flow where ground disparities exist between the ADC and the rest of the system. Isolation amplifiers typically used to accomplish these tasks are expensive. In cases where the signal is eventually converted to a digital form, it is cost effective to isolate the input using opto-couplers in a serial link.

The MAX187 is ideal in this application because it includes both T/H amplifier and voltage reference, operates from a single supply, and consumes very little power (Figure 16).

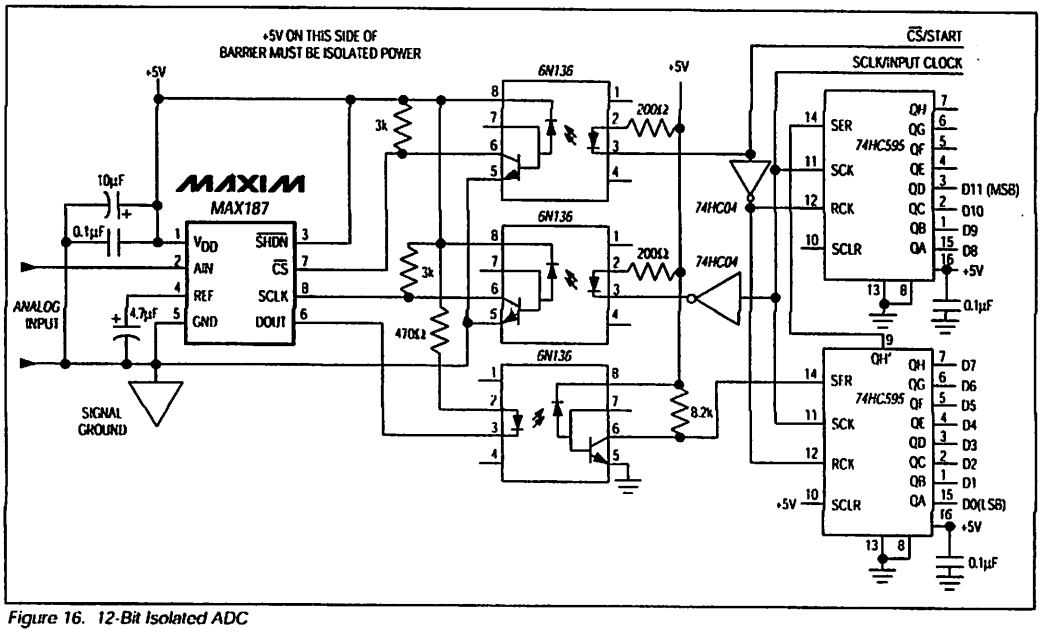


Figure 16. 12-Bit Isolated ADC

The ADC results are transmitted across a 1500V isolation barrier provided by three 6N136 opto-isolators. Isolated power must be supplied to the converter and the isolated side of the opto-couplers. 74HC595 three-state shift registers are used to construct a 12-bit parallel data output. The timing sequence is identical to the timing shown in Figure 8. Conversion speed is limited by the delay through the opto-isolators. With a 140kHz clock, conversion time is 100µs.

The universal 12-bit parallel data output can also be used without the isolation stage when a parallel interface is required. Clock frequencies up to 2.9MHz are possible without violating the 20ns shift-register setup time. Delay or invert the clock signal to the shift registers beyond 2.9MHz.

Layout, Grounding, Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 17 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at GND, separate from the logic ground. All other analog grounds should be connected to this ground. The 16-pin versions also have a dedicated DGND pin available. Connect DGND to this star ground point for further noise reduction. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the ADC's high speed comparator. Bypass this supply to the single point analog ground with 0.01µF and 4.7µF bypass capacitors. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter to attenuate supply noise (Figure 17).

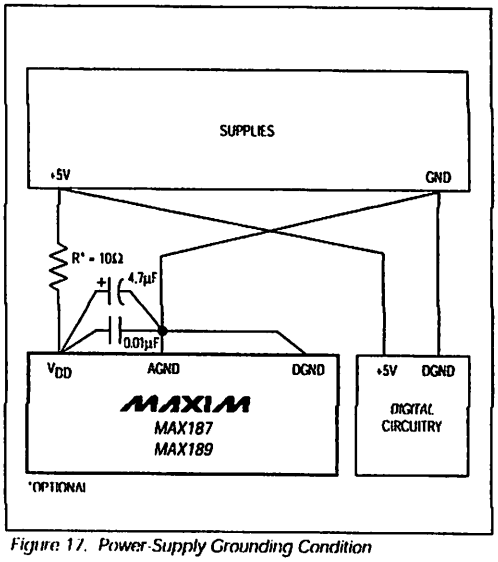


Figure 17. Power-Supply Grounding Condition

+5V, Low-Power, 12-Bit Serial ADCs

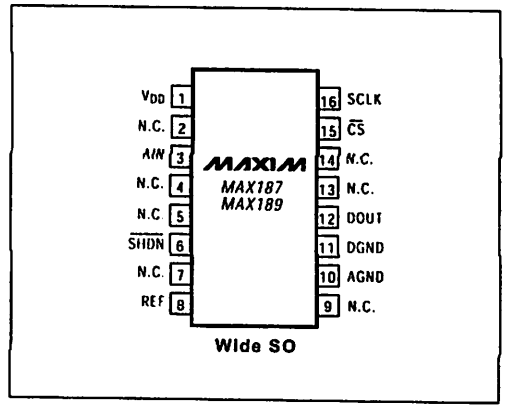
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX187AEPA	-40°C to +85°C	8 Plastic DIP	±½
MAX187BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX187CEPA	-40°C to +85°C	8 Plastic DIP	±2
MAX187AEWE	-40°C to +85°C	16 Wide SO	±½
MAX187BEWE	-40°C to +85°C	16 Wide SO	±1
MAX187CEWE	-40°C to +85°C	16 Wide SO	±2
MAX187AMJA	-55°C to +125°C	8 CERDIP**	±½
MAX187BMJA	-55°C to +125°C	8 CERDIP**	±1
MAX189ACPA	0°C to +70°C	8 Plastic DIP	±½
MAX189BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX189CCPA	0°C to +70°C	8 Plastic DIP	±2
MAX189ACWE	0°C to +70°C	16 Wide SO	±½
MAX189BCWE	0°C to +70°C	16 Wide SO	±1
MAX189CCWE	0°C to +70°C	16 Wide SO	±2
MAX189BC/D	0°C to +70°C	Dice*	±1
MAX189AEPA	-40°C to +85°C	8 Plastic DIP	±½
MAX189BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX189CEPA	-40°C to +85°C	8 Plastic DIP	±2
MAX189AEWE	-40°C to +85°C	16 Wide SO	±½
MAX189BEWE	-40°C to +85°C	16 Wide SO	±1
MAX189CEWE	-40°C to +85°C	16 Wide SO	±2
MAX189AMJA	-55°C to +125°C	8 CERDIP**	±½
MAX189BMJA	-55°C to +125°C	8 CERDIP**	±1

** Dice are specified at T_A = +25°C, DC parameters only.*

***Contact factory for availability and processing to MIL-STD-883.*

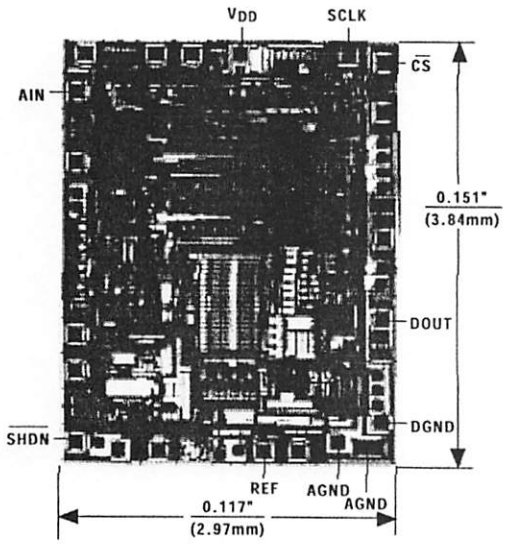
Pin Configurations (continued)



Wide SO

Chip Topography

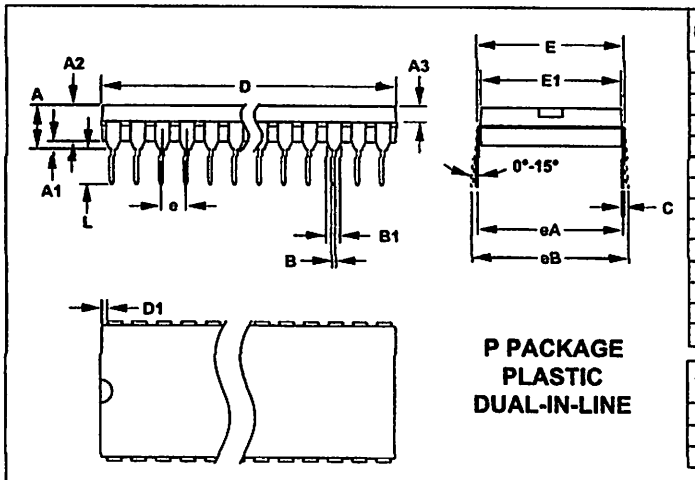
MAX187/MAX189



TRANSISTOR COUNT: 2278;
SUBSTRATE CONNECTED TO V_{DD}.

+5V, Low-Power, 12-Bit Serial ADCs

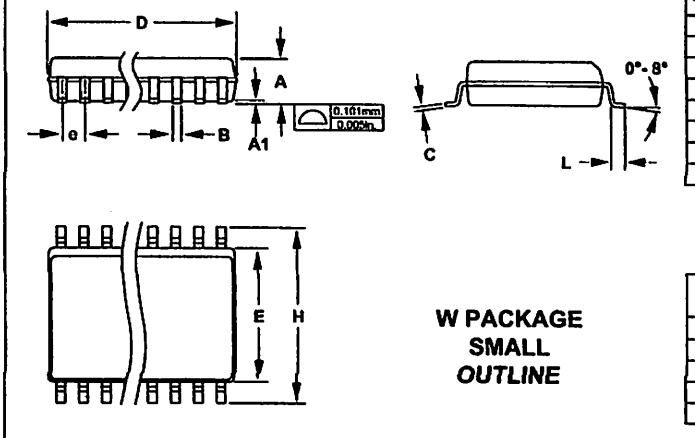
Package Information



P PACKAGE
PLASTIC
DUAL-IN-LINE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100	–	2.54	–
eA	0.600	–	15.24	–
eB	–	0.700	–	17.78
L	0.120	0.150	3.05	3.81

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	24	1.230	1.270	31.24	32.26
D	28	1.430	1.470	36.32	37.34
D	40	2.025	2.075	51.44	52.71



W PACKAGE
SMALL
OUTLINE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	*0.016*	*0.050*	*0.40*	*1.27*

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

21-0042A

Features

- Compatible with MCS®51 Products
- 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 1,000 Write/Erase Cycles
- 2K Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- 4V to 6V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Nine Interrupt Sources
- Programmable UART Serial Channel
- SPI Serial Interface
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down
- Programmable Watchdog Timer
- Dual Data Pointer
- Power-off Flag

Description

The AT89S8252 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of downloadable Flash programmable and erasable read-only memory and 2K bytes of EEPROM. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip downloadable Flash allows the program memory to be reprogrammed In-System through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with downloadable Flash on a monolithic chip, the Atmel AT89S8252 is a powerful microcontroller, which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S8252 provides the following standard features: 8K bytes of downloadable Flash, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S8252 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

The downloadable Flash can be changed a single byte at a time and is accessible through the SPI serial interface. Holding RESET active forces the SPI bus into a serial programming interface and allows the program memory to be written to or read from unless lock bits have been activated.

ATMEL®

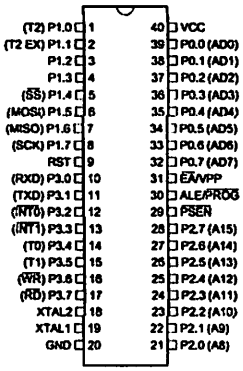
8-bit Microcontroller with 8K Bytes Flash

AT89S8252

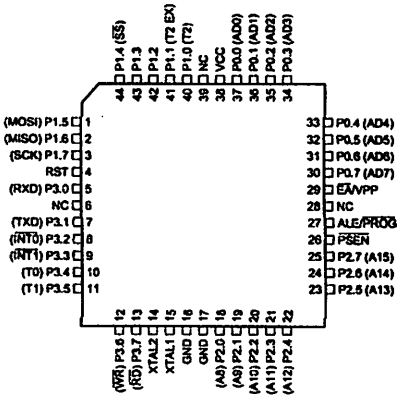
0401F–MICRO–11/03

Pin Configurations

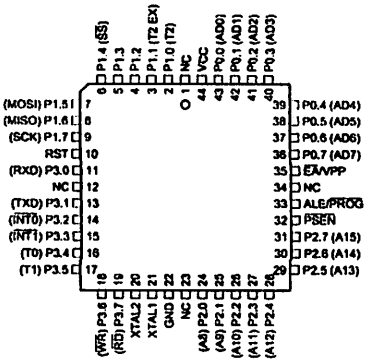
PDIP



TQFP



PLCC



Pin Description

VCC Supply voltage.

GND Ground.

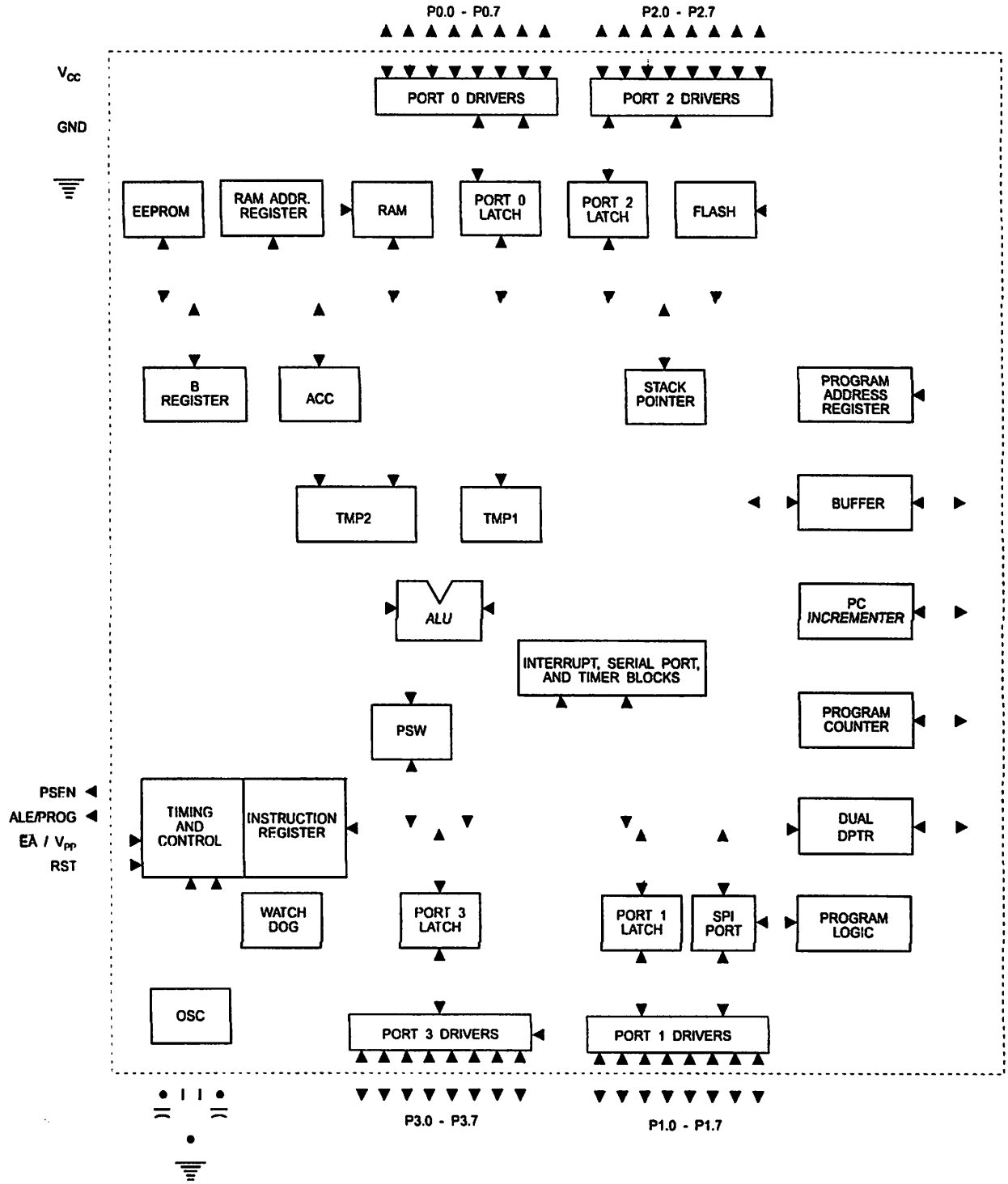
Port 0 Port 0 is an 8-bit open drain bi-didirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during *accesses to external program and data memory. In this mode, P0 has internal pull-ups.*

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1 Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers *can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high* by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Block Diagram



Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). *In this application, Port 2 uses strong internal pull-ups when emitting 1s. During* accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in *external execution mode*.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Table 1. AT89S8252 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DF H
0D0H	PSW 00000000					SPCR 000001XX			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CF H
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX						0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						WMCON 00000010		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

Table 2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if *Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.*
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When *either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.*

Watchdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in Table 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

Table 3. WMCON—Watchdog and Memory Control Register

WMCON Address = 96H — Reset Value = 0000 0010B

Bit	PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
	7	6	5	4	3	2	1	0

Symbol	Function
PS2 PS1 PS0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EEMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EEMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
DPS	*Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the* second bank, DP1
WDTRST RDY/$\overline{BSY}$	Watchdog Timer Reset and EEPROM Ready/$\overline{Busy}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{BSY}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{BSY}$ bit equals "0" and is automatically reset to "1" when programming is completed.
WDTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

Table 4. SPCR – SPI Control Register

SPCR Address = D5H — Reset Value = 0000 01XXB

Bit	7	6	5	4	3	2	1	0
	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

Symbol	Function
SPIE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
CPOL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
CPHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
SPR0 SPR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{osc.}$, is as follows: SPR1 SPR0 SCK = $F_{osc.}$ divided by 0 0 4 0 1 16 1 0 64 1 1 128

Table 5. SPSR – SPI Status Register

SPSR Address = AAH — Reset Value = 00XX XXXXB

Bit	7	6	5	4	3	2	1	0
	SPIF	WCOL	–	–	–	–	–	–

Symbol	Function
SPIF	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then reading/writing the SPI data register.
WCOL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

Table 6. SPDR – SPI Data Register

SPDR Address = 86H — Reset Value = unchanged

Bit	7	6	5	4	3	2	1	0
	SPD7	*SPD6*	*SPD5*	*SPD4*	*SPD3*	*SPD2*	*SPD1*	*SPD0*

Data Memory – EEPROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. RDY/$\overline{BSY}$ = 0 means

programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent internal oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			
PS2	**PS1**	**PS0**	**Period (nominal)**
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected.

Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

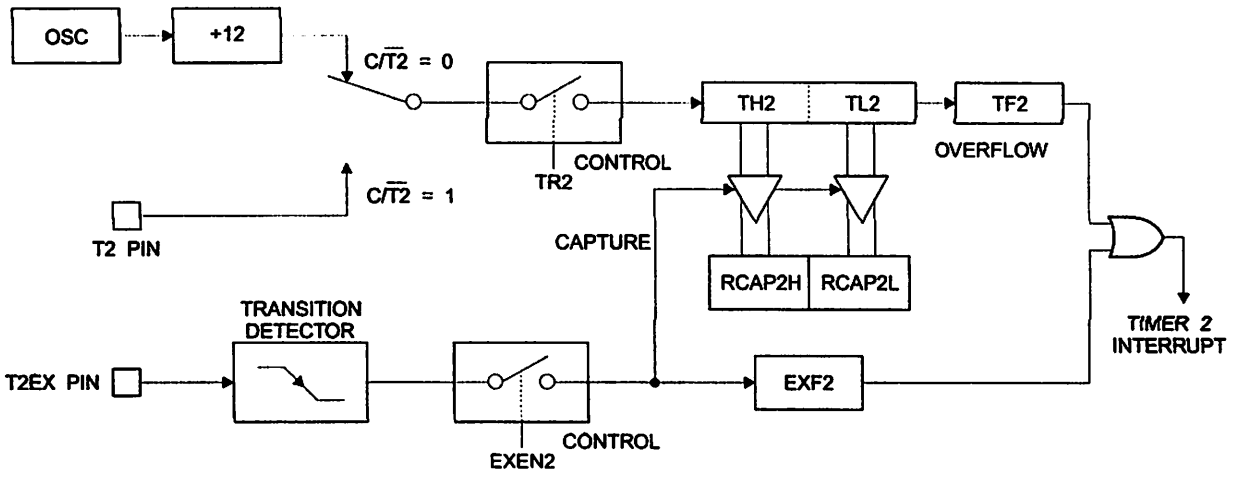
Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a I-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Figure 1. Timer 2 in Capture Mode



Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 2. Timer 2 in Auto Reload Mode (DCEN = 0)

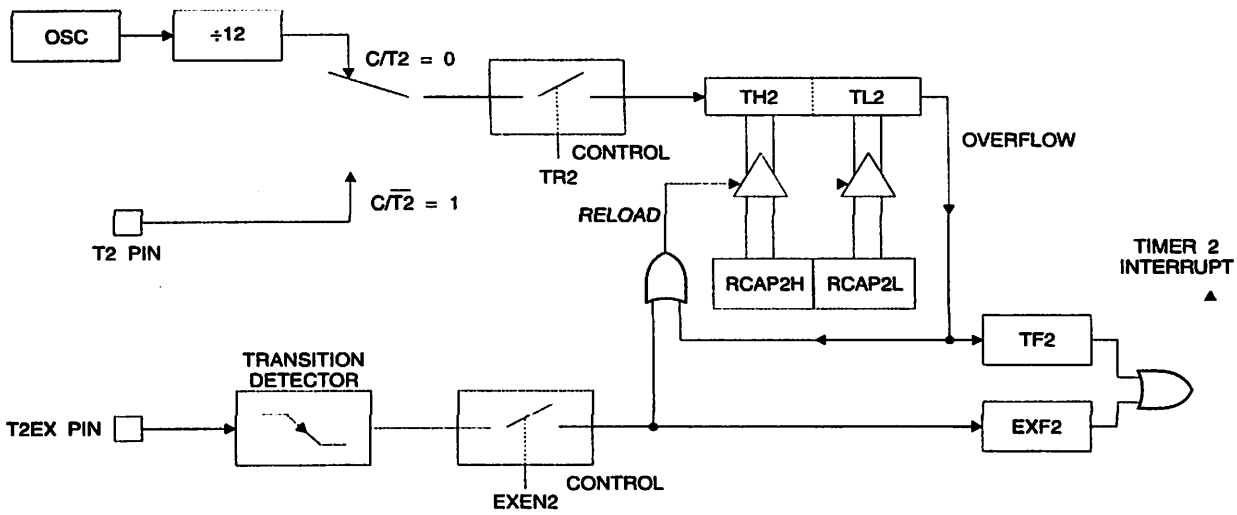


Table 9. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

	–	–	–	–	–	–	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
–	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

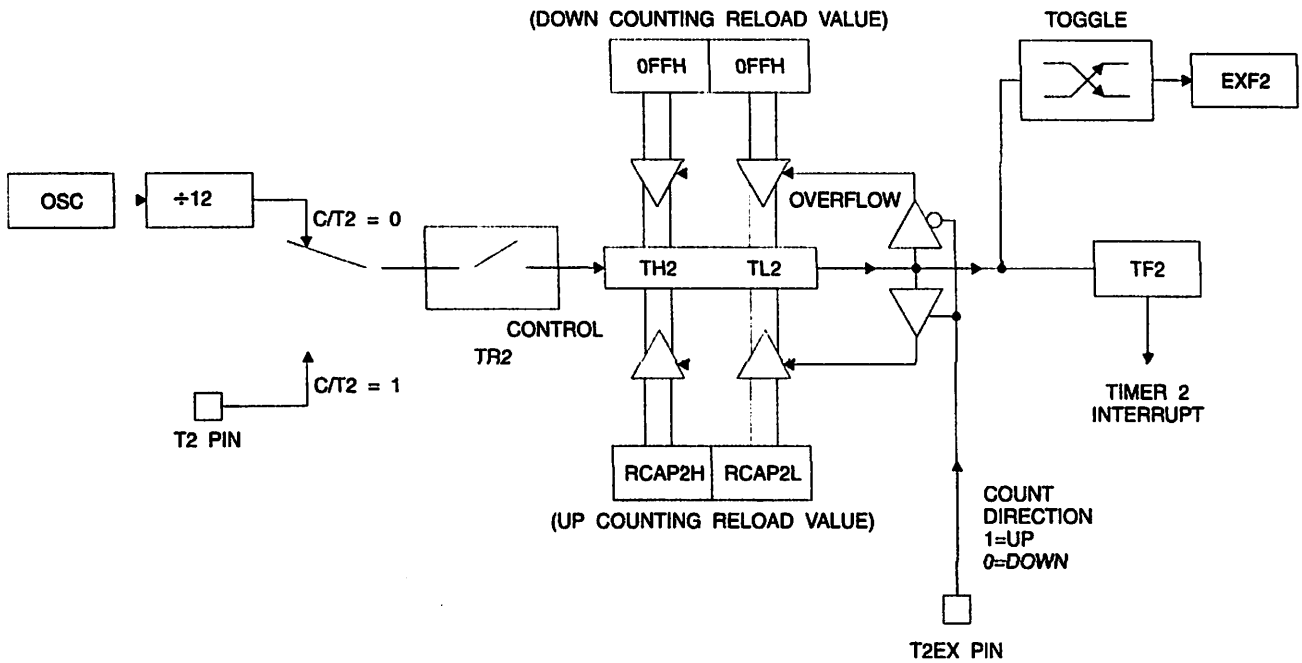
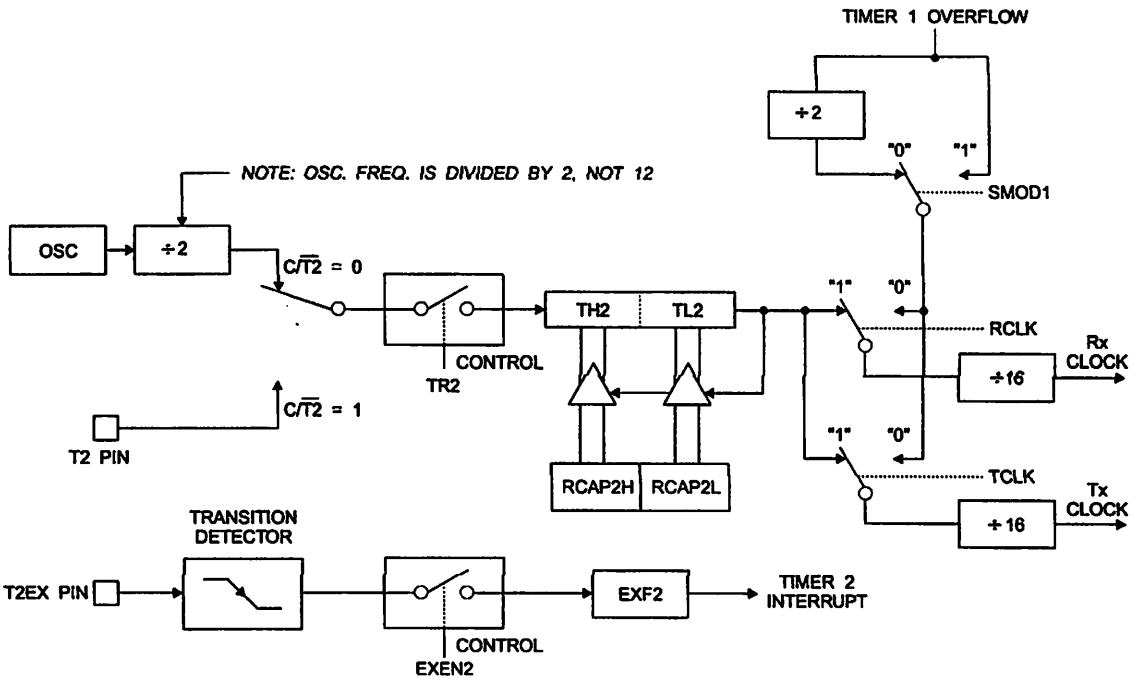


Figure 4. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, *TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is* incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/0 pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Figure 5. Timer 2 in Clock-out Mode

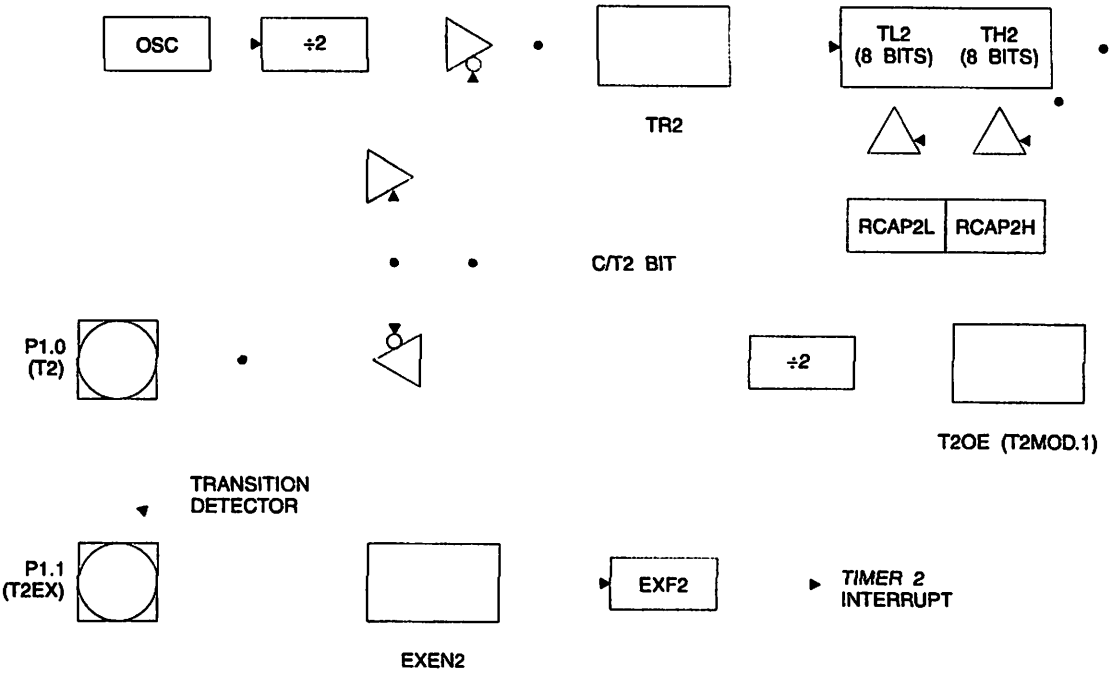
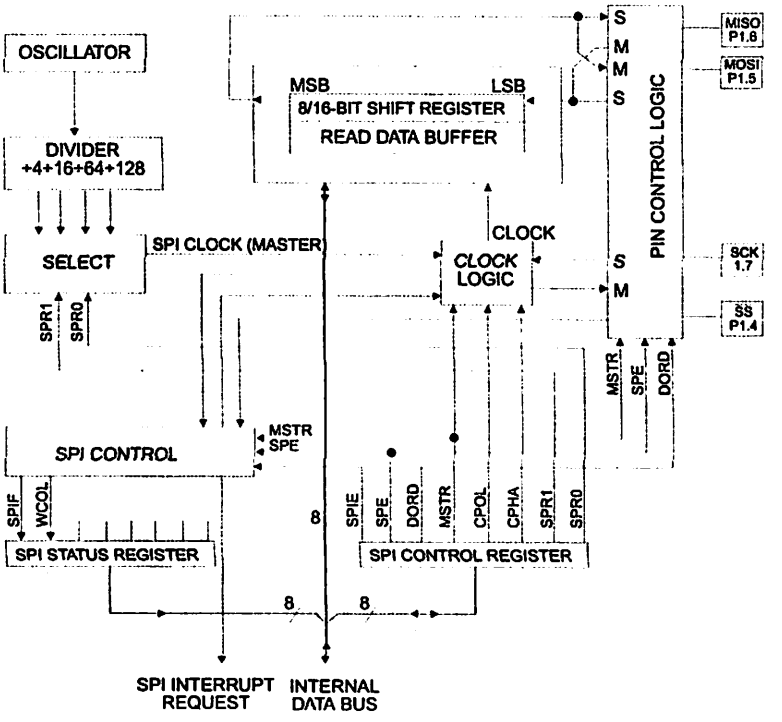


Figure 6. SPI Block Diagram



UART

The UART in the AT89S8252 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5 MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

Figure 7. SPI Master-slave Interconnection

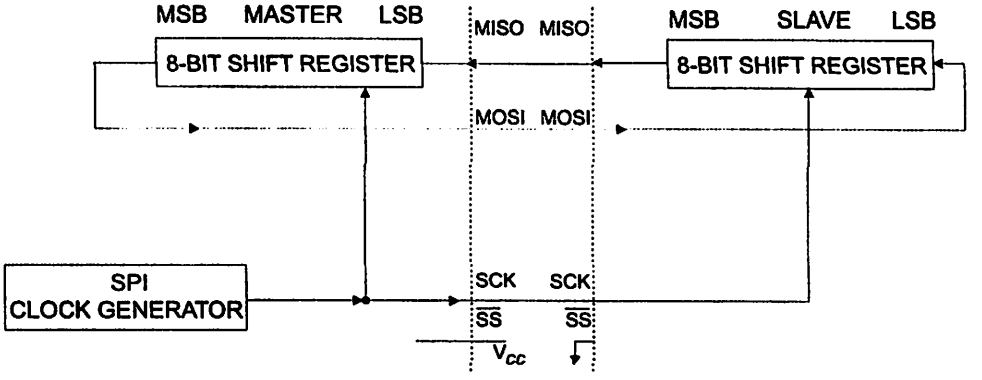
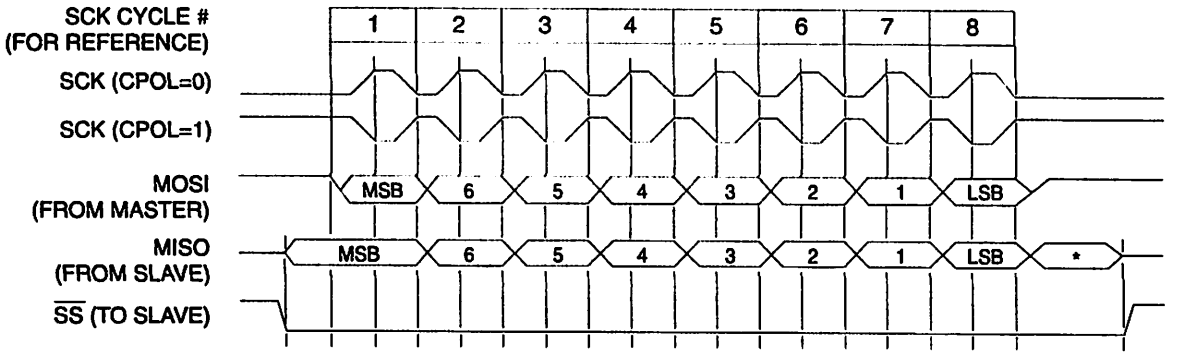
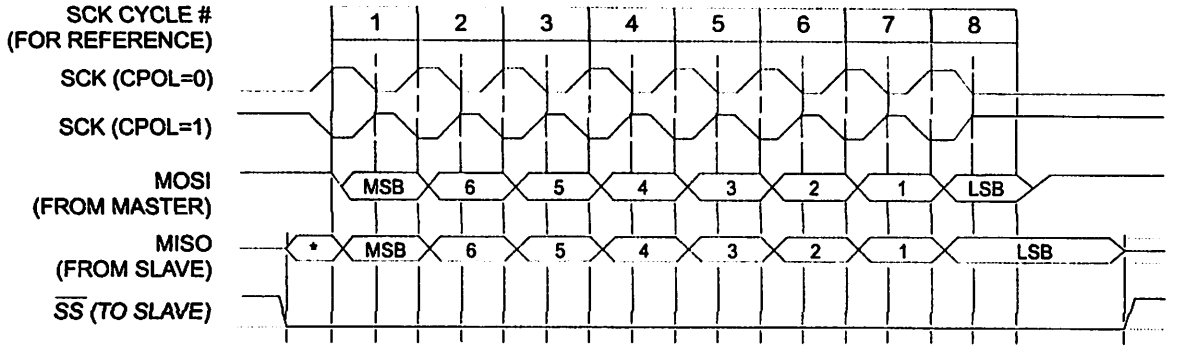


Figure 8. SPI transfer Format with CPHA = 0



Note: *Not defined but normally MSB of character just received

Figure 9. SPI Transfer Format with CPHA = 1



Note: *Not defined but normally LSB of previously transmitted character.

Interrupts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 10. Interrupt Enable (IE) Register

(MSB)(LSB)

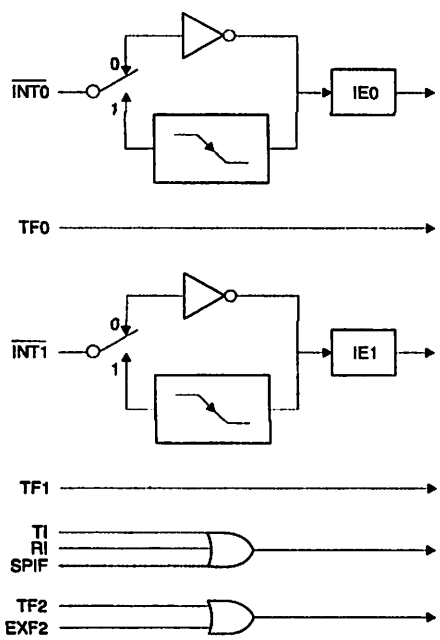
EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.		

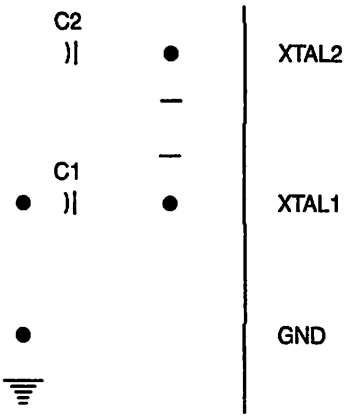
Figure 10. Interrupt Sources



Oscillator Characteristics

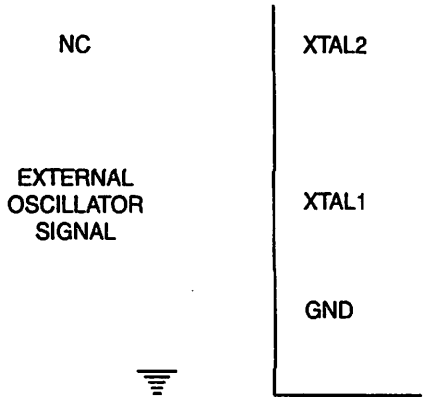
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but *minimum and maximum voltage high and low time specifications must be observed.*

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Power-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, the external interrupt must be enabled as level sensitive before entering power-down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Lock Bit Protection Modes[1][2]

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

Notes: 1. U = Unprogrammed
2. P = Programmed

Programming the Flash and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-voltage (12-V V_{PP}) Parallel programming mode and a Low-voltage (5-V V_{CC}) Serial programming mode. The serial programming mode provides a convenient way to reprogram the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to *27FFH for the Data array.*

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm: To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between V_{CC} and GND pins.
   Set RST pin to "H".
   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{PSEN}$ pin to "L"
   ALE pin to "H"
   $\overline{EA}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.
   Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:
   Set XTAL1 to "L".
   Set RST and $\overline{EA}$ pins to "L".
   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Data Polling: The AT89S8252 features DATA Polling to indicate the end of a byte write cycle. During a byte write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum *on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial* mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. DATA Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/BSY output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate BUSY. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse: A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

Programming Interface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Serial Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Algorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the *content at the selected address at serial output MISO/P1.6.*
5. At the end of a programming session, RST can be set low to commence normal operation.
6. Power-off sequence (if needed):

   Set XTAL1 to "L" (if a crystal is not used).

   Set RST to "L".

   Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

Instruction Set

Instruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Chip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
Read Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are *available at pin MISO during the third byte.*
Write Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
Read Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Write Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Write Lock Bits	1010 1100	LB1 LB2 LB3 x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

Notes:
1. DATA polling is used to indicate the end of a byte write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

Flash and EEPROM Parallel Programming Modes

Mode	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
Serial Prog. Modes	H	h[1]	h[1]	x						
Chip Erase	H	L	⌐⌐ (2)	12V	H	L	L	L	X	X
Write (10K bytes) Memory	H	L	⌐⌐	12V	L	H	H	H	DIN	ADDR
Read (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
Write Lock Bits:	H	L	⌐⌐	12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
Read Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
Read Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
Read Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Serial Prog. Enable	H	L	⌐⌐ (2)	12V	L	H	L	H	P0.0 = 0	X
Serial Prog. Disable	H	L	⌐⌐ (2)	12V	L	H	L	H	P0.0 = 1	X
Read Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

Notes:
1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10 ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{BSY}$.
4. *"X" = don't care*

Figure 13. Programming the Flash/EEPROM Memory

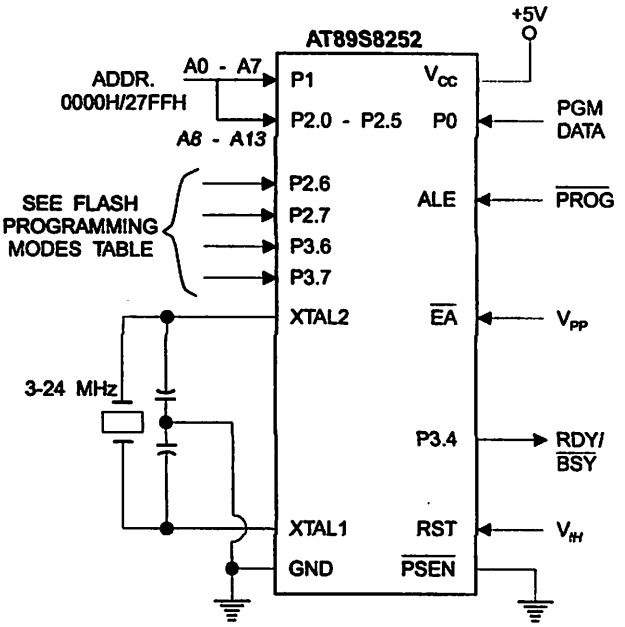


Figure 14. Verifying the Flash/EEPROM Memory

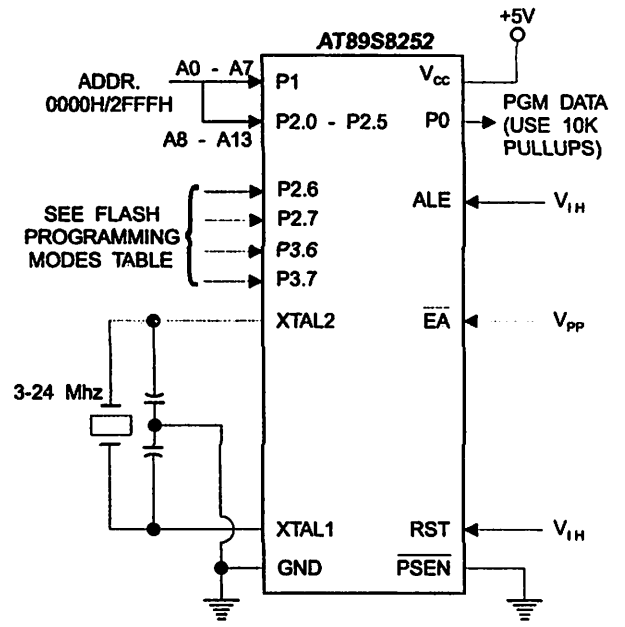
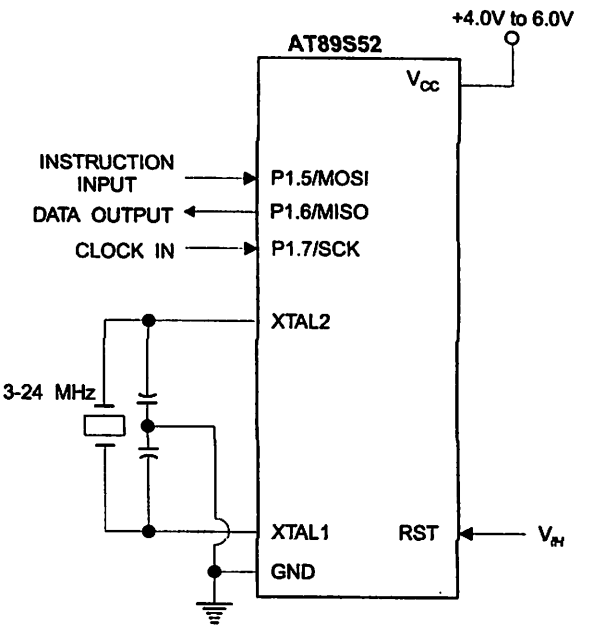


Figure 15. Flash/EEPROM Serial Downloading

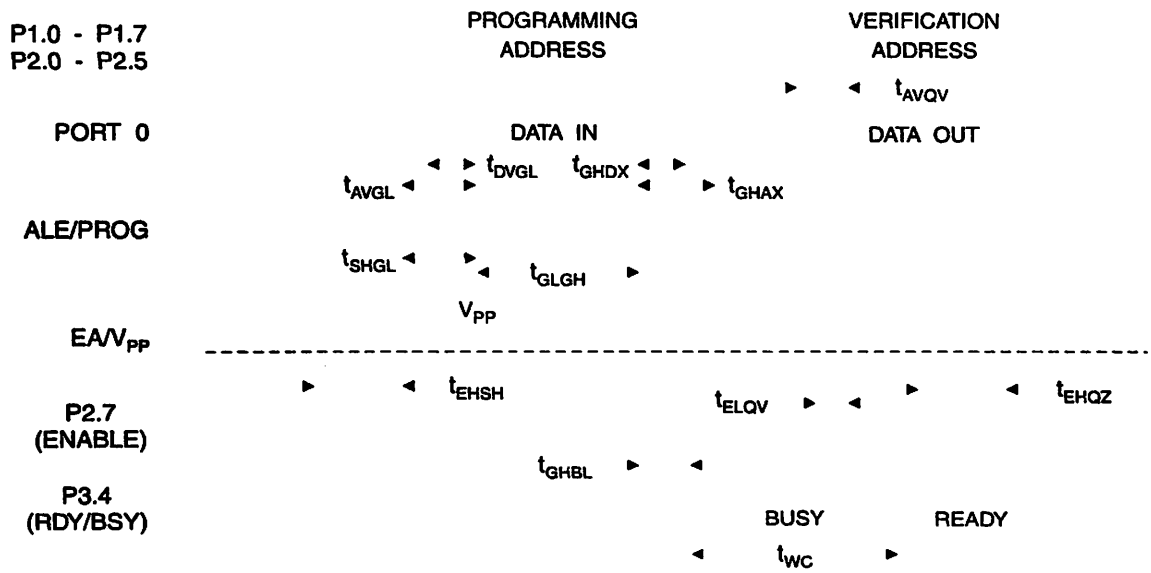


Flash Programming and Verification Characteristics – Parallel Mode

T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Flash/EEPROM Programming and Verification Waveforms – Parallel Mode



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin *with Respect to Ground*	*-1.0V to +7.0V*
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the *operational sections of this specification is not* implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

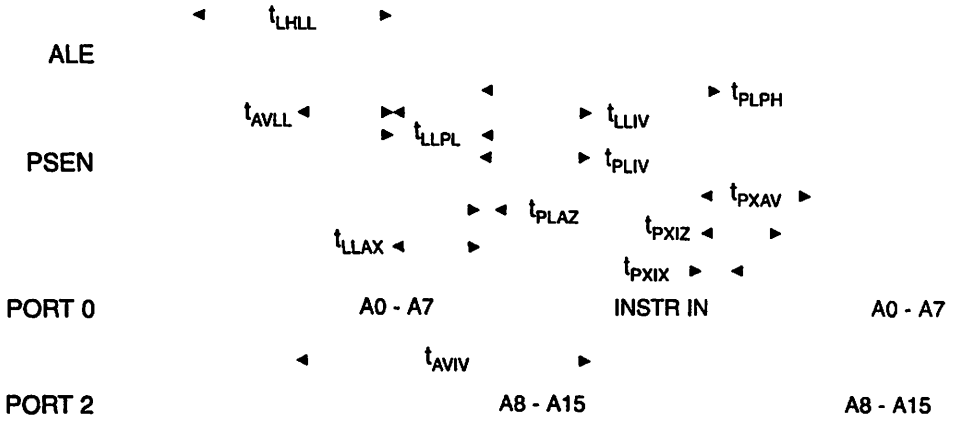
DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

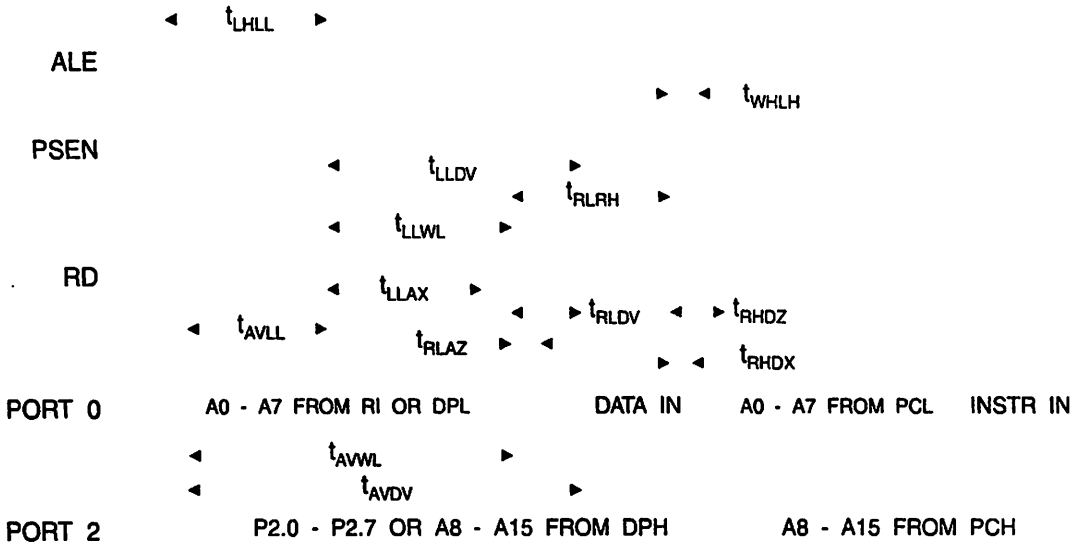
Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage (1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
V_{OL1}	Output Low-voltage (1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
V_{OH}	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	*Pin Capacitance*	*Test Freq. = 1 MHz, T_A = 25°C*		*10*	*pF*
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode (2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port: Port 0: 26 mA; Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V

External Program Memory Read Cycle



External Data Memory Read Cycle

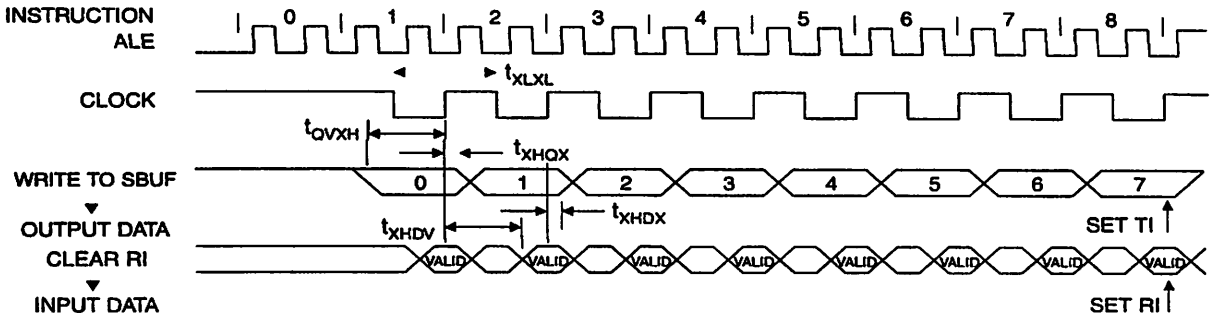


Serial Port Timing: Shift Register Mode Test Conditions

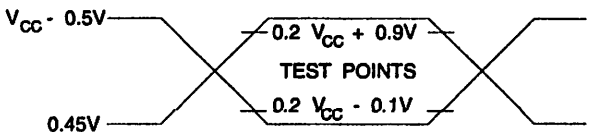
The values in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ - 117		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

Shift Register Mode Timing Waveforms

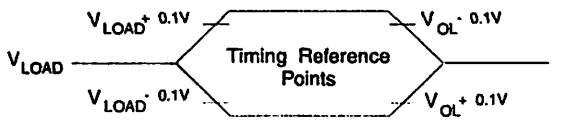


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

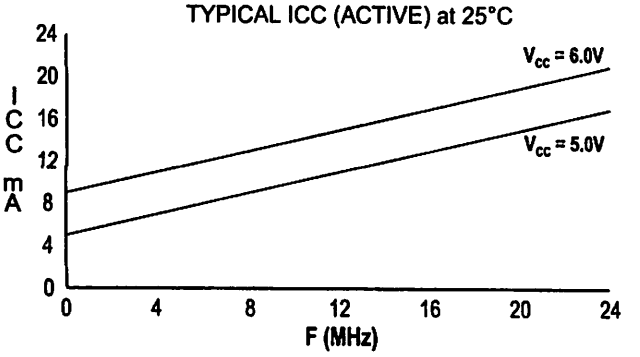
Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

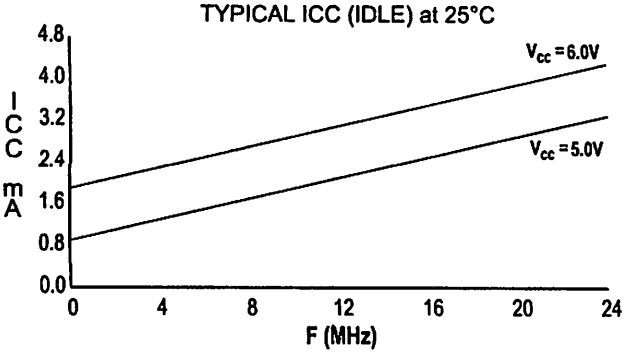
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



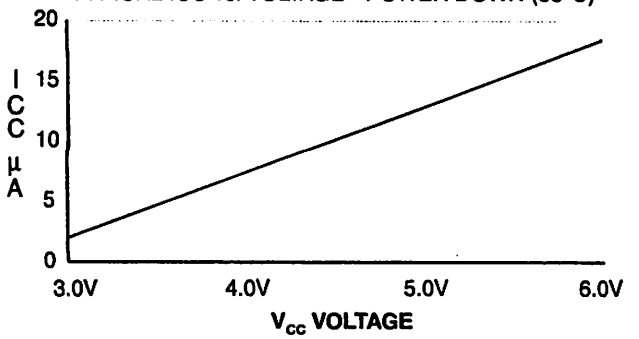
AT89S8252

TYPICAL ICC (IDLE) at 25°C



AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



Notes: 1. XTAL1 tied to GND for Icc (power-down)
2. Lock bits programmed

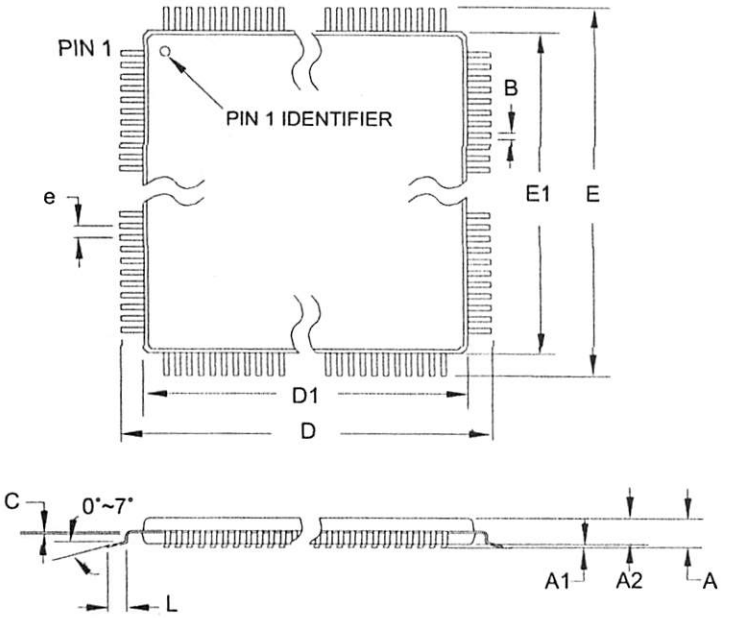
Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 6.0V	AT89S8252-24AC AT89S8252-24JC AT89S8252-24PC	44A 44J 40P6	Commercial (0° C to 70° C)
	4.0V to 6.0V	AT89S8252-24AI AT89S8252-24JI AT89S8252-24PI	44A 44J 40P6	Industrial (-40° C to 85° C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Packaging Information

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

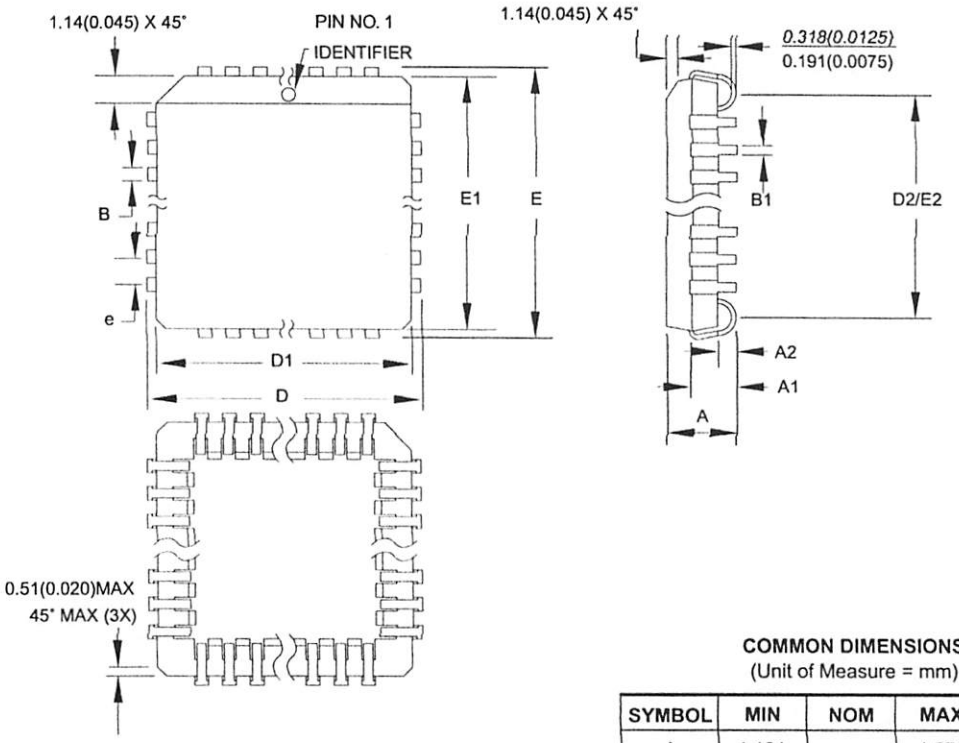
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

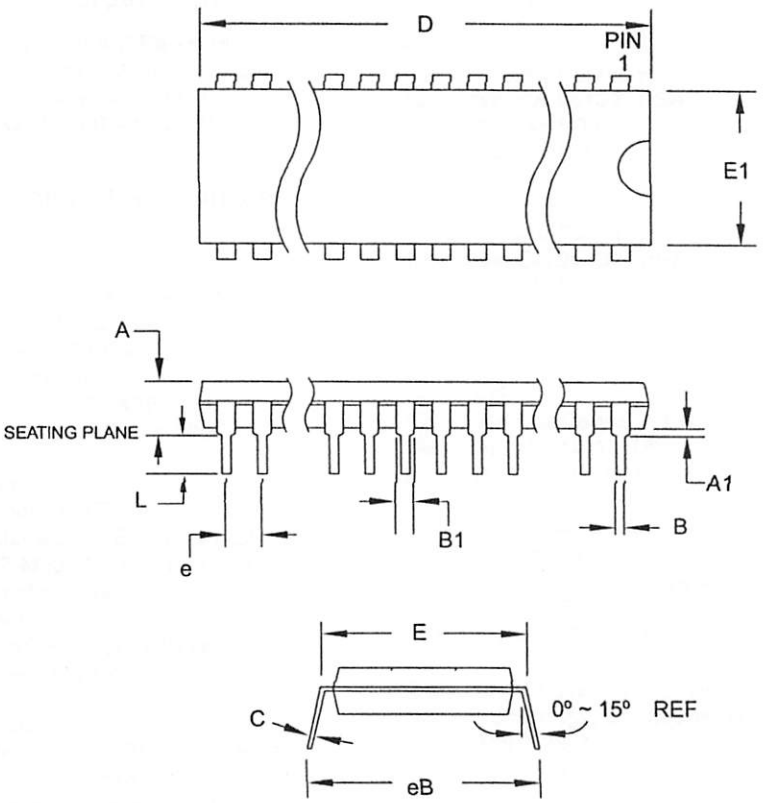
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	*0.660*	–	*0.813*	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

National Semiconductor

October 1991

TP5088 DTMF Generator for Binary Data

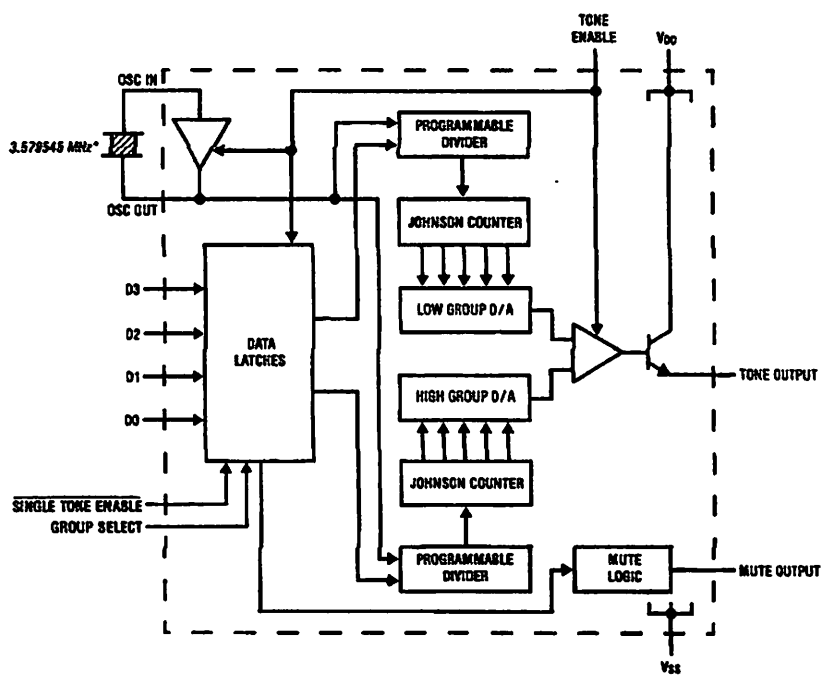
General Description

This CMOS device provides low cost tone-dialing capability in microprocessor-controlled telephone applications. 4-bit binary data is decoded directly, without the need for conversion to simulated keyboard inputs required by standard DTMF generators. With the TONE ENABLE input low, the oscillator is inhibited and the device is in a low power idle mode. On the low-to-high transition of TONE ENABLE, data is latched into the device and the selected tone pair from the standard DTMF frequencies is generated. An open-drain N-channel transistor provides a MUTE output during tone generation.

Features

- Direct microprocessor interface
- Binary data inputs with latches
- Generates 16 standard tone pairs
- On-chip 3.579545 MHz crystal-controlled oscillator
- Better than 0.64% frequency accuracy
- High group pre-emphasis
- Low harmonic distortion
- MUTE output interfaces to speech network
- Low power idle mode
- 3.5V–8V operation

Block Diagram



TL/H/5004–1

*Crystal Specification: Parallel Resonant 3.579545 MHz, $R_S \leq 150\Omega$, L = 100 mH, C_0 = 5 pF, C_1 = 0.02 pF.

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{DD} - V_{SS}$)	12V
$\overline{MUTE}$ Voltage	12V
Maximum Voltage at Any Other Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Operating Temperature, T_A	−30°C to +70°C
Storage Temperature	−55°C to +150°C
Maximum Power Dissipation	500 mW

Electrical Characteristics

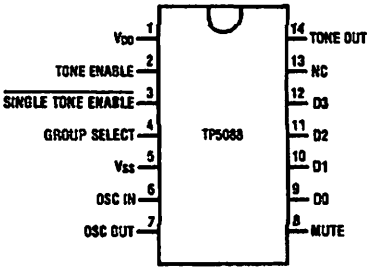
Unless otherwise noted, limits printed in **BOLD** *characters are guaranteed for* V_{DD} = 3.5V to 8V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Parameter	Conditions	Min	Typ	Max	Units
Minimum Supply Voltage, V_{DD} (min)	Generating Tones	**3.5**			V
Minimum Supply Voltage for Data Input, TONE ENABLE and MUTE Logic Functions		2			V
Operating Current					
Idle	R_L = ∞, D0–D3 Open		55	**350**	μA
Generating Tones	V_{DD} = 3.5V, Mute Open		1.5	**2.5**	mA
Input Pull-Up Resistance					
D0–D3			100		kΩ
TONE ENABLE			50		kΩ
Input Low Level					
TONE ENABLE, D0–D3				**0.2 V_{DD}**	V
Input High Level					
TONE ENABLE, D0–D3		**0.8 V_{DD}**			V
MUTE OUT Sink Current (TONE ENABLE LOW)	V_{DD} = 3.5V, V_o = 0.5V	**0.4**			mA
MUTE OUT Leakage Current (TONE ENABLE HIGH)	V_{DD} = 3.5V, V_o = V_{DD}		1		μA
Output Amplitudes	R_L = 240 Ω, V_{DD} = 3.5V, T_A = 25°C				
Low Group		**130**	170	**220**	mVrms
High Group		**180**	230	**310**	mVrms
Mean Output DC Offset	V_{DD} = 3.5V		1.2		V
	V_{DD} = 8V		3.6		V
High Group Pre-Emphasis		**2.2**	2.7	**3.2**	dB
Dual Tone/Total Harmonic Distortion Ratio	1 MHz Bandwidth, V_{DD} = 5V, R_L = 240Ω	**−20**			dB
Start-Up Time (to 90% Amplitude), t_{OSC}			4		ms
Data Set-Up Time, t_S (*Figure 2*)	V_{DD} = 5V	100			ns
Data Hold Time, t_H	V_{DD} = 5V	280			ns
Data Duration t_W	V_{DD} = 5V	600			ns

Note 1: R_L is the external load resistor connected from TONE OUT to V_{SS}.

Connection Diagram

Dual-In-Line Package



TL/H/5004–2

Top View

Order Number TP5088WM or TP5088N
See NS Package M14B or N14A

Functional Description

With the TONE ENABLE pin pulled low, the device is in a low power idle mode, with the oscillator inhibited and the output transistor turned off. Data on inputs D0–D3 is ignored until a rising transition on TONE ENABLE. Data meeting the timing specifications is latched in, the oscillator and output stage are enabled, and tone generation begins. The decoded data sets the high group and low group programmable counters to the appropriate divide ratios. These counters sequence two ratioed-capacitor D/A converters *through a series of 28 equal duration steps per sine wave* cycle. On-chip regulators ensure good stability of tone amplitudes with variations in supply voltage and temperature. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}.

Table I shows the accuracies of the tone output frequencies and Table II is the Functional Truth Table.

TABLE I. Output Frequency Accuracy

Tone Group	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group f_L	697	694.8	0.32
	770	770.1	+ 0.02
	852	852.4	+ 0.03
	941	940.0	0.11
High Group f_H	1209	1206.0	0.24
	1336	1331.7	0.32
	1477	1486.5	+ 0.64
	1633	1639.0	+ 0.37

Pin Descriptions

V_{DD} (Pin 1): This is the positive supply to the device, referenced to V_{SS}. The collector of the TONE OUT transistor is also connected to this pin.

V_{SS} (Pin 5): This is the negative voltage supply. All voltages are referenced to this pin.

OSC IN, OSC OUT (Pins 6 and 7): All tone generation timing is derived from the on-chip oscillator circuit. A low-cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) is needed between pins 6 and 7. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator is stopped when the TONE ENABLE input is pulled to logic low.

TONE ENABLE Input (Pin 2): This input has an internal pull-up resistor. When TONE ENABLE is pulled to logic low, the oscillator is inhibited and the tone generators and output transistor are turned off. A low to high transition on TONE ENABLE latches in data from D0–D3. The oscillator starts, and tone generation continues until TONE ENABLE is *pulled low again.*

MUTE (Pin 8): This output is an open-drain N-channel device that sinks current to V_{SS} when TONE ENABLE is low and no tones are being generated. The device turns off when TONE ENABLE is high.

D0, D1, D2, D3 (Pins 9, 10, 11, 12): These are the inputs for binary-coded data, which is latched in on the rising edge of TONE ENABLE. Data must meet the timing specifications of *Figure 2.* At all other times these inputs are ignored and may be multiplexed with other system functions.

TONE OUT (Pin 14): This output is the open emitter of an NPN transistor, the collector of which is connected internally to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group tones superimposed on a DC offset. When not generating tones, this output transistor is turned off to minimize the device idle current.

$\overline{\text{SINGLE TONE ENABLE}}$ (Pin 3): This input has an internal pull-up resistor. When pulled to V_{SS}, the device is in single tone mode and only a single tone will be generated at pin 14 (for testing purposes). For normal operation, leave this pin open-circuit or pull to V_{DD}.

GROUP SELECT (Pin 4): This pin is used to select the high group or low group frequency when the device is in single tone mode. It has an internal pull-up resistor. Leaving this pin open-circuit or pulling it to V_{DD} will generate the high group, while pulling to V_{SS} will generate the low group frequency at the TONE OUT pin.

TABLE II. Functional Truth Table

Keyboard Equivalent	Data Inputs				TONE ENABLE	TONES OUT		MUTE
	D3	D2	D1	D0		f_L (Hz)	f_H(Hz)	
X	X	X	X	X	0	0V	0V	0V
1	0	0	0	1	⌐	697	1209	O/C
2	0	0	1	0	⌐	697	1336	O/C
3	0	0	1	1	⌐	697	1477	O/C
4	0	1	0	0	⌐	770	1209	O/C
5	0	1	0	1	⌐	770	1336	O/C
6	0	1	1	0	⌐	770	1477	O/C
7	0	1	1	1	⌐	852	1209	O/C
8	1	0	0	0	⌐	852	1336	O/C
9	1	0	0	1	⌐	852	1477	O/C
0	1	0	1	0	⌐	941	1336	O/C
*	1	0	1	1	⌐	941	1209	O/C
#	1	1	0	0	⌐	941	1477	O/C
A	1	1	0	1	⌐	697	1633	O/C
B	1	1	1	0	⌐	770	1633	O/C
C	1	1	1	1	⌐	852	1633	O/C
D	0	0	0	0	⌐	941	1633	O/C

Timing Diagram

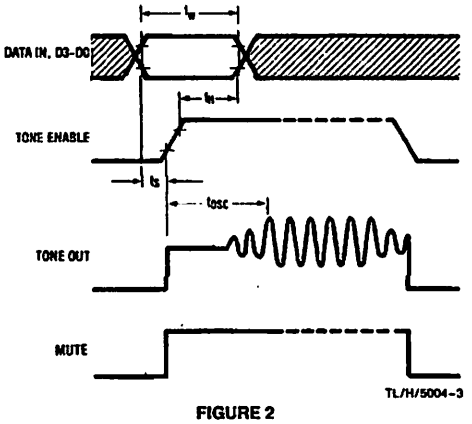
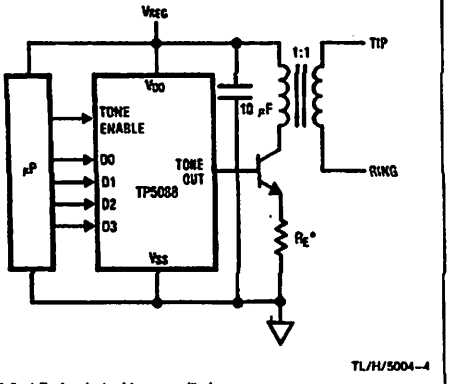


FIGURE 2

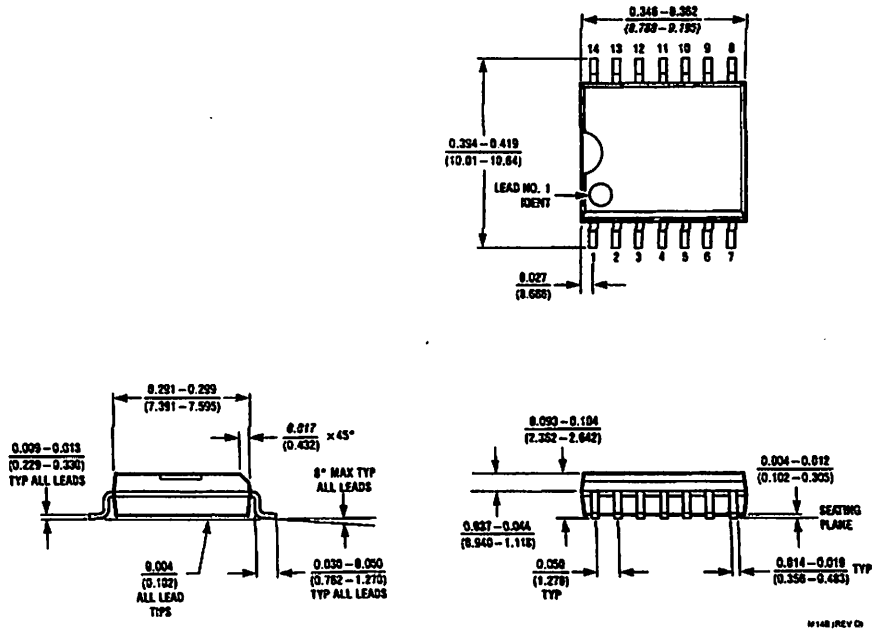
Typical Application



*Adjust R_E for desired tone amplitude.

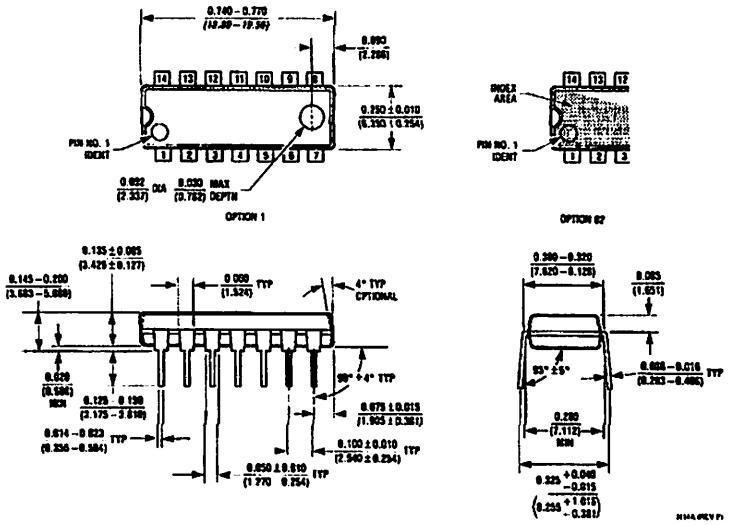
FIGURE 3

Physical Dimensions inches (millimeters)



Order Number TP5088WM
NS Package Number M14B

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line (N)
Order Number TP5088N
NS Package Number N14A

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

ISO²-CMOS MT8870D/MT8870D-1
Integrated DTMF Receiver

ISSUE 5 March 1997

Features
- Complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Backward compatible with MT8870C/MT8870C-1

Applications
- Receiver system for British Telecom (BT) or CEPT Spec (MT8870D-1)
- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- *Remote control*
- Personal computers
- Telephone answering machine

Ordering Information

MT8870DE/DE-1	18 Pin Plastic DIP
MT8870DS/DS-1	18 Pin SOIC
MT8870DN/DN-1	20 Pin SSOP

-40 °C to +85 °C

Description

The MT8870D/MT8870D-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

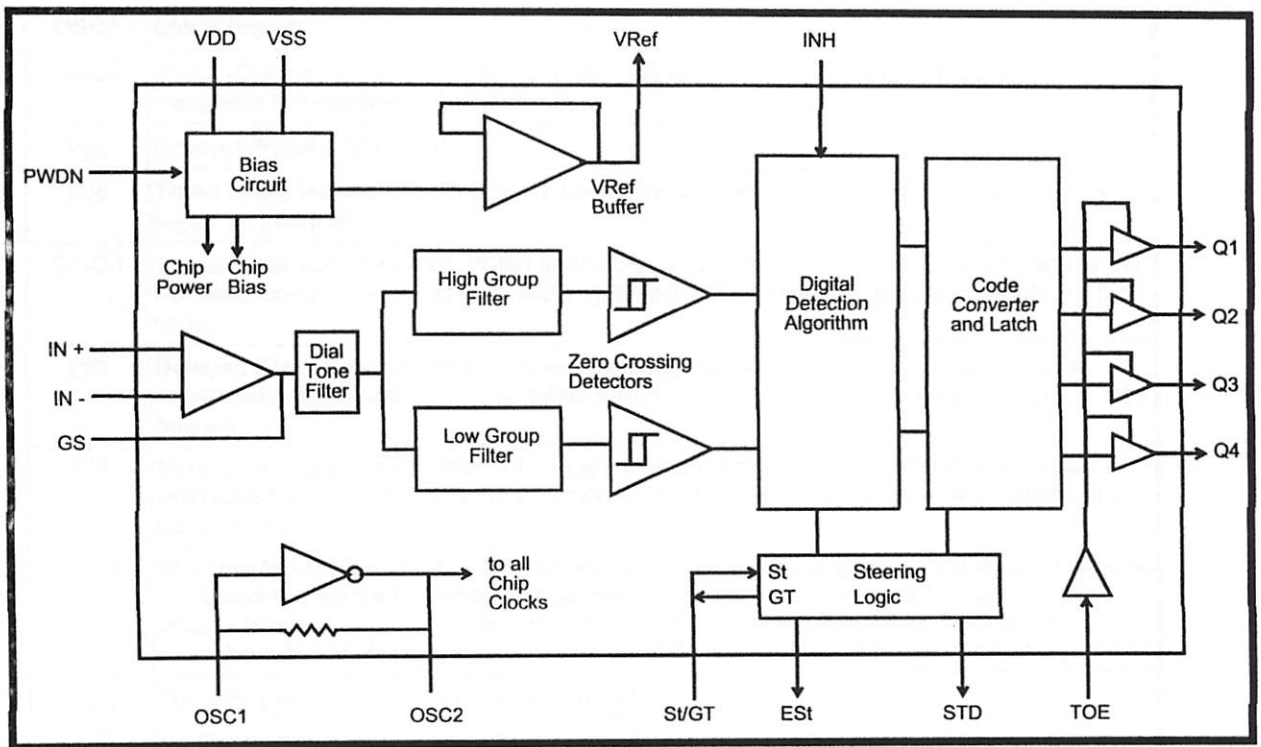


Figure 1 - Functional Block Diagram

Applications

RECEIVER SYSTEM FOR BRITISH TELECOM SPEC POR 1151

The circuit shown in Fig. 9 illustrates the use of MT8870D-1 device in a typical receiver system. BT Spec defines the input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing a suitable values of R_1 and R_2 to provide 3 dB attenuation, such that -34 dBm input signal will correspond to -37 dBm at the gain setting pin GS of MT8870D-1. As shown in the diagram, the component values of R_3 and C_2 are the guard time requirements when the total component tolerance is 6%. For better performance, it is recommended to use the non-symmetric guard time circuit in Fig. 8.

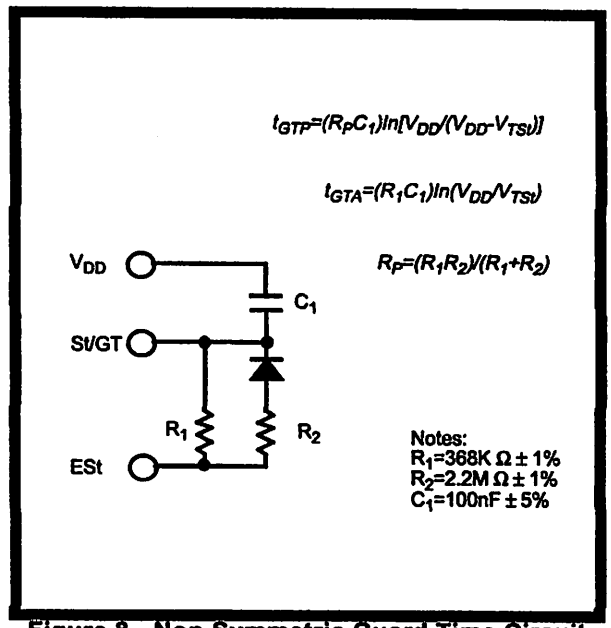


Figure 8 - Non-Symmetric Guard Time Circuit

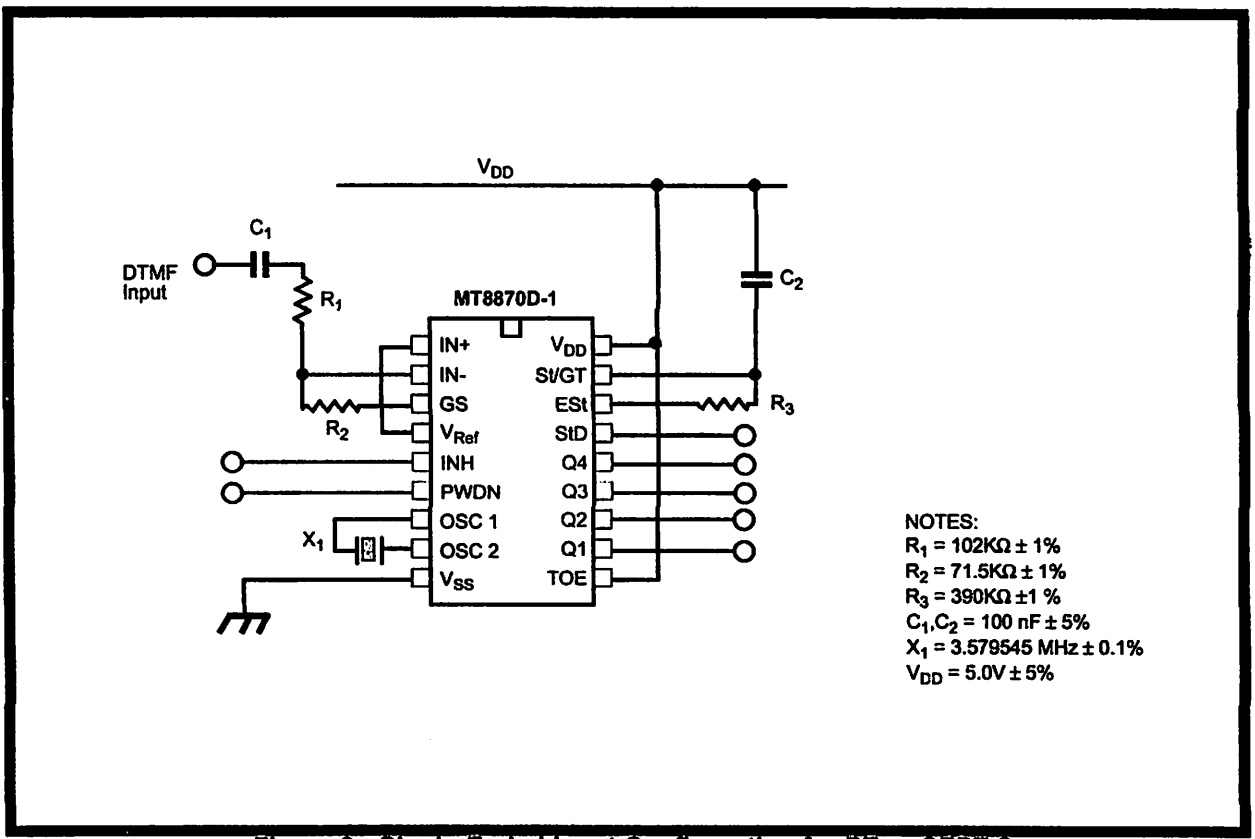


Figure 9 - Single-Ended Input Configuration for BT or CEPT Spec

Absolute Maximum Ratings†

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage	V_{DD}		7	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin (other than supply)	I_I		10	mA
4	Storage temperature	T_{STG}	-65	+150	°C
5	Package power dissipation	P_D		500	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Derate above 75 °C at 16 mW / °C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DC Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Operating Temperature	T_O	-40		+85	°C	
3	*Crystal/Clock Frequency*	*fc*		*3.579545*		MHz	
4	Crystal/Clock Freq.Tolerance	Δfc		±0.1		%	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - V_{DD}=5.0V± 5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUPPLY	Standby supply current	I_{DDQ}		10	25	µA	PWDN=V_{DD}
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_O		15		mW	fc=3.579545 MHz
4	INPUTS	High level input	V_{IH}	3.5			V	V_{DD}=5.0V
5		Low level input voltage	V_{IL}			1.5	V	V_{DD}=5.0V
6		Input leakage current	I_{IH}/I_{IL}		0.1		µA	V_{IN}=V_{SS} or V_{DD}
7		Pull up (source) current	I_{SO}		7.5	20	µA	TOE (pin 10)=0, V_{DD}=5.0V
8		Pull down (sink) current	I_{SI}		15	45	µA	INH=5.0V, PWDN=5.0V, V_{DD}=5.0V
9		Input impedance (IN+, IN-)	R_{IN}		10		MΩ	@ 1 kHz
10		Steering threshold voltage	V_{TSt}	2.2	2.4	2.5	V	V_{DD} = 5.0V
11	OUTPUTS	Low level output voltage	V_{OL}			V_{SS}+0.03	V	No load
12		High level output voltage	V_{OH}	V_{DD}-0.03			V	No load
13		Output low (sink) current	I_{OL}	1.0	2.5		mA	V_{OUT}=0.4 V
14		Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT}=4.6 V
15		V_{Ref} output voltage	V_{Ref}	2.3	2.5	2.7	V	No load, V_{DD} = 5.0V
16		V_{Ref} output resistance	R_{OR}		1		kΩ	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Operating Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C ,unless otherwise stated.

Gain Setting Amplifier

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input leakage current	I_{IN}			100	nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}	10			MΩ	
3	Input offset voltage	V_{OS}			25	mV	
4	Power supply rejection	PSRR	50			dB	1 kHz
5	Common mode rejection	CMRR	40			dB	0.75 V ≤ V_{IN} ≤ 4.25 V biased at V_{Ref}=2.5 V
6	DC open loop voltage gain	A_{VOL}	32			dB	
7	Unity gain bandwidth	f_C	0.30			MHz	
8	Output voltage swing	V_O	4.0			V_{pp}	Load ≥ 100 kΩ to V_{SS} @ GS
9	Maximum capacitive load (GS)	C_L			100	pF	
10	Resistive load (GS)	R_L			50	kΩ	
11	Common mode range	V_{CM}	2.5			V_{pp}	No Load

MT8870D AC Electrical Characteristics - V_{DD}=5.0V ±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C , using Test Circuit shown in Figure 10.

	Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	Valid input signal levels (each tone of composite signal)		-29		+1	dBm	1,2,3,5,6,9
			27.5		869	mV_{RMS}	1,2,3,5,6,9
2	Negative twist accept				8	dB	2,3,6,9,12
3	Positive twist accept				8	dB	2,3,6,9,12
4	Frequency deviation accept		±1.5% ± 2 Hz				2,3,5,9
5	Frequency deviation reject		±3.5%				2,3,5,9
6	Third tone tolerance			-16		dB	2,3,4,5,9,10
7	Noise tolerance			-12		dB	2,3,4,5,7,9,10
8	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

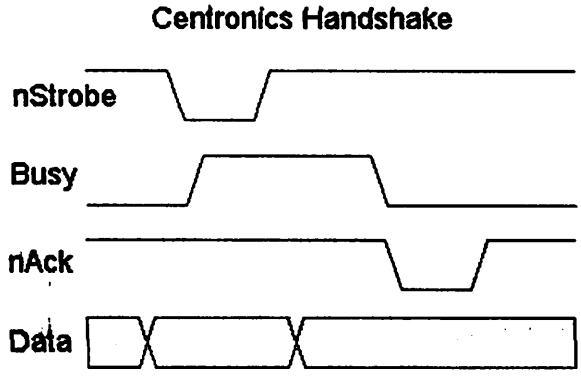
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

*NOTES
1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5 %± 2 Hz.
7. *Bandwidth limited (3 kHz) Gaussian noise.*
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Guaranteed by design and characterization.

Notes:

Centronics?

Centronics is an early standard for transferring data from a host to the printer. The majority of printers use this handshake. This handshake is normally implemented using a Standard Parallel Port under software control. Below is a simplified diagram of the 'Centronics' Protocol.



Data is first applied on the Parallel Port pins 2 to 7. The host then checks to see if the printer is busy. i.e. the busy line should be low. The program then asserts the strobe, waits a minimum of 1µS, and then de-asserts the strobe. Data is normally read by the printer/peripheral on the rising edge of the strobe. The printer will indicate that it is busy processing data via the Busy line. Once the printer has accepted data, it will acknowledge the byte by a negative pulse about 5µS on the nAck line.

Quite often the host will ignore the nAck line to save time. Latter in the Extended Capabilities Port, you will see a Fast Centronics Mode, which lets the hardware do all the handshaking for you. All the programmer must do is write the byte of data to the I/O port. The hardware will check to see if the printer is busy, generate the strobe. Note that this mode commonly doesn't check the nAck either.

Port Addresses

The Parallel Port has three commonly used base addresses. These are listed in table 2, below. The 3BCh base address was originally introduced used for Parallel Ports on early Video Cards. This address then disappeared for a while, when Parallel Ports were later removed from Video Cards. They has now reappeared as an option for Parallel Ports integrated onto motherboards, upon which their configuration can be changed using BIOS.

LPT1 is normally assigned base address 378h, while LPT2 is assigned 278h. However this may not always be the case as explained later. 378h & 278h have always been commonly used for Parallel Ports. The lower case h denotes that it is in hexadecimal. These addresses may change from machine to machine.

The above table, table 3, shows the address at which we can find the Printer Port's addresses in the BIOS Data Area. Each address will take up 2 bytes. The following sample program in C, shows how you can read these locations to obtain the addresses of your printer ports.

```
#include <stdio.h>
#include <dos.h>

void main(void)
{
 unsigned int far *ptraddr;  /* Pointer to location of Port Addresses */
 unsigned int address;       /* Address of Port */
 int a;

 ptraddr=(unsigned int far *)0x00000408;

 for (a = 0; a < 3; a++)
   {
    address = *ptraddr;
    if (address == 0)
          printf("No port found for LPT%d \n",a+1);
    else
          printf("Address assigned to LPT%d is %Xh\n",a+1,address);
    *ptraddr++;
   }
}
```

Software Registers - Standard Parallel Port (SPP)

Offset	Name	Read/Write	Bit No.	Properties
Base + 0	Data Port	Write (Note-1)	Bit 7	Data 7 (Pin 9)
			Bit 6	Data 6 (Pin 8)
			Bit 5	Data 5 (Pin 7)
			Bit 4	Data 4 (Pin 6)
			Bit 3	Data 3 (Pin 5)
			Bit 2	Data 2 (Pin 4)
			Bit 1	Data 1 (Pin 3)
			Bit 0	Data 0 (Pin 2)

Table 4 Data Port

Note 1 : If the Port is bi-directional then Read and Write Operations can be performed on the Data Register.

The base address, usually called the Data Port or Data Register is simply used for outputting data on the Parallel Port's data lines (Pins 2-9). This register is normally a write only port. If you read from the port, you should get the last byte sent. However if your port is bi-directional, you can receive data on this address. See *Bi-directional Ports* for more detail.

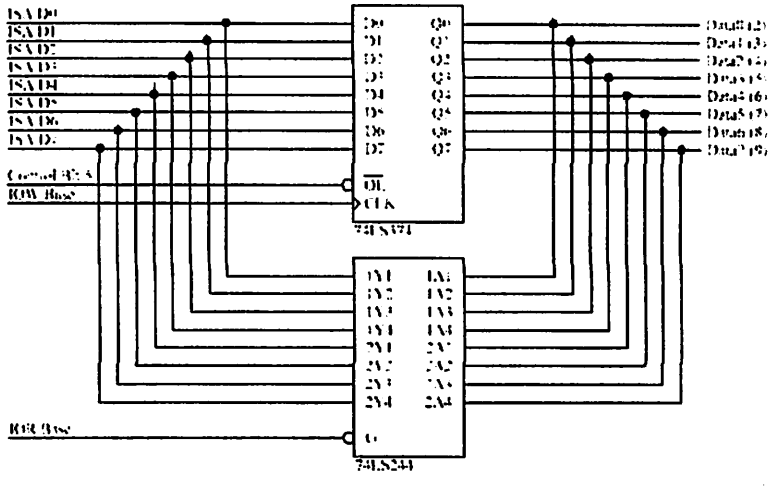
An external 4.7k resistor can be used to pull the pin high. I wouldn't use anything lower, just in case you do have an internal pull up resistor, as the external resistor would act in parallel giving effectively, a lower value pull up resistor. When in high impedance state the pin on the Parallel Port is high (+5v). When in this state, your external device can pull the pin low and have the control port change read a different value. This way the 4 pins of the Control Port can be used for bi-directional data transfer. However the Control Port must be set to xxxx0100 to be able to read data, that is all pins to be +5v at the port so that you can pull it down to GND (logic 0).

Bits 4 & 5 are internal controls. Bit four will enable the IRQ *(See Using the Parallel Ports IRQ)* and Bit 5 will enable the bi-directional port meaning that you can input 8 bits using (DATA0-7). This mode is only possible if your card supports it. Bits 6 & 7 are reserved. Any writes to these two bits will be ignored.

Bi-directional Ports

The schematic diagram below, shows a simplified view of the Parallel Port's Data Register. The original Parallel Port card's implemented 74LS logic. These days all this is crammed into one ASIC, but the theory of operation is still the same.

Standard Parallel Port Bi-Directional Operation



The non bi-directional ports were manufactured with the 74LS374's output enable tied permanent low, thus the data port is always output only. When you read the Parallel Port's data register, the data comes from the 74LS374 which is also connected to the data pins. Now if you can overdrive the '374 you can effectively have a Bi-directional Port. *(or a input only port, once you blow up the latches output!)*

What is very concerning is that people have actually done this. I've seen one circuit, a scope connected to the Parallel Port distributed on the Internet. The author uses an ADC of some type, but finds the ADC requires transistors on each data line, to make it work! No wonder why. Others have had similar trouble, the 68HC11 cannot sink enough current (30 to 40mA!)

then it may be unnecessary. If however you don't bother and your device is connected to the Parallel Port before your software has a chance to initialize then you may encounter problems.

Another problem to be aware of is the pull up resistors on the control port. The average pull-up resistor is 4.7k. In order to pull the line low, your device will need to sink 1mA, which some low powered devices may struggle to do. Now what happens if I suggest that some ports have 1K pull up resistors? Yes, there are such cards. Your device now has to sink 5mA. More reason to use the open collector inverters.

Open collector inverters were chosen over open collector buffers as they are more popular, and thus easier to obtain. There is no reason, however why you can't use them. Another possibility is to use transistors.

The input, D3 is connected via the inverter to Select Printer. Select Printer just happens to be bit 3 of the control port. *D2, D1 & D0* are connected to Init, Auto linefeed and strobe, respectively to make up the lower nibble. Now this is done, all we have to do is assemble the byte using software. The first thing we must do is to write xxxx0100 to the Control Port. This places all the control port lines high, so they can be pulled down to input data.

```
outportb(CONTROL, inportb(CONTROL) & 0xF0 | 0x04);
```

Now that this is done, we can read the most significant nibble. This just happens to be the most significant nibble of the status port. As we are only interested in the MSnibble we will AND the results with 0xF0, so that the LSnibble is clear. Busy is hardware inverted, but we won't worry about it now. Once the two bytes are constructed, we can kill two birds with one stone by toggling Busy and Init at the same time.

```
a = (inportb(STATUS) & 0xF0); /* Read MSnibble */
```

We can now read the LSnibble. This just happens to be LSnibble of the control port - How convenient! This time we are not interested with the MSnibble of the port, thus we AND the result with 0x0F to clear the MSnibble. Once this is done, it is time to combine the two bytes together. This is done by OR'ing the two bytes. This now leaves us with one byte, however we are not finished yet. Bits 2 and 7 are inverted. This is overcome by XOR'ing the byte with 0x84, which toggles the two bits.

```
a = a |(inportb(CONTROL) & 0x0F); /* Read LSnibble */

a = a ^ 0x84; /* Toggle Bit 2 & 7 */
```

Note: Some control ports are not open collector, but have totem pole outputs. This is also the case with EPP and ECP Ports. Normally when you place a Parallel Port in ECP or EPP mode, the control port becomes totem pole outputs only. Now what happens if you connect your *device to the Parallel Port in this mode? Therefore, in the interest of portability I* recommend using the next circuit, reading a nibble at a time.

```
outportb(CONTROL, inportb(CONTROL) & 0xFE); /* Select High Nibble (B)*/
a = a |(inportb(STATUS) & 0xF0); /* Read High Nibble */
byte = byte ^ 0x88;
```

The last line toggles two inverted bits which were read in on the Busy line. It may be necessary to add delays in the process, if the incorrect results are being returned.

Using the Parallel Port's IRQ

The Parallel Port's interrupt request is not used for printing under DOS or Windows. Early versions of OS-2 used them, but don't anymore. Interrupts are good when interfacing monitoring devices such as high temp alarms etc, where you don't know when it is going to be activated. It's more efficient to have an interrupt request rather than have the software poll the ports regularly to see if something has changed. This is even more noticeable if you are using your computer for other tasks, such as with a multitasking operating system.

The Parallel Port's interrupt request is normally IRQ5 or IRQ7 but may be something else if these are in use. It may also be possible that the interrupts are totally disabled on the card, if the card was only used for printing. The Parallel Port interrupt can be disabled and enabled using bit 4 of the control register, *Enable IRQ Via Ack Line.* Once enabled, an interrupt will occur upon a low to high transition (rising edge) of the nACK. However like always, some cards may trigger the interrupt on the high to low transition.

The following code is an Interrupt Polarity Tester, which serves as two things. It will determine which polarity your Parallel Port interrupt is, while also giving you an example for how to use the Parallel Port's Interrupt. It checks if your interrupt is generated on the rising or falling edge of the nACK line. To use the program simply wire **one of** the Data lines (Pins 2 to 9) to the Ack Pin (Pin 10). The easiest way to do this is to bridge some solder from DATA7 (Pin 9) to ACK (Pin 10) on a male DB25 connector.

```
/*  Parallel Port Interrupt Polarity Tester                    */
/*  2nd February 1998                                          */
/*  Copyright 1997 Craig Peacock                               */
/*  WWW     - http://www.senet.com.au/~cpeacock                */
/*  Email   - cpeacock@senet.com.au                            */

#include <dos.h>

#define PORTADDRESS 0x378  /* Enter Your Port Address Here */
#define IRQ 7              /* IRQ Here */

#define DATA PORTADDRESS+0
#define STATUS PORTADDRESS+1
#define CONTROL PORTADDRESS+2

#define PIC1 0x20
#define PIC2 0xA0

int interflag; /* Interrupt Flag */
int picaddr;   /* Programmable Interrupt Controller (PIC) Base Address */
```

```
void interrupt (*oldhandler)();

void interrupt parisr()  /* Interrupt Service Routine (ISR) */
{
  interflag = 1;
  outportb(picaddr,0x20); /* End of Interrupt (EOI) */
}

void main(void)
{
 int c;
 int intno;    /* Interrupt Vector Number */
 int picmask;  /* PIC's Mask */

 /* Calculate Interrupt Vector, PIC Addr & Mask. */

 if (IRQ >= 2 && IRQ <= 7) {
                            intno = IRQ + 0x08;
                            picaddr = PIC1;
                            picmask = 1;
                            picmask = picmask << IRQ;
                           }
 if (IRQ >= 8 && IRQ <= 15) {
                             intno = IRQ + 0x68;
                             picaddr = PIC2;
                             picmask = 1;
                             picmask = picmask << (IRQ-8);
                            }
 if (IRQ < 2 || IRQ > 15)
      {
       printf("IRQ Out of Range\n");
       exit();
      }

 outportb(CONTROL, inportb(CONTROL) & 0xDF); /* Make sure port is in Forward Direction */
 outportb(DATA,0xFF);
 oldhandler = getvect(intno); /* Save Old Interrupt Vector */
 setvect(intno, parisr);      /* Set New Interrupt Vector Entry */
 outportb(picaddr+1,inportb(picaddr+1) & (0xFF - picmask)); /* Un-Mask Pic */
 outportb(CONTROL, inportb(CONTROL) | 0x10); /* Enable Parallel Port IRQ's */

 clrscr();
 printf("Parallel Port Interrupt Polarity Tester\n");
 printf("IRQ %d : INTNO %02X : PIC Addr 0x%X : Mask 0x%02X\n",IRQ,intno,picaddr,picmask);
 interflag = 0; /* Reset Interrupt Flag */
 delay(10);
 outportb(DATA,0x00); /* High to Low Transition */
 delay(10);           /* Wait */
 if (interflag == 1) printf("Interrupts Occur on High to Low Transition of ACK.\n");
 else
   {
    outportb(DATA,0xFF); /* Low to High Transition */
    delay(10);           /* wait */
    if (interflag == 1) printf("Interrupts Occur on Low to High Transition of ACK.\n");
    else printf("No Interrupt Activity Occurred. \nCheck IRQ Number, Port Address "
                "and Wiring.");
    }

 outportb(CONTROL, inportb(CONTROL) & 0xEF); /* Disable Parallel Port IRQ's */
 outportb(picaddr+1,inportb(picaddr+1) | picmask); /* Mask Pic */
 setvect(intno, oldhandler); /* Restore old Interrupt Vector Before Exit */
}
```

Bit	Function	
7:5	*Selects Current Mode of Operation*	
	000	Standard Mode
	001	Byte Mode
	010	Parallel Port FIFO Mode
	011	ECP FIFO Mode
	100	EPP Mode
	101	Reserved
	110	FIFO Test Mode
	111	Configuration Mode
4	ECP Interrupt Bit	
3	DMA Enable Bit	
2	ECP Service Bit	
1	FIFO Full	
0	FIFO Empty	

Table 7 ECR - Extended Control Register

The table above is of the Extended Control Register. We are only interested in the three MSB of the Extended Control Register which selects the mode of operation. There are 7 possible modes of operation, but not all ports will support all modes. The EPP mode is one such example, not being available on some ports.

Modes of Operation

Standard mode — Selecting this mode will cause the ECP port to behave as a Standard Parallel Port, without bi-directional functionality.

Byte Mode / PS/2 mode — Behaves as a SPP in bi-directional mode. Bit 5 will place the port in reverse mode.

Parallel Port FIFO mode — In this mode, any data written to the Data FIFO will be sent to the peripheral using the SPP Handshake. The hardware will generate the handshaking required. Useful with non-ECP devices such as printers. You can have some of the features of ECP like FIFO buffers and hardware generation of handshaking but with the existing SPP handshake (Centronics) instead of the ECP Handshake.

ECP FIFO mode — Standard mode for ECP use. This mode uses the ECP Handshake described in *Interfacing the Extended Capabilities Port*[3]

When in ECP Mode though BIOS, and the ECR register is set to ECP FIFO Mode (011), the SPP registers may disappear.

EPP mode/*Reserved* — This will enable EPP Mode, if available. Under BIOS, if *ECP mode* is set then it's more than likely, this mode is not an option. However if BIOS is set to *ECP and EPP1.x Mode*, then EPP 1.x will be enabled.

Under Microsoft's Extended Capabilities Port Protocol and ISA Interface Standard this mode is Vendor Specified.