PERANCANGAN DAN PEMBUATAN ALAT SPEKTRUM AUDIO DISPLAY10 BAND BERBASIS SWITHCED CAPASITOR FILTER (MF 10) DIKONTROL MIKROKONTROLLER AVR ATMEL ATMEGA 8

SKRIPSI

Disusun Oleh:

ARY PRASOJO
01.17.071

KONSENTRASI TEKNIK ELEKTRONIKA
JURUSAN TEKNIK ELEKTRO S-1
FAKULTAS TEKNOLOGI INDUSTRI
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MEI 2009

LEMBAR PERSETUJUAN

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Disusun Untuk Melengkapi Dan Memenuhi Syarat
Guna Mencapai Gelar Sarjana Teknik

Disusun Oleh:
ARY PRASOJO
NIM: 01.17.071

Mengetahui,	Menyetujui
Ketua Jurusan Teknik Elektro	Dosen Pembimbing
Ir. F. Yudi Limpraptono, MT	Ir. Yudi Limpraptono, MT.
NIP. Y. 103 9500 274	NIP. Y. 103 9500 274

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ABSTRAKSI

Ary Prasojo, 01.17.071 "Perancangan dan Pembuatan Alat Spektrum Audio 10 Band Berbasis Switched Capasitor Filter (Mf 10) Dicontrol Microcontroller Atmel Avr Atmega 8 ", Skripsi Jurusan Teknik Elektro S1, Konsentrasi Teknik Elektronika S1 Institut Teknologi Nasional Malang,

Dosen Pembimbing : Ir. F. Yudi Limpraptono, MT

Kata Kunci : Spektrum Audio 10 Band, Switched Capasitor Filter (Mf 10), Microcontroller Atmel Avr Atmega 8,

Spektrum Audio 10 Band merupakan sistem yang digunakan untuk mengatur ketepatan dari proses yang telah dilakukan supaya dapat diketahui nilai keluaran dari sistem kerja sehingga dapat diketahui band berada pada penempatan yang tepat..

Dengan adanya sistem penempatan jalur band dengan menggunakan Switched Capasitor Filter (Mf 10) dicontrol Microcontroller Atmel AVR Atmega 8 maka dengan mudah dapat diketahui apabila terjadi penyimpangan keluaran dari proses yang telah dijalankan.

Skripsi ini menjelaskan tentang sistem penempatan band yang menggunakan Led Array sebagai tampilan keluaran sehingga dengan mudah dapat diketahui dengan cepat dan tepat hasil dari sistem yang telah berjalan.

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Atas nama Yesus sebagai Tuhanku yang senantiasa memberikan karunia dalam setiap langkah dan waktu mengiringi skripsi ini dapat terselesaikan dengan baik, yang diajukan sebagai syarat untuk menyelesaikan studi di Fakultas Teknologi Industri Jurusan Teknik Eektro Konsentrasi Elektronika, Institut Teknologi Nasional Malang.

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Malang, April 2009

Penulis

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BAB I
PENDAHULUAN

1.1. Latar Belakang.

Seiring dengan perkembangan pembangunan, teknologi elektronika mengalami kemajuan yang sangat pesat, menyebabkan manusia tidak akan lepas dari penggunaan berbagai macam peralatan elektronika yang ada, baik itu penggunaan peralatan yang berupa perangkat keras maupun perangkat lunak elektronika.

Perkembangan teknologi dibidang elektronika telah membawa perubahan dan kemajuan yang begitu cepat dan canggih. Kebutuhan akan produk-produk elektronika juga semakin meningkat. Bahkan bagi sebagian konsumen produk-produk elektronika tersebut telah menjadi kebutuhan primer. Dari sekian banyak produk elektronika yang tersebar di pasaran, salah satu yang paling diminati adalah perangkat audio.

Dampak perkembangan teknologi pada bidang elektronika telah banyak membawa perubahan dan kemajuan yang begitu cepat dan canggih terhadap segi kehidupan manusia. Pesatnya perkembangan teknologi menghasilkan berbagai terobosan dan penemuan baru di bidang pengontrolan.

Dalam perkembangannya, mikrokontroller dan Personal Computer (PC) banyak diterapkan dalam perancangan elektronika, karena Mikrokontroller dan Personal Computer mampu melakukan proses pengontrolan dan proses pengaturan system secara otomatis. Efektifitas Mikrokontroller dan PC inilah yang diperlukan manusia dalam menunjang rutinitas, baik dalam proses produksi pada industri untuk keperluan suatu pelayanan terhadap komunitas masyarakat, maupun dalam kehidupan sehari- hari.Saat ini penggunaan Mikrokontrollerdan PC telah dipacu penggunaanya untuk melayani kepentingan masyarakat.

Pada saat ini banyak piranti audio yang berada dipasaran pada umumnya tidak bertahan lama. Hal ini dikarenakan banyak faktor yang mempengaruhi, antara lain penggunaan komponen bermutu rendah dan sering terjadi loos control yang mengakibatkan komponen kelebihan beban sehingga mengakibatkan kerusakan pada piranti elektronika tersebut.

Dengan latar belakang tersebut diatas, maka penulis berkeinginan untuk lebih mempermudah dengan cara otomatisasi dengan memadukan Switched Capasitor Filter (Mf 10) yang Dicontrol Microcontroller Atmel AVR Atmega 8 sebagai piranti utama, diaplikasikan dengan Pony Prog 2000 sebagai downloader dan bahasa assembly Code Vision AVR, dimana akan mengolah input yang berupa arus untuk dirubah menjadi audio dan ketepatan jalur.

1.2. Rumusan Masalah.

Dengan latar belakang yang telah dikemukakan diatas, maka perlu dirumuskan dalam membuat Spektrum Audio 10 Band Berbasis Switched Capasitor Filter (Mf 10) Dicontrol Microcontroller Atmel Avr Atmega 8 yaitu:

1. Bagaimana merancang suatu peralatan yang dapat dipergunakan untuk menunjukkan ketepatan jalur yang digunakan.
2. Bagaimana membuat suatu sistem komunikasi dengan menggunakan Pony Prog 2000 dan mikrokontroller Atmel Avr Atmega 8.
3. Bagaimana merancang dan membuat rangkaian yang menunjang kerja sistem.
4. Bagaimana merancang software dengan menggunakan bahasa pemrograman Mikrokontroller
5. Bagaimana merancang software dengan menggunakan bahasa pemrograman Code Vision AVR untuk mengirimkan data menuju ke mikrokontroller maupun menerima aliran data dari Mikrokontroller.

Oleh karena itu dalam penulisan skripsi ini saya mencoba untuk merancang dan membuat suatu alat yang diberi judul :

" Perancangan Dan Pembuatan Alat Spektrum Audio Display 10 Band Berbasis Switched Capasitor Filter (Mf 10) Dikontrol Microcontroller AVR ATMEL Atmega 8 ".

1.3. Tujuan.

Adapun tujuan dari perancangan dan pembuatan alat ini adalah untuk menciptakan suatu alat pengatur ketepatan jalur pada piranti elektronika dengan berbasiskan switched kapasitor filter MF 10 berbasiskan mikrokontroller ATMEL AVR Atmega 8.

1.4. Batasan Masalah.

Dalam perancangan dan pembuatan alat Spektrum Audio ini perlu diberikan suatu ruang lingkup pembahasan agar tercapai tujuan yang diinginkan, sehingga perlu kiranya diberikan batasan- batasan, antara lain :

1. Pembahasan skripsi ini dititik beratkan pada sistem untuk menunjukan ketepatan jalur.
2. Mikrokontroler yang digunakan adalah ATMEL AVR Atmega 8.
3. Tidak membahas bagaimana sampling rate dibuat.
4. Tidak membahas rangkaian filter secara detail.
5. Pada skripsi ini tentang system catu daya tidak dibahas.

1.5. Metodologi.

Metodologi yang digunakan dalam penyusunan tugas akhir ini adalah sebagai berikut:

1. Study literature, meliputi:

   Melakukan kajian buku, majalah atau hasil penelitian di laboraturium.

2. Perencanaan tiap blok diagram

   Perencaan yang dilakukan berhubungan dengan prinsip kerja alat yang akan digunakan, kemudian komponen yang dipakai dilakukan penggabungan masing-masing blok yang telah disusun.

3. Pengujian alat

   Pengujian alat dilakukan perbloksystem dan keseluruhan system yang telah disusun sehngga disimpulkan suatu efektifitas penggunaan suatu alat.

4. Penyusunan Laporan Skripsi

   Menyusun data laporan berpedoman pada alat yang selesai dibuat beserta kesimpulan cara kerja dari alat tersebut.

1.6. Sistematika Penulisan.

Pembahasan laporan skripsi ini akan diuraiakan dan dijabarkan dalam setiap bab, dengan pembagian sebagai berikut:

BAB I : PENDAHULUAN

Terdiri dari latar belakang, rumusan masalah, batasan masalah, tujuan, metodologi, dan sistematika penulisan.

BAB II : LANDASAN TEORI

Membahas teori-teori yang mendukung dan menunjang perencanaan dan membuat alat yang digunakan.

BAB III : PERENCANAAN DAN PEMBUATAN ALAT

Berisi tentang proses perencanaan dan pembuatan sistem pembayaran pemakaian jasa internet di warnet.

BAB IV : PENGUJIAN ALAT

Berisi tentang pengujian terhadap alat yang dibuat.

BAB V : PENUTUP

Memuat tentang kesimpulan-kesimpulan yang diperoleh dari hasil pembuatan laporan skripsi ini serta saran untuk pengembangan lebih lanjut.

BAB II
LANDASAN TEORI

2.1. Umum.

Pada bagian ini akan dibahas teori penunjang untuk peralatan yang akan dirancang yaitu teori dasar Switched Kapasitor Filter (MF 10), teori dasar Mikrokontroller ATMEL AVR Atmega 8, teori dasar Transistor Switch sebagai saklar otomatis dan tampilan keluaran (LED Array).

2.2. Sistem Spektrum Audio Display 10 Band.

Sistem Spektrum Audio Display 10 Band adalah sistem penempatan jalur frekuensi yang digunakan dan disesuaikan dengan kapasitas jalur frekuensi dimana akan bekerja dari frekuensi 70 Hz hingga 16 KHz. Sistem penempatan jalur ini digunakan untuk menunjang proses kerja frekuensi dalam penempatanya yang digunakan dalam piranti elektronika audio yang menggunakan jalur frekuensi berbeda seperti, Operasional Amplifier, Radio Pemancar, dan lainnya. Secara umum fungsi utama dari Spektrum Audio Display 10 Band adalah :

- Mengubah sinyal elektrik yang sebagai masukan untuk dirubah menjadi arus DC yang digunakan untuk mengaktifkan LED Array sebagai tampilan output.
- Sebagai pedoman apabila terjadi penyimpang dalam penempatan jalur, dapat dengan mudah diketahui dikarenakan lebar band with melebihi dan dapat dilihat pada tampilan output.
- Dalam aplikasi untuk digunakan secara umum adalah pada tampilan equalizer pada piranti audio pada umumnya.

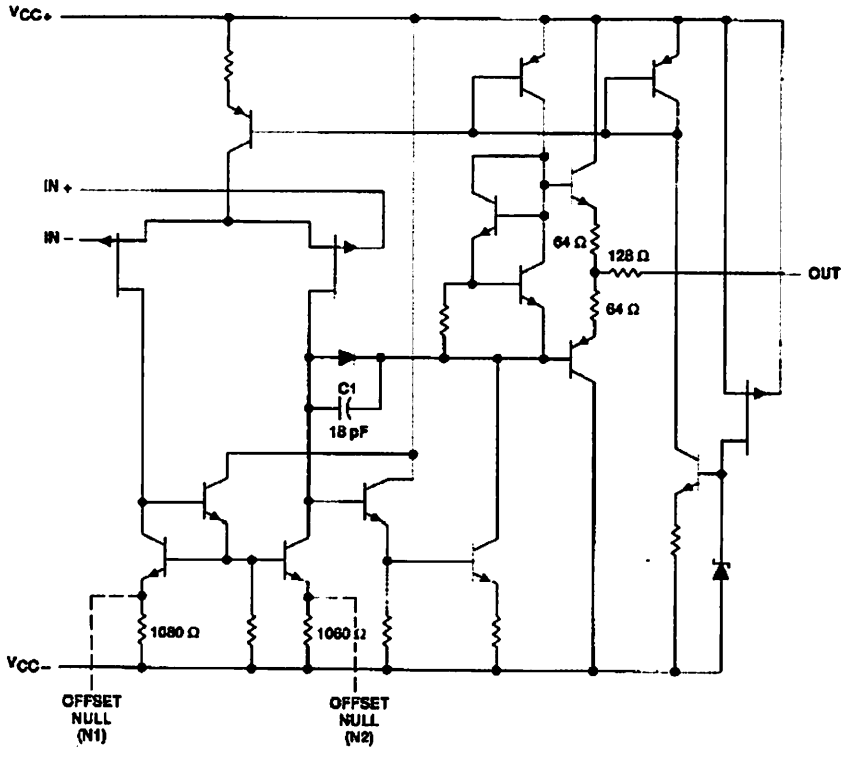
Komponen – Komponen utama dalam sistem Spektrum Audio Display 10 Band untuk melakukan proses dalam aplikasinya adalah : Buffer (NJM4558), Switched Capasitor Filter (MF 10), Mikrokontroller (AVR ATMEL Atmega 8), Transistor Switch

(A733), Serial To Pararel Shift Register (74HC595) dan LED Array (LEDTECH 10 Segment).

2.3. Buffer.

2.3.1. Pengenalan Dasar.

Komponen yang digunakan adalah IC NJM4558 dikarenakan komponen ini memiliki kemampuan untuk diaplikasikan dengan semua jenis filter, juga dapat diposisikan sebagai penguat. Komponen ini memang didesain untuk memiliki noise rendah karena terintregasi dengan bipolar output pada satu monolithic chip.



Gambar 2 - 1. Skematic Block IC NJM4558

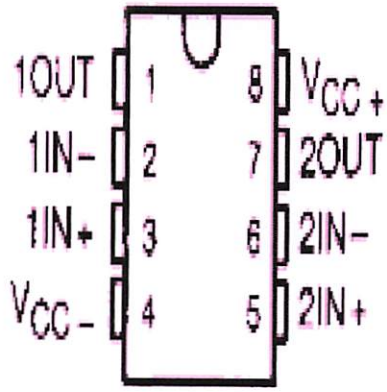
Kelebihan dari komponen ini adalah :

- Penggunaan daya rendah.

- Memiliki mode lebar jalur dan rentan terhadap tegangan diferensial.
- Bias input rendah dan arus offset.
- Dilengkapi pengaman rangkaian pada keluaran.
- Distorsi harmoni total rendah ±0.003% Typ.
- Noise rendah (V_n = 18 nV/ $\sqrt{Hz}$ Typ pada f = 1 KHz.
- Impedansi input tinggi dan daerah masukan JFET.
- Bebas dalam operasi Latch-Up.
- Slew Rate tinggi 13 V.

2.3.2. Konfigurasi Pin Pada IC NJM4558.

Konfigurasi kaki – kaki pada IC NJM4558 terdiri dari 8 pin seperti yang terlihat dibawah ini :



Gambar 2 - 2. Konfigurasi Pin IC NJM 4558.

Adapun fungsi dari tiap pin akan dijelaskan sebagai berikut :

Port 1 : 1OUT. Berfungsi sebagai pintu keluar 1 dari proses.

Port 2 : 1IN-. Berfungsi sebagai pintu masuk untuk arus negatif (-).

Port 3 : 1IN+. Berfungsi sebagai pintu masuk untuk arus positif (+).

Port 4 : VCC(-). Berfungsi sebagai sumber tegangan negative (-).

Port 5 : 2IN(+). Berfungsi sebagai pintu masuk untuk arus positif (+).

Port 6 : 2IN(-). Berfungsi sebagai pintu masuk untuk arus negatif (-).

Port 7 : 2OUT. Berfungsi sebagai pintu keluar dari gabungan kedua input.

Port 8 : VCC+ Berfungsi sebagai sumber tegangan positip (+).

Yang perlu diperhatikan dalam penggunaan komponen ini adalah :

- Semua tegangan rata – rata, kecuali tegangan diferensial memiliki respon dimana VCC_+ dan VCC-.
- Tegangan diferensial adalah IN_+ yang merespon pada IN-

Tabel 2 - 1. Rating Disposisi.

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	660 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
D (14 pin)	680 mW	7.6 mW/°C	60°C	608 mW	494 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	598 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
PW (8 pin)	525 mW	4.2 mW/°C	70°C	525 mW	N/A	N/A
PW (14 pin)	700 mW	5.6 mW/°C	70°C	700 mW	N/A	N/A
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

2.3.3. Karakteristik IC NJM4558.

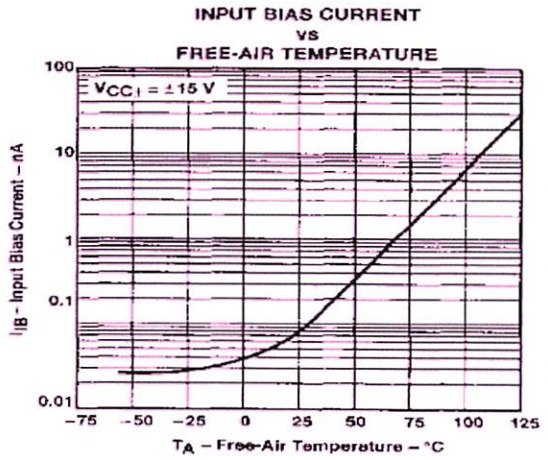
Tabel 2 - 2. Karakteristik IC NJM4558.

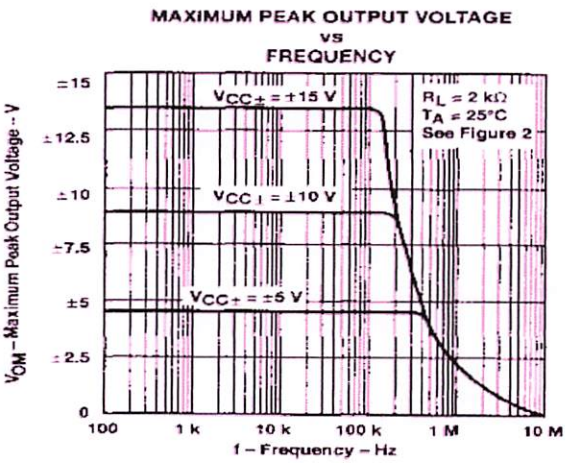
PARAMETER		TEST CONDITIONS†	T_A‡	TL071M TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	Full range		18			18		μV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		5	100		5	100	pA
			Full range			20			20	nA
I_{IB}	Input bias current‡	$V_O = 0$	25°C		65	200		65	200	pA
						50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	±12	±13.5		±12	±13.5		V
		$R_L \geq 10\ k\Omega$	Full range	±12			±12			
		$R_L \geq 2\ k\Omega$		±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2\ k\Omega$	25°C	35	200		35	200		V/mV
				15			15			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	$V_O = 0$, No load	25°C		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120		dB

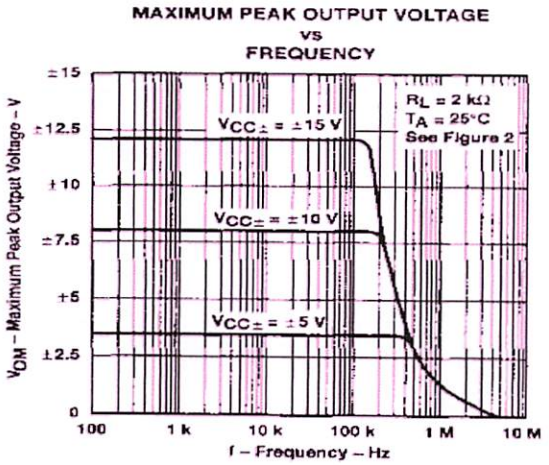
Tabel 2 - 3. Karakteristik operasional.

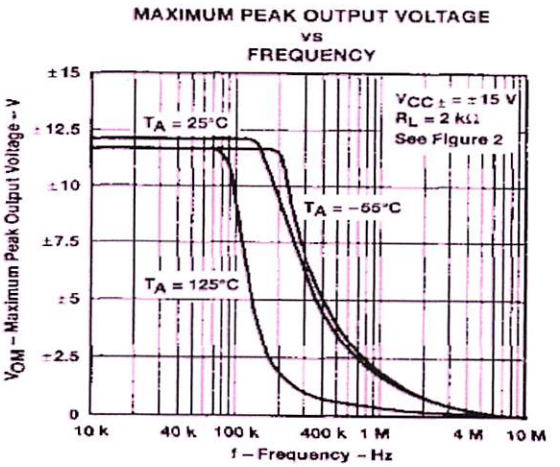
PARAMETER		TEST CONDITIONS		TL07xM			ALL OTHERS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2\ k\Omega$, See Figure 1	5	13		8	13		V/μs
t_r	Rise time overshoot factor	$V_I = 20$ mV, $C_L = 100$ pF,	$R_L = 2\ k\Omega$, See Figure 1		0.1			0.1		μs
					20%			20%		
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		μV
I_n	Equivalent input noise current	$R_S = 20\ \Omega$,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_{O(RMS)} = 10$ V, $R_L \geq 2\ k\Omega$,	$R_S \leq 1\ k\Omega$, f = 1 kHz		0.003%			0.003%		

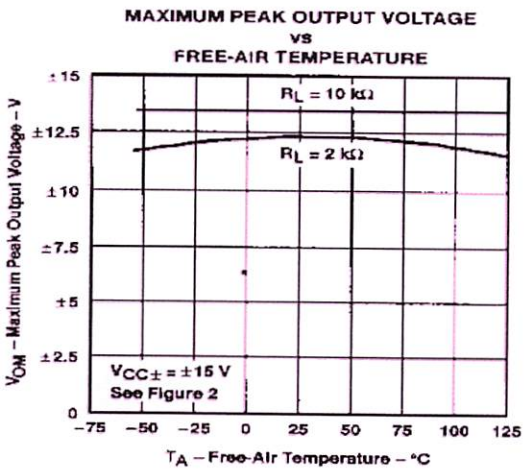
Grafik 2 - 1. Karakteristik IC NJM4558.

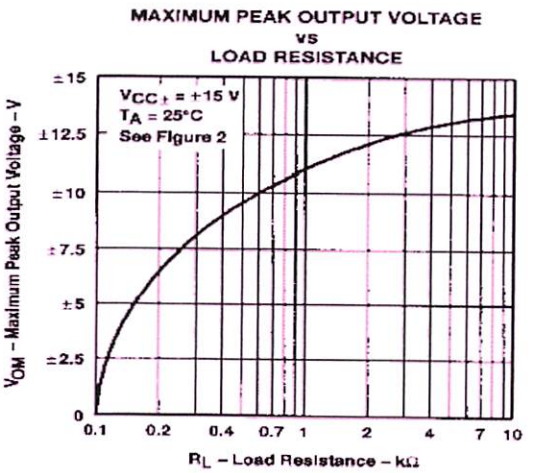


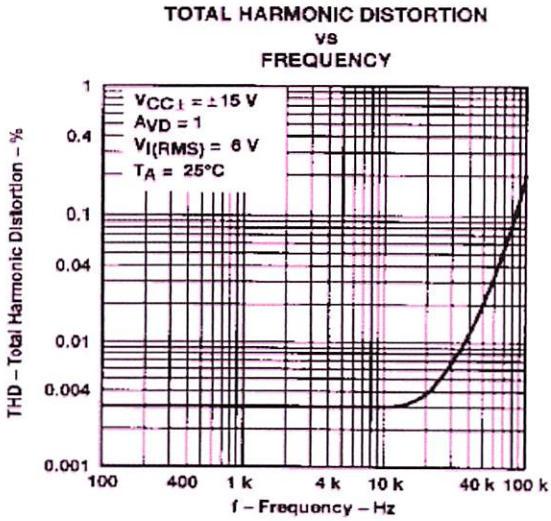


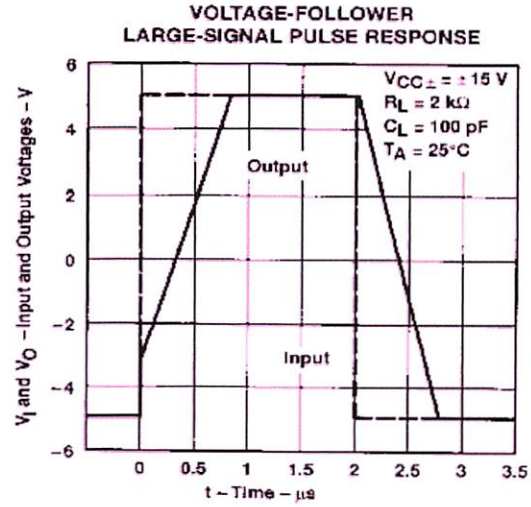


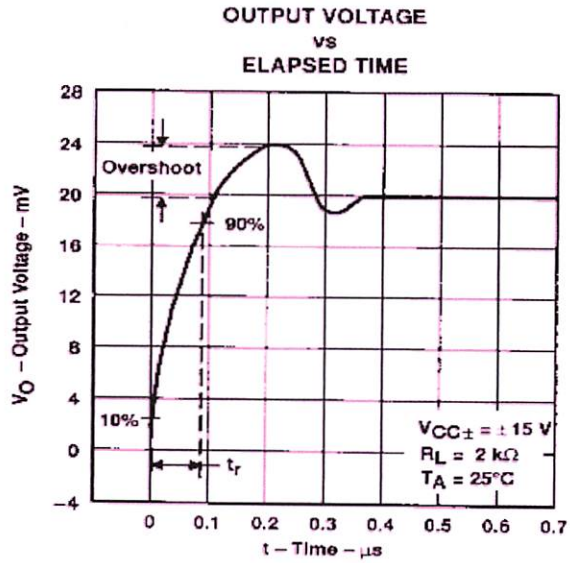












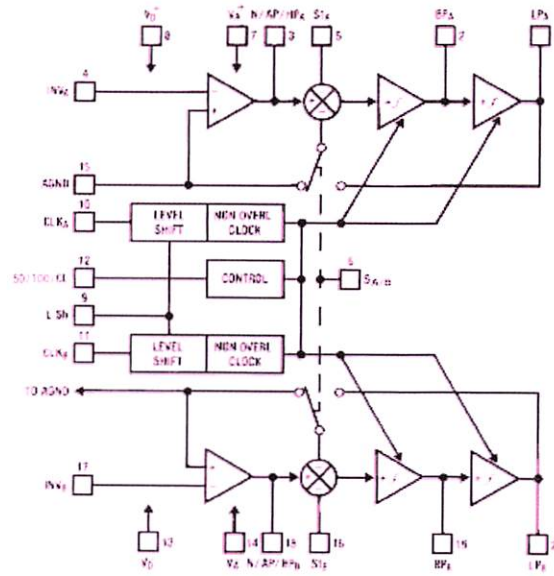
2.4. Switched Kapasitor Filter (MF 10).

2.4.1. Pengenalan Dasar.

Switched Kapasitor Filter (MF 10) merupakan komponen elektronika yang berfungsi sebagai saklar otomatis yang digerakkan secara elektrik dimana terdiri dari

filter yang dapat bersifat aktif dan pasif. Switched Kapasitor Filter (MF 10) dilengkapi dengan beberapa filter, yaitu :

- Low Pass Filter yang hanya meloloskan frekuensi rendah.
- High Pass Filter yang hanya meloloskan frekuensi tinggi.
- Band Pass Filter yang meloloskan frekuensi diantara Low Pass dan High Pass.

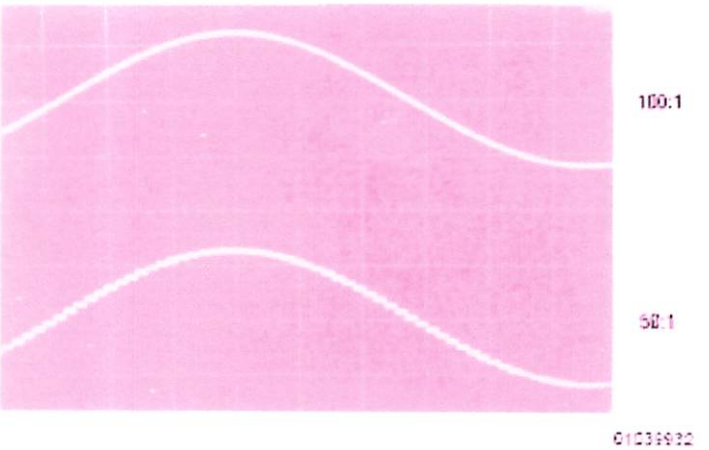


Gambar 2 - 3. Blok Diagram IC MF 10

Keunggulan dari Switched Capasitor Filter (MF 10)

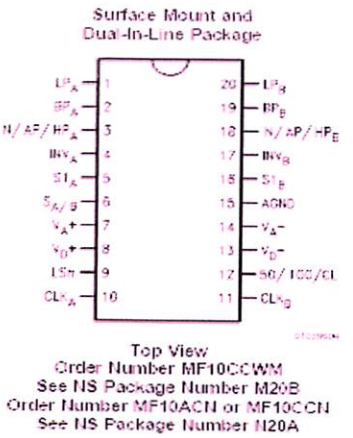
- Mudah dalam Penggunaan.
- Pulsa Akurasi Rasio Frekuensi pusat ± 0,6 %.
- Dalam keadaan diam kualitas pulsa mempertahankan stabilitas frekuensi.
- Sensitifitas rendah dalam penggunaan komponen variatif.
- Mudah diaplikasikan dengan Low Pass Filter, High Pass Filter, dan Band Pass Filter.
- Rentan Frekuensi operasional sampai 30 Khz.

- Fo x Q range maksimum mencapai 200 KHz.
- 20 Pin dengan lebar jalur dalam 0.3 mm.
- Bentuk kemasan yang minimum tapi terdiri 20 Pin.



Gambar 2 - 2. Gelombang Keluaran Sistem Data IC MF 10.

2.4.2. Konfigurasi Pin – Pin IC MF 10 (Switched Kapasitor Filter).



Gambar 2 - 5. Konfigurasi Pin IC MF 10

LP(1,20),BP(2,19),N/AP/HP(3,18). Fungsi ganda dari keluaran Low Pass, Band Pass, dimana arus keluar berkisar 1,5 mA sampai 3 mA dan lebar swing 1 Volt.

INV(4,17). Masukan inverting dari Op-Amp akan menghasilkan impedansi tinggi, tetapi apabila mendapat masukan dari non inverting maka AGND akan menjadikan INV_A dan INV_B menjadi impedansi rendah.

S1(5,16). Sebagai pin dari sinyal masukan yang dapat digunakan untuk segala jenis konfigurasi filter . S1 dapat bekerja apabila mendapat impedansi bias mencapai 1 Ω. Bila S1 tidak bekerja maka sinyal masukan dilangsungkan ke AGND.

$S_{A/B}$ (6). Saklar pin akan aktif bila dihubungkan dengan satu masukan AGND ($S_{A/B}$ kondisi V^-) atau untuk keluaran Low Pass Filter ($S_{A/B}$ kondisi V^+)m Memiliki fleksibilitas dalam konfigurasi filter dan operasi variasi mode.

V_A^-(7),V_D^+(8). Sumber analog positif dan sumber digital positif

CLKA(10), CLKB(11). Mengaktifkan saklar Kapasitor Filter maksimum pada saat op-amp bekerja maksimal pada system.

50/100/CL(12). Jika pada saat akif detak pulsa frekuensi utama 50 : 1, jika pada saat pasif detak pulsa frekuensi utama 100 : 1.

f_{CLK} adalah detak sinyal frekuensi luar yang diaplikasi pada pin 10 atau 11.

f_o adalah frekuensi pusat pada saat mendapat frekuensi maksimum pada saat Band Pass Filter mendapatkan frekuensi maksimum.

f_{notch} adalah kondisi pada saat frekuensi minimum dan pada idealnya f = 0.

F_z akan aktif apabila f_o dan Q_z aktif.

Q adalah faktor kualitas dari semua filter.

Q_z adalah factor kualiatas kedua dari semua pass filter dan nilainya relatife.

Maka persamaan nilai yang diperoleh :

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_O}{Q_Z} + \omega_O^2\right)}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

Q_z adalah kualitas faktor relative untuk semua karakteristik.

Dimana : Q_z = Respons untuk semua Pass.

H_{OBP} = Gain (dalam V/V) pada saat keluaran Band Pass, dimana f = f_o.

H_{OLP} = Gain (dalam V/V) pada saat keluaran Low Pass, dimana f = 0 Hz.

H_{OHP} = Gain (dalam V/V) pada saat keluaran High Pass, dimana f = $f_{CLK}/2$.

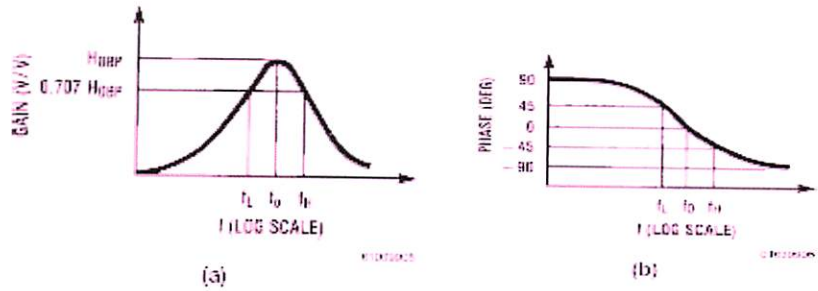
H_{ON} = Gain (dalam V/V) pada saat tidak ada keluaran, dimana f = 0.

$H_{ON\,1}$ = Gain (dalam V/V) pada saat f keluaran 0 Hz.

$H_{ON\,2}$ = Gain (dalam V/V) pada saat f keluaran sama dengan = $f_{CLK}/2$.

f_{notch} adalah frekuensi minimum (Idealnya 0).

f_Z adalah frekuensi pusat yang stabil bila f_o dan Q_Z kondisi High.



Grafik 2 – 2. Order Band Pass Response.

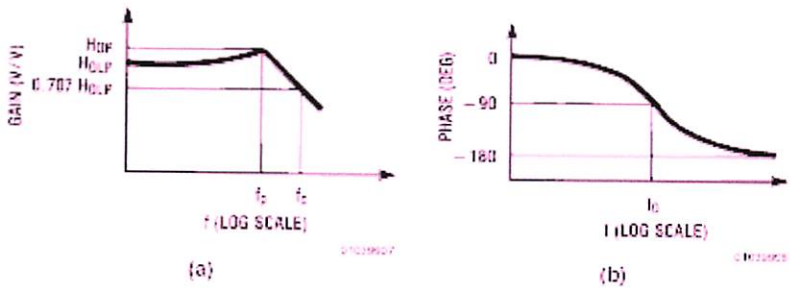
$$H_{BP}(s) = \frac{H_{0BP}\frac{\omega_0}{Q}s}{s^2 + \frac{s\omega_0}{Q} + \omega_0^2}$$

$$Q = \frac{f_0}{f_H - f_L};\ f_0 = \sqrt{f_L f_H}$$

$$f_L = f_0\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_0\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$\omega_0 = 2\pi f_0$$



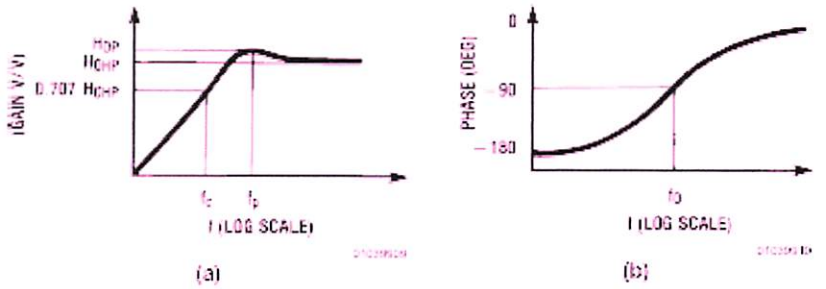
Grafik 2 – 3. Order Low Pass Response.

$$H_{LP}(s) = \frac{H_{0LP}\omega_0^2}{s^2 + \frac{s\omega_0}{Q} + \omega_0^2}$$

$$f_c = f_0\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_0\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{0P} = H_{0LP} \cdot \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$



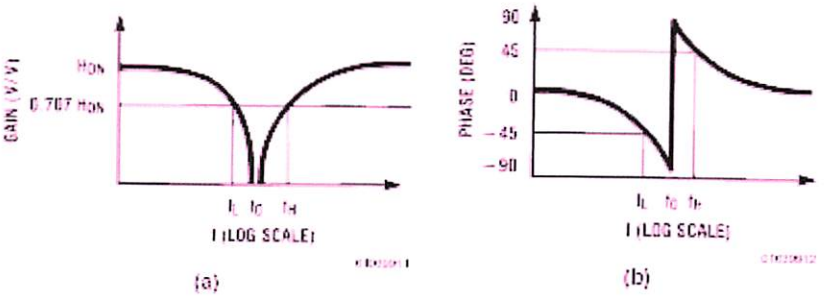
Grafik 2 – 4. Order High Pass Response.

$$H_{HP}(s) = \frac{H_{OHP}s^2}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

$$f_C = f_O \cdot \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_P = f_O \cdot \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \cdot \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$



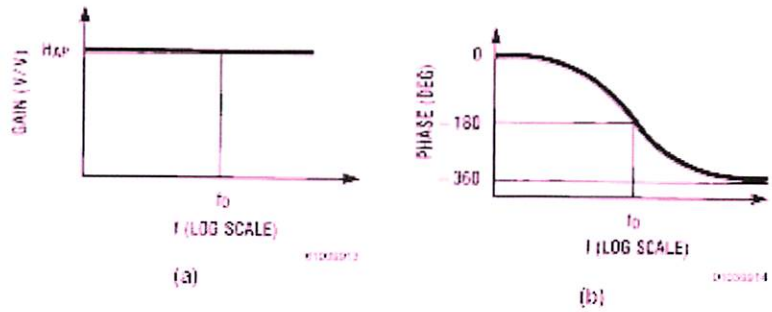
Grafik 2 – 5. Order Notch Response.

$$H_N(s) = \frac{H_{ON}(s^2 + \omega_0^2)}{s^2 + \frac{s\omega_0}{Q} + \omega_0^2}$$

$$Q = \frac{f_0}{f_H - f_L}; \quad f_0 = \sqrt{f_L f_H}$$

$$f_L = f_0\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_0\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$



Grafik 2 —6. Semua Pass Response.

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_0}{Q} + \omega_0^2\right)}{s^2 + \frac{s\omega_0}{Q} + \omega_0^2}$$

2.4.3. Karakteristik IC MF 10 (Switched Kapasitor Filter).

- Tegangan yang digunakan (V^+ - V^-) : 14 Volt.
- Tegangan dalam tiap Pin : V^++ 0,3V

  V^-- 0.3 V
- Arus masukan dalam tiap Pin : 5 mA.
- Arus Masukan : 20 mA.

- Dissipation Power : 500mW.
- Suhu Normal : 150 ° C.
- ESD Susceptabiliti : 2000 V.
- Informasi Soldering

  N Kemasan 10 Detik : 260°C.

  Vapor Phase 60 Detik : 215°C.

  Infrared 15 Detik : 220°C.
- Rating Operasi.

  Suhu Rata – Rata : $T_{Min} \leq T_A \leq T_{Max}$

  MF10ACN, MF10CCN : $0°C \leq T_A \leq 70°c$.

  MF 10CCWM : $0°C \leq T_A \leq 70°c$.

Tabel 2 - 4. Karakteristik Elektrik IC MF 10.

Electrical Characteristics

$V^+ = +5.00V$ and $V^- = -5.00V$ unless otherwise specified. Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions		MF10ACN, MF10CCN, MF10CCWM			Units
					Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$V^+ - V^-$	Supply Voltage	Min					9	V
		Max					14	V
I_S	Maximum Supply Current		Clock Applied to Pins 10 & 11 No Input Signal		6	12	12	mA
f_0	Center Frequency Range	Min	$f_0 \times Q < 200$ kHz		0.1		0.2	Hz
		Max			30		20	kHz
f_{CLK}	Clock Frequency Range	Min			5.0		10	Hz
		Max			1.5		1.0	MHz
f_{CLK}/f_0	50:1 Clock to Center Frequency Ratio Deviation	MF10A	Q = 10 Mode 1	$V_{pin12} = 5V$ $f_{CLK} = 250$ kHz	±0.2	±0.6	±0.6	%
		MF10C			±0.2	±1.5	±1.5	%
f_{CLK}/f_0	100:1 Clock to Center Frequency Ratio Deviation	MF10A	Q = 10 Mode 1	$V_{pin12} = 0V$ $f_{CLK} = 500$ kHz	±0.2	±0.6	±0.6	%
		MF10C			±0.2	±1.5	±1.5	%
	Clock Feedthrough		Q = 10 Mode 1		10			mV
	Q Error (MAX) (Note 4)		Q = 10 Mode 1	$V_{pin12} = 5V$ $f_{CLK} = 250$ kHz	±2	±6	±6	%
				$V_{pin12} = 0V$ $f_{CLK} = 500$ kHz	±2	±6	±6	%
H_{DLP}	DC Lowpass Gain		Mode 1 R1 = R2 = 10k		0	±0.2	±0.2	dB
V_{OS1}	DC Offset Voltage (Note 5)				±5.0	±20	±20	mV
V_{OS2}	DC Offset Voltage	Min	$V_{pin12} = +5V$	$S_{A/B} = V^+$	−150	−165	−185	mV

Electrical Characteristics (Continued)

V^+ = +5.00V and V^- = −5.00V unless otherwise specified. Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter		Conditions		MF10ACN, MF10CCN, MF10CCWM Typical (Note 6)	Tested Limit (Note 9)	Design Limit (Note 10)	Units
	(Note 5)	Max	(f_{CLK}/f_0 = 50)			−65	−65	
		Min	V_{pin12} = +5V (f_{CLK}/f_0 = 50)	$S_{A/B} = V^-$	−70			mV
		Max						
V_{OS2}	DC Offset Voltage (Note 5)	Min	V_{pin12} = +5V (f_{CLK}/f_0 = 50)	All Modes	−70	−100	−100	mV
		Max				−20	−20	
V_{OS2}	DC Offset Voltage (Note 5)		V_{pin12} = 0V (f_{CLK}/f_0 = 100)	$S_{A/B} = V^-$	−300			mV
			V_{pin12} = 0V (f_{CLK}/f_0 = 100)	$S_{A/B} = V^-$	−140			mV
V_{OS2}	DC Offset Voltage (Note 5)		V_{pin12} = 0V (f_{CLK}/f_0 = 100)	All Modes	−140			mV
V_{OUT}	Minimum Output Voltage Swing	BP, LP Pins	R_L = 5k		±4.25	±3.8	±3.8	V
		N/AP/HP Pin	R_L = 3.5k		±4.25	±3.8	±3.8	V
GBW	Op Amp Gain BW Product				2.5			MHz
SR	Op Amp Slew Rate				7			V/µs
	Dynamic Range(Note 6)		V_{pin12} = +5V (f_{CLK}/f_0 = 50)		83			dB
			V_{pin12} = 0V (f_{CLK}/f_0 = 100)		80			dB
I_{SC}	Maximum Output Short Circuit Current (Note 7)	Source			20			mA
		Sink			3.0			mA

Tabel 2 - 5. Karakteristik Logic Elektrik IC MF 10.

Logic Input Characteristics

Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J = 25°C$

Parameter		Conditions	MF10ACN, MF10CCN, MF10CCWM			Units
			Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
CMOS Clock Input Voltage	Min Logical "1"	$V^+ = +5V$, $V^- = -5V$, $V_{LSR} = 0V$		+3.0	+3.0	V
	Max Logical "0"			+3.0	+3.0	V
	Min Logical "1"	$V^+ = +10V$, $V^- = 0V$, $V_{LSR} = +5V$		+8.0	+8.0	V
	Max Logical "0"			+2.0	+2.0	V
TTL Clock Input Voltage	Min Logical "1"	$V^+ = +5V$, $V^- = -5V$, $V_{LSR} = 0V$		+2.0	+2.0	V
	Max Logical "0"			+0.8	+0.8	V

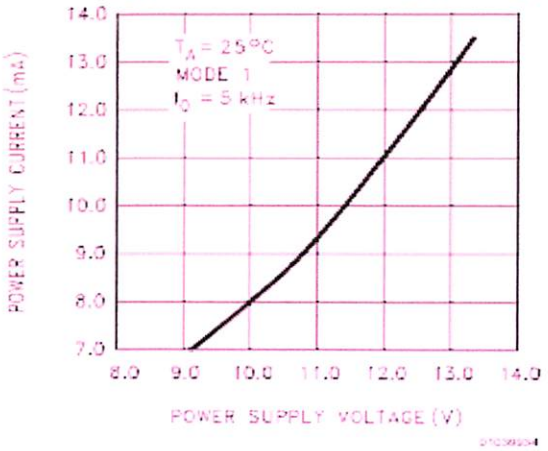
Logic Input Characteristics (Continued)

Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J = 25°C$

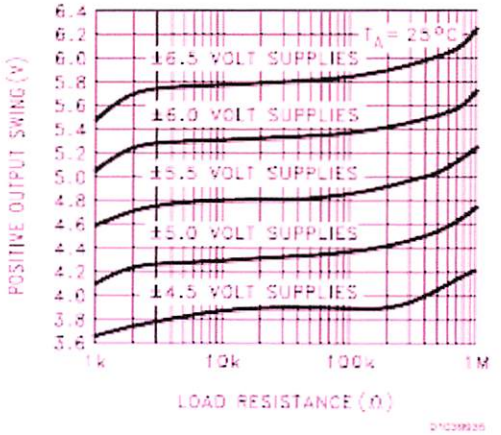
Parameter		Conditions	MF10ACN, MF10CCN, MF10CCWM			Units
			Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
	Min Logical "1"	$V^+ = +10V$, $V^- = 0V$, $V_{LSR} = 0V$		+2.0	+2.0	V
	Max Logical "0"			+0.8	+0.8	V

Grafik 2 - 7. Karakteristik Stabilitas Kondisi IC MF 10.

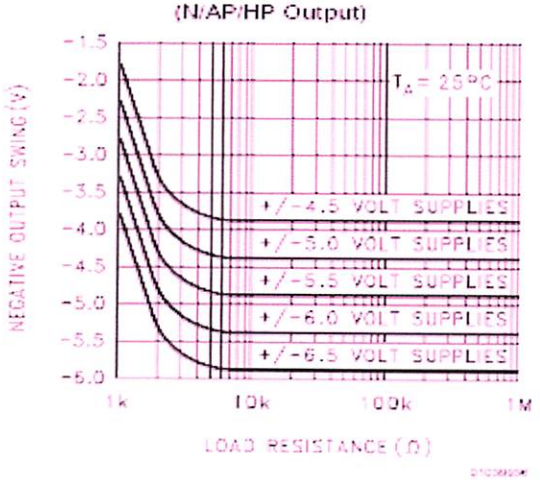
Power Supply Current vs. Power Supply Voltage



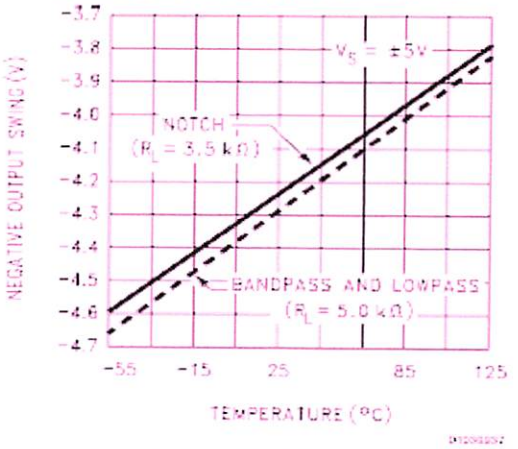
Positive Output Voltage Swing vs. Load Resistance (N/AP/HP Output)



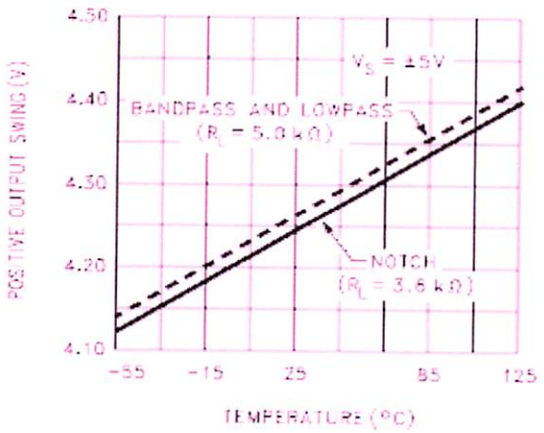
Negative Output Voltage Swing vs. Load Resistance (N/AP/HP Output)



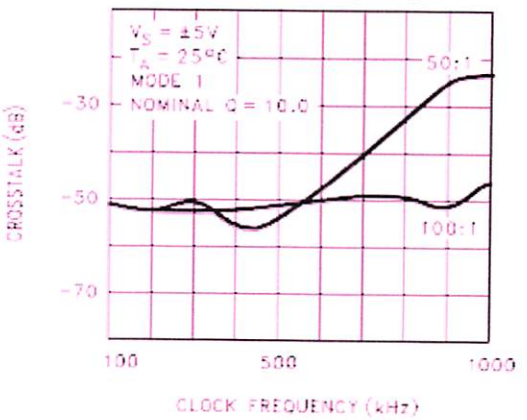
Negative Output Swing vs. Temperature



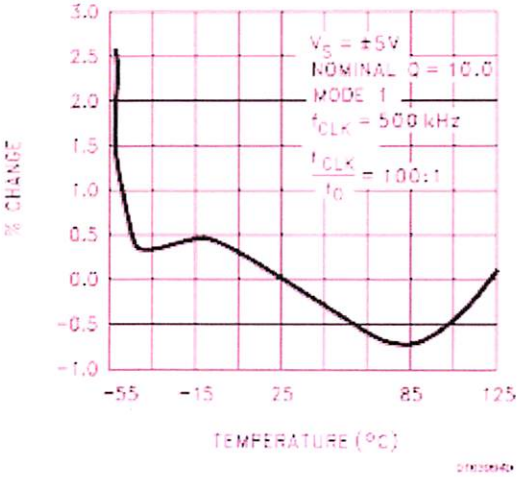
Positive Output Swing vs. Temperature



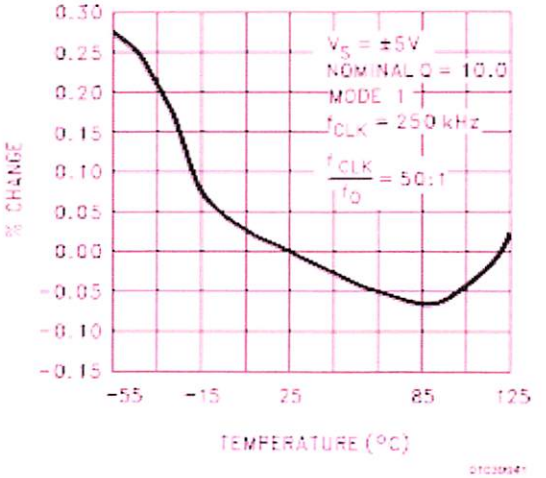
Crosstalk vs. Clock Frequency



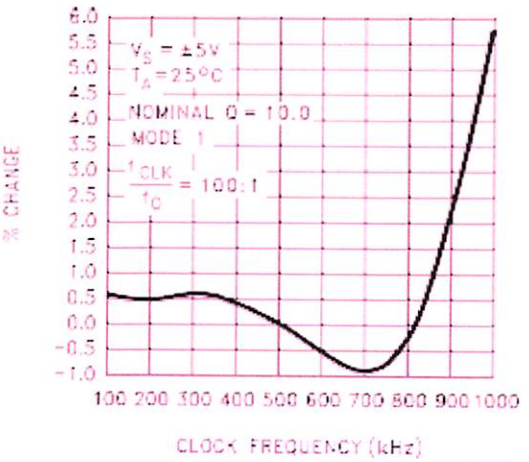
Q Deviation vs. Temperature



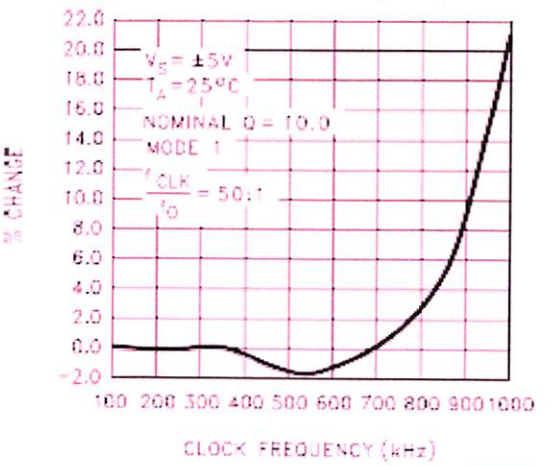
Q Deviation vs. Temperature



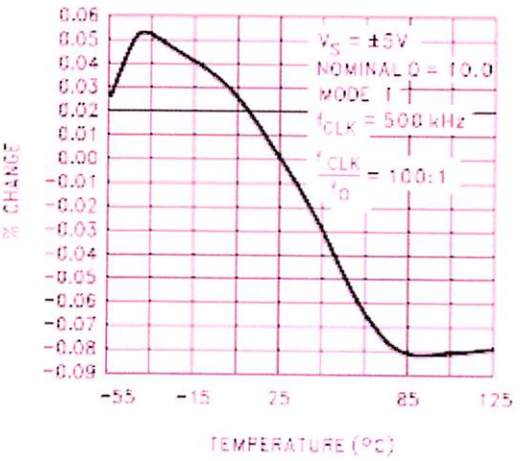
Q Deviation vs. Clock Frequency



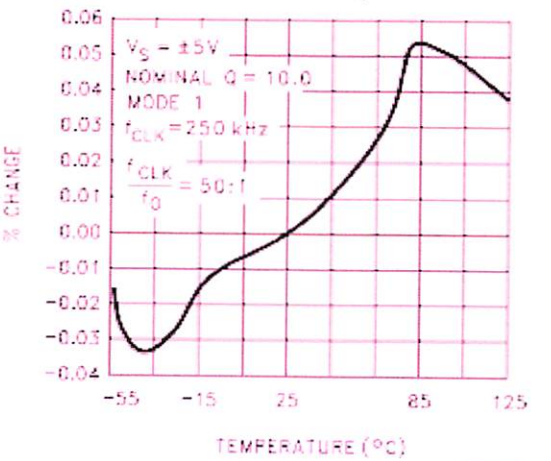
Q Deviation vs. Clock Frequency



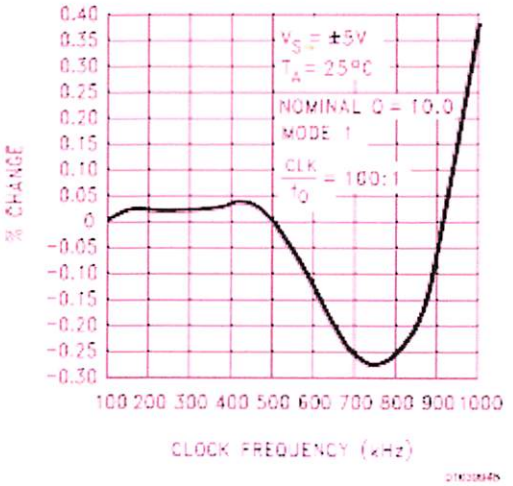
f_{CLK}/f_0 Deviation vs. Temperature



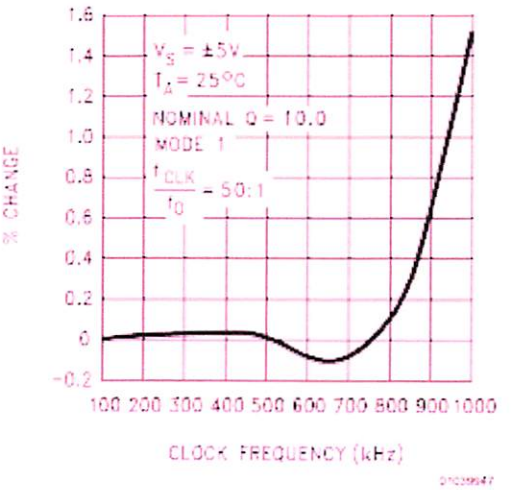
f_{CLK}/f_0 Deviation vs. Temperature



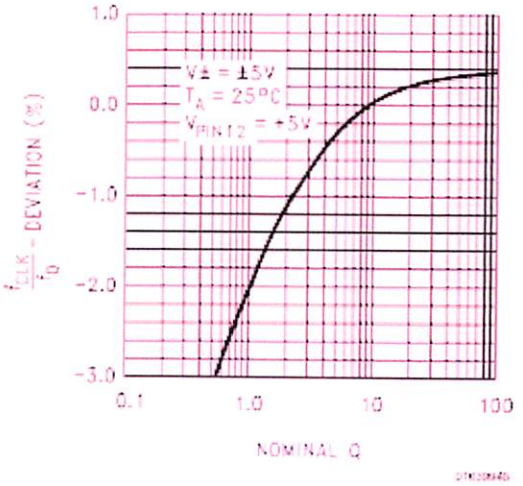
f_{CLK}/f_o Deviation vs. Clock Frequency



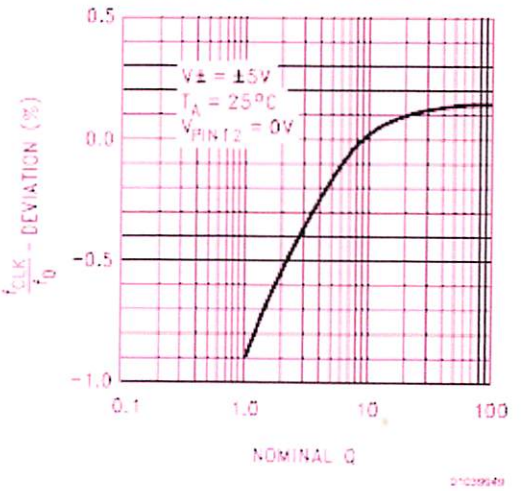
f_{CLK}/f_o Deviation vs. Clock Frequency



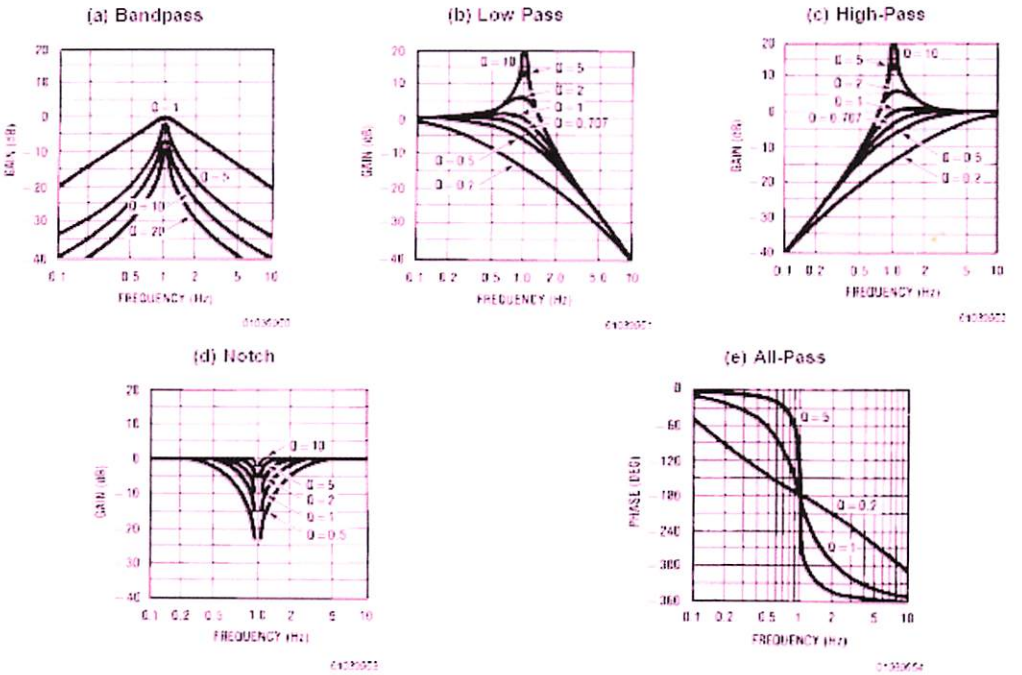
Deviation of f_{CLK}/f_o vs. Nominal Q



Deviation of f_{CLK}/f_o vs. Nominal Q



Grafik 2 - 8. Variasi Response Dari Sistem Kerja Filter atas fungsi Q.



2.5. Mikrokontroller ATMEL AVR Atmega 8.

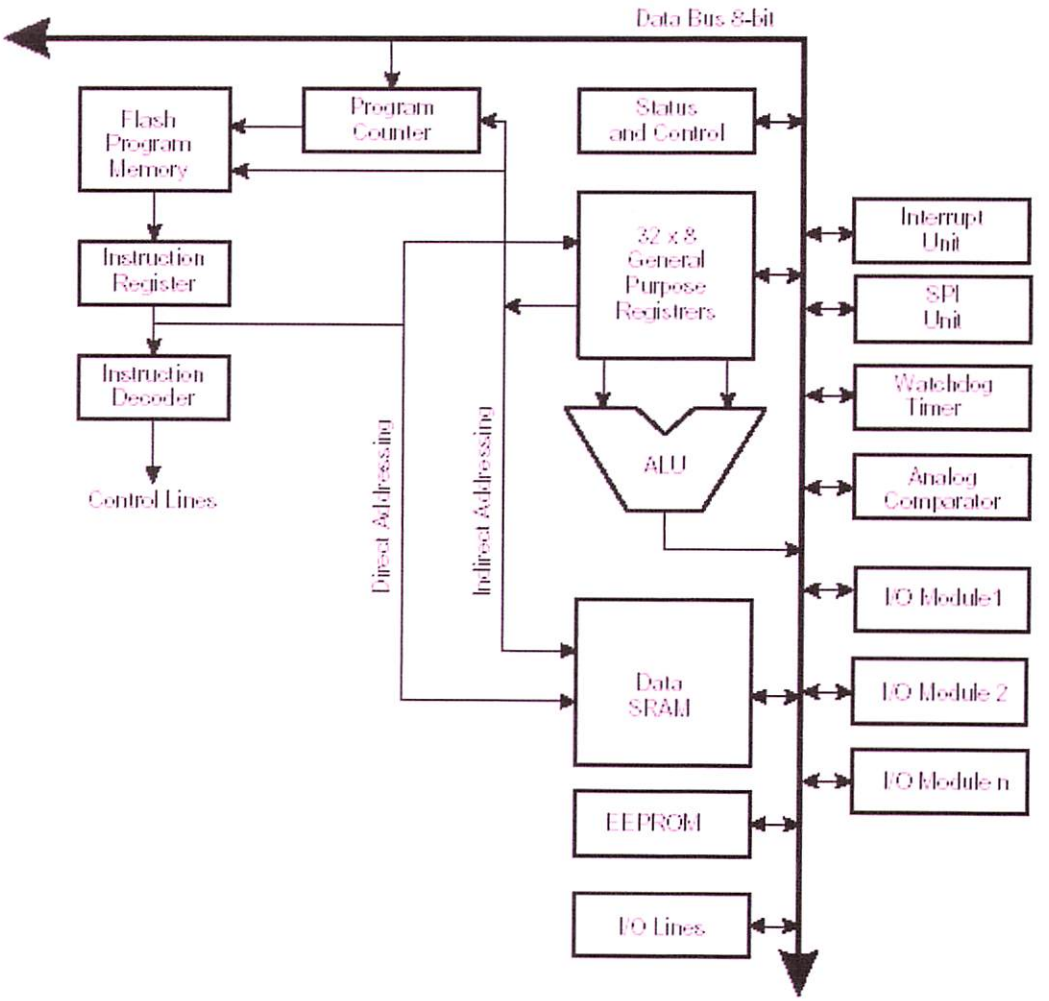
2.5.1 Arsitektur Mikrokontroller AVR ATMEL Atmega 8.

AVR Atmega8 adalah mikrokontroler 8-bit CMOS, low-power yang berdasarkan pada bentuk arsitektur AVR RISC (Reduced Instruction Set Komputer), yang hampir semua instruksinya selesai dikerjakan dalam satu siklus clock. AVR ATmega8 menggunakan instruksi tunggal (Single Clock Cycle), yaitu sistem mikrokontroler yang frekuensi kerja dalam chip sama dengan frekuensi kristal untuk osilator tanpa memerlukan rangkaian pembagi frekuensi setelah osilator yang diperlukan untuk memperoleh perbedaan fase dari clock, sehingga AVR 12 kali lebih cepat dibanding MCS51.

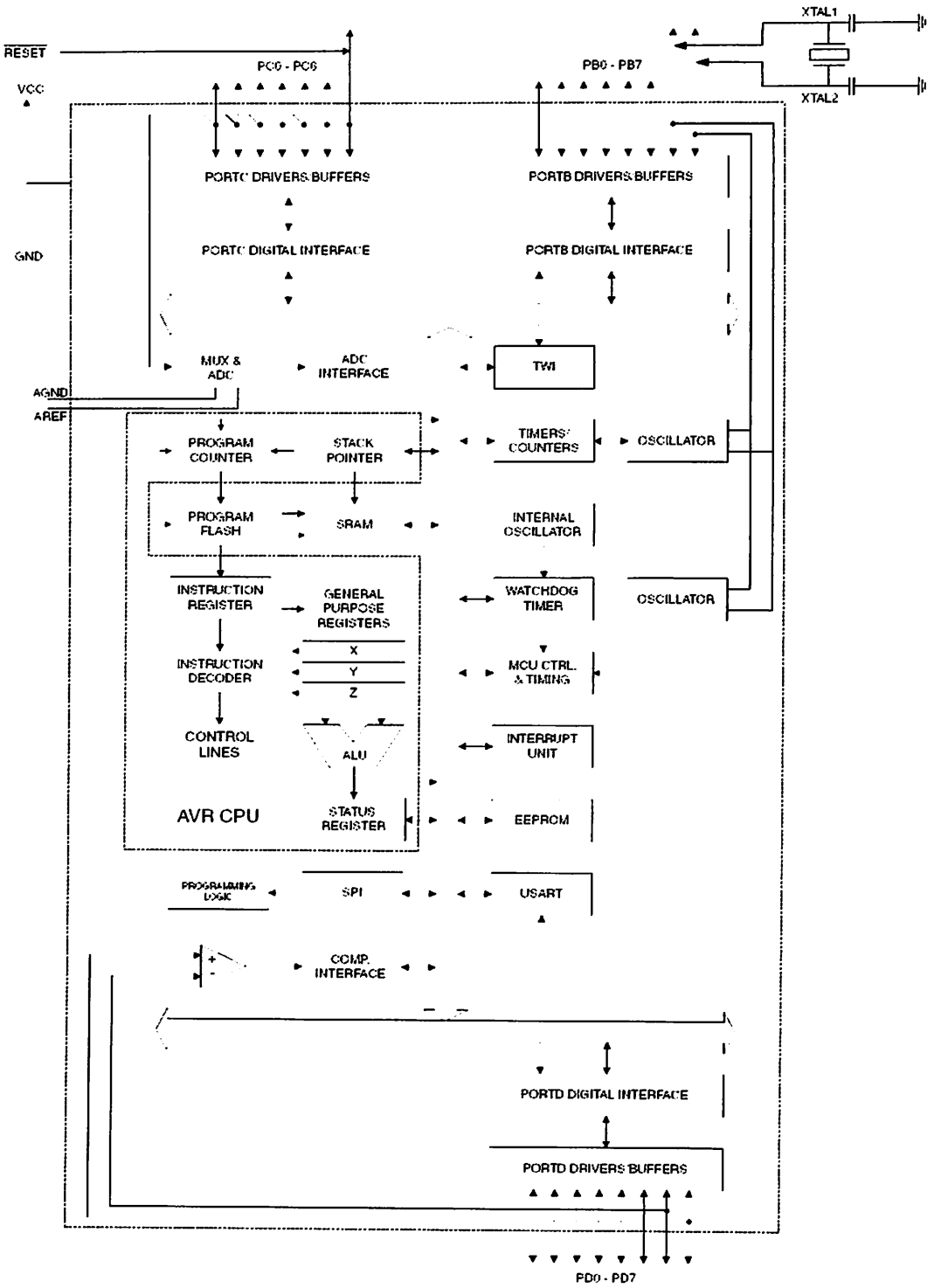
Berbagai karakteristik yang tersedia dalam IC ATmega8 adalah sebagai berikut:

- 8K bytes In-Sistem Programable Flash
- 512 bytes EEPROM (Electrical Erasable Programable Read Only Memory)

- 512 bytes SRAM (Static Random Access Memory)
- 23 jalur I/O general-purpose
- 32 x 8 general-purpose working register
- Timer/ Counter yang fleksibel dengan mode pembanding
- Interupsi internal dan eksternal
- Pemrograman serial UART (Universal Asynchronous Receiver and Transmitter)
- Serial Port SPI (Serial Peripheral Interface)
-



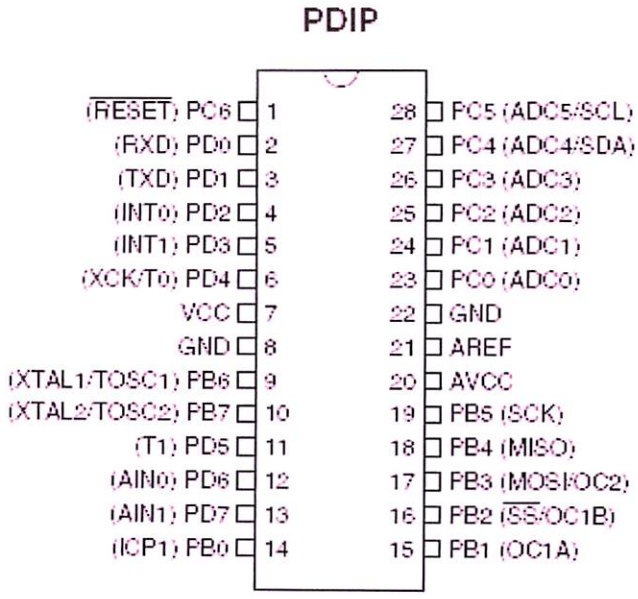
Gambar 2 - 6. Arsitektur Mikrokontroller AVR ATMEL Atmega 8



Gambar 2 - 7. Blok Diagram Mikrokontroller AVR ATMEL Atmega8

2.5.2. Konfigurasi Pin-Pin Mikrokontroller AVR ATMEL Atmega8.

Mikrokontroller ATmega8 mempunyai 28 pin seperti pada gambar di bawah ini:



Gambar 2 - 8. Konfigurasi Pin Mikrokontroller AVR ATMEL Atmega8

Fungsi tiap pin-nya adalah sebagai berikut:

a. Vcc: Tegangan Supply

b. Gnd: Ground

c. Port A (PA0-PA7): Port dua arah I/O 8-bit, kaki portnya dapat menyediakan resistor pull-up internal (dipilih untuk masing-masing bit). Port A juga dapat mengendalikan tampilan LED secara langsung.

d. Port B (PB0-PB7: Port dua arah I/O 8-bit dengan resistor pull-up internal, digunakan pada fungsi-fungsi khusus dari karakteristik ATmega8.

e. Port C (PC0-PC7): Port dua arah I/O 7-bit dengan resistor pull-up internal.

f. PC6/$\overline{\text{RESET}}$: Jika fuse RSTDISBL sudah diprogram, PC6 digunakan sebagai suatu pin I/O. Jika fuse RSTDISBL belum diprogram, PC6 digunakan sebagai inputan reset dimana level low dari pin ini lebih panjang dari pulsa minimum yang dihasilkan reset.

g. Port D (PD0-PD7): Port dua arah /O 7-bit dengan resistor pull-up internal. Sebagai input, port D menggunakan eksternal pull low dengan sumber arus jika pull up resistor diaktifkan.

h. $\overline{\text{RESET}}$: Input reset. Level low-nya untuk lebih panjang dari pulsa minimum yang dihasilkan reset, meskipun clock tidak bekerja.

i. AV_{CC}: sebagai supplay tegangan untuk A/D konverter port C (3..0), dan ADC (7..6). Pin ini harus dihubungkan dengan V_{CC} melalui low-pass filter.

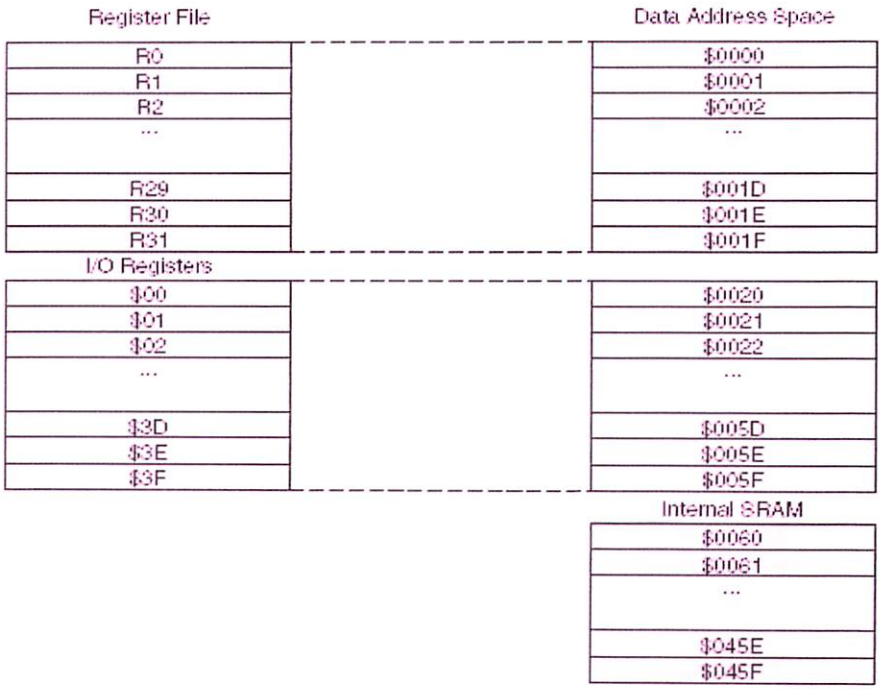
j. AREF: Pin analog referensi untuk A/D konverter.

k. ADC 7..6 (TQFT and MLF): Pada TQFP dan MLP, ADC 7..6 bekerja sebagai input analog untuk A/D konverter. Pin-pinnya mendapat daya dari power supplay analog dan dapat melayani 10 bit saluran ADC.

2.5.3. Peta Memori Mikrokontroller AVR ATMEL Atmega 8.

Mikrokontroller AVR ATMEL Atmega8 memiliki ruang pengalamatan memori data dan memori program yang terpisah. Memori data terbagi menjadi 3 bagian, yaitu 32 register umum, 64 buah register I/O, dan 1024 byte SRAM Internal.

Register keprluan umum menempati space data pada alamat terbawah, yaitu $00 sampai$1F. Sementara itu, register khusus unutk menangani I/O dan kontrol terhadap mikrokontroller menempati 64 alamat berikutnya, yaitu mulai dari $20 hingga $5F. register tersebut merupakan register yang khusus digunakan untuk mengatur fungsi terhadap peripheral mikrokontroller, seperti kontrol register, timer/ counter, fungsi-fungsi I/O, dan sebagainya. Alamat memori berikutnya digunakan untuk SRAM 1024 byte, yaitu pada lokasi $60 sampai dengan $45F. Konfigurasi memori data ditunjukkan pada gambar dibawah ini.



Gambar 2 - 9. Konfigurasi Memori Data

Mikrokontroller AVR ATMEL Atmega 8

Memori program yang terletak dalam Flash Sistem Reprogrammable Flash mempunyai 8K byte karena setiep instruksi memiliki lebar 16-bit atau 32-bit. AVR ATmega memiliki 4K byte x 16-bit Flash dengan alamat mulai dari $00 sampai $FFF. AVR tersebut memiliki 12-bit Program Counter sehingga mampu mengalamati isi Flash. Selain itu,AVR ATmega8 juga memiliki memori data berupa EEPROM 8-bit sebanyak 512 byte. Alamt EEPROM dimulai dari $000 sampai $1FF.

2.5.4. Status Register (SREG) Mikrokontroller AVR ATMEL Atmega 8

Status register adalah register berisis status yang dihasilkan pada setiap operasi yang dilakukan ketika suatu instruksi dieksekusi. SREG merupakan bagian dari inti CPU mikrokontroller.

Bit:	7	6	5	4	3	2	1	0	
	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Gambar 2 - 10. Status Register Mikrokontroller AVR ATMEL Atmega 8

Keteranga dari bit SREG adalah:

a. Bit7 - I: Global Interrupt Enable

Bit harus diset untuk meng-enable interupsi. Setelah itu, baru dapat mengaktifkan interupsi mana yang akan digunakan dengan cara meng-enable bit kontrol register yang bersangkutan secara individu. Bit akan di-clear apabila terjadi suatu interupsi, serta akan diset kembali oleh intruksi RETI.

b. Bit 6 – T: Bit Copy Storage

Intruksi BLD dan BST menggunakan bit-T sebagai sumber atau tujuan dalam operasi bit. Suatu bit dalam suatu register GPR dapat disalin ke bit T menggunakan instrusi BST, dan sebaliknya bit T dapat disalin kembali ke suatu bit dengan register GPR menggunakan instruksi BLD.

c. Bit 5 – H: Half Carry Flag

d. Bit 4 – S: Sign Bit, $S = N \oplus V$

Bit-S merupakan hasil operasi EOR antara flag-N (negative) dan flag V (komplemen dua overflow).

e. Bit 3 – V:Two's Complement Overflow Flag

Bit berguna untuk mendukung operasi aritmatika.

f. Bit 2 – N: Negative Flag

Apabila suatu operasi menghasilkan bilangan negative, maka flag-N akan diset.

g. Bit 1 – Z: Zero Flag

Bit akan diset bila hasil operasi yang diperoleh adalah nol.

h. Bit 0 – C: Carry Flag

Apabila suatu operasi menghasilkan carry, maka bit akan diset.

2.5.5. Register I/O.

Semua port pada AVR memiliki kebenaran fungsional read-modify-write ketika digunakan sebagai port I/O umum. Ini berarti bahwa arah dari satu pin port dapat diubah tanpa bermaksud mengubah arah dari pin yang lain. Logika port I/O dapat diubah-ubah dalam program secara byte atau hanya bit tertentu. Mengubah sebuah keluaran bit I/O dapat dilakukan menggunakan perintah cbi (clear bit I/O) untuk menhasilkan output low dan perintah sbi (set bit I/O) untuk menghasilkan output high. Pengubahan secara byte dilakukan dengan perintah in atau out yang menggunakan register bantu.

a. Port A

Tiga lokasi alamat memori I/O dilokasikan pada port A, masing-masing adalah register data-Port A, $1B ($3B), register data direction (register pengarah data)-DDRA, $1A ($3A), dan pin input port A-PIN A, $19 ($39). Pin-pin port A memiliki fungsi alternatif yang terhubung pada plihan data eksternal SRAM. Port A dapat dikonfigurasikan menjadi multiplexed low order alamat/data bus selama akses ke data memori eksternal. (blok diagram dapat dilihat pada lampiran).

b. Port B

Tiga lokasi alamat memori I/O yang dilokasikan pada port D, masing-masing adalah register data-port B, $18 ($38), register pengarah data-DDRB, $17 ($37), dan pin input port B-PINB, $16 ($36). (Blok diagram port B dan fungsi Timer/ Counter 2 pinnya dapat dilihat pada lampiran).

c. Port C

Tiga lokasi alamat memori I/O yang dilokasikan pada port C, masing-masing adalah register data-port C, $15 ($35), register pengarah data-DDRC, $14 ($34),

dan pin input port C-PINC, $13 ($33). (Blok diagram skematik dapat dilihat pada lampiran).

d. Port D

Tiga lokasi alamat memori I/O yang dilokasikan pada port D, masing-masing adalah register data-port D, $12 ($32), register pengarah data-DDRD, $11 ($31), dan pin input port D-PIND, $10 ($30). (Blok diagram skematik port D dan fungsi alternatif pinnya dapat dilihat pada lampiran).

2.5.6. Timer/ Counter 2.

Timer/ Counter 2 adalah 8 bit Timer/ Counter yang multifungsi. Deskripsi Timer/ counter 2 pada ATmega8 adalah sebagai berikut:

a. Sebagai Counter 1 kanal.
b. Timer dinolkan saat match compare (auto reload).
c. Dapat menghasilakan gelombang PWM dengan glitch-free.
d. Frekuensi generator.
e. Prescaler 10 bit untuk timer.
f. Interupsi timer yang disebabkan timer overflow dan match compare (TOV2 dan OCF2).
g. Dapat menggunakan clock dari kristal independent luar sebesar 32 kHz pada I/O clock.

Pengaturan Timer/Counter2 diatur oleh TCCR2 (Timer/ Counter Kontrol Register 0) yang dapat dilihat pada gambar berikut:

Bit	7	6	5	4	3	2	1	0	
	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	TCCR2
Read/Write	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Gambar 2 - 11. Register TCCR2

Penjelasan untuk setiap bit adalah:

a. bit 7 – FOC2: Force Output Compare

b. bit 6,3 – WGM21: WGM21:WGM20: Waveform Generator UnitI.

Bit tersebut mengontrol kenaikan counter, sumber dari nilai maksimum counter, dan tipe dari jenis Timer/ Counter yang dihasilkan, yaitu mode normal, clear timer, mode compare match, dan dua tipe dari PWM (Pulse Width Modulation). Berikut tabel setting pada bit untuk menghasilkan mode tertentu:

Tabel 2 - 9. Konfigurasi Bit WGM21 dan WGM20

Mode	WGM21 (CTC2)	WGM20 (PWM2)	Timer/Counter Mode of Operation[1]	TOP	Update of OCR2	TOV2 Flag Set
0	0	0	Normal	0xFF	Immediate	MAX
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	1	0	CTC	OCR2	Immediate	MAX
3	1	1	Fast PWM	0xFF	TOP	MAX

c. Bit 5,4 – COM01:COM00: Compare Match Output Mode

Bit mengontrol pin OC0 (Output Compare Pin). Apabila kedua bit tersebut nol atau clear, maka pin CO0 berfungsi sebagai pin biasa. Namun, jika salah satu bit set, maka fungsi bit tergantung pada setting bit pada WGM00 dan WGM01. Berikut daftar tabel setting bit pada WGM00 dan WGM01:

Tabel 2 - 10. Konfigurasi Bit COM21 dan COM20 Compare Output Mode non-PWM

COM21	COM20	Description
0	0	Normal port operation, OC2 disconnected.
0	1	Toggle OC2 on Compare Match
1	0	Clear OC2 on Compare Match
1	1	Set OC2 on Compare Match

Tabel 2 - 11. Konfigurasi Bit COM21 dan COM20 Compare Output Mode Fast PWM

COM21	COM20	Description
0	0	Normal port operation, OC2 disconnected.
0	1	Reserved
1	0	Clear OC2 on Compare Match, set OC2 at TOP
1	1	Set OC2 on Compare Match, clear OC2 at TOP

Tabel 2 - 12. Konfigurasi Bit COM21 dan COM20 Compare Output Mode Fast PWM

COM21	COM20	Description
0	0	Normal port operation, OC2 disconnected.
0	1	Reserved
1	0	Clear OC2 on Compare Match when up-counting. Set OC2 on Compare Match when downcounting.
1	1	Set OC2 on Compare Match when up-counting. Clear OC2 on Compare Match when downcounting.

d. Bit 2, 1, 0 – CS22, CS21, CS20

Ketiga bit tersebut memilih sumber clock yang akan digunakan oleh Timer/Counter. Berikut list tabelnya:

Tabel 2 - 13. Konfigurasi Bit Clock Select Untuk Memilih Sumber Clock

CS22	CS21	CS20	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	clk_{T2S}/(No prescaling)
0	1	0	clk_{T2S}/8 (From prescaler)
0	1	1	clk_{T2S}/32 (From prescaler)
1	0	0	clk_{T2S}/64 (From prescaler)
1	0	1	clk_{T2S}/128 (From prescaler)
1	1	0	clk_{T2S}/256 (From prescaler)
1	1	1	clk_{T2S}/1024 (From prescaler)

2.5.7. Interupsi.

Interupsi adalah kondisi yang membuat CPU berhenti dari rutinitas yang sedang dikerjakan (rutin utama) untuk mengerjakan rutin lain (rutin intrupsi). AVR ATMega8 memiliki 19 sumber interupsi.

a. Pada AVR terdapat 3 pin untuk interupsi eksternal, yaitu INT0, INT1, INT2. Interupsi eksternal dapat dibangkitkan apabila terdapat perubahan logika atau logika 0 pada pin interupsi. pengaturan kondisi keadaan yang menyebabkan terjadinya interupsi eksternal diatur oleh register MCUCR (MCU Kontrol Register). Yang terlihat pada gambar dibawah ini:

Bit	7	6	5	4	3	2	1	0	
	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	MCUCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Gambar 2 - 12. Register MCUCR

b. Bit ISC11 dan ISC10 bersama-sama menentukan kondisi yang dapat menyebabkan interupsi eksternal pada pin INT1. Keadaan selengkapnya dapat dilihat pada tabel dibawah ini:

Tabel 2 - 14. Beberapa Setting Kondisi Yang Menyebabkan Interupsi Eksternal I

ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Any logical change on INT1 generates an interrupt request.
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.

c. Bit ISC01 dan ISC00 bersama-sama menentukan kondisi yang dapat menyebabkan interupsi eksternal pada pin INT0. keadaan selengkapnya dapat dilihat pada tabel dibawah ini:

Tabel 2 - 15. Beberapa Setting Kondisi Yang Menyebabkan Interupsi Eksternal 0

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Any logical change on INT0 generates an interrupt request.
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

Pemilihan pengaktifan interupsi eksternal diatur oleh register GICR (General Interupsi Kontrol Register) yang terlihat seperti gambar berikut:

Bit	7	6	5	4	3	2	1	0	
	INT1	INT0	–	–	–	–	IVSEL	IVCE	GICR
Read/Write	R/W	R/W	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Gambar 2 - 13. General Interrupt Kontrol Register

Bit penyusun dapat dijelaskan sebagai berikut:

a. Bit INT1 adalah bit untuk mengaktifkan intrupsi ekternal 1. apabila bit tersebut diberi logika 1 dan bit-I pada SREG (status register) juga satu, maka interupsi eksternal 1 akan aktif.

b. Bit INT0 adalah bit untuk mengaktifkan intrupsi eksternal 0. apabiala bit tersebut diberi logika 1 dan bit-I pada SREG (status register) juga satu, maka interupsi eksternal 0 akan aktif.

c. Bit INT2 adalah bit untuk mengaktifkan interupsi ekternal 2 apabila bit tersebut diberi logika 1 dan bit-I pada SREG (status register) juga satu, maka ekternal 2 akan aktif.

Program interupsi dari masing-masing jenis interupsi eksternal akan dimulai dari vektor interupsi pada masing-masing jenis. Alamatnya dapat dilihat pada tabel di bawah.

Tabel 2 - 16. Macam Sumber Interupsi pada Mikrokontroller AVR ATMEL Atmega 8

Vector No.	Program Address(2)	Source	Interrupt Definition
1	0x000(1)	RESET	External Pin, Power-on Reset, Brown-out Reset, and Watchdog Reset
2	0x001	INT0	External Interrupt Request 0
3	0x002	INT1	External Interrupt Request 1
4	0x003	TIMER2 COMP	Timer/Counter2 Compare Match
5	0x004	TIMER2 OVF	Timer/Counter2 Overflow
6	0x005	TIMER1 CAPT	Timer/Counter1 Capture Event
7	0x006	TIMER1 COMPA	Timer/Counter1 Compare Match A
8	0x007	TIMER1 COMPB	Timer/Counter1 Compare Match B
9	0x008	TIMER1 OVF	Timer/Counter1 Overflow
10	0x009	TIMER0 OVF	Timer/Counter0 Overflow
11	0x00A	SPI, STC	Serial Transfer Complete
12	0x00B	USART, RXC	USART, Rx Complete
13	0x00C	USART, UDRE	USART Data Register Empty
14	0x00D	USART, TXC	USART, Tx Complete
15	0x00E	ADC	ADC Conversion Complete
16	0x00F	EE_RDY	EEPROM Ready
17	0x010	ANA_COMP	Analog Comparator
18	0x011	TWI	Two-wire Serial Interface
19	0x012	SPM_RDY	Store Program Memory Ready

Untuk inisialiasasi awal interupsi, perlu dituliskan terlebih dahulu vektor interupsi dari interupsi yang terdapat pada sistem. Vektor interupsi adalah nilai yang disimpan ke program counter pada saat terjadi interupsi sehingga program akan menuju ke alamat yang ditunjukkan oleh program counter. alamat interupsi eksternal 0 pada alamat 001H dan interupsi terima serial pada alamat 00B masing-masing alamat vektor memililki jarak yang berdekatan sehingga akan timbul masalah jika diperlukan rutin layanan interupsi yang panjang oleh sebab itu layanan interupsi ekternal 0 akan melompat ke alamat ext_int0 dan inetrupsi terima serial pada alamat USART_RXC.

Pengaktifan interupsi eksternal dilakukan dengan memberikan logika satu pada register GICR. Dengan demikian, pada pengaktifan interupsi ekternal 0, akan diberikan logika satu pada bit ke 6 register GICR. pengaktifan interupsi terima serial dilakukan

dengan memberikan logika 1 pada bit ke 7 register UCSRA. Terakhir, berikan perintah sei untuk menagaktifkan global interupt.

Interupsi dapat muncul kapan pun (kecuali jika bit enable interupsi dalam SREG clear) dengan demikian, interupsi juga dapat mencul ketika program sedang melakukan kalkulasi. Kalkulasi tersebut merubah flags dalam status register yang digunakan untuk next step dari kalkulasi atau untuk beberapa percabangan program. Jika ISR mengubah flags dalam SREG, maka kalkulasi yang sedang ditempatkan dalam program yang berjalan normal dapat di-corupt. Oleh sebab itu, perlu pengamanan SREG pada setiap subrutin interupsi.

2.5.8. Register TIMSK.

Selain register di atas terdapat pula register TIMSK (Timer/ Counter Interrupt Mask Register).

Bit	7	6	5	4	3	2	1	0	
	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	-	TOIE0	TIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Gambar 2 - 14. Register TIMSK

Penjelasan Untuk setiap bit adalah:

a. Bit 0 – TOIE0: Timer/ Counter 0 Overflow Interrup Enable
   Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka dilakukan enable interupsi Overflow Timer/ Counter 0.
b. Bit 1 – OCIE0: Timer/ Counter 0, Output Compare Match Interrupt Enable
   Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka bias dilakukan enable interupsi Output Compare Match Timer/ Counter 0.
c. Bit 2 – TOIE1: Timer/ Counter 1 Overflow Interrup Enable
   Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka dilakukan enable interupsi Overflow Timer/ Counter 1.
d. Bit 3 – OCIE1B: Timer/ Counter 1, Output Compare B Match Interrupt Enable

Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka dilakukan enable interupsi Overflow Compare Match B Timer/ Counter 1.

e. Bit 4 – OCIE1A: Timer/ Counter 1, Output Compare A Match Interrupt Enable

Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka dilakukan enable interupsi Overflow Compare Match A Timer/ Counter 1.

f. Bit 5 – TICIE1: Timer/ Counter 1 Input Capture Interrupt Enable

g. Bit 6 – TOIE2: Timer/ Counter 2, Overflow Interrupt Enable

Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka dilakukan enable interupsi Overflow Timer/ Counter 2.

h. Bit 7 – OCIE2: Timer/ Counter 2, Output Compare Match Interurpt Enable

Jika bit tersebut diberi logika satu dan bit i SREG juga set, maka bias dilakukan enable interupsi Output Compare Match Timer/ Counter 2.

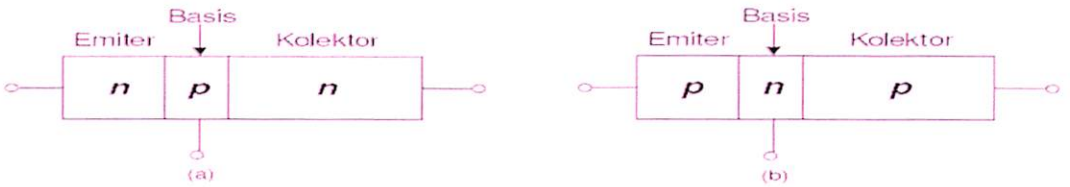
2.6. Transistor Switched.

2.6.1. Pengenalan Dasar.

Pada tahun 1949, Shockley mencoba teori dasar tansistor junction dan hasil pertamanya dihasilkan dalam tahun 1951, dampak transistor tersebut dalam elektronika berperan sangat besar. Di samping dimulainya Industri semikonduktor multi-bilyun dolar, transistor pun telah membuka jalan pada penemuan-penemuan rangkaian-terintegrasi, piranti opto-elektronik dan prosesor-mikro.

Pada rangkaian ini komponen yang digunakan adalah Transisitor PNP Silikon A733 produksi NEC.Komponen ini didesain khusus sebagai driver AF amplifier, karena memiliki fitur yang sangat sensitif pada h_{fe} dan ekselen linier dimana :

h_{FE} (V_{CE} = -6.0 V, I_C = -1.0 mA)



Gambar 2 - 15. Tiga Daerah Transistor.

(A) Transistor NPN. (B) Transistor PNP.

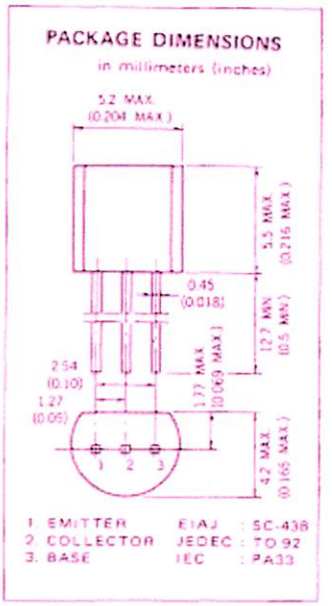
Pada Gambar 2-4a menunjukkan sebuah kristal npn. Emiter didope sangat banyak, dan berfungsi untuk mengemisikan atau menginjeksikan elektron ke dalam basis. Basis di dope sedikit, dan sangat tipis; basis melewatkan sebagian besar elektron-elektron yang diinjeksikan emiter ke kolektor. Tingkat doping (doping level) dari kolektor berada pada tingkat menengah, antara tingkat doping dari emiter dan tingkat doping dari basis. Kolektor dinamakan demikian, karena kolektor mengumpulkan atau menangkap elektron-elektron dari basis. Kolektor merupakan bagian yang terbesar dari tiga bagian tersebut; kolektor harus mendisipasikan lebih banyak panas daripada emiter atau basis.

Transistor pada Gambar 2-4a mempunyai dua sambungan (junction), satu di antara emiter dan basis dan lainnya diantara basis dan kolektor. Karena inilah, sebuah transistor sama seperti dua buah dioda. Transistor npn disebut juga diode emiter basis atau singkatnya dioda emiter. Transistor pnp pun disebut juga diode kolektor basis atau dioda kolektor.

Gambar 2-4b menunjukkan kemungkinan yang lain, yaitu sebuah transistor pnp. Transistor pnp merupakan komplemen dari transistor npn. Pembawa muatan mayoritas pada emiter adalah hole, sebagai pengganti dari muatan bebas. Ini berarti, pada transistor pnp dibutuhkan arus dan tegangan yang berlawanan dengan transistor npn.

2.6.2. Karakteristik Transistor A733.

Pada komponen ini memiliki 3 pin yang terdiri dari emitor, basis dan kolektor. Adapun daitunjukan pada gambar berikut :



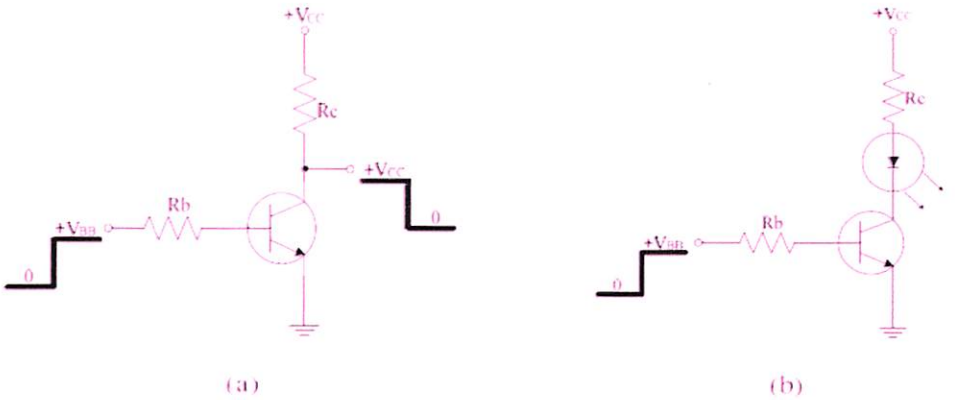
Gambar 2 - 16. Bentuk Dimensi Transistor A733.

Salah satu penggunaan dari transistor adalah sebagai switch atau saklar, artinya bahwa kita mengoperasikan transistor pada salah satu dari saturasi atau titik sumbat, tetapi tidak di tempat-tempat sepanjang garis beban.

Jika sebuah transistor berada dalam keadaan saturasi, transistor tersebut seperti sebuah switch yang tertutup dari kolektor ke emiter. Jika transistor tersumbat (cutoff), transistor seperti sebuah switch yang terbuka. Dalam transistor dikenal istilah aturan disain Soft saturation dan Hard saturation. Soft saturation berarti kita membuat transistor hampir saturasi, di mana arus basis hanya cukup untuk mengoperasikan transistor pada ujung atas dari garis beban. Soft saturation tidak dapat diandalkan pada produksi massa karena adanya perubahan-perubahan pada ßdc dan IB(sat). Soft saturation akan mengacu pada rancangan dimana transistor akan jenuh secara terbatas, dalam hal ini penguatan arus hanya sedikit lebih kecil daripada penguatan arus aktif.

Pada kondisi Hard saturation, berarti terdapat arus basis yang cukup kuat untuk membuat transistor saturasi pada semua harga dari ßdc. Untuk keadaan yang paling buruk dari temperatur dan arus, hampir semua transistor silikon sinyal kecil mempunyai ßdc lebih besar daripada 10. Karena itu, suatu pedoman disain untuk hard saturation

adalah mempunyai arus basis kira-kira sepersepuluh dari harga saturasi arus kolektor; ini menjamin hard saturation pada semua kondisi kerja. Sebagai contoh, jika ujung atas garis beban mempunyai arus kolektor sebesar 10 mA, maka akan di dapatkan arus basis sebesar 1 mA. Hal ini menjamin keadaan saturasi untuk semua transistor, arus, temperatur dan sebagainya. Di gunakan aturan 10 : 1 dalam proses mendisain rangkaian switching transistor, kecuali jika di tentukan lain. Ingat, ini hanya suatu pedoman. Jika nilai tahanan standar menghasilkan perbandingan IC/IB sedikit lebih besar daripada 10, hampir setiap transistor sinyal kecil akan menuju keadaan hard saturation.



Gambar 2 - 17. Contoh-contoh dari transistor yang digunakan sebagai switch.

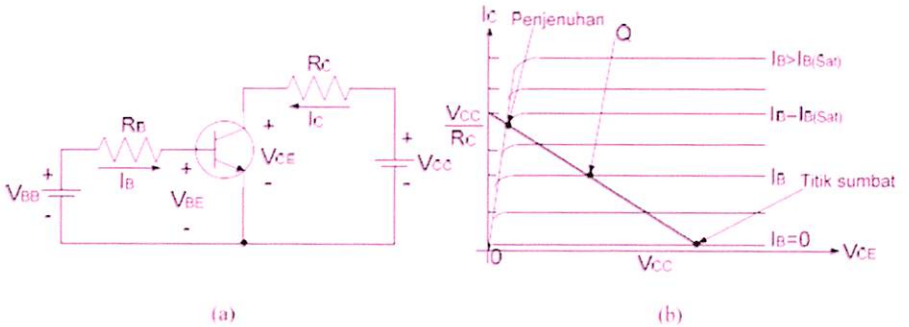
Gambar 2-6a menunjukkan sebuah rangkaian switching transistor yang digerakkan oleh tegangan step. Jika tegangan input nol, transistor tersumbat (cutoff). Dalam hal ini, transistor kelihatannya seperti sebuah switch yang terbuka. Dengan tidak adanya arus yang mengalir melalui tahanan kolektor, maka tegangan keluaran sama dengan +VBB.

Gambar 2-6b menunjukkan suatu disain dengan adanya sedikit variasi. Rangkaian ini disebut sebuah LED driver, karena transistor mengendalikan LED. Jika tegangan masukan rendah (low), transistor akan tersumbat (cutoff) dan LED padam. Jika tegangan masukan tinggi (high), transistor saturasi dan LED menyala.

Tabel 2 - 17. Karakteristik Transisitor A733.

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	90	200	600		$V_{CE}=-6.0$ V, $I_C=-1.0$ mA
NF	Noise Figure		6.0	20	dB	$V_{CE}=-6.0$ V, $I_C=-0.3$ mA, $R_G=10$ kΩ, f=100 Hz
f_T	Gain Bandwidth Product	100	180		MHz	$V_{CE}=-6.0$ V, $I_E=10$ mA
C_{ob}	Output Capacitance		4.5	6.0	pF	$V_{CB}=-10$ V, $I_E=0$, f=1.0 MHz
I_{CBO}	Collector Cutoff Current			-0.1	μA	$V_{CB}=-60$ V, $I_E=0$
I_{EBO}	Emitter Cutoff Current			-0.1	μA	$V_{EB}=-5.0$ V, $I_C=0$
V_{BE}	Base to Emitter Voltage	-0.58	-0.62	-0.68	V	$V_{CE}=-6.0$ V, $I_C=-1.0$ mA
$V_{CE(sat)}$	Collector Saturation Voltage		-0.18	-0.3	V	$I_C=-100$ mA, $I_B=-10$ mA

2.6.3. Persamaan Nilai Transistor.



Gambar 2 – 18. (a) Bias basis. (b) Garis beban dc.

Gambar 2-5a memperlihatkan rangkaian bias basis. Sebuah sumber tegangan VBB membias maju dioda emiter melalui resistor RB yang juga berfungsi membatasi arus. Penjumlahan tegangan di sekitar loop input memberikan :

I BRB VBE VBB = 0

sehingga arus bias pada basis adalah :

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

dimana VBE = 0,7 V untuk transistor silikon dan 0,3 V untuk germanium.

Dalam rangkaian kolektor, sumber tegangan VCC membias balik diode kolektor melalui RC. Dengan hukum tegangan Kirchhoff, diperoleh tegangan kolektor-emiter.

Dalam rangkaian bias basis yang di perlihatkan Gambar 2-5a, VCC dan RC adalah konstan, VCE dan IC adalah vertikal. Pada persamaan diatas apabila di sederhanakan akan dapat di tentukan besarnya arus Ic, seperti terlihat pada persamaan berikut :

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

Gambar 2-5b menunjukkan grafik dari persamaan diatas memotong kurva kurva dari kolektor. Perpotongan vertikal adalah pada VCC/RC dan perpotongan horizontal pada VCC.

Garis ini disebut garis beban dc karena garis ini menyatakan semua titik operasi yang mungkin. Perpotongan dari garis beban dc dengan arus basis adalah titik operasi kerja dari transistor. Titik dimana garis beban memotong kurva IB = 0 disebut titik sumbat (cutoff). Pada titik ini, arus basis nol dan arus kolektor sangat kecil, sehingga dapat diabaikan (hanya ada arus bocor ICEO). Pada titik sumbat, dioda emiter tidak lagi dibias maju,dan transistor kehilangan kerja normalnya. Untuk itu digunakan suatu pendekatan, bahwa tegangan kolektor-emiter adalah :

VCE (cutoff) , VCC (2-8)

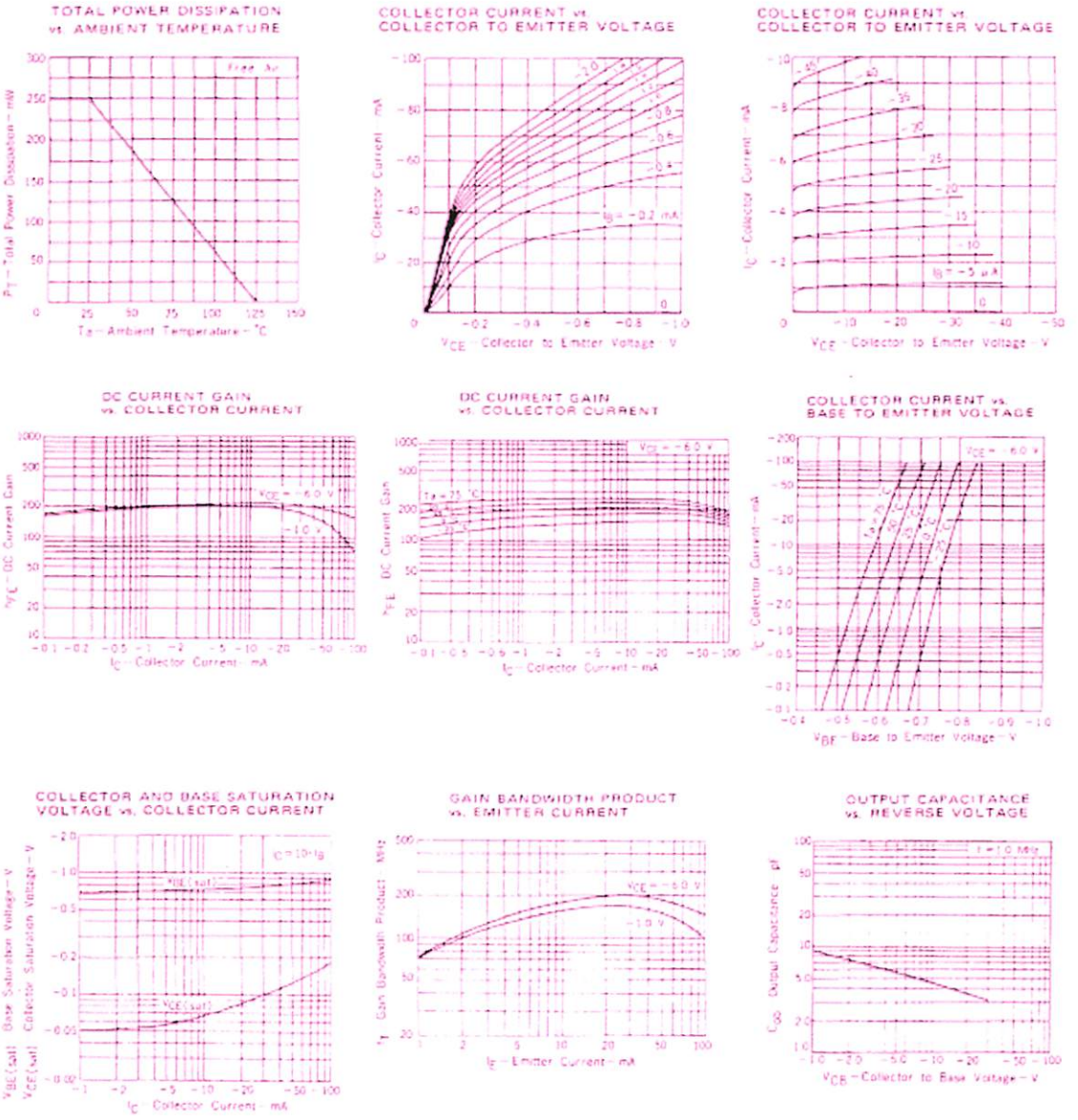
Perpotongan dari garis beban dan kurva IB = IB(sat) disebut saturasi. Pada titik ini, arus basis sama dengan IB(sat) dan arus kolektor adalah maksimum. Pada saturasi, dioda kolektor tidak lagi dibias balik, dan transistor kehilangan kerja normalnya. Untuk itu digunakan suatu pendekatan, bahwa arus kolektor pada saturasi adalah seperti di perlihatkan pada persamaan :

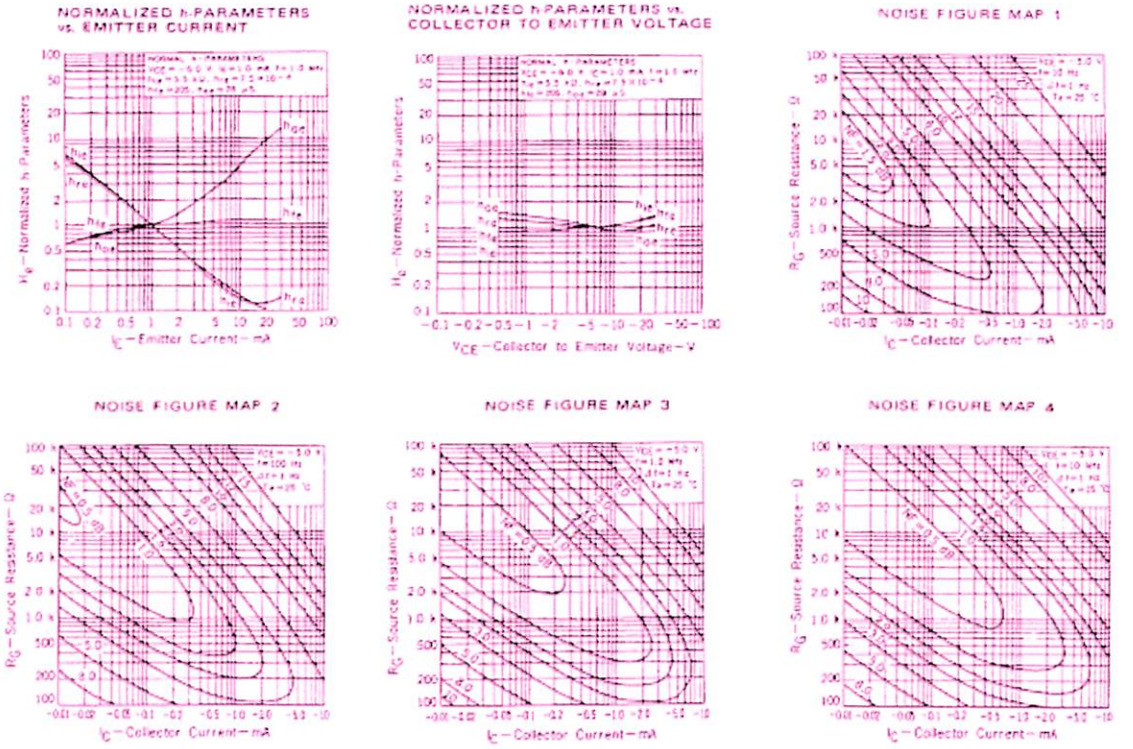
$$I_{C(Sat)} = \frac{VCC}{R_C}$$

dan arus basis yang tepat menimbulkan saturasi adalah seperti di perlihatkan pada persamaan :

$$I_{B(Sat)} = \frac{I_{C(Sat)}}{\beta_d}$$

Grafik 2 – 7. Tipikal Karakteristik Transistor A733



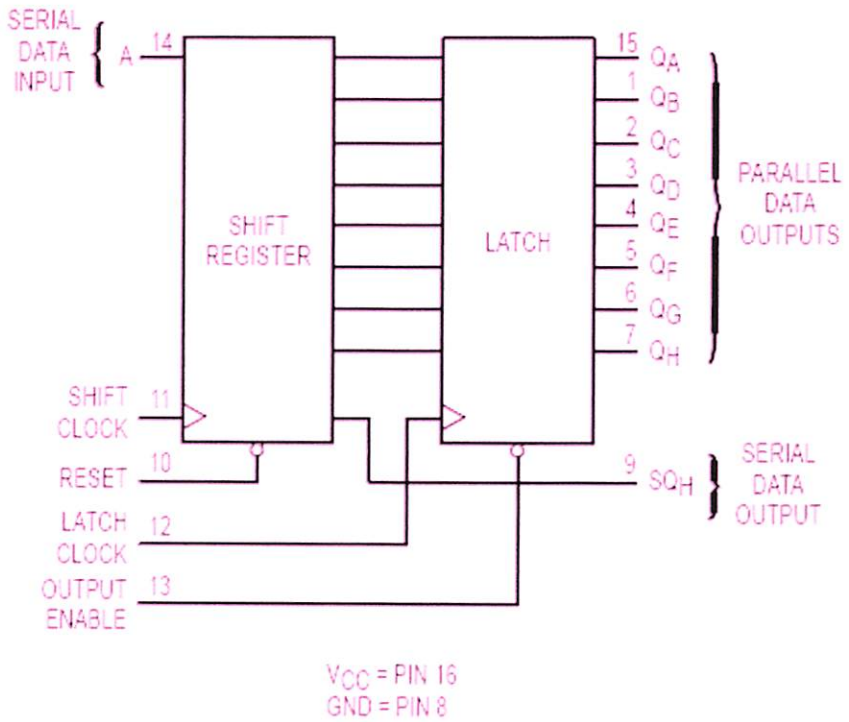


2.7. Serial To Pararel Shift Register.

2.7.1. Pengenalan Dasar.

Komponen yang digunakan pada skripsi ini adalah Motorola 74HC595 dikarenakan sebagai pendukung pembacaan transfer data dari Mikrokontroller AVR ATMEL Atmega 8. Adapun fitur yang dimiliki oleh Serial To Pararel Shift Register Motorola 74LS595 adalah sebagai berikut :

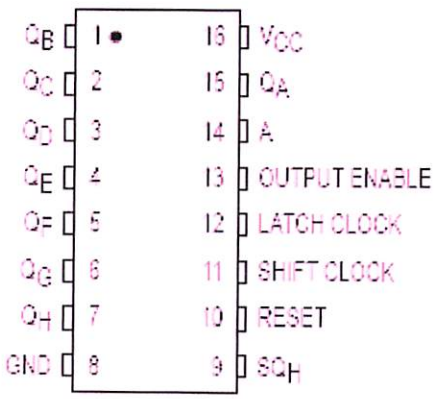
- Kapasitas output drive : 15 LSTTL.
- Output direck interface pada CMOS, NMOS, dan TTL.
- Rentan tegangan operasional 2 V hingga 6 V.
- Arus input minimum 1μA
- CMOS memiliki selektfitas tinggi pada noise.
- Chip komplek terdiri dari 328 FETs dan 82 gerbang ekivalen.
- Imunitas LATCH Dan Input fleksibel.



Gambar 2 - 19. Logic Diagram 74HC595

2.7.2. Konfigurasi Pin Serial To Pararel Shift Register Motorolla 74HC595.

Serial To Pararel Shift Register Motorolla 74LS595 memiliki 18 pin yang ditunjukan seperti dibawah ini :



Gambar 2 – 20. Konfigurasi Pin 74HC595

Adapun fungsi dari tian pin adalah sebagai berikut :

Port 1 : Q_B, Berfungsi sebagai output dari non inverter, 3-state, dan latch.

Port 2 : Q_C, Berfungsi sebagai output dari non inverter, 3-state, dan latch.

Port 3 : Q_D, Berfungsi sebagai output dari non inverter, 3-state, dan latch.

Port 4 : Q_E, Berfungsi sebagai output dari non inverter, 3-state, dan latch.

Port 5 : Q_F, Berfungsi sebagai output dari non inverter, 3-state, dan latch.

Port 6 : Q_G, Berfungsi sebagai output dari non inverter, 3-state, dan latch.

Port 7 : Q_H, Berfungsi sebagai output dari non inverter, 3-state, dan latch.

Port 8 : GND, Berfungsi sebagai ground.

Port 9 : SQ_H, Berfungsi sebagai output serial data yang memiliki 8-Bit shift register.

Port 10 : RESET, Berfungsi sebagai input reset shift register.

Port 11 : SHIFT LOCK, Berfungsi sebagai input shift register clock.

Port 12 : LATCH LOCK, Berfungsi sebagai input Latch Lock Storage.

Port 13 : OUTPUT ENABLE, Berfungsi sebagai aktifasi rendah low output enable (Q_A-Q_H)

Port 14:A, Berfungsi sebagai input serial data aktif pada 8-bit serial shift register.

Port 15 : Q_A, Berfungsi sebagai output dari non inverter, 3-state, dan latch.

Port 16 : VCC, Berfungsi sebagai sumber tegangan masuk.

2.7.3. Karakteristik Serial To Pararel Shift Register Motorolla 74HC595.

Tabel 2 - 18. Rating Maksimum.

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package) (Ceramic DIP)	 260 300	°C

Tabel 2 – 19. Rekomendasi Operasional.

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

Tabel 2 - 20. Karakter DC

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	≤ 85°C	≤ 125°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage, Q_A – Q_H	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low-Level Output Voltage, $Q_A - Q_H$	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \leq 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \leq 2.4$ mA $\lvert I_{out} \rvert \leq 6.0$ mA $\lvert I_{out} \rvert \leq 7.8$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
V_{OH}	Minimum High-Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \leq 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \leq 2.4$ mA $\lvert I_{out} \rvert \leq 4.0$ mA $\lvert I_{out} \rvert \leq 5.2$ mA	3.0 4.5 6.0	2.98 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \leq 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out} \rvert \leq 2.4$ mA $\lvert I_{out} \rvert \leq 4.0$ mA $\lvert I_{out} \rvert \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current, $Q_A - Q_H$	Output in High-Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\ \mu A$	6.0	4.0	40	160	μA

Tabel 2 - 21. Karakter AC.

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Shift Clock to SQ_H (Figures 1 and 7)	2.0 3.0 4.5 6.0	140 100 28 24	175 125 35 30	210 150 42 36	ns
t_{PHL}	Maximum Propagation Delay, Reset to SQ_H (Figures 2 and 7)	2.0 3.0 4.5 6.0	145 100 29 25	180 125 36 31	220 150 44 38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Clock to $Q_A - Q_H$ (Figures 3 and 7)	2.0 3.0 4.5 6.0	140 100 28 24	175 125 35 30	210 150 42 36	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to $Q_A - Q_H$ (Figures 4 and 8)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to $Q_A - Q_H$ (Figures 4 and 8)	2.0 3.0 4.5 6.0	135 90 27 23	170 110 34 29	205 130 41 35	ns

Tabel 2 - 12. Timing Requirement.

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0 3.0 4.5 6.0	75 60 15 13	95 70 19 16	110 80 22 19	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0	5.0 5.0 5.0 5.0	5.0 5.0 5.0 5.0	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	60 45 12 10	75 60 15 13	90 70 18 15	ns
t_w	Minimum Pulse Width, Shift Clock (Figure 1)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_w	Minimum Pulse Width, Latch Clock (Figure 6)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55 to 25°C	≤ 85°C	≤ 125°C	
t_{TLH}, t_{THL}	Maximum Output Transition Time, $Q_A - Q_H$ (Figures 3 and 7)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 31 18 15	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, SQ_H (Figures 1 and 7)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State), $Q_A - Q_H$	—	15	15	15	pF

Tabel 2 - 23. Fungsi Keseluruhan.

Operation	Inputs					Resulting Function			
	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output SQ_H	Parallel Outputs $Q_A - Q_H$
Reset shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	$D - SR_A$; $SR_N - SR_{N+1}$	U	$SR_G - SR_H$	U
Shift register remains unchanged	H	X	L, H, ↓	L, H, ↓	L	U	U	U	U
Transfer shift register contents to latch register	H	X	L, H, ↓	↑	L	U	$SR_N - LR_N$	U	SR_N
Latch register remains unchanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

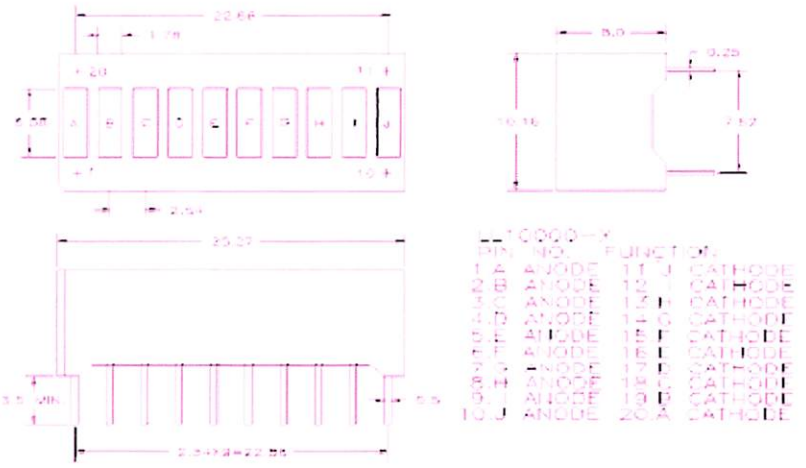
SR = shift register contents
LR = latch register contents
D = data (L, H) logic level
U = remains unchanged
↑ = Low-to-High
↓ = High-to-Low
* = depends on Reset and Shift Clock inputs
** = depends on Latch Clock input

2.8. LED Array.

2.8.1. Pengenalan Dasar.

LED Array yang digunakan dalan skripsi ini adalah produksi dari LEDTECH 10 Segment, dimana berfungsi sebagai tampilan output dari proses yang telah dilakukan. LED Array akan aktif apabila mendapai masukan arus dan logika 1, begitu pula akan pasif apabila tidak mendapat masukan arus dan logika 0.

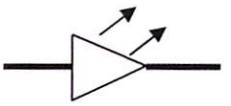
LED Array adalah deretan LED (Light Emiter Diode) yang terdiri dari anoda dan katoda, dimana apabila mendapat arus masuk akan aktif (menyala).



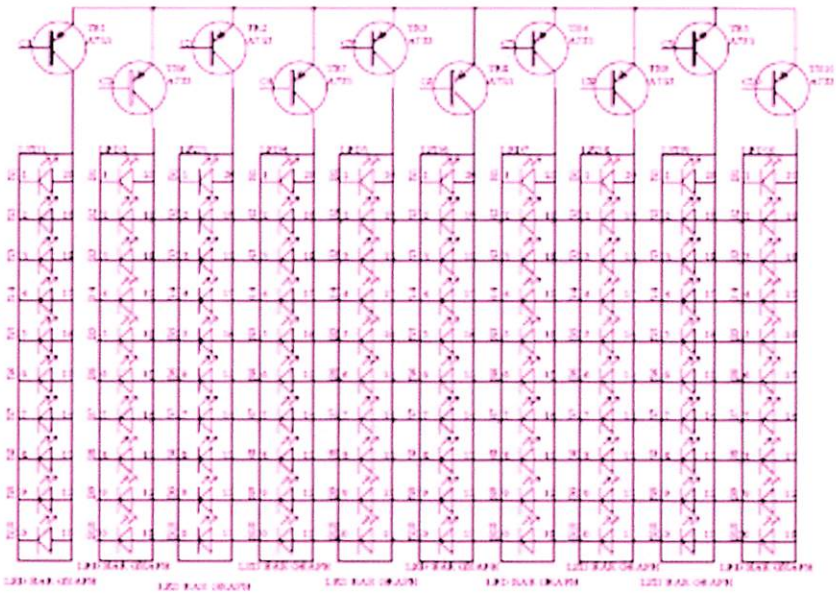
Gambar 2 - 21. Bentuk Fisik Dari LED Array LEDTECH 10 Segment.

2.8.2. Karakteristik LED Array.

LED Array pada dasarnya adalah deretan LED (Light Emiter Diode) yang disusun seefisien mungkin untuk mendapatkan dimensi yang tidak terlalu besar dan memerlukan arus yang memadai agar dapat mengaktifkan komponen tersebut.



Gambar 2 - 22. Simbol LED (Light Emiter Diode)



Gambar 2 - 23. LED Array LEDTECH 10 Segment.

Tabel 2 - 24. Karakteristik LED Array LEDTECH 10 Segment.

10 SEGMENT		λp (nm)	V_F (V)		I_V (mcd)	
PART NUMBER	CHIP COLOR	TYP.	TYP.	MAX.	MIN.	TYP.
LL10000-GEWAK	GREEN	572	2.1	2.4	4.6	7.7
LL10000-YEWAK	YELLOW	589	2.1	2.4	3.8	6.3
LL10000-OEWAK	ORANGE	630	2.1	2.4	5.3	8.8
LL10000-HRRRAK	ORANGE	630	2.1	2.4	5.3	8.8
LL10000-SBEWAK	SB RED	660	1.7	2.2	12.3	20.5
LL10000-MIEWAK	RED	660	1.7	2.2	7.4	12.3
LL10000-PREWAK	RED	700	2.1	2.4	1.2	2.1

BAB III
PERENCANAN DAN PEMBUATAN ALAT

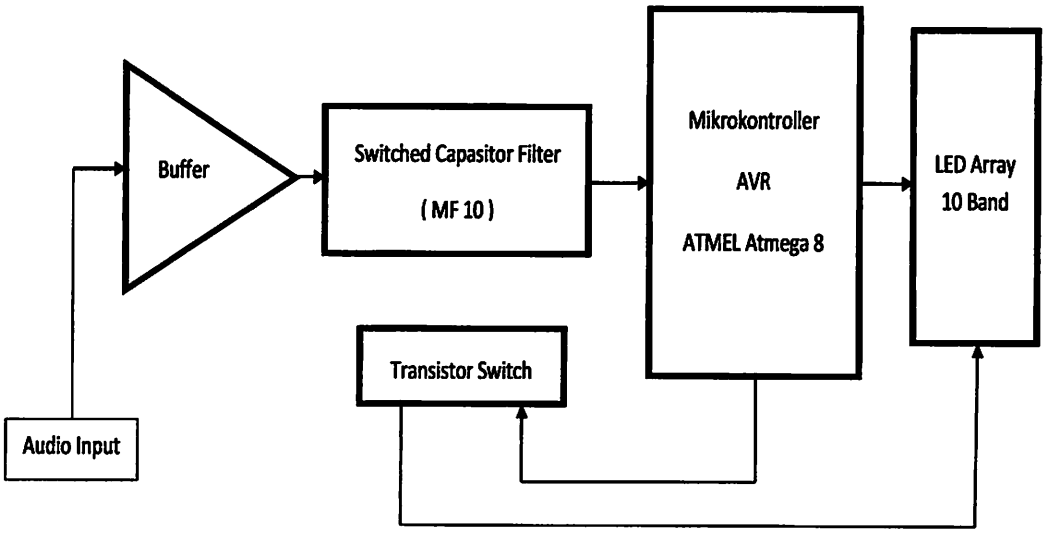
3.1. Pendahuluan.

Dalam perancangan alat ini dapat dibagi menjadi dua bagian yang terdiri atas perancangan perangkat keras dan perancangan perangkat lunak yang mendukung sistem kerja alat ini. Pada perancangan perangkat keras meliputi perancangan diagram blok sistem, perancangan rangkaian Switched Capasitor Filter (MF 10), Mikrokontroler AVR ATMEL Atmega 8, Transistor Switched, yang berfungsi sebagai media penghubung ke Personal Computer serta LED Array sebagai media tampilan keluaran dari system yang telah dilakukan. Sedangkan perancangan perangkat lunaknya, menjelaskan perangkat lunak yang digunakan untuk menjalankan sistem, dimana menggunakan bahasa Code Vision AVR C Compiller dan Ponyprog 2000 .

Dalam perencanaan ini dilakukan secara bertahap untuk memudahkan dalam menganalisis setiap bagiannya maupun dalam sistem keseluruhan. Perencanaan dan pembuatan sistem ini terdiri atas dua perencanaan utama, yaitu perencanaan perangkat keras dan perencanaan perangkat lunak, disamping itu aspek lainnya yang juga perlu dijelaskan dalam pembahasan bab ini seperti penentuan spesifikasi atas sistem yang dirancang dalam blok diagram dan prinsip kerja sistem.

3.2. Blok Diagram.

Adapun diagram blok dari perancangan alat ini adalah sebagai berikut:



Gambar 3 - 1. Blok Diagram Sistem

3.3. Spesifikasi Alat.

Perancangan alat ini mempunyai beberapa spesifikasi sebagai berikut:

1. Buffer yang digunakan sebagai pemilih sinyal masukan yang berupa sinyal audio.
2. IC MF 10 (Switched Capasitor Filter) berfungsi sebagai penyaring sinyal masukan dari Buffer.
3. Menggunakan mikrokontroler ATMEL AVR Atmega 8 sebagai pengolah data dan pengontrol keseluruhan kinerja system.
4. Transistor Switched berfungsi sebagai saklar elektrik akan menempatkan sinyal dari rentan 40 Hz – 65 KHz
5. LED Array sebagai tampilan keluaran dari proses kerja.
6. Perangkat lunak dari system kerja menggunakan Code Cision Compailler AVR dan Ponyprog 2000.

3.4. Prinsip Kerja Rangkaian.

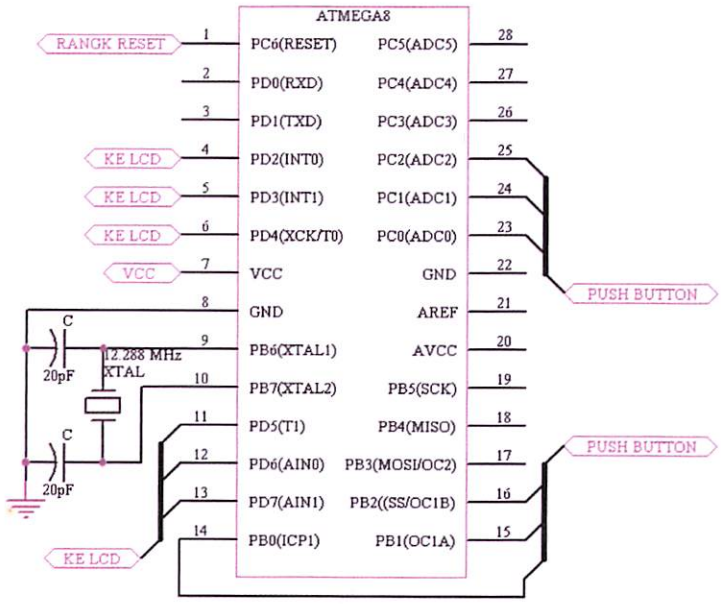
Pada dasarnya prinsip kerja dari alat ini adalah mendeteksi sinyal keluaran dari system yang telah dijalankan, dimana berupa sinyal audio dengan rentan frekuensi dari 60 Hz hingga 60 KHz. Cara kerja dari spektrum audio 10 band berbasis Switched Capasitor Filter (MF 10) dicontrol microcontroller ATMEL AVR Atmega 8 diawali dengan sinyal masukan dari audio input yang melewati Buffer akan diolah dan dipisahkan kemudian ditransfer ke Switched Capasitor Filter (MF 10) yang akan memilah sinyal dan disaring. Informasi tersebut akan diterjemahkan oleh mikrokontroler ATMEL AVR Atmega 8 sehingga data yang ada pada PC dapat ditampilkan pada LED Array sehingga dapat diketahui hasil dari proses kerja.

3.5. Perencanaan Perangkat Keras.

Perangkat keras yang digunakan dalam sistem ini terdiri atas beberapa bagian yaitu:

3.5.1. Mikrokontroler AVR ATMEL Atmega 8.

Komponen produksi ATMEL yang berorientasi control (mikrokontroller). Intel mengklarifikasikan dalam kelompok *embedded microcontroller*, yang artinya adalah mikrokontroler yang dapat diprogram ulang *(reprogrammable)*. Di dalam *chip* mikrokontroler ATMEL AVR Atmega 8 ini sudah tersedia berbagai macam peralatan pendukung mikroprosesor seperti RAM, *serial port, bus – bus* data dan lainnya yang membuat pemakai *chip* ini dapat menekan penambahan komponen pendukung.Pada rangkaian ini komponen utamanya adalah unit Mikrokontroler ATmega8. Komponen ini merupakan sebuah *chip* tunggal sebagai pengolah data dan pengontrolan alat. Sebagai pengolah data dan pengontrolan sistem, pin-pin mikrokontroler ATmega8 dihubungkan pada rangkaian pendukung membentuk suatu sistem, yang ditunjukkan pada gambar di bawah ini:



Gambar 3 - 2. Perencanaan Rangkaian Mikrokontroler AVR ATMEL Atmega 8.

Port – Port Yang Digunakan Dalam Sistem :

Port 1 : Reset (PC6). Digunakan sebagai rangkaian reset. Untuk interupt dari Port 1 meliputi Ekternal Pin, Power On-Reset, Brown Out Reset dan Watchdog Reset.

Port 2 : PDO (RXD). Digunakan sebagai input untuk mengaktifkan LED Array kolom ke 10.

Port 3 : PD1 (TXD). Digunakan sebagai input untuk mengaktifkan LED Array kolom ke 9.

Port 4 : PD2 (INT0). Digunakan sebagai input untuk mengaktifkan LED Array kolom ke 8.

Port 5 : PD3 (INT1). Digunakan sebagai input untuk mengaktifkan LED Array kolom ke 7.

Port 6 : PD4 (XCK/T0). Digunakan sebagai input untuk mengaktifkan LED Array kolom ke 6.

Port 7 : VCC. Digunakan sebagai sumber tegangan yang dibutuhkan.

Port 8 : GND. Digunakan sebagai ground.

Port 9 : PB6 (XTAL1).

Port 10: PB7 (XTAL2).

Port 11: PD5 (T1). Digunakan sebagai input untuk mengaktifkan LED Array kolom ke 1.

Port 12: PD6 (AIN0). Digunakan sebagai input untuk mengaktifkan LED Array kolom ke 2 .

Port 13: PD7 (AIN1). Digunakan sebagai input untuk mengaktifkan LED Array kolom ke 3 .

Port 14: PB0 (ICP1). Digunakan sebagai input untuk mengaktifkan LED Array kolom ke 4 .

Port 15: PB1 (OC1A). Digunakan sebagai input untuk mengaktifkan LED Array kolom ke 1.

Port 16: PB2 (SS/OC1B). Digunakan sebagai perantara ke Header 4 CONS5.

Port 17: PB3 (MOSI/OC2). Digunakan sebagai perantara ke CON1 ISP Port 1(RST).

Port 18: PB4 (MISO). Digunakan sebagai perantara ke CON1 ISP Port 4.

Port 19: PB5 (SCK). Digunakan sebagai perantara ke CON1 ISP Port 3.

Port 20: AVCC. Digunakan sebagai sumber tegangan yang dibutuhkan.

Port 21: AREFF. Digunakan sebagai sumber tegangan yang dibutuhkan.

Port 22: GND. Digunakan sebagai ground.

Port 23: PC0 (ADC0). Digunakan sebagai perantara ke Header 4CON5 Port 2.

Port 24: PC2 (ADC1).

Port 25: PC2 (ADC2).

Port 26: PC4 (ADC4). Digunakan sebagai kontrol pada Serial to Paralel Shift Register 74HC595 pembacaan CLK. Untuk interupt dari Port 26 meliputi

Port 27: PC4 (ADC4). Digunakan sebagai kontrol pada Serial to Paralel Shift Register 74HC595 pembacaan LATCH.

Port 28: PC5 (ADC5). Digunakan sebagai kontrol pada Serial to Paralel Shift Register 74HC595 pembacaan DIN.

3.5.2. Rangkaian Reset

Rangkaian reset dirancang agar mempunyai kemampuan power on reset yaitu reset yang terjadi pada saat system di nyalakan untuk pertama kalinya. Reset juga dapat dilakukan secara manual dengan menambahkan tombol reset berupa switch button

Untuk me-*reset* mikrokontroler atmega8, maka pin Reset diberi logika tinggi selama sekurangnya dua siklus mesin (24 periode osilator). Untuk membangkitkan sinyal *reset* kapasitor dihubungkan dengan V_{CC} dan sebuah resistor yang dihubungkan ke *ground*. Karena kristal yang digunakan mempunyai frekuensi sebesar 4 MHz, maka satu periode dapat dihitung dari persamaan :

$$T = \frac{1}{f_{XTAL}} = \frac{1}{4MHz} s = 0{,}25 \text{ x } 10^{-6} \text{ s}$$

Sehingga waktu minimal logika tinggi yang dibutuhkan untuk m*ereset* mikrokontroller adalah :

reset (min) = T × periode yang dibutuhkan

$= 0{,}25 \times 10^{-6} \times 24 = 6\ \mu s$

Jadi mikrokontroller membutuhkan waktu minimal 6 μs untuk m*ereset*. Waktu minimal inilah yang dijadikan pedoman untuk menentukan nilai R dan C. Dengan menentukan nilai R = 10 kΩ maka :

$$T = 2 \times \pi \times R \times C$$

$$C = \frac{T}{2 \times \pi \times R}$$

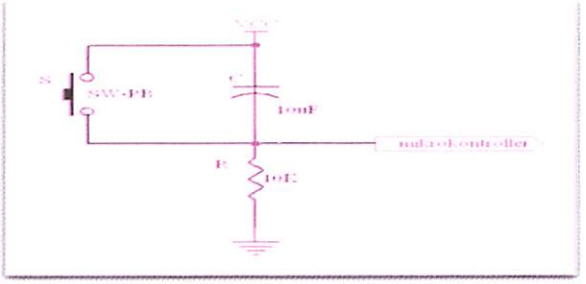
$$C = \frac{0{,}25 \times 10^{-6}}{2 \times 3{,}14 \times 10 \times 10^{3}}$$

$$C = 0.0039 \times 10^{-9}$$

$$C = 390 \text{ pF}$$

Jadi nilai komponen R = 10 kΩ dan C = 390 pf, namun C yang dipakai pada alat sebesar 10 μF, karena dengan C yang lebih besar maka akan lebih baik untuk menghilangkan bouncing.

Rangkaian reset ditunjukkan dalam gambar di bawah ini :

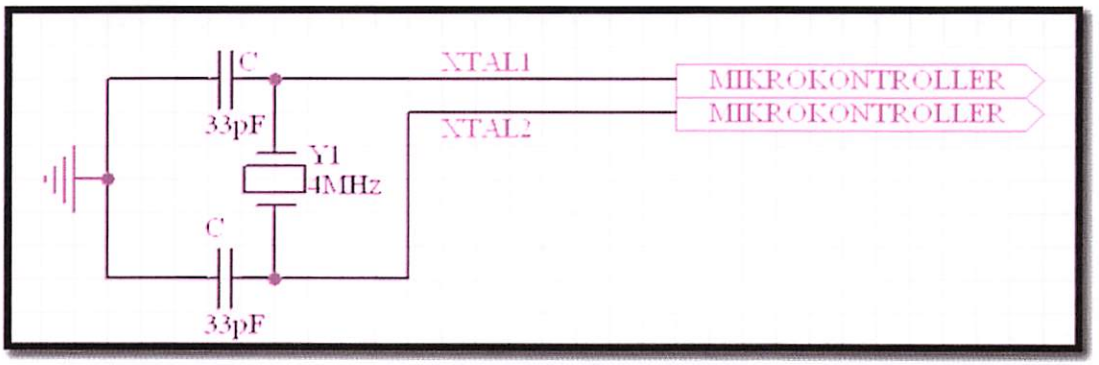


Gambar 3 - 3. Perencanaan Rangkaian Reset

3.5.3. Rangkaian Clock

Kecepatan proses yang diperlukan oleh mikrokontroller atmega8 ditentukan oleh sumber *clock* yang mengendalikan mikrokontroller tersebut. Untuk kristal *clock* dipasang Kristal dan resonator keramik yang berfungsi sebagai pembangkit *clock* osilator yang ada pada mikrokontroller. Rangkaian ini terdiri dari dua buah kapasitor dan sebuah kristal. Untuk mengendalikan frekuensi osilatornya cukup dengan menghubungkan Kristal pada pin 9 (P47/X_{out}) dan pin 10 (P46/X_{in}) serta dua buah kapasitor ke *ground.*

Dalam minimum kristal ini, menggunakan kristal 4 Mhz dan $C_1 = C_2$ yaitu sebesar 33 pF. Dengan rangkaian sebagai berikut :



Gambar 3 - 4. Perencanaan Rangkaian Clock

Dengan menggunakan nilai kristal dan kapasitor di atas maka dapat dihitung waktu yang diperlukan untuk 1 siklus mesin yaitu :

Diketahui : F = 4 MHz

$$T = \frac{1}{f}$$

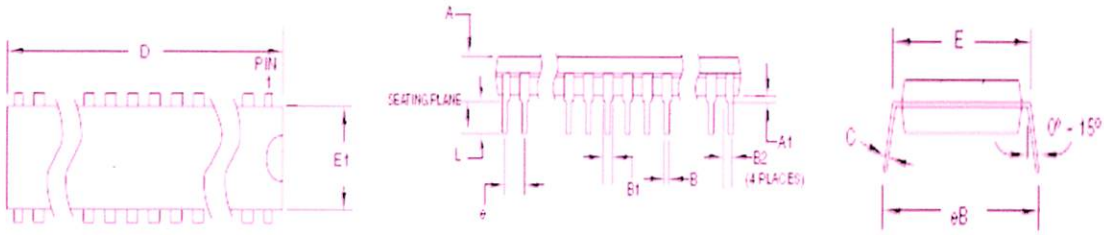
Maka $T = \frac{1}{4\ MHz} = \frac{1}{4}$ µs

Maka untuk 1 siklus mesin dari mikrokontroller atmega8 adalah sebesar:

$$T_m = 4 \times T$$

$$= 4 \times \frac{1}{4}\ \mu s = 1\ \mu s$$

Adapun dimensi fisik dari Mikrokontroler AVR ATMEL Atmega 8 adalah seperti gambar dibawah ini :



Gambar 3 - 5. Dimensi Fisik Mikrokontroler AVR ATMEL Atmega 8

Tabel 3 - 1. Keterangan Dimensi Fisik Mikrokontroler AVR ATMEL Atmega 8

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	4.5724	
A1	0.508	-	-	
D	34.544	-	34.798	Note 1
E	7.620	-	8.255	
E1	7.112	-	7.493	Note 1
B	0.381	-	0.533	
B1	1.143	-	1.397	
B2	0.762	-	1.143	
L	3.175	-	3.429	
C	0.203	-	0.356	
eB	-	-	10.160	
e	2.540 TYP			

3.5.4. Switched Capasitor Filter (MF 10).

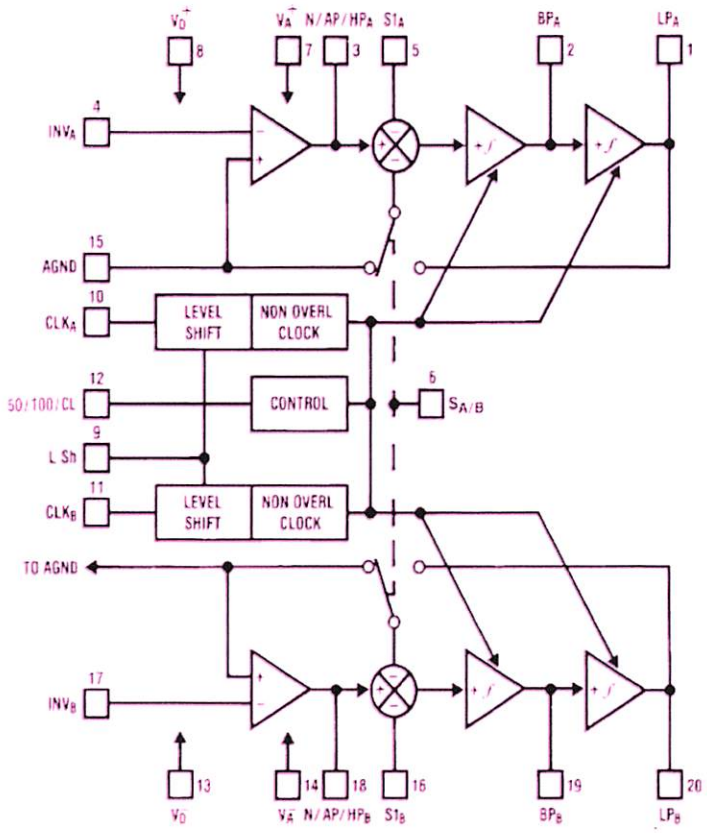
Komponen ini mempunyai fungsi utama sebagai penggerak saklar otomatis yang dioperasikan secara elektrik. Pada bagian ini akan bekerja setelah mendapat sinyal audio dari Buffer dan untuk fungsi saklar otomatis dikontrol oleh mikrokontroller AVR ATMEL Atmega 8.

Pada komponen ini dilengkapi dengan Low Pass Filter, Band Pass Filter, dan High Pass Filter. Filter yang digunakan dalam sistem adalh Band Pass Filter.

Band Pass Filter adalah suatu rangkaian yang khusus dirancang untuk hanya melewatkan isyarat dalam suatu lebar gelombang (Band With) pada frekuensi tertentu, dan menolak semua frekuensi dari lebar gelombang dari frekuensi yang dibatasi.

Lebar jalur sempit adalah sebuah filter yang memiliki bandwith lebih kecil dari sepersepuluh (/10) frekuensi resonan.(B < 0,1 ωr) dan factor kualitas (Q) lebih kecil dari rangkaian (Q < 10), sedangkan lebar jalur besar adalah sebuah filter yang memiliki bandwith lebih besar dari frekuensi resonan (B > 0,1 ωr) dan factor kualitas (Q) lebih besar dari rangkaian (Q > 10)

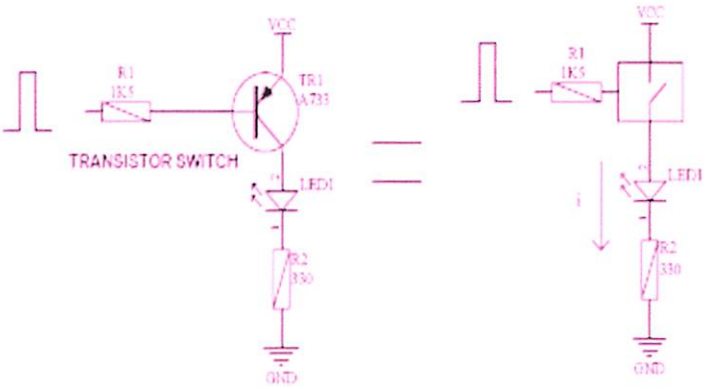
Pada Switched Capasitor Filter, band pass filter berada port 2 dan 19, seperti yang terlihat dibawah ini.



Gambar 3 - 6. Diagram Blok IC MF 10

3.5.5. Transistor Switch.

Pada perancangan dan pembuatan alat ini, transistor yang digunakan adalah PNP Silikon A733. Penggunaan komponen ini diharapkan dapat membantu fungsi kerja dari rangkaian dalam proses scanning display.



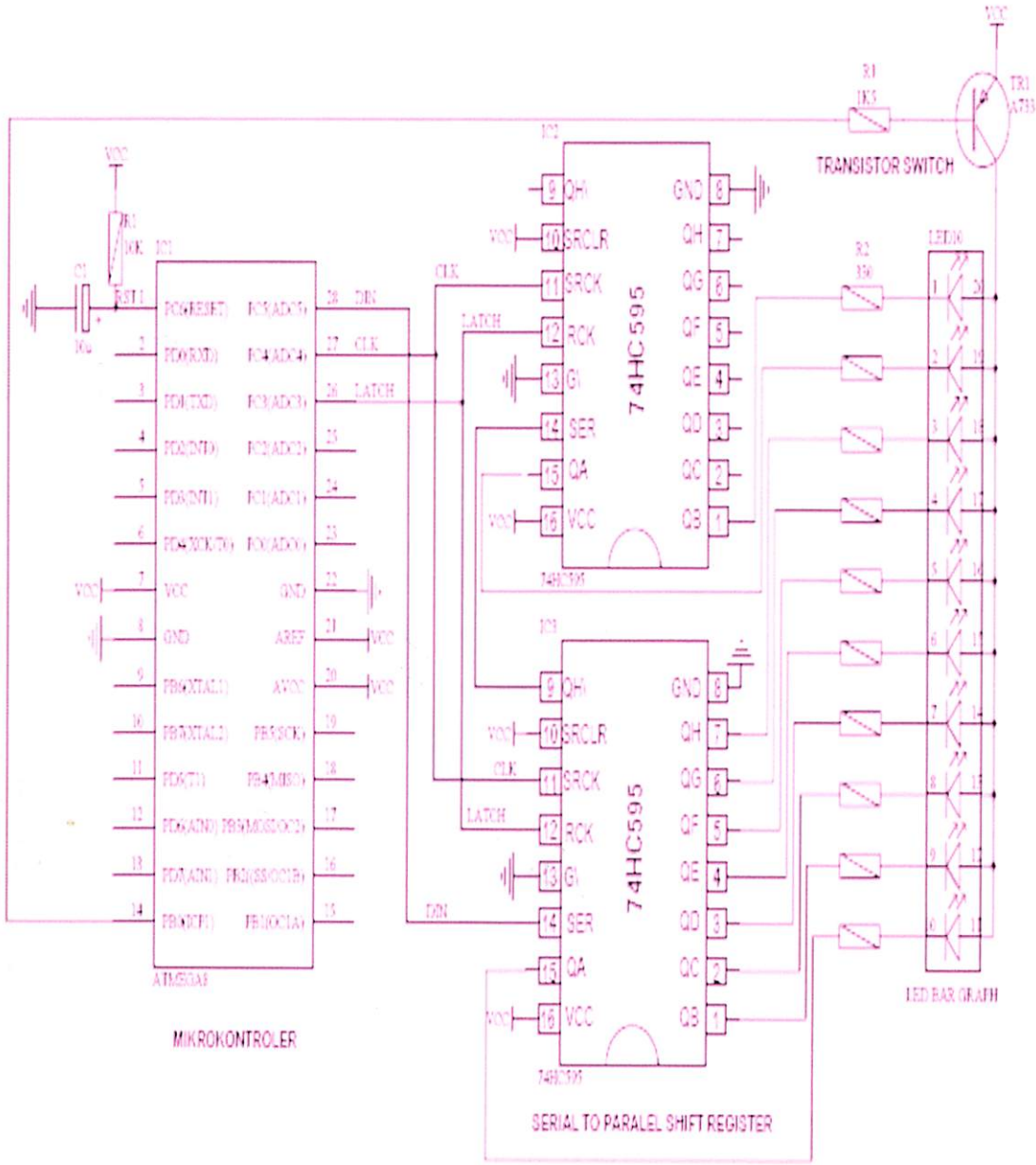
Gambar 3 - 7. Rangkaian Pengujian Transistor Switch.

3.5.6. Serial To Pararel Shift Register Motorolla 74HC595.

Pada perancangan dan pembuatan alat ini, Motorolla 74HC595 dikarenakan cukup memadai untuk mendukung system transfer data, dan memiliki real time yang cepat dan dilengkapi dengan port Data, Clock , dan Latch.

3.5.7. LED Array

Pada perancangan dan pembuatan alat ini, led array yang digunakan adalah Ledtech 10 Bit sebagai tampilan dari keluaran proses kerja Spektrum Audio Display 10 Band.

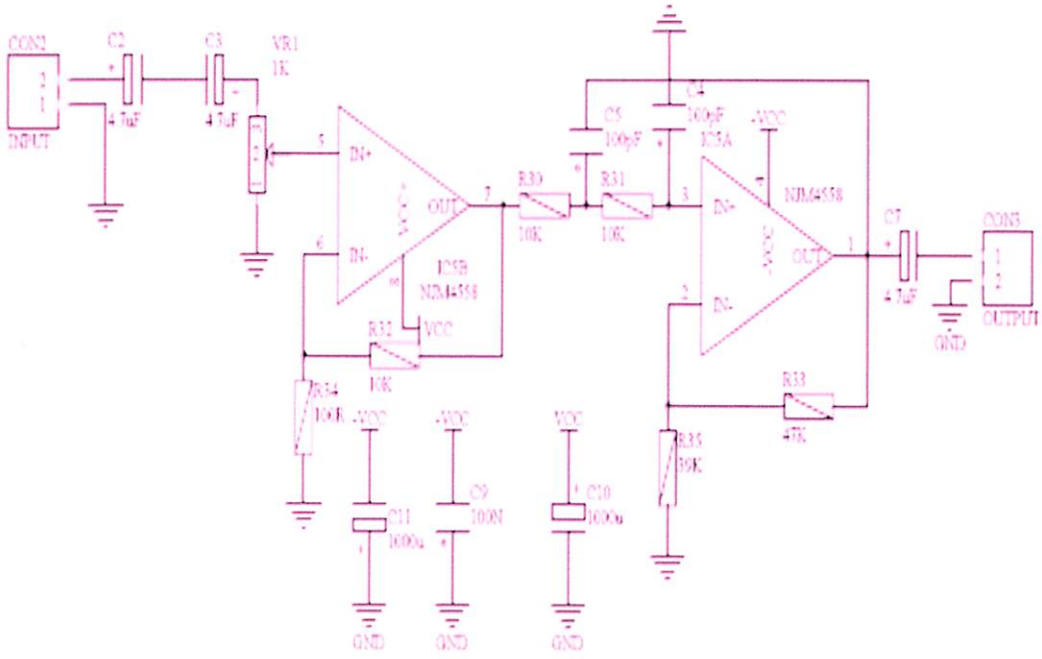


Gambar 3 - 8. Rangkaian Serial To Pararel Shift Register (74HC595), Transistor Switch (A733) Dan LED Array.

Rangkaian non inverting ampl.

3.5.8. Buffer.

Pada buffer terdapat rangkaian penguatan operasional amplifier yang terdiri dari penguat non-inverting, dimana input umpan balikan ke masukan positif untuk dikuatkan sesuai dengan arus yang dibutuhkan. Adapun rangkaian seperti gambar dibawah ini.



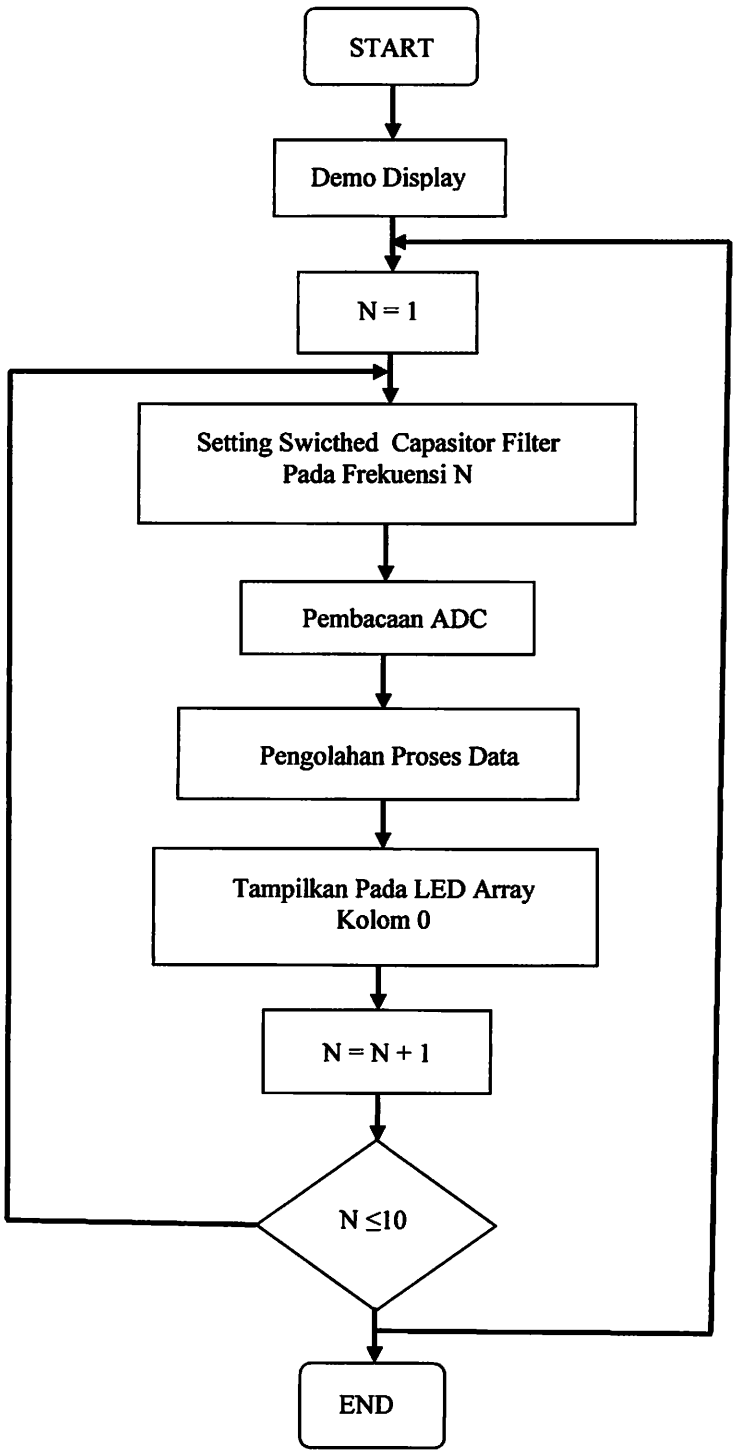
Gambar 3 - 9. Rangkaian Operasional Amplifier.

Perencanaan

3.7. Perencanaan Perangkat Lunak.

Perencanaan Perangkat Lunak diperlukan untuk menjalankan sistem sesuai dengan yang diharapkan. Untuk pemakaian mikrokontroller, perlu direncanakan perangkat lunak yang dapat mengatur system kerja operasional tersebut. Perangkat lunak disini adalah susunan perintah – perintah (program / software) didalam memori yang harus dikerjakan sebagai intruksi dari mikrokontroller.

Memori merupakan fasilitas utama karena disinilah disimpan perintah – perintah yang harus dikerjakan. Memori disini dapat dibedakan menurut fungsinya menjadi memori program dan memori data. Menurut letaknya memori dibedakan menjadi memori dalam dan memori luar. Memori luar diberikan apabila memori didalam mikrokontroller tidak mencukupi untuk menampung semua program dan data. Perencanaan perangkat lunak (Program / Software) didasarkan perencanaan perangkat keras (Hardware) yang telah dibuat sebelumnya, untuk mendapatkan ssstem kerja yang diharapkan oleh perangkat lunak dari alat tersebut terdapat di bagian lampiran dan untuk diagram alir (Flow Chart) dari alat tersebut adalah sebagai berikut :



Gambar 3 - 10. Flowchart Sistem Kerja.

BAB IV

PENGUKURAN DAN PENGUJIAN ALAT.

4.1. Umum

Setelah merancang keseluruhan sub-sistem selanjutnya dilakukan pengujian untuk mengetahui kerja masing-masing sub-sistem yang telah direncanakan. Setelah dilakukan pengujian terhadap masing-masing sub-sistem, selanjutnya seluruh sub-sistem tersebut digabungkan membentuk suatu sistem yang kemudian dilakukan pengujian sistem secara keseluruhan.Untuk memastikan sistem ini dapat bekerja sesuai dengan spesifikasi perencanaan, diperlukan serangkaian pengujian dan pengukuran.

Bab pengujian dan pengukuran ini menguraikan tentang bagian alat yang diuji, tujuan pengujian, langkah-langkah pengujian dan hasil pengujian yang menunjukkan unjuk kerja dari tiap-tiap bagian alat. Pembahasan dalam bab ini dibagi menurut pembagian alat yang diuji untuk mengetahui unjuk kerja sistem secara keseluruhan.

Pengujian sistem tersebut adalah pengujian perangkat keras (hardware) per blok dan alat secara keseluruhan. Berikut ini akan diberikan prosedur pengujian dan hasil pengamatan terhadap pengujian.

4.2. Tujuan Pengujian.

Pengujian pada masing-masing blok pada perencanaan dan pembuatan alat perancangan dan pembuatan alat spektrum audio 10 band berbasis switched kapasitor filter (mf 10) dicontrol mikrokontroller AVR ATMEL Atmega 8 ini bertujuan:

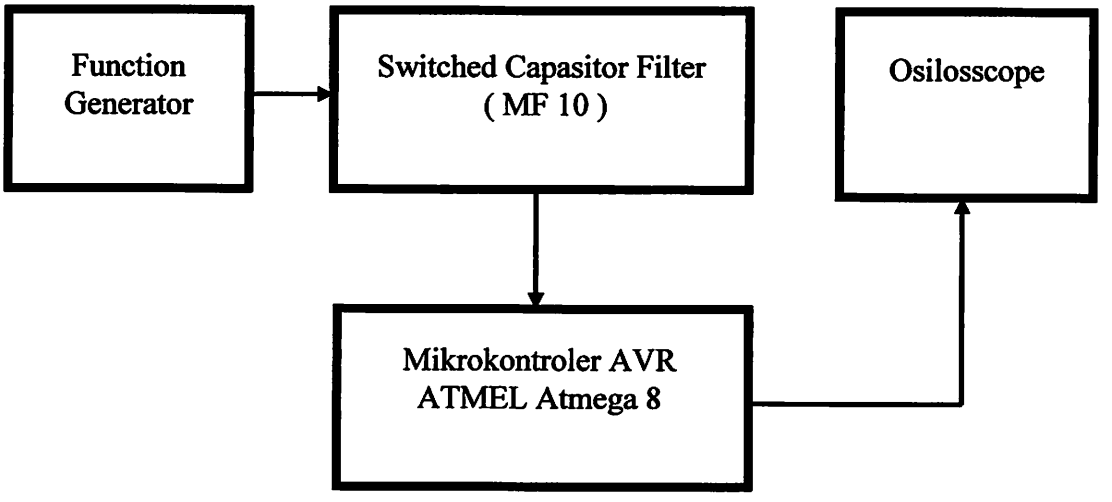
- Untuk mengetahui apakah tiap blok rangkaian dapat berfungsi dengan baik.
- Untuk mengetahui sistem kerja dengan menggunakan mikrokontroller ATMEGA 8 sebagai pengendali utama.

4.3. Pengujian Rangkaian Mikrokontroler AVR ATMEL Atmega 8 Dan Switched Capasitor Filter (IC MF 10).

Tujuan pengujian rangkaian Mikrokontroler AVR ATMEL Atmega 8 Dan Switched Capasitor Filter (MF 10) adalah untuk mengetahui sistem kerja rangkaian Switched Capasitor Filter (MF 10) dan respon terhadap lebar jalur pada frekuensi yang diinginkan.

Peralatan yang digunakan :

- Rangkaian Mikrokontroler AVR ATMEL Atmega 8 Dan Switched Capasitor Filter (MF 10).
- 1 Buah Function Generator.
- 1 Buah Osilosscope.

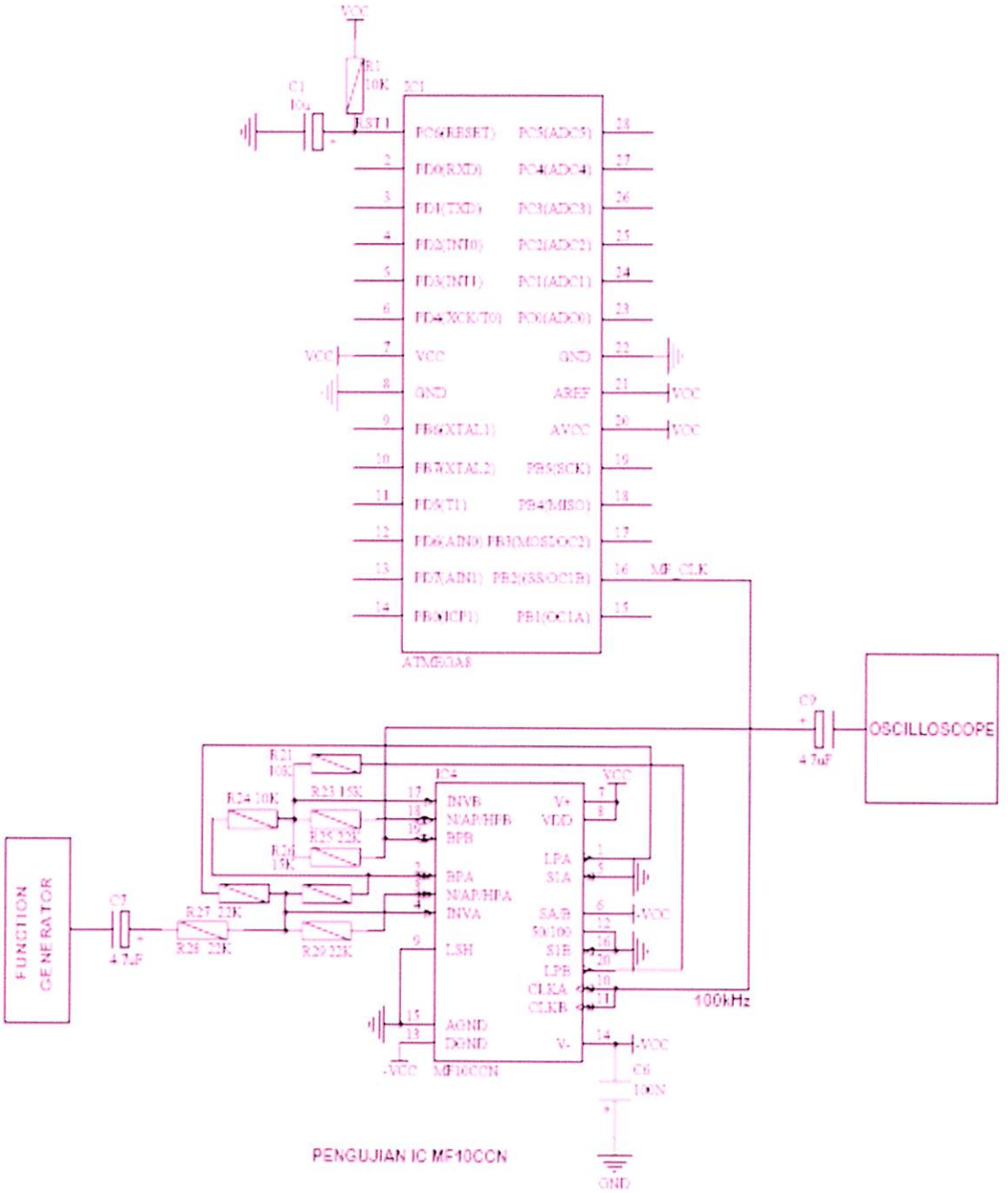


Gambar 4 - 1. Diagram Blok Pengujian Rangkaian Mikrokontroler AVR ATMEL Atmega 8 Dan Switched Capasitor Filter (IC MF 10).

Langkah – Langkah Pengujian Rangkaian Mikrokontroler AVR ATMEL Atmega 8 Dan Switched Capasitor Filter (MF 10) :

- Setting Function Generator pada frekuensi 100 Hz.
- Setting Ossilossope pada : T/Div = 2 μS.

  V/Div = 1 V.
- Menghubungkan dengan Switched Capasitor Filter (MF 10), dan Mikrokontroler AVR ATMEL Atmega 8.
- Mengaktifkan catu daya.
- Mengaktifkan listing program pengujian.
- Menghubungkan Switched Capasitor Filter (MF 10) dengan ossiloscope.
- Mengamati dan mengukur perubahan pada layar ossiloscope pada saat frekuensi diubah.



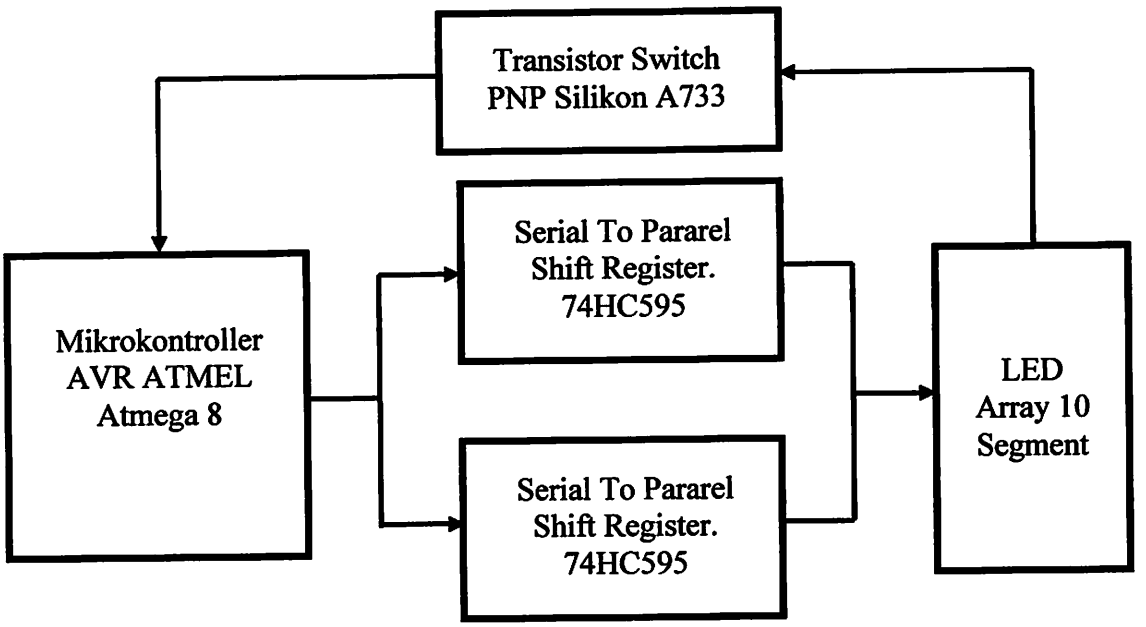
Gambar 4 - 2. Rangkaian Pengujian Mikrokontroler AVR ATMEL Atmega 8 Dan Switched Capasitor Filter (MF 10)

Listing program pengujian IC Switched Capasitor Filter (MF 10).

```
//=================================================================
//=================================================================
=================================================================
//      PENGUJIAN IC SWITCH CAPACITOR MF10CCN
// OLEH : ARY PRASOJO
// NIM  : 0117071
// TEKNIK ELEKTRO
// ITN - MALANG
//=================================================================
=================================================================

#include <mega8.h>
#include <delay.h>
#include <definisi.h>

// Timer 0 overflow interrupt service routine
interrupt [TIM0_OVF] void timer0_ovf_isr(void)
{
        TCNT0=0xF0;
        MF_CLOCK=~MF_CLOCK;
}

void jalan()
{
        OSCCAL=0x89; OCR1A=0X23; OCR1B=0X23;
 while(1);
}
```

4.4. Pengujian Rangkaian Serial To Pararel Shift Register Transistor Switch Dan LED Array.

Tujuan pengujian rangkaian Serial To Pararel Shift Register (74HC595), Transistor Switch Dan LED Array.adalah untuk mengetahui sistem kerja rangkaian, dimana saling mendukung untuk mendapatkan suatu system yang komplek. Adapun dapat ditunjujan dengan diagram blok dibawah ini :

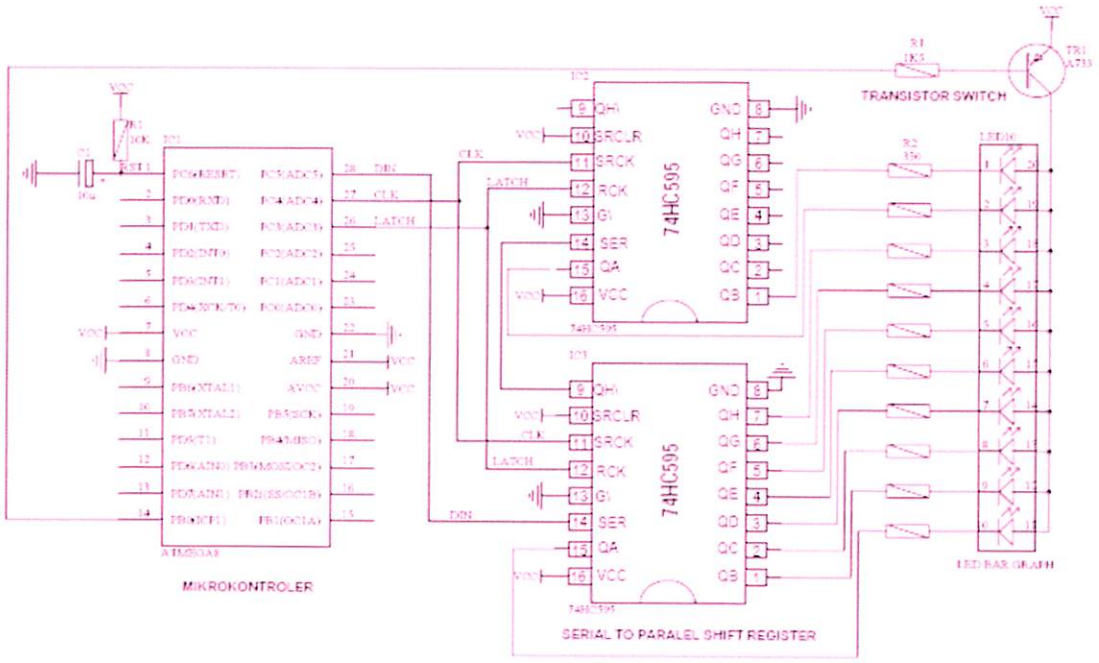


Gambar 4 - 8. Diagram Blok Pengujian Rangkaian Serial To Pararel Shift Register (74HC595), Transistor Switch (A733) Dan LED Array.

Langkah – Langkah Pengujian Rangkaian Serial To Pararel Shift Register (74HC595), Transistor Switch (A733) Dan LED Array :

- Menghubungkan rangkaian Pengujian Rangkaian Serial To Pararel Shift Register (74HC595), Transistor Switch (A733) Dan LED Array.
- Mengaktifkan catu daya.
- Mengaktifkan listing program pengujian.

- Mengaktifkan scanning display, dimana pada kondisi aktif maka transistor akan berada pada posisi off karena PNP, setelah mendapat masukan data dari Serial To Pararel Shift Register (74HC595), maka transistor dalam kondisi saturasi dimana scanning display akan berlangsung karena setiap mendapat masukan data, switch transistor aktif dengan posisi tutup, dan hanya ada 1 switch yang tertutup sedangkan yang lain terbuka.
- Menghubungkan dengan ossiloscope dan mengamati saat mendapat masukan data, clock dan latch.

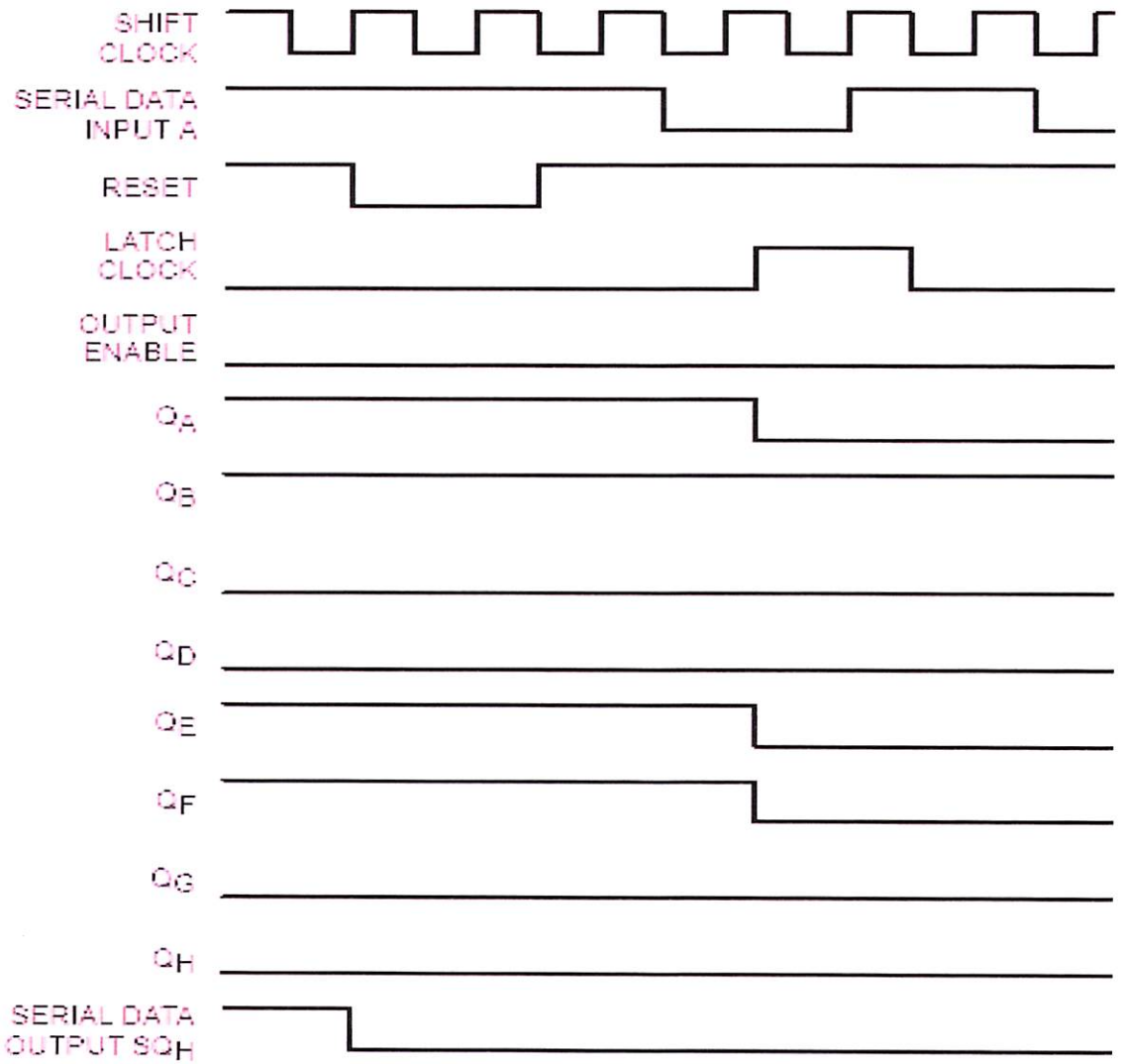


Gambar 4 - 9. Rangkaian Serial To Pararel Shift Register (74HC595), Transistor Switch (A733) Dan LED Array.

Listing program pengujian Rangkaian Serial To Pararel Shift Register (74HC595), Transistor Switch (A733) Dan LED Array.

```
//=================================================================
//=================================================================
//      PROGRAM PENGUJIAN IC SHIFT REGISTER SERIAL TO PARALEL
// DAN DISPLAY LED BAR GRAPH
// OLEH : ARY PRASOJO
// NIM  : 0117071
// TEKNIK ELEKTRO
// ITN - MALANG
//=================================================================
//=================================================================

#include <mega8.h>
#include <delay.h>

#definecolum1PORTD.5
#defineDIN              PORTC.5
#defineCLK              PORTC.3
#defineLATCH            PORTC.4

unsigned char n,m,j;

void kirim_data(unsigned char datane)
{
        j=11;DIN=1;
        while(j) {CLK=0; CLK=1; j--; }
        LATCH=0; LATCH=1;
```

```
        if(datane)
        {
                DIN=0;
                while(datane)
                {
                        CLK=0; CLK=1; datane--;
                }
                LATCH=0; LATCH=1;
        }
}

void start_up_demo()
{
// bar graph naik
        n=1;
        {
                while(n<11)
                {
                        kirim_data(n);
                        delay_ms(100);
                        n++;
                }
        }
}

void demoled()
{
        colum1=0;
        start_up_demo();
}
```



Gambar 4 - 10. Timming Diagram.

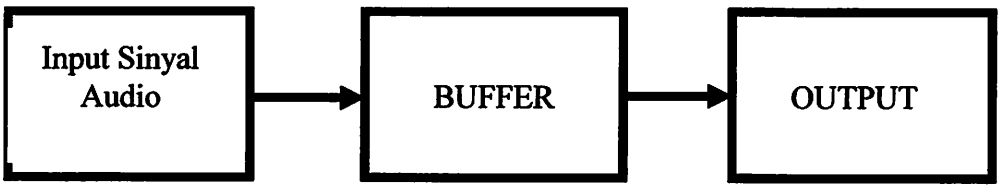
Kesimpulan Hasil Pengukuran Dan Pengujian Rangkaian Serial To Pararel Shift Register (74HC595), Transistor Switch (A733) Dan LED Array.

- Dibutuhkan real time dengan kecepatan tinggi untuk mendukung transfer data antar rangkaian.
- Pemasangan Serial To Pararel Shift Register (74HC595) secara ganda

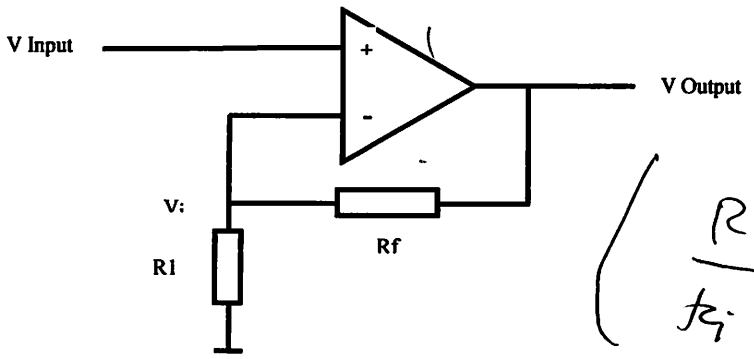
karena diperlukan port kaki tambahan untuk menunjang rangkaian LED array

4.5. Pengujian Rangkaian Operasional Amplifier.

Tujuan pengujian rangkaian Operasional Amplifier (OP-Amp) adalah untuk mengetahui sistem kerja rangkaian pada buffer dikarenakan sebagai penyangga utama atas masukan sinyal audio. Adapun seperti gambar diagram blok dibawah ini :



Gambar 4 - 11. Diagram Blok Rangkaian Operasional Amplifier.



$\left(\frac{Rf}{Ri}+1\right) =$

Gambar 4 - 12. Rangkaian Non - Inverting Amplifier.

Vi	Rf/Ri	Vout
5V	10	30 V

Hasil Perhitungan Pengujian Rangkaian Operasional Amplifier :

$$Vo = \left[1 + \frac{Rf}{R1}\right] Vi$$

$$= \left[1 + \frac{10\ K\Omega}{100\Omega}\right] 5V$$

$$= 2{,}5\ KV$$

$$Af = \frac{VO / VI}{1 + \frac{Rf}{R1}}$$

$$= \frac{2{,}5\ KV / 5\ V}{1 + \frac{10\ K\Omega}{100\ \Omega}}$$

$$= 10\ x$$

$$I = \frac{V}{R}$$

$$= \frac{3{,}3\ V}{330\ \Omega}$$

$$= 10\ mA$$

Kesimpulan Hasil Pengukuran Dan Pengujian Rangkaian Operasional Amplifier :

- Dari hasil perhitungan diperoleh bahwa :

$$\frac{VI - VO}{Rf} + \frac{Vi}{R1} = 0$$

4.6. Pengukuran Dan Pengujian Rangkaian Transistor Switch.

Tujuan pengukuran dan pengujian rangkaian transistor switch adalah untuk mengetahui sistem kerja rangkaian dalam menentukan scanning display pada proses yang berlangsung.

Peralatan yang dibutuhkan :

- 1 Buah Ossiloscope.
- Dataseet Transistor PNP Silikon A733

Langkah – Langkah Pengujian Rangkaian Transistor Swich :

- Menyiapkan dataseet dari transisitor A733 yang digunakan sebagai pembanding nilai dari hasil perhitungan.
- Aktifkan catu daya.
- Pengamatan data clock dari Mikrokontroller pada saat posisi saturasi dan off.
- Perbandingkan hasil pengukuran dengan hasil pada dataseet.

Hasil Perhitungan Pengujian Transistor Switch.

$$V_{R2} = VCC - V_{LED}$$

$$= 5\ V - 1{,}7\ V$$

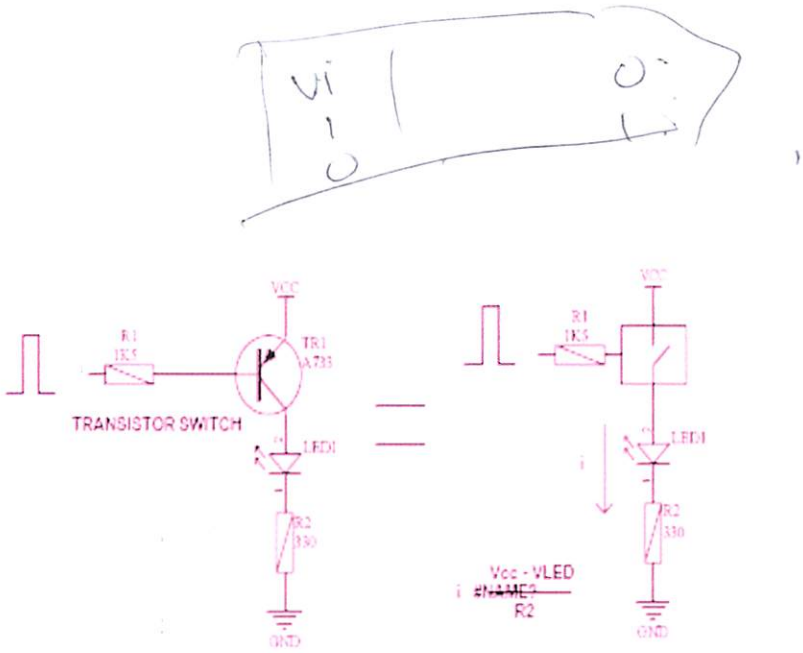
$$= 3{,}3\ V$$

$$I = \frac{V}{R}$$

$$= \frac{3{,}3\ V}{330\ \Omega}$$

$$= 10\ mA$$

bab III.



Gambar 4 – 13. Rangkaian Pengujian TransistorSwitch A733

Maka dapat diketahui hasil perbandingan perhitungan dan pengukuran :

$$7{,}4 > I_{LED} > 12{,}3$$

Jadi I_{LED} berada diantara nilai minimum dan nilai maksimum, berarti kondisi rangkaian Op-Amp normal.

Kesimpulan Hasil Pengukuran Dan Pengujian Rangkaian Transistor Switch :

- Rangkaian dalam kondisi normal apabila nilai I_{LED} berada diantara nilai minimum dan nilai maksimum dari nilai yang tertera pada dataseet.

BAB V
PENUTUP

5.1. Kesimpulan.

Dari Pengujian yang dilakukan dengan alat ini, maka dapat diambil kesimpulan :

1. *Output* frekuensi yang paling tinggi yang bisa dicapai pada alat ini adalah 60 Khz
2. Pada Frekuensi diatas 12 KHz terjadi sedikit penyimpangan dikarenakan transfer data antar register bersamaan.
3. Dari hasil pengujian didapatkan nilai error rata – rata pada pengujian DAC sebesar 0.08 %, error rata –rata pada pengujian frekuensi bentuk gelombang segitiga sebesar 0.05 %, error rata –rata pada pengujian frekuensi bentuk gelombang kotak 0.1625 % dan error rata –rata pada pengujian frekuensi bentuk gelombang sinus sebesar 0.4 %.
4. Perangkat lunak yang dibuat dapat beroperasi sesuai dengan fungsinya yaitu dapat menerima sinyal masukan dari perangkat-perangkat keras, mengolahnya dan kemudian menampilkan hasil pengolahan ke layar penampil (LED Array).

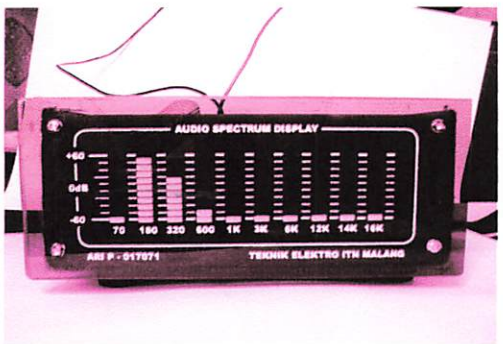
5.2. Saran.

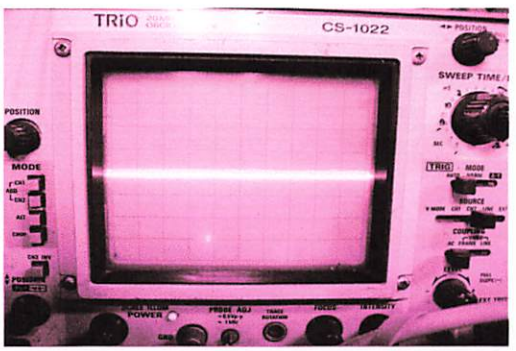
1. Untuk Pengembangan alat ini range frekuensinya bisa dinaikkan lagi, dan outputnya gelombangnya bisa ditambahkan
2. Agar alat ini dapat bekerja dengan lebih baik, sebaiknya menggunakan komponen-komponen yang lebih baik dan lebih sensitive .
3. Untuk pengembangan lebih lanjut, sebaiknya alat ini dihubungkan langsung ke komputer sehingga dapat dijadikan data base dan hasil pengukuran juga dapat langsung dicetak.

4. Sebaiknya rentan Frekuensi jangan terlalu dekat dikarenakan dalam pengukuran akan mendekati nilai sebelum dasesudahnya dikarenakan factor trial error.

Hasil Pengujian Dan Pengukuran :

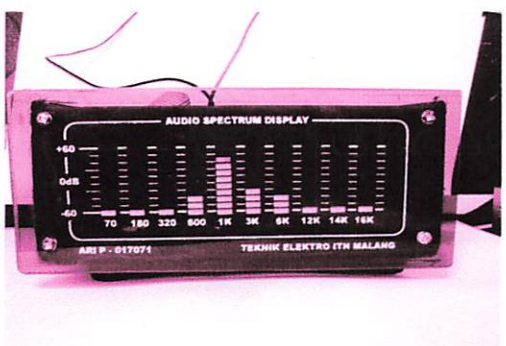
Pada frekuensi 180 Hz.

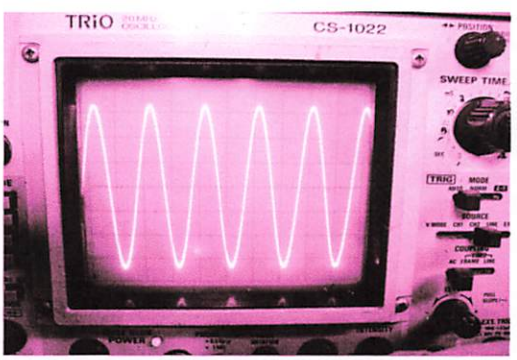




Gambar 4 - 3. Hasil Pengukuran Dan Pengujian Pada Frekuensi 180 Hz.

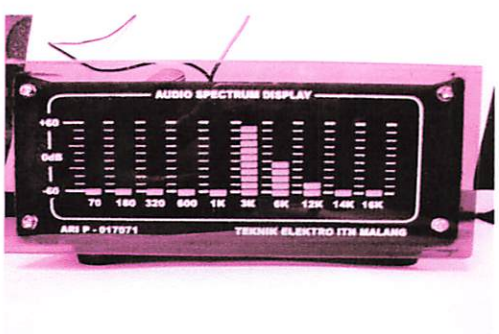
Pada Frekuensi 1 KHz.

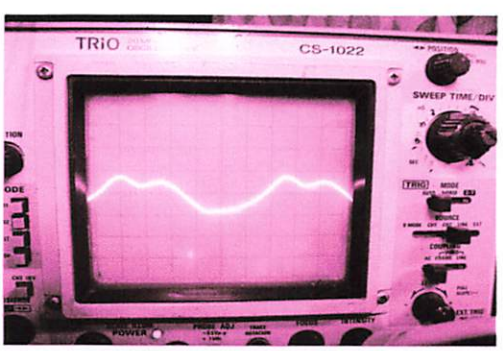




Gambar 4 - 4. Hasil Pengukuran Dan Pengujian Pada Frekuensi 1 KHz.

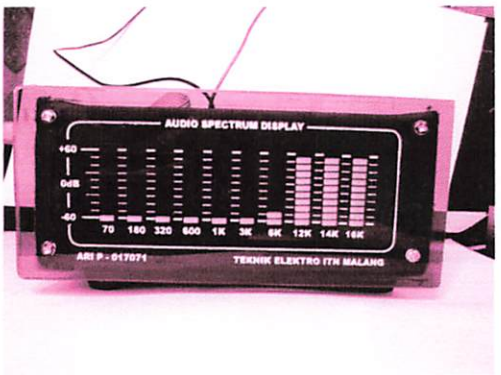
Pada Frekuansi 3 KHz.

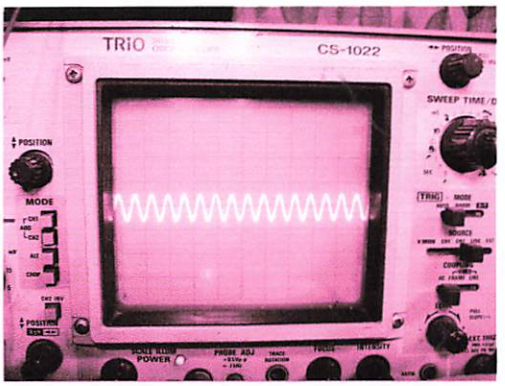




Gambar 4 - 5. Hasil Pengukuran Dan Pengujian Pada Frekuensi 3 KHz.

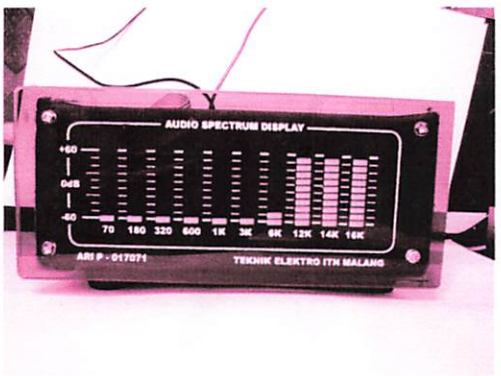
Pada Frekuensi 12 KHz.

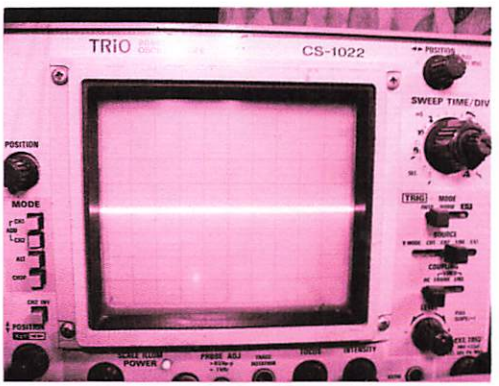




Gambar 4 - 6. Hasil Pengukuran Dan Pengujian Pada Frekuensi 12 KHz.

Pada Frekuensi 16 KHz.





Gambar 4 - 7. Hasil Pengukuran Dan Pengujian Pada Frekuensi 16 KHz.

Kesimpulan Hasil Pengukuran Dan Pengujian Mikrokontroler AVR ATMEL Atmega 8 Dan Switched Capasitor Filter (MF 10).

- Respon keluaran dari rangkaian menunjukkan fungsi yang sesuai dengan aplikasi, yaitu memberikan respon yang sesuai dengan masing – masing frekuensi yang diuji.
- Posisi terbaik dari frekuensi yang dicoba adalah 1 KHz, dimana terlihat lebar bandwith rata dengan munculnya lereng secara seimbang.

DAFTAR PUSTAKA

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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

LEMBAR BIMBINGAN SKRIPSI

Nama	: Ary Prasojo
Nim	: 01.17.071
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Judul Skripsi	: PERANCANGAN DAN PEMBUATAN ALAT SPEKTRUM AUDIO 10 BAND BERBASIS SWITCHED CAPASITOR FILTER (MF 10) DICONTROL MIKROCONTROLLER ATMEL AVR ATMEGA 8

Tanggal Mengajukan Skripsi	: 03 Desember 2008
Tanggal Menyelesaikan Skripsi	: 18 Maret 2009
Dosen Pembimbing	: Ir. F. Yudi Limpraptono, MT
Telah Dievaluasi Dengan Nilai	: 80 (Delapan Puluh)

Malang, Maret 2009

Mengetahui,	Menyetujui,
Ketua Jurusan Elektro	Dosen Pembimbing
Ir. F. Yudi Limpraptono, MT	Ir. F. Yudi Limpraptono, MT
NIP. P. 1039500274	NIP. P. 1039500274

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KONSENTRASI TEKNIK ELEKTRONIKA

BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

Nama Mahasiswa	:	ARY PRASOJO
N.I.M.	:	01.17.071
Jurusan	:	Teknik Elektro S-1
Konsentrasi	:	Teknik Elektronika
Judul Skripsi	:	PERANCANGAN DAN PEMBUATAN ALAT SPEKTRUM AUDIO 10 BAND BERBASIS SWITCHED CAPASITOR FILTER (MF 10) DICONTROL MICROCONTROLLER ATMEL AVR ATMEGA 8

Dipertahankan dihadapan Majelis Penguji Skripsi Jenjang Strata Satu (S-1)

Hari	:	Selasa.
Tanggal	:	24 Maret 2009
Dengan Nilai	:	80,50

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Panitia Ujian

(Ir. Sidik Noertjahjono, MT)
Ketua

(Ir. F. Yudi Limpraptono, MT)
Sekretaris

Anggota Penguji

(Joseph Deddy Irawan ST, MT)
Penguji Pertama

(I. Komang Somawirata, ST, MT)
Penguji Kedua

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JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR BIMBINGAN SKRIPSI

Nama : **ARY PRASOJO**
Nim : **01.17.071**
Masa Bimbingan :
Judul Skripsi : PERANCANGAN DAN PEMBUATAN ALAT SPEKTRUM AUDIO 10 BAND BERBASIS SWITCHED CAPASITOR FILTER (MF 10) DICONTROL MICROCONTROLLER ATMEL AVR ATMEGA 8

No.	Tanggal	Uraian	Paraf Pembimbing
1.		Bab I : - Perbaiki Sistematika Penulisan - Perbaiki Rumusan Masalah dan Tujuan	
2.		Bab II : - Perbaiki Teori Dasar	
3.		Bab III : - Perbaiki *Flowchart*	
4.		Bab IV : - Tampilkan Tabel Hasil Uji Pengukuran	
5.		Bab V : - Perbaiki Kesimpulan - Perbaiki Daftar Pustaka	
6.		Buat Makalah Seminar Hasil	
7.		Acc Seminar Hasil	
8.			25/05/09

Malang, 28 Mei 2009
Dosen Pembimbing,

Ir. F. Yudi Limpraptono, MT
NIP. P. 1039500274

Form.S-4b

15 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion 0.003% Typ
- Low Noise V_n = 18 nV/√Hz Typ at f = 1 kHz
- High Input Impedance . . . JFET Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/µs Typ
- Common-Mode Input Voltage Range Includes V_{CC+}

description

The JFET-input operational amplifiers in the TL07_ series are designed as low-noise versions of the TL08_ series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07_ series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

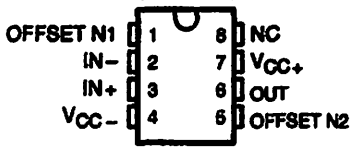
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

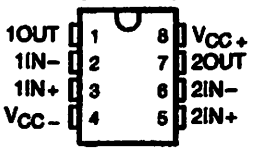
T_A	V_{IO}max AT 25°C	PACKAGE							
		SMALL OUTLINE (D)†	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP PACKAGE (PW)	FLAT PACKAGE (W)
0°C to 70°C	10 mV	TL071CD	—	—	—	—	TL071CP	TL071CPWLE	—
	6 mV	TL071ACD					TL071ACP	—	
	3 mV	TL071BCD					TL071BCP	—	
	10 mV	TL072CD	—	—	—	—	TL072CP	TL072CPWLE	—
	6 mV	TL072ACD					TL072ACP	—	
	3 mV	TL072BCD					TL072BCP	—	
	10 mV	TL074CD	—	—	—	TL074CN	—	TL074CPWLE	—
	6 mV	TL074ACD				TL074ACN		—	
	3 mV	TL074BCD				TL074BCN		—	
−40°C to 85°C	6 mV	TL071ID	—	—	—	—	TL071IP	—	—
		TL072ID				—	TL072P		
		TL074ID				TL074IN	—		
−55°C to 125°C	6 mV	—	TL071MFK	—	TL071MJG	—	—	—	—
	6 mV		TL072MFK	—	TL072MJG				—
	9 mV		TL074MFK	TL074MJ	—				TL074MW

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL071CDR). The PW package is only available left-ended taped and reeled (e.g., TL072CPWLE).

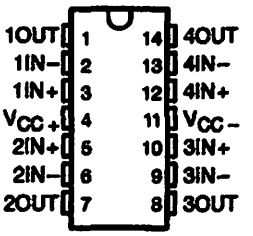
TL071, TL071A, TL071B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



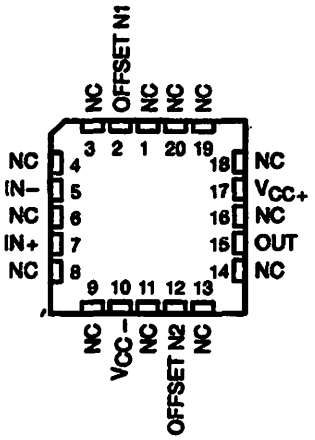
TL072, TL072A, TL072B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



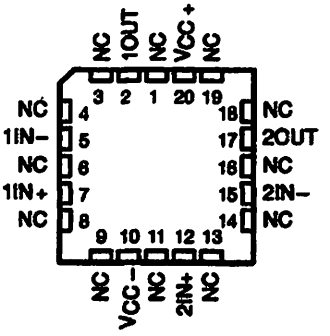
TL074, TL074A, TL074B
D, J, N, OR PW PACKAGE
TL074 . . . W PACKAGE
(TOP VIEW)



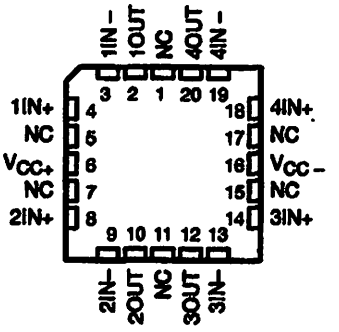
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)



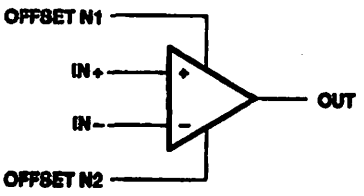
TL074
FK PACKAGE
(TOP VIEW)



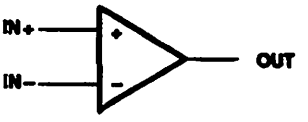
NC – No internal connection

symbols

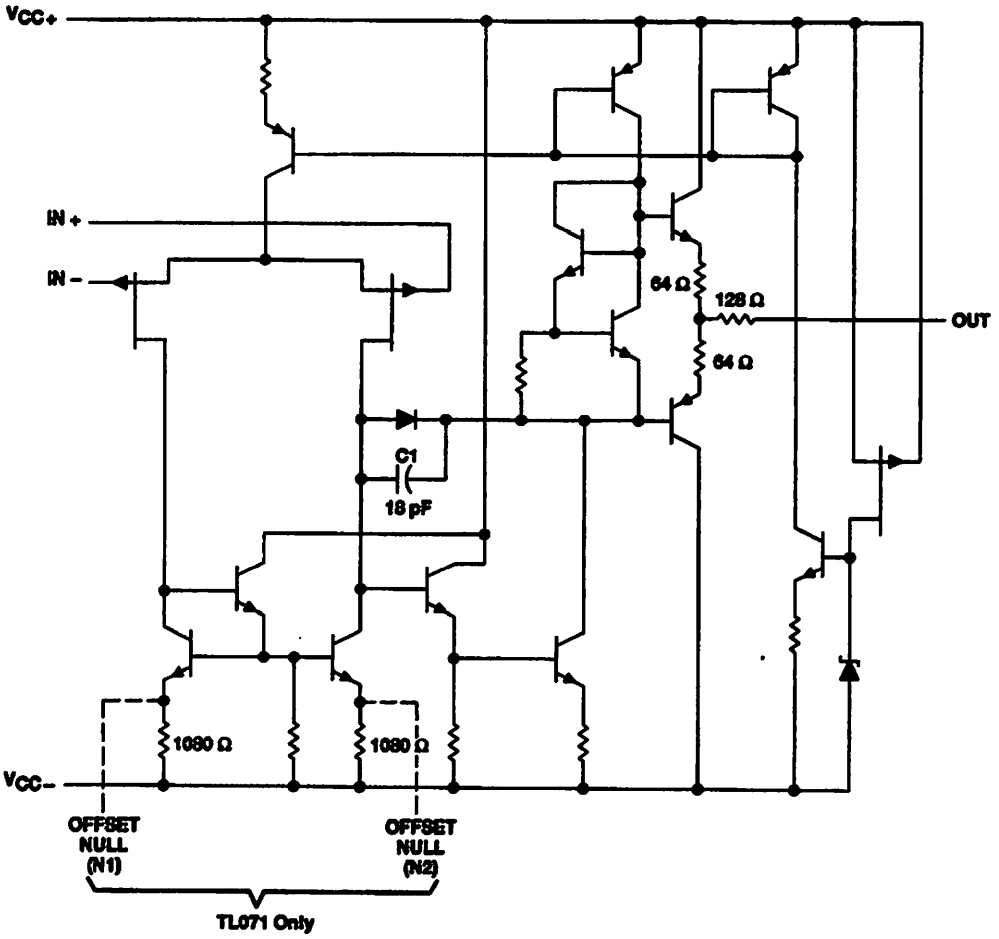
TL071



TL072 (each amplifier)
TL074 (each amplifier)



schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	8
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 18 V
Supply voltage, V_{CC-} (see Note 1) ..... −18 V
Differential input voltage, V_{ID} (see Note 2) ..... ±30 V
Input voltage, V_I (see Notes 1 and 3) ..... ±15 V
Duration of output short-circuit (see Note 4) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or W package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, or PW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
D (14 pin)	680 mW	7.6 mW/°C	60°C	608 mW	494 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	598 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
PW (8 pin)	525 mW	4.2 mW/°C	70°C	525 mW	N/A	N/A
PW (14 pin)	700 mW	5.6 mW/°C	70°C	700 mW	N/A	N/A
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071C TL072C TL074C			TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			TL071I TL072I TL074I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	10		3	6		2	3		3	6	mV
			Full range			13			7.5			5			8	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		μV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100		5	100		5	100	pA
			Full range			10			2			2			2	nA
I_{IB}	Input bias current§	V_O = 0	25°C		65	200		65	200		65	200		65	200	pA
			Full range			7			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			25			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	70	100		75	100		75	100		75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	70	100		80	100		80	100		80	100		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡ Full range is T_A = 0°C to 70°C for TL07_C,TL07_AC, TL07_BC and is T_A = −40°C to 85°C for TL07_I.
§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071M TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	Full range		18			18		µV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		5	100		5	100	pA
			Full range			20			20	nA
I_{IB}	Input bias current‡	$V_O = 0$	25°C		65	200		65	200	pA
						50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ	25°C	±12	±13.5		±12	±13.5		V
		$R_L \geq 10$ kΩ	Full range	±12			±12			
		$R_L \geq 2$ kΩ		±10			±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \geq 2$ kΩ	25°C	35	200		35	200		V/mV
				15			15			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ±15 V, $V_O = 0$, $R_S = 50\ \Omega$	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	$V_O = 0$, No load	25°C		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120		dB

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

‡ All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range is $T_A = -55°C$ to 125°C.

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electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T_A‡	TL071, TL071A, TL071B, TL072, TL072A, TL072B, TL074, TL074A, TL074B			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	V_{O} = 0, R_{S} = 50 Ω	25°C		3	15	mV
		Full range			20	
α_{VIO} Temperature coefficient of input offset voltage	R_{S} = 50 Ω	Full range		18		μV/°C
I_{IO} Input offset current	V_{O} = 0	25°C		5	100	pA
		Full range			20	nA
I_{IB} Input bias current	V_{O} = 0	25°C		65	200	pA
		Full range			20	nA
V_{ICR} Common-mode input voltage range		25°C	±11	+15 −12		V
V_{OM} Maximum peak output voltage swing	R_{L} = 10 kΩ	25°C	±12	±13.5		V
	R_{L} = 2 kΩ	Full range	±10	±12.7		
	R_{L} = 10 kΩ		±12			
A_{VD} Large-signal differential voltage amplification	V_{O} = ±10 V, R_{L} = 2 kΩ	25°C	25	100		V/mV
		Full range	15			
B_{1} Unity-gain bandwidth		25°C		3		MHz
r_{i} Input resistance		25°C		10¹²		Ω
$CMRR$ Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_{O} = 0, R_{S} = 50 Ω	25°C	80	86		dB
k_{SVR} Supply voltage rejection ratio ($\Delta V_{CC\pm}$/ΔV_{IO})	$V_{CC\pm}$ = ±9 V to ±15 V, V_{O} = 0, R_{S} = 50 Ω	25°C	80	86		dB
I_{CC} Supply current (per amplifier)	V_{O} = 0, No load	25°C		1.4	2.8	mA
P_{D} Total power dissipation	V_{O} = 0, No load	25°C		42		mW

†All characteristics are measured under open-loop operation. Junction temperature rises will also occur under high-speed operation or when driving a low-impedance load. For change in V_{IO} vs temperature, see Figure 4. Power bandwidth must be kept low enough so that the peak output current does not exceed the maximum rated output current.

‡Full range is −40°C to 125°C.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL07xM			ALL OTHERS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_I = 10$ V, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1	5	13		8	13		V/µs
t_r	Rise time overshoot factor	$V_I = 20$ mV, $C_L = 100$ pF,	$R_L = 2$ kΩ, See Figure 1		0.1			0.1		µs
					20%			20%		
V_n	Equivalent input noise voltage	$R_S = 20$ Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		µV
I_n	Equivalent input noise current	$R_S = 20$ Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_{O(RMS)} = 10$ V, $R_L \geq 2$ kΩ,	$R_S \leq 1$ kΩ, f = 1 kHz		0.003%			0.003%		

PARAMETER MEASUREMENT INFORMATION

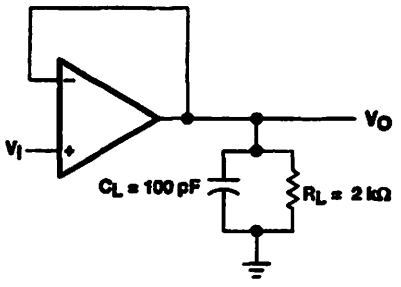

Figure 1. Unity-Gain Amplifier

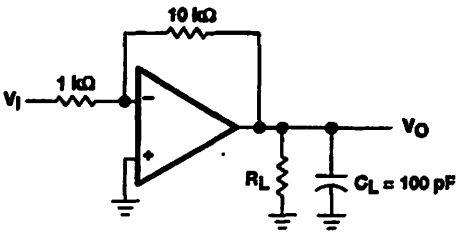

Figure 2. Gain-of-10 Inverting Amplifier

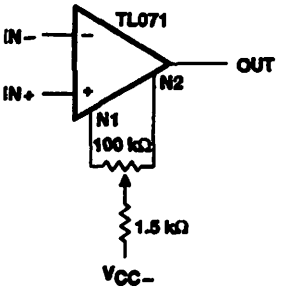

Figure 3. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	4
V_{OM}	Maximum output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	5, 6, 7 8 9 10
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	11 12
	Phase shift	vs Frequency	12
	Normalized unity-gain bandwidth	vs Free-air temperature	13
	Normalized phase shift	vs Free-air temperature	13
CMRR	Common-mode rejection ratio	vs Free-air temperature	14
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	15 16
P_D	Total power dissipation	vs Free-air temperature	17
	Normalized slew rate	vs Free-air temperature	18
V_n	Equivalent input noise voltage	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20
	Large-signal pulse response	vs Time	21
V_O	Output voltage	vs Time	22

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TYPICAL CHARACTERISTICS†

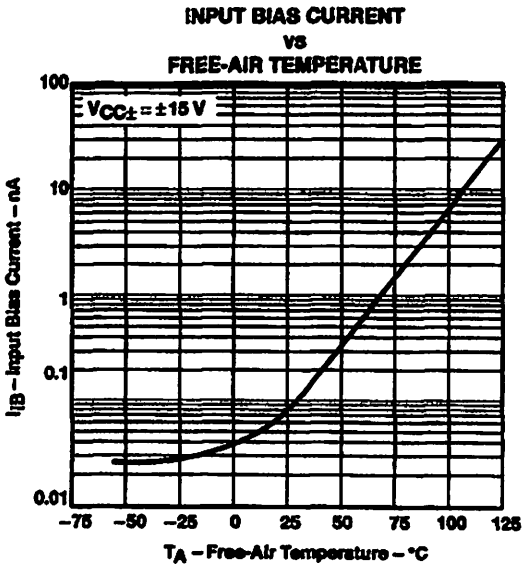


Figure 4

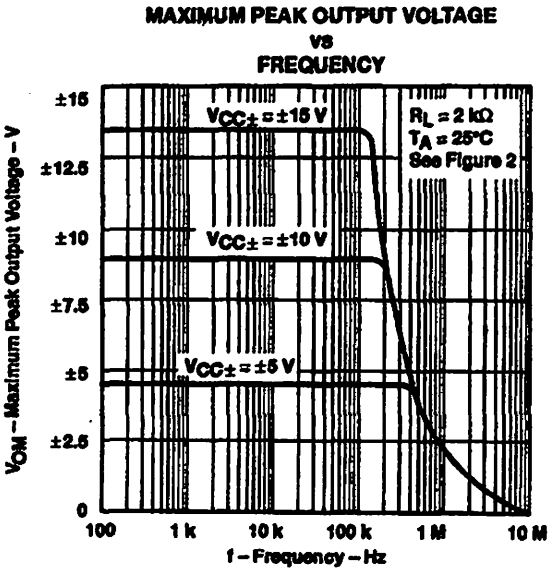


Figure 5

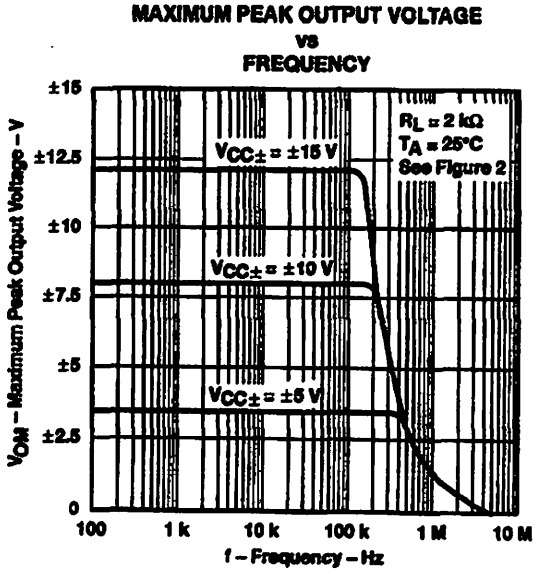


Figure 6

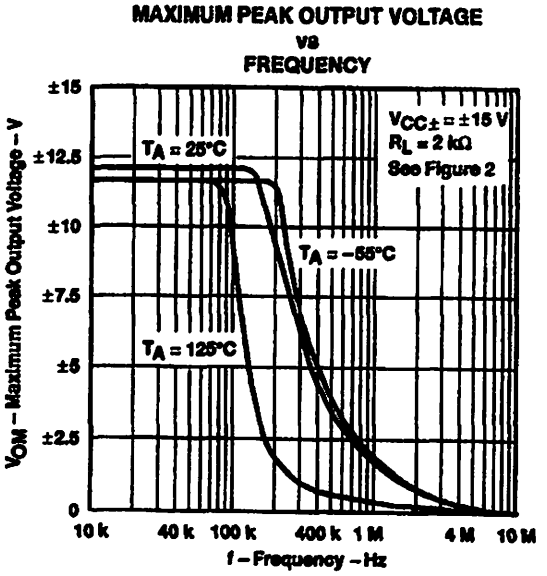


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

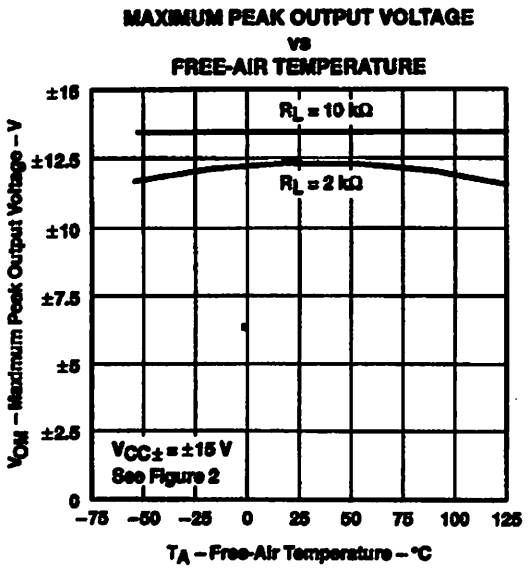


Figure 8

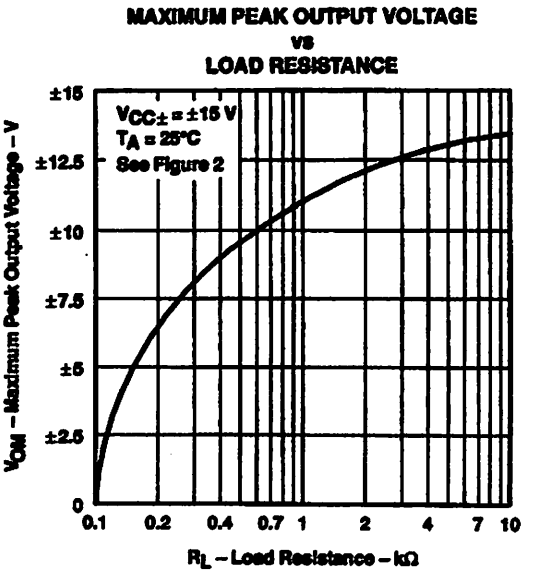


Figure 9

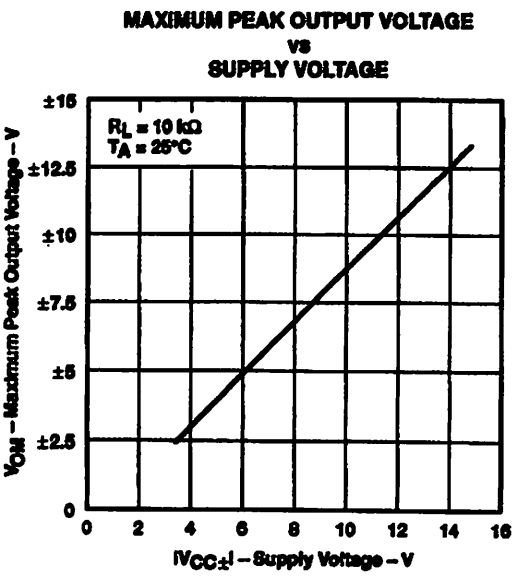


Figure 10

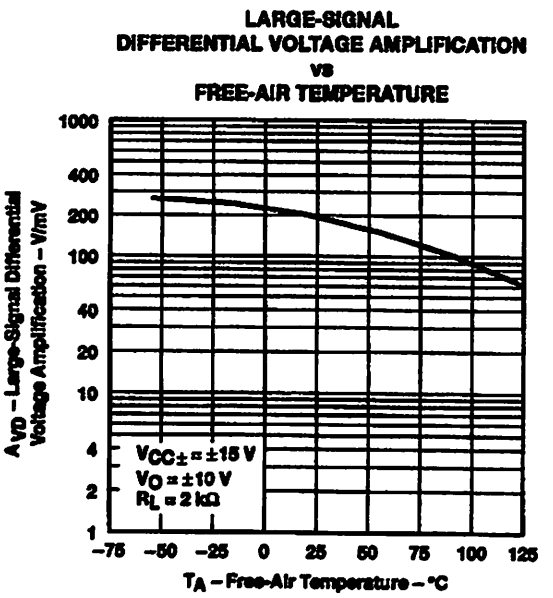


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

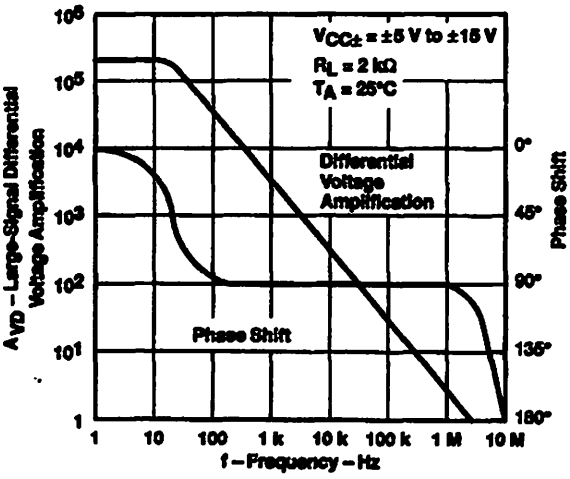


Figure 12

NORMALIZED UNITY-GAIN BANDWIDTH AND PHASE SHIFT vs FREE-AIR TEMPERATURE

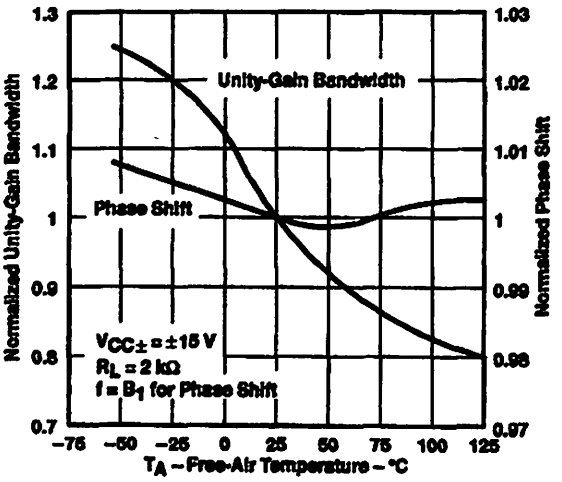


Figure 13

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

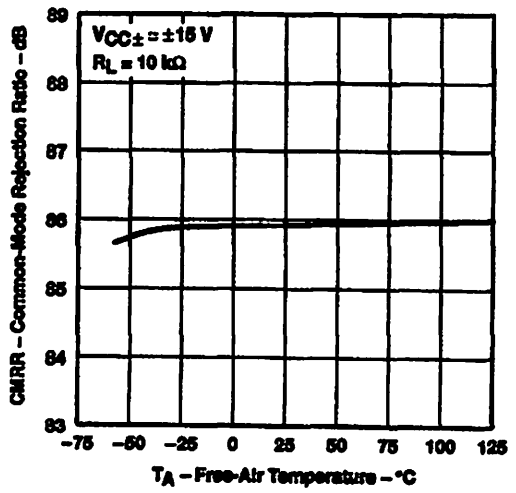


Figure 14

SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

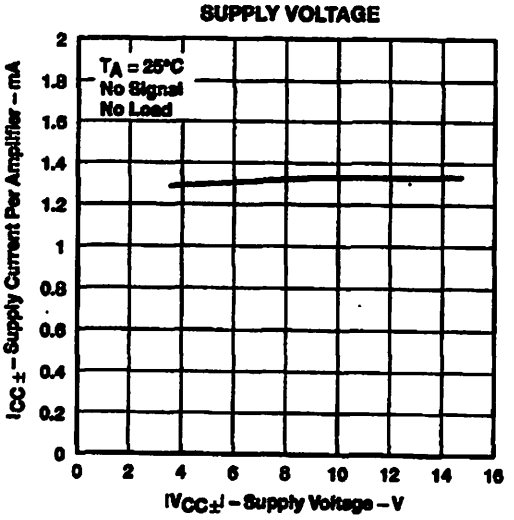


Figure 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

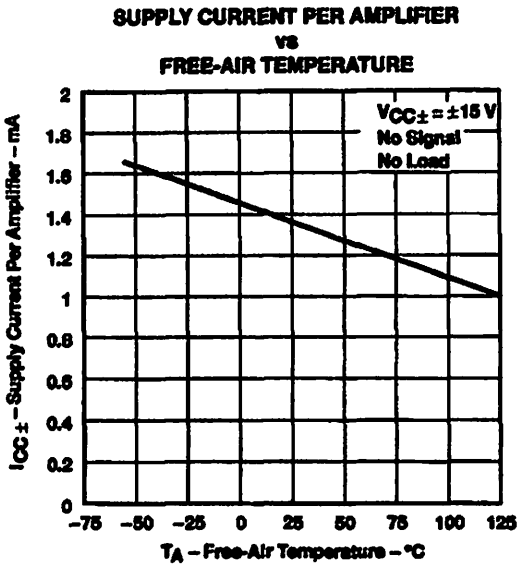


Figure 16

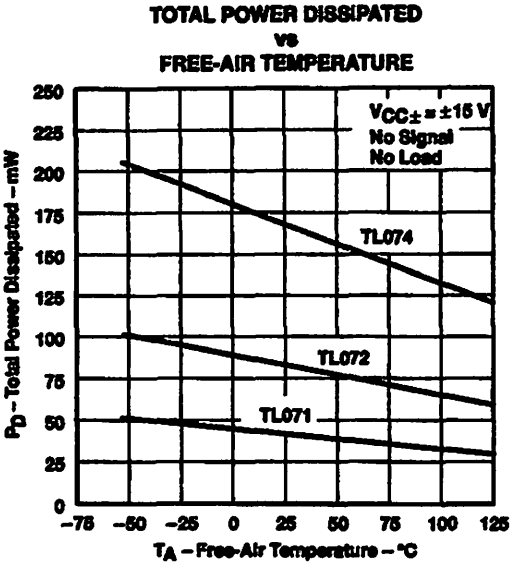


Figure 17

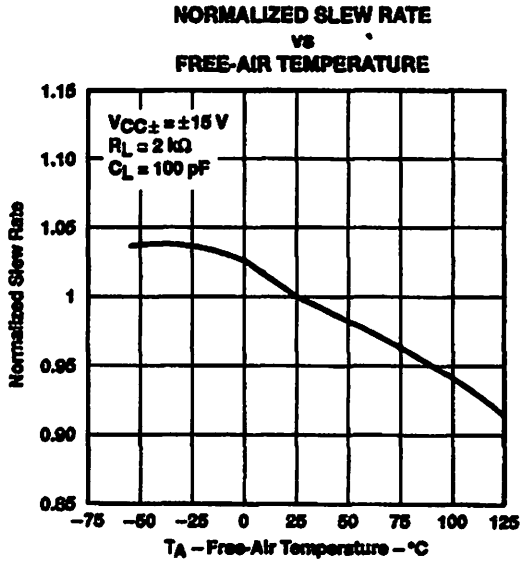


Figure 18

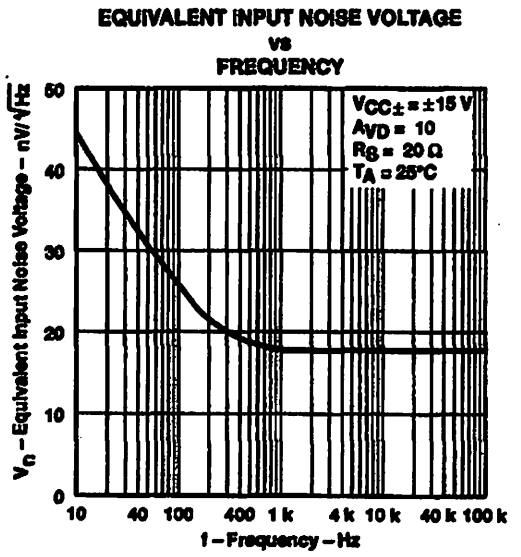


Figure 19

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

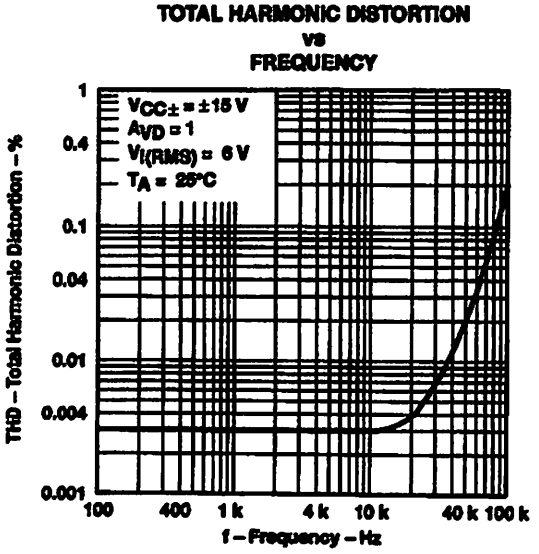


Figure 20

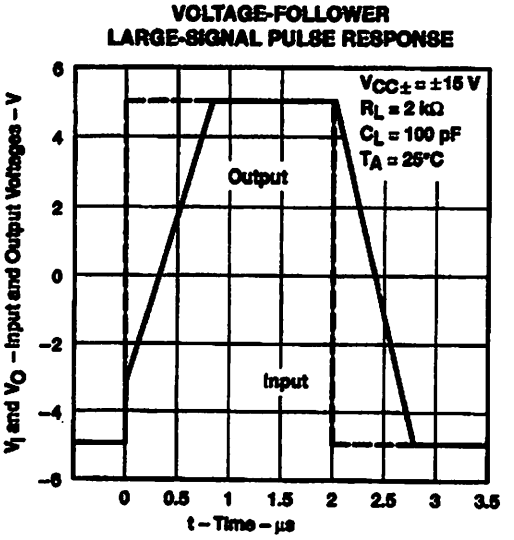


Figure 21

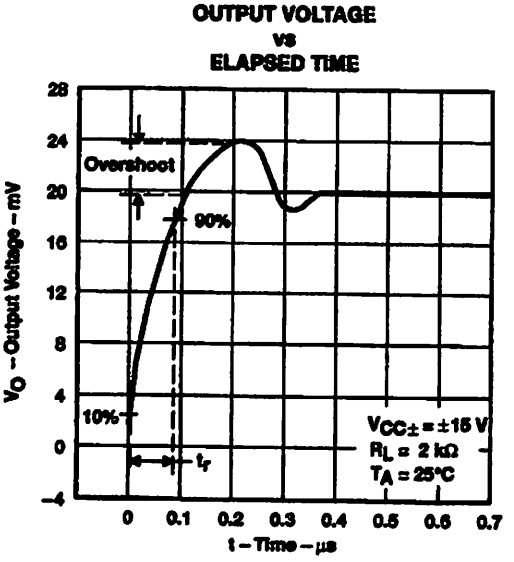


Figure 22

APPLICATION INFORMATION

Table of Application Diagrams

APPLICATION DIAGRAM	PART NUMBER	FIGURE
0.5-Hz square-wave oscillator	TL071	23
High-Q notch filter	TL071	24
Audio-distribution amplifier	TL074	25
100-kHz quadrature oscillator	TL072	26
AC amplifier	TL071	27

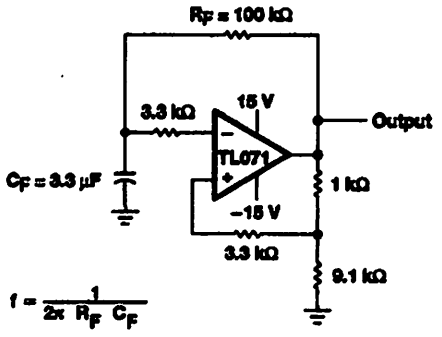


Figure 23. 0.5-Hz Square-Wave Oscillator

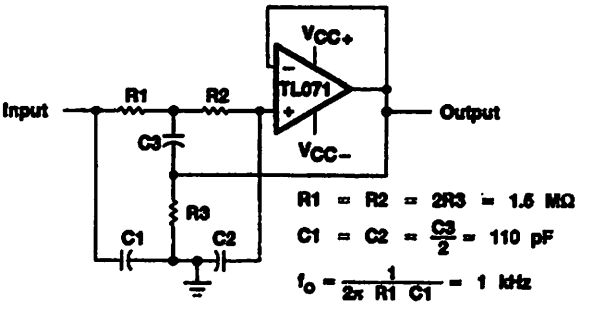


Figure 24. High-Q Notch Filter

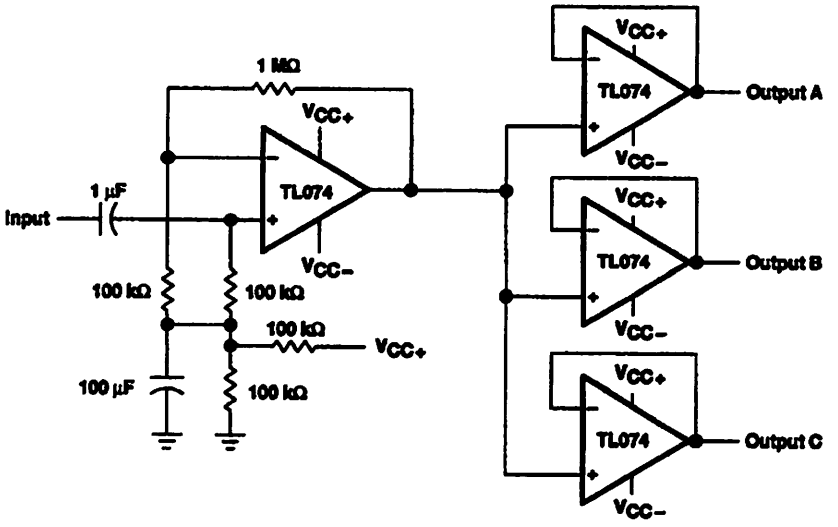
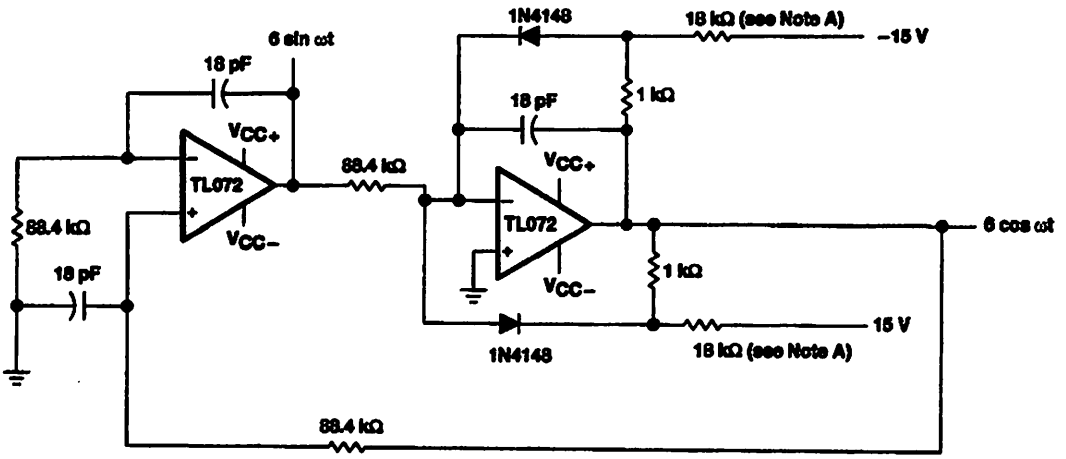


Figure 25. Audio-Distribution Amplifier

APPLICATION INFORMATION



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-kHz Quadrature Oscillator

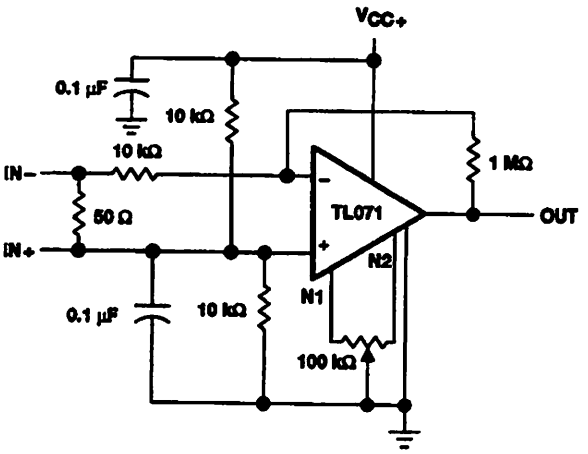


Figure 27. AC Amplifier

MC54/74HC595A

8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs

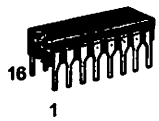
High–Performance Silicon–Gate CMOS

The MC54/74HC595A is identical in pinout to the LS595. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC595A consists of an 8–bit shift register and an 8–bit D–type latch with three–state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8–bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

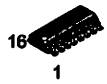
The HC595A directly interfaces with the Motorola SPI serial data port on CMOS MPUs and MCUs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- Improvements over HC595
  - — Improved Propagation Delays
  - — 50% Lower Quiescent Power
  - — Improved Input Noise and Latchup Immunity



J SUFFIX
CERAMIC PACKAGE
CASE 620–10

N SUFFIX
PLASTIC PACKAGE
CASE 648–08



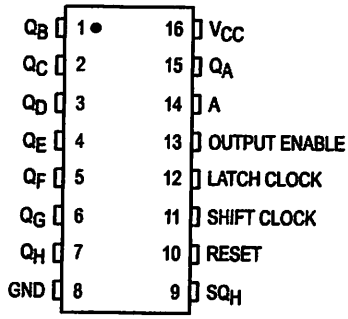
D SUFFIX
SOIC PACKAGE
CASE 751B–05

DT SUFFIX
TSSOP PACKAGE
CASE 948F–01

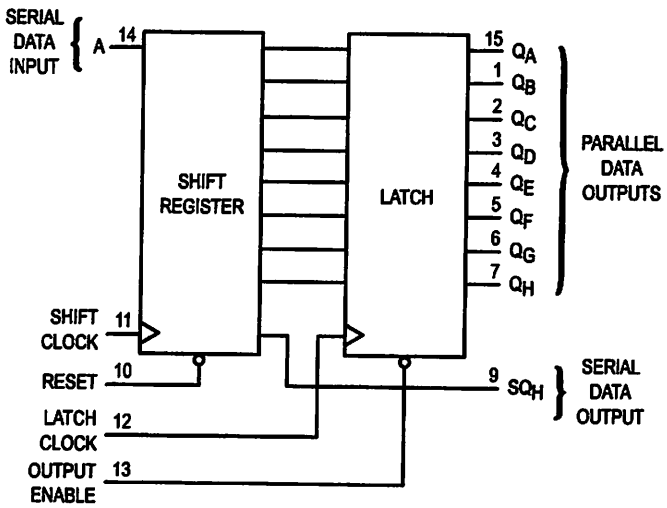
ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXAD	SOIC
MC74HCXXXADT	TSSOP

PIN ASSIGNMENT

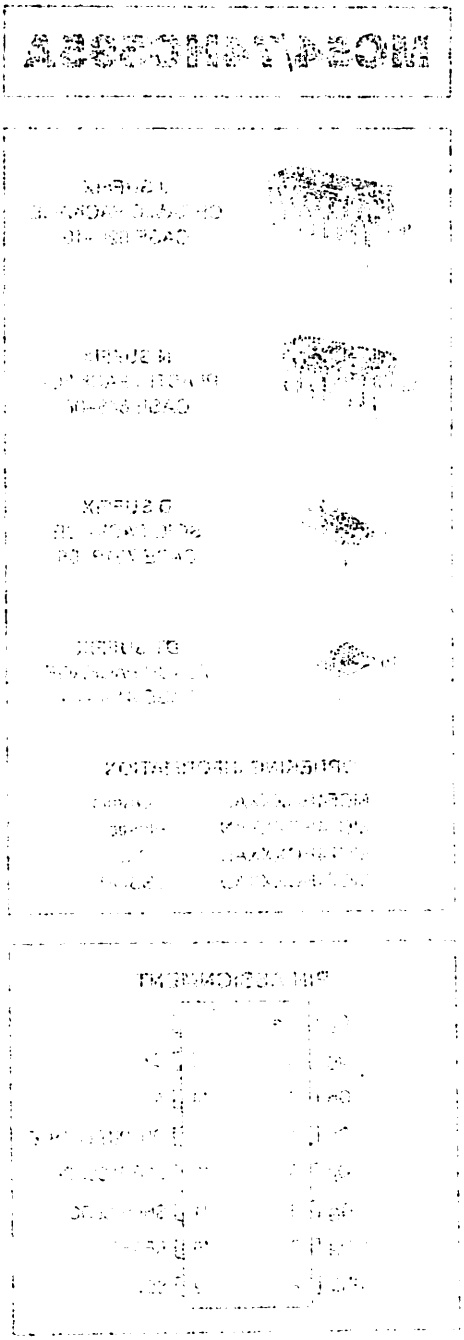


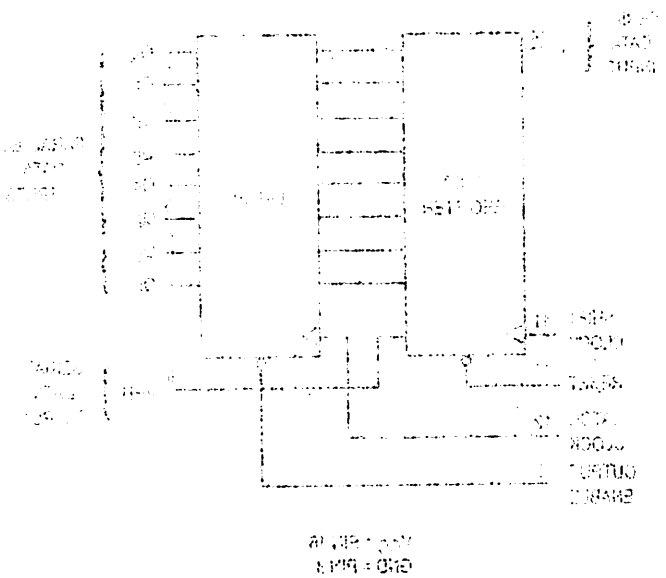
LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8

8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs





MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package) (Ceramic DIP)	 260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	≤ 85°C	≤ 125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{out}\rvert$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{out}\rvert$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage, Q_A – Q_H	V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\lvert I_{out}\rvert$ ≤ 2.4 mA $\lvert I_{out}\rvert$ ≤ 6.0 mA $\lvert I_{out}\rvert$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit −55 to 25°C	≤ 85°C	≤ 125°C	Unit
V_{OL}	Maximum Low–Level Output Voltage, $Q_A - Q_H$	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out}\rvert \le 20\ \mu A$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out}\rvert \le 2.4$ mA	3.0	0.26	0.33	0.4	
		$\lvert I_{out}\rvert \le 6.0$ mA	4.5	0.26	0.33	0.4	
		$\lvert I_{out}\rvert \le 7.8$ mA	6.0	0.26	0.33	0.4	
V_{OH}	Minimum High–Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out}\rvert \le 20\ \mu A$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out}\rvert \le 2.4$ mA	3.0	2.98	2.34	2.2	
		$\lvert I_{out}\rvert \le 4.0$ mA	4.5	3.98	3.84	3.7	
		$\lvert I_{out}\rvert \le 5.2$ mA	6.0	5.48	5.34	5.2	
V_{OL}	Maximum Low–Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out}\rvert \le 20\ \mu A$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IH}$ or V_{IL} $\lvert I_{out}\rvert \le 2.4$ mA	3.0	0.26	0.33	0.4	
		$\lvert I_{out}\rvert \le 4.0$ mA	4.5	0.26	0.33	0.4	
		$\lvert I_{out}\rvert \le 5.2$ mA	6.0	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three–State Leakage Current, $Q_A - Q_H$	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\ \mu A$	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit −55 to 25°C	≤ 85°C	≤ 125°C	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0	6.0	4.8	4.0	MHz
		3.0	15	10	8.0	
		4.5	30	24	20	
		6.0	35	28	24	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Shift Clock to SQ_H (Figures 1 and 7)	2.0	140	175	210	ns
		3.0	100	125	150	
		4.5	28	35	42	
		6.0	24	30	36	
t_{PHL}	Maximum Propagation Delay, Reset to SQ_H (Figures 2 and 7)	2.0	145	180	220	ns
		3.0	100	125	150	
		4.5	29	36	44	
		6.0	25	31	38	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Clock to $Q_A - Q_H$ (Figures 3 and 7)	2.0	140	175	210	ns
		3.0	100	125	150	
		4.5	28	35	42	
		6.0	24	30	36	
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to $Q_A - Q_H$ (Figures 4 and 8)	2.0	150	190	225	ns
		3.0	100	125	150	
		4.5	30	38	45	
		6.0	26	33	38	
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to $Q_A - Q_H$ (Figures 4 and 8)	2.0	135	170	205	ns
		3.0	90	110	130	
		4.5	27	34	41	
		6.0	23	29	35	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit −55 to 25°C	≤ 85°C	≤ 125°C	Unit
t_{TLH}, t_{THL}	Maximum Output Transition Time, $Q_A - Q_H$ (Figures 3 and 7)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 31 18 15	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, SQ_H (Figures 1 and 7)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State), $Q_A - Q_H$	—	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	300	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit 25°C to −55°C	≤ 85°C	≤ 125°C	Unit
t_{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0 3.0 4.5 6.0	75 60 15 13	95 70 19 16	110 80 22 19	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0	5.0 5.0 5.0 5.0	5.0 5.0 5.0 5.0	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 3.0 4.5 6.0	60 45 12 10	75 60 15 13	90 70 18 15	ns
t_w	Minimum Pulse Width, Shift Clock (Figure 1)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_w	Minimum Pulse Width, Latch Clock (Figure 6)	2.0 3.0 4.5 6.0	50 40 10 9.0	65 50 13 11	75 60 15 13	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output SQ_H	Parallel Outputs $Q_A - Q_H$
Reset shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	$D \rightarrow SR_A$; $SR_N \rightarrow SR_{N+1}$	U	$SR_G \rightarrow SR_H$	U
Shift register remains unchanged	H	X	L, H, ↓	L, H, ↓	L	U	U	U	U
Transfer shift register contents to latch register	H	X	L, H, ↓	↑	L	U	$SR_N \rightarrow LR_N$	U	SR_N
Latch register remains unchanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents
LR = latch register contents
D = data (L, H) logic level
U = remains unchanged
↑ = Low–to–High
↓ = High–to–Low
* = depends on Reset and Shift Clock inputs
** = depends on Latch Clock input

PIN DESCRIPTIONS

INPUTS

A (Pin 14)

Serial Data Input. The data on this pin is shifted into the 8–bit serial shift register.

CONTROL INPUTS

Shift Clock (Pin 11)

Shift Register Clock Input. A low– to–high transition on this input causes the data at the Serial Input pin to be shifted into the 8–bit shift register.

Reset (Pin 10)

Active–low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8–bit latch is not affected.

Latch Clock (Pin 12)

Storage Latch Clock Input. A low–to–high transition on this input latches the shift register data.

Output Enable (Pin 13)

Active–low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs (Q_A–Q_H) into the high–impedance state. The serial output is not affected by this control unit.

OUTPUTS

$Q_A - Q_H$ (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Noninverted, 3–state, latch outputs.

SQ_H (Pin 9)

Noninverted, Serial Data Output. This is the output of the eighth stage of the 8–bit shift register. This output does not have three–state capability.

[illegible]

[illegible]

[illegible]

SWITCHING WAVEFORMS

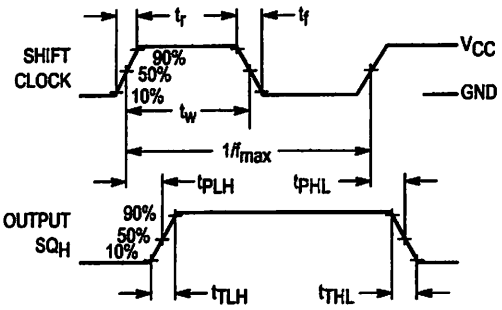


Figure 1.

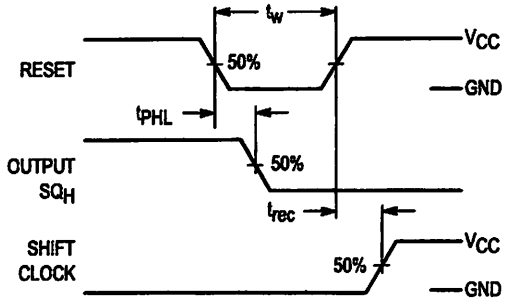


Figure 2.

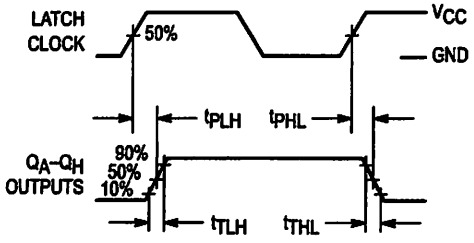


Figure 3.

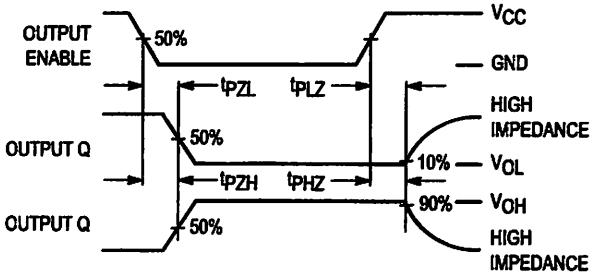


Figure 4.

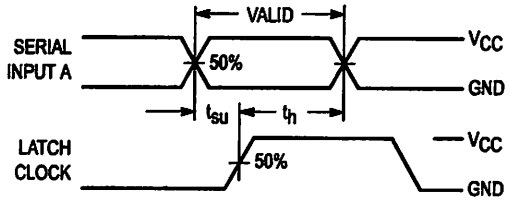


Figure 5.

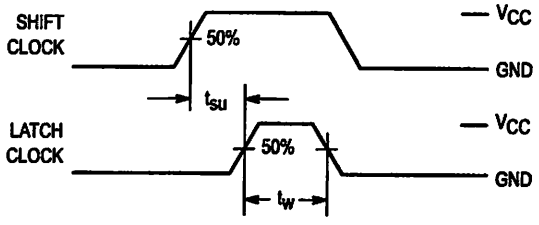
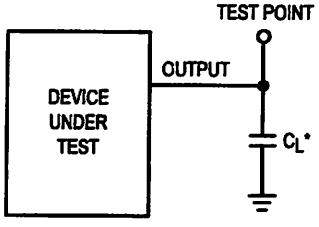


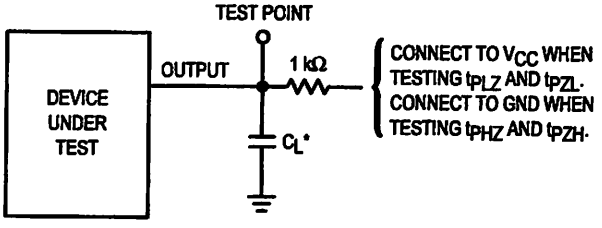
Figure 6.

TEST CIRCUITS



* Includes all probe and jig capacitance

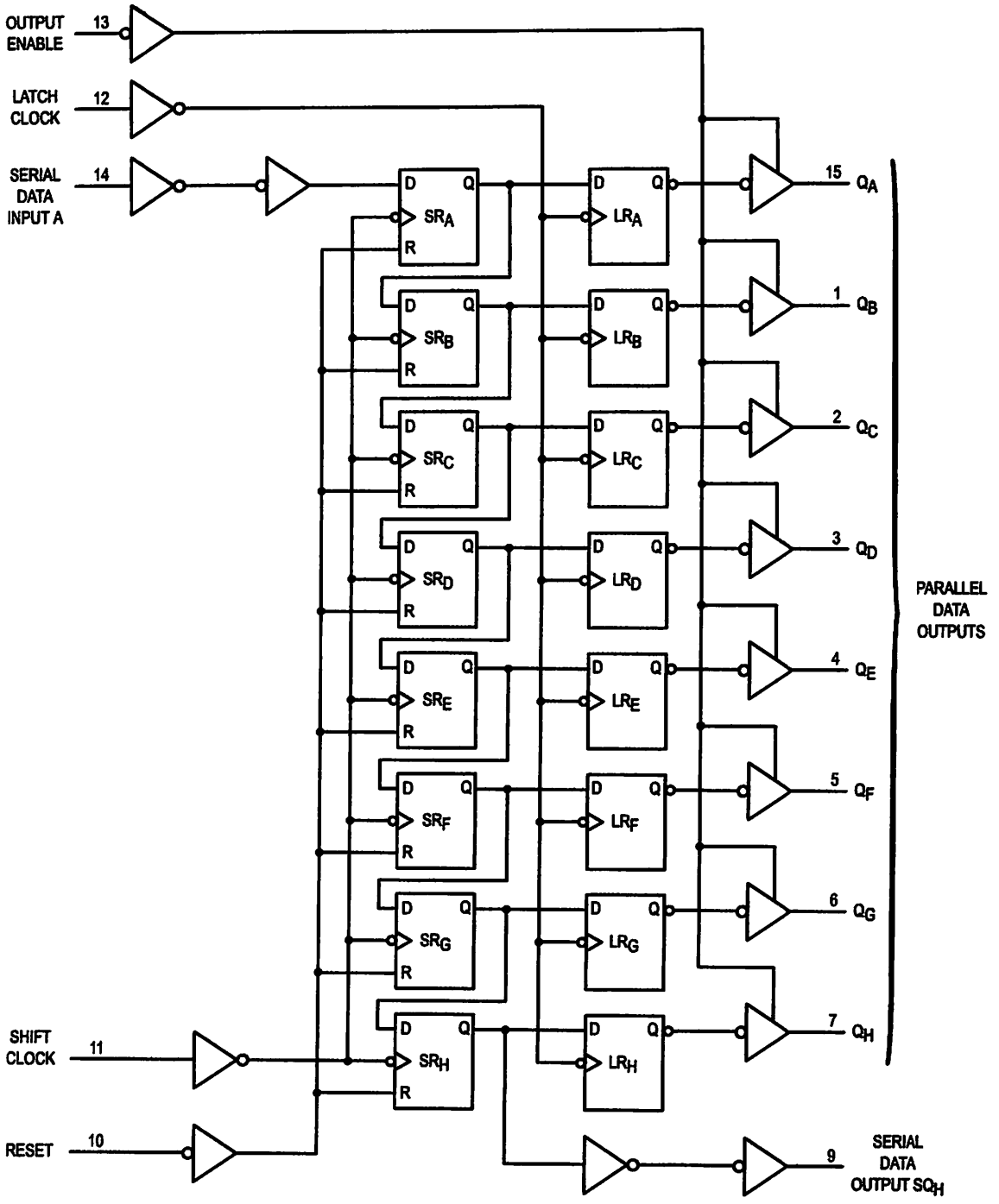
Figure 7.



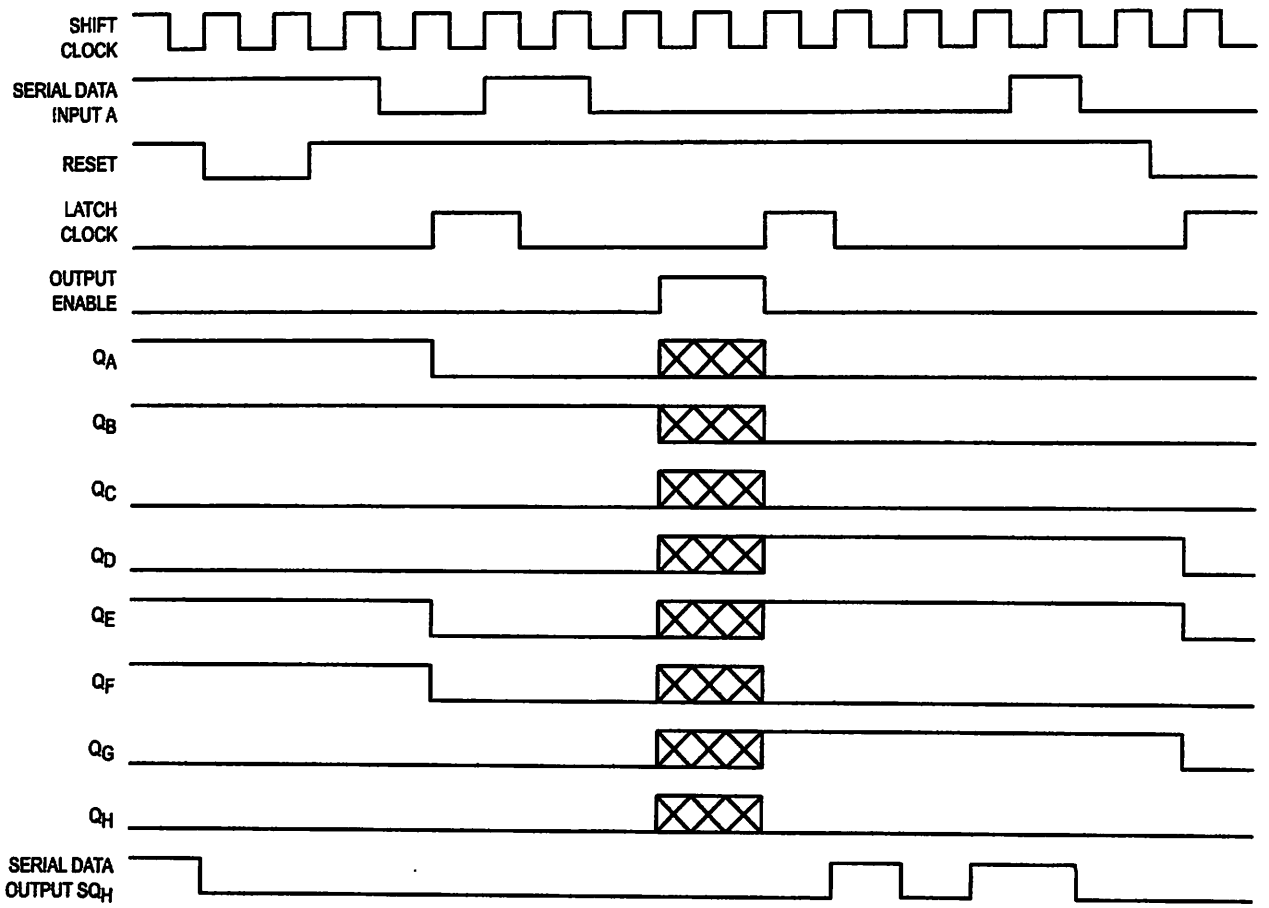
* Includes all probe and jig capacitance

Figure 8.

EXPANDED LOGIC DIAGRAM



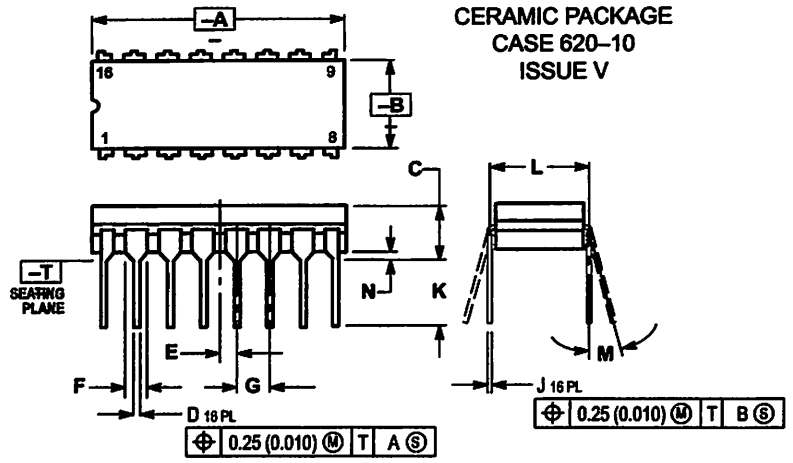
TIMING DIAGRAM



NOTE: ▩ implies that the output is in a high–impedance state.

OUTLINE DIMENSIONS

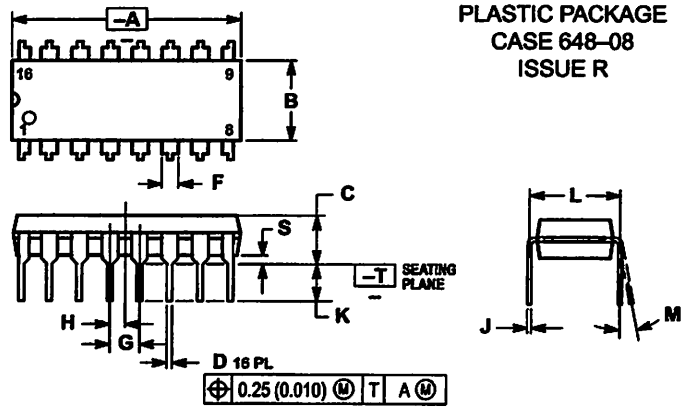
J SUFFIX
CERAMIC PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

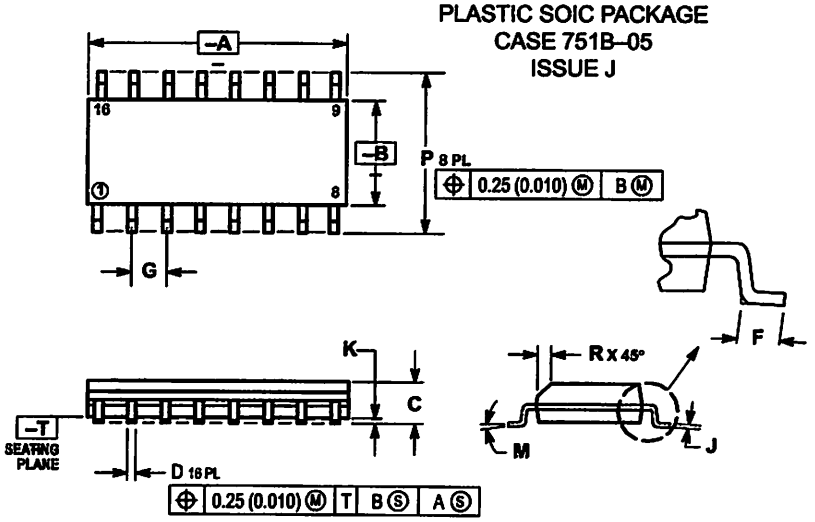
N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

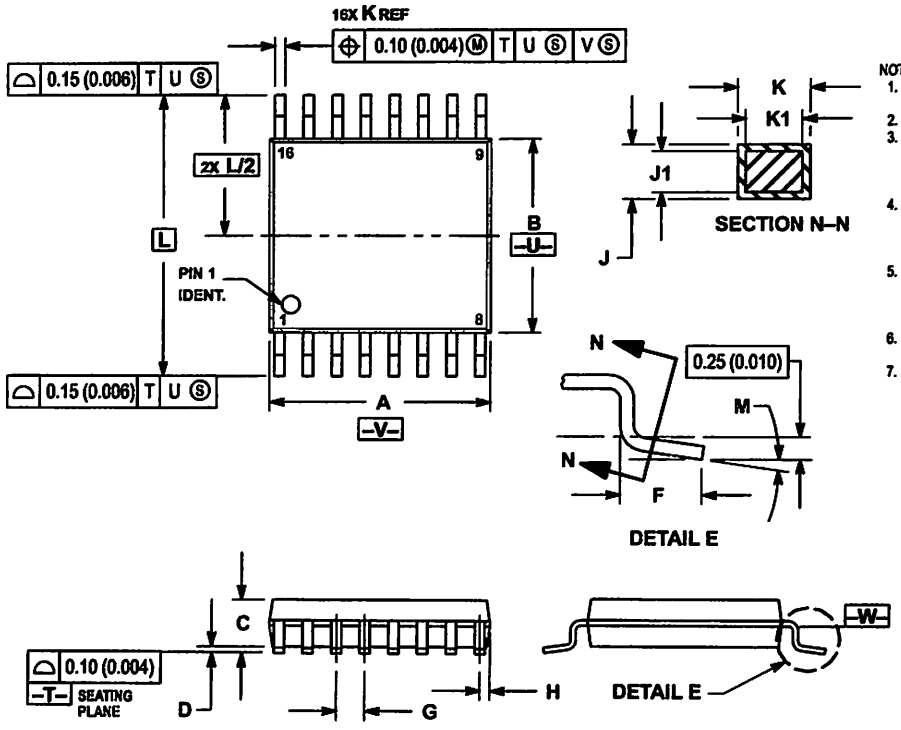


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
– US & Canada ONLY 1–800–774–1848

INTERNET: http://www.mot.com/SPS/

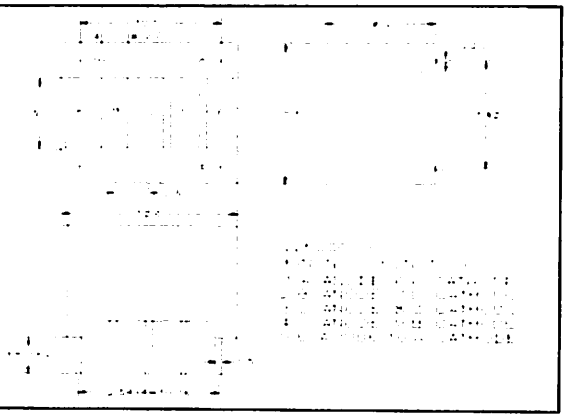
JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

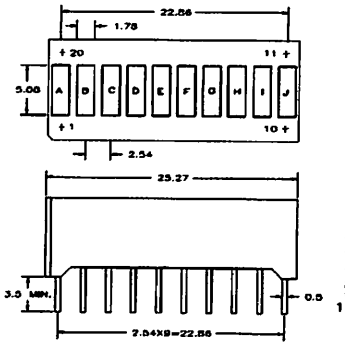
Ledtech BAR ARRAY / LCD BACK LIGHT

BAR ARRAY Electrical/Optical Characteristics at T_A=25℃

5 SEGMENT		λp (nm)	V_F (V)		I_V (mcd)	
PART NUMBER	CHIP COLOR	TYP.	TYP.	MAX.	MIN.	TYP.
LL5000-GEWAK	GREEN	572	2.1	2.4	4.6	7.7
LL5000-YEWAK	YELLOW	589	2.1	2.4	3.8	6.3
LL5000-OEWAK	ORANGE	630	2.1	2.4	5.3	8.8
LL5000-HRRRAK	ORANGE	630	2.1	2.4	5.3	8.8
LL5000-SBEWAK	SB RED	660	1.7	2.2	12.3	20.5
LL5000-M1EWAK	RED	660	1.7	2.2	7.4	12.3
LL5000-PREWAK	RED	700	2.1	2.4	1.2	2.1



10 SEGMENT		λp (nm)	V_F (V)		I_V (mcd)	
PART NUMBER	CHIP COLOR	TYP.	TYP.	MAX.	MIN.	TYP.
LL10000-GEWAK	GREEN	572	2.1	2.4	4.6	7.7
LL10000-YEWAK	YELLOW	589	2.1	2.4	3.8	6.3
LL10000-OEWAK	ORANGE	630	2.1	2.4	5.3	8.8
LL10000-HRRRAK	ORANGE	630	2.1	2.4	5.3	8.8
LL10000-SBEWAK	SB RED	660	1.7	2.2	12.3	20.5
LL10000-M1EWAK	RED	660	1.7	2.2	7.4	12.3
LL10000-PREWAK	RED	700	2.1	2.4	1.2	2.1

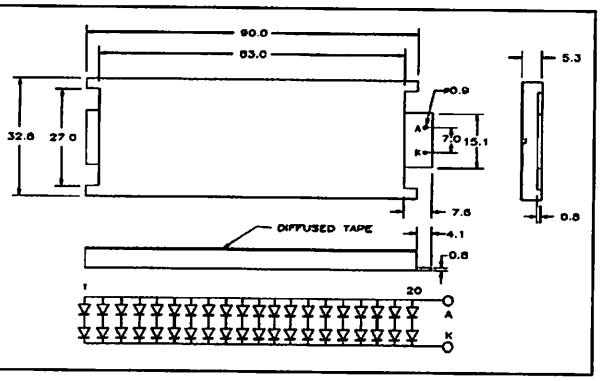


LL10000-X

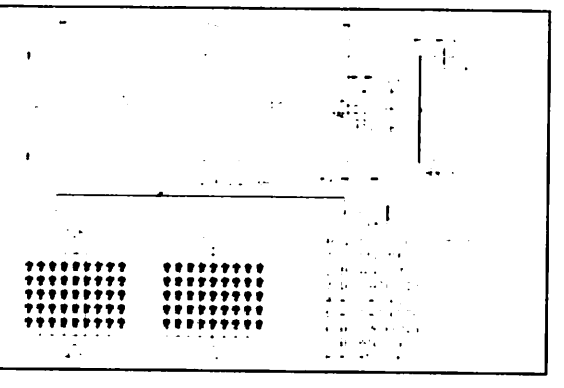
PIN NO.	FUNCTION		
1.A	ANODE	11.J	CATHODE
2.B	ANODE	12.I	CATHODE
3.C	ANODE	13.H	CATHODE
4.D	ANODE	14.G	CATHODE
5.E	ANODE	15.F	CATHODE
6.F	ANODE	16.E	CATHODE
7.G	ANODE	17.D	CATHODE
8.H	ANODE	18.C	CATHODE
9.I	ANODE	19.B	CATHODE
10.J	ANODE	20.A	CATHODE

LCD BACK LIGHT Electrical/Optical Characteristics at T_A=25℃

3.27"X1.06" (83.0mmX27.0mm)		@ 400mA				
PART NUMBER	CHIP COLOR	λp (nm)	V_F (V)		I_V (cd/m^2)	
		TYP.	TYP.	MAX.	MIN.	TYP.
LY1165-G	GREEN	572	4.2	4.8	60	100
LY1165-Y	YELLOW	589	4.2	4.8	50	80
LY1165-O	ORANGE	630	4.2	4.8	70	120
LY1165-M1	RED	660	3.4	4.4	90	140



3.98"X1.46" (101.0mmX37.0mm)		@ 360mA				
PART NUMBER	CHIP COLOR	λp (nm)	V_F (V)		I_V (cd/m^2)	
		TYP.	TYP.	MAX.	MIN.	TYP.
LY1166-G	GREEN	572	10.5	12.0	90	150
LY1166-Y	YELLOW	589	10.5	12.0	80	130
LY1166-O	ORANGE	630	10.5	12.0	100	170
LY1166-M1	RED	660	8.5	11.0	120	200



BAR ARRAY/LED BACK LIGHT

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NEC

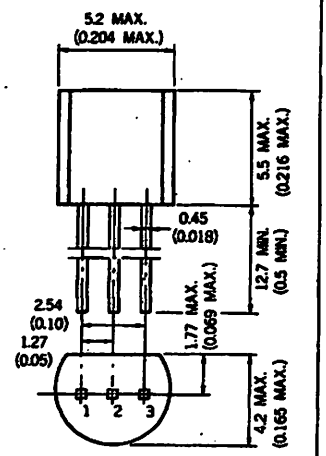
PNP SILICON TRANSISTOR
2SA733

DESCRIPTION The 2SA733 is designed for use in driver stage of AF amplifier.

FEATURES

- High h_{FE} and Excellent Linearity : 200 TYP.
  h_{FE} (V_{CE} = −6.0 V, I_C = −1.0 mA)

PACKAGE DIMENSIONS
in millimeters (inches)



1. EMITTER
2. COLLECTOR
3. BASE

EIAJ : SC-43B
JEDEC : TO-92
IEC : PA33

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature ..... −55 to +125 °C
- Junction Temperature ..... +125 °C Maximum

Maximum Power Dissipation (Ta = 25 °C)
- Total Power Dissipation ..... 250 mW

Maximum Voltages and Currents (Ta = 25 °C)
- V_{CBO} Collector to Base Voltage ..... −60 V
- V_{CEO} Collector to Emitter Voltage ..... −50 V
- V_{EBO} Emitter to Base Voltage ..... −5.0 V
- I_C Collector Current ..... −100 mA
- I_B Base Current ..... −20 mA

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	90	200	600		V_{CE} = −6.0 V, I_C = −1.0 mA
NF	Noise Figure		6.0	20	dB	V_{CE} = −6.0 V, I_C = −0.3 mA, R_G = 10 kΩ, f = 100 Hz
f_T	Gain Bandwidth Product	100	180		MHz	V_{CE} = −6.0 V, I_E = 10 mA
C_{ob}	Output Capacitance		4.5	6.0	pF	V_{CB} = −10 V, I_E = 0, f = 1.0 MHz
I_{CBO}	Collector Cutoff Current			−0.1	μA	V_{CB} = −60 V, I_E = 0
I_{EBO}	Emitter Cutoff Current			−0.1	μA	V_{EB} = −5.0 V, I_C = 0
V_{BE}	Base to Emitter Voltage	−0.58	−0.62	−0.68	V	V_{CE} = −6.0 V, I_C = −1.0 mA
$V_{CE(sat)}$	Collector Saturation Voltage		−0.18	−0.3	V	I_C = −100 mA, I_B = −10 mA

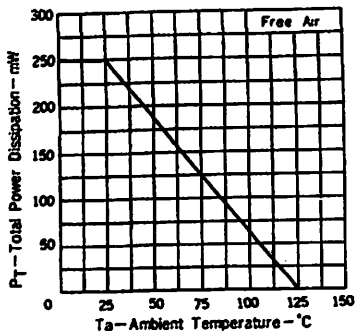
Classification of h_{FE}

Rank	R	Q	P	K
Range	90 – 180	135 – 270	200 – 400	300 – 600

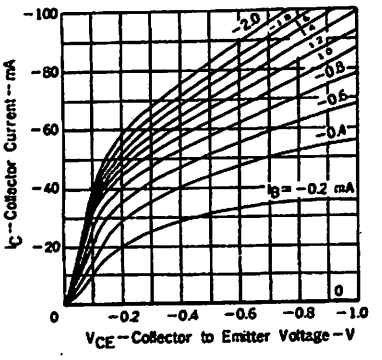
h_{FE} Test Conditions : V_{CE} = −6.0 V, I_C = −1.0 mA

TYPICAL CHARACTERISTICS (Ta = 25 °C unless otherwise noted)

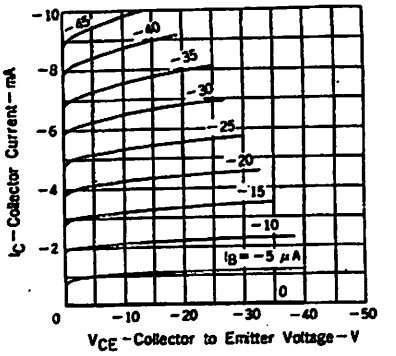
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



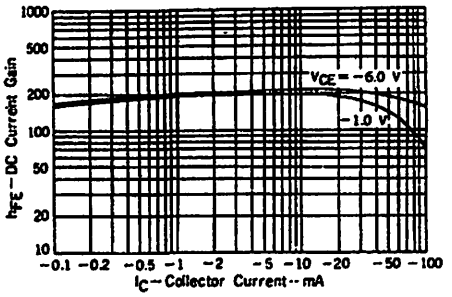
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



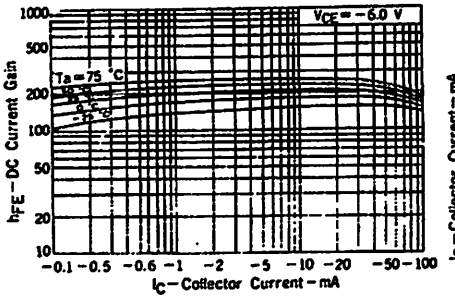
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



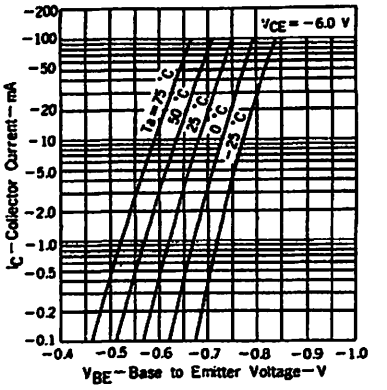
DC CURRENT GAIN vs. COLLECTOR CURRENT



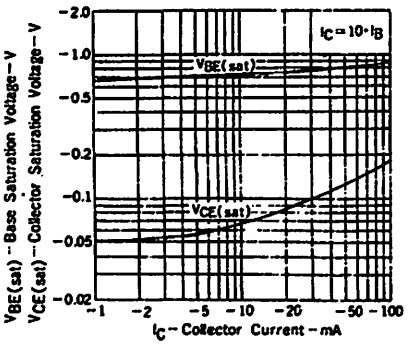
DC CURRENT GAIN vs. COLLECTOR CURRENT



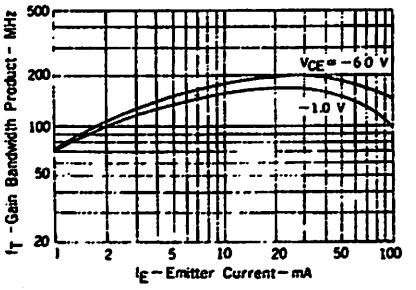
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



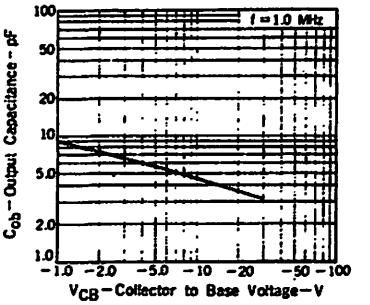
COLLECTOR AND BASE SATURATION VOLTAGE vs. COLLECTOR CURRENT



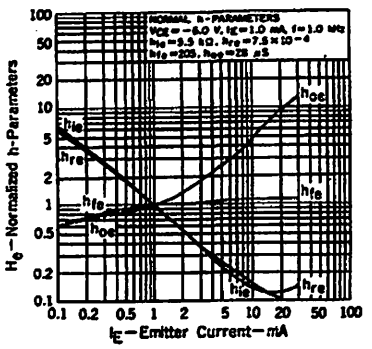
GAIN BANDWIDTH PRODUCT vs. EMITTER CURRENT



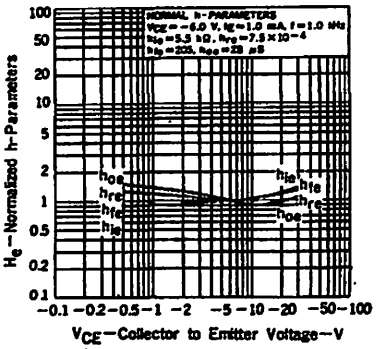
OUTPUT CAPACITANCE vs. REVERSE VOLTAGE



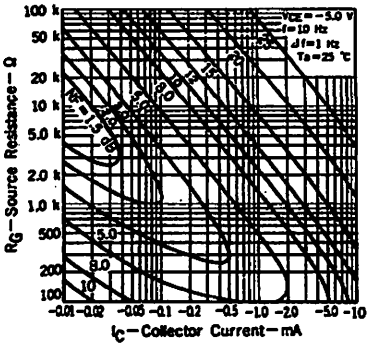
NORMALIZED h-PARAMETERS vs. EMITTER CURRENT



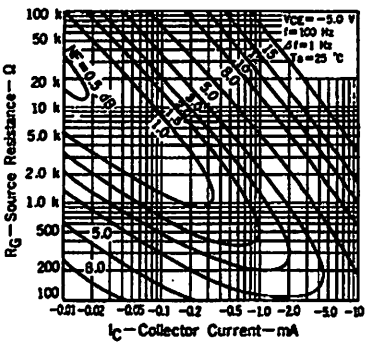
NORMALIZED h-PARAMETERS vs. COLLECTOR TO EMITTER VOLTAGE



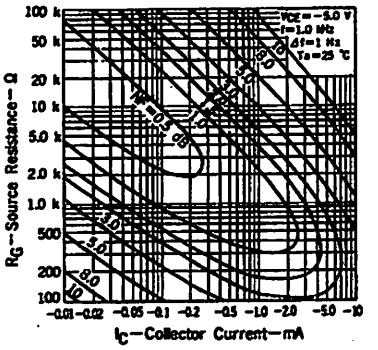
NOISE FIGURE MAP 1



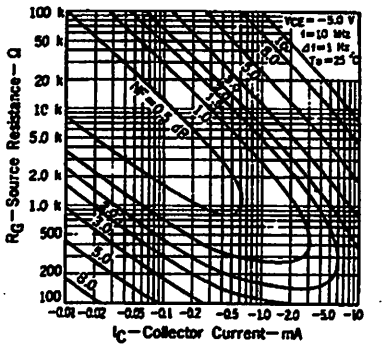
NOISE FIGURE MAP 2



NOISE FIGURE MAP 3



NOISE FIGURE MAP 4



National Semiconductor

May 2001

MF10
Universal Monolithic Dual Switched Capacitor Filter

General Description

The MF10 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10; higher than 4th order functions can be obtained by cascading MF10 packages.

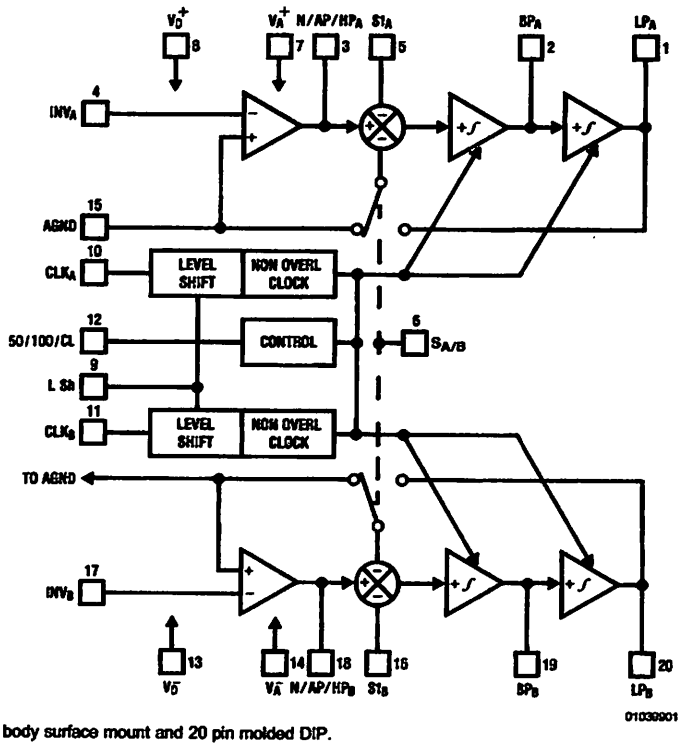
Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

For pin-compatible device with improved performance refer to LMF100 datasheet.

Features

- Easy to use
- Clock to center frequency ratio accuracy ±0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variation
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- f_O x Q range up to 200 kHz
- Operation up to 30 kHz
- 20-pin 0.3" wide Dual-In-Line package
- 20-pin Surface Mount (SO) wide-body package

System Block Diagram



Package in 20 pin molded wide body surface mount and 20 pin molded DIP.

National Semiconductor

May 2001

MF10
Universal Monolithic Dual Switched Capacitor Filter

General Description

The MF10 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10; higher than 4th order functions can be obtained by cascading MF10 packages.

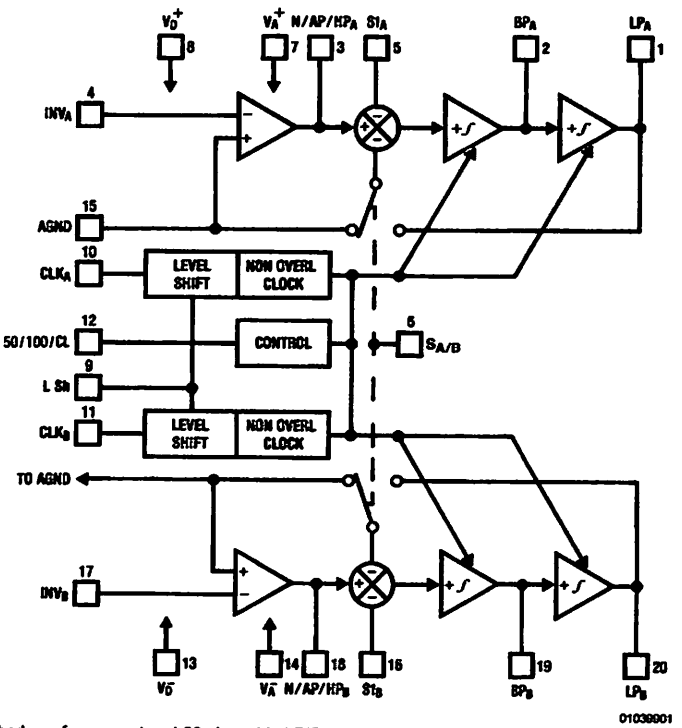
Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

For pin-compatible device with improved performance refer to LMF100 datasheet.

Features

- Easy to use
- Clock to center frequency ratio accuracy ±0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variation
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- f_O x Q range up to 200 kHz
- Operation up to 30 kHz
- 20-pin 0.3" wide Dual-In-Line package
- 20-pin Surface Mount (SO) wide-body package

System Block Diagram



Package in 20 pin molded wide body surface mount and 20 pin molded DIP.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	14V
Voltage at Any Pin	$V^+ + 0.3V$
	$V^- - 0.3V$
Input Current at Any Pin (Note 2)	5 mA
Package Input Current (Note 2)	20 mA
Power Dissipation (Note 3)	500 mW
Storage Temperature	150°C
ESD Susceptability (Note 11)	2000V
Soldering Information	
N Package: 10 sec	260°C
SO Package:	
Vapor Phase (60 Sec.)	215°C
Infrared (15 Sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
MF10ACN, MF10CCN	$0°C \le T_A \le 70°C$
MF10CCWM	$0°C \le T_A \le 70°C$

Electrical Characteristics

$V^+ = +5.00V$ and $V^- = -5.00V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions		MF10ACN, MF10CCN, MF10CCWM Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Units
$V^+ - V^-$	Supply Voltage	Min					**9**	V
		Max					**14**	V
I_S	Maximum Supply Current		Clock Applied to Pins 10 & 11 No Input Signal		8	12	**12**	mA
f_O	Center Frequency Range	Min	$f_O \times Q < 200$ kHz		0.1		**0.2**	Hz
		Max			30		**20**	kHz
f_{CLK}	Clock Frequency Range	Min			5.0		**10**	Hz
		Max			1.5		**1.0**	MHz
f_{CLK}/f_O	50:1 Clock to Center Frequency Ratio Deviation	MF10A	Q = 10 Mode 1	$V_{pin12} = 5V$ $f_{CLK} = 250$ KHz	±0.2	±0.6	**±0.6**	%
		MF10C			±0.2	±1.5	**±1.5**	%
f_{CLK}/f_O	100:1 Clock to Center Frequency Ratio Deviation	MF10A	Q = 10 Mode 1	$V_{pin12} = 0V$ $f_{CLK} = 500$ kHz	±0.2	±0.6	**±0.6**	%
		MF10C			±0.2	±1.5	**±1.5**	%
	Clock Feedthrough		Q = 10 Mode 1		10			mV
	Q Error (MAX) (Note 4)		Q = 10 Mode 1	$V_{pin12} = 5V$ $f_{CLK} = 250$ kHz	±2	±6	**±6**	%
				$V_{pin12} = 0V$ $f_{CLK} = 500$ kHz	±2	±6	**±6**	%
H_{OLP}	DC Lowpass Gain		Mode 1 R1 = R2 = 10k		0	±0.2	**±0.2**	dB
V_{OS1}	DC Offset Voltage (Note 5)				±5.0	±20	**±20**	mV
V_{OS2}	DC Offset Voltage	Min	$V_{pin12} = +5V$	$S_{A/B} = V^+$	−150	−185	**−185**	mV

Electrical Characteristics (Continued)

V^+ = +5.00V and V^- = −5.00V unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX}**; all other limits $T_A = T_J$ = 25˚C.

Symbol	Parameter		Conditions		MF10ACN, MF10CCN, MF10CCWM Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Units
	(Note 5)	Max	(f_{CLK}/f_O = 50)			−85	**−85**	
		Min	V_{pin12} = +5V	$S_{A/B} = V^-$	−70			mV
		Max	(f_{CLK}/f_O = 50)					
V_{OS3}	DC Offset Voltage	Min	V_{pin12} = +5V	All Modes	−70	−100	**−100**	mV
	(Note 5)	Max	(f_{CLK}/f_O = 50)			−20	**−20**	
V_{OS2}	DC Offset Voltage (Note 5)		V_{pin12} = 0V (f_{CLK}/f_O = 100)	$S_{A/B} = V^+$	−300			mV
			V_{pin12} = 0V (f_{CLK}/f_O = 100)	$S_{A/B} = V^-$	−140			mV
V_{OS3}	DC Offset Voltage (Note 5)		V_{pin12} = 0V (f_{CLK}/f_O = 100)	All Modes	−140			mV
V_{OUT}	Minimum Output	BP, LP Pins	R_L = 5k		±4.25	±3.8	**±3.8**	V
	Voltage Swing	N/AP/HP Pin	R_L = 3.5k		±4.25	±3.8	**±3.8**	V
GBW	Op Amp Gain BW Product				2.5			MHz
SR	Op Amp Slew Rate				7			V/μs
	Dynamic Range(Note 6)		V_{pin12} = +5V (f_{CLK}/f_O = 50)		83			dB
			V_{pin12} = 0V (f_{CLK}/f_O = 100)		80			dB
I_{SC}	Maximum Output Short	Source			20			mA
	Circuit Current (Note 7)	Sink			3.0			mA

Logic Input Characteristics

Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J$ = 25˚C

Parameter		Conditions	MF10ACN, MF10CCN, MF10CCWM Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Units
CMOS Clock Input Voltage	Min Logical "1"	V^+ = +5V, V^- = −5V, V_{LSh} = 0V		+3.0	**+3.0**	V
	Max Logical "0"			−3.0	**−3.0**	V
	Min Logical "1"	V^+ = +10V, V^- = 0V, V_{LSh} = +5V		+8.0	**+8.0**	V
	Max Logical "0"			+2.0	**+2.0**	V
TTL Clock Input Voltage	Min Logical "1"	V^+ = +5V, V^- = −5V, V_{LSh} = 0V		+2.0	**+2.0**	V
	Max Logical "0"			+0.8	**+0.8**	V

Logic Input Characteristics (Continued)

Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J = 25°C$

Parameter		Conditions	MF10ACN, MF10CCN, MF10CCWM			Units
			Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
	Min Logical "1"	$V^+ = +10V$, $V^- = 0V$,		+2.0	**+2.0**	V
	Max Logical "0"	$V_{LSh} = 0V$		+0.8	**+0.8**	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the MF10ACN/CCN when board mounted is 55°C/W. For the MF10AJ/CCJ, this number increases to 95°C/W and for the MF10ACWM/CCWM this number is 66°C/W.

Note 4: The accuracy of the Q value is a function of the center frequency (f_O). This is illustrated in the curves under the heading "Typical Performance Characteristics".

Note 5: V_{OS1}, V_{OS2}, and V_{OS3} refer to the internal offsets as discussed in the Applications Information Section 3.4.

Note 6: For ±5V supplies the dynamic range is referenced to 2.82V rms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 µV rms for the MF10 with a 50:1 CLK ratio and 280 µV rms for the MF10 with a 100:1 CLK ratio.

Note 7: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

Note 8: Typicals are at 25°C and represent most likely parametric norm.

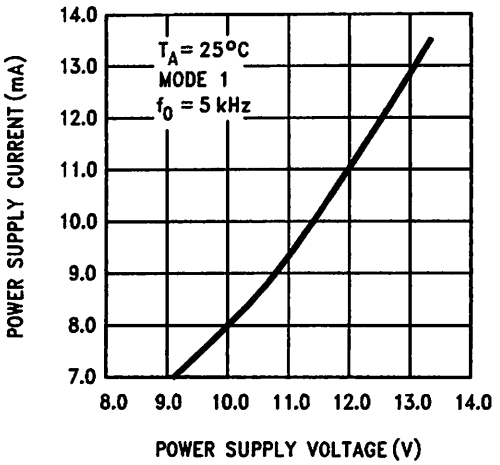
Note 9: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

Power Supply Current vs. Power Supply Voltage



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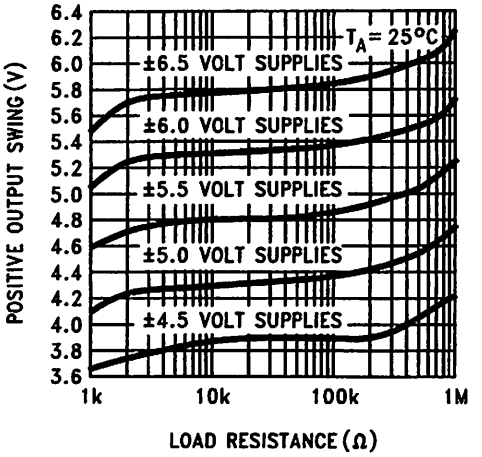
Positive Output Voltage Swing vs. Load Resistance (N/AP/HP Output)



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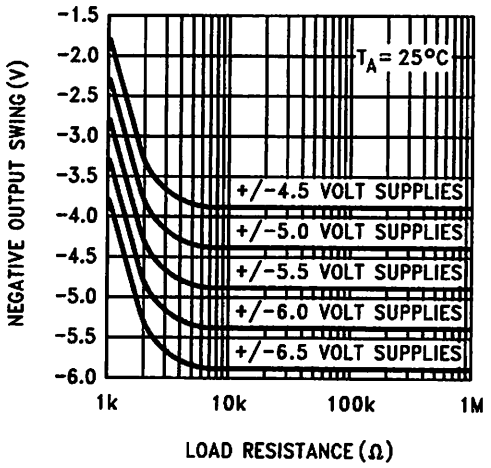
Negative Output Voltage Swing vs. Load Resistance (N/AP/HP Output)



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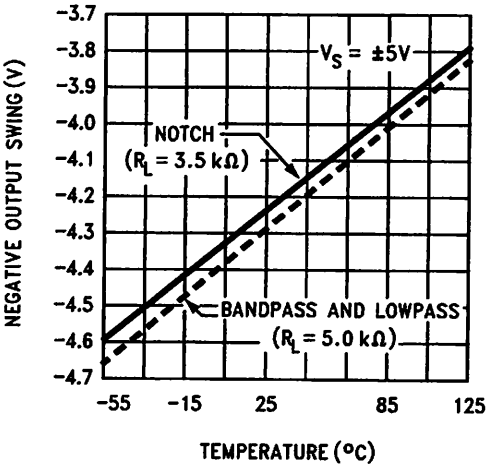
Negative Output Swing vs. Temperature



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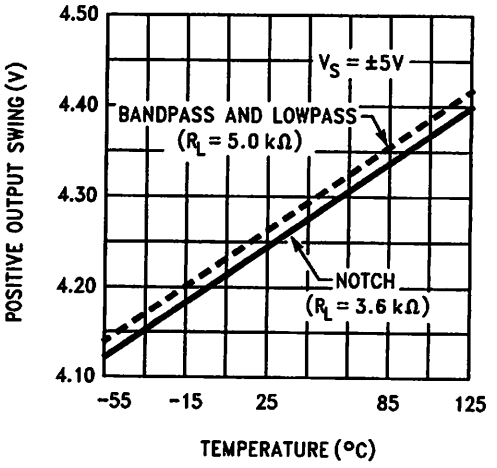
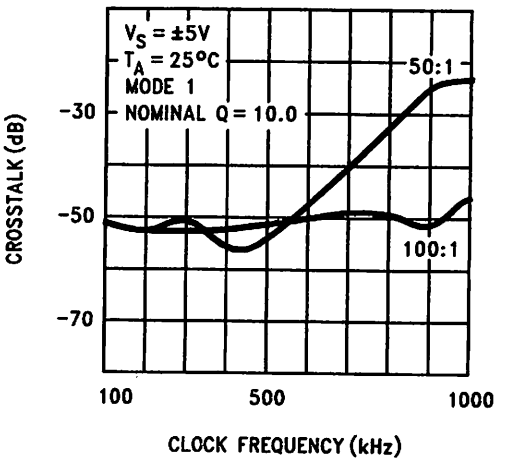
Positive Output Swing vs. Temperature



01039938

Crosstalk vs. Clock Frequency



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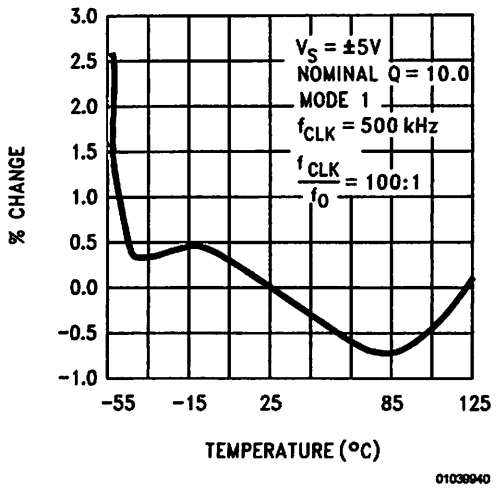
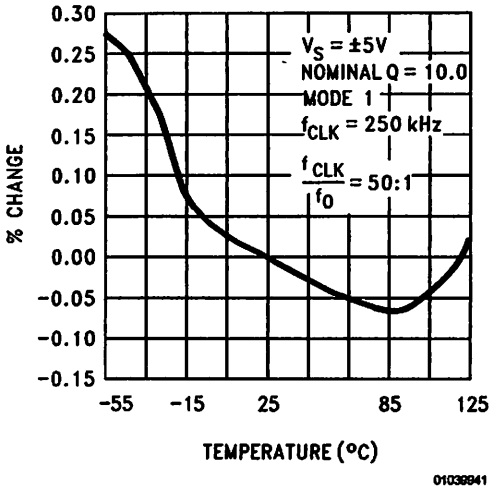
Typical Performance Characteristics (Continued)

Q Deviation vs. Temperature



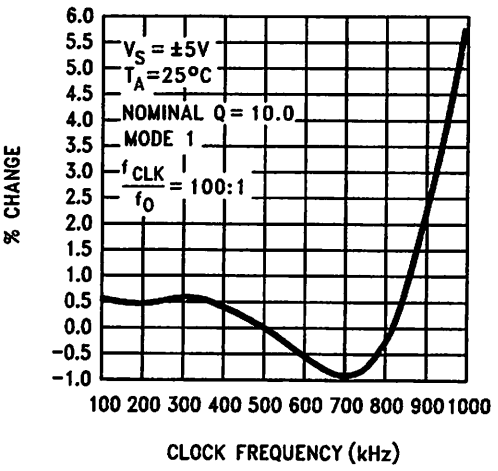
01039940

Q Deviation vs. Temperature



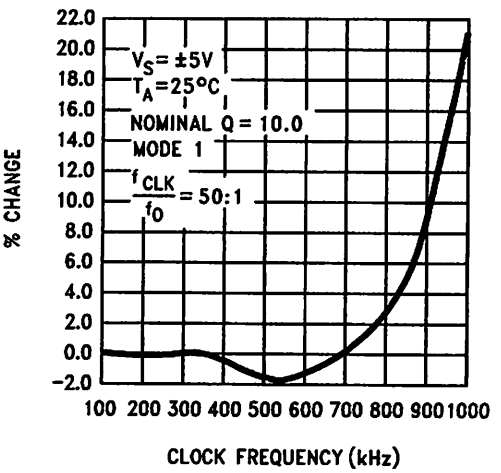
01039941

Q Deviation vs. Clock Frequency



01039942

Q Deviation vs. Clock Frequency



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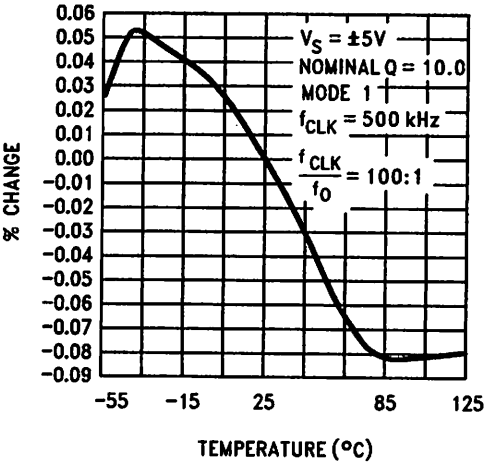
f_{CLK}/f_O Deviation vs. Temperature



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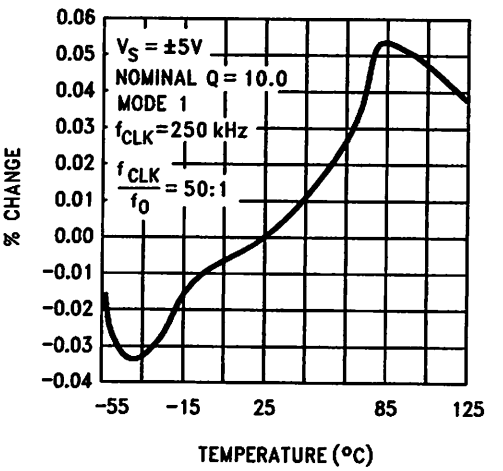
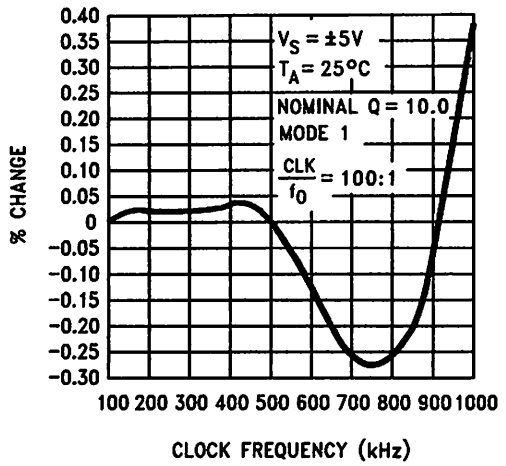
f_{CLK}/f_O Deviation vs. Temperature



01039945

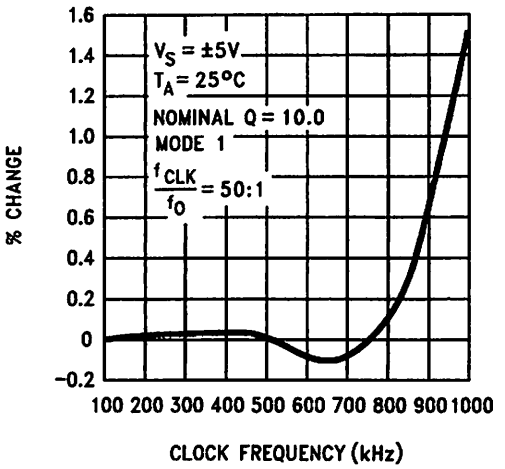
Typical Performance Characteristics (Continued)

f_{CLK}/f_O Deviation vs. Clock Frequency



01039946

f_{CLK}/f_O Deviation vs. Clock Frequency



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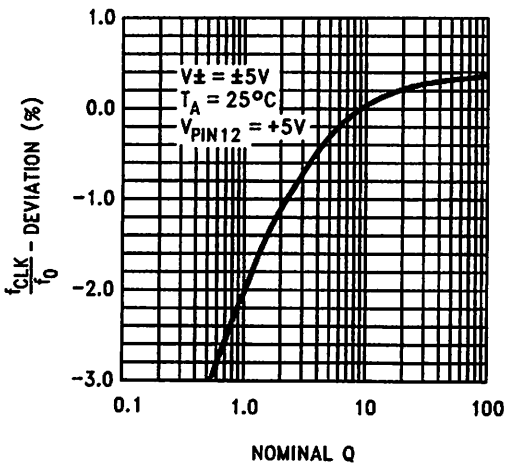
Deviation of f_{CLK}/f_O vs. Nominal Q



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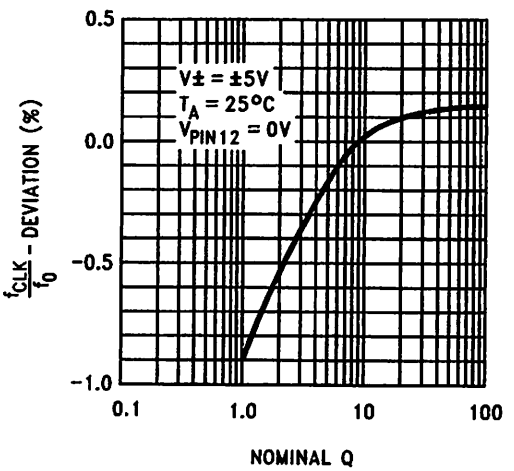
Deviation of f_{CLK}/f_O vs. Nominal Q



01039949

Pin Descriptions

LP(1,20), BP(2,19), N/AP/HP(3,18)
The second order lowpass, bandpass and notch/allpass/highpass outputs. These outputs can typically sink 1.5 mA and source 3 mA. Each output typically swings to within 1V of each supply.

INV(4,17) The inverting input of the summing op-amp of each filter. These are high impedance inputs, but the non-inverting input is internally tied to AGND, making INV_A and INV_B behave like summing junctions (low impedance, current inputs).

S1(5,16) S1 is a signal input pin used in the allpass filter configurations (see modes 4 and 5). The pin should be driven with a source impedance of less than 1 kΩ. If S1 is not driven with a signal it should be tied to AGND (mid-supply).

$S_{A/B}$(6) This pin activates a switch that connects one of the inputs of each filter's second summer to either AGND ($S_{A/B}$ tied to V^-) or to the lowpass (LP) output ($S_{A/B}$ tied to V^+). This offers the flexibility needed for configuring the filter in its various modes of operation.

V_A^+(7),V_D^+(8) Analog positive supply and digital positive supply. These pins are internally connected through the IC substrate and therefore V_A^+ and V_D^+ should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.

V_A^-(14), V_D^-(13) Analog and digital negative supplies. The same comments as for V_A^+ and V_D^+ apply here.

LSh(9) Level shift pin; it accommodates various clock levels with dual or single supply operation. With dual ±5V supplies, the MF10 can be driven with CMOS clock levels (±5V) and the LSh pin should be tied to the system ground. If the same supplies as above are used but only TTL clock levels, derived from 0V to +5V supply, are available, the LSh pin should be tied to the system ground. For single supply operation (0V and +10V) the V_A^-, V_D^-pins should be connected to the system ground, the AGND pin should be biased at +5V and the LSh pin should also be tied to the system ground for TTL clock levels. LSh should be biased at +5V for CMOS clock levels in 10V single-supply applications.

CLKA(10), CLKB(11)
Clock inputs for each switched capacitor filter building block. They should both be of the same level (TTL or CMOS). The level shift (LSh) pin description discusses how to accommodate their levels. The duty cycle of the clock should be close to 50% especially when clock frequencies above 200 kHz are used. This allows the maximum time for the internal op-amps to settle, which yields optimum filter operation.

50/100/CL(12) By tying this pin high a 50:1 clock-to-filter-center-frequency ratio is obtained. Tying this pin at mid-supplies (i.e. analog ground with dual supplies) allows the filter to operate at a 100:1 clock-to-center-frequency ratio. When the pin is tied low (i.e., negative supply with dual supplies), a simple current limiting circuit is triggered to limit the overall supply current down to about 2.5 mA. The filtering action is then aborted.

AGND(15) This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation. For a further discussion of mid-supply biasing techniques see the Applications Information (Section 3.2). For optimum filter performance a "clean" ground must be provided.

1.0 Definition of Terms

f_{CLK}: the frequency of the external clock signal applied to pin 10 or 11.

f_O: center frequency of the second order function complex pole pair. f_O is measured at the bandpass outputs of the MF10, and is the frequency of maximum bandpass gain. (*Figure 1*)

f_{notch}: the frequency of minimum (ideally zero) gain at the notch outputs.

f_z: the center frequency of the second order complex zero pair, if any. If f_z is different from f_O and if Q_Z is high, it can be observed as the frequency of a notch at the allpass output. (*Figure 10*)

Q: "quality factor" of the 2nd order filter. Q is measured at the bandpass outputs of the MF10 and is equal to f_O divided by the −3 dB bandwidth of the 2nd order bandpass filter (*Figure 1*). The value of Q determines the shape of the 2nd order filter responses as shown in *Figure 6*.

Q_Z: the quality factor of the second order complex zero pair, if any. Q_Z is related to the allpass characteristic, which is written:

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_O}{Q_Z} + \omega_O^2\right)}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

where Q_Z = Q for an all-pass response.

H_{OBP}: the gain (in V/V) of the bandpass output at f = f_O.

1.0 Definition of Terms (Continued)

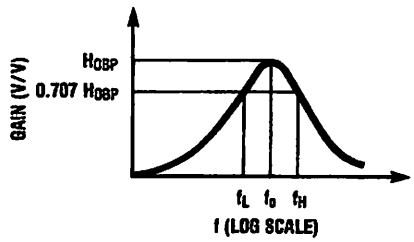
H_{OLP}: the gain (in V/V) of the lowpass output as $f \rightarrow 0$ Hz (*Figure 2*).

H_{OHP}: the gain (in V/V) of the highpass output as $f \rightarrow f_{CLK}/2$ (*Figure 3*).

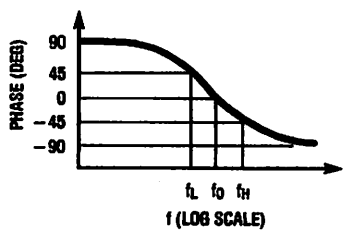
H_{ON}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz and as $f \rightarrow f_{CLK}/2$, when the notch filter has equal gain above and below the center frequency (*Figure 4*). When the low-frequency gain differs from the high-frequency gain, as in modes 2 and 3a (*Figure 11* and *Figure 8*), the two quantities below are used in place of H_{ON}.

H_{ON1}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz.

H_{ON2}: the gain (in V/V) of the notch output as $f \rightarrow f_{CLK}/2$.



(a)



(b)

$$H_{BP}(s) = \frac{H_{OBP}\frac{\omega O}{Q}s}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

$$Q = \frac{f_O}{f_H - f_L};\ f_O = \sqrt{f_L f_H}$$

$$f_L = f_O\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_O\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$\omega_O = 2\pi f_O$$

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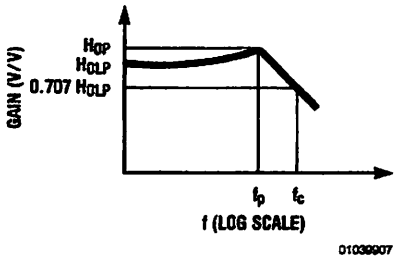
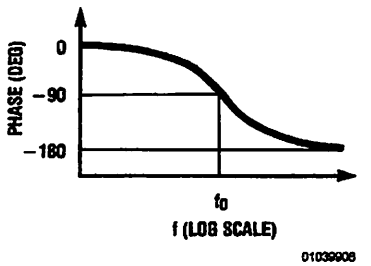
FIGURE 1. 2nd-Order Bandpass Response

1.0 Definition of Terms (Continued)



(a)



(b)

$$H_{LP}(s) = \frac{H_{OLP}\omega_0^2}{s^2 + \frac{s\omega_0}{Q} + \omega_0^2}$$

$$f_C = f_O \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

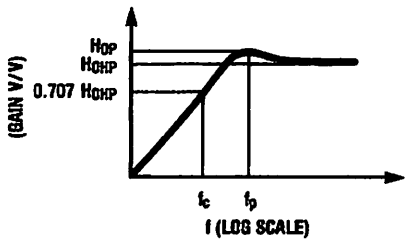
$$f_p = f_O\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

01039957

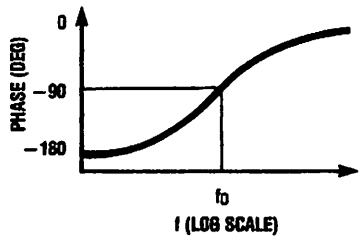
FIGURE 2. 2nd-Order Low-Pass Response

1.0 Definition of Terms (Continued)



01039909

(a)



01039910

(b)

$$H_{HP}(s) = \frac{H_{OHP}s^2}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

$$f_C = f_O \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

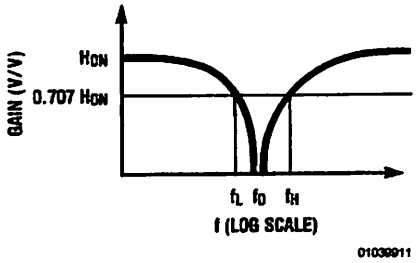
$$f_P = f_O \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

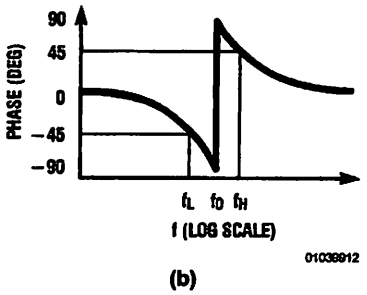
01039958

FIGURE 3. 2nd-Order High-Pass Response

1.0 Definition of Terms (Continued)



(a)



(b)

$$H_N(s) = \frac{H_{ON}(s^2 + \omega_O^2)}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

$$Q = \frac{f_O}{f_H - f_L};\ f_O = \sqrt{f_L f_H}$$

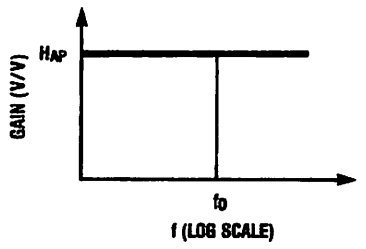
$$f_L = f_O\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_O\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

01039960

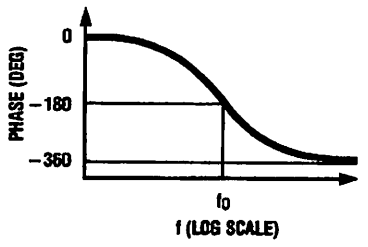
FIGURE 4. 2nd-Order Notch Response

1.0 Definition of Terms (Continued)



01039913

(a)



01039914

(b)

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_O}{Q} + \omega_O^2\right)}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

01039961

FIGURE 5. 2nd-Order All-Pass Response

1.0 Definition of Terms (Continued)

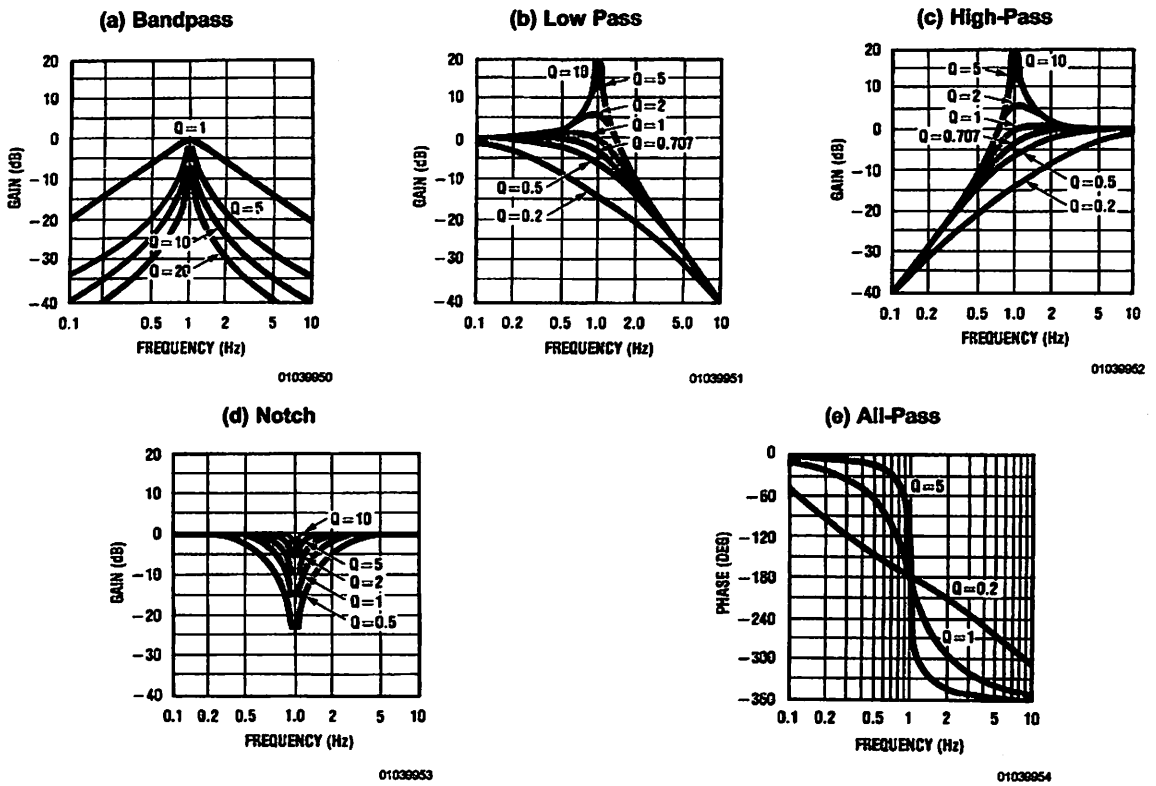


FIGURE 6. Response of various 2nd-order filters as a function of Q. Gains and center frequencies are normalized to unity.

2.0 Modes of Operation

The MF10 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain approach is appropriate. Since this is cumbersome, and since the MF10 closely approximates continuous filters, the following discussion is based on the well known frequency domain. Each MF10 can produce a full 2nd order function. See *Table 1* for a summary of the characteristics of the various modes.

MODE 1: Notch 1, Bandpass, Lowpass Outputs:

$$f_{notch} = f_O \text{ (See } \textit{Figure 7}\text{)}$$

f_O= center frequency of the complex pole pair

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

f_{notch}= center frequency of the imaginary zero pair = f_O.

$$H_{OLP} = \text{Lowpass gain (as } f \rightarrow 0) = -\frac{R2}{R1}$$

$$H_{OBP} = \text{Bandpass gain (at } f = f_O) = -\frac{R3}{R1}$$

$$H_{ON} = \text{Notch output gain as } \left.\begin{matrix} f \rightarrow 0 \\ f \rightarrow f_{CLK}/2 \end{matrix}\right\} = \frac{-R_2}{R_1}$$

$$Q = \frac{f_O}{BW} = \frac{R3}{R2}$$

= quality factor of the complex pole pair

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$$H_{OLP} = \frac{H_{OBP}}{Q} \text{ or } H_{OBP} = H_{OLP} \times Q$$

$$= H_{ON} \times Q.$$

$$H_{OLP(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)}$$

MODE 1a: Non-Inverting BP, LP (See *Figure 8*)

$$f_O = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -1;\ H_{OLP(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)}$$

$$H_{OBP_1} = -\frac{R3}{R2}$$

H_{OBP_2}= 1 (Non-Inverting)

Circuit Dynamics: $H_{OBP1} = Q$

Note: V_{IN} should be driven from a low impedance (<1 kΩ) source.

2.0 Modes of Operation (Continued)

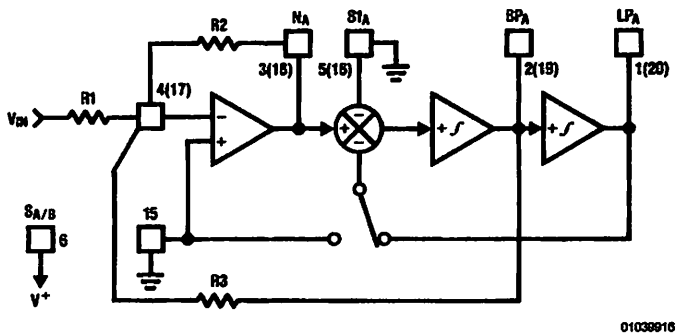


FIGURE 7. MODE 1

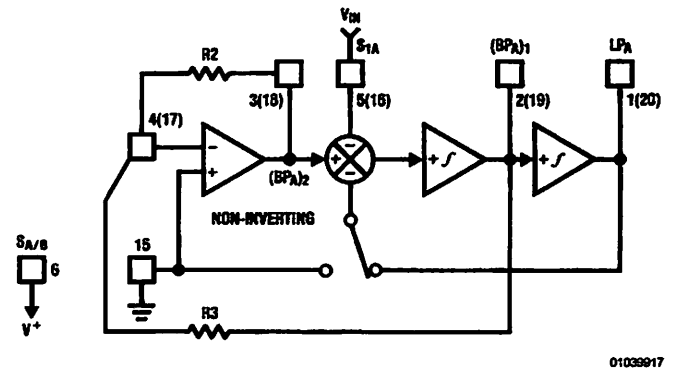


FIGURE 8. MODE 1a

MODE 2: Notch 2, Bandpass, Lowpass: $f_{notch} < f_O$ (See *Figure 9*)

f_O = center frequency

$$= \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}+1} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}+1}$$

$$f_{notch} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

Q = quality factor of the complex pole pair

$$= \frac{\sqrt{R2/R4+1}}{R2/R3}$$

H_{OLP} = Lowpass output gain (as f → 0)

$$= -\frac{R2/R1}{R2/R4+1}$$

H_{OBP} = Bandpass output gain (at f = f_O) = −R3/R1

H_{ON_1} = Notch output gain (as f → 0)

$$= -\frac{R2/R1}{R2/R4+1}$$

$$H_{ON_2} = \text{Notch output gain}\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$$

Filter dynamics: $H_{OBP} = Q\sqrt{H_{OLP}\,H_{ON_2}} = \sqrt{H_{ON1}\,H_{ON2}}$

MODE 3: Highpass, Bandpass, Lowpass Outputs (See *Figure 10*)

$$f_O = \frac{f_{CLK}}{100}\times\sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\times\sqrt{\frac{R2}{R4}}$$

Q = quality factor of the complex pole pair

$$= \sqrt{\frac{R2}{R4}}\times\frac{R3}{R2}$$

$$H_{OHP} = \text{Highpass Gain}\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$$

$$H_{OBP} = \text{Lowpass Gain}\left(\text{at } f = f_O\right) = -\frac{R3}{R1}$$

$$H_{OLP} = \text{Lowpass Gain}\left(\text{as } f \rightarrow 0\right) = -\frac{R4}{R1}$$

Circuit dynamics: $\frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}$;

$$H_{OBP} = \sqrt{H_{OHP}\times H_{OLP}}\times Q$$

$H_{OLP(peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OHP(peak)} \cong Q \times H_{OHP}$ (for high Q's)

2.0 Modes of Operation (Continued)

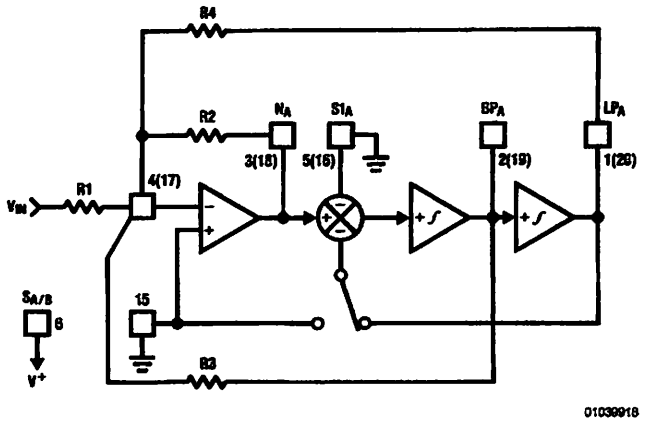
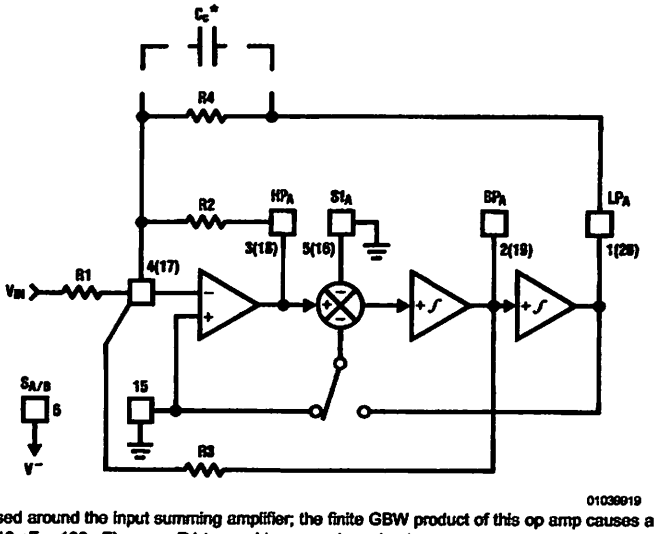


FIGURE 9. MODE 2



*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF − 100 pF) across R4 to provide some phase lead.

FIGURE 10. MODE 3

2.0 Modes of Operation (Continued)

MODE 3a: HP, BP, LP and Notch with External Op Amp (See *Figure 11*)

$$f_O = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

$$f_n = \text{notch frequency} = \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_l}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_l}}$$

$$H_{ON} = \text{gain of notch at}$$

$$f = f_O = \left\| Q\left(\frac{R_g}{R_l}H_{OLP} - \frac{R_g}{R_h}H_{OHP}\right)\right\|$$

$$H_{n1} = \text{gain of notch (as } f \rightarrow 0) = \frac{R_g}{R_l} \times H_{OLP}$$

$$H_{n2} = \text{gain of notch}\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right)$$

$$= -\frac{R_g}{R_h} \times H_{OHP}$$

MODE 4: Allpass, Bandpass, Lowpass Outputs(See *Figure 12*)

f_O = center frequency

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50},$$

f_z* = center frequency of the complex zero $\approx f_O$

$$Q = \frac{f_O}{BW} = \frac{R3}{R2},$$

Q_Z = quality factor of complex zero pair $= \frac{R3}{R1}$

For AP output make R1 = R2

$$H_{OAP}^* = \text{Allpass gain}\left(\text{at } 0 < f < \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1} = -1$$

$$H_{OLP} = \text{Lowpass gain (as } f \rightarrow 0)$$

$$= -\left(\frac{R2}{R1} + 1\right) = -2$$

$$H_{OBP} = \text{Bandpass gain (at } f = f_O)$$

$$= -\frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right)$$

Circuit Dynamics: $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)Q$

*Due to the sampled data nature of the filter, a slight mismatch of f_z and f_O occurs causing a 0.4 dB peaking around f_O of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

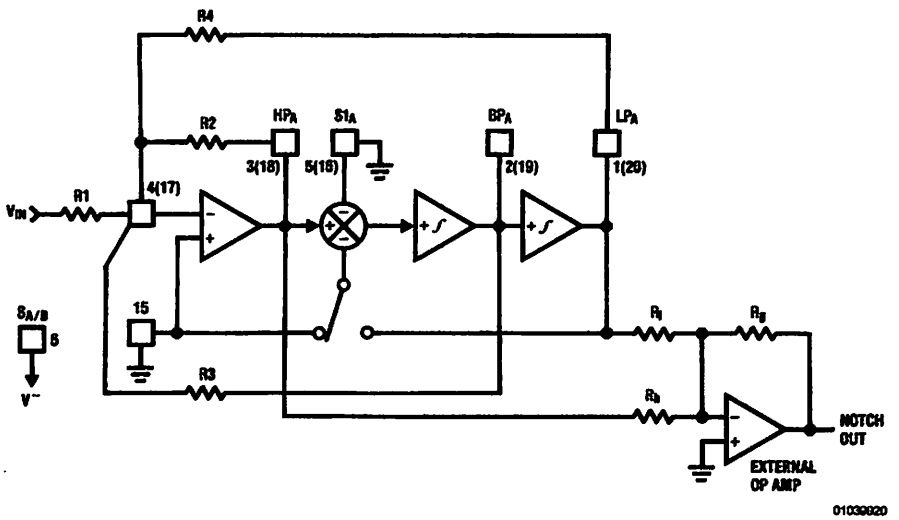


FIGURE 11. MODE 3a

2.0 Modes of Operation (Continued)

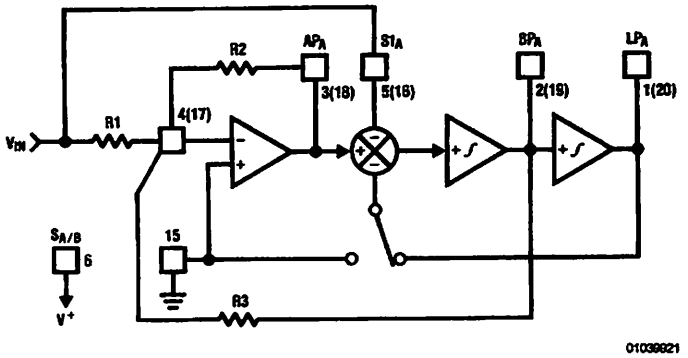


FIGURE 12. MODE 4

MODE 5: Numerator Complex Zeros, BP, LP (See *Figure 13*)

$$f_O = \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{50}$$

$$f_Z = \sqrt{1 - \frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 - \frac{R1}{R4}} \times \frac{f_{CLK}}{50}$$

$$Q = \sqrt{1 + R2/R4} \times \frac{R3}{R2}$$

$$Q_Z = \sqrt{1 - R1/R4} \times \frac{R3}{R1}$$

$H_{0_{Z1}}$ = gain at C.Z. output (as f → 0 Hz)

$$\frac{-R2(R4 - R1)}{R1(R2 + R4)}$$

$H_{0_{Z2}}$ = gain at C.Z. output $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = \frac{-R2}{R1}$

$$H_{OBP} = -\left(\frac{R2}{R1} + 1\right) \times \frac{R3}{R2}$$

$$H_{OLP} = -\left(\frac{R2 + R1}{R2 + R4}\right) \times \frac{R4}{R1}$$

MODE 6a: Single Pole, HP, LP Filter (See *Figure 14*)

f_C = cutoff frequency of LP or HP output

$$= \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

MODE 6b: Single Pole LP Filter (Inverting and Non-Inverting) (See *Figure 15*)

f_C = cutoff frequency of LP outputs

$$\cong \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

H_{OLP1} = 1 (non-inverting)

$$H_{OLP2} = -\frac{R3}{R2}$$

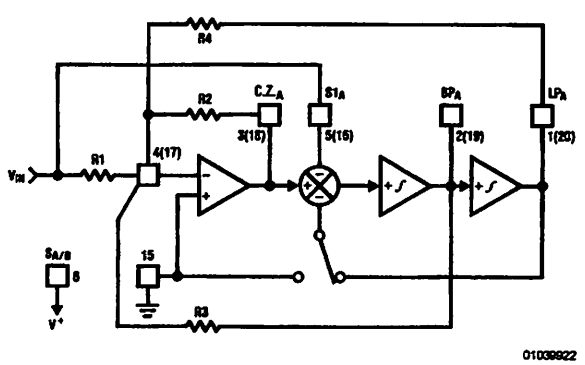


FIGURE 13. MODE 5

2.0 Modes of Operation (Continued)

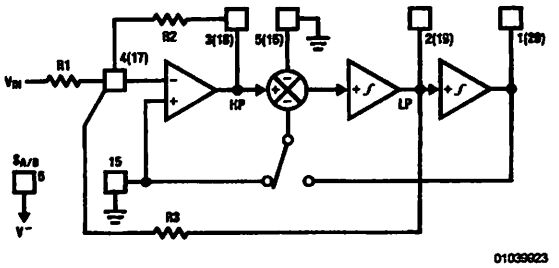


FIGURE 14. MODE 6a

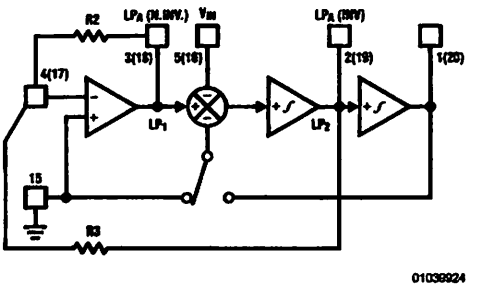


FIGURE 15. MODE 6b

TABLE 1. Summary of Modes. Realizable filter types (e.g. low-pass) denoted by asterisks. Unless otherwise noted, gains of various filter outputs are inverting and adjustable by resistor ratios.

Mode	BP	LP	HP	N	AP	Number of Resistors	Adjustable f_{CLK}/f_O	Notes
1	*	*		*		3	No	
1a	(2) $H_{OBP1} = -Q$ $H_{OBP2} = +1$	$H_{OLP} + 1$				2	No	May need input buffer. Poor dynamics for high Q.
2	*	*		*		3	Yes (above $f_{CLK}/50$ or $f_{CLK}/100$)	
3	*	*	*			4	Yes	Universal State-Variable Filter. Best general-purpose mode.
3a	*	*	*	*		7	Yes	As above, but also includes resistor-tuneable notch.
4	*	*			*	3	No	Gives Allpass response with $H_{OAP} = -1$ and $H_{OLP} = -2$.
5	*	*			*	4		Gives flatter allpass response than above if $R_1 = R_2 = 0.02R_4$.
6a		*	*			3		Single pole.
6b		(2) $H_{OLP1} = +1$ $H_{OLP2} = \frac{-R3}{R2}$				2		Single pole.

3.0 Applications Information

The MF10 is a general-purpose dual second-order state variable filter whose center frequency is proportional to the frequency of the square wave applied to the clock input (f_{CLK}). By connecting pin 12 to the appropriate DC voltage, the filter center frequency f_O can be made equal to either $f_{CLK}/100$ or $f_{CLK}/50$. f_O can be very accurately set (within ±6%) by using a crystal clock oscillator, or can be easily varied over a wide frequency range by adjusting the clock frequency. If desired, the f_{CLK}/f_O ratio can be altered by external resistors as in *Figures 9, 10, 11, 13, 14, 15.* The filter Q and gain are determined by external resistors.

All of the five second-order filter types can be built using either section of the MF10. These are illustrated in *Figure 1* through *Figure 5* along with their transfer functions and some related equations. *Figure 6* shows the effect of Q on the shapes of these curves. When filter orders greater than two are desired, two or more MF10 sections can be cascaded.

3.1 DESIGN EXAMPLE

In order to design a second-order filter section using the MF10, we must define the necessary values of three parameters: f_0, the filter section's center frequency; H_0, the passband gain; and the filter's Q. These are determined by the characteristics required of the filter being designed.

As an example, let's assume that a system requires a fourth-order Chebyshev low-pass filter with 1 dB ripple, unity gain at DC, and 1000 Hz cutoff frequency. As the system order is four, it is realizable using both second-order sections of an MF10. Many filter design texts include tables that list the characteristics (f_O and Q) of each of the second-order filter sections needed to synthesize a given higher-order filter. For the Chebyshev filter defined above, such a table yields the following characteristics:

$f_{0A} = 529$ Hz $Q_A = 0.785$

$f_{0B} = 993$ Hz $Q_B = 3.559$

For unity gain at DC, we also specify:

$H_{0A} = 1$

$H_{0B} = 1$

The desired clock-to-cutoff-frequency ratio for the overall filter of this example is 100 and a 100 kHz clock signal is available. Note that the required center frequencies for the two second-order sections will not be obtainable with clock-to-center-frequency ratios of 50 or 100. It will be necessary to adjust

$$\frac{f_{CLK}}{f_0}$$

externally. From *Table 1*, we see that Mode 3 can be used to produce a low-pass filter with resistor-adjustable center frequency.

In most filter designs involving multiple second-order stages, it is best to place the stages with lower Q values ahead of stages with higher Q, especially when the higher Q is greater than 0.707. This is due to the higher relative gain at the center frequency of a higher-Q stage. Placing a stage with lower Q ahead of a higher-Q stage will provide some attenuation at the center frequency and thus help avoid clipping of signals near this frequency. For this example, stage A has the lower Q (0.785) so it will be placed ahead of the other stage.

For the first section, we begin the design by choosing a convenient value for the input resistance: $R_{1A} = 20k$. The absolute value of the passband gain H_{OLPA} is made equal to 1 by choosing R_{4A} such that: $R_{4A} = -H_{OLPA}R_{1A} = R_{1A} = 20k$. If the 50/100/CL pin is connected to mid-supply for nominal 100:1 clock-to-center-frequency ratio, we find R_{2A} by:

$$R_{2A} = R_{4A}\frac{f_{0A}^2}{(f_{CLK}/100)^2} = 2 \times 10^4 \times \frac{(529)^2}{(1000)^2} = 5.6k \text{ and}$$

$$R_{3A} = Q_A\sqrt{R_{2A}R_{4A}} = 0.785\sqrt{5.6 \times 10^3 \times 2 \times 10^4} = 8.3k$$

The resistors for the second section are found in a similar fashion:

$$R_{1B} = 20k$$

$$R_{4B} = R_{1B} = 20k$$

$$R_{2B} = R_{4B}\frac{f_{0B}^2}{(f_{CLK}/100)^2} = 20k\frac{(993)^2}{(1000)^2} = 19.7k$$

$$R_{3B} = Q_B\sqrt{R_{2B}R_{4B}} = 3.559\sqrt{1.97\times10^4\times2\times10^4} = 70.6k$$

The complete circuit is shown in *Figure 16* for split ±5V power supplies. Supply bypass capacitors are highly recommended.

3.0 Applications Information (Continued)

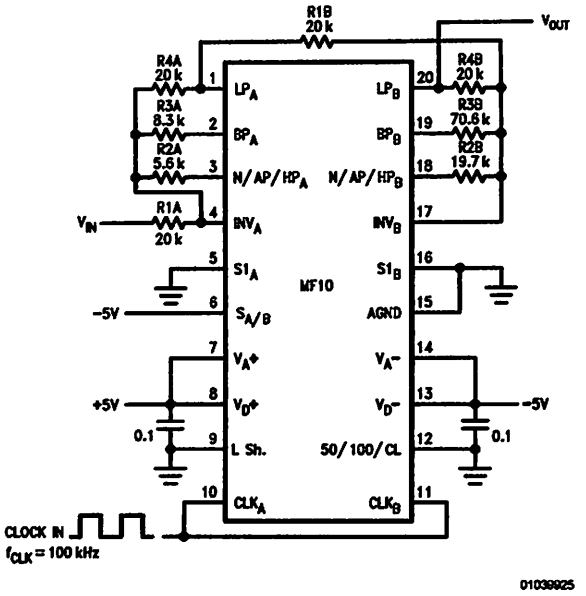


FIGURE 16. Fourth-Order Chebyshev Low-Pass Filter from Example in 3.1. ±5V Power Supply. 0V–5V TTL or −5V ±5V CMOS Logic Levels.

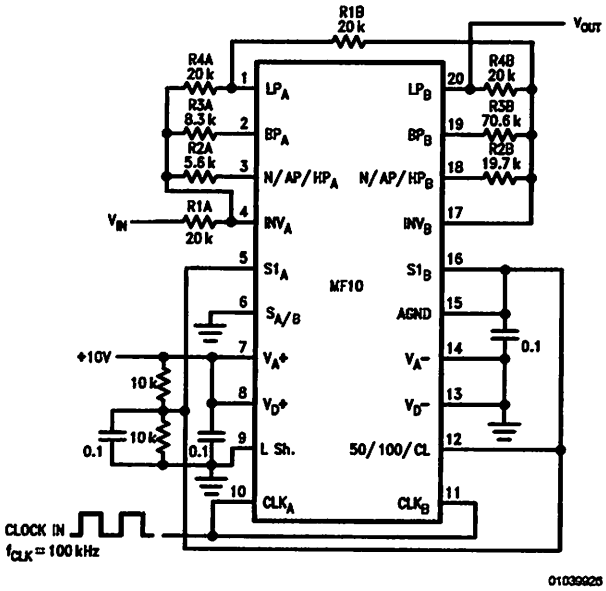
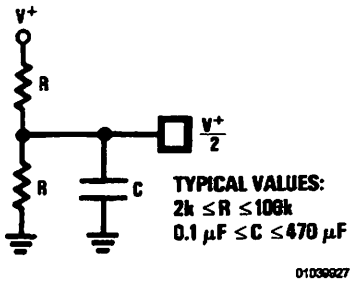
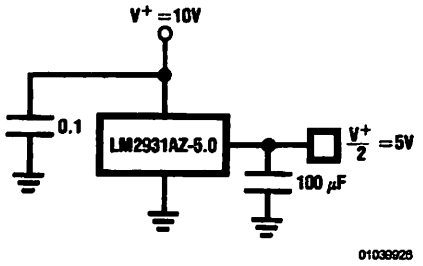


FIGURE 17. Fourth-Order Chebyshev Low-Pass Filter from Example in 3.1. Single +10V Power Supply. 0V–5V TTL Logic Levels. Input Signals Should be Referred to Half-Supply or Applied through a Coupling Capacitor.

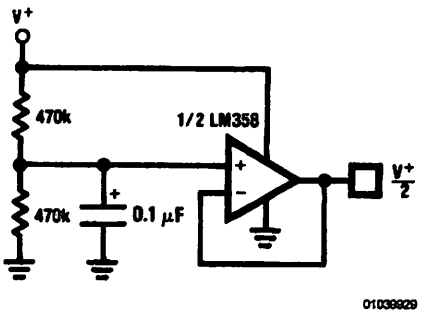
3.0 Applications Information (Continued)



(a) Resistive Divider with Decoupling Capacitor



(b) Voltage Regulator



(c) Operational Amplifier with Divider

FIGURE 18. Three Ways of Generating $V^+/2$ for Single-Supply Operation

3.0 Applications Information

(Continued)

3.2 SINGLE SUPPLY OPERATION

The MF10 can also operate with a single-ended power supply. *Figure 17* shows the example filter with a single-ended power supply. V_A^+ and V_D^+ are again connected to the positive power supply (8V to 14V), and V_A^- and V_D^- are connected to ground. The A_{GND} pin must be tied to $V^+/2$ for single supply operation. This half-supply point should be very "clean", as any noise appearing on it will be treated as an input to the filter. It can be derived from the supply voltage with a pair of resistors and a bypass capacitor (*Figure 18a*), or a low-impedance half-supply voltage can be made using a three-terminal voltage regulator or an operational amplifier (*Figure 18b* and *Figure 18c*). The passive resistor divider with a bypass capacitor is sufficient for many applications, provided that the time constant is long enough to reject any power supply noise. It is also important that the half-supply reference present a low impedance to the clock frequency, so at very low clock frequencies the regulator or op-amp approaches may be preferable because they will require smaller capacitors to filter the clock frequency. The main power supply voltage should be clean (preferably regulated) and bypassed with 0.1 µF.

3.3 DYNAMIC CONSIDERATIONS

The maximum signal handling capability of the MF10, like that of any active filter, is limited by the power supply voltages used. The amplifiers in the MF10 are able to swing to within about 1V of the supplies, so the input signals must be kept small enough that none of the outputs will exceed these limits. If the MF10 is operating on ±5V, for example, the outputs will clip at about 8 V_{p-p}. The maximum input voltage multiplied by the filter gain should therefore be less than 8 V_{p-p}.

Note that if the filter Q is high, the gain at the lowpass or highpass outputs will be much greater than the nominal filter gain (*Figure 6*). As an example, a lowpass filter with a Q of 10 will have a 20 dB peak in its amplitude response at f_O. If the nominal gain of the filter H_{OLP} is equal to 1, the gain at f_O will be 10. The maximum input signal at f_O must therefore be less than 800 mV_{p-p} when the circuit is operated on ±5V supplies.

Also note that one output can have a reasonable small voltage on it while another is saturated. This is most likely for a circuit such as the notch in Mode 1 (*Figure 7*). The notch output will be very small at f_O, so it might appear safe to apply a large signal to the input. However, the bandpass will have its maximum gain at f_O and can clip if overdriven. If one output clips, the performance at the other outputs will be degraded, so avoid overdriving any filter section, even ones whose outputs are not being directly used. Accompanying *Figure 7* through *Figure 15* are equations labeled "circuit dynamics", which relate the Q and the gains at the various outputs. These should be consulted to determine peak circuit gains and maximum allowable signals for a given application.

3.4 OFFSET VOLTAGE

The MF10's switched capacitor integrators have a higher equivalent input offset voltage than would be found in a typical continuous-time active filter integrator. *Figure 19* shows an equivalent circuit of the MF10 from which the output DC offsets can be calculated. Typical values for these offsets with $S_{A/B}$ tied to V^+ are:

V_{os1} = opamp offset = ±5 mV

V_{os2} = −150 mV @ 50:1: −300 mV @ 100:1

V_{os3} = −70 mV @ 50:1: −140 mV @ 100:1

When $S_{A/B}$ is tied to V^-, V_{os2} will approximately halve. The DC offset at the BP output is equal to the input offset of the lowpass integrator (V_{os3}). The offsets at the other outputs depend on the mode of operation and the resistor ratios, as described in the following expressions.

Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1\left\|H_{OLP}\right\|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 1a

$$V_{OS(N.INV.BP)} = \left(1 + \frac{1}{Q}\right) V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2}$$

3.0 Applications Information
(Continued)

Mode 2 and Mode 5

$$V_{OS(N)} = \left(\frac{R2}{R_p} + 1\right) V_{OS1} \times \frac{1}{1 + R2/R4}$$

$$+ V_{OS2} \frac{1}{1 + R4/R2} - \frac{V_{OS3}}{Q\sqrt{1 + R2/R4}}:$$

$$R_p = R1//R3//R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 3

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS1}\left[1 + \frac{R4}{R_p}\right] - V_{OS2}\left(\frac{R4}{R2}\right)$$

$$-V_{OS3}\left(\frac{R4}{R3}\right)$$

$$Rp = R1//R2//R3$$

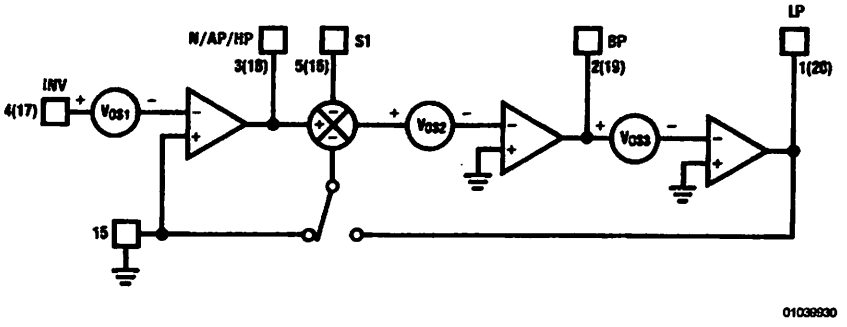


FIGURE 19. MF10 Offset Voltage Sources

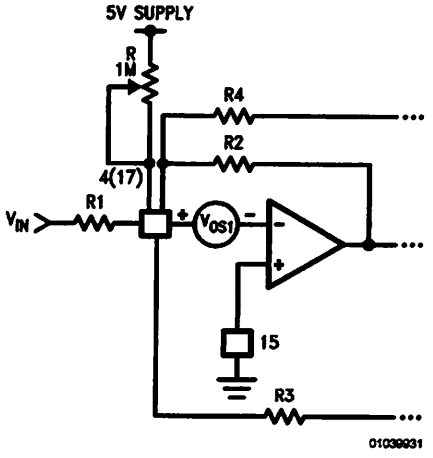


FIGURE 20. Method for Trimming V_{OS}

For most applications, the outputs are AC coupled and DC offsets are not bothersome unless large signals are applied to the filter input. However, larger offset voltages will cause clipping to occur at lower AC signal levels, and clipping at

3.0 Applications Information

(Continued)

any of the outputs will cause gain nonlinearities and will change f_O and Q. When operating in Mode 3, offsets can become excessively large if R2 and R4 are used to make f_{CLK}/f_O significantly higher than the nominal value, especially if Q is also high. An extreme example is a bandpass filter having unity gain, a Q of 20, and f_{CLK}/f_O = 250 with pin 12 tied to ground (100:1 nominal). R4/R2 will therefore be equal to 6.25 and the offset voltage at the lowpass output will be about +1V. Where necessary, the offset voltage can be adjusted by using the circuit of *Figure 20*. This allows adjustment of V_{OS1}, which will have varying effects on the different outputs as described in the above equations. Some outputs cannot be adjusted this way in some modes, however ($V_{OS(BP)}$ in modes 1a and 3, for example).

3.5 SAMPLED DATA SYSTEM CONSIDERATIONS

The MF10 is a sampled data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The MF10's sampling frequency is the same as its clock frequency.) If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_s/2$ + 100 Hz will cause the system to respond as though the input frequency was $f_s/2$ − 100 Hz. This phenomenon is known as "aliasing", and can be reduced or eliminated by limiting the input signal spectrum to less than $f_s/2$. This may in some cases require the use of a bandwidth-limiting filter ahead of the MF10 to limit the input spectrum. However, since the clock frequency is much higher than the center frequency, this will often not be necessary.

Another characteristic of sampled-data circuits is that the output signal changes amplitude once every sampling period, resulting in "steps" in the output voltage which occur at the clock rate (*Figure 21*). If necessary, these can be "smoothed" with a simple R–C low-pass filter at the MF10 output.

The ratio of f_{CLK} to f_C (normally either 50:1 or 100:1) will also affect performance. A ratio of 100:1 will reduce any aliasing problems and is usually recommended for wideband input signals. In noise sensitive applications, however, a ratio of 50:1 may be better as it will result in 3 dB lower output noise. The 50:1 ratio also results in lower DC offset voltages, as discussed in Section 3.4.

The accuracy of the f_{CLK}/f_O ratio is dependent on the value of Q. This is illustrated in the curves under the heading "Typical Performance Characteristics". As Q is changed, the true value of the ratio changes as well. Unless the Q is low, the error in f_{CLK}/f_O will be small. If the error is too large for a specific application, use a mode that allows adjustment of the ratio with external resistors.

It should also be noted that the product of Q and f_O should be limited to 300 kHz when f_O < 5 kHz, and to 200 kHz for f_O > 5 kHz.

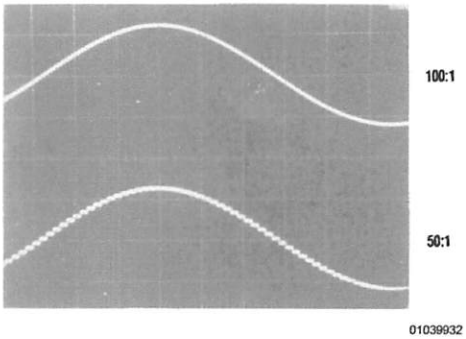
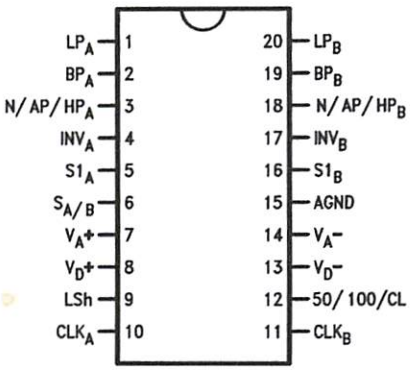


FIGURE 21. The Sampled-Data Output Waveform

3.0 Applications Information (Continued)

Connection Diagram

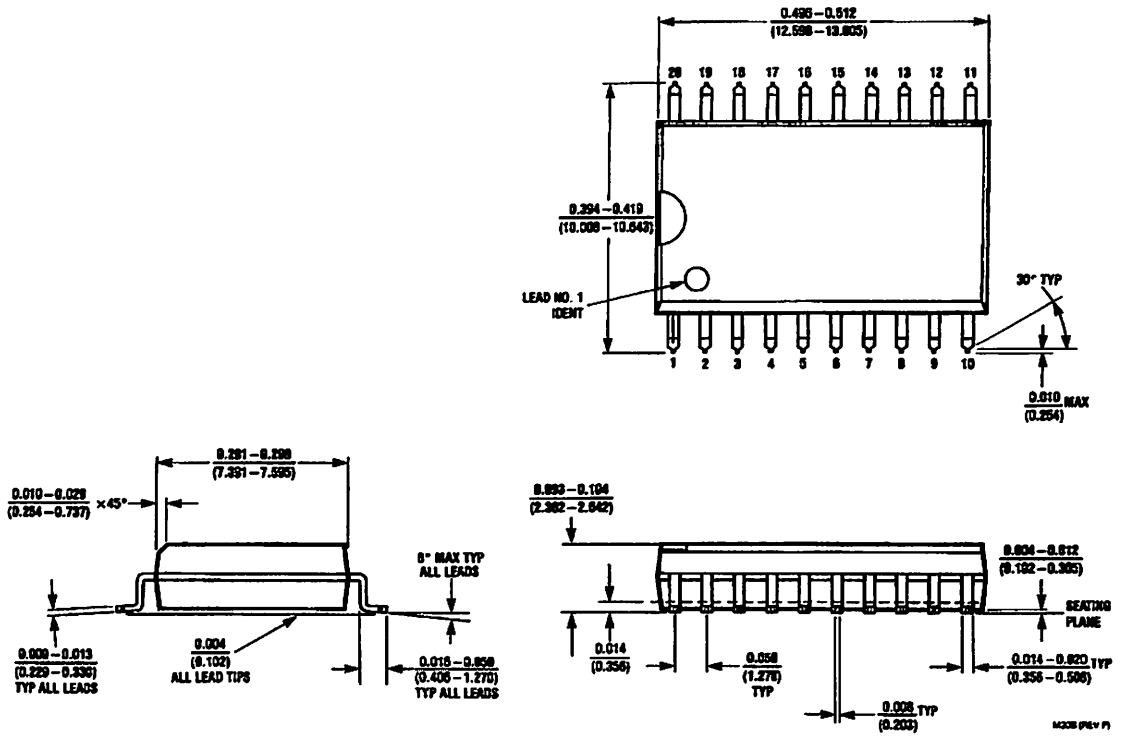
Surface Mount and Dual-In-Line Package



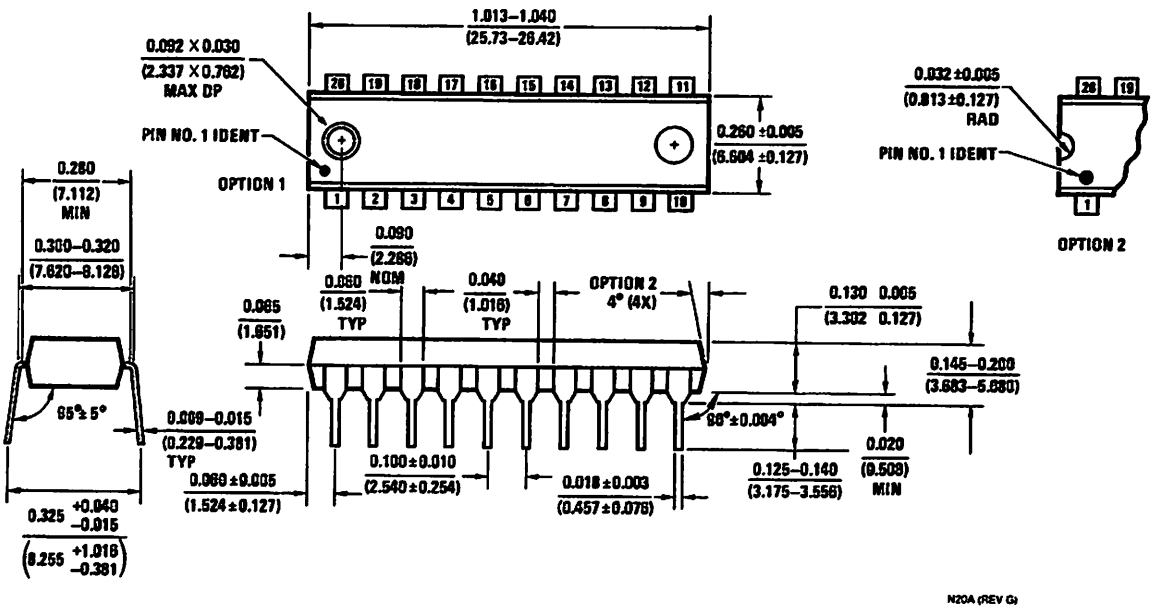
Top View
Order Number MF10CCWM
See NS Package Number M20B
Order Number MF10ACN or MF10CCN
See NS Package Number N20A

Physical Dimensions inches (millimeters)

unless otherwise noted



Molded Package (Small Outline) (M)
Order Number MF10ACWM or MF10CCWM
NS Package Number M20B



20-Lead Molded Dual-In-Line Package (N)
Order Number MF10ACN or MF10CCN
NS Package Number N20A

Notes

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
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Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 130 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 8K Bytes of In-System Self-programmable Flash program memory
  - 512 Bytes EEPROM
  - 1K Byte Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C[1]
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler, one Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Three PWM Channels
  - 8-channel ADC in TQFP and QFN/MLF package
    Eight Channels 10-bit Accuracy
  - 6-channel ADC in PDIP package
    Six Channels 10-bit Accuracy
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Five Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, and Standby
- I/O and Packages
  - 23 Programmable I/O Lines
  - 28-lead PDIP, 32-lead TQFP, and 32-pad QFN/MLF
- Operating Voltages
  - 2.7 - 5.5V (ATmega8L)
  - 4.5 - 5.5V (ATmega8)
- Speed Grades
  - 0 - 8 MHz (ATmega8L)
  - 0 - 16 MHz (ATmega8)
- Power Consumption at 4 Mhz, 3V, 25°C
  - Active: 3.6 mA
  - Idle Mode: 1.0 mA
  - Power-down Mode: 0.5 µA

8-bit AVR® with 8K Bytes In-System Programmable Flash

ATmega8
ATmega8L

Summary

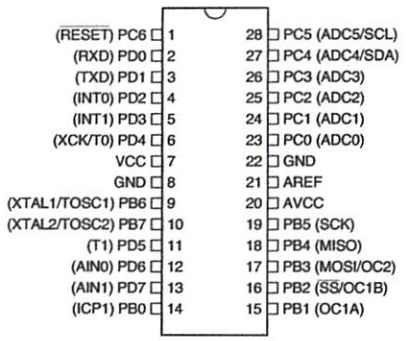
8-bit AVR with 8K Bytes In-System Programmable Flash

ATmega8
ATmega8L

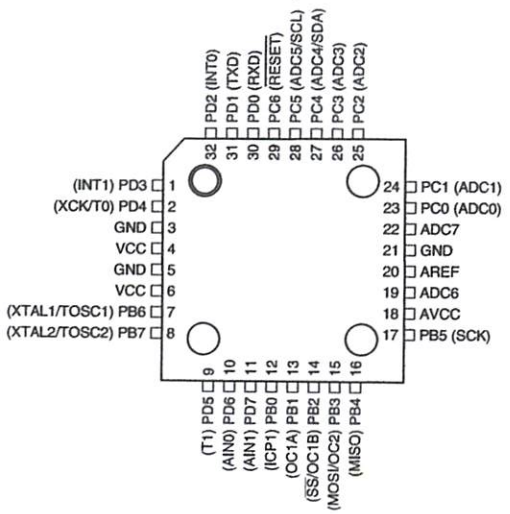
Summary

Pin Configurations

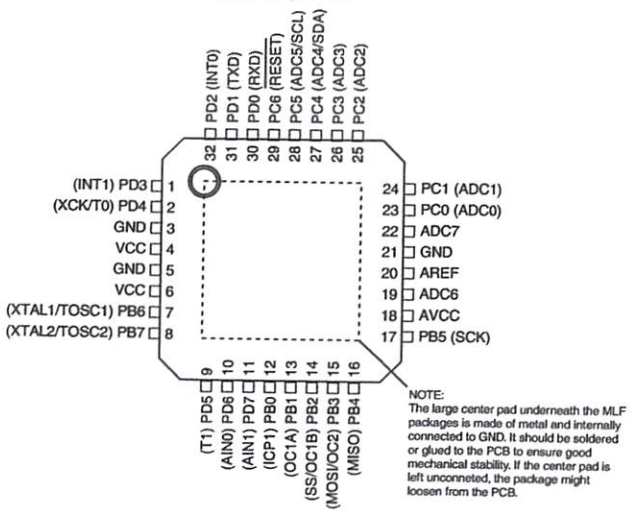
PDIP



TQFP Top View



MLF Top View



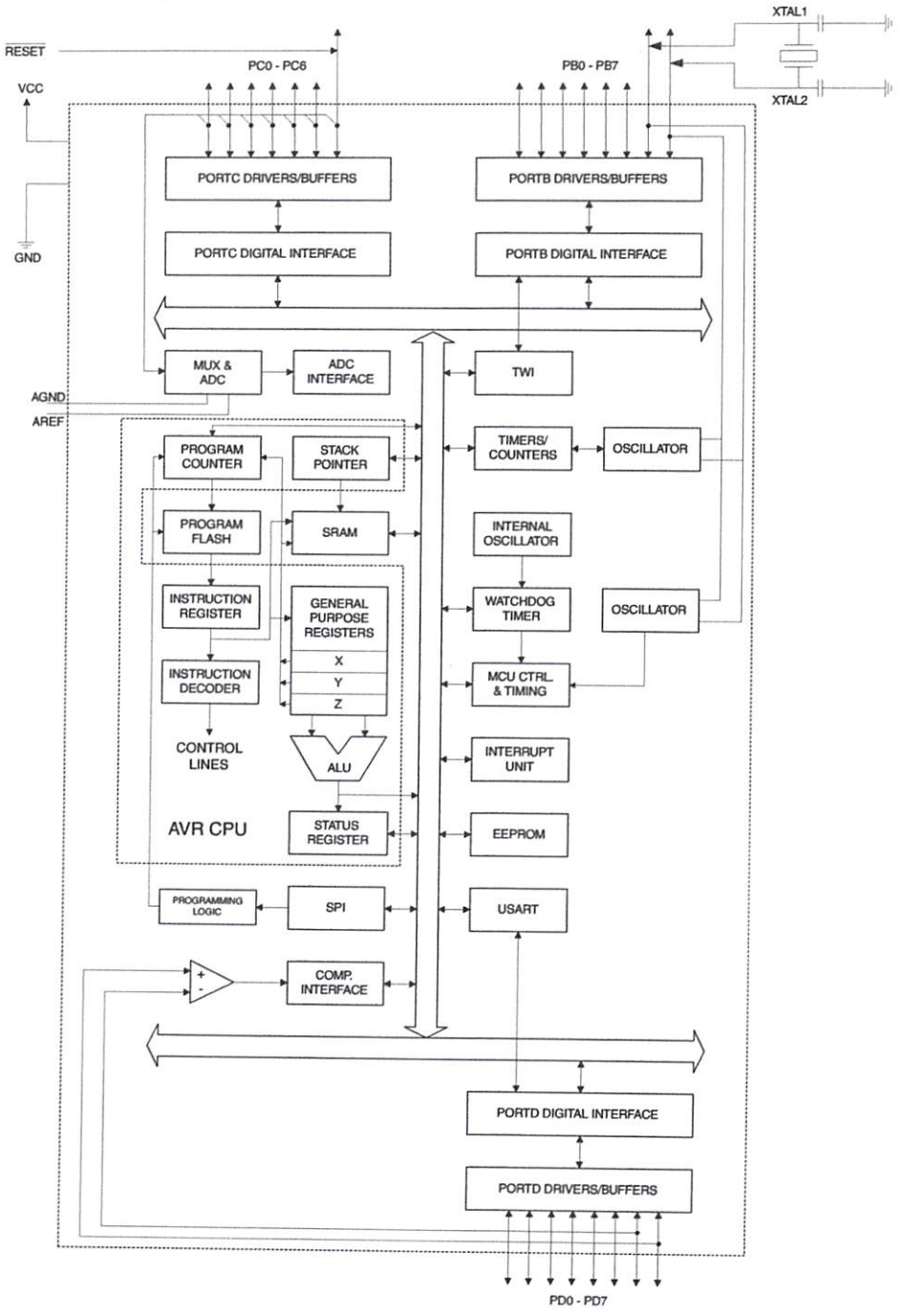
NOTE:
The large center pad underneath the MLF packages is made of metal and internally connected to GND. It should be soldered or glued to the PCB to ensure good mechanical stability. If the center pad is left unconneted, the package might loosen from the PCB.

Overview

The ATmega8 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8 achieves throughputs approaching 1 MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 1. Block Diagram



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Block Diagram

Figure 1. Block Diagram

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8 provides the following features: 8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes of EEPROM, 1K byte of SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, a 6-channel ADC (eight channels in TQFP and QFN/MLF packages) with 10-bit accuracy, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next Interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The Flash Program memory can be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash Section will continue to run while the Application Flash Section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega8 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega8 AVR is supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, In-Circuit Emulators, and evaluation kits.

Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

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Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

Pin Descriptions

VCC

Digital supply voltage.

GND

Ground.

Port B (PB7..PB0) XTAL1/XTAL2/TOSC1/ TOSC2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier.

If the Internal Calibrated RC Oscillator is used as chip clock source, PB7..6 is used as TOSC2..1 input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

The various special features of Port B are elaborated in "Alternate Functions of Port B" on page 58 and "System Clock and Clock Options" on page 25.

Port C (PC5..PC0)

Port C is an 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

PC6/$\overline{\text{RESET}}$

If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 38. Shorter pulses are not guaranteed to generate a Reset.

The various special features of Port C are elaborated on page 61.

Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega8 as listed on page 63.

$\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 38. Shorter pulses are not guaranteed to generate a reset.

Pin Descriptions

VCC	Digital supply voltage.
GND	Ground.
Port B (PB7..PB0) XTAL1/XTAL2/TOSC1/TOSC2	Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running. Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit. Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier. If the internal Calibrated RC Oscillator is used as chip clock source, PB7..6 is used as TOSC2..1 input for the Asynchronous Timer/Counter if the AS2 bit in ASSR is set. The various special features of Port B are elaborated in [illegible] and [illegible].
Port C (PC5..PC0)	Port C is an 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.
PC6/RESET	If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C. If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in [illegible]. Shorter pulses are not guaranteed to generate a Reset. The various special features of Port C are elaborated on [illegible].
Port D (PD7..PD0)	Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port D also serves the functions of various special features of the ATmega8 as listed on [illegible].
RESET	Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in [illegible]. Shorter pulses are not guaranteed to generate a reset.

AV_{CC}

AV_{CC} is the supply voltage pin for the A/D Converter, Port C (3..0), and ADC (7..6). It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. Note that Port C (5..4) use digital supply voltage, V_{CC}.

AREF

AREF is the analog reference pin for the A/D Converter.

ADC7..6 (TQFP and QFN/MLF Package Only)

In the TQFP and QFN/MLF package, ADC7..6 serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

AV_{CC}	AV_{CC} is the supply voltage pin for the A/D Converter, Port C (3..0), and ADC (7..6). It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. Note that Port C (3..0) use digital supply voltage, V_{CC}.
AREF	AREF is the analog reference pin for the A/D Converter.
ADC7..6 (TQFP and QFN/MLF Package Only)	In the TQFP and QFN/MLF package, ADC7..6 serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	11
0x3E (0x5E)	SPH	–	–	–	–	–	SP10	SP9	SP8	13
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	13
0x3C (0x5C)	Reserved									
0x3B (0x5B)	GICR	INT1	INT0	–	–	–	–	IVSEL	IVCE	49, 67
0x3A (0x5A)	GIFR	INTF1	INTF0	–	–	–	–	–	–	68
0x39 (0x59)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	–	TOIE0	72, 102, 122
0x38 (0x58)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	–	TOV0	73, 102, 122
0x37 (0x57)	SPMCR	SPMIE	RWWSB	–	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	213
0x36 (0x56)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	171
0x35 (0x55)	MCUCR	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	33, 66
0x34 (0x54)	MCUCSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	41
0x33 (0x53)	TCCR0	–	–	–	–	–	CS02	CS01	CS00	72
0x32 (0x52)	TCNT0	Timer/Counter0 (8 Bits)								72
0x31 (0x51)	OSCCAL	Oscillator Calibration Register								31
0x30 (0x50)	SFIOR	–	–	–	–	ACME	PUD	PSR2	PSR10	58, 75, 123, 193
0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	96
0x2E (0x4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	100
0x2D (0x4D)	TCNT1H	Timer/Counter1 – Counter Register High byte								101
0x2C (0x4C)	TCNT1L	Timer/Counter1 – Counter Register Low byte								101
0x2B (0x4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High byte								101
0x2A (0x4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low byte								101
0x29 (0x49)	OCR1BH	Timer/Counter1 – Output Compare Register B High byte								101
0x28 (0x48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low byte								101
0x27 (0x47)	ICR1H	Timer/Counter1 – Input Capture Register High byte								102
0x26 (0x46)	ICR1L	Timer/Counter1 – Input Capture Register Low byte								102
0x25 (0x45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	117
0x24 (0x44)	TCNT2	Timer/Counter2 (8 Bits)								119
0x23 (0x43)	OCR2	Timer/Counter2 Output Compare Register								119
0x22 (0x42)	ASSR	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	119
0x21 (0x41)	WDTCR	–	–	–	WDCE	WDE	WDP2	WDP1	WDP0	43
0x20[1] (0x40)[1]	UBRRH	URSEL	–	–	–	UBRR[11:8]				158
	UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	156
0x1F (0x3F)	EEARH	–	–	–	–	–	–	–	EEAR8	20
0x1E (0x3E)	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	20
0x1D (0x3D)	EEDR	EEPROM Data Register								20
0x1C (0x3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	20
0x1B (0x3B)	Reserved									
0x1A (0x3A)	Reserved									
0x19 (0x39)	Reserved									
0x18 (0x38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	65
0x17 (0x37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	65
0x16 (0x36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	65
0x15 (0x35)	PORTC	–	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	65
0x14 (0x34)	DDRC	–	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	65
0x13 (0x33)	PINC	–	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	65
0x12 (0x32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	65
0x11 (0x31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	65
0x10 (0x30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	65
0x0F (0x2F)	SPDR	SPI Data Register								131
0x0E (0x2E)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	131
0x0D (0x2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	129
0x0C (0x2C)	UDR	USART I/O Data Register								153
0x0B (0x2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	154
0x0A (0x2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	155
0x09 (0x29)	UBRRL	USART Baud Rate Register Low byte								158
0x08 (0x28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	194
0x07 (0x27)	ADMUX	REFS1	REFS0	ADLAR	–	MUX3	MUX2	MUX1	MUX0	205
0x06 (0x26)	ADCSRA	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	207
0x05 (0x25)	ADCH	ADC Data Register High byte								208
0x04 (0x24)	ADCL	ADC Data Register Low byte								208
0x03 (0x23)	TWDR	Two-wire Serial Interface Data Register								173
0x02 (0x22)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	174

Register Summary (Continued)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x01 (0x21)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0	173
0x00 (0x20)	TWBR	Two-wire Serial Interface Bit Rate Register								171

Notes:
1. Refer to the USART description for details on how to access UBRRH and UCSRC.
2. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
3. Some of the Status Flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← 0xFF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • (0xFF - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← 0xFF	None	1
MUL	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z,C	2
MULS	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1 / 2 / 3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
Mnemonics	**Operands**	**Description**	**Operation**	**Flags**	**#Clocks**

Instruction Set Summary (Continued)

BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
Mnemonics	**Operands**	**Description**	**Operation**	**Flags**	**#Clocks**

Instruction Set Summary (Continued)

CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package[1]	Operation Range
8	2.7 - 5.5	ATmega8L-8AU[2] ATmega8L-8PU[2] ATmega8L-8MU[2]	32A 28P3 32M1-A	Industrial (-40°C to 85°C)
16	4.5 - 5.5	ATmega8-16AU[2] ATmega8-16PU[2] ATmega8-16MU[2]	32A 28P3 32M1-A	Industrial (-40°C to 85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

Package Type	
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
28P3	28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
32M1-A	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

Ordering Information

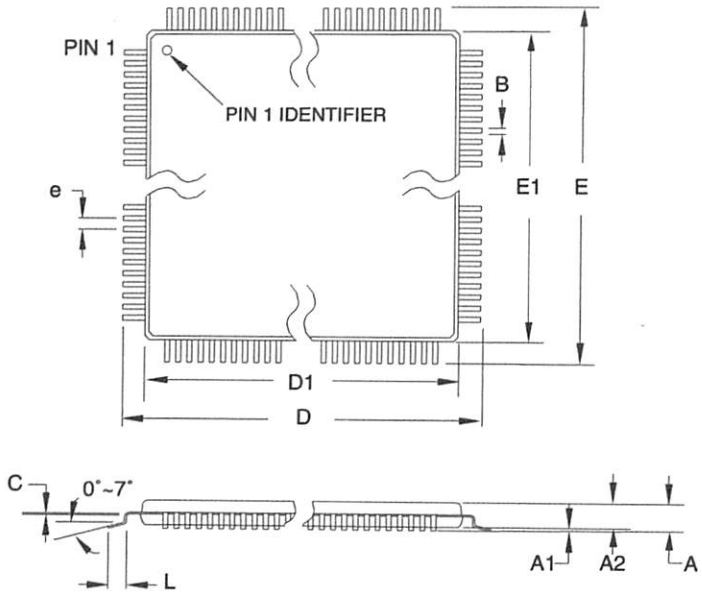
Press (MPa)	Power Supply	Ordering Code	Package	Description/Range
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering and numbering information quantities.

2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS Directive). Also Halide free and fully Green.

	Package Type
3SA	[illegible]
3SB3	[illegible]
3SM1-A	[illegible]

32A



COMMON DIMENSIONS
(Unit of Measure = mm)

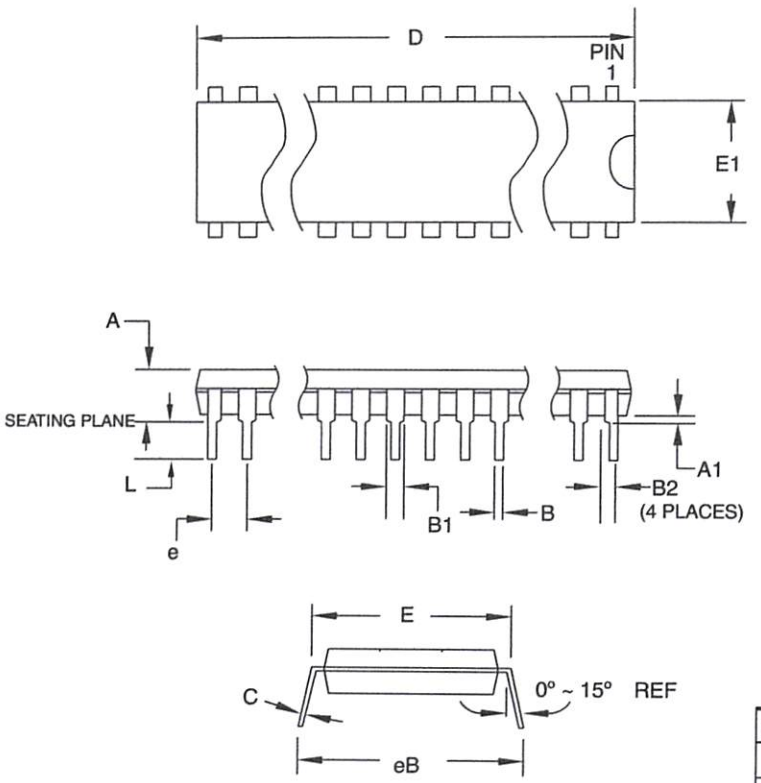
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32A,** 32-lead, 7 x 7 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	32A	B

28P3



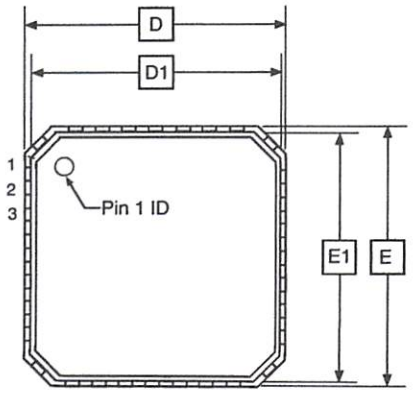
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.5724	
A1	0.508	–	–	
D	34.544	–	34.798	Note 1
E	7.620	–	8.255	
E1	7.112	–	7.493	Note 1
B	0.381	–	0.533	
B1	1.143	–	1.397	
B2	0.762	–	1.143	
L	3.175	–	3.429	
C	0.203	–	0.356	
eB	–	–	10.160	
e	2.540 TYP			

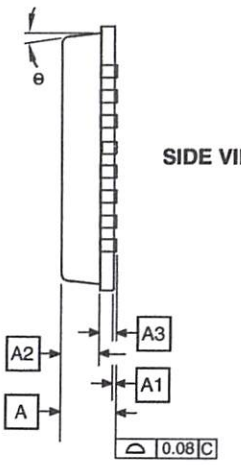
Note: 1. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

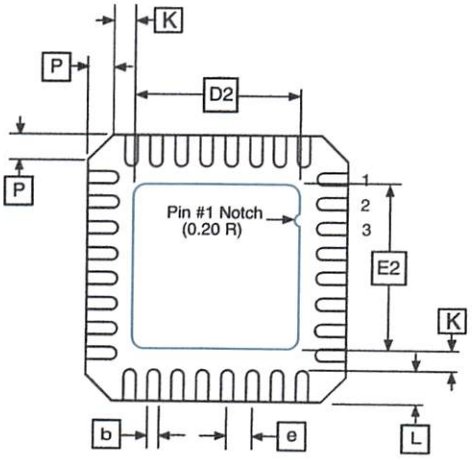
	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28P3**, 28-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	28P3	B



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A2	–	0.65	1.00	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	4.90	5.00	5.10	
D1	4.70	4.75	4.80	
D2	2.95	3.10	3.25	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	2.95	3.10	3.25	
e		0.50 BSC		
L	0.30	0.40	0.50	
P	–	–	0.60	
θ	–	–	12°	
K	0.20	–	–	

Note: JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.

5/25/06

2325 Orchard Parkway San Jose, CA 95131	TITLE **32M1-A**, 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm, 3.10 mm Exposed Pad, Micro Lead Frame Package (MLF)	DRAWING NO. 32M1-A	REV. E

Errata

The revision letter in this section refers to the revision of the ATmega8 device.

ATmega8 Rev. D to I

- **First Analog Comparator conversion may be delayed**
- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **Signature may be Erased in Serial Programming Mode**
- **CKOPT Does not Enable Internal Capacitors on XTALn/TOSCn Pins when 32 KHz Oscillator is Used to Clock the Asynchronous Timer/Counter2**
- **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request**

1. **First Analog Comparator conversion may be delayed**

   If the device is powered by a slow rising V_{CC}, the first Analog Comparator conversion will take longer than expected on some devices.

   Problem Fix / Workaround

   When the device has been powered or reset, disable then enable theAnalog Comparator before the first conversion.

2. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   If one of the timer registers which is synchronized to the asynchronous timer2 clock is written in the cycle before a overflow interrupt occurs, the interrupt may be lost.

   Problem Fix / Workaround

   Always check that the Timer2 Timer/Counter register, TCNT2, does not have the value 0xFF before writing the Timer2 Control Register, TCCR2, or Output Compare Register, OCR2

3. **Signature may be Erased in Serial Programming Mode**

   If the signature bytes are read before a chiperase command is completed, the signature may be erased causing the device ID and calibration bytes to disappear. This is critical, especially, if the part is running on internal RC oscillator.

   Problem Fix / Workaround:

   Ensure that the chiperase command has exceeded before applying the next command.

4. **CKOPT Does not Enable Internal Capacitors on XTALn/TOSCn Pins when 32 KHz Oscillator is Used to Clock the Asynchronous Timer/Counter2**

   When the internal RC Oscillator is used as the main clock source, it is possible to run the Timer/Counter2 asynchronously by connecting a 32 KHz Oscillator between XTAL1/TOSC1 and XTAL2/TOSC2. But when the internal RC Oscillator is selected as the main clock source, the CKOPT Fuse does not control the internal capacitors on XTAL1/TOSC1 and XTAL2/TOSC2. As long as there are no capacitors connected to XTAL1/TOSC1 and XTAL2/TOSC2, safe operation of the Oscillator is not guaranteed.

   Problem Fix / Workaround

   Use external capacitors in the range of 20 - 36 pF on XTAL1/TOSC1 and XTAL2/TOSC2. This will be fixed in ATmega8 Rev. G where the CKOPT Fuse will control internal capacitors also when internal RC Oscillator is selected as main clock source. For ATmega8 Rev. G, CKOPT = 0 (programmed) will enable the internal capacitors on XTAL1 and XTAL2. Customers who want compatibility between Rev. G and older revisions, must ensure that CKOPT is unprogrammed (CKOPT = 1).

5. **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request.**

   Reading EEPROM by using the ST or STS command to set the EERE bit in the EECR register triggers an unexpected EEPROM interrupt request.

Errata

AT89C668 Rev. D to I

The revision letter in this section refers to the revision of the AT89C668 device.

- First Analog Comparator conversion may be delayed
- Interrupts may be lost when writing the timer registers in the asynchronous timer
- Signature may be Erased in Serial Programming Mode
- CKOPT Does not Enable Internal Capacitors on XTAL1/TOSC1 Pins when 32 kHz Oscillator is Used to Clock the Asynchronous Timer/Counter2
- Reading EEPROM by using ST or STS to set EERE to trigger unexpected internal request

1. First Analog Comparator conversion may be delayed

If the device is powered by a slow rising V_{CC}, the first Analog Comparator conversion will take longer than expected on some devices.

Problem Fix / Workaround

When the device has been powered or reset, ignore the first Analog Comparator conversion before the first conversion.

2. Interrupts may be lost when writing the timer registers in the asynchronous timer

If one of the timer registers which is asynchronized to the asynchronous timer2 clock is written in the cycle before a overflow interrupt occurs, the interrupt may be lost.

Problem Fix / Workaround

Always check that the Timer2 Timer/Counter register (TCNT2) does not have the value 0xFF before writing the Timer2 Control Register, TCCR2, or Output Compare Register, OCR2.

3. Signature may be Erased in Serial Programming Mode

If the sequence to erase a locked before a programming command is issued, the signature may be erased, enabling the device to be reprogrammed. This is a critical security vulnerability if the part is running an internal RC oscillator.

Problem Fix / Workaround

Ensure that the chip erase command has completed before applying the next command.

4. CKOPT Does not Enable Internal Capacitors on XTAL1/TOSC1 Pins when 32 kHz Oscillator is Used to Clock the Asynchronous Timer/Counter2

When the internal RC Oscillator is used as the main clock source, it is possible to run the Timer/Counter2 asynchronously by connecting a 32 kHz Oscillator between XTAL1/TOSC1 and XTAL2/TOSC2. But after the internal RC Oscillator is selected as the main clock source, the CKOPT fuse does not connect the internal capacitors on XTAL1/TOSC1 and XTAL2/TOSC2. According to the datasheet, connecting the XTAL1/TOSC1 and XTAL2/TOSC2 pins directly to the Oscillator is not possible.

Problem Fix / Workaround

Use external capacitors in the range of 20 - 30 pF on XTAL1/TOSC1 and XTAL2/TOSC2. This will be fixed in AT89C668 Rev. D where the CKOPT fuse will connect internal capacitors also when internal RC Oscillator is selected as main clock source. For AT89C668 Rev. D CKOPT = 0 configuration will enable the internal capacitors on XTAL1 and XTAL2. Customers who want compatibility between Rev. D and later revisions should ensure that CKOPT is unprogrammed (CKOPT = 1).

5. Reading EEPROM by using ST or STS to set EERE will trigger unexpected internal request.

Reading EEPROM by using the ST or STS command with the EERE bit in the EECR register will trigger an unexpected EEPROM internal request.

Problem Fix / Workaround

Always use OUT or SBI to set EERE in EECR.

Problem Fix - Workaround

Always use OUT or SIN to see FERS in ECOA.

Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

Changes from Rev. 2486S- 08/07 to Rev. 2486T- 05/08

1. Updated Table 98 on page 240.
2. Updated "Ordering Information" on page 292.
   - Commercial Ordering Code removed.
   - No Pb-free packaging option removed.

Changes from Rev. 2486R- 07/07 to Rev. 2486S- 08/07

1. Updated "Features" on page 1.
2. Added "Data Retention" on page 7.
3. Updated "Errata" on page 17.
4. Updated "Slave Mode" on page 129.

Changes from Rev. 2486Q- 10/06 to Rev. 2486R- 07/07

1. Added text to Table 81 on page 218.
2. Fixed typo in "Peripheral Features" on page 1.
3. Updated Table 16 on page 42.
4. Updated Table 75 on page 206.
5. Removed redundancy and updated typo in Notes section of "DC Characteristics" on page 242.

Changes from Rev. 2486P- 02/06 to Rev. 2486Q- 10/06

1. Updated "Timer/Counter Oscillator" on page 32.
2. Updated "Fast PWM Mode" on page 89.
3. Updated code example in "USART Initialization" on page 138.
4. Updated Table 37 on page 97, Table 39 on page 98, Table 42 on page 117, Table 44 on page 118, and Table 98 on page 240.
5. Updated "Errata" on page 17.

Changes from Rev. 2486O-10/04 to Rev. 2486P- 02/06

1. Added "Resources" on page 7.
2. Updated "External Clock" on page 32.
3. Updated "Serial Peripheral Interface – SPI" on page 124.
4. Updated Code Example in "USART Initialization" on page 138.

Datasheet Revision History

Please note that the following page number and the sections are referred to this document. The referred revision in this section are referring to the datasheet revision.

Changes from Rev. 2485S- 06/07 to Rev. 2485T- 05/08	1. Updated [illegible] 2. Updated [illegible] Commercial Ordering Code [illegible] No Pb-free ordering [illegible]
Changes from Rev. 2485R- 07/07 to Rev. 2485S- 06/07	1. Updated [illegible] 2. Added [illegible] 3. Updated [illegible] 4. Updated [illegible]
Changes from Rev. 2485Q- 10/06 to Rev. 2485R- 07/07	1. Added [illegible] 2. Fixed typo in [illegible] 3. Updated [illegible] 4. Updated [illegible] 5. Removed [illegible] and updated typo in Notes section [illegible]
Changes from Rev. 2485P- 02/06 to Rev. 2485Q- 10/06	1. Updated [illegible] 2. Updated [illegible] 3. Updated code examples in [illegible] 4. Updated [illegible] 5. Updated [illegible]
Changes from Rev. 2485O- 10/04 to Rev. 2485P- 02/06	1. Added [illegible] 2. Updated [illegible] 3. Updated [illegible] 4. Updated Code Examples in [illegible]

5. Updated Note in "Bit Rate Generator Unit" on page 170.

6. Updated Table 98 on page 240.

7. Updated Note in Table 103 on page 248.

8. Updated "Errata" on page 17.

Changes from Rev. 2486N-09/04 to Rev. 2486O-10/04

1. Removed to instances of "analog ground". Replaced by "ground".

2. Updated Table 7 on page 29, Table 15 on page 38, and Table 100 on page 244.

3. Updated "Calibrated Internal RC Oscillator" on page 30 with the 1 MHz default value.

4. Table 89 on page 225 and Table 90 on page 225 moved to new section "Page Size" on page 225.

5. Updated descripton for bit 4 in "Store Program Memory Control Register – SPMCR" on page 213.

6. Updated "Ordering Information" on page 13.

Changes from Rev. 2486M-12/03 to Rev. 2486N-09/04

1. Added note to MLF package in "Pin Configurations" on page 2.

2. Updated "Internal Voltage Reference Characteristics" on page 42.

3. Updated "DC Characteristics" on page 242.

4. ADC4 and ADC5 support 10-bit accuracy. Document updated to reflect this.
Updated features in "Analog-to-Digital Converter" on page 196.
Updated "ADC Characteristics" on page 248.

5. Removed reference to "External RC Oscillator application note" from "External RC Oscillator" on page 28.

Changes from Rev. 2486L-10/03 to Rev. 2486M-12/03

1. Updated "Calibrated Internal RC Oscillator" on page 30.

Changes from Rev. 2486K-08/03 to Rev. 2486L-10/03

1. Removed "Preliminary" and TBDs from the datasheet.

2. Renamed ICP to ICP1 in the datasheet.

3. Removed instructions CALL and JMP from the datasheet.

4. Updated t_{RST} in Table 15 on page 38, V_{BG} in Table 16 on page 42, Table 100 on page 244 and Table 102 on page 246.

5. Replaced text "XTAL1 and XTAL2 should be left unconnected (NC)" after Table 9 in "Calibrated Internal RC Oscillator" on page 30. Added text regarding XTAL1/XTAL2 and CKOPT Fuse in "Timer/Counter Oscillator" on page 32.

	5. Updated Note [illegible]
	6. Updated [illegible]
	7. Updated Note [illegible]
	8. Updated [illegible]
Changes from Rev. 2486N-09/04 to Rev. 2486O-10/04	1. Removed to balance of "analog ground" replaced by "ground".
	2. Updated [illegible] and [illegible]
	3. Updated [illegible] with the 1 MHz default value.
	4. [illegible] and [illegible] moved to new section [illegible]
	5. Updated description for bit [illegible]
	6. Updated [illegible]
Changes from Rev. 2486M-12/03 to Rev. 2486N-09/04	1. Added note to MLF package in [illegible]
	2. Updated [illegible]
	3. Updated [illegible]
	4. ADC4 and ADC5 support 10-bit resolution. Document updated to reflect this. Updated features in [illegible] Updated [illegible]
	5. Removed reference to "External RC Oscillator application note" from [illegible]
Changes from Rev. 2486L-10/03 to Rev. 2486M-12/03	1. Updated [illegible]
Changes from Rev. 2486K-09/03 to Rev. 2486L-10/03	1. Removed "Bandgap" and TBDs from the datasheet.
	2. Renamed ICP to ICP1 in the datasheet.
	3. Removed instructions CALL and JMP from the datasheet.
	4. Updated I_{SB} in [illegible] V_{BG} in [illegible] and [illegible]
	5. Replaced text "XTAL1 and XTAL2 should be left unconnected (NC)" after [illegible] in [illegible] Added text regarding XTAL1/XTAL2 and CKOPT Fuse in [illegible]

6. Updated Watchdog Timer code examples in "Timed Sequences for Changing the Configuration of the Watchdog Timer" on page 45.

7. Removed bit 4, ADHSM, from "Special Function IO Register – SFIOR" on page 58.

8. Added note 2 to Figure 103 on page 215.

9. Updated item 4 in the "Serial Programming Algorithm" on page 238.

10. Added t_{WD_FUSE} to Table 97 on page 239 and updated Read Calibration Byte, Byte 3, in Table 98 on page 240.

11. Updated Absolute Maximum Ratings* and DC Characteristics in "Electrical Characteristics" on page 242.

Changes from Rev. 2486J-02/03 to Rev. 2486K-08/03

1. Updated V_{BOT} values in Table 15 on page 38.

2. Updated "ADC Characteristics" on page 248.

3. Updated "ATmega8 Typical Characteristics" on page 249.

4. Updated "Errata" on page 17.

Changes from Rev. 2486I-12/02 to Rev. 2486J-02/03

1. Improved the description of "Asynchronous Timer Clock – clkASY" on page 26.

2. Removed reference to the "Multipurpose Oscillator" application note and the "32 kHz Crystal Oscillator" application note, which do not exist.

3. Corrected OCn waveforms in Figure 38 on page 90.

4. Various minor Timer 1 corrections.

5. Various minor TWI corrections.

6. Added note under "Filling the Temporary Buffer (Page Loading)" on page 216 about writing to the EEPROM during an SPM Page load.

7. Removed ADHSM completely.

8. Added section "EEPROM Write during Power-down Sleep Mode" on page 23.

9. Removed XTAL1 and XTAL2 description on page 5 because they were already described as part of "Port B (PB7..PB0) XTAL1/XTAL2/TOSC1/TOSC2" on page 5.

10. Improved the table under "SPI Timing Characteristics" on page 246 and removed the table under "SPI Serial Programming Characteristics" on page 241.

11. Corrected PC6 in "Alternate Functions of Port C" on page 61.

12. Corrected PB6 and PB7 in "Alternate Functions of Port B" on page 58.

13. Corrected 230.4 Mbps to 230.4 kbps under "Examples of Baud Rate Setting" on page 159.

6. Updated Watchdog Timer code examples in [illegible]

7. Removed bit 4, ADHSM, from [illegible]

8. Added note 2 to [illegible]

9. Updated item 4 in the [illegible]

10. Added [illegible] to [illegible] and updated Read Calibration Byte, Byte 3, in [illegible]

11. Updated Absolute Maximum Ratings* and DC Characteristics in [illegible]

Changes from Rev. 2486L-02/03 to Rev. 2486K-08/03

1. Updated V_{BOT} values in [illegible]

2. Updated [illegible]

3. Updated [illegible]

4. Updated [illegible]

Changes from Rev. 2486I-12/02 to Rev. 2486L-02/03

1. Improved the description of [illegible]

2. Removed reference to the "Multipurpose Oscillator" application note and the "32 kHz Crystal Oscillator" application note, which do not exist.

3. Corrected OCn waveforms in [illegible]

4. Various minor Timer/Counter corrections.

5. Various minor TWI corrections.

6. Added note under [illegible] about writing to the EEPROM during an SPM Page load.

7. Removed ADHSM completely.

8. Added section [illegible]

9. Removed XTAL1 and XTAL2 description on [illegible] because they were already described as part of [illegible]

10. Improved the table under [illegible] and removed the table under [illegible]

11. Corrected PC6 in [illegible]

12. Corrected PB6 and PB7 in [illegible]

13. Corrected 250.4 kbps to 230.4 kbps under [illegible]

14. Added information about PWM symmetry for Timer 2 in "Phase Correct PWM Mode" on page 113.

15. Added thick lines around accessible registers in Figure 76 on page 169.

16. Changed "will be ignored" to "must be written to zero" for unused Z-pointer bits under "Performing a Page Write" on page 216.

17. Added note for RSTDISBL Fuse in Table 87 on page 223.

18. Updated drawings in "Packaging Information" on page 14.

Changes from Rev. 2486H-09/02 to Rev. 2486I-12/02

1. Added errata for Rev D, E, and F on page 17.

Changes from Rev. 2486G-09/02 to Rev. 2486H-09/02

1. Changed the Endurance on the Flash to 10,000 Write/Erase Cycles.

Changes from Rev. 2486F-07/02 to Rev. 2486G-09/02

1. Updated Table 103, "ADC Characteristics," on page 248.

Changes from Rev. 2486E-06/02 to Rev. 2486F-07/02

1. Changes in "Digital Input Enable and Sleep Modes" on page 55.
2. Addition of OCS2 in "MOSI/OC2 – Port B, Bit 3" on page 59.
3. The following tables have been updated:
   Table 51, "CPOL and CPHA Functionality," on page 132, Table 59, "UCPOL Bit Settings," on page 158, Table 72, "Analog Comparator Multiplexed Input(1)," on page 195, Table 73, "ADC Conversion Time," on page 200, Table 75, "Input Channel Selections," on page 206, and Table 84, "Explanation of Different Variables used in Figure 103 and the Mapping to the Z-pointer," on page 221.
4. Changes in "Reading the Calibration Byte" on page 234.
5. Corrected Errors in Cross References.

Changes from Rev. 2486D-03/02 to Rev. 2486E-06/02

1. Updated Some Preliminary Test Limits and Characterization Data
   The following tables have been updated:
   Table 15, "Reset Characteristics," on page 38, Table 16, "Internal Voltage Reference Characteristics," on page 42, DC Characteristics on page 242, Table , "ADC Characteristics," on page 248.
2. Changes in External Clock Frequency
   Added the description at the end of "External Clock" on page 32.
   Added period changing data in Table 99, "External Clock Drive," on page 244.
3. Updated TWI Chapter

14. Added information about PWM symmetry for Timer 2 in [illegible]

15. Added thick lines around accessible registers in [illegible]

16. Changed "will be ignored" to "must be written to zero" for unused 2-pointer bits under [illegible]

17. Added note for RSTISBR. Rise in [illegible]

18. Updated drawings in [illegible]

Changes from Rev. 2486H-09/02 to Rev. 2486I-12/02

1. Added errata for Rev. G, H, and I on [illegible]

Changes from Rev. 2486G-09/02 to Rev. 2486H-03/02

1. Changed the Endurance on the Flash to 10,000 Write/Erase Cycles.

Changes from Rev. 2486F-07/02 to Rev. 2486G-09/02

1. Updated [illegible]

Changes from Rev. 2486E-06/02 to Rev. 2486F-07/02

1. Changes in [illegible]
2. Addition of OCSz in [illegible]
3. The following tables have been updated:

   [illegible]

4. Changes in [illegible]
5. Corrected Errors in Cross References.

Changes from Rev. 2486D-03/02 to Rev. 2486E-06/02

1. Updated Some Preliminary Test Limits and Characterization Data

   The following tables have been updated:

   [illegible] DC Characteristics on [illegible]

2. Changes in External Clock Frequency

   Added the description at the end of [illegible]

   Added packet changing data in [illegible]

3. Updated TWI Chapter

More details regarding use of the TWI bit rate prescaler and a Table 65, "TWI Bit Rate Prescaler," on page 173.

Changes from Rev. 2486C-03/02 to Rev. 2486D-03/02

1. **Updated Typical Start-up Times.**

   The following tables has been updated:

   Table 5, "Start-up Times for the Crystal Oscillator Clock Selection," on page 28, Table 6, "Start-up Times for the Low-frequency Crystal Oscillator Clock Selection," on page 28, Table 8, "Start-up Times for the External RC Oscillator Clock Selection," on page 29, and Table 12, "Start-up Times for the External Clock Selection," on page 32.

2. **Added "ATmega8 Typical Characteristics" on page 249.**

Changes from Rev. 2486B-12/01 to Rev. 2486C-03/02

1. **Updated TWI Chapter.**

   More details regarding use of the TWI Power-down operation and using the TWI as Master with low TWBRR values are added into the datasheet.

   Added the note at the end of the "Bit Rate Generator Unit" on page 170.

   Added the description at the end of "Address Match Unit" on page 170.

2. **Updated Description of OSCCAL Calibration Byte.**

   In the datasheet, it was not explained how to take advantage of the calibration bytes for 2, 4, and 8 MHz Oscillator selections. This is now added in the following sections:

   Improved description of "Oscillator Calibration Register – OSCCAL" on page 31 and "Calibration Byte" on page 225.

3. **Added Some Preliminary Test Limits and Characterization Data.**

   Removed some of the TBD's in the following tables and pages:

   Table 3 on page 26, Table 15 on page 38, Table 16 on page 42, Table 17 on page 44, "TA = -40×C to 85×C, VCC = 2.7V to 5.5V (unless otherwise noted)" on page 242, Table 99 on page 244, and Table 102 on page 246.

4. **Updated Programming Figures.**

   Figure 104 on page 226 and Figure 112 on page 237 are updated to also reflect that AV_{CC} must be connected during Programming mode.

5. **Added a Description on how to Enter Parallel Programming Mode if RESET Pin is Disabled or if External Oscillators are Selected.**

   Added a note in section "Enter Programming Mode" on page 228.

More details regarding use of the TWI on rate prescaler are a [illegible]

Changes from Rev. 2486C-03/02 to Rev. 2486D-03/02

1. Updated Typical Start-up Times.
The following tables have been updated:
[illegible]

2. Added [illegible]

Changes from Rev. 2486B-12/01 to Rev. 2486C-03/02

1. Updated TWI Chapter.
More details regarding use of the TWI Power-down operation and using the TWI in Master with low TWBR values are added in the datasheet.
Added the note at the end of the [illegible]
Added the description at the end of [illegible]

2. Updated Description of OSCCAL Calibration Byte.
In the datasheet, it was not mentioned how to take advantage of the calibration [illegible] and a Mult Oscillator selection. This is now added in the following sections:
Improved description of [illegible]

3. Added Some Preliminary Test Limits and Characterization Data.
Removed some of the TBD's in the following tables are updated:
[illegible]

4. Updated Programming Figures.
[illegible] and [illegible] are updated to also reflect that AVCC must be connected during Programming mode.

5. Added a Description on how to Enter Parallel Programming Mode if the RET Pin is Disabled or if External Oscillators are Selected.
Added a note in section [illegible]

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
avr@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

2486TS–AVR–05/08

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: +1(408) 441-0311
Fax: +1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721 9778
Fax: (852) 2722-1369

Atmel Europe
Le Ribecs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60 70-00
Fax: (33) 1-30-60 71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
avr@atmel.com

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