INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

APLIKASI MIKROKONTROLER ATmega8 SEBAGAI AGENDA ELEKTRONIK YANG DITEMPATKAN PADA RUANG KERJA DENGAN TAMPILAN DOT MATRIK

SKRIPSI

MILIK
PERPUSTAKAAN
ITN MALANG

Disusun Oleh :

NAMA : YOKE RAHATNA KUSUMA
NIM : 01.17.158

OKTOBER 2005

LEMBAR PERSETUJUAN

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Disusun dan Diajukan untuk Melengkapi dan Memenuhi Syarat Mencapai Gelar Sarjana Teknik

Disusun Oleh :

NAMA : YOKE RAHATNA KUSUMA

NIM : 01.17.158

Mengetahui,	**Diperiksa dan Disetujui,**
Ketua Jurusan T. Elektro S-1	**Dosen Pembimbing**
(Ir. F. Yudi Limpraptono, MT)	**(Joseph Dedy Irawan, ST, MT)**
NIP.P. 1039500274	**NIP. 1039800324**

KONSENTRASI TEKNIK ELEKTRONIKA

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KONSENTRASI TEKNIK ELEKTRONIKA

BERITA ACARA UJIAN SKRIPSI

FAKULTAS TEKNOLOGI INDUSTRI

Nama : Yoke Rahatna Kusuma

NIM : 01.17.158

Jurusan : Teknik Elektro S-1

Konsentrasi : Teknik Elektronika

Judul Skripsi : Aplikasi Mikrokontroler ATmega8 Sebagai Agenda Elektrtonik Yang Ditempatkan Pada Ruang Kerja Dengan Tampilan Dot Matrik

Dipertahankan di hadapan majelis penguji Skripsi jenjang Strata satu (S-1) pada :

Hari : Jum'at

Tanggal : 7 Oktober 2005

Dengan Nilai : 80,9 (A)

Ketua Majelis Penguji

(Ir. Mochtar Asroni, MSME)
NIP.Y.1018100036

Sekretaris Majelis Penguji

(Ir. F. Yudi Limpraptono, MT)
NIP.Y.1039500274

Penguji I

(Ir. Usman Djuanda, MM)
NIP.P. 1018700143

Penguji II

(M. Ashar, ST, MT)

LEMBAR PERSEMBAHAN

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ALLAH SWT, yang telah memberikan Rahmat, Hidayah dan Karunia-Nya

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Terkadang aku lupa akan semua itu karena kenikmatan sesaat. Sungkem jiwa dan ragaku padamu wahai surga yang hidup.....mulialah kalian selalu "Ayah dan Ibu" sekarang, esok dan selamanya

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-Yoke-

ABSTRAK

Yoke Rahatna Kusuma, 2005, **Aplikasi Mikrokontroler ATmega8 Sebagai Agenda Elektronik Yang Ditempatkan Pada Ruang Kerja Dengan Tampilan Dot Matrik,** Teknik Elektro S-1/ Teknik Elektronika, Fakultas Teknologi Industri, Institut Teknologi Nasional Malang.
Dosen Pembimbing : Joseph Dedy Irawan, ST, MT.

Kata Kunci : Agenda elektronik, Mikrokontroler ATmega8

Kebutuhan fasilitas dan pelayanan informasi yang dapat membantu aktifitas manusia merupkan suatu lahan industri yang ikut berperan dalam era kemajuan teknologi infomasi saat ini. Agenda sebagai bagian dari bentuk informasi menjadi landasan dari penyusunan skripsi ini sampai pada pembuatan alat. Agenda merupakan catatan yang bertanggal dan biasa digunakan sebagai alat bantu untuk mengingat atau mencatat rencana aktifitas yang akan dilakukan atau sebagai catatan aktifitas yang sudah terlewati oleh waktu. Setiap individu dengan aktifitas akan berusaha melakukan hal tersebut dengan berbagai macam caranya masing-masing, misalnya ada yang menggunakan media tulis sebagai buku agenda, alat pengingat (*reminder* pada HP) atau PDA (*Personal Digital Assistance*). Dalam skripsi ini akan dibuat suatu agenda elektronik yang dapat digunakan oleh beberapa orang dan manfaat agenda yang lebih umum, yaitu berfungsi sebagai papan informasi. Alat ini nantinya untuk ditempatkan pada ruang kerja.

Agenda elektronik tersebut berisi tentang informasi yang ditampilkan dalam sebuah modul display dot matrik disertai penampil waktu (jam, menit, detik, tahun, bulan, tanggal) oleh modul *LCD* serta *buzzer* dan *ISD voice* sebagai penanda bunyi untuk agenda apabila sesuai dengan waktunya. Perangkat *keyboard* digunakan sebagai masukan baik itu data untuk agenda maupun tombol-tombol perintah. Agenda elektronik ini dapat menyimpan sejumlah 7 agenda dan sebanyak 200 karakter dapat diisikan pada setiap agenda.

Dengan digunakannya dot matrik sebagai modul penampil agenda, maka fungsi agenda akan dapat juga sebagai papan informasi yang pemanfaatannya bisa lebih luas dari pada agenda sebagai *personal assistance*. Dari gambaran diatas menjelaskan fungsi kerja alat yang kegunaan utama sebagai agenda elektronik dan dapat digunakan pula sebagai papan informasi yang penempatannya pada ruang kerja.

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Assalamu'alaikum Wr.Wb.

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Skripsi ini disusun untuk memenuhi persyaratan kelulusan dalam menyelesaikan pendidikan dan memperoleh gelar Sarjana Teknik pada Fakultas Teknik Industri Jurusan Elektro S-1 konsentrasi Teknik Elektronika Institut Teknologi Nasional Malang. Penyusun menyadari sepenuhnya bahwa dalam menyelesaikan skripsi ini banyak memperoleh bantuan dari berbagai pihak. Dalam kesempatan ini penyusun ucapkan terimakasih yang tulus kepada :

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BAB I

PENDAHULUAN

1.1 Latar Belakang

Agenda merupakan catatan yang bertanggal dan biasa digunakan sebagai alat bantu untuk mengingat atau mencatat rencana aktifitas yang akan dilakukan atau sebagai catatan aktifitas yang sudah terlewati oleh waktu. Setiap individu dengan aktifitas akan berusaha melakukan hal tersebut dengan berbagai macam caranya masing-masing, misalnya ada yang menggunakan media tulis sebagai buku agenda, alat pengingat (*reminder* pada HP) atau PDA (*Personal Digital Assistance*).

Dalam contoh diatas secara umum agenda digunakan sebagai alat bantu catatan pengingat secara individu yang biasanya selalu menyertai dimanapun pemiliknya berada. Dalam skripsi ini dibuat suatu agenda elektronik yang dapat digunakan oleh beberapa orang misalnya untuk kepentingan karyawan, yang ditempatkan pada ruang kerja. Dengan adanya aktifitas dan rutinitas karyawan yang teragenda akan sangat membantu dalam administrasi waktu kegiatan para karyawan dalam menjalankan aktivitasnya. Agenda elektronik akan mencatat semua kepentingan, misalnya jadual kerja, waktu istirahat dan makan siang, jadual rapat kerja, serta untuk mencatat kepentingan personal pengguna agenda. Agenda elektronik dilengkapi dengan fitur penanda untuk menandai suatu agenda telah dilaksanakan atau belum.

1.2 Permasalahan

Mengacu pada permasalahan yang diuraikan pada latar belakang, maka rumusan masalah dapat ditekankan pada:

- Bagaimana merancang sistem agenda elektronik dengan sistem pewaktu *Real Time Clock* (RTC).
- Bagaimana merancang sistem tersebut yang mampu menyimpan agenda dan mengatur sesuai urutan waktu untuk mengaktifkan memo yang tersimpan di dalam RAM yang digunakan sehingga ketika waktu telah sesuai dengan agenda dapat tampil dalam layar display dot matrik serta mengaktifkan rangkaian *buzzer*.
- Bagaimana merencanakan perangkat lunak (*software*) mikrokontroler untuk menjalankan sistem secara otomatis.

1.3 Ruang Lingkup

Dalam ruang lingkup pembahasan ini, permasalahan yang akan dibahas meliputi :

1. Mikrokontroler ATmega8 sebagai pengendali utama sistem.
2. Menggunakan komponen RTC sebagai pewaktu terprogram dan rangkaian ISD sebagai penanda agenda telah diaktifkan.
3. Menggunakan *keyboard* standar *IBM 102 key* sebagai perangkat untuk memasukkan data agenda ke dalam sistem.
4. Rangkaian dot matrik sebagai tampilan dan sistem *buzzer* sebagai penanda waktu untuk agenda (*reminder*).

Dalam tugas akhir ini tidak dibahas tentang sistem internal dot matrik, *RTC*, *RAM*, *keyboard* dan catu daya.

1.4 Tujuan

Tujuan yang ingin dicapai dalam penyusunan skripsi ini adalah dapat direalisasikannya agenda elektronik sehingga dapat membantu dalam mengingat aktifitas sehari-hari dalam ruangan kerja.

1.5 Metodologi

Dalam penyusunan skripsi ini diperlukan beberapa metode penelitian yang dapat disusun sebagai berikut :

1. *Studi Literatur*

Melakukan studi atas literatur mengenai beberapa komponen yang digunakan serta kajian teoritis, antara lain; mikrokontroller ATmega8515, mikrokontroler AT89S52, *LCD, ISD Voice 1420, RTC + NVRAM,* rangkaian dot matrik, *Buzzer* serta sistem *keyboard* terhadap MCU.

2. *Perencanaan Alat*

Perencanaan alat meliputi penentuan spesifikasi alat yang akan dibuat mengacu pada keberadaan komponen di pasaran, blok diagram sistem, dan cara kerja rangkaian. Dilanjutkan dengan perancangan perangkat lunak (*software*) serta *layout* rangkaian dalam PCB.

3. *Pengujian Alat*

Dimana alat ini di uji coba secara nyata pada kondisi yang mendekati sesungguhnya. Pengujian alat yang akan dilakukan terdiri atas :

- Pengujian perblok rangkaian yang direncanakan.
- Mengevaluasi hasil pengujian keseluruhan sistem.

4. *Analisis*

Dilakukan dengan membandingkan antara perencanaan peralatan dengan hasil pengujian sehingga bisa ditentukan spesifikasi baru dari alat yang dibuat serta untuk diambil kesimpulan.

1.6 Sistematika Penulisan

Sistematika pembahasan dalam laporan tugas akhir ini dibagi menjadi lima bab yaitu sebagai berikut :

BAB I : PENDAHULUAN

Menguraikan tentang latar belakang masalah, ruang lingkup masalah, rumusan masalah , batasan masalah, tujuan penulisan, dan sistematika pembahasan.

BAB II : LANDASAN TEORI

Menguraikan tentang teori dasar yang menunjang perencanaan alat.

BAB III : PERANCANGAN DAN PEMBUATAN ALAT

Menjelaskan tentang diagram blok rangkaian, prinsip kerja rangkaian sistem alat tersebut dan realsiasi alat.

BAB IV : PENGUJIAN ALAT

Menjelaskan tentang pengujian alat secara perblok .

BAB V : PENUTUP

Menjelaskan tentang kesimpulan dan saran.

LAMPIRAN : Berisi tentang gambar rangkaian, daftar komponen dan data IC yang digunakan.

BAB II

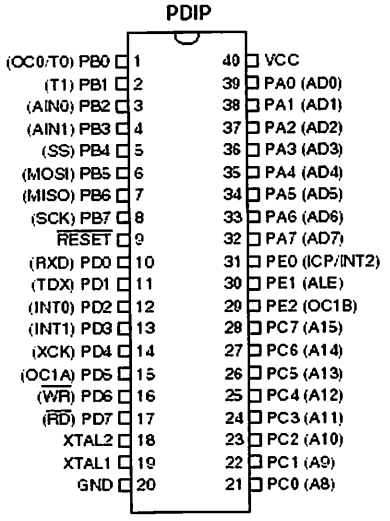
LANDASAN TEORI

Pada bagian bab ini akan dibahas teori penunjang sesuai dengan batasan masalah diatas yang terdiri dari 2 sistem, yaitu sistem utama yang terdiri dari : Mikrokontoler ATmega8515, *ISD Voice 1420*, LCD, *Keyboard.* Sedangkan untuk sistem display terdiri dari : Mikrokontroler AT89S52, *RTC* + *NVRAM*, Dot Matrik, *driver* LED, register geser, *buzzer*.

2.1. Mikrokontroler ATmega8515

2.1.1. Arsitektur

ATmega8515 adalah mikrokontroler 8-bit CMOS, *low-power* yang berdasarkan pada bentuk arsitektur AVR RISC (*Reduced Instruction Set Computer*), yang hampir semua instruksinya selesai dikerjakan dalam satu siklus clock. AVR ATmega8515 menggunakan instruksi tunggal (*Single Clock Cycle*), yaitu sistem mikrokontroler yang frekuensi kerja dalam *chip* sama dengan frekuensi kristal untuk osilator tanpa memerlukan rangkaian pembagi frekuensi setelah osilator yang diperlukan untuk memperoleh perbedaan fase dari *clock*, sehingga AVR 12 kali lebih cepat dibanding mikrokontroler generasi MCS51.



Gambar 2.1 Konfigurasi Pin ATmega8515

Sumber: *Data Sheet* ATmega8515

Berbagai karakteristik yang tersedia dalam IC ATmega8515 adalah sebagai berikut:

- 8K bytes *In-System Programable Flash*
- 512 bytes EEPROM (*Electrical Erasable Programable Read Only Memory*)
- 512 bytes SRAM (*Static Random Access Memory*)
- 32 jalur I/O *general-purpose*
- 32 *general-purpose working register*
- Timer/Counter yang fleksibel dengan mode pembanding
- Interupsi internal dan eksternal
- Pemrograman serial UART (*Universal Asynchronous Receiver and Transmitter)*
- Serial Port SPI (*Serial Peripheral Interface*)

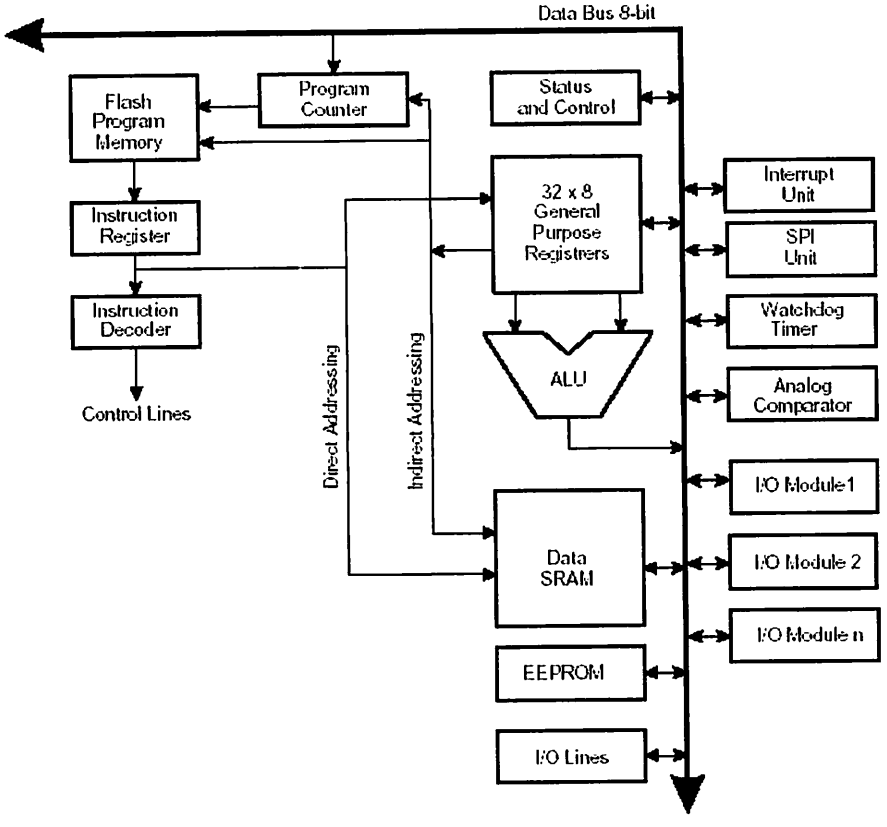
ATmega8515 mempunyai dua buah *power-save* mode yang dapat diatur melalui *software*, yaitu:

- Idle Mode

  Menghentikan CPU sementara SRAM, *Timer/ Counter*, port SPI, dan sistem tetap berfungsi.

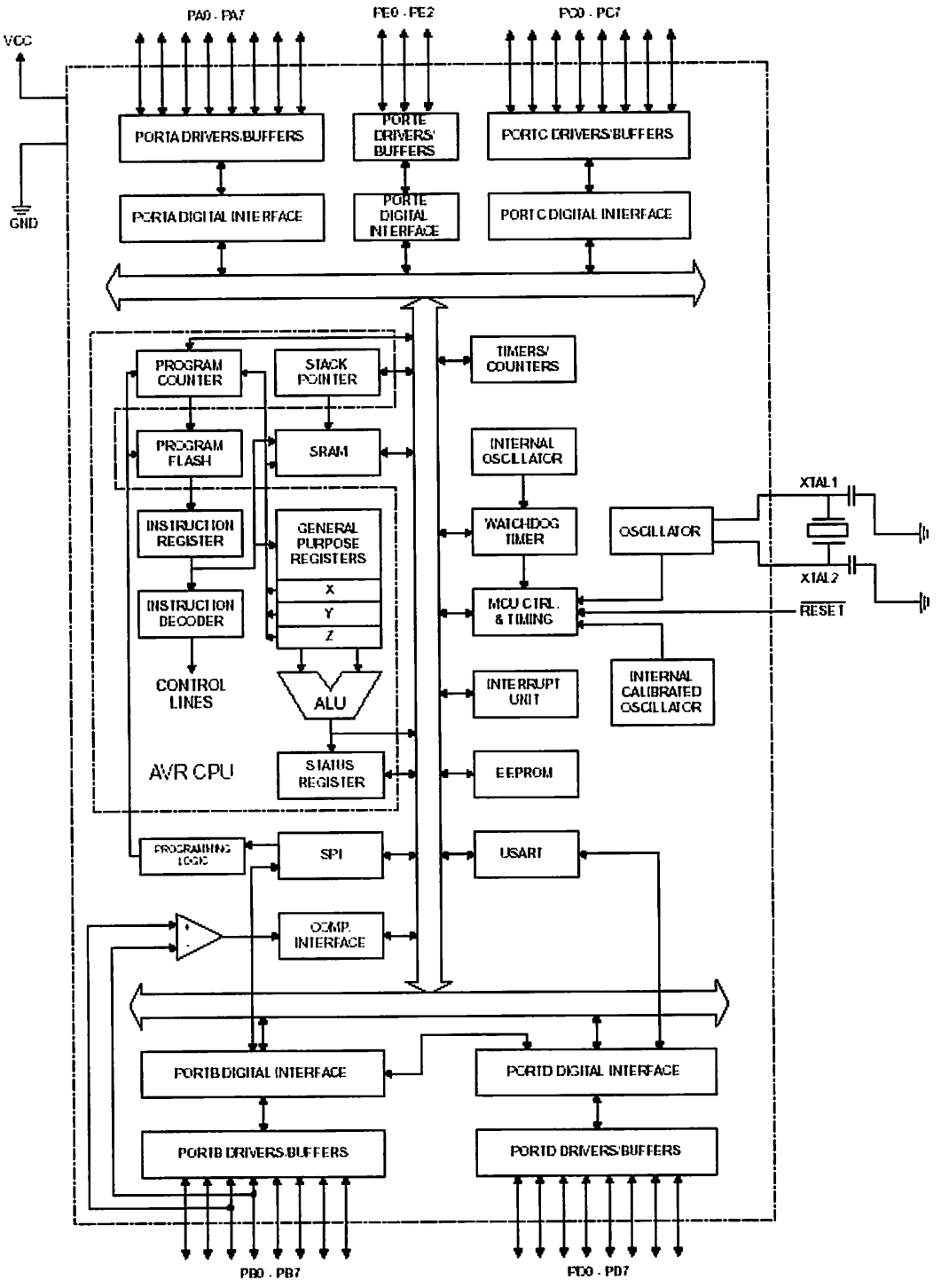
- Power-Down Mode

  Menyimpan isi register dan menahan osilator untuk tidak mengaktifkan fungsi-fungsi chip yang lain sampai terjadi reset atau interupsi dari luar.



Gambar 2.2 Arsitektur AVR ATmega8515

Sumber: *Data Sheet* ATmega8515



Gambar 2.3 Blok Diagram AVR ATmega8515

Sumber: *Data Sheet* ATmega8515

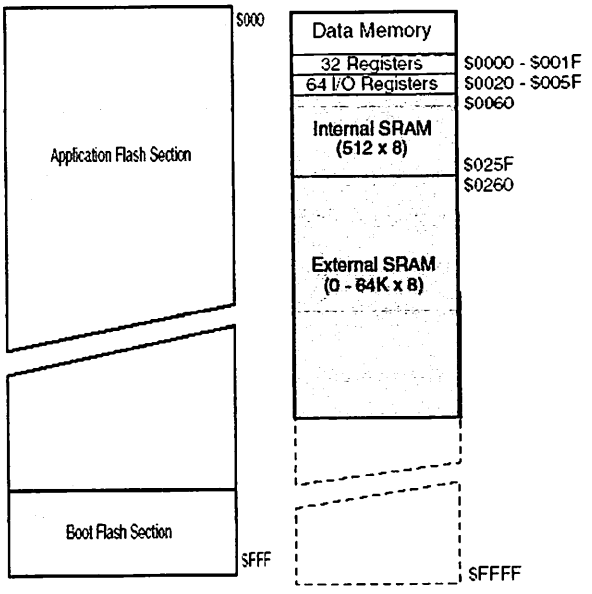
Deskripsi Pin:

- Vcc: Tegangan *Supply*
- Gnd: *Ground*
- Port A (PA0-PA7): Port dua arah I/O 8-bit, kaki portnya dapat menyediakan resistor *pull-up* internal (dipilih untuk masing-masing bit). Port A juga dapat mengendalikan tampilan LED secara langsung.
- Port B (PB0-PB7: Port dua arah I/O 8-bit dengan resistor *pull-up* internal, digunakan pada fungsi-fungsi khusus dari karakteristik ATmega8515.
- Port C (PC0-PC7): Port dua arah I/O 8-bit dengan resistor *pull-up* internal, digunakan sebagai alamat keluaran saat SRAM eksternal digunakan.
- Port D (PD0-PD7): Port dua arah /O 8-bit dengan resistor *pull-up* internal, digunakan untuk berbagai karakteristik khusus dari ATmega8515.
- RESET: Input reset, jika kaki pinnya mendapat input 0 (*low*) dalam jangka waktu lebih dari 50 ns maka akan menghasilkan kondisi reset, hal ini terjadi jika *clock* tidak berfungsi.
- XTAL1: Input untuk inverting oscillator amplifier.
- XTAL2: Output dari inverting oscillator amplifier.
- ICP: pin input untuk *Timer/Counter*1, berfungsi sebagai penangkap masukan (*input capture*).
- OC1B: Pin output untuk *Timer/Counter*1, berfungsi sebagai *output compare*B.
- ALE: *Address Latch Enable*, berfungsi sebagai pengunci alamat ketika memori eksternal digunakan. ALE berfungsi untuk mengunci logic 0 (*low*)

pada alamat yang diminta ke dalam pengunci alamat selama siklus akses pertama dan kaki AD0-AD7 digunakan pada siklus yang kedua.

AVR dibangun atas dasar arsitektur Harvard, dimana program dan data ditempatkan pada memori yang berlainan dengan cara menyediakan saluran data untuk memori-program yang terpisah dari saluran data untuk memori-data.

2.1.2. Memori Program (Flash ROM)



Gambar 2.4 Memory Maps

Sumber: *Data Sheet* Atmega8515

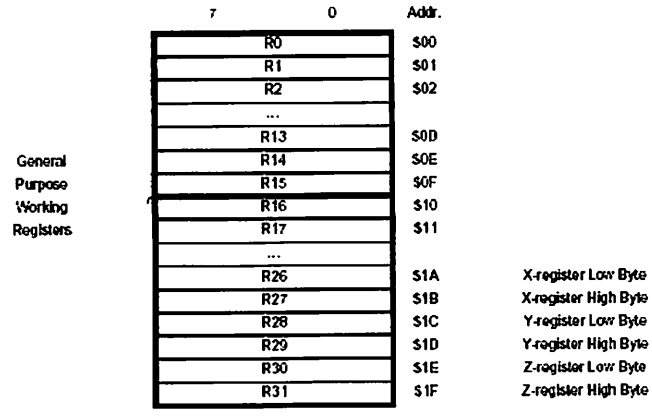
Memori program AVR ATmega8515 disusun sebagai sistem memori-program 4K x 16 bit, yang dinomori mulai dari $0000 sampai $0FFF seperti terlihat pada gambar 2.10. memori program pada ATmega8515 menggunakan

Programable Flash Program memory, tidak ada fasilitas untuk menambah memori program di luar *chip* ATmega8515.

Memori program tersebut dapat diisi ulang lewat saluran SPI (*Serial Peripheral Interface*) yang hanya memerlukan 3 jalur sinyal ditambah sebuah *ground*. Pengisian *flash* memori tersebut cukup menggunakan tegangan +5 volt, sehingga rangkaian pengisi memori-program sangat sederhana bahkan bisa dibuat dengan sistem ISP (*In-System Programing*), yaitu pengisian memori program langsung pada rangkaian peralatan tanpa menggunakan alat khusus untuk mengisi memori-program.

2.1.3. Memori Data

2.1.3.1. Register Serba Guna (*General Purpose Working Register*)



Gambar 2.5 Register Serba Guna

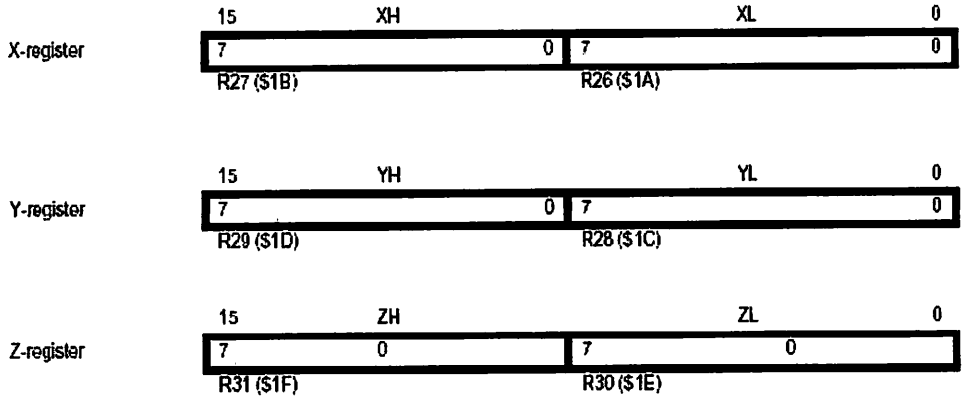
Sumber: *Data Sheet* ATmega8515

AVR ATmega8515 mempunyai 32 register serbaguna yang masing-masing berkapasitas 8 bit, menempati memori-data dengan nomor $0000 sampai $001F yang disebut sebagai R0 sampai R31. Semua register serba guna memiliki

kemampuan yang hampir simitris, semuanya bisa berfungsi sebagai akumulator sehingga bisa melakukan proses menunjang kerja ALU dengan sangat baik dan menghasilkan kecepatan kerja yang sangat tinggi.

Register-register tersebut dipecah menjadi 2 bagian, bagian pertama R0...R15, dan bagian kedua R16...R31. Instruksi-instruksi yang bekerja dengan bilangan konstanta (*immediate data*), misalnya instruksi SBCI, SUBI, CPI, ANDI, ORI dan LDI hanya bisa dipakai pada register bagian kedua R16...R31.

Register serba guna R0 dan R16...R31 memiliki kemampuan tambahan. R0 dipakai sebagai register penampung data dalam instruksi LPM (*Load Program Memory*). R26 dan R27, R28 dan R29 serta R30 dan R31 bisa dipasangkan untuk membentuk register 16 bit, pasangan-pasangan register ini dinamakan sebagai Register X, Register Y dan Register Z seperti pada gambar di bawah ini:



Gambar 2.6 Register X, Y dan Z

Sumber: *Data Sheet* ATmega8515

Pasangan register tersebut untuk mengamati memori data (16 bit *memory address register*), dipakai dalam instruksi-instruksi yang bekerja pada memori-data. Khusus register , selain dipakai untuk operasi memori-data bisa pula dipakai

untuk mengambil data konstanta yang disimpan dalam memori-program. Instruksi untuk keperluan ini adalah instruksi LPM.

2.1.3.2. Register I/O

AVR ATmega8515 mempunyai 64 register I/O yang masing-masing berkapasitas 8 bit, menempati memori-data dengan nomor $0020 sampai $005F. Selain bisa dikenali dengan nomor memori-data tersebut ke-64 register ini bisa dikenali pula dengan nomor register I/O dari nomor $00 sampai $3F. Dalam praktek register I/O ini lebih dikenal sebagai I/O dengan instruksi IN atau OUT dari pada sebagai memori data biasa. Register untuk timer 8 bit ditempatkan di memori data nomor $0052 dan $0053, dan untuk *watchdog timer* ditempatkan di $0041.

Selain untuk tempat register I/O, sebagian memor-data nomor $0020 sampai $005F dipakai untuk menyimpan informasi prosesor dan pengaturan kerja prosesor. Misalnya memori-data nomor $005F dipakai sebagai *Status Register* (SREG) yang bertugas untuk menampung petanda (*Flags*) dari hasil kerja ALU. SREG didefinisikan sebagai :

Bit	7	6	5	4	3	2	1	0	
	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Gambar 2.7 Status Register

Sumber: *Data Sheet* ATmega8515

- Bit7-I: *Global Interupt Enable*

  Bit ini hatus di set pada logic 0, maka seluruh interupsi tidak akan berfungsi walaupun masing-masing interupsi telah di set. Bit-I dikosongkan (*clear*) oleh *hardware* setelah terjadi interupsi dan di set oleh interupsi RETI untuk mengaktifkan interupsi berikutnya.

- Bit6-T: *Bit Copy Storage*

  Instruksi meng-copy bit BLD (Bit Load) dan BST (Bit Storage) menggunakan bit-T sebagai sumber dan tujuan pada operasi bit. Untuk meng-*copy* bit dari register dalam file register ke T digunakan instruksi BST dan bit yang ada di T dapat di-*copy* ke dalam bit yang ada di register dalam file register menggunakan instruksi BLD.

- Bit5-H: *Half Carry Flag*

  Bit-H mengindikasikan *half-carry* pada beberapa operasi aritmatika.

- Bit4-S: *Sign Bit*, $S=N \oplus V$

  Bit-S selalu terpisah atau antara *flag negative* N dan dua komplemen *overflow flag* V.

- Bit3-V: *Two's Complement Overflow flag*

  Bit-V ini mendukung dua komplemen aritmatika.

- Bit2-N: *Negative Flag*

  Bit-N mengindikasikan hasil negatif setelah operasi aritmatika dan logika yang berbeda.

- Bit1-Z: *Zero Flag*

Mengindikasikan hasil nol setelah operasi aritmatika dan logika yang berbeda.

- Bit0-C: *Carry Flag*

  Bit-C mengindikasikan carry pada operasi aritmatika atau logika.

Memori data $005D ($3D) dan $005E ($3E) dipakai *Stack Pointer* (SP) register yang bertugas untuk mencatat nomor memori data yang dipakai sebagai stack.

Bit	15	14	13	12	11	10	9	8	
	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SPH
	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SPL
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

Gambar 2.8 Stack Pointer

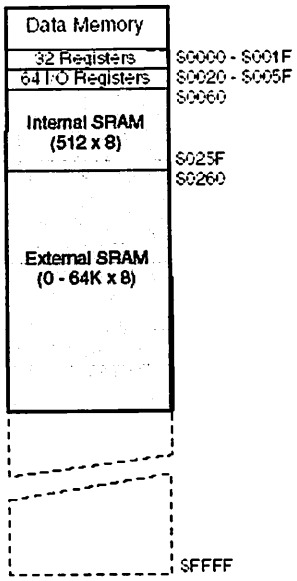
Sumber: *Data Sheet* ATmega8515

SP dikurangi 1 ketika data dimasukkan ke stack dengan instruksi PUSH dan dikurangi 2 ketika alamat dimasukkan ke stack dengan *subroutine call* dan interupsi. SP akan ditambah 1 ketika data dikeluarkan dari stack dengan instruksi POP dan ditambah 2 ketika alamat dikeluarkan dari stack dengan return dari subroutine RET atau return dari interupsi RETI.

2.1.3.3. SRAM Internal dan Eksternal

Seluruh data untuk memori data terdiri dari 8 jalur, menghubungkan register serbaguna, register I/O dan memori data internal maupun eksternal menjadi satu yang membentuk sistem memori 8 bit. Sistem memori-data ini

dibentuk dengan SRAM (*Static Random Access Memory*), seperti terlihat pada gambar 2.9



Gambar 2.9 Map Memori Data

Sumber: *Data Sheet* ATmega8515

AVR ATmega8515 memiliki 512 x 8 bit internal SRAM yang bebas dipakai untuk berbagai macam keperluan. Internal SRAM ini selain dipakai untuk menyimpan data sementara, juga dipakai stack untuk menyimpan nilai terakhir *program counter* (PC) sebelum AVR menjalankan subrutin atau melayani permintaan interupsi.

ATmega8515 memiliki kemampuan untuk menambah memori data di luar chip (eksternal SRAM). Kapasitas SRAM eksternal yang dipasang maksimal sebesar 64K byte, dengan pengertian nomor-nomor SRAM yang sudah dipakai di dalam chip (internal SRAM) tidak lagi dikenali sebagai SRAM eksternal. Pada gambar 2.15 SRAM internal ditempatkan sampai pada nomor $025F, dalam hal ini SRAM eksternal akan dikenali mulai dari nimor $0260 sampai $FFFF.

2.1.4. Reset dan Interupsi

ATmega8515 menyediakan 12 sumber interupsi yang berbeda. Interupsi-interupsi tersebut dan *vektor* pemisah *reset* masing-masing memiliki *vektor* pemisah program dalam memori program. Semua interupsi yang ditentukan oleh bit pengaktif individual harus di set pada *logic* 1 (high) bersama bit-1 pada status register untuk mengaktifkan perintah interupsi.

Alamat terendah dalam ruang memori-program secara otomatis didefinisikan sebagai *Reset* dan *Vektor* Interupsi. Daftar reset dan *vektor* interupsi secara lengkap ditunjukkan pada table di bawah ini:

Tabel 2.1 Reset dan Vektor Interupsi

Vector No.	Program Address(2)	Source	Interrupt Definition
1	$000(1)	RESET	External Pin, Power-on Reset, Brown-out Reset and Watchdog Reset
2	$001	INT0	External Interrupt Request 0
3	$002	INT1	External Interrupt Request 1
4	$003	TIMER1 CAPT	Timer/Counter1 Capture Event
5	$004	TIMER1 COMPA	Timer/Counter1 Compare Match A
6	$005	TIMER1 COMPB	Timer/Counter1 Compare Match B
7	$006	TIMER1 OVF	Timer/Counter1 Overflow
8	$007	TIMER0 OVF	Timer/Counter0 Overflow
9	$008	SPI, STC	Serial Transfer Complete
10	$009	USART, RXC	USART, Rx Complete
11	$00A	USART, UDRE	USART Data Register Empty
12	$00B	USART, TXC	USART, Tx Complete
13	$00C	ANA_COMP	Analog Comparator
14	$00D	INT2	External Interrupt Request 2
15	$00E	TIMER0 COMP	Timer/Counter0 Compare Match
16	$00F	EE_RDY	EEPROM Ready
17	$010	SPM_RDY	Store Program memory Ready

Sumber: *Data Sheet* ATmega8515

Tabel di atas juga membatasi tingkat prioritas dari interupsi yang berbeda. Alamat terendah merupakan prioritas tertinggi, *reset* merupakan prioritas tertinggi dan selanjutnya adalah INT0 (*External Interupt Request 0*).

Interupsi eksternal dipicu *(trigger)* oleh pin INT1 dan INT0. Interupsi akan aktif jika pin INT1/INT0 dikonfigurasikan sebagai *output*.

ATmega8515 memiliki 3 sumber *Reset* yaitu:

1. *Power-On Reset*

   MCU akan di *reset* secara otomatis jika tegangan catu daya lebih rendah dari tegangan ambang batas *reset* (*Power-On Reset Thresholt-*V_{POT}). Tegangan V_{POT} berkisar antara 0.4 sampai 1.0.

2. *External Reset*

   MCU akan di *reset* jika kaki *RESET* bernilai'0' dalam waktu >50 ns.

3. *Watchdog Reset*

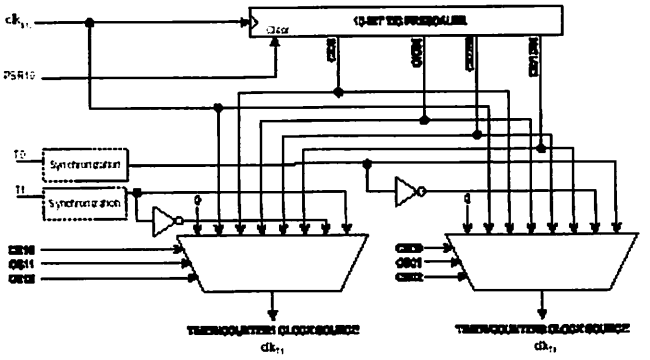
   Jika sistem *Watchdog* diaktifkan, MCU akan di *reset* jika dalam batas waktu yang ditentukan *Watchdog timer* tidak juga diaktifkan.

2.1.5. Timer/Counter 0

Timer/counter 0 (TCNT0) merupakan pencacah biner 8 bit, ditempatkan sebagai register I/O dengan nomor 32. TCNT0 bisa dipakai sebagai timer maupun sebagai counter, tergantung pada sumber sinyal yang dipakai untuk menggerakkannya. Sebagai timer sinyal penggeraknya berasal dari osilator kristal atau frekuensi yang diturunkan dari osilator kristal. Terdapat 5 frekuensi osilator kristal yang bisa dipilih yaitu CK, CK/8, CK/64, CK/256, atau CK/1024.

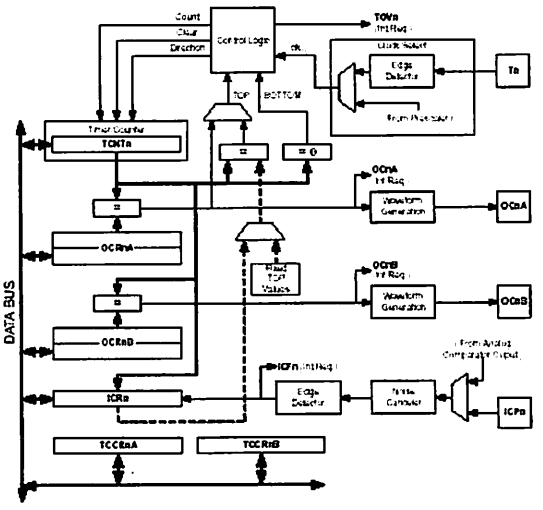
Sebagai counter sinyal yang dipakai sebgai penggerak berasal dari luar

chip yang disalurkan melalui pin T0 dari IC ATmega8515. frekuensi luar yang masuk ke pin T0 dilewatkan oleh sebuah inverter, sehingga bisa dipilih fase yang sesuai untuk menggerakkan pencacah biner. TCCR0 (*Timer/Counter 0 Control Register*) pada register I/O nomor $33 digunakan untuk menentukan apakah TCNT0 bekerja sebagai timer atau sebagai counter dan sekaligus untuk menghentikan atau menjalankan pencacahan TCNT0.



Gambar 2.10 Timer/Counter Prescaler

Sumber: *Data Sheet* ATmega8515

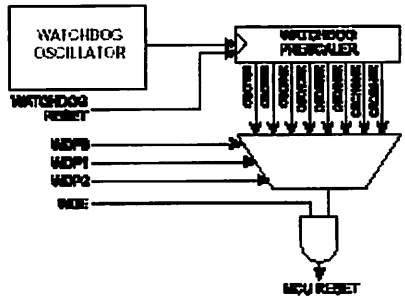


Gambar 2.11 Blok Diagram Timer/Counter

Sumber: *Data Sheet* ATmega8515

2.1.6. Watchdog Timer

Watchdog timer adalah sarana yang disediakan di dalam chip untuk mereset AVR secara otomatis jika sistem tidak dapat dikendalikan. Jika sistem watchdog diaktifkan, secara periodik AVR akan di reset oleh pencacah watchdog (*Watchdog Prescal*). Untuk memperlancar kerja sistem maka pencacah watchdog selalu di reset lewat perangkat lunak sebelum sempat mereset AVR, dengan demikian selama program pengendali AVR bekerja dengan normal dan bisa mereset pencacah watchdog maka sistem akan bekerja dengan normal, jika tidak pencacah watchdog akan mereset AVR.



Gambar 2.12 Watchdog Timer

Sumber: *Data Sheet* ATmega8515

Tabel 2.2 Watchdog Timer Prescale Select

WDP2	WDP1	WDP0	Number of WDT Oscillator Cycles	Typical Time-out at V_{CC} = 3.0V	Typical Time-out at V_{CC} = 5.0V
0	0	0	16K (16,384)	17.1 ms	16.3 ms
0	0	1	32K (32,768)	34.3 ms	32.5 ms
0	1	0	64K (65,536)	68.5 ms	65 ms
0	1	1	128K (131,072)	0.14 s	0.13 s
1	0	0	256K (262,144)	0.27 s	0.26 s
1	0	1	512K (524,288)	0.55 s	0.52 s
1	1	0	1,024K (1,048,576)	1.1 s	1.0 s
1	1	1	2,048K (2,097,152)	2.2 s	2.1 s

Sumber: *Data Sheet* ATmega8515

Seperti terlihat pada gambar 2.18, pencacah watchdog merupakan sebuah pencacah biner 11 bit yang digerakkan dengan sebuah rangkaian osilator dalam chip AVR, frekuensi osilator berubah pada tegangan catu daya AVR yang berlainan, tidak bisa diatur lebih lanjut. Tegangan catu daya 5 volt menghasilkan frekuensi 1 MHz, dan frekuensi pada tegangan 3 volt sebesar 350 KHz.

8 keluaran flip-flop pembentuk pencacah watchdog disalurkan ke rangkaian multiplex yang berfungsi sebagai pemilih periode watchdog, sehingga dengan mudah bisa diatur periode waktu pencacah watchdog mereset AVR lewat sinyal pada keluaran rangkaian multiplex. Keluaran rangkaian multiplex sebelum dipakai sebagai sinyal reset AVR dikendalikan dengan sebuah gerbang AND, untuk mengatur aktifitas *Watchdog Timer*.

2.1.7. EEPROM (*Electrical Erasable Programable Read Only Memory*)

EEPROM dalam AVR dikatakan sebagai memori-data khusus, karena saluran data, saluran alamat bahkan sinyal kontrol untuk EEPROM terpisah dari saluran data, saluran alamat dan sinyal kontrol untuk SRAM dan register I/O, meskipun sama-sama berada dalam satu chip.

EEPROM dapat ditulis ulang sampai 100.000 kali, waktu yang diperlukan untuk mengganti isi satu byte EEPROM berkisar antara 2.5 ms - 4 ms. Agar pengisian EEPROM dapat dilakukan dengan baik, sediakan sinyal yang menandai proses pengisian sudah selesai. Sesaat setelah EEPROM diisi, AVR akan berhenti bekerja selama 2 siklus clock. Hal ini juga terjadi saat setelah EEPROM dibaca isinya, AVR akan berhenti bekerja selama 4 siklus clock.

Dari segi pemrograman EEPROM merupakan perangkat register I/O yang terdiri dari 3 bagian yaitu:

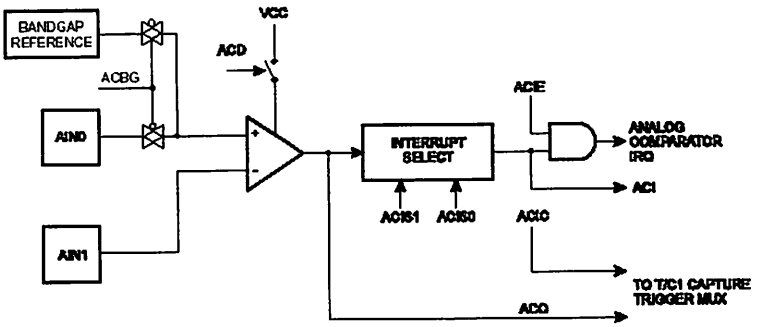
- EECR (*EEPROM Control Register*), yang ditempatkan di register I/O nomor $1C berfungsi untuk membangkitkan perintah mengisi EEPROM atau membaca isi EEPROM.
- EEDR (*EEPROM Data Register*), ditempatkan di register I/O nomor 1D, diperlakukan sebagai pengganti saluran data.
- EEAR (*EEPROM Address Register*), ditempatkan di register I/O nomor $1E, diperlakukan sebagai pengganti saluran alamat yang terdiri dari EEARH (*EEAR High Byte-Register* I/O nomor $1E) dan EEARL (*EEAR Low Byte-Register* I/O nomor $1F).

2.1.8. Pembanding Tegangan (*Analog Comparator*)

Pembanding tegangan AVR dibentuk dengan sebuah OpAmp (*Operasional Amplifier)* yang ditempatkan di dalam chip, input V+ dari OpAmp dihubungkan dengan kaki PB2 (AIN0), input V- dihubungkan dengan kaki PB3 (AIN1). Sedangkan output OpAmp tidak dihubungkan keluar chip, sehingga OpAmp tersebut hanya berfungsi sebagai pembanding tegangan , tidak bisa dipakai sebagai penguat karena tidak dipasangkan resistor antara output dan inputnya sebagai komponen *feedback.*

Tegangan AIN0 dan AIN1 selalu dibandingkan oleh OpAmp, jika tegangan pada AIN0 lebih positif dari AIN1 maka output OpAmp bernilai '1', sebaliknya jika tegangan pada AIN1 lebih positif dari AIN0 maka output OpAmp

bernilai'0'. Keadaan output OpAmp bisa dipakai untuk menbangkitkan sinyal permintaan layanan interupsi. Sinyal ini dibangkitkan saat output OpAmp berubah dari '0' ke '1', atau sebaliknya.



Gambar 2.13 Blok Diagram Analog Komparator

Sumber: *Data Sheet* ATmega8515

2.1.9. Port-Port I/O

Semua port pada AVR memiliki kebenaran fungsional *read-modify-write* ketika digunakan sebagai port I/O umum. Ini berarti bahwa arah dari satu pin port dapat diubah tanpa bermaksud mengubah arah dari pin yang lain dengan instruksi SBI dan CBI.

- Port A

  Tiga lokasi alamat memori I/O dilokasikan pada port A, masing-masing adalah register data-Port A, $1B ($3B), register data *direction* (register pengrah data)-DDRA, $1A ($3A), dan pin input port A-PIN A, $19 ($39). Pin-pin port A memiliki fungsi alternatif yang terhubung pada plihan data eksternal SRAM. Port A dapat dikonfigurasikan menjadi *multiplexed low order* alamat/data bus selama akses ke data memori eksternal. (blok diagram dapat dilihat pada lampiran).

- Port B

Tiga lokasi alamat memori I/O yang dilokasikan pada port D, masing-masing adalah register data-PORTB, $18 ($38), register pengarah data-DDRB, $17 ($37), dan pin input port B-PINB, $16 ($36). (Blok diagram port B dan fungsi alternative pinnya dapat dilihat pada lampiran).

- Port C

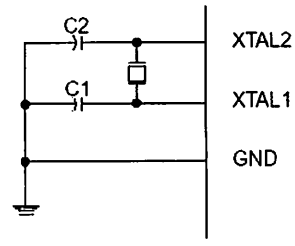
  Tiga lokasi alamat memori I/O yang dilokasikan pada port C, masing-masing adalah register data-PORTC, $15 ($35), register pengarah data-DDRC, $14 ($34), dan pin input port C-PINC, $13 ($33). (Blok diagram skematik dapat dilihat pada lampiran).

- Port D

  Tiga lokasi alamat memori I/O yang dilokasikan pada port D, masing-masing adalah register data-PORTD, $12 ($32), register pengarah data-DDRD, $11 ($31), dan pin input port D-PIND, $10 ($30). (Blok diagram skematik port D dan fungsi alternatif pinnya dapat dilihat pada lampiran).

2.1.10. Osilator Kristal

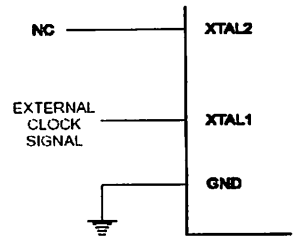
XTAL1 dan XTAL2 adalah input dan output dari inverting amplifier yang dapat dikonfigurasikan untuk digunakan sebagai osilator di dalam chip.



Gambar 2.14 Koneksi Osilator

Sumber: *Data Sheet* ATmega8515

Untuk menjalankan dari sumber clock eksternal XTAL2 tidak terhubung ke XTAL1 seperti gambar di bawah ini:



Gambar 2.15 Konfigurasi Drive External Clock

Sumber: *Data Sheet* ATmega8515

2.2 Pemutar/Perekam Suara ISD Voice 1420

Peralatan penyimpan informasi suara, ISD 1420 mempunyai kualitas bagus, dengan durasi penyimpanan 20 detik. Peralatan CMOS yang ada didalamnya adalah *chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smouthing filter,* dan *speaker amplifier.* ISD 1420 adalah kompatibel dengan mikrokontroler. Alamat dan jalur kendali dapat di hubungkan dengan mikrokontroler, sehingga mengijinkan penyimpanan dan pengalamatan yang komplek. Perekaman disimpan dalam suatu *chip* yang tidak mudah berubah dalam *cell* memori. Sinyal suara audio disimpan secara langsung ke memory pada tempat naturalnya dengan kualitas suara yang bagus.

Penjelasan dari masing-masing kaki ISD 1420 adalah sebagai berikut:

- *Voltage Input* (VCCA, VCCD), untuk mengurangi *noise*, rangkaian analog dan digital dalam IC ISD2500 digunakan sebagai *power supply* tersendiri dalam pak.

- *Groung Input* (VSSA,VSSD), pin ini harus dihubungkan dalam *power supply ground* dengan impedansi rendah.
- *Powe Down Input* (PD), ketika tidak sedang digunakan untuk merekam atau menyatakan, pin PD harus diberi logika tinggi. Ketika pulas *overflow* (OVF) rendah, PD harus dibawa ke logika tinggi untuk me-*reset address pointer* kembali ke awal perekaman atau *playback.*
- *Chip Enable Input* (CE), pin CE diberi logika rendah untuk membolehkan semua operasi perekaman dan *playback.* Alamat input dan *playback/record input* (P/R) ditahan dengan adanya transisi turun dari CE.
- *Playback/Record Input* (P/R), P/R *input* ditahan dengan adanya transisi turun dari pin CE. Logika tinggi akan memilih *playback cycle* dan logika rendah untuk memilih *record cycle..* Untuk *record cycle,* alamat *input* menetapkan mulainya alamat dan merekam secara kontinyu sampai PD atau CE ke transisi tinggi atau adanya *overflow.* Ketika *record cycle* terhenti dengan adanya transisi tinggi dari PD atau CE, sinyal *End-of-Message* (EOM) disimpan di alamat dan akan memutar suara perekaman sampai alamat EOM ditemukan.
- *End-of-Message Run Output* (EOM), sebuah alamat akan dimasukkan secara otomatis di akhir masing-masing perekaman. Pulsa *output* EOM akan rendah untuk setiap periode dari T_{EOM} diakhir masing-masing perekaman.
- *Microphone Input* (MIC), digunakan untuk mentransfer sinyal suara ke *on-chip preamplifier*. Rangkaian *on-chip Automatic gain Control* (AGC)

mengontrol penguatan dari *preamplifier* dari -15 sampai 24B.

- *Microphone Reference Ibput* (MIC REF), adalah *input* pembalik ke *microphonepreamplifire*. Ini untuk memberikan *noise-canceling* atau *common-mode rejection input* ke IC ini ketika dihubungkan ke sebuah *microphone* diferensial.
- *Overflow Output* (OVF), sinyal pulsa rendah pada akhir tempat memori, mengindikasikan bahwa IC ini telah terpenuhi dan pesan telah melebihi kapasitas. Keluaran OVF kemudian diikuti masukan CE sampai pulsa PD telah me-*reset*. Pin ini juga dapat untuk menambah beberapa IC 1420 untuk menambah durasi *recrd/playback*.
- *Automatic Gain Control Input* (AGC), AGC secara dinamik mengubah penguatan dari *preanplifire* untuk mengimbangi dari lebar jarak dari level *microphone input*. AGC memberikan jarak secara penuh dari suara rendah ke tinggi untuk direkam dengan distorsi minimal.
- Analog *Output* (ANA OUT), pin ini memberikan *preamplifier output* ke pengguna. Tegangan penguatan dari *preamplifier* ditentukan oleh level tegangan dari pin AGC.
- Analaog *Input* (ANA IN), pin ini akan mentransfer sinyal ke dalam chip untuk perekaman. Untuk *microphe input,* pin ANA OUT harus dihubungkan ke kapasitor eksternal ke pin ANA IN. Jika permintaan *input* diperoleh dari sumber lain darai *microphone,* sinyal ini dapat langsung dikopel oleh kapasitor ke pin ANA IN.

- *External Clock Input* (XCLK), untuk ISD 1420 mempunyaoi sebuah internal *pull-down*. Frekuensi *clock* sampling internal kurang lebih 1& dari spesifikasi. Frekuensi ini bervariasi dari ± 2,25% berada pada suhu kamar dan tegangan kerja. Jika *power supply* yang digunakan mempunyai toleransi ± 5% pada tempaeratur dan tegangan kerja. Jika *power supply* yang digunakan mempunyai presisi tinggi, maka alat ini dapat di-*clock* langsung pada pin XCLK. *Duty cyle* pada *input clock* tidak perlu dipermasalahkan karena *clock* dengan segera dibagi dua. Jika pin XCLK tidak digunakan, harus dihubungkan ke *ground.*

- *Speaker Output* (SP+/SP-), ISD 1420 telah mempunyai sebuah *driver on-chip* diferensial speaker, sanggup memikul beban 50 mW dalam 16 ohm dari AUX IN. Speaker *output* berada pada level VSSA selama proses *record* dan *power down.*

- *Auxilary Input* (AX/MX), dihubungkan langsung ke kaki keluaran *amplifier* dan keluaran speaker ketika CE, P/R berada pada logika tinggi dan *playback* tidak aktif.

- *Address Mode Input* (AX/MX), mempunyai dua fungsi tergantung pada level dari dua *Most Significant Bit* (MSB) dari alamat tersebut (A_8 dan A_9) . Jika salah satu atau keduanya dari dua MSB berlogika rendah, semua input diaggap sebagai bit alamat dan digunakan sebagai awal alamat untuk proses *record* atau *playback cycle* terbaru. Alamat input ditahan oleh transisi turun

dari CE. Jika kedua MSB, berlogika tinggi, *address/mode input* dianggap sebagai bit *mode*.

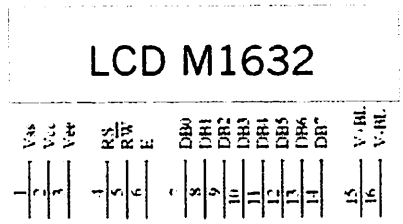
2.3 LCD (*Liquid Cristal Display*)

Liquid Cristal Display adalah modul tampilan yang mempunyi konsumsi daya yang relatif rendah dan terdapat sebuah kontroler CMOS didalamnya. Kontroler tersebut berfungsi sebagai pembangkit ROM / RAM dan *display* data RAM. Semua fungsi tampilan dikontrol oleh suatu instruksi, modul LCD dapat dengan mudah di*interface*kan dengan MPU.

LCD yang digunakan dalam Tugas Akhir ini adalah LCD yang memiliki kemampuan sebagai berikut :

- Meliputi 32 karakter yang dibagi menjadi 2 baris dengan display dot matrik 5 x 7 ditambah *cursor*.
- Karakter generator ROM dengan 192 karakter.
- Karakter generator RAM dengan 8 tipe karakter.
- Dilengkapi fungsi tambahan yaitu *display clear*, *cursor home*, *display ON/OFF*, *cursor ON / OFF*, *displat character blink*, *cursor shift* dan *display shift*.
- Internal data.
- 80 x 8 bit display data RAM.
- Dapat di*interface*kan dengan MPU 8 atau 4 bit.
- Internal otomatis dan reset pada *power ON*.
- + 5 Volt *power supply* tunggal.

Gambar dibawah ini menunjukkan LCD beserta pin – pinnya :



Gambar 2.16 Bentuk fisik dari LCD

Sumber : LCD Module User Manual, Seiko Instruments Inc

Dimana untuk definisi pin-pin yang terdapat dalam LCD tersebut dapat dilihat pada tabel berikut ini :

Tabel 2.3

Definisi pin-pin LCD

Nama pin	Jumlah	I/O	Tujuan	Fungsi
DB0 – DB3	4	I/O	MPU	Tristate bidirectional lower 4 data bus : data dibaca dari modul ke MPU ditulis ke modul melalui bus.
DB4 – DB7	4	I/O	MPU	Tristate bidirectional upper 4 data bus : data dibaca dari modul ke MPU atau dari MPU ditulis ke modul melaui bus.
E	1	Input	MPU	Sinyal operasi dimulai : sinyal aktif baca/tulis.
R/W	1	Input	MPU	Sinyal pilih data dan tulis (0 : tulis; 1 : baca).
RS	1	-	Power Supply	Sinyal pilih register : 0 : Instruction register (write) busy flag dan address counter (read) 1 : Data register (write dan read)
V_{LC}	1	-	Power Supply	Penyetelan kontras pada tampilan LCD
V_{DD}	1	-	Power Supply	+ 5 Volt
V_{SS}	1	-	Power Supply	Ground 0 Volt
V_{BL} -	1	-	-	Ground untuk lampu (back light)
V_{BL} +	1	-	-	+ 5 Volt untuk lampu (back light)

Sumber : LCD Module User Manual, Seiko Instruments Inc

2.4. Keyboard PC

2.4.1. Tata Kerja Keyboard PC

Setiap kali salah satu tombol keyboard ditekan atau dilepas, *keyboard* akan mengirim kode ke *host* (*host* adalah computer kalau *keyboard* dihibungkan ke PC, atau berupa mikrokontroler kalau *keyboard* dihubungkan ke peralatan berbasis mikrokontroler).

Komunikasi antar *keyboard* dan *host* adalah komunikasi dua arah, *keyboard* mengirim *scan code* ke *host*, *host* bisa mengirim perintah untuk mengatur kerja dari *keyboard*. Kode perintah untuk *keyboard* tidak sebanyak *scan code*, berikut ini daftar kode printah untuk *keyboard* (dalam heksadesimal) adalah:

- **ED,** perintah untuk menyalakan/memadamkan lampu indikator di *keyboard*, setelah menerima perintah **ED** dari *host*, *keyboard* akan menjawab dengan **FA** sebagai tanda perintah itu telah dikenali (**ACK** – *acknowlwdge*) dan menunggu 1 byte perintah lagi dari *host* untuk menentukan lampu indikator mana yang perlu di-nyala/padam-kan. 1 byte perintah susulan tersebut akan diartikan sebagai berikut : bit 0 dipakai untuk mengatur lampu indikator ***Scroll Lock***, bit 1 untuk ***Num Lock*** dan bit 2 untuk ***Caps Lock***, bit-bit lainnya diabaikan.
- **EE,** dipakai *host* untuk memeriksa apakah *keyboard* masih aktip. Setelah menerima perintah **EE** dari *host*, *keyboard* akan menjawab dengan **EE** pula, menandakan dirinya masih aktif.
- **F0,** ada *keyboard* yang dilengkapi 3 set *scan code*, perintah ini dipakai untuk memilih *scan code* yang ingin dipakai. Setelah menerima perintah **F0** dari

host, keyboard akan menjawab dengan **FA** sebagai tanda perintah itu telah dikenali (**ACK** – *acknowlwdge*) dan *host* menjawab 1 byte lagi (nilainya 1 2 atau 3) untuk memilih set *scan code*. Jika byte yang dikirimkan nilainya 0, *keyboard* akan menjawab dengan nomor set *scan code* yang saat itu dipakai.

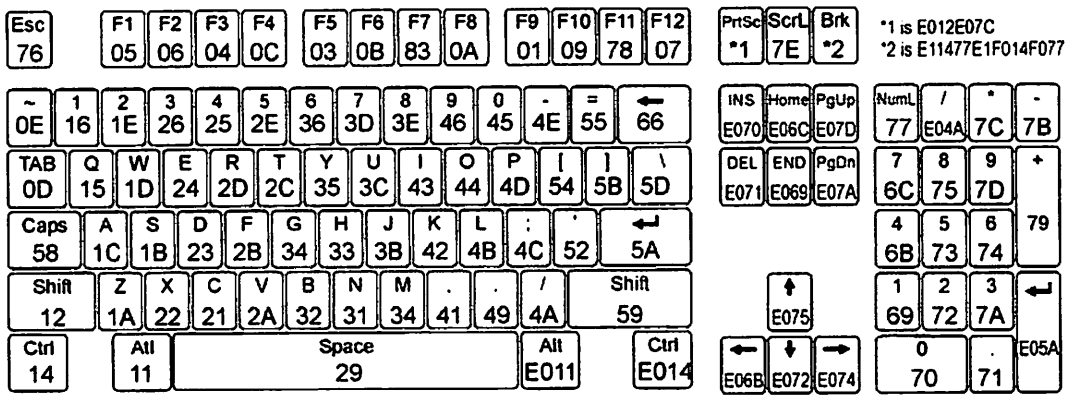
- **F3,** dipakai untuk mengatur kecepatan tanggapan *keyboard (Typematic Repeat Rate)*, setelah menerima perintah **F3** dari *host, keyboard* akan menjawab dengan **FA** sebagai tanda perintah itu telah dikenali (**ACK** – *acknowlwdge*) dan *host* menjawab 1 byte nilai kecepatan tanggapan *keyboard* yang dikehendaki.
- **F4,** dipakai untuk me-aktip-kan kembali *keyboard*, setelah menerima perintah ini *keyboard* akan menjawab dengan **FA** (**ACK** – *acknowlwdge*).
- **F5,** dipakai untuk me-nonaktip-kan *keyboard*, setelah menerima perintah ini *keyboard* akan menjawab dengan **FA** (**ACK** – *acknowlwdge*).
- **FE,** dipakai meminta *keyboard* mengirim ulang *scan code* terakhir yang dikirim.
- **FF,** Perintah untuk me-reset *keyboard*

Selain perintah dari *host, keyboard* juga mempunyai kode-kode lain selain *scan code* yang dikirimkan ke *host*, sebagai berikut :

- **FA,** berarti **ACK** (*acknowledge*), yaitu jawaban dari *keyboard* bahwa perintah dari *host* sudah dikenali dengan baik.
- **AA,** berarti *keyboard* selesai memeriksa diri dan siap bekerja setelah diberi catu daya

- **EE**, identik dengan perintah **EE** di atas
- **FE**, artinya minta *host* mengulang perintah terakhir yang dikirim
- **FF / 00**, berarti terjadi kesalahan di *keyboard*

Gambar 2.17 menjelsakan *scan code* masing-masing tombol *keyboard* PC. Terlihat pada gambar tersebut, *scan code* tidak berupa kode ASCII yang biasa dipakai mewakili huruf , dan ditentukan secara acak, juga. Sehingga setelah diterima *host*, *scan code* harus dirubah menjadi kode ASCII dengan memakai cara 'pencarian tabel'.

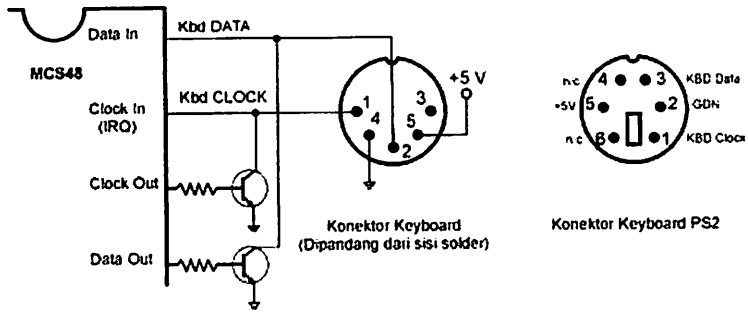


Gambar 2.17 *Keyboard* PC dan *ScanCode*

Sumber : *http://alds.stts.edu/digital/keyboard_files*

2.4.2. Rangkaian Penghubung

Keyboard PC dibangun dengan mikrokontroler MCS48, yang merupakan saudara tua MCS51 tapi jauh lebih sederhana. Untuk keperluan membentuk rangkaian penghubung tidak perlu diketahui bagaimana cara kerja mikrokontroler dalam keyboard, tapi cukup meninjau rangkaian elektronik bagian penghubung pada gambar 2.18.



Gambar 2.18 Penghubung dalam *Keyboard* PC

Sumber : *www.beyondlogic.org/2=kboard/11er*

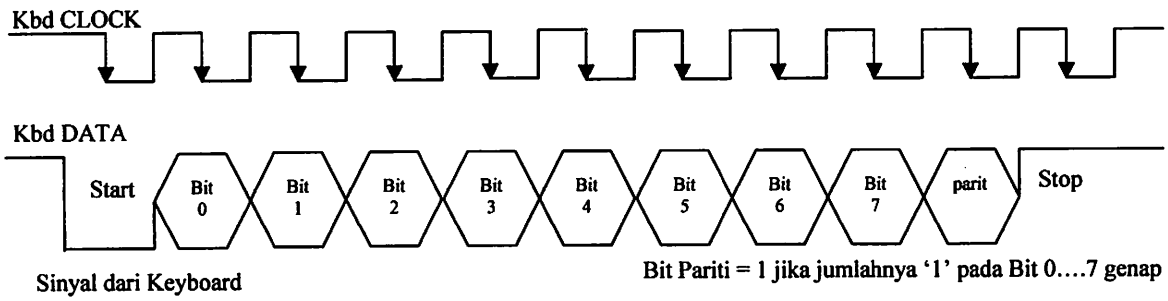
Kbd Clock dibangkitkan oleh MCS' 48, merupakan sinyal pendorong **Kbd Data** yang bias bersumber dari *keyboard* maupun bersumber dari PC. Level tegangan pada kedua sinyal ini memenuhi standart sinyal TTL biasa, jadi bias langsung dihubungkan ke Mikrokontroler. Sumber daya untuk *keyboard* dicatu dari luar, harus diperhatikan kebutuhan arusnya cukup besar bias sampai 300 mA.

2.4.3. Sinyal pengiriman data dari Keyboard

Saat tidak ada pengiriman data, sinyal **Kbd Clok** dan **Kbd Data** dalam kadaan '1'. Sinyal pengiriman data dari keyboard dari *keyboard* dalam gambar 2.11 dijelaskan sebagai berikut :

- Data mulai dikirimkan dengan me-nol-kan **Kbd data** sebagai tanda mulai pengiriman (start bit), berapa saat kemudian setelah **Kbd Data** stabil disusul **Kbd Clock** berubah menjadi '0' dan kembali '1' lagi, ini berarti selesai mengirimkan data 1 bit.
- Setelah mengirim 'start bit', dikirimkan bit 0, bit 1 dan seterusnya sampai bit 7.

- Menyusul dikirim 'parity bit', yaitu bit control yang berguna bagi host penerima data untuk memastikan data yang diterima tidak ada kesalahan. Jika banyaknya bit '1' yang terdapat di bit 0 sampai bit 7 ganjil,'parity bit' akan bernilai '1'.
- Sebagai penutup (stop bit) Kbd Data dikembalikan ke keadaan normalnya, yaitu '1'.



Gambar 2.19 Sinyal komunikasi data seri keyboard

Sumber : *www.beyondlogic.org/2=kboard/11er*

2.5 . Minimum Sistem AT89S52

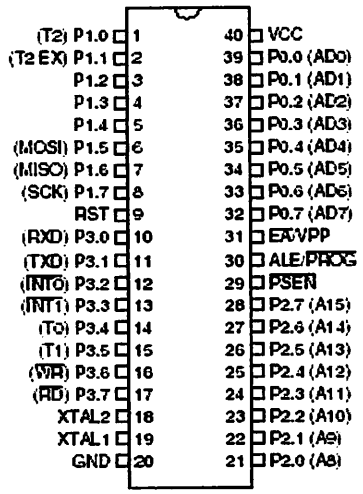
2.5.1. Minimum Sistem AT89S52

Mikrokontroller AT89S52 merupakan salah satu anggota keluarga dari MCS-51, yaitu suatu komponen produksi ATMEL yang berorientasi kontrol (*microcontroller*). Intel mengklarifikasikan dalam kelompok *embedded microcontroller*, yang artinya adalah mikrokontroller yang dapat diprogram ulang (*reprogrammable*). Di dalam *chip* mikrokontroller AT89S52 ini sudah tersedia berbagai macam peralatan pendukung mikroprosesor seperti RAM, *serial port, bus-bus* data dan lainnya yang membuat

Pemakai *chip* ini dapat menekan penambahan komponen pendukung. Spesifikasi perangkat keras dari mikrokontroller AT89S52 adalah sebagai berikut

- CPU (*Central Processing Unit*) dengan lebar data 8 *bit*.
- Prosesor *Boolean* untuk operasi logika 1 *bit*.
- Pembangkit clock internal.
- Tiga buah timer/counter 16 bit.
- Dua buah saluran interupsi eksternal.
- Jalur I/O dua arah (bidirectional) 32 buah.
- Memori program terpisah dari memori data.
- Memori data internal 256 byte.
- Alamat memori program eksternal 64 kilobyte.
- Alamat memori data eksternal 64 Kilobyte.
- Memori program internal sebesar 8 Kilobyte.

Gambar 2.20. memperlihatkan konfigurasi pin dari mikrokontroller AT89S52.



Gambar 2.20 Konfigurasi pin AT89S52
Sumber : *Atmel,* 2001:1-5

Adapun penjelasan dari masing-masing pin mikrokontroler AT9S52 :

- Pin 1 sampai 8

  Port 1 : merupakan 8-*bit* saluran masukan atau keluaran dua arah. Setiap saluran mampu melayani 4 masukan.

- Pin 9

  RST : Merupakan masukan *reset*. Logika *high* yang akaan membuat mikrokontroller AT9S52 menjalankan rutin *reset*.

- Pin 10 sampai 17

  Port 3 : *port* 3 terdiri dari 8 saluran masukan atau keluaran dua arah. Setiap salurannya mampu melayani 4 masukan. Selain sebagai *port* masukan atau keluaran, *port 3* juga mempunyai fungsi-fungsi khusus yang dimiliki oleh keluarga MCS-51. Fungsi tersebut dapat dilihat dalam tabel 2.4.

- Pin 18 sampai 19

  X1 (XTAL) dan X2 (XTAL2) : Jika dikonfigurasikan bersama sebuah kristal akan membentuk rangkaian osilator *on-chip* pada mikrokontroler (*Atmel,* 2001:15)

- Pin 20 sampai 27

  Port 2 : *Port 2* terdiri dari 8 saluran masukan atau keluaran dua arah. Setiap salurannya mampu melayani 4 masukan. *Port* 2 mengeluarkan alamat bagian tinggi (A8-A15), selama pengambilan instruksi dari memori program eksternal dan pengambilan data dari

memori data eksternal yang menggunakan mode pengalamatan 16-*bit* (dengan perintah MOVX@DPTR).

- Pin 29

  PSEN : *Program Store Enable* merupakan sinyal baca yang mengeksekusi memori program eksternal.

- Pin 30

  ALE/ *PROG* : *Addres Latch Enable* merupakan pulsa yang berfungsi menahan alamt rendah (A0-A7) pada *port* 0, selama dilakukan proses baca atau tulis memori eksternal. Pin ini juga berfungsi sebagai asukan pulsa program (PROG), selama dilakukan pemrograman pada EEPROM eksternal.

- Pin 31

  EA/VP : *External Access. EA* dihubungkan dengan VSS untuk memungkinkan pengambilan instruksi pada memori program eksternal yang berlokasi 0000h sampai FFFFh. Jika diingkan menggunakan memori pemrograman internal, maka *EA* dihubungkan dengan VCC.

- Pin 32 sampai 39

  Port 0 : *port* 0 terdiri dari 8 saluran masukkan atau keluaran dua arah. Setiap saluran mampu melayani 8 masukan. *Port* 0 merupakan saluran alamat bagian rendah (A0-A7), yang dimultipleks dengan saluran bus data (D0-D7), yang digunakan

pada saat mengakses memori data eksternal dan memori program eksternal.

- Pin 40

  VCC : masukan catu daya 5 volt, dengan toleransi ± 10%.

Keluarga MCS®51 yang diproduksi intel mempunyai konfigurasi yang berbeda beda sesuai dengan jenisnya. Masing masing saling kompatibel serta mempunyai kelebihan tersendiri. Misalnya mikrokontroller AT89S8252 merupakan padanan dari mikrokontroller 8051. Tabel 2.1. memperlihatkan sebagian dari keluarga MCS®51.

Tabel 2.4 Keluarga MCS®51

Tipe	Tipe tanpa EPROM	Tipe ber-EPROM	Kapasitas ROM	Kapasitas RAM	Port I/O	Pewaktu
8051	8031	-	4K	128	4	2
8051AH	8031H	8751H	4K	128	4	2
8052AH	8032AH	8752BH	8K	256	4	3
80C51BH	80C31BH	87C51	4K	128	4	2
80C52	80C32	-	8K	256	4	3
83C51FA	80C51BH	8751FA	8K	256	4	3
83C51FB	80V51FB	87C51FB	16K	256	4	3
83C152	80C152	-	8K	256	5	3
89S52	-	89S52	8K	256	4	3

Sumber : *Bereksperimen Dengan Mikrokontroller 8031,5.*

2.5.2. Organisasi Memori

Organisasi memori pada mikrokontroler AT89S52 dibagi menjadi dua bagian besar yaitu memori program dan memori data. Pembagiannya didasarkan atas fungsi dari penyimpanan data maupun program digunakan untuk menyimpan instruksi yang akan dijalankan oleh mokrokontroler, memori data digunkan sebagai tempat penyimpan data yang sedang diolah oleh mikrokontroler.

Program mikrokontroler disimpan di memori program berupa ROM. Mikrokontroler AT89S52 dilengkapi dengan ROM internal, untuk program yang besar digunakan ROM eksternal yang terpisah dari mikrkontroler. Untuk dapat menggunakan memori program eksternal ini penymat /$\overline{EA}$ dihuungkan dengan penyemat Vss (logika 0).

Memori program mikrokontroler menggunakan alamat 16 bit mulai 0000H – FFFFH, sehingga kapasitas penyimpanan program maksimal adalah 2^{16} *byte* atau 64 Kb. Sinyal yang digunkan untuk membaca memori program eksternal adalah $\overline{PSEN}$ (*Program Store Enable*).

Selain memori program mikrokontroller AT89S52 juga memiliki memori data internal berkapasitas 256 *byte* dan mampu mengakses memori data eksterna lsebesar 64Kb. Semua memori data internal dapat dialamati dengan pengalamatan langsung atau tidak langsung. Ciri dari pengalamatan langsung adalah *operand* berisi alamat data yang diolah. Sedangan cirri dari pengalamatan tidak langsung adalah *operand* alamat *register* yang berisi alat yang diolah. Untukmembaca data digunkan sinyal /$\overline{RD}$, sedangkan utuk menulis data digunkan sinyal/ $\overline{WR}$.

2.5.3. Register Fungsi Khusus

Register fungsi khusus (*Special Function Register*) terletak pada 128 *byte* bagian atas memori data internal dan berisi *register-register* untuk pelayanan *latch port, timer, program status words, control peripheral* dan sebagainya. Alamat register fungsi khusus ditunjukkan pada Tabel 2.5

Register-register ini hanya dapat diakses dengan pengalamatan langsung. Enam belas alamat pada register fungsi khusus dpaat dialamati per*bit* maupun per-

byte dan terletak pada alamat 80_H-FF_H. secara perangkat keras, register fungsi khusus ini dibedakan dengan memori data internal.

Tabel 2.5 Nama dan Alamat *Register* pada *Register* Fungsi Khusus

Simbol	Nama Register	Nilai pada saat reset	Alamat
ACC	*Accumulator*	00_H	$0E0_H$
B	*Register B*	00_H	$0F0_H$
PSW	*Program Status Word*	00_H	$0D0_H$
SP	*Stack Pointer*	07_H	81_H
DPTR	*Data pointer 2 byte*		
DPL	*Low byte*	0000_H	82_H
DPH	*High byte*	0000_H	83_H
P0	*Port 0*	FF_H	80_H
P1	*Port 1*	FF_H	90_H
P2	*Port 2*	FF_H	$0A0_H$
P3	*Port 3*	FF_H	$0B0_H$
IP	*Interrupt priority control*	$XXX00000_H$	$0B8_H$
IE	*Interrupt enable control*	$0XX00000_H$	$0A8_H$
TMOD	*Timer/counter mode control*	00_H	89_H
TCON	*Timer/counter control*	00_H	88_H
TH0	*Timer/counter 0 high byte*	00_H	$8C_H$
TL0	*Timer/counter 0 low byte*	00_H	$8A_H$
TH1	*Timer/counter 1 high byte*	00_H	$8D_H$
TL1	*Timer/counter 1 low byte*	00_H	$8B_H$
SCON	*Serial control*	00_H	98_H
SBUF	*Serial data buffer*	*Independen*	99_H
PCON	*Power control*	HMOS $0XXXXXXX_H$ CHMOS $0XXX0000_B$	87_H

Sumber : *Bereksperimen Dengan Mikrokontroler 8031,* 19-20.

Beberapa macam register fungsi khusus yang sering digunakan, dijelaskan sebagai berikut (Modul Pelatihan MCS-51, 14-15) :

- *Accumulator* (ACC) merupakan *register* untuk penambahan dan pengurangan. Perintah *Mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register B* merupakan *register* khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Program Status Word* (PSW) terdiri dari beberapa *bit* status yang menggambarkan kejadian di akumulator sebelumnya. Yaitu *carry bit,*

auxiliary carry, dua *bit* pemilih bang, bendera *overflow, parity bit,* dan dua bendera yang dapat didefinisikan sendiri oleh pemakai.

- *Stack Pointer* (SP) merupakan *register 8 bit* yang dapat diletakkan di alamat manapun pada RAM internal. Isi *register* ini dtambah sebelum data disimpan, selama instruksi *PUSH* dan *CALL*. Pada saat *reset, register* SP diinisialisasi pada alamat 07_H, sehingga *stack* akan mulai pada lokasi 08_H.
- *Data Pointer* (DPTR) terdiri dari dua *register*, yaitu untuk *byte* tinggi (*Data Pointer High,*DPH) dan *byte* rendah (*Data Pointer Low,*DPL) yang berfungsi untuk pengalamatan alamat 16 *bit.*
- *Port 0* sampai *port 3* merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada *port* 0,1,2,3. Masing-masing *register* ini dapat dialamati per-*byte* maupun per-*bit.*
- *Serial Data Buffer* (SDUF) merupakan dua *register* yang terpisah, *register buffer* pengirim dan sebuah *register buffer* penerima. Meletakkan data SBUF berarti meletakkan pada *buffer* pengirim yang akan mengirimkan data melalui transmisi serial. Membaca data SBUF berarti menerima data dari *buffer* penerima.
- *Control Register* terdiri dari *register* yang mempunyai gingsi kontrol. Untuk mengontol system interupsi, terdapat dua *register* khusus, yaitu *register* IP (*interrupt priority*) dan *register* IE (*interrupt enable*). Untuk mengontrol pelayanan *timer/counter* terdapat *register* khusus, yaitu *register* TCON (*timer/counter control*) serta untuk pelayanan *port* serial menggunakan *register* SCON (*serial port control*).

2.5.4. Port Masukan dan Keluaran

Mikrokontroler AT89S52 mempunyai 4 *port* dan masing-masing *port* terdiri dari 8 saluran *bit.* Keempat *port* ini bersifat *bidirectional* yaitu dapat digunakan sebagai masukan atau keluaran.

Port 0 digunakan sebagai saluran data yang dimultipleks dengan saluran alamat rendah untuk mengakses memori eksternal, baik momori program maupun memori data. *Port* 2 mengeluarkan bagian alamat tinggi untuk mode pengalamatan memori 16 *bit. Port* 1 dan 3 berfungsi sebagai saluran masukan dan keluaran multi fungsi. Jika dibutuhkan *port* 3 mempunyai fungsi khusus seperti ditunjukkan pada tabel 2.6.

Tabel 2.6 Fungsi Khusus *Port* 3

Nama Penyemat	Fungsi Khusus
Port 3.0	RxD (*port* masukan serial)
Port 3.1	TxD (*port* keluaran serial)
Port 3.2	/INT 0 (masukan interupsi eksternal 0)
Port 3.3	/INT 1 (masukan interupsi)
Port 3.4	T0(masukan pewaktu eksternal 0)
Port 3.5	T1 (masukan pewaktu eksternal 1)
Port 3.6	/WR (sinyal tulis memori data eksternal)
Port 3.7	/RD (sinyal baca memori data eksternal)

Sumber : *Atmel,* 2001:4.

2.5.5. Sistem Interupsi

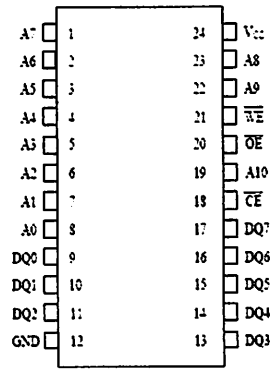
Mikrokontroler AT89S52 mempunyai dua sumber interupsi ekstenal dan sumber interupsi internal yang data deprogram agar sensitif terhadap perubahan level atau transisi. Interupsi *timer* aktif saat *register timer* yang bersangkuatan mengalami *rollover,* iterupsi seriak akan aktif pada saat mikrokontroler mengirim atau menerima data. Setiap sumber interupsi dapat diaktifkan atau dimatikan melalui perangkat lunak. Interupsi yang mempunyai tingkatan prioritas lebih

tinggi tidak dapat diinterupsi oleh yang lebih rendah. Meskipun demikian perangkat lunak dapat diubah, yaitu dalam *register interrupt priority* (IP).

2.6. SistemPewaktuan (*Real Time Clock*) IC DS1642

Real Time Clock (RTC) dan RAM dengan tipe *Non Volatile (NV)* produksi *Dallas Semiconductor* teintegrasi keduanya dalam satu komponen IC RTC NVRAM. Keduanya dapat diakses melalui bus alamat dan bus data, register RTC terdiri dari register tahun, bulan, tanggal, hari, jam, menit dan detik. Koreksi tiap register tersebut dirancang secara otomatis dan dapat dipertahankan akurasinya sampai 100 tahun. Di dalam komponen tersebut terdapat *battery internal* untuk mencatu *static RAM* dan secara otomatis akan men-*swtich* catu ke vcc ekternal jika vcc tersebut diatas tegangan catu *battery internal.*

DS1642 adalah serpih yang dipakai sebagai basis pewaktuan buatan *Dallas Semiconductor.* Terdiri atas 24 penyemat dengan konfigurasi penyemat seperti ditunjukkan dalam Gambar 2.21.



Gambar 2.21 Konfigurasi Penyemat IC DS1642

Sumber: *Dallas Semiconductor Data Sheets*, 1998:1

Keistimewaan IC DS1642 antara lain adalah:

- Terintegasi NV SRAM, RTC, *crystal,* sumber energi *lithium.*
- Standar JDEC *bytewide* 2K x 8 *static* RAM *pinout.*
- Menghitung detik, menit, jam dalam sehari-hari.
- Waktu aksesnya adalah 70ns dan 100ns.
- Seratus tahun kelender.
- Mempunyai catu daya *back-up.*
- Dapat tetap beroperasi selama lebih dari 10 tahun tanpa kehadiran catu daya *external* (karena adanya baterai cadangan di dalam RTC).

Secara keseluruhan, fungsi penyemat RTC DS1642 adalah :

- **DQ0 – DQ7 :**

  Merupakan bus alamat/data dua arah yang ter*multipleks*. Pengiriman data maupun alamat maupun ke RTC dilakukan melalui bus ini.

- **GND dan Vcc:**

  Merupakan penyemat catu daya. Vcc dihubungkan dengan catu daya +5 volt dan *ground.*

- **$\overline{OE}$ (Output Enable) :**

  Dihubungkan dengan sinyal $\overline{RD}$ yang berasal dari mikrokontroler untuk melakukan proses membaca data RAM *internal* RTC.

- **$\overline{WE}$ (Write Enable) :**

  Digunakan untuk proses penulisan data RAM *internal* RTC.

- **A0 – A7 (Address Input) :**

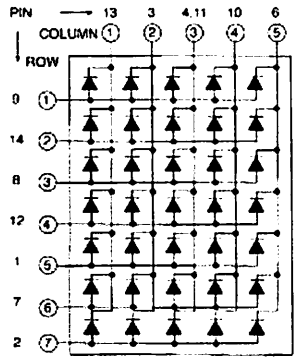
  Merupakan masukan untuk mengaktifkan periferal RTC.

RTC mempunyai RAM *internal* sebesar 64 byte, yang berisi data-data mengenai waktu yang sedang berjalan, seperti: detik, menit, jam, hari, tanggal, bulan, tahun, serta beberapa register. Secara otomatis RTC akan mengganti data dalam RAM *internal* sesuai dengan perhitungannya. Jika diinginkan mengambil data waktu, maka dibaca dalam RAM *internal* sesuai alamat yang dimaksud.

2.7 LED sebagai Dot Matrik

Tampilan matrik titik (Dot Matrik) terdiri dari sejumlah LED (*Light Emitting Diode*) yang disusun secara baris dan kolom. Susunan yang paling sering digunakan adalah matrik 5x7, yaitu lima kolom dan tujuh baris. Susunan X kali Y ini memungkinkan pengalamatan X dan Y, susunan LED di dalam dot matrik tersebut dapat digunakan sebagai penampil karakter yang diinginkan.

Matrik 5x7 dapat digunakan untuk menyajikan karakter *alfanumerik* yang lengkap. Proses pembangkitan karakter antara lain melibatkan proses *scaning* baris atau kolom, proses *scanning* tersebut akan memilih susunan (baris atau kolom) LED yang tepat untuk dinyalakan atau dipadamkan oleh *driver* dot matrik.. Proses ini diulang untuk baris atau kolom berikutnya dipilih dengan urutan tertentu, proses diatas diulang mulai baris paling atas (atau kolom pertama) hingga terahir yang berulang terus dengan frekuensi yang sama. Frekuensi *driving* LED diatas frekuensi kemampuan mata untuk membedakan padam dan nyala sehingga proses *scanning* dot matrik tidak terlihat. Rangkaian skematik dot matrik 5x7 ditunjukkan dalam Gambar 2.22.



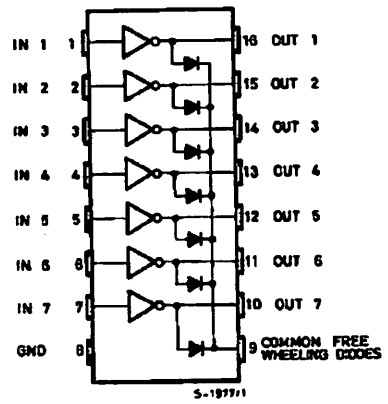
Gambar 2.22 Schematic Dot Matrik 5 x 7

Sumber : *Fairchild Semiconductor Data Sheets*, 2000:1

Jika frekuensi *scanning* diatas kemampuan mata manusia untuk melihat kedipan tersebut akan diperoleh bebas kedip. Jika matrik di *scan* dari kiri ke kanan kolom demi kolom disebut vertikal *scaning*, jika dilakukan baris demi baris disebut horizontal *scaning*.

2.8 *Driver* LED (ULN2003)

ULN2003 sebagai penggerak perangkat LED dalam dot matrik merupakan rangkaian transistor yang tersusun Darlington sebanyak 7-bit input-output. Input dari ULN2003 kompatibel dengan TTL dan +5v CMOS. Setiap saluran dari 7-bit output, mampu melewatkan arus maksimal 500 mA. Dengan karakteristik yang dimiliki, ULN2003 akan dirangkai sebagai penggerak perangkat LED dalam dot matrik (*driver*). Dalam Gambar 2.23 diperlihatkan diagram dari ULN2003.

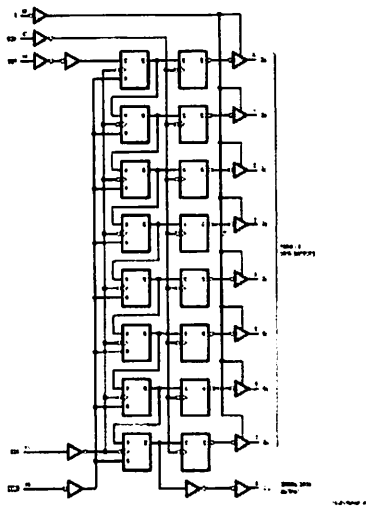


Gambar 2.23 Pin koneksi ULN2003

Sumber : *ST Microelectronic Data Sheet*, 1998:3

2.9 Register Geser (74HC595)

IC 74LS595 terdiri atas enam belas buah flip-flop tipe D. Register geser ini disusun dari enam belas buah *flip-flop* tipe D. Register ini disebut register geser 8-bit karena mempunyai delapan tempat untuk menyimpan data yaitu Qa sampai dengan Qd. Dari ke-enam belas flip-flop tersebut delapan untuk data serial dan delapan untuk data paralel. Selain enam belas flip-flop juga terdapat delapan buah *tristate* yang jika diilustrasikan berfungsi sebagai saklar, yaitu apabila kontrol aktif, keluaran akan sama dengan masukan, sedangkan bila kontrol dalam kondisi tidak aktif, maka keluaran akan berada dalam kondisi *Hi-Z*. Rangkaian *internal* 74LS595 ditunjukkan dalam Gambar 2.24.



Gambar 2.24 Rangkaian *internal* IC 74LS595

Sumber : *National Semiconductor Data Sheets*, 1988:5

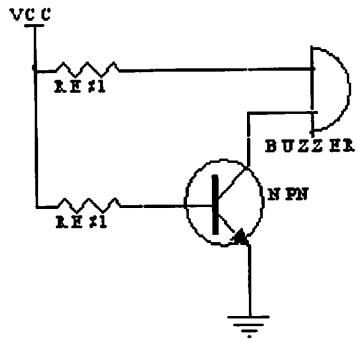
Fungsi dari masing-masing pin IC 74LS595 adalah :

- Pin SER (14) berfungsi sebagai masukan data secara serial.
- Pin SRCLK (11) berfungsi sebagai *clock* register geser serial.
- Pin SRCLR (10) berfungsi sebagai *clear* register geser serial.
- Pin RCLK (12) berfungsi sebagai *clock* bersama register *latch* .
- Pin E (13) berfungsi sebagai *enable tri state output* register geser
- Pin Q0 –Q7 dan Q'7 (1 - 7 ,9,15) berfungsi sebagai keluaran *register latch.*

2.10 Rangkaian *Buzzer*

Perangkat *Buzzer* digunakan untuk menghasilkan bunyi atau sinyal sirine merupakan komponen resonator *piezoelectric* yang digunakan untuk mengadakan isyarat terdengar sebagai alarm. *Buzzer* akan aktif dengan cara mengeluarkan sinyal suara (berbunyi) dengan lama waktu sesuai dengan perencanaan nanti.

Apabila penunjukan waktu sesuai dengan jadual agenda maka rangkaian *driver Buzzer* akan mengaktifkan *buzzer* selama waktu yang diinginkan. Gambar 2.25 menunjukkan rangkaian *driver buzzer.*



Gambar 2.25Rangkaian *Driver Buzzer*

Sumber: 303 Rangkaian Elektronika, 1997 : 278

BAB III

PERANCANGAN DAN PEMBUATAN ALAT

3.1 Pendahuluan

Pada bab ini akan dibahas mengenai peralatan yang direncanakan dan akan direalisasikan sebagaimana fungsinya. Adapun perencanaan dan pembuatan alat secara garis besar terdapat 2 (dua) bagian perangkat yang ada yaitui:

- Perencanaan dan pembuatan perangkat keras (Hardware)

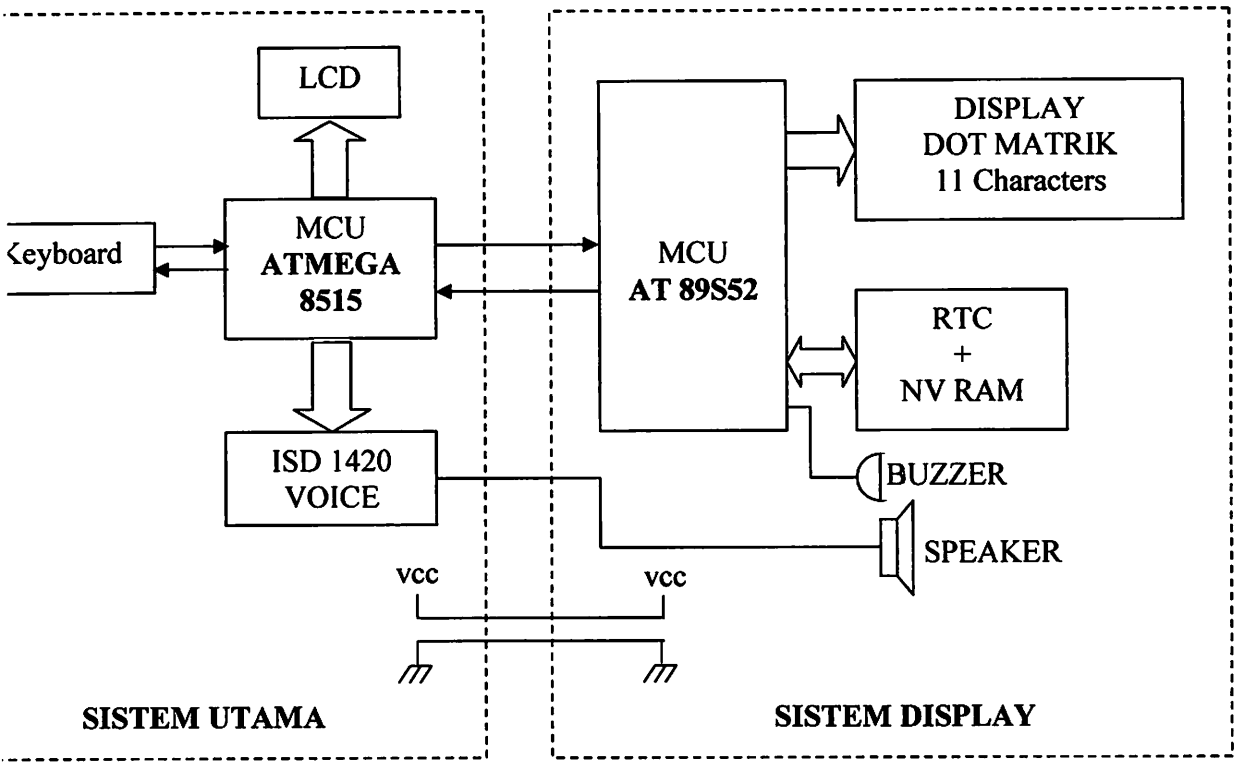
  Terdiri dari 2 sistem, yaitu sistem utama yang terdiri dari : mikrokontroler ATmega8515, ISD *Voice* 1420, LCD, *Keyboard*. Sedangkan untuk sistem display terdiri dari : Mikrokontroler AT89S52, RTC + NVRAM, Dot Matrik, *driver* LED, register geser, *Buzzer*.

- Perencanaan dan pembuatan perangkat lunak (Software)

Pada perencanaan perangkat keras akan meliputi seluruh periperal yang digunakan pada sistem ini. Pada perencanaan perangkat lunak akan meliputi *flowchart* dan *software* secara umum. Akan tetapi kedua perangkat tersebut dalam kerjanya akan saling menunjang satu sama lain.

3.2 Perencanaan Blok Diagram

Secara garis besar, prinsip kerja dari Agenda Elektronik dengan tampilan Dot Matrik dapat dijelaskan melalui diagram blok seperti berikut ini :



Gambar 3.1

Diagram Blok Keseluruhan Sistem

Dari gambar blok diagram diatas, maka dapat dilihat penjelasan dari tiap blok rangkaian Agenda Elektronik dengan tampilan Dot Matrik adalah sebagai berikut :

- **Mikrokontroler ATmega8515**

  Mikrokontroler ATmega8515 pada alat ini merupakan komponen utama karena mikrokontroler inilah yang akan mengontrol keseluruhan sistem pada alat ini.

- ***Keyboard***

  Sebagai piranti masukan (*input*) baik itu data ataupun perintah berasal dari perangkat *keyboard* PC yang dihubungkan langsung dengan ATmega8515 dengan jenis komunikasi serial asinkron.

- **Rangkaian Indikasi Suara (ISD *Voice* 1420)**

  Rangkaian ini merupakan media penyimpanan suara. Pada saat IC ini tidak ada catu daya tetapi data suara yang tersimpan didalamnya tidak akan hilang Rangkaiaan ini sudah terintegrasi didalam modul yang terdiri dari *mic*, gerbang *address* data, rangkaian penguat, serta output speaker.

- **LCD (*Liquid Cristal Display*)**

  Disini LCD berfungsi sebagai penampil menu dan agenda sebelum dikirim ke display Dot Matrik.

- **RTC (*Real Time Clock*) IC DS1642**

  Rangkaian RTC dan RAM dengan tipe *Non Volatile (NV)* produksi *Dallas Semiconductor* teintegrasi keduanya dalam satu komponen IC RTC NVRAM. RTC ini merupakan basis pewaktu yang digunakan untuk menentukan jadwal dan sistem informasi. *Real Time Clock* (RTC) terdiri dari register tahun, bulan, tanggal, hari, jam, menit dan detik. Koreksi tiap register tersebut dirancang secara otomatis dan dapat dipertahankan akurasinya sampai 100 tahun.

- **Rangkaian *Buzzer***

  Rangkaian *Driver Buzzer* digunakan untuk menggerakkan *Buzzer* merupakan komponen resonator *piezoelectric* yang digunakan untuk mengadakan isyarat terdengar sebagai alarm. *Buzzer* akan aktif dengan cara mengeluarkan sinyal suara (berbunyi) selama satu menit sesuai dengan perencanaan. Apabila penunjukan waktu sesuai dengan jadual agenda maka rangkaian *driver buzzer* akan mengaktifkan *buzzer* selama waktu yang diinginkan.

- **Tampilan**

  Pada perancangan digunakan dot matrik sebagai display. Dot matrik yang digunakan adalah modul dot matrik 5x7 akan digunakan untuk dapat menampilkan informasi. LED sebagai dot matrik menjadi media tampilan dari informasi yang akan ditampilkan. Dot matrik dengan ukuran 5x7 (tujuh baris dan lima kolom) yang tersusun dari sejumlah LED dirangkai sedemikian rupa.

3.3 Prinsip Kerja Alat

Diawali dengan pengisian agenda sesuai dengan yang akan ditampilkan, menggunakan keyboard. Kemudian data akan terkirim ke minimum sistem dan akan ditampilkan melalui *LCD*, dari sini kita bisa mengecek apakah agenda yang digunakan sudah benar atau belum. Kemudian kita mengeset waktu yang meliputi hari, tanggal, bulan, tahun, jam, menit, detik. Kegunaan dari pengesetan tersebut untuk menentukan kapan agenda tersebut akan ditampilkan. Setelah menentukan waktu dan jenis agenda kemudian data disimpan didalam ATmega8515, apabila ada kesalahan data yang sudah tersimpan data dapat diedit kembali dan juga dapat dihapus. Apabila agenda yang diset sudah sama dengan yang diinginkan maka ditekan tombol pada keyboard untuk mengirimkan data ke sistem display. Ketika waktu pada RTC sama dengan waktu pada agenda yang deprogram maka *buzzer* akan berbunyi, menandakan adanya agenda yang sedang aktif dan jenis kegiatan yang telah diprogram dapat dilihat pada tampilan yang berupa Dot Matrik.

3.4 Perancangan Perangkat Keras (*hardware*)

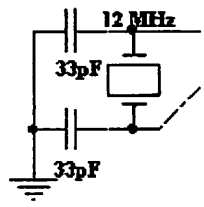
Dalam Tugas Akhir ini, perancangan agenda elektronik menggunakan Mikrokontroller Atmega8515 sebagai pengontrol utama, dan menggunakan dot matrik sebagai displaynya, serta komponen lain sebagai komponen pendukungnya.

3.4.1 Perencanaan Rangkaian Mikrokontroler Atmega8515

3.4.1.1 Perencanaan Rangkaian Clock

Mikrokontroller Atmega8515 memiliki internal *clock* pada pin 19 (X1) dan pin 18 (X2) yang berfungsi sebagai sumber *clock*, dan diperlukan rangkaian tambahan untuk membangkitkan *clock* tersebut.

Dalam sistem ini digunakan 2 (dua) buah kapasitor sebesar 33 pF dan kristal 12 MHz, dan gambar rangkaian *clock* dapat dilihat pada gambar 3.2 dibawah ini:

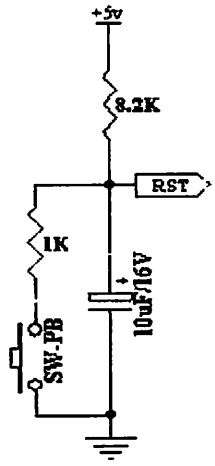


Gambar 3.2

Perencanaan Rangkaian *Clock* Atmega8515

3.4.1.2 Perencanaan Rangkaian Reset

Untuk melakukan reset sistem pada mikrokontroller dapat memanfaatkan pin reset. Pin tersebut dihubungkan dengan rangkaian reset eksternal yang ditunjukkan dibawah ini:



Gambar 3.3

Rangkaian Reset Eksternal

Selain menggunakan rangkaian reset eksternal, pe-reset-an pada MCU ATmega8515 juga dapat dilakukan dengan internal reset yang terdiri dari tiga macam cara yaitu :

- Power-On reset

  Mikrokonttroller akan dalam keadaan reset jika tegangan power supply berada dibawah tegangan ambang Power-on reset.

- *Watchdog* reset

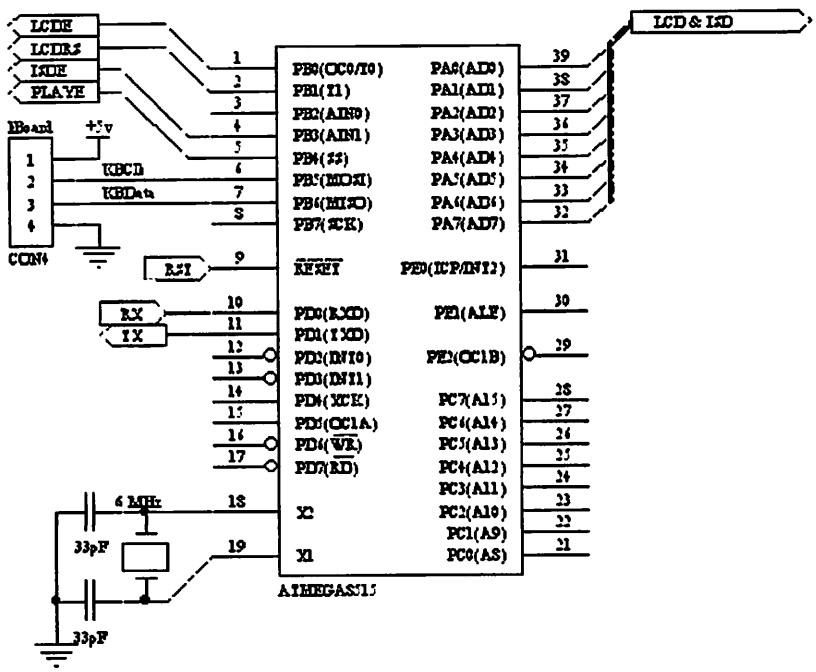
  Mikrokonttroler dalam keadaan mereset jika periode *Watchdog timer* berakhir dan *Watchdog* dalam kondisi *enable.*

- Brown-out reset

  Mikrokonttroler akan dalam keadaan reset jika tegangan *power supply* berada dibawah tegangan ambang *Brownout reset* dan detector *Brown-out* dalam kondisi *enable.*

3.4.1.3 Sistem Minimum ATmega8515

Pada rangkaian ini komponen utamanya adalah unit mikrokontroler ATmega8515L. Komponen ini merupakan sebuah *chip* tunggal sebagai pengolah data dan pengontrolan alat. Sebagai pengolah data dan pengontrolan sistem, pin-pin mikrokontroler ATmega8515L dihubungkan pada rangkaian pendukung membentuk suatu *minimum* sistem, yang ditunjukkan pada gambar berikut:

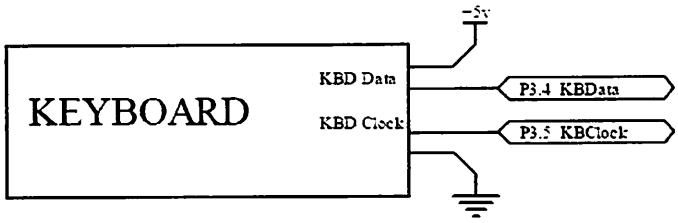


Gambar 3-4

Rangkaian Mikrokontroler ATmega8515L

3.4.2 *Keyboard* PC

Sebagai piranti masukan (*input*) baik itu data maupun perintah yang berasal dari perangkat *keyboard* PC (IBM *standart 102 key*) yang dihubungkan langsung dengan ATmega8515 (MCU 1) *dengan* jenis komunikasi serial *asinkron.* Dalam perencanaan antarmuka *keyboard* dihubungkan dengan P3.4 dan P3.5 dijelaskan dalam gambar 3.5.

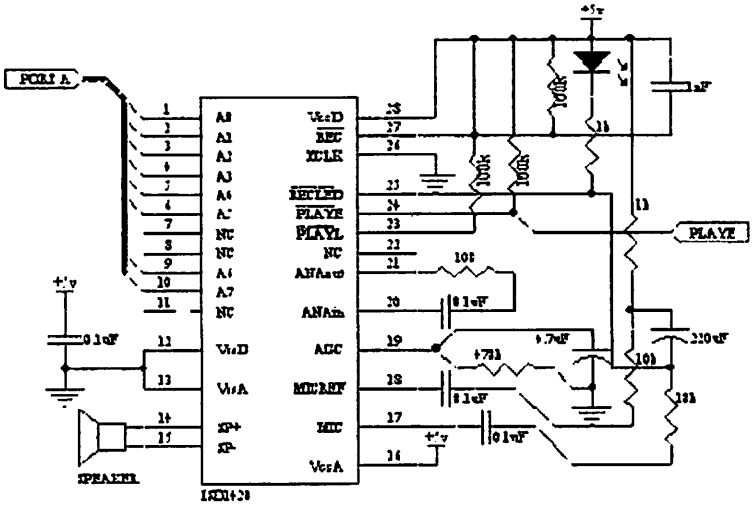


Gambar 3.5

Antarmuka *keyboard* dengan mikrokontroler

3.4.3 Antarmuka ISD 1420

Peralatan penyimpan informasi suara, ISD 1420 mempunyai kualitasyang bagus dengan durasi penyimpanan 20 detik. Ragkaian dapat dilihat pada gambar 3.6.



Gambar 3.6

Rangkaian ISD 1420

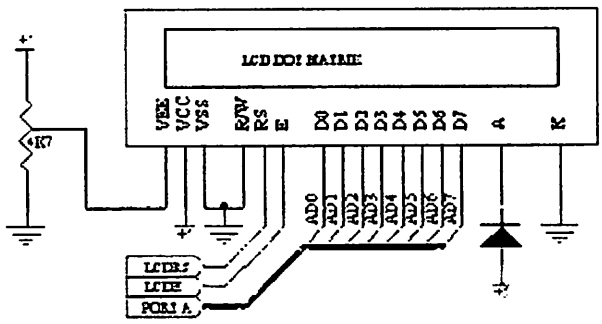
Peralatan *CMOS* yang ada didalamnya adalah *chip* osilator, *microphone preamplifier, automatic gain control, antialising filter, smouthing filter,* dan *speaker amplifier.* ISD 1420 kompatibel dengan mikrokontrler. Alamat dan jalur kendali dapat dihubungkan dengan mikrokontroler, sehingga mengijinkan penyimpanan dan

pengalamatan yang komplek. Perekaman disimpan dalam satu *chip* yang tidak mudah berubah dalam *cell* memori. Sinyal suara audio disimpan secara langsung ke memory pada tempat naturalnya dengan kualitas suara yang bagus.

3.4.4 Antarmuka LCD (*Liquid Cristal Display*)

Sebelum agenda ditampilkan pada *display* dot matrik, agenda akan ditampilkan dulu pada LCD yang terdapat pada modul utama, fungsinya untuk mengecek apakah data yang diisikan sudah benar. Pada LCD menggunakan jenis dot matrik tipe M 1632. LCD M 1632 dihubungkan dengan data bus mikro.

Dengan bantuan perangkat lunak yang dibuat, dapat ditampilkan karakter yang bisa dilihat pada layar tampilan, yaitu dengan mengendalikan pada pena E, R/W dan RS. Gambar dari rangkaian LCD M 1632, diperlihatkan pada gambar 3.7.

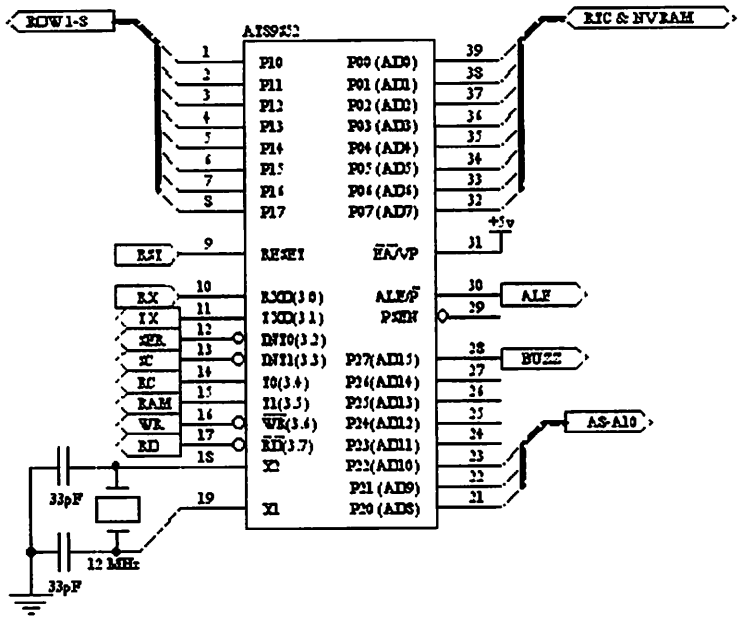


Gambar 3.7
Antarmuka LCD (*Liquid Cristal Display*)

3.4.5 Perancangan Mikrokontroler AT89S52

Komponen utama dari modul *display* adalah sebuah mikrokontroler AT89S52. Komponen ini merupakan *chip* tunggal dengan fasilitas RAM dan ROM *internal*. Dipilihnya AT89S52 karena produk ini kompatibel engan MCS-51 baik karakteristik dan pemrogramannya serta mudah didapatkan dipasaran dengan harga yang terjangkau. Seri

AT89S52 memiliki *internal* RAM yang cukup untuk mengolah data ingin ditampilkan dengan kapasitas *internal* RAM sebesar 256 byte. Dalam gambar 3.8 dijelaskan hubungan pin-pin AT89S52 dengan rangkaian pendukung dalam modul *display*.



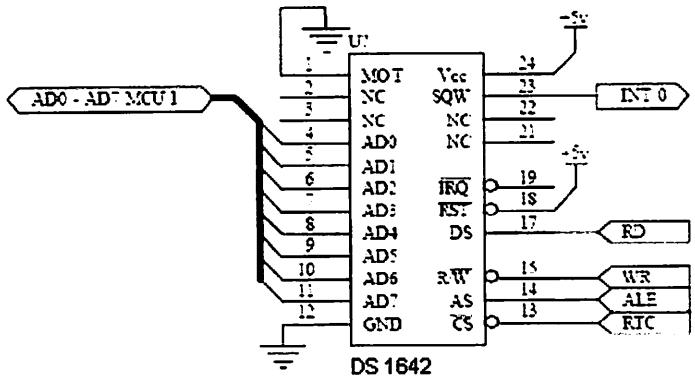
Gambar 3.8

Antarmuka AT89S52 dalam Modul *Display*

Port 1 dalam gambar 3.8 tersebut digunakan sebagai port untuk menampilkan data dalam dot matrik untuk satu kolom dan tujuh baris. Port tersebut akan dihubungkan dengan rangkaian transistor sebagai *driver* untuk memenuhi kebutuhan arus dot matrik. Sedangkan P2.0, p2.1 dan p2.2 sebagai port untuk *scanning* kolom dot matrik yang akan dihubungkan dengan *driver* kolom berupa komponen 74HC595. Port serial (RX dan TX) dihubungkan dengan MCU 1 dalam modul utama sebagai jalur komunikasi serial XTAL1 dan XTAL2 dihubungkan dengan rangkaian osilator, rangkaian ini terdiri dari kristal osilator 12 MHz dirangkai dengan dua buah kapasitor 33pF.

3.4.6 Antarmuka RTC dan NVRAM

Komponen RTC (*Real Time Clock*) dan NVRAM (*Non Volatile Random Access Memory*) produksi dari *DALLAS Semiconductor* dengan seri DS1642, terintegrasi keduanya dalam satu komponen IC RTC NVRAM. Komponen ini tidak memerlukan rangkaian eksternal seperti resistor, kapasitor dan rangkaian osilator, karena didalam IC ini sudah terintegrasi didalamnya. Komponen ini kompatibel dengan mikrokontroler jenis MCS-51 sehingga tidak memerlukan lagi komponen pendukung lain misalnya resistor *pull-up* ataupun *shift register latches*. Antarmuka RTC+NVRAM dengan sistem mikrokontroler AT89S52 (dalam modul *display*) ditunjukkan dalam gambar 3.9



Gambar 3.9

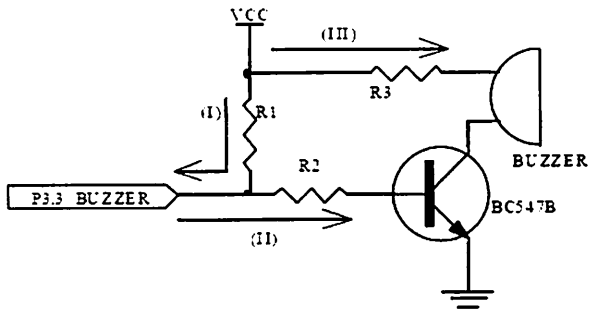
Antarmuka RTC+NVRAM dengan AT89S52

Untuk antarmuka, pin MOT RTC dihubungkan ke GND. Bus data RTC dihubungkan ke bus data sistem mikrokontroler AT89S52, sedangkan bus control R/W RTC dihubungkan ke pin WR mikrokontroler AT89S52, pin DS RTC dihubungkan ke pin RD mikrokontroler AT8S52, dan pin AS RTC dihubungkan ke pin ALE mikrokontroler AT89S52. *Chip select* (CS) RTC dihubungkan dengan P1.6 AT89S52 sebagai bit seleksi komponen, sehingga untuk menyeleksi komponen RTC harus

mengaktifkan juga P1.6. Pin SWQ dari RTC akan memberikan interupsi pada mikrokontroler sebagai tanda *update time* dari waktu yang diprosesnya.

3.4.7 Antarmuka *Buzzer*

Dalam perencanaan rangkaian ini port 3.3 dari AT89S52 akan langsung dihubungkan dengan rangkaian *buzzer*. Metode yang digunakan untuk *buzzer* aktif ialah dengan memberikan logika "1" pada port 3.3 dan logika "0" pada port 3.3 akan menjadikan *buzzer* tidak aktif. Dua keadaan logika tersebut dikontrol melalui *software*. Dalam gambar 3. dijelaskan bahwa keluaran dari P3.3 diberi resistor *pull-up* R1. Alasan diberi resistor *pull- up* R1 karena arus keluaran port 3.3 pada saat logika "1" sebagai Ib belum cukup untuk membangkitkan Ic yang direncanakan, sehingga diperlukan R *pull-up* untuk menambah arus R1. Rangkaian tersebut terdiri dari sebuah transistor NPN tipe BC547B yang dirangkai dengan tiga buah resistor, R1 adalah resistor *pull-up*.



Gambar 3.10

Antarmuka rangkaian *buzzer* dengan mikrokontroler

Transistor NPN BC574 dengan spesifikasi Vce(max) 45 V, Ic(max) 100mA dengan hfe min. = 200, direncanakan Ic yang diinginkan adalah 80 mA. Sedang buzzer yang digunakan adalah modul buzzer tipe aktif dengan tegangan kerja minimal +3 volt

sehingga langsung dihubungkan pada transistor sebagai driver. Dengan spesifikasi tersebut diatas maka dapat dihitunng untuk mendapatkan nilai R3. Analisisnya sebagai berikut :

$Vcc = +5V$

$\beta = 200$

$V_{CE} = 0{,}4\ V$

$V_{BE} = 0{,}7\ V$

$V_{BUZZER} = 3V$

$I_C = I_{BUZZER} = 80\ mA$

$$\beta = \frac{Ic}{Ib} \quad \text{.....(3.1)}$$

$$200 = \frac{80m}{Ib}$$

$Ib = 0{,}4\ mA$

$Vcc - Ic\ .\ R3 - V_{BUZZER} - V_{CE} = 0$

$5 - 80\ mA\ .\ R_3 - 3 - 0{,}4 = 0$

$$R_3 = \frac{1{,}6}{80.10^{-3}} = 20\ \Omega$$

Analisis rangkaian dalam Gambar 3.10 dalam kondisi logika "0" mikrokontroler untuk port 3 adalah sebagai berikut :

Untuk kondisi logika low pada loop 1 adalah :

Diketahui : $V_{OL} = 0{,}45\ V$ (max)

$I_{OL} = 1{,}6\ mA$ (max)

$V_{CC} = 5V$

$V_{CC} - I_{I}.R_{I} - V_{OL} = 0$ dimana ($I_I = I_{OL}$).....(3.2)

$5\ V - 1{,}6\ mA\ .\ R_I - 0{,}45\ V = 0$

$4{,}55 = 1{,}6\ m\ .\ R_I$

$R_I = 2{,}843{,}75\ \Omega$

Nilai minimum resistor pembatas arus yang ditunjukkan untuk kondisi *low* adalah 2843,75 Ω. Dalam perancangan ini digunakan resistor untuk R1 sebesar 10 kΩ sehingga tidak akan menimbulkan masalah bagi port 3.3 karena nilai arus yang akan dilewatkan dibawah nilai maksimum yang dijalankan.

Pada saat P3.3 berlogika "0" maka transistor akan *reverse* bias oleh P3.3, sehingga transistor tidak bekrja. Pada saat logika "1" P3.3 akan membias maju transistor dikarenakan oleh Voh sehingga akan ada arus I2 dan diperlukan R2 sebagai pembatas arus I2. Analisisnya sebagai berikut :

Dari persamaan 3.1 diperoleh Ib = 0,4 mA dan Gambar 3.10 dijelaskan sebagai I2. Ketika logika "1" terjadi pada P3.3 maka akan timbul Voh minimal 2,4 V sehingga bias didapatkan nilai R2, analisisnya sebagai berikut :

$V_{OH} - I_2\ .\ R_2 - V_{BE} = 0$ ($I_2 = Ib$) .....(3.3)

$2{,}4 - 0{,}4\ .10^{-3}\ .\ R_2 - 0{,}7 = 0$

$1{,}7 = 0{,}4\ .10^{-3}\ .\ R_2$

$R_2 = 4250\ \Omega$

Dalam perencanaan digunakan resistor R2 sebesar 8 kΩ, sehingga dengan menggunakan persamaan 3.3 akan didapatkan I2 pada kondisi Voh (min) adalah sebesar 0,21 mA dan dengan persamaan 4.1 dapat dihitung penguatan arus yang terjadi pada Ic ketika dalam kondisi Voh minimal dan dalam kondisi *hfe* minimal sebesar 42 mA.

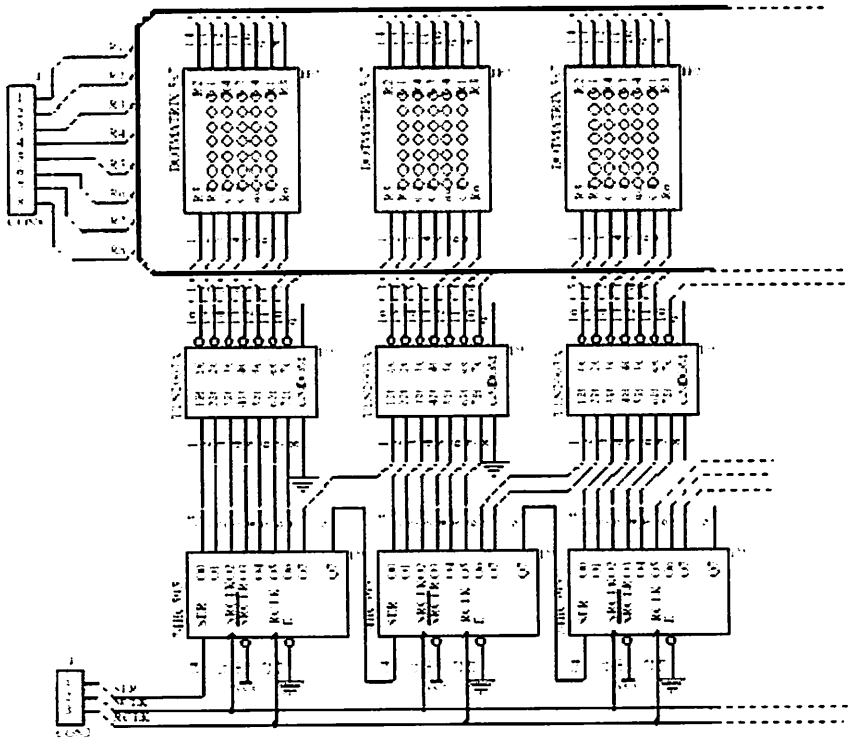
$I_C = \beta\ Ib$

$Ic = 200.\ 0{,}21.\ 10^{-3}$

$Ic = 42\ mA$

3.4.8 Rangkaian Driver Dot Matrik

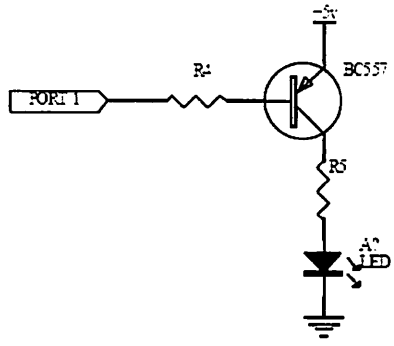
Dot matrik 5x7 (5 kolom dan 7 baris) tersusun dari 35 buah LED yang dirangkai dalam 5 kolom dan 7 baris. *Driver* setiap baris dot matrik dihubungkan dengan port 1 dari MCU modul *display*. Sedangkan kutub katoda dari LED akan dihubungkan dengan port dari ULN2003 yang dirangkai dengan *driver scan* kolom 74HC595. Rangkaian *display* dot matrik dapat dijelaskan dalam gambar 3.11.



Gambar 3.11

Rangkaian *display* Dot Matrik

Setiap port dalam P1 akan menangani satu baris dot matrik, dank arena sistem *scan* yang digunakan adalah *scanning* kolom, maka setiap port 1 hanya akan mendriver satu LED pada setiap barisnya, sedangkan arus untuk mengaktifkan sebuah LED dot matrik berdasarkan *datasheet* sebesar 30 mA. Apabila dot matrik dioperasikan dalam keadan 1/10 *duty cycle*, dapat dialirkan arus maksimal seesar 100mA dan dalam perencanaan alat *duty cycle* lebih kecil dari nilai tersebut. Gambar 3.12 menjelaskan analisa gambar port yang men*driver* tiap LED dot matrik.



Gambar 3.12

***Driver* Setiap Baris Dot Matrik**

Dari gambar 3.12 kondisi *low* dalam port 1 akan mengaktifkan rangkaian *driver* dot matrik tersebut. Kondisi tersebut akan berkaitan dengan karakteristik port MCU ketika logika *low*, yaitu : Iol (max) = 1,6 mA. Vol (max)= 0,45 V.

Arus yang diberikan ke dot matrik (Ic) sebesar 60 mA dengan tegangan bias 4 V. Dapat diperoleh nilai R5 (Rc) dari persamaan 3.4 dengan Vce = 0,4 V sebagai berikut :

$$R_5 = \frac{V_{EE} - (V_{EC} + V_{LED})}{I_{LED}} \quad \text{.....(3.4)}$$

$$R_5 = \frac{5 - (0{,}4 + 4)}{60x10^{-3}} = 10\Omega$$

Nilai minimum resistor R4 dapat diketahui dari persamaan3.5

$$R_4 = \frac{V_{EE} - (V_{EB} + V_{OL})}{I_{OL}} \qquad \text{.....(3.5)}$$

$$R_4 = \frac{5 - (0{,}7 + 0{,}45)}{1{,}6x10^{-3}} = 2406{,}25\ \Omega$$

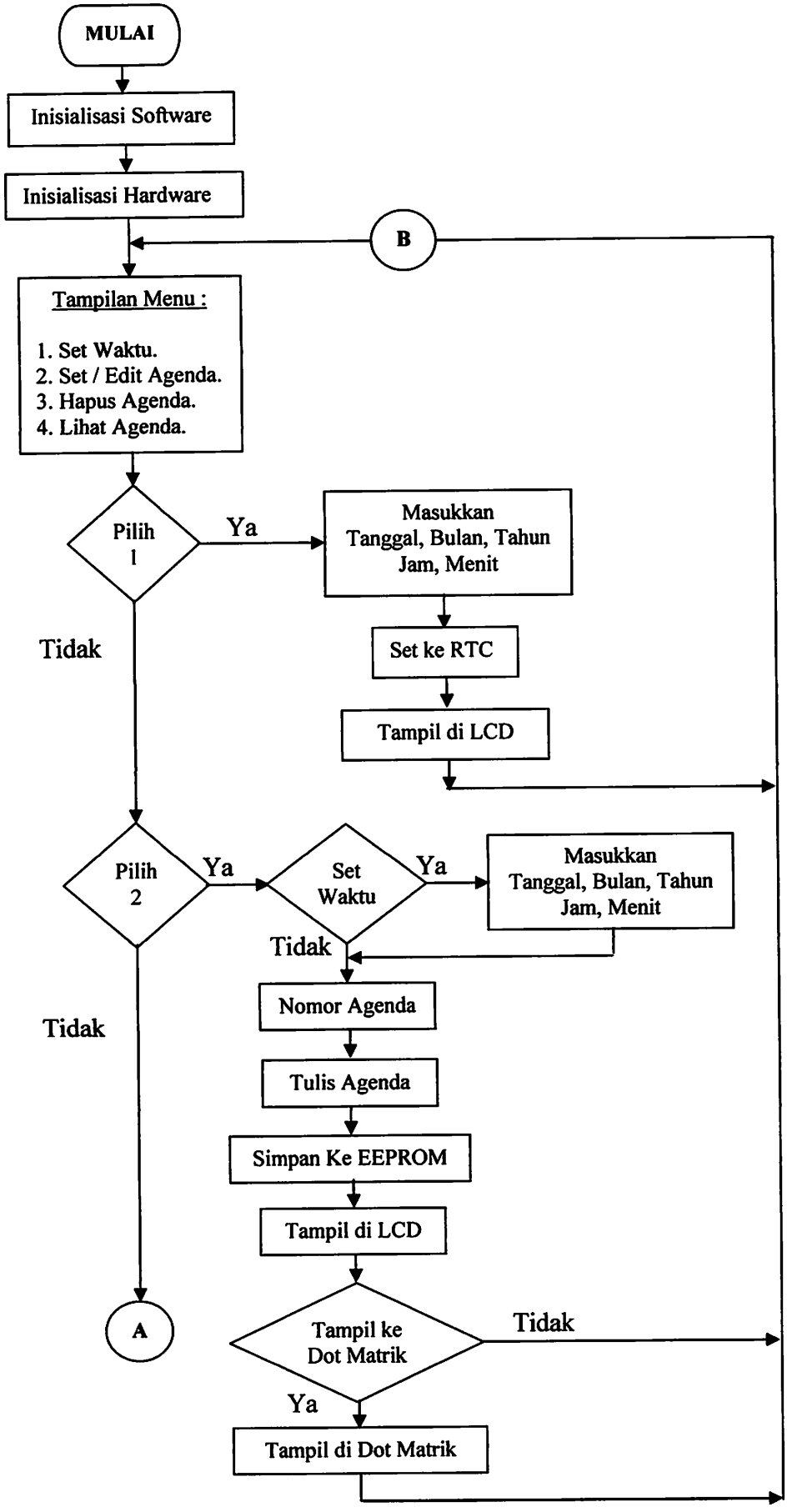
Digunakan resistor 12 kΩ untuk R4, dengan nilai tersebut arus Ib (Iol) dapat dihitung kembali. Dari persamaan 4.5 duperoleh arus sebesar 0,32 mA, tidak melebihi arus maksimal Iol. Dengan menggunakan persamaan 4.1 dpat diperoleh Ic baru sebesar 64 mA.

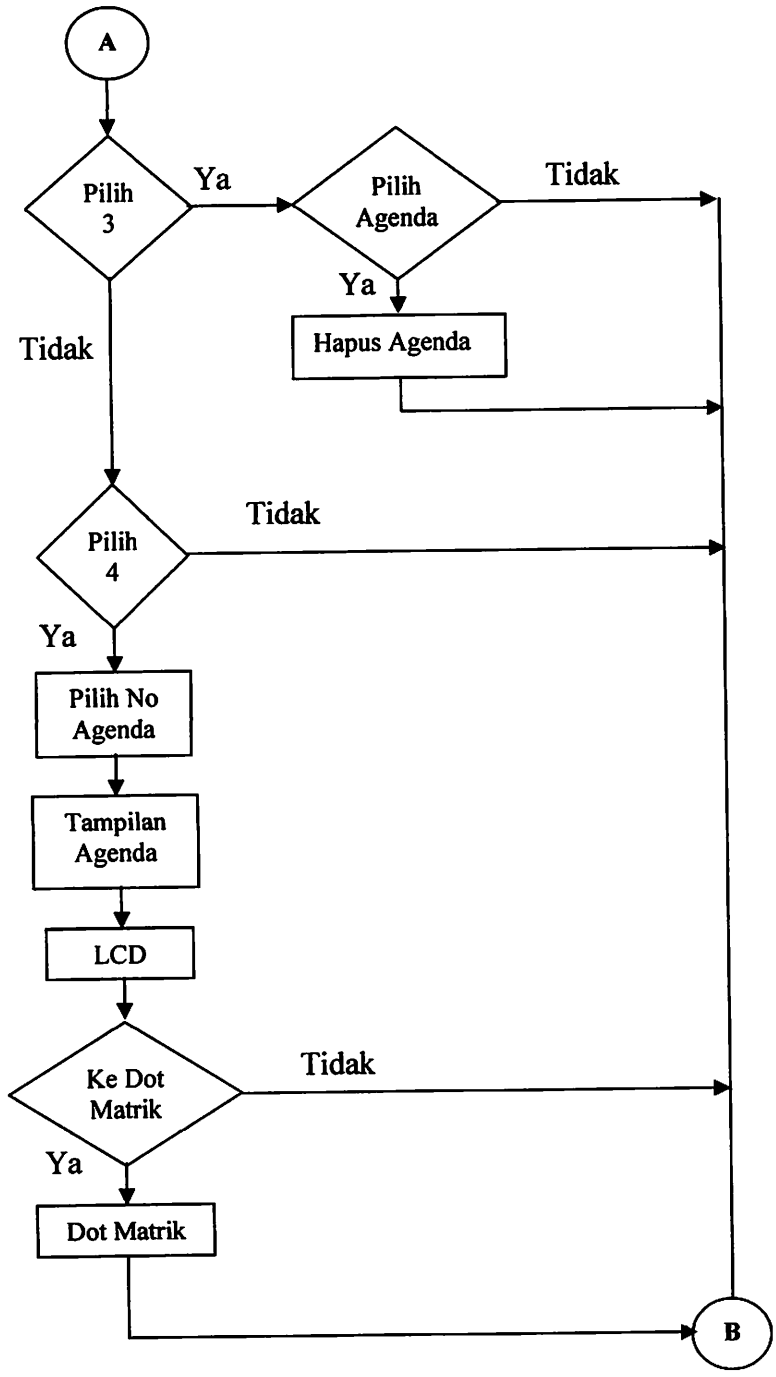
3.5 Perencanaan Perangkat Lunak (*software*)

Perencanaan perangkat lunak ini didasarkan pada perencanaan perangkat keras yang telah dibuat seelumnya untuk mendapatkan sistem kerja yang diharapkan. Terdapat dua modul rangakaian yaitu modul utama (MCU 1) dengan pengendali utama mikrokontroler ATmega8515L dan modul *display* (MCU 2) dengan mikrokontroler AT89S52. Pembuatan perangkat lunak sistem aplikasi berdasarkan pada semua kejadian yang harus dikerjakan perangkat keras.

Untuk mikrokontroller ATmega8515L bahasa yang digunakan adalah bahasa pemrograman *assembler* milik AVR RISC. Pembuatan perangkat lunak harus melalui proses-proses uji coba secara *software* maupun secara *hardware*.

Secara garis besar, sistem kerja dari perangkat lunak dapat dilihat pada diagram alir seperti Gambar 3.13 di bawah ini:


MULAI
Inisialisasi Software
Inisialisasi Hardware
B
Tampilan Menu :
1. Set Waktu.
2. Set / Edit Agenda.
3. Hapus Agenda.
4. Lihat Agenda.
Pilih 1
Ya
Masukkan Tanggal, Bulan, Tahun Jam, Menit
Set ke RTC
Tampil di LCD
Tidak
Pilih 2
Ya
Set Waktu
Ya
Masukkan Tanggal, Bulan, Tahun Jam, Menit
Tidak
Nomor Agenda
Tulis Agenda
Simpan Ke EEPROM
Tampil di LCD
Tidak
A
Tampil ke Dot Matrik
Tidak
Ya
Tampil di Dot Matrik



Gambar 3.13

Perangkat Lunak Sistem Utama dan Sistem Display

BAB IV

PENGUJIAN ALAT

Setelah merancang keseluruhan sistem, selanjutnya dilakukan pengujian untuk mengetahui unjuk kerja masing-masing sistem. Dilakukan pengujian terhadap masing-masing sistem. Selanjutnya seluruh sistem tersebut digabungkan membentuk suatu sistem agenda elektronik dengan tampilan dot matrik dan dilakukan pengujian secara keseluruhan. Pengujian yang dilakukan terhadap masing-masing sistem secara keseluruhan.

Bagian yang diuji adalah :

1. Rangkaian minimum sistem (antarmuka *keyboard*).
2. Rangkaian pada sistem utama dengan mikrokontroler ATmega8515.
3. Rangkaian display dot matrik dengan mikrokontroler AT89S52.

Setelah semua bagian diatas diuji, langkah berikutnya adalah pengujian sistem secara keseluruhan. Dalam setiap pengujian dijelaskan tujuan pengujian, alat-alat yang digunakan, langkah-langkah yang dilakukan, serta analisis hasil pengujian.

4.1 Pengujian minimum sistem ATmega 8515 Modul Utama

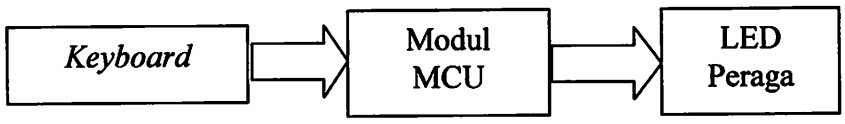
4.1.1 Tujuan

Tujuan pengujian ini adalah untuk mengetahui apakah sistem minimum modul utama yang dihubungkan dengan *keyboard* dapat bekerja sesuai dengan data yang diberikan.

4.1.2 Peralatan yang digunakan

1. Seperangkat kompuer.
2. Modul *programmer writer*.
3. Modul minimum sistem.
4. LED peraga.
5. *Keyboard* PC.
6. Catu daya 5 volt.

Blok diagram pengujian minimum sistem yang meliputi pengujian *keyboard* ditunjukkan dalam gambar 4.1.



Gambar 4.1

Pengujian MCU ATmega8515 dengan antarmuka *keyboard*

4.1.3 Prosedur pengujian

1. Merangkai peralatan seperti gambar 5.1.
2. Membuat program masukan data *keyboard* dalam modul utama, kemudian data tersebut dikonversi oleh program menjadi kode ASCII untuk dikirimkan oleh mikrokontroler melalui port 0 menuju modul LED peraga. Dalam modul utama membaca scan code dari *keyboard* untuk ditampilkan dalam modul LED peraga.
3. Mengaktifkan catu daya.

4. Melakukan penekanan *keyboard.*
5. Mengamati keluaran LED peraga.

4.1.4 Program pembacaan *keyboard*

Program utama dalam pengambilan data dari *keyboard* akan mengambil *scan code* dari keyboard kemudian akan diubah menjadi kode ASCII. Proses merubah *scan code* menjadi SCII dilakukan dengan metode '*lookup table*' dalam prosedur program jdASCII.

```
;---------------Merubah Scancode jadi ASCII dengan metode 'Lihat Tabel'.
jdASCII :  push dpl
           push dph
           mov dptr, #Scan code
           movc a, @a+dptr
           pop dph
           pop dpl
           ret
;--------------Interface KEYBOARD
           KBDclock     bit p  3.5
           KBDdata      bit p  3.4
AmbilBit : jnb KBDclock,s          ;
           jb  KBDclock,s          ;
           mov c, KBDdata          ;
           ret
AmbilByte : acall AmbilBit
            jb  AmbilByte
            mov r7, #08h
AmbilLagi : acall AmbilBit         ;
            Rrc a                  ;
```

```
            Djnz r7, AmbilLagi      ;
            Mov r7, a               ;
            Mov c,p                 ;
            Clr a                   ;
            Mov acc.0,c             ;
            Acall AmbilBit          ;
            Mov acc.1,c             ;
            Mov c,p                 ;
            Jnc salah               ;
            Mov a,r7                ;
            Acall AmbilBit          ;
            Ret
;-------------TULIS procedure
Tulis :     lcall AmbilByte
            Lcall JdASCII
            Mov P0,a
            Ljmp tulis
```

4.1.5 Hasil pengujian

Hasil eksekusi program modul utama dapat dilihat pada tabel 4.1.

TABEL 4.1 Hasil Eksekusi Program

Tombol	Data Keyboard (ScanCode)	Kode ASCII	Keluaran LED peraga
F1	05_H	$(C0_H)$ $1100\ 0000_b$	$1100\ 0000_b$
F2	06_H	$(C1_H)$ $1100\ 0001_b$	$1100\ 0001_b$
F3	04_H	$(C3_H)$ $1100\ 0011_b$	$1100\ 0011_b$
1	16_H	(31_H) $0011\ 0001_b$	$0011\ 0001_b$
2	$1E_H$	(32_H) $1100\ 0010_b$	$1100\ 0010_b$

3	26_H	(33_H) 0011 0011_b	0011 0011_b
A	$1C_H$	(41_H) 0100 0001_b	0100 0001_b
B	32_H	(42_H) 0100 0010_b	0100 0010_b
C	21_H	(43_H) 0100 0011_b	0100 0011_b

4.1.6 Analisis hasil pengujian

Dari hasil pengujian diketahui bahwa ketika ada penekanan tombol *keyboard*, sistem dalam *keyboard* akan mengirimkan data berupa *scan code* dari tombol yang ditekan ke modul MCU. Selanjutnya data *scan code* tersebut akan dikonversi oleh program MCU menjadi kode ASCII yang ditampilkan dalam port 0 berupa data biner. Dari tabel tersebut keluaran pada LED peraga sudah sesuai dengan kode ASCII dari tombol *keyboard* yang ditekan. Tidak terjadi kesalahan konversi dari scan code ke ASCII. Hal in menunjukan bahwa rangkaian dan program antarmuka *keyboard* dengan mikrokontroler bekerja sesuai dengan yang diharapkan.

4.2 Pengujian Rangkaian *Real Time Clock* (RTC)

4.2.1 Tujuan

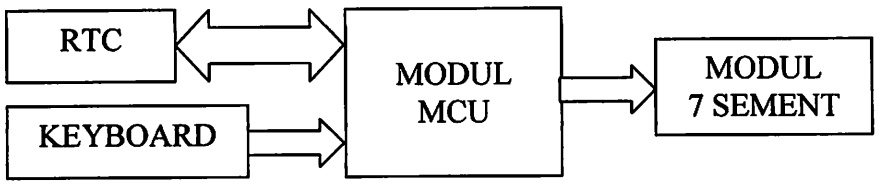
Tujuan pengujian rangkaian *real time clock* adalah untuk mengetahui apakah rangkaian ini dapat bekerja untuk menampilkan waktu. Perangkat lunak yang digunakan untuk menguji unjuk kerja rangkaian RTC adalah sebuah program akses data konfigurasi *setting* waktu dari RTC.

4.2.2 Peralatan yang digunakan

1. Modul Minimum Sistem AT89C51
2. Modul *Real Time Clock* (RTC)

3. Modul 7-segment
4. *Keyboard* IBM PC
5. Catu Daya 5 volt

Blok diagram pengujian *real time clock* ditunjukkan dalam Gambar 5.2



Gambar 4.2 Rangkaian Pengujian RTC 1642

4.2.3 Prosedur Pengujian

1. Merangkaia peralatan seperti dalam gambar 4.2.
2. Membuat perangkat lunak pengujian rangkaian *real time clock.* Program ini berisi inisialisasi *real time clock,* dan interupsi timer. Program kemudian mengirimkan data karakter berupa jam, menit dan detik ke modul 7-*segment.*
3. Mengisi program ke MCU dengan menggunakan *Programme Writer.*
4. Menjalankan program untuk prosedur waktu (RTC).

4.2.4 Program Utama Aplikasi RTC

Program utama aplikasi RTC dihubungkan dalam interupsi eksternal ROM MCU, sehingga leaknya berada dalam alamat ROM 03_H. Sebelum RTC diaktifkan, terlebih dahulu dilakukan inisialisasi untuk mengatur kerja dari RTC tersebut. Sinyal *Up-date* dari RTC dihubungkan dengan program *interrupt external* 0.

```
;-------------------------------------
;INISIALISASI & SET RTC
;-------------------------------------
SetRTC:         mov a,#80h
                mov dptr,#07F8h ;reg A Wr
                clr XRAM
                nop
                movx @dptr,a
                nop
                mov dptr,#07FFh
                mov a,#05h      ;thn
                nop
                movx @dptr,a
                nop
                mov dptr,#07FEh
                mov a,#09h      ;bln
                nop
                movx @dptr,a
                nop
                mov dptr,#07FDh
                mov a,#20h      ;tgl
                nop
                movx @dptr,a
                nop
                mov dptr,#07FCh
                mov a,#03h      ;day
                nop
                movx @dptr,a
                nop
                mov dptr,#07FBh
                mov a,#23h      ;hour
                nop
                movx @dptr,a
                nop
                mov dptr,#07FAh
                mov a,#08h      ;mnt
                nop
                movx @dptr,a
                nop
                mov dptr,#07F9h
                mov a,#40h      ;sec
                nop
                movx @dptr,a
                nop
                mov dptr,#07F8h
                mov a,#00h
                nop
                movx @dptr,a
                nop
                setb XRAM
                ret
```

4.2.5 Hasil Pengujian dan Analisis

Dari pengujian diperoleh hasil bahwa dalam modul *7-segment* trlihat informasi waktu berupa jam, menit, detik, tangal, bulan dan tahun, dengan tampilan detik yang berubah setiap detik. Dengan demikian rangkaian *real time clock* dapat berfungsi dan dapat diakses oleh perangkat lunak.

Setting waktu dilakukan dengan penakanan *keyboard* (F12) untuk perintah set waktu. Program untuk setting waktu dapat dilihat dalam lampiran program prosedur waktu.

4.3 Pengujian Rangkaian ISD 1420

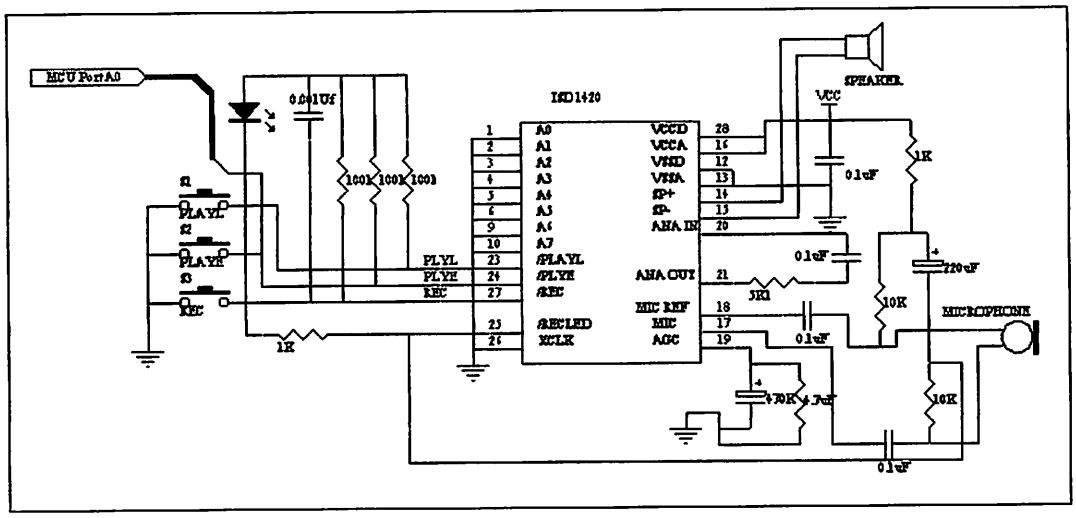
Tujuan dari pengujian rangkaian ISD tersebut adalah untuk mengetahui apakah *IC voice* dapat menyimpan suara yang teleh direkam.

4.3.1 Peralatan yang digunakan :

1. 1 buah *Mic* dan *Speaker*
2. Catu daya 5 volt DC
3. 1 buah ISD 1420

4.3.2 Prosedur pengujian:

Pasang rangkaian penyimpan suara seperti pada Gambar 4.4. Kemudian aktifkan rekam dan selanjutnya informasi suara dikeluarkan. Setelah beberapa detik, tekan tombol untuk menghentikan perekaman suara. Untuk memutar ulang suara yang telah direkam, tekan tombol play.



Gambar 4.3

Rangkaian ISD 1420

4.3.3 Hasil Pengujian:

Waktu (dalam detik)	Suara yang dikeluarkan
8	Informasi Agenda
3	Informasi

4.4 Pengujian Modul *Display* Dot Matrik

4.4.1 Tujuan

Untuk mengetahui apakah seluruh LED dot matrik dapat menyala sesuai data yang diberikan oleh mikrokontroler.

4.4.2 Peralatan yang Digunakan

1. Modul *display* dot matrik
2. Rangkaian *driver* kolom *display* dot matrik.

3. Modul minimum sistem AT89C51
4. Catu daya 5 volt.

Blok diagram pengujian display dot matrik ditunjukkan dalam gambar 4.3.

Gambar 4.4 Diagram Blok pengujian *display* dot matrik

4.4.3 Program Utama *Display* Dot Matrik

```
;-----------------------------------
; EQUATION
;-----------------------------------
                XREG   Equ 4000h

                SERr   bit P3.2
                SCLK   bit P3.3
                RCLK   bit P3.4
                XRAM   Bit P3.5
                Buzz   Bit P2.7
                roww   Equ P1

                DMenu  Equ 10h        ;01=Edit,02=Hapus,03=Baca,04=SetTime
                DNomerEqu 11h
                DTSet  Equ 12h        ;
                DBln   Equ 13h        ;BCD
                DTgl   Equ 14h        ;BCD
                DJam   Equ 15h        ;BCD
                Dmnt   Equ 16h
                Ddtk   Equ 17h
                Dthn   Equ 18h

                DBaca  Equ 20h
                DEdit  Equ 21h
                DHapus Equ 22h
                TeHaN  Equ 0ah
                TeElN  Equ 0fh


;-----------------------------------
; Vektor ROM
;-----------------------------------
                org 00h
                ljmp mulai
                org 0bh
                ljmp IntT0do
                org 23h
                ljmp Intser
```

```
                ljmp IntT0do

                org 23h
                ljmp Intser

;-----------------------------------
; INT Timer 0
;-----------------------------------
IntT0do: clr EA
                push Acc
                push 01h
                push PSW
                mov a,0bh
                cjne a,#76h,kanan2
                mov 0bh,#30h
kanan2:         mov TH0,TeHaN ;0FEH
                mov TL0,TeElN  ;60H

                mov roww,#0ffh
                inc 09h
                mov a,09h
                cjne a,#01h,kanan

                clr SERr
                clr SCLK
                ;nop
                setB SERr
                ;nop
                setB SCLK
                ;nop
                clr SERr
                clr Sclk
                CLR Rclk
                ;nop
                SETB Rclk

kanan4:         mov r1,0bh      ;rev
                mov a,@r1       ;rev
                mov roww,a      ;rev
                inc 0bh         ;rev
                pop PSW
                pop 01h
                pop Acc
                Setb EA
                reti

kanan:          cjne a,#46h,kanan3
                mov 09h,#00h
kanan3:         clr Sclk
                ;nop
                clr Rclk
                ;nop
                setb Sclk
                ;nop
                setb Rclk
```

```
;nop
clr Sclk
;nop
clr Rclk
ljmp kanan4
```

4.4.4 Prosedur Pengujian

1. Merangkai modul seperti dalam gambar 4.4
2. Membuat program tampilan dot matrik dan menulis data yang akan ditampilkan oleh dot matrik
3. Memasukan program tampilan dot matrik kedalam mikrokontroler
4. Mengaktifkan catu daya rangkaian
5. Mencatat tampilan dari dot matrik

4.4.5 Hasil Pengujian dan Analisis

Percobaan *display* dot matrik ini untuk menguji apakah seluruh LED dot matrik dan rangkaian transistor sebagai *driver* baris dot matrik bekerja dengan baik atau tidak. Rangkaian dot matrik disambungkan secara berurutan melalui *shift register* pada sisi kolomnya, sedangkan pada sisi baris dihubungkan dengan rangkaian *driver* kolom. Apabila logika 1 diberikan pada data baris dan logika 0 pada data kolom, maka LED dot matrik yang berada dalam baris dan kolom aktif tersebut akan menyala. Sebaliknya LED dot matrik akan padam pada semua kolom yang tidak aktif, sehingga sebenarnya hanya satu kolom saja yang aktif tiap periode *scan* kolomnya. Karena frekuensi *scan* kolom diatas 24 Hz, maka mata normal tidak bisa untuk mengikuti gerak *scan* tersebut sehingga seluruh kolom terlihat aktif semua. Hasil pengujian rangkaian modul MCU, modul *driver* dan modul dot matrik dapat bekerja sesuai dengan tujuan yang diharapkan.

4.5 Pengujian Secara Keseluruhan

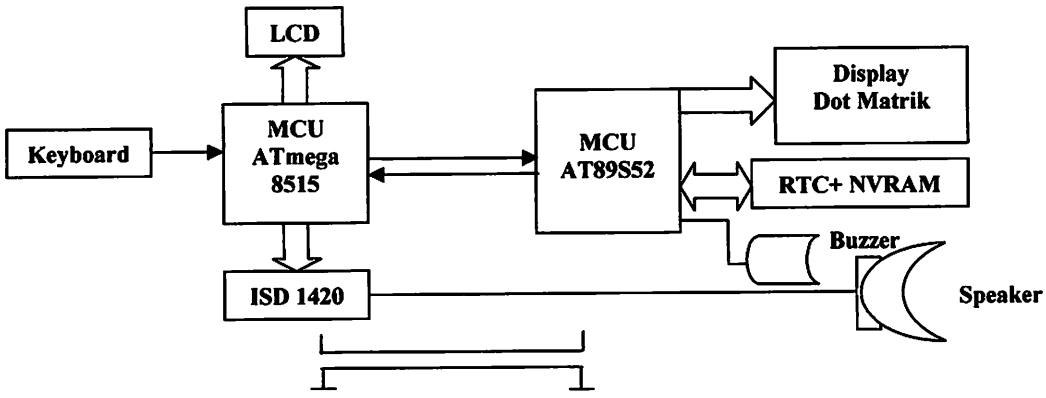
4.5.1 Tujuan

Pengujian keseluruhan sistem bertujuan untuk mengetahui kinerja sistem secara keseluruhan, apakah telah berhasil sesuai dengan spesifikasi yang diharapkan.

4.5.2 Peralatan yang Digunakan

1. Modul Utama (*keyboard*, LCD, ISD)
2. Modul *Display* (rangkaian *display* dot matrik)
3. Kabel penghubung serial
4. Sumber tegangan 5 volt

Blok diagram pengujian sistem keseluruhan ditunjukkan dalam gambar 4.5.



Gambar 4.5 Pengujian Keseluruhan Sistem

4.5.3 Program Utama

Program utama dalam tiap modul berbeda disesuaikan dengan aplikasinya. Untuk program lengkap dilampirkan dalam lampiran program. Bagian utama dari tiap *listing* program dari tiap modul sebagai berikut :

4.5.4 Prosedur Pengujian

1. Merangkai sistem seperti dalam gambar 4.5
2. Mengaktifkan catu daya
3. Mengirimkan perintah dan data melalui *keyboard* dan dikirim ke modul *display* dot matrik
4. Mengamati informasi yang ditampilkan

4.5.5 Hasil Pengujian dan Analisis

Hasil pengujian didapatkan data seperti yang ditunjukkan gambar 4.6.

Gambar 4.6 Hasil pengujian sistem keseluruhan

Setelah penakanan tombol perintah *keyboard* aktif ditekan (F1), selanjutnya program akan menunggu perintah berikutnya. Apabila tombol perintah 'tulis' ditekan (F3) maka modul utama akan mengirim kode pada modul *display* sebagai kode prosedur 'tulis' untuk diaktifkan. Selanjutnya modul utama akan mengirimdata sesuai penekanan tombol *keyboard* untuk dikirim ke modul *display*, kemudian modul *display* akan menampilkan data tersebut sampai ada perintah untuk mengakhiri prosedur 'tulis'.

Secara *up-to-date* modul utama akan mengirim data waktu (tanggal, bulan, tahun, jam, menit, detik) pada rangkaian display LCD yang berbasis pada sistem pewaktu RTC. Dari hasil pengujian dalam gambar 4.6 dapat dijelaskan bahwa sistem secara keseluruhan dapat bekerja dan data yang ditampilkan dalam dot matrik sesuai dengan data yang ditekan pada keyboard.

BAB V

PENUTUP

5.1 Kesimpulan

Dari hasil perancangan dan pengujian alat dapat diambil kesimpulan sebagai berikut :

1. Agenda Elektronik ini bisa menyimpan sampai 7 buah agenda, untuk satu agenda maksimum 200 karakter.
2. Dari hasil pengujian diperoleh data hasil penekanan *keyboard* berupa data *scan code* yang diproses oleh MCU, data ini dikonversi oleh program MCU menjadi kode ASCII yang ditampilkan dalam bentuk teks pada LCD. Untuk satu agenda bisa menampilkan maksimum 200 karakter.
3. Sistem pewaktu RTC (*Real Time Clock*) pada rangkaian display mampu menampilkan data berupa waktu dengan format tanggal / bulan / tahun dan jam : menit : detik pada rangkaian display LCD dot matrik.
4. IC ISD 1420 dapat menyimpan suara dengan durasi maksimal 20 detik.

5.2 Saran

Ada beberapa hal yang perlu diperhatikan dalam pengembangan alat ini dikemudian hari. Meskipun alat ini sudah dapat bekerja dengan baik dan sesuai dengan sistem yang direncanakan masih ada hal-hal yang perlu diperhatikan, diantaranya :

1. Untuk pengembangan lebih lanjut, dapat ditambahkan *eksternal* RAM dengan kapasitas yang lebih besar agar agenda yang disimpan bisa lebih dari 7 buah agenda.
2. Proses komunikasi untuk input data dan perintah dapat digunakan sistem komunikasi *wireless* sehingga dapat dioperasikan dalam jarak dan tempat yang dapat disesuaikan.
3. Penggantian komponen dot matrik dengan *pixel* yang lebih rapat atau warna beragam akan dapat memberikan tampilan karakter yang lebih baik, tanpa mengurangi dimensi alat.
4. Suara yang dikeluarkan IC ISD bisa lebih dari 20 detik dengan cara mengganti IC ISD dengan kapasitas yang lebih besar.
5. Untuk penggunaan agenda elektronik dalam jumlah yang besar, tidak lagi digunakan komunikasi serial RX-TX, namun memakai RS.

DAFTAR PUSTAKA

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LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGURA-GURA 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Yoke Rahatna Kusuma
Nim : 0117158
Masa Bimbingan : 18-Jul-2005 s/d 18-Jan-2006
Judul Skripsi : Aplikasi Mikrokontroller ATMEGA 8 sebagai agenda elektronik yang ditempatkan pada ruang kerja dengan tampilan dot matrik

NO	Tanggal	Uraian	Paraf Pembimbing
1.	20 Juli 2005	Diagram Blok	
2.	20 Juli 2005	Flowchart Sistem	
3.	13-9-2005	Rumus Buzzer Bab III	
4.	20-9-2005	Foto alat seluruhnya	
5.	20-9-2005	Acc Bab I, II	
6.	20-9-2005	Acc Bab III, IV, V	
7.	20-9-2005	Listing program	
8.	24-9-2005	Demo Alat	
9.	24-9-2005	Acc ujian compre	
10.			

Malang, 24-9-2005
Dosen Pembmbing

Joseph Dedy Irawan, ST, MT

Form. S-4a

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : YOKE. RAKATNA. KUSUMA
N I M :
Perbaikan meliputi :

- BUAT. CAYOUT. PADA PEMBUATAN
- Kompilasi rujs dimasukkan hasil pengujian.

Malang, 200

(_____)

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA :
N I M :
Perbaikan meliputi :

- Rangkaian display Dot Matrik perbaiki !
- Kesimpulan
- pengujian data keyboard ke dot Matrik & suara !

Malang, 200

(M. ASHAR)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama : Yoke Rahatna Kusuma

NIM : 01.17.158

Masa Bimbingan : 18 Juli 2005 s/d 18 Januari 2006

Judul : Aplikasi Mikrokontroler ATmega8 Sebagai Agenda Elektronik Yang Ditempatkan Pada Ruang Kerja Dengan Tampilan Dot Matrik

No	Tanggal	Uraian	Paraf
1	7 Oktober 2005	• Buat Layout PCBnya • Kesimpulan sesuai hasil pengujian	
2	7 Oktober 2005	• Perbaiki rangkaian dot matrik • Pengujian data keyboard ke dot matrik	

Disetujui

Penguji I

(Ir. Usman Djuanda, MM)
NIP. 1018700143

Penguji II

(M. Ashar, ST, MT)

Mengetahui
Dosen Pembimbing

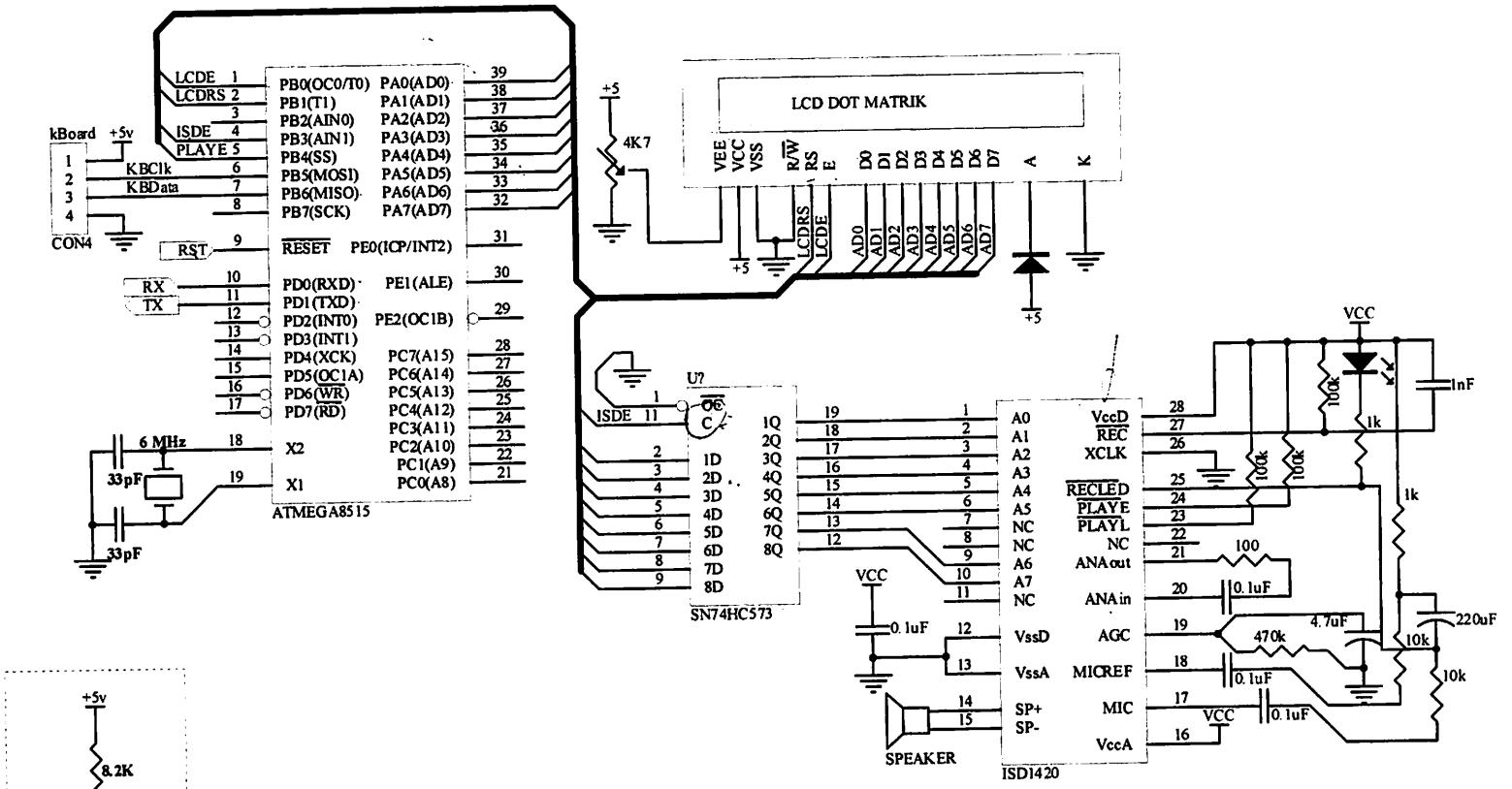
(Joseph Dedy Irawan, ST, MT)
NIP.1039800324

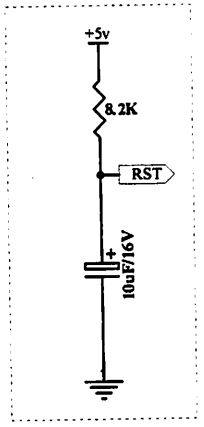
INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

LEMBAR BIMBINGAN SKRIPSI

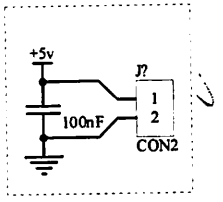
Nama	: Yoke Rahatna Kusuma
NIM	: 01.17.158
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Judul Skripsi	: Aplikasi Mikrokontroler ATmega8 Sebagai Agenda Elektrtonik Yang Ditempatkan Pada Ruang Kerja Dengan Tampilan Dot Matrik
Tanggal Pengajuan Skripsi	: 27 Mei 2005
Selesai Penulisan Skripsi	: 16 September 2005
Dosen Pembimbing	: Joseph Dedy Irawan, ST, MT
Telah Dievaluasi Dengan Nilai	: 83 (A)

Mengetahui	Diperiksa Dan Disetujui,
Ketua Jurusan T. Elektro S-1	Dosen Pembimbing
(Ir. F. Yudi Limpraptono, MT)	(Joseph Dedy Irawan, ST, MT)
NIP.Y.1039500274	NIP.1039800324



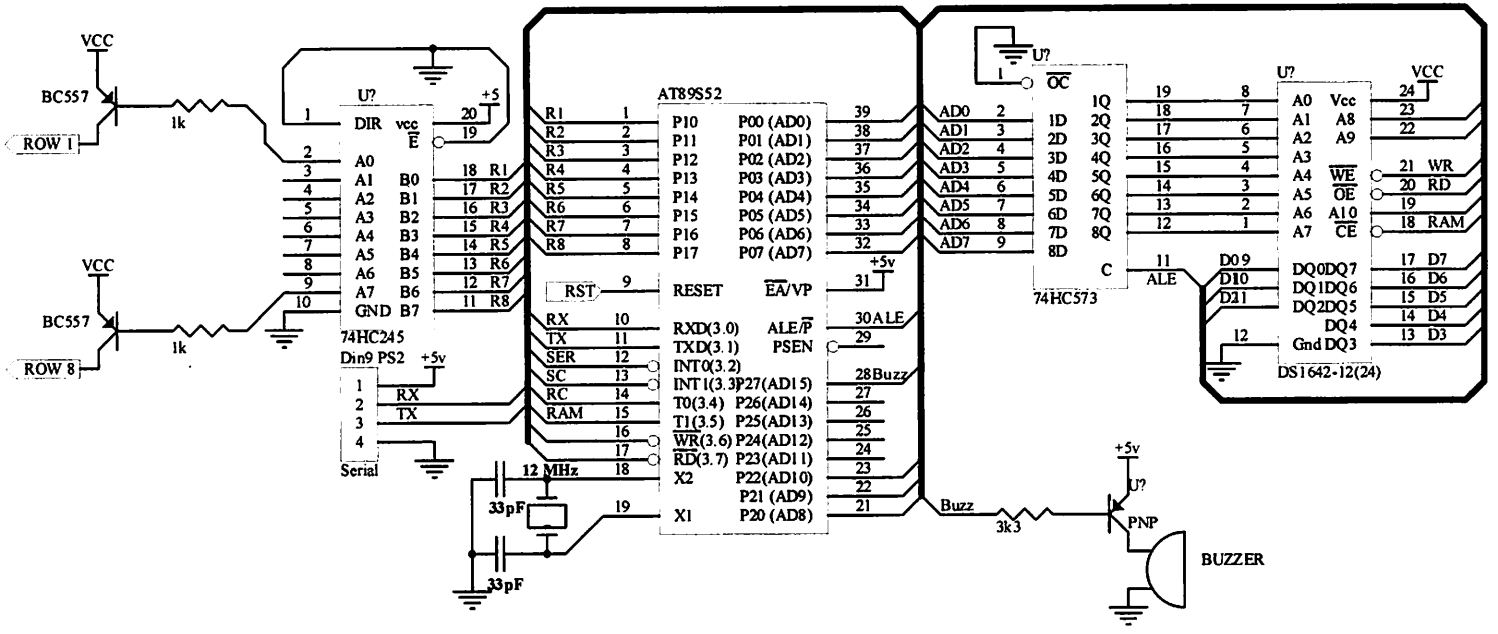


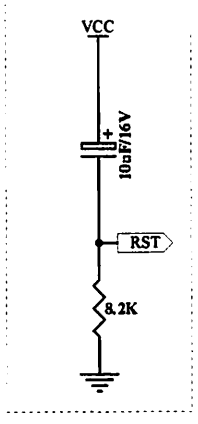
Rangkaian RESET MCU



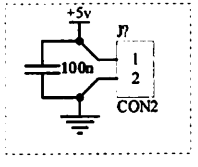
Power Suply

Title	YOKE 1		
Size A4	Number		Revision
Date:	9/12/2005	Sheet of	
File:	E:\My Document C\..\Mcu8515.sch	Drawn By:	



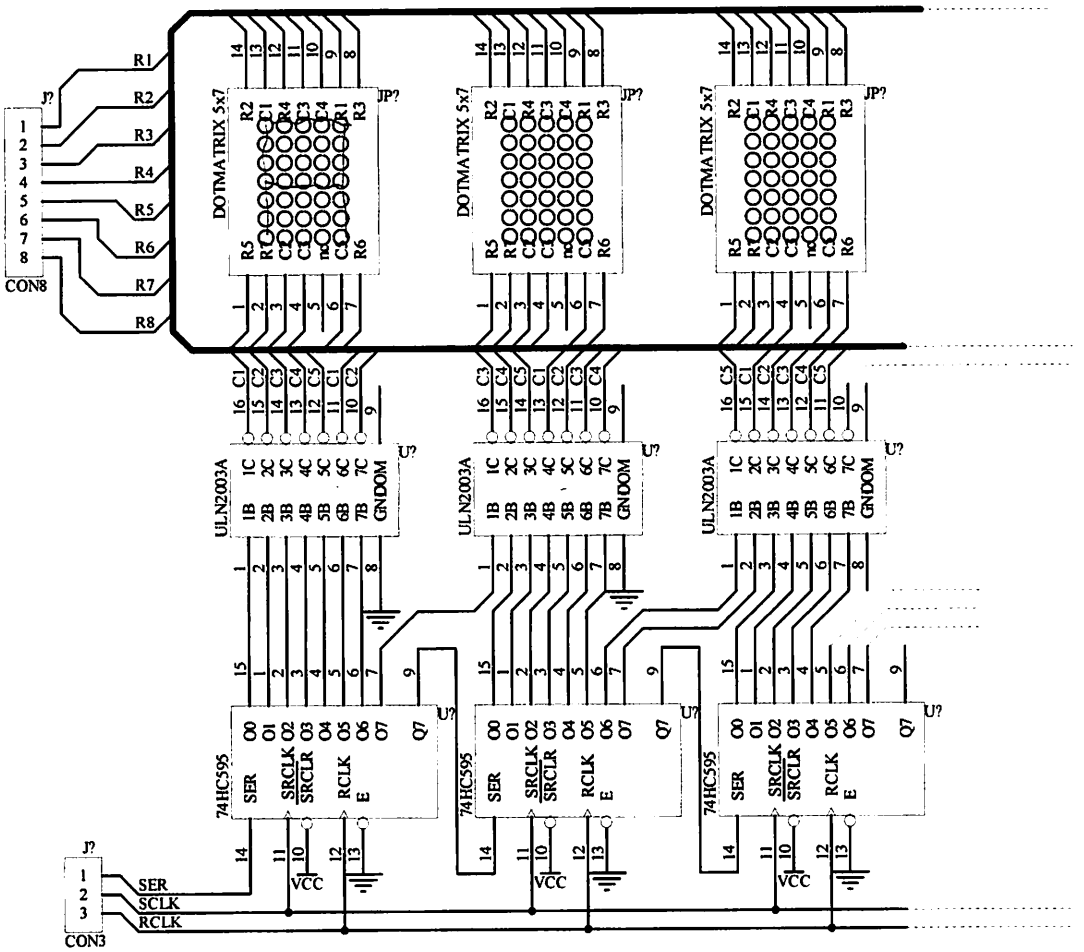


Rangkaian RESET MCU



Power Suply

Title		
Size A4	Number	Revision
Date: 9/12/2005		Sheet of
File: E:\My Document C\..\Tampil.sch		Drawn By:



Title		
Size A4	Number	Revision
Date: 9/12/2005	Sheet of	
File: E:\My Document C\..\DMatrik.sch	Drawn By:	

Program Inti Sistem Display

```
;----------------iRAM
; 09h            = reg E kolom display
; 0ah            = xxxxxxxxxxxxxx
; 0bh            = kolom seleksi
; 0ch            = data serial
; 0dh            = DPL
; 0eh            = DPH
; 0fh            = xxxxxxxxxxxxxxxxx
; 16h-1dh        = Mingkem
; 1eh-25h        = stengaah
; 26h-2dh        = Mangap
;
; 30h-76h        = addr kolom (Ek = 46h)
; C8h-100h       = SP (56)
; (20-7D)        = ASCII enable code
; (00-83)        = ScanCode enable code
;----------------xRAM DS1642
; 0000 ---- 00ff = working reg.
; 0100 01 02 03 04 05 06 07 08 10----E0 F8 F9---FF
;  E  no Ts Bl Tg Jm Mn        A-208d   A  not used
; 7 agenda sampai pada address:
; 0700 01 02 03 04 05 06 07 08 10----E0 F8 F9---FF

;----------------------------------
; EQUATION
;----------------------------------
                XREG   Equ 4000h

                SERr   bit P3.2
                SCLK   bit P3.3
                RCLK   bit P3.4
                XRAM   Bit P3.5
                Buzz   Bit P2.7
                roww   Equ P1

                DMenu  Equ 10h          ;01=Edit,02=Hapus,03=Baca,04=SetTime
                DNomerEqu 11h
                DTSet  Equ 12h          ;
                DBln   Equ 13h          ;BCD
                DTgl   Equ 14h          ;BCD
                DJam   Equ 15h          ;BCD
                Dmnt   Equ 16h
                Ddtk   Equ 17h
                Dthn   Equ 18h

                DBaca  Equ 20h
                DEdit  Equ 21h
                DHapus Equ 22h
                TeHaN  Equ 0ah
                TeElN  Equ 0fh
;-----------------------------------
;inisialisasi timer & int
;-----------------------------------
```

```
INITHARD:   mov 0bh,#30h    ;addr kolom
            mov 09h,#00h    ;E kolom 46h
            mov TeHaN,#0FEh
            mov TeElN,#60h
            mov SCON,#50h ;serial mode 1 REN
            MOV TMOD,#21H       ;timer 1 mode 2,timer 0 mode 1
            MOV TH0,TeHaN
            MOV TL0,TeElN
            mov TH1,#0F3h ;Reload  for 2404 @ 12 Mhz
            ;orl 87h,#80h    ;set SMOD
            setb TR1        ;Turn on timer 1
            mov IP,#02h     ;int T0
            mov TCON,#50h
            mov IE,#92h     ;EA,ES,ET0
            SETB TR0
            setb TR1
            mov 0eh,#00h
            mov 0dh,#00h
            ret
;-------------------------------------
;Clear Tampilan
;-------------------------------------
Clear:      push PSW
            push Acc
            push 01h
            mov r1,#30h
clear1:     mov @r1,#0ffh
            inc r1
            cjne r1,#76h,clear1
            pop 01h
            pop Acc
            pop PSW
            ret

;-------------------------------------
;Bunyi tiiiiii
;-------------------------------------
Tititi:     setb Buzz
            lcall del01sec
            lcall del01sec
            clr Buzz
            lcall del01sec
            lcall del01sec
            setb Buzz
            lcall del01sec
            lcall del01sec
            clr Buzz
            lcall del025sec
            lcall del01sec
            setb Buzz
            lcall del025sec
            lcall del01sec
            clr Buzz
            ret

Tiitok:     setb Buzz
```

```
                lcall del01sec
                lcall del10ms
                clr Buzz
                lcall delay_2
                ret

;-------------------------------------
;INISIALISASI & SET RTC
;-------------------------------------
SetRTC:         mov a,#80h
                mov dptr,#07F8h ;reg A Wr
                clr XRAM
                nop
                movx @dptr,a
                nop
                mov dptr,#07FFh
                mov a,#05h      ;thn
                nop
                movx @dptr,a
                nop
                mov dptr,#07FEh
                mov a,#09h      ;bln
                nop
                movx @dptr,a
                nop
                mov dptr,#07FDh
                mov a,#20h      ;tgl
                nop
                movx @dptr,a
                nop
                mov dptr,#07FCh
                mov a,#03h      ;day
                nop
                movx @dptr,a
                nop
                mov dptr,#07FBh
                mov a,#23h      ;hour
                nop
                movx @dptr,a
                nop
                mov dptr,#07FAh
                mov a,#08h      ;mnt
                nop
                movx @dptr,a
                nop
                mov dptr,#07F9h
                mov a,#40h      ;sec
                nop
                movx @dptr,a
                nop
                mov dptr,#07F8h
                mov a,#00h
                nop
                movx @dptr,a
                nop
                setb XRAM
```

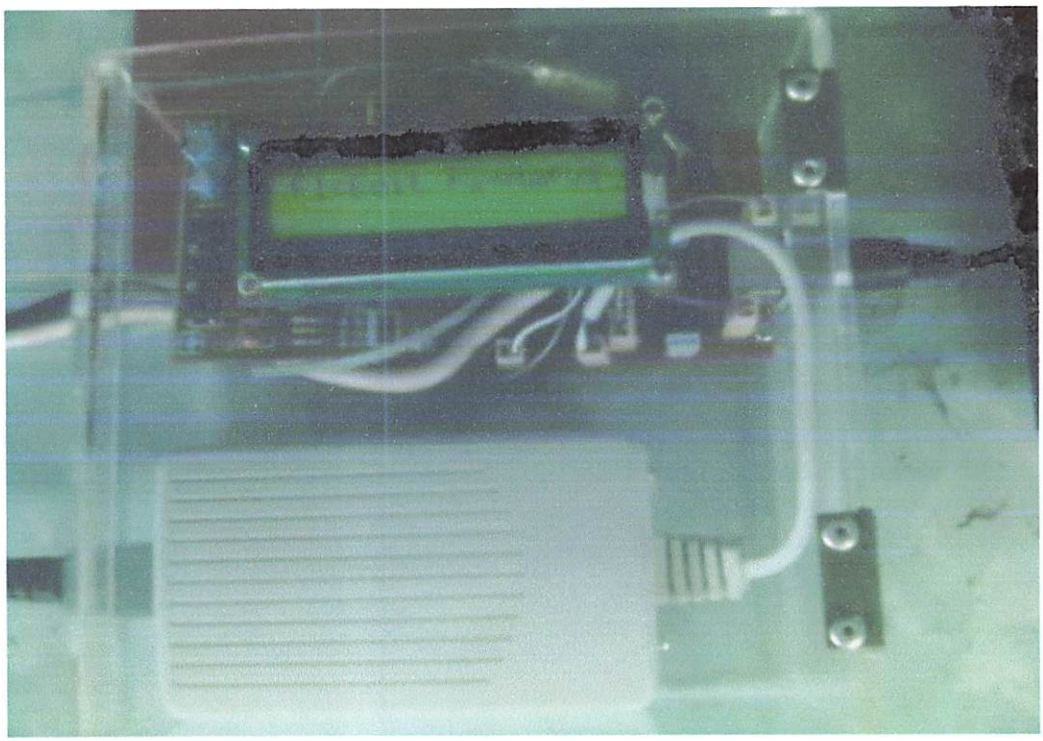
```
                ret

;-----------------------------------------
; Ambil Data Waktu RTC
;-----------------------------------------
AmbilRTC:       push acc
                push dph
                push dpl
                mov dptr,#07f8h
                mov a,#40h
                clr XRAM
                movx @dptr,a
                setb XRAM
                mov dptr,#07F9h         ;dtk
                clr XRAM
                movx a,@dptr
                setb XRAM
                mov Ddtk,a
                inc dptr
                clr XRAM
                movx a,@dptr
                setb XRAM
                mov Dmnt,a              ;mnt
                inc dptr
                clr XRAM
                movx a,@dptr
                setb XRAM
                mov Djam,a              ;jam
                inc dptr
                inc dptr
                clr XRAM
                movx a,@dptr
                setb XRAM
                mov Dtgl,a              ;tanggal
                inc dptr
                clr XRAM
                movx a,@dptr
                setb XRAM
                mov Dbln,a              ;bulan
                inc dptr
                clr XRAM
                movx a,@dptr
                setb XRAM
                mov Dthn,a              ;Tahun
                mov dptr,#07f8h
                mov a,#00h
                clr XRAM
                movx @dptr,a
                setb XRAM
                pop dpl
                pop dph
                pop acc
                ret
;-------------------------------------
;Program Starting
;-------------------------------------
```

```
Mulai:      nop
            nop
            nop
            nop
            nop
            nop
            nop
            nop
            nop
            nop
            nop
            nop
            mov SP,#0C8h    ;55d
            lcall Tititi
            lcall del05sec
            ;lcall setRTC
            lcall blank
            lcall InitHard
            clr ES

loopi00: lcall del01sec
            lcall Tititi
            lcall T_Waktu
            lcall Searching
            lcall Animasi
            lcall Searching
            Lcall T_Waktu
            clr EA
            lcall blank
            lcall clear
            lcall InitHard
            setb EA
            setb ES
            lcall del01sec
            mov dptr,#0000h
loopi33: lcall Searching
            inc dph
            clr XRAM
            movx a,@dptr
            setb XRAM
            cjne a,#0aah,loopi22
            mov a,#0cch
            lcall SerOut
            lcall Tampil22
            ljmp loopi44
loopi22: mov a,dph
            cjne a,#07h,loopi33
            mov dptr,#TextT00
            lcall Tampil11
            lcall del05sec
            ;mov dptr,#0000h
            ljmp loopi00
loopi44: push dph
            push dpl
            mov dptr,#TextT00
            lcall Tampil11
```

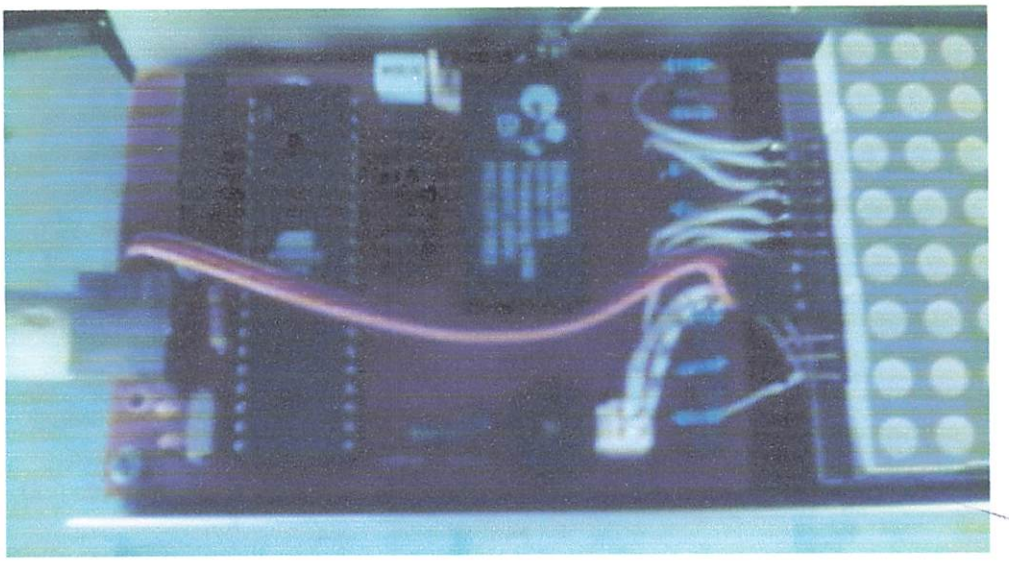
```
                lcall del05sec
                pop dpl
                pop dph
                ljmp loopi33

TextT00:        db '   *space*  ',00h
TextT11:        db '   welcome ',00h

;-----------------------------------
; Tabel ASCII
;-----------------------------------
                ORG     1800H
                DB      0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;space
                DB      0FFH,0FFH,041H,0FFH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;seru
                DB      0FFH,0F1H,0FFH,0F1H,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;ptik2
                DB      0D7H,001H,0D7H,001H,0D7H,0FFH,00,00,00,00,00,00,00,00,00,00 ;pager
                DB      0B7H,0ABH,001H,0ABH,0DBH,0FFH,00,00,00,00,00,00,00,00,00,00 ;dolar
                DB      05CH,0D9H,0EFH,037H,03BH,0FFH,00,00,00,00,00,00,00,00,00,00 ;prsen
                DB      093H,06DH,055H,0BBH,05FH,0FFH,00,00,00,00,00,00,00,00,00,00 ;and
                DB      0FFH,0F5H,0F9H,0FFH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;ptik1
                DB      0FFH,0C7H,0BBH,07DH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;kbka
                DB      0FFH,07DH,0BBH,0C7H,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;kttup
                DB      0D7H,0EFH,083H,0EFH,0D7H,0FFH,00,00,00,00,00,00,00,00,00,00 ;bntng
                DB      0EFH,0EFH,083H,0EFH,0EFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;plus
                DB      0FFH,05FH,09FH,0FFH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;koma
                DB      0F7H,0F7H,0F7H,0F7H,0F7H,0FFH,00,00,00,00,00,00,00,00,00,00 ;min
                DB      0FFH,09FH,09FH,0FFH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;ttik
                DB      0DFH,0EFH,0F7H,0FBH,0FDH,0FFH,00,00,00,00,00,00,00,00,00,00 ;garing
                DB      0C1H,0AEH,0B6H,0BAH,0C1H,0FFH,00,00,00,00,00,00,00,00,00,00 ;0
                DB      0FFH,0FFH,0BDH,080H,0BFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;1
                DB      0BDH,09EH,0AEH,0B6H,0B9H,0FFH,00,00,00,00,00,00,00,00,00,00 ;2
                DB      0DEH,0BEH,0BAH,0B4H,0CEH,0FFH,00,00,00,00,00,00,00,00,00,00 ;3
                DB      0E7H,0EBH,0EDH,080H,0EFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;4
                DB      0D0H,0B6H,0B6H,0B6H,0CEH,0FFH,00,00,00,00,00,00,00,00,00,00 ;5
                DB      0C3H,0B5H,0B6H,0B6H,0CFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;6
                DB      0FEH,08EH,0F6H,0FAH,0FCH,0FFH,00,00,00,00,00,00,00,00,00,00 ;7
                DB      0C9H,0B6H,0B6H,0B6H,0C9H,0FFH,00,00,00,00,00,00,00,00,00,00 ;8
                DB      0F9H,0B6H,0B6H,0D6H,0E1H,0FFH,00,00,00,00,00,00,00,00,00,00 ;9
                DB      0FFH,0C9H,0C9H,0FFH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;ttik2
                DB      0FFH,0A9H,0C9H,0FFH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;tikoma
                DB      0F7H,0EBH,0DDH,0BEH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;lkcl
                DB      0EBH,0EBH,0EBH,0EBH,0EBH,0FFH,00,00,00,00,00,00,00,00,00,00 ;smdng
                DB      0BEH,0DDH,0EBH,0F7H,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;lbsr
                DB      0FDH,0FEH,0AEH,0F6H,0F9H,0FFH,00,00,00,00,00,00,00,00,00,00 ;ttnya
                DB      0CDH,0B6H,086H,0BEH,0C1H,0FFH,00,00,00,00,00,00,00,00,00,00 ;akurng
                DB      081H,0EEH,0EEH,0EEH,081H,0FFH,00,00,00,00,00,00,00,00,00,00 ;A
                DB      080H,0B6H,0B6H,0B6H,0C9H,0FFH,00,00,00,00,00,00,00,00,00,00 ;B
                DB      0C1H,0BEH,0BEH,0BEH,0DDH,0FFH,00,00,00,00,00,00,00,00,00,00 ;C
                DB      080H,0BEH,0BEH,0DDH,0E3H,0FFH,00,00,00,00,00,00,00,00,00,00 ;D
                DB      080H,0B6H,0B6H,0B6H,0BEH,0FFH,00,00,00,00,00,00,00,00,00,00 ;E
                DB      080H,0F6H,0F6H,0F6H,0FEH,0FFH,00,00,00,00,00,00,00,00,00,00 ;F
                DB      0C1H,0BEH,0B6H,0B6H,085H,0FFH,00,00,00,00,00,00,00,00,00,00 ;G
                DB      080H,0F7H,0F7H,0F7H,080H,0FFH,00,00,00,00,00,00,00,00,00,00 ;H
                DB      0FFH,0BEH,080H,0BEH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;I
                DB      0DFH,0BFH,0BEH,0C0H,0FEH,0FFH,00,00,00,00,00,00,00,00,00,00 ;J
                DB      080H,0F7H,0EBH,0DDH,0BEH,0FFH,00,00,00,00,00,00,00,00,00,00 ;K
```

```
        DB      080H,0BFH,0BFH,0BFH,0BFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;L
        DB      080H,0FDH,0F3H,0FDH,080H,0FFH,00,00,00,00,00,00,00,00,00,00 ;M
        DB      080H,0FBH,0F7H,0EFH,080H,0FFH,00,00,00,00,00,00,00,00,00,00 ;N
        DB      0C1H,0BEH,0BEH,0BEH,0C1H,0FFH,00,00,00,00,00,00,00,00,00,00 ;O
        DB      080H,0F6H,0F6H,0F6H,0F9H,0FFH,00,00,00,00,00,00,00,00,00,00 ;P
        DB      0C1H,0BEH,0AEH,0DEH,0A1H,0FFH,00,00,00,00,00,00,00,00,00,00 ;Q
        DB      080H,0F6H,0E6H,0D6H,0B9H,0FFH,00,00,00,00,00,00,00,00,00,00 ;R
        DB      0B9H,0B6H,0B6H,0B6H,0CEH,0FFH,00,00,00,00,00,00,00,00,00,00 ;S
        DB      0FEH,0FEH,080H,0FEH,0FEH,0FFH,00,00,00,00,00,00,00,00,00,00 ;T
        DB      0C0H,0BFH,0BFH,0BFH,0C0H,0FFH,00,00,00,00,00,00,00,00,00,00 ;U
        DB      0E0H,0DFH,0BFH,0DFH,0E0H,0FFH,00,00,00,00,00,00,00,00,00,00 ;V
        DB      0C0H,0BFH,0CFH,0BFH,0C0H,0FFH,00,00,00,00,00,00,00,00,00,00 ;W
        DB      09CH,0EBH,0F7H,0EBH,09CH,0FFH,00,00,00,00,00,00,00,00,00,00 ;X
        DB      0F8H,0F7H,08FH,0F7H,0F8H,0FFH,00,00,00,00,00,00,00,00,00,00 ;Y
        DB      09EH,0AEH,0B6H,0BAH,0BCH,0FFH,00,00,00,00,00,00,00,00,00,00 ;Z
        DB      0FFH,080H,0BEH,0BEH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;kbka
kotk
        DB      0EAH,0E9H,083H,0E9H,0EAH,0FFH,00,00,00,00,00,00,00,00,00,00 ;garing kr
        DB      0FFH,0BEH,0BEH,0BEH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;kttupktk
        DB      0FBH,0FDH,0FEH,0FDH,0FBH,0FFH,00,00,00,00,00,00,00,00,00,00 ;capil
        DB      0BFH,0BFH,0BFH,0BFH,0BFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;gr bwh
        DB      0FFH,0FEH,0FDH,0FBH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;ptk bwh
        DB      0DFH,0ABH,0ABH,0ABH,087H,0FFH,00,00,00,00,00,00,00,00,00,00 ;a
        DB      080H,0B7H,0BBH,0BBH,0C7H,0FFH,00,00,00,00,00,00,00,00,00,00 ;b
        DB      0C7H,0BBH,0BBH,0BBH,0DFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;c
        DB      0C7H,0BBH,0BBH,0B7H,080H,0FFH,00,00,00,00,00,00,00,00,00,00 ;d
        DB      0C7H,0ABH,0ABH,0ABH,0E7H,0FFH,00,00,00,00,00,00,00,00,00,00 ;e
        DB      0F7H,081H,0F6H,0FEH,0FDH,0FFH,00,00,00,00,00,00,00,00,00,00 ;f
        DB      0E7H,05BH,05BH,05BH,083H,0FFH,00,00,00,00,00,00,00,00,00,00 ;g
        DB      080H,0F7H,0FBH,0FBH,087H,0FFH,00,00,00,00,00,00,00,00,00,00 ;h
        DB      0FFH,0BBH,082H,0BFH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;i
        DB      0BFH,07FH,077H,087H,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;j
        DB      080H,0EFH,0D7H,0BBH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;k
        DB      0FFH,0BEH,080H,0BFH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;l
        DB      083H,0FBH,0E7H,0FBH,087H,0FFH,00,00,00,00,00,00,00,00,00,00 ;m
        DB      083H,0F7H,0FBH,0FBH,087H,0FFH,00,00,00,00,00,00,00,00,00,00 ;n
        DB      0C7H,0BBH,0BBH,0BBH,0C7H,0FFH,00,00,00,00,00,00,00,00,00,00 ;o
        DB      007H,0D7H,0D7H,0D7H,0EFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;p
        DB      0F7H,0EBH,0EBH,0E7H,003H,0FFH,00,00,00,00,00,00,00,00,00,00 ;q
        DB      083H,0F7H,0FBH,0FBH,0F7H,0FFH,00,00,00,00,00,00,00,00,00,00 ;r
        DB      0B7H,0ABH,0ABH,0ABH,0DFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;s
        DB      0FBH,0C0H,0B7H,0BFH,0DFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;t
        DB      0C3H,0BFH,0BFH,0DFH,083H,0FFH,00,00,00,00,00,00,00,00,00,00 ;u
        DB      0E3H,0DFH,0BFH,0DFH,0E3H,0FFH,00,00,00,00,00,00,00,00,00,00 ;v
        DB      0C3H,0BFH,0CFH,0BFH,0C3H,0FFH,00,00,00,00,00,00,00,00,00,00 ;w
        DB      0BBH,0D7H,0EFH,0D7H,0BBH,0FFH,00,00,00,00,00,00,00,00,00,00 ;x
        DB      0E7H,05FH,05FH,05FH,087H,0FFH,00,00,00,00,00,00,00,00,00,00 ;y
        DB      0BBH,09BH,0ABH,0B3H,0BBH,0FFH,00,00,00,00,00,00,00,00,00,00 ;z
        DB      0FFH,0F7H,0C9H,0BEH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;lncip bk
        DB      0FFH,0FFH,080H,0FFH,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;vrtikl
        DB      0FFH,0BEH,0C9H,0F7H,0FFH,0FFH,00,00,00,00,00,00,00,00,00,00 ;lncip ttp

        end
```

Sistem Utama

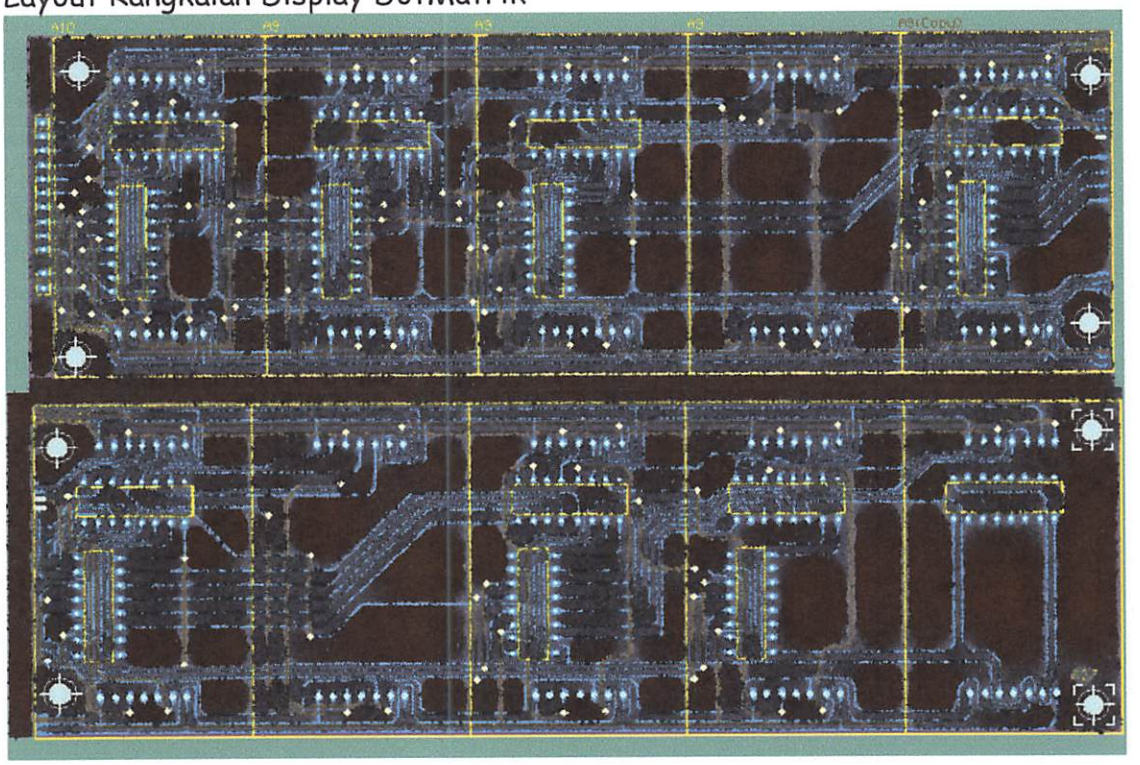


Sistem Display

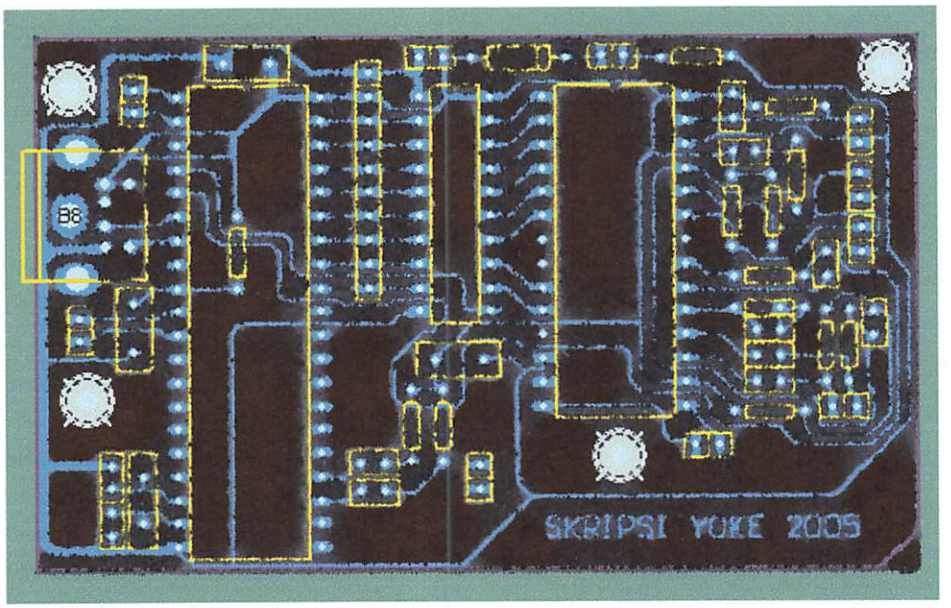


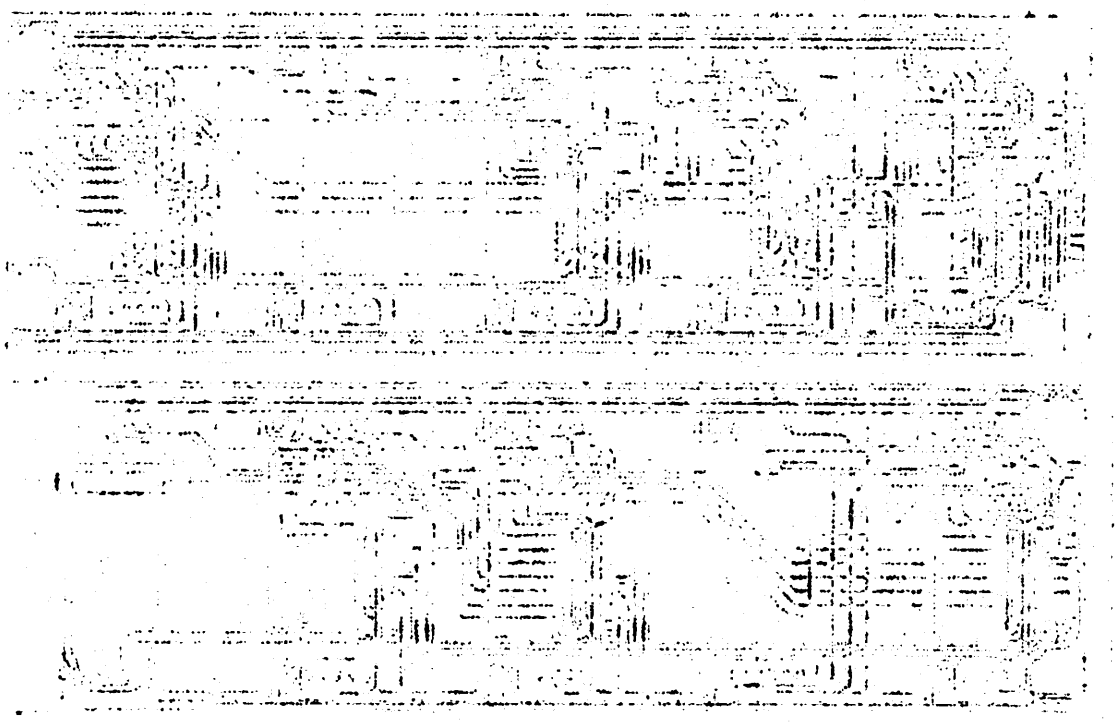
LAYOUT PCB

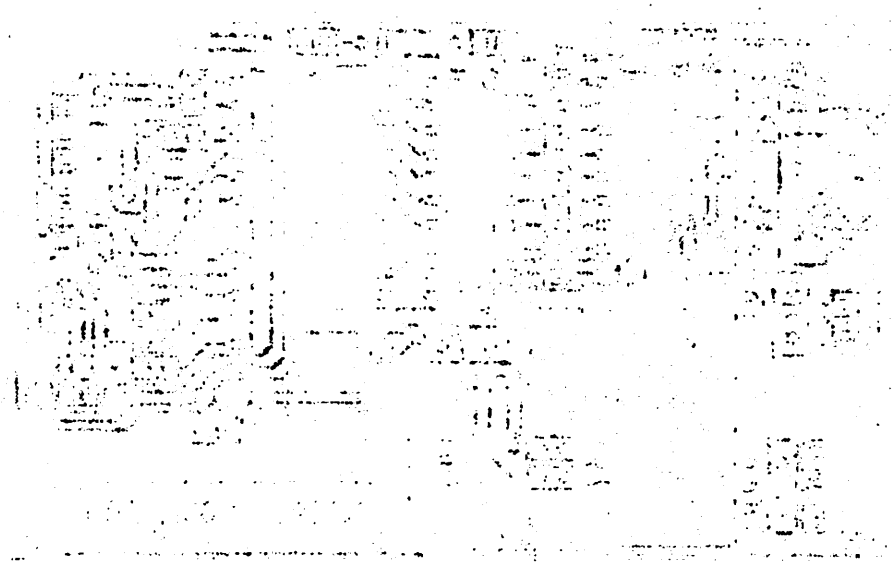
Layout Rangkaian Display DotMatrik



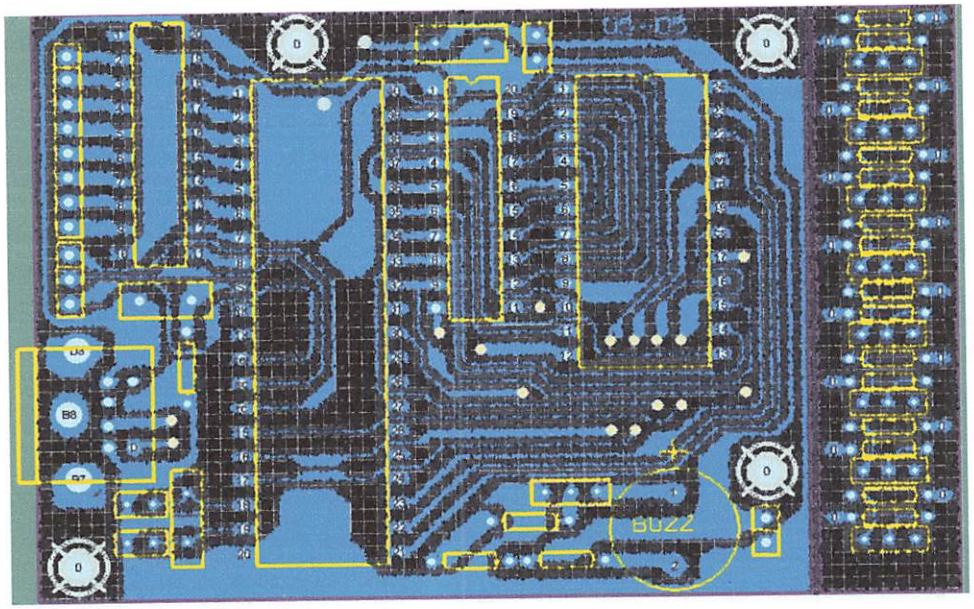
Layout Rangkaian Sistem Utama







Layout Rangkaian Sistem Display



res

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Endurance: 10,000 Write/Erase Cycles
tional Boot Code Section with Independent Lock bits
In-System Programming by On-chip Boot Program
True Read-While-Write Operation
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Endurance: 100,000 Write/Erase Cycles
2 Bytes Internal SRAM
to 64K Bytes Optional External Memory Space
ogramming Lock for Software Security
eral Features
ne 8-bit Timer/Counter with Separate Prescaler and Compare Mode
ne 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture
ode
ree PWM Channels
rogrammable Serial USART
aster/Slave SPI Serial Interface
rogrammable Watchdog Timer with Separate On-chip Oscillator
n-chip Analog Comparator
al Microcontroller Features
ower-on Reset and Programmable Brown-out Detection
ternal Calibrated RC Oscillator
xternal and Internal Interrupt Sources
hree Sleep Modes: Idle, Power-down and Standby
d Packages
5 Programmable I/O Lines
0-pin PDIP, 44-lead TQFP, 44-lead PLCC, and 44-pad QFN/MLF
ting Voltages
.7 - 5.5V for ATmega8515L
.5 - 5.5V for ATmega8515
d Grades
- 8 MHz for ATmega8515L
- 16 MHz for ATmega8515

8-bit AVR® Microcontroller with 8K Bytes In-System Programmable Flash

ATmega8515
ATmega8515L

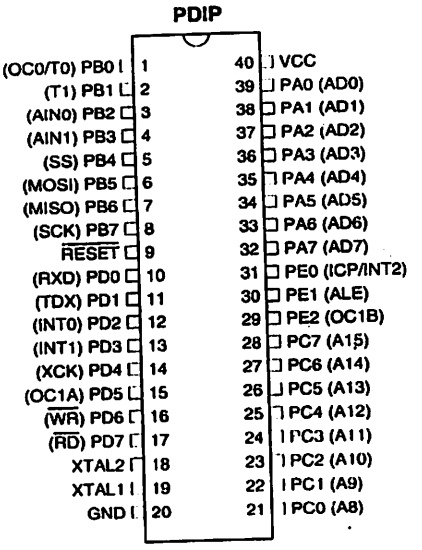
Summary

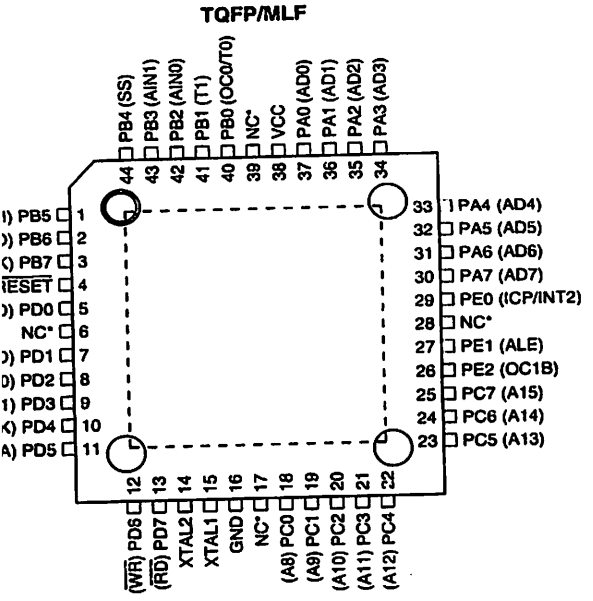
Rev. 2512GS–AVR–03/05

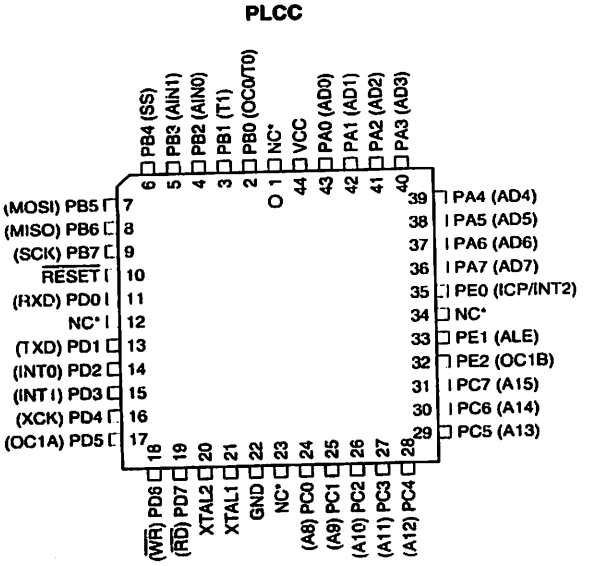
Note: This is a summary document. A complete document is available on our Web site at www.atmel.com.

onfigurations

1. Pinout ATmega8515







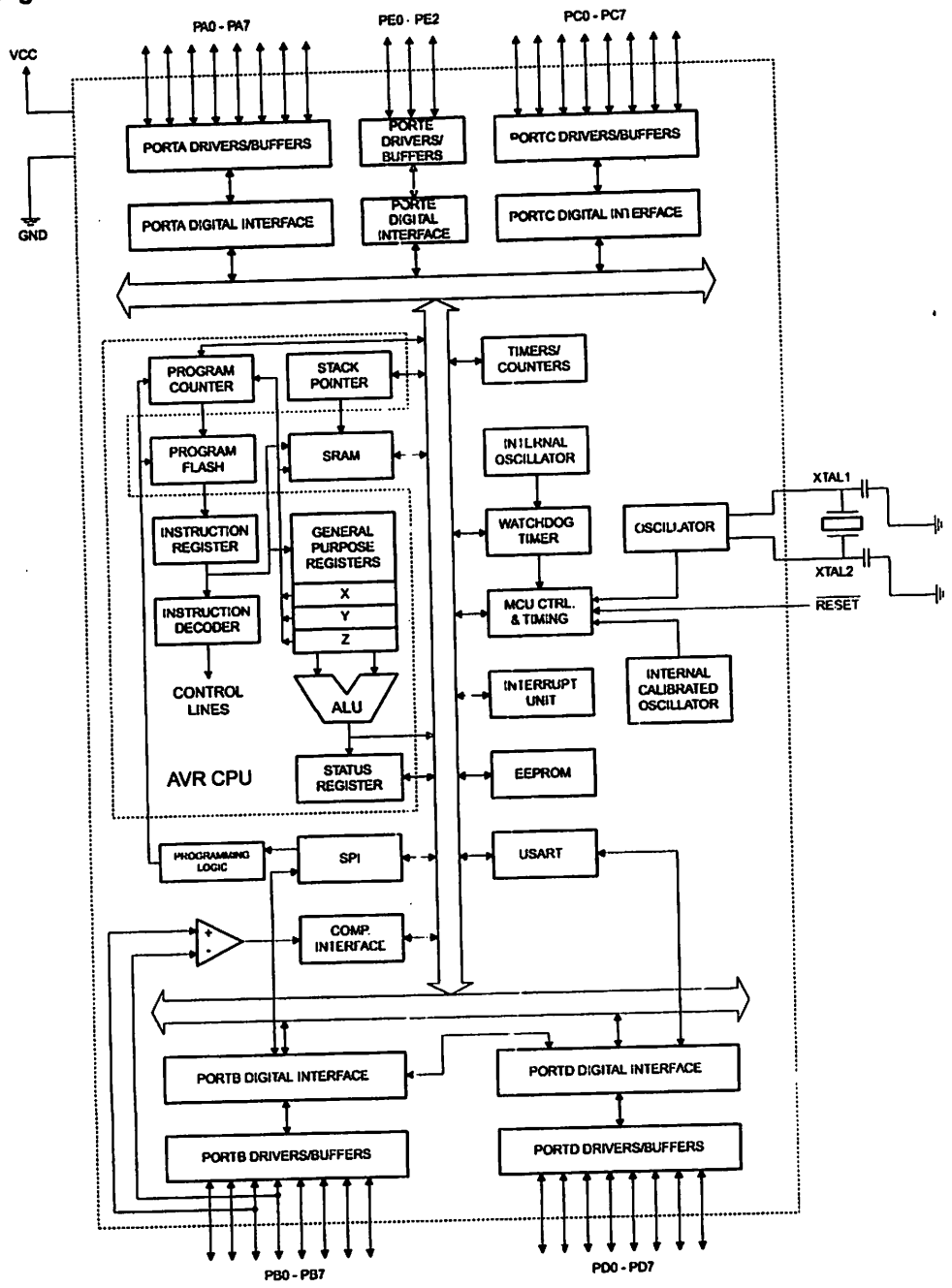
NOTES:
1. MLF bottom pad should be soldered to ground.
2. * NC = Do not connect (May be used in future devices)

iew

The ATmega8515 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8515 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Diagram

Figure 2. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8515 provides the following features: 8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes EEPROM, 512 bytes SRAM, an External memory interface, 35 general purpose I/O lines, 32 general purpose working registers, two flexible Timer/Counters with compare modes, Internal and External interrupts, a Serial Programmable USART, a programmable Watchdog Timer with internal Oscillator, a SPI serial port, and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and Interrupt system to continue functioning. The Power-down mode saves the Register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density nonvolatile memory technology. The On-chip ISP Flash allows the Program memory to be reprogrammed In-System through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-programmable Flash on a monolithic chip, the Atmel ATmega8515 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega8515 is supported with a full suite of program and system development tools including: C Compilers, Macro assemblers, Program debugger/simulators, In-circuit Emulators, and Evaluation kits.

laimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

)S4414/8515 and ıega8515 ıpatibility

The ATmega8515 provides all the features of the AT90S4414/8515. In addition, several new features are added. The ATmega8515 is backward compatible with AT90S4414/8515 in most cases. However, some incompatibilities between the two microcontrollers exist. To solve this problem, an AT90S4414/8515 compatibility mode can be selected by programming the S8515C Fuse. ATmega8515 is 100% pin compatible with AT90S4414/8515, and can replace the AT90S4414/8515 on current printed circuit boards. However, the location of Fuse bits and the electrical characteristics differs between the two devices.

S4414/8515 Compatibility

Programming the S8515C Fuse will change the following functionality:

- The timed sequence for changing the Watchdog Time-out period is disabled. See "Timed Sequences for Changing the Configuration of the Watchdog Timer" on page 52 for details.
- The double buffering of the USART Receive Registers is disabled. See "AVR USART vs. AVR UART – Compatibility" on page 135 for details.
- PORTE(2:1) will be set as output, and PORTE0 will be set as input.

escriptions

Digital supply voltage.

Ground.

(PA7..PA0)

Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATmega8515 as listed on page 66.

(PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega8515 as listed on page 66.

(PC7..PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

(PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega8515 as listed on page 71.

(PE2..PE0)

Port E is an 3-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port E also serves the functions of various special features of the ATmega8515 as listed on page 73.

$\overline{T}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 18 on page 45. Shorter pulses are not guaranteed to generate a reset.

I

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2

Output from the inverting Oscillator amplifier.

ister Summary

ress	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$5F)	SREG	I	T	H	S	V	N	Z	C	9
$5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	11
$5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	11
$5C)	Reserved	-								
$5B)	GICR	INT1	INT0	INT2	-	-	-	IVSEL	IVCE	56, 77
$5A)	GIFR	INTF1	INTF0	INTF2	-	-	-	-	-	78
$59)	TIMSK	TOIE1	OCIE1A	OCIE1B	-	TICIE1	-	TOIE0	OCIE0	92, 123
$58)	TIFR	TOV1	OCF1A	OCF1B	-	ICF1	-	TOV0	OCF0	92, 124
$57)	SPMCR	SPMIE	RWWSB	-	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	168
$56)	EMCUCR	SM0	SRL2	SRL1	SRL0	SRW01	SRW00	SRW11	ISC2	28,41,77
$55)	MCUCR	SRE	SRW10	SE	SM1	ISC11	ISC10	ISC01	ISC00	28,40,76
$54)	MCUCSR	-	-	SM2	-	WDRF	BORF	EXTRF	PORF	40,48
$53)	TCCR0	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	90
($52)	TCNT0	Timer/Counter0 (8 Bits)								92
($51)	OCR0	Timer/Counter0 Output Compare Register								92
($50)	SFIOR	-	XMBK	XMM2	XMM1	XMM0	PUD	-	PSR10	30,65,95
($4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	118
($4E)	TCCR1B	ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10	121
($4D)	TCNT1H	Timer/Counter1 - Counter Register High Byte								122
($4C)	TCNT1L	Timer/Counter1 - Counter Register Low Byte								122
($4B)	OCR1AH	Timer/Counter1 - Output Compare Register A High Byte								122
($4A)	OCR1AL	Timer/Counter1 - Output Compare Register A Low Byte								122
($49)	OCR1BH	Timer/Counter1 - Output Compare Register B High Byte								122
($48)	OCR1BL	Timer/Counter1 - Output Compare Register B Low Byte								122
($47)	Reserved	-								-
($46)	Reserved	-								-
($45)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								123
($44)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								123
($43)	Reserved	-								-
($42)	Reserved	-								-
($41)	WDTCR	-	-	-	WDCE	WDE	WDP2	WDP1	WDP0	50
($40)[1]	UBRRH	URSEL	-	-	-	UBRR[11:8]				157
	UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	155
($3F)	EEARH	-	-	-	-	-	-	-	EEAR8	18
($3E)	EEARL	EEPROM Address Register Low Byte								18
($3D)	EEDR	EEPROM Data Register								19
($3C)	EECR	-	-	-	-	EERIE	EEMWE	EEWE	EERE	19
($3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	74
($3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	74
($39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	74
($38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	74
($37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	74
($36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	74
($35)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	74
($34)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	74
($33)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	75
($32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	75
($31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	75
($30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	75
($2F)	SPDR	SPI Data Register								131
($2E)	SPSR	SPIF	WCOL	-	-	-	-	-	SPI2X	131
($2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	129
($2C)	UDR	USART I/O Data Register								153
($2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	153
($2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	154
($29)	UBRRL	USART Baud Rate Register Low Byte								157
($28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	162
($27)	PORTE	-	-	-	-	-	PORTE2	PORTE1	PORTE0	75
($26)	DDRE	-	-	-	-	-	DDE2	DDE1	DDE0	75
($25)	PINE	-	-	-	-	-	PINE2	PINE1	PINE0	75
($24)	OSCCAL	Oscillator Calibration Register								38

1. Refer to the USART description for details on how to access UBRRH and UCSRC.
2. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

3. Some of the Status Flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

ıction Set Summary

nics	Operands	Description	Operation	Flags	#Clocks
TIC AND LOGIC INSTRUCTIONS					
	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
	Rd	One's Complement	Rd ← $FF − Rd	Z,C,N,V	1
	Rd	Two's Complement	Rd ← $00 − Rd	Z,C,N,V,H	1
	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FF - K)	Z,N,V	1
	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
	Rd	Decrement	Rd ← Rd − 1	Z,N,V	1
	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
	Rd	Set Register	Rd ← $FF	None	1
	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z,C	2
	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z,C	2
	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z,C	2
	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
	Rd, Rr	Fractional Multiply Signed	R1:R0 ← (Rd x Rr) << 1	Z,C	2
	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
INSTRUCTIONS					
	k	Relative Jump	PC ← PC + k + 1	None	2
		Indirect Jump to (Z)	PC ← Z	None	2
	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
		Indirect Call to (Z)	PC ← Z	None	3
		Subroutine Return	PC ← STACK	None	4
		Interrupt Return	PC ← STACK	I	4
	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
	Rd,Rr	Compare	Rd − Rr	Z, N,V,C,H	1
	Rd,Rr	Compare with Carry	Rd − Rr − C	Z, N,V,C,H	1
	Rd,K	Compare Register with Immediate	Rd − K	Z, N,V,C,H	1
	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
	P, b	Skip if Bit in I/O Register Is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC← PC+k + 1	None	1/2
	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
	k	Branch if Overflow Flag Is Set	if (V = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Overflow Flag Is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2
	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2

ics	Operands	Description	Operation	Flags	#Clocks
NSFER INSTRUCTIONS					
	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
	Rd, K	Load Immediate	Rd ← K	None	1
	Rd, X	Load Indirect	Rd ← (X)	None	2
	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
	Rd, Y	Load Indirect	Rd ← (Y)	None	2
	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
	Rd, Z	Load Indirect	Rd ← (Z)	None	2
	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
	X, Rr	Store Indirect	(X) ← Rr	None	2
	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
	Y, Rr	Store Indirect	(Y) ← Rr	None	2
	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
	Z, Rr	Store Indirect	(Z) ← Rr	None	2
	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
		Load Program memory	R0 ← (Z)	None	3
	Rd, Z	Load Program memory	Rd ← (Z)	None	3
	Rd, Z+	Load Program memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
		Store Program memory	(Z) ← R1:R0	None	-
	Rd, P	In Port	Rd ← P	None	1
	P, Rr	Out Port	P ← Rr	None	1
	Rr	Push Register on Stack	STACK ← Rr	None	2
	Rd	Pop Register from Stack	Rd ← STACK	None	2
BIT-TEST INSTRUCTIONS					
	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1
	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
	Rd	Swap Nibbles	Rd(3..0)← Rd(7..4),Rd(7..4)← Rd(3..0)	None	1
	s	Flag Set	SREG(s) ← 1	SREG(s)	1
	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
		Set Carry	C ← 1	C	1
		Clear Carry	C ← 0	C	1
		Set Negative Flag	N ← 1	N	1
		Clear Negative Flag	N ← 0	N	1
		Set Zero Flag	Z ← 1	Z	1
		Clear Zero Flag	Z ← 0	Z	1
		Global Interrupt Enable	I ← 1	I	1
		Global Interrupt Disable	I ← 0	I	1
		Set Signed Test Flag	S ← 1	S	1
		Clear Signed Test Flag	S ← 0	S	1
		Set Twos Complement Overflow.	V ← 1	V	1
		Clear Twos Complement Overflow	V ← 0	V	1
		Set T in SREG	T ← 1	T	1
		Clear T in SREG	T ← 0	T	1
		Set Half Carry Flag in SREG	H ← 1	H	1
		Clear Half Carry Flag in SREG	H ← 0	H	1
ONTROL INSTRUCTIONS					

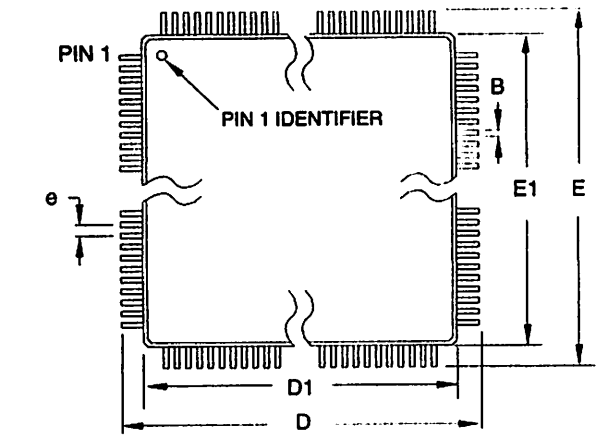
ics	Operands	Description	Operation	Flags	#Clocks
		No Operation		None	1
		Sleep	(see specific descr. for Sleep function)	None	1
		Watchdog Reset	(see specific descr. for WDR/timer)	None	1

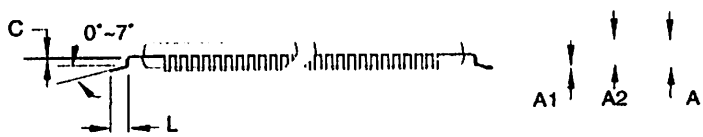
ing Information

ed (MHz)	Power Supply	Ordering Code	Package[1]	Operation Range
8	2.7 - 5.5V	ATmega8515L-8AC	44A	Commercial (0°C to 70°C)
		ATmega8515L-8PC	40P6	
		ATmega8515L-8JC	44J	
		ATmega8515L-8MC	44M1	
		ATmega8515L-8AI	44A	Industrial (-40°C to 85°C)
		ATmega8515L-8PI	40P6	
		ATmega8515L-8JI	44J	
		ATmega8515L-8MI	44M1	
		ATmega8515-16AU[2]	44A	
		ATmega8515-16PU[2]	40P6	
		ATmega8515L-8MU[2]	44M1	
16	4.5 - 5.5V	ATmega8515-16AC	44A	Commercial (0°C to 70°C)
		ATmega8515-16PC	40P6	
		ATmega8515-16JC	44J	
		ATmega8515-16MC	44M1	
		ATmega8515-16AI	44A	Industrial (-40°C to 85°C)
		ATmega8515-16PI	40P6	
		ATmega8515-16JI	44J	
		ATmega8515-16MI	44M1	
		ATmega8515-16AU[2]	44A	
		ATmega8515-16PU[2]	40P6	
		ATmega8515-16MU[2]	44M1	

1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities..
2. Pb-free packaging alternative, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive).Also Halide free and fully Green.

	Package Type
	44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
	44-lead, Plastic J-Leaded Chip Carrier (PLCC)
	44-pad, 7 x 7 x 1.0 mm body, lead pitch 0.50 mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)





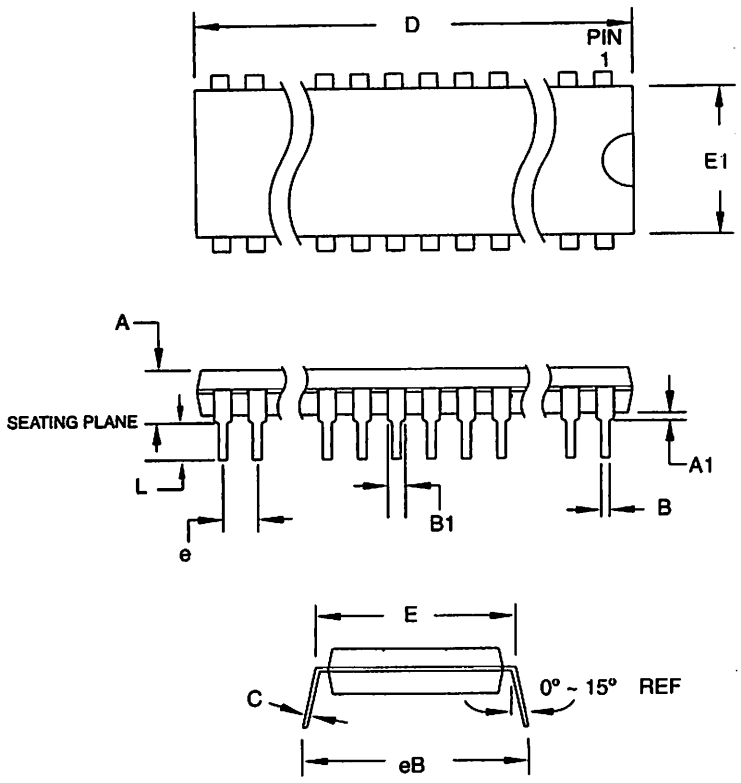
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	44A, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B



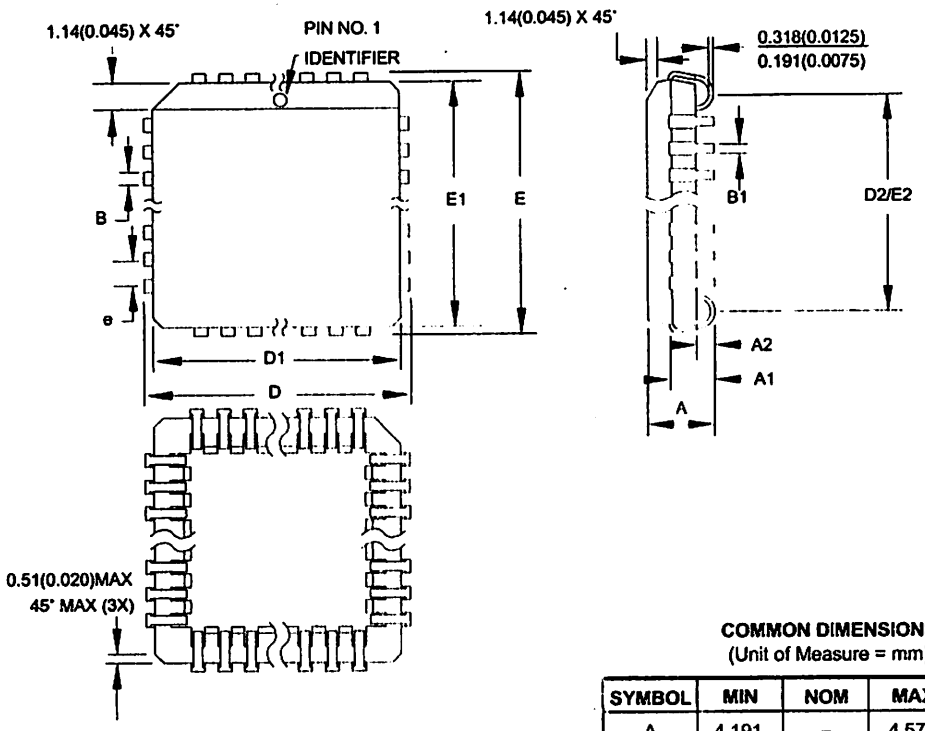
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	40P6, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B



COMMON DIMENSIONS
(Unit of Measure = mm)

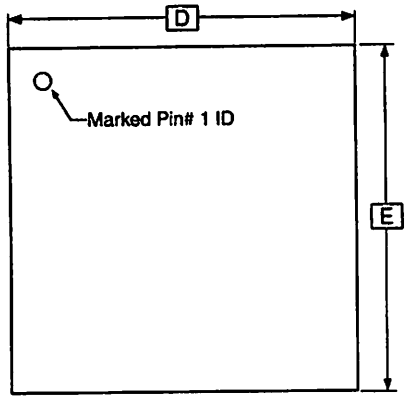
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

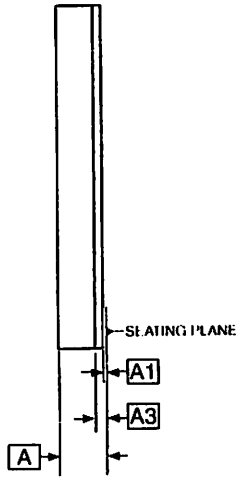
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

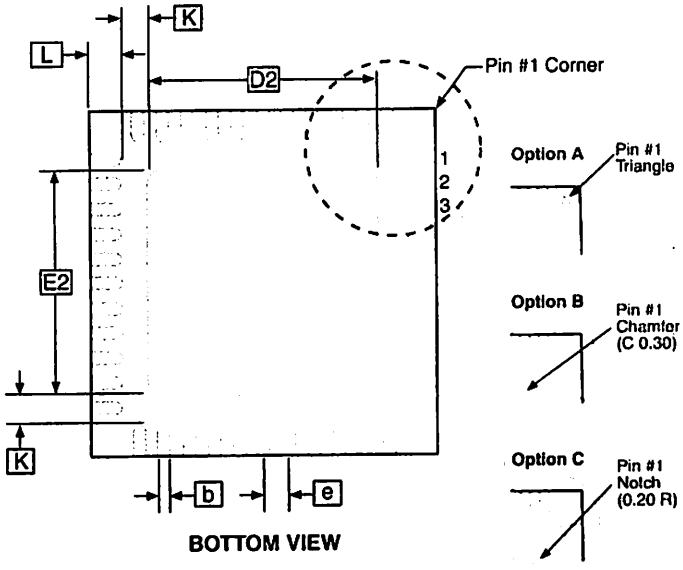
1



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.25 REF		
b	0.18	0.23	0.30	
D		7.00 BSC		
D2	5.00	5.20	5.40	
E		7.00 BSC		
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

3/18/05

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	44M1, 44-pad, 7 x 7 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.20 mm Exposed Pad, Micro Lead Frame Package (MLF)	44M1	F

ata

The revision letter in this section refers to the revision of the ATmega8515 device.

ıega8515(L) Rev. B

There are no errata for this revision of ATmega8515.

asheet Change
for ATmega8515

Please note that the referring page numbers in this section are referring to this document. The referring revision in this section are referring to the document revision.

nges from Rev. 2F-12/03 to Rev. 2G-03/05

1. MLF-package alternative changed to "Quad Flat No-Lead/Micro Lead Frame Package QFN/MLF".
2. Updated "Electrical Characteristics" on page 195
3. Updated "Ordering Information" on page 11.

nges from Rev. 2F-12/03 to Rev. 2E-09/03

1. Updated "Calibrated Internal RC Oscillator" on page 38.

nges from Rev. 2D-02/03 to Rev. 2E-09/03

1. Removed "Preliminary" from the datasheet.
2. Updated Table 18 on page 45 and "Absolute Maximum Ratings" and "DC Characteristics" in "Electrical Characteristics" on page 195.
3. Updated chapter "ATmega8515 Typical Characteristics" on page 205.

nges from Rev. 2C-10/02 to Rev. 2D-02/03

1. Added "EEPROM Write During Power-down Sleep Mode" on page 22.
2. Improved the description in "Phase Correct PWM Mode" on page 87.
3. Corrected OCn waveforms in Figure 53 on page 110.
4. Added note under "Filling the Temporary Buffer (page loading)" on page 171 about writing to the EEPROM during an SPM page load.
5. Updated Table 93 on page 193.
6. Updated "Packaging Information" on page 12.

nges from Rev. 2B-09/02 to Rev. 2C-10/02

1. Added "Using all Locations of External Memory Smaller than 64 KB" on page 30.
2. Removed all TBD.
3. Added description about calibration values for 2, 4, and 8 MHz.
4. Added variation in frequency of "External Clock" on page 39.
5. Added note about V_{BOT}, Table 18 on page 45.
6. Updated about "Unconnected pins" on page 63.
7. Updated "16-bit Timer/Counter1" on page 96, Table 51 on page 118 and Table 52 on page 119.

8. Updated "Enter Programming Mode" on page 182, "Chip Erase" on page 182, Figure 77 on page 185, and Figure 78 on page 186.

9. Updated "Electrical Characteristics" on page 195, "External Clock Drive" on page 197, Table 96 on page 197 and Table 97 on page 198, "SPI Timing Characteristics" on page 198 and Table 98 on page 200.

10. Added "Errata" on page 16.

nges from Rev. 2A-04/02 to Rev. 2B-09/02

1. Changed the Endurance on the Flash to 10,000 Write/Erase Cycles.

nel Corporation

325 Orchard Parkway
an Jose, CA 95131, USA
el: 1(408) 441-0311
ax: 1(408) 487-2600

gional Headquarters

ope
mel Sarl
oute des Arsenaux 41
ase Postale 80
H-1705 Fribourg
vitzerland
el: (41) 26-426-5555
ax: (41) 26-426-5500

a
oom 1219
inachem Golden Plaza
' Mody Road Tsimshatsui
ast Kowloon
ong Kong
el: (852) 2721-9778
ax: (852) 2722-1369

an
', Tonetsu Shinkawa Bldg.
24-8 Shinkawa
uo-ku, Tokyo 104-0033
pan
el: (81) 3-3523-3551
ax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
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38521 Saint-Egreve Cedex, France
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2512GS–AVR–03/05

Interfacing the AT keyboard.

Vhy would you want to interface the Keyboard? The IBM keyboard can be a cheap alternative n a Microprocessor development system. Or maybe you want a remote terminal, just couple it lodule.

laybe you have a RS-232 Barcode Scanner or other input devices, which you want to use witl oftware which only allows you to key in numbers or letters. You could design yourself a little b :S-232 into a Keyboard Transmission, making it transparent to the software.

n interfacing example is given showing the keyboard's protocols in action. This interfacing ex 8HC705J1A MCU to decode an IBM AT keyboard and output the ASCII equivalent of the key PS.

lote that this page only deals with AT Keyboards. If you have any XT keyboards, you wish to i onsider placing them in a museum. We will not deal with this type of keyboard in this documer Keyboards use a different protocol compared to the AT, thus code contained on this page will b

PC Keyboard Theory

The IBM keyboard you most probably have sitting in front of you, sends scan codes to yo The scan codes tell your Keyboard Bios, what keys you have pressed or released. Take t 'A' Key. The 'A' key has a scan code of 1C (hex). When you press the 'A' key, your keybo down it's serial line. If you are still holding it down, for longer than it's typematic delay, an sent. This keeps occurring until another key has been pressed, or if the 'A' key has been

However your keyboard will also send another code when the key has been released. Ta of the 'A' key again, when released, the keyboard will send F0 (hex) to tell you that the ke proceeding scan code has been released. It will then send 1C, so you know which key ha released.

Your keyboard only has one code for each key. It doesn't care it the shift key has been pr send you the same code. It's up to your keyboard BIOS to determine this and take the ap Your keyboard doesn't even process the Num Lock, Caps Lock and Scroll Lock. When yc Caps Lock for example, the keyboard will send the scan code for the cap locks. It is then keyboard BIOS to send a code to the keyboard to turn on the Caps lock LED.

Now there's 101 keys and 8 bits make 256 different combinations, thus you only need to : per key, right?

Nop. Unfortunately a handful of the keys found on your keyboard are extended keys, and two scan code. These keys are preceded by a E0 (hex). But it doesn't stop at two scan cc about E1,14,77,E1,F0,14,F0,77! Now that can't be a valid scan code? Wrong again. It's h sent when you press the Pause/break key. Don't ask me why they have to make it so lon were having a bad day or something?

When an extended key has been released, it would be expect that F0 would be sent to te has been released. Then you would expect E0, telling you it was an extended key followe code for the key pressed. However this is not the case. E0 is sent first, followed by F0, wl extended key has been released.

Keyboard Commands

Besides Scan codes, commands can also be sent to and from the keyboard. The followin the function of these commands. By no means is this a complete list. These are only som common commands.

Host Commands

These commands are sent by the Host to the Keyboard. The most common comma setting/resetting of the Status Indicators (i.e. the Num lock, Caps Lock & Scroll Lock more common and useful commands are shown below.

ED Set Status LED's - This command can be used to turn on and off the Lock, Caps Lock & Scroll Lock LED's. After Sending ED, keyboard w with ACK (FA) and wait for another byte which determines their Statu controls the Scroll Lock, Bit 1 the Num Lock and Bit 2 the Caps lock. 7 are ignored.

EE Echo - Upon sending a Echo command to the Keyboard, the keyboard sh with a Echo (EE)

F0 Set Scan Code Set. Upon Sending F0, keyboard will reply with ACK (wait for another byte, 01-03 which determines the Scan Code Used. S 00 as the second byte will return the Scan Code Set currently in Use

F3 Set Typematic Repeat Rate. Keyboard will Acknowledge command with F wait for second byte, which determines the Typematic Repeat Rate.

F4 Keyboard Enable - Clears the keyboards output buffer, enables Keyb Scanning and returns an Acknowledgment.

F5 Keyboard Disable - Resets the keyboard, disables Keyboard Scanning an an Acknowledgment.

FE Resend - Upon receipt of the resend command the keyboard will re- t the last byte sent.

FF Reset - Resets the Keyboard.

Commands

Now if the Host Commands are send from the host to the keyboard, then the keybo must be sent from the keyboard to host. If you think this way, you must be correct. E some of the commands which the keyboard can send.

FA Acknowledge

AA Power On Self Test Passed (BAT Completed)

EE See Echo Command (Host Commands)

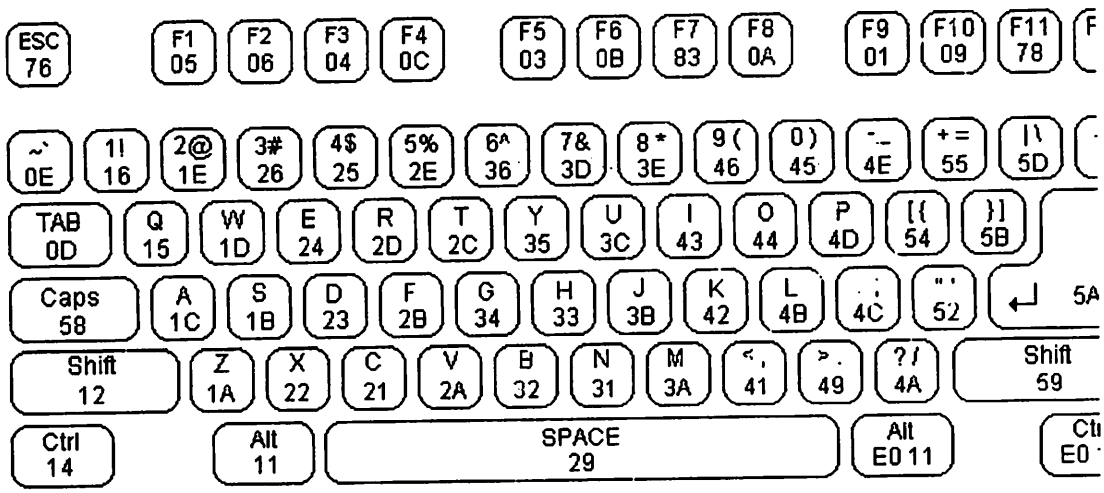
FE Resend - Upon receipt of the resend command the Host should re-transm byte sent.

00 Error or Buffer Overflow

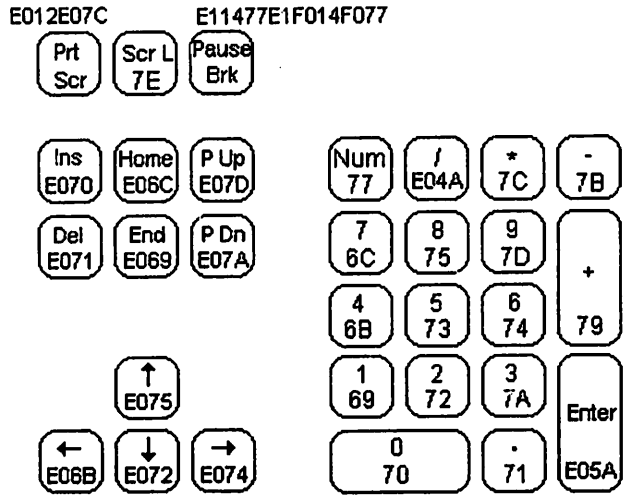
FF Error or Buffer Overflow

can Codes

The diagram below shows the Scan Code assigned to the individual keys. The Scan code the bottom of the key. E.g. The Scan Code for ESC is 76. All the scan codes are shown i

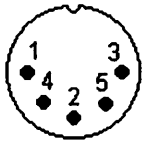


As you can see, the scan code assignments are quite random. In many cases the e convert the scan code to ASCII would be to use a look up table. Below is the scan c extended keyboard & Numeric keypad.



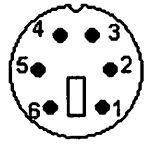
The Keyboard's Connector

The PC's AT Keyboard is connected to external equipment using four wires. These wires below for the 5 Pin DIN Male Plug & PS/2 Plug.



5 Pin DIN

1. KBD Clock
2. KBD Data
3. N/C
4. GND
5. +5V (VCC)



PS/2

1. KBD Clock
2. GND
3. KBD Data
4. N/C
5. +5V (VCC)
6. N/C

A fifth wire can sometimes be found. This was once upon a time implemented as a Keybc today is left disconnected on AT Keyboards. Both the KBD Clock and KBD Data are Opei directional I/O Lines. If desired, the Host can talk to the keyboard using these lines.

Note: Most keyboards are specified to drain a maximum 300mA. This will need to be con. powering your devices

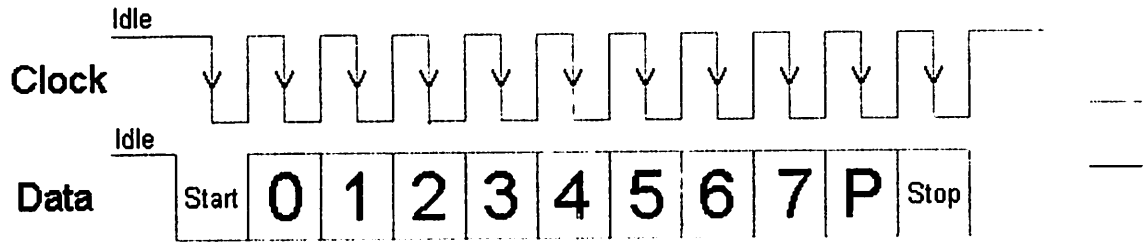
The Keyboard's Protocol

Keyboard to Host

As mentioned before, the PC's keyboard implements a bi-directional protocol. The keybo: data to the Host and the Host can send data to the Keyboard. The Host has the ultimate p direction. It can at anytime (although the not recommended) send a command to the keyt

The keyboard is free to send data to the host when both the KBD Data and KBD Clock lir (Idle). The KBD Clock line can be used as a Clear to Send line. If the host takes the KBD the keyboard will buffer any data until the KBD Clock is released, ie goes high. Should th KBD Data line low, then the keyboard will prepare to accept a command from the host.

The transmission of data in the forward direction, ie Keyboard to Host is done with a fram first bit is a Start Bit (Logic 0) followed by 8 data bits (LSB First), one Parity Bit (Odd Parit Bit (Logic 1). Each bit should be read on the falling edge of the clock.

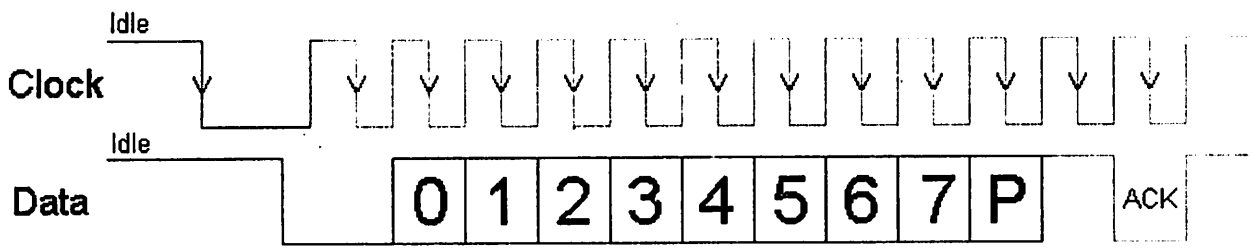


The above waveform represents a one byte transmission from the Keyboard. The keyboa generally change it's data line on the rising edge of the clock as shown in the diagram. Tl has to be valid on the falling edge of the clock. The Keyboard will generate the clock. The the clock signal typically ranges from 20 to 30 Khz. The Least Significant Bit is always se

Host to Keyboard

The Host to Keyboard Protocol is initiated by taking the KBD data line low. However to pr keyboard from sending data at the same time that you attempt to send the keyboard data to take the KBD Clock line low for more than 60us. This is more than one bit length. Then line is taken low, while the KBD clock line is released.

The keyboard will start generating a clock signal on it's KBD clock line. This process can 10mS. After the first falling edge has been detected, you can load the first data bit on the This bit will be read into the keyboard on the next falling edge, after which you can place data. This process is repeated for the 8 data bits. After the data bits come an Odd Parity



Once the Parity Bit has been sent and the KBD Data Line is in a idle (High) state for the r the keyboard will acknowledge the reception of the new data. The keyboard does this by Data line low for the next clock transition. If the KBD Data line is not idle after the 10th bit

bits + Parity), the keyboard will continue to send a KBD Clock signal until the KBD Data li idle.

nterfacing Example - Keyboard to ASCII Decoder

Normally in this series of web pages, we connect something to the PC, to demonstrate th work. However this poses a problem with the keyboard. What could be possibly want to s computer via the keyboard interface?

Straight away any devious minds would be going, why not a little box, which generates pa could keep sending characters to the computer until it finds the right sequence. Well I'm r encourage what could possibly be illegal practices.

In fact a reasonably useful example will be given using a 68HC705J1A single chip microc will get it to read the data from the keyboard, convert the scan codes into ASCII and senc 232 format at 9600 BPS. However we won't stop here, you will want to see the bi-directio KBD Clock & Data lines, thus we will use the keyboards status LEDS, Num Lock, Caps L Lock.

This can be used for quite a wide range of things. Teamed up with a reasonably sized 4 li character LCD panel, you could have yourself a little portable terminal. Or you could use microcontroller development system. The 68HC705J1A in a One Time Programmable (O fraction of the cost of a 74C922 keyboard decoder chip, which only decodes a 4 x 4 matri binary.

The keyboard doesn't need to be expensive either. Most people have many old keyboard around the place. If it's an AT Keyboard, then use it (XT keyboards will not work with this ever see the introduction of USB keyboards, then there could be many redundant AT key waiting for you to hook them up.

Features

Before we start with the technical aspects of the project, the salesman in me wants to tell features packed into the 998 bytes of code.

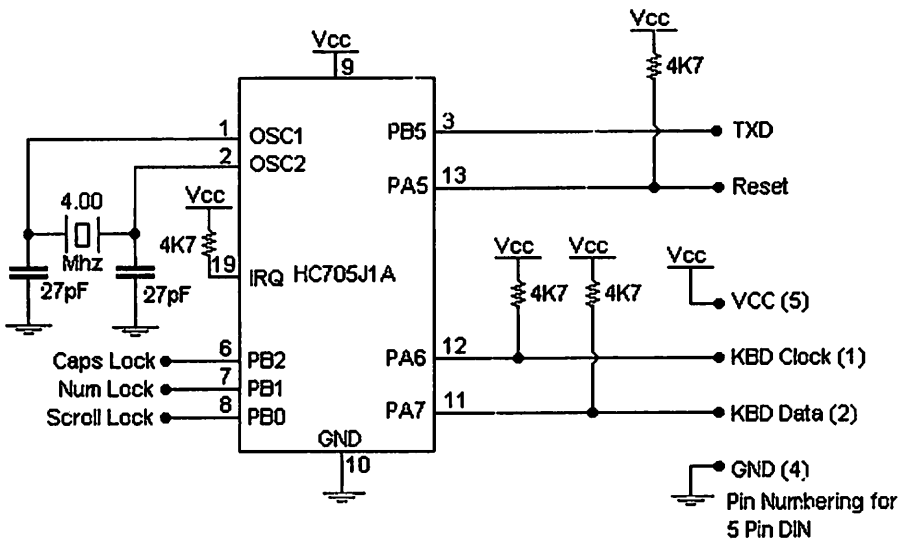
- Use of the keyboard's bi-directional protocol allowing the status of the Num Lock, C Scroll Lock to be displayed on the Keyboards LEDs.
- External Reset Line activated by ALT-CTRL-DEL. If you are using it with a Microcor development system, you can reset the MCU with the keyboard. *I've always wantec use the three fingered solute on the HC11!*
- Scroll Lock and Num Lock toggles two Parallel Port Pins on the HC705. This can be things on or off, Select Memory Pages, Operating Systems etc
- "ALTDEC" or what I call the Direct Decimal Enter Routine. Just like using a PC, whe

decimal number when holding down one of the ALT keys the number is sent as bin system. E.g. If you press and hold down ALT, then type in 255 and release ALT, the will be sent to the system. *Note. Unlike the PC, you can use both the numeric keyp numbers along the top of the keyboard.*

- "CTRLHEX" or you guessed it, Direct Hexadecimal Enter Routine. This function is n the PC. If you hold CTRL down, you can enter a Hexadecimal number. Just the thin Development Systems or even debugging RS-232 Comms?
- Output is in ASCII using a RS-232 format at 9600 BPS. If using it with a developme can tap it in after the RS-232 Line Transceivers to save you a few dollars on RS-23 Converters.

Schematic & Hardware

The schematic below, shows the general connections of the keyboard to the HC705.



The TXD pin, while it transmits in RS-232 format, is not at RS-232 Voltage Levels. If you it to RS-232 Devices then you will need to attach a RS-232 Level Converter of some kind using it with a development system, you can bypass both RS-232 Level Converters and c directly to the RXD pin of the MCU. However the keyboard can't be a direct replacement a development system, unless you want to type in your code each time! You may want to or switch inline to switch between your RS-232 Port and the Keyboard.

The Keyboard requires open collector/open drain outputs. This is achieved by using the D Register (DDR). A zero is written to the port which is internally latched. The DDR is then the line from logic 0 to high impedance. If the port pin is an output, a logic zero will be pre if the port is set to be an input, the port will be high impedance which is pulled high by the resistors.

The circuit is designed to run on a 4Mhz crystal (2Mhz Bus Speed). The timing for the RS transmission is based on the bus speed, thus this crystal has to be 4 Mhz. If you are luck

have a 4 Mhz E Clock on your development system you can use it.

The power supply can also create a slight problem. A standard keyboard can drain about thus it would be recommended to use it's own regulator rather than taking a supply from e Decoupling capacitors are not shown on the general schematic but are implied for reliable Consult your MC68HC705J1A Technical Data Manual for more Information.

Reading Bytes from the Keyboard.

Now it is time to look at the code. I cannot include a description of all the code in this artic is just on 19 pages. Most of it (hopefully) is easy to follow. (Just like other good code, cou of spelling errors while you are at it!)

Remember the KBD Clock line? If you take it low, the keyboard will buffer any keys press Keyboard will only attempt to send when both the Data and Clock lines are idle (high). As considerable time to decode the keys pressed, we must stop the keyboard from sending some of the data may be lost or corrupted.

```
Receive  ldx     #08                    ;Number of Bits
         clr     PAR                    ;Clear Parity Register
         bclr    clk,DDRA               ;Clear to Send

         brset   clk,PORTA,*            ;wait on idle Clock
         brset   data,PORTA,Receive     ;False Start Bit, Restart
```

The program, will keep the KBD Clock line low, unless it is ready to accept data. We will retrieve the data bits from the keyboard, thus we will load index register X with the numbe want to receive. PAR will be used to verify the parity bit at the end of the transmission. W first.

We can then place the KBD Clock line in the idle state so that the keyboard will start tran key has been pressed. The program then loops while the clock line is Idle. If the KBD clo loop is broken and the KBD Data pin is read. This should be the start bit which should be branch to the start of the receive routine and try again.

```
Recdata  ror     byte
         jsr     highlow                ;Wait for high to low Transition
         brset   data,PORTA,Recset
         bclr    7,byte
         jmp     Recnext
Recset   bset    7,byte
         inc     PAR
Recnext  decx
         bne     Recdata                ;Loop until 8 bits been received
```

Once the start bit has been detected, the 8 data bits must follow. The data is only valid or edge of the clock. The subroutine highlow shown below will wait for the falling edge of the

```
highlow brclr   clk,PORTA,*             ;Loop until Clk High
        brset   clk,PORTA,*             ;Loop until Clk Low
        rts
```

After the falling edge we can read the level of the KBD Data line. If it is high we can set th byte or if it is clear, we can clear it. You will notice if the bit is set, we also increment PAR track of the number of 1's in the byte and thus can be used to verify the Parity Bit. Index r decremented as we have read a bit. It then repeats the above process, until the entire 8 b read.

```
        lda         PORTA           ; MSb is Parity.
        rola                        ; Shift MSbit to LSbit.
        rola                        ; thru carry
        eor         PAR
        and         #$01
        beq         r_error
```

After the 8 data bits, comes the dreaded parity bit. We could ignore it if we wanted to, but do something about it. We have been keeping a tally of the number of 1's in PAR. The ke odd parity, thus the parity bit should be the complement of the LSbit in memory location, I exclusive OR-ing PAR with the Parity Bit, we get a 1 if both the bits are different. I.e a '1' i checks out.

As we are only interested in the LSbit we can quite happy XOR the accumulator with PAF single out the LSb using the AND function. If the resultant is zero, then a parity error has the program branches to r_error.

```
        jsr     highlow
        brclr   data,PORTA,r_error      ;Stop Bit Detection

        bset    clk,DDRA                ;Prevent Keyboard from sending data
                                        ;(Clear to Send)
        rts
```

After the Parity Bits comes the Stop Bit. Once again we can ignore it if we desire. Howev chosen to branch to an error routine if this occurs. The stop bit should be set, thus an err it is clear.

```
r_error lda     #$FE                    ;Resend
        sta     byte
        jsr     Transmit
        jmp     Receive                 ;Try again
```

What you do as error handling is up to you. In most cases it will never be executed. In fac know if the above error handling routine works. I need to program another HC705 to senc bit. I've tried it out in close proximity to the Washing Machine, but I really need a controlle

When an error occurs in the Parity or Stop Bit we should assume that the rest of the byte errors as well. We could ignore the error and process the received byte, but it could have results. Instead the keyboard has a resend command. If we issue a resend (FE) to the ke keyboard should send the byte back again. This is what occurs here.

You may notice that we branch to the error routine which transmits a resend command st without waiting for the corrupt transmission to finish. This is not a problem, as the keyboa any transmission to be successful, if the 10th bit is sent, i.e. the parity bit. If we interrupt tl before the parity bit is sent, the keyboard will place the current byte in it's buffer for later t

Reading a byte doesn't really require bi-directional data and clock lines. If you can proces enough then no handshaking (RTS) is required. This means you no longer need to fiddle Direction Register. I have successfully done this with the HC705, outputting only scan co bus. But as you can imagine, you must be quick in order to catch the next transmission.

Writing Bytes to the Keyboard.

The following routine given here is a generic one which can be used for your own purpos normal execution of this program the KBD clock line should be low, to prevent data being MCU isn't ready for it. However in this example, we take low the KBD clock line and wait which is pointless as the line is already low and has been like this for quite some time, sir the last transmission or reception.

```
transmit ldx     #$08                    ;8 Data Bits
         bset    clk,DDRA                ;Set Clock Low
         lda     #$13                    ;Delay 64uS
         jsr     delay
         clra                            ;Clear Parity Register
         bset    data,DDRA               ;Set Data Low
         bclr    clk,DDRA                ;Release Clock Line
         jsr     highlow
```

The program then initiates the Host to Keyboard transmission by taking the KBD data line releasing the KBD clock line. We must then wait for a high to low transition on the KBD cl load the first bit on the KBD data line.

```
loop     ror     byte
         bcs     mark
space    bset    data,DDRA               ; Clear Bit
         jmp     next
mark     bclr    data,DDRA               ; Clear Bit
         inca                            ; Parity Calculation
next     jsr     highlow                 ; Wait for high to low transition
         decx
         bne     loop
```

The loading of the individual bits on the KBD data line is done in very similar fashion to th The X register is used to keep track of the number of bits sent. Also simular to the read c increment the accumulator so we can calculate the parity bit later on.

```
         and     #$01
         bne     clr_par
set_par  bclr    data,DDRA
         jmp     tr_ackn
clr_par  bset    data,DDRA
tr_ackn  jsr     highlow
```

After the data bits have been sent, it is now time to send the parity bit. Unlike the read cy ignore the parity bit. If we do the keyboard will issue a resend (FE) command if the parity a 50% probability!

```
         bclr    data,DDRA               ;Release Data Line
```

```
        jsr     highlow
        brset   data,PORTA,error        ;Check for Ack
        brclr   clk,PORTA,*             ;Wait for idle line

        bset    clk,DDRA                ;Prevent Keyboard from sending data
                                        ;(Clear to Send)
        rts
```

Once the Parity bit has been set and the falling edge of the KBD clock detected, we must KBD data line, and wait for another falling edge of the KBD clock to see if the Keyboard h acknowledged the byte. The keyboard does this by pulling the KBD data line low. If it is n program branches to an error handler. If all has been successful, the MCU pulls down the prevent it from transmitting.

```
error   lda     #$FF        ;Reset
        sta     byte
        jsr     transmit
        rts
```

We have taken a harsher approach to handing any transmit errors. Ideally we should wai keyboard to send a resend command and then retransmit the byte. However what we ha issue a reset to the keyboard. So far I've never had an error, however if this starts to bec then a better error handler could be written.

Download Source Code

- Download Keybrd05.zip - Source code for 68HC705J1A (20,604 Bytes)
- View .Lst (List) File

Links to other information.

- Two Line Mini-Terminal — Roger Schaefer has developed a Mini RS-232 Terminal using the 6 input device the terminal uses a **standard IBM compatible PC key** normal full duplex mode the controller converts the keyboard scan c and transmits them to the RS-232 output. Input from the RS-232 is c LCD.

Copyright 1999-2001 Craig Peacock - 19th August 2001.

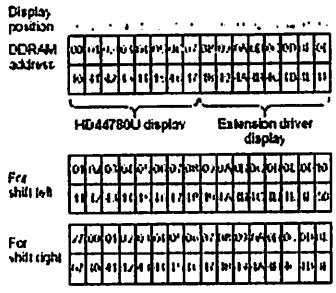
M1632 MODULE LCD 16 X 2 BARIS (M1632)

Deskripsi:

M1632 adalah merupakan modul LCD dengan tampilan 16 x 2 baris dengan konsumsi daya y rendah. Modul ini dilengkapi dengan mikrokontroler yang didisain khusus untuk mengendalikan L(Mikrokontroler HD44780 buatan Hitachi yang berfungsi sebagai pengendali LCD ini mempunyai CGR((Character Generator Read Only Memory), CGRAM (Character Generator Random Access Memory) DDRAM (Display Data Random Access Memory).

DDRAM

DDRAM adalah merupakan memori tempat karakter yang ditampilkan berada. Contoh, ur karakter 'A' atau 41H yang ditulis pada alamat 00, maka karakter tersebut akan tampil pada baris pert dan kolom pertama dari LCD. Apabila karakter tersebut ditulis di alamat 40, maka karakter tersebut a tampil pada baris kedua kolom pertama dari LCD.



Gambar 1

DDRAM M1632 (diambil dari data sheet HD44780)

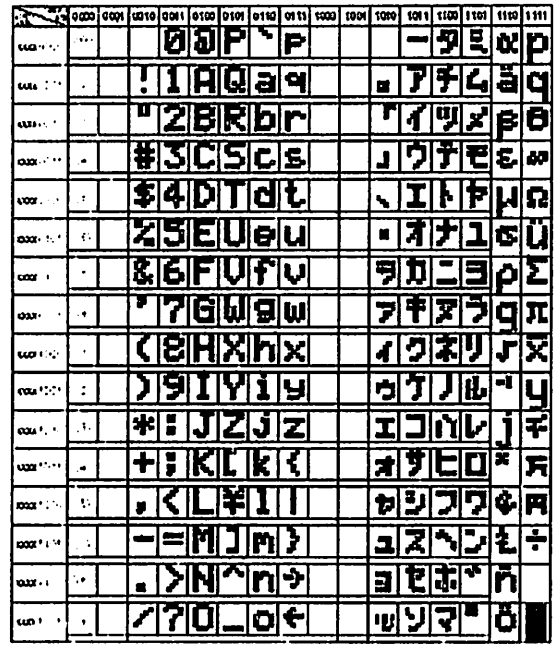
CGRAM

CGRAM adalah merupakan memori untuk menggambarkan pola sebuah karakter di m bentuk dari karakter dapat diubah-ubah sesuai keinginan. Namun memori ini akan hilang saat power su tidak aktif, sehingga pola karakter akan hilang.

CGROM

CGROM adalah merupakan memori untuk menggambarkan pola sebuah karakter di mana tersebut sudah ditentukan secara permanen dari HD44780 sehingga pengguna tidak dapat mengubah Namun karena ROM bersifat permanen, maka pola karakter tersebut tidak akan hilang walaupun po supply tidak aktif

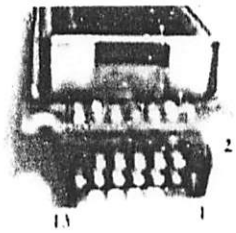
Pada gambar 2, tampak terlihat pola-pola karakter yang tersimpan dalam lokasi-lokasi tert dalam CGROM. Pada saat HD44780 akan menampilkan data 41H yang tersimpan pada DDRAM, m HD44780 akan mengambil data di alamat 41H (0100 0001) yang ada pada CGROM yaitu pola karakter A



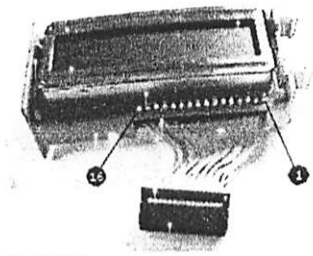
Gambar 2
Hubungan antara CGROM dan DDRAM (diambil dari data sheet HD44780)

Pin Out

No	Nama Pin	Deskripsi
1	VCC	+5V
2	GND	0V
3	VEE	Tegangan Kontras LCD
4	RS	Register Select, 0 = Register Perintah, 1 = Register I
5	R/W	1 = Read, 0 = Write
6	E	Enable Clock LCD, logika 1 setiap kali pengiriman a pembacaan data
7	D0	Data Bus 0
8	D1	Data Bus 1
9	D2	Data Bus 2
10	D3	Data Bus 3
11	D4	Data Bus 4
12	D5	Data Bus 5
13	D6	Data Bus 6
14	D7	Data Bus 7
15	Anoda (Kabel coklat untuk LCD Hitachi)	Tegangan positif backlight
16	Katoda (Kabel merah untuk LCD Hitachi)	Tegangan negatif backlight



Gambar 3
Pin Out M1632 LCD Hitachi



Gambar 4
Pin Out LCD M1632 Standard

Register

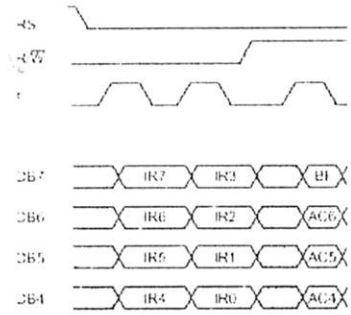
HD44780, mempunyai dua buah Register yang aksesnya diatur dengan menggunakan kaki Pada saat RS berlogika 0, maka register yang diakses adalah Register Perintah dan pada saat RS berlog 1, maka register yang diakses adalah Register Data

Register Perintah

Register ini adalah register di mana perintah-perintah dari mikrokontroler ke HD44780 pada : proses penulisan data atau tempat status dari HD44780 dapat dibaca pada saat pembacaan data.

Penulisan Data ke Register Perintah

Penulisan data ke Register Perintah dilakukan dengan tujuan mengatur tampilan LCD, inisiali dan mengatur Address Counter maupun Address Data. Gambar 5 menunjukkan proses penulisan data register perintah dengan menggunakan mode 4 bit interface. Kondisi RS berlogika 0 menunjukkan ak data ke Register Perintah. R/W berlogika 0 yang menunjukkan proses penulisan data akan dilakukan. Nib tinggi (bit 7 sampai bit 4) terlebih dahulu dikirimkan dengan diawali pulsa logika 1 pada E Clo Kemudian Nibble rendah (bit 3 sampai bit 0) dikirimkan dengan diawali pulsa logika 1 pada E Clock l Untuk mode 8 bit interface, proses penulisan dapat langsung dilakukan secara 8 bit (bit 7 ... bit 0) diawali sebuah pulsa logika 1 pada E Clock.



Gambar 5
Timing diagram Penulisan Data ke Register Perintah Mode 4 bit Interface

Tabel 1
Perintah-perintah M1632

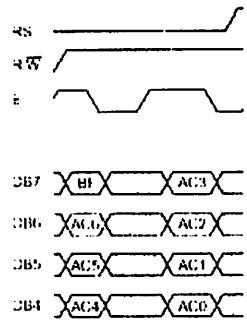
Perintah	D7	D6	D5	D4	D3	D2	D1	D0	Deskripsi
Hapus Display	0	0	0	0	0	0	0	1	Hapus Display dan DDRAM
Posisi Awal	0	0	0	0	0	0	1	X	Set Alamat DDRAM di 0
Set Mode	0	0	0	0	0	1	I/D	S	Atur arah pergeseran cursor dan displ

Display On/OFF	0	0	0	0	1	D	C	B	Atur display (D) On/OFF, cursor ON/OFF, Blinking (B)
Geser Cursor/Display	0	0	0	1	S/C	R/L	X	X	Geser Cursor atau display tanpa men alamat DDRAM
Set Fungsi	0	0	1	DL	N	F	X	X	Atur panjang data, jumlah baris tampil, dan font karakter
Set Alamat CGRAM	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Data dapat dibaca atau ditulis se alamat diatur
Set Alamat DDRAM	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Data dapat dibaca atau ditulis se alamat diatur

X = diabaikan
I/D 1 Increment, 0 Decrement
S 0=Display tidak geser
S/C 1=Display Shift, 0=Geser Cursor
R/L 1=Geser Kiri, 0=Geser Kanan
DL 1=8 bit, 0=4bit
N 1 2 baris, 0 1 baris
F 1 5x10, 0 5x8
D 0=Display OFF, 1=Display ON
C 0=Cursor OFF, 1=Cursor ON
B 0=Blinking OFF, 1=Blinking ON

Pembacaan Data dari Register Perintah

Proses pembacaan data pada register perintah biasa digunakan untuk melihat status busy dari L atau membaca Address Counter. RS diatur pada logika 0 untuk akses ke Register Perintah, R/W diatur p logika 1 yang menunjukkan proses pembacaan data. 4 bit nibble tinggi dibaca dengan diawali pulsa log 1 pada E Clock dan kemudian 4 bit nibble rendah dibaca dengan diawali pulsa logika 1 pada E Cl Untuk Mode 8 bit interface, pembacaan 8 bit (nibble tinggi dan rendah) dilakukan sekaligus dengan diav sebuah pulsa logika 1 pada E Clock.



Gambar 6
Timing Diagram Pembacaan Register Perintah Mode 4 bit Interface

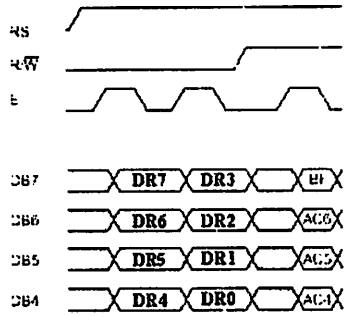
Register Data

Register ini adalah register di mana mikrokontroler dapat menuliskan atau membaca data ke dari DDRAM. Penulisan data pada register ini akan menempatkan data tersebut ke DDRAM sesuai den alamat yang telah diatur sebelumnya

Penulisan Data ke Register Data

Penulisan data pada Register Data dilakukan untuk mengirimkan data yang akan ditampilkan pa LCD. Proses diawali dengan adanya logika 1 pada RS yang menunjukkan akses ke Register Data, kondisi R/W diatur pada logika 0 yang menunjukkan proses penulisan data. Data 4 bit nibble tinggi (bit 7 hingga

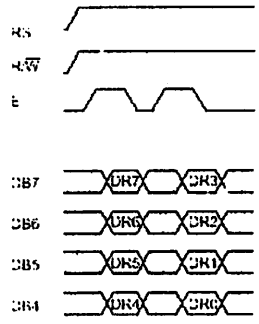
bit 4) dikirim dengan diawali pulsa logika 1 pada sinyal E Clock dan kemudian diikuti 4 bit nibble rendah (bit 3 hingga bit 0) yang juga diawali pulsa logika 1 pada sinyal E Clock.



Gambar 7
Timing Diagram Penulisan Data ke Register Data Mode 4 bit Interface

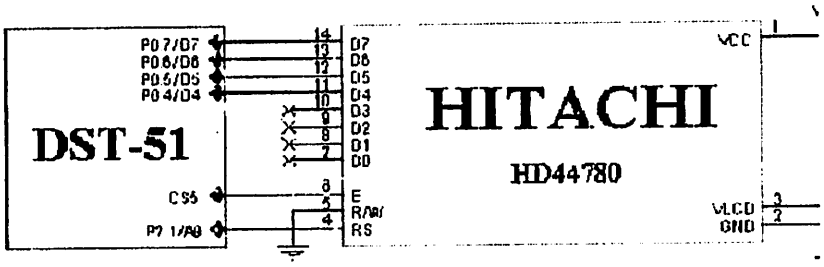
Pembacaan Data dari Register Data

Pembacaan data dari Register Data dilakukan untuk membaca kembali data yang tampil p LCD. Proses dilakukan dengan mengatur RS pada logika 1 yang menunjukkan adanya akses ke Regi Data. Kondisi R/W diatur pada logika tinggi yang menunjukkan adanya proses pembacaan data. Data 4 nibble tinggi (bit 7 hingga bit 4) dibaca dengan diawali adanya pulsa logika 1 pada E Clock dan dilanjut dengan data 4 bit nibble rendah (bit 3 hingga bit 0) yang juga diawali dengan pulsa logika 1 pada E Clock

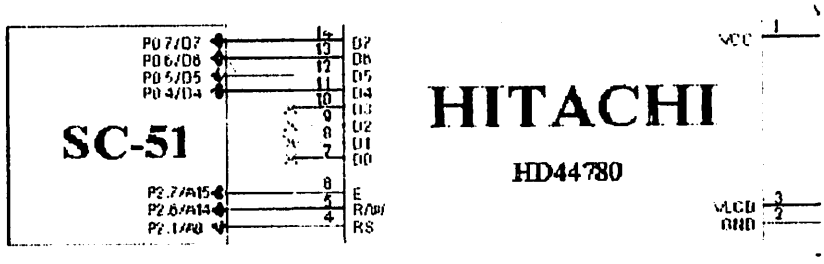


Gambar 8
Timing Diagram Pembacaan Data dari Register Data Mode 4 bit Interface

Antar muka LCD dengan mikrokontroler



Gambar 9
Antar muka dengan Modul DST-51



Gambar 10
Antar Muka dengan Modul SC-51 atau AT8951

Program
Rutin-rutin Program untuk DST-51 yang diassembly dengan [illegible] atau [illegible]
Rutin-rutin Program untuk SC-51/AT8951 yang diassembly dengan [illegible] atau [illegible]
Rutin delay yang diassembly dengan [illegible] atau [illegible]
Datasheet [illegible]

Allt mellan antenn och jord

Datum 970925

PRODUKTINFORMATION FRÅN

ELFA

HÄMTFAX +46 8 735 35 33
FAX ON DEMAND +46 8 735 35 29
INTERNET http://www.elfa.se
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Antal sidor: 21

LFA artikelnr.

3-107-09 ISD1416P Ljudlagringskrets
3-107-17 ISD1416G Y Ljudlagringskrets
73-107-25 ISD1420P Ljudlagringskrets
73-107-33 ISD1420G Y Ljudlagringskrets

ISD1400 Series

Single-Chip Voice Record/Playback Devices 16- and 20-Second Durations

FEATURES

- Easy-to-use single-chip voice Record/Playback solution
- High-quality, natural voice/audio reproduction
- Push-button interface
  - Playback can be edge- or level-activated
- Single-chip durations of 16 and 20 seconds
- Automatic power-down mode
  - Enters standby mode immediately following a Record or Playback cycle
  - Standby current 0.5 µA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100K record cycles (typical)
- On-chip clock source
- No programmer or development system needed
- Single +5 volt power supply
- Available in die form, DIP, and SOIC packaging
- Industrial temperature (−40°C to +85°C) versions available

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ISD1400 SERIES SUMMARY

Part Number	Minimum Duration (Seconds)	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD1416	16	8.0	3.3
ISD1420	20	6.4	2.6

GENERAL DESCRIPTION

Information Storage Devices' ISD1400 ChipCorder® Series provides high-quality, single-chip record/playback solutions to short-duration messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, and speaker amplifier. A minimum record/playback subsystem can be configured with a microphone, a speaker, several passives, two push-buttons, and a power source.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

DETAILED DESCRIPTION

Speech/Sound Quality

The ISD1400 Series includes devices offered at 6.4 and 8.0 KHz sampling frequencies, allowing the user a choice of speech quality options. The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state digital solutions.

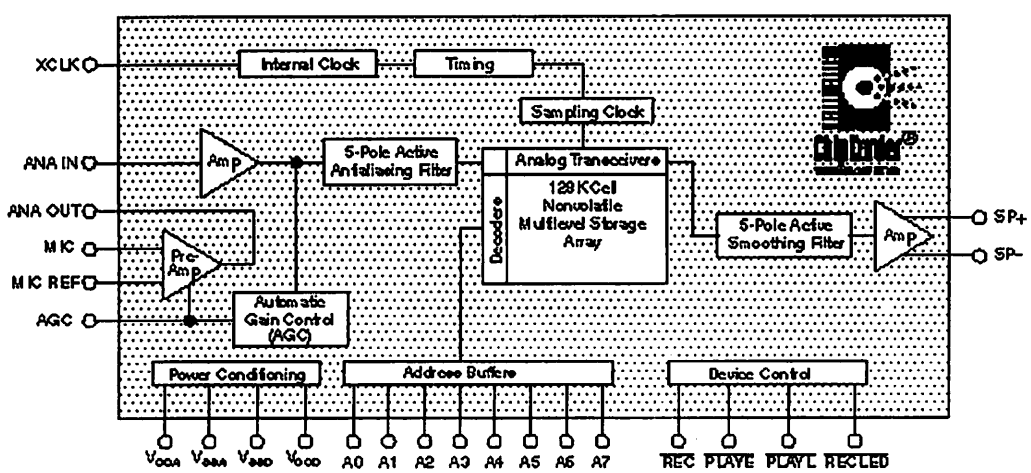
Duration

To meet end system requirements, the ISD1400 Series offers single-chip solutions at 16 and 20 seconds.

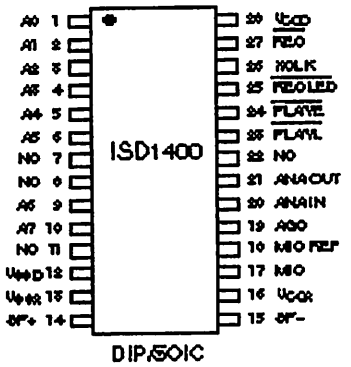
EEPROM Storage

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

ISD1400 SERIES BLOCK DIAGRAM



ISD1400 SERIES PINOUTS



NOTE: NC means Must Not Connect.

Basic Operation

The ISD1400 ChipCorder Series devices are controlled by a single Record signal, $\overline{REC}$, and either of two push-button control playback signals, $\overline{PLAYE}$ (edge-activated playback), and $\overline{PLAYL}$ (level-activated playback). The ISD1400 parts are configured for simplicity of design in a single-message application. Using the address lines will allow multiple message applications. Device operation is explained on page 2-75.

Automatic Power-Down Mode

At the end of a Playback or Record cycle, the ISD1400 Series devices automatically return to a low-power standby mode, consuming typically 0.5 µA. During a Playback cycle, the device powers down automatically at the end of the message. During a Record cycle, the device powers down immediately after $\overline{REC}$ is released HIGH.

Addressing (optional)

In addition to providing simple message playback, the ISD1400 Series provides a full addressing capability.

The ISD1400 Series storage array has 160 distinct addressable segments, providing the following resolutions. See Chapter 5, Application Information for ISD1400 address tables.

Part Number	Minimum Duration (Seconds)
ISD1416	100 ms
ISD1420	125 ms

PIN DESCRIPTION

NOTE

The $\overline{REC}$ signal is debounced for 50 ms on the rising edge to prevent a false retriggering from a push-button switch.

Voltage Inputs (V_{CCA}, V_{CCD})

Analog and digital circuits internal to the ISD1400 Series use separate power buses to minimize noise on the chip. These power buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the power supply be decoupled as close as possible to the package.

Ground Inputs (V_{SSA}, V_{SSD})

Similar to V_{CCA} and V_{CCD}, the analog and digital circuits internal to the ISD1400 Series use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.

Record ($\overline{REC}$)

The $\overline{REC}$ input is an active-LOW Record signal. The device records whenever $\overline{REC}$ is LOW. This signal must remain LOW for the duration of the Recording. $\overline{REC}$ takes precedence over either Playback ($\overline{PLAYE}$ or $\overline{PLAYL}$) signal. If $\overline{REC}$ is pulled LOW during a Playback cycle, the Playback immediately ceases and Recording begins.

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A Record cycle is completed when $\overline{REC}$ is pulled HIGH or the memory space is filled.

An end-of-message marker (EOM) is internally recorded, enabling a subsequent Playback cycle to terminate appropriately. The device automatically powers down to standby mode when $\overline{REC}$ goes HIGH.

Playback, Edge-Activated (PLA$\overline{YE}$)

When a LOW-going transition is detected on this input signal, a Playback cycle begins. Playback continues until an end-of-message (EOM) is encountered or the end of the memory space is reached. Upon completion of the Playback cycle, the device automatically powers down into standby mode. Taking $\overline{PLAYE}$ HIGH during a Playback cycle will not terminate the current cycle.

Playback, Level-Activated (PLA$\overline{YL}$)

When this input signal transitions from HIGH to LOW, a Playback cycle is initiated. Playback continues until $\overline{PLAYL}$ is pulled HIGH, an EOM marker is detected, or the end of the memory space is reached. The device automatically powers down to standby mode upon completion of the Playback cycle.

NOTE

In Playback, if either $\overline{PLAYE}$ or $\overline{PLAYL}$ is held LOW during EOM or OVERFLOW, the device will still enter standby and the internal oscillator and timing generator will stop. However, the rising edge of $\overline{PLAYE}$ and $\overline{PLAYL}$ are not debounced and any subsequent falling edge (particularly switch bounce) present on the input pins will initiate another Playback.

Record LED Output ($\overline{RECLED}$)

The output $\overline{RECLED}$ is LOW during a Record cycle. It can be used to drive an LED to provide feedback that a Record cycle is in progress. In addition, $\overline{RECLED}$ pulses LOW momentarily when an EOM is encountered in a Playback cycle.

Microphone Input (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from -15 to 24 dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 K Ohm resistance on this pin, determine the low-frequency cutoff for the ISD1400 Series passband. See Chapter 5, Application Information for additional information on low-frequency cutoff calculations.

Microphone Reference (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected differentially to a microphone.

Automatic Gain Control (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of sound, from whispers to loud sounds, to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C6 on the schematic on page 2-75) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R5) and an external capacitor (C6) connected in parallel between the AGC Pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases.

Analog Output (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

Analog Input (ANA IN)

The ANA IN pin transfers the input signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

External Clock Input (XCLK)

The external clock input for the ISD1400 devices has an internal pull-down device. The ISD1400 is configured at the factory with an internal sampling clock frequency that guarantees its minimum nominal record/playback time. For instance, an ISD1420 operating within specification will be observed to always have a minimum of 20 seconds of recording time. The sampling frequency is then maintained to a variation of ±2.25% over the commercial temperature and operating voltage ranges, while still maintaining the minimum specified recording duration. This will result in some devices having a few percent more than nominal recording time.

The internal clock has a ±5% tolerance over the industrial temperature and voltage range. A regulated power supply is recommended for industrial temperature parts. If greater precision is required, the device can be clocked through the XCLK pin as follows:

Part Number	Sample Rate	Required Clock
ISD1416	8.0 KHz	1024 KHz
ISD1420	6.4 KHz	819.2 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. ***IF THE XCLK IS NOT USED, THIS INPUT SHOULD BE CONNECTED TO GROUND.***

Speaker Outputs (SP+, SP–)

The SP+ and SP– pins provide direct drive for loudspeakers with impedances as low as 16 ohms. A single output may be used, but, for direct-drive loudspeakers, the two opposite-polarity outputs provide an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP+ and SP– are used, a speaker-coupling capacitor is not required. A single-ended connection will require an AC-coupling capacitor between the SP pin and the speaker. The speaker outputs are in a high-impedance state during a record cycle, and hold at V_{SSA} during Power Down.

Address Inputs (A0–A7)

The Address Inputs have two functions, depending upon the level of the two Most Significant Bits (MSB) of the address.

If either of the two MSBs is LOW, the inputs are ***ALL*** interpreted as address bits and are used as the start address for the current Record or Playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of $\overline{PLAYE}$, $\overline{PLAYL}$, or $\overline{REC}$.

OPERATIONAL MODES

The ISD1400 Series is designed with several built-in operational modes provided to allow maximum functionality with a minimum of additional components, described in detail below. The operational modes use the address pins on the ISD1400 devices, but are mapped outside the valid address range. When the two Most Significant Bits

(MSBs) are HIGH (A6 and A7), the remaining address signals are interpreted as mode bits and not as address bits. Therefore, operational modes and direct addressing are ***NOT*** compatible and cannot be used simultaneously.

There are two important considerations for using operational modes. First, all operations begin initially at address 0, which is the beginning of the ISD1400 address space. Later operations can begin at other address locations, depending on the operational mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from Record to Playback but not from Playback to Record when A4 is HIGH in Operational Mode.

Second, an Operational Mode is executed when any of the control inputs, $\overline{PLAYE}$, $\overline{PLAYL}$, or $\overline{REC}$, go LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going control input signal, at which point the current address/mode levels are sampled and executed.

NOTE

The two MSBs are on pins 9 and 10 for each ISD1400 Series device.

OPERATIONAL MODES DESCRIPTION

The Operational Modes can be used in conjunction with a microcontroller, or they can be hard-wired to provide the desired system operation.

A0 — Message Cueing

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each control input LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for Playback only, and is typically used with the A4 Operational Mode.

A1 — Delete EOM Markers

The A1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one EOM marker set at the end of the final message. When this operational mode is configured, messages recorded sequentially are played back as one continuous message.

OPERATIONAL MODES TABLE

Address Crtl. (HIGH)	Function	Typical Use	Jointly Compatible*
A0	Message cueing	Fast-forward through messages	A4
A1	Delete EOM markers	Position EOM marker at the end of the last message	A3, A4
A2	Unused		
A3	Looping	Continuous playback from Address 0	A1
A4	Consecutive addressing	Record/Play multiple consecutive messages	A0, A1
A5	Unused		

NOTE: An asterisk (*) indicates additional operational modes which can be used simultaneously with the given mode.

A2 — Unused

A3 — Message Looping

The A3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space.

A message can completely fill the ISD1400 device and will loop from beginning to end. Pulsing $\overline{\text{PLAYE}}$ will start the Playback and pulsing $\overline{\text{PLAYL}}$ will end the Playback.

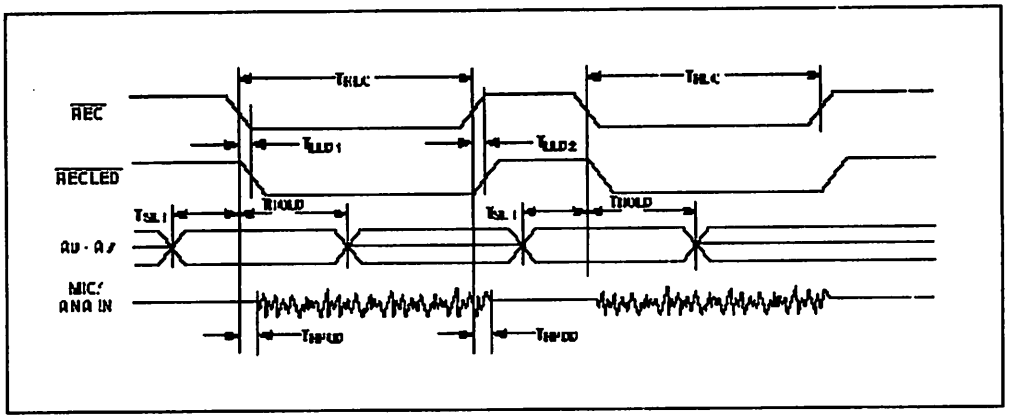
A4 — Consecutive Addressing

During normal operations, the address pointer will reset when a message is played through to an EOM marker. The A4 Operational Mode inhibits the address pointer reset, allowing messages to be recorded or played back consecutively. When the device is in a static state; i.e., not recording or playing back, momentarily taking this pin LOW will reset the address counter to zero.

A5 — Unused

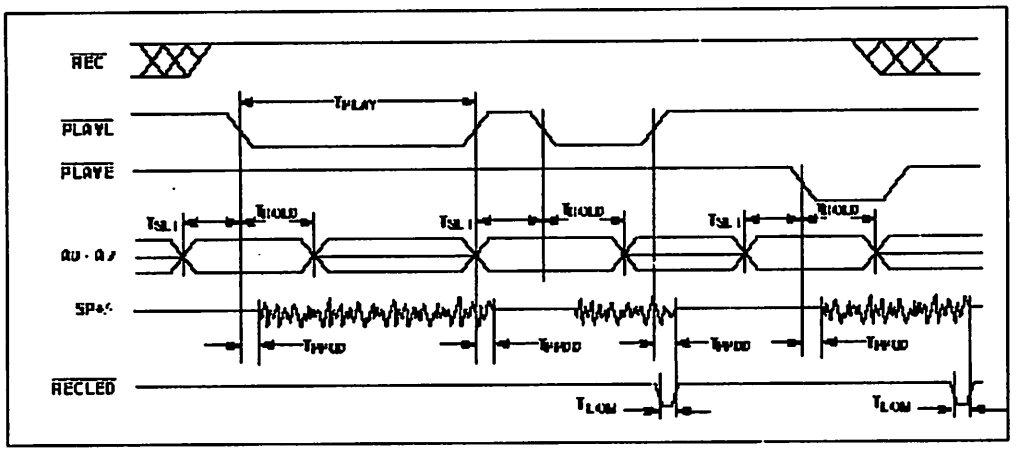
TIMING DIAGRAMS

Record



2

Playback



NOTES: 1. $\overline{\text{REC}}$ must be HIGH for the entire duration of a Playback cycle.
2. $\overline{\text{RECLED}}$ functions as an EOM during Playback.

ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)

Condition	Value
Junction temperature	150° C
Storage temperature range	-65° C to +150° C
Voltage applied to any pin	(V_{SS} -0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} -1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering - 10 seconds)	300° C
V_{CC} - V_{SS}	-0.3 V to + 7.0 V

NOTE: Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

OPERATING CONDITIONS (PACKAGED PARTS)

Condition	Value
Commercial operating temperature(1)	0° C to +70° C
Industrial operating temperature(1)	-40° C to +85° C
Supply voltage (V_{CC})(2)	+4.5 V to +5.5 V
Ground voltage (V_{SS})(3)	0 V

NOTES: 1. Case temperature.
2. V_{CC} = V_{CCA} = V_{CCD}.
3. V_{SS} = V_{SSA} = V_{SSD}.

2

DC PARAMETERS (PACKAGED PARTS)

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = - 1.6 mA
I_{CC}	V_{CC} Current (Operating)		15	30	mA	V_{CC} = 5.5 V (3), R_{EXT} = ∞
I_{SB}	V_{CC} Current (Standby)		0.5	10	µA	(3) (4)
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC} (5)
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	17	KΩ	Pins 17, 18

DC PARAMETERS (PACKAGED PARTS) – CONTINUED

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
$R_{ANA\ IN}$	ANA IN Input Resistance	2.5	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	20	23	26	dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		–45	–15	dB	AGC = 2.5 V
A_{ARP}	ANA IN to SP+/– Gain	20	22	25	dB	
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	
I_{PREH}	Preamp Out Source		–2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} = 2.0 V

NOTES:
1. Typical values @ T_A = 25° C and 5.0 V.
2. All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100% tested.
3. V_{CCA} and V_{CCD} connected together.
4. $\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be at V_{CCD}.
5. XCLK pin.

2

AC PARAMETERS (PACKAGED PARTS)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	— ISD1416 — ISD1420			8 6.4	KHz KHz	(5) (5)
F_{CF}	Filter Pass Band	— ISD1416 — ISD1420		3.3 2.6		KHz KHz	3 dB Roll-Off Point (3)(6) 3 dB Roll-Off Point (3)(6)
T_{REC}	Record Duration	— ISD1416 — ISD1420	16 20			sec sec	
T_{PLAY}	Playback Duration	— ISD1416 — ISD1420	16 20			sec sec	(5) (5)
T_{LED1}	$\overline{RECLED}$ ON Delay			5		msec	
T_{LED2}	$\overline{RECLED}$ OFF Delay	— ISD1416 — ISD1420	30 40	38.9 48.6	95 110	msec msec	
T_{SET}	Address Setup Time		300			nsec	
T_{HOLD}	Address Hold Time		0			nsec	
T_{RPUD}	Rec. Power-Up Delay	— ISD1416 — ISD1420		26 32		msec msec	
T_{RPDD}	Rec. Power-Down Delay	— ISD1416 — ISD1420		26 32		msec msec	

AC PARAMETERS (PACKAGED PARTS) – CONTINUED

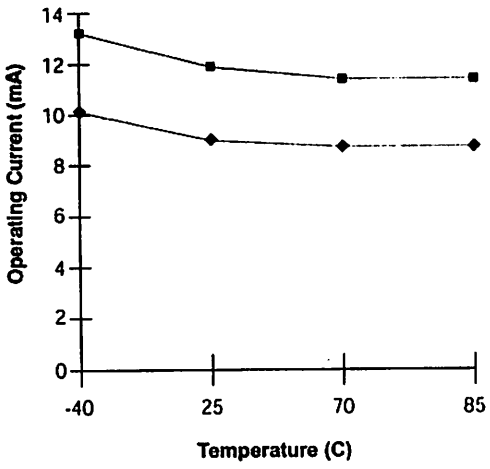
Symbol	Characteristic	Min(2)	Typ (1)	Max(2)	Units	Conditions
T_{PPUD}	Play Power-Up Delay — ISD1416 — ISD1420		26 32		msec msec	
T_{PPDD}	Play Power-Down Delay — ISD1416 — ISD1420		6.5 8.1		msec msec	
T_{EOM}	EOM Pulse Width — ISD1416 — ISD1420		12.5 15.625		msec msec	
THD	Total Harmonic Distortion		1	3	%	@ 1 KHz
P_{OUT}	Speaker Output Power		12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins		1.25	2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage			20	mV	Peak-to-Peak (4)
V_{IN2}	ANA IN Input Voltage			50	mV	Peak-to-Peak

NOTES:
1. Typical values @ T_A = 25° C and 5.0 V.
2. All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100% tested.
3. Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).
4. With 5.1 KΩ series resistor at ANA IN.
5. Sampling frequency and Playback duration will vary as much as ±2.25% over the commercial temperature and voltage ranges. It may vary as much as ±5% over the industrial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum Playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions).
6. Filter specification applies to the antialiasing filter and to the smoothing filter.

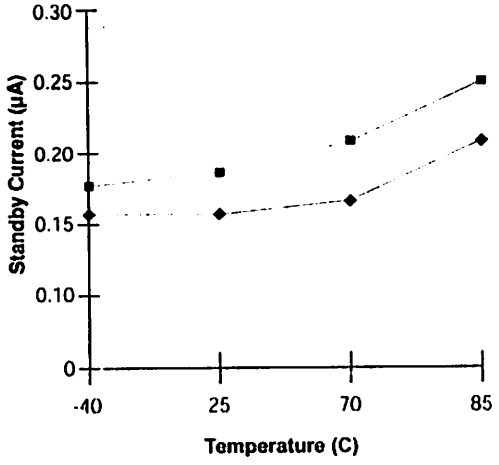
2

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)

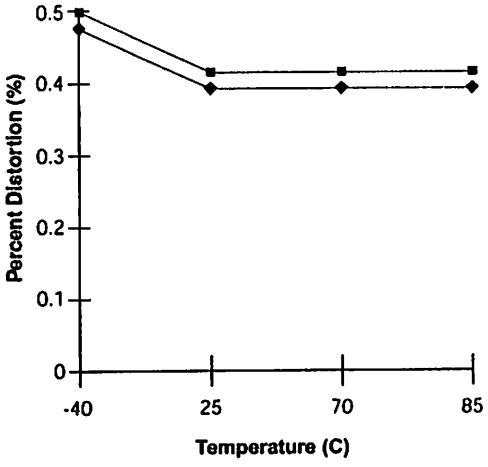
RECORD MODE OPERATING CURRENT (I_{CC})



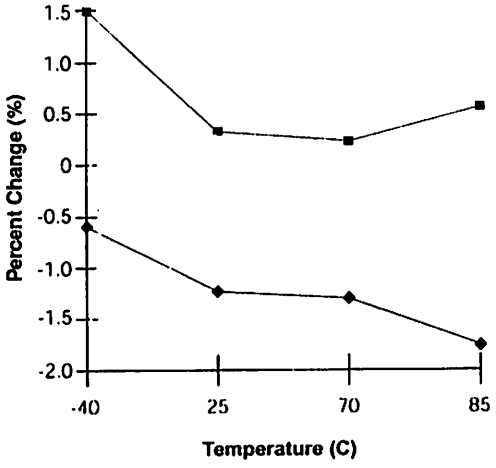
STANDBY CURRENT (I_{SB})



TOTAL HARMONIC DISTORTION



OSCILLATOR STABILITY



■ 5.5 Volts ◆ 4.5 Volts

ABSOLUTE MAXIMUM RATINGS (DIE)

Condition	Value
Junction temperature	150° C
Storage temperature range	-65° C to +150° C
Voltage applied to any pad	(V_{SS} -0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pad (Input current limited to ± 20 mA)	(V_{SS} -1.0 V) to (V_{CC} + 1.0 V)
V_{CC} - V_{SS}	-0.3 V to + 7.0 V

NOTE: Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

OPERATING CONDITIONS (DIE)

Condition	Value
Commercial operating temperature range	0° C to +50° C
Supply voltage (V_{CC})(1)	+4.5 V to +6.5 V
Ground voltage (V_{SS})(2)	0 V

NOTES: 1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.

2

DC PARAMETERS (DIE)

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -1.6 mA
I_{CC}	V_{CC} Current (Operating)		15	30	mA	V_{CC} = 5.5 V (3), $R_{EXT} = \infty$
I_{SB}	V_{CC} Current (Standby)		0.5	10	µA	(3) (4)
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC} (5)
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	17	KΩ	Pins 17, 18

DC PARAMETERS (DIE) – CONTINUED

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
$R_{ANA\ IN}$	ANA IN Input Resistance	2.5	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	20	23	26	dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		-45	-15	dB	AGC = 2.5 V
A_{ARP}	ANA IN to SP+/– Gain	20	22	25	dB	
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	
I_{PREH}	Preamp Out Source		-2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} 2.0 V

NOTES:
1. Typical values @ T_A = 25° C and 5.0 V.
2. All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100% tested.
3. V_{CCA} and V_{CCD} connected together.
4. $\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be at V_{CCD}.
5. XCLK pin.

2

AC PARAMETERS (DIE)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	— ISD1416 — ISD1420			8 6.4	KHz KHz	(5) (5)
F_{CF}	Filter Pass Band	— ISD1416 — ISD1420		3.3 2.6		KHz KHz	3 dB Roll-Off Point (3)(6) 3 dB Roll-Off Point (3)(6)
T_{REC}	Record Duration	— ISD1416 — ISD1420	16 20			sec sec	
T_{PLAY}	Playback Duration	— ISD1416 — ISD1420	16 20			sec sec	(5) (5)
T_{LED1}	$\overline{RECLED}$ ON Delay			5		msec	
T_{LED2}	$\overline{RECLED}$ OFF Delay	— ISD1416 — ISD1420	30 40	38.9 48.6	95 110	msec msec	
T_{SET}	Address Setup Time		300			nsec	
T_{HOLD}	Address Hold Time		0			nsec	
T_{RPUD}	Rec. Power-Up Delay	— ISD1416 — ISD1420		26 32		msec msec	
T_{RPDD}	Rec. Power-Down Delay	— ISD1416 — ISD1420		26 32		msec msec	

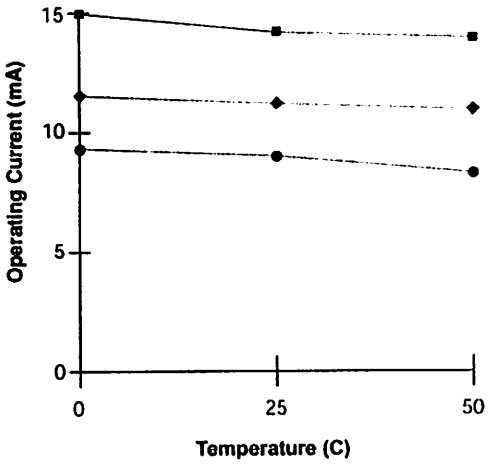
AC PARAMETERS (DIE) – CONTINUED

Symbol	Characteristic	Min(2)	Typ (1)	Max(2)	Units	Conditions
T_{PPUD}	Play Power-Up Delay — ISD1416 — ISD1420		26 32		msec msec	
T_{PPDD}	Play Power-Down Delay — ISD1416 — ISD1420		6.5 8.1		msec msec	
T_{EOM}	EOM Pulse Width — ISD1416 — ISD1420		12.5 15.625		msec msec	
THD	Total Harmonic Distortion		1	3	%	@ 1 KHz
P_{OUT}	Speaker Output Power		12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins		1.25	2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage			20	mV	Peak-to-Peak (4)
V_{IN2}	ANA IN Input Voltage			50	mV	Peak-to-Peak

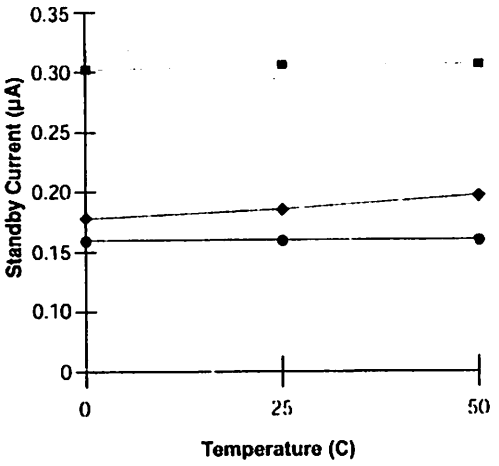
NOTES:
1. Typical values @ T_A = 25° C and 5.0 V.
2. All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100% tested.
3. Low-frequency cutoff depends upon value of external capacitor . (see Pin Descriptions).
4. With 5.1 KΩ series resistor at ANA IN.
5. Sampling frequency and Playback duration will vary as much as ±2.25% over the commercial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum Playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions).
6. Filter specification applies to the antialiasing filter and to the smoothing filter.

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (DIE)

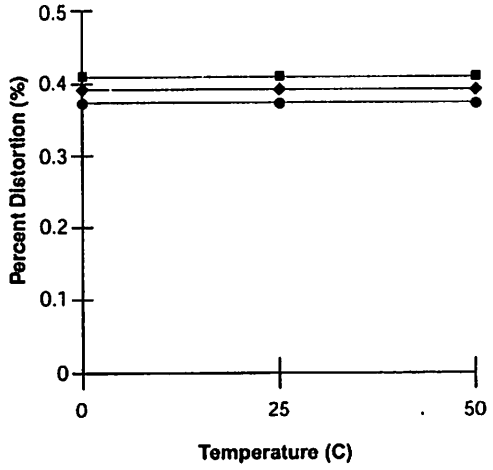
RECORD MODE OPERATING CURRENT (I_{CC})



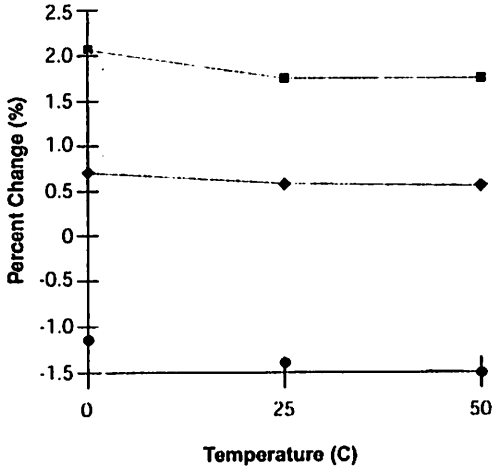
STANDBY CURRENT (I_{SB})



TOTAL HARMONIC DISTORTION

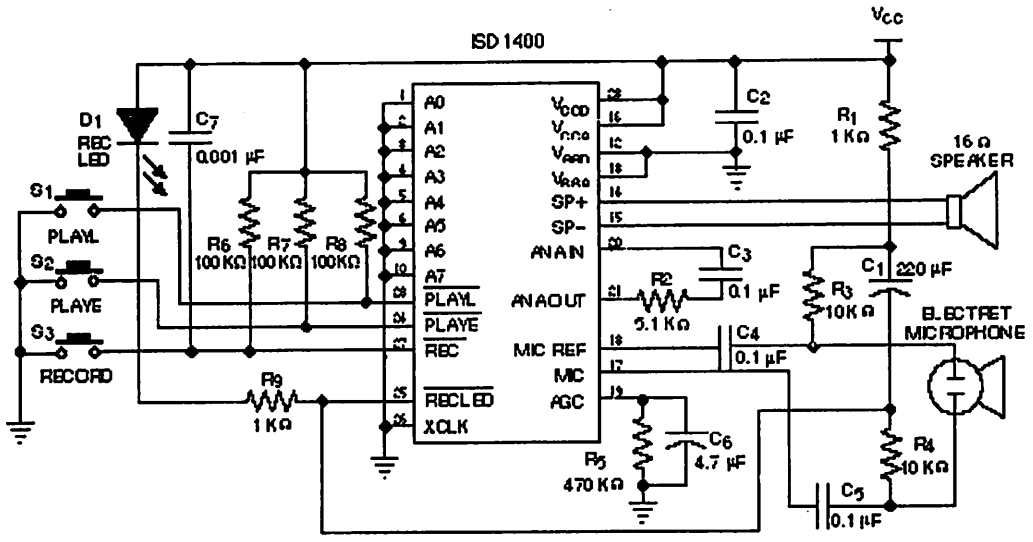


OSCILLATOR STABILITY



■ 6.5 Volts ◆ 5.5 Volts ● 4.5 Volts

APPLICATION EXAMPLE



FUNCTIONAL DESCRIPTION EXAMPLE

The following example operating sequence demonstrates the functionality of the ISD1400 Series devices.

1. **Record a message filling the address space.**

   Pulling the $\overline{REC}$ signal LOW initiates a Record cycle from the beginning of the message space. If $\overline{REC}$ is held LOW, the Recording continues until the message space has been filled. Once the message space is filled, Recording ceases. The device will automatically power down after $\overline{REC}$ is pulled HIGH.

2. **Edge-activated playback.**

   Pulling the $\overline{PLAYE}$ signal LOW initiates a Playback cycle from the beginning of the message space or at a selected location. The rising edge of $\overline{PLAYE}$ has no effect on operation. If a Recording has filled the message space, the entire message is played. When the device reaches the EOM marker, it automatically powers down. A subsequent falling edge on $\overline{PLAYE}$ initiates a new Play cycle from the start address.

3. **Level-activated playback.**

   Pulling the $\overline{PLAYL}$ signal LOW initiates a Playback cycle from the beginning of the message space or a selected location. If Recording has filled the message space, the entire message is played. When the device reaches the EOM marker, it automatically powers down. A subsequent falling edge on $\overline{PLAYL}$ initiates a new Play cycle from the starting address.

4. **Level-activated playback (truncated).**

   If $\overline{PLAYL}$ is pulled HIGH any time during the Playback cycle, the device stops playing and enters the power-down mode. A subsequent falling edge on $\overline{PLAYL}$ initiates a new Play cycle from the start address.

5. **Record (interrupting playback).**

   The $\overline{REC}$ signal takes precedence over other operations. Any LOW-going transition on $\overline{REC}$ initiates a new Record operation from the beginning of the start address or at a selected location, regardless of any current operation in progress.

6. **Record a message, partially filling the address space.**

   A record operation need not fill the entire message space. Releasing the $\overline{REC}$ signal HIGH before filling the message space causes the recording to stop and an EOM to be placed. The device powers down automatically.

7. **Play back a message, partially filling the address space.**

   Pulling the $\overline{PLAYE}$ or $\overline{PLAYL}$ signal LOW initiates a Playback cycle which is then completed when the EOM marker is encountered. Playback ceases and the device powers down.

8. **$\overline{RECLED}$ operation.**

   The $\overline{RECLED}$ output pin provides an active-LOW signal which can be used to drive an LED as a "record-in-progress" indicator. It returns to a HIGH state when the $\overline{REC}$ pin is released HIGH or when the recording is completed due to the message space being filled. This pin also pulses LOW to indicate an EOM at the end of a message being played.

APPLICATIONS NOTE

Some users may experience an unexpected recording taking place when their circuit is powered up, or the batteries are changed and V_{CC} rises faster than $\overline{REC}$. This undesired recording prevents playback of the previously recorded message. A spurious End Of Message (EOM) marker appears at the very beginning of the memory, preventing access to the original message, and nothing is played.

To prevent this occurrence, place a capacitor (approx. 0.001 µF) between the control pin ($\overline{REC}$) and V_{CC}. This pulls the control pin voltage up with V_{CC} as it rises. Once the voltage is HIGH, the pull-up device will keep the pin HIGH until intentionally pulled LOW, preventing the false EOM marker.

Since this anomaly depends on factors such as the capacitance of the user's printed circuit board, not all circuit designs will exhibit the spurious marker. However, it is recommended that the capacitor is included for design reliability. A more detailed explanation and resolution of this occurrence is described in Chapter 5, Application Information.

ORDERING INFORMATION

Product Number Descriptor Key

ISD14 _ _ _ _

ISD1400 Series

Duration:
16 = 16 Seconds
20 = 20 Seconds

Special Temperature Field:
Blank = Commercial Packaged (0°C to +70°C)
or Commercial Die (0°C to +50°C)
I = Industrial (-40°C to +85°C)

Package Type:
P = 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP)
S = 28-Lead 0.300-Inch Plastic Small Outline Package (SOIC)
X = Die

2

When ordering ISD1400 Series devices, please refer to the following valid part numbers.

Part Number	Part Number
ISD1416P	ISD1420P
ISD1416PI	ISD1420PI
ISD1416S	ISD1420S
ISD1416SI	ISD1420SI
ISD1416X	ISD1420X

For the latest product information, access ISD's worldwide website at http://www.isd.com.

atures

- ›mpatible with MCS®-51 Products
- : Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
-)V to 5.5V Operating Range
- ılly Static Operation: 0 Hz to 33 MHz
- ıree-level Program Memory Lock
- ;6 x 8-bit Internal RAM
- : Programmable I/O Lines
- ıree 16-bit Timer/Counters
- ;ght Interrupt Sources
- ıll Duplex UART Serial Channel
- ow-power Idle and Power-down Modes
- ıterrupt Recovery from Power-down Mode
- /atchdog Timer
- ual Data Pointer
- ower-off Flag
- ast Programming Time
- lexible ISP Programming (Byte and Page Mode)
- ıreen (Pb/Halide-free) Packaging Option

Description

› AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K es of in-system programmable Flash memory. The device is manufactured using ıel's high-density nonvolatile memory technology and is compatible with the indus- standard 80C51 instruction set and pinout. The on-chip Flash allows the program mory to be reprogrammed in-system or by a conventional nonvolatile memory pro- ımmer. By combining a versatile 8-bit CPU with in-system programmable Flash on ıonolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a hly-flexible and cost-effective solution to many embedded control applications.

e AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a -vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, d clock circuitry. In addition, the AT89S52 is designed with static logic for operation wn to zero frequency and supports two software selectable power saving modes. e Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and errupt system to continue functioning. The Power-down mode saves the RAM con- ıts but freezes the oscillator, disabling all other chip functions until the next interrupt hardware reset.

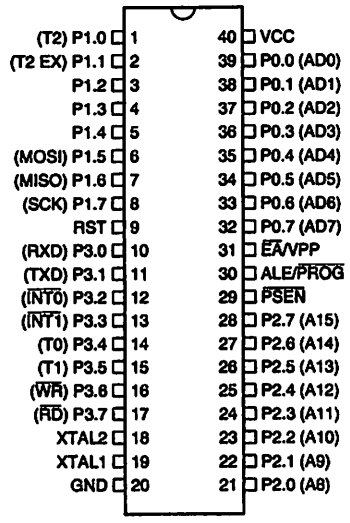
8-bit Microcontroller with 8K Bytes In-System Programmable Flash

AT89S52

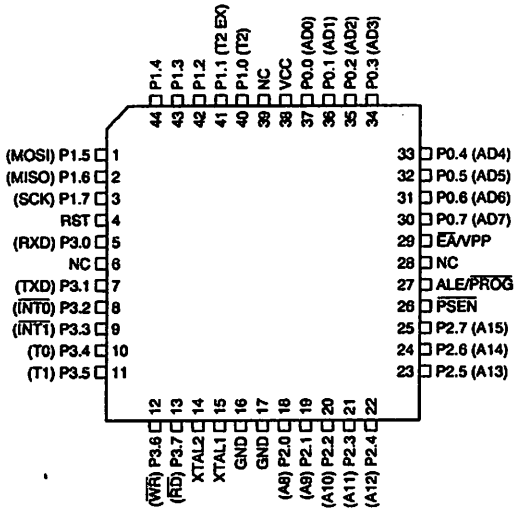
1919C–MICRO–3/05

Pin Configurations

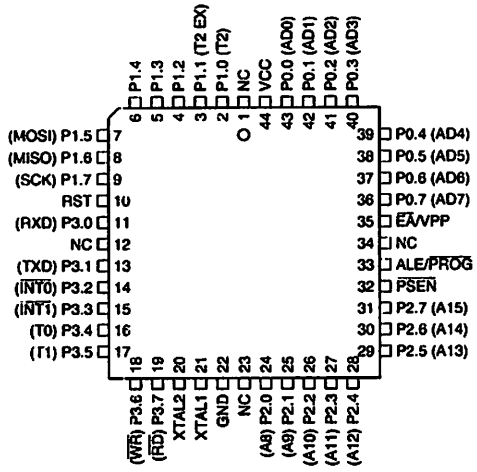
40-lead PDIP



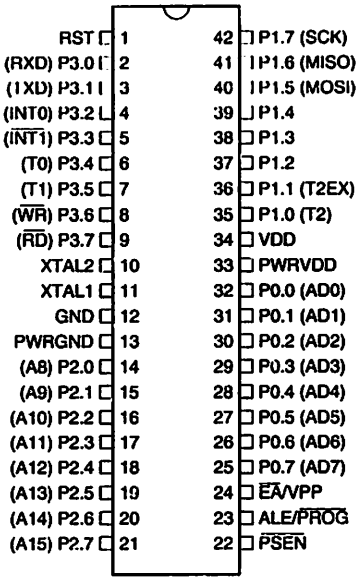
44-lead TQFP



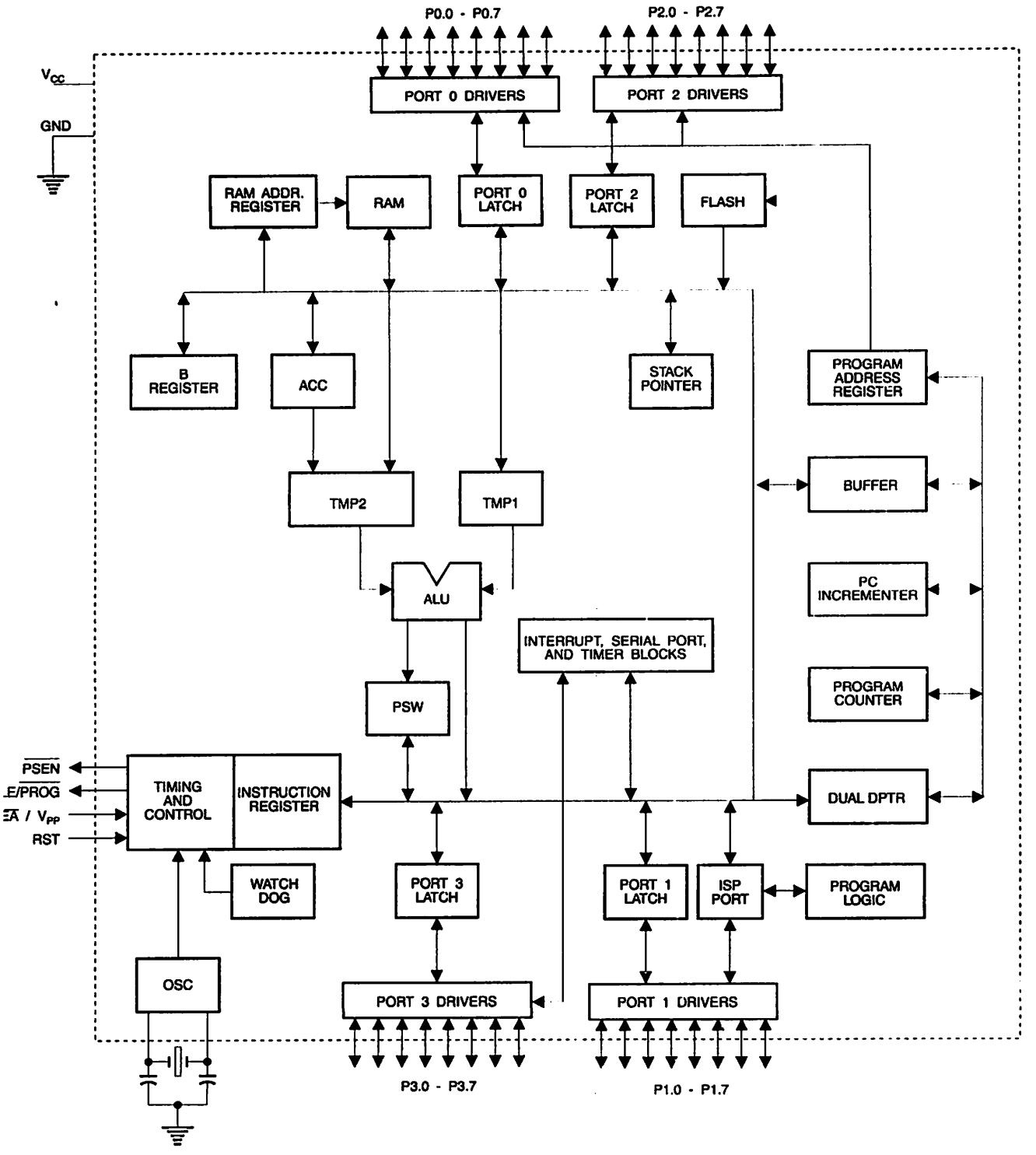
2.3 44-lead PLCC



2.4 42-lead PDIP



Block Diagram



Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives high for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{\text{PROG}}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S52 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

0 $\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

1 XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

2 XTAL2

Output from the inverting oscillator amplifier.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in 2) and T2MOD (shown in Table 10-2) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

e 5-1. AT89S52 SFR Map and Reset Values

F8H									0FFH
F0H	B 00000000								0F7H
E8H									0EFH
E0H	ACC 00000000								0E7H
D8H									0DFH
D0H	PSW 00000000								0D7H
C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
C0H									0C7H
B8H	IP XX000000								0BFH
B0H	P3 11111111								0B7H
A8H	IE 0X000000								0AFH
A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

le 5-2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H

Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
	7	6	5	4	3	2	1	0

mbol	Function
2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
XF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
CLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
CLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
XEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
R2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
P/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

e 5-3. AUXR: Auxiliary Register

XR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

Reserved for future expansion

ALE Disable/Enable ALE

DISALE	Operating Mode
0	ALE is emitted at a constant rate of 1/6 the oscillator frequency
1	ALE is active only during a MOVX or MOVC instruction

RTO Disable/Enable Reset out

DISRTO	
0	Reset pin is driven High after WDT times out
1	Reset pin is input only

IDLE Disable/Enable WDT in IDLE mode

WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

al Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data nter Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 ects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before essing the respective Data Pointer Register.

wer Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power It can be set and rest under software control and is not affected by reset.

le 5-4. AUXR1: Auxiliary Register 1

JXR1 Address = A2H Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

Reserved for future expansion

PS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S52, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are to external memory.

Data Memory

The AT89S52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When

WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S52 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S52 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S52 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, please click on the document link below:

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S52 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, please click on the document link below:

. Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in . Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Table 10-1. Timer 2 Operating Modes

RCLK +TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

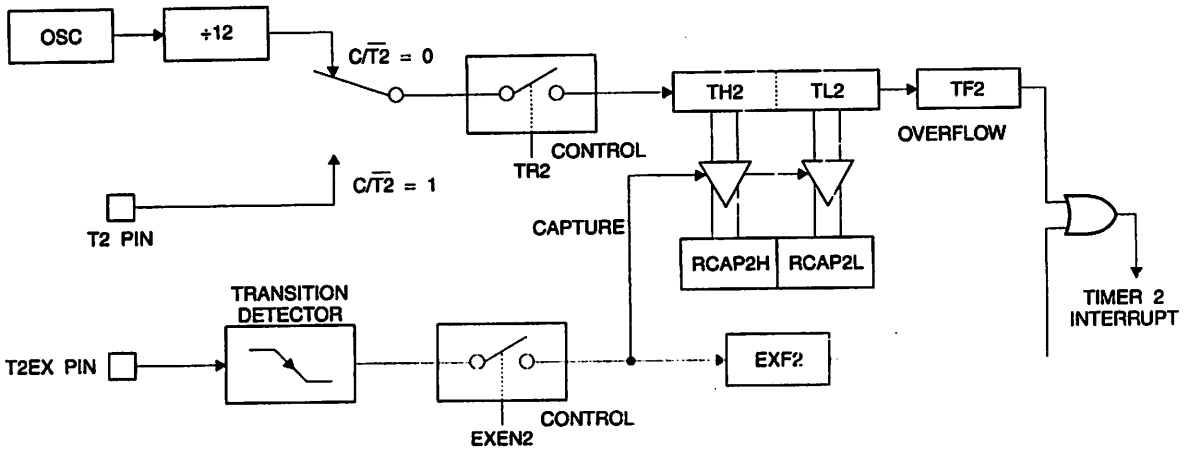
.1 Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in .

.2 Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

ıre 10-1. Timer in Capture Mode



le 10-2. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H Reset Value = XXXX XX00B

Not Bit Addressable

	–	–	–	–	–	–	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

mbol	Function
	Not implemented, reserved for future
OE	Timer 2 Output Enable bit
EN	When set, this bit allows Timer 2 to be configured as an up/down counter

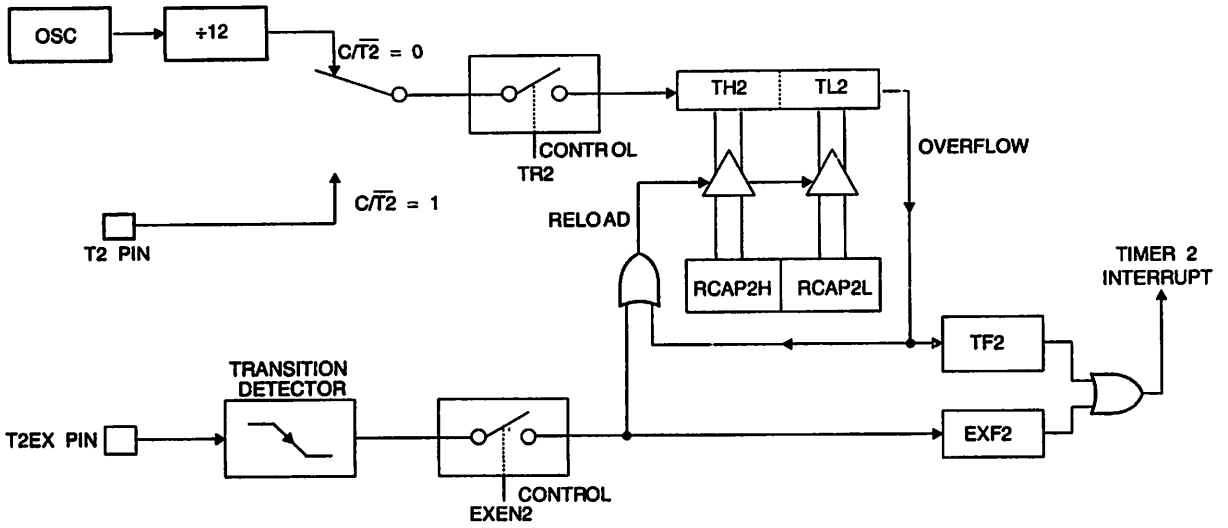
shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in Timer in Capture ModeRCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in . In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

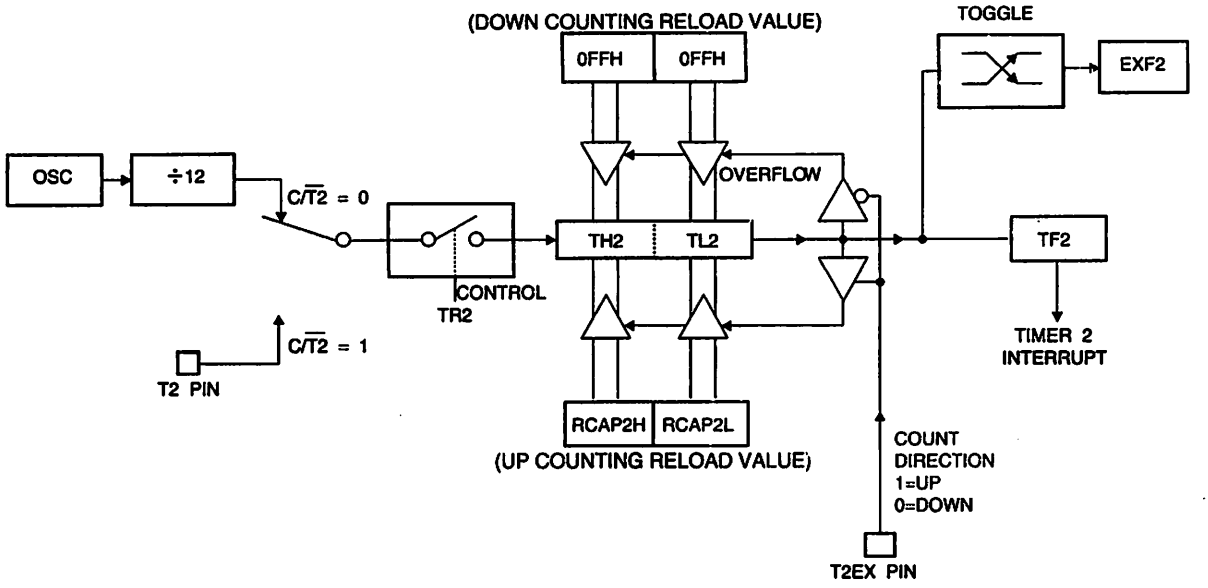
A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

ure 10-2. Timer 2 Auto Reload Mode (DCEN = 0)



ure 10-3. Timer 2 Auto Reload Mode (DCEN = 1)



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON ( ). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in .

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

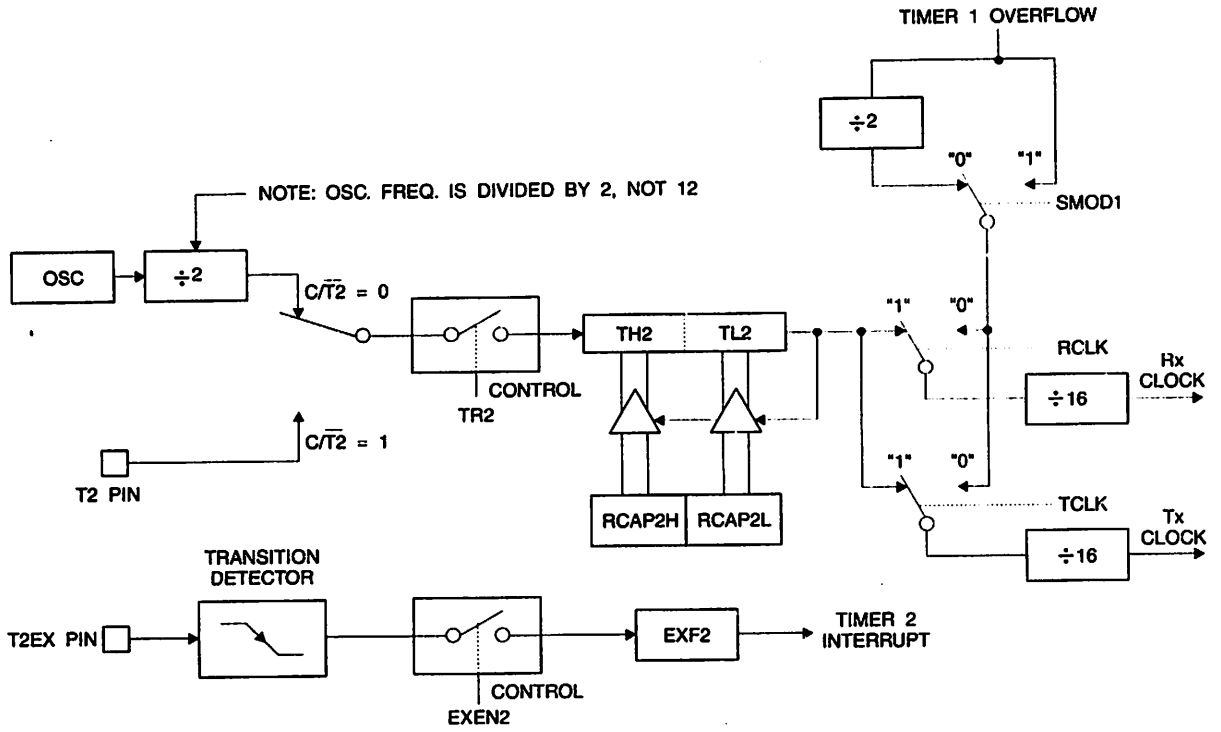
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536\text{-RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in . This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus, when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

ıre 11-1. Timer 2 in Baud Rate Generator Mode



;. Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in . This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

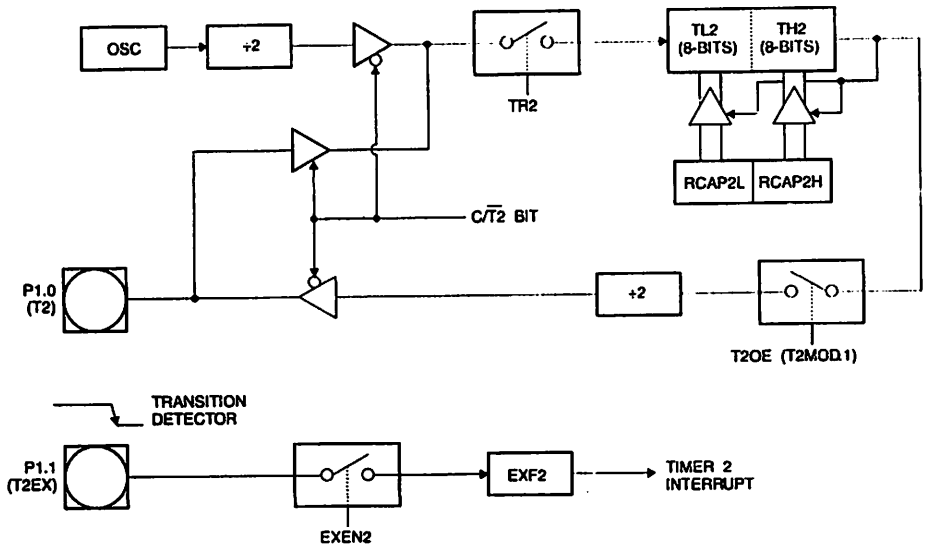
To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536-(\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

ıre 12-1. Timer 2 in Clock-Out Mode



. Interrupts

The AT89S52 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in .

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that shows that bit position IE.6 is unimplemented. User software should not write a 1 to this bit position, since it may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

le 13-1. Interrupt Enable (IE) Register

(MSB)							(LSB)
EA	–	ET2	ES	ET1	EX1	ET0	EX0

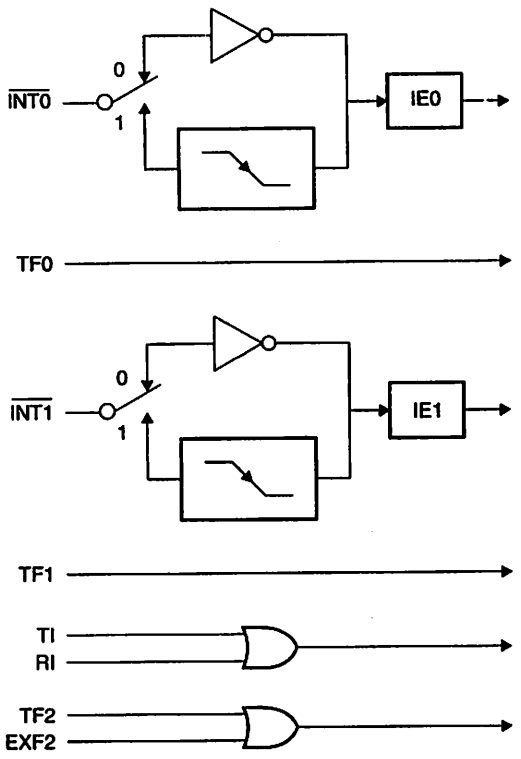
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

mbol	Position	Function
	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
	IE.6	Reserved.
2	IE.5	Timer 2 interrupt enable bit.
S	IE.4	Serial Port interrupt enable bit.
T1	IE.3	Timer 1 interrupt enable bit.
X1	IE.2	External interrupt 1 enable bit.
T0	IE.1	Timer 0 interrupt enable bit.
X0	IE.0	External interrupt 0 enable bit.

ser software should never write 1s to reserved bits, because they may be used in future AT89 products.

ure 13-1. Interrupt Sources



. Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in . Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in . There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

. Idle Mode

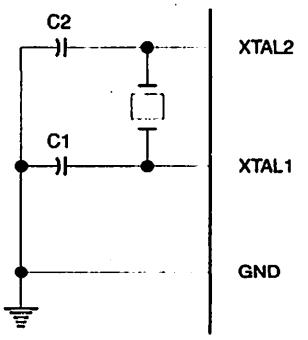
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

. Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 16-1. Oscillator Connections



Note: 1. C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 16-2. External Clock Drive Configuration

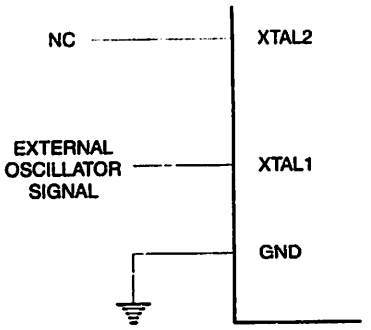


Table 16-1. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

7. Program Memory Lock Bits

The AT89S52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in .

Table 17-1. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

. Programming the Flash – Parallel Mode

The AT89S52 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S52 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S52, the address, data, and control signals should be set up according to the ( ) and and . To program the AT89S52, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S52 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. **The status of the individual lock bits can be verified directly by reading them back.**

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 52H indicates AT89S52
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

. Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

. Serial Programming Algorithm

To program and verify the AT89S52 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   a. Apply power between VCC and GND pins.
   b. Set RST pin to "H".

If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

1. Set XTAL1 to "L" (if a crystal is not used).
2. Set RST to "L".
3. Turn V_{CC} power off.

Data Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

. Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in

. Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

le 22-1. Flash Programming Modes

de	V_{CC}	RST	$\overline{PSEN}$	ALE/ $\overline{PROG}$	$\overline{EA}$/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.4-0 Address	P1.7-0 Address
ite Code Data	5V	H	L	⌣	12V	L	H	H	H	H	D_{IN}	A12-8	A7-0
ad Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A12-8	A7-0
ite Lock Bit 1	5V	H	L	⌣	12V	H	H	H	H	H	X	X	X
ite Lock Bit 2	5V	H	L	⌣	12V	H	H	H	L	L	X	X	X
ite Lock Bit 3	5V	H	L	⌣	12V	H	L	H	H	L	X	X	X
ad Lock Bits 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
ip Erase	5V	H	L	⌣	12V	H	L	H	L	L	X	X	X
ad Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	X 0000	00H
ad Device ID	5V	H	L	H	H	L	L	L	L	L	52H	X 0001	00H
ad Device ID	5V	H	L	H	H	L	L	L	L	L	06H	X 0010	00H

es:
1. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{BSY}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 22-1. Programming the Flash Memory (Parallel Mode)

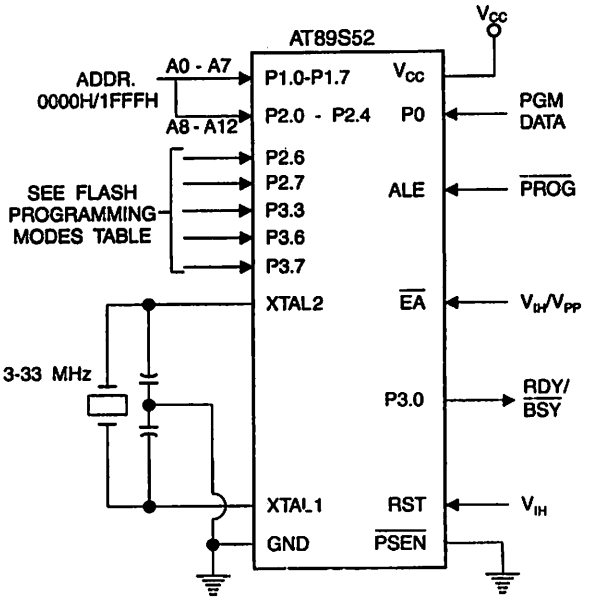
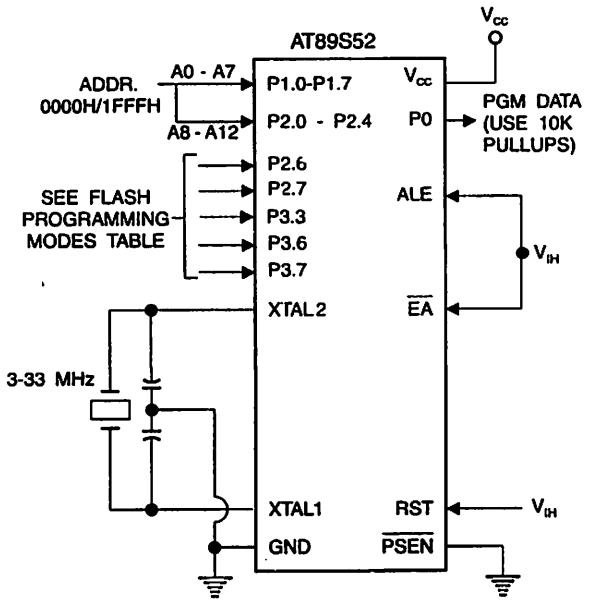


Figure 22-2. Verifying the Flash Memory (Parallel Mode)



. Flash Programming and Verification Characteristics (Parallel Mode)

= 20°C to 30°C, V_{CC} = 4.5 to 5.5V

mbol	Parameter	Min	Max	Units
P	Programming Supply Voltage	11.5	12.5	V
	Programming Supply Current		10	mA
:	V_{CC} Supply Current		30	mA
CLCL	Oscillator Frequency	3	33	MHz
GL	Address Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
AX	Address Hold After $\overline{PROG}$	48 t_{CLCL}		
GL	Data Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
DX	Data Hold After $\overline{PROG}$	48 t_{CLCL}		
SH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48 t_{CLCL}		
GL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
SL	V_{PP} Hold After $\overline{PROG}$	10		µs
GH	$\overline{PROG}$ Width	0.2	1	µs
QV	Address to Data Valid		48 t_{CLCL}	
QV	$\overline{ENABLE}$ Low to Data Valid		48 t_{CLCL}	
QZ	Data Float After $\overline{ENABLE}$	0	48 t_{CLCL}	
BL	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
C	Byte Write Cycle Time		50	µs

ure 23-1. Flash Programming and Verification Waveforms – Parallel Mode

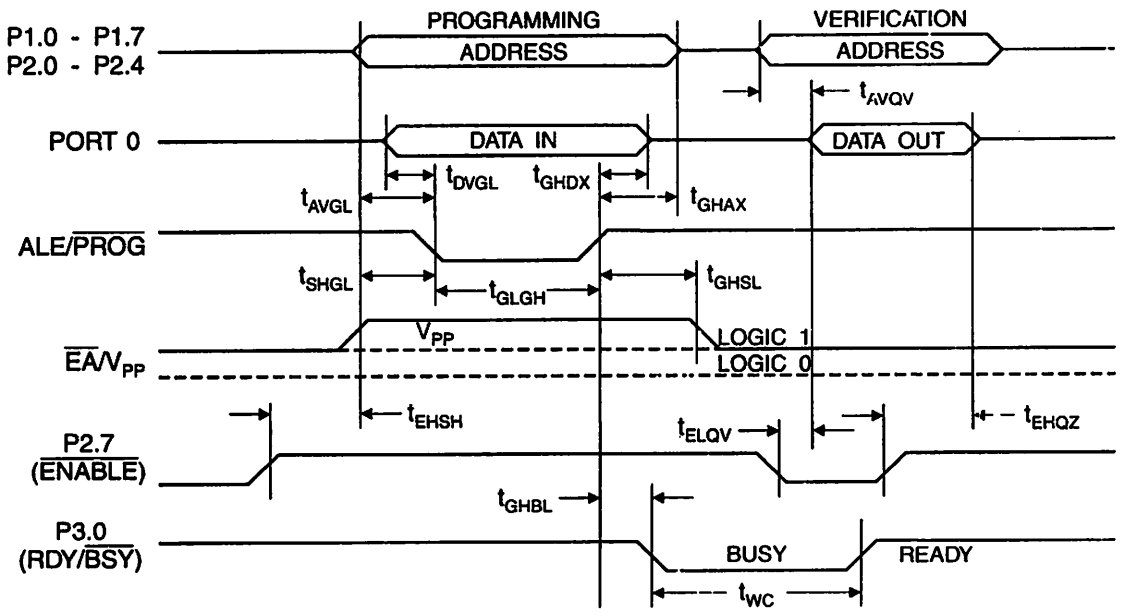
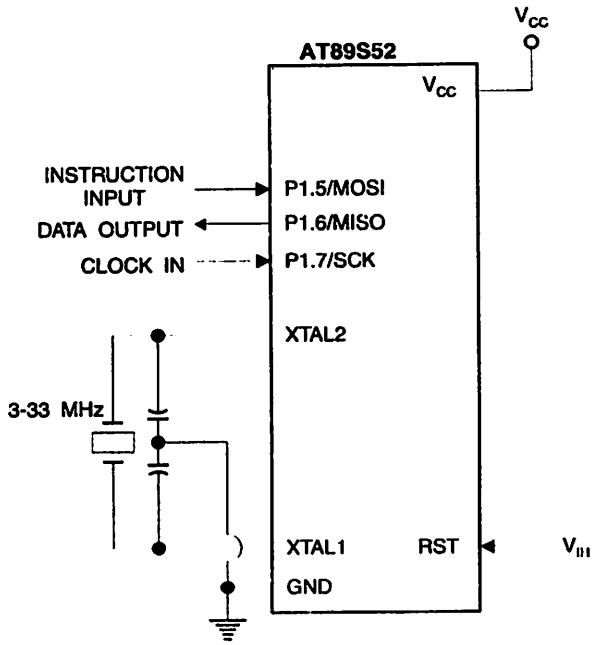
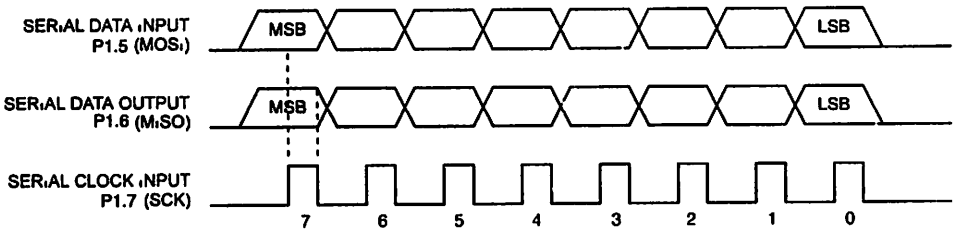


Figure 23-2. Flash Memory Serial Downloading



4. Flash Programming and Verification Waveforms – Serial Mode

Figure 24-1. Serial Programming Waveforms



le 24-1. Serial Programming Instruction Set

	Instruction Format				
struction	Byte 1	Byte 2	Byte 3	Byte 4	Operation
ogramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
ip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
ad Program Memory yte Mode)	0010 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
rite Program Memory yte Mode)	0100 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
rite Lock Bits	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
ad Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xxx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
ad Signature Bytes	0010 1000	xxx A12 A11 A10 A9 A8	A7 xxx xxx0	Signature Byte	Read Signature Byte
ad Program Memory age Mode)	0011 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
rite Program Memory age Mode)	0101 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

e: 1. B1 = 0, B2 = 0 ---> Mode 1, no lock protection
B1 = 0, B2 = 1 ---> Mode 2, lock bit 1 activated
B1 = 1, B2 = 0 ---> Mode 3, lock bit 2 activated
B1 = 1, B2 = 1 ---> Mode 4, lock bit 3 activated

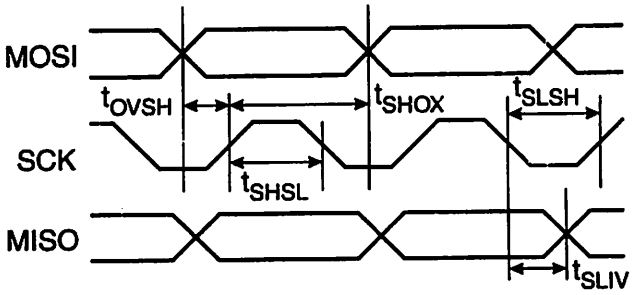
} Each of the lock bit modes needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

. Serial Programming Characteristics

ure 25-1. Serial Programming Timing



ble 25-1. Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

ymbol	Parameter	Min	Typ	Max	Units
t_{CLCL}	Oscillator Frequency	3		33	MHz
LCL	Oscillator Period	30			ns
HSL	SCK Pulse Width High	8 t_{CLCL}			ns
LSH	SCK Pulse Width Low	8 t_{CLCL}			ns
VSH	MOSI Setup to SCK High	t_{CLCL}			ns
HOX	MOSI Hold after SCK High	2 t_{CLCL}			ns
LIV	SCK Low to MISO Valid	10	16	32	ns
RASE	Chip Erase Instruction Cycle Time			500	ms
WC	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

. Absolute Maximum Ratings*

perating Temperature	-55°C to +125°C
orage Temperature	-65°C to +150°C
ltage on Any Pin th Respect to Ground	-1.0V to +7.0V
aximum Operating Voltage	6.6V
C Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

'. DC Characteristics

e values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

ymbol	Parameter	Condition	Min	Max	Units
L	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
L1	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
H	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
H1	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
OL	Output Low Voltage (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
OL1	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
OH	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
OH1	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-300	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RST	Reset Pulldown Resistor		50	300	KΩ
O	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode	V_{CC} = 5.5V		50	µA

es: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

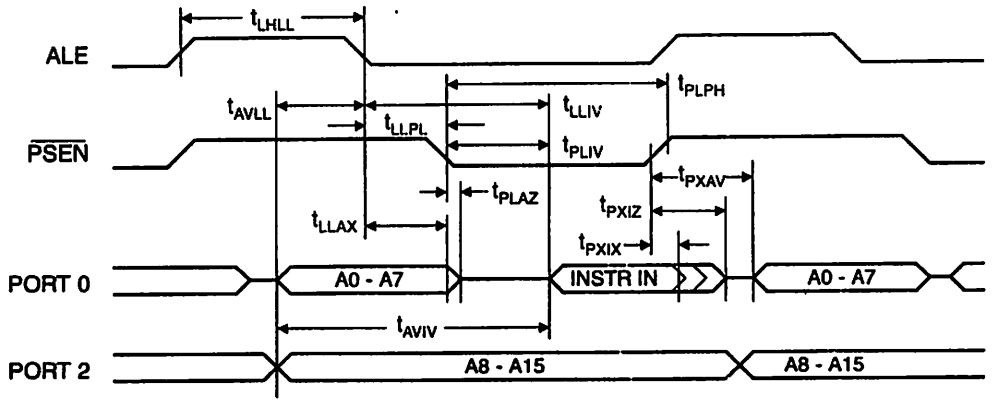
. AC Characteristics

ler operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other ɔuts = 80 pF.

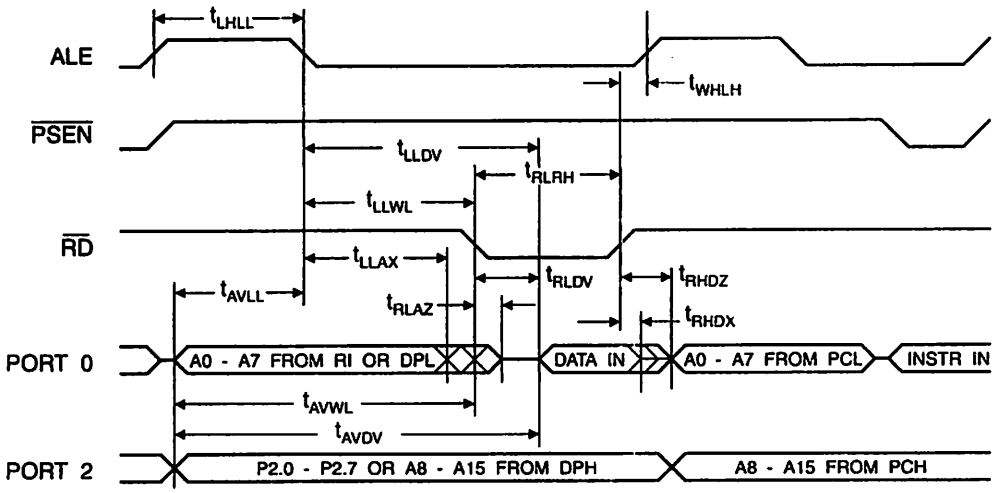
1 External Program and Data Memory Characteristics

		12 MHz Oscillator		Variable Oscillator		
'mbol	Parameter	Min	Max	Min	Max	Units
CLCL	Oscillator Frequency			0	33	MHz
ILL	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
'LL	Address Valid to ALE Low	43		t_{CLCL}-25		ns
AX	Address Hold After ALE Low	48		t_{CLCL}-25		ns
IV	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
PL	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
PH	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
JV	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
KIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
KIZ	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
KAV	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
VIV	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
LAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
LRH	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
LWH	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
LDV	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
HDX	Data Hold After $\overline{RD}$	0		0		ns
HDZ	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
LDV	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
VDV	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
LWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
VWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
VWX	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
VWH	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
'HQX	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
LAZ	$\overline{RD}$ Low to Address Float		0		0	ns
'HLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

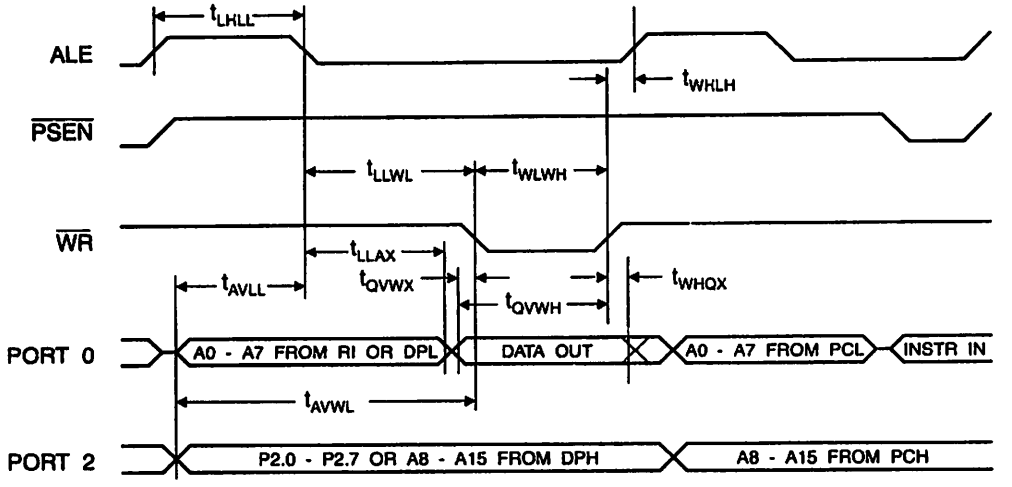
. External Program Memory Read Cycle



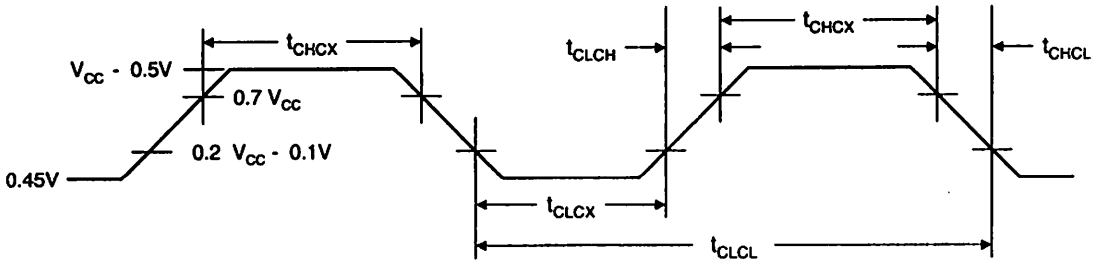
. External Data Memory Read Cycle



. External Data Memory Write Cycle



. External Clock Drive Waveforms



. External Clock Drive

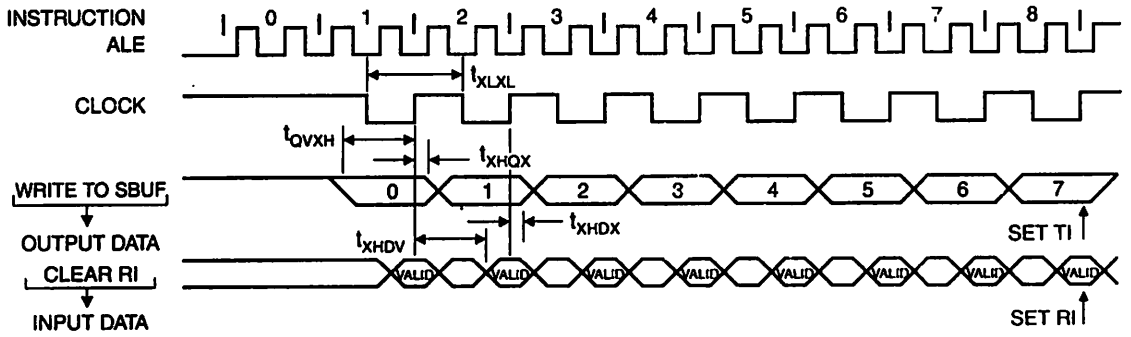
ymbol	Parameter	Min	Max	Units
t_{CLCL}	Oscillator Frequency	0	33	MHz
LCL	Clock Period	30		ns
HCX	High Time	12		ns
LCX	Low Time	12		ns
LCH	Rise Time		5	ns
HCL	Fall Time		5	ns

. Serial Port Timing: Shift Register Mode Test Conditions

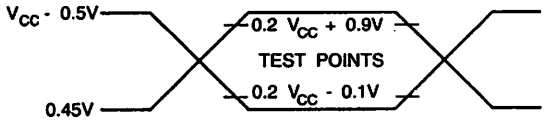
values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

mbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
XL	Serial Port Clock Cycle Time	1.0		12 t_{CLCL}		µs
/XH	Output Data Setup to Clock Rising Edge	700		10 t_{CLCL}-133		ns
QX	Output Data Hold After Clock Rising Edge	50		2 t_{CLCL}-80		ns
DX	Input Data Hold After Clock Rising Edge	0		0		ns
DV	Clock Rising Edge to Input Data Valid		700		10 t_{CLCL}-133	ns

. Shift Register Mode Timing Waveforms



. AC Testing Input/Output Waveforms



e: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

. Float Waveforms

e: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

1. Ordering Information

1.1 Standard Package

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S52-24AC AT89S52-24JC AT89S52-24PC AT89S52-24SC	44A 44J 40P6 42PS6	Commercial (0°C to 70°C)
		AT89S52-24AI AT89S52-24JI AT89S52-24PI AT89S52-24SI	44A 44J 40P6 42PS6	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S52-33AC AT89S52-33JC AT89S52-33PC AT89S52-33SC	44A 44J 40P6 42PS6	Commercial (0°C to 70°C)

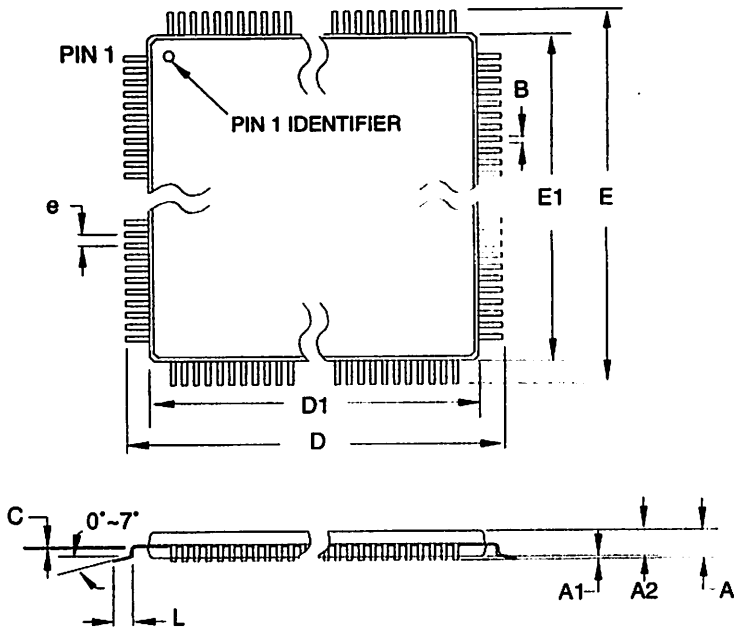
1.2 Green Package Option (Pb/Halide-free)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S52-24AU AT89S52-24JU AT89S52-24PU	44A 44J 40P6	Industrial (-40°C to 85°C)

Package Type	
4A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
4J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
0P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
2PS6	42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Packaging Information

1 44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

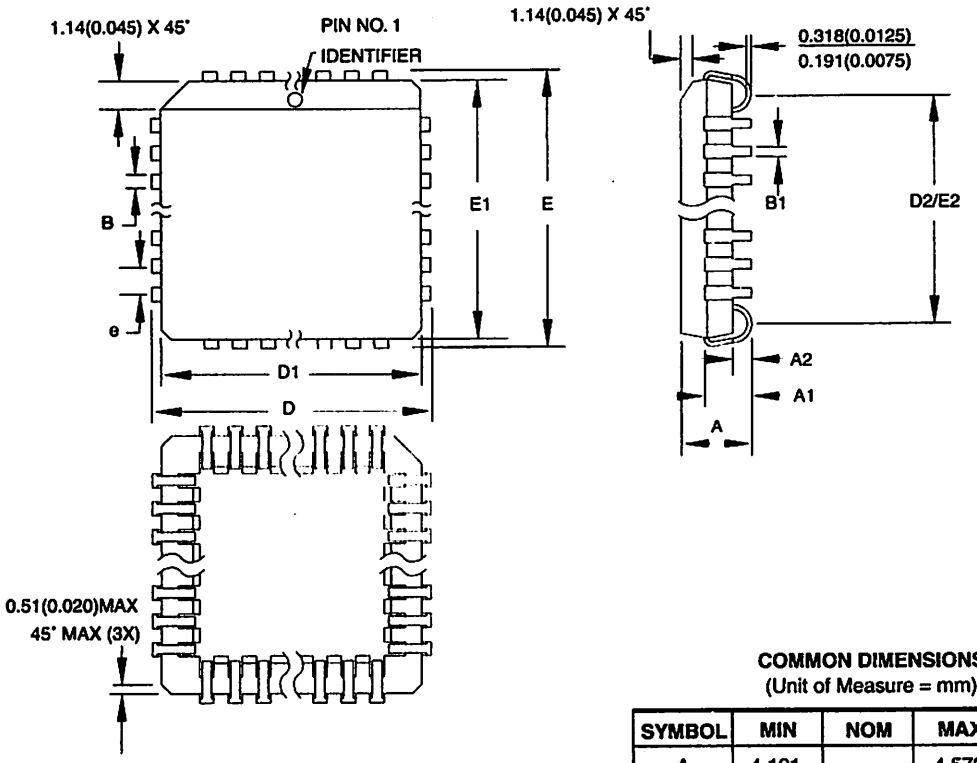
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A**, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

.2 44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

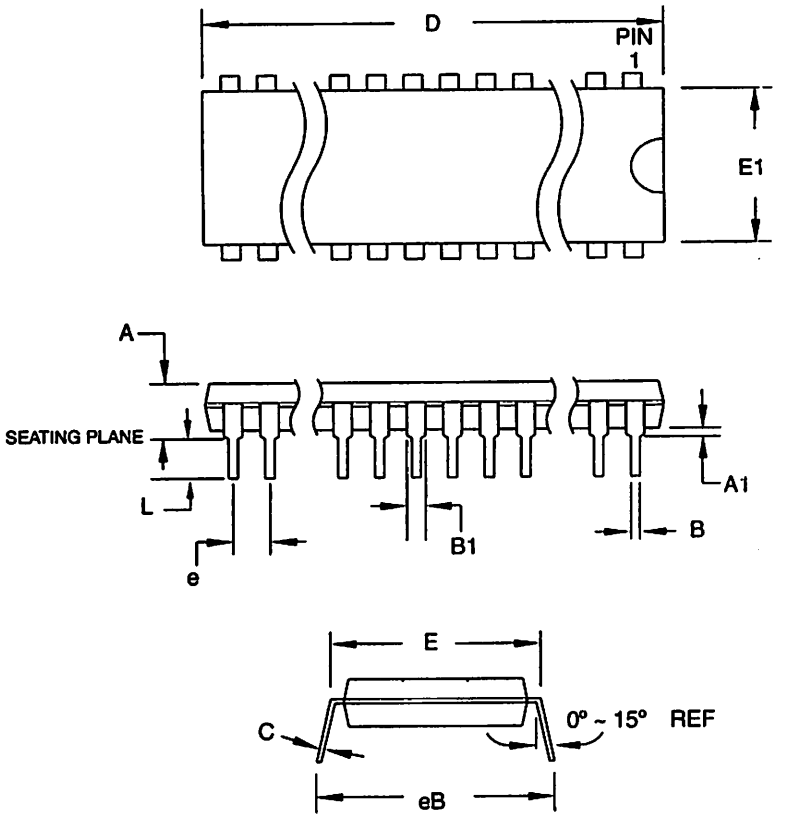
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

3 40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

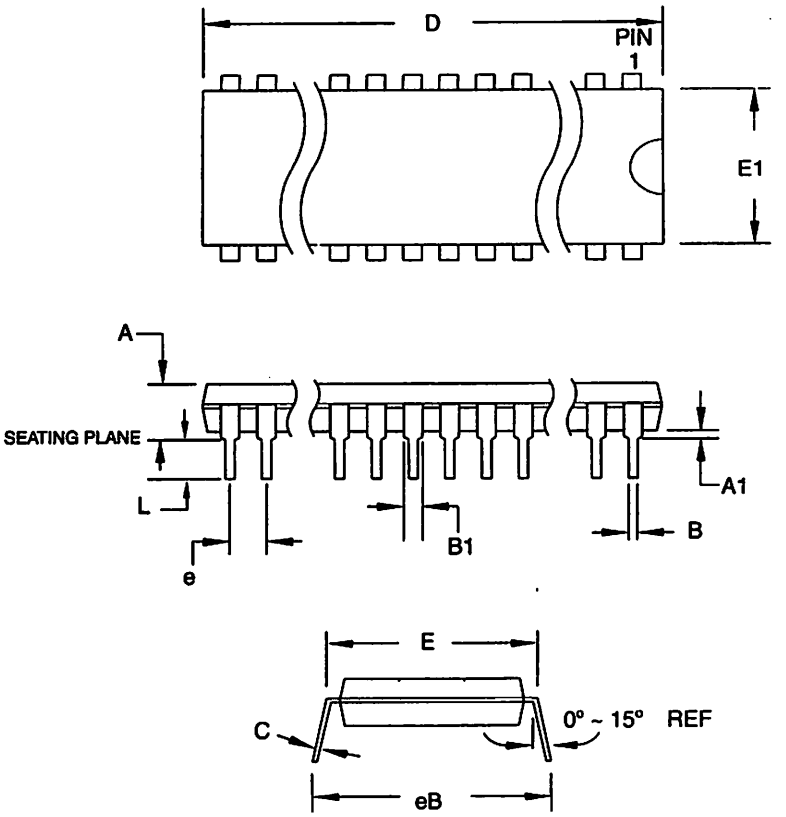
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

4 42PS6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.83	
A1	0.51	–	–	
D	36.70	–	36.96	Note 2
E	15.24	–	15.88	
E1	13.46	–	13.97	Note 2
B	0.38	–	0.56	
B1	0.76	–	1.27	
L	3.05	–	3.43	
C	0.20	–	0.30	
eB	–	–	18.55	
e	1.78 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/6/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**42PS6**, 42-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	42PS6	A

tmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

legional Headquarters

:urope
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

lsia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

apan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
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Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

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Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

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1919C–MICRO–3/05 xM

DALLAS SEMICONDUCTOR

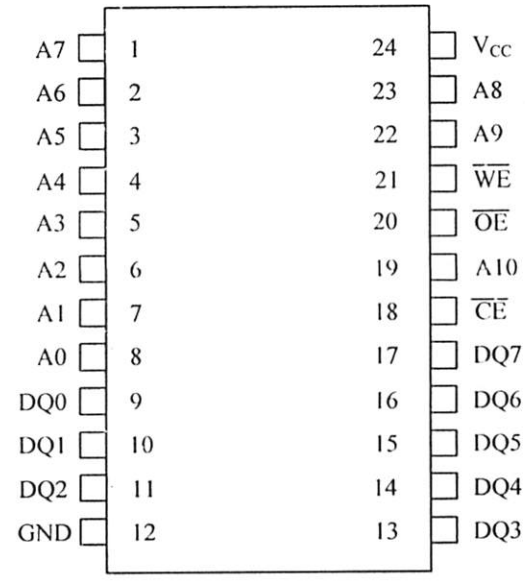
www.dalsemi.com

DS1642
Nonvolatile Timekeeping RAM

FEATURES

- Integrated NV SRAM, real time clock, crystal, power fail control circuit and lithium energy source
- Standard JEDEC bytewide 2K x 8 static RAM pinout
- Clock registers are accessed identically to the static RAM. These registers are resident in the eight top RAM locations
- Totally nonvolatile with over 10 years of operation in the absence of power
- Access times of 70 ns and 100 ns
- Quartz accuracy ±1 minute a month @ 25°C, factory calibrated
- BCD coded year, month, date, day, hours, minutes, and seconds with leap year compensation valid up to 2100
- Power-fail write protection allows for ±10% V_{CC} power supply tolerance
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time

PIN ASSIGNMENT



PIN DESCRIPTION

A0-A10	- Address Input
$\overline{CE}$	- Chip Enable
$\overline{OE}$	- Output Enable
$\overline{WE}$	- Write Enable
V_{CC}	- +5 Volts
GND	- Ground
DQ0-DQ7	- Data Input/Output

ORDERING INFORMATION

DS1642-70	70 ns access
DS1642-100	100 ns access

DESCRIPTION

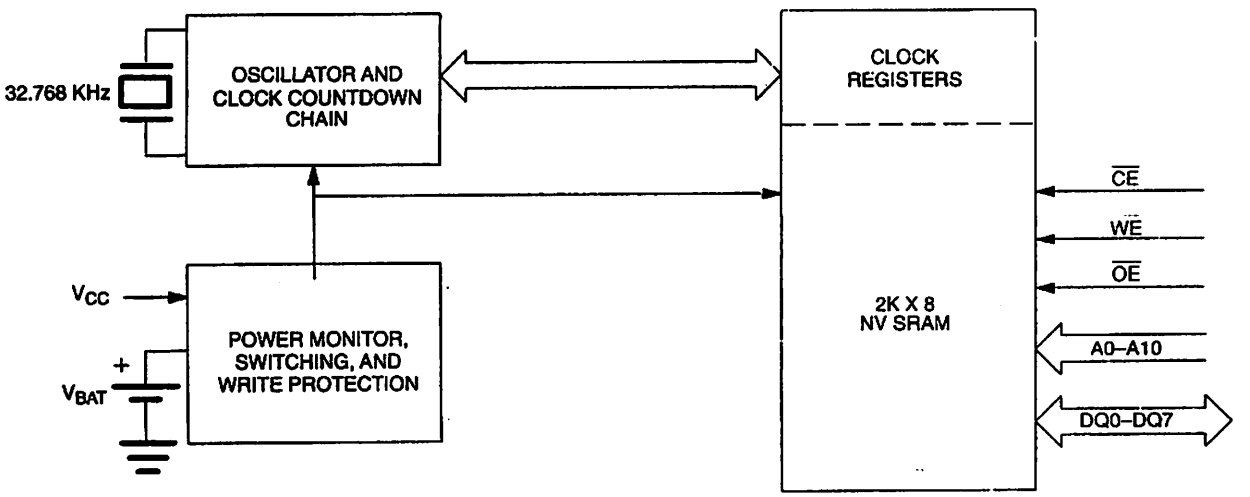
The DS1642 is a 2K x 8 nonvolatile static RAM and a full-function real time clock which are both accessible in a bytewide format. The nonvolatile time keeping RAM is pin- and function-equivalent to any JEDEC standard 2K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets, providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double-buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also

revents time loss as the timekeeping countdown continues unabated by access to time register data. The)S1642 also contains its own power-fail circuitry which deselects the device when the V_{CC} supply is in n out-of-tolerance condition. This feature prevents loss of data from unpredictable system operation ·ought on by low V_{CC} as errant access and update cycles are avoided.

:LOCK OPERATIONS-READING THE CLOCK

/hile the double-buffered register structure reduces the chance of reading incorrect data, internal updates) the DS1642 clock registers should be halted before clock data is read to prevent reading of data in ·ansition. However, halting the internal clock register updating process does not affect clock accuracy. Jpdating is halted when a 1 is written into the read bit, the 7th most significant bit in the control register. ıs long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the :ount, that is day, date, and time that was current at the moment the halt command was issued. However, he internal clock registers of the double-buffered system continue to update so that the clock accuracy is ıot affected by the access of data. All of the DS1642 registers are updated simultaneously after the clock ;tatus is reset. Updating is within a second after the read bit is written to 0.

DS1642 BLOCK DIAGRAM Figure 1



DS1642 TRUTH TABLE Table 1

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5 VOLTS ± 10%	V_{IH}	X	X	DESELECT	HIGH Z	STANDBY
	V_{IL}	X	V_{IL}	WRITE	DATA IN	ACTIVE
	V_{IL}	V_{IL}	V_{IH}	READ	DATA OUT	ACTIVE
	V_{IL}	V_{IH}	V_{IH}	READ	HIGH Z	ACTIVE
<4.5 VOLTS >V_{BAT}	X	X	X	DESELECT	HIGH Z	CMOS STANDBY
<V_{BAT}	X	X	X	DESELECT	HIGH Z	DATA RETENTION MODE

;ETTING THE CLOCK

'he 8th bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts pdates to the DS1642 registers. The user can then load them with the correct day, date and time data in 4-hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters ıd allows normal operation to resume.

·TOPPING AND STARTING THE CLOCK OSCILLATOR

he clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off › minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to 1 stops the oscillator.

⁻REQUENCY TEST BIT

3it 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the ›scillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is ›eing read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid i.e., $\overline{CE}$ low, and $\overline{OE}$ low) and address for seconds register remain valid and stable.

:LOCK ACCURACY

Γhe DS1642 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The clock is :alibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. Γhe DS1642 does not require additional calibration and temperature deviations will have a negligible :ffect in most applications. For this reason, methods of field clock calibration are not available and not ıecessary.

)S1642 REGISTER MAP – BANK1 Table 2

ADDRESS	DATA								FUNCTION	
	B7	B6	B5	B4	B3	B2	B1	B0		
7FF	-	-	-	-	-	-	-	-	YEAR	00-99
7FE	X	X	X	-	-	-	-	-	MONTH	01-12
7FD	X	X	-	-	-	-	-	-	DATE	01-31
7FC	X	FT	X	X	X	-	-	-	DAY	00-23
7FB	X	X	-	-	-	-	-	-	HOUR	00-59
7FA	X	-	-	-	-	-	-	-	MINUTES	00-59
7F9	$\overline{OSC}$	-	-	-	-	-	-	-	SECONDS	00-59
7F8	W	R	X	X	X	X	X	X	CONTROL	A

$\overline{OSC}$ = STOP BIT
W = WRITE BIT
R = READ BIT
X = UNUSED
FT = FREQUENCY TEST

NOTE:

All indicated "X" bits are not dedicated to any particular function and can be used as normal RAM bits.

RETRIEVING DATA FROM RAM OR CLOCK

The DS1642 is in the read mode whenever $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple–through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1642 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

When V_{CC} is within nominal limits (V_{CC} > 4.5 volts) the DS1642 can be accessed as described above by read or write cycles. However, when V_{CC} is below the power-fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM is blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. When V_{CC} falls below the level of the internal battery supply, power input is switched from the V_{CC} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CC} is returned to nominal level.

BATTERY LONGEVITY

The DS1642 has a lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1642 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V_{CC} power. Each DS1642 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{PF}, the lithium energy source is enabled for battery backup operation. Actual life expectancy of the DS1642 will be much longer than 10 years since no lithium battery energy is consumed when V_{CC} is present.

BSOLUTE MAXIMUM RATINGS*

oltage on Any Pin Relative to Ground	–0.3V to +7.0V
perating Temperature	0°C to 70°C
orage Temperature	–20°C to +70°C
oldering Temperature	260°C for 10 seconds (See Note 6)

This is a stress rating only and functional operation of the device at these or any other conditions above ose indicated in the operation sections of this specification is not implied. Exposure to absolute aximum rating conditions for extended periods of time may affect reliability.

ECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
ogic 1 Voltage All Inputs	V_{IH}	2.2		V_{CC}+0.3	V	1
ogic 0 Voltage All Inputs	V_{IL}	-0.3		0.8	V	1

C ELECTRICAL CHARACTERISTICS

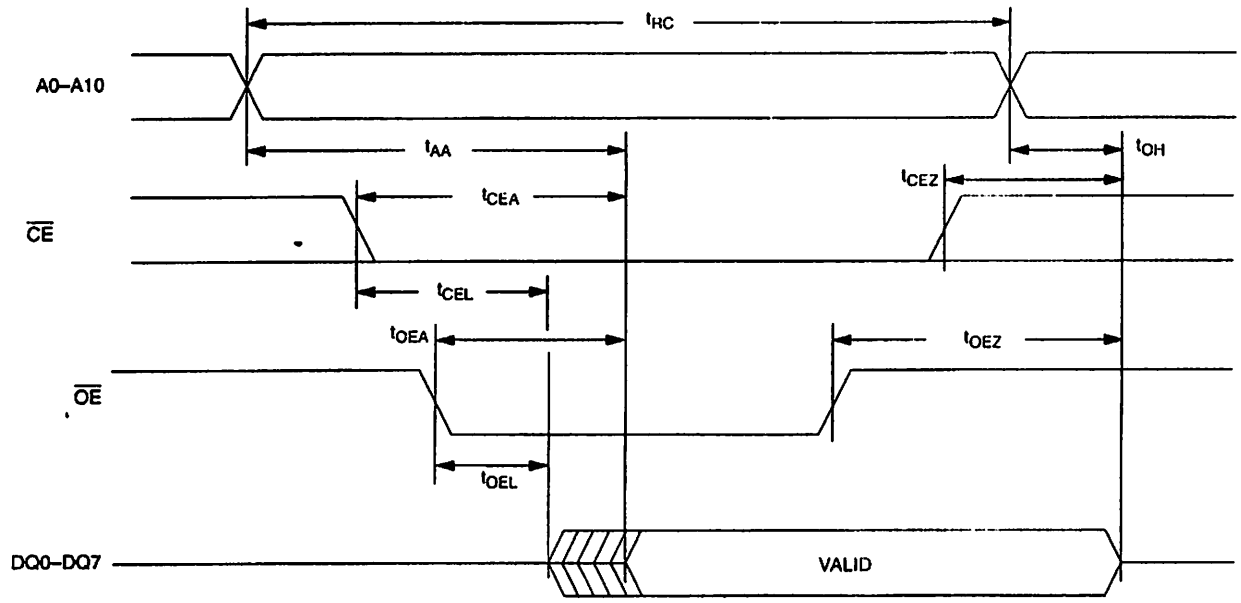
($0°C \leq t_A \leq 70°C$; V_{CC} (MAX) $\leq V_{CC} \leq V_{CC}$ (MIN))

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}		15	50	mA	2, 3
TTL Standby Current ($\overline{CE} = V_{IH}$)	I_{CC1}		1	3	mA	2, 3
CMOS Standby Current ($\overline{CE} \leq V_{CC}$-0.2V)	I_{CC2}		1	3	mA	2, 3
Input Leakage Current (any input)	I_{IL}	-1		+1	µA	
I/O Leakage Current (any output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0 mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} = +2.1 mA)	V_{OL}			0.4		1
Write Protection Voltage	V_{PF}	4.25	4.37	4.50	V	1

EAD CYCLE, AC CHARACTERISTICS (0°C to 70°C; VCC = 5.0V ± 10%)

PARAMETER	SYMBOL	70 ns access		100 ns access		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		ns	
Address Access Time	t_{AA}		70		100	ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5		5		ns	
$\overline{CE}$ Access Time	t_{CEA}		70		100	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}		25		35	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{OE}$ Access Time	t_{OEA}		35		55	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}		25		35	ns	
Output Hold from Address	t_{OH}	5		5		ns	

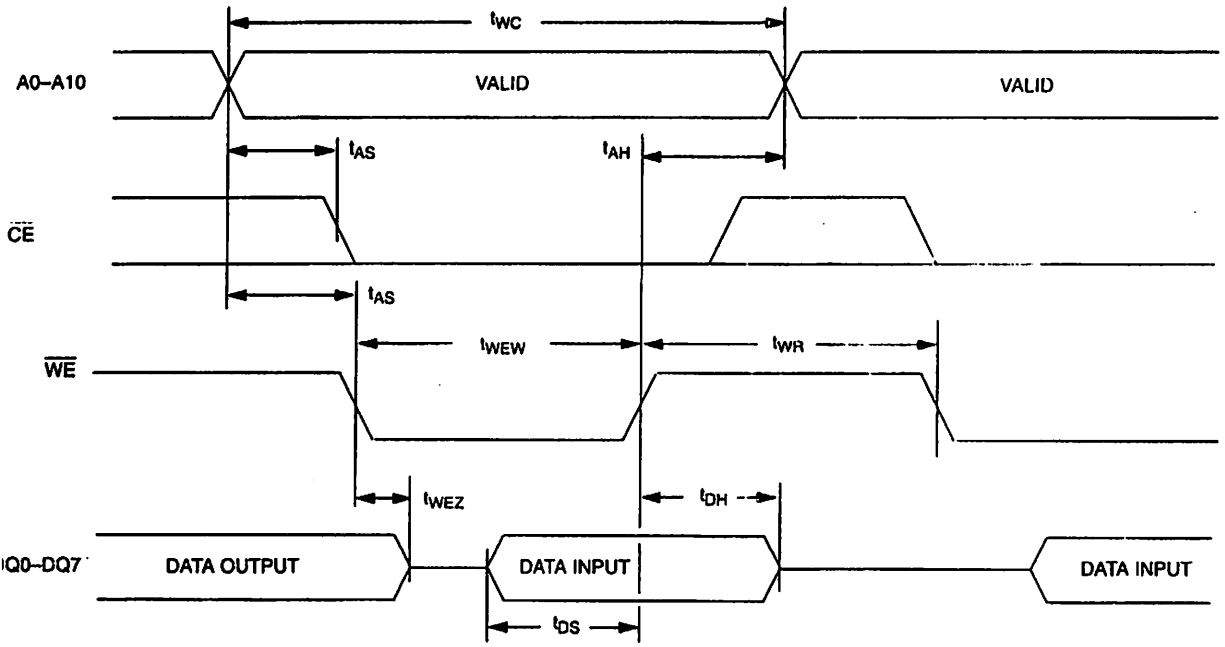
EAD CYCLE TIMING DIAGRAM



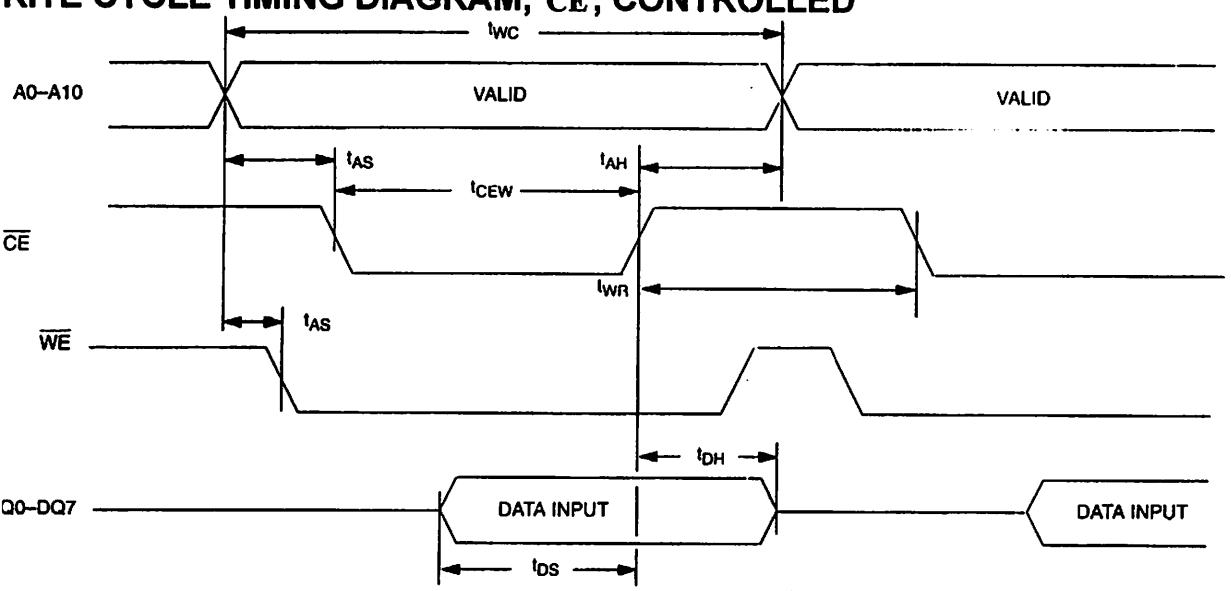
VRITE CYCLE, AC CHARACTERISTICS (0°C to 70°C; VCC = 5.0V ± 10%)

PARAMETER	SYMBOL	70 ns access		100 ns access		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Write Cycle Time	t_{WC}	70		100		ns	
Address Setup Time	t_{AS}	0		0		ns	
$\overline{WE}$ Pulse Width	t_{WEW}	50		70		ns	
$\overline{CE}$ Pulse Width	t_{CEW}	60		75		ns	
Data Setup Time	t_{DS}	30		40		ns	
Data Hold Time	t_{DH}	0		0		ns	
Address Hold Time	t_{AH}	5		5		ns	
$\overline{WE}$ Data Off Time	t_{WEZ}		25		35	ns	
Write Recovery Time	t_{WR}	5		5		ns	

'RITE CYCLE TIMING DIAGRAM, WRITE-ENABLE CONTROLLED



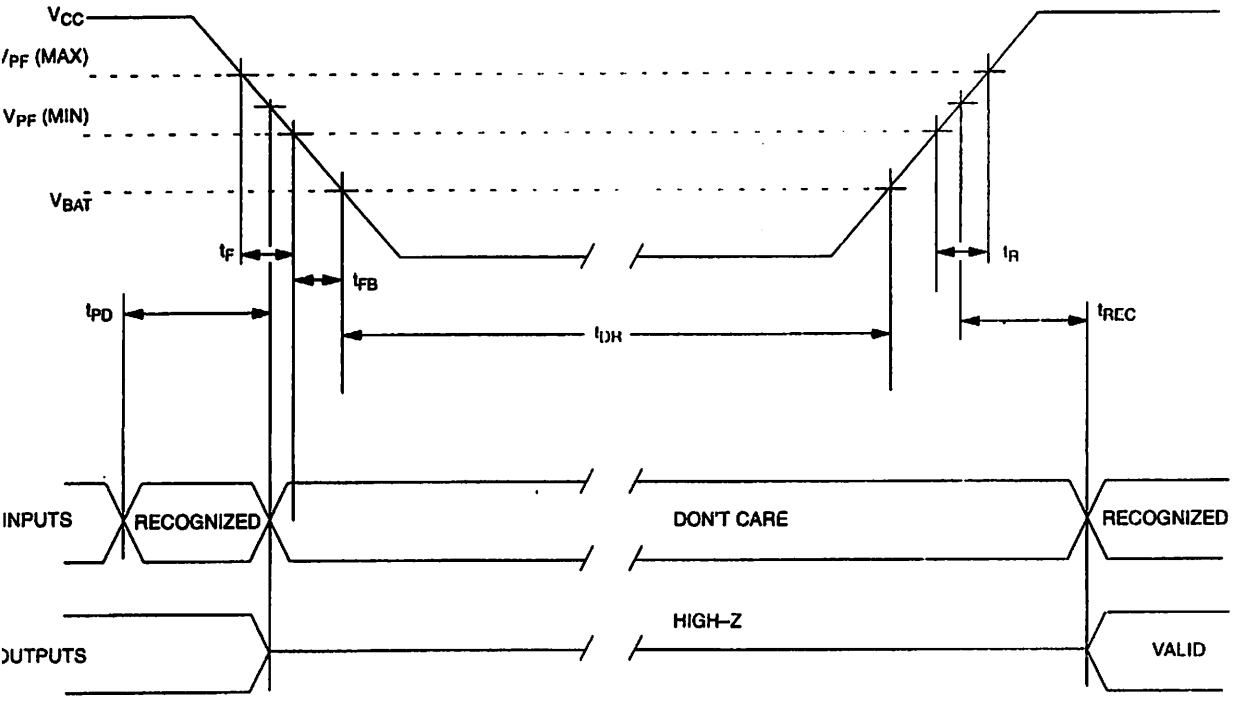
RITE CYCLE TIMING DIAGRAM, $\overline{CE}$, CONTROLLED



OWER-UP/DOWN AC CHARACTERISTICS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH} Before Power-down	t_{PD}	0			µs	
V_{CC} Fall Time: V_{PF} (MAX) to V_{PF} (Min)	t_F	300			µs	
V_{CC} Fall Time: V_{PF} (MIN) to V_{BAT}	t_{FB}	10			µs	
V_{CC} Rise Time: V_{PF} (MIN) to V_{PF} (MAX)	t_R	0			µs	
Power-up Recover Time	t_{REC}			35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	4, 5

OWER-UP/DOWN WAVEFORM TIMING



APACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on all pins (except DQ)	C_{IN}			7	pF	
Capacitance on DQ pins	C_O			10	pF	

: TEST CONDITIONS

tput Load: 100 pF + 1TTL Gate
ut Pulse Levels: 0.0 to 3.0 Volts
ning Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
ut Pulse Rise and Fall Times: 5 ns

TES:

Voltages are referenced to ground.

Typical values are at 25°C and nominal supplies.

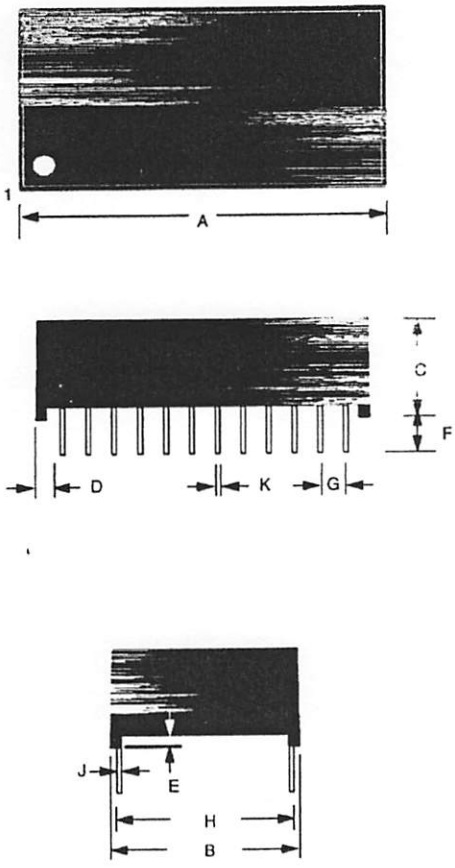
Outputs are open.

Data retention time is at 25°C.

Each DS1642 has a built–in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as a cumulative time in the absence of V_{CC} starting from the time power is first applied by the user.

Real Time Clock Modules can be successfully processed through conventional wave–soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used to prevent damage to the crystal.

DS1642 24-PIN PACKAGE



PKG	24-PIN	
DIM.	MIN	MAX
A IN.	1.270	0.290
MM	37.34	37.85
B IN.	0.675	0.700
MM	17.15	17.78
C IN.	0.315	0.335
MM	8.00	78.51
D IN.	0.075	0.105
MM	1.91	2.67
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.140	0.180
MM	3.56	4.57
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.010	0.018
MM	0.25	0.45
K IN.	0.015	0.025
MM	0.43	0.58

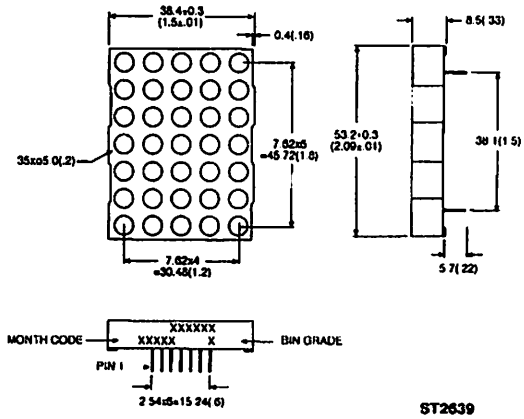
FAIRCHILD
SEMICONDUCTOR™

2.0" 5 × 7 DOT MATRIX DISPLAYS

YELLOW GMA 2875C GMC 2875C
HER GMA 2975C GMC 2975C
GREEN GMA 2475C GMC 2475C
BICOLOR RED/GREEN GMA 2675C

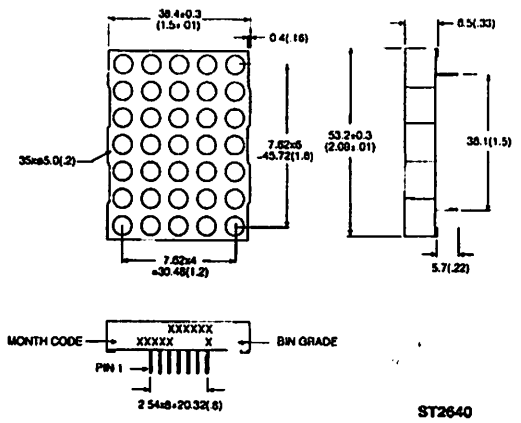
PACKAGE DIMENSIONS

A. GMX2X75C



ST2639

B. GMA2675C



ST2640

NOTES:
1. ALL PINS ARE 0.5 (.02).
2. DIMENSIONS IN MILLIMETERS (INCH), TOLERANCE IS ±0.25 (.01) UNLESS OTHERWISE NOTED.

DESCRIPTION

These are 5×7 dot matrix displays with large emitting area (0.2" diameter) LED sources. The GMX2X75C series are single color displays with the exception of GMA2675C which is a bicolor of red/green dispiays.

All displays have gray face and white dot color. Other face or dot colors are available with minimum requirement.

The X in GMX denotes row anode or row cathode.

FEATURES

- 2.0" (50.7 mm) character height
- Low power requirement
- High contrast & brightness
- Wide viewing angle 130°
- 5 × 7 array with X-Y select
- Compatible with USASCII and EBCDIC codes
- X-Y stackable
- Choice of two matrix orientation anode or cathode column
- Easy mounting on PCB
- Categorized for luminous intensity
- Single color displays have the choice of 3 bright colors — yellow/orange/green
- Multicolor color displays are applicable to 3 bright colors — greens, orange (HER) and yellow (green and HER mixed)

FAIRCHILD
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2.0" 5 × 7 DOT MATRIX DISPLAYS

ABSOLUTE MAXIMUM RATING (T_A = 25°C unless otherwise specified)

PARAMETER	YELLOW	HER	GREEN	UNITS
Power dissipation per dot/color	60	70	75	mW
Peak forward current per dot/color (duty cycle 1/10, 10KHz)	80	100	100	mA
Continuous I_F per dot/color	20	25	25	mA
Reverse voltage V_R per dot/color	5	5	5	V
Operating and storage temperature range				−25°C to +85°C
Soldering time at 260°C (1/16 inch below seating plane)				3 sec

MODEL NUMBERS

PART NO. YELLOW	HER	GREEN	MULTI-COLOR	DESCRIPTION	PACKAGE DIMENSION	INTERNAL CIRCUIT DIAGRAM
GMC2875C	GMC2975C	GMC2475C		Anode column, cathode row	A	A
GMA2875C	GMA2975C	GMA2475C		Cathode column, anode row	A	B
			GMA2675C	Cathode column, anode row	B	C

ELECTRICAL/OPTICAL CHARACTERISTICS (T_A = 25°C Unless otherwise specified) QMX 2075C

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Average luminous intensity		3000		μcd	I_F=20 mA
Peak emission wavelength		585		nm	I_F=20 mA
Spectral line half-width		30		nm	I_F=20 mA
Forward voltage, any dot		2.1	2.8	V	I_F=20 mA
Reverse voltage, any dot			100	μA	V_R=5 V

TYPICAL ELECTRICAL/OPTICAL CHARACTERISTIC CURVES (T_A = 25°C Unless otherwise specified)

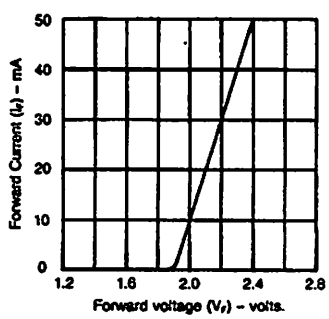

Fig. 1. Forward Current vs. Forward Voltage

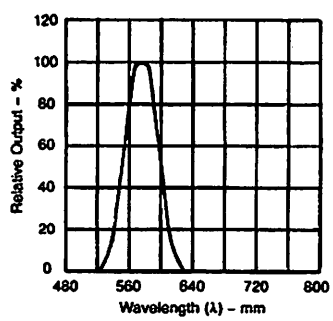

Fig. 2. Spectral Response

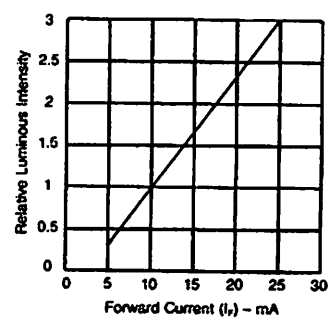

Fig. 3. Relative Luminous Intensity vs. Forward Current

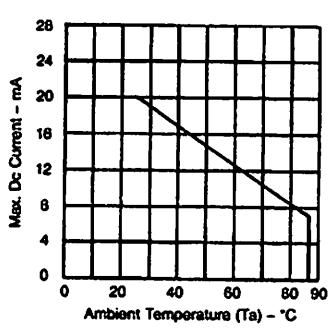

Fig. 4. Maximum Allowable DC Current Per Segment vs. A Function of Ambient Temperature

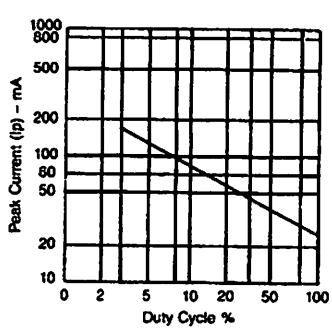

Fig. 5. Luminous Intensity vs. Duty Cycle

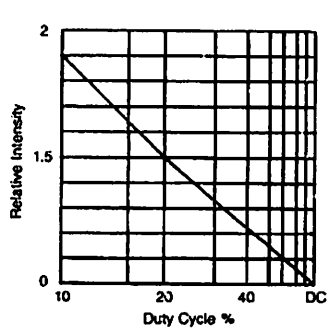

Fig. 6. Max Peak Current vs. Duty Cycle % (Refresh Rate f=1 KHz)

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2.0" 5 × 7 DOT MATRIX DISPLAYS

ELECTRICAL/OPTICAL CHARACTERISTICS (T_A = 25°C Unless otherwise specified) QMX 2975C

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Average luminous intensity		3000		μcd	I_F=20 mA
Peak emission wavelength		635		nm	I_F=20 mA
Spectral line half-width		30		nm	I_F=20 mA
Forward voltage, any dot		2.1	2.8	V	I_F=20 mA
Reverse voltage, any dot			100	μA	V_R=5 V

TYPICAL ELECTRICAL/OPTICAL CHARACTERISTIC CURVES (T_A = 25°C Unless otherwise specified)

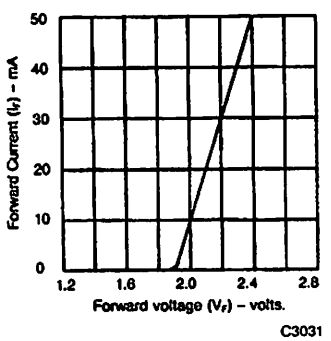


Fig. 1. Forward Current vs. Forward Voltage

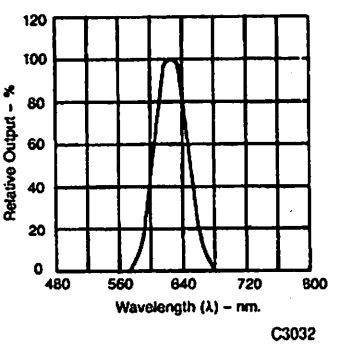


Fig. 2. Spectral Response

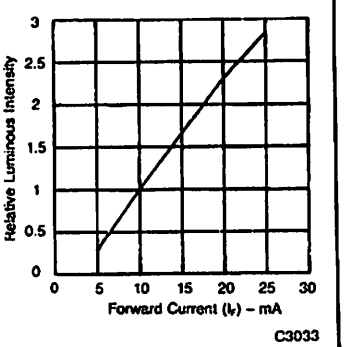


Fig. 3. Relative Luminous Intensity vs. Forward Current

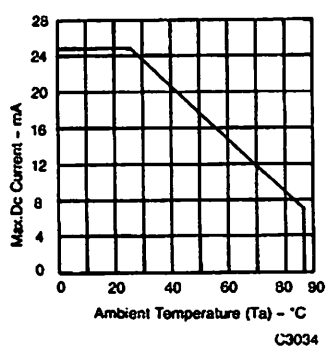


Fig. 4. Maximum Allowable DC Current Per Segment vs. A Function of Ambient Temperature

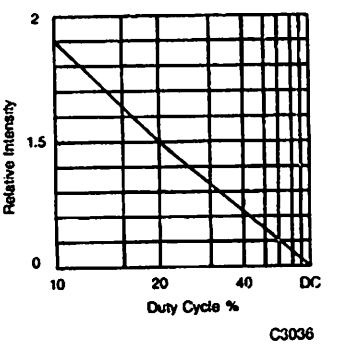


Fig. 5. Luminous Intensity vs. Duty Cycle

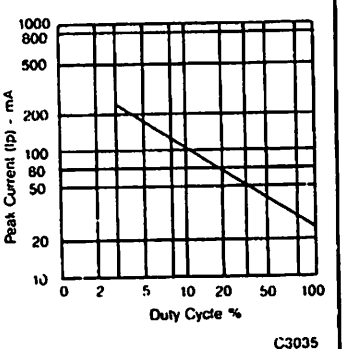


Fig. 6. Max. Peak Current vs. Duty Cycle % (Refresh Rate f=1 KHz)

FAIRCHILD
SEMICONDUCTOR

2.0" 5 × 7 DOT MATRIX DISPLAYS

ELECTRICAL/OPTICAL CHARACTERISTICS (T_A = 25°C Unless otherwise noted)
QMX 2475C

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Average luminous intensity		3000		μcd	I_F=20 mA
Peak emission wavelength		565		nm	I_F=20 mA
Spectral line half-width		30		nm	I_F=20 mA
Forward voltage, any dot		2.1	2.8	V	I_F=20 mA
Reverse voltage, any dot			100	μA	V_R=5 V

TYPICAL ELECTRICAL/OPTICAL CHARACTERISTIC CURVES
(T_A = 25°C Unless otherwise noted)

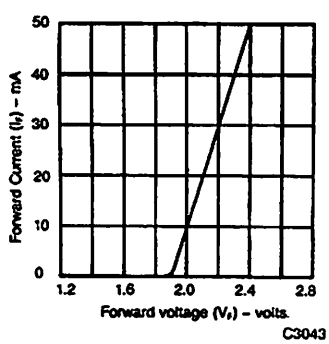


Fig. 1. Forward Current vs. Forward Voltage

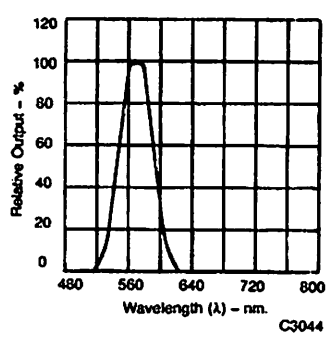


Fig. 2. Spectral Response

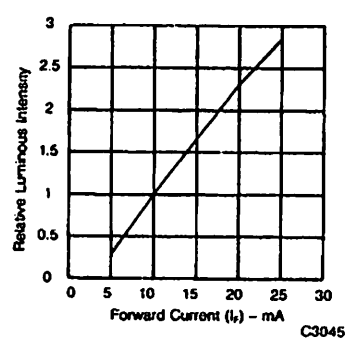


Fig. 3. Relative Luminous Intensity vs. Forward Current

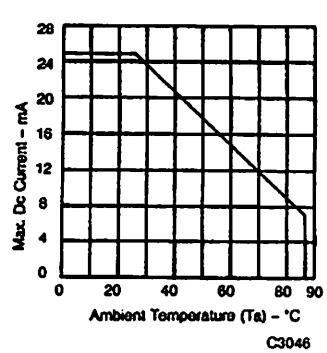


Fig. 4. Maximum Allowable DC Current Per Segment vs. A Function of Ambient Temperature

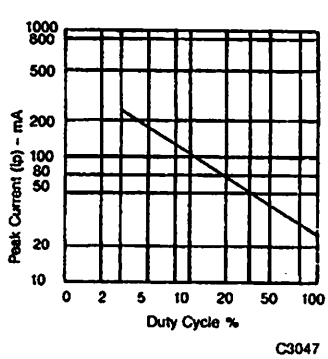


Fig. 5. Max Peak Current vs. Duty Cycle % (Refresh Rate f=1 KHz)

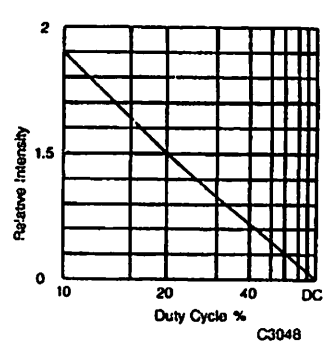


Fig. 6. Luminous Intensity vs. Duty Cycle (Average I=10 mA Per Seg.)

FAIRCHILD
SEMICONDUCTOR

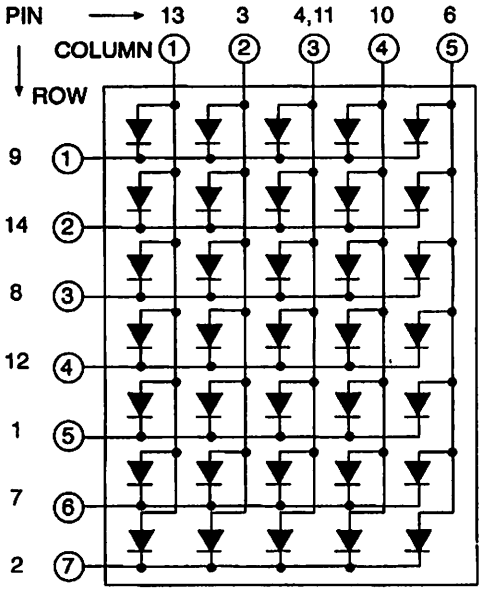
2.0" 5 × 7 DOT MATRIX DISPLAYS

PIN CONNECTION

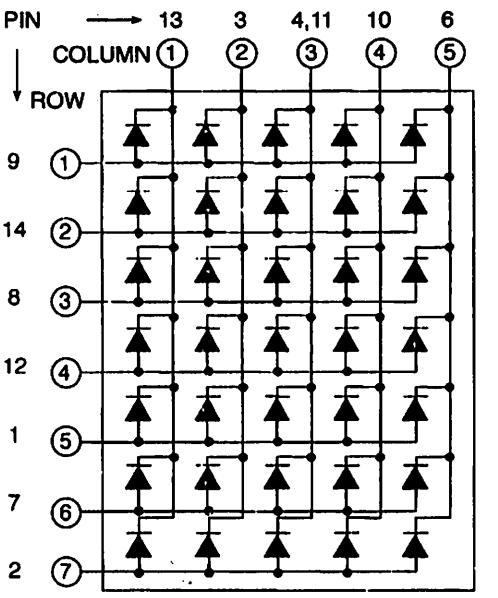
PIN NO.	GMC2X75C	GMA2X75C	GMA2675C
1	Cathode row 5	Anode row 5	Cathode column 1 green
2	Cathode row 7	Anode row 7	Cathode column 2 green
3	Anode column 2	Cathode column 2	Cathode column 2 HER
4	Anode column 3	Cathode column 3	Cathode column 3 HER
5	Cathode row 4	Anode row 4	Anode row 6
6	Anode column 5	Cathode column 5	Anode row 7
7	Cathode row 6	Anode row 6	Cathode column 4 HER
8	Cathode row 3	Anode row 3	Anode row 5
9	Cathode row 1	Anode row 1	No connection
10	Anode column 4	Cathode column 4	Cathode column 5 green
11	Anode column 3	Cathode column 3	Cathode column 5 HER
12	Cathode row 4	Anode row 4	Cathode column 4 green
13	Anode column 1	Cathode column 1	Anode column 3 green
14	Cathode row 2	Anode row 2	Anode row 4
15			Anode row 2
16			Anode row 1
17			Anode row 3
18			Cathode column 1 HER

INTERNAL CIRCUIT DIAGRAM

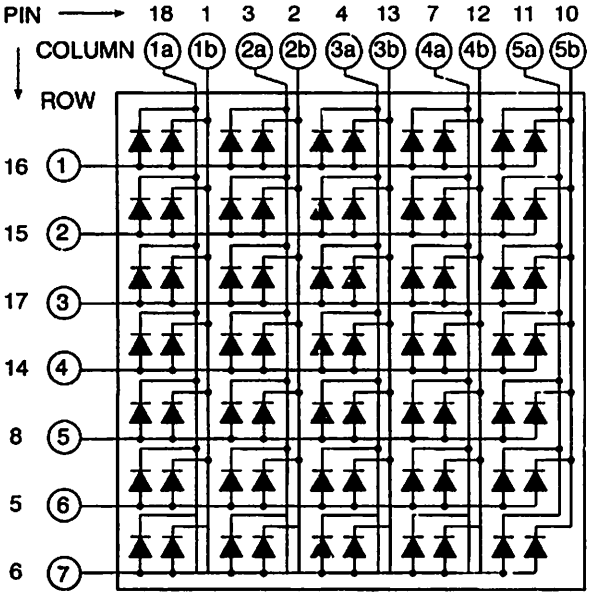
A. GMC2X75C



B. GMA2X75C



C. GMA2675C



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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