LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN PLL BERBASIS PIC16F84 DENGAN PENAMPIL LCD DAN APLIKASINYA SEBAGAI EXCITER FM

SKRIPSI

Diajukan Untuk Memenuhi Salah Satu Syarat Memperoleh Gelar Sarjana Teknik
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Judul Skripsi	: Perencanaan dan pembuatan PLL berbasis PIC16F84 dengan penampil LCD dan aplikasinya sebagai exciter FM.

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ABSTRAKSI

PERENCANAAN DAN PEMBUATAN PLL BERBASIS PIC16F84 DENGAN PENAMPIL LCD DAN APLIKASINYA SEBAGAI EXCITER FM

(Nanang Roni Wibowo, 0217062, Teknik Elektro/Elektronika S-1)
(Dosen Pembimbing : Ir.Sidik Noertjahjono, MT ; Ir.F. Yudi Limpraptono, MT)

Kata Kunci : Transmitter FM, Teknik PLL, Exciter FM

Penggunaan teknik modulasi telah berkembang pesat, diantaranya adalah teknik modulasi frekuensi yang murah dan lebih tahan terhadap noise, namun demikian dalam beberapa aplikasi belum menerapkan teknik kendali dengan umpan balik. Dalam Skripsi ini akan dipaparkan mengenai teknik penguncian phasa menggunakan PLL, yaitu teknik dengan membandingkan sinyal frekuensi output dengan sinyal frekuensi referensi dari oscilator kristal, error dari kedua sinyal tersebut berbentuk beda phasa, dengan *low pass filter* diperoleh tegangan dc untuk mengendalikan VCO dengan sistem antiphase. Sinyal yang akan dibandingkan diambil dari harmonisa kedua frekuensi output, besar pencacahan ditampilkan mikrokontroler ke LCD sebagai nilai frekuensi. Perangkat ini dioperasikan untuk bekerja pada frekuensi FM 87,5 – 108 MHz dengan spasi 100KHz tiap channel. Perangkat lunak digunakan : MPLAB IDE V74.3. Perangkat keras yang digunakan : minimum sistem PIC16F84, VCO, detector phase, ÷N *Counter*, *D Flip Flop,* Oscilator kristal, keypad, dan LCD.

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KATA PENGANTAR

Dengan mengucap puji syukur kehadirat Allah SWT atas segala rahmat, hidayah dan inayah-Nya, sehingga penulis bisa menyelesaikan laporan skripsi dengan judul :

"PERENCANAAN DAN PEMBUATAN PLL BERBASIS PIC16F84 DENGAN PENAMPIL LCD DAN APLIKASINYA SEBAGAI EXCITER FM"

Pada kesempatan ini penulis ingin menyampaikan apresiasi dan terima kasih yang sebesar-besarnya kepada dosen pembimbing skripsi yaitu :

Ir.Sidik Noertjahjono, MT dan Ir.F. Yudi Limpraptono, MT

Yang telah memberikan bimbingan dan pengarahan, sehingga skripsi ini dapat diselesaikan. Selain itu penulis juga ingin menyampaikan terima kasih kepada :

- Bapak Ir.F.Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro S-1.
- Bapak Ir.Sidik Noertjahjono, MT selaku Kasie Laboratorium Jaringan Telekomunikasi.
- Bapak Ir. Eko Nurcahyo, MT selaku Dosen Wali.
- Bapak dan Ibu serta kakak dan adikku tersayang yang telah memberi dukungan materil dan moril beserta doa yang makbul selama penulis menyelesaikan skripsi ini.

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Semenjak komunikasi radio dikembangkan oleh ilmuwan ***Guglielmo Marconi*** tahun 1894, maka sejak itu pula mata dunia terbuka akan pentingnya komunikasi nirkabel yang sanggup menghubungkan antar negara. Komunikasi nirkabel dalam penerapannya di Indonesia menjadi salah satu teknologi yang berkembang dengan cepat, hal ini terjadi dengan melihat kondisi wilayah Indonesia yang mayoritas pegunungan dan laut.

Pergeseran kebutuhan manusia yang menginginkan penyampaian informasi yang cepat dan akurat menjadikan perkembangan komunikasi selalu berkembang, salah satu perkembangan yang sampai sekarang terus dikembangkan adalah teknologi pemodulasian frekuensi karena lebih tahan terhadap noise dari pada modulasi amplitudo.

Kebutuhan masyarakat sekarang sudah mulai bergeser, dahulu informasi hanya diterima melalui isyarat Morse (telegram) kemudian berkembang dengan teknologi pemodulasian amplitudo dan diperbaiki lagi dengan teknologi pemodulasian frekuensi. Kelebihan teknologi pemodulasian frekuensi adalah diperolehnya sinyal informasi lebih jernih mendekati sumber aslinya.

Pada transmitter dengan pemodulasian frekuensi, pengiriman informasi dilakukan dengan merubah perubahan amplitudo sinyal informasi kedalam bentuk perubahan frekuensi dari sinyal *carrier* sehingga diperlukan kestabilan dari frekuensi *center* tidak bergeser.

BAB I

PENDAHULUAN

1.1. Latar Belakang

Sementara komunikasi radio dikembangkan oleh Marconi dan Braun pada tahun 1894, maka sejak itu pula mulai dunia terbuka akan pentingnya komunikasi nirkabel yang sangat mempengaruhi aktivitas manusia. Komunikasi nirkabel dalam penerapannya di Indonesia menjadi salah satu teknologi yang berkembang dengan cepat. Hal ini terjadi dengan melihat kondisi wilayah Indonesia yang mayoritas pegunungan dan laut.

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Karena kestabilan frekuensi *center* menentukan salah satu kualitas pemodulasian, maka pengontrolannya pun diberlakukan berbeda pula. Untuk mengontrol sistem dibutuhkan komponen dan rangkaian elektronik yang mampu menjaga agar nilai elektrisnya tidak bergeser dari yang diinginkan yaitu menggunakan PLL (Phase Locked Loop) pada pemodulasian agar dicapai standarisasi dari CCIR (Commite Consultatif International des Radiocommunication).

1.2. Permasalahan

Berdasarkan latar belakang yang telah diuraikan sebelumnya dapat dirumuskan permasalahannya mencakup:

1. Bagaimana merancang dan membuat rangkaian PLL sebagai pengendali oscilator terkendali tegangan.
2. Bagaimana merancang dan membuat oscilator terkendali tegangan untuk exciter FM.
3. Bagaimana merancang dan membuat perangkat lunak berbasis mikrokontroler PIC16F84.

1.3. Tujuan

Adapun tujuan perancangan dan pembuatan alat ini adalah menerapkan teknologi PLL berbasis mikrokontroler yang memberikan tampilan pada LCD.

1.4. Batasan Masalah

Dalam menyusun tugas akhir ini diperlukan suatu batasan masalah agar tidak menyimpang dari ruang lingkup yang akan dibahas. Adapun batasan masalahnya:

1. Alat ini bekerja pada jalur VHF.
2. Tidak membahas final amplifier.
3. Hanya membahas masalah perancangan perangkat kerasnya .
4. Tidak membahas masalah antenna dan saluran transmisi.
5. Pemroses sinyal informasi, catu daya hanya di jelaskan secara umum.

1.5. Metodologi

Metodologi yang digunakan dalam pembahasan skripsi ini adalah :

1. Studi Literatur rangkaian oscilator, penguat frekuensi tinggi, filter dan pembagi frekuensi serta teori mikrokontroler PIC16F84.
2. Merencanakan dan membuat secara langsung alat dengan praktek secara langsung tiap bagian rangkaian.
3. Melakukan pengujian terhadap tiap bagian alat.
4. Melakukan pengujian keseluruhan sistem yang direncanakan
5. Penyusunan laporan skripsi.

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4. Melakukan pengujian keseluruhan sistem yang direncanakan
5. Penyusunan laporan skripsi.

1.6. Sistematika Penulisan

Penulisan tugas akhir ini terbagi menjadi lima bab dengan sistematika sebagai berikut:

BAB I PENDAHULUAN

Berisi latar belakang, tujuan, permasalahan, batasan masalah, metodologi, dan sistematika penulisan.

BAB II LANDASAN TEORI

Membahas teori – teori dasar sebagai penunjang perencanaan dan pembuatan alat.

BAB III PERENCANAAN DAN PEMBUATAN ALAT

Membahas tentang perencanaan alat baik perangkat keras maupun perangkat lunak sistem berdasarkan diagram blok.

BAB IV PENGUJIAN ALAT

Membahas pengujian tiap bagian dan keseluruhan sistem serta analisa terhadap hasil pengujian..

BAB V PENUTUP

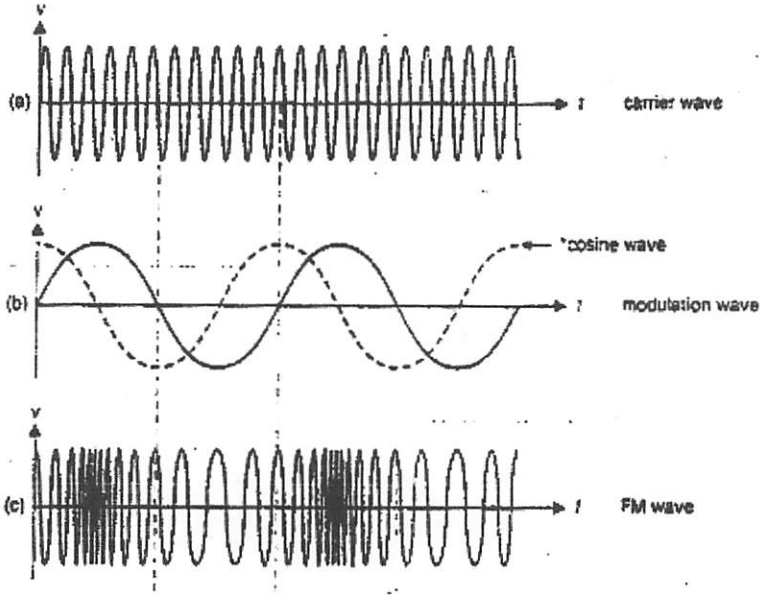
Berisi kesimpulan dan saran.

BAB II

TEORI PENUNJANG

2.1. Modulasi Frekuensi

Merupakan salah satu teknik pemodulasian dimana deviasi frekuensi sinyal carrier disebabkan oleh perubahan amplitude sinyal informasi, sebagaimana ditunjukan dalam gambar 2-1, berikut:



Gambar 2-1. Gelombang FM untuk Sinyal Pemodulasi Gelombang Sinus; (a) Sinyal Carrier; (b) Sinyal Informasi ; (c) Gelombang FM[1]

[1] Hioki. Warren. "Telecommunication Third Edition". Prentice-Hall International.Inc. 1998. USA. Hal 50

2.2. Index Modulasi

Merupakan perbandingan antara deviasi frekuensi maksimum terhadap frekuensi sinyal informasi, dan diberikan oleh persamaan, sebagai berikut :

$$m_f = \frac{\delta}{f_m}$$

indeks modulasi untuk FM sebanding dengan amplitudo dari signal modulasi yang mengakibatkan deviasi (δ) dan juga berbanding terbalik terhadap frekuensi sinyal modulasi.

2.3. Analisa Frekuensi Sinyal FM

Mengingat dalam AM, komponen frekuensi terdiri atas frekuensi carrier tetap dengan sisi band atas dan bawah sama ditunjukan di atas dan bawah frekuensi carrier. Komponen frekuensinya merupakan pencerminan terhadap lainya serta identik, untuk spectrum frekuensi gelombang FM jauh lebih komplek. Untuk sinyal modulasi sinus terhadap frekuensi carrier FM diperoleh sisi band yang tak terhingga, kompleksitas sisi bandnya meningkat dengan kompleksitas sinyal modulasi.

Analisa komponen frekuensi dan amplitudo dalam gelombang FM memerlukan penggunaan matematika integral yang komplek yang diketahui sebagai fungsi *Bessel* jenis pertama pada ordè ke-n, seperti ditunjukan dalam persamaan berikut:

$$\begin{aligned} e_{FM} &= A_c J_0(m_f)\sin\omega_c t + A_c\{J_1(m_f)[\sin(\omega_c+\omega_m)t - \sin(\omega_c-\omega_m)t \\ &+ A_c\{J_2(m_f)[\sin(\omega_c+2\omega_m)t - \sin(\omega_c-2\omega_m)t \\ &+ A_c\{J_3(m_f)[\sin(\omega_c+3\omega_m)t - \sin(\omega_c-3\omega_m)t + ...dst \end{aligned}$$

2.2. Indeks Modulasi

Menunjukkan perbandingan antara deviasi frekuensi maksimum terhadap frekuensi sinyal informasi, dan dituliskan oleh persamaan, sebagai berikut :

$$M_f = \frac{\delta}{f_m}$$

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$$e_{FM} = A_c J_0(m_f)\sin\omega_c t + A_c J_1(m_f)[\sin(\omega_c + \omega_m)t - \sin(\omega_c - \omega_m)t$$
$$+ A_c J_2(m_f)[\sin(\omega_c + 2\omega_m)t - \sin(\omega_c - 2\omega_m)t$$
$$+ A_c J_3(m_f)[\sin(\omega_c + 3\omega_m)t - \sin(\omega_c - 3\omega_m)t + \ldots\text{dst}$$

Keterangan :

e_{FM} = Amplitudo sesaat gelombang FM yang dimodulasi

A_C = Amplitudo puncak Carrier

J_n = Solusi untuk fungsi *Bessel* orde ke-n dari index modulasi m_f

m_f = Indeks Modulasi FM.

Pada persamaan diatas dapat dilihat bahwa gelombang FM berisi nilai tak hingga pada komponen sisi bandnya yang mempunyai amplitudo tersendiri didahului koefisien $J_n(m_f)$. Masing – masing sisiband atas dan bawah digantikan oleh frekuensi carrier oleh integral berlipat dari frekuensi modulasi. Dengan bantuan komputer matematika integral tersebut sudah ditabelkan dan digrafikan seperti berikut:

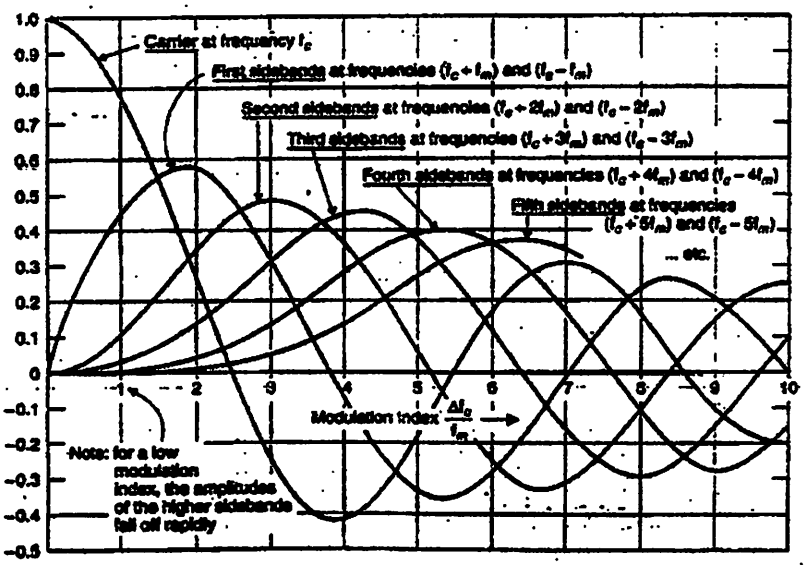
Tabel 2-1. Hasil Perhitungan Fungsi *Bessel*[2]

TABLE 4-1
Bessel functions of the first kind

Modulation Index (m_f)	Carrier Frequency J_0	J_1	J_2	J_3	J_4	J_5	J_6	J_7	J_8	J_9	J_{10}	J_{11}	J_{12}	J_{13}	J_{14}	J_{15}	J_{16}
						to or order of sidebands											
0.00	1.00	--															
0.25	0.98	0.12	—														
0.5	0.94	0.31	0.03														
1.0	0.77	0.44	0.11	0.02	—												
1.5	0.51	0.56	0.23	0.06	0.01	—											
2.0	0.22	0.58	0.35	0.13	0.03	—											
2.5	0.05	0.50	0.45	0.22	0.07	0.02	—										
3.0	0.26	0.34	0.49	0.31	0.13	0.04	0.01	—									
4.0	0.40	0.07	0.36	0.43	0.28	0.13	0.05	0.02									
5.0	0.18	−0.33	0.05	0.36	0.39	0.26	0.13	0.05	0.02	—							
6.0	0.15	−0.28	0.24	0.11	0.36	0.36	0.25	0.13	0.06	0.02	—						
7.0	0.30	0.00	0.30	0.17	0.16	0.35	0.34	0.23	0.13	0.06	0.02	—					
8.0	0.17	0.23	0.11	0.29	0.10	0.19	0.34	0.32	0.22	0.13	0.06	0.03	—				
9.0	0.09	0.24	0.14	−0.18	−0.27	−0.06	0.20	0.33	0.30	0.21	0.12	0.06	0.03	0.01	—		
10.0	0.25	0.04	0.25	0.06	−0.22	−0.23	−0.01	0.22	0.31	0.29	0.20	0.12	0.06	0.03	0.01	—	
12.0	0.05	−0.22	0.08	0.20	0.18	−0.07	−0.24	−0.17	0.05	0.23	0.30	0.27	0.20	0.12	0.07	0.03	0.01
15.0	0.01	0.21	0.04	−0.19	−0.12	0.13	0.21	0.03	−0.17	−0.22	−0.09	0.10	0.24	0.28	0.25	0.18	0.12

Source: E. Jahnke, *Bessel Functions*, Dover Publications, Inc., New York, N.Y., 1948. Courtesy of the publisher.

[2] Hioki. Warren. "Telecommunication Third Edition". Prentice-Hall International.Inc. 1998. USA. Hal 54



Grafik 2-1. Komponen Spectral dari Frekuensi Carrier[3]

2.4. Kebutuhan Bandwitdh pada FM

Secara teori gelombang FM mempunyai band sisi tak hingga, sehingga membutuhkan bandwitdh tak terhingga yang dibutuhkan untuk pemancaran dan penerimaan. Dalam kenyataan, bagaimanapun amplitudo band sisi diabaikan diluar range frekuensi yang pasti dari carrier. Range tersebut merupakan fungsi dari indeks modulasi m_f, sehingga semakin tinggi indeks modulasi semakin tinggi bandwitdh yang dibutuhkan.

$$BW = 2(n * f_n)$$

Dengan menggunakan diatas dapat diperoleh kebutuhan bandwitdh, dengan n adalah komponen band sisi tertinggi, f_m adalah frekuensi modulasi tertinggi. Pada tahun 1938 J.R. Carson dalam memorandumnya menuliskan

[3] Hioki. Warren. "Telecommunication Third Edition". Prentice-Hall International.Inc. 1998. USA. Hal 53

Gambar 2-1. Komponen Spektral dari Frekuensi Carrier[5]

2.4. Kebutuhan Bandwidth pada FM

Secara teori gelombang FM memerlukan band sisi tak hingga, sehingga membutuhkan bandwidth tak terhingga yang dibutuhkan untuk pemancaran dan penerimaan. Dalam kenyataan, bagaimanapun amplitudo band sisi dibatasi dalam range frekuensi yang pasti dari carrier. Range tersebut merupakan fungsi dari indeks modulasi m_f, sehingga semakin tinggi indeks modulasi semakin tinggi bandwidth yang dibutuhkan.

$$BW = 2(n * f_m)$$

Dengan menggunakan cara dapat diperoleh kebutuhan bandwidth dengan n adalah komponen band sisi terhingga, f_m adalah frekuensi modulasi terhingga. Pada tahun 1938 J.R. Carson dalam memorandumnya menuliskan

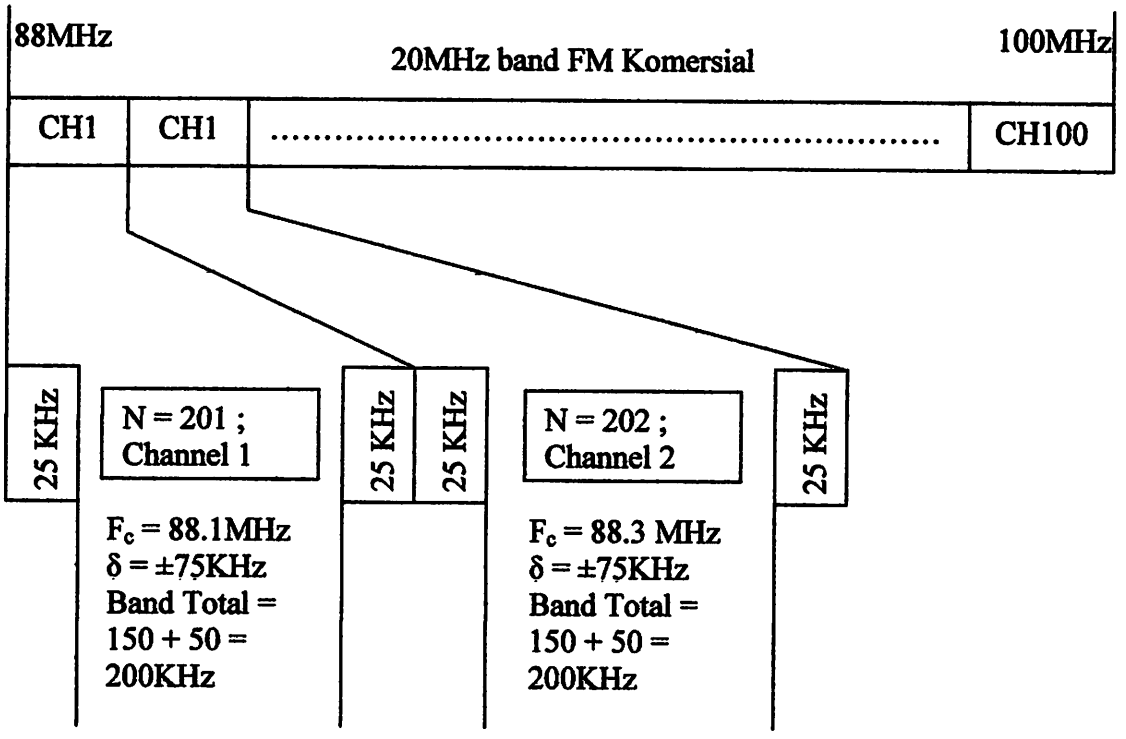
[5] Hioki, Wayne. "Telecommunication Third Edition". Prentice-Hall International,Inc. 1998. USA. Hal 53

bahwa bandwitdh yang diperlukan untuk transmisi gelombang modulasi sudut sebagaimana dirumuskan berikut:

$$BW = 2(\delta + f_m)$$

2.5. FM Broadcast

Band untuk FM komersial, sebagaimana ditunjukan dalam Gambar 2-2. diperluas dari 88 – 108 MHz dan dibagi kedalam 100 channel, alokasi bandwitdh yang diperbolehkan oleh FCC sebesar 200KHz dan ditunjukan dalam nilai numerik N.



Gambar 2-2. Band FM Broadcast Komersial[4]

[4] Hioki. Warren. "Telecommunication Third Edition". Prentice-Hall International.Inc. 1998. USA. Hal 60

Masing- masing channel range mulai 88,1 MHz dengan N = 201 hingga 107,9 MHz dengan N = 300, hal ini dapat ditemukan dengan menggunakan persamaan:

$$N = 5(f - 47{,}9)$$

deviasi sinyal carrier yang diperbolehkan adalah ±75KHz, pemancar diperbolehkan untuk memodulasi frekuensi carrier dengan range band frekuensi dari 50 Hz ke maksimum 15KHz, sehingga range indeks modulasinya 5 untuk f_m 15KHz dan 1500 untuk f_m 50Hz, sehingga kebutuhan bandwitdh sebesar 150KHz dengan 25KHz band pandu pada sisi atas dan bawah frekuensi center, sehingga total bandwitdh keseluruhan 200KHz.

2.6. Pre Emphasis

Pengaruh dari noise terhadap signal carrier FM sebanding langsung terhadap frekuensi modulasi. Meningkatnya frekuensi modulasi f_m, menurunkan SNR (*signal to noise ratio*), karena informasi yang dikirimkan seperti suara dan music mempunyai frekuensi yang berubah, dan disalurkan melalui band modulasi yang diberikan, sehingga pemancar perlu untuk meningkatkan level signal dari frekuensi modulasi yang lebih tinggi sebelum dilakukan proses modulasi, hal ini untuk memelihara SNR yang seragam terhadap frekuensi modulasi yang lebih tinggi dan biasa disebut *Pre-Emphasis*, kebalikan dari proses ini disebut *De-Emphasis* yang diletakan pada bagian penerima.

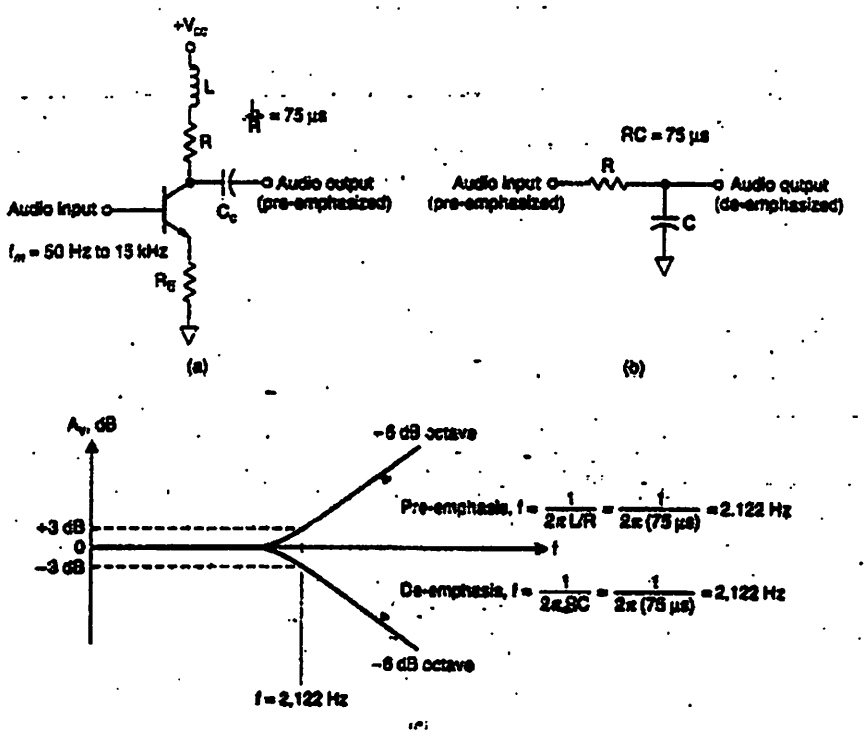
Missing- missing channel range mulai 88.1 MHz dengan N = 291 hingga 107,9 MHz dengan N = 300. Hal ini dapat ditentukan dengan menggunakan persamaan:

$$\lambda = 5(\gamma - 472,9)$$

deviasi sinyal carrier yang diperbolehkan adalah ±75KHz. pemancar diperbolehkan untuk memodulasi frekuensi carrier dengan range band frekuensi dari 50 Hz ke maksimum 15KHz. sehingga range indeks modulasinya 5 untuk f_m 15KHz dan 1500 untuk f_m 50Hz. sehingga kebutuhan bandwidth sebesar 150KHz dengan 25KHz band pandu pada sisi atas dan bawah frekuensi center. sehingga total bandwidth keseluruhan 200KHz.

2.6. Pre Emphasis

Pengaruh dari noise terhadap sinyal carrier FM sebanding langsung terhadap frekuensi modulasi. Meningkatnya frekuensi modulasi f_m menurunkan SNR (signal to noise ratio). karena informasi yang dikirimkan seperti suara dan music mempunyai frekuensi yang berubah. dan disalurkan melalui band modulasi yang diberikan. sehingga pemancar perlu untuk meningkatkan level sinyal dari frekuensi modulasi yang lebih tinggi sebelum dilakukan proses modulasi. hal ini untuk memelihara SNR yang seragam terhadap frekuensi modulasi yang lebih tinggi dan biasa disebut Pre-Emphasis. kebalikan dari proses ini disebut De-Emphasis yang dilakukan pada bagian penerima.



Gambar 2-3. Rangkaian Emphasis dengan konstanta waktu 75µS serta Respon Frekuensi[5]

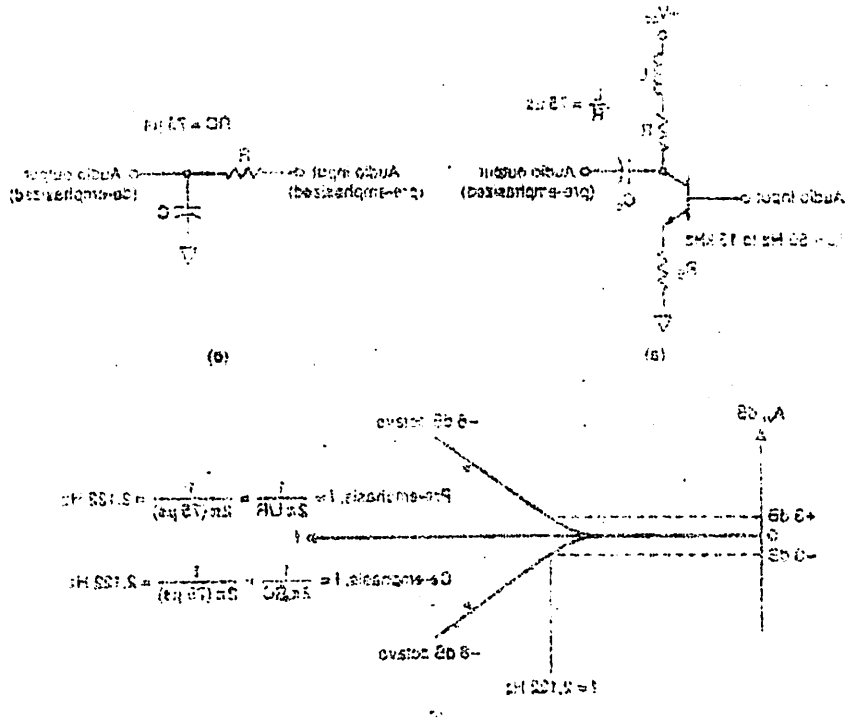
Berdasarkan peraturan FCC stasiun pemancar FM broadcast untuk menyertakan rangkaian Pre-Emphasis dengan konstanta waktu 75µS.

2.7. Daya pada Gelombang FM

Daya total pada gelombang FM didistribusikan pada carrier dan komponen band sisinya. Jika dijumlahkan daya pada carrier dan semua band sisinya untuk beberapa indeks modulasi, akan sama dengan daya total dari carrier tak termodulasi, sehingga dapat dinyatakan :

$$P_T = \frac{V_{Crms}^{\ 2}}{R}$$

[5] Hioki. Warren. "Telecommunication Third Edition". Prentice-Hall International.Inc. 1998. USA. Hal 67



Gambar 2-3. Rangkaian Emphasis dengan Konstanta waktu 75μs serta Respon Frekuensi[2]

Berdasarkan peraturan FCC siaran pemancar FM broadcast untuk menyerakan rangkaian Pre-Emphasis dengan konstanta waktu 75μs.

2.7. Daya pada Modulasi FM

Daya total pada gelombang FM didistribusikan pada carrier dan komponen band sisinya. Jika dijumlahkan daya pada carrier dan semua band sisinya untuk beberapa indeks modulasi, akan sama dengan daya total dari carrier tak termodulasi, sehingga dapat dinyatakan :

$$P_t = \frac{V_{c(rms)}^2}{R}$$

[2] Hioki, Warren, "Telecommunication Third Edition", Prentice-Hall International,Inc. 1998, USA. Hal 67

sedangkan untuk carrier yang termodulasi :

$$P_T = P_{J0} + P_{J1} + P_{J2} + P_{J3} + ... + P_{Jn}$$

$$P_T = \frac{V_{J0}^{\ 2}}{R} + \frac{V_{J1}^{\ 2}}{R} + \frac{V_{J2}^{\ 2}}{R} + \frac{V_{J3}^{\ 2}}{R} + ... + \frac{V_{Jn}^{\ 2}}{R}$$

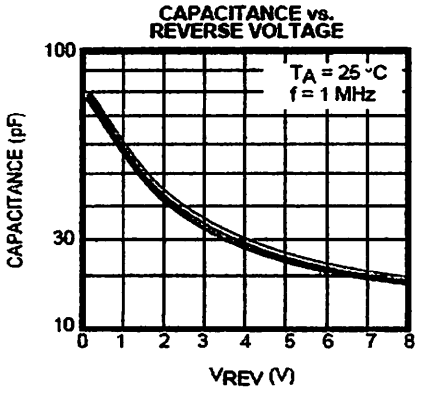
dengan P_T adalah daya total rms dari gelombang tak termodulasi, V_{Crms} adalah tegangan rms signal carrier, R adalah resistansi beban dalam hal ini 50Ω.

2.8. Modulator FM

Terdapat dua metode untuk menghasilkan signal FM : langsung dan tak langsung. Metode langsung terjadi ketika signal modulasi secara langsung digunakan untuk merubah frekuensi atau phasa dari signal carrier. Sedangkan metode tak langsung digunakan untuk merubah phasa dari signal carrier, yang secara tak langsung merubah frekuensinya.

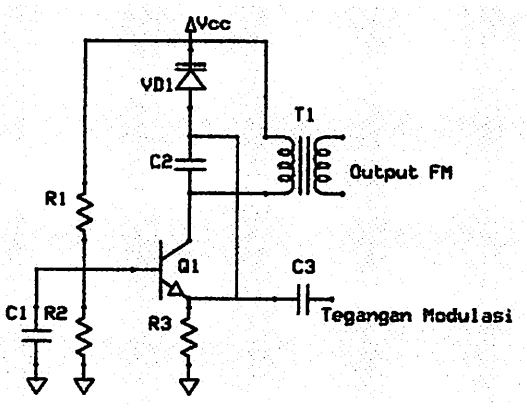
- Modulator Varactor

Modulator varactor menggunakan dioda varactor pada *tank circuits* untuk memperoleh signal FM langsung. Dioda varactor merupakan komponen semikonduktor yang diproduksi khusus untuk mempunyai sifat kapasitif pada saat dibias balik, yang membedakan dioda varactor dengan lainya adalah perbandingan pengaturannya yang lebar, sebagai contoh pada gambar 2-4.



Grafik 2-2. Kurva Karakteristik Dioda Varactor[6]

Perbandingan pengaturannya dinyatakan sebagai perbandingan kapasitansi *junction* C_t yang diukur pada saat tegangan balik 1Volt dan kapasitansi *junction* C_t pada saat tegangan balik 8 volt, diperoleh perbandingan sebesar 1:3.



Gambar 2-4. Aplikasi Dioda Varactor pada Oscilator Colpitts[7]

Dioda varactor dibias oleh tegangan Vcc dan potensial emitor Q1, umpan balik diambilkan dari *tank circuits* dan di berikan ke emitor Q1. signal input audio memodulasi kapasitansi dioda varactor, selanjutnya frekuensi resonansi dari *tank*

[6] Datasheet Dioda Varactor MV2109
[7] Hioki. Warren. "Telecommunication Third Edition". Prentice-Hall International.Inc. 1998. USA. Hal 69

circuits berubah dengan tegangan sesaat dari signal modulasi, sehingga dihasilkan signal FM pada output T1.

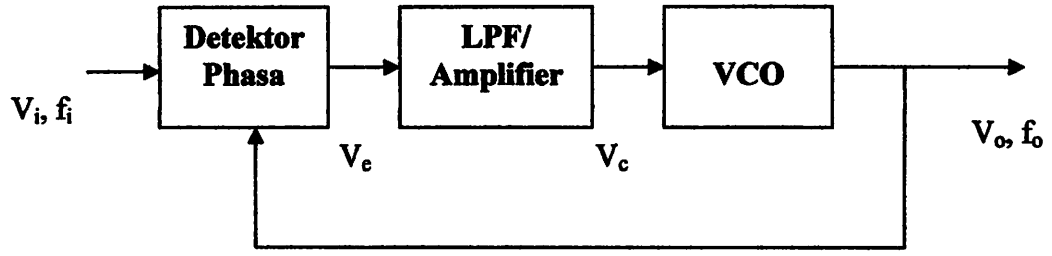
- Modulator Reactance

Modulator reaktansi adalah metode lain untuk menghasilkan FM secara langsung, yaitu dengan menempatkan komponen L atau C variabel pada *tank circuits* dari oscilator frekuensi carrier dan reaktansinya dibuat berubah sebagai fungsi dari signal modulasi.

2.9. PLL (*Phase Lock Loop*)

PLL merupakan sistem umpan balik elektronik yang terdiri atas detektor phasa, kombinasi tapis lolos bawah dan penguat, serta oscilator yang dikendalikan oleh tegangan atau VCO (*Voltage Controlled Oscilator*). Mengkombinasikan fungsi tersebut kedalam sistem loop tertutup membolehkan pelacakan frekuensi dan phasa. Saat hal ini terjadi VCO dikatakan dalam kondisi terkunci phasanya terhadap sinyal input.

VCO menghasilkan sinyal yang frekuensinya kira –kira sama dengan frekuensi *free-running*. Frekuensi ini merupakan frekuensi pada saat PLL tidak terkunci atau loop terbuka. VCO dirancang sehingga frekuensi outputnya lebih besar dari kebutuhan output PLL dan nilai frekuensinya dikendalikan oleh tegangan pada inputnya, bentuk dasar dari PLL dapat digambarkan sebagai berikut:



Gambar 2-5. Diagram Blok Dasar PLL[8]

Ketika signal input V_i dengan frekuensi f_i diberikan ke detektor phasa, frekuensinya dibandingkan dengan frekuensi output f_o dari VCO, hasil perbandingan tersebut menghasilkan tegangan *error* V_e yang menunjukan beda phasa antara frekuensi input f_i dan frekuensi output f_o, tegangan ini kemudian difilter dan dikuatkan untuk menghasilkan tegangan kendali VCO, yaitu V_c. Yang membetulkan frekuensi VCO menjaga penguncian phasanya terhadap sinyal input.

- Detektor Phasa

Pada prinsipnya detektor phasa merupakan rangkaian *mixer* (pencampur) yang menghasilkan bentuk penjumlahan dan pengurangan dari sinyal input dan output. Jika sinyal input dan output dinyatakan sebagai berikut :

$$v_i = V_{in} Sin\omega_{in} t$$
$$v_o = V_{out} Sin\omega_{out} t$$

tegangan *error* sesaat dari output detektor phasa adalah :

[8] Hioki. Warren. "Telecommunication Third Edition". Prentice-Hall International.Inc. 1998. USA. Hal 94

$$v_e = v_{in} * v_{out} = V_{in} Sin\omega_{in} t * V_{out} Sin\omega_{out} t$$
$$v_e = \frac{1}{2} V_{in} V_{out} [Cos(\omega_{in} - \omega_{out})t - Cos(\omega_{in} + \omega_{out})t]$$

Persamaan diatas terdapat dua bentuk persamaan penjumlahan dan pengurangan, dengan memfilter bentuk penjumlahan dan menguatkan bentuk pengurangan diperoleh tegangan kendali VCO.

$$V_c = \frac{1}{2} A_V V_{in} V_{out} [Cos(\omega_{in} - \omega_{out})t$$

berdasarkan persamaan diatas diperoleh bahwa saat kondisi terkunci ($f_{in} = f_{out}$), ω_{in}–ω_{out} adalah sama dengan nol dan tegangan kendali VCO, V_c menjadi sebuah tegangan DC tetap.level tegangan ini diperlukan PLL untuk menjaga peguncian terhadap sinyal input. Apabila frekuensi sinyal input berubah, tegangan kendali VCO juga ikut berubah dan menyebabkan frekuensi output VCO juga berubah.

- LPF (*Low Pass Filter*)

Rangkaian filter ini sebagaimana telah dikemukan diatas berfungsi memfilter sinyal frekuensi tinggi dari detektor phasa agar tidak dikuatkan sehingga hanya sinyal dibawah frekuensi cutoff saja yang diteruskan.

- VCO (*Voltage Controlled Oscillator*)

Merupakan salah satu jenis oscilator yang dapat dirubah dengan memberikan bias tegangan, teknik yang paling sederhana untuk melakukan pengendalian ini dengan menggunakan dioda varactor.

➢ Frekuensi Referensi

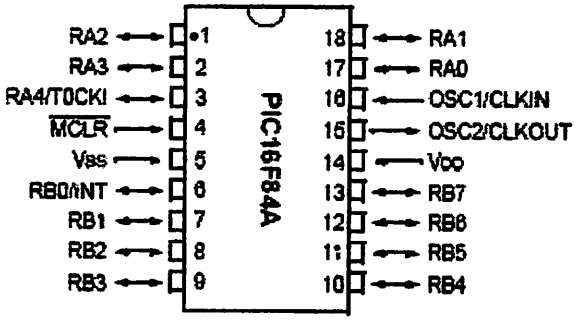
Frekuensi referensi harus mempunyai ketelitian dan kestabilan yang tinggi sehingga digunakan oscilator kristal sebagaimana diketahui kristal mempunyai nilai Q yang tinggi. Fungsi dari bagian ini adalah sebagai frekuensi inputan yang dibandingkan dengan frekuensi tinggi VCO.

➢ *Devider*

Fungsi rangkaian ini adalah mencacah frekuensi keluaran dari VCO sehingga sama dengan frekuensi dari oscilator referensi, rangkaian ini akan terus melakukan pencacahan sampai diperoleh frekuensi outputnya sama dengan frekuensi referensi.

2.10. Mikrokontroler PIC16F84

Merupakan salah satu mikrokontroler yang dikeluarkan oleh perusahaan Microchip.Inc dari keluarga PIC16Fxx, yang dikemas dalam bentuk *DIP (Dual in Line Package)*,dengan menggunakan ICSP bentuk fisik dari mikrokontroler ini sebagaimana gambar berikut :



Gambar 2-6. Pin Diagram PIC16F84[9]

[9] http://www.microchip.com/

- Frekuensi Referensi

Frekuensi referensi harus mempunyai kestabilan dan ketelitian yang tinggi sehingga digunakan oscillator kristal sebagaimana dikatahui kristal mempunyai nilai Q yang tinggi. Fungsi dari bagian ini adalah sebagai frekuensi input yang dibandingkan dengan frekuensi tinggi VCO.

- Devider

Fungsi rangkaian ini adalah menurunkan frekuensi keluaran dari VCO sehingga sama dengan frekuensi dari oscillator referensi. rangkaian ini akan terus melakukan pencocahan sampai diperoleh frekuensi outputnya sama dengan frekuensi referensi.

2.10. Mikrokontroler PIC16F84

Merupakan salah satu mikrokontroler yang dikeluarkan oleh perusahaan Microchip.Inc dari keluarga PIC16Fxx. yang dikemas dalam bentuk DIP (Dual in Line Package).dengan menggunakan ICSP bentuk fisik dari mikrokontroler ini sebagaimana gambar berikut :

Gambar 2-6. Pin Diagram PIC 16F84[9]

[9] http://www.microchip.com/

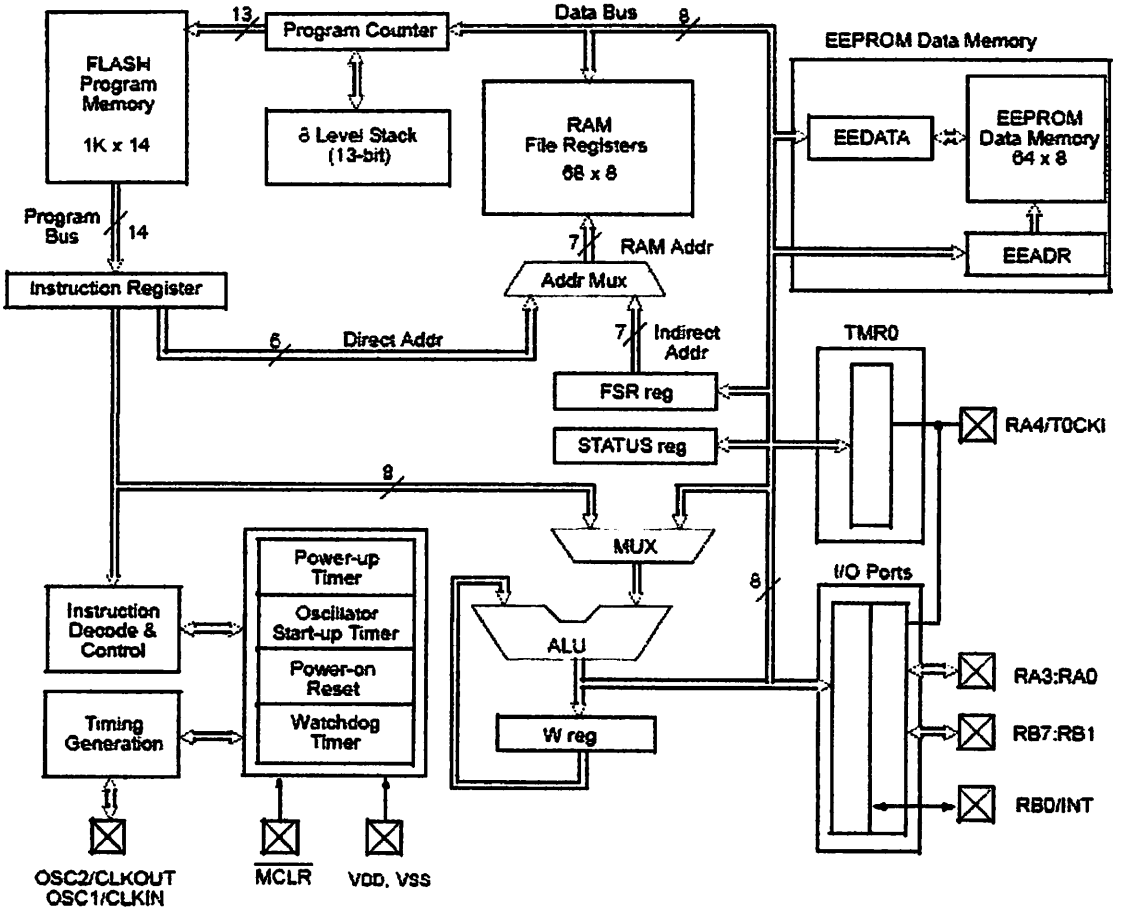
Fungsi Pin- pin pada mikrokontroler PIC16F84 :

1. OSC1/CLKIN : Input sumber clock external atau input oscilator kristal.
2. OSC2/CLKOUT : output oscilator kristal. Dihubungkan ke kristal atau resonator pada mode oscilator kristal. Pada mode RC, pin OSC2 mengeluarkan CLKOUT, yang mempunyai ¼ frekuensi OSC1 dan menyatakan kecepatan cycle instruksi.
3. MLCR : Tegangan input Master Clear / reset, aktif *low* akan mereset mikrokontroler.
4. RA0-RA4 : PortA input output dua arah, untuk RA4/TOCK1 dapat berfungsi sebagai input clock TMR0 timer / counter. Outputnya *Open Drain.*
5. RB0- RB7 : PortB input output dua arah, dapat diprogram untuk pull-up internal melalui software. RB0/INT juga berfungsi sebagai input interrupt, RB4-RB7 dapat difungsikan sebagai pin interrupt, RB6-RB7 digunakan sebagai jalur clock dan data pada komunikasi serial.
6. Vss : Ground bagi pin- pin I/O.
7. Vdd : jalur positif bagi pin- pin I/O.

2.10.1. Arsitektur mikrokontroler

Mikrokontroler PIC16Fxx merupakan mikrokontroler dari keluarga RISC (*Reduce Instruction Set Command*), yaitu mikrokontroler yang memori data dan

memori programnya mempunyai bus sendiri, hal ini sebagaimana ditunjukan dalam Gambar berikut :



Gambar 2-7. Arsitektur MCU PIC16F84 [10]

Feature dari mikrokontroler PIC16F84 :

1. 35 instruksi
2. Instruksi hanya 1 *cycle* terkecuali instruksi percabangan dan lompatan 2 *cycle*.

[10] http://www.microchip.com/

3. 1024 memori program
4. 68 byte memori data RAM
5. 64 byte memori data EEPROM
6. lebar memori program 14 bit
7. lebar memori data 8 bit
8. mempunyai 15 SFR (*Special Function Register*)
9. 8 level stack
10. mempunyai 4 sumber interrupt :
    a. interrupt eksternal pin RB0/ INT
    b. overflow dari TMR0
    c. PORTB.4 – PORTB7
    d. Proses penulisan pada EEPROM lengkap.

2.10.2. Organisasi Memori

Pada mikrokontroler PIC terdapat dua block memori yaitu memori program dan memori data, dengan masing –masing memiliki bus tersendiri, sehingga dapat dilakukan pengaksesan secara bersamaan.

Memori data kelompokan menjadi *general perpose RAM* dan *Special Function Register(SFRs)*. Disamping itu terdapat pula memori data EEPROM yang mempunyai metode pengalamatan sendiri.

- Memori Program

PIC dari keluarga PIC16Fxx mempunyai 13 bit program counter sehingga mampu mengalamati sampai 8Kx14 spasi memori program, untuk PIC16F84 1Kx14 pertama diimplementasikan secara khusus, pengaksesan

3. 1024 memori program

4. 68 byte memori data RAM

5. 64 byte memori data EEPROM

6. lebar memori program 14 bit

7. lebar memori data 8 bit

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9. 8 level stack

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b. overflow dari TMR0

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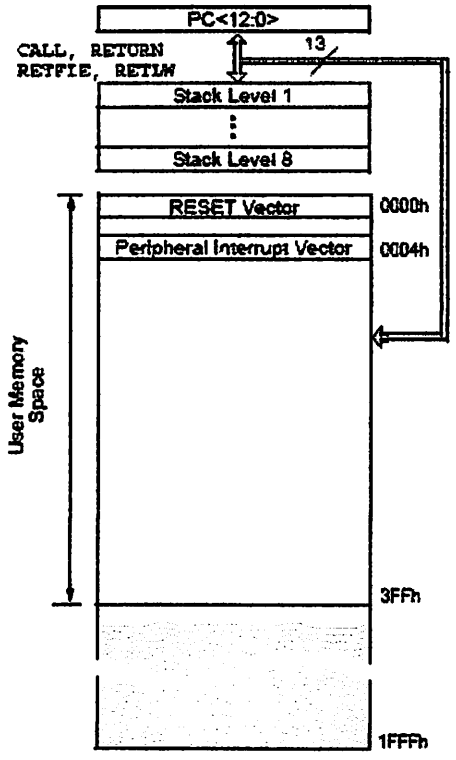
Memori data kelompokan menjadi general purpose RAM dan Special Function Register(SFR). Disamping itu terdapat pula memori data EEPROM yang mempunyai metode pengalamatan sendiri.

- Memori Program

PIC dari keluarga PIC16Fxx mempunyai 13 bit program counter sehingga mampu mengalamati sampai 8Kx14 spasi memori program. untuk PIC16F84 1Kx14 perrama diimplementasikan secara khusus. pengaksesan

terhadap bagian ini akan menimbulkan masalah sehingga untuk lokasi 20h, 420h,820h,c20h,1020h,1420h,1820h, dan 1c20h instruksinya akan sama.



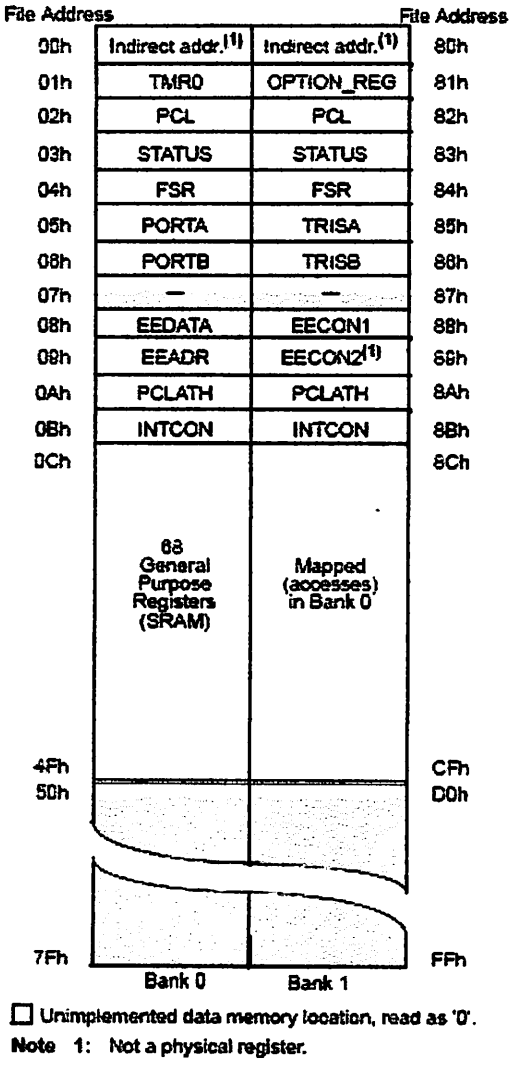
Gambar 2-7. Peta Memori Program PIC16F84[11]

Vector Reset berada pada alamat 0000h sedangkan vector interrupt berada pada alamat 0004h.

- Memori Data

Memori data dipisahkan menjadi dua wilayah, yang pertama adalah register fungsi khusus atau SFR, dan kedua wilayah Register tujuan umum atau GPR, SFR berfungsi sebagai pengendali kerja dari perangkat.

[11] http://www.microchip.com/



Gambar 2-8. Peta Register File PIC16F84[12]

Kapasitas memori data dibank kan untuk kedua SFR maupun GPR, wilayah GPR dibankan untuk mengijinkan lebih besar 116 byte, sedangkan wilayah bank SFR adalah untuk mengendalikan fungsi peripheral, untuk melakukannya diperlukan bit yang mengatur perpindahan antar bank yang diletakan pada register STATUS yaitu pada bit RP0.

[12] http://www.microchip.com/

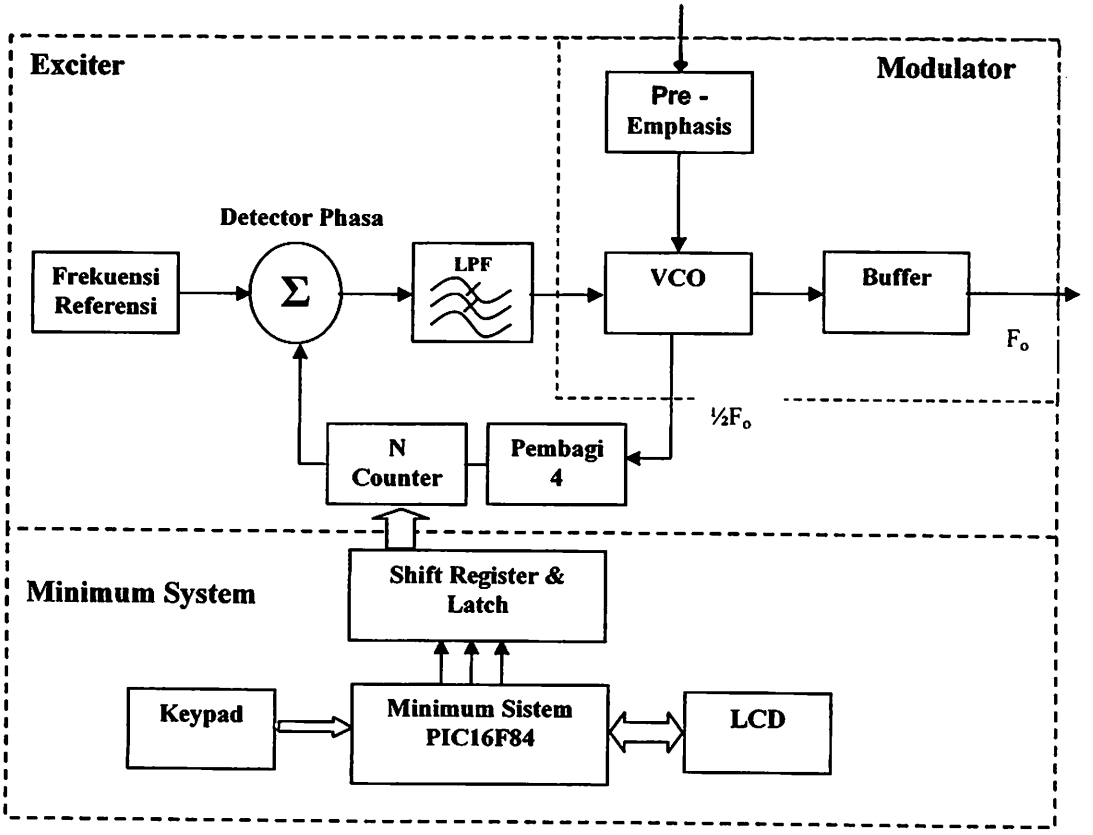
BAB III

PERENCANAAN DAN PEMBUATAN ALAT

3.1. Gambaran Umum

Alat yang dirancang berfungsi sebagai pembangkit sinyal carrier pada transmiter FM dengan kekuatan daya pancar 1 Watt menggunakan sistem pengendalian PLL berbasiskan mikrokontroler.

Pada bab III ini hanya membahas tentang perencanaan dan realisasinya pada sistem transmitter berbasiskan PLL. Adapun diagram blok dari alat yang dirancang sbb:



Gambar 3-1. Diagram Blok Exciter FM

3.2. Perancangan Alat

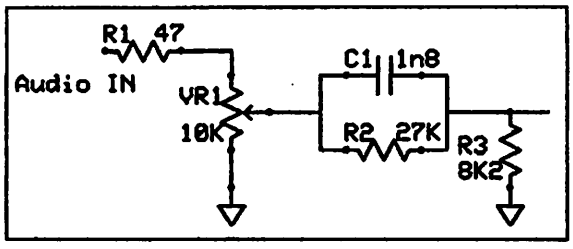
Pada transmitter ini terdapat tiga hal pokok yang hendak dirancang, yaitu : Unit RF, Unit PLL, Unit Minimum Sistem, dengan masing- masing bagian terdapat sub bagian, sebagai berikut :

1. Unit RF
    a. Pre-Emphasis
    b. LPF (*Low Pass Filter*)
    c. VCO (*Voltage Controlled Oscillator*)
    d. Penguat Penyangga / Buffer
2. Unit PLL
    a. Oscilator Lokal
    b. Detektor Fasa
    c. Pembagi 4
    d. N Counter
3. Unit Minimum Sistem PIC16F84

3.2.1. Unit RF

3.2.1.1. Pre- Emphasis

Untuk menyeragamkan level audio pada seluruh range frekuensinya diperlukan komponen yang mampu menaikan level audio untuk frekuensi yang lebih tinggi. FCC menyatakan konstanta waktu $\tau = RC = 75\mu S$ untuk USA dan $50\mu S$ untuk Inggris.



Gambar 3-2. Skematik Rangkaian Pre – Emphasis

Untuk $\tau = RC = 75\mu S$.

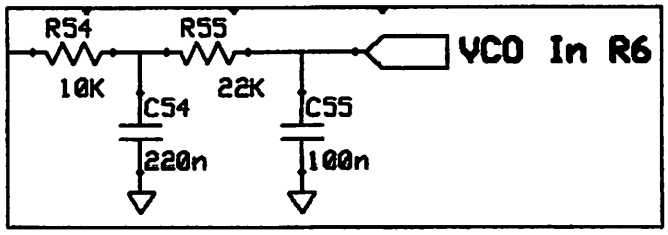
$\tau = R2 * C1$

$= 27.10^3 * 1{,}8.10^{-9}$

$= 48{,}6\mu S$

3.2.1.2. LPF (*Low Pass Filter*)

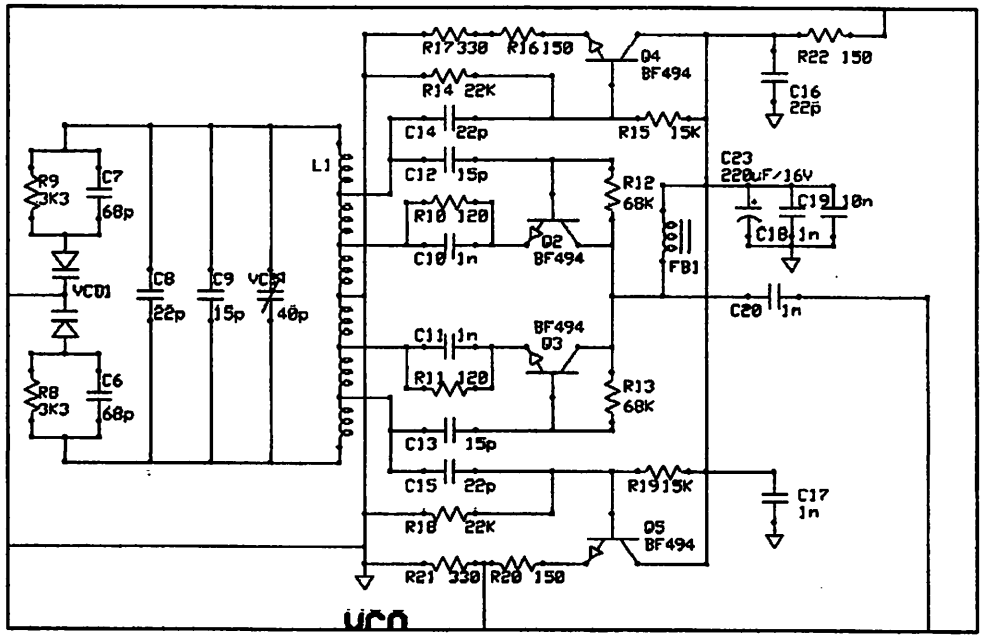
Karakteristik utama sistem PLL sepenuhnya ditentukan oleh bagian ini, dua fungsi utma filter adalah menghilangkan komponen frekuensi tinggi dan noise dari keluaran detektor fasa, LPF direncanakan menggunakan komponen passive, seperti dalam gambar 3-3.



Gambar 3-3. LPF (*Low Pass Filter*)

3.2.1.3. VCO (*Voltage Controlled Oscilator*)

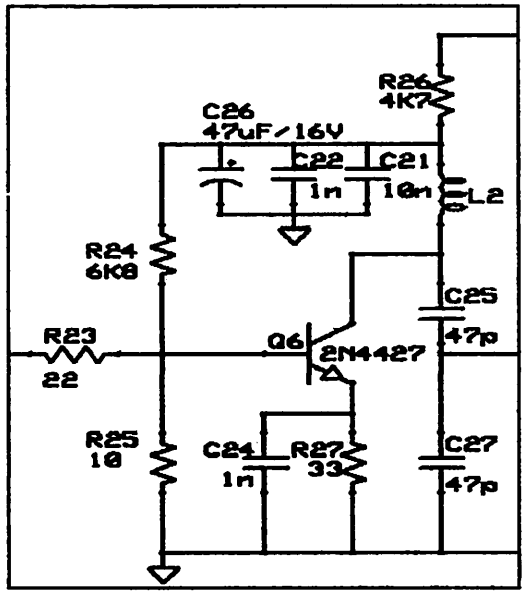
Sebelum signal audio dipancarkan terlebih dahulu harus dimodulasikan ke rangkaian modulator FM, dimana perubahan amplitudo signal informasi tersebut dirubah ke dalam bentuk perubahan frekuensi carrier. Adapun bentuk dari oscilator menggunakan jenis hartley yang berkerja secara antiphase, sehingga satu oscilator bekerja pada separuh dari frekuensi outputnya. Adapun bentuk VCO yang direncakan :



Gambar 3-4. Rangkaian VCO

3.2.1.4. Penguat Penyangga/ Buffer

Rangkaian buffer disini berfungsi sebagai pemegang kestabilan dari osilator modulator ketika dibebani rangkaian selanjutnya. Konfigurasi rangkaian menggunakan kelas A dengan transistor 2N4427A. Tujuan digunakan rangkaian kelas A supaya signal output tetap linier. Berikut gambar rangkaian buffer:

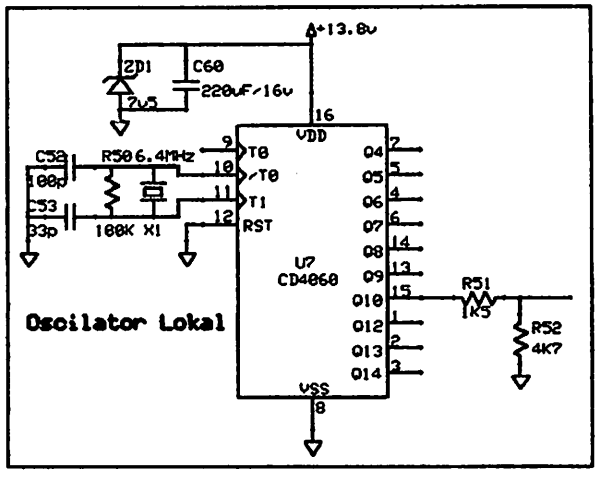


Gambar 3-5. Rangkaian Buffer

3.2.2. Unit PLL

3.2.2.1. Oscilator Lokal

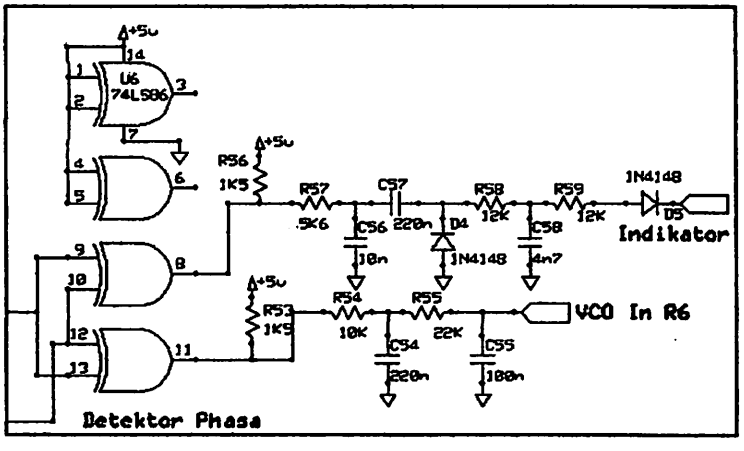
Sebelum phase detector bekerja, diperlukan osilator referensi yang dibentuk dari kristal osilator fundamental 6.4 MHz yang dibentuk dengan IC TTL agar didapat bentuk signal square. Kemudian frekuensi 6.4 MHz ini dibagi menggunakan IC CMOS HCF4060 14-Stage Ripple Counter dengan pembagi 1024 sehingga outputnya menjadi 6.25 KHz. Berikut adalah gambar rangkaian osilator referensi beserta pembaginya :



Gambar 3-5. Rangkaian Oscilator Lokal dan Pembaginya.

3.2.2.2. Detektor Fasa

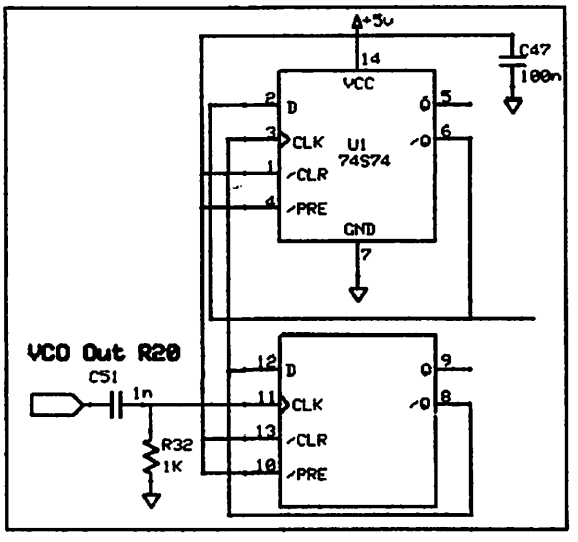
Rangkaian Detektor fasa menggunakan komponen TTL dari IC 74LS86 Quad 2-Input Exclusive OR, gerbang OR mempunyai sifat jika kedua inputnya berbeda maka outputnya *high* dan jika sama maka outputnya *low*, rangkaian menerima signal persegi dari oscillator local yang merupakan sumber frekuensi referensi dan dari N Devider yang merupakan signal dari VCO yang telah turunkan. Karena inputnya kontinyu output dari rangkaian akan diperoleh signal PWM (*Pulse witdh modulation*) dengan mengambil level DC yang digunakan untuk tegangan koreksi VCO, berikut adalah gambar rangkaian detector fasa:



Gambar 3-6. Rangkaian Detektor Fasa

3.2.2.3. Pembagi 4

Untuk menurunkan singal dari VCO diperlukan rangkaian pembagi yang dibentuk dari IC 74ALS74 D Flip Flop sebelum diberikan ke N Counter, untuk memperoleh pembagian sebesar 4 kali diperlukan dua Flip flop, adapun bentuk rangkaiannya seperti berikut :



Gambar 3-7. Rangkaian Pembagi 4

3.2.2.4. N Counter

Setelah oscillator carrier audio modulator dihasilkan, maka sebelum fasanya dibandingkan dibagian phase detector terlebih dahulu dibagi frekuensinya menyesuaikan besarnya frekuensi referensi phase detector agar phase output dihasilkan nilai *low* yang berarti tidak ada perbedaan fasa antara frekuensi set dan frekuensi referensi, ini berarti juga bahwa frekuensi modulator tetap terjaga. Untuk membagi frekuensi set diperlukan komponen 74LS193 BCD/ Decade Counter. Rumusnya adalah :

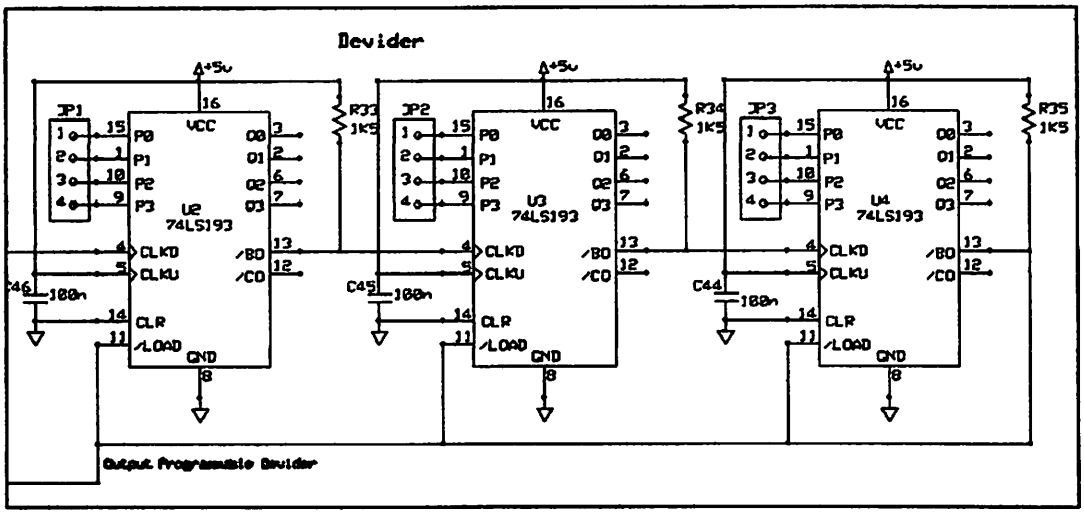
$$N_s = \frac{f_{modulator}}{f_{referensi}}$$

$$N_s = \frac{12.5.10^6}{6.25.10^3} = 2000$$

Sedangkan rumus untuk mendapatkan frekuensi set adalah :

$$f_s = \frac{f_{modulator}}{N_s} \qquad f_s = \frac{12.5.10^6}{2000} = 6.25 \text{ KHz}$$

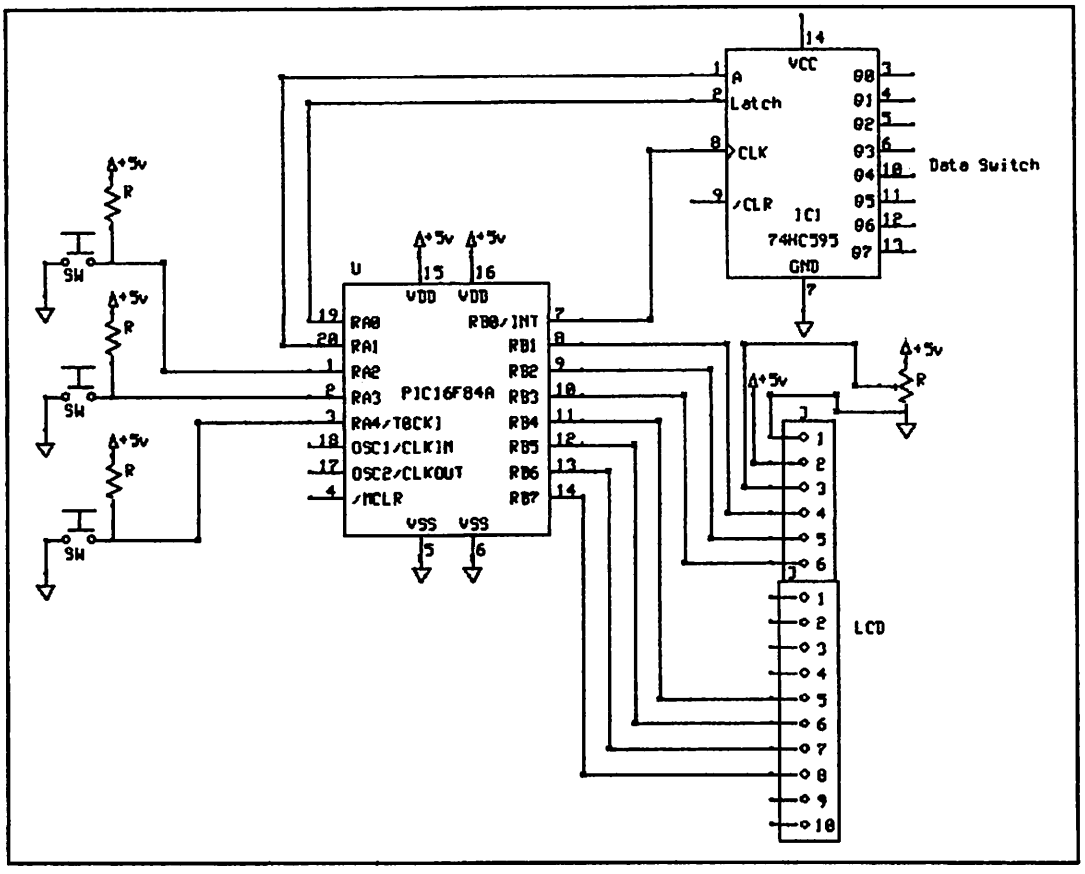
Berikut adalah gambar rangkaian Programmable Divider 74LS193 :



Gambar 3-8. Rangkaian N Devider

3.2.3. Unit Minimum Sistem

Bagian ini merupakan bagian pemroses pusat, komponen utamanya menggunakan mikrokontroler PIC16F84, sebagai inputan digunakan 3 tombol push button yang berfungsi untuk menaikan dan menurunkan nilai data biner untuk menset N counter, yang dikeluarkan melalui Pin RA1 secara serial ke IC 74HC595 shift dan latch register, data pencacahan yang dikirimkan oleh mikrokontroler kemudian dikirimkan ke LCD dam bentuk nilai frekuensinya. Adapun bentuk rangkaian keseluruhan minimum system PIC16F84 sebagai berikut :



Gambar 3-9. Rangkaian Minimum Sistem PIC16F84

3.3. Perancangan Software

Untuk mempermudah dalam pemrograman maka program dibuat dalam rutin – rutin tertentu, sehingga program utamanya dapat dibuat menjadi lebih sederhana. Terdapat tiga rutin untuk menangani proses input output data :

1. Rutin button.inc[1]

```
button    macro  port,pin,hilo,label
  local   pushed1          ; deklarasikan label untuk rutin lokal
  local   pushed2
  local   exit1
  local   exit2
  ifndef  debouncedelay            ; untuk mengenablekan debounce
#define   debouncedelay .10        ; menentukan besar delay
```

[1] http://www.mikroe.com/

```
        ; debounce
 endif
 if hilo  ==0                    ; pull up
 ifbit    port,pin,exit1         ; jika satu, tombol tidak ditekan
          pausems      debouncedelay      ; delay 10ms
debounce

pushed1
 ifnotbit port,pin,pushed1
 pausems debouncedelay  ; menunggu hingga dilepaskan dan
 goto label             ; melompat ke label yang ditentukan

exit1
 else                           ; pull down
 ifnotbit port,pin,exit2        ; jika nol, tombol tidak ditekan
 pausems debouncedelay          ; delay 10ms untuk debounce

pushed2
 ifbit port,pin,pushed2
 pausems debouncedelay                  ; menunggu hingga
tombol dilepaskan
 goto label
exit2
```

2. Rutin H595.inc[2]

Rutin ini manangani operasi pengiriman data dari mikro ke Shift register dan latch 74HC595, yang dikirimkan adalah data, clock, dan latch, adapun bentuk rutinya sebagai berikut :

```
hc595   macro  var,var1

 local   loop
 movlw  .8
 movwf  var1

loop     rlf      var,f

 btfss   STATUS,C
 bcf     data
 btfsc   STATUS,C
```

[2] http://www.mikroe.com/

```
bsf     data

bsf     Clock
nop
bcf     Clock

decfsz  var1,f
goto    loop

bsf     latch
nop
bcf     latch
endm
```

3. Rutin LCD.inc[3]

Rutin ini menangani kerja pengiriman dan pembacaan dari dan ke LCD, adapun program untuk rutin ini adalah :

```
CONSTANT    FUNCTSET8   = b'00110000'
CONSTANT    FUNCTSET4   = b'00100000'
CONSTANT    DDZERO      = b'10000000'

CONSTANT    LCD2L       = b'00101000'
CONSTANT    LCDCONT     = b'00001100'

CONSTANT    LCDSH       = b'00101000'

; Data Perintah menampilkan ke LCD

CONSTANT    LCDCLR      = b'00000001'
CONSTANT    LCDCH       = b'00000010'
CONSTANT    LCDCL       = b'00000100'
CONSTANT    LCDCR       = b'00000110'
CONSTANT    LCDSL       = b'00011000'

CONSTANT    LCDSR       = b'00011100'

CONSTANT    LCDL1       = b'10000000'
CONSTANT    LCDL2       = b'11000000'

;*****************************************************************
;
; Inisialisasi LCD
;*****************************************************************
;
```

[3] http://www.mikroe.com/

```
lcdinit   macro

          bank1
          clrf    LCDdsport
          bank0

          call    Delay1ms
          call    Delay1ms
          call    Delay1ms
          call    Delay1ms
          movlw   FUNCTSET8
          call    SendW
          call    Delay1ms
          call    Delay1ms
          movlw   DDZERO
          call    SendW

          movlw   FUNCTSET4
          call    SendW

;Perintah menginisialisasi LCD

          lcdcmd  LCD2L
          lcdcmd  LCDCONT
          lcdcmd  LCDSH
          lcdcmd  LCDCLR
          endm

;*******************************************************************************
;
; lcdcmd mengirim perintah ke LCD
; lcd clr berarti sama dengan lcdcmd 0x01
;*******************************************************************************
;

lcdcmd    macro   LCDcommand
          movlw   LCDcommand
          call    LCDcomd
          endm

lcdclr    macro
          movlw   LCDCLR
          call    LCDcomd
          endm

LCD_DDAdr      macro  DDRamAddress
          local   value = DDRamAddress | 0x80
                  movlw  value
                  call   LCDcomd
```

```
                endm

LCDcomd     clrf    LCDbuf
            goto    LCDwr

LCDdata clrf    LCDbuf
            bsf             LCDbuf,RS

LCDwr   movwf   LCDtemp
            andlw   b'11110000'
            iorwf   LCDbuf,w
            call    SendW
            swapf   LCDtemp,w
            andlw   b'11110000'
            iorwf   LCDbuf,w
            call    SendW
            return

SendW
            clrf    LCDdsport
            movwf   LCDdsport
            call    Delay1ms
            bsf             LCDdsport,EN
            bcf             LCDdsport,EN
            call    Delay1ms
            clrf    LCDdsport
            return

;*****************************************************************************
;
; macro lcdtext mampu mencetak 16 karakter yang dinyatakan
; macro parameter. parameter 1, select, pilih baris untuk
; ditampilkan
; jika  select = 0, text dicetak dari posisi cursor secara langsung
;*****************************************************************************
;

lcdtext     macro   select,text
            local   Message
            local   Start
            local   Exit
            local   i=0
            goto    Start
 dt text
 dt 0

Start
 if select ==1
 lcdcmd LCDL1
 else
```

```
 if select ==2
          lcdcmd LCDL2
          endif
 endif
 while i<16
 call     Message+1
 addlw    0
 bz       Exit
 call     LCDdata
i=i+1
 endw
Exit
 endm

;*****************************************************************************
;
; macro mencetak 1 byte ke LCD
;*****************************************************************************
;

lcdbyte  macro  arg0
         digbyte arg0

         movf   Dig1,w
         btfsc  STATUS,Z
         movlw  0x0f0
         addlw  0x030
         call   LCDdata

         movf   Dig2,w
         btfsc  STATUS,Z
         movlw  0x0f0
         addlw  0x030
         call   LCDdata

         movf   Dig3,w
         addlw  0x030
         call   LCDdata

         endm
Delay1ms:
         movlw  .100
         movwf  LOOPcnt

Delay10us:
         nop
         nop
         nop
         nop
         nop
```

```
        nop
        nop

        decfsz  LOOPcnt,f
        goto    Delay10us

        return

endif
endm
```

BAB IV

PENGUJIAN ALAT

4.1. Tujuan

Bab ini membahas tentang pengujian alat yang telah dibuat. Secara umum, pengujian ini bertujuan untuk mengetahui apakah piranti yang telah direalisasikan dapat bekerja sesuai dengan spesifikasi yang telah direncanakan. Pada tugas akhir ini pengujian dilakukan terhadap beberapa subsistem yang meliputi:

- Pengujian Pre –Emphasis
- Pengujian VCO
- Pengujian Detektor Phasa
- Pengujian Oscilator Lokal
- Pengujian PLL.

4.2. Pengujian Pre- Emphasis

4.2.1. Tujuan

Mengetahui level audio pada setiap range frekuensi audio

4.2.2. Peralatan yang digunakan

1. Osciloscope Hewlett Packard type HP54600A 100MHz 2 Channel
2. Function Generator GW Model GFG-80206
3. Rangkaian Pre- Emphasis
4. Kabel Probe

4.2.3. Prosedur Pengujian

BAB IV

PENGUJIAN ALAT

4.1. Tujuan

Bab ini membahas tentang pengujian alat yang telah dibuat. Secara umum, pengujian ini bertujuan untuk mengetahui apakah piranti yang telah direalisasikan dapat bekerja sesuai dengan spesifikasi yang telah ditentukan. Pada tugas akhir ini pengujian dilakukan terhadap beberapa subsistem yang meliputi:

- Pengujian Pre –Emphasis
- Pengujian VCO
- Pengujian Detektor Phasa
- Pengujian Oscillator Lokal
- Pengujian PLL.

4.2. Pengujian Pre- Emphasis

4.2.1. Tujuan

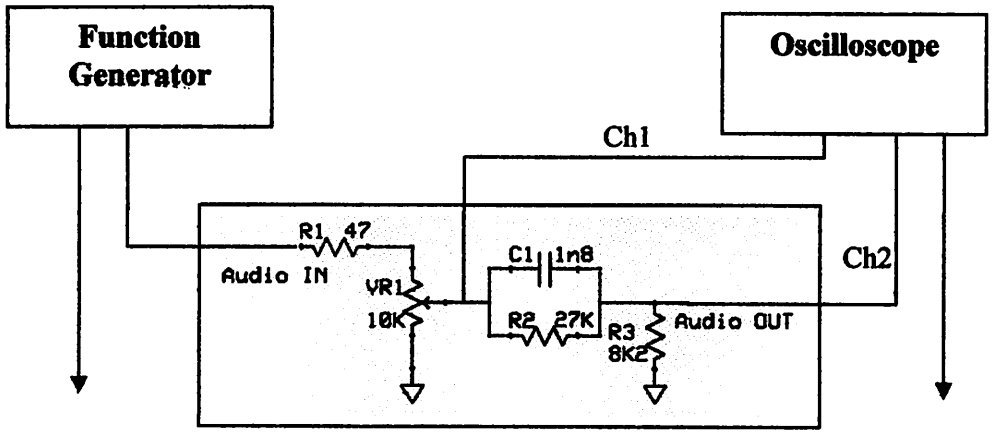
Mengetahui level audio pada setiap range frekuensi audio

4.2.2. Peralatan yang digunakan

1. Oscilloscope Hewlet Packard type HP5-600A 100MHz 2 Channel
2. Function Generator GW Model GFG-8020G
3. Rangkaian Pre- Emphasis
4. Kabel Probe

4.2.3. Prosedur Pengujian

1. Merangkai Peralatan yang digunakan sesuai Gambar 4-1 berikut:



Gambar 4-1. Pengukuran Rangkaian Pre- Emphasis

2. Mengaktifkan Function Generator pada Sinus $5V_{P-P}$.
3. Mengamati sinyal output pada osciloscope dan mencatat pada Tabel 4-1.
4. Mengulangi Langkah 2 dan 3 untuk nilai frekuensi yang berbeda.

4.2.4. Hasil Pengujian

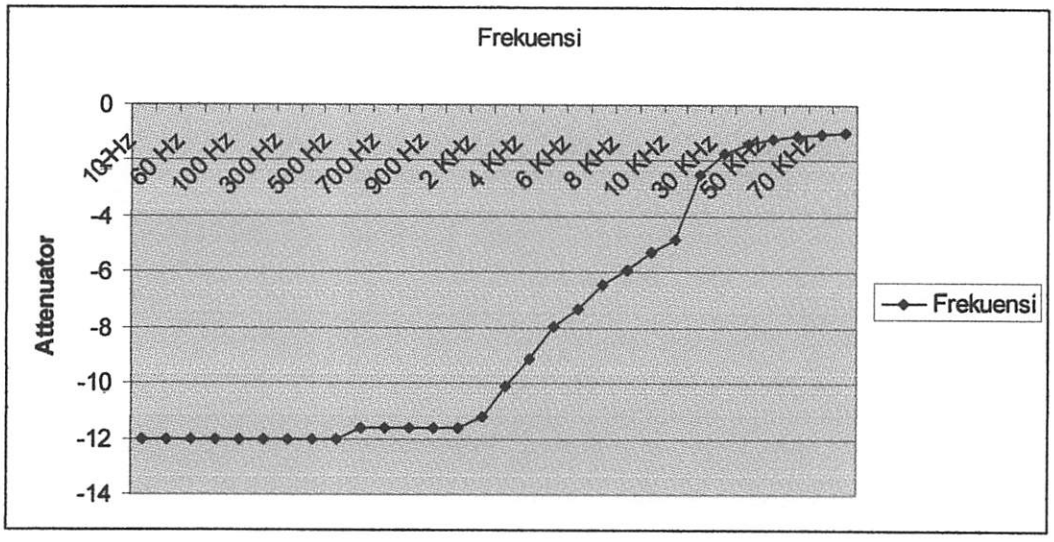
Tabel 4-1. Data Hasil Pengukuran Pre-Emphasis

No.	Frekuensi	V_{in} V_{P-P})	Pre - Emphasis	
			V_{Out} (V_{P-P})	dB
1	10 Hz	5 V	1.250	-12.041
2	30 Hz	5 V	1.250	-12.041
3	60 Hz	5 V	1.250	-12.041
4	90 Hz	5 V	1.250	-12.041
5	100 Hz	5 V	1.250	-12.041
6	200 Hz	5 V	1.250	-12.041
7	300 Hz	5 V	1.250	-12.041
8	400 Hz	5 V	1.250	-12.041
9	500 Hz	5 V	1.250	-12.041
10	600 Hz	5 V	1.312	-11.621
11	700 Hz	5 V	1.312	-11.621
12	800 Hz	5 V	1.312	-11.621
13	900 Hz	5 V	1.312	-11.621
14	1 KHz	5 V	1.312	-11.621
15	2 KHz	5 V	1.375	-11.213

16	3 KHz	5 V	1.562	-10.106
17	4 KHz	5 V	1.750	-9.119
18	5 KHz	5 V	2	-7.959
19	6 KHz	5 V	2.156	-7.306
20	7 KHz	5 V	2.375	-6.466
21	8 KHz	5 V	2.531	-5.914
22	9 KHz	5 V	2.719	-5.291
23	10 KHz	5 V	2.875	-4.807
24	20 KHz	5 V	3.750	-2.499
25	30 KHz	5 V	4.094	-1.736
26	40 KHz	5 V	4.250	-1.412
27	50 KHz	5 V	4.344	-1.222
28	60 KHz	5 V	4.406	-1.099
29	70 KHz	5 V	4.437	-1.038
30	80 KHz	5 V	4.469	-0.975

4.2.5. Kesimpulan

1. Grafik Respon Frekuensi terhadap Attenuator dalam dB :



Grafik 4-1. Respon Frekuensi terhadap Attenuator.

2. Dari grafik diperoleh besar slope sebesar 6.33 dB / Octave

4.3. Pengujian VCO

4.3.1. Tujuan

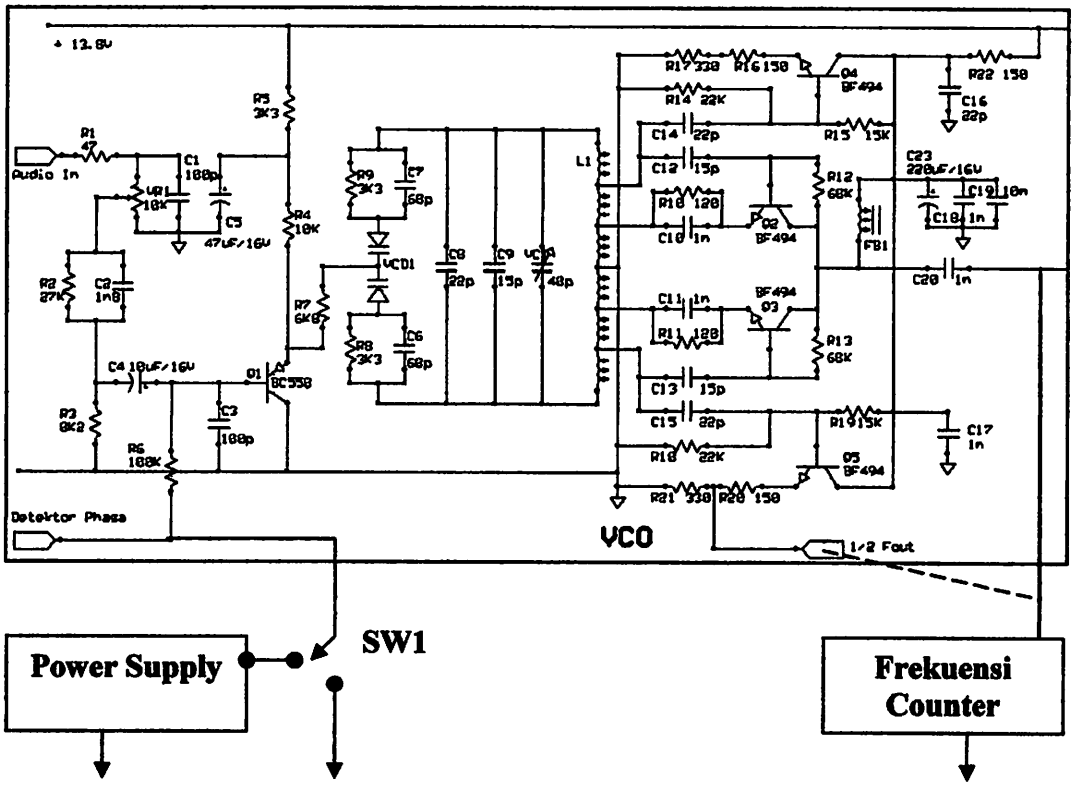
Untuk mengetahui frekuensi dasar, range frekuensi, respon frekuensi

4.3.2. Peralatan Yang Digunakan :

1. Osciloscope Hewlett Packard type HP54600A 100MHz 2 Channel
2. Frequency Counter GW model GFC-8131
3. Power Supply ED2900
4. Rangkaian VCO
5. Kabel, Probe.

4.3.3. Prosedur Pengujian

1. Merangkai peralatan yang digunakan sesuai Gambar 4-2 berikut :



Gambar 4-2. Pengukuran VCO

4.3. Pengujian VCO

4.3.1. Tujuan

Untuk mengetahui frekuensi dasar, range frekuensi, respon frekuensi

4.3.2. Peralatan Yang Digunakan :

1. Oscilloscope Hewlett Packard type HP54600A 100MHz 2 Channel
2. Frequency Counter GW model GFC-8131
3. Power Supply ED2900
4. Rangkaian VCO
5. Kabel Probe.

4.3.3. Prosedur Pengujian

1. Merangkai peralatan yang digunakan sesuai Gambar 4-2 berikut :

Gambar 4-2. Pengukuran VCO

2. Mengaktifkan frekuensi counter dan VCO, switch ke ground.
3. Mengukur frekuensi pada R20 dan C20, serta mencatat hasilnya pada tabel 4-2.
4. Memindahkan Switch ke Power Supply ED-2900.
5. Menaikan Power Supply sebesar 0,1Volt tiap stepnya
6. Mengukur Frekuensi pada R20 dan C20, mencatat nilainya pada tabel 4-2.

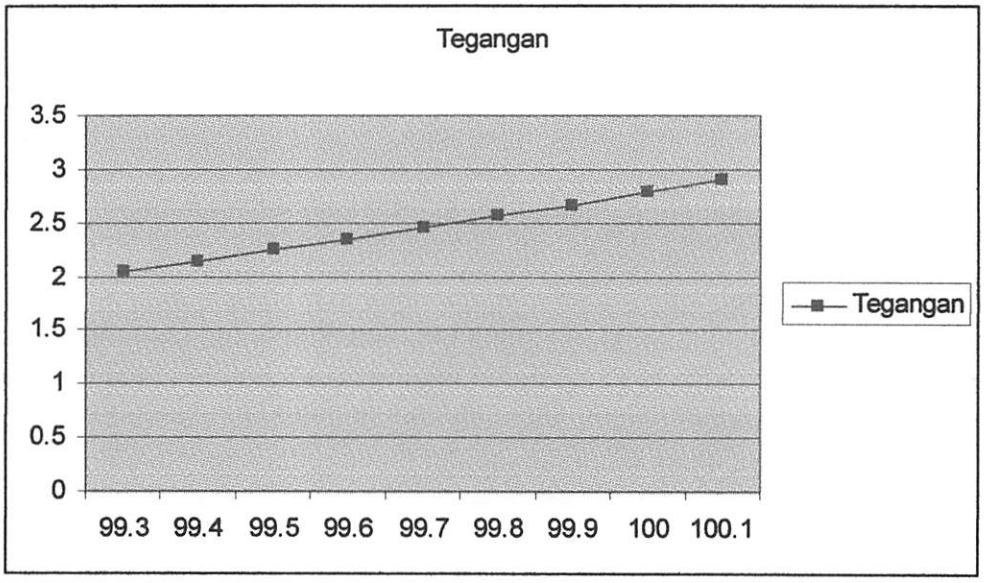
4.3.4. Hasil Pengujian

Tabel 4-2. Data Pengukuran VCO

No.	SW-Ground		SW ke Power Supply		
	F_{R20}	F_{C20}	V_{R6}(volt)	F_{R20}(MHz)	F_{C20}(MHz)
1	50MHz	100MHz	2.05	99.3	49.65
2			2.15	99.4	49.7
3			2.25	99.5	49.75
4			2.35	99.6	49.8
5			2.46	99.7	49.85
6			2.56	99.8	49.9
7			2.67	99.9	49.95
8			2.79	100.0	50
9			2.91	100.1	50.05

4.3.5. Kesimpulan

1. Saat dioda varactor tidak terbias, VCO sudah mempunyai nilai frekuensi osilasi sebesar 100 MHz, hasil penjumlahan Frekuensi per oscilator 50MHz.
2. Grafik respon frekuensi output terhadap tegangan bias dc:



Grafik 4-2. Respon Frekuensi Terhadap Tegangan

4.4. Pengujian Detektor Phasa

4.4.1. Tujuan

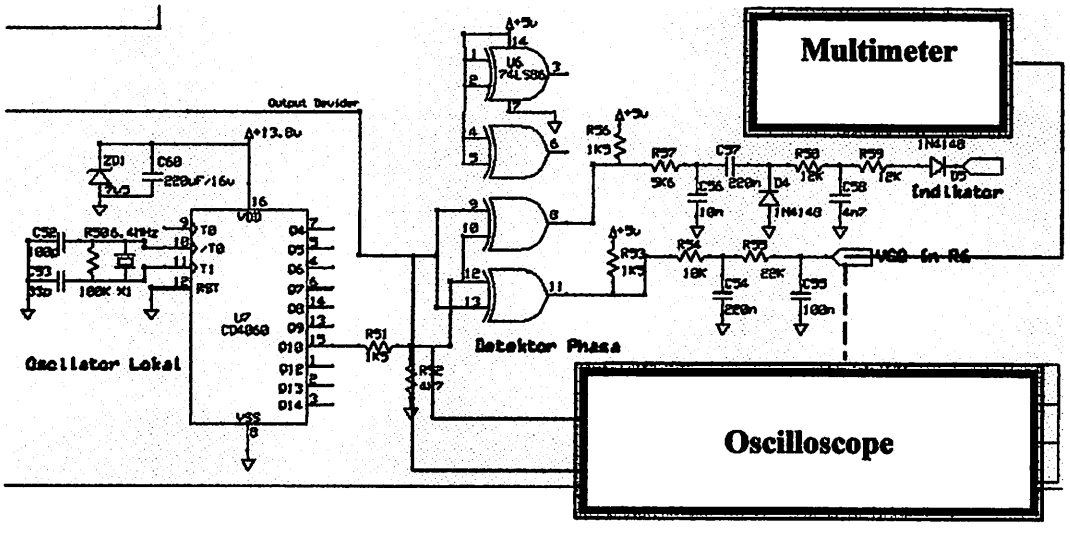
Mengetahui beda phasa dan tegangan outputnya.

4.4.2. Peralatan yang digunakan

1. Oscilloscope Hewlett Packard type HP54600A 100MHz 2 Channel
2. Multimeter Digital DT9202
3. Rangkaian Detektor Phasa
4. Power Supply
5. Kabel

4.4.3. Prosedure Pengujian

1. Merangkai peralatan yang digunakan sesuai Gambar 4-2 berikut :



Gambar 4-3. Pengukuran Rangkaian Detektor Phasa

2. Mengamati bentuk gelombang pada Osciloscope dan mencatat nilai *Duty Cycle* saat kondisi terkunci pada tabel 4-3.

4.4. Pengujian Detektor Phasa

4.4.1. Tujuan

Mengetahui beda phasa dan tegangan output-nya.

4.4.2. Peralatan yang digunakan

1. Oscilloscope Hewlett Packard type HP54600A 100MHz 2 Channel
2. Multimeter Digital D 17202
3. Rangkaian Deteksi Phasa
4. Power Supply
5. Kabel

4.4.3. Prosedure Pengujian

1. Merangkai peralatan yang digunakan sesuai Gambar 4-2 berikut :

Gambar 4-2. Pengukuran Rangkaian Deteksi Phasa

2. Mengamati bentuk gelombang pada Oscilloscope dan mencatat nilai Duty Cycle saat kondisi terkunci pada tabel 4-2.

4.4.4. Hasil Pengujian

Tabel 4-3. Data Pengukuran Detektor Phasa

Frekuensi (MHz)	***Duty Cycle* (%)**	**Tegangan dc (Volt)**
99.5	39.1	2.25
99.6	40.6	2.35
99.7	40.7	2.46
99.8	43.0	2.56
99.9	45.4	2.67
100	47.1	2.79
100.1	47.7	2.91
100.2	50.1	3.02

4.4.5. Kesimpulan

1. untuk manaikan frekuensi maka diperlukan level tegangan DC yang naik pula, level tegangan ini diperoleh dari prosentase *dutycycle* yang semakin naik.
2. untuk kenaikan frekuensi sebesar 100KHz diperlukan kenaikan tegangan 0,1 volt

4.5. Pengujian Oscilator Lokal

4.5.1. Tujuan

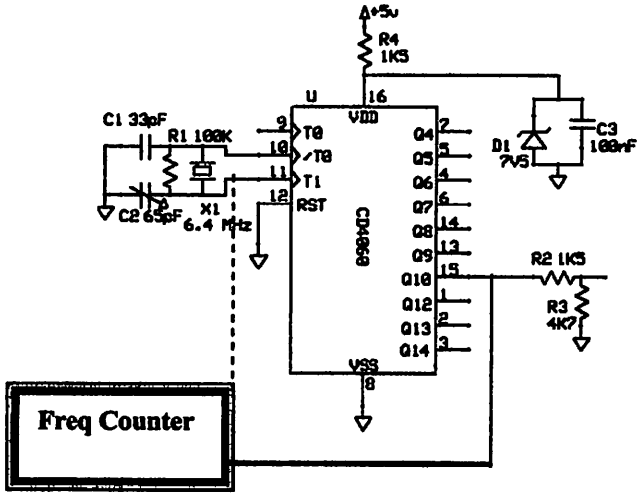
Mengetahui besar frekuensi dari oscilator lokal yang yang dijadikan frekuensi referensi.

4.5.2. Peralatan yang digunakan

1. Frequency Counter GW model GFC-8131
2. Rangkaian Oscilator Lokal
3. Power Supply
4. Kabel

4.5.3. Prosedur Pengujian

1. Merangkai peralatan yang digunakan seperti Gambar 4-4.



Gambar 4-4. Pengukuran Rangkaian Frekuensi Referensi

2. Mengaktifkan peralatan dan memberikan tegangan ke rangkaian oscilator lokal.
3. Mengukur Frekuensi pada Kristal dan frekuensi output, kemudian mencatat pada tabel 4-4.

4.5. Pengujian Oscilator Lokal

4.5.1. Tujuan

Mengetahui besar frekuensi dari oscilator lokal yang yang dijadikan frekuensi referensi.

4.5.2. Peralatan yang digunakan

1. Frequency Counter GW model GFC-8131
2. Rangkaian Oscilator Lokal
3. Power Supply
4. Kabel

4.5.3. Prosedur Pengujian

1. Menangkai peralatan yang digunakan seperti Gambar 4-4.

Gambar 4-4. Pengukuran Rangkaian Frekuensi Referensi

2. Mengaktifkan peralatan dan memberikan tegangan ke rangkaian oscilator lokal.
3. Mengukur Frekuensi pada Kristal dan frekuensi output. kemudian menerat pada tabel 4-4.

4.5.4. Hasil Pengujian

Tabel 4-4. Data Pengukuran Oscilator Lokal

Frekuensi Kristal (MHz)	Frekuensi Referensi (KHz)
6.4	6.250

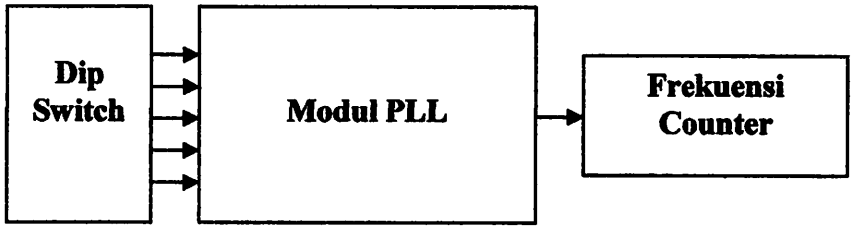
4.6. Pengukuran PLL

4.6.1. Tujuan

Mengetahui data biner terhadap frekuensi output.

4.6.2. Prosedur Pengujian

1. Merangkai peralatan yang digunakan seperti Gambar 4-5.



Gambar 4-5. Pengukuran Rangkaian Frekuensi Referensi

2. Mengaktifkan sistem keseluruhan dan memberikan data pencacahan seperti tabel 4-5.
3. Mengamati Frekuensi output dari sistem dan mencatat pada tabel 4-5.

4.6.3. Hasil Pengujian

Tabel 4-5. Data Pengujian PLL

Dip Switch												F_{out}
D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	(MHz)
ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	87.5
ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	87.6
ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	ON	87.7
ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	87.8
ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	87.9
ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	88
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	ON	88.1
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	88.2
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	ON	88.3
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	88.4
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	88.5
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	88.6
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	88.7
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	88.8
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON	88.9
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	89
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	89.1
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	89.2
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	89.3
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	89.4
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	89.5
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	89.6
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	89.7
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	OFF	89.8
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	ON	89.9
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF	90
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON	ON	90.1
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON	OFF	90.2
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	ON	90.3
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	90.4
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	ON	ON	ON	90.5
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	ON	ON	OFF	90.6
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF	ON	90.7
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF	OFF	90.8
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON	90.9
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	ON	OFF	91
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	91.1
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	91.2
ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	ON	ON	91.3

4.6.3. Hasil Pengujian

Tabel 4-5. Data Pengujian PLL

Dip Switch												F_{out}
D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	(MHz)
ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	87.5
ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	87.6
ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	ON	87.7
ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	87.8
ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	87.9
ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	88
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	ON	88.1
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	88.2
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	ON	88.3
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	88.4
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	88.5
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	88.6
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	88.7
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	88.8
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON	88.9
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	89
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	89.1
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	89.2
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	89.3
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	89.4
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	89.5
ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	89.6
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	89.7
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	OFF	89.8
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	ON	89.9
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF	90
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON	ON	90.1
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON	OFF	90.2
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	ON	90.3
ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	90.4
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	ON	ON	ON	90.5
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	ON	ON	OFF	90.6
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF	ON	90.7
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF	OFF	90.8
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON	90.9
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	ON	OFF	91
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	91.1
ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	91.2
ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	ON	ON	91.3

ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	ON	OFF	91.4
ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	OFF	ON	91.5
ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	91.6
ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	ON	ON	91.7
ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF	91.8
ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	ON	91.9
ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	92
ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	ON	92.1
ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	92.2
ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	92.3
ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	92.4
ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	ON	92.5
ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	92.6
ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	92.7
ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	92.8
ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	ON	92.9
ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	OFF	93
ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	ON	93.1
ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	93.2
ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	ON	ON	93.3
ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	ON	OFF	93.4
ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	ON	93.5
ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	93.6
ON	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	ON	ON	93.7
ON	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	ON	OFF	93.8
ON	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	ON	93.9
ON	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	94
ON	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON	94.1
ON	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	94.2
ON	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	94.3
ON	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	94.4
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	ON	94.5
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	OFF	94.6
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON	94.7
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	94.8
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	ON	94.9
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	95
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	95.1
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	95.2
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	95.3
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	95.4
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	95.5
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	95.6
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	95.7
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	95.8
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	95.9
ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	96

91.4	OFF	ON	ON	ON	OFF	ON	ON	OFF	OFF	OFF	ON	ON
91.5	ON	OFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF	ON	ON
91.6	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF	ON	ON
91.7	ON	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	ON	ON
91.8	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	ON	ON
91.9	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON
92	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON
92.1	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
92.2	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
92.3	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON
92.4	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON
92.5	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
92.6	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON
92.7	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON
92.8	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON
92.9	ON	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON
93	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON
93.1	ON	OFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON
93.2	OFF	OFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON
93.3	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON
93.4	OFF	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON
93.5	ON	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON
93.6	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON
93.7	ON	ON	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON
93.8	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON
93.9	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON
94	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON
94.1	ON	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON
94.2	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON
94.3	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON
94.4	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON
94.5	ON	ON	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	ON
94.6	OFF	ON	ON	ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON
94.7	ON	OFF	ON	ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON
94.8	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON
94.9	ON	ON	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON
95	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON
95.1	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON
95.2	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON
95.3	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON
95.4	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON
95.5	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON
95.6	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON
95.7	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	ON
95.8	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	ON
95.9	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	ON
96	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	ON

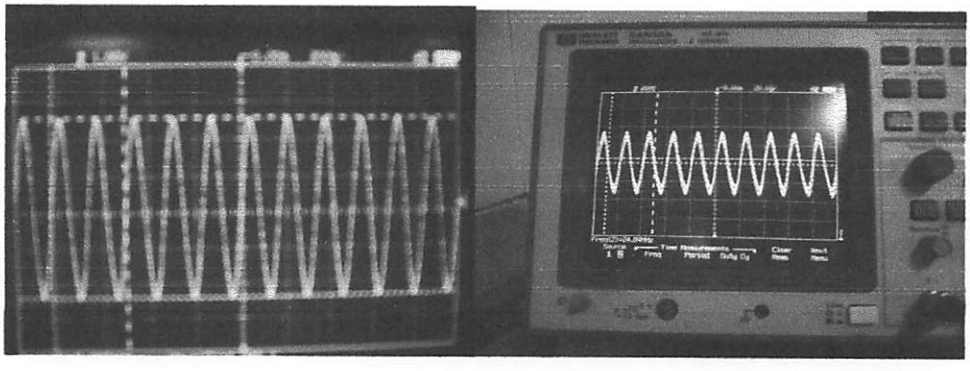
ON	ON	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	96.1
ON	ON	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	96.2
ON	ON	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON	96.3
ON	ON	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	96.4
ON	ON	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	ON	ON	96.5
ON	ON	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF	96.6
ON	ON	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	ON	96.7
ON	ON	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	96.8
ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	ON	ON	96.9
ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	ON	OFF	97
ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	ON	97.1
ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	97.2
ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	97.3
ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	97.4
ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	97.5
ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	97.6
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	97.7
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	97.8
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	ON	97.9
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	98
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	ON	98.1
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	98.2
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	98.3
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	98.4
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	98.5
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	98.6
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	98.7
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	98.8
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	98.9
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	99
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	99.1
ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	99.2
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	99.3
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	99.4
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	ON	99.5
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	99.6
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	ON	99.7
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	99.8
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	99.9
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	100
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	100.1
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	100.2
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	100.3
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	100.4
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	100.5
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	100.6
ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	100.7

96.1	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
96.2	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
96.3	ON	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
96.4	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
96.5	ON	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
96.6	OFF	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
96.7	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON
96.8	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
96.9	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
97	OFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
97.1	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON
97.2	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON
97.3	ON	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
97.4	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
97.5	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
97.6	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
97.7	ON	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON
97.8	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
97.9	ON	OFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON
98	OFF	OFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON
98.1	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON
98.2	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON
98.3	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON
98.4	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
98.5	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
98.6	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
98.7	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON
98.8	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON
98.9	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
99	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
99.1	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
99.2	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
99.3	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
99.4	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
99.5	ON	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
99.6	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
99.7	ON	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
99.8	OFF	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
99.9	ON	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
100	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON
100.1	ON	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON
100.2	OFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON
100.3	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON
100.4	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON
100.5	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON
100.6	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON
100.7	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON

ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	100.8
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	100.9
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	101
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	101.1
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	101.2
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	101.3
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	101.4
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	101.5
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	101.6
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	101.7
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	101.8
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	101.9
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	102
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	102.1
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	102.2
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	102.3
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	102.4
ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	102.5
ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	102.6
ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON	OFF	ON	102.7
ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	102.8
ON	OFF	ON	ON	ON	ON	ON	ON	ON	OFF	ON	ON	102.9
ON	OFF	ON	ON	ON	ON	ON	ON	ON	OFF	ON	OFF	103
ON	OFF	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	103.1
ON	OFF	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	103.2
ON	OFF	ON	ON	ON	ON	ON	ON	OFF	ON	ON	ON	103.3
ON	OFF	ON	ON	ON	ON	ON	ON	OFF	ON	ON	OFF	103.4
ON	OFF	ON	ON	ON	ON	ON	ON	OFF	ON	OFF	ON	103.5
ON	OFF	ON	ON	ON	ON	ON	ON	OFF	ON	OFF	OFF	103.6
ON	OFF	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	ON	103.7
ON	OFF	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	OFF	103.8
ON	OFF	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	ON	103.9
ON	OFF	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	104
ON	OFF	ON	ON	ON	ON	ON	OFF	ON	ON	ON	ON	104.1
ON	OFF	ON	ON	ON	ON	ON	OFF	ON	ON	ON	OFF	104.2
ON	OFF	ON	ON	ON	ON	ON	OFF	ON	ON	OFF	ON	104.3
ON	OFF	ON	ON	ON	ON	ON	OFF	ON	ON	OFF	OFF	104.4
ON	OFF	ON	ON	ON	ON	ON	OFF	ON	OFF	ON	ON	104.5
ON	OFF	ON	ON	ON	ON	ON	OFF	ON	OFF	ON	OFF	104.6
ON	OFF	ON	ON	ON	ON	ON	OFF	ON	OFF	OFF	ON	104.7
ON	OFF	ON	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	104.8
ON	OFF	ON	ON	ON	ON	ON	OFF	OFF	ON	ON	ON	104.9
ON	OFF	ON	ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	105
ON	OFF	ON	ON	ON	ON	ON	OFF	OFF	ON	OFF	ON	105.1
ON	OFF	ON	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	105.2
ON	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	ON	ON	105.3
ON	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	ON	OFF	105.4

100.8	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
100.9	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
101	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
101.1	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
101.2	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
101.3	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
101.4	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
101.5	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
101.6	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
101.7	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
101.8	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
101.9	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
102	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
102.1	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
102.2	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
102.3	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
102.4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
102.5	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	ON
102.6	OFF	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	ON
102.7	ON	OFF	ON	ON	ON	ON	ON	ON	ON	ON	OFF	ON
102.8	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	ON	OFF	ON
102.9	ON	ON	OFF	ON	ON	ON	ON	ON	ON	ON	OFF	ON
103	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	ON	OFF	ON
103.1	ON	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	OFF	ON
103.2	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	OFF	ON
103.3	ON	ON	ON	ON	OFF	ON	ON	ON	ON	ON	OFF	ON
103.4	OFF	ON	ON	ON	OFF	ON	ON	ON	ON	ON	OFF	ON
103.5	ON	OFF	OFF	ON	OFF	ON	ON	ON	ON	ON	OFF	ON
103.6	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	ON	OFF	ON
103.7	ON	ON	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	ON
103.8	OFF	ON	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	ON
103.9	ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	ON
104	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	ON
104.1	ON	ON	ON	ON	ON	OFF	ON	ON	ON	ON	OFF	ON
104.2	OFF	ON	ON	ON	ON	OFF	ON	ON	ON	ON	OFF	ON
104.3	ON	OFF	ON	ON	ON	OFF	ON	ON	ON	ON	OFF	ON
104.4	OFF	OFF	ON	ON	ON	OFF	ON	ON	ON	ON	OFF	ON
104.5	ON	ON	ON	OFF	ON	OFF	ON	ON	ON	ON	OFF	ON
104.6	OFF	ON	ON	OFF	ON	OFF	ON	ON	ON	ON	OFF	ON
104.7	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	OFF	ON
104.8	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	OFF	ON
104.9	ON	ON	ON	ON	OFF	OFF	ON	ON	ON	ON	OFF	ON
105	OFF	ON	ON	ON	OFF	OFF	ON	ON	ON	ON	OFF	ON
105.1	ON	OFF	ON	ON	OFF	OFF	ON	ON	ON	ON	OFF	ON
105.2	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON
105.3	ON	ON	OFF	ON	OFF	OFF	ON	ON	ON	ON	OFF	ON
105.4	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON

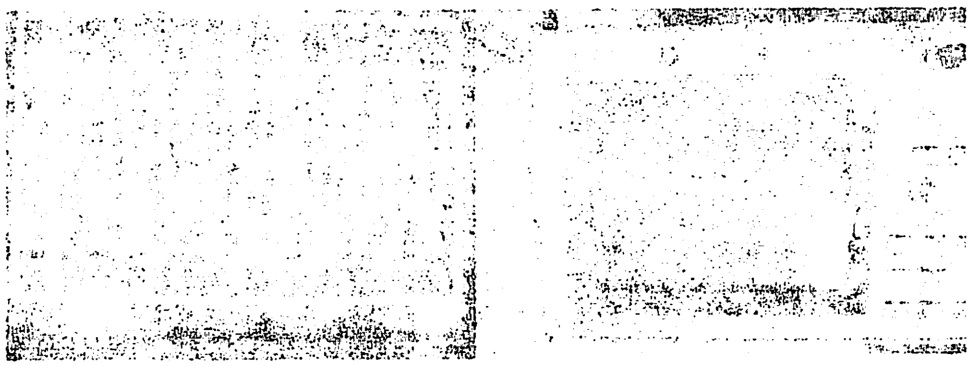
ON	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	105.5
ON	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	105.6
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	ON	ON	ON	105.7
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	ON	ON	OFF	105.8
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	ON	OFF	ON	105.9
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	ON	OFF	OFF	106
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	OFF	ON	ON	106.1
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	OFF	ON	OFF	106.2
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	OFF	OFF	ON	106.3
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	OFF	OFF	OFF	106.4
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	ON	ON	ON	106.5
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	ON	ON	OFF	106.6
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	ON	OFF	ON	106.7
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	ON	OFF	OFF	106.8
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	ON	ON	106.9
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	ON	OFF	107
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	ON	107.1
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	107.2
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	ON	ON	107.3
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	ON	OFF	107.4
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	ON	107.5
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	107.6
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	OFF	ON	ON	107.7
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	OFF	ON	OFF	107.8
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	ON	107.9
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	108



(a) **(b)**

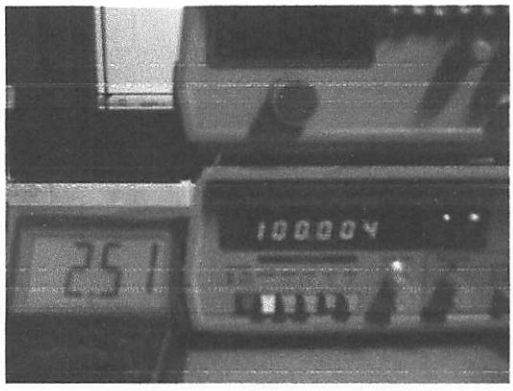
Gambar 4-6. Hasil Pengujian Pre Emphasis, (a) Sinyal Input, (b) Sinyal Output

ON	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	105.5
ON	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	105.6
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	ON	ON	ON	105.7
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	ON	ON	OFF	105.8
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	ON	OFF	ON	105.9
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	ON	OFF	OFF	106
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	OFF	ON	ON	106.1
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	OFF	ON	OFF	106.2
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	OFF	OFF	ON	106.3
ON	OFF	ON	ON	ON	ON	OFF	ON	ON	OFF	OFF	OFF	106.4
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	ON	ON	ON	106.5
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	ON	ON	OFF	106.6
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	ON	OFF	ON	106.7
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	ON	OFF	OFF	106.8
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	ON	ON	106.9
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	ON	OFF	107
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	ON	107.1
ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	107.2
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	ON	ON	107.3
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	ON	OFF	107.4
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	ON	107.5
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	107.6
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	OFF	ON	ON	107.7
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	OFF	ON	OFF	107.8
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	ON	107.9
ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	108

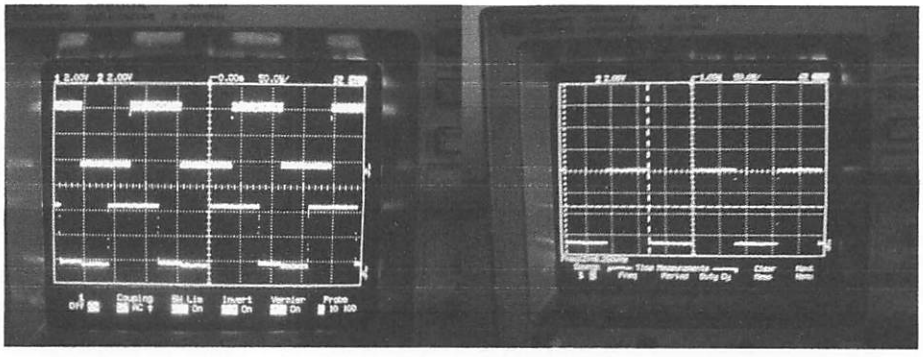


(a) (b)

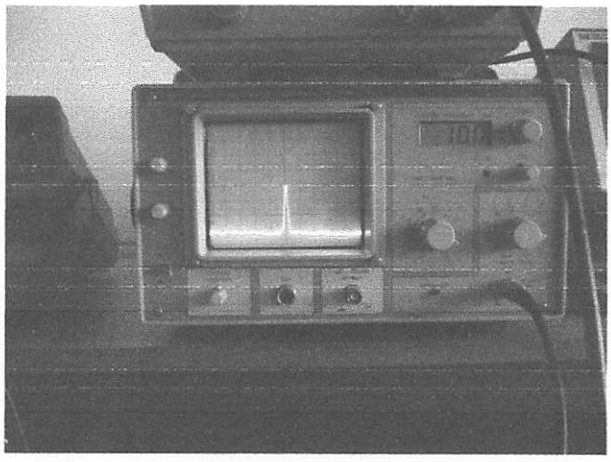
Gambar 4-6. Hasil Pengujian Pre Emphasis (a) Sinyal Input (b) Sinyal Output



Gambar 4-7. Hasil Pengujian VCO



Gambar 4-8. Hasil Pengujian Detektor Phasa



Gambar 4-10. Hasil Pengujian PLL

BAB V

PENUTUP

5.1 Kesimpulan

Berdasarkan hasil pengujian dan analisa alat yang telah dibuat maka dapat disimpulkan :

1. Spesifikasi alat :
   - Respon frekuensi audio :10 Hz – 15 KHz / 6 dB/octave
   - Range frekuensi : 87,5 – 108 MHz
   - Frekuensi step : 100 KHz /step
   - Daya : 0,9 Watt
2. Hasil Pengujian :
   - Respon Pre- Emphasis terhadap frekuensi audio 10 Hz – 15 KHz dengan slope pada frekuensi cut- off 6,33 dB/ octave.
   - Respon frekuensi terhadap tegangan input dari VCO 0,1 Volt untuk tiap kenaikan frekuensi sebesar 100KHz.
   - Tegangan output detector phasa sebesar 0,1 Volt tiap 100KHz step.
   - Frekuensi referensi sebesar 6,25 KHz dari kristal 6,4MHz.
   - Frekuensi output 87,5 MHz dengan data biner 001101101010, dan frekuensi 108 MHz dengan data biner 010000110111.
3. Kelebihan Alat :
   - PLL menggunakan VCO dengan antiphase sehingga dengan komponen aktif frekuensi rendah dapat dihasilkan frekuensi tinggi .

- Sinyal umpan balik yang diambil dari satu sisi oscillator maka tidak diperlukan *Prescaller* yang mahal.
- Terdapat isolasi antara frekuensi output dengan frekuensi umpan balik.
-

5.2 Saran

Dalam pembuatan masih terdapat beberapa kekurangan sehingga untuk mencapai hasil yang lebih baik dan pengembangan lebih lanjut maka dapat diberikan saran – saran sebagai berikut :

1. dalam proses pembuatan PCB dipergunakan double layer untuk menghindari kapasitansi liar.
2. LPF menggunakan jenis aktif filter sehingga range tegangannya lebih lebar dan tidak perlu proses tuning.
3. Dapat dipergunakan metode *Dual Modullus Prescaller* sehingga step frekuensinya sama dengan frekuensi referensi.
4. Perlu ditambahkan Dioda Varactor pada filter output sehingga daya output flat pada semua range frekuensi.

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5. http://www.mikroe.com
6. http://educypedia.be/electronics

LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

FORMULIR BIMBINGAN SKRIPSI

NAMA : NANANG RONI WIBOWO
NIM : 02.17.062
Masa Bimbingan : 09 Januari – 09 Juli 2007
Judul Skripsi : Perencanaan dan Pembuatan PLL berbasis PIC16F84 dengan penampil LCD dan Aplikasinya sebagai Exciter FM.

No.	Tanggal	Uraian	Paraf Pembimbing
1.	4/12 06.	Konsultasi judul skripsi.	
2.	29/01 07.	Konsep ttg PLL Synthesizer menggunakan PIC.	
3.	5/02 07.	Realisasi VCO dgn parameter2 yg. diukur sbg. objek pengukuran.	
4.	21/02 07.	Bab IV, ukur fasa & output VCO yg. dpt. mengenai Freq.	
5.	27/2 07.	Bab IV, ukur perubahan freq. thd. perubahan fasa.	
6.	29/2 07.	Bab V, simpulkan freq. ref. thd pembagi dr. µc (PIC)	
7.	5/3 07.	Bab III, lengkapi perancangan filter output VCO	
8.	8/3 07.	Bab II, cantumkan berbagai jenis VCO utk PLL	
9.	13/3 07.	Bab I, tinjau lagi batasan masalah & permasalahan.	
10.	14/3 07.	Cap. Skripsi Selesai, siap ujian.	

Malang, 15/3 07
Dosen Pembimbing I

Ir. Sidik Noertjahjono, MT
NIP. 1028700167

Form S- 4A

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

FORMULIR BIMBINGAN SKRIPSI

NAMA : NANANG RONI WIBOWO
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No.	Tanggal	Uraian	Paraf Pembimbing
1.		Bab I + Bab II	
2.		Bab III	
3.		Bab IV	
4.		Bab V	
5.		Lengkapi	
9.			
10.			

Malang, ...
Dosen Pembimbing II

Ir. F.Yudi Limpraptono, MT
NIP. 1039500274

Form S- 4A

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
Jl. Karanglo KM. 2 Malang

FORMULIR PERBAIKAN SKRIPSI

Dalam pelaksanaan Ujian Skripsi Jenjang Strata Satu (S-1) Jurusan Teknik Elektro Konsentrasi Teknik Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

Nama	: Nanang Roni Wibowo
NIM	: 02.17.062
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Masa Bimbingan	: 09 Januari 2007 – 09 Juli 2007
Judul Skripsi	: Perencanaan dan pembuatan PLL berbasis PIC16F84 dengan penampil LCD dan aplikasinya sebagai exciter FM.

Tanggal	Uraian	Paraf
17 Maret 2007	❖ Lokalisasi masing- masing bagian di skema rangkaian berdasarkan blok diagram	
	❖ Tentukan bagian exciter di blok diagram.	
	❖ Buat kesimpulan dalam format : 1. Spesifikasi alat yang dibuat. 2. Hasil pengujian. 3. Kelebihan alat.	
	❖ Analisa kebutuhan arus terhadap frekuensi dan daya output yang dikeluarkan alat. Tentukan kondisi optimum spesifikasi alat.	

Dosen Penguji

DR. Cahyo Chrysdian, MSc
NIP. 103 0400 412

Mengetahui,

Dosen Pembimbing I	Dosen Pembimbing II
Ir. Sidik Noertjahjono, MT	Ir. F. Yudi Limpraptono, MT
NIP. 102 8700 167	NIP. Y. 103 9500 274

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : NANANG RONI WIBOWO
N I M : 0217062 .
Perbaikan meliputi :

(1) Keterangan utama kaitan di ~~blok diagram~~ skema rangkaian berdasarkan blok diagram.

(2) Tentukan bagian exciter di blok diagram. ~~[illegible]~~

(3) Buat kesimpulan dlm format.
  (1) spec alat yg dibuat
  (2) hasil pengujian
  (3) kelebihan alat

(4) Analisa kestabilan arus thd freq & daya output yg dikeluarkan alat.
Tentukan kondisi optimum spec operasi alat.

Malang, 12/3 - 2007

(Dr. Cahyo Crysdian, MSc.)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
Jl. Karanglo KM. 2 Malang

FORMULIR PERBAIKAN SKRIPSI

Dalam pelaksanaan Ujian Skripsi Jenjang Strata Satu (S-1) Jurusan Teknik Elektro Konsentrasi Teknik Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

Nama	: Nanang Roni Wibowo
NIM	: 02.17.062
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Masa Bimbingan	: 09 Januari 2007 – 09 Juli 2007
Judul Skripsi	: Perencanaan dan pembuatan PLL berbasis PIC16F84 dengan penampil LCD dan aplikasinya sebagai exciter FM.

Tanggal	Uraian	Paraf
17 Maret 2007	❖ Sesuaikan alat dengan isi laporan	

Dosen Penguji

I Komang Somawirata, ST, MT
NIP. Y. 103 0100 0361

Mengetahui,

Dosen Pembimbing I

Ir. Sidik Noertjahjono, MT
NIP. 102 8700 167

Dosen Pembimbing II

Ir. F. Yudi Limpraptono, MT
NIP. Y. 103 9500 274

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

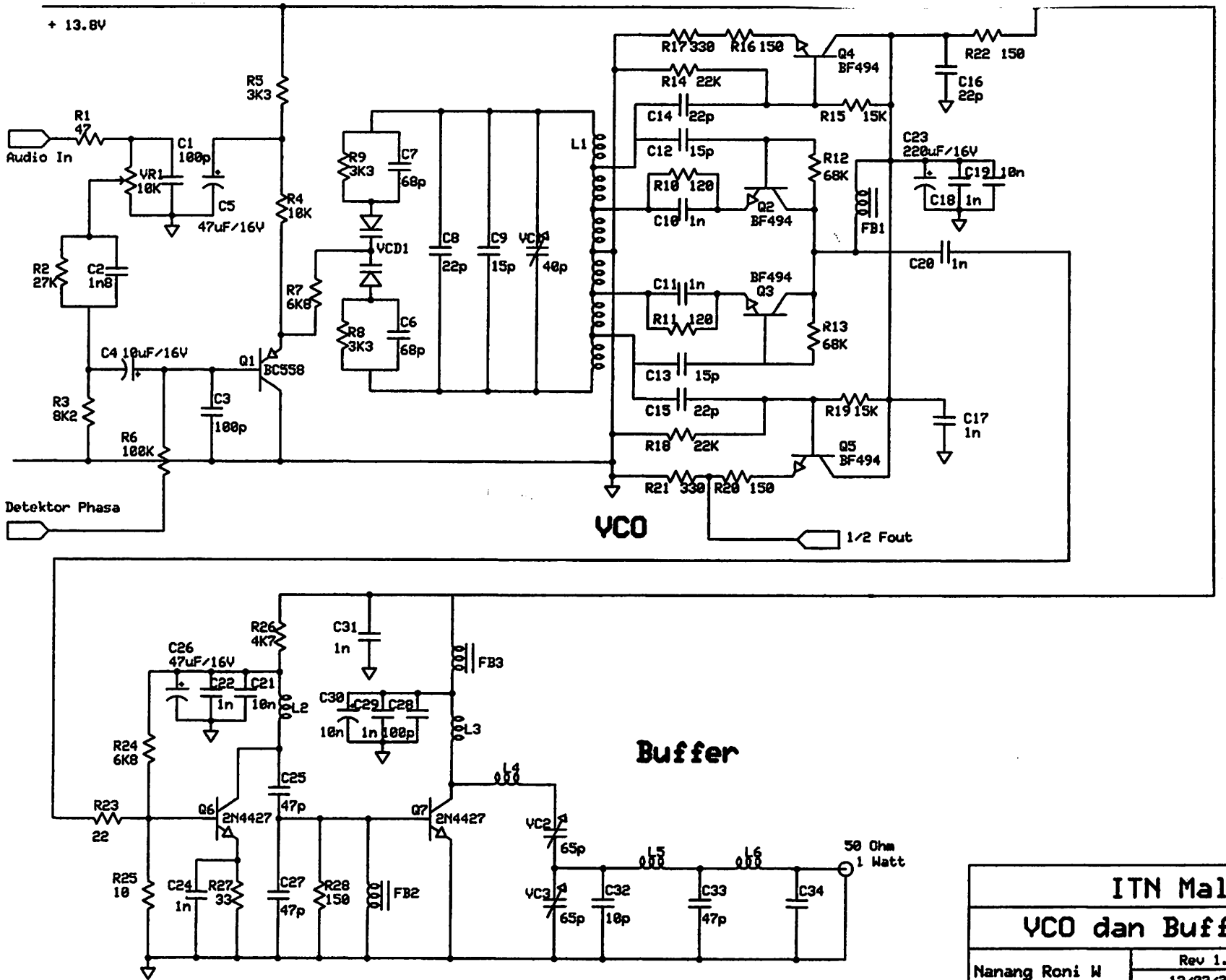
Dalam pelaksanaan Ujian Skripsi Jenjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

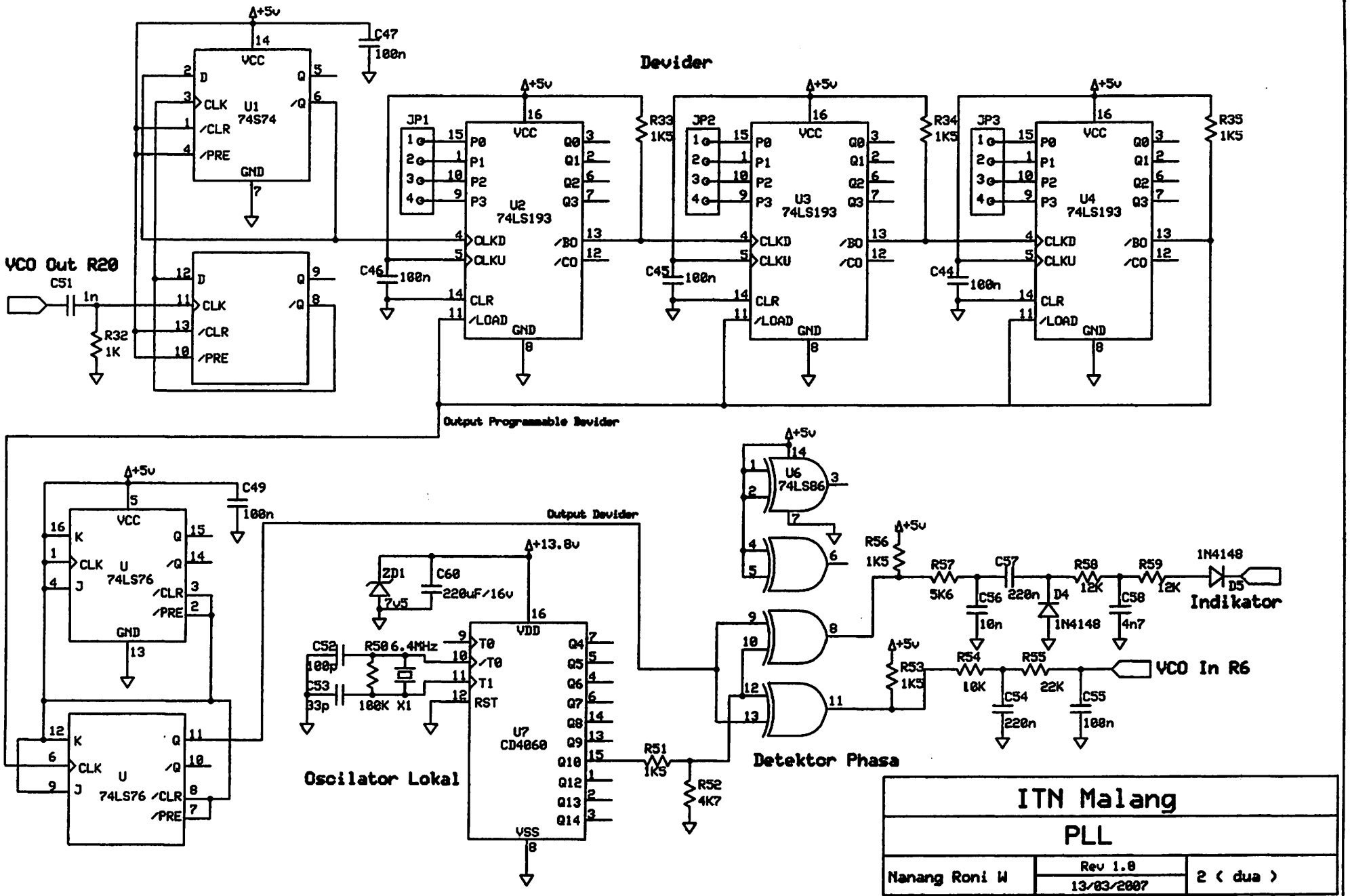
NAMA : WAHYU RONI W
NIM : 02.17.062.
Perbaikan meliputi :

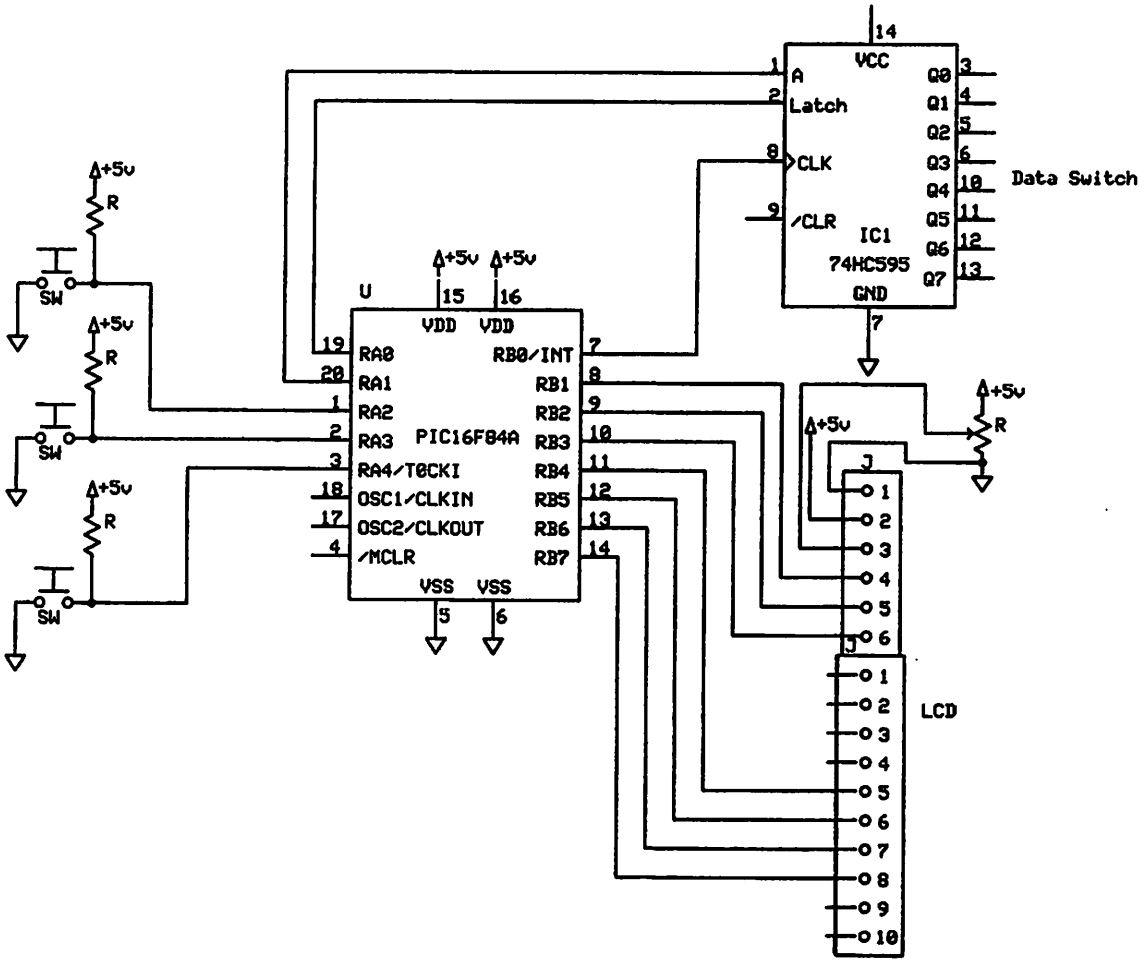
Sebaiknya Alat bapa Uji Laporan

Malang, 17-03-2007

(Rowang S)


+ 13.8V
R1 47
Audio In
C1 100p
VR1 10K
C5 47uF/16V
R5 3K3
R4 10K
R2 27K
C2 1n8
R7 6K8
C4 10uF/16V
Q1 BC558
R3 8K2
R6 100K
C3 100p
Detektor Phasa
R9 3K3
C7 68p
VCD1
R8 3K3
C6 68p
C8 22p
C9 15p
VC1 40p
L1
R17 330
R16 150
Q4 BF494
R14 22K
C14 22p
R15 15K
C12 15p
R10 120
C10 1n
Q2 BF494
R12 68K
FB1
C11 1n
R11 120
BF494 Q3
R13 68K
C13 15p
C15 22p
R19 15K
R18 22K
Q5 BF494
R21 330
R20 150
1/2 Fout
R22 150
C16 22p
C23 220uF/16V
C19 10n
C18 1n
C20 1n
C17 1n
VCO
R26 4K7
C26 47uF/16V
C22 1n
C21 10n
C31 1n
FB3
C30 10n
C29 1n
C28 100p
L2
L3
L4
R24 6K8
C25 47p
R23 22
Q6 2N4427
Q7 2N4427
VC2 65p
L5
L6
50 Ohm 1 Watt
R25 10
C24 1n
R27 33
C27 47p
R28 150
FB2
VC3 65p
C32 10p
C33 47p
C34
Buffer
ITN Malang
VCO dan Buffer 1 Watt
Nanang Roni W
Rev 1.0
12/03/2007
1 (Satu)


Devider
VCO Out R20
C51
1n
R32
1K
U1
74S74
C47
100n
JP1
JP2
JP3
U2
74LS193
U3
74LS193
U4
74LS193
R33
1K5
R34
1K5
R35
1K5
C46
100n
C45
100n
C44
100n
Output Programmable Devider
C49
100n
U
74LS76
Output Devider
ZD1
7v5
C60
220uF/16v
+13.8v
C52
100p
C53
33p
R506.4MHz
100K X1
U7
CD4060
R51
1K5
R52
4K7
Oscilator Lokal
U6
74LS86
Detektor Phasa
R56
1K5
R57
5K6
C57
220n
C56
10n
R58
12K
R59
12K
C58
4n7
D4
1N4148
1N4148
D5
Indikator
R53
1K5
R54
10K
R55
22K
C54
220n
C55
100n
VCO In R6
ITN Malang
PLL
Nanang Roni W
Rev 1.0
13/03/2007
2 (dua)



Company Name		
Schematic Name		
Designer's name	Rev 1.0 3/9/2007	Page # or name

MMBV2101LT1 Series, MV2105, MV2101, MV2109, LV2205, LV2209

Silicon Tuning Diodes

6.8–100 pF, 30 Volts
Voltage Variable Capacitance Diodes

These devices are designed in popular plastic packages for the high volume requirements of FM Radio and TV tuning and AFC, general frequency control and tuning applications. They provide solid–state reliability in replacement of mechanical tuning methods. Also available in a Surface Mount Package up to 33 pF.

- High Q
- Controlled and Uniform Tuning Ratio
- Standard Capacitance Tolerance – 10%
- Complete Typical Design Curves

ON Semiconductor™

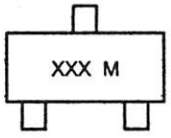
http://onseml.com

SOT–23

TO–92

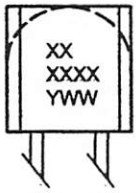
MARKING DIAGRAM

TO–236AB, SOT–23
CASE 318–08
STYLE 8



XXX = Device Code*
M = Date Code
* See Table

TO–226AC, TO–92
CASE 182
STYLE 1



XX = Device Code Line 1*
XXXX = Device Code Line 2*
M = Date Code
* See Table

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Vdc
Forward Current	I_F	200	mAdc
Forward Power Dissipation	P_D		mW
@ T_A = 25°C MMBV21xx		225	mW/°C
Derate above 25°C		1.8	
@ T_A = 25°C MV21xx		280	
Derate above 25°C LV22xx		2.8	
Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

DEVICE MARKING

MMBV2101LT1 = M4G	MMBV2108LT1 = 4X	MV2109 = MV2109
MMBV2103LT1 = 4H	MMBV2109LT1 = 4J	LV2205 = LV2205
MMBV2105LT1 = 4U	MV2101 = MV2101	LV2209 = LV2209
MMBV2107LT1 = 4W	MV2105 = MV2105	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$				Vdc
MMBV21xx, MV21xx		30	–	–	
LV22xx		25	–	–	
Reverse Voltage Leakage Current (V_R = 25 Vdc, T_A = 25°C)	I_R	–	–	0.1	μAdc
Diode Capacitance Temperature Coefficient (V_R = 4.0 Vdc, f = 1.0 MHz)	TC_C	–	280	–	ppm/°C

Preferred devices are recommended choices for future use and best overall value.

Device	C_T, Diode Capacitance V_R = 4.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 4.0 Vdc, f = 50 MHz	TR, Tuning Ratio C_2/C_{30} f = 1.0 MHz		
	Min	Nom	Max	Typ	Min	Typ	Max
MMBV2101LT1/MV2101	6.1	6.8	7.5	450	2.5	2.7	3.2
MMBV2103LT1	9.0	10	11	400	2.5	2.9	3.2
LV2205/MMBV2105LT1/MV2105	13.5	15	16.5	400	2.5	2.9	3.2
MMBV2107LT1	19.8	22	24.2	350	2.5	2.9	3.2
MMBV2108LT1	24.3	27	29.7	300	2.5	3.0	3.2
LV2209MMBV2109LT1/MV2109	29.7	33	36.3	200	2.5	3.0	3.2

MMBV2101LT1, MMBV2103LT1, MMBV2105LT1, MMBV2107LT1 thru MMBV2109LT1, are also available in bulk. Use the device title and drop the "T1" suffix when ordering any of these devices in bulk.

PARAMETER TEST METHODS

1. C_T, DIODE CAPACITANCE

($C_T = C_C + C_J$). C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

2. TR, TUNING RATIO

TR is the ratio of C_T measured at 2.0 Vdc divided by C_T measured at 30 Vdc.

3. Q, FIGURE OF MERIT

Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equations:

$$Q = \frac{2\pi fC}{G}$$

(Boonton Electronics Model 33AS8 or equivalent). Use Lead Length ≈ 1/16".

4. TC_C, DIODE CAPACITANCE TEMPERATURE COEFFICIENT

TC_C is guaranteed by comparing C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = −65°C with C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = +85°C in the following equation, which defines TC_C:

$$TC_C = \left|\frac{C_T(+85°C) - C_T(-65°C)}{85 + 65}\right| \cdot \frac{10^6}{C_T(25°C)}$$

Accuracy limited by measurement of C_T to ±0.1 pF.

TYPICAL DEVICE CHARACTERISTICS

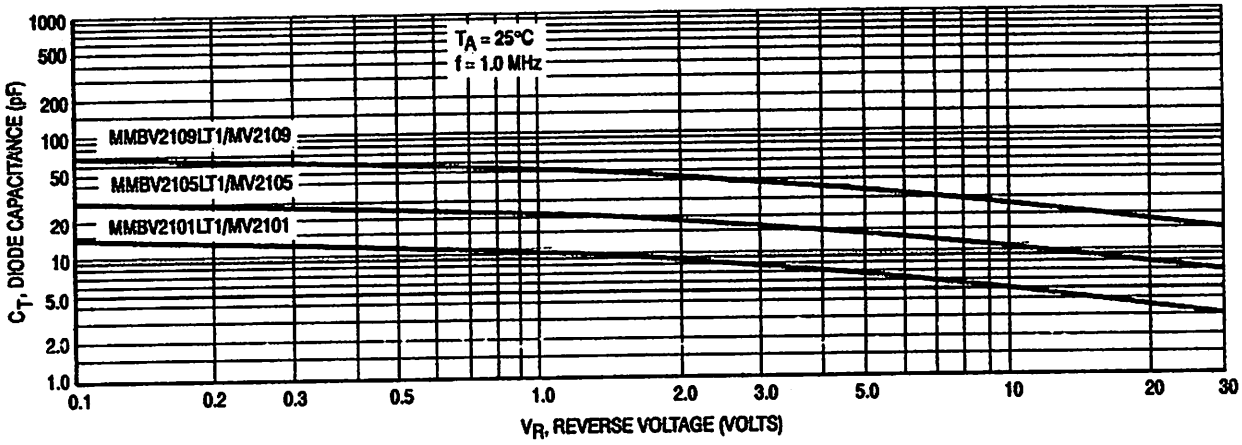


Figure 1. Diode Capacitance versus Reverse Voltage

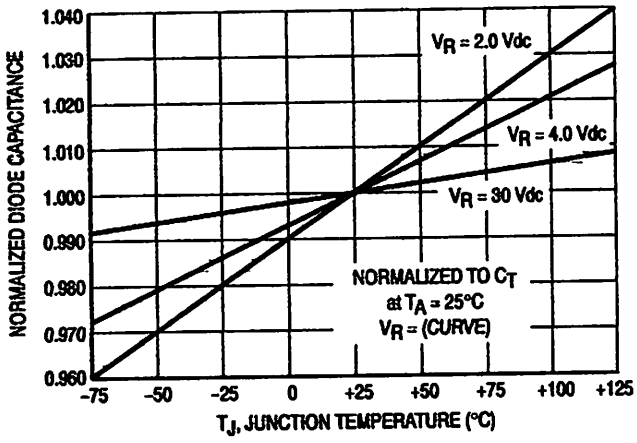


Figure 2. Normalized Diode Capacitance versus Junction Temperature

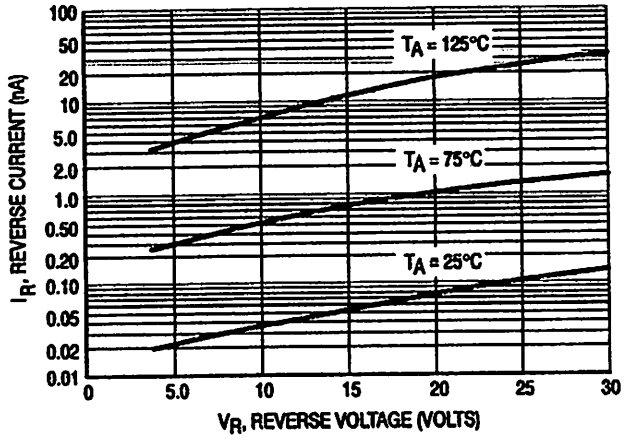


Figure 3. Reverse Current versus Reverse Bias Voltage

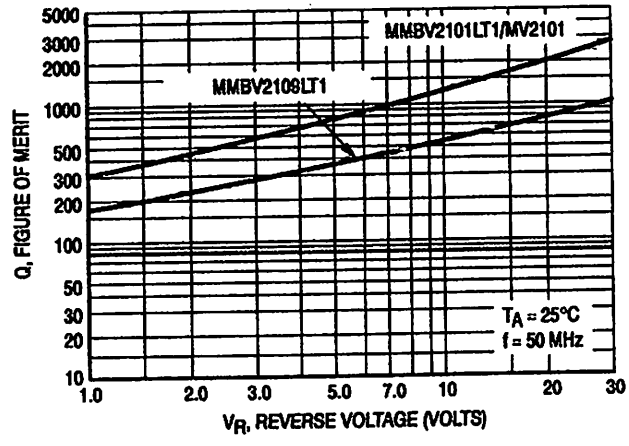


Figure 4. Figure of Merit versus Reverse Voltage

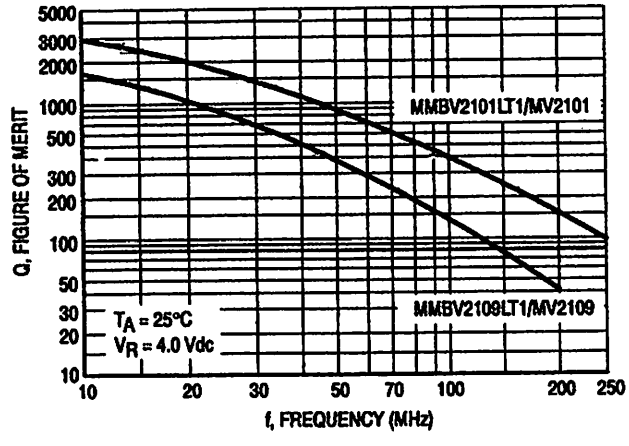
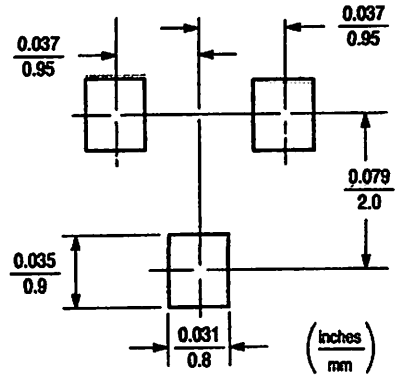


Figure 5. Figure of Merit versus Frequency

INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–23

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches.

The stencil opening size for the surface mounted package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 7 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time.

The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

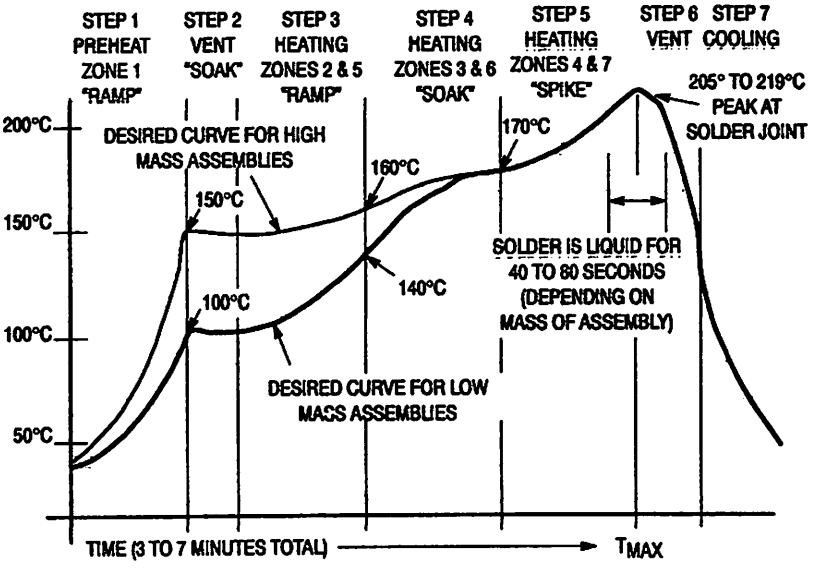
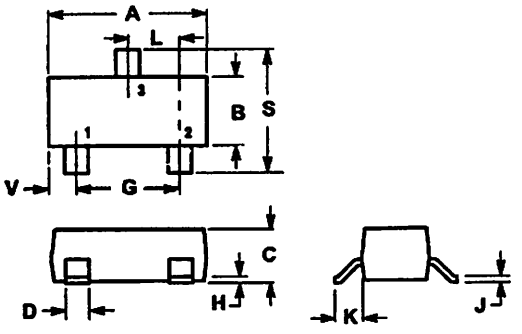


Figure 6. Typical Solder Heating Profile

PACKAGE DIMENSIONS

SOT–23 (TO–236AB)
CASE 318–08
ISSUE AF



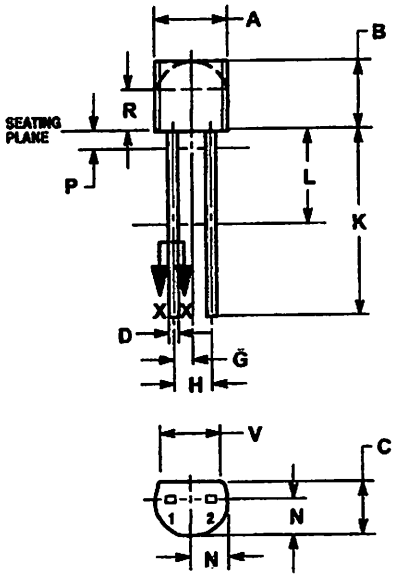
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

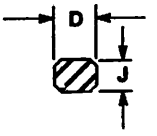
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 6:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

PACKAGE DIMENSIONS

TO–92 (TO–226AC)
CASE 182–06
ISSUE L





SECTION X–X

STYLE 1:
PIN 1. ANODE
2. CATHODE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND ZONE R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.21
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.050 BSC		1.27 BSC	
H	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.41
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.03	2.66
P	—	0.050	—	1.27
R	0.115	—	2.93	—
V	0.135	—	3.43	—

Thermal Clad is a trademark of the Bergquist Company.

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Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.

MMBV2101LT1/D

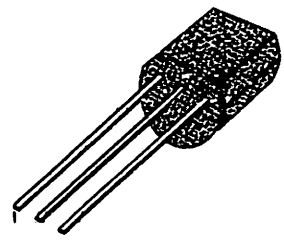
BC556/557/558/559/560

PNP EPITAXIAL SILICON TRANSISTOR

SWITCHING AND AMPLIFIER

- HIGH VOLTAGE: BC558, V_{CEO}= -65V
- LOW NOISE: BC559, BC560
- Complement to BC548 ... BC 550

TO-92



1. Collector 2. Base 3. Emitter

ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

Characteristic	Symbol	Rating	Unit
Collector-Base Capacitance	V_{CBO}		
: BC558		-80	V
: BC557/560		-50	V
: BC558/559		-30	V
Collector-Emitter Voltage	V_{CEO}		
: BC556		-65	V
: BC557/560		-45	V
: BC558/559		-30	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current (DC)	I_C	-100	mA
Collector Dissipation	P_C	500	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-65 ~ 150	°C

ELECTRICAL CHARACTERISTICS (T_A=25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Collector Cut-off Current	I_{CBO}	V_{CB}= -30V, I_E=0			-15	nA
DC Current Gain	h_{FE}	V_{CE}= -5V, I_C=2mA	110		800	
Collector Emitter Saturation Voltage	V_{CE} (sat)	I_C= -10mA, I_B= -0.5mA		-90	-300	mV
		I_C= -100mA, I_B= -5mA		-250	-650	mV
Collector Base Saturation Voltage	V_{BE} (on)	I_C= -10mA, I_B= -0.5mA		-700		mV
		I_C= -100mA, I_B= -5mA		-900		mV
Base Emitter On Voltage	V_{BE} (on)	V_{CE}= -5V, I_C= -2mA	-600	-660	-750	mV
		V_{CE}= -5V, I_C= -10mA			-800	mV
Current Gain Bandwidth Product	f_T	V_{CE}= -5V, I_C= -10mA		150		MHz
Collector Base Capacitance	C_{CBO}	V_{CB}= -10V, f=1MHz			6	pF
Noise Figure : BC556/557/558	NF	V_{CE}= -5V, I_C= -200μA		2	10	dB
: BC559/560		f=1KHz, R_G=2KΩ		1	4	dB
: BC559	NF	V_{CE}= -5V, I_C= -200μA		1.2	4	dB
: BC560		R_G=2KΩ f=30~15000MHz		1.2	2	dB

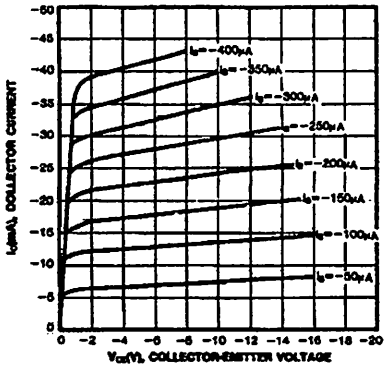
h_{FE} CLASSIFICATION

Classification	A	B	C
h_{FE}	110-220	200-450	420-800

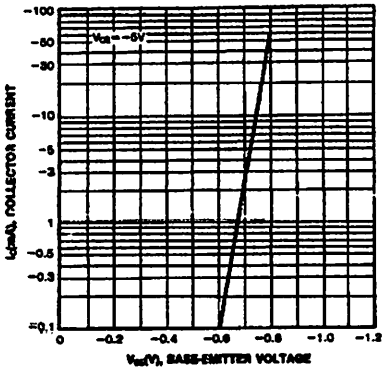
Rev. B

FAIRCHILD SEMICONDUCTOR™

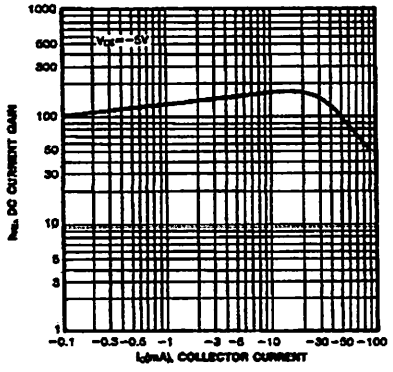
STATIC CHARACTERISTIC



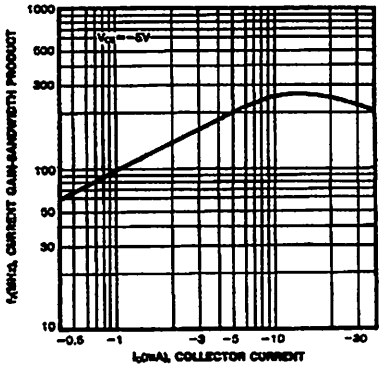
BASE-EMITTER VOLTAGE



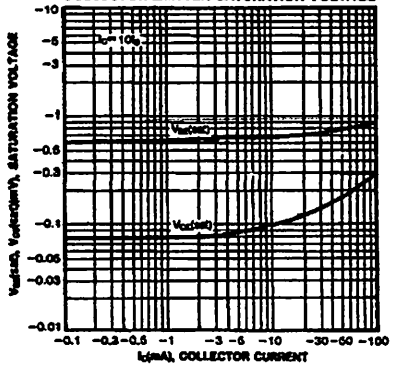
DC CURRENT GAIN



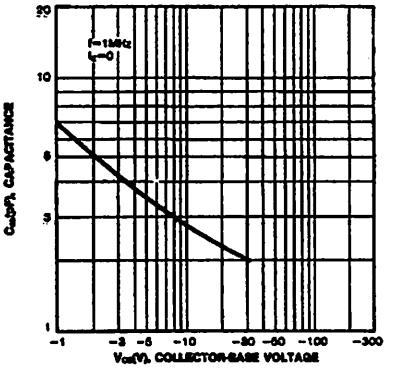
CURRENT GAIN-BANDWIDTH PRODUCT



BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE



COLLECTOR OUTPUT CAPACITANCE



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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

BF494 · BF495

NPN SILICON RF SMALL SIGNAL TRANSISTORS

MICRO ELECTRONICS

THE BF494, BF495 ARE NPN SILICON PLANAR EPITAXIAL TRANSISTORS FOR RF SMALL SIGNAL APPLICATIONS UP TO 100MHz.

CASE TO-92E

CBE

ABSOLUTE MAXIMUM RATINGS

		BF494	BF495
Collector-Base Voltage	V_{CBO}	30V	30V
Collector-Emitter Voltage	V_{CEO}	20V	20V
Emitter-Base Voltage	V_{EBO}	5V	5V
Collector Current	I_C	30mA	
Total Power Dissipation ($T_A \leq 75°C$)	P_{tot}	300mW derate 4mW/°C above 75°C	
Operating Junction & Storage Temperature	T_j, T_{stg}	-55 to 150°C	

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	BF494 MIN	BF494 TYP	BF494 MAX	BF495 MIN	BF495 TYP	BF495 MAX	UNIT	TEST CONDITIONS
Emitter-Base Breakdown Voltage	BV_{EBO}	5			5			V	I_E=10μA I_C=0
Collector Cutoff Current	I_{CBO}			0.1			0.1	μA	V_{CB}=30V I_E=0
Collector Cutoff Current	I_{CEO}			1			1	μA	V_{CE}=20V I_B=0
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$		0.1			0.1		V	I_C=10mA I_B=1mA
Base-Emitter Voltage	V_{BE}	.65	.68	.74	.65	.68	.74	V	I_C=1mA V_{CE}=10V
D.C. Current Gain	H_{FE}	67	115	220	36	67	125		I_C=1mA V_{CE}=10V*
Current Gain-Bandwidth Product	f_T		260			200		MHz	I_C=1mA V_{CE}=10V
Feedback Capacitance	Cre		.85			.85		pF	I_C=1mA V_{CE}=10V f=450KHz
Noise Figure	NF		4			4		dB	I_C=1mA V_{CE}=10V R_G=100Ω f=100MHz
Mixing Noise Figure	NF_c		2					dB	I_C=1mA V_{CE}=10V R_G=830Ω f=1MHz
	NF_c					2.5		dB	I_C=1mA V_{CE}=10V R_G=670Ω f=1MHz

* HFE Grouping :

B : 100-220 C : 72-110 D : 36-80

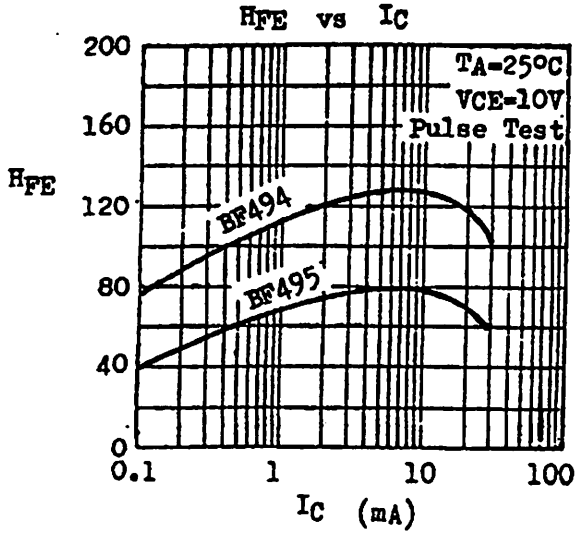
MICRO ELECTRONICS LTD.

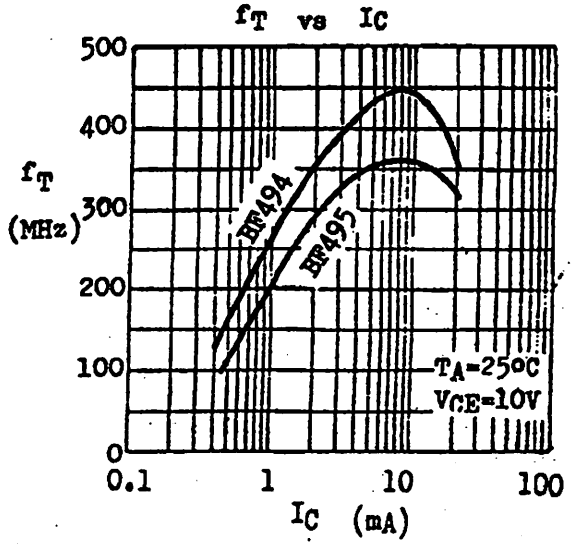
38 HUNG TO ROAD, KWUN TONG, HONG KONG. TELEX 43510
KWUN TONG P. O. BOX69477 CABLE ADDRESS "MICROTRON" FAX: 3-4103
TELEPHONE:- 3-430181-6 ~~3-699969.~~ ~~3-662428~~

=450kHz	g_{11}=0.33mU	$\|y_{12}\|$=2.8μU	$\|y_{21}\|$=36mU	g_{22}=6μU
ommon Emitter	b_{11}=0.065mU	$-\theta_{12}$=90°	$-\theta_{21}$=0°	b_{22}=4.5μU
	C_{11}=23pF			C_{22}=1.6pF
=10.7MHz	g_{11}=0.45mU	$\|y_{12}\|$=65μU	$\|y_{21}\|$=36mU	g_{22}=8.5μU
ommon Emitter	b_{11}=1.5mU	$-\theta_{12}$=90°	$-\theta_{21}$=10°	b_{22}=0.11mU
	C_{11}=22pF			C_{22}=1.6pF
=100MHz	g_{11}=36mU	$\|y_{12}\|$=420μU	$\|y_{21}\|$=33mU	g_{22}=22μU
ommon Base	$-b_{11}$=3mU	$-\theta_{12}$=88°	$-\theta_{21}$=146°	b_{22}=1.1mU
	$-C_{11}$=4.8pF			C_{22}=1.75pF

F495 TYPICAL y-PARAMETERS AT T_A=25°C I_C=1mA V_{CE}=10V

=450kHz	g_{11}=0.5mU	$\|y_{12}\|$=2.6μU	$\|y_{21}\|$=36mU	g_{22}=2.7μU
ommon Emitter	b_{11}=0.1mU	$-\theta_{12}$=90°	$-\theta_{21}$=0°	b_{22}=4.5μU
	C_{11}=32pF			C_{22}=1.6pF
=10.7MHz	g_{11}=0.6mU	$\|y_{12}\|$=60μU	$\|y_{21}\|$=36mU	g_{22}=4.5μU
ommon Emitter	b_{11}=2mU	$-\theta_{12}$=90°	$-\theta_{21}$=10°	b_{22}=0.11mU
	C_{11}=30pF			C_{22}=1.6pF
=100MHz	g_{11}=38mU	$\|y_{12}\|$=410μU	$\|y_{21}\|$=34mU	g_{22}=12μU
ommon Base	$-b_{11}$=1mU	$-\theta_{12}$=85°	$-\theta_{21}$=140°	b_{22}=1.1mU
	$-C_{11}$=1.6pF			C_{22}=1.75pF





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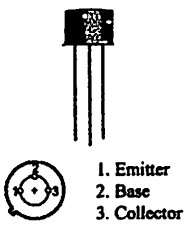
2N4427

& MICROWAVE DISCRETE
W POWER TRANSISTORS

ures

Silicon NPN, To-39 packaged VHF/UHF Transistor
1 Watt Minimum Power Output @ 175 MHz
500 MHz Current-Gain Bandwidth Product @ 50mA
Power Gain, G_{PE} = 10dB (Min) @ 175 MHz



TO-39

CRIPTION:

on NPN transistor, designed for VHF and UHF equipment. Applications include amplifier; pre-driver, driver, and ut stages. Also suitable for oscillator and frequency-multiplier functions.

OLUTE MAXIMUM RATINGS (Tcase = 25°C)

Symbol	Parameter	Value	Unit
V_{CEO}	Collector-Emitter	20	Vdc
V_{CBO}	Collector-Base Voltage	40	Vdc
V_{EBO}	Emitter-Base Voltage	2.0	Vdc
I_C	Collector Current	400	mA

rmal Data

P_D	Total Device Dissipation @ T_A = 25°C Derate above 25°C	1.0 5.71	Watts mW/ °C

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:TRICAL SPECIFICATIONS (Tcase = 25°C)

C

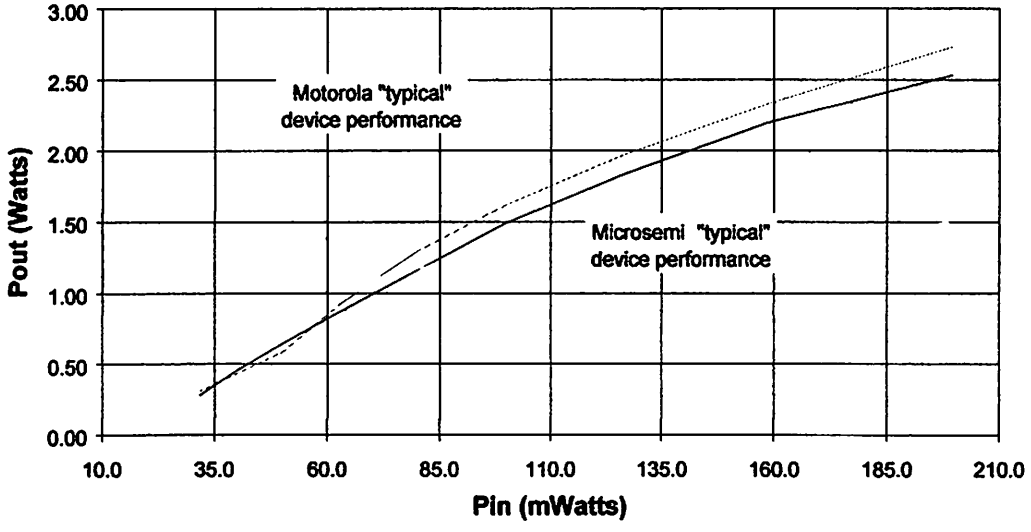
mbol	Test Conditions	Value			
		Min.	Typ.	Max.	Unit
CER	Collector-Emitter Sustaining Voltage (IC = 5.0 mAdc, RBE = 10 ohms)	40	-	-	Vdc
CEO	Collector-Emitter Sustaining Voltage (IC=5.0 mAdc, IB=0)	20	-	-	Vdc
EO	Collector Cutoff Current (VCE = 12 Vdc, IB = 0)	-	-	20	µA
EX	Collector Cutoff Current (VCE = 40 Vdc, VBE = -1.5 Vdc)	-	-	100	µA
EBO	Emitter Cutoff Current (VEB = 2.0 Vdc, IC = 0)	-	-	100	µA
HFE	DC Current Gain (IC = 100 mAdc, VCE = 5.0 Vdc) (IC = 360 mAdc, VCE = 5.0 Vdc)	10 5	- -	200 -	- -
E(sat)	Collector-Emitter Saturation Voltage (IC = 100 mAdc, IB = 20 mAdc)	-	-	0.5	Vdc

MIC

mbol	Test Conditions	Value			
		Min.	Typ.	Max.	Unit
f_T	Current-Gain - Bandwidth Product (IC = 50 mAdc, VCE = 15 Vdc, f = 200 MHz)	500	-	-	MHz
OB	Output Capacitance (VCB = 12 Vdc, IE = 0, f = 1.0 MHz)	-	4.0	-	pF

TIONAL

Symbol	Test Conditions		Value			
			Min.	Typ.	Max.	Unit
G_{PE}	Power Gain	Test Circuit-Figure 1 Pin = 0.1 W, VCE = 12Vdc f = 175 MHz	10	-	-	dB
Pout	Output Power	Test Circuit-Figure 1 Pin = 0.1 W, VCE = 12Vdc f = 175 MHz	1.0	-	-	Watts
η_C	Collector Efficiency	Test Circuit-Figure 1 Pin = 0.1 W, VCE = 12Vdc f = 175 MHz	45	-	-	%



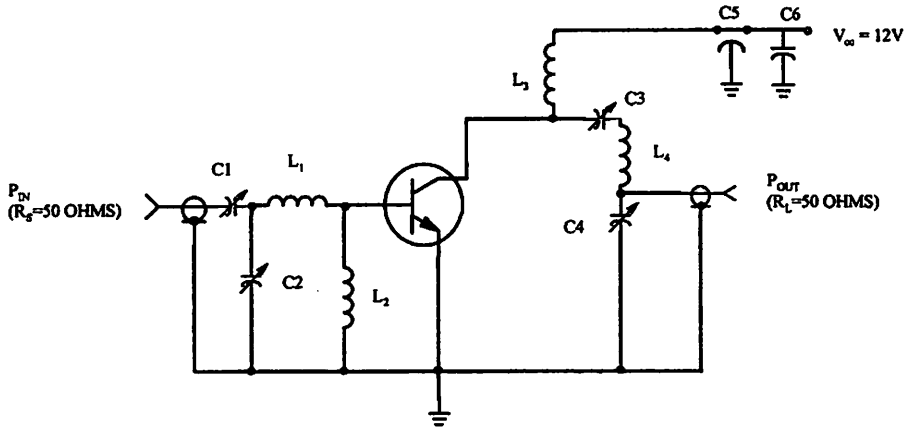


Figure 1 - 175 MHz RF AMPLIFIER CIRCUIT FOR G_{PE}, P_{OUT}, AND EFFICIENCY SPECIFICATIONS.

L_1: 2 TURNS No. 16 wire, 3/16" ID, 1/4" long

L_2: Ferrite choke, Z=450 ohms

L_3: 2 TURNS No. 16 wire, 1/4" ID, 1/4" long

L_4: 4 TURNS No. 16 wire, 3/8" ID, 3/8" long

Capacitor values in pF unless

Tuning capacitors are air variable otherwise indicated.

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Low Power PA, LNA, and General Purpose Discrete Selector Guide

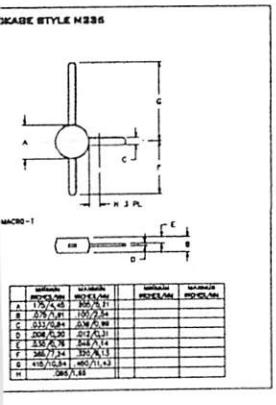
Package	Device	Type	GPE Freq (MHz	Pout (watts)	GPE (dB)	Efficiency (%)	GPE VCC	BVCEO	IC max (mA)
SO-8	MRF4427, R2	NPN	175	0.15	18	60	12	20	400
TO-39	2N4427	NPN	175	1	10	50	12	20	400
POWER MACRO	MRF553	NPN	175	1.5	11.5	60	12.5	16	500
POWER MACRO	MRF553T	NPN	175	1.5	11.5	50	12.5	16	500
TO-39	MRF607	NPN	175	1.75	11.5	50	12.5	16	330
TO-39	2N6255	NPN	175	3	7.8	50	12.5	18	1000
TO-72	2N5179	NPN	200		20		6	12	50
MACRO X	MRF559	NPN	512	0.5	10	65	7.5	16	150
MACRO X	MRF559	NPN	512	0.5	13	60	12.5	16	150
TO-39	2N3866A	NPN	400	1	10	45	28	30	400
SO-8	MRF3866, R1, R2	NPN	400	1	10	45	28	30	400
POWER MACRO	MRF555	NPN	470	1.5	11	50	12.5	16	400
POWER MACRO	MRF555T	NPN	470	1.5	11	50	12.5	16	400
MACRO X	MRF559	NPN	870	0.5	6.5	70	7.5	16	150
MACRO X	MRF559	NPN	870	0.5	9.5	65	12.5	16	150
SO-8	MRF8372,R1,R2	NPN	870	0.75	8	55	12.5	16	200
POWER MACRO	MRF557	NPN	870	1.5	8	55	12.5	16	400
POWER MACRO	MRF557T	NPN	870	1.5	8	55	12.5	16	400

RF (Low Power PA / General Purpose) Selection Guide

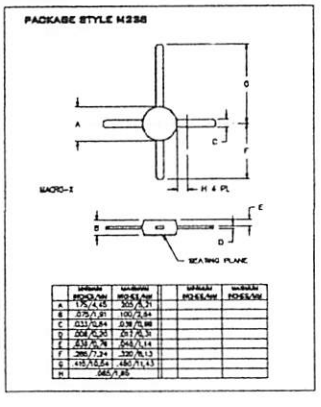
Packag	Device	Type	Freq (MHz)	NF	NF(dB)	IC (mA)	NF VCE	GN (dB)	Gu Max (dB)	Ftau (MHz)	Ccb(pF)	BVCEO	IC max (mA)
TO-39	2N5109	NPN	200	3	10	15			12	1200	3.5	20	400
TO-39	MRF5943C	NPN	200	3.4	30	15			11.4	1000		30	400
SO-8	MRF5943, R1, R2	NPN	200	3.4	30	15			15	1300		30	400
TO-72	2N5179	NPN	200	4.5	1.5	8			17	900	1	12	50
TO-72	2N2857	NPN	300	5.5	50	6			13	1600	1	15	40
TO-39	MRF517	NPN	300	7.5	50	15			5.5	4600	3	25	150
TO-72	MRF904	NPN	450	1.5	5	6			11	4000	1	15	30
TO-72	2N6304	NPN	450	5	2	5			14	1400	1	15	50
MACRO T	BFR91	NPN	500	1.9	2	5	11		16.5	5000	1	12	35
MACRO T	BFR96	NPN	500	2	10	10			14.5	500	2.6	15	100
SO-8	MRF5812, R1, R2	NPN	500	2	50	10	15.5		17.8	5000		15	200
MACRO X	MRF581A	NPN	500	2	50	10	14		15	5000		15	200
Macro	BFR90	NPN	500	2.4	2	10	15		18	5000	1	15	30
TO-72	BFY90	NPN	500	2.5	2	5			20	1300		15	50
TO-72	MRF914	NPN	500	2.5	5	10			15	4500		12	40
MACRO X	MRF581	NPN	500	2.5	50	10	15		17.8	5000		16	200
TO-39	MRF586	NPN	500	3	90	15	11		14.5	4500	2.2	17	200
MACRO X	MRF951	NPN	1000	1.3	5	6	14		17	8000	0.45	10	100
MACRO X	MRF571	NPN	1000	1.5	10	6	10			8000	1	10	70
MACRO T	BFR91	NPN	1000	2.5	2	5	8		11	5000	1	12	35
MACRO T	BFR90	NPN	1000	3	2	10	10		12.5	5000	1	15	30
TO-39	MRF545	PNP							14	1400	2	70	400
TO-39	MRF544	NPN							13.5	1500		70	400

RF (LNA / General Purpose) Selection Guide

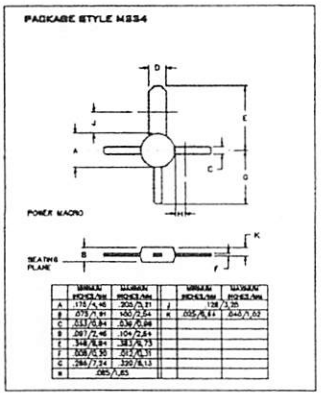
Low Cost RF Plastic Package Options



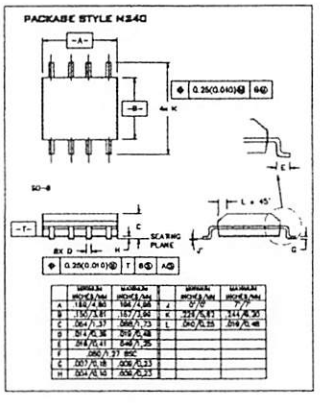
Macro T



Macro X



Power



SO-8

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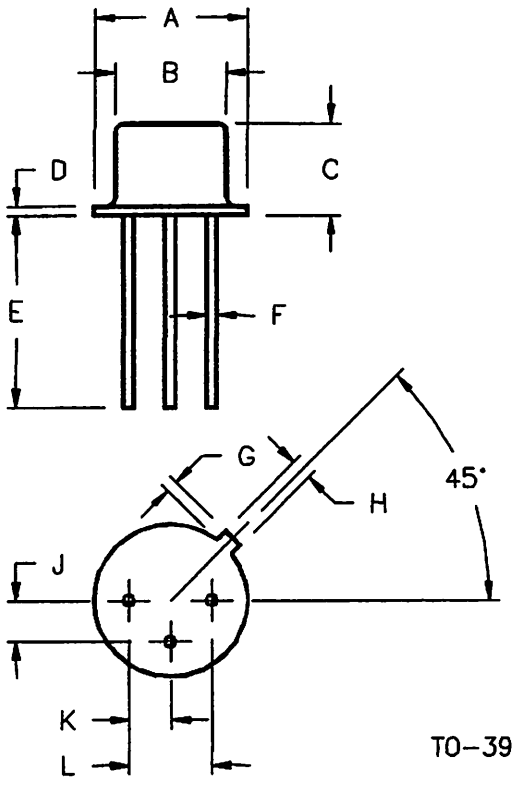
PACKAGE STYLE M246



	MINIMUM INCHES/MM	MAXIMUM INCHES/MM		MINIMUM INCHES/MM	MAXIMUM INCHES/MM
A	.350/8,89	.370/9,40	J	.095/2,41	.105/2,67
B	.315/8,00	.335/8,51	K	.095/2,41	.105/2,67
C	.240/6,10	.260/6,60	L	.190/4,83	.210/5,33
D	.015/0,38	.045/1,14			
E	.500/12,70				
F	.016/0,41	.019/0,48			
G	.029/0,74	.040/1,02			
H	.028/0,71	.034/0,86			

FAIRCHILD
SEMICONDUCTOR™

BC546/547/548/549/550

Switching and Amplifier

- High Voltage: BC546, V_{CEO}=65V
- Low Noise: BC549, BC550
- Complement to BC556 . . BC560

1 TO-92

1. Collector 2. Base 3. Emitter

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage : BC546	80	V
	: BC547/550	50	V
	: BC548/549	30	V
V_{CEO}	Collector-Emitter Voltage : BC546	65	V
	: BC547/550	45	V
	: BC548/549	30	V
V_{EBO}	Emitter-Base Voltage : BC546/547	6	V
	: BC548/549/550	5	V
I_C	Collector Current (DC)	100	mA
P_C	Collector Dissipation	500	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{CBO}	Collector Cut-off Current	V_{CB}=30V, I_E=0			15	nA
h_{FE}	DC Current Gain	V_{CE}=5V, I_C=2mA	110		800	
V_{CE} (sat)	Collector-Emitter Saturation Voltage	I_C=10mA, I_B=0.5mA		90	250	mV
		I_C=100mA, I_B=5mA		200	600	mV
V_{BE} (sat)	Base-Emitter Saturation Voltage	I_C=10mA, I_B=0.5mA		700		mV
		I_C=100mA, I_B=5mA		900		mV
V_{BE} (on)	Base-Emitter On Voltage	V_{CE}=5V, I_C=2mA	580	660	700	mV
		V_{CE}=5V, I_C=10mA			720	mV
f_T	Current Gain Bandwidth Product	V_{CE}=5V, I_C=10mA, f=100MHz		300		MHz
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0, f=1MHz		3.5	6	pF
C_{ib}	Input Capacitance	V_{EB}=0.5V, I_C=0, f=1MHz		9		pF
NF	Noise Figure : BC546/547/548	V_{CE}=5V, I_C=200μA		2	10	dB
	: BC549/550	f=1KHz, R_G=2KΩ		1.2	4	dB
	: BC549	V_{CE}=5V, I_C=200μA		1.4	4	dB
	: BC550	R_G=2KΩ, f=30~15000MHz		1.4	3	dB

h_{FE} Classification

Classification	A	B	C
h_{FE}	110 ~ 220	200 ~ 450	420 ~ 800

Typical Characteristics

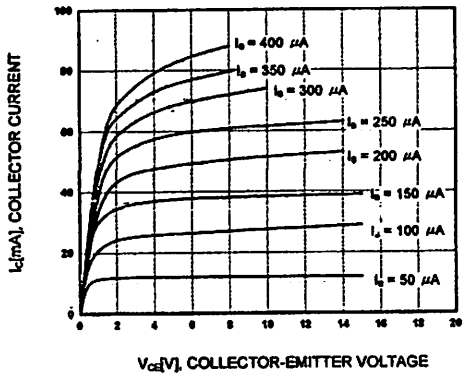


Figure 1. Static Characteristic

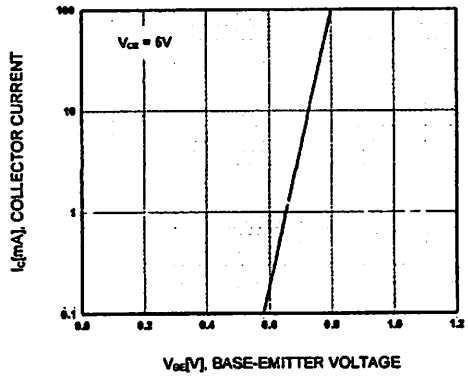


Figure 2. Transfer Characteristic

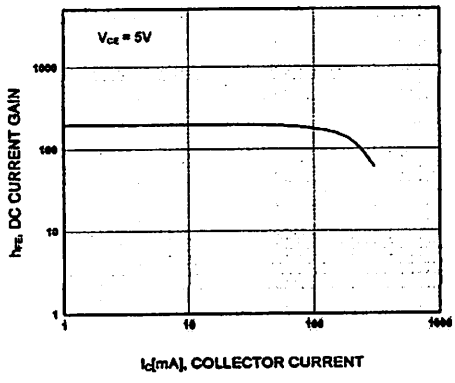


Figure 3. DC current Gain

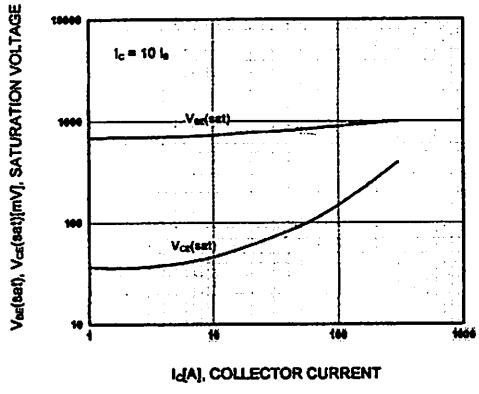


Figure 4. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

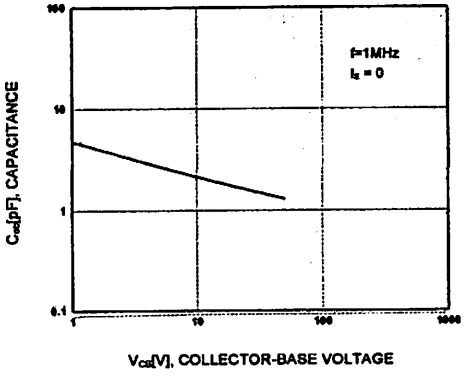


Figure 5. Output Capacitance

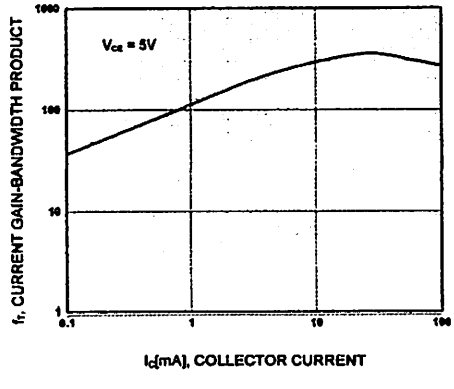
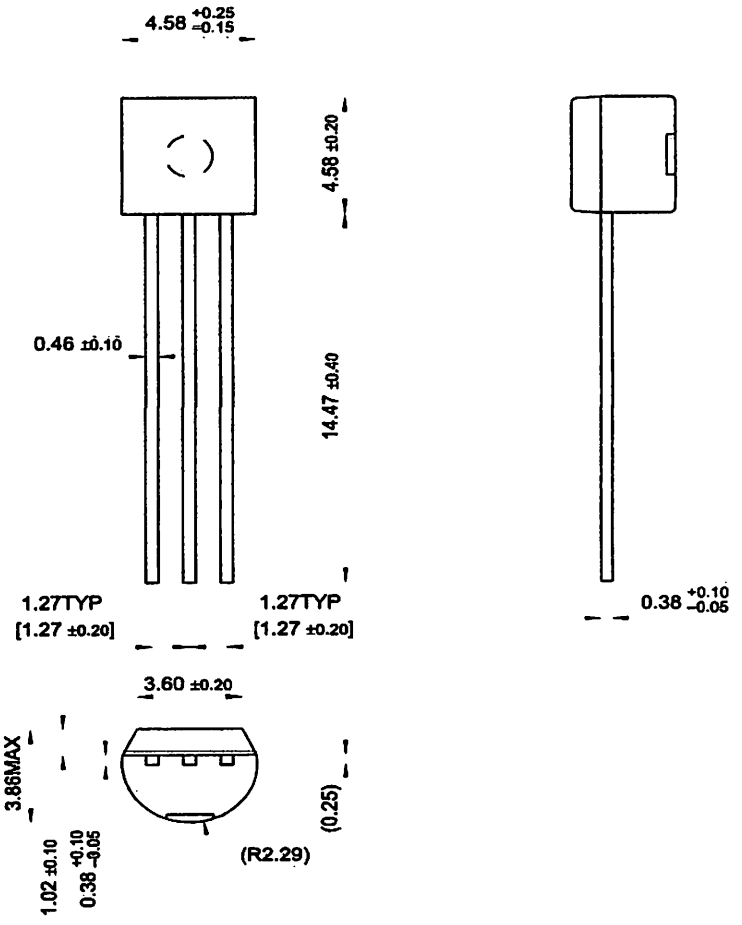


Figure 6. Current Gain Bandwidth Product

Package Demensions

TO-92



Dimensions in Millimeters

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SuperSOT™-6
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

SN74LS76A

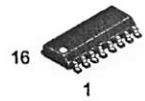
Dual JK Flip-Flop with Set and Clear

The SN74LS76A offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW clock transitions.

ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

LOW POWER SCHOTTKY

PLASTIC
N SUFFIX
CASE 648



SOIC
D SUFFIX
CASE 751B

MODE SELECT – TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	K	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	$\overline{q}$

* Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.

H, h = HIGH Voltage Level

L, l = LOW Voltage Level

X = Immaterial

l, h (q) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the HIGH–to–LOW clock transition

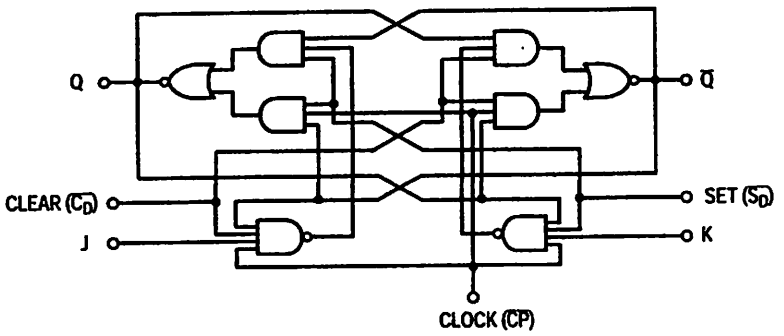
GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA

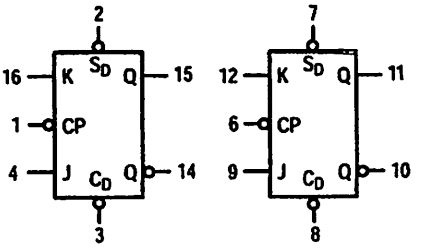
ORDERING INFORMATION

Device	Package	Shipping
SN74LS76AN	16 Pin DIP	2000 Units/Box
SN74LS76AD	16 Pin	2500/Tape & Reel

LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = PIN 5
GND = PIN 13

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage		2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage			0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
				0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current	J, K Clear Clock			20 60 80	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
		J, K Clear Clock			0.1 0.3 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current	J, K Clear, Clock			−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				6.0	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

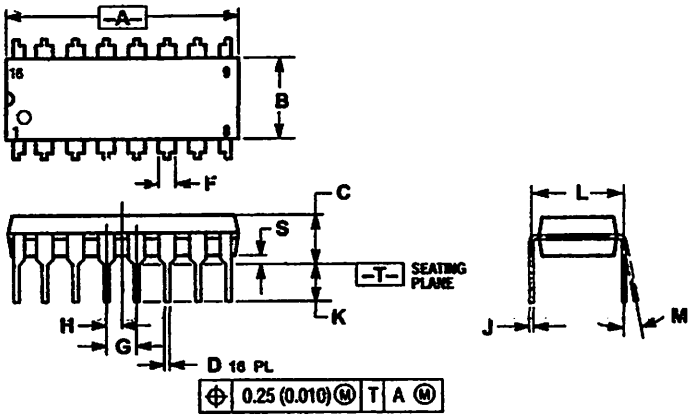
Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	30	45		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Clock, Clear, Set to Output		15	20	ns	
			15	20	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_W	Clock Pulse Width High	20			ns	V_{CC} = 5.0 V
t_W	Clear Set Pulse Width	25			ns	
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

PACKAGE DIMENSIONS

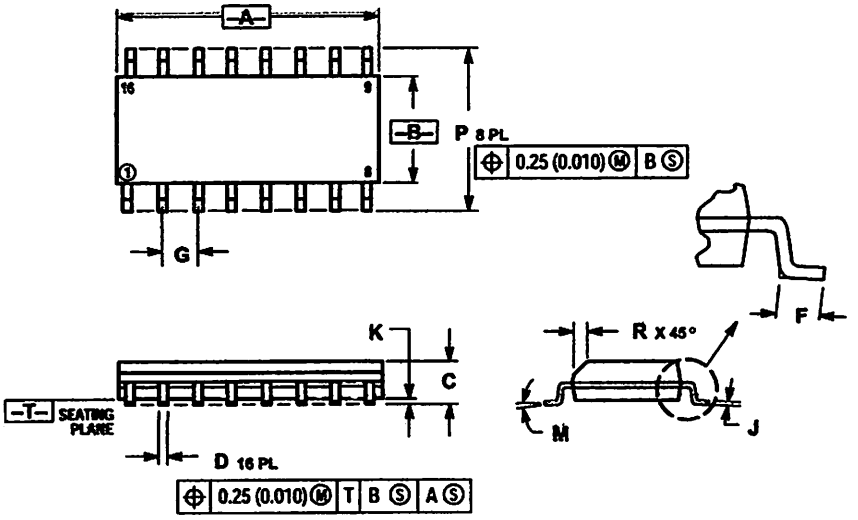
N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PUBLICATION ORDERING INFORMATION

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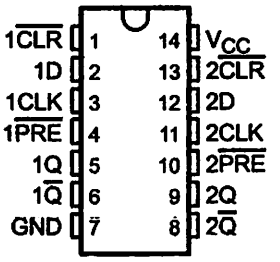
SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDAS143C – APRIL 1982 – REVISED AUGUST 1995

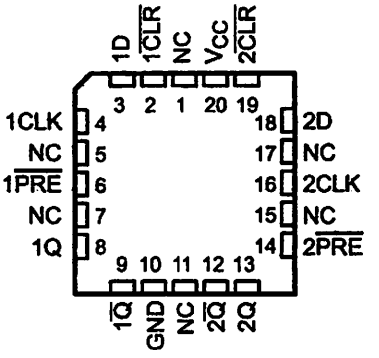
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (C_L = 50 pF) (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS74A	50	6
'AS74A	134	26

SN54ALS74A, SN54AS74A . . . J PACKAGE
SN74ALS74A, SN74AS74A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS74A, SN54AS74A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain two independent positive-edge-triggered D-type flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54ALS74A and SN54AS74A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS74A and SN74AS74A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† The output levels in this configuration are not specified to meet the minimum levels for V_{OH} if the lows at $\overline{PRE}$ and $\overline{CLR}$ are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

TEXAS INSTRUMENTS
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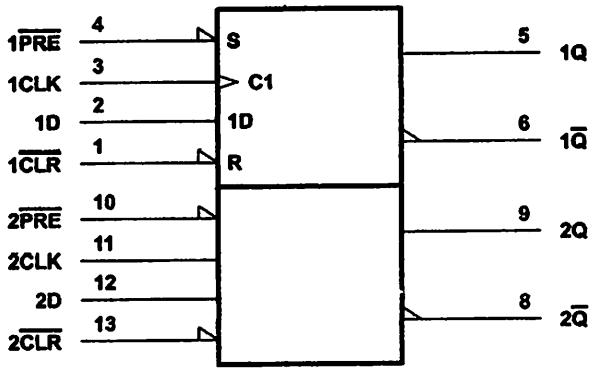
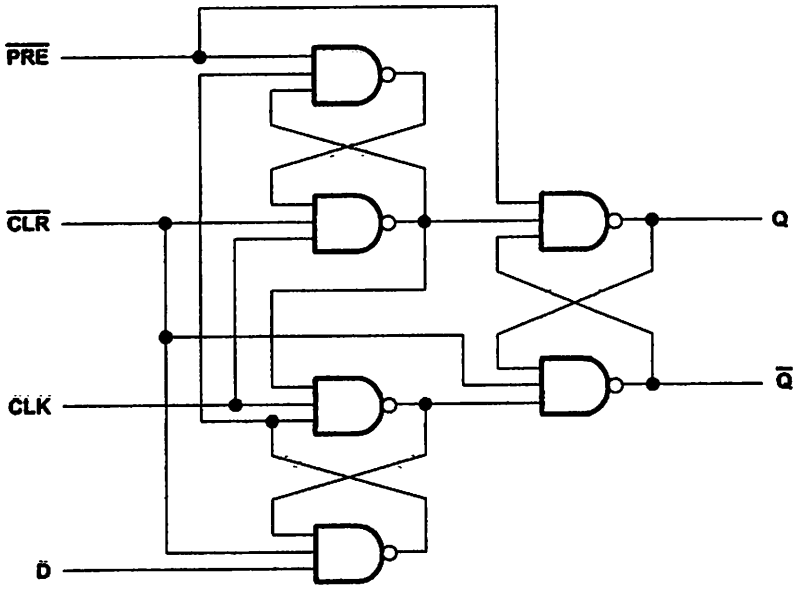
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Operating free-air temperature range, T_A: SN54ALS74A ..... −55°C to 125°C
SN74ALS74A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS74A			SN74ALS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		34	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			15			ns
		CLK high	17.5			14.5			
		CLK low	17.5			14.5			
t_{su}	Setup time before CLK↑	Data	16			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time after CLK↑	Data	2			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS74A			SN74ALS74A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	CLK or D	V_{CC} = 4.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	CLK or D	V_{CC} = 4.5 V,	V_I = 2.7 V			20			20	µA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK or D	V_{CC} = 4.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.4	4		2.4	4	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54ALS74A		SN74ALS74A		
			MIN	MAX	MIN	MAX	
f_{max}			25		34		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	18	3	13	ns
t_{PHL}			5	17	5	15	
t_{PLH}	CLK	Q or $\overline{Q}$	5	23	5	16	ns
t_{PHL}			5	20	5	18	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Operating free-air temperature range, T_A: SN54AS74A ..... −55°C to 125°C
SN74AS74A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS74A			SN74AS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}*	Clock frequency		0		90	0		105	MHz
t_w*	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t_{su}*	Setup time before CLK↑	Data	4.5			4.5			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2			2			
t_h*	Hold time after CLK↑	Data	0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

* On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS74A			SN74AS74A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC}–2			V_{CC}–2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5			–0.5	mA
	$\overline{PRE}$ or $\overline{CLR}$					–1.8			–1.8	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		10.5	16		10.5	16	mA

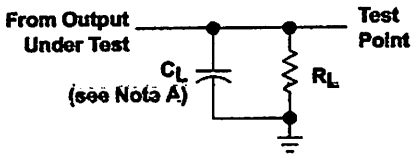
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Figure 1)

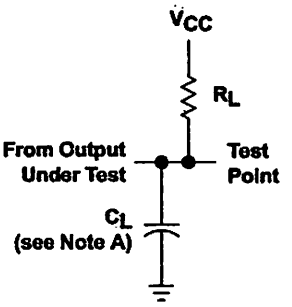
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			SN54AS74A		SN74AS74A		
			MIN	MAX	MIN	MAX	
f_{max}*			90		105		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2	9	2	7.5	ns
t_{PHL}			2.5	11.5	2.5	10.5	
t_{PLH}	CLK	Q or $\overline{Q}$	2.5	10	3	8	ns
t_{PHL}			3.5	10.5	3	9	

* On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not production tested.
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

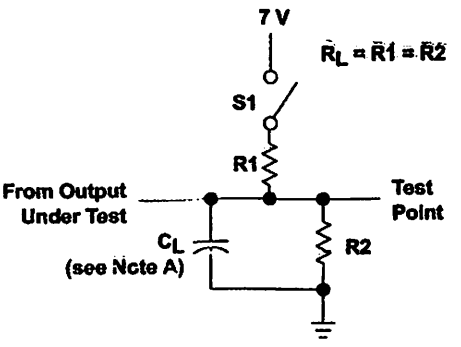
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



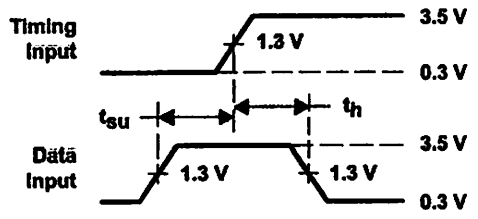
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



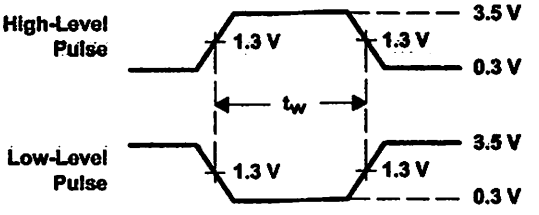
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



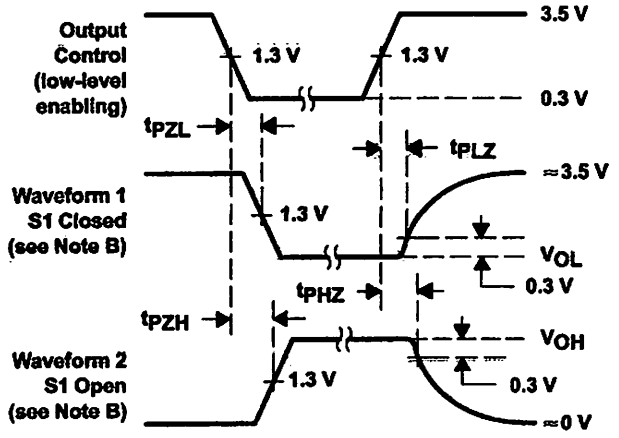
LOAD CIRCUIT FOR 3-STATE OUTPUTS



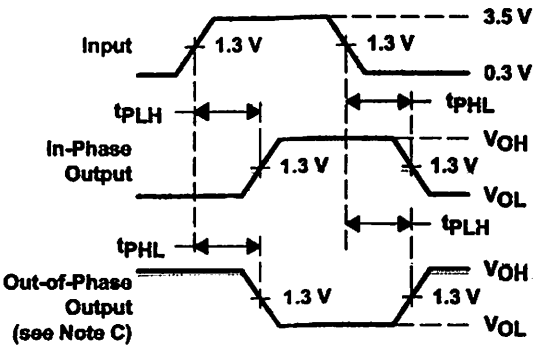
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS86
Quad 2-Input Exclusive-OR Gate

General Description

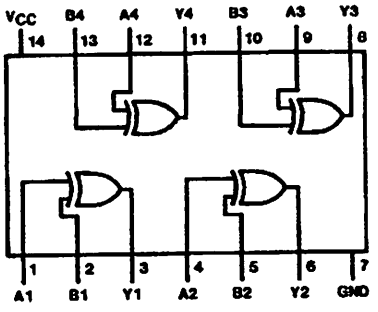
This device contains four independent gates each of which performs the logic exclusive-OR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS86M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS86SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS86N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.2	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			40	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max (Note 4)		6.1	10	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max (Note 5)		9	15	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CCH} is measured with all outputs OPEN, one input at each gate at 4.5V, and the other inputs grounded.

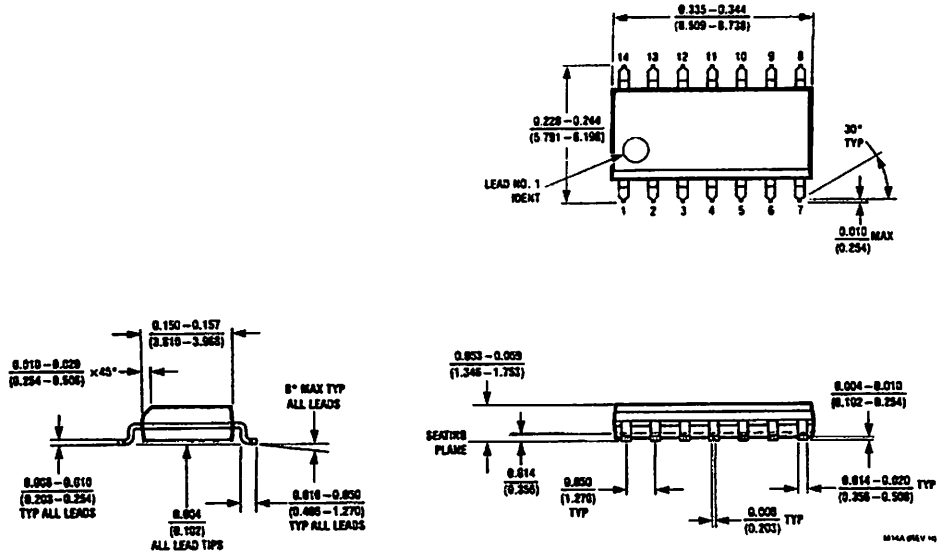
Note 5: I_{CCL} is measured with all outputs OPEN and all inputs grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

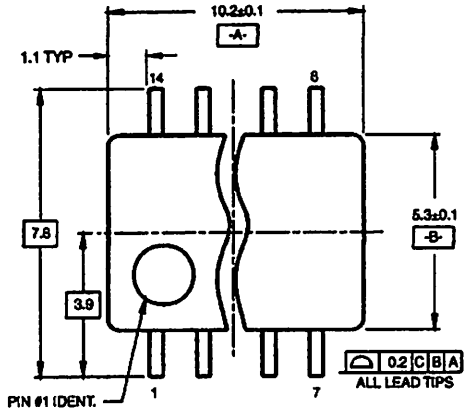
Symbol	Parameter	Conditions	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input Low		18		23	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			17		21	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input High		10		15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			12		15	ns

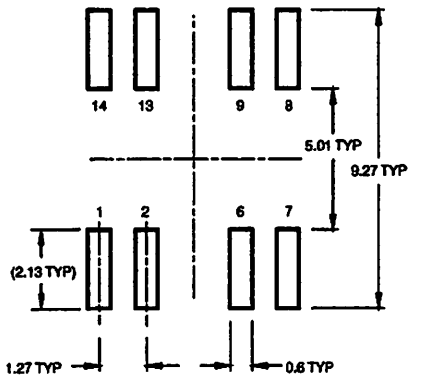
Physical Dimensions inches (millimeters) unless otherwise noted



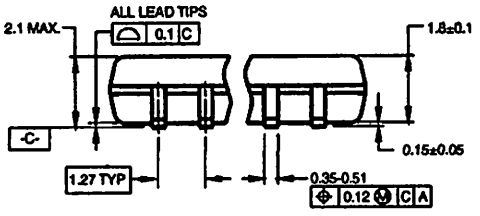
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

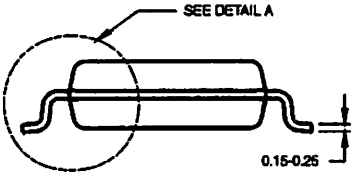
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





LAND PATTERN RECOMMENDATION





DIMENSIONS ARE IN MILLIMETERS

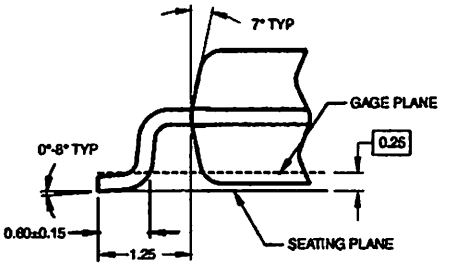
NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

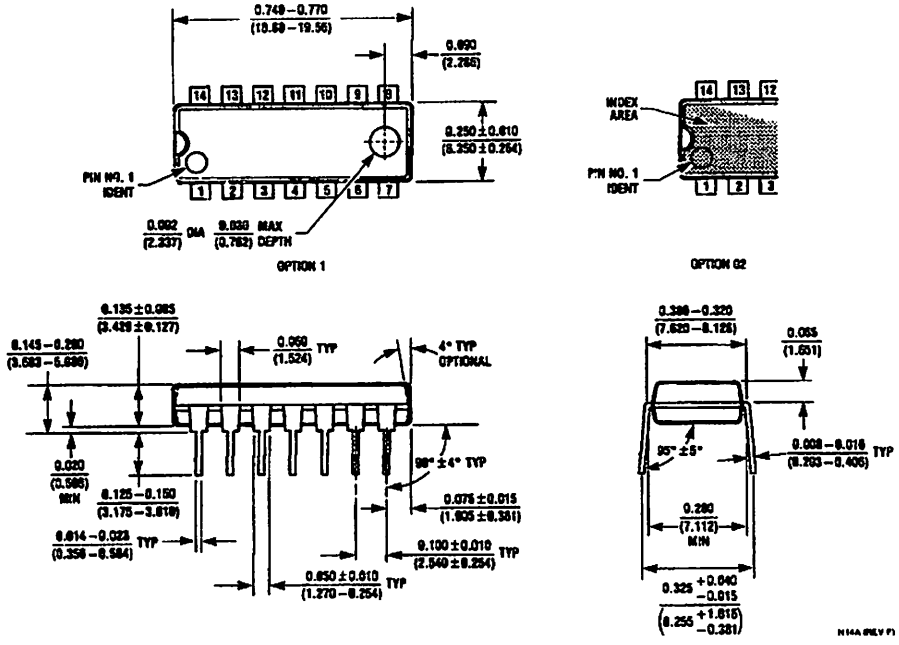
M14DRevB1



DETAIL A

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

HCF4060B

14-STAGE RIPPLE CARRY BINARY COUNTER/DIVIDER AND OSCILLATOR

- MEDIUM-SPEED OPERATION
- COMMON RESET
- FULLY STATIC OPERATION
- BUFFERED INPUTS AND OUTPUTS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

DIP SOP

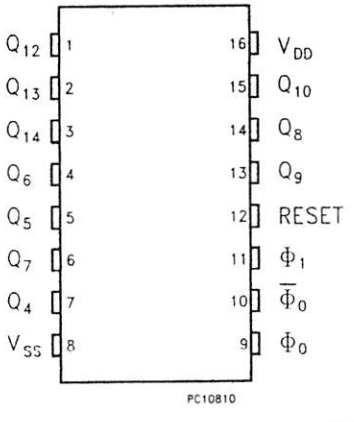
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4060BEY	
SOP	HCF4060BM1	HCF4060M013TR

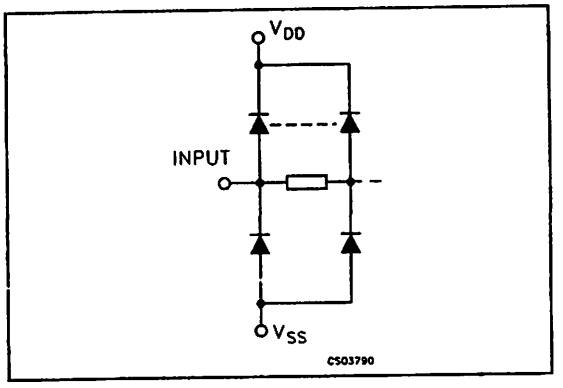
DESCRIPTION

The HCF4060B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
The HCF4060B consists of an oscillator section and 14 ripple carry binary counter stages.
The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which reset the counter to the all 0's state and disable oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕ_1 (and ϕ_0). All inputs and outputs are fully buffered. Schmitt trigger action on the clock pin permits unlimited clock rise and fall time.

PIN CONNECTION



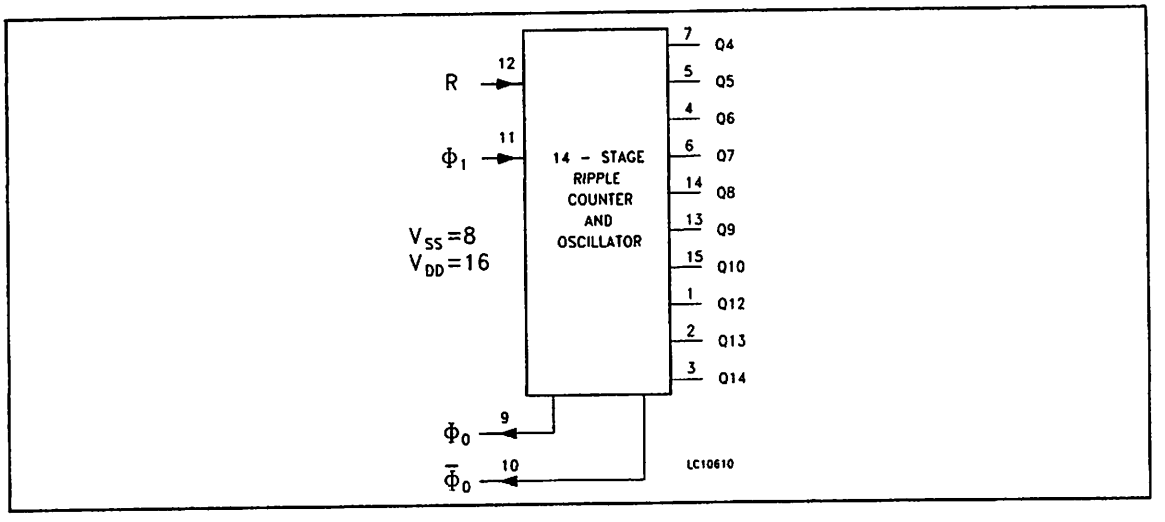
INPUT EQUIVALENT CIRCUIT



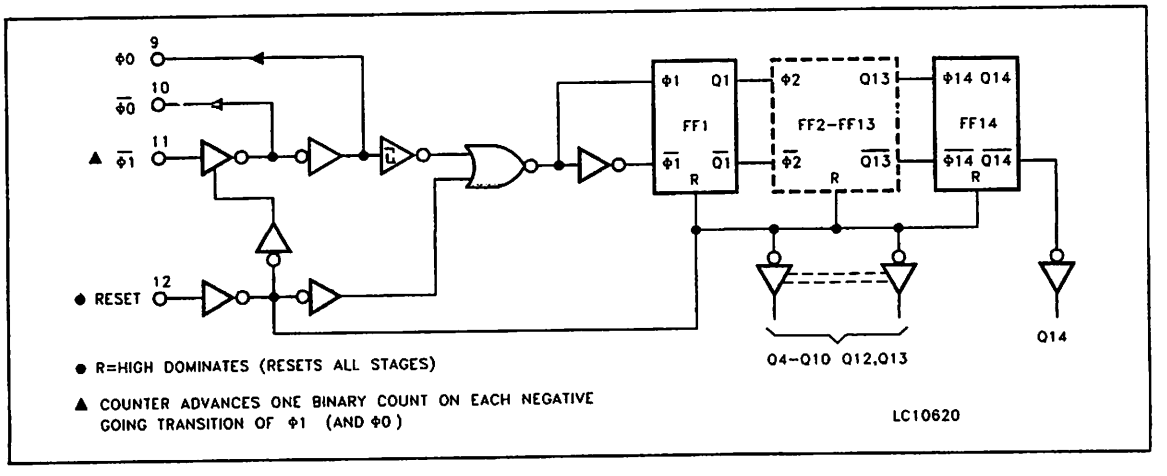
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 13, 14, 15	Q_{12}, Q_{13}, Q_{14}, Q_6, Q_5, Q_7, Q_4, Q_9, Q_8, Q_{10}	Outputs
9, 10, 11	Φ_0, $\bar{\Phi}_0$, Φ_1	Oscillator Input
12	RESET	Reset
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage tc the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (µA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		5		150	µA
		0/10			10		0.04	10		10		300	
		0/15			15		0.04	20		20		600	
		0/20			20		0.08	100		100		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.3		±0.3		±1	µA
C_I	Input Capacitance		Any Input				5	7.5					pF

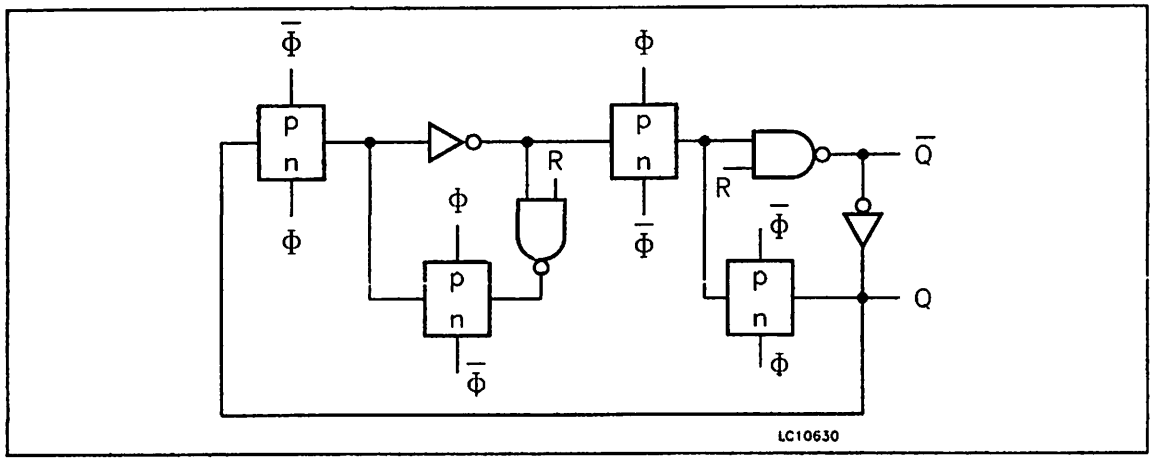
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

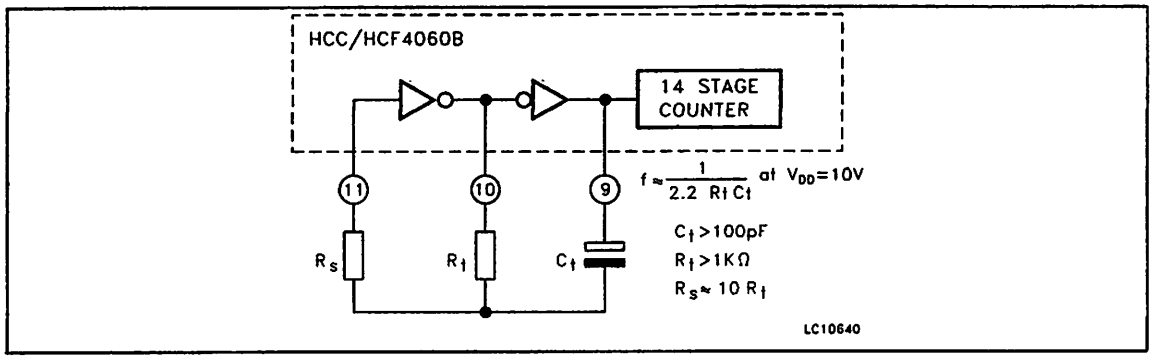
Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_{PLH} t_{PHL}	Propagation Delay Time (ϕ to Q_4 out)	5			370	740	ns
		10			150	300	
		15			100	200	
t_{PLH} t_{PHL}	Propagation Delay Time (Q_n to Q_{n+1})	5			100	200	ns
		10			50	100	
		15			40	80	
t_W	Input Pulse Width	5	f = 100 KHz		50	100	ns
		10			20	40	
		15			15	30	
t_r t_f	Input Pulse Rise and Fall Time	5		Unlimited			µs
		10					
		15					
f_{max}	Maximum Clock Input Frequency	5		3.5	7		MHz
		10		8	16		
		15		12	24		
RESET OPERATION							
t_{PHL}	Propagation Delay Time	5			180	360	ns
		10			80	160	
		15			50	100	
t_W	Input Pulse Width	5			60	120	ns
		10			30	60	
		15			20	40	
RC OPERATION							
	Variation of Frequency (Unit-to-Unit)	5	C_X= 200pF, R_S= 560KΩ, R_X= 50KΩ	18	21.5	25	KHz
		10		20	23	26	
		15		21.1	24	27	
	Variation of Frequency With Voltage Change (Same Unit)	5 to 10	C_X= 200pF, R_S= 560KΩ, R_X= 50KΩ			2	KHz
		10 to 15				1	
R_X		5	C_X= 10µF			20	MΩ
		10	C_X= 50µF			20	
		15	C_X= 10µF			10	
C_X		5	R_X= 500KΩ			1000	µF
		10	R_X= 300KΩ			50	
		15	R_X= 300KΩ			50	
	Maximum Oscillator Frequency (**)	10	R_X= 5KΩ, C_X= 15pF	530	650	810	KHz
		15		690	800	940	

(*) Typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times= 20 ns.
(**) RC Oscillator applications are not recommended at supply voltages below 7V for R_X < 50KΩ

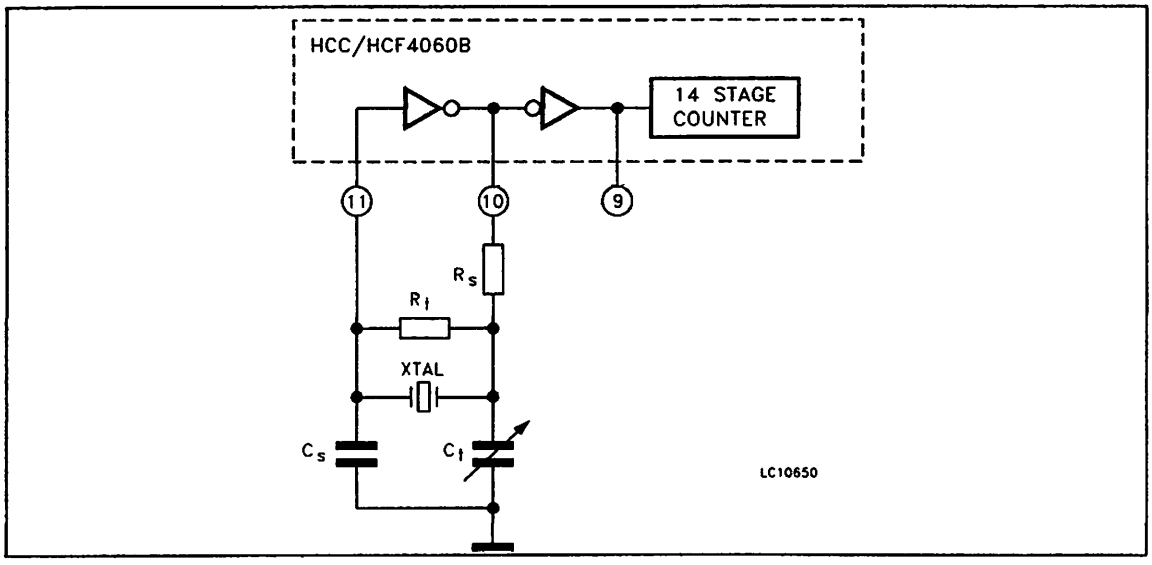
DETAIL OF TYPICAL FLIP-FLOP STAGE



TYPICAL RC OSCILLATOR CIRCUIT

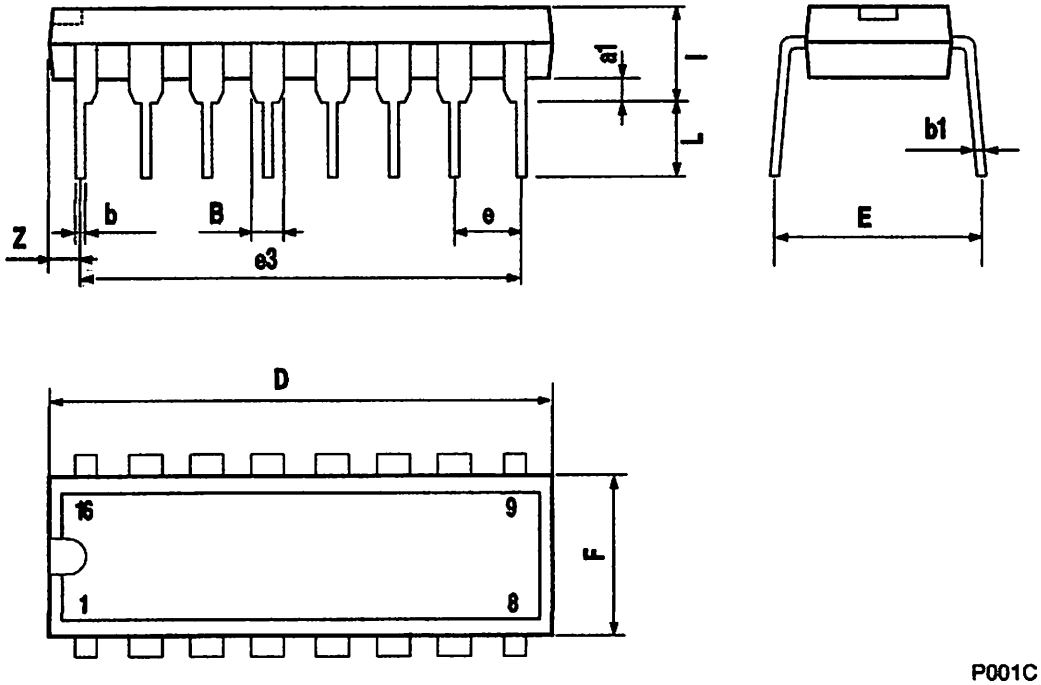


TYPICAL CRYSTAL OSCILLATOR CIRCUIT



Plastic DIP-16 (0.25) MECHANICAL DATA

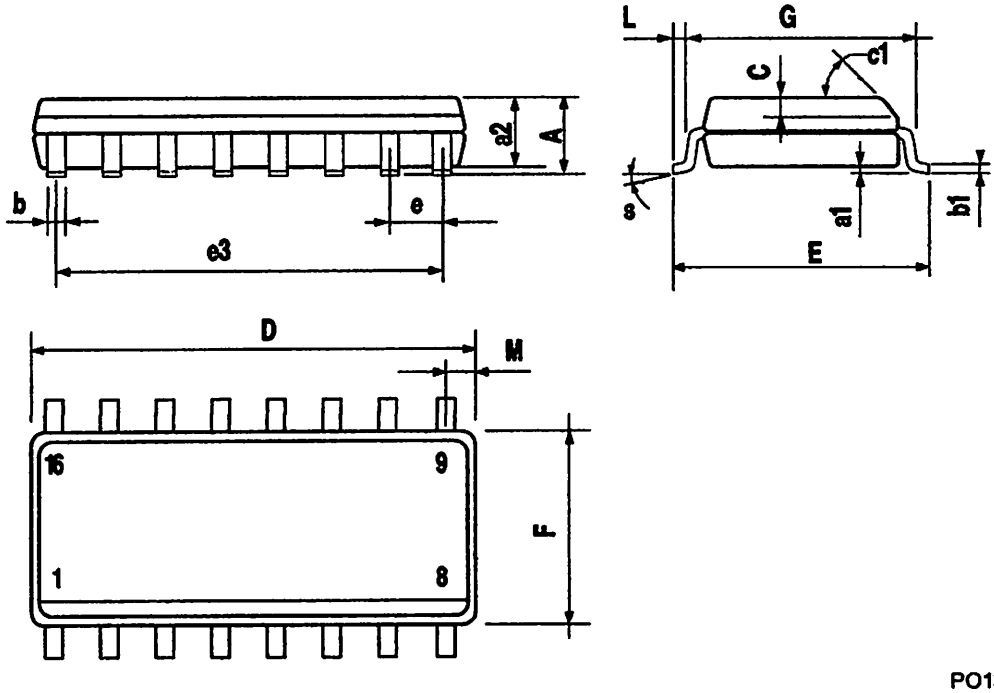
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

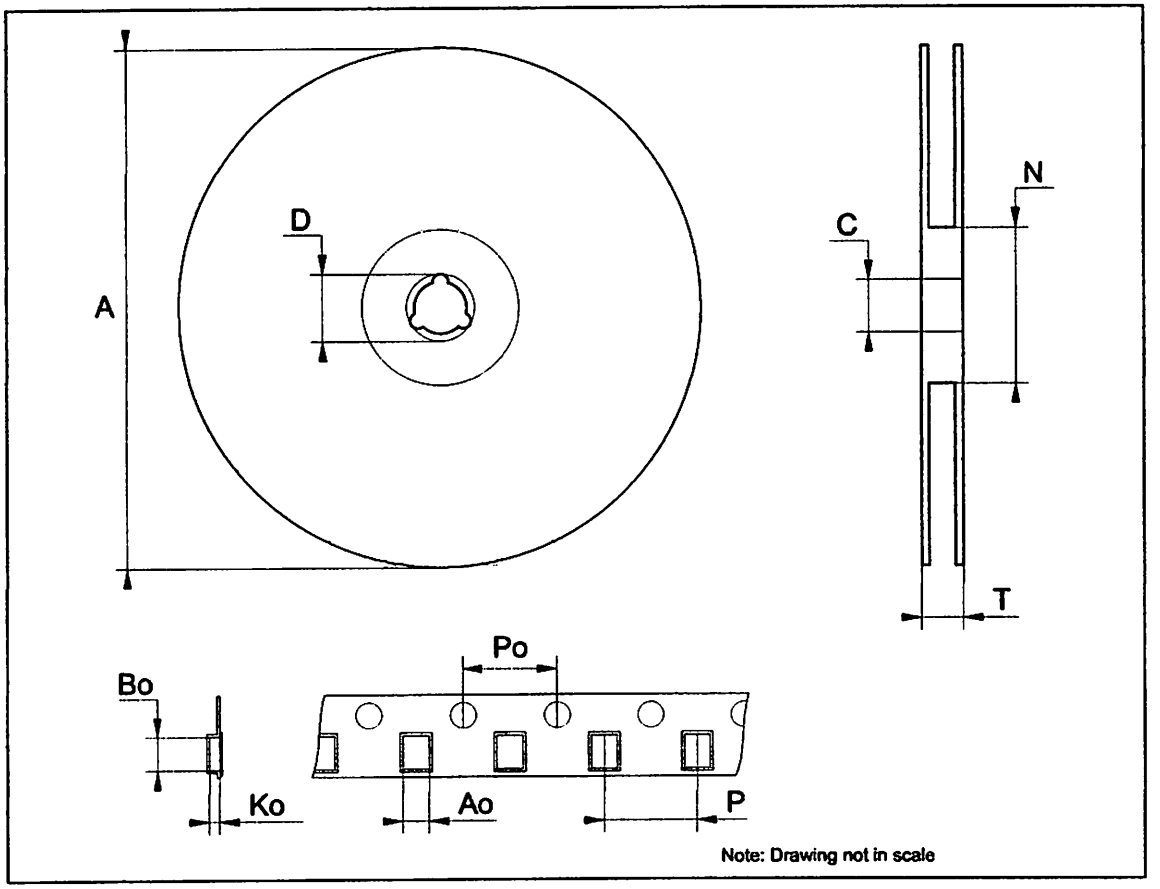
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.008
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8		° (max.)			



PO13H

Tape & Reel SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.45		6.65	0.254		0.262
Bo	10.3		10.5	0.406		0.414
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

MOTOROLA

SN54/74LS192
SN54/74LS193

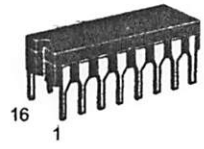
PRESETTABLE BCD/DECADE UP/DOWN COUNTER
PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

PRESETTABLE BCD/DECADE UP/DOWN COUNTER
PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER
LOW POWER SCHOTTKY

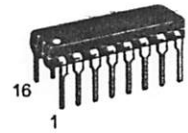
The SN54/74LS192 is an UP/DOWN BCD Decade (8421) Counter and the SN54/74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load (PL) and the Master Reset (MR) inputs asynchronously override the clocks.

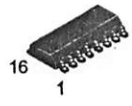
- Low Power . . . 95 mW Typical Dissipation
- High Speed . . . 40 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Master Reset and Parallel Load
- Individual Preset Inputs
- Cascading Circuitry Internally Provided
- Input Clamp Diodes Limit High Speed Termination Effects



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

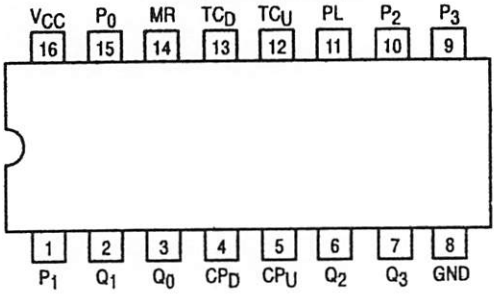


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

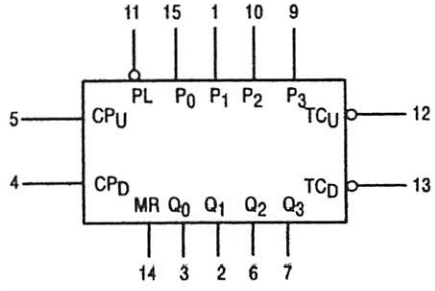
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC SYMBOL

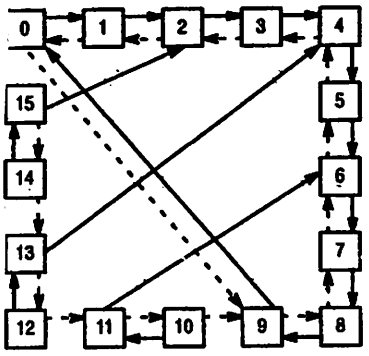


PIN NAMES

		LOADING (Note a) HIGH	LOW
CP_U	Count Up Clock Pulse Input	0.5 U.L.	0.25 U.L.
CP_D	Count Down Clock Pulse Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Asynchronous Master Reset (Clear) Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input	0.5 U.L.	0.25 U.L.
P_n	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_n	Flip-Flop Outputs (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Note b)	10 U.L.	5 (2.5) U.L.
TC_U	Terminal Count Up (Carry) Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

TATE DIAGRAMS



LS192

LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC_U} = Q_0 \cdot Q_3 \cdot \overline{CP_U}$

$TC_D = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CP_D$

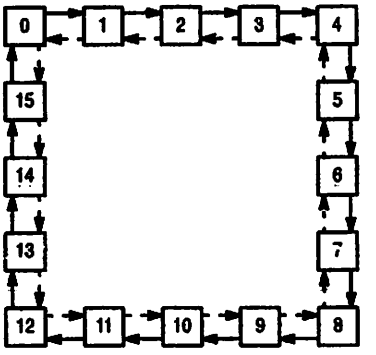
LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC_U} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP_U}$

$TC_D = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CP_D$

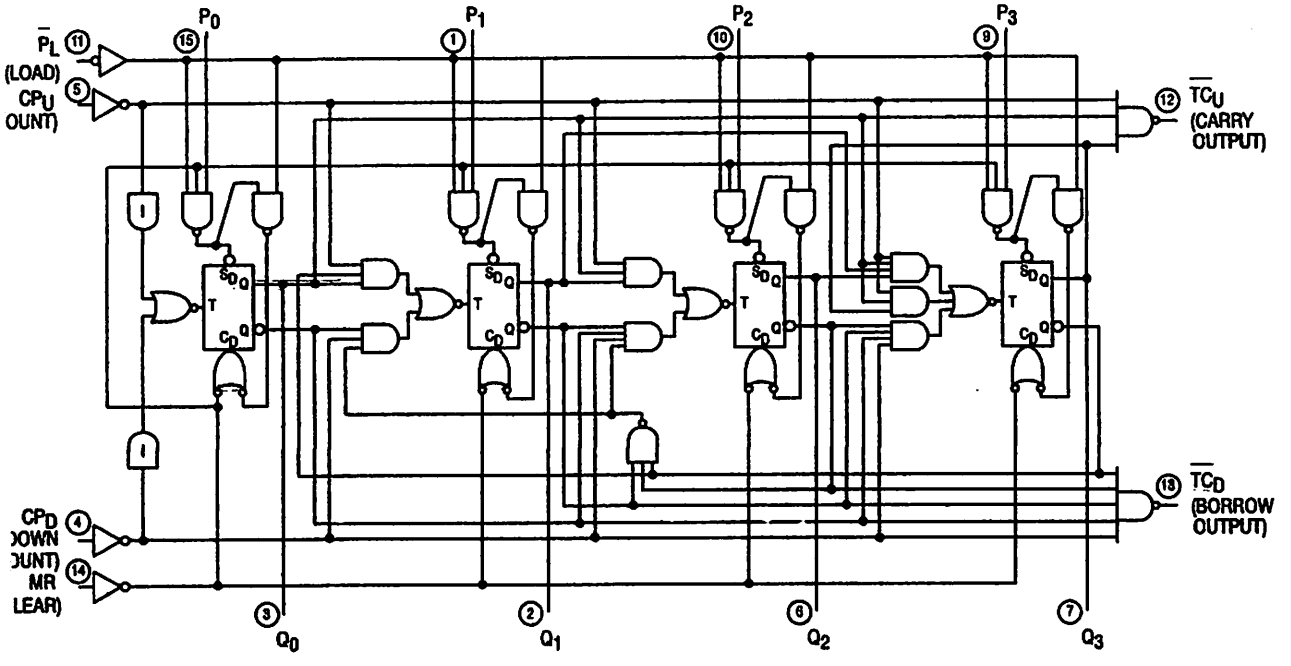
COUNT UP ——————

COUNT DOWN - - - - - -



LS193

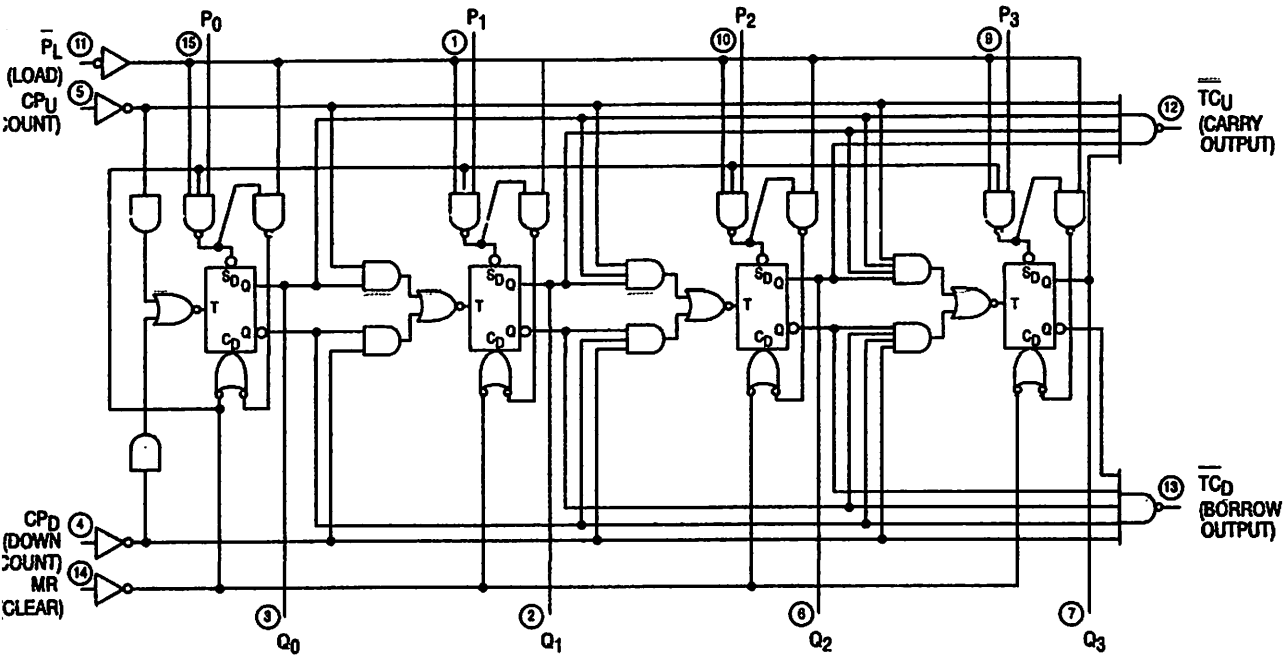
GIC DIAGRAMS



LS192

C = PIN 16
D = PIN 8
= PIN NUMBERS

)GIC DIAGRAMS (continued)



LS193

V_{CC} = PIN 16
GND = PIN 8
◯ = PIN NUMBERS

ICTIONAL DESCRIPTION

ıe LS192 and LS193 are Asynchronously Presettable ade and 4-Bit Binary Synchronous UP/DOWN (Revers-) Counters. The operating modes of the LS192 decade nter and the LS193 binary counter are identical, with the / difference being the count sequences as noted in the te Diagrams. Each circuit contains four master/slave flops, with internal gating and steering logic to provide ster reset, individual preset, count up and count down ırations.

ach flip-flop contains JK feedback from slave to master h that a LOW-to-HIGH transition on its T input causes the ıe, and thus the Q output to change state. Synchronous tching, as opposed to ripple counting, is achieved by ing the steering gates of all stages from a common Count line and a common Count Down line, thereby causing all te changes to be initiated simultaneously. A LOW-to-HIGH ısition on the Count Up input will advance the count by one; imilar transition on the Count Down input will decrease the int by one. While counting with one clock input, the other ould be held HIGH. Otherwise, the circuit will either count by ıs or not at all, depending on the state of the first flip-flop, ich cannot toggle as long as either Clock input is LOW.

The Terminal Count Up ($\overline{TC_U}$) and Terminal Count Down (TC_D) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the LS192, 15 for the LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause TC_U to go LOW. TC_U will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the TC_D output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load (PL) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⎍ = LOW-to-HIGH Clock Transition

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				34	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	25	32		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	$\overline{CP_U}$ Input to TC_U Output		17 18	26 24	ns	
t_{PLH} t_{PHL}	$\overline{CP_D}$ Input to TC_D Output		16 15	24 24	ns	
t_{PLH} t_{PHL}	Clock to Q		27 30	38 47	ns	
t_{PLH} t_{PHL}	$\overline{PL}$ to Q		24 25	40 40	ns	
t_{PHL}	MR Input to Any Output		23	35	ns	

SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
	Any Pulse Width	20			ns	V_{CC} = 5.0 V
	Data Setup Time	20			ns	
	Data Hold Time	5.0			ns	
	Recovery Time	40			ns	

FINITIONS OF TERMS

TUP TIME (t_s) is defined as the minimum time required for correct logic level to be present at the logic input prior to the ransition from LOW-to-HIGH in order to be recognized and nsferred to the outputs.

LD TIME (t_h) is defined as the minimum time following the transition from LOW-to-HIGH that the logic level must be ntained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the PL transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

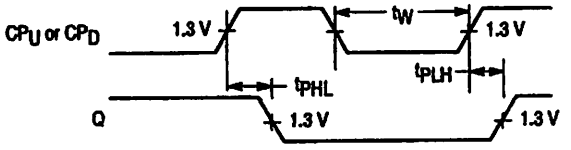


Figure 1

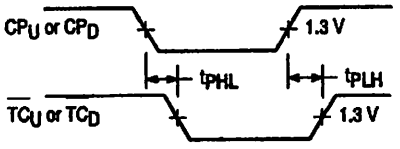
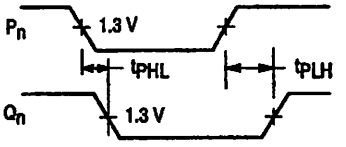


Figure 2



NOTE: $\overline{PL}$ = LOW

Figure 3

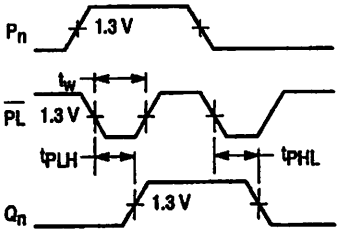


Figure 4

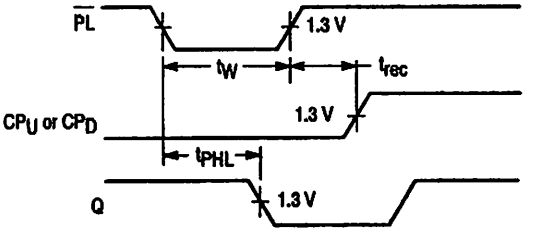
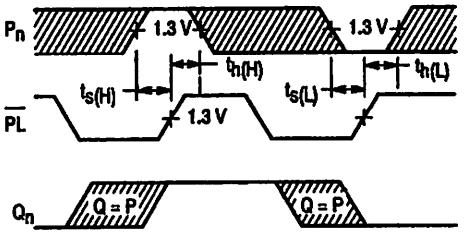


Figure 5



* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 6

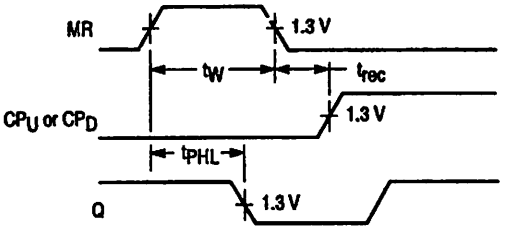
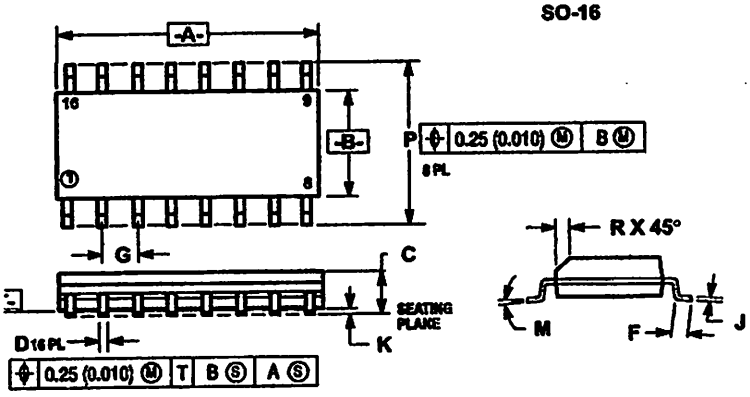


Figure 7

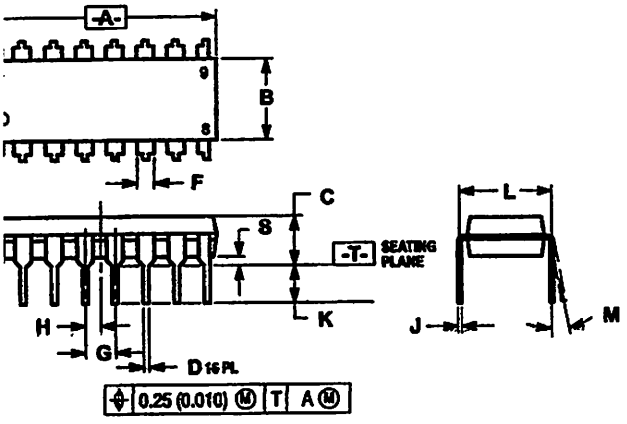
Case 751B-03 D Suffix
16-Pin Plastic
SO-16



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

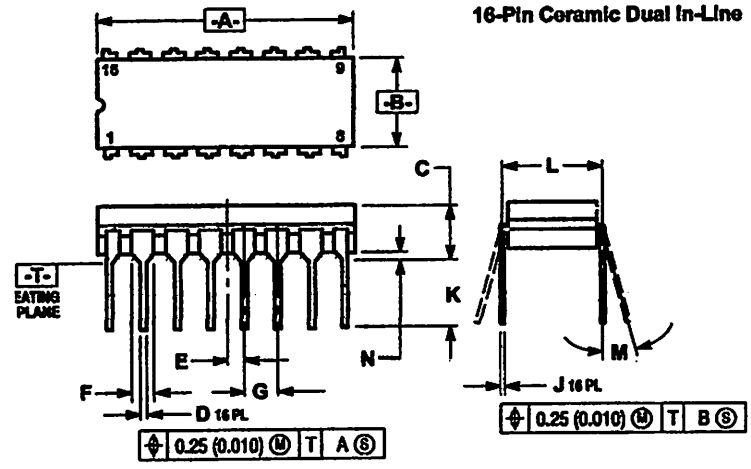
Case 648-08 N Suffix
16-Pin Plastic



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

Case 620-09 J Suffix
16-Pin Ceramic Dual In-Line



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

MC54/74HC595A

-Bit Serial-Input/Serial or arallel-Output Shift Register ith Latched 3-State Outputs

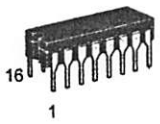
gh–Performance Silicon–Gate CMOS

The MC54/74HC595A is identical in pinout to the LS595. The device uts are compatible with standard CMOS outputs; with pullup resistors, y are compatible with LSTTL outputs.

The HC595A consists of an 8–bit shift register and an 8–bit D–type latch n three–state parallel outputs. The shift register accepts serial data and vides a serial output. The shift register also provides parallel data to the bit latch. The shift register and latch have independent clock inputs. This vice also has an asynchronous reset for the shift register.

The HC595A directly interfaces with the Motorola SPI serial data port on IOS MPUs and MCUs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- Improvements over HC595
  - — Improved Propagation Delays
  - — 50% Lower Quiescent Power
  - — Improved Input Noise and Latchup Immunity



J SUFFIX
CERAMIC PACKAGE
CASE 620–10

N SUFFIX
PLASTIC PACKAGE
CASE 648–08

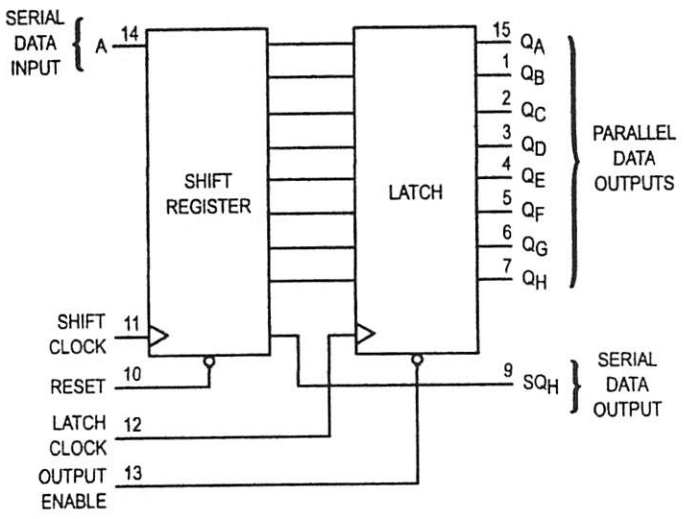
D SUFFIX
SOIC PACKAGE
CASE 751B–05

DT SUFFIX
TSSOP PACKAGE
CASE 948F–01

ORDERING INFORMATION

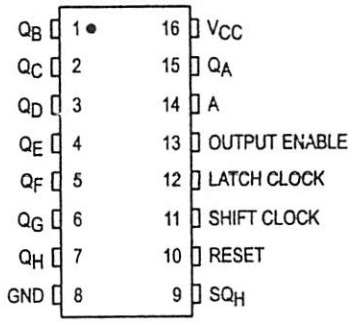
MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXAD	SOIC
MC74HCXXXADT	TSSOP

LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8

PIN ASSIGNMENT



MOTOROLA

(IMUM RATINGS*

nbol	Parameter	Value	Unit
:C	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
'in	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
out	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
in	DC Input Current, per Pin	± 20	mA
ut	DC Output Current, per Pin	± 35	mA
:C	DC Supply Current, V_{CC} and GND Pins	± 75	mA
D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
	TSSOP Package†	450	
stg	Storage Temperature	– 65 to + 150	°C
L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	°C
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

ximum Ratings are those values beyond which damage to the device may occur.
ictional operation should be restricted to the Recommended Operating Conditions.
rating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

COMMENDED OPERATING CONDITIONS

mbol	Parameter		Min	Max	Unit
CC	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
, Vout	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
TA	Operating Temperature, All Package Types		– 55	+ 125	°C
r, tf	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

mbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
IH	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V, $\|I_{out}\|$ ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
IL	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V, $\|I_{out}\|$ ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
OH	Minimum High–Level Output Voltage, Q_A – Q_H	V_{in} = V_{IH} or V_{IL}, $\|I_{out}\|$ ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in} = V_{IH} or V_{IL}, $\|I_{out}\|$ ≤ 6.0 mA	4.5	3.98	3.84	3.7	
		$\|I_{out}\|$ ≤ 7.8 mA	6.0	5.48	5.34	5.2	
OL	Maximum Low–Level Output Voltage, Q_A – Q_H	V_{in} = V_{IH} or V_{IL}, $\|I_{out}\|$ ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in} = V_{IH} or V_{IL}, $\|I_{out}\|$ ≤ 6.0 mA	4.5	0.26	0.33	0.4	
		$\|I_{out}\|$ ≤ 7.8 mA	6.0	0.26	0.33	0.4	

E: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

ELECTRICAL CHARACTERISTICS (Continued)

ymbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OH}	Minimum High–Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage, SQ_H	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three–State Leakage Current, $Q_A - Q_H$	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA	6.0	4.0	40	160	μA

ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

ymbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
PLH, PHL	Maximum Propagation Delay, Shift Clock to SQ_H (Figures 1 and 7)	2.0 4.5 6.0	140 28 24	175 35 30	210 42 36	ns
PHL	Maximum Propagation Delay, Reset to SQ_H (Figures 2 and 7)	2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	ns
PLH, PHL	Maximum Propagation Delay, Latch Clock to $Q_A - Q_H$ (Figures 3 and 7)	2.0 4.5 6.0	140 28 24	175 35 30	210 42 36	ns
PLZ, PHZ	Maximum Propagation Delay, Output Enable to $Q_A - Q_H$ (Figures 4 and 8)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
PZL, PZH	Maximum Propagation Delay, Output Enable to $Q_A - Q_H$ (Figures 4 and 8)	2.0 4.5 6.0	135 27 23	170 34 29	205 41 35	ns
TLH, THL	Maximum Output Transition Time, $Q_A - Q_H$ (Figures 3 and 7)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
TLH, THL	Maximum Output Transition Time, SQ_H (Figures 1 and 7)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance	—	10	10	10	pF
Cout	Maximum Three–State Output Capacitance (Output in High–Impedance State), $Q_A - Q_H$	—	15	15	15	pF

E: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, $V_{CC} = 5.0$ V	
CPD	Power Dissipation Capacitance (Per Package)*	300	pF

ed to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the torola High–Speed CMOS Data Book (DL129/D).

REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

ol	Parameter	V_{CC} V	Guaranteed Limit 25°C to −55°C	≤ 85°C	≤ 125°C	Unit
	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0 4.5 6.0	50 10 9.0	65 13 11	75 15 13	ns
	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0 4.5 6.0	5.0 5.0 5.0	5.0 5.0 5.0	5.0 5.0 5.0	ns
	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0 4.5 6.0	50 10 9.0	65 13 11	75 15 13	ns
	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
	Minimum Pulse Width, Shift Clock (Figure 1)	2.0 4.5 6.0	50 10 9.0	65 13 11	75 15 13	ns
	Minimum Pulse Width, Latch Clock (Figure 6)	2.0 4.5 6.0	50 10 9.0	65 13 11	75 15 13	ns
	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

FUNCTION TABLE

peration	Inputs Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Resulting Function Shift Register Contents	Latch Register Contents	Serial Output SQ_H	Parallel Outputs $Q_A - Q_H$
ft register	L	X	X	L, H, ↘	L	L	U	L	U
into shift	H	D	↗	L, H, ↘	L	$D \rightarrow SR_A$; $SR_N \rightarrow SR_{N+1}$	U	$SR_G \rightarrow SR_H$	U
ter remains d	H	X	L, H, ↘	L, H, ↘	L	U	U	U	U
hift register latch register	H	X	L, H, ↘	↗	L	U	$SR_N \rightarrow LR_N$	U	SR_N
ster remains	X	X	X	L, H, ↘	L	*	U	*	U
allel outputs	X	X	X	X	L	*	**	*	Enabled
uts into high state	X	X	X	X	H	*	**	*	Z

egister contents
egister contents

D = data (L, H) logic level
U = remains unchanged
X = don't care
Z = high impedance
* = depends on Reset and Shift Clock inputs
** = depends on Latch Clock input

PIN DESCRIPTIONS

ITS

In 14)

rial Data Input. The data on this pin is shifted into the t serial shift register.

ITROL INPUTS

t Clock (Pin 11)

ift Register Clock Input. A low– to–high transition on this t causes the data at the Serial Input pin to be shifted into }–bit shift register.

et (Pin 10)

tive–low, Asynchronous, Shift Register Reset Input. A on this pin resets the shift register portion of this device . The 8–bit latch is not affected.

Latch Clock (Pin 12)

Storage Latch Clock Input. A low–to–high transition on this input latches the shift register data.

Output Enable (Pin 13)

Active–low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs (Q_A–Q_H) into the high–impedance state. The serial output is not affected by this control unit.

OUTPUTS

Q_A – Q_H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Noninverted, 3–state, latch outputs.

SQ_H (Pin 9)

Noninverted, Serial Data Output. This is the output of the eighth stage of the 8–bit shift register. This output does not have three–state capability.

SWITCHING WAVEFORMS

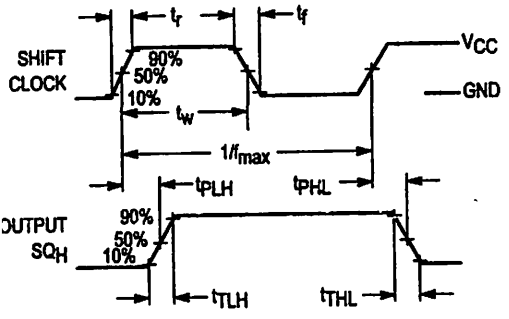


Figure 1.

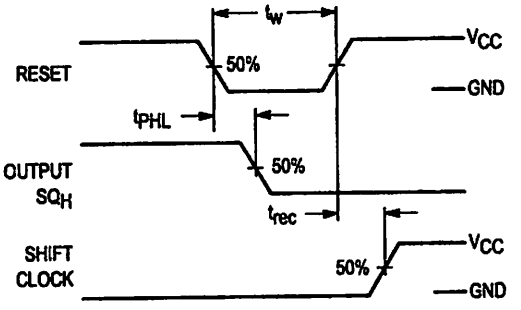


Figure 2.

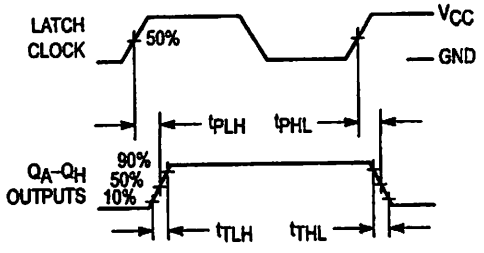


Figure 3.

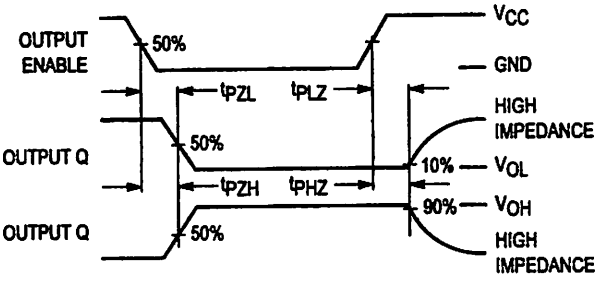


Figure 4.

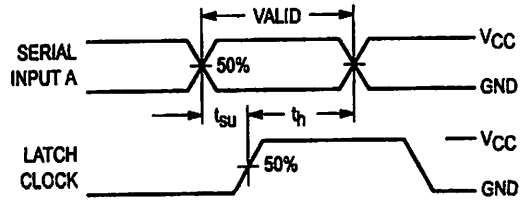


Figure 5.

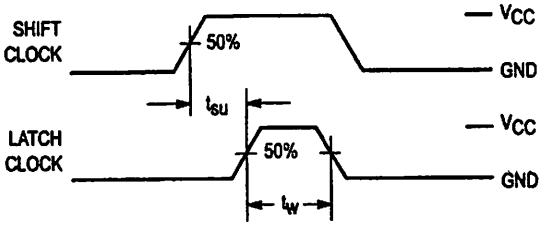
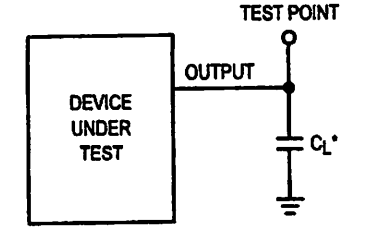


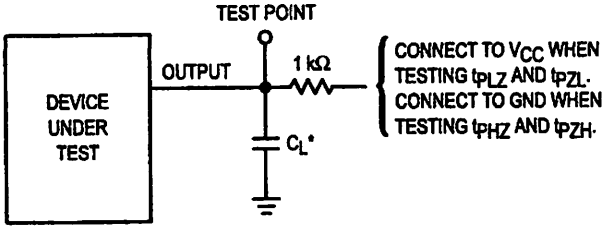
Figure 6.

TEST CIRCUITS



* Includes all probe and jig capacitance

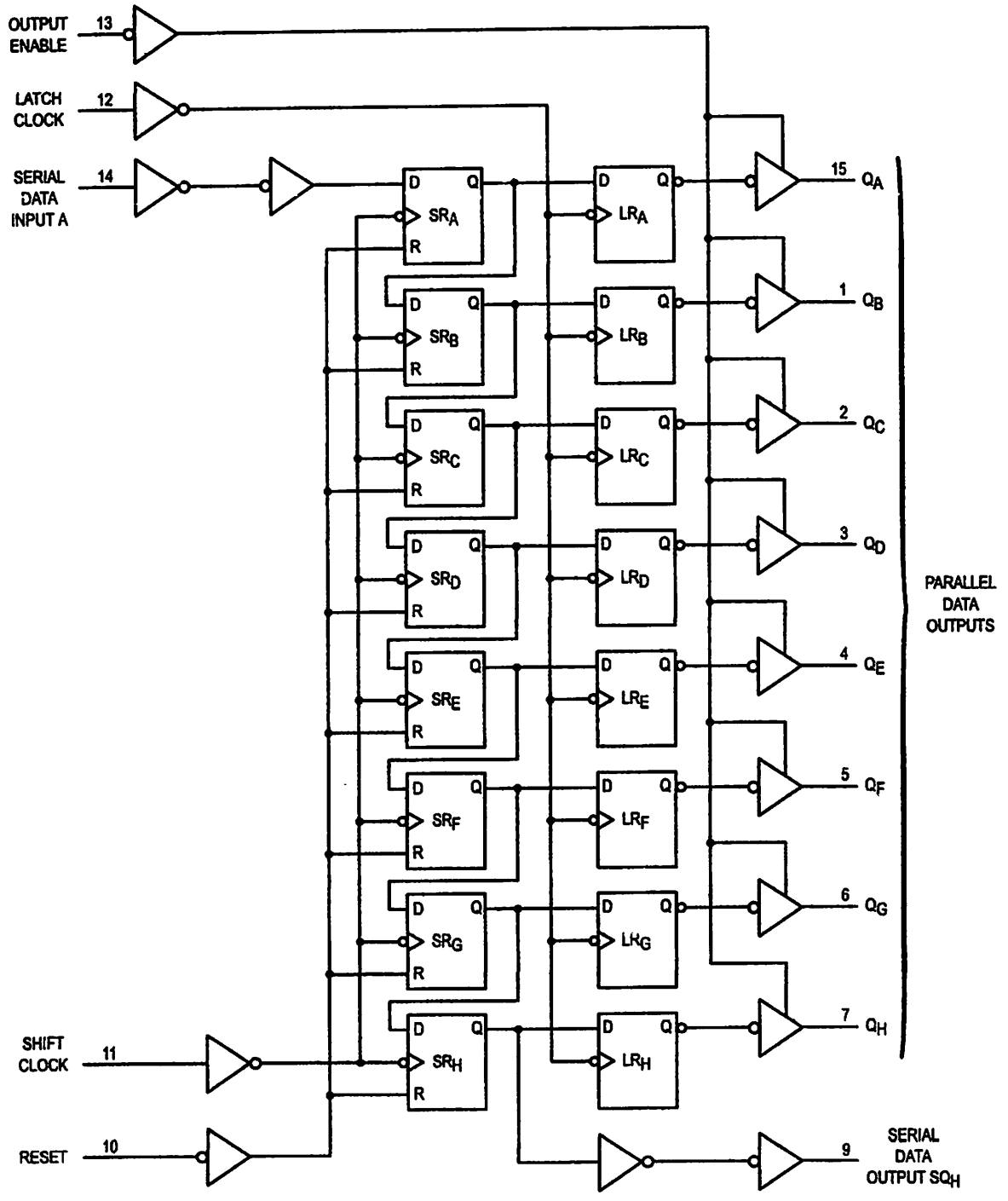
Figure 7.



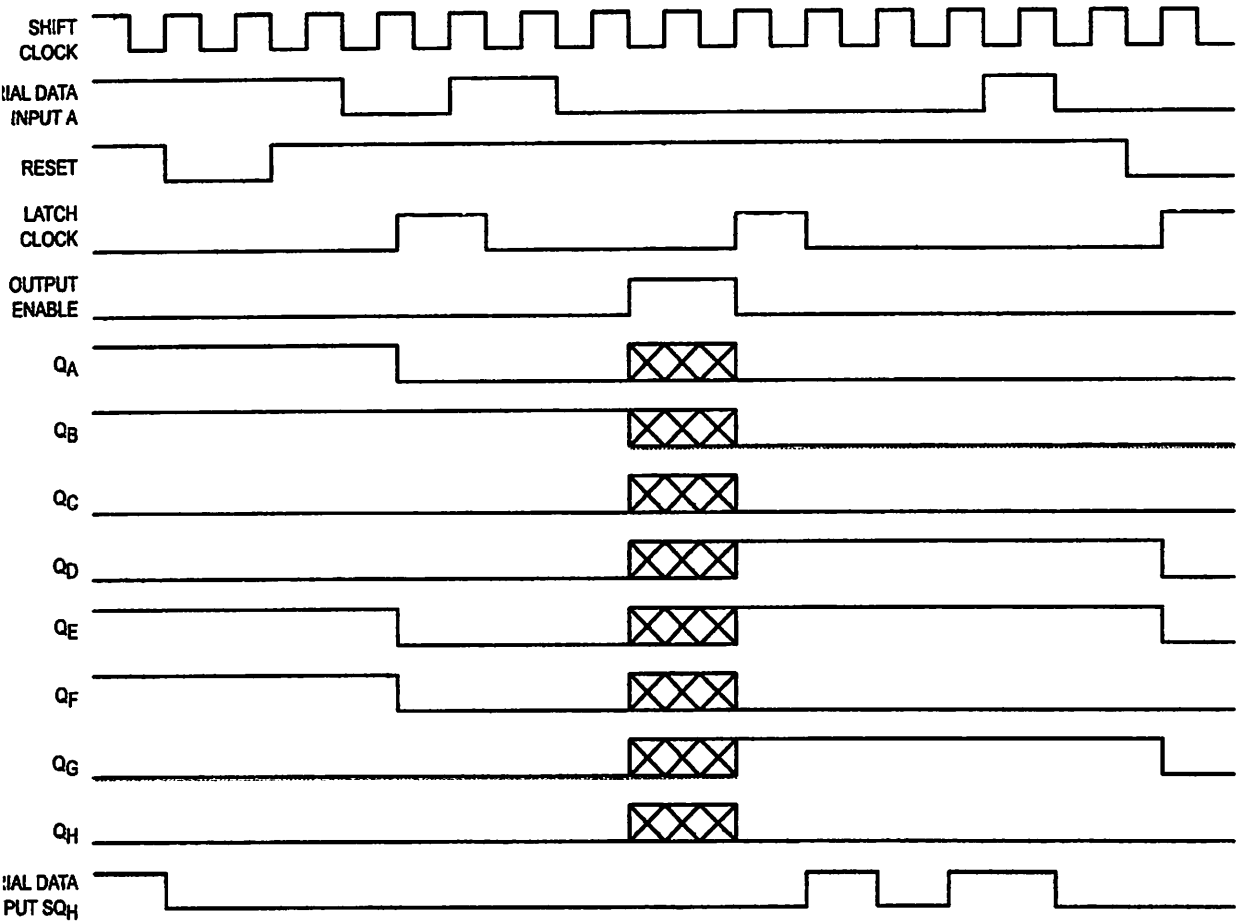
* Includes all probe and jig capacitance

Figure 8.

EXPANDED LOGIC DIAGRAM



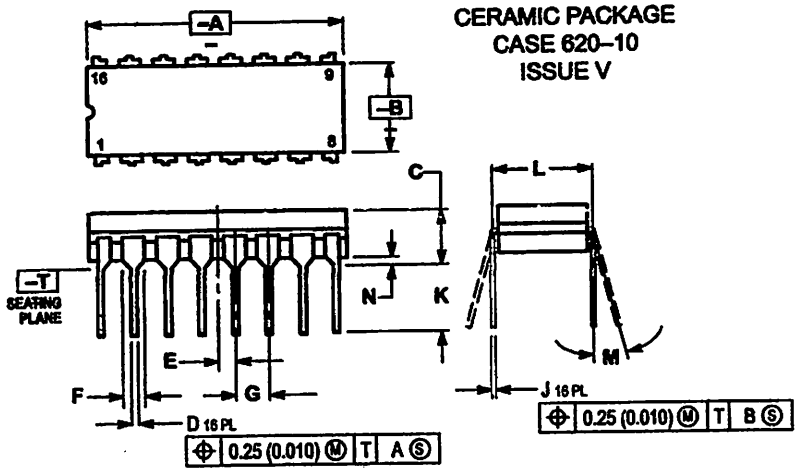
TIMING DIAGRAM



NOTE: ⊠ implies that the output is in a high–impedance state.

OUTLINE DIMENSIONS

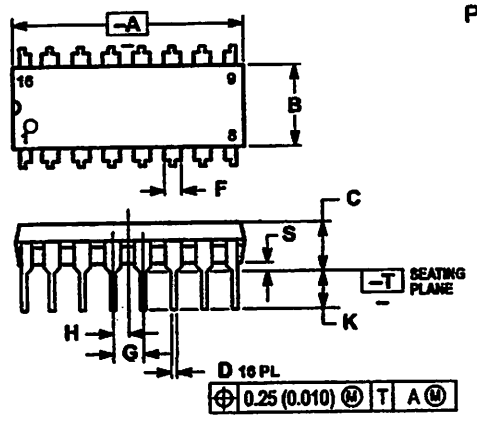
J SUFFIX
CERAMIC PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

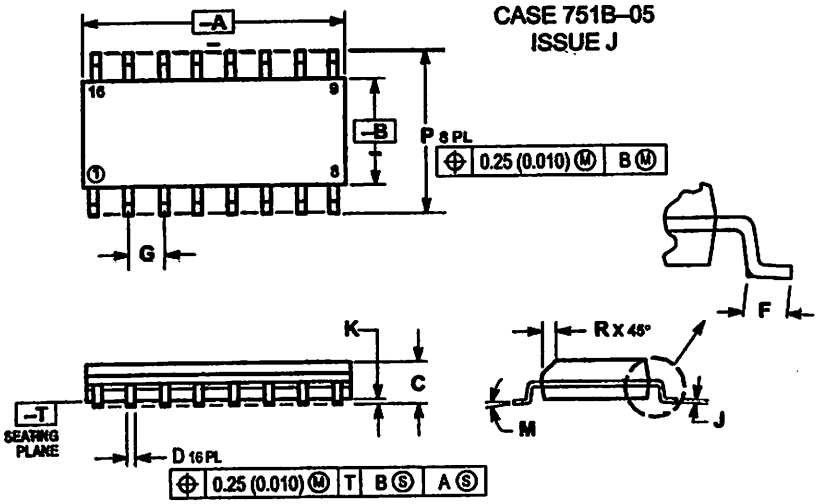
N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

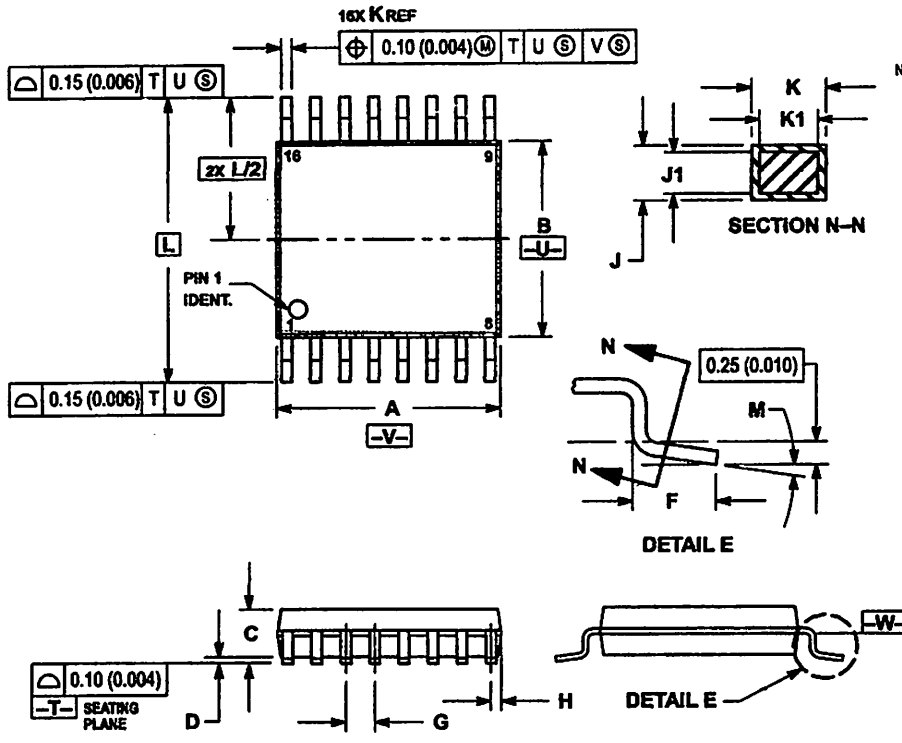


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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PIC16F84A
Data Sheet

18-pin Enhanced FLASH/EEPROM
8-bit Microcontroller

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable".
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

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MICROCHIP

PIC16F84A

18-pin *Enhanced* FLASH/EEPROM 8-Bit Microcontroller

gh Performance RISC CPU Features:

- nly 35 single word instructions to learn
- ll instructions single-cycle except for program ranches which are two-cycle
- perating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- 024 words of program memory
- 8 bytes of Data RAM
- 4 bytes of Data EEPROM
- 4-bit wide instruction words
- -bit wide data bytes
- 5 Special Function Hardware registers
- ight-level deep hardware stack
- irect, indirect and relative addressing modes
- our interrupt sources:
  - External RB0/INT pin
  - TMR0 timer overflow
  - PORTB<7:4> interrupt-on-change
  - Data EEPROM write complete

ripheral Features:

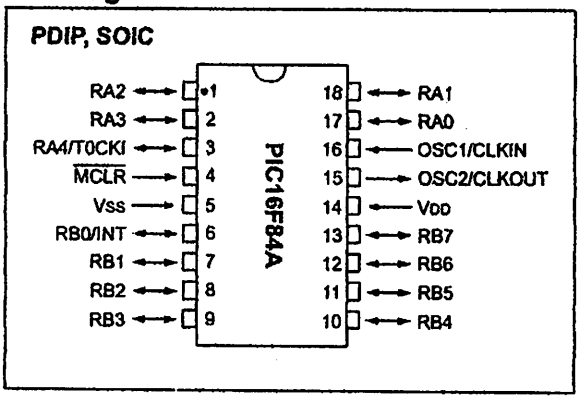
- 3 I/O pins with individual direction control
- igh current sink/source for direct LED drive
  - 25 mA sink max. per pin
  - 25 mA source max. per pin
- MR0: 8-bit timer/counter with 8-bit ogrammable prescaler

cial Microcontroller Features:

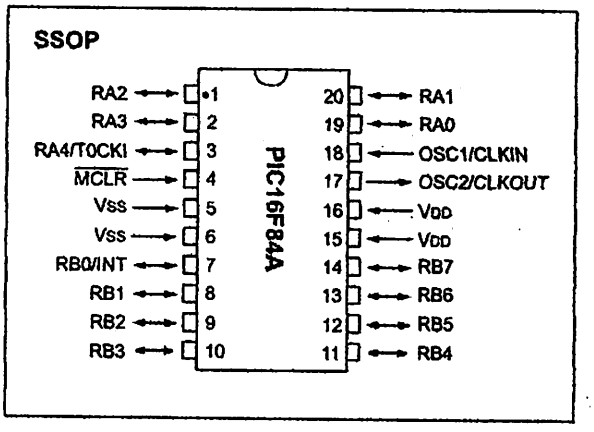
- ',000 erase/write cycles *Enhanced* FLASH ogram memory typical
- ,000,000 typical erase/write cycles EEPROM ta memory typical
- EPROM Data Retention > 40 years
- Circuit Serial Programming™ (ICSP™) - via o pins
- wer-on Reset (POR), Power-up Timer (PWRT), scillator Start-up Timer (OST)
- atchdog Timer (WDT) with its own On-Chip RC scillator for reliable operation
- de protection
- wer saving SLEEP mode
- lectable oscillator options

Pin Diagrams

PDIP, SOIC



SSOP



CMOS Enhanced FLASH/EEPROM Technology:

- Low power, high speed technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.0V to 5.5V
  - Industrial: 2.0V to 5.5V
- Low power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 15 µA typical @ 2V, 32 kHz
  - < 0.5 µA typical standby current @ 2V

Table of Contents

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DEVICE OVERVIEW

document contains device specific information for operation of the PIC16F84A device. Additional mation may be found in the PICmicro™ Mid-ge Reference Manual, (DS33023), which may be nloaded from the Microchip website. The Refer- Manual should be considered a complementary ment to this data sheet, and is highly recom- ded reading for a better understanding of the e architecture and operation of the peripheral iles.

PIC16F84A belongs to the mid-range family of the licro® microcontroller devices. A block diagram of evice is shown in Figure 1-1.

The program memory contains 1K words, which translates to 1024 instructions, since each 14-bit program memory word is the same width as each device instruction. The data memory (RAM) contains 68 bytes. Data EEPROM is 64 bytes.

There are also 13 I/O pins that are user-configured on a pin-to-pin basis. Some pins are multiplexed with other device functions. These functions include:

- External interrupt
- Change on PORTB interrupt
- Timer0 clock input

Table 1-1 details the pinout of the device with descriptions and details for each pin.

RE 1-1: PIC16F84A BLOCK DIAGRAM

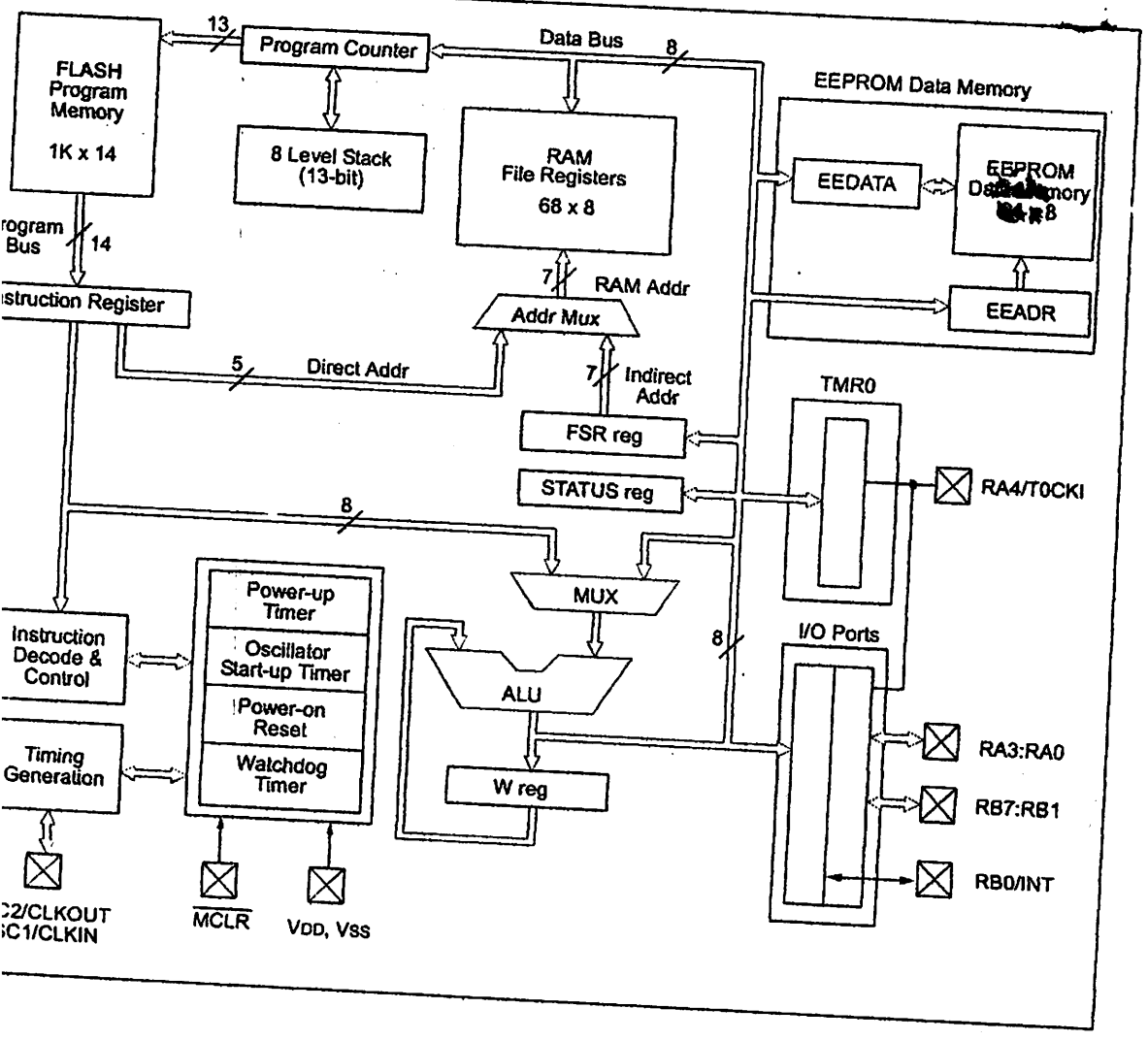


TABLE 1-1: PIC16F84A PINOUT DESCRIPTION

Pin Name	PDIP No.	SOIC No.	SSOP No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	18	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	19	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
MCLR	4	4	4	I/P	ST	Master Clear (Reset) input/programming voltage input. This pin is an active low RESET to the device.
						PORTA is a bi-directional I/O port.
RA0	17	17	19	I/O	TTL	
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RA4/T0CKI	3	3	3	I/O	ST	Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	7	I/O	TTL/ST(1)	RB0/INT can also be selected as an external interrupt pin.
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	Interrupt-on-change pin.
RB5	11	11	12	I/O	TTL	Interrupt-on-change pin.
RB6	12	12	13	I/O	TTL/ST(2)	Interrupt-on-change pin. Serial programming clock.
RB7	13	13	14	I/O	TTL/ST(2)	Interrupt-on-change pin. Serial programming data.
VSS	5	5	5,6	P	—	Ground reference for logic and I/O pins.
VDD	14	14	15,16	P	—	Positive supply for logic and I/O pins.

Legend: I= input O = Output I/O = Input/Output P = Power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

0 MEMORY ORGANIZATION

ere are two memory blocks in the PIC16F84A. ese are the program memory and the data memory. ch block has its own bus, so that access to each ck can occur during the same oscillator cycle.

e data memory can further be broken down into the neral purpose RAM and the Special Function gisters (SFRs). The operation of the SFRs that trol the "core" are described here. The SFRs used ontrol the peripheral modules are described in the tion discussing each individual peripheral module.

data memory area also contains the data ROM memory. This memory is not directly mapped the data memory, but is indirectly mapped. That is, ndirect address pointer specifies the address of the EEPROM memory to read/write. The 64 bytes of EEPROM memory have the address range Fh. More details on the EEPROM memory can be d in Section 3.0.

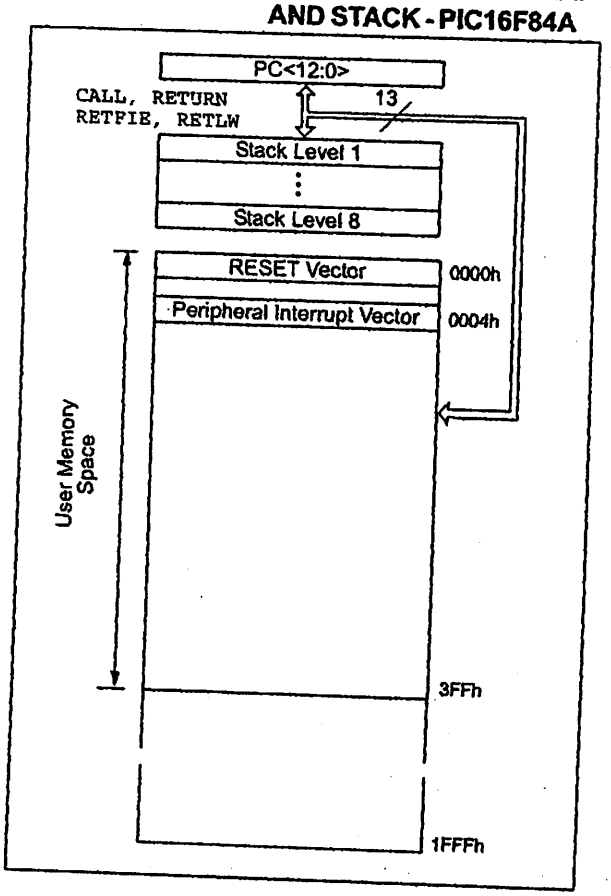
itional information on device memory may be found he PICmicro™ Mid-Range Reference Manual, 33023).

Program Memory Organization

PIC16FXX has a 13-bit program counter capable dressing an 8K x 14 program memory space. For IC16F84A, the first 1K x 14 (0000h-03FFh) are ically implemented (Figure 2-1). Accessing a loca- above the physically implemented address will a wraparound. For example, for locations 20h, 820h, C20h, 1020h, 1420h, 1820h, and 1C20h, struction will be the same.

ESET vector is at 0000h and the interrupt vector 004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK - PIC16F84A



2.2 Data Memory Organization

The data memory is partitioned into two areas. The first is the Special Function Registers (SFR) area, while the second is the General Purpose Registers (GPR) area. The SFRs control the operation of the device.

Portions of data memory are banked. This is for both the SFR area and the GPR area. The GPR area is banked to allow greater than 116 bytes of general purpose RAM. The banked areas of the SFR are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register. Figure 2-2 shows the data memory map organization.

Instructions MOVWF and MOVF can move values from the W register to any location in the register file ("F"), and vice-versa.

The entire data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (FSR) (Section 2.5). Indirect addressing uses the present value of the RP0 bit for access into the banked areas of data memory.

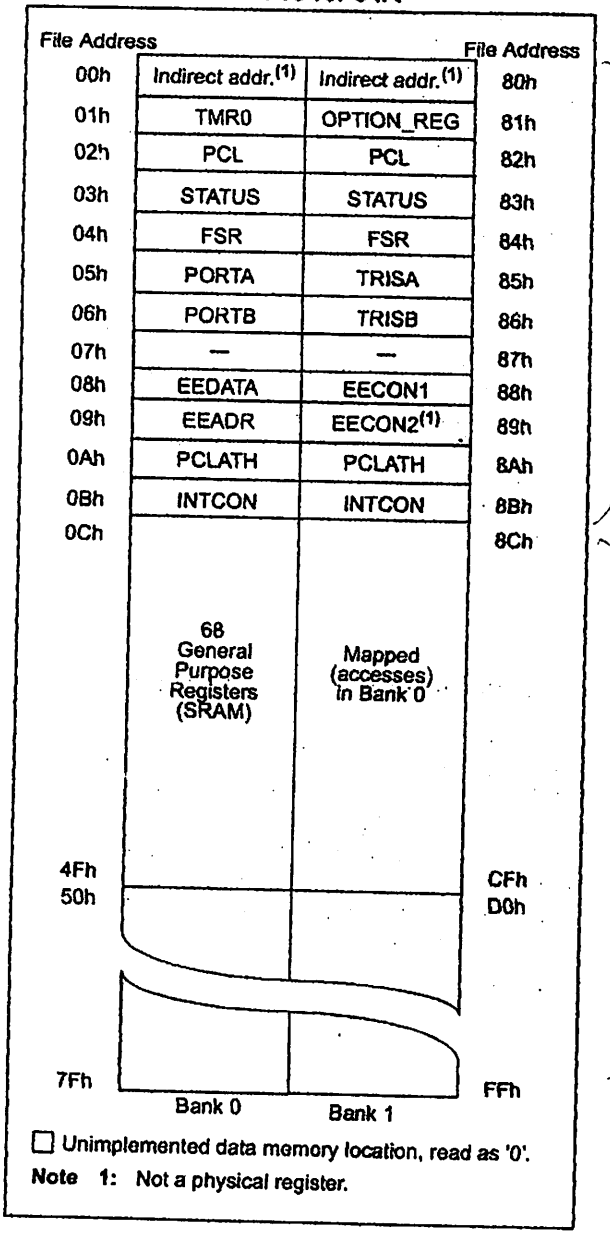
Data memory is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (STATUS<5>). Setting the RP0 bit selects Bank 1. Each Bank extends up to 7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers, implemented as static RAM.

2.2.1 GENERAL PURPOSE REGISTER FILE

Each General Purpose Register (GPR) is 8-bits wide and is accessed either directly or indirectly through the FSR (Section 2.5).

The GPR addresses in Bank 1 are mapped to addresses in Bank 0. As an example, addressing location 0Ch or 8Ch will access the same GPR.

FIGURE 2-2: REGISTER FILE MAP - PIC16F84A



☐ Unimplemented data memory location, read as '0'.

Note 1: Not a physical register.

Special Function Registers

ıecial Function Registers (Figure 2-2 and 1) are used by the CPU and Peripheral s to control the device operation. These are static RAM.

The special function registers can be classified into two sets, core and peripheral. Those associated with the core functions are described in this section. Those related to the operation of the peripheral features are described in the section for that specific feature.

2-1: SPECIAL FUNCTION REGISTER FILE SUMMARY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on RESET	Details on page
DF	Uses contents of FSR to address Data Memory (not a physical register)								---- ----	11
ИR0	8-bit Real-Time Clock/Counter								xxxx xxxx	20
CL	Low Order 8 bits of the Program Counter (PC)								0000 0000	11
TATUS(2)	IRP	RF I	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
SR	Indirect Data Memory Address Pointer 0								xxxx xxxx	11
ORTA(4)	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	16
ORTB(5)	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	18
—	Unimplemented location, read as '0'								—	—
EDATA	EEPROM Data Register								xxxx xxxx	13,14
EADR	EEPROM Address Register								xxxx xxxx	13,14
CLATH	—	—	—	Write Buffer for upper 5 bits of the PC(1)					---0 0000	11
TCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	10
OF	Uses Contents of FSR to address Data Memory (not a physical register)								---- ----	11
TION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	9
L	Low order 8 bits of Program Counter (PC)								0000 0000	11
ATUS (2)	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	8
R	Indirect data memory address pointer 0								xxxx xxxx	11
ISA	—	—	—	PORTA Data Direction Register					---1 1111	16
ISB	PORTB Data Direction Register								1111 1111	18
—	Unimplemented location, read as '0'								—	—
CON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	13
CON2	EEPROM Control Register 2 (not a physical register)								---- ----	14
LATH	—	—	—	Write buffer for upper 5 bits of the PC(1)					---0 0000	11
CON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	10

x = unknown, u = unchanged, - = unimplemented, read as '0', q = value depends on condition

The upper byte of the program counter is not directly accessible. PCLATH is a slave register for PC<12:8>. The contents of PCLATH can be transferred to the upper byte of the program counter, but the contents of PC<12:8> are never transferred to PCLATH.

The $\overline{TO}$ and $\overline{PD}$ status bits in the STATUS register are not affected by a $\overline{MCLR}$ Reset.

Other (non power-up) RESETS include: external RESET through $\overline{MCLR}$ and the Watchdog Timer Reset.

On any device RESET, these pins are configured as inputs.

This is the value that will be in the port output latch.

2.3.1 STATUS REGISTER

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bit for data memory.

As with any register, the STATUS register can be the destination for any instruction. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u uluu` (where u = unchanged).

Only the `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions should be used to alter the STATUS register (Table 7-2), because these instructions do not affect any status bit.

Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16F84A and should be programmed as cleared. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

2: The C and DC bits operate as a $\overline{borrow}$ and digit borrow out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

3: When the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. The specified bit(s) will be updated according to device logic

REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

bit 7-6 **Unimplemented:** Maintain as '0'

bit 5 **RP0:** Register Bank Select bits (used for direct addressing)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)

bit 4 $\overline{TO}$: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 $\overline{PD}$: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions) (for $\overline{borrow}$, the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0 **C:** Carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions) (for $\overline{borrow}$, the polarity is reversed)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note: A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2 OPTION REGISTER

OPTION register is a readable and writable ister which contains various control bits to configure TMR0/WDT prescaler, the external INT interrupt, t0, and the weak pull-ups on PORTB.

Note: When the prescaler is assigned to the WDT (PSA = '1'), TMR0 has a 1:1 prescaler assignment.

GISTER 2-2: OPTION REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 **$\overline{\text{RBPU}}$:** PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS2:PS0:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.4 PCL and PCLATH

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13 bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. If the program counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP. All updates to the PCH register go through the PCLATH register.

2.4.1 STACK

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution.

Mid-range devices have an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not modified when the stack is PUSHed or POPed.

After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

2.5 Indirect Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 2-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

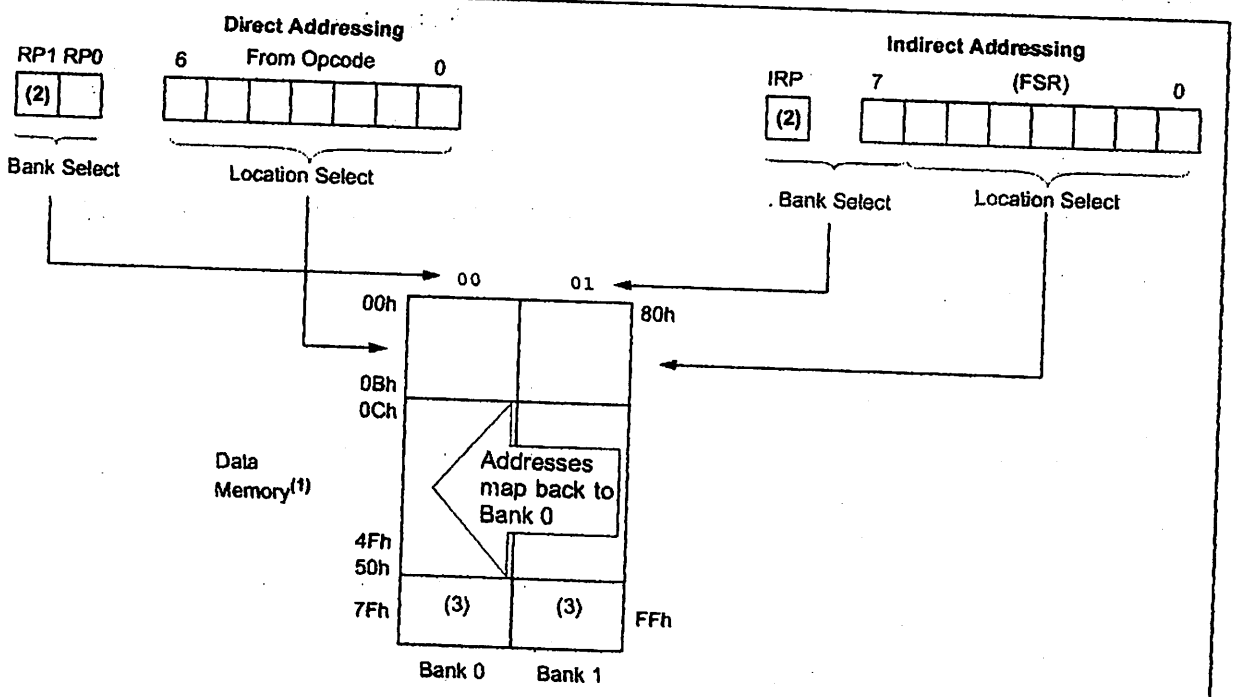
A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 2-2.

EXAMPLE 2-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
        movlw   0x20    ;initialize pointer
        movwf   FSR     ;to RAM
NEXT    clrf    INDF    ;clear INDF register
        incf    FSR     ;inc pointer
        btfss   FSR,4   ;all done?
        goto    NEXT    ;NO, clear next
CONTINUE
        :               ;YES, continue
```

An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-3. However, IRP is not used in the PIC16F84A.

FIGURE 2-3: DIRECT/INDIRECT ADDRESSING



Note 1: For memory map detail, see Figure 2-2.

2: Maintain as clear for upward compatibility with future products.

3: Not implemented.