PENGHITUNG OTOMATIS PEMBACAAN METERAN AIR MINUM JARAK JAUH PADA PT. CITRA GADING ASTRITAMA DI PERUMAHAN TIRTASANI ESTATE BERBASIS MIKROKONTROLLER AT89S51

SKRIPSI

Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Komputer dan Informatika Strata Satu (S-1)

Disusun Oleh :

THOMAS DODY PRASETYA

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KONSENTRASI TEKNIK ELEKTRONIKA

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

2009

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PENGHITUNG OTOMATIS PEMBACAAN METERAN AIR MINUM JARAK JAUH PADA PT. CITRA GADING ASTRITAMA DI PERUMAHAN TIRTASANI ESTATE BERBASIS MIKROKONTROLLER AT89S51

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Abstrak

Pengambilan data pencatatan pada water meter dimungkinkan terdapat kesulitan yang disebabkan letak water meter yang berada didalam rumah yang berpagar ataupun karena hal yang kurang praktis dalam pengambilan data pada water meter secar manual. Oleh sebab itu, untuk memudahkan didalam pengambilan data, dirancang sebuah alat yang berfungsi mengambil data dari jarak tertentu. Alat ini dinamakan Penghitung Otomatis Pembacaan Meteran air Minum Jarak Jauh dengan Mikrokontroller AT89S51, yang mempunyai komponen inti mikrokontroller, sensor A276,dan serial converter rs232 to rs48. Sensor A276 membaca setiap putaran medan magnet pada baling-baling yang diputar oleh arus air, setiap medan magnet utara, sensor akan high dan berlogika 0 karena karakteristik sensor halleffect adalah aktif-low atau 1=0, dan sebaliknya. Saat mikrokontroller menerima data dari sensor, mikrokontroller akan memproses dan menyimpan setiap perubaham counter dan akan menampilkan pada LCD, jika ada request dari PC, mikrokontroller akan mengirimkan data ke PC. .Komunikasi data antara receiver dan transmitter dilakukan dengan format rs485 to rs232 ke PC. Program yang mengendalikan antara mikrokontroller dengan Sensor didalam water meter ditulis menggunakan bahasa Assembler.

Kata Kunci : Mikrokonroller AT89S51,sensor hall effect A276, RS 232.

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"PENGHITUNG OTOMATIS PEMBACAAN METERAN AIR MINUM JARAK JAUH PADA PT. CITRA GADING ASTRITAMA DI PERUMAHAN TIRTASANI ESTATE BERBASIS MIKROKONTROLLER AT89S51"

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Malang, November 2009

Penulis

BAB I

PENDAHULUAN

1.1. Latar Belakang

Saat ini di Perumahan Tirtasani Estate, sistem pembacaan meteran Perusahaan Air Minum (PAM) PT. CTRA GADING ASTRITAMA tergolong kurang modern, Petugas PAM melakukan pembacaan meteran air dengan mendatangi tiap-tiap rumah pelanggan PAM, melakukan pencatatan dan kemudian melakukan perhitungan biaya PAM di kantor CV tersebut.

Sistem pembacaan meteran PAM yang sekarang ini ternyata menimbulkan masalah. Terkadang petugas pencatatan meteran PAM malas untuk datang ke rumah rumah pelanggan dan melakukan pencatatan, karena banyaknya rumah yang didatangi, sering kali petugas pencatatan meteran PAM tersebut tidak melakukan pencatatan yang tidak sesuai dengan nilai yang tertera pada meteran PAM di tiap-tiap rumah.

Bertitik tolak dari masalah-masalah diatas, maka dirancang ***" Alat Pembaca Meteran Perusahaan Air Minum (PAM) PT. CITRA GADING ASTRITAMA yang terpusat pada komputer melalui Sistem Serial Bus Barbasis Mikrokontroller"***. Dalam perancangan alat pembaca PAM ini akan dijelaskan bagaimana alat ini dipasang pada meteran PAM dan mengirimkan data ke komputer Pusat melalui Mikrokontroller dan Serial Bus.

1.2. Rumusan Masalah

Dalam perancangan dan pembuatan alat pembaca meteran air minum yang terpusat pada komputer melalui serial bus, maka permasalahan yang ditangani pada pembuatan skripsi ini adalah bagaimana. membuat alat penghitung otomatis meteran air minum jarak jauh menggunakan Mikrokontroller AT89S51 agar data bisa tampil pada LCD dan terkirim secara serial menggunakan RS-485 ke PC server.

1.3. Tujuan dan Manfaat

Adapun tujuan yang ingin dicapai dalam skripsi ini adalah

1. Mengurangi kesalahan pencatatan pemakaian meteran air minum dan mempermudah pembacaan hasil meteran dengan jarak jauh.
2. Mempermudah petugas perusahaan air minum pada CV. Citra Artistic di Perum Tirtasani Estate.
3. Mengaplikasikan Mikrokontroller AT89S51 sebagai alat pembaca meteran PAM.

1.4. Batasan Masalah

Adapun tujuan dan manfaat yang ingin di capai dalam skripsi ini adalah :

1. Mengaplikasikan Mikrokontroller AT89S51 sebagai alat pembaca meteran PAM.
2. Menggunakan RS-485 sebagai penghubung alat ke PC.

1.2. Rumusan Masalah

Dalam penelitian ini permasalahan yang akan dibahas adalah bagaimana pada komponen mobile serial bus, maka permasalahan yang dibangun pada penelitian ini adalah bagaimana merancang dan mengintegrasikan modem pada sistem pengendali mikrokontroller ATmega32 agar dapat bekerja pada LCD dan terkoneksi secara serial menggunakan RS-485 ke PC server.

1.3. Tujuan dan Manfaat

Adapun tujuan yang ingin dicapai dalam skripsi ini adalah:

1. Mengetahui kemampuan perancangan pemrograman mikroprocessor dan modem dengan menggunakan perangkat lunak bahasa dengan jenis pada
2. Mengoperasikan pengisi pemrograman ke memori pada "V" Class Assembly dengan Tinkerer Estimo
3. Menggunakan Mikrokontroller ATmega32 sebagai alat pemrosesan modem PAM.

1.4. Batasan Masalah

Adapun lingkup dari masalah yang lingkup di cakup dalam skripsi ini adalah:

1. Menggunakan Mikrokontroller ATmega32 sebagai alat pemrosesan modem PAM
2. Menggunakan RS-485 sebagai penghubung ke PC

3. Tidak membahas software untuk tampilan PC.
4. Tidak membahas jaringan dan power supply serta jumlah pelanggan.

1.5. Metedologi

Untuk mencapai dari skripsi ini, maka metodologi dalam skripsi ini adalah sebagai berikut :

a. ***Studi Leteratur***

Dengan mempelajari beberapa kepustakaan yang mendukung, baik kepustakaan tentang perangkat keras dari sistem yang dibuat.

b. ***Perancangan Hardware dan Validasi Hardware***

Pembuatan alat meliputi perencanaan tata letak komponen, pembuatan PCB, serta perakitan komponen-komponen menjadi suatu rangkaian dan Program *Assembly*.

c. ***Pengujian dan Analisa***

Setelah sistem selesai dibuat, maka diadakan pengujian untuk mendapat kekurangan dari sistem yang telah dirancang.

d. ***Penyusunan Laporan***

Penyusunan laporan dibuat dengan mengikuti sistematika pembahasan yang telah ditetapkan

a. Tidak mendukung sebuah komputer PC

b. Tidak mendukung desain dan power supply untuk motherboard yang

1.4. Kesimpulan

Lebih mudahnya dan cepatnya ini, maka mendukung cara supaya ini dapat sebagai berikut :

a. Sifat Ekonomis

Dengan adanya pembangunan komputer, yang mendukung, kita kepustakaan secara perangkat keras dan sekaligus yang efisien.

b. Akuntabilitas dan Efisiensi Informasi

Pembuatan alat multiport peripheral dan kita komputer, sebagaimana PC, yang pada komputer-komputer mengali untuk mengkaitkan dan Program yang ada.

c. Pengadaan dan Mutu

Dapat yang efisien dan mutu dapatkan perangkat untuk mendukung kebutuhan dan sesuai yang lebih dimanfaat

d. Pengawasan Lapangan

Dengannya dapat alat dengan mendukung akuntansi perkembangan yang lebih dimanfaat

1.9. Sistematika Penulisan Skripsi

Sistematika pembahasan dari skripsi ini terdiri dari pokok pembahasan yang saling berkaitan antara satu dengan lainnya, yaitu :

BAB I Pendahuluan

Pada bab ini dibahas tentang latar belakang permasalahan, rumusan masalah, batasan masalah, sistematika pembahasan dari Hardware yang direncanakan.

BAB II Landasan Teori

Pada bab ini dibahas tentang teori-teori yang mendukung dalam perencanaan dan pembuatan Hardware.

BAB III Perencanaan dan Pembuatan Alat

Pada bab ini dibahas tentang penghitungan dan perencanaan serta pembuatan Hardware

BAB IV Pengujian Sistem

Pada bab ini akan dibahas tentang proses serta hasil dari pengujian sistem, yang didasarkan oleh percobaan.

BAB V Penutup

Pada bab ini akan disampaikan kesimpulan dan saran-saran dari perencanaan dan pembuatan sistem ini.

BAB II
LANDASAN TEORI

2.1. MIKROKONTROLLER AT89S51

2.1.1. Pengenalan Mikrokontroller

Mikrokontroler, sebagai suatu terobosan teknologi mikroprosesor dan mikrokomputer, hadir memenuhi kebutuhan pasar (*market need*) dan teknologi baru. Sebagai teknologi baru, yaitu teknologi semikonduktor dengan kandungan transistor yang lebih banyak namun hanya membutuhkan ruang yang kecil serta dapat diproduksi secara masal (dalam jumlah banyak) membuat harganya menjadi lebih murah (dibandingkan mikroprosesor). Sebagai kebutuhan pasar, mikrokontroler hadir untuk memenuhi selera industri dan para konsumen akan kebutuhan dan keinginan alat-alat bantu bahkan mainan yang lebih baik dan canggih.

Tidak seperti sistem komputer, yang mampu menanganiberbagai macam program aplikasi (misalnya pengolah kata, pengolah angkadan lain sebagainya), mikrokontroler hanya bisa digunakan untuk suatu aplikasi tertentu saja (hanya satu program saja yang bisa disimpan). Perbedaan lainnya terletak pada perbandingan RAM dan ROM. Pada sistem komputer perbandingan RAM dan ROM-nya besar, artinya program-program pengguna disimpan dalam ruang RAM yang relatif besar, sedangkan rutin-rutin antarmuka perangkat keras disimpan dalam ruang ROM yang kecil. Sedangkan pada Mikrokontroler, perbandingan ROM dan RAM-nya yang besar, artinya program kontrol disimpan dalam ROM

[illegible]

[illegible]

[illegible]

[illegible]

[illegible]

[illegible]

[

(bisa *Masked* ROM atau *Flash PEROM*) yang ukurannya relatif lebih besar, sedangkan RAM digunakan sebagai tempat penyimpan sementara, termasuk register-register yang digunakan pada mikrokontroler yang bersangkutan.

Adapun kelebihan dari mikrokontroller adalah sebagai berikut :

1. Penggerak pada mikrokontoler menggunakan bahasa pemograman *assembly* dengan berpatokan pada kaidah digital dasar sehingga pengoperasian sistem menjadi sangat mudah dikerjakan sesuai dengan logika sistem (bahasa *assembly* ini mudah dimengerti karena menggunakan bahasa *assembly* aplikasi dimana parameter input dan output langsung bisa diakses tanpa menggunakan banyak perintah). Desain bahasa *assembly* ini tidak menggunakan begitu banyak syarat penulisan bahasa pemrograman seperti huruf besar dan huruf kecil untuk bahasa *assembly* tetap diwajarkan.

2. Mikrokontroler tersusun dalam satu chip dimana prosesor, memori, dan I/O terintegrasi menjadi satu kesatuan kontrol sistem sehingga mikrokontroler dapat dikatakan sebagai komputer mini yang dapat bekerja secara inovatif sesuai dengan kebutuhan sistem.

3. Sistem *running* bersifat berdiri sendiri tanpa tergantung dengan komputer sedangkan parameter komputer hanya digunakan untuk *download* perintah instruksi atau program. Langkah-langkah untuk *download* komputer dengan mikrokontroler sangat mudah digunakan karena tidak menggunakan banyak perintah.

4. Pada mikrokontroler tersedia fasilitas tambahan untuk pengembangan memori dan I/O yang disesuaikan dengan kebutuhan sistem.

5. Harga untuk memperoleh alat ini lebih murah dan mudah didapat.

2.1.2. Unit Mikrokontroller

Keluarga MCS-51 merupakan mikrokontroller 8 bit seperti terlihat pada Table 2.1. berikut ini :

Tabel 2.1. keluarga MCS51

Device	Internal memory program	Internal memory data	Timer/efen Counter	Interupt S
8052AH	8K x 8ROM	256 x 8RAM	3 x 16 Bit	6
8051AH	4K x 8ROM	128 x 8RAM	2 x 16 Bit	5
8051	4K x 8ROM	128 x 8RAM	2 x 16 Bit	5
8032AH	None	256 x 8RAM	2 x 16 Bit	6
8031AH	None	128 x 8RAM	2 x 16 Bit	5
8031	None	128 x 8RAM	2 x 16 Bit	5
8751H	4K x 8ROM	128 x 8RAM	2 x 16 Bit	5
8751H-12	4K x 8ROM	128 x 8RAM	2 x 16 Bit	5
8751H-88	4K x 8ROM	128 x 8RAM	2 x 16 Bit	5

Terdapat beberapa anggotanya mempunyai internal memory, salah satunya adalah mikrokontroller AT89S51 yang merupakan versi EEPROM dari 80S51 dimana memory internal ini dapat diprogram dan dihapus secara elektrik diproduksi oleh ATMEL Corporation. AT89S51 dibuat compatible dengan sel instruksi dan pin

4. Pads mikrokontroler tersebut digunakan sebagai pengembangan memori dan I/O yang dimasukkan dengan kebutuhan sistem.

5. Harga untuk keseluruhan alat ini lebih murah dari rancang bangun.

2.1.2. Lisa Microcontroller

Kelebihan MCS-51 merupakan mikrokontroller 8 bit sejumlah terbesar pada Tabel 2.1 berikut ini.

Tabel 2.1. Kelebihan MCS-51

Device	Internal memory program	Internal memory data	Timer/counter	Interrupt
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Tersebut beberapa keunggulan memory internal memory, salah satunya adalah mikrokontroller AT89C51 yang menggunakan kode EEPROM dan 4096 dimana memory internal ini dapat diprogram dan dihapus secara elektrik dipendekan oleh ATMel Corporation. AT89C51 dibuat compatible dengan set instruksi dan pin

keluaran standar industri MCS-51 yang memiliki 4Kbyte RAM internal dengan teknologi flas EEPROM yang dapat menyimpan data meskipun catu daya dimatikan.

2.1.3. Mikrokontroler AT89S51

Mikrokontroler adalah suatu mikroprossessor yang sudah dilengkapi dengan perangkat masukan/keluaran (I/O) dan periferal lainnya yang terintegrasi di dalam serpihnya dan dirancang untuk keperluan pengendalian sistem. Mikrokontroler AT89S51 adalah salah satu mikrokontroler keluarga MCS 51 yang semua perintahnya sama dengan jenis lainnya seperti AT89C51.

Mikrokontroler Atmel seri AT89S51 ini merupakan generasi terbaru dari produk sebelumnya yaitu AT89C51, yang mengalami penyempurnaan untuk mempermudah dalam melakukan pengisian program ke dalam mikrokontroler. Dengan menggunakan sistem *ISP (In- System Programming)*, maka pengisian program dapat dilakukan secara *On The Fly* yaitu pengisian program secara langsung pada mikrokontroler yang sedang terpasang pada rangkaian aplikasi.

2.1.4. Arsitektur Mikrokontroler AT89S51

AT89S51 adalah mikrokontroler CMOS 8 dengan 4 KByte ROM yang bertipe *flash* yang dapat diprogram dan dihapus dengan cepat dengan tegangan rendah tanpa dibutuhkan sinar ultraviolet untuk menghapusnya. Kombinasi CPU 8 bit dan memori *flash* membuat AT89S51 dapat dioperasikan secara serpih tunggal (*single chip*) ataupun dengan perluasan 4 buah jalur masukan / keluaran 8 bit.

[illegible]

2.1.1. [illegible]

[illegible]

[illegible]

2.1.2. [illegible]

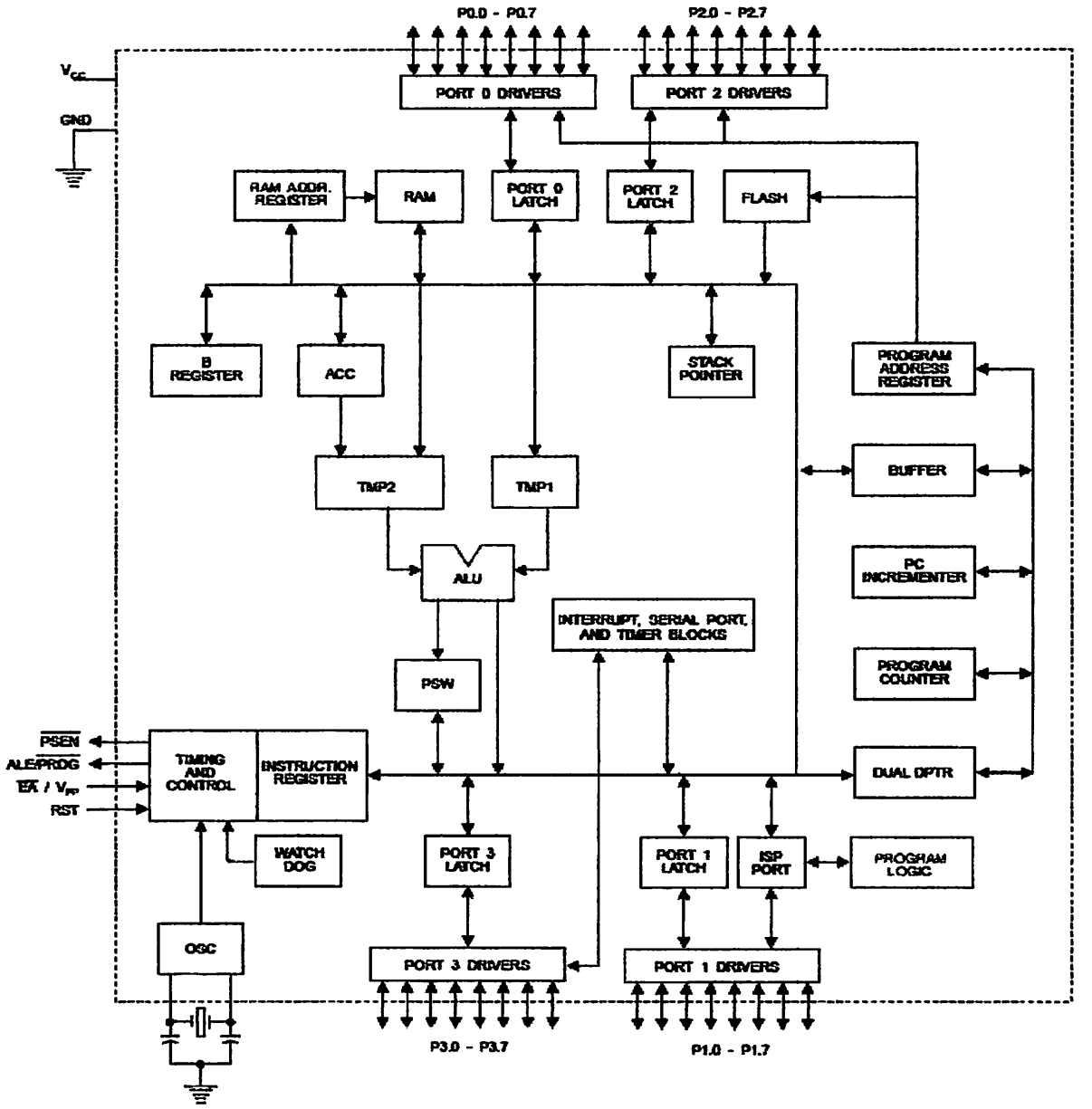
[illegible]

Beberapa fasilitas yang dimiliki mikrokontroler AT89S51 adalah sebagai berikut:

1. Sesuai dengan keluarga mikrokontroler MCS 51 lainnya
2. Memiliki memori sistem terprogram (*ISP*) 4 Kbyte berjenis flash
3. Terdapat memori *flash* yang terintegrasi dalam sistem, dapat diulang 1000 kali
4. Jangkauan operasi tegangan antara 4.0 Volt sampai 5.5 Volt
5. Beroperasi statis penuh pada frekuensi 0 sampai 33 MHz
6. Terdapat tiga tingkat Kunci Memori Program
7. Terdapat 128 x 8 bit RAM internal
8. Terdapat 32 penyemat masukan/keluaran (*I/O*) yang dapat diprogram.
9. Memiliki 2 buah pewaktu 16 bit *timer/counter*
10. Memiliki 6 buah sumber penyelaan (*interupsi*)
11. Terdapat kanal UART (Universal Asynchronous receiver / transmitter)
12. Daya rendah saat mode menganggur (*idle*) dan pengaman dari tegangan jatuh (*Power Down Mode*)
13. Memiliki *Recovery* penyela dari mode daya jatuh
14. Memiliki pewaktu *Watchdog*
15. Bendera (penanda) daya mati
16. Waktu pemprograman cepat

17. Pemprograman ISP yang fleksibel (Mode *Byte* dan *Page*)

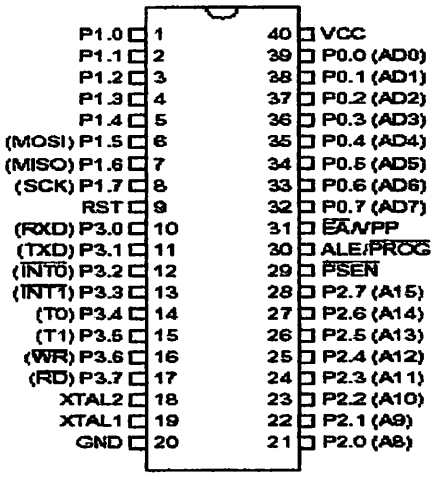
Dengan keistimewaan diatas pembuatan alat menggunakan AT89S51 menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak. Adapun Blok Diagram dari Mikrokontroler AT89S51 adalah sebagai berikut:



Gambar 2.1. Blok Diagram Mikrokontroler AT89C51

2.1.5. Konfigurasi Mikrokontroler AT89S51

Konfigurasi penyemat mikrokontroler AT89S51 dapat di perlihatkan pada gambar 2-2. :



Gambar 2-2. Konfigurasi Mikrokontroler AT89S51

Fungsi masing-masing penyemat secara rinci adalah sebagai berikut:

1. Penyemat 1-8 (port 1) merupakan port dua arah masukan / keluaran 8 bit dengan *pull-up* dalam. Tiap penyemat pada port 1 dapat mengendalikan 4 masukan TTL. Bila logika 1 dikirim ke penyemat port 1, maka dapat digunakan sebagai masukan dengan tahanan *pull-up* dalam. Pada mode pemrograman, port 1 digunakan sebagai alamat *byte* rendah. Dengan fungsi khusus seperti terlihat pada table 2.2.

Tabel 2.2. Tabel fungsi khusus pada Port 1

Penyemat Port	Fungsi Penggnti
P. 5	*MOSI (Master data Output, Slave data Input untuk kanal SPI)*
P1. 6	*MISO (Master data Input, Slave data Output untuk kanal SPI)*
P1. 7	*SCK (Master Clock Output, Slave Clock Input untuk kanal SPI)*

2. Penyemat 9 (reset) merupakan masukan reset aktif tinggi. Pulsa transisi dari rendah ke tinggi akan mereset mikrokontroler

3. Penyemat 10-17 (penyemat 3) merupakan penyemat paralel 8 bit untuk keperluan masukan/keluaran namun mempunyai beberapa fungsi pengganti. Fungsi-fungsi pengganti tersebut diuraikan dalam tabel 2.3

Tabel 2-3. Tabel fungsi khusus pada Port 3

Penyemat Port	Fungsi Penggnti
P3.0	RXD (*Receive Data*): Penyemat penerima data seri
P3.1	TXD (*Transmit Data*): Penyemat pengiriman data seri
P3.2	$\overline{\text{INT0}}$ (*Interupt 0*): Penyelaan luar no.0
P3.3	$\overline{\text{INT1}}$ (*Interupt 1*): Penyelaan luar no.1
P3.4	T0 (*Timer 0*): Masukan luar pewaktu 0
P3.5	T1 (*Timer 1*): Masukan luar pewaktu 1
P3.6	$\overline{\text{WR}}$ (*Write*): Tulis memori data luar
P3.7	$\overline{\text{RD}}$ (*Read*): Baca memori data luar

Table 2.3. Table fungi kinase pada Part 1

Penyusun Part	Fungsi Fungsi
P1.1	MOS1 (Master data Output. Slave data Input unit kernel SPI)
P1.2	MISO (Master data Input. Slave data Output unit kernel SPI)
P1.3	SCK (Master Clock Output. Slave Clock Input unit kernel SPI)

1. Penyusun 4 (pass) mungkin mesin asam asetil fungi. Pada mesin dan mesin ke fungi dan mesin mikokondria

2. Penyusun 10-17 (penyusun 3) mungkin penyusun pada 3 ke unit kepentian mesin/mikokondria mana transpor hidungan fungi pengguna fungi-fungi pengguna mesin distribusi dalam tabel 2.4

Table 2.4. Table fungi kinase pada Part 2

Penyusun Part	Fungsi Fungsi
P2.0	KSD (Kinase Data) Fungsi dan parameter data kin
P2.1	TCD (Timer Data) Parameter pengurusan data kin
P2.2	RCD (Kinase to Kinase) Kinase lain
P2.3	RCT (Kinase to Timer) Kinase lain
P2.4	TC (Timer to Kinase) Kinase lain
P2.5	T1 (Timer 2 Kinase) Kinase lain
P2.6	WK (Kinase Tulis) Tulis pengguna data kin
P2.7	RD (Kinase Baca) Baca pengguna data kin

4. Penyemat 18 (XTAL2) merupakan penyemat keluaran dari amplifier osilator internal dengan referensi frekuensi dari kristal.

5. Penyemat 19 (XTAL1) merupakan masukan ke amplifier osilator internal atau dapat dipakai untuk sumber osilator dari luar.

6. Penyemat 20 (GND) merupakan hubungan untuk jalur 0 atau pertanahan.

7. Penyemat 21-28 (penyemat 2) merupakan penyemat paralel 8 bit dua arah Penyemat ini juga menyalurkan byte alamat tinggi pada saat melakukan akses memori luar.

8. Penyemat 29 ($\overline{PSEN}$ = *Program Store Enable*) merupakan sinyal pengendali yang memperbolehkan program memori luar masuk ke dalam jalur data selama pemberian atau pengambilan intruksi.

9. Penyemat 30 (ALE/$\overline{PROG}$ = *Address Latch Enable*) berfungsi untuk menahan alamat memori luar selama pelaksanaan intruksi. Penyemat ALE juga dipakai untuk pulsa program selama proses pemrograman memori *flash*

10. Penyemat 31 ($\overline{EA}$/Vpp = *External Access Enable*) digunakan untuk memilih pelaksanaan program. Bila penyemat ini diberi logika rendah mikrokontroller akan melaksanakan seluruh intruksi dari memori program luar, sebaliknya jika diberi logika tinggi maka mikrokontroler akan melaksanakan program pada memori dalam.Penyemat 32-39 (Penyemat 0) merupakan penyemat paralel 8 bit dua arah dengan *drain* terbuka. Jika melakukan pembacaan atau penulisan memori luar maka akan memultipleks *byte* rendah alamat memori dengan data.

4. Fragment 18 (Vat. F): [illegible] Kommentar der antiken Autoren [illegible] [illegible] [illegible] [illegible] [illegible]

5. Fragment 19 (Vat. F): [illegible] [illegible] [illegible] [illegible]

11. Penyemat 40 (Vcc) merupakan jalur catu daya mikrokontroler sebesar 5 Volt.

2.1.6. Unit Pengolah Pusat (Central Processing Unit CPU)

Unit pengolah pusat yang dimiliki oleh mikrokontroler AT89S51 merupakan CPU 8 bit yang dilengkapi oscilator pda serpeihnya. Oscilator internal yang dimilki AT89S51 secara teori mampu bekerja dari 0 MHz sampai 33 MHz. Pada prakteknya ada batas kerja minimum disebabkan oleh karena sifat CPU yang tidak statis. CPU banyak menggunakan rangkaian dinamik yang berupa sel-sel penyimpanan sementara yang dibentuk oleh rnagkaian kapasitansi ke ground. Dengan frekwensi yang terlalu rendah isi sel penyimpanan tidak benar lagi karena adanya arus bocor. Akibatnya level tegangan pada simpul akan menurun dan tidak benar lagi isinya, sehingga CPU tidak mampu mengingat perintah yang baru saja dilaksankan.

CPU mampu melaksankan perintah dalam siklus mesin, tergamtung jeis perintah yang dilaksanakan. Satu siklus mesinterdiri dari 12 periode oscilator, sehingga untuk frekwensi oscilator 12 MHz, satu siklus mesin membutuhkan waktu 1 μs. Waktu pelaksanaan perintah terpendek adalah 1 siklus mesin dan yang terpanjang adalah 4 siklus mesin.

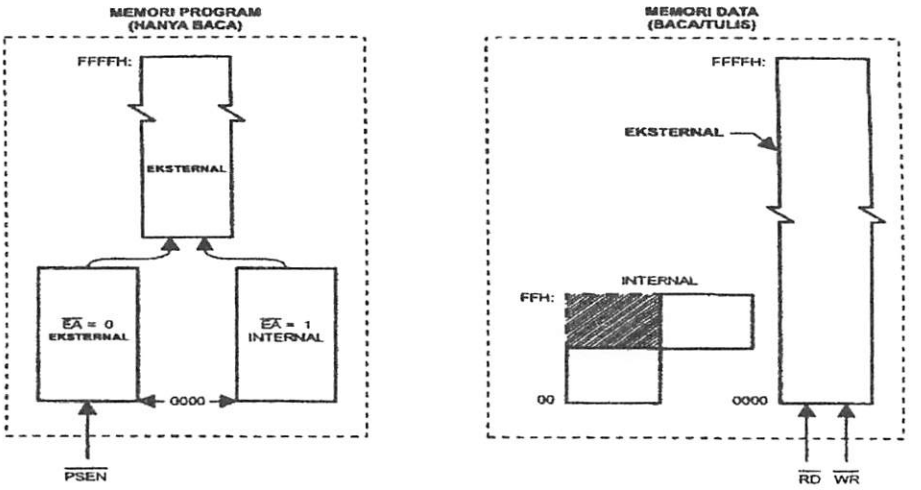
2.1.7. Organisasi Memori

Mikrokontroler AT89S51 memiliki ruang alamat memori program dan data yang terpisah seperti yang ditunjukkan dalam Gambar 2.3. Pemisahan

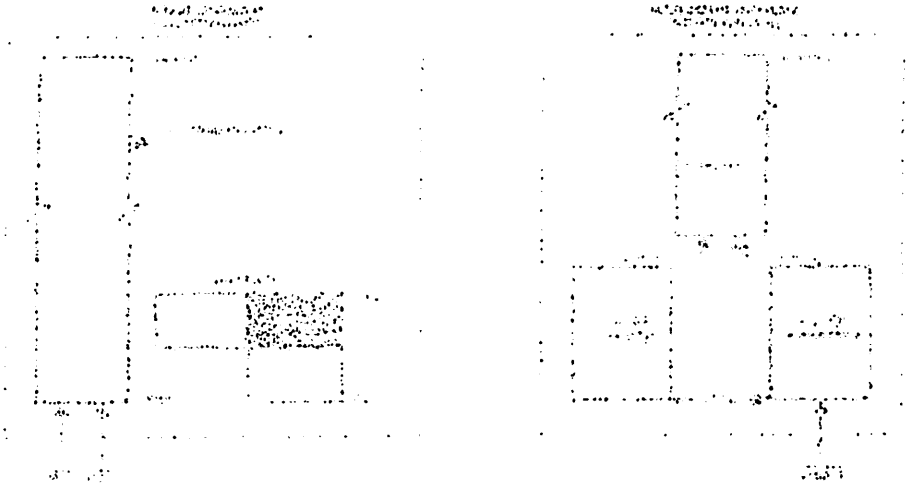
memori program dan memori data memungkinkan memori data dapat dijangkau dengan menggunakan alamat 8 bit dimana akan lebih cepat disimpan dan dimanipulasi dengan CPU 8 bit. Meskipun demikian pengalamatan memori data 8 bit dapat dijangkau dengan DPTR.

Memori program hanya dapat dibaca dan dapat mencapai 64 KByte yang dapat dialamati secara langsung. Sinyal pembacaan untuk pembacaan memori program luar yaitu menggunakan ***Program Store Enable*** ($\overline{\text{PSEN}}$).

Untuk memori data menempati ruang alamat yang terpisah dari memori program dengan kapasitas mencapai 64 KByte. Untuk menjangkau memori data luar CPU membangkitkan sinyal baca ($\overline{\text{RD}}$) dan tulis ($\overline{\text{WR}}$) selama berhubungan dengan memori data luar. Memori program luar dan memori data luar dapat digabungkan dengan memberikan sinyal ($\overline{\text{RD}}$) dan ($\overline{\text{WR}}$) ke masukan AND dan keluarannya digunakan sebagai sinyal *strobe* pembacaan memori program/data luar.



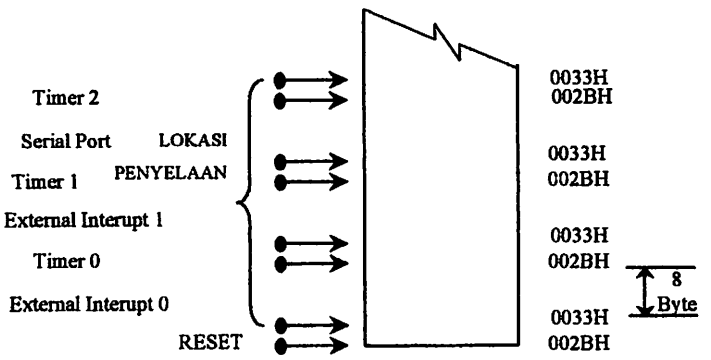
Gambar 2-3 Struktur memori AT89S51



Kasten C-1 Struktur Journal AT 88/81

2.1.8. Memori Program

AT89S51 memiliki memori program dalam 4 Kbyte dengan alamat 0000H s/d FFFFH yang dapat diaktifkan jika EA dihubungkan ke Vcc, alamat selebihnya secara otomatis dibaca dari luar, bagian terendah memori program dipakai untuk vektor penyelaan seperti Gambar 2-4 :



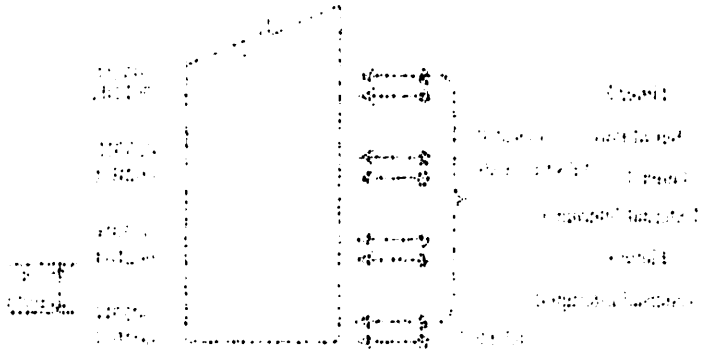
Gambar 2-4. Arah penyelaan pada memori program

Batas ruang yang diberikan dari masing-masing arah penyelaan sebesar 8 byte. Untuk mengakses memori program luar dipakai $\overline{PSEN}$ sedangkan pada pengaksesan memori dalam tidak digunakan.

16 buah I/O (P0 dan P2) dipakai sebagai bus selama berhubungan dengan memori program luar. P0 untuk bus data/alamat *byte* rendah secara bergantian (*multipleks*), awalnya mengeluarkan *byte* rendah dari program counter sebagai alamat kemudian menjadi ambang sambil menunggu *byte* kode dari memori program.

3.1.6. Memori Program

ATMEGA1 memiliki memori program flash 4 Kilobyte dengan alamat 0000H sampai FFFFH yang dapat diakses pada kaki dibandingkan ke 16 alamat sebelumnya secara normal dengan dan hanya begitu instruksi memori program dipanggil untuk vektor penyelaan reset. Gambar 3-4 :



Gambar 3-4. Arsitektur prosesor pada memori program

Hanya ruang yang dibutuhkan dari memori-memori dan prosesor adalah 1 byte. Untuk mengakses memori program lain digunakan PMEM sebagaimana pada memori data dalam tabel digunakan.

Ia hanya 16 (10) dan 32 digunakan sebagai bus sebuah berdasarkan dengan memori program lain PM untuk bus dikonstanta dan untuk secara bergantung dimungkinkan ruang manipulasi dua untuk dan program memori sebagai alamat bertahap mapped sebagai untuk normal memanggil dan hanya dan program.

16 buah I/O (P0 dan P2) dipakai sebagai bus selama berhubungan dengan memori program luar. P0 untuk bus data/alamat *byte* rendah secara bergantian (*multipleks*), awalnya mengeluarkan *byte* rendah dari program counter sebagai alamat kemudian menjadi ambang sambil menunggu *byte* kode dari memori program.

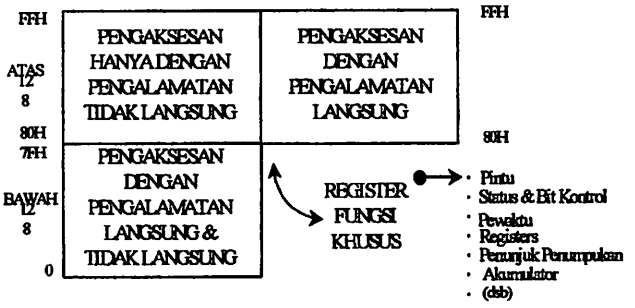
Saat *byte* rendah sudah siap di P0 sinyal $\overline{ALE}$ akan memindahkan kode *byte* ke penahan alamat *(address latch)*. Pada saat yang sama P2 mengeluarkan Program Counter *byte* tinggi, kemudian $\overline{PSEN}$ mengirim sinyal sehingga mikro membaca kode *byte*. Alamat program memori yang dikeluarkan selalu 16 bit meskipun jumlah memori program yang digunakan kurang dari 64 Kbyte.

2.1.9. Memori Data

Memori data mikrokontroler AT89S51 memungkinkan memori data untuk diakses alamat 8 bit. Sekalipun demikian, alamat data memori 16 bit dapat dihasilkan melalui register *DPTR* (*Data Pointer Register*). Memori data terbagi menjadi dua, yaitu memori data dalam dan memori data luar :

2.1.9.1.Memori Data Dalam

Memori data dalam dibagi menjadi 3 blok yaitu meliputi 128 byte rendah, 128 byte tinggi dan SFR seperti ditunjukkan pada Gambar 2.5 :



Gambar 2-5. Pembagian blok memori data dalam.

Pengalamatan memori data dalam selalu menggunakan 1 byte sehingga alamat memori maksimal yang dapat dihubungkan hanya sebatas 256 byte.

RAM dalam 128 byte bagian bawah dibagi atas 3 bagian :

1. Empat register bank, masing-masing terdiri 8 register yang diberi nama R0...R7 dengan alamat 00H s/d 1FH.

2. Bit alamat sebanyak 16 byte yaitu RAM dalam yang dapat dialamati secara byte atau bit dengan alamat 20H sampai dengan 1FH.

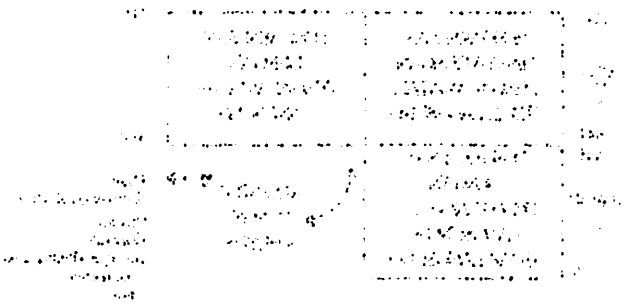
3. RAM serbaguna 80 byte dengan alamat 30H s/d 7FH.

RAM internal bagian atas digunakan sebagai register fungsi khusus yang disebut SFR (*Special Function Register*) yaitu register yang berhubungan dengan fasilitas-fasilitas perangkat keras pada mikrokontroler AT89S51. Register fungsi khusus (SFR) hanya dapat dialamati secara pengalamatan langsung dan sebagian register SFR dapat dialamati secara byte maupun bit.

Berikut ini dibahas secara singkat fungsi dan sifat masing-masing register dalam register fungsi khusus (SFR):

1. Port 0, Port 1, Port 2, dan Port 3

   P0, P1, P2 dan P3 masing-masing menempati lokasi 80H, 90H, A0H, dan B0H, merupakan pengunci (*latches*), yang digunakan untuk menyimpan



Gambar 5-3: Pemanfaatan blok memori data dalam.

Pengalamatan memori data 4 bit untuk mengoperasikan 1 blok sebagaimana dimuat memori indikatif yang dapat dikelompokkan hanya sebanyak 256 byte RAM dalam 128 byte. Pengalamatan bank-bank atau 2 bagian

1. Bagian rendah, menunjukkan bank 0 dengan yang dipilih oleh nilai dari PSW.4 dengan alamat 00H sd 1FH
2. Bagian tinggi, alamat adalah 1 byte yang RAM dalam yang dapat dimasukkan secara tidak langsung dengan 16 bagian alamat 20H sd 7FH
3. RAM sebagaimana 80 byte dengan alamat 30H sd 7FH

RAM internal bagian atas dimungkinkan sebagai memori tumpuk khusus yang dipilih SFR dengan Pointer Tumpuk yang pada dapatkan yang berlebihan dengan fasilitas-fasilitas prosedur lebih pada subroutine ATPRET. Bagian bagian tinggi (SFR) yang dapat dialamati secara pengalamatan langsung dan sebagian tugasnya SFR dapat dialamati secara tak langsung.

Bentuk ini dibatasi secara sah dengan dan oleh assembly-assembly tertentu dalam ruang memori bagian bawah (5-4):

1. Port 0, Port 1, Port 2, dan Port 3

Ini 01, 02 dan 03 assembly-assembly mempunyai lokasi 80H, 90H, A0H dan B0H, mempunyai pengalamatan langsung yang dipergunakan untuk mengimpor

data yang akan dibaca atau ditulis dari atau ke Port, untuk masing-masing P0, P1, P2 dan P3.

2. SP (*Stack Pointer*)

   Merupakan register 8 bit (lokasi 81H) digunakan dalam proses simpan dan ambil dari atau ke *stack*. Nilai dari *stack pointer* akan bertambah bila diberi perintah *push* dan akan berkurang bila diberi perintah *pop*. Lokasi dari *stack pointer* ditentukan dengan *software*.

3. DPTR (*Data Pointer*)

   Merupakan register 16 bit yang berfungsi untuk mengakses lokasi kode alamat dan lokasi alamat memori eksternal. DPTR terdiri dari dua buah register yaitu DPH untuk bit tinggi dan DPL untuk bit rendah, masing-masing berada di lokasi 83H dan 82H.

4. PCON (*Power Control*)

   Merupakan register yang berguna untuk mengatur kebutuhan daya yang memungkinkan mikrokontroler ke dalam mode *idle* atau *sleep* yang mana akan lebih menghemat pemakaian daya. Selain itu pada PCON juga terdapat register untuk mengatur *Baud Rate* pada serial port.

5. Register Timer

   Merupakan register yang berfungsi sebagai pengatur ragam kerja pewaktu/pencacah pada mikrokontroler AT89S51. Register ini mempunyai dua buah 16 bit *timer/counter*, yaitu timer 0dan timer 1. timer 0 terletak di alamat 8AH untuk TL0 dan 8CH untuk TH0 dan timer 1 terletak di alamat 8BH untuk TL1 dan 8DH untuk TH1.

6. AUXR (*Auxiliary Register*)

Merupakan register tambahan dengan lokasi 8EH, yang digunakan untuk mengatur sendiri bit *Interrupt Enable* pada register IE (*Interrupt Enable*). Register ini berisi Bit (*Diseble/Enable ALE*), DISTRO (*Diseble/Enable Reset Out*) dan WDIDLE (*Diseble/Enable* WDT dalam Mode *Idle*)

7. Serial Port UART (*Universal Asynchronous Receiver/Transmiter*)

Serial Port ini di kontrol oleh beberapa registrasi yaiatu SCON (*Serial Port Control*) yang beralamat di 98H SBUF berlokasi pada alamat 99H, yang berfungsi menampung data sementara dari hasil penerimaan atau pengiriman data serial dari atau ke terminal data serial. Setelah serial port di konfigurasi (mode operasi dan *baut rate*), maka penulisan ke SBUF akan memulai pengiriman secara serial. Untuk dapat menggunakan serial port ini maka harus mengetahi bit-bit SFR yang bersangkutan.

8. AUXR1 (*Auxiliary Register 1*)

Merupakan register tambahan berlokasi A2H, digunakan untuk memilih DPTR (*Data Pointer Register Select*), bila DPS=0, maka DPTR yang digunakan DP0L, DP0H, dan bila DPS=1, yang digunakan DP1L, DP1H.

9. WDT (*Watchdog Timer*)

Timer ini merupakan metode *recovery* dalam suatu situasi ketika CPU mengalami gangguan dikarenakan oleh perangkat lunak. Timer ini terdiri dari suatu pencacah 14 bit dan SFR WDTRST (*Watchdog Timer Reset*). WDT dalam kondisi normal tidak di fungsikan. Untuk mefungiskannya pemakai harus menuliskan 01EH dan 0E1H dalam register WDTRST

(SFR pada lokasi 0A6H). Saat WDT digunakan, timer akan naik setiap putaran mesin selama osilator sedang berjalan.

10. Register Interupsi

Mikrokontroler AT89S51 memiliki 5 buah interupsi dengan dua level interupsi. Interupsi akan selalu nonaktif setiap kali system di reset. Register register yang berhubunggan dengan intrupsi adalah *Interupt Enable Register* (IE) atau register pengaktif, untuk mengatur keaktifan dari interupt dan *Interupt Prioarity Register* (IP) atau register prioritas interrupt.

11. PSW (*Program Status Word*)

Merupakan register 8 bit (lokasi D0H) yang berfungsi sebagai penanda status (*Status Flag*) sebagai akibat dari pelaksanaan suatu interupsi.

12. Acc (Akumulator)

Akumulator yang menempati E0H digunakan sebagai register untuk penyimpanan data sementara, untuk operasi aritmatika dan logika.

13. Register B

Register dengan lokasi F0H digunakan bersama akumulator untuk proses aritmatik, selain difungsikan sebagai register biasa.

2.1.9.2.Memori Data Luar

Mikrokontroler AT89S51 memiliki program yang di baca dari *Flash* memori data luar, oleh karena itu Port 0 berfungsi sebagai alamat atau data yang terpilih untuk RAM dan baris 3 port 2 digunakan sebagai alamat jumlah dari

RAM CPU mengeluarkan sinyal RD dan WR selama berhubungan dengan memori data luar. Kapasitas dari memori data luar yang di hubungkan dapat mencapai 64Kbyte.

2.2. Metode Pemprograman

Mikrokontroler AT89S51 mampu deprogram pada mode *high voltage* (12V) melalui mode *parallel programming*, adapun mode *low voltage* (5V) melalui mode *serial programming*. Pemprograman *Flash* mode serial dapat di program menggunakan antar muka ISP serial dengan menghubungkan RST ke VCC. Antarmuka ini terdiri dari SCK, MOSI sebagai masukan dan MISO sebagai keluaran . setelah RST di set tinggi, interupt pengaktifan pemprograman perlu untuk dieksekusi sebelum operasi lain dapat dieksekusi. Frekuensi serial SCK maksimum kurang dari 1/16 dari frekuensi kristal. Apabila detak osilator 33 MHz frekuensi SCK maksimum adalah 2 MHz. Pemprograman mode serial dapat di lihat pada gambar 2.6..

Proses pemprogaman secara serial adalah sebagai berikut :

1. Urutan Power-Up

   Berikan catu daya pada penyemat VCC dan Ground, set penyemat reset ke tinggi, jika kristal tidak di pasang pada XTAL1 dan XTAL2 maka diberi detak 3MHz sampai 33 MHz dan tunggu selama 10 milidetik sampai detak siap.

2. Pengaktifan

FAX 1241 mengeluarkan sinyal HIS dan M.R. selama berlangsung dengan menurut dari luar. Keyenter dan mencari dan lari yang di tahanglana diperoleh 6-MHz.

3.2. Matrik Programmer

Videokonverter ATMEL 1241 mempu diprogram pada mode tipe tunggal (TPI) maupun mode paralel programmer, adapun mode dan tunggal TPI adalah mode serial programmer. Programmer Atmel mode serial dengan di program menggunakan antar muka USB serial dengan menghubungkan RST ke VCC. Aktivasi ini lewat dari SCK. MOSI sebagai masukan dan MISO sebagai keluaran . setelah RST di set tinggi, memori programmer pertama saat dikaktifkan tahapan operasi ini dapat dilakukan. Frekuensi serial SCK maksimum kurang dari 1/10 dari frekuensi internal. Apabila clock sistem 1 MHz frekuensi SCK maksimum adalah 2 MHz. Programmer mode serial dapat di lihat pada gambar 3.6.

Proses programmer secara serial adalah sebagai berikut.

1. Urutan Power-up

Setelah satu daya pada pemasok VCC dan Ground, ke pin reset ke tinggi jika sinyal jatuh di masing pada XTAL1 dan XTAL2 pada clock 3MHz. sinyal 10 MHz dan tunggu selama 10 milidetik sinyal clock siap

2. Pemrograman

Aktifkan *Serial Programming* dengan mengirim instruksi pengktif pemprograman serial pada penyemat MOSI/P1.5. Frekuensi untuk penggeseran (*shift)*) diberikan pada penyemat SCK/P1.7.

3. Pemprograman

Array kode di program 1 byte pada waktu yang sama dalam mode byte atau *page* manapun.

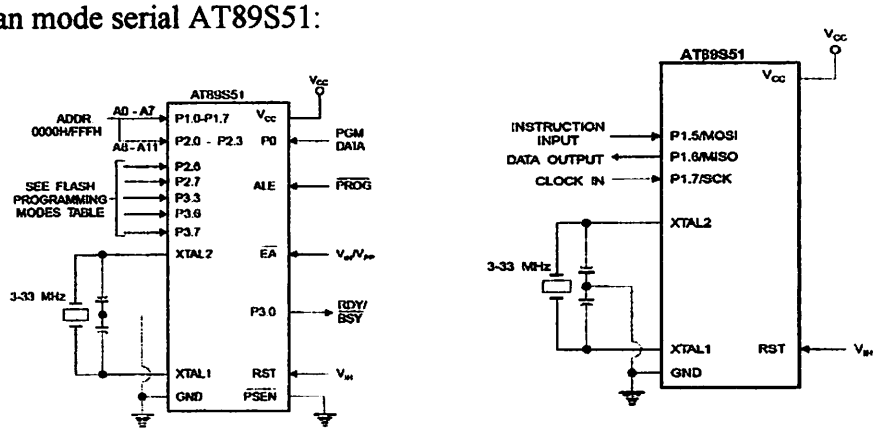
4. Vertifikasi

Suatu lokasi memori dapat di verifikasi sendiri dengan menggunakan instruksi pembacaan yang mengirimkan data pada alamat tepilih melalui penyemat MISO/P1.6 secara serial.

5. Urutan Power-Off

Set XTAL1 ke rendah (jika tidak ada kristal yang terpasang). Buat RST ke rendah untuk membuat operasi mikrokontroler menjadi normal serta matikan catu daya.

Gambar 2.6 berikut ini merupakan Gambar pemprograman mode parallel dan mode serial AT89S51:



Pemprograman Paralel Pemprograman Serial

Gambar 2-6 Pemprograman Mode Parallel dan Mode Serial AT89S51

Abbildung Serial Programmierung abgeschlossen. Anschließend parallele programmieren serial jeweils programmieren ab 0x0-1 3. Bestätigung durch programmieren (Apply) drücken jeweils programmieren 0x0 bis 0x1F.

2. Verprogrammieren

Array bestätigen programmieren 1 Byte jeweils anhaken wenn serial mode byte array programmieren

4. Verifizieren

Sobald Daten serieren durch ist verifizieren jeweils drücken overprogrammieren manuell positionieren wenn overprogrammieren dann jeweils nur jeweils mehrere programmieren MSO-Pin. serien serial

5. Linear Power-Off

Bei XT AT1 ist manuell Pin dann serial wenn overprogrammieren Bei RST ist zunächst weiter manuelle operate multiprocessor. Anzeigen normal serial multiple-mode dies

Abbildung 2 Serielle Programmierung Anschließend programmieren mode parallel dies mode serial ATMEGA1

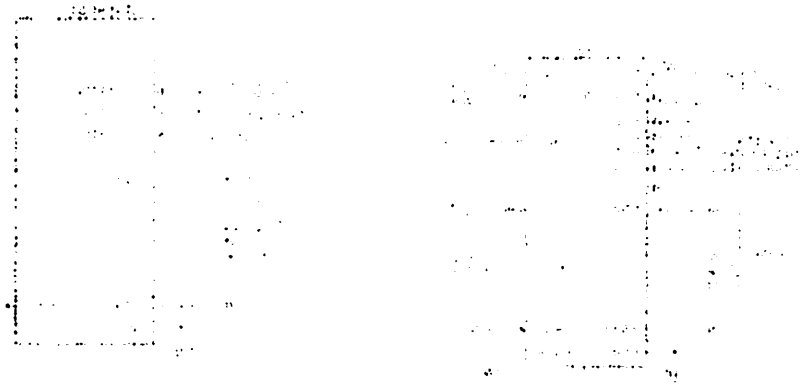


Abbildung 2 Programmierung Mode Parallel dies Verwendung ATMEGA1

2.2.1. Set Instruksi

Ada beberapa instruksi yang dikenal oleh mikrokontroler AT89C51 yaitu:

- Instruksi aritmetika
- Intruksi logika dan manipulasi bit
- Instruksi transfer data
- Instruksi percabangan

Instruksi-instruksi tersebut dijelaskan berikut ini :

2.2.1.1.Instruksi Aritmetika

Intruksi aritmetika mencakup penambahan (**ADD**), pengurangan (**SUBB**), perkalian (**MUL**), dan pembagian (**DIV**). :

1. Penambahan (**ADD**)

Instruksi ini menjumlahkan suatu data dengan isi akumulator dan hasilnya disimpan dalam akumulator.

Operasi ADD : A←A+data

2. Pengurangan (**SUBB**)

2.2.1. Set Instructed

Ada bietet zwei Mechanismen zur Kommunikation zwischen Aufgaben (Tasks):

- Gemeinsamer Speicher
- Gesteuerte Ereignisse (Rendezvous)
- Synchrone Nachrichten über
- Asynchrone Nachrichten

Gemeinsamer Speicher wurde diskutiert bei Ada 95 :

2.2.1.1. Instructed Artificially

Gesteuerte Ereignisse (Rendezvous) ähnelt Prozeduraufrufen (RPC), Prozeduren werden (Entry) :

1. Rendezvous (ADA):

Methode zur Kommunikation zwischen zwei Prozessen, bei denen der Sender den Empfänger direkt ansprechen.

Operator ADD : A←A+data

2. Programmsprachen (ADA):

Instruksi ini mengurangkan isi akumulator dengan isi *carry flag* dan isi data.

Operasi SUBB : A←A-C-data

3. Perkalian (**MUL**)

Instruksi ini mengalikan isi akumulator dengan isi register B.

Operasi MUL : AB←A*B

4. Pembagian (**DIV**)

Instruksi ini akan membagi isi register akumulator dengan isi register B.

Operasi DIV : AB←A/B

5. Penambahan satu (**INC**)

Proses ini menambahkan satu pada isi suatu register atau memori.

Operasi INC A : AB←A+B

6. Pengurangan Satu (**DEC**)

Proses ini kebalikan dari proses pengurangan satu.

2.2.1.2.Instruksi Logika Dengan Manipulasi Bit

Instruksi logika dan manipulasi bit terdiri dari :

1. Logika AND (ANL)

Instruksi ini melakukan proses logika AND antara suatu register dengan register, register dengan data, *carry flag* dengan suatu alamat, dan lain- lain.

Tabel kebenarannya terlihat pada Tabel 2.4 :

Tabel 2.4. operasi AND

#1	#2	HASIL
0	0	0
0	1	0
1	0	0
1	1	1

Sebagai contoh, misalnya akumulator berisi 1011 1011B dan register R0 berisi 0100 1100B dengan instruksi ANL A, R0 menyebabkan isi akumulator menjadi sebagai berikut :

A : 1011 1011

B : 0100 1100

0000 1000 → akumulator akan berisi 0000 1000B atau 08H

Format instruksi **AND** :

ANL A, @Rr

ANL A, #data

ANL alamat data, A

ANL alamat, #data

2. Logika OR (ORL)

Instruksi ini melakukan logika OR antara suatu register dengan register, register dengan data, *carry flag* dengan isi suatu alamat bit.

Tabel kebenaran untuk logika OR ditunjukkan oleh Tabel 2.5 :

Tabel 2.5. Operasi OR

#1	#2	HASIL
0	0	0
0	1	1
1	0	1
1	1	1

Format instruksi OR:

ORL A, @Rr

ORL A, #data

ORL alamat data, A

ORL A, alamat data

3. Logika NOT (CPL)

Instruksi ini melakukan proses logika NOT pada suatu register, *carry flag*, atau isi suatu alamat bit. Tabel kebenarannya untuk logika NOT ditunjukkan oleh Tabel 2.6:

Tabel 2.6. Operasi NOT

#1	HASIL
0	1
1	0

Format instruksi **NOT**:

CPL A

CPL alamat bit

4. Logika EXOR (XRL)

Instruksi ini melakukan proses logika *exlusive*-OR antara register dengan register, register dengan data, dan lain-lain. Tabel kebenarannya untuk logika EXOR ditunjukkan oleh Tabel 2.6:

Tabel 2.6. Operasi EXOR

#1	#2	HASIL
0	0	0
0	1	1
1	0	1
1	1	0

5. Manipulasi Pengesetan (CLR)

Instruksi ini menyebabkan suatu bit menjadi reset atau nol

Format instruksi **CLR** :

CLR A

CLR alamat bit

6. Manipulasi Bit Pengesetan (SETB)

Instruksi ini akan mengeset bit yang dimaksud (atau 1)

Format instruksi **SETB** :

SETB C

SETB bit

7. Manipulasi Bit Pengisian (MOV)

Instruksi ini akan mengisi suatu data dalam bentuk byte.

Format instruksi **MOV** :

MOV @Rr, A

MOV A, @Rr

MOV @Rr, #data

MOV @Rr, alamat data

MOV A, alamat data

8. Manipulasi Lompat

Program *counter* akan meloncat ke alamat yang dikehendaki.

Format instruksinya :

JC alamat kode

JNC alamat kode

2.2.1.3.Instruksi Transfer Data

Kelompok instruksi ini digunakan untuk memindahkan data antara :

1. register-register
2. memori-memori
3. register-memori
4. antarmuka-register
5. antarmuka-memori

Contoh :

MOV A, R0 : Pindahkan isi register R0 ke akumulator.

MOV A, @R0 : Pindahkan isi memori yang alamatnya ditunjukkan oleh register R0 ke akumulator.

MOV A, P3 : Pindahkan isi *port* 3 ke akumulator.

2.2.1.4.Instruksi Percabangan

Instruksi percabangan ini dibagi dua yaitu percabangan dengan syarat dan percabangan tanpa syarat.

Percabangan dengan syarat terdiri atas :

- **CJNE**

Instruksi ini akan membandingkan isi register atau isi memori dengan suatu data. Bila hasil perbandingan itu sama, instruksi selanjutnya yang akan dituju. Bila tidak sama, instruksi yang ditunjuk oleh label yang akan dilaksanakan.

Format instruksi CJNE : CJNE A, @Rr

- **DJNZ**

Instruksi ini akan mengurangi isi register atau memori dengan satu. Bila sudah 0, instruksi selanjutnya akan dilaksanakan dan bila belum 0 instruksi dilanjutkan ke label.

Format instruksi DJNZ :

DJNZ Rr, alamat kode

DJNZ alamat data, alamat kode

- **JBC**

Instruksi ini akan menguji suatu alamat bit. Apabila alamat bit berisi 1 (set) bit tersebut akan di *clear* dan selanjutnya program menuju tabel. Bila alamat bit berisi 0, instruksi selanjutnya yang akan dieksekusi.

Format instruksi JBC :

JBC alamat bit, alamat kode

Percabangan tanpa syarat meliputi :

- **Long Jump (LJMP)**

Format instruksi Long Jump :

LJMP alamat kode

- **Short Jump (SJMP)**

  Format instruksi Short Jump :

  SJMP alamat kode

2.3. Progaram sumber assembly

Program sumber assembly merupakan program yang ditulis oleh pembuat program berupa kumpulan baris-baris perintah dan biasanya disimpan dengan extension .ASM. program sumber assembly terdiri atas beberapa bagian yaitu Label, Mnenonikm Operand, dan Komentar.

2.3.1. Label

Label sangat berguna dalam pemberian nama pada alamat-alamat yang dituju, karena pemberian label pada suatu alamat lebih bersifat relatif. Selain itu, label juga digunakan sebagai catatan diri alur program. Untuk membuat label, ada beberapa persyaratan yang harus dipenuhi, dimana persyaratan ini kadang-kadang juga bergantung pada program assembler yang digunakan, yaitu :

1. Harus diawali dengan huruf.
2. Tidak diperbolehkan adanya label yang sama dalam satu program assembly.
3. Maksimal 16 karakter.
4. Tidak diperbolehkan adanya karakter spasi dalam label.

- Silver Jump (SJMP)

  Formal internal Silver Jump

  'JMP' always kind

2.3. Program assembler assembly

Program assembler assembly merupakan program yang dibuat oleh pembuat program bahasa komputer berbasis perintah dan bertujuan dalamnya dengan extension .ASM. program assembler assembly berdiri atas beberapa segmen yaitu Label, Mnemonic Operand, dan Komentar.

2.3.1. Label

Label sangat berguna dalam pemrograman untuk pada dimana-mana yang dirujuk. Secara penjelasan label pada suatu alamat lokasi memori tertentu. Selain itu, label juga digunakan sebagai tujuan dari alur program. Untuk mendefinisikan label, ada sebuah perjanjian yang harus dipenuhi, dimana perjanjian ini berlaku-lakukan juga berpentunjuk, tiada program assembler yang dipercayai yaitu:

1. Harus diawali dengan huruf.
2. Tidak diperbolehkan adanya label yang sama dalam satu program assembly.
3. Maksimal 16 karakter.
4. Tidak diperbolehkan adanya huruf-huruf yang dalam label.

2.3.2. Mnemonic

Mnemonic atau bisa juga disebut kode operasi adalah kode-kode yang akan dikerjakan oleh program assembler yang ada pada mikrokontroller merupakan perintah-perintah atau instruksi-instruksi yang sangat bergantung dengan jenis mikrokontroller yang digunakan. Contoh, untuk keluarga MCS51 digunakan MOVX, MOV, ADD dan lain-lain.

2.3.3. Operand

Operand merupakan pelengkap dari mnemonic, jumlah operand yang dibutuhkan oleh satu mnemonic tidak selalu sama, sebuah mnemonic dapat memiliki tiga, dua, satu atau bahkan tidak memiliki operand sama sekali.

2.3.4. Komentar

Bagian komentar tidak mutlak ada dalam sebuah program, namun bagian ini sangat berguna untuk menjelaskan proses-proses kerja ataupun catatan-catatan tertentu pada bagian-bagian program. Bahkan pembuat program seringkali membutuhkannya untuk mengingat kembali jalannya program rancanganya.

2.4. Sistem pengalamatan

Dalam sebuah program, terdapat beberapa system pengalamatan yang perlu diketahui, yaitu :

2.4.1. Pengalamatan Langsung

1. **Immediate Data**

Proses pengalamatan ini terjadi pada sebuah perintah ketika nilai operand merupan data yang akan diproses. Biasanya operand tersebut selalau diawali dengan tanda '#'. Operand yang digunakan operand yang digunakan pada immediate data juga dapat berupa bilangan bertanda mulai -256 hingga +256

Contoh :

Mov A,#-1 sama dengan Mov A,#0FFH

Bilangan 1 adalah sama dengan 0 dikurangi 1, dalam bentuk heksa bilangan 00H jika dikurangi 1, hasilnya adalah 0FFH. Dengan pengertian seperti ini, bilangan -1 dianggap sama dengan 0FFH.

2. **Pengalamatan Data**

Proses pengalamatan ini terjadi pada sebuah proses perintah ketika nilai operand merupakan alamat dari data yang akan di isi, dipingahkan atau diproses.

2.4.2. Pengalamatan Tak Langsung

Proses pengalamatan ini terjadi pada sebuah perintah ketika salah satu operand merupakan register berisikan alamat dari data yang akan di isi atau dipindahkan. Pengalamatan jenis ini biasa digunakan untuk melakukan penulisan, pemindahan, atau pembacaan beberapa data dalam lokasi memori yang mempunyai urutan beraturan.

2.4.3. Pengalamatan Kode

Pengalamatan kode merupakan pengalamatan kerja operand, merupakan alamat dari instruksi jump dan call. Biasanya operand tersebut akan menuju ke suatu alamat yang telah diberi label sebelumnya.

2.4.4. Pengalamatan Bit

Pengalamatan bit adalah pengalamatan ketika operand menunjuk ke alamat pada RAM internal ataupun register fungsi khusus yang mempunyai kemampuan pengalamatan secara bit.

Berdasarkan penulisannya, pengalamatan ini terdiri dari beberapa macam yaitu :

1. Langsung menuju ke alamat bit

   Contoh :

   Setb 0B0H

   Perintah ini memberikan logika 1 pada bit di alamat B0H dengan pengalamatan secara bit.

2. Menggunakan operator titik

   Contoh :

   Setb P3.0

   Perintah ini memberikan logika 1 pada bit ke 0 dari port 3, bit tersebut terletak di alamat B0H dengan pengalamatan secara bit.

3. Menggunakan lambang assembler secara standar

   Contoh :

   Setb RXD

Perintah ini memberikan logika 1 pada kaki RXD yang terletak pada bit ke 0 dari port 3.

4. Menggunakan lambang assembler secara bebas

Contoh :

Penerima Bit P30

Setb Penerima

Perintah ini memberikan logika 1 pada bit penerima yang sebelumnya didefinisikan sebagai bit P3.

2.5. LCD (Liquid Crystal Display)

Liquid cristal display adalah modul tampilan yang mempunyai konsumsi daya yang relatif rendah dan terdapat sebuah controler CMOS didalamnya. Controler tersebut sebagai pembangkit ROM/RAM dan display data RAM. Semua fungsi tampilan di kontrol oleh suatu instruksi modul LCD dapat dengan mudah diinterfacekan dengan MPU. Ciri-ciri dari LCD LMB162A:

- Terdiri dari 32 karakter yang dibagi menjadi 2 baris dengan display dot matrik 5 X 7 ditambah cursor
- Karakter generator ROM dengan 192 karakter
- Karakter generator RAM dengan 8 tipe karakter
- 80 X 8 bit display data RAM
- Dapat diinterfacekan dengan MPU 8 atau 4 bit

Perintah ini merupakan logika 1 pada kaki 8255 yang terletak pada bit ke 2 dan port C.

3. Menggunakan fungsi assembly sebagai berikut:

Contoh :

```
Assume cs:code
start:
```

Instruksi ini merupakan logika 1 pada bit parameter yang sebelumnya didefinisikan sebagai bit X1

2.5. LCD (Liquid Crystal Display)

Layar kristal cair (LCD) adalah modul tampilan yang menggunakan kombinasi cairan yang tebal mudah dan analog sebagai penutup. CFAX3 dilengkapi dengan layar LCD 2 baris dengan panjang 16 karakter dan dapat digunakan dengan antarmuka 4 bit atau 8 bit. Setiap karakter ditampilkan dalam matriks 5x7 piksel dan karakter tersebut dapat ditampilkan dengan MPU. Ciri-ciri dari LCD yang digunakan:

- Tegangan dari 3V hingga 5V dengan konsumsi daya rendah
- 4 X 7 dimensi matrix
- Kecepatan generator 60Hz dengan 1/16 kecepatan
- Kecepatan generator 64Hz dengan 5 tipe karakter
- 80 X 8 bit display data RAM
- Tipe display dot matrix

- Dilengkapi fungsi tambahan : Display clear, cursor home, display ON/OFF, cursor ON/ OFF, display character blink, cursor shift dan display shift
- Internal data
- Internal otomatis dan reset pada power ON
- +5 V power supply tunggal

Tabel 2.7. merupakan pin-pin LCD berserta konfigurasinya:

Tabel 2.7.
Pin-Pin LCD Dan Konfigurasinya

Nama pin	jumlah	I/O	Tujuan	Fungsi
DB0-DB3	4	I/O	MPU	Trisate bidirectional lower data bus: data dibaca dari modul ke MPU atau dari MPU ditulis ke modul melalui bus
DB4-DB7	4	I/O	MPU	Tristatebidirectional upper fourdata bus: data dibaca dari modul ke MPU atau dari MPU ditulis ke modul melalui bus
E	1	Input	MPU	Sinyal operasi dimulai: sinyal aktif baca/tulis
R/W	1	Input	MPU	Sinyalpilih data dan tulis (0:tulis,1:baca)
RS	1	-	Power supply	Sinyal pilih register 0: Instruction register (write) Busy flag dan addess counter (read) 1:Data register (write dan read)
Vo	1	-	Power supply	Penyetelan kontras pada tampilan LCD
VDD	1	-	Power supply	+ 5V
VSS	1	-	Power supply	Ground 0V
LEDA	1	-	Power supply	Led power supply (+5v)
LEDK	1	-	Power supply	Led power supply (0v)

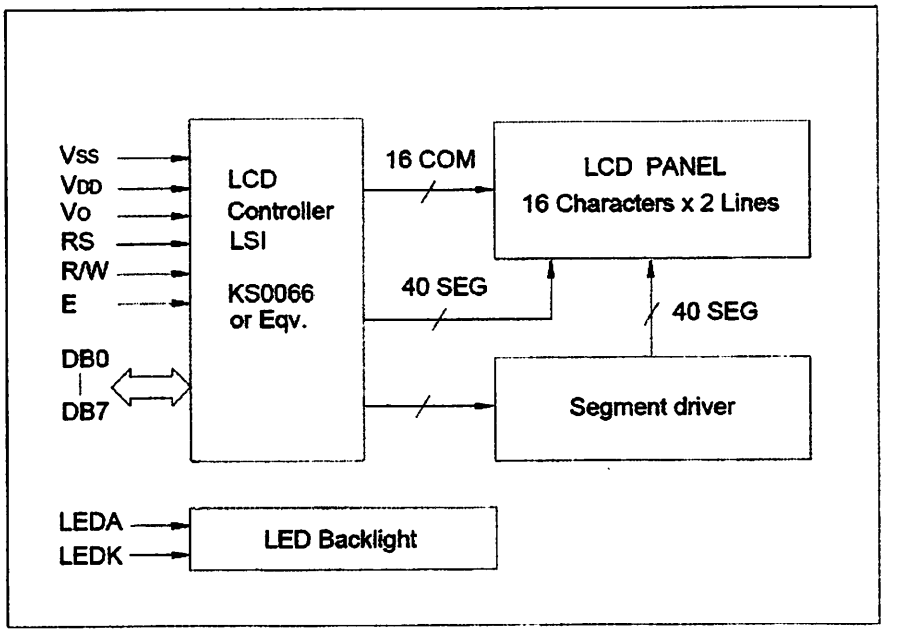
- Differenzierte Farbe- Schwarzwiedergabe: Display [illegible] [illegible] (Grafik) [illegible] [illegible] Farbe (DM-CRT) display [illegible] [illegible] [illegible] [illegible] display [illegible]
- Interne Uhr
- Internes Anschluß für zwei Joysticks [illegible] [illegible]
- [illegible] V [illegible] [illegible]

Tabelle 3.2: Programmierbare Parameter [illegible] [illegible] [illegible]:

Tabelle 3.2
Pin-Belegung [illegible]

Name pin	Sample	LED	Value	Function
DRC-DRS	0	[illegible]	[illegible]	[illegible]
DRA-DRF	1	[illegible]	[illegible]	[illegible]
[illegible]	1	[illegible]	[illegible]	[illegible]
[illegible]	1	[illegible]	[illegible]	[illegible]
[illegible]	1	-	[illegible]	[illegible]
[illegible]	1	-	[illegible]	[illegible]
[illegible]	1	-	[illegible]	[illegible]
[illegible]	1	-	[illegible]	[illegible]
[illegible]	1	-	[illegible]	[illegible]
[illegible]	1	-	[illegible]	[illegible]

2.5.1. Blog diagram dari LCD LMB162A



Gambar 2.7 Blog Diagram dari LMB162A

Register

Control LCD mempunyai 2 register 8 bit yaitu *Instruction register* (IR) dan *Data Register* (DR). Kedua register tersebut dipilih melalui *Register Select* (RS). IR menyimpan kode instruksi seperti *Display clear* dan *cursor shift*, dan alamat informasi dari *Display* Data RAM (DD RAM) dan karakter generator RAM (CG RAM).

DR menyimpan data sementara untuk ditulis ke DD RAM atau CG RAM, atau dibaca dari DD RAM atau CG RAM. Ketika data ditulis ke DD RAM atau CG RAM dari MPU, data di DR secara otomatis ditulis ke DD RAM atau CG RAM dengan operasi internal. Tetapi ketika data dibaca dari DD RAM atau CG RAM maka alamat data ditulis pada IR.Data tersebut akan dimasukkan ke DR dan MPU akan membaca data dari DR, Setelah operasi pembacaan, alamat berikutnya

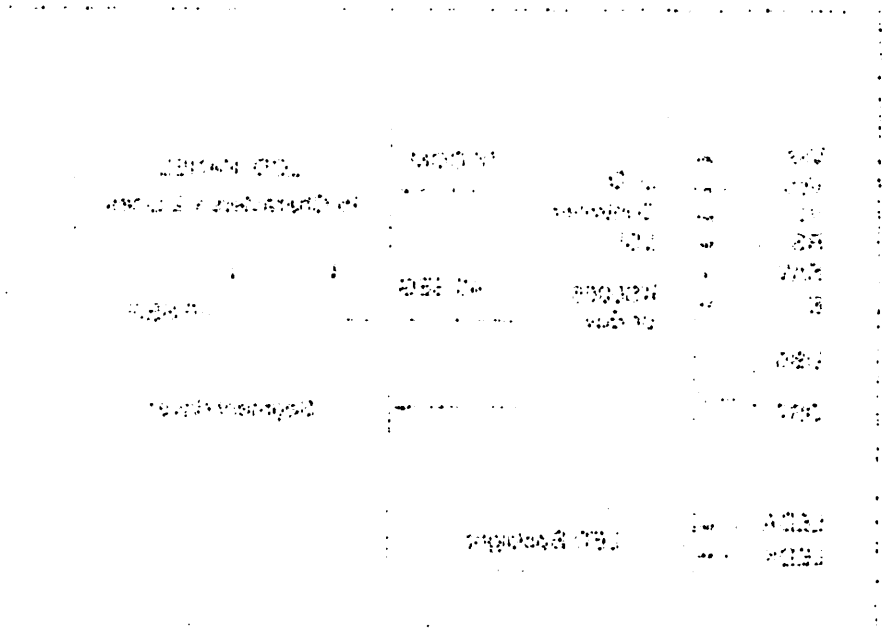


Abbildung 3.7 Blockdiagramm des LMS68040

Quellen

Es sind 1KB monoportiert 2 Register 8 bit breite Datenbus-Operation 32bit breite Adresse (DMA. Lesen Schreibe Register Bereich direkt mehrere digitale Ausgänge Verbindung zum Prozessor (PMA. Die monoportiert sind mehrere Speicherbereiche Speicherbereich Adresse und Daten Bereich Adressen und Daten Bus RAM (PD RAM) und Instruktion prozessor RAM (CD RAM)

Die Speicherbereiche dieser Instruktion erreichen Adresse bei CD RAM und PD RAM also Adressen und Daten RAM und CD RAM. Schreiben und Lesen bei CD RAM und PD RAM der Speicherbereich CD RAM ist 4 KB Speicherbereich direkt an CD RAM und CD RAM direkten operiert intern. Jeder Speicherbereich direkt an CD RAM und CD RAM mit einer eigenen Adresse und Daten Bus PD RAM Speicherbereich an CD RAM und PD RAM mit einer eigenen Adresse und Daten Bus. Jeder Speicherbereich direkt

diset data dari DD RAM atau CG RAM pada alamat tersebut akan dimasukkan ke DR untuk operasi berikutnya.

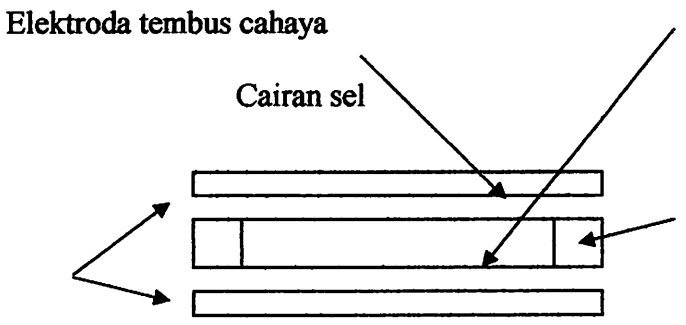
Display data RAM (DD RAM) mempunyai kapsitas area 80 X 8 bit. Beberapa area dari DDRAM yang tidak digunakan untuk display dapat digunakan sebagai General data RAM.

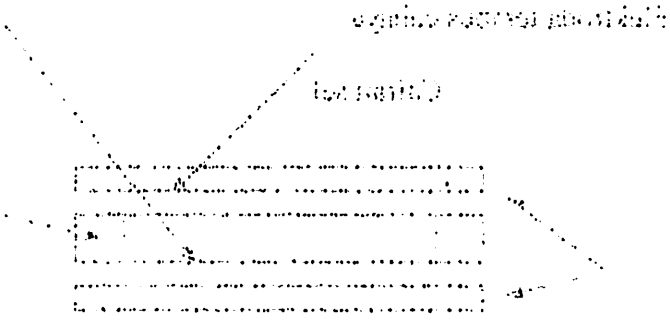
Pada LCD masing-masing pin mempunyai range alamat tersendiri, alamat itu diekspresikan dengan bilangan heksa. Untuk line 1 range alamat berkisar antara 00h-0fh sedangkan untuk line 2 alamat berkisar antara 40h-4fh

Encoder

Informasi atau data ada kalanya dikodekan dalam bentuk kode. Untuk mengkode data digital tersebut digunakan suatu encoder. Salah satu contoh dari encoder adalah encoder 16 to 4 line yang digunakan untuk mengkode 16 saluran data desimal menjadi 4 saluran data BCD. Keluaran encoder merupakan kode dari salah stu input yang diaktifkan. Endcoder mempunyai 2^N masukan dan N buah line keluaran.

Gambar 2.7. berikut ini merupakan konstruksi dari cairan sel kristal pada LCD :





Penyekat

Kaca

Gambar 2.8. Konstruksi dari Cairan Sel Kristal

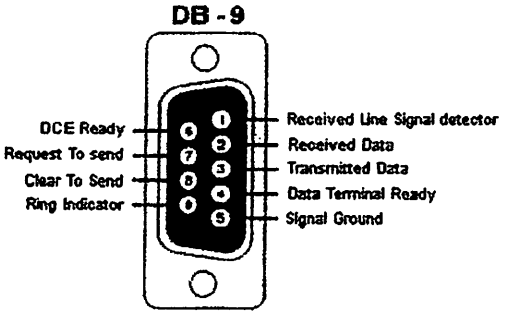
2.6. IC MAX 232

2.6.1. Interface

Interface merupakan suatu piranti yang dapat menghubungkan satu peralatan ke peralatan lain sehingga peralatan tersebut dapat berkomunikasi. Sedangkan suatu cara/proses untuk menghubungkan dua sistem yang berbeda agar bisa bekerja sama disebut interfacing.

2.6.2. Konfigurasi pin

Jika suatu komputer dihubungkan dengan komputer lain atau suatu periferal lain, maka bisa dilakukan hubungan komunikasi data. Sebuah komputer dapat bertukar informasi melalui *interface port I/O* serial yang disebut *interface* RS 232. RS 232 merupakan interface antara peralatan terminal data dan peralatan komunikasi data dengan menggunakan data biner serial sebagai data yang ditransmisikan. Salah satu konektor yang biasa digunakan untuk komunikasi serial ini adalah konektor DB 9. Konektor DB 9 ditunjukkan pada Gambar 2.8.



Gambar 2.8. Konektor DB 9

Pada dasarnya semua pin-pin memiliki fungsi-fungsi tetapi untuk keperluan RS 232 ini hanya beberapa saja yang penting.

Fungsi yang ada untuk konektor DB 9 adalah sebagaimana tampak dalam Tabel 2.8 berikut :

TABEL 2.8.

KONFIGURASI PIN DB 9

EIA 232 (RS 232) FUNCTION	PIN
Data Carrier Detect (DCD)	1
Received Data (RxD)	2
Transmitted Data (TxD)	3
Data Terminal Ready (DTR)	4
Sinyal Ground (GND)	5
Data Set Ready (DSR)	6
Request To Send (RTS)	7
Clear To Send (CTS)	8
Ring Indikator (RI)	9

Jalur data (TxD dan RxD) untuk transport data, TxD adalah jalur output pada komputer, data dikirim dari pin ini. Sedangkan RxD adalah penerima untuk komputer, data yang datang akan diterima oleh pin ini. Pin ke empat adalah

output (RTS) di mana sebuah sinyal akan diberikan pada alat yang dihubungkan dengan maksud meminta kiriman data. CTS adalah sinyal masukan yang menunggu sinyal dari alat yang terhubung. Ketika alat tersebut menerima sinyal RTS dan bisa menerima data maka ia akan mengirimkan sinyal balik yang merupakan CTS. DTR adalah sinyal keluaran yang memberi tanda bahwa ada alat yang terhubung dan akan mengirimkan data. DSR merupakan sinyal input yang mana jika alat yang terhubung manerima sinyal DTR ia akan memberi sinyal balik kemudian diterima sebagai sinyal DSR.

2.6.3. Protokol Komunikasi pada RS 232

Beberapa protokol dalam interface RS 232 adalah:

- Start Bit

  Merupakan sebuah bit dengan logic "0" dimana bit ini yang menandakan bahwa akan ada karakter atau data yang mengikutinya. Bit ini langsung diberikan oleh sinyal device tanpa harus mensetnya terlebih dahulu.

- Data Bit

  Merupakan bit yang mewakili dari karakter yang diikutinya *data bit* ini dapat diset sepanjang antara 5 sampai 8 bit.

- Pariti Bit

  Merupakan bit yang digunakan sebagai *error checking* pada *receiver* , apabila terjadi kesalahan maka *receiver* akan menset *error flag* (parity error) pada special register. *Parity bit* ini menghitung jumlah data yang

output (PCB) di mana sebuah sinyal akan dibaca ke suatu alat yang dikendalikan dengan mikroprosesor menggunakan bahasa C++. Sinyal analog masukan yang masuk ke dalam pin yang terhubung kepada alat mikroprosesor akan sinyal RTD dan fase masukan dan suatu ia akan diterjemahkan sinyal listrik yang merupakan CTS 1000 adalah sinyal keluaran yang masukan suatu lahan sebagai yang terhubung dan akan menyimpankan data. ESP8266 menjadikan sinyal input yang masuk pada alat yang terhubung masukan sinyal CTS 1000 ke dalam mikroprosesor sinyal listrik kemudian dimasukan sebagai sinyal CTS.

3.4.3. Prototipe Identifikasi pada Tahap 3.2.2

Beberapa prototipe dalam subsistem 3.2.2 adalah :

- Alat 1(a)

Merupakan sebuah alat dengan fungsi "0" ketika lift ini yang mencondisikan bahwa akan sebelum alat suatu yang mengantarkan lift ini bergerak dibawah oleh sinyal dengan tanpa suatu masukan sebelah atasnya

- Alat 1(b)

Merupakan lift yang mencondisi oleh sinyal yang dikirimkan dari lift dengan dibuat sebagai antara 1 sampai 8 ke

- Alat 1(c)

Merupakan lift yang dipasangkan sebagai [illegible] pada [illegible] dapatkan tegang kesalahan pada [illegible] [illegible] yang [illegible] pada [illegible] dengan [illegible] dan [illegible] dengan [illegible] yang

berlogic '1' pada data bit. Perhitungan jumlah data bit tersebut tergantung dari jenis *parity* yang diset. Untuk parity *EVEN* maka jumlah data bit yang berlogic '1' ditambah dengan *parity bit* akan menghasilkan jumlah yang ganjil. Sedangkan untuk *parity MARK* merupakan *parity bit* selalu berlogic '1' begitu pula pada space, parity bit selalu berlogic ' 0' dan *parity NONE* disini *parity bit* yang diabaikan.

- Stop Bit

  Merupakan bit yang menandakan akhir dari suatu paket data (biasanya 1 byte data). Seperti pada start bit, bit ini langsung diberikan dari serial device. *Stop bit* ini dapat diset panjangnya menjadi satu bit, satu setengah dan dua bit.

- Baut Rate

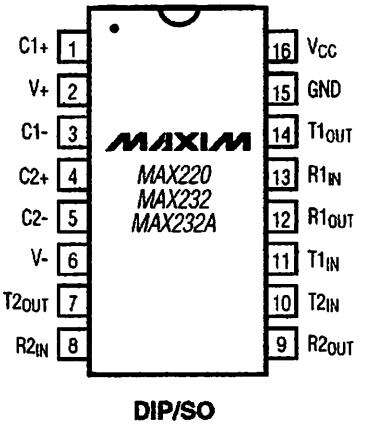
  Sebenarnya *baut rate* berarti pergantian kondisi tiap detik *(State Change of the Line persecond),* tetapi karena hanya ada 2 kondisi pada serial *(logic* 0 *dan 1)* maka dapat juga digunakan untuk menunjukkan kecepatan dari transmisi *(bits per second).*

Saluran data pada port seri PC menggunakan standard RS232, dimana logic 0 (low) dinyatakan sebagai tegangan antara +3 Volt sampai +10 Volt dan logic 1 (high) dinyatakan sebagai tegangan antara -3 Volt sampai -10 Volt. Level tegangan ini tidak sesuai dengan level tegangan yang dipakai pada port seri

AT89C51 yang menggunakan standard TTL (Transistor Transistor Logic), yaitu level tegangan baku dalam rangkaian – rangkaian digital.

Dalam standar TTL logic 0 (low) dinyatakan sebagai tegangan antara 0 Volt sampai 0.8 Volt, dan logic 1 (high) dinyatakan sebagai tegangan antara 3.5 Volt sampai 5 Volt. Karena perbedaan tegangan tersebut, agar port seri PC tidak merusak port seri AT89C51 antara keduanya dipasangkan IC MAX232 sebagai penyesuai tegangan.

Konfigurasi Pin IC MAX232 dapat di lihat pada Gambar 2.9 berikut ini :



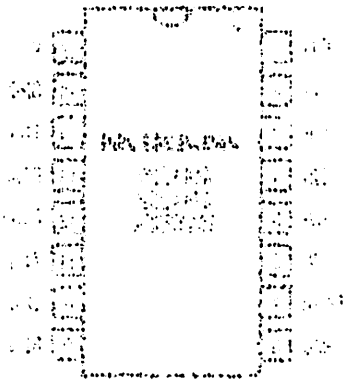
Gambar 2.9. Konfigurasi Pin IC MAX232

Rangkaian dasar dari MAX 232 dapat dilihat pada Gambar 2.10 berikut ini:

ATMEL's very microprocessor standard TTL / transistor Transistor Logic, yaitu level logic pada dalam mengadakan – tanpa kan digital.

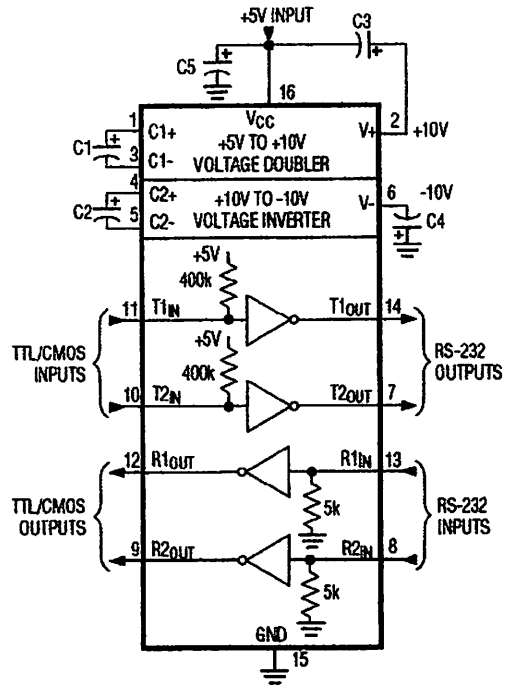
Dalam standar TTL, logic 0 (low) dinyatakan sebagai logic pada antara 0 Volt sampai 0,8 Volt, dan logic 1 (high) dinyatakan sebagai logic pada antara 2,4 Volt sampai 5 Volt. Karena perbedaan tegangan masukan, dapat pula kan IC tidak mampu pada ATMEL(3) antara keluaran dipasangkan IC MAX232 sebagai penerima dipindah.

Konfigurasi Pin IC MAX232 dapat dilihat pada Gambar 2.9 berikut ini



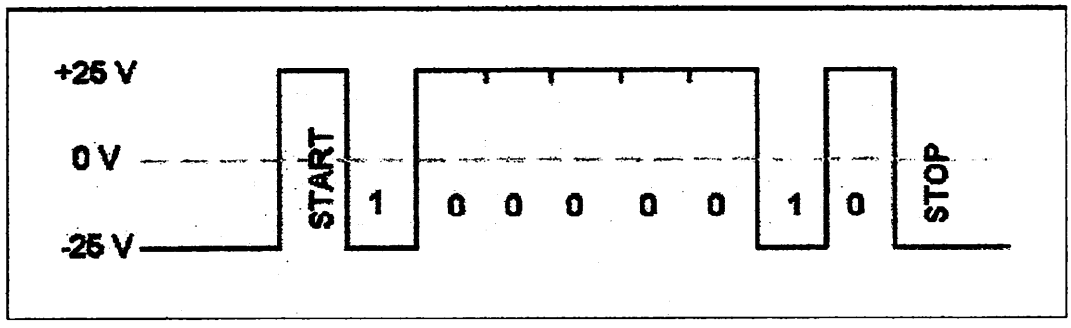
Gambar 2.9. Konfigurasi Pin IC MAX232

Keunggulan dari dari MAX 232 dapat dilihat pada Gambar 2.10 berikut ini.

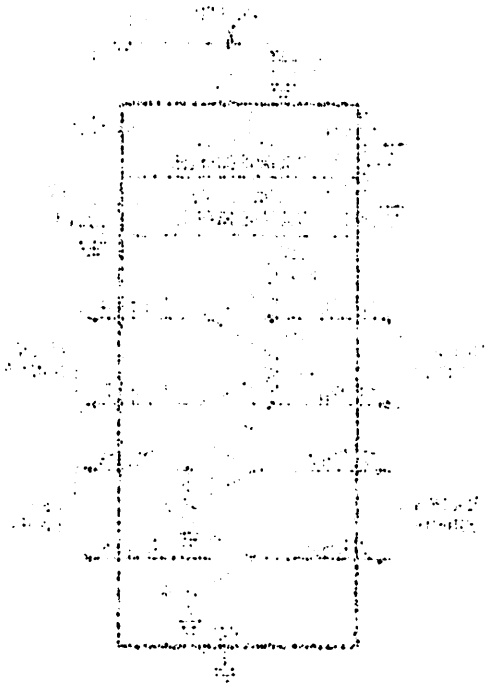


Gambar 2.10. Rangkaian Operasi MAX 232

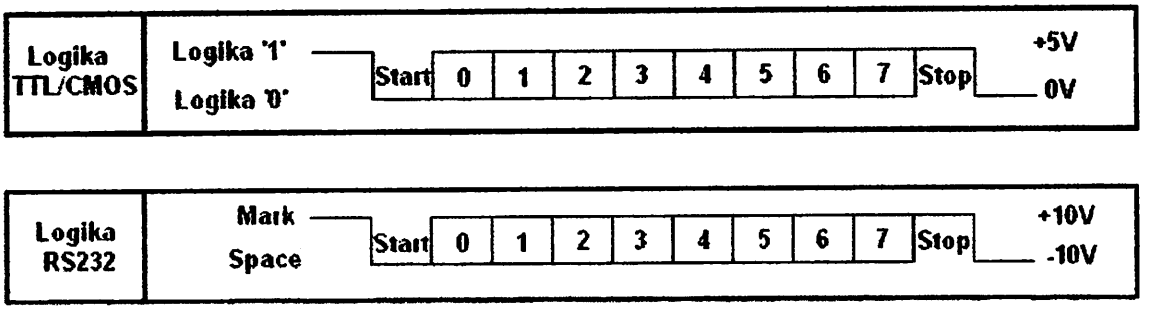
Gambar berikut ini adalah contoh level tegangan RS-232 pada pengiriman huruf 'A' dalam format ASCII tanpa bit paritas.



Gambar 2.11 : Level tegangan RS-232 pada pengiriman huruf 'A' tanpa bit paritas

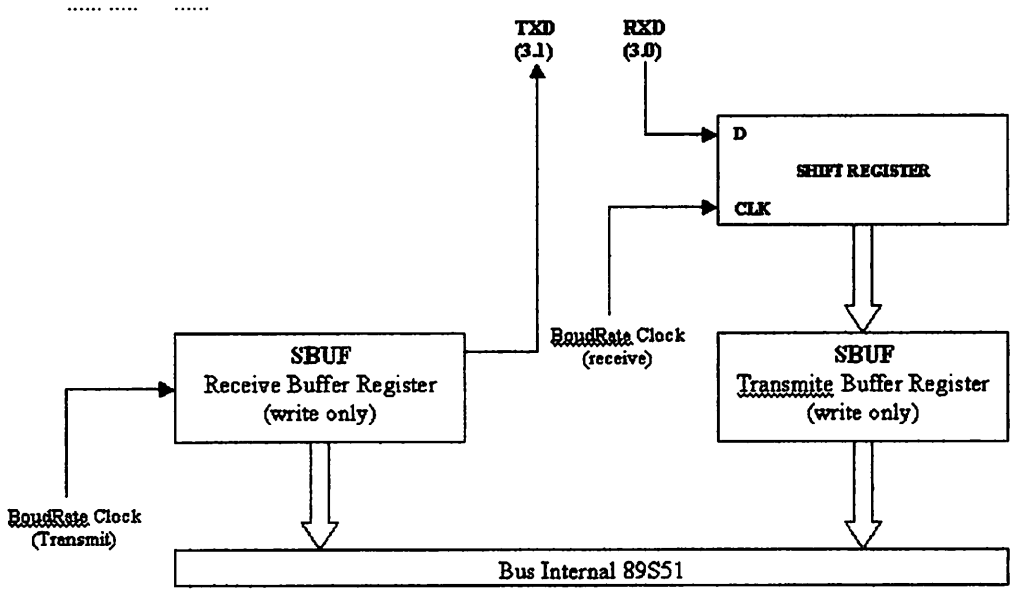


Logika RS232 muncul pada kaki Transmit (TD), Receive (RD) dan kaki gerbang yang lain (RTS, CTS, DCD dan sebagainya).



Gambar 2.12. Aras tegangan logika TTL dan CMOS pada gerbang seri Pulsa.

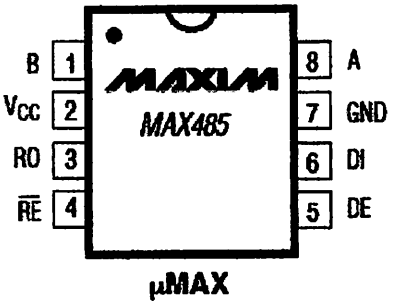
Berikut ini adalah Gambar 2.13. merupakan blog diagram gerbang untuk komunikasi serial pada Mikrokontroller AT89S51 :



Gambar 2.13. Blog diagram Gerbang untuk Komunikasi Seri

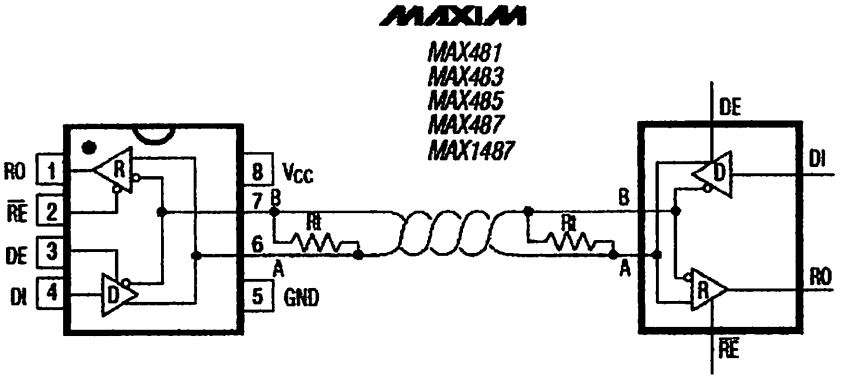
2.7. IC MAX 485

IC (*Integrated Circuit*) untuk serial RS-485 yang digunakan dalam Skripsi ini adalah jenis IC MAX 485 (Gambar 2.11.). IC ini memenuhi standar RS-485 yang dikeluarkan oleh *Maxim.*



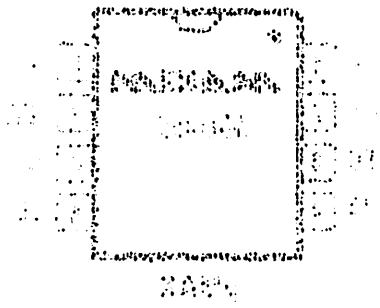
Gambar 2.14. IC MAX 485

Gambar 2.12. berikut ini merupakan Typical Operating Circuit dari IC Max 485 :



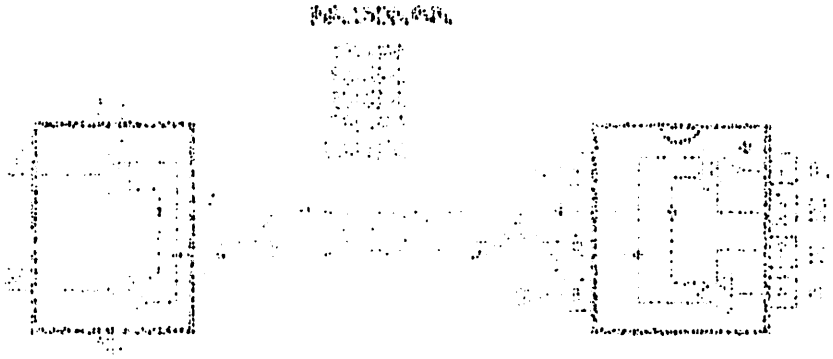
Gambar 2.15. Typical Operating Circuit

Jika diperhatikan dalam Gambar 2.12., *output* dan *complementary output* dari *driver* maupun *receiver* digabung manjadi satu secara internal dalam IC. Ini menunjukkan bahwa IC MAX 485 dirancang untuk sistem *2-wire* (*half-duplex*). Kelebihan IC MAX 485 adalah adanya antisipasi terhadap kondisi *fail-safe* yakni



Gambar 2.14. IC MAX 485

Gambar 2.15. Contoh IC MAX 485 sebagai Operasing Circuit dan IC Sejenis 485



Gambar 2.16. Typical Operating Circuit

Ada dipentukan dalam Gambar 2.16. Ketika dua operasional amplifier dan diterima masukan co-mode digitalnya maka akan keluar internal dalam IC. Ini menyebabkan bahwa IC MAX 485 dirancang untuk [illegible] Kesatuan IC MAX 485 sebagai adanya [illegible] pada

kondisi dimana bus jaringan berada dalam keadaan terbuka. Keadaan ini dapat disebabkan terputusnya jaringan atau karena seluruh *node* berada dalam keadaan siap menerima data sehingga tidak ada satu pun *driver* yang aktif. Secara otomatis *output* dari *receiver* memiliki logika 1, yang jika diterjemahkan dalam komunikasi serial adalah kondisi *idle*. Sifat ini menyebabkan IC MAX 485 tidak memerlukan tambahan resistor bias lagi yang biasanya digunakan untuk melakukan *pull up* dan *pull down* dalam bus jaringan, agar *output receiver* berada dalam kondisi *idle*.

2.8. SENSOR HALL EFECT A276

2.8.1. Detektor Medan Magnet Dengan Hall Effect Sensor

Medan magnet atau sering dikatakan dengan magnetic field itu tidak dapat dirasakan oleh indra manusia. Detektor medan magnet tidaklah terlalu sukar untuk dibuat namun cukup memiliki kepekaan yang cukup baik.

Untuk membuat detektor medan magnet ini tidak membutuhkan banyak komponen sehingga mudah dibuat dan tidak membutuhkan biaya yang banyak tetapi menghasilkan kepekaan yang baik. Detektor medan magnet di dalam skripsi ini tidaklah dititikberatkan pada ketelitian pengukuran tetapi pada ada tidaknya medan magnet dalam radius sekitar 10 cm yang mempunyai kekutaan medan magnet konstan atau berubah dengan frekuensi yang tidak terlalu tinggi, sekitar sampai 20KHz.

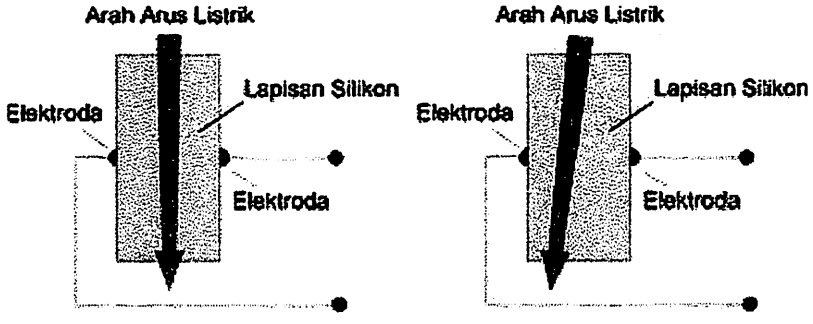
2.8.2. *Hall Effect* Sensor

Hall effect sensor merupakan sensor yang digunakan untuk mendeteksi medan magnet. *Hall Effect* sensor akan menghasilkan sebuah tegangan yang proporsional dengan kekuatan medan magnet yang diterima oleh sensor tersebut.

Pendeteksian perubahan kekuatan medan magnet cukup mudah dan tidak memerlukan apapun selain sebuah induktor yang berfungsi sebagai sensornya. Kelemahan dari detektor dengan menggunakan induktor adalah kekuatan medan magnet yang statis (kekuatan medan magnetnya tidak berubah) tidak dapat dideteksi.

Oleh sebab itu diperlukan cara yang lain untuk mendeteksinya yaitu dengan sensor yang dinamakan dengan '*hall effect*' sensor. Sensor ini terdiri dari sebuah lapisan silikon yang berfungsi untuk mengalirkan arus listrik.

Gambar 2.13 berikut ini merupakan konfigurasi dari Hall Effect Sensor :



Gambar 2.16 konfigurasi Hall Effect Sensor

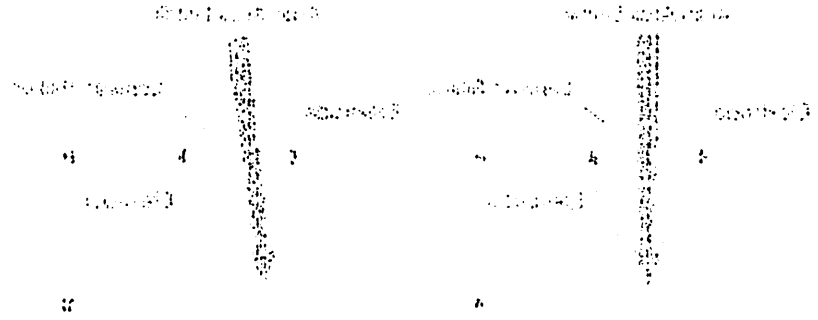
Sensor *hall effect* ini hanya terdiri dari sebuah lapisan silikon dan dua buah elektroda pada masing-masing sisi silikon. Hal ini akan menghasilkan perbedaan tegangan pada outputnya ketika lapisan silikon ini dialiri oleh arus

Hall effect sensor mengadopsi sensor yang si gunakan untuk mendeteksi medan magnet. Hall effect sensor akan mengindentifikasi adanya keberadaan yang proporsional dengan kekuatan medan magnet yang dikenalnya oleh sensor tersebut.

Analisa sensor produksi kebutuhan medan sangat cukup mudah dan tidak memerlukan peralatan khusus untuk indikator yang lentingkan adalah konstanta. Kelemahan dari diantara dengan menggunakan indikator adalah kekurang medan magnet yang ada. Kebutuhan medan magnetnya lebih banyak. Tidak akan dideteksi.

Dari sebab itu diperlukan cara yang lain untuk mendeteksi arus yaitu dengan sensor yang dikenalkan dengan "Hall effect" sensor. Sensor ini terdiri dari sebuah lapisan silikon yang ditempel antara konfigurasi sensor tersebut.

Gambar 3.13 Contoh di sensor/medan konfigurasi dari Hall Effect Sensor



Gambar 3.14 konfigurasi Hall Effect Sensor

Sensor ini efektif ini terus terdiri dari sebuah lapisan silikon dan dua lapisan elektroda pada sisi-sisinya yang sama. Hal ini akan menghasilkan perbedaan tegangan pada elektroda-elektroda tersebut ketika ia dialiri oleh arus

listrik. Tanpa adanya pengaruh dari medan magnet maka arus yang mengalir pada silikon tersebut akan tepat ditengah-tengah silikon dan menghasilkan tegangan yang sama antara elektrode sebelah kiri dan elektrode sebelah kanan sehingga menghasilkan tegangan beda tegangan 0 volt pada outputnya.

Ketika terdapat medan magnet mempengaruhi sensor ini maka arus yang mengalir akan berbelok mendekati/menjauhi sisi yang dipengaruhi oleh medan magnet. Ketika arus yang melalui lapisan silikon tersebut mendekati sisi silikon sebelah kiri maka terjadi ketidakseimbangan tegagan output dan hal ini akan menghasilkan sebuah beda tegangan di outputnya.

Semakin besar kekuatan medan magnet yang mempengaruhi sensor ini akan menyebabkan pembelokan arus di dalam lapisan silikon ini akan semakin besar dan semakin besar pula ketidakseimbangan tegangan antara kedua sisi lapisan silikon pada sensor. Semakin besar ketidakseimbangan tegangan ini akan menghasilkan beda tegangan yang semakin besar pada output sensor ini.

Arah pembelokan arah arus pada lapisan silikon ini dapat digunakan untuk mengetahui polaritas kutub medan *hall effect* sensor ini. Sensor *hall effect* ini dapat bekerja jika hanya salah satu sisi yang dipengaruhi oleh medan magnet. Jika kedua sisi silikon dipengaruhi oleh medan magnet maka arah arus tidak akan dipengaruhi oleh medan magnet itu. Oleh sebab itu jika kedua sisi silikon dipengaruhi oleh medan magnet yang mempengaruhi magnet maka tegangan outputnya tidak akan berubah.

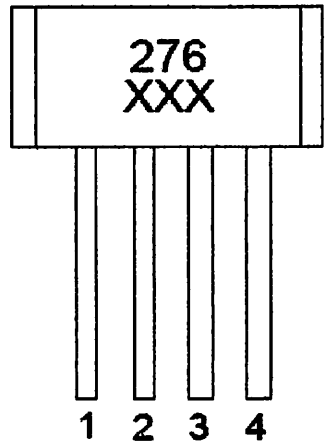
Sensor yang digunakan di dalam Skripsi ini adalah sensor A276 (Gambar 2.14). Sensor ini akan menghasilkan tegangan yang proporsional dengan kekuatan medan magnet yang dideteksi oleh sensor ini. Selain itu komponen ini dipilih karena relatif murah, mudah digunakan dan mempunyai performa yang cukup baik. Sensor A276 ini mempunyai 4 pin antara lain :

Pin 1 : VCC, pin tegangan suplai

Pin 3 : D0B, pin tegangan output.

Pin2 : DO, pin tegangan output.

Pin 4 : VSS, pin ground.

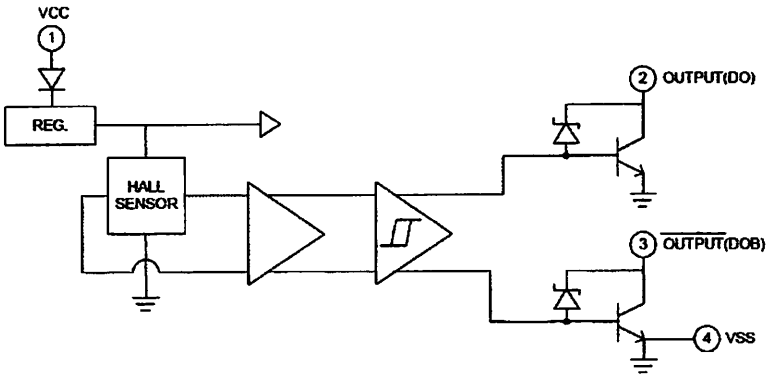


Gambar 2.17 Hall Effect Sensor A276

Di dalam sensor ini sudah dibangun sebuah penguat yang memperkuat sinyal dari rangkaian sensor dan menghasilkan tegangan output ditengah-tengah tegangan suplai. Pada sensor ini jika mendapat pengaruh medan magnet dengan polaritas kutub utara maka akan menghasilkan pengurangan pada tegangan output

sebaliknya jika terdapat pengaruh medan magnet dengan polaritas kutub selatan maka akan menghasilkan peningkatan tegangan pada outputnya. Sensor ini dapat merespon perubahan kekuatan medan magnet mulai kekuatan medan magnet yang statis maupun kekuatan medan magnet yang berubah-ubah dengan frekuensi sampai 20KHz.

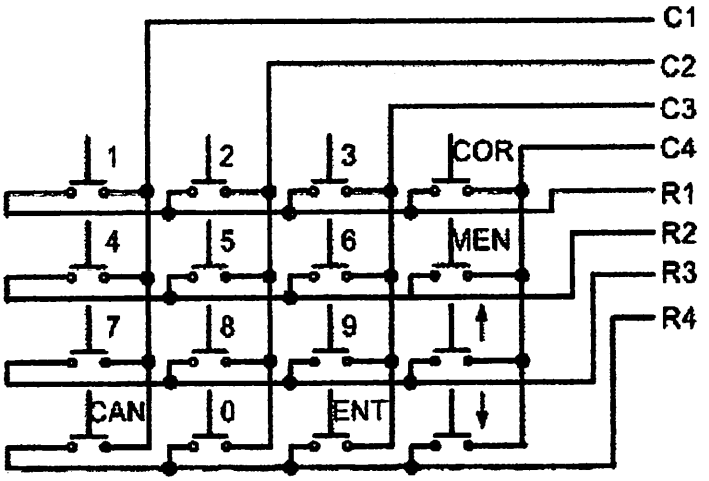
Gambar 2.15 berikut ini merupakan blog diagram dari hall effect sensor A276 :



Gambar 2.18. Blok Diagram Hall Effect Sensor A276

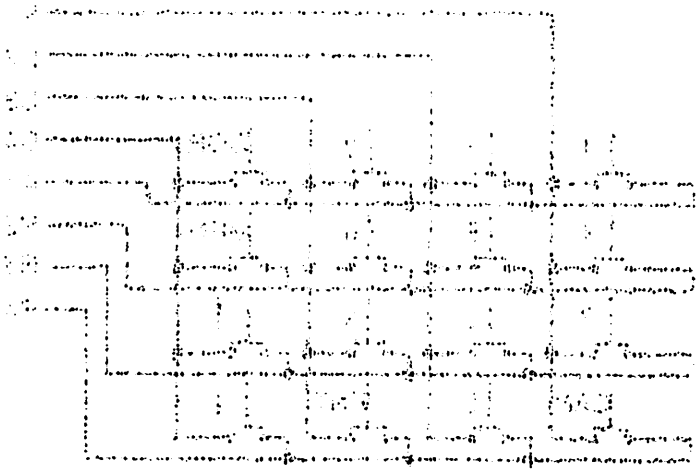
Sensor hall effect A267 ini mempunyai suplai tegangan yang cukup lebar yaitu mulai 3,5 sampai 20V dengan kepekaan perubahan kekuatan medan magnet sampai frekuensi 23KHz.

2.9. KEYPAD 4X4



Gambar 2.19 Rangkaian dasar keypad 4x4

Keypad serig digunakan sebagi suatu input pada beberapa peralatan yang berbasis mikroprosessor atau mikrokontroller. Keypad sesungguhnya terdiri dari sejumlah saklar, yang terhubung sebagai baris dan kolom dengan susuan seperti yang ditunjukkan pada Gambar 2.16. Agar mikrokontroller dapat melakukan scan keypad, maka port mengeluarkan salah satu bit dari 4 bit yang terhubung pada kolom dengan logika low "0" dan selanjutnya membaca 4 bit pada baris untuk menguji jika ada tombol yang ditekan pada kolom tersebut. Sebagai konsekuensi, selama tidak ada tombol yang ditekan, maka mikrokontroller akan melihat sebagai logika high "1" pada setiap pin yang terhubung ke baris.



Gambar 3.16 Hasil rutean dari layout 1a

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

3.1. Umum

Pada pengerjaan skripsi ini, Mikrokontroller yang meliputi software / hardware. Sebelum membahas tentang perencanaan dan pembuatan, maka harus ada perencanaan yang matang agar sistem dapat direalisasikan dengan baik sesuai target. Oleh karena itu perlu kita perhatikan juga hardware yang hendak dikontrol.

3.2. Perencanaan Sistem Kerja

Prinsip kerja dari penghitung otomatis pembacaan meteran air minum jarak jauh ini adalah sistem penerimaan beda tegangan pada output sensor hall effect yang berasal dari flow meter. Jika sensor pada flow meter ini mendapat pengaruh medan magnet dengan polaritas kutub utara maka akan menghasilkan pengurangan pada tegangan output sebaliknya jika terdapat pengaruh medan magnet dengan polaritas kutub selatan maka akan menghasilkan peningkatan tegangan pada outputnya. Didalam pengiriman data counter sebuah Mikrokontroller AT89S51 berfungsi untuk mengidentifikasikan data yang masuk dan mengolah data tersebut sehingga menghasilkan data counter yang sesuai dengan data yang terdapat pada flow meter, maka pada flow meter juaga diberikan sebuah LCD yang berfungsi sebagai tampilan untuk menampilkan data yang berasal dari mikrokontroller, sesuai data yang

BAB III

PERENCANAAN DAN PEMBAHASAN

3.1. Umum

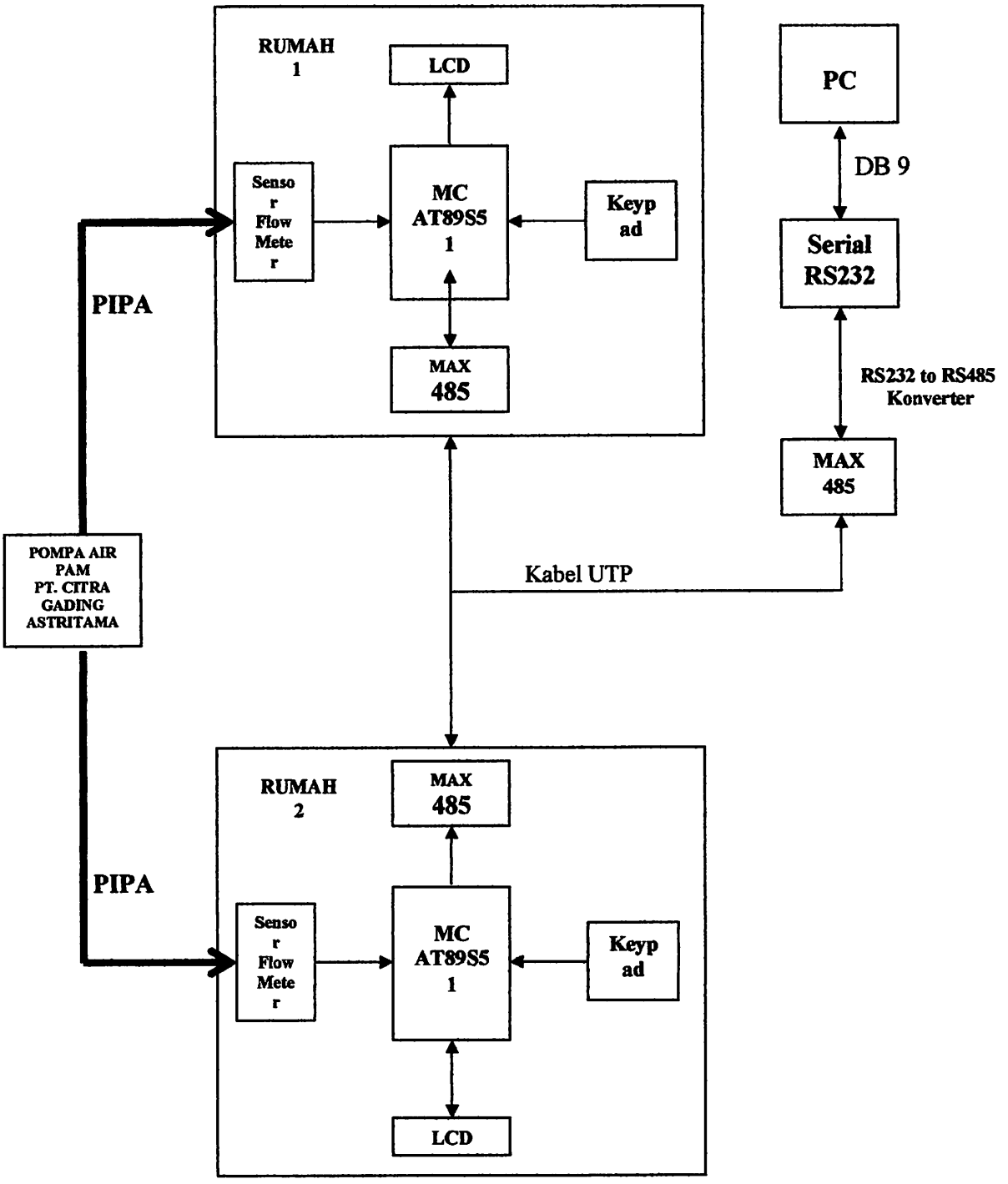
Pada pengujian alat ini, [illegible] yang [illegible] [illegible] [illegible]

dihasilkan oleh flow meter tersebut yaitu berupa jumlah putaran yang dihasilkan oleh piringan yang terdapat pada Transmiter Water meter.

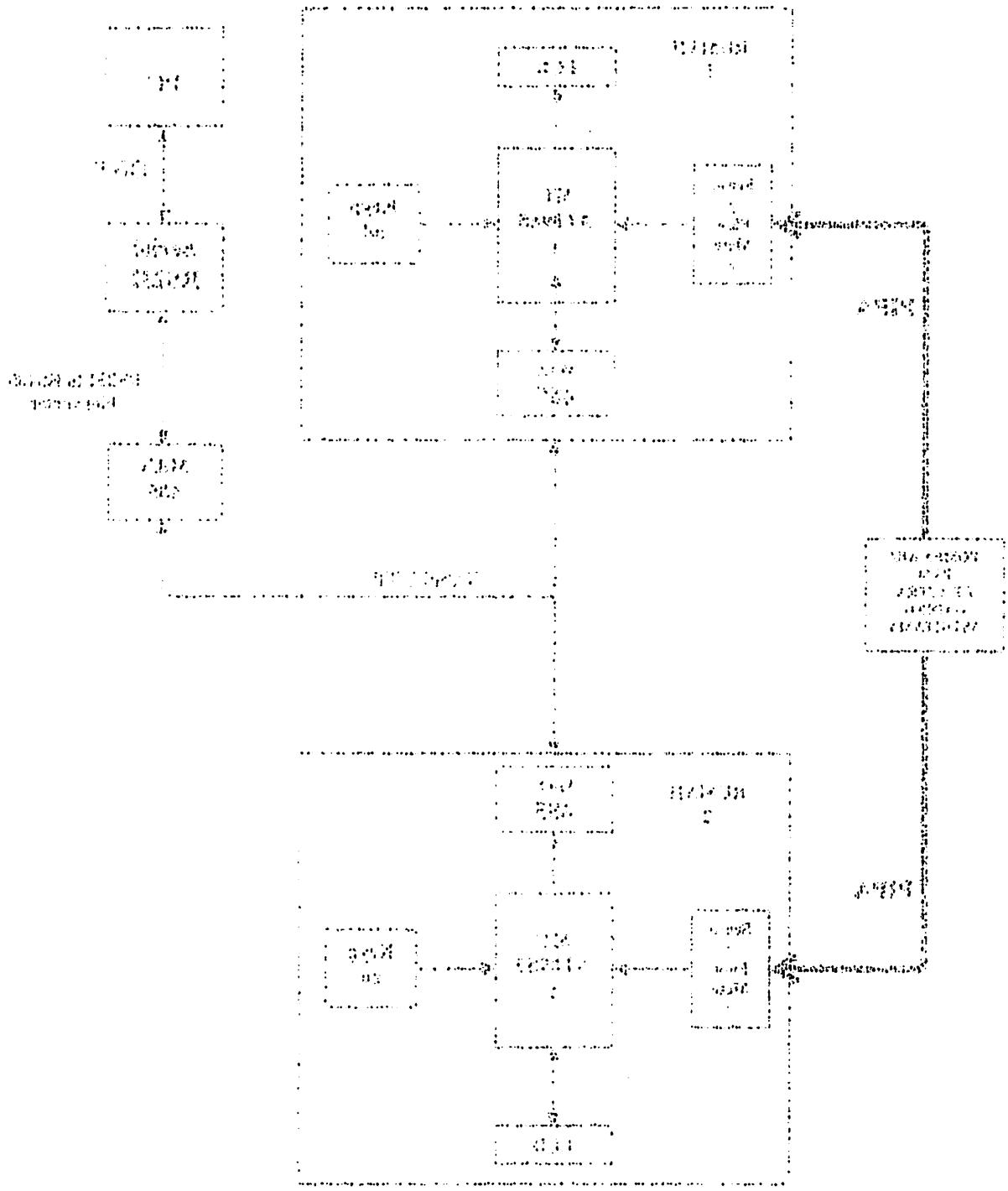
Data yang diambil akan disimpan ke dalam memori AT89S51, yang nantinya selain data dalam memori tersebut dapat ditampilkan dalam PC melalui port RS 232, disamping dapat dilihat secara langsung dari LCD. Selain mengolah data counter pada flow meter, AT89S51 juga berfungsi sebagai proses data tagihan pembayaran dan request data KWH meter. Proses request data diawali oleh konsumen dengan memilih menu yang akan dipilih melalui keypad yang ditampilkan ke dalam LCD. Setelah konsumen tersebut menekan tombol SEND pada keypad. Data tersebut kemudian dikirim melalui RS 232 menuju komputer yang ada di server. Kemudian dari komputer yang ada di server ini akan memproses request data yang berisikan tagihan 1 bulan lalu atau request tagihan bulan pada saat ini dan di tampilkan pada LCD konsumen.

Sistem ini menggunakan 1 buah komputer, dua buah rangkaian minimum Mikrokontroller AT89S51 sebagai simulasi rumah 1 dan 2, satu buah LCD, dua buah sensor hall effect dan satu buah keypad.

Perangkat penghitung otomatis pembacaan meteran air minum jarak jauh ini dapat digambarkan secara blok diagram seperti pada gambar 3.1 :



Gambar 3.1. Diagram blok Receiver water meter digital



Fungsi dari masing-masing rangkaian subsistem dalam gambar di atas adalah sebagai berikut :

- **Rumah**

Sebagai pelanggan Perusahaan Air Minum (PAM) CV.CITRA ARTISTIK di Perumahan Tirtasani Estate.

- **Sensor Flowmeter**

Digunakan untuk mendeteksi volume air masuk dan menambah 1 data counter (data komulatif) ke Mikrokontroller.

- **PAM PT. CITRA GADING ASTRITAMA**

Sebagai Perusahaan Air Minum di Perumahan Tirtasani Estate.

- **LCD**

Sebagai tampilan pada sistem perhitungan otomatis pembacaan meteran air minum.

- **Mikrokontroller AT89S51**

Digunakan untuk menambah data counter komulatif pada setiap perubahan logic yang di terima dari sensor.

- **MAX 485**

Digunakan untuk level Converter yang berfungsi menambah level data serial TTL menjadi level RS 485.

- **PC**

Digunakan sebagai pengolah data pada sistem perhitungan otomatis pembacaan meteran air minum yang di inputkan dari mikrokontroller.

- **Keypad (4x4)**

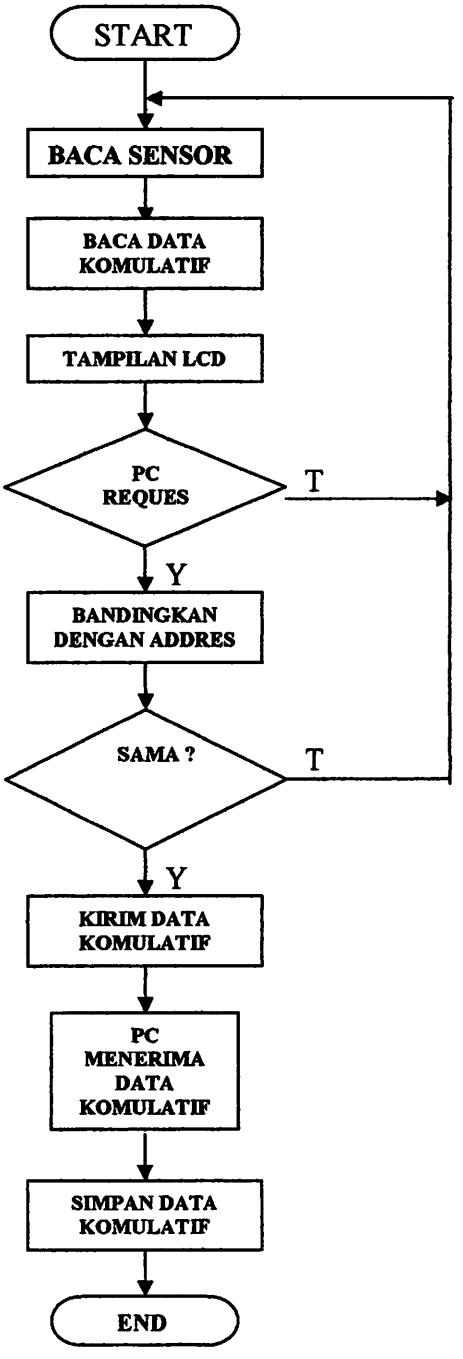
Digunakan untuk menampilkan data yang dimasukkan dari konsumen dari keypad ke LCD dan PC.

- **Serial RS 232**

Sebagai penghubung MAX 485 dari mikrokontroller ke PC.

Pengendalian seluruh sistem terletak pada Mikrokontroller AT89S51. dimana Mikrokontroller harus mampu mengintegrasikan seluruh alamat kerja dari alat alat pendukungnya seperti masukan dari keypad yang selanjutnya dikeluarkan melalui LCD dan dikirim melalui Port RJ 11, kabel serial DB9 ke komputer. Kode dimasukkan melalui keypad berupa tombol tombol angka dari 0 sampai 9 ditambah tombol tombol lain yang dapat difungsikan antara lain untuk CAN,COR, ENT, MEN, UP, dan DOWN.

Berikut ini Gambar 3.2. merupakan *flowchart* dari sistem yang dipakai dalam Skripsi :



Gambar 3.2 Flowchart Keseluruhan Sistem

3.3. Perancangan Perangkat Keras

3.3.1. Mikrokontroller AT89S51

3.3.1.1.Mikrokontroller sebagai sistem minimum

Pada bagian ini akan dibahas tentang perancangan perangkat keras yang terdiri dari Rangkaian Minimum AT89S51, Rangkaian Keypad, Rangkaian LCD, Rangkaian sensor hall effect, Rangkaian RS 485 dan konektor RJ 11. Rangkaian tersebut tersusun dari komponen-komponen 3 buah kapasitor, sebuah resistor dan sebuah kristal atau resonator keramik. Rangkaian kapasitor dan kristal atau resonator keramik digunakan sebagai rangkaian pembangkit internal clock generator yang terdapat pada AT89S51. Nilai kapasitansi ditentukan sesuai dengan jenis oscilator yang digunakan, yaitu:

C1 dan C2 = 20pF – 40pF untuk kristal

C1 dan C2 = 30pF – 50pF untuk resonator keramik.

Karena dalam rancangan digunakan oscilator kristal maka harga kapasitor yang di gunakan adalah sebesar 33pF.

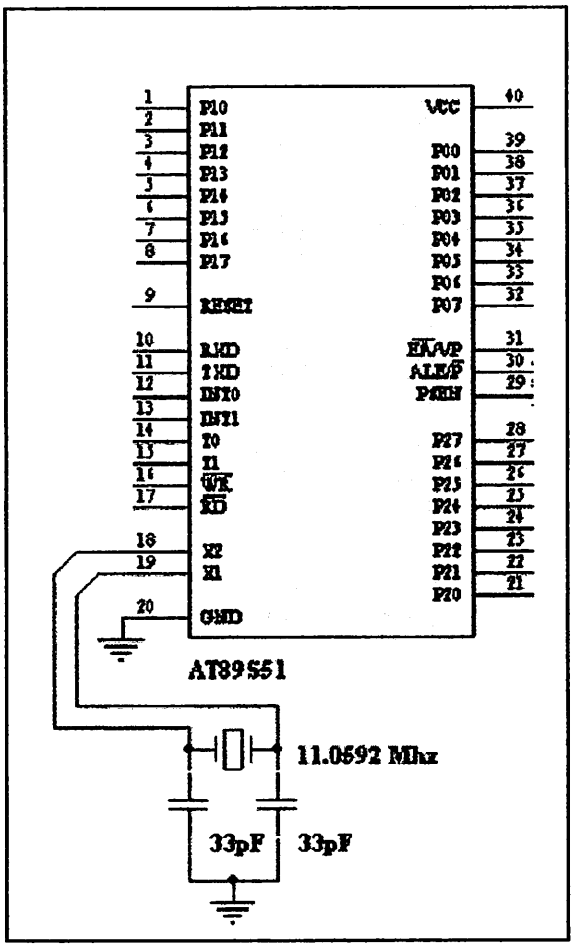
Mikrokontroller AT89S51 mempunyai frekwensi maksimal 12 MHz, dimana 1 siklus mesin = 12 clock. Dalam rangkaian digunakan kristal dengan harga 11,0592 MHz, maka program akan dijalankan pada setiap langkahnya selama 1,085 μs. Siklus tersebut diambil berdasarkan ketentuan mikrokontroller AT89S51 yaitu 12 clock = 1 siklus mesin, sedangkan frekwensi yang digunakan 12 MHz, maka waktu yang

dipakai dalam setiap 1 siklus mesin adalah 1μs. Dengan demikian perhitungannya dapat dilihat sebagai berikut:

$f = 11{,}0592$ MHz $\qquad T = \frac{1}{f} \qquad T = \frac{1}{11{,}0592 \times 10^6}$

Karena 1 siklus mesin = 12T maka,

$$1 \text{ siklus mesin} = 12 \times \frac{1}{11.0592 \times 10^6} = 1{,}085\ \mu s.$$

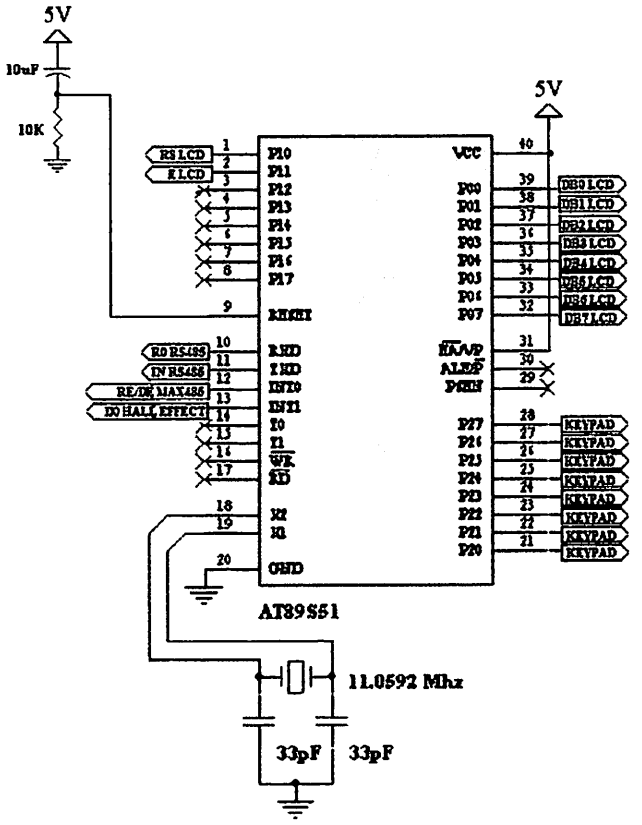


Gambar 3.3. Rangkaian Minimum Sistem Mikrokontroller AT89S51

3.3.1.2. Perencanaan Port-Port Pada Mikrokontoller AT89S51

Pada skripsi ini IC mikrokontroller AT89S51 digunakan sebagai pusat pengendali kerja dari alat yang dibuat karena pada IC inilah akan disimpan program-program *(software)* perintah serta alamat yang akan dituju program. Untuk melaksanakan fungsi tersebut diatas maka perlu dirancang port-port I/O serta sinyal-sinyal yang akan digunakan dengan seksama.

Gambar 3.4. menunjukkan rancangan port-port I/O serta sinyal-sinyal pada IC mikrokontroller AT89S51 yang dimanfaatkan pada skripsi ini.



Gambar 3.4. Rancangan Pemakaian Port-Port Mikrokontroller AT89S51

- **Port 0**

Port 0 merupakan port dua fungsi yang berada pada pin 32-39 dari IC AT89S51. Dalam perancangan, P0.0-P0.7 digunakan sebagai port keluaran ke LCD.

- **Port 1**

Port 1 disediakan sebagai port I/O dan menempati pin 1-8, dalam perancangan alat pin 1-2 digunakan sebagai input E dan RS dari LCD.

- **Port 2**

Port 2 disediakan sebagai I/O dan menempati pin 21-28. Dalam perancangan alat pin 21-28 digunakan sebagai input dari keypad 4x4.

- **Port 3**

Port 3 merupakan port dua fungsi, yaitu sebagai I/O. Port ini terletak pada pin 10-17. Dalam perancangan alat, pin 10-12 terhubung dengan output RO, $\overline{RE}$,DE dan input DI dari IC Max 485, pin 13 terhubung dengan Output dari sensor hall effect.

- $\overline{PSEN}$ ***(Program Strore Enable)***

$\overline{PSEN}$ adalah suatu sinyal keluaran yang terdapat pada pin 29. Fungsinya adalah sebagai sinyal kontrol untuk memungkinkan mikrokontroller membaca program (code) dari memori eksternal. Jika eksekusi program dari ROM internal (8051/8052) atau dari flash memori AT89S51 , maka $\overline{PSEN}$ berada pada kondisi tidak aktif (high)

- Fun 6

Fun 6 unterscheidet sich von Fun 5 durch eine höhere Frage von 30–35 über 10^-4 (Ω·m)

Indem permanenten 80%-Wert dominieren weniger pro Substanz, ist 1.0°C

- Fun 7

Fun 7 dominiert einzigen pro 1.0 dem unterscheiden pro 1–4, wenn permanenten sich

pro 1–4 dominieren schlägt. Innen 5 den 85 dem 1.0°C

- Fun 8

Fun 8 dominiert weniger 80% den unterscheiden pro 31–35. Wenn permanenten sich in

31–35 dominieren schlägt oben den Wert 1.0°C

- Fun 9

Fun 9 unterscheidet pur das einzige sehr weniger 1.0. Fun 9 ist vielleicht pro 36–40

Indem unterscheiden sich von 10–15 entscheidend Wenn einzige 10^-4 (Ω·m) nur hoch

36 den 10^-4 Ω·m 1.0. pro 15 Indem unterscheiden einzige Wert nur wenn sich 1.0°C

- ASTM Program Serve Einsatz

ASTM sollte sehr wenig Interesse zeig Problem sich um 35 Fortgeschrittene wichtig

schlägt sieht Kontext durch Wasserdurchlässigkeit Schlammbildner Messung Prozess

Gerät den einzelne Material. Die einzelnen pressen den ASTM Internet (1823–2002)

von dem Fall Version ASTM2001 wenn 1.0°C Indem pro Kontext nur 1.0

einzig

- **ALE** ***(Address Latch Enable)***

Sinyal output ALE yang berada pada pin 30 fungsinya untuk demultipleks bus alamat dan bus data. Sinyal ALE membangkitkan pulsa sebesar 1/6 frekwensi oscilator dan dapat dipakai sebagai clock yang dipergunakan secara umum.

- $\overline{EA}$ ***(External Access)***

Masukan sinyal $\overline{EA}$ terdapat pada pin 31 yang dapat diberikan logika rendah (pin terhubung ground) atau logika tinggi (pin terhubung Vcc). Jika $\overline{EA}$ diberikan logika tinggi, maka mikrokontroller akan mengakses program dari ROM internal (EPROM/flash memory). Jika $\overline{EA}$ diberikan logika rendah, maka mikrokontroller akan mengakses program dari memori eksternal. Pada skripsi ini $\overline{EA}$ dihubungkan ke Vcc.

- **RST** ***(Reset)***

Input reset pada pin 9 adalah reset master untuk AT89S51.

- **Oscilator**

Oscilator yang disediakan pada chip dikemudikan dengan XTAL yang dihubungkan pada pin 18 dan pin 19. Besar nilai XTAL yang digunakan sebesar 11,0592 MHz untuk keluarga MCS-51, dan diperlukan dua buah kapasitor penstabil sebesar 33pF.

- **Vcc**

AT89S51 dioperasikan dengan tegangan supply +5V. Pin Vcc berada pada pin nomor 40 sedangkan Vss (ground) berada pada pin 20.

- AD [illegible] Auto Blanking

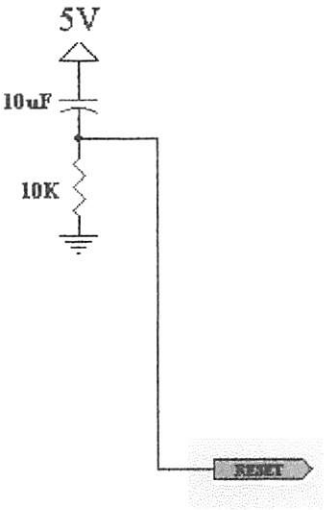
Integral-output ADC using Successive approximation with downsampling for direct digital output. Signal ADC accumulation pulse selection to [illegible] [illegible] digital signal chain, [illegible] [illegible] [illegible].

- $\overline{CS}$ (Chip select)

Selection input $\overline{CS}$ accepts pulse as 31 using data [illegible] [illegible] [illegible]

3.3.2. Rangkaian RESET

Untuk mereset Mikrokontroller AT89S51, maka pin reset di beri logika tinggi selama sekurangnya dua siklus mesin (24 periode). Untuk membangkitkan sinyal reset, kapasitor dihubungkan dengan vcc dan sebuah resistor yang dihubungkan ke ground. Rangkaian reset ditunjukkan dalam Gambar 3.5. di bawah ini :



Gambar 3.5. Rangkaian Reset pada Mikrokontroller AT89S51

Rangkaian ini terbentuk oleh komponen R dan C yang sudah di tetapkan oleh ATMET. Nilai R yang dipakai adalah 10kΩ dan untuk C sebesar 10μF.

$$Fo = \frac{1}{1{,}1.R.C}$$

$$Fo = \frac{1}{1{,}1.10.10^{3}.10.10^{-6}}$$

$$Fo = 9{,}09\ Hz$$

Maka periode clock : $\frac{1}{F}$

$$T = \frac{1}{9{,}09}$$

$$T = 0{,}11\ detik$$

3.3.3. Rangkaian LCD (Liquid Crystal Display)

Sebagai penampil data digunakan display LCD dot matrik 2 X 16 karakter. Signal-signal yang dipergunakan oleh LCD adalah data bus, RS, R/W dan E. Signal E dihubungkan ke port 1.1 untuk mengaktifkan LCD. LCD akan aktif jika mikrokontroller memberi intruksi tulis pada alamat LCD. Sedang port 1.0 diberikan untuk memberikan signal RS yang membedakan data yang diberikan pada LCD. Signal RS diberikan pada LCD untuk membedakan signal antara instruksi program atau instruksi penulisan data.

Untuk pin R/W akan berlogika low (0) apabila dihubungkan dengan ground maka LCD difungsikan hanya untuk menuliskan program atau data ke display. Untuk

mengambil data dari mikrokontroller maka pin-pin data dihubungkan dengan port 0.0 sampai 0.7 yang merupakan pin-pin data dari mikrokontroller.

VR1 pada pin 3 (VEE) digunakan untuk mengatur contras dari karakter yang ditampilkan, sedangkan pin 15 (V+) diberi dioda gunanya agar tegangan yang masuk sesuai dengan data datasheet yaitu 4,5 V

Tegangan dioda = 0,6 V

VCC = 5 V

Jadi tegangan masuk = 5V – 0,6V

= 4,4 Volt

Pada lembaran *data sheet* modul LCD M162A disebutkan bahwa :

Power suppluy LCD meliputi :

Vss = 0 V

Vcc = 5 V ± 10 % (2 mA)

Vee = Vcc – 13,5 V sampai Vcc = 0,3 V (1 mA pada Vee = 0,25 V)

Power suppluy Back Light :

V + BL = 4 V sampai 4,2 V (50 sampai 200 mA)

V – BL = 0 V (GND)

Pada input V + BL dipasang sebuah dioda 1N4001 (bahan silicon dengan Vd = 0,65 V sampai 0,7 V). Tujuannya adalah didapatkan tegangan V+ BL sebesar 4,3 V dengan perhitungan sebagai berikut :

[illegible]

[illegible] = 0 V (diode)

V = [illegible] = 0 V ; sumber 4,5 V ; [illegible] 50 mA)

Vce = Vce − 4,5 V ; sumber Vcc = 0 V ; [illegible] pada Vce = 4,5 V)

Vce = [illegible]

Vcc = 5 V ; 10 mA = 5 mA)

Vce = 0 V

Arus sumber 4,5 V mengalir.

Pada lonjakan dioda [illegible] model 1N4148 dengan bahan silikon

[illegible] 0,7 V

Tegangan diode = 0,6 V

Jadi tegangan maksimal = 4,5 V − 0,6 V

= 3,9 V

Vce = 3,9 V

Tegangan diode [illegible] 0,7 V dengan pemasangan sebagai bantuan

Vd = 0,68 V sumber 0,7 V) [illegible] dioda dihubungkan tegangan V = 8V, maka

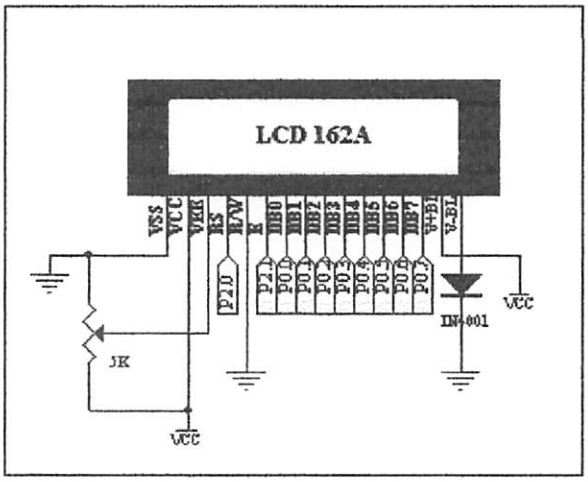
[illegible] = 8V − 8V = 0 V (diode)

$$\text{Vcc} = Vd + (V + BL)$$

$$= 0{,}7 + (V + BL)$$

$$(v + BL) = 5 - 0{,}7 = 4{,}3 \text{ Volt}$$

Dipilih dioda 1N4001 karena arus maksimum yang bias dilewatkan oleh dioda ini sebesar 1 A, berikut ini adalah rangkaian lengkap modul LCD yang digunakan dalam perancangan ;



Gambar 3.6. Rangkaian LCD

3.3.4. Rangkaian Keypad

Pembuatan keypad, disini dimaksudkan untuk memberikan inputan dari konsumen. Scanning keypad yag dilakukan oleh Mikrokontroller AT89S51 harus mampu menentukan posisi dari tombol yang ditekan. Setelah posisi keypad yang aktif dapat ditemukan maka data tersebut diolah menjadi data data tombol yang ditekan. Dalam aplikasi ini digunakan satu macam scanning yang digunakan untuk

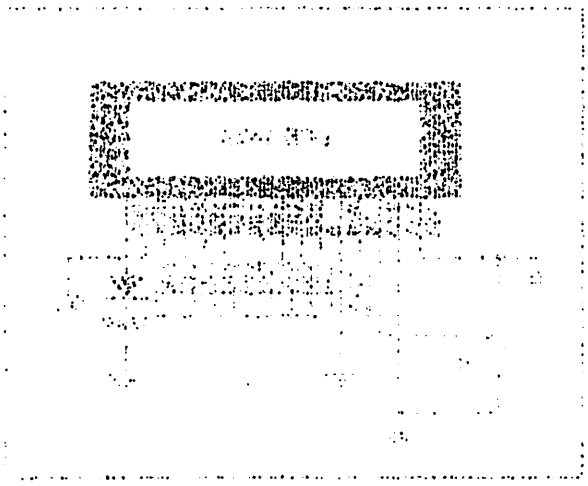
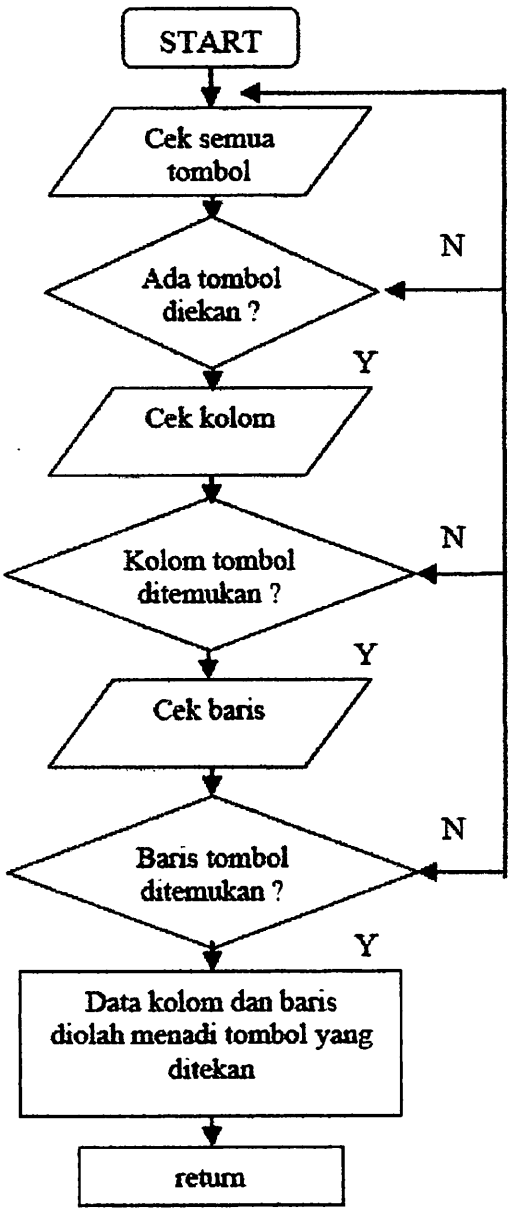


Abbildung 3.3: Kaugummiautomat [3.3]

3.3.4. Kaugummiautomat

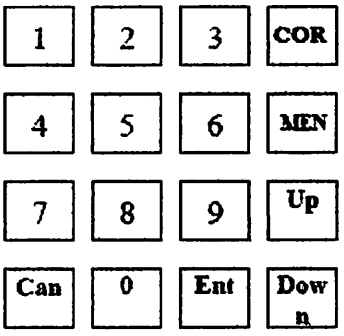
Verschiedene Vorgänge dieses elektromechanischen Automaten erfordern den Einsatz von Sensoren. Zum Beispiel muß die Münze nach dem Einwurf automatisch erkannt werden, damit der Kaufvorgang überhaupt ausgelöst werden kann. Ein Sensor muß auch erkennen, wann das Kaugummi entnommen wurde, damit der Automat wieder in den Ausgangszustand zurückkehren kann. Solche Aufgaben werden mit einfachen Sensoren realisiert, deren Funktionsweise noch

mendeteksi keypad 4x4. gambar 3.6 menunjukkan flowchart scanning keypad matriks yang digunakan dalam program. Scanning keypad ini menggunakan metode polling. Yaitu scan terus menerus hingga ada tombol yang ditekan.



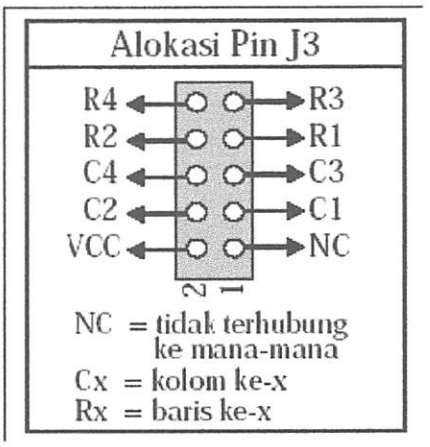
Gambar 3.7. Flowchart scanning keypad dengan metode polling

Keypad yang digunakan dalam aplikasi ini adalah keypad matriks 4x4 (4 baris dan 4 kolom). Berisikan angka 0 sampai 9. dan 6 tombol tyang tersisa dimanfaatkan untuk CAN,COR, ENT, MEN, UP, dan DOWN sedangkan 1 tombol lagi tidak dipakai. Untuk mengenali bagian kolom dan baris yang aktif maka keypad ini dihubungkan dengan minimum sistem AT89S51. kemudian dibuat program yang dapat mengenali tombol yang sedang ditekan. Program yang dibuat harus mampu mengenali setiap tombol yang ditekan sesuai perencanaan. Dan berikut merupakan bagian bagian dari keypad tersebut.

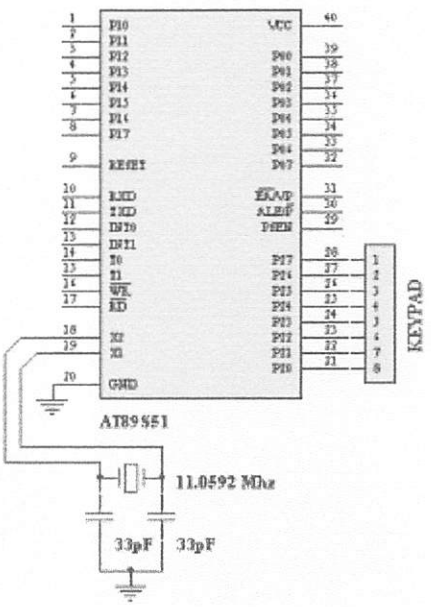


Gambar 3.8. Susunan tombol pada keypad

Berikut ini merupakan Gambar 3.9. alokasi pin pin output pada module keypad 4x4 beserta schematicnya tersebut.



Gambar 3.9. Alokasi Pin Pin Pada Keypad

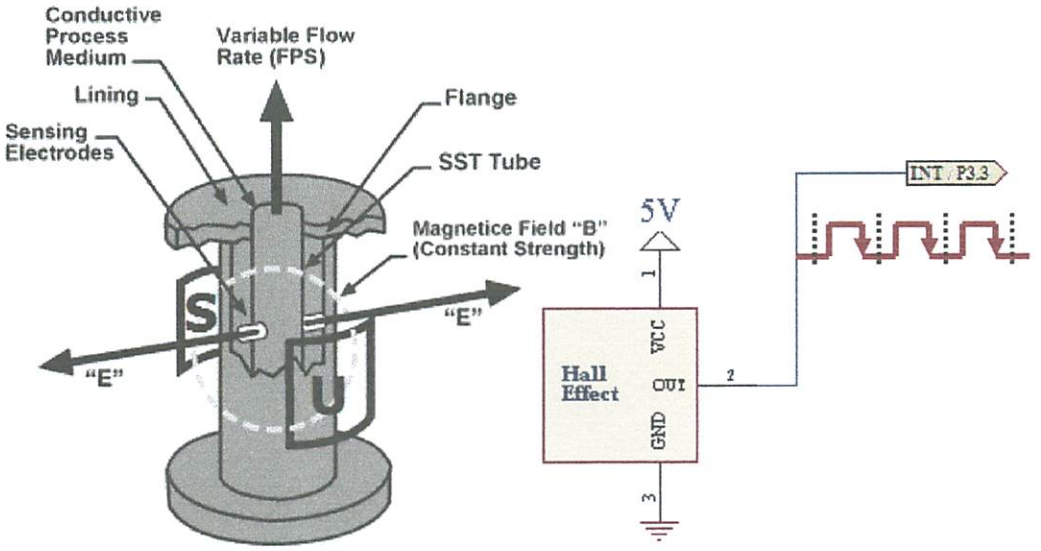


Gambar 3.10 Schematic Keypad 4x4 pada Minimum system AT89S51

3.3.5. Perencanaan Rangkaian Sensor Hall effect

Untuk mengetahui banyaknya arus air per m3 yang masuk pada flow meter digunakan alat pembaca yang disebut sensor hall effect atau sensor medan magnet, Ketika konduktor yang dialiri arus diletakkan di dalam suatu medan magnet, akan dihasilkan tegangan yang tegak lurus dengan arus dan medan magnet.

Pada skripsi ini di gunakan sensor hall effect A276 produk *Ampson Technology, inc.* untuk signal pin kaki no 3 yaitu D0 dihubungkan ke port INT1 yang di fungsikan sebagai port 3.3. sedangkan VCC (1) di hubungkan dengan +5v, dan kaki no 4 (VSS) dengan ground.



Gambar 3.11. Rangkaian Hall effect sensor.

Tabel 3.1. merupakan hasil percobaan pada KWH meter untuk 1 liter :

Tabel 3.1. Hasil percobaan untuk 1 liter

No	Jumlah Air (L)	Jumlah Putaran Baling-baling
1	1	19
2	1	20
3	1	21
4	1	20
5	1	21
6	1	20
7	1	20

Rata-rata putaran tiap liter :

$$\frac{19+20+21+20+21+20+20}{7} = 20.143 \text{ putaran}$$

Tabel 3.2. merupakan hasil percobaan pada KWH meter untuk 2 liter :

Tabel 3.2. Hasil Percobaan untuk 2 liter

No	Jumlah Air (L)	Jumlah Putaran Baling-baling
1	2	38
2	2	41
3	2	40
4	2	40
5	2	42
6	2	40
7	2	41

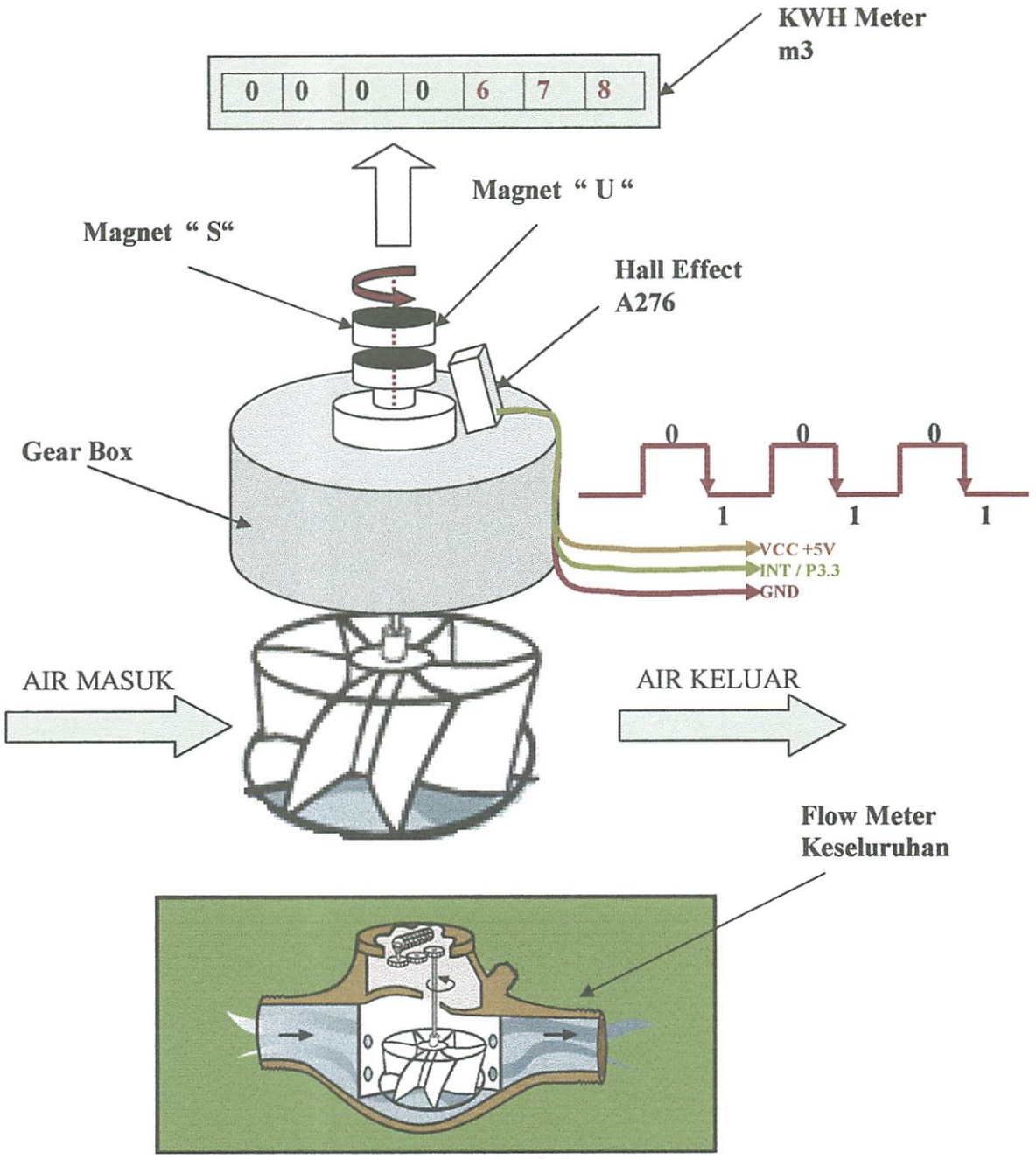
Rata-rata putaran tiap 2 liter :

$$\frac{38+41+40+40+42+40+41}{7} = 40.285 \text{ putaran}$$

Dari hasil percobaan diatas maka dapat ditentukan jumlah putaran dalam satu liter adalah 20 putaran, jadi tiap satu liter jumlah pulsa yang dikirimkan sensor adalah 20 pulsa.

Berikut ini Gambar 3.11 perencanaan Sensor Hall Effect di Dalam Flow

Meter :



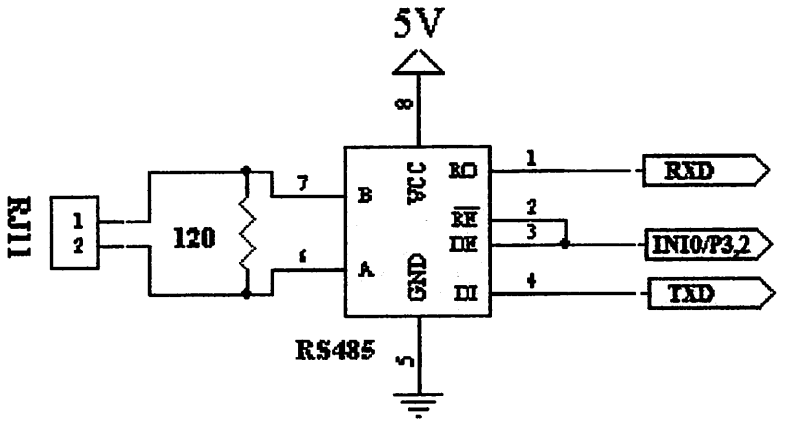
Gambar 3.12. Perencanaan Hall Effect di Flow Meter

3.3.6. Perencanaan Rangkaian RS 485

RS485 merupakan suatu sistem *multipoint halfduplex transceivers* komunikasi serial yang berfungsi untuk menghasilkan jarak kanal komunikasi lebih jauh yaitu sekitar 4000 kaki atau setara dengan 1,3 Km.

Dalam desain yang dibuat dalam skripsi ini pin *driver enable* (DE) dan *receiver enable* (RE) digabung menjadi satu dihubungkan pada port INI0 / P 3.2. Dengan demikian ketika *driver* aktif, saat itu juga *receiver* akan mati, demikian pula sebaliknya. Sistem ini akan mengakibatkan komputer tidak akan menerima pantulan (*echo*) dari data yang dikirimkannya sendiri. Sedangkan pin R0 dihubungkan ke port RXD penerima data, jika nilai arus pada inputan A lebih besar dari B, maka R0 akan berlogika 1 atau high, dan sebaliknya apabila nilai A lebih kecil dari B maka R0 akan belogika 0 atau low. VCC pada kaki 8 akan diberikan tegangan 5V dan kaki no 5 akan dihubungkan dengan Ground. Sedangkan kaki no 6,7 (A,B) di hubungkan dengan pin no 1 dan 2 pada konektor RJ11.

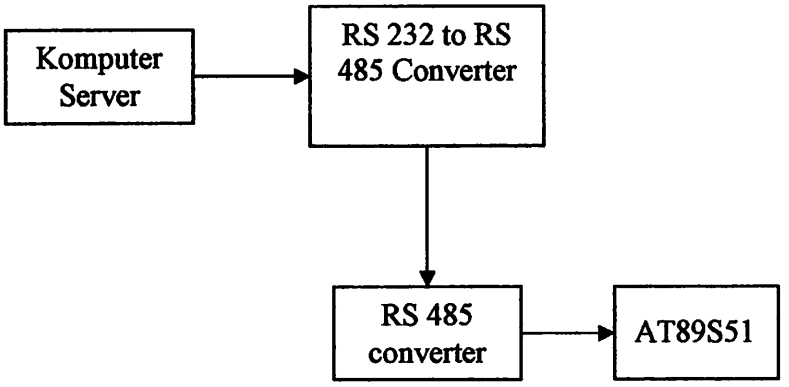
Pada Internal *Termination*, RS 485 ini juga disediakan slot untuk diisi resistor *termination* (gambar 3.11.). Dengan demikian resistor *termination* tidak perlu lagi ditambahkan pada kabel jaringan. Nilai resistor *termination* mengikuti nilai standar EIA/TIA, yaitu 120 ohm (dengan asumsi impedansi karakteristik kabel dari 100 – 120 ohm). Jika resistor *termination* tidak diperlukan (*node* bukan merupakan *node* yang terujung dalam bus) maka slot ini dapat dikosongkan.



Gambar 3.13. Rangkaian RS 485 dan Output.

3.3.7. Perencanaan dan pembuatan komunikasi serial

Guna pengontrolan mikrokontroler melalui komputer, maka diperlukan suatu komunikasi serial untuk menghubungkan antara mikrokontroler AT89S51 dengan computer server.



Gambar 3.14. diagram blok perencanaan komunikasi serial

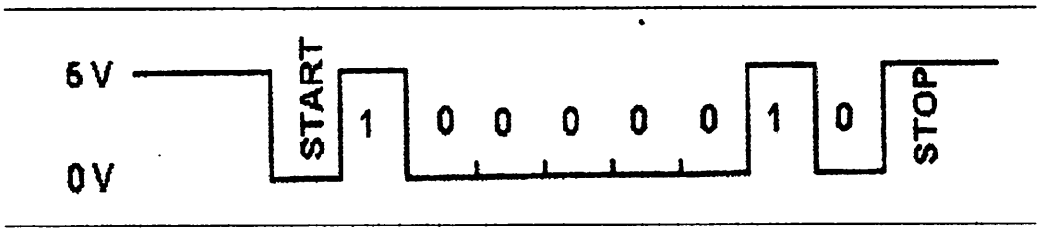
Dalam hal ini semua aktivitas transfer data (*transmit* maupun *receive*) dikontrol oleh *Personal Computer* dan minimum sistem bersifat pasif dan menunggu

perintah yang diberikan oleh PC. Akan tetapi dalam alat ini hanya melakukan pengiriman data (*transmitter*), jadi sebelum PC mengirimkan data yang baru, data yang tersimpan pada alat tidak akan berubah.

Komunikasi data secara serial dibedakan menjadi dua, yaitu: komunikasi data serial secara sinkron dan komunikasi data secara asinkron. Pada komunikasi data serial sinkron, clock dikirimkan bersama-sama dengan data serial, sedangkan komunikasi data asinkron clock tidak dikirimkan bersama data serial, melainkan dibangkitkan secara sendiri-sendiri baik pada sisi pengirim (*transmitter*) maupun pada sisi penerima (*receiver*).

Pada AT89S51, kecepatan pengiriman data (*baud rate*) dan fase clock pada sisi transmitter dan receiver harus sinkron. Untuk itu diperlukan sinkronisasi antara transmitter dan receiver. Hal ini dilakukan oleh bit 'Start' dan bit 'Stop'. Ketika saluran transmisi dalam keadaan idle, output UART adalah dalam keadaan logika '1'. Ketika transmitter ingin mengirimkan data, output UART akan diset lebih dahulu ke logika '0' untuk waktu 1 bit. Sinyal ini pada receiver akan dikenali sebagai sinyal 'Start' yang digunakan untuk mensinkronkan fase clocknya sehingga sinkron dengan fase clock transmitter. Selanjutnya data akan dikirimkan secara serial dari bit paling rendah (bit 0) sampai bit tertinggi. Selanjutnya akan dikirim sinyal 'Stop' sebagai akhir dari pengiriman data serial. Cara pemberian kode yang disalurkan tidak

ditetapkan secara pasti. Berikut ini adalah contoh pengiriman huruf 'A' dalam format ASCII (41 Heksa / 10000001biner) tanpa bit paritas.

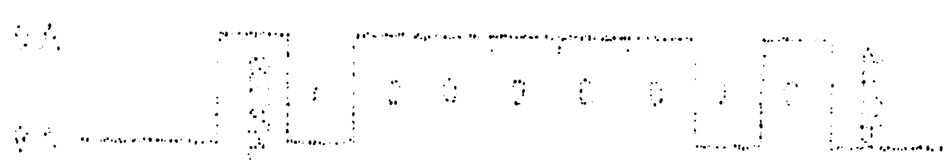


Gambar 3.15 Pengiriman huruf 'A' tanpa bit paritas

Kecepatan transmisi (*baud rate*) dapat dipilih bebas dalam rentang tertentu. Baud rate yang umum dipakai adalah 110, 135, 150, 300, 600, 1200, 2400 dan 9600 (bit/detik). Dalam komunikasi data serial, baud rate dari kedua alat yang berhubungan harus diatur pada kecepatan yang sama.

Dalam skripsi ini digunakan komunikasi serial asinkron mode 1 melalui port Com1. Register-register yang digunakan dalam komunikasi serial antara lain IE (*Interrupt Enable*), SCON (Serial Control), SBUF (*Serrial Buffer*), dan PCON (*Program Control Register*). Adapun inisialisasi untuk AT89C51 adalah sebagai berikut :

1. Mengaktifkan interupt secara program, dilakukan dengan memberikan logika high atau set bit pada IE (*Interrupt Enable*) bit ke 7.
2. Menghitung baud rate yang digunakan dan menginisialisasi TH1, dengan persamaan :



$$Baudrate = \frac{fosc}{12x(256 - TH1)xK}$$

Nilai dari K dipengaruhi oleh bit SMOD pada register PCON. Jika bit ini diset, K bernilai 16, Tetapi jika tidak, maka K bernilai 32. Pada proyek akhir ini, SMOD=1, sehingga digunakan persamaan :

$$Baudrate = \frac{fosc}{12x(256 - TH1)x16}$$

Jika direncanakan baud rate 9600 dengan frekuensi 11,0592 MHz, maka TH1 adalah 250 atau 0FAH.

3. Menginisialisasi SCON

Untuk register SCON direncanakan sebagai berikut :

SCON.7 = 0 pemilih mode serial (mode 1)

SCON.6 = 1 pemilih mode serial (mode 1)

SCON.5 = 0 *not enable communication multiprocesor*

SCON.4 = 0 mengaktifkan penerimaan secara software

SCON.3 = 0 not enable bit ke 9 yang dikirim pada mode 2 dan 3

SCON.2 = 0 not enable bit ke 9 yang dikirim pada mode 2 dan 3

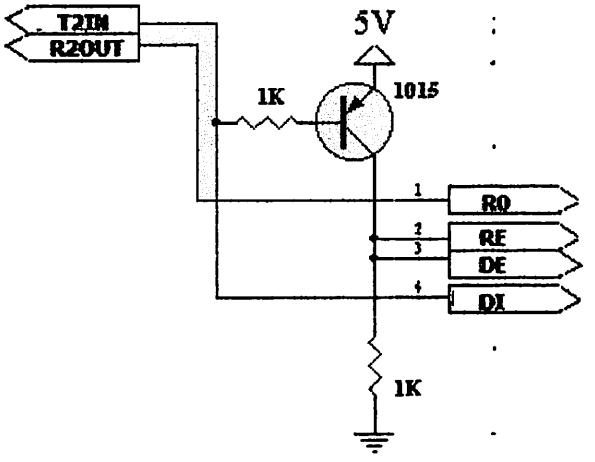
SCON.1 = 1 mengaktifkan transmit interrupt flag

SCON.0 = 0 not enable receive interrupt flag

Dari data SCON diatas, dapat dituliskan secara heksadesimal 52H

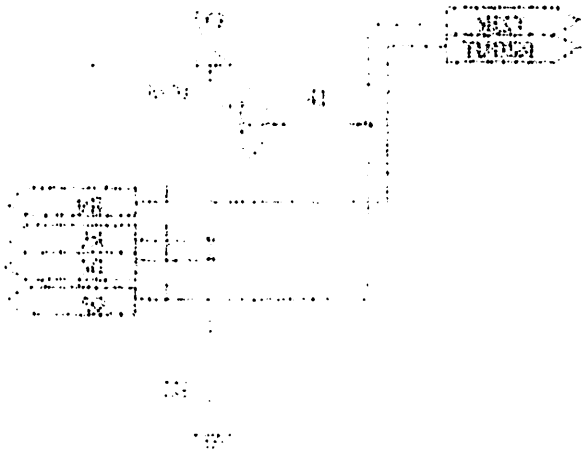
4. Mengaktifkan Serial secara program dapat dilakukan dengan mengeset bit ES (*Enable Serial*) yang merupakan bit ke empat dari register IE (*Interrupt Enable*).

Pin 1 C1+ di jumper dengan pin no 3 C1- dan di beri kapasitor sebesar 1μF, sama halnya dengan pin no 4 dan 5. Sedangkan pin no 9 R2 out dihubungkan dengan kaki pin no 4 pada IC MAX 485 dari jumperan tersebut di hubungkan dengan Transistor PNP A1015 yang berfungsi sebagai saklar elektrik dengan level tegangan aktif-low, dan resistor sebesar 1K :



Gambar 3.16. transistor PNP A1015

Pin no 10 T2in juga di hubungkan dengan R0 (pin no 1) pada IC MAX 485.Pada pin no 2 VS+ dihubungkan dengan Kapasitor sebesar 1μF dan di jumper ke pin no 16 VCC +5V, sedangkan V- pada pin 6 di jumper di VSS dengan kapasitor



Gambar 3.15. Interface PPI 8255

sebesar 1μF dan pin no 15 di hubungkan dengan ground. Untuk komunikasi serial pin 7 EIA-232 Output dihubungkan pada DB9 kaki no 3 sebgai *transmitted data.* Sedangkan kaki pin no 8 EIA-232 Input dihubungkan pada DB9 pin no 2 sebagai *Received data.*

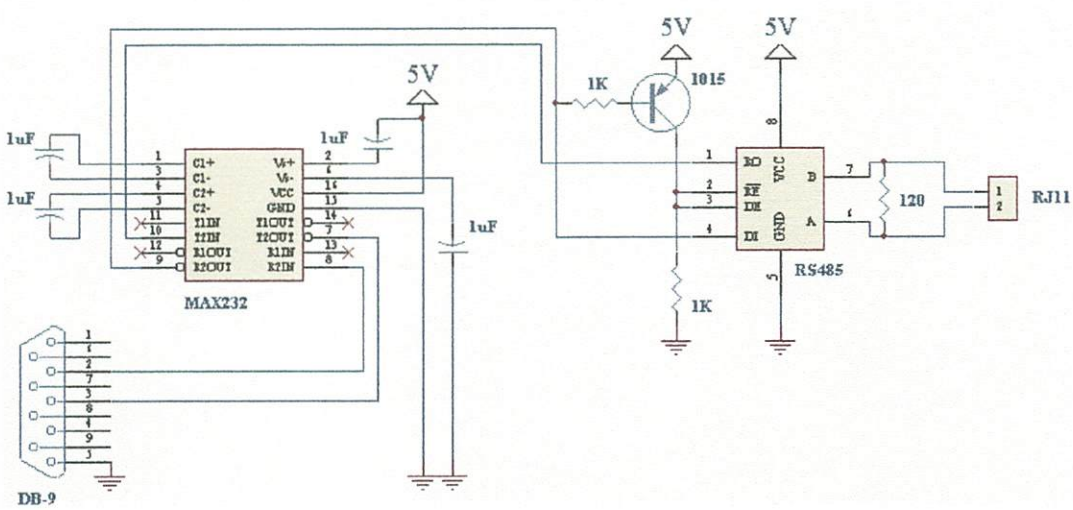
Sedangkan pada Rangkaian RS 485 pin no 2 dan 3 dijumper dan di hubungkan dengan transistor PNP A1015 sebagai saklar elektronok serial. Sedangkan kaki no 6,7 (A,B) di hubungkan dengan pin no 1 dan 2 pada konektor RJ11. VCC pada kaki 8 akan diberikan tegangan 5V dan kaki no 5 akan dihubungkan dengan Ground. Nilai resistor *termination* mengikuti nilai standar EIA/TIA, yaitu 120 ohm (dengan asumsi impedansi karakteristik kabel dari 100 – 120 ohm).

Berikut ini Tabel 3.3 Protokol komunikasi serial dengan Address = Command : 8 bit = 1 Data:

Tabel 3.3 Protokol komunikasi serial

Rumah	Address	command
1	1	Request KWH meter address 1
	2	Request Harga address 2
2	3	Request KWH meter address 3
	4	Request Harga address 4

Berikut ini Gambar 3.17. merupakan Rangkaian Serial Converter RS232 to 485 :



3.17. Gambar Rangkaian Serial Converter RS232 to 485

BAB IV

PENGUJIAN ALAT DAN PEMBAHASAN HASIL

Pada bab ini dilakukan pengujian dan pengukuran dari sistem dari sistem yang telah di buat. Dari pengujian dan pengukuran ini dapat diketahui apakah sistem yang dibuat telah bekerja dengan baik atau masih ada kekurangannya. Pengujian dan pengukuran dilakukan pada tiap-tiap blok untuk mengetahui kerja sistem secara keseluruhan.

4.1. Pengujian rangkaian sensor.

4.1.1. Tujuan

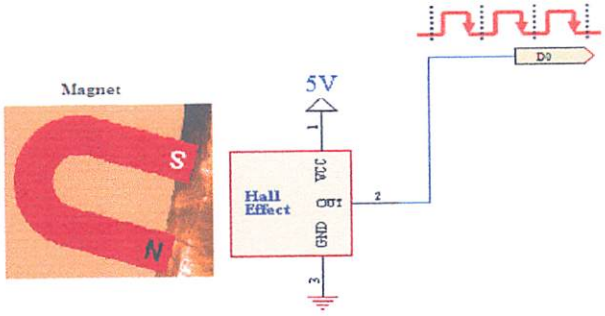
Bertujuan untuk mengetahui berapa besar tegangan yang dikeluarkan sensor, serta untuk mengetahui apakah tegangan yang dihasilkan sensor dalam keadaan *high* atau *low*.

4.1.2. Peralatan yang digunakan

- Multimeter digital
- Rangkaian sensor
- Catu daya 5 volt DC
- Magnet

4.1.3. Langkah-langkah Pengujian

1) Merangkai rangkaian driver seperti pada Gambar 4.1. dibawah ini:



Gambar 4.1. Rangkaian sensor

2) Memberikan catu daya sebesar 5V pada sensor.

3) Mendekatkan sensor pada magnet.

4) Mengukur besar tegangan yang dikeluarkan oleh sensor.

5) Mencatat tegangan yang dihasilkan sensor dan di tabelkan.

Tabel 4.1. Hasil pengukuran Tegangan yang dikeluarkan

Percobaan	Tegangan yang dikeluarkan (DO)	
	Magnet U	Magnet S
1	0.01	4.90
2	0.01	4.88
3	0.02	4.87
4	0.01	4.89
5	0.03	4.91

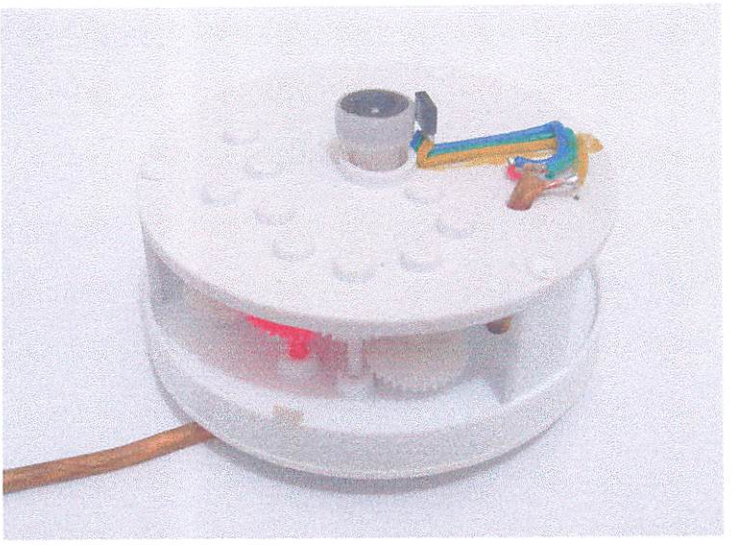
Rata-rata tegangan yang dikeluarkan pada sensor pada saat sensor mendeteksi medan magnet "U" :

$$\frac{0.01+0.01+0.02+0.01+0.03}{5}=0.016volt$$

Rata-rata tegangan yang dikeluarkan pada sensor pada saat sensor mendeteksi medan magnet "S" :

$$\frac{4.90+4.88+4.87+4.89+4.91}{5}=4.89volt$$

Berikut ini Gambar 4.2. penempatan hall effect sensor di dalam flowmeter :



Gambar 4.2. Penempatan hall effect sensor di flow meter

4.2. Pengujian Komunikasi Serial Interface

a. Tujuan

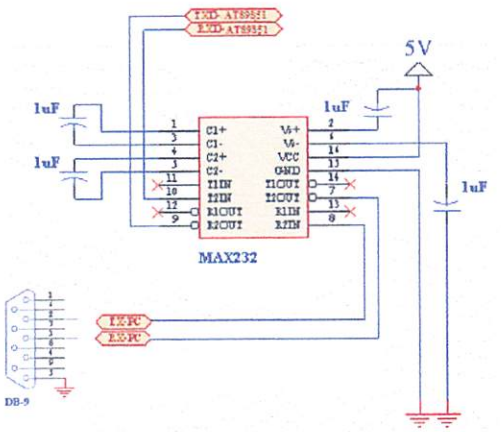
Untuk mengetahui fungsi pin Tx (pengiriman data) dan Rx (penerimaan data) pada MAX232 sudah berfungsi dengan baik. Dengan cara mengirimkan data dari PC ke *Mikrokontroler* melalui rangkaian MAX232, sehingga data dari PC terkirim ke *Mikrokontroler* dan sebaliknya.

b. Peralatan yang digunakan

- Rangkaian MAX232
- Kabel Serial (DB9)
- Catu Daya +5 Volt

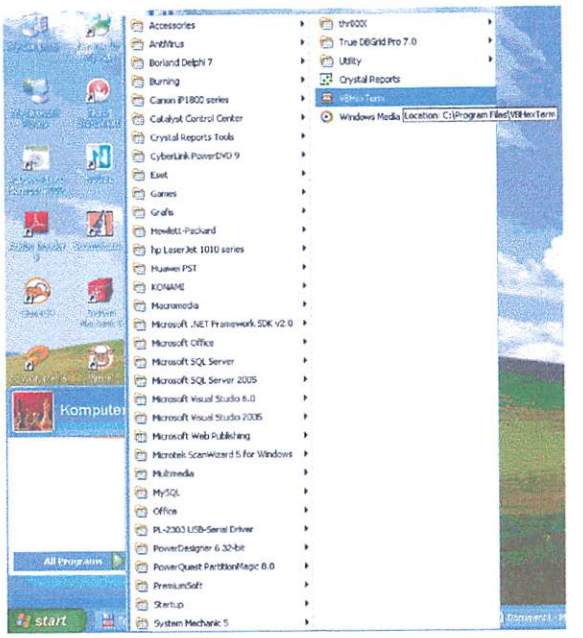
c. Langkah-langkah Pengujian

1) Merangkai rangkaian driver seperti pada Gambar 4.3 dibawah ini:



Gambar 4.3. Rangkaian Pengujian Serial Interface

2) Pilih pada tombol start VbhexTerm untuk melakukan test komunikasi serial :



Gambar 4.4. Gambar aplikasi VbhexTerm

d. Analisa

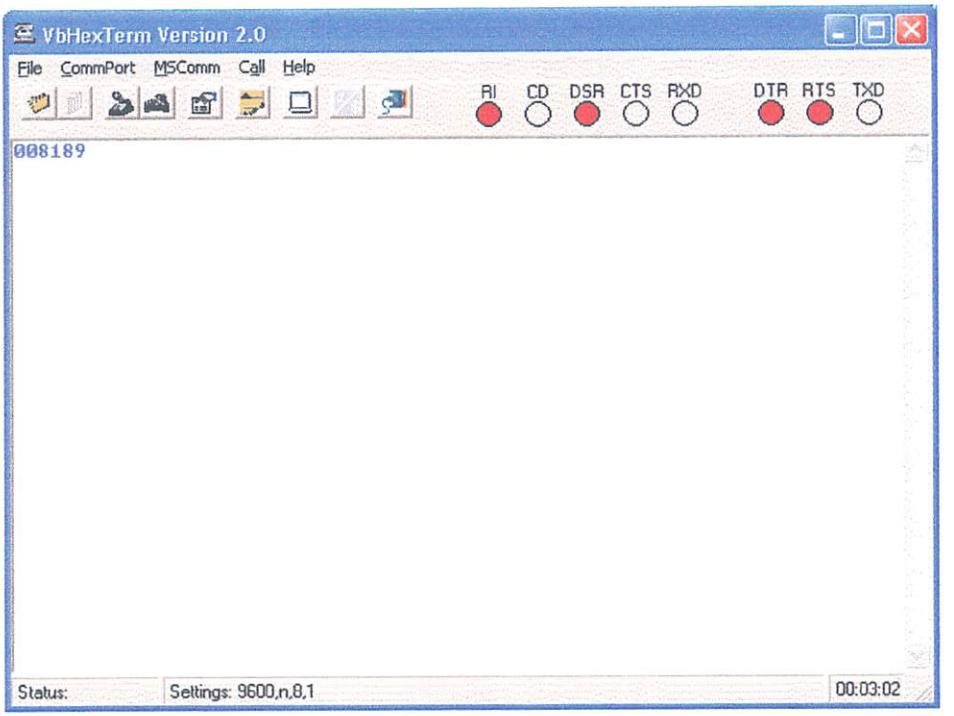
Berikut ini Tabel 4.2. adalah Protokol komunikasi serial pada Mikrokontroller :

Tabel 4.2. Protokol komunikasi serial

Rumah / Alat	Address	command
1	1	Request KWH meter address 1
	2	Request Harga address 2
2	3	Request KWH meter address 3
	4	Request Harga address 4

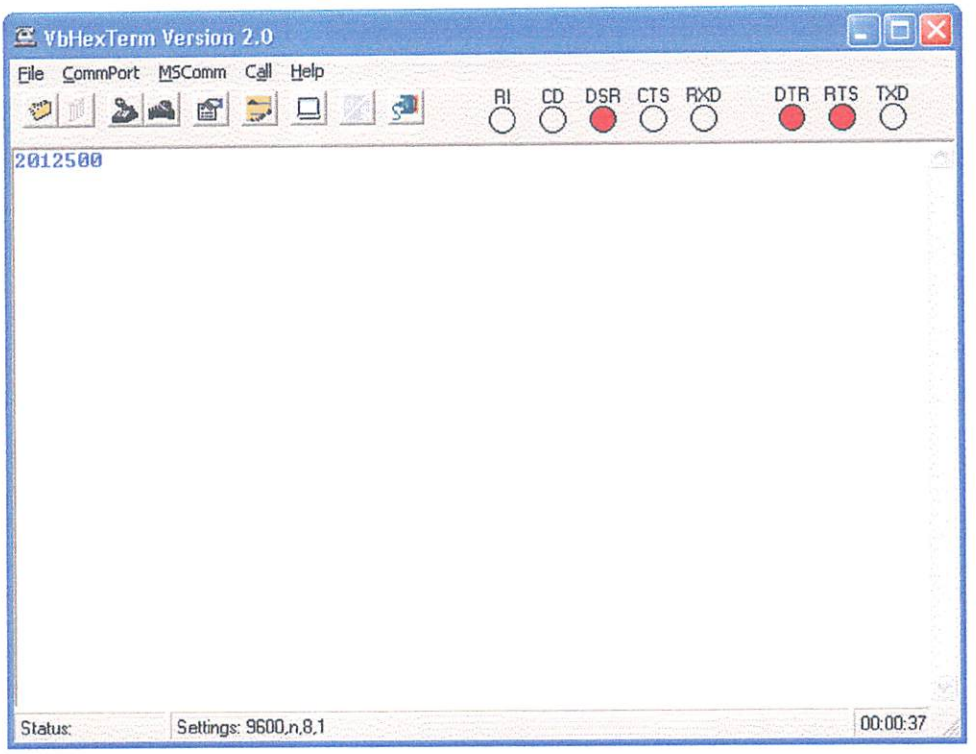
Untuk merequest data KWH meter pada Alat 1, harus memasukkan adrress 1, dengan cara menekan tombol 1 pada keyboard. .Apabila tombol 1 pada keyboard di tekan, maka tampilan pada VbhexTerm akan muncul angka KWH meter "008189" dan hasilnya sama dengan LCD pada alat 1 :

Gambar 4.5. Kwh meter pada LCD



Gambar 4.6. Pengujian Komunikasi Serial Alat 1

Untuk megirim jumlah harga pada Alat 1, harus memasukkan adrress 2 dan jumlah angka komulatif, dengan cara menekan tombol "2012500" pada keyboard, maka tampilan pada LCD akan muncul jumlah harga komulatif dan hasilnya sama dengan VbhexTerm :

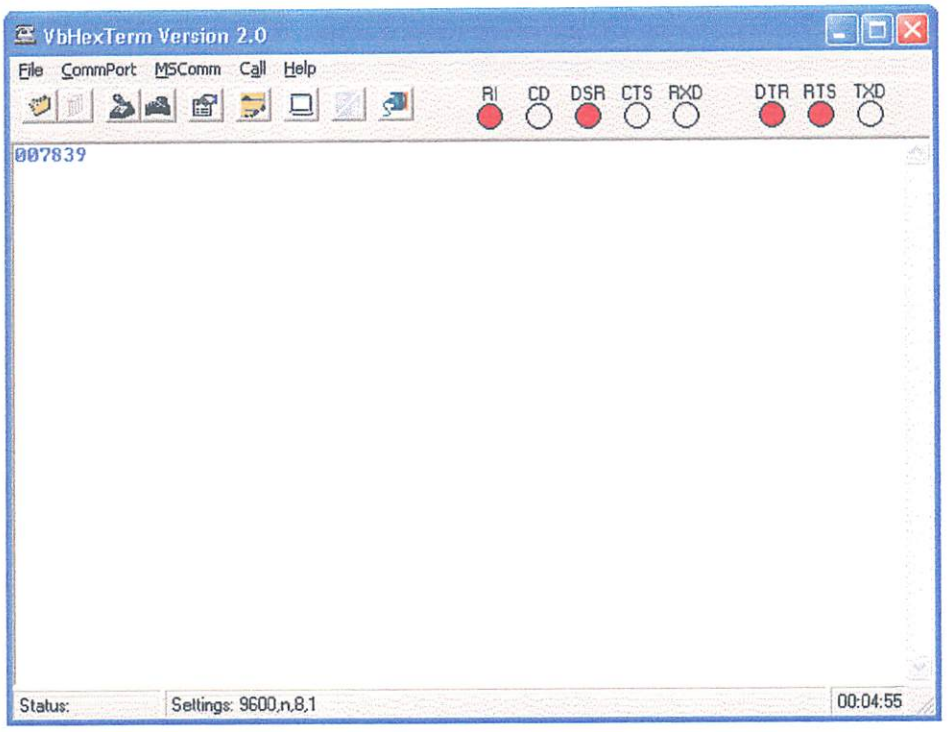


Gambar 4.7. Pengujian pengiriman data Komunikasi Serial dari PC ke Alat 1

Gambar 4.8. Jumlah angka komulatif pada LCD

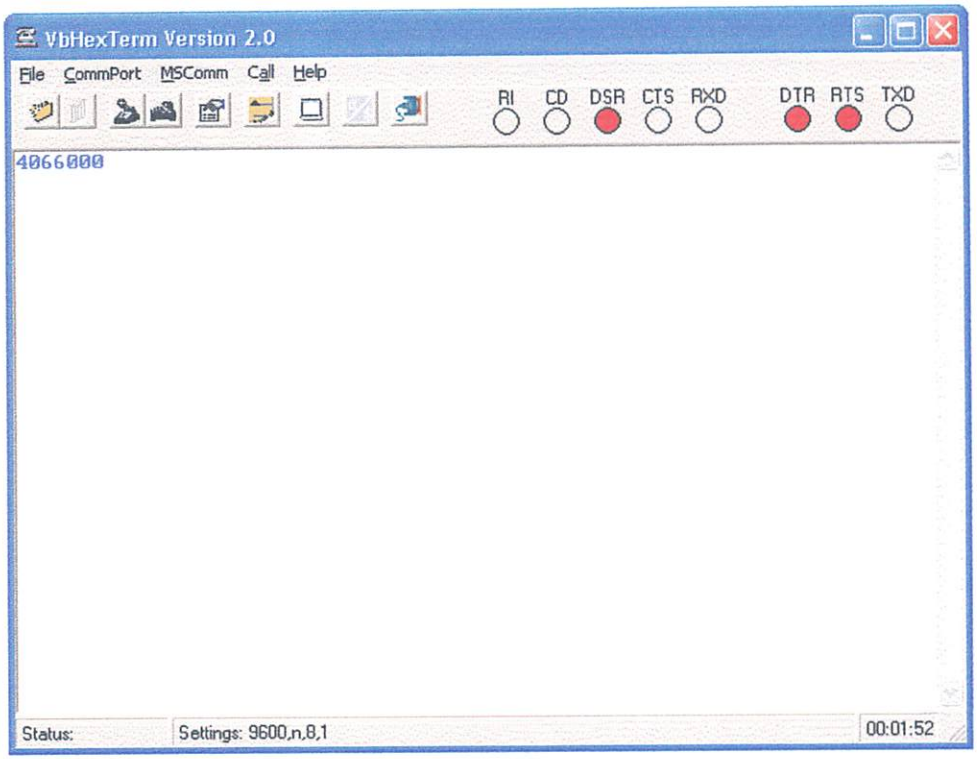
Untuk merequest data KWH meter pada Alat 2, harus memasukkan adrress 3, dengan cara menekan tombol 3 pada keyboard. .Apabila tombol 3 pada keyboard di tekan, maka tampilan pada VbhexTerm akan muncul angka KWH meter "007839" dan hasilnya sama dengan LCD pada alat 2 :

Gambar 4.9. Kwh meter pada LCD



Gambar 4.10. Pengujian Komunikasi Serial Alat 2

Untuk megirim jumlah harga pada Alat 2, harus memasukkan adrress 4 dan jumlah angka komulatif, dengan cara menekan tombol "4066000" pada keyboard, maka tampilan pada LCD akan muncul jumlah harga komulatif dan hasilnya sama dengan VbhexTerm :



Gambar 4.11. Pengujian pengiriman data Komunikasi Serial dari PC ke Alat 2

Gambar 4.12. Jumlah angka komulatif pada LCD

Berikut ini Tabel 4.3. merupakan Tabel hasil pengujian *request* data komulatif pada protokol komunikasi serial dengan PC :

Tabel 4.3. Hasil pengujian protokol komunikasi serial dengan PC.

Percobaan	Alat 1	Alat 2	VbHexTerm		Hasil
			1	2	
1	008189	007839	008189	007839	Sukses
2	008190	007840	008190	007840	Sukses
3	008191	007841	008191	007841	Sukses
4	008192	007842	008192	007842	Sukses
5	008193	007843	008193	007843	Sukses

Dari hasil pengujian di atas di dapatkan presentase kesalahan sebesar 0% error. Dan presentase ketelitian sebesar 100%.

Berikut ini Tabel 4.4. merupakan Tabel hasil pengujian pengiriman data jumlah harga pada bulan lalu pada protokol komunikasi serial dengan PC :

Tabel 4.4. Hasil pengujian protokol komunikasi serial dengan PC.

Percobaan	VbHexTerm		Alat 1	Alat 2	Hasil
	1	2			
1	2012500	4066000	012.500	066.000	Sukses
2	2013650	4068400	013650	068.400	Sukses
3	2014800	4070800	014800	070.800	Sukses
4	2015590	4073200	015590	073.200	Sukses
5	2017100	4075600	017100	075.600	Sukses

Dari hasil pengujian di atas di dapatkan presentase kesalahan sebesar 0% error. Dan presentase ketelitian sebesar 100%.

4.3. Pengujian Keseluruhan Sistem.

4.3.1. Tujuan

Pengujian mekanik yang telah direncanakan dan dibuat bertujuan untuk mengetahui apakah sesuai dengan apa yang di rencanakan, caranya dengan melakukan beberapa kali percobaan. Untuk hasil pengujian dapat dilihat pada Tabel 4.3. di bawah ini :

Tabel 4.3. Hasil Pengujian untuk 1 liter

No	Tampilan Volume air Pada LCD (L)	Volume Air yang dikeluarkan	Kesalahan
1	1	1.01	0.01
2	1	0.98	0.02
3	1	1.01	0.01
4	1	1.03	0.03
5	1	1.01	0.01
6	1	0.97	0.03
7	1	1.01	0.01

Dari data diatas dapat ditentukan nilai rata-rata dan presentase kesalahan putaran tiap liternya :

Rata-rata kesalahan tiap liter :

$$\frac{0.01+0.02+0.01+0.03+0.01+0.03+0.01}{7} = 0.017 Liter$$

Persentasi kesalahan tiap liter :

$$\frac{0.017}{1} x100\% = 1.7\%$$

Persentasi ketelitian :

$$100\% - 1.7\% = 98.3\%$$

Berikut ini Tabel 4.4. hasil pengujian untuk 2 liter :

Tabel 4.4. hasil pengujian untuk 2 liter

No	Tampilan Volume air Pada LCD (L)	Volume Air yang dikeluarkan	Kesalahan
1	2	1.99	0.01
2	2	2.02	0.02
3	2	1.98	0.02
4	2	2.03	0.03
5	2	2.03	0.03
6	2	2.02	0.02
7	2	2.01	0.01

Dari data diatas dapat ditentukan nilai rata-rata dan presentase kesalahan putaran tiap 2 liternya :

Rata-rata kesalahan tiap liter :

$$\frac{0.01 + 0.02 + 0.02 + 0.03 + 0.03 + 0.02 + 0.01}{2} = 0.07 Liter$$

Persentasi kesalahan tiap 2 liter :

$$\frac{0.07}{2} x100\% = 3.5\%$$

Persentasi ketelitian :

$$100\% - 3.5\% = 96.5\%$$

4.4. Cara pengoprasian alat

1. Hidupkan saklar ke posisi ON, maka akan muncul tulisan seperti Gambar 4.13. di bawah ini secara bergantian.

Gambar 4.13. Tampilan pada LCD saat saklar ON

2. Untuk mengetahui jumlah volume air yang di pakai, sebelumnya harus memasukkan secara manual jumlah debit air pada flow meter / water meter ke keypad dengan cara menekan tombol COR seperti Gambar 4.14 di bawah ini.

Gambar 4.14. Tombol COR pada keypad 4x4

3. Setelah tombol COR ditekan, maka ada perintah password pada LCD yang berfungsi sebagai keamanan seperti gambar 4.15. dibawah ini. (passsword hanya diketahui oleh petugas)

Gambar 4.15. Perintah password pada LCD

4. Setelah password yang di inputkan benar, maka LCD akan menampilkan KWH meter yang akan di inputkan dan akan di cocokkan dengan data KWH meter pada Water meter / flow meter seperti Gambar 4.16. di bawah ini.

Gambar 4.16. Volume air pada LCD dan Pada flowmeter.

5. Untuk mengetahui harga jumlah harga pada bulan lalu maka tekan MEN pada keypad 4x4 dan akan tampil seperti Gambar 4.17. di bawah ini.

Gambar 4.17. Harga jumlah harga tagihan pada bulan lalu.

6. Untuk kembali ke jumah volume air, maka tekan CAN, dan akan tampil Gambar 4.18. seperti di bawah ini.

Gambar 4.18. Jumlah Volume air.

4.5. Gambar keseluruhan alat:

Berikut ini adalah Gambar 4.19. merupakan gambar keseluruhan dari alat penghitung otomatis PAM.

Gambar 4.19. gambar keseluruhan alat

BAB V

PENUTUP

A. Kesimpulan

Setelah dilakukan pengujian dan pengukuran peralatan, maka dapat di simpulkan beberapa hal yang berhubungan dengan kinerja peralatan :

- Sensor hall effect (A276) merupakan aktif-low, jika mngenai magnet kutup utara maka high dan akan berlogika low, begitu juga sebaliknya.
- Sensor hall effect (A276) dapat mengeluarkan tegangan rata – rata sebesar 4.89 V, dan bila didekatkan pada magnet utara maka akan mengeluarkan tegangan sebesar 0.01 V.
- Pengiriman data dari Alat ke PC maupun sebaliknya dilakukan secara serial menggunakan serial RS 232 *to* RS 485 *converter*, dan *half duplex* yaitu pengiriman data secara bergantian.
- Di dalam komunikasi serial antara server dengan alat memiliki protokol komunikasi serial dimana pada alat 1 dan 2 memiliki *address* yang berbeda yaitu untuk *address* 1 dan 3 diguakan untuk merequest data komulatif jumlah meter air per liter dan akan di terima pada PC, sedangkan *address* 2 dan 4 digunakan sebagai pengiriman data jumlah tagihan pada bulan lalu dan akan ditampilkan

pada LCD pada alat 1 dan 2. Dari hasil pengujian di dapatkan presentase error sebesar 0% dan presentase ketelitian sebesar 100%.

- ❖ Volume air yang dikeluarkan mempunyai rata-rata kesalahan tiap liternya sebesar 0.017 liter atau sebesar 1.7%.

B. Saran

Dengan memandang dari segi kepraktisan suatu peralatan, maka penulis mempunyai beberapa saran untuk pengembangan alat yang di buat apabila ada pihak yang berminat mengembangkan sekaligus memasarkan secara luas.

Antara lain :

- Alat ini sebaiknya dilengkapi dengan memori eksternal, agar bisa menyimpan harga KWH 1 tahun kebelakang, dan bisa menyimpan data meteran KWH terakhir setiap ada kerusakan yang membuat alat sampai padam.

DAFTAR PUSTAKA

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LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
Jl. Karanglo KM.2 Malang

FORMULIR PERBAIKAN SKRIPSI

Nama : Thomas Dody Prasetya
Nim : 05.12.211
Jurusan : Teknik Elektro S-1
Konsentrasi : Teknik Elektronika
Masa Bimbingan : 29 Mei – 29 November 2009
Judul Skripsi : **PENGHITUNG OTOMATIS PEMBACAAN METERAN AIR MINUM JARAK JAUH PADA PT. CITRA GADING ASTRITAMA DI PERUMAHAN TIRTASANI ESTATE BERBASIS MIKROKONTROLLER AT89S51**

No	Penguji	Tanggal	Uraian	Paraf
1.	Penguji I	06 Oktober 2009	1. Kata Pengantar belum ada. 2. Kesimpulan dilengkapi dari hasil – hasil pengujian antara lain : • Ketelitian alat • Komunikasi dengan PC • Faktor keberhasilan	
2.	Penguji II	06 Oktober 2009	1. Kesimpulan dari hasil pengujian.	

Disetujui

Penguji I

Ir. F. Yudi Limpraptono, MT
NIP .Y. 103 9500 274

Penguji II

I. Komang Somawirata ST, MT
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Mengetahui

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M. Ibrahim Ashari ST, MT
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Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika / T.Infokom, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Tasdiks Prody P.
NIM :
Perbaikan meliputi :

(1). Kata pengantar Belum ada
(2) Kesimpulan dilengkapi dari hasil pengujian antara lain :
- Kelebihan alat
- Komunikasi dg PC
- Faktor kelebihan dll.

Malang, 200

( )

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

ılam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. ıergi Listrik / T. Elektronika / T.Infokom, maka perlu adanya perbaikan skripsi untuk ahasiswa :

AMA : THOMAS D. P.
I M : 05. 12. 261.
rbaikan meliputi :

Kerjakan pulum dari tim penguji

Malang 26-10-2009

( )

PERHITUNGAN OTOMATIS PEMBACAAN METERAN AIR MINUM JARAK JAUH PADA CV.TIRTA ARTISTIK DI PERUMAHAN TIRTASANI ESTATE BERBASIS MIKROKONTROLLER AT89S51

PROPOSAL SKRIPSI

Disusun Oleh :

THOMAS DODY P.

NIM : 05.12.211

Diperiksa dan Disetujui,
Ketua Jurusan Teknik Elektro S-1

Ir. F. YUDI LIMPRAPTONO, MT
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JURUSAN TEKNIK ELEKTRO S -1
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MAKALAH PROPOSAL SKRIPSI

PERHITUNGAN OTOMATIS PEMBACAAN METERAN AIR MINUM JARAK JAUH PADA CV.TIRTA ARTISTIK DI PERUMAHAN TIRTASANI ESTATE BERBASIS MIKROKONTROLLER AT89S51

Diajukan untuk memenuhi persyaratan dalam memperoleh gelar Sarjana Teknik

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2009

INSTITUT TEKNOLOGI NASIONAL MALANG

FAKULTAS TEKNOLOGI INDUSTRI

JURUSAN TEKNIK ELEKTRO S-1

KONSENTRASI TEKNIK ELEKTRONIKA

PENGHITUNG OTOMATIS PEMBACAAN METERAN AIR MINUM JARAK JAUH PADA PT. CITRA GADING ASTRITAMA DI PERUMAHAN TIRTASANI ESTATE BERBASIS MIKROKONTROLLER AT89S51

MAKALAH SEMINAR HASIL

Oleh:

THOMAS DODY P.
05.12.211

Malang, Agustus 2009

Diperiksa dan Disetujui

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PERMOHONAN PERSETUJUAN SKRIPSI

Yang betanda tangan dibawah ini :

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Fakultas : Teknologi Industri
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Konsentrasi : **TEKNIK ELEKTRONIKA**
TEKNIK ENERGI LISTRIK
TEKNIK KOMPUTER DAN INFORMATIKA
Alamat : Jln. Candi Mendut 37

Dengan ini kami mengajukan permohonan untuk mendapatkan persetujuan untuk membuat ***SKRIPSI Tingkat Sarjana.*** Untuk melengkapi permohonan tersebut, bersama kami lampirkan persyaratan-persyaratan yang harus dipenuhi.
Adapun persyaratan-persyaratan pengambilan ***SKRIPSI*** adalah sebagai berikut :

1. Telah melaksanakan semua praktikum sesuai dengan konsentrasinya (✓)
2. Telah lulus dan menyerahkan Laporan Praktek Kerja (✓)
3. Telah lulus seluruh mata kuliah keahlian (MKB) sesuai konsentrasinya (✓)
4. Telah menempuh mata kuliah ≥ 134 sks dengan IPK ≥ 2 dan tidak ada nilai E (✓)
5. Telah mengikuti secara aktif kegiatan seminar skripsi yang diadakan Jurusan (.....)
6. Memenuhi persyaratan administrasi (.....)

Demikian permohonan ini untuk mendapatkan penyelesaian lebih lanjut dan atas perhatiannya kami ucapkan terima kasih.

Telah diteliti kebenaran data tersebut diatas
Recording Teknik Elektro

(Inggi Handayani)

Malang, ...200
Pemohon

(Thomas Dody P.)

Disetujui
Ketua Jurusan Teknik Elektro

Ir. F. Yudi Limpraptono, MT
NIP. Y. 1039500274

Mengetahui
Dosen Wali

(.....)

Catatan :
Bagi mahasiswa yang telah memenuhi persyaratan mengambil SKRIPSI agar membuat proposal dan mendapat persetujuan dari Ketua Jurusan/Sekretaris Jurusan T. Elektro S-1

1. 4.17.5 / 3.02
2. 138

PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL MALANG

INSTITUT TEKNOLOGI NASIONAL MALANG

FAKULTAS TEKNOLOGI INDUSTRI
FAKULTAS TEKNIK SIPIL DAN PERENCANAAN
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Malang, 2 Juni 2009

Nomor : ITN- 919/7/TA /2009
Lampiran :
Perihal : ***Bimbingan Skripsi***

Kepada : Yth. Sdr. M. IBRAHIM ASHARI, ST, MT
Dosen Pembimbing
Jurusan Teknik Elektro S-1
di
Malang

Dengan hormat.
Sesuai dengan permohonan dan persetujuan dalam proposal skipsi untuk mahasiswa:

Nama	: THOMAS DODY PRASETYA
Nim	: 05 12 211
Fakultas	: **Teknologi Industri**
Jurusan	: **Teknik Elektro S-1**
Konsentrasi	: **Teknik Elektronika**

Maka dengan ini pembimbingan tersebut kami serahkan sepenuhnya kepada Saudara/i selama masa waktu 6 (enam) bulan. terhitung mulai tanggal:

29 MEI 2009 s/d 29 NOVEMBER 2009

Sebagai satu syarat untuk menempuh Ujian sarjana.
Demikian atas perhatian serta kerjasama yang baik kami ucapkan terima kasih

Ketua Jurusan
Teknik Elektro S-1

INSTITUT TEKNOLOGI NASIONAL MALANG FAKULTAS TEKNOLOGI INDUSTRI ITN JURUSAN TEKNIK ELEKTRO STRATA-1

Ir. F. Yudi Limpraptono, MT
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Tindasan:
1. Mahasiswa yang Bersangkutan
2. Arsip

Form S-4a

PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL MALANG

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FAKULTAS TEKNOLOGI INDUSTRI
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Perihal : ***Bimbingan Skripsi***

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Jurusan Teknik Elektro S-1
di
Malang

Dengan hormat,
Sesuai dengan permohonan dan persetujuan dalam proposal skipsi untuk mahasiswa:

Nama	: THOMAS DODY PRASETYA
Nim	: 05 12 211
Fakultas	: Teknologi Industri
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika

Maka dengan ini pembimbingan tersebut kami serahkan sepenuhnya kepada Saudara/i selama masa waktu 6 (enam) bulan, terhitung mulai tanggal:

29 MEI 2009 s/d 29 NOVEMBER 2009

Sebagai satu syarat untuk menempuh Ujian sarjana.
Demikian atas perhatian serta kerjasamanya yang baik kami ucapkan terima kasih

Ketua Jurusan
Teknik Elektro S-1

Ir. F. Yudi Limpraptono, MT
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Tindasan:
1. Mahasiswa yang Bersangkutan
2. Arsip

Form S-4a

JURUSAN TEKNIK ELEKTRO S-1
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG

BERITA ACARA SEMINAR PROPOSAL SKRIPSI
PROGRAM STUDI TEKNIK ELEKTRO S1

ONSENTRASI	TEKNIK ELEKTRONIKA

Nama Mahasiswa	THOMAS DODY-P	NIM	0512211
Keterangan Pelaksanaan	Tanggal: 29 MEI 2009	Waktu: 14.30	Tempat / Ruang: SEMINAR

Spesifikasi Judul (berilah tanda silang) *)

a.	Sistem Tenaga Elektrik	e.	Embbeded System	i.	Sistem Informasi
b.	Konversi Energi	f.	Antar Muka	j.	Jaringan Komputer
c.	Sistem Kendali	g.	Elektronika Telekomunikasi	k.	Web
d.	Tegangan Tinggi	h.	Elektronika Instrumentasi	l.	Algoritma Cerdas

Judul Proposal yang diseminarkan Mahasiswa	PERHITUNGAN OTOMATIS PEMBACAAN AIR MINUM JARAK JAUH PADA CV. TIRTA ARTISTIK DI PERUMAHAN TIRTASANI ESTATE BERBASIS MIKROKONTROLLER AT89S51
Perubahan Judul yang diusulkan oleh Kelompok Dosen Keahlian	.....

Catatan :
- permasalahan menyimpang dari judul
- pemilihan alat ?

Catatan :

Persetujuan Judul Skripsi

Disetujui, Dosen Keahlian I	Disetujui, Dosen Keahlian II
.....	.....

Mengetahui, Ketua Jurusan	Disetujui, Calon Dosen Pembimbing	
	Pembimbing I	Pembimbing II
Ir. F. Yudi Limpraptono,MT NIP. Y. 1039500274	M. Ibrahim Ashari	.....

Keterangan :
Dilingkari a, b, c, ... sesuai dengan bidang keahlian

Form S-3c

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura-gura No. 2
MALANG

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Judul skripsi : **Penghitung Otomatis Pembacaan Meteran Air Minum Jarak Jauh Pada PT. CITRA GADING ASTRITAMA di Perumahan Tirtasani Estate Berbasis Mikrokontroller AT89S51**

NO	TANGGAL	URAIAN	PARAF PEMBIMBING
1	3/juli 2009	Bimbingan Bab I + II	
2	13 agustus 2009	BAB III Revisi	
3		ACC Bimbingan Proposal seminar Hasil	
4	11 Sept. 2009	BAB III, IV, V	
5	11 Sept. 2009	Kompre	
6			
7			
8			
9			
10			

Malang,
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Masa Bimbingan : **29 may – 29 November 2009**
Judul skripsi : **Penghitung Otomatis Pembacaan Meteran Air Minum Jarak Jauh Pada PT. CITRA GADING ASTRITAMA di Perumahan Tirtasani Estate Berbasis Mikrokontroller AT89S51**

NO	TANGGAL	URAIAN	PARAF PEMBIMBING
1	30 juni 09	acc Bab I	
2	3 juli 09	Revisi Bab II	
3	14 juli 09	acc Bab III	
4	10 agust 09	acc Bab II	
5		ACC Hasil Bimbingan Proposal seminar	
6	8 sept 09	Revisi bab IV dan bab V.	
7	9 sept 09	acc Bab IV dan bab V.	
8			
9			
10			

Malang,
Dosen Pembimbing I

M. Ibrahim Ashari ST, MT
NIP.Y. 1030100358

```
        org     00h
        ljmp    init

        org     23h
        clr     ES
        jnb     RI,$
        clr     RI
        mov     Dsrl,SBUF
        setb    ES
        reti

        Rest    Bit P1.0                ; RS LCD
        Enbl    Bit P1.1                ; E LCD
        Slct    Bit P3.2                ; selector RS485 -> TX/RX
        Snsr    Bit P3.3                ; sensor hall effect
        Stsn    Bit 20h.0               ; status sensor
        Dsrl    Equ 30h
        Dhg0    Equ 31h
        Dhg1    Equ 32h
        Dhg2    Equ 33h
        Dhg3    Equ 34h
        Dhg4    Equ 35h
        Dhg5    Equ 36h
        Buf0    Equ 40h
        Buf1    Equ 41h
        Buf2    Equ 42h
        Buf3    Equ 43h
        Buf4    Equ 44h
        Buf5    Equ 45h
        Char    Equ 50h
        Cnt0    Equ 51h
        Cnt1    Equ 52h
        Dly0    Equ 53h
        Dly1    Equ 54h
        Dly2    Equ 55h
        Dly3    Equ 56h

it:     lcall   lcd_in                  ; inisialisasi LCD
        lcall   srl_in                  ; inisialisasi serial
        lcall   rstmtr                  ; reset meter
        lcall   rshbll                  ; reset harga bulan lalu

lai:    mov     DPTR,#nama
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#nim
        acall   line2
        mov     Char,#16
        acall   tulis
        mov     Dly3,#20
        lcall   delay3
        mov     DPTR,#jur
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#univ
        acall   line2
        mov     Char,#16
        acall   tulis
        mov     Dly3,#20
        lcall   delay3

op0:    lcall   lcdclr
        lcall   rstcmd
        mov     DPTR,#tpkwmt
```

```
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#angka

ɔp1:    mov     P0,#0C4h
        acall   w_ins
        mov     A,R7
        acall   wr_chr
        mov     A,R6
        acall   wr_chr
        mov     A,R5
        acall   wr_chr
        mov     A,R4
        acall   wr_chr
        mov     P0,#' '
        acall   w_chr
        mov     A,R3
        acall   wr_chr
        mov     A,R2
        acall   wr_chr
        mov     A,R1
        acall   wr_chr
        mov     P0,#0D0h
        acall   w_ins
        acall   delay1
        sjmp    loop1

ting:   acall   lcdclr
        mov     DPTR,#psswrd
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#angka
        mov     P0,#0C5h
        acall   w_ins
        acall   tg_tkn
        mov     Buf0,R0
        mov     A,R0
        acall   wr_chr
        acall   tg_lps
        acall   tg_tkn
        mov     Buf1,R0
        mov     A,R0
        acall   wr_chr
        acall   tg_lps
        acall   tg_tkn
        mov     Buf2,R0
        mov     A,R0
        acall   wr_chr
        acall   tg_lps
        acall   tg_tkn
        mov     Buf3,R0
        mov     A,R0
        acall   wr_chr
        acall   tg_lps
        acall   tg_tkn
        mov     Buf4,R0
        mov     A,R0
        acall   wr_chr
        acall   tg_lps
        acall   tg_tkn
        mov     Buf5,R0
        mov     A,R0
        acall   wr_chr
        acall   tg_lps
```

```
        mov     A,Buf0
        mov     B,#9
        clr     C
        subb    A,B
        jnz     pswslh
        mov     A,Buf1
        mov     B,#8
        clr     C
        subb    A,B
        jnz     pswslh
        mov     A,Buf2
        mov     B,#3
        clr     C
        subb    A,B
        jnz     pswslh
        mov     A,Buf3
        mov     B,#4
        clr     C
        subb    A,B
        jnz     pswslh
        mov     A,Buf4
        mov     B,#7
        clr     C
        subb    A,B
        jnz     pswslh
        mov     A,Buf5
        mov     B,#2
        clr     C
        subb    A,B
        jnz     pswslh
        sjmp    pswbnr
wslh:   mov     DPTR,#stripe
        acall   line2
        mov     Char,#16
        acall   tulis
        mov     Dly3,#5
        lcall   delay3
        mov     SP,#07h
        ljmp    loop0
wbnr:   acall   lcdclr
        mov     DPTR,#tpkwmt
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#angka
        mov     P0,#0C4h
        acall   w_ins
        acall   tg_tkn
        mov     A,R0
        mov     R7,A
        acall   wr_chr
        acall   tg_lps
        acall   tg_tkn
        mov     A,R0
        mov     R6,A
        acall   wr_chr
        acall   tg_lps
        acall   tg_tkn
        mov     A,R0
        mov     R5,A
        acall   wr_chr
        acall   tg_lps
        acall   tg_tkn
        mov     A,R0
        mov     R4,A
```

```
        acall   wr_chr
        acall   tg_lps
        mov     P0,#' '
        acall   w_chr
        acall   tg_tkn
        mov     A,R0
        mov     R3,A
        acall   wr_chr
        acall   tg_lps
        acall   tg_tkn
        mov     A,R0
        mov     R2,A
        acall   wr_chr
        acall   tg_lps
        acall   tg_tkn
        mov     A,R0
        mov     R1,A
        acall   wr_chr
        acall   tg_lps
        mov     Cnt0,#0
        mov     Cnt1,#0
        mov     P0,#0D0h
        acall   w_ins
        mov     SP,#07h
        ljmp    loop0

uest:   mov     DPTR,#tptbll
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#tprpnl
        acall   line2
        mov     Char,#16
        acall   tulis
        mov     P0,#0C6h
        lcall   w_ins
        mov     P0,Dhg0
        lcall   w_chr
        mov     P0,Dhg1
        lcall   w_chr
        mov     P0,Dhg2
        lcall   w_chr
        mov     P0,#'.'
        lcall   w_chr
        mov     P0,Dhg3
        lcall   w_chr
        mov     P0,Dhg4
        lcall   w_chr
        mov     P0,Dhg5
        lcall   w_chr
        mov     P0,#0D0h
        lcall   w_ins
ues:    lcall   scnkpd
        lcall   delay0
        cjne    R0,#11,rques
        mov     SP,#07h
        ljmp    loop0

_sns:   jb      Snsr,bcsns0
        jb      Stsn,bcsns1
        setb    Stsn
        inc     Cnt0
        acall   tbhdta
        sjmp    bcsns1
sns0:   jnb     Snsr,bcsns1
        clr     Stsn
```

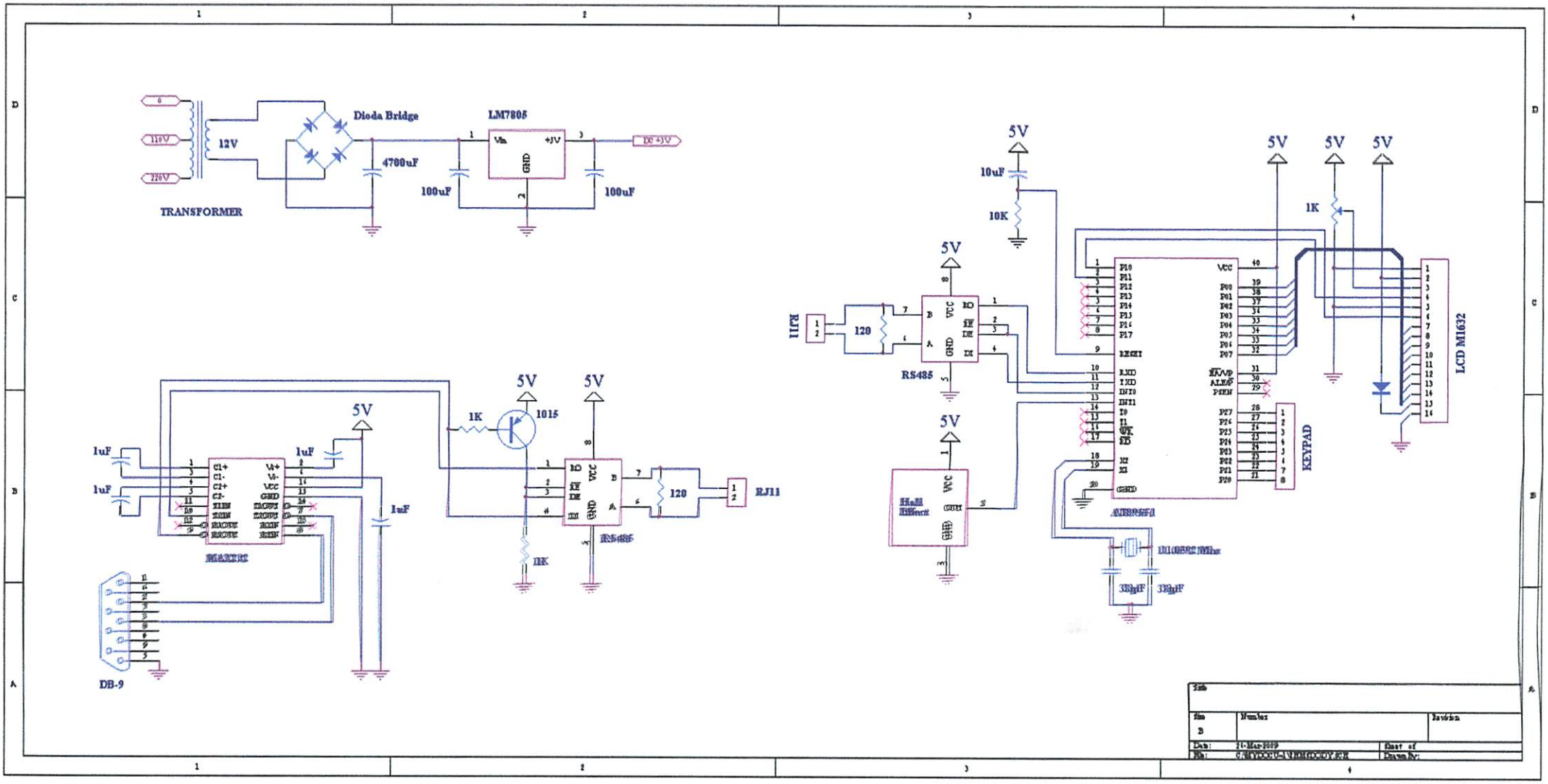
```
;ns1: ret

ıdta: mov     A,Cnt0
      cjne    A,#020,tbhdt0
      mov     A,Cnt1
      cjne    A,#0,tbhdt0
      mov     Cnt1,#1
      ljmp    tbhdt7
ıdt0: cjne    A,#040,tbhdt1
      mov     A,Cnt1
      cjne    A,#1,tbhdt1
      mov     Cnt1,#2
      ljmp    tbhdt7
ıdt1: cjne    A,#060,tbhdt2
      mov     A,Cnt1
      cjne    A,#2,tbhdt2
      mov     Cnt1,#3
      ljmp    tbhdt7
ıdt2: cjne    A,#079,tbhdt3
      mov     A,Cnt1
      cjne    A,#3,tbhdt3
      mov     Cnt1,#4
      ljmp    tbhdt7
ıdt3: cjne    A,#099,tbhdt4
      mov     A,Cnt1
      cjne    A,#4,tbhdt4
      mov     Cnt1,#5
      ljmp    tbhdt7
ıdt4: cjne    A,#119,tbhdt5
      mov     A,Cnt1
      cjne    A,#5,tbhdt5
      mov     Cnt1,#6
      ljmp    tbhdt7
ıdt5: cjne    A,#139,tbhdt6
      mov     A,Cnt1
      cjne    A,#6,tbhdt6
      mov     Cnt1,#7
      ljmp    tbhdt7
ıdt6: cjne    A,#158,tbhdt8
      mov     A,Cnt1
      cjne    A,#7,tbhdt8
      mov     Cnt1,#0
      mov     Cnt0,#0
ıdt7: inc     R1
      cjne    R1,#10,tbhdt8
      mov     R1,#0
      inc     R2
      cjne    R2,#10,tbhdt8
      mov     R2,#0
      inc     R3
      cjne    R3,#10,tbhdt8
      mov     R3,#0
      inc     R4
      cjne    R4,#10,tbhdt8
      mov     R4,#0
      inc     R5
      cjne    R5,#10,tbhdt8
      mov     R5,#0
      inc     R6
      cjne    R6,#10,tbhdt8
      mov     R6,#0
      inc     R7
      cjne    R7,#10,tbhdt8
      mov     R7,#0
ıdt8: ret
```

```
_cmd: mov     A,Dsrl
      cjne    A,#'3',ckcmd0          ; if request 3
      acall   kr_dta
      ljmp    ckcmd1
cmd0: cjne    A,#'4',ckcmd1          ; if request 4
      acall   tg_cmd
      mov     Dhg0,Dsrl
      acall   tg_cmd
      mov     Dhg1,Dsrl
      acall   tg_cmd
      mov     Dhg2,Dsrl
      acall   tg_cmd
      mov     Dhg3,Dsrl
      acall   tg_cmd
      mov     Dhg4,Dsrl
      acall   tg_cmd
      mov     Dhg5,Dsrl

cmd1: mov     Dly3,#2                ; lewati transfer
      lcall   delay3                 ; data meter & bulan lalu
      lcall   rstcmd                 ; reset command
      ret

_dta: mov     A,R6
      mov     B,#30h
      add     A,B
      lcall   kr_srl
      mov     A,R5
      mov     B,#30h
      add     A,B
      lcall   kr_srl
      mov     A,R4
      mov     B,#30h
      add     A,B
      lcall   kr_srl
      mov     A,R3
      mov     B,#30h
      add     A,B
      lcall   kr_srl
      mov     A,R2
      mov     B,#30h
      add     A,B
      lcall   kr_srl
      mov     A,R1
      mov     B,#30h
      add     A,B
      lcall   kr_srl
      ret

l_in: mov     Dly3,#1
      lcall   delay3
      mov     TMOD,#20h
      mov     TH1,#0FDh
      mov     SCON,#50h
      setb    TR1
      setb    ES
      setb    EA
      clr     Slct                   ; RS485 receive
      ret

_srl: setb    Slct                   ; RS485 transmit
      clr     ES
      mov     SBUF,A
      jnb     TI,$
      clr     TI
      setb    ES
```

```
        clr     Slct                    ; RS485 receive
        ret

_cmd:   acall   rstcmd
:md0:   mov     A,Dsrl
        cjne    A,#0FFh,tgcmd1
        sjmp    tgcmd0
:md1:   ret

tcmd:   mov     Dsrl,#0FFh
        ret

tmtr:   mov     R1,#0                   ; reset meter digit 0
        mov     R2,#0                   ; reset meter digit 1
        mov     R3,#0                   ; reset meter digit 2
        mov     R4,#0                   ; reset meter digit 3
        mov     R5,#0                   ; reset meter digit 4
        mov     R6,#0                   ; reset meter digit 5
        mov     R7,#0                   ; reset meter digit 6
        ret

nbll:   mov     Dhg0,#'0'
        mov     Dhg1,#'0'
        mov     Dhg2,#'0'
        mov     Dhg3,#'0'
        mov     Dhg4,#'0'
        mov     Dhg5,#'0'
        ret

nkpd:   mov     R0,#10
        lcall   delay0
l1:     mov     P2,#11111110b
        mov     A,P2
b1:     cjne    A,#11101110b,c1b2
        mov     R0,#1
b2:     cjne    A,#11011110b,c1b3
        mov     R0,#2
b3:     cjne    A,#10111110b,c1b4
        mov     R0,#3
b4:     cjne    A,#01111110b,col2
        mov     R0,#13

l2:     mov     P2,#11111101b
        mov     A,P2
b1:     cjne    A,#11101101b,c2b2
        mov     R0,#4
b2:     cjne    A,#11011101b,c2b3
        mov     R0,#5
b3:     cjne    A,#10111101b,c2b4
        mov     R0,#6
b4:     cjne    A,#01111101b,col3
        mov     R0,#14

l3:     mov     P2,#11111011b
        mov     A,P2
b1:     cjne    A,#11101011b,c3b2
        mov     R0,#7
b2:     cjne    A,#11011011b,c3b3
        mov     R0,#8
b3:     cjne    A,#10111011b,c3b4
        mov     R0,#9
b4:     cjne    A,#01111011b,col4
        mov     R0,#15

l4:     mov     P2,#11110111b
        mov     A,P2
```

```
)1:    cjne    A,#11100111b,c4b2
       mov     R0,#11
)2:    cjne    A,#11010111b,c4b3
       mov     R0,#0
)3:    cjne    A,#10110111b,c4b4
       mov     R0,#12
)4:    cjne    A,#01110111b,back
       mov     R0,#16
:k:    ret

_tkn:  lcall   scnkpd
_tk0:  cjne    R0,#16,tg_tk1
       ljmp    tg_tkn
_tk1:  cjne    R0,#15,tg_tk2
       ljmp    tg_tkn
_tk2:  cjne    R0,#14,tg_tk3
       ljmp    tg_tkn
_tk3:  cjne    R0,#13,tg_tk4
       ljmp    tg_tkn
_tk4:  cjne    R0,#12,tg_tk5
       ljmp    tg_tkn
_tk5:  cjne    R0,#11,tg_tk6
       ljmp    tg_tkn
_tk6:  cjne    R0,#10,tg_tk7
       ljmp    tg_tkn
_tk7:  ret

_lps:  lcall   scnkpd
       cjne    R0,#10,tg_lps
       ret

ıe1:   mov     P0,#080h
       acall   w_ins
       ret

ıe2:   mov     P0,#0C0h
       acall   w_ins
       ret

lis:   clr     A
       acall   wr_chr
       inc     DPTR
       djnz    Char,tulis
       ret

_chr:  movc    A,@A+DPTR
       mov     P0,A
       acall   w_chr
       ret

ins:   clr     Enbl
       clr     Rest
       setb    Enbl
       clr     Enbl
       acall   delay0
       ret

:hr:   clr     Enbl
       setb    Rest
       setb    Enbl
       clr     Enbl
       acall   delay0
       ret

l_in:  mov     Dly3,#1
       lcall   delay3
```

```
        mov     P0,#01h         ; Display Clear
        acall   w_ins
        mov     P0,#38h         ; Function Set
        acall   w_ins
        mov     P0,#0Dh         ; Display On, Cursor, Blink
        acall   w_ins
        mov     P0,#06h         ; Entry Mode
        acall   w_ins
        mov     P0,#02h         ; Cursor Home
        acall   w_ins
        ret

dclr:   mov     P0,#01h         ; Display Clear
        acall   w_ins
        acall   delay0
        acall   delay0
        ret

lay0:   djnz    Dly0,delay0
        ret

lay1:   acall   scnkpd
        cjne    R0,#13,dely10
        ljmp    seting
 y10:   cjne    R0,#14,dely11
        ljmp    rquest
 y11:   mov     A,Dsrl
        cjne    A,#0FFh,dely12
        ljmp    dely13
 y12:   acall   ck_cmd
 y13:   acall   bc_sns
        djnz    Dly1,delay1
        ret

ay2:    mov     Dly2,#20
y2:     acall   delay1
        djnz    Dly2,dely2
        ret

ay3:    lcall   delay0
        djnz    Dly1,delay3
        djnz    Dly3,delay3
        ret

a:      DB      '  Thomas  Dody  '
:       DB      '  NIM: 0512211  '
:       DB      '   T. Elektro   '
/:      DB      '   ITN Malang   '
wmt:    DB      '   Kwh  Meter   '
:kw:    DB      '  Setting  Kwh  '
ll:     DB      'Tagihan Bln Lalu'
nl:     DB      '    Rp     .    '
rd:     DB      '    PASSWORD    '
pe:     DB      '    --------    '
a:      DB      '0123456789      '

        end
```


TRANSFORMER
12V
Dioda Bridge
4700uF
LM7805
Vin
+5V
GND
100uF
100uF
DC +5V
5V
10uF
10K
1K
1015
120
RJ11
RS485
Hall Effect
AT89S52
KEYPAD
LCD M1632
MAX232
DB-9
1uF
1uF
1uF
1uF
1K
1K
120
RJ11
RS485
33pF
33pF
Title
Size
B
Number
Revision
Date: 21-Mar-2009
File: C:\MYCODE\LVMMCODE.PCB
Sheet of
Drawn by:

tures

npatible with MCS®-51 Products
Bytes of In-System Programmable (ISP) Flash Memory
Endurance: 1000 Write/Erase Cycles
V to 5.5V Operating Range
ly Static Operation: 0 Hz to 33 MHz
ee-level Program Memory Lock
x 8-bit Internal RAM
Programmable I/O Lines
16-bit Timer/Counters
Interrupt Sources
l Duplex UART Serial Channel
v-power Idle and Power-down Modes
rrupt Recovery from Power-down Mode
tchdog Timer
al Data Pointer
ver-off Flag
t Programming Time
xible ISP Programming (Byte and Page Mode)

scription

T89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K of In-System Programmable Flash memory. The device is manufactured using l's high-density nonvolatile memory technology and is compatible with the indus-andard 80C51 instruction set and pinout. The on-chip Flash allows the program ory to be reprogrammed in-system or by a conventional nonvolatile memory pro-mer. By combining a versatile 8-bit CPU with In-System Programmable Flash on nolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a y-flexible and cost-effective solution to many embedded control applications.

T89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of , 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-r two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and circuitry. In addition, the AT89S51 is designed with static logic for operation to zero frequency and supports two software selectable power saving modes. dle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and upt system to continue functioning. The Power-down mode saves the RAM con-but freezes the oscillator, disabling all other chip functions until the next external upt or hardware reset.

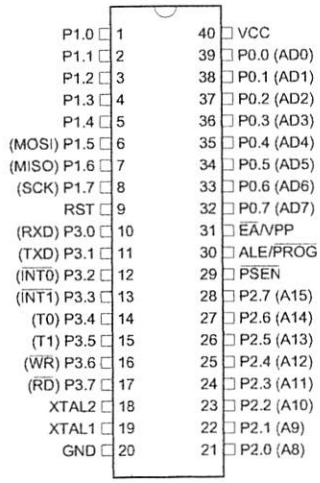
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

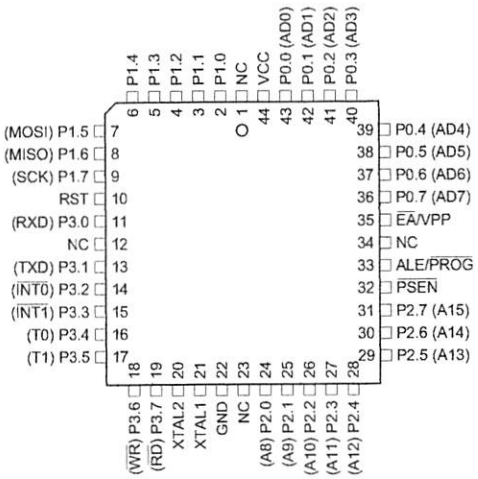
2487B–MICRO–12/03

Configurations

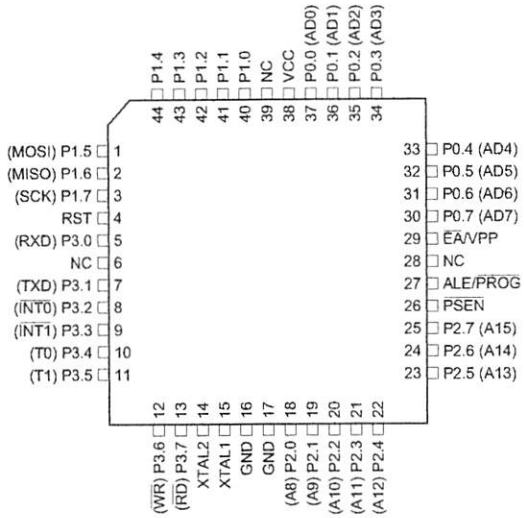
PDIP



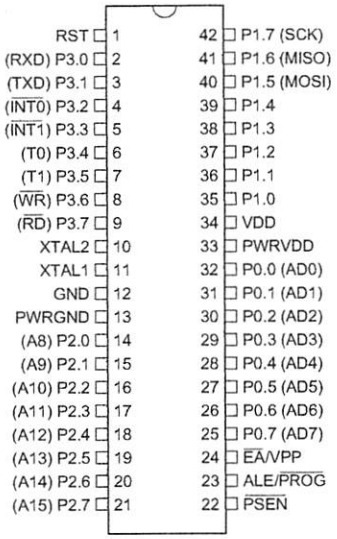
PLCC



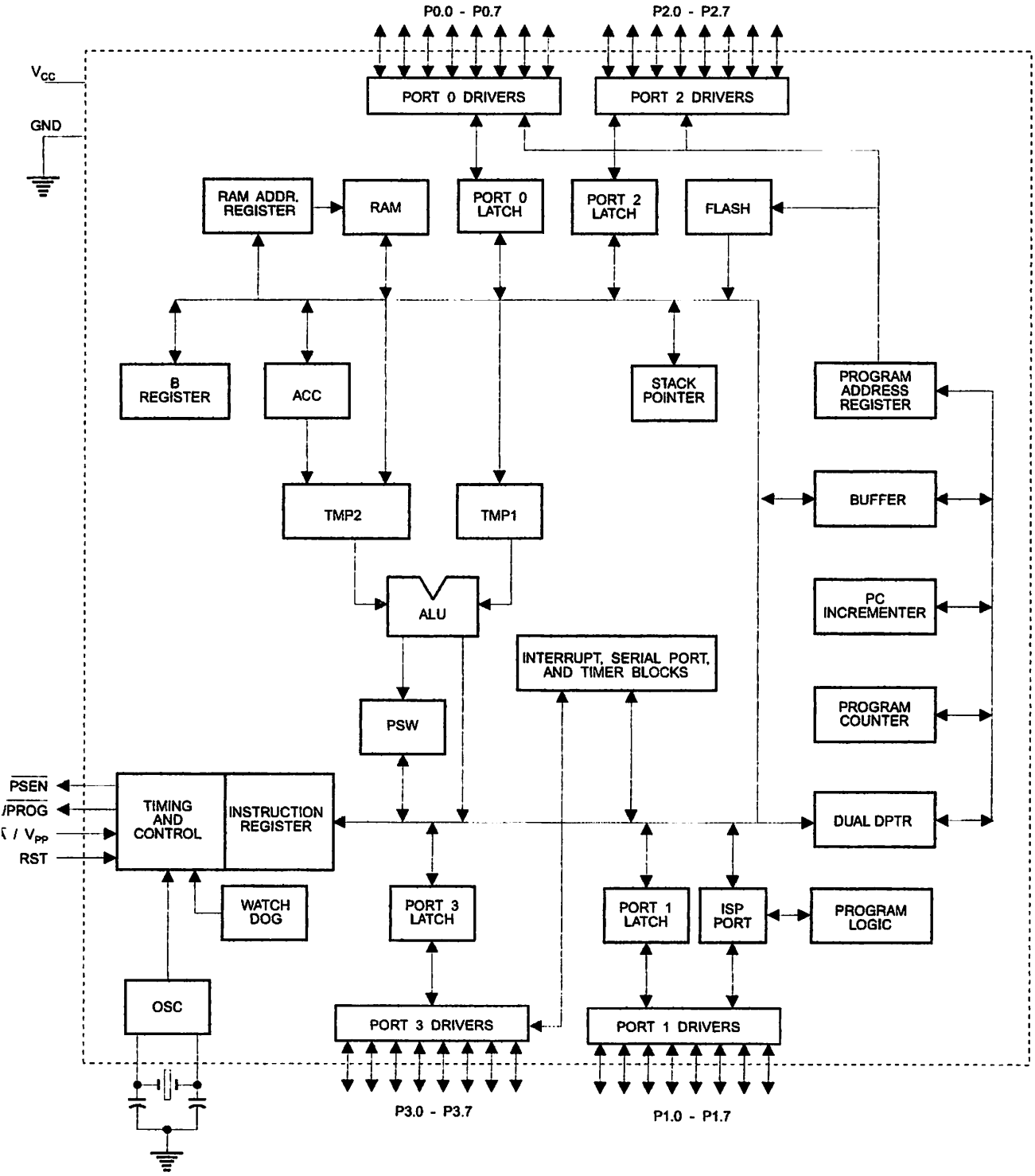
TQFP



PDIP



ck Diagram


P0.0 - P0.7
P2.0 - P2.7
VCC
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PROGRAM COUNTER
PSW
PSEN
/PROG
/ VPP
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
ISP PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

Description

:	Supply voltage (all packages except 42-PDIP).
)	Ground (all packages except 42-PDIP; for 42-PDIP GND connects only the logic core and the embedded program memory).
)	Supply voltage for the 42-PDIP which connects only the logic core and the embedded program memory.
RVDD	Supply voltage for the 42-PDIP which connects only the I/O Pad Drivers. The application board **MUST** connect both VDD and PWRVDD to the board supply voltage.
RGND	Ground for the 42-PDIP which connects only the I/O Pad Drivers. PWRGND and GND are weakly connected through the common silicon substrate, but not through any metal link. The application board **MUST** connect both GND and PWRGND to the board ground.
: 0	Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs. Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification**.
: 1	Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups. Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

t 2	Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{N}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

/PP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

L1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

L2

Output from the inverting oscillator amplifier

ecial
nction
gisters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

e 1. AT89S51 SFR Map and Reset Values

8H									0FFH
0H	B 00000000								0F7H
8H									0EFH
0H	ACC 00000000								0E7H
8H									0DFH
0H	PSW 00000000								0D7H
C8H									0CFH
C0H									0C7H
B8H	IP XX000000								0BFH
B0H	P3 11111111								0B7H
A8H	IE 0X000000								0AFH
A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE
Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset-out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1 Address = A2H Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

nory anization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

ram Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

chdog er e-time bled with et-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

ng the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

[illegible]

[illegible]

[illegible]

T During ver-down Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

RT

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the Atmel Web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture", then "Documentation", and "Other Documents". Open the Adobe® Acrobat® file "AT89 Series Hardware Description".

er 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the Atmel Web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture", then "Documentation", and "Other Documents". Open the Adobe Acrobat file "AT89 Series Hardware Description".

rrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit positions IE.6 and IE.5 are unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

Table 4. Interrupt Enable (IE) Register

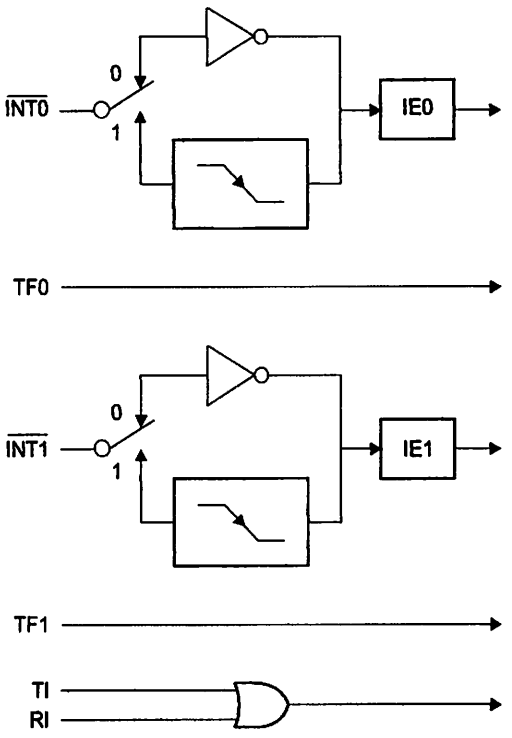
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

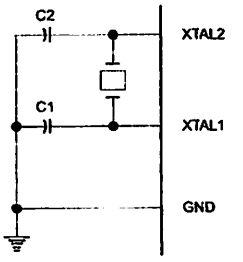
Figure 1. Interrupt Sources



illator racteristics

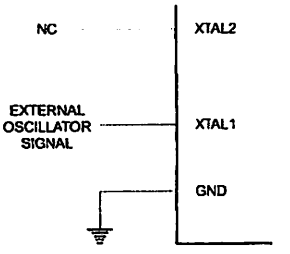
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

ver-down de

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt ($\overline{INT0}$ or $\overline{INT1}$). Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

gram nory Lock s

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

gramming Flash – allel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash Programming Modes table (Table 7) and Figures 4 and 5. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. **The status of the individual lock bits can be verified directly by reading them back.**

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates AT89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

gramming Flash – ial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

al ıramming ırithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

$\overline{\text{Data}}$ Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

al gramming ruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8.

gramming rface – allel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer worldwide support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

7. Flash Programming Modes

e	V_{CC}	RST	$\overline{\text{PSEN}}$	ALE/ $\overline{\text{PROG}}$	$\overline{\text{EA}}$/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
Code Data	5V	H	L	(2) ⌣	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
Lock Bit 1	5V	H	L	(3) ⌣	12V	H	H	H	H	H	X	X	X
Lock Bit 2	5V	H	L	(3) ⌣	12V	H	H	H	L	L	X	X	X
Lock Bit 3	5V	H	L	(3) ⌣	12V	H	L	H	H	L	X	X	X
Lock Bits 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Erase	5V	H	L	(1) ⌣	12V	H	L	H	L	L	X	X	X
Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

:
1. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{\text{BSY}}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

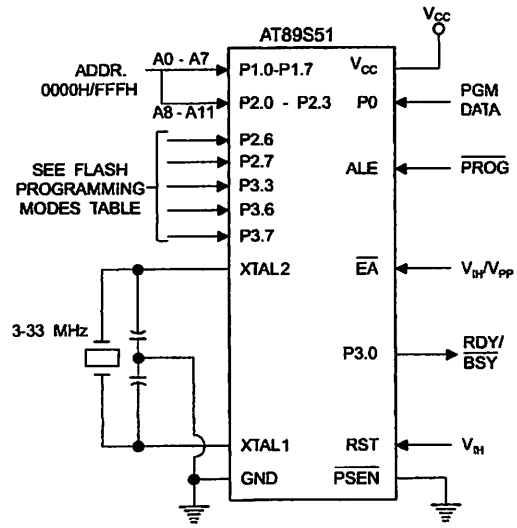
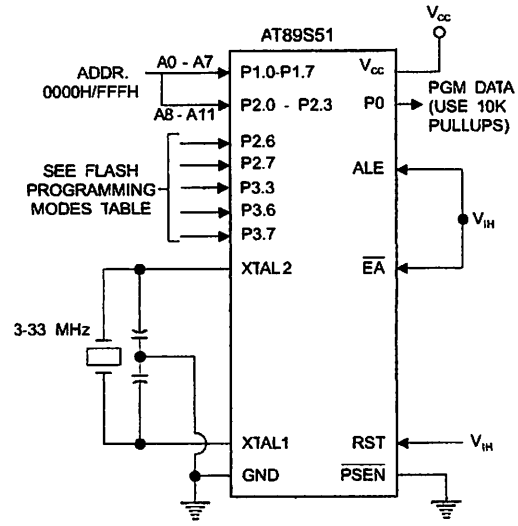


Figure 5. Verifying the Flash Memory (Parallel Mode)

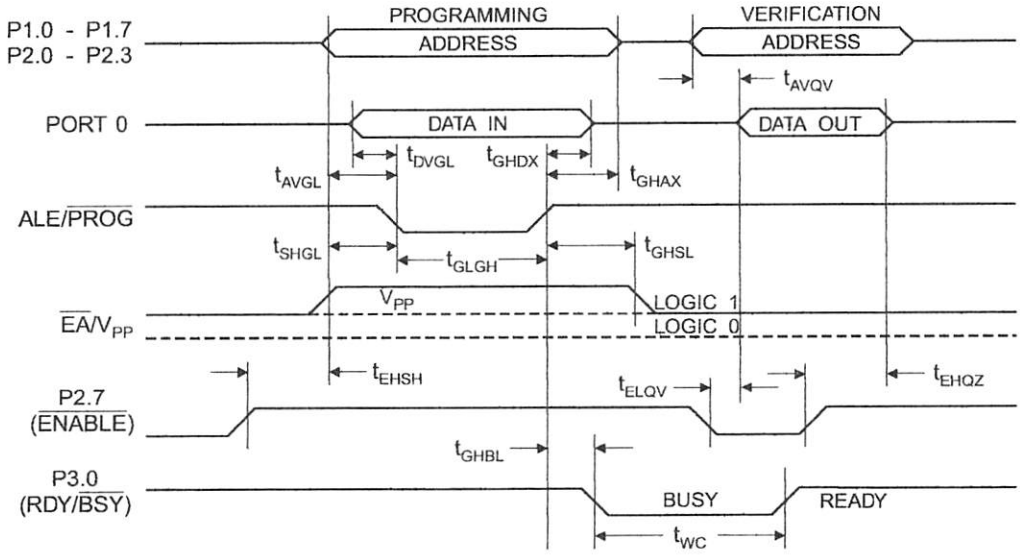


sh Programming and Verification Characteristics (Parallel Mode)

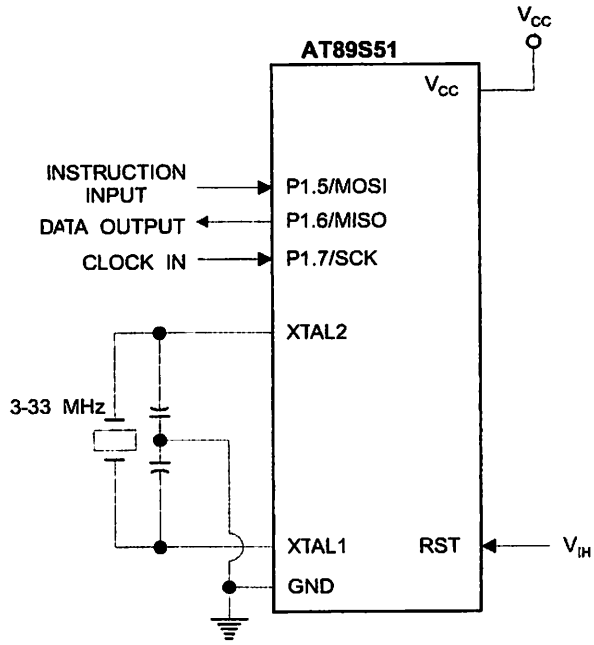
20°C to 30°C, V_{CC} = 4.5 to 5.5V

bol	Parameter	Min	Max	Units
	Programming Supply Voltage	11.5	12.5	V
	Programming Supply Current		10	mA
	V_{CC} Supply Current		30	mA
CL	Oscillator Frequency	3	33	MHz
	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
X	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
X	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
H	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
L	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
L	V_{PP} Hold After $\overline{PROG}$	10		µs
H	$\overline{PROG}$ Width	0.2	1	µs
V	Address to Data Valid		$48t_{CLCL}$	
V	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
Z	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
L	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		50	µs

re 6. Flash Programming and Verification Waveforms – Parallel Mode

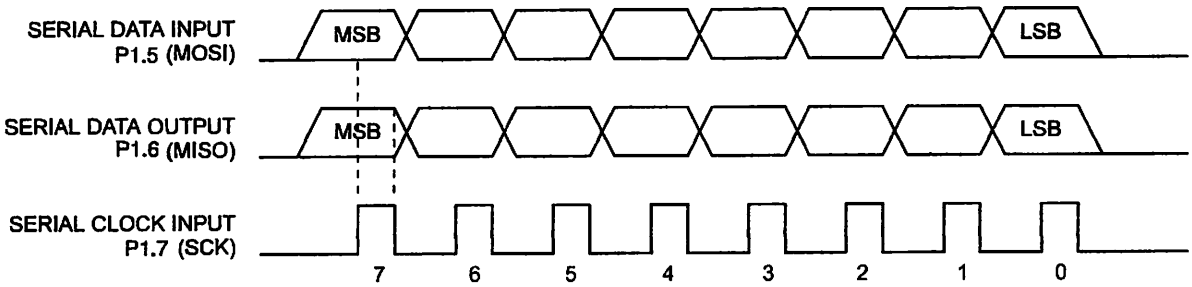


e 7. Flash Memory Serial Downloading



sh Programming and Verification Waveforms – Serial Mode

e 8. Serial Programming Waveforms



8. Serial Programming Instruction Set

ruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
ramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
d Program Memory e Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
e Program Memory e Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
e Lock Bits(1)	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
d Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xxx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
d Signature Bytes	0010 1000	xxxx A11 A10 A9 A8	A7 xxx xxx0	Signature Byte	Read Signature Byte
d Program Memory e Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
e Program Memory e Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

1. B1 = 0, B2 = 0 → Mode 1, no lock protection
   B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
   B1 = 1, B2 = 1 → Mode 4, lock bit 3 activated

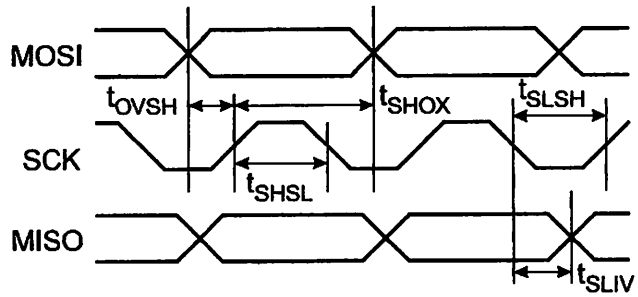
   } Each of the lock bit modes need to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

rial Programming Characteristics

ure 9. Serial Programming Timing



ble 9. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

ymbol	Parameter	Min	Typ	Max	Units
t_{CLCL}	Oscillator Frequency	3		33	MHz
LCL	Oscillator Period	30			ns
HSL	SCK Pulse Width High	8 t_{CLCL}			ns
LSH	SCK Pulse Width Low	8 t_{CLCL}			ns
VSH	MOSI Setup to SCK High	t_{CLCL}			ns
HOX	MOSI Hold after SCK High	2 t_{CLCL}			ns
LIV	SCK Low to MISO Valid	10	16	32	ns
RASE	Chip Erase Instruction Cycle Time			500	ms
WC	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

solute Maximum Ratings*

rating Temperature ..... -55°C to +125°C

age Temperature ..... -65°C to +150°C

age on Any Pin
Respect to Ground .....-1.0V to +7.0V

imum Operating Voltage 6.6V

Output Current ..... 15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

bol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
	Output Low Voltage(1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
	Output Low Voltage(1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
1	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
ST	Reset Pulldown Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode(2)	V_{CC} = 5.5V		50	µA

s: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

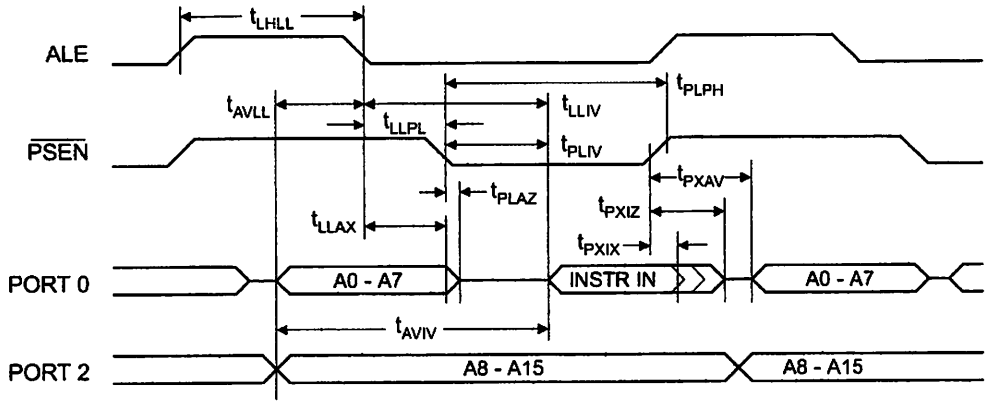
Characteristics

· operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other ts = 80 pF.

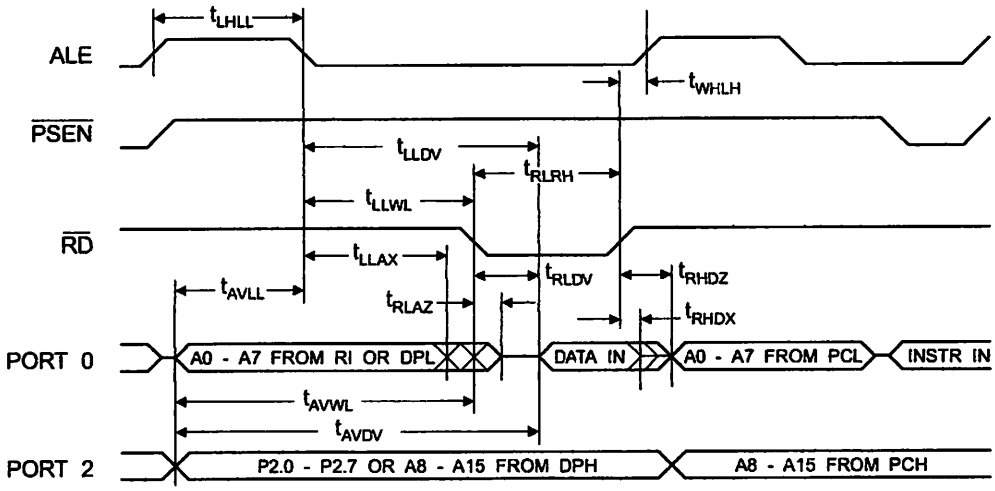
ernal Program and Data Memory Characteristics

bol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
CL	Oscillator Frequency			0	33	MHz
	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
	Address Valid to ALE Low	43		t_{CLCL}-25		ns
	Address Hold After ALE Low	48		t_{CLCL}-25		ns
	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
	$\overline{PSEN}$ Low to Address Float		10		10	ns
l	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
H	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
(	Data Hold After $\overline{RD}$	0		0		ns
?	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
x	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
H	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
x	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
	$\overline{RD}$ Low to Address Float		0		0	ns
H	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

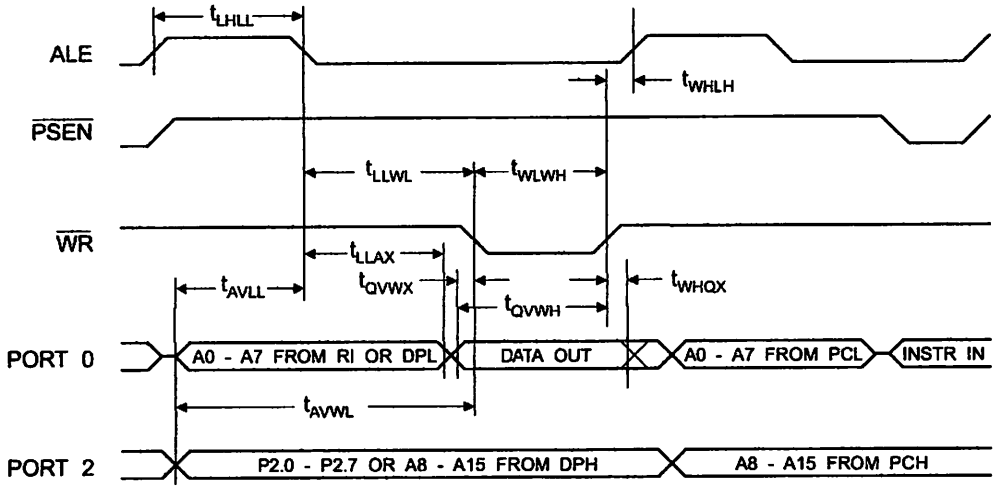
ernal Program Memory Read Cycle



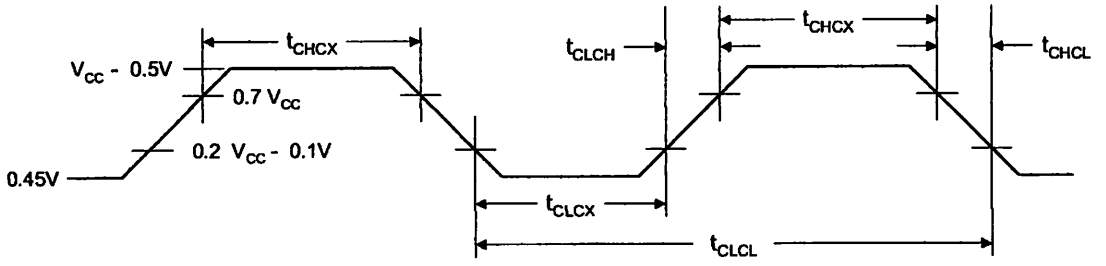
ernal Data Memory Read Cycle



ernal Data Memory Write Cycle



ernal Clock Drive Waveforms



ernal Clock Drive

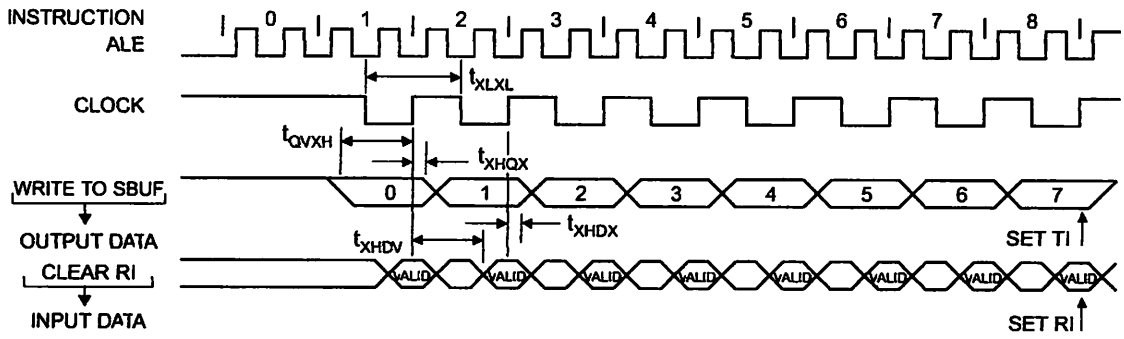
bol	Parameter	Min	Max	Units
CL	Oscillator Frequency	0	33	MHz
	Clock Period	30		ns
(	High Time	12		ns
:	Low Time	12		ns
I	Rise Time		5	ns
.	Fall Time		5	ns

ial Port Timing: Shift Register Mode Test Conditions

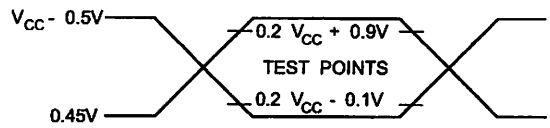
/alues in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

ıbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
.	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
-ı	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
x	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
x	Input Data Hold After Clock Rising Edge	0		0		ns
v	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

ft Register Mode Timing Waveforms

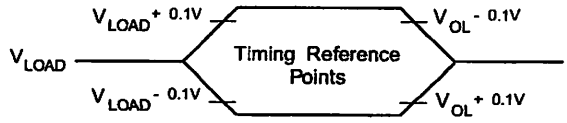


Testing Input/Output Waveforms(1)



1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

at Waveforms(1)



1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

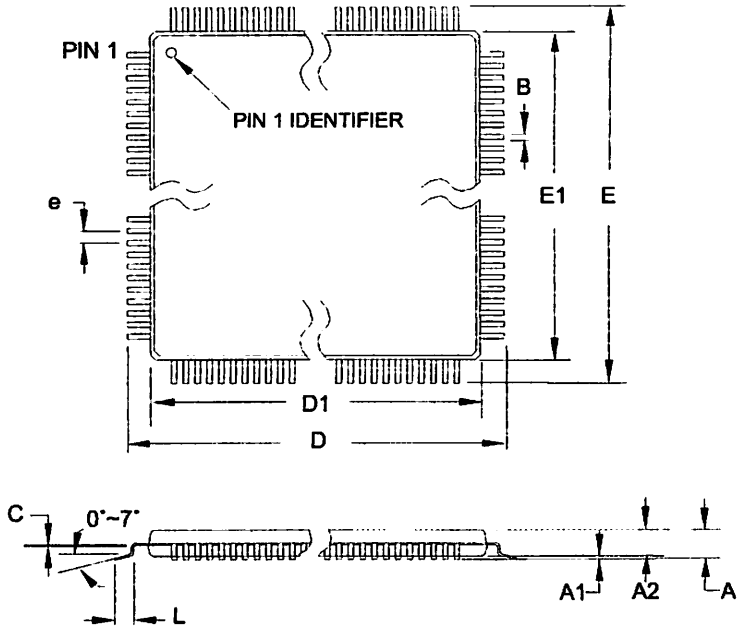
ering Information

ıeed IHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC AT89S51-24SC	44A 44J 40P6 42PS6	Commercial (0° C to 70° C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI AT89S51-24SI	44A 44J 40P6 42PS6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC AT89S51-33SC	44A 44J 40P6 42PS6	Commercial (0° C to 70° C)

	Package Type
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S6	42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

:kaging Information

– TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

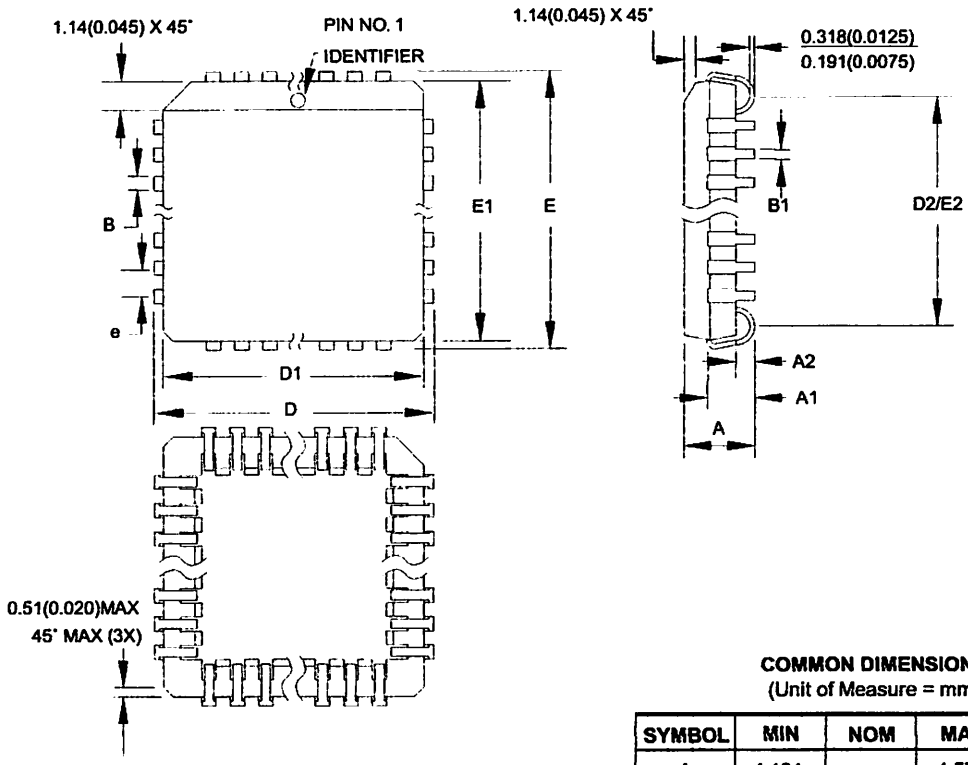
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

– PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

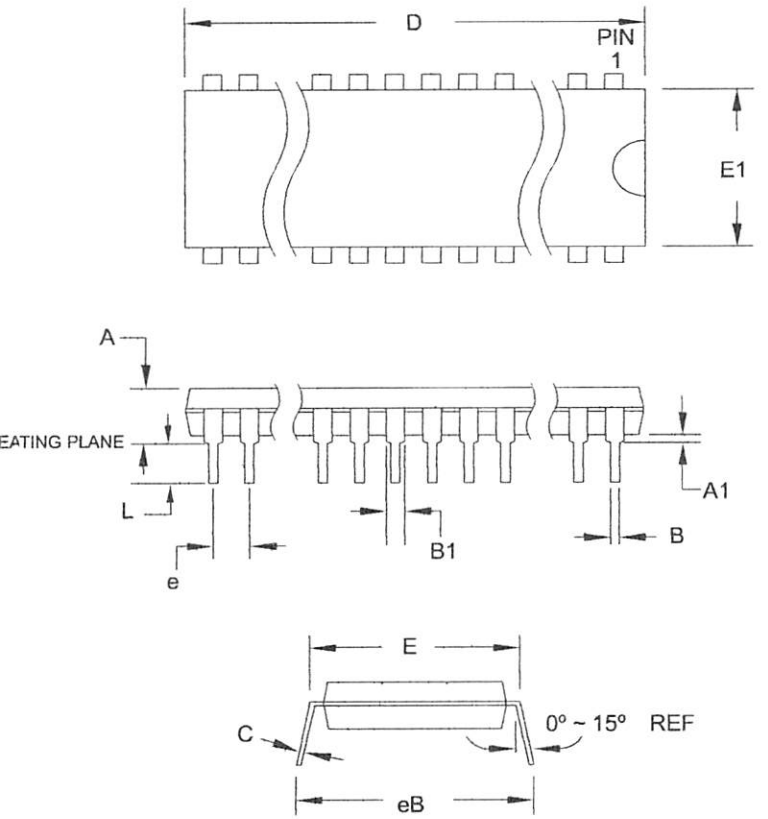
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

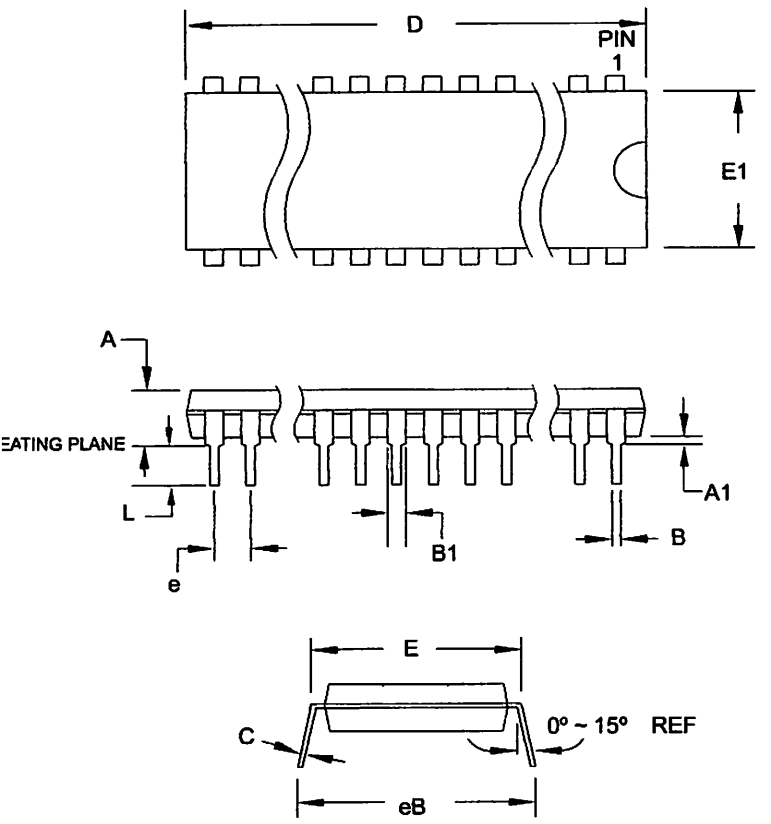
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.83	
A1	0.51	–	–	
D	36.70	–	36.96	Note 2
E	15.24	–	15.88	
E1	13.46	–	13.97	Note 2
B	0.38	–	0.56	
B1	0.76	–	1.27	
L	3.05	–	3.43	
C	0.20	–	0.30	
eB	–	–	18.55	
e	1.78 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/6/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**42PS6**, 42-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	42PS6	A

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2487B–MICRO–12/03

COMPLEMENTARY OUTPUT HALL EFFECT LATCHED SINK DRIVER

FEATURES

- On-chip Hall sensor with two different sensitivity and hysteresis settings for A276/A277.
- Internal bandgap regulator allows temperature compensated operations and a wide operating voltage range.
- High output sinking capability up to 300mA for driving large load.
- Lower current change rate reduces the peak output voltages during switching.
- Build in protection diode for chip reverse power connecting.
- Available in die form or rugged low profile 4 pin SIP packages.

GENERAL DESCRIPTION

A276/A277 are integrated Hall sensors with output drivers designed for electronic commutation of brushless DC motor applications. The device includes an on-chip Hall voltage generator for magnetic sensing, a comparator that amplifies the Hall voltage, and a Schmitt trigger to provide switching hysteresis for noise rejection, and complementary open-collector drivers for sinking large current loads. An internal bandgap regulator is used to provide temperature compensated supply voltage for internal circuits and allows a wide operating supply range.

If a magnetic flux density larger than threshold Bop, DO is turned on(low) and DOB is turned off (high). The output state is held until a magnetic flux density reversal falls below Brp causing DO to be turned off and DOB turned on.

A276/A277 are rated for operation over temperature range from -20 °C to 85 °C and voltage range from 3.5V to 20V. The devices are available in low cost die forms or rugged 4 pin SIP packages.

APPLICATIONS

- Brushless DC Motor
- Brushless DC Fan
- Revolution Counting
- Speed Measurement

COMPLEMENTARY OUTPUT VERTICAL DEFLECT LATCHED SINK DRIVER

FEATURES

- Complete self contained vertical deflection solution for monitors and TV receivers
- Internal protection against output short circuits
- Low power consumption
- Low cost
- Internal thermal shutdown
- Protection in the form of a current limit protection (for DIP packages)

GENERAL DESCRIPTION

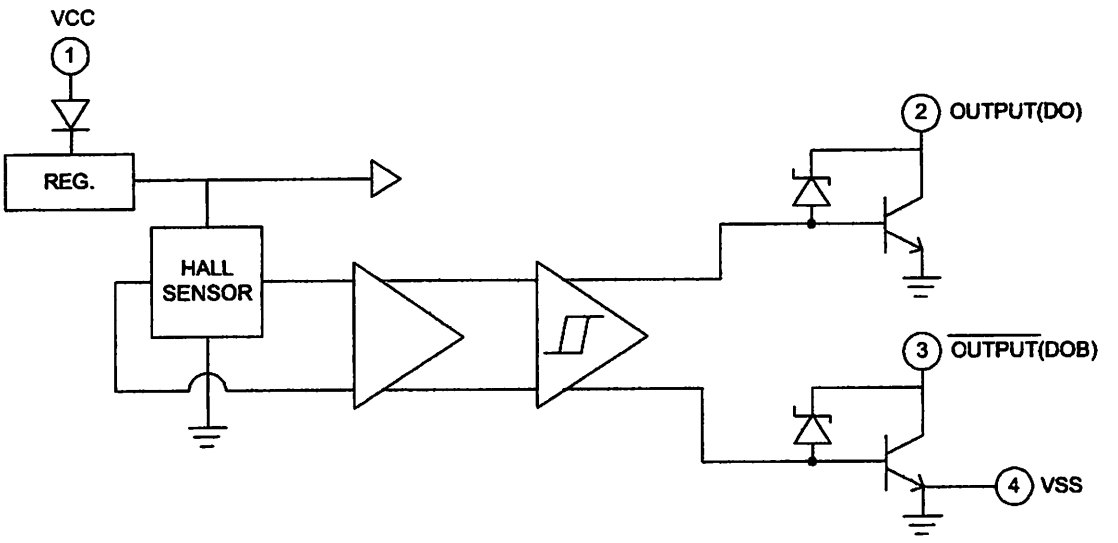
A279/A277 are integrated circuits in a bipolar process designed for deflection applications. It provides the functions for a complete vertical deflection system. The device includes a sawtooth generator, a comparator, an error amplifier, a flyback generator, a power-on/off protection, and a thermal trigger circuit. A switching preamplifier for using a separate power stage is also included. An internal reference voltage for the error amplifier and a voltage regulator are also included. Supply voltage range

A279/A277 are rated for operation over a temperature range from -25°C to 85°C and supply voltage from 9V to 30V. The device has a maximum peak output current of 1.5A (DIP package) or 2A (SIP package).

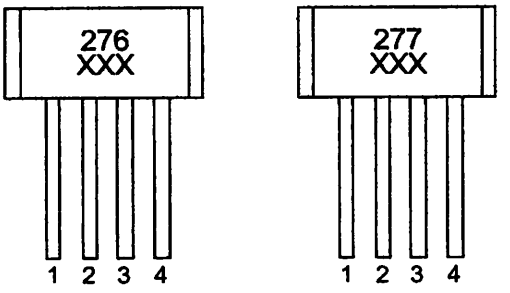
APPLICATIONS

- Small size CC monitor
- Standard CC TVs
- Industrial CC monitor
- Speed telewriter equipment

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION



1 : VCC

2 : DO

3 : D0B

4 : VSS

REMARK : XXX : DATE CODE (ex : 52Z)
52 : WEEK (ex=>52:52 WEEK . 35:35 WEEK)
Z : YEAR (ex=>Z:DC2001 , Y:DC2002 , X:DC2003)

Name	P/I/O	Pin #	Description
Vcc	P	1	Positive Power Supply
DO	O	2	Output Pin
DOB	O	3	Output Pin
Vss	P	4	Ground

[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
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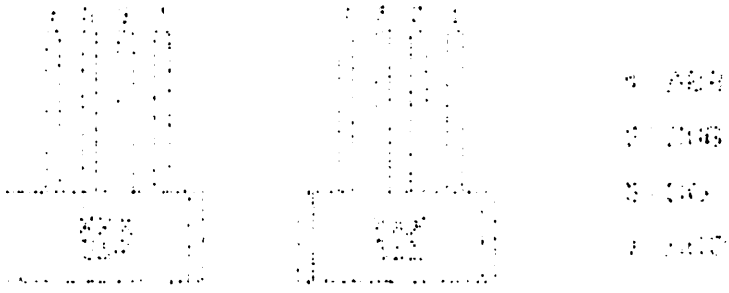

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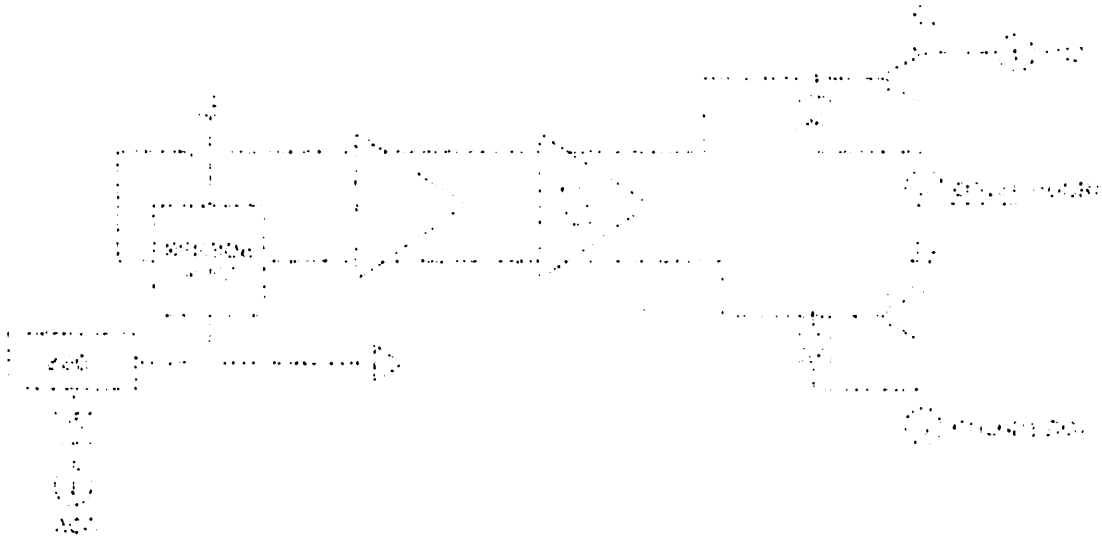

[illegible]

ABSOLUTE MAXIMUM RATING (at Ta=25 °C)

Supply Voltage, Vcc ---------- 20V
Reverse V_{CC} Polarity Voltage, V_{RCC} ---------- -35V
Magnetic flux density, B ---------- Unlimited
Output OFF Voltage, Vce ---------- 50V(Note 1)
Output ON Current, Ic
Continuous ---------- 300mA
Hold ---------- 400mA
Peak (Start Up) ---------- 700mA
Operating Temperature Range,
Ta ---------- (-20 °C to +85 °C)
Storage Temperature Range,
Ts ---------- (-65 °C to +150 °C)
Package Power Dissipation,
Pd ---------- 500mW
Maximum Junction Temp , Tj ---------- 175 °C

(Note1) Output Zener protection voltage.

ELECTRICAL CHARACTERISTICS (Ta =+25 °C , Vcc=4.0V to 20V)

Characteristic	Symbol	Conditions	Min	Typ	Max	Units
Low Supply Voltage	Vce	Vcc=3.5V, IL=100mA	—	0.4	—	V
Supply Voltage	Vcc	—	3.5	—	20	V
Output Saturation Voltage	Vce(sat)	Vcc=14V, IL=300mA	—	600	900	mV
Output Leakage Current	Icex	Vce=14V, Vcc=14V	—	< 0.1	10	uA
Supply Current	Icc	Vcc=20V, Output Open	—	13	20	mA
Output Rise Time	tr	Vcc=14V, RL=820Ω, CL=20pF	—	3.0	10	us
Output Falling Time	tf	Vcc=14V, RL=820Ω, CL=20pF	—	0.3	1.5	us
Switch Time Differential	Δt	Vcc=14V, RL=820Ω, CL=20pF	—	3.0	10	us

[illegible] Technologies Inc.

ABSOLUTE MAXIMUM RATING (at Temp=[illegible])

[illegible]

ELECTRICAL CHARACTERISTICS (Ta=[illegible], Vcc=[illegible], Vcm=[illegible])

Characteristic	Symbol	Conditions	Min	Typ	Max	Units
[illegible]	[illegible]	[illegible]	—	[illegible]	—	[illegible]
[illegible]	[illegible]	—	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	—	[illegible]	[illegible]	[illegible]
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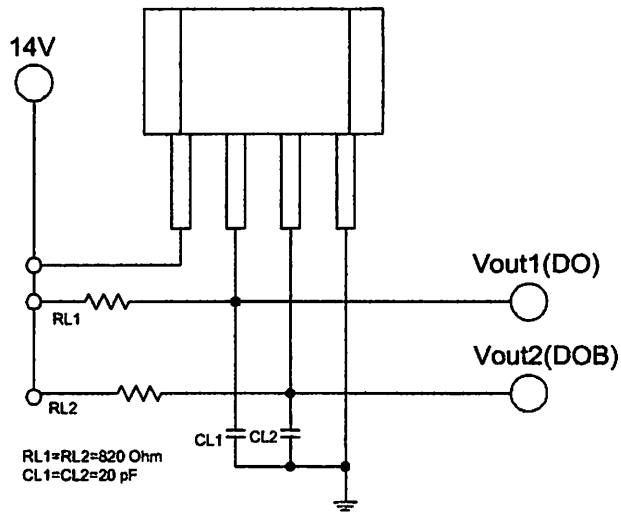
[illegible]	[illegible]	[illegible]	—	[illegible]	[illegible]	[illegible]

MAGNETIC CHARACTERISTICS

Characteristic		Symbol	Ta=+25 °C Min	Ta=+25 °C Max	Ta=0 °C to 70 °C Min	Ta=0 °C to 70 °C Max	Units
Operate Point	A276	Bop	—	100	—	100	G
	A277	Bop	0	70	0	70	G
Release Point	A276	Brp	-100	—	-100	—	G
	A277	Brp	-70	0	-70	0	G
Hysteresis	A276	Bhys	50	150	30	200	G
	A277	Bhys	40	110	20	140	G

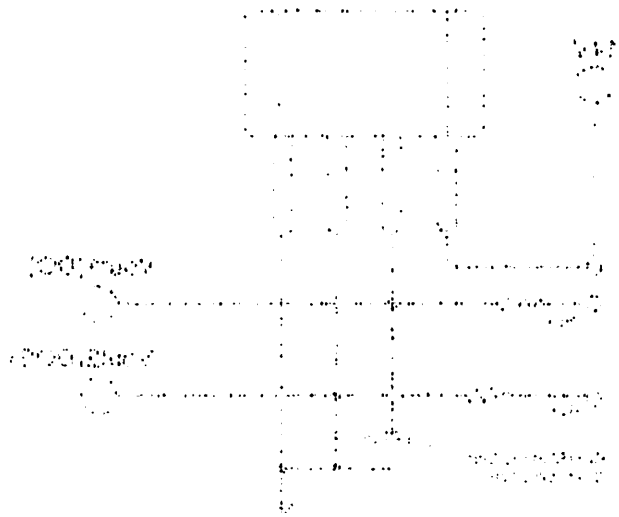
TEST CIRCUIT



MAGNETIC CHARACTERISTICS

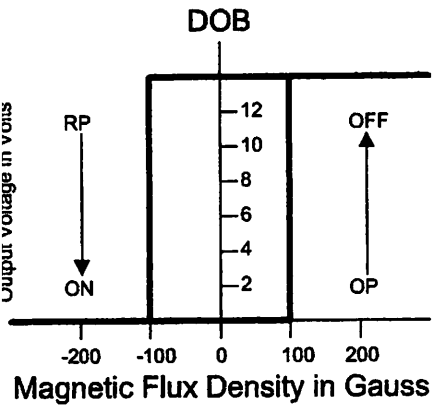
Characteristic	Typical		Temperature Min	Temperature Max	Temperature Min	Temperature Max	Units
Operate Point	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	G
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	G
Release Point	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	G
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	G
Hysteresis	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	G
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	G

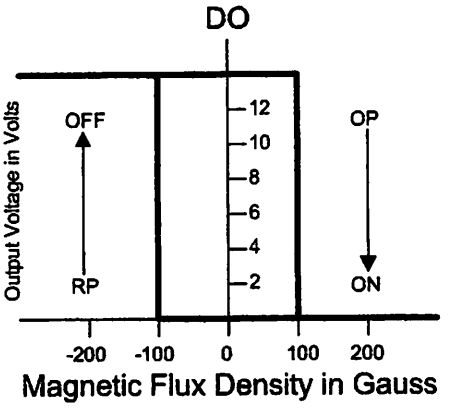
TEST CIRCUIT



HYSTERESIS CHARACTERISTICS

A276





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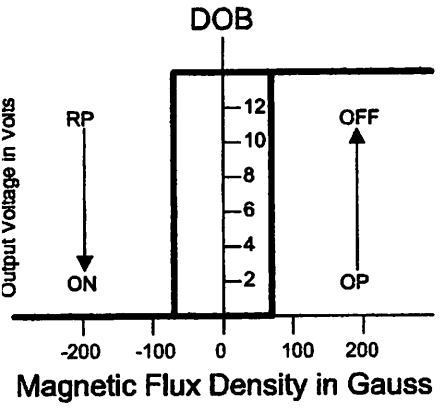
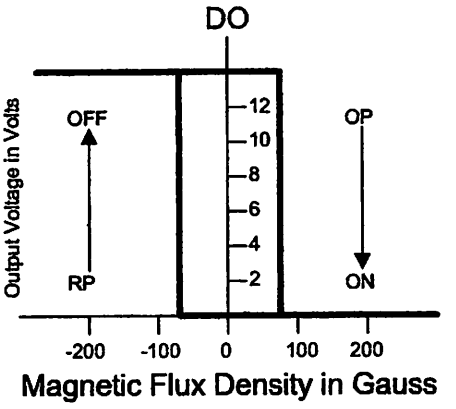
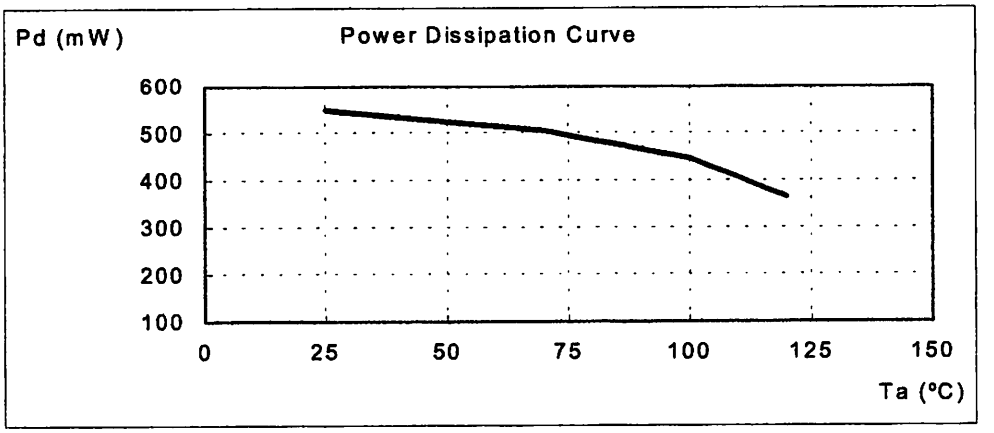


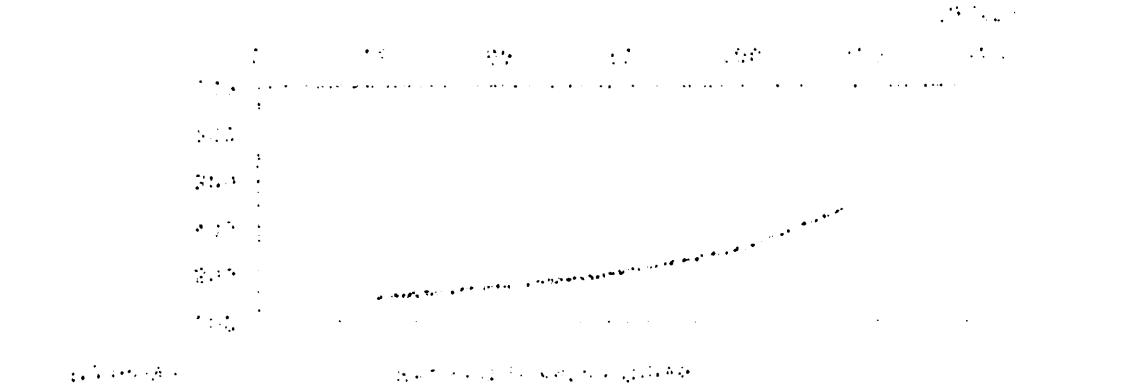


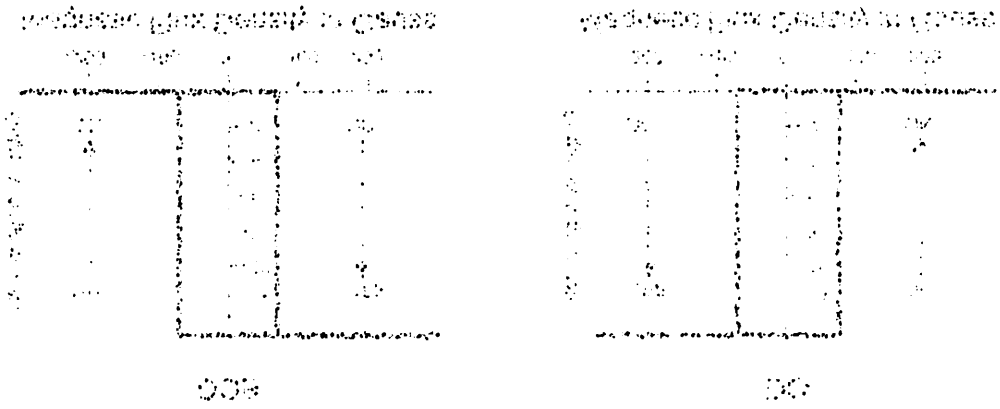
POWER DISSIPATION VS. ENVIRONMENT TEMPERATURE

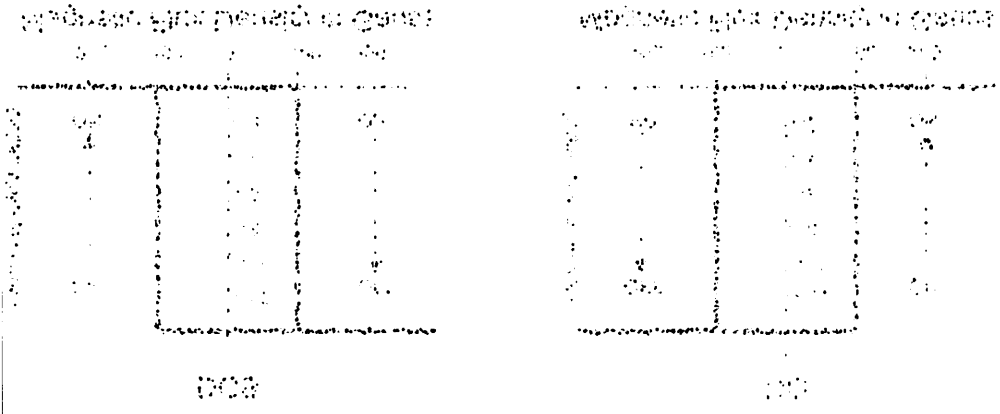
Ta (°C)	25	50	60	70	80	85	90	95	100	105	110	115	120
Pd (mW)	550	525	515	505	485	475	465	455	445	425	405	385	365



Note : TO92 4 pin (SIP-4L) package.

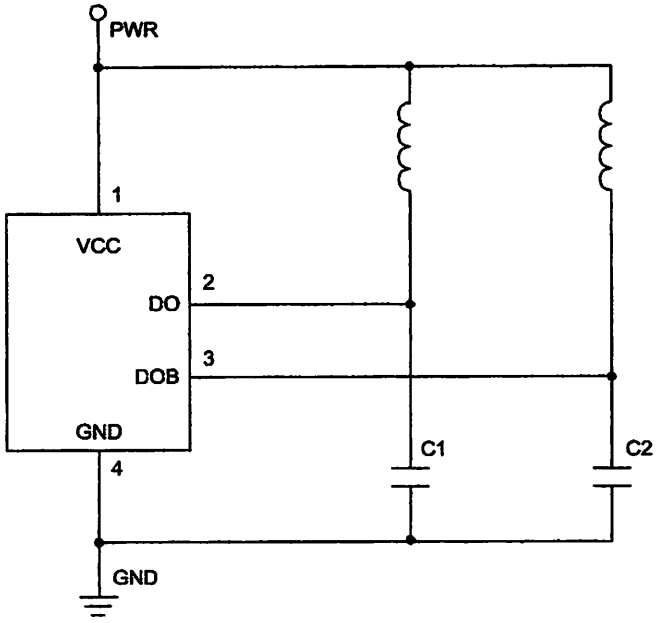






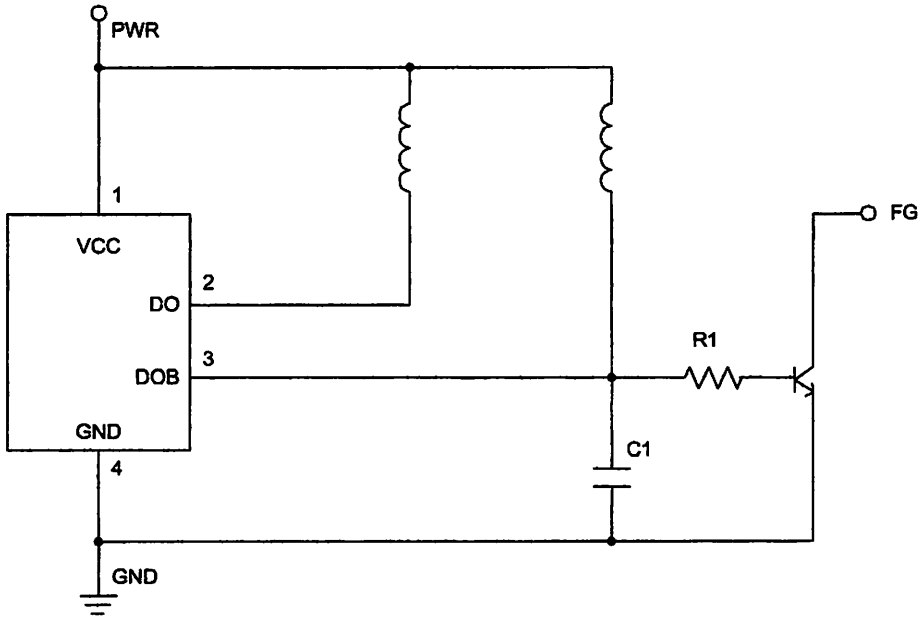
APPLICATION CIRCUITS - DOUBLE COIL

1.Output on current , Ic > 250mA



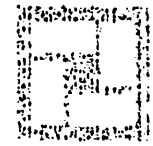
Remark : C1,C2:Capacitor 2.2μF~4.7μF(optional)

2.With FG output



Remark : C1:Capacitor 0.1μF~1μF

R1:Resister 1KΩ



APPLICATION CIRCUITS - SOURCE CTRL

1.Output in Reverse, R_S > 250mA

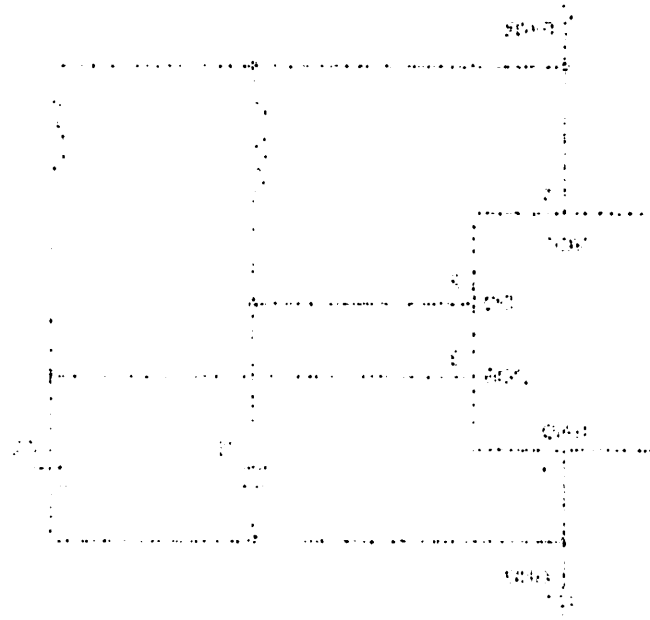


Figure 1: Circuit Diagram Typical Application

2.With FD Output

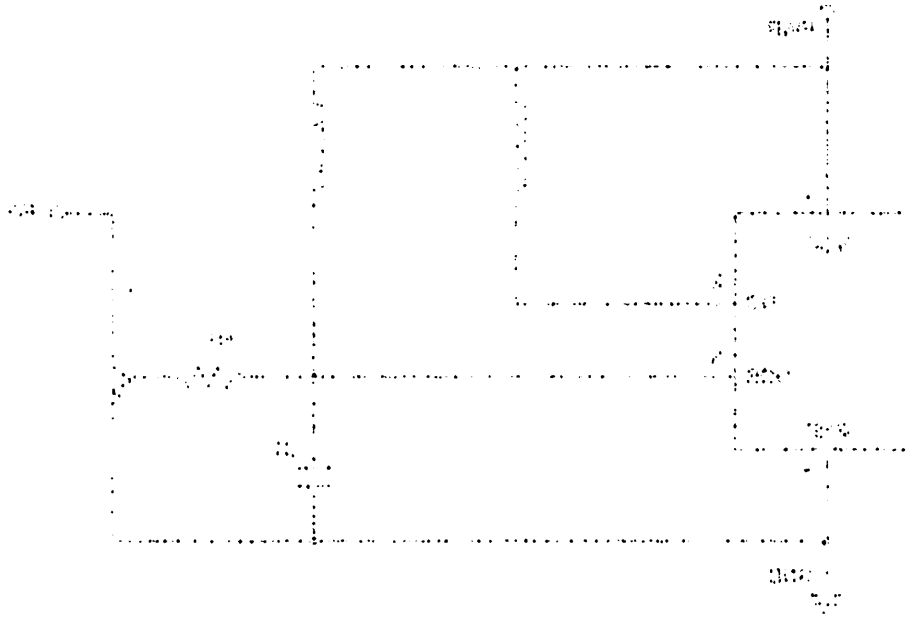
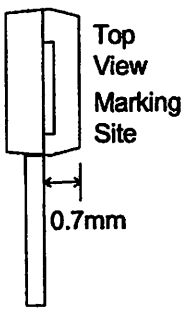


Figure 2: Circuit Diagram Typical Application

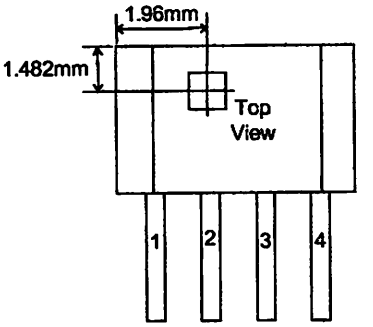
(FD Pin Used)

PACKAGE INFORMATION

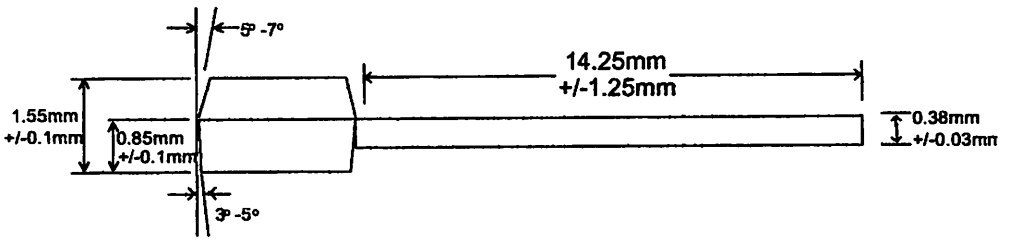
Active Area Depth

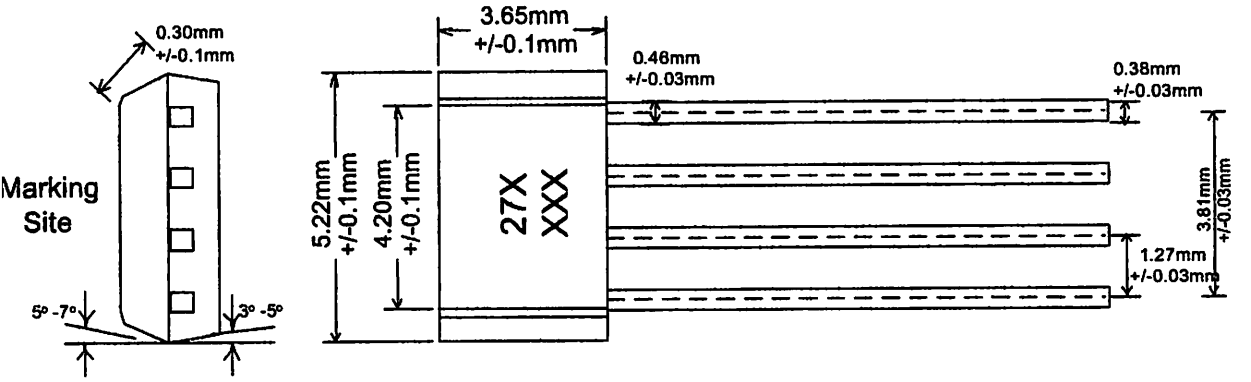


Package Sensor Location



PACKAGE DIMENSION





REMARK:27X(276 or 277)
XXX(DATE CODE)

SPECIFICATION

Model: LMB162A

1. BASIC SPECIFICATIONS

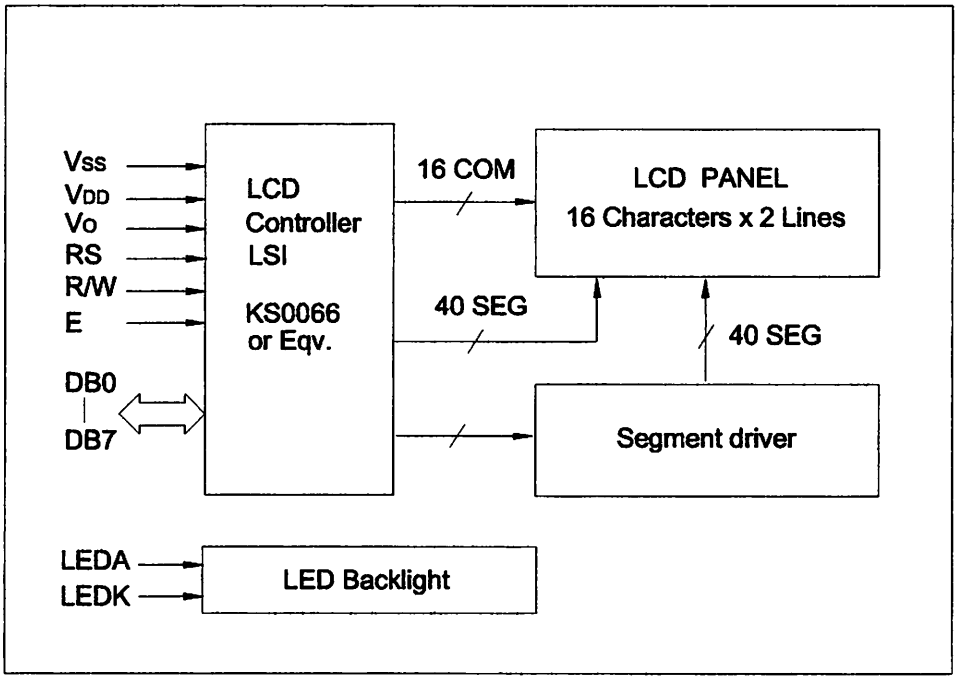
1.1 Display Specifications

LCD Mode	:	STN—Positive—Transflective
Display Color	:	Dark Blue
Background Color	:	Yellow-Green
Driving Duty	:	1/16 Duty
Viewing Direction	:	6:00
Backlight	:	LED

1.2 Mechanical Specifications

Outline Dimension	:	80.0(W) X 36.0(H) X 14.0(T)	mm
Viewing Area	:	64.6(W) X 16.0(H)	mm
Number of Characters	:	16 Characters X 2 Lines	
Character Size	:	2.95 X 5.55	mm
Dot Size	:	0.55 X 0.65	mm
Weight	:		

1.3 Block Diagram



1. BASIC SPECIFICATIONS

1.1 Display Specifications

LCD Mode	:	STN – Positive – Transflective
Display Color	:	Dark Blue
Background Color		Yellow-Green
Driving Duty	:	1/16 Duty
Viewing Direction	:	6O'C
Backlight	:	LED

1.2 Mechanical Specifications

Outline Dimension	:	60.0(W) X 36.0(H) X 4.4 (T)	mm
Viewing Area	:	54.0(W) X 16.0(H)	mm
Number of Characters	:	16 Characters X 2 Lines	
Character Size	:	2.45 X 3.85	mm
Dot Size	:	0.55 X 0.65	mm
Weight	:		

1.3 Block Diagram

Vss	:			
Vdd	:	LCD		LCD PANEL
Vo	:	Controller		16 Characters x 2 Lines
RS	:	LSI		
R/W	:			
E	:	Ratioder		
		IC Con.		
DB0				
DB7				Segment Driver
LED A	:			
LED K	:	LED Backlight		

1.4 Terminal Functions

Pin No.	Symbol	Level	Function
1	VSS	-	Ground
2	VDD	-	Power Supply for Logic (+5V)
3	VO	-	Power Supply for LCD
4	RS	H/L	Register Selection H: Display Data L: Instruction Code
5	R/W	H/L	Read/Write Selection H: Read Operation L: Write Operation
6	E	H, H→L	Enable Signal. Read data when E is "H", write data at the falling edge of E.
7	DB0	H/L	In 8-bit mode, used as low order bi-directional data bus. In 4-bit mode, open these terminals.
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	In 8-bit mode, used as high order bi-directional data bus. In 4-bit mode, used as both high and low order data bus.
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	
15	LEDA	--	LED Power Supply (+5V)
16	LEDK	--	LED Power Supply (0v)

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Supply Voltage(Logic)	VDD-VSS	-0.3	7.0	V
Supply Voltage(LCD)	VDD-VO	-0.3	13.0	V
Input Voltage	VI	-0.3	VDD+0.3	V
Operating Temp.	Topr	-20	70	℃
Storage Temp.	Tstg	-30	80	℃

2.4 Terminal Functions

Pin No.	Symbol	I/O	Function
1	VSS	-	Ground
2	VCC	-	Power Supply for Logic (+5V)
3	VE	-	Power Supply for LCD
4	RS	H/L	Register Selection H: Display Data RAM Selection L: Instruction Code
5	R/W	H/L	Read/Write Selection H: Read (Module → MPU) L: Write (MPU → Module)
6	E	H, H→L	Enable Signal. Data Read Mode when E is "H" and Data is in the falling edge of E.
7	DB0	H/L	In 8-bit mode: used as low order bidirectional data bus
8	DB1	H/L	
9	DB2	H/L	In 4-bit mode: open (from module)
10	DB3	H/L	
11	DB4	H/L	In 8-bit mode: used as high order bidirectional data bus.
12	DB5	H/L	
13	DB6	H/L	In 4-bit mode: used as both high and low order data.
14	DB7	H/L	
15	LED Power Supply (+5V)		
16	LED Power Supply (0V)	-	

3. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Supply Voltage(Logic)	VCC-VSS	-0.3	7.0	V
Supply Voltage(LCD)	VE-VSS	-0.3	13.0	V
Input Voltage	Vi	-0.3	VCC+0.3	V
Operating Temp.	Topr	-20	70	°C
Storage Temp.	Tstg	-30	80	

3. ELECTRICAL CHARACTERISTICS

3.1 DC Characteristics

(VDD=5.0V±10%, Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	UNIT
Supply Voltage (Logic)	VDD		4.5	5.0	5.5	V
Supply Voltage (LCD Drive)	VDD-VO		–	5.0	–	V
Input High Voltage	VIH		2.2	–	VDD	V
Input Low Voltage	VIL		-0.3	–	0.6	V
Output High Voltage	VOH	IOH=-0.2mA	2.4	–	VDD	V
Output Low Voltage	VOL	IOL=1.2mA	0	–	0.4	V
Supply Current (Logic)	IDD	VDD=5.0V	–	1.5	3.0	mA

3.2 Interface Timing Chart

(VDD=5.0V±10%, Ta=25℃)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode Refer to fig.1	E Cycle Time	tc	500	–	–	ns
	E Rise/Fall Time	tR, tF	–	–	20	
	E Pulse Width (High,Low)	tw	230	–	–	
	R/W and RS Setup Time	tSU1	40	–	–	
	R/W and RS Hold Time	tH1	10	–	–	
	Data Setup Time	tSU2	80	–	–	
	Data Hold Time	tH2	10	–	–	
Read Mode Refer to fig.2	E Cycle Time	tc	500	–	–	ns
	E Rise/Fall Time	tR, tF	–	–	20	
	E Pulse Width (High,Low)	tw	230	–		
	R/W and RS Setup Time	tSU	40	–		
	R/W and RS Hold Time	tH	10	–		
	Data Output Delay Time	tD	–	–	120	
	Data Hold Time	tDH	5	–	–	

3. ELECTRICAL CHARACTERISTICS

3.1 DC Characteristics

[VCC=+3.0V±10%, Ta=-20~70°C]

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (Logic)	VDD		4.5	5.0	5.5	V
Supply Voltage (VCC Driver)	VDD-VCC		-	5.0	-	V
Driver Supply Voltage	VCC		2.5	-	VDD	V
Input Low Voltage	VIL		-0.3	-	0.8	V
Input High Voltage	VIH	[illegible]	2.4	-	VDD	V
Output Low Voltage	VOL	[illegible]	0	-	0.4	V
Supply Current (Logic)	IDD	[illegible]	-	4.5	3.0	mA

3.2 Interface Timing Chart

[VCC=+3.0V±10%, Ta=20~70°C]

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Address Sig.)	E Cycle Time	tc	500	-	-	ns
	E Rise/Fall Time	tr, tf	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu	40	-	-	
	R/W and RS Hold Time	th	10	-	-	
	Data Setup Time	tsu	80	-	-	
	Data Hold Time	th	10	-	-	
Read Mode (Address Sig.)	E Cycle Time	tc	500	-	-	ns
	E Rise/Fall Time	tr, tf	-	-	20	
	E Pulse Width (High, Low)	tw	230	-		
	R/W and RS Setup Time	tsu	40	-		
	R/W and RS Hold Time	th	10	-		
	Data Output Delay Time	td	-	-	120	
	Data Hold Time	tdh	5	-	-	

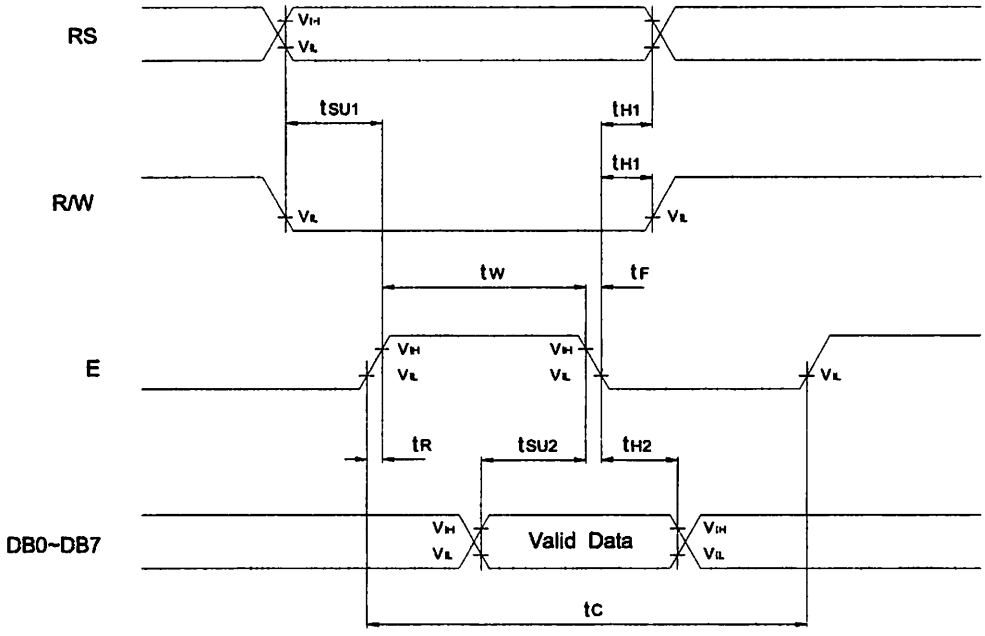


Fig.1 MPU Write Timing

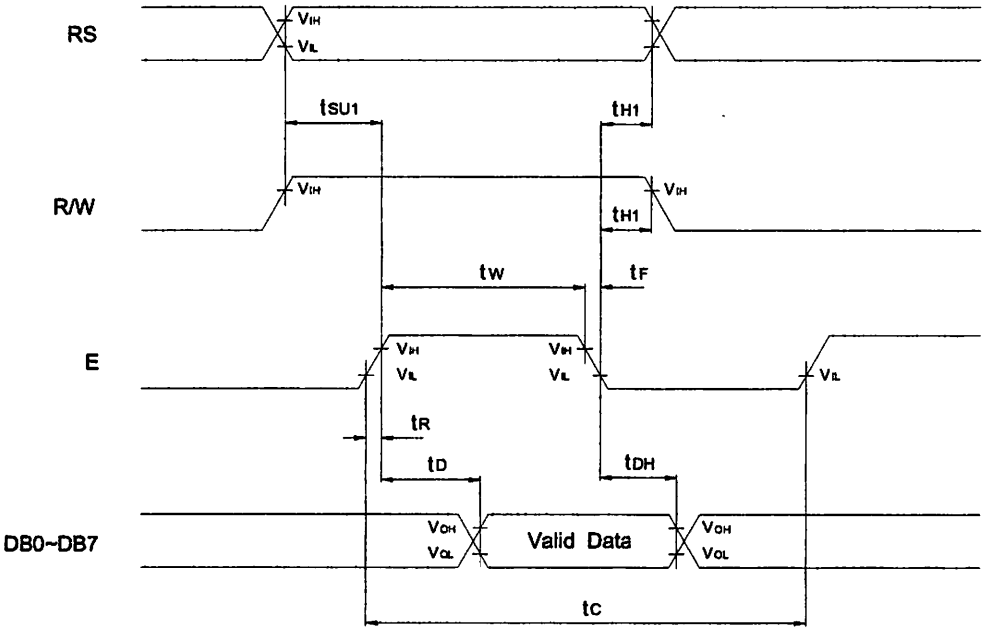
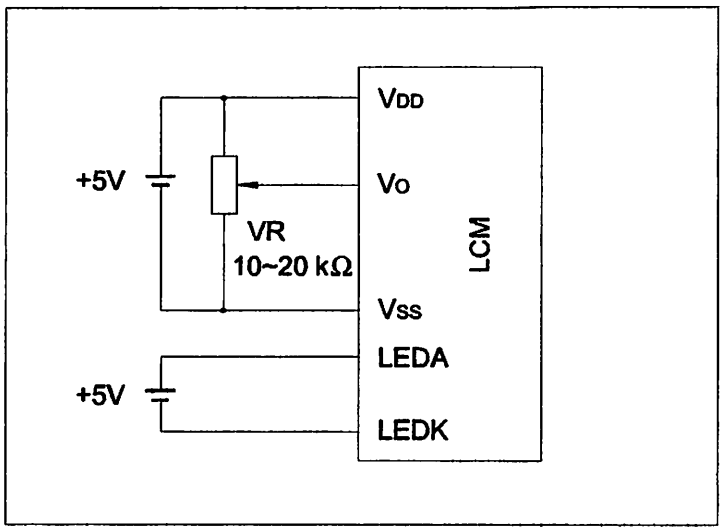


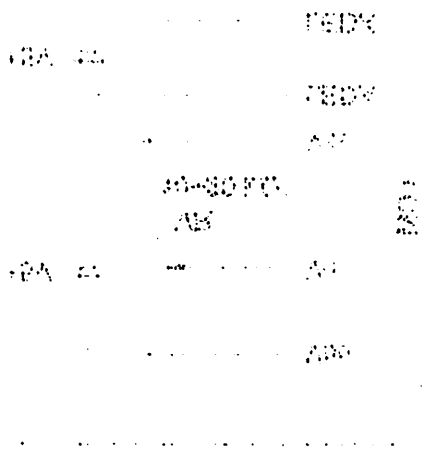
Fig.2 MPU Read Timing

3.3 LED Backlight Characteristics (Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	UNIT
Forward Voltage	Vf		3.9	4.1	4.3	V
Forward Current	If	Vf=4.1V	–	110	–	mA
Peak Wave Length	λ p	If=110mA	–	568	–	nm
Luminance	Lv	If=110mA	–	100	–	cd/m^2

3.4 Power Supply





3 V power supply

Frequency	TA	IL=210mV	—	100	—	MHz
Peak Value Factor	γ0	IL=210mV	—	282	—	mV
Crest Factor	K	Ap=0.1A	—	110	—	mV
Crest Factor	Ac		3.6	4.1	4.3	A
Item	Symbol	Condition	Min	Typ	Max	Unit

3 TEST Bridge Characteristics (1.5 V)

4. OPERATING PRINCIPLES & METHODES

4.1 Register

The LCD Controller has two 8-bit registers, the Instruction register (IR) and the data register (DR).

The IR is a write only register to store instruction codes like Display Clear or Cursor Shift as well as addresses for the Display Data RAM (DD RAM) or the Character Generator RAM (CG RAM).

The DR is a read/write register used for temporarily storing data to be read/written to/from the DD RAM or CG RAM. Data written into the DR is automatically written into DD RAM or CG RAM by an internal operation of the display controller.

The DR is also used to store data when reading out data from DD RAM or CG RAM.

When address information is written into IR, data is read out from DD RAM or CG RAM to DR by an internal operation. Data transfer is then completed by reading the DR.

After performing a read from the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read cycle. The register select (RS) signal determines which of these two registers is selected.

Table 4.1 Selection of Registers

RS	R/W	Function
0	0	Instruction Write operation (MPU writes instruction code to IR)
	1	Read Busy flag (DB7) and Address Counter (DB0 ~ DB6)
1	0	Data Write operation (MPU writes data to DR)
	1	Data Read operation (MPU reads data from DR)

4.2 Busy Flag (BF)

When the busy flag is high or "1" the module is performing an internal operation and the next instruction will not be accepted. The busy flag outputs to DB7 when RS = 0 and a read operation is performed. The next instruction must not be written until ensuring that the busy flag is low or "0".

4.3 Address Counter (AC)

The address counter (AC) assigns addresses to the DD RAM and the CG RAM.

When the address of an instruction is written into the IR, the address information is sent from the IR to the AC. The selection of either DD RAM or CG RAM is also determined concurrently by the same instruction. After writing into or reading from the DD RAM or CG RAM the address counter (AC) is automatically increased by 1 or decreased by 1 (determined by the I/D bit in the "Entry Mode Set" command). AC contents are output to DB0 ~ DB6 when RS = 0 and a read operation is performed.

4. OPERATING PROCEDURES & METHODES

4.1 Register

The LCD Controller has two 8-bit registers, the Instruction register (IR) and the data register (DR).

The IR is a write only register to store instruction codes such Display clear or Cursor Shift as well as addresses for the Display Data RAM (DD RAM) or the Character Generator RAM (CG RAM).

The DR is a read/write register used for temporarily storing data to be written into or read from the DD RAM or CG RAM. Data written into the DR is automatically written into DD RAM or CG RAM by an internal operation of the display controller.

The DR is also used to store data when reading out data from DD RAM or CG RAM.

When address information is written into IR, data is read out from DD RAM or CG RAM to DR by an internal operation. Data transfer is then completed by reading the DR.

After performing a read from the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read cycle. The register select (RS) signal determines which of these two registers is selected.

Table 4.1 Selection of Registers

RS	R/W	Function
0	0	Instruction Write operation (MPU writes instruction code to IR)
	1	Busy flag (DB7) and Address Counter (DB0 – DB6)
1	0	Data Write operation (MPU writes data to DR)
	1	Data Read operation (MPU reads data from DR)

4.2 Busy Flag (BF)

When the busy flag is high or "1" the module is performing an internal operation and the next instruction will not be accepted. The busy flag outputs to DB7 when RS = 0 and a read operation is performed. The next instruction must not be written until ensuring that the busy flag is low or "0".

4.3 Address Counter (AC)

The address counter (AC) assigns addresses to the DD RAM and to CG RAM.

When the address of an instruction is written into the IR, the address information is sent from the IR to the AC. The selection of either DD RAM or CG RAM is also determined consecutively by the same instruction. After writing into or reading from the DD RAM or CG RAM the address counter (AC) is automatically increased by 1 or decreased by 1 respectively by the LCD to the "Entry Mode Set" command. AC contents are output to DB0 – DB6 when RS = 0 and a read operation is performed.

4.4 Display Data RAM (DD RAM)

The Display Data RAM (DD RAM) stores the display data represented in 8-bit character codes. Its capacity is 80 x 8 bits or 80 characters. The Display Data RAM that is not used for the display can be used as a general data RAM.

The DD RAM address (ADD) is set in the Address Counter (AC) and is represented in hexadecimal. The address counter can be written by using the "Set DD RAM Address" instruction and can be read by using the "Read Busy Flag and Address" instruction. In each case, data bits DB0-DB6 represent the DD RAM address. In the read operation, bit DB7 represents the "Busy Flag".

MSB							LSB
BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Relations between DD RAM addresses and positions on the liquid crystal display are shown below.

		1	2	3	—	14	15	16	← Display Position
DD RAM Addr.	Line 1	00H	01H	02H	—	0DH	0EH	0FH	
	Line 2	40H	41H	42H	—	4DH	4EH	4FH	

When display shift operation is performed, the DD RAM address moves as follows:

For left shift:

		1	2	3	—	14	15	16	← Display Position
DD RAM Addr.	Line 1	01H	02H	03H	—	0EH	0FH	10H	
	Line 2	41H	42H	43H	—	4EH	4FH	50H	

For right shift:

		1	2	3	—	14	15	16	← Display Position
DD RAM Addr.	Line 1	27H	00H	01H	—	0CH	0DH	0EH	
	Line 2	67H	40H	41H	—	4CH	4DH	4EH	

4.6 Display Data RAM (DD RAM)

The Display Data RAM (DD RAM) stores the display data represented in 8-bit character codes. Its capacity is 80 × 8 bits or 80 characters. The Display Data RAM that is not used for the display can be used as a general data RAM.

The DD RAM address (ADD) is set in the Address Counter (AC) and is accessed in hexadecimal. The address counter can be written by using the "Set DD RAM Address" instruction and can be read by using the "Read Busy Flag and Address" instruction. In each case, data bits DB0-DB6 represent the DD RAM address. In the read operation, bit DB7 represents the "Busy Flag".

MSB							LSB
AC6	AC5	AC4	AC3	AC2	AC1	AC0	

Relations between DD RAM addresses and positions on the liquid crystal display are shown below.

DD RAM Addr.	1	2	3	...	14	15	16	Display Position
Line 1	00H	01H	02H	...	0DH	0EH	0FH	
Line 2	40H	41H	42H	...	4DH	4EH	4FH	

When display shift operation is performed, the DD RAM address moves as follows.

For left shift

DD RAM Addr.	1	2	3	...	14	15	16	Display Position
Line 1	01H	02H	03H	...	0EH	0FH	10H	
Line 2	41H	42H	43H	...	4EH	4FH	50H	

For right shift

DD RAM Addr.	1	2	3	...	14	15	16	Display Position
Line 1	27H	00H	01H	...	0CH	0DH	0EH	
Line 2	67H	40H	41H	...	4CH	4DH	4EH	

4.5 Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 7 dot or 5 x 10 dot character patterns from 8-bit character codes. It can generate up to 192 types of 5x7 dot character patterns and 32 types of 5x10 dot character patterns. Table 4.3 shows the relation between character codes and character patterns of the standard character font.

4.6 Character Generator RAM (CG RAM)

The CG RAM is a 64 x 8 bit RAM in which the user can program custom character patterns. With 5 x 7 dots, 8 types of character patterns can be written and with 5 x 10 dots 4 types of character patterns can be written. To write previously programmed characters from the CG RAM to the DD RAM, character codes 00H through 07H are used. (See character font Table 4.3). Unused CG RAM locations can be used for general purpose RAM.

The relationship between CG RAM address and data and the displayed character is shown in Tables 4.2

To program a 5 x 7 character pattern into the CG RAM location (for example, character code 01H), the following steps should be taken.

A. Use the "Set CG RAM address" command to position the CG RAM pointer to the 1st row of character code 01H (CG RAM address=48H).

B. Use the "Write Data to CG or DD RAM" Command to write the top row of the custom character (Only lower 5-bit of character pattern data is valid).

C. The CG RAM address is automatically increased if the I/D bit is set in the "Entry Mode Set" command. When this is the case, return to step B until all rows of the character are written.

D. After writing all 7 rows of data, use the "Set DD RAM address" command to return the address counter to a DD RAM location.

E. To display the custom character written above, use the "Write Data to CG or DD RAM" command with the data being 01H to display the character in the DD RAM address.

4.4 Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 7 dot or 5 x 10 dot character patterns from 8-bit character codes. It can generate up to 192 types of 5x7 dot character patterns and 32 types of 5x10 character patterns. Table 4.3 shows the relationship between character codes and character patterns of the standard character ROM.

4.5 Character Generator RAM (CG RAM)

The CG RAM is a 64 x 8 bit RAM in which the user can program custom character patterns. With 8 x 7 dots, 8 types of character patterns can be written and with 5 x 10 dots, 4 types of character patterns can be written. To write previously programmed character patterns from the CG RAM to the DD RAM, character codes 0H through 07H are used. The character patterns (Table 4.3) stored in CG RAM locations can be used for general purpose RAM.

The relationship between CG RAM addresses and data and the displayed character is shown in Table 4.4.

To program a 5 x 7 character pattern into the CG RAM between (for example) characters code 11H, the following steps should be taken.

A. Use the "Set CG RAM address" command to position the CG RAM pointer to the start of character code 0 and CG RAM address=08H.

B. Use the "Write Data to CG or DD RAM" command to write the top row of the 5 column character (only lower 5-bit of character pattern data is valid).

C. The CG RAM address is automatically increased if the CG bit is set in the "Entry Mode Set" command. When this is the case, return to step B until all rows of the character pattern are written.

D. After writing all 7 rows of data, in the "Set DD RAM address" command to return the address counter to a DD RAM location.

E. To display the custom character written above, use the "Write Data to DD or CG RAM" command with the data being 00H or display the character in the DD RAM address.

Table 4.2 Relation between CG RAM address, character codes (DD RAM) and character patterns (5x7 dots)

Character Code (DDRAM data)								CGRAM Address						CGRAM Data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	×	0	0	0	0	0	0	0	0	0	×	×	×	0				0	
																		0	0	0		
																		0	0	0		pattern 1
																		0	0	0		
																		0	0	0		
																		0	0	0		cursor
																	0	0	0	0	0	position
0	0	0	0	×	1	1	1	0	0	0	0	0	0	×	×	×		0	0	0		
											0	0	1					0	0	0		
											0	1	0					0	0	0		pattern 8
											0	1	1									
											1	0	0					0	0	0		
											1	0	1					0	0	0		
											1	1	0					0	0	0		cursor
											1	1	1				0	0	0	0	0	position

Notes:

1. Character code bits 0~2 correspond to CG RAM address bit 3~5 (3 bits: 8 types).
2. CG RAM address bits 0~2 designate the line position within a character pattern. The 8th line is the cursor position and display is determined by the logical OR of the 8th line and the cursor. Maintain the 8th line data, corresponding to the cursor display position, in the "0" state for cursor display. When the 8th line data is "1", bit 1 lights up regardless of cursor existence.
3. Character pattern row positions correspond to CG RAM data bits 0~4 as shown in the above (bit 4 being at the left end). Since CG RAM data bits 5~7 are not used for display, they can be used for the general data RAM as memory elements still exit.
4. As shown in Table 4.2, CG RAM character patterns are selected when character code bits 4~7 are all "0". However as character code bit 3 is an ineffective bit, the "A" in the character pattern example is selected by character code "00H" or "08H".
5. "1" for CG RAM data corresponds to selected pixels and "0" for non-selected.

Table 4.2 Relation between CG RAM address, character codes (DD RAM) and character patterns (5x7 dots)

Character Code (DDRAM data)								CGRAM Address								CGRAM Data								Character Pattern
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	A7	A6	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	pattern 1
																0	0	0	0	0	0	0	0	
																0	0	0	0	0	0	0	0	
																0	0	0	0	0	0	0	0	
																0	0	0	0	0	0	0	0	
																0	0	0	0	0	0	0	0	
																0	0	0	0	0	0	0	0	
																0	0	0	0	0	0	0	0	
																0	0	0	0	0	0	0	0	
0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	pattern 8
																0	0	0	0	0	0	0	0	
																0	0	0	0	0	0	0	0	
																0	0	0	0	0	0	0	0	
																0	0	0	0	0	0	0	0	
																0	0	0	0	0	0	0	0	
																0	0	0	0	0	0	0	0	
																0	0	0	0	0	0	0	0	

Notes:

1. Character code bits 0-2 correspond to CG RAM address for 3-bit to pick 8 areas.
2. CG RAM address bits 0-2 designate the line position within a character pattern. The 5th line is the cursor position and display is determined by the logical OR of the 5th line and the cursor. Maintain the 5th line data corresponding to the cursor display position in the "0" state for cursor display. When the 5th line data is "1", bit 1 lights up regardless of cursor existence.
3. Character pattern row positions correspond to CG RAM data bits 4-0 as shown in the above (bit 4 being at the left end). Since CG RAM data bits 5-7 are not used for display they can be used for the general data RAM as memory elements still well.
4. As shown in Table 4.3, CG RAM character patterns are selected when character code bits 4-7 are all "0". However as character code bit 3 is not affected by the "A" in the character pattern example is selected by character code "0AH" or "0BH".
5. "1" for CG RAM data corresponds to selected pixel and "0" for non-selected.

Table 4.3 CGROM Character Code Table

Upper 4bit / Lower 4bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	(2)															
0010	(3)															
0011	(4)															
0100	(5)															
0101	(6)															
0110	(7)															
0111	(8)															
1000	(1)															
1001	(2)															
1010	(3)															
1011	(4)															
1100	(5)															
1101	(6)															
1110	(7)															
1111	(8)															

5. MPU INTERFACE

5.1 General

(1). The LCD controller can be operated in either 4 or 8 bits mode. Instructions/Data are written to the display using the signal timing characteristics found in section 3.2.
When operating in 4-bit mode, data is transferred in two 4-bit operations using data bits DB4~DB7. DB0~DB3 are not used. When using 4-bit mode, data is transferred twice before the instruction cycle is complete. The higher order 4 bits (contents of DB4~DB7 when interface data is 8 bits long) is transferred first, then the lower order 4 bits (contents of DB0~DB3 when interface data is 8 bits long) is transferred. Check the busy flag after 4-bit data has been transferred twice (one instruction). A 4-bit two operation will then transfer the busy flag and address counter data.
(2). When operating in 8-bit mode, data is transferred using the full 8-bit bus DB0~DB7.

5.2 Initialization

5.2.1 Initialization by the Internal Reset Circuit

The display can be initialized using the internal reset circuit when the power is turned on. The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. The busy flag will go active 10ms after Vcc rises to 4.5V.

(1). Display Clear

(2). Function set:

DL = 1 : 8 bit interface operation
N = 0 : 1 - line display
F = 0 : 5 x 7 dot character font

(3). Display ON/OFF Control:

D = 0 : Display OFF
C = 0 : Cursor OFF
B = 0 : Blink OFF

(4). Entry Mode Set

I/D = 1 : +1 (Increment Mode)
S = 0 : No Display Shift operation

If the internal power supply reset timing cannot be met (0.1ms<trcc<10ms), the internal reset circuit will not operate normally and initialization will not be performed. In this case, the display must be initialized by software.

5.2.2 Software Initialization

Although software initialization is not mandatory, it is recommended that this procedure always be performed. When the internal power supply reset timing cannot be met, then the display must be initialized using one of the following procedures.

5. MPU INTERFACE

5.1 General

(1) The LCD controller can be operated in either 4 or 8 bits mode. Instruction codes are written to the display using the signal timing characteristics found in section 5.2.

When operating in 4-bit mode, data is transferred in two 4-bit operations using data bits DB4-DB7. DB0-DB3 are not used. When using 8-bit mode, data is transferred twice before the instruction cycle is completed. The higher order 4 bits (contents of DB4-DB7 when interface data is 8 bits long) is transferred first. Then the lower order 4 bits (contents of DB0-DB3 when interface data is 8 bits long) is transferred. Check the busy flag after 4-bit data has been transferred twice (one instruction). A 4-bit two operation will then transfer the busy flag and address counter data.

(2) When operating in 8-bit mode, data is transferred using the full 8-bit bus DB0-DB7.

5.2 Initialization

5.2.1 Initialization by the Internal Reset Circuit

The display can be initialized using the internal reset circuit when the power is turned on. The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. The busy flag will go active 10ms after Vcc rises to 4.5V.

(1) Display Clear

(2) Function set:

DL = 1 : 8 bit interface operation

N = 0 : 1 - line display

F = 0 : 5 x 7 dot character font

(3) Display ON/OFF Control:

D = 0 : Display OFF

C = 0 : Cursor OFF

B = 0 : Blink OFF

(4) Entry Mode Set:

ID = 1 : +1 (Increment Mode)

S = 0 : No Display Shift operation

If the internal power supply rises during 10ms not be met, the internal reset circuit will not operate normally and initialization will not be performed. In this case, the display must be initialized by software.

5.2.2 Software Initialization

Although software initialization is not mandatory, it is recommended that the procedure shown be performed. When the internal power supply reset timing cannot be met, then the display must be initialized using one of the following procedures.

(1). 8-Bit Initialization:

Power on

↓

Wait for more than 30ms after V_{DD} rises to 4.5V.

↓

Function Set									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	N	F	X	X

↓

Wait for more than 39 μ s

↓

Display ON/OFF Control									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

↓

Wait for more than 39 μ s

↓

Display Clear									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

↓

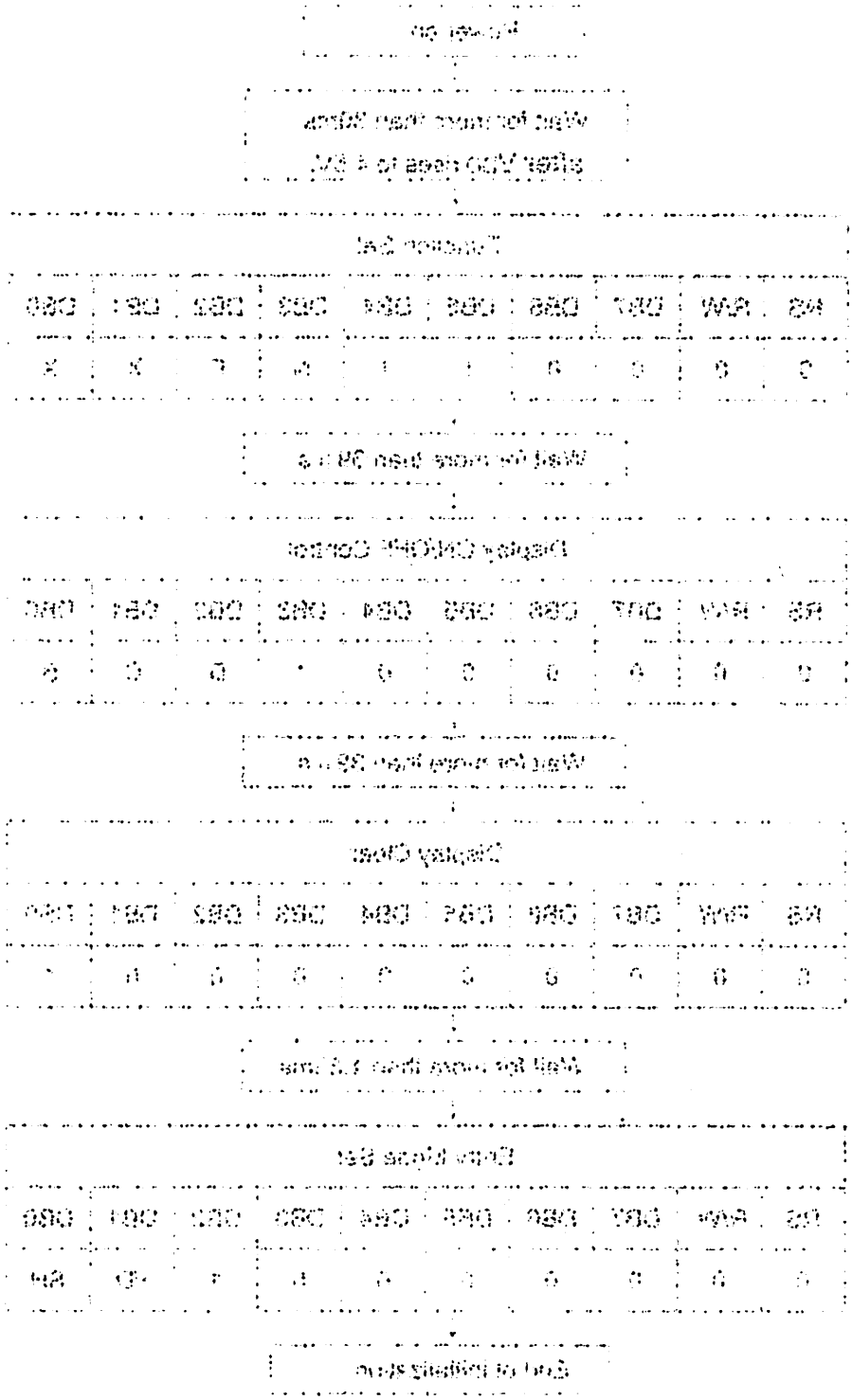
Wait for more than 1.53ms

↓

Entry Mode Set									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

↓

End of initialization


Turn on
Wait for more than 50ms
after VDD rises to 4.5V
Transfer Set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 1 0 0 1 X
Wait for more than 39 μs
Display ON/OFF Control
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 1 0 0 0
Wait for more than 39 μs
Display Clear
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 0 0 0 1
Wait for more than 1.5 ms
Entry Mode Set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 1 I/D S
Start of initialization

(2). 4-Bit Initialization:

Power on

↓

Wait for more than 30ms after V_{DD} rises to 4.5V.

↓

Function Set									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	X	X	X	X
0	0	0	0	1	0	X	X	X	X
0	0	N	F	X	X	X	X	X	X

↓

Wait for more than 39 μ s

↓

Display ON/OFF Control									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	1	D	C	B	X	X	X	X

↓

Wait for more than 39 μ s

↓

Display Clear									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	1	X	X	X	X

↓

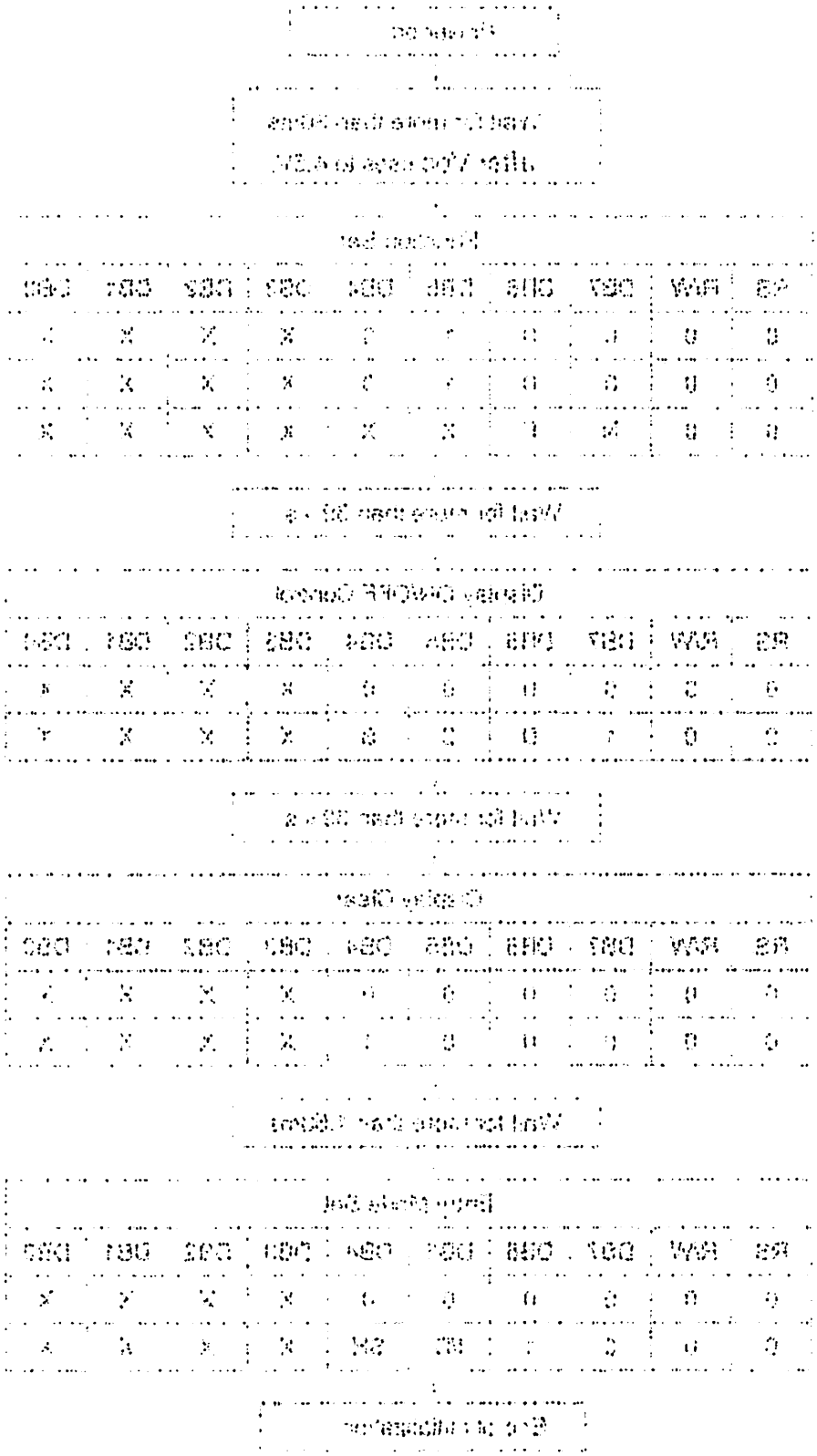
Wait for more than 1.53ms

↓

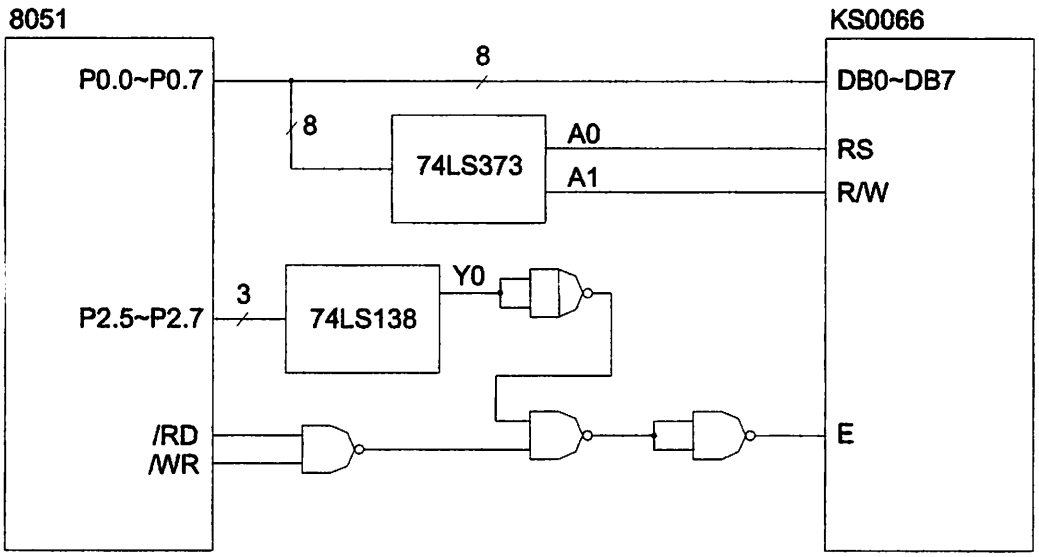
Entry Mode Set									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	1	I/D	SH	X	X	X	X

↓

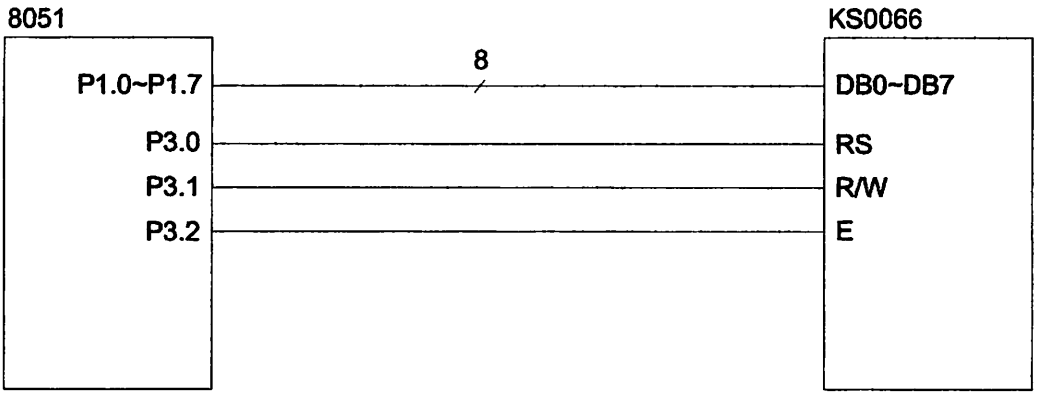
End of initialization



5.3 Connection with 8051 Family MPU



a. Application Circuit 1



b. Application Circuit 2

6. DISPLAY CONTROL INSTRUCTION

Table 6.1 Instructions

Instruction	Instruction code										Description	Execution time (fosc=270KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DDRAM address to 00H.	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	-	Sets DDRAM address to 00H in AC and returns shifted display to its original position. The contents of DDRAM remain unchanged.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Sets cursor move direction and enable the shift of entire display. These operations are performed during data write and read.	39μs
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set ON/OFF of entire display (D), cursor ON/OFF(C), and blinking of cursor position character(B).	39μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Moves cursor and shifts display without changing DDRAM contents.	39μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Sets interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line), and display font type (F: 5x11dots/5x8dots)	39μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address Counter.	39μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0μs
Write data to CG or DD RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43us
Read data from CG or DD RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43us

"-" : don't care

Note: 1. Make sure to check the busy flag before sending the instruction to the display. If the busy flag is not checked, the time between first and next instruction must be longer than the instruction execution time list in the Table 6.1.

2. After execution of CG RAM/DD RAM data write or read instruction, the RAM address counter is increased or decreased by 1. The RAM address counter is updated after the busy flag turns off.

3. DISPLAY CONTROL INSTRUCTION

Table 3.1 Instructions

Mnemonic	Instruction code												Description	Execution time (in 2MHz)
	M7	M6	M5	M4	D3	D2	D1	D0	D7	D6	D5	D4		
[illegible]	0	0	0	0	0	0	0	0	0	0	0	1	[illegible]	[illegible]
[illegible]	0	0	0	0	0	0	0	0	0	0	1	0	[illegible]	[illegible]
[illegible]	0	0	0	0	0	0	0	0	0	1	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	0	0	0	0	0	0	0	0	1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	0	0	0	0	0	0	0	1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	0	0	0	0	0	0	1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	0	0	0	0	0	1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	0	0	0	0	1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	0	0	0	1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	0	0	1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	0	1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Note: 1. Make sure to check the busy flag before sending the instruction to the display. If the busy flag is not checked, the time between that and next instruction must be longer than the instruction execution time listed in the Table 3.1.

2. After execution of CG RAM/DD RAM data write or read instruction, the RAM address counter is incremented or decreased by 1. The RAM address counter is updated after the busy flag turns off.

6.1 Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing the space code "20H" to all DD RAM addresses, and set DD RAM address to "00H" into address counter. Returns cursor to the original position, namely, brings the cursor to the upper left end of the display. The execution of clear display instruction sets entry mode to increment mode (I/D = 1).

6.2 Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Sets the DD RAM address "00H" in address counter. Return display to its original position if it was shifted. DD RAM contents do not change. The cursor or the blink moves to the upper left end of the display. Contents of DD RAM remain unchanged.

6.3 Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Sets the move direction of cursor and display.

I/D: Increases (I/D = 1) or decreases (ID = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM.
The cursor or blink moves to the right when increased by 1 and to the left when decreased by 1. The same applies to writing and reading the CG RAM.

S: Shifts the entire display when S = 1; shifts to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and only the display seems to move. The display does not shift when reading from DD RAM or writing/reading into/from CG RAM.
When S = 0, the display does not shift.

6.4 Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

8.1 Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing the space code "20H" to all DD RAM addresses, and set DD RAM address to "00H" into address counter. Returns cursor to the original position, namely, brings the cursor to the upper left end of the display. The execution of clear display instruction sets entry mode to increment mode (I/D = 1).

8.2 Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	*

Sets the DD RAM address "00H" in address counter. Returns display to its original position if it was shifted. DD RAM contents do not change. The cursor or the blink moves to the upper left end of the display. Contents of DD RAM remain unchanged.

8.3 Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Sets the move direction of cursor and display

I/D: Increase (I/D = 1) or decrease (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM.

The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading the CG RAM.

SH: Shifts the entire display when S = 1, shifts to the left when I/D = 0 and to the right when I/D = 1. Then it looks as if the cursor stands still and only the display seems to move. The display does not shift when reading from DD RAM or writing/reading information CG RAM.

When S = 0 the display does not shift.

8.4 Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Controls the display ON/OFF status, Cursor ON/OFF and Cursor Blink function.

D: The entire display is ON when D = 1 and OFF when D = 0. The display data remains in the DD RAM when display is OFF, it can be displayed immediately by setting D = 1.

C: The cursor displays when C = 1 and does not display when C = 0. The cursor is displayed on the 8th line when 5x7 dots character font has been selected.

B: The character indicated by the cursor blinks when B = 1. The blink is displayed by switching between all "High" data and display characters at 0.4 sec intervals.
The cursor and the blink can be set to display simultaneously.
When B = 0, the blink is off.

6.5 Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display.
Note that the display shift is performed simultaneously in all lines.
The contents of address counter do not change when display shift is performed.

Table 6.2 Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shifts cursor position to the left (AC is decreased by 1)
0	1	Shifts cursor position to the right (AC is increased by 1)
1	0	Shifts the entire display to the left, cursor follows the display shift.
1	1	Shifts the entire display to the right, cursor follows the display shift.

6.6 Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

Sets the interface data length, the number of lines, and character font.

DL: Sets interface data length. Data is sent or received in 8-bit length (DB7 ~ DB0) when DL = 1, and in 4-bit length (DB7 ~ DB4) when DL = 0. When the 4-bit length is selected, data must be sent or received twice.

N: Sets the number of lines

Controls the display ON/OFF status. Cursor ON/OFF and Cursor Blink function.

D: The entire display is ON when D = 1 and OFF when D = 0. The display data remains in the DD RAM when display is OFF. It can be displayed immediately by setting D = 1.

C: The cursor displays when C = 1 and does not display when C = 0. The cursor is displayed on the 8th line when 5x7 dots character font has been selected.

B: The character indicated by the cursor blinks when B = 1. The blink is produced by switching between all "High" data and display characters at 0.4 sec intervals. The cursor and the blink can be set to display simultaneously. When B = 0, the blink is off.

5.5 Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	S/C	R/L	*	*	*

Shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search or for the display.

Note that the display shift is performed simultaneously in all lines.

The contents of address counter do not change when display shift is performed.

Table 5.2 Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shifts cursor position to the left (AC is decreased by 1)
0	1	Shifts cursor position to the right (AC is increased by 1)
1	0	Shifts the entire display to the left. Cursor follows the display shift.
1	1	Shifts the entire display to the right. Cursor follows the display shift.

5.6 Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	*	*

Sets the interface data length, the number of lines, and character font.

DL: Sets interface data length. Data is sent or received in 8-bit length (DB7 – DB0) when DL = 1 and in 4-bit length (DB7 – DB4) when DL = 0. When the 4-bit length is selected, data must be sent or received twice.

N: Sets the number of lines

N = 0 : 1 line display (1/8 duty)
N = 1 : 2 line display (1/16 duty)
F: Sets character font.
F = 0 : 5 x 7 dots
F = 1 : 5 x 10 dots
Note: Perform the function at the head of the program before executing all instructions (except Busy flag/address read).

6.7 Set CG RAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Sets the CG RAM address to the address counter. Data is then written/read to/from the CG RAM.

6.8 Set DD RAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Sets the DD RAM address to the address counter. Data is then written/read to/from the DD RAM.
When in 1-line display mode (N = 0), DD RAM address is from "00H" to "4FH".
When in 2-line display mode (N = 1), DD RAM address corresponding to 1st line and 3rd line of the display is from "00H" to "27H"; the address corresponding to 2nd and 4th line of the display is from "40H" to "67H".

6.9 Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Reads the busy flag (BF) and value of the address counter (AC). BF = 1 indicates that internal operation is in progress and the next instruction will not be accepted until BF is set to "0". The BF status should be checked before each write operation. At the same time the value of the address counter is read out. The address counter is used by both CG and DD RAM and its value is determined by the previous instruction.

N = 0 : 1 line display (7-8 duty)
N = 1 : 2 line display (13-16 duty)
F: Dots character font
F = 0 : 5 x 7 dots
F = 1 : 5 x 10 dots
(Note: Function the function at the beginning of the program before executing all instructions (except Busy flag/address check).

3.7 Set CG RAM Address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG

Sets the CG RAM address in the address counter. Data is then written/read between the CG RAM.

3.8 Set DD RAM Address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD

Sets the DD RAM address in the address counter. Data is then written/read between the DD RAM.

When in 1-line display mode (N = 0), DD RAM address is from "00H" to "4FH".
When in 2-line display mode (N = 1), DD RAM address corresponding to 1st line and 2nd line of the display is from "00H" to "27H". The address corresponding to 2nd and 4th line of the display is from "40H" to "67H".

3.9 Read Busy Flag & Address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	ADD	ADD	ADD	ADD	ADD	ADD	ADD

Reads the busy flag (BF) and value in the address counter (ADD). If BF = 1 indicates that internal operation is in progress and an new instruction will not be accepted until BF is set to "0". The BF status should be checked before each write operation. At the same time the value of the address counter is read out. The address counter is used by both CG and DD RAM and its value is determined by the previous instruction.

6.10 Write Data to CG or DD RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

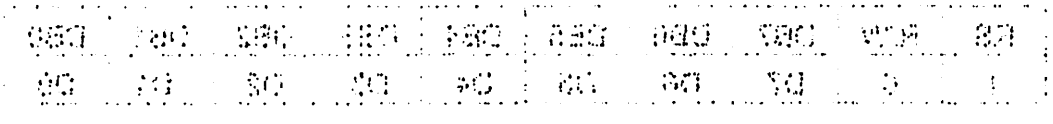
Writes binary 8-bit data to the CG or DD RAM.
The previous address set instruction (CG RAM address set or DD RAM address set) determines whether the CG or DD RAM is to be written. After a write the address is automatically increased or decreased by 1, according to the entry mode. The entry mode also determines display shift.

6.11 Read Data from CG or DD RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Reads binary 8-bit data from the CG RAM or DD RAM.
The previous address set instruction (CG RAM address set or DD RAM address set) determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. If RAM data is read several times without RAM address instruction set before read operation, the correct RAM data can be obtained from the second read. The "address set" instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading DD RAM). The cursor shift instruction operation is the same as that of the DD RAM address set instruction.
After a read the address is automatically increased or decreased by 1, according to the entry mode; however, display shift is not executed no matter what the entry mode is.
Note: The address counter (AC) is automatically increased or decreased by 1 after a "write" instruction to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if "read" instructions are executed.
The conditions for correct data read out are: (a) Execute either the address set instruction or cursor shift instruction (only with DD RAM) or (b) The execution of the "read data" instruction from the second time when the read instruction is performed multiple times in serial.

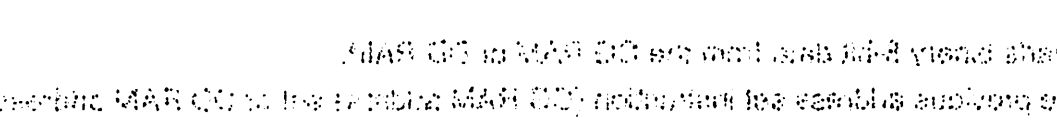
6.1.0 Write Data to CS or DD RAM



Writes binary 8-bit data to the CG or DD RAM

The previous address set instruction (CG RAM address set or DD RAM address set) determines whether the CG or DD RAM is to be written. After a write the address is automatically increased or decreased by 1 according to the entry mode. The entry mode also determines display shift.

6.1.1 Read Data from CG or DD RAM



Reads binary 8-bit data from the CG RAM or DD RAM.

The previous address set instruction (CG RAM address set or DD RAM address set) determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you do not, the first read data will be invalidated. If RAM data is read several times without RAM address instruction set before read operation, the correct RAM data can be obtained from the second read. The address set instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading DD RAM). The cursor shift instruction operation is the same as that of the DD RAM address set instruction.

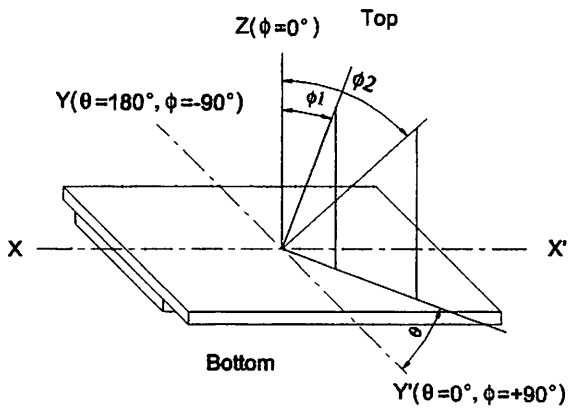
After a read the address is automatically increased or decreased by 1 according to the entry mode; however, display shift is not executed regardless of whether the entry mode is set. The address counter (AC) is automatically increased or decreased by 1 after a "write" instruction to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if "read" instructions are executed.

The conditions for correct data read out are: (a) Execute either the address set instruction or cursor shift instruction (only with DD RAM) or (b) The execution of the "read data" instruction from the second time after the read instruction is executed multiple times in serial.

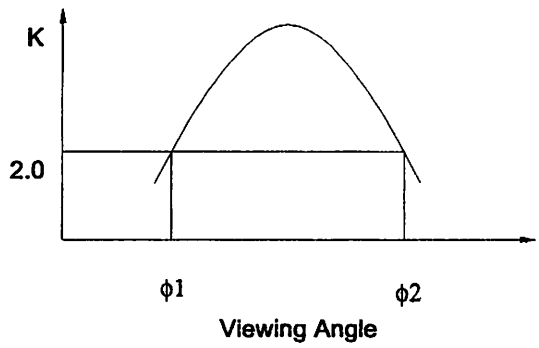
7. ELECTRO—OPTICAL CHARACTERISTICS (Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
View Angle	Φ2-Φ1	K≥2 , θ=0°	–	80	–	Deg	Note1, Note2
Contrast	K	Φ=0° ,θ=0°	3	–	–	–	Note3
Response Time	tr (rise)	Φ=0° ,θ=0°	–	250	–	ms	Note3
	tf (fall)	Φ=0° ,θ=0°	–	250	–	ms	

Note1: Definition of Viewing Angle θ ,Φ



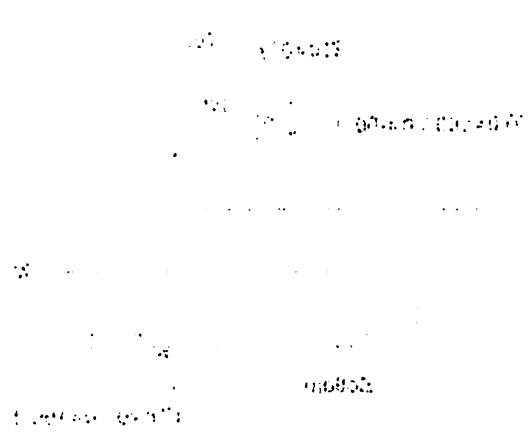
Note2: Definition of viewing Angle Range: Φ1,Φ2



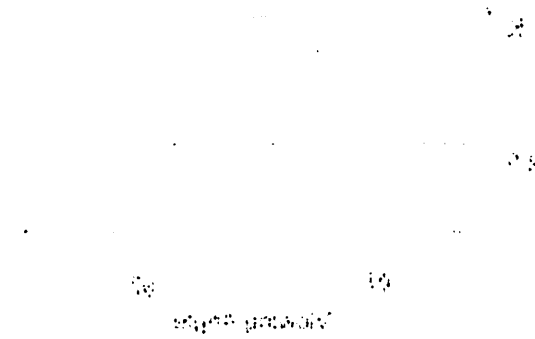
7. ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
View Angle	θ2, θ1	K=3, φ=0	–	60	–	Deg.	Normal Viewing
Contrast	K	θ=0°, φ=0°	3	–	–	–	Note(1)
Response Time	tr (rise)	θ=0°, φ=0°	–	250	–	ms	Note(2)
	tf (fall)	θ=0°, φ=0°	–	250	–	ms	

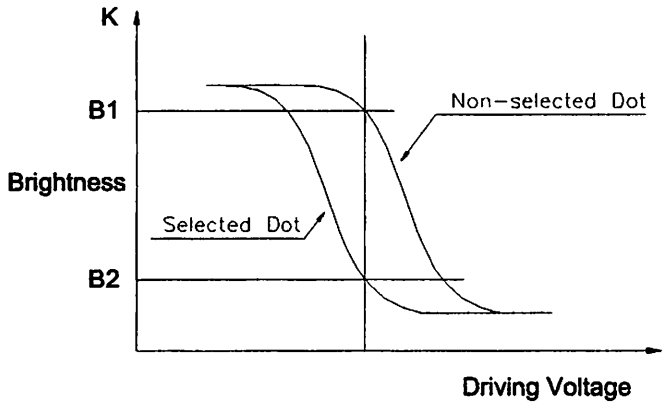
Note(1) Definition of Viewing Angle θ, φ



Note(2) Definition of viewing Angle Range

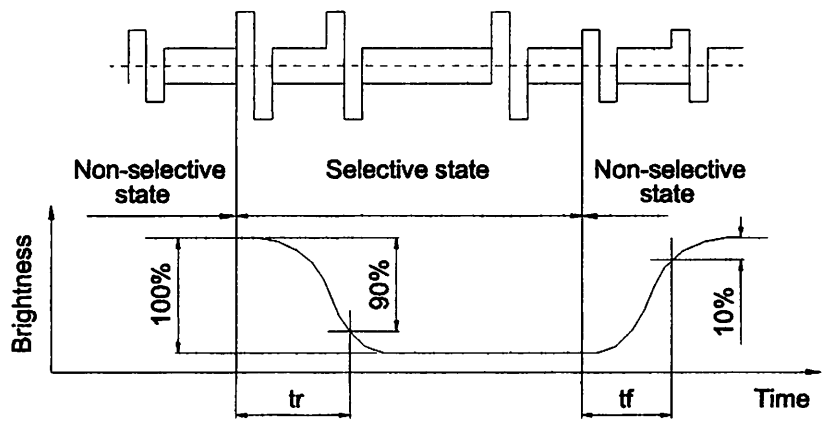


Note3: Definition of Contrast

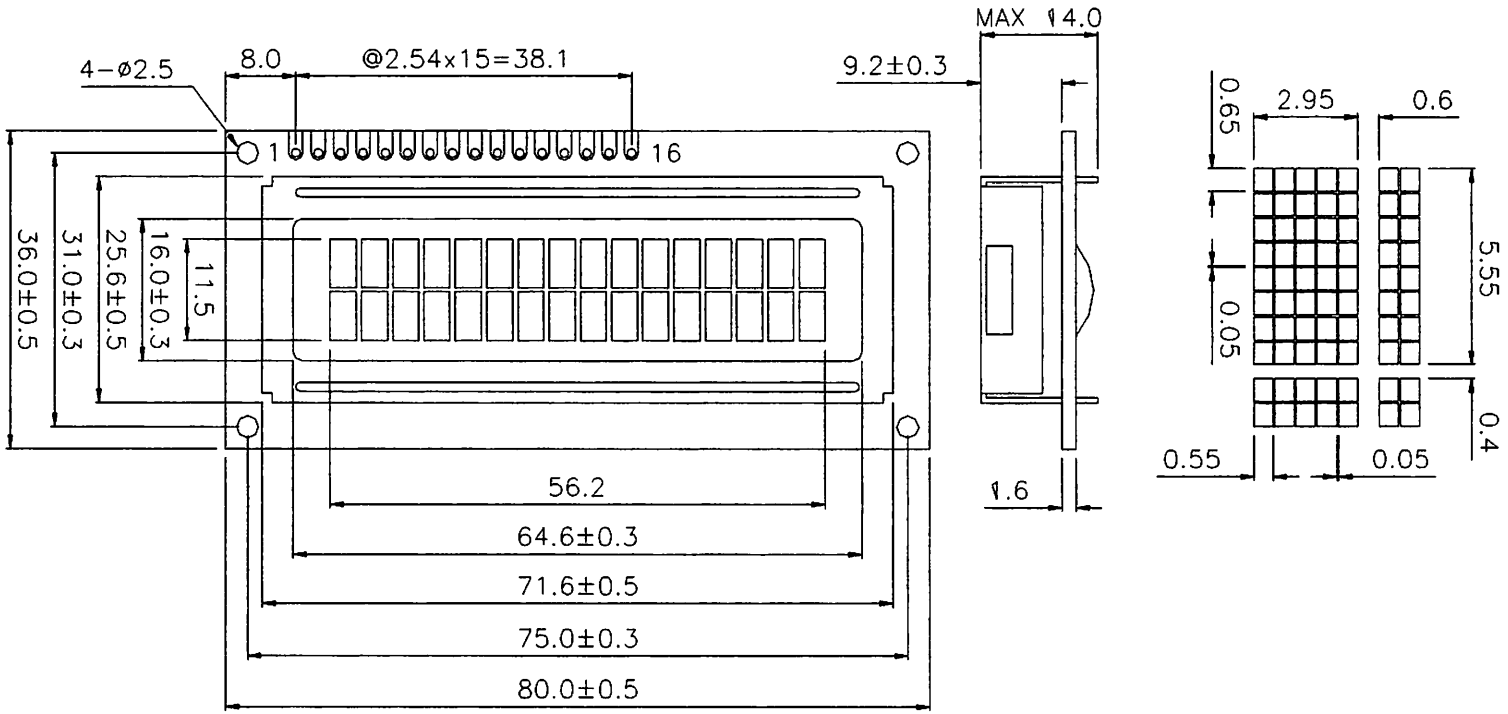


$$\text{Contrast} = \frac{\text{Brightness of non-selected dot (B1)}}{\text{Brightness of selected dot (B2)}}$$

Note4: Definition of Response Time



8. DIMENSIONAL OUTLINE



Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Symbol	VSS	VDD	Vo	RS	R/W	E	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	LEDA	LEDK

9. PRECAUTIONS FOR USE OF LCD MODULE

9.1 Handing Precautions

1) The display panel is made of glass. Do not subject it to a mechanical shock by Dropping it from a high place, etc.
2) If the display panel is damaged and the liquid crystal substance inside it leaks out, Be sure not to get any in your mouth. If the substance comes into contact with your Skin or clothes, promptly wash it off using soap and water.
3) Do not apply excessive force on the surface of display or the adjoining areas of LCD module since this may cause the color tone to vary.
4) The polarizer covering the display surface of the LCD module is soft and easily Scratched. Handle this polarizer carefully.
5) If the display surface of LCD module becomes contaminated, blow on the Surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten Cloth with one of the following solvents.
   - Isopropyl alcohol
   - Ethyl alcohol

   Solvents other than those mentioned above may damage the polarizer. Especially, do not use following.
   - Water
   - Ketone
   - Aromatic Solvents
6) When mounting the LCD module make sure that it is free of twisting, warping, and Distortion. Distortion has great influence upon display quality. Also keep the Stiffness enough regarding the outer case.
7) Be sure to avoid any solvent such as flux for soldering never stick to Heat-Seal. Such solvent on Heat-Seal may cause connection problem of heat-Seal and TAB.
8) Do not forcibly pull or bend the TAB I/O terminals.
9) Do not attempt to disassemble or process the LCD module.
10) NC terminal should be open. Do not connect anything.
11) If the logic circuit power is off, do not apply the input signals.
12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
    - Be sure to ground the body when handling the LCD module.
    - Tools required for assembly, such as soldering irons, must be properly grounded.
    - To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
    - The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

9.2 Storage Precautions

1) When storing the LCD module, avoid exposure to direct sunlight or to the light of Fluorescent lamps and high temperature/high humidity. Whenever possible, the

8. PRECAUTIONS FOR USE OF LCD MODULE

8.1 Handling Precautions

1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
2) If the display panel is damaged and the liquid crystal substance inside it leaks out, be careful not to get any in your mouth. If the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
3) Do not apply mechanical force on the surface of display or the adjoining areas of LCD module since this may cause the color tone to vary.
4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
5) If the display surface of LCD module becomes contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten a cloth with one of the following solvents.
   - Isopropyl alcohol
   - Ethyl alcohol

   Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following.
   - Water
   - Ketone
   - Aromatic Solvents
6) When mounting the LCD module make sure that it is free of twisting, warping, or distortion. Distortion has a great influence upon display quality. Also keep the stress enough regarding to a minimum.
7) Be sure to avoid any solvent such as flux for soldering never stick to front-glass. Such solvent on front-glass may cause corrosion problem of front-glass and TAB.
8) Do not touch, pull or bend the TAB I/O terminals.
9) Do not attempt to disassemble or remodel the LCD module.
10) LCD terminal should be open. Do not connect anything.
11) If the logic circuit power is off, do not apply the input signals.
12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
   - Be sure to ground the body when handling the LCD modules.
   - Tools required for assembly, such as soldering iron, must be properly grounded.
   - To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
   - The LCD module is packed with a film to protect the display surface. Peel this film slowly, paying off the protection film since static electricity may be generated.

8.2 Storage Precautions

1) When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps and high temperature/high humidity. It is better to keep the

LCD module should be stored in the same conditions in which they were shipped from Our company.

2) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets or a current flow in a high humidity environment.

9.3 Design Precautions

1) The absolute maximum ratings represents the rated value beyond which LCD module can not exceed. When the LCD modules are used in excess of this rated value, their operating characteristics may be adversely affected.
2) To prevent the occurrence of erroneous operation caused by noise, attention must be paid to satisfy VIL, VIH specification values, including taking the precaution of using signal cables that are short.
3) The liquid crystal display exhibits temperature dependency characteristics. Since recognition of the display becomes difficult when the LCD is used outside its designated operating temperature range, be sure to use the LCD within this range. Also, keep in mind that the LCD driving voltage levels necessary for clear displays will vary according to temperature.
4) Sufficiently notice the mutual noise interference occurred by peripheral devices.
5) To cope with EMI, take measures basically on outputting side.
6) If DC is impressed on the liquid crystal display panel, display definition is rapidly deteriorated by the electrochemical reaction that occurs inside the liquid crystal display panel. To eliminate the opportunity of DC impressing, be sure to maintain the AC characteristics of the input signals sent to the LCD Module.

9.4 Others

1) Liquid crystals solidify under low temperatures (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white).
   Air bubbles may also be generated if the LCD module is subjected to a strong shock at a low temperature.
2) If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.
3) To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity, etc., exercise care to avoid touching the following sections when handling the module:
   - Terminal electrode sections.
   - Part of pattern wiring on TAB, etc.

LCD modules should be stored in the same condition as which they were shipped from our company.

2) Electrical case is prohibited contact of the electronic circuit of the LCD module is accelerated by water droplets or a current flow in a high humidity environment.

9.3 Design Precautions

1) The absolute maximum ratings represents the most stress beyond which LCD modules can not exceed. When the LCD modules are used in excess of this upper value, their operating characteristics may be unfavorably affected.

2) To prevent the occurrence of electrolysis, apply zero volts between the data terminals and ground when the power is off. VDD discharge voltage should be kept to exactly 0V. Voltage should be kept to 1 sec or less when the power is off.

3) The liquid crystal display is a fragile component. Some precautions. Some malfunction of the display becomes difficult when the LCD is used outside the designated operating temperature range. Be sure to use the LCD within the range. Also, keep in mind that the LCD driving voltage levels necessary for clear display will vary according to temperature.

4) Continuously notice the minimum value intensity current by permanent current.

5) To cope with EMI, take measures mechanically on circuit board.

6) If LCD is impressed on the liquid crystal display panel, display deterioration is caused by the electrochemical reaction. Do not leave the liquid crystal display panel. To eliminate the occurrence of DC impressing, be sure to maintain an AC characterization of the input signals even in the LCD "off".

9.4 Others

1) Liquid crystals solidify under low temperatures (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white).
   Air bubbles may also be generated if the LCD module is exposed to a strong shock at a low temperature.

2) If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as a faint image and a slight contrast irregularity may also appear. A method of erasing stubborn patterns can be repeated by suspending use for some time. It should be noted that the occurrence does not adversely affect performance reliability.

3) To minimize the performance degradation of the LCD modules resulting from electrostatic discharge, avoid handling, such as touching the module unnecessarily.
   Handling precautions when handling the module:
   - Terminal electrode handling
   - Peel off protection sheet on TAB, etc.

19-0410; Rev 3; 7/96

MAXIM

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

General Description

The MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E are low-power transceivers for RS-485 and RS-422 communications in harsh environments. Each driver output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. These parts contain one driver and one receiver. The MAX483E, MAX487E, MAX488E, and MAX489E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, thus allowing error-free data transmission up to 250kbps. The driver slew rates of the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E are not limited, allowing them to transmit up to 2.5Mbps.

These transceivers draw as little as 120µA supply current when unloaded or when fully loaded with disabled drivers (see *Selection Table*). Additionally, the MAX481E, MAX483E, and MAX487E have a low-current shutdown mode in which they consume only 0.5µA. All parts operate from a single +5V supply.

Drivers are short-circuit current limited, and are protected against excessive power dissipation by thermal shutdown circuitry that places their outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX487E and MAX1487E feature quarter-unit-load receiver input impedance, allowing up to 128 transceivers on the bus. The MAX488E–MAX491E are designed for full-duplex communications, while the MAX481E, MAX483E, MAX485E, MAX487E, and MAX1487E are designed for half-duplex applications. For applications that are not ESD sensitive see the pin- and function-compatible MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487.

Applications

Low-Power RS-485 Transceivers
Low-Power RS-422 Transceivers
Level Translators
Transceivers for EMI-Sensitive Applications
Industrial-Control Local Area Networks

Features

- **ESD Protection: ±15kV—Human Body Model**
- **Slew-Rate Limited for Error-Free Data Transmission (MAX483E/487E/488E/489E)**
- **Low Quiescent Current:**
  120µA (MAX483E/487E/488E/489E)
  230µA (MAX1487E)
  300µA (MAX481E/485E/490E/491E)
- **-7V to +12V Common-Mode Input Voltage Range**
- **Three-State Outputs**
- **30ns Propagation Delays, 5ns Skew (MAX481E/485E/490E/491E/1487E)**
- **Full-Duplex and Half-Duplex Versions Available**
- **Allows up to 128 Transceivers on the Bus (MAX487E/MAX1487E)**
- **Current Limiting and Thermal Shutdown for Driver Overload Protection**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX481ECPA	0°C to +70°C	8 Plastic DIP
MAX481ECSA	0°C to +70°C	8 SO
MAX481EEPA	-40°C to +85°C	8 Plastic DIP
MAX481EESA	-40°C to +85°C	8 SO

Ordering Information continued on last page.

Selection Table

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	LOW-POWER SHUTDOWN	RECEIVER/ DRIVER ENABLE	QUIESCENT CURRENT (µA)	NUMBER OF TRANSMITTERS ON BUS	PIN COUNT
MAX481E	Half	2.5	No	Yes	Yes	300	32	8
MAX483E	Half	0.25	Yes	Yes	Yes	120	32	8
MAX485E	Half	2.5	No	No	Yes	300	32	8
MAX487E	Half	0.25	Yes	Yes	Yes	120	128	8
MAX488E	Full	0.25	Yes	No	No	120	32	8
MAX489E	Full	0.25	Yes	No	Yes	120	32	14
MAX490E	Full	2.5	No	No	No	300	32	8
MAX491E	Full	2.5	No	No	Yes	300	32	14
MAX1487E	Half	2.5	No	No	Yes	230	128	8

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±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 12V
Control Input Voltage ($\overline{RE}$, DE) ..... -0.5V to (V_{CC} + 0.5V)
Driver Input Voltage (DI) ..... -0.5V to (V_{CC} + 0.5V)
Driver Output Voltage (Y, Z; A, B) ..... -8V to +12.5V
Receiver Input Voltage (A, B) ..... -8V to +12.5V
Receiver Output Voltage (RO) ..... -0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) .. 800mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
Operating Temperature Ranges
MAX4_ _C_ _/MAX1487EC_ A ..... 0°C to +70°C
MAX4_ _E_ _/MAX1487EE_ A ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Driver Output (no load)	V_{OD1}					5	V
Differential Driver Output (with load)	V_{OD2}	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 8		1.5		5	
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 8				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R = 27Ω or 50Ω, Figure 8				3	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 8				0.2	V
Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		2.0			V
Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$				0.8	V
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	µA
Input Current (A, B)	I_{IN2}	DE = 0V; V_{CC} = 0V or 5.25V, all devices except MAX487E/MAX1487E	V_{IN} = 12V			1.0	mA
			V_{IN} = -7V			-0.8	
		MAX487E/MAX1487E, DE = 0V, V_{CC} = 0V or 5.25V	V_{IN} = 12V			0.25	mA
			V_{IN} = -7V			-0.2	
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			70		mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		3.5			V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV				0.4	V
Three-State (high impedance) Output Current at Receiver	I_{OZR}	0.4V ≤ V_O ≤ 2.4V				±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V, all devices except MAX487E/MAX1487E		12			kΩ
		-7V ≤ V_{CM} ≤ 12V, MAX487E/MAX1487E		48			kΩ

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
No-Load Supply Current (Note 3)	I_{CC}	MAX488E/MAX489E, DE, DI, $\overline{RE}$ = 0V or V_{CC}				120	250	µA
		MAX490E/MAX491E, DE, DI, $\overline{RE}$ = 0V or V_{CC}				300	500	
		MAX481E/MAX485E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			500	900	
			DE = 0V			300	500	
		MAX1487E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			300	500	
			DE = 0V			230	400	
		MAX483E/MAX487E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}	MAX483E		350	650	
				MAX487E		250	400	
			DE = 0V			120	250	
Supply Current in Shutdown	I_{SHDN}	MAX481E/483E/487E, DE = 0V, $\overline{RE}$ = V_{CC}				0.5	10	µA
Driver Short-Circuit Current, V_O = High	I_{OSD1}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Driver Short-Circuit Current, V_O = Low	I_{OSD2}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}			7		95	mA
ESD Protection		A, B, Y and Z pins, tested using Human Body Model				±15		kV

SWITCHING CHARACTERISTICS—MAX481E/MAX485E, MAX490E/MAX491E, MAX1487E

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		10	40	60	ns
	t_{PHL}			10	40	60	
Driver Output Skew to Output	t_{SKEW}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5	10	ns
Driver Rise or Fall Time	t_R, t_F	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481E, MAX485E, MAX1487E	3	20	40	ns
			MAX490EC/E, MAX491EC/E	5	20	25	
Driver Enable to Output High	t_{ZH}	Figures 11 and 13, C_L = 100pF, S2 closed			45	70	ns
Driver Enable to Output Low	t_{ZL}	Figures 11 and 13, C_L = 100pF, S1 closed			45	70	ns
Driver Disable Time from Low	t_{LZ}	Figures 11 and 13, C_L = 15pF, S1 closed			45	70	ns
Driver Disable Time from High	t_{HZ}	Figures 11 and 13, C_L = 15pF, S2 closed			45	70	ns
Receiver Input to Output	t_{PLH}, t_{PHL}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481E, MAX485E, MAX1487E	20	60	200	ns
			MAX490EC/E, MAX491EC/E	20	60	150	
| t_{PLH} - t_{PHL} | Differential Receiver Skew	t_{SKD}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5		ns
Receiver Enable to Output Low	t_{ZL}	Figures 9 and 15, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 9 and 15, C_{RL} = 15pF, S2 closed			20	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 9 and 15, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 9 and 15, C_{RL} = 15pF, S2 closed			20	50	ns
Maximum Data Rate	f_{MAX}			2.5			Mbps
Time to Shutdown	t_{SHDN}	MAX481E (Note 5)		50	200	600	ns

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

SWITCHING CHARACTERISTICS—MAX481E/MAX485E, MAX490E/MAX491E, MAX1487E (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Enable from Shutdown to Output High (MAX481E)	$t_{ZH(SHDN)}$	Figures 11 and 13, C_L = 100pF, S2 closed		45	100	ns
Driver Enable from Shutdown to Output Low (MAX481E)	$t_{ZL(SHDN)}$	Figures 11 and 13, C_L = 100pF, S1 closed		45	100	ns
Receiver Enable from Shutdown to Output High (MAX481E)	$t_{ZH(SHDN)}$	Figures 9 and 15, C_L = 15pF, S2 closed, A - B = 2V		225	1000	ns
Receiver Enable from Shutdown to Output Low (MAX481E)	$t_{ZL(SHDN)}$	Figures 9 and 15, C_L = 15pF, S1 closed, B - A = 2V		225	1000	ns

SWITCHING CHARACTERISTICS—MAX483E, MAX487E/MAX488E/MAX489E

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

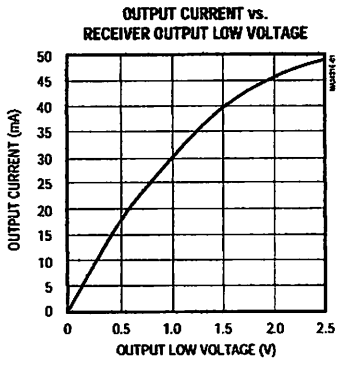
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250	800	2000	ns
	t_{PHL}		250	800	2000	
Driver Output Skew to Output	t_{SKEW}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		20	800	ns
Driver Rise or Fall Time	t_R, t_F	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
Driver Enable to Output High	t_{ZH}	Figures 11 and 13, C_L = 100pF, S2 closed	250		2000	ns
Driver Enable to Output Low	t_{ZL}	Figures 11 and 13, C_L = 100pF, S1 closed	250		2000	ns
Driver Disable Time from Low	t_{LZ}	Figures 11 and 13, C_L = 15pF, S1 closed	300		3000	ns
Driver Disable Time from High	t_{HZ}	Figures 11 and 13, C_L = 15pF, S2 closed	300		3000	ns
Receiver Input to Output	t_{PLH}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
	t_{PHL}		250		2000	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100		ns
Receiver Enable to Output Low	t_{ZL}	Figures 9 and 15, C_{RL} = 15pF, S1 closed		25	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 9 and 15, C_{RL} = 15pF, S2 closed		25	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 9 and 15, C_{RL} = 15pF, S1 closed		25	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 9 and 15, C_{RL} = 15pF, S2 closed		25	50	ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	250			kbps
Time to Shutdown	t_{SHDN}	MAX483E/MAX487E (Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483E/MAX487E, Figures 11 and 13, C_L = 100pF, S2 closed			2000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483E/MAX487E, Figures 11 and 13, C_L = 100pF, S1 closed			2000	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483E/MAX487E, Figures 9 and 15, C_L = 15pF, S2 closed			2500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483E/MAX487E, Figures 9 and 15, C_L = 15pF, S1 closed			2500	ns

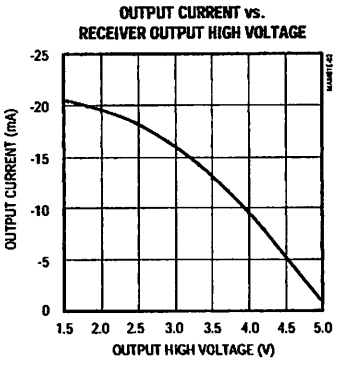
NOTES FOR ELECTRICAL/SWITCHING CHARACTERISTICS

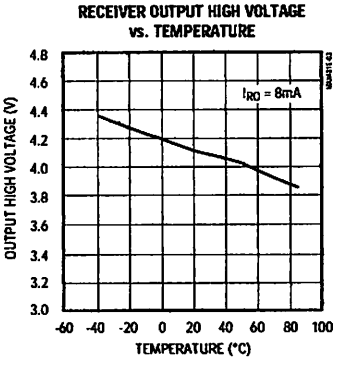
Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
Note 2: All typical specifications are given for V_{CC} = 5V and T_A = +25°C.
Note 3: Supply current specification is valid for loaded transmitters when DE = 0V.
Note 4: Applies to peak current. See *Typical Operating Characteristics*.
Note 5: The MAX481E/MAX483E/MAX487E are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

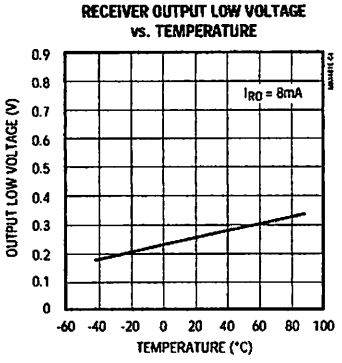
Typical Operating Characteristics

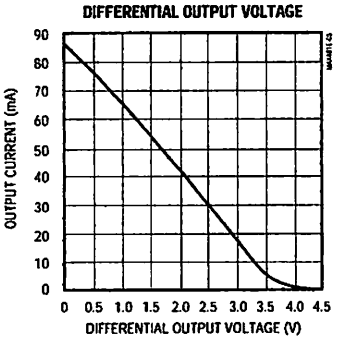
(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)









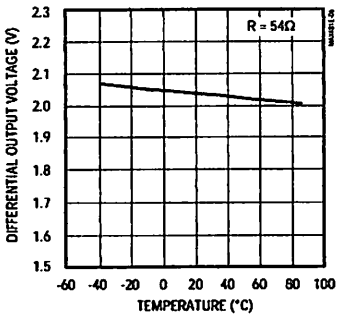


±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

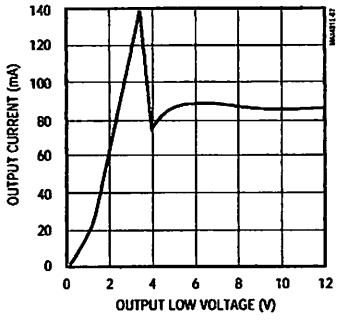
Typical Operating Characteristics (continued)

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

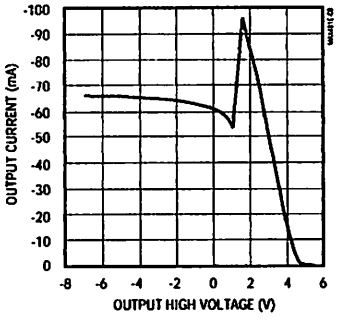
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



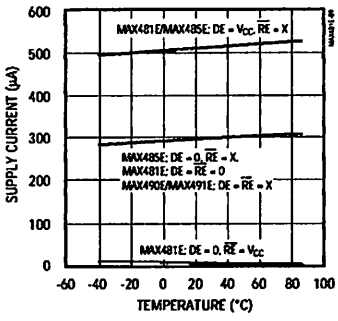
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



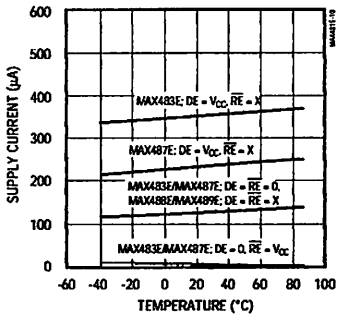
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



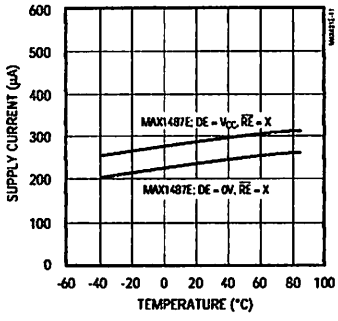
MAX481E/MAX485E/MAX490E/MAX491E SUPPLY CURRENT vs. TEMPERATURE



MAX483E/MAX487E–MAX489E SUPPLY CURRENT vs. TEMPERATURE



MAX1487E SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
MAX481E/MAX483E MAX485E/MAX487E MAX1487E	MAX488E MAX490E	MAX489E MAX491E		
1	2	2	RO	Receiver Output: If A > B by 200mV, RO will be high; If A < B by 200mV, RO will be low.
2	—	3	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	—	4	DE	Driver Output Enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	3	5	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	4	6, 7	GND	Ground
—	5	9	Y	Noninverting Driver Output
—	6	10	Z	Inverting Driver Output
6	—	—	A	Noninverting Receiver Input and Noninverting Driver Output
—	8	12	A	Noninverting Receiver Input
7	—	—	B	Inverting Receiver Input and Inverting Driver Output
—	7	11	B	Inverting Receiver Input
8	1	14	V_{CC}	Positive Supply: $4.75V \le V_{CC} \le 5.25V$
—	—	1, 8, 13	N.C.	No Connect—not internally connected

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

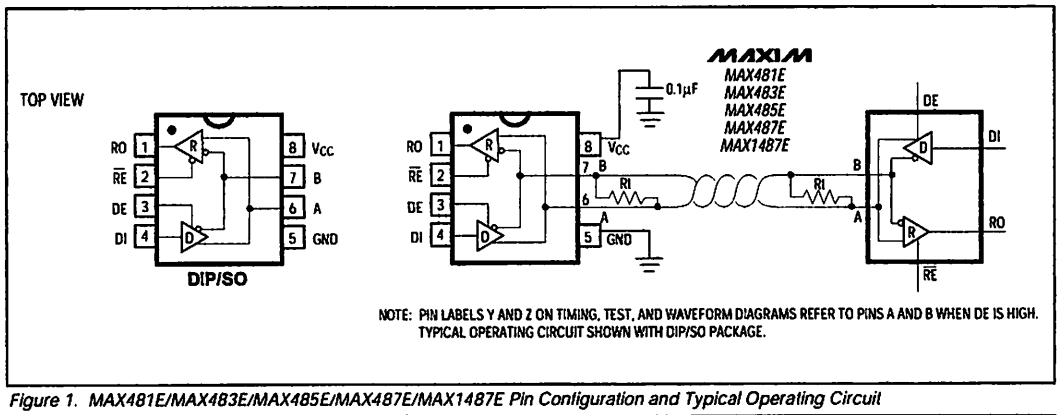


Figure 1. MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E Pin Configuration and Typical Operating Circuit

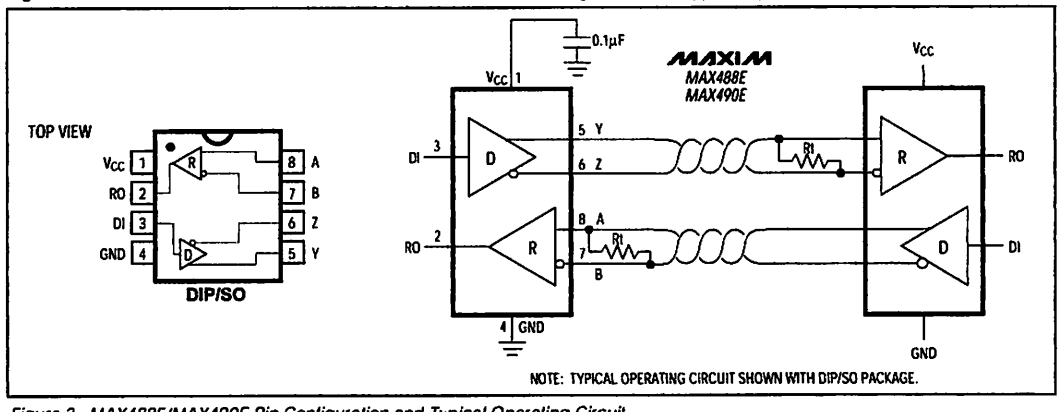


Figure 2. MAX488E/MAX490E Pin Configuration and Typical Operating Circuit

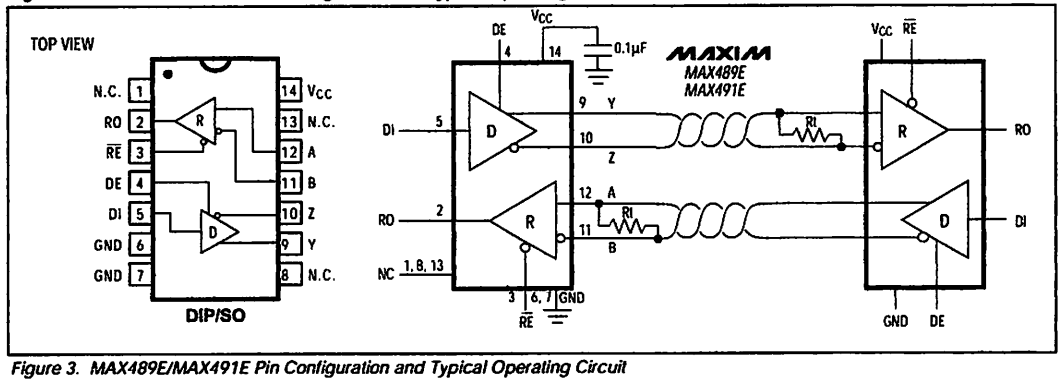


Figure 3. MAX489E/MAX491E Pin Configuration and Typical Operating Circuit

Function Tables (MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E)

Table 1. Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z*	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481E/MAX483E/MAX487E

Table 2. Receiving

INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ -0.2V	0
0	0	Inputs open	1
1	0	X	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481E/MAX483E/MAX487E

Applications Information

The MAX481E/MAX483E/MAX485E/MAX487E–MAX491E and MAX1487E are low-power transceivers for RS-485 and RS-422 communications. These "E" versions of the MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 provide extra protection against ESD. The rugged MAX481E, MAX483E, MAX485E, MAX497E–MAX491E, and MAX1487E are intended for harsh environments where high-speed communication is important. These devices eliminate the need for transient suppressor diodes and the associated high capacitance loading. The standard (non-"E") MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 are recommended for applications where cost is critical.

The MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E can transmit and receive at data rates up to 2.5Mbps, while the MAX483E, MAX487E, MAX488E, and MAX489E are specified for data rates up to 250kbps. The MAX488E–MAX491E are full-duplex transceivers, while the MAX481E, MAX483E, MAX487E, and MAX1487E are half-duplex. In addition, driver-enable (DE) and receiver-enable (RE) pins are included on the MAX481E, MAX483E, MAX485E, MAX487E, MAX489E, MAX491E, and MAX1487E. When disabled, the driver and receiver outputs are high impedance.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E keep working without latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to ±15kV using the Human Body Model.

Other ESD test methodologies include IEC10004-2 contact discharge and IEC1000-4-2 air-gap discharge (formerly IEC801-2).

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 4 shows the Human Body Model, and Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits (Figure 6).

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

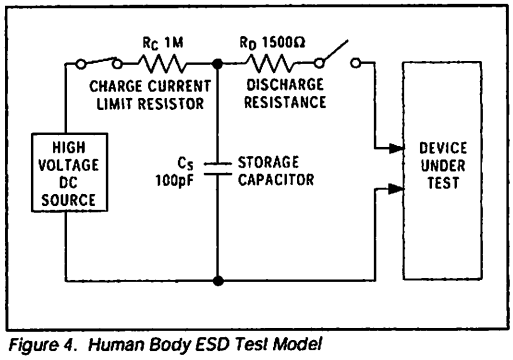


Figure 4. Human Body ESD Test Model

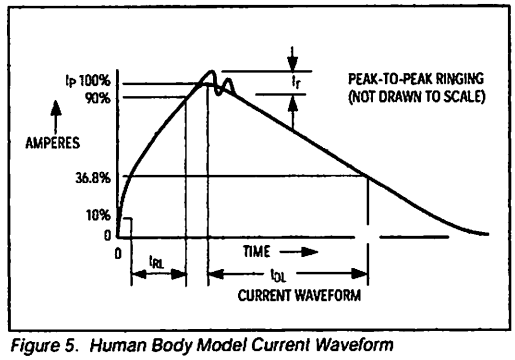


Figure 5. Human Body Model Current Waveform

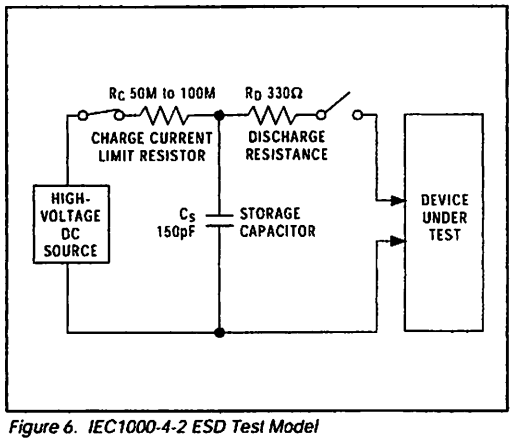


Figure 6. IEC1000-4-2 ESD Test Model

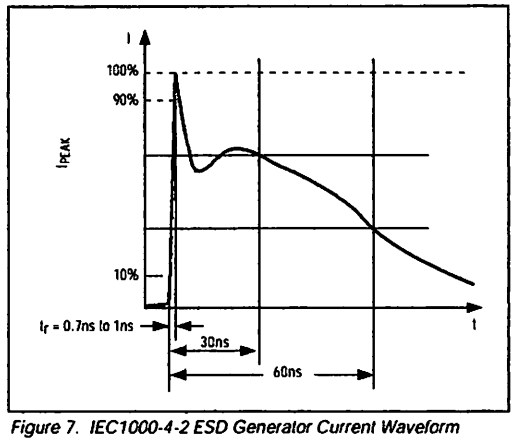


Figure 7. IEC1000-4-2 ESD Generator Current Waveform

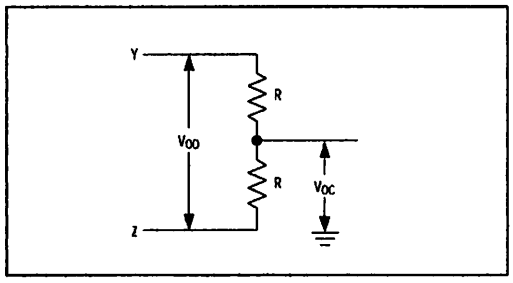


Figure 8. Driver DC Test Load

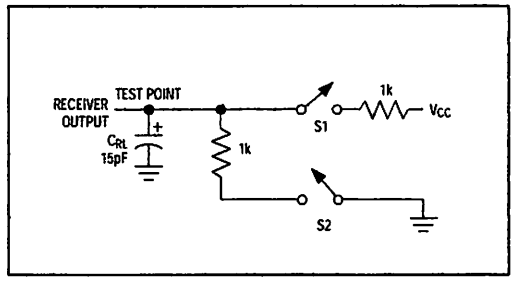


Figure 9. Receiver Timing Test Load

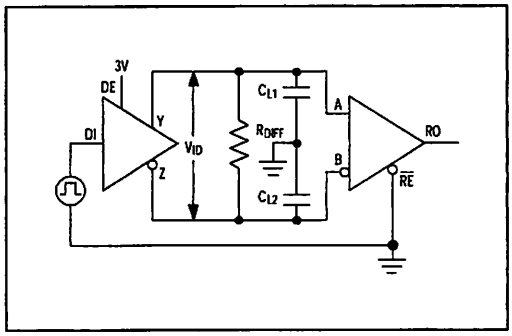


Figure 10. Driver/Receiver Timing Test Circuit

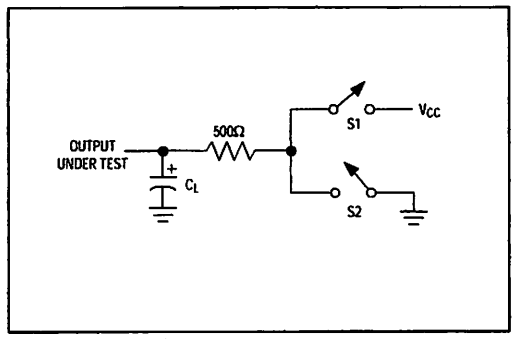


Figure 11. Driver Timing Test Load

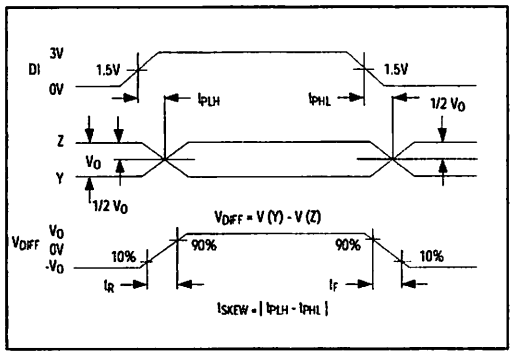


Figure 12. Driver Propagation Delays

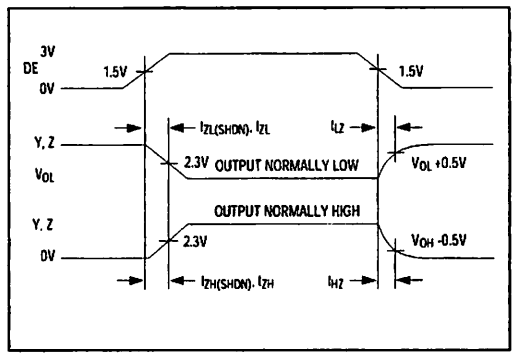


Figure 13. Driver Enable and Disable Times (except MAX488E and MAX490E)

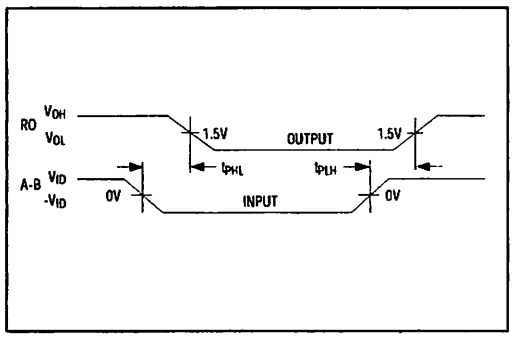


Figure 14. Receiver Propagation Delays

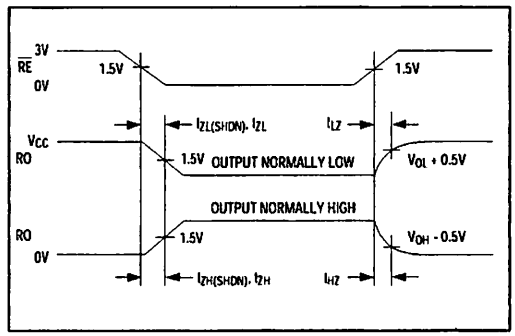


Figure 15. Receiver Enable and Disable Times (except MAX488E and MAX490E)

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

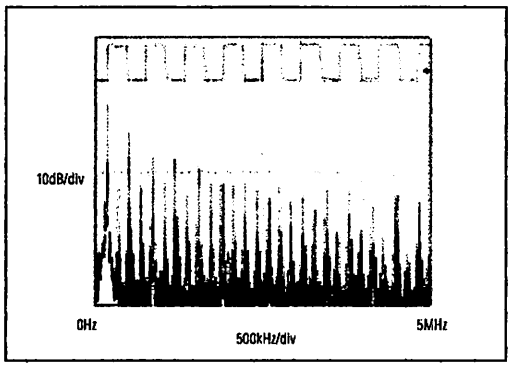


Figure 16. Driver Output Waveform and FFT Plot of MAX485E/MAX490E/MAX491E/MAX1487E Transmitting a 150kHz Signal

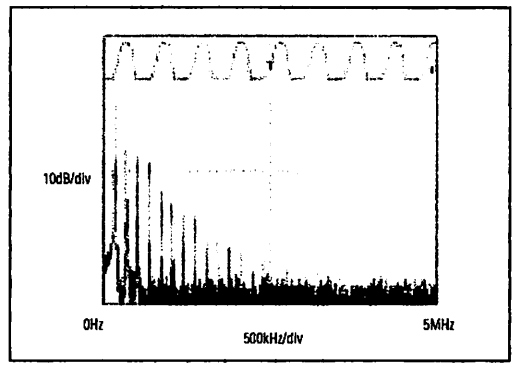


Figure 17. Driver Output Waveform and FFT Plot of MAX483E/MAX487E–MAX489E Transmitting a 150kHz Signal

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2, because series resistance is lower in the IEC1000-4-2 model. Hence, the ESD withstand voltage measured to IEC1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7 shows the current waveform for the 8kV IEC1000-4-2 ESD contact-discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing—not just inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

MAX487E/MAX1487E: 128 Transceivers on the Bus

The 48kΩ, 1/4-unit-load receiver input impedance of the MAX487E and MAX1487E allows up to 128 transceivers on a bus, compared to the 1-unit load (12kΩ input impedance) of standard RS-485 drivers (32 transceivers maximum). Any combination of MAX487E/MAX1487E and other RS-485 transceivers with a total of 32 unit loads or less can be put on the bus. The MAX481E, MAX483E, MAX485E, and MAX488E–MAX491E have standard 12kΩ receiver input impedance.

MAX483E/MAX487E/MAX488E/MAX489E: Reduced EMI and Reflections

The MAX483E and MAX487E–MAX489E are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 16 shows the driver output waveform and its Fourier analysis of a 150kHz signal transmitted by a MAX481E, MAX485E, MAX490E, MAX491E, or MAX1487E. High-frequency harmonics with large amplitudes are evident. Figure 17 shows the same information displayed for a MAX483E, MAX487E, MAX488E, or MAX489E transmitting under the same conditions. Figure 17's high-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

Low-Power Shutdown Mode (MAX481E/MAX483E/MAX487E)

A low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. The devices will not shut down unless both the driver and receiver are disabled. In shutdown, the devices typically draw only 0.5µA of supply current.

$\overline{RE}$ and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

For the MAX481E, MAX483E, and MAX487E, the t_{ZH} and t_{ZL} enable times assume the part was not in the low-power shutdown state (the MAX485E, MAX488E–MAX491E, and MAX1487E can not be shut down). The $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ enable times assume the parts were shut down (see *Electrical Characteristics*).

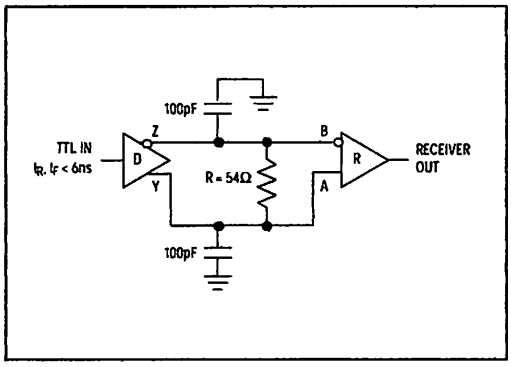


Figure 18. Receiver Propagation Delay Test Circuit

It takes the drivers and receivers longer to become enabled from the low-power shutdown state ($t_{ZH(SHDN)}$, $t_{ZL(SHDN)}$) than from the operating mode (t_{ZH}, t_{ZL}). (The parts are in operating mode if the $\overline{RE}$, DE inputs equal a logical 0,1 or 1,1 or 0, 0.)

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation delay times. Typical propagation delays are shown in Figures 19–22 using Figure 18's test circuit.

The difference in receiver delay times, t_{PLH} - t_{PHL}, is typically under 13ns for the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E, and is typically less than 100ns for the MAX483E and MAX487E–MAX489E.

The driver skew times are typically 5ns (10ns max) for the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E, and are typically 100ns (800ns max) for the MAX483E and MAX487E–MAX489E.

Typical Applications

The MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 25 and 26 show typical network application circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX483E and MAX487E–MAX489E are more tolerant of imperfect termination. Bypass the V_{CC} pin with 0.1µF.

Isolated RS-485

For isolated RS-485 applications, see the MAX253 and MAX1480 data sheets.

Line Length vs. Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. Figures 23 and 24 show the system differential voltage for the parts driving 4000 feet of 26AWG twisted-pair wire at 110kHz into 100Ω loads.

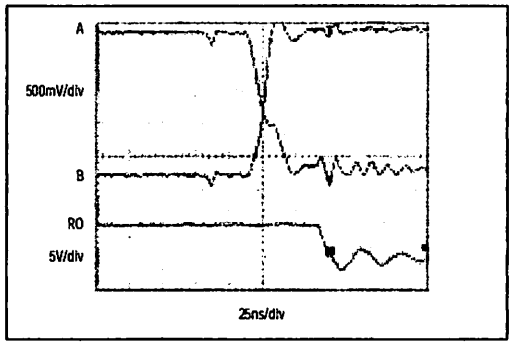


Figure 19. MAX481E/MAX485E/MAX490E/MAX1487E Receiver t_{PHL}

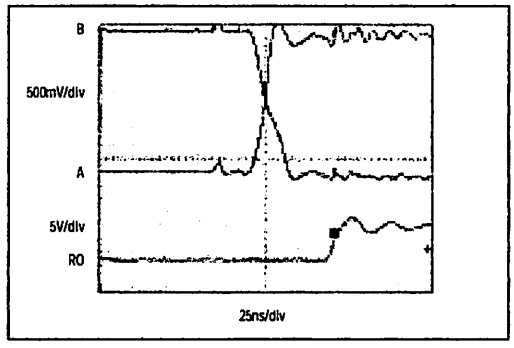


Figure 20. MAX481E/MAX485E/MAX490E/MAX491E/ MAX1487E Receiver t_{PLH}

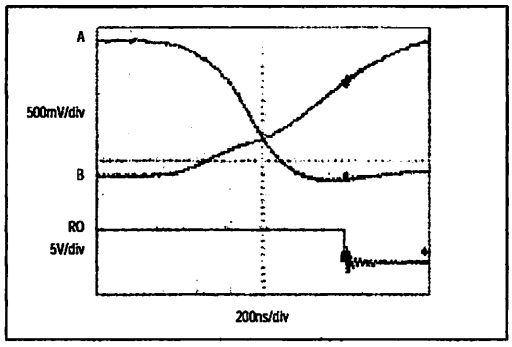


Figure 21. MAX483E/MAX487E–MAX489E Receiver t_{PHL}

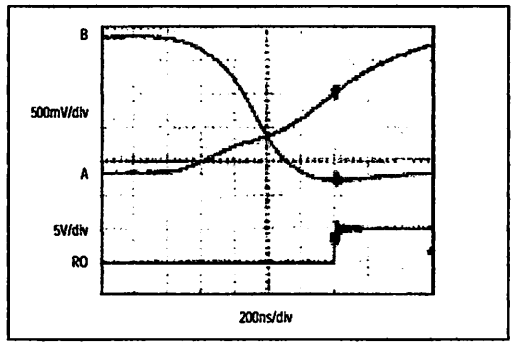


Figure 22. MAX483E/MAX487E–MAX489E Receiver t_{PLH}

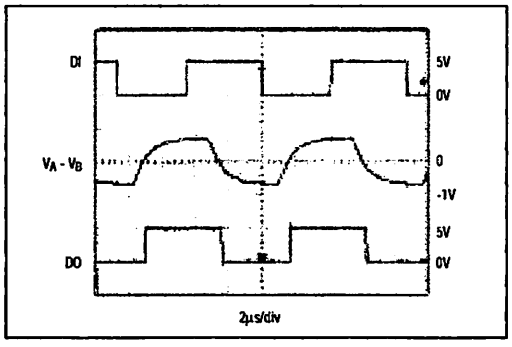


Figure 23. MAX481E/MAX485E/MAX490E/MAX491E/ MAX1487E System Differential Voltage at 110kHz Driving 4000ft of Cable

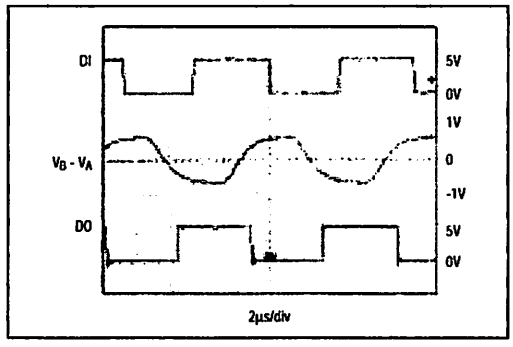


Figure 24. MAX483E/MAX1487E–MAX489E System Differential Voltage at 110kHz Driving 4000ft of Cable

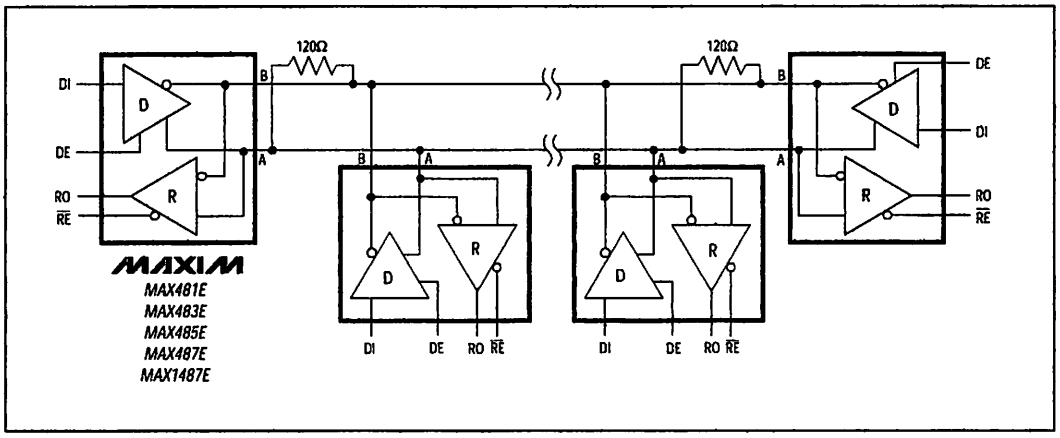


Figure 25. MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E Typical Half-Duplex RS-485 Network

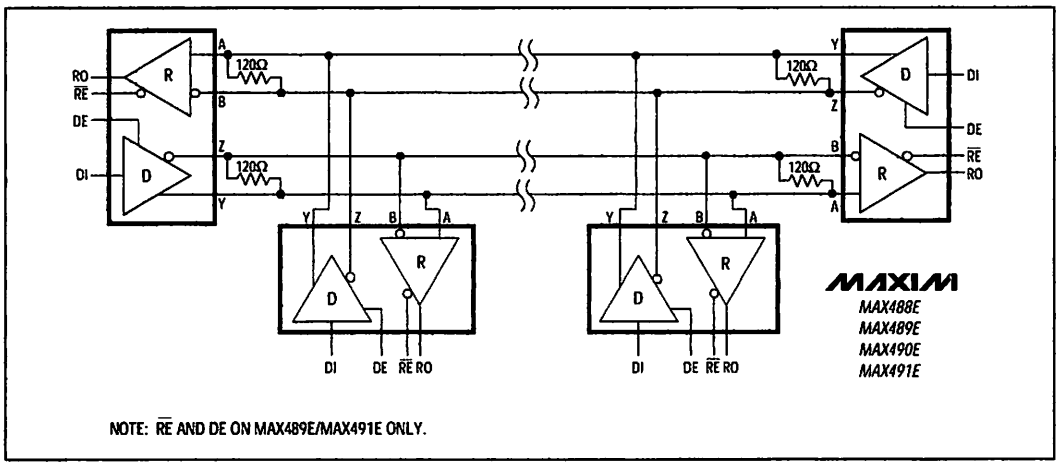


Figure 26. MAX488E–MAX491E Full-Duplex RS-485 Network

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX483ECPA	0°C to +70°C	8 Plastic DIP
MAX483ECSA	0°C to +70°C	8 SO
MAX483EEPA	-40°C to +85°C	8 Plastic DIP
MAX483EESA	-40°C to +85°C	8 SO
MAX485ECPA	0°C to +70°C	8 Plastic DIP
MAX485ECSA	0°C to +70°C	8 SO
MAX485EEPA	-40°C to +85°C	8 Plastic DIP
MAX485EESA	-40°C to +85°C	8 SO
MAX487ECPA	0°C to +70°C	8 Plastic DIP
MAX487ECSA	0°C to +70°C	8 SO
MAX487EEPA	-40°C to +85°C	8 Plastic DIP
MAX487EESA	-40°C to +85°C	8 SO
MAX488ECPA	0°C to +70°C	8 Plastic DIP
MAX488ECSA	0°C to +70°C	8 SO
MAX488EEPA	-40°C to +85°C	8 Plastic DIP
MAX488EESA	-40°C to +85°C	8 SO

PART	TEMP. RANGE	PIN-PACKAGE
MAX489ECPD	0°C to +70°C	14 Plastic DIP
MAX489ECSD	0°C to +70°C	14 SO
MAX489EEPD	-40°C to +85°C	14 Plastic DIP
MAX489EESD	-40°C to +85°C	14 SO
MAX490ECPA	0°C to +70°C	8 Plastic DIP
MAX490ECSA	0°C to +70°C	8 SO
MAX490EEPA	-40°C to +85°C	8 Plastic DIP
MAX490EESA	-40°C to +85°C	8 SO
MAX491ECPD	0°C to +70°C	14 Plastic DIP
MAX491ECSD	0°C to +70°C	14 SO
MAX491EEPD	-40°C to +85°C	14 Plastic DIP
MAX491EESD	-40°C to +85°C	14 SO
MAX1487ECPA	0°C to +70°C	8 Plastic DIP
MAX1487ECSA	0°C to +70°C	8 SO
MAX1487EEPA	-40°C to +85°C	8 Plastic DIP
MAX1487EESA	-40°C to +85°C	8 SO

Chip Information

TRANSISTOR COUNT: 295

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UTC LM78XX LINEAR INTEGRATED CIRCUIT

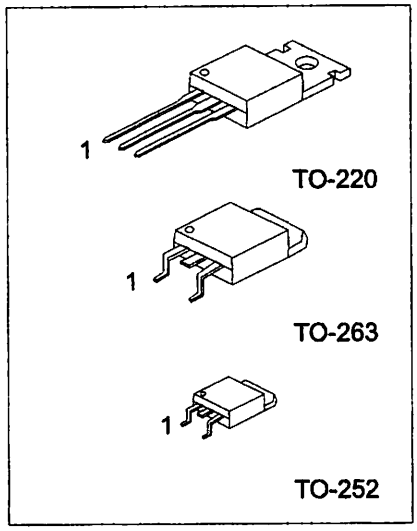
3-TERMINAL 1A POSITIVE VOLTAGE REGULATOR

DESCRIPTION

The UTC 78XX family is monolithic fixed voltage regulator integrated circuit. They are suitable for applications that required supply current up to 1 A.

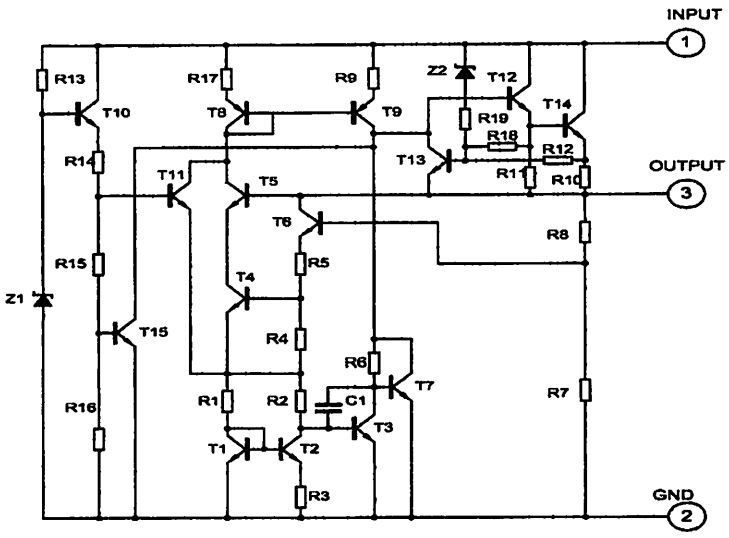
FEATURES

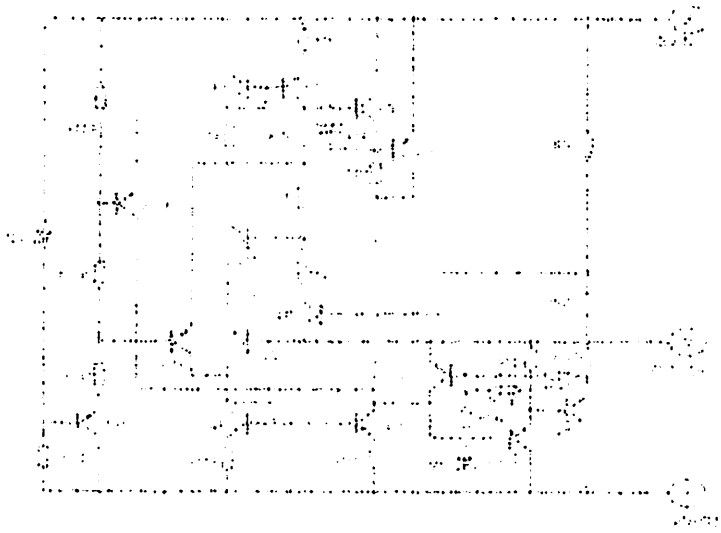
*Output current up to 1.5 A
*Fixed output voltage of 5V, 6V, 8V, 9V, 10V, 12V, 15V ,18V and 24V available
*Thermal overload shutdown protection
*Short circuit current limiting
*Output transistor SOA protection



1: Input 2: GND 3: Output

TEST CIRCUIT





FEATURES

- Adjustable output voltage
- Output current to 1.5A
- Internal thermal overload protection
- Internal short circuit current limit
- Output transistor safe area protection
- Output voltage range 1.25V to 37V
- Guaranteed 1% output voltage tolerance (LM317A)
- Guaranteed max. 0.01%/V line regulation (typ)
- Guaranteed max. 0.3% load regulation (typ)
- Guaranteed 80dB ripple rejection (typ)
- Guaranteed max. 100μA quiescent current
- Guaranteed max. 5mA quiescent current change over line and load

DESCRIPTION

The LM317 series are adjustable three terminal positive voltage regulators capable of supplying in excess of 1.5A over a 1.25V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they offer superior regulation over fixed voltage regulators, plus internal current limiting, thermal shutdown and safe area protection, making it virtually indestructible. If adequate heat sinking is provided, they can deliver over 1.5A current to a load. They are also more efficient than standard fixed voltage regulators.

ABSOLUTE MAXIMUM RATINGS

(Operating temperature range applies unless otherwise specified)

PARAMETER	SYMBOL	RATING		UNIT
Input voltage(for Vo=5~18V)			35	V
(for Vo=24V)	V_I		40	V
Output Current	I_o		1	A
Power Dissipation	PD	Internally	Limited	W
Operating Junction Temperature Range	T_{OPR}	-20	+150	°C
Storage Temperature Range	T_{STG}	-55	+150	°C

UTC LM7805 ELECTRICAL CHARACTERISTICS

(V_I=10V, Io=0.5A, Tj= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, Io=5mA - 1.0A	4.80	5.0	5.20	V
		V_I =7.5V to 20V, Io=5mA - 1.0A,PD<15W	4.75		5.25	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			50	mV
		Tj=25°C,Io=0.25A - 0.75A			25	mV
Line regulation	ΔVo	V_I =7V to 25V,Tj=25°C			50	mV
		V_I =7.5V to 20V,Tj=25°C,Io=1A			50	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	V_I =7.5V to 20V			1.0	mA
	ΔIq	Io=5mA - 1.0A			0.5	mA
Output Noise Voltage	V_N	10Hz<=f<=100kHz		40		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-0.6		mV/°C
Ripple Rejection	RR	V_I =8V - 18V,f=120Hz,Tj=25°C	62	80		dB
Peak Output Current	I_{PK}	Tj=25°C		1.8		A
Short-Circuit Current	Isc	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7806 ELECTRICAL CHARACTERISTICS

(V_I=11V, Io=0.5A, Tj= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, Io=5mA - 1.0A	5.76	6.0	6.24	V
		V_I =8.5V to 21V, Io=5mA - 1.0A, PD<15W	5.70		6.30	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			60	mV
		Tj=25°C,Io=0.25A - 0.75A			30	mV
Line regulation	ΔVo	V_I =8V to 25V,Tj=25°C			60	mV
		V_I =8.5V to 21V,Tj=25°C,Io=1A			60	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	V_I =8.5V to 21V			1.0	mA
	ΔIq	Io=5mA - 1.0A			0.5	mA
Output Noise Voltage	V_N	10Hz<=f<=100kHz		45		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-0.7		mV/°C
Ripple Rejection	RR	V_I =9V - 19V,f=120Hz,Tj=25°C	59	75		dB

UTC LM308X LINEAR INTEGRATED CIRCUIT

ABSOLUTE MAXIMUM RATINGS

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UTC LM308X ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LM308X			UNIT
			MIN	TYP	MAX	
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UTC LM308X ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LM308X			UNIT
			MIN	TYP	MAX	
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PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak Output Current	I_{PK}	Tj=25°C		1.8		A
Short-Circuit Current	Isc	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7808 ELECTRICAL CHARACTERISTICS

(VI=14V, Io=0.5A, Tj= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, Io=5mA - 1.0A	7.68	8.0	8.32	V
		V_I =10.5V to 23V, Io=5mA - 1.0A, PD<15W	7.60		8.40	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			80	mV
		Tj=25°C,Io=0.25A - 0.75A			40	mV
Line regulation	ΔVo	V_I =10.5V to 25V,Tj=25°C			80	mV
		V_I =10.5V to 23V,Tj=25°C,Io=1A			80	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	V_I =10.5V to 23V			1.0	mA
	ΔIq	Io=5mA - 1.0A			0.5	mA
Output Noise Voltage	V_N	10Hz<=f<=100kHz		58		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-0.9		mV/°C
Ripple Rejection	RR	V_I =11.5V to 21.5V, f=120Hz,Tj=25°C	56	72		dB
Peak Output Current	I_{PK}	Tj=25°C		1.8		A
Short-Circuit Current	Isc	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7809 ELECTRICAL CHARACTERISTICS

(VI=15V, Io=0.5A, Tj= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, Io=5mA - 1.0A	8.64	9.0	9.36	V
		V_I =11.5V to 24V, Io=5mA - 1.0A,PD<15W	8.55		9.45	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			90	mV
		Tj=25°C,Io=0.25A - 0.75A			45	mV
Line regulation	ΔVo	V_I =11.5V to 25 V, Tj=25°C, PD<15W			90	mV
		V_I =11.5V to 24V,Tj=25°C, Io<=1A			90	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	V_I =11.5V to 24V			1.0	mA
	ΔIq	Io=5mA – 1.0A			0.5	mA
Output Noise Voltage	V_N	10Hz<=f<=100kHz		58		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-1.1		mV/°C
Ripple Rejection	RR	V_I =12.5V to 22.5V, f=120Hz,Tj=25°C	56	72		dB
Peak Output Current	I_{PK}	Tj=25°C		1.8		A
Short-Circuit Current	Isc	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM709X LINEAR INTEGRATED CIRCUIT

UTC LM709X ELECTRICAL CHARACTERISTICS

UTC LM709X ELECTRICAL CHARACTERISTICS

UTC LM7810 ELECTRICAL CHARACTERISTICS

(V_I=16V, I_O=0.5A, T_j= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, Io=5mA - 1.0A	9.60	10.0	10.40	V
		V_I =12.5V to 25V, Io=5mA - 1.0A,PD<=15W	9.50		10.50	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			100	mV
		Tj=25°C,Io=0.25A - 0.75A			50	mV
Line regulation	ΔVo	V_I =13V to 25V,Tj=25°C			100	mV
		V_I =13V to 25V, Tj=25°C,Io<=1A			100	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	V_I =12.6V to 25V			1.0	mA
	ΔIq	Io=5mA - 1.0A			0.5	mA
Output Noise Voltage	V_N	10Hz<=f<=100kHz		58		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-1.1		mV/°C
Ripple Rejection	RR	V_I =13V - 23V,f=120Hz,Tj=25°C	56	72		dB
Peak Output Current	I_{PK}	Tj=25°C		1.8		A
Short-Circuit Current	Isc	V_I=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7812 ELECTRICAL CHARACTERISTICS

(V_I=19V, I_O=0.5A, T_j= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, Io=5mA - 1.0A	11.52	12.0	12.48	V
		V_I =14.5V to 27V, Io=5mA - 1.0A,PD<15W	11.40		12.60	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			120	mV
		Tj=25°C,Io=0.25A - 0.75A			60	mV
Line regulation	ΔVo	V_I =14.5V to 30V,Tj=25°C			120	mV
		V_I =14.6V to 27V,Tj=25°C, Io=1A			120	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	V_I =14.5V to 30V			1.0	mA
	ΔIq	Io=5mA - 1.0A			0.5	mA
Output Noise Voltage	V_N	10Hz<=f<=100kHz		75		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-1.5		mV/°C
Ripple Rejection	RR	V_I =15V - 25V,f=120Hz,Tj=25°C	55	72		dB
Peak Output Current	I_{PK}	Tj=25°C		1.8		A
Short-Circuit Current	Isc	V_I=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM741CX ELECTRICAL CHARACTERISTICS

(unless otherwise noted, for the LM741CX, 0°C ≤ T_A ≤ 70°C, V_S = ±15V, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	V_{OS}	R_S ≤ 10kΩ		2.0	6.0	mV
		R_S ≤ 50Ω		1.0	5.0	
Input Offset Current	I_{OS}			20	200	nA
				3.0	30	
Input Bias Current	I_B			80	500	nA
				30	80	
Input Resistance	R_{IN}	T_A = 25°C, V_S = ±20V	1.0	6.0		MΩ
Input Offset Voltage Adjustment Range	V_{OS}	T_A = 25°C, V_S = ±20V	±10			mV
Input Capacitance	C_{IN}			1.4		pF
Offset Voltage Adjustment Range	V_{OS}	T_A = 25°C, V_S = ±20V	±10			mV
Large Signal Voltage Gain	A_{VOL}	V_S = ±20V, V_O = ±15V, R_L ≥ 2kΩ	50	200		V/mV
		V_S = ±15V, V_O = ±10V, R_L ≥ 2kΩ	20	200		
Output Voltage Swing	V_O	V_S = ±20V, R_L ≥ 10kΩ	±16	±18		V
		V_S = ±15V, R_L ≥ 2kΩ	±10	±14		
Output Short Circuit Current	I_{SC}			25	40	mA
Common Mode Rejection Ratio	CMRR	R_S ≤ 10kΩ, V_{CM} = ±12V	70	90		dB
		R_S ≤ 50Ω, V_{CM} = ±12V	50	80		
Supply Voltage Rejection Ratio	PSRR	R_S ≤ 10kΩ, V_S = ±20V to ±5V	77	96		dB
		R_S ≤ 50Ω, V_S = ±20V to ±5V	60	86		
Transient Response Rise Time	T_R	V_S = ±20V, R_L = 2kΩ, C_L ≤ 100pF, V_{IN} = ±20mV, A_V = 1		0.25		μs
Transient Response Overshoot	K_O			6.0		%
Slew Rate	SR	V_S = ±20V, R_L = 2kΩ, C_L ≤ 100pF, A_V = 1	0.3	0.7		V/μs

UTC LM741CX ELECTRICAL CHARACTERISTICS

(unless otherwise noted, for the LM741CX, -55°C ≤ T_A ≤ 125°C, V_S = ±15V, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	V_{OS}	R_S ≤ 10kΩ		2.0	7.5	mV
		R_S ≤ 50Ω		1.0	6.0	
Input Offset Current	I_{OS}			20	500	nA
				3.0	70	
Input Bias Current	I_B			80	1500	nA
				30	200	
Input Resistance	R_{IN}	T_A = 25°C, V_S = ±20V	1.0	6.0		MΩ
Input Offset Voltage Adjustment Range	V_{OS}	T_A = 25°C, V_S = ±20V	±10			mV
Input Capacitance	C_{IN}			1.4		pF
Offset Voltage Adjustment Range	V_{OS}	T_A = 25°C, V_S = ±20V	±10			mV
Large Signal Voltage Gain	A_{VOL}	V_S = ±20V, V_O = ±15V, R_L ≥ 2kΩ	25	200		V/mV
		V_S = ±15V, V_O = ±10V, R_L ≥ 2kΩ	10	200		
Output Voltage Swing	V_O	V_S = ±20V, R_L ≥ 10kΩ	±16	±18		V
		V_S = ±15V, R_L ≥ 2kΩ	±10	±14		
Output Short Circuit Current	I_{SC}			25	40	mA
Common Mode Rejection Ratio	CMRR	R_S ≤ 10kΩ, V_{CM} = ±12V	70	90		dB
		R_S ≤ 50Ω, V_{CM} = ±12V	50	80		
Supply Voltage Rejection Ratio	PSRR	R_S ≤ 10kΩ, V_S = ±20V to ±5V	77	96		dB
		R_S ≤ 50Ω, V_S = ±20V to ±5V	60	86		
Transient Response Rise Time	T_R	V_S = ±20V, R_L = 2kΩ, C_L ≤ 100pF, V_{IN} = ±20mV, A_V = 1		0.25		μs
Transient Response Overshoot	K_O			6.0		%
Slew Rate	SR	V_S = ±20V, R_L = 2kΩ, C_L ≤ 100pF, A_V = 1	0.3	0.7		V/μs

UTC LM7815 ELECTRICAL CHARACTERISTICS

(V_I=23V, I_O=0.5A, T_j= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, Io=5mA - 1.0A	14.40	15.0	15.60	V
		V_I =17.5V to 30V, Io=5mA - 1.0A,PD<15W	14.25		15.75	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			150	mV
		Tj=25°C,Io=0.25A - 0.75A			75	mV
Line regulation	ΔVo	V_I =18.5V to 30V,Tj=25°C			150	mV
		V_I =17.7V to 30V, Tj=25°C, Io =1A			150	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	V_I =17.5V to 30V			1.0	mA
	ΔIq	Io=5mA - 1.0A			0.5	mA
Output Noise Voltage	V_N	10Hz<=f<=100kHz		90		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-1.8		mV/°C
Ripple Rejection	RR	V_I =18.5V to 28.5V f=120Hz,Tj=25°C	54	70		dB
Peak Output Current	I_{PK}	Tj=25°C		1.8		A
Short-Circuit Current	Isc	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7818 ELECTRICAL CHARACTERISTICS

(VI=27V, Io=0.5A, Tj= 0°C - 125°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25°C, Io=5mA - 1.0A	17.28	18.0	18.72	V
		V_I =21V to 33V,Io=5mA - 1.0A	17.10		18.90	V
Load Regulation	ΔVo	Tj=25°C,Io=5mA - 1.5A			180	mV
		Tj=25°C,Io=0.25A - 0.75A			90	mV
Line regulation	ΔVo	V_I =21V to 33V,Tj=25°C			180	mV
		V_I =21V to 33V, Tj=25°C, Io =<1A,PD<15W			180	mV
Quiescent Current	Iq	Tj=25°C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	V_I =21.5V to 33V			1.0	mA
	ΔIq	Io=5mA - 1.0A			0.5	mA
Output Noise Voltage	V_N	10Hz<=f<=100kHz		110		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-2.2		mV/°C
Ripple Rejection	RR	V_I =22V - 32V,f=120Hz,Tj=25°C	53	69		dB
Peak Output Current	I_{PK}	Tj=25°C		1.8		A
Short-Circuit Current	Isc	VI=35V, Tj=25°C		250		mA
Dropout Voltage	Vd	Tj=25°C		2.0		V

UTC LM7824 ELECTRICAL CHARACTERISTICS

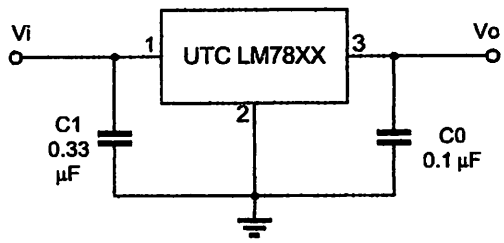
(V_I=33V, I_O=0.5A, T_J= 0°C - 12°C, C1=0.33uF, Co=0.1uF, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	T_J=25°C, I_O=5mA - 1.0A	23.04	24.0	24.96	V
		V_I =27V to 38V,I_O=5mA - 1.0A	22.80		25.20	V
Load Regulation	ΔVo	T_J=25°C,I_O=5mA - 1.5A			240	mV
		T_J=25°C,I_O=0.25A - 0.75A			120	mV
Line regulation	ΔVo	V_I =27V to 38V,T_J=25°C			240	mV
		V_I =27V to 38V,T_J=25°C,I_O=1A			240	mV
Quiescent Current	I_Q	T_J=25°C, I_O=<1A			8.0	mA
Quiescent Current Change	ΔIq	V_I =28V to 38V			1.0	mA
	ΔIq	I_O=5mA - 1.0A			0.5	mA
Output Noise Voltage	V_N	10Hz<=f<=100kHz		170		μV
Temperature coefficient of Vo	ΔVo/ΔT	I_O=5mA		-2.8		mV/°C
Ripple Rejection	RR	V_I =28V - 38V,f=120Hz,T_J=25°C	50	66		dB
Peak Output Current	I_{PK}	T_J=25°C		1.8		A
Short-Circuit Current	Isc	VI=35V, T_J=25°C		250		mA
Dropout Voltage	Vd	T_J=25°C		2.0		V

Note 1: The Maximum steady state usable output current are dependent on input voltage, heat sinking, lead length of the package and copper pattern of PCB. The data above represents pulse test conditions with junction temperatures specified at the initiation of test.

Note 2: Power dissipation<0.5W

APPLICATION CIRCUIT



Note 1: To specify an output voltage, substitute voltage value for "XX".

Note 2: Bypass capacitors are recommended for optimum stability and transient response and should be located as close as possible to the regulators.

UTC LM8XX SERIES ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	LM8XX			UNIT
		MIN	TYP	MAX	
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APPLICATION CIRCUIT

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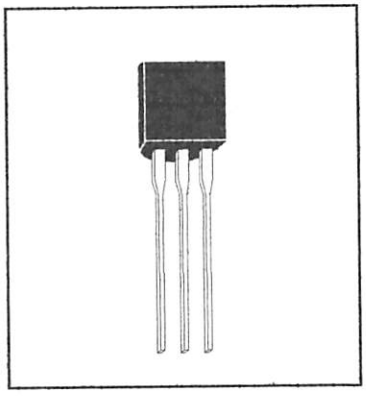
HSA1015

NP EPITAXIAL PLANAR TRANSISTOR



escription

he HSA1015 is designed for use in driver stage of AF amplifier and eneral purpose amplification.

bsolute Maximum Ratings

Maximum Temperatures
Storage Temperature ..... -55 ~ +150 °C
Junction Temperature ..... +150 °C Maximum

Maximum Power Dissipation
Total Power Dissipation (Ta=25°C) ..... 400 mW

Maximum Voltages and Currents (Ta=25°C)
VCBO Collector to Base Voltage ..... -50 V
VCEO Collector to Emitter Voltage ..... -50 V
VEBO Emitter to Base Voltage ..... -5 V
IC Collector Current ..... -150 mA

haracteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BVCBO	-50	-	-	V	IC=-100uA, IE=0
BVCEO	-50	-	-	V	IC=-1mA, IB=0
BVEBO	-5	-	-	V	IE=-10uA, IC=0
ICBO	-	-	-100	nA	VCB=-50V, IE=0
IEBO	-	-	-100	nA	VEB=-5V, IC=0
*VCE(sat)	-	-	-300	mV	IC=-100mA, IB=-10mA
*VBE(sat)	-	-	-1.1	V	IC=-100mA, IB=-10mA
*hFE1	120	-	700		VCE=-6V, IC=-2mA
*hFE2	25	-	-		VCE=-6V, IC=-150mA
fT	80	-	-	MHz	VCE=-10V, IC=-1mA, f=100MHz
Cob	-	-	7	pF	VCB=-10V, f=1MHz, IE=0

*Pulse Test : Pulse Width ≤380us, Duty Cycle≤2%

lassification Of hFE1

Rank	Y	GR	BL
Range	120-240	200-400	350-700

HSA1015

PNP EPITAXIAL PLANAR TRANSISTOR

Description

The HSA1015 is designed for use in driver stage of AF amplifier and low speed switching applications.

Absolute Maximum Ratings

Operation Temperature
Storage Temperature ..... -55~150°C
Junction Temperature ..... -55~150°C

Maximum Power Dissipation
Total Power Dissipation (Ta=25°C) 400mW

Maximum Voltage and Current (Ta=25°C)
V_{CBO} Collector to Base Voltage ..... -50V
V_{CEO} Collector to Emitter Voltage ..... -50V
V_{EBO} Emitter to Base Voltage ..... -5V
I_C Collector Current ..... -150mA

Characteristics (Ta=25°C)

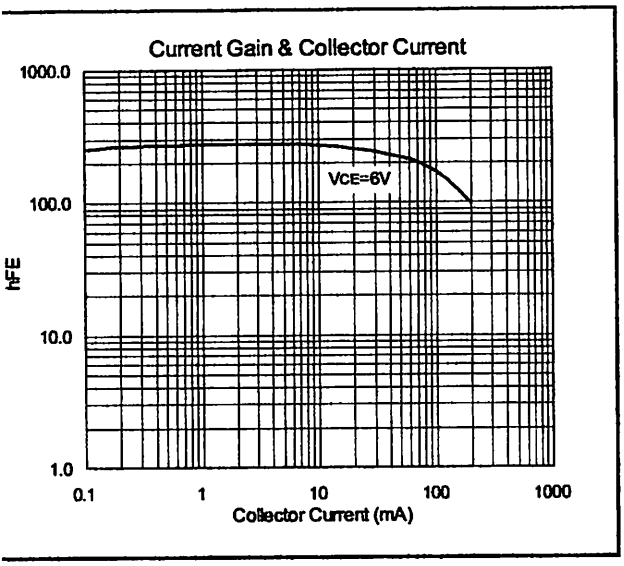
Symbol	Min	Typ	Max	Unit	Test Conditions
BV_{CBO}	-50	-	-	V	I_C=-100μA, I_E=0
BV_{CEO}	-50	-	-	V	I_C=-1mA, I_B=0
BV_{EBO}	-5	-	-	V	I_E=-100μA, I_C=0
I_{CBO}	-	-	-100	nA	V_{CB}=-50V, I_E=0
I_{EBO}	-	-	-100	nA	V_{EB}=-5V, I_C=0
$V_{CE(sat)}$	-	-	-0.3	V	I_C=-100mA, I_B=-10mA
$V_{BE(sat)}$	-	-	-1.1	V	I_C=-100mA, I_B=-10mA
$h_{FE(1)}$	70	-	700		V_{CE}=-6V, I_C=-1mA
$h_{FE(2)}$	25	-	-		V_{CE}=-6V, I_C=-150mA
f_T	80	-	-	MHz	V_{CE}=-6V, I_C=-10mA, f=30MHz
C_{ob}	-	3.5	4	pF	V_{CB}=-10V, I_E=0, f=1MHz
C_{ib}	-	10	-	pF	V_{EB}=-0.5V, I_C=0, f=1MHz
NF	-	-	1	dB	V_{CE}=-6V, I_C=-0.1mA, f=1KHz, Rg=10KΩ

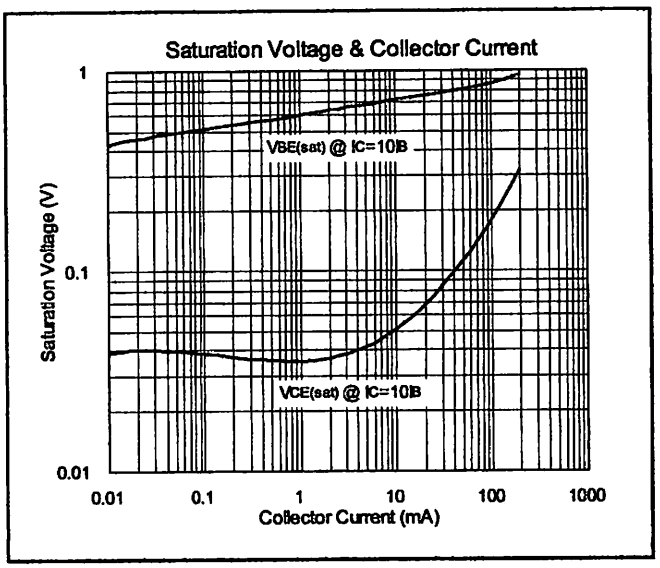
*Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%

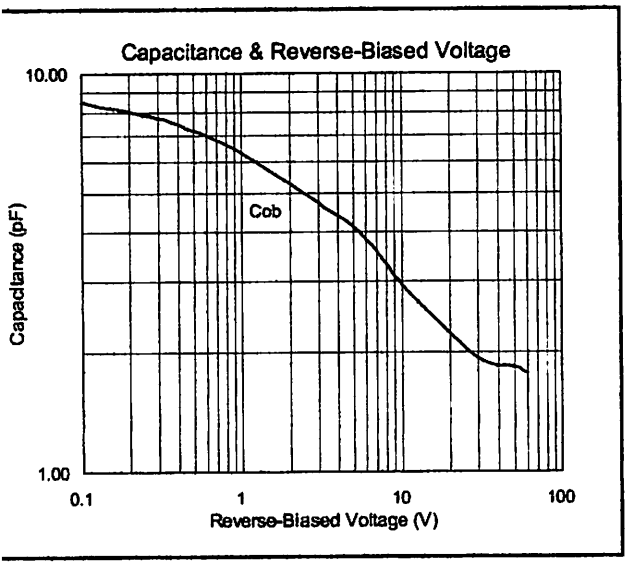
Classification Of $h_{FE(1)}$

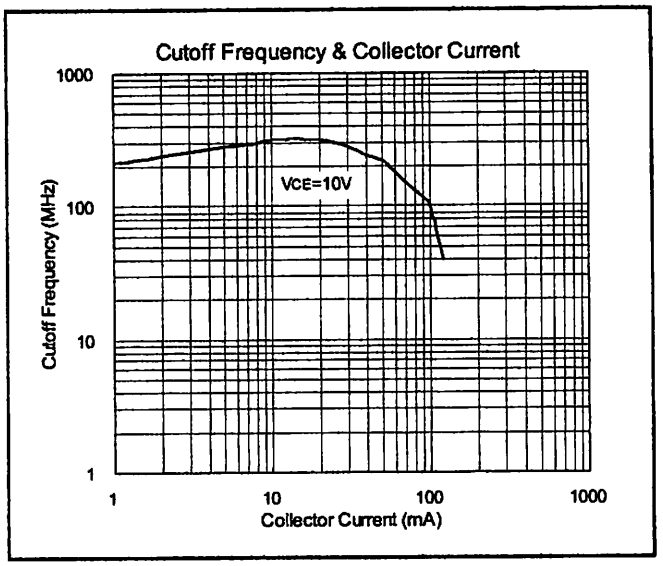
Rank	Y	GR	BL
Range	120~240	200~400	350~700

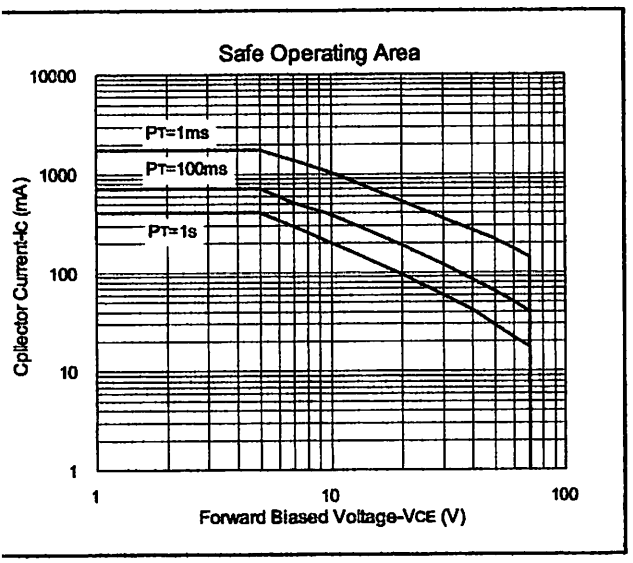
haracteristics Curve

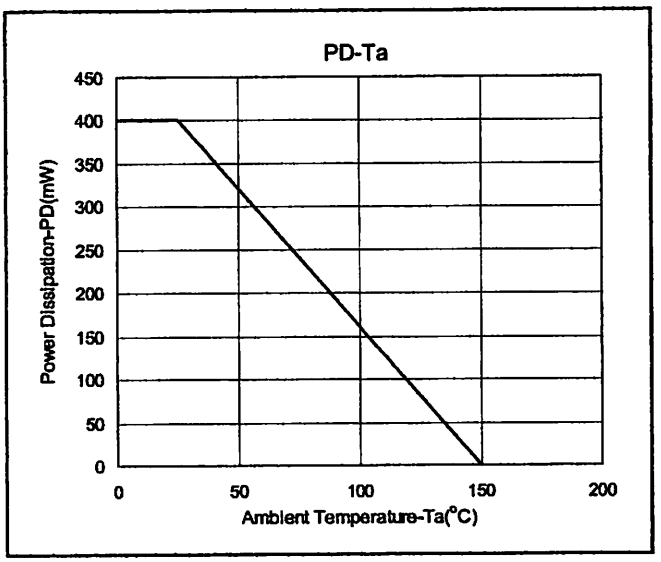




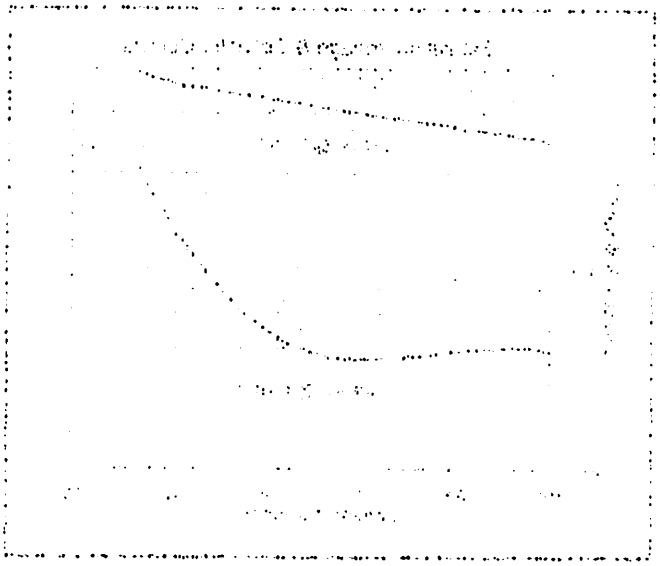


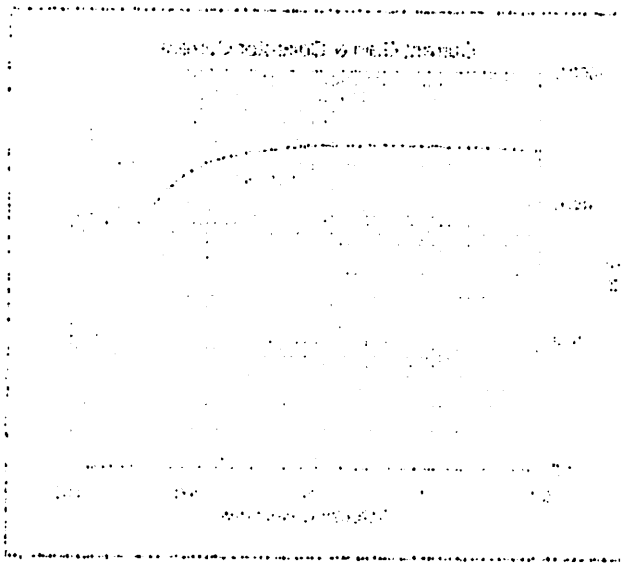


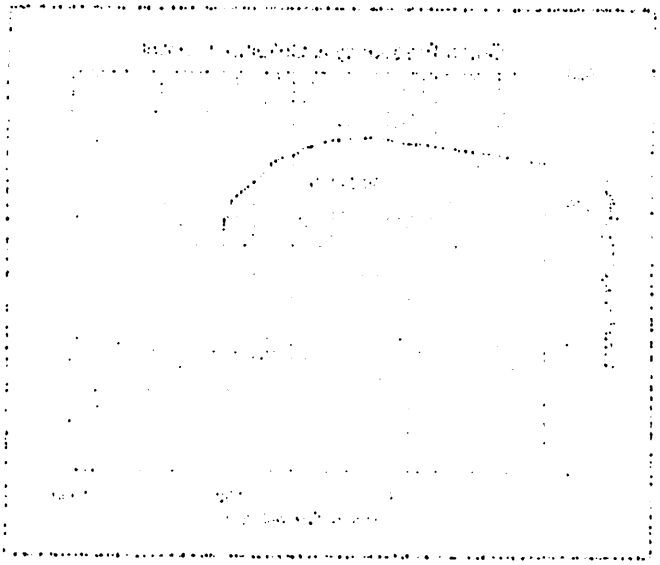


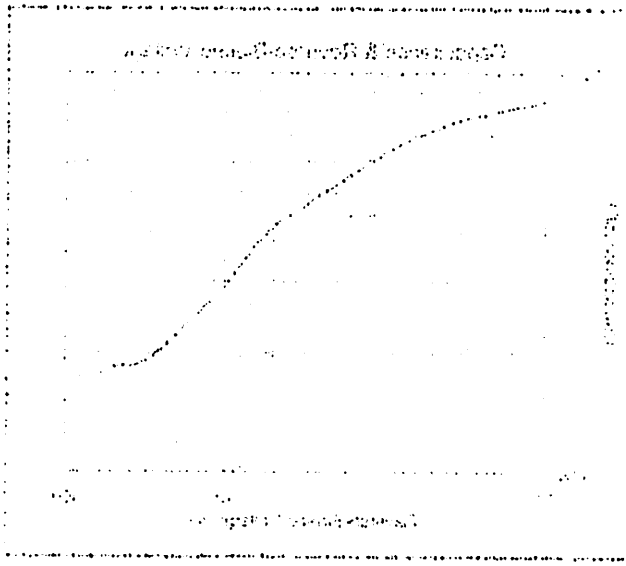


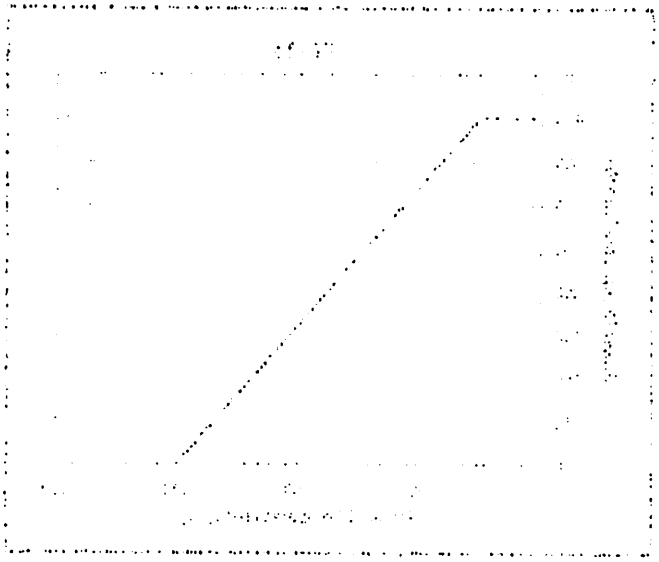
Characterization Curve

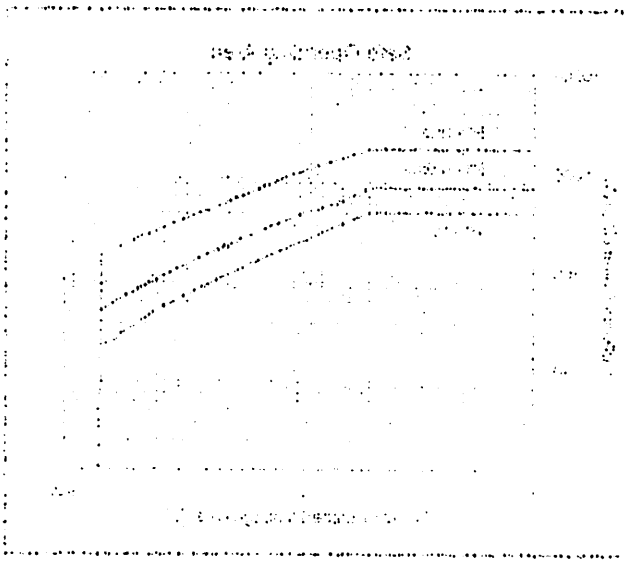




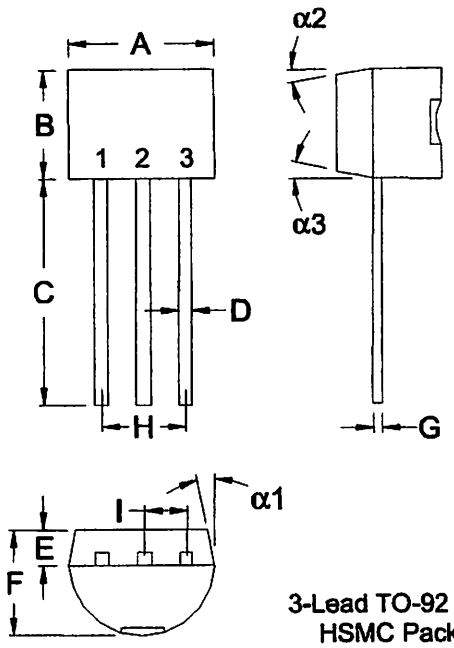


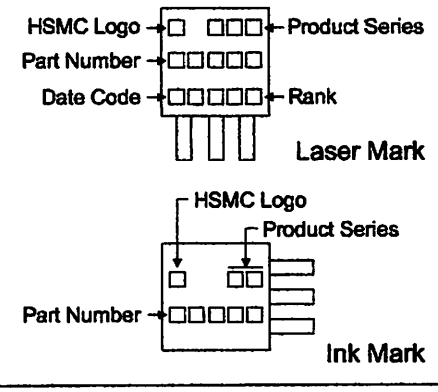






D-92 Dimension





Style : Pin 1.Emitter 2.Collector 3.Base

3-Lead TO-92 Plastic Package
HSMC Package Code : A

*:Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1704	0.1902	4.33	4.83	G	0.0142	0.0220	0.36	0.56
B	0.1704	0.1902	4.33	4.83	H	-	*0.1000	-	*2.54
C	0.5000	-	12.70	-	I	-	*0.0500	-	*1.27
D	0.0142	0.0220	0.36	0.56	α1	-	*5°	-	*5°
E	-	*0.0500	-	*1.27	α2	-	*2°	-	*2°
F	0.1323	0.1480	3.36	3.76	α3	-	*2°	-	*2°

Notes : 1.Dimension and tolerance based on our Spec. dated Apr. 25,1996.
2.Controlling dimension : millimeters.
3.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
4.If there is any question with packing specification or packing method, please contact your local HSMC sales office.

Material :

- Lead : 42 Alloy ; solder plating
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0

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HI-SINCERITY
MICROELECTRONICS CORP.

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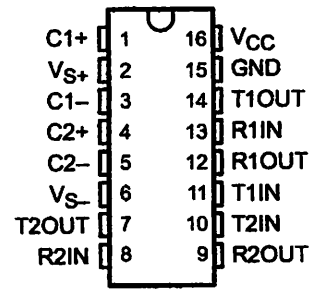
Datasheets for electronics components.

- Meet or Exceed TIA/EIA-232-F and ITU Recommendation V.28
- Operate With Single 5-V Power Supply
- Operate Up to 120 kbit/s
- Two Drivers and Two Receivers
- ±30-V Input Levels
- Low Supply Current . . . 8 mA Typical
- Designed to be Interchangeable With Maxim MAX232
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
- Applications
  - TIA/EIA-232-F
  - Battery-Powered Systems
  - Terminals
  - Modems
  - Computers

MAX232 . . . D, DW, N, OR NS PACKAGE
MAX232I . . . D, DW, OR N PACKAGE
(TOP VIEW)



description/ordering information

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels from a single 5-V supply. Each receiver converts EIA-232 inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube	MAX232N	MAX232N
	SOIC (D)	Tube	MAX232D	MAX232
		Tape and reel	MAX232DR	
	SOIC (DW)	Tube	MAX232DW	MAX232
		Tape and reel	MAX232DWR	
	SOP (NS)	Tape and reel	MAX232NSR	MAX232
–40°C to 85°C	PDIP (N)	Tube	MAX232IN	MAX232IN
	SOIC (D)	Tube	MAX232ID	MAX232I
		Tape and reel	MAX232IDR	
	SOIC (DW)	Tube	MAX232IDW	MAX232I
		Tape and reel	MAX232IDWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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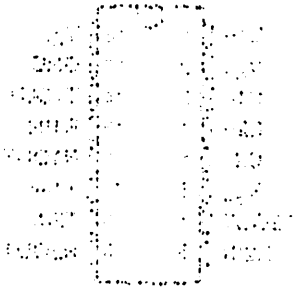

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Function Tables

EACH DRIVER

INPUT TIN	OUTPUT TOUT
L	H
H	L

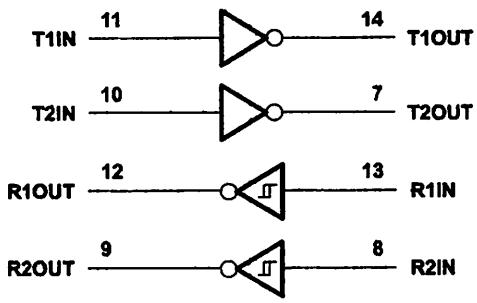
H = high level, L = low level

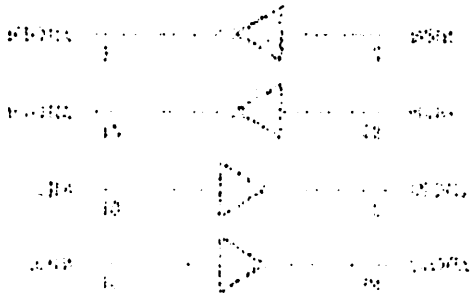
EACH RECEIVER

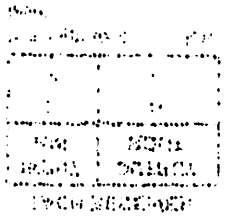
INPUT RIN	OUTPUT ROUT
L	H
H	L

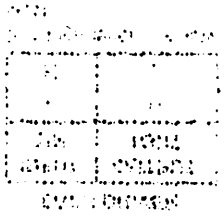
H = high level, L = low level

gic diagram (positive logic)









absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input supply voltage range, V_{CC} (see Note 1) ..... –0.3 V to 6 V
Positive output supply voltage range, V_{S+} ..... V_{CC} – 0.3 V to 15 V
Negative output supply voltage range, V_{S-} ..... –0.3 V to –15 V
Input voltage range, V_I: Driver ..... –0.3 V to V_{CC} + 0.3 V
Receiver ..... ±30 V
Output voltage range, V_O: T1OUT, T2OUT ..... V_{S-} – 0.3 V to V_{S+} + 0.3 V
R1OUT, R2OUT ..... –0.3 V to V_{CC} + 0.3 V
Short-circuit duration: T1OUT, T2OUT ..... Unlimited
Package thermal impedance, θ_{JA} (see Note 2): D package ..... 73°C/W
DW package ..... 57°C/W
N package ..... 67°C/W
NS package ..... 64°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

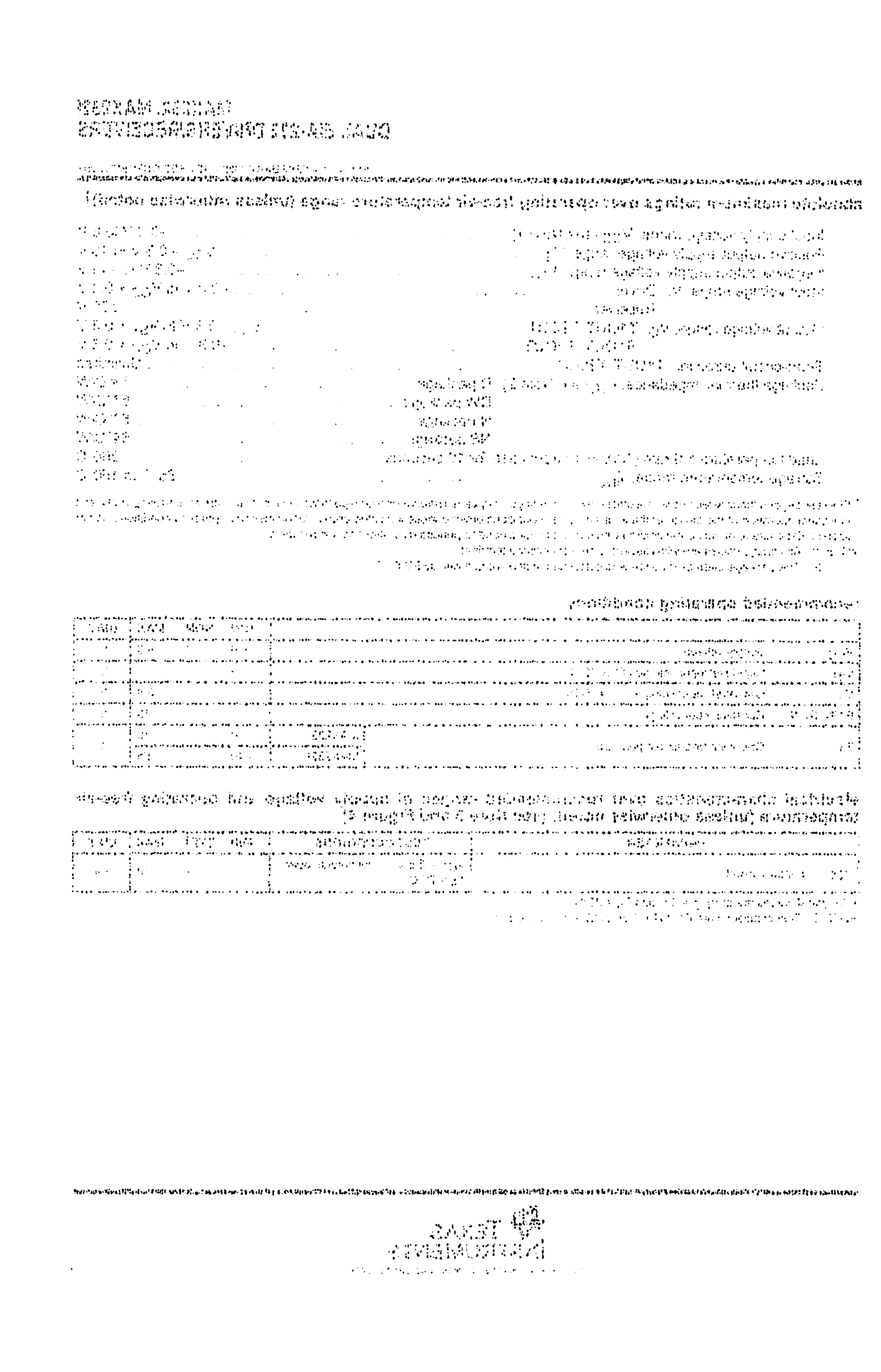
recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (T1IN,T2IN)		2			V
V_{IL}	Low-level input voltage (T1IN, T2IN)				0.8	V
R1IN, R2IN	Receiver input voltage				±30	V
T_A	Operating free-air temperature	MAX232	0		70	°C
		MAX232I	–40		85	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3 and Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5 V, All outputs open, T_A = 25°C		8	10	mA

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 3: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.



DRIVER SECTION

ectrical characteristics over recommended ranges of supply voltage and operating free-air mperature range (see Note 3)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
OH	High-level output voltage	T1OUT, T2OUT	R_L = 3 kΩ to GND		5	7		V
OL	Low-level output voltage‡	T1OUT, T2OUT	R_L = 3 kΩ to GND			–7	–5	V
o	Output resistance	T1OUT, T2OUT	V_{S+} = V_{S-} = 0,	V_O = ±2 V	300			Ω
OS§	Short-circuit output current	T1OUT, T2OUT	V_{CC} = 5.5 V,	V_O = 0		±10		mA
S	Short-circuit input current	T1IN, T2IN	V_I = 0				200	µA

All typical values are at V_{CC} = 5 V, T_A = 25°C.
The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage evels only.
Not more than one output should be shorted at a time.
OTE 3: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

witching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R	Driver slew rate	R_L = 3 kΩ to 7 kΩ, See Figure 2			30	V/µs
R(t)	Driver transition region slew rate	See Figure 3		3		V/µs
	Data rate	One TOUT switching		120		kbit/s

OTE 3: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

lectrical characteristics over recommended ranges of supply voltage and operating free-air emperature range (see Note 3)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
OH	High-level output voltage	R1OUT, R2OUT	I_{OH} = –1 mA		3.5			V
OL	Low-level output voltage‡	R1OUT, R2OUT	I_{OL} = 3.2 mA				0.4	V
IT+	Receiver positive-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V,	T_A = 25°C		1.7	2.4	V
IT–	Receiver negative-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V,	T_A = 25°C	0.8	1.2		V
hys	Input hysteresis voltage	R1IN, R2IN	V_{CC} = 5 V		0.2	0.5	1	V
i	Receiver input resistance	R1IN, R2IN	V_{CC} = 5,	T_A = 25°C	3	5	7	kΩ

All typical values are at V_{CC} = 5 V, T_A = 25°C.
The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage evels only.
OTE 3: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

witching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 3 and Figure 1)

PARAMETER		TYP	UNIT
PLH(R)	Receiver propagation delay time, low- to high-level output	500	ns
PHL(R)	Receiver propagation delay time, high- to low-level output	500	ns

OTE 3: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

[illegible] SECTION

[illegible] electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
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† All typical values are at V_{CC} = 5 V, T_A = 25°C.
[illegible]

[illegible] switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
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[illegible] Switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
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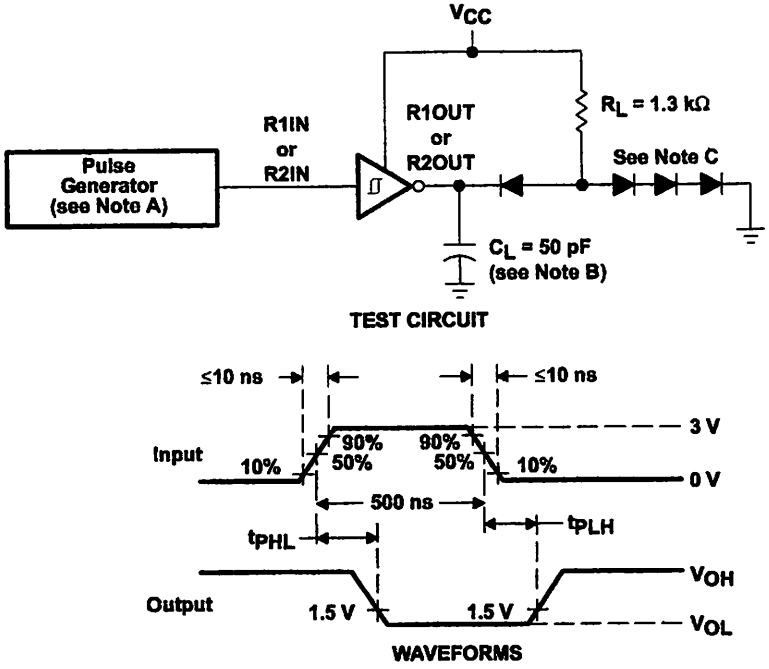
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
[illegible]

[illegible] switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 3 and Figure 4)

PARAMETER	TYP	UNIT
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]

† All typical values are at V_{CC} = 5 V.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements

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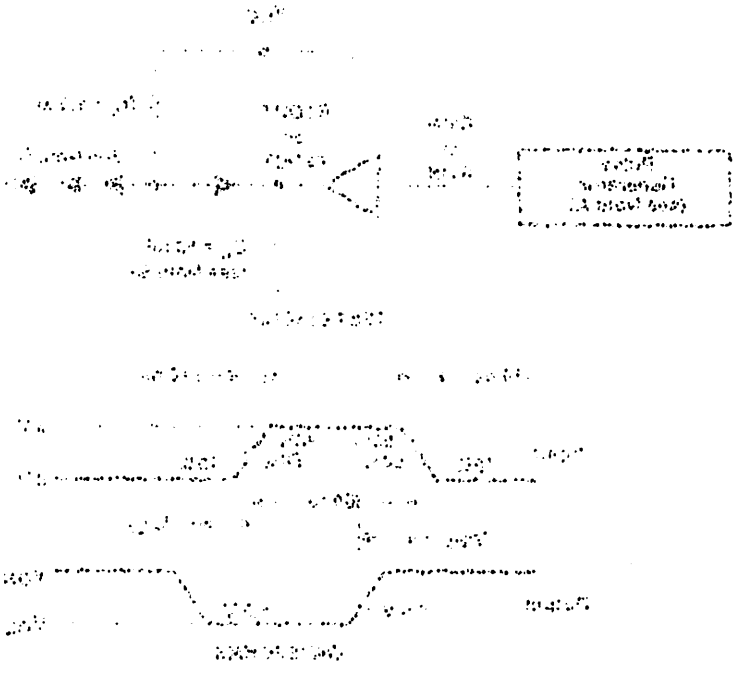

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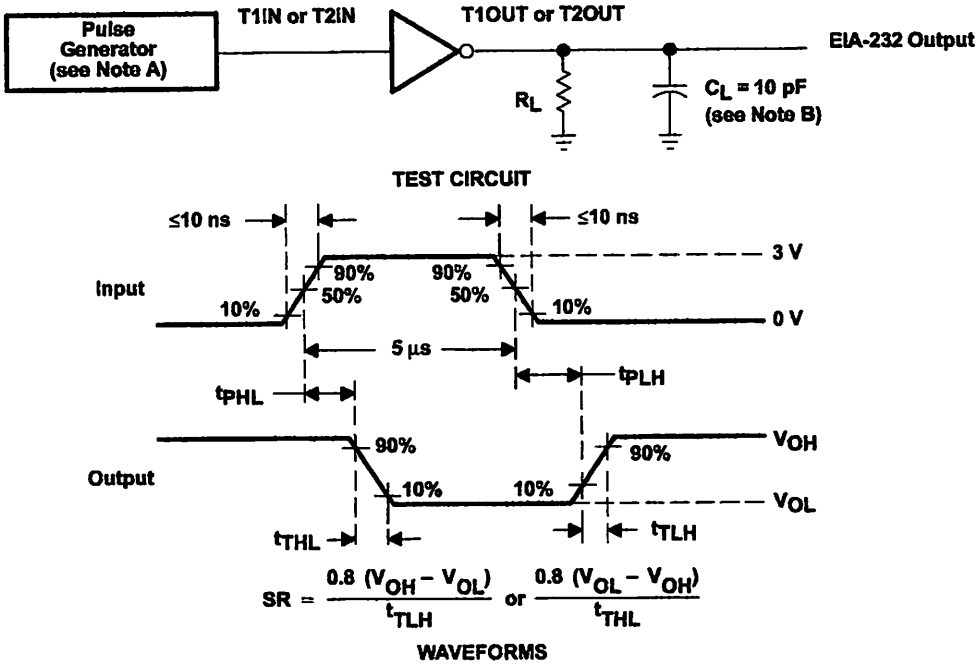
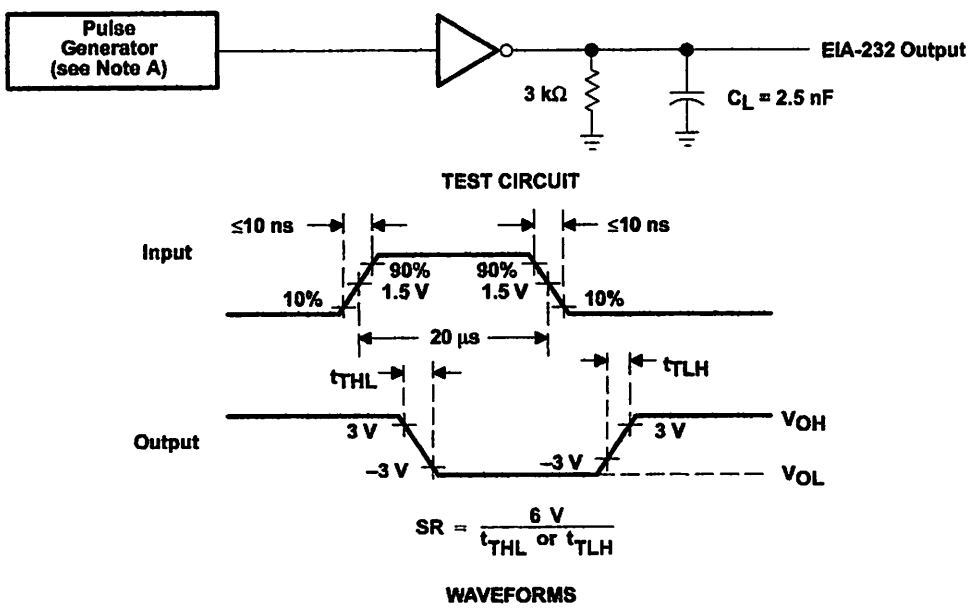
Figure 1. [illegible]

PARAMETER MEASUREMENT INFORMATION



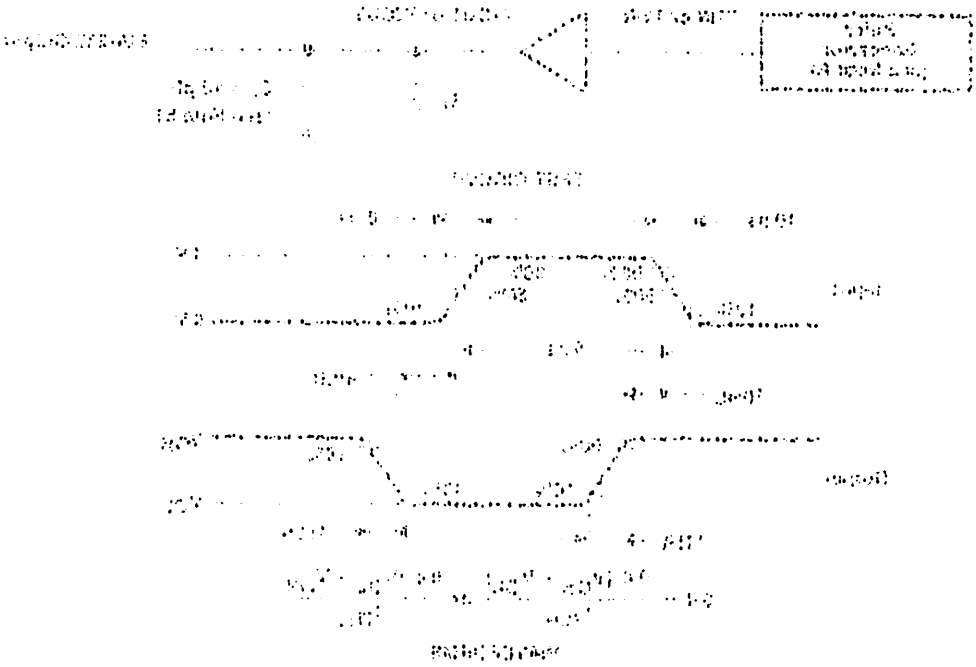
OTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

Figure 2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5-µs Input)

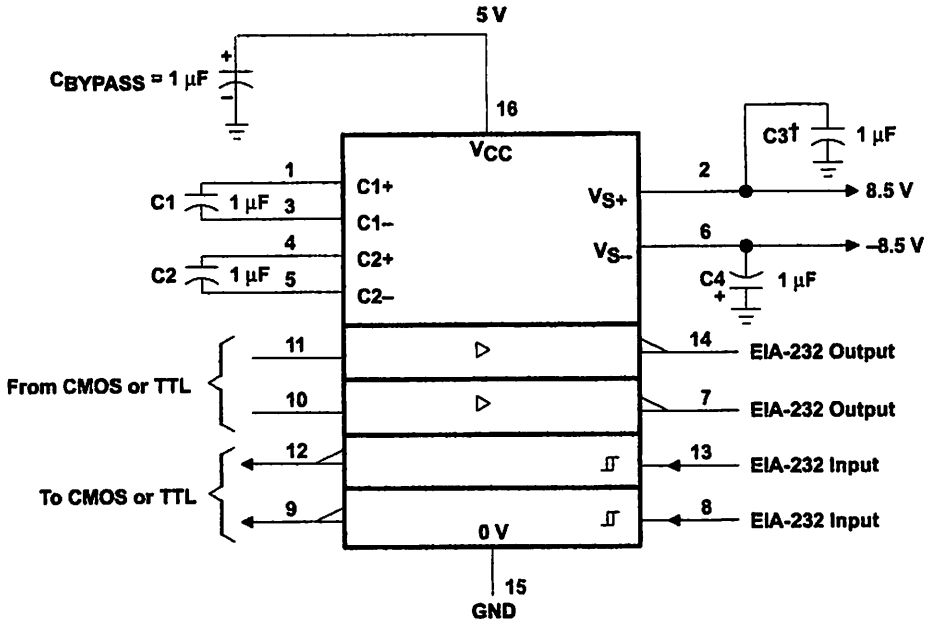


OTE A: The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

Figure 3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20-µs Input)



APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

Figure 4. Typical Operating Circuit

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