# SKRIPSI

## PERENCANAAN DAN PEMBUATAN ALAT KONTROL PENJEJAK MATAHARI YANG DIGUNAKAN UNTUK OPTIMASI PENYERAPAN RADIASI MATAHARI PADA SEL SURYA BERBASIS MIKROKONTROLER ATMEGA 16



*Disusun Oleh:*

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**JURUSAN TEKNIK ELEKTRO S-1**
**KONSENTRASI TEKNIK ELEKTRONIKA**
**FAKULTAS TEKNOLOGI INDUSTRI**
**INSTITUT TEKNOLOGI NASIONAL MALANG**

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## LEMBAR PERSETUJUAN

# PERENCANAAN DAN PEMBUATAN ALAT KONTROL PENJEJAK MATAHARI YANG DIGUNAKAN UNTUK OPTIMASI PENYERAPAN RADIASI MATAHARI PADA SEL SURYA BERBASIS MIKROKONTROLER AT MEGA 16

## SKRIPSI

*Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektronika Strata Satu (S-1)*


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**2008**

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
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Dipertahankan di hadapan majelis penguji Skripsi jenjang Strata satu ( S-1 ) pada :

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# ABSTRAKSI

## PERENCANAAN DAN PEMBUATAN ALAT KONTROL PENJEJAK MATAHARI YANG DIGUNAKAN UNTUK OPTIMASI PENYERAPAN RADIASI MATAHARI PADA SEL SURYA BERBASIS MIKROKONTROLER ATMEGA16

(Neal Ajie, 03.17.104, Teknik Elektro S.1/Elektronika)
(Dosen Pembimbing I: Ir. Yusuf Ismail Nakhoda, MT.)
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Dalam era modern saat ini dibutuhkan sumber energi listrik baru dan itu bisa lapat dari matahari dikarenakan energi matahari tidak akan habis, dengan nggunakan sebuah modul sel surya. Karena penggunaan modul sel surya untuk nghasilkan energi listrik sangat kecil, sehingga diperlukan mekanisasi dan kontrol tuk membantu mengoptimalkan penyerapan radiasi matahari,dimana modul sel surya i nantinya dapat bergerak mengikuti arah matahari.

Dalam pembuatan peralatan pengontrolan ini, memanfaatkan mikrokontroler AT EGA 16 sebagai pemroses utama.Untuk gerakan dari panel sel surya terdiri dari dua ah motor DC, dan untuk mendeteksi dari cahaya matahari digunakan lima buah sensor DR, empat sensor untuk mendeteksi empat arah yaitu timur, barat, utara, selatan, dan tu sensor digunakan untuk mendeteksi terbenamnya matahari.Alat ini bekerja dengan embandingkan antar dua sensor yang saling behadapan, apabila salah satu sensor lebih lap/tidak mendapat sinar matahari maka modul sel surya akan bergerak sampai kedua nsor sama – sama mendapat cahaya.

Penggunaan Kontrol semacam ini dapat memaksimalkan modul sel surya untuk enyerap radiasi matahari Ini dapat dilihat dari perolehan energi pada saat pengujian itu untuk diam sebesar108.6 Wh/hari sedangkan yang bergerak sebesar 184.4 Wh/hari . alam kontrol utamanya juga akan diperoleh error alat yang sudah dikonversikan dalam ersen yaitu sebesar 8.33 % pada saat panel sel surya menghadap arah timur, 10 % saat enghadap tegak lurus, 5.83 % saat menghadap barat.Dimana ini juga berpengaruh rhadap hasil penyerapan radiasi matahari.

**Kata kunci:** modul sel surya, sensor, LDR, charge control, AT MEGA 16, op amp

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Malang, Maret 2008

Penulis

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# JAYALAH NEGERI INI

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# BAB I

# PENDAHULUAN

## 1.1. Latar Belakang

Berkembangnya ilmu pengetahuan dan teknologi sekarang ini, khususnya perkembangan teknologi dibidang elektronik. Perkembangan ini haruslah dibarengi dengan kualitas sumber daya manusia yang tinggi pula. Terciptanya alat – alat yang serba modern belum tentu dapat kita beli, ini disebabkan harga dari alat tersebut masih terlalu mahal. Hal ini dapat kita atasi apabila kita dapat membuat sendiri alat tersebut sehingga biaya yang kita keluarkan lebih murah dibandingkan kita membeli alat tersebut dalam keadaan sudah jadi.

Sebagai contoh disini adalah pembangkit listrik tenaga matahari, dimana konsumsi listrik saat ini sebagian besar berasal dari listrik PLN yang sebagian besar sumbernya adalah pembangkit listrik tenaga air (PLTA) dan pembangkit listrik tenaga uap (PLTU). Sedangkan di negara kita banyak sumber – sumber alam yang dapat dijadikan pembangkit listrik,contohnya pembangkit listrik tenaga angin, dan juga pembangkit listrik tenaga surya yang sudah ada saat ini.karena energi matahari yang melimpah mungkin sekali untuk digunakan sebagai penghasil energi listrik yang handal. Karena itu disini penulis ingin membuat alat yang dapat membantu mengoptimalkan penyerapan matahari pada *solar cell*.

Dimana alat ini nantinya dapat bekerja secara otomatis yaitu dengan mengikuti arah terbit dan terbenamnya matahari, tidak hanya itu, karena matahari mempunyai "gerak semu matahari" sebagai efek dari revolusi bumi. Sehingga pada bulan – bulan tertentu matahari terbit dan tenggelam pada arah yang tidak biasanya kadang matahari terlihat berada di belahan utara, lain waktu berada dibelahan selatan, dan kadang ada kalanya berada tepat dikhatulistiwa. Beruntunglah kita yang secara geografis tinggal didekat khatulistiwa ( kepulauan indonesia membentang dari 6 derajat LS, 11 derajat LU ), sebab bukan hal yang sulit untuk dapat mengamati gerak bolak – balik matahari dibelahan utara dan selatan sampai dikedua garis baliknya ( utara dan selatan ).

Pada tanggal 21 maret, matahari melintasi khatulistiwa dititik *vernal equinox* dalam perjalanannya dari selatan menuju utara. *Vernal equinox* ini menandai satu dari dua titik istimewa di sepanjang garis potong antara bidang khatulistiwa langit (perluasan khatulistiwa bumi) dengan bidang *ekliptika* (bidang orbit Bumi mengitari Matahari). Pada saat tersebut posisi terbit dan terbenam Matahari tepat di arah timur dan barat dan siang malam akan memiliki panjang waktu yang sama, yakni masing-masing selama 12 jam (kata *equinox* sendiri berarti *equal night*). Ketika Matahari mencapai titik tertingginya di bola langit dalam gerak semu harian, saat itulah sebatang tongkat tegak di khatulistiwa akan kehilangan bayang-bayangnya. Tibanya Matahari di titik *vernal equinox* ini menandai awal musim semi dibelahan utara Bumi dan awal musim gugur bagi belahan selatan.

Tiga bulan berikutnya, yakni sekitar tanggal 21 Juni, Matahari tiba di posisi paling utara (*summer solstice*) dalam pergerakannya di bola langit. Bagi penduduk

belahan utara Bumi, saat ini menandai siang terpanjang (musim panas) pada sepanjang tahun dan sebaliknya, sebagai siang terpendek selama revolusi Bumi bagi mereka yang tinggal di belahan selatan. Setelah berada di titik terjauhnya di utara khatulistiwa, karena itu guna mengoptimalkan jatuhnya sinar matahari pada permukaan *Solar Cell* dibuatlah alat ini. Dimana energi yang dihasilkan dari proses ini, akan disimpan di *Accu* yang diharapkan akan menggantikan posisi *solar cell* sebagai penyuplai utama arus listrik pada malam hari. Selain itu *Accu* disini juga berperan untuk penyetabil arus dan tegangan sebelum masuk ke beban. Penyusunan dan pembuatan skripsi PERENCANAAN DAN PEMBUATAN ALAT KONTROL PENJEJAK MATAHARI YANG DIGUNAKAN UNTUK OPTIMASI PENYERAPAN RADIASI MATAHARI PADA SEL SURYA BERBASIS MIKROKONTROLER AT MEGA 16 ini diharapkan akan tercipta alat bantu yang dapat memberikan kemudahan bagi kita dan masyarakat umumnya, dalam memanfaatkan sumber daya alam untuk konsumsi sehari – hari.

## 1.2. Rumusan Masalah

Masalah yang ditekankan pada penyusunan skripsi ini adalah:

Bagaimana merencanakan dan membuat alat kontrol yang digunakan sebagai penjejak posisi matahari untuk optimasi penyerapan sinar matahari pada sel surya ( *Fotovoltaik* ).

## 1.3. Batasan Masalah

- *Fotovoltaik* yang digunakan sudah dalam bentuk modul
- Kemiringan *fotovoltaik* sebesar 45°.
- Pemanfaatan sensor sebagai pendeteksi posisi dimana matahari berada pada saat itu.
- Mengenai perhitungan mekanis tidak dibahas dalam tugas akhir ini.
- Menggunakan *mikrokontroler AT MEGA 16* sebagai kontrol otomatis gerakan fotovoltaik.
- Membahas sistem kerja *driver relay* yang digunakan sebagai kontrol gerak dari motor.

## 1.4. Tujuan

Tujuan dari pembuatan skripsi ini adalah merencanakan dan membuat alat kontrol yang dapat mengoptimalkan penyerapan sinar matahari untuk pembangkit listrik tenaga surya.

## 1.5. Metodologi Perancangan

Metodologi yang digunakan dalam perancangan dan pembuatan alat control penjejak matahari yang digunakan untuk optimasi penyerapan radiasi matahari pada sel surya berbasis mikrokontroler AT Mega16 adalah sebagai berikut:

a. Studi literatur untuk memahami pemrograman mikrokontroler AT Mega16 dan rangkaian komparator.

b. Pada tahap realisasi alat yang dibuat, dilakukan perancangan alat yang meliputi merancang rangkaian untuk tiap-tiap blok dan rancangan rangkaian keseluruhan sistem, pembuatan PCB, dan perakitan hasil rancangan.

c. Untuk mengetahui cara kerja alat, maka dilakukan pengujian tiap blok dan pengujian secara keseluruhan. Pengujian tiap blok meliputi pengujian : (1).Detektor cahaya (LDR), (2).Rangkaian Driver Motor DC, (3).Rangkaian *Charge Control*, (4).Pengkondisi Sinyal, (5).Pengambilan Data Daya yang dihasilkan Sel Surya, (6).Pengujian keseluruhan sistem dilakukan dengan menggabungkan seluruh rangkaian elektronik, mekanik alat dan program.

d. Menganalisis hasil pengujian untuk membuat kesimpulan.

## 1.6. Sistematika Penulisan

Sistematika pembahasan dari skripsi ini terdiri dari pokok pembahasan yang saling berkaitan antara satu dengan lainnya, yaitu :

**Bab I Pendahuluan**

Pada bab ini dibahas tentang latar belakang permasalahan, rumusan masalah, batasan masalah, sistematika pembahasan dari alat yang direncanakan.

**Bab II Landasan Teori**

Pada bab ini dibahas tentang teori-teori yang mendukung dalam perencanaan dan pembuatan alat PERENCANAAN DAN PEMBUATAN ALAT KONTROL PENJEJAK MATAHARI YANG DIGUNAKAN

UNTUK OPTIMASI PENYERAPAN RADIASI MATAHARI PADA SEL SURYA BERBASIS MIKROKONTROLER AT MEGA 16 ini.

**Bab III Perencanaan Dan Pembuatan Alat**

Pada bab ini dibahas tentang perencanaan dan pembuatan perangkat keras (hardware).

**Bab IV Pengujian Alat**

Pada bab ini dibahas tentang proses serta hasil dari pengujian alat.

**Bab V Penutup**

Pada bab ini akan disampaikan kesimpulan dari perencanaan dan pembuatan serta pengujian alat.

**LAMPIRAN-LAMPIRAN**

# BAB II

# TEORI DASAR

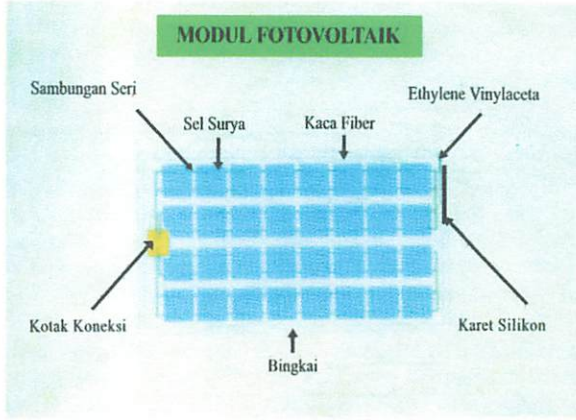
## 2.1. Pendahuluan

Pada bab ini akan dibahas mengenai teori penunjang dari peralatan yang direncanakan. Teori penunjang ini akan membahas tentang komponen dan peralatan pendukung pada alat yang dibuat. Pokok pembahasan pada bab ini adalah :

- Teori tentang Panel Surya
- Teori tentang Baterai Penyimpanan (Accu)
- Teori tentang Motor DC
- Teori tentang LDR
- Teori tentang Relay
- Mikrokontroller AT MEGA 16
- Mikrokontroler AT89C2051

## 2.2. Panel Surya

Panel surya adalah suatu komponen elektronika yang dapat mengubah energi surya menjadi energi listrik dalam bentuk arus searah (DC). Modul *fotovoltaik* adalah unit rangkaian yang lengkap (dilapisi bahan kedap air) dan tahan terhadap perubahan cuaca. Tersusun dari sejumlah sel surya yang dirangkai secara seri dan paralel. Hal ini bertujuan untuk meningkatkan tegangan dan arus yang dihasilkan sehingga cukup untuk pemakaian *system* catu daya beban.




Gambar 2.1. Sel Surya Bahan Polykristal[13]

Secara garis besar kerja dari sel surya (bahan dasar *silicon*) yang terlihat pada gambar, dapat dijelaskan sebagai berikut. Bila *foton* yang terdiri dari jutaan *partikel* berenergi tinggi akibat *radiasi* matahari menumbuk *atom silicon* dari sel surya dan menghasilkan *electron – electron* bebas yang siap mengalir diujung – ujung terminal sel surya. Kemudian bila beban seperti lampu dipasang diantara terminal negative dan positif dari sel surya maka *electron* akan mengalir sebagai arus listrik searah yang dapat menghidupkan lampu tersebut. Energi matahari tersedia terus – menerus, maka arus listrik akan dialirkan ke beban terus – menerus. Semakin besar *radiasi* matahari yang mengenai sel surya, maka semakin besar pula arus yang dihasilkan oleh sel surya tersebut.

Sel surya akan selalu memproduksi energi listrik bila disinari oleh matahari, oleh itu karena sel surya tidak akan habis/ rusak dalam membangkitkan energi listrik.

Biasanya kerusakan terjadi karena sel tersebut pecah/ karena faktor lain, sehingga bila sel surya dilindungi dengan baik maka usianya bisa mencapai duapuluh tahun.

Modul *fotovoltaik* yang digunakan adalah jenis *silicon kristal*. Dimana jenis *silicon kristal* ini sendiri dibagi menjadi dua yaitu, bentuk *kristal polisilikon (polikristal)* dan kristal tunggal *silicon(monosilikon)*. Selain jenis *silicon kristal* tersebut kini telah dikembangkan juga jenis lain seperti *Gallium Arsenide, Amorphous Silikon, Copper Indium Diselenide* dan lain – lain.

Untuk mendapatkan keluaran energi listrik yang maksimum maka permukaan modul *fotovoltaik* harus selalu mengarah ke matahari. Karena matahari mempunyai lintasan dengan sudut tertentu, maka diperlukan suatu alat yang dapat mengikuti gerak matahari.

Selain pengaruh arah dari modul *fotovoltaik*, temperature juga dapat mempengaruhi energi listrik yang dihasilkan, semakin tinggi temperature modul *fotovoltaik* jenis silicon kristal maka akan semakin berkurang tegangan yang dihasilkannya yaitu sebesar 0,04V sampai 0,10V per °C. oleh karena itu dalam pemasangan *fotovoltaik* diusahakan adanya sirkulasi udara dibawah modul *fotovoltaik*. Hal ini dilakukan untuk menghindasri terjadinya akumulasi panas dari bagian bawah modul *fotovoltaik*.

Spesifikasi modul fotovoltaik yang digunakan:

- Tegangan nominal($V_{nom}$) lebih dari 12V.
- Tegangan terbuka ($V_{oc}$) lebih dari 18V.
- Arus pada daya puncak mencapai 3A dengan toleransi 10%

- Temperature sel maksimum 42°C

## 2.3. Baterai Penyimpanan

Baterai pada system ini yang lebih tepat berfungsi sebagai penyimpan energi listrik secara kimiawi di siang hari dan berfungsi sebagai catu daya dimalam hari. Baterai terdiri dari sejumlah sel *elektrokimia* yang mempunyai dua buah *elektroda* yang direndam dalam larutan *elektrolit* dan akan menghasilkan arus listrik bila ada beban diantara kedua *elektroda.*

### 2.3.1. *Accumulator* (Baterai *sel timbal – asam*)

*Akumulator* atau *Accu* adalah salah satu komponen sumber arus arus searah. *Akumulator* termasuk elemen elektrokimia yang dapat memperbaharui bahan pereaksinya setelah dialiri arus dari sumber lain yang arahnya berlawanan dengan arus yang dihasilkan elemen tersebut.

Yang dimaksud dengan elemen *elektrokimia* adalah system sumber arus yang pada dasarnya mengubah energi kimia menjadi energi listrik, didalam sumber ini terjadi reaksi *oksidasi reduksi* sehingga menimbulkan *electron* bebas yang dapat terus menerus mengalir selama jangka waktu tertentu jika kutub – kutub sumber ini berada dalam keadaan tertutup.


Gambar 2.2. Bentuk Fisik A*kumulator*[11]

Pada *akumulator* digunakan larutan $H_2SO_4$ sebagai *elektrolit*, sebagai *elektroda* positif *(anode)* digunakan $PbO_2$ dan *elektroda* negative *(katode)* digunakan Pb. Sewaktu baterai diisi *(charged)*, $PbO_2$ akan berkumpul pada *anode* , Pb berkumpul pada *katode* dan akan mengakibatkan jumlah dari asam *sulfat* relative bertambah sehingga bila diukur berat jenisnya atau *specific grafity (SG)* nya akan lebih besar dari satu. Sewaktu terjadi pengisian berlebih *(over charged)* dapat terbentuk gas *hydrogen* dan gas *oksigen* yang cukup berbahaya. Pada saat dibebani atau pada proses pengeluaran *(discharged)*, akan terbentuk $PbSO_4$ yang berkumpul di *anode* dan di *katode*, dan jumlah asam sulfat akan berkurang sedangkan jumlah air dalam elektrolit akan bertambah sehingga bila diukur harga *SG*- nya akan mendekati satu.

### 2.3.2 Karakteristik Akumulator

Akumulator mempunyai elemen yang disebut sebagai sel. Setiap sel dalam baterai ini menghasilkan tegangan diantara *anode* dan *katode* sebesar 2V, sehingga

untuk menghasilkan tegangan 12V dibutuhkan 6 buah sel baterai yang dihubungkan secara seri. Sel ini dapat digabungkan atau dikelompokkan secara:

a. Seri

Dengan menghubungkan sel *akumulator* secara seri akan diperoleh tegangan *output* lebih besar dengan arus tetap.

b. Paralel

Dengan menghubungkan sel *akumulator* secara parallel akan diperoleh arus yang lebih besar dengan tegangan tetap.

c. Seri paralel

Dengan menghubungkan sel *akumulator* secara seri dan paralel maka akan diperoleh tegangan dan arus *output* yang lebih besar.

### 2.3. 3 Kapasitas dan Rating Arus

*Akumulator* mempunyai rating dalam arti untuk mengetahui berapa besar arus *discharge* yang bisa dikeluarkan secara berkelanjutan selama selang waktu tertentu, dengan tegangan *output* tetap dipertahankan diatas level *minimumnya.* Kapasitas *akumulator* dinyatakan dalam Ah *(ampere Hour).* Sehingga untuk pemakaian sebentar arus yang diberikan adalah kecil. Untuk mencegah jangan sampai *akumulator* rusak karena panas *(over charge),* maka harus diketahui rating arus *maksimum*nya. Persamaan umum dinyatakan dalam:

$$C = A \times h$$

Dimana: C = kapasitas akumulator (*ampere hour*)

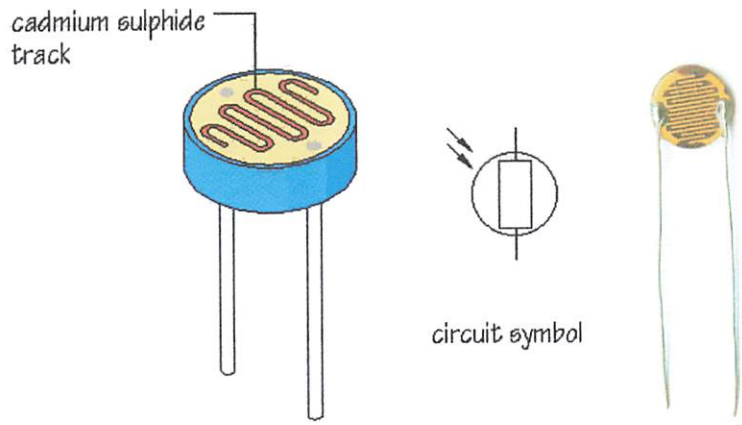
A = *Ampere*

H = *Hour* (jam)

Muatan *akumulator* dalam kondisi 100% bila tegangan terminalnya dalam kondisi terbuka sebesar 12,65V, sedangkan muatan akumulator dalam kondisi 0% *(discharge)* bila tegangan terminalnya 11,89V atau dibawahnya.

## 2.4. LDR (*Light Dependent Resistor*)

LDR atau *Light Dependent Resistor* adalah salah satu jenis resistor yang nilai hambatannya dipengaruhi oleh cahaya yang diterima olehnya. LDR dibuat dari *Cadmium Sulfida* yang peka terhadap cahaya. Seperti yang telah diketahui bahwa cahaya memiliki dua sifat yang berbeda yaitu sebagai gelombang *elektromagnetik* dan *foton/partikel* energi (*dualisme* cahaya). Saat cahaya menerangi LDR, foton akan menabrak ikatan *Cadmium Sulfida* dan melepaskan elektron. Semakin besar intensitas cahaya yang datang, semakin banyak elektron yang terlepas dari ikatan. Sehingga hambatan LDR akan turun saat cahaya meneranginya.




Gambar 2.3. Simbol LDR dan Gambar Fisik LDR[10]

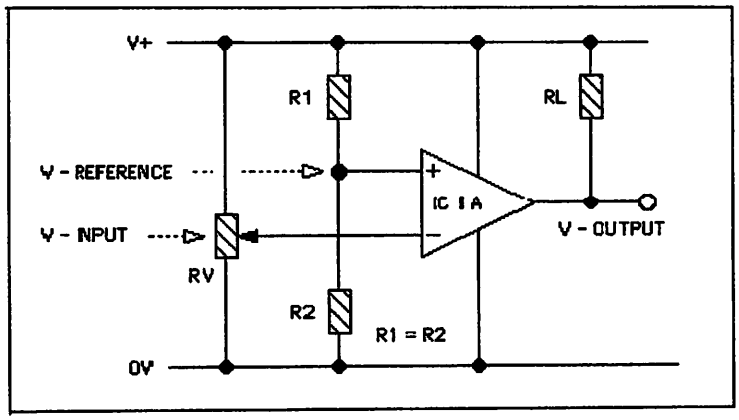
LDR akan mempunyai hambatan yang sangat besar saat tak ada cahaya yang mengenainya (gelap). Dalam kondisi ini hambatan LDR, mampu mencapai 1 M ohm. Akan tetapi saat terkena sinar, hambatan LDR akan turun secara drastis hingga nilai beberapa puluh ohm saja. Dalam aplikasi, dianjurkan untuk mengukur nilai Rmax dan Rmin dari LDR. Pengukuran Rmax dilakukan saat gelap ("agak gelap") dan pengukuran Rmin dilakukan saat terang.

### 2.4.1 *Komparator*

*Komparator* merupakan rangkaian *elektronik* yang akan membandingkan suatu *input* dengan referensi tertentu untuk menghasilkan *output* berupa dua nilai *(high dan low).* Suatu *komparator* mempunyai dua masukan yang terdiri dari tegangan *acuan (Vreference)* dan tegangan masukan *(Vinput)* serta satu tegangan *ouput (Voutput).*

Dalam operasinya, *komparator* akan mempunyai sebuah keluaran konstan yang bernilai "*low*" saat *Vinput* < *Vreferensi* dan "*high*" saat *Vinput* > *Vreferensi* (atau sebaliknya). Nilai dari "*low*" dan "*high*" tersebut akan ditentukan oleh desain dari *komparator* itu sendiri. Keadaan output ini disebut sebagai karakteristik *output komparator.*

Gambar 2-4a menunjukkan sebuah *komparator* sederhana, terdapat *Vreferensi* yang merupakan hasil bagi tegangan dari tegangan sumber, sehingga *Vreferensi* akan bernilai separuh tegangan sumber. Sedangkan tegangan input divariasikan dari 0 V hingga Vsumber.




Gambar 2.4. Komparator Untai sederhana. [10]

Jelas bahwa masukkan dari *komparator* dibandingkan dengan suatu nilai acuan tertentu *(Vreferensi)* keluaran dan didigitalkan menurut dua nilai kemungkinan yaitu: nilai "0" saat *Voutput low* dan nilai "1" saat *Voutput high*. Dengan kata lain, *komparator* bertindak sebagai pengubah analog ke digital 1 bit. Tegangan dengan logika "0" atau "1" ini, tentu saja dapat dilpertukarkan dengan rangkaian digital seperti *IC TTL, ECL* ataupun *CMOS*.

## 2.5. Motor Penggerak

Yang dimaksud mesin penggerak adalah alat yang digunakan untuk mengoptimalkan gerakan modul panel surya. Dalam hal ini mesin penggerak yang digunakan adalah mesin penggerak elektrik (motor). Motor disini berfungsi untuk memutar modul panel surya sehingga modul panel surya dapat mengikuti posisi matahari untuk mendapatkan intensitas cahaya maksimum.

### 2.5.1. Pengertian Motor Arus Searah

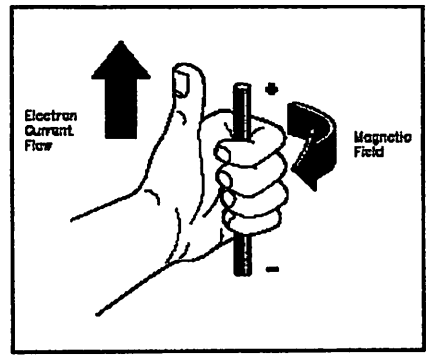
motor arus searah (DC) adalah suatu mesin yang berfungsi mengubah tenaga listrik arus searah menjadi tenaga mekanik dimana tenaga gerak berupa putaran *rotor*.

Dalam kehidupan sehari – hari motor arus searah sering dijumpai, sebagai contoh adalah motor yang dipasang untuk *starter* mobil, mainan anak, pada *tape recorder* dan lain – lain. Sedangkan pada industri, motor DC dapat dijumpai pada *elevator, conveyor* dan lain – lain.

Gambar 2.5. Bentuk Fisik Motor DC dalam Berbagai Ukuran[12]

### 2.5.2. Prinsip Dasar Motor Arus Searah

Prinsip dasar motor arus searah adalah kalau sebuah kawat berarus diletakkan antara kutub magnet (U.S), maka pada kawat tersebut akan bekerja suatu gaya yang akan menggerakkan kawat tersebut. Arah gerak dari kawat tersebut dapat ditentukan dengan "kaidah tangan kiri" yang berbunyi sebagai berikut:"apabila tangan kiri dibiarkan terbuka dan diletakkan diantara kutub utara dan kutub selatan, sehingga garis – garis gaya yang keluar dari kutub utara menembus telapak tangan kiri dan arus didalam kawat mengalir searah dengan keempat jari, maka kawat tersebut akan mendapat gaya yang jatuhnya sesuai dengan arah ibu jari".




Gambar 2.6. Kaidah Tangan Kiri[12]

Adapun besarnya gaya yang bekerja pada kawat tersebut dapat dirumuskan dengan:

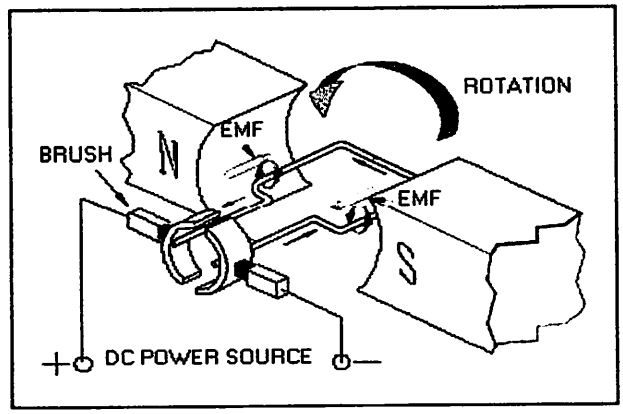
$$F = B.L.I \text{ } Newton$$

Dimana:

B = kerapatan *fluks* magnet (*weber*)

L = panjang penghantar (meter)

I = arus listrik (*ampere*)




Gambar 2.7. Konstruksi Dasar Motor DC[12]

Jika sebuah lilitan terletak dalam magnet yang *homogen*, maka kedua sisi belitan tersebut mempunyai arus yang daerahnya berlawanan.

Pada motor arus searah (DC) kumparan pada *rotor*nya tidak satu, tapi terdiri dari kumparan dan *komutator* yang banyak dengan maksud untuk mendapatkan *torsi* yang kuat dan terus menerus.

### 2.5.3. Jenis – jenis Motor DC

Berdasarkan sumber arus penguat magnetnya, motor DC dibedakan menjadi dua, yaitu:

1. Motor arus searah penguatan terpisah (jika arus penguat magnet diperoleh dari sumber arus searah diluar motor tersebut).
2. Motor arus searah dengan penguat sendiri (jika arus penguat magnet diperoleh dari motor itu sendiri).

Berdasarkan hubungan lilitan penguat magnet terhadap lilitan jangkar, motor arus searah dibedakan menjadi:

1. Motor Shunt

   Motor ini mempunyai kecepatan hampir konstan, motor ini punya putaran yang hampir *konstan* walaupun terjadi perubahan beban.

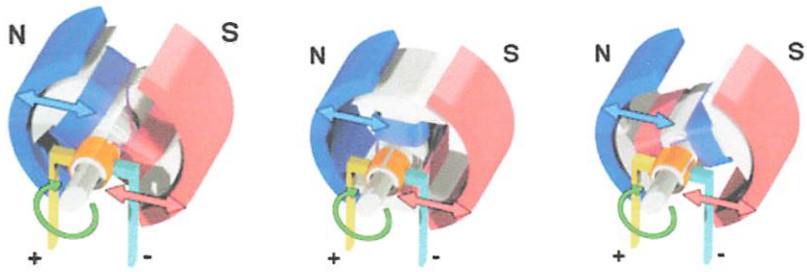
2. Motor Seri

   Merupakan motor arus searah yang mempunyai kecepatan putar yang tidak konstan, jika beban tinggi maka putaran akan melambat dan sebaliknya jika putaran rendah maka putaran akan cepat.

3. Motor Kompon

   Motor ini mempunyai sifat seperti motor seri dan shunt, tergantung lilitan mana yang kuat ( kumparan *seri/ shunt*).

### 2.5.4. Cara Memutar Balik Arah Putaran Motor DC




Gambar 2.8. Arah Putaran Motor DC[12]

Untuk membalik arah putaran motor DC, dapat dilakukan dengan dengan 2 cara, yaitu:

1. Membalik arah arus jangkar, sedangkan arah arus penguat tetap.
2. Membalik arah arus penguat, sedangkan arah arus jangkar tetap.

Jika keduanya dibalik ( arah arus jangkar dan arus penguat) maka arah putaran motor akan tetap (tidak membalik).

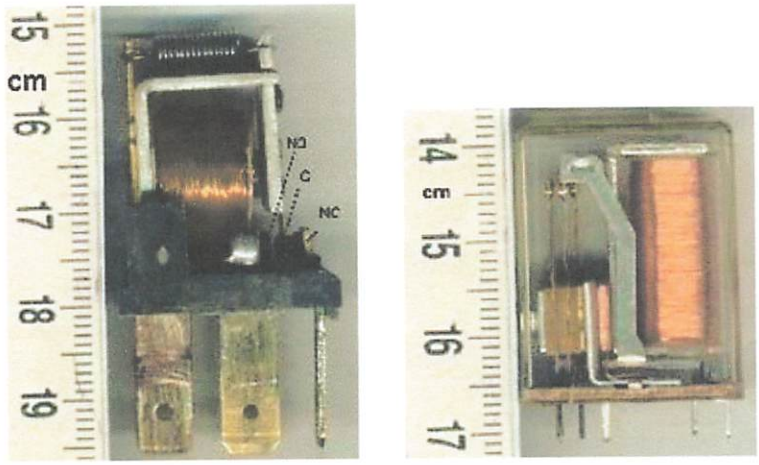
## 2.6. *Relay*

*Relay* merupakan salah satu jenis *saklar magnetic* yang dapat memutuskan atau menghubungkan kontak – kontak dari jarak jauh dengan arus yang kita alirkan

kekumparan (inti). Sebuah *relay* terdiri dari satu kumparan dan inti, yang mana bila dialiri arus kumparan tersebut akan menjadi magnet dan menutup atau membuka kontak. Keuntungan *relay* adalah dapat menghubungkan daya yang besar dengan memberi daya yang kecil pada kumparannya.

*Relay* digolongkan berdasarkan arusnya menjadi 2, yaitu:

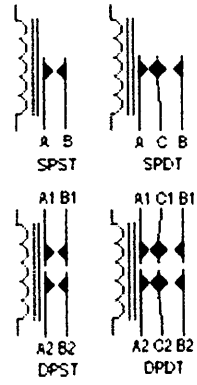
1. *Relay* arus searah *( DC Relays*)
2. *Relay* arus bolak – balik *(AC Relays*)




Gambar 2.9.Bentuk Fisik R*elay* [14]

*Relay* terdiri dari 4 jenis, yaitu:

1. DPDT *(Double – Pole, Double – Throw*)
2. SPDT (*Single – Pole, Double – Throw*)
3. DPST (*Double – Pole, Single – Throw*)
4. SPST (*Single – Pole, Single – Pole)*




Gambar 2.10. Jenis – jenis R*elay*[14]

*Relay* merupakan suatu alat untuk menghubungkan atau memutuskan kontak antara komponen satu dengan yang lain. Dalam memutus atau menghubungkan kontak digerakkan oleh *fluksi* yang timbul akibat adanya magnet listrik. Jadi fluksi inilah yang menghubungkan atau memutuskan kontak dan antara kumparan dengan bagian saklar tidak ada hubungan listrik.

Ada beberapa jenis susunan kontak *relay* dimana semuanya terisolasi terhadap arus listrik yang ada didalam kumparan. Jenis susunan kontak sebagai berikut:

1. *Normally Open* ( normal membuka)

   Yaitu kontak – kontak tertutup pada saat kumparan relay dialiri arus listrik.

2. *Normally Close* ( normal tertutup)

   Yaitu kontak – kontak terbuka pada saat kumparan relay dialiri arus listrik.

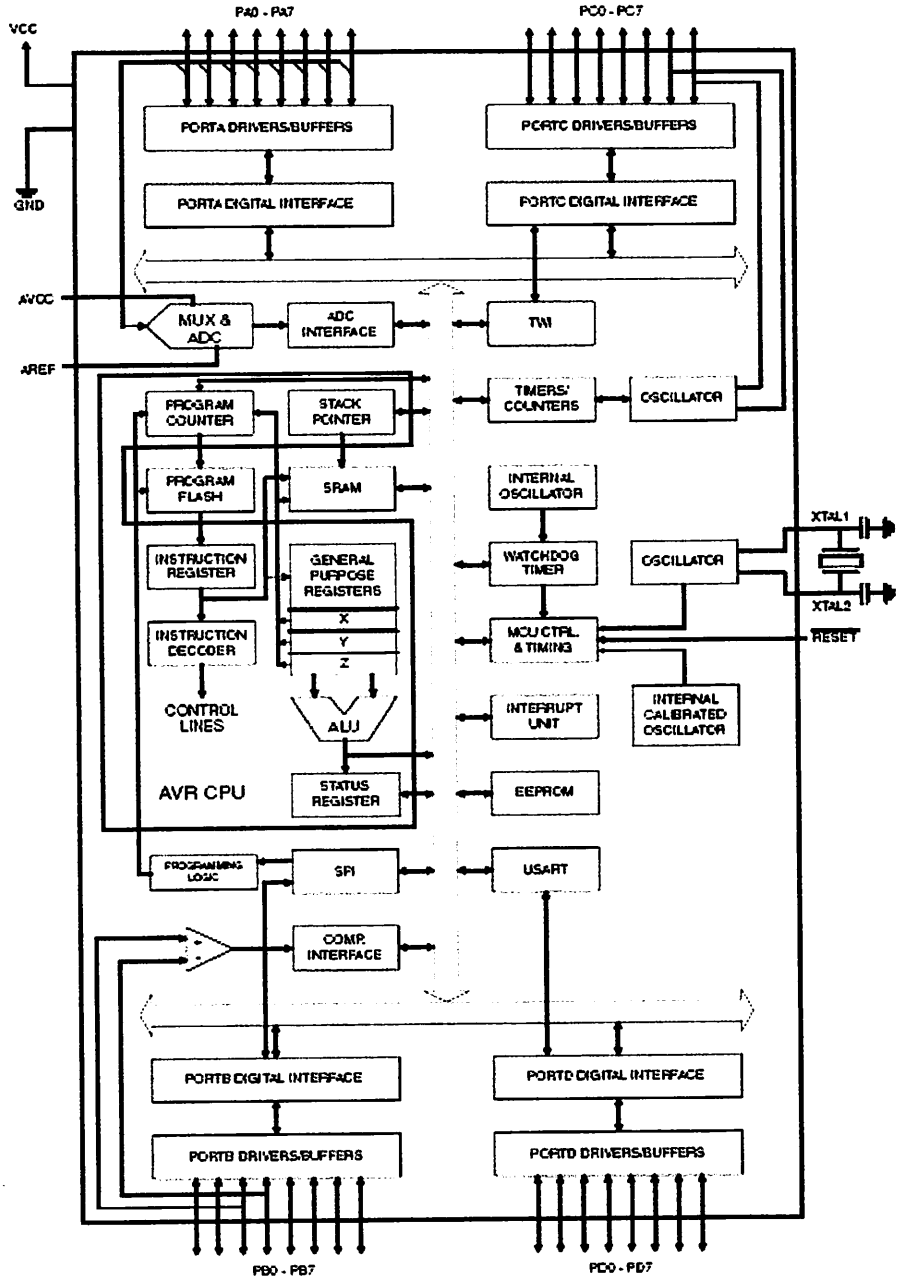
## 2.7. *Mikrokontroler* AT MEGA 16

### 2.7.1 Pendahuluan

*Mikrokontroler* AVR memiliki arsitektur RISC 8 bit, dimana semua instruksi dikemas dalam kode 16-bit (*16-bit word*) dan sebagian besar instruksi dieksekusi dalam 1 (satu) *siklus clock*, berbeda dengan instruksi MCS51 yang membutuhkan *12 siklus clock.* Tentu saja itu terjadi karena kedua jenis *mikrokontrol* tersebut memiliki arsitektur yang berbeda. AVR berteknologi RISC *(Reduced Instruction Set Computing*). Secara umum , AVR dapat dikelompokkan menjadi 4 kelas, yaitu *ATtiny,* keluarga AT90Sxx, keluarga ATMega, dan AT86RFxx. Pada dasarnya yang membedakan masing-masing kelas adalah *memori*, *peripheral*, dan fungsinya. Dari segi arsitektur dan instruksi yang digunakan, mereka bisa dikatakan hampir sama.

Oleh karena itu, dipergunakan salah satu AVR produk Atmel, yaitu ATMega 16, buku pembelajaran mikrokontroler dengan pemahaman pemrograman menggunakan simulasi yang terdapat pada *software BASCOM* dan juga praktek langsung hardware. Selain karena mudah didapatkan dan murah, ATMega16 juga memiliki fasilitas yang lengkap.

## 2.7.2 Arsitektur ATMega16




Gambar 2.11. Blok Diagram Fungsional ATMega 16[16]

Dari gambar tersebut dapat dilihat bahwa ATMega16 memiliki bagian sebagai berikut :

1. Saluran I/O sebanyak 32 buah, yaitu *Port* A, *Port* B, *Port* C, dan *Port* D.
2. ADC 10 bit sebanyak 8 saluran.
3. Tiga buah *Timer/Counter* dengan kemampuan pembandingan.
4. CPU yang terdiri atas 32 buah register.
5. *Watchdog Timer* dengan osilator internal.
6. SRAM sebesar 1 Kbyte.
7. *Memori Flash* sebesar 16 kb dengan kemampuan *Read While Write*.
8. *Port* antarmuka SPI.
9. EEPROM sebesar 512 byte yang dapat diprogram saat operasi.
10. Antarmuka komparator analog.
11. Port USART untuk komunikasi serial.

### 2.7.3. Fitur ATMega16

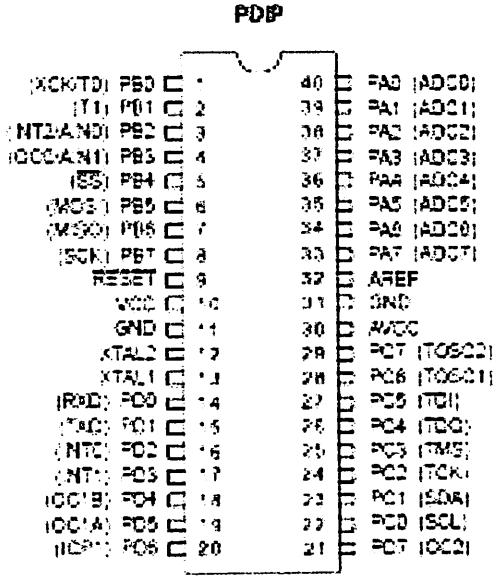
Kapabilitas detail dari ATMega16 adalah sebagai berikut :

1. Sistem mikroprosesor 8 bit berbasis *RISC* dengan kecepatan maksimal 16 MHz.
2. Kapabilitas memori *flash* 16 KB, *SRAM* sebesar 1Kbyte, dan *EEPROM* (*Electrically Erasable Programmable Read Only Memory*) sebesar 512 byte.
3. *ADC* internal dengan fidelitas 10 bit sebanyak 8 *channel*.
4. Enam pilihan mode *sleep* menghemat penggunaan daya listrik.

### 2.7.4 Konfigurasi Pin ATMega16

Konfigurasi pin ATMega16 bisa dilihat pada gambar 2-13, Dari gambar tersebut dapat dijelaskan secara fungsional konfigurasi pin ATMega16 sebagai berikut :

1. VCC merupakan pin yang berfungsi sebagai pin masukan catu daya.
2. GND merupakan pin *ground.*
3. Port A (PA0..PA7) merupakan pin I/O dua arah dan pin masukan ADC.
4. Port B (PB0..PB7) merupakan pin I/O dua arah dan pin fungsi khusus, yaitu Timer/Counter, komparator analog, dan SPI.
5. Port C (PC0..PC7) merupakan pin I/O dua arah dan pin fungsi khusus, yaitu TWI, komparator analog, dan *Timer Oscilator.*
6. Port D (PD0..PD7) merupakan pin I/O dua arah dan pin fungsi khusus, yaitu komparator analog, interupsi eksternal, dan komunikasi serial.
7. RESET merupakan pin yang digunakan utuk me-reset mikrokontroler.
8. XTAL1 dan XTAL2 merupakan pin masukan *clock* eksternal.
9. AVCC merupakan pin masukan tegangan untuk ADC.
10. AREF merupakan pin masukan tegangan referensi ADC.




Gambar 2.12. Pin ATMega16[16]

### 2.7.5 Peta Memori

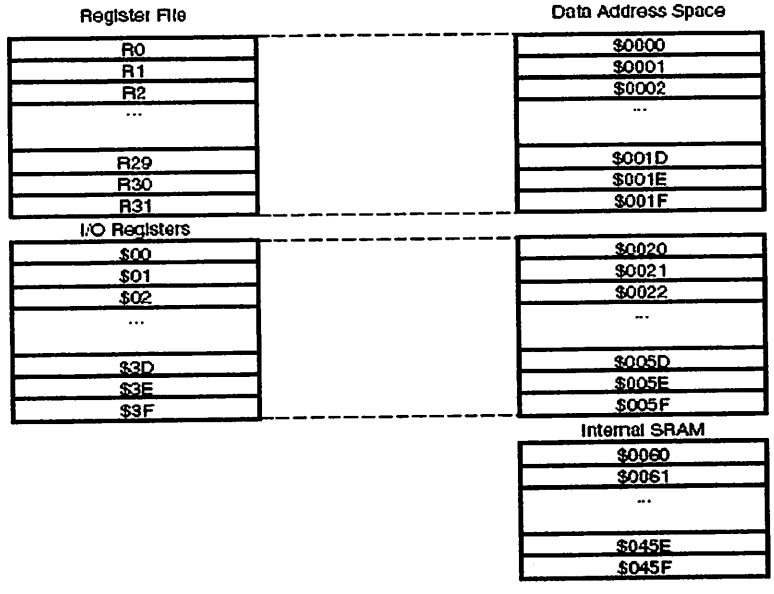
AVR ATMega16 memiliki ruang pengamatan *memori data* dan *memori program* yang terpisah.

Memori data terbagi menjadi 3 bagian, yaitu 32 buah *register* umum, 64 buah *register I/O*, dan 512 *byte* SRAM *Internal*.

*Register* keperluan umum menempati *space* data pada alamat terbawah, yaitu $00 sampai $1F. Sementara itu, register khusus untuk menangani *I/O* dan control terhadap *mikrokontroler* menempati 64 alamat berikutnya, yaitu mulai dari $20 hingga $5F. *Register* tersebut merupakan *register* yang khusus digunakan untuk mengatur fungsi terhadap berbagai *peripheral mikrokontroler*, seperti control *register, timer/counter*, fungsi-fungsi I/O, dan sebagainya. *Register* khusus alamat

memori secara lengkap dapat dilihat pada Tabel 2-1. Alamat memori berikutnya digunakan untuk SRAM 512 byte, yaitu pada lokasi $60 sampai dengan $25F. Konfigurasi memori data ditunjukkan pada gambar dibawah ini.

Tabel 2.1. Konfigurasi Memori Data AVR ATmega16[16]




Memori program yang terletak dalam *Flash PEROM* tersusun dalam word atau 2 byte karena setiap instruksi memiliki lebar 16-bit atau 32-bit. AVR ATMega16memiliki 4K*Byte*X16-bit *Flash PEROM* dengan alamat mulai dari $000 sampai $FFF. AVR tersebut memiliki 12-bit *Program Counter* (PC) sehingga mampu mengamati isi *Flash.*

Selain itu, AVR ATMega16 juga memiliki memori data berupa EEPROM 8-bit sebanyak 512 *byte*. Alamat EEPROM dimulai dari $000 sampai $1FF.

Tabel 2.2. Tabel Konfigurasi Pin I/O[16]

| DDxn | PORTxn | PUD (In SFIOR) | I/O | Pull-up | Comment |
|---|---|---|---|---|---|
| 0 | 0 | X | Input | No | Tri-state (Hi-Z) |
| 0 | 1 | 0 | Input | Yes | Pxn will source current if ext. pulled low. |
| 0 | 1 | 1 | Input | No | Tri-state (Hi-Z) |
| 1 | 0 | X | Output | No | Output Low (Sink) |
| 1 | 1 | X | Output | No | Output High (Source) |

### 2.7.6 Status Register (SREG)

Status Register adalah register berisi status yang dihasilkan pada setiap operasi yang dilakukan ketika suatu instruksi dieksekusi. SREG merupakan bagian dari inti CPU mikrokontroler.

a. Bit 7 – I : *Global Interrupt Enable*

Bit harus diset untuk meng-enable interupsi. Setelah itu, anda dapat mengaktifkan interupsi mana yang akan anda gunakan dengan cara meng-enable bit control register yang bersangkutan secara individu. Bit akan di-clear apabila terjadi suatu interupsi yang dipicu oleh hardware, dan bit tidak akan mengizinkan terjadinya interupsi, serta akan diset kembali oleh instruksi RETI.

b. Bit 6 – T : *Bit Copy Storage*

Instruksi BLD dan BST menggunakan bit-T sebagai sumber atau tujuan dalam operasi bit. Suatu bit dalam sebuah register GPR dapat disalin ke bit menggunakan instruksi BST, dan sebaliknya bit-T dapat disalin kembali ke suatu bit dalam register GPR menggunakan instruksi BLD.

c. Bit 5 – H : *Half Carry Flag*

d. Bit 4 – S : *Sign Bit*

Bit-S merupakan hasil operasi EOR antara flag-N (negatif) dan flag V (komplemen dua overflow).

e. Bit 3 – V : *Two's Complement Overflow Flag*

Bit berguna untuk mendukung operasi aritmatika.

f. Bit 2 – N : *Negative Flag*

Apabila suatu operasi menghasilkan bilangan negatif, maka flag-N akan diset.

g. Bit 1 – Z : *Zero Flag*

Bit akan diset bila hasil operasi yang diperoleh adalah nol

h. Bit 0 – C : *Carry Flag*

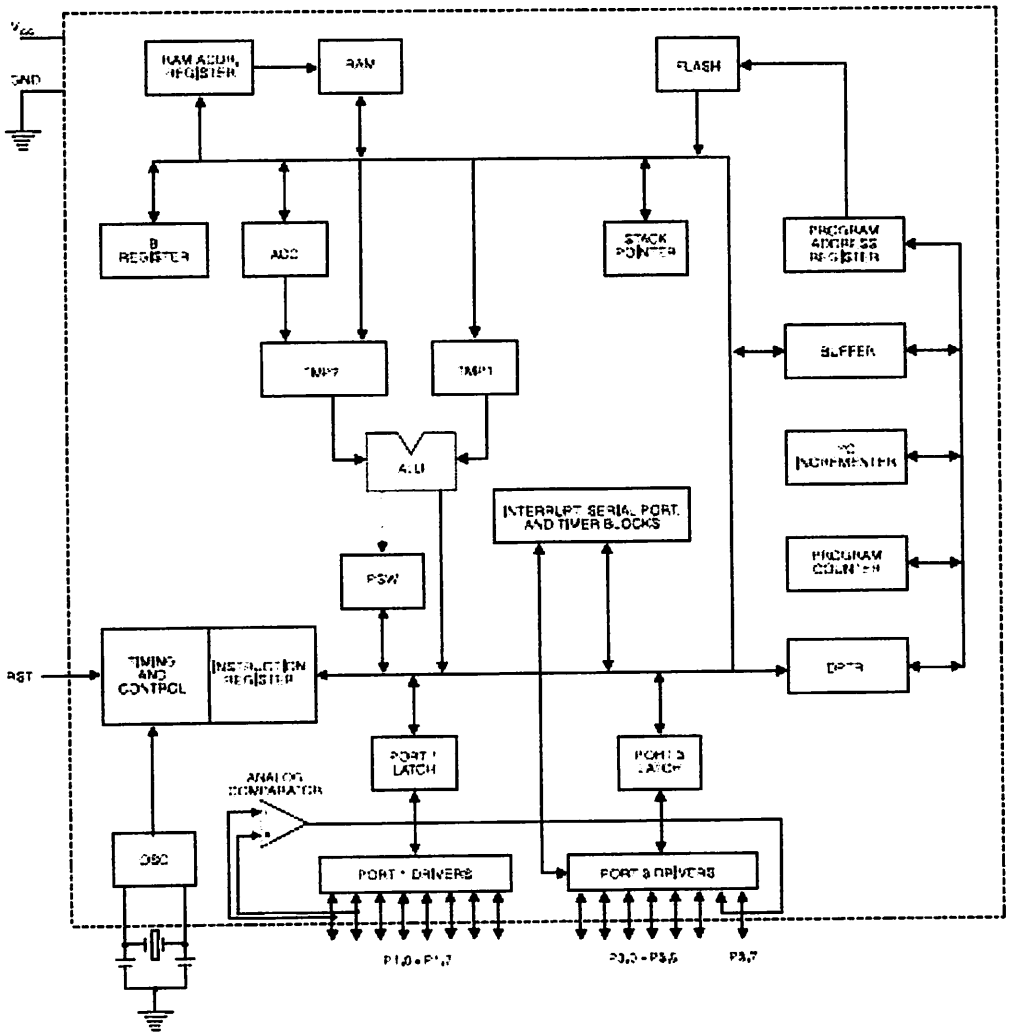
Apabila suatu operasi menghasilkan carry, maka bit akan diset.

## 2.8. *Mikrokontroler* AT89C2051

### 2.8.1. Pendahuluan

AT89C2051 merupakan mikro yang low – voltage, mempunyai 8bit CMOS dengan 2k bytes flash programmable dan erasable read only memory (PEROM), AT89C2051 mempunyai standar arsitektur yaitu 2k bytes flash, 128 bytes RAM, 15 jalur I/O, 2 timer/counter 16 bit, 5 vektor arsitektur 2 level interup, serial port full duplex, on chip komparator.

### 2.8.2 Arsitektur AT89C2051



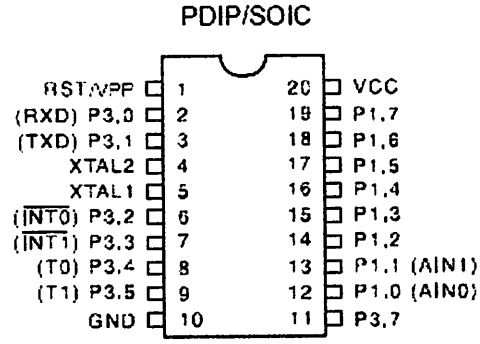

Gambar 2.13. Blok Diagram Fungsional AT89C2051[7]

Dari gambar tersebut dapat dilihat bahwa AT89C2051 memiliki bagian sebagai berikut:

1. 2K bytes reprogrammable flash memory.
2. beroperasi penuh pada frekuensi 0 Hz – 24 MHz.
3. 2 level program memory lock.

4. 128 x 8 – bit internal RAM.
5. 15 programable jalur I/O.
6. 2 timer/ counter 16 bit.
7. 6 interup.
8. serial UART channel.
9. on chip analog komparator.
10. low power idle dan mode power down.

### 2.8.3 konfigurasi AT89C2051




Gambar 2.14. Pin AT89C2051[7]

Konfigurasi pin AT89C2051 bisa dilihat pada gambar tersebut, dapat dijelaskan secara fungsional konfigurasi pin AT89C2051 sebagai berikut:

1. VCC merupakan pin masukan catu daya.
2. GND merupakan pin ground.
3. Port 1.0 – 1.7 merupakan pin bidirectional I / O 8 bit, juga menerima data kode dari Flash.

4. port 3 dibagi menjadi tiga bagian yaitu P3.0 – P3.5 mempunyai fungsi yang spesial, P3.6 merupakan input dan output on chip komparator dan bukan digunakan untuk pin I/O biasa. P3.7 pin bidirectional I/O, sedangkan P3.0 – P3.5 dapat dilihat pada tabel berikut:

Tabel 2.3. Tabel Konfigurasi P3.0 – P3.5[7]

| Port Pin | Alternate Functions |
|---|---|
| P3.0 | RXD (serial input port) |
| P3.1 | TXD (serial output port) |
| P3.2 | $\overline{\text{INT0}}$ (external interrupt 0) |
| P3.3 | $\overline{\text{INT1}}$ (external interrupt 1) |
| P3.4 | T0 (timer 0 external input) |
| P3.5 | T1 (timer 1 external input) |

5. RST merupakan pin yang digunakan utuk me-RESET mikrokontroler.
6. XTAL1 dan XTAL2 merupakan pin masukan *clock* eksternal.

### 2.8.4 SFR (Special Function Register)

Beberapa macam register fungsi khusus yang sering digunakan adalah sebagai berikut :

- *Accumulator* (ACC) merupakan register untuk penambahan dan pengurangan, perintah Mneumonic untuk mengakses akumulator disederhanakan sebagai A.
- *Register B* merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Stack Pointer* (SP) merupakan register 8 bit yang dapat diletakkan di alamat manapun pada RAM internal.

- *2 Data Pointer* (DPTR) terdiri atas dua register yaitu untuk byte tinggi (*data pointer high*, DPH) dan byte rendah (*data Pointer Low*, DPL) yang berfungsi untuk mengunci alamat 16 bit.
- *Port 1 dan 3* merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada port 1 dan 3. Masing-masing register ini dapat dialamati per-*byte* maupun per-bit.
- *Control Register* terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua register khusus yaitu register IP (*Interrupt Priority*) dan register IE *(Interupt Enable*). Untuk mengontrol pelayanan timer/counter terdapat register khusus yaitu register TCON (*Timer/Counter Control*) serta pelayanan port serial menggunakan register SCON (*Serial Port Control).*

Tabel 2.4. *Special Fuction Register* AT89C2051
SFR Map dan Reset Values[7]

**Table 1.** AT89C2051 SFR Map and Reset Values

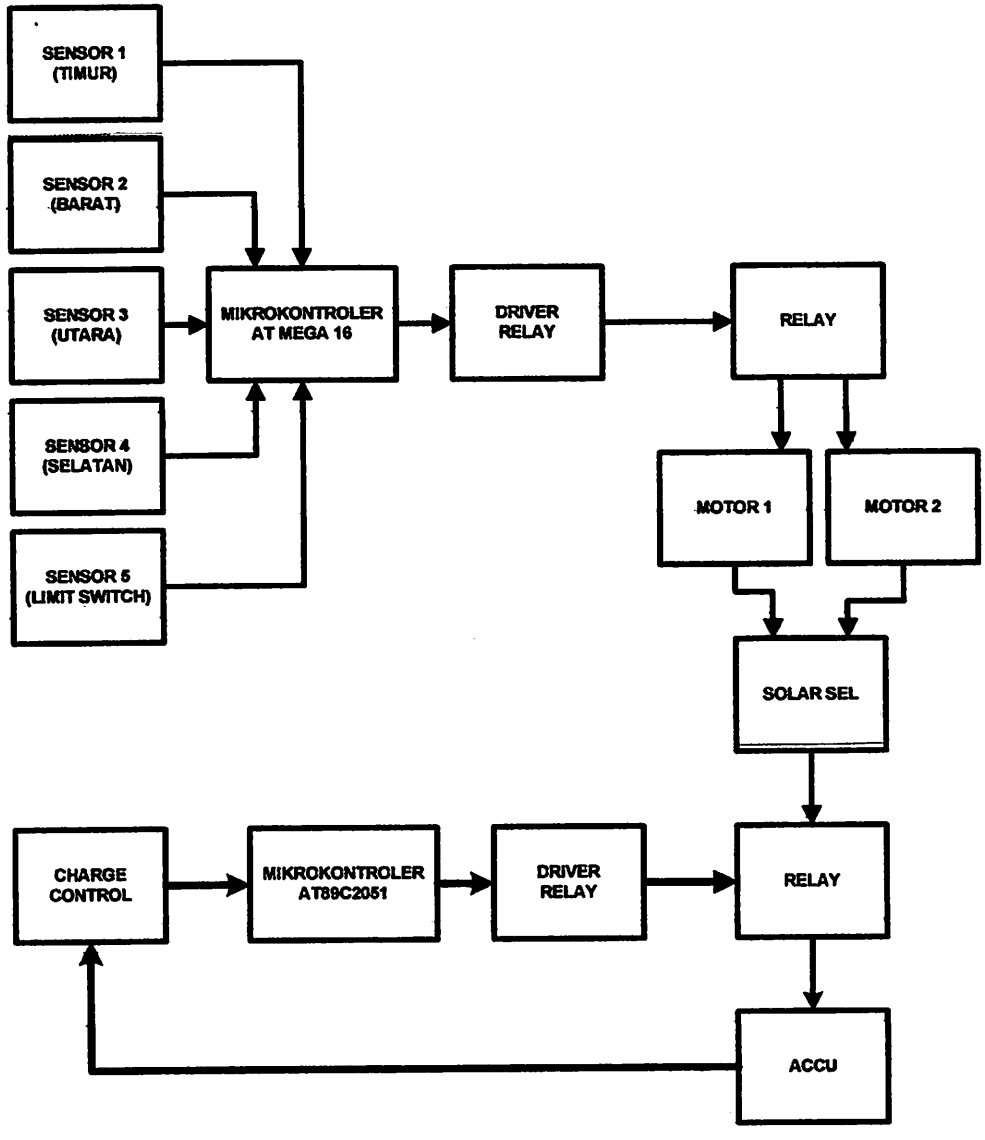
| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0F8H | | | | | | | | | 0FFH |
| 0F0H | B<br>00000000 | | | | | | | | 0F7H |
| 0E8H | | | | | | | | | 0EFH |
| 0E0H | ACC<br>00000000 | | | | | | | | 0E7H |
| 0D8H | | | | | | | | | 0DFH |
| 0D0H | PSW<br>00000000 | | | | | | | | 0D7H |
| 0C8H | | | | | | | | | 0CFH |
| 0C0H | | | | | | | | | 0C7H |
| 0B8H | IP<br>XXX00000 | | | | | | | | 0BFH |
| 0B0H | P3<br>11111111 | | | | | | | | 0B7H |
| 0A8H | IE<br>0XX00000 | | | | | | | | 0AFH |
| 0A0H | | | | | | | | | 0A7H |
| 98H | SCON<br>00000000 | SBUF<br>XXXXXXXX | | | | | | | 9FH |
| 90H | P1<br>11111111 | | | | | | | | 97H |
| 88H | TCON<br>00000000 | TMOD<br>00000000 | TL0<br>00000000 | TL1<br>00000000 | TH0<br>00000000 | TH1<br>00000000 | | | 8FH |
| 80H | | SP<br>00000111 | DPL<br>00000000 | DPH<br>00000000 | | | | PCON<br>0XXX0000 | 87H |

# BAB III

# PERENCANAAN DAN PEMBUATAN ALAT

## 3.1. Perancangan Perangkat Keras (Hardware)

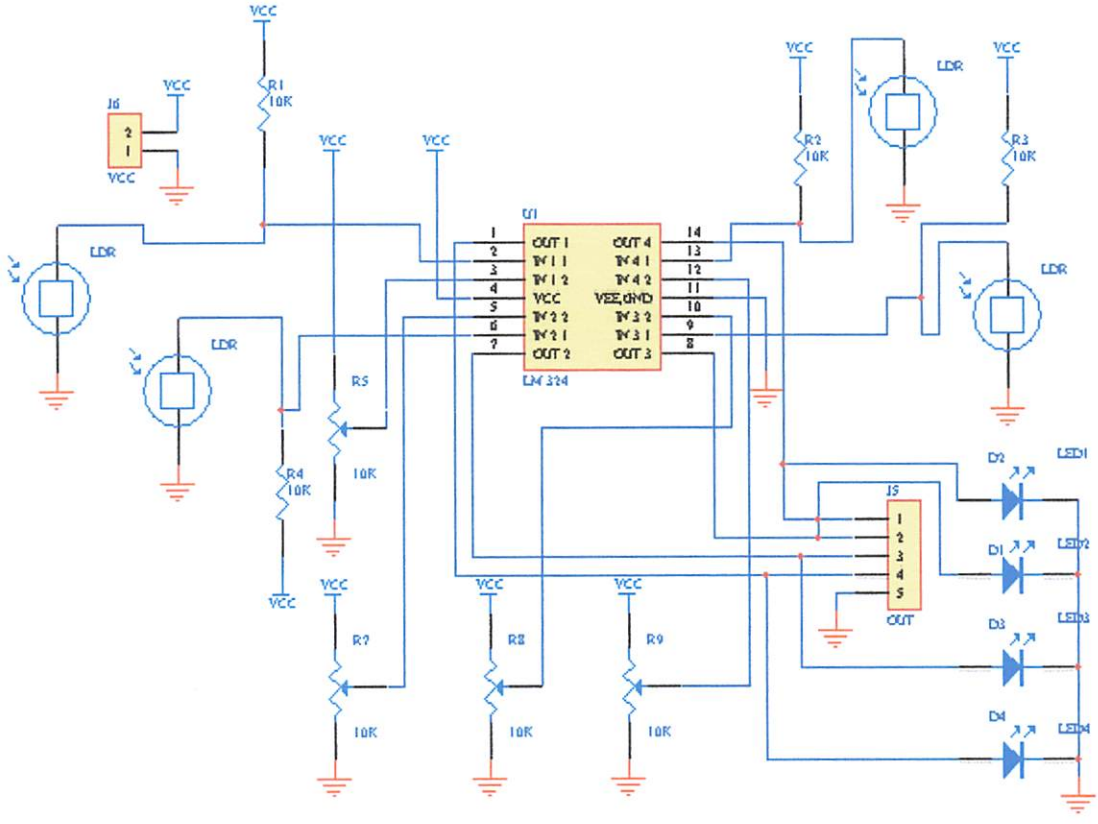
Blok diagram sistem dapat dilihat pada gambar dibawah ini:




Gambar 3.1. Diagram Blok Sistem

### 3.1.1. Rangkaian Sensor LDR

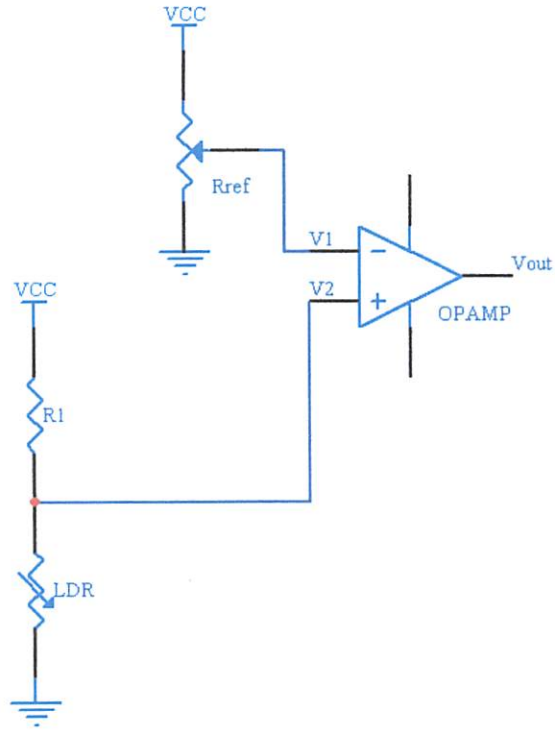
Disini digunakan sensor LDR untuk mengetahui arah matahari yaitu dengan cara mencari cahaya matahari, dimana semakin banyak terang cahaya matahari yang mengenai LDR maka hambatannya akan semakin kecil.




Gambar 3.2. Gambar Rangkaian Sensor

Karena pada rangkaian ini diperlukan sensor untuk mencari matahari maka digunakan LDR, juga digunakan op amp LM 324. Dimana jika LDR terkena cahaya maka akan terjadi perubahan tegangan pada LDR sehingga ada perbedaan antara Vcc 5 V dengan tegangan pada LDR , kemudian Voutput dari LDR dibandingkan dengan Vref, maka outputnya diperoleh logika "1 ". Apabila LDR tidak terkena cahaya atau

gelap maka ada perubahan tegangan dimana resistansinya dianggap tak hingga maka Vout pada LDR menjauhi 5V, kemudian Vout LDR dibandingkan dengan Vref , maka outputnya diperoleh logika"0".




Gambar 3.3. Gambar Rangkaian Komparator

Saat terang dianggap resistansi LDR = 20 Ω maka V2 = $\frac{RLDR}{R1 + RLDR} \bullet Vcc$

Maka V2 = $\frac{20}{10k + 20} \bullet 5V$

= 0.0099 V

Variabel Rref dianggap 50% (position) sehingga V1 = 2,5 V

Vout = (V1 – V2). Aol

= (2.5 – 0.0099).200000

= 2.4901 . 200000

= 498020 Volt

atau dapat dikatakan = -0.00 V Vcc – 2V

= 5 – 2 = 3 V

Saat gelap dianggap resistansi LDR = 1000000 Ω maka V2 = $\frac{RLDR}{R1 + RLDR} \bullet Vcc$

Maka V2 = $\frac{1000000}{10k + 1000000} \bullet 5V$

= 4.95 V

V1 = tetap 50%

= 2.5 V

Vout = (V1 – V2).Aol

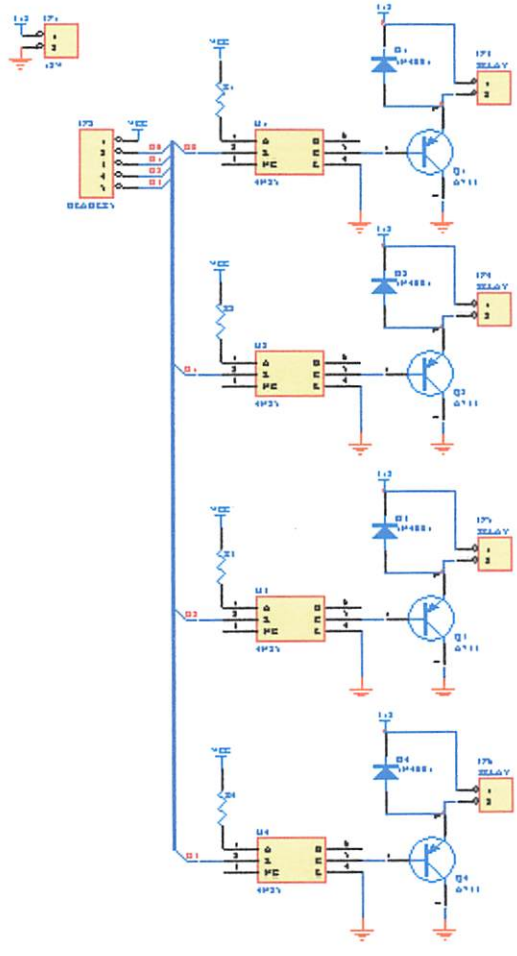
= (2.5 – 4.95).200000

= - 490000 V dibawah Vcc

=-Vsat = karena V- op amp = Ground maka Vout = Ground = 0 = - Vsat = 0 - 2

= - 2 V atau dapat dikatakan = - 0.00

### 3.1.2. Rangkaian Driver motor



Gambar 3.4. Gambar Rangkaian *Optocoupler*

Pada perancangan *driver* ini terdiri dari empat sebuah o*ptocoupler* dan 4 transistor A733. Pemasangan *optocoupler* berfungsi sebagai penahan *bouncing* yang muncul akibat kelebihan arus yang ditimbulkan oleh beban, sehingga dapat menyebabkan kerusakan fisik maupun nonfisik (*program*) pada mikrokontroler. Walaupun sebenarnya *bouncing* itu sendiri telah diantisipasi dengan memasang

sebuah diode yang terpasang paralel dengan *relay*nya sebelum masuk ke beban. Rangkaian ini terdiri dari *optocoupler* 4N25, transistor A733, Diode dan *relay*.

Cara kerja dari rangkaian diatas adalah untuk mengaktifkan *relay*, mikrokontroler akan mengeluarkan logika "0" pada port A.0 – A.3, dengan begitu akan ada arus yang mengalir akan membuat transistor NPN pada *optocoupler* menjadi saturasi. Dengan rangkaian seperti diatas, kolektor dari transistor pada *optocoupler* terhubung pada basis transistor A733 dan emitornya pada *ground*, maka ketika transistor pada *optocoupler* saturasi akan membuat transistor A733 juga mengalami saturasi.

*Relay* yang digunakan memiliki tegangan 12 volt dan hambatan 376 ohm,hfe A733 adalah 260 dan Vce sebesar 0.3 V maka arus yang mengaliri *relay* adalah :

$$I_E = \frac{V_{EE} - V_{CE}}{R_{RELAY}} = \frac{12V - 0.3}{376\Omega} = 0.031 \text{ A}$$

$$I_C = I_E - I_B \quad \text{.....(1.1)}$$

$$I_B = \frac{I_C}{hfe} \quad \text{.....(1.2)}$$

Dari persamaan 1.1 dan 1.2 didapatkan:

$$I_B = \frac{I_E}{hfe + 1}$$

$$I_B = \frac{0.031A}{260 + 1} = 0.12mA \quad \text{.....(1.3)}$$

Dari datasheet dapat diketahui arus kolektor maksimum yang dapat mengalir pada transistor pada *optocoupler* 4N25 adalah 150 mA, sedangkan dengan arus basis pada transistor A733 sebesar 0.12 mA masih dibawah arus maksimum yang dapat

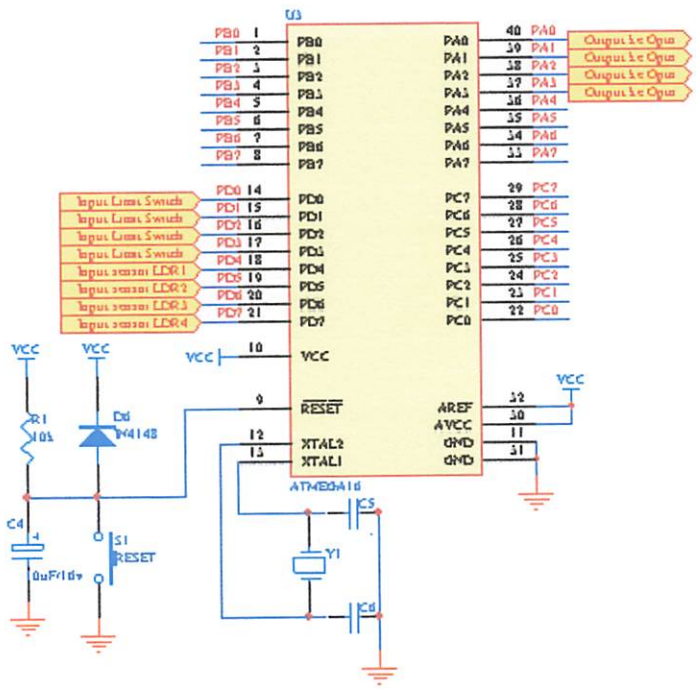
dilewatkan pada transistor *optocoupler* 4N25. Pada *optocoupler* 4N25 memiliki Vled = 3 volt dan Iled = 60 mA sehingga dapat dicari *resistor* yang harus dipakai:

$$R_1 = \frac{V_{CC} - V_{LED}}{I_{LED}} = \frac{5-3}{60mA} = 33.3\Omega$$

Karena besar hambatan dipasaran sebesar 33.3 ohm tidak ada maka dipakai hambatan sebesar 39 ohm.

Pada rangkaian opto ini menggunakan IC opto 4N25, apabila logika dari mikro "1", maka transistor opto tidak aktif sehingga tegangan pada relay tidak memperoleh referensi ground sehingga relay tidak aktif dan motor tidak berputar, apabila logika dari mikro "0", maka transistor opto aktif sehingga tegangan pada relay memperoleh referensi ground sehingga relay aktif dan motor berputar.

### 3.1.3. Perancangan minimum sistem ATMega 16



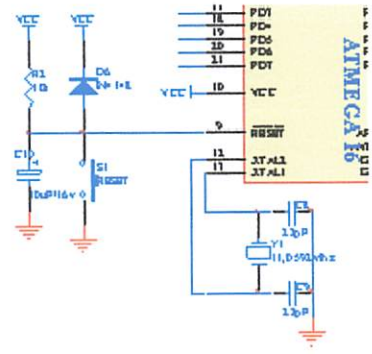

Gambar 3.5. Rangkaian Minimum Sistem ATMega 16[16]

Mikrokontroler yang digunakan adalah mikrokontroler keluarga AVR ATMega 16 yang mempunyai arsitektur RISC(*Reduce Instruction Set*). ATMega 16 mempunyai memory flash ROM sebesar 16KB, sehingga memungkinkan untuk mengaplikasikannya sebagai otak kontrol dari penjejak matahari. Data yang diperoleh dari detektor akan diolah dan dikeluarkan sebagai aplikasi dari gerakkan motor.

Alokasi penggunaan pin mikrokontroler :

- PD.4-PD.7 digunakan sebagai port input yang akan menerima sinyal digital dari rangkaian pengkondisi sinyal yang terhubung pada sensor.
- PD.0-PD.3 digunakan sebagai port input yang akan menerima sinyal digital dari limit Switch.
- PA.0 – PA.3 digunakan sebagai port output yang terhubung dengan *opto coupler*, yang menggerakkan motor.
- Pin no.9 ialah pin reset mikrokontroler ATMega 16, reset terjadi bila pin ini diberi logika *low* dengan level tegangan 0 volt selama 1,5 μs atau lebih.
- $X_1$ dan $X_2$ sebagai masukan dari rangkaian osilator kristal. Rangkaian osilator kristal terdiri atas osilator 12 MHz, kapasitor $C_1$ dan $C_2$ yang masing-masing bernilai 22 pF yang akan membangkitkan pulsa *clock* yang digunakan sebagai penggerak bagi sejumlah operasi internal CPU.

Perancangan rangkaian reset pada mikrokontroler ATMega 16 adalah dengan memberikan logika low pada pin reset mikrokontroler ATMega 16. Rangkaian reset ini diperoleh dari *application note AVR Design Consideration* dari ATMEL. Berikut ialah gambar rancangan rangkaian reset pada ATMega 16 :




Gambar 3.6. Rangkaian *Reset* pada ATMega16[16]

Osilator pada rangkaian minimum sistem ATMega 16 menggunakan kristal 12 MHz dan capasitor 22 pF. Nilai kapasitor ini diperoleh dari tabel datasheet tentang penggunaan kapasitor untuk rangkaian osilator / sistem clock pada ATMega 16. Penggunaan kristal 12 MHz ini bertujuan agar perhitungan bautrate tidak mengalami error yang disebabkan karena selisih perhitungan. Perhitungan bautrate pada ATMega 16 dengan menggunakan kristal 12 MHz :

Bautrate yang diinginkan ialah 115200 bps, maka nilai pada *UBRR(USART Baut Rate Register)* dapat ditentukan dengan perhitungan :

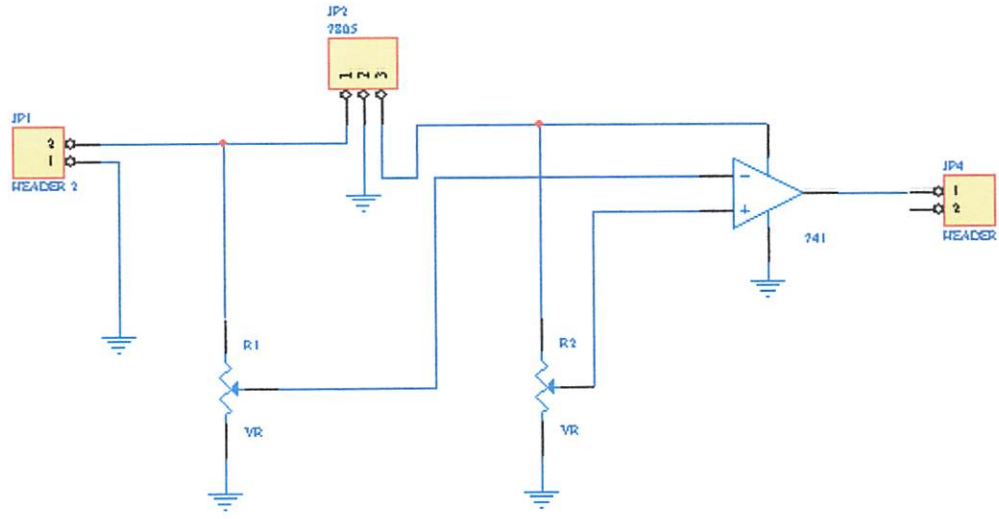
$$UBRR = \frac{fosc}{16.Baud} - 1$$

$$UBRR = \frac{12000000}{16.115200} - 1$$

$$UBRR = \frac{12000000}{1843200} - 1$$

$$UBRR = 6.5 - 1 = 5.5 = 5.5H$$

### 3.1.4. Perancangan Rangkaian *Charge Control*

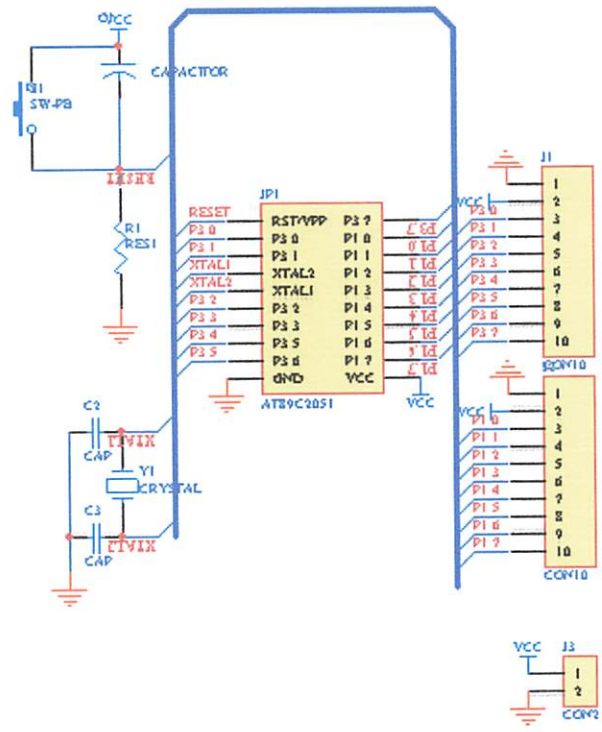



Gambar 3.7. Rangkaian *Charge Control*

Pada rangkaian *charge control* ini terdiri dari IC 7805 dan IC 741 sebagai komparator antara *charge control* dengan tegangan akumulator dan 2 VR yang masing – masing bernilai 10K, dimana digunakan sebagai Vref dan Vdari *accu* yang nantinya akan dicharge dari solar sel ke aki. Dimana cara kerja dari *charge control* ini adalah pada saat *accu* dalam keadaan drop dimana disini diset tegangan *accu* dalam keadaan drop adalah 10 V pada saat inilah *accu* membutuhkan charge dari sel surya maka relay akan terbuka dan akan men – *charge* aki sampai waktu yang telah diprogram pada mikrokontroler apabila waktu charge telah habis maka relay akan

menutup. Untuk menghindari adanya bouncing pada relay digunakan mikro AT89C2051 sebagai *timer*, *charge control* akan membandingkan tegangan referensi dengan tegangan *accu* secara terus menerus sampai tegangan didapatkan sama dengan tegangan *set point*, jadi *charge control* akan membandingkan terus apakah tegangan *accu* berbeda dengan tegangan referensi, jika sudah pada batas bawah maka *accu* akan men – *charge*, jika belum maka komparator akan membandingkan lagi.

### 3.1.5. Perancangan minimum sistem AT89C2051 untuk *Charge Control*




Gambar 3.8. Rangkaian Minimum Sistem AT89C2051

Pada rangkaian *charge control* digunakan *timer* untuk mengontrol *charge* solar sel ke *accu*, karena *charge control* tersebut memakai relay untuk memutus dan menyambungkan antara solar sel dengan *accu*, mikro ini digunakan sebagai timer

tersebut apabila tidak maka akan mengakibatkan *boucing* pada relay, karena itulah digunakan mikro untuk menghindari *bouncing* tersebut.

Alokasi penggunaan pin:

- P1.5 digunakan sebagai port input yang akan menerima sinyal digital dari rangkaian pengkondisi sinyal yang terhubung pada *charge control.*
- P1.7 digunakan sebagai port output yang akan masuk pada opto, kemudian memutus atau menyambungkan relay.
- Pin no.1 ialah pin reset mikrokontroler AT89C2051, reset terjadi bila pin ini diberi logika low dengan level tegangan 0 volt.
- $X_1$ dan $X_2$ sebagai masukan dari rangkaian osilator kristal. Rangkaian osilator kristal terdiri atas osilator 12 MHz, kapasitor $C_1$ dan $C_2$ yang masing-masing bernilai 30 pF yang akan membangkitkan pulsa *clock* yang digunakan sebagai penggerak bagi sejumlah operasi internal CPU.

AT89C2051 merupakan IC CMOS 8 – bit mikrokomputer dengan 2k bytes PEROM (*Programmable Erasable Read Only Memory*), 128 bytes RAM. Mikro ini nantinya hanya digunakan untuk timer dari charge control dalam pemutusan dan penyambungan relay. Mikro ini mempunyai rangkaian clock yang nantinya digunakan untuk timer. Rangkaian tersebut tersusun dari komponen-komponen 2 buah capasitor, 1 buah IC mikrokontroller, sebuah resistor dan sebuah kristal atau *resonator* keramik. Rangkaian capasitor dan kristal atau *resonator*

keramik digunakan sebagai rangkaian pembangkit *internal clock generator* yang terdapat pada AT89C2051. Nilai kapasitansi ditentukan sesuai dengan jenis oscilator yang digunakan, yaitu:

C1 dan C2 = 10pF – 30pF untuk kristal

C1 dan C2 = 10pF – 40pF untuk resonator keramik.

Karena dalam perancangan digunakan *oscilator* kristal maka nilai capasitor yang dipakai dalam perancangan adalah sebesar 10pF.

Mikrokontroller AT89C2051 mempunyai *frekwensi* maksimal 12 MHz, dimana 1 siklus mesin = 12 clock. Dalam rangkaian digunakan kristal dengan harga 12 MHz, maka program akan dijalankan pada setiap langkahnya selama 1μs. Siklus tersebut diambil berdasarkan ketentuan mikrokontroller AT89C2051 yaitu 12 *clock* = 1 siklus mesin, sedangkan *frekwensi* yang digunakan 12 MHz, maka waktu yang dipakai dalam setiap 1 siklus mesin adalah 1μs. Dengan demikian perhitungannya dapat dilihat sebagai berikut:

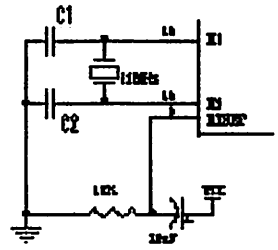
f = 12 MHz

$$T = \frac{1}{f}$$

$$T = \frac{1}{12 \times 10^6}$$

Karena 1 siklus mesin = 12T maka,

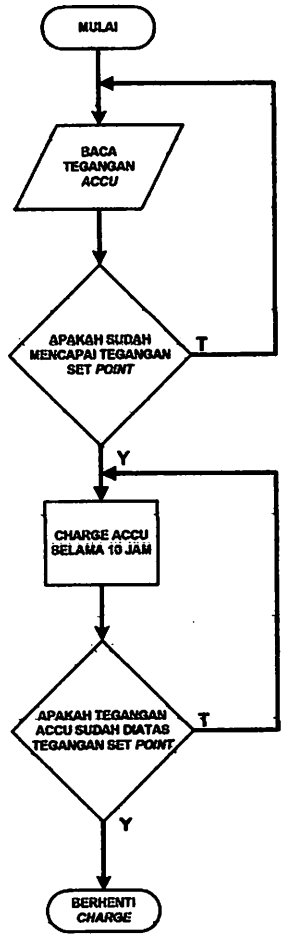
$$1 \text{ siklus mesin} = 12 \text{ x } \frac{1}{12 \times 10^6} = 1\mu s.$$



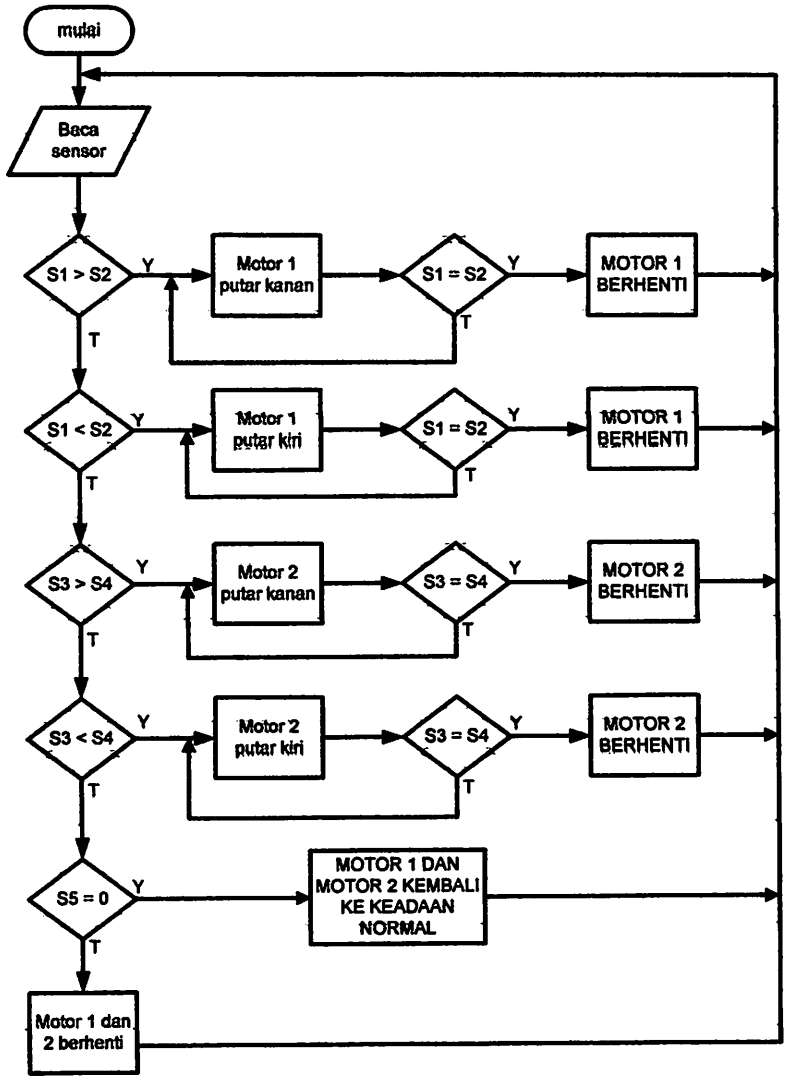

Gambar 3.9. Gambar Rangkaian Clock dan Reset AT89C2051

### 3.1.6. Diagram Alir Perancangan

*Flowchart* rangkaian sebagai berikut:




Gambar 3.10. Gambar *Flowchart Charge Control*




Gambar 3.11. Gambar *Flowchart* Kontrol Penjejak Matahari

# BAB IV

# PENGUJIAN ALAT

Dalam bab ini akan di bahas mengenai pengujian alat yang telah dibuat. Hal ini dapat dilakukan untuk mengetahui kekurangan kerja sistem yang telah dibuat, sehingga dapat diketahui apakah alat tersebut dapat bekerja sesuai dengan yang telah di rencanakan. Dalam rangka pengujian alat tersebut diuraikan percobaan yang telah di lakukan untuk mengetahui respon dari keseluruan alat yang telah dirancang.

## 4.1. Tujuan Pengujian

Tujuan pengujian yang dilakukan terhadap sistem aplikasi ini adalah sebagai berikut :

- Mengetahui unjuk kerja rangkaian sensor LDR (Light Dependent Resistor)
- Mengetahui unjuk kerja rangkaian driver motor DC.
- Mengetahui unjuk kerja rangkaian charge control.
- Mengetahui unjuk kerja rangkaian pengkondisi sinyal.
- Mengetahui hasil penerimaan tegangan oleh aki antara solar sel yang diam dengan yang bergerak.
- Mengetahui error dari kontrol alat.

## 4.2. Alat-alat untuk pengujian

Alat-alat yang digunakan dalam pengujian adalah :

1. Multimeter Digital
2. Power suplay +5 Volt dan +12 Volt

## 4.3. Pengujian dan Pengukuran

### 4.3.1. Sensor Cahaya

Pengujian ini dilakukan untuk mengetahui nilai resistansi sensor cahaya yang dibentuk dari 4 buah LDR yang akan berubah nilai resistansinya bila terkena cahaya.

Tabel 4.1. Tabel Hasil Perbandingan Resistansi LDR

| KONDISI | RESISTANSI (KOhm) |
|---|---|
| GELAP | 6.19 |
| TERANG | 0.3 |

### 4.3.2. Driver Motor DC

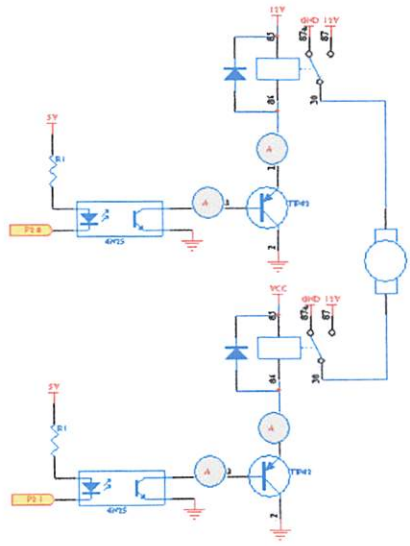
Pengujian rangkaian driver motor ini bertujuan untuk mengetahui apakah rangkaian ini dapat bekerja sebagaimana mestinya, yaitu dapat menggerakkan motor dengan arah yang bersesuaian dengan kombinasi masukannya.

Metode pengujian dilakukan seperti pada gambar. Pengujian dilakukan dengan memberi kombinasi logika pada inputan driver dan mengamati arah putaran motor DC pada keluarannya, serta mengukur tegangan pada keluaran driver.


Gambar 4.1. Metode Pengujian Rangkaian Driver Motor DC

#### 4.3.2.1 Langkah pengujian

1. Hubungkan alat dan bahan seperti rangkaian dibawah ini:

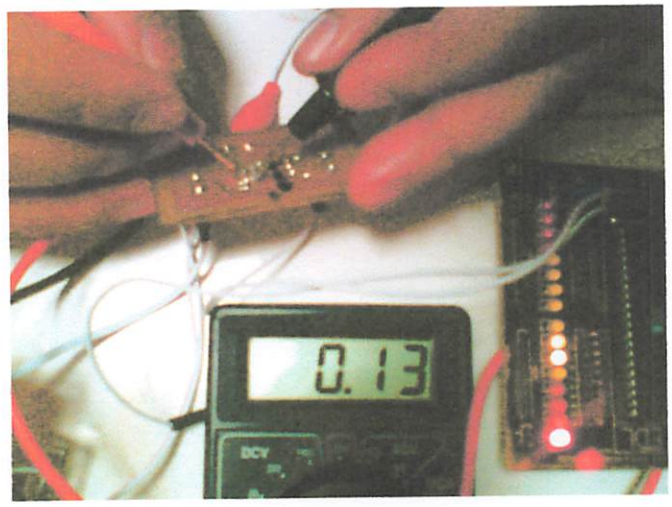


Gambar 4.2. Rangkaian Pengujian Driver Motor DC

2. Berikan masukan aktif *low* pada input rangkaian *driver* melalui port mikrokontroler.

3. Amati hasil yang ditunjukkan amperemeter

#### 4.3.2.2. Hasil Pengujian




Gambar 4.3. Hasil Pengujian Arus Basis pada Driver Motor DC

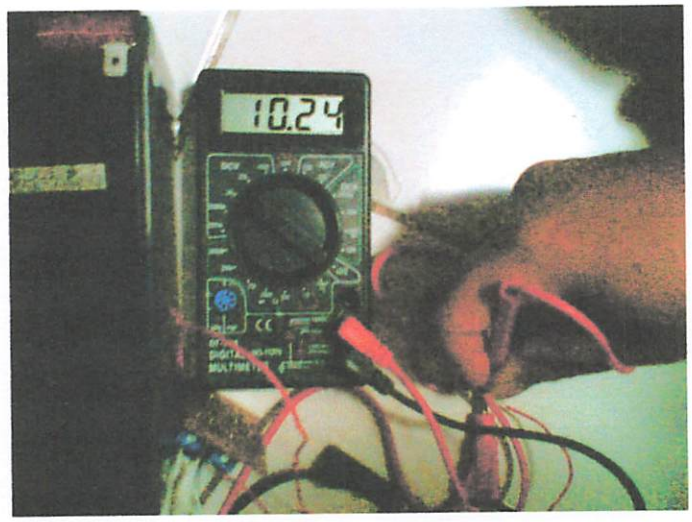
Dari hasil perhitungan didapatkan arus yang mengalir pada basis A733 adalah 0.12 mA, Sedangkan dari hasil pengujian didapatkan arus yang mengalir adalah 0.13 mA. Maka dapat diketahui persentase *error* hasil pengujian terhadap perhitungan adalah:

Dengan menggunakan persamaan 4.1 didapatkan :

$$\%\text{error} = \frac{|0.12mA - 0.13mA|}{0.12mA} x100\% = 8.33\%$$

### 4.3.3. Charge Control

Pengujian rangkaian *charge control* ini bertujuan untuk mengetahui apakah rangkaian ini dapat bekerja sebagaimana mestinya, yaitu dapat secara otomatis memutus kontak saat waktu yang diprogram pada mikro habis. Saat tegangan sama dengan komparator batas bawah dari accu maka sel surya men – *charge*.

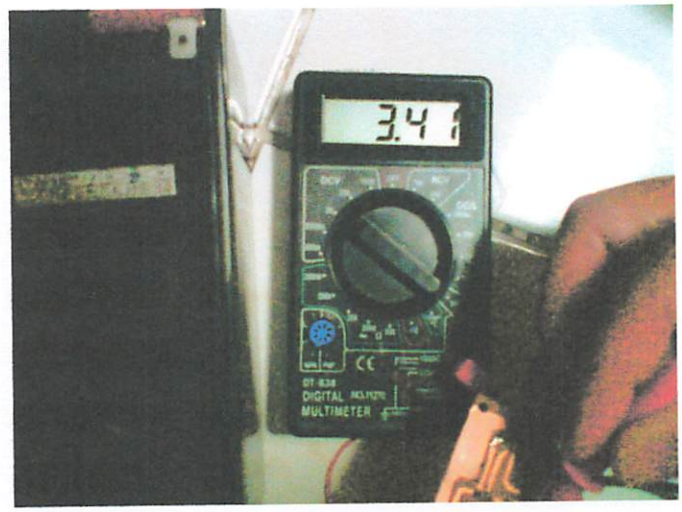



Gambar 4.4.Hasil Pengujian Tegangan *Set point*

*Charge control* ini terdiri dari Vrefl dan Vref2 , Vrefl merupakan input dari *accu* sedang Vref2 merupakan tegangan referensi yang nantinya dipakai untuk pembanding dari Vrefl, untuk Vref2 diberikan potensio 2. Supaya tegangan Vref2 tetap 5 V pada saat tegangan *accu* drop atau turun maka diberikan regulator 7805. Karena Vref2

menggunakan regulator agar tegangan tetap berada di 5 V maka Vref1 juga diberikan potensio 1 supaya membagi tegangan dari accu, jika tegangan *accu* turun Vref1 juga turun atau berbanding lurus.

Karena itu ditetapkan Vref2 = 3.41 V, jika diinginkan pada saat tegangan *accu* turun/ drop pada batas 10 V maka pada potensio 1 akan dicari tegangan dari 10V dari *accu* menjadi 3.41 V,

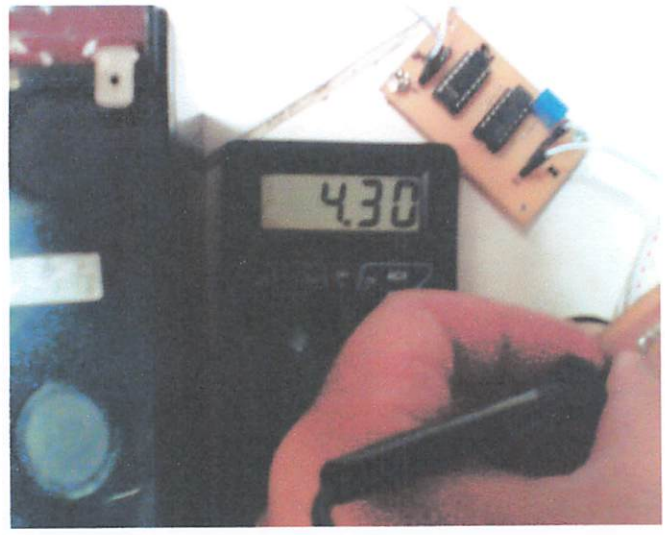



Gambar 4.5.Hasil Pengujian Tegangan Referensi1

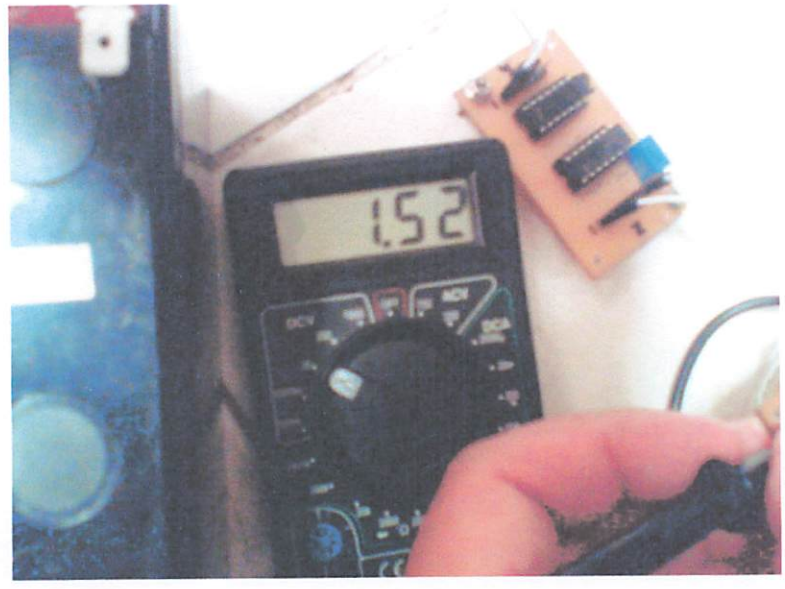
karena *charge control* merupakan rangkaian komparator maka:

Saat Vref1 < Vref2 , output dari 741 = 4.3 V (high).

Saat Vref1 > Vref2, output dari 741 = 1.5 V (low).



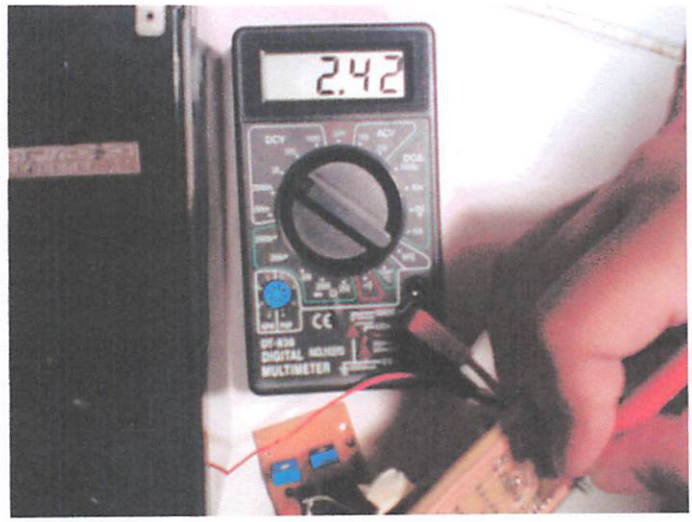

Gambar 4.6.a. Hasil Pengujian Tegangan *Output High* dari Komparator




Gambar 4.6.b. Hasil Pengujian Tegangan *Output Low* dari Komparator

Karena mikro tidak menerima 1.5 V maka harus dimasukkan ke rangkaian pengkondisi sinyal yaitu LM324 dan 7414, dimana LM324 untuk membandingkan kembali dan 7414 untuk pengkondisi sinyal, pada saat output 741 = 4.3 V maka kondisi

akan high, dan turun pada 1.5 V.jadi tegangan Vref pada LM324 (pengkondisi sinyal) harus diantaranya, jadi diambil Vref = 2.4 V.

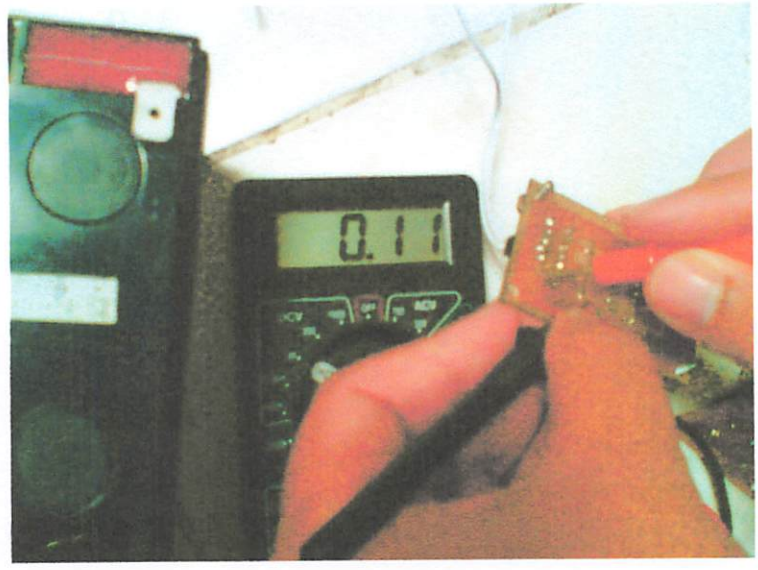



Gambar 4.7.Hasil Pengujian Tegangan Referensi Pengkondisi Sinyal

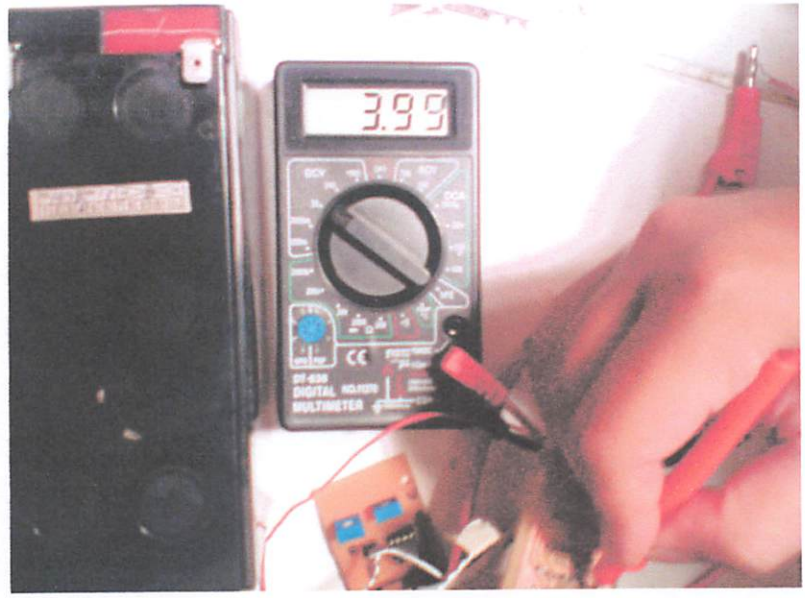
Maka didapatkan:

Vout 741 < Vref / Vout 741 = Vref maka output 7414 = 3.99V

Vout 741 > Vref maka output 7414 = 0.11V




Gambar 4.8.a. Hasil Pengujian Tegangan *Output Low* dari *Schmit Trigger*



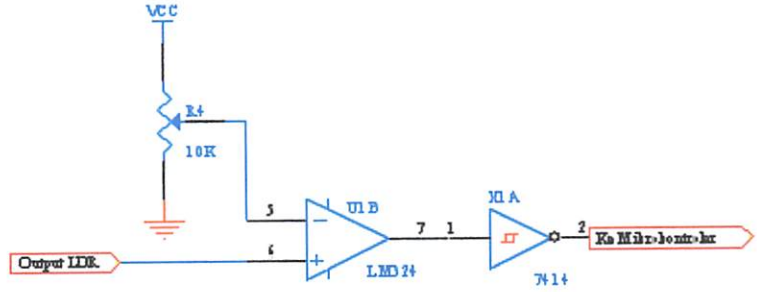
Gambar 4.8.b. Hasil Pengujian Tegangan *Output High* dari *Schmit Trigger*

### 4.3.4. Rangkaian Pengkondisi Sinyal

Gambar 4.9 menunjukkan rangkaian pengkondisi sinyal yang terdiri dari *non inverting amplifier*, komparator *op amp* dan IC *schmitt trigger* 74LS14 agar *output*-nya berupa sinyal digital.

Metode pengujiannya sebagai berikut:

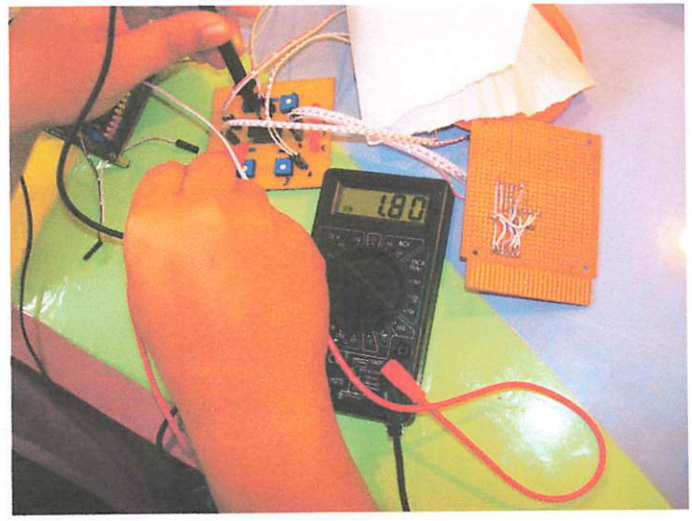
- Merangkai rangkaian pengkondisi sinyal seperti gambar 4.9
- Memasang catu daya DC 5 volt.
- Mengukur tegangan keluaran dengan *AVO meter*.



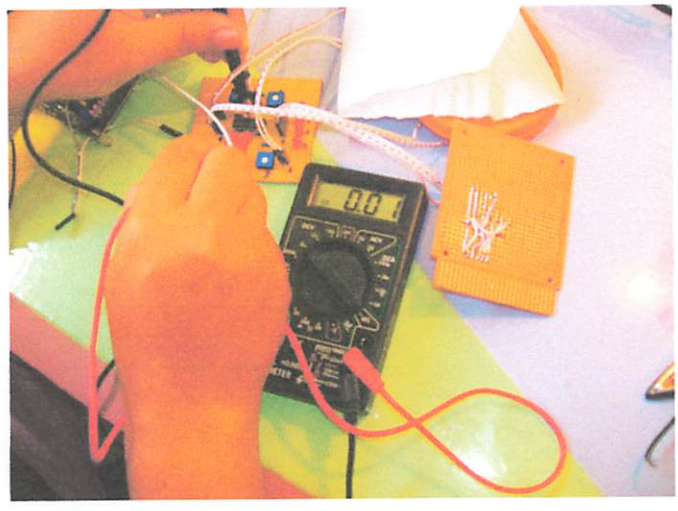

Gambar 4.9. Rangkaian Pengkondisi Sinyal

#### 4.3.4.1. Hasil dan analisa pengujian

Hasil pengujian setelah sinyal input melewati rangkaian *non inverting amplifier* ditunjukkan dalam tabel sebagai berikut :



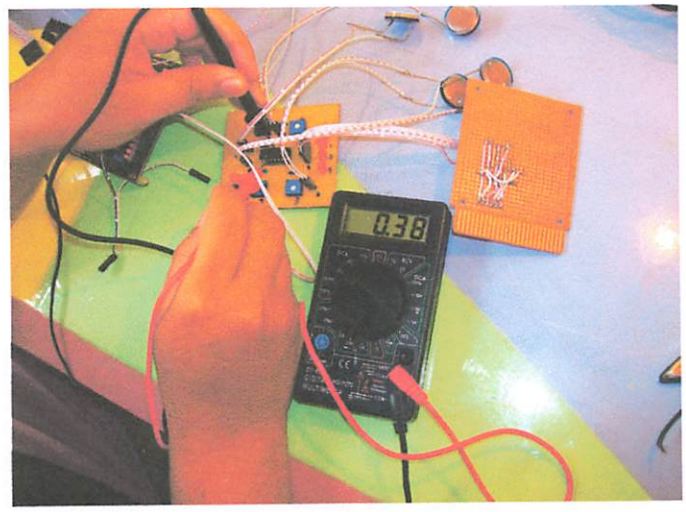
Gambar 4.10.a. Hasil Pengujian Tegangan Input
dari Komparator pada saat Gelap



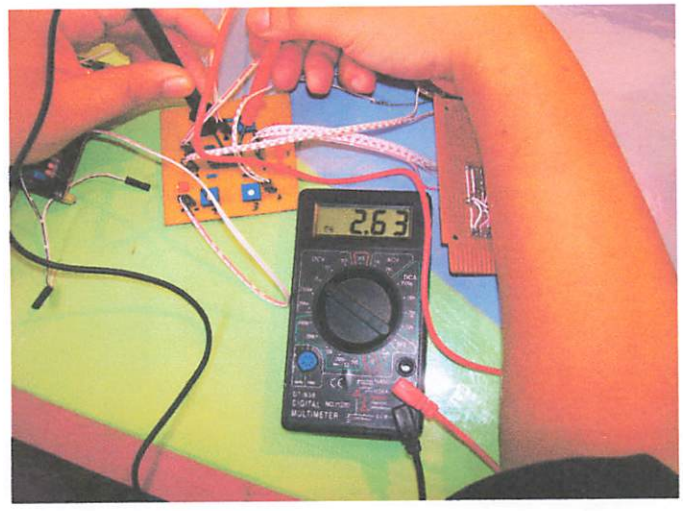
Gambar 4.10.b. Hasil Pengujian Tegangan Output
dari Komparator pada saat Gelap

Tabel 4.2. Tabel Hasil Pengujian Rangkaian Komparator Detektor Cahaya pada saat Gelap

| No LDR | Tegangan Input (V) | Tegangan Referensi (V) | Tegangan Output (V) |
|---|---|---|---|
| **Sensor 1** | 1.8 | 0.7 | 0.01 |
| **Sensor 2** | 2.18 | 2 | 0.02 |
| **Sensor 3** | 0.77 | 0.3 | 0.01 |
| **Sensor 4** | 1.49 | 1.2 | 0.01 |




Gambar 4.11.a. Hasil Pengujian Tegangan Input dari Komparator pada saat Terang




Gambar 4.11.b. Hasil Pengujian Tegangan Output dari Komparator pada saat Terang

Tabel 4.3. Tabel Hasil Pengujian Rangkaian Romparator Detektor Cahaya pada saat Terang

| No LDR | Tegangan Input (V) | Tegangan Referensi (V) | Tegangan Output (V) |
|---|---|---|---|
| Sensor 1 | 0,38 | 0,7 | 2,63 |
| Sensor 2 | 0.88 | 2 | 2.61 |
| Sensor 3 | 0.18 | 0.3 | 2.65 |
| Sensor 4 | 0.72 | 1.2 | 2.60 |

Setelah mengetahui tegangan output dari rangkaian komparator, pada table diatas terdapat inputan yang berbeda – beda karena pada rangkaian sensor ini mempunyai Vref tersendiri dari masing – masing LDR, jadi setting Vrefnya berbeda – beda untuk masing – masing LDR. Output dari rangkaian komparator berupa tegangan sudah berada dalam level TTL karena catu daya pada op amp yang digunakan pada rangkaian komparator ialah 5 volt.

Untuk dapat membuat sinyal yang lebih baik output dari rangkaian komparator dimasukkan pada IC *schmitt trigger* 74LS14. Sinyal yang dihasilkan dari *output schmitt trigger* akan digunakan sebagai sinyal input dari mikrokontroler ATMega 16 dan kemudian diolah pada program mikrokontroler ATMega 16.

### 4.3.5. Perbedaan hasil kapasitas tegangan akhir pada *Accu*

Pada pengujian akhir ini nantinya akan didapatkan perbedaan hasil dari pengisian aki dimana didapatkan hasil sebagai berikut:


Gambar 4.12.a. Tegangan Awal Accu Saat Sel Surya Diam


Gambar 4.12.b. Tegangan Akhir Accu Saat Sel Surya Diam

Tabel 4.4. Tabel Hasil Perhitungan Pengisian *Accu* pada saat Sel Surya Diam

| Data | Jam Pengisian | Arus (ampere) | Tegangan Awal (Volt) | Tegangan Akhir (Volt) | Wh/Hari |
|---|---|---|---|---|---|
| I | 08.00-09.00 | 0.3 | 8.18 | 8.18 | 19.63 |
| II | 09.00-10.00 | 0.23 | 8.18 | 8.18 | 15.05 |
| III | 10.00-11.00 | 0.57 | 8.18 | 8.25 | 37.6 |
| IV | 11.00-12.00 | 2.27 | 8.25 | 8.37 | 151.9 |

| | | | | | |
|---|---|---|---|---|---|
| V | 12.00-13.00 | 2.54 | 8.37 | 8.64 | 175.6 |
| VI | 13.00-14.00 | 2.36 | 8.64 | 8.88 | 167.7 |
| VII | 14.00-15.00 | 2.24 | 8.88 | 9.08 | 162.7 |
| IX | 15.00-16.00 | 1.86 | 9.08 | 9.3 | 138.4 |


Gambar 4.13.a. Tegangan Awal Accu Saat Sel Surya Gerak


Gambar 4.13.b. Tegangan Awal Accu Saat Sel Surya Gerak

Tabel 4.5. Tabel Hasil Perhitungan Pengisian *Accu* pada Saat Sel Surya Bergerak

| Data | Jam Pengisian | Arus (ampere) | Tegangan Awal (Volt) | Tegangan Akhir (Volt) | Wh/Hari |
|---|---|---|---|---|---|
| I | 08.00-09.00 | 2.32 | 8.15 | 8.35 | 154.98 |
| II | 09.00-10.00 | 2.44 | 8.35 | 8.6 | 167.9 |
| III | 10.00-11.00 | 2.48 | 8.6 | 8.87 | 175.98 |
| IV | 11.00-12.00 | 2.52 | 8.87 | 9.15 | 184.5 |
| V | 12.00-13.00 | 2.53 | 9.15 | 9.4 | 190.3 |
| VI | 13.00-14.00 | 2.58 | 9.4 | 9.7 | 200.2 |
| VII | 14.00-15.00 | 2.55 | 9.7 | 9.96 | 203.2 |
| IX | 15.00-16.00 | 2.42 | 9.96 | 10.23 | 198.1 |

Dari data diatas maka diperoleh perbandingan sebagai berikut:

$$\bar{x} = \frac{\sum xi}{n}$$

$\bar{x}$ = rata – rata daya (wh/hari)

xi = jumlah daya

n = banyaknya data

- Diam

$$\bar{x} = \frac{19.63+15.05+37.6+151.9+175.6+167.7+162.7+138.4}{8}$$

= 108.6 Wh/hari

- Gerak

$$\bar{x} = \frac{154.98+167.9+175.98+184.5+190.3+200.2+203.2+198.1}{8}$$

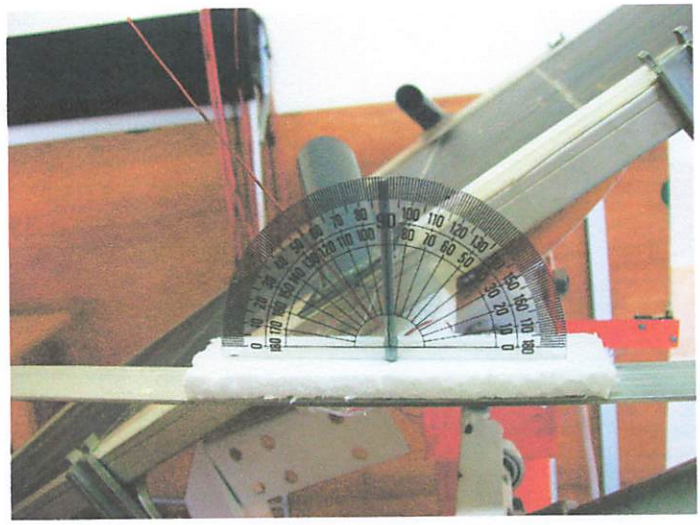
= 184.4 Wh/hari

### 4.3.6. Error Alat

Error dari alat dapat diketahui dari perbandingan sudut antara letak sumber cahaya dengan sudut dari sel surya, kami menentukan sudut untuk sumber cahayanya sebesar:

1. Untuk arah timur = $60^0$
2. Untuk arah tegak lurus = $90^0$
3. Untuk arah barat = $120^0$

Jadi nantinya akan dibagi menjadi 3 bagian, sehingga error dari alat dapat diketahui sebagai berikut:



Gambar 4.14. Pengujian Alat Saat Arah Timur

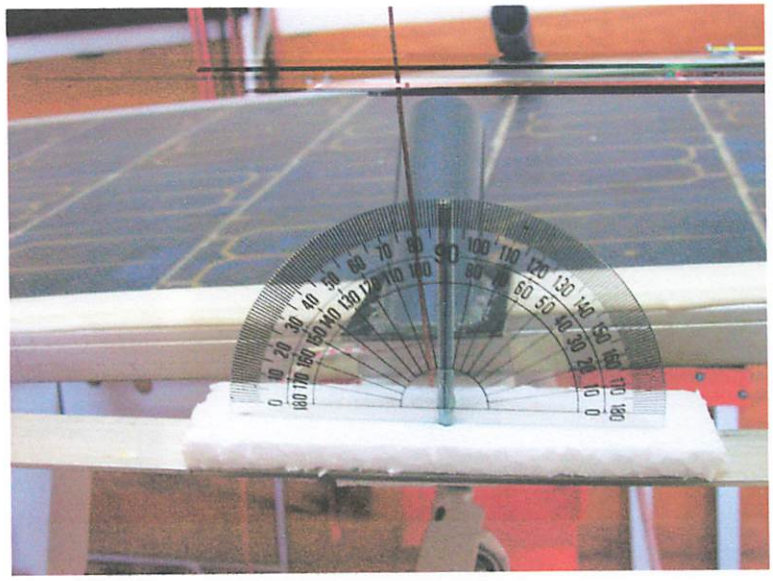
a. Untuk arah timur

Diketahui sudut sumber cahaya = $60^o$

Sudut dari alat = $55^o$

$$\text{Error alat} = \frac{60^{\circ} - 55^{0}}{60^{0}} \bullet 100\%$$

$$= 8.33\ \%$$



Gambar 4.15. Pengujian Alat Saat Arah Tegak Lurus

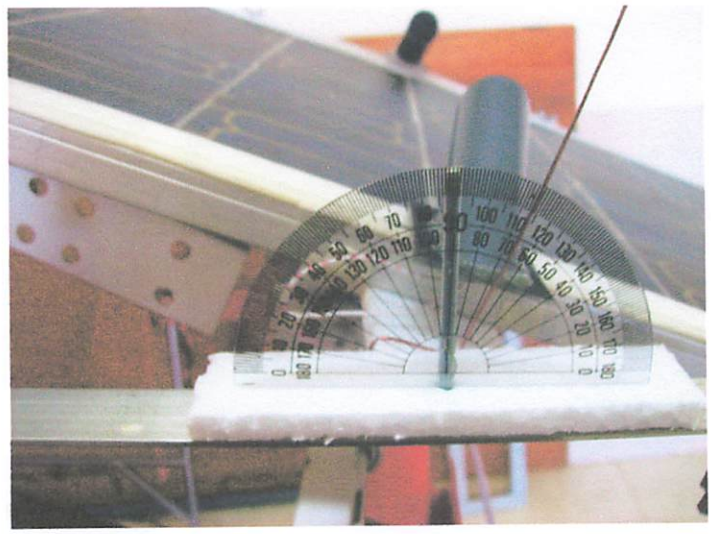
b. untuk arah tegak lurus

diketahui sudut sumber cahaya = $90^{\circ}$

sudut dari alat = $81^{\circ}$

$$\text{Error alat} = \frac{90^{\circ} - 81^{0}}{90^{0}} \bullet 100\%$$

$$= 10\ \%$$



Gambar 4.16. Pengujian Alat Saat Arah Barat

c. untuk arah tegak lurus

diketahui sudut sumber cahaya = $120^{o}$

sudut dari alat = $113^{o}$

$$\text{Error alat} = \frac{120^{o} - 113^{0}}{120^{0}} \bullet 100\%$$

$$= 5.83\ \%$$

### 4.3.7. Arah Posisi Sel Surya Saat Bergerak

Gambar 4.17. Alat Kontrol Modul Sel surya Arah Timur

Gambar 4.18. Alat Kontrol Modul Sel surya Arah Barat

Gambar 4.19. Alat Kontrol Modul Sel surya Arah Utara

Gambar 4.20. Alat Kontrol Modul Sel surya Arah Selatan

Gambar 4.21. Alat Kontrol Modul Sel surya Arah Tegak Lurus

# BAB V

# PENUTUP

## 5.1 Kesimpulan

Selama dalam perencanaan dan pengujian dari keseluruhan sistem yang telah di buat maka dapat ditarik beberapa kesimpulan antara lain:

1. Dari hasil pengujian diperoleh daya sebesar 108.6 Wh/ hari pada saat modul sel surya diam, sedangkan pada saat modul sel surya bergerak sebesar 184.4 Wh/ hari.
2. Error kontrol dari alat diperoleh untuk arah timur sebesar 8.33 %, sedangkan arah tegak lurus sebesar 10 %, untuk arah barat sebesar 5.83 %.
3. Hambatan dari LDR pada saat terang 0.3 Kohm dan pada saat gelap 6.19Kohm, ini juga tergantung pada intensitas dari cahaya yang masuk.
4. Karena adanya perbedaan hambatan LDR maka tegangan input dari op amp juga berbeda – beda antar LDR.
5. Untuk *charge control* tergantung dari *timer* yang diset, karena *timer* sudah diset untuk 10 jam, jadi akan men – *charge* selama 10 jam saja, apabila sudah 10 jam dan *accu* belum penuh otomatis *charge control* akan memutus tegangan yang mengalir dari modul sel surya, sehingga tidak dipengaruhi oleh penuh atau tidaknya accu.
6. Cuaca sangat mempengaruhi peng – *charge* – an dari *accu.*

7. Posisi dari sensor LDR juga sangat menentukan kepresisian dari kontrol terhadap matahari.

**5.2. Saran – Saran**

Untuk meningkatkan kepresisian dari kontrol dapat diperlukan pengujian yang lebih, karena banyak sekali yang mempengaruhi dari kepresisian alat. Untuk lebih meningkatkan perolehan daya dari panel sel surya dapat digunakan panel yang lebih besar. Untuk lebih menghemat atau efisiensi dari alat dapat juga setelah *accu* sudah penuh dialihkan pemakaiannya pada fungsi yang lain. Cuaca dan keadaan dari awan serta posisi dari matahari sangat mempengaruhi perolehan daya dari panel sel surya.

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

# FORMULIR PERBAIKAN SKRIPSI

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NIM : 03.17.104

Jurusan : Teknik Elektro S-1

Konsentrasi : Teknik Elektronika

Judul : Perancangan Dan Pembuatan Alat Kontrol Penjejak Matahari yang Digunakan Untuk Optimasi Penyerapan Radiasi Matahari Pada Sel Surya Berbasis Mikrokontroler AT MEGA 16.

Hari / Tanggal Ujian Skripsi : Sabtu / 15 Maret 2008

| No | Tanggal | Uraian | Paraf |
|---|---|---|---|
| 1 | 15/3/2008 | Pengujian rangkaian komparator harus ada kolom tegangan referensi sebagai bandingan | |

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Mengetahui,

Dosen Pembimbing I

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NIP.P. 1030100361

## Daftar Pustaka


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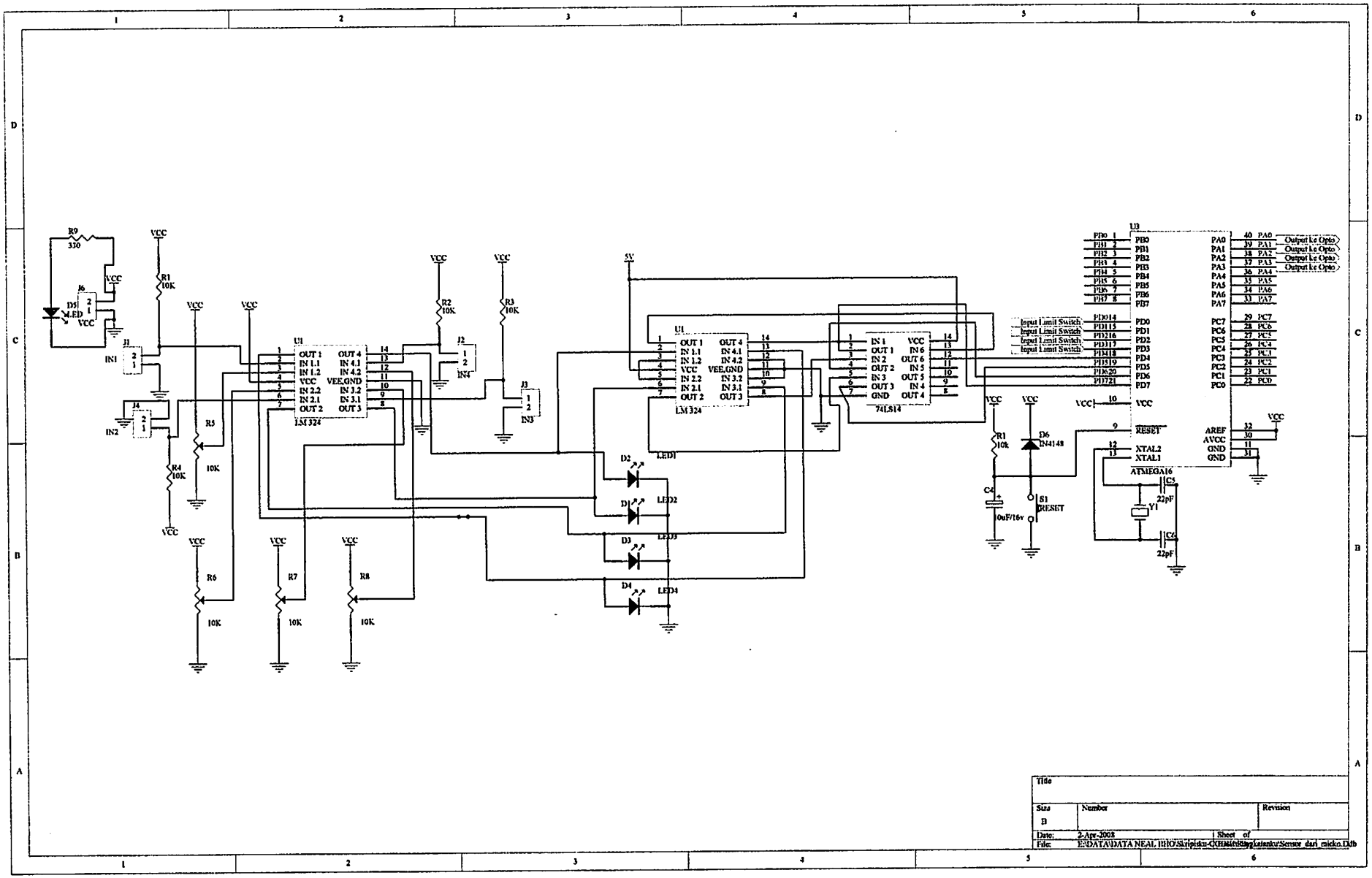
# LAMPIRAN


R9
330
LED
J6
D5
VCC
R1
10K
J1
IN1
J4
IN2
R4
10K
R5
10K
U1
LM324
OUT 1
IN 1.1
IN 1.2
VCC
IN 2.2
IN 2.1
OUT 2
OUT 4
IN 4.1
IN 4.2
VEE,GND
IN 3.2
IN 3.1
OUT 3
R2
10K
J2
IN4
R3
10K
J3
IN3
R6
10K
R7
10K
R8
10K
5V
LED1
D2
LED2
D1
LED3
D3
LED4
D4
74LS14
IN 1
OUT 1
IN 2
OUT 2
IN 3
OUT 3
GND
VCC
IN 6
OUT 6
IN 5
OUT 5
IN 4
OUT 4
Input Limit Switch
U3
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
RESET
XTAL2
XTAL1
ATMEGA16
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PC7
PC6
PC5
PC4
PC3
PC2
PC1
PC0
AREF
AVCC
GND
Output ke Opto
D6
IN4148
C4
0uF/16v
S1
RESET
C5
22pF
Y1
C6
22pF
Title
Size
B
Number
Revision
Date:
2-Apr-2008
Sheet of
File:
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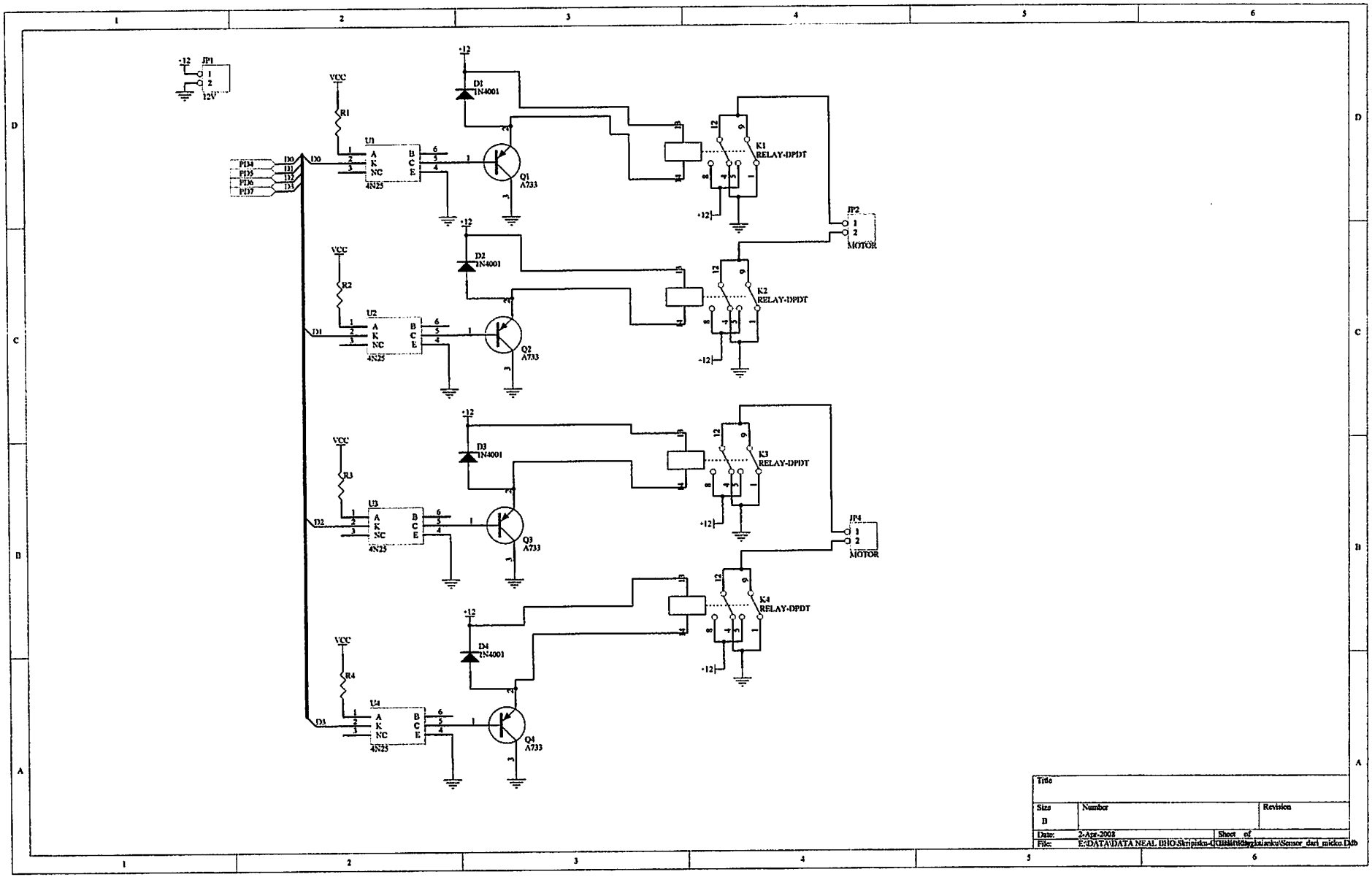
+12
JP1
1
2
12V
VCC
R1
D1
1N4001
U1
A
K
NC
B
C
E
4N25
Q1
A733
K1
RELAY-DPDT
PD34
PD35
PD36
PD37
D0
D1
D2
D3
JP2
MOTOR
R2
U2
Q2
A733
K2
R3
U3
Q3
A733
K3
JP4
R4
U4
Q4
A733
K4
Title
Size
B
Number
Revision
Date:
2-Apr-2008
Sheet of
File:
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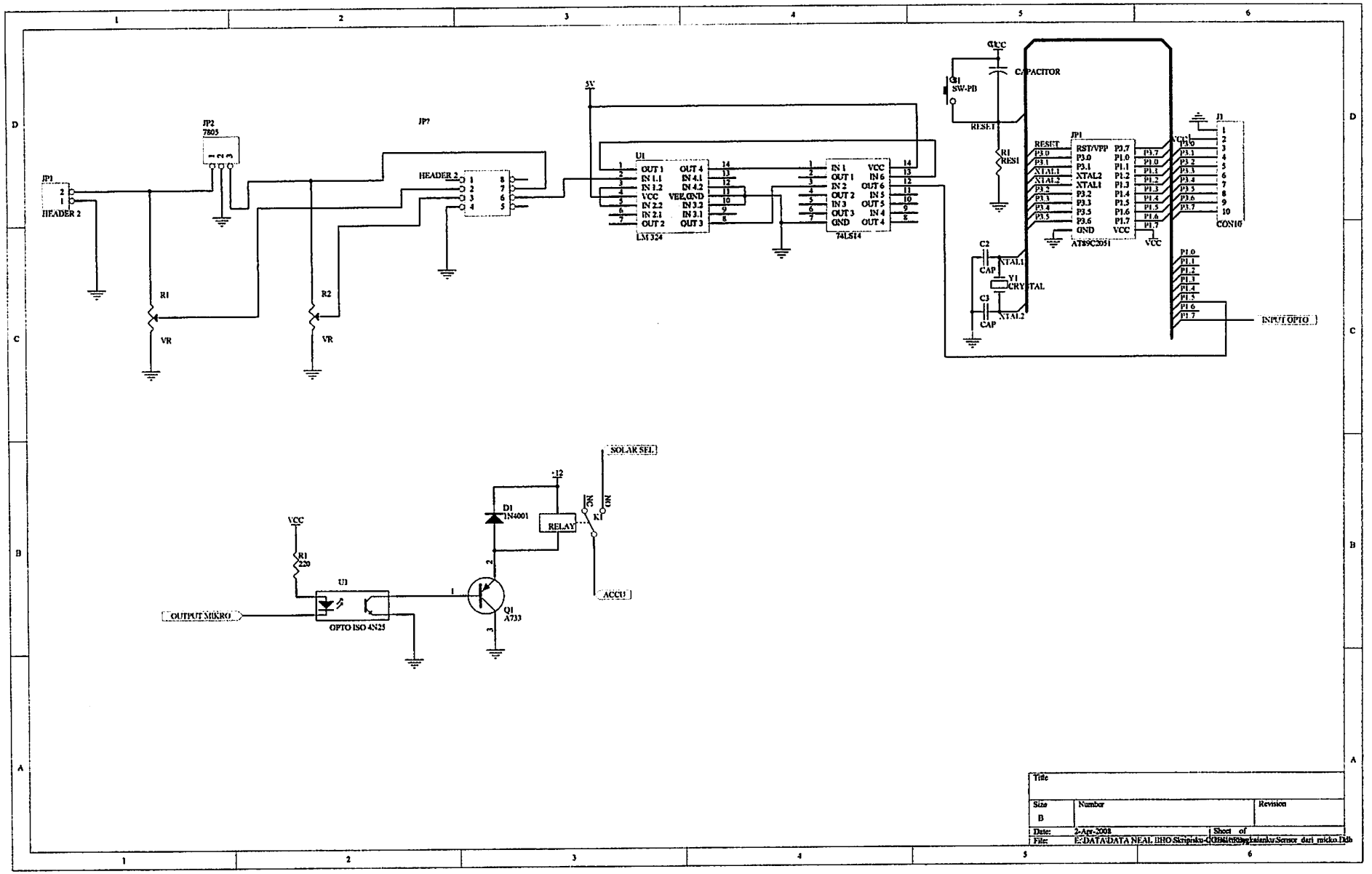

JP1
HEADER 2
JP2
7805
JP7
HEADER 2
R1
VR
R2
VR
5V
U1
LM324
74LS14
VCC
CAPACITOR
SW-PB
RESET
R1
RES1
JP1
AT89C2051
C2
CAP
Y1
CRYSTAL
C3
CAP
XTAL1
XTAL2
J1
CON10
INPUT OPTO
SOLAR SEL
+12
D1
1N4001
RELAY
K1
NC
NO
COM
ACCU
VCC
R1
220
U3
OPTO ISO 4N25
Q1
A733
OUTPUT MIKRO
Title
Size
B
Number
Revision
Date:
2-Apr-2008
Sheet of
File:
E:\DATA\DATA NEAL BHO Skripsiku-C\BHO Skripsiku\Sensor dari micko.Ddb

# KONTROL SEL SURYA

```
$regfile = "m16def.dat"
$crystal = 11059200
Declare Sub Putarkanan
Declare Sub Putarkiri
Declare Sub Maju
Declare Sub Mundur
Declare Sub Berhenti
Config Porta = Output
Config Portd = Input


Awal:
Do
Portd = &B11111111
  If Pind.7 = 1 And Pind.6 = 1 And Pind.5 = 0 And Pind.4 = 1 Then
    waitms 500
    Call Putarkanan
      If Pind.2 = 0 Then
        Goto Sore
      End If
  End If

  If Pind.7 = 1 And Pind.6 = 0 And Pind.5 = 0 And Pind.4 = 0 Then
    Waitms 500
    Call Putarkanan
      If Pind.2 = 0 Then
        Goto Sore
      End If
  End If

  If Pind.7 = 1 And Pind.6 = 0 And Pind.5 = 1 And Pind.4 = 0 Then
    Waitms 500
    Call Berhenti
  End If

  If Pind.7 = 0 And Pind.6 = 1 And Pind.5 = 1 And Pind.4 = 1 Then
    Waitms 500
    Call Putarkiri
  End If

  If Pind.7 = 1 And Pind.6 = 1 And Pind.5 = 1 And Pind.4 = 0 Then
    Waitms 500
    Call Mundur
```

```
    If Pind.1 = 0 Then
      Goto Mentok1
    End If
End If

If Pind.7 = 0 And Pind.6 = 1 And Pind.5 = 0 And Pind.4 = 0 Then
  Waitms 500
  Call Mundur
    If Pind.1 = 0 Then
      Goto Mentok1
    End If
End If

If Pind.7 = 1 And Pind.6 = 0 And Pind.5 = 1 And Pind.4 = 1 Then
  Waitms 500
  Call Maju
    If Pind.0 = 0 Then
      Goto Mentok2
    End If
End If

If Pind.7 = 0 And Pind.6 = 0 And Pind.5 = 0 And Pind.4 = 1 Then
  Waitms 500
  Call Maju
    If Pind.0 = 0 Then
      Goto Mentok2
    End If
End If

If Pind.7 = 0 And Pind.6 = 1 And Pind.5 = 0 And Pind.4 = 1 Then
  Waitms 500
  Call Berhenti
End If

If Pind.7 = 1 And Pind.6 = 1 And Pind.5 = 1 And Pind.4 = 1 Then
  Waitms 500
  Call Berhenti
End If

If Pind.7 = 0 And Pind.6 = 0 And Pind.5 = 0 And Pind.4 = 0 Then
  Call Putarkiri
    If Pind.3 = 0 Then
      Goto Hilang
    End If
End If
```

```
Loop


Mentok1:
Call Berhenti
Do
Portd = &B11111111
  If Pind.7 = 1 And Pind.6 = 1 And Pind.5 = 0 And Pind.4 = 1 Then
    Call Putarkanan
      If Pind.2 = 0 Then
        Goto Sore
      End If
  End If

  If Pind.7 = 0 And Pind.6 = 1 And Pind.5 = 1 And Pind.4 = 1 Then
    Call Putarkiri
  End If

  If Pind.7 = 1 And Pind.6 = 1 And Pind.5 = 0 And Pind.4 = 1 Then
    Call Berhenti
  End If

  If Pind.7 = 0 And Pind.6 = 0 And Pind.5 = 0 And Pind.4 = 0 Then
    Call Putarkiri
      If Pind.3 = 0 Then
        Goto Hilang
      End If
  End If
Loop

Mentok2:
Call Berhenti
Do
Portd = &B11111111
  If Pind.7 = 1 And Pind.6 = 1 And Pind.5 = 0 And Pind.4 = 1 Then
    Waitms 500
    Call Putarkanan
      If Pind.2 = 0 Then
        Goto Sore
      End If
  End If

  If Pind.7 = 0 And Pind.6 = 1 And Pind.5 = 1 And Pind.4 = 1 Then
    Waitms 500
    Call Putarkiri
  End If
```

```
  If Pind.7 = 1 And Pind.6 = 1 And Pind.5 = 1 And Pind.4 = 1 Then
    Call Berhenti
  End If

  If Pind.7 = 0 And Pind.6 = 0 And Pind.5 = 0 And Pind.4 = 0 Then
    Waitms 500
    Call Putarkiri
      If Pind.3 = 0 Then
        Goto Hilang
      End If
  End If
Loop
Sore:
Portd = &B11111111
Do
Call Putarkiri
  If Pind.3 = 0 Then
    Goto Hilang
  End If
Loop
Hilang:
Do
Portd = &B11111111
Call Berhenti
Call Putarkanan
Wait 2
  Do
  If Pind.7 = 0 And Pind.6 = 0 And Pind.5 = 0 And Pind.4 = 0 Then
    Call Berhenti

  Else
  Goto Awal
  End If
  Loop
Loop



End
Sub Putarkanan
  Porta.0 = 0
  Porta.1 = 1
  Porta.2 = 1
  Porta.3 = 1
End Sub
```

```
Sub Putarkiri
  Porta.0 = 1
  Porta.1 = 0
  Porta.2 = 1
  Porta.3 = 1
End Sub

Sub Mundur
  Porta.0 = 1
  Porta.1 = 1
  Porta.2 = 0
  Porta.3 = 1
End Sub

Sub Maju
  Porta.0 = 1
  Porta.1 = 1
  Porta.2 = 1
  Porta.3 = 0
End Sub

Sub Berhenti
  Porta.0 = 1
  Porta.1 = 1
  Porta.2 = 1
  Porta.3 = 1
End Sub
```

## CHARGE CONTROL

```
org    00h

MULAI:  jnb    p1.5,mulai
        CLR    P1.7
        MOV    R4,#150

AKHIR:  CALL   TIMER
        DJNZ   R4,AKHIR
        setb   P1.7
        SJMP   mulai

TIMER:  mov    tmod,#01
        MOV    R3,#120
habis:
        mov    R2,#184

loop:   mov    th0,#0d8h
        mov    tl0,#0f0h
        setb   tr0

wait:   jnb    tf0,$
        clr    tr0
        clr    tf0
        djnz   R2,loop
        cpl    P1.6
        DJNZ   R3,HABIS
        RET
end
```

National Semiconductor

August 2000

# LM741
# Operational Amplifier

## General Description

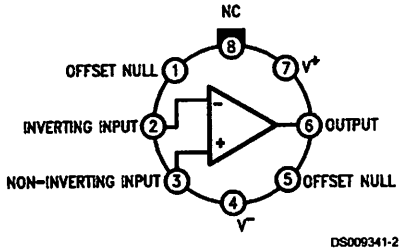
The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

## Connection Diagrams

**Metal Can Package**

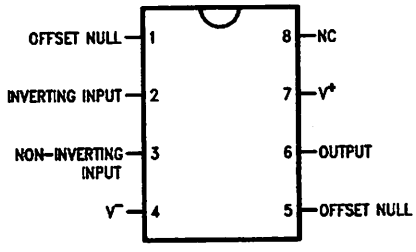



DS009341-2

Note 1: LM741H is available per JM38510/10101

**Order Number LM741H, LM741H/883** (Note 1), **LM741AH/883 or LM741CH**
**See NS Package Number H08C**

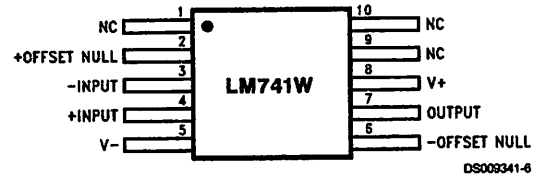
**Dual-In-Line or S.O. Package**




DS009341-3

**Order Number LM741J, LM741J/883, LM741CN**
**See NS Package Number J08A, M08A or N08E**

**Ceramic Flatpak**

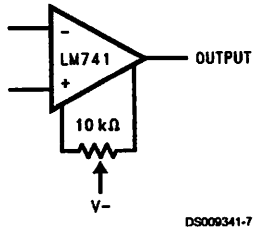



DS009341-6

**Order Number LM741W/883**
**See NS Package Number W10A**

## Typical Application

**Offset Nulling Circuit**




DS009341-7

## Absolute Maximum Ratings (Note 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

(Note 7)

| | LM741A | LM741 | LM741C |
|---|---|---|---|
| Supply Voltage | ±22V | ±22V | ±18V |
| Power Dissipation (Note 3) | 500 mW | 500 mW | 500 mW |
| Differential Input Voltage | ±30V | ±30V | ±30V |
| Input Voltage (Note 4) | ±15V | ±15V | ±15V |
| Output Short Circuit Duration | Continuous | Continuous | Continuous |
| Operating Temperature Range | −55°C to +125°C | −55°C to +125°C | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C |
| Junction Temperature | 150°C | 150°C | 100°C |
| Soldering Information | | | |
| N-Package (10 seconds) | 260°C | 260°C | 260°C |
| J- or H-Package (10 seconds) | 300°C | 300°C | 300°C |
| M-Package | | | |
| Vapor Phase (60 seconds) | 215°C | 215°C | 215°C |
| Infrared (15 seconds) | 215°C | 215°C | 215°C |
| See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. | | | |
| ESD Tolerance (Note 8) | 400V | 400V | 400V |

## Electrical Characteristics (Note 5)

| Parameter | Conditions | LM741A | | | LM741 | | | LM741C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A$ = 25°C | | | | | | | | | | |
| | $R_S \le 10\ k\Omega$ | | | | | 1.0 | 5.0 | | 2.0 | 6.0 | mV |
| | $R_S \le 50\Omega$ | | 0.8 | 3.0 | | | | | | | mV |
| | $T_{AMIN} \le T_A \le T_{AMAX}$ | | | | | | | | | | |
| | $R_S \le 50\Omega$ | | | 4.0 | | | | | | | mV |
| | $R_S \le 10\ k\Omega$ | | | | | | 6.0 | | | 7.5 | mV |
| Average Input Offset Voltage Drift | | | | 15 | | | | | | | µV/°C |
| Input Offset Voltage Adjustment Range | $T_A$ = 25°C, $V_S$ = ±20V | ±10 | | | | ±15 | | | ±15 | | mV |
| Input Offset Current | $T_A$ = 25°C | | 3.0 | 30 | | 20 | 200 | | 20 | 200 | nA |
| | $T_{AMIN} \le T_A \le T_{AMAX}$ | | | 70 | | 85 | 500 | | | 300 | nA |
| Average Input Offset Current Drift | | | | 0.5 | | | | | | | nA/°C |
| Input Bias Current | $T_A$ = 25°C | | 30 | 80 | | 80 | 500 | | 80 | 500 | nA |
| | $T_{AMIN} \le T_A \le T_{AMAX}$ | | | 0.210 | | | 1.5 | | | 0.8 | µA |
| Input Resistance | $T_A$ = 25°C, $V_S$ = ±20V | 1.0 | 6.0 | | 0.3 | 2.0 | | 0.3 | 2.0 | | MΩ |
| | $T_{AMIN} \le T_A \le T_{AMAX}$, $V_S$ = ±20V | 0.5 | | | | | | | | | MΩ |
| Input Voltage Range | $T_A$ = 25°C | | | | | | | ±12 | ±13 | | V |
| | $T_{AMIN} \le T_A \le T_{AMAX}$ | | | | ±12 | ±13 | | | | | V |

## lectrical Characteristics (Note 5) (Continued)

| Parameter | Conditions | LM741A | | | LM741 | | | LM741C | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| e Signal Voltage Gain | $T_A$ = 25°C, $R_L \geq 2$ kΩ | | | | | | | | | | |
| | $V_S$ = ±20V, $V_O$ = ±15V | 50 | | | | | | | | | V/mV |
| | $V_S$ = ±15V, $V_O$ = ±10V | | | | 50 | 200 | | 20 | 200 | | V/mV |
| | $T_{AMIN} \leq T_A \leq T_{AMAX}$, | | | | | | | | | | |
| | $R_L \geq 2$ kΩ, | | | | | | | | | | |
| | $V_S$ = ±20V, $V_O$ = ±15V | 32 | | | | | | | | | V/mV |
| | $V_S$ = ±15V, $V_O$ = ±10V | | | | 25 | | | 15 | | | V/mV |
| | $V_S$ = ±5V, $V_O$ = ±2V | 10 | | | | | | | | | V/mV |
| ıut Voltage Swing | $V_S$ = ±20V | | | | | | | | | | |
| | $R_L \geq 10$ kΩ | ±16 | | | | | | | | | V |
| | $R_L \geq 2$ kΩ | ±15 | | | | | | | | | V |
| | $V_S$ = ±15V | | | | | | | | | | |
| | $R_L \geq 10$ kΩ | | | | ±12 | ±14 | | ±12 | ±14 | | V |
| | $R_L \geq 2$ kΩ | | | | ±10 | ±13 | | ±10 | ±13 | | V |
| ıut Short Circuit | $T_A$ = 25°C | 10 | 25 | 35 | | 25 | | | 25 | | mA |
| ent | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | 10 | | 40 | | | | | | | mA |
| ımon-Mode | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | | | | | | | | | | |
| ıction Ratio | $R_S \leq 10$ kΩ, $V_{CM}$ = ±12V | | | | 70 | 90 | | 70 | 90 | | dB |
| | $R_S \leq 50$Ω, $V_{CM}$ = ±12V | 80 | 95 | | | | | | | | dB |
| ply Voltage Rejection | $T_{AMIN} \leq T_A \leq T_{AMAX}$, | | | | | | | | | | |
| o | $V_S$ = ±20V to $V_S$ = ±5V | | | | | | | | | | |
| | $R_S \leq 50$Ω | 86 | 96 | | | | | | | | dB |
| | $R_S \leq 10$ kΩ | | | | 77 | 96 | | 77 | 96 | | dB |
| ısient Response | $T_A$ = 25°C, Unity Gain | | | | | | | | | | |
| ise Time | | | 0.25 | 0.8 | | 0.3 | | | 0.3 | | µs |
| vershoot | | | 6.0 | 20 | | 5 | | | 5 | | % |
| dwidth (Note 6) | $T_A$ = 25°C | 0.437 | 1.5 | | | | | | | | MHz |
| v Rate | $T_A$ = 25°C, Unity Gain | 0.3 | 0.7 | | | 0.5 | | | 0.5 | | V/µs |
| ply Current | $T_A$ = 25°C | | | | | 1.7 | 2.8 | | 1.7 | 2.8 | mA |
| ver Consumption | $T_A$ = 25°C | | | | | | | | | | |
| | $V_S$ = ±20V | | 80 | 150 | | | | | | | mW |
| | $V_S$ = ±15V | | | | | 50 | 85 | | 50 | 85 | mW |
| M741A | $V_S$ = ±20V | | | | | | | | | | |
| | $T_A = T_{AMIN}$ | | | 165 | | | | | | | mW |
| | $T_A = T_{AMAX}$ | | | 135 | | | | | | | mW |
| M741 | $V_S$ = ±15V | | | | | | | | | | |
| | $T_A = T_{AMIN}$ | | | | | 60 | 100 | | | | mW |
| | $T_A = T_{AMAX}$ | | | | | 45 | 75 | | | | mW |

ote 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is nctional, but do not guarantee specific performance limits.

Order this document by LM324/D

MOTOROLA

# LM324, LM324A, LM224, LM2902, LM2902V

# Quad Low Power Operational Amplifiers

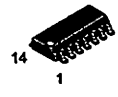
## QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

**SEMICONDUCTOR TECHNICAL DATA**

The LM324 series are low–cost, quad operational amplifiers with true differential inputs. They have several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 32 V with quiescent currents about one–fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

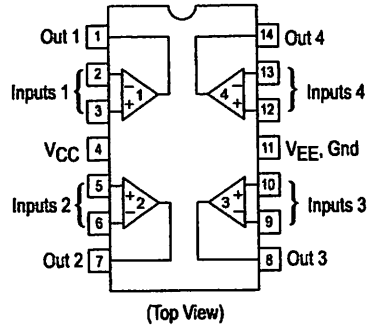
- Short Circuited Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents: 100 nA Maximum (LM324A)
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Operation


**N SUFFIX**
PLASTIC PACKAGE
CASE 646
(LM224, LM324, LM2902 Only)




**D SUFFIX**
PLASTIC PACKAGE
CASE 751A
(SO–14)

**PIN CONNECTIONS**




**MAXIMUM RATINGS** ($T_A$ = +25°C, unless otherwise noted.)

| Rating | Symbol | LM224 LM324, LM324A | LM2902, LM2902V | Unit |
|---|---|---|---|---|
| Power Supply Voltages Single Supply Split Supplies | $V_{CC}$ $V_{CC}$, $V_{EE}$ | 32 ±16 | 26 ±13 | Vdc |
| Input Differential Voltage Range (See Note 1) | $V_{IDR}$ | ±32 | ±26 | Vdc |
| Input Common Mode Voltage Range | $V_{ICR}$ | –0.3 to 32 | –0.3 to 26 | Vdc |
| Output Short Circuit Duration | $t_{SC}$ | Continuous | | |
| Junction Temperature | $T_J$ | 150 | | °C |
| Storage Temperature Range | $T_{stg}$ | –65 to +150 | | °C |
| Operating Ambient Temperature Range | $T_A$ | –25 to +85 0 to +70 | –40 to +105 –40 to +125 | °C |

**NOTE:** 1. Split Power Supplies.

**ORDERING INFORMATION**

| Device | Operating Temperature Range | Package |
|---|---|---|
| LM2902D | $T_A$ = –40° to +105°C | SO–14 |
| LM2902N | | Plastic DIP |
| LM2902VD | $T_A$ = –40° to +125°C | SO–14 |
| LM2902VN | | Plastic DIP |
| LM224D | $T_A$ = –25° to +85°C | SO–14 |
| LM224N | | Plastic DIP |
| LM324AD | $T_A$ = 0° to +70°C | SO–14 |
| LM324AN | | Plastic DIP |
| LM324D | | SO–14 |
| LM324N | | Plastic DIP |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{EE}$ = Gnd, $T_A$ = 25°C, unless otherwise noted.)

| Characteristics | Symbol | LM224 | | | LM324A | | | LM324 | | | LM2902 | | | LM2902V | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage<br>$V_{CC}$ = 5.0 V to 30 V (26 V for LM2902, V), $V_{ICR}$ = 0 V to $V_{CC}$ –1.7 V, $V_O$ = 1.4 V, $R_S$ = 0 Ω | $V_{IO}$ | | | | | | | | | | | | | | | | mV |
| $T_A$ = 25°C | | – | 2.0 | 5.0 | – | 2.0 | 3.0 | – | 2.0 | 7.0 | – | 2.0 | 7.0 | – | 2.0 | 7.0 | |
| $T_A$ = $T_{high}$[1] | | – | – | 7.0 | – | – | 5.0 | – | – | 9.0 | – | – | 10 | – | – | 13 | |
| $T_A$ = $T_{low}$[1] | | – | – | 7.0 | – | – | 5.0 | – | – | 9.0 | – | – | 10 | – | – | 10 | |
| Average Temperature Coefficient of Input Offset Voltage<br>$T_A$ = $T_{high}$ to $T_{low}$[1] | $\Delta V_{IO}/\Delta T$ | – | 7.0 | – | – | 7.0 | 30 | – | 7.0 | – | – | 7.0 | – | – | 7.0 | – | µV/°C |
| Input Offset Current | $I_{IO}$ | – | 3.0 | 30 | – | 5.0 | 30 | – | 5.0 | 50 | – | 5.0 | 50 | – | 5.0 | 50 | nA |
| $T_A$ = $T_{high}$ to $T_{low}$[1] | | – | – | 100 | – | – | 75 | – | – | 150 | – | – | 200 | – | – | 200 | |
| Average Temperature Coefficient of Input Offset Current<br>$T_A$ = $T_{high}$ to $T_{low}$[1] | $\Delta I_{IO}/\Delta T$ | – | 10 | – | – | 10 | 300 | – | 10 | – | – | 10 | – | – | 10 | – | pA/°C |
| Input Bias Current | $I_{IB}$ | – | –90 | –150 | – | –45 | –100 | – | –90 | –250 | – | –90 | –250 | – | –90 | –250 | nA |
| $T_A$ = $T_{high}$ to $T_{low}$[1] | | – | – | –300 | – | – | –200 | – | – | –500 | – | – | –500 | – | – | –500 | |
| Input Common Mode Voltage Range[2] | $V_{ICR}$ | | | | | | | | | | | | | | | | V |
| $V_{CC}$ = 30 V (26 V for LM2902, V) | | 0 | – | 28.3 | 0 | – | 28.3 | 0 | – | 28.3 | 0 | – | 24.3 | 0 | – | 24.3 | |
| $V_{CC}$ = 30 V (26 V for LM2902, V), $T_A$ = $T_{high}$ to $T_{low}$ | | 0 | – | 28 | 0 | – | 28 | 0 | – | 28 | 0 | – | 24 | 0 | – | 24 | |
| Differential Input Voltage Range | $V_{IDR}$ | – | – | $V_{CC}$ | – | – | $V_{CC}$ | – | – | $V_{CC}$ | – | – | $V_{CC}$ | – | – | $V_{CC}$ | V |
| Large Signal Open Loop Voltage Gain | $A_{VOL}$ | | | | | | | | | | | | | | | | V/mV |
| $R_L$ = 2.0 kΩ, $V_{CC}$ = 15 V, for Large $V_O$ Swing, $T_A$ = $T_{high}$ to $T_{low}$[1] | | 50<br>25 | 100<br>– | –<br>– | 25<br>15 | 100<br>– | –<br>– | 25<br>15 | 100<br>– | –<br>– | 25<br>15 | 100<br>– | –<br>– | 25<br>15 | 100<br>– | –<br>– | |
| Channel Separation 10 kHz ≤ f ≤ 20 kHz, Input Referenced | CS | – | –120 | – | – | –120 | – | – | –120 | – | – | –120 | – | – | –120 | – | dB |
| Common Mode Rejection, $R_S$ ≤ 10 kΩ | CMR | 70 | 85 | – | 65 | 70 | – | 65 | 70 | – | 50 | 70 | – | 50 | 70 | – | dB |
| Power Supply Rejection | PSR | 65 | 100 | – | 65 | 100 | – | 65 | 100 | – | 50 | 100 | – | 50 | 100 | – | dB |
| Output Voltage–High Limit ($T_A$ = $T_{high}$ to $T_{low}$)[1] | $V_{OH}$ | | | | | | | | | | | | | | | | V |
| $V_{CC}$ = 5.0 V, $R_L$ = 2.0 kΩ, $T_A$ = 25°C | | 3.3 | 3.5 | – | 3.3 | 3.5 | – | 3.3 | 3.5 | – | 3.3 | 3.5 | – | 3.3 | 3.5 | – | |
| $V_{CC}$ = 30 V (26 V for LM2902, V), $R_L$ = 2.0 kΩ | | 26 | – | – | 26 | – | – | 26 | – | – | 22 | – | – | 22 | – | – | |
| $V_{CC}$ = 30 V (26 V for LM2902, V), $R_L$ = 10 kΩ | | 27 | 28 | – | 27 | 28 | – | 27 | 28 | – | 23 | 24 | – | 23 | 24 | – | |

**NOTES:** 1. $T_{low}$ = –25°C for LM224 = 0°C for LM324, A = –40°C for LM2902 = –40°C for LM2902V; $T_{high}$ = +85°C for LM224 = +70°C for LM324, A = +105°C for LM2902 = +125°C for LM2902V

2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is $V_{CC}$ –1.7 V.

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{EE}$ = Gnd, $T_A$ = 25°C, unless otherwise noted.)

| Characteristics | Symbol | LM224 | | | LM324A | | | LM324 | | | LM2902 | | | LM2902V | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage – Low Limit, $V_{CC}$ = 5.0 V, $R_L$ = 10 kΩ, $T_A$ = $T_{high}$ to $T_{low}$(1) | $V_{OL}$ | – | 5.0 | 20 | – | 5.0 | 20 | – | 5.0 | 20 | – | 5.0 | 100 | – | 5.0 | 100 | mV |
| Output Source Current ($V_{ID}$ = +1.0 V, $V_{CC}$ = 15 V) | $I_{O+}$ | | | | | | | | | | | | | | | | mA |
| $T_A$ = 25°C | | 20 | 40 | – | 20 | 40 | – | 20 | 40 | – | 20 | 40 | – | 20 | 40 | – | |
| $T_A$ = $T_{high}$ to $T_{low}$(1) | | 10 | 20 | – | 10 | 20 | – | 10 | 20 | – | 10 | 20 | – | 10 | 20 | – | |
| Output Sink Current ($V_{ID}$ = –1.0 V, $V_{CC}$ = 15 V) $T_A$ = 25°C | $I_{O-}$ | 10 | 20 | – | 10 | 20 | – | 10 | 20 | – | 10 | 20 | – | 10 | 20 | – | mA |
| $T_A$ = $T_{high}$ to $T_{low}$(1) | | 5.0 | 8.0 | – | 5.0 | 8.0 | – | 5.0 | 8.0 | – | 5.0 | 8.0 | – | 5.0 | 8.0 | – | |
| ($V_{ID}$ = –1.0 V, $V_O$ = 200 mV, $T_A$ = 25°C) | | 12 | 50 | – | 12 | 50 | – | 12 | 50 | – | – | – | – | – | – | – | µA |
| Output Short Circuit to Ground(3) | $I_{SC}$ | – | 40 | 60 | – | 40 | 60 | – | 40 | 60 | – | 40 | 60 | – | 40 | 60 | mA |
| Power Supply Current ($T_A$ = $T_{high}$ to $T_{low}$)(1) $V_{CC}$ = 30 V (26 V for LM2902, V), $V_O$ = 0 V, $R_L$ = ∞ | $I_{CC}$ | – | – | 3.0 | – | 1.4 | 3.0 | – | – | 3.0 | – | – | 3.0 | – | – | 3.0 | mA |
| $V_{CC}$ = 5.0 V, $V_O$ = 0 V, $R_L$ = ∞ | | – | – | 1.2 | – | 0.7 | 1.2 | – | – | 1.2 | – | – | 1.2 | – | – | 1.2 | |

**NOTES:** 1. $T_{low}$ = –25°C for LM224 = 0°C for LM324, A = –40°C for LM2902 = –40°C for LM2902V
$T_{high}$ = +85°C for LM224 = +70°C for LM324, A = +105°C for LM2902 = +125°C for LM2902V

2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is $V_{CC}$ –1.7 V.

**Representative Circuit Diagram**
(One–Fourth of Circuit Shown)

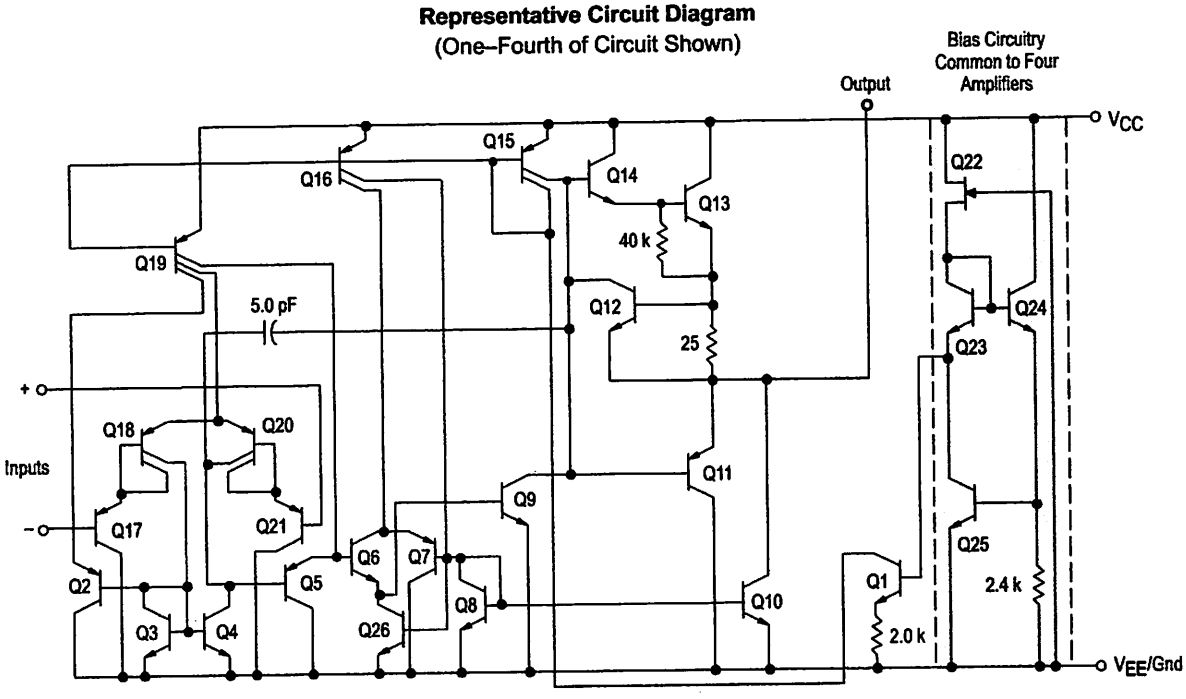
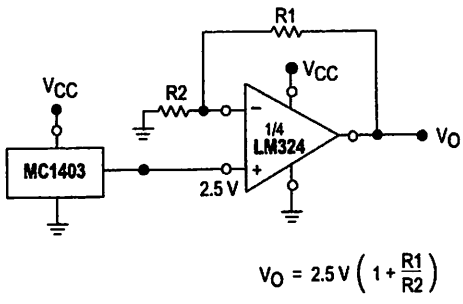
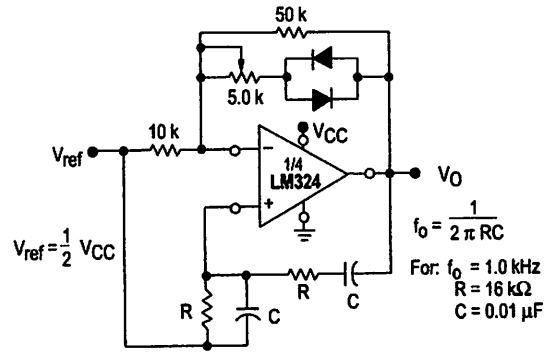


**Figure 7. Voltage Reference**




$$V_O = 2.5\,V\left(1+\frac{R1}{R2}\right)$$

**Figure 8. Wien Bridge Oscillator**

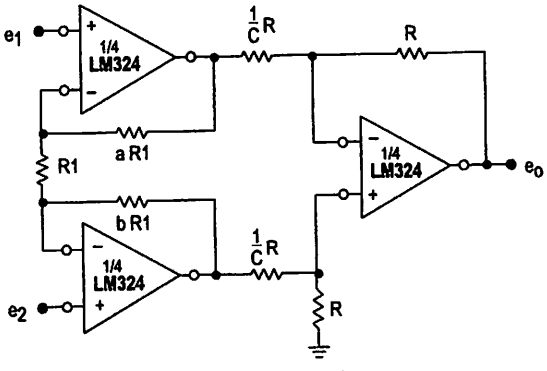



$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2\pi RC}$$

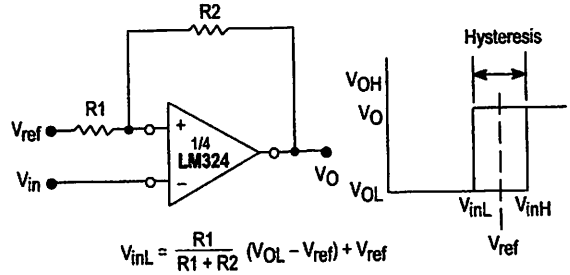
For: $f_o$ = 1.0 kHz
R = 16 kΩ
C = 0.01 µF

**Figure 9. High Impedance Differential Amplifier**




$$e_o = C(1 + a + b)(e_2 - e_1)$$

**Figure 10. Comparator with Hysteresis**

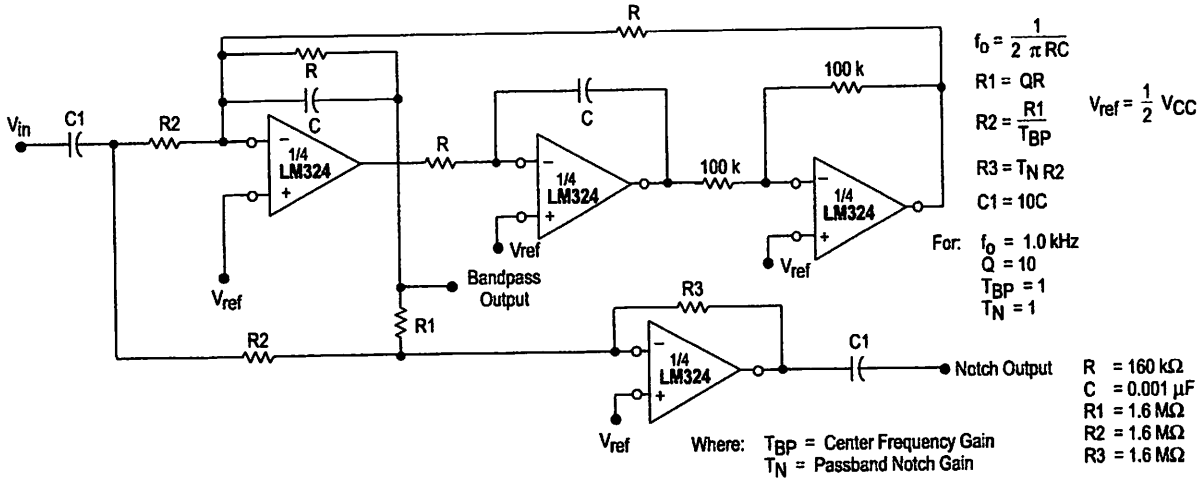



$$V_{inL} = \frac{R1}{R1 + R2}(V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2}(V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

**Figure 11. Bi-Quad Filter**




$$f_o = \frac{1}{2\pi RC}$$

R1 = QR

$$R2 = \frac{R1}{T_{BP}}$$

R3 = $T_N$ R2

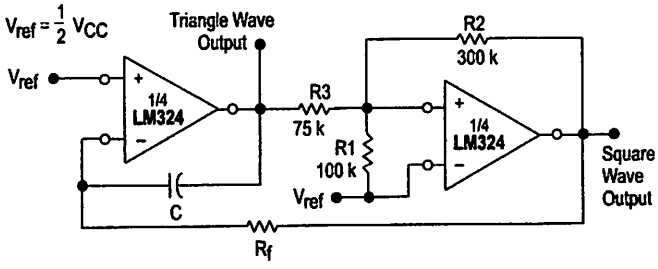
C1 = 10C

$$V_{ref} = \frac{1}{2} V_{CC}$$

For: $f_o$ = 1.0 kHz
Q = 10
$T_{BP}$ = 1
$T_N$ = 1

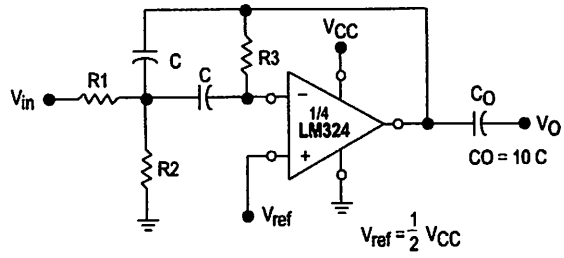
R = 160 kΩ
C = 0.001 µF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

**Figure 12. Function Generator**




$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if } R3 = \frac{R2\,R1}{R2 + R1}$$

**Figure 13. Multiple Feedback Bandpass Filter**




Given: $f_0$ = center frequency
$A(f_0)$ = gain at center frequency

Choose value $f_0$, C

Then: $R3 = \frac{Q}{\pi f_0 C}$

$$R1 = \frac{R3}{2\,A(f_0)}$$

$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

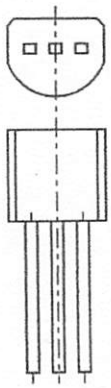
For less than 10% error from operational amplifier, $\frac{Q_0\,f_0}{BW} < 0.1$

where $f_0$ and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

# TO-92 Plastic-Encapsulate Transistors

## A733 TRANSISTOR(PNP)



**TO-92**

1.EMITTER

2.COLLECTOR

3.BASE

1 2 3

## FEATURES

**Power dissipation**

$P_{CM}$: 0.25W (Tamb=25℃)

**Collector current**

$I_{CM}$: -0.15A

**Collector-base voltage**

$V_{(BR)CBO}$: -60 V

**Operating and storage junction temperature range**

$T_J, T_{stg}$: -55℃ to + 150℃

## ELECTRICAL CHARACTERISTICS

(Tamb=25℃ unless otherwise specified)

| Parameter | Symbol | Test conditions | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Collector-base breakdown voltage | $V_{(BR)CBO}$ | $I_C$= -5 μ A, $I_E$=0 | -60 | | | V |
| Collector-emitter breakdown voltage | $V_{(BR)CEO}$ | $I_C$= -1 mA, $I_B$=0 | -50 | | | V |
| Emitter-base breakdown voltage | $V_{(BR)EBO}$ | $I_E$= -50 μ A, $I_C$=0 | -5 | | | V |
| Collector cut-off current | $I_{CBO}$ | $V_{CB}$= -60 V, $I_E$=0 | | | -0.1 | μ A |
| Emitter cut-off current | $I_{EBO}$ | $V_{EB}$= -5 V, $I_C$=0 | | | -0.1 | μ A |
| DC current gain | $h_{FE}$ | $V_{CE}$= -6 V, $I_C$= -1 mA | 90 | 200 | 600 | |
| Collector-emitter saturation voltage | $V_{CEsat}$ | $I_C$= -100 mA, $I_B$= -10 mA | | -0.18 | -0.3 | V |
| Transition frequency | $f_T$ | $V_{CE}$= -6 V, $I_C$= -10 mA<br>f =30MHz | 50 | 180 | | MHz |

## CLASSIFICATION OF $h_{FE}$

| Rank | R | Q | P | K |
|---|---|---|---|---|
| Range | 90-180 | 135-270 | 200-400 | 300-600 |

FAIRCHILD
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# MC78XX/LM78XX/MC78XXA

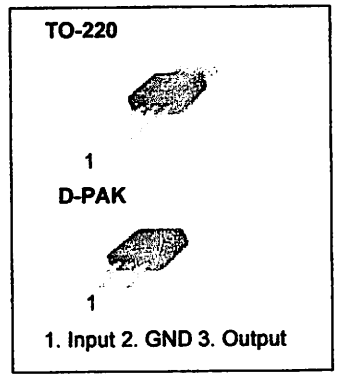
## 3-Terminal 1A Positive Voltage Regulator

### Features

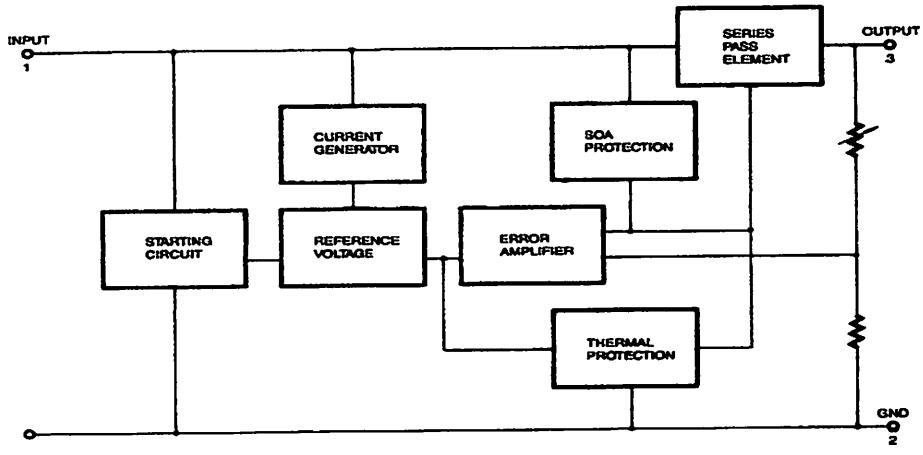
- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

### Description

The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.




### Internal Block Digram




Rev. 1.0.1

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (for $V_O$ = 5V to 18V)<br>(for $V_O$ = 24V) | $V_I$<br>$V_I$ | 35<br>40 | V<br>V |
| Thermal Resistance Junction-Cases (TO-220) | $R_{\theta JC}$ | 5 | °C/W |
| Thermal Resistance Junction-Air (TO-220) | $R_{\theta JA}$ | 65 | °C/W |
| Operating Temperature Range | $T_{OPR}$ | 0 ~ +125 | °C |
| Storage Temperature Range | $T_{STG}$ | -65 ~ +150 | °C |

## Electrical Characteristics (MC7805/LM7805)

(Refer to test circuit ,0°C < $T_J$ < 125°C, $I_O$ = 500mA, $V_I$ = 10V, $C_I$= 0.33μF, $C_O$= 0.1μF, unless otherwise specified)

| Parameter | Symbol | Conditions | | MC7805/LM7805 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 4.8 | 5.0 | 5.2 | V |
| | | 5.0mA ≤ $I_O$ ≤ 1.0A, $P_O$ ≤ 15W<br>$V_I$ = 7V to 20V | | 4.75 | 5.0 | 5.25 | |
| Line Regulation (Note1) | Regline | $T_J$=+25 °C | $V_O$ = 7V to 25V | - | 4.0 | 100 | mV |
| | | | $V_I$ = 8V to 12V | - | 1.6 | 50 | |
| Load Regulation (Note1) | Regload | $T_J$=+25 °C | $I_O$ = 5.0mA to1.5A | - | 9 | 100 | mV |
| | | | $I_O$ =250mA to 750mA | - | 4 | 50 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.0 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1.0A | | - | 0.03 | 0.5 | mA |
| | | $V_I$= 7V to 25V | | - | 0.3 | 1.3 | |
| Output Voltage Drift | $\Delta V_O/\Delta T$ | $I_O$= 5mA | | - | -0.8 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz, $T_A$=+25 °C | | - | 42 | - | μV/Vo |
| Ripple Rejection | RR | f = 120Hz<br>$V_O$ = 8V to 18V | | 62 | 73 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$ =+25 °C | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 15 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$ = 35V, $T_A$ =+25 °C | | - | 230 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$ =+25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Changes in $V_o$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7805A)

(Refer to the test circuits. 0°C < $T_J$ < 125°C, $I_O$ =1A, $V_I$ = 10V, $C_I$=0.33μF, $C_O$=0.1μF, unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 4.9 | 5 | 5.1 | V |
| | | $I_O$ = 5mA to 1A, $P_O \leq$ 15W<br>$V_I$ = 7.5V to 20V | | 4.8 | 5 | 5.2 | |
| Line Regulation (Note1) | Regline | $V_I$ = 7.5V to 25V<br>$I_O$ = 500mA | | - | 5 | 50 | mV |
| | | $V_I$ = 8V to 12V | | - | 3 | 50 | |
| | | $T_J$ =+25 °C | $V_I$= 7.3V to 20V | - | 5 | 50 | |
| | | | $V_I$= 8V to 12V | - | 1.5 | 25 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C<br>$I_O$ = 5mA to 1.5A | | - | 9 | 100 | mV |
| | | $I_O$ = 5mA to 1A | | - | 9 | 100 | |
| | | $I_O$ = 250mA to 750mA | | - | 4 | 50 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.0 | 6 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1A | | - | - | 0.5 | mA |
| | | $V_I$ = 8 V to 25V, $I_O$ = 500mA | | - | - | 0.8 | |
| | | $V_I$ = 7.5V to 20V, $T_J$ =+25 °C | | - | - | 0.8 | |
| Output Voltage Drift | $\Delta V/\Delta T$ | $I_O$ = 5mA | | - | -0.8 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz<br>$T_A$ =+25 °C | | - | 10 | - | μV/Vo |
| Ripple Rejection | RR | f = 120Hz, $I_O$ = 500mA<br>$V_I$ = 8V to 18V | | - | 68 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$ =+25 °C | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 17 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$= 35V, $T_A$ =+25 °C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$= +25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Change in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

National Semiconductor

June 1989

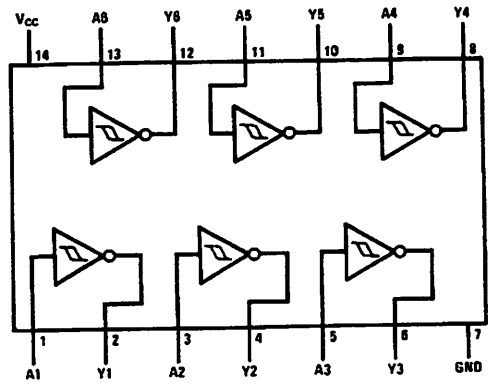
# 54LS14/DM74LS14 Hex Inverters with Schmitt Trigger Inputs

## General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

## Connection Diagram

**Dual-In-Line Package**




TL/F/6353–1

**Order Number 54LS14DMQB, 54LS14FMQB, 54LS14LMQB, DM74LS14M or DM74LS14N**
**See NS Package Number E20A, J14A, M14A, N14A or W14B**

## Function Table

$Y = \overline{A}$

| Input | Output |
|---|---|
| A | Y |
| L | H |
| H | L |

H = High Logic Level
L = Low Logic Level



RRD-B30M105/Printed in U. S. A.

## Absolute Maximum Ratings (Note)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | |
| 54LS | −55°C to +125°C |
| DM74LS | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

## Recommended Operating Conditions

| Symbol | Parameter | 54LS14 | | | DM74LS14 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{T+}$ | Positive-Going Input Threshold Voltage (Note 1) | 1.5 | 1.6 | 2.0 | 1.4 | 1.6 | 1.9 | V |
| $V_{T-}$ | Negative-Going Input Threshold Voltage (Note 1) | 0.6 | 0.8 | 1.1 | 0.5 | 0.8 | 1 | V |
| HYS | Input Hysteresis (Note 1) | 0.4 | 0.8 | | 0.4 | 0.8 | | V |
| $I_{OH}$ | High Level Output Current | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low Level Output Current | | | 4 | | | 8 | mA |
| $T_A$ | Free Air Operating Temperature | −55 | | 125 | 0 | | 70 | °C |

## Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | | Min | Typ (Note 2) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.5 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max, $V_{IL}$ = Max | 54LS | 2.5 | 3.4 | | V |
| | | | DM74 | 2.7 | 3.4 | | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max, $V_{IH}$ = Min | 54LS | | 0.25 | 0.4 | V |
| | | | DM74 | | 0.35 | 0.5 | |
| | | $V_{CC}$ = Min, $I_{OL}$ = 4 mA | DM74 | | 0.25 | 0.4 | |
| $I_{T+}$ | Input Current at Positive-Going Threshold | $V_{CC}$ = 5V, $V_I$ = $V_{T+}$ | DM74 | | −0.14 | | mA |
| $I_{T-}$ | Input Current at Negative-Going Threshold | $V_{CC}$ = 5V, $V_I$ = $V_{T-}$ | DM74 | | −0.18 | | mA |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = Max, $V_I$ = 7V | DM74 | | | 0.1 | mA |
| | | $V_{CC}$ = Max, $V_I$ = 10.0V | 54LS | | | | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7V | | | | 20 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4V | | | | −0.4 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (Note 3) | 54LS | −20 | | −100 | mA |
| | | | DM74 | −20 | | −100 | |
| $I_{CCH}$ | Supply Current with Outputs High | $V_{CC}$ = Max | | | 8.6 | 16 | mA |
| $I_{CCL}$ | Supply Current with Outputs Low | $V_{CC}$ = Max | | | 12 | 21 | mA |

Note 1: $V_{CC}$ = 5V.

Note 2: All typicals are at $V_{CC}$ = 5V, $T_A$ = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## Switching Characteristics at $V_{CC}$ = 5V and $T_A$ = 25°C (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | $R_L$ = 2 kΩ | | | | Units |
|---|---|---|---|---|---|---|
| | | $C_L$ = 15 pF | | $C_L$ = 50 pF | | |
| | | Min | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | 5 | 22 | 8 | 25 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | 5 | 22 | 10 | 33 | ns |

GlobalOptoisolator™

| VDE | UL | CSA | SETI | SEMKO | DEMKO | NEMKO | BABT |
|---|---|---|---|---|---|---|---|

# 6-Pin DIP Optoisolators Transistor Output

**4N25***
**4N25A***
**4N26***
[CTR = 20% Min]
**4N27**
**4N28**
[CTR = 10% Min]
*Motorola Preferred Devices

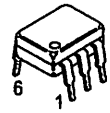
The 4N25/A, 4N26, 4N27 and 4N28 devices consist of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon phototransistor detector.

- Most Economical Optoisolator Choice for Medium Speed, Switching Applications
- Meets or Exceeds All JEDEC Registered Specifications
- ***To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.***

**Applications**

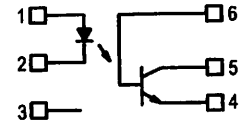
- General Purpose Switching Circuits
- Interfacing and coupling systems of different potentials and impedances
- I/O Interfacing
- Solid State Relays

**STYLE 1 PLASTIC**




**STANDARD THRU HOLE**
**CASE 730A–04**

**SCHEMATIC**




PIN 1. LED ANODE
2. LED CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| **INPUT LED** | | | |
| Reverse Voltage | $V_R$ | 3 | Volts |
| Forward Current — Continuous | $I_F$ | 60 | mA |
| LED Power Dissipation @ $T_A$ = 25°C<br>with Negligible Power in Output Detector<br>Derate above 25°C | $P_D$ | 120<br><br>1.41 | mW<br><br>mW/°C |
| **OUTPUT TRANSISTOR** | | | |
| Collector–Emitter Voltage | $V_{CEO}$ | 30 | Volts |
| Emitter–Collector Voltage | $V_{ECO}$ | 7 | Volts |
| Collector–Base Voltage | $V_{CBO}$ | 70 | Volts |
| Collector Current — Continuous | $I_C$ | 150 | mA |
| Detector Power Dissipation @ $T_A$ = 25°C<br>with Negligible Power in Input LED<br>Derate above 25°C | $P_D$ | 150<br><br>1.76 | mW<br><br>mW/°C |
| **TOTAL DEVICE** | | | |
| Isolation Surge Voltage(1)<br>(Peak ac Voltage, 60 Hz, 1 sec Duration) | $V_{ISO}$ | 7500 | Vac(pk) |
| Total Device Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 250<br>2.94 | mW<br>mW/°C |
| Ambient Operating Temperature Range(2) | $T_A$ | −55 to +100 | °C |
| Storage Temperature Range(2) | $T_{stg}$ | −55 to +150 | °C |
| Soldering Temperature (10 sec, 1/16" from case) | $T_L$ | 260 | °C |

1. Isolation surge voltage is an internal device dielectric breakdown rating.
   For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.
2. Refer to Quality and Reliability Section in Opto Data Book for information on test conditions.

**Preferred** devices are Motorola recommended choices for future use and best overall value.
GlobalOptoisolator is a trademark of Motorola, Inc.





MOTOROLA

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)(1)

| Characteristic | | Symbol | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUT LED** | | | | | | |
| Forward Voltage ($I_F$ = 10 mA) | $T_A$ = 25°C<br>$T_A$ = –55°C<br>$T_A$ = 100°C | $V_F$ | —<br>—<br>— | 1.15<br>1.3<br>1.05 | 1.5<br>—<br>— | Volts |
| Reverse Leakage Current ($V_R$ = 3 V) | | $I_R$ | — | — | 100 | µA |
| Capacitance (V = 0 V, f = 1 MHz) | | $C_J$ | — | 18 | — | pF |
| **OUTPUT TRANSISTOR** | | | | | | |
| Collector–Emitter Dark Current ($V_{CE}$ = 10 V, $T_A$ = 25°C | 4N25,25A,26,27<br>4N28 | $I_{CEO}$ | —<br>— | 1<br>1 | 50<br>100 | nA |
| ($V_{CE}$ = 10 V, $T_A$ = 100°C) | All Devices | $I_{CEO}$ | — | 1 | — | µA |
| Collector–Base Dark Current ($V_{CB}$ = 10 V) | | $I_{CBO}$ | — | 0.2 | — | nA |
| Collector–Emitter Breakdown Voltage ($I_C$ = 1 mA) | | $V_{(BR)CEO}$ | 30 | 45 | — | Volts |
| Collector–Base Breakdown Voltage ($I_C$ = 100 µA) | | $V_{(BR)CBO}$ | 70 | 100 | — | Volts |
| Emitter–Collector Breakdown Voltage ($I_E$ = 100 µA) | | $V_{(BR)ECO}$ | 7 | 7.8 | — | Volts |
| DC Current Gain ($I_C$ = 2 mA, $V_{CE}$ = 5 V) | | $h_{FE}$ | — | 500 | — | — |
| Collector–Emitter Capacitance (f = 1 MHz, $V_{CE}$ = 0) | | $C_{CE}$ | — | 7 | — | pF |
| Collector–Base Capacitance (f = 1 MHz, $V_{CB}$ = 0) | | $C_{CB}$ | — | 19 | — | pF |
| Emitter–Base Capacitance (f = 1 MHz, $V_{EB}$ = 0) | | $C_{EB}$ | — | 9 | — | pF |
| **COUPLED** | | | | | | |
| Output Collector Current ($I_F$ = 10 mA, $V_{CE}$ = 10 V) | 4N25,25A,26<br>4N27,28 | $I_C$ (CTR)(2) | 2 (20)<br>1 (10) | 7 (70)<br>5 (50) | —<br>— | mA (%) |
| Collector–Emitter Saturation Voltage ($I_C$ = 2 mA, $I_F$ = 50 mA) | | $V_{CE(sat)}$ | — | 0.15 | 0.5 | Volts |
| Turn–On Time ($I_F$ = 10 mA, $V_{CC}$ = 10 V, $R_L$ = 100 Ω)(3) | | $t_{on}$ | — | 2.8 | — | µs |
| Turn–Off Time ($I_F$ = 10 mA, $V_{CC}$ = 10 V, $R_L$ = 100 Ω)(3) | | $t_{off}$ | — | 4.5 | — | µs |
| Rise Time ($I_F$ = 10 mA, $V_{CC}$ = 10 V, $R_L$ = 100 Ω)(3) | | $t_r$ | — | 1.2 | — | µs |
| Fall Time ($I_F$ = 10 mA, $V_{CC}$ = 10 V, $R_L$ = 100 Ω)(3) | | $t_f$ | — | 1.3 | — | µs |
| Isolation Voltage (f = 60 Hz, t = 1 sec)(4) | | $V_{ISO}$ | 7500 | — | — | Vac(pk) |
| Isolation Resistance (V = 500 V)(4) | | $R_{ISO}$ | $10^{11}$ | — | — | Ω |
| Isolation Capacitance (V = 0 V, f = 1 MHz)(4) | | $C_{ISO}$ | — | 0.2 | — | pF |

1. Always design to the specified minimum/maximum electrical limits (where applicable).
2. Current Transfer Ratio (CTR) = $I_C/I_F$ x 100%.
3. For test circuit setup and waveforms, refer to Figure 11.
4. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

## TYPICAL CHARACTERISTICS

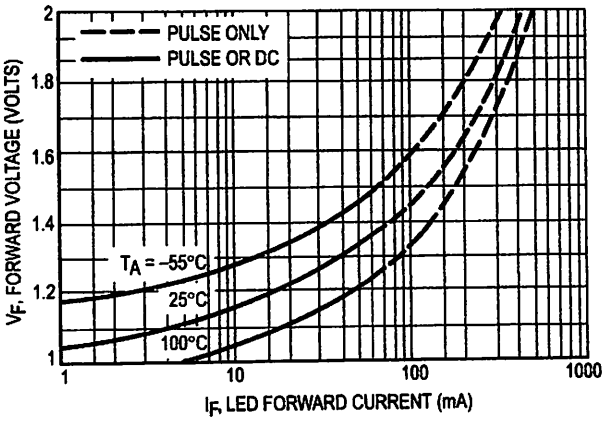



**Figure 1. LED Forward Voltage versus Forward Current**

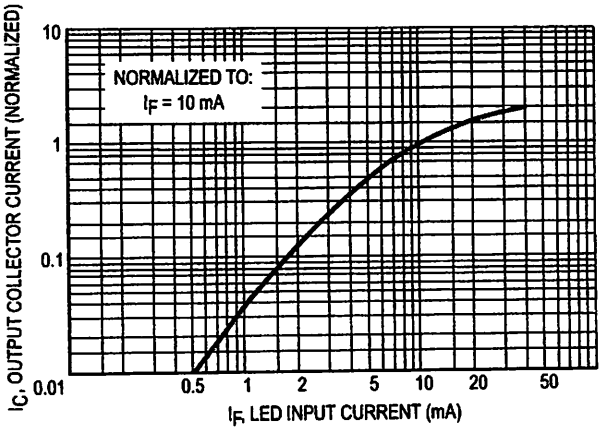



**Figure 2. Output Current versus Input Current**

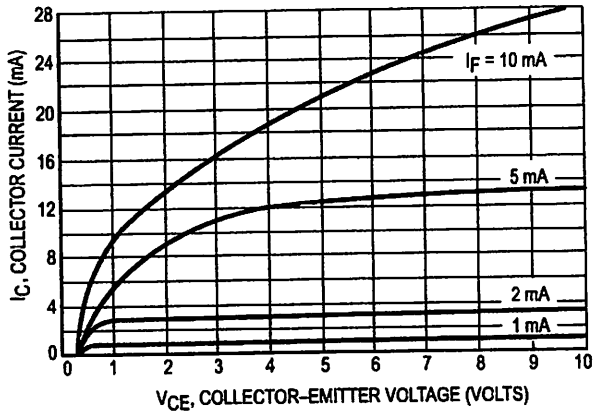



**Figure 3. Collector Current versus Collector–Emitter Voltage**

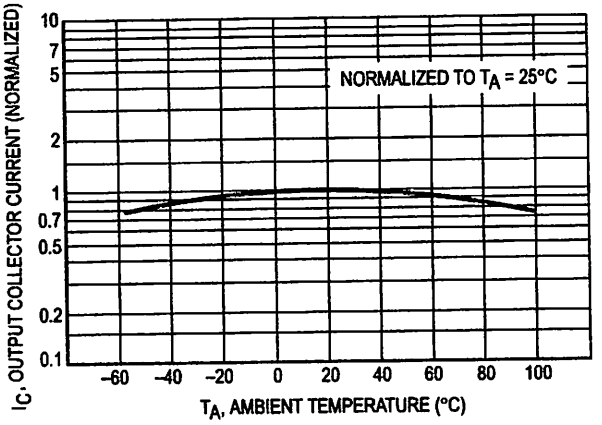



**Figure 4. Output Current versus Ambient Temperature**

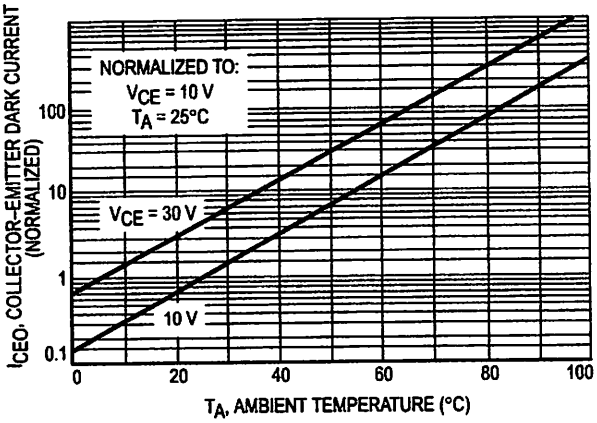



**Figure 5. Dark Current versus Ambient Temperature**

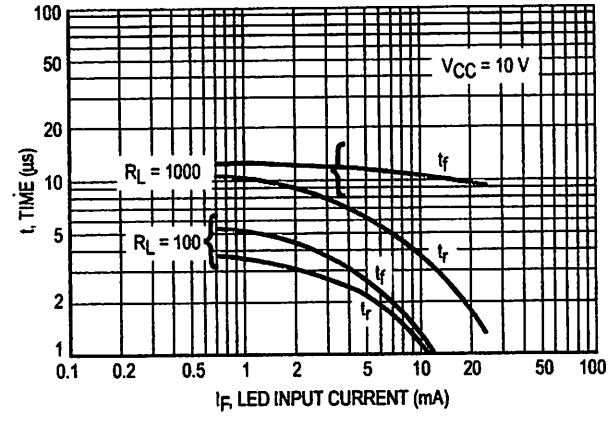



**Figure 6. Rise and Fall Times (Typical Values)**

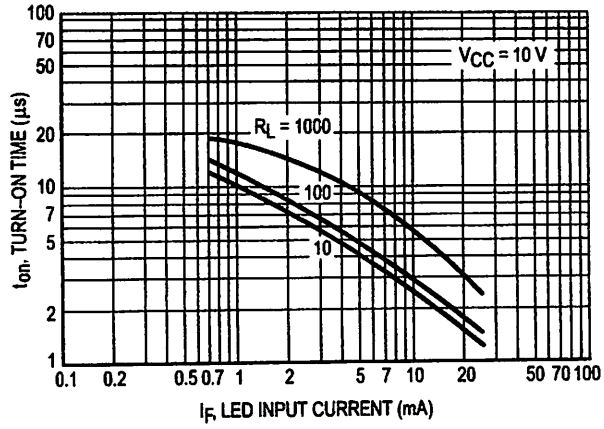



**Figure 7. Turn–On Switching Times (Typical Values)**

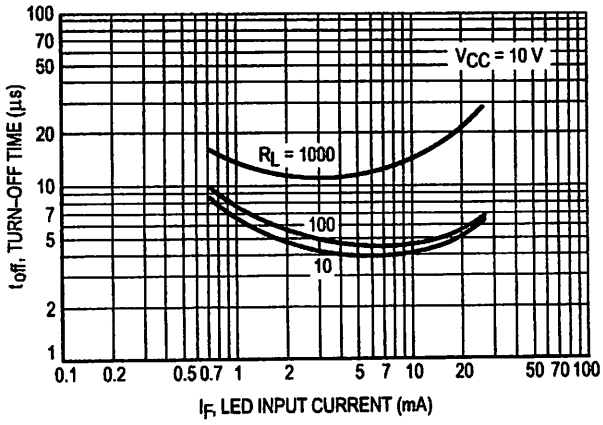



**Figure 8. Turn–Off Switching Times (Typical Values)**

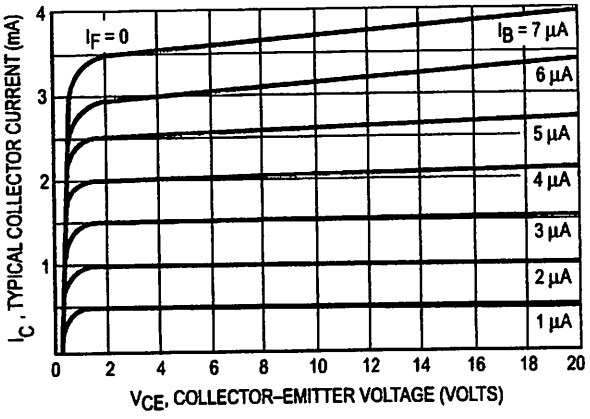



**Figure 9. DC Current Gain (Detector Only)**

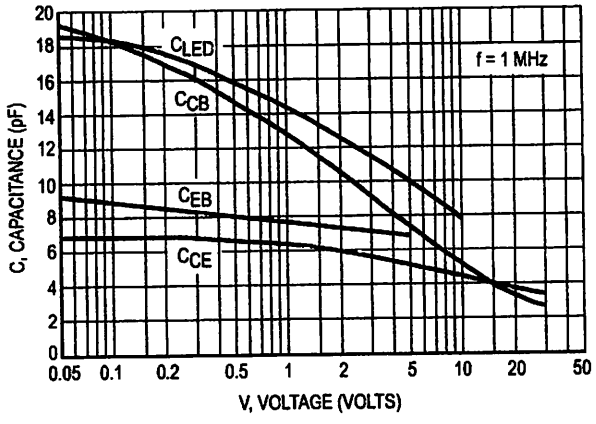



**Figure 10. Capacitances versus Voltage**

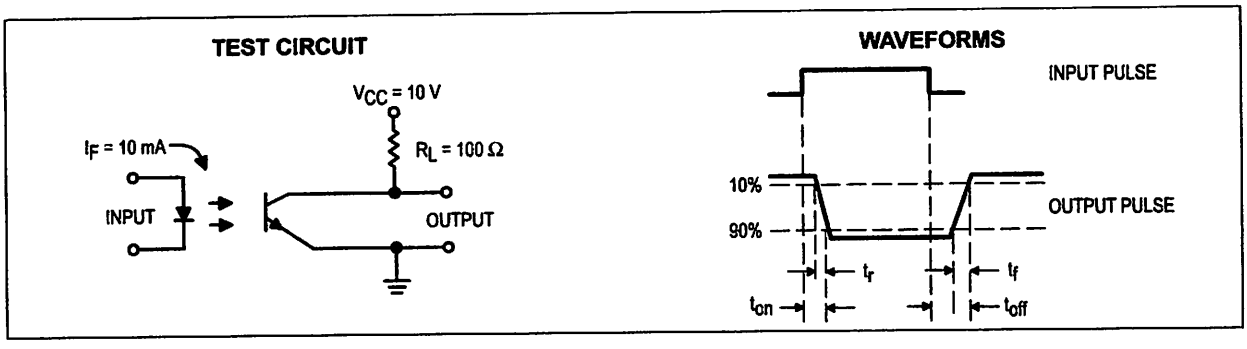



**Figure 11. Switching Time Test Circuit and Waveforms**

## ıtures

ıh-performance, Low-power AVR® 8-bit Microcontroller
vanced RISC Architecture
· 131 Powerful Instructions – Most Single-clock Cycle Execution
· 32 x 8 General Purpose Working Registers
· Fully Static Operation
· Up to 16 MIPS Throughput at 16 MHz
· On-chip 2-cycle Multiplier
nvolatile Program and Data Memories
· 16K Bytes of In-System Self-Programmable Flash
  Endurance: 10,000 Write/Erase Cycles
· Optional Boot Code Section with Independent Lock Bits
  In-System Programming by On-chip Boot Program
  True Read-While-Write Operation
· 512 Bytes EEPROM
  Endurance: 100,000 Write/Erase Cycles
· 1K Byte Internal SRAM
· Programming Lock for Software Security
AG (IEEE std. 1149.1 Compliant) Interface
· Boundary-scan Capabilities According to the JTAG Standard
· Extensive On-chip Debug Support
· Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
ripheral Features
· Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
· One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
· Real Time Counter with Separate Oscillator
· Four PWM Channels
· 8-channel, 10-bit ADC
  8 Single-ended Channels
  7 Differential Channels in TQFP Package Only
  2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
· Byte-oriented Two-wire Serial Interface
· Programmable Serial USART
· Master/Slave SPI Serial Interface
· Programmable Watchdog Timer with Separate On-chip Oscillator
· On-chip Analog Comparator
ıecial Microcontroller Features
· Power-on Reset and Programmable Brown-out Detection
· Internal Calibrated RC Oscillator
· External and Internal Interrupt Sources
· Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
) and Packages
· 32 Programmable I/O Lines
· 40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF
ɔerating Voltages
· 2.7 - 5.5V for ATmega16L
· 4.5 - 5.5V for ATmega16
ɔeed Grades
· 0 - 8 MHz for ATmega16L
· 0 - 16 MHz for ATmega16
ɔwer Consumption @ 1 MHz, 3V, and 25°C for ATmega16L
· Active: 1.1 mA
· Idle Mode: 0.35 mA
· Power-down Mode: < 1 µA

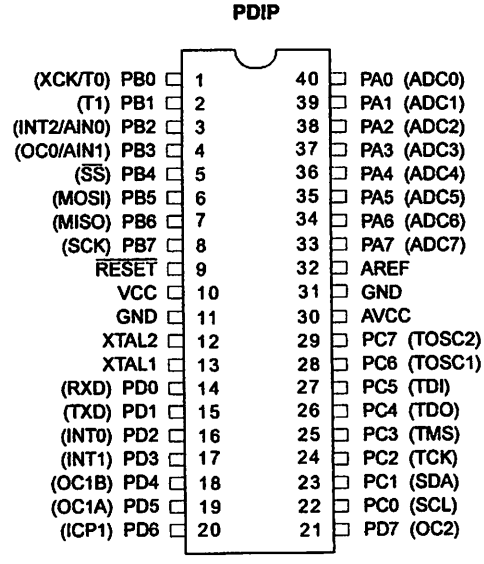
# 8-bit AVR® Microcontroller with 16K Bytes In-System Programmable Flash

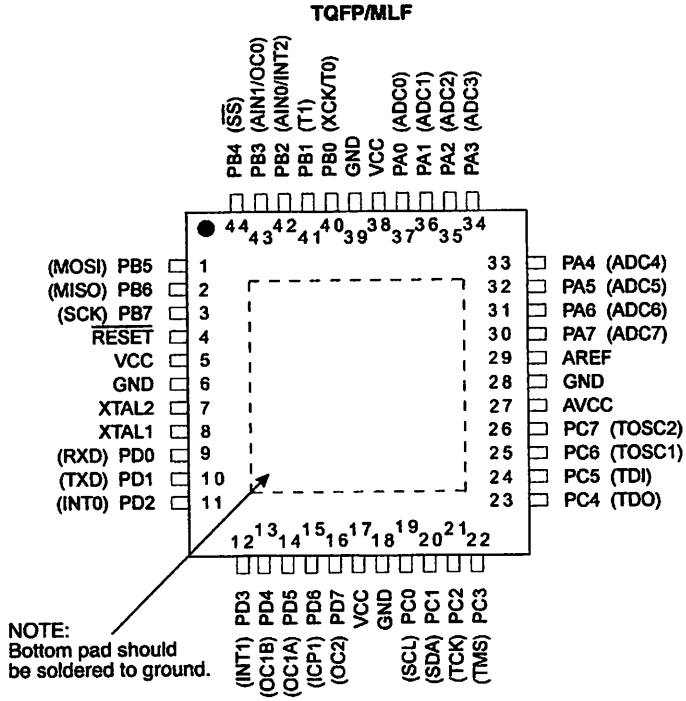
## ATmega16
## ATmega16L

2466L–AVR–06/05

## Configurations

**Figure 1.** Pinout ATmega16




## sclaimer

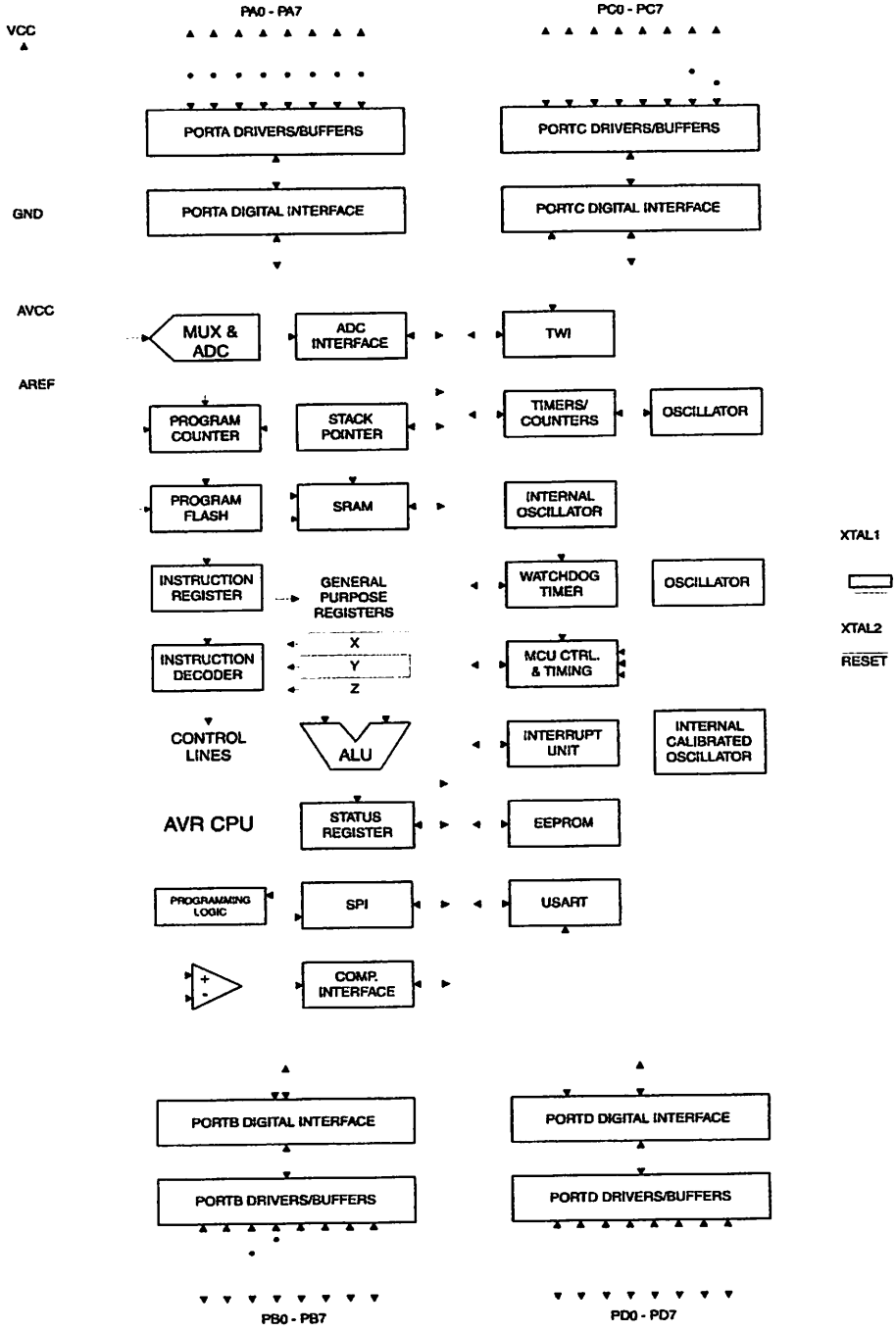
Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

## erview

The ATmega16 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega16 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

## ck Diagram

**Figure 2.** Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega16 provides the following features: 16K bytes of In-System Programmable Flash Program memory with Read-While-Write capabilities, 512 bytes EEPROM, 1K byte SRAM, 32 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary-scan, On-chip Debugging support and programming, three flexible Timer/Counters with compare modes, Internal and External Interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain (TQFP package only), a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the USART, Two-wire interface, A/D Converter, SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next External Interrupt or Hardware Reset. In Power-save mode, the Asynchronous Timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using Atmel's high density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega16 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega16 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

## ı Descriptions

**C**

Digital supply voltage.

**D**

Ground.

**rt A (PA7..PA0)**

Port A serves as the analog inputs to the A/D Converter.

Port A also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

**B (PB7..PB0)**

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega16 as listed on page 56.

**C (PC7..PC0)**

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PC5(TDI), PC3(TMS) and PC2(TCK) will be activated even if a reset occurs.

Port C also serves the functions of the JTAG interface and other special features of the ATmega16 as listed on page 59.

**D (PD7..PD0)**

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega16 as listed on page 61.

**SET**

Reset Input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 36. Shorter pulses are not guaranteed to generate a reset.

**AL1**

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

**AL2**

Output from the inverting Oscillator amplifier.

**CC**

AVCC is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to $V_{CC}$, even if the ADC is not used. If the ADC is used, it should be connected to $V_{CC}$ through a low-pass filter.

**EF**

AREF is the analog reference pin for the A/D Converter.

## esources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

## out Code amples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C Compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C Compiler documentation for more details.

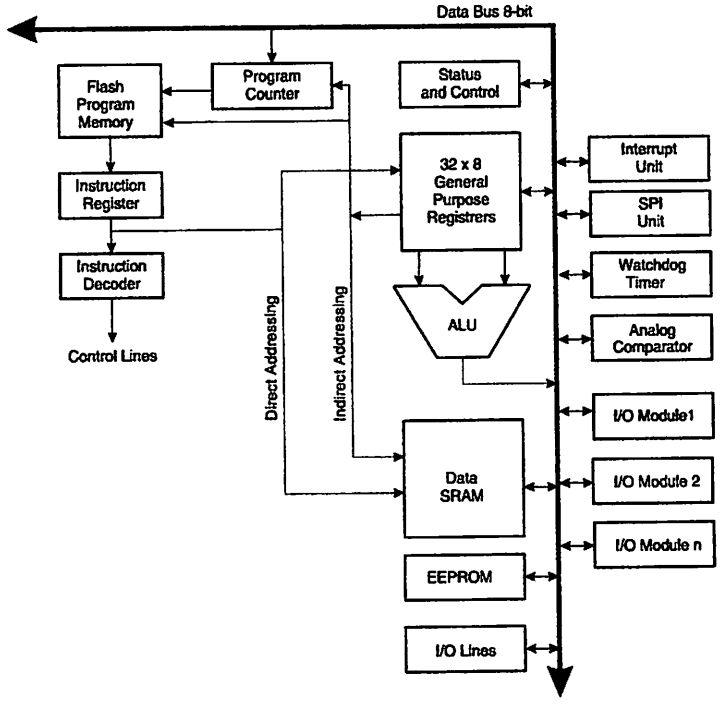
# R CPU Core

## oduction

This section discusses the AVR core architecture in general. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations, control peripherals, and handle interrupts.

## hitectural Overview

**Figure 3.** Block Diagram of the AVR MCU Architecture




In order to maximize performance and parallelism, the AVR uses a Harvard architecture – with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Reprogrammable Flash memory.

The fast-access Register File contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing – enabling efficient address calculations. One of the these address pointers can also be used as an address pointer for look up tables in Flash Program memory. These added function registers are the 16-bit X-, Y-, and Z-register, described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After

an arithmetic operation, the Status Register is updated to reflect information about the result of the operation.

Program flow is provided by conditional and unconditional jump and call instructions, able to directly address the whole address space. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

Program Flash memory space is divided in two sections, the Boot program section and the Application Program section. Both sections have dedicated Lock bits for write and read/write protection. The SPM instruction that writes into the Application Flash memory section must reside in the Boot Program section.

During interrupts and subroutine calls, the return address Program Counter (PC) is stored on the Stack. The Stack is effectively allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The Stack Pointer SP is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the Status Register. All interrupts have a separate interrupt vector in the interrupt vector table. The interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, SPI, and other I/O functions. The I/O Memory can be accessed directly, or as the Data Space locations following those of the Register File, $20 - $5F.

## U – Arithmetic Logic it

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed. The ALU operations are divided into three main categories – arithmetic, logical, and bit-functions. Some implementations of the architecture also provide a powerful multiplier supporting both signed/unsigned multiplication and fractional format. See the "Instruction Set" section for a detailed description.

## ıtus Register

The Status Register contains information about the result of the most recently executed arithmetic instruction. This information can be used for altering program flow in order to perform conditional operations. Note that the Status Register is updated after all ALU operations, as specified in the Instruction Set Reference. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt. This must be handled by software.

The AVR Status Register – SREG – is defined as:

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | I | T | H | S | V | N | Z | C | SREG |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bit 7 – I: Global Interrupt Enable**

The Global Interrupt Enable bit must be set for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers. If the Global Interrupt Enable Register is cleared, none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred, and is set by the RETI instruction to enable subsequent interrupts. The I-bit can also be set and cleared by the application with the SEI and CLI instructions, as described in the instruction set reference.

- **Bit 6 – T: Bit Copy Storage**

The Bit Copy instructions BLD (Bit LoaD) and BST (Bit STore) use the T-bit as source or destination for the operated bit. A bit from a register in the Register File can be copied into T by the BST instruction, and a bit in T can be copied into a bit in a register in the Register File by the BLD instruction.

- **Bit 5 – H: Half Carry Flag**

The Half Carry Flag H indicates a Half Carry in some arithmetic operations. Half Carry is useful in BCD arithmetic. See the "Instruction Set Description" for detailed information.

- **Bit 4 – S: Sign Bit, $S = N \oplus V$**

The S-bit is always an exclusive or between the Negative Flag N and the Two's Complement Overflow Flag V. See the "Instruction Set Description" for detailed information.

- **Bit 3 – V: Two's Complement Overflow Flag**

The Two's Complement Overflow Flag V supports two's complement arithmetics. See the "Instruction Set Description" for detailed information.

- **Bit 2 – N: Negative Flag**

The Negative Flag N indicates a negative result in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

- **Bit 1 – Z: Zero Flag**

The Zero Flag Z indicates a zero result in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

- **Bit 0 – C: Carry Flag**

The Carry Flag C indicates a carry in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

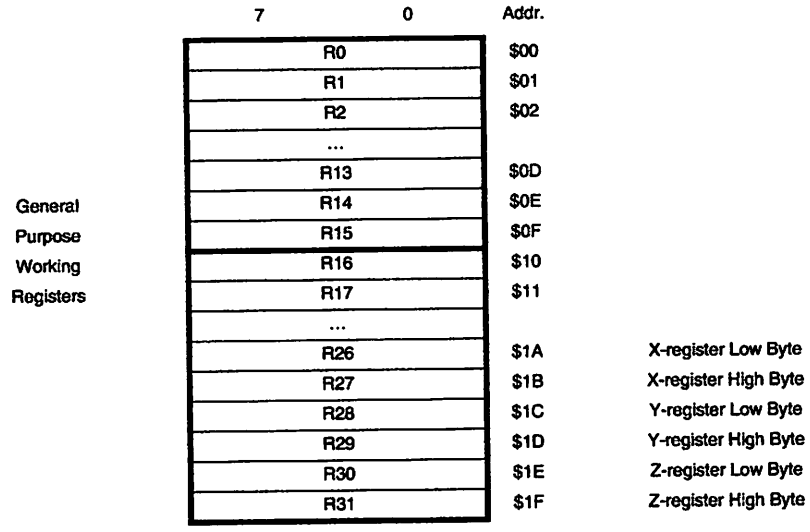
## ıeral Purpose ;ister File

The Register File is optimized for the AVR Enhanced RISC instruction set. In order to achieve the required performance and flexibility, the following input/output schemes are supported by the Register File:

- One 8-bit output operand and one 8-bit result input
- Two 8-bit output operands and one 16-bit result input
- Two 8-bit output operands and one 16-bit result input
- One 16-bit output operand and one 16-bit result input

Figure 4 shows the structure of the 32 general purpose working registers in the CPU.

**Figure 4.** AVR CPU General Purpose Working Registers



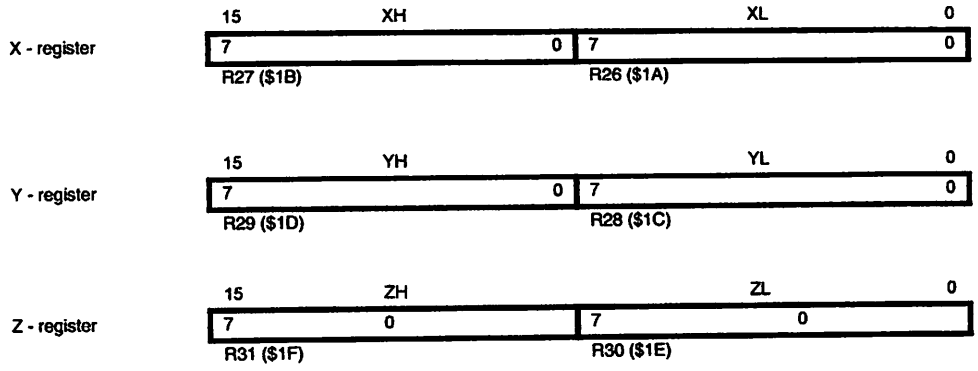

Most of the instructions operating on the Register File have direct access to all registers, and most of them are single cycle instructions.

As shown in Figure 4, each register is also assigned a data memory address, mapping them directly into the first 32 locations of the user Data Space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y-, and Z-pointer Registers can be set to index any register in the file.

### X-register, Y-register and gister

The registers R26..R31 have some added functions to their general purpose usage. These registers are 16-bit address pointers for indirect addressing of the Data Space. The three indirect address registers X, Y, and Z are defined as described in Figure 5.

**Figure 5.** The X-, Y-, and Z-registers




In the different addressing modes these address registers have functions as fixed displacement, automatic increment, and automatic decrement (see the Instruction Set Reference for details).

### ıck Pointer

The Stack is mainly used for storing temporary data, for storing local variables and for storing return addresses after interrupts and subroutine calls. The Stack Pointer Register always points to the top of the Stack. Note that the Stack is implemented as growing from higher memory locations to lower memory locations. This implies that a Stack PUSH command decreases the Stack Pointer. If software reads the Program Counter from the Stack after a call or an interrupt, unused bits (15:13) should be masked out.

The Stack Pointer points to the data SRAM Stack area where the Subroutine and Interrupt Stacks are located. This Stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. The Stack Pointer must be set to point above $60. The Stack Pointer is decremented by one when data is pushed onto the Stack with the PUSH instruction, and it is decremented by two when the return address is pushed onto the Stack with subroutine call or interrupt. The Stack Pointer is incremented by one when data is popped from the Stack with the POP instruction, and it is incremented by two when data is popped from the Stack with return from subroutine RET or return from interrupt RETI.

The AVR Stack Pointer is implemented as two 8-bit registers in the I/O space. The number of bits actually used is implementation dependent. Note that the data space in some implementations of the AVR architecture is so small that only SPL is needed. In this case, the SPH Register will not be present.

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
|---|---|---|---|---|---|---|---|---|---|
| | SP15 | SP14 | SP13 | SP12 | SP11 | SP10 | SP9 | SP8 | SPH |
| | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | SPL |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

## truction Execution ning

This section describes the general access timing concepts for instruction execution. The AVR CPU is driven by the CPU clock $clk_{CPU}$, directly generated from the selected clock source for the chip. No internal clock division is used.

Figure 6 shows the parallel instruction fetches and instruction executions enabled by the Harvard architecture and the fast-access Register File concept. This is the basic pipelining concept to obtain up to 1 MIPS per MHz with the corresponding unique results for functions per cost, functions per clocks, and functions per power-unit.

**Figure 6.** The Parallel Instruction Fetches and Instruction Executions

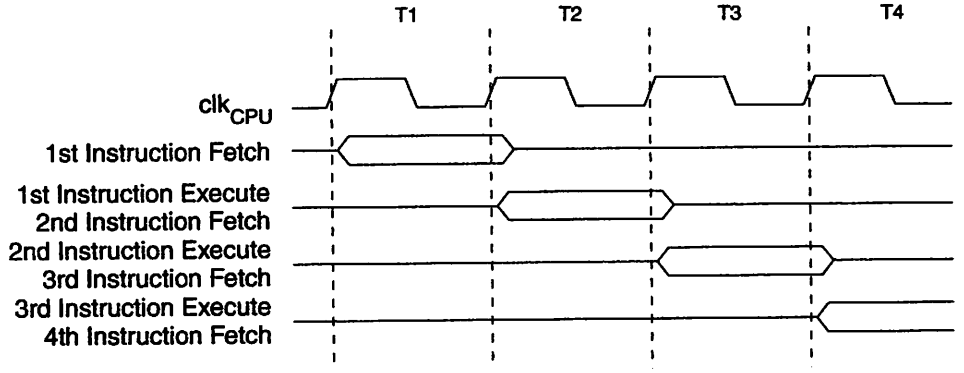
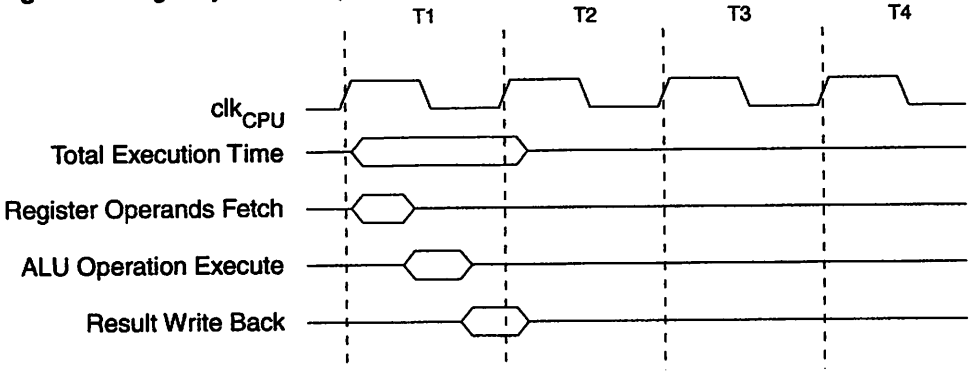



Figure 7 shows the internal timing concept for the Register File. In a single clock cycle an ALU operation using two register operands is executed, and the result is stored back to the destination register.

**Figure 7.** Single Cycle ALU Operation




## set and Interrupt ndling

The AVR provides several different interrupt sources. These interrupts and the separate reset vector each have a separate program vector in the program memory space. All interrupts are assigned individual enable bits which must be written logic one together with the Global Interrupt Enable bit in the Status Register in order to enable the interrupt. Depending on the Program Counter value, interrupts may be automatically disabled when Boot Lock bits BLB02 or BLB12 are programmed. This feature improves software security. See the section "Memory Programming" on page 259 for details.

The lowest addresses in the program memory space are by default defined as the Reset and Interrupt Vectors. The complete list of vectors is shown in "Interrupts" on page 43. The list also determines the priority levels of the different interrupts. The lower the address the higher is the priority level. RESET has the highest priority, and next is INT0

– the External Interrupt Request 0. The Interrupt Vectors can be moved to the start of the Boot Flash section by setting the IVSEL bit in the General Interrupt Control Register (GICR). Refer to "Interrupts" on page 43 for more information. The Reset Vector can also be moved to the start of the boot Flash section by programming the BOOTRST Fuse, see "Boot Loader Support – Read-While-Write Self-Programming" on page 246.

When an interrupt occurs, the Global Interrupt Enable I-bit is cleared and all interrupts are disabled. The user software can write logic one to the I-bit to enable nested interrupts. All enabled interrupts can then interrupt the current interrupt routine. The I-bit is automatically set when a Return from Interrupt instruction – RETI – is executed.

There are basically two types of interrupts. The first type is triggered by an event that sets the Interrupt Flag. For these interrupts, the Program Counter is vectored to the actual Interrupt Vector in order to execute the interrupt handling routine, and hardware clears the corresponding Interrupt Flag. Interrupt Flags can also be cleared by writing a logic one to the flag bit position(s) to be cleared. If an interrupt condition occurs while the corresponding interrupt enable bit is cleared, the Interrupt Flag will be set and remembered until the interrupt is enabled, or the flag is cleared by software. Similarly, if one or more interrupt conditions occur while the Global Interrupt Enable bit is cleared, the corresponding Interrupt Flag(s) will be set and remembered until the global interrupt enable bit is set, and will then be executed by order of priority.

The second type of interrupts will trigger as long as the interrupt condition is present. These interrupts do not necessarily have Interrupt Flags. If the interrupt condition disappears before the interrupt is enabled, the interrupt will not be triggered.

When the AVR exits from an interrupt, it will always return to the main program and execute one more instruction before any pending interrupt is served.

Note that the Status Register is not automatically stored when entering an interrupt routine, nor restored when returning from an interrupt routine. This must be handled by software.

When using the CLI instruction to disable interrupts, the interrupts will be immediately disabled. No interrupt will be executed after the CLI instruction, even if it occurs simultaneously with the CLI instruction. The following example shows how this can be used to avoid interrupts during the timed EEPROM write sequence.

Assembly Code Example

```
in  r16, SREG      ; store SREG value
cli    ; disable interrupts during timed sequence
sbi EECR, EEMWE    ; start EEPROM write
sbi EECR, EEWE
out SREG, r16      ; restore SREG value (I-bit)
```

C Code Example

```
char cSREG;
cSREG = SREG;  /* store SREG value */
/* disable interrupts during timed sequence */
_CLI();
EECR |= (1<<EEMWE); /* start EEPROM write */
EECR |= (1<<EEWE);
SREG = cSREG; /* restore SREG value (I-bit) */
```

When using the SEI instruction to enable interrupts, the instruction following SEI will be executed before any pending interrupts, as shown in this example.

Assembly Code Example

```
sei   ; set global interrupt enable
sleep ; enter sleep, waiting for interrupt
; note: will enter sleep before any pending
; interrupt(s)
```

C Code Example

```
_SEI(); /* set global interrupt enable */
_SLEEP(); /* enter sleep, waiting for interrupt */
/* note: will enter sleep before any pending interrupt(s) */
```

### ɪrrupt Response Time

The interrupt execution response for all the enabled AVR interrupts is four clock cycles minimum. After four clock cycles the program vector address for the actual interrupt handling routine is executed. During this four clock cycle period, the Program Counter is pushed onto the Stack. The vector is normally a jump to the interrupt routine, and this jump takes three clock cycles. If an interrupt occurs during execution of a multi-cycle instruction, this instruction is completed before the interrupt is served. If an interrupt occurs when the MCU is in sleep mode, the interrupt execution response time is increased by four clock cycles. This increase comes in addition to the start-up time from the selected sleep mode.

A return from an interrupt handling routine takes four clock cycles. During these four clock cycles, the Program Counter (two bytes) is popped back from the Stack, the Stack Pointer is incremented by two, and the I-bit in SREG is set.

## R ATmega16 mories

This section describes the different memories in the ATmega16. The AVR architecture has two main memory spaces, the Data Memory and the Program Memory space. In addition, the ATmega16 features an EEPROM Memory for data storage. All three memory spaces are linear and regular.

## System programmable Flash gram Memory

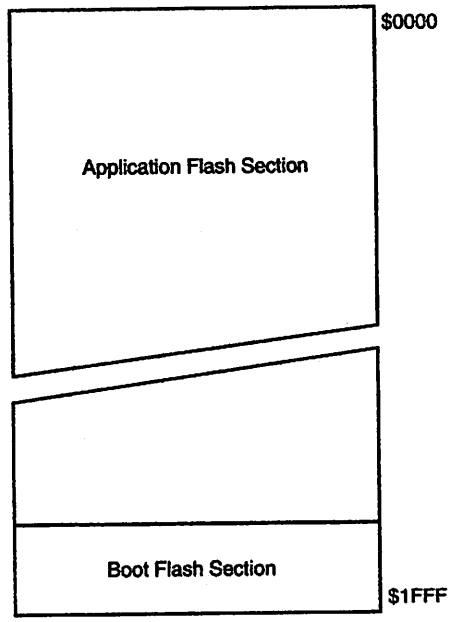
The ATmega16 contains 16K bytes On-chip In-System Reprogrammable Flash memory for program storage. Since all AVR instructions are 16 or 32 bits wide, the Flash is organized as 8K x 16. For software security, the Flash Program memory space is divided into two sections, Boot Program section and Application Program section.

The Flash memory has an endurance of at least 10,000 write/erase cycles. The ATmega16 Program Counter (PC) is 13 bits wide, thus addressing the 8K program memory locations. The operation of Boot Program section and associated Boot Lock bits for software protection are described in detail in "Boot Loader Support – Read-While-Write Self-Programming" on page 246. "Memory Programming" on page 259 contains a detailed description on Flash data serial downloading using the SPI pins or the JTAG interface.

Constant tables can be allocated within the entire program memory address space (see the LPM – Load Program Memory Instruction Description).

Timing diagrams for instruction fetch and execution are presented in "Instruction Execution Timing" on page 11.

**Figure 8.** Program Memory Map



## AM Data Memory

Figure 9 shows how the ATmega16 SRAM Memory is organized.

The lower 1120 Data Memory locations address the Register File, the I/O Memory, and the internal data SRAM. The first 96 locations address the Register File and I/O Memory, and the next 1024 locations address the internal data SRAM.

The five different addressing modes for the data memory cover: Direct, Indirect with Displacement, Indirect, Indirect with Pre-decrement, and Indirect with Post-increment. In the Register File, registers R26 to R31 feature the indirect addressing pointer registers.

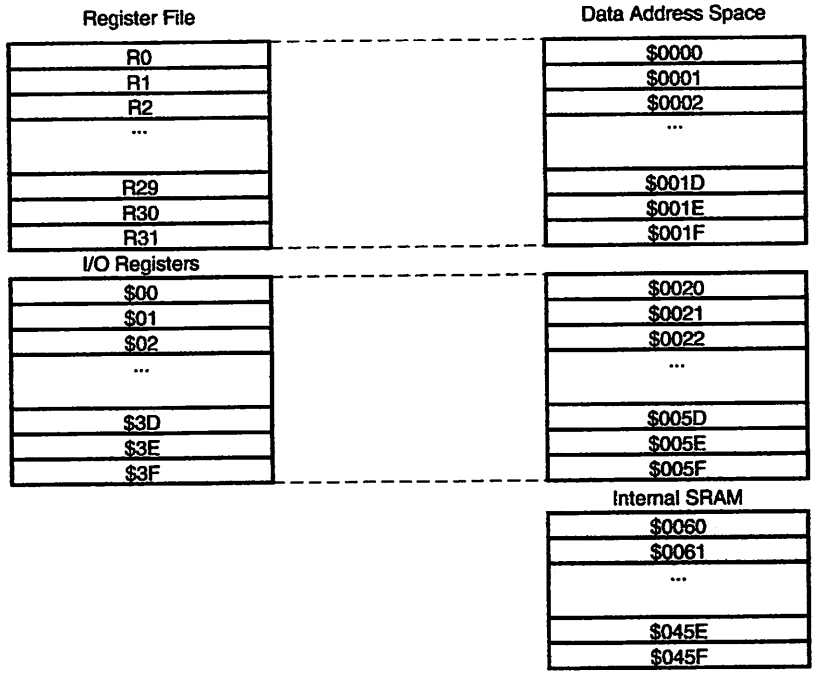
The direct addressing reaches the entire data space.

The Indirect with Displacement mode reaches 63 address locations from the base address given by the Y- or Z-register.

When using register indirect addressing modes with automatic pre-decrement and post-increment, the address registers X, Y, and Z are decremented or incremented.

The 32 general purpose working registers, 64 I/O Registers, and the 1024 bytes of internal data SRAM in the ATmega16 are all accessible through all these addressing modes. The Register File is described in "General Purpose Register File" on page 9.

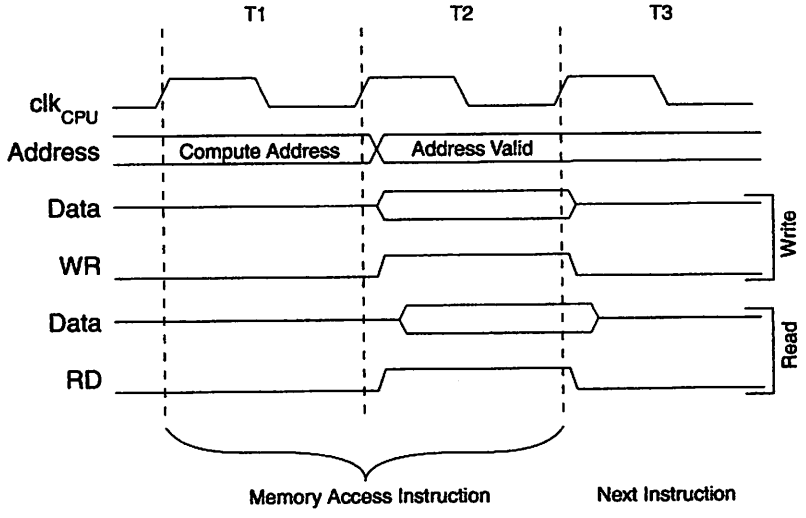
**Figure 9.** Data Memory Map



### a Memory Access Times

This section describes the general access timing concepts for internal memory access. The internal data SRAM access is performed in two $clk_{CPU}$ cycles as described in Figure 10.

**Figure 10.** On-chip Data SRAM Access Cycles




### :PROM Data Memory

The ATmega16 contains 512 bytes of data EEPROM memory. It is organized as a separate data space, in which single bytes can be read and written. The EEPROM has an endurance of at least 100,000 write/erase cycles. The access between the EEPROM and the CPU is described in the following, specifying the EEPROM Address Registers, the EEPROM Data Register, and the EEPROM Control Register.

For a detailed description of SPI, JTAG, and Parallel data downloading to the EEPROM, see page 273, page 278, and page 262, respectively.

### PROM Read/Write Access

The EEPROM Access Registers are accessible in the I/O space.

The write access time for the EEPROM is given in Table 1. A self-timing function, however, lets the user software detect when the next byte can be written. If the user code contains instructions that write the EEPROM, some precautions must be taken. In heavily filtered power supplies, $V_{CC}$ is likely to rise or fall slowly on Power-up/down. This causes the device for some period of time to run at a voltage lower than specified as minimum for the clock frequency used. See "Preventing EEPROM Corruption" on page 20 for details on how to avoid problems in these situations.

In order to prevent unintentional EEPROM writes, a specific write procedure must be followed. Refer to the description of the EEPROM Control Register for details on this.

When the EEPROM is read, the CPU is halted for four clock cycles before the next instruction is executed. When the EEPROM is written, the CPU is halted for two clock cycles before the next instruction is executed.

### EEPROM Address Register – EEARH and EEARL

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
|---|---|---|---|---|---|---|---|---|---|
| | – | – | – | – | – | – | – | EEAR8 | EEARH |
| | EEAR7 | EEAR6 | EEAR5 | EEAR4 | EEAR3 | EEAR2 | EEAR1 | EEAR0 | EEARL |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Read/Write | R | R | R | R | R | R | R | R/W | |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | |
| | X | X | X | X | X | X | X | X | |

- **Bits 15..9 – Res: Reserved Bits**

These bits are reserved bits in the ATmega16 and will always read as zero.

- **Bits 8..0 – EEAR8..0: EEPROM Address**

The EEPROM Address Registers – EEARH and EEARL – specify the EEPROM address in the 512 bytes EEPROM space. The EEPROM data bytes are addressed linearly between 0 and 511. The initial value of EEAR is undefined. A proper value must be written before the EEPROM may be accessed.

### EEPROM Data Register – EEDR

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | MSB | | | | | | | LSB | EEDR |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bits 7..0 – EEDR7.0: EEPROM Data**

For the EEPROM write operation, the EEDR Register contains the data to be written to the EEPROM in the address given by the EEAR Register. For the EEPROM read operation, the EEDR contains the data read out from the EEPROM at the address given by EEAR.

### EEPROM Control Register EECR

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | – | – | – | – | EERIE | EEMWE | EEWE | EERE | EECR |
| Read/Write | R | R | R | R | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | |

- **Bits 7..4 – Res: Reserved Bits**

These bits are reserved bits in the ATmega16 and will always read as zero.

- **Bit 3 – EERIE: EEPROM Ready Interrupt Enable**

Writing EERIE to one enables the EEPROM Ready Interrupt if the I bit in SREG is set. Writing EERIE to zero disables the interrupt. The EEPROM Ready interrupt generates a constant interrupt when EEWE is cleared.

- **Bit 2 – EEMWE: EEPROM Master Write Enable**

The EEMWE bit determines whether setting EEWE to one causes the EEPROM to be written. When EEMWE is set, setting EEWE within four clock cycles will write data to the EEPROM at the selected address If EEMWE is zero, setting EEWE will have no effect.

When EEMWE has been written to one by software, hardware clears the bit to zero after four clock cycles. See the description of the EEWE bit for an EEPROM write procedure.

- **Bit 1 – EEWE: EEPROM Write Enable**

The EEPROM Write Enable Signal EEWE is the write strobe to the EEPROM. When address and data are correctly set up, the EEWE bit must be written to one to write the value into the EEPROM. The EEMWE bit must be written to one before a logical one is written to EEWE, otherwise no EEPROM write takes place. The following procedure should be followed when writing the EEPROM (the order of steps 3 and 4 is not essential):

1. Wait until EEWE becomes zero.
2. Wait until SPMEN in SPMCR becomes zero.
3. Write new EEPROM address to EEAR (optional).
4. Write new EEPROM data to EEDR (optional).
5. Write a logical one to the EEMWE bit while writing a zero to EEWE in EECR.
6. Within four clock cycles after setting EEMWE, write a logical one to EEWE.

The EEPROM can not be programmed during a CPU write to the Flash memory. The software must check that the Flash programming is completed before initiating a new EEPROM write. Step 2 is only relevant if the software contains a Boot Loader allowing the CPU to program the Flash. If the Flash is never being updated by the CPU, step 2 can be omitted. See "Boot Loader Support – Read-While-Write Self-Programming" on page 246 for details about boot programming.

Caution: An interrupt between step 5 and step 6 will make the write cycle fail, since the EEPROM Master Write Enable will time-out. If an interrupt routine accessing the EEPROM is interrupting another EEPROM Access, the EEAR or EEDR reGister will be modified, causing the interrupted EEPROM Access to fail. It is recommended to have the Global Interrupt Flag cleared during all the steps to avoid these problems.

When the write access time has elapsed, the EEWE bit is cleared by hardware. The user software can poll this bit and wait for a zero before writing the next byte. When EEWE has been set, the CPU is halted for two cycles before the next instruction is executed.

- **Bit 0 – EERE: EEPROM Read Enable**

The EEPROM Read Enable Signal – EERE – is the read strobe to the EEPROM. When the correct address is set up in the EEAR Register, the EERE bit must be written to a logic one to trigger the EEPROM read. The EEPROM read access takes one instruction, and the requested data is available immediately. When the EEPROM is read, the CPU is halted for four cycles before the next instruction is executed.

The user should poll the EEWE bit before starting the read operation. If a write operation is in progress, it is neither possible to read the EEPROM, nor to change the EEAR Register.

The calibrated Oscillator is used to time the EEPROM accesses. Table 1 lists the typical programming time for EEPROM access from the CPU.

**Table 1.** EEPROM Programming Time

| Symbol | Number of Calibrated RC Oscillator Cycles[1] | Typ Programming Time |
|---|---|---|
| EEPROM write (from CPU) | 8448 | 8.5 ms |

Note: 1. Uses 1 MHz clock, independent of CKSEL Fuse setting.

The following code examples show one assembly and one C function for writing to the EEPROM. The examples assume that interrupts are controlled (for example by disabling interrupts globally) so that no interrupts will occur during execution of these functions. The examples also assume that no Flash Boot Loader is present in the software. If such code is present, the EEPROM write function must also wait for any ongoing SPM command to finish.

**Assembly Code Example**

```
EEPROM_write:
  ; Wait for completion of previous write
  sbic EECR,EEWE
  rjmp EEPROM_write
  ; Set up address (r18:r17) in address register
  out  EEARH, r18
  out  EEARL, r17
  ; Write data (r16) to data register
  out  EEDR,r16
  ; Write logical one to EEMWE
  sbi  EECR,EEMWE
  ; Start eeprom write by setting EEWE
  sbi  EECR,EEWE
  ret
```

**C Code Example**

```
void EEPROM_write(unsigned int uiAddress, unsigned char ucData)
{
  /* Wait for completion of previous write */
  while(EECR & (1<<EEWE))
    ;
  /* Set up address and data registers */
  EEAR = uiAddress;
  EEDR = ucData;
  /* Write logical one to EEMWE */
  EECR |= (1<<EEMWE);
  /* Start eeprom write by setting EEWE */
  EECR |= (1<<EEWE);
}
```

The next code examples show assembly and C functions for reading the EEPROM. The examples assume that interrupts are controlled so that no interrupts will occur during execution of these functions.

Assembly Code Example

```
EEPROM_read:
  ; Wait for completion of previous write
  sbic EECR,EEWE
  rjmp EEPROM_read
  ; Set up address (r18:r17) in address register
  out  EEARH, r18
  out  EEARL, r17
  ; Start eeprom read by writing EERE
  sbi  EECR,EERE
  ; Read data from data register
  in   r16,EEDR
  ret
```

C Code Example

```
unsigned char EEPROM_read(unsigned int uiAddress)
{
  /* Wait for completion of previous write */
  while(EECR & (1<<EEWE))
    ;
  /* Set up address register */
  EEAR = uiAddress;
  /* Start eeprom read by writing EERE */
  EECR |= (1<<EERE);
  /* Return data from data register */
  return EEDR;
}
```

**PROM Write During Power-wn Sleep Mode**

When entering Power-down Sleep mode while an EEPROM write operation is active, the EEPROM write operation will continue, and will complete before the Write Access time has passed. However, when the write operation is completed, the Oscillator continues running, and as a consequence, the device does not enter Power-down entirely. It is therefore recommended to verify that the EEPROM write operation is completed before entering Power-down.

**:venting EEPROM rruption**

During periods of low $V_{CC}$, the EEPROM data can be corrupted because the supply voltage is too low for the CPU and the EEPROM to operate properly. These issues are the same as for board level systems using EEPROM, and the same design solutions should be applied.

An EEPROM data corruption can be caused by two situations when the voltage is too low. First, a regular write sequence to the EEPROM requires a minimum voltage to operate correctly. Secondly, the CPU itself can execute instructions incorrectly, if the supply voltage is too low.

EEPROM data corruption can easily be avoided by following this design recommendation:

Keep the AVR RESET active (low) during periods of insufficient power supply voltage. This can be done by enabling the internal Brown-out Detector (BOD). If the detection level of the internal BOD does not match the needed detection level, an external low $V_{CC}$ Reset Protection circuit can be used. If a reset occurs while a write operation is in progress, the write operation will be completed provided that the power supply voltage is sufficient.

## Memory

The I/O space definition of the ATmega16 is shown in "Register Summary" on page 331.

All ATmega16 I/Os and peripherals are placed in the I/O space. The I/O locations are accessed by the IN and OUT instructions, transferring data between the 32 general purpose working registers and the I/O space. I/O Registers within the address range $00 - $1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Refer to the Instruction Set section for more details. When using the I/O specific commands IN and OUT, the I/O addresses $00 - $3F must be used. When addressing I/O Registers as data space using LD and ST instructions, $20 must be added to these addresses.

For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

Some of the Status Flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

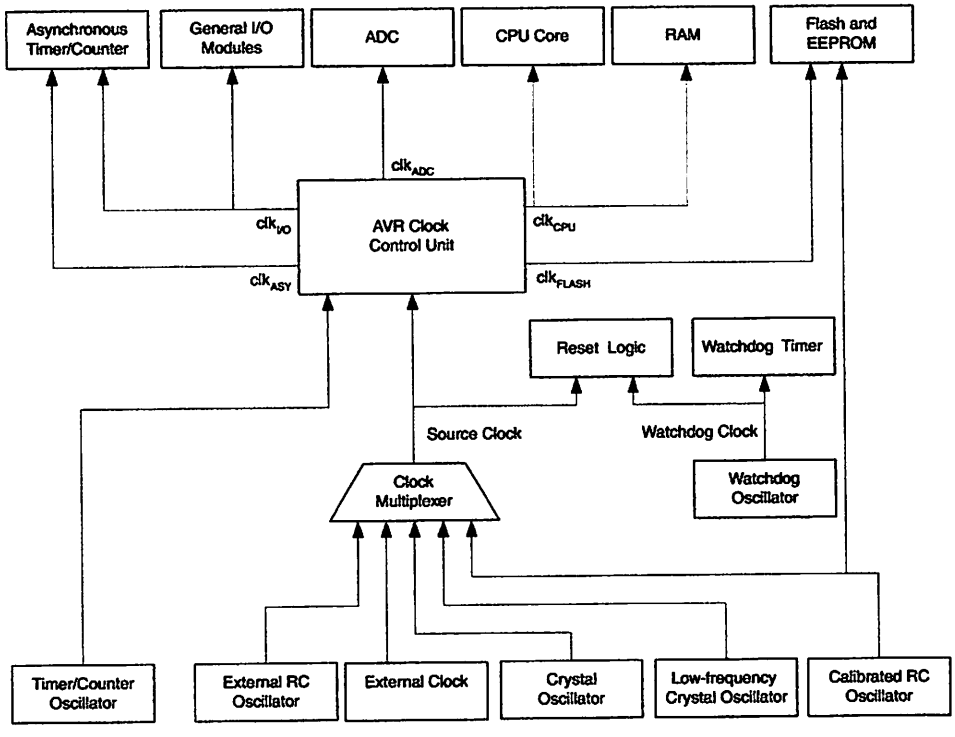
The I/O and Peripherals Control Registers are explained in later sections.

# stem Clock and ɔck Options

## ıck Systems and their ıtribution

Figure 11 presents the principal clock systems in the AVR and their distribution. All of the clocks need not be active at a given time. In order to reduce power consumption, the clocks to modules not being used can be halted by using different sleep modes, as described in "Power Management and Sleep Modes" on page 30. The clock systems are detailed Figure 11.

**Figure 11.** Clock Distribution




### U Clock – $clk_{CPU}$

The CPU clock is routed to parts of the system concerned with operation of the AVR core. Examples of such modules are the General Purpose Register File, the Status Register and the data memory holding the Stack Pointer. Halting the CPU clock inhibits the core from performing general operations and calculations.

### Clock – $clk_{I/O}$

The I/O clock is used by the majority of the I/O modules, like Timer/Counters, SPI, and USART. The I/O clock is also used by the External Interrupt module, but note that some external interrupts are detected by asynchronous logic, allowing such interrupts to be detected even if the I/O clock is halted. Also note that address recognition in the TWI module is carried out asynchronously when $clk_{I/O}$ is halted, enabling TWI address reception in all sleep modes.

### ısh Clock – $clk_{FLASH}$

The Flash clock controls operation of the Flash interface. The Flash clock is usually active simultaneously with the CPU clock.

**nchronous Timer Clock – sy**

The Asynchronous Timer clock allows the Asynchronous Timer/Counter to be clocked directly from an external 32 kHz clock crystal. The dedicated clock domain allows using this Timer/Counter as a real-time counter even when the device is in sleep mode.

**C Clock – $clk_{ADC}$**

The ADC is provided with a dedicated clock domain. This allows halting the CPU and I/O clocks in order to reduce noise generated by digital circuitry. This gives more accurate ADC conversion results.

## ock Sources

The device has the following clock source options, selectable by Flash Fuse bits as shown below. The clock from the selected source is input to the AVR clock generator, and routed to the appropriate modules.

**Table 2.** Device Clocking Options Select(1)

| Device Clocking Option | CKSEL3..0 |
|---|---|
| External Crystal/Ceramic Resonator | 1111 - 1010 |
| External Low-frequency Crystal | 1001 |
| External RC Oscillator | 1000 - 0101 |
| Calibrated Internal RC Oscillator | 0100 - 0001 |
| External Clock | 0000 |

Note: 1. For all fuses "1" means unprogrammed while "0" means programmed.

The various choices for each clocking option is given in the following sections. When the CPU wakes up from Power-down or Power-save, the selected clock source is used to time the start-up, ensuring stable Oscillator operation before instruction execution starts. When the CPU starts from Reset, there is as an additional delay allowing the power to reach a stable level before commencing normal operation. The Watchdog Oscillator is used for timing this real-time part of the start-up time. The number of WDT Oscillator cycles used for each time-out is shown in Table 3. The frequency of the Watchdog Oscillator is voltage dependent as shown in "ATmega16 Typical Characteristics" on page 299.

**Table 3.** Number of Watchdog Oscillator Cycles

| Typ Time-out ($V_{CC}$ = 5.0V) | Typ Time-out ($V_{CC}$ = 3.0V) | Number of Cycles |
|---|---|---|
| 4.1 ms | 4.3 ms | 4K (4,096) |
| 65 ms | 69 ms | 64K (65,536) |

## fault Clock Source

The device is shipped with CKSEL = "0001" and SUT = "10". The default clock source setting is therefore the 1 MHz Internal RC Oscillator with longest startup time. This default setting ensures that all users can make their desired clock source setting using an In-System or Parallel Programmer.

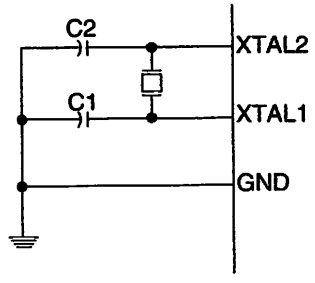
## ystal Oscillator

XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier which can be configured for use as an On-chip Oscillator, as shown in Figure 12. Either a quartz crystal or a ceramic resonator may be used. The CKOPT Fuse selects between two different Oscillator amplifier modes. When CKOPT is programmed, the Oscillator output will oscillate will a full rail-to-rail swing on the output. This mode is suitable when operating in a very noisy environment or when the output from XTAL2 drives a second clock buffer. This mode has a wide frequency range. When CKOPT is unprogrammed, the Oscillator has a smaller output swing. This reduces power consumption considerably.

This mode has a limited frequency range and it can not be used to drive other clock buffers.

For resonators, the maximum frequency is 8 MHz with CKOPT unprogrammed and 16 MHz with CKOPT programmed. C1 and C2 should always be equal for both crystals and resonators. The optimal value of the capacitors depends on the crystal or resonator in use, the amount of stray capacitance, and the electromagnetic noise of the environment. Some initial guidelines for choosing capacitors for use with crystals are given in Table 4. For ceramic resonators, the capacitor values given by the manufacturer should be used.

**Figure 12.** Crystal Oscillator Connections




The Oscillator can operate in three different modes, each optimized for a specific frequency range. The operating mode is selected by the fuses CKSEL3..1 as shown in Table 4.

**Table 4.** Crystal Oscillator Operating Modes

| CKOPT | CKSEL3..1 | Frequency Range (MHz) | Recommended Range for Capacitors C1 and C2 for Use with Crystals (pF) |
|---|---|---|---|
| 1 | 101[1] | 0.4 - 0.9 | – |
| 1 | 110 | 0.9 - 3.0 | 12 - 22 |
| 1 | 111 | 3.0 - 8.0 | 12 - 22 |
| 0 | 101, 110, 111 | 1.0 ≤ | 12 - 22 |

Note: 1. This option should not be used with crystals, only with ceramic resonators.

The CKSEL0 Fuse together with the SUT1..0 Fuses select the start-up times as shown in Table 5.

**Table 5.** Start-up Times for the Crystal Oscillator Clock Selection

| CKSEL0 | SUT1..0 | Start-up Time from Power-down and Power-save | Additional Delay from Reset ($V_{CC}$ = 5.0V) | Recommended Usage |
|---|---|---|---|---|
| 0 | 00 | 258 CK[1] | 4.1 ms | Ceramic resonator, fast rising power |
| 0 | 01 | 258 CK[1] | 65 ms | Ceramic resonator, slowly rising power |
| 0 | 10 | 1K CK[2] | – | Ceramic resonator, BOD enabled |
| 0 | 11 | 1K CK[2] | 4.1 ms | Ceramic resonator, fast rising power |
| 1 | 00 | 1K CK[2] | 65 ms | Ceramic resonator, slowly rising power |
| 1 | 01 | 16K CK | – | Crystal Oscillator, BOD enabled |
| 1 | 10 | 16K CK | 4.1 ms | Crystal Oscillator, fast rising power |
| 1 | 11 | 16K CK | 65 ms | Crystal Oscillator, slowly rising power |

Notes:
1. These options should only be used when not operating close to the maximum frequency of the device, and only if frequency stability at start-up is not important for the application. These options are not suitable for crystals.
2. These options are intended for use with ceramic resonators and will ensure frequency stability at start-up. They can also be used with crystals when not operating close to the maximum frequency of the device, and if frequency stability at start-up is not important for the application.

## w-frequency Crystal cillator

To use a 32.768 kHz watch crystal as the clock source for the device, the Low-frequency Crystal Oscillator must be selected by setting the CKSEL Fuses to "1001". The crystal should be connected as shown in Figure 12. By programming the CKOPT Fuse, the user can enable internal capacitors on XTAL1 and XTAL2, thereby removing the need for external capacitors. The internal capacitors have a nominal value of 36 pF.

When this Oscillator is selected, start-up times are determined by the SUT Fuses as shown in Table 6.

**Table 6.** Start-up Times for the Low-frequency Crystal Oscillator Clock Selection

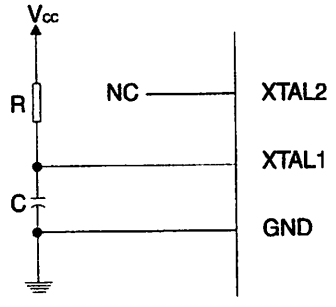
| SUT1..0 | Start-up Time from Power-down and Power-save | Additional Delay from Reset ($V_{CC}$ = 5.0V) | Recommended Usage |
|---|---|---|---|
| 00 | 1K CK(1) | 4.1 ms | Fast rising power or BOD enabled |
| 01 | 1K CK(1) | 65 ms | Slowly rising power |
| 10 | 32K CK | 65 ms | Stable frequency at start-up |
| 11 | Reserved | | |

Note: 1. These options should only be used if frequency stability at start-up is not important for the application.

## ternal RC Oscillator

For timing insensitive applications, the external RC configuration shown in Figure 13 can be used. The frequency is roughly estimated by the equation f = 1/(3RC). C should be at least 22 pF. By programming the CKOPT Fuse, the user can enable an internal 36 pF capacitor between XTAL1 and GND, thereby removing the need for an external capacitor. For more information on Oscillator operation and details on how to choose R and C, refer to the External RC Oscillator application note.

**Figure 13.** External RC Configuration




The Oscillator can operate in four different modes, each optimized for a specific frequency range. The operating mode is selected by the fuses CKSEL3..0 as shown in Table 7.

**Table 7.** External RC Oscillator Operating Modes

| CKSEL3..0 | Frequency Range (MHz) |
|---|---|
| 0101 | 0.1 ≤ 0.9 |

**Table 7.** External RC Oscillator Operating Modes

| CKSEL3..0 | Frequency Range (MHz) |
|---|---|
| 0110 | 0.9 - 3.0 |
| 0111 | 3.0 - 8.0 |
| 1000 | 8.0 - 12.0 |

When this Oscillator is selected, start-up times are determined by the SUT Fuses as shown in Table 8.

**Table 8.** Start-up Times for the External RC Oscillator Clock Selection

| SUT1..0 | Start-up Time from Power-down and Power-save | Additional Delay from Reset ($V_{CC}$ = 5.0V) | Recommended Usage |
|---|---|---|---|
| 00 | 18 CK | – | BOD enabled |
| 01 | 18 CK | 4.1 ms | Fast rising power |
| 10 | 18 CK | 65 ms | Slowly rising power |
| 11 | 6 CK[1] | 4.1 ms | Fast rising power or BOD enabled |

Note: 1. This option should not be used when operating close to the maximum frequency of the device.

## ilibrated Internal RC cillator

The Calibrated Internal RC Oscillator provides a fixed 1.0, 2.0, 4.0, or 8.0 MHz clock. All frequencies are nominal values at 5V and 25°C. This clock may be selected as the system clock by programming the CKSEL Fuses as shown in Table 9. If selected, it will operate with no external components. The CKOPT Fuse should always be unprogrammed when using this clock option. During Reset, hardware loads the calibration byte into the OSCCAL Register and thereby automatically calibrates the RC Oscillator. At 5V, 25°C and 1.0 MHz Oscillator frequency selected, this calibration gives a frequency within ± 3% of the nominal frequency. Using calibration methods as described in application notes available at www.atmel.com/avr it is possible to achieve ±1% accuracy at any given $V_{CC}$ and Temperature. When this Oscillator is used as the Chip Clock, the Watchdog Oscillator will still be used for the Watchdog Timer and for the reset time-out. For more information on the pre-programmed calibration value, see the section "Calibration Byte" on page 261.

**Table 9.** Internal Calibrated RC Oscillator Operating Modes

| CKSEL3..0 | Nominal Frequency (MHz) |
|---|---|
| 0001[1] | 1.0 |
| 0010 | 2.0 |
| 0011 | 4.0 |
| 0100 | 8.0 |

Note: 1. The device is shipped with this option selected.

When this Oscillator is selected, start-up times are determined by the SUT Fuses as shown in Table 10. XTAL1 and XTAL2 should be left unconnected (NC).

**Table 10.** Start-up Times for the Internal Calibrated RC Oscillator Clock Selection

| SUT1..0 | Start-up Time from Power-down and Power-save | Additional Delay from Reset ($V_{CC}$ = 5.0V) | Recommended Usage |
|---|---|---|---|
| 00 | 6 CK | – | BOD enabled |
| 01 | 6 CK | 4.1 ms | Fast rising power |
| 10[1] | 6 CK | 65 ms | Slowly rising power |
| 11 | Reserved | | |

Note: 1. The device is shipped with this option selected.

### :illator Calibration Register SCCAL

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | CAL7 | CAL6 | CAL5 | CAL4 | CAL3 | CAL2 | CAL1 | CAL0 | OSCCAL |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | Device Specific Calibration Value | | | | | | | | |

- **Bits 7..0 – CAL7..0: Oscillator Calibration Value**

Writing the calibration byte to this address will trim the Internal Oscillator to remove process variations from the Oscillator frequency. This is done automatically during Chip Reset. When OSCCAL is zero, the lowest available frequency is chosen. Writing non-zero values to this register will increase the frequency of the Internal Oscillator. Writing $FF to the register gives the highest available frequency. The calibrated Oscillator is used to time EEPROM and Flash access. If EEPROM or Flash is written, do not calibrate to more than 10% above the nominal frequency. Otherwise, the EEPROM or Flash write may fail. Note that the Oscillator is intended for calibration to 1.0, 2.0, 4.0, or 8.0 MHz. Tuning to other values is not guaranteed, as indicated in Table 11.

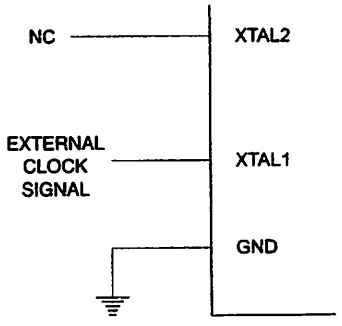
**Table 11.** Internal RC Oscillator Frequency Range.

| OSCCAL Value | Min Frequency in Percentage of Nominal Frequency (%) | Max Frequency in Percentage of Nominal Frequency (%) |
|---|---|---|
| $00 | 50 | 100 |
| $7F | 75 | 150 |
| $FF | 100 | 200 |

## ternal Clock

To drive the device from an external clock source, XTAL1 should be driven as shown in Figure 14. To run the device on an external clock, the CKSEL Fuses must be programmed to "0000". By programming the CKOPT Fuse, the user can enable an internal 36 pF capacitor between XTAL1 and GND.

**Figure 14.** External Clock Drive Configuration




When this clock source is selected, start-up times are determined by the SUT Fuses as shown in Table 12.

**Table 12.** Start-up Times for the External Clock Selection

| SUT1..0 | Start-up Time from Power-down and Power-save | Additional Delay from Reset ($V_{CC}$ = 5.0V) | Recommended Usage |
|---|---|---|---|
| 00 | 6 CK | – | BOD enabled |
| 01 | 6 CK | 4.1 ms | Fast rising power |
| 10 | 6 CK | 65 ms | Slowly rising power |
| 11 | Reserved | | |

When applying an external clock, it is required to avoid sudden changes in the applied clock frequency to ensure stable operation of the MCU. A variation in frequency of more than 2% from one clock cycle to the next can lead to unpredictable behavior. It is required to ensure that the MCU is kept in reset during such changes in the clock frequency.

## mer/Counter Oscillator

For AVR microcontrollers with Timer/Counter Oscillator pins (TOSC1 and TOSC2), the crystal is connected directly between the pins. No external capacitors are needed. The Oscillator is optimized for use with a 32.768 kHz watch crystal. Applying an external clock source to TOSC1 is not recommended.

## wer Management d Sleep Modes

Sleep modes enable the application to shut down unused modules in the MCU, thereby saving power. The AVR provides various sleep modes allowing the user to tailor the power consumption to the application's requirements.

To enter any of the six sleep modes, the SE bit in MCUCR must be written to logic one and a SLEEP instruction must be executed. The SM2, SM1, and SM0 bits in the MCUCR Register select which sleep mode (Idle, ADC Noise Reduction, Power-down, Power-save, Standby, or Extended Standby) will be activated by the SLEEP instruction. See Table 13 for a summary. If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU wakes up. The MCU is then halted for four cycles in addition to the start-up time, it executes the interrupt routine, and resumes execution from the instruction following SLEEP. The contents of the Register File and SRAM are unaltered when the device wakes up from sleep. If a Reset occurs during sleep mode, the MCU wakes up and executes from the Reset Vector.

Figure 11 on page 22 presents the different clock systems in the ATmega16, and their distribution. The figure is helpful in selecting an appropriate sleep mode.

### U Control Register – UCR

The MCU Control Register contains control bits for power management.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | SM2 | SE | SM1 | SM0 | ISC11 | ISC10 | ISC01 | ISC00 | MCUCR |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bits 7, 5, 4 – SM2..0: Sleep Mode Select Bits 2, 1, and 0**

These bits select between the six available sleep modes as shown in Table 13.

**Table 13.** Sleep Mode Select

| SM2 | SM1 | SM0 | Sleep Mode |
|---|---|---|---|
| 0 | 0 | 0 | Idle |
| 0 | 0 | 1 | ADC Noise Reduction |
| 0 | 1 | 0 | Power-down |
| 0 | 1 | 1 | Power-save |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Standby(1) |
| 1 | 1 | 1 | Extended Standby(1) |

Note: 1. Standby mode and Extended Standby mode are only available with external crystals or resonators.

- **Bit 6 – SE: Sleep Enable**

The SE bit must be written to logic one to make the MCU enter the sleep mode when the SLEEP instruction is executed. To avoid the MCU entering the sleep mode unless it is the programmers purpose, it is recommended to write the Sleep Enable (SE) bit to one just before the execution of the SLEEP instruction and to clear it immediately after waking up.

### e Mode

When the SM2..0 bits are written to 000, the SLEEP instruction makes the MCU enter Idle mode, stopping the CPU but allowing SPI, USART, Analog Comparator, ADC, Two-wire Serial Interface, Timer/Counters, Watchdog, and the interrupt system to continue operating. This sleep mode basically halts $clk_{CPU}$ and $clk_{FLASH}$, while allowing the other clocks to run.

Idle mode enables the MCU to wake up from external triggered interrupts as well as internal ones like the Timer Overflow and USART Transmit Complete interrupts. If wake-up from the Analog Comparator interrupt is not required, the Analog Comparator can be powered down by setting the ACD bit in the Analog Comparator Control and Status Register – ACSR. This will reduce power consumption in Idle mode. If the ADC is enabled, a conversion starts automatically when this mode is entered.

### IC Noise Reduction ıde

When the SM2..0 bits are written to 001, the SLEEP instruction makes the MCU enter ADC Noise Reduction mode, stopping the CPU but allowing the ADC, the External Interrupts, the Two-wire Serial Interface address watch, Timer/Counter2 and the Watchdog to continue operating (if enabled). This sleep mode basically halts $clk_{I/O}$, $clk_{CPU}$, and $clk_{FLASH}$, while allowing the other clocks to run.

This improves the noise environment for the ADC, enabling higher resolution measurements. If the ADC is enabled, a conversion starts automatically when this mode is entered. Apart form the ADC Conversion Complete interrupt, only an External Reset, a Watchdog Reset, a Brown-out Reset, a Two-wire Serial Interface Address Match Interrupt, a Timer/Counter2 interrupt, an SPM/EEPROM ready interrupt, an External level interrupt on INT0 or INT1, or an external interrupt on INT2 can wake up the MCU from ADC Noise Reduction mode.

### ıwer-down Mode

When the SM2..0 bits are written to 010, the SLEEP instruction makes the MCU enter Power-down mode. In this mode, the External Oscillator is stopped, while the External interrupts, the Two-wire Serial Interface address watch, and the Watchdog continue operating (if enabled). Only an External Reset, a Watchdog Reset, a Brown-out Reset, a Two-wire Serial Interface address match interrupt, an External level interrupt on INT0 or INT1, or an External interrupt on INT2 can wake up the MCU. This sleep mode basically halts all generated clocks, allowing operation of asynchronous modules only.

Note that if a level triggered interrupt is used for wake-up from Power-down mode, the changed level must be held for some time to wake up the MCU. Refer to "External Interrupts" on page 66 for details.

When waking up from Power-down mode, there is a delay from the wake-up condition occurs until the wake-up becomes effective. This allows the clock to restart and become stable after having been stopped. The wake-up period is defined by the same CKSEL Fuses that define the reset time-out period, as described in "Clock Sources" on page 23.

### ıwer-save Mode

When the SM2..0 bits are written to 011, the SLEEP instruction makes the MCU enter Power-save mode. This mode is identical to Power-down, with one exception:

If Timer/Counter2 is clocked asynchronously, i.e., the AS2 bit in ASSR is set, Timer/Counter2 will run during sleep. The device can wake up from either Timer Overflow or Output Compare event from Timer/Counter2 if the corresponding Timer/Counter2 interrupt enable bits are set in TIMSK, and the Global Interrupt Enable bit in SREG is set.

If the Asynchronous Timer is NOT clocked asynchronously, Power-down mode is recommended instead of Power-save mode because the contents of the registers in the

Asynchronous Timer should be considered undefined after wake-up in Power-save mode if AS2 is 0.

This sleep mode basically halts all clocks except $clk_{ASY}$, allowing operation only of asynchronous modules, including Timer/Counter2 if clocked asynchronously.

### ındby Mode

When the SM2..0 bits are 110 and an external crystal/resonator clock option is selected, the SLEEP instruction makes the MCU enter Standby mode. This mode is identical to Power-down with the exception that the Oscillator is kept running. From Standby mode, the device wakes up in six clock cycles.

### tended Standby Mode

When the SM2..0 bits are 111 and an external crystal/resonator clock option is selected, the SLEEP instruction makes the MCU enter Extended Standby mode. This mode is identical to Power-save mode with the exception that the Oscillator is kept running. From Extended Standby mode, the device wakes up in six clock cycles..

**ıle 14.** Active Clock Domains and Wake Up Sources in the Different Sleep Modes

| | Active Clock domains | | | | | Oscillators | | Wake-up Sources | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ɜep ıde | $clk_{CPU}$ | $clk_{FLASH}$ | $clk_{IO}$ | $clk_{ADC}$ | $clk_{ASY}$ | Main Clock Source Enabled | Timer Osc. Enabled | INT2 INT1 INT0 | TWI Address Match | Timer 2 | SPM / EEPROM Ready | ADC | Other I/O |
| e | | | X | X | X | X | X(2) | X | X | X | X | X | X |
| )C )ise ɜdu- on | | | | X | X | X | X(2) | X(3) | X | X | X | X | |
| )wer )wn | | | | | | | | X(3) | X | | | | |
| )wer ıve | | | | | X(2) | | X(2) | X(3) | X | X(2) | | | |
| andby(1) | | | | | | X | | X(3) | X | | | | |
| ɜten- ɜd andby(1) | | | | | X(2) | X | X(2) | X(3) | X | X(2) | | | |

ɜes: 1. External Crystal or resonator selected as clock source.
2. If AS2 bit in ASSR is set.
3. Only INT2 or level interrupt INT1 and INT0.

### ıimizing Power nsumption

There are several issues to consider when trying to minimize the power consumption in an AVR controlled system. In general, sleep modes should be used as much as possible, and the sleep mode should be selected so that as few as possible of the device's functions are operating. All functions not needed should be disabled. In particular, the following modules may need special consideration when trying to achieve the lowest possible power consumption.

### ılog to Digital Converter

If enabled, the ADC will be enabled in all sleep modes. To save power, the ADC should be disabled before entering any sleep mode. When the ADC is turned off and on again, the next conversion will be an extended conversion. Refer to "Analog to Digital Converter" on page 202 for details on ADC operation.

### ılog Comparator

When entering Idle mode, the Analog Comparator should be disabled if not used. When entering ADC Noise Reduction mode, the Analog Comparator should be disabled. In the other sleep modes, the Analog Comparator is automatically disabled. However, if the Analog Comparator is set up to use the Internal Voltage Reference as input, the Analog Comparator should be disabled in all sleep modes. Otherwise, the Internal Voltage Reference will be enabled, independent of sleep mode. Refer to "Analog Comparator" on page 199 for details on how to configure the Analog Comparator.

### ıwn-out Detector

If the Brown-out Detector is not needed in the application, this module should be turned off. If the Brown-out Detector is enabled by the BODEN Fuse, it will be enabled in all sleep modes, and hence, always consume power. In the deeper sleep modes, this will contribute significantly to the total current consumption. Refer to "Brown-out Detection" on page 38 for details on how to configure the Brown-out Detector.

### ɜrnal Voltage Reference

The Internal Voltage Reference will be enabled when needed by the Brown-out Detector, the Analog Comparator or the ADC. If these modules are disabled as described in the sections above, the internal voltage reference will be disabled and it will not be consuming power. When turned on again, the user must allow the reference to start up before the output is used. If the reference is kept on in sleep mode, the output can be used immediately. Refer to "Internal Voltage Reference" on page 40 for details on the start-up time.

### tchdog Timer

If the Watchdog Timer is not needed in the application, this module should be turned off. If the Watchdog Timer is enabled, it will be enabled in all sleep modes, and hence, always consume power. In the deeper sleep modes, this will contribute significantly to the total current consumption. Refer to "Watchdog Timer" on page 40 for details on how to configure the Watchdog Timer.

### rt Pins

When entering a sleep mode, all port pins should be configured to use minimum power. The most important thing is then to ensure that no pins drive resistive loads. In sleep modes where the both the I/O clock ($clk_{I/O}$) and the ADC clock ($clk_{ADC}$) are stopped, the input buffers of the device will be disabled. This ensures that no power is consumed by the input logic when not needed. In some cases, the input logic is needed for detecting wake-up conditions, and it will then be enabled. Refer to the section "Digital Input Enable and Sleep Modes" on page 52 for details on which pins are enabled. If the input buffer is enabled and the input signal is left floating or have an analog signal level close to $V_{CC}/2$, the input buffer will use excessive power.

**G Interface and chip Debug System**

If the On-chip debug system is enabled by the OCDEN Fuse and the chip enter Power down or Power save sleep mode, the main clock source remains enabled. In these sleep modes, this will contribute significantly to the total current consumption. There are three alternative ways to avoid this:

- Disable OCDEN Fuse.
- Disable JTAGEN Fuse.
- Write one to the JTD bit in MCUCSR.

The TDO pin is left floating when the JTAG interface is enabled while the JTAG TAP controller is not shifting data. If the hardware connected to the TDO pin does not pull up the logic level, power consumption will increase. Note that the TDI pin for the next device in the scan chain contains a pull-up that avoids this problem. Writing the JTD bit in the MCUCSR register to one or leaving the JTAG fuse unprogrammed disables the JTAG interface.

# stem Control and set

## etting the AVR

During Reset, all I/O Registers are set to their initial values, and the program starts execution from the Reset Vector. The instruction placed at the Reset Vector must be a JMP – absolute jump – instruction to the reset handling routine. If the program never enables an interrupt source, the Interrupt Vectors are not used, and regular program code can be placed at these locations. This is also the case if the Reset Vector is in the Application section while the Interrupt Vectors are in the Boot section or vice versa. The circuit diagram in Figure 15 shows the reset logic. Table 15 defines the electrical parameters of the reset circuitry.

The I/O ports of the AVR are immediately reset to their initial state when a reset source goes active. This does not require any clock source to be running.

After all reset sources have gone inactive, a delay counter is invoked, stretching the Internal Reset. This allows the power to reach a stable level before normal operation starts. The time-out period of the delay counter is defined by the user through the CKSEL Fuses. The different selections for the delay period are presented in "Clock Sources" on page 23.

## set Sources

The ATmega16 has five sources of reset:

- Power-on Reset. The MCU is reset when the supply voltage is below the Power-on Reset threshold ($V_{POT}$).
- External Reset. The MCU is reset when a low level is present on the $\overline{\text{RESET}}$ pin for longer than the minimum pulse length.
- Watchdog Reset. The MCU is reset when the Watchdog Timer period expires and the Watchdog is enabled.
- Brown-out Reset. The MCU is reset when the supply voltage $V_{CC}$ is below the Brown-out Reset threshold ($V_{BOT}$) and the Brown-out Detector is enabled.
- JTAG AVR Reset. The MCU is reset as long as there is a logic one in the Reset Register, one of the scan chains of the JTAG system. Refer to the section "IEEE 1149.1 (JTAG) Boundary-scan" on page 226 for details.

**Figure 15.** Reset Logic

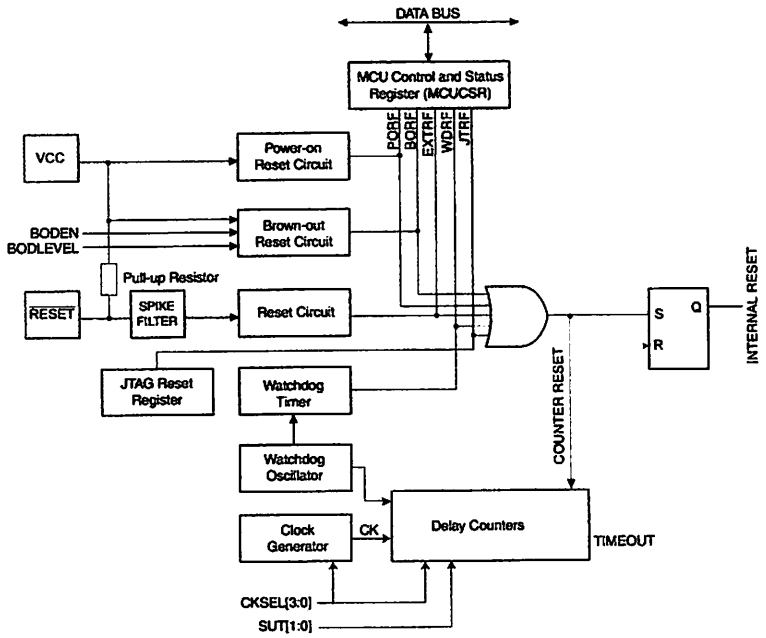



**Table 15.** Reset Characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{POT}$ | Power-on Reset Threshold Voltage (rising) | | | 1.4 | 2.3 | V |
| | Power-on Reset Threshold Voltage (falling)[1] | | | 1.3 | 2.3 | V |
| $V_{RST}$ | $\overline{\text{RESET}}$ Pin Threshold Voltage | | 0.1 $V_{CC}$ | | 0.9$V_{CC}$ | V |
| $t_{RST}$ | Minimum pulse width on $\overline{\text{RESET}}$ Pin | | | | 1.5 | µs |
| $V_{BOT}$ | Brown-out Reset Threshold Voltage[2] | BODLEVEL = 1 | 2.5 | 2.7 | 3.2 | V |
| | | BODLEVEL = 0 | 3.6 | 4.0 | 4.5 | |
| $t_{BOD}$ | Minimum low voltage period for Brown-out Detection | BODLEVEL = 1 | | 2 | | µs |
| | | BODLEVEL = 0 | | 2 | | µs |
| $V_{HYST}$ | Brown-out Detector hysteresis | | | 50 | | mV |

Notes: 1. The Power-on Reset will not work unless the supply voltage has been below $V_{POT}$ (falling).

2. $V_{BOT}$ may be below nominal minimum operating voltage for some devices. For devices where this is the case, the device is tested down to $V_{CC} = V_{BOT}$ during the production test. This guarantees that a Brown-out Reset will occur before $V_{CC}$ drops to a voltage where correct operation of the microcontroller is no longer guaranteed. The test is performed using BODLEVEL = 1 for ATmega16L and BODLEVEL = 0 for ATmega16. BODLEVEL = 1 is not applicable for ATmega16.

**ver-on Reset**

A Power-on Reset (POR) pulse is generated by an On-chip detection circuit. The detection level is defined in Table 15. The POR is activated whenever $V_{CC}$ is below the detection level. The POR circuit can be used to trigger the Start-up Reset, as well as to detect a failure in supply voltage.

A Power-on Reset (POR) circuit ensures that the device is reset from Power-on. Reaching the Power-on Reset threshold voltage invokes the delay counter, which determines how long the device is kept in RESET after $V_{CC}$ rise. The RESET signal is activated again, without any delay, when $V_{CC}$ decreases below the detection level.

**Figure 16.** MCU Start-up, $\overline{\text{RESET}}$ Tied to $V_{CC}$.

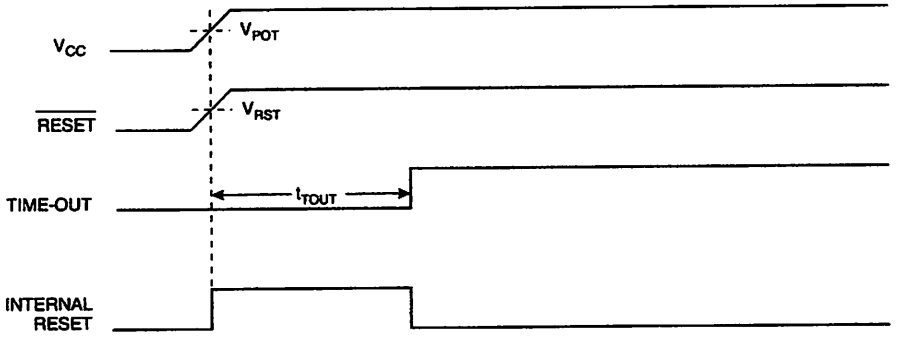
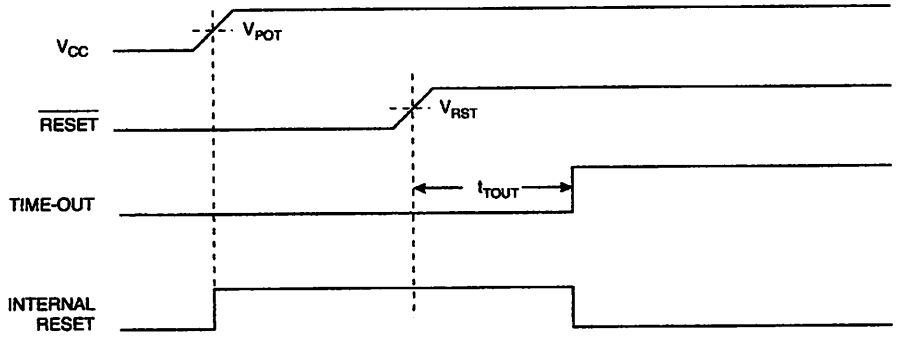


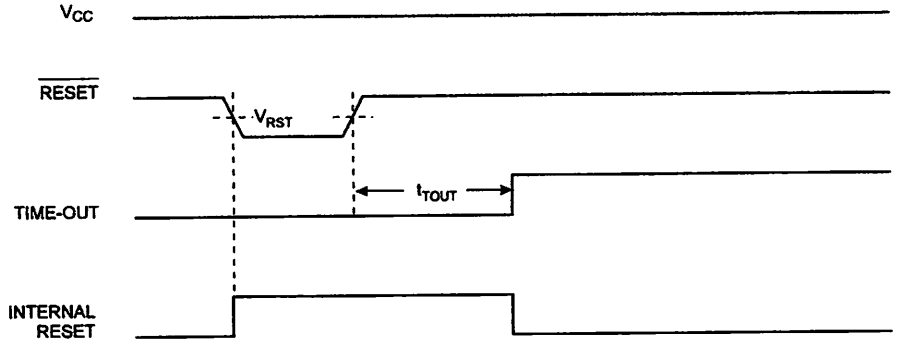

**Figure 17.** MCU Start-up, $\overline{\text{RESET}}$ Extended Externally



### ernal Reset

An External Reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than the minimum pulse width (see Table 15) will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset. When the applied signal reaches the Reset Threshold Voltage – $V_{RST}$ – on its positive edge, the delay counter starts the MCU after the Time-out period $t_{TOUT}$ has expired.

**Figure 18.** External Reset During Operation



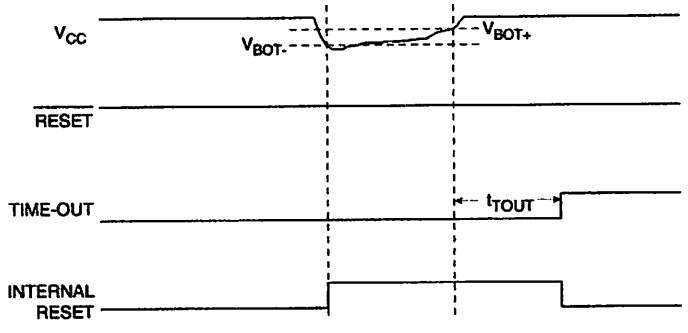

### own-out Detection

ATmega16 has an On-chip Brown-out Detection (BOD) circuit for monitoring the $V_{CC}$ level during operation by comparing it to a fixed trigger level. The trigger level for the BOD can be selected by the fuse BODLEVEL to be 2.7V (BODLEVEL unprogrammed), or 4.0V (BODLEVEL programmed). The trigger level has a hysteresis to ensure spike free Brown-out Detection. The hysteresis on the detection level should be interpreted as $V_{BOT+} = V_{BOT} + V_{HYST}/2$ and $V_{BOT-} = V_{BOT} - V_{HYST}/2$.

The BOD circuit can be enabled/disabled by the fuse BODEN. When the BOD is enabled (BODEN programmed), and $V_{CC}$ decreases to a value below the trigger level ($V_{BOT-}$ in Figure 19), the Brown-out Reset is immediately activated. When $V_{CC}$ increases above the trigger level ($V_{BOT+}$ in Figure 19), the delay counter starts the MCU after the Time-out period $t_{TOUT}$ has expired.

The BOD circuit will only detect a drop in $V_{CC}$ if the voltage stays below the trigger level for longer than $t_{BOD}$ given in Table 15.

**Figure 19.** Brown-out Reset During Operation



# ectrical Characteristics

## solute Maximum Ratings*

| | |
|---|---|
| erating Temperature | -55°C to +125°C |
| rage Temperature | -65°C to +150°C |
| ltage on any Pin except $\overline{\text{RESET}}$ th respect to Ground | -0.5V to $V_{CC}$+0.5V |
| ltage on $\overline{\text{RESET}}$ with respect to Ground | -0.5V to +13.0V |
| aximum Operating Voltage | 6.0V |
| Current per I/O Pin | 40.0 mA |
| Current $V_{CC}$ and GND Pins | 200.0mA PDIP and 0.0mA TQFP/MLF |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Characteristics

= -40°C to 85°C, $V_{CC}$ = 2.7V to 5.5V (Unless Otherwise Noted)

| ymbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| L | Input Low Voltage except XTAL1 and $\overline{\text{RESET}}$ pins | $V_{CC}$=2.7 - 5.5 | -0.5 | | 0.2 $V_{CC}$[1] | V |
| H | Input High Voltage except XTAL1 and $\overline{\text{RESET}}$ pins | $V_{CC}$=2.7 - 5.5 | 0.6 $V_{CC}$[2] | | $V_{CC}$ +0.5 | V |
| H1 | Input High Voltage XTAL1 pin | $V_{CC}$=2.7 - 5.5 | 0.7 $V_{CC}$[2] | | $V_{CC}$ +0.5 | V |
| IL1 | Input Low Voltage XTAL1 pin | $V_{CC}$=2.7 - 5.5 | -0.5 | | 0.1 $V_{CC}$[1] | V |
| IH2 | Input High Voltage $\overline{\text{RESET}}$ pin | $V_{CC}$=2.7 - 5.5 | 0.9 $V_{CC}$[2] | | $V_{CC}$ +0.5 | V |
| IL2 | Input Low Voltage $\overline{\text{RESET}}$ pin | $V_{CC}$=2.7 - 5.5 | -0.5 | | 0.2 $V_{CC}$ | V |
| OL | Output Low Voltage[3] (Ports A,B,C,D) | $I_{OL}$ = 20 mA, $V_{CC}$ = 5V<br>$I_{OL}$ = 10 mA, $V_{CC}$ = 3V | | | 0.7<br>0.5 | V<br>V |
| OH | Output High Voltage[4] (Ports A,B,C,D) | $I_{OH}$ = -20 mA, $V_{CC}$ = 5V<br>$I_{OH}$ = -10 mA, $V_{CC}$ = 3V | 4.2<br>2.2 | | | V<br>V |
| - | Input Leakage Current I/O Pin | Vcc = 5.5V, pin low (absolute value) | | | 1 | µA |
| H | Input Leakage Current I/O Pin | Vcc = 5.5V, pin high (absolute value) | | | 1 | µA |
| RST | Reset Pull-up Resistor | | 30 | | 60 | kΩ |
| pu | I/O Pin Pull-up Resistor | | 20 | | 50 | kΩ |

: -40°C to 85°C, $V_{CC}$ = 2.7V to 5.5V (Unless Otherwise Noted) (Continued)

| mbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Power Supply Current | Active 1 MHz, $V_{CC}$ = 3V (ATmega16L) | | 1.1 | | mA |
| | | Active 4 MHz, $V_{CC}$ = 3V (ATmega16L) | | 3.8 | 5 | mA |
| | | Active 8 MHz, $V_{CC}$ = 5V (ATmega16) | | 12 | 15 | mA |
| | | Idle 1 MHz, $V_{CC}$ = 3V (ATmega16L) | | 0.35 | | mA |
| | | Idle 4 MHz, $V_{CC}$ = 3V (ATmega16L) | | 1.2 | 2 | mA |
| | | Idle 8 MHz, $V_{CC}$ = 5V (ATmega16) | | 5.5 | 7 | mA |
| | Power-down Mode[5] | WDT enabled, $V_{CC}$ = 3V | | <8 | 15 | µA |
| | | WDT disabled, $V_{CC}$ = 3V | | < 1 | 4 | µA |
| ICIO | Analog Comparator Input Offset Voltage | $V_{CC}$ = 5V<br>$V_{in}$ = $V_{CC}$/2 | | | 40 | mV |
| CLK | Analog Comparator Input Leakage Current | $V_{CC}$ = 5V<br>$V_{in}$ = $V_{CC}$/2 | -50 | | 50 | nA |
| CPD | Analog Comparator Propagation Delay | $V_{CC}$ = 2.7V<br>$V_{CC}$ = 4.0V | | 750<br>500 | | ns |

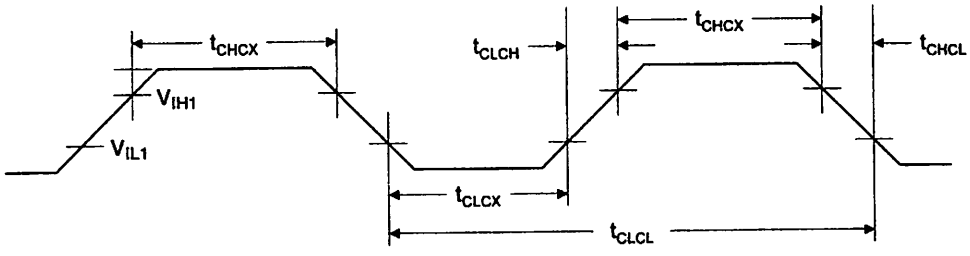
es:
1. "Max" means the highest value where the pin is guaranteed to be read as low
2. "Min" means the lowest value where the pin is guaranteed to be read as high
3. Although each I/O port can sink more than the test conditions (20 mA at Vcc = 5V, 10 mA at Vcc = 3V) under steady state conditions (non-transient), the following must be observed:
   PDIP Package:
   1] The sum of all IOL, for all ports, should not exceed 200 mA.
   2] The sum of all IOL, for port A0 - A7, should not exceed 100 mA.
   3] The sum of all IOL, for ports B0 - B7,C0 - C7, D0 - D7 and XTAL2, should not exceed 100 mA.
   TQFP and QFN/MLF Package:
   1] The sum of all IOL, for all ports, should not exceed 400 mA.
   2] The sum of all IOL, for ports A0 - A7, should not exceed 100 mA.
   3] The sum of all IOL, for ports B0 - B4, should not exceed 100 mA.
   4] The sum of all IOL, for ports B3 - B7, XTAL2, D0 - D2, should not exceed 100 mA.
   5] The sum of all IOL, for ports D3 - D7, should not exceed 100 mA.
   6] The sum of all IOL, for ports C0 - C7, should not exceed 100 mA.
   If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
4. Although each I/O port can source more than the test conditions (20 mA at Vcc = 5V, 10 mA at Vcc = 3V) under steady state conditions (non-transient), the following must be observed:
   PDIP Package:
   1] The sum of all IOH, for all ports, should not exceed 200 mA.
   2] The sum of all IOH, for port A0 - A7, should not exceed 100 mA.
   3] The sum of all IOH, for ports B0 - B7,C0 - C7, D0 - D7 and XTAL2, should not exceed 100 mA.
   TQFP and QFN/MLF Package:
   1] The sum of all IOH, for all ports, should not exceed 400 mA.
   2] The sum of all IOH, for ports A0 - A7, should not exceed 100 mA.
   3] The sum of all IOH, for ports B0 - B4, should not exceed 100 mA.
   4] The sum of all IOH, for ports B3 - B7, XTAL2, D0 - D2, should not exceed 100 mA.

5] The sum of all IOH, for ports D3 - D7, should not exceed 100 mA.
6] The sum of all IOH, for ports C0 - C7, should not exceed 100 mA.If IOH exceeds the test condition, VOH may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.

5. Minimum $V_{CC}$ for Power-down is 2.5V.

## ternal Clock Drive veforms

**Figure 145.** External Clock Drive Waveforms




## ternal Clock Drive

**Table 118.** External Clock Drive[1]

| Symbol | Parameter | $V_{CC}$ = 2.7V to 5.5V | | $V_{CC}$ = 4.5V to 5.5V | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $1/t_{CLCL}$ | Oscillator Frequency | 0 | 8 | 0 | 16 | MHz |
| $t_{CLCL}$ | Clock Period | 125 | | 62.5 | | ns |
| $t_{CHCX}$ | High Time | 50 | | 25 | | ns |
| $t_{CLCX}$ | Low Time | 50 | | 25 | | ns |
| $t_{CLCH}$ | Rise Time | | 1.6 | | 0.5 | µs |
| $t_{CHCL}$ | Fall Time | | 1.6 | | 0.5 | µs |
| $\Delta t_{CLCL}$ | Change in period from one clock cycle to the next | | 2 | | 2 | % |

Note: 1. Refer to "External Clock" on page 29 for details.

**Table 119.** External RC Oscillator, Typical Frequencies ($V_{CC}$ = 5)

| R [kΩ][1] | C [pF] | f[2] |
|---|---|---|
| 33 | 22 | 650 kHz |
| 10 | 22 | 2.0 MHz |

Notes: 1. R should be in the range 3 kΩ - 100 kΩ, and C should be at least 20 pF.
2. The frequency will vary with package type and board layout.

## ɔ-wire Serial Interface Characteristics

le 120 describes the requirements for devices connected to the Two-wire Serial Bus. The ATmega16 Two-wire Serial rface meets or exceeds these requirements under the noted conditions.

ing symbols refer to Figure 146.

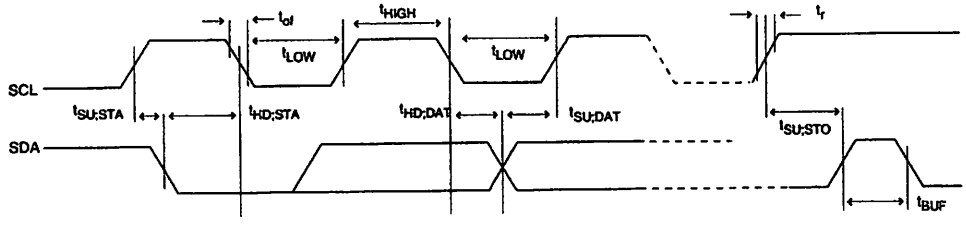
**le 120.** Two-wire Serial Bus Requirements

| mbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| | Input Low-voltage | | -0.5 | $0.3\ V_{CC}$ | V |
| I | Input High-voltage | | $0.7\ V_{CC}$ | $V_{CC} + 0.5$ | V |
| /S(1) | Hysteresis of Schmitt Trigger Inputs | | $0.05\ V_{CC}$(2) | – | V |
| L(1) | Output Low-voltage | 3 mA sink current | 0 | 0.4 | V |
| ) | Rise Time for both SDA and SCL | | $20 + 0.1C_b$(3)(2) | 300 | ns |
| 1) | Output Fall Time from $V_{IHmin}$ to $V_{ILmax}$ | 10 pF < $C_b$ < 400 pF(3) | $20 + 0.1C_b$(3)(2) | 250 | ns |
| (1) | Spikes Suppressed by Input Filter | | 0 | 50(2) | ns |
| | Input Current each I/O Pin | $0.1V_{CC} < V_i < 0.9V_{CC}$ | -10 | 10 | µA |
| 1) | Capacitance for each I/O Pin | | – | 10 | pF |
| :L | SCL Clock Frequency | $f_{CK}$(4) > max(16$f_{SCL}$, 250kHz)(5) | 0 | 400 | kHz |
| ) | Value of Pull-up resistor | $f_{SCL} \le 100$ kHz | $\frac{V_{CC} - 0,4V}{3mA}$ | $\frac{1000ns}{C_b}$ | Ω |
| | | $f_{SCL} > 100$ kHz | $\frac{V_{CC} - 0,4V}{3mA}$ | $\frac{300ns}{C_b}$ | Ω |
| ɔ;STA | Hold Time (repeated) START Condition | $f_{SCL} \le 100$ kHz | 4.0 | – | µs |
| | | $f_{SCL} > 100$ kHz | 0.6 | – | µs |
| ɔW | Low Period of the SCL Clock | $f_{SCL} \le 100$ kHz(6) | 4.7 | – | µs |
| | | $f_{SCL} > 100$ kHz(7) | 1.3 | – | µs |
| GH | High period of the SCL clock | $f_{SCL} \le 100$ kHz | 4.0 | – | µs |
| | | $f_{SCL} > 100$ kHz | 0.6 | – | µs |
| U;STA | Set-up time for a repeated START condition | $f_{SCL} \le 100$ kHz | 4.7 | – | µs |
| | | $f_{SCL} > 100$ kHz | 0.6 | – | µs |
| D;DAT | Data hold time | $f_{SCL} \le 100$ kHz | 0 | 3.45 | µs |
| | | $f_{SCL} > 100$ kHz | 0 | 0.9 | µs |
| U;DAT | Data setup time | $f_{SCL} \le 100$ kHz | 250 | – | ns |
| | | $f_{SCL} > 100$ kHz | 100 | – | ns |
| U;STO | Setup time for STOP condition | $f_{SCL} \le 100$ kHz | 4.0 | – | µs |
| | | $f_{SCL} > 100$ kHz | 0.6 | – | µs |
| UF | Bus free time between a STOP and START condition | $f_{SCL} \le 100$ kHz | 4.7 | – | µs |
| | | $f_{SCL} > 100$ kHz | 1.3 | – | µs |

tes:
1. In ATmega16, this parameter is characterized and not 100% tested.
2. Required only for $f_{SCL} > 100$ kHz.
3. $C_b$ = capacitance of one bus line in pF.
4. $f_{CK}$ = CPU clock frequency

5. This requirement applies to all ATmega16 Two-wire Serial Interface operation. Other devices connected to the Two-wire Serial Bus need only obey the general $f_{SCL}$ requirement.
6. The actual low period generated by the ATmega16 Two-wire Serial Interface is ($1/f_{SCL}$ - $2/f_{CK}$), thus $f_{CK}$ must be greater than 6 MHz for the low time requirement to be strictly met at $f_{SCL}$ = 100 kHz.
7. The actual low period generated by the ATmega16 Two-wire Serial Interface is ($1/f_{SCL}$ - $2/f_{CK}$), thus the low time requirement will not be strictly met for $f_{SCL}$ > 308 kHz when $f_{CK}$ = 8 MHz. Still, ATmega16 devices connected to the bus may communicate at full speed (400 kHz) with other ATmega16 devices, as well as any other device with a proper $t_{LOW}$ acceptance margin.

**Figure 146.** Two-wire Serial Bus Timing




## I Timing
## aracteristics

See Figure 147 and Figure 148 for details.

**Table 121.** SPI Timing Parameters

| | Description | Mode | Min | Typ | Max | |
|---|---|---|---|---|---|---|
| 1 | SCK period | Master | | See Table 58 | | |
| 2 | SCK high/low | Master | | 50% duty cycle | | |
| 3 | Rise/Fall time | Master | | 3.6 | | |
| 4 | Setup | Master | | 10 | | |
| 5 | Hold | Master | | 10 | | |
| 6 | Out to SCK | Master | | 0.5 • $t_{SCK}$ | | ns |
| 7 | SCK to out | Master | | 10 | | |
| 8 | SCK to out high | Master | | 10 | | |
| 9 | $\overline{SS}$ low to out | Slave | | 15 | | |
| 10 | SCK period | Slave | 4 • $t_{ck}$ | | | |
| 11 | SCK high/low | Slave | 2 • $t_{ck}$ | | | |
| 12 | Rise/Fall time | Slave | | | 1.6 | µs |
| 13 | Setup | Slave | 10 | | | |
| 14 | Hold | Slave | 10 | | | |
| 15 | SCK to out | Slave | | 15 | | ns |
| 16 | SCK to $\overline{SS}$ high | Slave | 20 | | | |
| 17 | $\overline{SS}$ high to tri-state | Slave | | 10 | | |
| 18 | $\overline{SS}$ low to SCK | Slave | 2 • $t_{ck}$ | | | |

## IC Characteristics – Preliminary Data

**ble 122.** ADC Characteristics

| ymbol | Parameter | Condition | Min(1) | Typ(1) | Max(1) | Units |
|---|---|---|---|---|---|---|
| | Resolution | Single Ended Conversion | | 10 | | Bits |
| | | Differential Conversion Gain = 1x or 20x | | 8 | | Bits |
| | | Differential Conversion Gain = 200x | | 7 | | Bits |
| | Absolute Accuracy (Including INL, DNL, Quantization Error, Gain, and Offset Error). | Single Ended Conversion $V_{REF}$ = 4V, $V_{CC}$ = 4V ADC clock = 200 kHz | | 1.5 | 2.5 | LSB |
| | | Single Ended Conversion $V_{REF}$ = 4V, $V_{CC}$ = 4V ADC clock = 1 MHz | | 3 | 4 | LSB |
| | | Single Ended Conversion $V_{REF}$ = 4V, $V_{CC}$ = 4V ADC clock = 200 kHz Noise Reduction mode | | 1.5 | | LSB |
| | | Single Ended Conversion $V_{REF}$ = 4V, $V_{CC}$ = 4V ADC clock = 1 MHz Noise Reduction mode | | 3 | | LSB |
| | Integral Non-linearity (INL) | Single Ended Conversion $V_{REF}$ = 4V, $V_{CC}$ = 4V ADC clock = 200 kHz | | 1 | | LSB |
| | Differential Non-linearity (DNL) | Single Ended Conversion $V_{REF}$ = 4V, $V_{CC}$ = 4V ADC clock = 200 kHz | | 0.5 | | LSB |
| | Gain Error | Single Ended Conversion $V_{REF}$ = 4V, $V_{CC}$ = 4V ADC clock = 200 kHz | | 1 | | LSB |
| | Offset Error | Single Ended Conversion $V_{REF}$ = 4V, $V_{CC}$ = 4V ADC clock = 200 kHz | | | | LSB |
| | Conversion Time | Free Running Conversion | 13 | | 260 | µs |
| | Clock Frequency | | 50 | | 1000 | kHz |
| AVCC | Analog Supply Voltage | | $V_{CC}$ - 0.3(2) | | $V_{CC}$ + 0.3(3) | V |
| $V_{REF}$ | Reference Voltage | Single Ended Conversion | 2.0 | | AVCC | V |
| | | Differential Conversion | 2.0 | | AVCC - 0.2 | V |
| $V_{IN}$ | Input voltage | Single ended channels | GND | | $V_{REF}$ | V |
| | | Differential channels | 0 | | $V_{REF}$ | V |
| | Input bandwidth | Single ended channels | | 38.5 | | kHz |
| | | Differential channels | | 4 | | kHz |

## egister Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| $3F ($5F) | SREG | I | T | H | S | V | N | Z | C | 7 |
| $3E ($5E) | SPH | – | – | – | – | – | SP10 | SP9 | SP8 | 10 |
| $3D ($5D) | SPL | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | 10 |
| $3C ($5C) | OCR0 | Timer/Counter0 Output Compare Register | | | | | | | | 83 |
| $3B ($5B) | GICR | INT1 | INT0 | INT2 | – | – | – | IVSEL | IVCE | 46, 67 |
| $3A ($5A) | GIFR | INTF1 | INTF0 | INTF2 | – | – | – | – | – | 68 |
| $39 ($59) | TIMSK | OCIE2 | TOIE2 | TICIE1 | OCIE1A | OCIE1B | TOIE1 | OCIE0 | TOIE0 | 83, 114, 132 |
| $38 ($58) | TIFR | OCF2 | TOV2 | ICF1 | OCF1A | OCF1B | TOV1 | OCF0 | TOV0 | 84, 115, 132 |
| $37 ($57) | SPMCR | SPMIE | RWWSB | – | RWWSRE | BLBSET | PGWRT | PGERS | SPMEN | 250 |
| $36 ($56) | TWCR | TWINT | TWEA | TWSTA | TWSTO | TWWC | TWEN | – | TWIE | 178 |
| $35 ($55) | MCUCR | SM2 | SE | SM1 | SM0 | ISC11 | ISC10 | ISC01 | ISC00 | 30, 66 |
| $34 ($54) | MCUCSR | JTD | ISC2 | – | JTRF | WDRF | BORF | EXTRF | PORF | 39, 67, 229 |
| $33 ($53) | TCCR0 | FOC0 | WGM00 | COM01 | COM00 | WGM01 | CS02 | CS01 | CS00 | 81 |
| $32 ($52) | TCNT0 | Timer/Counter0 (8 Bits) | | | | | | | | 83 |
| [1] ($51)[1] | OSCCAL | Oscillator Calibration Register | | | | | | | | 28 |
| | OCDR | On-Chip Debug Register | | | | | | | | 225 |
| $30 ($50) | SFIOR | ADTS2 | ADTS1 | ADTS0 | – | ACME | PUD | PSR2 | PSR10 | 55,86,133,199,219 |
| $2F ($4F) | TCCR1A | COM1A1 | COM1A0 | COM1B1 | COM1B0 | FOC1A | FOC1B | WGM11 | WGM10 | 109 |
| $2E ($4E) | TCCR1B | ICNC1 | ICES1 | – | WGM13 | WGM12 | CS12 | CS11 | CS10 | 112 |
| $2D ($4D) | TCNT1H | Timer/Counter1 – Counter Register High Byte | | | | | | | | 113 |
| $2C ($4C) | TCNT1L | Timer/Counter1 – Counter Register Low Byte | | | | | | | | 113 |
| $2B ($4B) | OCR1AH | Timer/Counter1 – Output Compare Register A High Byte | | | | | | | | 113 |
| $2A ($4A) | OCR1AL | Timer/Counter1 – Output Compare Register A Low Byte | | | | | | | | 113 |
| $29 ($49) | OCR1BH | Timer/Counter1 – Output Compare Register B High Byte | | | | | | | | 113 |
| $28 ($48) | OCR1BL | Timer/Counter1 – Output Compare Register B Low Byte | | | | | | | | 113 |
| $27 ($47) | ICR1H | Timer/Counter1 – Input Capture Register High Byte | | | | | | | | 114 |
| $26 ($48) | ICR1L | Timer/Counter1 – Input Capture Register Low Byte | | | | | | | | 114 |
| $25 ($45) | TCCR2 | FOC2 | WGM20 | COM21 | COM20 | WGM21 | CS22 | CS21 | CS20 | 127 |
| $24 ($44) | TCNT2 | Timer/Counter2 (8 Bits) | | | | | | | | 129 |
| $23 ($43) | OCR2 | Timer/Counter2 Output Compare Register | | | | | | | | 129 |
| $22 ($42) | ASSR | – | – | – | – | AS2 | TCN2UB | OCR2UB | TCR2UB | 130 |
| $21 ($41) | WDTCR | – | – | – | WDTOE | WDE | WDP2 | WDP1 | WDP0 | 41 |
| [2] ([2] ($40)[2] | UBRRH | URSEL | – | – | – | UBRR[11:8] | | | | 165 |
| | UCSRC | URSEL | UMSEL | UPM1 | UPM0 | USBS | UCSZ1 | UCSZ0 | UCPOL | 164 |
| $1F ($3F) | EEARH | – | – | – | – | – | – | – | EEAR8 | 17 |
| $1E ($3E) | EEARL | EEPROM Address Register Low Byte | | | | | | | | 17 |
| $1D ($3D) | EEDR | EEPROM Data Register | | | | | | | | 17 |
| $1C ($3C) | EECR | – | – | – | – | EERIE | EEMWE | EEWE | EERE | 17 |
| $1B ($3B) | PORTA | PORTA7 | PORTA6 | PORTA5 | PORTA4 | PORTA3 | PORTA2 | PORTA1 | PORTA0 | 64 |
| $1A ($3A) | DDRA | DDA7 | DDA6 | DDA5 | DDA4 | DDA3 | DDA2 | DDA1 | DDA0 | 64 |
| $19 ($39) | PINA | PINA7 | PINA6 | PINA5 | PINA4 | PINA3 | PINA2 | PINA1 | PINA0 | 64 |
| $18 ($38) | PORTB | PORTB7 | PORTB6 | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | 64 |
| $17 ($37) | DDRB | DDB7 | DDB6 | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | 64 |
| $16 ($36) | PINB | PINB7 | PINB6 | PINB5 | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | 64 |
| $15 ($35) | PORTC | PORTC7 | PORTC6 | PORTC5 | PORTC4 | PORTC3 | PORTC2 | PORTC1 | PORTC0 | 65 |
| $14 ($34) | DDRC | DDC7 | DDC6 | DDC5 | DDC4 | DDC3 | DDC2 | DDC1 | DDC0 | 65 |
| $13 ($33) | PINC | PINC7 | PINC6 | PINC5 | PINC4 | PINC3 | PINC2 | PINC1 | PINC0 | 65 |
| $12 ($32) | PORTD | PORTD7 | PORTD6 | PORTD5 | PORTD4 | PORTD3 | PORTD2 | PORTD1 | PORTD0 | 65 |
| $11 ($31) | DDRD | DDD7 | DDD6 | DDD5 | DDD4 | DDD3 | DDD2 | DDD1 | DDD0 | 65 |
| $10 ($30) | PIND | PIND7 | PIND6 | PIND5 | PIND4 | PIND3 | PIND2 | PIND1 | PIND0 | 65 |
| $0F ($2F) | SPDR | SPI Data Register | | | | | | | | 140 |
| $0E ($2E) | SPSR | SPIF | WCOL | – | – | – | – | – | SPI2X | 140 |
| $0D ($2D) | SPCR | SPIE | SPE | DORD | MSTR | CPOL | CPHA | SPR1 | SPR0 | 138 |
| $0C ($2C) | UDR | USART I/O Data Register | | | | | | | | 161 |
| $0B ($2B) | UCSRA | RXC | TXC | UDRE | FE | DOR | PE | U2X | MPCM | 162 |
| $0A ($2A) | UCSRB | RXCIE | TXCIE | UDRIE | RXEN | TXEN | UCSZ2 | RXB8 | TXB8 | 163 |
| $09 ($29) | UBRRL | USART Baud Rate Register Low Byte | | | | | | | | 165 |
| $08 ($28) | ACSR | ACD | ACBG | ACO | ACI | ACIE | ACIC | ACIS1 | ACIS0 | 200 |
| $07 ($27) | ADMUX | REFS1 | REFS0 | ADLAR | MUX4 | MUX3 | MUX2 | MUX1 | MUX0 | 215 |
| $06 ($26) | ADCSRA | ADEN | ADSC | ADATE | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 | 217 |
| $05 ($25) | ADCH | ADC Data Register High Byte | | | | | | | | 218 |
| $04 ($24) | ADCL | ADC Data Register Low Byte | | | | | | | | 218 |
| $03 ($23) | TWDR | Two-wire Serial Interface Data Register | | | | | | | | 180 |
| $02 ($22) | TWAR | TWA6 | TWA5 | TWA4 | TWA3 | TWA2 | TWA1 | TWA0 | TWGCE | 180 |

| ddress | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| 01 ($21) | TWSR | TWS7 | TWS6 | TWS5 | TWS4 | TWS3 | – | TWPS1 | TWPS0 | 179 |
| 00 ($20) | TWBR | Two-wire Serial Interface Bit Rate Register | | | | | | | | 178 |

es:
1. When the OCDEN Fuse is unprogrammed, the OSCCAL Register is always accessed on this address. Refer to the debugger specific documentation for details on how to use the OCDR Register.
2. Refer to the USART description for details on how to access UBRRH and UCSRC.
3. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
4. Some of the Status Flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

## struction Set Summary

| emonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| THMETIC AND LOGIC INSTRUCTIONS | | | | | |
| ) | Rd, Rr | Add two Registers | Rd ← Rd + Rr | Z,C,N,V,H | 1 |
| : | Rd, Rr | Add with Carry two Registers | Rd ← Rd + Rr + C | Z,C,N,V,H | 1 |
| W | Rdl,K | Add Immediate to Word | Rdh:Rdl ← Rdh:Rdl + K | Z,C,N,V,S | 2 |
| 3 | Rd, Rr | Subtract two Registers | Rd ← Rd - Rr | Z,C,N,V,H | 1 |
| 3I | Rd, K | Subtract Constant from Register | Rd ← Rd - K | Z,C,N,V,H | 1 |
| : | Rd, Rr | Subtract with Carry two Registers | Rd ← Rd - Rr - C | Z,C,N,V,H | 1 |
| :I | Rd, K | Subtract with Carry Constant from Reg. | Rd ← Rd - K - C | Z,C,N,V,H | 1 |
| W | Rdl,K | Subtract Immediate from Word | Rdh:Rdl ← Rdh:Rdl - K | Z,C,N,V,S | 2 |
| D | Rd, Rr | Logical AND Registers | Rd ← Rd • Rr | Z,N,V | 1 |
| DI | Rd, K | Logical AND Register and Constant | Rd ← Rd • K | Z,N,V | 1 |
| | Rd, Rr | Logical OR Registers | Rd ← Rd v Rr | Z,N,V | 1 |
| I | Rd, K | Logical OR Register and Constant | Rd ← Rd v K | Z,N,V | 1 |
| R | Rd, Rr | Exclusive OR Registers | Rd ← Rd ⊕ Rr | Z,N,V | 1 |
| M | Rd | One's Complement | Rd ← $FF – Rd | Z,C,N,V | 1 |
| G | Rd | Two's Complement | Rd ← $00 – Rd | Z,C,N,V,H | 1 |
| R | Rd,K | Set Bit(s) in Register | Rd ← Rd v K | Z,N,V | 1 |
| R | Rd,K | Clear Bit(s) in Register | Rd ← Rd • ($FF - K) | Z,N,V | 1 |
| : | Rd | Increment | Rd ← Rd + 1 | Z,N,V | 1 |
| C | Rd | Decrement | Rd ← Rd – 1 | Z,N,V | 1 |
| T | Rd | Test for Zero or Minus | Rd ← Rd • Rd | Z,N,V | 1 |
| R | Rd | Clear Register | Rd ← Rd ⊕ Rd | Z,N,V | 1 |
| R | Rd | Set Register | Rd ← $FF | None | 1 |
| IL | Rd, Rr | Multiply Unsigned | R1:R0 ← Rd x Rr | Z,C | 2 |
| ILS | Rd, Rr | Multiply Signed | R1:R0 ← Rd x Rr | Z,C | 2 |
| ILSU | Rd, Rr | Multiply Signed with Unsigned | R1:R0 ← Rd x Rr | Z,C | 2 |
| IUL | Rd, Rr | Fractional Multiply Unsigned | R1:R0 ← (Rd x Rr) << 1 | Z,C | 2 |
| IULS | Rd, Rr | Fractional Multiply Signed | R1:R0 ← (Rd x Rr) << 1 | Z,C | 2 |
| IULSU | Rd, Rr | Fractional Multiply Signed with Unsigned | R1:R0 ← (Rd x Rr) << 1 | Z,C | 2 |
| ANCH INSTRUCTIONS | | | | | |
| MP | k | Relative Jump | PC ← PC + k + 1 | None | 2 |
| IP | | Indirect Jump to (Z) | PC ← Z | None | 2 |
| IP | k | Direct Jump | PC ← k | None | 3 |
| CALL | k | Relative Subroutine Call | PC ← PC + k + 1 | None | 3 |
| ALL | | Indirect Call to (Z) | PC ← Z | None | 3 |
| LL | k | Direct Subroutine Call | PC ← k | None | 4 |
| ET | | Subroutine Return | PC ← STACK | None | 4 |
| ETI | | Interrupt Return | PC ← STACK | I | 4 |
| PSE | Rd,Rr | Compare, Skip if Equal | if (Rd = Rr) PC ← PC + 2 or 3 | None | 1/2/3 |
| P | Rd,Rr | Compare | Rd – Rr | Z, N,V,C,H | 1 |
| PC | Rd,Rr | Compare with Carry | Rd – Rr – C | Z, N,V,C,H | 1 |
| PI | Rd,K | Compare Register with Immediate | Rd – K | Z, N,V,C,H | 1 |
| BRC | Rr, b | Skip if Bit in Register Cleared | if (Rr(b)=0) PC ← PC + 2 or 3 | None | 1/2/3 |
| BRS | Rr, b | Skip if Bit in Register is Set | if (Rr(b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| BIC | P, b | Skip if Bit in I/O Register Cleared | if (P(b)=0) PC ← PC + 2 or 3 | None | 1/2/3 |
| BIS | P, b | Skip if Bit in I/O Register is Set | if (P(b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if (SREG(s) = 1) then PC←PC+k + 1 | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if (SREG(s) = 0) then PC←PC+k + 1 | None | 1/2 |
| BREQ | k | Branch if Equal | if (Z = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRNE | k | Branch if Not Equal | if (Z = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRCS | k | Branch if Carry Set | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLO | k | Branch if Lower | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRMI | k | Branch if Minus | if (N = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRPL | k | Branch if Plus | if (N = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if (N ⊕ V= 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if (N ⊕ V= 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if (H = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if (H = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if (T = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if (T = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if (V = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if (V = 0) then PC ← PC + k + 1 | None | 1/2 |

| emonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| E | k | Branch if Interrupt Enabled | if ( I = 1) then PC ← PC + k + 1 | None | 1 / 2 |
| D | k | Branch if Interrupt Disabled | if ( I = 0) then PC ← PC + k + 1 | None | 1 / 2 |
| A TRANSFER INSTRUCTIONS | | | | | |
| / | Rd, Rr | Move Between Registers | Rd ← Rr | None | 1 |
| /W | Rd, Rr | Copy Register Word | Rd+1:Rd ← Rr+1:Rr | None | 1 |
| | Rd, K | Load Immediate | Rd ← K | None | 1 |
| | Rd, X | Load Indirect | Rd ← (X) | None | 2 |
| | Rd, X+ | Load Indirect and Post-Inc. | Rd ← (X), X ← X + 1 | None | 2 |
| | Rd, - X | Load Indirect and Pre-Dec. | X ← X - 1, Rd ← (X) | None | 2 |
| | Rd, Y | Load Indirect | Rd ← (Y) | None | 2 |
| | Rd, Y+ | Load Indirect and Post-Inc. | Rd ← (Y), Y ← Y + 1 | None | 2 |
| | Rd, - Y | Load Indirect and Pre-Dec. | Y ← Y - 1, Rd ← (Y) | None | 2 |
| D | Rd,Y+q | Load Indirect with Displacement | Rd ← (Y + q) | None | 2 |
| | Rd, Z | Load Indirect | Rd ← (Z) | None | 2 |
| | Rd, Z+ | Load Indirect and Post-Inc. | Rd ← (Z), Z ← Z+1 | None | 2 |
| | Rd, -Z | Load Indirect and Pre-Dec. | Z ← Z - 1, Rd ← (Z) | None | 2 |
| D | Rd, Z+q | Load Indirect with Displacement | Rd ← (Z + q) | None | 2 |
| S | Rd, k | Load Direct from SRAM | Rd ← (k) | None | 2 |
| | X, Rr | Store Indirect | (X) ← Rr | None | 2 |
| | X+, Rr | Store Indirect and Post-Inc. | (X) ← Rr, X ← X + 1 | None | 2 |
| | - X, Rr | Store Indirect and Pre-Dec. | X ← X - 1, (X) ← Rr | None | 2 |
| | Y, Rr | Store Indirect | (Y) ← Rr | None | 2 |
| | Y+, Rr | Store Indirect and Post-Inc. | (Y) ← Rr, Y ← Y + 1 | None | 2 |
| | - Y, Rr | Store Indirect and Pre-Dec. | Y ← Y - 1, (Y) ← Rr | None | 2 |
| D | Y+q,Rr | Store Indirect with Displacement | (Y + q) ← Rr | None | 2 |
| | Z, Rr | Store Indirect | (Z) ← Rr | None | 2 |
| | Z+, Rr | Store Indirect and Post-Inc. | (Z) ← Rr, Z ← Z + 1 | None | 2 |
| | -Z, Rr | Store Indirect and Pre-Dec. | Z ← Z - 1, (Z) ← Rr | None | 2 |
| D | Z+q,Rr | Store Indirect with Displacement | (Z + q) ← Rr | None | 2 |
| S | k, Rr | Store Direct to SRAM | (k) ← Rr | None | 2 |
| M | | Load Program Memory | R0 ← (Z) | None | 3 |
| M | Rd, Z | Load Program Memory | Rd ← (Z) | None | 3 |
| M | Rd, Z+ | Load Program Memory and Post-Inc | Rd ← (Z), Z ← Z+1 | None | 3 |
| M | | Store Program Memory | (Z) ← R1:R0 | None | - |
| | Rd, P | In Port | Rd ← P | None | 1 |
| T | P, Rr | Out Port | P ← Rr | None | 1 |
| SH | Rr | Push Register on Stack | STACK ← Rr | None | 2 |
| P | Rd | Pop Register from Stack | Rd ← STACK | None | 2 |
| AND BIT-TEST INSTRUCTIONS | | | | | |
| I | P,b | Set Bit in I/O Register | I/O(P,b) ← 1 | None | 2 |
| I | P,b | Clear Bit in I/O Register | I/O(P,b) ← 0 | None | 2 |
| L | Rd | Logical Shift Left | Rd(n+1) ← Rd(n), Rd(0) ← 0 | Z,C,N,V | 1 |
| R | Rd | Logical Shift Right | Rd(n) ← Rd(n+1), Rd(7) ← 0 | Z,C,N,V | 1 |
| IL | Rd | Rotate Left Through Carry | Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7) | Z,C,N,V | 1 |
| IR | Rd | Rotate Right Through Carry | Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0) | Z,C,N,V | 1 |
| R | Rd | Arithmetic Shift Right | Rd(n) ← Rd(n+1), n=0..6 | Z,C,N,V | 1 |
| VAP | Rd | Swap Nibbles | Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0) | None | 1 |
| ET | s | Flag Set | SREG(s) ← 1 | SREG(s) | 1 |
| LR | s | Flag Clear | SREG(s) ← 0 | SREG(s) | 1 |
| T | Rr, b | Bit Store from Register to T | T ← Rr(b) | T | 1 |
| D | Rd, b | Bit load from T to Register | Rd(b) ← T | None | 1 |
| C | | Set Carry | C ← 1 | C | 1 |
| C | | Clear Carry | C ← 0 | C | 1 |
| N | | Set Negative Flag | N ← 1 | N | 1 |
| N | | Clear Negative Flag | N ← 0 | N | 1 |
| Z | | Set Zero Flag | Z ← 1 | Z | 1 |
| Z | | Clear Zero Flag | Z ← 0 | Z | 1 |
| I | | Global Interrupt Enable | I ← 1 | I | 1 |
| I | | Global Interrupt Disable | I ← 0 | I | 1 |
| S | | Set Signed Test Flag | S ← 1 | S | 1 |
| S | | Clear Signed Test Flag | S ← 0 | S | 1 |
| V | | Set Twos Complement Overflow. | V ← 1 | V | 1 |
| V | | Clear Twos Complement Overflow | V ← 0 | V | 1 |
| ET | | Set T in SREG | T ← 1 | T | 1 |
| T | | Clear T in SREG | T ← 0 | T | 1 |
| H | | Set Half Carry Flag in SREG | H ← 1 | H | 1 |

| nemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| H | | Clear Half Carry Flag in SREG | H ← 0 | H | 1 |
| CU CONTROL INSTRUCTIONS | | | | | |
| )P | | No Operation | | None | 1 |
| EEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| )R | | Watchdog Reset | (see specific descr. for WDR/timer) | None | 1 |
| REAK | | Break | For On-Chip Debug Only | None | N/A |

## atures

ompatible with MCS®-51Products
K Bytes of Reprogrammable Flash Memory
– Endurance: 1,000 Write/Erase Cycles
.7V to 6V Operating Range
ully Static Operation: 0 Hz to 24 MHz
wo-level Program Memory Lock
28 x 8-bit Internal RAM
5 Programmable I/O Lines
wo 16-bit Timer/Counters
ix Interrupt Sources
rogrammable Serial UART Channel
irect LED Drive Outputs
n-chip Analog Comparator
ow-power Idle and Power-down Modes
reen (Pb/Halide-free) Packaging Option

## Description

e AT89C2051 is a low-voltage, high-performance CMOS 8-bit microcomputer with bytes of Flash programmable and erasable read-only memory (PEROM). The vice is manufactured using Atmel's high-density nonvolatile memory technology d is compatible with the industry-standard MCS-51 instruction set. By combining a satile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C2051 is a power- microcomputer which provides a highly-flexible and cost-effective solution to many bedded control applications.

e AT89C2051 provides the following standard features: 2K bytes of Flash, 128 tes of RAM, 15 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt chitecture, a full duplex serial port, a precision analog comparator, on-chip oscillator d clock circuitry. In addition, the AT89C2051 is designed with static logic for opera- n down to zero frequency and supports two software selectable power saving odes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial rt and interrupt system to continue functioning. The power-down mode saves the AM contents but freezes the oscillator disabling all other chip functions until the next rdware reset.

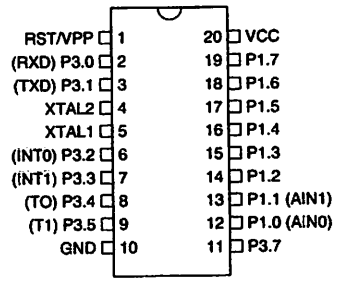
# 8-bit Microcontroller with 2K Bytes Flash

# AT89C2051

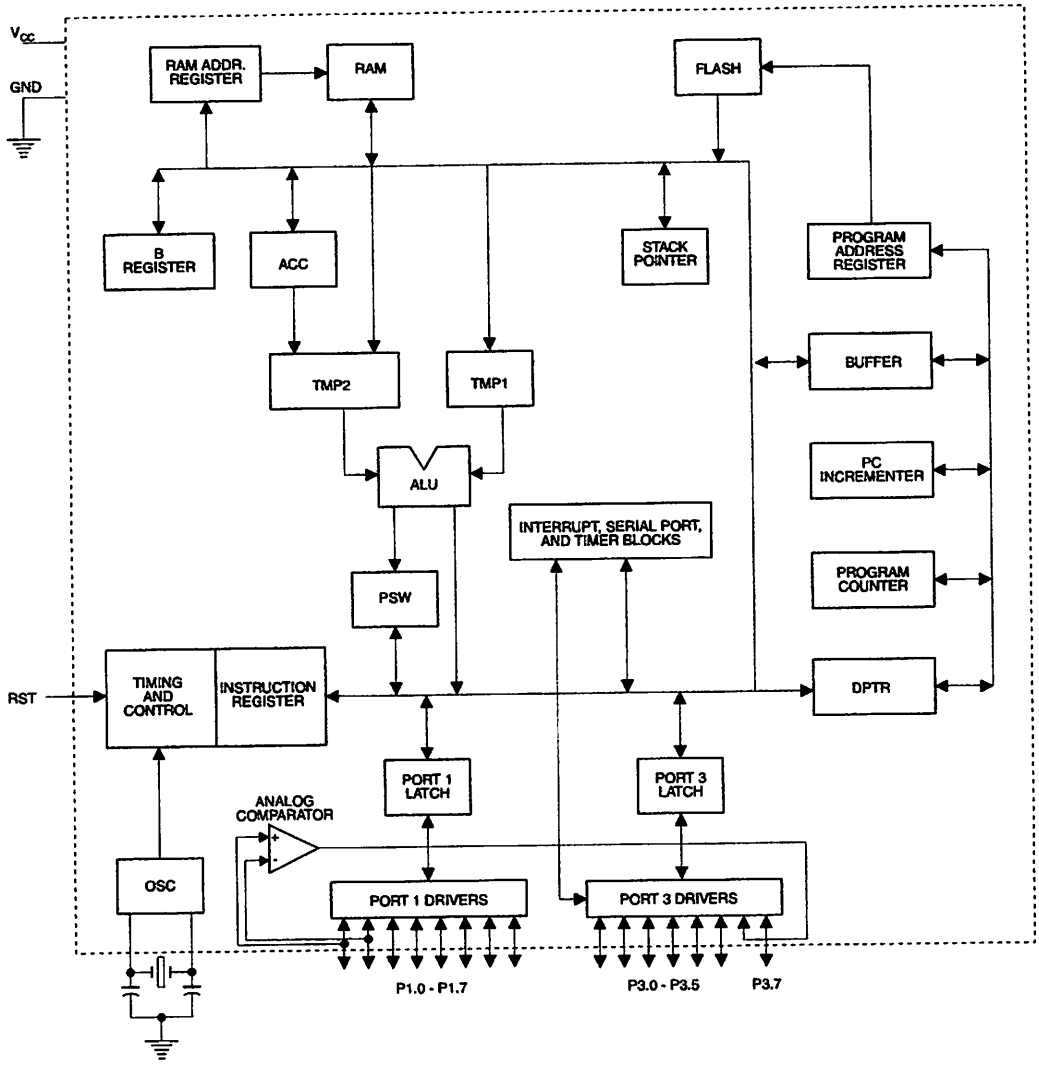
0368G–MICRO–6/05

# Pin Configuration

## 20-lead PDIP/SOIC




# Block Diagram



## Pin Description

### VCC

Supply voltage.

### GND

Ground.

### Port 1

The Port 1 is an 8-bit bi-directional I/O port. Port pins P1.2 to P1.7 provide internal pull-ups. P1.0 and P1.1 require external pull-ups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. The Port 1 output buffers can sink 20 mA and can drive LED displays directly. When 1s are written to Port 1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs and are externally pulled low, they will source current ($I_{IL}$) because of the internal pull-ups.

Port 1 also receives code data during Flash programming and verification.

### Port 3

Port 3 pins P3.0 to P3.5, P3.7 are seven bi-directional I/O pins with internal pull-ups. P3.6 is hard-wired as an input to the output of the on-chip comparator and is not accessible as a general-purpose I/O pin. The Port 3 output buffers can sink 20 mA. When 1s are written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current ($I_{IL}$) because of the pull-ups.

Port 3 also serves the functions of various special features of the AT89C2051 as listed below:

| Port Pin | Alternate Functions |
|---|---|
| P3.0 | RXD (serial input port) |
| P3.1 | TXD (serial output port) |
| P3.2 | $\overline{INT0}$ (external interrupt 0) |
| P3.3 | $\overline{INT1}$ (external interrupt 1) |
| P3.4 | T0 (timer 0 external input) |
| P3.5 | T1 (timer 1 external input) |

Port 3 also receives some control signals for Flash programming and verification.

### RST

Reset input. All I/O pins are reset to 1s as soon as RST goes high. Holding the RST pin high for two machine cycles while the oscillator is running resets the device.

Each machine cycle takes 12 oscillator or clock cycles.

### XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

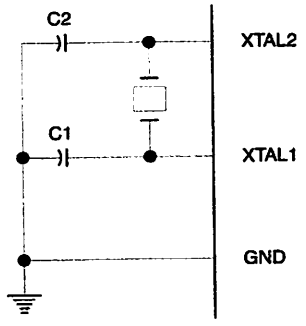
### XTAL2

Output from the inverting oscillator amplifier.

## Oscillator Characteristics

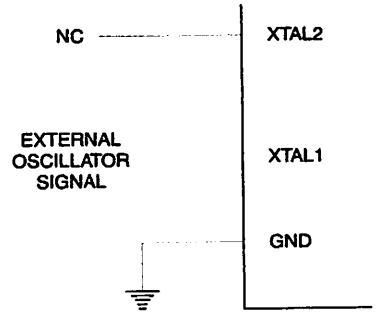
The XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 5-1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 5-2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

**Figure 5-1.** Oscillator Connections




Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

**Figure 5-2.** External Clock Drive Configuration



## Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in the table below.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

**ble 6-1.** AT89C2051 SFR Map and Reset Values

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| F8H | | | | | | | | 0FFH |
| F0H | B<br>00000000 | | | | | | | 0F7H |
| E8H | | | | | | | | 0EFH |
| E0H | ACC<br>00000000 | | | | | | | 0E7H |
| D8H | | | | | | | | 0DFH |
| D0H | PSW<br>00000000 | | | | | | | 0D7H |
| C8H | | | | | | | | 0CFH |
| C0H | | | | | | | | 0C7H |
| B8H | IP<br>XXX00000 | | | | | | | 0BFH |
| B0H | P3<br>11111111 | | | | | | | 0B7H |
| A8H | IE<br>0XX00000 | | | | | | | 0AFH |
| A0H | | | | | | | | 0A7H |
| 98H | SCON<br>00000000 | SBUF<br>XXXXXXXX | | | | | | 9FH |
| 90H | P1<br>11111111 | | | | | | | 97H |
| 88H | TCON<br>00000000 | TMOD<br>00000000 | TL0<br>00000000 | TL1<br>00000000 | TH0<br>00000000 | TH1<br>00000000 | | 8FH |
| 80H | | SP<br>00000111 | DPL<br>00000000 | DPH<br>00000000 | | | PCON<br>0XXX0000 | 87H |

## Restrictions on Certain Instructions

The AT89C2051 and is an economical and cost-effective member of Atmel's growing family of microcontrollers. It contains 2K bytes of Flash program memory. It is fully compatible with the MCS-51 architecture, and can be programmed using the MCS-51 instruction set. However, there are a few considerations one must keep in mind when utilizing certain instructions to program this device.

All the instructions related to jumping or branching should be restricted such that the destination address falls within the physical program memory space of the device, which is 2K for the AT89C2051. This should be the responsibility of the software programmer. For example, LJMP 7E0H would be a valid instruction for the AT89C2051 (with 2K of memory), whereas LJMP 900H would not.

### Branching Instructions

**LCALL, LJMP, ACALL, AJMP, SJMP, JMP @A+DPTR** – These unconditional branching instructions will execute correctly as long as the programmer keeps in mind that the destination branching address must fall within the physical boundaries of the program memory size (locations 00H to 7FFH for the 89C2051). Violating the physical space limits may cause unknown program behavior.

**CJNE [...], DJNZ [...], JB, JNB, JC, JNC, JBC, JZ, JNZ** – With these conditional branching instructions the same rule above applies. Again, violating the memory boundaries may cause erratic execution.

For applications involving interrupts the normal interrupt service routine address locations of the 80C51 family architecture have been preserved.

### MOVX-related Instructions, Data Memory

The AT89C2051 contains 128 bytes of internal data memory. Thus, in the AT89C2051 the stack depth is limited to 128 bytes, the amount of available RAM. External DATA memory access is not supported in this device, nor is external PROGRAM memory execution. Therefore, no MOVX [...] instructions should be included in the program.

A typical 80C51 assembler will still assemble instructions, even if they are written in violation of the restrictions mentioned above. It is the responsibility of the controller user to know the physical features and limitations of the device being used and adjust the instructions used correspondingly.

## Program Memory Lock Bits

On the chip are two lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the Table 8-1.

**Table 8-1.** Lock Bit Protection Modes[1]

| Program Lock Bits | | | |
|---|---|---|---|
| | LB1 | LB2 | Protection Type |
| 1 | U | U | No program lock features |
| 2 | P | U | Further programming of the Flash is disabled |
| 3 | P | P | Same as mode 2, also verify is disabled |

Note: 1. The Lock Bits can only be erased with the Chip Erase operation.

## Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

**The P1.0 and P1.1 should be set to "0" if no external pull-ups are used, or set to "1" if external pull-ups are used.**

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

## . Power-down Mode

In the power-down mode the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before $V_{CC}$ is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

**The P1.0 and P1.1 should be set to "0" if no external pull-ups are used, or set to "1" if external pull-ups are used.**

## . Programming The Flash

The AT89C2051 is shipped with the 2K bytes of on-chip PEROM code memory array in the erased state (i.e., contents = FFH) and ready to be programmed. The code memory array is programmed one byte at a time. *Once the array is programmed, to re-program any non-blank byte, the entire memory array needs to be erased electrically.*

**Internal Address Counter:** The AT89C2051 contains an internal PEROM address counter which is always reset to 000H on the rising edge of RST and is advanced by applying a positive going pulse to pin XTAL1.

**Programming Algorithm:** To program the AT89C2051, the following sequence is recommended.

1. Power-up sequence:
   Apply power between $V_{CC}$ and GND pins
   Set RST and XTAL1 to GND
2. Set pin RST to "H"
   Set pin P3.2 to "H"
3. Apply the appropriate combination of "H" or "L" logic
   levels to pins P3.3, P3.4, P3.5, P3.7 to select one of the programming operations
   shown in the PEROM Programming Modes table.

To Program and Verify the Array:

4. Apply data for Code byte at location 000H to P1.0 to P1.7.
5. Raise RST to 12V to enable programming.
6. Pulse P3.2 once to program a byte in the PEROM array or the lock bits. The byte-write cycle is self-timed and typically takes 1.2 ms.
7. To verify the programmed data, lower RST from 12V to logic "H" level and set pins P3.3 to P3.7 to the appropriate levels. Output data can be read at the port P1 pins.
8. To program a byte at the next address location, pulse XTAL1 pin once to advance the internal address counter. Apply new data to the port P1 pins.
9. Repeat steps 6 through 8, changing data and advancing the address counter for the entire 2K bytes array or until the end of the object file is reached.
10. Power-off sequence:
    set XTAL1 to "L"
    set RST to "L"
    Turn $V_{CC}$ power off

**$\overline{\text{Data}}$ Polling:** The AT89C2051 features $\overline{\text{Data}}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P1.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin any time after a write cycle has been initiated.

**Ready/$\overline{\text{Busy}}$:** The Progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. Pin P3.1 is pulled low after P3.2 goes High during programming to indicate BUSY. P3.1 is pulled High again when programming is done to indicate READY.

**Program Verify:** If lock bits LB1 and LB2 have not been programmed code data can be read back via the data lines for verification:

1. Reset the internal address counter to 000H by bringing RST from "L" to "H".
2. Apply the appropriate control signals for Read Code data and read the output data at the port P1 pins.
3. Pulse pin XTAL1 once to advance the internal address counter.
4. Read the next code data byte at the port P1 pins.
5. Repeat steps 3 and 4 until the entire array is read.

The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

**Chip Erase:** The entire PEROM array (2K bytes) and the two Lock Bits are erased electrically by using the proper combination of control signals and by holding P3.2 low for 10 ms. The code array is written with all "1"s in the Chip Erase operation and must be executed before any non-blank memory byte can be re-programmed.

**Reading the Signature Bytes:** The signature bytes are read by the same procedure as a normal verification of locations 000H, 001H, and 002H, except that P3.5 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(001H) = 21H indicates 89C2051

## . Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

## . Flash Programming Modes

| ode | | RST/VPP | P3.2/PROG | P3.3 | P3.4 | P3.5 | P3.7 |
|---|---|---|---|---|---|---|---|
| rite Code Data[1][3] | | 12V | ⌐‾⌐ | L | H | H | H |
| ead Code Data[1] | | H | H | L | L | H | H |
| rite Lock | Bit - 1 | 12V | ⌐‾⌐ | H | H | H | H |
| | Bit - 2 | 12V | ⌐‾⌐ | H | H | L | L |
| hip Erase | | 12V | ⌐‾⌐ (2) | H | L | L | L |
| ead Signature Byte | | H | H | L | L | L | L |

tes:
1. The internal PEROM address counter is reset to 000H on the rising edge of RST and is advanced by a positive pulse at XTAL1 pin.
2. Chip Erase requires a 10 ms $\overline{\text{PROG}}$ pulse.
3. P3.1 is pulled Low during programming to indicate RDY/$\overline{\text{BSY}}$.

**Figure 13-1.** Programming the Flash Memory

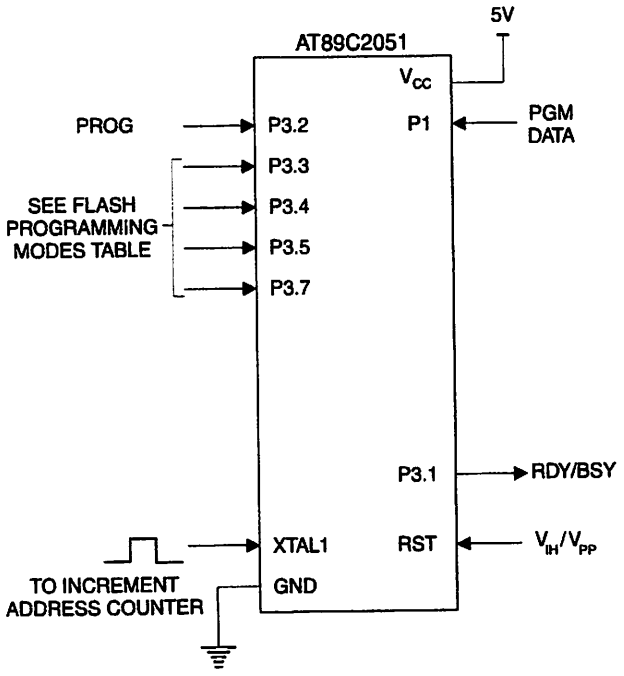
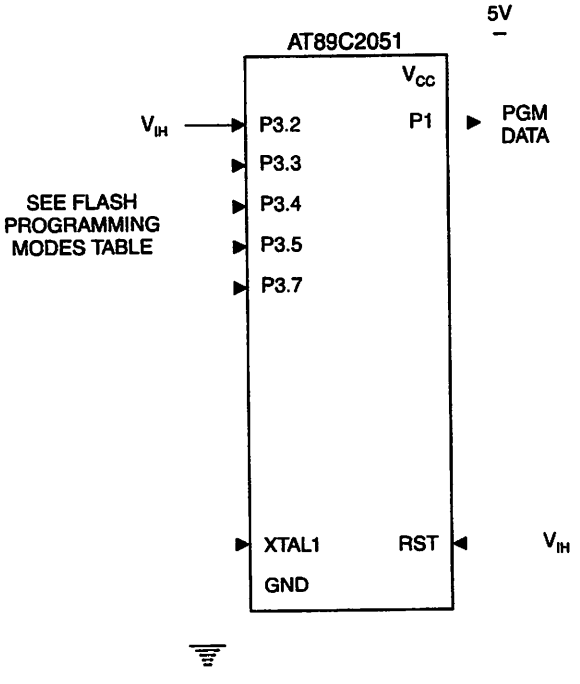



**Figure 13-2.** Verifying the Flash Memory



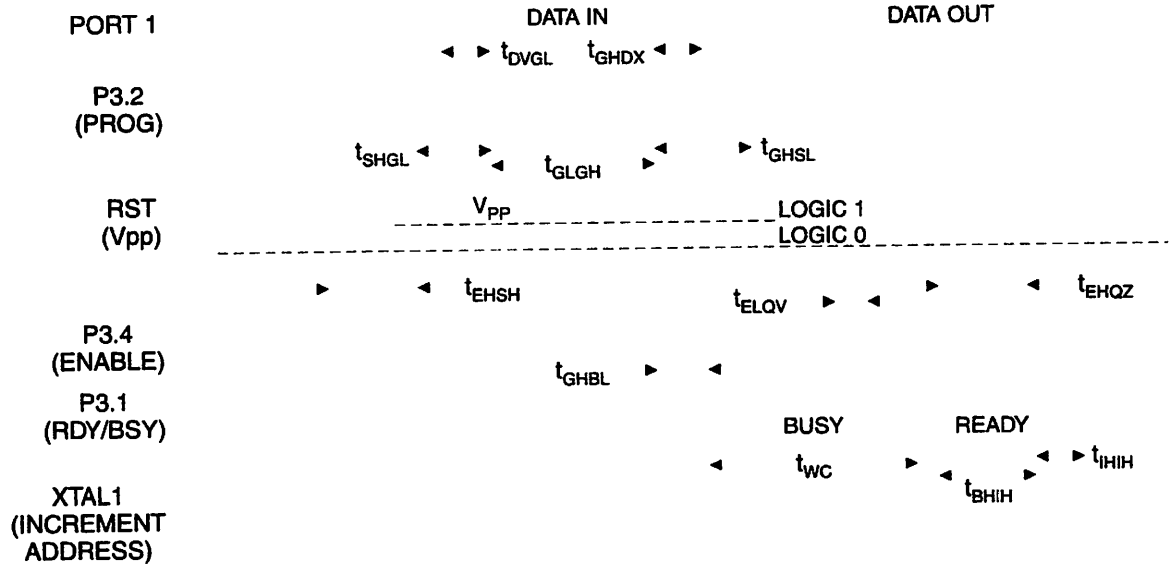
## Flash Programming and Verification Characteristics

: 0°C to 70°C, $V_{CC}$ = 5.0 ± 10%

| mbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| P | Programming Enable Voltage | 11.5 | 12.5 | V |
| | Programming Enable Current | | 250 | µA |
| GL | Data Setup to $\overline{PROG}$ Low | 1.0 | | µs |
| DX | Data Hold after $\overline{PROG}$ | 1.0 | | µs |
| SH | P3.4 ($\overline{ENABLE}$) High to $V_{PP}$ | 1.0 | | µs |
| GL | $V_{PP}$ Setup to $\overline{PROG}$ Low | 10 | | µs |
| SL | $V_{PP}$ Hold after $\overline{PROG}$ | 10 | | µs |
| GH | $\overline{PROG}$ Width | 1 | 110 | µs |
| QV | $\overline{ENABLE}$ Low to Data Valid | | 1.0 | µs |
| QZ | Data Float after $\overline{ENABLE}$ | 0 | 1.0 | µs |
| BL | $\overline{PROG}$ High to $\overline{BUSY}$ Low | | 50 | ns |
| C | Byte Write Cycle Time | | 2.0 | ms |
| IH | RDY/$\overline{BSY}$\ to Increment Clock Delay | 1.0 | | µs |
| IL | Increment Clock High | 200 | | ns |

e: 1. Only used in 12-volt programming mode.

## Flash Programming and Verification Waveforms



## . Absolute Maximum Ratings*

| | |
|---|---|
| erating Temperature | -55°C to +125°C |
| rage Temperature | -65°C to +150°C |
| ltage on Any Pin h Respect to Ground | -1.0V to +7.0V |
| ximum Operating Voltage | 6.6V |
| Output Current | 25.0 mA |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

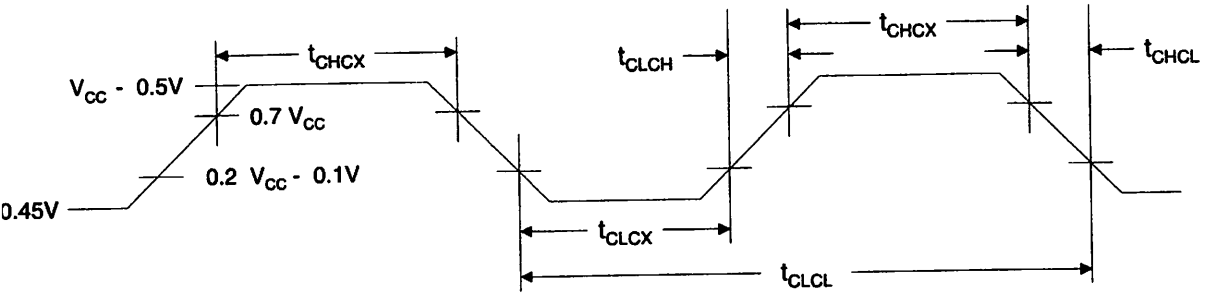
## . DC Characteristics

= -40°C to 85°C, $V_{CC}$ = 2.7V to 6.0V (unless otherwise noted)

| mbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| L | Input Low-voltage | | -0.5 | 0.2 $V_{CC}$ - 0.1 | V |
| H | Input High-voltage | (Except XTAL1, RST) | 0.2 $V_{CC}$ + 0.9 | $V_{CC}$ + 0.5 | V |
| H1 | Input High-voltage | (XTAL1, RST) | 0.7 $V_{CC}$ | $V_{CC}$ + 0.5 | V |
| OL | Output Low-voltage[1] (Ports 1, 3) | $I_{OL}$ = 20 mA, $V_{CC}$ = 5V<br>$I_{OL}$ = 10 mA, $V_{CC}$ = 2.7V | | 0.5 | V |
| OH | Output High-voltage (Ports 1, 3) | $I_{OH}$ = -80 µA, $V_{CC}$ = 5V ± 10% | 2.4 | | V |
| | | $I_{OH}$ = -30 µA | 0.75 $V_{CC}$ | | V |
| | | $I_{OH}$ = -12 µA | 0.9 $V_{CC}$ | | V |
| | Logical 0 Input Current (Ports 1, 3) | $V_{IN}$ = 0.45V | | -50 | µA |
| L | Logical 1 to 0 Transition Current (Ports 1, 3) | $V_{IN}$ = 2V, $V_{CC}$ = 5V ± 10% | | -750 | µA |
| I | Input Leakage Current (Port P1.0, P1.1) | 0 < $V_{IN}$ < $V_{CC}$ | | ±10 | µA |
| OS | Comparator Input Offset Voltage | $V_{CC}$ = 5V | | 20 | mV |
| CM | Comparator Input Common Mode Voltage | | 0 | $V_{CC}$ | V |
| RST | Reset Pull-down Resistor | | 50 | 300 | kΩ |
| IO | Pin Capacitance | Test Freq. = 1 MHz, $T_A$ = 25°C | | 10 | pF |
| CC | Power Supply Current | Active Mode, 12 MHz, $V_{CC}$ = 6V/3V | | 15/5.5 | mA |
| | | Idle Mode, 12 MHz, $V_{CC}$ = 6V/3V<br>P1.0 & P1.1 = 0V or $V_{CC}$ | | 5/1 | mA |
| | Power-down Mode[2] | $V_{CC}$ = 6V, P1.0 & P1.1 = 0V or $V_{CC}$ | | 100 | µA |
| | | $V_{CC}$ = 3V, P1.0 & P1.1 = 0V or $V_{CC}$ | | 20 | µA |

tes:
1. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 20 mA
   Maximum total $I_{OL}$ for all output pins: 80 mA
   If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum $V_{CC}$ for Power-down is 2V.

## External Clock Drive Waveforms




## . External Clock Drive

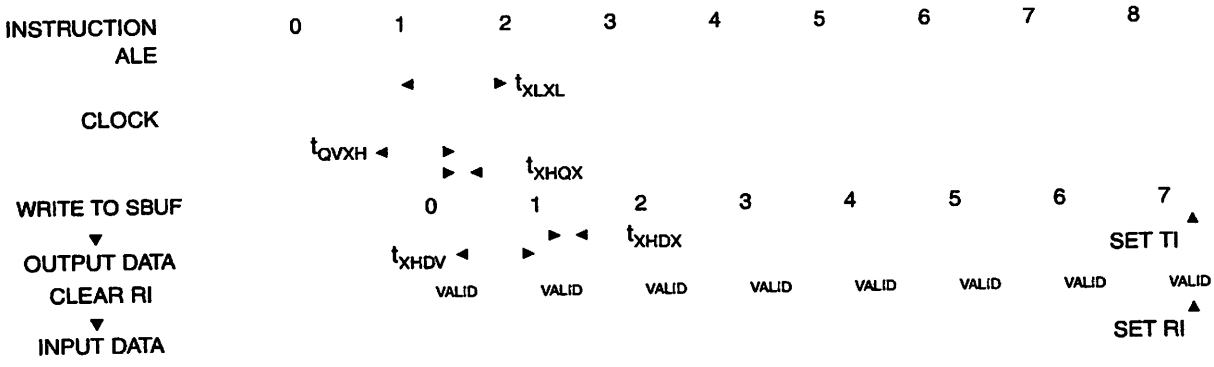
| mbol | Parameter | $V_{CC}$ = 2.7V to 6.0V | | $V_{CC}$ = 4.0V to 6.0V | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| CLCL | Oscillator Frequency | 0 | 12 | 0 | 24 | MHz |
| CL | Clock Period | 83.3 | | 41.6 | | ns |
| CX | High Time | 30 | | 15 | | ns |
| CX | Low Time | 30 | | 15 | | ns |
| CH | Rise Time | | 20 | | 20 | ns |
| CL | Fall Time | | 20 | | 20 | ns |

## ). Serial Port Timing: Shift Register Mode Test Conditions

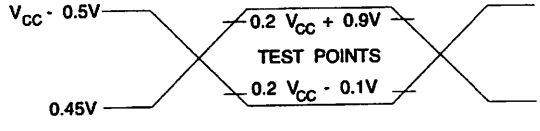
= 5.0V ± 20%; Load Capacitance = 80 pF

| ymbol | Parameter | 12 MHz Osc | | Variable Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| XL | Serial Port Clock Cycle Time | 1.0 | | 12 $t_{CLCL}$ | | µs |
| VXH | Output Data Setup to Clock Rising Edge | 700 | | 10 $t_{CLCL}$-133 | | ns |
| HQX | Output Data Hold after Clock Rising Edge | 50 | | 2 $t_{CLCL}$-117 | | ns |
| HDX | Input Data Hold after Clock Rising Edge | 0 | | 0 | | ns |
| HDV | Clock Rising Edge to Input Data Valid | | 700 | | 10 $t_{CLCL}$-133 | ns |

## Shift Register Mode Timing Waveforms

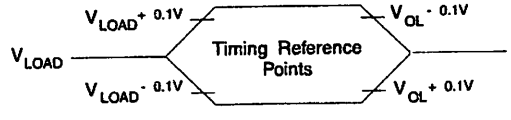



## . AC Testing Input/Output Waveforms[1]




e: 1. AC Inputs during testing are driven at $V_{CC}$ - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at $V_{IH}$ min. for a logic 1 and $V_{IL}$ max. for a logic 0.

## . Float Waveforms[1]




te: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded $V_{OH}/V_{OL}$ level occurs.