TUGAS AKHIR

PENGUKUR TEKANAN DARAH DIGITAL DENGAN PEMANFAATAN MIKROKONTROLER AT89S51

Disusun Oleh :

NAMA : M. ALI ROFIK

NIM : 04.52.215

JURUSAN TEKNIK ELEKTRO DIII

KOSENTRASI TEKNIK ELEKTRONIKA DIII

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

SEPTEMBER 2008

LEMBAR PERSETUJUAN
TUGAS AKHIR

PENGUKUR TEKANAN DARAH DIGITAL DENGAN PEMANFAATAN MIKROKONTROLER AT89S51

Disusun oleh :

Nama : M. ALI ROFIK
Nim : 04.52.215

Mengetahui	Diperiksa dan Disetujui
Ketua Program Studi	Dosen Pembimbing
Teknik Elektro D-III	
Ir. H.Choirul Saleh, MT	**Ir. F. Yudi Lipraptono, MT**
NIP. Y. 1018.800.190	**NIP. Y. 1039.500.274**

KONSENTRASI TEKNIK ELEKTRONIKA D-III
JURUSAN TEKNIK ELEKTRO D-III
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
SEPTEMBER 2008

ABSTRAK

PENGUKURAN TEKANAN DARAH DIGITAL DENGAN PEMANFAATAN MIKROKONTROLER AT89S51

(Muhammad Ali Rofik)
(Dosen Pembimbing : Ir. F. Yudi Lipraptono, MT)

Perencanaan dan pembuatan alat pengukur tekanan darah secara digital berbasisi mikrokontroler ini dibuat untul mengetahui nilai tekanan darah secara lebih presisi dibanding dengan pengukuran secara analog dengan menggunakan air raksa, dan penunjuk jarum. Dalam perencanaan dan pembuatan alat ini digunakan komponen yang mendukung untuk pengukuran tekanan darah, seperti sensor MPX2050GP sebagai sensor tekanan, dan kondensor mic yang digunakan untuk sensor suara.
Pendeteksian terhadap kenaikan tekanan dilkukan oleh sensor MPX2050GP, sedangkan untuk mendeteksi suara detak jantung digunakan kondensor mic. Komponen utama yang digunakan adalah mikrokontroler AT89S51 dan untuk pengoperasian alat digunakan perangkat lunak (sofware) menggunakan bahasa Assembly. Komponen tersebut akan menerima input berupa data dari sensor suara dan ADC, yang kemudian diproses sehingga menghasilkan outputan tampilan dari LCD dan ISD, sesuai dengan penggunaannya untuk mengukur tekanan darah manusia. Hasil pengukuran ditampilkan oleh LCD 2 x16 M1632, dan suara oleh ISD 2560 berupa tekanan sistolik dan diastolik user, yang mana untuk tekanan normal adalah ± 110 mmHg – 120 mmHg untuk tekanan sistole, dan ± 70 mmHg – 80 mmHg untuk tekanan diastole.

Kata Kunci : LCD & ISD, AT89S51, Tekanan Darah Digital, Pengukuran.

LEMBAR PERSEMBAHAN

بِسْمِ اللَّهِ الرَّحْمَٰنِ الرَّحِيمِ

يَرْفَعِ اللَّهُ الَّذِينَ آمَنُوا مِنكُمْ وَالَّذِينَ أُوتُوا الْعِلْمَ دَرَجَاتٍ

Pertama- tama aku panjatkan puji dan syukur kepada allah SWT, yang telah memberikan rahmad, taufiq dan Hidayah kepada penulis dan memberikan kemudahan selama proses TA, dan akhirnya aku bisa lulus. Sholawat serta salam selalu aku persembahkan kepada beliau Nabi besar Muhammad SAW, yang telah memberikan petunjuk kepada seluruh alam.

Kupersembahkan karyaku ini, Kepada kedua orang tuaku yang selalu aku hormati dan banggakan, yang telah memberikan pengorbanan begitu besar kepada penulis mulai kecil hingga dewasa, sampai akhirnya bisa lulus kuliah. Pengorbanan dan usaha kalian merupakan ibadah yang semoga dapat menjadi bukit pahala yang dapat memberikan manfaat di dunia dan akhirat. Disini penulis tidak dapat memberikan suatu yang lebih, ataupun yang terbaik, tapi penulis akan selalu berusaha untuk melakukan itu. Amin. Dan untuk semua saudaraku, makasih telah sabar memberikan dorongan kepada penulis, baik materi, saran, tenaga dan semuanya. Makasih banyak……., smoga aku dapat membalas dengan yang lebih baik. Amin.

TO : temen-temen kampus My friends : Beny, Rudra, Oland, Malik, Nita, Dani,.. semuanya angkatan 2004, makasih atas semuanya, kalian adalah teman seperjuangan, suka & duka telah kita rasakan bersama, kuharap kenangan yang ada takkan terlupa sampai kapanpun, persahabatan adalah sesuatu yang indah yang kekal, yang dapat memberikan berkah di dunia dan akhirat.

Buat teman-teman yang belum lulus, sabar…, sabar…., sabar……., pasti ada waktunya, telat bukan berarti kalah…., pasti ada suatu hikmah dibalik segalanya, yang jelas tetap positif thingking, selalu bersyukur, jalani dan goal.

Buat temen2ku yang bisa aku sebutin satu persatu, makasi dah support n daoin aku selama ini. Buat seseorang yang selalu aku kagumi…., lanjutkan perjuanganmu tuk menuntut ilmu, jadilah pencinta ilmu (حُبُّ ا لعِلم) karena ilmu memang pantas untuk dicintai "ilmu iku cahaya yang akan selalu menerangi" , makasih atas semuanya…..

Buat semuanya temen2 yang lulus, kita dah lulus tapi ingat ada sesuatu yang lebih sulit dari pada membuat sebuah Tugas Akhir, kita akan menghadapi dunia nyata, kehidupan perjuangan untuk masa depan kita, masa depan di dunia dan di akhirat. Selalu ingat jalan yang lurus,…. Jangan sia-siakan pengorbanan kedua orang tua kalian, perjuangan kita. Ingat meskipun tidak bisa menjadi yang terbaik, jadilah orang baik.

KATA PENGANTAR

Dengan mengucap puji syukur kepada Allah SWT, atas limpahan rahmat dan hidayah-Nya, serta perlindungan, pertolongan dan ridho-Nya sehingga penulis dapat menyelesaikan Tugas Akhir ini tepat pada waktunya, serta tak terlupakan iringan salam dan sholawat bagi junjungan kami Nabi besar Muhammad SAW.

Tugas Akhir ini suatu kewajiban yang dilakukan bagi setiap mahasiswa Institut Teknologi Nasuonal Malang dengan tujuan untuk memenuhi persyaratan untuk memperoleh kelulusan pada program Diploma III Jurusan Teknik Elektronika D-III di Institut Teknologi Nasuonal Malang.

Dengan pengerahan segenap usaha, akhirnya kami dapat menyelesaikan tugas akhir kami yang berjudul : " **PENGUKURAN TEKANAN DARAH DIGITAL DENGAN PEMANFAATAN MIKROKONTROLER AT89S51** "

Pembuatan Tugas Akhir ini telah banyak melibat banyak orang, maka sepantasnya bila penulis mencoba mengucapkan terima kasih kepada :

1. Bapak Prof. Dr. Ir. Abraham Lomi, MSEE, selaku rektor Institut Teknologi Nasional Malang
2. Bapak Ir. Choirul Saleh, MT selaku Ketua Jurusan Teknik Elektro D-III Institut Teknologi Nasional Malang
3. Bapak Ir. F. Yudi Lipraptono, MT selaku dosen pembimbing Tugas Akhir.
4. Kepada semua pihak yang telah membantu penyelesaian Tugas Akhir ini.

Dengan terselesaikannya buku laporan tugas akhir ini, kami berharap semoga buku ini dapat membawa manfaat bagi pembaca umumnya dan juga bagi kami pada khususnya serta semua pihak yang berkepentingan. Kami menyadari bahwa kami adalah manusia biasa yang tidak luput dari kesalahan dan kekurangan. Untuk itu, kritikan dan saran yang bersifat membangun kami harapkan untuk perbaikan selanjutnya.

Malang, September 2008

Penulis

DAFTAR ISI

DAFTAR GAMBAR

DAFTAR TABEL

BAB I

PENDAHULUAN

1.1 Latar Belakang

Jantung merupakan organ tubuh yang berfungsi untuk memompa darah yang dialirakn tubuh manusia dan hal ini dilakukan secara terus menerus. Karean fungsinya yang sangat penting itulah, maka kita harus senantiasa menjaga kesehatan.

Di dalam bidang kedokteran tidak dapat dipungkiri bahwa saat ini orang telah banyak mendapat masalah mengenai kondisi kesehatannya. Salah satu cara yang paling banyak digunakan untuk mengamati tingkat kesehatan seseorang adalah dengan melihat tekanan darah dan detak jantung. Tekanan darah merupakan faktor yang amat penting pada sistem sirkulasi. Peningkatan atau penurunan teknanan darah rata-rata akan mempengaruhi sistem kerja tubuh.

Tapi kebanyakan orang melihat tekanan darah menggunakan alat berbentuk analog yaitu dengan melihat air raksa dan suara dan pentrakrof sehingga hanya beberapa orang yang mengerti yang bisa menjalankan alat itu.

Berangkat dari permasalah diatas, maka timbul suatu ide gagasan untuk membuat suatu alat yang dapat mengetahui tekanan darah pada tubuh secara digital yang dapat dan mudah untuk dimengerti dan dilihat secara cepat dan tepat. Sehingga dengan adanya alat dapat membantu baik dokter maupun orang awam yang dalam bidang kedokteran untuk melihat darah.

Pada perencaaan alat ini secara otomatis akan dapat menampilkan besarnya tekanan darah yang sedang mengalir dalam tubuh manusia, dan sebagai sarana pengindera dari tekanan darah adalah digunakan tranduser tekanan (MPX2050) serta mikrokontroler AT89S51 sebagai pengontrol alat secara keseluruhan, LCD dan ISD sebagai tampilan dan keluaran suara serta Kondensor Mic sebagai sensor suara jantung.

1.2 Rumusan Masalah

Dalam perancangan dan pembuatan pengukur tekanan darah digital ini dapat dirumuskan beberapa masalah yang akan dibahas sebagai berikut :

1. Bagaimana merancang dan membuat alat pengukur tekanan darah yang menggunakan mikrokontroler AT89S51?
2. Bagaimana cara mengubah besaran tekanan yang terdapat pada manset (Hand Cuff), serta kondensor mic menjadi besaran analog yang dapat dibaca oleh mikrokontroler serta dapat ditampilkan pada LCD dan ISD sebagai outputan suara ?

1.3 Tujuan

Tujuan dari pembuatan alat ini adalah digunakan untuk Tugas Akhir untuk membuat alat yang dapat mengukur tekanan darah pada tubuh secara digital yang ditampilkan melalui sebuah LCD dan ISD yang dikendalikan oleh sebuah mikrokontroler AT89S51 sehingga dapat membantu masyarakat bila memerlukan pengukuran darah secara mudah.

1.4 Batasan Masalah

Sehubungan dengan tugas dan pembuatan alat yang cukup lengkap, maka penulis akan membatasi masalah tersebut dengan tujuan untuk mencegah kemungkinan terjadi perluasan dan penyimpangan pembahasan dari fokus permasalahan, berhubung keterbatasan waktu dan biaya, maka diperlukan pembatasan permasalahan yang meliputi :

1. Hanya membahas tentang arsitektur AT89S51
2. Untuk memompa cuff dilakukan secara otomatis dengan menggunakan motor sehingga alat ini lebih praktis.
3. Pada alat ini ouput ditampilkan pada LCD dan juga menggunakan keluaran suara.
4. Alat pengukur tekanan darah ini memerlukan daya 5 Volt.

1.5 Metodologi Peneletian

Metodologi penelitian yang dipakai skripsi ini adalah :

1. Studi literatur yang mempelajari teori-teori yang berkaitan mengenai cara kerja komponen yang digunakan dalam Perancangan dan Pembuatan Alat Pengukur Tekanan Darah digital berbasis Mikrokontroler AT89S51
2. Perencanaan dan Pembuatan alat pengukur Tekanan darah Digital berbasis Mikrokontroler AT89S51
3. Pelaksanaan uji coba alat dari hasil Perancangan dan Pembuatan Alat Pengukur Tekanan Darah Digital Berbasis Mikrokontroler AT89S51
4. Penyusunan Tugas Akhir dan menyimpulkan hasil perancangan dan pembuatan alat.

1.6 Sistematika Penulisan

Sistematika penulisan yang akan digunakan untuk membahas masalah dalam Tugas Akhir ini diperlukan gambaran susunan alat secara keseluruhan yang selanjutnya ditentukan komponen-komponen utama dan pendukung yang digunakan dan kemungkinan untuk disederhanakan baik untuk bentuk, biaya pembuatannya agar didapatkan susunan yang seefisien dan seefektif mungkin.

Adapun pembahasan Tugas Akhir ini dibagi menjadi beberapa bab sebagai berikut :

BAB I Pendahuluan, yang memuat latar belakang, Rumusan Masalah, Tujuan, Batasan Masalah, Metodologi serta Sistematika Penulisan.

BAB II Teori Dasar, berisi tentang dasar-dasar teori peralatan yang digunakan.

BAB III Perencanaan dan pembuatan alat, membahas tentang perencanaan dan pembuatan alat yang akan dibuat.

BAB IV Analisa dan Pengujian Alat, berisikan tentang pengujian alat yang telah dibuat, pengoperasian dan spesifikasi alat.

BAB V Penutup, yang berisi kesimpulan dan saran.

BAB II

DASAR TEORI

2.1 Pengertian Tekanan Darah

Dalam sistem sirkulasi darah dalam tubuh, tekanan darah merupakan parameter yang sangat penting, mengingat selalu diperlukan untuk daya dorong mengalirnya darah dalam pembulu arteri, arteriola, kapiler dan sistem vena. Jantung adalah bagian organ tubuh yang berfungsi sebagai pemompa darah. Dengan adanya aktifitas jantung, maka terjadilah aliran darah dari pembulu vena ke pembulu arteri pada sistem sirkulasi tertutup. ada dua jenis pengukuran tekanan darah *(blood pressure)*, yaitu sistolik dan diastolik. *Yang dimaksud dengan tekanan darah disini adalah tenaga yang dikeluarkan oleh darah untuk dapat mengalir melalui pembuluh darah.* Ukuran tekanan darah dinyatakan dalam bentuk mmHg. Hg merupakan singkatan dari *hydragyrum*, yaitu merupakan air raksa yang ada didalam tabung tensi meter. Jadi jika tekanan darah seseorang adalah sebesar 140 mm Hg, maka maksudnya adalah tenaga yang dikeluarkan oleh darah untuk mendorong air raksa didalam tabung tensimeter setinggi 140 mm.

2.1.1 Sistole dan Diastole

Aktivitas jantung yang memompa darah dengan cara mengadakan kontraksi dan relaksasi, menimbulkan tekanan darah di dalam sistem sirkulasi. Pada waktu sistole ventrikel (fase ejeksi cepat) darah dipompa ke

aorta dan arteri para tekanan arteri pada saat itu naik sampai sekitar 120 mmHg, tekanan ini yang dalam pengukuran tekanan darah disebut sebagai tekanan *sistolik.* Kenaikan tekanan darah ini menyebabkan aorta mengalami distensi, sehingga tekanan di dalamya turun sedikit, jika dilihat pada grafik tekanan darah terhadap waktu, maka akan dilihat sebagai incisure atau celah akibat penurunan tekanan sesaat dan disusul dengan kenaikannya kembali. Pada saat diastole ventrikel, maka tekanan aorta cenderung sampai dengan sekitar 80 mmHg, tekanan inilah yang pada saat pemeriksaan tekanan darah dikenal sebagai tekanan *diastolik.*

Tekanan pada orang dewasa sangat bervariasi. Tekanan darah terdiri dari tekanan sistolik yang berkisar antara 95 mmHg – 140 mmHg, tekanan yang dapat meningkat dengan bertambahnya usia, dilain pihak tekanan diastolik berkisar antara 60 mmHg – 90 mmHg. Namun tekanan darah normal biasanya berkisar antara 120 mmHg untuk sistolik dan 80 mmHg untuk tekanan diastolik. Tekanan darah normal dipengaruhi oleh beberapa faktor antara lain : usia, jenis kelamin, perjalanan dalam sehari semalam yang membentuk perubahan tekanan darah. Tekanan darah normal untuk usia dan jenis kelamin tertentu bukan merupalan nilai tertentu, tetapi berupa range tertentu seperti diperlihatkan pada tabel 2.1 dibawah ini.

Table. 2.1 Harga rata-rata sistolik dan diastolik berdasarakan usia dan jenis kelamin. [1]

USIA	PRIA		WANITA	
	Sistolik (mmHd)	Diastolik (mmHg)	Sistolik (mmHg	Diastolik (mmHg)
20 – 24	128 ± 14	75 ± 13	121 ± 13	75 ± 12
25 – 29	128 ± 14	75 ± 22	122 ± 15	73 ± 12
30 – 34	129 ± 16	77 ± 14	124 ± 15	75 ± 12
35 – 39	130 ± 18	79 ± 15	127 ± 17	78 ± 13
40 – 44	132 ± 19	81 ± 14	132 ± 20	80 ± 13
45 – 49	136 ± 22	83 ± 14	140 ± 26	84 ± 16
50 – 54	144 ±26	87 ± 16	147 ± 28	86 ± 15
55 – 59	150 ± 27	88 ± 16	150 ± 28	88 ± 16
60 – 64	156 ± 28	91 ± 16	158 ± 30	90 ± 16
65 – 69	158 ± 30	89 ± 17	166 ± 30	91 ± 15
Over 70	165 ± 32	89 ± 17	171 ± 31	91 ± 16

2.1.2 Pengukuran Tekanan Darah

Berdasarkan caranya, pengukuran tekanan darah dapat dibagi menjadi dua bagian yaitu : a. pengukuran secara langsung *(invasive)* dan pengukuran darah secara tidak langsung *(non invasive)*.

2.1.2.1 Pengukuran secara Langsung (invasive)

Pengukuran tekanan darah secara langsung *(invasive)* yaitu dengan memasukkan alat pengukur ke dalam tubuh atau melalui cara pembedahan terhadap pasien. Pengukuran langsung ini pertama kali dilakukan oleh Professor dari Lyon dengan menggunakan alat pengukur tekanan darah hemodynamometer. Pengukuran model ini masih digunakan di rumah sakit modern untuk mengukur tekanan cairan sumsum tulang belakang *(spiral fluid)* dan tekanan vena pusat (*central venous pressure (CVP)*).

2.1.2.2 Pengukuran Secara Tak Langsung (non invasive)

Pengukuran tekanan darah secara tak langsung yaitu pengukuran yang dilakukan diluar tubuh pasien. Selain mudah, pengukuran jenis ini juga tidak berbahaya bagi pasien, oleh karena itu pengukuran secara tak lansung lebih banyak digunakan.

Pengukuran darah secara tak langsung memerlukan piranti yang disebut *Sphygmomanometer*, yang terdiri dari balon karet *(bladder)* yang dapat dikembangkan dan terbungkus oleh sarung kain atau bisa disebut manset *(hand cuff)*, karet pompa udara, 2 buah pipa karet dan sebuah manometer. Pada pengukuran tekanan darah secara tak langsung ada beberapa metode yang digunakan untuk menentukan besarnya tekanan darah, antara lain.

1. Metode Palpalasi

   Metode palpasi yaitu menggunakan indera peraba untuk menentukan denyut pasien pada arteri radialis. caranya dengan menaikkan tekanan manset yang telah dipasang pada lengan kanan atas sampai denyut arteri radialis lenyap/hilang. Kemudian operator membuka katub udara pada manset sampai suatu pulsa menjadi teraba pada arteri, tekanan pada saat kondisi ini terjadi merupakan tekanan sistolik. Metode ini hanya bisa mendeteksi tekanan sistolik sebab terdapat perubahan yang tidak terpalpasi (teraba) yang terjadi pada tekanan diastolik, sehingga teknik ini sering kali tak bisa digunakan pada penderita hipotensi atau penderita tekanan darah rendah.

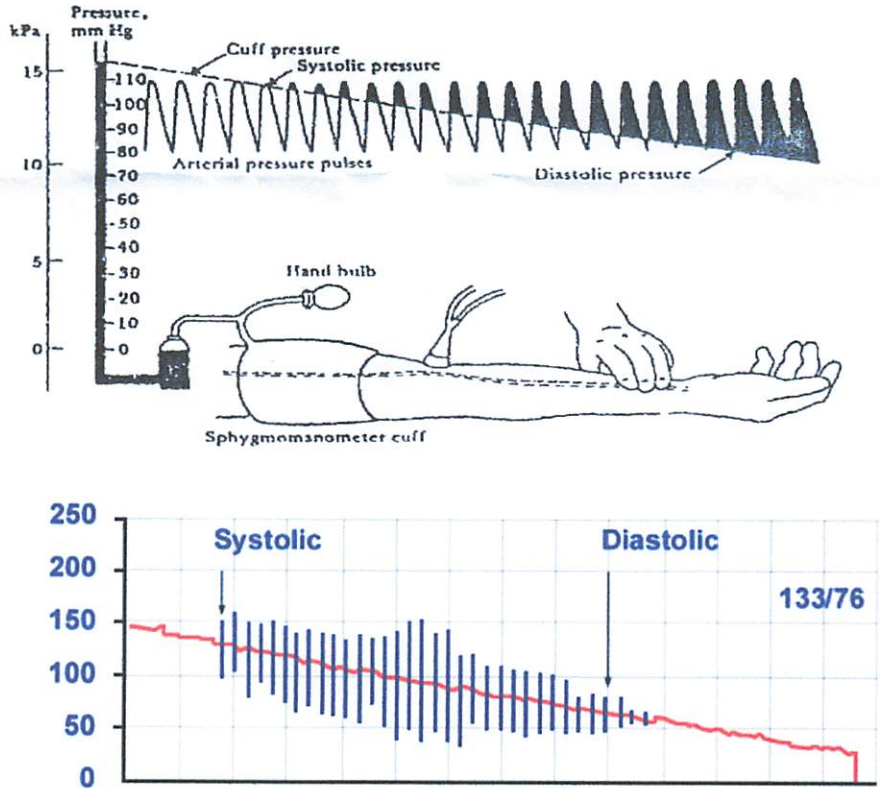
2. Metode Auskultasi

Metode auskultasi yaitu menggunakan pendengaran untuk menentukan denyut pasien, yaitu dengan cara mendengarkan suara dari stetoskop yang disebut dengan suara *korotkoff*, metode inilah yang paling banyak digunakan dalam menentukan besarnya nilai tekanan darah.

Prosedur pengukuran tekanan darah dengan menggunakan metode auskultasi ini adalah sebagai berikut :

1. Manset dibelitkan melingkar pada lengan atas pasien pada titik pertengahan antara siku dan bahu. Stetoskop diletakkan diatas arteri brakialis, dengan tekanan yang ringan agar semua ujung stetoskop melekat rapat di kulit.
2. Manset dikembangkan sehingga tekanan dalam balon karet mencapai suatu harga lebih besar dari tekanan sistolik yang diperkirakan. Tekanan ini menekan dan menjepit jaringan di lengan atas kanan, menyebabkan pembuluh darah menguncup. Karena tekanan manset melebihi tekanan sistolik pembuluh arteri brakialis, maka tidak ada aliran darah ke lengan bawah dan jari.
3. kemudian operator mengurangi dengan perlahan (kira-kira 3 mmHg/s, tekanan di dalam manset dan mengamati nilai meteran tekanan atau kolom air raksa. Bila tekanan sistolik pertama melebih tekanan manset, operator mulai mendengar bunyi detakan atau suara Korotkoff yaitu bunyi dalam stetoskop yang diakibatkan

oleh pancaran darah yang mencoba mendorong melalui manset tersebut. Suara korotkoff hilang atau menjadi tersaring bila tekanan manset jatuh dibawah tekanan diastolik penderita. Untuk membaca tekanan darah, operator mencatat nilai tekanan saat suara mulai ada (sistolik) dan juga saat suara korotkoff hilang (diastolik). Tekanan ini biasanya dicatat dalam perbandingan sistolik dan diastolik (misalnya 110/90). Metode ini hanya mempunyai kelemahan yaitu pengukuran harus dilakukan pada tempat yang tenang, agar suaru Korotkoff dapat terdengan jelas.



Gambar 2.1 Ilustrasi Pengkuran tekanan Darah Auskultasi [2]

3. Metode Osilometri

Metode osilometri yang menggunakan osilasi pada kolom air raksa untuk menentukan tekanan sistolik dan diastolik. Untuk mengamati osilasi yang terjadi ini diperlukan perhitungan-perhitungan dari komputer agar hasil yang diperoleh lebih akurat.

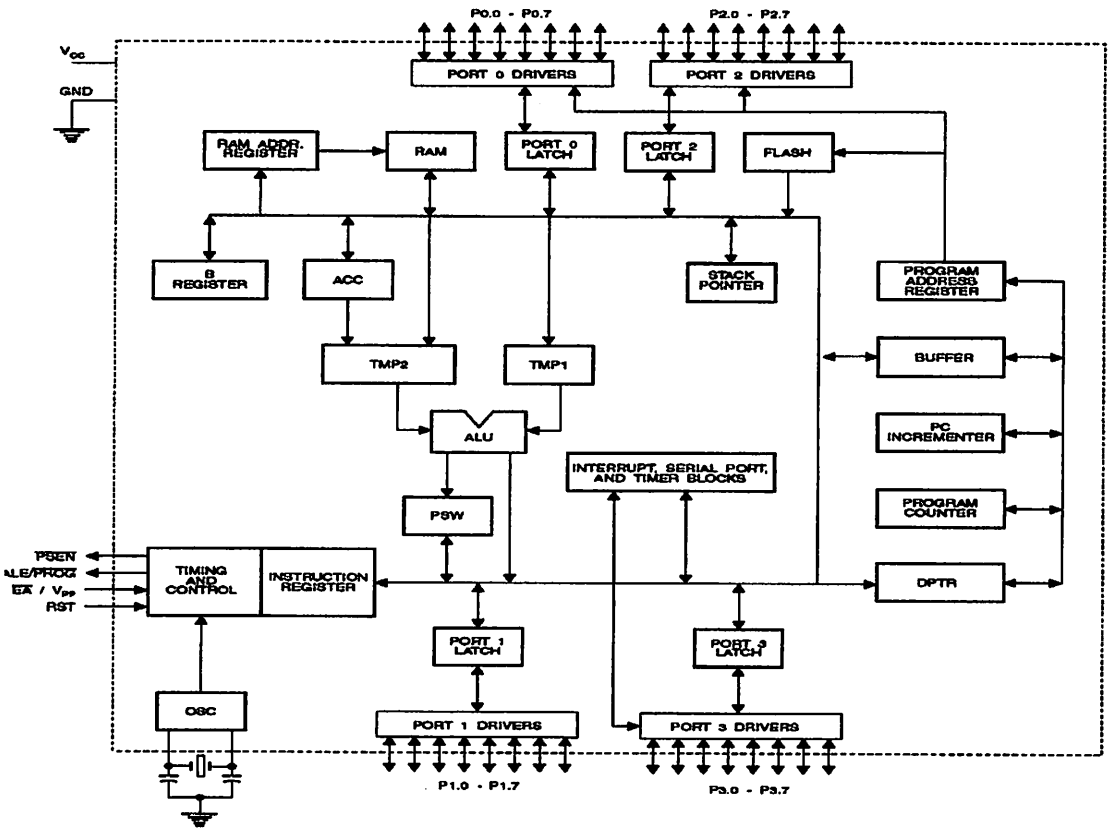
Prosedur pengukuran metode ini adalah sebagai berikut :

1. Manset (Cuff) dibelitkan melingkar pada lengan atas pasien pada titik pertengahan antara siku dan bahu.
2. Manset (Cuff) dikembangkan sehingga tekanan dalam balon karet mencapai suatu harga lebih besar dari tekanan sistolik yang diperkirakan sehingga tidak ada aliran darah ke lengah bawah dan jari.
3. Kemudian operator mengurangi dengan perlahan tekanan di dalam manset dan mengamati nilai pada meteran atau kolom air raksa. Sampai suatu ketika tekanan manset lebih rendah dari tekanan puncak tekanan sistolik pembulu arteri, saat terjadi osilasi pertama nilai pada kolom air raksa disebut sistolik, sedangkan saat amplitudo osilasi kembali pada level pulsa normal lagi, nilai pada kolom air raksa adalah besarnya tekanan diastolik.

2.2 Mikrokontroler AT89S51

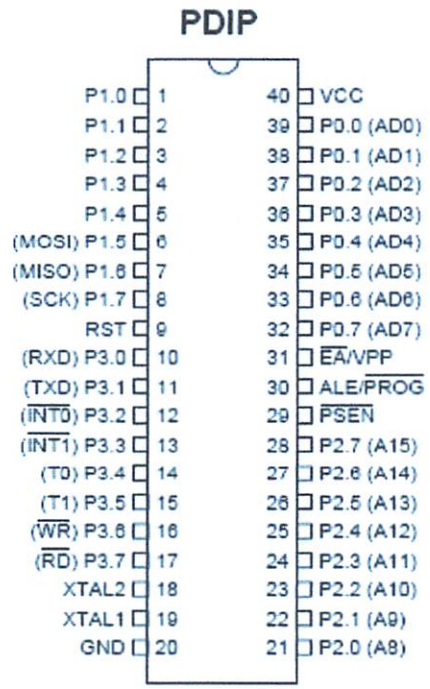
Mikrokontroller terdiri dari mikroprosesor, timer, counter, perangkat I/O, dan internal memory. Pada dasarnya mikrokontroller mempunyai fungsi yang sama dengan mikroprosesor, yaitu untuk mengontrol kerja suatu system. Di dalam mikrokontroller terdapat CPU, ALU, PC, SP, dan register lain yang terdapat pada mikroprosesor, tetapi dengan penambahan perangkat-perangkat lain seperti ROM, RAM, PIO, SIO, Counter, dan rangkaian Clock.

AT89S51 adalah mikrokontroler yang memiliki kapabilitas instruksi dan konfigurasi pin sama dengan mikrokontroler MCS-51.Blok diagram AT89S51 ditunjukkan pada gambar 2.1.



Gambar 2.2 . Blok Diagram AT89S51[3]

Mikrokontroller AT89S51 memiliki 3 pin sebanyak 40 buah seperti ditunjukkan pada gambar 2.3 sebagai berikut :



Gambar 2.3 Susunan Kaki MCS-51 [3]

Pin AT89S51 dibedakan menjadi pin sumber tegangan, pin osilator, pin I/O, dan pin untuk proses interupsi luar.

Fungsi dari pin-pin AT89S51 :

a. Pin 40 adalah pin Vcc, yaitu pin positif sumber tegangan 5 volt DC

b. Pin 20 adalah pin Vss,yaitu pin *grounding* sumber tegangan.

c. Pin 32-39 adalah pin port 0, merupakan port I/O 8 bit *full duplex*. Port ini dapat digunakan sebagai gabungan antara alamat dan data selama ada pengambilan dan penyimpanan data dengan eksternal ROM dan RAM.

d. Pin 1-8 adalah pin port 1, merupakan port I/O 8 bit full duplex. Setiap pin dapat digunakan sebagai masukan atau keluaran tanpa tergantung dari pin yang lain.

e. Pin 21-28 adalah pin port 2, sama seperti port 0. port ini dapat digunakan sebagai address bus tinggi, selama ada penghambilan dan penyimpanan data dengan eksternal ROM dan RAM.

f. Pin 10-17 adalah pin port 3, sama seperti port 1, tetapi port ini memiliki keistimewaan seperti pada table berikut:

Tabel.2.2. Fungsi Alternatif Port 3[3]

Kaki Port	Fungsi Alternatif
P3.0	RXD (masukan penerima data serial)
P3.1	TXD (keluaran pengirim data serial)
P3.2	INT 0 (interupsi eksternal 0)
P3.3	INT 1 (interupsi eksternal 1)
P3.4	T0 (masukan eksternal pewaktu/pencacah 0)
P3.5	T1 (masukan eksternal pewaktu/pencacah 1)
P3.6	WR (strobe penulisan memori data eksternal)
P3.7	RD (strobe pembacaan memori data eksternal)

g. Pin 9 adalah RST/VPD, pin ini berfungsi untuk me-reset system AT89C51. kondisi high (logika '1') dari pin ini selama dua siklus clock (siklus mesin) akan me-reset mikrokontroller yang bersangkutan.

h. Pin 30 adalah pin ALE/PROG, pin ini berfungsi untuk mengunci low address (alamat rendah) pada saat akses memori program selama operasi normal.

i. Pin 29 adalah pin PSEN, Program Strobe Enable merupakan strobe output yang dipergunakan untuk membaca eksternal program memori. PSEN aktif setiap dua siklus mesin.

j. Pin 31 adalah pin EA/VPP, Eksternal Acces Enable secara eksternal harus disambung ke logika '0' jika diinginkan MCS 51 menjadi *enable* untuk mengakses kode mesin dari program memori eksternal. Namun jika EA dihubungkan ke logika '1' maka *device* akan mengambil kode mesin dari *internal* program memori, kecuali jika program *counter* berisi lebih besar dari 0FFFh.

k. Pin 18 adalah pin XTAL1, pin ini merupakan input ke *inverting amplifier* osilator. Pin ini dihubungkan dengan kristal atau sumber osilator dari luar.

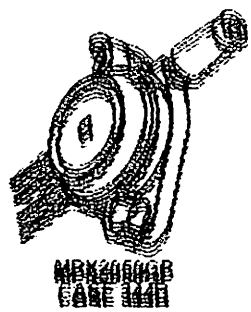
l. Pin 19 adalah pin XTAL 2, pin ini merupakan output dari *inverting amplifier* osilator. Pin ini dihubungkan dengan kristal atau ground jika menggunakan sumber kristal *internal*.

2.3 Tranducer

Tranducer adalah sebuah alat pengubah energi, yang dapat merubah energi dalam bentuk sama atau dalam bentuk yang lain. Transmisi energi ini bisa berupa energi listrik, mekanik, kimia, atau panas. Berdasarkan dengan jenisnya transducer ada dua macam yaitu : Tranducer pasif , Tranducer ini tidak dapat menghasilkan tegangan sendiri tetapi dapat menghasilkan perubahan nilai resistansi, kapasitansi, atau induktansi apabila mengalami perubahan kondisi sekeliling. Jika kondisi berubah pada lingkungan sekitar maka nilai resistansi akan berubah yang dapat mempengaruhi perubahan tegangan atau kuat aru yang dihasilkan tranducer., 2. Tranducer Aktif ,Tranducer ini dapat menghasilkan energi listrik, sehingga tidak memerlukan catu daya eksternal.

1.3.1 Tranducer Tekanan

Tranducer tekanan adalah suatu alat yang digunakan untuk mengubah energi tekanan menjadi tegangan. Perubahan dari nilai tahanan dari sebuah konduktor yang disebabkan berubahnya dimensi dari material. Berikut ini merupakan salah satu bentuk fisik dari tranducer tekanan.



Gambar 2.4 Bentuk fisik Tranducer Tekanan. [4]

Tranducer diatas merupakan tranducer tekanan dengan 4 buah kaki yang memang support untuk pengukuran tekanan darah.

2.4 Kondensor Mic

Kondensor merupakan suatu tranducer yang dapat merubah gelombang suara menjadi sinyal listrik. Mickropohon condenser dapat mengubah gelombang suara kedalam besaran kapasitansi, sehingga bila ada gelombang suara masuk ke dalam mikrophone maka sekat rongga di dalamnya menjadi bergetar menyebabkan perubahan kapasitansi , perubahan nilai kapasitansi itu meyebabkan perubahan besaran listrik pada suatu frekuensi yang sebanding gelombang suara itu. yaitu apabila nilai kapasitansi bertambah maka akan terjadi besaran arus dan bila nilai kapasitansi menurun besaran arus semakin mengecil.

Gambar 2.5 Kondenser mic [9]

Microphone kondenser mempunyai tangkapan frekuensi yang lebar, menerima getaran suara hampir dari semua arah, kepekaan suara sangat sensitif yaitu ± 46 dBV, respon frekuensi sangat baik antara 20 Hz – 18 KHz, impedansi keluaran 15 Ω dan tidak dipengaruhi oleh panjang kabel yang dipakai.

2.5 Penguat (Op-Amp)

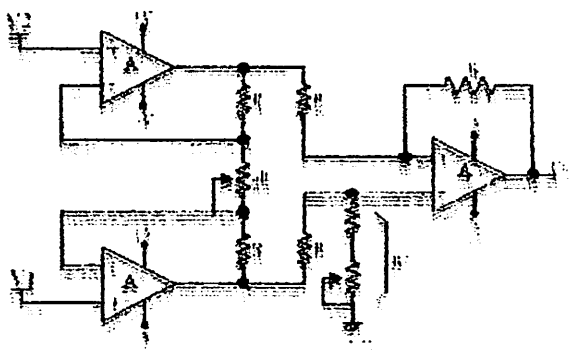
Op – Amp merupakan suatu peralatan yang digunakan untuk menguatkan sinyal, atau energi yang berguna dalam pembentukan sumber arus atau tegangan.

Op-Amp mempunyai karakteristik yang iedeal hanya mempunyai dua sifat yang diperlukan dalam analisa rangkaian yaitu :

- Arus yang masuk ke kedua kutub masukannya sama dengan 0
- Tegangan diantara dua kutub masukkannya sama dengan 0

Pada tugas akhir ini Op-Amp digunakan sebagai penguat instrumentasi yang mana terdiri dari beberapa Op-Amp.

Jika tegangan masukan dari setiap Op-Amp besarnya 0 v, maka tegangan I titik 1 dan 2 sama dengan V1 dan V2. bila v1 lebih besar dari v2 maka besar tegangan antara titik 1 dan 2 adalah V1 – V2. arus yang melalui hambatan aR yaitu : $I = \frac{V1-V2}{aR}$



Gambar. 2.6 Penguat Instrumentasi. [5]

Besar tegangan keluaran A_2 yaitu : $V_{A2} = V_2 - \frac{V_1 - V_2}{a}$

Besar tegangan keluaran A_1 yaitu : $V_{A1} = V_1 + \frac{V_1 - V_2}{a}$

Besar tegangan keluaran A_3 yaitu : $V_0 = (V_1 - V_2)1 + \frac{2}{a}$

Besar penguat dari rangkaian penguat instrumentasi yaitu : $\frac{V_0}{(V_1 - V_2)} = \left(1 + \frac{2}{a}\right)$

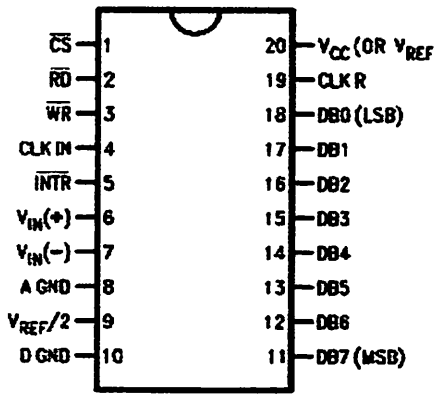
Dari persamaan diatas di dapat nilai a yaitu : $a = \frac{2}{\left(\frac{V_0}{(V_1 - V)_2}\right) - 1}$

2.6 ADC (Analog Digital Converter)

Ada bermacam-macam pengubah analog ke digital, namun yang paling banyak digunakan adalah ADC jenis pencacah berturut-turut *(Succesive Aproximation Counter)* sebab memberikan hasil yang paling baik dengan biaya yang relatif lebih murah.

Rangkaian pembanding (comparator) membentuk dasar dari semua pengubah A/D. rangkaian ini membandingkan suatu tegangan yang tidak diketahui terhadap sebuah tegangan referensi tersebut yang lebih besar. Pada dasarnya sebuah rangkaian pembanding adalah penguatan selisih tingkat ganda berpenguatan tinggi, dimana keadaan keluaran ditentukan oleh polaritas relatif dari kedua sinyal masukan.

Konverter A/d tersedia sebagai rangkaian terpadu (IC) dengan resolusi 8 bit sampai 16 bit. Konveter ini menggunakan aproksimasi berturut-turut untuk mengkonversi masukan analog menjadi data digital 8 bit yang ekivalen. Keluaran digital akan muncul bila CS dan RD dalam keadaan rendah mengalami reset. Pin WR digunakan untukmemulai suatu konversi WR kembali pada keadaan tinggi.



Gambar 2.6 Konfigurasi Pin-pin ADC 080X [6]

Beberapa karakter dan fungsi pin yang perlu diketahui adalah :

1. Dua input analog, yakni Vin (+) dan Vin (-) yang merupakan input diferensial, artinya untuk membedakan antara input analog (Vin) dengan tegangan yang digunakan (analog Vin = Vin (+) – Vin (-)). Apabila digunakan untukpengukuran tunggal, maka yang digunakan adalah input Vin (+) dan Vin (-) harus dihubungakan ke analog ground. Selama beroperasi normal converter ini menggunakan Vcc = = 5V sebagai tegangan referesninya, dan input analognya mempunyai variasi range antara 0-5 volt.
2. dapat mengkonversi tegangan input analog menjadi 8 bit output digital. Output digitalnya memiliki buffer tristate sehingga dapat dengan mudah dihubungkan dengan bus data dari prosessor.
3. Mempunyai fasilitas internal clock dengan frekuensi 1(1.1 RC) dengan R dan C merupakan komponen luar yang harus ditambahkan. Frekuensi

clock tipikalnya adalah 606 KHz yang menggunakan R =10 Kohm dan C = 150 pF, apabila menggunakan eksternal clock maka pin CLK IN harus digunakan.

4. Dengan menggunakan frekuensi clock 606 KHz lama waktu konversinya adalah 100 ms.
5. Fasilitas lainnya adalah sambungan ground untuk tegangan digital maupun analognya. Pin 8 digunakan sebagai analog ground yang dihubungkan pada titik referensi rangkain analognya (tegangan input analog). Pin 10 sebagai digital ground digital dari sistem.

Pemakaian ADC 0804 khusus digunakan untuk memudahkan berhubungan dengan data bus mikroprosessor. ADC ini digunakan sebagai fungsi dasar dari mikroporsesor dan fungsi-fungsi darsar dari system I/O adalah sebagai berikut

1. CS (Chip Select)

   Input ini mempunyai sifat aktif low pada saat RD dan WR diguakan. Dengan CS sama dengan High digital berada ditingkat Hi-Z, dna pada kondisi tidakmengkonversi.

2. RD (Output Enable)

   Digunakan untuk mengenable buffer output digital. Dengan CS=RD=low pin output digital memiliki level logika akhir dari ADC.

3. WR (Start Conversi)

   Digunakan untuk memulai konversi denganmemberi pulsa input start low sesaat.

4. INTR (end Conversion)

   Siyal output sesaat akan menuju high setelah konversi diberikan dan akan low setelah selesai konversi.

5. Vref/2

   Adalah input opsional yang digunakan untukmenghasilkan tegangan referensi dan dapat merubah range input analognya. Pada saat input belum disambungkan input masih 2.5 V (Vcc/2) dengan menghubugkan tegangan luar apda port maka internal referensiakan berubah yang membagi tegangan tersebut demikian halnya terhadap range input analognya.

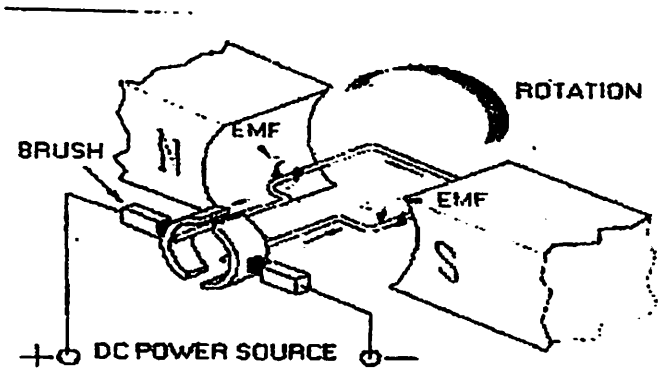
6. CLK-IN

   Digunakan untuk eksternal clock input atau dengan menghubungkan kapasitor untuk penggunakan internal clock

7. CLK-R

   Sebuah resistor harus dihubungan pada pin ini untuk menggunakan internal clock.

2.7 Motor DC



Gambar 2.7 Kontruksi Motor DC[5]

Motor DC merupakan motor yang dikendalikan oleh arus DC, pada saat terminal motor diberi tegangan DC, maka arus elektron akan menglair melalui konduktor dari terminal negatif menuju ke terminal positif. Karena konduktor berada diantara medan magnet, maka akan timbul medan magnet. Arah garis gaya medan magnet yang dihasilkan oleh magnet permanen adalah dari kutub utara menujuke selatan. Sementara pada konduktor yang dekat dengan kutub selatan, arah garis gaya magnet disisi sebelah bawah searah dengan garis gaya magnet permanen sedangkan di sisi sebelah atas arah garis gaya magnet berlawanaan arah dengan garis gaya magnet permanen. Ini menyebabkan medan magnet disisi sebelah bahwa lebih rapat daripada sisi sebelah atas. Dengan demikian konduktor akan terdorong ke arah atas, sementara pada konduktor yang dekat dengan kutub utara, arah garis gaya magnet disisi sebelah atas searah dengan garis gaya magnet permanen sedangan disisisebelah bawah arah garis gaya magnet berlawanan arah dengan garis gaya magnet permanen. Ini menyebabkan medan magnet disisi sebelah atas lebih rapat daripada sisi sebelah bawah. Dengan demikian konduktor

akan terdorong ke arah bawah. Pada akhirnya konduktor akan membentuk gerakan berputar berlawanan dengan jarum jam

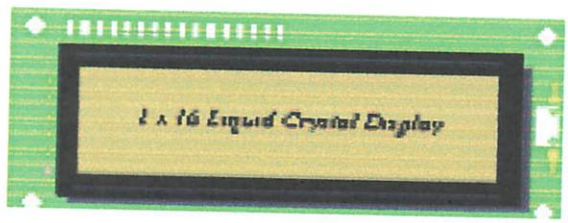
2.8 Push Button (Saklar Tekan)

Saklar tekan dioperasikan dengan cara menekan sebuah tombol. Terdapat dua jenis saklar semcam ini. Kebanyakan diantaranya temasuk kedalam jenis push to make (tekan untuk menyambungkan). Denganmenekan tombol, kontak-kontak akan saling bersentuhan dan saklar menutup. Jenis lainnya adalah push to break (tekan untuk memutuskan). Kontak-kontaknya adalah normal tertutup, namun akan dipaksana membuka ketika tombol ditekan.

Masing-masing jenis saklar yangdisebutkan diatas dapat bekerja untuk memutuskan atau menghubungkan sambungan selama sekejap. Tombol tersebut akan menghubungkan atau memutuskan selama tombol tersebut ditekan.

2.9 LCD (Liquid CrystalDisplay)

LCD yaitu suatu bentuk cristal cair yang akan ber'emulsi' jika dikenakan taegangan kepadanya. Bagian tampilan ini berupa dot matrik 2 x 16 sehingga jenis yangmampu ditampilkan akan lebih baik resolusinya jika dibandingkan dengan 7 segment. Liquid adalah modul tampilan yang mempunyai konsumsi daya yang relatif rendah danterdapat sebual modul cotroler CMOS di dalamnya. Controler tersebut sebagai pembangkit dari karakter ROM/RAM dan display data RAM. Keunggulan dari LCD adalah bentuknya yang kecil, sehingga sangat praktis apabila digunakan.



Gambar 2.8 tampilan LCD 2 x 16 [7]

Pada LCD ini terdapat 8 bit data (bidirectional bus) dan 3 buah sinyal kontrol yaitu RS, R.W, dan E.

Ketiga sinyal kontrol tersebut mempunyai fungsi sebgai berikut :

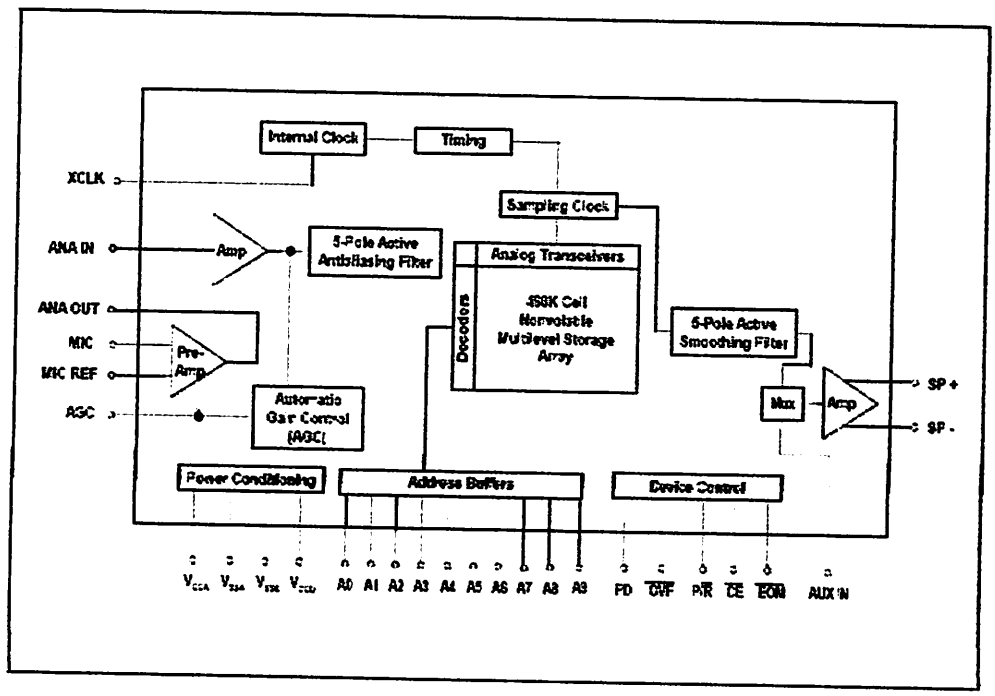
1. RS. Digunakan untuk memilih register yaitu register IR (Instruction regiter) atau DR (data register)
2. R/W digunakan utnuk memilih fungsi yaitu kita membaca atau menulis pada kedua register IR dan DR
3. E berguna untuk memberikan sinyal pada bahwa data akan ditulis atau dibaca ke register.

Dengan adanya ketiga sinyal kontrol tersebut hubungan antara hardware dan software sangatlah erat, banyak sekali cara menggunakan memprogram LCD in idikarenakan penyusunan hardware yang berbeda. Tetapi kita melihat lagi pada hasil keluaran mikrokontroler atau alat yang menggunakan LCD pasti mempunyai kesamaan yaitu beetuk sinyal kontrol yang sama pada saat menulis keregister ataupun membacanya.

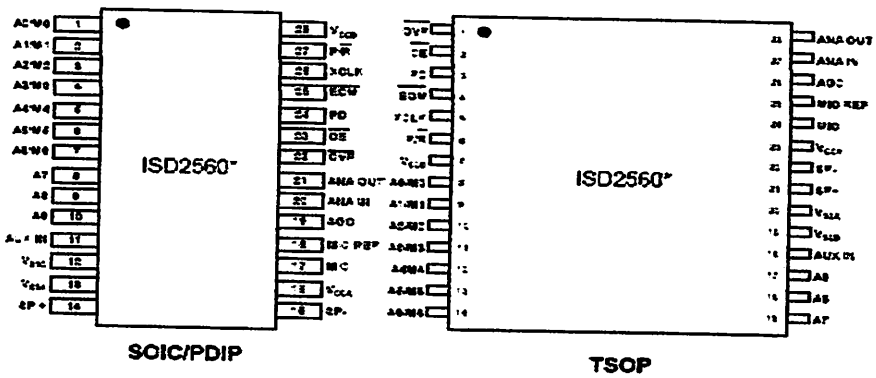
2.10 Information Store Device 2560

Alat ini merupakan seri chip perekan yang menyediakan kualitas tinggi. Chip tunggal record untuk 60 detik. Perangkat CMOS ini dilengkapi internal oscilator, preamplifier microphone, kontrol penguatan otomatis, filter yang jernih, penguat speaker dan penyimpan multilevel dengan kapasitan yang besar.

Sebagai tambahan ISD 2560 dapat digabungkan dengan mikrokontrolerh yang menyediakan pembuat pesan yang banyak dan dapat dialamatkan



Gambar. 2.9 block Diagram ISD 2500series[8]



Gambar 2.10 Pin Konfigurasi ISD2560 [8]

Keterangan Pin ISD 2560 adalah sebagai berikut :

1. Micropon Input (MIC)

   Sinyal dari microphone diteruskan ke preamplifier dimana sinyal tersebut dikontrol oleh Automatic Gain Control (AGC) dalam batas -15 s/d 24 dB. Batas frekuensi yang diizinkan adalah frekuensi rendah cut-off.

2. Microphone Reference Input (MIC REF)

   Dihubungkan seri dengan kapasitor dan digroundkan, jika tidak digunakan maka pin ini dibiarkantidak terhubung.

3. Analog Output (ANA OUT)

   Pin ini menyediakan preamplifier output untuk digunakan oleh pengguna. Penguatan tegangan ditentukan oleh level tegangan pada AGC.

4. Analog Input (ANA IN)

   Sinyal pada pin ini diteruskan pada chip internal untu proses perekaman. Jika menggunakan input lain selain microphone maka pin ANA IN ini dipasang kopling kapasitor. Dan jika menggunakan microphone input (MIC) maka ANA IN harus dihubungkan seri melalui kapasitor terhadap ANA OUT.

5. Automatic Gain Control Input (AGC)

   AGC secara terusmenerus mengatur penguatan pada preamplifier untuk mengimbangi lebar batas level microphone input. AGC mengizinkan hingga batas maksimal suatu untuk direkam dengan perubahan yang minimum.

6. Speaker Output (SP +/SP-)

   Semua perangkat pada seri ISD2500 memmiliki dirver internal differensial speaker dengan kemampuan 50 miiliwatt dengan hambatan 16 ohm.

7. Power Down (PD)

   Pada saat tidak diperlukan proses perekaman dan play, PD harus diset tinggi (=1)

8. Chip Enable Input (CE)

   Pn CE diset rendah (=0) untuk memperolehkan seluruhoperasi rekam/play. Input pengalamatan dan input rekam/play hanya dapat dikontrol oleh CE dalam konsisi sinyal turun (Falling edge).

9. Playback/record Input (P/R)

   P/R dikontrol oleh siyak turun (falling edge) oleh pin CE. Jika P/R diset pada lebel yang rendah maka saat itu adalah mode rekam/record.

10. Eksternal clock input (XCLK)

Perangkat ISD2500 dikonfigurasikan pada titik frekuensi clock dengan internal sampling hingga 1 % dari spesifikasi. Berikut spesifikasi dari ISD 2560 sample rate = 8.0 Khz required Clock 1024 Khz. Pada pembuatan alat ini XCLK tidak digunakan maka input pin ini harus dihubungkan terhadap ground.

11. End Of Message/Run Output (EOM)

Dalam proses perekaman secara otomatis non volatile storage pada perangkat ISD2500 akan menandakan akhir dati tiap pesan/mesaage. Ini sebagia tanda saat pesan telah selesai dan melampaui maka pulsa output EOM akan rendah dalam waktu Toem yaitu 18.75ms pada akhir tipa pesan.

12. Overflow Output (OVF)

Sinyal pulsa ini akan rendah pada saat kahir dari kapasitas memory, yang mengindikasikan bahwa memori telah penuh terisi dan pesan mengalami overflow/kelebihan. Output OVF akan mengikuti input CE hingga pulas PD melakukan reset pada perangkat.

13. Auxiliary Input (AUX IN)

Pin ini dimultiplexkan keluat melalui pin amplifier output dan speaker output ketika CE diset tinggi danplay telah selesai dilakukan,atau jika pada perangkat inimengalami overflow. Pini ini digunakan jika terdapat input tambahan dari perangkat lain.

14. Voltage Input (Vcca, Vccd)

    Untuk meminimalkan derau, rangkaian analog dan digital pada ISD 2560 ini harus memisahkan suber tegangannya danjika perlu ditambahkan kopel.

15. Ground Input (Vssa, Vssd)

    Perangkat ISD2560 menyediakan perangkat secara terpisah antara analog dan perangkat ground. Pin ini dapat juga dihubungkan bersama dan dihubungkan pada power supply ground.

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

Perencanan suatu alat sangat diperlukan untuk mendapatkan suatu sistem yang stabil dan ideal dalam proses pembuatan alat. Dalam bab ini akan dijelaskan tentang perencanaan alat-alat yang digunakan dalam pembuatan tensi darah digital berbasis Mikrokontroler AT89S51.

3.1 Spesifikasi Alat

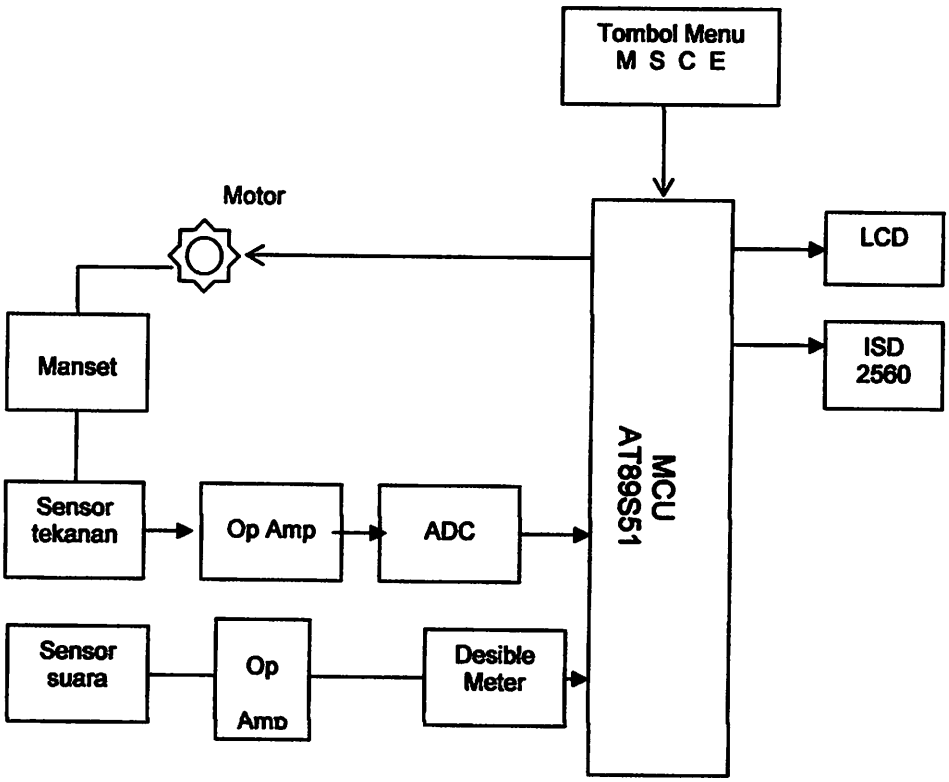
Alat yang akan dibuat ini memiliki spesifikasi sebagai berikut :

1) Komponen pengolah utama adalah Mikrokontroler AT89S51
2) Sensor tekanan yang digunakan adalah MPX2050GP yang mana sensor ini memang pengaplikasiannya diantaranya untuk pengukuran tekanan darah.
3) Sensor suara yang digunakan adalah kondensor mic
4) Tampilan alat yang digunakan adalah LCD 2 x 16 dan ISD 2560
5) Range tekanan darah bervariasi antara 0-200 mmHg

3.2 Perencanaan Hardware.

3.2.1 Diagram Blok

Untuk membuat alat tensi darah digital ini diperlukan diagram blok yang akan digunakan sebagai panduan untuk menjalankan dan pembuatan alat, adapun diagram blok dapat dilihat pada gambar berikut ini :



Gambar 3.1 Diagram block perencanaan alat

Dari diagram blok diatas, dapat dijelaskan bahwa secara garis besar alat pengukur tekanan darah digital ini berbasis mikronkontroler AT89S51 memiliki bagian-bagian sebagai berikut :

1) Tombol Menu

Digunakan untuk mengaktifkan peralatan pengukuran tekananan darah. Tombol menu menggunakan push button yang terdiri dari 4 buah yaitu M = Menu , S = Selec C = Cancel, dan E = Enter.

2) Sensor Tekanan

Sensor tekanan yang digunakan adalah MPX2050GP yang mana sensor ini digunakan untuk mendeteksi pengukuran tekanan darah. Prinsip kerja

dari sensor MPX2050GP ini adalah merubah tekanan yang ada dimanset menjadi tegangan.

3) Sensor Suara

Sensor suara yang digunakan adalah kondensor mic yang akan mendeteksi adanya detak jantung untuk menentukan tekanan sistole dan diastole.

4) Manset (Hand Cuff)

Manset merupakan alat yang diletakkan ditangan yang mana manset ini akan menggembung bila dialiri udara dan bisa menghentikan sementara aliran darah yang ada di lengan.

5) Motor

Motor digunakan untuk memompa udara kedalam manset (Hand Cuff)

6) Op Amp (Operational Amplifier)

Merupakan penguat tegangan yang digunakan untuk memperkuat outputan sensor-sensor yang digunakan.

7) ADC (Analog To Digital Converter)

ADC digunakan untuk merubah data analog menjadi data digital sehingga dapat dibaca oleh mikrokontroler.

8) Desible Meter

Seperti halnya Band pass Desible mendata frekuensi yang masuk

9) MCU

Mikrokontroler yang digunakan adalah AT89S51 digunakan sebagai pusat kontrol utama yang akan memproses dan mengola semua data yang masuk padanya.

10) LCD (Liquid Cristal Display)

LCD ini digunakan untuk menampilkan hasil pengukuran berupa tekanan sistole dan diastole dalam bentuk tulisan.

11) ISD (Information Store Device) 2560

ISD merupakan alat untuk menampilan hasil pengukuran tapi dalam bentuk suara.

3.2.2 Sensor Tekanan

Sensor tekanan yang digunakan adalah MPX2050GP yang mana sensor ini digunakan untuk merubah besaran tekanan menjadi besaran listrik berupa tegangan. Besar daya yang diperlukan adalah max 16 Volt, dan sensor ini dapat mengukur tekanan sampai dengan 7,25 PSI atau sebesar 375 mmHg.

Pada umumnya satuan tekanan yang dipakai adalah Kpa atau PSI, dan untuk mendapatkan nilai satuan dalam mmHg maka harus mengkonversikan dari PSI ke mmHg.

Jika I Kpa = 0.145 Psi

Jika I PSI = 51,727 mmHg , maka 1 mmHg adalah

$$= \frac{1\ mmHg}{51{,}73\ mmHg} x\ 1\ psi = 0{,}01933 PSI$$

Maka untuk memperoleh besarnya tekanan maksimal 200 mmHg adalah

Besar tekanan dalam satuan PSI $= \frac{200\ mmHg}{51{,}73\ mmHg} x\ 1\ psi = 3{,}866 PSI$ (26 Kpa)

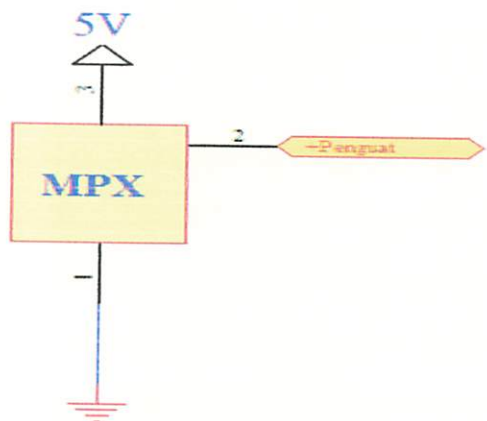
Dari data sheet sensor MPX2050GP mampu mengukur tekanan sampai dengan 7,25 PSI atau 375,02 mmHg, mempunyai range tegangan antara 0-40 mV

Jadi , Pertambahan tegangan $= \frac{40\ mV}{375{,}02\ mmHg} = 0{,}10666\ mV / mmHg$

Jadi setiap kenaikan 1 mmHg maka teganan akan bertambah sebesar 0,1066 mV. Jadi teganan yang dibutuhkan untuk mengukur tekanan sebesar 200 mmHg atau 4,834 PSI adalah sebesar

Tegangan yang dibutuhkan = 0,10666 mV x 200 mmHg

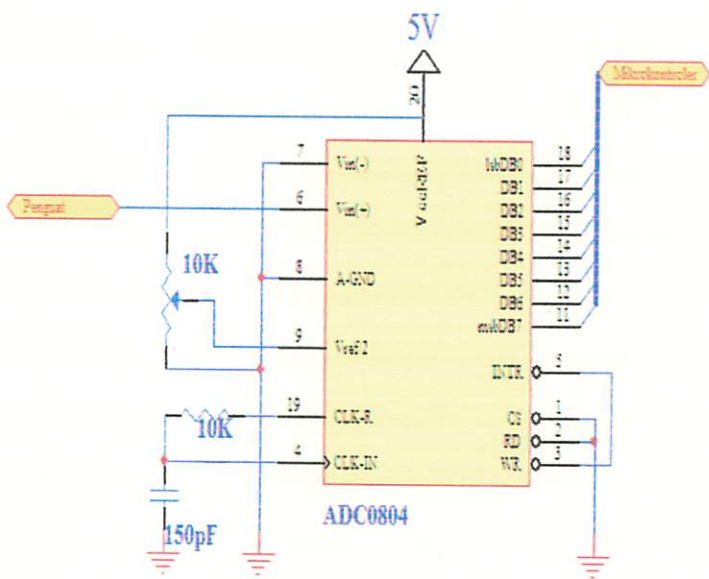
= 21,33 mV



Gambar 3.2 Scematic MPX2050GP

3.2.3 ADC (Analog Digital Converter)

Jenis ADC yang banyak dgunakan dan banyak tersedia di pasar adalah jenis ADC 0804, 0808, dan 0809, dan masih banyak lagi jenis yang lain. Chip ini dibuat dengan teknologi CMOS yang mempunyai kemampuan melakukan konversi sebanyak 8 buah chanel input analog serta multiplexing yaitu untuk ADC 0808 dan ADC 0809. Adapun data keluaran digital yang dihasilkan adalah 8 bit. Rangkaian ADC ini dilengkapi dengan rangkaian tegangan referensi. Fungsi rangkaian tegangan referensi ini adalah untuk mendapatkan resoulusi 1 bit yang diinginkan. Pada laporan ini jenis ADC yang digunakan adalah ADC 0804 yang ditunjukkan pada gambar berikut :



Gambar 3.3 Gambar Scematic Rangkaian ADC 0804

Agar dapat diproses oleh mikrokontroler, maka sinyal yang masuk dari sensor yang merupakan sinyal analog harus dirubah menjadi sinyal digital, untuk itu digunakan rangkaian ADC 0804. Rangkaian ADC ini

punya 8 bit keluaran (DB0 – DB7) yang dihubungkan kemasukkan kontroler. Sedangkan masukkan pada ADC ini dibatasi antara 0 sampai 5 Volt. Pada pin CS dan RD diberi logika rendah karena pin CS akan mengaktifkan ADC 0804, sedangkan RD berfungsi agar ADC membaca secara terus menerus data dari rangkaian penguat. Untuk pin INTR dihubungkan juga ke pin WR maksudnya ketika adanya data konversi maka pin INTR akan aktif, dan aktifnya pin ini akan mengaktifkan pin WR yang akan melakukan penulisan data pada mikrokontroler.

ADC 0804 membutukan Vref/2 sebesar setengah dari masukan analognya. Karena masukan tegangan analog yang direncanakan maksimu 5 volt maka dibutuhkan tegangan referensi 2,5 volt. Tegangan ini diperloeh dari pembagi tegangan, sehingga digunakanlah resistor 1 K dan didapatkan

$$Vref = \frac{1K}{1k+1k} x5V = 2{,}5V$$

Kerja ADC akan optimal bila frekuensi clock yang digunakan sebesar 640 Khz (datasheet), maka dengan menentukan R = 10 KΩ maka dapat diperoleh nilai C dengan rumus $f = \frac{1}{1{,}1RC}$, sehingga didapatkan :

$C = \frac{1}{1{,}1x640x10} = 147.10^{-12}$,pada perancangan alat ini digunakan C=150 pF.

ADC 0804 mempunyai 8 bit keluaran. Dari bit keluaran tersebut diketahui persen resolusinya dengan persamaan berikut :

$$resolusi = \frac{Vref}{2^n - 1} \text{ maka } resolusi = \frac{5}{2^8 - 1} = 19{,}6\ mV$$

Berdasarkan datasheet tegangan masukkan maksimum untuk ADC 0804 adalah 5 Volt. Sehingga

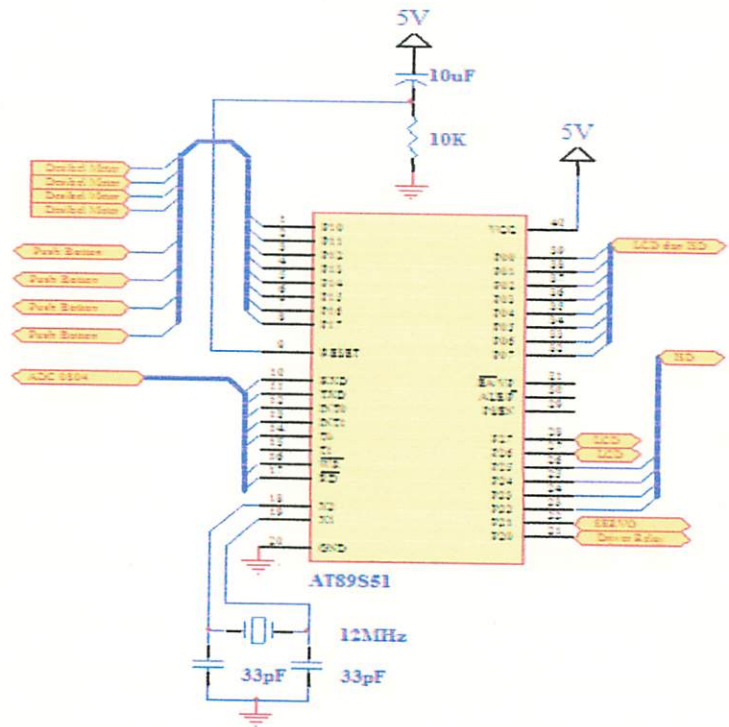
$$OutputADC = \frac{Vin}{\text{Re}solusi}$$

$$Output = \frac{5}{19{,}6\ mV}$$

$$output = 254(FE \quad h)$$

3.2.4 Mikrokontroler AT89S51

Mikrokontroler didalam perencanaan ini merupakan komponen utama, karena komponen inilah yang mengatur keseluruhan sistem agar dapat bekerja dengan baik dan optimal. Perancangan mikronkontroler AT89S51 dapat dilihat pada gambar dibawah ini.



Gambar. 3.4 Rangkaian Mikrokontroler AT89S51

Pada gambar biatas komponen utamanya adalah mikrokontroler AT89S51 yang compatible dengan keluarga MCS-51. komponen ini merupakan sebuah chip tunggal sebagai pengolah dara dan pengontrol alat.

Untuk mengaktifkan mikrokontroler diperlukan power + 5 Volt pada pin 40 dan ground pada pin 30. disamping itu diperlukan juga pengaktifa osilator yang terdapat dalam rangkaian mikrokontroler. Untuk mengaktifkan osilator tersebut dalam perancanganini digunakan kristal 12 Mhz dan kapaistor 33 pF. Digunakan kristal 12 Mhz untuk memperoleh kecepatan pelaksanaan instruksi persiklus sebesar 1 μ detik (1/12 Mhz x 12 siklus periode).

Frekuensi clock yang dihasilkan oleh rangkaian osilator menyebabkan terjadinya interval waktu yang kecil di dalam mikrokontroler. Interval waktu inilah yang digunakan untuk melaksanakan instruksi sederhana, ataupun instruksi-instruksi kompleks lainnya. Rangkaian reset berfungsi untuk mereset mikrokontroler pada saat power on.

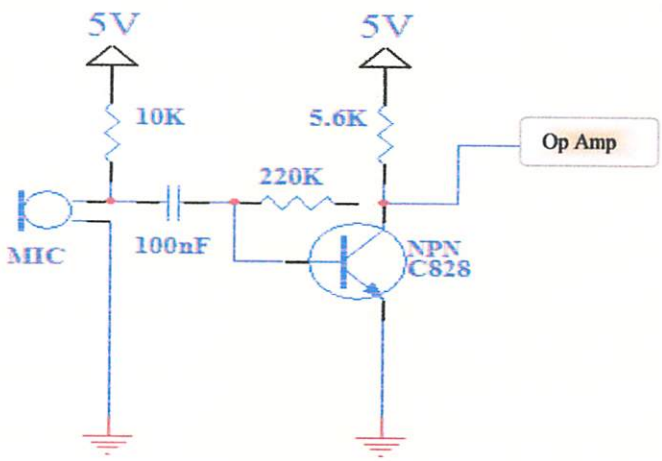
Adapun port-port yang digunakan pada rangkaian mikrokontroler AT89S51 ini adalah sebagai berikut :

- Port 0 (P0.0 sampai P0.7) digunakan sebagai port keluaran untuk menampilkan tampilan LCD dan ISD.
- Port 1 (P1.0 sampai P1.4) digunakan sebagai port masukan untuk menerima masukan data dari Desible Meter.

- Port 1 (P1.5 sampai P1.7) digunakan sebagai port masukan untuk menerima masukan data dari Push Button.
- Port 2.0 digunakan sebagai port masukan dari penekanan tombol Relay
- Port 2.1 digunakan sebagai masukan motor servo.
- Port.3.0 digunakan sebagai masukan dari outputan ADC.

3.2.5 Sensor Suara

Rangkaian sensor suara ini dipergunakan untuk mendeteksi ada tidaknya suara detak jantung. Perancangan dari sensor suara dapat dilihat pada gambar dibawah ini :



Gambar. 3.5 Rangkaian sensor suara

Komponen utama pada rangkaian sensor suara adalah kondensor mic. Kondensor ini yang nantinya akan menangkap ada tidaknya suara dari detak jantung yang diukur. Karena keluaran dari kondensor sangat kecil sekali sehingga diperlukan rangkaiaan penguat yang dibentuk dari transistor

supaya keluarannya dapat diterima dan dideteksi oleh mikrokontroler. dan diketahui

Vcc : 5 volt, Vbe = 0,7 V, Hfe = 96 maka,

$$Ic = \frac{Vcc}{Rc} = \frac{5}{5{,}6.10^{3}} = 0{,}9mA$$

$$Ib = \frac{Ic}{Hfe} = \frac{0{,}9.10^{-3}}{96} = 9{,}37\mu A$$

$$Rb = \frac{Vb - Vbe}{Ib} = \frac{5 - 0{,}7}{9{,}37.10^{-6}} = \frac{4{,}3}{9{,}37.10^{-6}} = 458K\Omega$$

$$Vout = \frac{Rf}{rb} x\, Vin$$

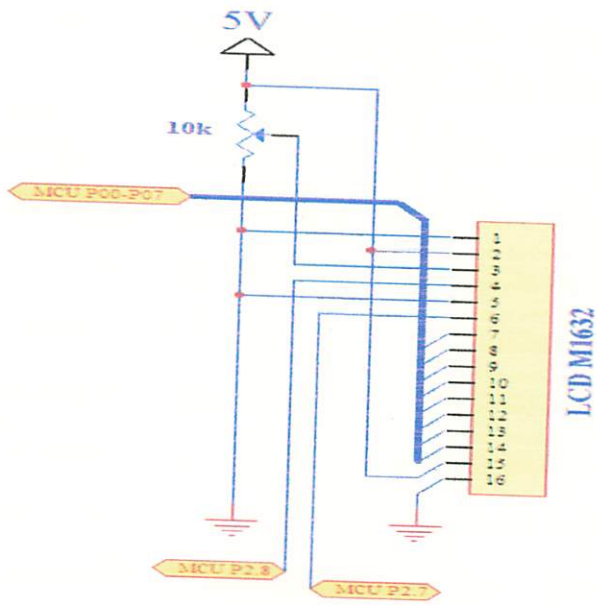
$$Vout = \frac{220}{458} x5 = \frac{1100}{458} = 2{,}40Volt$$

Keluaran tegangan yang telah dikuatkan tersebut telah mampu untuk dideteksi oleh mikrokontroler, sehingga mikrokontroler dapat mengolah data dan melanjutkan perintah lainnya.

3.2.6 LCD (liquid Cristal Display)

Sebagai penampil data dalam perancangan ini digunakan tampilan berupa LCD, yang mana LCD ini memudahkan untuk melihat secara visual terhadap tampilan dari nilai tekanan sistolik dan diastolik dari tekanan darah yang diukur. Pada perancangan alat ini dipergunakan LCD dot matrik M1632 2 x 16 karakter.

Liquid Cristal Dispai ini mempunyai konsumsi daya yang relative rendah dan terdapat sebuah controler CMOS di dalamya. Controler tersebut sebagai pembangkit dari katakter ROM/RAM dan display data RAM. Semua fungsi tampilan dikontrol oleh suatu instruksi yang dilakukan oleh sofware pada mikrokontroler. Semua pin data (DO sampai D7) dan pin kontrol EN dan RS dihubungkan dengan mikrokontroler. Pada pin 2 dihubungkan ke VCC, pin 1dan pin5 dihubungkan ke ground. Pin R/W (pin 5) diberi logika 0 sehingga LCD bekerja dalam mode tulis. Perancangan rangkaian LCD dapat dilihat pada gambar dibawah ini :

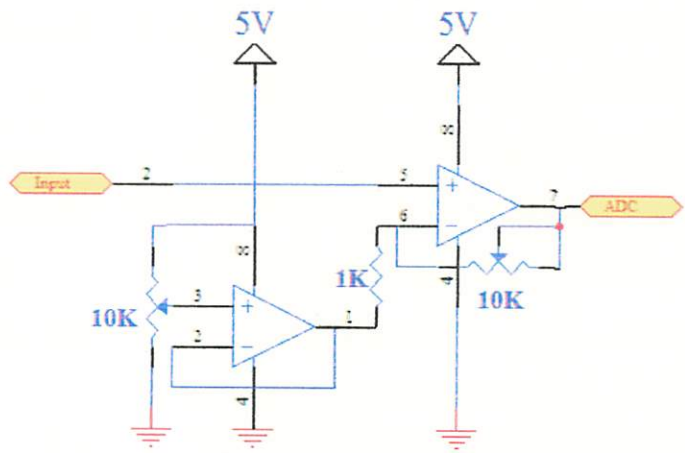


Gambar 3.6 Rangkain LCD

Vr pada pin 3 (VEE) digunakan untuk mengatur contras dari karakter.

3.2.7 Rangkaian Penguat

Fungsi dari rangkaian penguat adalah meguatkan besar tegangan yang dihasilkan oleh sensor tekanan sehingga dapat diolah oleh pengolah ADC 0804.



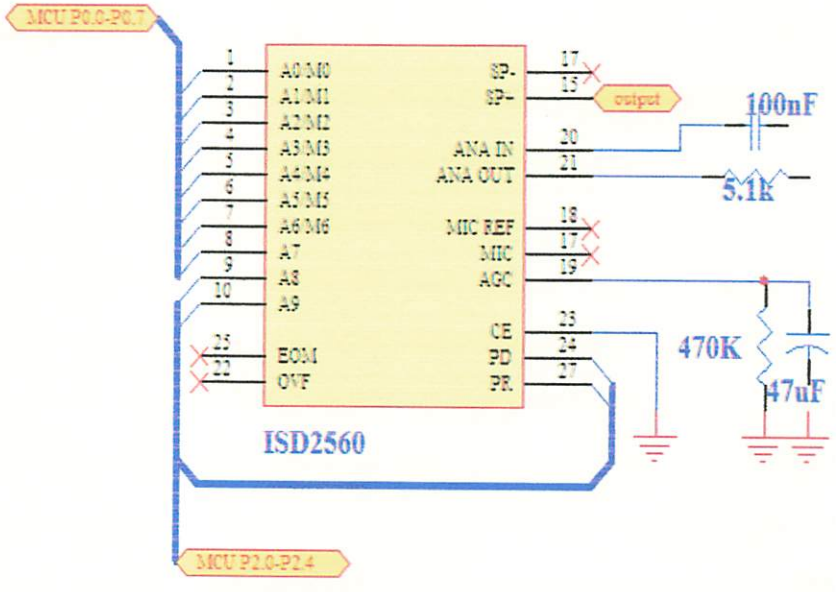
Gambar 3.7 Scematic rangkaian penguat

Dua IC LM358 dan R serta Vr (variabel Resistor) membentuk rangkaian penguat yang dapat menghasilkan penguat yang dapat diubah-ubah. Vo yang diinginkan untuk mencatu input dari ADC adalah 5 Volt sedangkan sensor tekanan untuk pengukuran 200 mmHG adalah 21,33 mV, maka dapat dicari nilai penguatan yaitu :

$$\text{Penguatan} = \frac{Vo}{(V_1 - V_2)} = \frac{5000}{21{,}33} = 234{,}4$$

3.2.8 Perancangan Rangkaian ISD 2560

Rangkaian ISD 2560 digunakan untuk memutar suara tekanan darah yang dihasilkan, yang mana berdasarkan data sheet ISD 2560 ini mampu merekam suara dengan waktu maksimal perekaman 60 detik. Adapun gambar rangkaian adalah sebagai berikut :

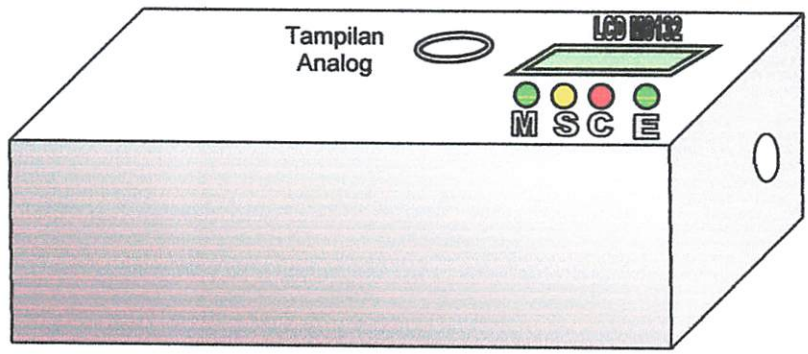


Gambar 3.8 rangkaian Scematik ISD 2560

Pada rangkaian diatas ouput dihubungkan dengan keluaran berupa speaker 8 ohm untuk mengeluarkan hasil pengukuran tekanan darah distole dan diastole.

3.3 Perencanaan Mekanik

Untuk membuat tampilan alat semakin bagus diperlukan perancangan kotak sebagai berikut :



Gambar 3.9 Gambar Mekanik Alat

Perancangan bahan mekanik menggunakan kayu triplek yang dibungkus scorlet dengan ukuran kurang lebih P = 40 cm, L= 20 dan T = 20 cm. Bagian samping dibuatkan lubang kecil sebagai tempat selang yang nantinya dibungkan ke pompa. Pada bagian belakang dibuat celah untuk masukan power supply dan bagian atas ditempatkan sebuah LCD sebagai tampilan digital dan sebuah meteran analog sebagai pembanding.

Dibawah tampilan LCD terdapat 4 tombol push on yang digunakan untuk memasukkan input perintah berupa :

M = Menu, merupakan pilihan menu yang akan dijalankan

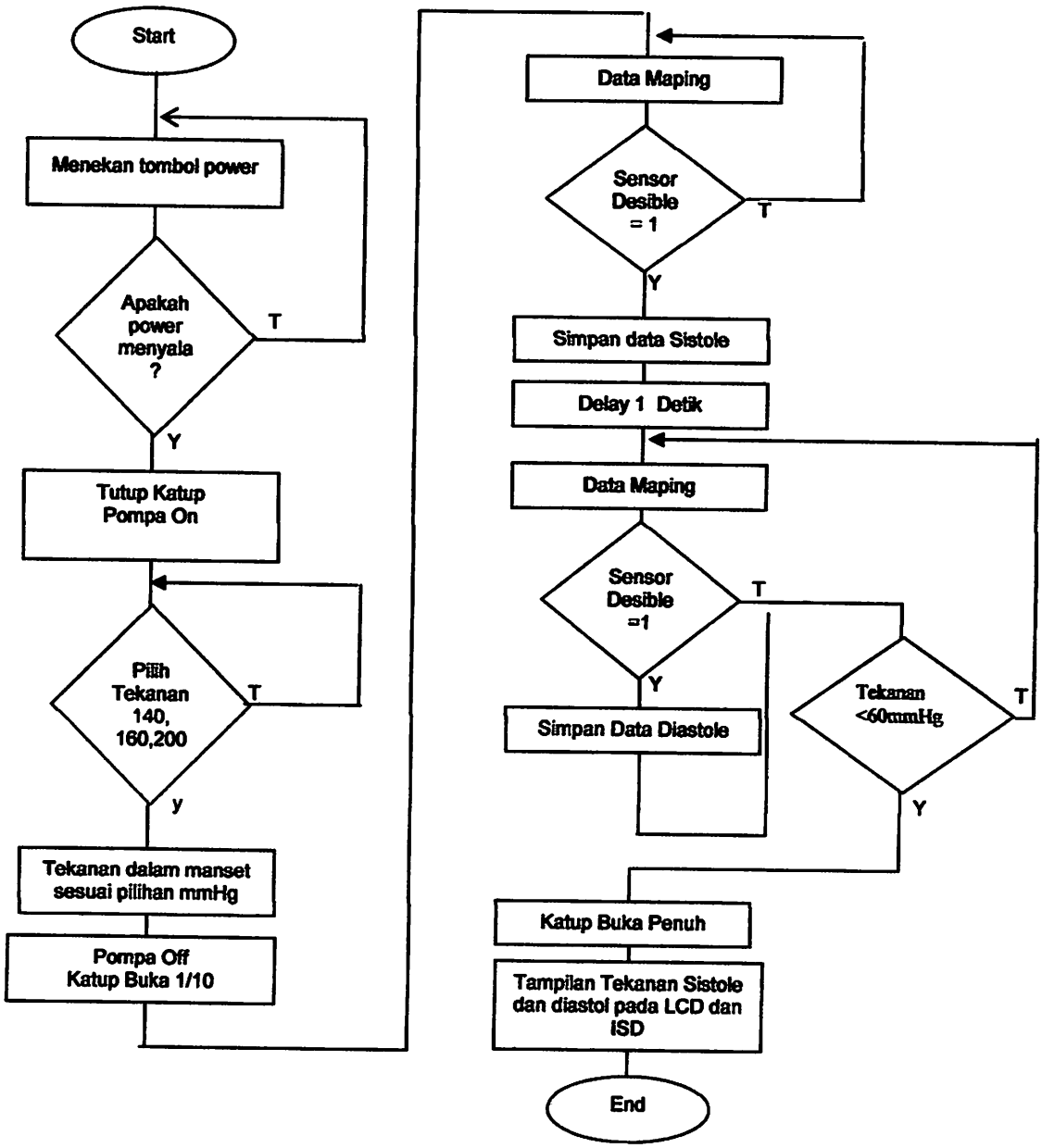
S = Select, merupakan tombol pilihan

C = Cancel, merupakan tombol pembatalan perintah

E = Enter, merupakan tombol perintah langsung pengukuran.

3.4 Perancangan Sofware

Pada pembuatan alat ini agar sistem dapat bekerja sesuai dengan yang diharapkan maka diperlukan pemrograman. Program yang digunakan adalah program yang ditulis dalam bahasa Assembler yang kemudian didownloadkan ke mikrokontroler, Adapun jalannya alat ini dapat dilihat pada flowchart dibawah ini :



Gambar 3.10 Flowchart Program

BAB IV

PENGUJIAN DAN ANALISA DATA

Setelah dilakukan perencanaan dan pembuatan alat diperlukan suatu pengujian alat agar alat dapat bekerja secara optimal sesuai dengan yang diinginkan. Pengujian alat ini meliputi pengujian perangkat seperti pengujian sensor tekanan, rangkaian ADC dan rangkaian keseluruhan.

4.1 Pengoperasian Alat

1. Berikan tegangan pada power supply
2. Cutt of dililitkan pada lengan kanan atas
3. Tekan tombol on untuk memulai pengoperasian alat
4. Pilih menu. Selec, Cancel dan Enter
5. Tunggu sampai pompa mati
6. Hasil pengukuran akan ditampilkan pada LCD dan suara speaker.

4.2 Pengujian Sensor Tekanan

Pada sensor tekanan dilakukan pengujian sebagai berikut :

- Tujuan

  Sensor yang digunakan adalah MPX2050GP, pengujian dilakukan bertujuan untuk mengetahui apakah sensor bekerja dengan baik.

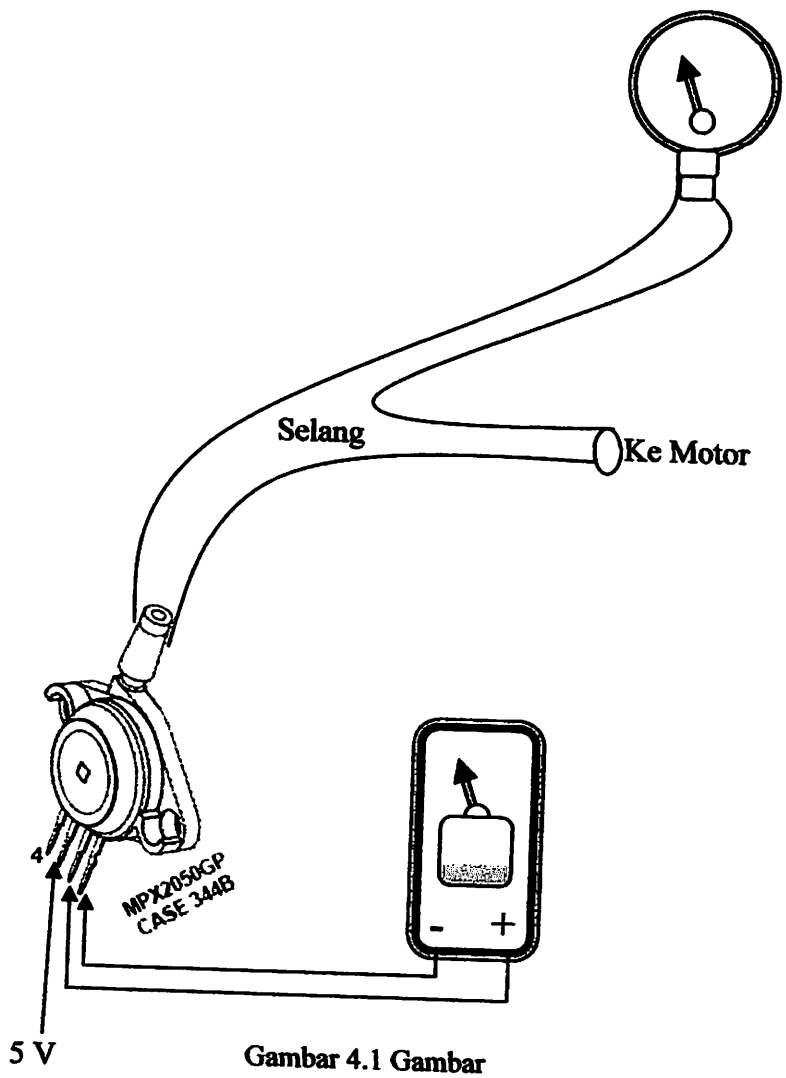
- Peralatan yang digunakan

  1. Pengukur besaran tekanan
  2. Selang udara
  3. Pompa Udara

4. Power Supply
5. Alat Ukur

- Prosedur Pengujian

1. Merangkai segala peralatan sesuai dengan gambar
2. Menjalankan pompa untuk memberikan tekanan pada sensor
3. mengamati secara bersamaan keluaran tekanan pada pengukur besaran tekanan serta voltmeter
4. Mencatat keluaran tegangan yang tertera pada voltmeter.



Gambar 4.1 Gambar Pengujian sensor

- Hasil Pengujian

  a. Perhitungan

  Pada bab 3 diketahui bahwa pertambahan tegangan/mmHg adalah = 0,10666 mV. Jadi di dapat data sebagai berikut

  - Tekanan 200mmHg

    Vout = Pertambahan tegangan x besar tekanan

    Vout = 0,1066 x 200mmHg = 21,33 mV.

  - Tekanan 180 mmHg

    Vout = Pertambahan tegangan x besar tekanan

    Vout = 0,1066 x 180 mmHg = 19,21 mV.

  - Tekanan 160 mmHg

    Vout = Pertambahan tegangan x besar tekanan

    Vout = 0,1066 x 160 mmHg = 17,07 mV.

  - Tekanan 140 mmHg

    Vout = Pertambahan tegangan x besar tekanan

    Vout = 0,1066 x 140 mmHg = 14,94 mV.

  - Tekanan 120 mmHg

    Vout = Pertambahan tegangan x besar tekanan

    Vout = 0,1066 x 120 mmHg = 12,8 mV.

  - Tekanan 100 mmHg

    Vout = Pertambahan tegangan x besar tekanan

    Vout = 0,1066 x 100 mmHg = 10,67 mV.

  - Tekanan 80 mmHg

Vout = Pertambahan tegangan x besar tekanan

Vout = 0,1066 x 80 mmHg = 8,54 mV.

- Tekanan 60 mmHg

Vout = Pertambahan tegangan x besar tekanan

Vout = 0,1066 x 60 mmHg = 6,3 mV.

b. Hasil Pengukuran dan perhitungan

Setelah dilakukan pengujian di dapat data data sebagai berikut :

Tekanan (mmHg)	Tegangan keluaran		Selisih (%)
	Pengukuran (mV)	Perhitungan (mV)	
200	20,80	21,34	0,025
180	20,10	19,21	0,046
160	17,50	17,07	0,025
140	14,80	14,94	0,009
120	13,01	12,8	0,016
100	10,90	10,67	0,021
80	8,65	8,54	0,012
60	8,01	6,37	0,25
Total			0,404

Tabel 4.1 Hasil Pengujian Sensor Tekanan

Pengujian error didapat dari rumus

$$\text{Error} = \frac{perhitungan - pengukuran}{perhitungan} x100\%$$

Contoh : untuk tekanan 200 mmHg

$$\text{Error} = \frac{21,34 - 20,80}{21,34} x100\%$$

$$= 0,025\ \%$$

4.3 Pengujian Rangkaian ADC

- **Tujuan**

  Untuk mengetahui apakah rangkain ADC ini bekerja dengan baik dan mampu mengkondisikan kelurannya 0 dan 1.

- **Peralatan yang digunakan**

  1. Multimeter digital
  2. Rangkaian ADC 0804
  3. Power supply 5 Volt

- **Prosedur Pengujian**

  1. Membuat rangkaian ADC sesuai perencanaan
  2. Menghubugnkan rangkaian ADC dengan catu daya
  3. Melakukan pengukuran
  4. Mengamati hasil pengujian

- **Hasil Pengujian**

  - Perhitungan

    Pada bab 3 diketahui bahwa besarnya resolusi dapat dihitung dengan rumus :

    $$\text{Resolusi} = \frac{Vref}{2^{8-1}}$$

    $$\text{Resolusi} = \frac{5}{255} = 19{,}6\ mV$$

    $$\text{Output ADC} = \frac{Vin}{\text{Re}solusi}$$

- Untuk tegangan 5 Volt

$$\text{Output ADC} = \frac{5}{19{,}6.10^{-3}} = 254(FE\ h)$$

- Untuk tegangan 4,41 Volt

$$\text{Output ADC} = \frac{4{,}41}{19{,}6.10^{-3}} = 225$$

- Untuk tegangan 3,92 Volt

$$\text{Output ADC} = \frac{3{,}92}{19{,}6.10^{-3}} = 200$$

- Untuk tegangan 3,43 Volt

$$\text{Output ADC} = \frac{3{,}43}{19{,}6.10^{-3}} = 175$$

- Untuk tegangan 2,94 Volt

$$\text{Output ADC} = \frac{2{,}94}{19{,}6.10^{-3}} = 150$$

- Untuk tegangan 2,45 Volt

$$\text{Output ADC} = \frac{2{,}45}{19{,}6.10^{-3}} = 125$$

- Untuk tegangan 1,96 Volt

$$\text{Output ADC} = \frac{1{,}96}{19{,}6.10^{-3}} = 100$$

- Untuk tegangan 1,47 Volt

$$\text{Output ADC} = \frac{1{,}47}{19{,}6.10^{-3}} = 75$$

o Pengujian dan pengukuran

Setelah dilakukan pengujian di dapat data data sebagai berikut :

Vin	Data Keluaran		Selisih
	Pengukuran Desimal	Perhitungan desimal	
4,96	253	255	2
4,41	221	225	4
3,92	199	200	1
3,43	170	175	5
2,94	148	150	2
2,45	124	125	1
1,96	98	100	2
1,47	74	75	1

Tabel 4.2 Hasil Pengujian Rangkaian ADC

4.4 Pengujian Pengukur Tekanan Darah secara keseluruhan

Pengujian seluruh sistem dilakukan dengan membandingkan nilai tekanan darah menggunakan analog dengan tekanan darah yang dibuat. Pengujian dilakukan pada 3 orang dengan perulangan sebanyak 3 kali.

- Tujuan

  Mengetahui keakuratan dari pada alat yang telah dibuat

- Peralatan yang digunakan

  1. Pengukur tekanan darah yang telah dirancang
  2. Tensi darah analog

- Prosedur Pengujian .

  1. Menjalankan pompa untuk memberi tekanan pada sensor
  2. Melakukan pencatatan hasil keluaran dari tekanan darah yang dirancang dan tekanan darah analog.

Gambar 4.2 Gambar Alat Keseluruhan

- Hasil Pengujian

a. User Pertama

Jenis Kelamin	Umur	Percobaan	Tekanan sistolik dan diastolik (mmHG)		Error (%)
			Analog	Digital	
L	25	1	110/60	105/61	0,045/0,016
		2		118/65	0,072/0,083
		3		111/63	0,019/0,050
Total eror					0.14/0,167

Tabel 4.3 Hasil Pengujian Tekanan Darah Pada user Pertama

- Kesalahan dapat dicari dari rumus

$$\text{Error} = \frac{ana\log - digital}{ana\log} x100\%$$

$$\text{Error} = \frac{110-105}{110} x100\% = 0{,}045\%$$

- Tekanan sistolik

$$\text{Kesalahan rata-rata} = \frac{0{,}14}{3} = 0{,}05\%$$

- Tekanan diastolik

$$\text{Kesalahan rata-rata} = \frac{0{,}167}{3} = 0{,}06\%$$

b. User Kedua

Jenis Kelamin	Umur	Percobaan	Tekanan sistolik dan diastolik (mmHG)		Error (%)
			Analog	Digital	
L	15	1	90/60	88/65	0,023/0,083
		2		84/63	0,067/0,05
		3		85/61	0,05/0,016
Total eror					0,14/0,153

Tabel 4.4 Hasil Pengujian Tekanan Darah Pada user Kedua

- Kesalahan dapat dicari dari rumus

$$\text{Error} = \frac{ana\log - digital}{ana\log} x100\%$$

$$\text{Error} = \frac{90-88}{90} x100\% = 0{,}023\%$$

- Tekanan sistolik

$$\text{Kesalahan rata-rata} = \frac{0{,}14}{3} = 0{,}05\%$$

- Tekanan diastolik

$$\text{Kesalahan rata-rata} = \frac{0{,}153}{3} = 0{,}051\%$$

c. User Ketiga

Jenis Kelamin	Umur	Percobaan	Tekanan sistolik dan diastolik (mmHG)		Error (%)
			Analog	Digital	
P	40	1	100/65	107/68	0,07/0,046
		2		91/68	0,09/0,046
		3		95/69	0,05/0,06
Total eror					0,21/0,16

Tabel 4.5 Hasil Pengujian Tekanan Darah Pada user Ketiga

- Kesalahan dapat dicari dari rumus

$$\text{Error} = \frac{ana\log - digital}{ana\log} x100\%$$

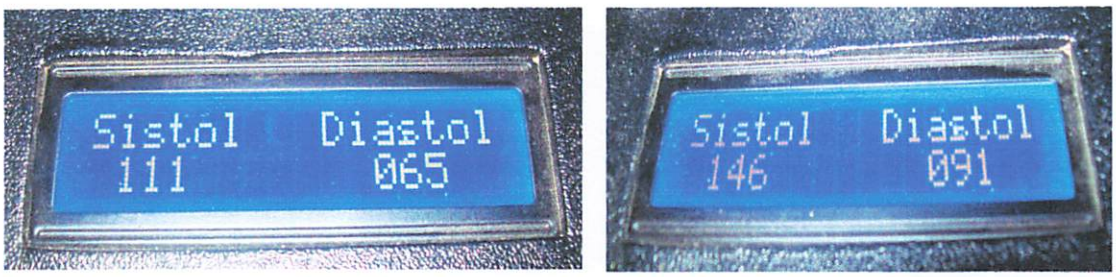
$$\text{Error} = \frac{100-107}{100} x100\% \quad = \quad 0,,07\%$$

- Tekanan sistolik

$$\text{Kesalahan rata-rata} = \frac{0,21}{3} = 0,07\ \%$$

- Tekanan diastolik

$$\text{Kesalahan rata-rata} = \frac{0,167}{3} = 0,06\%$$



Gambar 4.3 Gambar Hasil Pengukuran

Dari perhitungan semua error diatas dapat diambil rata-rata 3 user keseluruhan sebagai berikut :

- Prosenstase kesalahan sistolik

$$\text{Kesalahan rata-rata} = \frac{\sum kesalahan}{9}\%$$

$$\text{Kesalahan rata-rata} = \frac{1{,}7}{9} = 0{,}2\%$$

- Prosenstase kesalahan diastolik

$$\text{Kesalahan rata-rata} = \frac{\sum kesalahan}{9}\%$$

$$\text{Kesalahan rata-rata} = \frac{1{,}5}{9} = 0{,},16\%$$

BAB V

PENUTUP

A. Kesimpulan

Dari hasil perancangan dan pembuatan alat pengukur tekanan darah digital berbasis mikrokontroler AT89S51 tersebut, dapat diambil beberapa kesimpulan sebagai berikut :

1. Pada pembuatan alat ini hanya memerlukan 200 mmHg atau sekitar 3,87 psi. Pilihan tekanan darah terdapat tiga pilihan yaitu 140, 160 dan 200 mmHg. Penurunan tekanan dilakukan dengan pengaturan katup yang dihubungkan dengan motor servo sebagai pemutar.
2. Sumber tegangan menggunakan power supply 5 Volt, sedangkan pada waktu tekanan maksimal 200 mmHg terdapat tegangan keluaran sebesar 21,33 mV.
3. Dari hasil perbandingan pengukuran dan perhitungan alat ini memiliki kesalahan tekanan sistolik 0,2 % dan diastolik diastolik 0,16 %
4. Besarnya eror kebanyakan dikarenakan terlalu pekanya sensor suara yang digunakan sehingga sedikit pergeseran pada waktu mengukur dapat membuat harga pengukuran yang tidak stabil.

B. Saran

1. Diharapkan alat ini dibuat portable dengan menggunakan catu tegangan dari baterai sehingga bisa dibawa kemana-mana.
2. Diharapkan setelah membaca Tugas Akhir ini, dapat dipergunakan sebaik-baiknya
3. Untuk lebih signifikan dalam pengukuran frekuensi suara jantung diharapkan dapat menggunakan penyaring suara yang lebih akurat.
4. Untuk lebih memperkecil ukuran alat alangkah lebih baiknya digunakan ukuran motor yang lebih kecil dan lebih praktis.

DAFTAR PUSTAKA

[1] John G. Webster, *Medical Instrumentation Aplication and Design*, Hougton Miffin Company, Boston, 1978, 375

[2] Internet, *Blood Pressure & Hipertension*, 2008

[3] Data Sheet *Atmel T89S51*, Atmel Corporation, 2001.

[4] Data Sheet *MPX2050*, Motorola Inc, 2005

[5] Robert F. Coughlin and Frederick F. Driscoll, *Penguat Operasional dan Rangkaian Terpadu Linear*, Penerjemah Ir. Herman Widodo Soemitro, Erlangga, 1983.

[6] Data Sheet *ADC 080X*, National semiconductor., 2001

[7] Data sheet LCD 2x16, Winboard.2005

[8] Data Sheet ISD 2560/75/90/120, Winbond Electronic Corp.

[9] www. buzzer-speaker.com

LAMPIRAN

PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL MALANG

INSTITUT TEKNOLOGI NASIONAL MALANG

FAKULTAS TEKNOLOGI INDUSTRI
FAKULTAS TEKNIK SIPIL DAN PERENCANAAN
PROGRAM PASCASARJANA MAGISTER TEKNIK

ERSERO) MALANG
NIAGA MALANG

Kampus I : Jl. Bendungan Sigura-gura No. 2 Telp. (0341) 551431 (Hunting), Fax. (0341) 553015 Malang 65145
Kampus II : Jl. Raya Karanglo, Km 2 Telp. (0341) 417636 Fax. (0341) 417634 Malang

Nomor : 085/EL-08/TA/2008
Lampiran : -
Perihal : Bimbingan Tugas Akhir

Kepada : Yth. Ir. Yudi Lipraptono,MT
Dosen Institut Teknologi Nasional
Malang

Dengan Hormat,

Sesuai dengan permohonan persetujuan dalam Tugas Akhir untuk mahasiswa:

N a m a	:	M. Ali Rofik
No. Mahasiswa	:	0452215
Program Studi	:	Teknik Elektro D-III
Judul Tugas Akhir	:	Pengukur Tekanan Darah Digital dengan Pemanfaatan MK AT 89S51

Maka dengan ini pembimbingan Tugas Akhir tersebut kami serahkan sepenuhnya kepada saudara, terhitung mulai tanggal 16/08/2008 s/d 04/12/2008

Demikian agar maklum dan atas perhatian serta bantuannya kami ucapkan terima kasih.

Malang, 4 Agustus 2008
Ketua Program Studi
Teknik Elektro D-III

Ir. Choirul Saleh,MT
NIP. 1018800190

PERKUMPULAN PENGELOLA PENDIDIKAN UMUM DAN TEKNOLOGI NASIONAL MALANG
INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
FAKULTAS TEKNIK SIPIL DAN PERENCANAAN
PROGRAM PASCASARJANA MAGISTER TEKNIK

BNI (PERSERO) MALANG
BANK NIAGA MALANG

Kampus I : Jl. Bendungan Sigura-gura No. 2 Telp. (0341) 551431 (Hunting), Fax. (0341) 553015 Malang 65145
Kampus II : Jl. Raya Karanglo, Km 2 Telp. (0341) 417636 Fax. (0341) 417634 Malang

Nomor : 080/EL-04/TA/2008
Lampiran : -
Perihal : Bimbingan Tugas Akhir

Kepada : Yth. Ir. Yudi Lipraptono,MT
Dosen Institut Teknologi Nasional
Malang

Dengan Hormat,

Sesuai dengan permohonan persetujuan dalam Tugas Akhir untuk mahasiswa:

N a m a : M. Ali Rofik
No. Mahasiswa : 0452215
Program Studi : Teknik Elektro D-III
Judul Tugas Akhir : Pengukur Tekanan Darah Digital dengan Pemanfaatan MK ATMEGA 8535

Maka dengan ini pembimbingan Tugas Akhir tersebut kami serahkan sepenuhnya kepada saudara, terhitung mulai tanggal 16/04/2008 s/d 04/08/2008

Demikian agar maklum dan atas perhatian serta bantuannya kami ucapkan terima kasih.

Malang, 116 April 2008
Ketua Jurusan Jurusan Teknik Elektro D-III

Ir. Choirul Saleh,MT
NIP. 1018800190

INSTITUT TEKNOLOGI NASIONAL MALANG
JURUSAN TEKNIK ELEKTRO DIPLOMA TIGA (D-III)
MALANG

UT - 1

Lampiran : 1(satu) berkas Proposal
Perihal : Permohonan Kesediaan Dosen Pembimbing

Kepada : Yth. Bapak/Ibu. Ir. Yudi Lipraptono,MT
Institut Teknologi Nasional Malang
di
M a l a n g

Dengan hormat,

Kami yang bertanda tangan dibawah ini :

N a m a : M. Ali Rofik

No. Mahasiswa : 0452215

Program Studi : Teknik Elektro D-III

Dengan ini mengajukan permohonan, sekiranya Bapak/Ibu bersedia menjadi Dosen Pembimbing Utama/Pendamping*), untuk penyusunan Tugas Akhir .

Judul Tugas Akhir : Pengukur Tekanan Darah Digital dengan Pemanfaatan MK ATMEGA 8535

Adapun tugas tersebut adalah salah satu syarat untuk menempuh Ujian Tugas Akhir Program D-III.
Demikian permohonan kami dan atas kesediaan Bapak/Ibu kami ucapkan terima kasih.

Malang, 116 April 2008

Mengetahui
Ketua Jurusan
Teknik Elektro D-III

Ir. Choirul Saleh,MT
NIP.Y. 1018800190

M. Ali Rofik

INSTITUT TEKNOLOGI NASIONAL MALANG
JURUSAN TEKNIK ELEKTRO DIPLOMA TIGA (D-III)
MALANG

UT - 2

KESEDIAAN PEMBIMBING
TUGAS AKHIR

Sesuai permohonan dari mahasiswa :

N a m a : M. Ali Rofik

No. Mahasiswa : 0452215

Program Studi : Teknik Elektro D-III

Judul Tugas Akhir : Pengukur Tekanan Darah Digital dengan Pemanfaatan MK ATMEGA 8535

Bahwa kami bersedia membimbing Tugas Akhir dari mahasiswa tersebut.

Jangka waktu penyelesaian Tugas Akhir selama 4 (empat) bulan mulai tanggal 16/04/2008 s/d 04/08/2008 dan apabila dalam jangka waktu tersebut belum selesai maka tugas akhir tersebut dinyatakan **GUGUR**

Malang, 16 April 2008

Dosen Pembimbing;

Ir. Yudi Lipraptono,MT

NIP. 1039700274

Nb :
Setelah disetujui agar formulir ini diserahkan Mahasiswa yang bersangkutan kepada sekretaris Program Studi Teknik Elektro D-III

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNOLOGI ELEKTRO D-III

LEMBAR ASISTENSI
BIMBINGAN TUGAS AKHIR

Nama : MOH. ALI ROFIK
NIM : 04.52.215
Jurusan : Teknik Elektro D-III
Judul : PENGUKUR TEKANAN DARAH DIGITAL DENGAN PEMANFATAN MIKROKONTROLER AT89S51
Dosen Pembimbing : Ir. F. Yudi Lipraptono, MT

No	Tanggal	Asistensi	Paraf
1		Bab I	
2		Bab II	
3		Bab III	
4		Bab IV	
5		Demo	
6	17/9 08	Bab V	

Malang, Agustus 2008

Ir. F. Yudi Lipraptono, MT
NIPY. 1039.500.274

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNOLOGI ELEKTRO D-III

LEMBAR PERBAIKAN

Nama : Muhammad Ali Rofik
Nim : 04.52.215
Program Studi : Teknik Elektro D-III
Konsentrasi : Teknik Elektronika
Judul : PENGUKUR TEKANAN DARAH DIGITAL DENGAN PEMANFATAN MIKROKONTROLER AT89S51
Dosen Pembimbing : Ir. F. Yudi Lipraptono, MT

No	Tanggal	Revisi	Paraf
1		Teori Dasar Kondensor Mic	
2		Gambar Alat	
3			

Telah diperiksa / disetujui

(Ir. Eko Nur Cahyo)
Dosen Penguji I

(Irmalia Suryani Faradisa, ST,MT)
Dosen Penguji II

Mengetahui

(Ir. F. Yudi Lipraptono, MT)
Dosen Pembimbing

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
PROGRAM STUDI TEKNIK ELEKTRONIKA
MALANG

BERITA ACARA UJIAN TUGAS AKHIR
PROGRAM STUDI TEKNIK ELEKTRO D-III
FAKULTAS TEKNOLOGI INDUSTRI

Nama	: MUHAMMAD ALI ROFIK
Nim	: 04.52.215
Program Studi	: Teknik Elektro D-III
Konsentrasi	: Teknik Elektronika
Judul Tugas Akhir	: Pengukur Tekanan Darah Digital Dengan Pemanfaatan Mikrokontroler AT89S51

Dipertahankan dihadapan Tim Penguji Tugas Akhir jenjang Diploma Tiga (D-III) :

Pada Hari	: Rabu
Tanggal	: 24 September 2008
Dengan Nilai	: 79.00 (B+)

Panitia ujian Tugas Akhir

INSTITUT TEKNOLOGI NASIONAL MALANG FAKULTAS TEKNOLOGI INDUSTRI ITN DEKAN

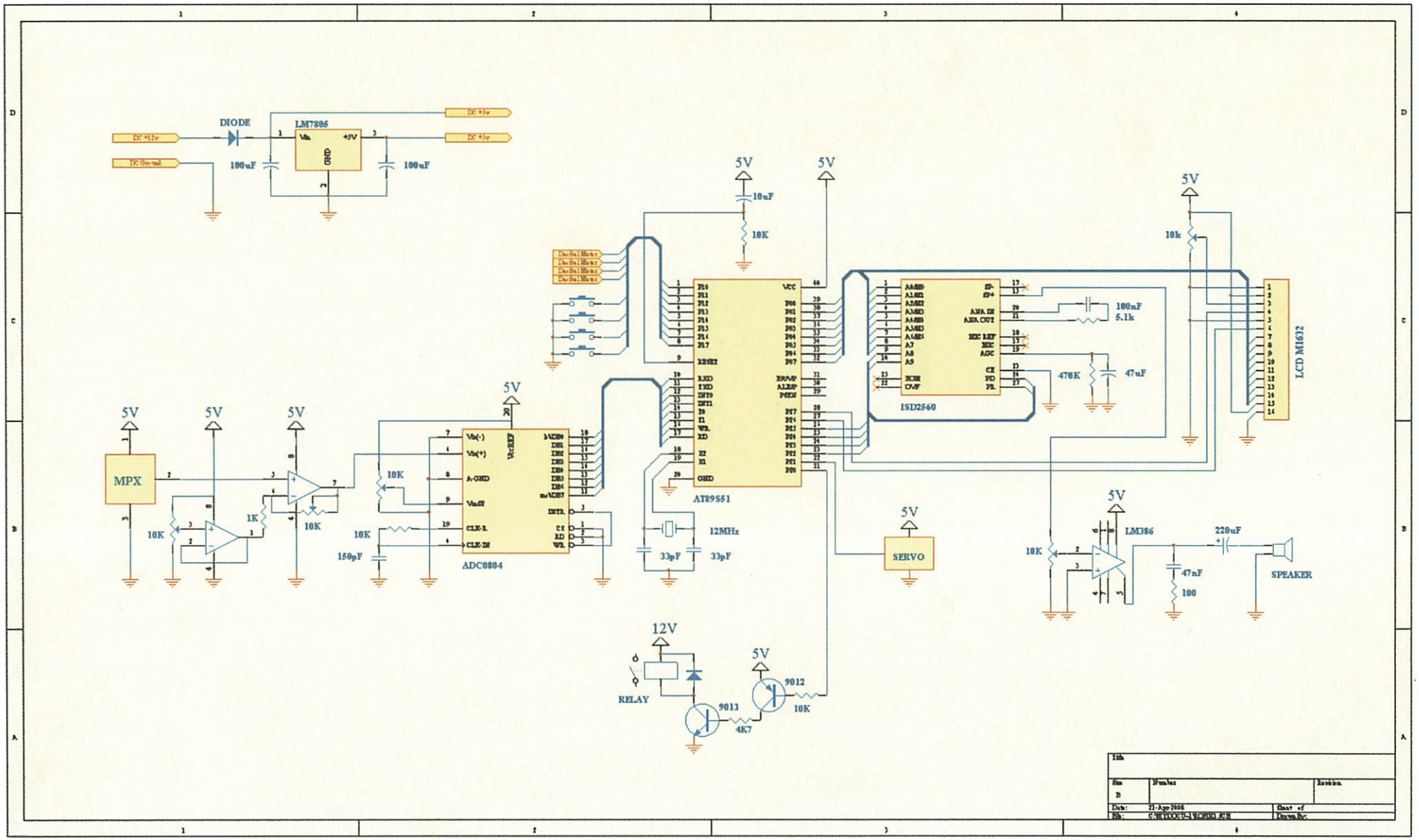
(Ir. Mochtar Asroni, MSME)
Ketua Majelis Penguji

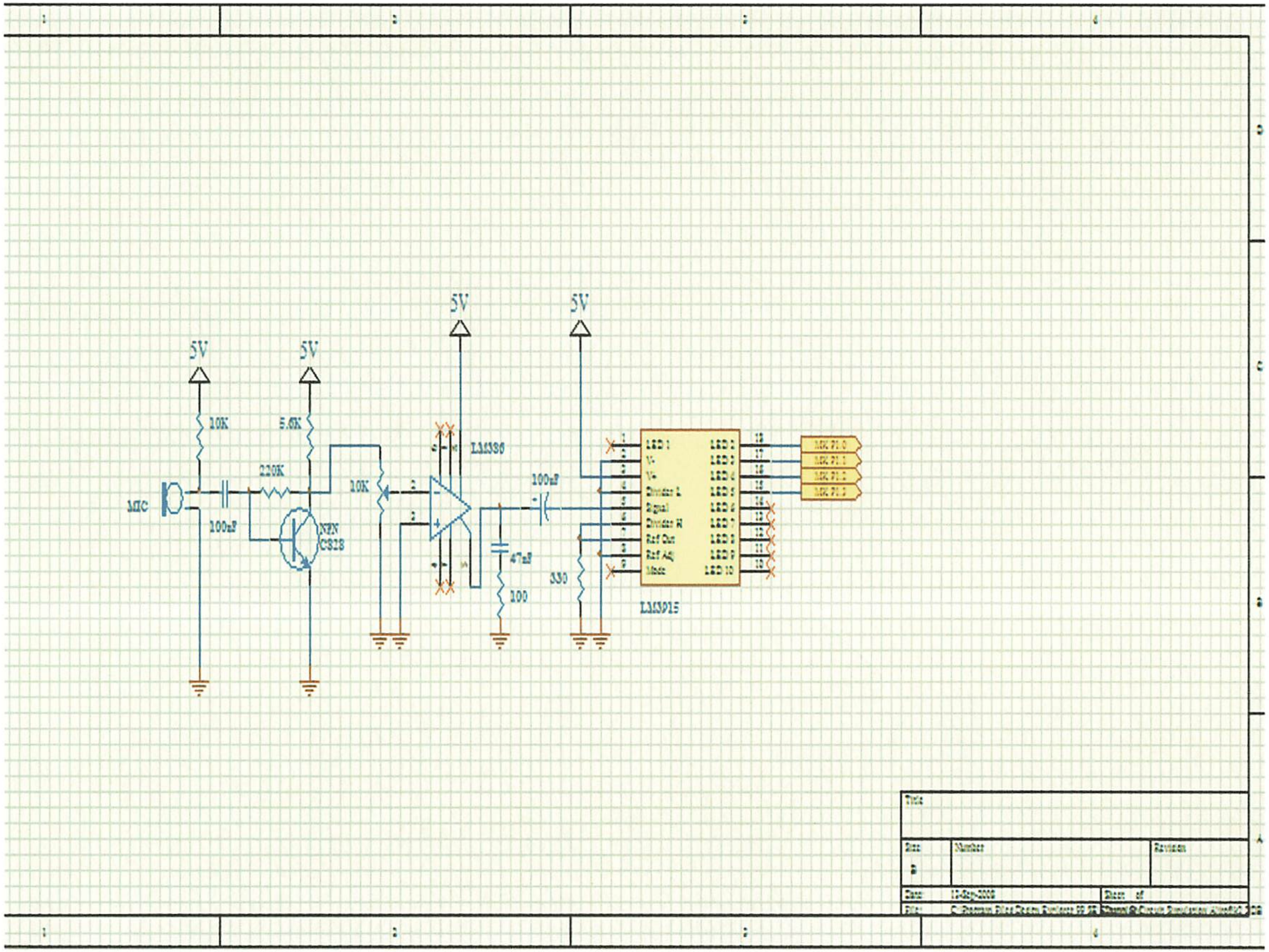
(Ir. H. Choirul Saleh, MT)
Sekretaris Majelis Penguji

Anggota Penguji

(Ir. Eko Nur Cahyo)
Dosen Penguji I

(Irmalia Suryani Faradisa, ST,MT)
Dosen Penguji II


DIODE
LM7805
100uF
100uF
5V
10uF
10K
10k
100nF
5.1k
470K
47uF
ISD2560
LCD M1632
MPX
1K
10K
ADC0804
150pF
AT89S51
12MHz
33pF
33pF
SERVO
LM386
220uF
47nF
100
SPEAKER
12V
RELAY
9013
4K7
9012



MIC
5V
10K
100nF
220K
5.6K
NPN
C828
10K
LM386
47uF
100
330
LM3915
LED 1
V-
V+
Divider L
Signal
Divider H
Ref Out
Ref Adj
Mode
LED 2
LED 3
LED 4
LED 5
LED 6
LED 7
LED 8
LED 9
LED 10
Title
Size
B
Number
Revision
Date:
Sheet of
File:

```
        org   00h
;
        Dcbl   Bit P1.3
        Tbl3   Bit P1.4
        Tbl2   Bit P1.5
        Tbl1   Bit P1.6
        Tbl0   Bit P1.7
        Srvo   Bit P2.0
        Pmpa   Bit P2.1
        Hibt   Bit P2.2          ; ISD address High
        ISTR   Bit P2.3          ; ISD start
        Lobt   Bit P2.4          ; ISD address Low
        Rest   Bit P2.6
        Enbl   Bit P2.7
        Stts   Bit 20h.0
        Bicr   Equ 30h
        Dbts   Equ 31h
        Char   Equ 32h
        Cntr   Equ 33h
        DtsL   Equ 34h
        Dtsl1  Equ 35h
        Dtss   Equ 36h           ; data sistol
        Dtds   Equ 37h           ; data diastol
        Buf0   Equ 38h
        Buf1   Equ 39h
        Buf2   Equ 3Ah
        Dly0   Equ 3Bh
        Dly1   Equ 3Ch
        Dly2   Equ 3Dh
;
init:  acall  lcd_in
       acall  inir_in
       mov    Dbts,#140
       mov    R6,#1
;
mulai: mov    DPTR,#nama
       acall  line1
       mov    Char,#16
       acall  tulis
       mov    DPTR,#nim
       acall  line2
       mov    Char,#16
       acall  tulis
       acall  delay2
       mov    DPTR,#jur
       acall  line1
```

```
        mov   Char,#16
        acall tulis
        mov   DPTR,#univ
        acall line2
        mov   Char,#16
        acall tulis
        acall delay2
        sjmp  mulai
;
plmenu: mov   DPTR,#tplmenu
        lcall line1
        mov   Char,#16
        lcall tulis
plmnu0: cjne  R6,#1,plmnu1
        mov   DPTR,#tmamn0
plmnu1: cjne  R6,#2,plmnu2
        mov   DPTR,#tmamn1
plmnu2: lcall line2
        mov   Char,#16
        lcall tulis
        lcall tlptb1
plmnu3: lcall delay0
        jb    Tbl1,plmnu5
        inc   R6
        cjne  R6,#3,plmnu4
        mov   R6,#1
plmnu4: ljmp  plmnu0
plmnu5: jb    Tbl2,plmnu6
        mov   SP,#07h
        ljmp  mulai
plmnu6: jb    Tbl3,plmnu3
        lcall tlptb3
plmnu7: cjne  R6,#1,plmnu8
        mov   R7,#1
        ljmp  tester
plmnu8: cjne  R6,#2,plmnu7
        mov   R7,#1
        ljmp  seting
;
tester: mov   DPTR,#tmamn0
        lcall line1
        mov   Char,#16
        lcall tulis
tster0: cjne  R7,#1,tster1
        mov   DPTR,#tsbmn0
tster1: cjne  R7,#2,tster2
```

```
        mov    DPTR,#tsbmn1
 tster2: cjne   R7,#3,tster3
        mov    DPTR,#tsbmn2
 tster3: lcall  line2
        mov    Char,#16
        lcall  tulis
        lcall  tlptb1
        lcall  tlptb3
 tster4: lcall  delay0
        jb     Tbl1,tster6
        inc    R7
        cjne   R7,#4,tster5
        mov    R7,#1
 tster5: ljmp   tster0
 tster6: jb     Tbl2,tster7
        lcall  tlptb2
        ljmp   plmenu
 tster7: jb     Tbl3,tster4
        lcall  tlptb3
 tster8: cjne   R7,#1,tster9
        ljmp   tstpmp
 tster9: cjne   R7,#2,tsterA
        ljmp   tstsrv
 tsterA: cjne   R7,#3,tster8
        ljmp   tstsns
;
 tstpmp: mov    DPTR,#tsbmn0
        lcall  line1
        mov    Char,#16
        lcall  tulis
 tspmp0: mov    DPTR,#tsbmn7
        lcall  line2
        mov    Char,#16
        lcall  tulis
 tspmp1: jb     Tbl3,tspmp2
        clr    Pmpa
        mov    DPTR,#tsbmn8
        lcall  line2
        mov    Char,#16
        lcall  tulis
        lcall  tlptb3
 tspmp2: jnb    Tbl3,tspmp3
        setb   Pmpa
 tspmp3: jb     Tbl2,tspmp0
        lcall  tlptb2
        ljmp   tester
```

```
;
tstsrv: mov    DPTR,#tsbmn1
        lcall  line1
        mov    Char,#16
        lcall  tulis
        mov    R6,#1
tssrv0: cjne   R6,#1,tssrv1
        mov    DPTR,#tsbmn9
tssrv1: cjne   R6,#2,tssrv2
        mov    DPTR,#tsbmnA
tssrv2: cjne   R6,#3,tssrv3
        mov    DPTR,#tsbmnB
tssrv3: lcall  line2
        mov    Char,#16
        lcall  tulis
        lcall  tlptb1
        lcall  tlptb3
tssrv4: cjne   R6,#1,tssrv6
        mov    Cntr,#100
tssrv5: lcall  srvo01
        djnz   Cntr,tssrv5
tssrv6: cjne   R6,#2,tssrv8
        mov    Cntr,#100
tssrv7: lcall  srvo02
        djnz   Cntr,tssrv7
tssrv8: cjne   R6,#3,tssrvA
        mov    Cntr,#100
tssrv9: lcall  srvo00
        djnz   Cntr,tssrv9
;
tssrvA: lcall  delay0
        jb     Tbl1,tssrvC
        inc    R6
        cjne   R6,#4,tssrvB
        mov    R6,#1
tssrvB: ljmp   tssrv0
tssrvC: jb     Tbl2,tssrvA
        lcall  tlptb2
        ljmp   tester
;
tstsns: acall  lcdclr
        mov    DPTR,#tsbmn2
        lcall  line1
        mov    Char,#16
        lcall  tulis
tssns0: mov    P0,#0C4h
```

```
        acall  w_ins
;       mov    DPTR,#lookup
        mov    A,P3
;       movc   A,@A+DPTR
        mov    B,#100
        div    AB
        mov    DPTR,#angka
        acall  wr_chr
        mov    A,B
        mov    B,#10
        div    AB
        acall  wr_chr
        mov    A,B
        acall  wr_chr
        mov    P0,#' '
        acall  w_chr
        mov    P0,#'m'
        acall  w_chr
        mov    P0,#'m'
        acall  w_chr
        mov    P0,#'H'
        acall  w_chr
        mov    P0,#'g'
        acall  w_chr
        mov    P0,#0D0h
        acall  w_ins
        acall  delay1
        jb     Tbl2,tssns0
        lcall  tlptb2
        ljmp   tester
;
seting: mov    DPTR,#stgbts
        lcall  line1
        mov    Char,#16
        lcall  tulis
stbts0: cjne   R7,#1,stbts1
        mov    DPTR,#tsbmn4
stbts1: cjne   R7,#2,stbts2
        mov    DPTR,#tsbmn5
stbts2: cjne   R7,#3,stbts3
        mov    DPTR,#tsbmn6
stbts3: lcall  line2
        mov    Char,#16
        lcall  tulis
        lcall  tlptb1
        lcall  tlptb3
```

```
stbts4: lcall  delay0
        jb     Tbl1,stbts6
        inc    R7
        cjne   R7,#4,stbts5
        mov    R7,#1
stbts5: ljmp   stbts0
stbts6: jb     Tbl2,stbts7
        lcall  tlptb2
        ljmp   plmenu
stbts7: jb     Tbl3,stbts4
        lcall  tlptb3
stbts8: cjne   R7,#1,stbts9
        mov    Dbts,#140
stbts9: cjne   R7,#2,stbtsA
        mov    Dbts,#160
stbtsA: cjne   R7,#3,stbtsB
        mov    Dbts,#200
stbtsB: ljmp   plmenu
;
stpngr: acall  lcdclr
        mov    DPTR,#tsbmnE
        lcall  line1
        mov    Char,#16
        lcall  tulis
        lcall  tlptb3
stpng0: jb     Tbl2,stpng1
        lcall  tlptb2
        mov    SP,#07h
        ljmp   mulai
stpng1: jb     Tbl3,stpng0
        lcall  tlptb3
        clr    Stts
        mov    DPTR,#btspmp
        lcall  line1
        mov    Char,#16
        lcall  tulis
        mov    DPTR,#angka
        mov    P0,#89h
        acall  w_ins
        mov    A,Dbts
        mov    B,#100
        div    AB
        lcall  wr_chr
        mov    A,B
        mov    B,#10
        div    AB
```

```
        lcall   wr_chr
        mov     A,B
        lcall   wr_chr
        mov     P0,#0D0h
        acall   w_ins
        mov     Cntr,#100
stpng2: lcall   srvo00                  ; katup tutup
        djnz    Cntr,stpng2
        clr     Pmpa
        mov     DPTR,#tggpas
        lcall   line2
        mov     Char,#16
        lcall   tulis
stpng3: mov     P0,#0C9h
        acall   w_ins
        mov     DPTR,#lookup
        mov     A,P3
        movc    A,@A+DPTR
        mov     B,#100
        div     AB
        mov     DPTR,#angka
        lcall   wr_chr
        mov     A,B
        mov     B,#10
        div     AB
        lcall   wr_chr
        mov     A,B
        lcall   wr_chr
        mov     P0,#0D0h
        acall   w_ins
;
        mov     DPTR,#lookup
        mov     A,P3
        movc    A,@A+DPTR
        mov     B,#bits
        div     AB
        cjne    A,#0,stpng4
        ljmp    stpng3
stpng4: setb    Pmpa
        mov     Cntr,#50
stpng5: lcall   srvo00                  ; katup buka
        djnz    Cntr,stpng5
        acall   delay3
        acall   lcdclr
        mov     DPTR,#sisdia
        lcall   line1
```

```
        mov    Char,#16
        lcall  tulis
 stpng6: jb    Stts.ckdtk0
        mov    P0,#0C1h
        acall  w_ins
        mov    DPTR,#lookup
        mov    A,P3
        movc   A,@A+DPTR
        mov    Dtss,A
        mov    B,#100
        div    AB
        mov    DPTR,#angka
        lcall  wr_chr
        mov    A,B
        mov    B,#10
        div    AB
        lcall  wr_chr
        mov    A,B
        lcall  wr_chr
        mov    P0,#0D0h
        acall  w_ins
;
ckdtk0: jb     Dcbl,ckdtk1
        setb   Stts
        mov    P0,#0CBh
        acall  w_ins
        mov    DPTR,#lookup
        mov    A,P3
        movc   A,@A+DPTR
        mov    Dtds,A
        mov    B,#100
        div    AB
        mov    DPTR,#angka
        lcall  wr_chr
        mov    A,B
        mov    B,#10
        div    AB
        lcall  wr_chr
        mov    A,B
        lcall  wr_chr
        mov    P0,#0D0h
        acall  w_ins
;
ckdtk1: mov    DPTR,#lookup
        mov    A,P3
        movc   A,@A+DPTR
```

```
      mov   B,A
      mov   A,#60
      div   AB
      cjne  A,#0,stpng7
      ljmp  stpng6
stpng7: mov   Cntr,#100
stpng8: lcall  srvo02                ; katup buka 2
      djnz  Cntr,stpng8
;
      mov   A,Dtss
      acall sstlan
      acall bcrdpg
      mov   A,Dtds
      acall dstlan
      acall bcrdpg
;
bole00: jb    Tbl2,bole00            ; tekan cancel
      acall tlptb2
      mov   SP,#07h                  ; reset RAM
      ljmp  mulai
;
bcrdpg: mov   B,#100                       ; ISD bicara data pengukuran
      div   AB                 ;\
      mov   Buf0,A             ; |
      mov   A,B                ; |
      mov   B,#10              ; | cacah data
      div   AB                 ; |
      mov   Buf1,A             ; |
      mov   Buf2,B             ;/
;
bcrp00: mov   A,Buf0
      cjne  A,#0,bcrp01              ; digit pertama = 0 lompat
      sjmp  bcrp03
bcrp01: cjne  A,#1,bcrp02            ; digit pertama = 1 -> seratus
      acall serats
      sjmp  bcrp03                   ; digit pertama bkn 0/1 ->
bcrp02: acall cekn0                  ;  cocokkan data
      acall ratus                    ;  ratus
;
bcrp03: mov   A,Buf1
      cjne  A,#0,bcrp04              ; digit kedua = 0 lompat
      sjmp  bcrp08
bcrp04: cjne  A,#1,bcrp07            ; digit kedua = 1 ->
      mov   A,Buf2                   ;  digit ketiga = 0 -> sepuluh
        cjne  A,#0,bcrp05
      acall sepulh                   ;  digit ketiga = 1 -> sebelas
```

```
        sjmp   bcrp0A
  bcrp05: cjne   A,#1,bcrp06
        acall  sebels                ;  digit ketiga bkn 0/1 ->
        sjmp   bcrp0A
  bcrp06: acall  cckn0               ;  cocokkan data
        acall  belas                 ;  belas
        sjmp   bcrp0A
  ;
  bcrp07: acall  cckn0               ;  digit kedua bkn 0/1 ->
        acall  puluh                 ;  cocokkan data + puluh
  bcrp08: mov    A,Buf2                    ;  digit ketiga = 0 -> lompat
          cjne   A,#0,bcrp09
        sjmp   bcrp0A
  bcrp09: acall  cckn0               ;  cocokkan data
  bcrp0A: ret
  ;
  satu:  clr    Lobt                 ; satu
        clr    Hibt
        mov    P0,#00
        clr    ISTR
        mov    Bicr,#10
        lcall  bicara
        setb   ISTR
        lcall  delay1
        ret
  ;
  dua:   clr    Lobt                 ; dua
       clr    Hibt
       mov    P0,#16
       clr    ISTR
       mov    Bicr,#10
       lcall  bicara
       setb   ISTR
       lcall  delay1
       ret
  ;
  tiga:  clr    Lobt                 ; tiga
       clr    Hibt
       mov    P0,#30
       clr    ISTR
       mov    Bicr,#10
       lcall  bicara
       setb   ISTR
       lcall  delay1
       ret
;
```

```
empat: clr   Lobt              ; empat
       clr   Hibt
       mov   P0,#48
       clr   ISTR
       mov   Bicr,#10
       lcall bicara
       setb  ISTR
       lcall delay1
       ret
;
lima:  clr   Lobt              ; lima
       clr   Hibt
       mov   P0,#64
       clr   ISTR
       mov   Bicr,#10
       lcall bicara
       setb  ISTR
       lcall delay1
       ret
;
enam:  clr   Lobt              ; enam
       clr   Hibt
       mov   P0,#80
       clr   ISTR
       mov   Bicr,#10
       lcall bicara
       setb  ISTR
       lcall delay1
       ret
;
tujuh: clr   Lobt              ; tujuh
       clr   Hibt
       mov   P0,#96
       clr   ISTR
       mov   Bicr,#10
       lcall bicara
       setb  ISTR
       lcall delay1
       ret
;
delapn: clr  Lobt              ; delapan
       clr   Hibt
       mov   P0,#114
       clr   ISTR
       mov   Bicr,#12
       lcall bicara
```

```
        setb   ISTR
        lcall  delay1
        ret
;
sembln: clr    Lobt                ; sembilan
        clr    Hibt
        mov    P0,#130
        clr    ISTR
        mov    Bicr,#12
        lcall  bicara
        setb   ISTR
        lcall  delay1
        ret
;
sepulh: clr    Lobt                ; sepuluh
        clr    Hibt
        mov    P0,#145
        clr    ISTR
        mov    Bicr,#12
        lcall  bicara
        setb   ISTR
        lcall  delay1
        ret
;
puluh:  clr    Lobt                ; puluh
        clr    Hibt
        mov    P0,#160
        clr    ISTR
        mov    Bicr,#10
        lcall  bicara
        setb   ISTR
        lcall  delay1
        ret
;
sebels: clr    Lobt                ; sebelas
        clr    Hibt
        mov    P0,#178
        clr    ISTR
        mov    Bicr,#12
        lcall  bicara
        setb   ISTR
        lcall  delay1
        ret
;
belas:  clr    Lobt                ; belas
       clr    Hibt
```

```
        mov    P0,#192
        clr    ISTR
        mov    Bicr,#10
        lcall  bicara
        setb   ISTR
        lcall  delay1
        ret
;
serats: clr    Lobt                ; seratus
        clr    Hibt
        mov    P0,#210
        clr    ISTR
        mov    Bicr,#12
        lcall  bicara
        setb   ISTR
        lcall  delay1
        ret
;
ratus:  clr    Lobt                ; ratus
        clr    Hibt
        mov    P0,#224
        clr    ISTR
        mov    Bicr,#10
        lcall  bicara
        setb   ISTR
        lcall  delay1
        ret
;
sstlan: clr    Lobt                ; sistol anda
        clr    Hibt
        mov    P0,#240
        clr    ISTR
        mov    Bicr,#16
        lcall  bicara
        setb   ISTR
        lcall  delay1
        ret
;
dstlan: setb   Lobt                ; diastol anda
        clr    Hibt
        mov    P0,#8
        clr    ISTR
        mov    Bicr,#16
        lcall  bicara
        setb   ISTR
        lcall  delay1
```

```
        ret
;
cckn0: cjne   A,#1,cckn1
       lcall  satu
cckn1: cjne   A,#2,cckn2
       lcall  dua
cckn2: cjne   A,#3,cckn3
       lcall  tiga
cckn3: cjne   A,#4,cckn4
       lcall  empat
cckn4: cjne   A,#5,cckn5
       lcall  lima
cckn5: cjne   A,#6,cckn6
       lcall  enam
cckn6: cjne   A,#7,cckn7
       lcall  tujuh
cckn7: cjne   A,#8,cckn8
       lcall  delapn
cckn8: cjne   A,#9,cckn9
       lcall  sembln
cckn9: ret
;
line1: mov    P0,#080h
       acall  w_ins
       ret
;
tlptb0: lcall  delay0
       jnb    Tbl0,tlptb0
       ret
;
tlptb1: lcall  delay0
       jnb    Tbl1,tlptb1
       ret
;
tlptb2: lcall  delay0
       jnb    Tbl2,tlptb2
       ret
;
tlptb3: lcall  delay0
       jnb    Tbl3,tlptb3
       ret
;
srvo00: mov    DtsL,#0D0h          ; tutup
       mov    DtsH,#0F6h
       lcall  htpwsv
       ret
```

```
;
srvo01: mov   DtsL,#050h          ; buka 1
     mov   DtsH,#0F7h
     lcall  htpwsv
       ret
;
srvo02: mov   DtsL,#050h          ; buka 2
     mov   DtsH,#0FEh
     lcall  htpwsv
       ret
;
htpwsv: setb  Srvo                ; pwm logic 1
     mov   TL0,DtsL          ;\
     mov   TH0,DtsH          ; | tahan selama ? ms
     lcall  tnggu            ;/
     clr   Srvo               ; pwm logic 0
     mov   TL0,#0E0h          ;\
     mov   TH0,#0B1h          ; | tahan selama 20ms
     lcall  tnggu             ;/
     ret
;
tnggu: clr   TF0                  ;\
     setb  TR0                ; | tahan selama ? ms
     jnb   TF0,$              ;/
     clr   TR0
     ret
;
tmr_in: mov   TMOD,#11h
     ret
;
line2:  mov   P0,#0C0h
     acall  w_ins
     ret
;
tulis:  clr   A
     acall  wr_chr
     inc   DPTR
     djnz   Char.tulis
     ret
;
wr_chr: movc  A,@A+DPTR
     mov   P0,A
     acall  w_chr
     ret
;
w_ins:  clr   Enbl
```

1 - 2ms

```
        clr   Rest
        setb  Enbl
        clr   Enbl
        acall delay0
        ret
;
w_chr:  clr   Enbl
        setb  Rest
        setb  Enbl
        clr   Enbl
        acall delay0
        ret
;
lcd_in: acall delay1
        mov   P0,#01h          ; Display Clear
        acall w_ins
        mov   P0,#38h          ; Function Set
        acall w_ins
        mov   P0,#0Dh          ; Display On, Cursor, Blink
        acall w_ins
        mov   P0,#06h          ; Entry Mode
        acall w_ins
        mov   P0,#02h          ; Cursor Home
        acall w_ins
        ret
;
lcdclr: mov   P0,#01h          ; Display Clear
        acall w_ins
        acall delay0
        acall delay0
        ret
;
delay0: djnz  Dly0,delay0
        ret
;
delay1: lcall delay0
        djnz  Dly1,delay1
dly10:  jb    Tbl0,dly11
        mov   R6,#1
        ljmp  plmenu
dly11:  jb    Tbl3,dly12
        ljmp  stpngr
dly12:  ret

;
delay2: mov   Dly2,#20
```

```
dely2: acall  delay1
       djnz   Dly2,dely2
       ret
;
delay3: mov    Dly2,#8
dely3: acall  delay1
       djnz   Dly2,dely3
       ret
;
bicara: djnz   Dly0,bicara
       djnz   Dly1,bicara
       djnz   Bicr,bicara
       ret
;
nama:  DB     ' Ali Rofik  '
nim:   DB     'NIM: 04.52.215'
jur:   DB     'Teknik Elektro'
univ:  DB     ' ITN Malang  '
tpmenu: DB    '>>  Menu  <<'
tmamn0: DB     ' Pengujian  '
tmamn1: DB     ' Pengaturan  '
tsbmn0: DB     ' Test Pompa  '
tsbmn1: DB     ' Test Katup  '
tsbmn2: DB     ' Test Sensor  '
tsbmn3: DB     ' Test Desibel '
tsbmn4: DB     'Batas 140 mmHg'
tsbmn5: DB     'Batas 160 mmHg'
tsbmn6: DB     'Batas 200 mmHg'
tsbmn7: DB     ' Enter = On  '
tsbmn8: DB     ' Pompa Aktif  '
tsbmn9: DB     ' Katup Buka 1  '
tsbmnA: DB     ' Katup Buka 2  '
tsbmnB: DB     ' Katup Tutup  '
stgbts: DB    'Pengaturan Batas'
tsbmnE: DB     'Start Pengukuran'
btspmp: DB    'Bts Pmp:   mmHg'
sisdia: DB    'Sistol  Diastol'
tggpas: DB    'Tekanan:   mmHg'
angka:  DB    '0123456789   '
;
;          0  1  2  3  4  5  6  7  8  9
lookup: DB     000,000,000,000,000,000,000,000,000,000          ; 000 - 009
       DB     000,000,000,000,001,001,002,002,003,004          ; 010 - 019
       DB     005,006,007,008,009,010,012,014,016,018          ; 020 - 029
       DB     020,022,024,026,028,030,031,033,035,037          ; 030 - 039
       DB     039,040,041,043,045,047,049,050,052,054          ; 040 - 049
```

```
DB    056,058,060,061,063,065,067,069,070,072          ; 050 - 059
DB    073,074,076,077,079,080,082,084,086,088          ; 060 - 069
DB    090,091,093,095,097,099,100,101,103,105          ; 070 - 079
DB    107,109,110,111,113,115,116,118,119,120          ; 080 - 089
DB    121,123,125,127,129,130,131,133,135,137          ; 090 - 099
DB    139,140,141,143,145,146,147,149,150,151          ; 100 - 109
DB    153,155,157,159,160,161,163,165,167,169          ; 110 - 119
DB    170,171,172,174,175,176,178,179,180,181          ; 120 - 129
DB    182,183,185,187,189,190,192,194,196,198          ; 130 - 139
DB    200,202,204,206,208,210,211,212,214,216          ; 140 - 149
DB    217,219,220,221,223,225,226,227,229,230          ; 150 - 159
DB    232,234,236,238,240,241,242,243,245,246          ; 160 - 169
DB    247,248,249,250,000,000,000,000,000,000          ; 170 - 179
DB    000,000,000,000,000,000,000,000,000,000          ; 180 - 189
DB    000,000,000,000,000,000,000,000,000,000          ; 190 - 199
DB    000,000,000,000,000,000,000,000,000,000          ; 200 - 209
DB    000,000,000,000,000,000,000,000,000,000          ; 210 - 219
DB    000,000,000,000,000,000,000,000,000,000          ; 220 - 229
DB    000,000,000,000,000,000,000,000,000,000          ; 230 - 239
DB    000,000,000,000,000,000,000,000,000,000          ; 240 - 249
DB    000,000,000,000,000,000                    ; 250 - 255
;
    end
```

8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

eatures

- Compatible with MCS-51® Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)

escription

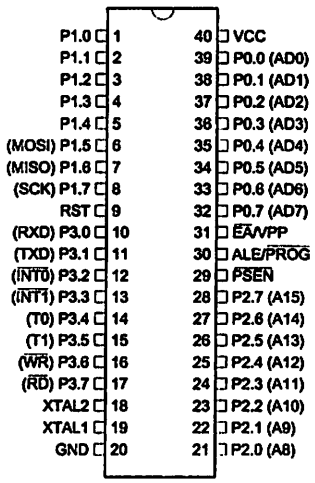
he AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K tes of in-system programmable Flash memory. The device is manufactured using mel's high-density nonvolatile memory technology and is compatible with the indus- y-standard 80C51 instruction set and pinout. The on-chip Flash allows the program emory to be reprogrammed in-system or by a conventional nonvolatile memory pro- ammer. By combining a versatile 8-bit CPU with in-system programmable Flash on a onolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a ghly-flexible and cost-effective solution to many embedded control applications.

he AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of AM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five- ector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and ock circuitry. In addition, the AT89S51 is designed with static logic for operation own to zero frequency and supports two software selectable power saving modes. he Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and terrupt system to continue functioning. The Power-down mode saves the RAM con- nts but freezes the oscillator, disabling all other chip functions until the next external terrupt or hardware reset.

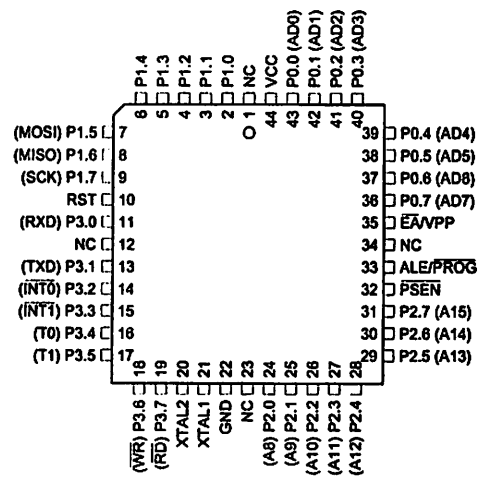
Rev. 2487A–10/01

in Configurations

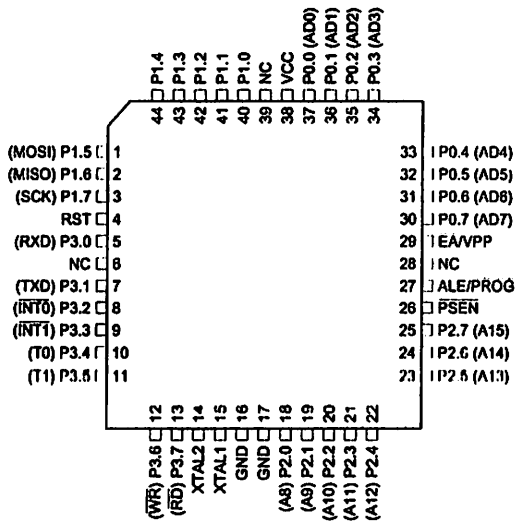
PDIP



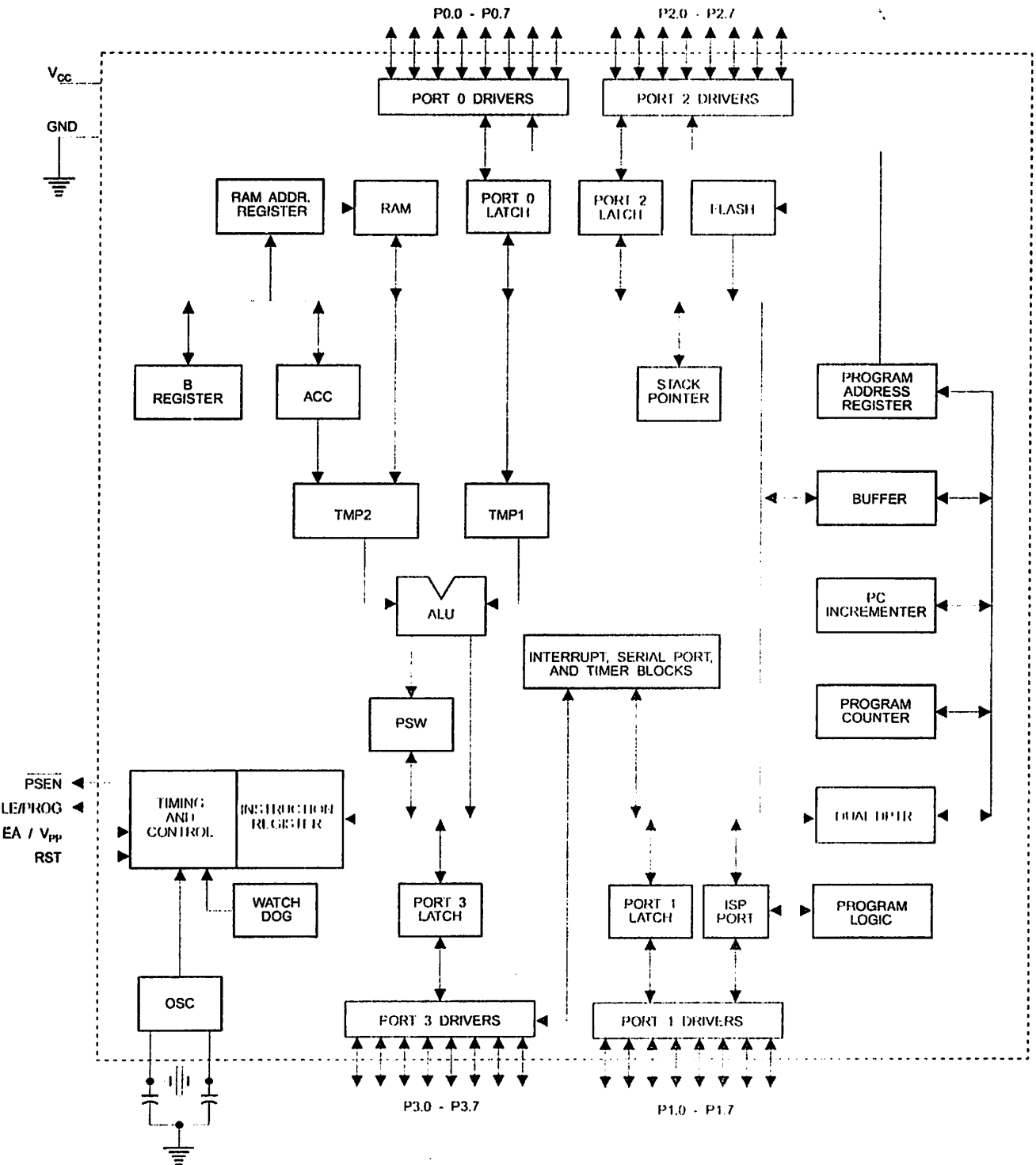
PLCC



TQFP



lock Diagram



n Description

CC Supply voltage.

ND Ground.

ort 0 Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

ort 1 Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

ort 2 Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

ort 3 Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

ST Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

LE/$\overline{PROG}$ Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{SEN}$ Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

V/VPP External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

EA should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

TAL1 Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

TAL2 Output from the inverting oscillator amplifier

pecial
unction
egisters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

ble 1. AT89S51 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H									0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DPS Data Pointer Register Select

DPS

0 Selects DPTR Registers DP0L, DP0H

1 Selects DPTR Registers DP1L, DP1H

emory rganization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

ogram Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

ıta Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

atchdog mer)ne-time ıabled with ɜset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

ɜing the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

/DT During ower-down nd Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

ART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

mer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

terrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

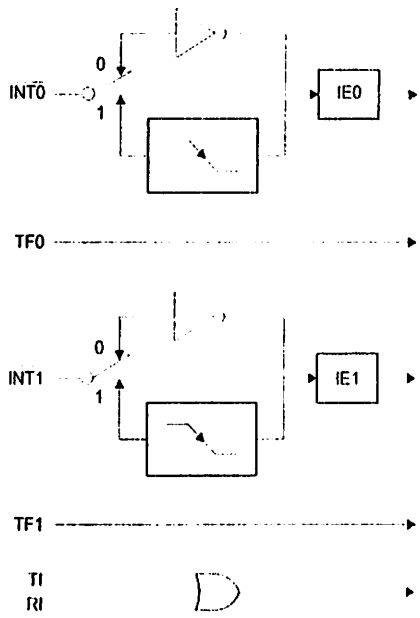
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

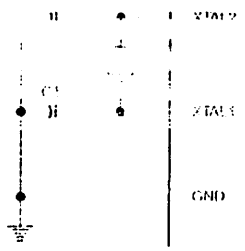
Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

Figure 1. Interrupt Sources



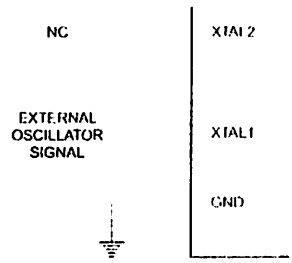
scillator haracteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.



Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



le Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated either by a hardware reset or by activation of an enabled external interrupt into INT0 or INT1. Exit from Power-down by either reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

rogram emory Lock its

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

rogramming e Flash – rallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte by byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89S51 features Data Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

rogramming
e Flash –
erial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

rial
ogramming
gorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

erial ogramming struction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

rogramming terface – arallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

ble 7. Flash Programming Modes

ode	V_{CC}	RST	PSEN	ALE/ PROG	EA/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
rite Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
ead Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
rite Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
rite Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
rite Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
ead Lock Bits 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
hip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
ead Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
ead Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
ead Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

es:
1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/BSY signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

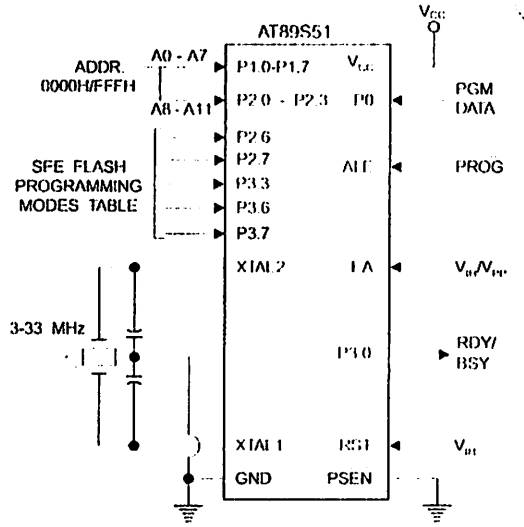
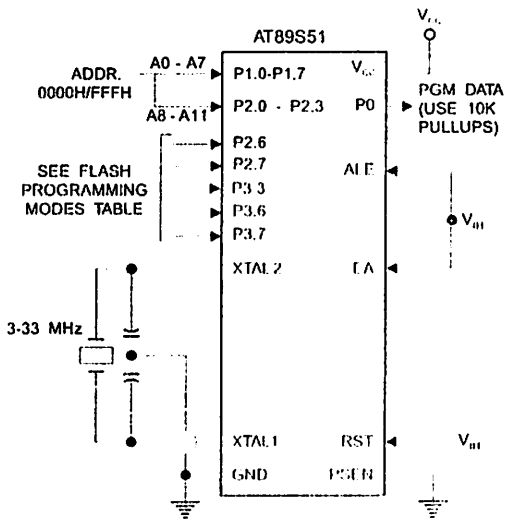


Figure 5. Verifying the Flash Memory (Parallel Mode)

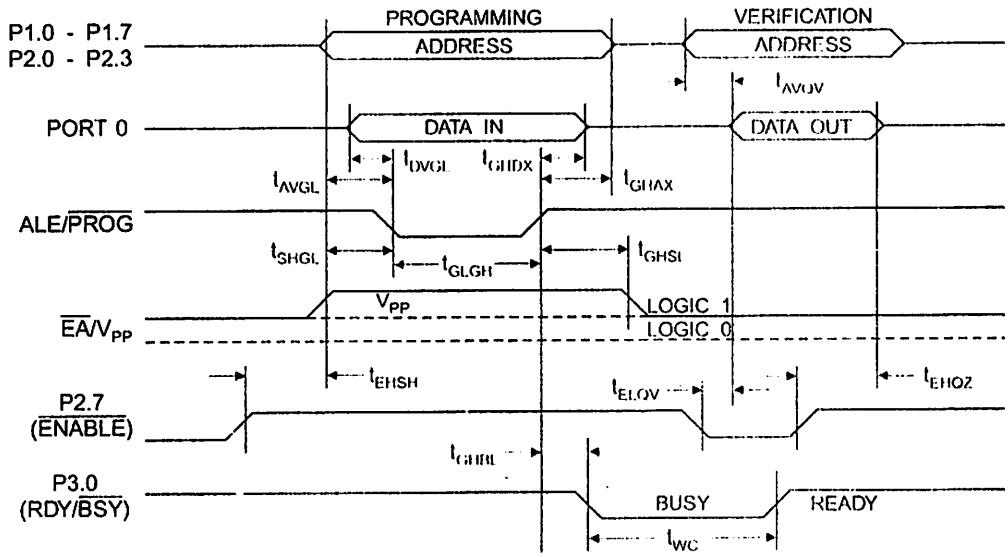


ash Programming and Verification Characteristics (Parallel Mode)

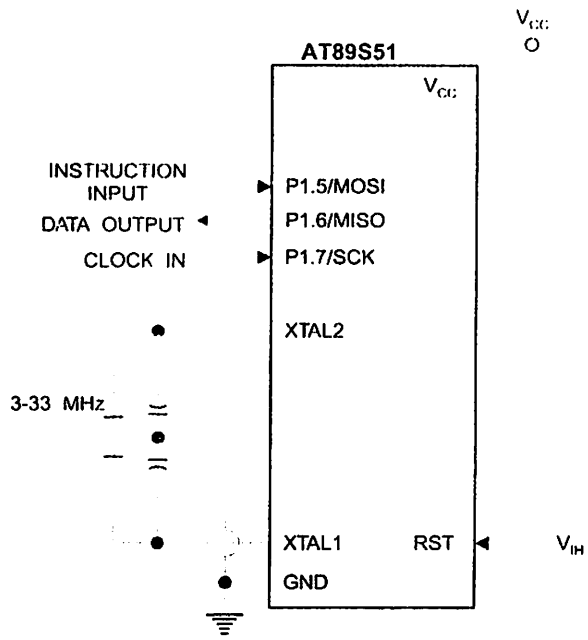
= 20°C to 30°C, V_{CC} = 4.5 to 5.5V

ymbol	Parameter	Min	Max	Units
PP	Programming Supply Voltage	11.5	12.5	V
P	Programming Supply Current		10	mA
C	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
VGL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
HAX	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
VGL	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
HDX	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
HSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
HGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
HSL	V_{PP} Hold After $\overline{PROG}$	10		µs
LGH	$\overline{PROG}$ Width	0.2	1	µs
VQV	Address to Data Valid		$48t_{CLCL}$	
LQV	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
HQZ	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
HBL	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
C	Byte Write Cycle Time		50	µs

jure 6. Flash Programming and Verification Waveforms – Parallel Mode

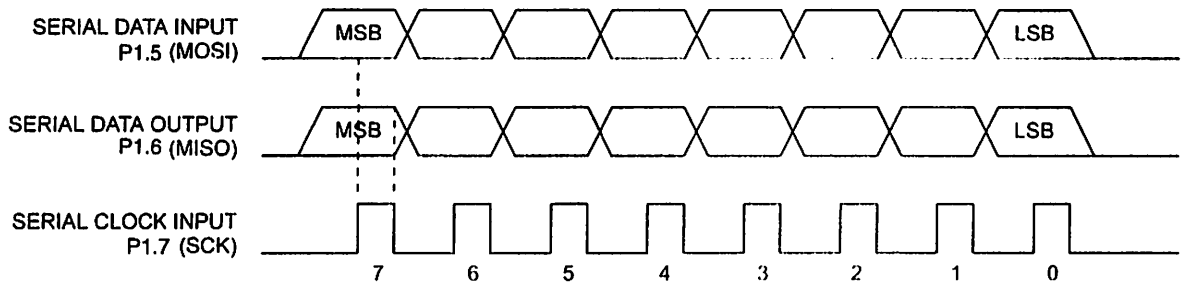


igure 7. Flash Memory Serial Downloading



lash Programming and Verification Waveforms – Serial Mode

gure 8. Serial Programming Waveforms



ıble 8. Serial Programming Instruction Set

nstruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory Byte Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Write Program Memory Byte Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Write Lock Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Read Signature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
Read Program Memory Page Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory Page Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

ıtes: 1. The signature bytes are not readable in Lock Bit Modes 3 and 4.

2. B1 = 0, B2 = 0 → Mode 1, no lock protection
   B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 → Mode 4, lock bit 3 activated

   } Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Serial Programming Characteristics

Figure 9. Serial Programming Timing

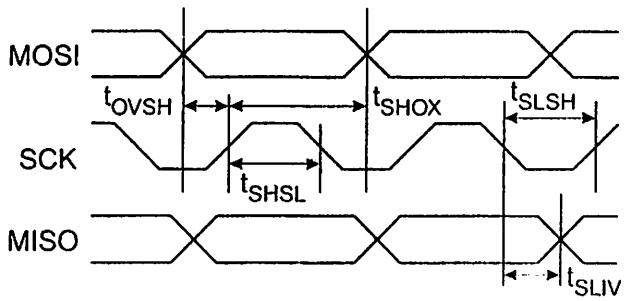


Table 9. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	8 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	8 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

bsolute Maximum Ratings*

)perating Temperature	-55°C to +125°C
;torage Temperature	-65°C to +150°C
'oltage on Any Pin ;ith Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
)C Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C Characteristics

e values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

ymbol	Parameter	Condition	Min	Max	Units
IL	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
IL1	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
IH	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
IH1	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
OL	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
OL1	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
OH	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
OH1	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
L	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-650	µA
I	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RST	Reset Pulldown Resistor		50	300	KΩ
IO	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
C	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

es: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

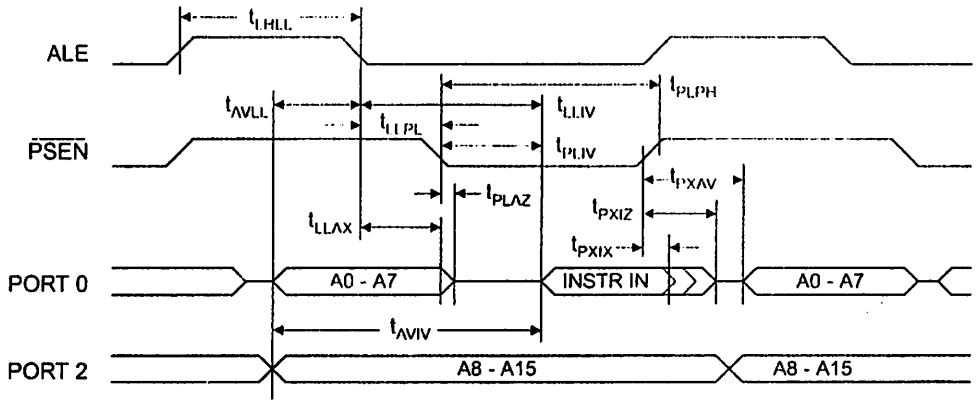
C Characteristics

der operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other tputs = 80 pF.

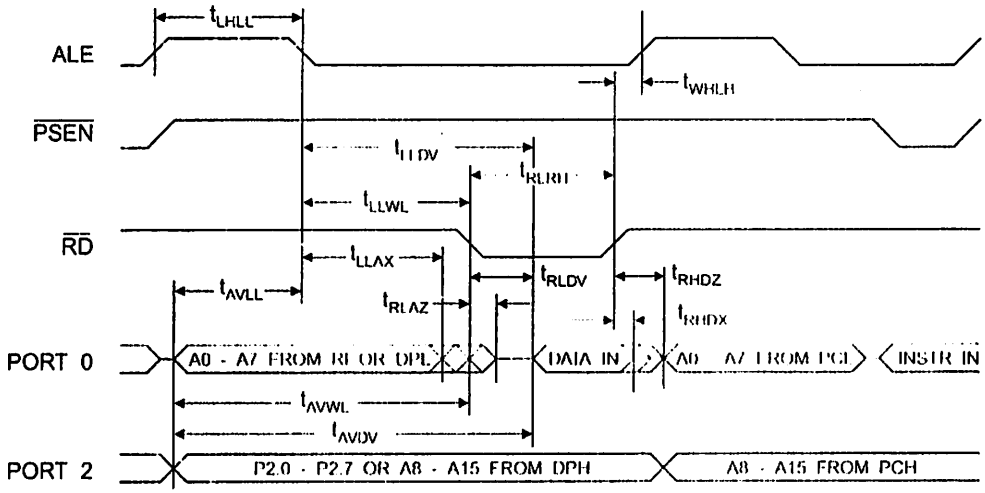
kternal Program and Data Memory Characteristics

ymbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{CLCL}	Oscillator Frequency			0	33	MHz
HLL	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
VLL	Address Valid to ALE Low	43		t_{CLCL}-25		ns
LAX	Address Hold After ALE Low	48		t_{CLCL}-25		ns
LIV	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
LPL	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
LPH	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
LIV	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
XIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
XIZ	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
XAV	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
AIV	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
LAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
LRH	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
LWH	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
LDV	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
HDX	Data Hold After $\overline{RD}$	0		0		ns
HDZ	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
LDV	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
ADV	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
LWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
AWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
QWX	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
QWH	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
WHQX	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
RLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
WHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

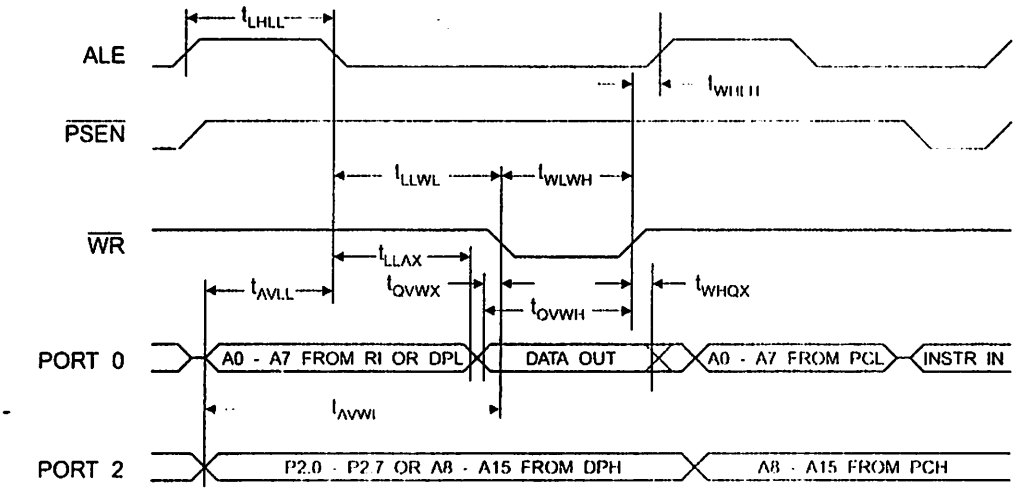
xternal Program Memory Read Cycle



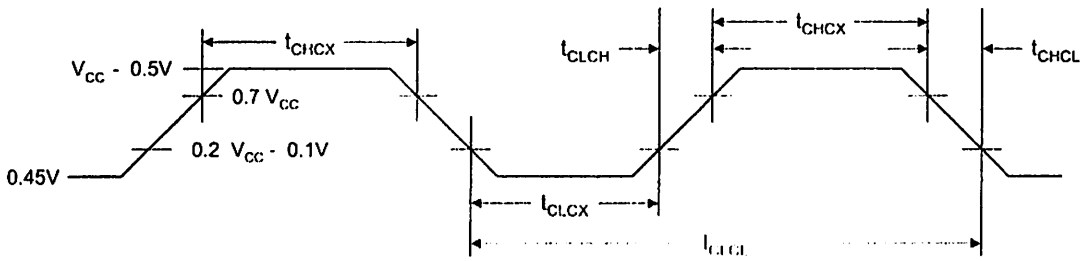
xternal Data Memory Read Cycle



xternal Data Memory Write Cycle



xternal Clock Drive Waveforms



xternal Clock Drive

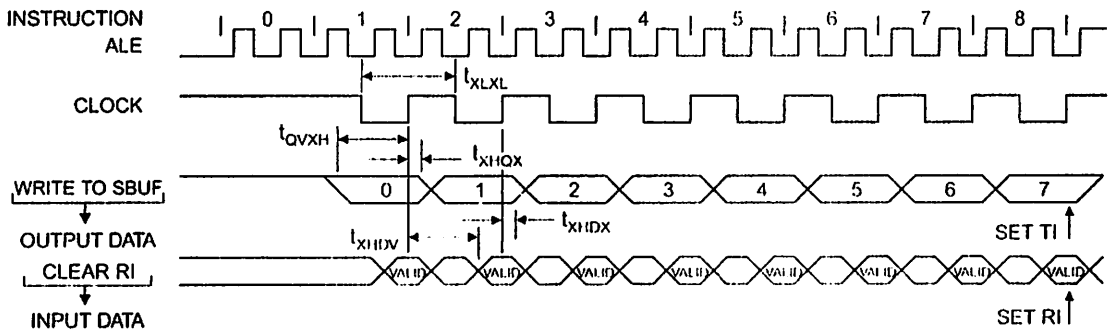
ymbol	Parameter	Min	Max	Units
$/t_{CLCL}$	Oscillator Frequency	0	33	MHz
:LCL	Clock Period	30		ns
:HCX	High Time	12		ns
:LCX	Low Time	12		ns
:LCH	Rise Time		5	ns
:HCL	Fall Time		5	ns

erial Port Timing: Shift Register Mode Test Conditions

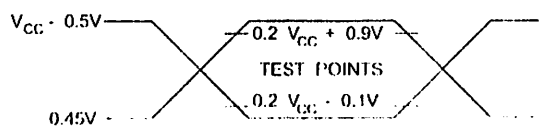
e values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

ymbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
LXL	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
VXH	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
HQX	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
HDX	Input Data Hold After Clock Rising Edge	0		0		ns
HDV	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

hift Register Mode Timing Waveforms

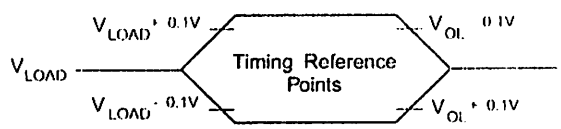


C Testing Input/Output Waveforms[1]



te: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

oat Waveforms[1]



te: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

rdering Information

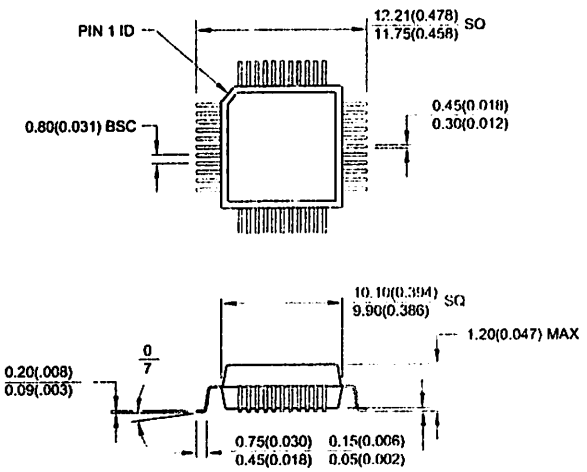
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC	44A 44J 40P6	Commercial (0° C to 70° C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI	44A 44J 40P6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC	44A 44J 40P6	Commercial (0° C to 70° C)

= Preliminary Availability

	Package Type
4A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
4J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
0P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

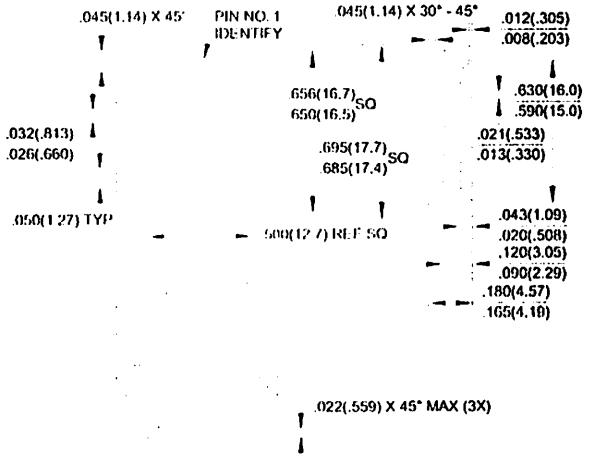
ıckaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*

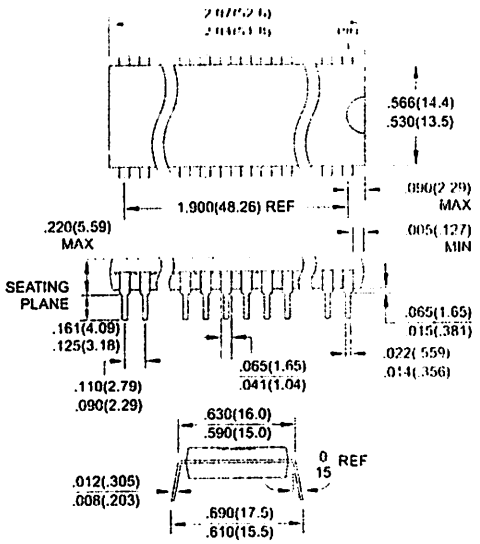


***Controlling dimension: millimeters**

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



40P6, 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC



Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Product Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-7658-3000
FAX (33) 4-7658-3480

Atmel Heilbronn
Theresienstrasse 2
POB 3535
D-74025 Heilbronn, Germany
TEL (49) 71 31 67 25 94
FAX (49) 71 31 67 24 23

Atmel Nantes
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 0 2 40 18 18 18
FAX (33) 0 2 40 18 19 60

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-357-000
FAX (44) 1355-242-743

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

2487A–10/01/xM

National Semiconductor

December 1994

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

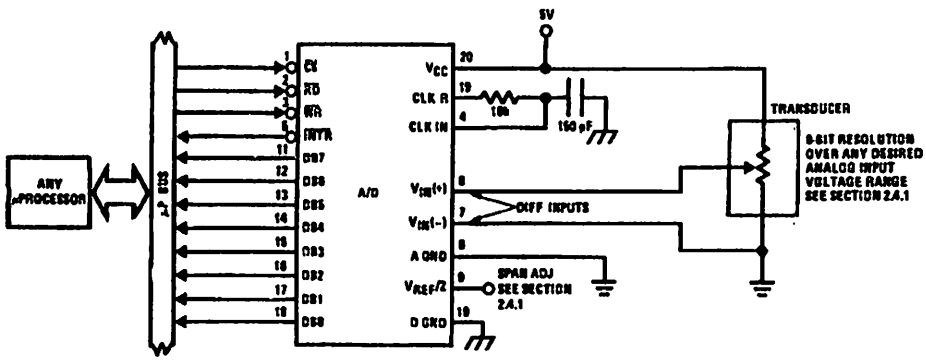
Features

- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

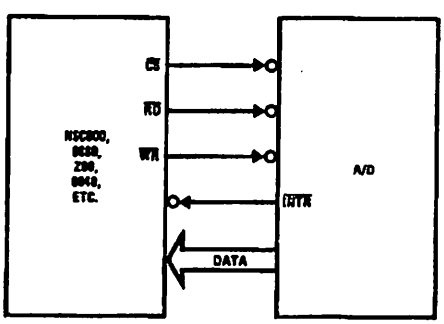
- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 μs

Typical Applications



TL/H/5671–1

8080 Interface



TL/H/5671–31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

TRI-STATE® is a registered trademark of National Semiconductor Corp.
Z-80® is a registered trademark of Zilog Corp.

  RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ, ADC0802LJ/883	$-55°C \le T_A \le +125°C$
ADC0801/02/03/04LCJ	$-40°C \le T_A \le +85°C$
ADC0801/02/03/05LCN	$-40°C \le T_A \le +85°C$
ADC0804LCN	$0°C \le T_A \le +70°C$
ADC0802/03/04LCV	$0°C \le T_A \le +70°C$
ADC0802/03/04LCWM	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			±1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC} = 5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}

AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = 5V_{DC}$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V_{CC} = 4.75\ V_{DC}$			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	$V_{IN} = 5\ V_{DC}$		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	$V_{IN} = 0\ V_{DC}$	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	$I_O = 360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	$I_O = -360\ \mu A$ $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 $I_{OUT} = 1.6$ mA, $V_{CC} = 4.75\ V_{DC}$ $I_{OUT} = 1.0$ mA, $V_{CC} = 4.75\ V_{DC}$			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	$I_O = -360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	$I_O = -10\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT} = 0\ V_{DC}$ $V_{OUT} = 5\ V_{DC}$	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, $T_A = 25°C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, $T_A = 25°C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	$f_{CLK} = 640$ kHz, $V_{REF}/2 =$ NC, $T_A = 25°C$ and $\overline{CS} = 5V$		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at $f_{CLK} = 640$ kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

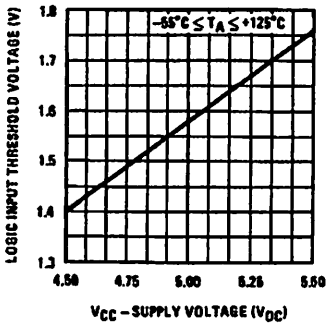
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

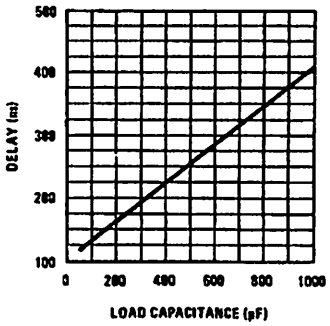
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

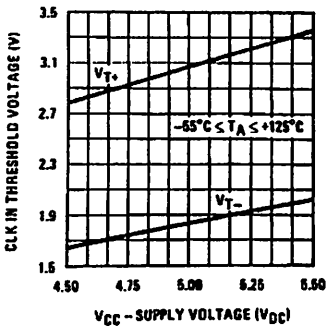
Logic Input Threshold Voltage vs. Supply Voltage



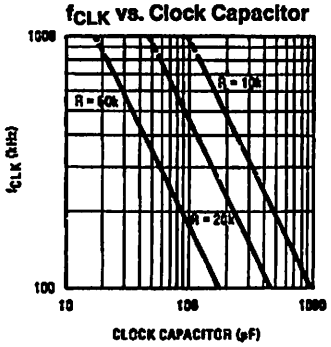
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



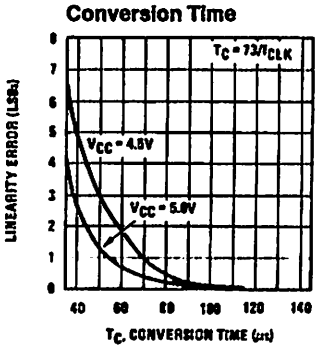
CLK IN Schmitt Trip Levels vs. Supply Voltage



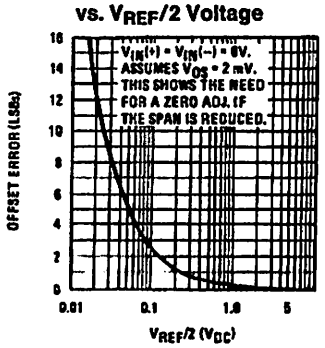
f_{CLK} vs. Clock Capacitor



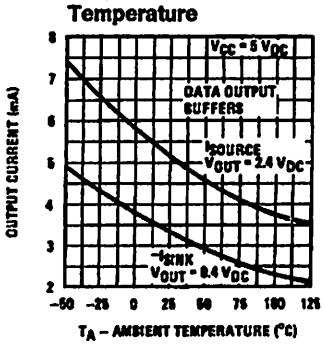
Full-Scale Error vs Conversion Time



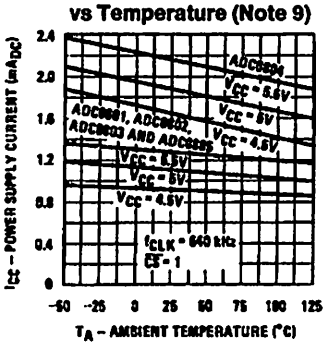
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



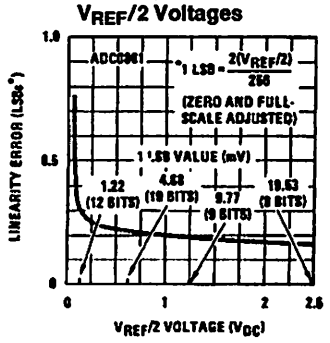
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)

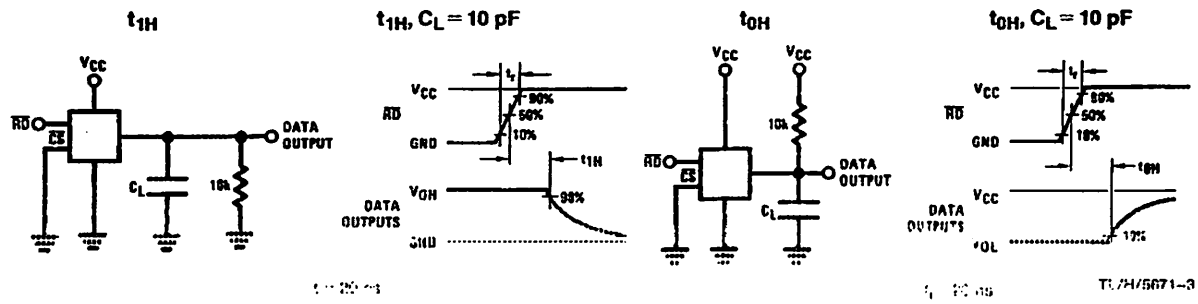


Linearity Error at Low $V_{REF}/2$ Voltages

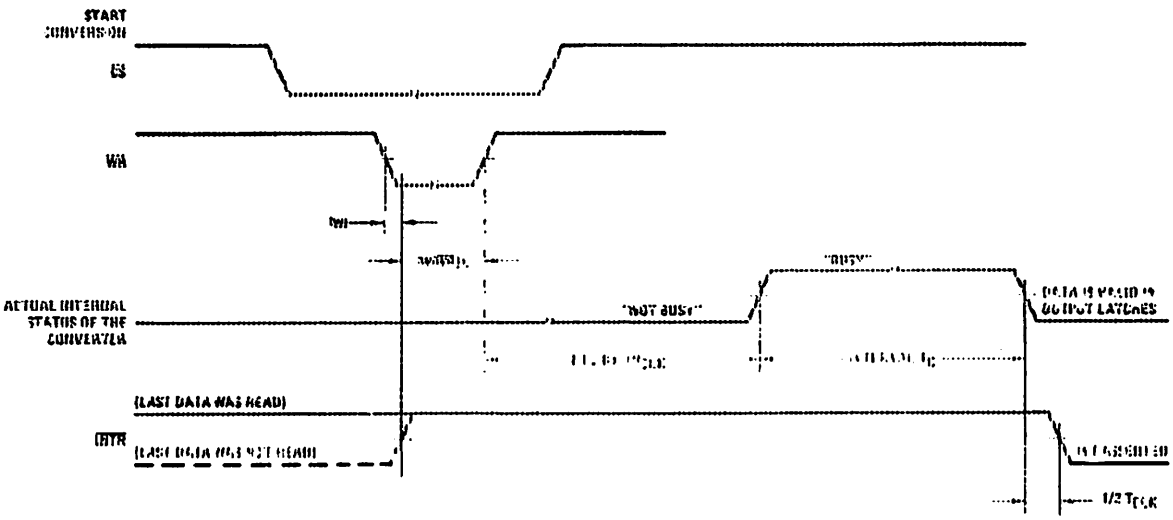


TL/H/5671–2

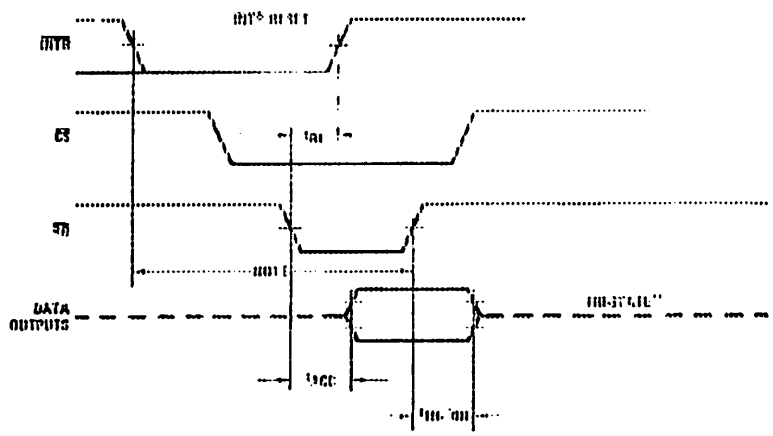
TRI-STATE Test Circuits and Waveforms



Timing Diagrams (All timing is measured from the 50% voltage points)



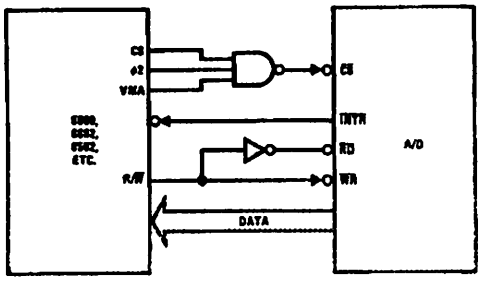
Output Enable and Reset INTR



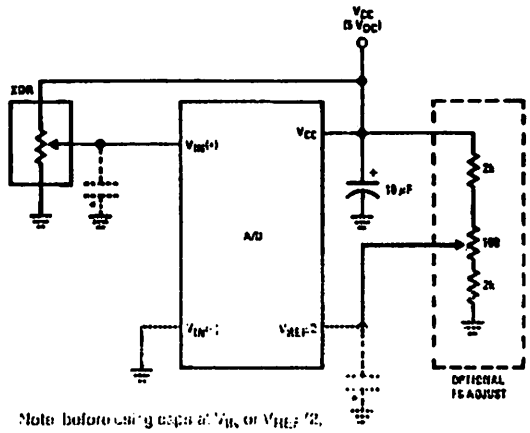
Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of INTR.

Typical Applications (Continued)

6800 Interface

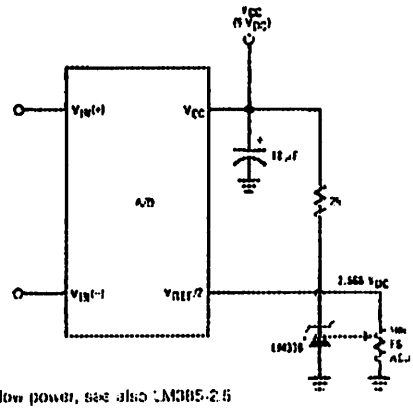


Ratiometric with Full-Scale Adjust



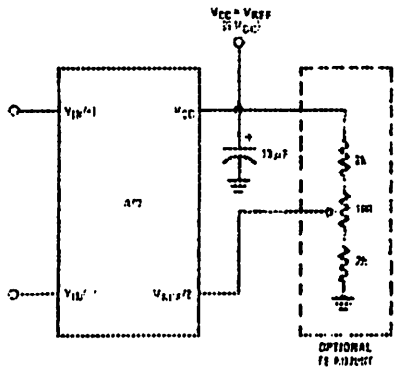
Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

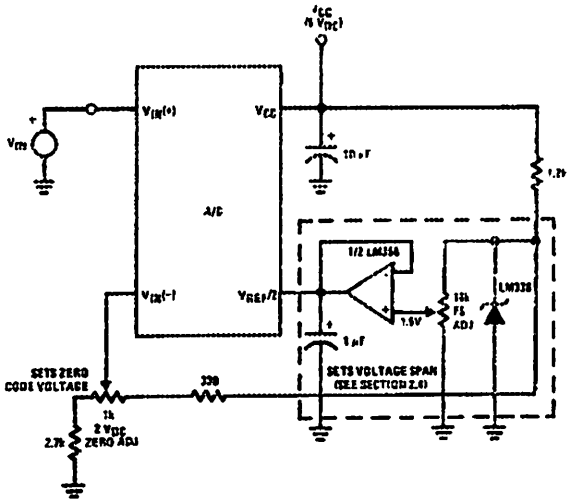


*For low power, see also LM385-2.5

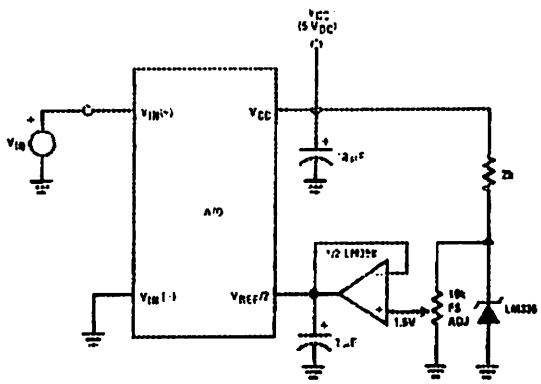
Absolute with a 5V Reference



Zero-Shift and Span Adjust: 2V < V_{IN} < 5V



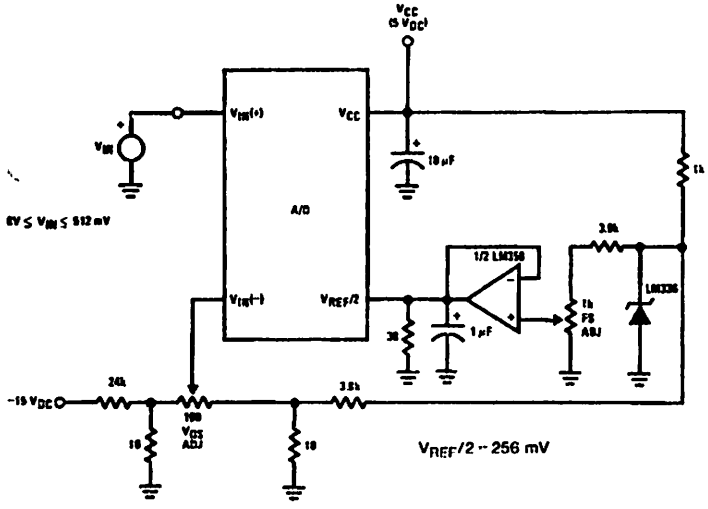
Span Adjust: 0V < V_{IN} < 3V



TL/H/5671–5

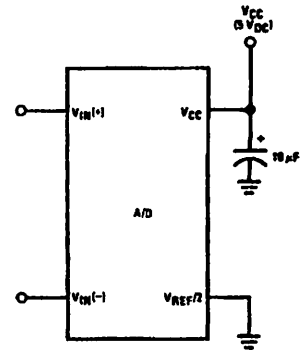
Typical Applications (Continued)

Directly Converting a Low-Level Signal



$V_{REF}/2 = 256$ mV

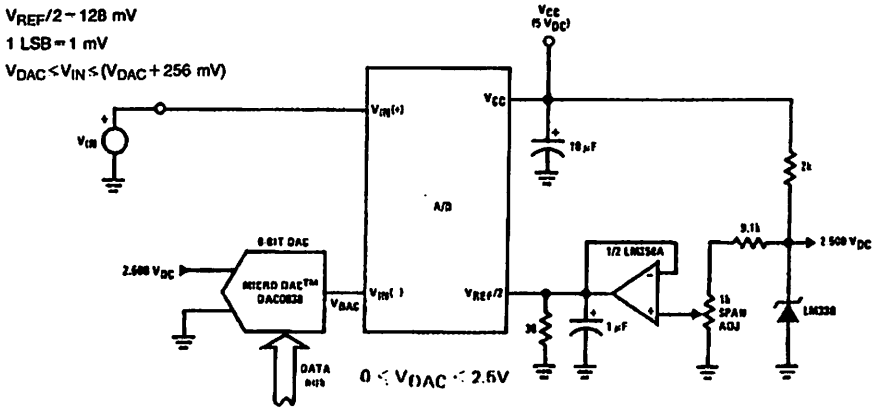
A µP Interfaced Comparator



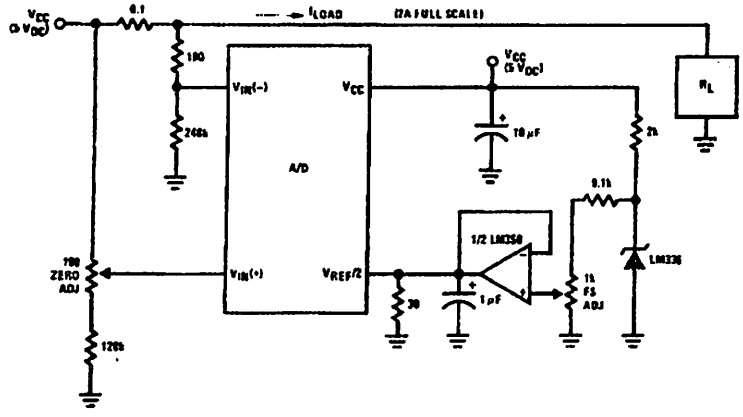
For: $V_{IN}(+) > V_{IN}(-)$
Output = FF_{HEX}
For: $V_{IN}(+) < V_{IN}(-)$
Output = 00_{HEX}

1 mV Resolution with µP Controlled Range

$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC} + 256$ mV)



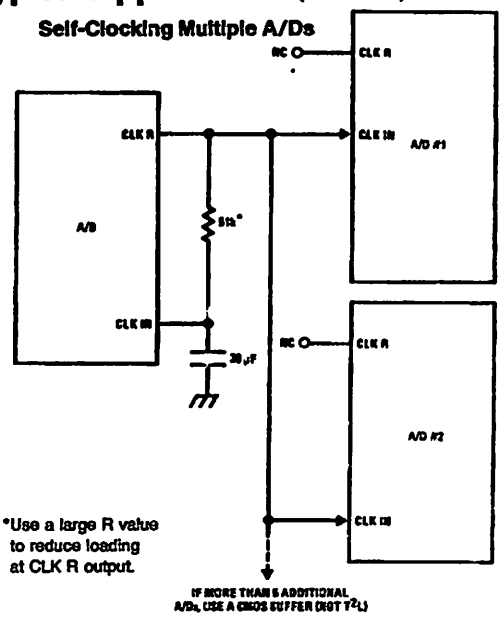
Digitizing a Current Flow



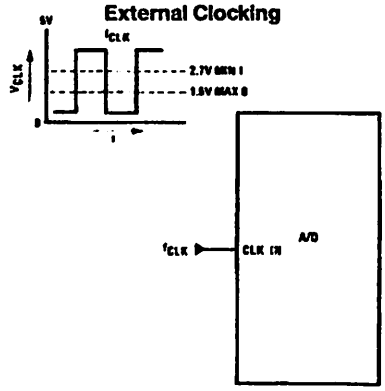
TL/H/5671–6

Typical Applications (Continued)

Self-Clocking Multiple A/Ds

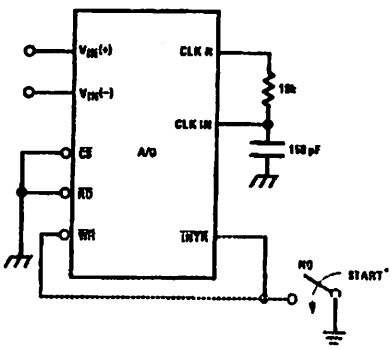


External Clocking



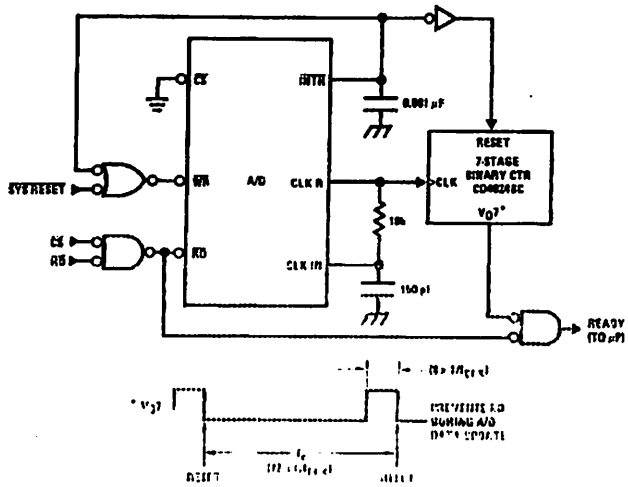
100 kHz ≤ f_{CLK} ≤ 1460 kHz

Self-Clocking in Free-Running Mode

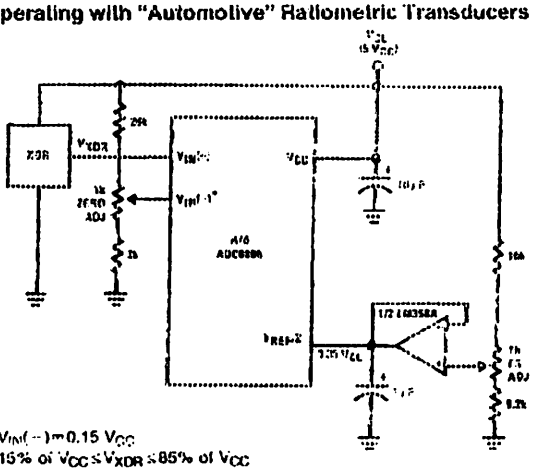


*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

μP Interface for Free-Running A/D

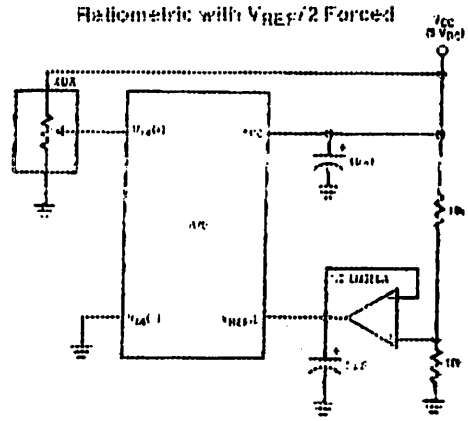


Operating with "Automotive" Ratiometric Transducers



*$V_{IN}(-)$ = 0.15 V_{CC}
15% of V_{CC} ≤ V_{XDR} ≤ 85% of V_{CC}

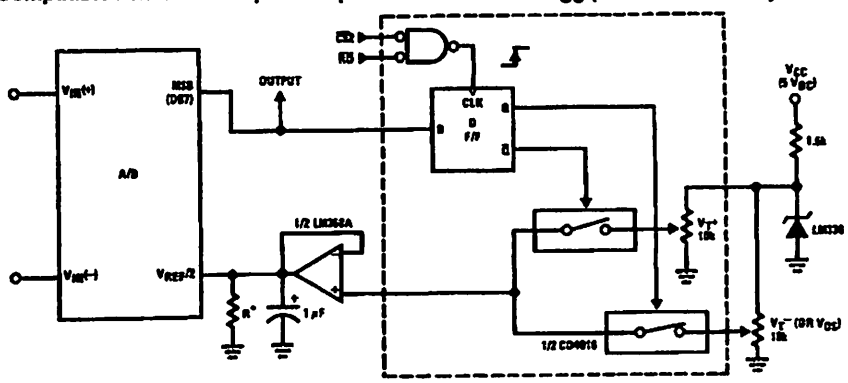
Ratiometric with $V_{REF}/2$ Forced



TL/H/5671–7

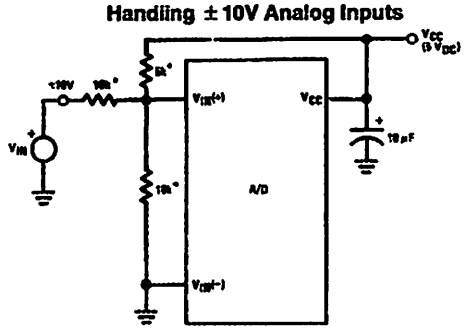
Typical Applications (Continued)

μP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)



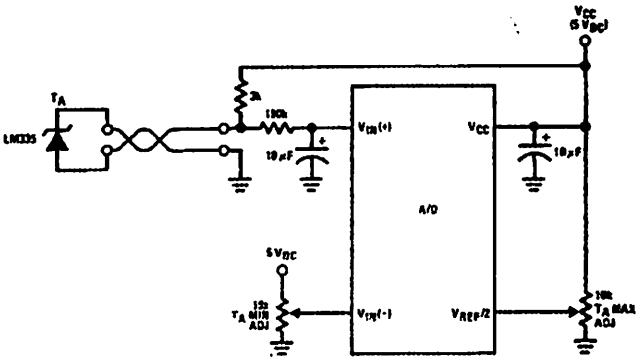
*See *Figure 5* to select R value
DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

Handling ±10V Analog Inputs

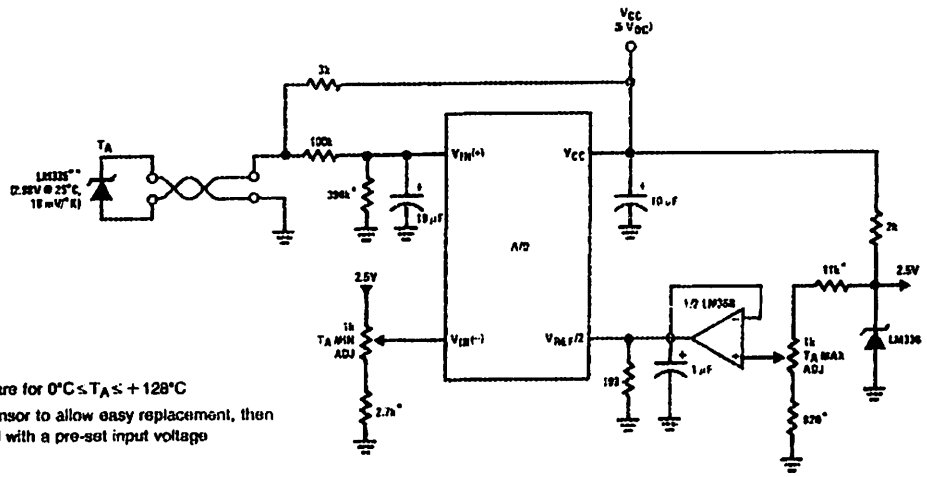


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, μP Interfaced, Temperature-to-Digital Converter



μP Interfaced Temperature-to-Digital Converter

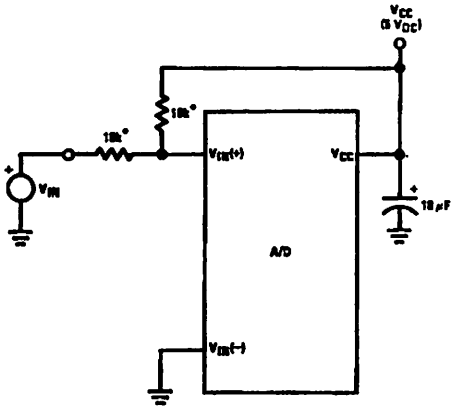


*Circuit values shown are for $0°C \leq T_A \leq +128°C$
**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage

TL/H/5671–8

Typical Applications (Continued)

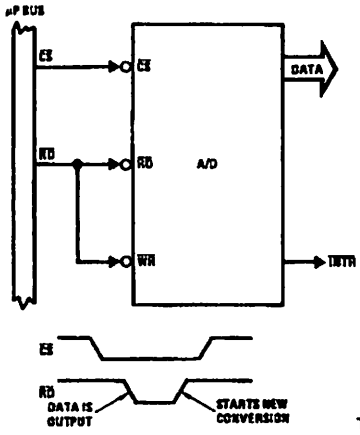
Handling ±5V Analog Inputs



TL/H/5671–33

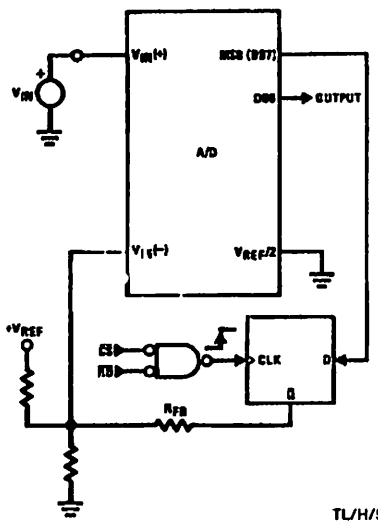
*Beckman Instruments #694-3-R10K resistor array

Read-Only Interface



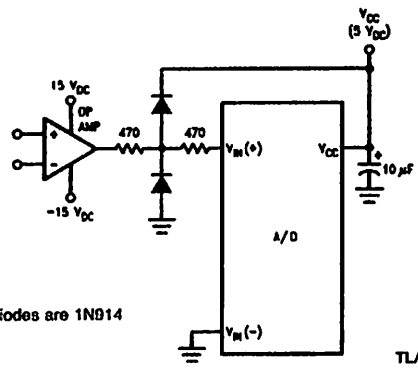
TL/H/5671–34

µP Interfaced Comparator with Hysteresis



TL/H/5671–35

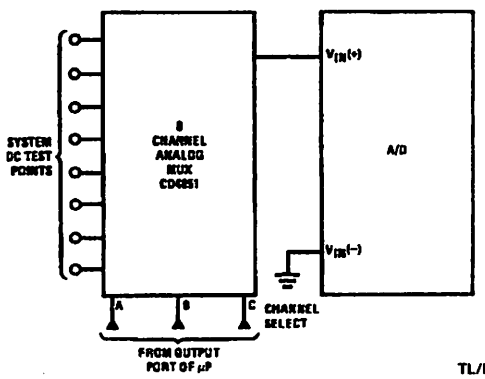
Protecting the Input



Diodes are 1N914

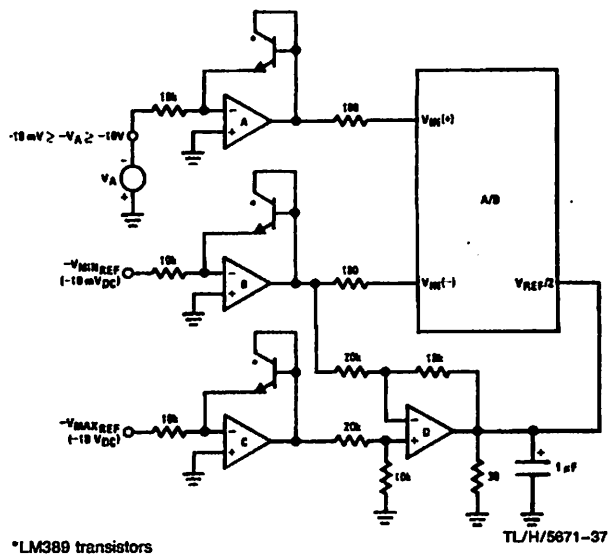
TL/H/5671–9

Analog Self-Test for a System



TL/H/5671–38

A Low-Cost, 3-Decade Logarithmic Converter



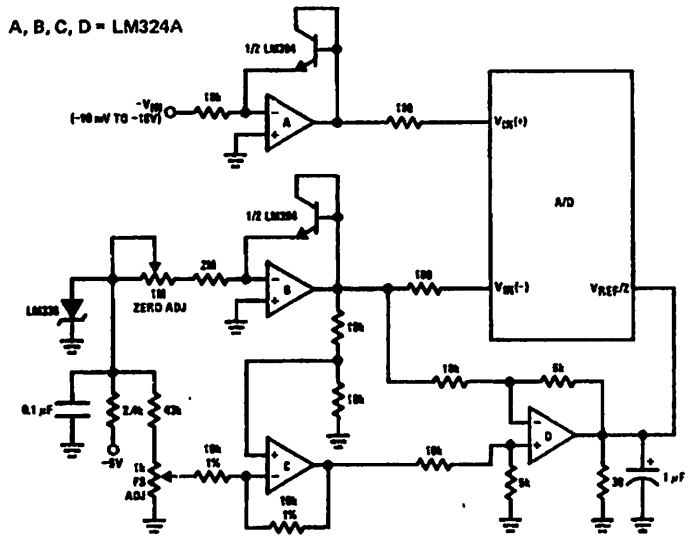
TL/H/5671–37

*LM389 transistors

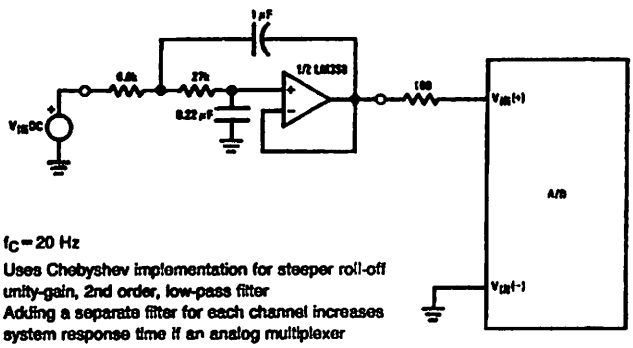
A, B, C, D = LM324A quad op amp

Typical Applications (Continued)

3-Decade Logarithmic A/D Converter



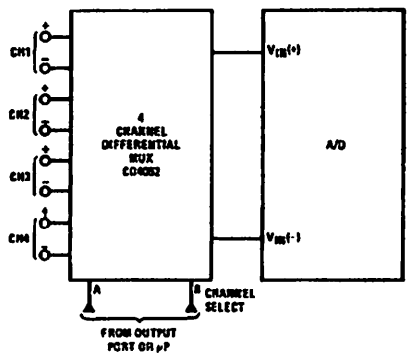
Noise Filtering the Analog Input



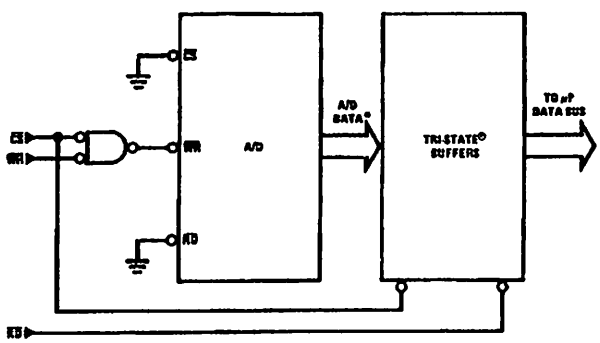
$f_C = 20$ Hz

Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

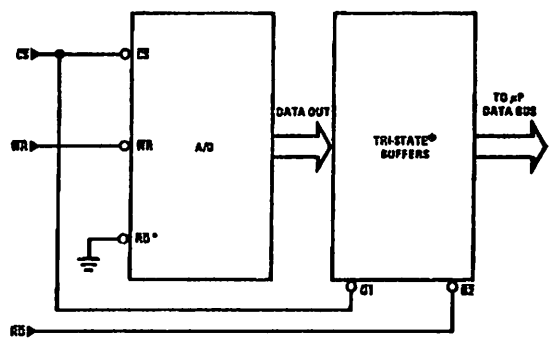


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

Increasing Bus Drive and/or Reducing Time on Bus

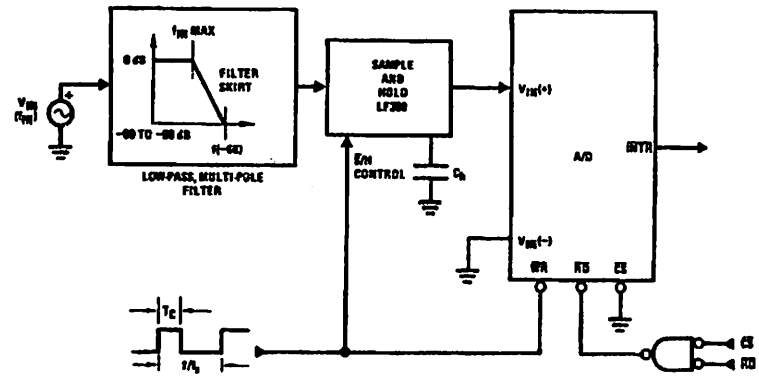


TL/H/5671–10

*Allows output data to set-up at falling edge of $\overline{CS}$

Typical Applications (Continued)

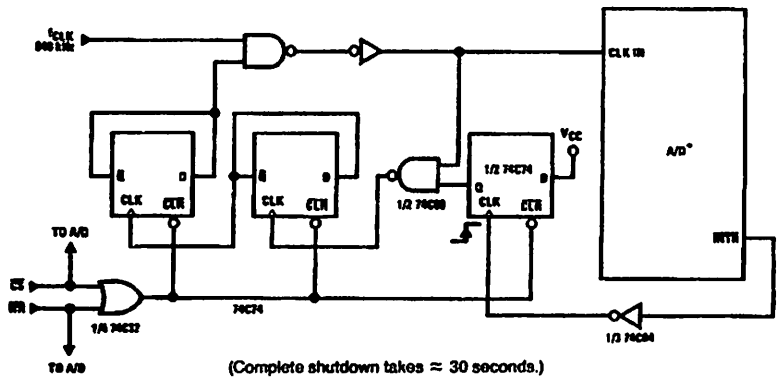
Sampling an AC Input Signal



Note 1: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

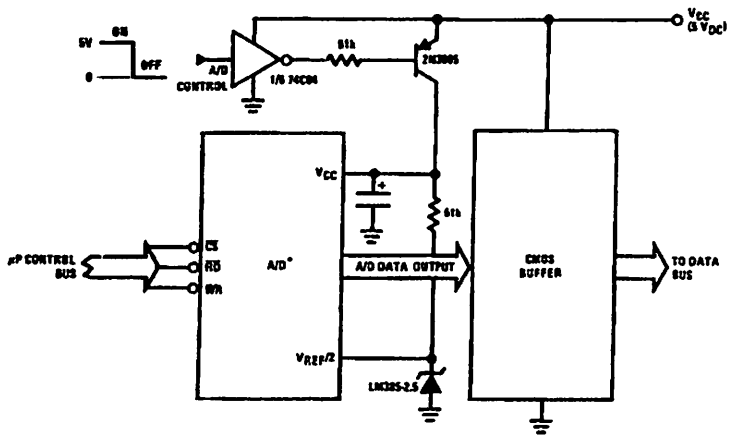
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



TL/H/5671–11

*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

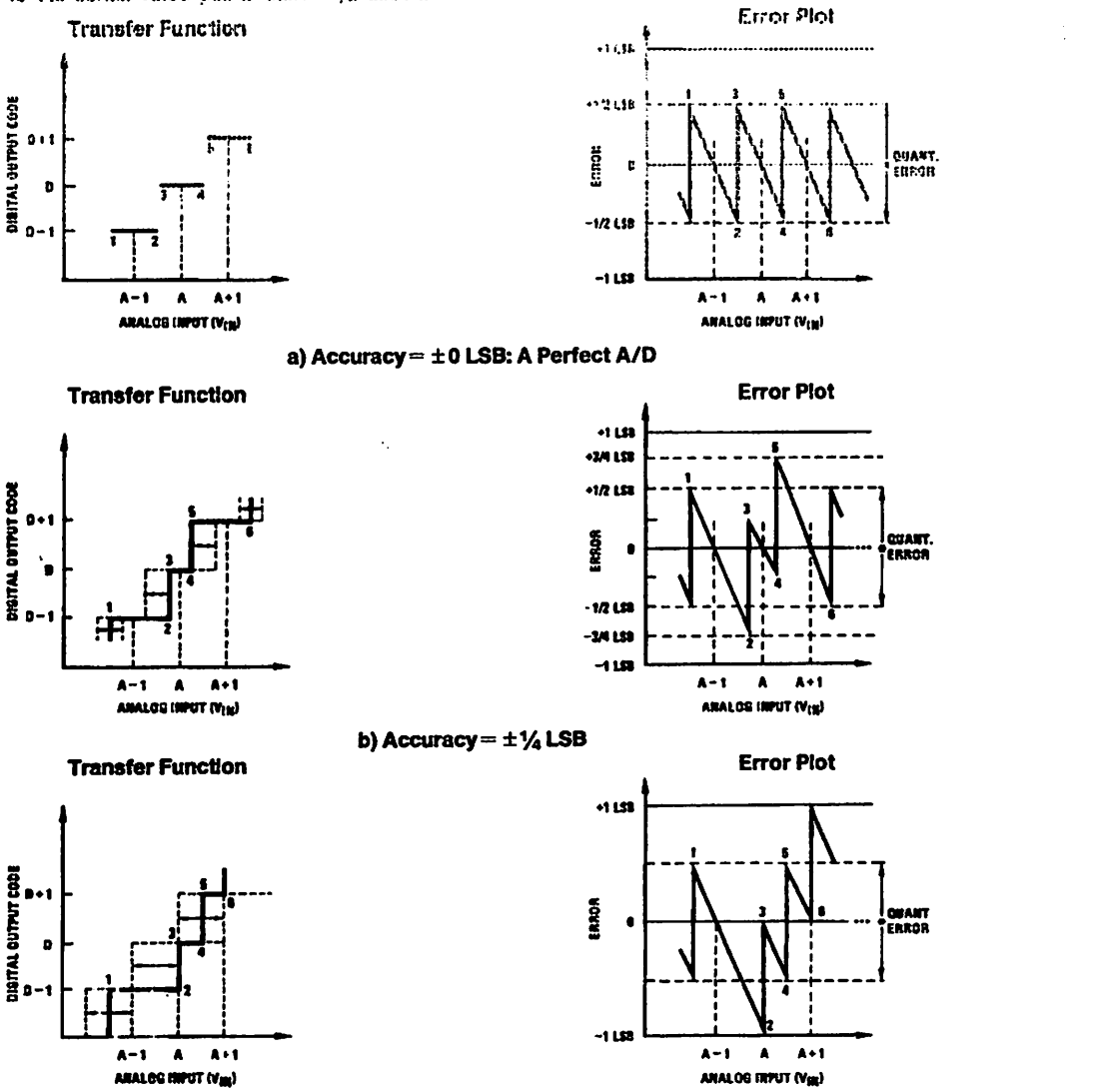
1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D − 1, D, and D + 1. For the perfect A/D, not only will center-value (A − 1, A, A + 1, ...) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ± ½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend ± ½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Figure 1b shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ± ¼ LSB. In other words, if we apply an analog input equal to the center-value ± ¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is + ½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.



TL/H/5671–12

FIGURE 1. Clarifying the Error Specs of an A/D Converter

Functional Description

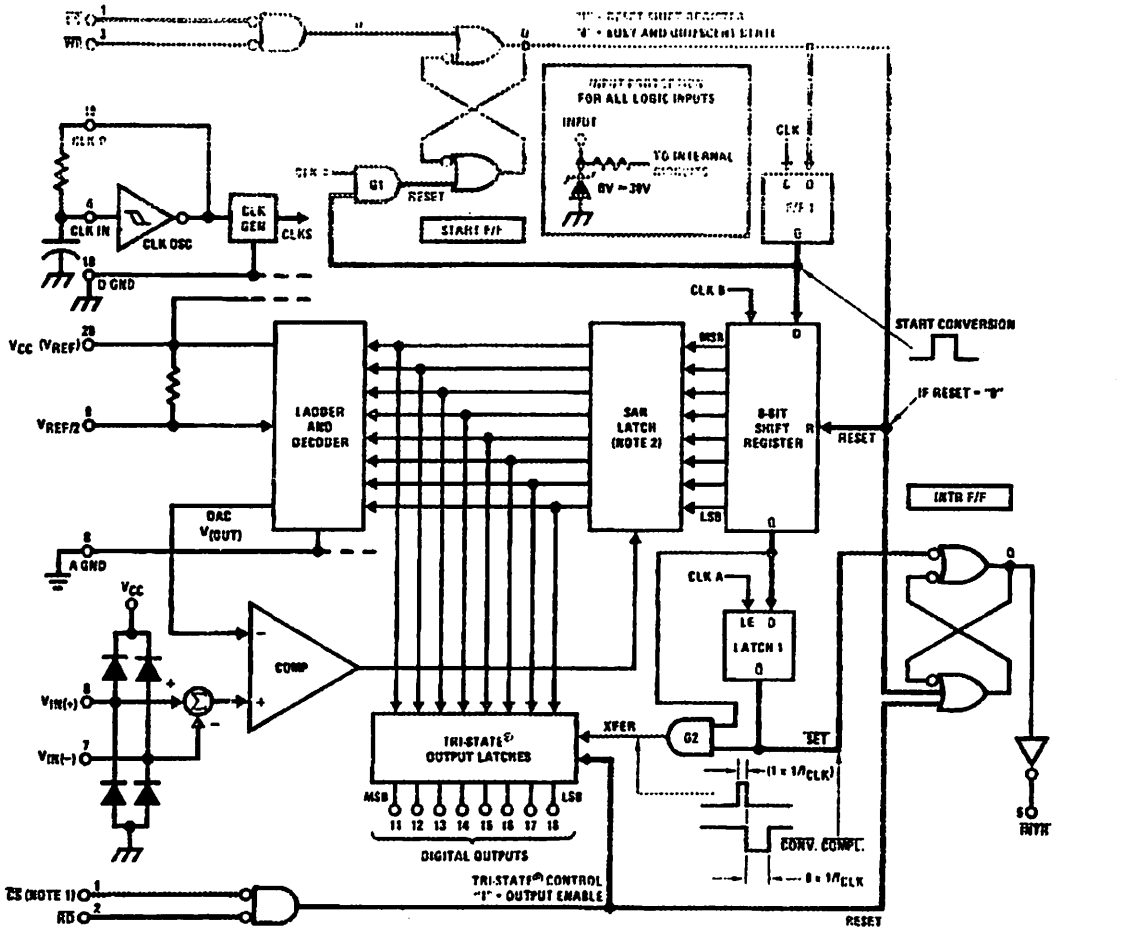
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS} = 0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 2*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having CS and WR simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.



Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register

FIGURE 2. Block Diagram

Functional Description (Continued)

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.6), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the Q output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T²L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^{3})}{(6.28)(60)(4.5)}$$

which gives

$V_P \cong 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

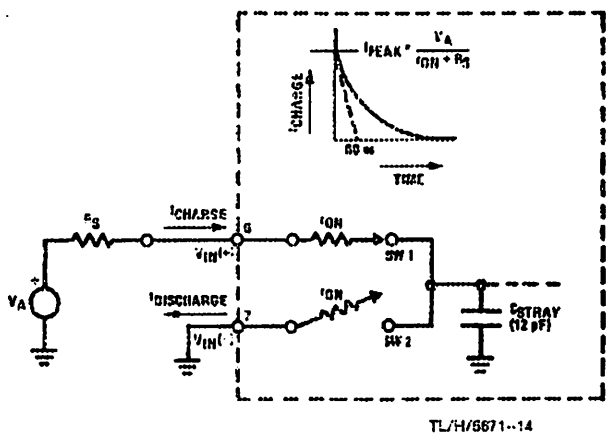
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



TL/H/5671–14

r_{ON} of SW 1 and SW 2 = 5 kΩ

$\tau = r_{ON} C_{STRAY} = 5\ k\Omega \times 12\ pF = 60\ ns$

FIGURE 3. Analog Input Impedance

Functional Description (Continued)

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of $V_{CC}+50$ mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

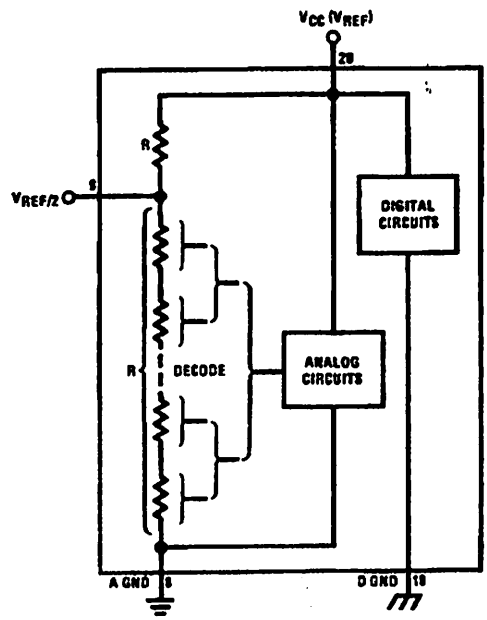
2.3.4 Noise

The leads to the analog inputs (pin 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.

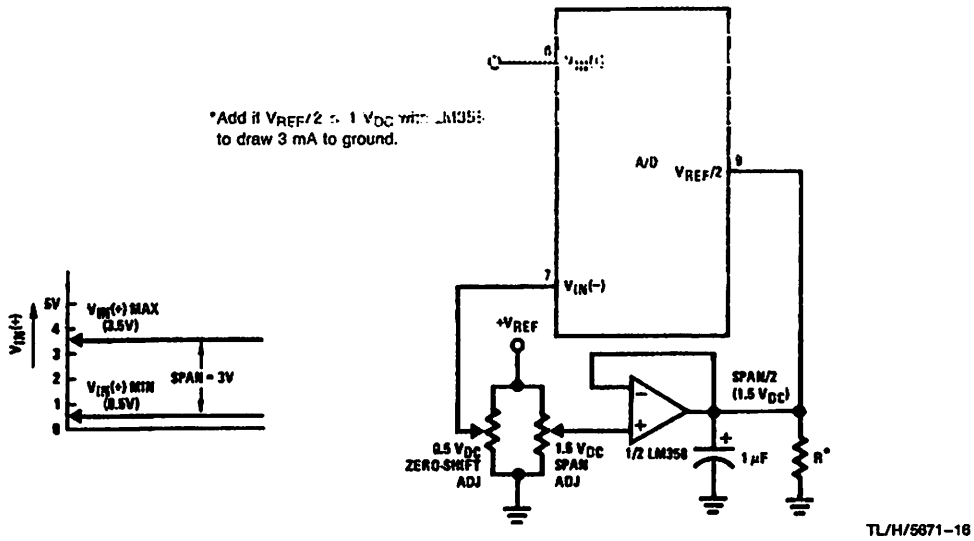


TL/H/5671–15

FIGURE 4. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.



a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5V (Digital Out = =00_{HEX}) to 3.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of +10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} ( ) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

Functional Description (Continued)

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+) \text{ fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = The high end of the analog input range

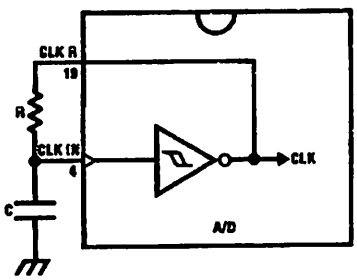
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6*.



$$f_{CLK} \cong \frac{1}{1.1\,RC}$$

$$R \cong 10\ k\Omega$$

TL/H/5671–17

FIGURE 6. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

Functional Description (Continued)

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

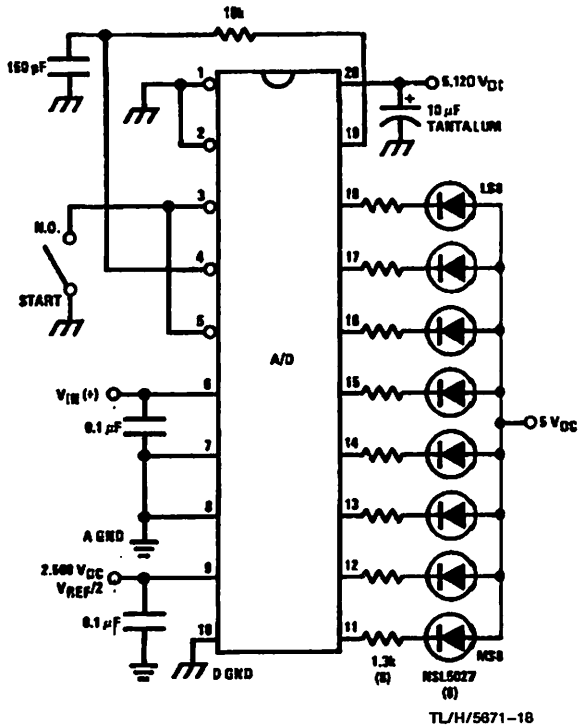
3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120−1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in Table I, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.



TL/H/5671–18

FIGURE 7. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A−C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10*.

Functional Description (Continued)

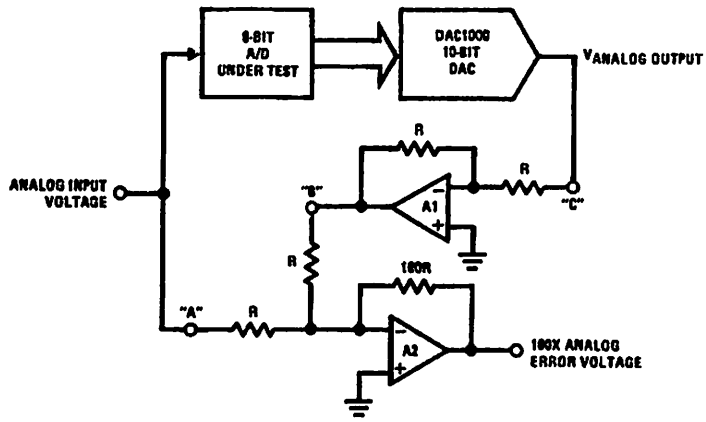
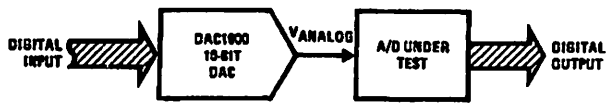


FIGURE 8. A/D Tester with Analog Error Output



TL/H/5671–19

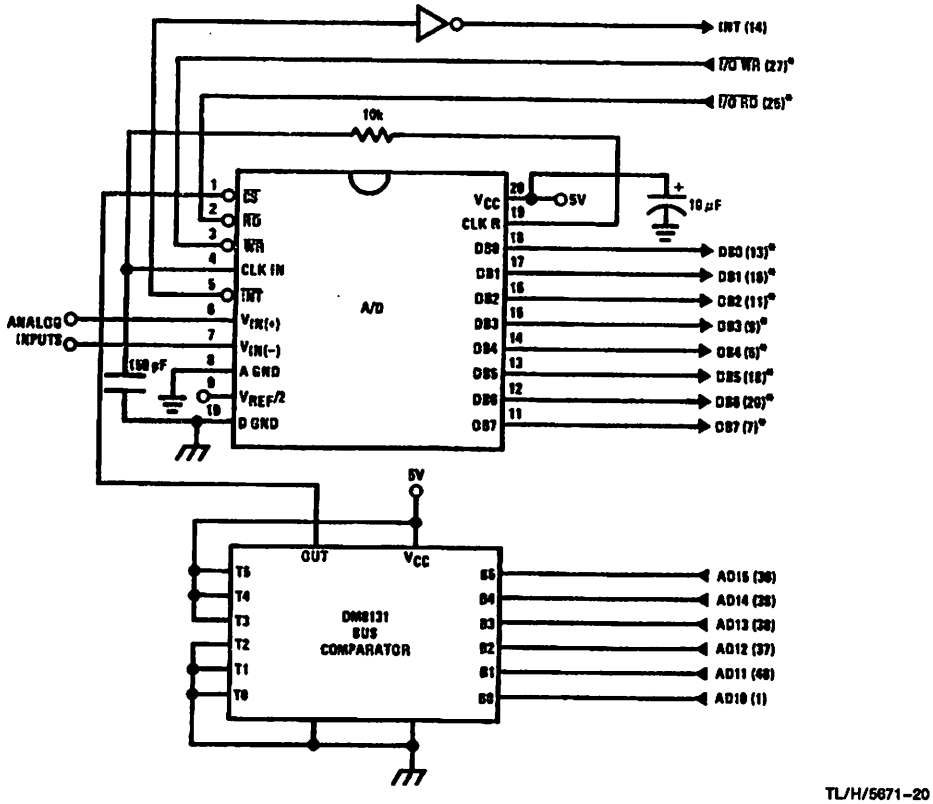
FIGURE 9. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

EX	BINARY				FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$	
					MS GROUP	LS GROUP	VMS GROUP*	VLS GROUP*
F	1	1	1	1	15/16	15/256	4.800	0.300
E	1	1	1	0	7/8	7/128	4.480	0.280
D	1	1	0	1	13/16	13/256	4.160	0.260
C	1	1	0	0	3/4	3/64	3.840	0.240
B	1	0	1	1	11/16	11/256	3.520	0.220
A	1	0	1	0	5/8	5/128	3.200	0.200
9	1	0	0	1	9/16	9/256	2/880	0.180
8	1	0	0	0	1/2	1/32	2/560	0.160
7	0	1	1	1	7/16	7/256	2.240	0.140
6	0	1	1	0	3/8	3/128	1.920	0.120
5	0	1	0	1	5/16	2/256	1.600	0.100
4	0	1	0	0	1/4	1/64	1/280	0.080
3	0	0	1	1	3/16	3/256	0.960	0.060
2	0	0	1	0	1/8	1/128	0.640	0.040
1	0	0	0	1	1/16	1/256	0.320	0.020
0	0	0	0	0			0	0

Display Output = VMS Group + VLS Group

Functional Description (Continued)



TL/H/5671–20

Note 1: *Pin numbers for the DP8228 system controller, others are INS8080A.

Note 2: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 10. ADC0801–INS8080A CPU Interface

SAMPLE PROGRAM FOR *FIGURE 10* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:      JMP     LD DATA
  •       •           •
  •       •           •
0100    21 00 02    START:      LXI H 0200H         ;HL pair will point to
                                                    ;data storage locations
0103    31 00 04    RETURN:     LXI SP 0400H        ;Initialize stack pointer (Note 1)
0106    7D                      MOV A, L            ;Test # of bytes entered
0107    FE 0F                   CPI 0F H            ;If # = 16. JMP to
0109    CA 13 01                JZ CONT             ;user program
010C    D3 E0                   OUT E0 H            ;Start A/D
010E    FB                      EI                  ;Enable interrupt
010F    00          LOOP:       NOP                 ;Loop until end of
0110    C3 0F 01                JMP LOOP            ;conversion
0113      •         CONT:         •
  •       •           •           •
  •       •         (User program to  •
  •       •         process data)     •
  •       •           •           •
  •       •           •           •
0300    DB E0       LD DATA:    IN E0 H             ;Load data into accumulator
0302    77                      MOV M, A            ;Store data
0303    23                      INX H               ;Increment storage pointer
0304    C3 03 01                JMP RETURN
```

Note 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 2: All address used were arbitrarily chosen.

Functional Description (Continued)

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

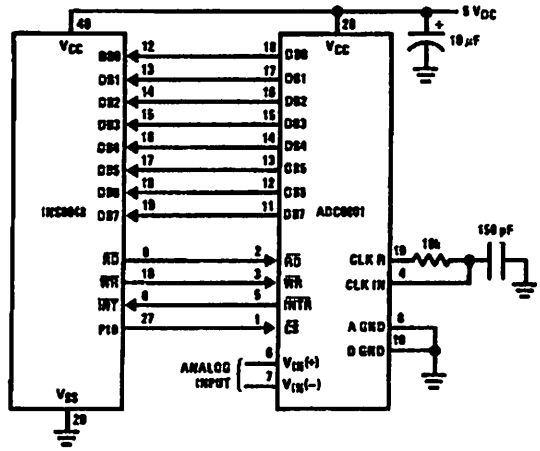
4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 10* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 11*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.



TL/H/5671–21

FIGURE 11. INS8048 Interface

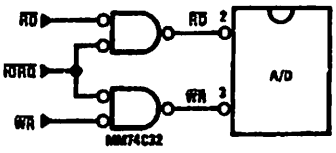
SAMPLE PROGRAM FOR *FIGURE 11* INS8048 INTERFACE

```
04 10                   JMP     10H             ;Program starts at addr 10
                        ORG     3H
04 50                   JMP     50H             ;Interrupt jump vector
                        ORG     10H             ;Main program
99 FE                   ANL     P1, #0FEH       ;Chip select
81                      MOVX    A, @R1          ;Read in the 1st data
                                                ;to reset the intr
89 01           START:  ORL     P1, #1          ;Set port pin high
B8 20                   MOV     R0, #20H        ;Data address
B9 FF                   MOV     R1, #0FFH       ;Dummy address
BA 10                   MOV     R2, #10H        ;Counter for 16 bytes
23 FF           AGAIN:  MOV     A, #0FFH        ;Set ACC for intr loop
99 FE                   ANL     P1, #0FEH       ;Send CS (bit 0 of P1)
91                      MOVX    @R1, A          ;Send WR out
05                      EN      I               ;Enable interrupt
96 21           LOOP:   JNZ     LOOP            ;Wait for interrupt
EA 1B                   DJNZ    R2, AGAIN       ;If 16 bytes are read
00                      NOP                     ;go to user's program
00                      NOP
                        ORG     50H
81              INDATA: MOVX    A, @R1          ;Input data, CS still low
A0                      MOV     @R0, A          ;Store in memory
18                      INC     R0              ;Increment storage counter
89 01                   ORL     P1, #1          ;Reset CS signal
27                      CLR     A               ;Clear ACC to get out of
93                      RETR                    ;the interrupt loop
```

Functional Description (Continued)

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 13*.



TL/H/5671–23

FIGURE 13. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived fom the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 14* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 15* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

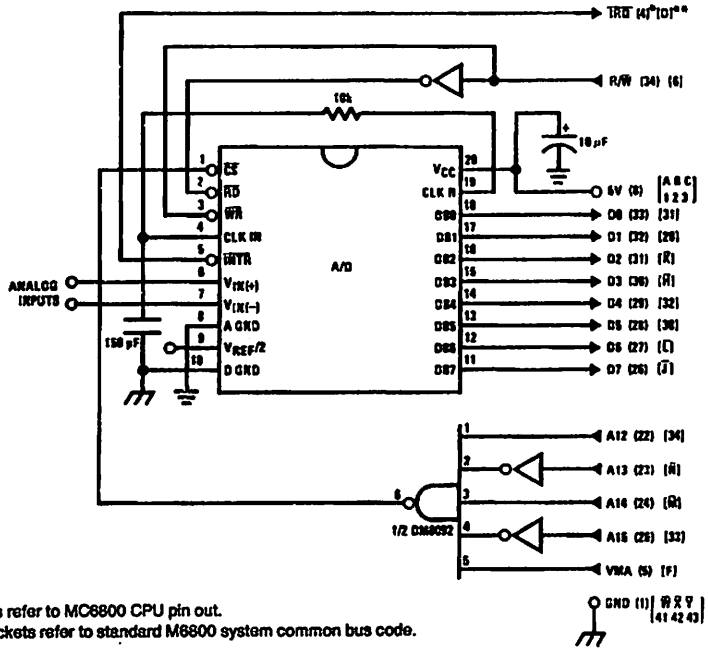
A sample interface program equivalent to the previous one is shown below *Figure 15*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 16*.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.
Note 2: Number or letters in brackets refer to standard M6800 system common bus code.

TL/H/5671–24

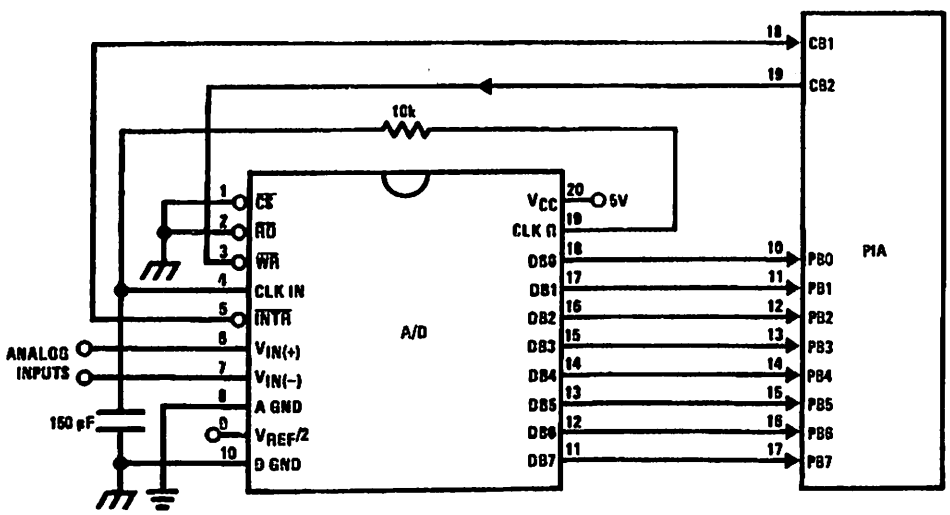
FIGURE 14. ADC0801-MC6800 CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 14* ADC0801-MC6800 CPU INTERFACE

```
0010  DF 36     DATAIN  STX   TEMP2   ; Save contents of X
0012  CE 00 2C          LDX   #$002C  ; Upon IRQ low CPU
0015  FF FF F8          STX   $FFF8   ; jumps to 002C
0018  B7 50 00          STAA  $5000   ; Start ADC0801
001B  0E                CLI
001C  3E        CONVRT  WAI           ; Wait for interrupt
001D  DE 34             LDX   TEMP1
001F  8C 02 0F          CPX   #$020F  ; Is final data stored?
0022  27 14             BEQ   ENDP
0024  B7 50 00          STAA  $5000   ; Restarts ADC0801
0027  08                INX
0028  DF 34             STX   TEMP1
002A  20 F0             BRA   CONVRT
002C  DE 34     INTRPT  LDX   TEMP1
002E  B6 50 00          LDAA  $5000   ; Read data
0031  A7 00             STAA  X       ; Store it at X
0033  3B                RTI
0034  02 00     TEMP1   FDB   $0200   ; Starting address for
                                      ; data storage
0036  00 00     TEMP2   FDB   $0000
0038  CE 02 00  ENDP    LDX   #$0200  ; Reinitialize TEMP1
003B  DF 34             STX   TEMP1
003D  DE 36             LDX   TEMP2
003F  39                RTS           ; Return from subroutine
                                      ; To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.



TL/H/5671–25

FIGURE 15. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 15* ADC0801–MC6820 PIA INTERFACE

```
0010  CE 00 38     DATAIN   LDX    #$0038     ; Upon IRQ low CPU
0013  FF FF F8              STX    $FFF8      ; jumps to 0038
0016  B6 80 06              LDAA   PIAORB     ; Clear possible IRQ flags
0019  4F                    CLRA
001A  B7 80 07              STAA   PIACRB
001D  B7 80 06              STAA   PIAORB     ; Set Port B as input
0020  0E                    CLI
0021  C6 34                 LDAB   #$34
0023  86 3D                 LDAA   #$3D
0025  F7 80 07     CONVRT   STAB   PIACRB     ; Starts ADC0801
0028  B7 80 07              STAA   PIACRB
002B  3E                    WAI                ; Wait for interrupt
002C  DE 40                 LDX    TEMP1
002E  8C 02 0F              CPX    #$020F     ; Is final data stored?
0031  27 0F                 BEQ    ENDP
0033  08                    INX
0034  DF 40                 STX    TEMP1
0036  20 ED                 BRA    CONVRT
0038  DE 40        INTRPT   LDX    TEMP1
003A  B6 80 06              LDAA   PIAORB     ; Read data in
003D  A7 00                 STAA   X          ; Store it at X
003F  3B                    RTI
0040  02 00        TEMP1    FDB    $0200      ; Starting address for
                                               ; data storage
0042  CE 02 00     ENDP     LDX    #$0200     ; Reinitialize TEMP1
0045  DF 40                 STX    TEMP1
0047  39                    RTS                ; Return from subroutine
                   PIAORB   EQU    $8006      ; To user's program
                   PIACRB   EQU    $8007
```

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

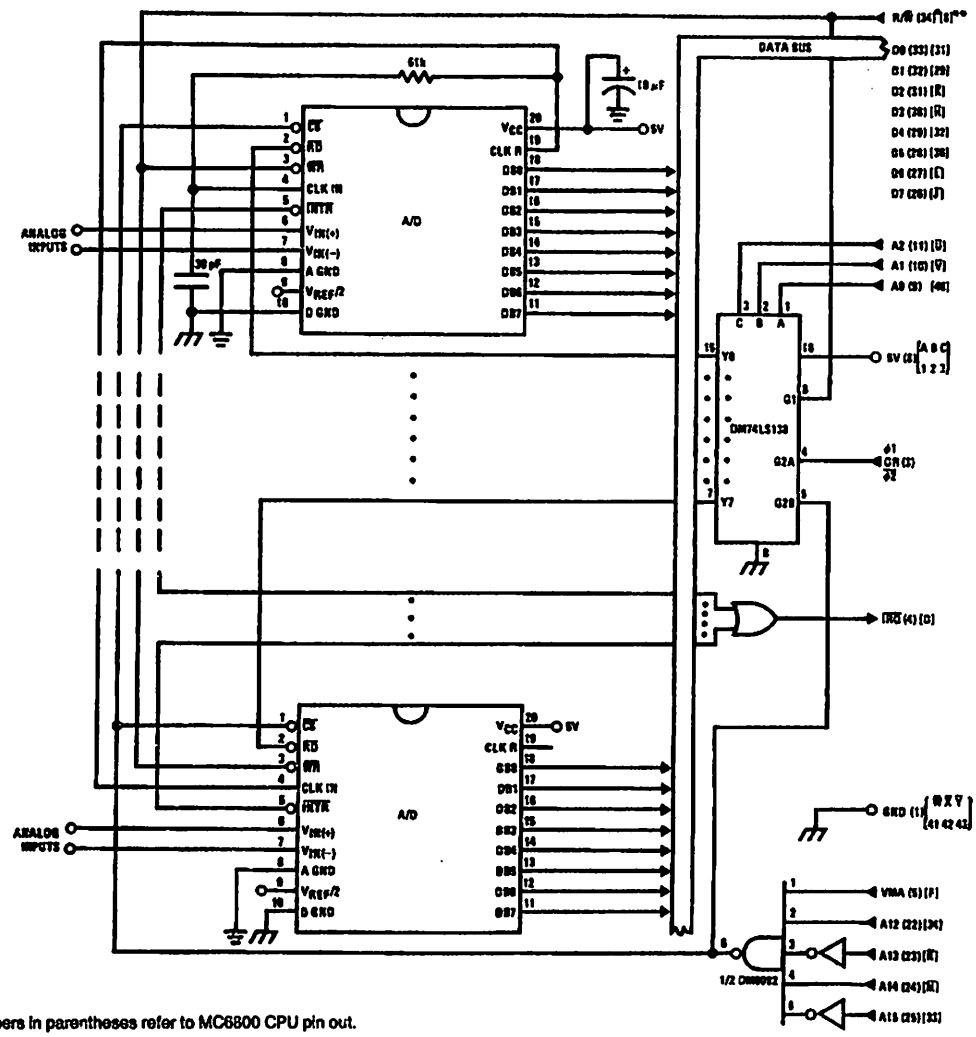
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers of letters in brackets refer to standard M6800 system common bus code.

TL/H/5671–26

FIGURE 16. Interfacing Multiple A/Ds in an MC6800 System

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE	MNEMONICS			COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 17* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

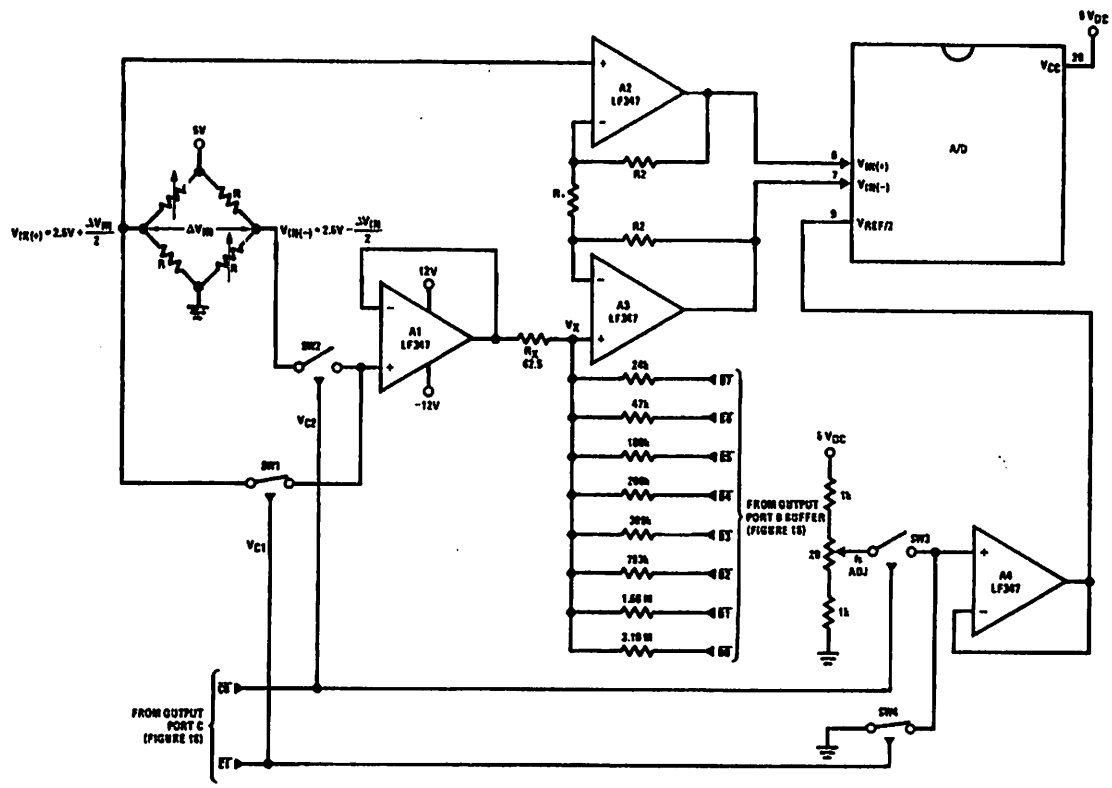
$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 18*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_x increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 μV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.

Functional Description (Continued)

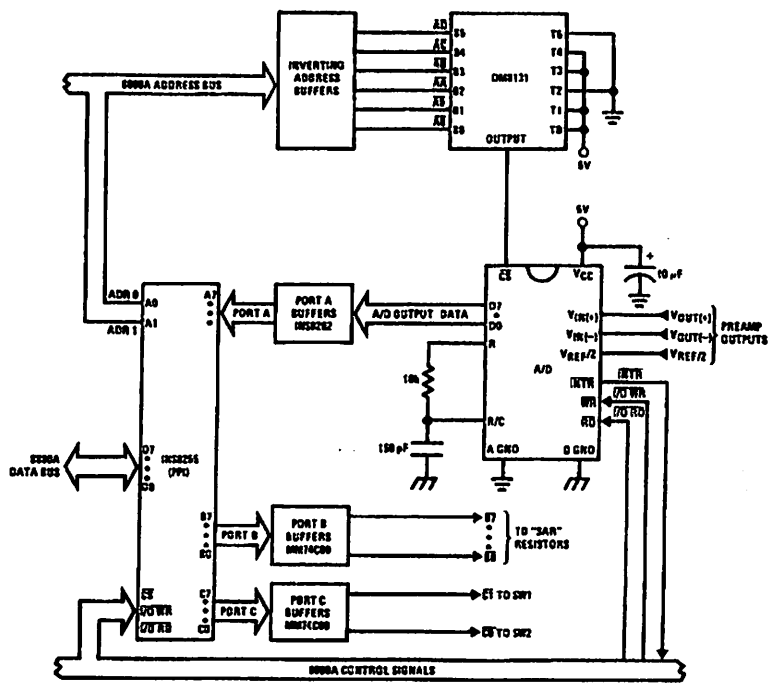


Note 1: R2 = 49.5 R1

Note 2: Switches are LMC13334 CMOS analog switches.

Note 3: The 9 resistors used in the auto-zero section can be ± 5% tolerance.

FIGURE 17. Gain of 100 Differential Transducer Preamp



TL/H/5671–27

FIGURE 18. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 19*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 20*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

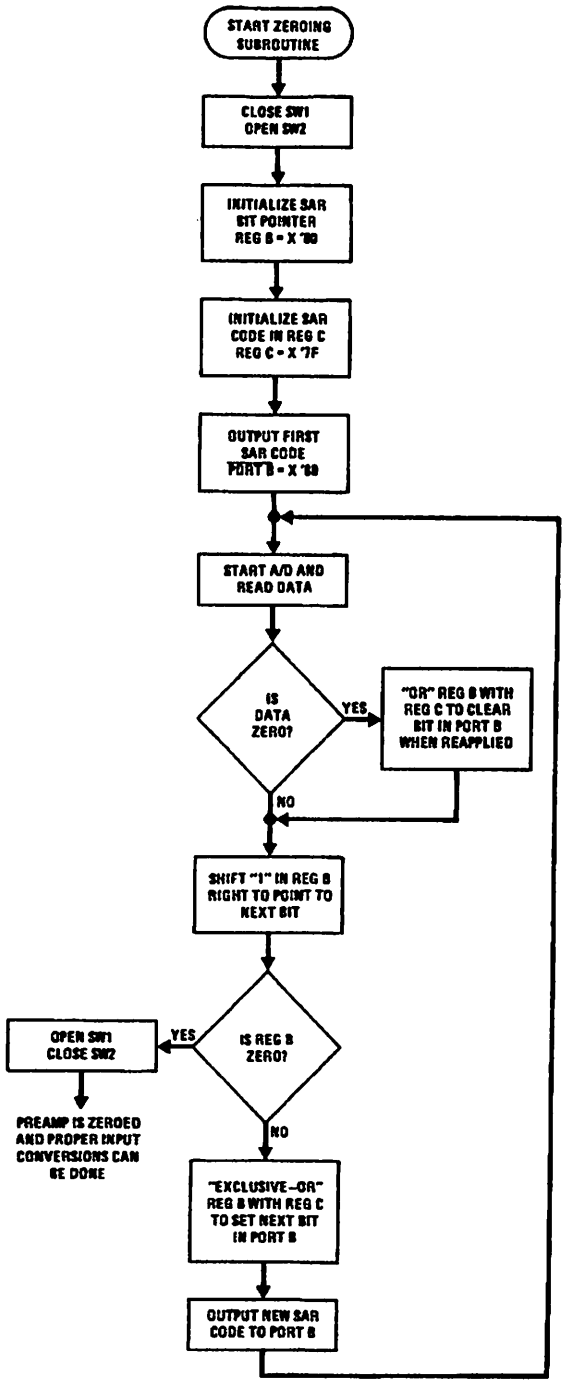
PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 21* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.



TL/H/5671–28

FIGURE 19. Flow Chart for Auto-Zero Routine

```
3D00   3E90     MVI 90
3D02   D3E7     Out Control Port                    ;Program PPI
3D04   2601     MVI H 01          Auto-Zero Subroutine
3D06   7C       MOV A,H
3D07   D3E6     OUT C                              ;Close SW1 open SW2
3D09   0680     MVI B 80                           ;Initialize SAR bit pointer
3D0B   3E7F     MVI A 7F                           ;Initialize SAR code
3D0D   4F       MOV C,A           Return
3D0E   D3E5     OUT B                              ;Port B = SAR code
3D10   31AA3D   LXI SP 3DAA       Start            ;Dimension stack pointer
3D13   D3E4     OUT A                              ;Start A/D
3D15   FB       IE
3D16   00       NOP               Loop             ;Loop until INT asserted
3D17   C3163D   JMP Loop
3D1A   7A       MOV A,D           Auto-Zero
3D1B   C600     ADI 00
3D1D   CA2D3D   JZ Set C                           ;Test A/D output data for zero
3D20   78       MOV A,B           Shift B
3D21   F600     ORI 00                             ;Clear carry
3D23   1F       RAR                                ;Shift "1" in B right one place
3D24   FE00     CPI 00                             ;Is B zero? If yes last
3D26   CA373D   JZ Done                            ;approximation has been made
3D29   47       MOV B,A
3D2A   C3333D   JMP New C
3D2D   79       MOV A,C           Set C
3D2E   B0       ORA B                              ;Set bit in C that is in same
3D2F   4F       MOV C,A                            ;position as "1" in B
3D30   C3203D   JMP Shift B
3D33   A9       XRA C             New C            ;Clear bit in C that is in
3D34   C30D3D   JMP Return                         ;same position as "1" in B
3D37   47       MOV B,A           Done             ;then output new SAR code.
3D38   7C       MOV A,H                            ;Open SW1, close SW2 then
3D39   EE03     XRI 03                             ;proceed with program. Preamp
3D3B   D3E6     OUT C                              ;is now zeroed.
3D3D            •                 Normal
                •
                •
                Program for processing
                proper data values
3C3D   DBE4     IN A              Read A/D Subroutine  ;Read A/D data
3C3F   EEFF     XRI FF                             ;Invert data
3C41   57       MOV D,A
3C42   78       MOV A,B                            ;Is B Reg = 0? If not stay
3C43   E6FF     ANI FF                             ;in auto zero subroutine
3C45   C21A3D   JNZ Auto-Zero
3C48   C33D3D   JMP Normal
```

Note: All numerical values are hexadecimal representations.

FIGURE 20. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80® Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

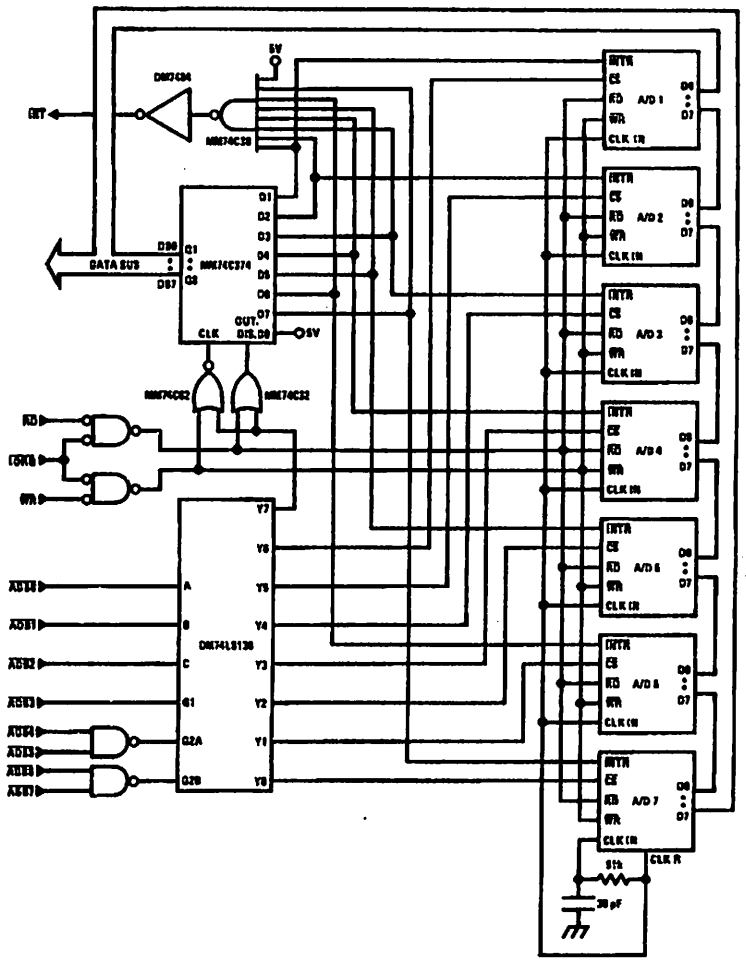
3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.



TL/H/5671-29

FIGURE 21. Multiple A/Ds with Z-80 Type Microprocessor

INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE	SOURCE STATEMENT	COMMENT
0038	E5	PUSH HL	; Save contents of all registers affected by
0039	C5	PUSH BC	; this subroutine.
003A	F5	PUSH AF	; Assumed INT mode 1 earlier set.
003B	21 00 3E	LD (HL), X3E00	; Initialize memory pointer where data will be stored.
003E	0E 01	LD C, X01	; C register will be port ADDR of A/D converters.
0040	D300	OUT X00, A	; Load peripheral status word into 8-bit latch.
0042	DB00	IN A, X00	; Load status word into accumulator.
0044	47	LD B,A	; Save the status word.
0045	79	TEST LD A,C	; Test to see if the status of all A/D's have
0046	FE 08	CP, X08	; been checked. If so, exit subroutine
0048	CA 60 00	JPZ, DONE	
004B	78	LD A,B	; Test a single bit in status word by looking for
004C	1F	RRA	; a "1" to be rotated into the CARRY (an $\overline{INT}$
004D	47	LD B,A	; is loaded as a "1"). If CARRY is set then load
004E	DA 5500	JPC, LOAD	; contents of A/D at port ADDR in C register.
0051	0C	NEXT INC C	; If CARRY is not set, increment C register to point
0052	C3 4500	JP,TEST	; to next A/D, then test next bit in status word.
0055	ED 78	LOAD IN A, (C)	; Read data from interrupting A/D and invert
0057	EE FF	XOR FF	; the data.
0059	77	LD (HL),A	; Store the data
005A	2C	INC L	
005B	71	LD (HL),C	; Store A/D identifier (A/D port ADDR).
005C	2C	INC L	
005D	C3 51 00	JP,NEXT	; Test next bit in status word.
0060	F1	DONE POP AF	; Re-establish all registers as they were
0061	C1	POP BC	; before the interrupt.
0062	E1	POP HL	
0063	C9	RET	; Return to original program

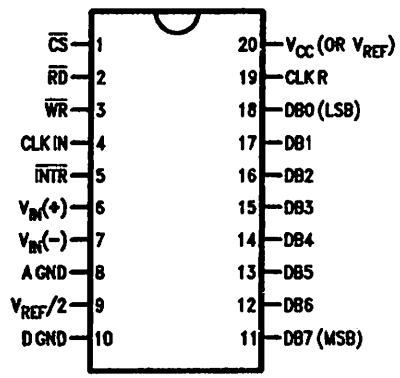
Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted				ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM	ADC0802LCV		ADC0802LCN
	±½ Bit Adjusted	ADC0803LCWM	ADC0803LCV		ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCV	ADC0804LCN	ADC0805LCN
PACKAGE OUTLINE		M20B—Small Outline	V20A—Chip Carrier	N20A—Molded DIP	

TEMP RANGE		−40°C TO +85°C	−55°C TO +125°C
ERROR	±¼ Bit Adjusted	ADC0801LCJ	ADC0801LJ
	±½ Bit Unadjusted	ADC0802LCJ	ADC0802LJ,
	±½ Bit Adjusted	ADC0803LCJ	ADC0802LJ/883
	±1Bit Unadjusted	ADC0804LCJ	
PACKAGE OUTLINE		J20A—Cavity DIP	J20A—Cavity DIP

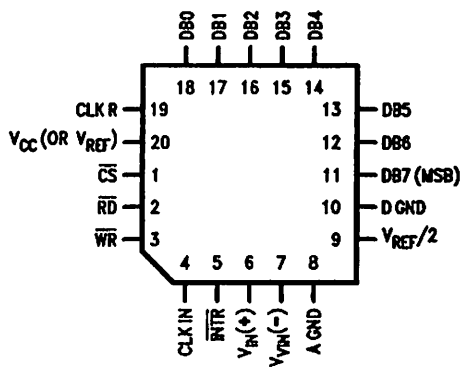
Connection Diagrams

ADC080X
Dual-In-Line and Small Outline (SO) Packages



TL/H/5671–30

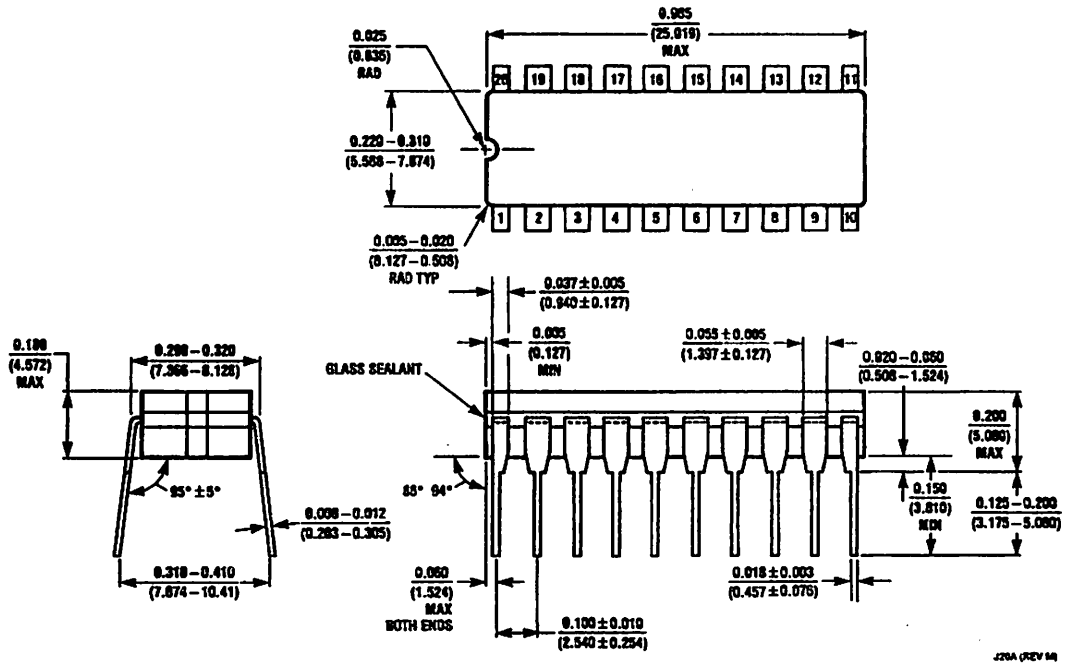
ADC080X
Molded Chip Carrier (PCC) Package



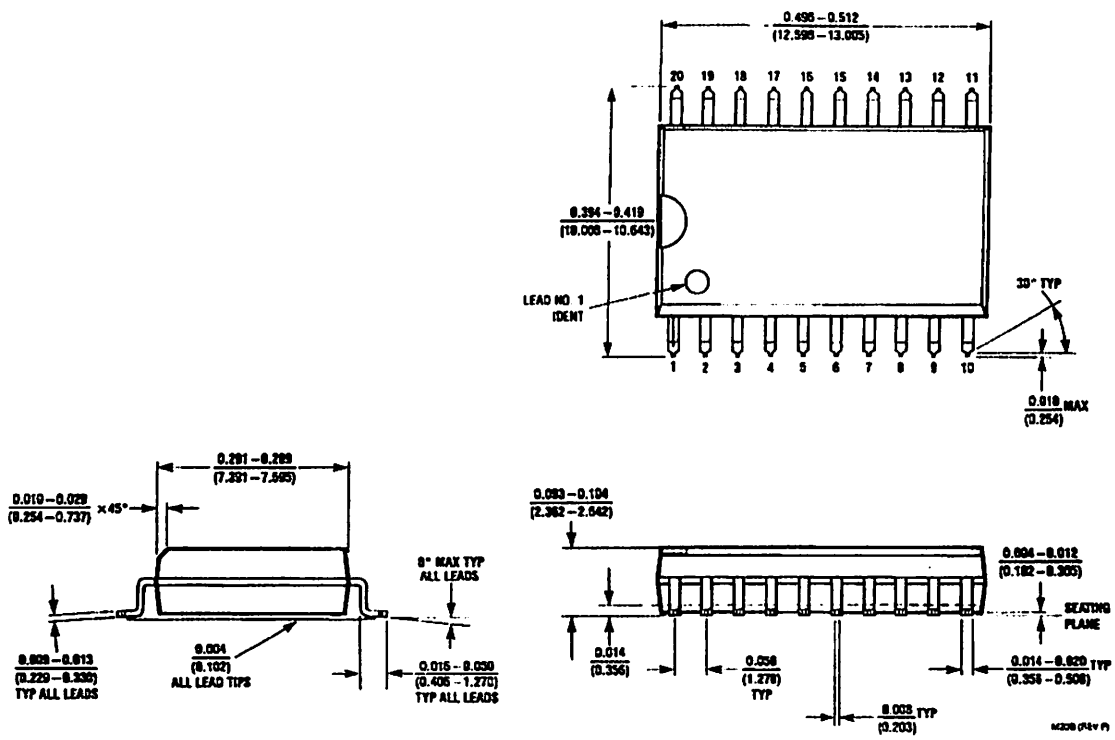
TL/H/5671–32

See Ordering Information

Physical Dimensions inches (millimeters)

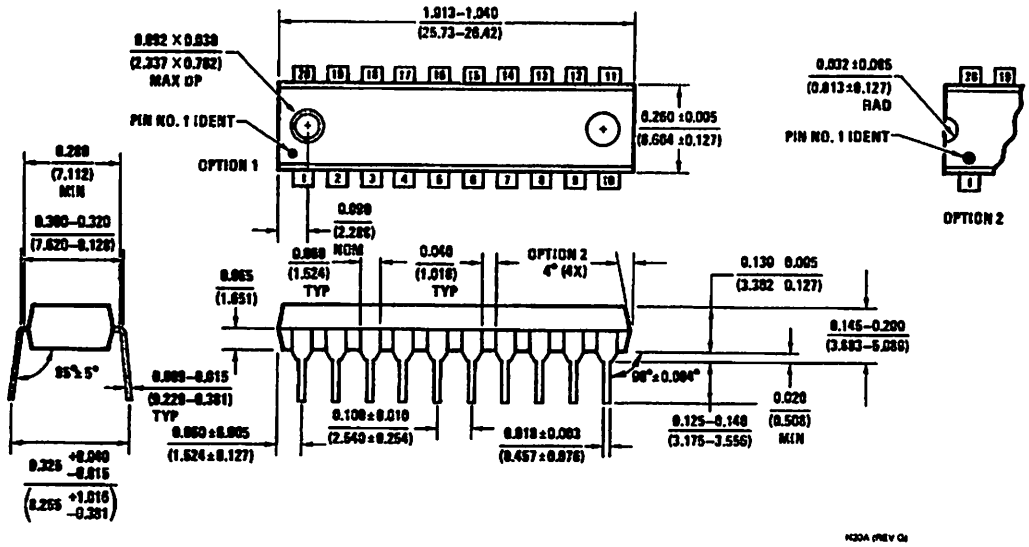


Dual-In-Line Package (J)
Order Number ADC0801LJ, ADC0802LJ, ADC0801LCJ,
ADC0802LCJ, ADC0803LCJ or ADC0804LCJ
ADC0802LJ/883 or 5962-9096601MRA
NS Package Number J20A



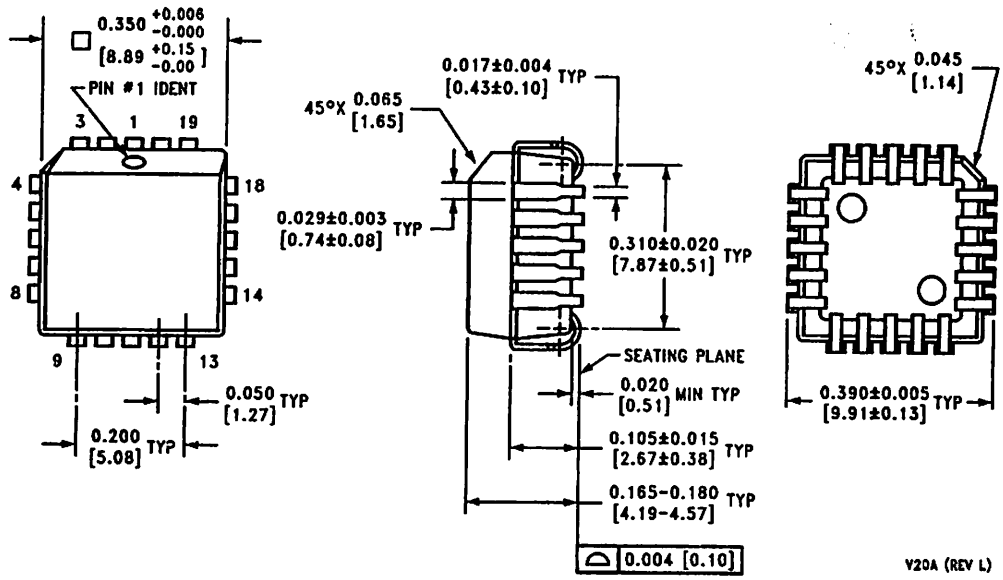
SO Package (M)
Order Number ADC0802LCWM, ADC0803LCWM or ADC0804LCWM
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number ADC0801LCN, ADC0802LCN,
ADC0803LCN, ADC0804LCN or ADC0805LCN
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



Molded Chip Carrier Package (V)
Order Number ADC0802LCV, ADC0803LCV or ADC0804LCV
NS Package Number V20A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

50 kPa On-Chip Temperature Compensated & Calibrated Silicon Pressure Sensors

MPX2050 SERIES

0 to 50 kPa (0 to 7.25 psi)
40 mV FULL SCALE SPAN
(TYPICAL)

The MPX2050 series device is a silicon piezoresistive pressure sensors providing a highly accurate and linear voltage output — directly proportional to the applied pressure. The sensor is a single, monolithic silicon diaphragm with the strain gauge and a thin–film resistor network integrated on–chip. The chip is laser trimmed for precise span and offset calibration and temperature compensation.

Features

- Temperature Compensated Over 0°C to +85°C
- Unique Silicon Shear Stress Strain Gauge
- Easy to Use Chip Carrier Package Options
- Ratiometric to Supply Voltage
- Differential and Gauge Options
- ±0.25% Linearity (MPX2050)

Application Examples

- Pump/Motor Controllers
- Robotics
- Level Indicators
- Medical Diagnostics
- Pressure Switching
- Non–Invasive Blood Pressure Measurement

Figure 1 shows a block diagram of the internal circuitry on the stand–alone pressure sensor chip.

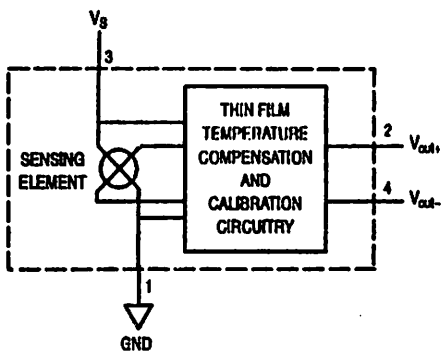
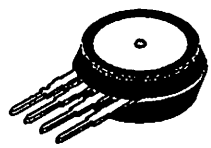


Figure 1. Temperature Compensated Pressure Sensor Schematic

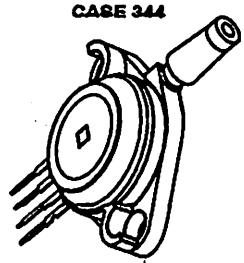
VOLTAGE OUTPUT versus APPLIED DIFFERENTIAL PRESSURE

The differential voltage output of the sensor is directly proportional to the differential pressure applied.

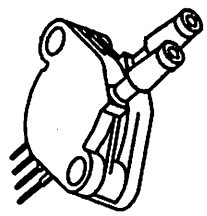
The output voltage of the differential or gauge sensor increases with increasing pressure applied to the pressure side (P1) relative to the vacuum side (P2). Similarly, output voltage increases as increasing vacuum is applied to the vacuum side (P2) relative to the pressure side (P1).



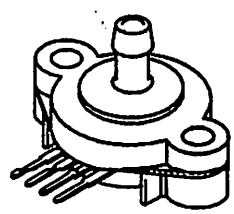
MPX2050D
CASE 344



MPX2050GP
CASE 344B



MPX2050DP
CASE 344C



MPX2050GSX
CASE 344F

PIN NUMBER			
1	Gnd	3	V_S
2	$+V_{out}$	4	$-V_{out}$

NOTE: Pin 1 is noted by the notch in the lead.

AXIMUM RATINGS(NOTE)

Rating	Symbol	Value	Unit
Maximum Pressure (P1 > P2)	P_{max}	200	kPa
Storage Temperature	T_{stg}	–40 to +125	°C
Operating Temperature	T_A	–40 to +125	°C

TE: Exposure beyond the specified limits may cause permanent damage or degradation to the device.

ERATING CHARACTERISTICS (V_S = 10 Vdc, T_A = 25°C unless otherwise noted, P1 > P2)

Characteristic		Symbol	Min	Typ	Max	Unit
ressure Range[1]		P_{OP}	0	—	50	kPa
upply Voltage[2]		V_S	—	10	16	Vdc
upply Current		I_o	—	6.0	—	mAdc
ull Scale Span[3]	MPX2050	V_{FSS}	38.5	40	41.5	mV
ffset[4]	MPX2050	V_{off}	–1.0	—	1.0	mV
ensitivity		$\Delta V/\Delta P$	—	0.8	—	mV/kPa
nearity[5]	MPX2050	—	–0.25	—	0.25	$\%V_{FSS}$
ressure Hysteresis[5] (0 to 50 kPa)		—	—	±0.1	—	$\%V_{FSS}$
mperature Hysteresis[5] (–40°C to +125°C)		—	—	±0.5	—	$\%V_{FSS}$
mperature Effect on Full Scale Span[5]		TCV_{FSS}	–1.0	—	1.0	$\%V_{FSS}$
mperature Effect on Offset[5]		TCV_{off}	–1.0	—	1.0	mV
put Impedance		Z_{in}	1000	—	2500	Ω
utput Impedance		Z_{out}	1400	—	3000	Ω
esponse Time[6] (10% to 90%)		t_R	—	1.0	—	ms
arm–Up		—	—	20	—	ms
ffset Stability[7]		—	—	±0.5	—	$\%V_{FSS}$

ES:

1. 1.0 kPa (kiloPascal) equals 0.145 psi.
2. Device is ratiometric within this specified excitation range. Operating the device above the specified excitation range may induce additional error due to device self–heating.
3. Full Scale Span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.
4. Offset (V_{off}) is defined as the output voltage at the minimum rated pressure.
5. Accuracy (error budget) consists of the following:
   - Linearity: Output deviation from a straight line relationship with pressure, using end point method, over the specified pressure range.
   - Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to and from the minimum or maximum operating temperature points, with zero differential pressure applied.
   - Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from the minimum or maximum rated pressure, at 25°C.
   - TcSpan: Output deviation at full rated pressure over the temperature range of 0 to 85°C, relative to 25°C.
   - TcOffset: Output deviation with minimum rated pressure applied, over the temperature range of 0 to 85°C, relative to 25°C.
6. Response Time is defined as the time for the incremental change in the output to go from 10% to 90% of its final value when subjected to a specified step change in pressure.
7. Offset stability is the product's output deviation when subjected to 1000 hours of Pulsed Pressure, Temperature Cycling with Bias Test.

LINEARITY

Linearity refers to how well a transducer's output follows the equation: $V_{out} = V_{off} + sensitivity \times P$ over the operating pressure range. There are two basic methods for calculating nonlinearity: (1) end point straight line fit (see Figure 2) or (2) a least squares best line fit. While a least squares fit gives the "best case" linearity error (lower numerical value), the calculations required are burdensome.

Conversely, an end point fit will give the "worst case" error (often more desirable in error budget calculations) and the calculations are more straightforward for the user. Motorola's specified pressure sensor linearities are based on the end point straight line method measured at the midrange pressure.

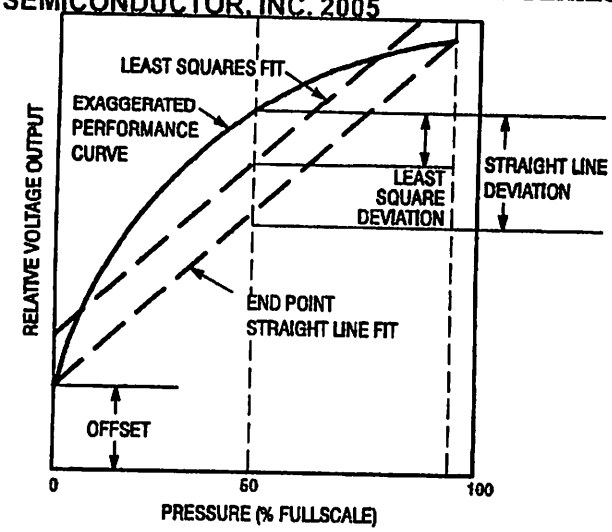


Figure 2. Linearity Specification Comparison

ON–CHIP TEMPERATURE COMPENSATION and CALIBRATION

Figure 3 shows the minimum, maximum and typical output characteristics of the MPX2050 series at 25°C. The output is directly proportional to the differential pressure and is essentially a straight line.

The effects of temperature on Full–Scale Span and Offset are very small and are shown under Operating Characteristics.

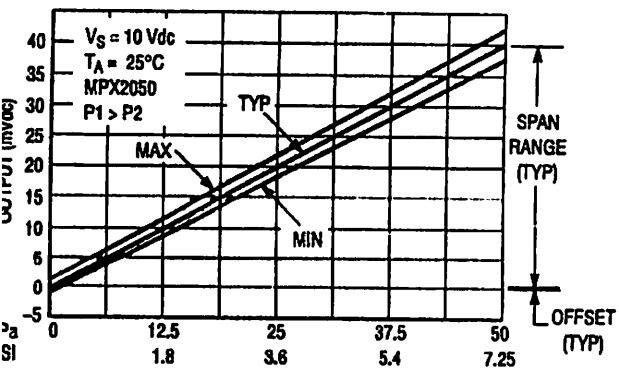


Figure 3. Output versus Pressure Differential

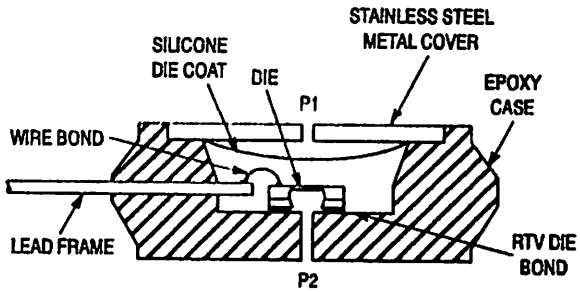


Figure 4. Cross–Sectional Diagram (not to scale)

Figure 4 illustrates the differential or gauge configuration the basic chip carrier (Case 344). A silicone gel isolates e die surface and wire bonds from the environment, while lowing the pressure signal to be transmitted to the silicon aphragm.

The MPX2050 series pressure sensor operating characteristics and internal reliability and qualification tests are based on use of dry air as the pressure media. Media other than dry air may have adverse effects on sensor performance and long term reliability. Contact the factory for information regarding media compatibility in your application.

PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE

Motorola designates the two sides of the pressure sensor ; the Pressure (P1) side and the Vacuum (P2) side. The essure (P1) side is the side containing the silicone gel ich isolates the die. The Motorola MPX pressure sensor is designed to operate with positive differential pressure applied, P1 > P2.

The Pressure (P1) side may be identified by using the table below:

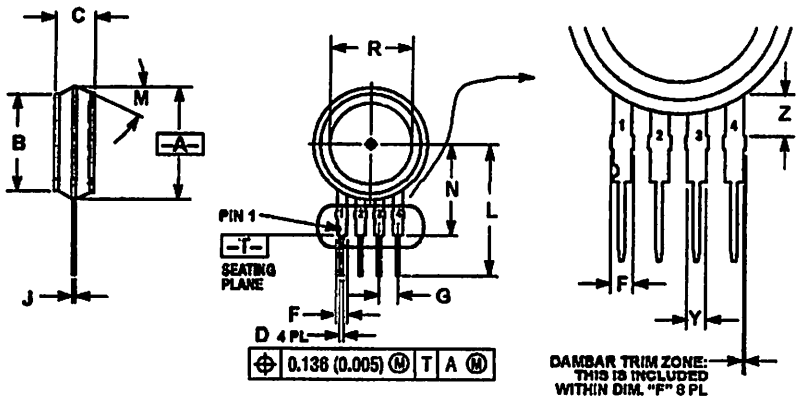
Part Number	Case Type	Pressure (P1) Side Identifier
MPX2050D	344	Stainless Steel Cap
MPX2050DP	344C	Side with Part Marking
MPX2050GP	344B	Side with Port Attached
MPX2050GSX	344F	Side with Port Attached

DERING INFORMATION

MPX2050 series pressure sensors are available in differential and gauge configurations. Devices are available in the basic nent package or with pressure port fittings which provide printed circuit board mounting ease and barbed hose pressure nections.

evice Type	Options	Case Type	MPX Series	
			Order Number	Device Marking
sic Element	Differential	344	MPX2050D	MPX2050D
rted Elements	Differential, Dual Port	344C	MPX2050DP	MPX2050DP
	Gauge	344B	MPX2050GP	MPX2050GP
	Gauge Axial PC Mount	344F	MPX2050GSX	MPX2050D

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION -A- IS INCLUSIVE OF THE MOLD STOP RING. MOLD STOP RING NOT TO EXCEED 16.00 (0.630).

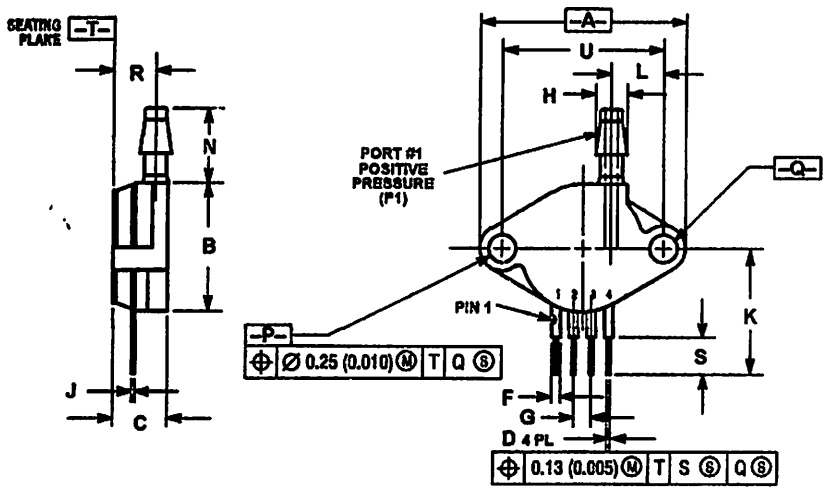
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.595	0.630	15.11	16.00
B	0.514	0.534	13.06	13.56
C	0.200	0.220	5.08	5.59
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.40
L	0.695	0.725	17.65	18.42
M	30° NOM		30° NOM	
N	0.475	0.495	12.07	12.57
R	0.430	0.450	10.92	11.43
Y	0.048	0.052	1.22	1.32
Z	0.106	0.118	2.69	3.00

STYLE 1:
PIN 1. GROUND
2. + OUTPUT
3. + SUPPLY
4. - OUTPUT

STYLE 2:
PIN 1. V_{CC}
2. - SUPPLY
3. + SUPPLY
4. GROUND

STYLE 3:
PIN 1. GND
2. -VOUT
3. VS
4. +VOUT

CASE 344–15
ISSUE Z



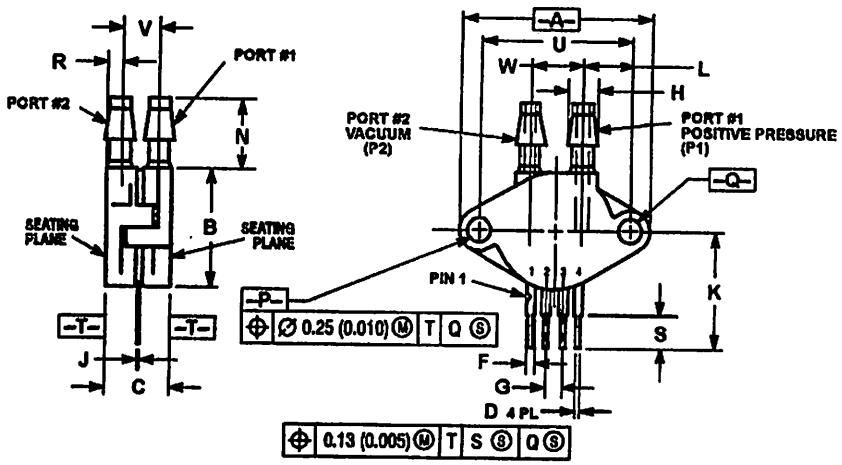
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.145	1.175	29.08	29.85
B	0.685	0.715	17.40	18.16
C	0.305	0.325	7.75	8.26
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
H	0.182	0.194	4.62	4.93
J	0.014	0.016	0.36	0.41
K	0.695	0.725	17.65	18.42
L	0.290	0.300	7.37	7.62
N	0.420	0.440	10.67	11.18
P	0.153	0.159	3.89	4.04
Q	0.153	0.159	3.89	4.04
R	0.230	0.250	5.84	6.35
S	0.220	0.240	5.59	6.10
U	0.910 BSC		23.11 BSC	

STYLE 1:
PIN 1. GROUND
2. + OUTPUT
3. + SUPPLY
4. - OUTPUT

CASE 344B–01
ISSUE B

PACKAGE DIMENSIONS — CONTINUED

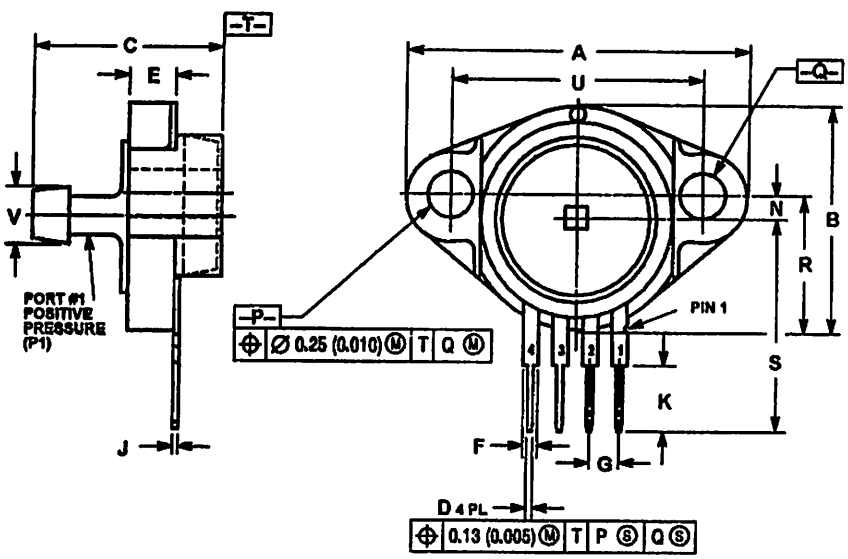


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.145	1.175	29.08	29.85
B	0.685	0.715	17.40	18.16
C	0.405	0.435	10.29	11.05
D	0.016	0.020	0.41	0.51
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
H	0.182	0.194	4.62	4.93
J	0.014	0.016	0.36	0.41
K	0.695	0.725	17.65	18.42
L	0.290	0.300	7.37	7.62
N	0.420	0.440	10.67	11.18
P	0.153	0.159	3.89	4.04
Q	0.153	0.159	3.89	4.04
R	0.083	0.083	1.60	2.11
S	0.220	0.240	5.59	6.10
U	0.910 BSC		23.11 BSC	
V	0.248	0.278	6.30	7.06
W	0.310	0.330	7.87	8.38

STYLE 1:
PIN 1. GROUND
2. + OUTPUT
3. + SUPPLY
4. - OUTPUT

CASE 344C–01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.080	1.120	27.43	28.45
B	0.740	0.760	18.80	19.30
C	0.630	0.650	16.00	16.51
D	0.016	0.020	0.41	0.51
E	0.160	0.180	4.06	4.57
F	0.048	0.064	1.22	1.63
G	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.41
K	0.220	0.240	5.59	6.10
N	0.070	0.080	1.78	2.03
P	0.150	0.160	3.81	4.06
Q	0.150	0.160	3.81	4.06
R	0.440	0.460	11.18	11.68
S	0.695	0.720	17.65	18.42
U	0.840	0.860	21.34	21.84
V	0.192	0.194	4.62	4.92

STYLE 1:
PIN 1. GROUND
2. V (+) OUT
3. V SUPPLY
4. V (-) OUT

CASE 344F–01
ISSUE B

NOTES

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3–20–1, Minami–Azabu. Minato–ku, Tokyo 106–8573 Japan. 81–3–3440–3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852–26668334

Technical Information Center: 1–800–521–6274

HOME PAGE: http://www.motorola.com/semiconductors/

Winbond Electronics Corp.

ISD2560/75/90/120

SINGLE-CHIP, MULTIPLE-MESSAGES, VOICE RECORD/PLAYBACK DEVICE 60-, 75-, 90-, AND 120-SECOND DURATION

Publication Release Date: May 2003
Revision 1.0

Winbond Electronics Corp.

1. GENERAL DESCRIPTION

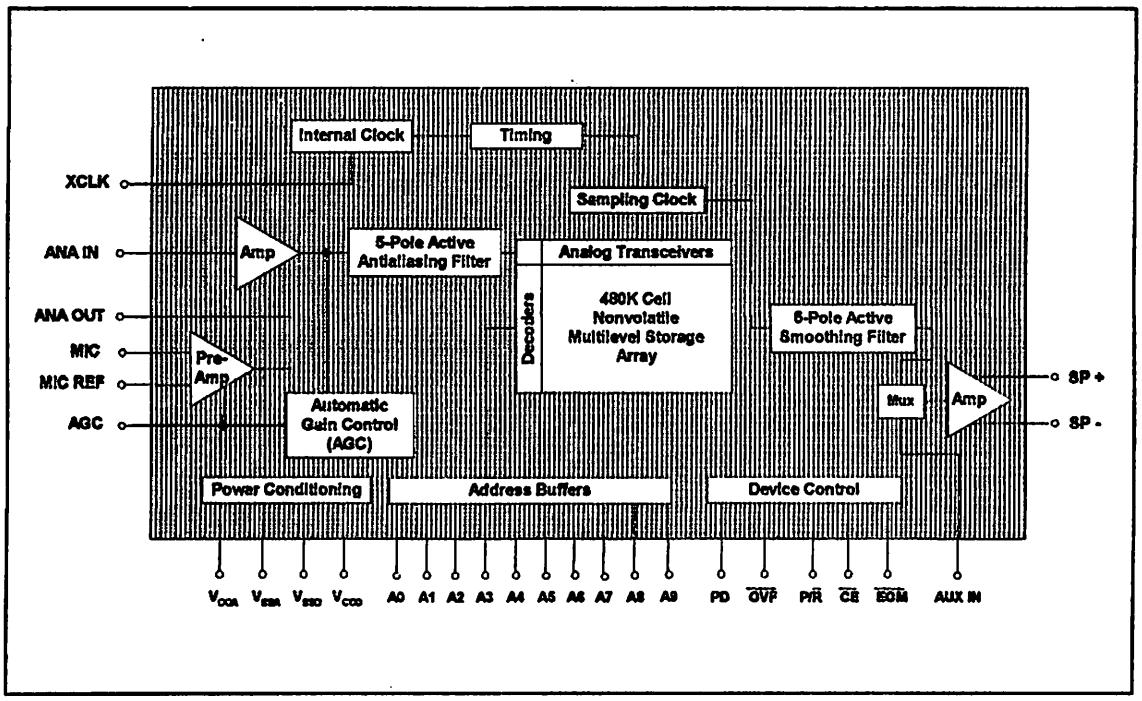
Winbond's ISD2500 ChipCorder® Series provide high-quality, single-chip, Record/Playback solutions for 60- to 120-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, speaker amplifier, and high density multi-level storage array. In addition, the ISD2500 is microcontroller compatible, allowing complex messaging and addressing to be achieved. Recordings are stored into on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through Winbond's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

2. FEATURES

- Easy-to-use single-chip, voice record/playback solution
- High-quality, natural voice/audio reproduction
- Single-chip with duration of 60, 75, 90, or 120 seconds.
- Manual switch or microcontroller compatible
- Playback can be edge- or level-activated
- Directly cascadable for longer durations
- Automatic power-down (push-button mode)
  - Standby current 1 µA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- Programmer support for play-only applications
- Single +5 volt power supply
- Available in die form, PDIP, SOIC and TSOP packaging
- Temperature = die (0°C to +50°C) and package (0°C to +70°C)

Winbond Electronics Corp.

3. BLOCK DIAGRAM



4. TABLE OF CONTENTS

Functional Description (Continued)

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.6), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the Q output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)}$$

which gives

$V_P \cong 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

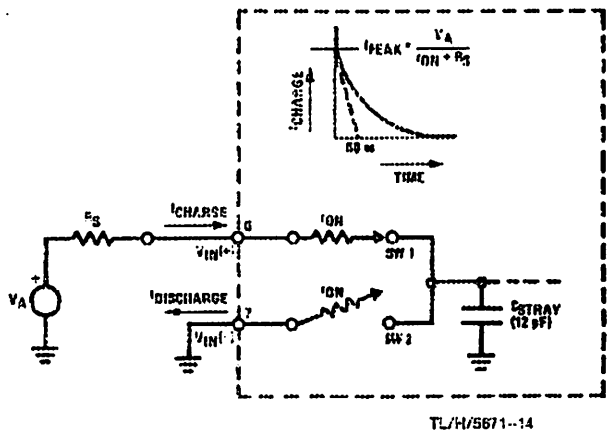
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



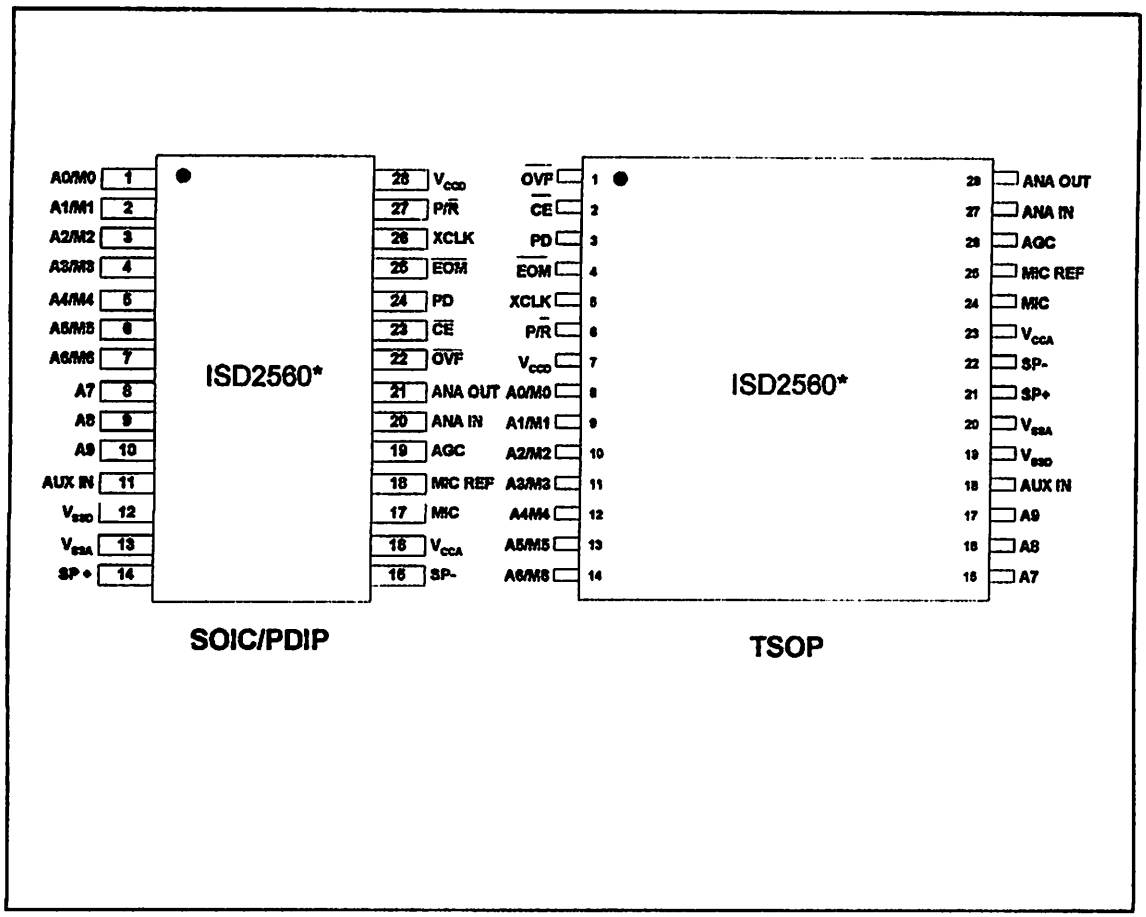
TL/H/5671–14

r_{ON} of SW 1 and SW 2 = 5 kΩ

$\tau = r_{ON} C_{STRAY} = 5\ k\Omega \cdot 12\ pF = 60\ ns$

FIGURE 3. Analog Input Impedance

5. PIN CONFIGURATION



* Same pinouts for ISD2575 / 2590 / 25120 products

6. PIN DESCRIPTION

PIN NAME	PIN NO.		FUNCTION
	SOIC/ PDIP	TSOP	
Ax/Mx	1-10/ 1-7	8-17/ 8-14	**Address/Mode Inputs**: The Address/Mode Inputs have two functions depending on the level of the two Most Significant Bits (MSB) of the address pins (A8 and A9). If either or both of the two MSBs are LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output any internal address information during the operation. Address inputs are latched by the falling edge of $\overline{CE}$. If both MSBs are HIGH, the Address/Mode inputs are interpreted as Mode bits according to the Operational Mode table on page 12. There are six operational modes (M0...M6) available as indicated in the table. It is possible to use multiple operational modes simultaneously. Operational Modes are sampled on each falling edge of $\overline{CE}$, and thus Operational Modes and direct addressing are mutually exclusive.
AUX IN	11	18	**Auxiliary Input:** The Auxiliary Input is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is HIGH, $P/\overline{R}$ is HIGH, and playback is currently not active or if the device is in playback overflow. When cascading multiple ISD2500 devices, the AUX IN pin is used to connect a playback signal from a following device to the previous output speaker drivers. For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.
V_{SSA}, V_{SSD}	13, 12	20, 19	**Ground**: The ISD2500 series of devices utilizes separate analog and digital ground busses. These pins should be connected separately through a low-impedance path to power supply ground.
SP+/SP-	14/15	21/22	**Speaker Outputs**: All devices in the ISD2500 series include an on-chip differential speaker driver, capable of driving 50 mW into 16 Ω from AUX IN (12.2mW from memory). [1] The speaker outputs are held at V_{SSA} levels during record and power down. It is therefore not possible to parallel speaker outputs of multiple ISD2500 devices or the outputs of other speaker drivers. [2] A single-end output may be used (including a coupling capacitor between the SP pin and the speaker). These outputs may be used individually with the output signal taken from either pin. However, the use of single-end output results in a 1 to 4 reduction in its output power.

[1] Connection of speaker outputs in parallel may cause damage to the device.
[2] Never ground or drive an unused speaker output.

PIN NAME	PIN NO. SOIC/ PDIP	PIN NO. TSOP	FUNCTION
V_{CCA}, V_{CCD}	16, 28	23, 7	**Supply Voltage**: To minimize noise, the analog and digital circuits in the ISD2500 series devices use separate power busses. These voltage busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.
MIC	17	24	**Microphone**: The microphone pin transfers input signal to the on-chip preamplifier. A built-in Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the ISD2500 series passband. See Winbond's Application Information for additional information on low-frequency cutoff calculation.
MIC REF	18	25	**Microphone Reference**: The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected to a differential microphone.
AGC	19	26	**Automatic Gain Control**: The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2 on the schematic of Figure 5 in section 11) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2) connected in parallel between the AGC pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases.
ANA IN	20	27	**Analog Input**: The analog input transfers analog signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.
ANA OUT	21	28	**Analog Output**: This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

PIN NAME	PIN NO. SOIC/ PDIP	PIN NO. TSOP	FUNCTION
$\overline{OVF}$	22	1	**Overflow**: This signal pulses LOW at the end of memory array, indicating the device has been filled and the message has overflowed. The $\overline{OVF}$ output then follows the $\overline{CE}$ input until a PD pulse has reset the device. This pin can be used to cascade several ISD2500 devices together to increase record/playback durations.
$\overline{CE}$	23	2	**Chip Enable**: The $\overline{CE}$ input pin is taken LOW to enable all playback and record operations. The address pins and playback/record pin (P/$\overline{R}$) are latched by the falling edge of $\overline{CE}$. $\overline{CE}$ has additional functionality in the M6 (Push-Button) Operational Mode as described in the Operational Mode section.
PD	24	3	**Power Down**: When neither record nor playback operation, the PD pin should be pulled HIGH to place the part in standby mode (see I_{SB} specification). When overflow ($\overline{OVF}$) pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the memory array. The PD pin has additional functionality in the M6 (Push-Button) Operation Mode as described in the Operational Mode section.
$\overline{EOM}$	25	4	**End-Of-Message**: A nonvolatile marker is automatically inserted at the end of each recorded message. It remains there until the message is recorded over. The $\overline{EOM}$ output pulses LOW for a period of T_{EOM} at the end of each message. In addition, the ISD2500 series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5V. In this case, $\overline{EOM}$ goes LOW and the device is fixed in Playback-only mode. When the device is configured in Operational Mode M6 (Push-Button Mode), this pin provides an active-HIGH signal, indicating the device is currently recording or playing. This signal can conveniently drive an LED for visual indicator of a record or playback operation in process.

<table>
<tr><th rowspan="2">PIN NAME</th><th colspan="2">PIN NO.</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>SOIC/ PDIP</th><th>TSOP</th></tr>
<tr><td>XCLK</td><td>26</td><td>5</td><td>External Clock: The external clock input has an internal pull-down device. The device is configured at the factory with an internal sampling clock frequency centered to ±1 percent of specification. The frequency is then maintained to a variation of ±2.25 percent over the entire commercial temperature and operating voltage ranges. If greater precision is required, the device can be clocked through the XCLK pin as follows:
<table>
<tr><th>Part Number</th><th>Sample Rate</th><th>Required Clock</th></tr>
<tr><td>ISD2560</td><td>8.0 kHz</td><td>1024 kHz</td></tr>
<tr><td>ISD2575</td><td>6.4 kHz</td><td>819.2 kHz</td></tr>
<tr><td>ISD2590</td><td>5.3 kHz</td><td>682.7 kHz</td></tr>
<tr><td>ISD25120</td><td>4.0 kHz</td><td>512 kHz</td></tr>
</table>
These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. If the XCLK is not used, this input must be connected to ground.</td></tr>
<tr><td>P/$\overline{R}$</td><td>27</td><td>6</td><td>Playback/Record: The P/$\overline{R}$ input pin is latched by the falling edge of the $\overline{CE}$ pin. A HIGH level selects a playback cycle while a LOW level selects a record cycle. For a record cycle, the address pins provide the starting address and recording continues until PD or $\overline{CE}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a record cycle is terminated by pulling PD or $\overline{CE}$ HIGH, then End-Of-Message ($\overline{EOM}$) marker is stored at the current address in memory. For a playback cycle, the address inputs provide the starting address and the device will play until an $\overline{EOM}$ marker is encountered. The device can continue to pass an $\overline{EOM}$ marker if $\overline{CE}$ is held LOW in address mode, or in an Operational Mode. (See Operational Modes section)</td></tr>
</table>

8. TIMING DIAGRAMS

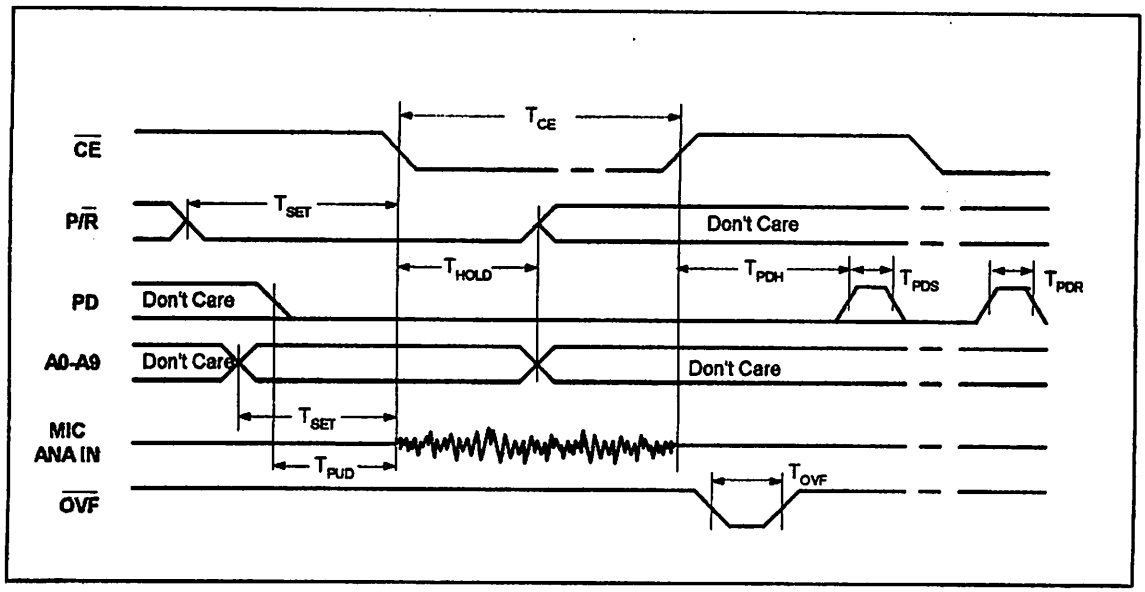


FIGURE 1: RECORD

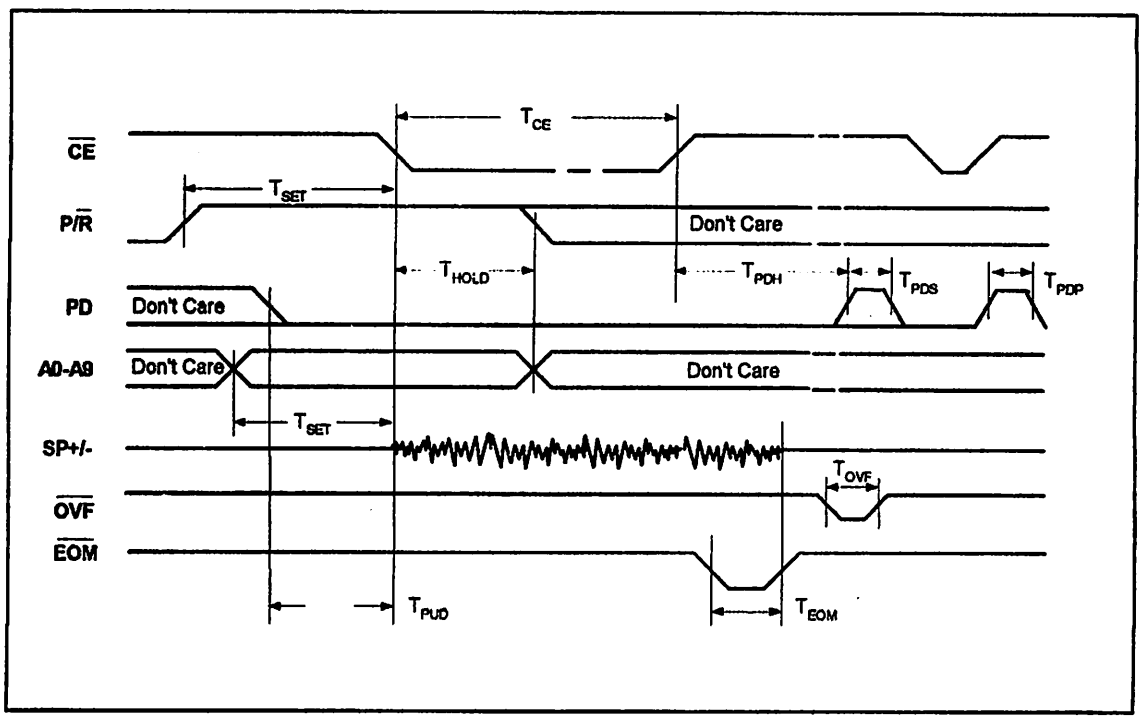


FIGURE 2: PLAYBACK

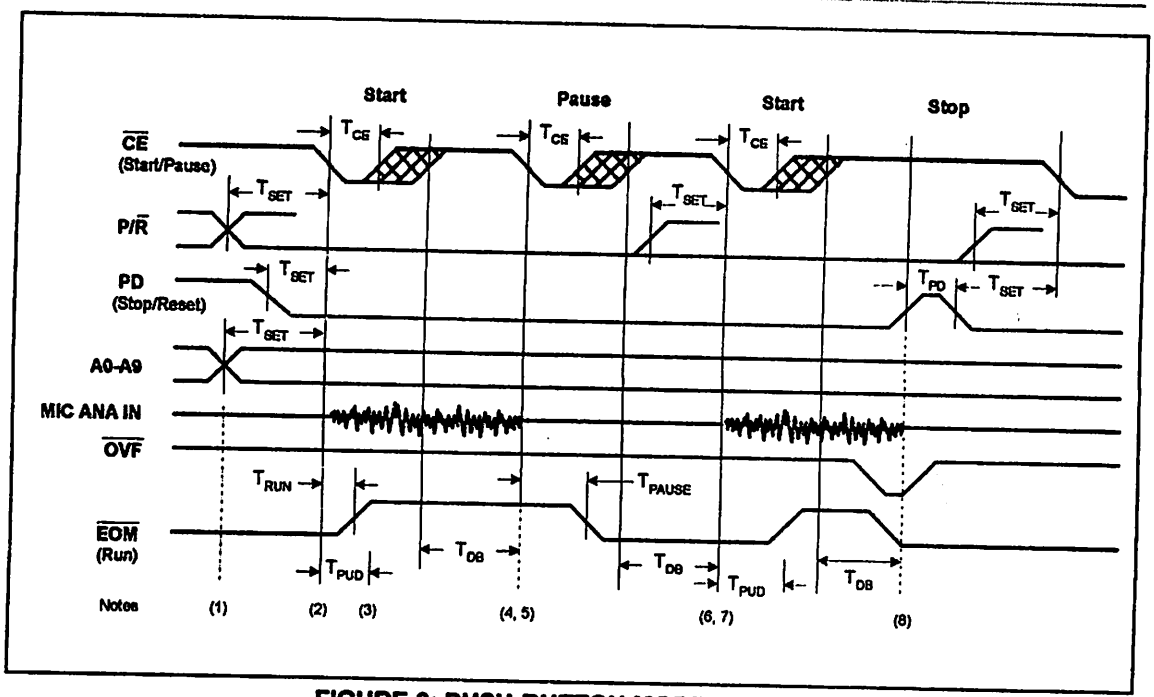


FIGURE 3: PUSH-BUTTON MODE RECORD

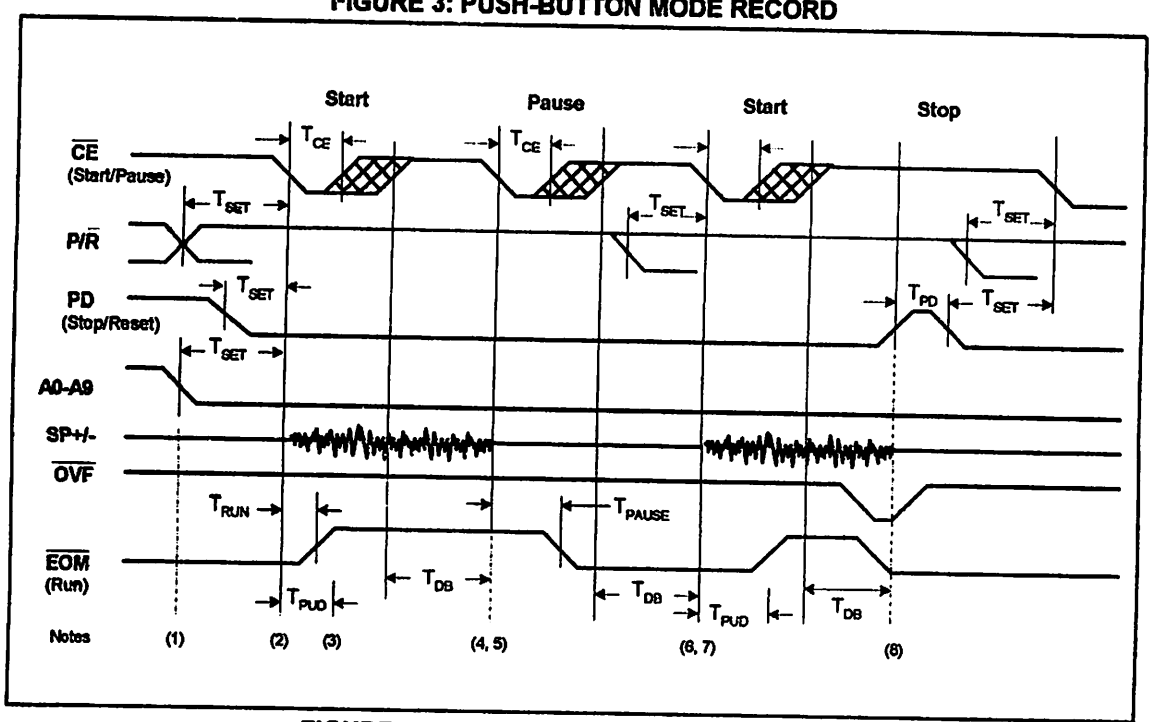


FIGURE 4: PUSH-BUTTON MODE PLAYBACK

Notes for Push-Button modes:

1. A9, A8, and A6 = 1 for push-button operation.
2. The first $\overline{CE}$ LOW pulse performs a start function.
3. The part will begin to play or record after a power-up delay T_{PUD}.
4. The part must have $\overline{CE}$ HIGH for a debounce period T_{DB} before it will recognize another falling edge of $\overline{CE}$ and pause.
5. The second $\overline{CE}$ LOW pulse, and every even pulse thereafter, performs a Pause function.
6. Again, the part must have $\overline{CE}$ HIGH for a debounce period T_{DB} before it will recognize another falling edge of $\overline{CE}$, which would restart an operation. In addition, the part will not do an internal power down until $\overline{CE}$ is HIGH for the T_{DB} time.
7. The third $\overline{CE}$ LOW pulse, and every odd pulse thereafter, performs a Resume function.
8. At any time, a HIGH level on PD will stop the current function, reset the address counter, and power down the device.

10. ELECTRICAL CHARACTERISTICS

10.1. PARAMETERS FOR PACKAGED PARTS

TABLE 8: DC PARAMETERS – Packaged Parts

PARAMETER	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	V_{CC} - 0.4			V	I_{OH} = -10 µA
$\overline{OVF}$ Output High Voltage	V_{OH1}	2.4			V	I_{OH} = -1.6 mA
$\overline{EOM}$ Output High Voltage	V_{OH2}	V_{CC} – 1.0	V_{CC} - 0.8		V	I_{OH} = -3.2 mA
V_{CC} Current (Operating)	I_{CC}		25	30	mA	R_{EXT} = ∞ [3]
V_{CC} Current (Standby)	I_{SB}		1	10	µA	[3]
Input Leakage Current	I_{IL}			±1	µA	
Input Current HIGH w/Pull Down	I_{ILPD}			130	µA	Force V_{CC} [4]
Output Load Impedance	R_{EXT}	16			Ω	Speaker Load
Preamp Input Resistance	R_{MIC}	4	9	15	KΩ	MIC and MIC REF Pins
AUX IN Input Resistance	R_{AUX}	5	11	20	KΩ	
ANA IN Input Resistance	$R_{ANA\ IN}$	2.3	3	5	KΩ	
Preamp Gain 1	A_{PRE1}	21	24	26	dB	AGC = 0.0V
Preamp Gain 2	A_{PRE2}		-15	5	dB	AGC = 2.5V
AUX IN/SP+ Gain	A_{AUX}		0.98	1.0	V/V	
ANA IN to SP+/- Gain	A_{ARP}	21	23	26	dB	
AGC Output Resistance	R_{AGC}	2.5	5	9.5	KΩ	

Notes:

[1] Typical values @ T_A = 25° and V_{CC} = 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} connected together.

[4] XCLK pin only.

11. TYPICAL APPLICATION CIRCUIT

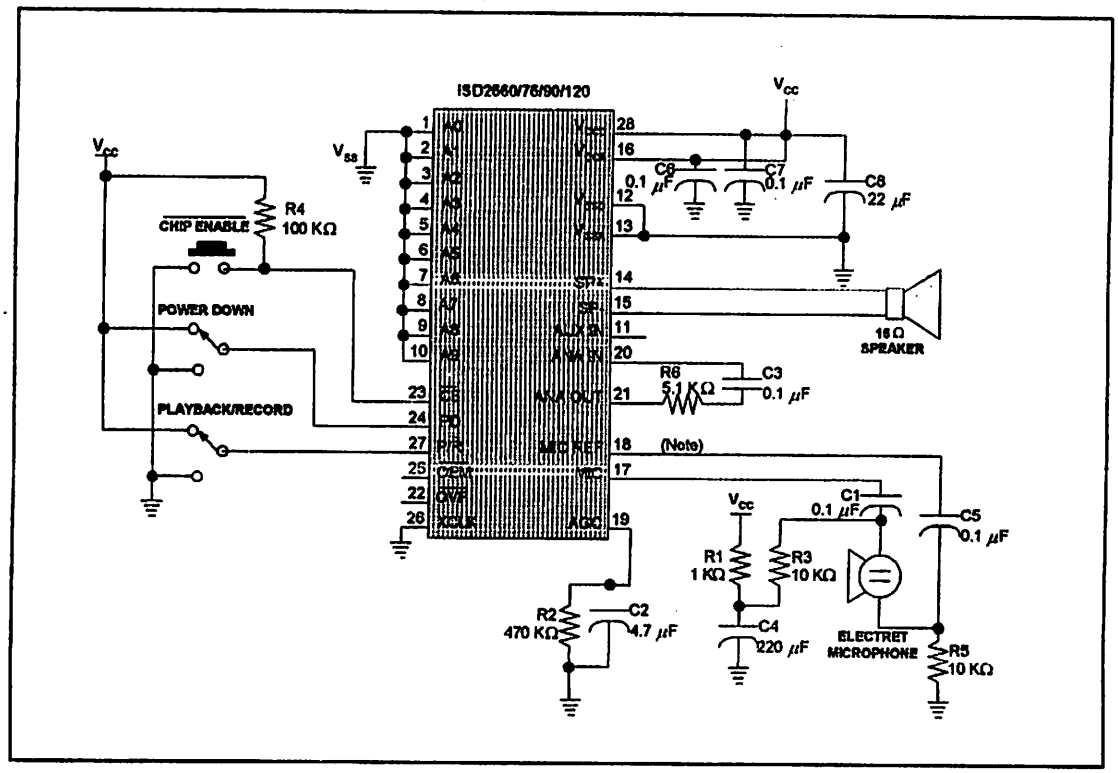


FIGURE 5: DESIGN SCHEMATIC

Note: If desired, pin 18 (PDIP package) may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage. Additional design example schematics are provided below.

Winbond Electronics Corp.

The contents of this document are provided only as a guide for the applications of Winbond products. Winbond makes no representation or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to discontinue or make changes to specifications and product descriptions at any time without notice. No license, whether express or implied, to any intellectual property or other right of Winbond or others is granted by this publication. Except as set forth in Winbond's Standard Terms and Conditions of Sale, Winbond assumes no liability whatsoever and disclaims any express or implied warranty of merchantability, fitness for a particular purpose or infringement of any intellectual property.

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipments intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental injury could occur.

Application examples and alternative uses of any integrated circuit contained in this publication are for illustration only and Winbond makes no representation or warranty that such applications shall be suitable for the use specified.

ISD® and ChipCorder® are trademarks of Winbond Electronics Corporation.

The 100-year retention and 100K record cycle projections are based upon accelerated reliability tests, as published in the Winbond Reliability Report, and are neither warranted nor guaranteed by Winbond.

Information contained in this ISD® ChipCorder® data sheet supersedes all data for the ISD ChipCorder products published by ISD® prior to August, 1998.

This data sheet and any future addendum to this data sheet is(are) the complete and controlling ISD® ChipCorder® product specifications. In the event any inconsistencies exist between the information in this and other product documentation, or in the event that other product documentation contains information in addition to the information in this, the information contained herein supersedes and governs such other information in its entirety.

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441797
http://www.winbond-usa.com/

Winbond Electronics (Shanghai) Ltd.
27F, 299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62356998

Taipei Office
9F, No. 480, Pueiguang Rd.
Neihu District
Taipei, 114 Taiwan
TEL: 886-2-81777168
FAX: 886-2-87153579

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG. 3-7-18
Shinyokohama Kohokuku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
KowLoon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

LIQUID CRYSTAL DISPLAY MODULE

M 1 6 3 2

USER MANUAL

Seiko Instruments Inc.

PREFACE

This manual describes technical informations on functions and instructions of M1632 from Seiko Instruments Inc. Please read this instruction manual carefully to understand all the module functions and make the best use of them. Description details may be changed without notice.

Revision Record

Edition	Revision	Date
1	Original	April 1985
2	Completely revised	Jan. 1987

1. GENERAL

1.1 General

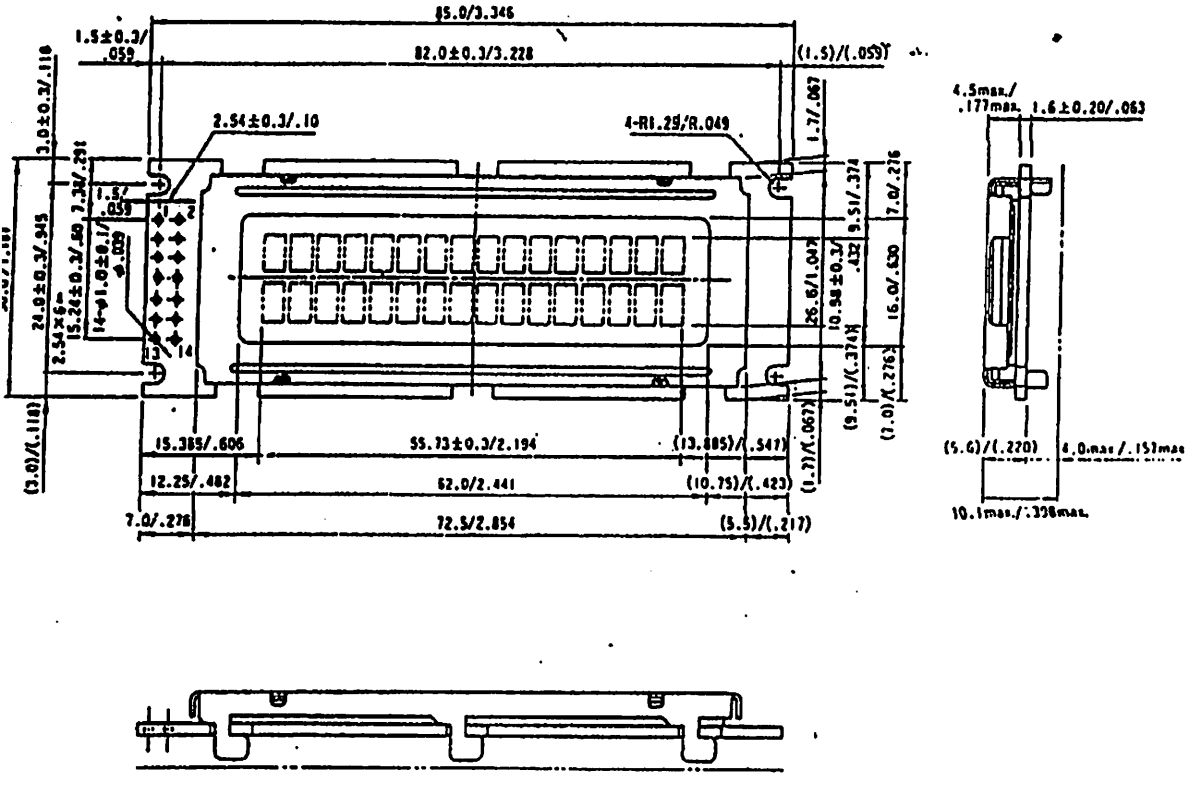
The M1632 is a low-power-consumption dot-matrix liquid crystal display (LCD) module with a high-contrast wide-view TN LCD panel and a CMOS LCD drive controller built in. The controller has a built-in character generator ROM/RAM, and display data RAM. All the display functions are controlled by instructions and the module can easily be interfaced with an MPU. This makes the module applicable to a wide range of purposes including terminal display units for microcomputers and display units for measuring gages.

1.2 Features

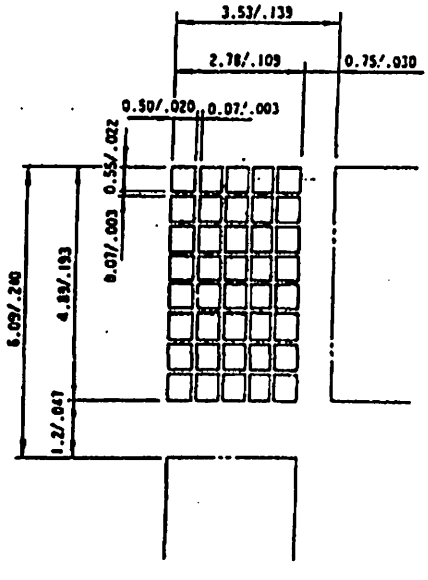
- 16-character, two-line TN liquid crystal display of 5 x 7 dot matrix + cursor
- Duty ratio: 1/16
- Character generator ROM for 192 character types.
  (character font: 5 x 7 dot matrix)
- Character generator RAM for eight character types (program write)
  (character font: 5 x 7 dot matrix)
- 80 x 8 bit display data RAM (80 characters maximum)
- Interface with four-bit and eight-bit MPUs possible
- Display data RAM and character generator RAM readable from MPU
- Many instruction functions

  Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, and Display Shift
- Built-in oscillator circuit
- +5 V single power supply
- Built-in automatic reset circuit at power-on
- CMOS process
- Operating temperature range: 0°C to 50°C

1.3 Dimensions Diagram



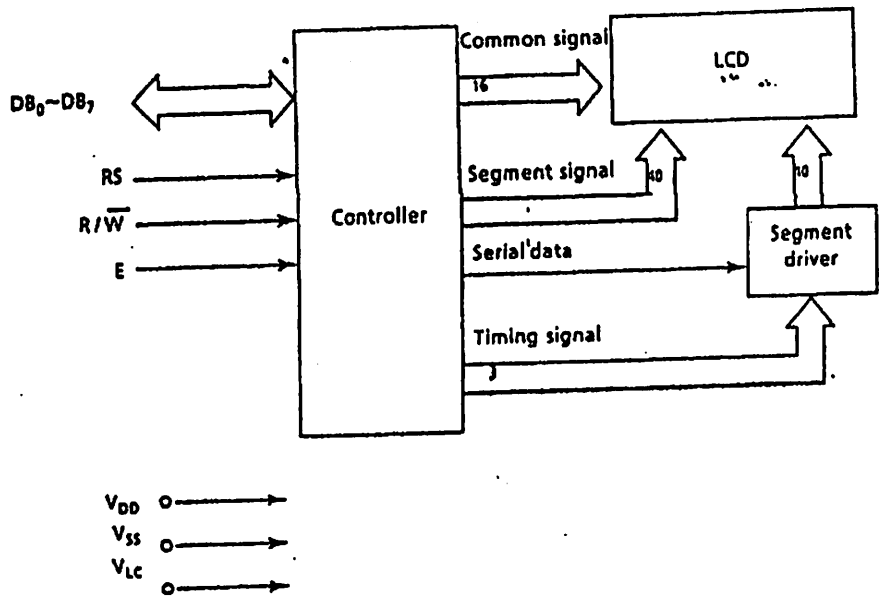
Unit : mm/inch
General tolerance : ± 0.5 mm



No.	Symbol	Level	Function	
1	Vss	-	Power Supply	0V (GND)
2	Vcc	-		5V ±10%
3	Vcc	-		for LCD Drive
4	RS	H/L	H: Data Input L: Instruction Input	
5	R/W	H/L	H:READ L:WRITE	
6	E	H, ↓	Enable Signal	
7	DB0	H/L	Data Bus	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+ BL	-	Back Light Supply	4 - 4.2V 50-200mA
16	V- BL	-		0V (GND)

Figure 1 Dimensions diagran

1.4 Block Diagram



1.5 Absolute Maximum Ratings

V_{SS} = 0 V

Item	Symbol	Standard	Unit	Remarks
Power supply voltage	V_{DD}	− 0.3 to + 7.0	V	
	V_{LC}	V_{DD} − 13.5 to V_{DD} + 0.3	V	
Input voltage	V_{in}	− 0.3 to V_{DD} + 0.3,	V	
Operating temperature	T_{opr}	0 to + 50	°C	
Storage temperature	T_{stg}	− 20 to + 60	°C	At 50% RH

.6 Electrical Characteristics

V_{DD} = 5 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Conditions	Standard			Unit
				Min.	Typ.	Max.	
Input voltage	High	V_{IH1}		2.2	–	V_{DD}	V
	Low	V_{IL1}		0	–	0.6	V
Output voltage (TTL)	High	V_{OH1}	$-I_{OH}$ = 0.205 mA	2.4	–	–	V
	Low	V_{OL1}	I_{OL} = 1.2 mA	–	–	0.4	V
Output voltage (CMOS)	High	V_{OH2}	$-I_{OH}$ = 0.04 mA	0.9V_{DD}	–	–	V
	Low	V_{OL2}	I_{OL} = 0.04 mA	–	–	0.1V_{DD}	V
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		$-V_{LC}$	V_{DD} = 5 V, T_A = 25°C	–	0.25	–	V
Current consumption		I_{DD}		–	2.0	3.0	mA
		I_{LC}	V_{LC} = 0.25V	–	–	1.0	mA
Clock oscillation freq.		f_{osc}	Resistance oscillation	190	270	350	kHz

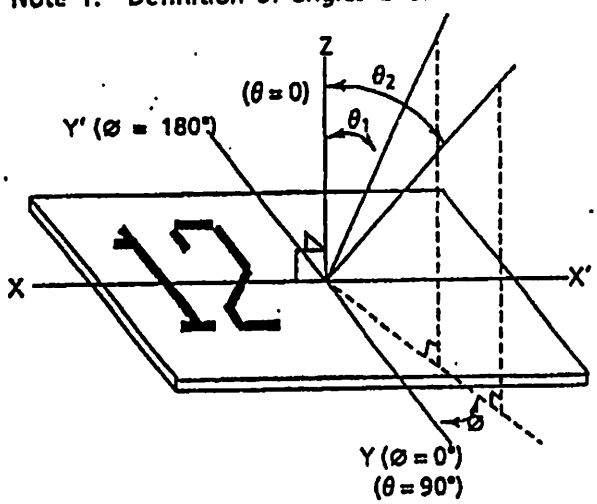
1.7 Optical Characteristics

1.7.1 Optical characteristics

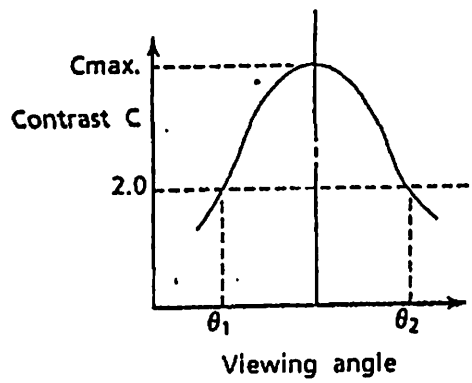
Maximum viewing angle: 6 o'clock (ϕ = 0°)
T_A = 25°C, V_{opr} = 4.75 V

Item	Symbol	Conditions	Min.	Typ.	Max.	Remarks
Viewing angle	$\theta_2 - \theta_1$	$C \geq 2.0$, $\phi = 0°$	35	–	–	See Notes 1 and 2.
Contrast	C	$\theta = 25°$, $\phi = 0°$	5	8	–	See Note 3.
Rise time	t_{on}	$\theta = 25°$, $\phi = 0°$	–	60 ms	70 ms	See Note 4.
Fall time	t_{off}	$\theta = 25°$, $\phi = 0°$	–	150 ms	170 ms	See Note 4.

Note 1: Definition of angles ϕ and θ

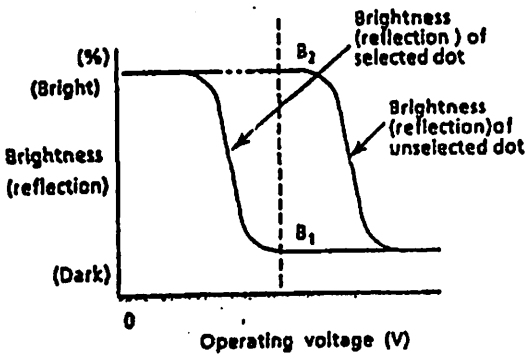


Note 2: Definition of viewing angles θ_1 and θ_2

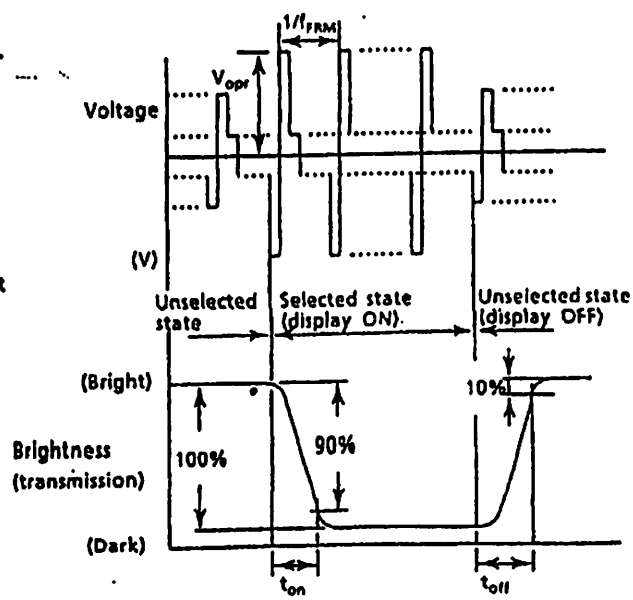


Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



V_{opr} : Operating voltage (V)
f_{FRM} : Frame frequency (Hz)
t_{on} : Response time (rise)(ms)
t_{off} : Response time (fall)(ms)

1.7.2 Recommended operating voltage

The viewing angle and screen contrast of the LCD panel can be varied by changing the liquid crystal operating voltage (V_{opr}), that is V_{LC}.

The optical characteristics is influenced by an ambient temperature. The recommended value of V_{opr} for an ambient temperatures are shown below.

Temperature (℃)	0	10	25	40	50
Voltage V_{opr} (V)	5.00	4.90	4.75	4.60	4.50

$V_{opr} = V_{DD} - V_{LC}$

OPERATING INSTRUCTIONS

2.1 Terminal Functions

Table 1 Terminal functions

Signal name	No. of terminals	I/O	Destination	Function
DB_0 to DB_3	4	I/O	MPU	Tristate bidirectional lower four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. If the interface data is 4 bits, the signals are not used.
DB_4 to DB_7	4	I/O	MPU	Tristate bidirectional upper four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. DB_7 is also used as a busy flag.
E	1	Input	MPU	Operation start signal: The signal activates data write or read.
R/$\overline{W}$	1	Input	MPU	Read (R) and Write ($\overline{W}$) selection signals 0 : Write 1 : Read
RS	1	Input	MPU	Register selection signals 0 : Instruction register (Write) Busy flag and address counter (Read) 1 : Data register (Write and Read)
V_{LC}	1	–	Power supply	Power supply terminal for driving liquid crystal display: The screen contrast can be varied by changing V_{LC}.
V_{DD}	1	–	Power supply	+5 V
V_{SS}	1	–	Power supply	Ground terminal: 0 V

2.2 Basic Operations

2.2.1 Registers

The controller has two kinds of eight-bit registers: the instruction register (IR) and the data register (DR). They are selected by the register select (RS) signal as shown in Table 2.

The IR stores instruction codes such as Display Clear and Cursor Shift, and the address information of display data RAM (DD RAM) and character generator RAM (CG RAM). They can be written from the MPU, but cannot be read to the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM, or read from DD RAM or CG RAM. When data is written into DD RAM or CG RAM from the MPU, the data in the DR is automatically written into DD RAM or CG RAM by internal operation. However, when data is read from DD RAM or CG RAM, the necessary data address is written into the IR. The specified data is read out to the DR and then the MPU reads it from the DR. After the read operation, the next address is set and DD RAM or CG RAM data at the address is read into the DR for the next read operation.

Table 2 Register selection

RS	$R/\overline{W}$	Operation
0	0	IR selection, IR write. Internal operation : Display clear
0	1	Busy flag (DB_7) and address counter (DB_0 to DB_6) read
1	0	DR selection, DR write. Internal operation : DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation : DD RAM or CG RAM to DR

2.2.2 Busy flag (BF)

The flag indicates whether the module is ready to accept the next instruction. As shown in Table 2, the signal is output to DB_7 if RS = 0 and $R/\overline{W}$ = 1. If the value is 1, the module is working internally and the instruction cannot be accepted. If the value is 0, the next instruction can be written. Therefore, the flag status needs to be checked before executing an instruction. If an instruction is executed without checking the flag status, wait for more than the execution time shown by 2.4 Instruction Outline.

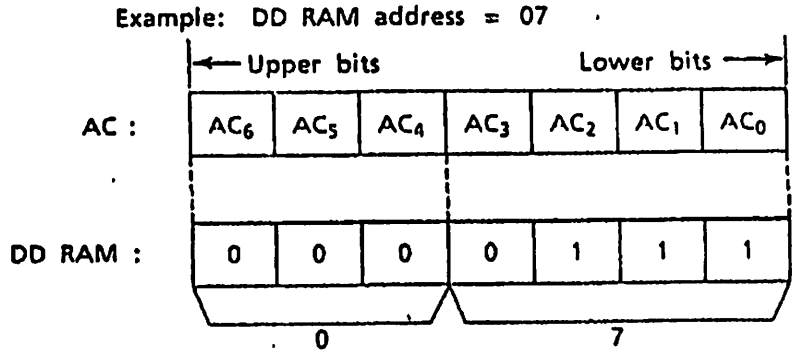
2.2.3 Address counter (AC)

The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB_0 to DB_6 as shown in Table 2 if RS = 0 and $R/\overline{W} = 1$.

2.2.4 Display data RAM (DD RAM)

DD RAM has a capacity of up to 80 × 8 bits and stores display data of 80 eight-bit character codes. Some storage areas of DD RAM which are not used for display can be used as general data RAM.

A DD RAM address to be set in the AC is expressed in hexadecimal form as follows.



00H to 0FH of the DD RAM address is set in the line 1, and 40H to 4FH in the line 2.

Note : The addresses in the digit 16 of line 1 and the digit 1 of line 2 are not consecutive.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM address
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

If the display is shifted, DD RAM address 00_H to 27_H are displayed in line 1 and 40_H to 67_H in line 2. The following figures are examples of display shifts.

*Left shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	DD RAM address
Line 2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	

*Right shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	DD RAM address
Line 2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

2.5 Character generator ROM (CG ROM)

Character generator ROM generates 192 types of 5 x 7 dot-matrix character patterns from eight-bit character codes.

Table 3 shows the correspondence between the CG ROM character codes and character patterns.

2.6 Character generator RAM (CG RAM)

CG RAM is used to create character patterns freely by programming. Eight types of character patterns can be written.

Table 4 shows the character patterns created from CG RAM addresses and data. To display a created character pattern, the character code in the left column of the table is written into DD RAM corresponding to the display position (digit). The areas not used for display are available as general data RAM.

Table 3 Correspondence between character codes and character patterns

Upper bit 4 bit / Lower bit 4 bit	0 0000	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	1010	1011	1100	1101	1110	1111
×××0000	CG RAM (1)												
×××0001	(2)												
×××0010	(3)												
×××0011	(4)												
×××0100	(5)												
×××0101	(6)												
×××0110	(7)												
×××0111	(8)												
×××1000	(1)												
×××1001	(2)												
×××1010	(3)												
×××1011	(4)												
×××1100	(5)												
×××1101	(6)												
×××1110	(7)												
×××1111	(8)												

Table 4 Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data)

Character code (DD RAM data) 7 6 5 4 3 2 1 0 ←Upper bit Lower bit→	CG RAM address 5 4 3 ←Upper bit 2 1 0 Lower bit→	Character pattern (CG RAM data) 7 6 5 4 3 2 1 0 ←Upper bit Lower bit→
0 0 0 0 * 0 0 0	0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1
0 0 0 0 * 0 0 1	0 0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1
		0 0 0 0 0 1
0 0 0 0 * 1 1 1	1 1 1	1 0 0 1 0 1 1 1 0 1 1 1

Example of character pattern (R)

← Cursor position

Example of character pattern (¥)

Notes: • In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display.

• Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).

• CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is changed to 1, one bit lights, regardless of the cursor.

The character pattern column positions correspond to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.

When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00_H and 08_H select the same character.

2.3 Timing Characteristics

2.3.1 Write timing characteristics

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		t_{CYCE}	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er}, t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$ — E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data setup time		t_{DSW}	195	–	ns
Data hold time		t_H	10	–	ns

Write operation

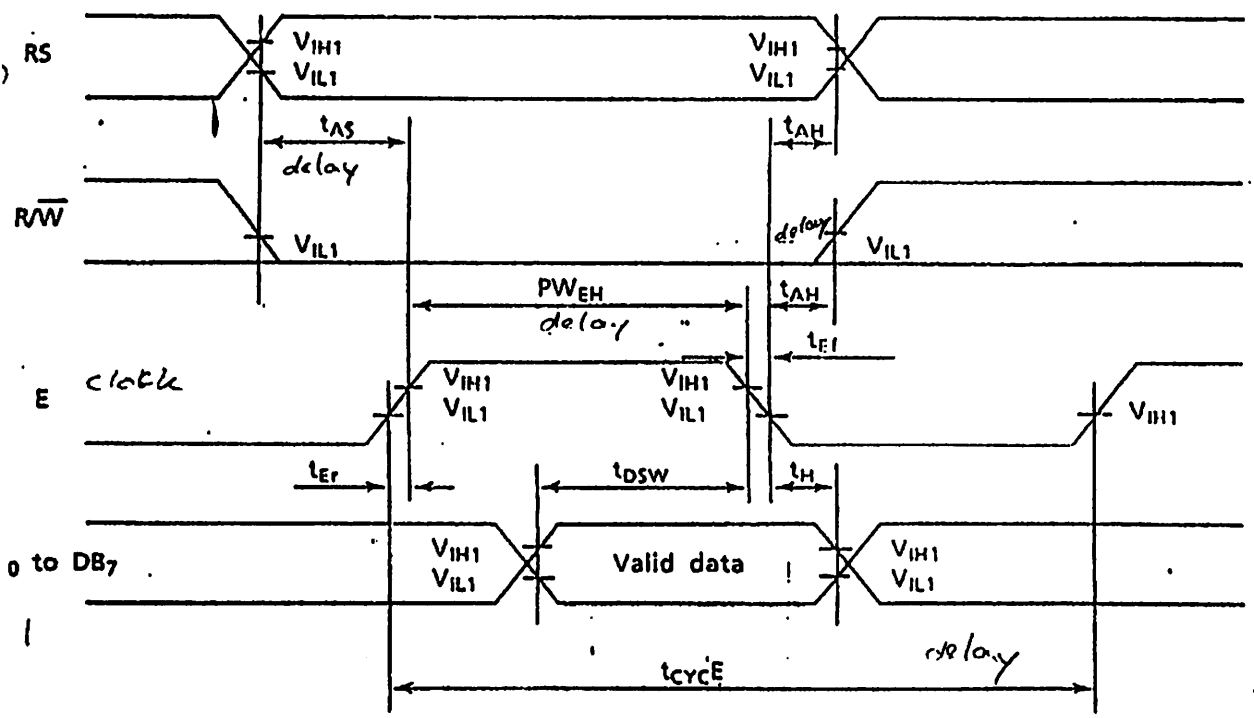


Figure 3 Data write from MPU to module

2.3.2 Read timing characteristics

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		t_{CYCE}	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er},t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$—E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data delay time		t_{DDR}	–	320	ns
Data hold time		t_{H}	20	–	ns

Read operation

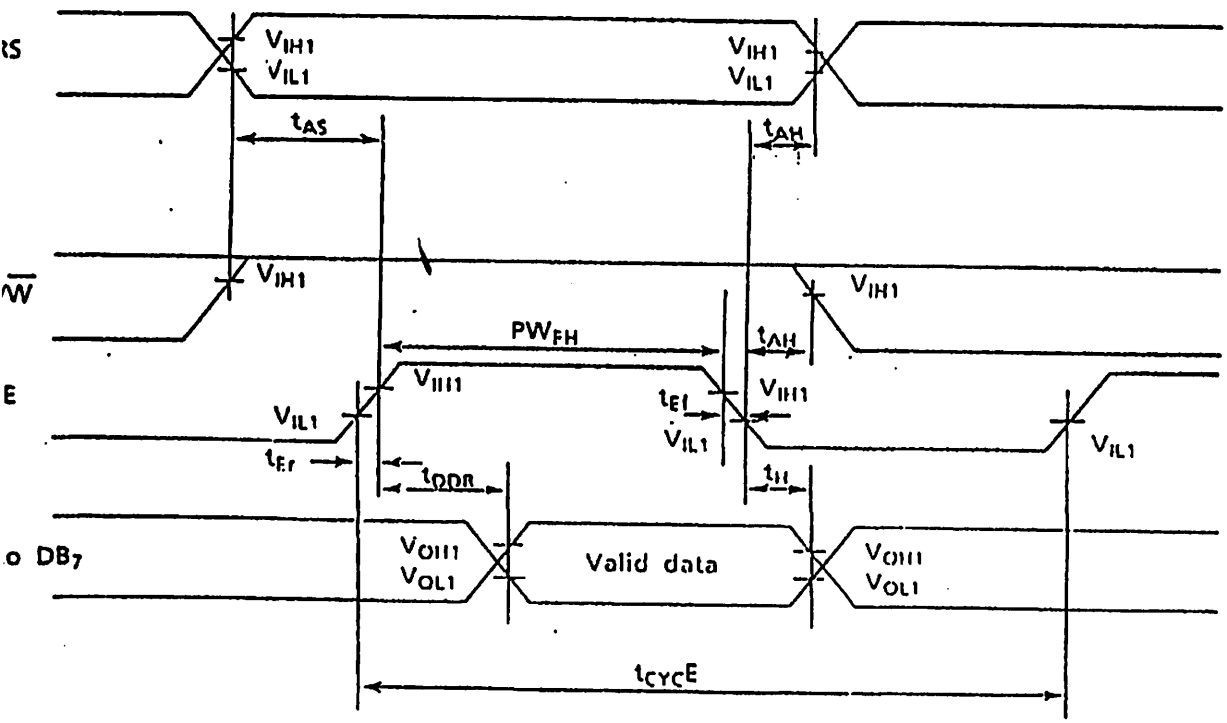


Figure 4 Data read from module to MPU

Instruction Outline

Table 5 List of instructions

Instruction	Code										Function	Execution time
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Display clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns cursor to home position (address 0)	1.64 ms
Cursor Home	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change.	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets direction of cursor movement and whether display will be shifted when data is written or read	40 µs
Display ON / OFF Control	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)	40 µs
Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents	40 µs
Function Set	0	0	0	0	1	DL	1	*	*	*	Sets interface data length (DL)	40 µs
CG RAM Address Set	0	0	0	1	A_{CG}						Sets CG RAM address to start transmitting or receiving CG RAM data	40 µs
DD RAM Address Set	0	0	1	A_{DD}							Sets DD RAM address to start transmitting or receiving DD RAM data	40 µs
BF/Address Read	0	1	BF	AC							Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM)	0 µs
Data Write to CG RAM or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	40 µs
Data Read from CG RAM or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM	40 µs

nvalid bit
: CG RAM address
: DD RAM address

I/D = 1 : Increment
I/D = 0 : Decrement

S = 1 : Display shift
S = 0 : No display shift

D = 1 : Display ON
D = 0 : Display OFF

C = 1 : Cursor ON
C = 0 : Cursor OFF

B = 1 : Blink ON
B = 0 : Blink OFF

S/C = 1 : Display shift
S/C = 0 : Cursor movement

R/L = 1 : Right shift
R/L = 0 : Left shift

DL = 1 : 8 bits
DL = 0 : 4 bits

BF = 1 : Internal operation in progress
BF = 0 : Instruction can be accepted

nstruction Details

Display Clear

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Display Clear clears all display and returns cursor to home position (address 0).

Space code 20 (hexadecimal) is written into all the addresses of DD RAM, and DD RAM address 0 is set to the AC. If shifted, the display returns to the original position. After execution of the Display Clear instruction, the entry mode is incremented.

Note : When executing the Display Clear instruction, follow the restrictions listed in Table 6.

Cursor Home

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	1	*

* : Invalid bit

Cursor Home returns cursor to home position (address 0).

DD RAM address 0 is set to the AC. The cursor returns to the home position. If shifted, the display returns to the original position. The DD RAM contents do not change. If the cursor or blinking is ON, it returns to the left side.

Note : When executing the Cursor Home instruction, follow the restrictions listed in Table 6.

Table 6 Restrictions on execution of Display Clear and Cursor Home instructions

Conditions of use	Restrictions
When executing the Display Clear or Cursor Home instruction when the display is shifted (after execution of Display Shift instruction)	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{osc}$* second after the first execution. Example: 1.5 ms, 3 ms, 4.5 ms for f_{osc} = 270 kHz *f_{osc}: Oscillation frequency
When 23_H, 27_H, 63_H, or 67_H is used as a DD RAM address to execute Cursor Home instruction	Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)

3) Entry Mode Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry Mode Set sets the direction of cursor movement and whether display will be shifted.

I/D : The DD RAM address is incremented or decremented by one when a character code is written into or read from DD RAM. This is also true for writing into or reading from CG RAM.

When I/D = 1, the address is incremented by one and the cursor or blink moves to the right.

When I/D = 0, the address is decremented by one and the cursor or blink moves to the left.

S : If S = 1, the entire display is shifted either to the right or left for writing into DD RAM. The cursor position does not change, only the display moves. There is no display shift for reading from DD RAM.

When S = 1 and I/D = 1, the display shifts to the left.
When S = 1 and I/D = 0, the display shifts to the right.

If S = 0, the display does not shift.

4) Display ON/OFF Control

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display ON/OFF Control turns the total display and the cursor ON and OFF, and makes the cursor position start blinking. Cursor ON/OFF and blinking is done at the column indicated by the specified DD RAM address by the AC.

D : When D = 1, the display is turned ON.
When D = 0, the display is turned OFF.
If D = 0 is used, display data remains in DD RAM. Change 0 to 1 to display data.

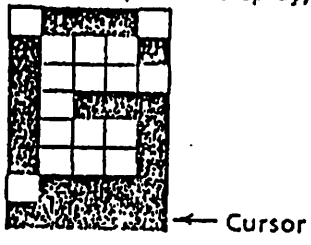
C : When C = 1, the cursor is displayed.
When C = 0, the cursor is not displayed.

The cursor is displayed in the dot line below the 5 x 7 dot-matrix character fonts. If the cursor is OFF, display data is written into DD RAM in the order specified by I/D.

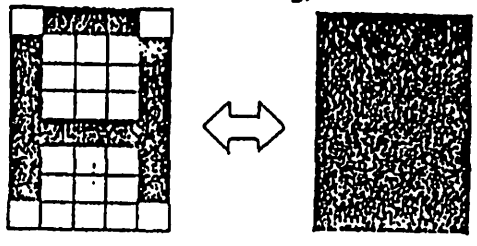
B : When B = 1, the character at the cursor position starts blinking.
When B = 0, it does not blink.

For blinking, all-black dots and the character are switched about every 0.4 seconds. The cursor and blinking can be set at the same time.

Example: C = 1 (cursor display)



B = 1 (blinking)



i) Cursor/Display Shift

	RS	R/$\overline{W}$	DD_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* :Invalid bit

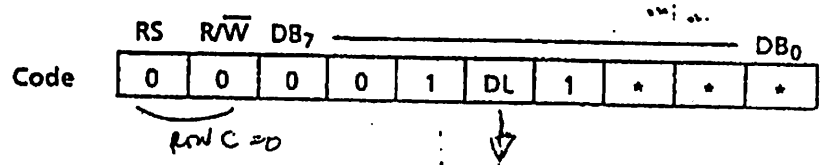
Cursor/Display Shift moves the cursor and shifts the display without changing the DD RAM contents.

The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. Since the DD RAM capacity is 40-character and two lines, the cursor is shifted from digit 40 of line 1 to digit 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. Therefore, the display pattern of line 2 is not shifted to line 1.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one).
0	1	The cursor position is shifted to the right (the AC increments one).
1	0	The entire display is shifted to the left with the cursor.
1	1	The entire display is shifted to the right with the cursor.

Note: If only display shift is done, the AC contents do not change.

Function Set



Function Set sets the interface data length.

DL : Interface data length

When DL = 1, the data length is set at eight bits (DB_7 to DB_0).

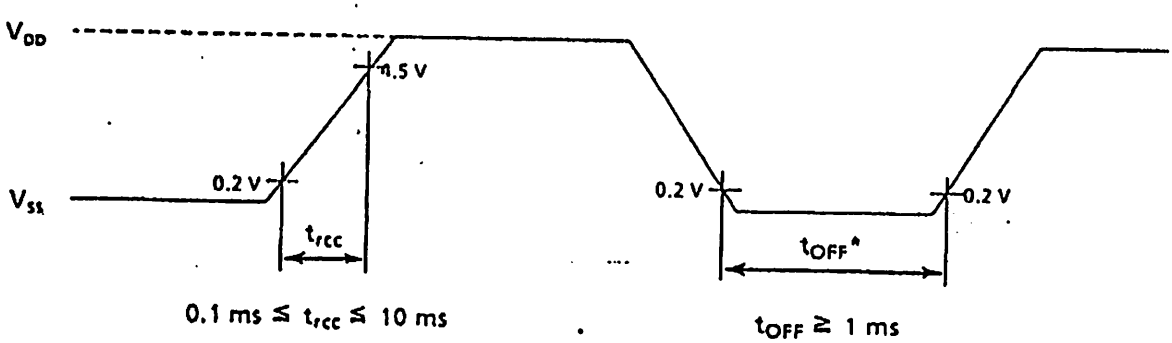
When DL = 0, the data length is set at four bits (DB_7 to DB_4).

The upper four bits are transferred first, then the lower four bits follow.

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

Remarks: Initialization

The system is automatically initialized at power-on if the following power supply conditions are satisfied.



*t_{OFF}: Time when power supply is OFF if cut instantaneously or turned ON and OFF repeatedly

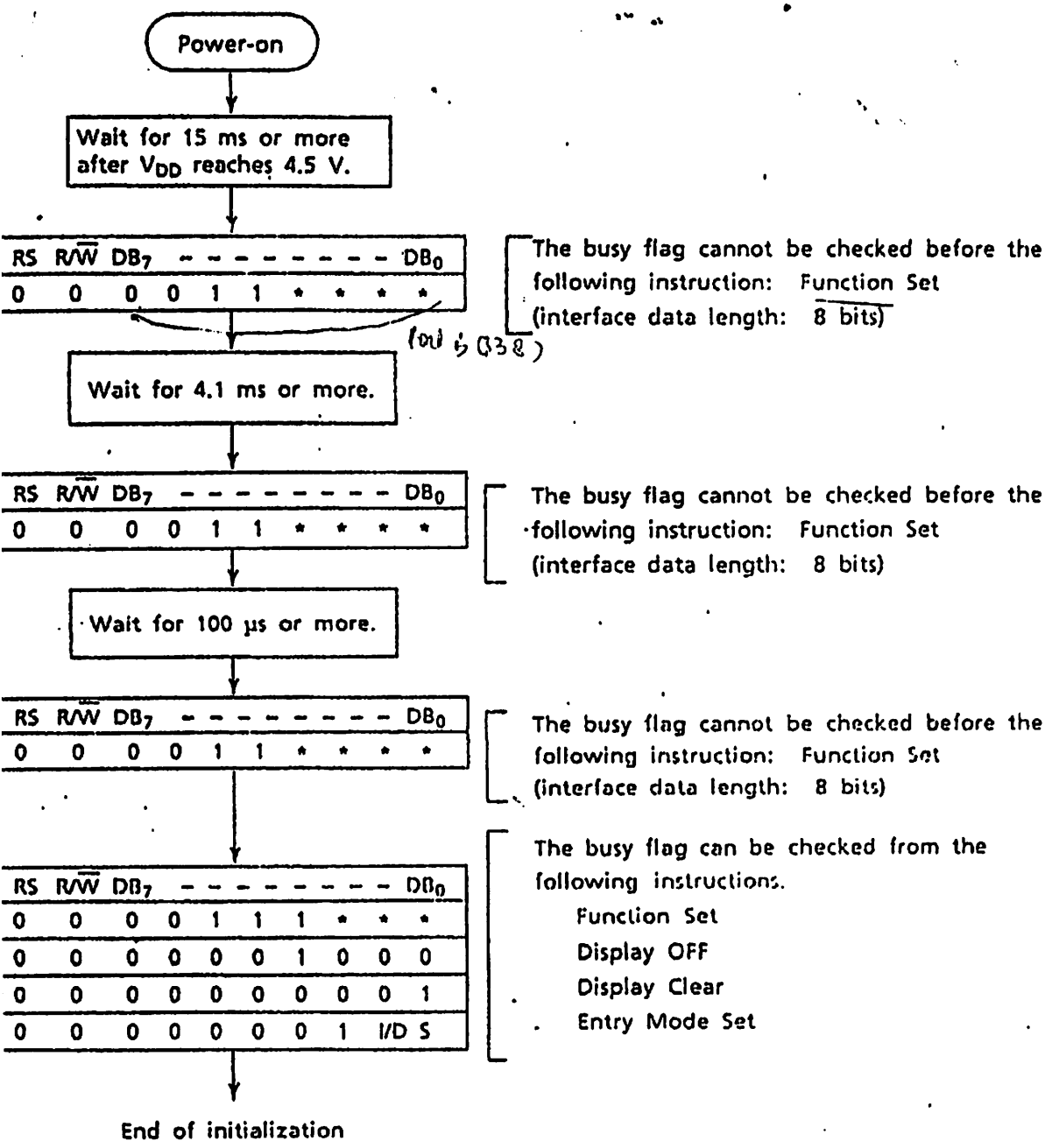
The following instructions are executed for initialization.

- 5 x 7 dot-matrix character font: 1/8 duty
- Display clear
- Function Set — DL = 1: Interface data length: 8 bits
- Display ON/OFF Control — D = 0: Display OFF; C = 0: Cursor OFF; B = 0: Blink OFF
- Entry mode — I/O = 1: Increment; S = 0: No display shift

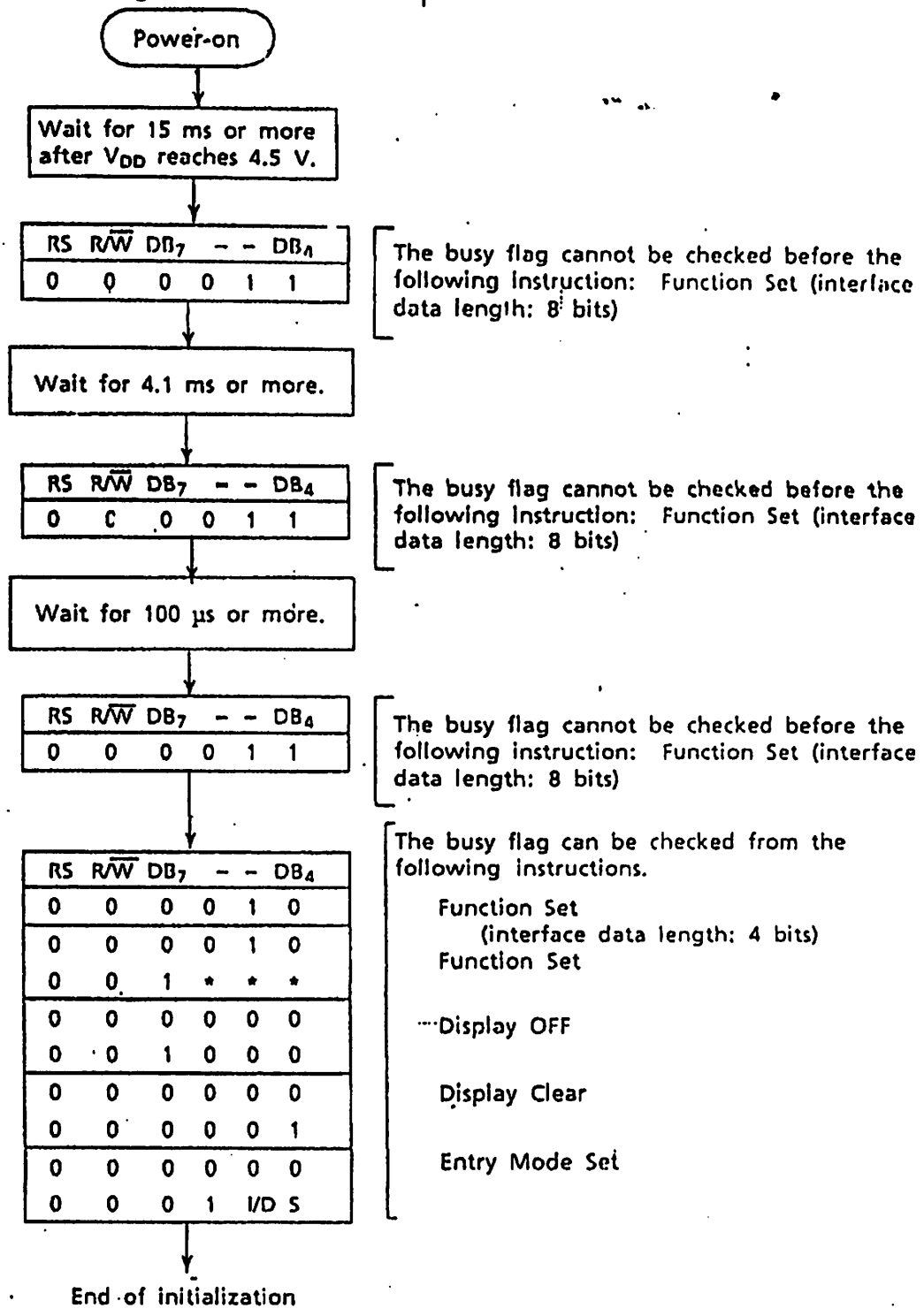
Since the condition is not suitable for the M1632, further function setting is necessary.

If automatic initialization is not executed because the above power supply conditions are not satisfied, use the instruction from next page on.

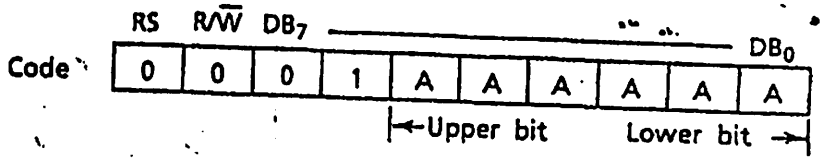
Interface data length : Eight bits



Interface data length: Four bits

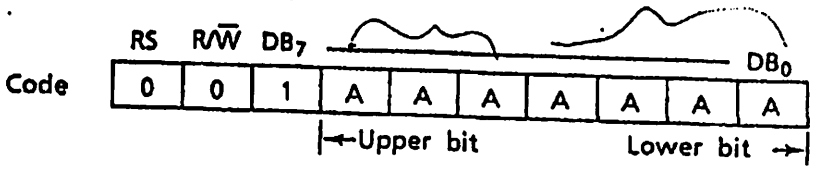


) CG RAM Address Set



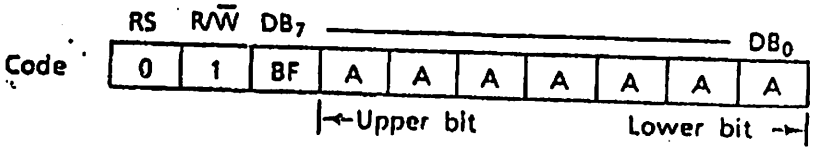
CG RAM addresses expressed as binary AAAAAA are set to the AC. Then data in CG RAM is written from or read to the MPU.

) DD RAM Address Set



DD RAM addresses expressed as binary AAAAAAA are set to the AC. Then data in DD RAM is written from or read to the MPU. The addresses used for display in line 1 (AAAAAAA) are 00_H to 27_H and those for line 2 (AAAAAAA) are 40_H to 67_H.

Busy Flag/Address Read



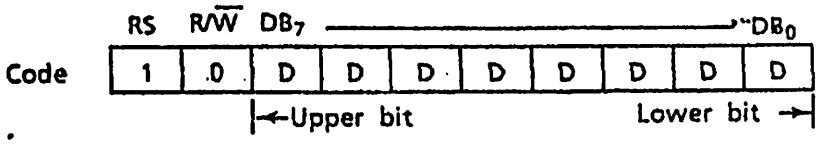
The BF signal is read out, indicating that the module is working internally because of the previous instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

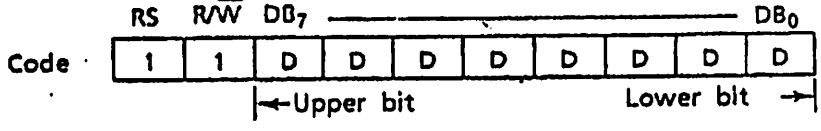
Therefore, make sure that BF = 0 before writing the next instruction. The AC values of binary AAAAAAA are read out at the same time as reading the busy flag. The AC addresses are used for both CG RAM and DD RAM but the address set before execution of the instruction determines which address is to be used.

0) Data Write to CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is written into CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

1) Data Read from CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. In addition, either instruction (7) or (8) must be executed immediately before this instruction. If no address set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.
After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

Note : The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

Correct data is read out under the following conditions.

- An address set instruction is executed immediately before readout.
- For DD RAM, the Cursor Shift instruction is executed immediately before readout.
- The second, or later, instruction is executed in consecutive execution of read instructions.

Examples of Instruction Use

1) Interface data length: Eight bits

Instruction	Display	Operation
Power-on RS: — R/W: — DB7 — DB0: —		The built-in reset circuit initializes the module.
Function Set ✓ RS: 0 R/W: 0 DB7 — DB0: 0 0 1 1 1 * * *		The interface data length is set to 8 bits. The character format becomes 5 x 7 dot-matrix at 1/16 duty cycle.
Display ON/OFF Control RS: 0 R/W: 0 DB7 — DB0: 0 0 0 0 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
Entry Mode Set RS: 0 R/W: 0 DB7 — DB0: 0 0 0 0 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
Write to CG RAM or DD RAM RS: 1 R/W: 0 DB7 — DB0: 0 1 0 0 1 1 0 0	L_	L is written. The AC is incremented by one and the cursor shifts to the right.
Write to CG RAM or DD RAM RS: 1 R/W: 0 DB7 — DB0: 0 1 0 0 0 0 1 1	LC_	C is written.
⋮	⋮	
Write to CG RAM or DD RAM RS: 1 R/W: 0 DB7 — DB0: 0 0 1 1 0 0 1 0	LCD MODULE M1632	2 is written in digit 16. Cursor disappears.

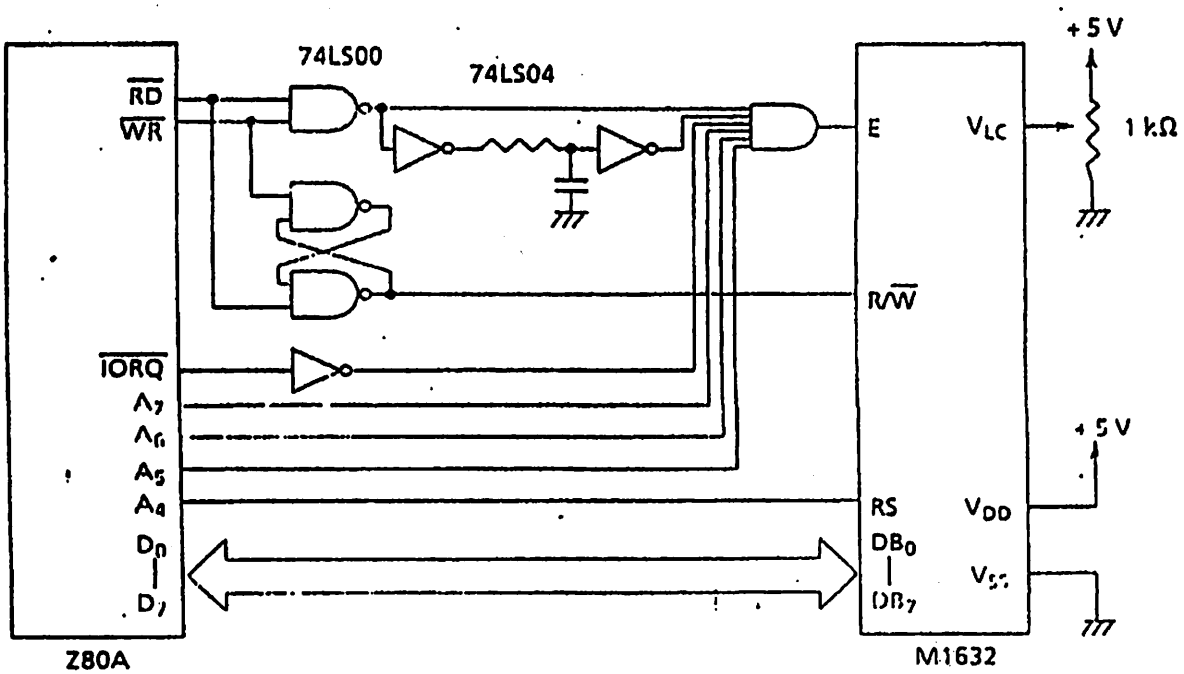
o.	Instruction	Display	Operation
	DD RAM address set RS: 0, R/W: 0, DB7 —— DB0: 1 1 0 0 0 0 0 0	LCD MODULE M1632 _	The DD RAM address is set so that the cursor appears at digit 1 of line 2.
0	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 —— DB0: 0 0 1 1 0 0 0 1	LCD MODULE M1632 1_	1 is written.
1	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 —— DB0: 0 0 1 1 0 1 1 0	LCD MODULE M1632 16_	6 is written.
2	⋮	⋮	
3	Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 —— DB0: 0 1 0 1 0 0 1 1	LCD MODULE M1632 16DIGITS,2LINES	S is written.
4	DD RAM address set RS: 0, R/W: 0, DB7 —— DB0: 1 0 0 0 0 0 0 0	LCD MODULE M1632 16DIGITS,2LINES	The cursor returns to the home position.
;	Display clear RS: 0, R/W: 0, DB7 —— DB0: 0 0 0 0 0 0 0 1	_	All the display disappears and the cursor remains at the home position.
;	⋮	⋮	

(2) Interface data length: Four bits

No.	Instruction	Display	Operation
1	Power-on RS: 0, R/W: 0, DB7 — DB4: 0 0 1 1		The built-in reset circuit initializes the module.
2	Function Set RS: 0, R/W: 0, DB7 — DB4: 0 0 1 0 0 0 0 0 1 0		Four-bit operation mode is set. *Eight-bit operation mode is set by initlallzation, and the instruction is executed only once.
3	Function Set RS: 0, R/W: 0, DB7 — DB4: 0 0 1 0 0 0 1 * * *		The 4-bit operation mode, 1/16 duty cycle, and 5 x 7 dot-matrix character format are selected. Then 4-bit operation mode starts.
4	Display ON/OFF Control RS: 0, R/W: 0, DB7 — DB4: 0 0 0 0 0 0 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
	Entry Mode Set RS: 0, R/W: 0, DB7 — DB4: 0 0 0 0 0 0 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
	Write to CG RAM or DD RAM. RS: 1, R/W: 0, DB7 — DB4: 0 1 0 0 1 0 1 1 0 0	L_	L is written. the AC is incremented by one and the cursor shifts to the right.

7 MPU Connection Diagrams

2.7.1 Z80A



2.7.2 Z80A and 8255A