SKRIPSI

PERANCANGAN DAN PEMBUATAN MODEM DTMF *(Dual Tone Multy Frekuensi)* BERBASISKAN DDS *(Direct Digital Synthesis)* YANG DIAPLIKASIKAN PADA PERALATAN RADIO KOMUNIKASI

Disusun Oleh :

EFENDI

04.12.202

JURUSAN TEKNIK ELEKTRO S-1

KONSENTRASI TEKNIK ELEKTRONIKA

FAKULTAS TEKNOLOGI INDUSTRI

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MARET 2010

LEMBAR PERSETUJUAN

PERANCANGAN DAN PEMBUATAN MODEM DTMF
(Dual Tone Multy Frekuensi)* BERBASISKAN DDS *(Direct Digital Synthesis)
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SKRIPSI

Disusun Dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh
Gelar Sarjana Teknik Elektronika Strata Satu (S-1)

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ABSTRAKSI

PERANCANGAN DAN PEMBUATAN MODEM DTMF *(Dual Tone Multy Frekuensi)* BERBASISKAN DDS *(Direct Digital Synthesis)* YANG DIAPLIKASIKAN PADA PERALATAN RADIO KOMUNIKASI

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Kata Kunci : MC AT89S51, Sistem DDS, DTMF

Pada era globalisasi sekarang ini teknologi berkembang pesat diberbagai bidang, khususnya bidang elektronika banyak diciptakan alat yang dapat membantu pekerjaan manusia menjadi lebih cepat dan mudah untuk diselesaikan. Alat kontrol jarak jauh dinilai dapat membantu kita dalam menjalankan pekerjaan dengan lebih efisien.

Perancangan dan Pembuatan Modem DTMF ini menggunakan mikrokotroller AT89S51 sebagai pengolah data Counter 74HC590, EEPROM AT28C16 dan DAC R2R adalah sistem DDS, serta DTMF MT8870 adalah sebagai pengubah data analog menjadi gelombang *Dual Tone Multy Frekuensi.*

Dari pengujian yang dilakukan diperoleh bahwa semua sistem dapat bekerja dengan baik, sesuai dengan yang diinginkan.

KATA PENGANTAR

Alhamdulillah, puji syukur kehadirat-Mu Ya Allah yang telah memberikan rahmat dan hidayah-Nya, sehingga saya dapat menyelesaikan skripsi yang berjudul **" PERANCANGAN DAN PEMBUATAN MODEM DTMF *(Dual Tone Multy Frekuensi)* BERBASISKAN DDS *(Direct Digital Synthesis)* YANG DIAPLIKASIKAN PADA PERALATAN RADIO KOMUNIKASI"** . Skripsi ini merupakan persyaratan kelulusan Studi di Jurusan Teknik Elektro S-1 Konsentrasi Teknik Elektronika ITN Malang dan untuk mencapai gelar Sarjana Teknik.

Keberhasilan peyelesaian laporan skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penulis menyampaikan terima kasih kepada :

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Penulis telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam menyelasaikan laporan ini. Untuk itu Penulis mengharapkan saran dan kritik yang membangun dari pembaca demi kesempurnaan laporan ini.

Harapan penulis semoga laporan skripsi ini memberikan manfaat bagi perkembangan ilmu pengetahuan dan pembaca.

Malang, Maret 2009

Penulis

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Perkembangan teknologi informasi dan elektronika saat ini berkembang pesat. Perkembangan ini dapat dilihat dengan banyaknya alat-alat komunikasi. Alat-alat komunikasi tersebut dalam menyampaikan data terkadang penyampaiannya tidak selalu dapat disampaikan ke tujuan dengan benar. Banyaknya gangguan seperti noise dalam penyampaian inilah yang terkadang menghambat penyampaian data.

Alat kontrol jarak jauh dinilai tepat membantu kita dalam menjalankan pekerjaan dengan lebih efisien, praktis dan nyaman. Dalam kehidupan sehari-hari sudah banyak dijumpai alat modulasi data yang menggunakan bermacam-macam media komunikasi pada aplikasinya, seperti alat yang dibuat diatas yaitu perencanaan dan pembuatan modem DTMF dengan memakai DDS yang diaplikasikan pada peralatan radio komunikasi.

Dengan adanya alat yang dibuat maka akan terjaga kerahasiaan datanya dari kebocoran pada saat mengirim data memakai DTMF yang dilengkapi dengan sistem DDS.

1.2. Rumusan Masalah

Permasalahan dalam perencanaan dan pembuatan modem DTMF berbasis metode DDS (*Direct Digital Synthesis*) dengan menggunakan modul transmitter adalah bagaimana cara membuat suatu alat dan software yang dapat mendukung

dalam proses pembuatan suatu modem DTMF yang dapat menstransmisikan data melalui media udara dan dapat berfungsi untuk menghasilkan suatu modulasi yang diharapkan lebih efisien.

1.3. Batasan Masalah

Dalam menyusun skripsi ini diperlukan suatu batasan masalah agar tidak menyimpang dari ruang lingkup yang akan dibahas. Adapun batasan masalahnya adalah sebagai berikut :

a) Tidak membahas catu daya
b) Tidak membahas *noise-noise*
c) DAC menggunakan R2R
d) Tidak membahas Modul transmitter dan receiver dari wireless microphone sebagai pengirim dan penerima data
e) Menggunakan mikrokontroler AT89S51 untuk pemrosesan data.
f) Menggunakan LCD sebagai penampil data.

1.4. Tujuan

Tujuan dari skripsi ini adalah merencanakan dan membuat modem DTMF (Dual Tone Multi Frekuensi) berbasis DDS (*Direct Digital Synthesis*) dengan media transmisi udara yaitu dengan menggunakan modul Transmitter yang diharapkan akan menghasilkan transmisi data yang lebih cepat dan modulasi yang flexible dan efisien.

1.5. Metodologi Penulisan

Metodologi yang dipakai dalam pembuatan skripsi ini adalah:

1. Studi Literatur

   Dengan mencari referensi-referensi yang berhubungan dengan perencanaan dan pembuatan alat yang akan dibuat.

2. *Field Research*

   Dengan melakukan penelitian secara langsung mengenai objek-objek yang berhubungan langsung dengan perencanaan alat yang akan dibuat.

3. *Design* dan Pembuatan Alat

   Yaitu meliputi pembuatan PCB, perakitan komponen serta penyolderan dan pembuatan perangkat lunak.

4. Pengujian Alat

   Dengan melakukan pengujian perblok rangkaian dan kerja seluruh sistem pada alat tersebut.

1.6. Sistematika Penulisan

Sistematika penulisan skripsi sebagai berikut :

BAB I PENDAHULUAN

Membahas tentang latar belakang, rumusan masalah, tujuan, batasan masalah, metodologi dan sistematika penulisan pada penulisan skripsi ini.

BAB II LANDASAN TEORI

Berisikan tentang penjelasan dan teori-teori yang berhubungan denagn komponen-komponen yang digunakan dalan perancangan alat.

BAB III PERENCANAAN DAN PEMBUATAN ALAT

Membahas tentang perancangan alat yang terdiri dari perancangan perangkat keras dan perancangan perangkat lunak.

BAB IV PENGUJIAN ALAT

Membahas tentang pengujian peralatan secara keseluruhan dan analisa hasil pengujian.

BAB V PENUTUP

Berisikan kesimpulan yang didapat selama perancangan dan pembuatan alat serta saran-saran.

BAB II

DASAR TEORI

2.1 Latar Belakang DDS

Sistem DDS (*Direct Digital Synthesis*) merupakan salah satu cara untuk menghasilkan sinyal sinusodial secara langsung. Inti dari sistem ini adalah arsitektur akumulator dengan resolusi mencapai mili Hertz dan frekuensi sinyal yang dihasilkan dapat diatur tergantung dari sinyal frekuensi referensi dan metode perancangan. Keluaran sistem DDS yang diproses oleh Mikrokontroler berupa sinyal digital kemudian menjadi masukan untuk DAC *(D/A converter)* dan LPF *(Low Pass Filter)* untuk menghasilkan sinyal sinusoidal yang sempurna.

Semua parameter kontrol sistem DDS berada dalam bentuk besaran digital. Sistem DDS pada dasarnya terdiri atas akumulator phasa, LUT (*Look Up Table*), dan osilator sebagai pembangkit frekwensi referensi (*Clock*). Sedangkan DAC (*Digital to Analog Converter*) dan LPF (*Low Pass Filter*) merupakan komponen-komponen penunjang sistem DDS.

2.1.1 Kelebihan Dan Fleksibilitas DDS

Kelebihan penggunaan Sistem DDS adalah Karakteristik sistem DDS itu sendiri, dimana keutamaan dari sistem ini adalah memiliki *settling time/*kecepatan yang cepat dan memiliki resolusi frekwensi yang halus terhadap frekwensi keluaran, operasi atas suatu spektrum frekwensi yang lebar dan dengan kemajuan dalam desain teknologi proses. serta sangat ringkas dan sedikit membutuhkan pemakain daya. sehingga sangat memungkinkan sistem DDS bisa lebih dikembangkan untuk desain alat yang berkaitan

dengan aplikasi-aplikasi *frequency hopping* serta sistem-sistem yang berkaiatan dengan peralatan pemancar radio,TV, peralatan test, dll. Gambar 2.1 menunjukkan Signal Sinusoida *Direct Digital Synthesis.*

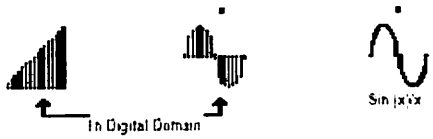


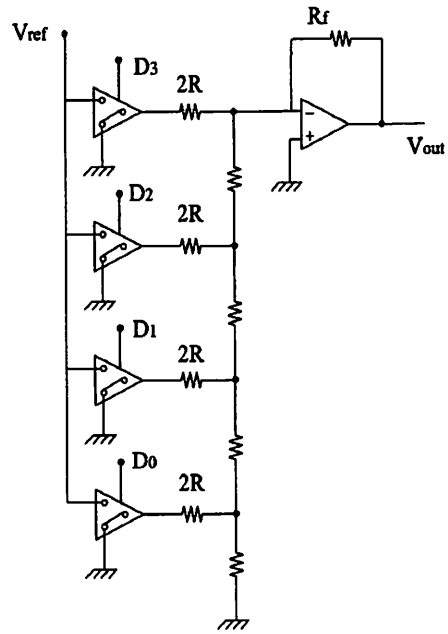
Figure 1-4. Signal flow through the DDS architecture

Gambar 2.1 Signal Sinusoida *Direct digital synthesis* (DDS) [3]

2.1.2 R2R *Digital To Analog Converter*

DAC digunakan untuk mengkonversi data digital menjadi sinyal analog. Pada umumnya semua bentuk konverter digital ke analog akan menghasilkan suatu keluaran yang berupa arus dan tegangan yang merupakan bentuk hasil perkalian antara tegangan analog referensi dengan data digital tertentu (*Multiplying D/A Converter*). Misalnya untuk mengubah data digital (00110011) menjadi analog 0-5 V. Sekarang kita akan membuat 8 bit DAC maksudnya range yang bisa ditangani antara 0 (0000 0000) sampai 255 (1111 1111) yang akan mengasilkan nilai tegangan output 0-5 Volt. Sehingga setiap 1 bit bernilai 5/255=0.019 v maka saat input diberi data 129 (1000 0001) pada tegangan output keluar 129 x 0.019=2.451 V.

Karena konverter digital ke analog ini banyak macamnya, maka pada umumnya dipakai cara konversi dengan rangkaian resistor berbobot (*binary weighted resistor*) dimana posisi dari bit digital yang akan diberikan akan menghasilkan besar arus tegangan yang sesuai bobot biner pada data digital. Didalam penerapannya, cara pemakaian harga tahanan yang bervariasi akan menimbulkan kesulitan dalam memilih harga tahanan yang sesuai, sehingga dipakai rangkaian tangga tahanan R2R yang lebih sederhana. Gambar 2.2 menunjukkan Rangkaian DAC dengan R-2R Ladder



Gambar 2.2 Rangkaian DAC dengan R-2R Ladder[3]

Tahanan keluaran Vout dapat dihitung dengan rumus berikut :

$$\text{Vout} = -\frac{Rf}{R}Vref\left(\frac{D_0}{2^n}+\frac{D_1}{2^{n-1}}+\frac{D_2}{2^{n-2}}\right)-\left(\frac{D_{(n-2)}}{2^2}+\frac{D_{(n-1)}}{2^1}\right)$$

Dimana : $D_0 ... D_1$ = bernilai 1 atau 0

n = banyaknya bit masukan

Vref = tegangan referensi

2.2 Mikrokontroler AT89S51.

2.2.1 Pendahuluan

Perbedaan mendasar antara mikrokontroler dan mikroprosesor adalah mikrokontroler selain memiliki CPU juga dilengkapi memori dan input output yang merupakan kelengkapan sebagai sistem minimum mikrokomputer, sehingga sebuah mikrokontroler dapat dikatakan sebagai mikrokomputer dalam keping tunggal *(Single Chip Microcomputer)* yang dapat berdiri sendiri.

Mikrokontroler AT89S51 adalah mikrokontroler ATMEL yang kompatibel penuh dengan mikrokontroler keluarga MCS – 51, membutuhkan daya rendah, memiliki performance yang tinggi dan merupakan mikrokomputer 8 bit yang dilengkapi 4 Kbyte EEPROM *(Electrical Erasable and Programmable Read Only Memory)* dan 128 Byte RAM internal. Program memori dapat diprogram berulang – ulang atau dengan menggunakan *Programmer Nonvolatile Memory.*

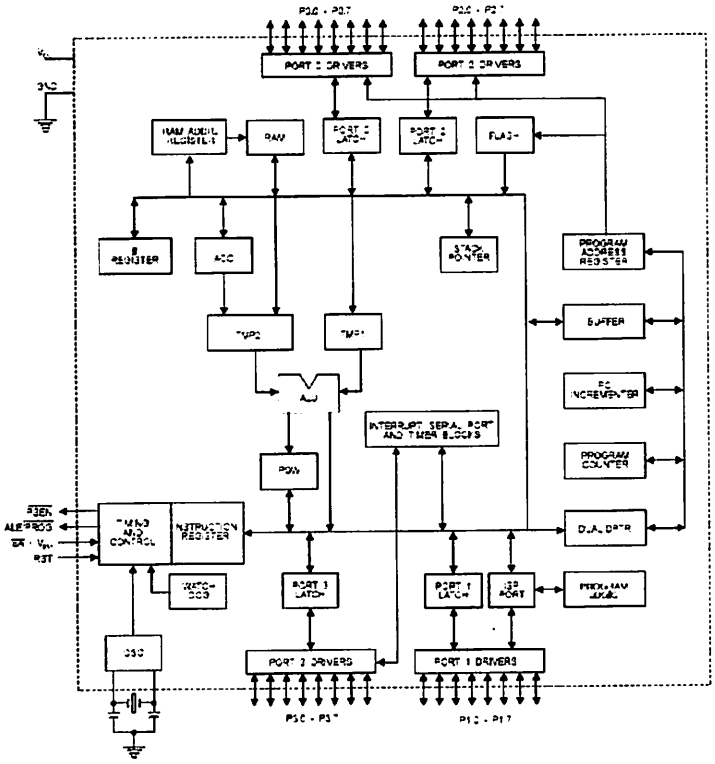
Dalam sistem mikrokontroler terdapat dua hal yang mendasar, yaitu: perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

2.2.2 Perangkat keras mikrokontroler AT89S51

Secara umum Mikrokontroler AT89S51 memiliki :

- CPU 8 bit termasuk keluarga MCS-51
- 4 Kb *Flash memory*
- 128 byte *Internal* RAM
- 4 buah Port I/O, masing – masing terdiri atas 8 jalur I/O
- 2 *Timer/ counter* 16 bit
- 1 *Serial Port Full Duplex*
- Kecepatan pelaksanaan intruksi per siklus 1 μs pada frekwensi *clock* 12 MHz

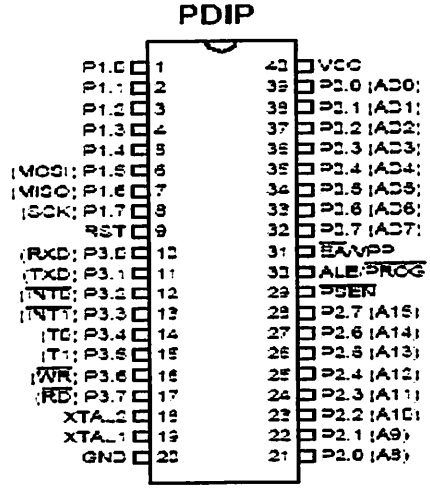
Dengan keistimewaan diatas pembuatan alat menggunakan AT89S51 menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak. Adapun Blok Diagram dari Mikrokontroler AT89S51 adalah seperti pada gambar 2.3



Gambar 2.3 Blok Diagram Mikrokontroler AT89S51[11]

2.2.3 Konfigurasi Pin-Pin Mikrokontroler AT89S51.

Mikrokontroler AT89S51 terdiri dari 40 pin dengan konfigurasi seperti pada gambar 2.4



Gambar 2.4 Konfigurasi Pin-Pin AT89S51[11]

Fungsi tiap pin-nya adalah sebagai berikut :

1. **GND** (Pin 20)

   Dihubungkan dengan Ground Rangkaian.

2. **VCC** (Pin 40)

   Dihubungkan dengan sumber tegangan +5V.

3. **Port 0** (P0.0-P0.7) (Pin 32-39)

   Port 0 (P0.0 – P0.7) merupakan port I/O 8 bit dua arah. Port ini digunakan sebagai multipleks bus alamat rendah (A0 – A7) dan bus data selama pengaksesan ke memori eksternal.

4. **Port 1** (P1.0 -P1.7) (Pin 1-8)

   Merupakan port input – output dua arah dengan *pull-up*. Port ini berfungsi sebagai input atau output dan bekerja baik untuk operasi bit maupun byte, tergantung dari pengaturan software.

5. **Port 2** (P2.0 -P2.7) (Pin 21-28)

   Port 2 (P2.0 – P2.7) merupakan input – output dua arah dengan *pull-up*. Port 2 mengeluarkan *high order address byte* selama pengambilan (*fetch*) program memori eksternal dan selama mengakses data memori eksternal. Port 2 juga menerima *high order address bit* dan beberapa sinyal kontrol selama pemrograman dan verifikasi.

6. **Port 3** (P3.0-P3.7) (Pin 10-17)

   Merupakan port input-output dengan *internal pull-up*, dimana Port 3 juga memiliki fungsi khusus dan dapat dilihat pada tabel 2.1

Tabel 2.1 Fungsi Khusus Pada Port 3. [11]

Pin Port	Fungsi Khusus
Port 3.0	RxD (Port masukan serial)
Port 3.1	TxD (Port keluaran Serial)
Port 3.2	$\overline{\text{INT0}}$ (Masukan Interupsi Eksternal 0)
Port 3.3	$\overline{\text{INT1}}$ (Masukan Interupsi Eksternal 1)
Port 3.4	T0 (Masukan Pewaktu Eksternal 0)
Port 3.5	T1 (Masukan Pewaktu Eksternal 1)
Port 3.6	$\overline{\text{WR}}$ (sinyal tulis memori data eksternal)
Port 3.7	$\overline{\text{RW}}$ (sinyal baca memori data eksternal)

7. **RST (*Reset*),** pin 9.

   Input reset merupakan reset master untuk AT89S51.

8. **ALE / Prog (*Address Latch Enable*),** pin 30.

   Digunakan untuk menahan alamat memori eksternal selama pelaksanaan intruksi.

9. **PSEN (*Program Strobe Enable*),** pin 29.

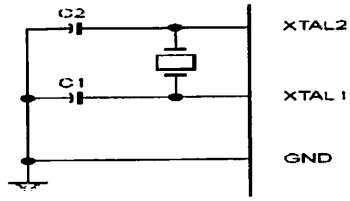
   Merupakan sinyal pengontrol yang memperbolehkan program memori eksternal masuk kedalam bus.

10. **EA / VPP (*External Access*),** pin 31.

Dapat diberikan logika rendah (Ground) atau logika tinggi (+5V). Jika diberikan logika tinggi maka mikrokontroler akan mengakses program dari ROM internal (EEPROM/Flash Memori), dan jika diberikan logika rendah maka mikrokontroler akan mengakses program dari memori eksternal.

11. **X-TAL 1 dan X-TAL 2,** pin 19, 18.

Pin ini dihubungkan dengan kristal bila menggunakan osilator internal. X-TAL 1 merupakan masukan ke rangkaian osilator internal sedangkan X-TAL 2 keluaran dari rangkaian osilator internal . Untuk keperluan ini diperlukan kapasitor penstabil sebesar 30pF. Dan nilai dari X-TAL tersebut antara 4 – 24 Mhz. Untuk lebih jelasnya dapat dilihat pada gambar 2.5.



Gambar 2.5 Osilator AT89S51 [11]

2.2.4 Organisasi Memori.

Organisasi memori pada mikrokontroler AT89S51 dapat dibagi menjadi dua bagian besar yaitu memori program dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpanan data maupun program. Memori program digunakan untuk menyimpan instruksi-instruksi yang akan dijalankan oleh mikrokontroler, sedangkan memori data digunakan sebagai tempat yang sedang diolah mikrokontroler.

Program mikrokontroler disimpan dalam memori program berupa ROM. Mikrokontroler 89S51 dilengkapi dengan ROM internal, sehingga untuk menyimpan program tidak digunakan ROM eksternal yang terpisah dari mikrokontroler. Agar tidak menggunakan memori program eksternal, EA (*Eksternal Address enable*) dihubungkan dengan Vcc.

Memori program mikrokontroler menggunakan alamat 16 bit mulai 0000H-FFFFH, sehingga kapasitas penyimpanan program maksimal adalah 4Kb.

Sinyal /PSEN (*Program Strobe Enable*) tidak digunakan jika digunakan memori program internal.

Selain memori program mikrokontroler AT89S51 juga memiliki data internal 128 *byte* dan mampu mengakses memori data eksternal sebesar 64 Kb. Semua memori data internal dapat dialamati dengan data langsung atau tidak langsung. Ciri dari pengalamatan langsung adalah *operand* alamat *register* yang berisi alamat data yang akan diolah. Sebagian memori tersebut dapat dialamati dengan pengalamatan register, dan sebagian lagi dapat dialamati dengan memori satu bit. Untuk membaca data digunakan sinyal /RD sedangkan untuk menulis digunakan sinyal /WR.

2.2.5 SFR (*Special Function Register*).

Register fungsi khusus (*Special Function Register*) terletak pada 128 byte bagian atas memori data internal dan berisi register-register untuk pelayanan latch port, timer, program status words, control peripheral dan sebagainya. Alamat register fungsi khusus ditunjukkan pada tabel 2.2.

Tabel 2.2 Special Function Register[11]

Simbol	Nama Register	Alamat
ACC	Accumulator	$E0_H$
B	Register B	$F0_H$
PSW	Program Status Word	$D0_H$
SP	Stack Pointer	81_H
DPL	Bit rendah	82_H
DPH	Bit Tinggi	83_H
P0	Port 0	80_H
P1	Port 1	90_H
P2	Port 2	$A0_H$
P3	Port 3	$B0_H$
IP	Interupt Periority Control	$B8_H$
IE	Interupt Enable Control	$A8_H$
TMOD	Timer/Counter Mode Control	89_H
TCON	Timer/Counter Control	88_H
TH0	Timer/Counter 0 High Control	$8C_H$
TL0	Timer/Counter 0 Low Control	$8A_H$
TH1	Timer/Counter 1 High Control	$8D_H$
TL1	Timer/Counter 1 Low Control	$8B_H$
SCON	Serial Control	98_H
SBUF	Serial Data Buffer	99_H
PCON	Power Control	87_H

Beberapa macam register fungsi khusus yang sering digunakan adalah sebagai berikut ini:

- *Accumulator* (ACC) merupakan register untuk penambahan dan pengurangan. Perintah *mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- *Register B* merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Stack Pointer* (SP) merupakan register 8 bit yang dapat diletakkan di alamat manapun pada RAM internal.
- *Data Pointer* (DPTR) terdiri dari dua register, yaitu untuk byte tinggi (Data Pointer High, DPH) dan byte rendah (Data Pointer Low, DPL) yang berfungsi untuk mengunci alamat 16 bit.
- *Port 0* sampai *Port 3* merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada port 0, 1, 2, 3. Masing-masing register ini dapat dialamati per-byte maupun per-bit.
- *Control Register* terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua register khusus, yaitu register IP (*Interupt Priority*) dan register IE (*Interupt Enable*). Untuk mengontrol pelayanan timer/counter terdapat register khusus, yaitu register TCON (*timer/counter control*) serta pelayanan port serial menggunakan register SCON (*Serial Port Control*).

2.6.6. Sistem Interupsi.

Mikrokontroler AT89S51 mempunyai 5 buah sumber interupsi yang dapat membangkitkan permintaan interupsi, yaitu INT0, INT1, T1, T2 dan Port Serial. Saat terjadinya interupsi mikrokontroler secara otomatis akan menuju ke subrutin pada

alamat tersebut. Setelah interupsi selesai dikerjakan, mikrokontroler akan mengerjakan program semula. Tiap-tiap sumber interupsi dapat enable atau disable secara software.

Tingkat prioritas semua sumber *interupt* dapat diprogram sendiri-sendiri dengan *set* atau *clear* bit pada (*Interupt Priority*). Jika dua permintaan interupsi dengan tingkat prioritas yang berbeda diterima secara bersamaan, permintaan interupsi dengan prioritas tertinggi yang akan dilayani. Jika permintaan interupsi dengan prioritas yang sama diterima bersamaan, akan dilakukan polling untuk menentukan mana yang akan dilayani. Bit-bit pada IP adalah sebagai berikut:

–	–	–	**PS**	**PT1**	**PX1**	**PT0**	**PX0**

Priority bit = 1 menandakan prioritas tinggi

Priority bit = 0 menandakan prioritas rendah

Simbol	**Posisi**	**Fungsi**
–	IP.7	Kosong
–	IP.6	Kosong
–	IP.5	Kosong
PS	IP.4	Bit prioritas interupsi port serial
PT1	IP.3	Bit prioritas interupsi Timer 1
PX1	IP.2	Bit prioritas interupsi
PT0	IP.1	Bit prioritas interupsi Timer 0
PX0	IP.0	Bit prioritas interupsi

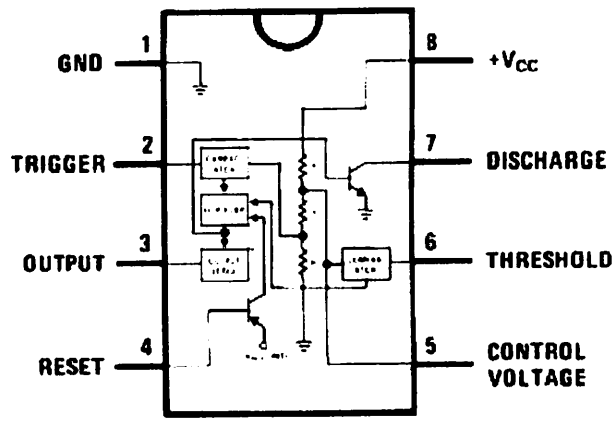
Tingkatan Prioritas Interupsi dapat dilihat para tabel 2.3 berikut ini.

Tabel 2.3 Tingkatan Prioritas Interupsi [11]

Prioritas Interupsi	Sumber Interupsi	Alamat Vektor
1	IE0 (Interupsi eksternal 0)	0003_H
2	TF0 (timer overflow flag 0)	$000B_H$
3	IE1 (interupsi eksternal 1)	0013_H
4	TF1 (timer overflow flag 1)	$001B_H$
5	R1 dan T1	0023_H

2.3 *Timer*

Timer adalah suatu alat yang sangat stabil untuk membangkitkan sinyal. Timer LM555 memiliki 8 pin dengan konfigurasi seperti pada gambar 2.6.



Gambar 2.6 Konfigurasi Pin-Pin LM555 [7]

- **Pin 1 (GROUND)** : Merupakan titik 0V komponen yang dihubungkan dengan ground rangkaian atau ground supply. Pin ini ditunjukkan oleh titik (notch) yang terdapat pada badan komponen.
- **Pin 2 (TRIGGER)** : Merupakan salah satu input komparator bagian bawah yang akan dibandingkan dengan input lain pada komparator tersebut yang telah direferensikan nilainya sebesar 1/3 tegangan supply (Vs). Jika input trigger berubah dari HIGH ke LOW dan besarnya kurang dari 1/3 Vs maka komparator bagian bawah ini akan mengaktifkan flip-flop sehingga akan dihasilkan output IC 555 dalam kondisi HIGH. Pin trigger ini mempunyai impedansi yang sangat besar, yaitu > 2MΩ.
- **Pin 3 (OUTPUT)** : Output IC 555 dinyatakan pada pin ini.
- **Pin 4 (RESET)** : Digunakan untuk membuat output IC 555 dalam kondisi LOW (reset) untuk semua kondisi input. Reset akan terjadi saat pin ini diberikan tegangan sebesar ? 0,7V.
- **Pin 5 (CONTROL)** : Merupakan salah satu input komparator bagian atas dimana input lain dari komparator adalah pin Threshold pada IC 555. Pin ini digunakan untuk mengatur tegangan ambang (threshold) yang telah diatur secara default sebesar 2/3 tegangan supply (Vs). Biasanya pin ini jarang digunakan dan saat tidak digunakan pin ini dihubungkan pada titik ground rangkaian melalui sebuah kapasitor 0,01uF yang berguna untuk mengurangi gangguan noise.
- **Pin 6 (THRESHOLD)** : Saat tegangan input pin ini berubah dari LOW ke HIGH dan besarnya lebih dari 2/3 tegangan supply (Vs) maka komparator bagian atas akan mereset flip-flop sehingga akan dihasilkan output IC 555 dalam kondisi LOW.

- **Pin 7 (DISCHARGE)** : Merupakan jalur pembuangan arus yang berasal dari kaki kolektor transistor NPN yang terdapat pada IC 555. Pin ini biasanya dihubungkan pada sebuah kapasitor yang juga berfungsi untuk mengatur pewaktuan (timing) IC 555.
- **Pin 8 (VCC)** : Sebagai input sumber tegangan DC yang digunakan untuk mengaktifkan IC 555. Sumber tegangan yang digunakan sebesar 5V – 15V

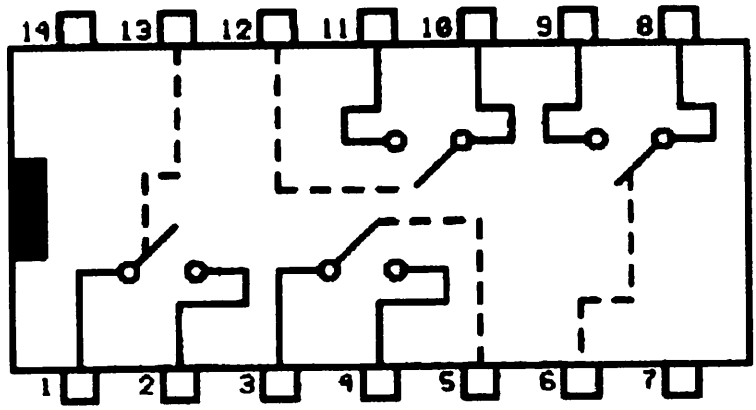
Dalam aplikasi rangkaiannya, IC timer 555 mempunyai 3 mode operasi dasar, yaitu :

1. Monostable: Output rangkaian monostable hanya berupa satu pulsa (HIGH) saja, yaitu saat input sinyal yang diumpankan pada pin trigger berubah dari kondisi HIGH ke LOW. Rangkaian monostable juga biasa disebut dengan rangkaian one-shoot.
2. Astable: Output rangkaian astable berupa gelombang kotak yang berosilasi pada frekuensi dan periode tertentu, tergantung dari komponen RC yang digunakan.
3. Bistable: Output rangkaian bistable mempunyai 2 kondisi output yang dipengaruhi oleh input pada pin trigger dan reset. Atau dapat dikatakan, output rangkaian bistable serupa dengan output rangkaian astable yang dioperasikan secara manual tanpa menggunakan komponen RC sebagai pengatur pewaktuan (timing).

2.4 Selector CD4066

CD4066 adalah sebuah switch yang dapat digunakan untuk transmisi atau multiplexing dari sinyal analog maupun sinyal digital. Dari pin-pinnya sangat mirip dengan CD4016 tetapi resistansinya lebih rendah.

CD4066 terdiri dari 4 bagian yang mempunyai tugas masing-masing, 2 buah device P dan N pada switch bertugas menentukan hidup atau mati secara bersamaan dengan Kontrol sinyal. IC CD4066 memiliki 14 pin dengan konfigurasi sepert gambar 2.7 berikut ini.



Gambar 2.7 Konfigurasi Pin-Pin CD4066 [8]

Fungsi dari pin-pin IC CD4066 dapat dilihat pada tabel 2.4 dibawah ini.

Tabel 2.4 Fungsi Pin CD4066 [8]

PIN	SIGNAL	DIR	NOTE
1	I1	IN	INPUT #1
2	O1	OUT	OUTPUT #1
3	I2	IN	INPUT #2
4	O2	OUT	OUTPUT #2
5	I3	IN	INPUT #3
6	O3	OUT	OUTPUT #4
7	GND	----	GROUND
8	I3	IN	INPUT #3
9	O3	OUT	OUTPUT #3
10	I4	IN	INPUT #4
11	O4	OUT	OUTPUT#4
12	C4	IN	CONTROL #4
13	C1	IN	CONTROL #1
14	VCC	----	SUPPLY VOLTAGE 5V

2.5 *Counter*

2.5.1 Diskripsi

Counter atau rangkaian penghitung adalah rangkaian logika sequensial yang dapat dipergunakan untuk menghitung jumlah pulsa yang masuk dan dinyatakan dengan suatu bilangan biner. Hal ini dikarenakan counter membutuhkan karakteristik memori. Pewaktu (*Timer*) memegang peranan penting dalam pengoperasian counter. Counter digital memiliki karakteristik penting:

1. Jumlah hitungan maksimum (*Modulus counter*)
2. Menghitung ke atas atau ke bawah
3. Operasi asinkron atau sinkron
4. Bergerak bebas atau berhenti sendiri

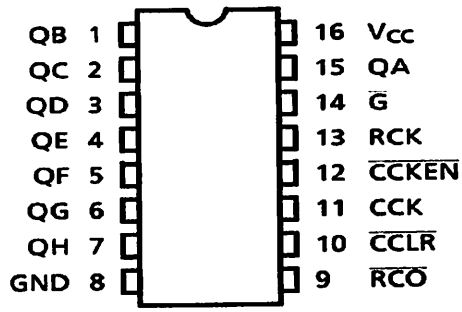
Ada beberapa jenis counter dalam pembahasan sistem digital, diantaranya yaitu Binary Counter, Up Counter, Down Counter, Johnson Counter, Decade Counter, dan masih banyak lagi. namun, dalam makalah ini akan dibahas tentang Decade Counter atau dikenal juga Ripple Counter Modulo-10.

Pencacahan sekuensial/berurutan dari *counter modulo*-10 atau decade counter adalah dari 0000 sampai 1001 (0 hingga 9 desimal). Counter mod-10 memiliki 4 bit dengan harga: 8-an, 4-an, 2-an dan 1-an. Untuk itu dibutuhkan empat *flip-flop* yang dihubungkan seperti Ripple Counter. Kita harus menambahkan gerbang NAND untuk menghapus (*clear*) semua *flip-flop* kembali ke keadaan nol segera sesudah hitungan ke- 10. Karena modulus-10 menghitung hingga 9 (1001), maka hitungan berikut (10 - 1010) digunakan untuk menghasilkan pulsa *reset*. Hal ini dilakukan dengan mengumpankan kedua logika 1 pada 1010 kedalam gerbang NAND yang akan mereset seluruh *flip-flop* kembali ke 0000 lagi. Maka counter akan menghitung mulai 000 hingga 1001 lagi. Dengan menggunakan gerbang NAND, kita dapat membuat

sejumlah counter modulo yang lain, dengan tetap memperhatikan logika 1 sebagai "tanda" tercapainya batas penghitungan. Counter ini dapat dibangun dari berberapa *flip-flop* individual, namun juga diproduksi keempat *flip-flop* dalam satu paket IC, yang bahkan sudah menyertakan gerbang reset NAND.

2.5.2 LM74HC590

Berdasar jumlah pin pada LM74HC590 yaitu memiliki 16 pin dan juga memiliki fungsi-fungsi yang berbeda-beda seperti ditunjukkan pada gambar 2.8.



Gambar 2.8 LM74HC590 [4]

Tabel kebenaran dari LM74HC590 dapat dilihat pada tabel 2.5 dibawah ini.

Tabel 2.5 Tabel kebenaran [4]

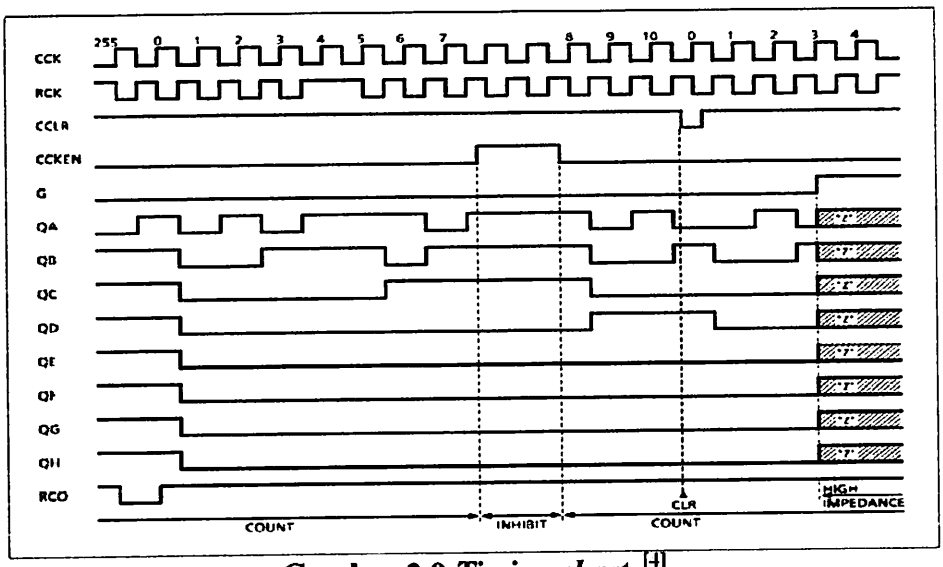
INPUT					FUNCTION
G	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
H	X	X	X	X	Q OUTPUTS DISABLE
L	X	X	X	X	Q OUTPUTS ENABLE
X	↑	X	X	X	COUNTER DATA IS STORED INTO REGISTER
X	↓	X	X	X	REGISTER STATE IS NOT CHANGED
X	X	L	X	X	COUNTER CLEAR
X	X	H	L	↑	ADVANCE ONE COUNT
X	X	H	L	↓	NO COUNT
X	X	H	H	X	NO COUNT

X : Don't care

$RCO = \overline{QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'}$

(QA'~QH' : Internal outputs of the counter)

Gambar *Timing chart* dari LM74HC590 dapat dilihat pada gambar 2.9 berikut ini.



Gambar 2.9 *Timing chart* [4]

2.6 EEPROM *(Electrically Erasable Programmable Read Only Memory)*

2.6.1 Deskripsi

EEPROM merupakan kependekan dari *Electrically Erasable Programmable Read-Only Memory*. EEPROM adalah tipe khusus dari PROM (*Programmable Read-Only Memory*) yang bisa dihapus dengan memakai perintah elektris. Seperti juga tipe PROM lainnya, EEPROM dapat menyimpan isi datanya, bahkan saat listrik sudah dimatikan.

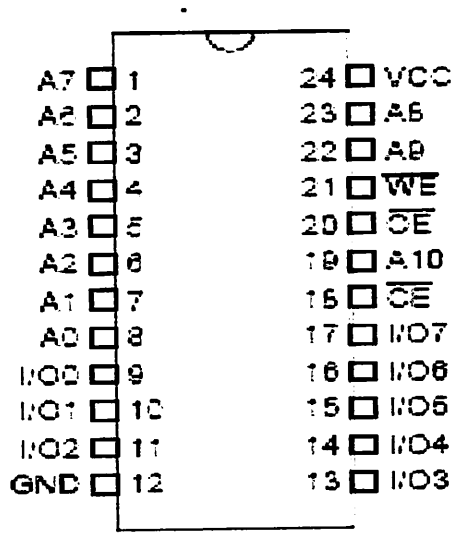
EEPROM sangat mirip dengan flash memory yang disebut juga flash EEPROM. Perbedaan mendasar antara flash memory dan EEPROM adalah penulisan dan penghapusan EEPROM dilakukan dilakukan pada data sebesar satu byte, sedangkan pada flash memory penghapusan dan penulisan data ini dilakukan pada data sebesar satu block. Oleh karena itu flash memory lebih cepat.

Dengan ROM biasa, penggantian BIOS hanya dapat dilakukan dengan mengganti chip. Sedangkan pada EEPROM program akan memberikan instruksi kepada pengendali chip supaya memberikan perintah elektronis untuk kemudian

mendownload kode BIOS baru untuk dikirimkan kepada chip. Hal ini berarti perusahaan dapat dengan mudah mendistribusikan BIOS baru atau *update*, misalnya dengan menggunakan disket. Hal ini disebut juga flash BIOS.

2.6.2 Konfigurasi Pin AT28C16

Berdasar jumlah pin pada IC EEPROM AT28C16 yaitu memiliki 24 pin dan juga memiliki fungsi-fungsi yang berbeda-beda, gambar 2.10 merupakan konfigurasi dari AT28C16.



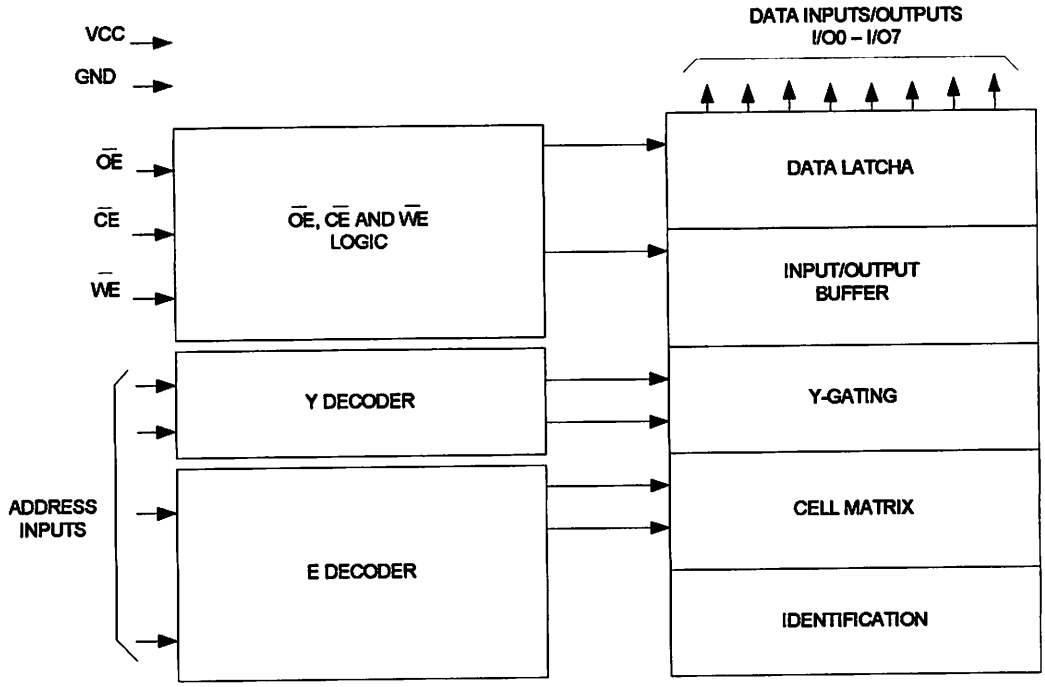
Gambar 2.10 Konfigurasi Pin AT28C16 [5]

Tabel 2.6 dibawah ini merupakan tabel konfigurasi pin dari AT28C16.

Tabel. 2.6 Tabel Konfigurasi Pin [5]

Pin Name	Function
A0 - A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

Diagram Blok dari AT28C16 ditunjukan pada gambar 2.11



Gambar 2.11 Diagram Blok AT28C16 [5]

2.7 *Mixer*

Mixer merupakan suatu sicuit pengali dua buah frekuensi menjadi frekuensi baru, yang frekuensinya penjumlahan dan pengurangan dari frekuensi asal dengan frekuensi pembawanya. Jadi mixer beroperasi dengan melakukan proses perkalian fungsi trigonometri

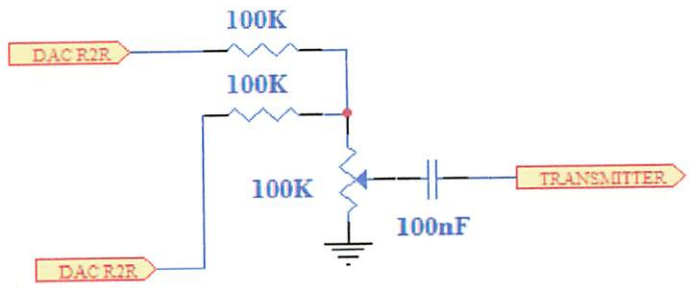
V1 (t) VOUT (t)

V2 (t)

Sesusai deret Taylor, hubungan antara input dan output adalah:

$v0(t) = a\ vi(t) + b\ [vi(t)]2 + c\ [vi(t)]3 + \ldots$

Rangakaian *Mixer* ditunjukan seperti gambar 2.12 berikut ini.



Gambar 2.12 Rangkaian *Mixer*

2.8 DTMF (*Dual Tone Multiple Frequency*)

DTMF (*Dual Tone Multiple Frequency*) merupakan metode yang paling banyak digunakan dalam bidang telekomunikasi. Sebagian besar industri telekomunikasi manggunakan sistem DTMF sebagai *tone* dialer karena lebih efisiensi dan memberikan kecepatan dalam melakukan *dialing*. Dalam perkembangannya, pensinyalannya DTMF tidak saja digunakan untuk sistem *dialing* saja namun akan digunakan untuk sistem komunikasi data, pengendali jarak jauh melalui telepon, mesin penjawab telepon dan lain-lain.

DTMF menggunakan 16 buah audio frekuensi yang merupakan sistem sinyal frekuensi ganda. Dalam sistem ini, sebuah frekuensi tersusun atas sebuah kombinasi dari 2 buah audio frekuensi, yaitu *low* group dan hig group,yang dipilih satu demi satu pada tiap frekuensi (lebih tinggi atau lebih rendah) yang membentuk sebuah pasangan nada. penekanan masing-masing *keypad* akan dialokasikan dan dihubungkan dengan sebuah angka atau kode. Alokasi frekwensi DTMF seperti ditujukkan pada tabel 2.7.

Tabel 2.7 Alokasi frekwensi DTMF [6]

Low frequency (Hz)	High frequency (Hz)			
	1209	1336	1477	1633
697	1	2	3	A
770	4	5	6	B
852	7	8	9	C
941	#	0	*	D

Dari tabel 2.7 dapat dibaca bahwa setiap penekanan tombol di pesawat telepon, telpon akan membangkitkan dua nada (*tone*) yaitu nada berfrekuensi tinggi dan nada berfrekuensi rendah. Kedua sinyal tersebut dikirimkan ke penerima.

2.8.1 Rangkaian DTMF Decoder

Untuk menangkap tombol apa yang ditekan oleh penelepon maka peranti pertama yang harus disediakan adalah peranti yang bertugas mendeteksi sinyal apa yang dikirimkan. Jika sinyal yang dikirimkan bukan sinyal bicara melainkan sinyal yang dikarenakan penekanan tombol telepon maka dapat digunakan tabel 2.7 untuk melakukan pendekode-an. Untuk itu diperlukan sebuah rangkaian elektronik yang mendapat masukan dari kabel telepon dan keluaran bilangan hasil pendekodean sinyal tersebut.

Jika dilihat tombol tombol yang di kodekan ada 16 buah, digunakan 2 buah nada dengan variasi nilai masing masing nada 4 nilai. Keluaran dari rangkaian ini yang diharapkan adalah bilangan biner 4 digit. Dari tabel 2.7 dapat
di buat tabel 2.8 dibawah ini yang menunjukan konversi masukan menjadi keluaran. Karena ada 16 buah keluaran sebetulnya keluran ini jika dilambangkan dengan bilangan biner dapat diwakili dengan 4 bit bilangan biner dari 0000 sampai dengan

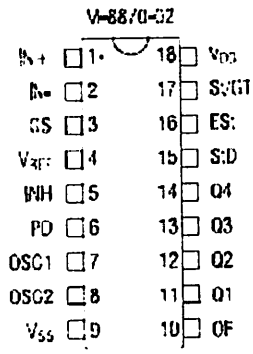
1111. Pada tabel 2.8 berikut ini menunjukan fungsi transfer input ke output data DTMF.

Tabel 2.8 Fungsi Transfer dari input menjadi *output* [6]

Frekwensi rendah	Frekwensi Tinggi	Tombol yang ditekan
697 Hz	1209 Hz	1
697 Hz	1366 Hz	2
697 Hz	1477 Hz	3
697 Hz	1633 Hz	A
770 Hz	1209 Hz	4
770 Hz	1366 Hz	5
770 Hz	1477 Hz	6
770 Hz	1633 Hz	B
852 Hz	1209 Hz	7
852 Hz	1366 Hz	8
852 Hz	1477 Hz	9
852 Hz	1633 Hz	C
941 Hz	1209 Hz	*
941 Hz	1366 Hz	0
941 Hz	1477 Hz	#
941 Hz	1633 Hz	D

Untuk keperluan mendekode masukan tersebut diperlukan sebuah peranti elektronika dengan masukan sinyal telepon dan keluaran logika 4 bit. Untuk keperluan ini dapat digunakan salah satu produk IC *Dual Tone Multiple Frquencies*

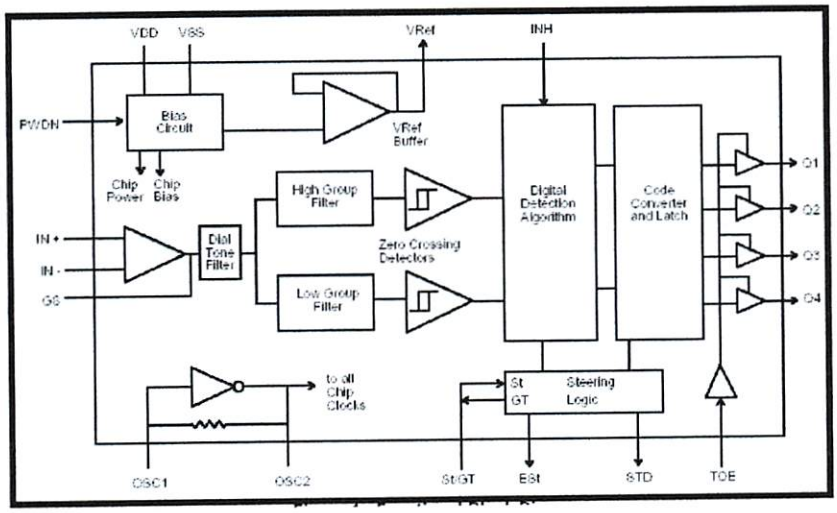
Dekoder yaitu MT8770 produk MITEL. Konfigurasi dari MT8870 dapat dilihat pada gambar 2.13.



Gambar 2.13 Konfigurasi pin IC MT 8870 [7]

Decoder ini mengkodekan sinyal– sinyal DTMF menjadi kode biner (*binary code*) 4 bit. Decoder ini telah dilengkapi dengan filter untuk frekuensi tinggi (*high frequency*) dan frekuensi rendah (*low frequency*) serta sebuah digital decoder. Filter menggunakan *switched capacitor* untuk membedakan frekuensi yang masuk, sedang decoder menggunakan teknik pencacahan (*counting techniques*) secara digital untuk mendeteksi dan mengkodekan 16 buah pasangan frekuensi DTMF menjdai kode biner 4 bit. Selain itu, MT8870 juga dilengkapi dengn rangkaian internal penguat differential, *oscillator clock*,dan sebuah rangkaian *latch* 3 *state* pada bagian *output*.dengan demikian rangkaian external tambahan untuk membentuk sebuah decoder DTMF yang lengkap dapat dikurangi.

Block diagram dari decoder MT8870 pada gambar 2.14 berikut ini.



Gambar 2.14 Diagram blok IC MT8770 [7]

Fungsi masing-masing kaki *decoder* MT 8870 adlah sebagai berikut :

1. *Non Inverting* OP – AMP (IN +)

   Sinyal dimasukan ke kaki ini apabila tidak diperlukan pembalikan fase.

2. *Inverting* OP – AMP (IN -)

   Sinyal dimasukan ke kaki ini apabila diperlukan pembalikan fase.

3. *Gain select* (GS)

   Kaki ini diperlukan untuk pemilihan penguatan sinyal. Apabila diperlukan penguatan, maka diperlukan sebuah resistor yang dihubungkan ke kaki ini.

4. Vref

   Tegangan referensai nominal $^1/_2$ VDD digunakansebagai input bias.

5. *Inhid* (INH)

   Digunakan dalam mendeteksi nada yang diwakili karakter A, B, C dan D.

6. *Power Down* (PD)

   Logika high diberikan pada saat menerima sinyal (standbay mode)

7. OSC1

   Kaki ini sebagai masukan dari *crystal oscillator*. Nilai kristal yang digunakan sebesar 3,579545 MHZ

8. OSC2

   Kaki ini sebagai keluaran dari crytal oscillator.

9. *Ground* (Vss)
10. *Three State Output Enable* (TOE)

    Kaki ini berfungsi untuk mengendalikan data keluaran Q1, Q2, Q3, dan Q4. Bila kaki ini diberikan logika high, maka akan mengeluarkan data.
11. Q1 – Q4

    Output data 4 bit.
12. *Delayed Steering* (StD)

    Bila masukan mendeteksi nada – nada DTMF, maka kaki ini akan memberikan logika high dan sebaliknya.
13. *Early Steering* (Est)

    Kaki ini akan mengeluarkan logika high apabila bagian digital algoritma pasangan nada – nada DTMF (sinyal kondisi). Bila sinyal kondisi tersebut hilang seketika, maka akan menyebabkan Est berlogika low.
14. *Steering Input / Guard Biderectional* (St/GT)

    Jika tegangan yang terdeteksi oleh St lebih besar daripada tegangan VTSt, maka menyebabkan pasangan nada yang terdeteksi untuk dicatat dan dilakukan penguncian keluaran yang terbaru. Jika tegangn yang dideteksi lebih kecil maka akan bebas menerima pasangan nada yang baru.
15. *Power Supply* (VDD)

    Kaki ini dihubungkan ke sumber tegangan 5 Volt.

IC MT 8870 memerlukan komponen luar untuk menerima nada – nada DTMF. Komponen tersebut untuk penguat masukan, oscillator clock, dan rangkaian kendali.

Nilai R3 yang digunakan dalam penguat ditentukan dengan persamaan :

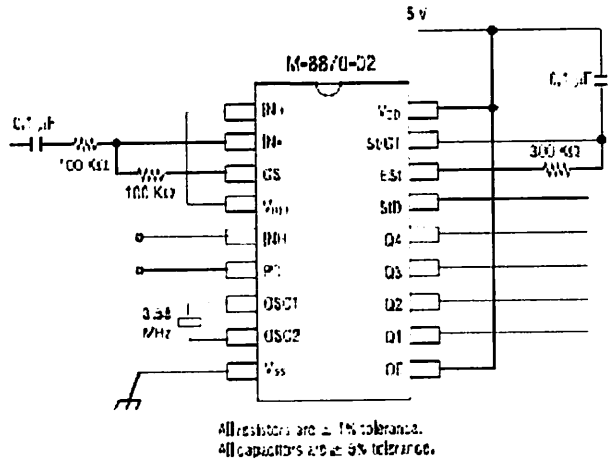
$$R3 = \frac{R2 \cdot R5}{R2 + R5} \quad \text{..... (i)}$$

Sedangkan penguatan tegangan dihitung dengan persamaan :

$$\text{Av diff} = \frac{R5}{R1} \quad \text{..... (ii)}$$

Dimana : Avdiff = penguatan tegangan (kali).

Rangkaian oscillator sudah ada dalam IC ini secara internal, sehingga hanya memerlukan 1 komponen external, yaitu berupa crystal oscillator yang dipasang antara kaki 7 dan kaki 8. kristal yang digunakan bernilai 3,579545 MHz.Rangkaian kendali berfungsi untuk mengendalikan *output* StD. Pada gambar 2.15 berikut adalah rangakaian dasar kendali dari MT8870.



Gambar 2.15 Rangkaian dasar kendali [7]

Logika high pada Est menyebabkan tegangan VC2 naik dan apabila logika pada ESt kembali rendah kembali rendah, maka akan membuat tegangan VC2

2.9 LCD (*Liquid Crystal Display*)

Merupakan komponen optoelektronik yaitu komponen yang bekerja atau dipengaruhi oleh sinar (optolistirk), komponen pembangkit cahaya (*Light Emiting*) dan komponen – komponen yang akan mengubah sinar. LCD terbuat dari bahan Kristal cair yang merupakan suatu komponen oraganik dan mempunyai sifat optik seperti benda padat meskipun bahan tetap cair.

Sel Kristal cair terdiri dari selapis bahan Kristal cair yang diapit antara dua kaca tipis yang transparan. Antara dua lembar kaca tersebut diberi bahan Kristal cair

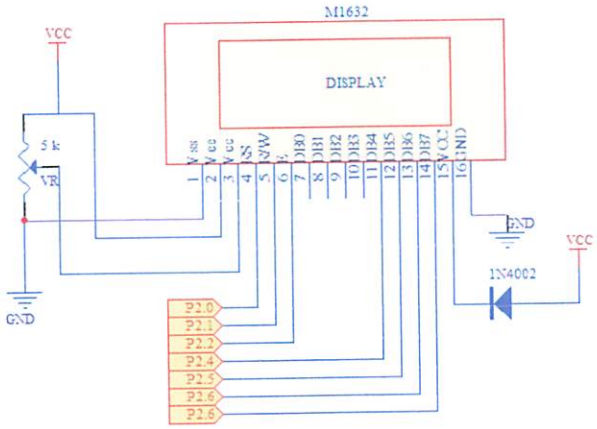
(*liquid crystal*) yang tembus cahaya. Permukaan luar dari masing – masing keeping kaca mempunyai lapisan penghantar tembus cahaya seperti oxide timah (*tin oxide*) atau oxide indium (*indium oxide*). Sel mempunyai ketebalan sekitar 1×10^{-5} meter dan diisi dengan crstal cair.

Karena sel – sel kristal cair merefleksikan cahaya dan bulan membangkitkan cahaya maka konsumsi daya yang dibutuhkan relatif rendah. Energi yang dipergunakan hanya untuk mengaktifkan kristal cair. Pada dasarnya LCD bekerja pada tegangan rendah (13 – 15 Vrms), frekwensi rendah (25 – 60 Hz) sinyal AC dan memakai arus listrik yang sangat kecil (25 – 300 μA). LCD sering kali ditata sebagai tampilan *seven segment* untuk menampilkan angka tetapi juga memiliki keistimewaan lain yaitu, kemampuan untuk menampilkan karakter dan berbagai macam simbol.

Salah satu jenis LCD diantaranya adalah LCD M1632. Suatu jenis piranti dengan konsumsi daya yang rendah, disusun dari dot matrik dan dikontrol oleh ROM atau RAM generator karakter dan RAM data display. Pengontrolan utamanya adalah pada ROM generator dan display data RAM yang menghasilkan kode ASCH jika padanya diberikan input ASCH. Untuk dapat difungsikan dengan baik maka perlu diperhatikan proses analisasi yang telah ditentukan oleh pabrik pembuatannya. Timing penganalisasian sangat dipertimbangkan, karena jika melesat sampai ordo sama dengan *milisecon* maka dapat dipastikan LCD tidak dapat berfungsi.

LCD Display Module M1632 buatan Seiko Instrument Inc. ini terdiri dari dua bagian, yang pertama merupakan panel LCD sebagai media penampil informasi dalam bentuk huruf/angka dua baris, masing – masing baris bisa menampung 16 huruf/angka. Bagian kedua merupakan sebuah sistem yang dibentuk dengan mikrokontroler yang ditempelkan dibalik pada panel LCD, berfungsi mengatur tampilan informasi serta berfungsi mengatur komunikasi M1632 dengan

mikrokontroler yang memakai tampilan LCD itu. Dengan demikian pemakaian M1632 menjadi sederhana, sistem lain yang M1632 cukup mengirimkan kode – kode ASCH dari informasi yang ditampilkan seperti layaknya memakai sebuah printer. Pada gambar 2.16 dibawah ini menunjukan rangkaian LCD M1632.



Gambar 2.16 Rangkaian LCD M1632 [14]

Adapun karekteristik dari LCD M1632 antara lain :

- Dengan 16 karakter – 2 baris dalam bentuk dotmatrik 5x7 dan cursor
- *Duty ratio* 1/16
- Memiliki ROM pembangkit karakter untuk 192 jenis karakter
- RAM untuk data display sebanyak 80x8 bit
- Dapat dirangkai dengan MPU 8 bit / 4 bit
- RAM data *display* dan RAM pembangkit karakter dapat dibaca oleh MPU
- Memiliki fungsi intruksi anatara lain *display on/off, cursor on/off, display* karakter *blink, cursor shift* dan *display shift.*
- Memiliki rangkaian oscillator sendiri
- Catu tegangan tunggal yaitu ± 5V
- Memiliki rangkaian *reset* otomatis pada catu daya yang dihidupkan.

LCD memiliki 16 pin, masing – masing memiliki fungsi seperti pada tabel 2.9.

Tabel 2.9 Fungsi tiap pin LCD [14]

No pin	Simbol	Level	fungsi	
1	Vss	-	Power supply	0 V (GND)
2	Vcc	-		5 V ± 10%
3	VEE	-		For LCD drive
4	RS	H/L	Sinyal seleksi regester H ; data input [register data (*write/read*)] L ; *instruction input* [register instruksi *(write), busy flag* dan *address counter (read)*]	
5	R/W	H/L	H ; *read* L ; *write*	
6	E	H	*Enable* signal [sinyal penanda mulai operasi, aktif saat operasi *write* atau *read*]	
7	DB0	H/L	4 *bit* bus data *lower* 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L	4 *bit* bus data *upper* 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler, DB7 juga sebagai *busy flag*	
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+BL	-	Back Light Supply	4 – 4,2 V 50 – 200 mA
16	V-BL	-		0 V (GND)

Instruksi Operasi pada LCD dapat dilihat seperti table 2.10 dibawah ini

Tabel 2.10 Instruksi pada LCD [14]

Instruksi	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
Display Clear	0	0	0	0	0	0	0	0	0	1
Cursor Home	0	0	0	0	0	0	0	0	1	*
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S
Display On/Off	0	0	0	0	0	0	1	D	C	B
Cursor Display Shift	0	0	0	0	0	1	S/C	R/L	*	*
Function Set	0	0	0	0	1	DL	1	*	*	*
CG RAM Address Set	0	0	0	1	ACG					
DD RAM Address Set	0	0	1	ADD						
BF/Address Read	0	1	BF	AC						
Data Write to CG RAM	1	0	Write data							
Data Read from CG RAM	1	1	Read data							

Pada LCD juga terdapat instruksi – instruksi sebagai berikut :

1. *Display Clear*

   Memberikan tampilan yang ada pada LCD serta menyimpan, sedangkan kursor kembali ke posisi semula.

2. *Cursor Home*

   Hanya memberikan tampilan dan kursor kembali ke semula

3. *Empty Mode Set* : layar beraksi sebagai tampilan tulis

   S : 1/10 = menggeser layar

   1/0 : 1 = kursor bergerak ke kanan dan layar bergerak ke kiri

   1/0 : 0 = kursor bergerak ke kiri dan layar bergerak ke kanan

4. *Display On/Off Control*

   D : 1 = layar on

   D : 0 = layar off

C : 1 = kursor on

C : 0 = kursor off

B : 1 = kursor berkedip – kedip

B : 0 = kursor tidak berkedip – kedip

5. *Cursor Display Shift*

   S/C : 1 = LCD diidentifikasikan sebagai layar

   S/C : 0 = LCD diidentifikasikan sebagai kursor

   R/L : 1 = menggeser satu spasi ke kanan

   R/L : 0 = menggeser satu spasi ke kiri

6. *Fuction Set*

   DL : 1 = panjang data LCD pada 8 bit

   DL : 0 = panjang data LCD pada 4 bit

   Bit upper di transfer terlebih dahulu kemudian diikuti dengan 4 bit lower

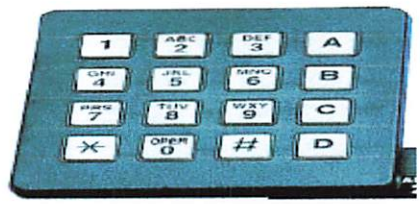
   N : 1/0 = LCD menggunakan 2 atau 1 baris karakter

   P : 1/0 = LCD menggunakan 5 x 10 dot matrik

7. CG RAM *address set* : menulis alamat RAM ke karakter
8. DD RAM *address set* : menulis alamat RAM ke tampilan
9. BF/*address set* : BF = 1/0, LCD dalam keadaan sibuk atau tidak sibuk
10. Data *write to* CG RAM or DD RAM : membaca byte dari alamat terakhir RAM yang dipilih.

2.10 Keypad 4x4

Teknik yang sering digunakan dalam perancangan keypad adalah teknik multiplexing empat buah jalur baris dan empat jalur kolom. Bila baris dan kolom ini disidangkan maka akan terbentuk titik-titik potong yang membentuk matriks 4x4. seperti pada Gambar 2.17



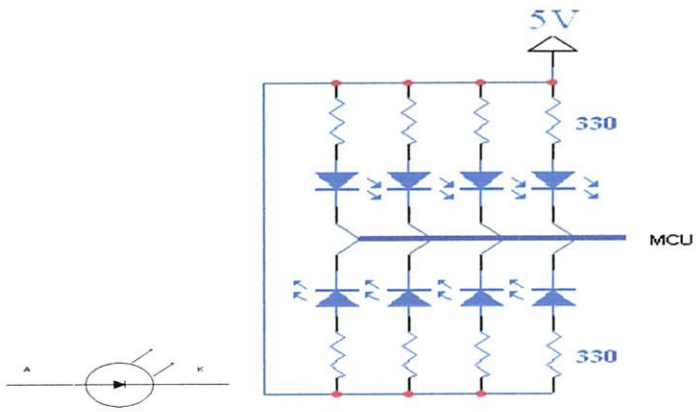
Gambar 2.17 Penampang Dasar Keypad [9]

Rangkaian ini dapat dianalogikan dengan empat buah kabel terbuka yang disilangkan dengan empat kabel terbuka lainnya. Bila pada suatu titik, kabel yang disilangkan itu disentuhkan maka diasumsikan bahwa tombol keypad pada posisi yang- bersilangan tersebut ditekan. Untuk mengidentifikasikan letak atau posisi tombol yang ditekan itu, bahwa susunan matrix keypad itu membetuk koordinat (x,y) dalam dua dimensi, informasi posisi yang diperlukan adalah informasi tentang nilai x dan y.

2.11 LED (*Light Emitting Dioda*)

LED adalah dioda semi konduktor yang khusus yang dirancang untuk memancarkan cahaya apabila arus melaluinya. Apabila diberi bias maju, energi electron yang mengalir melewati tahanan sambungan diubah langsung menjadi energi cahaya. Karena LED adalah dioda, maka arus hanya akan mengalir apabila LED dihubungkan dengan bias maju.

Keuntungan utama pemggunaan LED sebagai sumber cahaya dibandingkan dengan bola lampu cahaya biasa adalah penggunaan daya yang jauh lebih rendah, jauh lama umurnya, dan beroperasi dengan kecepatan tinggi. Simbol dan rangkaian LED dapat dilihat pada gambar 2.18.



Gambar 2.18 Simbol dan rangkaian LED

I=V/R

Dimana : I = Arus
V = Tegangan
R = Tahanan

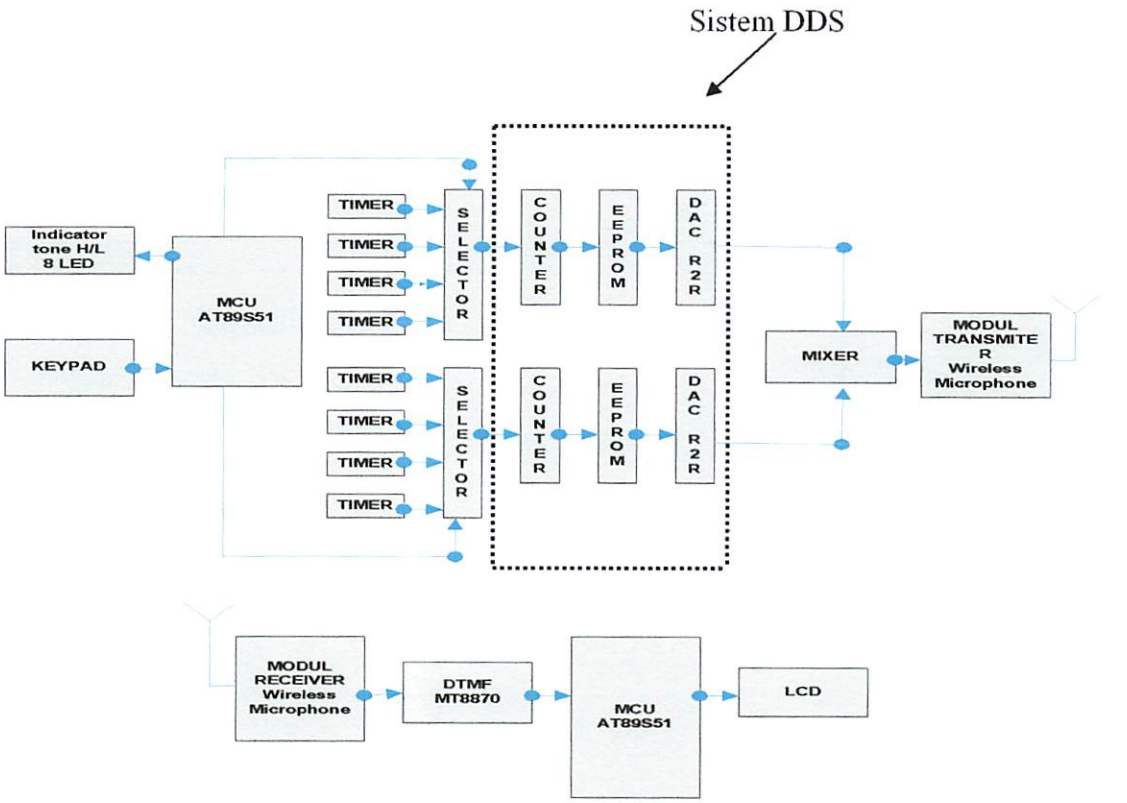
BAB III

PERENCANAAN DAN PEMBUATAN ALAT

Bab ini akan membahas tentang perencanaan dan pembuatan Modem DTMF berbasiskan DDS yang diaplikasikan pada peralatan radio komunikasi, meliputi perancangan perangkat keras (*hardware*) dan perangkat lunak (*software*), untuk lebih detailnya akan dijelaskan pada sub bab berikut ini :

3.1.Diagram Blok Rangkaian

Secara garis besar, prinsip kerja alat ini dapat digambarkan seperti pada gambar 3.1 dibawah ini:



Gambar 3.1 Blok Diagram Rangkaian

Prinsip kerja dari blok diagram diatas adalah :

1. ***Keypad***

   Keypad yang terhubung pada mikrokontroller AT89S51 berfungsi sebagai tombol untuk inputan.

2. **Mikrokontroler AT89S51**

   Berfungsi sebagai pengolah data yang akan dikirim ke sistem DDS

3. **LED**

   sebagai indikasi Tone High atau Low frekwensi DTMF 8 LED

4. ***COUNTER***

   Berfungsi untuk menggeser data biner dengan memberikan Clock

5. **EEPROM**

   Berisi data pembentuk DDS dari data 0-255 menjadi tegangan 0-5V

6. **R 2 R**

   Berfungsi untuk mengubah sinyal digital dari EEPROM menjadi output analog

7. ***Timer***

   Membangkitkan sinyal yang akan diseleksi oleh selector

8. **Selector**

   Menyeleksi sinyal yang telah di bangkitkan oleh Timer

9. ***MIXER***

   Berfungsi untuk pencampur frekuensi tinggi dan frekuensi rendah

10. **Modul *transmitter***

    Berfungsi untuk mengirim data ke modul receiver

11. Modul *receiver*

Berfungsi untuk penerima data dari modul transmitter

12. DTMF MT8870

Berfungsi sebagai pengubah data analog menjadi gelombang dual tone multy frekuensi

13. LCD

Berfungsi sebagai outputan data

3.2. Perencanaaan *Hardware*

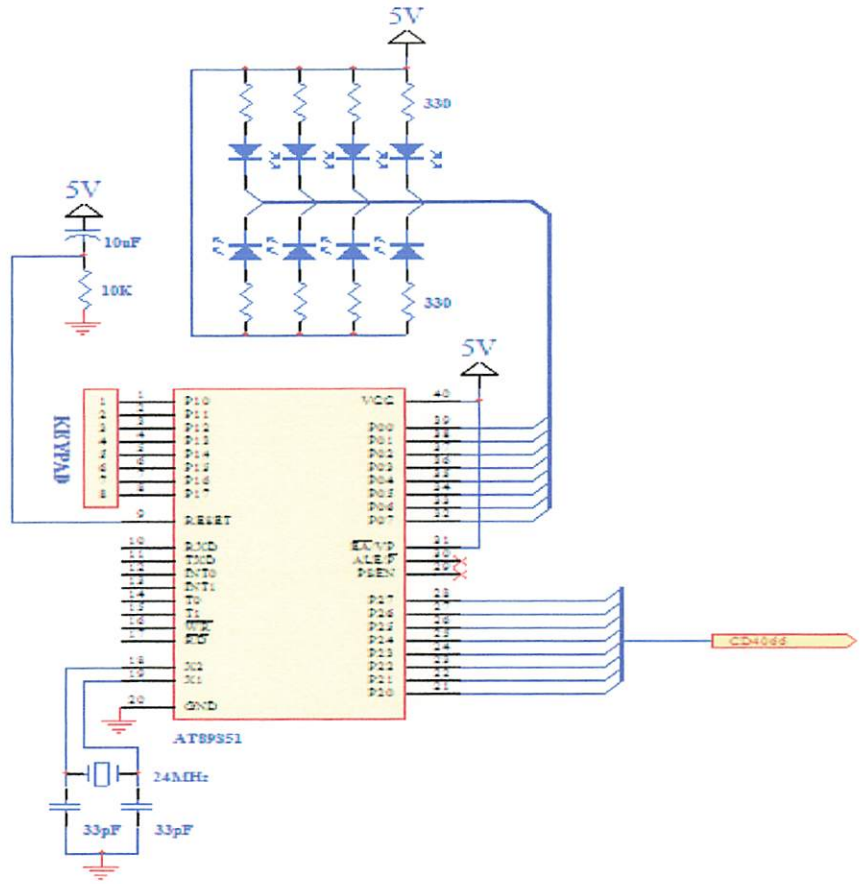
Dalam perencanaan ini rancangan *hardware* yang dibuat bertujuan guna mendukung dan memberikan kemudahan pada proses kerja perancangan *software* agar nantinya sesuai dengan kondisi yang diinginkan, Untuk perancangan *hardware* sendiri dibagi menjadi 6 bagian yaitu :

1. Minimum Sistem AT89S51
2. Antarmuka Mikrokontroler ke *keypad*
3. Sistem metode DDS
4. Minimum sistem T*imer*
5. minimum sistem *Selector*
6. Minimum Sistem Dekoder DTMF MT8870
7. Antarmuka Mikrokontroler ke modul *LCD*

3.2.1 Perancangan Minimum Sistem Mikrokontroler AT89S51

Penggunaan mikrokontroller AT89S51 harus didukung oleh beberapa rangkaian penunjang agar dapat melakukan fungsinya, antara lain rangkaian *clock* dan rangkaian

pendukung yang lain. Perancangan mikrokontroler pada box 1 dapat dilihat pada gambar 3.2 dibawah ini.

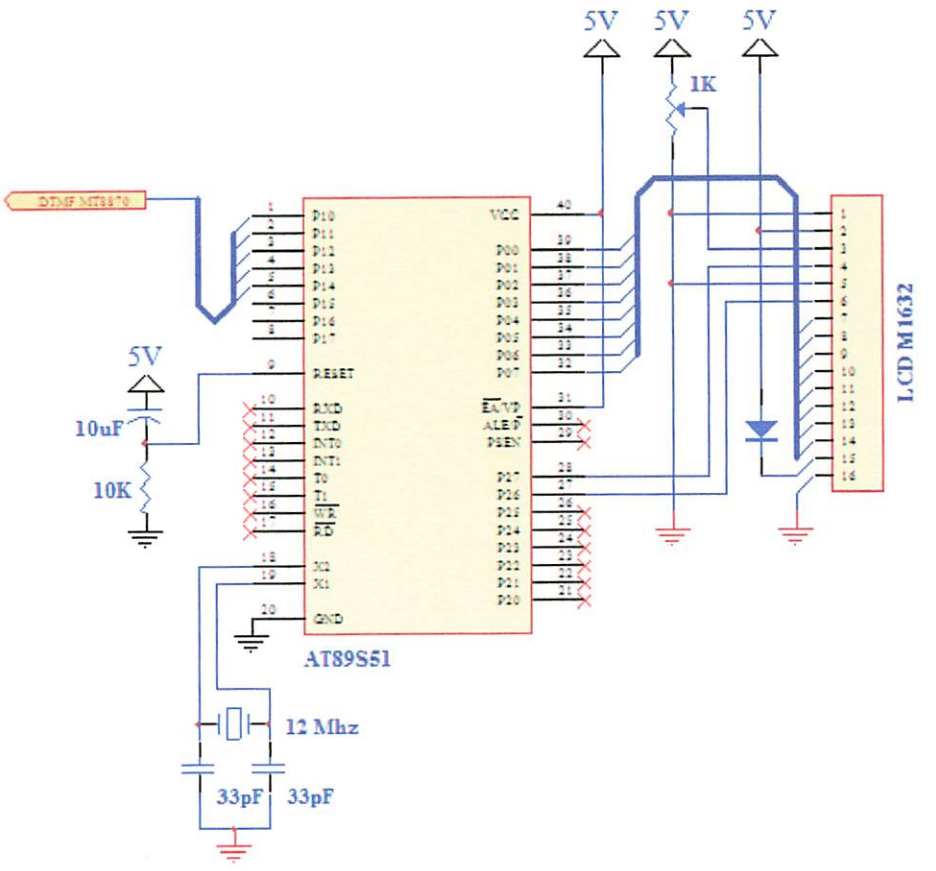


Gambar 3.2 Perancangan mikrokontroler box 1

Dari 40 pin di atas, yang kita pergunakan adalah :

1. Pin 1-8 / port(1.0-1.7) digunakan sebagai masukan (*inputan*) modul *keypad*
2. Pin 9 / Port (RST) digunakan sebagai *reset* sistem
3. Pin 18-19 / Port(XTAL1-XTAL2) digunakan sebagai sistem *clock*.
4. Pin 20 / port (GND) menuju *ground*
5. Pin 21-22 menuju Selector
6. Pin 32-39 / port (0.0-0.7) digunakan sebagai *outputan 8* LED

Perancangan mikrokontroler pada box 2 adalah seperti gambar 3.3 berikut ini



Gambar 3.3 Perancangan mikrokontroler box 2

Konfigurasi pin:

1. Pin 1-5 / port (1.0-1.4) digunakan sebagai masukan (*inputan*) DTMF MT8870
2. Pin 9 / Port (RST) digunakan sebagai *reset* sistem
3. Pin 18-19 / Port(XTAL1-XTAL2) digunakan sebagai sistem *clock*
4. Pin 20 / port (GND) menuju *ground*
5. Pin 2.7-2.8 / port (2.6 -2.7)dan 32-39 / port (0.0-0.7) digunakan sebagai keluaran (*outputan*) LCD

3.2.1.1 Rangkaian *clock*

Kecepatan proses pengolahan data pada mikrokontroller ditentukan oleh *clock* (pewaktu) yang dikendalikan oleh mikrokontroller tersebut. Pada mikrokontroller AT89S51 terdapat *internal clock generator* yang berfungsi sebagai sumber *clock*, tapi masih memerlukan rangkaian tambahan untuk membangkitkan *clock* yang diinginkan.

Rangkaian tambahan ini terdiri atas 2 buah kapasitor dan sebuah kristal yang terangkai sedemikian rupa dan kemudian dihubungkan dengan port yang khusus tersedia pada mikrokontroller.

Dalam perancangan rangkaian ini menggunakan :

- 2 Kapasitor 33 pF. Penentuan besarnya kapasitansi disesuaikan dengan spesifikasi pada data sheet.
- Kristal 24 MHz.

Dengan demikian perhitungannya dapat dilihat sebagai berikut :

f = 24 MHz

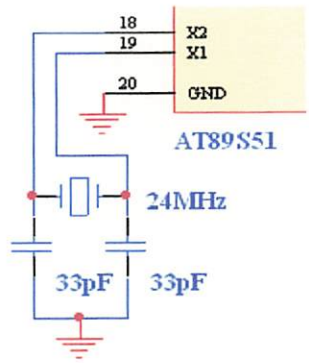
$$T = \frac{1}{f}$$

$$T = \frac{1}{24x10^6}$$

karena 1 siklus mesin = 12T maka

$$1 \text{ siklus mesin} = 12 \text{ x } \frac{1}{24x10^6} = 0{,}5\ \mu s$$

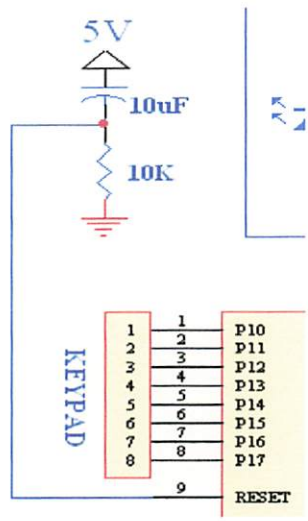
Gambar rangkaian clok adalah seperti gambar 3.4 berikut ini



Gambar 3.4 Rangkaian *Clock*

3.2.1.2 Rangkaian *reset*

Untuk *mereset* mikrokontroler AT89S51, maka pin RST diberi logika tinggi selama sekurangnya dua siklus mesin (24 periode osilator). Untuk membangkitkan sinyal *reset* kapasitor dihubungkan dengan Vcc dan sebuah resistor yang dihubungkan ke *ground*. Gambar 3.5 merupakan gambar rangkaian reset



Gambar 3.5 Rangkaian *Reset*

Rangkaian *reset* bertujuan agar mikrokontroller dapat menjalankan proses dari awal. Rangkaian *reset* untuk mikrokontroller dirancang agar mempunyai kemampuan *power on reset*, yaitu *reset* yang terjadi pada saat sistem dinyalakan untuk pertama kalinya. *Reset* juga bias dilakukan secara manual dengan menekan tombol *reset* yang berupa *switch push button.*

Rangkaian reset dalam mikrokontroller AT89S51 akan melakukan reset setelah catu daya dihidupkan. Pada saat kondisi reset maka faktor reset pada alamat 0000H akan dituju oleh mikrokontroller AT89S51 (dalam hal ini program counter) agar program yang terdapat didalam mikrokontroller kembali ke kondisi semula atau dengan kata lain mikrokontroller mengakses awal dari program yang telah diisi didalamnya. Didalam reset ini akan mengunakan beberapa macam cara untuk mereset miktrokontroller AT89S51. Cara pertama mengunakan Switch (manual), dimana user yang akan mengoperasikan switch ini. Cara ke dua mengunakan capasitor 10 uF, dimana capasitor tersebut akan berkondisi aktif high selama beberapa detik.. Karena kristal yang digunakan mempunyai frekuensi sebesar 24 MHz, maka satu periode membutuhkan waktu sebesar :

$$T = \frac{1}{f_{XTAL}} = \frac{1}{24MHz} = 4,166 \times 10^{-8}$$

Sehingga waktu minimal logika yang dibutuhkan untuk me-*reset* mikrokontroller adalah :

Reset (minimal) = T x periode yang dibutuhkan

$= 4.166 \times 10^{-8} \times 24 = 1\mu s$

Jadi mikrokontroller membutuhkan waktu minimal 1μs untuk me-*reset*. Waktu inilah yang dijadikan pedoman untuk menetukan nilai R dan C. Dengan menetukan nilai

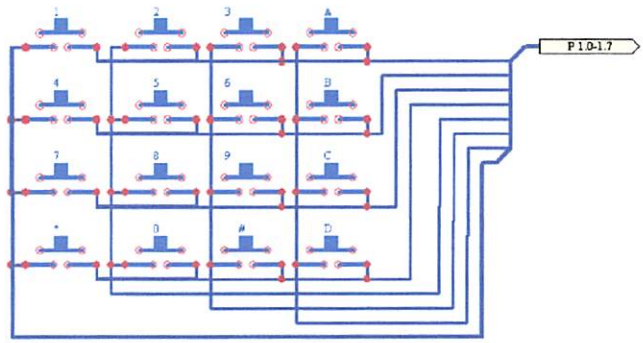
R = 10 kΩ dan C = 10 μF, maka :

$T = 0.357\ R.C = 0{,}357 \times 10000\ \Omega \times 10.10^{-6} = 35{,}7$ ms

Jadi dengan nilai komponen R = 10 kΩ dan C = 10 μF dapat memenuhi syarat minimal untuk waktu yang dibutukan mikrokontroller

3.2.2 Rangkaian *Keypad*

Keypad yang digunakan adalah keypad matriks 4x4. Port yang digunakan untuk sinyal port 1.4 – port 1.7 dari mikrokontroller masuk ke kelompok baris *keypad*, sedangkan kelompok kolom *keypad* dihubungkan ke port 1.0 – port 1.3 mikrokontroller. Untuk fungsi dari tombol-tombol *keypad* tergantung pada pemrogram. Gambar 3.6 berikut merupakan blok diagram dari penyambungan keypad ke mikrokontroller.



Gambar 3.6 Blok Diagram Hubungan Keypad Dengan Mikrokontroller.

Apabila terjadi penekanan tombol maka data yang dihasilkan dalam bentuk hexadesimal akan diterjemahkan oleh mikrokontroller menjadi desimal. Dari kombinasi penekanan tersebut menghasilkan 16 tombol atau kemungkinan yang akan terbentuk karakter angka dan simbol. Teknik pembacaan pada *keypad* ini, yaitu model *scaning* 4 jalur baris dan 4

jalur kolom. Bila baris dan kolom ini disilangkan maka akan terbentuk titik-titik potong yang membentuk *matrik* 4x 4.

3.2.3 Rangkaian *Counter*

Counter atau rangkaian penghitung adalah rangkaian logika sequensial yang dapat dipergunakan untuk menghitung jumlah pulsa yang masuk dan dinyatakan dengan suatu bilangan biner. Pewaktu (*Timer*) memegang peranan penting dalam pengoperasian *counter*, didalam rangkaian ini *counter* akan menggeser data biner dengan memberikan clock menuju EEPROM.

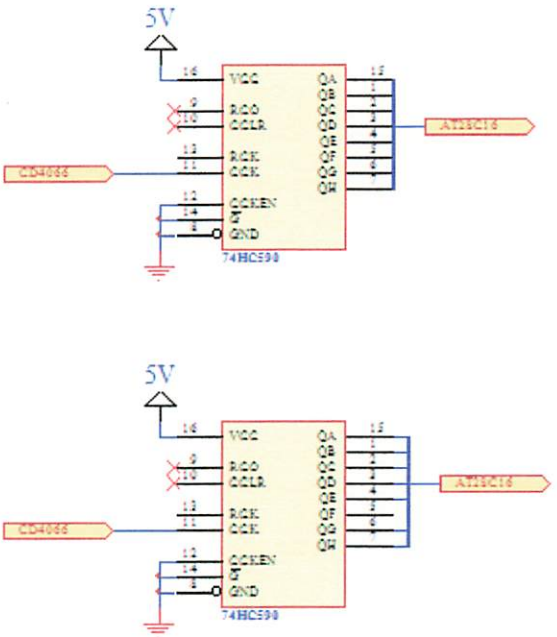
Counter digital memiliki karakteristik penting:

1. Jumlah hitungan maksimum (*Modulus counter*)
2. Menghitung ke atas atau ke bawah
3. Operasi asinkron atau sinkron
4. Bergerak bebas atau berhenti sendiri

Ada beberapa jenis counter dalam pembahasan sistem digital, diantaranya yaitu *Binary Counter*, *Up Counter*, *Down Counter*, *Johnson Counter*, *Decade Counter*, dan masih banyak lagi. Namun, dalam makalah ini akan dibahas tentang Decade Counter atau dikenal juga *Ripple Counter Modulo*-10.

Pencacahan sekuensial/berurutan dari *counter modulo*-10 atau decade counter adalah dari 0000 sampai 1001 (0 hingga 9 desimal). Counter mod-10 memiliki 4 bit dengan harga: 8-an, 4-an, 2-an dan 1-an. Untuk itu dibutuhkan empat *flip-flop* yang dihubungkan seperti Ripple Counter. Kita harus menambahkan gerbang NAND untuk menghapus (*clear*) semua *flip-flop* kembali ke keadaan nol segera sesudah hitungan ke- 10. Karena modulus-

10 menghitung hingga 9 (1001), maka hitungan berikut (10 – 1010) digunakan untuk menghasilkan pulsa *reset*. Hal ini dilakukan dengan mengumpankan kedua logika 1 pada 1010 kedalam gerbang NAND yang akan mereset seluruh *flip-flop* kembali ke 0000 lagi. Maka counter akan menghitung mulai 0000 hingga 1001 lagi. Dengan menggunakan gerbang NAND, kita dapat membuat sejumlah counter modulo yang lain, dengan tetap memperhatikan logika 1 sebagai "tanda" tercapainya batas penghitungan. Counter ini dapat dibangun dari berberapa *flip-flop* individual, namun juga diproduksi keempat *flip-flop* dalam satu paket IC, yang bahkan sudah menyertakan gerbang reset NAND. Rangkaian Counter pada skripsi ini ditunjukan seperti gambar 3.7 dibawah ini.

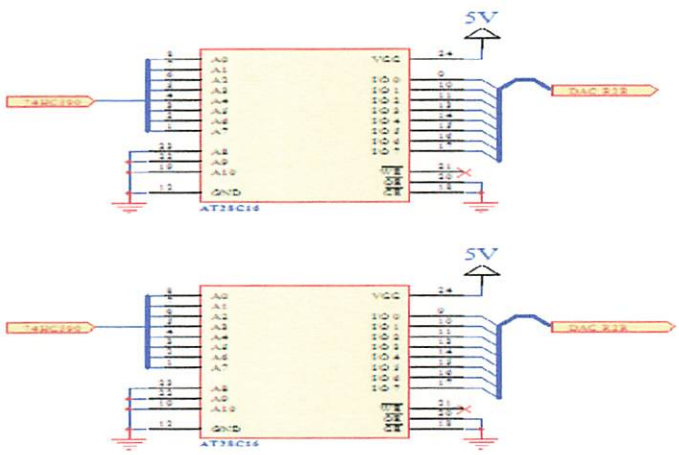


Gambar 3.7 Rangkaian *Counter*

3.2.4 Rangkaian EEPROM

EEPROM merupakan kependekan dari *Electrically Erasable Programmable Read-Only Memory*. Dalam rangkaian ini EEPPROM yang digunakan adalah tipe AT28C16 yang memiliki kapasitas memori 16 Kb, EEPROM dalam rangkaian ini digunakan untuk menyimpan data DDS 0-255 yang akan dikirim ke DAC menjadi sinyal Analog.

EEPROM sangat mirip dengan flash memory yang disebut juga flash EEPROM. Perbedaan mendasar antara flash memory dan EEPROM adalah penulisan dan penghapusan EEPROM dilakukan dilakukan pada data sebesar satu byte, sedangkan pada flash memory penghapusan dan penulisan data ini dilakukan pada data sebesar satu block. Oleh karena itu flash memory lebih cepat. Seperti juga tipe PROM lainnya, EEPROM dapat menyimpan isi datanya, bahkan saat listrik sudah dimatikan. Gambar 3.8 merupakan gambar dari rangkaian EEPROM.



Gambar 3.8 Rangkaian EEPROM

3.2.5 Rangkaian *Digital Analog Converter* (DAC) R-2R

Digital To Analog Converter R 2 R digunakan untuk mengkonversi data *digital* menjadi sinyal *analog*. Pada umumnya semua bentuk konverter *digital* ke *analog* akan menghasilkan suatu keluaran yang berupa arus dan tegangan yang merupakan bentuk hasil perkalian antara tegangan analog referensi dengan data digital tertentu (*Multiplying D/A Converter*).

Karena konverter *digital* ke *analog* ini banyak macamnya, maka pada umumnya dipakai cara konversi dengan rangkaian resistor berbobot (*binary weighted resistor*) dimana posisi dari bit digital yang akan diberikan akan menghasilkan besar arus tegangan yang sesuai bobot biner pada data *digital*. Didalam penerapannya, cara pemakaian harga tahanan yang bervariasi akan menimbulkan kesulitan dalam memilih harga tahanan yang sesuai, sehingga dipakai rangkaian tangga tahanan R-2R yang lebih sederhana.

Tahanan keluaran V*out* dapat dihitung dengan rumus berikut;

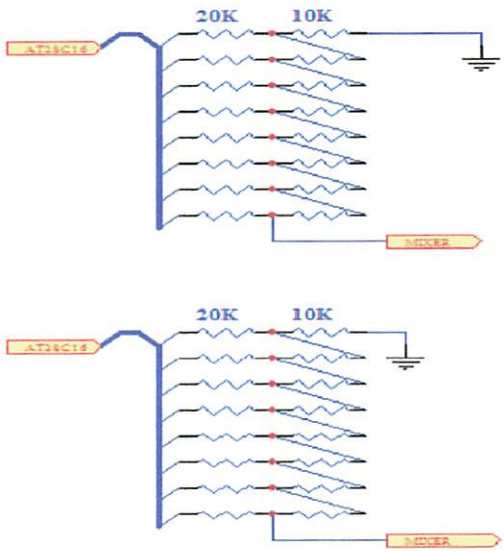
$$\text{Vout} = - \frac{Rf}{R} Vref \left(\frac{D_0}{2^n} + \frac{D_1}{2^{n-1}} + \frac{D_2}{2^{n-2}} \right) - \left(\frac{D_{(n-2)}}{2^2} + \frac{D_{(n-1)}}{2^1} \right)$$

Dimana: $D_0 ... D_1$ = bernilai 1 atau 0

n = banyaknya bit masukan

Vre = tegangan referensi

Gambar 3.9 menunjukan rangkaian DAC R-2R sebagai pengubah data digital ke analog.



Gambar 3.9 Rangkaian DAC R-2R (Digital Analog Converter)

3.2.6 *Timer* IC LM555

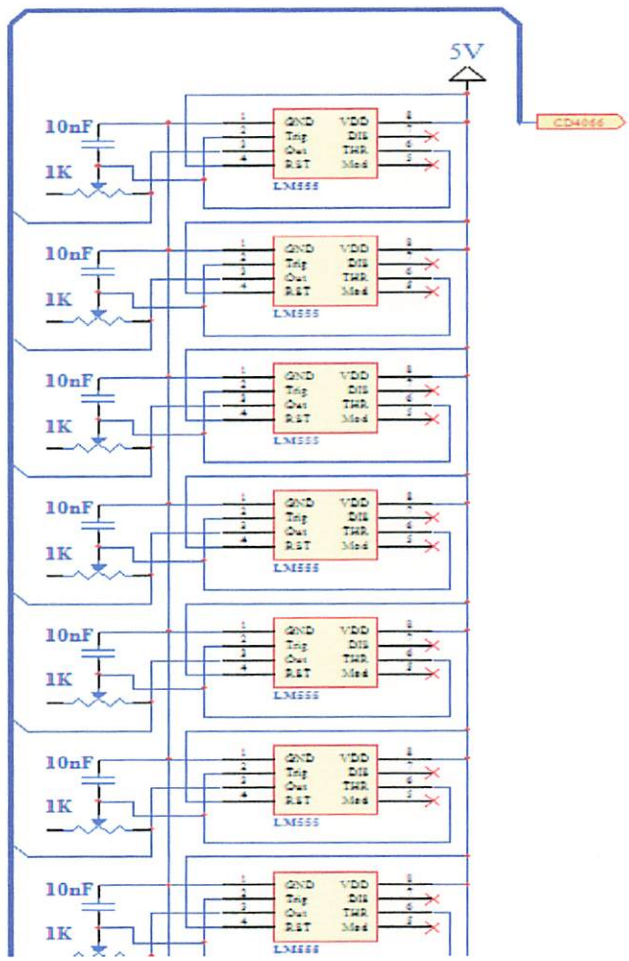
Pada perancangan ini digunakan IC LM555 sebagai pembangkit sinyal yang berbentuk square. Rangkaian yang dibuat pada perancangan alat ini adalah rangkaian astable, dimana besar pulsa yang dihasilkan dapat di atur, dengan cara menentukan besar resistor dan capasitor yang digunakan.

Output dari IC ini di hubungkan dengan Selector CD4066, Clock dari IC 555 ini diseleksi oleh Selector sesuai inputan dari keypad dan akan diteruskan ke Counter .

$$F = \frac{1}{1{,}1.R..C} \qquad R = 1\ K\Omega \quad C = 1\ nF$$

$$F = \frac{1}{1{,}1.(1.10^{3}).(10.10^{-9})} \qquad F = \frac{1}{11.10^{-6}} \qquad F = \frac{1.10^{5}}{1{,}1} \qquad F = 9090{,}90\ Hz$$

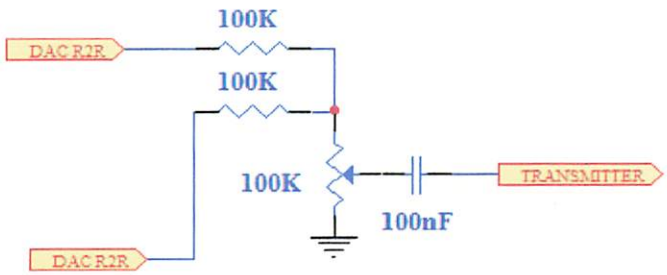
Gambar 3.10 menunjukan perancangan Rangkaian Timer LM555 sebagai pembangkit sinyal



Gambar 3.10 Rangkaian *Timer* LM555

3.2.7 *Mixer*

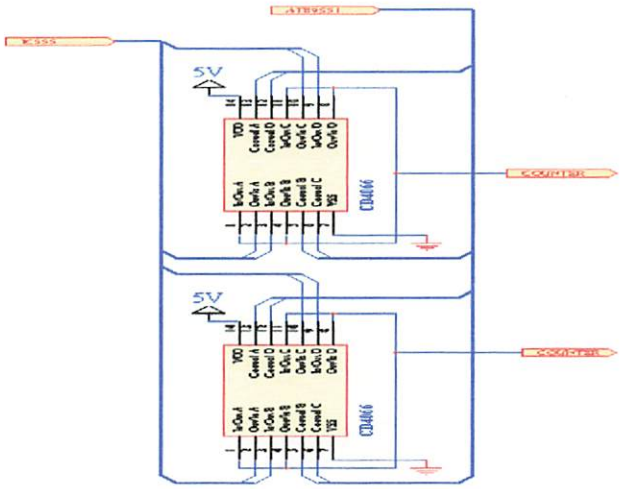
Dalam laporan ini mixer bertugas mencampur sinyal analog yang dihasilkan dari dua buah DAC-R2R yang akan dikirimkan ke Transmitter sebelum ditransmisikan ke Receiver. Rangkaian *Mixer* dapat dilihat pada gambar 3.11



Gambar 3.11 Rangkaian *Mixer*

3.2.8 *Selector*

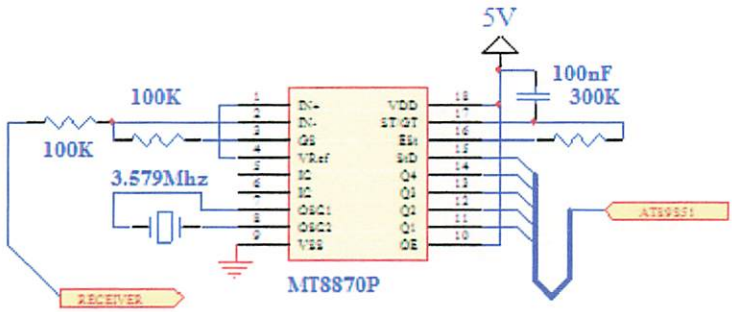
Dalam laporan ini Selector berfungsi menyeleksi sinyal manakah yang akan dikirim ke *Counter* yang sebelumnya telah dibangkitkan oleh *Timer*. *Selector* menggunakan IC CD4066 yang dapat digunakan untuk mentransmisikan dari sinyal analog maupun digital, rangkaian Selector dapat ditunjukan pada gambar 3.12



Gambar 3.12 Rangkaian *selector*

3.2.9 Minimum Sistem Dekoder DTMF MT8870

Dekoder DTMF MT8870, Decoder DTMF merupakan rangkaian yang dapat menghasilkan kode biner dari sinyal DTMF. Dalam rangkaian ini DTMF MT8870 mempunyai bentuk tugas merubah sinyal analog yang dikirim melalui receiver menjadi gelombang dual tone multy frekwensi. Rangkaian DTMF MT8870 dapat ditunjukan pada gambar 3.13.

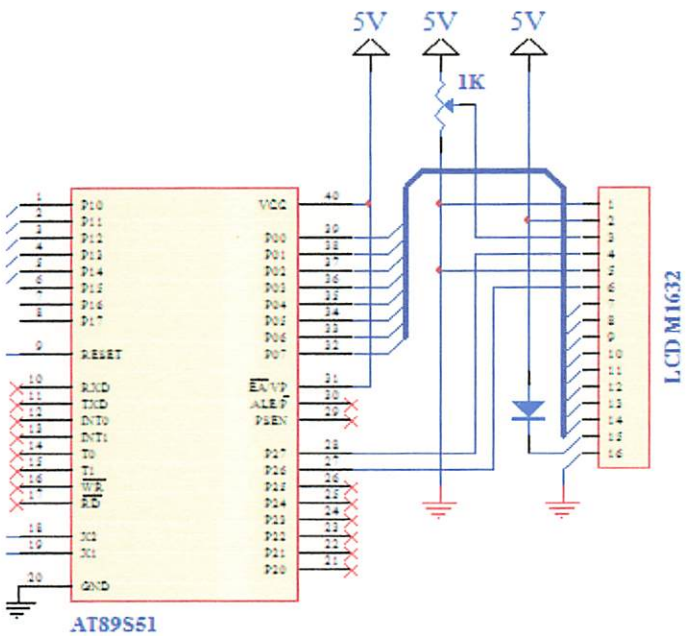


Gambar 3.13 Rangkaian DTMF MT8870

Decoder ini mengkodekan sinyal– sinyal DTMF menjadi kode biner (*binary code*) 4 bit. Decoder ini telah dilengkapi dengan filter untuk frekuensi tinggi (*high frequency*) dan frekuensi rendah (*low frequency*) serta sebuah digital decoder. Filter menggunakan *switched capacitor* untuk membedakan frekuensi yang masuk, sedang decoder menggunakan teknik pencacahan (*counting techniques*) secara digital untuk mendeteksi dan mengkodekan 16 buah pasangan frekuensi DTMF menjadi kode biner 4 bit. Selain itu, MT8870 juga dilengkapi dengan rangkaian internal penguat differential, *oscillator clock*,dan sebuah rangkaian latch 3 state pada bagian *output*. Dengan demikian rangkaian external tambahan untuk membentuk sebuah decoder DTMF yang lengkap dapat dikurangi.

3.2.10 LCD (*Liquid Crystal Display*)

Dalam aplikasi ini menggunakan sebuah layar LCD (*Liquid Crystal Display*) yaitu jenis M1632 yang merupakan LCD dua baris dengan setiap barisnya terdiri atas 16 karakter. Masukan yang diperlukan untuk mengendalikan modul ini berupa bus data yang masih ter-*multiplex* dengan bus alamat. Sementara pengendalian dot matrik LCD dilakukan secara internal oleh kontroler yang sudah terpasang pada modul LCD. Rangkaian LCD dapat ditunjukan pada gambar 3.14



Gambar 3.14 Rangkaian LCD

Konfigurasi pin – pin pada *Liquid Crystal Display* (LCD) sebagai berikut:

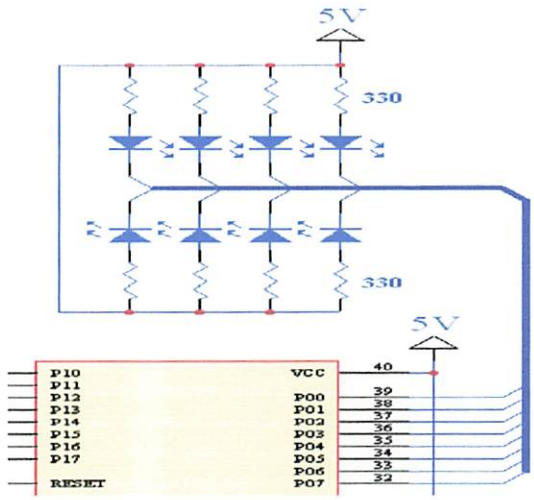
- Pin 1, 3 dan 5 dihubungkan dengan trinpot 1K untuk pengaturan kecerahan pada *Liquid Crystal Dispaly* (LCD).
- Pin 2 sebagai Vcc dihubungkan ke tegangan sumber +5 Volt DC.

- Pin 4 sebagai *Sinyal Register* (SR) yang dihubungkan dengan pin 28 pada mikrokontroler 2
- Pin 6 sebagai *Enable* (E) yang dihubungkan dengan pin 27 pada mikrokontroler 2
- Pin 7 – 14 sebagai *bit bus* data *Lower* dan *Upper* dua arah yang dihubungkan dengan port0-port7.
- Pin 15 pada LCD yang dihubungkan dengan kaki katoda dioda agar tegangan yang masuk sesuai data sheet 4,3V.
- Pin 16 sebagai *Ground.*

3.2.11 Rangkaian LED (*Light Emiting Dioda*)

LED adalah dioda semi konduktor yang khusus yang dirancang untuk memancarkan cahaya apabila arus melaluinya. Apabila diberi bias maju, energi electron yang mengalir melewati tahanan sambungan diubah langsung menjadi energi cahaya. Karena LED adalah dioda, maka arus hanya akan mengalir apabila LED dihubungkan dengan bias maju.

Keuntungan utama penggunaan LED sebagai sumber cahaya dibandingkan dengan bola lampu cahaya biasa adalah penggunaan daya yang jauh lebih rendah, jauh lama umurnya, dan beroperasi dengan kecepatan tinggi. Dalam aplikasi ini LED digunakan untuk mengetahui frekwensi DTMF yang aktif HIGH dan LOW. Gambar 3.15 menunjukan gambar rangkaian LED.



Gambar 3.15 Rangkaian LED

V = 5 V , V LED = 1,8 V , I LED = 10 mA, I LED = 10 mA

$$\text{R LED} = \frac{V - VLED}{I}$$

$$\text{R LED} = \frac{5 - 1{,}8}{10} = 0{,}32 \text{ K}\Omega = 330\ \Omega$$

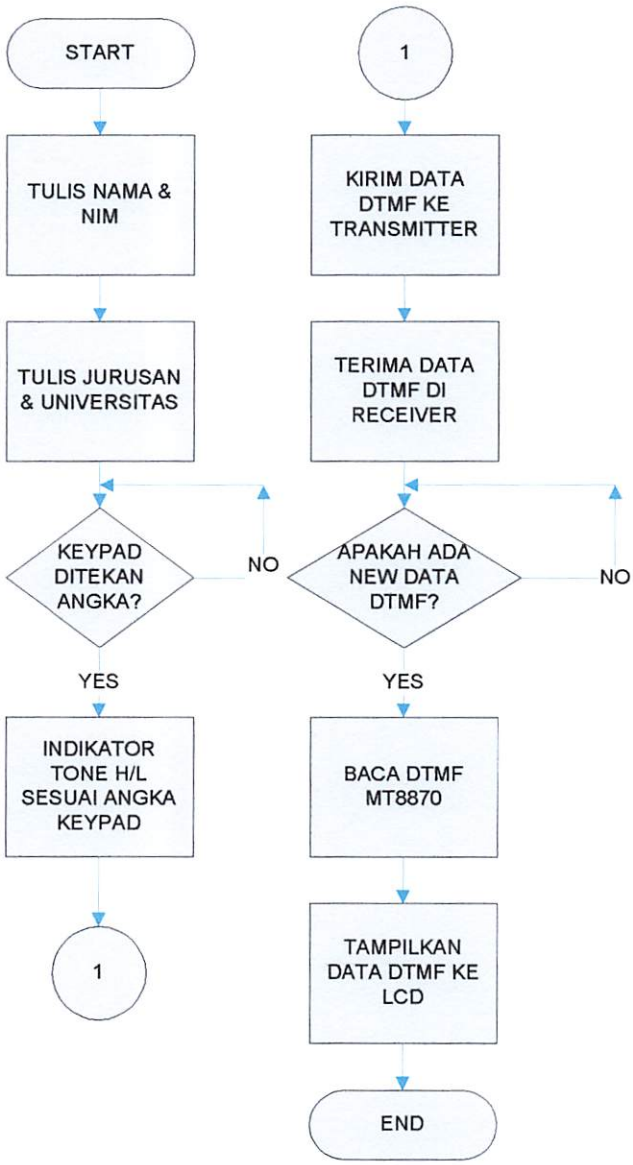
3.3 Perencanaan Perangkat Lunak / *Software*

3.3.1 *Software* di Mikrokontroller (MCU)

Untuk pemakaian mikrokontroler di dalam suatu sistem, perlu direncanakan perangkat lunak mikrokontroler yang dapat mengatur sistem tersebut. Perangkat lunak disini adalah susunan perintah-perintah (program) di dalam memori yang harus dilaksanakan adalah mikrokontroler. Di dalam suatu mikrokontroler memori merupakan suatu fasilitas utama karena disinilah disimpan perintah-perintah yang harus dijalankan. Memori disini dapat dibedakan menurut fungsinya menjadi memori program dan memori

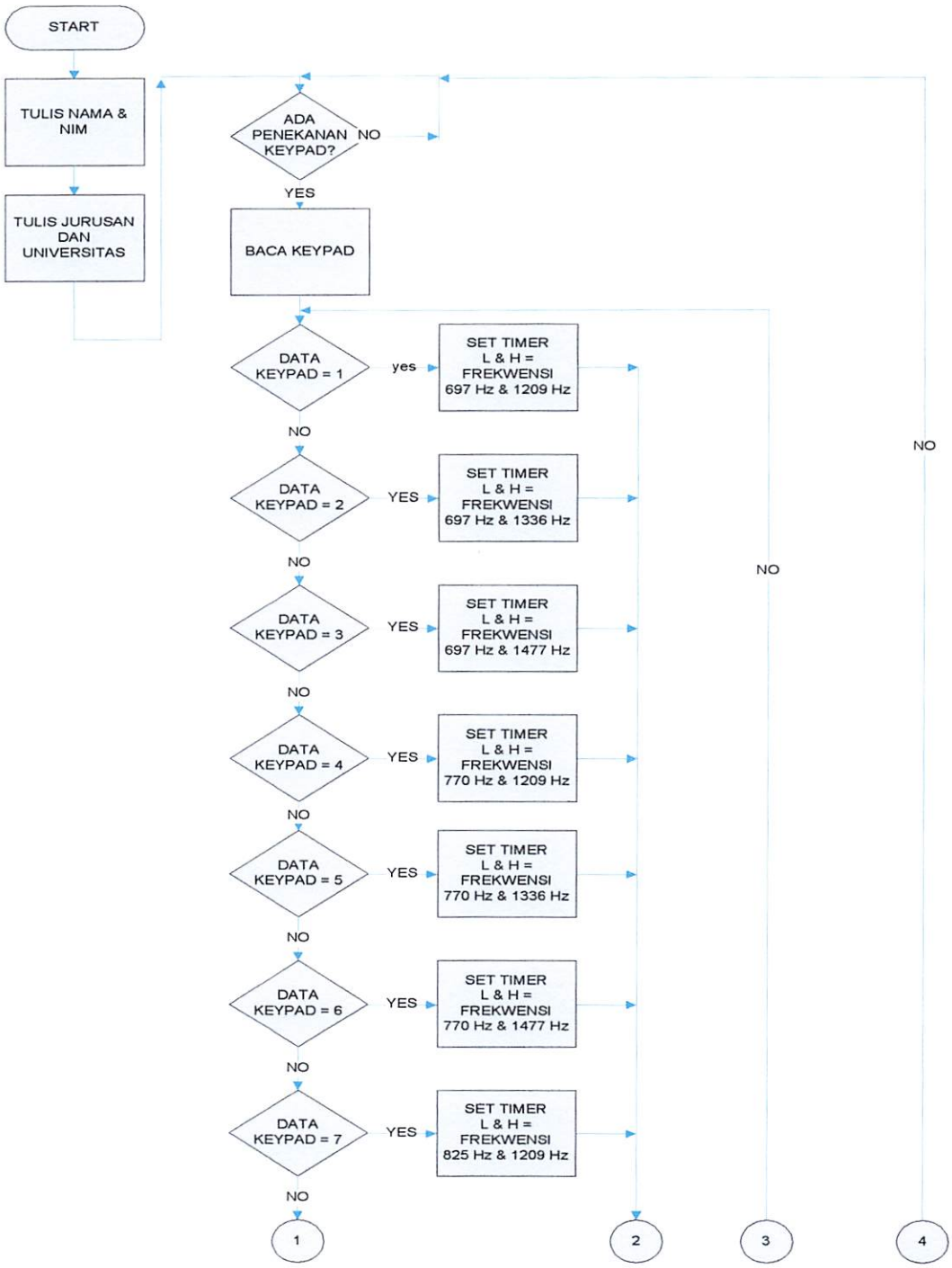
data. *Software* dari alat tersebut terdapat dibagian lampiran dan diagram alirnya adalah seperti terlihat pada gambar 3.16 berikut ini :

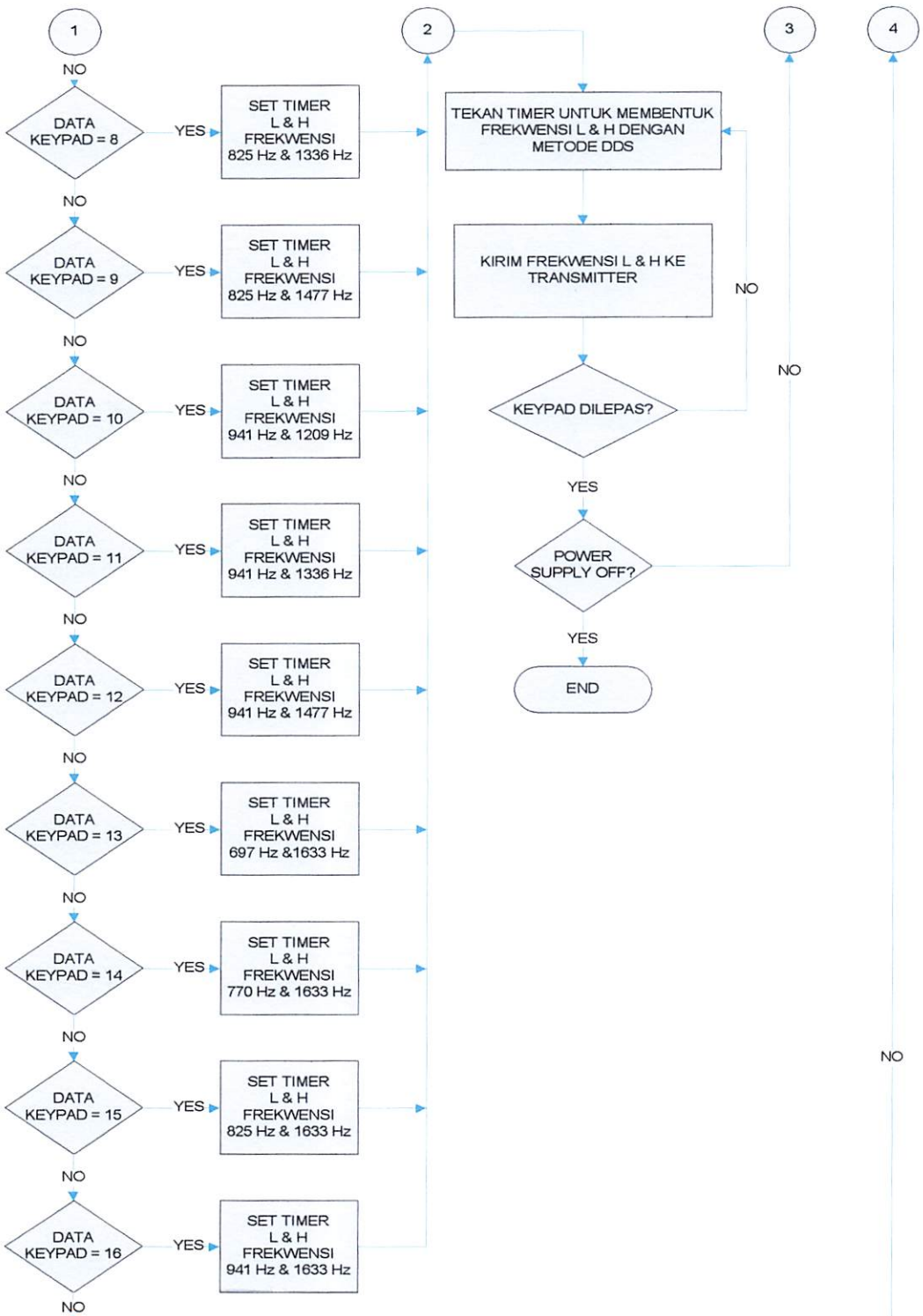
3.3.2 Flowchart Kerja Rangkaian Keseluruhan



Gambar 3.16 Flowchart Kerja Rangkaian Keseluruhan

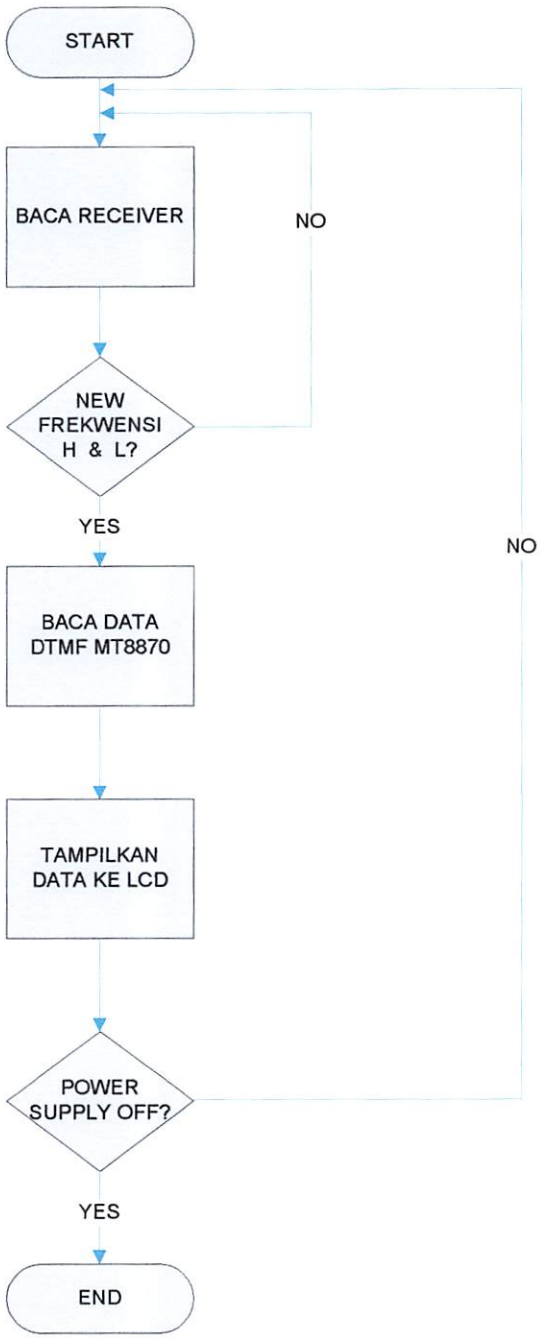
3.3.3 Flowchart Box 1





Gambar 3.17 Flowchart Box 1

3.3.4 Flowchart Box 2



Gambar 3.18 Flowchart Box 2

BAB IV

PENGUJIAN ALAT

Bab ini akan membahas pengujian alat yang telah dirancang, dirakit serta direalisasikan. Tujuan pengujian alat ini adalah mengetahui kerja dari masing-masing sistem yang dibuat secara per-Blok. Dengan demikian dapat diketahui kepresisian kerja dari alat yang direncanakan dan dibuat. Secara umum tujuan dari pengujian alat tersebut adalah sebagai berikut :

1. Mengetahui proses kerja dari masing-masing rangkaian (Blok).
2. Memudahkan pendataan spesifikasi alat.
3. Mengetahui hasil dari suatu perencanaan yang telah dibuat.
4. Memudahkan perawatan dan perbaikan apabila sewaktu-waktu terjadi kerusakan.

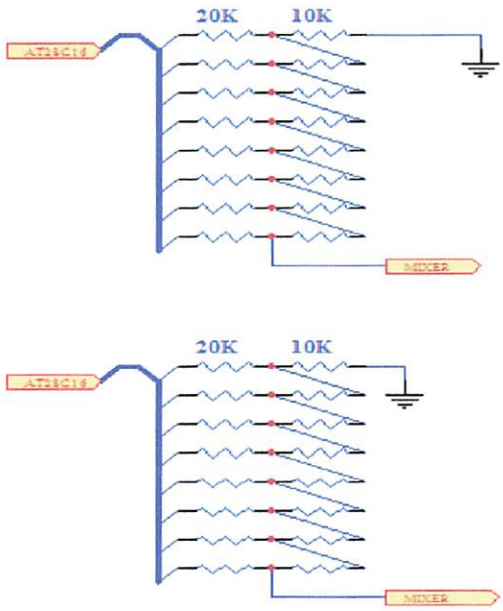
4.1 Pengujian Rangkaian DAC R2R

4.1.1. Tujuan

Pengujian rangkaian DAC R2R ini bertujuan untuk mengetahui bagaimana kondisi sinyal sinusoida pada saat dijalankan.

4.1.2. Langkah- Langkah Pengujian

1. Menyusun rangkaian DAC R2R seperti pada gambar 4-1.
2. Rangkaian minimum sistem AT89S51
3. Menggunakan multitester digital
4. Menghubungkan rangkaian DAC R2R dengan tegangan Vcc (5V).
5. Mengamati hasil pengujian.seperti pada gambar 4.1



Gambar 4.1 Rangkaian DAC R2R

4.1.3. Hasil dan Analisa

Setelah melakukan pengujian DAC R2R maka hasil yang diperoleh adalah sebagai berikut :

Tabel 4.1 Hasil Perhitungan dan Pengukuran DAC

No	Data Digital		Tegangan (V)		*Error* (%)
	Desimal	Biner	Pengukuran	Perhitungan	
1	0	00000000	0	0	0
2	25	00011001	2,95	2,96	0.01
3	51	00110011	3,96	3.98	0.02

4	77	01001101	3,44	3.47	0.03
5	103	01100111	4,47	4,49	0.02
6	129	10000001	2.49	2.51	0.02
7	155	10011011	4,48	4,5	0.02
8	182	10110110	1,18	1.19	0.01
9	208	11010001	2,6	2,63	0.03
10	233	11101001	2,93	2,94	0.01
11	255	11111111	4,97	4,98	0.01

Sedangkan hasil perhitungan tegangan analog yang keluar dari rangkaian DAC R2R menggunakan rumus sebagai berikut :

$$\text{Vout} = Vref\left(\frac{D_0}{128}+\frac{D_1}{64}+\frac{D_2}{32}+\frac{D_3}{16}+\frac{D_4}{8}+\frac{D_5}{4}+\frac{D_6}{2}+\frac{D_7}{1}\right)$$

Ket :

Vref = 5 V

Dn = Logika bit ke – ^{n}

$$\text{Vout} = 5x\left(\frac{0}{256}+\frac{0}{128}+\frac{0}{64}+\frac{1}{32}+\frac{1}{16}+\frac{0}{8}+\frac{0}{4}+\frac{1}{2}\right)$$

V_{out} = 2,96V

Dari contoh perhitungan, maka nilai tegangan analog hasil keluaran dari DAC R2R bisa diketahui. Dengan diketahuinya nilai tegangan analog keluaran DAC R2R hasil pengujian dan perhitungan, maka % kesalahan dapat diketahui dengan rumusan sebagai berikut :

$$Error \text{ rata-rata} = \frac{jumlaherror}{banyaknyapercobaan}$$

$$= \frac{0{,}18}{11} = 0{,}016\%$$

Adapun perbandingan antara tegangan keluaran DAC R2R hasil perhitungan, hasil pengujian dan % kesalahan yang terjadi ditampilkan pada tabel 4.1

4.2. Pengujian LCD

4.2.1. Tujuan

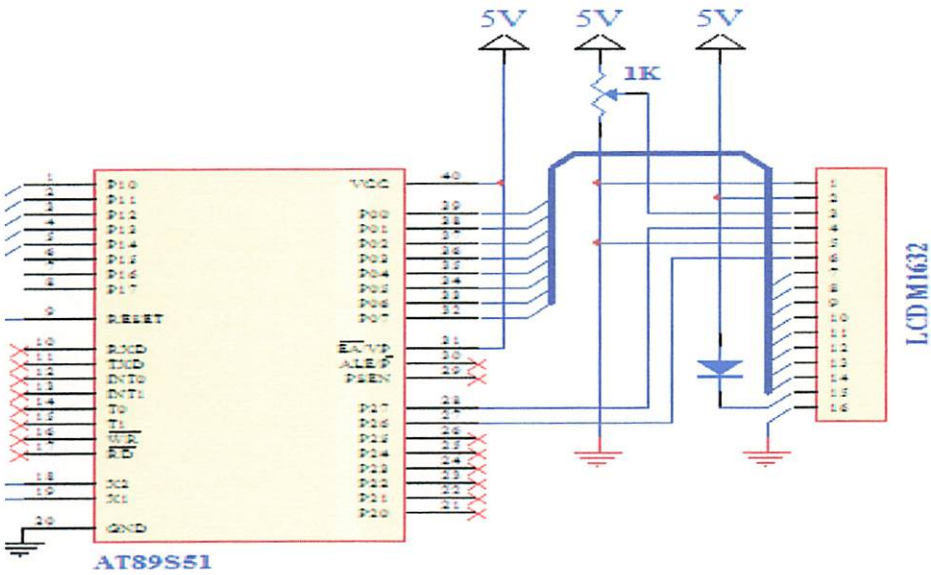
Adapun tujuan dari pengujian rangkaian ini untuk mengetahui kondisi keluaran LCD yaitu sebagai tampilan,juga mencatat nilai tegangan yang masuk pada LCD sebelum dan sesudah melewati diode.

4.2.2. Alat-alat yang digunakan

- LCD
- Rangkaian mikrokontroler AT 89S51
- Catu daya.
- Voltmeter digital

4.2.3. Langkah-Langkah Pengujian

1. Menyusun rangkaian pengujian seperti pada gambar 4.2

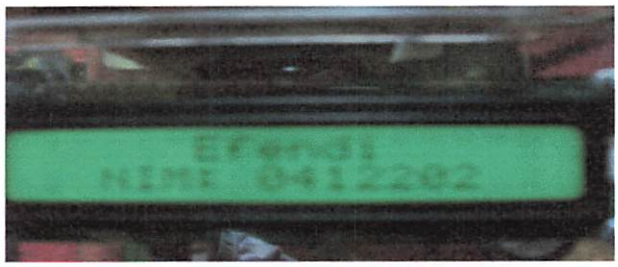


Gambar 4.2 Rangkaian Pengujian LCD

2. Membuat *software* pengujian rangkaian LCD, program ini berisi inisialisasi *mikrokontroler* dan LCD.
3. Mengaktifkan catu daya.
4. Mengoperasikan program dan hasil keluaran akan ditunjukkan pada layar penampil kristal cair.
5. Mengukur besarnya tegangan awal yang masuk pada LCD dan tegangan setelah lewat pada dioda.

4.2.4. Hasil pengujian

Dari hasil pengujian maka didapatkan tampilan seperti yang terlihat pada gambar 4.3:



Gambar 4.3 Tampilan Pengujian LCD

Cara menampilkan data diatas adalah dengan memasukan progam seperti dibawah ini :

```
Delay1: acall   delay0
        djnz    Dly1,delay1
        ret
delay2: mov   dly2, #20
dely2:  acall   delay1
        djnz    dly2,delay2
        ret
nama:  DB     '  Efendi  '
nim:   DB     ' NIM: 0412202 '
jurs:  DB     ' Teknik Elektro '
univ:  DB     '  ITN Malang  '
judul: DB     '  Data DTMF   '
angka: DB     '  0123456789  '
```

dan pada waktu pertama dinyalakan maka akan keluar seperti tabel 4.2

Tabel 4.2 Hasil Pengujian Rangkaian LCD

No	Tegangan Awal LCD (Volt)	Tegangan Setelah Melewati Dioda (Volt)
1	4,87	4,25

Gambar 4.4 menunjukan pengukuran tegangan awal pada LCD

Gambar 4.4 Pengukuran Tegangan Awal LCD

Gambar 4.5 menunjukan pengukuran tegangan setelah melewati dioda

Gambar 4.5 Pengukuran Tegangan Setelah Melewati Dioda.

4.3. Pengujian Keypad 4 x 4

4.3.1. Tujuan

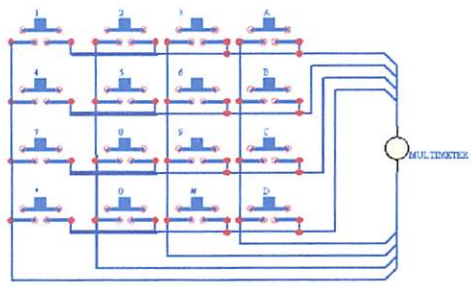
Untuk menguji apakah tombol keypad dapat bekerja sebagai inputan,dan mensimulasikan tombol yang ditekan melalui suara buzzer pada multimeter digital.

4.3.2. Alat yang digunakan

- Multimeter digital
- Keypad

4.3.3. Prosedur Pengujian

1. Menyusun rangkaian pengujian keypad seperti pada gambar 4.6



Gambar 4.6 Pengujian Rangkaian *Keypad.*

2. Memberikan kombinasi masukan dengan menekan tombol-tombol *keypad* dengan memasukan program sebagai berikut:

```
;
klmpk0: DB    '.1'          ; 2
klmpk1: DB    'abc2'        ; 4
klmpk2: DB    'def3'        ; 4
klmpk3: DB    'ghi4'        ; 4
klmpk4: DB    'jkl5'        ; 4
klmpk5: DB    'mno6'        ; 4
klmpk6: DB    'pqrs7'       ; 5
klmpk7: DB    'tuv8'        ; 4
```

```
klmpk8: DB    'wxyz9'          ; 5
klmpk9: DB    ' 0'             ; 2
;
```

3. Mengamati hasil penekanan *keypad.* Kemudian mencatat hasil pengamatan pada tabel 4.3

4.3.4. Hasil Pengujian

Tabel 4.3 Hasil Pengujian *Keypad.*

TOMBOL	BARIS				KOLOM			
	1	2	3	4	1	2	3	4
1	1	0	0	0	1	0	0	0
2	1	0	0	0	0	1	0	0
3	1	0	0	0	0	0	1	0
A	1	0	0	0	0	0	0	1
4	0	1	0	0	1	0	0	0
5	0	1	0	0	0	1	0	0
6	0	1	0	0	0	0	1	0
B	0	1	0	0	0	0	0	1
7	0	0	1	0	1	0	0	0
8	0	0	1	0	0	1	0	0
9	0	0	1	0	0	0	1	0
C	0	0	1	0	0	0	0	1
#	0	0	0	1	1	0	0	0

0	0	0	0	1	0	1	0	0
*	0	0	0	1	0	0	1	0
D	0	0	0	1	0	0	0	1

*Keterangan : cara membaca tabel diatas adalah jika antara baris dan kolom terhubung (1) maka akan membentuk matrik baris dan kolom sesuai penekanan tombol *keypad.*

4.4. Pengukuran frekuensi wireless

4.4.1. Tujuan

Adapun tujuan dari pengujian rangkaian ini untuk mengetahui frekuensi yang dipancarkan oleh microphone wireless yaitu 113.908 MHz.

4.4.2. Alat-alat yang digunakan

- Modul microphone wireless
- Frekuensi Counter

4.4.3. Hasil pengujian

Dari hasil pengujian maka didapatkan tampilan seperti yang terlihat pada gambar 4.7

Gambar 4.7 Pengukuran frekuensi microphone wireless

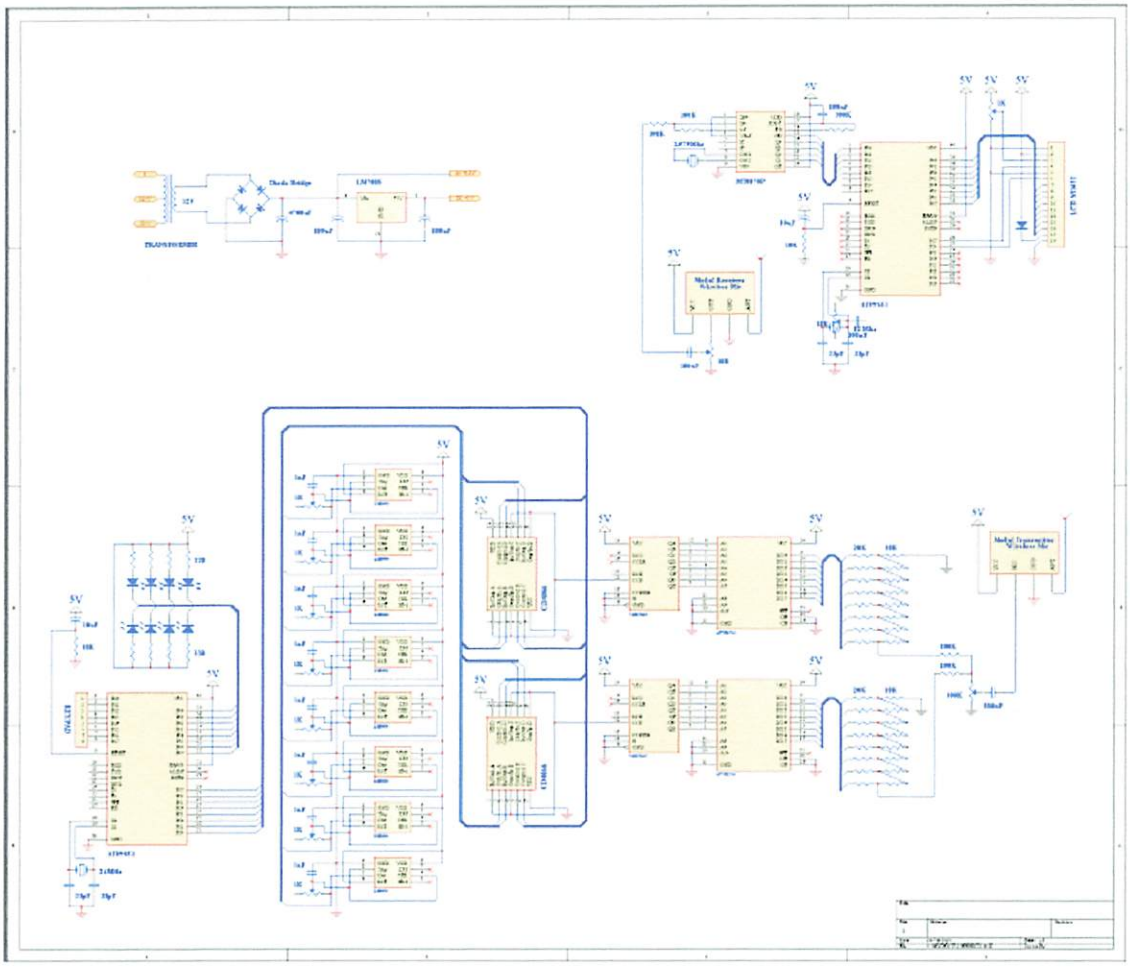
4.5. Pengujian Rangkaian keseluruhan

4.5.1. Tujuan

Pengujian ini bertujuan untuk mengetahui kinerja perangkat keras secara keseluruhan apabila dijalankan.

4.5.2. Langkah-Langkah Pengujian

1. Menyusun rangkaian keseluruan seperti pada gambar 4.8
2. Menghubungkan rangkaian keseluruan dengan jala-jala listrik.
3. Mengamati hasil yang ditunjukan pada LCD.



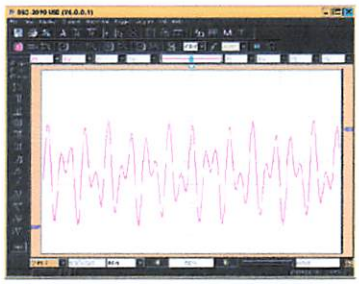
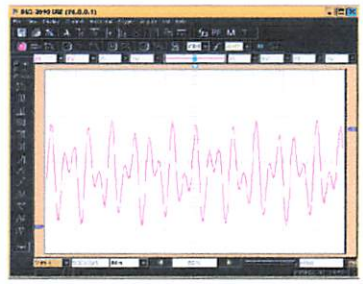
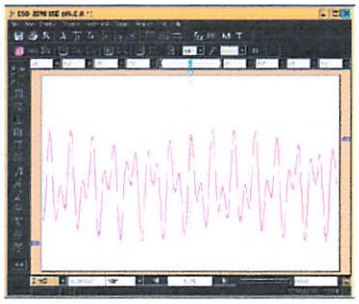
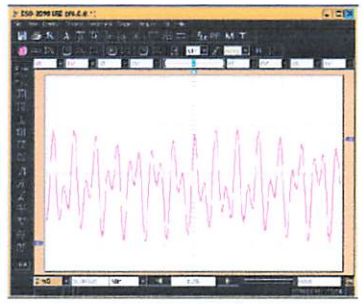
Gambar 4.8 Rangkaian Keseluruhan

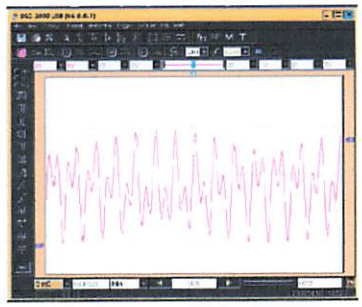
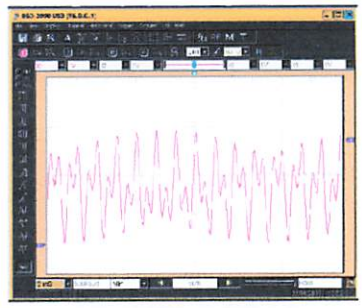
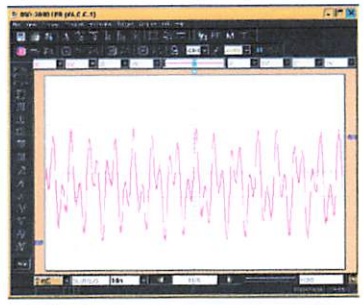
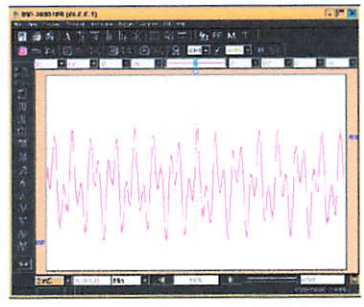
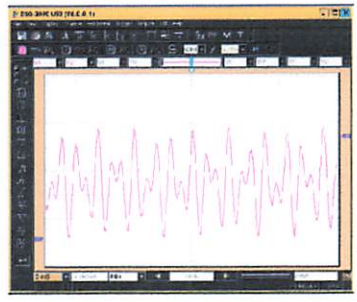
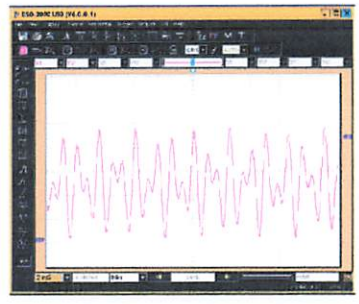
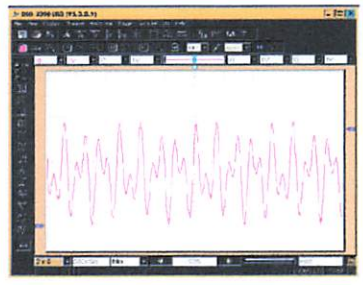
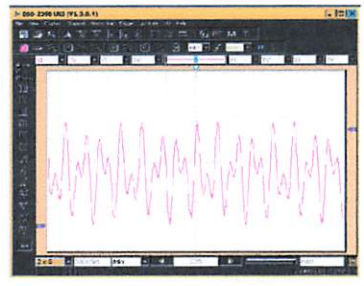
4.5.3. Hasil dan Analisa

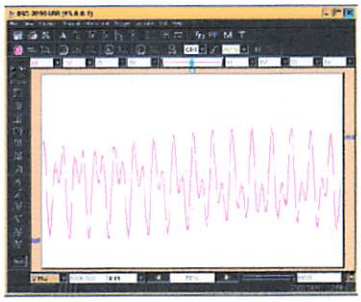
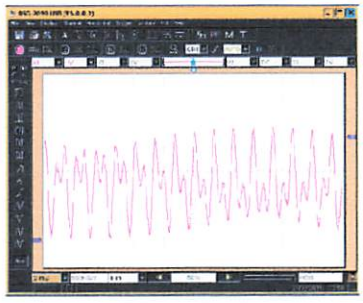
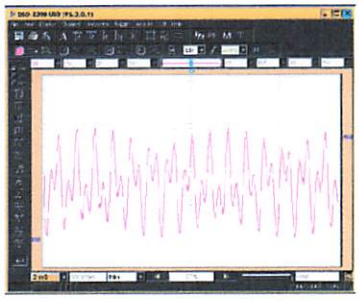
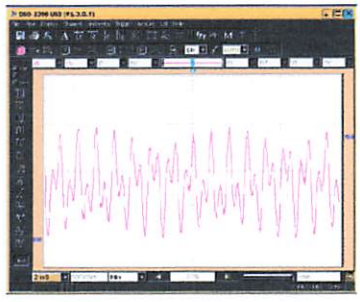
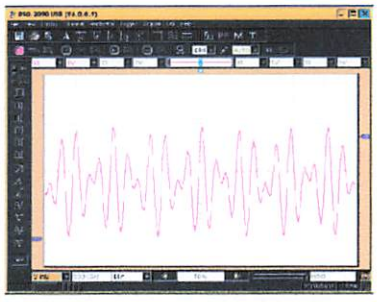
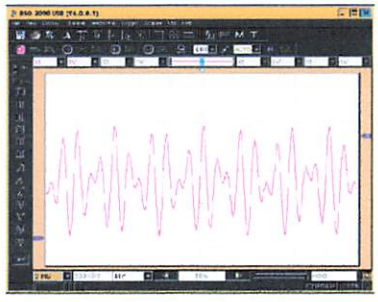
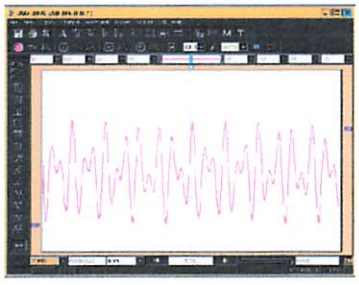
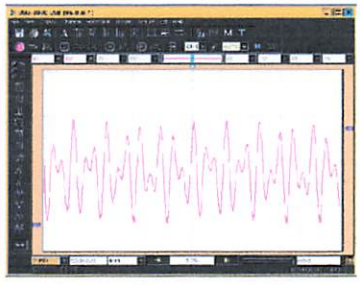
Pengujian sistem secara keseluruhan dilakukan dengan menggabungkan semua blok rangkaian dan menjalankan perangkat lunak yang telah dibuat untuk menjalankan peralatan. Pengujian ini dimaksudkan untuk mengetahui kerja sistem keseluruhan.

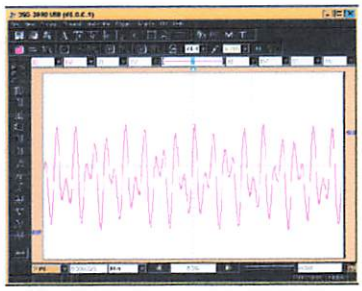
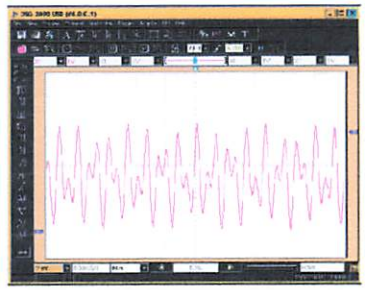
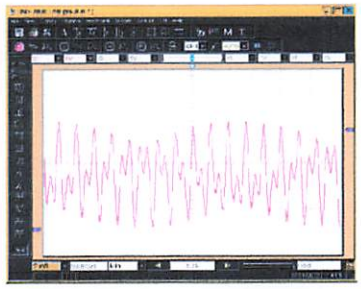
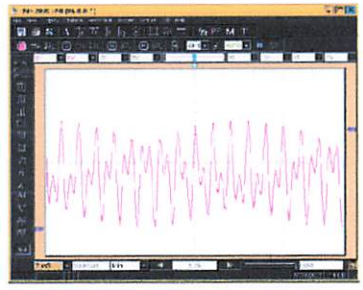
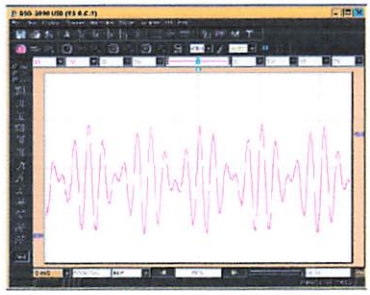
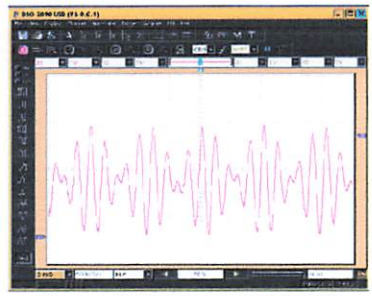
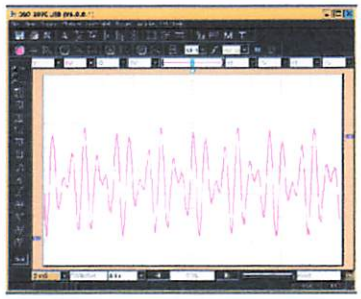
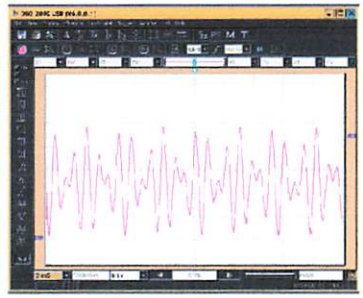
Hasil dari pengujian alat untuk rangkaian keseluruhan dapat dilihat pada tabel 4.4

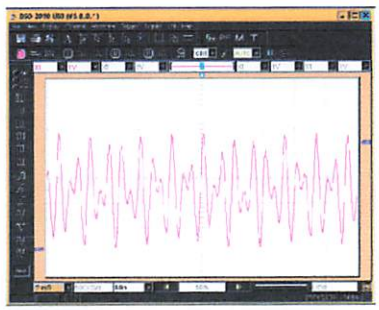
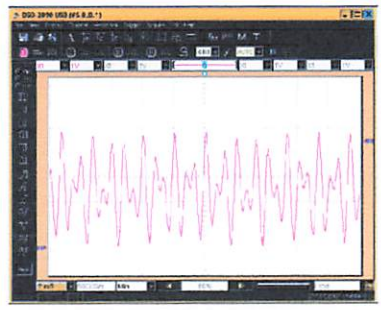
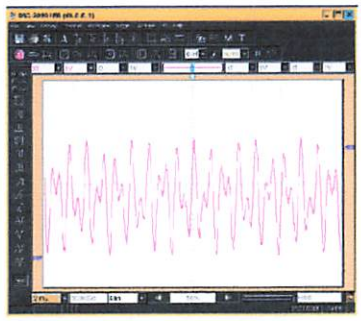
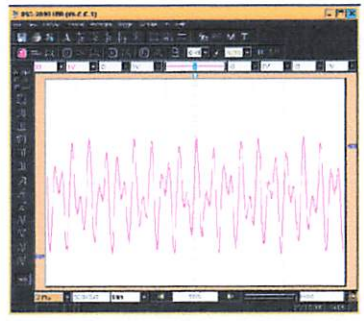
Tabel 4.4 Bentuk Gelombang DTMF di *Transmitter* dan *Reveiver*

NO	FREKWENSI	BENTUK GELOMBANG DTMF DI *TRANSMITTER*	BENTUK GELOMBANG DTMF DI *RECEIVER*
1	697 Hz & 1209 Hz		
2	697 Hz & 1366 Hz		

3	697 Hz & 1477 Hz		
4	697 Hz & 1633 Hz		
5	770 Hz & 1209 Hz		
6	770 Hz & 1366 Hz		

7	770 Hz & 1477 Hz		
8	770 Hz & 1633 Hz		
9	852 Hz & 1209 Hz		
10	852 Hz & 1366 Hz		

11	852 Hz & 1477 Hz		
12	852 Hz & 1633 Hz		
13	941 Hz & 1209 Hz		
14	941 Hz & 1366 Hz		

15	941 Hz & 1477Hz		
16	941 Hz & 1633 Hz		

Tabel 4.5 Dibawah ini menunjukan hasil pengujian frekwensi *LOW* secara keseluruhan.

Tabel 4.5 Hasil Pengujian *Frekwensi LOW* Secara Keseluruhan

TOMBOL YANG DITEKAN	TAMPILAN LCD	DATA *FREK. LOW*	HASIL PENGUKURAN *FREK. LOW*	SELISIH	*ERROR* (%)
1	01	697 Hz	697,3 Hz	0,3	0,043
2	02	697 Hz	697,3 Hz	0,3	0,043
3	03	697 Hz	697,3 Hz	0,3	0,043
4	04	770 Hz	770,4 Hz	0,4	0,051
5	05	770 Hz	770,4 Hz	0,4	0,051
6	06	770 Hz	770,4 Hz	0,4	0,051
7	07	852 Hz	853,3 Hz	1,3	0,152
8	08	852 Hz	853,3 Hz	1,3	0,152

9	09	852 Hz	853,3 Hz	1,3	0,152
0	10	941 Hz	941,7 Hz	0,7	0,074
*	11	941 Hz	941,7 Hz	0,7	0,074
#	12	941 Hz	941,7 Hz	0,7	0,074
A	13	697 Hz	697,3 Hz	0,3	0,043
B	14	770 Hz	770,4 Hz	0,4	0,051
C	15	852 Hz	853,3 Hz	1,3	0,152
D	00	941 Hz	941,7 Hz	0,7	0,074

Dari tabel diatas didapatkan *error* rata-rata sebagai berikut :

$$\textit{Error}\ \text{rata-rata} = \frac{\textit{jumlaherror}}{\textit{banyaknyapercobaan}}$$

$$= \frac{1{,}28}{16} = 0{,}08\%$$

Dari perhitungan *frekwensi low* diatas dapat disimpulkan bahwa alat mempunyai kesalahan atau *error* dalam setiap pengujian sebesar 0,08%.

Tabel 4.6 dibawah ini menunjukan hasil pengujian frekwensi *HIGH* secara keseluruhan.

Tabel 4.6 Hasil Pengujian *Frekwensi HIGH* Secara Keseluruhan

TOMBOL YANG DITEKAN	TAMPILAN LCD	DATA *FREK. HIGH*	HASIL PENGUKURAN *FREK. HIGH*	SELISIH	*ERROR* (%)
1	01	1209 KHz	1211 KHz	2	0,16
2	02	1336 KHz	1337 KHz	1	0,07
3	03	1477 KHz	1475 KHz	2	0,13
4	04	1209 KHz	1211 KHz	2	0,16
5	05	1336 KHz	1337 KHz	1	0,07
6	06	1477 KHz	1475 KHz	2	0,13
7	07	1209 KHz	1211 KHz	2	0,16
8	08	1336 KHz	1337 KHz	1	0,07
9	09	1477 KHz	1475 KHz	2	0,13
0	10	1366 KHz	1211 KHz	2	0,16
*	11	1209 KHz	1337 KHz	1	0,07
#	12	1477 KHz	1475 KHz	2	0,13
A	13	1633 KHz	1634 KHz	1	0,06
B	14	1633 KHz	1634 KHz	1	0,06
C	15	1633 KHz	1634 KHz	1	0,06
D	00	1633 KHz	1634 KHz	1	0,06

Dari tabel diatas didapatkan *error* rata-rata sebagai berikut :

$$\textit{Error}\ \text{rata-rata} = \frac{\textit{jumlaherror}}{\textit{banyaknyapercobaan}}$$

$$= \frac{1{,}68}{16} = 0{,}105\%$$

Dari perhitungan *frekwensi* high diatas dapat disimpulkan bahwa alat mempunyai kesalahan atau *error* dalam setiap pengujian sebesar 0,105%.

Untuk hasil pengujian jarak ditunjukan pada tabel 4.7 dibawah ini.

Tabel 4.7 Hasil Pengujian jarak

NO	JARAK (M)	TANPA PENGHALANG	DENGAN PENGHALANG
1	1	BISA	BISA
2	2	BISA	BISA
3	3	BISA	BISA
4	4	BISA	BISA
5	5	BISA	BISA
6	6	BISA	BISA
7	7	BISA	TIDAK BISA
8	8	BISA	TIDAK BISA
9	9	TIDAK BISA	TIDAK BISA

BAB V

PENUTUP

5.1 Kesimpulan

Dari pengamatan dan analisa selama proses perancangan dan pembuatan alat dapat diambil beberapa kesimpulan sebagai berikut :

1. Pada alat ini mampu membuat sinyal sinus dari sistem DDS dengan lebih baik karena menggunakan *Timer* LM555 yang mampu bekerja dengan kecepatan tinggi.
2. *Timer* LM555 dengan kecepatan yang disesuaikan dimasukkan ke *Counter* 8 bit untuk menjalankan data DDS yang disimpan pada EEPROM sebanyak 256 data menghasilkan sinyal sinus yang baik dengan *frekwensi* DTMF.
3. Jarak efektif tanpa penghalng adalah 8 meter dan dengan penghalang adalah 6 meter
4. Bentuk sinyal pada waktu *frekwensi Low* sama atau pada waktu *frekwensi high* sama bentuk sinyal hampir mirip misal jika ditekan tombol 1 dan 2, tombol 1 mempunyai frekwensi 697 Hz dan 1209 Hz sedangkan tombol 2 mempunyai frekwensi 697 Hz dan 1336 Hz jadi *frekwensi low*nya yang sama.
5. *Error* pada pengukuran dan perhitungan DAC sebesar 0,016%
6. *Error* pada pengujian frekuensi *LOW* sebesar 0,08% dan *Error* pada pengujian frekuensi *HIGH* sebesar 0,105%

5.2 Saran- saran

Ada beberapa hal yang perlu diperhatikan dalam pengembangan alat ini, antara lain :

1. Agar alat ini dapat bekerja dengan baik, diharapkan untuk mengikuti petunjuk pengoperasian alat dengan benar
2. Agar hasil bentuk gelombang DTMF baik diharapkan menggunakan *Counter* dan EEPROM masing-masing 2 buah yang berfungsi untuk membuat *frekwensi low* dan *frekwensi high.*

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4. Data Sheet LM74HC590, http://www.all datasheet.com
5. Data sheet AT28C16, http://www.all datasheet.com
6. Data sheet MT8870, http://www.all datasheet.com
7. Data sheet LM555, http://www.all datasheet.com
8. Data sheet CD4066, http://www.all datasheet.com
9. Data sheet Keypad, http://www.all datasheet.com
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12. http://www.Analog.com
13. http://www.Delta-electronic.com
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LAMPIRAN

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Jl. Karanglo KM.2 Malang

FORMULIR PERBAIKAN SKRIPSI

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Nim : 04.12.202
Jurusan : Teknik Elektro S-1
Konsentrasi : Teknik Elektronika
Judul Skripsi : Perancangan Dan Pembuatan Modem DTMF (*Dual Tone Multy Frekuensi*) Berbasiskan DDS (*Direct Digital Synthesis*) Yang Diaplikasikan Pada Peralatan Radio Komunikasi
Hari / Tanggal ujian skripsi : Selasa / 9 Februari 2010

Penguji	Revisi	Paraf
Penguji I	1. Tambahkan kalimat pengantar pada gambar 2. Error pada kesimpulan 3. Daftar pustaka diurut abjad	
Penguji II	1. Ukur Frekuensi pada Wireless 2. Perbaiki Flow chart untuk Box 2	

Disetujui

Penguji I

M. Ibrahim Ashari ST, MT
NIP.Y. 103. 010.0358

Penguji II

Ir. Eko Nurcahyo
NIP.Y. 102.870.0172

Mengetahui

Dosen Pembimbing I

Ir. TH. Mimien Mustikawati, MT
NIP.Y. 103 000.0352

Dosen Pembimbing II

Sotyohadi ST, Msc
NIP.P. 103.970.0309

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FORMULIR BIMBINGAN SKRIPSI

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Nim : 04.12.202
Masa Bimbingan : 29 Mei 2009 s/d 29 November 2009
Judul Skripsi : **PERANCANGAN DAN PEMBUATANMODEM DTMF (Dual Tone Multy Frekuensi) BERBASISKAN DDS (Direct Digital Synthesis) YANG DIAPLIKASIKAN PADA PERALATAN RADIO KOMUNIKASI**

NO	Tanggal	Uraian	Paraf Pembimbing
1	25-06-'09	Bab I + II revisi	
2	30-06-'09	Bab I + II ok	
3	3/12-06-09	Bab III revisi	
4	4/12 '09	Bab III ok	
5	4/12 '09	Demo alat	
6	9/12 '09	Bab IV ok, Bab V revisi	
7		Seminar hasil	
8		kompro	
9			
10			

Malang,
Dosen Pembimbing I

Ir. TH. Mimien Mustikawati, MT
NIP. 103 000 0352

Form S-4b

Institu Teknologi Nasional Malang
Fakultas Teknologi Industri
Jurusan Teknik Elektro S-1

FORMULIR BIMBINGAN SKRIPSI

Nama : EFENDI
Nim : 04.12.202
Masa Bimbingan : 29 Mei 2009 s/d 29 November 2009
Judul Skripsi : **PERANCANGAN DAN PEMBUATANMODEM DTMF (Dual Tone Multy Frekuensi) BERBASISKAN DDS (Direct Digital Synthesis) YANG DIAPLIKASIKAN PADA PERALATAN RADIO KOMUNIKASI**

NO	Tanggal	Uraian	Paraf Pembimbing
1	1-07-'09	Bab I+II Revisi	
2	04-07-09	Bab I+II Ok	
3	04-12-09	Bab III	
4	04-12-09	Demo alat	
5	09-12-09	Bab 4+5	
6			
7			
8			
9			
10			

Malang, 28-1-2010
Dosen Pembimbing II

Sotyohadi, ST. MSc
NIP.1030 970 0309

Form S-4b

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Jenjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika / T.Infokom, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : afandi
NIM : 0412202
Perbaikan meliputi :

1. tambahkan reaktansi pada gbr 1
2. sistem pd lampiran
3. daftar pustaka sesuai abjad

Malang, 9 feb '10

(M. Ibrahim Ashari, ST MT)

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

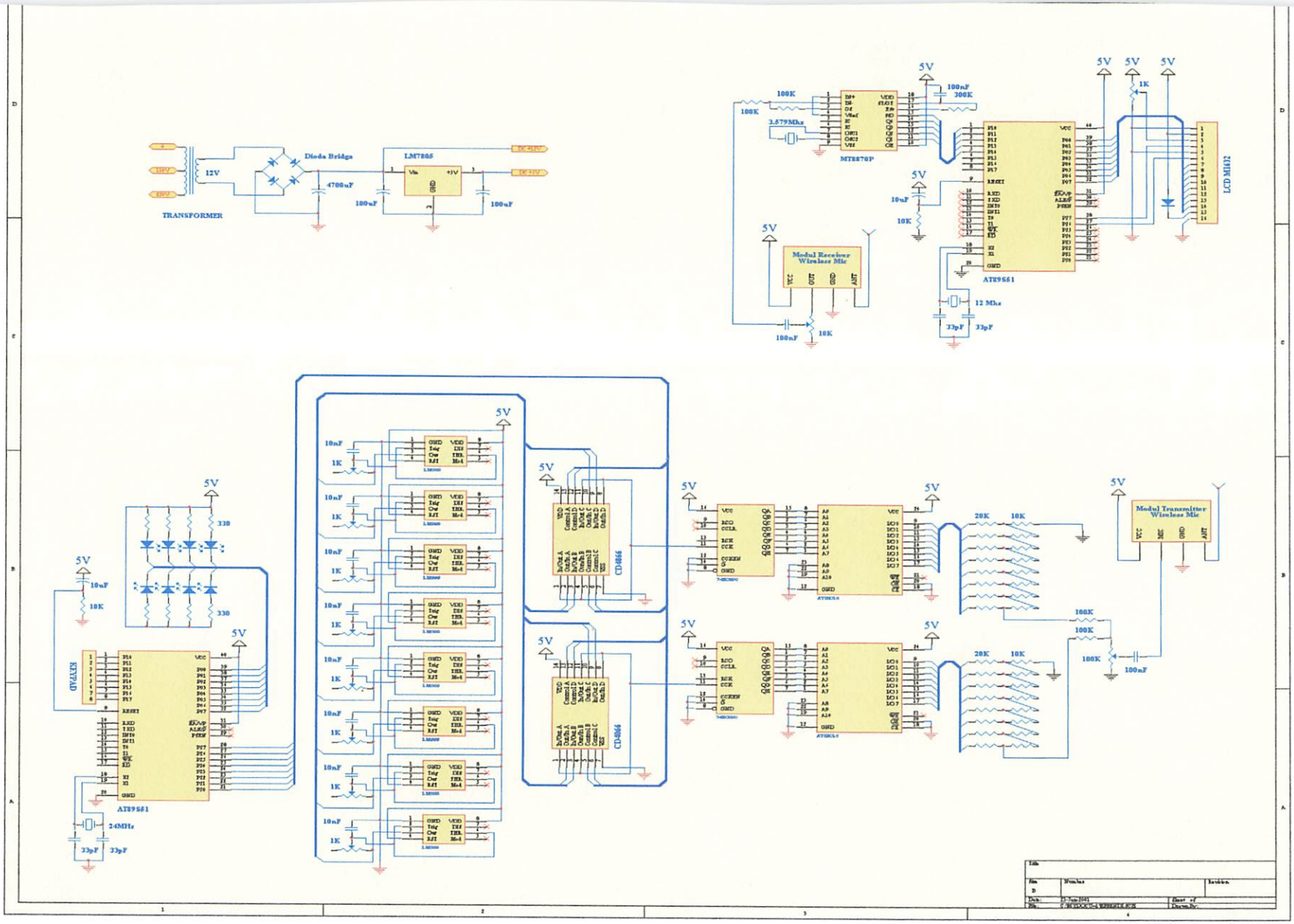
Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika / T.Infokom, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : EFENI
NIM : 04122 02
Perbaikan meliputi :

1. Ukur freq pada wireless
2. Perbaiki flowchart utk BOX 2.

Malang,

(_____)


TRANSFORMER
12V
Dioda Bridge
4700uF
LM7805
100uF
100uF
MT8870P
3.579Mhz
100K
100nF
300K
5V
1K
10uF
10K
Modul Receiver Wireless Mic
VCC
OUT
GND
ANT
100nF
10K
AT89S61
12 Mhz
33pF
33pF
LCD M1632
KEYPAD
330
330
10uF
10K
24MHz
33pF
33pF
CD4066
20K
10K
Modul Transmitter Wireless Mic
VCC
MIC
GND
ANT
100K
100nF

```
; crystal 24Mhz, memory AT28C16, counter 74HC590
; DDS 256 data, 1 cycle sine per 255 counter
;-------------------------------------------------------------------------
-----
        org     00h                     ; program reset
;
        Ldl3    Bit P0.0
        Ldl2    Bit P0.1
        Ldl1    Bit P0.2
        Ldl0    Bit P0.3
        Ldh0    Bit P0.4
        Ldh1    Bit P0.5
        Ldh2    Bit P0.6
        Ldh3    Bit P0.7

        Ckl0    Bit P2.0
        Ckl1    Bit P2.1
        Ckl2    Bit P2.2
        Ckl3    Bit P2.3
        Ckh0    Bit P2.4
        Ckh1    Bit P2.5
        Ckh2    Bit P2.6
        Ckh3    Bit P2.7

        Df0L    Equ 30h
        Df0H    Equ 31h
        Df1L    Equ 32h
        Df1H    Equ 33h

        Dly0    Equ 40h
        Dly1    Equ 41h
;
init:   acall   rsthdw
;
cek00:  acall   tg_tkn
        cjne    R0,#01,cek01
        setb    Ckl0
        setb    Ckh0
        clr     Ldl0
        clr     Ldh0
        acall   tg_lps
        acall   rsthdw
cek01:  cjne    R0,#02,cek02
        setb    Ckl0
        setb    Ckh1
        clr     Ldl0
        clr     Ldh1
        acall   tg_lps
        acall   rsthdw
cek02:  cjne    R0,#03,cek03
        setb    Ckl0
        setb    Ckh2
        clr     Ldl0
        clr     Ldh2
        acall   tg_lps
        acall   rsthdw
cek03:  cjne    R0,#04,cek04
        setb    Ckl1
        setb    Ckh0
        clr     Ldl1
        clr     Ldh0
```

```
        acall   tg_lps
        acall   rsthdw
cek04:  cjne    R0,#05,cek05
        setb    Ckl1
        setb    Ckh1
        clr     Ldl1
        clr     Ldh1
        acall   tg_lps
        acall   rsthdw
cek05:  cjne    R0,#06,cek06
        setb    Ckl1
        setb    Ckh2
        clr     Ldl1
        clr     Ldh2
        acall   tg_lps
        acall   rsthdw
cek06:  cjne    R0,#07,cek07
        setb    Ckl2
        setb    Ckh0
        clr     Ldl2
        clr     Ldh0
        acall   tg_lps
        acall   rsthdw
cek07:  cjne    R0,#08,cek08
        setb    Ckl2
        setb    Ckh1
        clr     Ldl2
        clr     Ldh1
        acall   tg_lps
        acall   rsthdw
cek08:  cjne    R0,#09,cek09
        setb    Ckl2
        setb    Ckh2
        clr     Ldl2
        clr     Ldh2
        acall   tg_lps
        acall   rsthdw
cek09:  cjne    R0,#11,cek10
        setb    Ckl3
        setb    Ckh0
        clr     Ldl3
        clr     Ldh0
        acall   tg_lps
        acall   rsthdw
cek10:  cjne    R0,#00,cek11
        setb    Ckl3
        setb    Ckh1
        clr     Ldl3
        clr     Ldh1
        acall   tg_lps
        acall   rsthdw
cek11:  cjne    R0,#12,cek12
        setb    Ckl3
        setb    Ckh2
        clr     Ldl3
        clr     Ldh2
        acall   tg_lps
        acall   rsthdw
cek12:  cjne    R0,#13,cek13
        setb    Ckl0
        setb    Ckh3
```

```
        clr     Ldl0
        clr     Ldh3
        acall   tg_lps
        acall   rsthdw
cek13:  cjne    R0,#14,cek14
        setb    Ckl1
        setb    Ckh3
        clr     Ldl1
        clr     Ldh3
        acall   tg_lps
        acall   rsthdw
cek14:  cjne    R0,#15,cek15
        setb    Ckl2
        setb    Ckh3
        clr     Ldl2
        clr     Ldh3
        acall   tg_lps
        acall   rsthdw
cek15:  cjne    R0,#16,cek16
        setb    Ckl3
        setb    Ckh3
        clr     Ldl3
        clr     Ldh3
        acall   tg_lps
        acall   rsthdw
cek16:  ljmp    cek00
;
rsthdw: setb    Ldl0
        setb    Ldl1
        setb    Ldl2
        setb    Ldl3
        setb    Ldh0
        setb    Ldh1
        setb    Ldh2
        setb    Ldh3
        clr     Ckl0
        clr     Ckl1
        clr     Ckl2
        clr     Ckl3
        clr     Ckh0
        clr     Ckh1
        clr     Ckh2
        clr     Ckh3
        ret
;
scnkpd: mov     R0,#10              ; keypad hitam
        acall   delay0
col1:   mov     P1,#11111110b
        mov     A,P1
c1b1:   cjne    A,#11101110b,c1b2
        mov     R0,#16
c1b2:   cjne    A,#11011110b,c1b3
        mov     R0,#12
c1b3:   cjne    A,#10111110b,c1b4
        mov     R0,#0
c1b4:   cjne    A,#01111110b,col2
        mov     R0,#11
;
col2:   mov     P1,#11111101b
        mov     A,P1
c2b1:   cjne    A,#11101101b,c2b2
```

```
        mov     R0,#15
c2b2:   cjne    A,#11011101b,c2b3
        mov     R0,#9
c2b3:   cjne    A,#10111101b,c2b4
        mov     R0,#8
c2b4:   cjne    A,#01111101b,col3
        mov     R0,#7
;
col3:   mov     P1,#11111011b
        mov     A,P1
c3b1:   cjne    A,#11101011b,c3b2
        mov     R0,#14
c3b2:   cjne    A,#11011011b,c3b3
        mov     R0,#6
c3b3:   cjne    A,#10111011b,c3b4
        mov     R0,#5
c3b4:   cjne    A,#01111011b,col4
        mov     R0,#4
;
col4:   mov     P1,#11110111b
        mov     A,P1
c4b1:   cjne    A,#11100111b,c4b2
        mov     R0,#13
c4b2:   cjne    A,#11010111b,c4b3
        mov     R0,#3
c4b3:   cjne    A,#10110111b,c4b4
        mov     R0,#2
c4b4:   cjne    A,#01110111b,back
        mov     R0,#1
back:   ret
;
tg_tkn: acall   scnkpd
        cjne    R0,#10,tgtkn
        sjmp    tg_tkn
tgtkn:  ret
;
tg_lps: acall   scnkpd
        cjne    R0,#10,tg_lps
        ret
;
delay0: djnz    Dly0,delay0
        ret
;
delay1: acall   delay0
        djnz    Dly1,delay1
        ret
;
        end
```

```
        org     00h
;
        DTRq    Bit P1.4
        Rest    Bit P2.6
        Enbl    Bit P2.7
        Char    Equ 30h
        Dly0    Equ 31h
        Dly1    Equ 32h
        Dly2    Equ 33h
;
init:   acall   lcd_in
;
mulai:  mov     DPTR,#nama
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#nim
        acall   line2
        mov     Char,#16
        acall   tulis
        acall   delay2
        mov     DPTR,#jur
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#univ
        acall   line2
        mov     Char,#16
        acall   tulis
        acall   delay2
;
        acall   lcdclr
        mov     DPTR,#judul
        acall   line1
        mov     Char,#16
        acall   tulis
        mov     DPTR,#angka
measr0: acall   delay0
        jnb     DTRq,measr0
        mov     P0,#0C7h
        acall   w_ins
        mov     A,P1
        anl     A,#15
        mov     B,#10
        div     AB
        acall   wr_chr
        mov     A,B
        acall   wr_chr
        mov     P0,#0D0h
        acall   w_ins
measr1: acall   delay0
        jb      DTRq,measr1
        sjmp    measr0
;
line1:  mov     P0,#080h
        acall   w_ins
        ret
;
line2:  mov     P0,#0C0h
        acall   w_ins
        ret
```

```
;
tulis:  clr     A
        acall   wr_chr
        inc     DPTR
        djnz    Char,tulis
        ret
;
wr_chr: movc    A,@A+DPTR
        mov     P0,A
        acall   w_chr
        ret
;
w_ins:  clr     Enbl
        clr     Rest
        setb    Enbl
        clr     Enbl
        acall   delay0
        ret
;
w_chr:  clr     Enbl
        setb    Rest
        setb    Enbl
        clr     Enbl
        acall   delay0
        ret
;
lcd_in: acall   delay1
        mov     P0,#01h             ; Display Clear
        acall   w_ins
        mov     P0,#38h             ; Function Set
        acall   w_ins
        mov     P0,#0Dh             ; Display On, Cursor, Blink
        acall   w_ins
        mov     P0,#06h             ; Entry Mode
        acall   w_ins
        mov     P0,#02h             ; Cursor Home
        acall   w_ins
        ret
;
lcdclr: mov     P0,#01h             ; Display Clear
        acall   w_ins
        acall   delay0
        acall   delay0
        ret
;
delay0: djnz    Dly0,delay0
        ret
;
delay1: acall   delay0
        djnz    Dly1,delay1
        ret
;
delay2: mov     Dly2,#20
dely2:  acall   delay1
        djnz    Dly2,dely2
        ret
;
nama:   DB      '     Efendi     '
nim:    DB      '  NIM: 0412202  '
jur:    DB      '   T. Elektro   '
univ:   DB      '   ITN Malang   '
```

```
judul:  DB      '   Data  DTMF    '
angka:  DB      '0123456789       '
;
        end
```

atures

- ɔmpatible with MCS-51® Products
- (Bytes of In-System Programmable (ISP) Flash Memory
  - – Endurance: 1000 Write/Erase Cycles
- 0V to 5.5V Operating Range
- ılly Static Operation: 0 Hz to 33 MHz
- ıree-level Program Memory Lock
- !8 x 8-bit Internal RAM
- ! Programmable I/O Lines
- vo 16-bit Timer/Counters
- x Interrupt Sources
- ıll Duplex UART Serial Channel
- ɔw-power Idle and Power-down Modes
- terrupt Recovery from Power-down Mode
- atchdog Timer
- ıal Data Pointer
- ɔwer-off Flag
- ıst Programming Time
- exible ISP Programming (Byte and Page Mode)

scription

AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K ıs of in-system programmable Flash memory. The device is manufactured using el's high-density nonvolatile memory technology and is compatible with the indus- ıtandard 80C51 instruction set and pinout. The on-chip Flash allows the program nory to be reprogrammed in-system or by a conventional nonvolatile memory pro- nmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a ıolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a ly-flexible and cost-effective solution to many embedded control applications.

AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of M, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five- or two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and k circuitry. In addition, the AT89S51 is designed with static logic for operation n to zero frequency and supports two software selectable power saving modes. Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and rupt system to continue functioning. The Power-down mode saves the RAM con- ɜ but freezes the oscillator, disabling all other chip functions until the next external rupt or hardware reset.

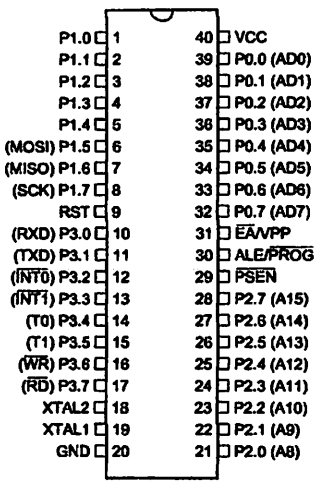
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

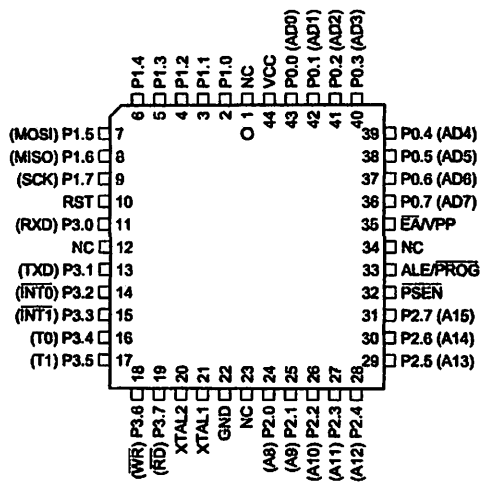
Rev. 2487A–10/01

n Configurations

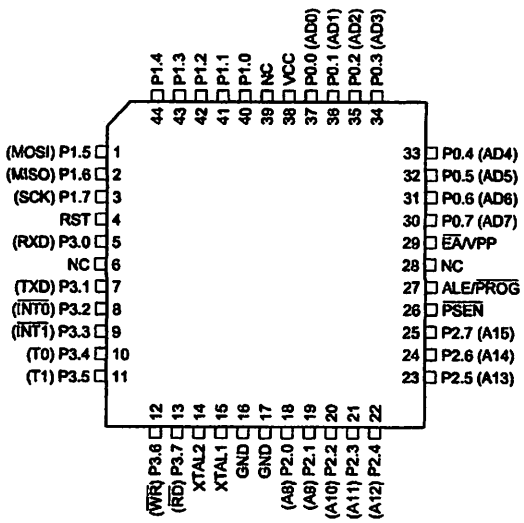
PDIP



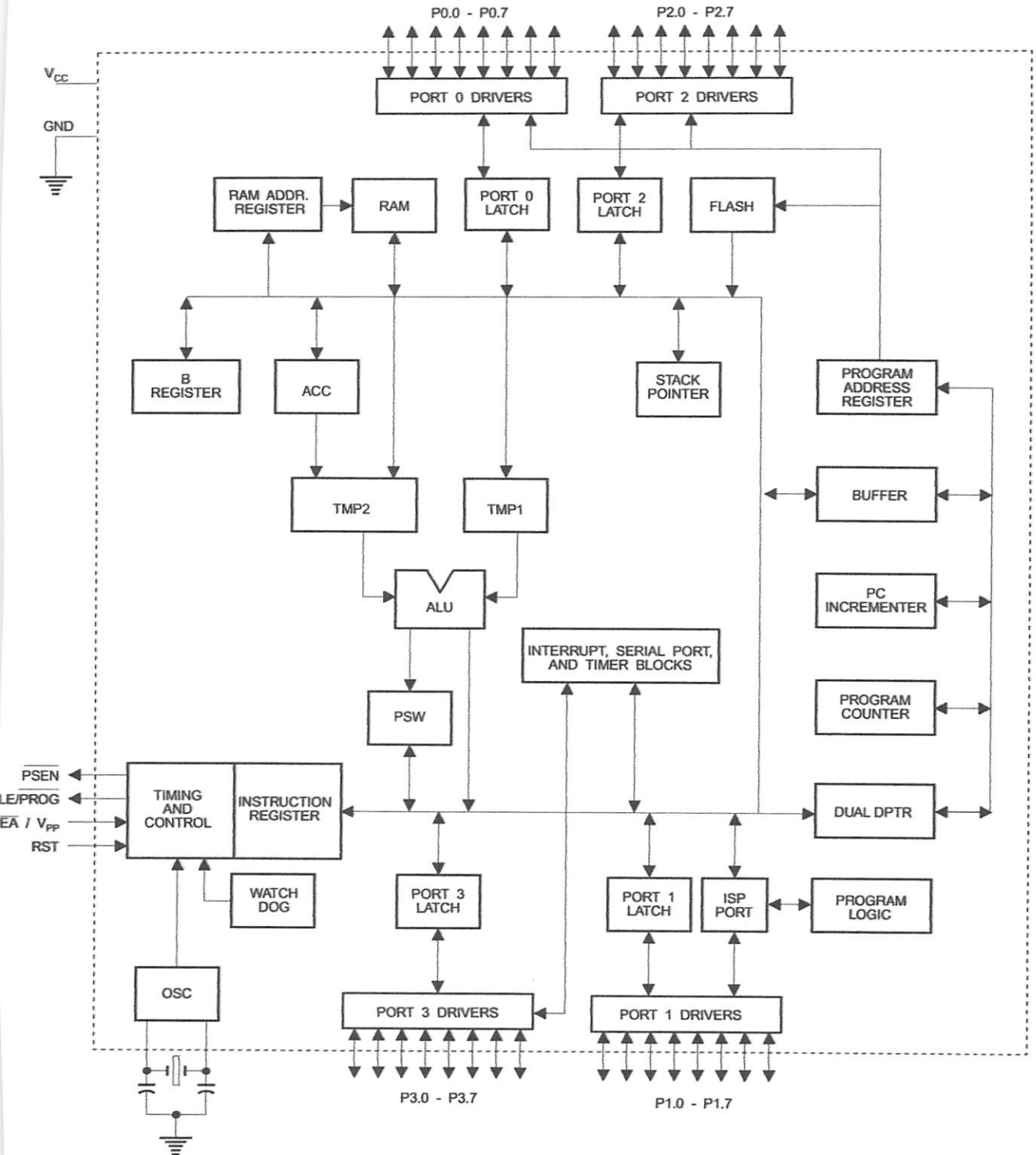
PLCC



TQFP



ock Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
ALE/PROG
EA / V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
ISP PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7

1 Description

C Supply voltage.

ID Ground.

rt 0 Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

rt 1 Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

rt 2 Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

rt 3 Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

T

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

E/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{EN}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

AL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

AL2

Output from the inverting oscillator amplifier

ecial nction egisters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

ble 1. AT89S51 SFR Map and Reset Values

0F8H								0FFH
0F0H	B 00000000							0F7H
0E8H								0EFH
0E0H	ACC 00000000							0E7H
0D8H								0DFH
0D0H	PSW 00000000							0D7H
0C8H								0CFH
0C0H								0C7H
0B8H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A8H	IE 0X000000							0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

emory ganization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

ogram Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

ta Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

atchdog mer ne-time abled with set-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

ing the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

DT During ›wer-down ıd Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

ıRT

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

mer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

terrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

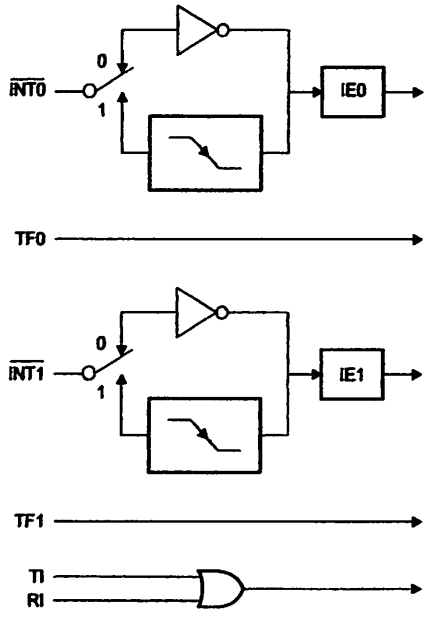
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

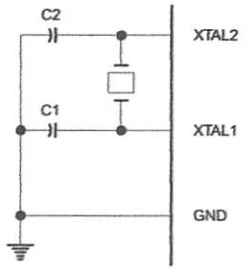
Figure 1. Interrupt Sources



cillator aracteristics

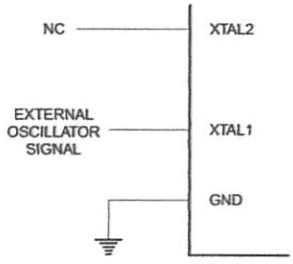
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



le Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

wer-down ode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{INT0}$ or $\overline{INT1}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

·ogram emory Lock its

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

·ogramming e Flash – arallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

ogramming e Flash – rial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

rial ogramming gorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

·rial ·ogramming ·struction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

·ogramming ·terface – ·rallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

·le 7. Flash Programming Modes

·ode	V_{CC}	RST	PSEN	ALE/ PROG	EA/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
·rite Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
·ad Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
·rite Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
·rite Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
·rite Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
·ead Lock Bits 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
·hip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
·ead Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
·ead Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
·ead Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

·es:
1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/BSY signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

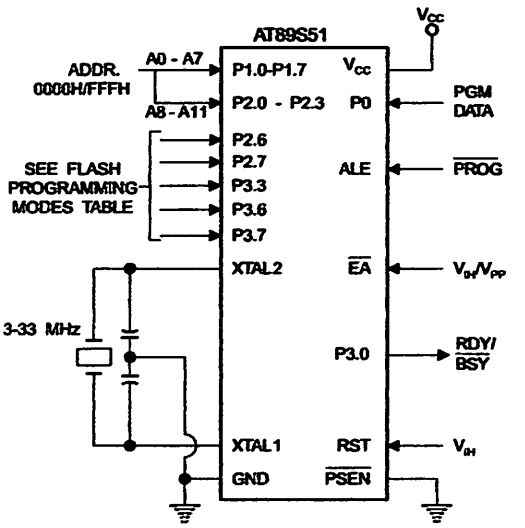
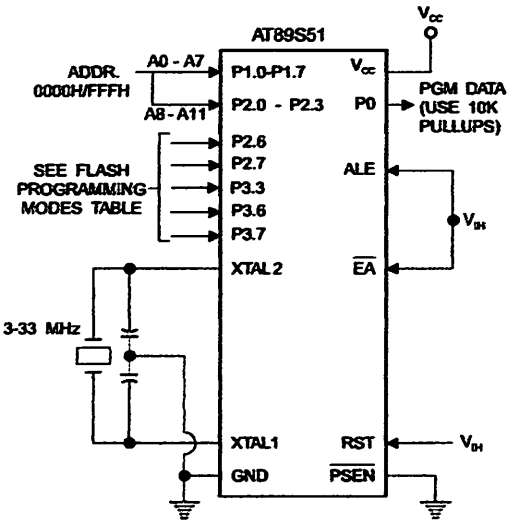


Figure 5. Verifying the Flash Memory (Parallel Mode)

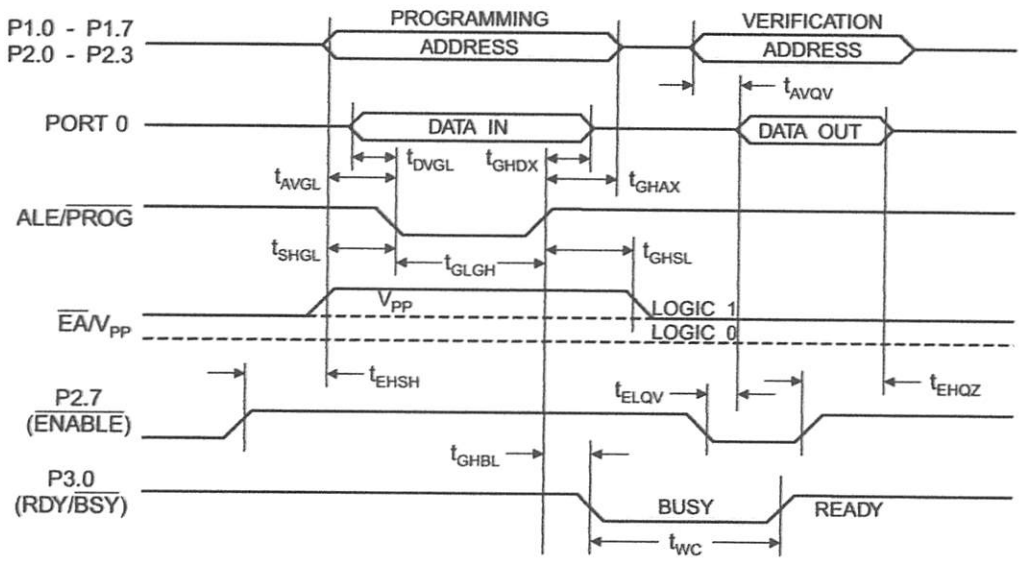


ash Programming and Verification Characteristics (Parallel Mode)

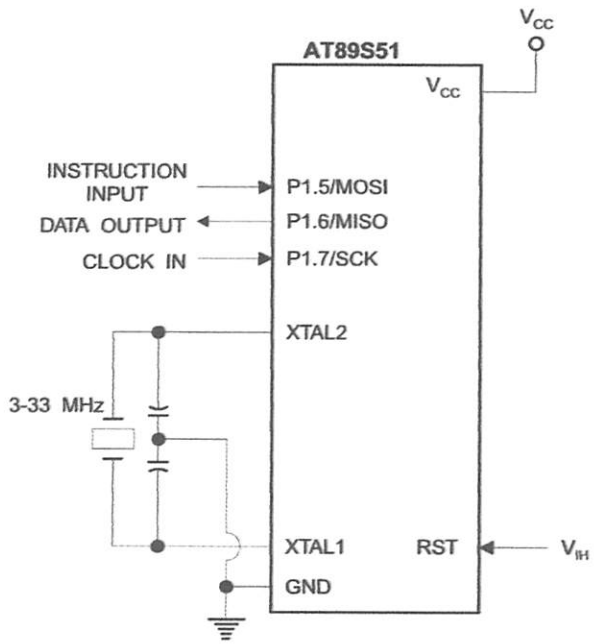
= 20°C to 30°C, V_{CC} = 4.5 to 5.5V

mbol	Parameter	Min	Max	Units
PP	Programming Supply Voltage	11.5	12.5	V
P	Programming Supply Current		10	mA
C	V_{CC} Supply Current		30	mA
$^1/_{tCLCL}$	Oscillator Frequency	3	33	MHz
AVGL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHAX	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
DVGL	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHDX	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
EHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
SHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
GHSL	V_{PP} Hold After $\overline{PROG}$	10		µs
GLGH	$\overline{PROG}$ Width	0.2	1	µs
AVQV	Address to Data Valid		$48t_{CLCL}$	
ELQV	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
EHQZ	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
GHBL	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
WC	Byte Write Cycle Time		50	µs

jure 6. Flash Programming and Verification Waveforms – Parallel Mode

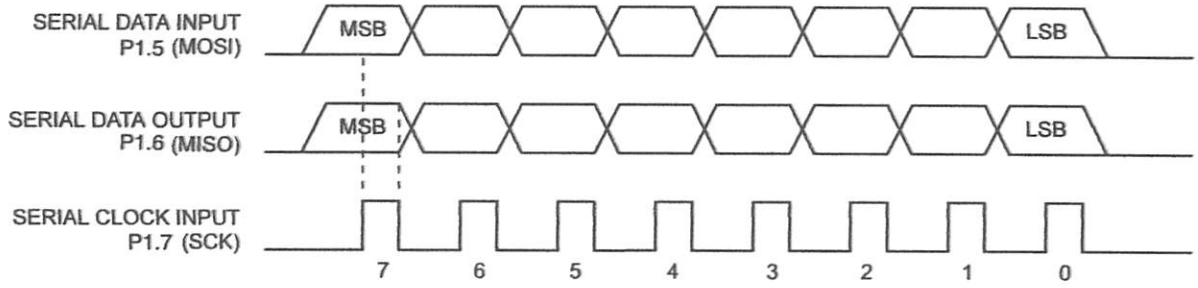


ure 7. Flash Memory Serial Downloading



ash Programming and Verification Waveforms – Serial Mode

ure 8. Serial Programming Waveforms



le 8. Serial Programming Instruction Set

struction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
·ogramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
hip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
ead Program Memory Byte Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
/rite Program Memory Byte Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
/rite Lock Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
ead Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
ead Signature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
ead Program Memory 'age Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
rite Program Memory 'age Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

es: 1. The signature bytes are not readable in Lock Bit Modes 3 and 4.

2. B1 = 0, B2 = 0 →Mode 1, no lock protection
   B1 = 0, B2 = 1 →Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 →Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 →Mode 4, lock bit 3 activated

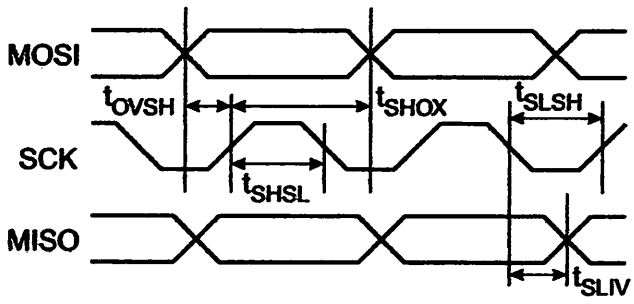
   } Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

erial Programming Characteristics

igure 9. Serial Programming Timing



able 9. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	8 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	8 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

›solute Maximum Ratings*

›erating Temperature	-55°C to +125°C
›orage Temperature	-65°C to +150°C
›ltage on Any Pin th Respect to Ground	-1.0V to +7.0V
aximum Operating Voltage	6.6V
C Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C Characteristics

e values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

ymbol	Parameter	Condition	Min	Max	Units
IL	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
IL1	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
IH	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
IH1	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
OL	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
OL1	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
OH	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
OH1	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
L	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-650	µA
I	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RST	Reset Pulldown Resistor		50	300	KΩ
IO	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
C	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

es: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

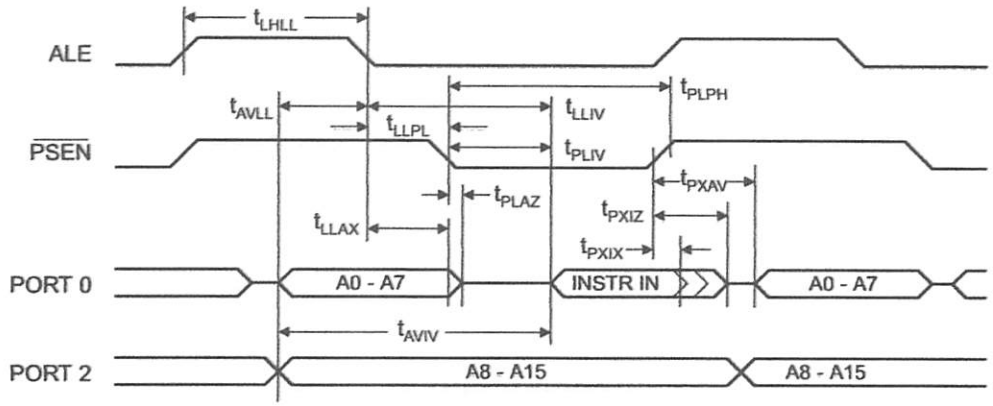
: Characteristics

ler operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other puts = 80 pF.

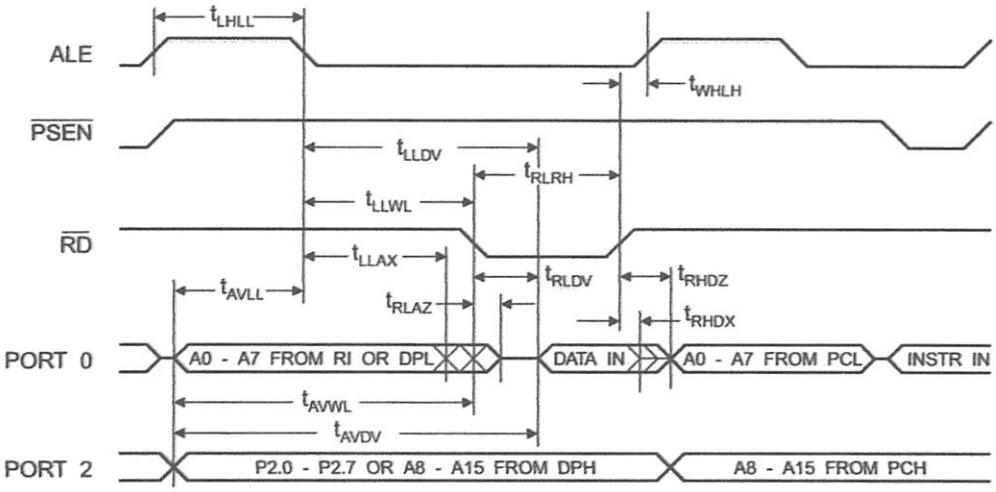
xternal Program and Data Memory Characteristics

ymbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{CLCL}	Oscillator Frequency			0	33	MHz
HLL	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
VLL	Address Valid to ALE Low	43		t_{CLCL}-25		ns
LAX	Address Hold After ALE Low	48		t_{CLCL}-25		ns
LIV	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
LPL	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
LPH	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
LIV	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
XIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
XIZ	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
XAV	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
VIV	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
LAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
LRH	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
TLWH	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
LDV	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
HDX	Data Hold After $\overline{RD}$	0		0		ns
HDZ	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
LDV	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
VDV	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
LWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
VWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
WX	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
VWH	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
THQX	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
LAZ	$\overline{RD}$ Low to Address Float		0		0	ns
HLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

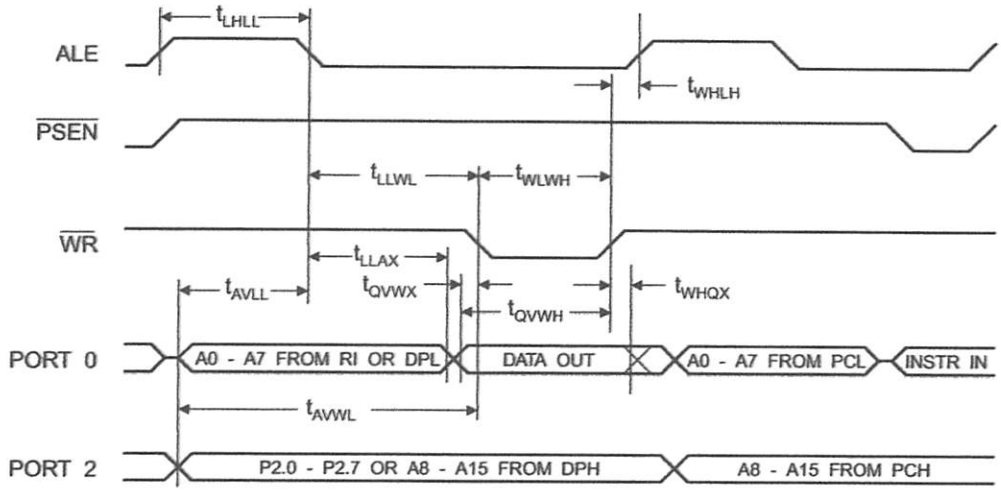
ternal Program Memory Read Cycle



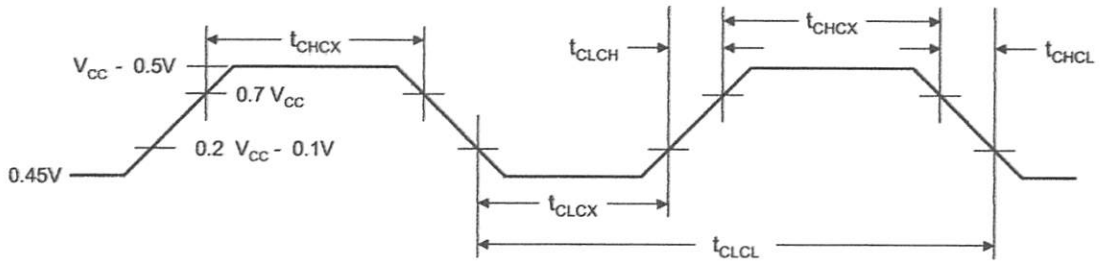
xternal Data Memory Read Cycle



ternal Data Memory Write Cycle



ternal Clock Drive Waveforms



ternal Clock Drive

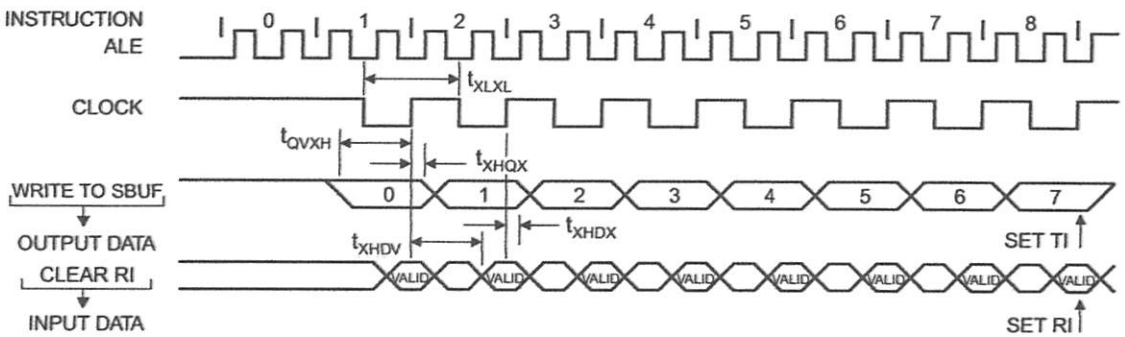
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	33	MHz
t_{CLCL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

rial Port Timing: Shift Register Mode Test Conditions

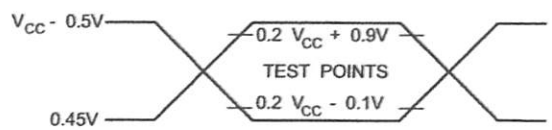
values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

ymbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
LXL	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
VXH	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
HQX	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
XDX	Input Data Hold After Clock Rising Edge	0		0		ns
XDV	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

hift Register Mode Timing Waveforms

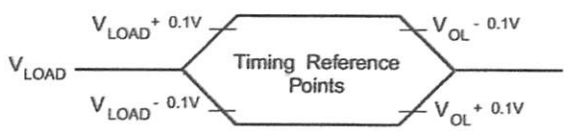


C Testing Input/Output Waveforms[1]



te: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

oat Waveforms[1]



e: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

dering Information

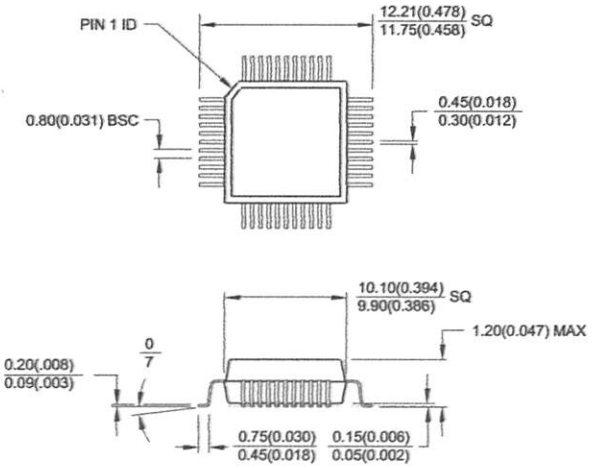
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC	44A 44J 40P6	Commercial (0° C to 70° C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI	44A 44J 40P6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC	44A 44J 40P6	Commercial (0° C to 70° C)

= Preliminary Availability

	Package Type
A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

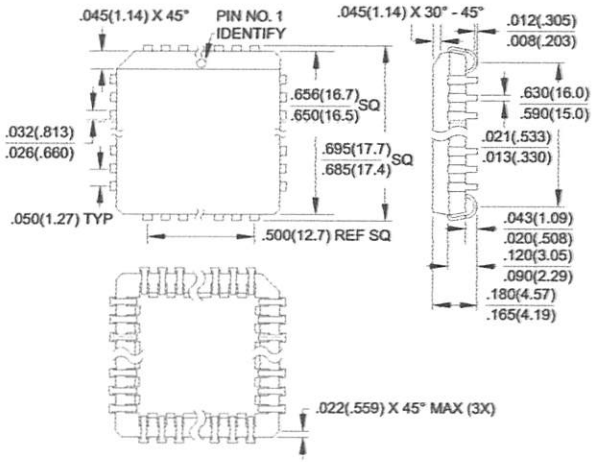
ckaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*

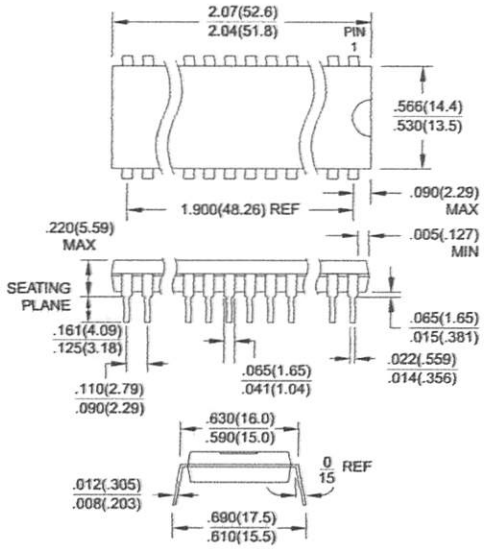


*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



40P6, 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC



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2487A–10/01/xM

atures

- ast Read Access Time - 150 ns
- ast Byte Write - 200 µs or 1 ms
- elf-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
-)irect Microprocessor Control
  - $\overline{\text{DATA}}$ POLLING
- .ow Power
  - 30 mA Active Current
  - 100 µA CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- 5V ± 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Pinout
- Commercial and Industrial Temperature Ranges

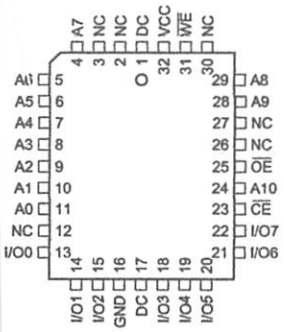
escription

e AT28C16 is a low-power, high-performance Electrically Erasable and Program-ble Read Only Memory with easy to use features. The AT28C16 is a 16K memory anized as 2,048 words by 8 bits. The device is manufactured with Atmel's reliable nvolatile CMOS technology. *(continued)*

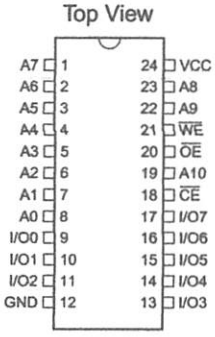
n Configurations

n Name	Function
0 - A10	Addresses
E	Chip Enable
E	Output Enable
E	Write Enable
O0 - I/O7	Data Inputs/Outputs
C	No Connect
C	Don't Connect

PLCC
Top View



PDIP, SOIC
Top View



e: PLCC package pins 1 and 17
DON'T CONNECT.

16K (2K x 8) Parallel EEPROMs

AT28C16

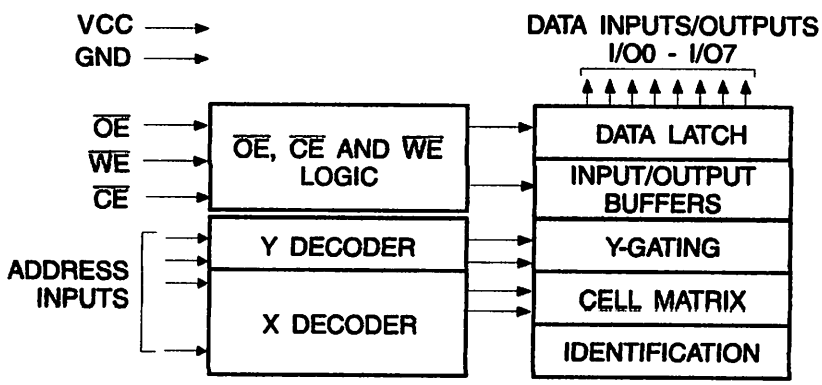
Rev. 0540B–10/98

· AT28C16 is accessed like a static RAM for the read or e cycles without the need of external components. Dur- a byte write, the address and data are latched inter- y, freeing the microprocessor address and data bus for er operations. Following the initiation of a write cycle, device will go to a busy state and automatically clear d write the latched data using an internal control timer. e end of a write cycle can be determined by $\overline{DATA}$ LLING of I/O_7. Once the end of a write cycle has been tected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA.

Atmel's 28C16 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of EEPROM are available for device identification or tracking.

lock Diagram



bsolute Maximum Ratings*

mperature Under Bias	-55°C to +125°C
rage Temperature	-65°C to +150°C
Input Voltages (including NC Pins) h Respect to Ground	-0.6V to +6.25V
Output Voltages h Respect to Ground	-0.6V to V_{CC} + 0.6V
ltage on $\overline{OE}$ and A9 ith Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

ıvice Operation

AD: The AT28C16 is accessed like a Static RAM. en $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored he memory location determined by the address pins is ıerted on the outputs. The outputs are put in a high ıedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line ıtrol gives designers increased flexibility in preventing s contention.

TE WRITE: Writing data into the AT28C16 is similar to iting into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ ıut with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) ini- tes a byte write. The address location is latched on the ıt falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on ı first rising edge. Internally, the device performs a self- ıar before write. Once a byte write has been started, it l automatically time itself to completion. Once a pro- ımming operation has been initiated and for the duration t_{WC}, a read operation will effectively be a polling opera- ı.

ST BYTE WRITE: The AT28C16E offers a byte write ıe of 200 µs maximum. This feature allows the entire /ice to be rewritten in 0.4 seconds.

TA POLLING: The AT28C16 provides $\overline{DATA}$ POLLING ıignal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power on delay—once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write; and (c) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C16 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

C and AC Operating Range

		AT28C16-15
perating mperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%

perating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$

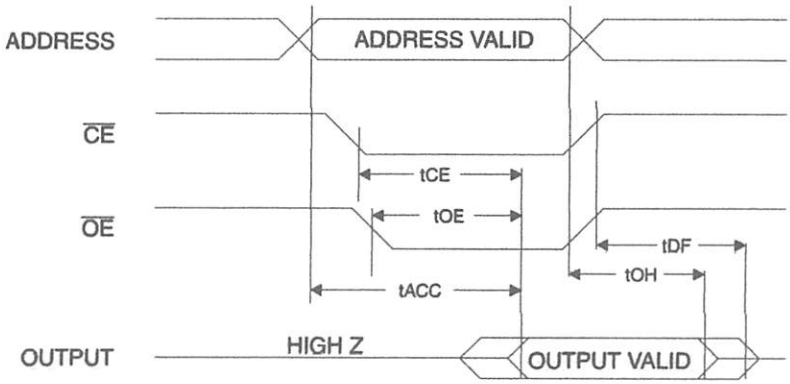
C Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0V$ to $V_{CC} + 1V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0V$ to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to $V_{CC} + 1.0V$			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to $V_{CC} + 1.0V$	Com.		2	mA
			Ind.		3	mA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; $I_{OUT} = 0$ mA $\overline{CE} = V_{IL}$	Com.		30	mA
			Ind.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA		2.4		V

; Read Characteristics

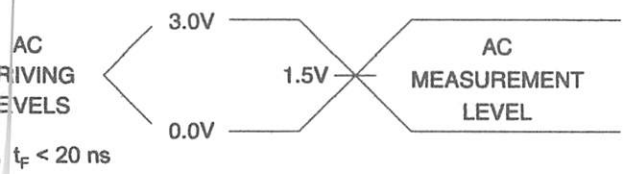
ymbol	Parameter	AT28C16-15		Units
		Min	Max	
CC	Address to Output Delay		150	ns
E(1)	$\overline{CE}$ to Output Delay		150	ns
E(2)	$\overline{OE}$ to Output Delay	10	70	ns
F(3)(4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	ns
H	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

C Read Waveforms(1)(2)(3)(4)

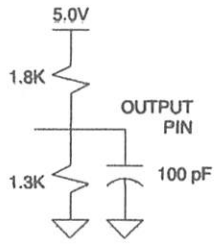


es: 1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

put Test Waveforms and easurement Level



Output Test Load



n Capacitance

1 MHz, T = 25°C(1)

mbol	Typ	Max	Units	Conditions
N	4	6	pF	V_{IN} = 0V
UT	8	12	pF	V_{OUT} = 0V

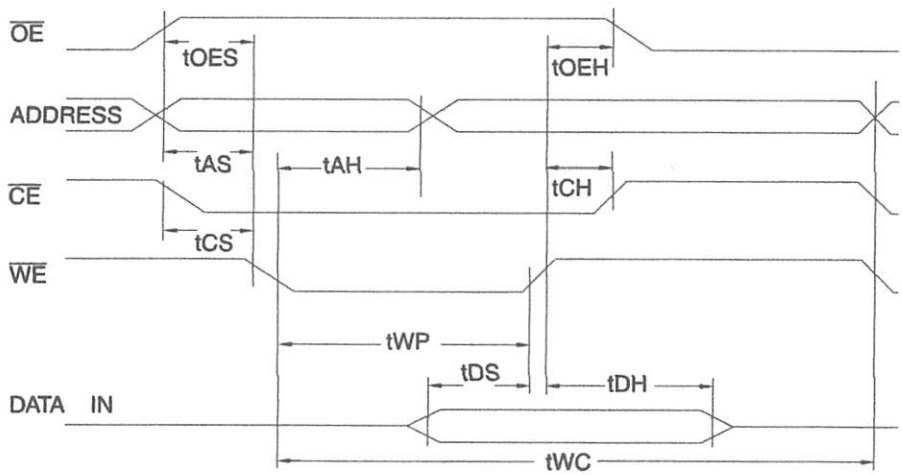
e: 1. This parameter is characterized and is not 100% tested.

: Write Characteristics

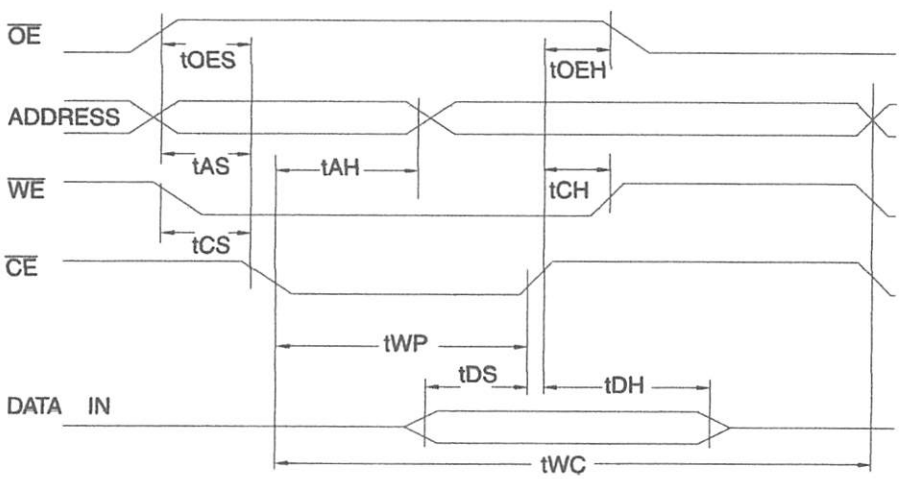
mbol	Parameter		Min	Typ	Max	Units
, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
H	Address Hold Time		50			ns
P	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
S	Data Set-up Time		50			ns
H, t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
S, t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time		0			ns
C	Write Cycle Time	AT28C16		0.5	1.0	ms
		AT28C16E		100	200	µs

C Write Waveforms

E Controlled



E Controlled

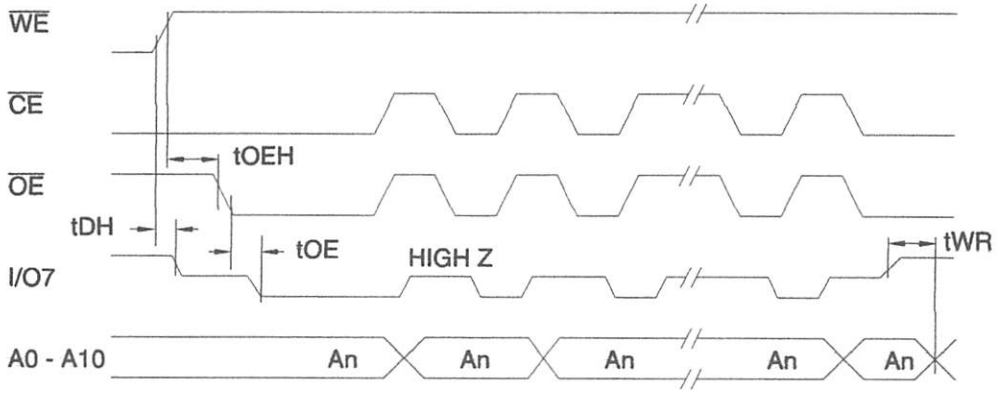


ata Polling Characteristics[1]

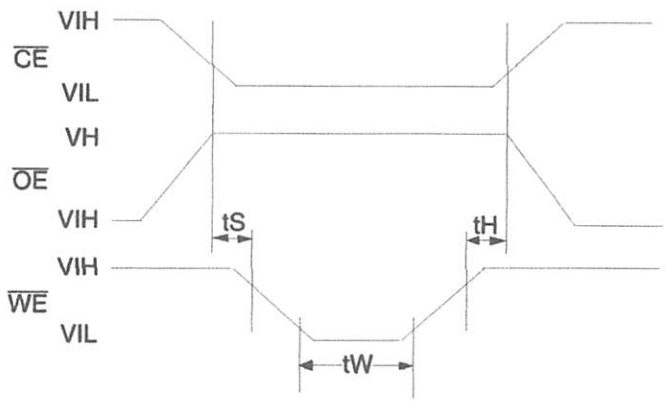
mbol	Parameter	Min	Typ	Max	Units
H	Data Hold Time	10			ns
EH	$\overline{OE}$ Hold Time	10			ns
E	$\overline{OE}$ to Output Delay[2]				ns
VR	Write Recovery Time	0			ns

tes: 1. These parameters are characterized and not 100% tested.
2. See AC Characteristics.

ata Polling Waveforms

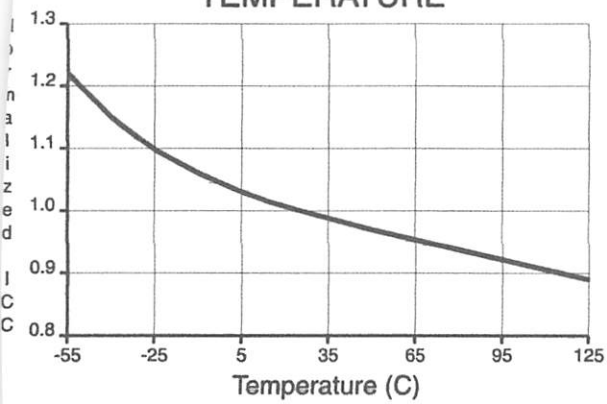


hip Erase Waveforms

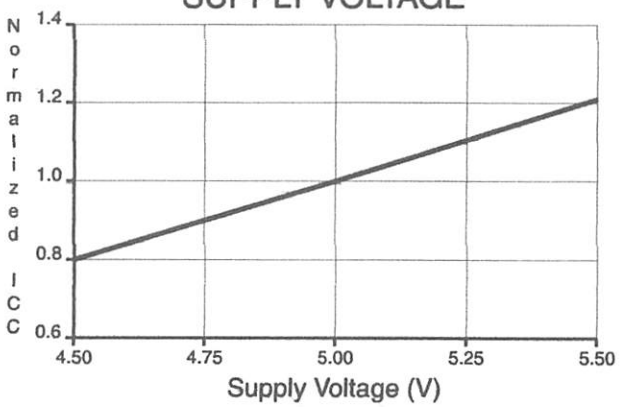


t_H = 1 µsec (min.)
= 10 msec (min.)
= 12.0V ± 0.5V

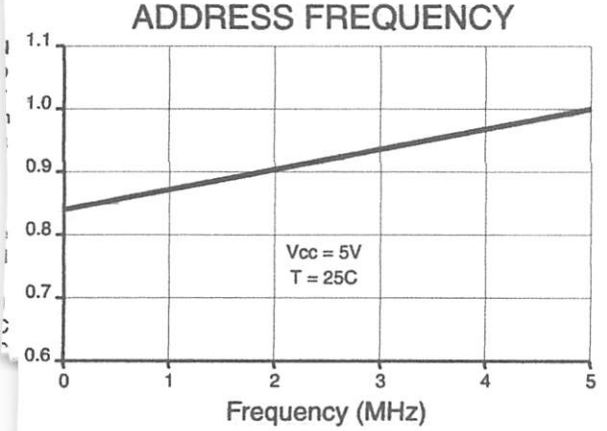
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



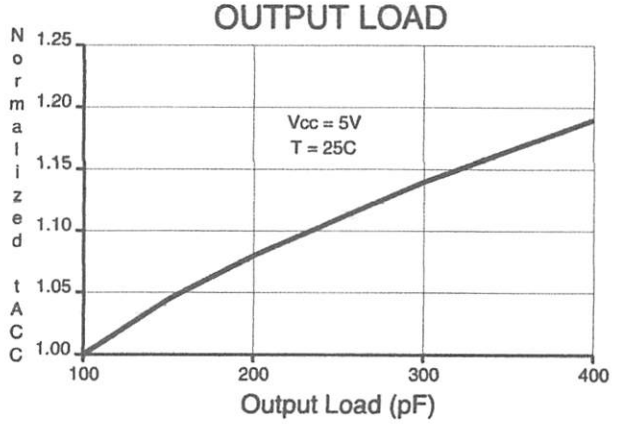
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



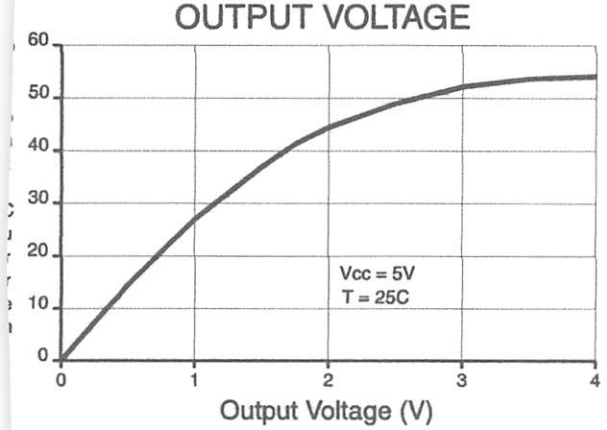
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



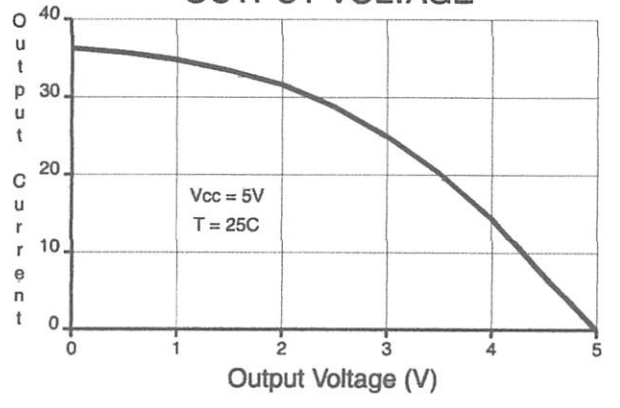
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



dering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C16(E)-15JC AT28C16(E)-15PC AT28C16(E)-15SC	32J 24P6 24S	Commercial (0°C to 70°C)
	45	0.1	AT28C16(E)-15JI AT28C16(E)-15PI AT28C16(E)-15SI	32J 24P6 24S	Industrial (-40°C to 85°C)

tes: 1. See Valid Part Numbers table below.

2. The 28C16 200 ns and 250 ns speed selections have been removed from valid selections table and are replaced by the faster 150 ns T_{AA} offering.
3. The 28C16 ceramic package offerings have been removed. New designs should utilize the 28C256 ceramic offerings.

alid Part Numbers

e following table lists standard Atmel products that can be ordered.

evice Numbers	Speed	Package and Temperature Combinations
T28C16	15	JC, JI, PC, PI, SC, SI
T28C16E	15	JC, JI, PC, PI, SC, SI
T28C16	-	W

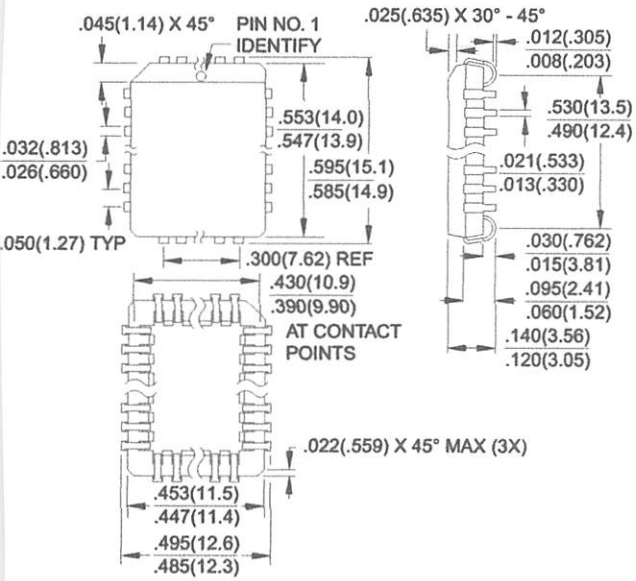
e Products

eference Section: Parallel EEPROM Die Products

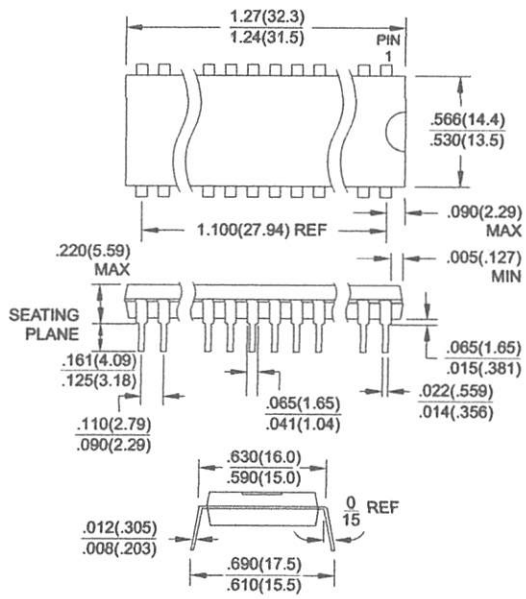
Package Type	
J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
	Die
Options	
ank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs

ckaging Information

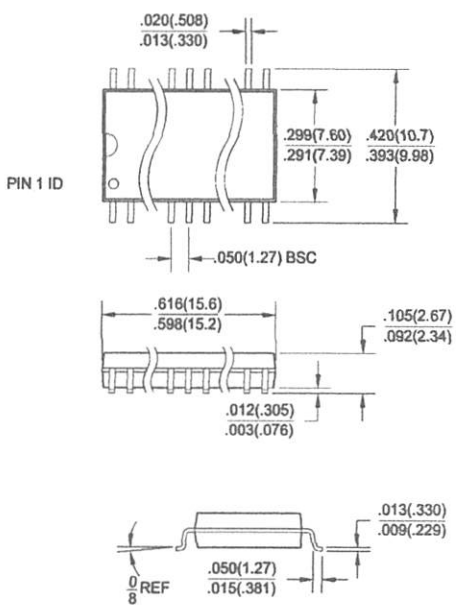
32J, 32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AA



24P6, 24-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AA



24S, 24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



ISO²-CMOS MT8870D/MT8870D-1
Integrated DTMF Receiver

ISSUE 5 March 1997

Features
- Complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Backward compatible with MT8870C/MT8870C-1

Applications
- Receiver system for British Telecom (BT) or CEPT Spec (MT8870D-1)
- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote control
- Personal computers
- Telephone answering machine

Ordering Information

MT8870DE/DE-1	18 Pin Plastic DIP
MT8870DS/DS-1	18 Pin SOIC
MT8870DN/DN-1	20 Pin SSOP

-40 °C to +85 °C

Description

The MT8870D/MT8870D-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

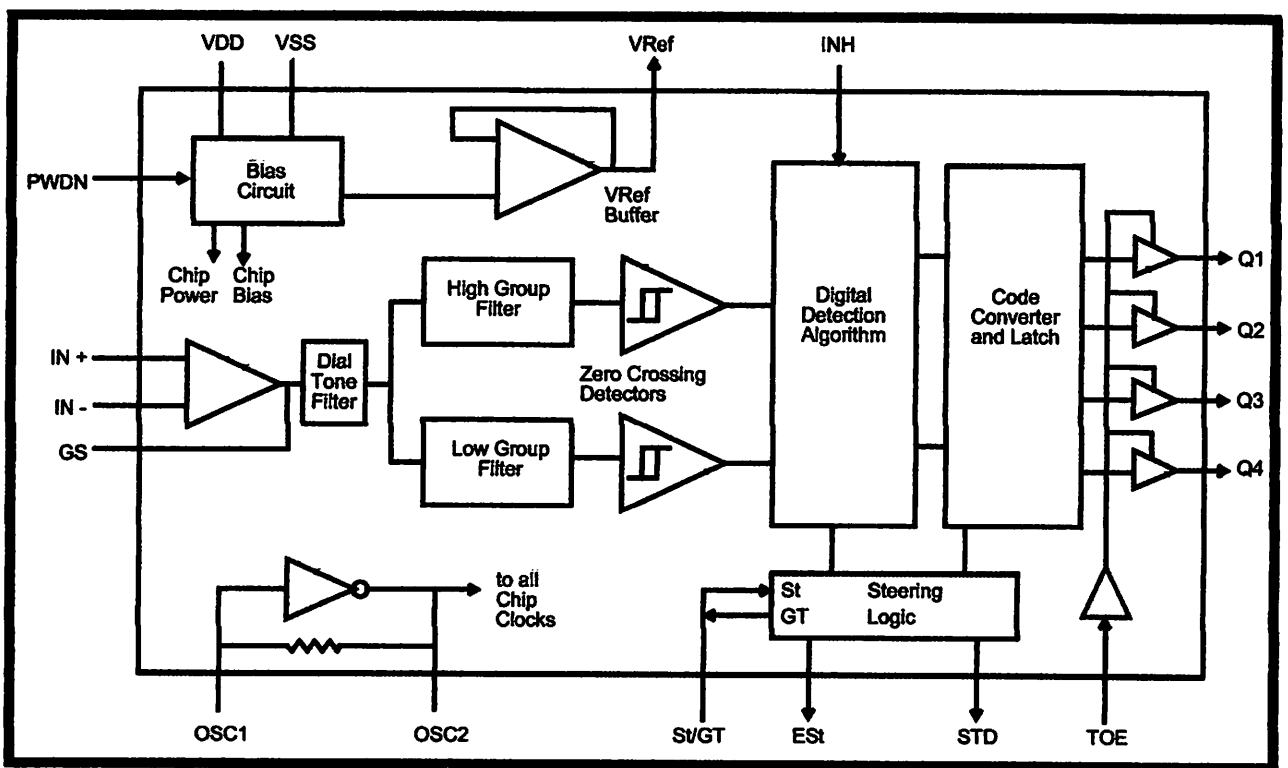


Figure 1 - Functional Block Diagram

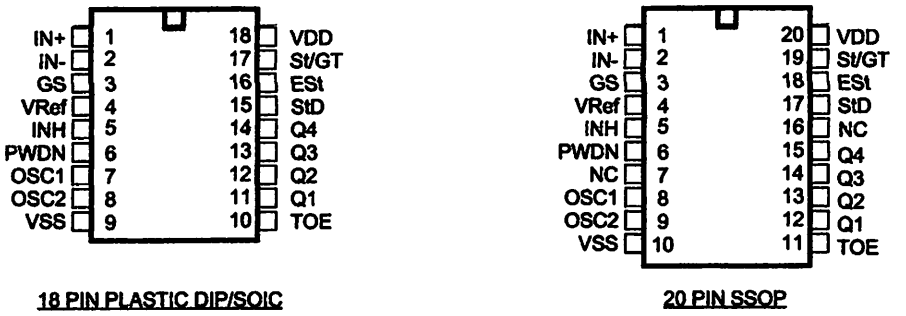


Figure 2 - Pin Connections

Description

Pin # 20	Name	Description
1	IN+	**Non-Inverting Op-Amp (Input).**
2	IN-	**Inverting Op-Amp (Input).**
3	GS	**Gain Select.** Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V_{Ref}	**Reference Voltage (Output).** Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig. 6 and Fig. 10).
5	INH	**Inhibit (Input).** Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
6	PWDN	**Power Down (Input).** Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down.
8	OSC1	**Clock (Input).**
9	OSC2	**Clock (Output).** A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
10	V_{SS}	**Ground (Input).** 0V typical.
11	TOE	**Three State Output Enable (Input).** Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
12-15	Q1-Q4	**Three State Data (Output).** When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
17	StD	**Delayed Steering (Output).**Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}.
18	ESt	**Early Steering (Output).** Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
19	St/GT	**Steering Input/Guard time (Output) Bidirectional.** A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
20	V_{DD}	**Positive power supply (Input).** +5V typical.
7, 16	NC	No Connection.

Functional Description

The MT8870D/MT8870D-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Figure 3). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while

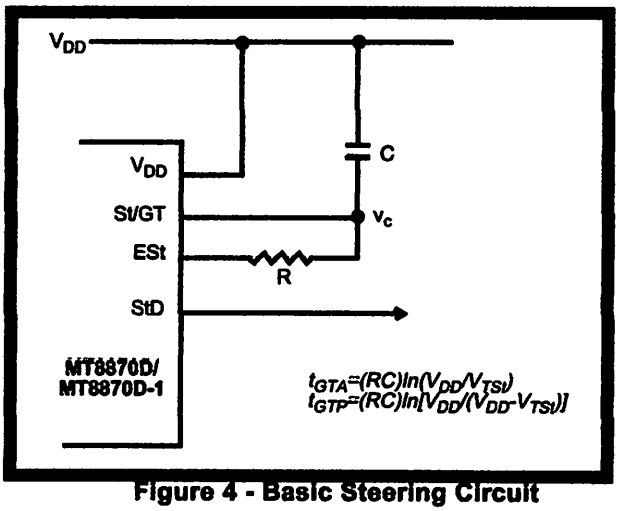


Figure 4 - Basic Steering Circuit

providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 4) to rise as the capacitor discharges. Provided signal

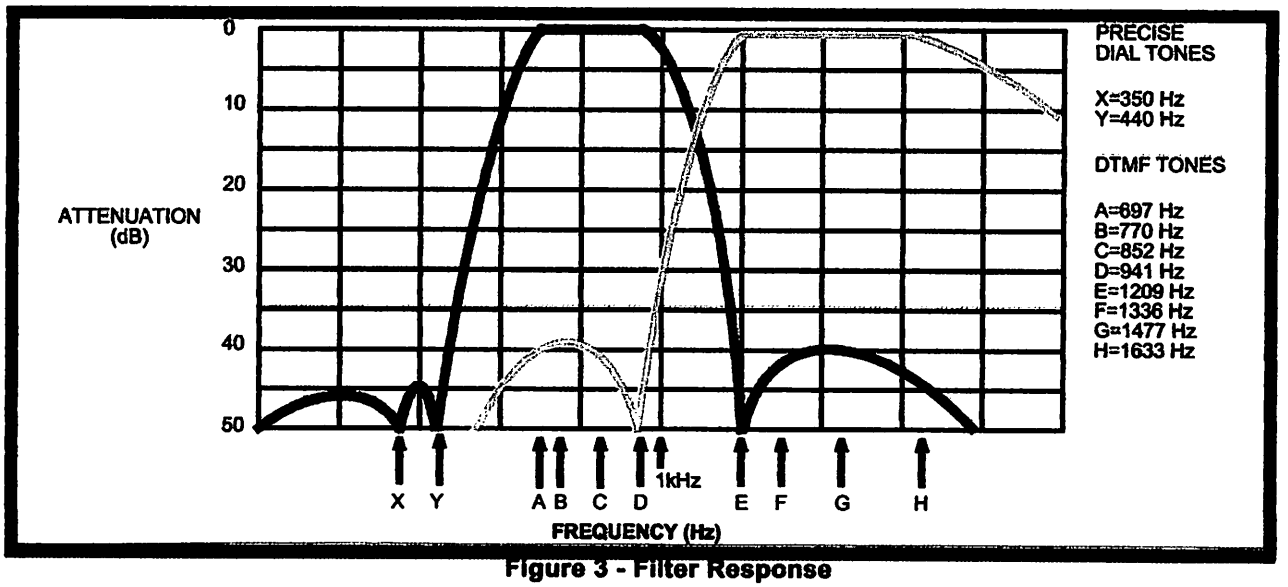


Figure 3 - Filter Response

dition is maintained (ESt remains high) for the dation period (t_{GTP}), v_c reaches the threshold $_{St}$) of the steering logic to register the tone pair, hing its corresponding 4-bit code (see Table 1) ı the output latch. At this point the GT output is ivated and drives v_c to V_{DD}. GT continues to drive h as long as ESt remains high. Finally, after a ort delay to allow the output latch to settle, the layed steering output flag (StD) goes high, inalling that a received tone pair has been gistered. The contents of the output latch are ade available on the 4-bit output bus by raising the ee state control input (TOE) to a logic high. The eering circuit works in reverse to validate the erdigit pause between signals. Thus, as well as ecting signals too short to be considered valid, the ceiver will tolerate signal interruptions (dropout) ı short to be considered a valid pause. This facility, gether with the capability of selecting the steering ıe constants externally, allows the designer to lor performance to meet a wide variety of system quirements.

ıard Time Adjustment

many situations not requiring selection of tone ration and interdigital pause, the simple steering cuit shown in Figure 4 is applicable. Component ues are chosen according to the formula:

$$t_{REC}=t_{DP}+t_{GTP}$$
$$t_{ID}=t_{DA}+t_{GTA}$$

e value of t_{DP} is a device parameter (see Figure) and t_{REC} is the minimum signal duration to be cognized by the receiver. A value for C of 0.1 µF is recommended for most applications, leaving R to be selected by the designer.

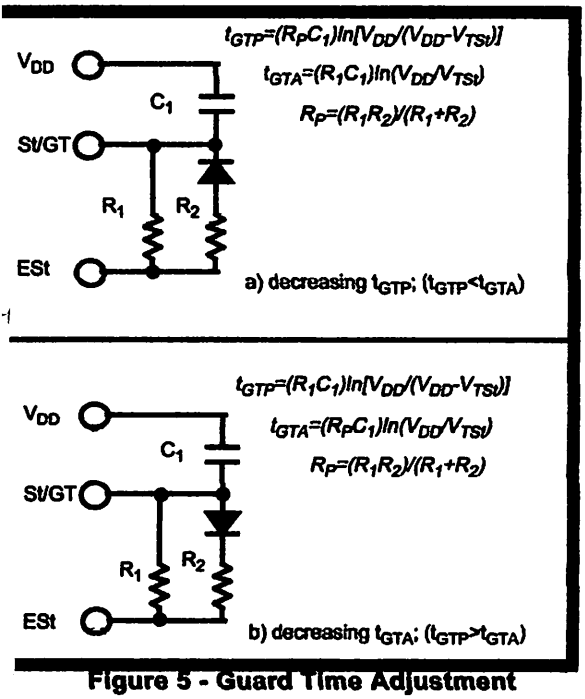


Figure 5 - Guard Time Adjustment

Digit	TOE	INH	ESt	Q_4	Q_3	Q_2	Q_1
ANY	L	X	H	Z	Z	Z	Z
1	H	X	H	0	0	0	1
2	H	X	H	0	0	1	0
3	H	X	H	0	0	1	1
4	H	X	H	0	1	0	0
5	H	X	H	0	1	0	1
6	H	X	H	0	1	1	0
7	H	X	H	0	1	1	1
8	H	X	H	1	0	0	0
9	H	X	H	1	0	0	1
0	H	X	H	1	0	1	0
*	H	X	H	1	0	1	1
#	H	X	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0
A	H	H	L	undetected, the output code will remain the same as the previous detected code			
B	H	H	L				
C	H	H	L				
D	H	H	L				

Table 1. Functional Decode Table
L=LOGIC LOW, H=LOGIC HIGH, Z=HIGH IMPEDANCE
X = DON'T CARE

Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 5.

Power-down and Inhibit Mode

A logic high applied to pin 6 (PWDN) will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones representing characters A, B, C, and D. The output code will remain the same as the previous detected code (see Table 1).

Differential Input Configuration

The input arrangement of the MT8870D/MT8870D-1 provides a differential-input operational amplifier as well as a bias source (V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 10 with the op-amp connected for unity gain and V_{Ref} biasing the input at $^1/_2V_{DD}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5.

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally connected as shown in Figure 10 (Single-Ended Input Configuration). However, it is possible to configure several MT8870D/MT8870D-1 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Figure 7 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, i.e., precision balancing capacitors are not required.

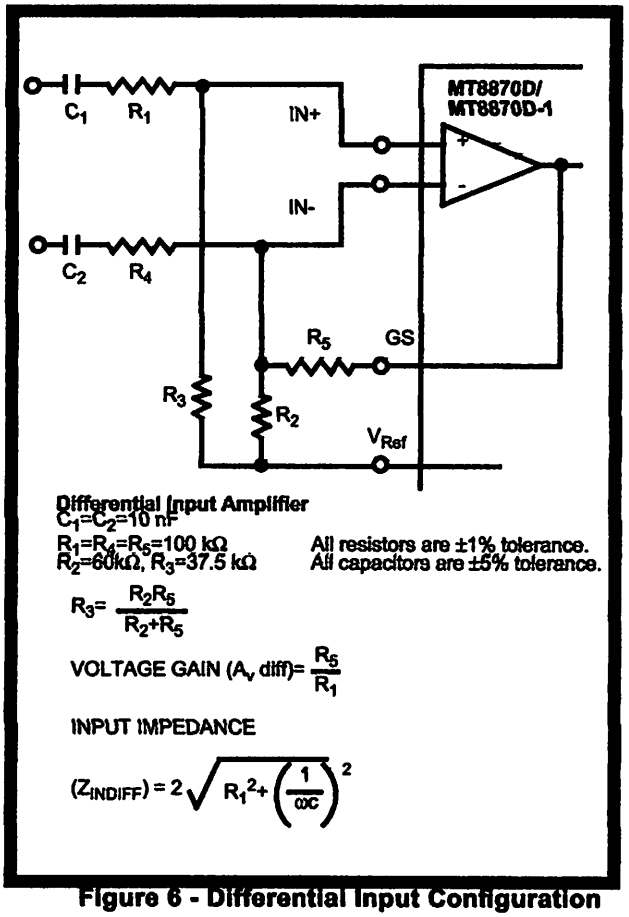


Figure 6 - Differential Input Configuration

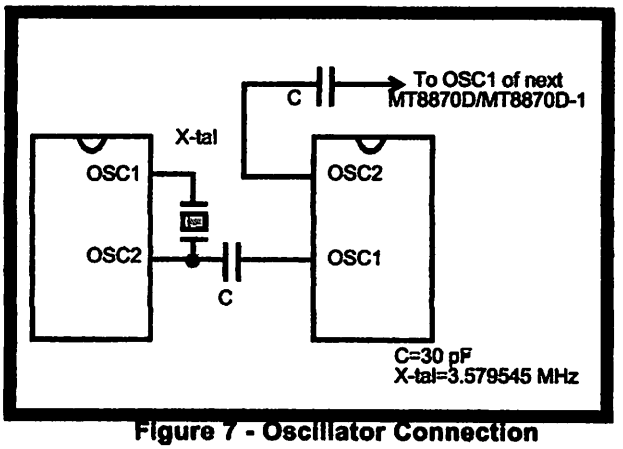


Figure 7 - Oscillator Connection

Parameter	Unit	Resonator
R1	Ohms	10.752
L1	mH	.432
C1	pF	4.984
C0	pF	37.915
Qm	-	896.37
Δf	%	±0.2%

Table 2. Recommended Resonator Specifications

Note: Qm=quality factor of RLC model, i.e., $1/2\Pi fR1C1$.

plications

CEIVER SYSTEM FOR BRITISH TELECOM EC POR 1151

e circuit shown in Fig. 9 illustrates the use of 8870D-1 device in a typical receiver system. BT ec defines the input signals less than -34 dBm as non-operate level. This condition can be attained choosing a suitable values of R_1 and R_2 to ovide 3 dB attenuation, such that -34 dBm input nal will correspond to -37 dBm at the gain setting GS of MT8870D-1. As shown in the diagram, the mponent values of R_3 and C_2 are the guard time quirements when the total component tolerance is . For better performance, it is recommended to e the non-symmetric guard time circuit in Fig. 8.

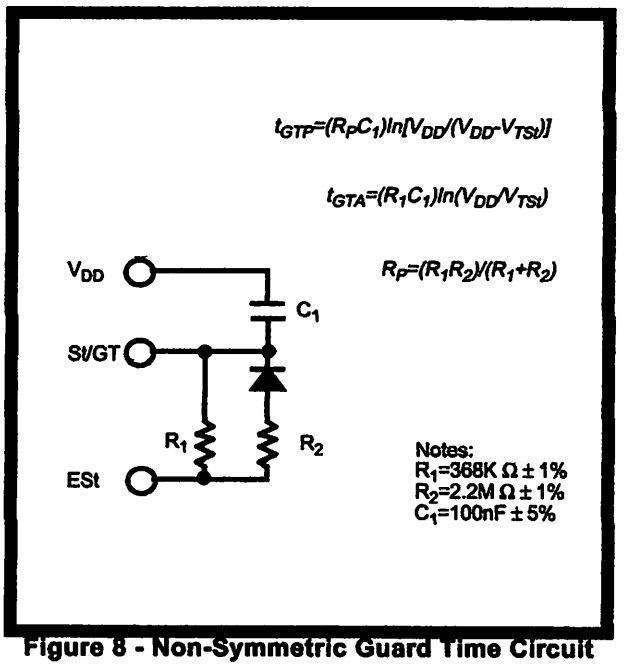
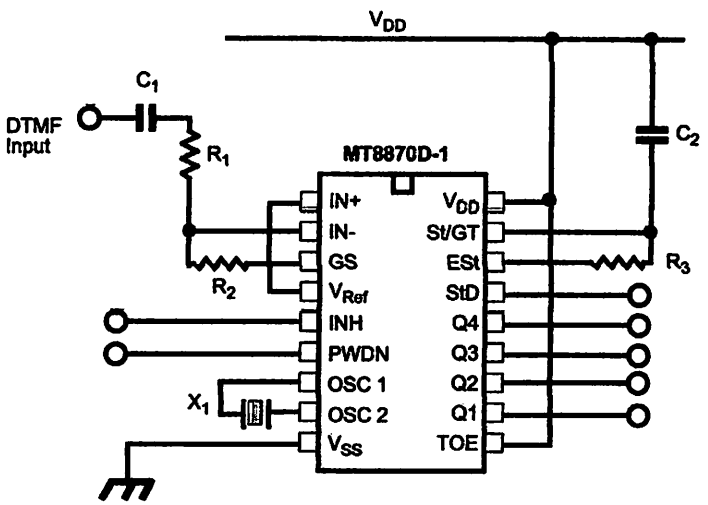


Figure 8 - Non-Symmetric Guard Time Circuit



NOTES:
R_1 = 102KΩ ± 1%
R_2 = 71.5KΩ ± 1%
R_3 = 390KΩ ±1 %
C_1,C_2 = 100 nF ± 5%
X_1 = 3.579545 MHz ± 0.1%
V_{DD} = 5.0V ± 5%

Figure 9 - Single-Ended Input Configuration for BT or CEPT Spec

Absolute Maximum Ratings†

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage	V_{DD}		7	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin (other than supply)	I_I		10	mA
4	Storage temperature	T_{STG}	-65	+150	°C
5	Package power dissipation	P_D		500	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75 °C at 16 mW / °C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DC Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Operating Temperature	T_O	-40		+85	°C	
3	Crystal/Clock Frequency	fc		3.579545		MHz	
4	Crystal/Clock Freq.Tolerance	Δfc		±0.1		%	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - V_{DD}=5.0V± 5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUPPLY	Standby supply current	I_{DDQ}		10	25	µA	PWDN=V_{DD}
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_O		15		mW	fc=3.579545 MHz
4	INPUTS	High level input	V_{IH}	3.5			V	V_{DD}=5.0V
5		Low level input voltage	V_{IL}			1.5	V	V_{DD}=5.0V
6		Input leakage current	I_{IH}/I_{IL}		0.1		µA	V_{IN}=V_{SS} or V_{DD}
7		Pull up (source) current	I_{SO}		7.5	20	µA	TOE (pin 10)=0, V_{DD}=5.0V
8		Pull down (sink) current	I_{SI}		15	45	µA	INH=5.0V, PWDN=5.0V, V_{DD}=5.0V
9		Input impedance (IN+, IN-)	R_{IN}		10		MΩ	@ 1 kHz
10		Steering threshold voltage	V_{TSt}	2.2	2.4	2.5	V	V_{DD} = 5.0V
11	OUTPUTS	Low level output voltage	V_{OL}			V_{SS}+0.03	V	No load
12		High level output voltage	V_{OH}	V_{DD}-0.03			V	No load
13		Output low (sink) current	I_{OL}	1.0	2.5		mA	V_{OUT}=0.4 V
14		Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT}=4.6 V
15		V_{Ref} output voltage	V_{Ref}	2.3	2.5	2.7	V	No load, V_{DD} = 5.0V
16		V_{Ref} output resistance	R_{OR}		1		kΩ	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

erating Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C ,unless otherwise stated.
n Setting Amplifier

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
	Input leakage current	I_{IN}			100	nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}	10			MΩ	
3	Input offset voltage	V_{OS}			25	mV	
4	Power supply rejection	PSRR	50			dB	1 kHz
5	Common mode rejection	CMRR	40			dB	0.75 V ≤ V_{IN} ≤ 4.25 V biased at V_{Ref} =2.5 V
6	DC open loop voltage gain	A_{VOL}	32			dB	
7	Unity gain bandwidth	f_C	0.30			MHz	
8	Output voltage swing	V_O	4.0			V_{pp}	Load ≥ 100 kΩ to V_{SS} @ GS
9	Maximum capacitive load (GS)	C_L			100	pF	
10	Resistive load (GS)	R_L			50	kΩ	
11	Common mode range	V_{CM}	2.5			V_{pp}	No Load

T8870D AC Electrical Characteristics - V_{DD}=5.0V ±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C , using Test Circuit shown in Figure 10.

	Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
	Valid input signal levels (each tone of composite signal)		-29		+1	dBm	1,2,3,5,6,9
			27.5		869	mV_{RMS}	1,2,3,5,6,9
	Negative twist accept				8	dB	2,3,6,9,12
	Positive twist accept				8	dB	2,3,6,9,12
	Frequency deviation accept		±1.5% ± 2 Hz				2,3,5,9
	Frequency deviation reject		±3.5%				2,3,5,9
	Third tone tolerance			-16		dB	2,3,4,5,9,10
	Noise tolerance			-12		dB	2,3,4,5,7,9,10
	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

ypical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

OTES
dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
Digit sequence consists of all DTMF tones.
Tone duration= 40 ms, tone pause= 40 ms.
Signal condition consists of nominal DTMF frequencies.
Both tones in composite signal have an equal amplitude.
Tone pair is deviated by ±1.5 %± 2 Hz.
Bandwidth limited (3 kHz) Gaussian noise.
The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
For an error rate of better than 1 in 10,000.
Referenced to lowest level frequency component in DTMF signal.
Referenced to the minimum valid accept level.
Guaranteed by design and characterization.

MT8870D-1 AC Electrical Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C , using Test Circuit shown in Figure 10.

	Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	Valid input signal levels (each tone of composite signal)		-31		+1	dBm	Tested at V_{DD}=5.0V 1,2,3,5,6,9
			21.8		869	mV_{RMS}	
2	Input Signal Level Reject		-37			dBm	Tested at V_{DD}=5.0V 1,2,3,5,6,9
			10.9			mV_{RMS}	
3	Negative twist accept				8	dB	2,3,6,9,13
4	Positive twist accept				8	dB	2,3,6,9,13
5	Frequency deviation accept		±1.5%± 2 Hz				2,3,5,9
6	Frequency deviation reject		±3.5%				2,3,5,9
7	Third zone tolerance			-18.5		dB	2,3,4,5,9,12
8	Noise tolerance			-12		dB	2,3,4,5,7,9,10
9	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

*NOTES
1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5 %± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Referenced to Fig. 10 input DTMF tone level at -25dBm (-28dBm at GS Pin) interference frequency range between 480-3400Hz.
13. Guaranteed by design and characterization.

Electrical Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ To ≤ +85°C , using Test Circuit shown in Figure 10.

		Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
	TIMING	Tone present detect time	t_{DP}	5	11	14	ms	Note 1
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 1
3		Tone duration accept	t_{REC}			40	ms	Note 2
4		Tone duration reject	$t_{\overline{REC}}$	20			ms	Note 2
5		Interdigit pause accept	t_{ID}			40	ms	Note 2
6		Interdigit pause reject	t_{DO}	20			ms	Note 2
7	OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	µs	TOE=V_{DD}
8		Propagation delay (St to StD)	t_{PStD}		12	16	µs	TOE=V_{DD}
9		Output data set up (Q to StD)	t_{QStD}		3.4		µs	TOE=V_{DD}
0		Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	load of 10 kΩ, 50 pF
1		Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	load of 10 kΩ, 50 pF
2	PDWN	Power-up time	t_{PU}		30		ms	Note 3
3		Power-down time	t_{PD}		20		ms	
4	CLOCK	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
5		Clock input rise time	t_{LHCL}			110	ns	Ext. clock
6		Clock input fall time	t_{HLCL}			110	ns	Ext. clock
7		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
8		Capacitive load (OSC2)	C_{LO}			30	pF	

ypical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

OTES:
Used for guard-time calculation purposes only.
These, user adjustable parameters, are not device specifications. The adjustable settings of these minimums and maximums are recommendations based upon network requirements.
With valid tone present at input, t_{PU} equals time from PDWN going low until ESt going high.

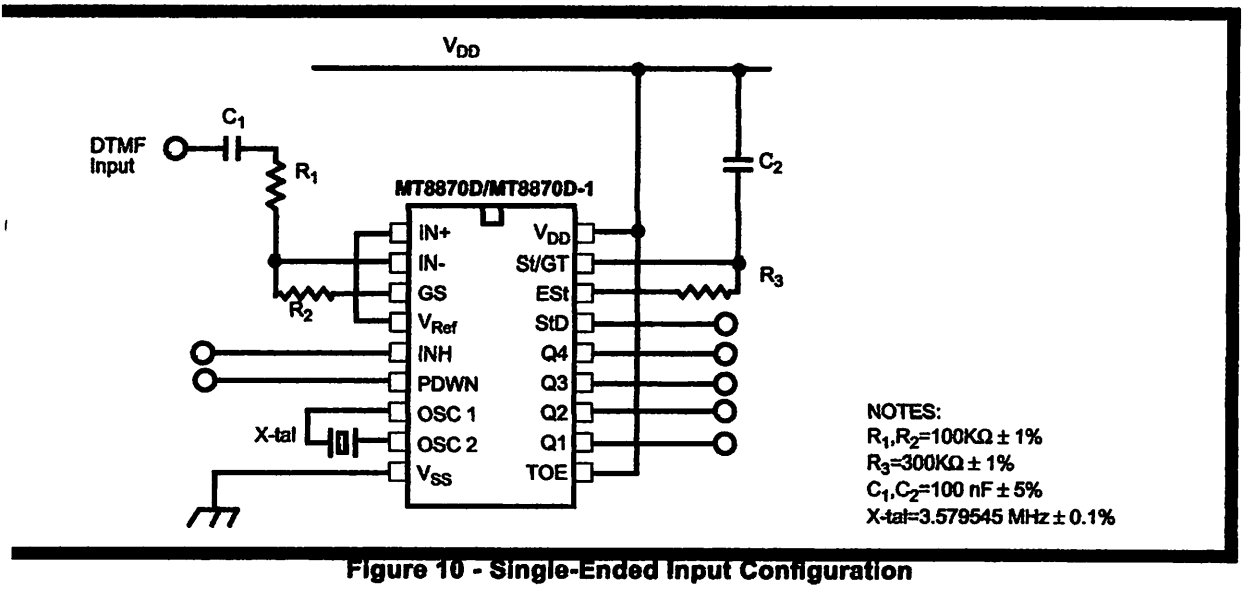
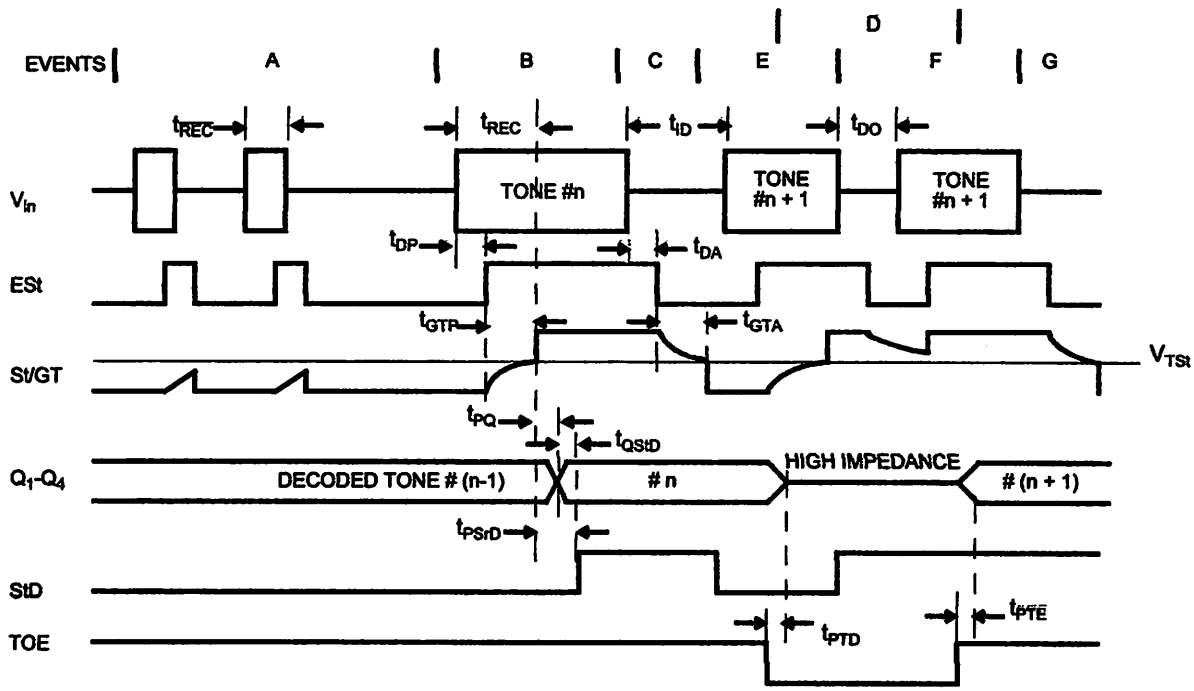


Figure 10 - Single-Ended Input Configuration



EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.

B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS

C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMIAN LATCHED UNTIL NEXT VALID TONE.

D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.

E) TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE).

F) ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED.

G) END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

EXPLANATION OF SYMBOLS

V_{in} DTMF COMPOSITE INPUT SIGNAL.

ESt EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.

St/GT STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.

Q_1-Q_4 4-BIT DECODED TONE OUTPUT.

StD DELAYED STEERING OUTPUT. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL.

TOE TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE.

t_{REC} MAXIMUM DTMF SIGNAL DURATION NOT DETECED AS VALID

t_{REC} MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION

t_{ID} MAXIMUM TIME BETWEEN VALID DTMF SIGNALS.

t_{DO} MAXIMUM ALLOWABLE DROP OUT DURING VALID DTMF SIGNAL.

t_{DP} TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS.

t_{DA} TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS.

t_{GTP} GUARD TIME, TONE PRESENT.

t_{GTA} GUARD TIME, TONE ABSENT.

Figure 11 - Timing Diagram

es:

National Semiconductor

February 2000

LM555 Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

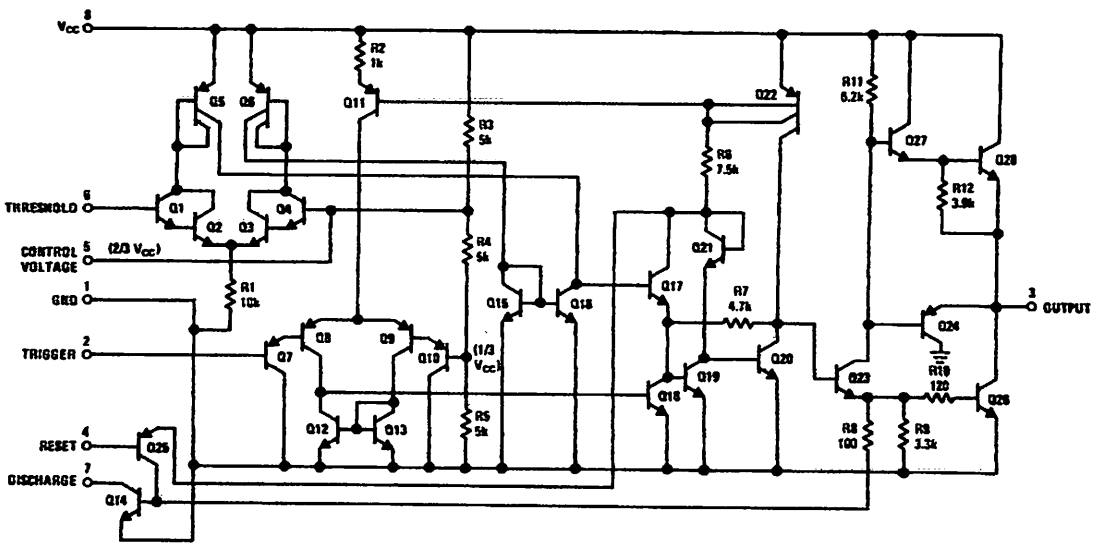
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

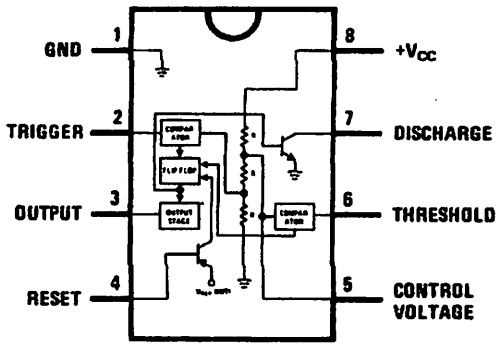
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Connection Diagram

Dual-In-Line, Small Outline and Molded Mini Small Outline Packages



Top View

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

Absolute Maximum Ratings (Note 2)

Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Packages	
(SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

(T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 4)		10	15	mA
Timing Error, Monostable					
Initial Accuracy			1		%
Drift with Temperature	R_A = 1k to 100kΩ, C = 0.1µF, (Note 5)		50		ppm/°C
Accuracy over Temperature			1.5		%
Drift with Supply			0.1		%/V
Timing Error, Astable					
Initial Accuracy			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100kΩ, C = 0.1µF, (Note 5)		150		ppm/°C
Accuracy over Temperature			3.0		%
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V		5		V
	V_{CC} = 5V		1.67		V
Trigger Current			0.5	0.9	µA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V	9	10	11	V
	V_{CC} = 5V	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat (Note 7)					
Output Low	V_{CC} = 15V, I_7 = 15mA		180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5mA		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V				
	I_{SINK} = 10mA		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.75	V
	I_{SINK} = 100mA		2	2.5	V
	I_{SINK} = 200mA		2.5		V
	V_{CC} = 5V				
	I_{SINK} = 8mA				V
	I_{SINK} = 5mA		0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200mA, V_{CC} = 15V		12.5		V
	I_{SOURCE} = 100mA, V_{CC} = 15V	12.75	13.3		V
	V_{CC} = 5V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 106°C/W (DIP), 170°C/W (S0-8), and 204°C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

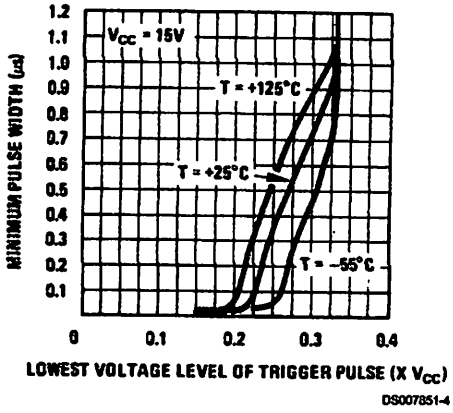
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

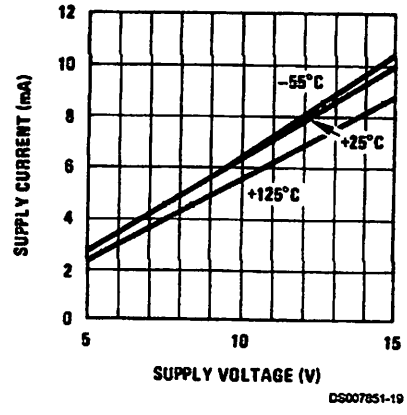
Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Typical Performance Characteristics

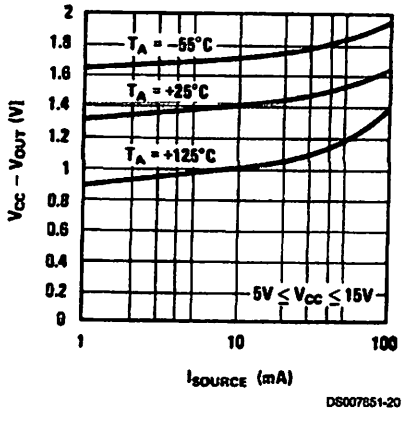
Minimum Pulse Width Required for Triggering



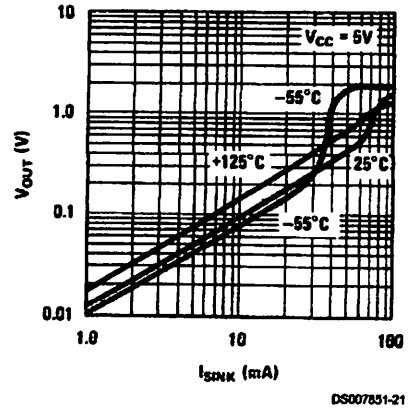
Supply Current vs. Supply Voltage



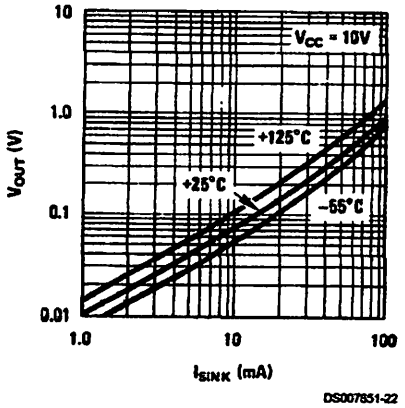
High Output Voltage vs. Output Source Current



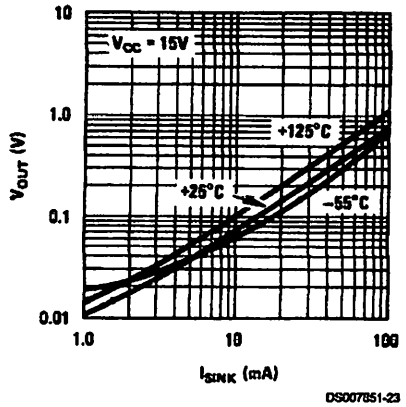
Low Output Voltage vs. Output Sink Current



Low Output Voltage vs. Output Sink Current

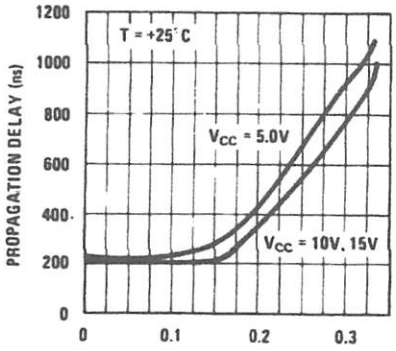


Low Output Voltage vs. Output Sink Current



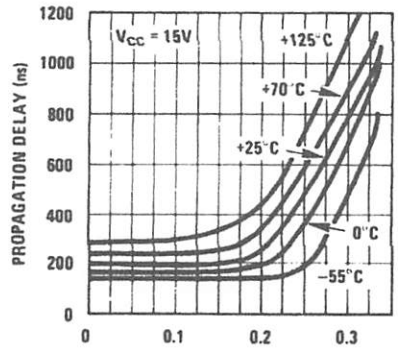
Typical Performance Characteristics (Continued)

Output Propagation Delay vs. Voltage Level of Trigger Pulse



DS007851-24

Output Propagation Delay vs. Voltage Level of Trigger Pulse



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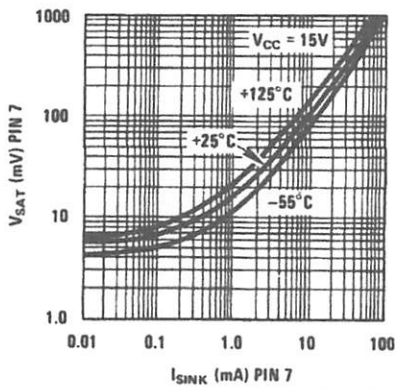
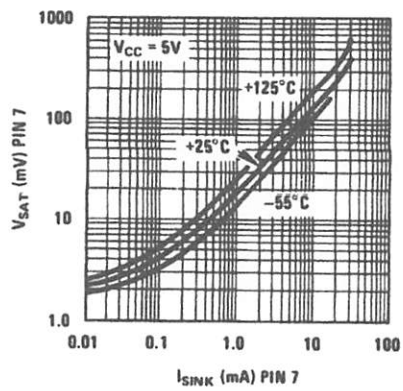
Discharge Transistor (Pin 7) Voltage vs. Sink Current



DS007851-26

Discharge Transistor (Pin 7) Voltage vs. Sink Current



DS007851-27

Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

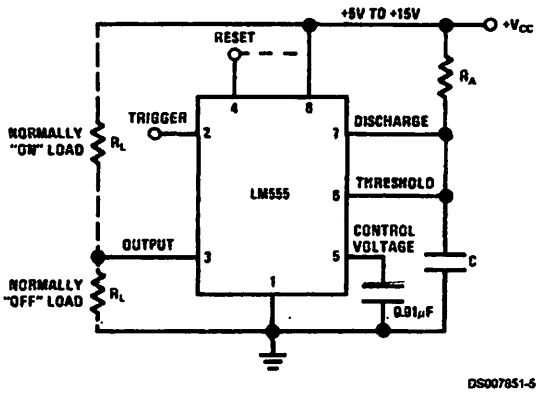
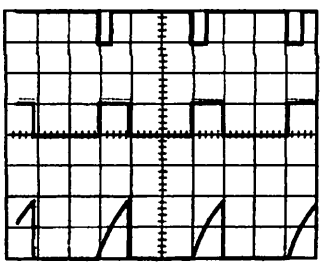


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



V_{CC} = 5V — Top Trace: Input 5V/Div.
TIME = 0.1 ms/DIV. — Middle Trace: Output 5V/Div.
R_A = 9.1kΩ — Bottom Trace: Capacitor Voltage 2V/Div.
C = 0.01µF

FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10µs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

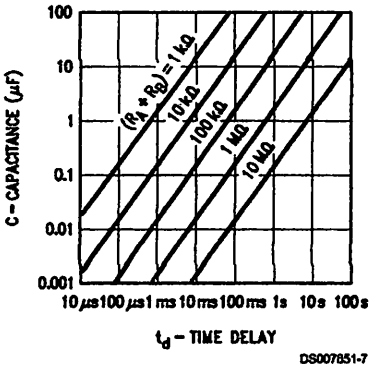


FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

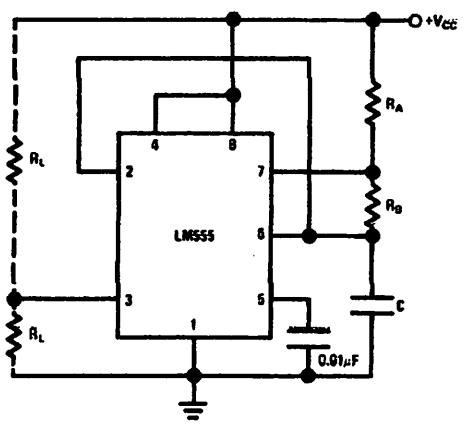
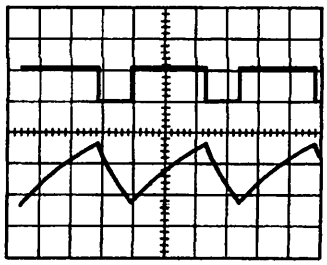


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



V_{CC} = 5V Top Trace: Output 5V/Div.
TIME = 20µs/DIV. Bottom Trace: Capacitor Voltage 1V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

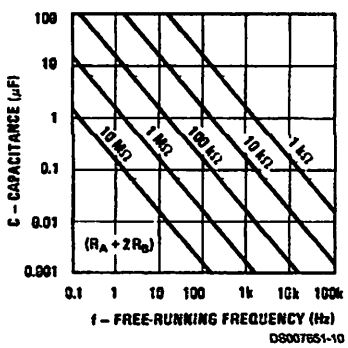
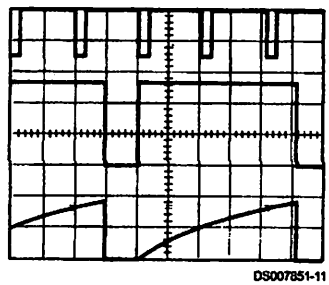


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



V_{CC} = 5V Top Trace: Input 4V/Div.
TIME = 20µs/DIV. Middle Trace: Output 2V/Div.
R_A = 9.1kΩ Bottom Trace: Capacitor 2V/Div.
C = 0.01µF

FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

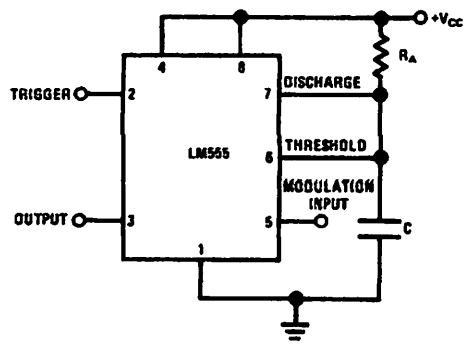
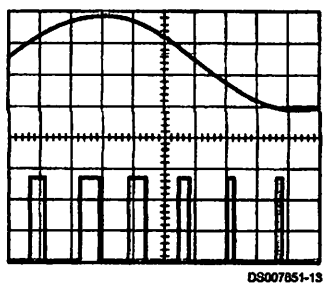


FIGURE 8. Pulse Width Modulator



V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1kΩ
C = 0.01µF

FIGURE 9. Pulse Width Modulator

Applications Information (Continued)

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

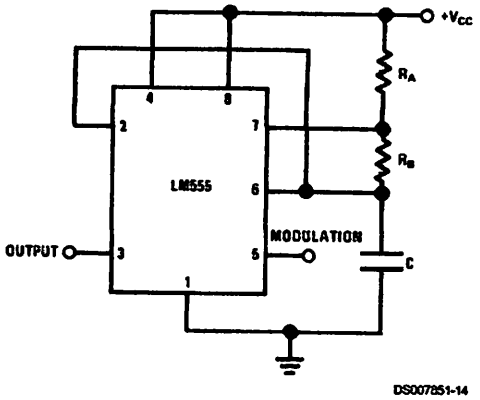
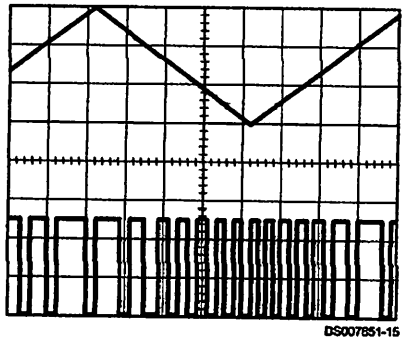


FIGURE 10. Pulse Position Modulator



cc = 5V
IME = 0.1 ms/DIV.
A = 3.9kΩ
B = 3kΩ
= 0.01μF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output 2V/Div.

FIGURE 11. Pulse Position Modulator

INEAR RAMP

/hen the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.

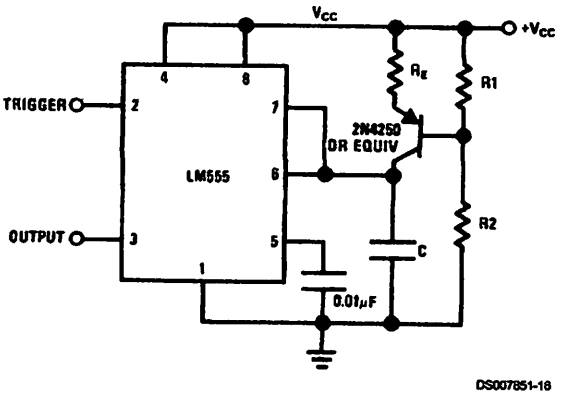


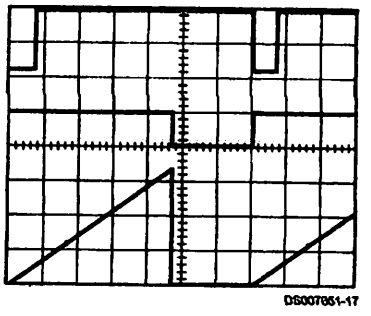
FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$

$$V_{BE} \simeq 0.6V$$



V_{CC} = 5V
TIME = 20μs/DIV.
R_1 = 47kΩ
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 μF

Top Trace: Input 3V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 13. Linear Ramp

Applications Information (Continued)

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ ln\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$

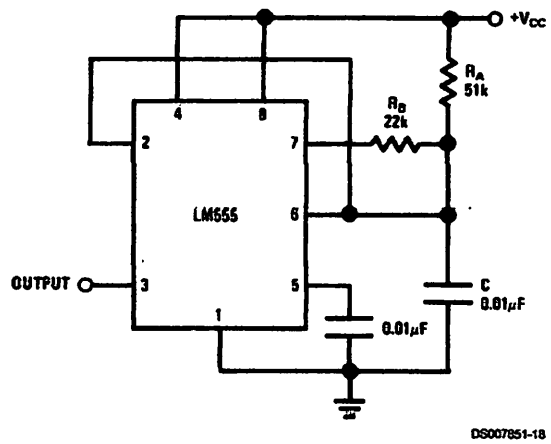


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

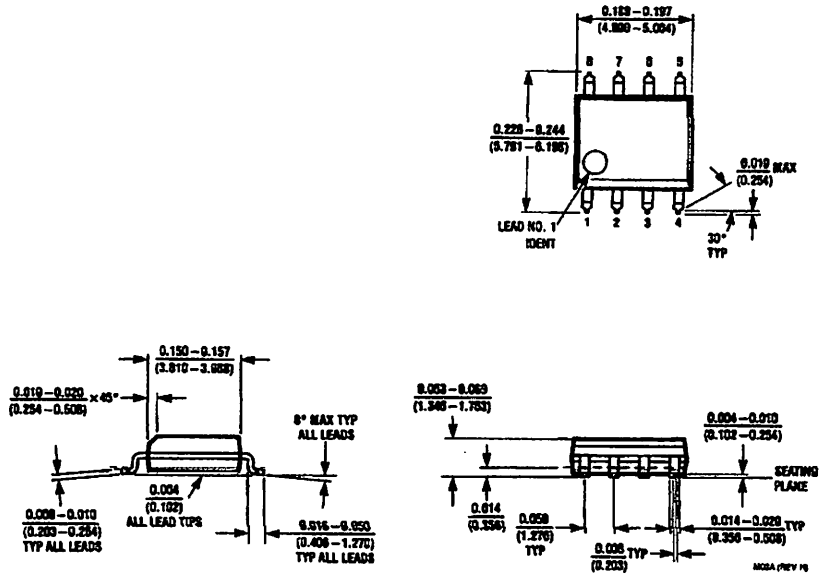
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

Lower comparator storage time can be as long as 10µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10µs minimum.

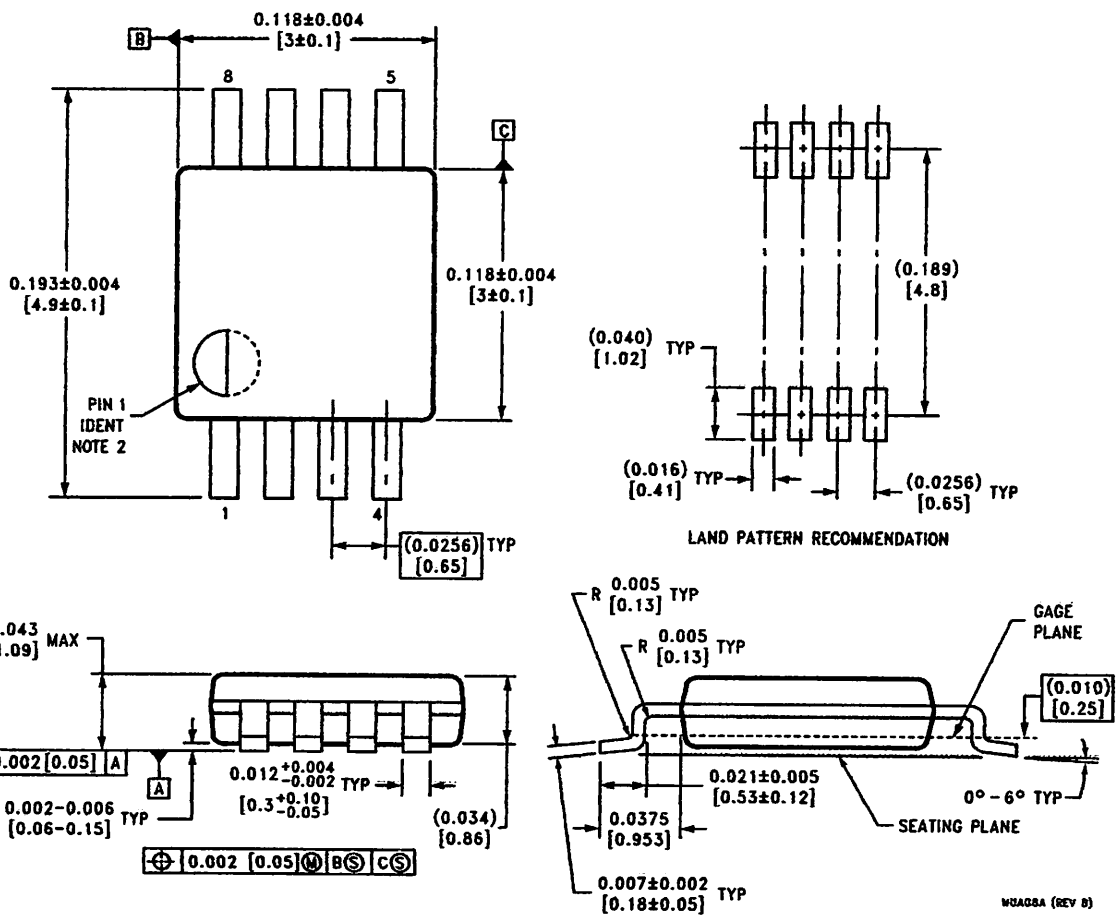
Delay time reset to output is 0.47µs typical. Minimum reset pulse width must be 0.3µs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

Physical Dimensions inches (millimeters) unless otherwise noted

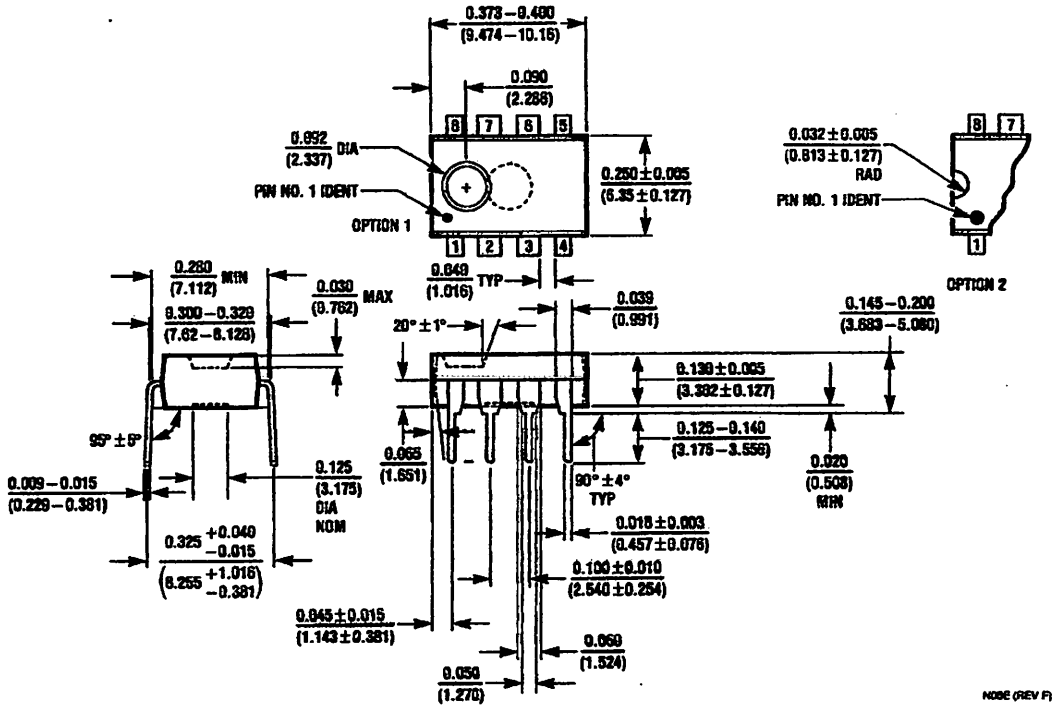


Small Outline Package (M)
NS Package Number M08A



8-Lead (0.118" Wide) Molded Mini Small Outline Package
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
NS Package Number N08E

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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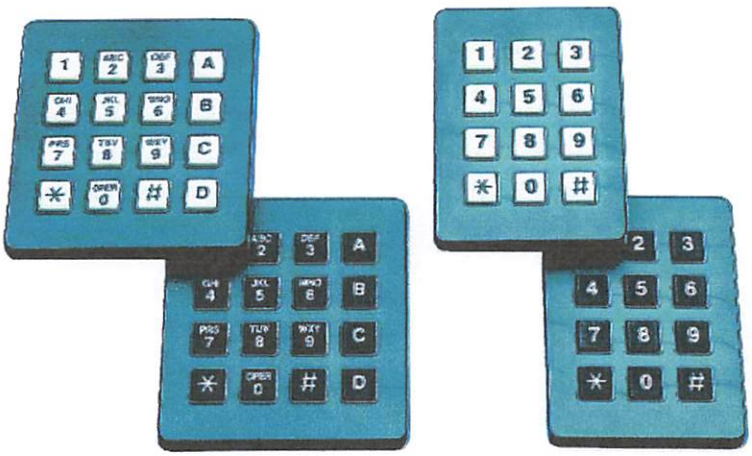
SERIES 96
Conductive Rubber

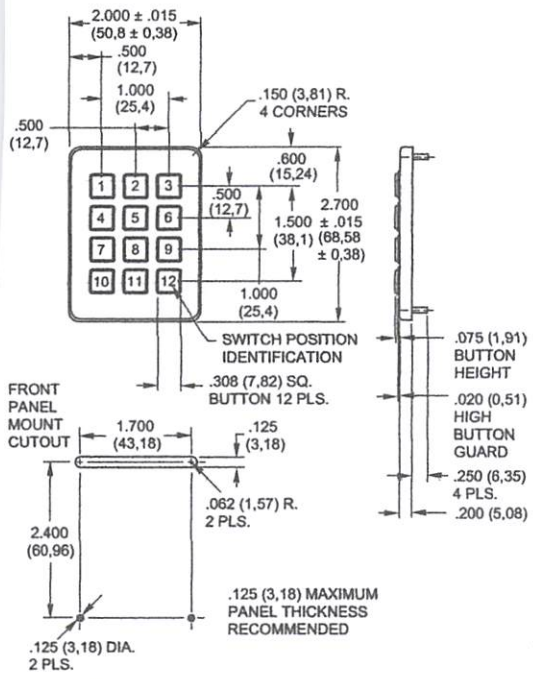
FEATURES
- Quality, Economical Keyboards
- Easily Customized Legends
- Matrix Circuitry
- Backlit and Shielded Options Available
- Termination Mates With Standard Connectors
- Tactile Feedback to Operator
- 1,000,000 Operations per Button
- Compatible With High Resistance Logic Inputs



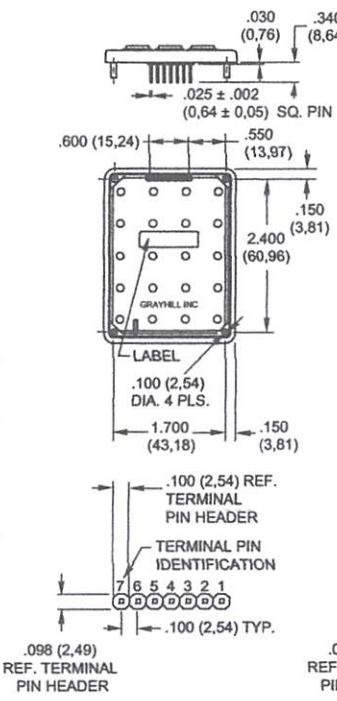
The Series 96 is Grayhill's most economical 3x4 and 4x4 keypad family. The contact system utilizes conductive rubber to mate the appropriate PC board traces. Offered in matrix circuitry, with shielded and backlit options. Built with quality component parts, the Series 96 is subjected to our rigid statistical process control to insure that it meets our reliability standards.

DIMENSIONS In inches (and millimeters)

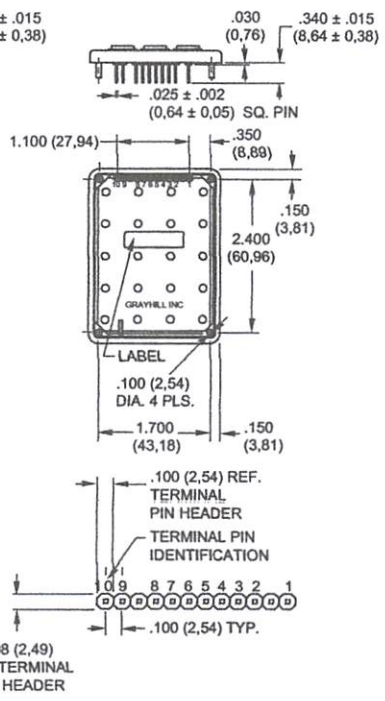
3x4 Front Mount Keyboard



Standard Versions

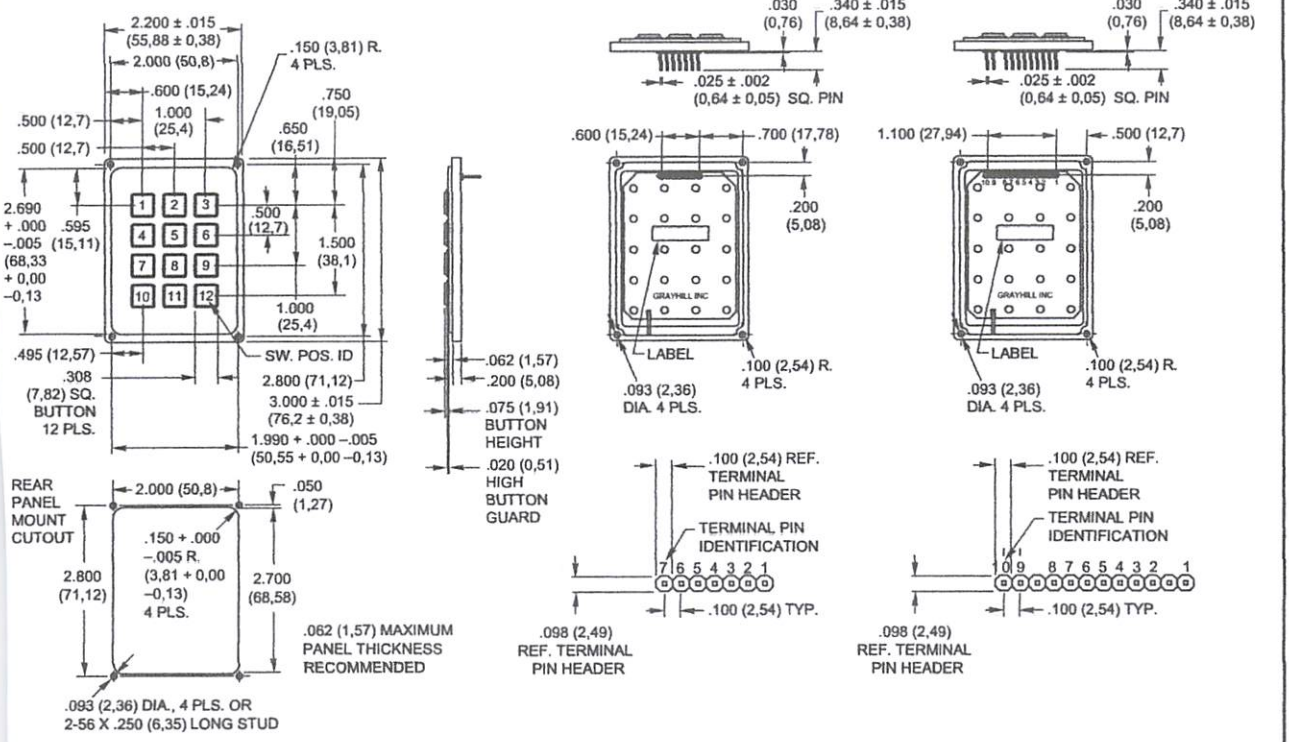


Shielded/Backlit Versions



DIMENSIONS In inches (and millimeters)

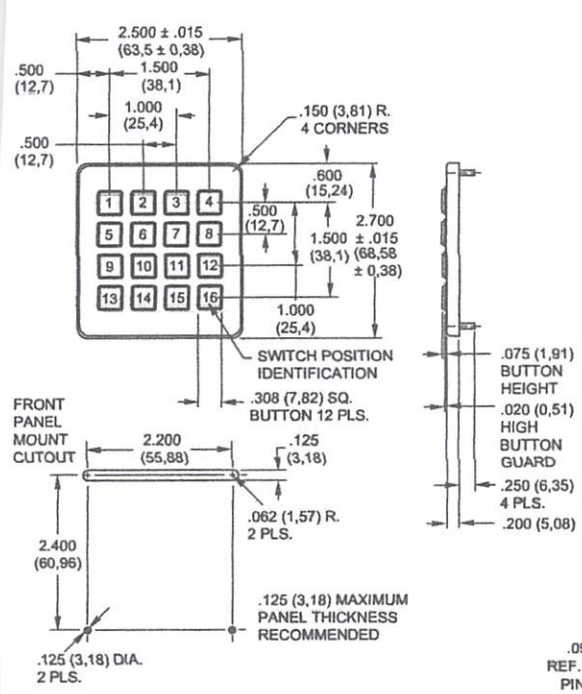
3x4 Rear Mount Keyboard



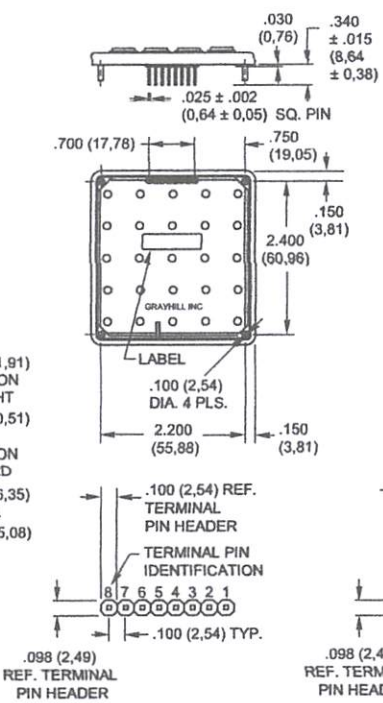
Standard Versions

Shielded/Backlit Versions

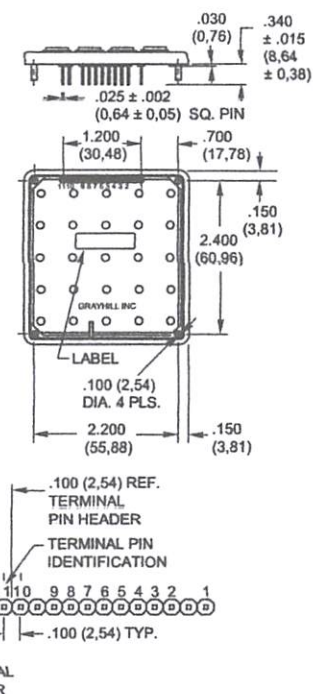
4x4 Front Mount Keyboard



Standard Versions

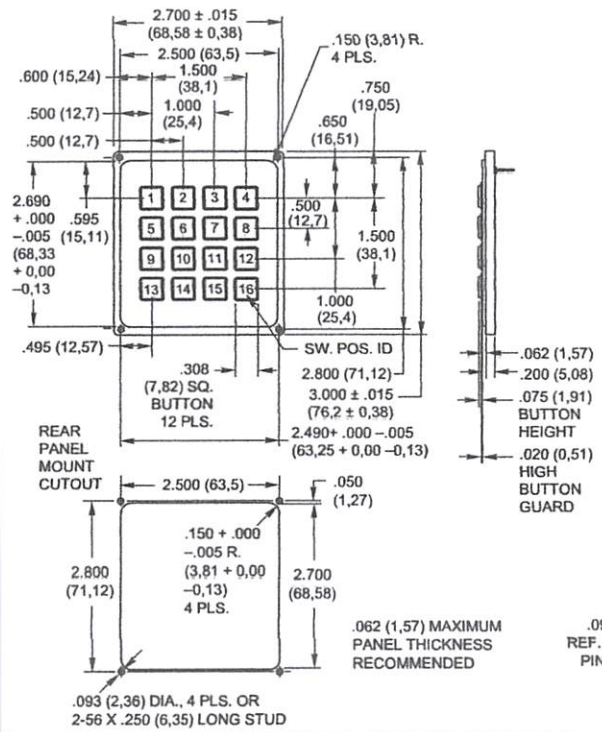


Shielded/Backlit Versions

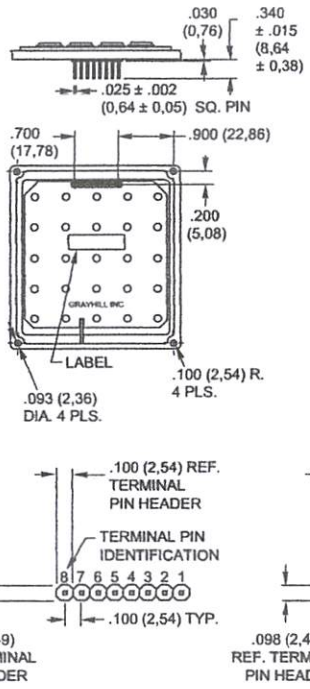


DIMENSIONS In inches (and millimeters)

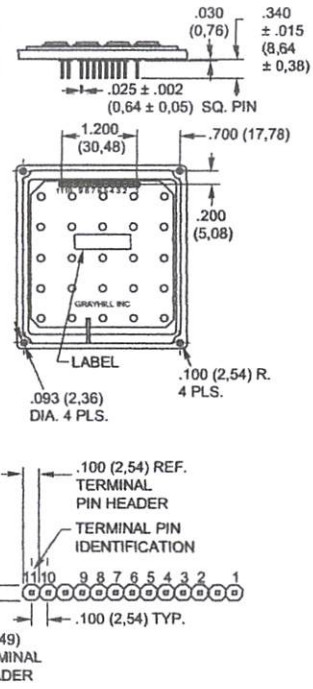
4x4 Rear Mount Keyboard



Standard Versions



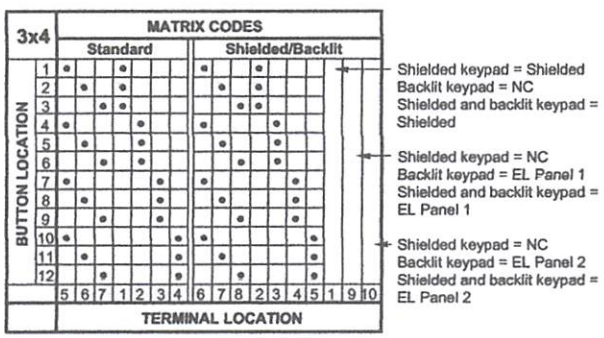
Shielded/Backlit Versions



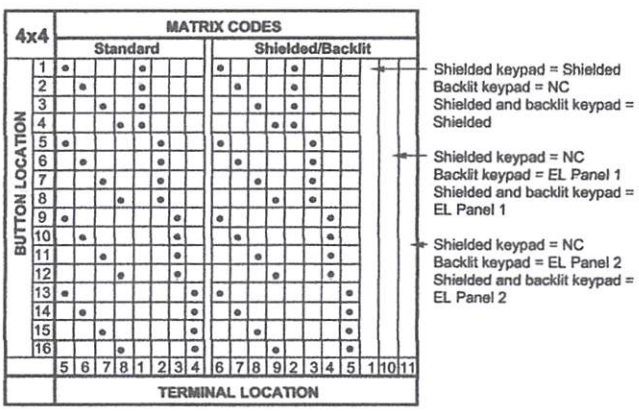
MODE AND TRUTH TABLES

Dots in the chart indicate connected terminals when switch is closed.
Terminals are identified on the keyboard.

12 Button Keypads



16 Button Keypads



SPECIFICATIONS

Rating Criteria

Rating at 12 Vdc: 5 milliamps for .5 seconds
Contact Bounce: < 12 milliseconds
Contact Resistance: < 100 ohms (at stated operating force)
Voltage Breakdown: 250 Vac between components
Mechanical Operation Life: 1,000,000 operations per key
Insulation Resistance: > 10^{12} ohms @ 500 Vdc
Push Out Force Per Pin: 5 lbs.

Operating Features

Travel: .040 minimum
Operating Force: 175 ± 40 grams
Operating Temperature: -30°C to +80°C

Material and Finishes

Terminal Pin: Phosphor bronze, solder-plated
PC Board: FR-4 glass cloth epoxy
Keypad: Silicone rubber, durometer 50 ± 5
Housing: ABS, cycolac "KJW"
Housing Color: Black

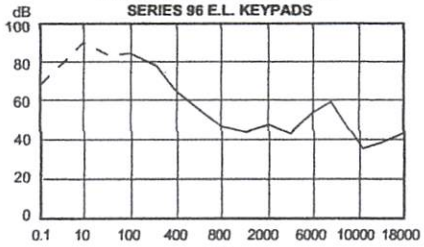
Shielding Effectiveness

Results shown are typical for a standard Grayhill Series 84S keyboard. A conductive gasket will generally increase the shielding, depending on the size and shape of the gasket and its material. Data derived for E-Field Radiation.

Test Method:
Measurements were made with the keyboard mounted to a brass plate, which in turn was mounted to a shielded enclosure containing the receiving equipment. A signal generator provided the frequency source that was radiated from the transmitting antenna to the enclosed receiving antenna. The spacing between antennas was maintained constant throughout the frequency range. The effectiveness rating is determined by establishing a reference reading without obstruction between the two antennas and determining the difference between that reading and the test setup reading.

Note:
When measured in actual equipment, shielding effectiveness is determined by many factors. This method accurately represents the shielding effectiveness of the Grayhill Series 84S under ideal test conditions.

SHIELDING EFFECTIVENESS OF SERIES 96 E.L. KEYPADS



— – Represents shielding effectiveness greater than or equal to line.

Frequency M Hz	Rating in dB
0.1	≥ 66.2
10	≥ 94.8
100	90.5
400	64.2
800	42.3
2,000	40.5
6,000	33.1
10,000	34.4
18,000	37.0

STANDARD LEGENDS

Available through Grayhill Distributors

To order one of the configurations below, use the dash number shown here; select the keypad size and code, and order the part number with the appropriate legend dash number.

-102

-006

-152

-056

ORDERING INFORMATION

96AB2-102-FS-EL

Grayhill Series Number
Keyboard Size: A = 3x4, B = 4x4
Circuitry: B2 = Matrix (terminal pin header)

E.L. Panel Backlighting Option
EL = Backlit, Blank = Non-backlit
EMI/RFI Shielding Option
S = Shielded, Blank = Non-shielded
Mounting Option: F = Front panel mount, R = Rear panel mount
Standard Legend Choices
12 Position legends
102 = Black legends on a white button
152 = White legends on a black button
16 Position legends
006 = Black legends on a white button
056 = White legends on a black button

Available from your local Grayhill Distributor. For prices and discounts, contact a local Sales Office, an authorized local Distributor or Grayhill.

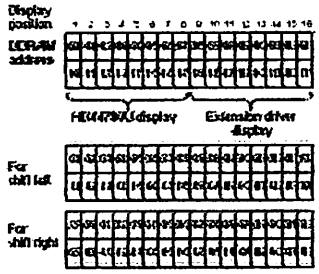
M1632 MODULE LCD 16 X 2 BARIS (M1632)

Deskripsi:

M1632 adalah merupakan modul LCD dengan tampilan 16 x 2 baris dengan konsumsi daya y rendah. Modul ini dilengkapi dengan mikrokontroler yang didisain khusus untuk mengendalikan L(Mikrokontroler HD44780 buatan Hitachi yang berfungsi sebagai pengendali LCD ini mempunyai CGR((Character Generator Read Only Memory), CGRAM (Character Generator Random Access Memory) DDRAM (Display Data Random Access Memory).

DDRAM

DDRAM adalah merupakan memori tempat karakter yang ditampilkan berada. Contoh, ur karakter 'A' atau 41H yang ditulis pada alamat 00, maka karakter tersebut akan tampil pada baris pert dan kolom pertama dari LCD. Apabila karakter tersebut ditulis di alamat 40, maka karakter tersebut a tampil pada baris kedua kolom pertama dari LCD.



Gambar 1
DDRAM M1632 (diambil dari data sheet HD44780)

CGRAM

CGRAM adalah merupakan memori untuk menggambarkan **pola sebuah karakter** di m bentuk dari karakter dapat diubah-ubah sesuai keinginan. Namun memori ini akan hilang saat power sup tidak aktif, sehingga pola karakter akan hilang.

CGROM

CGROM adalah merupakan memori untuk menggambarkan **pola sebuah karakter** di mana p tersebut sudah ditentukan secara permanen dari HD44780 sehingga pengguna tidak dapat mengubah l Namun karena ROM bersifat permanen, maka pola karakter tersebut tidak akan hilang walaupun po supply tidak aktif

Pada gambar 2, tampak terlihat pola-pola karakter yang tersimpan dalam lokasi-lokasi tert dalam CGROM. Pada saat HD44780 akan menampilkan data 41H yang tersimpan pada DDRAM, m HD44780 akan mengambil data di alamat 41H (0100 0001) yang ada pada CGROM yaitu pola karakter A

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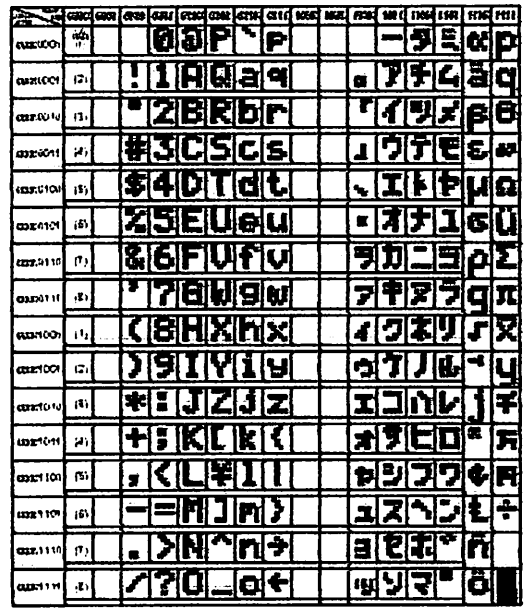
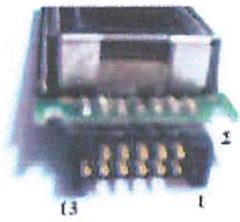


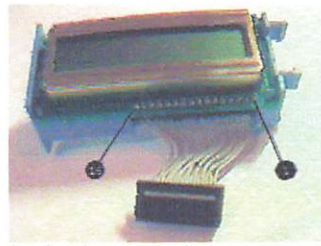
Gambar 2
Hubungan antara CGROM dan DDRAM (diambil dari data sheet HD44780)

Pin Out

No	Nama Pin	Deskripsi
1	VCC	+5V
2	GND	0V
3	VEE	Tegangan Kontras LCD
4	RS	Register Select, 0 = Register Perintah, 1 = Register I
5	R/W	1 = Read, 0 = Write
6	E	Enable Clock LCD, logika 1 setiap kali pengiriman . pembacaan data
7	D0	Data Bus 0
8	D1	Data Bus 1
9	D2	Data Bus 2
10	D3	Data Bus 3
11	D4	Data Bus 4
12	D5	Data Bus 5
13	D6	Data Bus 6
14	D7	Data Bus 7
15	Anoda (Kabel coklat untuk LCD Hitachi)	Tegangan positif backlight
16	Katoda (Kabel merah untuk LCD Hitachi)	Tegangan negatif backlight



Gambar 3
Pin Out M1632 LCD Hitachi



Gambar 4
Pin Out LCD M1632 Standard

Register

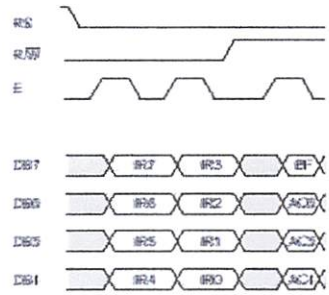
HD44780, mempunyai dua buah Register yang aksesnya diatur dengan menggunakan kaki Pada saat RS berlogika 0, maka register yang diakses adalah Register Perintah dan pada saat RS berlog 1, maka register yang diakses adalah Register Data

Register Perintah

Register ini adalah register di mana perintah-perintah dari mikrokontroler ke HD44780 pada : proses penulisan data atau tempat status dari HD44780 dapat dibaca pada saat pembacaan data.

Penulisan Data ke Register Perintah

Penulisan data ke Register Perintah dilakukan dengan tujuan mengatur tampilan LCD, inisiali dan mengatur Address Counter maupun Address Data. Gambar 5 menunjukkan proses penulisan data register perintah dengan menggunakan mode 4 bit interface. Kondisi RS berlogika 0 menunjukkan al data ke Register Perintah. RW berlogika 0 yang menunjukkan proses penulisan data akan dilakukan. Nib tinggi (bit 7 sampai bit 4) terlebih dahulu dikirimkan dengan diawali pulsa logika 1 pada E Clc Kemudian Nibble rendah (bit 3 sampai bit 0) dikirimkan dengan diawali pulsa logika 1 pada E Clock l: Untuk mode 8 bit interface, proses penulisan dapat langsung dilakukan secara 8 bit (bit 7 ... bit 0) diawali sebuah pulsa logika 1 pada E Clock.



Gambar 5
Timing diagram Penulisan Data ke Register Perintah Mode 4 bit Interface

Tabel 1
Perintah-perintah M1632

Perintah	D7	D6	D5	D4	D3	D2	D1	D0	Deskripsi
Hapus Display	0	0	0	0	0	0	0	1	Hapus Display dan DDRAM
Posisi Awal	0	0	0	0	0	0	1	X	Set Alamat DDRAM di 0
Set Mode	0	0	0	0	0	1	I/D	S	Atur arah pergeseran cursor dan displ

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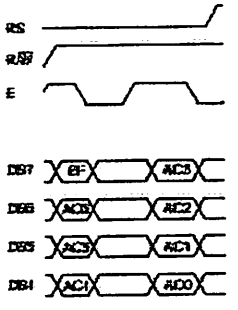
Display On/OFF	0	0	0	0	1	D	C	B	Atur display (D) On/OFF, cursor ON/OFF, Blinking (B)
Geser Cursor/Display	0	0	0	1	S/C	R/L	X	X	Geser Cursor atau display tanpa men alamat DDRAM
Set Fungsi	0	0	1	DL	N	F	X	X	Atur panjang data, jumlah baris : tampil, dan font karakter
Set Alamat CGRAM	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Data dapat dibaca atau ditulis set alamat diatur
Set Alamat DDRAM	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Data dapat dibaca atau ditulis set alamat diatur

X = diabaikan
I/D 1=Increment, 0=Decrement
S 0=Display tidak geser
S/C 1=Display Shift, 0=Geser Cursor
R/L 1=Geser Kiri, 0=Geser Kanan
DL 1=8 bit, 0=4bit
N 1=2 baris, 0=1 baris
F 1=5x10, 0=5x8
D 0=Display OFF, 1=Display ON
C 0=Cursor OFF, 1=Cursor ON
B 0=Blinking OFF, 1=Blinking ON

Pembacaan Data dari Register Perintah

Proses pembacaan data pada register perintah biasa digunakan untuk melihat status busy dari L atau membaca Address Counter. RS diatur pada logika 0 untuk akses ke Register Perintah, R/W diatur p logika 1 yang menunjukkan proses pembacaan data. 4 bit nibble tinggi dibaca dengan diawali pulsa log 1 pada E Clock dan kemudian 4 bit nibble rendah dibaca dengan diawali pulsa logika 1 pada E Clo Untuk Mode 8 bit interface, pembacaan 8 bit (nibble tinggi dan rendah) dilakukan sekaligus dengan diav sebuah pulsa logika 1 pada E Clock.



Gambar 6
Timing Diagram Pembacaan Register Perintah Mode 4 bit Interface

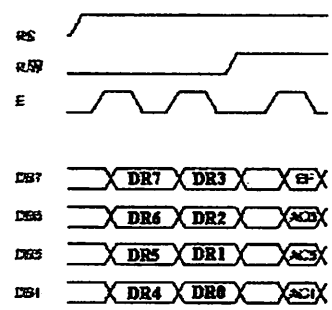
Register Data

Register ini adalah register di mana mikrokontroler dapat menuliskan atau membaca data ke dari DDRAM. Penulisan data pada register ini akan menempatkan data tersebut ke DDRAM sesuai den alamat yang telah diatur sebelumnya

Penulisan Data ke Register Data

Penulisan data pada Register Data dilakukan untuk mengirimkan data yang akan ditampilkan pa LCD. Proses diawali dengan adanya logika 1 pada RS yang menunjukkan akses ke Register Data, kondisi R/W diatur pada logika 0 yang menunjukkan proses penulisan data. Data 4 bit nibble tinggi (bit 7 hingga

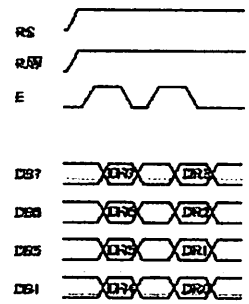
bit 4) dikirim dengan diawali pulsa logika 1 pada sinyal E Clock dan kemudian diikuti 4 bit nibble rendah (bit 3 hingga bit 0) yang juga diawali pulsa logika 1 pada sinyal E Clock.



Gambar 7
Timing Diagram Penulisan Data ke Register Data Mode 4 bit Interface

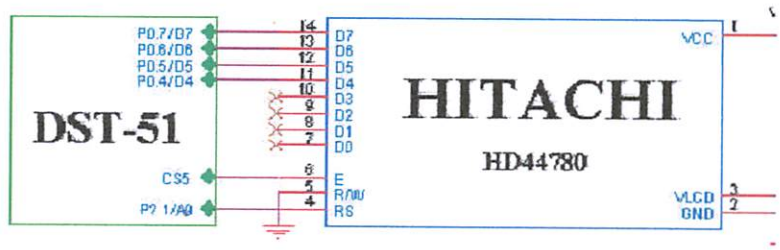
Pembacaan Data dari Register Data

Pembacaan data dari Register Data dilakukan untuk membaca kembali data yang tampil p LCD. Proses dilakukan dengan mengatur RS pada logika 1 yang menunjukkan adanya akses ke Regi Data. Kondisi R/W diatur pada logika tinggi yang menunjukkan adanya proses pembacaan data. Data 4 nibble tinggi (bit 7 hingga bit 4) dibaca dengan diawali adanya pulsa logika 1 pada E Clock dan dilanjut dengan data 4 bit nibble rendah (bit 3 hingga bit 0) yang juga diawali dengan pulsa logika 1 pada E Clock

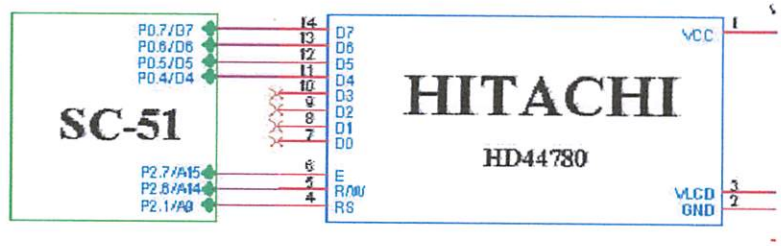


Gambar 8
Timing Diagram Pembacaan Data dari Register Data Mode 4 bit Interface

Antar muka LCD dengan mikrokontroler



Gambar 9
Antar muka dengan Modul DST-51



Gambar 10
Antar Muka dengan Modul SC-51 atau AT8951

Program
Rutin-rutin Program untuk DST-51 yang diassembly dengan ALDS atau ASM51
Rutin-rutin Program untuk SC-51/AT8951 yang diassembly dengan ALDS atau ASM51
Rutin delay yang diassembly dengan ALDS atau ASM51
Datasheet HD44780

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC590AP, TC74HC590AF

8-BIT BINARY COUNTER/REGISTER WITH 3-STATE OUTPUTS

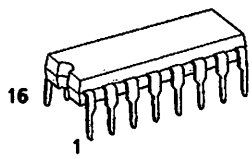
The TC74HC590A is a high speed CMOS 8-BIT COUNTER/REGISTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal counter counts on the positive going edge of Counter Clock (CCK) when Counter Clock Enable ($\overline{CCKEN}$) is low. When Counter Clear ($\overline{CCLR}$) is low, the internal counter is cleared asynchronously to the clock.

Data in the internal counter are loaded into the register at positive going edge of Register Clock (RCK), and the register outputs are countrolled by enable input ($\overline{G}$).

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



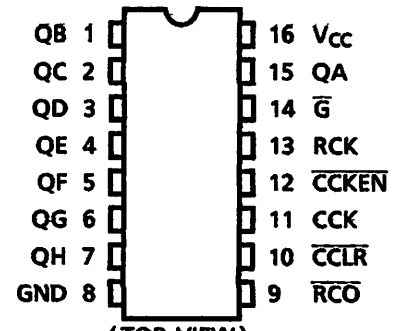
P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

FEATURES:

- High Speed ..... f_{MAX} = 62MHz(typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ..... $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability ..... 15 LSTTL Loads For QA~QH
  10 LSTTL Loads For $\overline{RCO}$
- Symmetrical Output Impedance ···
  $|I_{OH}| = I_{OL}$ = 6mA(Min.) For QA~QH
  $|I_{OH}| = I_{OL}$ = 4mA(Min.) For $\overline{RCO}$
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· VCC (opr.) = 2V~6V
- Pin and Function Compatible with 74LS590

PIN ASSIGNMENT



TRUTH TABLE

INPUT					FUNCTION
G	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
H	X	X	X	X	Q OUTPUTS DISABLE
L	X	X	X	X	Q OUTPUTS ENABLE
X	↑	X	X	X	COUNTER DATA IS STORED INTO REGISTER
X	↓	X	X	X	REGISTER STATE IS NOT CHANGED
X	X	L	X	X	COUNTER CLEAR
X	X	H	L	↑	ADVANCE ONE COUNT
X	X	H	L	↓	NO COUNT
X	X	H	H	X	NO COUNT

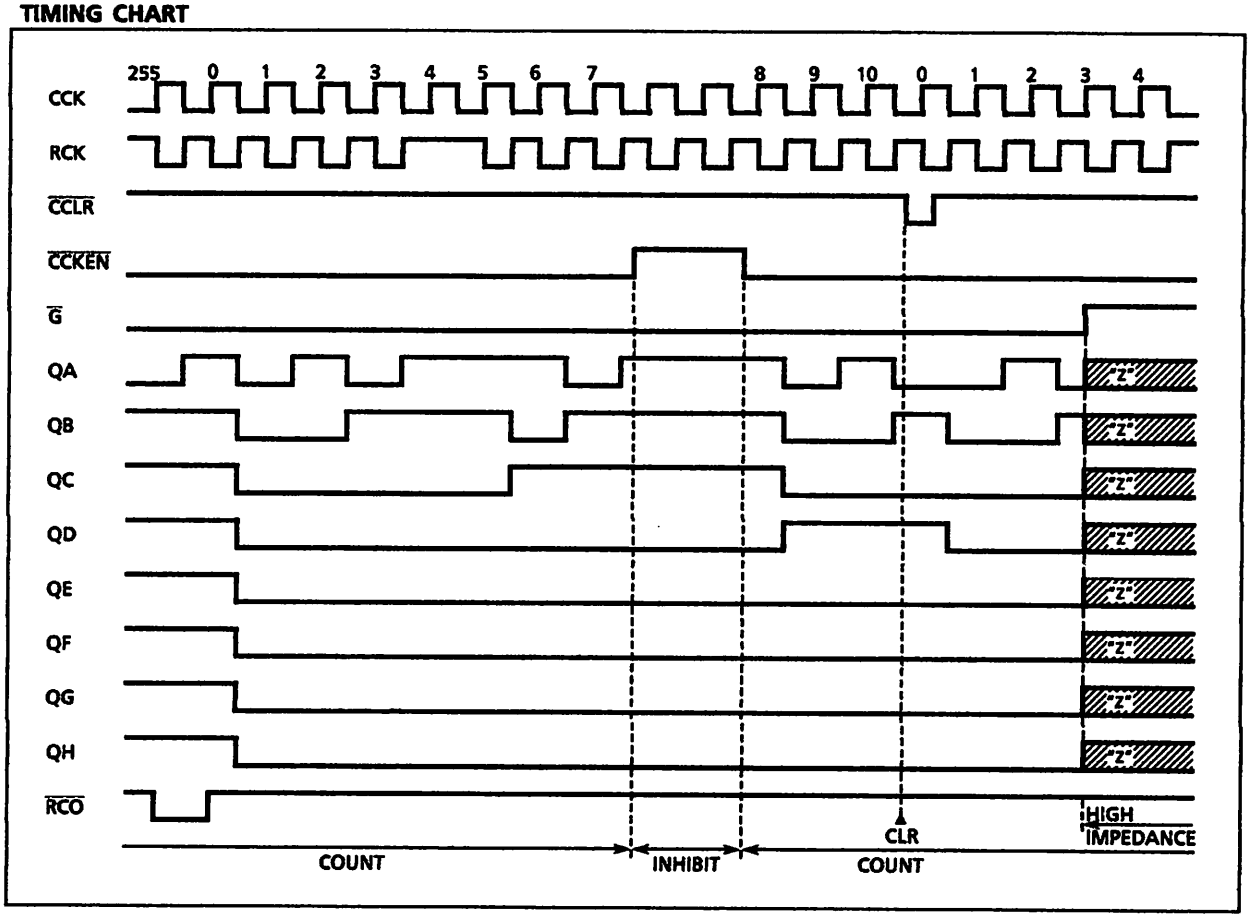
X : Don't care

$\overline{RCO} = \overline{QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'}$

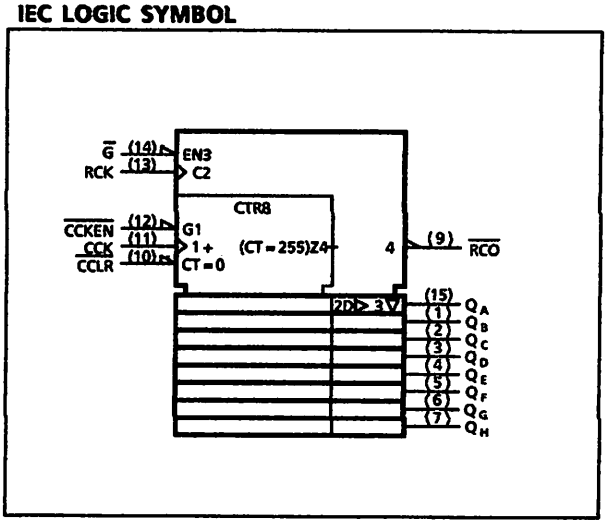
(QA'~QH' : Internal outputs of the counter)

980508E8A2

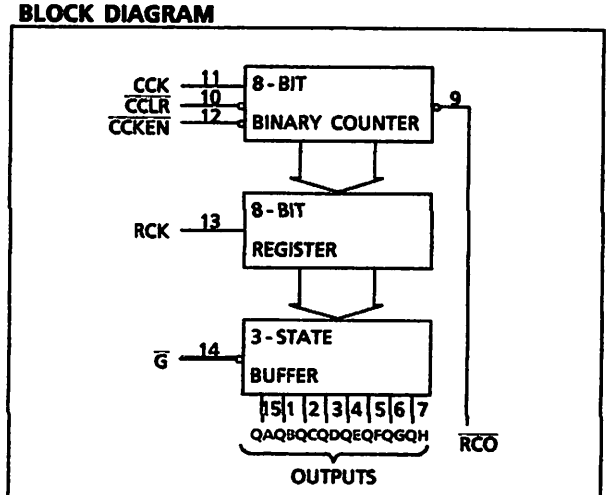
TIMING CHART



IEC LOGIC SYMBOL

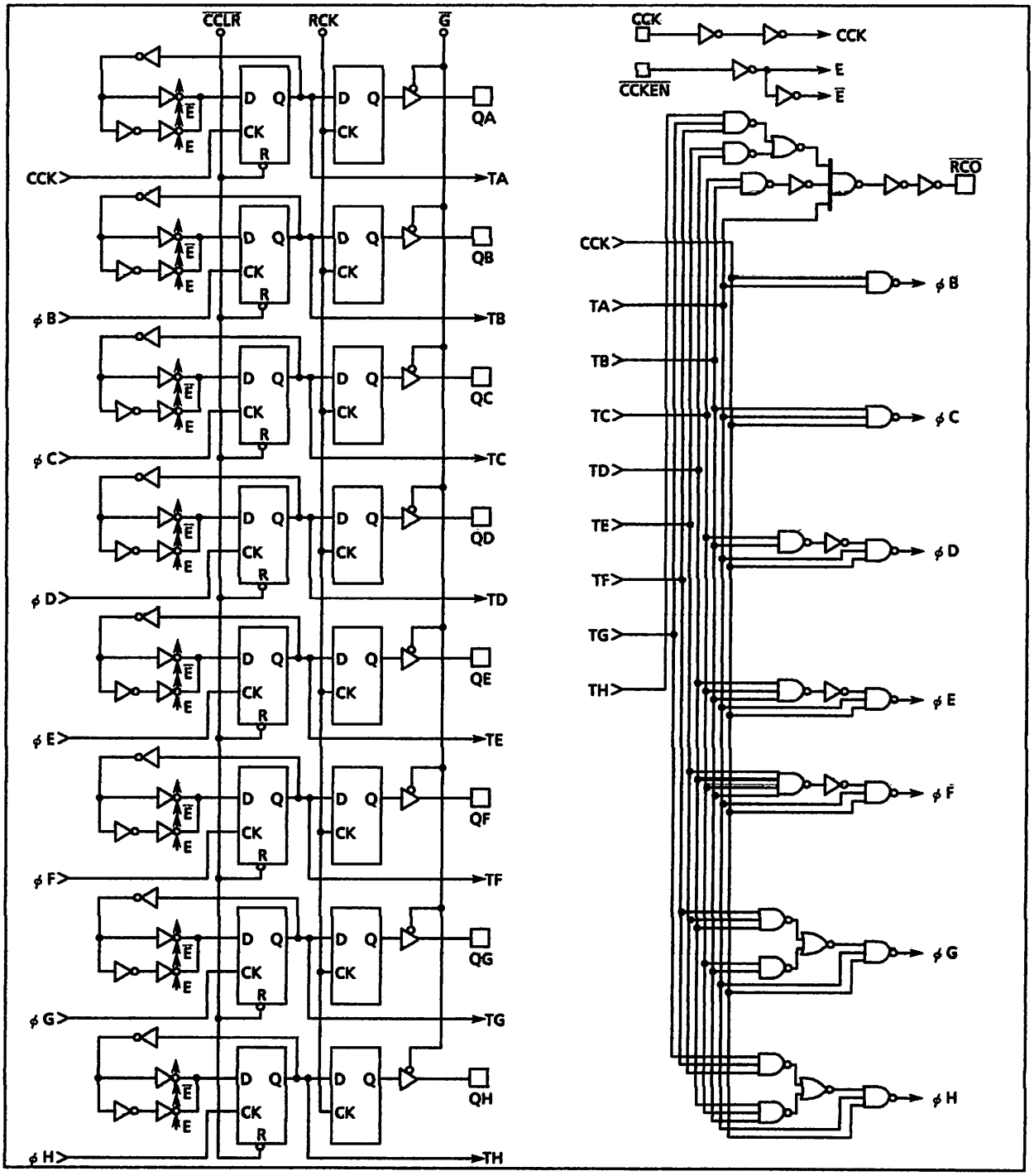


BLOCK DIAGRAM



980508EBA2'

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current ($\overline{RCO}$) (Q_A~Q_H)	I_{OUT}	±25 ±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta= −40°C~65°C. From Ta=65°C to 85 °C a derating factor of −10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0~ 500 (V_{CC}=4.5V) 0~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}				2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}				2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}		I_{OH} = −20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
			$\overline{RCO}$	I_{OH} = −4 mA I_{OH} = −5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	—	4.13 5.63	—	
			QA~QH	I_{OH} = −6 mA I_{OH} = −7.8mA	4.5 6.0	4.18 5.68	4.31 5.80	—	4.13 5.63	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}		I_{OL} = 20μA	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			$\overline{RCO}$	I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
			QA~QH	I_{OL} = 6 mA I_{OL} = 7.8mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND			6.0	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND			6.0	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND			6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYP.	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width (CCK, RCK)	$t_{W(H)}$ $t_{W(L)}$		2.0 4.5 6.0	— — —	75 15 13	95 19 16	ns
Minimum Pulse Width ($\overline{CCLR}$)	$t_{W(L)}$		2.0 4.5 6.0	— — —	75 15 13	95 19 16	
Minimum Set−up Time ($\overline{CCKEN}$−CCK)	t_s		2.0 4.5 6.0	— — —	100 20 17	125 25 21	
Minimum Set−up Time (CCK−$\overline{RCK}$)	t_s		2.0 4.5 6.0	— — —	200 40 34	250 50 43	
Minimum Hold Time	t_h		2.0 4.5 6.0	— — —	0 0 0	0 0 0	
Minimum Removal Time ($\overline{CCLR}$)	t_{rem}		2.0 4.5 6.0	— — —	75 15 13	95 19 16	
Clock Frequency	f		2.0 4.5 6.0	— — —	6 33 39	5 26 31	MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (CCK−$\overline{RCO}$)	t_{pLH} t_{pHL}		—	18	28	
Propagation Delay Time ($\overline{CCLR}$−$\overline{RCO}$)	t_{pLH}		—	20	30	
Maximum Clock Frequency	f_{MAX}		32	62	—	MHz

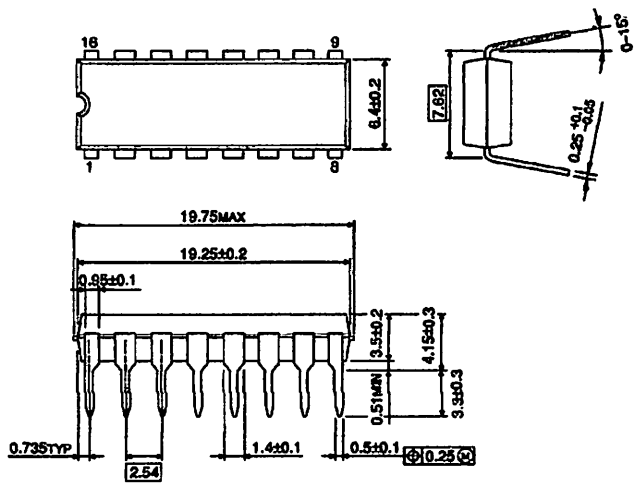
AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Output Transition Time (Qn)	t_{TLH} t_{THL}		50	2.0	—	25	60	—	75	ns
				4.5	—	7	12	—	15	
				6.0	—	6	10	—	13	
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		50	2.0	—	30	75	—	95	
				4.5	—	8	15	—	19	
				6.0	—	7	13	—	16	
Propagation Delay Time (CCK−$\overline{RCO}$)	t_{pLH} t_{pHL}		50	2.0	—	75	163	—	205	
				4.5	—	22	33	—	41	
				6.0	—	17	28	—	35	
Propagation Delay Time ($\overline{CCLR}$−$\overline{RCO}$)	t_{pLH}		50	2.0	—	78	175	—	220	
				4.5	—	23	35	—	44	
				6.0	—	18	30	—	37	
Propagation Delay Time (RCK−Qn)	t_{pLH} t_{pHL}		50	2.0	—	62	145	—	180	
				4.5	—	19	29	—	36	
				6.0	—	15	25	—	31	
			150	2.0	—	78	185	—	230	
				4.5	—	24	37	—	46	
				6.0	—	19	31	—	39	
Output Enable time	t_{pZL} t_{pZH}	R_L = 1kΩ	50	2.0	—	43	105	—	130	
				4.5	—	14	21	—	26	
				6.0	—	12	18	—	22	
			150	2.0	—	58	150	—	190	
				4.5	—	19	30	—	38	
				6.0	—	16	26	—	33	
Output Disable time	t_{pLZ} t_{pHZ}	R_L = 1kΩ	50	2.0	—	33	105	—	130	
				4.5	—	16	21	—	26	
				6.0	—	12	18	—	22	
Maximum Clock Frequency	f_{MAX}		50	2.0	6	12	—	5	—	MHz
				4.5	30	51	—	24	—	
				6.0	35	80	—	28	—	
Input Capacitance	C_{IN}				—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} (1)				—	34	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

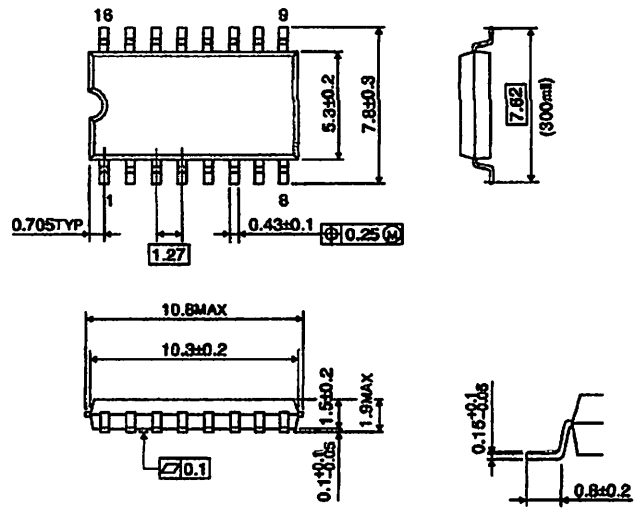
$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm

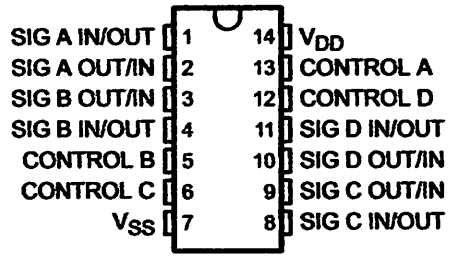


Weight : 0.18g (Typ.)

SCHS051D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

- 15-V Digital or ±7.5-V Peak-to-Peak Switching
- 125-Ω Typical On-State Resistance for 15-V Operation
- Switch On-State Resistance Matched to Within 5 Ω Over 15-V Signal-Input Range
- On-State Resistance Flat Over Full Peak-to-Peak Signal Range
- High On/Off Output-Voltage Ratio: 80 dB Typical at f_{is} = 10 kHz, R_L = 1 kΩ
- High Degree of Linearity: <0.5% Distortion Typical at f_{is} = 1 kHz, V_{is} = 5 V p-p, $V_{DD} - V_{SS} \geq 10$ V, R_L = 10 kΩ
- Extremely Low Off-State Switch Leakage, Resulting in Very Low Offset Current and High Effective Off-State Resistance: 10 pA Typical at $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C
- Extremely High Control Input Impedance (Control Circuit Isolated From Signal Circuit): 10^{12} Ω Typical
- Low Crosstalk Between Switches: –50 dB Typical at f_{is} = 8 MHz, R_L = 1 kΩ
- Matched Control-Input to Signal-Output Capacitance: Reduces Output Signal Transients
- Frequency Response, Switch On = 40 MHz Typical
- 100% Tested for Quiescent Current at 20 V
- 5-V, 10-V, and 15-V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13-B, *Standard Specifications for Description of "B" Series CMOS Devices*
- Applications:
  - Analog Signal Switching/Multiplexing: Signal Gating, Modulator, Squelch Control, Demodulator, Chopper, Commutating Switch
  - Digital Signal Switching/Multiplexing
  - Transmission-Gate Logic Implementation
  - Analog-to-Digital and Digital-to-Analog Conversion
  - Digital Control of Frequency, Impedance, Phase, and Analog-Signal Gain

E, F, M, NS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full signal-input range.

The CD4066B consists of four bilateral switches, each with independent controls. Both the p and the n devices in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 1, the well of the n-channel device on each switch is tied to either the input (when the switch is on) or to V_{SS} (when the switch is off). This configuration eliminates the variation of the switch-transistor threshold voltage with input signal and, thus, keeps the on-state resistance low over the full operating-signal range.

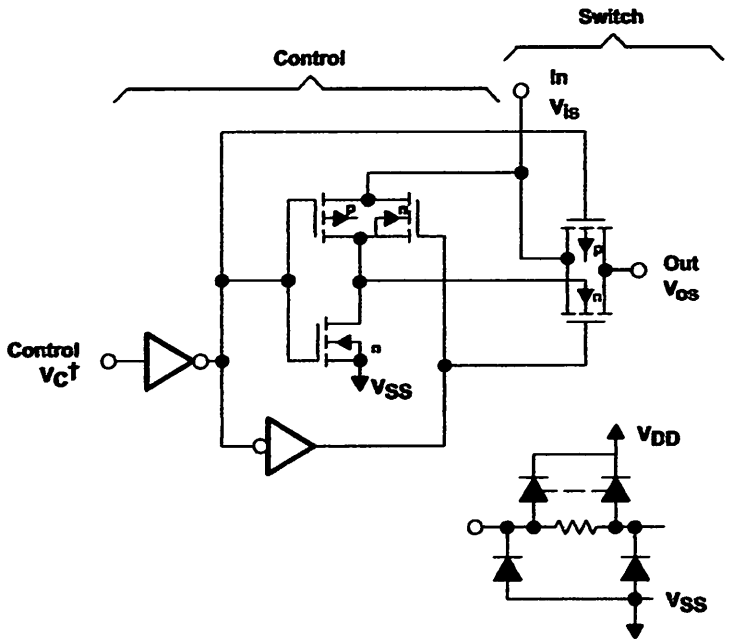
The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage and more constant on-state impedance over the input-signal range. However, for sample-and-hold applications, the CD4016B is recommended.

escription/ordering information (continued)

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP – F	Tube of 25	CD4066BF3A	CD4066BF3A
	PDIP – E	Tube of 25	CD4066BE	CD4066BE
	SOIC – M	Tube of 50	CD4066BM	CD4066BM
		Reel of 2500	CD4066BM96	
		Reel of 250	CD4066BMT	
	SOP – NS	Reel of 2000	CD4066BNSR	CD4066B
	TSSOP – PW	Tube of 90	CD4066BPW	CM066B
		Reel of 2000	CD4066BPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



† All control inputs are protected by the CMOS protection network.

NOTES: A. All p substrates are connected to V_{DD}.
B. Normal operation control-line biasing: switch on (logic 1), $V_C = V_{DD}$; switch off (logic 0), $V_C = V_{SS}$
C. Signal-level range: $V_{SS} \le V_{IS} \le V_{DD}$

92CS-29113

Figure 1. Schematic Diagram of One-of-Four Identical Switches and Associated Control Circuitry

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

DC supply-voltage range, V_{DD} (voltages referenced to V_{SS} terminal) ..... –0.5 V to 20 V
Input voltage range, V_{is} (all inputs) ..... –0.5 V to V_{DD} + 0.5 V
DC input current, I_{IN} (any one input) ..... ±10 mA
Package thermal impedance, θ_{JA} (see Note 1): E package ..... 80°C/W
M package ..... 86°C/W
NS package ..... 76°C/W
PW package ..... 113°C/W
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max ..... 265°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	3	18	V
T_A	Operating free-air temperature	–55	125	°C

lectrical characteristics

PARAMETER		TEST CONDITIONS	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES						UNIT
					–55°C	–40°C	85°C	125°C	25°C TYP	25°C MAX	
I_{DD}	Quiescent device current		0, 5	5	0.25	0.25	7.5	7.5	0.01	0.25	µA
			0, 10	10	0.5	0.5	15	15	0.01	0.5	
			0, 15	15	1	1	30	30	0.01	1	
			0, 20	20	5	5	150	150	0.02	5	
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
r_{on}	On-state resistance (max)	$V_C = V_{DD}$, R_L = 10 kΩ returned to $\frac{(V_{DD} - V_{SS})}{2}$, $V_{IS} = V_{SS}$ to V_{DD}		5	800	850	1200	1300	470	1050	Ω
				10	310	330	500	550	180	400	
				15	200	210	300	320	125	240	
Δr_{on}	On-state resistance difference between any two switches	R_L = 10 kΩ, $V_C = V_{DD}$		5					15		Ω
				10					10		
				15					5		
THD	Total harmonic distortion	$V_C = V_{DD}$ = 5 V, V_{SS} = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 10 kΩ, f_{is} = 1-kHz sine wave							0.4		%
	–3-dB cutoff frequency (switch on)	$V_C = V_{DD}$ = 5 V, V_{SS} = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 1 kΩ							40		MHz
	–50-dB feedthrough frequency (switch off)	$V_C = V_{SS}$ = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 1 kΩ							1		MHz
I_{is}	Input/output leakage current (switch off) (max)	V_C = 0 V, V_{is} = 18 V, V_{os} = 0 V; and V_C = 0 V, V_{is} = 0 V, V_{os} = 18 V		18	±0.1	±0.1	±1	±1	$\pm 10^{-5}$	±0.1	µA
	–50-dB crosstalk frequency	$V_C(A) = V_{DD}$ = 5 V, $V_C(B) = V_{SS}$ = –5 V, $V_{is}(A)$ = 5 V_{p-p}, 50-Ω source, R_L = 1 kΩ							8		MHz
t_{pd}	Propagation delay (signal input to signal output)	R_L = 200 kΩ, $V_C = V_{DD}$, V_{SS} = GND, C_L = 50 pF, V_{is} = 10 V (square wave centered on 5 V), t_r, t_f = 20 ns		5					20	40	ns
				10					10	20	
				15					7	15	
C_{is}	Input capacitance	V_{DD} = 5 V, $V_C = V_{SS}$ = –5 V							8		pF
C_{os}	Output capacitance	V_{DD} = 5 V, $V_C = V_{SS}$ = –5 V							8		pF
C_{ios}	Feedthrough	V_{DD} = 5 V, $V_C = V_{SS}$ = –5 V							0.5		pF

electrical characteristics (continued)

CHARACTERISTIC		TEST CONDITIONS	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES						UNIT
				–55°C	–40°C	85°C	125°C	25°C TYP	25°C MAX	
Control (V_C)										
V_{ILC}	Control input, low voltage (max)	$\|I_{is}\| < 10\ \mu A$, $V_{is} = V_{SS}$, $V_{OS} = V_{DD}$, and $V_{is} = V_{DD}$, $V_{OS} = V_{SS}$	5	1	1	1	1		1	V
			10	2	2	2	2		2	
			15	2	2	2	2		2	
V_{IHC}	Control input, high voltage	See Figure 6	5	3.5 (MIN)						V
			10	7 (MIN)						
			15	11 (MIN)						
I_{IN}	Input current (max)	$V_{is} \le V_{DD}$, $V_{DD} - V_{SS} = 18$ V, $V_{CC} \le V_{DD} - V_{SS}$	18	±0.1	±0.1	±1	±1	$\pm 10^{-5}$	±0.1	µA
	Crosstalk (control input to signal output)	$V_C = 10$ V (square wave), t_r, $t_f = 20$ ns, $R_L = 10$ kΩ	10					50		mV
	Turn-on and turn-off propagation delay	$V_{IN} = V_{DD}$, t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 1$ kΩ	5					35	70	ns
			10					20	40	
			15					15	30	
	Maximum control input repetition rate	$V_{is} = V_{DD}$, V_{SS} = GND, $R_L = 1$ kΩ to GND, $C_L = 50$ pF, $V_C = 10$ V (square wave centered on 5 V), t_r, $t_f = 20$ ns, $V_{OS} = 1/2\ V_{OS}$ at 1 kHz	5					6		MHz
			10					9		
			15					9.5		
C_I	Input capacitance							5	7.5	pF

switching characteristics

V_{DD} (V)	SWITCH INPUT						SWITCH OUTPUT, V_{os} (V)	
	V_{is} (V)	I_{is} (mA)						
		–55°C	–40°C	25°C	85°C	125°C	MIN	MAX
5	0	0.64	0.61	0.51	0.42	0.36		0.4
5	5	–0.64	–0.61	–0.51	–0.42	–0.36	4.6	
10	0	1.6	1.5	1.3	1.1	0.9		0.5
10	10	–1.6	–1.5	–1.3	–1.1	–0.9	9.5	
15	0	4.2	4	3.4	2.8	2.4		1.5
15	15	–4.2	–4	–3.4	–2.8	–2.4	13.5	

TYPICAL CHARACTERISTICS

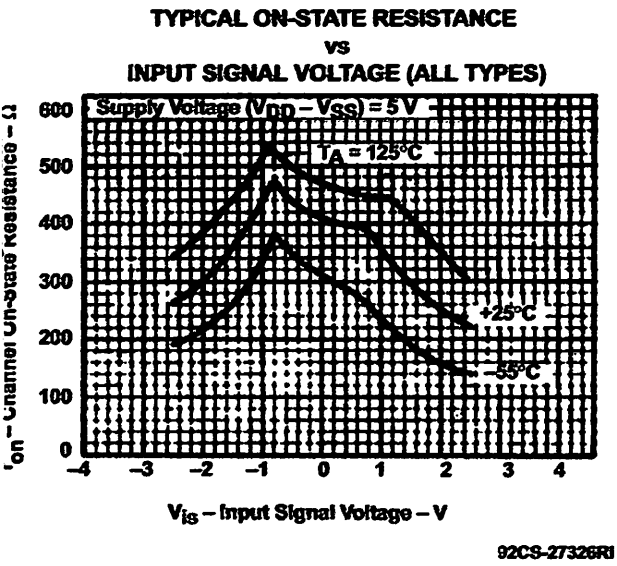


Figure 2

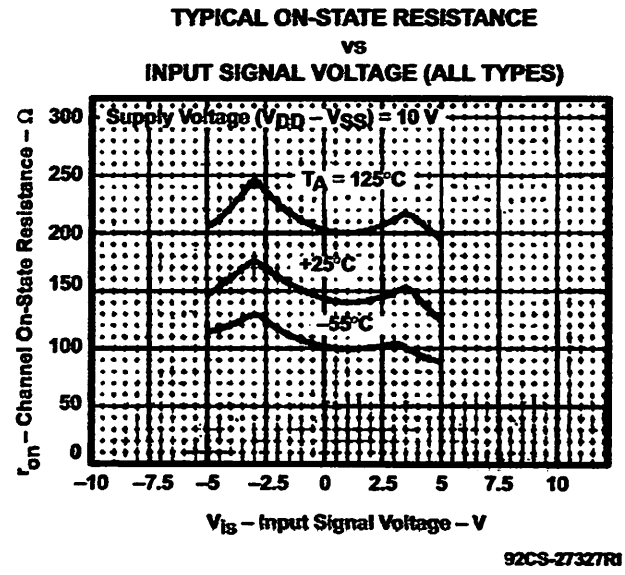


Figure 3

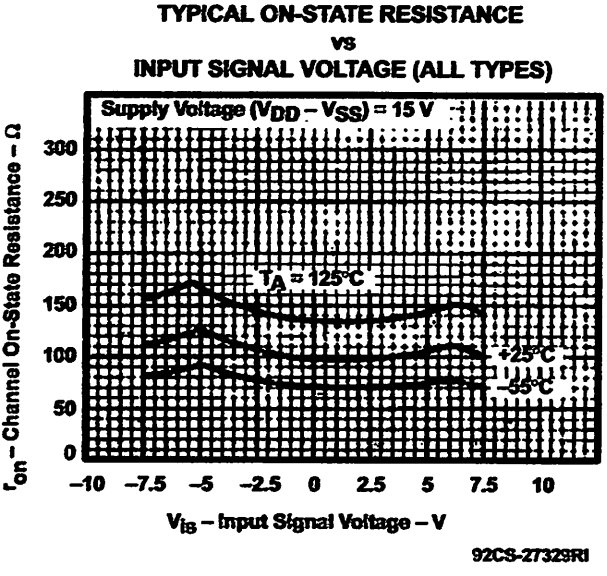


Figure 4

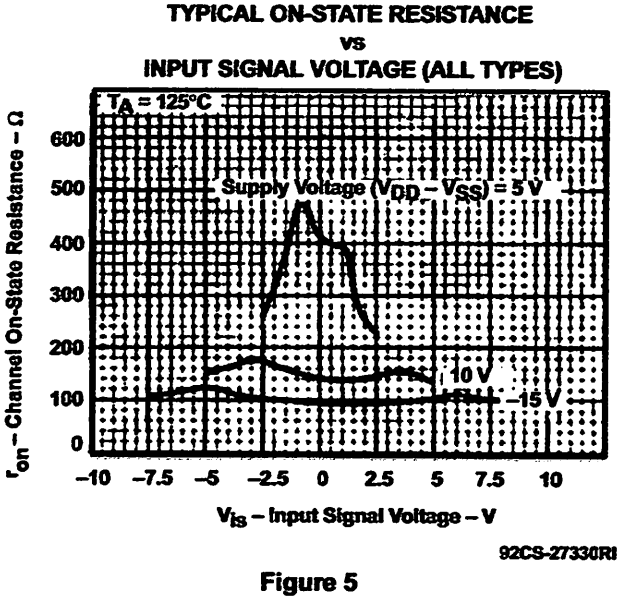
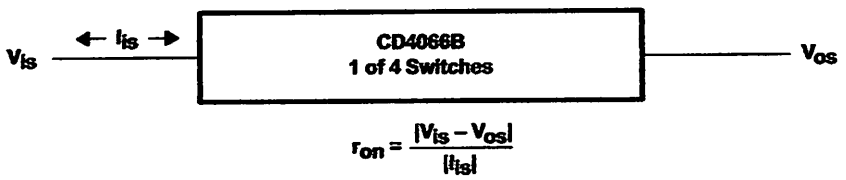


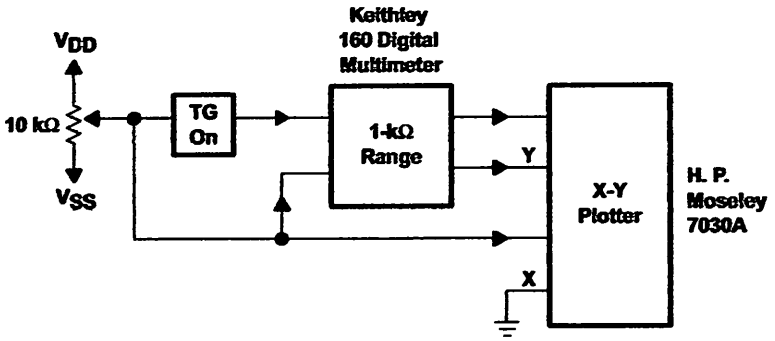
Figure 5

TYPICAL CHARACTERISTICS



92CS-30966

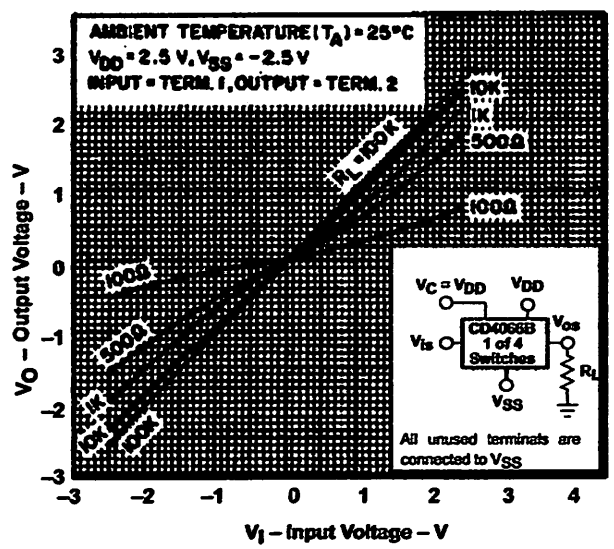
Figure 6. Determination of r_{on} as a Test Condition for Control-Input High-Voltage (V_{IHC}) Specification



92CS-22716

Figure 7. Channel On-State Resistance Measurement Circuit

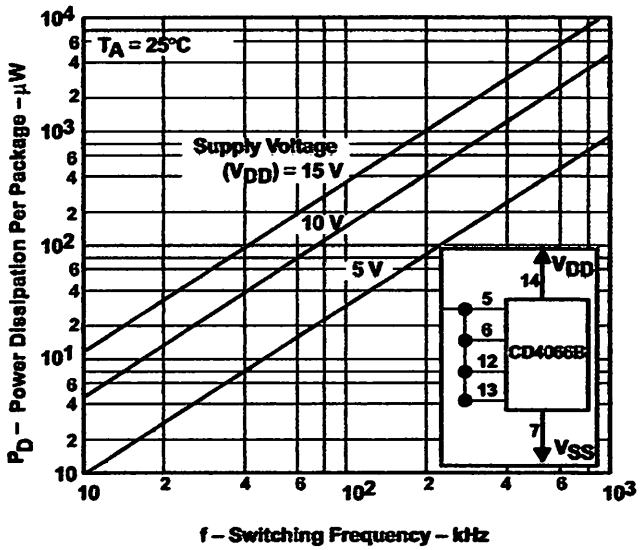
TYPICAL ON CHARACTERISTICS
FOR 1 OF 4 CHANNELS



92CS-30919

Figure 8

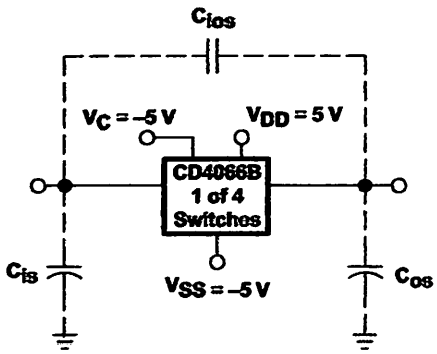
POWER DISSIPATION PER PACKAGE
vs
SWITCHING FREQUENCY



92C-30920

Figure 9

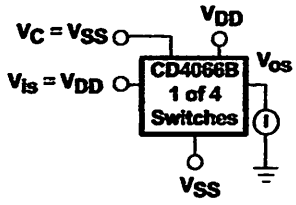
TYPICAL CHARACTERISTICS



92CS-30921

Measured on Boonton capacitance bridge, model 75a (1 MHz); test-fixture capacitance nulled out.

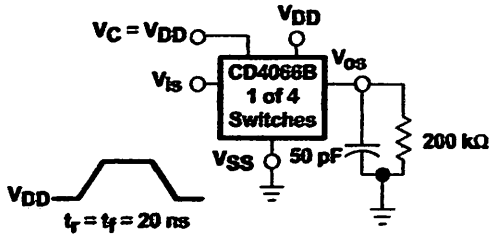
Figure 10. Typical On Characteristics for One of Four Channels



92CS-30922

All unused terminals are connected to V_{SS}.

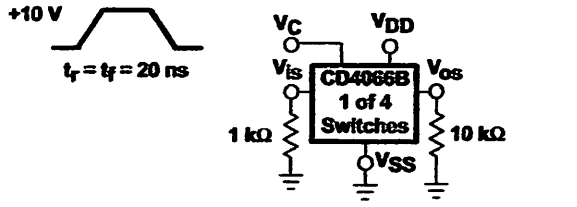
Figure 11. Off-Switch Input or Output Leakage



92CS-30923

All unused terminals are connected to V_{SS}.

Figure 12. Propagation Delay Time Signal Input (V_{is}) to Signal Output (V_{os})

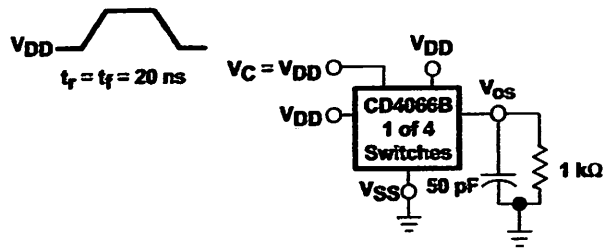


92CS-30924

All unused terminals are connected to V_{SS}.

Figure 13. Crosstalk-Control Input to Signal Output

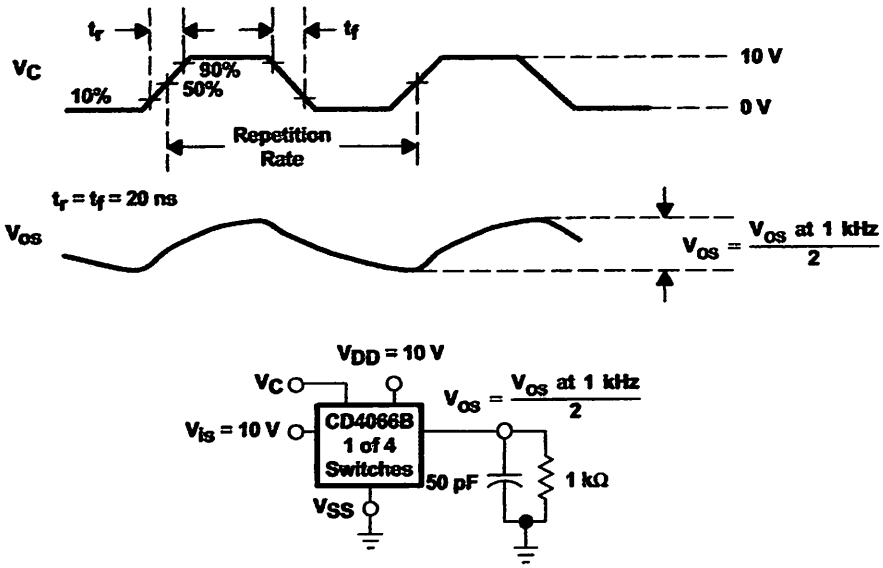
TYPICAL CHARACTERISTICS



92CS-30925

NOTES: A. All unused terminals are connected to V_{SS}.
B. Delay is measured at V_{OS} level of +10% from ground (turn-on) or on-state output level (turn-off).

Figure 14. Propagation Delay, t_{PLH}, t_{PHL} Control-Signal Output

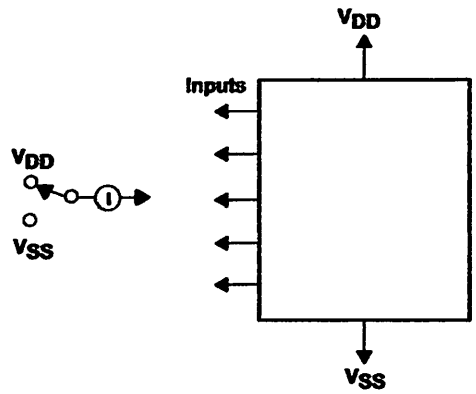


All unused terminals are connected to V_{SS}.

92CS-30925

Figure 15. Maximum Allowable Control-Input Repetition Rate

TYPICAL CHARACTERISTICS



Measure inputs sequentially to both V_{DD} and V_{SS}. Connect all unused inputs to either V_{DD} or V_{SS}. Measure control inputs only.

Figure 16. Input Leakage-Current Test Circuit

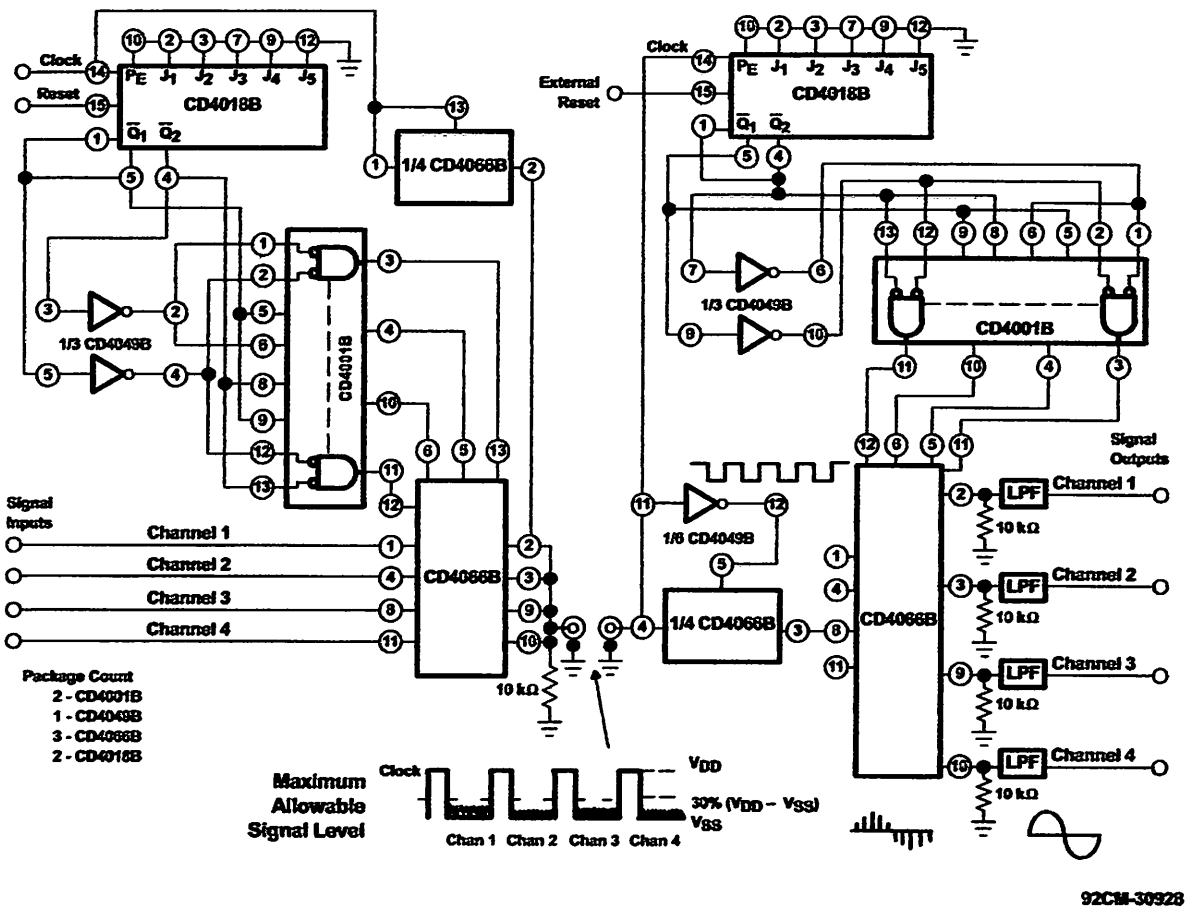
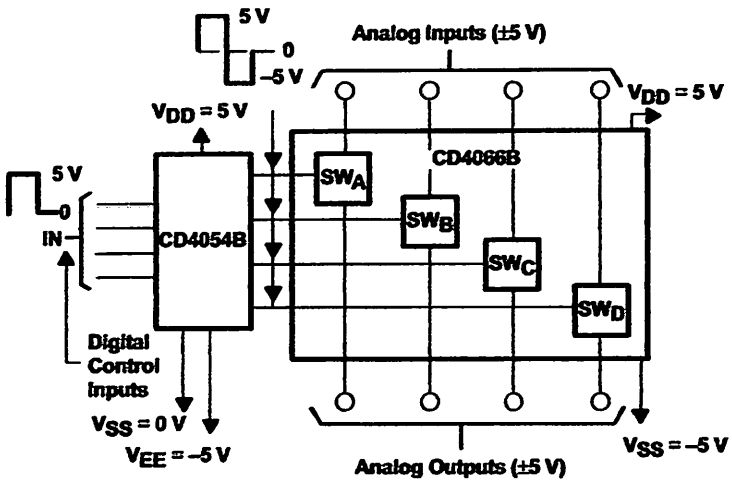


Figure 17. Four-Channel PAM Multiplex System Diagram

TYPICAL CHARACTERISTICS



92CS-30927

Figure 18. Bidirectional Signal Transmission Via Digital Control Logic

APPLICATION INFORMATION

In applications that employ separate power sources to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4066B.

In certain applications, the external load-resistor current can include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 V (calculated from r_{on} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD4066BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4066BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4066BF	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
CD4066BF3A	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
CD4066BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
JM38510/05852BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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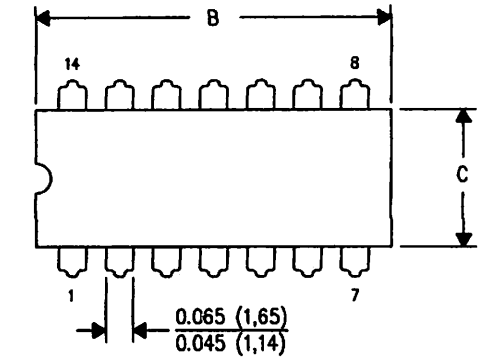
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

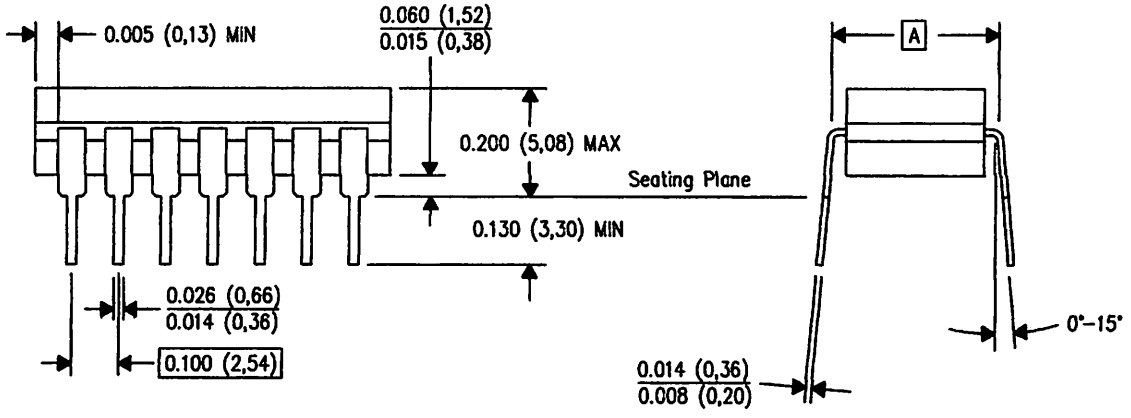
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



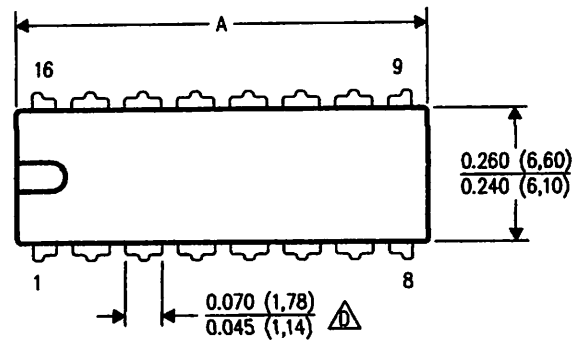
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**)

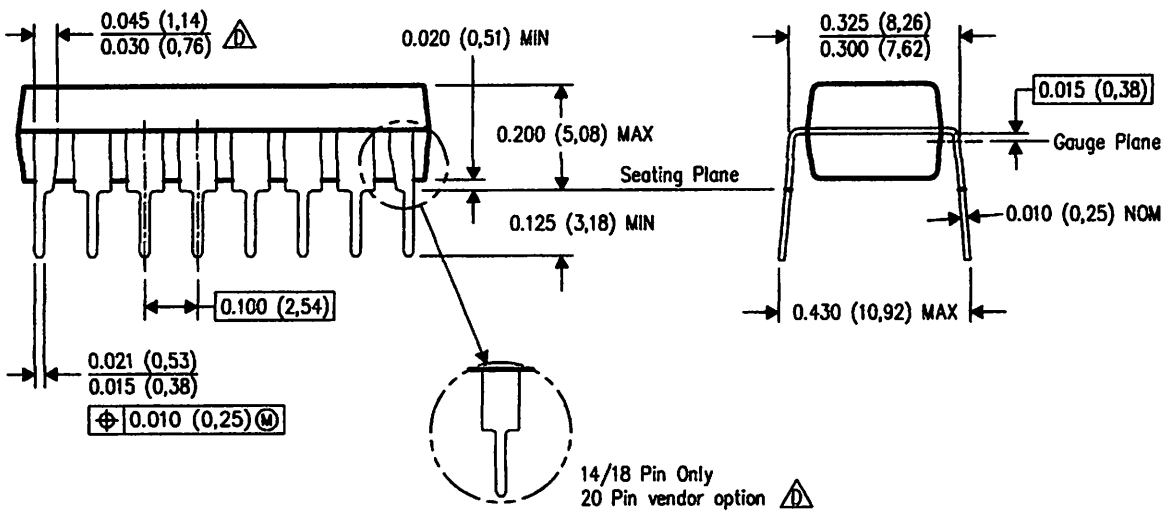
PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

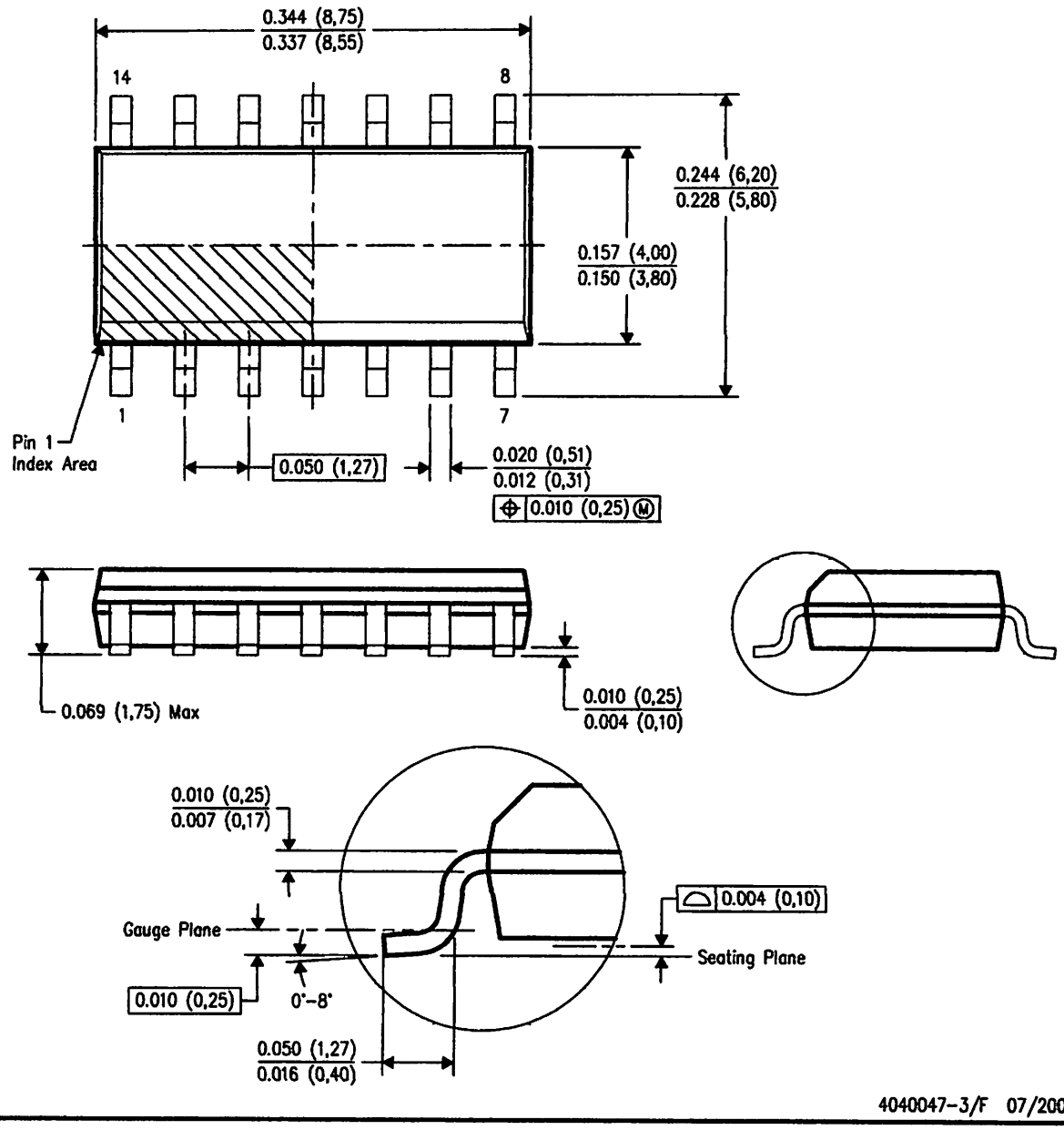
C



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE

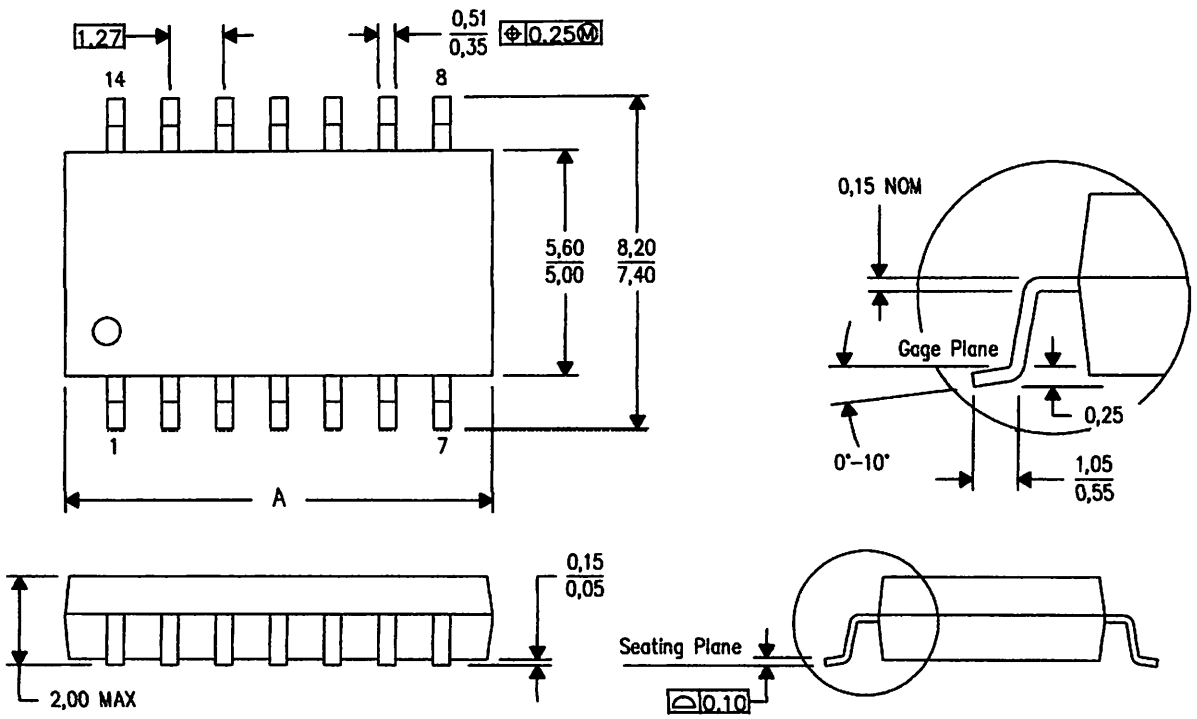


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



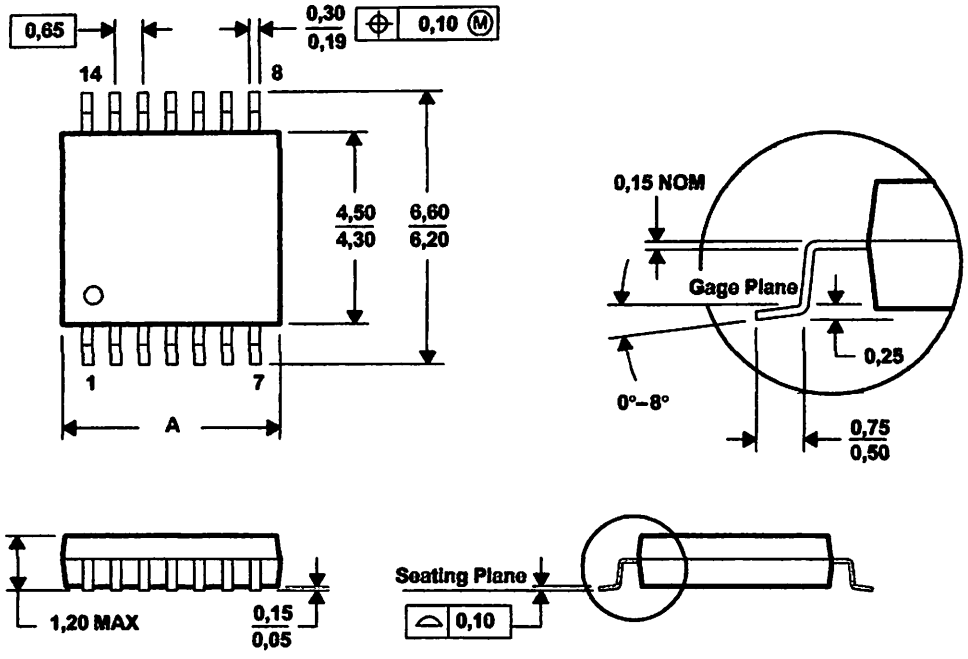
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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