

**SMART METER MENGGUNAKAN IC ADE7753 DENGAN
KONEKSI WIRELESS UNTUK PENGUKUR DAYA LISTRIK
PADA SISTEM SMART GRID**

SKRIPSI



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PERPUSTAKAAN
ITN MALANG

**PROGRAM STUDI TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
2015**

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THE NATIONAL ACADEMY OF SCIENCES
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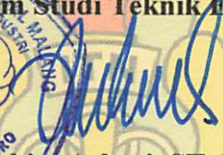
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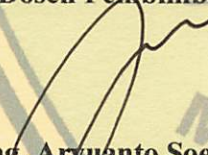
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ABSTRAK

Smart Grid adalah suatu jaringan cerdas yang diharapkan dapat memenuhi kebutuhan energi listrik. Pada teknologi *smart grid* memungkinkan untuk memonitoring dan controlling dengan komunikasi dua arah, yang digunakan untuk menghemat atau efisiensi penggunaan tenaga listrik. Sistem *smart grid* memerlukan *Smart meter* sebagai pengambilan data daya listrik untuk dikirim ke pusat kendali.

Smart meter merupakan komponen yang paling penting sebagai *monitoring* dan *control* daya. Pada *smart meter* terdapat IC ADE7753 berfungsi sebagai sensor pengukur daya. IC ADE7753 juga membutuhkan input arus dan tegangan untuk input arus menggunakan trafo arus CST-1020 dengan rasio 1000:1 dan untuk input tegangan menggunakan rangkaian pembagi tegangan. Menggunakan modul Xbee sebagai transfer data antara smart meter dengan pc. Sistem pengontrol beban menggunakan modul driver relay. Pada alat ini juga tertanam mikrokontroler arduino mega2560 sebagai pusat pengolah data. Sehingga setiap komponen dapat bekerja sesuai fungsi masing-masing.

Dari hasil pengukuran dan pengujian hasil sistem monitoring di dapat error sebesar 1,1% pada sensor tegangan, 1,8% error pada sensor arus, 2,2% error pada daya aktif, 4,9% error pada daya reaktif, dan untuk cosphi error sebesar 1,7%. Sedangkan untuk tampilan *monitoring* dan *control* menggunakan *software* delphi.

Kata kunci : *Smart meter, Monitoring daya, ADE7753*

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Malang, 24 Agustus 2015

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BAB 1

PENDAHULUAN

1.1 Latar Belakang

Smart Grid adalah suatu jaringan cerdas yang diharapkan dapat memenuhi kebutuhan energi listrik. Dimana komunikasi terjadi dua arah antara produsen listrik serta konsumennya telah diimplementasikan menggunakan teknologi analog bertahun-tahun lamanya dan merupakan teknologi yang menggabungkan bidang informasi, komunikasi dan tenaga listrik yang bertujuan untuk menghemat atau efisiensi penggunaan tenaga listrik. Pada teknologi *smart grid* memungkinkan untuk memonitoring dan *controlling* dengan komunikasi dua arah yang menggunakan jaringan *wireless* sebagai teknologi komunikasi dan juga berfungsi sebagai manajemen pemakaian daya listrik secara praktis dan efisien. Pada suatu sistem *smart grid*, *smart meter* merupakan komponen yang paling penting sebagai monitoring dan *control* daya. Smart meter juga berperan sebagai monitoring pemakaian daya listrik. *Smart meter* menggunakan jaringan komunikasi *wireless* ke pusat kendali untuk *monitoring* dan *control*. Pada sistem *smart grid* terdapat pusat *control* yang berfungsi untuk monitoring dan mengontrol pemakaian daya listrik.

Dalam penelitian ini rangkaian smart meter menggunakan ic *ade7753* yang memberikan informasi tentang daya, arus dan tegangan dengan komunikasi SPI. Arduino digunakan untuk antar muka antara smart meter dengan personal computer yang berguna sebagai monitoring dan controlling daya listrik. Modul Xbee berfungsi sebagai komunikasi antara PC dengan *Smart Meter*, yang menggunakan jaringan *wireless*. Diharapkan pada penelitian ini pemakaian daya listrik dapat di monitoring dan controlling secara otomatis dengan jaringan *wireless* untuk efisiensi pemakaian daya listrik.

1.2 Rumusan Masalah

Mengacu pada permasalahan diatas yang diuraikan pada skripsi ini, maka dapat dirumuskan masalah sebagai berikut:

1. Bagaimana membuat pengukur daya listrik menggunakan ade7753?
2. Bagaimana menggunakan komunikasi dua arah untuk system control dan monitoring, antara pc dengan arduino menggunakan wireless?

1.3 Tujuan

Adapun tujuan dari penulisan skripsi ini adalah:

Tujuan dari penelitian ini adalah membuat suatu sistem alat yang mampu memonitoring dan *controlling* daya listrik di kwh meter digital secara otomatis dengan menggunakan jaringan wifi untuk efisiensi pemakaian daya listrik .

1.4 Batasan Masalah

Agar tidak terjadi penyimpangan maksud dan tujuan utama penyusunan skripsi ini maka batasan masalah pada skripsi ini antara lain:

1. Tidak membahas secara detail tentang jaringan komunikasi *wireless*.
2. Tidak membahas *topology* jaringan yang digunakan.
3. Menggunakan tegangan kerja 220 /50 hz dengan daya maksimal 500watt
4. Satu modul *smart meter* ini hanya dapat digunakan untuk maksimal daya 500watt.
5. Menggunakan modul Xbee dalam komunikasi *wireless*.
6. Control hanya digunakan sebagai saklar on/off pada aplikasi.

1.5 Metodologi

Metode yang digunakan dalam pembahasan skripsi ini adalah:

1. Studi Literatur

Mencari referensi–referensi yang berhubungan dengan perencanaan dan pembuatan alat yang akan dibuat.

2. Perancangan Alat

Sebelum melaksanakan pembuatan terhadap alat, dilakukan perancangan terhadap alat yang meliputi merancang rangkaian keseluruhan alat, serta penalaran metode yang digunakan.

3. Pembuatan Alat

Pada tahap ini realisasi alat yang dibuat, dilakukan perakitan sistem terhadap seluruh hasil rancangan yang telah dibuat.

4. Pengujian Alat

Untuk mengetahui cara kerja alat, maka dilakukan pengujian secara keseluruhan, dan menganalisa hasil pengujian alat untuk membuat kesimpulan.

1.6 Sistematika Penulisan

Untuk mendapatkan arah yang tepat mengenai hal-hal yang akan dibahas maka dalam skripsi ini disusun sebagai berikut :

BAB I : PENDAHULUAN

Memuat latar belakang, rumusan masalah, tujuan, batasan masalah, metodologi, dan sistematika penulisan.

BAB II : KAJIAN PUSTAKA

Membahas tentang dasar-dasar teori yang menunjang dalam perencanaan dan pembuatan smart grid menggunakan ic ade 7753 dengan menggunakan jaringan wifi

BAB III : PERENCANAAN DAN PEMBUATAN ALAT

Membahas tentang perencanaan dan proses pembuatan meliputi perencanaan, pembuatan alat, cara kerja dan penggunaan alat.

BAB IV : PENGUJIAN DAN ANALISA

Menjelaskan hasil pengujian dan analisa alat dari hasil yang diperoleh.

BAB V : PENUTUP

Menjelaskan kesimpulan dan saran.

BAB II

LANDASAN TEORI

Untuk memudahkan dalam memahami sistem ini, maka diperlukan teori-teori dasar yang menunjang dan dapat dijelaskan tentang karakteristik komponen-komponen yang digunakan maupun masalah yang dibahas sehingga dapat diperkirakan prinsip dan cara kerja secara umum dari sistem ini. Selain itu dengan dasar teori yang ada dapat menambahkan pemahaman yang mendukung dalam perancangan dan pembuatan alat ini.

2.1. Daya listrik

Daya adalah energi yang digunakan untuk melakukan usaha. dalam sistem tenaga listrik, daya merupakan jumlah energi yang digunakan untuk melakukan kerja atau usaha. Daya listrik dinyatakan dalam satuan Watt atau *Horse power* (HP). *Horse power* merupakan satuan daya listrik dimana 1 HP setara 746 Watt atau *lbft/second*. Sedangkan Watt merupakan unit daya listrik dimana 1 Watt memiliki daya setara dengan daya yang dihasilkan oleh perkalian arus 1 Ampere dan tegangan 1 Volt.

Dalam listrik arus bolak balik, daya terbagi menjadi 3 (tiga), yaitu daya aktif (P), daya reaktif (Q), dan daya semu (S).

1. Daya Aktif

Daya Aktif adalah perkalian antara tegangan dengan arus yang sefasa dengan tegangan.

$$P = V.I \cos\phi \dots\dots\dots(2-1)$$

2. Daya Reaktif

Daya Reaktif adalah perkalian antara tegangan dan arus yang berbeda fasa 90° terhadap tegangan.

$$P = V.I \sin\phi \dots\dots\dots(2-2)$$

3. Daya Semu

Daya Semu adalah penjumlahan daya aktif dengan daya reaktif

$S = P + JQ \dots\dots\dots(2-3)$

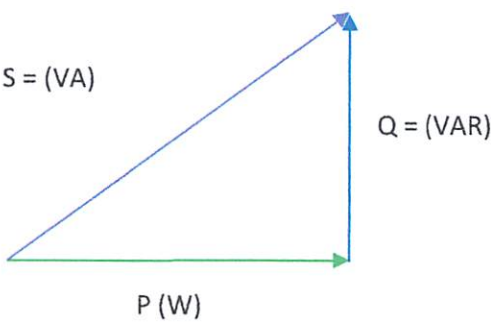
$S = \sqrt{(V.I\sin\varphi)^2 + (V.ICos\varphi)^2} \dots\dots\dots(2-4)$

$S = \sqrt{(V.I)^2(\sin\varphi)^2 + (V.I)^2(Cos\varphi)^2} \dots\dots\dots(2-5)$

$S = \sqrt{(V.I)^2} \dots\dots\dots(2-6)$

$S = V.I \dots\dots\dots(2-7)$

Hubungan antara daya aktif, daya reaktif dan daya semu dapat dilihat pada gambar 2.1.



Gambar 2.1. Segitiga Daya
(Sumber:[http://www.google.com/factor daya](http://www.google.com/factor%20daya))

Faktor daya adalah perbandingan daya aktif dan daya semu.

Faktor Daya = $\frac{\text{Daya Aktif}}{\text{Daya Semu}}$

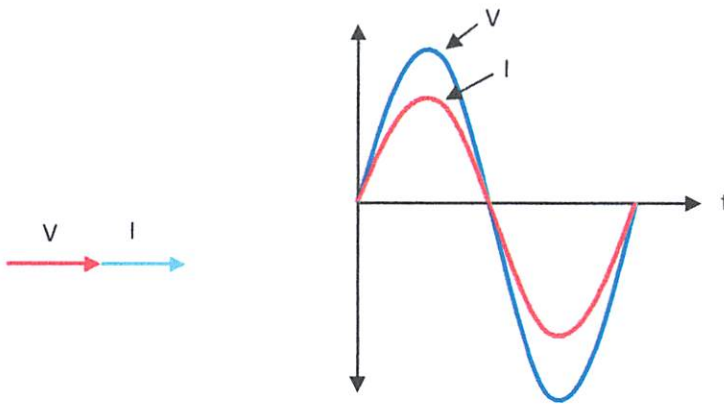
Faktor daya = $\text{Cos}\varphi$

Nilai faktor daya adalah antara 0 sampai 1. semakin besar nilai faktor daya maka besar daya aktif akan semakin mendekati besar daya semu. Untuk daya aktif (P) dan tegangan (V) yang sama, semakin besar nilai faktor daya maka semakin kecil arus (I) yang mengalir di kawat penghantar. Hal ini berarti arus (I) berbanding terbalik dengan faktor daya ($\cos\phi$).

Dalam sistem tenaga listrik dikenal 3 jenis faktor daya yaitu faktor daya sepasa (*unity*), faktor daya terbelakang (*lagging*) dan faktor daya terdahulu (*leading*) yang ditentukan oleh jenis beban yang ada pada sistem.

2.1.1.Faktor Daya Sefasa (*Unity*)

Faktor daya sepasa adalah keadaan dimana tegangan sepasa dengan arus. Nilai faktor dayanya adalah 1. Faktor daya sefasa akan terjadi bila jenis beban adalah resistif murni.



(a). Diagram fasor. (b). Hubungan tegangan dan arus terhadap waktu.

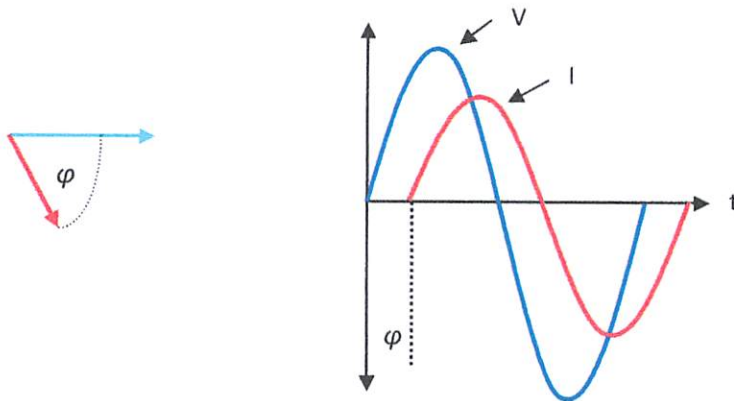
Gambar 2.2. Arus Sefasa dengan Tegangan

(Sumber: [http://www.google.com/faktor daya](http://www.google.com/faktor%20daya))

Pada gambar terlihat bahwa sudut yang dibentuk oleh tegangan dan arus (sudut ϕ) adalah 0° . Nilai $\cos\phi$ adalah 1 sehingga daya aktif sama dengan daya semu.

2.1.2. Faktor Daya Terbelakang (*Lagging*)

Faktor daya terbelakang (*lagging*) adalah keadaan dimana arus tertinggal terhadap tegangan sebesar φ .

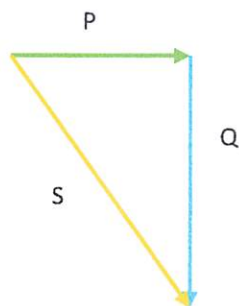


(a). Diagram fasor (b). Hubungan tegangan dan arus terhadap waktu

Gambar 2.3. Arus tertinggal dengan tegangan sebesar φ

(Sumber: <http://www.google.com/factor daya>)

Hubungan antara daya aktif, daya reaktif, dan daya semu pada faktor daya terbelakang dapat dilihat pada gambar 2.4.

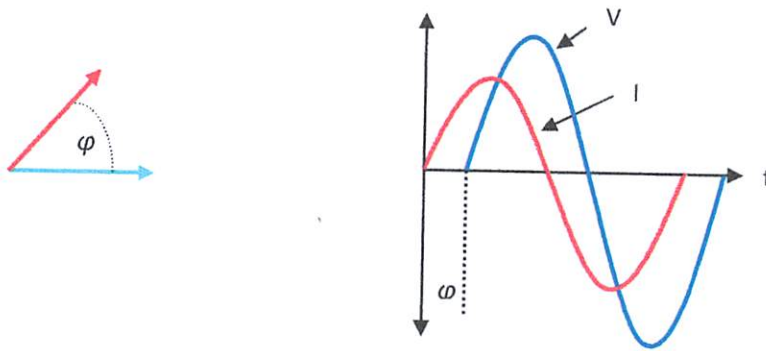


Gambar 2.4. Perbandingan Daya Aktif, Daya Reaktif, dan Daya Semu Pada Faktor Daya Tertinggal (*lagging*)

(Sumber: <http://www.google.com/factor daya>)

2.1.3. Faktor Daya Mendahului (*Leading*)

Faktor daya mendahului (*leading*) adalah keadaan dimana arus mendahului tegangan sebesar φ .

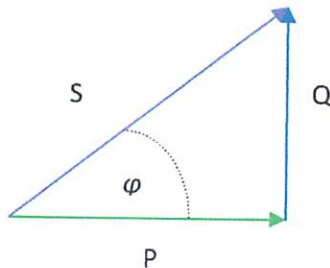


(a). Diagram fasor (b). Hubungan tegangan dan arus terhadap waktu

Gambar 2.5. Arus Mendahului Tegangan sebesar φ

(Sumber: [http://www.google.com/gambar/hubungan tegangan dan arus terhadap waktu](http://www.google.com/gambar/hubungan_tegangan_dan_arus_terhadap_waktu))

Hubungan antara daya aktif, daya reaktif, dan daya semu pada faktor daya mendahului dapat dilihat pada gambar 2.6.



Gambar 2.6. Perbandingan Daya Aktif, Daya Reaktif, Dan Daya Semu Pada Faktor Daya Mendahului (*Leading*)

(Sumber: [http://www.google.com/factor daya](http://www.google.com/factor_daya))

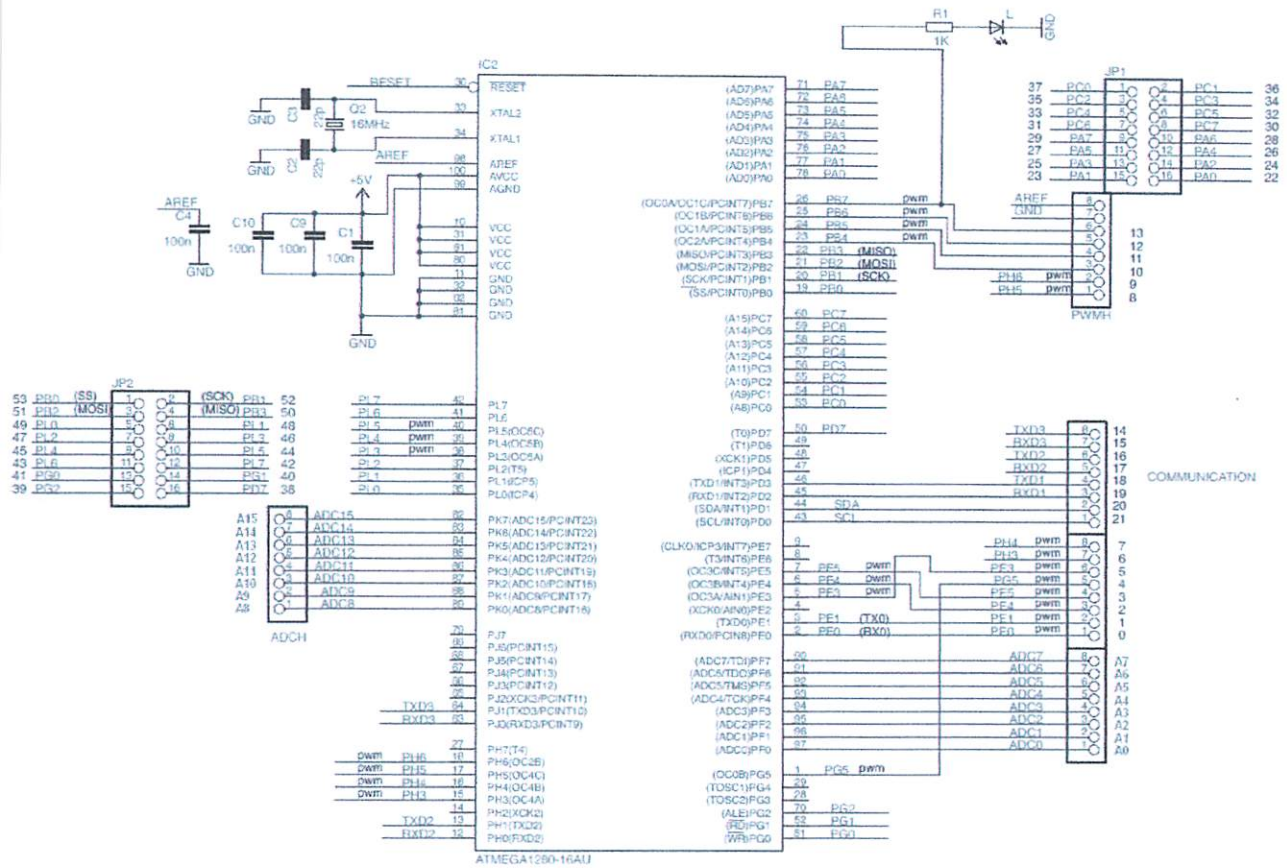
2.2.Mikrokontroller Arduino Mega

Arduino Mega 2560 adalah board *Arduino* yang merupakan perbaikan dari board Arduino Mega sebelumnya .ArduinoMega awalnya memakai chip ATmega1280 dan kemudian diganti dengan chip ATmega2560, oleh karena itu namanya diganti menjadi Arduino Mega 2560. Arduino Mega2560 bagusnya dipakai bila kita perlu mengendalikan banyak alat/sensor/aktuator.Atau apa bila kita perlu menggunakan lebih dari 1 modul serial, seperti modul Xbee misalnya, secara bersamaan. Arduino Mega 2560 mempunyai 4 port serial, lebih banyak dari Arduino Uno yang hanya punya 1 port serial. Atau apabila kita memerlukan ukuran Flash Memory yang lebih besar karena program yang dibuat sudah cukup tidak cukup dengan 32KB flash memory yang ada di Arduino Uno. Flash Memory sebesar 256KB yang ada di Arduino Mega 2560 rasanya sudah cukup besar untuk kebanyakan program di *microcontroller*.

Ringkasan.

Table 2.1. Ringkasan atmega 2560

Microcontroller	ATmega2560
Operating Voltage	5V
Input Voltage (recommended)	7-12V
Input Voltage (limits)	6-20V
Digital I/O Pins	54 (of which 15 provide PWM output)
Analog Input Pins	16
DC Current per I/O Pin	40 mA
DC Current for 3.3 V Pin	50 mA
Flash Memory	256 KB of which 8 KB used by bootloader
SRAM	8 KB
EEPROM	4 KB
Clock Speed	16 MHz

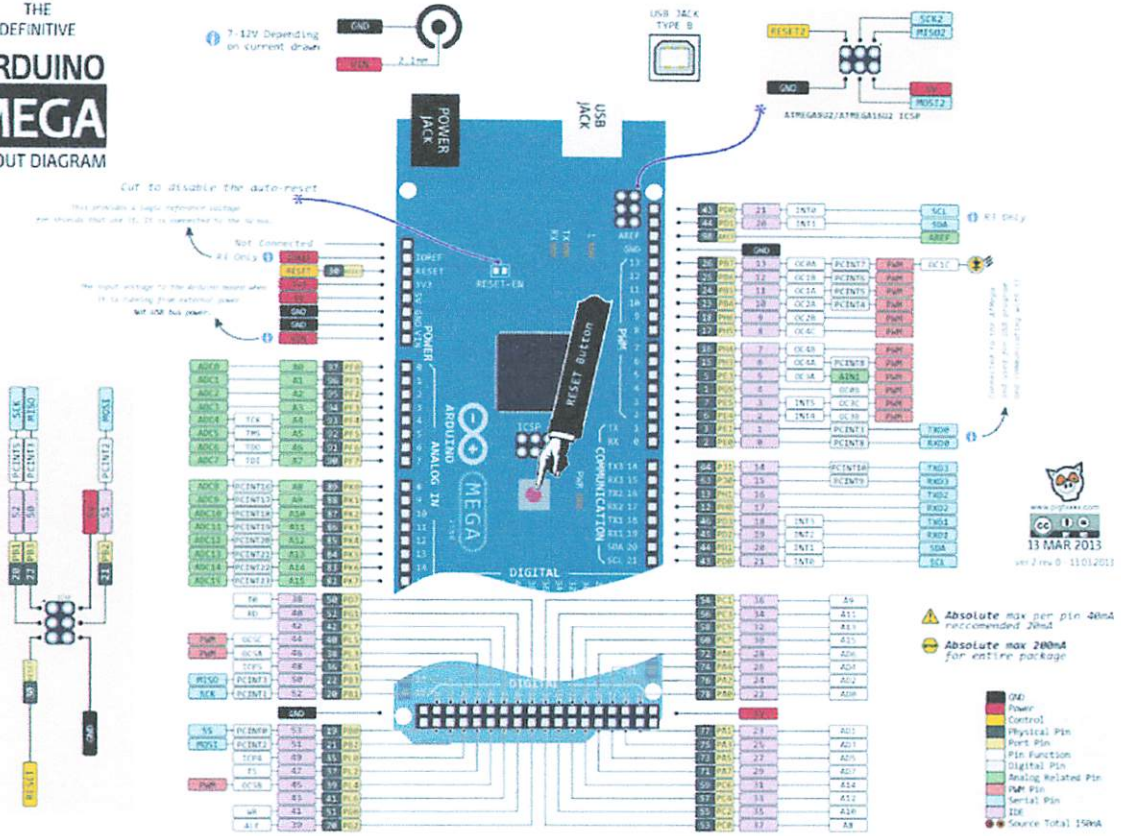


ARDUINO MEGA PINS SCHEMATIC			
DESIGN:	Tom Searff	Rev	
EMAIL:	esearff@tomsgad.com		
Doc	1	of	1

Gambar 2.7. Arduino Mega

(Sumber: http://www.google.com/arduino_mega2560)

THE
DEFINITIVE
**ARDUINO
MEGA**
PINOUT DIAGRAM

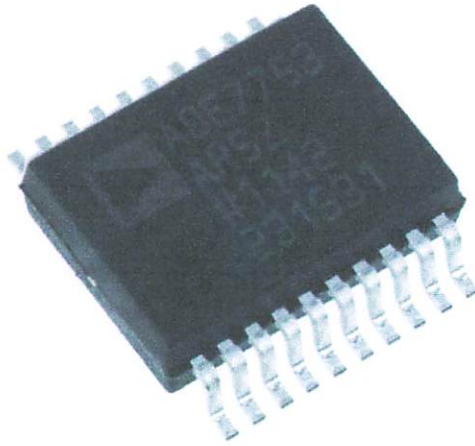


Gambar 2.8. Arduino Mega

(Sumber: <http://www.google.com/arduino mega2560>)

2.3 ADE 7753

Ade7753 adalah IC untuk pengukuran energy pada ic ade7753 ini dibutuhkan inputan sensor tegangan dan sensor arus untuk mendeteksi daya aktif. Untuk inputan dari sensor tegangan dan arus terdapat pada pin kaki 6,7 sebagai inputan tegangan dan pin 4,5 sebagai inputan arus. Pada ade7753 untuk komunikasi menggunakan SPI terdapat di pin 20,19,18,17.



Gambar 2.9 ade7753

(Sumber: <http://www.google.com/ade7753>)

Spesifikasi

- Akurasi tinggi mendukung dengan IEC 60687/61036/61268 and IEC 62053-21/62053-22/62053-23
- Dalam chip ini digital integrator dapat berkomunikasi untuk sensor arus dengan di/dt output
- Mendeteksi Aktif, reaktif dan apparent energy
- 0,1% error dalam pengukuran aktif energy
- Dalam chip ini sensor temperature ($\pm 3^{\circ}\text{C}$ typical)
- SPI serial interface
- Supply 5volt, tegangan rendah 25mW typical

2.4. LCD (Liquid Crystal Display)

LCD (*Liquid Crystal Display*) adalah suatu jenis media tampilan yang menggunakan Kristal cair sebagai penampil utama. LCD terdiri dari lapisan-lapisan cairan Kristal diantara 2 pelat kaca. Film transparan yang dapat menghantarkan listrik atau *back pane*, diletakkan pada lembaran blakang kaca. Bagian transparan film yang dapat menghantarkan arus listrik pada bagian luar dari karakter yang diinginkan dilapiskan pada pelat bagian depan. Pada saat terdapat tegangan antara segment dan *back pane*, bagian yang berarus listrik ini mengubah transmisi cahaya melalui daerah di bawah segment film. Berdasarkan jenis tampilan, LCD dapat dikelompokkan menjadi beberapa jenis, yaitu :



Gambar 2.10 Bentuk Fisik LCD 16x4

(Sumber: <http://gravitech.us>)

- Segment LCD

LCD jenis ini terbentuk dari beberapa *seven segment display* atau *sixteen segment display*, namun ada juga yang menggunakan gabungan dari keduanya. LCD jenis ini sering dipakai pada jam digital dan alat ukur digital.

- Dot Matrix Character LCD

LCD jenis ini terbentuk dari beberapa dot matrix display berukuran 5x7 atau 5x9, yang membentuk sebuah matrix yang lebih besar dengan berbagai kombinasi jumlah kolom dan baris. Kombinasi ini menentukan jumlah karakter yang dapat ditampilkan oleh LCD tersebut, seperti 4 baris x16 karakter atau 4 baris x 16 karakter.

- Grapich LCD

LCD jenis ini masih terus berkembang sampai saat ini. Resolusi LCD jenis ini bervariasi, diantaranya 128x64, 128x128, 240x64, 240x128.

2.4.1. Register LCD

Register-register yang terdapat pada LCD adalah sebagai berikut :

- IR (*Instruction Register*), digunakan untuk menentukan fungsi yang harus dikerjakan oleh LCD serta pengalamatan DDRAM atau CGRAM.
- DR (*Data Register*) digunakan sebagai tempat data pada DDRAM atau CGRAM yang dapat dituliskan atau dibaca oleh computer atau system minimum. Saat dibaca, DR menyimpan data DDRAM atau CGRAM, setelah itu data alamat berikutnya secara otomatis ke DR. pada waktu menulis, cukup melakukan inisialisasi DDRAM atau CGRAM sejak alamat awal tersebut.
- BF (*Busy Flag*) digunakan untuk memberi tanda bahwa LCD dalam keadaan siap atau sibuk. Apabila LCD sedang melakukan operasi internal, BF di-set menjadi 1, sehingga tidak akan menerima perintah dari luar. Jadi BF harus di-cek apakah telah doreset menjadi 0 ketika akan menulis LCD (member data pada LCD). Cara untuk menulis LCD adalah dengan mengeset RS menjadi 0 dan mengeset R/W menjadi 1.
- AC (*Address Counter*), digunakan untuk menunjuk alamat pada DDRAM atau CGRAM dibaca atau ditulis, maka AC secara otomatis menunjukkan alamat berikutnya. Alamat yang disimpan AC dapat dibaca bersamaan dengan BF.
- DDRAM (*Display Data Random Access Memory*), digunakan sebagai tempat penyimpanan data sebesar 80 byte. AC menunjukan alamat karakter yang sedang ditampilkan.

- CGROM (*Character Generator Read Only Memory*) pada LCD telah terdapat ROM untuk menyimpan karakter-karakter ASCII (*American Standart Code for Interchange Information*), sehingga cukup memasukan kode ASCII untuk menampilkannya.
- CGRAM (*character Generator Random Access Memory*) sebagai data storage untuk merancang karakter yang dikehendaki. Untuk CGRAM terletak pada kode ASCII dari 00h sampai 0Fh, tetapi hanya delapan karakter yang disediakan . alamat CGRAM hanya 6 bit, 3 bit untuk mengatur tinggi karakter dan 3 bit tinggi menjadi 3 bit rendah DDRAM yang menunjukan karakter, sedangkan 3 bit rendah sebagai posisi data CGRAM untuk membuat tampilan satu baris dalam dot matrix 5x7 karakter tersebut, dimulai dari atas. Sehingga karakter untuk kode ASCII 00h sama dengan 09h sampai 07h dengan 0FH. Dengan demikian, untuk perancangan satu karakter memerlukan penulisan data ke CGRAM sampai delapan kali.
- *Cursor and Blink Control Circuit*, merupakan rangkaian yang menghasilkan tampilan kursor dan kondisi *blink* (berkedip-kedip).

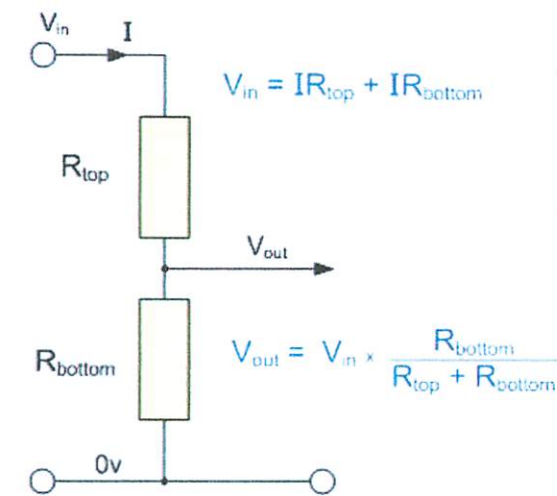
Fungsi masing-masing pin dari LCD Dot Matriks ini dapat dilihat pada Tabel berikut:

Tabel 2.2.Pin-Pin LCD dan Fungsinya

Pin No.	Symbol	Level	Description
1	Vss	0V	Ground
2	Vdd	5.0V	Supply Voltage for Logic
3	V0	VR	Operating voltage for LCD
4	RS	H/L	H: DATA, L: Instruction code
5	R/W	H/L	H: Read (MPU-Module) L: Write(MPU-Module)
6	E	H,H-L	Chip enable signal
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	A	4.2-4.6V	LED +
16	K	0V	LED -

2.5.Sensor Tegangan

Sensor tegangan berfungsi sebagai pembagi tegangan agar output dari sensor tegangan ini sesuai dengan karakter adc mikrokontroller . Pembagi tegangan (*voltage divider*) menghubungkan resistor seri seperti pada gambar dibawah ini, tegangan yang berbeda muncul di setiap resistor menghasilkan sebuah rangkaian yang disebut Rangkaian Pembagi Tegangan. Hukum tegangan Kirchoff menyatakan bahwa " tegangan dalam rangkaian tertutup sama dengan jumlah semua tegangan (IR) di seluruh rangkaian". Rangkaian dasar Resistor Seri sebagai Pembagi Tegangan dapat dilihat pada Gambar rangkaian dibawah ini.



Gambar 2.11. Rangkaian Pembagi Tegangan

(Sumber : <http://electronical-instrument.blogspot.com/2010/06/rangkaian-pembagi-tegangan.html>)

Dalam rangkaian dua resistor yang dihubungkan secara seri melalui V_{in} , yang merupakan tegangan listrik yang terhubung ke resistor, R_{top} , di mana tegangan keluaran V_{out} adalah tegangan resistor R_{bottom} yang diberikan oleh formula. Jika lebih resistor dihubungkan secara seri pada rangkaian maka tegangan yang berbeda akan muncul di setiap resistor berkaitan dengan masing-masing hambatan R ($I \times R$ Hukum Ohm) menyediakan tegangan berbeda dari satu sumber pasokan atau catudaya. Namun, harus berhati-hati ketika menggunakan jaringan jenis ini sebagai impedansi karena dapat mempengaruhi tegangan keluaran.

2.6.Trafo arus

Triad cst-1020 berfungsi sebagai trafo arus atau sering disebut dengan CT ini merupakan sensor arus yang dapat mengukur arus AC. dengan bentuk bulat terbuat dari material magnetic yang dililit koil sehingga berbentuk toroida. sensor ini tergolong sensor arus non kontak. untuk menggunakan sensor ini kabel yang dialiri arus listrik dimasukan kedalam lubangnya. Berikut gambar trafo arus atau CT



Gambar 2.12.trafo arus

(sumber: <http://www.google.com/gambar/triad-cst-1020>)

Pada CT lilitan primernya adalah kabel yang kita ingin ukur dan untuk lilitan sekundernya terdapat di dalam CT tersebut dengan jumlah N lilitan.

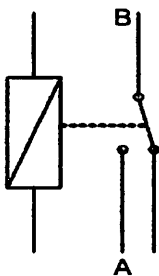
Berikut karakteristik dari cst-1020 pada produk triad.

- Arus primer 20 ampere
- Turns ratio 1000:1
- Burden resistor 100 ohm
- Frekuensi 50/60 hz
- Resistan DC 40 ohm
- Voltage secondary 0.0977 VAC

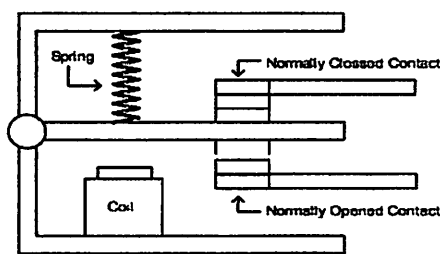
2.7. Relay

Relay adalah suatu saklar yang menghubungkan rangkaian beban on dan off dengan pemberian energi elektromagnetis, yang membuka atau menutup kontak pada rangkaian.

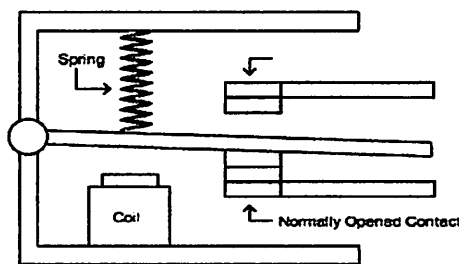
Pada dasarnya relay terdiri atas sebuah kumparan / koil dengan inti besi lunak, kontak relay dan lidah berpegas. Dasar kerja relay adalah jika kumparan dialiri arus maka terjadi perubahan medan magnet di sekitar kumparan, akibatnya besi lunak yang terdapat dalam inti kumparan berubah menjadi magnet dan menarik lidah berpegas sehingga kontak Normally Open (NO) menjadi saklar tertutup. Lidah inilah yang dijadikan sebagai salah satu kontak saklar. Jika arus dimatikan, berarti kumparan kehilangan arus maka sifat magnet pada besi lunak hilang dan lidah tertarik oleh pegas sehingga kontak Normally Closed (NC) tertutup. Pemasangan kumparan relay dihubungkan secara seri dengan rangkaian driver dan lidah kontak juga dihubungkan seri dengan beban. Hal ini akan menjaga keamanan rangkaian dari arus beban yang lebih besar daripada arus driver.



a. Simbol Relay SPDT



b. Konstruksi Relay Tanpa Tegangan



c. Konstruksi Relay Dengan Tegangan

Gambar 2.13. Relay SPDT

(Sumber: <http://www.google.com/gambar/skematik relay spdt>)

Relay mempunyai dua buah kontak yaitu Normally Open(NO) dan Normally Closed (NC). Normally Open adalah kontak relay dimana kontak ini terbuka pada saat kumparan relay tidak dialiri arus, sedang Normally Closed adalah kontak relay yang akan tertutup pada saat relay tidak dialiri arus dan secepatnya membuka kembali ketika kumparan diberi arus. Agar lebih jelas berikut cara kerja dari sebuah relay:

- a) Mula-mula relay dalam keadaan tanpa arus, posisi kontak dalam keadaan Normally Closed (NO), karena lidah tertarik oleh gaya pegas,
- b) Arus diberikan pada koil, terjadi medan magnet dalam kumparan dengan inti besi lunak
- c) Medan magnet yang dihasilkan dalam inti besi menarik lidah berpegas sampai terhubung dengan kontak Normally Open, keadaan ini mengubah kontak Normally Closed terbuka dan kontak Normally Open tertutup.
- d) Jika sumber arus dihilangkan maka medan elektromagnet pada inti besi lunak hilang dan lidah tertarik oleh gaya pegas. Lidah kontak seperti posisi semula dan posisi kontak Normally Closed tertutup. Bahan yang digunakan sebagai kontaktor relay bermacam-macam, disesuaikan dengan kebutuhan dan harga yang dimiliki oleh kontak tersebut.

Bahan-bahan tersebut rata-rata merupakan suatu penghantar yang baik seperti silver / perak, Perak Cadmium Oxide, Palladium, Platina, dan Emas. Pemilihan bahan ini tentu saja berpengaruh pada harga dan kualitas barang yang digunakan.

2.8.Xbee

Xbee ini berfungsi sebagai pengirim dan penerima data dengan menggunakan transfer data secara wireless dengan jarak 50m-3km untuk pengiriman dan penerimaan data. Dengan jarak 50m-3km Xbee tidak boleh terhalang oleh benda agar jarak jangkauan dapat maksimal.pada Xbee banyak digunakan oleh tim robot sebagai control atau monitoring secara jarak jauh yang dapat dikontrol atau monitoring melalui personal computer dengan komunikasi Serial RS232 atau TTL.

Gambar sebagai berikut:



Gamabar 2.14. modul Xbee

(Sumber:<http://www.google.com/gambar/xbee>)

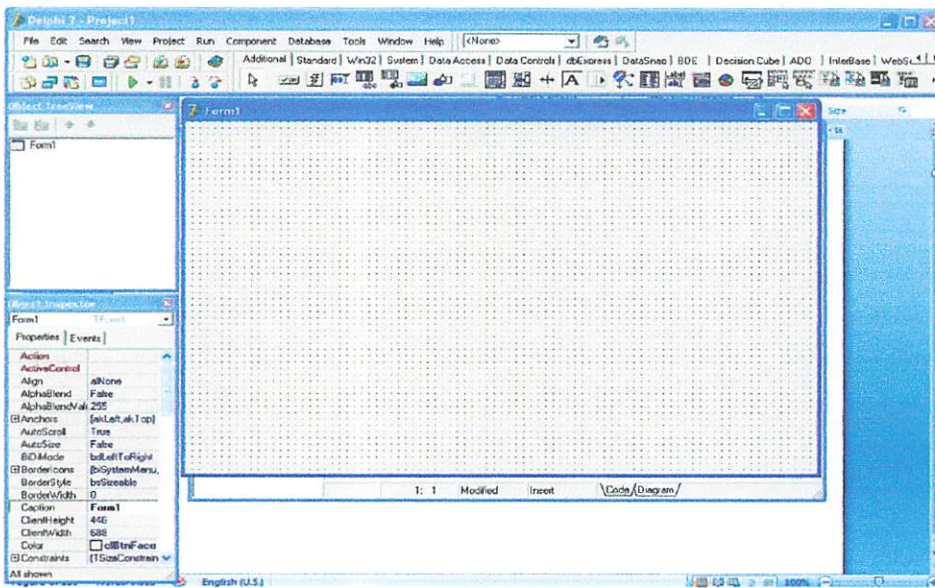
Fitur Xbee

- 100 mW daya output
- Panjang rentang: 4000 meter
- Miniatur jejak: 0.9 "x 1.63"
- Terpadu PCB F antenna atau konektor U.FL untuk antenna eksternal
- Seluruh Dunia penerimaan: FCC, IC dan CE
- Powerfull Texas Instruments 256k MSP430 dengan 802.15.4 MAC atau ZigBee Stack
- LSR interface serial berdasarkan 802.15.4 MAC
- operasi daya rendah
- RoHS compliant
- Pengembangan Efisien dengan jasa desain LSR.
- Pilihan Lisensi tersedia untuk membeli desain atau mengintegrasikan desain.

2.9. Borland Delphi

Borlan Delphi adalah lah sebuah perangkat lunak (software) yang digunakan untuk membuat aplikasi berbasis antarmuka grafis di lingkungan sistem operasi Microsoft Windows. Delphi dibuat oleh perusahaan Borland Software Corporation. Delphi telah ada sejak 1993 dan versi yang saya gunakan dalam pembuatan aplikasi di tulisan ini adalah Delphi versi 7.0 . Bahasa pemrograman yang digunakan Delphi adalah bahasa Pascal.

Keunggulan bahasa pemrograman ini terletak pada produktifitas , kualitas, pengembangan perangkat lunak, kecepatan aplikasi, pola desain yang menarik serta di perkuat dengan program yang terstruktur, keunggulan lain dari Delphi adalah dapat di gunakan untuk merancang program apliksi yang memiliki tampilan seperti program lain yang berbasis windows.



Gambar 2.15.IDE Borland Delphi

2.10. Komponen Delphi

Berikut ini adalah beberapa komponen yang sering digunakan saat pembuatan aplikasi dari Component Palette Standar

Tabel 2.3. Beberapa komponen dari Component Palette Standard

Componen Palette standard		
Icon	Nama	Keterangan
	Frames	Membuka sebuah dialog box yang menampilkan daftar frames yang disertakan pada proyek
A	Label	Menampilkan teks yang tidak dapat diubah oleh us
	Edit	Menampilkan sebaris teks yang dapat diisi oleh user
	Memo	Menampilkan sebuah area pengeditan dimana user dapat memasukkan atau memodifikasi beberapa baris teks didalamnya
	Button	Untuk membuat tombol tekan yang akan diisi dengan suatu aksi tertentu
	Listbox	Menampilkan daftar pilihan yang dapat digulung (scroll)
	Scrol bar	Dapat digunakan untuk meluaskan area pandang di form
	Radio group	Digunakan untuk membuat sekelompok radio-butto

2.11. Komunikasi Data

Komunikasi data adalah bagian dari telekomunikasi yang secara khusus berkenaan dengan transmisi atau pemindahan data dan informasi diantara komputer dan piranti-piranti yang lain dalam bentuk digital yang dikirimkan melalui media komunikasi data. Data berarti informasi yang disajikan oleh isyarat digital.

Komponen-komponen komunikasi data :

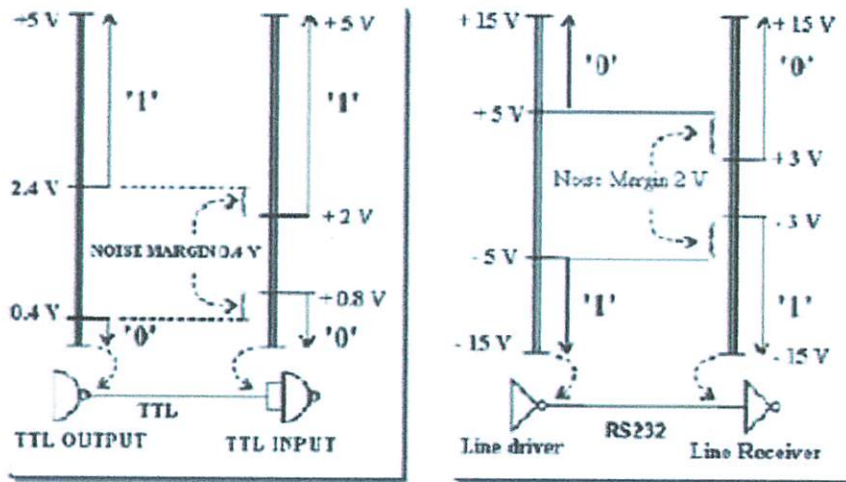
1. Pengirim, adalah piranti yang mengirimkan data.
2. Penerima, adalah piranti yang menerima data.
3. Data, adalah informasi yang akan dipindahkan.
4. Media pengirim, adalah media atau saluran yang digunakan untuk mengirimkan data.
5. Protokol, adalah aturan-aturan yang berfungsi untuk menyelaraskan hubungan. Pola komunikasi pada elektronika dapat diklasifikasikan menurut arah komunikasi, tipe sinyal dan keaslian sinyal.

2.12. Standart RS232

Standar RS232 ditetapkan oleh *Electronic Industry Association and Telecommunication Industry Association* pada tahun 1962. Nama lengkapnya adalah *EIA/TIA-232 Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange*. Meskipun namanya cukup panjang tetapi standar ini hanya menyangkut komunikasi data antara komputer dengan alat-alat pelengkap komputer. Ada dua hal pokok yang diatur standar RS232, antara lain adalah:

1. Bentuk sinyal dan level tegangan yang dipakai

RS232 dibuat pada tahun 1962, jauh sebelum IC TTL populer, oleh karena itu level tegangan yang ditentukan untuk RS232 tidak ada hubungannya dengan level tegangan TTL, bahkan dapat dikatakan jauh berbeda. Berikut perbedaan antara level tegangan RS232 dan TTL seperti gambar 2.19 berikut:



Gambar2.16. Perbedaan antara level tegangan RS232 dan TTL

2. Penentuan jenis sinyal dan konektor yang dipakai

- Sebuah 'spasi' atau space (logika 0) antara tegangan +3 s/d +25 volt
- Sebuah 'tanda' atau mark (logika 1) antara tegangan -3 s/d -25 volt
- Daerah tegangan antara +3 s/d -3 volt tidak didefinisikan
- Tegangan rangkaian terbuka tidak boleh lebih dari 25 volt (dengan acuan ground)
- Arus hubung singkat rangkaian tidak boleh lebih dari 500 mA

BAB III

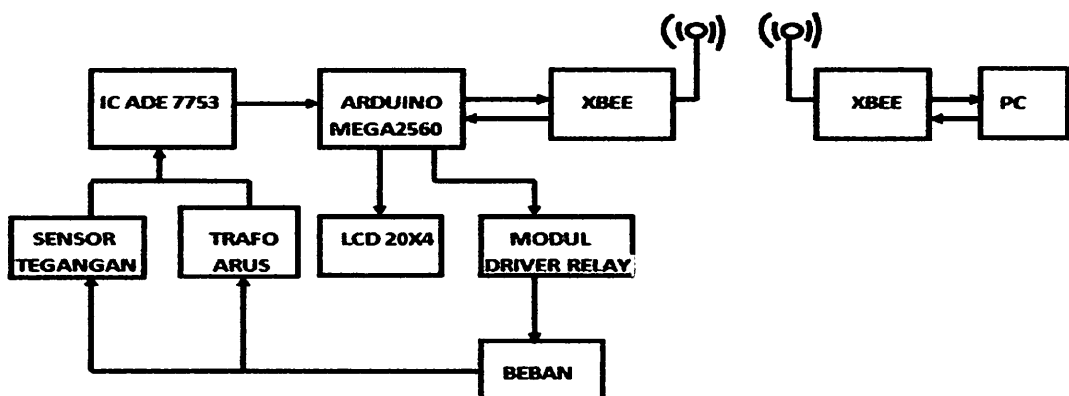
PERANCANGAN DAN PEMBUATAN ALAT

3.1. Pendahuluan

Pada bab ini akan membahas mengenai perancangan dan pembuatan alat pembahsan akan dilakakuan pada setiap blok rangkaian, cara kerja masing-masing blok rangkaian, perhitungan dan fungsi masing-masing blok rangkaian tersebut. Secara garis besar terdapat tiga bagian perangkat yang ada yaitu perancang perangkat keras (*Hardware*). Perancangan perangkat lunak (*Software*) dan perancangan mekanik. Pada perancangan mekanik. Pada perancangan perangkat keras akan meliputi seluruh *peripheral* yang digunakan pada sistem ini. Pada perancangan perangkat lunak akan meliputi diagram alir dan *software* secara umum. Akan tetapi kedua perangkat ini dalam kerjanya akan saling menunjang satu sama lain. Secara umum cara kerja alat ini adalah melihat daya aktif dan *control* beban. personal computer digunakan sebagai monitoring daya dan control beban secara *wireless* dengan modul Xbee. Rangkaian ini terdiri dari arduino mega sebagai *control* dan *monitoring* daya dan ic ade7753 sebagai pengolah data dari masukan sensor tegangan dan sensor arus untuk menghasilkan daya aktif yang akan dikirim ke arduino.

3.1 Blok Diagram Sistem Keseluruhan

3.1.1



Gambar 3.1 Diagram blok alat

Penjelasan diagram blok system:

- Ade7753
Berfungsi sebagai chip yang mampu memberikan informasi tentang daya, arus dan tegangan yang dihasilkan oleh beban. Pada ic ade7753 ini menggunakan komunikasi SPI yang terdapat pada pin 17,18,19,20.
- Trafo arus
Berfungsi sebagai melihat arus yang mengalir pada beban dan akan dibaca oleh ic ade7753.
- Sensor tegangan
Berfungsi sebagai melihat tegangan yang terdapat pada beban dan sensor tegangan akan dibaca oleh ic ade7753.
- Arduino mega2560
Berfungsi digunakan untuk antar muka antara kwh meter dan sistem jaringan menggunakan teknologi Xbee yang bekerja pada jaringan wireless.
- Lcd 16x4
Berfungsi untuk tampilan daya, arus, tegangan pada arduino.
- Relay
Berfungsi untuk pemutus dan penghubung antara arduino dengan beban sebagai *control* yang dilakukan oleh pc.
- Beban
Berfungsi untuk membebani menggunakan lampu agar terjadi suatu beban dan dapat dibaca oleh ade7753 dan data dapat di *monitoring* pada pc.
- Xbee
Berfungsi sebagai pengirim data dari arduino ke pc melalui jaringan *wireless* agar dapat di monitor pada pc.
- Pc
Berfungsi sebagai monitoring dan controlling daya yang dikirim dari arduino ke pc.

Cara Kerja Sistem

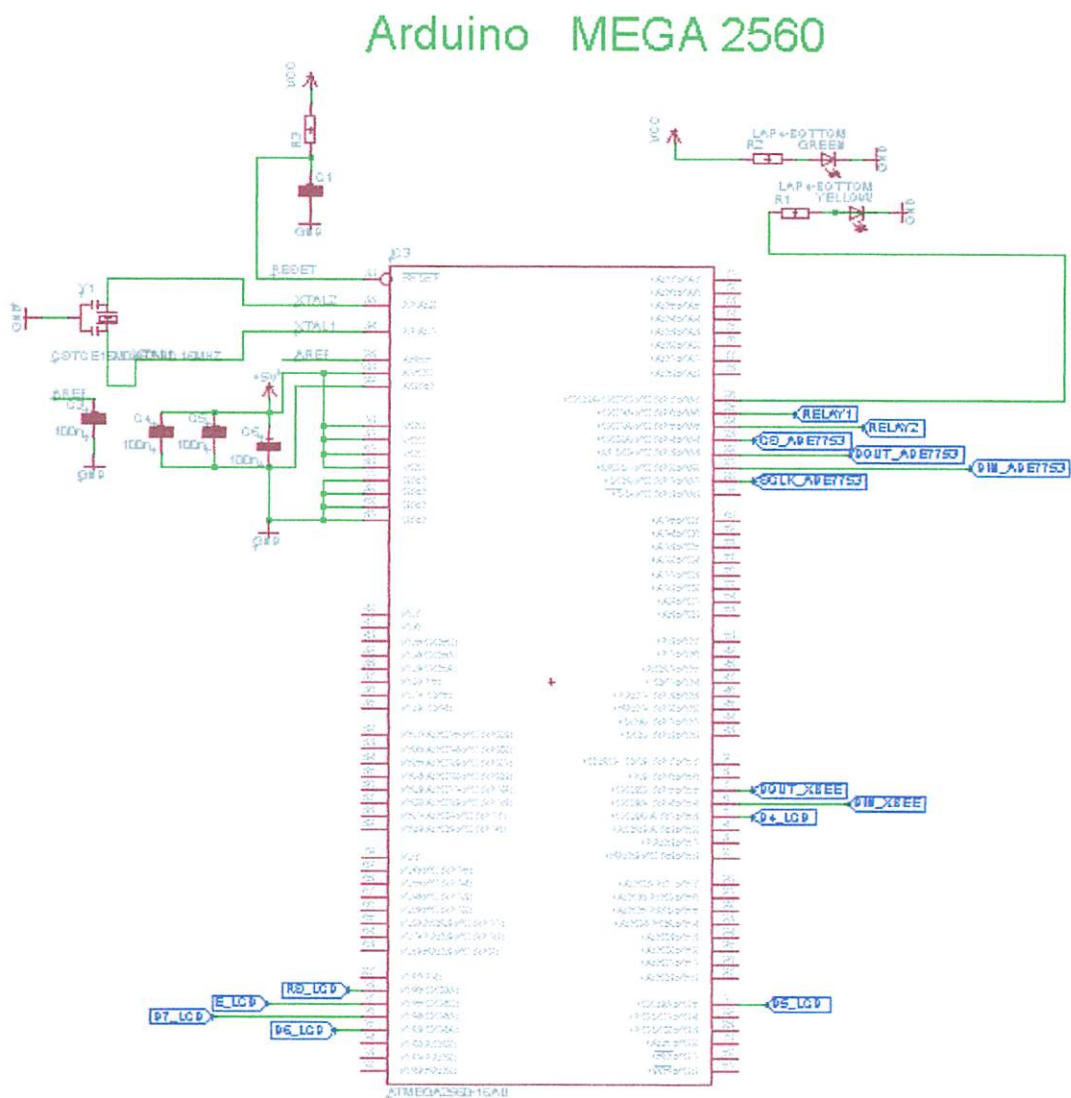
Dari diagram block pada gambar 3.1 dapat dijelaskan cara kerja *smart meter* sebagai berikut. Dimana ic *ade7753* berfungsi sebagai monitoring daya dan terdapat sensor arus dan tegangan untuk monitoring daya, kemudian data yang di hasilkan oleh ic *ade7753* dikirim ke Arduino. komunikasi dua arah menggunakan arduino yang berkerja sebagai monitoring daya dan control. Data yang di peroleh pada arduino akan diteruskan ke modul Xbee kemudian data akan dikirim ke personal computer secara *wireless* sebagai jaringan komunikasi, personal computer berfungsi untuk *control* dan monitoring daya.

Pada sistem ini personal computer mempunyai dua fungsi yaitu sebagai *monitoring* dan *control*. Data dari smart meter akan diolah oleh arduino, proses pengiriman data ke personal computer menggunakan modul Xbee melalui jaringan *wireless* sebagai *monitoring* daya. Personal computer memberikan perintah kontrol kepada arduino untuk kontrol beban.

3.2 Perancangan Arduino Mega

Pada perancangan dan pembuatan alat ini mikrokontroler arduino digunakan untuk menerima sinyal analog dan digital dari IC ADE7753 kemudian memproses sinyal yang masuk tersebut untuk selanjutnya di kirim ke perangkat output LCD, Xbee dan Personal komputer.

Mikrokontroler ini juga akan memproses sinyal masukan dari personal computer untuk *control* beban. Konfigurasi pin-pin yang digunakan pada perancangan dan pembuatan alat ini dapat dilihat pada gambar 3.2.



Gambar 3.2. Skematik Arduino Mega

Pada arduino mega menggunakan crystal 16Mhz bertujuan agar perhitungan baudrate tidak mengalami error yang disebabkan selisih perhitungan. Perhitungan baud rate pada atmega 16 dengan baut rate yang diinginkan adalah 38400bps. Perhitungan clock dapat dihitung sebagai berikut

Diketahui :

$$UBRR = (f_{osc} / 16 \cdot \text{Baud}) - 1$$

$$UBRR = (16000000 / 16 \cdot 38400) - 1$$

$$UBRR = (16000000 / 614400) - 1$$

$$UBRR = 26 - 1$$

$$= 25$$

$$= 16 \text{ MHz}$$

Penggunaan Kristal 16,0000 MHz memungkinkan hasil perhitungan baudrate tidak sisa dan error dari selisih perhitungan tidak ada. Sehingga dengan menggunakan nilai Kristal 16,0000MHz maka dapat dihitung waktu yang diperlukan untuk satu siklus mesin yaitu

$f = 16,0000 \text{ MHz}$ Sehingga :

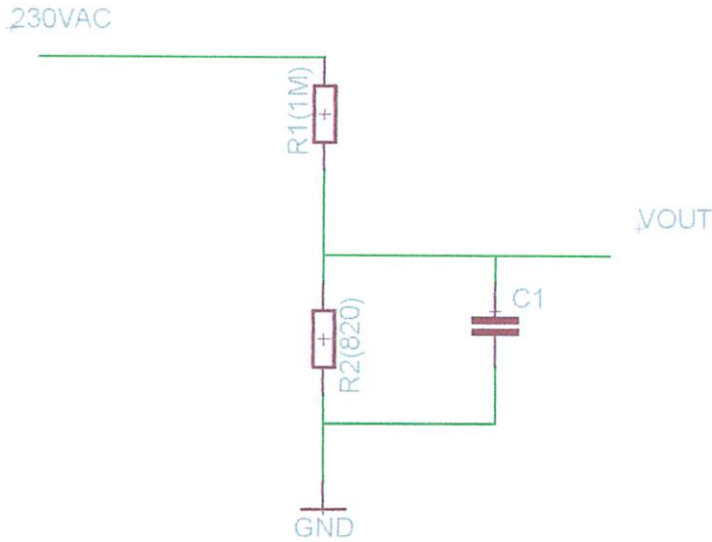
$$T = \frac{1}{f_{\text{kristal}}}$$

$$T = \frac{1}{16,0000 \text{ MHz}}$$

$$T = 6.25 \cdot 10^{-8}$$

3.3.Perancangan Sensor tegangan

Pada perancangan dan pembuatan sensor tegangan ini menggunakan dua buah resistor sebagai inputan dari tegangan ac 220v ke pin ic ade7753 yaitu pin 7 untuk positif dan pin 6 untuk netral.



Gambar 3.3.Rangkaian Sensor Tegangan

Pada ADC IC ADE7753 hanya mampu menerima tegangan ac maksimal 0.5 volt, sedangkan pada IC ADE7753 inputan nya menggunakan tegangan 220volt/110volt AC maka tidak diperlukan converter ke tegangan dc. Maka dengan rangkaian pembagi tegangan ini sangat membantu sekali sebagai sensor tegangan. Nilai dari resistor tersebut dapat dicari dengan rumus sebagai berikut :

$$V_{out} = \frac{R_2}{R_1 + R_2} \times V_{in} \dots \dots \dots (3.1)$$

Dimana :

V_{out} = Tegangan output dari resistor (V)

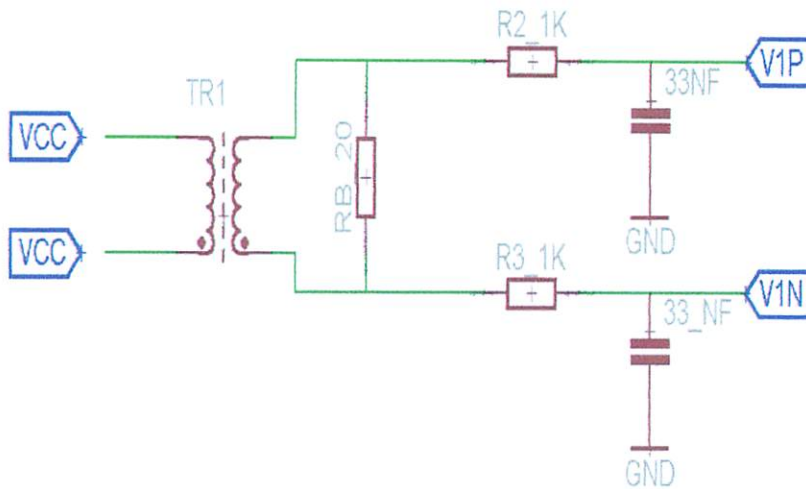
V_{in} = Tegangan sumber (V)

R_1 dan R_2 = Resistor (Ω)

$$\begin{aligned} V_{out} &= \frac{820}{1000000 + 820} \times 230 \\ &= 0.000819 \times 230 \\ &= 0.188 \text{ v} \end{aligned}$$

3.4. Perancangan trafo arus

Pada perancangan ini Triad cst-1020 berfungsi sebagai trafo arus atau sering disebut dengan CT ini merupakan sensor arus yang dapat mengukur arus AC. dengan bentuk bulat terbuat dari material magnetic yang dililit koil berikut gambar rangkaian trafo arus.



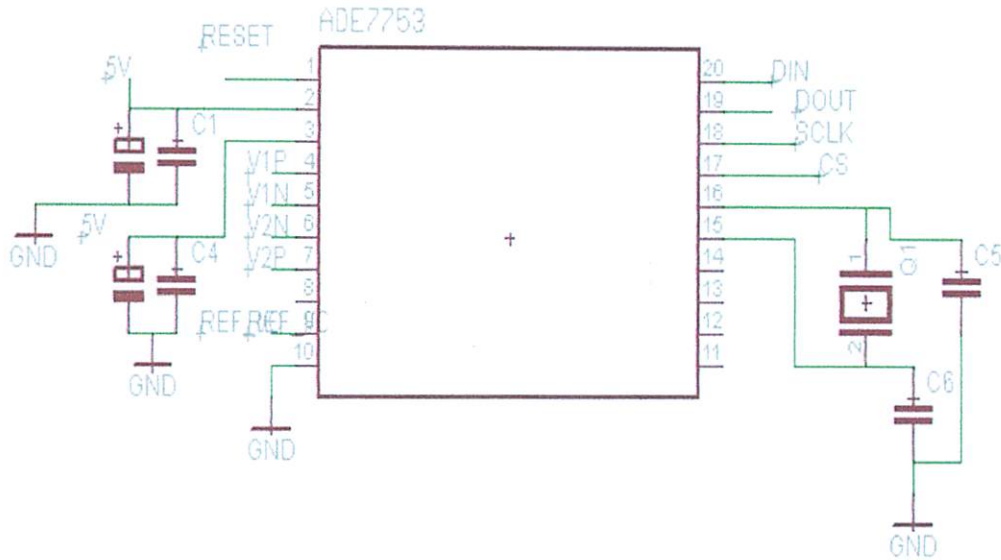
Gambar 3.4. Rangkaian Trafo Arus

Pada rangkaian CT atau trafo arus yang berfungsi seperti rangkaian pembagi tegangan dimana R1 dan R2 menggunakan 1k dan Rb menggunakan 20ohm. Pada inputan kaki V1P, V1N terdapat ADC sebesar 0,5 Volt. berikut perhitungan maksimal tegangan yang dapat terukur pada rangkaian trafo arus.:

$$\begin{aligned}
 V_{out} &= \frac{R_b}{R_1 + R_2 + R_b} \times V_{IN} \\
 &= \frac{20}{1000 + 1000 + 20} \times 20 \\
 &= 0,009 \times 20 \\
 &= 0,19 \text{ volt}
 \end{aligned}$$

3.5.Perancangan ADE7753

Pada perancangan ic ade7753 ini saya menggunakan sensor tegangan sebagai inputan pada pin kaki 6,7 dan untuk mendeteksi arus saya menggunakan trafo arus dengan type CST-1020 maksimal arus yaitu 20A, yang akan di inputkan pada pin kaki 4 dan 5 untuk maksimal ADC pada ic ade7753 0,5volt. Berikut perancangan IC ADE7753.



Gambar 3.5.Skematik ADE7753

Pada ade7753 juga terdapat clock 3,58-4Mhz yang sudah di tentukan oleh data sheet. Pada clock IC ADE7753 digunakan untuk kecepatan transfer data. pada ic ade7753 pin 17,18,19,20 digunakan sebagai komunikasi *Serial Peripheral Interface* (SPI) antara ic dengan arduino. Dengan menggunakan nilai crystal 3,58/4MHz maka dapat dihitung waktu yang diperlukan untuk satu siklus mesin.

Berikut perhitungan crystall pada IC ADE7753 dengan clock 3,58Mhz

$f = 16,0000 \text{ MHz}$ Sehingga :

$$T = \frac{1}{f_{\text{kristal}}}$$

$$T = \frac{1}{3,58000 \text{ MHz}}$$

$$T = 27.932961 \cdot 10^{-8}$$

3.5.1 Pembacaan cosphi

Pada perancangan ade7753 cosphi menggunakan beban lampu 35watt dapat dihitung dengan contoh dan rumus perhitungan sebagai berikut :

$$\text{Cosphi} = \frac{P}{S} \dots\dots\dots (3.2)$$

$$0.99 = \frac{35}{S}$$

$$S = 35 / 0.99$$

$$= 35,35 \text{ watt}$$

Maka hasil yang diperoleh pada daya semu sebesar 35,35 VA

3.5.2 Pembacaan daya aktif

Pada perancangan ade7753 daya aktif menggunakan beban lampu 35watt dapat dihitung dengan contoh dan rumus perhitungan sebagai berikut :

$$P = V \times I \times \text{cosphi} \dots\dots\dots (3.3)$$

$$= 224 \times 0.15 \times 0.99$$

$$= 34.65 \text{ Watt}$$

Maka hasil yang akan didapat pada pembacaan sensor untuk daya aktif sebesar 34 watt

3.5.3 Pembacaan daya reaktif

Pada perancangan ade7753 daya reaktif dengan beban bor listrik dengan beban 450 watt dapat dihitung dengan contoh dan rumus perhitungan sebagai berikut :

$$P = V \times I \times \text{sinphi} \dots\dots\dots (3.4)$$

$$P = 225 \times 2,00 \times \text{sinphi}$$

$$= 225 \times 2,00 \times 0.198$$

$$= 89,1 \text{ VAR}$$

Untuk mendapatkan nilai sinphi mencari nilai daya semu dan nilai cosphi untuk merubah nilai cosphi agar menjadi nilai sudut.

Mencari nilai daya semu :

$$S = V \times I$$

$$450 = 225 \times 2,00$$

Mencari nilai cosphi :

$$\text{Cosphi} = \frac{P}{S}$$

$$= \frac{441}{450}$$

$$= 0.98$$

Mencari nilai sinphi :

$$\text{Cosphi} = \arccos 0.98$$

$$= 11.47^\circ$$

$$= \sin 11,47^\circ$$

$$= 0.198$$

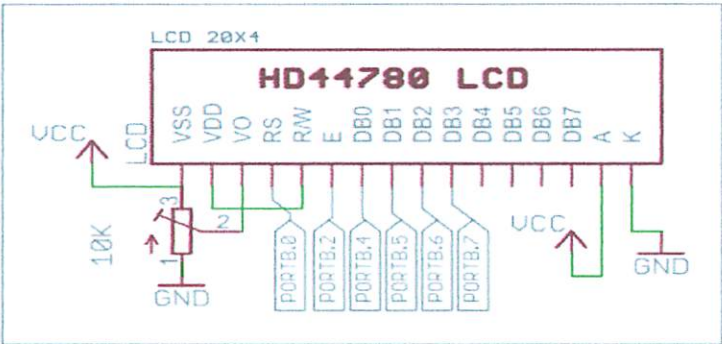
3.6.Perancangan LCD 16x4

Dalam perancangan ini menggunakan sebuah layar LCD dengan dimensi 16x4 yang tampilanya terdiri dari 4 baris yang masing – masing barisnya berisi 16 karakter. Berikut fungsi masing – masing pin LCD.

Table 3.1.Fungsi Masing-masing Sinyal LCD

Nama sinyal	Fungsi
DB0-DB7	Merupakan saluran data, berisi perintah dan data yang akan di tampilkan di LCD
Enable	Sinyal operasi awal, sinyal ini mengaktifkan data tulis atau baca
R/W	Sinyal seleksi tulis atau baca 0 : tulis 1 : baca
RS	Sinyal pemilih register 0 : instruksi register (tulis) 1 : data register (baca dan tulis)

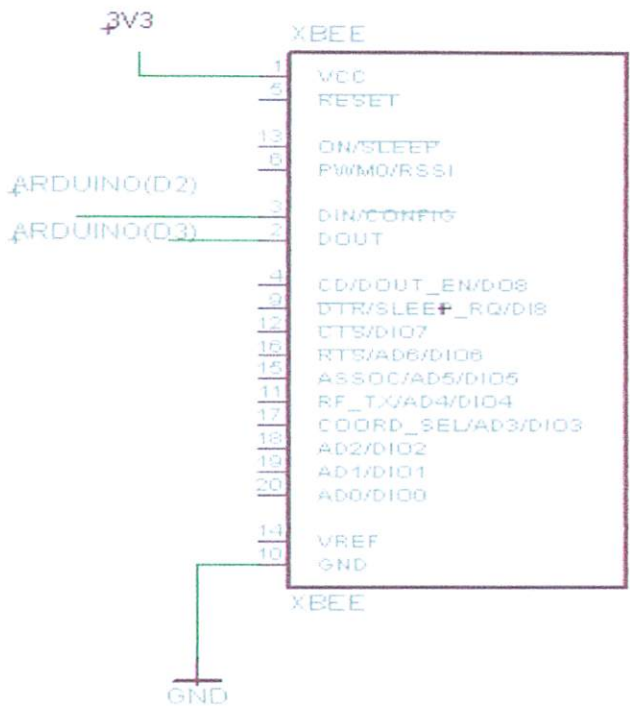
Secara garis besar pemrograman LCD diatur oleh 3 sinyal yaitu RS, R/W, Enable dan 8 buah saluran data. Karena pada tugas akhir ini LCD difungsikan sebagai komunikai 4 bit, jadi saluran data yang dipakai hanya D4 s/d D7. VR pada rangkaian digunakan untuk mengatur kontras LCD.



Gambar 3.6. Skema Rangkaian LCD Modul

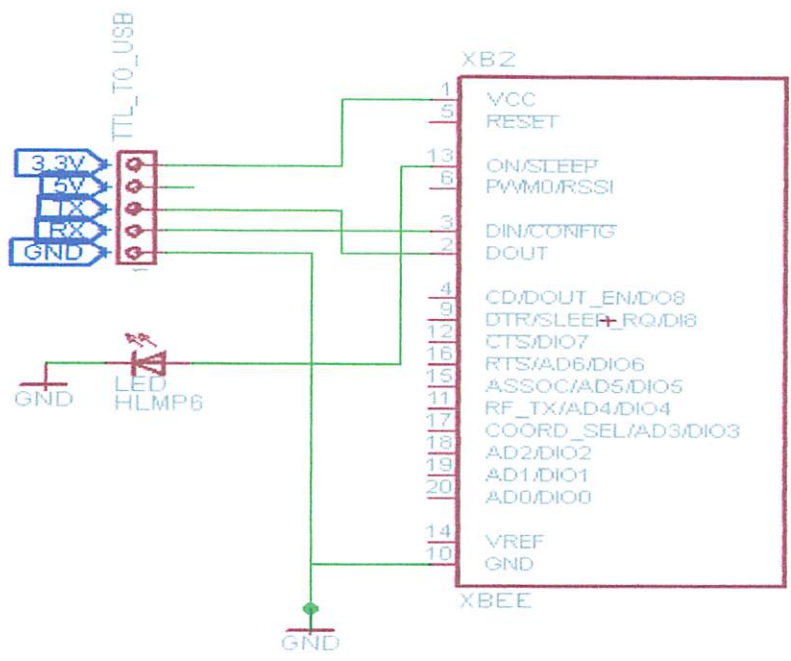
3.7 Perancangan Xbee

Dalam perancangan ini menggunakan jaringan *wireless* dengan modul xbee tujuan untuk pengiriman data dari arduino ke pc melalui jarak yang jauh dengan harapan data mampu dikirim dengan jarak yang kita inginkan dan data tetap valid. Pada xbee ini juga memerlukan supply 3volt. berikut gambar 3.7 konfigurasi xbee.



Gambar 3.7 Konfigurasi Xbee dengan Arduino

Xbee ini merupakan jenis *wireless* dengan type 802.15.4 dengan ke mampuan jarak pengiriman data 50-3000m untuk komunikasi xbee menggunakan serial TTL dan juga untuk konsumsi daya cukup kecil yaitu 3.3v pada Xbee ini juga dibekali dengan antenna kecil yang berguna sebagai pemancar agar jangkauan sinyal lebih jauh dan stabil. Pin Xbee yang digunakan sebagai transfer data yaitu pin 3 sebagai data input dan pin 3 sebagai data out.

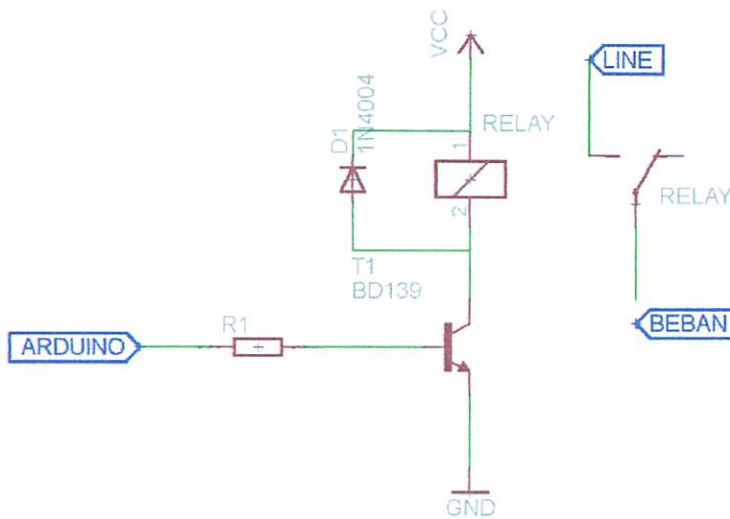


Gambar 3.8 Konfigurasi Xbee pin TTL to USB

Karena pada modul usb tidak terdapat usb untuk berkomunikasi dengan komputer maka diperlukan konverter usb to ttl tersebut, USB to TTL tersebut sudah terdapat tegangan 3,3v yang di perlukan untuk catu daya xbee jadi tidak perlu catu daya eksternal untuk memberi masukan tegangan pada xbee

3.8. Perancangan driver relay

Driver relay adalah rangkaian yang digunakan untuk mengendalikan pengoprasian relay. driver relay ini berfungsi sebagai *control* yang dilakukan oleh mikrokontroller arduino mega dengan beban sebagai pembatasan. Pada rangkaian driver relay juga terdapat transistor dengan type SS9013 dimana berdasarkan datasheet pengutan atau h_{FE} transistor ini minimal 64, nilai V_{be} 1,2 volt, dan nilai V_{ce} 0.6V. Berikut gambar rangkaian driver relay.



Gambar 3.9. Driver Relay

maka dalam perancangan driver relay ini R_1 dapat ditentukan dengan perhitungan sebagai berikut:

diketahui :

$$I_{Cmax} = 500 \text{ mA}$$

$$V_{CEt} = 0,6 \text{ V}$$

$$V_{BE} = 1,2 \text{ V}$$

$$h_{FE} = 64$$

$$R_{coil} = 70 \, \Omega$$

$$V_{relay} = 5 \text{ V}$$

$$V_{BB} = 5 \text{ V}$$

Maka :

$$V_{\text{relay}} = I_c \cdot R_{\text{coil}} + V_{ce}$$

$$5V = I_c \cdot 70\Omega + 0,6V$$

$$I_c = \frac{5 - 0,6}{70}$$

$$= 0.063 \text{ mA}$$

$$I_B = \frac{I_c}{h_{FE}}$$

$$I_B = \frac{0.063}{64}$$

$$= 0.000984 \text{ mA}$$

Perhitungan nilai R_B :

$$V_{BB} = I_B \cdot R_B + V_{Be}$$

$$5V = 0.00098 \text{ mA} \cdot R_B + 1,2V$$

$$R_B = \frac{5 - 1,2}{0,00098}$$

$$= 3877.551 \Omega \approx 3k8\Omega$$

Harga untuk nilai pada basis Transistor atau R_1 yaitu $3k\Omega$ pada perhitungan tersebut menggunakan inputan dari mikrokontroller dengan tegangan TTL atau VCC 5V.

3.10.Flowchart Sistem



Gambar 3.12. Flowchart sistem

BAB IV

PENGUJIAN DAN PEMBAHASAN

1. Umum

Pada bab ini membahas tentang pengujian serta pembahasan hasil perancangan dari sistem monitoring daya menggunakan ic ade7753 yang bertujuan untuk mengetahui apakah rangkaian tersebut dapat bekerja dengan baik dan sesuai dengan perancangan serta digunakan untuk mengetahui kekurangan ataupun kelemahan dari sistem.

Setelah perancangan dan pembuatan alat telah selesai maka selanjutnya akan diuji terlebih dahulu dari masing-masing blok rangkaian. Setelah semua blok dari sistem telah diuji dan bekerja dengan baik maka selanjutnya dilakukan pengujian alat secara keseluruhan.

Pengujian yang dilakukan meliputi:

- Pengujian LCD 16x4
- Pengujian Arduino mega2560
- Pengujian pengiriman data xbee ke PC
- Pengujian sensor tegangan, trafo arus CST-1020 dan ADE7753
- Pengujian Driver Relay
- Pengujian aplikasi Borland delphi
- Pengujian keseluruhan

4.1. Pengujian Rangkaian Sensor Tegangan

4.1.1. Tujuan Pengujian Rangkaian Sensor Tegangan

Pengujian ini dilakukan untuk mengetahui apakah sensor tegangan ini pembacaanya sesuai dan dapat di baca oleh mikrokontroller Arduino Mega2560.

4.1.2.Peralatan Yang Digunakan

1. AVO meter
2. Sensor Tegangan
3. Power supply
4. Rangkaian ADE7753
5. Arduino mega2560
6. Personal computer
7. Lcd 16x4
8. Arduino mega2560
9. Software arduino

4.1.3.Prosedur Pengujian Sensor Tegangan

1. Pengujian sensor tegangan pada Arduino Mega2560.
2. Persiapkan rangkaian ade7753.
3. Sambungkan pin ADE7753 dengan Arduino.
4. Upload program ke arduino.
5. Amati perubahan tegangan pada personal komputer.
6. Amati dan Catat hasil pengukuran AVO dan pembacaan sensor.
7. Bandingkan hasil pengukuran dan pembacaan.

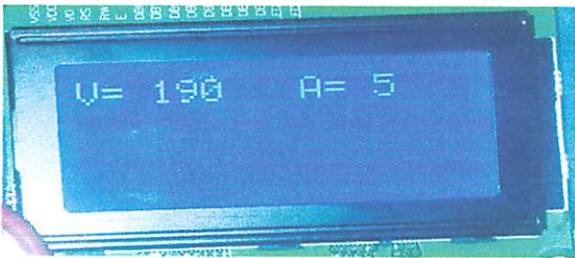
4.1.4.Hasil Pengujian Sensor Tegangan

Tabel 4.1 Hasil Pengujian Sensor Tegangan

NO	Sumber tegangan (V)	Pengukuran Sumber tegangan (V)	Pembacaan Sensor (V)	Error(%)
1	205	205	203	0,9
2	201	201	197	1,9
3	189	189	190	0,5
4	193	193	189	2
5	185	185	184	0,5
Jumlah % dalam pengukuran				5.8
Presentase kesalahan dalam %				1.1



Gambar 4.1.Hasil pengukuran Tegangan dengan multimeter digital



Gambar 4.2.Hasil pembacaan sensor tegangan

4.1.5. Analisa Pengujian

Untuk Mencari presentase nilai kesalahan (% error) dari hasil pengujian terhadap pengukuran dapat dirumuskan sebagai berikut:

Perhitungan nilai eror pada sensor tegangan dapat dicari dengan persamaan

$$\begin{aligned}
 \%Error &= \frac{|OutputSensor - Pengukuran|}{Pengukuran} \times 100\% \\
 &= \frac{|203 - 205|}{205} \times 100\% \\
 &= \frac{|-2|}{205} \times 100\% \\
 &= 0.009 \times 100\% \\
 &= 0,9 \%
 \end{aligned}$$

Sehingga didapatkan persen error rata-rata :

$$\begin{aligned}
 \%Error &= \frac{jumlah\ kesalahan\ \%}{jumlah\ pengujian} \\
 \%Error &= \frac{5,8}{5} \\
 &= 1.1\%
 \end{aligned}$$

Berdasarkan dari tabel 4.1 dapat dilihat presentase kesalahan terbesar adalah 1.9 % sedangkan kesalahan rata – rata pada pengujian ini adalah 1.1 % dengan kesalahan kurang dari 2% maka pada rangkaian sensor tegangan dapat dikatakan bekerja dengan baik sesuai dengan aplikasi yang telah direncanakan.

4.2.Pengujian Arduiono mega2560

4.2.1.Tujuan Pengujian Arduiono mega2560

Pengujian ini dilakukan untuk mengetahui apakah rangkaian Arduino Mega2560 berkerja dengan baik.

4.2.2.Peralatan Yang Digunakan

- 1. AVO meter
- 2. Power suppley
- 3. Arduino mega2560
- 4. Personal computer
- 5. Software arduino

4.2.3.Prosedur Pengujian arduino mega2560

- 1. Pengujian pin 13 pada arduino mega.
- 2. Persiapkan arduino mega2560.
- 3. Upload program ke arduino.
- 4. Ukur tegangan pada pin 13.

Tabel 4.2 Hasil output pengukuran arduino

Logika pin 13	Tegangan Pin Digital Arduino (Volt)	Status pin 13
0	0	OFF
1	4.93	ON



Gambar 4.3 pengukuran pada pin 13 arduino

4.3.Pengujian Rangkaian Trafo Arus CST-1020

4.3.1.Tujuan Pengujian Trafo Arus CST-1020

Pengujian ini dilakukan untuk mengetahui apakah Trafo arus (CT) dapat dibaca oleh mikrokontroller Arduino Mega2560.

4.3.2.Peralatan Yang Digunakan

1. AVO meter
2. Rangkaian ADE7753
3. Trafo Arus Triad CST-1020 20A
4. Beban Lampu
5. Power supplay
6. Arduino mega2560
7. Personal computer
8. Software Arduino
9. Lcd 16x4

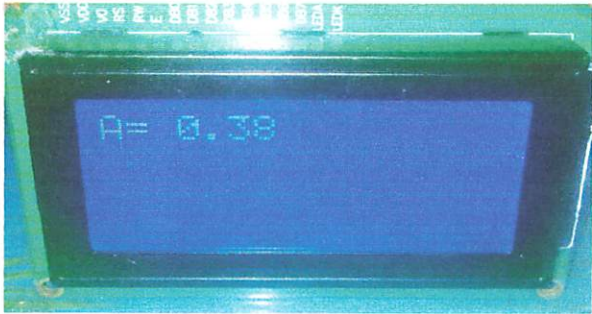
4.3.3.Prosedur Pengujian Trafo Arus CST-1020

1. Pengujian Trafo Arus (CT) pada arduino mega 2560.
2. Persiapkan rangkaian ade7753
3. Sambungkan pin ade7753 ke arduino
4. Upload program ke arduino
5. Amati perubahan arus pada LCD.
6. Amati dan Catat hasil pengukuran AVO dan pembacaan sensor.
7. Bandingkan hasil pengukuran dan pembacaan.

4.3.4.Hasil Pengujian Trafo Arus CST-1020

Tabel 4.3 Hasil Pengujian Trafo Arus CST-1020

NO	Beban	Pengukuran Arus (A)	Pembacaan Sensor (A)	Error(%)
1	0	0.00	0.00	0
2	100	0.40	0.38	5
3	200	0.82	0.80	2.4
4	400	1.64	1.61	1.8
5	450	1.90	1.90	0
Jumlah % dalam pengukuran				9.2
Presentase kesalahan dalam %				1.8



Gambar 4.4 Hasil pembacaan sensor dengan beban 100watt



Gambar 4.5 Hasil Pembacaan arus dengan multimeter digital menggunakan beban 100watt

4.3.5. Analisa Pengujian

Untuk mencari presentase nilai kesalahan (% error) dari hasil pengujian terhadap pengukuran dapat dirumuskan sebagai berikut:

Perhitungan nilai error pada Trafo Arus CST-1020 dapat dicari dengan persamaan

$$\%Error = \frac{|Output\ sensor - pengukuran|}{Pengukuran} \times 100\%$$

$$\begin{aligned}\%Error &= \frac{|1.61 - 1.64|}{1.64} 100\% \\ &= 1.8\%\end{aligned}$$

Sehingga didapatkan persen error rata-rata :

$$\%Error = \frac{jumlah\ keseluruhan\ \%}{jumlah\ pengujian}$$

$$\begin{aligned}\%Error &= \frac{9.2}{5} \\ &= 1.8\%\end{aligned}$$

4.4 Pengujian LCD 16x4

4.4.1 Tujuan Pengujian LCD 16x4

Pengujian ini dilakukan untuk mengetahui apakah LCD dapat menampilkan karakter yang di inputkan mikrokontroller Arduino Mega 2560.

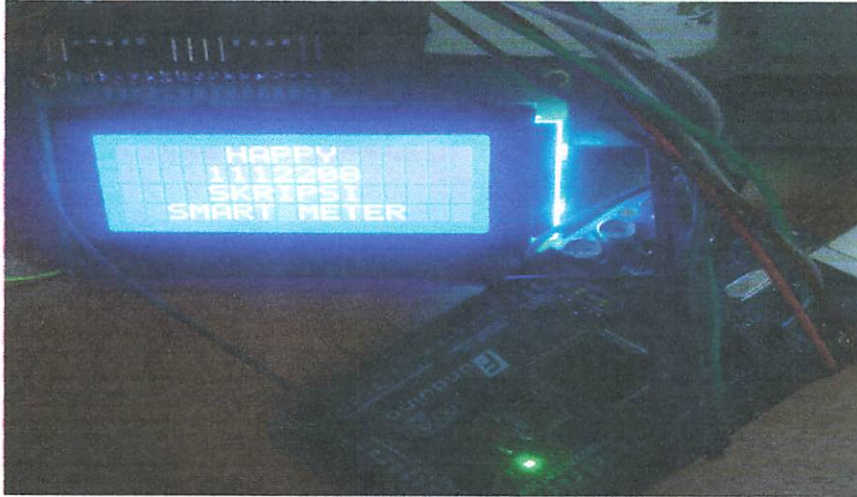
4.4.2.Peralatan Yang Digunakan

1. Arduino mega2560
2. Software Arduino
3. Personal computer
4. LCD 16x4
5. Catu daya 5V

4.4.3.Prosedur Pengujian LCD 16x4

1. Sambungkan pin LCD ke Pin digital Arduino
2. Menghubungkan pin vcc dan pin ground dengan power supply 5 volt
3. Amati karakter yang muncul apakah sesuai dengan apa yang di inputkan pada program.

4.4.3. Hasil Pengujian LCD 16x4



Gambar 4.6 Hasil Pengujian LCD 16x4

Ada beberapa hal yang perlu mendapat perhatian penuh pada saat pengujian sistem minimum ini. Diantaranya adalah masalah kabel konektor, kabel konektor yang digunakan terutama pada LCD haruslah benar-benar terhubung dengan baik. jika tidak maka data yang dikirim ke LCD akan mengalami losing dan LCD tidak bisa bekerja secara maksimal. Dari hasil pengujian LCD pada skripsi ini, LCD menampilkan huruf sesuai dengan apa yang diprogram.

4.5 Pengujian Xbee

4.5.1 Tujuan Pengujian Xbee

Pengujian ini dilakukan untuk mengetahui apakah pengiriman data secara wireless dapat dikirim ke pc dengan baik.

4.5.2.Peralatan Yang Digunakan

1. Arduino mega2560
2. Xbee
3. Software arduino
4. Software XCTU
5. Catu daya 5V
6. PC (Personal Komputer)
7. Lcd 16x4

4.5.3.Prosedur Pengujian Xbee

1. Sambungkan pin Xbee ke Pin digital Arduino
2. Menghubungkan pin Xbee dengan arduino
3. Setting xbee.
4. Upload program ke arduino
5. Amati apakah data yang dikirim dapat diterima.

4.6.Pengujian ADE7753

4.6.1.Tujuan Pengujian ADE7753

Pengujian ini dilakukan untuk mengetahui apakah rangkaian ade7753 bekerja dengan baik dan dapat memperoleh hasil yang dingkan.

4.6.2.Peralatan Yang Digunakan

1. Arduino mega2560.
2. Rangkaian Ade7753.
3. Catu daya 5V.
4. Tegangan AC 220V/50HZ.
5. Lcd 16x4.
6. Lampu, bor listrik
7. PC personal komputer.
8. Cos phi meter.

4.6.3.Prosedur Pengujian ADE7753

1. Rangkaian ade7753
2. Hubungkan pin ade7753 dengan pin arduino.
3. Hubungkan pin Lcd degan Pin digital arduino.
4. Menghubungkan pin vcc dan pin ground dengan power suppley 5 dan 3.3 volt.
5. Menghubungkan rangkaian pembagi tegangan dengan AC 220Volt/50Hz.
6. Menghubungkan rangkain trafo arus CST-1020 dengan beban.
7. Rangkai alat ukur cos phi meter.
8. Upload program ke arduino.
9. Amati dan Catat hasil pengukuran AVO dan pembacaan sensor.
10. Bandingkan hasil pengukuran dan pembacaan.

4.6.4.Hasil Pengujian ade7753 daya aktif

Tabel 4.4 Hasil Pengujian daya aktif ADE7753

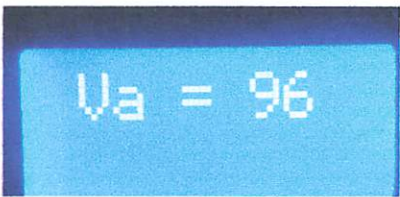
NO	Beban	AVO		Pembacaan Sensor	Error(%)
		Volt	Ampere		
1	0	239	0.00	0	0
2	100	239	0.40	96	4
3	200	239	0.82	194	3
4	400	239	1.64	392	2
5	450	239	1,90	440	2,2
Jumlah % dalam pengukuran					11,2
Presentase kesalahan dalam %					2,2



Gambar 4.9 Hasil Pengukuran arus dengan beban 100 watt



Gambar 4.10 Hasil pembacaan tegangan dengan beban 100watt



Gambar 4.11 Hasil pembacaan sensor dengan beban 100watt

4.6.5. Analisa Pengujian

Untuk Mencari presentase nilai kesalahan (% error) dari hasil pengujian terhadap pengukuran dapat dirumuskan sebagai berikut:

Perhitungan nilai error pada ADE7753 daya aktif dapat dicari dengan persamaan

$$\%Error = \frac{|Output_{sensor} - pengukuran|}{Pengukuran} \times 100\%$$

$$\begin{aligned}\%Error &= \frac{100 - 96}{100} \times 100\% \\ &= 4\%\end{aligned}$$

Sehingga didapatkan persen error rata-rata :

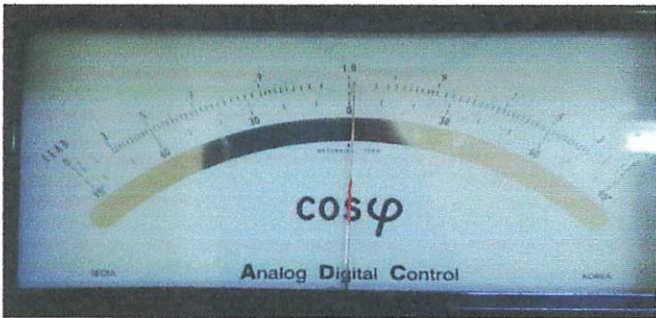
$$\%Error \text{ Rata-rata} = \frac{jumlah_{keseluruhan} \%}{jumlah_{pengujian}}$$

$$\begin{aligned}\%Error &= \frac{11,2}{5} \\ &= 2,2\%\end{aligned}$$

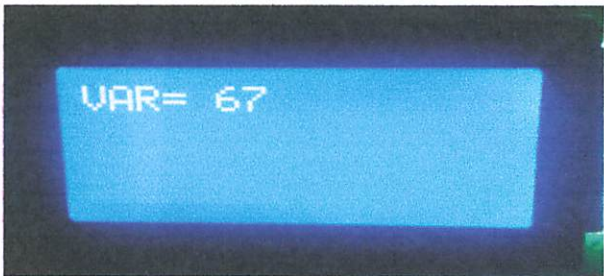
4.6.6.Hasil Pengujian ade7753 daya reaktif

Tabel 4.5 Hasil Pengujian daya reaktif ADE7753

NO	Jenis Beban	Perhitungan (VAR)	Pembacaan Sensor (VAR)	Error(%)
1	Bor listrik	63	67	6.3
2	Kipas angin	20	24	6
3	Monitor	37	38	2.7
4	Gerindra	172	180	4.6
Jumlah % dalam pengukuran				19.6
Presentase kesalahan dalam %				4,9



Gambar 4.12 Hasil Pengukuran daya reaktif



Gambar 4.13 Hasil Pembacaan sensor

4.6.7. Analisa Pengujian

Untuk Mencari presentase nilai kesalahan (% error) dari hasil pengujian terhadap pengukuran dapat dirumuskan sebagai berikut:

Perhitungan nilai error pada ADE7753 daya reaktif dapat dicari dengan persamaan

$$\%Error = \frac{|Output\ sensor - pengukuran|}{Pengukuran} \times 100\%$$

$$\begin{aligned}\%Error &= \frac{67-63}{63} \times 100\% \\ &= 6,3\%\end{aligned}$$

Sehingga didapatkan persen error rata-rata :

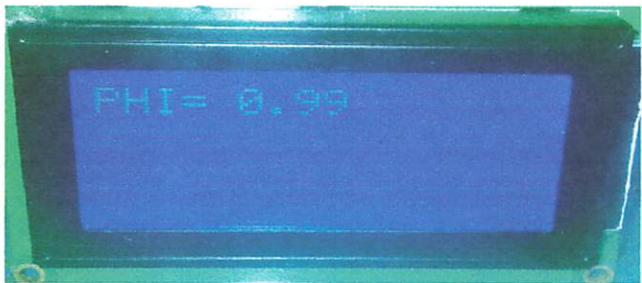
$$\%Error = \frac{jumlah\ kesalahan\ \%}{jumlah\ pengujian}$$

$$\begin{aligned}\%Error &= \frac{19,6}{4} \\ &= 4,9\%\end{aligned}$$

4.6.8.Hasil Pengujian ade7753 cosphi

Tabel 4.6 Hasil Pengujian cosphi ADE7753

NO	Jenis Beban	Pengukuran cosphi	Pembacaan Sensor (cosphi)	Error(%)
1	Solder	0.99	0.97	2.0
2	Lampu pijar	0.99	0.99	0
3	Bor listrik	0.99	0.96	3.0
4	Seterika	0.98	0.95	0
5	Lampu TL	0.27	0.28	3.7
Jumlah % dalam pengukuran				8.7
Presentase kesalahan dalam %				1.7



Gambar 4.14 Hasil Pembacaan sensor dengan beban lampu pijar



Gambar 4.15 Hasil Pengukuran dengan cosphi meter menggunakan beban lampu pijar

4.6.9. Analisa Pengujian

Untuk Mencari presentase nilai kesalahan (% error) dari hasil pengujian terhadap pengukuran dapat dirumuskan sebagai berikut:

Perhitungan nilai error pada ADE7753 cosphi dapat dicari dengan persamaan

$$\%Error = \frac{|\text{Output sensor} - \text{pengukuran}|}{\text{Pengukuran}} \times 100\%$$

$$\begin{aligned} \%Error &= \frac{0.97 - 0.99}{0.99} \times 100\% \\ &= 2.0\% \end{aligned}$$

Sehingga didapatkan persen error rata-rata :

$$\%Error = \frac{\text{jumlah keseluruhan \%}}{\text{jumlah pengujian}}$$

$$\begin{aligned} \%Error &= \frac{8.7}{5} \\ &= 1.7\% \end{aligned}$$

4.7. Pengujian Driver Relay

4.7.1.Tujuan Pengujian Driver Relay

Pengujian dari driver relay yaitu untuk mengetahui apakah driver relay dapat bekerja dengan baik sesuai dengan perintah dari mikrokontroller dan untuk mengetahui kerja dari relay yang digunakan sebagai pengontrol ada tidaknya aliran listrik ke beban.

4.7.2.Peralatan Yang Digunakan

- 1. Arduino mega 2560
- 2. Personal Computer
- 3. Modul Driver Relay
- 4. Power supllly 5 volt
- 5. Multimeter Digital

4.7.3.Prosedur Pengujian driver relay

- 1. Menghubungkan PIN driver relay dengan pin digital arduino
- 2. Menghubungkan PINvcc dan ground dengan power supply 5 volt
- 3. Memprogram Arduino dengan memberikan logic 0 dan logic 1 untuk menguji Modul Driver Relay
- 4. Mencatat hasil pengujian yang dilakukan

4.7.4.Hasil Pengujian

Tabel 4.7 Data Pengamatan Driver Relay

Logika Pin Arduino	Tegangan Pin Digital Arduino (Volt)	Status Relay
0	0	OFF
1	4.93	ON



Gambar 4.16 tegangan output pada pin arduino untuk fungsi relay

Pada tabel 4.4 terlihat Mikrokontroller diprogram saat logika PIN digital '0' maka relay akan off dan jika mikrokontroller berlogika '1' maka relay akan on.

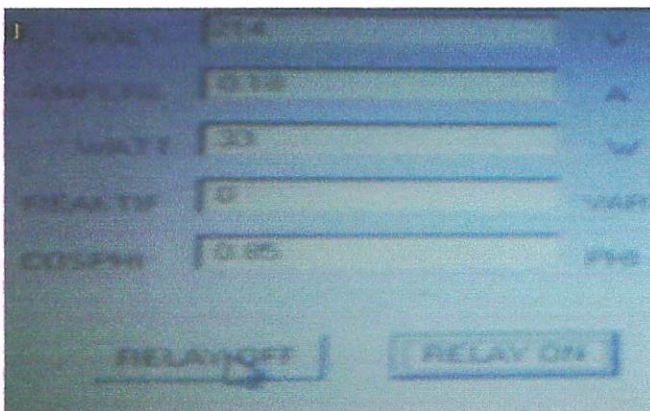
4.8 Hasil Pengujian Keseluruhan

Setelah melakukan pengujian terhadap masing-masing blok rangkaian, selanjutnya adalah melakukan pengujian sistem secara keseluruhan. Pengujian ini dilakukan dengan cara menggabungkan seluruh blok rangkaian menjadi satu, sehingga sistem dapat diuji dengan lengkap.

Sistem ini terdiri dari sensor tegangan untuk mendeteksi tegangan, trafo arus sebagai mendeteksi arus. Sensor yang di pakai untuk mendeteksi tegangan, arus, cosphi, daya aktif dan daya reaktif adalah IC ADE7753.



Gambar 4.17 tampilan hasil pengukuran



Gambar 4.18 tampilan layout hasil pengukuran

Tabel 4.8 Data Pengamatan daya yang dikirim pada pc secara wireless

NO	Beban	Jarak (meter)	Pembacaan Beban yang diterima oleh PC	Status pembacaan beban yang dikirim
1	100	5	96	Terkirim
2	100	10	96	Terkirim
3	100	20	96	Terkirim
4	100	30	96	Terkirim
5	100	60	0	Tidak Terkirim

BAB V

PENUTUP

5.1 kesimpulan

Setelah perencanaan dan pembuatan sistem kemudian pengujian dan analisa, penulisan menyampaikan bebeapa kesimpulan dan saran yaitu sebagai berikut :

1. Pada IC ADE7753 mampu menampilkan data informasi berupa tegangan.
2. Pada IC ADE7753 mampu menampilkan data informasi berupa arus beban.
3. Pada IC ADE7753 mampu menampilkan data informasi berupa daya.
4. Pengiriman data sensor menggunakan Xbee yang mampu mengirim secara jarak jauh
5. Presentase error rata-rata pada pengujian sensor tegangan mencapai 1,1%.
6. Presentase error rata-rata pada pengujian trafo arus mencapai 1,8%.
7. Presentase error rata-rata pada pengujian IC ADE7753 untuk daya aktif mencapai 2,2%.
8. Presentase error rata-rata pada pengujian IC ADE7753 untuk daya reaktif mencapai 4,9%.
9. Presentase error rata-rata pada pengujian IC ADE7753 untuk cosphi mencapai 1,7%.

5.2 Saran

1. Pada pengembangan selanjutnya perlu dipertimbangkan untuk nilai beban yang besar.
2. Menggunakan transformator sebagai filter pada rangkaian sensor tegangan.
3. Pada pembangan Xbee untuk pengiriman data bisa secara multi point.
4. Pada pengembangan selanjutnya bisa ditambahkan untuk control dan monitoring agar sistem smart meter lebih baik.

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LAMPIRAN



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4. Konsentrasi : TEKNIK ELEKTRONIKA

Judul : **SMART METER MENGGUNAKAN IC ADE7753
DENGAN KONEKSI WIRELESS UNTUK PENGUKUR
DAYA LISTRIK PADA SISTEM SMART GRID**

Dipertahankan dihadapan Majelis Penguji Skripsi Jenjang Strata Satu (S-1) pada :

Hari : Rabu

Tanggal : 19 Agustus 2015

Dengan Nilai : 84,6(A)

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Ketua Majelis Penguji

Sekretaris Majelis Penguji

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Tanggal : 24 September 2015

Telah dilakukan perbaikan skripsi oleh :

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1.	Pengujian jarak pengiriman data	Eng

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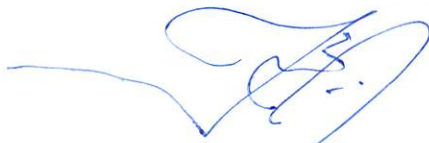
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Komsentrasi : Teknik Elektronika
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No	Materi Perbaikan	Keterangan
1.	Calibrasi	
2	Smart di masukan ke saran	

Dosen Penguji II



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Tanggal, 28 Mei 2015

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ITN MALANG

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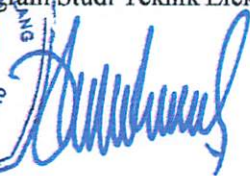
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Yang bertanda tangan di bawah ini:

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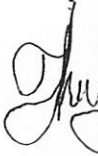
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Demikian surat pernyataan ini saya buat, dan apabila di kemudian hari ada pelanggaran atas surat pernyataan ini, saya bersedia menerima sanksinya.

Malang, September 2015

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NIM : 1112208



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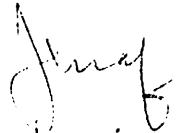
Dengan ini kami mengajukan permohonan untuk mendapatkan persetujuan untuk membuat SKRIPSI Tingkat Sarjana. Untuk melengkapi permohonan tersenut, bersama ini kami lampirkan persyaratan-persyaratan yang harus dipenuhi.

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2. Telah lulus dan menyerahkan laporan Praktek Kerja (.....✓.....)
3. Telah lulus seluruh mata kuliah keahlian (MKB) sesuai konsentrasinya (.....✓.....)
4. Telah menempuh matakuliah > 134 sks dengan IPK > 2 dan tidak ada nilai E (.....✓.....)
5. Telah mengikuti secara aktif kegiatan seminar Skripsi yang diadakan Jurusan (.....✓.....)
6. Memenuhi persyaratan administrasi (.....✓.....)

Demikian permohonan ini untuk mendapatkan penyelesaian lebih lanjut dan atas perhatiannya kami ucapkan terima kasih.

Telah diteliti kebenarannya data tersebut diatas
Recording Teknik Elektro S-I

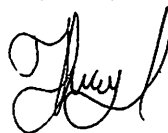

(.....pro. Ibrakayari.....)

Disetujui
Ketua Prodi Teknik Elektro S-I

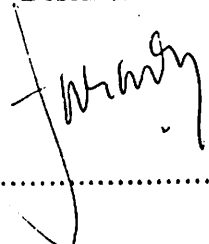

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(.....)

Catatan:

Bagi mahasiswa yang telah memenuhi persyaratan mengambil SKRIPSI agar membuat proposal dan mendapat persetujuan dari Ketua Prodi T. elektro S-I

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Nama Pembimbing : Ibrahim Ashari, ST, MT
Judul Skripsi : SMART METER MENGGUNAKAN IC ADE7753 DENGAN KOMUNIKASI WIRELESS UNTUK PENGUKUR DAYA LISTRIK PADA SISTEM SMART GRID

Minggu Ke-	Hari, Tanggal	Waktu Bimbingan	Materi Bimbingan	Paraf
1	Rabu- 10 Mei 2015	13.00 - 13.15	acc Bab I acc Bab II	
2	Kamis 21 Mei 2015	11.00 - 11.15	acc Bab III	
3	6 Jun 2015	15.00 15.15	Laporan progres tugas akhir skripsi	
4	7 Jun 2015	13.00 13.20	acc Bab IV	
5	15 Jun 2015	10.00 10.15	acc Bab V	
6	1/8/2015		acc makalah/laporan skripsi	
7				

Malang, 28 April 2015
Pembimbing

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NiM : 1112208
Nama Pembimbing : Dr.ENG.Aryuanto soedtdjo.,ST,MT
Judul Skripsi : SMART METER MENGGUNAKAN IC ADE7753 DENGAN KOMUNIKASI WIRELESS UNTUK PENGUKUR DAYA LISTRIK PADA SISTEM SMART GRID

Minggu Ke-	Hari, Tanggal	Waktu Bimbingan	Materi Bimbingan	Paraf
1	Rabu 13/05/15	14.00	Bab Skema & PCB	
2	Rabu 13/05/15	14.15	Bab 1 - 3	
3	Kamis 21/5	13.00	Perancangan ALG + X Bus t t	
4	Rabu 10/6	14.00	Bab 3	
5	7/7	13.00	Bab 4	
6				
7				

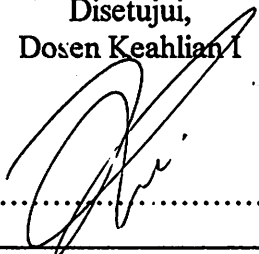
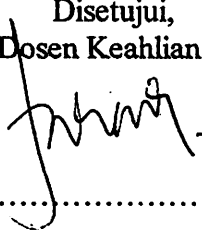
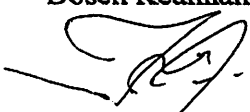
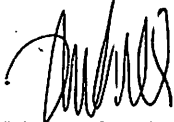
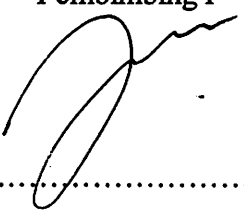
Malang, 28 April 2015

Pembimbing

Dr. Eng Aryuanto soedtdjo.,ST, MT
NIP.Y. 1030800417



BERITA ACARA SEMINAR PROPOSAL SKRIPSI
PROGRAM STUDI TEKNIK ELEKTRO S-1
Konsentrasi : Teknik Elektronika

Nim	: 1112208	
Nama	: HAPPY PRA ETIYONO	
Konsentrasi Jurusan	: Teknik Elektronika	
Jadwal Pelaksanaan:	Waktu	Tempat
09 April 2015	09.00	III.1.5
Judul proposal yang diseminarkan Mahasiswa	SMART METER MENGGUNAKAN IC ADE 7753 DENGAN KONEKSI WIFI UNTUK PENGUKUR DAYA LISTRIK PADA SISTEM SMART GRID	
Perubahan judul yang diusulkan oleh Kelompok Dosen Keahlian	wifi → wireless.	
Catatan : - Teori tgg Pengukuran daya oleh IC ADE 7753		
Catatan :		
Persetujuan judul Skripsi		
Disetujui, Dosen Keahlian I  (.....)	Disetujui, Dosen Keahlian II  (.....)	Disetujui, Dosen Keahlian III  (.....)
Mengetahui, Ketua Program Studi Teknik Elektro S-1  M. Ibrahim Ashari, ST, MT NIP. P 1030100358	Disetujui, Calon Dosen Pembimbing ybs	
	Pembimbing I  (.....)	Pembimbing II  (.....)

BERITA ACARA RAPAT PERSI TUJUAN JUDUL/PROPOSAL SKRIPSI

PROGRAM STUDI TEKNIK ELEKTRO S-1

Konsentrasi: Teknik Elektronika SI

tanggal: 1 APRIL - 2015

NIM	1112208
Nama	Happy Prashyano
Judul yang diajukan	Smart meter menggunakan IC ADE 7753 Dg koneksi wifi utk pengukur daya listrik. Pd sistem smart grid.
Disetujui/Ditolak	
Catatan:	
Pembimbing yang diusulkan:	
1. Aryanto	
2. Ibrahim A.	
Menyetujui	
1. Koordinator Dosen Kelompok Keahlian	
	
2. Dosen Kelompok Keahlian (Terlampir)	

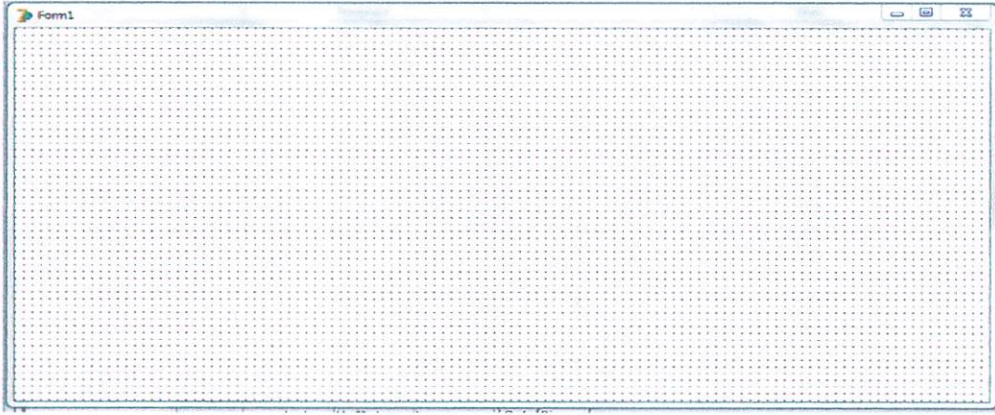
Coret yang tidak perlu

BERITA ACARA SEMINAR PROGRESS SKRIPSI PROGRAM STUDI TEKNIK ELEKTRO S1

KONSENTRASI		Elektronika	
Nama Mahasiswa	HAPPY PRASETIYONO	NIM	1112208
Keterangan	Tanggal	Waktu	Tempat / Ruang
Pelaksanaan			
Judul Skripsi	SMART METER MENGGUNAKAN IC ADE 7753 DENGAN KONEKSI WIFI UNTUK PENGUKUR DAYA LISTRIK PADA SISTEM SMART GRID		
Perubahan Judul			
Catatan : Revisi skripsi diteliti lagi.			
Mengetahui, Ketua Jurusan.  M. Ibrahim Ashari, ST, MT		Disetujui, Dosen Pembimbing Pembimbing I  Dr. Eng. Aryanto Soetedjo, ST, MT Pembimbing II:  M. Ibrahim Ashari, ST, MT	

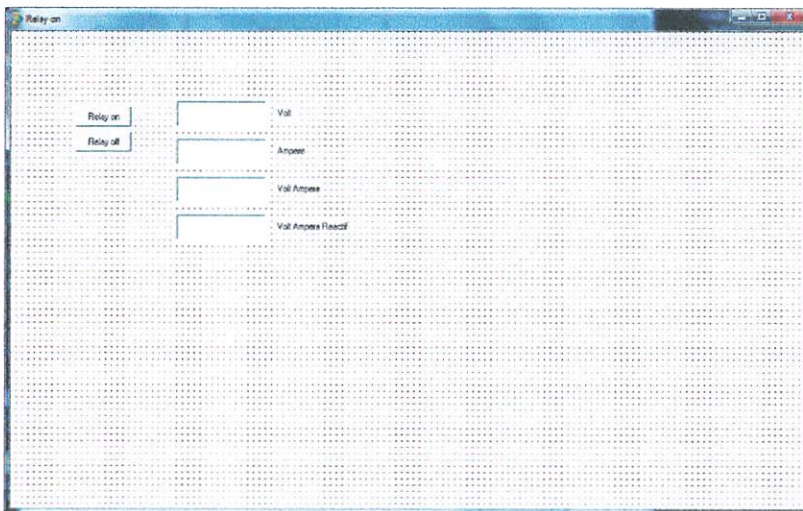
3.9.Perancangan Aplikasi delphi

Untuk membuat tampilan form aplikasi kita buka program *delphi7* dan secara otomatis form aplikasi akan tampil dan siap untuk di gunakan. Seperti yang terlihat pada gambar 3.10 di bawah:



Gambar 3.10 Form Kerja Aplikasi

Setelah membuka Delphi dan form kerja maka langkah selanjutnya adalah penambahan komponen komponen yang akan di gunakan. Dan komponen-komponen yang di maksud adalah komponen yang ada pada table komponen yaitu komponen Button, Edit, Serial, Label, dan di beri label sesuai yang akan kita buat yang mana setelah di tambahkan dan di beri label maka tampilan aplikasi akan terlihat seperti pada gambar 3.11.



Gambar 3.11 Aplikasi

Formulir Perbaikan Ujian Skripsi

Pelaksanaan Ujian Skripsi Jenjang Strata 1 Jurusan Teknik Elektro Konsentrasi T.Energi Listrik, /
ronika, /T. Komputer, / T.Telekomunikasi, Maka Perlu Adanya Perbaikan Skripsi Untuk Mahasiswa:

: HAPPY P.
: 11.12.208

kan Meliputi :

Calibration

Smart ? → dimasukkan ke layar !

Malang, ...20



(.....I.....)

Formulir Perbaikan Ujian Skripsi

Pelaksanaan Ujian Skripsi Jenjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik, /
ronika, /T. Komputer, / T. Telekomunikasi, Maka Perlu Adanya Perbaikan Skripsi Untuk Mahasiswa:

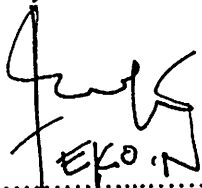
: HAPPY.P

: 1112208

kan Meliputi :

urbaikan pengujian utle jarak pengiriman data

Malang, 19 - 08 - 2015


(.....EKO.N.....)

```

#include "ADE7753.h"

#include<Wire.h>

#include <avr/io.h>

#include<SPI.h>

#include <SoftwareSerial.h>

#include<math.h>

////////////////////////////////////

#define RELAY1 11

#define RELAY2 12

#define tXbee 3          // SoftSerial Txpin

#define rXbee 2          // SoftSerial Rxdpin

#define PI 3.14159265

SoftwareSerial wifi(rXbee,tXbee);

#include <LiquidCrystal.h>

LiquidCrystal lcd(7, 6, 5, 4, 8,9 );

////////////////////////////////////

#define BUFFER_SIZE 4

#define SEND_TO_DB 1

#define RESET_DATA 1


#define slaveSelectPin 10

#define WRITE 0x80

#define CLKIN 1

#define SAG_PIN 2

#define IRQ_PIN 3

#define RESET_PIN 5


/* register adresses */

/* 24 bit */


#define Waveform 0x01 /* waveform sample register*/

#define AENERGY 0x02 /* active energy register */

```

```
#define RAENERGY 0x03
#define LAENERGY 0x04  /* line accumulation active energy register*/
#define VAENERGY 0x05  /* apparent energy register */
#define RVAENERGY 0x06
#define LVAENERGY 0x07
#define LVARENERGY 0x08
#define IRMS 0x16
#define VRMS 0x17
#define IPEAK 0x22
#define VPEAK 0x24
////////////////////////////////////
String inputString = "";    // a string to hold incoming data
unsigned long metered_data[5];
float meters[3];
float CALL[2];
boolean metering ;
boolean stringComplete = false; // whether the string is complete
long r1,r2,r3;

void setup()
{
  pinMode(RELAY1, OUTPUT);
  pinMode(RELAY2, OUTPUT);
  pinMode(rXbee,INPUT);
  pinMode(tXbee,OUTPUT);
  pinMode(slaveSelectPin, OUTPUT);
  pinMode(RESET_PIN, OUTPUT);
  lcd.begin(20, 4);
  lcd.clear();
  inputString.reserve(200);

  digitalWrite(slaveSelectPin, HIGH);
```

```
digitalWrite(RESET_PIN, HIGH);

SPI.setDataMode(SPI_MODE1);
SPI.setClockDivider(SPI_CLOCK_DIV32);
SPI.setBitOrder(MSBFIRST);
SPI.begin();

Serial.begin(9600);
delay (100);
}
////////////////////////////////////
void loop ()
{
digitalWrite(RELAY2,HIGH);    // Turns Relay Off
get_sample();
}

void reactive()
{
ADE7753 meter = ADE7753();

meter.setMode(0x0080); //Se inicia el modo de acumulación de energía.
meter.setLineCyc(10); //Se fija el número de medios ciclos ocupados en la medición. 10 medio ciclos
equivalen a 1 segundo trabajando en una red de 50 Hz (Chile).

//r1=meter.getReactiveEnergy(); //Extrae la energía activa acumulada, sincronizando la medición con
los cruces por cero de la señal de voltaje.

meter.setMode(0x0080);
meter.setLineCyc(20); // 0,2 segundos de medición.
r2=meter.getReactiveEnergy();

meter.setMode(0x0080);
meter.setLineCyc(30); // 0,3 segundos de medición.
```

```
    r3=meter.getReactiveEnergy();
}
////////////////////////////////////
void enableMeter(void)
{
    digitalWrite(slaveSelectPin, LOW);
}
////////////////////////////////////
void disableMeter(void)
{
    digitalWrite(slaveSelectPin, HIGH);
}
////////////////////////////////////
void enableShield(void)
{
    metering = true;
    digitalWrite(RESET_PIN, HIGH);
}
////////////////////////////////////
void disableShield(void)
{
    metering = false;
    digitalWrite(RESET_PIN, LOW);
}
////////////////////////////////////
unsigned long readREG24(int adress)
{
    enableMeter();
    unsigned long reg, a, b;
    delayMicroseconds(5);
    SPI.transfer(adress);
    delayMicroseconds(5);
```

```
reg = SPI.transfer(0x00);  
a = SPI.transfer(0x00);  
b = SPI.transfer(0x00);  
delayMicroseconds(5);  
disableMeter();
```

```
reg = reg << 8;  
reg = reg + a;  
reg = reg << 8;  
reg = reg + b;
```

```
return reg;
```

```
}
```

```
void serialEvent() {
```

```
  while (Serial.available()) {
```

```
    char inChar = (char)Serial.read();
```

```
    inputString += inChar;
```

```
    if (inChar == '\n') {
```

```
      stringComplete = true;
```

```
    }
```

```
  }
```

```
}
```

```
////////////////////////////////////
```

```
void get_sample()
```

```
{
```

```
  SPI.setDataMode(SPI_MODE1);
```

```
  SPI.setClockDivider(SPI_CLOCK_DIV32);
```

```
  SPI.setBitOrder(MSBFIRST);
```

```
  SPI.begin();
```

```
  reactive();
```

```
  serialEvent(); //call the function
```

```
if (stringComplete) {
if (inputString == "ON\n")
{
digitalWrite(RELAY2,HIGH);
digitalWrite(RELAY1,HIGH);
Serial.println("2 ON");
}
if (inputString == "OFF\n")
{
digitalWrite(RELAY2,LOW);
digitalWrite(RELAY1,LOW);

Serial.println("2 OFF");
}
inputString = "";
stringComplete = false;
}
////////////////////////////////////
//monitoring tegangan
delay(1800);
lcd.clear();
Serial.println("AWAL");
if(metered_data[1]<=178)
{
Serial.print("V = ");
Serial.println("0");
lcd.setCursor(0,0);
lcd.write("V=");
lcd.print("0");
}
else
{
```

////////////////////////////////////

```
if(meters[2]>=4.00)
{
    digitalWrite(RELAY1,LOW);
}
```

////////////////////////////////////

```
if(meters[2]<=0.03)
{
    Serial.print("A = ");
    Serial.println("0.00");
    lcd.setCursor(9,0);
    lcd.write("A=");
    lcd.print("0.00");
}
```

```
else
{
    Serial.print("A = ");
    Serial.println((meters[2]),2);
    lcd.setCursor(9,0);
    lcd.write("A=");
    lcd.print((meters[2]),2);
}
```

////////////////////////////////////

```
//monitoring daya aktif
```

```
Serial.print("W = ");
Serial.println(metered_data[2]);
lcd.setCursor(9,1);
lcd.write("W=");
lcd.print(metered_data[2]);

////////////////////////////////////

//monitoring daya semu
//Serial.print("VA =");
//Serial.println(metered_data[3]);
//lcd.setCursor(4,2);
//lcd.write("VA= ");
//lcd.print(readREG24(VAENERGY));

////////////////////////////////////

//monitoring daya reaktif
Serial.print("VAR= ");
Serial.println(metered_data[4]);
lcd.setCursor(0,1);
lcd.write("VAR=");
lcd.print(metered_data[4]);

////////////////////////////////////

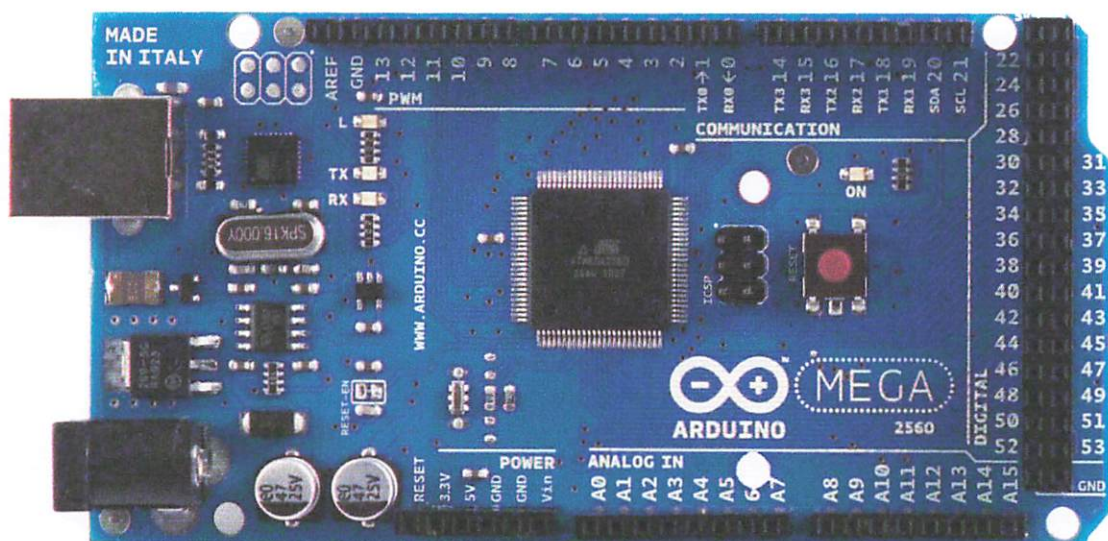
//monitoring cosphi
Serial.print("PHI= ");
Serial.println(meters[3],2);
lcd.setCursor(-4,2);
lcd.write("PHI=");
lcd.print(meters[3],2);

////////////////////////////////////

metered_data[1] = readREG24(VRMS) * 1.414*0.003502;//0.00321;// 0.00238//0.00178;//*
0.00247;// * 0.00218;//kalibrasi : vrms/1.414/1000; atau vrms * 0.006865
metered_data[2] = readREG24(RAENERGY) * 0.001885*3600;//0.001885;kalibrasi contoh
220x10x19.98/3600/28363= hasil / 3600= finish terus nilai finish dikali 3600
metered_data[3] = readREG24(RVAENERGY) * 0.001*3600;//0.000190//0.0001
```

```
metered_data[4] = (readREG24(LVARENERGY)*metered_data[2])*CALL[2] ;/* metered_data[2]) *  
CALL[2];  
  
CALL[1]      = acos (meters[3])*180.0/PI;  
CALL[2]      = sin (CALL[1]*PI/180.0);  
  
meters[1] = readREG24(IRMS) * 0.0000112;//KALIBRASI :(PEMBACAAN TEGANGAN/PEMBACAAN  
DAYA AKTIF)= 0,0000112 (PEMBACAAN ARUS * 0,0000112)//  
meters[2] = meters[1];//100 ;  
meters[3] = (metered_data[2]+0.000001)/(metered_data[3]+0.000001);  
  
}
```

Arduino MEGA 2560



Product Overview

The Arduino Mega 2560 is a microcontroller board based on the ATmega2560 ([datasheet](#)). It has 54 digital input/output pins (of which 14 can be used as PWM outputs), 16 analog inputs, 4 UARTs (hardware serial ports), a 16 MHz crystal oscillator, a USB connection, a power jack, an ICSP header, and a reset button. It contains everything needed to support the microcontroller; simply connect it to a computer with a USB cable or power it with a AC-to-DC adapter or battery to get started. The Mega is compatible with most shields designed for the Arduino Duemilanove or Diecimila.

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Enviromental Policies
half sqm of green via Impatto Zero®

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Technical Specification

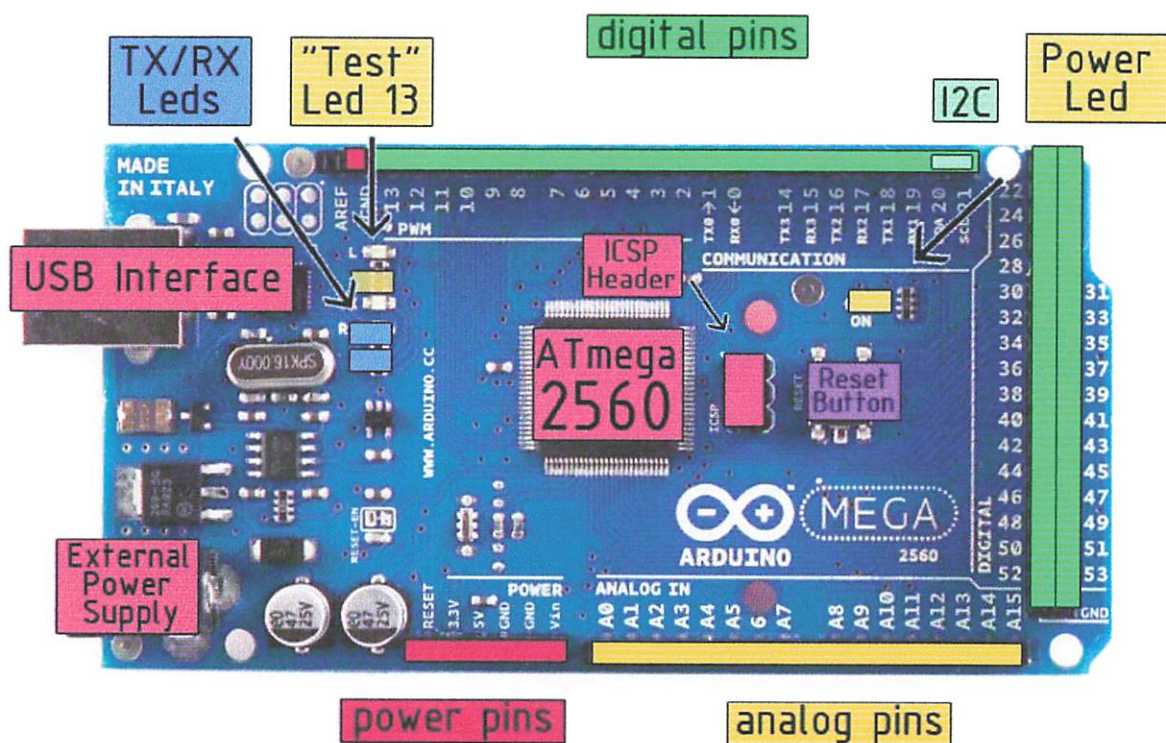


EAGLE files: [arduino-mega2560-reference-design.zip](#) Schematic: [arduino-mega2560-schematic.pdf](#)

Summary

Microcontroller	ATmega2560
Operating Voltage	5V
Input Voltage (recommended)	7-12V
Input Voltage (limits)	6-20V
Digital I/O Pins	54 (of which 14 provide PWM output)
Analog Input Pins	16
DC Current per I/O Pin	40 mA
DC Current for 3.3V Pin	50 mA
Flash Memory	256 KB of which 8 KB used by bootloader
SRAM	8 KB
EEPROM	4 KB
Clock Speed	16 MHz

the board



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Power

The Arduino Mega2560 can be powered via the USB connection or with an external power supply. The power source is selected automatically. External (non-USB) power can come either from an AC-to-DC adapter (wall-wart) or battery. The adapter can be connected by plugging a 2.1mm center-positive plug into the board's power jack. Leads from a battery can be inserted in the Gnd and Vin pin headers of the POWER connector.

The board can operate on an external supply of 6 to 20 volts. If supplied with less than 7V, however, the 5V pin may supply less than five volts and the board may be unstable. If using more than 12V, the voltage regulator may overheat and damage the board. The recommended range is 7 to 12 volts.

The Mega2560 differs from all preceding boards in that it does not use the FTDI USB-to-serial driver chip. Instead, it features the Atmega8U2 programmed as a USB-to-serial converter.

The power pins are as follows:

- **VIN.** The input voltage to the Arduino board when it's using an external power source (as opposed to 5 volts from the USB connection or other regulated power source). You can supply voltage through this pin, or, if supplying voltage via the power jack, access it through this pin.
- **5V.** The regulated power supply used to power the microcontroller and other components on the board. This can come either from VIN via an on-board regulator, or be supplied by USB or another regulated 5V supply.
- **3V3.** A 3.3 volt supply generated by the on-board regulator. Maximum current draw is 50 mA.
- **GND.** Ground pins.

Memory

The ATmega2560 has 256 KB of flash memory for storing code (of which 8 KB is used for the bootloader), 8 KB of SRAM and 4 KB of EEPROM (which can be read and written with the [EEPROM library](#)).

Input and Output

Each of the 54 digital pins on the Mega can be used as an input or output, using [pinMode\(\)](#), [digitalWrite\(\)](#), and [digitalRead\(\)](#) functions. They operate at 5 volts. Each pin can provide or receive a maximum of 40 mA and has an internal pull-up resistor (disconnected by default) of 20-50 kOhms. In addition, some pins have specialized functions:

- **Serial: 0 (RX) and 1 (TX); Serial 1: 19 (RX) and 18 (TX); Serial 2: 17 (RX) and 16 (TX); Serial 3: 15 (RX) and 14 (TX).** Used to receive (RX) and transmit (TX) TTL serial data. Pins 0 and 1 are also connected to the corresponding pins of the ATmega8U2 USB-to-TTL Serial chip .
- **External Interrupts: 2 (interrupt 0), 3 (interrupt 1), 18 (interrupt 5), 19 (interrupt 4), 20 (interrupt 3), and 21 (interrupt 2).** These pins can be configured to trigger an interrupt on a low value, a rising or falling edge, or a change in value. See the [attachInterrupt\(\)](#) function for details.
- **PWM: 0 to 13.** Provide 8-bit PWM output with the [analogWrite\(\)](#) function.
- **SPI: 50 (MISO), 51 (MOSI), 52 (SCK), 53 (SS).** These pins support SPI communication, which, although provided by the underlying hardware, is not currently included in the Arduino language. The SPI pins are also broken out on the ICSP header, which is physically compatible with the Duemilanove and Diecimila.
- **LED: 13.** There is a built-in LED connected to digital pin 13. When the pin is HIGH value, the LED is on, when the pin is LOW, it's off.
- **I²C: 20 (SDA) and 21 (SCL).** Support I²C (TWI) communication using the [Wire library](#) (documentation on the Wiring website). Note that these pins are not in the same location as the I²C pins on the Duemilanove.

The Mega2560 has 16 analog inputs, each of which provide 10 bits of resolution (i.e. 1024 different values). By default they measure from ground to 5 volts, though is it possible to change the upper end of their range using the AREF pin and [analogReference\(\)](#) function.

There are a couple of other pins on the board:

- **AREF.** Reference voltage for the analog inputs. Used with [analogReference\(\)](#).
- **Reset.** Bring this line LOW to reset the microcontroller. Typically used to add a reset button to shields which block the one on the board.



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Communication

The Arduino Mega2560 has a number of facilities for communicating with a computer, another Arduino, or other microcontrollers. The ATmega2560 provides four hardware UARTs for TTL (5V) serial communication. An ATmega8U2 on the board channels one of these over USB and provides a virtual com port to software on the computer (Windows machines will need a .inf file, but OSX and Linux machines will recognize the board as a COM port automatically). The Arduino software includes a serial monitor which allows simple textual data to be sent to and from the board. The RX and TX LEDs on the board will flash when data is being transmitted via the ATmega8U2 chip and USB connection to the computer (but not for serial communication on pins 0 and 1).

A [SoftwareSerial library](#) allows for serial communication on any of the Mega's digital pins.

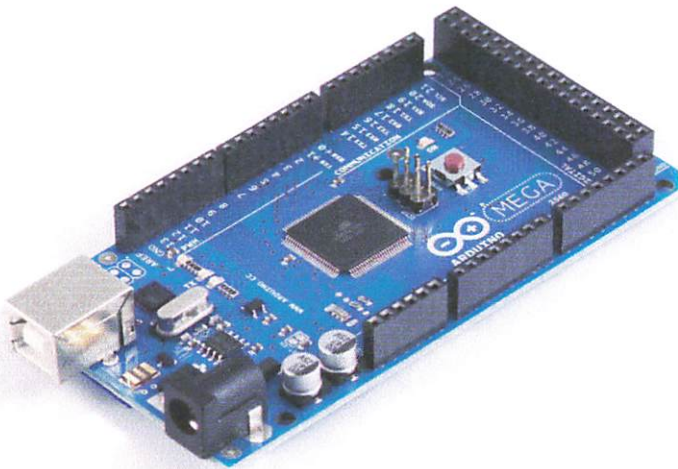
The ATmega2560 also supports I2C (TWI) and SPI communication. The Arduino software includes a Wire library to simplify use of the I2C bus; see the [documentation on the Wiring website](#) for details. To use the SPI communication, please see the ATmega2560 datasheet.

Programming

The Arduino Mega2560 can be programmed with the Arduino software ([download](#)). For details, see the [reference](#) and [tutorials](#).

The ATmega2560 on the Arduino Mega comes preburned with a [bootloader](#) that allows you to upload new code to it without the use of an external hardware programmer. It communicates using the original STK500 protocol ([reference](#), [C header files](#)).

You can also bypass the bootloader and program the microcontroller through the ICSP (In-Circuit Serial Programming) header; see [these instructions](#) for details.



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Automatic (Software) Reset

Rather than requiring a physical press of the reset button before an upload, the Arduino Mega2560 is designed in a way that allows it to be reset by software running on a connected computer. One of the hardware flow control lines (DTR) of the ATmega8U2 is connected to the reset line of the ATmega2560 via a 100 nanofarad capacitor. When this line is asserted (taken low), the reset line drops long enough to reset the chip. The Arduino software uses this capability to allow you to upload code by simply pressing the upload button in the Arduino environment. This means that the bootloader can have a shorter timeout, as the lowering of DTR can be well-coordinated with the start of the upload.

This setup has other implications. When the Mega2560 is connected to either a computer running Mac OS X or Linux, it resets each time a connection is made to it from software (via USB). For the following half-second or so, the bootloader is running on the Mega2560. While it is programmed to ignore malformed data (i.e. anything besides an upload of new code), it will intercept the first few bytes of data sent to the board after a connection is opened. If a sketch running on the board receives one-time configuration or other data when it first starts, make sure that the software with which it communicates waits a second after opening the connection and before sending this data.

The Mega contains a trace that can be cut to disable the auto-reset. The pads on either side of the trace can be soldered together to re-enable it. It's labeled "RESET-EN". You may also be able to disable the auto-reset by connecting a 110 ohm resistor from 5V to the reset line; see [this forum thread](#) for details.

USB Overcurrent Protection

The Arduino Mega has a resettable polyfuse that protects your computer's USB ports from shorts and overcurrent. Although most computers provide their own internal protection, the fuse provides an extra layer of protection. If more than 500 mA is applied to the USB port, the fuse will automatically break the connection until the short or overload is removed.

Physical Characteristics and Shield Compatibility

The maximum length and width of the Mega PCB are 4 and 2.1 inches respectively, with the USB connector and power jack extending beyond the former dimension. Three screw holes allow the board to be attached to a surface or case. Note that the distance between digital pins 7 and 8 is 160 mil (0.16"), not an even multiple of the 100 mil spacing of the other pins.

The Mega is designed to be compatible with most shields designed for the Diecimila or Duemilanove. Digital pins 0 to 13 (and the adjacent AREF and GND pins), analog inputs 0 to 5, the power header, and ICSP header are all in equivalent locations. Further the main UART (serial port) is located on the same pins (0 and 1), as are external interrupts 0 and 1 (pins 2 and 3 respectively). SPI is available through the ICSP header on both the Mega and Duemilanove / Diecimila. **Please note that I²C is not located on the same pins on the Mega (20 and 21) as the Duemilanove / Diecimila (analog inputs 4 and 5).**



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How to use Arduino



Arduino can sense the environment by receiving input from a variety of sensors and can affect its surroundings by controlling lights, motors, and other actuators. The microcontroller on the board is programmed using the [Arduino programming language](#) (based on [Wiring](#)) and the Arduino development environment (based on [Processing](#)). Arduino projects can be stand-alone or they can communicate with software on running on a computer (e.g. Flash, Processing, MaxMSP).

Arduino is a cross-platform program. You'll have to follow different instructions for your personal OS. Check on the [Arduino site](http://arduino.cc/en/Guide/HomePage) for the latest instructions. <http://arduino.cc/en/Guide/HomePage>

Linux Install

Windows Install

Mac Install

Once you have downloaded/unzipped the arduino IDE, you can Plug the Arduino to your PC via USB cable.

Blink led

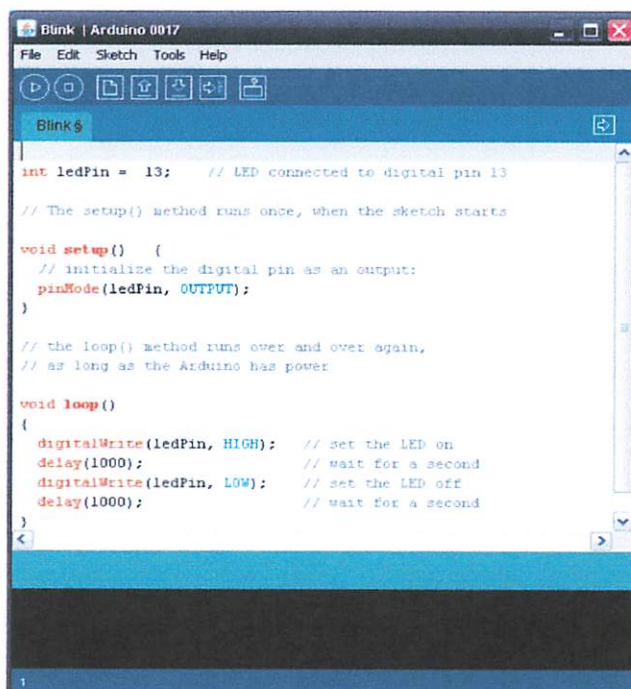
Now you're actually ready to "burn" your first program on the arduino board. To select "blink led", the physical translation of the well known programming "hello world", select

**File>Sketchbook>
Arduino-0017>Examples>
Digital>Blink**

Once you have your sketch you'll see something very close to the screenshot on the right.

In Tools>Board select MEGA

Now you have to go to
Tools>SerialPort
and select the right serial port, the one arduino is attached to.



Done compiling.

Press Compile button
(to check for errors)



Upload



TX RX Flashing



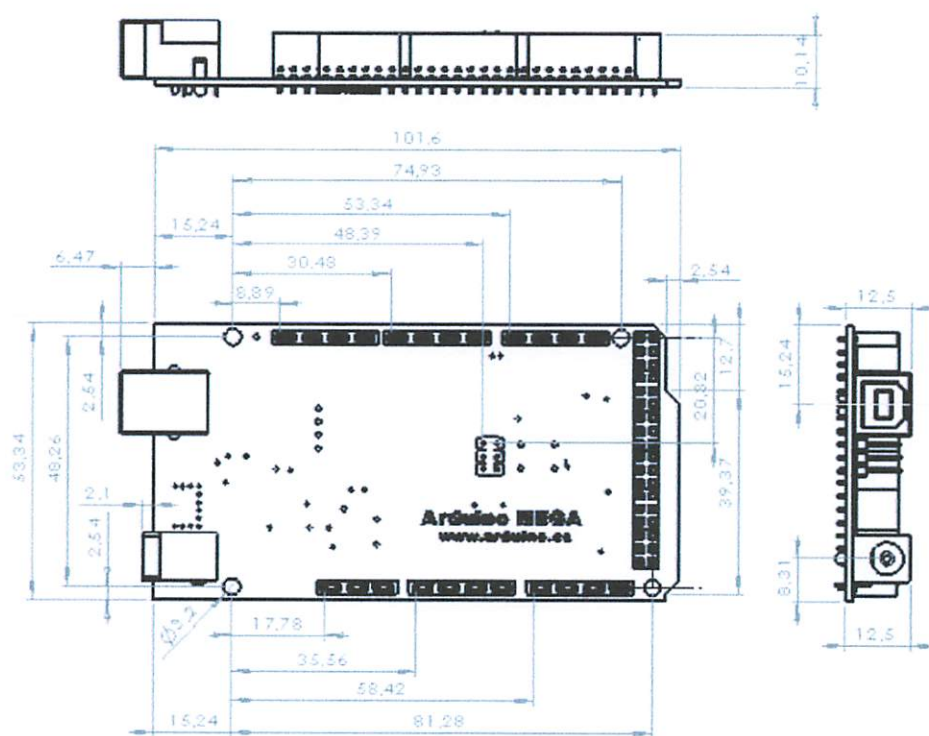
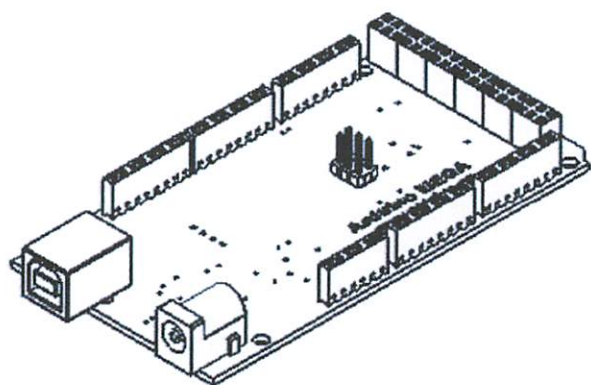
Blinking Led!



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RADIONICS





Radiospares

RADIONICS

ALLIED ELECTRONICS

Terms & Conditions



1. Warranties

1.1 The producer warrants that its products will conform to the Specifications. This warranty lasts for one (1) years from the date of the sale. The producer shall not be liable for any defects that are caused by neglect, misuse or mistreatment by the Customer, including improper installation or testing, or for any products that have been altered or modified in any way by a Customer. Moreover, The producer shall not be liable for any defects that result from Customer's design, specifications or instructions for such products. Testing and other quality control techniques are used to the extent the producer deems necessary.

1.2 If any products fail to conform to the warranty set forth above, the producer's sole liability shall be to replace such products. The producer's liability shall be limited to products that are determined by the producer not to conform to such warranty. If the producer elects to replace such products, the producer shall have a reasonable time to replacements. Replaced products shall be warranted for a new full warranty period.

1.3 EXCEPT AS SET FORTH ABOVE, PRODUCTS ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." THE PRODUCER DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING PRODUCTS, INCLUDING BUT NOT LIMITED TO, ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE

1.4 Customer agrees that prior to using any systems that include the producer products, Customer will test such systems and the functionality of the products as used in such systems. The producer may provide technical, applications or design advice, quality characterization, reliability data or other services. Customer acknowledges and agrees that providing these services shall not expand or otherwise alter the producer's warranties, as set forth above, and no additional obligations or liabilities shall arise from the producer providing such services.

1.5 The Arduino™ products are not authorized for use in safety-critical applications where a failure of the product would reasonably be expected to cause severe personal injury or death. Safety-Critical Applications include, without limitation, life support devices and systems, equipment or systems for the operation of nuclear facilities and weapons systems. Arduino™ products are neither designed nor intended for use in military or aerospace applications or environments and for automotive applications or environment. Customer acknowledges and agrees that any such use of Arduino™ products which is solely at the Customer's risk, and that Customer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

1.6 Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products and any use of Arduino™ products in Customer's applications, notwithstanding any applications-related information or support that may be provided by the producer.

2. Indemnification

The Customer acknowledges and agrees to defend, indemnify and hold harmless the producer from and against any and all third-party losses, damages, liabilities and expenses it incurs to the extent directly caused by: (i) an actual breach by a Customer of the representation and warranties made under this terms and conditions or (ii) the gross negligence or willful misconduct by the Customer.

3. Consequential Damages Waiver

In no event the producer shall be liable to the Customer or any third parties for any special, collateral, indirect, punitive, incidental, consequential or exemplary damages in connection with or arising out of the products provided hereunder, regardless of whether the producer has been advised of the possibility of such damages. This section will survive the termination of the warranty period.

4. Changes to specifications

The producer may make changes to specifications and product descriptions at any time, without notice. The Customer must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." The producer reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The product information on the Web Site or Materials is subject to change without notice. Do not finalize a design with this information.



Environmental Policies



The producer of Arduino™ has joined the Impatto Zero® policy of LifeGate.it. For each Arduino board produced is created / looked after half squared Km of Costa Rica's forest's.



radiospares

RADIONICS



Current Sense Transformers

High Frequency

CST206/306 Description

Designed for switching power supply applications, Triad current sense transformers are used to detect the current passing through a conductor.

These transformers are very reliable and operate effectively over the frequency range of 20 kHz-200 kHz. They are constructed of UL rated 130°C materials. Both models are available with a center tap option.

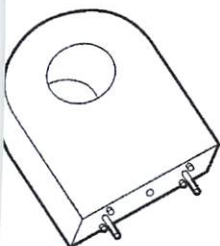


Figure A

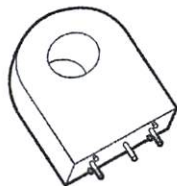


Figure B

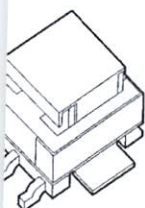
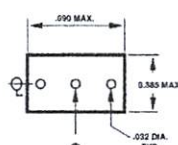
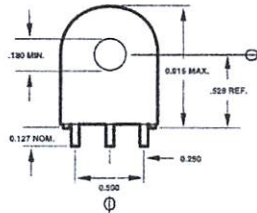
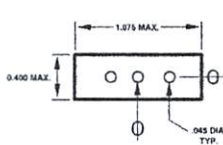
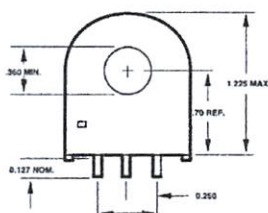
Section/ Figure	Type No.	ET V _{pk} SEC REF 20 kHz	Turns Count	Min. Ind. mH	DCR Max. Ohms	Pri. Amps
A	CST206-1A	2000	100	14.0	.580	110.0 RMS
B	CST206-1T	2000	100 CT	14.0	.580	110.0 RMS
A	CST206-2A	4000	200	56.0	3.500	80.0 RMS
B	CST206-2T	4000	200 CT	56.0	3.500	80.0 RMS
A	CST206-3A	6000	300	130.0	12.400	70.0 RMS
B	CST206-3T	6000	300 CT	130.0	12.400	70.0 RMS
B	CST306-1A	500	50	3.5	.340	35.0 RMS
A	CST306-1T	500	50 CT	3.5	.580	35.0 RMS
B	CST306-2A	1000	100	14.0	1.550	25.0 RMS
A	CST306-2T	1000	100 CT	14.0	1.550	25.0 RMS
B	CST306-3A	2000	200	55.0	3.750	25.0 RMS
A	CST306-3T	2000	200 CT	55.0	3.750	25.0 RMS

Outline Dimensions

Technical Notes

Derate ET product by 32% for 50 kHz, 52% for 100 Hz and 50% for unidirectional operation.
Rated primary current renders approximately 40°C temperature rise.

- CST206 models have maximum recommended terminating resistance of 1 ohm per turn.
- Primary is inserted through hole in casing.
- 3 pin or center tapped (CT) models are designed with a T suffix.



CSE5 Description

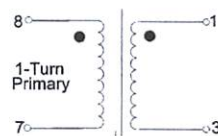
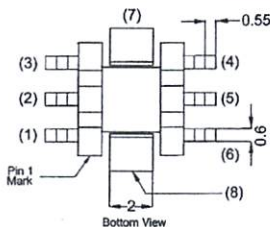
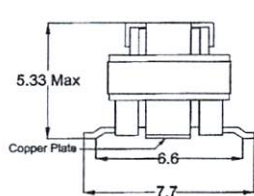
Designed to monitor current at 250 kHz and above. These transformers have a primary current rating of 10 Amps.

Part No.	Turns N1:N2 @ 10kHz	Secondary Inductance μH Min.	Secondary DCR mΩ Max
CSE5-100201	1:20	80	550
CSE5-100301	1:30	180	870
CSE5-100401	1:40	320	1140
CSE5-100501	1:50	500	1500
CSE5-100601	1:60	720	1750
CSE5-100701	1:70	980	4750
CSE5-101001	1:100	2000	5500
CSE5-101251	1:125	3000	8500

Outline Dimensions

Technical Notes

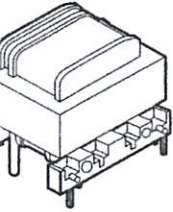
m}



Current Sense Transformers

Class B
UL File: E205349

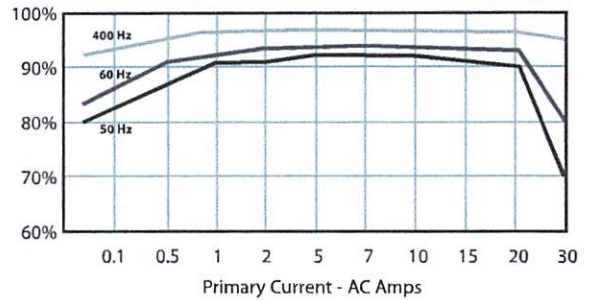
Low Frequency



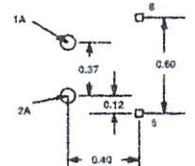
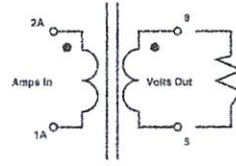
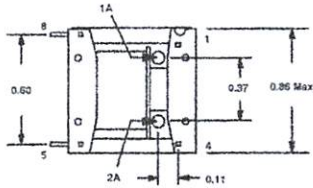
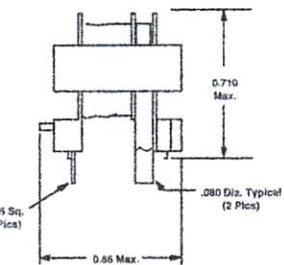
:: CSE187L Description

Designed to monitor current in low frequency applications. This Triad part may be used to monitor current from .1 to 30 amperes at frequencies from 50 Hz to 400 Hz.

CSE187L Performance Graph



Outline Dimensions



Technical Notes

1. Turns ratio: Primary to sense 1:500
2. Suggested burden resistor: 60 ohms.
3. Typical output: 110 mV/Amp.

4. Primary DCR: 250 μ Ohms maximum.
5. Sense DCR: 21 ohms maximum.
6. Constructed with UL recognized materials (Class B, 130°C).

7. Hi-pot: 2,500 volts wdg-wdg.
8. Potted version available with a dielectric strength of 4,000 volts wdg-wdg.



:: CST Series Description

Triad current sense transformers are used to detect the current passing through a conductor. These transformers are very reliable and operate effectively between 50-60 Hz. They are constructed of UL rated 130°C materials.

Specifications

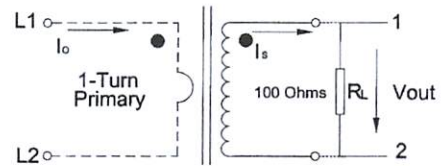
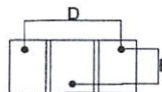
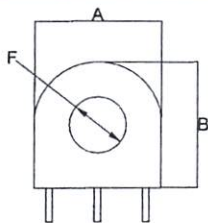
Part No.	Ip Amps	Turns Ratio	Terminating Resistor		DCR (Ohms) Nominal	Volts/Amp @ rated Ip for various loads				Net Weight (grams) REF	Case Dimensions – mm					
			Ohms	Watt		100	500	2K	5K		A	B	C	D	E	F
C-1005	5	1000:1	100	0.0025	40.00	0.0958	0.4490	1.3694	1.8402	20.0	23.50	24.80	12.00	15.00	7.50	8.50
C-1010	10	1000:1	100	0.0100	40.00	0.0969	0.4565	0.9686	1.1912	20.0	23.50	24.80	12.00	15.00	7.50	8.50
C-1015	15	1000:1	100	0.0230	40.00	0.0971	0.4429	0.7508	0.9439	20.0	23.50	24.80	12.00	15.00	7.50	8.50
C-1020	20	1000:1	100	0.0400	40.00	0.0977	0.3943	0.6174	0.7662	20.0	23.50	24.80	12.00	12.00	7.50	8.50
C-1025	25	1000:1	100	0.0630	46.00	0.0976	0.4364	0.7496	0.9664	30.0	30.20	30.20	14.30	20.32	10.16	11.40
C-1030	30	1000:1	100	0.0900	46.00	0.0977	0.4160	0.6710	0.8750	30.0	30.20	30.20	14.30	20.32	10.16	11.40

Primary Current

Outline Dimensions

Technical Notes

Pin length: 5 ± 1 mm
Pin diameter: 0.8 ± 0.1 mm
Pin 3 normally for mechanical support only



Current Sense Transformers

High Frequency

CST206/306 Description

Designed for switching power supply applications, Triad current sense transformers are used to detect the current passing through a conductor.

These transformers are very reliable and operate effectively over the frequency range of 20 kHz-200 kHz. They are constructed of UL rated 130°C materials. Both models are available with a center tap option.

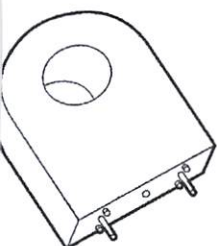


Figure A

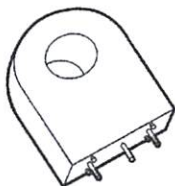


Figure B

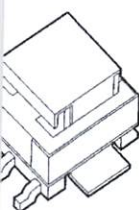
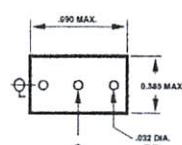
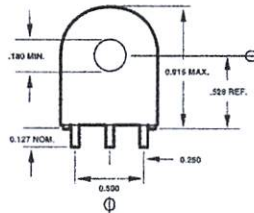
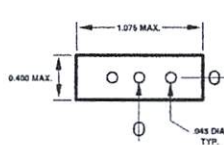
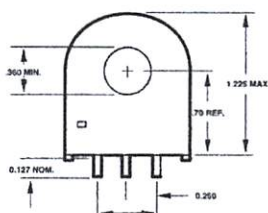
Section/ Figure	Type No.	ET VpSEC REF 20 kHz	Turns Count	Min. Ind. mH	DCR Max. Ohms	Pri. Amps
A	CST206-1A	2000	100	14.0	.580	110.0 RMS
B	CST206-1T	2000	100 CT	14.0	.580	110.0 RMS
A	CST206-2A	4000	200	56.0	3.500	80.0 RMS
B	CST206-2T	4000	200 CT	56.0	3.500	80.0 RMS
A	CST206-3A	6000	300	130.0	12.400	70.0 RMS
B	CST206-3T	6000	300 CT	130.0	12.400	70.0 RMS
B	CST306-1A	500	50	3.5	.340	35.0 RMS
A	CST306-1T	500	50 CT	3.5	.580	35.0 RMS
B	CST306-2A	1000	100	14.0	1.550	25.0 RMS
A	CST306-2T	1000	100 CT	14.0	1.550	25.0 RMS
B	CST306-3A	2000	200	55.0	3.750	25.0 RMS
A	CST306-3T	2000	200 CT	55.0	3.750	25.0 RMS

Outline Dimensions

Technical Notes

Derate ET product by 32% for 50 kHz, 52% for 100 Hz and 50% for unidirectional operation.
Rated primary current renders approximately 40°C temperature rise.

- CST206 models have maximum recommended terminating resistance of 1 ohm per turn.
- Primary is inserted through hole in casing.
- 3 pin or center tapped (CT) models are designed with a T suffix.



CSE5 Description

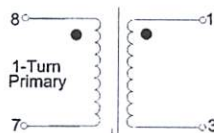
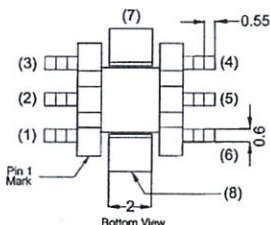
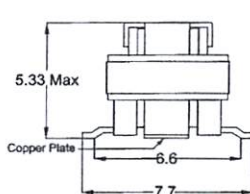
Designed to monitor current at 250 kHz and above. These transformers have a primary current rating of 10 Amps.

Part No.	Turns N1:N2 @ 10kHz	Secondary Inductance µH Min.	Secondary DCR mΩ Max
CSE5-100201	1:20	80	550
CSE5-100301	1:30	180	870
CSE5-100401	1:40	320	1140
CSE5-100501	1:50	500	1500
CSE5-100601	1:60	720	1750
CSE5-100701	1:70	980	4750
CSE5-101001	1:100	2000	5500
CSE5-101251	1:125	3000	8500

Outline Dimensions

Technical Notes

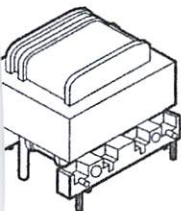
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Current Sense Transformers

Class B
UL File: E205349 

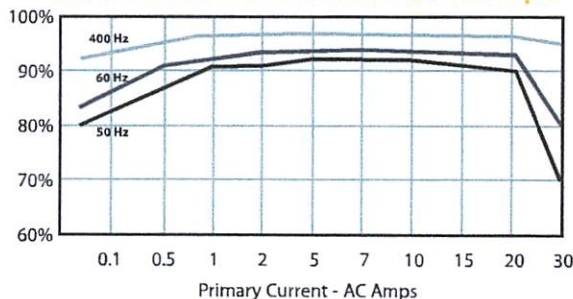
Low Frequency



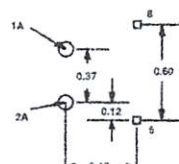
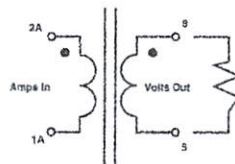
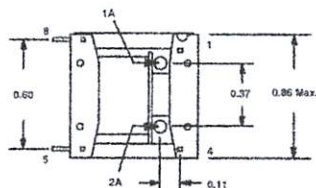
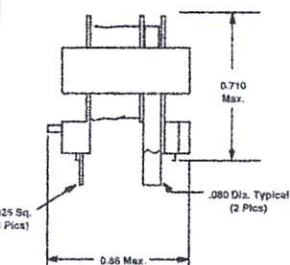
:: CSE187L Description

Designed to monitor current in low frequency applications. This Triad part may be used to monitor current from .1 to 30 amperes at frequencies from 50 Hz to 400 Hz.

CSE187L Performance Graph



Outline Dimensions



Technical Notes

1. Turns ratio: Primary to sense 1:500
2. Suggested burden resistor: 60 ohms.
3. Typical output: 110 mV/Amp.

4. Primary DCR: 250 μ Ohms maximum.

5. Sense DCR: 21 ohms maximum.

6. Constructed with UL recognized materials (Class B, 130°C).

7. Hi-pot: 2,500 volts wdg-wdg.

8. Potted version available with a dielectric strength of 4,000 volts wdg-wdg.



:: CST Series Description

Triad current sense transformers are used to detect the current passing through a conductor. These transformers are very reliable and operate effectively between 50-60 Hz. They are constructed of UL rated 130°C materials.

Specifications

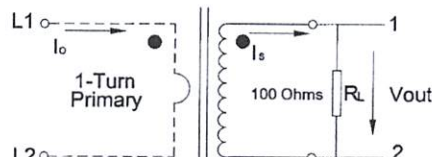
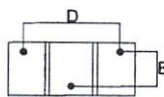
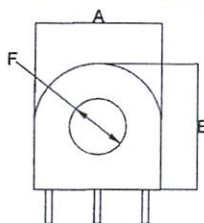
Part No.	Ip Amps	Turns Ratio	Terminating Resistor		DCR (Ohms) Nominal	Volts/Amp @ rated Ip for various loads				Net Weight (grams) REF	Case Dimensions – mm					
			Ohms	Watt		100	500	2K	5K		A	B	C	D	E	F
T-1005	5	1000:1	100	0.0025	40.00	0.0958	0.4490	1.3694	1.8402	20.0	23.50	24.80	12.00	15.00	7.50	8.50
T-1010	10	1000:1	100	0.0100	40.00	0.0969	0.4565	0.9686	1.1912	20.0	23.50	24.80	12.00	15.00	7.50	8.50
T-1015	15	1000:1	100	0.0230	40.00	0.0971	0.4429	0.7508	0.9439	20.0	23.50	24.80	12.00	15.00	7.50	8.50
T-1020	20	1000:1	100	0.0400	40.00	0.0977	0.3943	0.6174	0.7662	20.0	23.50	24.80	12.00	12.00	7.50	8.50
T-1025	25	1000:1	100	0.0630	46.00	0.0976	0.4364	0.7496	0.9664	30.0	30.20	30.20	14.30	20.32	10.16	11.40
T-1030	30	1000:1	100	0.0900	46.00	0.0977	0.4160	0.6710	0.8750	30.0	30.20	30.20	14.30	20.32	10.16	11.40

Primary Current

Outline Dimensions

Technical Notes

in length: 5 ± 1 mm
in diameter: 0.8 ± 0.1 mm
in 3 normally for mechanical support only



FEATURES

High accuracy; supports IEC 60687/61036/61268 and IEC 62053-21/62053-22/62053-23
On-chip digital integrator enables direct interface to current sensors with di/dt output
PGA in the current channel allows direct interface to shunts and current transformers
Active, reactive, and apparent energy; sampled waveform; current and voltage rms
Less than 0.1% error in active energy measurement over a dynamic range of 1000 to 1 at 25°C
Positive-only energy accumulation mode available
On-chip user programmable threshold for line voltage surge and SAG and PSU supervisory
Digital calibration for power, phase, and input offset
On-chip temperature sensor ($\pm 3^\circ\text{C}$ typical)
SPI-compatible serial interface
Pulse output with programmable frequency
Interrupt request pin (IRQ) and status register
Reference 2.4 V with external overdrive capability
Single 5 V supply, low power (25 mW typical)

GENERAL DESCRIPTION

The ADE7753¹ features proprietary ADCs and DSP for high accuracy over large variations in environmental conditions and line. The ADE7753 incorporates two second-order 16-bit Σ - Δ ADCs, a digital integrator (on CH1), reference circuitry, temperature sensor, and all the signal processing required to perform active, reactive, and apparent energy measurements,

line-voltage period measurement, and rms calculation on the voltage and current. The selectable on-chip digital integrator provides direct interface to di/dt current sensors such as Rogowski coils, eliminating the need for an external analog integrator and resulting in excellent long-term stability and precise phase matching between the current and voltage channels.

The ADE7753 provides a serial interface to read data, and a pulse output frequency (CF), which is proportional to the active power. Various system calibration features, i.e., channel offset correction, phase calibration, and power calibration, ensure high accuracy. The part also detects short duration low or high voltage variations.

The positive-only accumulation mode gives the option to accumulate energy only when positive power is detected. An internal no-load threshold ensures that the part does not exhibit any creep when there is no load. The zero-crossing output (ZX) produces a pulse that is synchronized to the zero-crossing point of the line voltage. This signal is used internally in the line cycle active and apparent energy accumulation modes, which enables faster calibration.

The interrupt status register indicates the nature of the interrupt, and the interrupt enable register controls which event produces an output on the IRQ pin, an open-drain, active low logic output.

The ADE7753 is available in a 20-lead SSOP package.

FUNCTIONAL BLOCK DIAGRAM

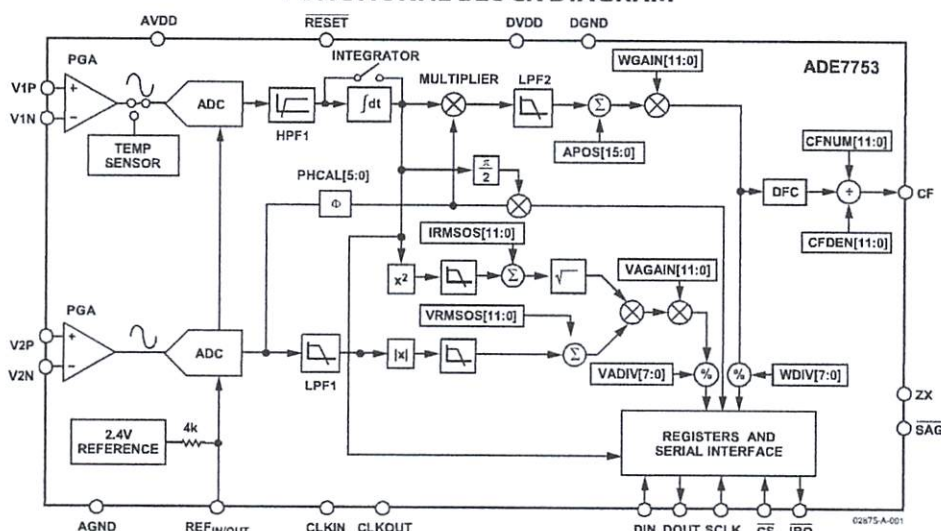


Figure 1.

U.S. Patents 5,745,323; 5,760,617; 5,862,069; 5,872,469.

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8/03—Revision 0: Initial Version

CIFICATIONS

$V_{DD} = 5\text{ V} \pm 5\%$, $AGND = DGND = 0\text{ V}$, on-chip reference, $CLKIN = 3.579545\text{ MHz XTAL}$, T_{MIN} to $T_{MAX} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$. See tests in the Typical Performance Characteristics section.

1.

Parameter	Spec	Unit	Test Conditions/Comments
POWER MEASUREMENT ACCURACY			
Active Power Measurement Error			$CLKIN = 3.579545\text{ MHz}$
Channel 1 Range = 0.5 V Full Scale			Channel 2 = 300 mV rms/60 Hz, gain = 2
Gain = 1	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 2	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 4	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 8	0.1	% typ	Over a dynamic range 1000 to 1
Channel 1 Range = 0.25 V Full Scale			
Gain = 1	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 2	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 4	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 8	0.2	% typ	Over a dynamic range 1000 to 1
Channel 1 Range = 0.125 V Full Scale			
Gain = 1	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 2	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 4	0.2	% typ	Over a dynamic range 1000 to 1
Gain = 8	0.2	% typ	Over a dynamic range 1000 to 1
Active Power Measurement Bandwidth	14	kHz	
Offset Error 1 between Channels ¹	± 0.05	max	Line Frequency = 45 Hz to 65 Hz, HPF on
Power Supply Rejection ¹			$AV_{DD} = DV_{DD} = 5\text{ V} + 175\text{ mV rms}/120\text{ Hz}$
Output Frequency Variation (CF)	0.2	% typ	Channel 1 = 20 mV rms, gain = 16, range = 0.5 V
			Channel 2 = 300 mV rms/60 Hz, gain = 1
Power Supply Rejection ¹			$AV_{DD} = DV_{DD} = 5\text{ V} \pm 250\text{ mV dc}$
Output Frequency Variation (CF)	± 0.3	% typ	Channel 1 = 20 mV rms/60 Hz, gain = 16, range = 0.5 V
			Channel 2 = 300 mV rms/60 Hz, gain = 1
RMS Measurement Error	0.5	% typ	Over a dynamic range 100 to 1
RMS Measurement Bandwidth	14	kHz	
RMS Measurement Error	0.5	% typ	Over a dynamic range 20 to 1
RMS Measurement Bandwidth	140	Hz	
ANALOG INPUTS²			
Minimum Signal Levels	± 0.5	V max	See the Analog Inputs section
Input Impedance (dc)	390	k min	V1P, V1N, V2N, and V2P to AGND
Bandwidth	14	kHz	
Offset Error ^{1,2}			$CLKIN/256$, $CLKIN = 3.579545\text{ MHz}$
Channel 1			External 2.5 V reference, gain = 1 on Channels 1 and 2
Range = 0.5 V Full Scale	± 4	% typ	V1 = 0.5 V dc
Range = 0.25 V Full Scale	± 4	% typ	V1 = 0.25 V dc
Range = 0.125 V Full Scale	± 4	% typ	V1 = 0.125 V dc
Channel 2	± 4	% typ	V2 = 0.5 V dc
Offset Error ¹	± 32	mV max	Gain 1
Channel 1	± 13	mV max	Gain 16
	± 32	mV max	Gain 1
Channel 2	± 13	mV max	Gain 16
SPREADSHEET SAMPLING			
Channel 1			Sampling $CLKIN/128$, $3.579545\text{ MHz}/128 = 27.9\text{ kSPS}$
Signal-to-Noise Plus Distortion	62	dB typ	See the Channel 1 Sampling section
Bandwidth(–3 dB)	14	kHz	150 mV rms/60 Hz, range = 0.5 V, gain = 2
			$CLKIN = 3.579545\text{ MHz}$

Parameter	Spec	Unit	Test Conditions/Comments
Channel 2 Signal-to-Noise Plus Distortion Bandwidth (–3 dB)	60 140	dB typ Hz	See the Channel 2 Sampling section 150 mV rms/60 Hz, gain = 2 CLKIN = 3.579545 MHz
REFERENCE INPUT REFIN/OUT Input Voltage Range Input Capacitance	2.6 2.2 10	V max V min pF max	2.4 V + 8% 2.4 V – 8%
ON-CHIP REFERENCE Reference Error Current Source Output Impedance Temperature Coefficient	±200 10 3.4 30	mV max μA max kΩ min ppm/°C typ	Nominal 2.4 V at REFIN/OUT pin
CLKIN Input Clock Frequency	4 1	MHz max MHz min	All specifications CLKIN of 3.579545 MHz
DIGITAL INPUTS RESET, DIN, SCLK, CLKIN, and CS Input High Voltage, VINH Input Low Voltage, VINL Input Current, IIN Input Capacitance, CIN	2.4 0.8 ±3 10	V min V max μA max pF max	DVDD = 5 V ± 10% DVDD = 5 V ± 10% Typically 10 nA, VIN = 0 V to DVDD
DIGITAL OUTPUTS SAG and IRQ Output High Voltage, VOH Output Low Voltage, VOL ZX and DOUT Output High Voltage, VOH Output Low Voltage, VOL CF Output High Voltage, VOH Output Low Voltage, VOL	4 0.4 4 0.4 4 1	V min V max V min V max V min V max	Open-drain outputs, 10 kΩ pull-up resistor ISOURCE = 5 mA ISINK = 0.8 mA ISOURCE = 5 mA ISINK = 0.8 mA ISOURCE = 5 mA ISINK = 7 mA
POWER SUPPLY AVDD DVDD ALDD DLDD	4.75 5.25 4.75 5.25 3 4	V min V max V min V max mA max mA max	For specified performance 5 V – 5% 5 V + 5% 5 V – 5% 5 V + 5% Typically 2.0 mA Typically 3.0 mA

See the Terminology section for explanation of specifications.
See the Analog Inputs section.

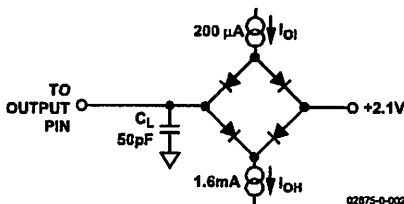


Figure 2. Load Circuit for Timing Specifications

ING CHARACTERISTICS

= $DV_{DD} = 5\text{ V} \pm 5\%$, $AGND = DGND = 0\text{ V}$, on-chip reference, $CLKIN = 3.579545\text{ MHz XTAL}$, T_{MIN} to $T_{MAX} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.
e tested during initial release and after any redesign or process change that could affect this parameter. All input signals are specified with
= 5 ns (10% to 90%) and timed from a voltage level of 1.6 V . See Figure 3, Figure 4, and the ADE7753 Serial Interface section.

2.

Parameter	Spec	Unit	Test Conditions/Comments
Timing	50	ns (min)	$\overline{CS}$ falling edge to first SCLK falling edge.
	50	ns (min)	SCLK logic high pulse width.
	50	ns (min)	SCLK logic low pulse width.
	10	ns (min)	Valid data setup time before falling edge of SCLK.
	5	ns (min)	Data hold time after SCLK falling edge.
	4	μs (min)	Minimum time between the end of data byte transfers.
	50	ns (min)	Minimum time between byte transfers during a serial write.
	100	ns (min)	$\overline{CS}$ hold time after SCLK falling edge.
Timing	4	μs (min)	Minimum time between read command (i.e., a write to communication register) and data read.
	50	ns (min)	Minimum time between data byte transfers during a multibyte read.
	30	ns (min)	Data access time after SCLK rising edge following a write to the communications register.
	100	ns (max)	Bus relinquish time after falling edge of SCLK.
	10	ns (min)	
	100	ns (max)	Bus relinquish time after rising edge of $\overline{CS}$.
	10	ns (min)	

um time between read command and data read for all registers except waveform register, which is $t_9 = 500\text{ ns}$ min.
red with the load circuit in Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V .
d from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 2. The measured number is then extrapolated back
ove the effects of charging or discharging the 50 pF capacitor. This means that the time quoted in the timing characteristics is the true bus relinquish time of
t and is independent of the bus loading.

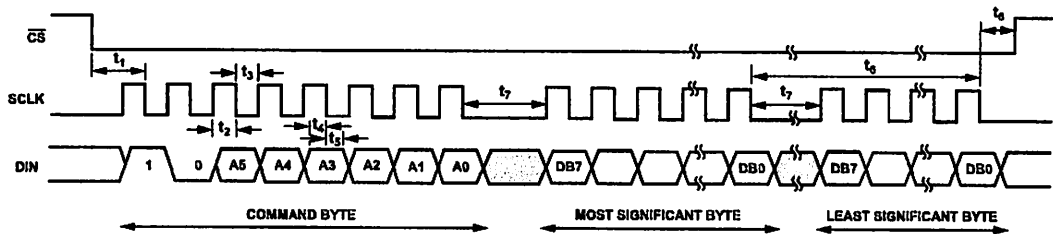


Figure 3. Serial Write Timing

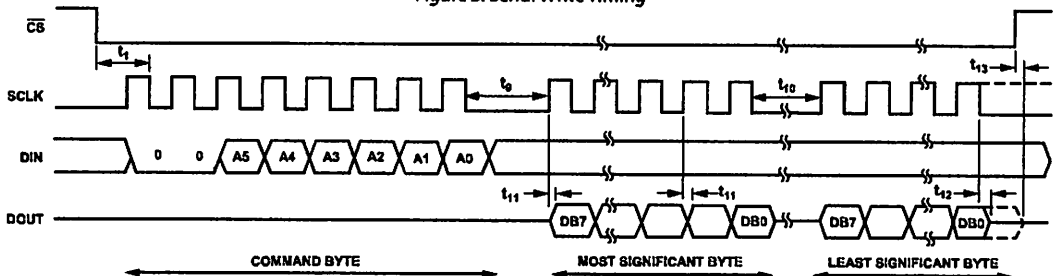


Figure 4. Serial Read Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
VDD to AGND	−0.3 V to +7 V
VDD to DGND	−0.3 V to +7 V
VDD to AVDD	−0.3 V to +0.3 V
Analog Input Voltage to AGND, V1P, V1N, V2P, and V2N	−6 V to +6 V
Reference Input Voltage to AGND	−0.3 V to AVDD + 0.3 V
Digital Input Voltage to DGND	−0.3 V to DVDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DVDD + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
0-Lead SSOP, Power Dissipation	450 mW
θ _{JA} Thermal Impedance	112°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



MINOLOGY

Measurement Error

Error associated with the energy measurement made by the ADE7753 is defined by the following formula:

Percentage Error =

$$\frac{\text{Energy Register ADE7753} - \text{True Energy}}{\text{True Energy}} \times 100\%$$

Error between Channels

The digital integrator and the high-pass filter (HPF) in Channel 1 have a non-ideal phase response. To offset this phase response and equalize the phase response between channels, two phase-correction networks are placed in Channel 1: one for the digital integrator and the other for the HPF. The phase correction networks correct the phase response of the corresponding measurement and ensure a phase match between Channel 1 (current) and Channel 2 (voltage) to within $\pm 0.1^\circ$ over a range of 45 Hz to 65 Hz with the digital integrator off. With the digital integrator on, the phase is corrected to within $\pm 0.4^\circ$ over a range of 45 Hz to 65 Hz.

Supply Rejection

Supply rejection identifies the ADE7753 measurement error as a percentage of the true energy when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when an ac (175 mV rms/120 Hz) signal is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading—see the Measurement Error definition.

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied $\pm 5\%$. Any error introduced is again expressed as a percentage of the reading.

ADC Offset Error

The dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection—see the Typical Performance Characteristics section. However, when HPF1 is switched on, the offset is removed from Channel 1 (current) and the power calculation is not affected by this offset. The offsets can be removed by performing an offset calibration—see the Analog Inputs section.

Gain Error

The difference between the measured ADC output code (minus the offset) and the ideal output code—see the Channel 1 ADC and Channel 2 ADC sections. It is measured for each of the input ranges on Channel 1 (0.5 V, 0.25 V, and 0.125 V). The difference is expressed as a percentage of the ideal code.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

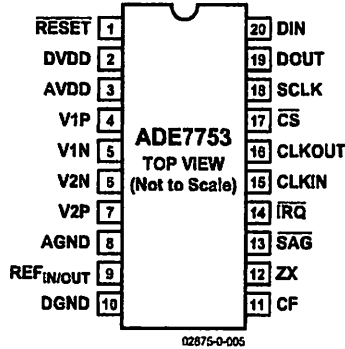


Figure 5. Pin Configuration (SSOP Package)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
5	RESET	Reset Pin for the ADE7753. A logic low on this pin holds the ADCs and digital circuitry (including the serial interface) in a reset condition.
	DVDD	Digital Power Supply. This pin provides the supply voltage for the digital circuitry in the ADE7753. The supply voltage should be maintained at $5\text{ V} \pm 5\%$ for specified operation. This pin should be decoupled to DGND with a $10\text{ }\mu\text{F}$ capacitor in parallel with a ceramic 100 nF capacitor.
	AVDD	Analog Power Supply. This pin provides the supply voltage for the analog circuitry in the ADE7753. The supply should be maintained at $5\text{ V} \pm 5\%$ for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling. The typical performance graphs show the power supply rejection performance. This pin should be decoupled to AGND with a $10\text{ }\mu\text{F}$ capacitor in parallel with a ceramic 100 nF capacitor.
	V1P, V1N	Analog Inputs for Channel 1. This channel is intended for use with a di/dt current transducer such as a Rogowski coil or another current sensor such as a shunt or current transformer (CT). These inputs are fully differential voltage inputs with maximum differential input signal levels of $\pm 0.5\text{ V}$, $\pm 0.25\text{ V}$, and $\pm 0.125\text{ V}$, depending on the full-scale selection—see the Analog Inputs section. Channel 1 also has a PGA with gain selections of 1, 2, 4, 8, or 16. The maximum signal level at these pins with respect to AGND is $\pm 0.5\text{ V}$. Both inputs have internal ESD protection circuitry, and, in addition, an overvoltage of $\pm 6\text{ V}$ can be sustained on these inputs without risk of permanent damage.
	V2N, V2P	Analog Inputs for Channel 2. This channel is intended for use with the voltage transducer. These inputs are fully differential voltage inputs with a maximum differential signal level of $\pm 0.5\text{ V}$. Channel 2 also has a PGA with gain selections of 1, 2, 4, 8, or 16. The maximum signal level at these pins with respect to AGND is $\pm 0.5\text{ V}$. Both inputs have internal ESD protection circuitry, and an overvoltage of $\pm 6\text{ V}$ can be sustained on these inputs without risk of permanent damage.
7	AGND	Analog Ground Reference. This pin provides the ground reference for the analog circuitry in the ADE7753, i.e., ADCs and reference. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, for example, anti-aliasing filters, current and voltage transducers, etc. To keep ground noise around the ADE7753 to a minimum, the quiet ground plane should be connected to the digital ground plane at only one point. It is acceptable to place the entire device on the analog ground plane.
	REF_IN/OUT	Access to the On-Chip Voltage Reference. The on-chip reference has a nominal value of $2.4\text{ V} \pm 8\%$ and a typical temperature coefficient of $30\text{ ppm}/^\circ\text{C}$. An external reference source can also be connected at this pin. In either case, this pin should be decoupled to AGND with a $1\text{ }\mu\text{F}$ ceramic capacitor.
	DGND	Digital Ground Reference. This pin provides the ground reference for the digital circuitry in the ADE7753, i.e., multiplier, filters, and digital-to-frequency converter. Because the digital return currents in the ADE7753 are small, it is acceptable to connect this pin to the analog ground plane of the system. However, high bus capacitance on the DOUT pin could result in noisy digital current, which could affect performance.
1	CF	Calibration Frequency Logic Output. The CF logic output gives active power information. This output is intended to be used for operational and calibration purposes. The full-scale output frequency can be adjusted by writing to the CFDEN and CFNUM registers—see the Energy-to-Frequency Conversion section.

	Mnemonic	Description
	ZX	Voltage Waveform (Channel 2) Zero-Crossing Output. This output toggles logic high and logic low at the zero crossing of the differential signal on Channel 2—see the Zero-Crossing Detection section.
	$\overline{\text{SAG}}$	This open-drain logic output goes active low when either no zero crossings are detected or a low voltage threshold (Channel 2) is crossed for a specified duration—see the Line Voltage Sag Detection section.
	$\overline{\text{IRQ}}$	Interrupt Request Output. This is an active low open-drain logic output. Maskable interrupts include active energy register rollover, active energy register at half level, and arrivals of new waveform samples—see the ADE7753 Interrupts section.
	CLKIN	Master Clock for ADCs and Digital Signal Processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7753. The clock frequency for specified operation is 3.579545 MHz. Ceramic load capacitors of between 22 pF and 33 pF should be used with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for load capacitance requirements.
	CLKOUT	A crystal can be connected across this pin and CLKIN as described for Pin 15 to provide a clock source for the ADE7753. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used.
	$\overline{\text{CS}}$	Chip Select. Part of the 4-wire SPI serial interface. This active low logic input allows the ADE7753 to share the serial bus with several other devices—see the ADE7753 Serial Interface section.
	SCLK	Serial Clock Input for the Synchronous Serial Interface. All serial data transfers are synchronized to this clock—see the ADE7753 Serial Interface section. The SCLK has a Schmitt-trigger input for use with a clock source that has a slow edge transition time, for example, opto-isolator output.
	DOUT	Data Output for the Serial Interface. Data is shifted out at this pin on the rising edge of SCLK. This logic output is normally in a high impedance state unless it is driving data onto the serial data bus—see the ADE7753 Serial Interface section.
	DIN	Data Input for the Serial Interface. Data is shifted in at this pin on the falling edge of SCLK—see the ADE7753 Serial Interface section.

ommended to drive the RESET, SCLK, and $\overline{\text{CS}}$ pins with either a push-pull without an external series resistor or with an open-collector with a 10 k Ω pull-up
r. Pull-down resistors are not recommended because under some conditions, they may interact with internal circuitry.

TYPICAL PERFORMANCE CHARACTERISTICS

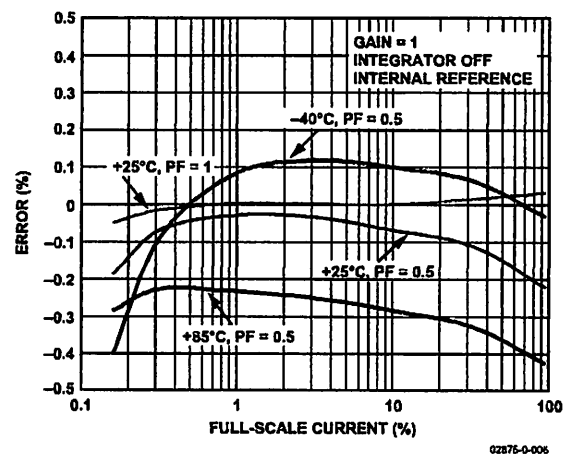


Figure 6. Active Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference and Integrator Off

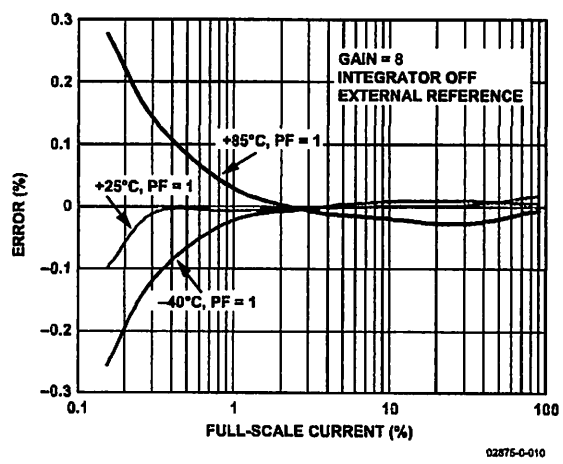


Figure 9. Active Energy Error as a Percentage of Reading (Gain = 8) over Temperature with External Reference and Integrator Off

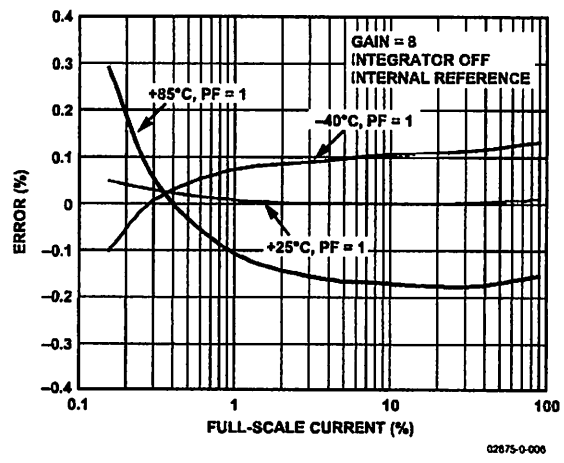


Figure 7. Active Energy as a Percentage of Reading (Gain = 8) over Temperature with Internal Reference and Integrator Off

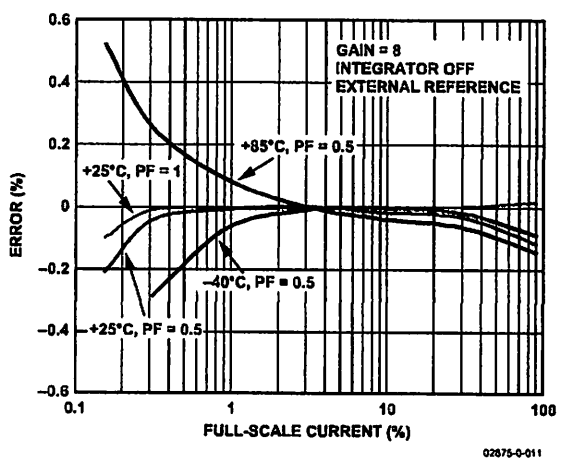


Figure 10. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with External Reference and Integrator Off

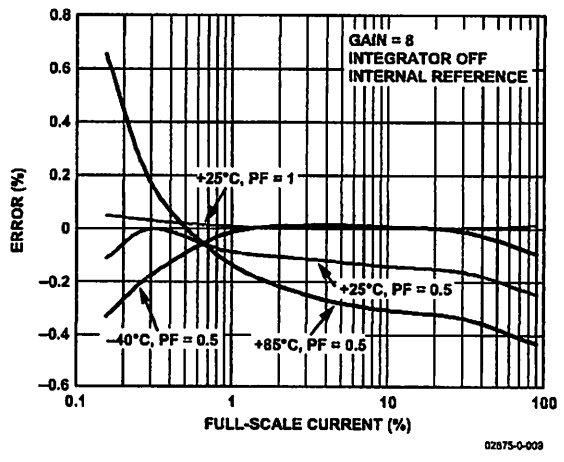


Figure 8. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference and Integrator Off

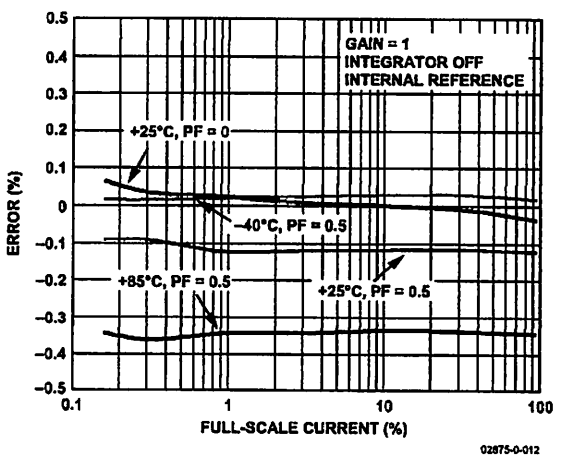
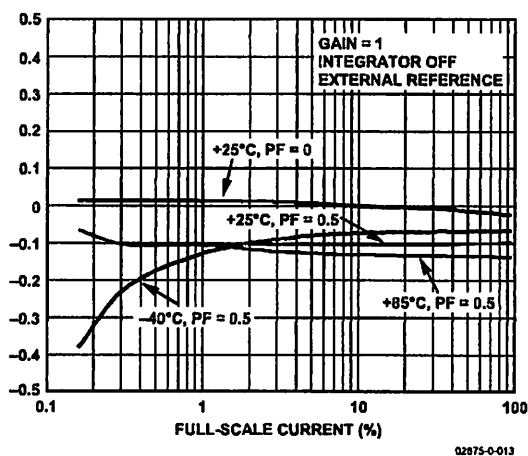
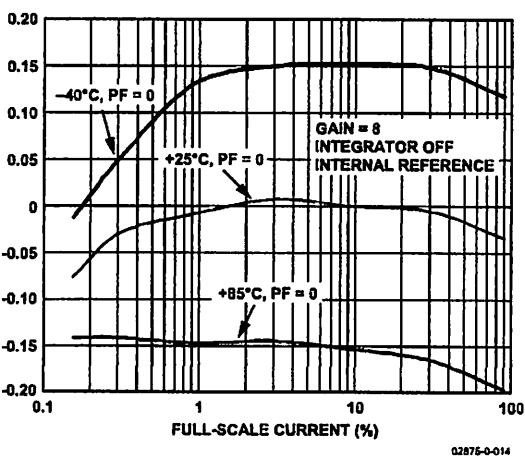


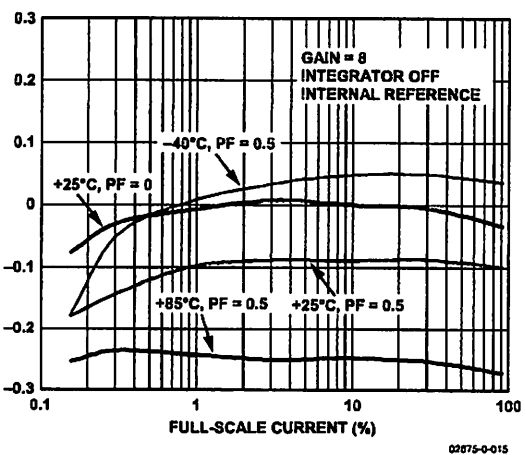
Figure 11. Reactive Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference and Integrator Off



12. Reactive Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with External Reference and Integrator Off



13. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Temperature with Internal Reference and Integrator Off



14. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference and Integrator Off

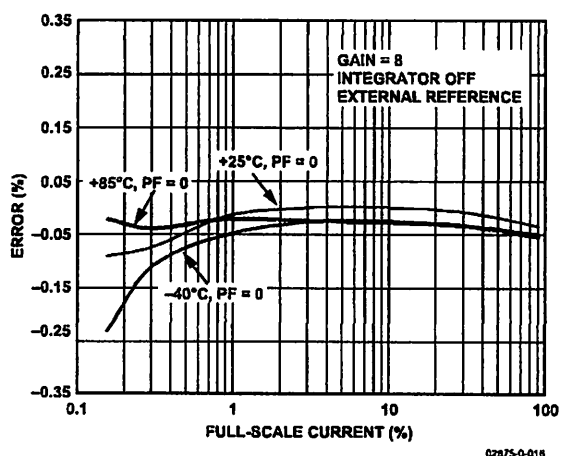


Figure 15. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Temperature with External Reference and Integrator Off

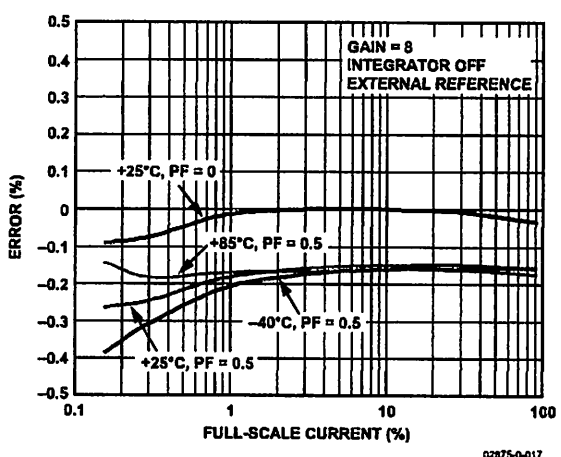


Figure 16. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with External Reference and Integrator Off

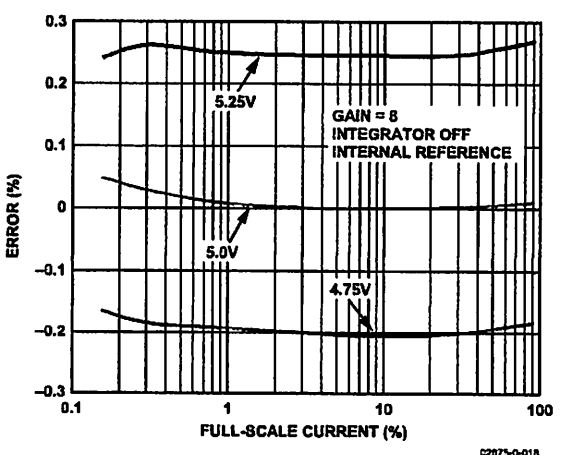


Figure 17. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Supply with Internal Reference and Integrator Off

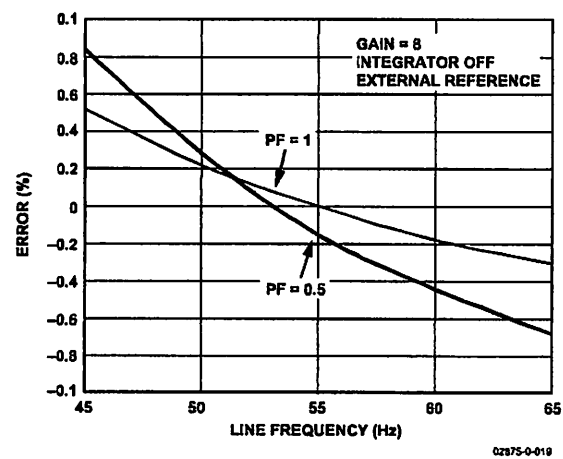


Figure 18. Active Energy Error as a Percentage of Reading (Gain = 8) over Frequency with External Reference and Integrator Off

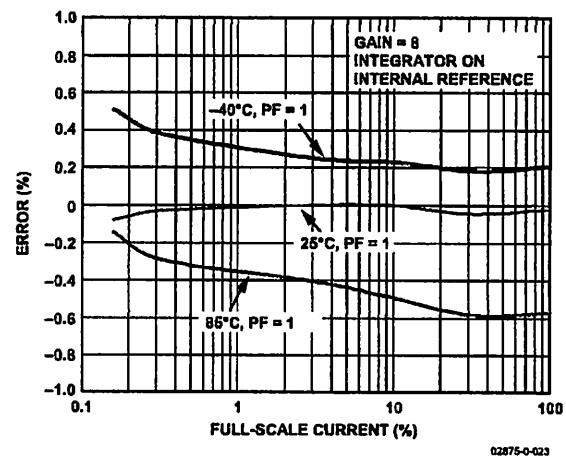


Figure 21. Active Energy Error as a Percentage of Reading (Gain = 8) over Temperature with Internal Reference and Integrator On

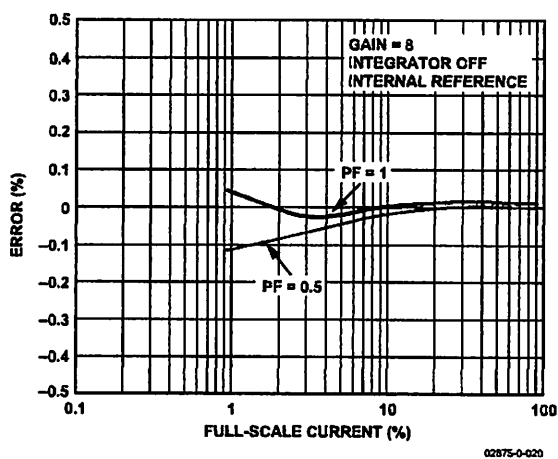


Figure 19. IRMS Error as a Percentage of Reading (Gain = 8) with Internal Reference and Integrator Off

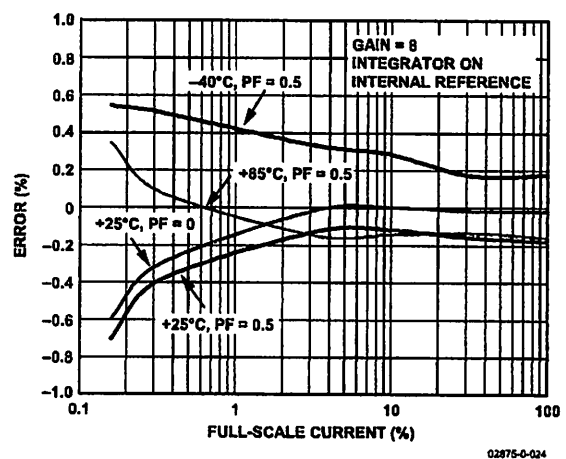


Figure 22. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference and Integrator On

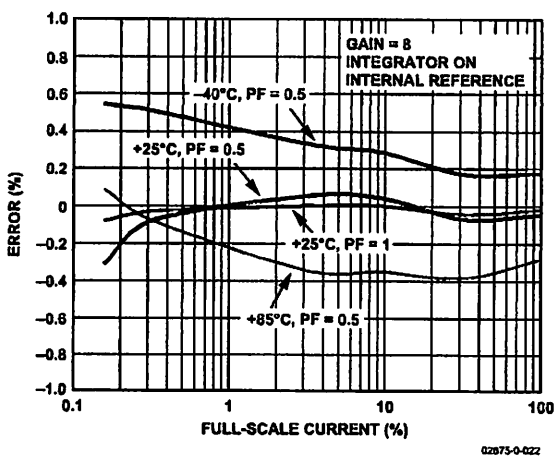


Figure 20. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference and Integrator On

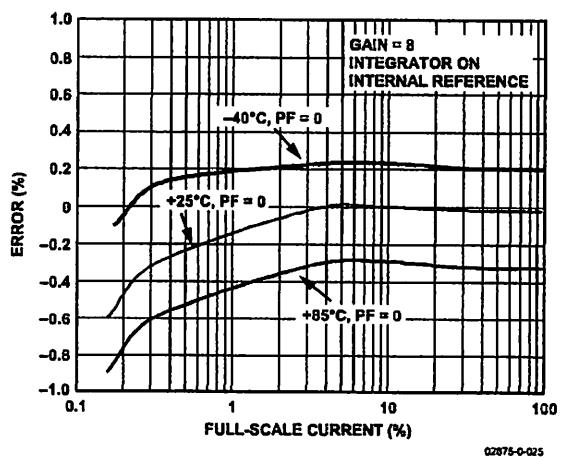


Figure 23. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Temperature with Internal Reference and Integrator On

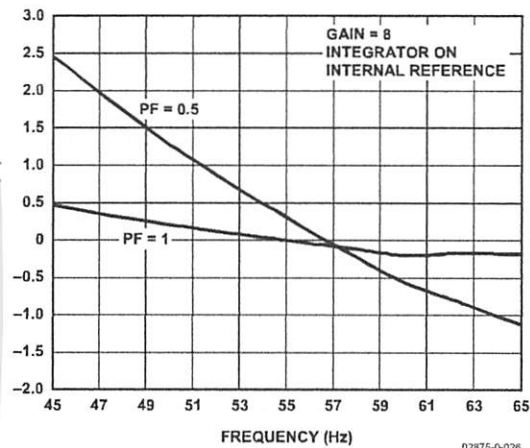


Figure 24. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference and Integrator On

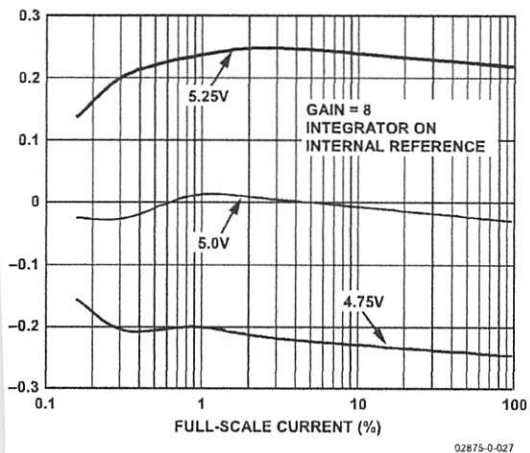


Figure 25. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Supply with Internal Reference and Integrator On

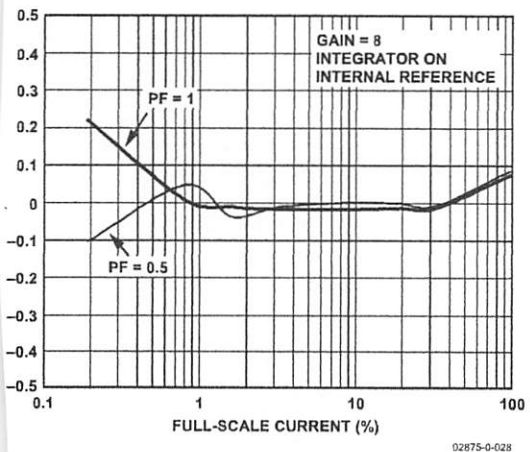


Figure 26. IRMS Error as a Percentage of Reading (Gain = 8) with Internal Reference and Integrator On

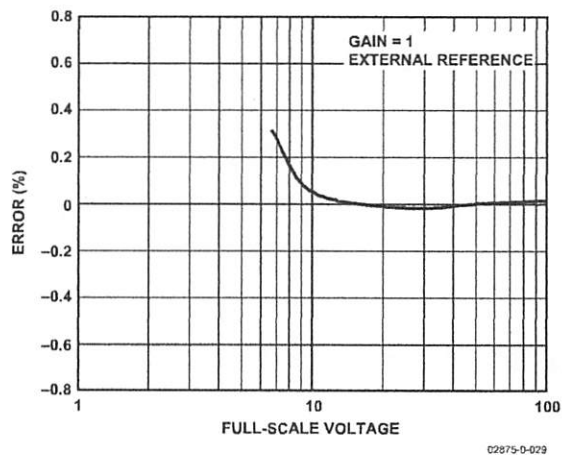


Figure 27. VRMS Error as a Percentage of Reading (Gain = 1) with External Reference

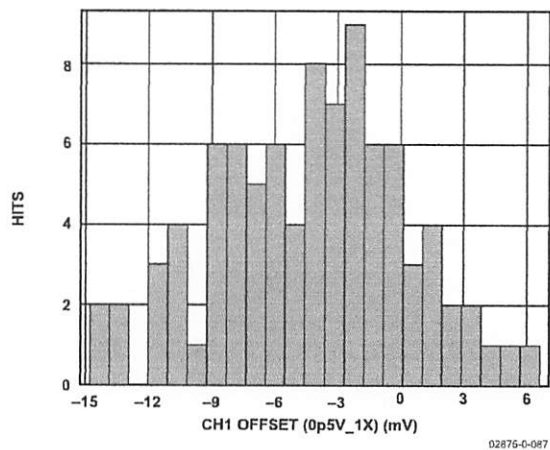


Figure 28. Channel 1 Offset (Gain = 1)

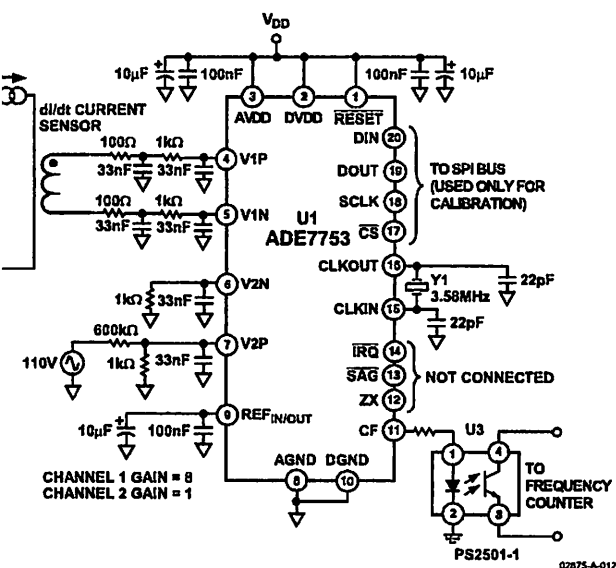


Figure 29. Test Circuit for Performance Curves with Integrator On

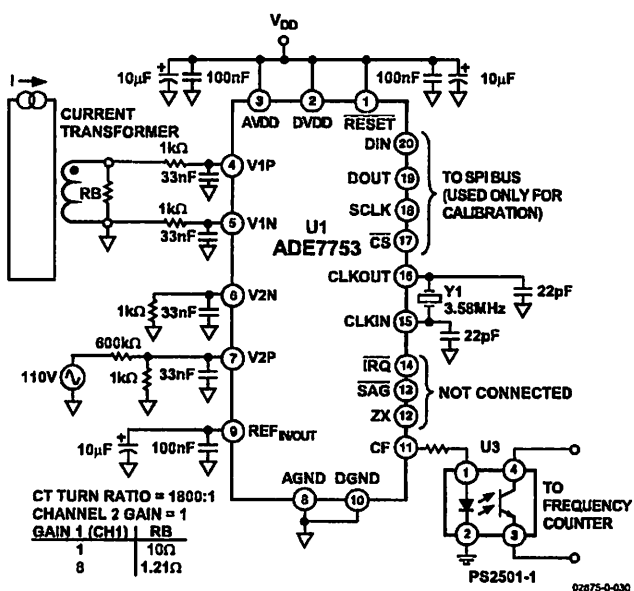


Figure 30. Test Circuit for Performance Curves with Integrator Off

ORY OF OPERATION

LOG INPUTS

DE7753 has two fully differential voltage input channels. maximum differential input voltage for input pairs V1P/V1N 2P/V2N is ±0.5 V. In addition, the maximum signal level log inputs for V1P/V1N and V2P/ V2N is ±0.5 V with t to AGND.

analog input channel has a programmable gain amplifier with possible gain selections of 1, 2, 4, 8, and 16. The selections are made by writing to the gain register—see 32. Bits 0 to 2 select the gain for the PGA in Channel 1, the gain selection for the PGA in Channel 2 is made via to 7. Figure 31 shows how a gain selection for Channel 1 le using the gain register.

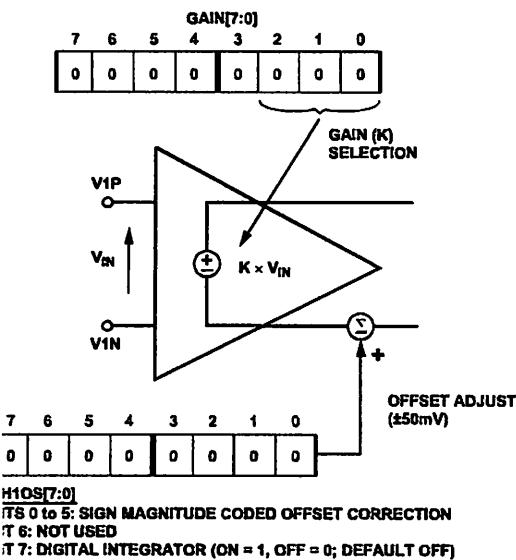


Figure 31. PGA in Channel 1

dition to the PGA, Channel 1 also has a full-scale input selection for the ADC. The ADC analog input range on is also made using the gain register—see Figure 32. As oned previously, the maximum differential input voltage 7. However, by using Bits 3 and 4 in the gain register, the um ADC input voltage can be set to 0.5 V, 0.25 V, or V. This is achieved by adjusting the ADC reference—see DE7753 Reference Circuit section. Table 5 summarizes the um differential input signal level on Channel 1 for the s ADC range and gain selections.

Table 5. Maximum Input Signal Levels for Channel 1

Max Signal Channel 1	ADC Input Range Selection		
	0.5 V	0.25 V	0.125 V
0.5 V	Gain = 1	—	—
0.25 V	Gain = 2	Gain = 1	—
0.125 V	Gain = 4	Gain = 2	Gain = 1
0.0625 V	Gain = 8	Gain = 4	Gain = 2
0.0313 V	Gain = 16	Gain = 8	Gain = 4
0.0156 V	—	Gain = 16	Gain = 8
0.00781 V	—	—	Gain = 16

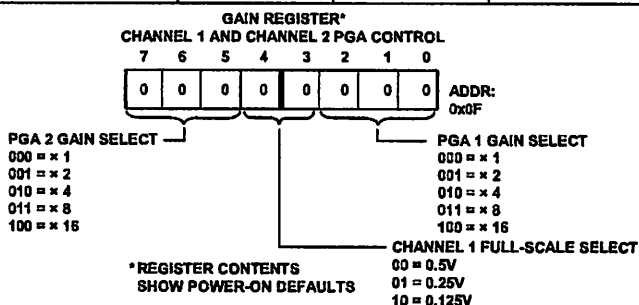


Figure 32. ADE7753 Analog Gain Register

It is also possible to adjust offset errors on Channel 1 and Channel 2 by writing to the offset correction registers, CH1OS and CH2OS, respectively. These registers allow channel offsets in the range ±20 mV to ±50 mV (depending on the gain setting) to be removed. Channel 1 and 2 offset registers are sign magnitude coded. A negative number is applied to the Channel 1 offset register, CH1OS, for a negative offset adjustment. Note that the Channel 2 offset register is inverted. A negative number is applied to CH2OS for a positive offset adjustment. It is not necessary to perform an offset correction in an energy measurement application if HPF in Channel 1 is switched on. Figure 33 shows the effect of offsets on the real power calculation. As seen from Figure 33, an offset on Channel 1 and Channel 2 contributes a dc component after multiplication. Because this dc component is extracted by LPF2 to generate the active (real) power information, the offsets contribute an error to the active power calculation. This problem is easily avoided by enabling HPF in Channel 1. By removing the offset from at least one channel, no error component is generated at dc by the multiplication. Error terms at cos(ωt) are removed by LPF2 and by integration of the active power signal in the active energy register (AENERGY[23:0]) —see the Energy Calculation section.

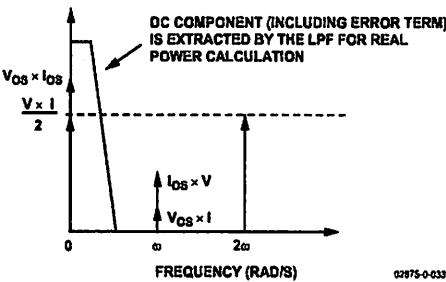


Figure 33. Effect of Channel Offsets on the Real Power Calculation

The contents of the offset correction registers are 6-bit, sign and magnitude coded. The weight of the LSB depends on the gain setting, i.e., 1, 2, 4, 8, or 16. Table 6 shows the correctable offset span for each of the gain settings and the LSB weight (mV) for the offset correction registers. The maximum value that can be written to the offset correction registers is $\pm 31d$ —see Figure 34. Figure 34 shows the relationship between the offset correction register contents and the offset (mV) on the analog inputs for a gain setting of 1. In order to perform an offset adjustment, the analog inputs should be first connected to AGND, and there should be no signal on either Channel 1 or Channel 2. A read from Channel 1 or Channel 2 using the waveform register indicates the offset in the channel. This offset can be canceled by writing an equal and opposite offset value to the Channel 1 offset register, or an equal value to the Channel 2 offset register. The offset correction can be confirmed by performing another read. Note when adjusting the offset of Channel 1, one should disable the digital integrator and the HPF.

Table 6. Offset Correction Range—Channels 1 and 2

Gain	Correctable Span	LSB Size
	± 50 mV	1.61 mV/LSB
	± 37 mV	1.19 mV/LSB
	± 30 mV	0.97 mV/LSB
	± 26 mV	0.84 mV/LSB
	± 24 mV	0.77 mV/LSB

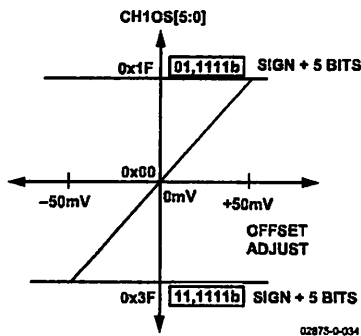


Figure 34. Channel 1 Offset Correction Range (Gain = 1)

The current and voltage rms offsets can be adjusted with the IRMSOS and VRMSOS registers—see Channel 1 RMS Offset Compensation and Channel 2 RMS Offset Compensation sections.

di/dt CURRENT SENSOR AND DIGITAL INTEGRATOR

A di/dt sensor detects changes in magnetic field caused by ac current. Figure 35 shows the principle of a di/dt current sensor.

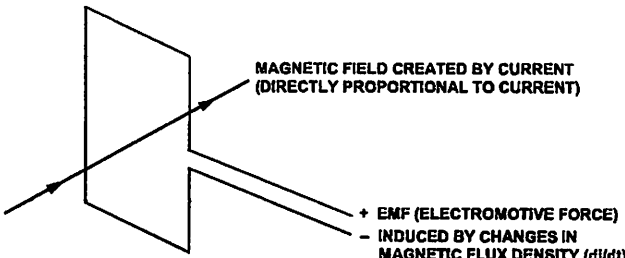


Figure 35. Principle of a di/dt Current Sensor

The flux density of a magnetic field induced by a current is directly proportional to the magnitude of the current. The changes in the magnetic flux density passing through a conductor loop generate an electromotive force (EMF) between the two ends of the loop. The EMF is a voltage signal, which is proportional to the di/dt of the current. The voltage output from the di/dt current sensor is determined by the mutual inductance between the current-carrying conductor and the di/dt sensor. The current signal needs to be recovered from the di/dt signal before it can be used. An integrator is therefore necessary to restore the signal to its original form. The ADE7753 has a built-in digital integrator to recover the current signal from the di/dt sensor. The digital integrator on Channel 1 is switched off by default when the ADE7753 is powered up. Setting the MSB of CH1OS register turns on the integrator. Figure 36 to Figure 39 show the magnitude and phase response of the digital integrator.

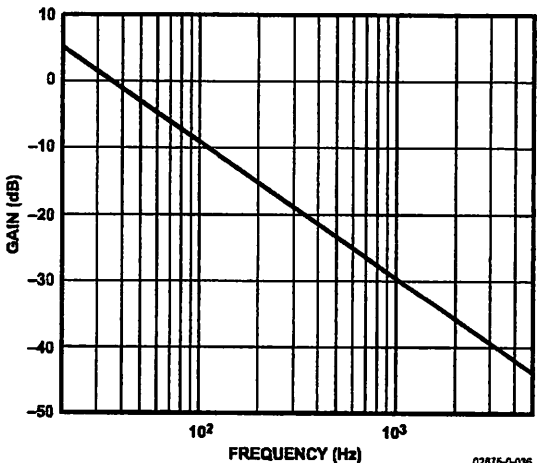


Figure 36. Combined Gain Response of the Digital Integrator and Phase Compensator

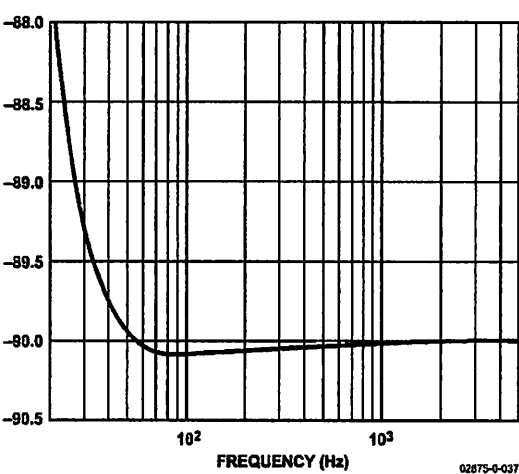


Figure 37. Combined Phase Response of the Digital Integrator and Phase Compensator

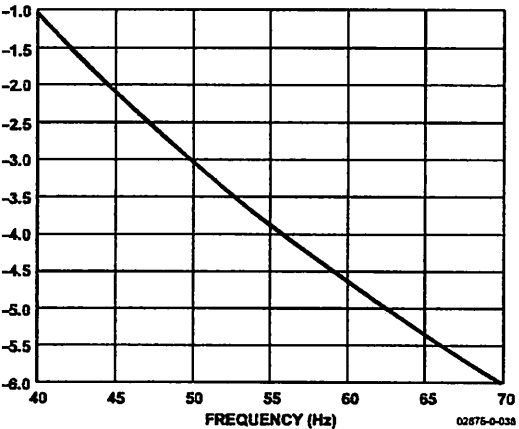


Figure 38. Combined Gain Response of the Digital Integrator and Phase Compensator (40 Hz to 70 Hz)

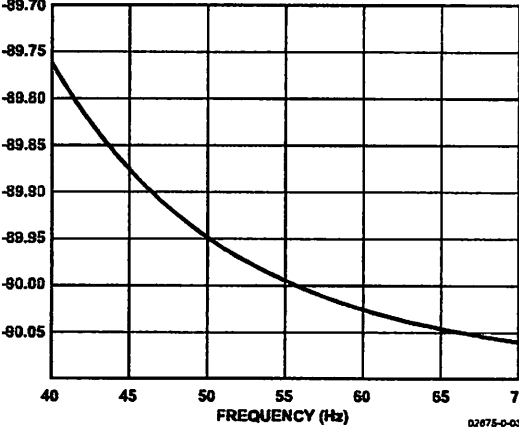


Figure 39. Combined Phase Response of the Digital Integrator and Phase Compensator (40 Hz to 70 Hz)

at the integrator has a -20 dB/dec attenuation and an approximately -90° phase shift. When combined with a di/dt the resulting magnitude and phase response should be a 1 over the frequency band of interest. The di/dt sensor $)$ dB/dec gain associated with it. It also generates signifi-

cant high frequency noise, therefore a more effective anti-aliasing filter is needed to avoid noise due to aliasing—see the Antialias Filter section.

When the digital integrator is switched off, the ADE7753 can be used directly with a conventional current sensor such as a current transformer (CT) or with a low resistance current shunt.

ZERO-CROSSING DETECTION

The ADE7753 has a zero-crossing detection circuit on Channel 2. This zero crossing is used to produce an external zero-crossing signal (ZX), and it is also used in the calibration mode—see the Calibrating an Energy Meter Based on the ADE7753 section. The zero-crossing signal is also used to initiate a temperature measurement on the ADE7753—see the Temperature Measurement section.

Figure 40 shows how the zero-crossing signal is generated from the output of LPF1.

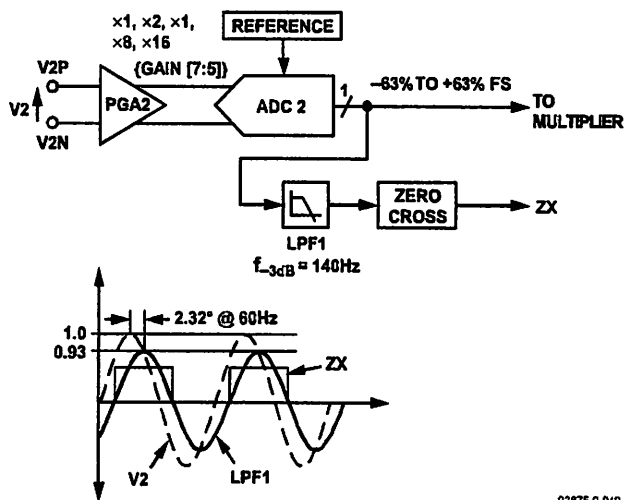


Figure 40. Zero-Crossing Detection on Channel 2

The ZX signal goes logic high on a positive-going zero crossing and logic low on a negative-going zero crossing on Channel 2. The zero-crossing signal ZX is generated from the output of LPF1. LPF1 has a single pole at 140 Hz (at CLKIN = 3.579545 MHz). As a result, there is a phase lag between the analog input signal V2 and the output of LPF1. The phase response of this filter is shown in the Channel 2 Sampling section. The phase lag response of LPF1 results in a time delay of approximately 1.14 ms (@ 60 Hz) between the zero crossing on the analog inputs of Channel 2 and the rising or falling edge of ZX.

The zero-crossing detection also drives the ZX flag in the interrupt status register. The ZX flag is set to Logic 0 on the rising and falling edge of the voltage waveform. It stays low until the status register is read with reset. An active low in the $\overline{\text{IRQ}}$ output also appears if the corresponding bit in the interrupt enable register is set to Logic 1.

the flag in the interrupt status register as well as the $\overline{\text{IRQ}}$ output are reset to their default values when the interrupt status register with reset (RSTSTATUS) is read.

Zero-Crossing Timeout

The zero-crossing detection also has an associated timeout register, ZXTOUT. This unsigned, 12-bit register is decremented (1 LSB) every $128/\text{CLKIN}$ seconds. The register is reset to its user programmed full-scale value every time a zero crossing is detected on Channel 2. The default power-on value in this register is 0xFFFF. If the internal register decrements to 0 before zero crossing is detected and the DISSAG bit in the mode register is Logic 0, the SAG pin goes active low. The absence of a zero crossing is also indicated on the $\overline{\text{IRQ}}$ pin if the ZXTOUT enable bit in the interrupt enable register is set to Logic 1. In the absence of the enable bit setting, the ZXTOUT flag in the interrupt status register is always set when the internal ZXTOUT register is decremented to 0—see the ADE7753 Interrupts section. The ZXTOUT register can be written/read by the user and has an address of 1Dh—see the ADE7753 Serial Interface section. The resolution of the register is $128/\text{CLKIN}$ seconds per LSB. Thus the maximum delay for an interrupt is 0.15 second ($128/\text{CLKIN} \times 2^{12}$).

Figure 41 shows the mechanism of the zero-crossing timeout detection when the line voltage stays at a fixed dc level for more than $\text{CLKIN}/128 \times \text{ZXTOUT}$ seconds.

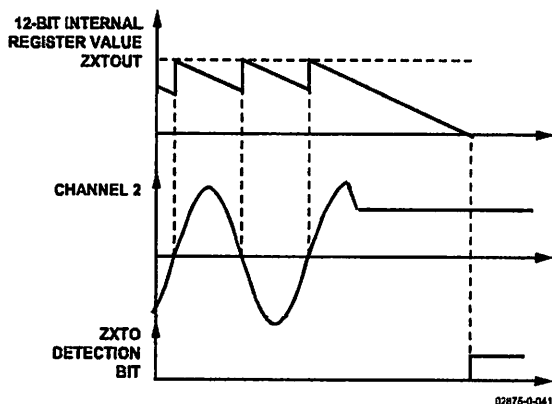


Figure 41. Zero-Crossing Timeout Detection

PERIOD MEASUREMENT

The ADE7753 also provides the period measurement of the line. The period register is an unsigned 16-bit register and is updated every period. The MSB of this register is always zero.

The resolution of this register is $2.2 \mu\text{s}/\text{LSB}$ when $\text{CLKIN} = 3.579545 \text{ MHz}$, which represents 0.013% when the line frequency is 60 Hz. When the line frequency is 60 Hz, the value of the period register is approximately $\text{CLKIN}/4/32/60 \text{ Hz} \times 16 = 7457\text{d}$. The length of the register enables the measurement of line frequencies as low as 13.9 Hz.

The period register is stable at $\pm 1 \text{ LSB}$ when the line is established and the measurement does not change. A settling time of 1.8 seconds is associated with this filter before the measurement is stable.

POWER SUPPLY MONITOR

The ADE7753 also contains an on-chip power supply monitor. The analog supply (AV_{DD}) is continuously monitored by the ADE7753. If the supply is less than $4 \text{ V} \pm 5\%$, then the ADE7753 goes into an inactive state, that is, no energy is accumulated when the supply voltage is below 4 V. This is useful to ensure correct device operation at power-up and during power-down. The power supply monitor has built-in hysteresis and filtering, which give a high degree of immunity to false triggering due to noisy supplies.

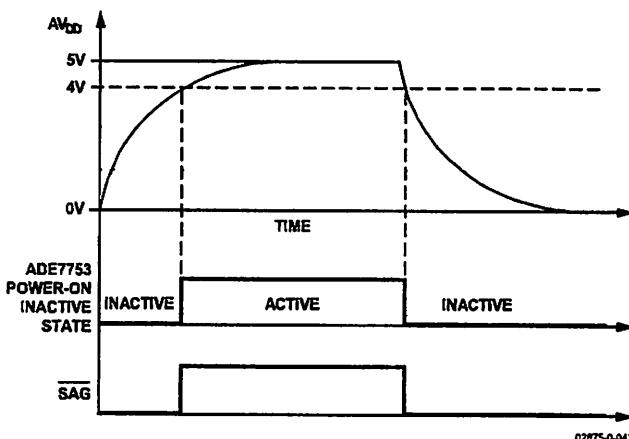


Figure 42. On-Chip Power Supply Monitor

As seen in Figure 42, the trigger level is nominally set at 4 V. The tolerance on this trigger level is about $\pm 5\%$. The $\overline{\text{SAG}}$ pin can also be used as a power supply monitor input to the MCU. The $\overline{\text{SAG}}$ pin goes logic low when the ADE7753 is in its inactive state. The power supply and decoupling for the part should be such that the ripple at AV_{DD} does not exceed $5 \text{ V} \pm 5\%$, as specified for normal operation.

LINE VOLTAGE SAG DETECTION

In addition to the detection of the loss of the line voltage signal (zero crossing), the ADE7753 can also be programmed to detect when the absolute value of the line voltage drops below a certain peak value for a number of line cycles. This condition is illustrated in Figure 43.

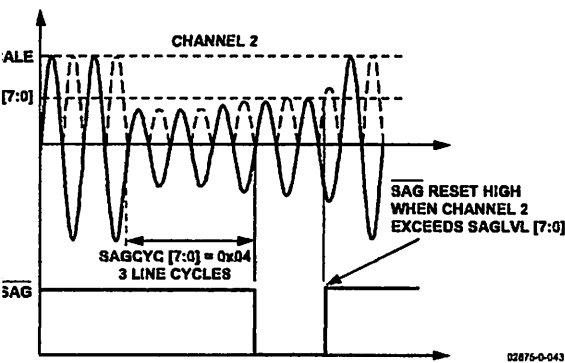


Figure 43. ADE7753 Sag Detection

Figure 43 shows the line voltage falling below a threshold that is set in the sag level register (SAGLVL[7:0]) for three line cycles. Values 0 and 1 are not valid for the SAGCYC register, and values greater than 1 represent one more than the desired number of line cycles. For example, when the sag cycle (SAGCYC[7:0]) is 0x04, the SAG pin goes active low at the end of the line cycle for which the line voltage (Channel 2 signal) falls below the threshold, if the DISSAG bit in the mode register is set to 1. As is the case when zero crossings are no longer detected, the sag event is also recorded by setting the SAG flag in the interrupt status register. If the SAG enable bit is set to 1, the $\overline{\text{IRQ}}$ logic output goes active low—see the ADE7753 Interrupts section. The SAG pin goes logic high again when the absolute value of the signal on Channel 2 exceeds the sag level set in the sag level register. This is shown in Figure 43 when the SAG pin goes high again during the fifth line cycle from the time the signal on Channel 2 first dropped below the sag level.

Sag Level Set

The contents of the sag level register (1 byte) are compared to the absolute value of the most significant byte output from LPF1. This value is shifted left by one bit, thus, for example, the nominal maximum code from LPF1 with a full-scale signal on Channel 2 is 0x18—see the Channel 2 Sampling section. Shifting one bit left gives 0x4A30. Therefore writing 0x4A to the SAG level register puts the sag detection level at full scale. Writing 0x00 puts the sag detection level at 0. The SAG level register is updated to the most significant byte of a waveform sample shifted left and detection is made when the contents of the sag level register are greater.

Peak Level Detection

The ADE7753 can also be programmed to detect when the absolute value of the voltage or current channel exceeds a set peak value. Figure 44 illustrates the behavior of the peak level detection for the voltage channel. Both Channel 1 and Channel 2 are monitored at the same time.

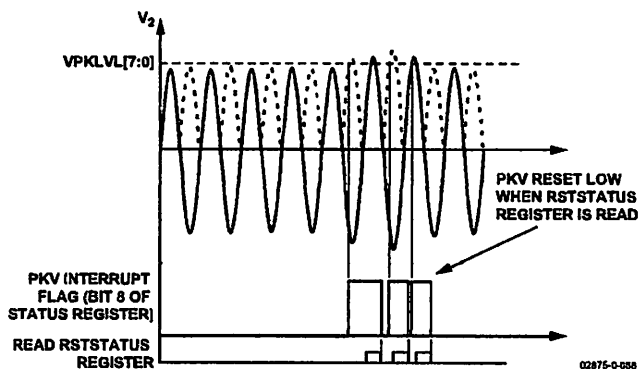


Figure 44. ADE7753 Peak Level Detection

Figure 44 shows a line voltage exceeding a threshold that is set in the voltage peak register (VPKLVL[7:0]). The voltage peak event is recorded by setting the PKV flag in the interrupt status register. If the PKV enable bit is set to Logic 1 in the interrupt mask register, the $\overline{\text{IRQ}}$ logic output goes active low. Similarly, the current peak event is recorded by setting the PKI flag in the interrupt status register—see the ADE7753 Interrupts section.

Peak Level Set

The contents of the VPKLVL and IPKLVL registers are respectively compared to the absolute value of Channel 1 and Channel 2 after they are multiplied by 2. Thus, for example, the nominal maximum code from the Channel 1 ADC with a full-scale signal is 0x2851EC—see the Channel 1 Sampling section. Multiplying by 2 gives 0x50A3D8. Therefore, writing 0x50 to the IPKLVL register, for example, puts the Channel 1 peak detection level at full scale and sets the current peak detection to its least sensitive value. Writing 0x00 puts the Channel 1 detection level at 0. The detection is done by comparing the contents of the IPKLVL register to the incoming Channel 1 sample. The $\overline{\text{IRQ}}$ pin indicates that the peak level is exceeded if the PKI or PKV bits are set in the interrupt enable register (IRQEN[15:0]) at Address 0x0A.

Peak Level Record

The ADE7753 records the maximum absolute value reached by Channel 1 and Channel 2 in two different registers—IPEAK and VPEAK, respectively. VPEAK and IPEAK are 24-bit unsigned registers. These registers are updated each time the absolute value of the waveform sample from the corresponding channel is above the value stored in the VPEAK or IPEAK register. The contents of the VPEAK register correspond to 2× the maximum absolute value observed on the Channel 2 input. The contents of IPEAK represent the maximum absolute value observed on the Channel 1 input. Reading the RSTVPEAK and RSTIPEAK registers clears their respective contents after the read operation.

DE7753 INTERRUPTS

ADE7753 interrupts are managed through the interrupt status register (STATUS[15:0]) and the interrupt enable register (IREN[15:0]). When an interrupt event occurs in the ADE7753, the corresponding flag in the status register is set to Logic 1—see the Interrupt Status Register section. If the enable bit for this interrupt in the interrupt enable register is Logic 1, then the $\overline{\text{IRQ}}$ logic output goes active low. The flag bits in the status register are set irrespective of the state of the enable bits.

To determine the source of the interrupt, the system master (MCU) should perform a read from the status register with reset (RSTATUS[15:0]). This is achieved by carrying out a read from Address 0x0C. The $\overline{\text{IRQ}}$ output goes logic high on completion of the interrupt status register read command—see the Interrupt Timing section. When carrying out a read with reset, the ADE7753 is designed to ensure that no interrupt events are missed. If an interrupt event occurs just as the status register is being read, the event is not lost and the $\overline{\text{IRQ}}$ logic output is guaranteed to go high for the duration of the interrupt status register data transfer before going logic low again to indicate the pending interrupt. See the next section for a more detailed description.

Using the ADE7753 Interrupts with an MCU

Figure 46 shows a timing diagram with a suggested implementation of ADE7753 interrupt management using an MCU. At time t_1 , the $\overline{\text{IRQ}}$ line goes active low indicating that one or more interrupt events have occurred in the ADE7753. The $\overline{\text{IRQ}}$ logic output should be tied to a negative edge-triggered external interrupt on the MCU. On detection of the negative edge, the MCU should be configured to start executing its interrupt service routine (ISR). On entering the ISR, all interrupts should be disabled by using the global interrupt enable bit. At this point, the MCU external interrupt flag can be cleared to capture interrupt events that occur during the current ISR. When the MCU interrupt flag is cleared, a read from the status register with reset is carried out. This causes the $\overline{\text{IRQ}}$ line to be reset logic high (t_2)—see the Interrupt Timing section. The status register contents are used to determine the source of the interrupt(s) and therefore the appropriate action to be taken. If a subsequent interrupt event occurs during the ISR, that event is recorded by the MCU external interrupt flag being set again (t_3). On returning from the ISR, the global interrupt mask is cleared (same instruction cycle), and the external interrupt flag causes the MCU to jump to its ISR once again. This ensures that the MCU does not miss any external interrupts.

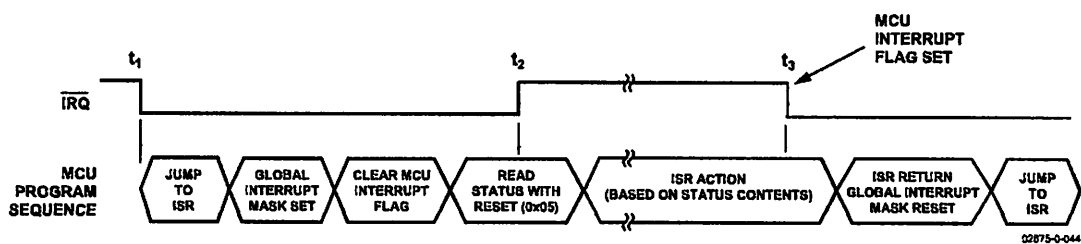


Figure 45. ADE7753 Interrupt Management

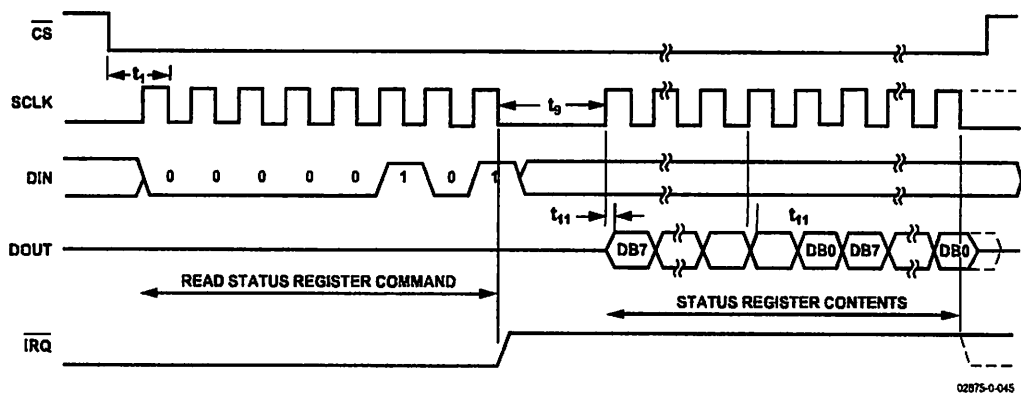


Figure 46. ADE7753 Interrupt Timing

Interrupt Timing

The ADE7753 Serial Interface section should be reviewed first when reviewing the interrupt timing. As previously described, when the $\overline{\text{IRQ}}$ output goes low, the MCU ISR must read the interrupt status register to determine the source of the interrupt. After reading the status register contents, the $\overline{\text{IRQ}}$ output is set high on the last falling edge of SCLK of the first byte transfer (interrupt status register command). The $\overline{\text{IRQ}}$ output is held high until the last bit of the next 15-bit transfer is shifted out (interrupt status register contents)—see Figure 45. If an interrupt is pending at this time, the $\overline{\text{IRQ}}$ output goes low again. If an interrupt is pending, the $\overline{\text{IRQ}}$ output stays high.

TEMPERATURE MEASUREMENT

The ADE7753 also includes an on-chip temperature sensor. A temperature measurement can be made by setting Bit 5 in the mode register. When Bit 5 is set logic high in the mode register, the ADE7753 initiates a temperature measurement on the next zero crossing. When the zero crossing on Channel 2 is detected, the voltage output from the temperature sensing circuit is connected to ADC1 (Channel 1) for digitizing. The resulting data is processed and placed in the temperature register (bits [7:0]) approximately 26 μs later ($96/\text{CLKIN}$ seconds). If enabled in the interrupt enable register (Bit 5), the $\overline{\text{IRQ}}$ output goes active low when the temperature conversion is finished.

The contents of the temperature register are signed (two's complement) with a resolution of approximately 1.5 LSB/ $^{\circ}\text{C}$. The temperature register produces a code of 0x00 when the ambient temperature is approximately -25°C . The temperature measurement is uncalibrated in the ADE7753 and has an offset error as high as $\pm 25^{\circ}\text{C}$.

ADE7753 ANALOG-TO-DIGITAL CONVERSION

Analog-to-digital conversion in the ADE7753 is carried out by two second-order Σ - Δ ADCs. For simplicity, the block diagram in Figure 47 shows a first-order Σ - Δ ADC. The converter is made up of the Σ - Δ modulator and the digital low-pass filter.

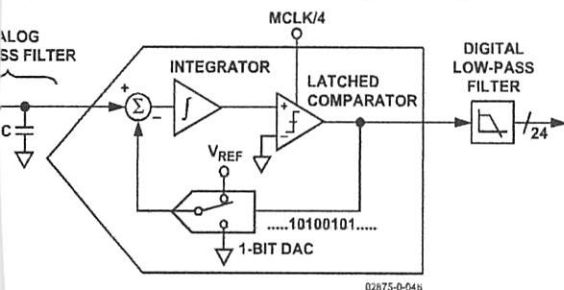


Figure 47. First-Order Σ - Δ ADC

A Σ - Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7753, the sampling clock is equal to $\text{CLKIN}/4$. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and therefore the bit stream) can approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged is a meaningful result obtained. This averaging is carried out in the second part of the ADC, the digital low-pass filter. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ - Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is oversampling. Oversampling means that the signal is sampled at a rate (frequency), which is many times higher than the bandwidth of interest. For example, the sampling rate in the ADE7753 is $\text{CLKIN}/4$ (894 kHz) and the band of interest is 40 Hz to 2 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered—see Figure 48. However, oversampling alone is not efficient enough to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling ratio of 4 is required just to increase the SNR by only 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. In the Σ - Δ modulator, the noise is shaped by the integrator, which has a high-pass-type response for the quantization noise. The result is that most of the noise is at the higher frequencies where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 48.

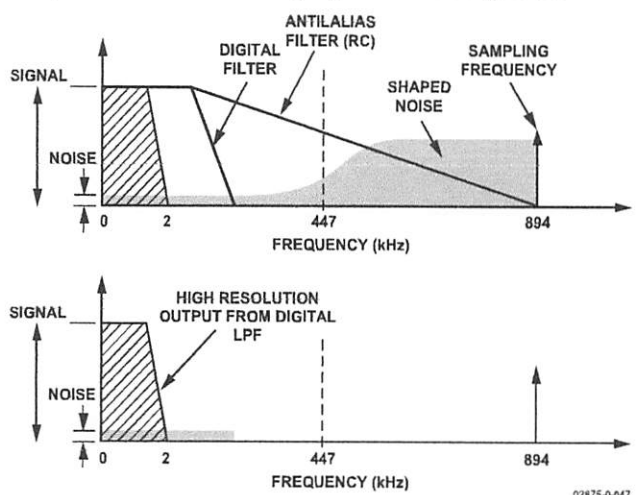


Figure 48. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

ntialias Filter

Figure 47 also shows an analog low-pass filter (RC) on the input to the modulator. This filter is present to prevent aliasing. Aliasing is an artifact of all sampled systems. Aliasing means that frequency components in the input signal to the ADC, which are higher than half the sampling rate of the ADC, appear in the sampled signal at a frequency below half the sampling rate. Figure 49 illustrates the effect. Frequency components (arrows shown in black) above half the sampling frequency (also known as the Nyquist frequency, i.e., 447 kHz) are imaged or folded back down below 447 kHz. This happens with all ADCs regardless of the architecture. In the example shown, only frequencies near the sampling frequency, i.e., 894 kHz, move into the band of interest for metering, i.e., 40 Hz to 400 kHz. This allows the use of a very simple LPF (low-pass filter) to attenuate high frequency (near 900 kHz) noise, and prevent distortion in the band of interest. For conventional current sensors, a simple RC filter (single-pole LPF) with a corner frequency of 10 kHz produces an attenuation of approximately 40 dB at 894 kHz—see Figure 49. The 20 dB per decade attenuation is usually sufficient to eliminate the effects of aliasing for conventional current sensors. However, for a di/dt sensor such as a Rogowski coil, the sensor has a 20 dB per decade gain. This neutralizes the -20 dB per decade attenuation produced by one simple LPF. Therefore, when using a di/dt sensor, care should be taken to offset the 20 dB per decade gain. One simple approach is to cascade two RC filters to produce the -40 dB per decade attenuation needed.

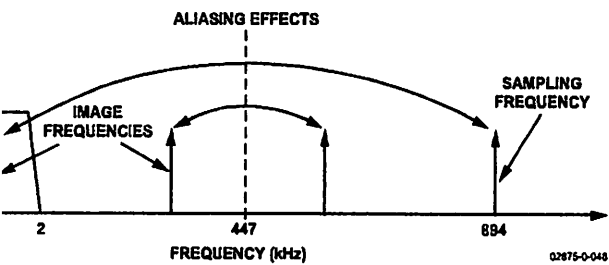


Figure 49. ADC and Signal Processing in Channel 1 Outline Dimensions

ADC Transfer Function

The following expression relates the output of the LPF in the Δ ADC to the analog input signal level. Both ADCs in the ADE7753 are designed to produce the same output code for the same input signal level.

$$\text{Code (ADC)} = 3.0492 \times \frac{V_{IN}}{V_{OUT}} \times 262,144 \quad (1)$$

Therefore with a full-scale signal on the input of 0.5 V and an internal reference of 2.42 V, the ADC output code is nominally 5,151 or 2851Fh. The maximum code from the ADC is 62,144; this is equivalent to an input signal level of ±0.794 V. However, for specified performance, it is recommended that the full-scale input signal level of 0.5 V not be exceeded.

ADE7753 Reference Circuit

Figure 50 shows a simplified version of the reference output circuitry. The nominal reference voltage at the REF_{IN/OUT} pin is 2.42 V. This is the reference voltage used for the ADCs in the ADE7753. However, Channel 1 has three input range selections that are selected by dividing down the reference value used for the ADC in Channel 1. The reference value used for Channel 1 is divided down to ½ and ¼ of the nominal value by using an internal resistor divider, as shown in Figure 50.

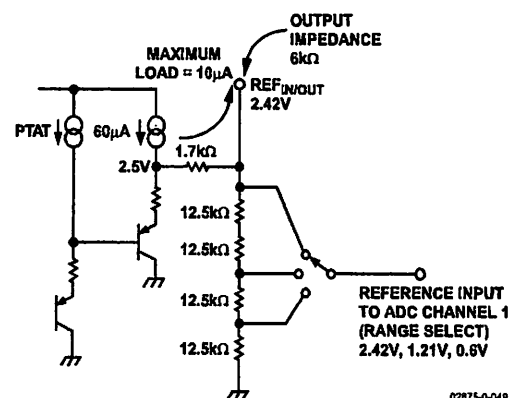


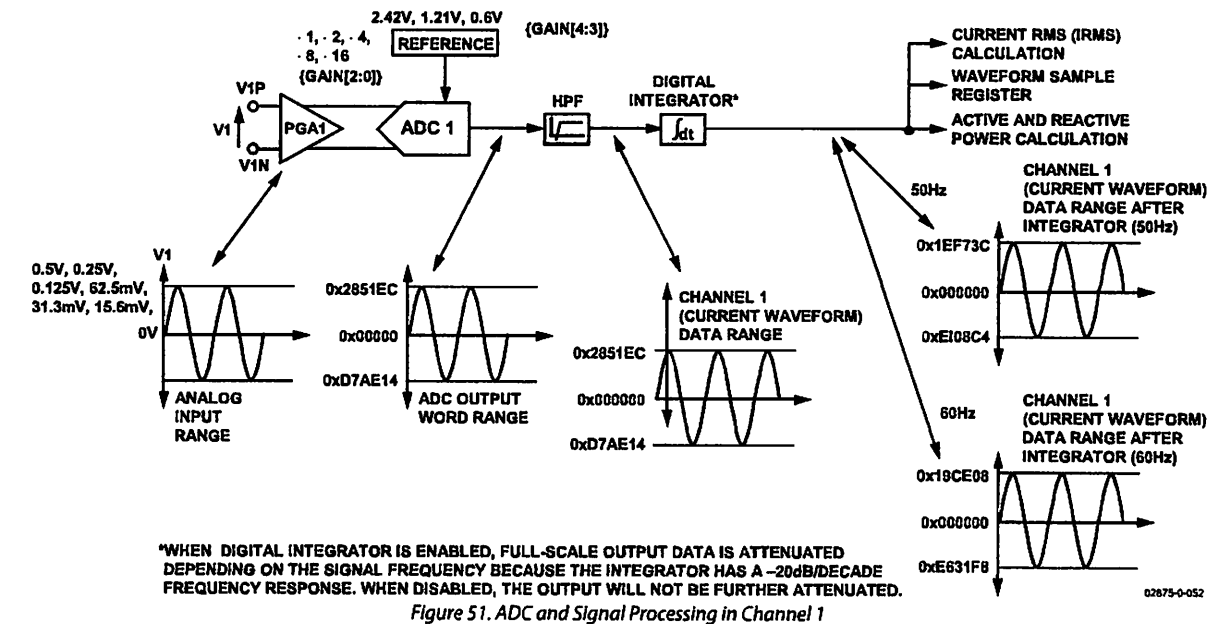
Figure 50. ADE7753 Reference Circuit Output

The REF_{IN/OUT} pin can be overdriven by an external source, for example, an external 2.5 V reference. Note that the nominal reference value supplied to the ADCs is now 2.5 V, not 2.42 V, which has the effect of increasing the nominal analog input signal range by $2.5/2.42 \times 100\% = 3\%$ or from 0.5 V to 0.5165 V.

The voltage of the ADE7753 reference drifts slightly with temperature—see the ADE7753 Specifications for the temperature coefficient specification (in ppm/°C). The value of the temperature drift varies from part to part. Since the reference is used for the ADCs in both Channels 1 and 2, any x% drift in the reference results in 2x% deviation of the meter accuracy. The reference drift resulting from temperature changes is usually very small and it is typically much smaller than the drift of other components on a meter. However, if guaranteed temperature performance is needed, one needs to use an external voltage reference. Alternatively, the meter can be calibrated at multiple temperatures. Real-time compensation can be achieved easily by using the on-chip temperature sensor.

CHANNEL 1 ADC

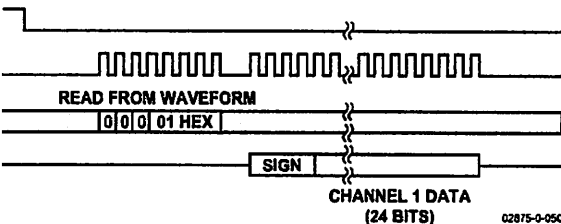
Figure 51 shows the ADC and signal processing chain for Channel 1. In waveform sampling mode, the ADC outputs a signed two's complement 24-bit data-word at a maximum of 27.9 kSPS (CLKIN/128). With the specified full-scale analog input signal of 0.5 V (or 0.25 V or 0.125 V—see the Analog Inputs section) the ADC produces an output code that is approximately between 0x2851EC (+2,642,412d) and 0xD7AE14 (-2,642,412d)—see Figure 51.



Channel 1 Sampling

Waveform samples can also be routed to the waveform register (MODE[14:13] = 1,0) to be read by the system master. In waveform sampling mode, the WSMP bit (Bit 3) in the interrupt enable register must also be set to Logic 1. The apparent power, and energy calculation remain interrupted during waveform sampling.

In waveform sampling mode, one of four output sample rates can be chosen by using Bits 11 and 12 of the mode register (MODE[11:10]). The output sample rate can be 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS—see the Mode Register (0x09) section. The interrupt request output, $\overline{IRQ}$, signals a new sample availability when active low. The timing is shown in Figure 52. The 24-bit waveform samples are transferred from the ADE7753 one byte (8 bits) at a time, with the most significant byte shifted out first. The 24-bit data-word is right justified—see the ADE7753 Interface section. The interrupt request output $\overline{IRQ}$ stays active until the interrupt routine reads the reset status register—see the ADE7753 Interrupts section.



Channel 1 RMS Calculation

Root mean square (rms) value of a continuous signal $V(t)$ is defined as

$$VRMS = V_{rms} = \sqrt{\frac{1}{T} \int_0^T V^2(t) dt} \quad (2)$$

For time sampling signals, rms calculation involves squaring the signal, taking the average and obtaining the square root:

$$VRMS = V_{rms} = \sqrt{\frac{1}{N} \times \sum_{i=1}^N V^2(i)} \quad (3)$$

The ADE7753 simultaneously calculates the rms values for Channel 1 and Channel 2 in different registers. Figure 53 shows the detail of the signal processing chain for the rms calculation on Channel 1. The Channel 1 rms value is processed from the samples used in the Channel 1 waveform sampling mode. The Channel 1 rms value is stored in an unsigned 24-bit register (IRMS). One LSB of the Channel 1 rms register is equivalent to one LSB of a Channel 1 waveform sample. The update rate of the Channel 1 rms measurement is $CLKIN/4$.

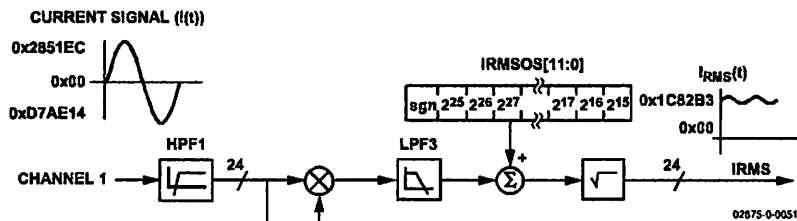


Figure 53. Channel 1 RMS Signal Processing

With the specified full-scale analog input signal of 0.5 V, the DC produces an output code that is approximately 2,642,412d—see the Channel 1 ADC section. The equivalent rms value of a full-scale ac signal are 1,868,467d (0x1C82B3). The current rms measurement provided in the ADE7753 is accurate to within 0.5% for signal input between full scale and full scale/100. Table 7 shows the settling time for the IRMS measurement, which is the time it takes for the rms register to reflect the value at the input to the current channel. The conversion from the register value to amps must be done externally in the microprocessor using an amps/LSB constant. To minimize noise, synchronize the reading of the rms register with the zero crossing of the voltage input and take the average of a number of readings.

Table 7.

	95%	100%
Integrator Off	219 ms	895 ms
Integrator On	78.5 ms	1340 ms

Channel 1 RMS Offset Compensation

The ADE7753 incorporates a Channel 1 rms offset compensation register (IRMSOS). This is a 12-bit signed register that can be used to remove offset in the Channel 1 rms calculation. An offset could exist in the rms calculation due to input noises that are integrated in the dc component of $V^2(t)$. The offset calibration allows the content of the IRMS register to match the theoretical value even when the Channel 1 input is low.

One LSB of the Channel 1 rms offset is equivalent to 32,768 LSB of the square of the Channel 1 rms register. Assuming that the maximum value from the Channel 1 rms calculation is 1,868,467d with full-scale ac inputs, then 1 LSB of the Channel 1 rms offset represents 0.46% of measurement error at -60 dB from full scale.

$$IRMS = \sqrt{IRMS_0^2 + IRMSOS \times 32768}$$
 (4)

where $IRMS_0$ is the rms measurement without offset correction. To measure the offset of the rms measurement, two data points are needed from non-zero input values, for example, the base current, I_b , and $I_{max}/100$. The offset can be calculated from these measurements.

CHANNEL 2 ADC
Channel 2 Sampling

In Channel 2 waveform sampling mode (MODE[14:13] = 1,1 and WSMP = 1), the ADC output code scaling for Channel 2 is not the same as Channel 1. The Channel 2 waveform sample is a 16-bit word and sign extended to 24 bits. For normal operation, the differential voltage signal between V2P and V2N should not exceed 0.5 V. With maximum voltage input (± 0.5 V at PGA gain of 1), the output from the ADC swings between 0x2852 and 0xD7AE ($\pm 10,322d$). However, before being passed to the waveform register, the ADC output is passed through a single-pole, low-pass filter with a cutoff frequency of 140 Hz. The plots in Figure 54 show the magnitude and phase response of this filter.

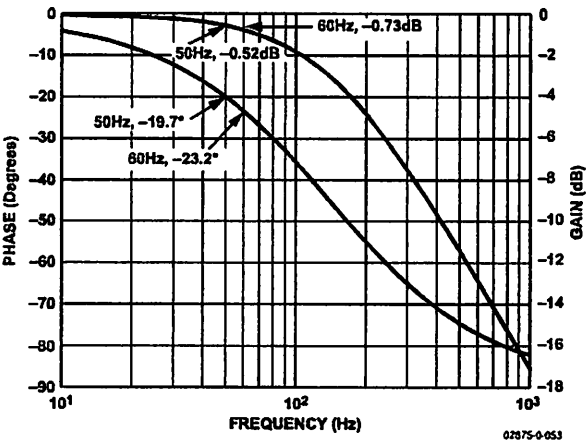


Figure 54. Magnitude and Phase Response of LPF1

The LPF1 has the effect of attenuating the signal. For example, if the line frequency is 60 Hz, then the signal at the output of LPF1 is attenuated by about 8%.

$$|H(f)| = \frac{1}{\sqrt{1 + \left(\frac{60 \text{ Hz}}{140 \text{ Hz}}\right)^2}} = 0.919 = -0.73 \text{ dB}$$
 (5)

Note LPF1 does not affect the active power calculation. The signal processing chain in Channel 2 is illustrated in Figure 55.

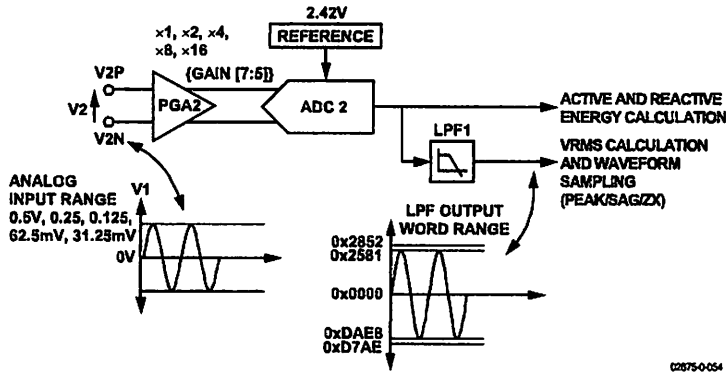


Figure 55. ADC and Signal Processing in Channel 2

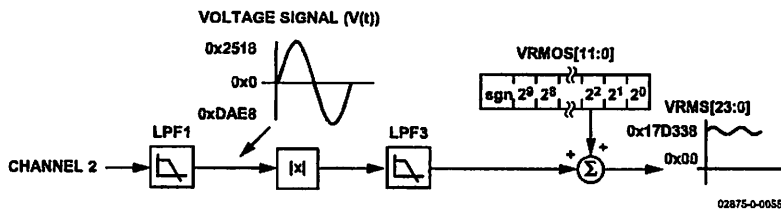


Figure 56. Channel 2 RMS Signal Processing

Channel 2 has only one analog input range (0.5 V differential). Channel 1, Channel 2 has a PGA with gain selections of 1, 2, 4, 8, and 16. For energy measurement, the output of the ADC is sent directly to the multiplier and is not filtered. An HPF is required to remove any dc offset since it is only required to remove the offset from one channel to eliminate errors due to the offset in the power calculation. When in waveform sampling mode, one of four output sample rates can be chosen by using the mode register. The available output sample rates are 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS—see the Mode Register (0x09) section. The interrupt request output $\overline{\text{IRQ}}$ indicates that a sample is available by going active low. The timing diagram is the same as that for Channel 1, as shown in Figure 52.

Channel 2 RMS Calculation

Figure 56 shows the details of the signal processing chain for the rms estimation on Channel 2. This Channel 2 rms estimation is implemented in the ADE7753 using the mean absolute value calculation, as shown in Figure 56. The Channel 2 rms value is processed from the samples used in the Channel 2 waveform sampling mode. The rms value is slightly attenuated because of LPF1. Channel 2 rms value is stored in the unsigned 24-bit VRMS register. The sampling rate of the Channel 2 rms measurement is $\text{CLKIN}/4$. For the specified full-scale ac analog input signal of 0.5 V, the output from the LPF1 swings between 0x2518 and 0xDAE8 at 100%—see the Channel 2 ADC section. The equivalent rms value of this full-scale ac signal is approximately 1,561,400 (0x17D338) in the VRMS register. The voltage rms measurement provided in the ADE7753 is accurate to within $\pm 0.5\%$ for the input between full scale and full scale/20. Table 8 shows the settling time for the VRMS measurement, which is the time for the rms register to reflect the value at the input to

the voltage channel. The conversion from the register value to volts must be done externally in the microprocessor using a volts/LSB constant. Since the low-pass filtering used for calculating the rms value is imperfect, there is some ripple noise from the 2ω term present in the rms measurement. To minimize the noise effect in the reading, synchronize the rms reading with the zero crossings of the voltage input.

Table 8.

95%	100%
220 ms	670 ms

Channel 2 RMS Offset Compensation

The ADE7753 incorporates a Channel 2 rms offset compensation register (VRMSOS). This is a 12-bit signed register that can be used to remove offset in the Channel 2 rms calculation. An offset could exist in the rms calculation due to input noises and dc offset in the input samples. The offset calibration allows the contents of the VRMS register to be maintained at 0 when no voltage is applied. One LSB of the Channel 2 rms offset is equivalent to one LSB of the rms register. Assuming that the maximum value from the Channel 2 rms calculation is 1,561,400d with full-scale ac inputs, then one LSB of the Channel 2 rms offset represents 0.064% of measurement error at -60 dB down of full scale.

$$\text{VRMS} = \text{VRMS}_0 + \text{VRMSOS} \tag{6}$$

where VRMS_0 is the rms measurement without offset correction. The voltage rms offset compensation should be done by testing the rms results at two non-zero input levels. One measurement can be done close to full scale and the other at approximately full scale/10. The voltage offset compensation can be derived

om these measurements. If the voltage rms offset register does not have enough range, the CH2OS register can also be used.

PHASE COMPENSATION

When the HPF is disabled, the phase error between Channel 1 and Channel 2 is 0 from dc to 3.5 kHz. When HPF is enabled, Channel 1 has the phase response illustrated in Figure 58 and Figure 59. Also shown in Figure 60 is the magnitude response of the filter. As can be seen from the plots, the phase response is most 0 from 45 Hz to 1 kHz. This is all that is required in typical energy measurement applications. However, despite being internally phase compensated, the ADE7753 must work with transducers, which could have inherent phase errors. For example, a phase error of 0.1° to 0.3° is not uncommon for a current transformer (CT). These phase errors can vary from part to part, and they must be corrected in order to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors. The ADE7753 provides a means of digitally calibrating these small phase errors. The ADE7753 allows a small time delay or time advance to be introduced into the signal processing chain to compensate for small phase errors. Because the compensation is a time shift, this technique should be used only for small phase errors in the range of 0.1° to 0.5°. Correcting large phase errors using a time shift technique can introduce significant phase errors at higher harmonics.

The phase calibration register (PHCAL[5:0]) is a two's complement signed single-byte register that has values ranging from 0x21 (-31d) to 0x1F (31d).

The register is centered at 0x0D, so that writing 0x0D to the register gives 0 delay. By changing the PHCAL register, the time delay in the Channel 2 signal path can change from -102.12 μs to +39.96 μs (CLKIN = 3.579545 MHz). One LSB is equivalent to 2.22 μs (CLKIN/8) time delay or advance. A line frequency of 60 Hz gives a phase resolution of 0.048° at the fundamental (i.e., 360° × 2.22 μs × 60 Hz). Figure 57 illustrates how the phase compensation is used to remove a 0.1° phase lead in Channel 1 due to the external transducer. To cancel the lead (0.1°) in Channel 1, a phase lead must also be introduced into Channel 2. The resolution of the phase adjustment allows the introduction of a phase lead in increment of 0.048°. The phase lead is achieved by introducing a time advance into Channel 2. A time advance of 4.48 μs is made by writing -2 (0x0B) to the time delay block, thus reducing the amount of time delay by 4.48 μs, or equivalently, a phase lead of approximately 0.1° at line frequency of 60 Hz. 0x0B represents -2 because the register is centered with 0 at 0x0D.

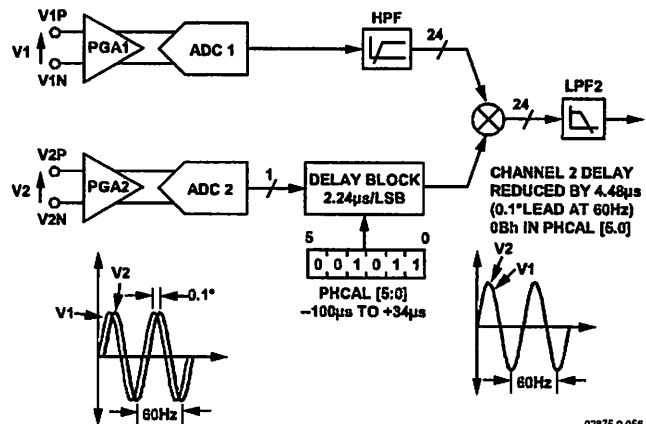


Figure 57. Phase Calibration

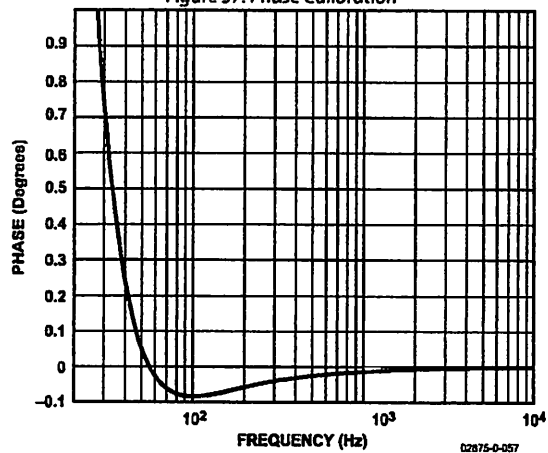


Figure 58. Combined Phase Response of the HPF and Phase Compensation (10 Hz to 1 kHz)

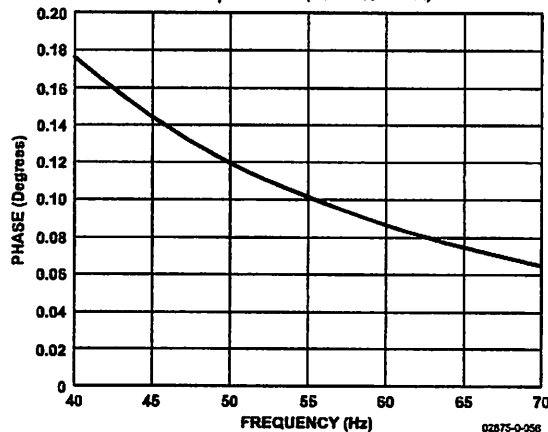


Figure 59. Combined Phase Response of the HPF and Phase Compensation (40 Hz to 70 Hz)

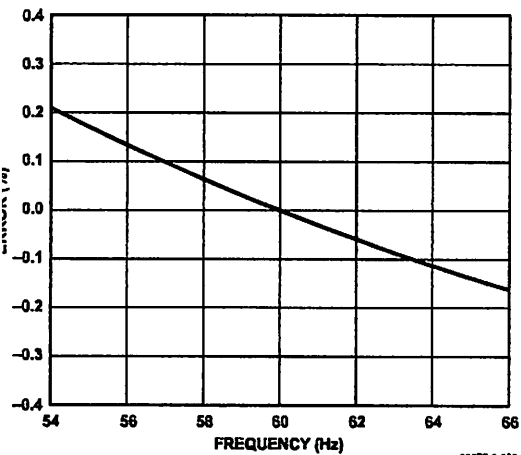


Figure 60. Combined Gain Response of the HPF and Phase Compensation

ACTIVE POWER CALCULATION

Active power is defined as the rate of energy flow from source to load. It is defined as the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal and is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. Equation 9 gives an expression for the instantaneous power in an ac system.

$$p(t) = \sqrt{2} \times V \sin(\omega t) \quad (7)$$

$$p(t) = \sqrt{2} \times I \sin(\omega t) \quad (8)$$

where V is the rms voltage.

where I is the rms current.

$$p(t) = v(t) \times i(t) \quad (9)$$
$$p(t) = VI - VI \cos(2\omega t) \quad (10)$$

The average power over an integral number of line cycles (n) is given by the expression in Equation 10.

$$P = \frac{1}{nT} \int_0^{nT} p(t) dt = VI \quad (10)$$

where T is the line cycle period.

Power is referred to as the active or real power.

Since the active power is equal to the dc component of the instantaneous power signal $p(t)$ in Equation 8, i.e., VI . This relationship is used to calculate active power in the ADE7753. The instantaneous power signal $p(t)$ is generated by multiplying

the current and voltage signals. The dc component of the instantaneous power signal is then extracted by LPF2 (low-pass filter) to obtain the active power information. This process is illustrated in Figure 61.

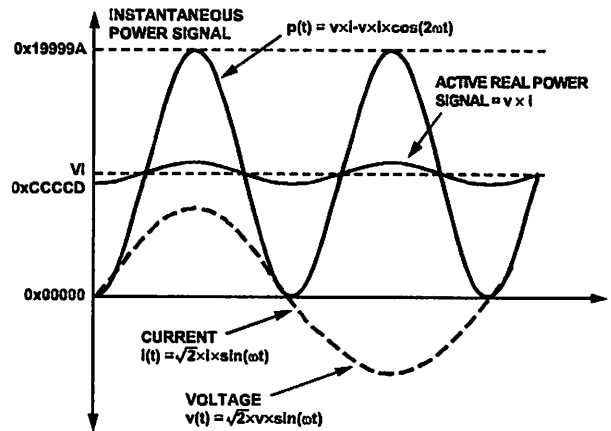


Figure 61. Active Power Calculation

Since LPF2 does not have an ideal “brick wall” frequency response—see Figure 62, the active power signal has some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Because the ripple is sinusoidal in nature, it is removed when the active power signal is integrated to calculate energy—see the Energy Calculation section.

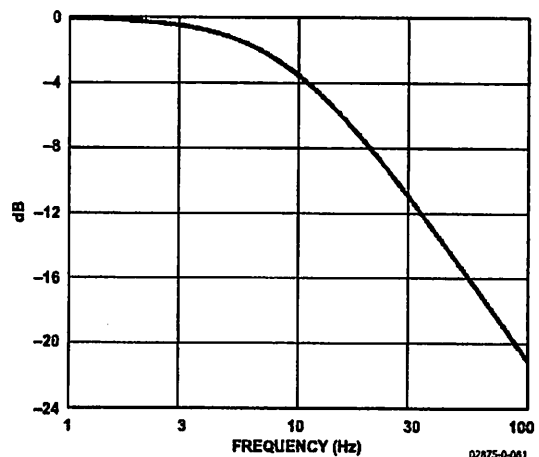


Figure 62. Frequency Response of LPF2

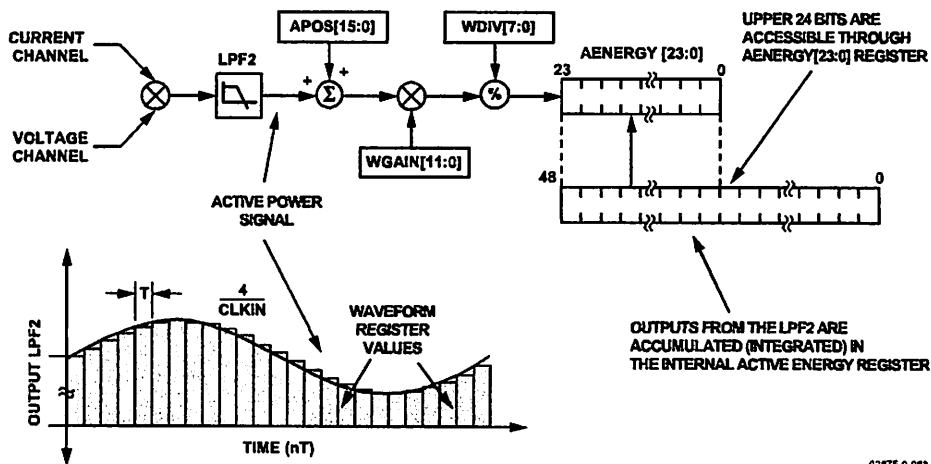


Figure 63. ADE7753 Active Energy Calculation

Figure 63 shows the signal processing chain for the active power calculation in the ADE7753. As explained, the active power is calculated by low-pass filtering the instantaneous power signal. Note that when reading the waveform samples from the output of LPF2, the gain of the active energy can be adjusted by using the multiplier and watt gain register (WGAIN[11:0]). The gain is adjusted by writing a two's complement 12-bit word to the watt gain register. Equation 11 shows how the gain adjustment is related to the contents of the watt gain register:

$$\text{Output WGAIN} = \left(\text{Active Power} \times \left\{ 1 + \frac{\text{WGAIN}}{2^{12}} \right\} \right) \quad (11)$$

For example, when 0x7FF is written to the watt gain register, the power output is scaled up by 50%. $0x7FF = 2047d$, $2047/2^{12} = 0.5$. Similarly, $0x800 = -2048d$ (signed two's complement) and the power output is scaled by -50%. Each LSB scales the power output by 0.0244%. Figure 64 shows the maximum code (in hex) output range for the active power signal (LPF2). Note that the output range changes depending on the contents of the watt gain register. The minimum output range is given when the watt gain register contents are equal to 0x800, and the maximum range is given by writing 0x7FF to the watt gain register. This can be used to calibrate the active power (or energy) calculation in the ADE7753.

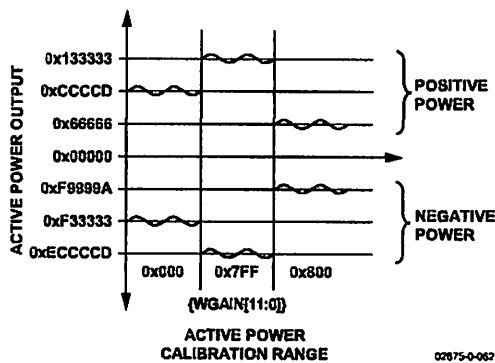


Figure 64. Active Power Calculation Output Range

ENERGY CALCULATION

As stated earlier, power is defined as the rate of energy flow. This relationship can be expressed mathematically in Equation 12.

$$P = \frac{dE}{dt} \quad (12)$$

where:

P is power.

E is energy.

Conversely, energy is given as the integral of power.

$$E = \int P dt \quad (13)$$

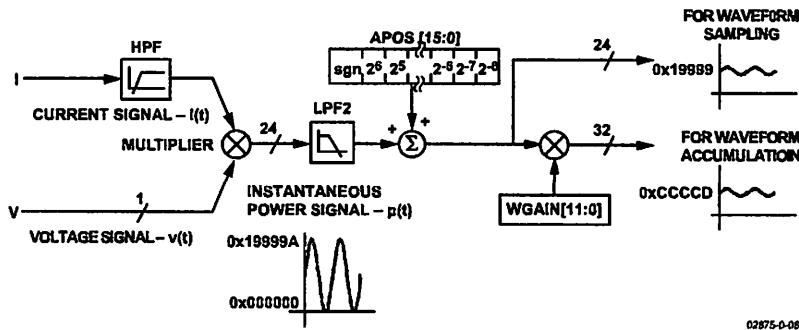


Figure 65. Active Power Signal Processing

DE7753 achieves the integration of the active power signal by continuously accumulating the active power signal in an internal 49-bit energy register. The active energy register ENERGY[23:0] represents the upper 24 bits of this internal register. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 14 describes the relationship.

$$E = \int p(t)dt = \lim_{T \rightarrow 0} \left\{ \sum_{n=1}^{\infty} p(nT) \times T \right\} \quad (14)$$

n is the discrete time sample number.
T is the sample period.

The discrete time sample period (T) for the accumulation register in the ADE7753 is 1.1µs (4/CLKIN). As well as accumulating the energy, this integration removes any sinusoidal components that might be in the active power signal. Figure 65 illustrates this discrete time integration or accumulation. The active power signal in the waveform register is continuously added to the internal active energy register. This addition is a signed operation; therefore negative energy is subtracted from the active energy register contents. The exception to this is when POAM is enabled in the MODE[15:0] register. In this case, only positive power contributes to the active energy accumulation—see the Power-Only Accumulation Mode section.

The output of the multiplier is divided by WDIV. If the value in the WDIV register is equal to 0, then the internal active energy register is divided by 1. WDIV is an 8-bit unsigned register. After dividing by WDIV, the active energy is accumulated in an internal energy accumulation register. The upper 24 bits of the energy register are accessible through a read to the active energy register (AENERGY[23:0]). A read to the RAENERGY register returns the content of the AENERGY register and the upper 24 bits of the internal register are cleared. As shown in Figure 65, the active power signal is accumulated in an internal 49-bit signed register. The active power signal can be read from the waveform register by setting MODE[14:13] = 0,0 and setting the WSMP register (bit 3) in the interrupt enable register to 1. Like the Channel 1 and Channel 2 waveform sampling modes, the waveform data is available at sample rates of 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS—see Figure 52.

Figure 66 shows this energy accumulation for full-scale signals (sinusoidal) on the analog inputs. The three curves displayed illustrate the minimum period of time it takes the energy register to roll over when the active power gain register contents are 0x7FF, 0x000, and 0x800. The watt gain register is used to carry out power calibration in the ADE7753. As shown, the fastest integration time occurs when the watt gain register is set to maximum full scale, i.e., 0x7FF.

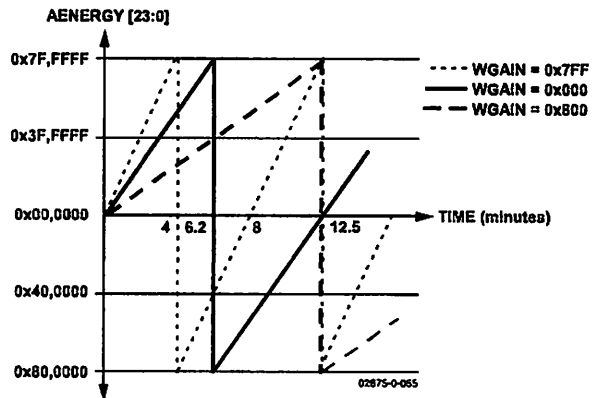


Figure 66. Energy Register Rollover Time for Full-Scale Power (Minimum and Maximum Power Gain)

Note that the energy register contents rolls over to full-scale negative (0x800000) and continues to increase in value when the power or energy flow is positive—see Figure 66. Conversely, if the power is negative, the energy register underflows to full-scale positive (0x7FFFFFFF) and continues to decrease in value.

By using the interrupt enable register, the ADE7753 can be configured to issue an interrupt (IRQ) when the active energy register is greater than half-full (positive or negative) or when an overflow or underflow occurs.

Integration Time under Steady Load

As mentioned in the last section, the discrete time sample period (T) for the accumulation register is 1.1 µs (4/CLKIN). With full-scale sinusoidal signals on the analog inputs and the WGAIN register set to 0x000, the average word value from each LPF2 is 0xCCCCD—see Figure 61. The maximum positive value that can be stored in the internal 49-bit register is 2⁴⁸ or

FFFF,FFFF,FFFF before it overflows. The integration time under these conditions with WDIV = 0 is calculated as follows:

$$Time = \frac{0 \times FFFF, FFFF, FFFF}{0 \times CCCC D} \times 1.12 \mu s = 375.8 s = 6.26 min(15)$$

When WDIV is set to a value different from 0, the integration time varies, as shown in Equation 16.

$$Time = Time_{WDIV=0} \times WDIV(16)$$

POWER OFFSET CALIBRATION

The ADE7753 also incorporates an active power offset register (APOS[15:0]). This is a signed twos complement 16-bit register that can be used to remove offsets in the active power calculation—see Figure 65. An offset could exist in the power calculation due to crosstalk between channels on the PCB or in the IC itself. The offset calibration allows the contents of the active power register to be maintained at 0 when no power is being consumed. The 256 LSBs (APOS = 0x0100) written to the active power offset register are equivalent to 1 LSB in the waveform sample register. Assuming the average value, output from LPF2 is 838,861 (838,861d) when inputs on Channels 1 and 2 are both at full scale. At -60 dB down on Channel 1 (1/1000 of the Channel 1 full-scale input), the average word value output from LPF2 is 838.861 (838,861/1,000). One LSB in the LPF2 output is a measurement error of $1/838,861 \times 100\% = 0.119\%$ of the average value. The active power offset register has a resolution equal to 1/256 LSB of the waveform register, therefore the power set correction resolution is $0.00047\%/LSB$ ($0.119\%/256$) at -60 dB.

ENERGY-TO-FREQUENCY CONVERSION

The ADE7753 also provides energy-to-frequency conversion for calibration purposes. After initial calibration at manufacturing, the manufacturer or end customer often verify the energy meter calibration. One convenient way to verify the meter calibration is for the manufacturer to provide an output frequency, which is proportional to the energy or active power under steady load conditions. This output frequency can provide a simple, single-referenced, optically isolated interface to external calibration equipment. Figure 67 illustrates the energy-to-frequency conversion in the ADE7753.

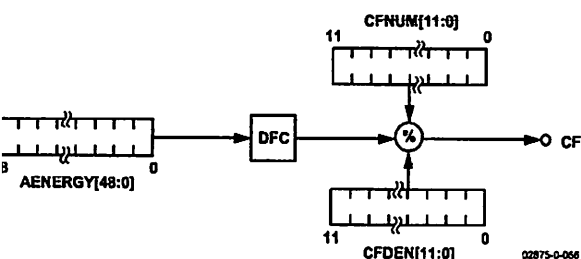


Figure 67. ADE7753 Energy-to-Frequency Conversion

The digital-to-frequency converter (DFC) is used to generate the pulsed output. The DFC generates a pulse each time 1 LSB of the active energy register is accumulated. An output pulse is generated when $(CFDEN + 1)/(CFNUM + 1)$ number of pulses

are generated at the DFC output. Under steady load conditions, the output frequency is proportional to the active power.

The maximum output frequency, with ac input signals at full scale and CFNUM = 0x00 and CFDEN = 0x00, is approximately 23 kHz.

The ADE7753 incorporates two registers, CFNUM[11:0] and CFDEN[11:0], to set the CF frequency. These are unsigned 12-bit registers, which can be used to adjust the CF frequency to a wide range of values. These frequency-scaling registers are 12-bit registers, which can scale the output frequency by $1/2^{12}$ to 1 with a step of $1/2^{12}$.

If the value 0 is written to any of these registers, the value 1 would be applied to the register. The ratio $(CFNUM + 1)/(CFDEN + 1)$ should be smaller than 1 to ensure proper operation. If the ratio of the registers $(CFNUM + 1)/(CFDEN + 1)$ is greater than 1, the register values would be adjusted to a ratio $(CFNUM + 1)/(CFDEN + 1)$ of 1. For example, if the output frequency is 1.562 kHz while the contents of CFDEN are 0 (0x000), then the output frequency can be set to 6.1 Hz by writing 0xFF to the CFDEN register.

When CFNUM and CFDEN are both set to one, the CF pulse width is fixed at 16 CLKIN/4 clock cycles, approximately 18 μs with a CLKIN of 3.579545 MHz. If the CF pulse output is longer than 180 ms for an active energy frequency of less than 5.56 Hz, the pulse width is fixed at 90 ms. Otherwise, the pulse width is 50% of the duty cycle.

The output frequency has a slight ripple at a frequency equal to twice the line frequency. This is due to imperfect filtering of the instantaneous power signal to generate the active power signal—see the Active Power Calculation section. Equation 9 from the Active Power Calculation section gives an expression for the instantaneous power signal. This is filtered by LPF2, which has a magnitude response given by Equation 17.

$$|H(f)| = \frac{1}{\sqrt{1 + \frac{f^2}{8.9^2}}}(17)$$

The active power signal (output of LPF2) can be rewritten as

$$p(t) = VI - \left[\frac{VI}{\sqrt{1 + \left(\frac{2f_L}{8.9} \right)^2}} \right] \times \cos(4\pi f_L t)(18)$$

where f_L is the line frequency, for example, 60 Hz.

From Equation 13,

$$E(t) = VI t - \left[\frac{VI}{4\pi f_L \sqrt{1 + \left(\frac{2f_L}{8.9} \right)^2}} \right] \times \sin(4\pi f_L t)(19)$$

LINE CYCLE ENERGY ACCUMULATION MODE

In line cycle energy accumulation mode, the energy accumulation of the ADE7753 can be synchronized to the Channel 2 zero crossing so that active energy can be accumulated over an integral number of half line cycles. The advantage of summing the active energy over an integer number of line cycles is that the sinusoidal component in the active energy is reduced to 0. This eliminates any ripple in the energy calculation. Energy is accumulated more accurately and in a shorter time because the integration period can be shortened. By using the line cycle energy accumulation mode, the energy calibration can be greatly simplified, and the time required to calibrate the meter can be significantly reduced. The ADE7753 is placed in line cycle energy accumulation mode by setting Bit 7 (CYCMODE) in the mode register. In line cycle energy accumulation mode, the ADE7753 accumulates the active power signal in the WAENERGY register (Address 0x04) for an integral number of line cycles, as shown in Figure 69. The number of half line cycles is specified in the LINECYC register (Address 0x1C). The ADE7753 can accumulate active power for up to 65,535 half line cycles. Because the active power is integrated on an integral number of line cycles, at the end of a line cycle energy accumulation cycle the CYCEND flag in the interrupt status register is set (Bit 2). If the CYCEND enable bit in the interrupt enable register is enabled, the IRQ output also goes active low. Thus the IRQ line can also be used to signal the completion of the line cycle energy accumulation. Another calibration cycle can start as long as the CYCMODE bit in the mode register is set.

From Equations 13 and 18,

$$E(t) = \int_0^{nT} VI dt - \left\{ \frac{VI}{\sqrt{1 + \left(\frac{f}{8.9}\right)^2}} \right\} \int_0^{nT} \cos(2\pi ft) dt \quad (20)$$

where:
 n is an integer.
 T is the line cycle period.

Since the sinusoidal component is integrated over an integer number of line cycles, its value is always 0. Therefore,

$$E = \int_0^{nT} VI dt + 0 \quad (21)$$

$$E(t) = VI nT \quad (22)$$

Note that in this mode, the 16-bit LINECYC register can hold a maximum value of 65,535. In other words, the line energy accumulation mode can be used to accumulate active energy for a maximum duration over 65,535 half line cycles. At 60 Hz line frequency, it translates to a total duration of $65,535/120 \text{ Hz} = 546 \text{ seconds}$.

POSITIVE-ONLY ACCUMULATION MODE

In positive-only accumulation mode, the energy accumulation is done only for positive power, ignoring any occurrence of negative power above or below the no-load threshold, as shown in Figure 70. The CF pulse also reflects this accumulation method when in this mode. The ADE7753 is placed in positive-only accumulation mode by setting the MSB of the mode register (MODE[15]). The default setting for this mode is off. Transitions in the direction of power flow, going from negative to positive or positive to negative, set the IRQ pin to active low if the interrupt enable register is enabled. The interrupt status registers, PPOS and PNEG, show which transition has occurred—see the ADE7753 register descriptions in Table 12.

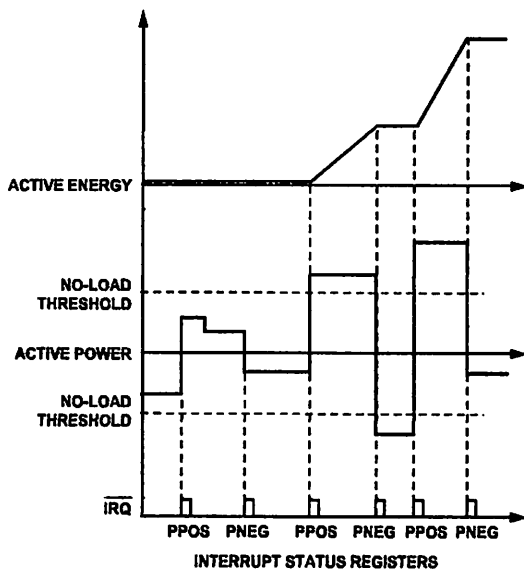


Figure 70. Energy Accumulation in Positive-Only Accumulation Mode

NO-LOAD THRESHOLD

The ADE7753 includes a no-load threshold feature on the active energy that eliminates any creep effects in the meter. The ADE7753 accomplishes this by not accumulating energy if the multiplier output is below the no-load threshold. This threshold is 0.001% of the full-scale output frequency of the multiplier. Compare this value to the IEC1036 specification, which states that the meter must start up with a load equal to or less than 0.4% Ib. This standard translates to .0167% of the full-scale output frequency of the multiplier.

REACTIVE POWER CALCULATION

Reactive power is defined as the product of the voltage and current waveforms when one of these signals is phase-shifted by

The resulting waveform is called the instantaneous reactive power signal. Equation 25 gives an expression for the instantaneous reactive power signal in an ac system when the phase of the current channel is shifted by $+90^\circ$.

$$v(t) = \sqrt{2}V \sin(\omega t + \theta) \quad (23)$$

$$i(t) = \sqrt{2}I \sin(\omega t)$$

$$i'(t) = \sqrt{2}I \sin\left(\omega t + \frac{\pi}{2}\right) \quad (24)$$

where θ is the phase difference between the voltage and current.

V is the rms voltage.

I is the rms current.

$$p(t) = v(t) \times i'(t) \quad (25)$$

$$p(t) = VI \sin(\theta) + VI \sin(2\omega t + \theta)$$

The average reactive power over an integral number of lines (n) is given in Equation 26.

$$RP = \frac{1}{nT} \int_0^{nT} Rp(t) dt = VI \sin(\theta) \quad (26)$$

where:

T is the line cycle period.

RP is referred to as the reactive power.

Note that the reactive power is equal to the dc component of the instantaneous reactive power signal $Rp(t)$ in Equation 25. This is the relationship used to calculate reactive power in the ADE7753. The instantaneous reactive power signal $Rp(t)$ is generated by multiplying Channel 1 and Channel 2. In this case, the phase of Channel 1 is shifted by $+90^\circ$. The dc component of the instantaneous reactive power signal is then extracted by a low-pass filter in order to obtain the reactive power information. Figure 71 shows the signal processing in the reactive power calculation in the ADE7753.

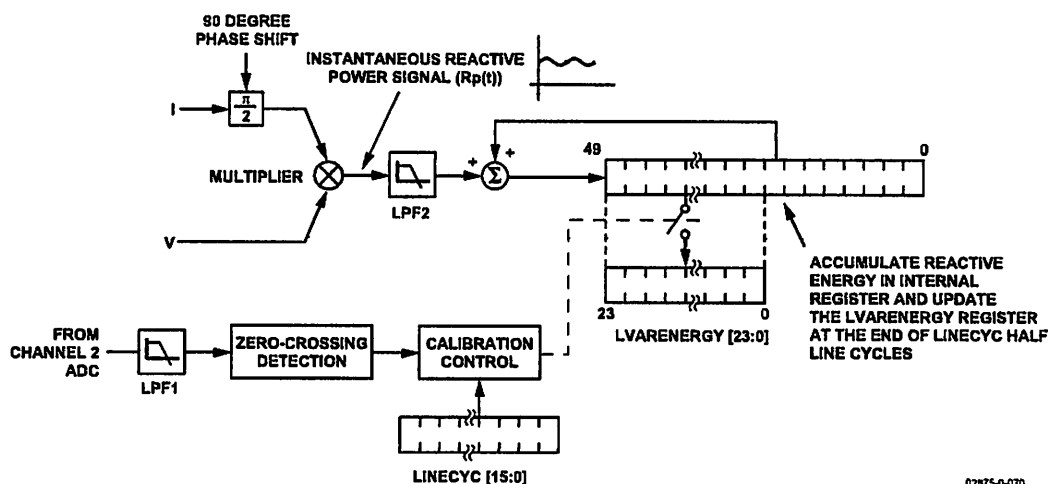


Figure 71. Reactive Power Signal Processing

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The features of the line reactive energy accumulation are the same as the line active energy accumulation. The number of half line cycles is specified in the LINECYC register. LINECYC is an unsigned 16-bit register. The ADE7753 can accumulate reactive power for up to 65535 combined half cycles. At the end of an energy calibration cycle, the CYCEND flag in the interrupt status register is set. If the CYCEND mask bit in the interrupt mask register is enabled, the $\overline{\text{IRQ}}$ output also goes active low. Thus the $\overline{\text{IRQ}}$ line can also be used to signal the end of a calibration. The ADE7753 accumulates the reactive power signal in the LVARENERGY register for an integer number of half cycles, as shown in Figure 71.

Sign of Reactive Power Calculation

Note that the average reactive power is a signed calculation. The phase shift filter has -90° phase shift when the integrator is enabled, and $+90^\circ$ phase shift when the integrator is disabled. Table 9 summarizes the relationship between the phase difference between the voltage and the current and the sign of the resulting VAR calculation.

Table 9. Sign of Reactive Power Calculation

Angle	Integrator	Sign
between 0° to 90°	Off	Positive
between -90° to 0°	Off	Negative
between 0° to 90°	On	Positive
between -90° to 0°	On	Negative

Apparent Power Calculation

The apparent power is defined as the maximum power that can be delivered to a load. V_{rms} and I_{rms} are the effective voltage and current delivered to the load; the apparent power (AP) is defined as $V_{\text{rms}} \times I_{\text{rms}}$. The angle θ between the active power and the apparent power generally represents the phase shift due to non-resistive loads. For single-phase applications, θ represents the angle between the voltage and the current signals—see Figure 72.

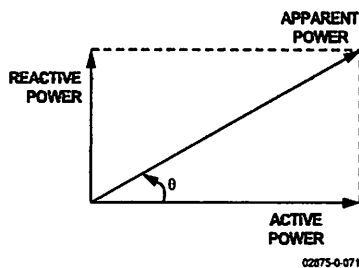


Figure 72. Power Triangle

The apparent power is defined as $V_{\text{rms}} \times I_{\text{rms}}$. This expression is dependent from the phase angle between the current and the voltage.

Figure 73 illustrates the signal processing in each phase for the calculation of the apparent power in the ADE7753.

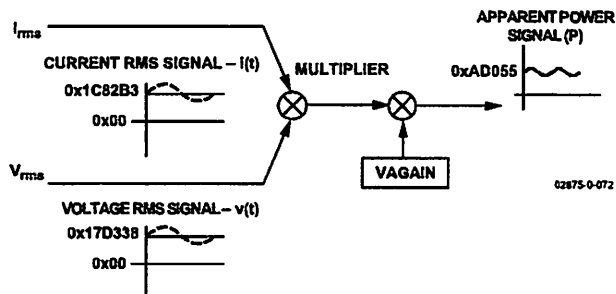


Figure 73. Apparent Power Signal Processing

The gain of the apparent energy can be adjusted by using the multiplier and VAGAIN register (VAGAIN[11:0]). The gain is adjusted by writing a twos complement, 12-bit word to the VAGAIN register. Equation 29 shows how the gain adjustment is related to the contents of the VAGAIN register.

$$\text{Output VAGAIN} = \left(\text{Apparent Power} \times \left\{ 1 + \frac{\text{VAGAIN}}{2^{12}} \right\} \right) \quad (29)$$

For example, when 0x7FF is written to the VAGAIN register, the power output is scaled up by 50%. $0x7FF = 2047d$, $2047/2^{12} = 0.5$. Similarly, $0x800 = -2047d$ (signed twos complement) and power output is scaled by -50% . Each LSB represents 0.0244% of the power output. The apparent power is calculated with the current and voltage rms values obtained in the rms blocks of the ADE7753. Figure 74 shows the maximum code (hexadecimal) output range of the apparent power signal. Note that the output range changes depending on the contents of the apparent power gain registers. The minimum output range is given when the apparent power gain register content is equal to 0x800 and the maximum range is given by writing 0x7FF to the apparent power gain register. This can be used to calibrate the apparent power (or energy) calculation in the ADE7753.

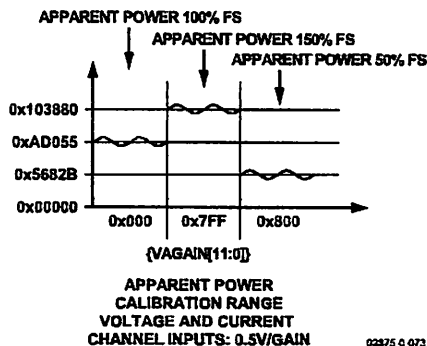


Figure 74. Apparent Power Calculation Output Range

Apparent Power Offset Calibration

Each rms measurement includes an offset compensation register to calibrate and eliminate the dc component in the rms value—see Channel 1 RMS Calculation and Channel 2 RMS Calculation sections. The Channel 1 and Channel 2 rms values are then multiplied together in the apparent power signal processing. Since no additional offsets are created in the multiplication of the rms values, there is no specific offset

ensation in the apparent power signal processing. The compensation of the apparent power measurement is by calibrating each individual rms measurement.

APPARENT ENERGY CALCULATION

Apparent energy is given as the integral of the apparent

$$\text{Apparent Energy} = \int \text{Apparent Power}(t) dt \quad (30)$$

DE7753 achieves the integration of the apparent power by continuously accumulating the apparent power signal internal 49-bit register. The apparent energy register ENERGY[23:0] represents the upper 24 bits of this internal register. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 31 assesses the relationship

$$\text{Apparent Energy} = \lim_{T \rightarrow 0} \left\{ \sum_{n=0}^{\infty} \text{Apparent Power}(nT) \times T \right\} \quad (31)$$

where

n = discrete time sample number.

T = sample period.

T = discrete time sample period (T) for the accumulation register in the ADE7753 is $1.1 \mu\text{s}$ ($4/\text{CLKIN}$).

Figure 75 shows this discrete time integration or accumulation. Apparent power signal is continuously added to the internal register. This addition is a signed addition even if the apparent power remains theoretically always positive.

The upper 24 bits of the internal register are divided by VADIV. If the content of the VADIV register is 0, then the internal active energy register is divided by 1. VADIV is an 8-bit unsigned register. The upper 24 bits are then written in the 24-bit apparent energy register (VAENERGY[23:0]). The RVAENERGY register (24 bits) is provided to read the apparent energy. This register is reset to 0 after a read operation.

Figure 76 shows this apparent energy accumulation for full-scale signals (sinusoidal) on the analog inputs. The three curves plotted illustrate the minimum time it takes the energy register to rollover when the VAGAIN registers content is equal to 0x7FF, 0x000, and 0x800. The VAGAIN register is used to carry out apparent power calibration in the ADE7753. As shown, the fastest rollover time occurs when the VAGAIN register is set to maximum full scale, i.e., 0x7FF.

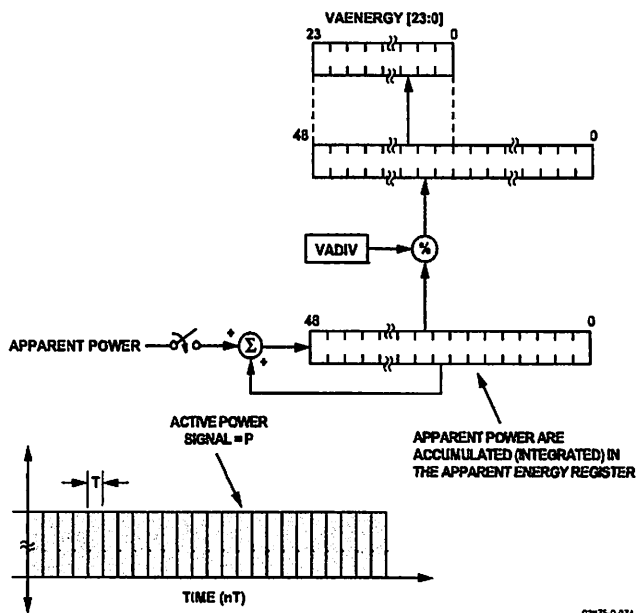


Figure 75. ADE7753 Apparent Energy Calculation

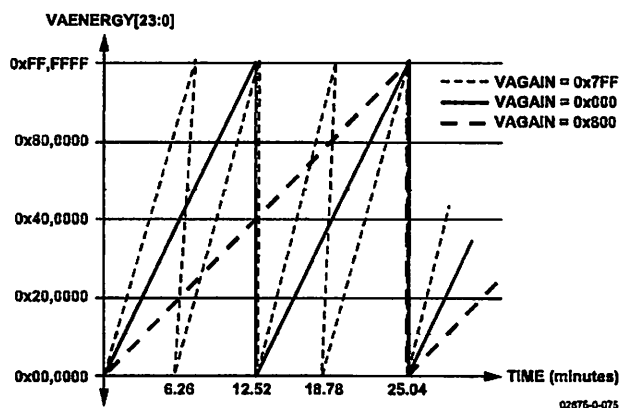


Figure 76. Energy Register Rollover Time for Full-Scale Power (Maximum and Minimum Power Gain)

Note that the apparent energy register is unsigned—see Figure 76. By using the interrupt enable register, the ADE7753 can be configured to issue an interrupt (IRQ) when the apparent energy register is more than half full or when an overflow occurs. The half full interrupt for the unsigned apparent energy register is based on 24 bits as opposed to 23 bits for the signed active energy register.

Integration Times under Steady Load

As mentioned in the last section, the discrete time sample period (T) for the accumulation register is $1.1 \mu\text{s}$ ($4/\text{CLKIN}$). With full-scale sinusoidal signals on the analog inputs and the VAGAIN register set to 0x000, the average word value from apparent power stage is 0xAD055—see the Apparent Power Calculation section. The maximum value that can be stored in the apparent energy register before it overflows is 2^{24} or 0xFF,FFFF. The average word value is added to the internal register, which can store 2^{48} or 0xFFFF,FFFF,FFFF before it

overflows. Therefore, the integration time under these conditions with $VADIV = 0$ is calculated as follows:

$$Time = \frac{0xFFFF, FFFF, FFFF}{0xD055} \times 1.2 \mu s = 888 s = 12.52 \text{ min} (32)$$

When $VADIV$ is set to a value different from 0, the integration time varies, as shown in Equation 33.

$$Time = Time_{WDIV=0} \times VADIV \quad (33)$$

LINE APPARENT ENERGY ACCUMULATION

The ADE7753 is designed with a special apparent energy accumulation mode, which simplifies the calibration process. By using the on-chip zero-crossing detection, the ADE7753 accumulates the apparent power signal in the LVAENERGY register for an integral number of half cycles, as shown in Figure 77. The line apparent energy accumulation mode is always active.

The number of half line cycles is specified in the LINECYC register, which is an unsigned 16-bit register. The ADE7753 can accumulate apparent power for up to 65535 combined half cycles. Because the apparent power is integrated on the same integral number of line cycles as the line active energy register, these two values can be compared easily. The active energy and the apparent energy are calculated more accurately because of this precise timing control and provide all the information needed for reactive power and power factor calculation. At the end of an energy calibration cycle, the CYCEND flag in the interrupt status register is set. If the CYCEND mask bit in the interrupt mask register is enabled, the $\overline{IRQ}$ output also goes active low. Thus the $\overline{IRQ}$ line can also be used to signal the end of a calibration.

The line apparent energy accumulation uses the same signal path as the apparent energy accumulation. The LSB size of these two registers is equivalent.

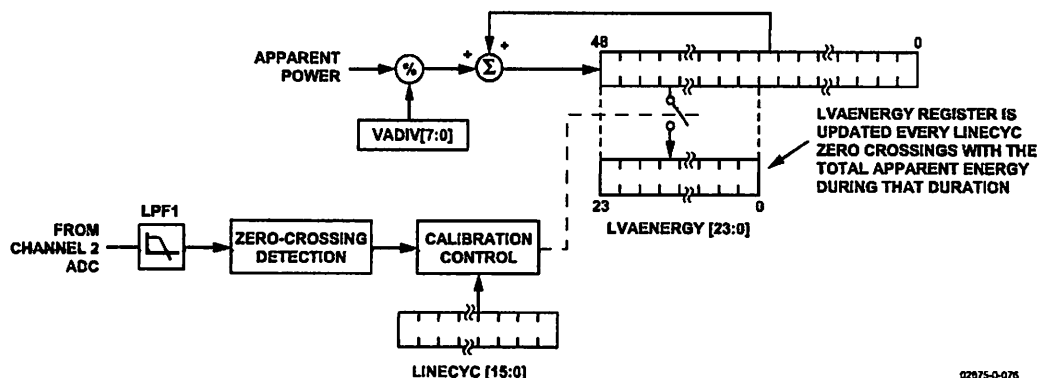


Figure 77. ADE7753 Apparent Energy Calibration

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ENERGIES SCALING

ADE7753 provides measurements of active, reactive, and apparent energies. These measurements do not have the same gain and thus cannot be compared directly to each other.

10. Energies Scaling

	PF = 1	PF = 0.707	PF = 0
Factor On at 50 Hz			
Active	Wh	Wh × 0.707	0
Reactive	0	Wh × 0.508	Wh × 0.719
Apparent	Wh × 0.848	Wh × 0.848	Wh × 0.848
Factor Off at 50 Hz			
Active	Wh	Wh × 0.707	0
Reactive	0	Wh × 0.245	Wh × 0.347
Apparent	Wh × 0.848	Wh × 0.848	Wh × 0.848
Factor On at 60 Hz			
Active	Wh	Wh × 0.707	0
Reactive	0	Wh × 0.610	Wh × 0.863
Apparent	Wh × 0.827	Wh × 0.827	Wh × 0.827
Factor Off at 60 Hz			
Active	Wh	Wh × 0.707	0
Reactive	0	Wh × 0.204	Wh × 0.289
Apparent	Wh × 0.827	Wh × 0.827	Wh × 0.827

CALIBRATING AN ENERGY METER BASED ON THE ADE7753

ADE7753 provides gain and offset compensation for active and apparent energy calibration. Its phase compensation corrects error in active, apparent and reactive energy. If a shunt is used, offset and phase calibration may not be required. A reference meter or an accurate source can be used to calibrate the ADE7753.

When using a reference meter, the ADE7753 calibration output frequency, CF, is adjusted to match the frequency output of the reference meter. A pulse output is only provided for the active energy measurement in the ADE7753. If it is desired to use a reference meter for calibrating the VA and VAR, then additional code would have to be written in a microprocessor to produce a pulsed output for these quantities. Otherwise, VA and VAR calibration require an accurate source.

The ADE7753 provides a line cycle accumulation mode for calibration using an accurate source. In this method, the active energy accumulation rate is adjusted to produce a desired CF frequency. The benefit of using this mode is that the effect of the ripple noise in the active energy is eliminated. Up to 65535 half line cycles can be accumulated, thus providing a stable energy value to average. The accumulation time is calculated from the line cycle period, measured by the ADE7753 in the PERIOD register, and the number of half line cycles in the accumulation, fixed by the LINECYC register.

Current and voltage rms offset calibration removes any apparent energy offset. A gain calibration is also provided for apparent energy. Figure 79 shows an optimized calibration flow for active energy, rms, and apparent energy.

Active and apparent energy gain calibrations can take place concurrently, with a read of the accumulated apparent energy register following that of the accumulated active energy register.

Figure 78 shows the calibration flow for the active energy portion of the ADE7753.



Figure 78. Active Energy Calibration

The ADE7753 does not provide means to calibrate reactive energy gain and offset. The reactive energy portion of the ADE7753 can be calibrated externally, through a MCU.

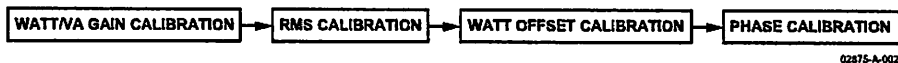


Figure 79. Apparent and Active Energy Calibration

Watt Gain

The first step of calibrating the gain is to define the line voltage, base current and the maximum current for the meter. A meter constant needs to be determined for CF, such as 3200 imp/kWh or 3.2 imp/Wh. Note that the line voltage and the maximum current scale to half of their respective analog input ranges in this example.

The expected CF in Hz is

$$CF_{expected} \text{ (Hz)} = \frac{\text{MeterConstant(imp/Wh)} \times \text{Load(W)}}{3600 \text{ s/h}} \times \cos(\varphi) \quad (34)$$

where φ is the angle between I and V, and $\cos(\varphi)$ is the power factor.

The ratio of active energy LSBs per CF pulse is adjusted using the CFNUM, CFDEN, and WDIV registers.

$$CF_{expected} = \frac{LAENERGY}{\text{AccumulationTime(s)}} \times WDIV \times \frac{(CFNUM + 1)}{(CFDEN + 1)} \quad (35)$$

The relationship between watt-hours accumulated and the quantity read from AENERGY can be determined from the amount of active energy accumulated over time with a given load:

$$\text{Wh/LSB} = \frac{\text{Load(W)} \times \text{Accumulation Time(s)}}{LAENERGY \times 3600 \text{ s/h}} \quad (36)$$

where Accumulation Time can be determined from the value in the line period and the number of half line cycles fixed in the LINECYC register.

$$\text{Accumulation time(s)} = \frac{LINECYC_{IB} \times \text{Line Period(s)}}{2} \quad (37)$$

The line period can be determined from the PERIOD register:

$$\text{Line Period(s)} = \text{PERIOD} \times \frac{8}{CLKIN} \quad (38)$$

The AENERGY Wh/LSB ratio can also be expressed in terms of the meter constant:

$$\text{Wh/LSB} = \frac{\frac{(CFNUM + 1)}{(CFDEN + 1)} \times WDIV}{\text{MeterConstant(imp/Wh)}} \quad (39)$$

In a meter design, WDIV, CFNUM, and CFDEN should be kept constant across all meters to ensure that the Wh/LSB constant is maintained. Leaving WDIV at its default value of 0 ensures maximum resolution. The WDIV register is not included in the CF signal chain so it does not affect the frequency pulse output.

The WGAIN register is used to finely calibrate each meter. Calibrating the WGAIN register changes both CF and AENERGY for a given load condition.

$$AENERGY_{expected} = AENERGY_{nominal} \times \left(1 + \frac{WGAIN}{2^{12}}\right) \quad (40)$$

$$CF_{expected} \text{ (Hz)} = CF_{nominal} \times \frac{(CFNUM + 1)}{(CFDEN + 1)} \times \left(1 + \frac{WGAIN}{2^{12}}\right) \quad (41)$$

When calibrating with a reference meter, WGAIN is adjusted until CF matches the reference meter pulse output. If an accurate source is used to calibrate, WGAIN is modified until the active energy accumulation rate yields the expected CF pulse rate.

The steps of designing and calibrating the active energy portion of a meter with either a reference meter or an accurate source are outlined in the following examples. The specifications for this example are

Meter Constant:	MeterConstant(imp/Wh)
= 3.2	
Base Current:	$I_b = 10 \text{ A}$
Maximum Current:	$I_{MAX} = 60 \text{ A}$
Line Voltage:	$V_{nominal} = 220 \text{ V}$
Line Frequency:	$f_l = 50 \text{ Hz}$

The first step in calibration with either a reference meter or an accurate source is to calculate the CF denominator, CFDEN. This is done by comparing the expected CF pulse output to the nominal CF output with the default CFDEN = 0x3F and CFNUM = 0x3F and when the base current is applied.

The expected CF output for this meter with the base current applied is 1.9556 Hz using Equation 34.

$$CF_{IB(expected)} \text{ (Hz)} = \frac{3.200 \text{ imp/Wh} \times 10 \text{ A} \times 220 \text{ V}}{3600 \text{ s/h}} \times \cos(\varphi) = 1.9556 \text{ Hz}$$

Alternatively, $CF_{expected}$ can be measured from a reference meter pulse output if available.

$$CF_{expected} \text{ (Hz)} = CF_{ref} \quad (42)$$

The maximum CF frequency measured without any frequency division and with ac inputs at full scale is 23 kHz. For this example, the nominal CF with the test current, I_b , applied is 958 Hz. In this example the line voltage and maximum current scale half of their respective analog input ranges. The line voltage and maximum current should not be fixed at the maximum analog inputs to account for occurrences such as spikes on the line.

$$CF_{nominal} \text{ (Hz)} = 23 \text{ kHz} \times \frac{1}{2} \times \frac{1}{2} \times \frac{I}{I_{MAX}} \quad (43)$$

$$CF_{IB(nominal)} \text{ (Hz)} = 23 \text{ kHz} \times \frac{1}{2} \times \frac{1}{2} \times \frac{10}{60} = 958 \text{ Hz}$$

The nominal CF on a sample set of meters should be measured using the default CFDEN, CFNUM, and WDIV to ensure that the best CFDEN is chosen for the design.

With the CFNUM register set to 0, CFDEN is calculated to be 489 for the example meter:

$$CFDEN = INT\left(\frac{CF_{IB(nominal)}}{CF_{IB(expected)}}\right) - 1 \quad (44)$$

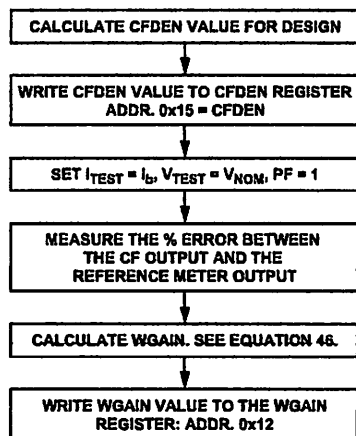
$$CFDEN = INT\left(\frac{958}{1.9556}\right) - 1 = (490 - 1) = 489$$

value for CFDEN should be loaded into each meter before calibration. The WGAIN and WDIV registers can then be used to calibrate the CF output. The following sections explain how to calibrate a meter based on ADE7753 when using a reference meter or an accurate source.

Rating Watt Gain Using a Reference Meter Example

CFDEN and CFNUM values for the design should be written to their respective registers before beginning the calibration steps shown in Figure 80. When using a reference meter, the %ERROR in CF is measured by comparing the CF output of the ADE7753 meter with the pulse output of the reference meter with the same test conditions applied to both meters. Equation 45 defines the percent error with respect to the pulse outputs of both meters (using the base current, I_b):

$$\%ERROR_{CF(IB)} = \frac{CF_{IB} - CF_{ref(IB)}}{CF_{ref(IB)}} \times 100 \quad (45)$$



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Figure 80. Calibrating Watt Gain Using a Reference Meter

For this example:

Meter Constant: $MeterConstant(imp/Wh)$
= 3.2

CF Numerator: $CFNUM = 0$

CF Denominator: $CFDEN = 489$

% Error measured at Base Current:

$$\%ERROR_{CF(IB)} = -3.07\%$$

One LSB change in $WGAIN$ changes the active energy registers and CF by 0.0244%. $WGAIN$ is a signed two's complement register and can correct for up to a 50% error. Assuming a -3.07% error, $WGAIN$ is 126:

$$WGAIN = INT\left(-\frac{\%ERROR_{CF(IB)}}{0.0244\%}\right) \quad (46)$$

$$WGAIN = INT\left(-\frac{-3.07\%}{0.0244\%}\right) = 126$$

When CF is calibrated, the AENERGY register has the same Wh/LSB constant from meter to meter if the meter constant, WDIV, and the CFNUM/CFDEN ratio remain the same. The Wh/LSB ratio for this meter is 6.378×10^{-4} using Equation 39 with WDIV at the default value.

$$\frac{Wh}{LSB} = \frac{\frac{(CFNUM + 1)}{(CFDEN + 1)} \times WDIV}{MeterConstant(imp/Wh)}$$

$$\frac{Wh}{LSB} = \frac{1}{\frac{(490 + 1)}{3.200 \text{ imp/Wh}}} = \frac{1}{490 \times 3.2} = 6.378 \times 10^{-4}$$

Calibrating Watt Gain Using an Accurate Source Example

The CFDEN value calculated using Equation 44 should be written to the CFDEN register before beginning calibration and zero should be written to the CFNUM register. First, the line accumulation mode and the line accumulation interrupt should be enabled. Next, the number of half line cycles for the energy accumulation is written to the LINECYC register. This sets the accumulation time. Reset the interrupt status register and wait for the line cycle accumulation interrupt. The first line cycle accumulation results may not have used the accumulation time set by the LINECYC register and should be discarded. After resetting the interrupt status register, the following line cycle readings will be valid. When LINECYC half line cycles have elapsed, the $\overline{IRQ}$ pin goes active low and the nominal LAENERGY with the test current applied can be read. This LAENERGY value is compared to the expected LAENERGY value to determine the WGAIN value. If apparent energy gain calibration is performed at the same time, LVAENERGY can be read directly after LAENERGY. Both registers should be read before the next interrupt is issued on the $\overline{IRQ}$ pin. Refer to the Apparent Energy Calculation section for more details. Figure 81 details the steps that calibrate the watt gain using an accurate source.

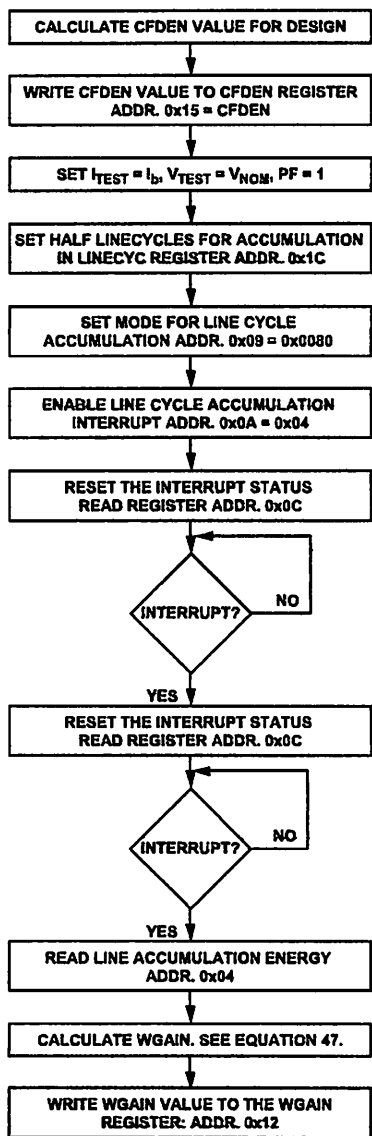


Figure 81. Calibrating Watt Gain Using an Accurate Source

Equation 47 describes the relationship between the expected LAENERGY value and the LAENERGY measured in the test condition:

$$WGAIN = INT \left(\left(\frac{LAENERGY_{IB(expected)}}{LAENERGY_{IB(nominal)}} - 1 \right) \times 2^{12} \right) \quad (47)$$

The nominal LAENERGY reading, $LAENERGY_{IB(nominal)}$, is the LAENERGY reading with the test current applied. The expected LAENERGY reading is calculated from the following equation:

$$LAENERGY_{IB(expected)} = INT \left(\frac{CF_{IB(expected)} \times Accumulation\ Time(s)}{\frac{CFNUM + 1}{CFDEN + 1} \times WDIV} \right) \quad (48)$$

where $CF_{IB(expected)}$ (Hz) is calculated from Equation 34, accumulation time is calculated from Equation 37, and the line period is determined from the PERIOD register according to Equation 38.

For this example:

Meter Constant:	MeterConstant(imp/Wh)
= 3.2	
Test Current:	$I_b = 10\ A$
Line Voltage:	$V_{nominal} = 220\ V$
Line Frequency:	$f_l = 50\ Hz$
Half Line Cycles:	$LINECYC_{IB} = 2000$
CF Numerator:	$CFNUM = 0$
CF Denominator:	$CFDEN = 489$
Energy Reading at Base Current:	

$$LAENERGY_{IB(nominal)} = 17174$$

$$\text{Period Register Reading: } PERIOD = 8959$$

$$\text{Clock Frequency: } CLKIN = 3.579545\ MHz$$

$CF_{expected}$ is calculated to be 1.9556 Hz according to Equation 34. $LAENERGY_{expected}$ is calculated to be 19186 using Equation 48.

$$CF_{IB(expected)}(Hz) = \frac{3.200\ imp/Wh \times 220\ V \times 10\ A}{3600\ s/h} \times (\cos(\phi) = 1.9556\ Hz)$$

$$LAENERGY_{IB(expected)} = INT \left(\frac{CF_{IB(expected)} \times LINECYC_{IB} / 2 \times PERIOD \times 8 / CLKIN}{\frac{CFNUM + 1}{CFDEN + 1} \times WDIV} \right)$$

$$LAENERGY_{IB(expected)} = INT \left(\frac{1.9556 \times 2000 / 2 \times 8959 \times 8 / (3.579545 \times 10^6)}{\frac{1}{489 + 1}} \right) = 19186.4$$

$$INT(19186.4) = 19186$$

WGAIN is calculated to be 480 using Equation 47.

$$WGAIN = INT \left(\left(\frac{19186}{17174} - 1 \right) \times 2^{12} \right) = 480$$

Note that WGAIN is a signed twos complement register.

With WDIV and CFNUM set to 0, LAENERGY can be expressed as

$$ENERGY_{IB(expected)} = CF_{M(expected)} \times LINECYC_{IB} / 2 \times PERIOD \times 8 / CLKIN \times (CFDEN + 1)$$

calculated Wh/LSB ratio for the active energy register, Equation 39 is 6.378×10^{-4} :

$$Wh/LSB = \frac{1}{\frac{(489+1)}{3.200 \text{ imp/Wh}}} = 6.378 \times 10^{-4}$$

Offset

calibration allows outstanding performance over a wide range, for example, 1000:1. To do this calibration two measurements are needed at unity power factor, one at I_b and one at the lowest current to be corrected. Either line cycle accumulation measurements or frequency measurements are used to determine the energy offset. Gain calibration should be performed prior to offset calibration.

Offset calibration is performed by determining the active energy error rate. Once the active energy error rate has been determined, the value to write to the APOS register to correct offset is calculated.

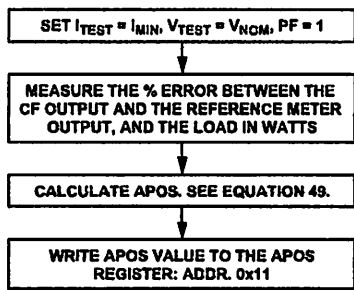
$$APOS = - \frac{AENERGY \text{ Error Rate} \times 2^{35}}{CLKIN} \quad (49)$$

ENERGY registers update at a rate of $CLKIN/4$. The two complement APOS register provides a fine adjustment to the power calculation. It represents a fixed amount of power to be adjusted every $CLKIN/4$. The 8 LSBs of the APOS register are fractional such that one LSB of APOS represents one-eighth of the least significant bit of the internal active energy register. Therefore, one LSB of the APOS register represents 2^{-33} AENERGY[23:0] active energy register.

Steps involved in determining the active energy error rate through line accumulation and reference meter calibration are shown in the following sections.

Calibrating Watt Offset Using a Reference Meter Example

Figure 82 shows the steps involved in calibrating watt offset using a reference meter.



02875-A-000

Figure 82. Calibrating Watt Offset Using a Reference Meter

Example:

Constant:

$$MeterConstant(\text{imp/Wh}) = 3.2$$

Minimum Current:

$$I_{MIN} = 40 \text{ mA}$$

Load at Minimum Current:

$$W_{MIN} = 9.6 \text{ W}$$

CF Error at Minimum Current:

$$\%ERROR_{CF(I_{MIN})} = 1.3\%$$

CF Numerator:

$$CFNUM = 0$$

CF Denominator:

$$CFDEN = 489$$

Clock Frequency:

$$CLKIN = 3.579545 \text{ MHz}$$

Using Equation 49, APOS is calculated to be -522 for this example.

$$CF \text{ Absolute Error} = CF_{I_{MIN}(nominal)} - CF_{I_{MIN}(expected)} \quad (50)$$

$$CF \text{ Absolute Error} =$$

$$(\%ERROR_{CF(I_{MIN})}) \times W_{MIN} \times \frac{MeterConstant(\text{imp/Wh})}{3600} \quad (51)$$

$$CF \text{ Absolute Error} =$$

$$\left(\frac{1.3\%}{100} \right) \times 9.6 \times \frac{3.200}{3600} = 0.000110933 \text{ Hz}$$

Then,

$$AENERGY \text{ Error Rate (LSB/s)} =$$

$$CF \text{ Absolute Error} \times \frac{CFDEN + 1}{CFNUM + 1} \quad (52)$$

$$AENERGY \text{ Error Rate (LSB/s)} =$$

$$0.000110933 \times \frac{490}{1} = 0.05436$$

Using Equation 49, APOS is -522.

$$APOS = - \frac{0.05436 \times 2^{35}}{3.579545 \times 10^6} = -522$$

APOS can be represented as follows with CFNUM and WDIV set at 0:

$$APOS = - \frac{(\%ERROR_{CF(I_{MIN})}) \times W_{MIN} \times \frac{MeterConstant(\text{imp/Wh})}{3600} \times (CFDEN + 1) \times 2^{35}}{CLKIN}$$

Calibrating Watt Offset with an Accurate Source Example

Figure 83 is the flowchart for watt offset calibration with an accurate source.

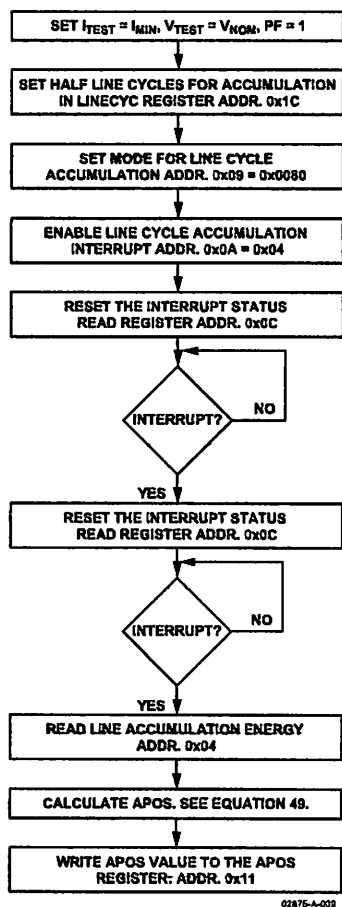


Figure 83. Calibrating Watt Offset with an Accurate Source

For this example:

Meter Constant: $MeterConstant(imp/Wh)$
 3.2
 Line Voltage: $V_{nominal} = 220\text{ V}$
 Line Frequency: $f_l = 50\text{ Hz}$
 CF Numerator: $CFNUM = 0$
 CF Denominator: $CFDEN = 489$
 Base Current: $I_b = 10\text{ A}$
 Half Line Cycles Used at Base Current:

$$LINECYC_{(I_b)} = 2000$$

Period Register Reading: $PERIOD = 8959$

Clock Frequency: $CLKIN = 3.579545\text{ MHz}$

Expected LAENERGY Register Value at Base Current
from the Watt Gain section): $LAENERGY_{IB(expected)} = 19186$

Minimum Current: $I_{MIN} = 40\text{ mA}$

Number of Half Line Cycles used at Minimum Current:
 $LINECYC_{(I_{MIN})} =$

700

Active energy Reading at Minimum Current:

$$LAENERGY_{IMIN(nominal)} = 1395$$

The $LAENERGY_{expected}$ at I_{MIN} is 1370 using Equation 53.

$$LAENERGY_{IMIN(expected)} =$$

$$INT \left(\frac{I_{MIN}}{I_b} \times LAENERGY_{IB(expected)} \times \frac{LINECYC_{I_{MIN}}}{LINECYC_{I_b}} \right) \quad (53)$$

$$LAENERGY_{IMIN(expected)} =$$

$$INT \left(\frac{0.04}{10} \times 19186 \times \frac{35700}{2000} \right) = INT(1369.80) = 1370$$

where:

$LAENERGY_{IB(expected)}$ is the expected LAENERGY reading at I_b from the watt gain calibration.

$LINECYC_{I_{MIN}}$ is the number of half line cycles that energy is accumulated over when measuring at I_{MIN} .

More line cycles could be required at the minimum current to minimize the effect of quantization error on the offset calibration. For example, if a test current of 40 mA results in an active energy accumulation of 113 after 2000 half line cycles, one LSB variation in this reading represents an 0.8% error. This measurement does not provide enough resolution to calibrate out a <1% offset error. However, if the active energy is accumulated over 37,500 half line cycles, one LSB variation results in 0.05% error, reducing the quantization error.

APOS is -672 using Equations 55 and 49.

$$LAENERGY \text{ Absolute Error} =$$

$$LAENERGY_{IMIN(nominal)} - LAENERGY_{IMIN(expected)}$$

$$LAENERGY \text{ Absolute Error} = 1395 - 1370 = 25 \quad (54)$$

$$AENERGY \text{ Error Rate (LSB/s)} =$$

$$\frac{LAENERGY \text{ Absolute Error}}{LINECYC / 2} \times \frac{CLKIN}{8 \times PERIOD} \quad (55)$$

$$AENERGY \text{ Error Rate (LSB/s)} =$$

$$\frac{25}{35700 / 2} \times \frac{3.579545 \times 10^6}{8 \times 8959} = 0.069948771$$

$$APOS = - \frac{AENERGY \text{ Error Rate} \times 2^{35}}{CLKIN}$$

$$APOS = - \frac{0.069948771 \times 2^{35}}{3.579545 \times 10^6} = -672$$

Phase Calibration

The PHCAL register is provided to remove small phase errors. The AD7753 compensates for phase error by inserting a small delay or advance on the voltage channel input. Phase leads up to 1.84° and phase lags up to 0.72° at 50 Hz can be corrected. The error is determined by measuring the active energy at I_B for two power factors, PF = 1 and PF = 0.5 inductive.

CTs may introduce large phase errors that are beyond the range of the phase calibration register. In this case, coarse phase compensation has to be done externally with an analog filter.

Phase error can be obtained from either CF or LAENERGY measurements:

$$\text{Error} = \frac{LAENERGY_{IB, PF=0.5} - LAENERGY_{IB(expected)} / 2}{LAENERGY_{IB(expected)} / 2} \quad (56)$$

After gain and offset calibration have been performed, there should be 0% error in CF at unity power factor and then:

$$\text{Error} = \%ERROR_{CF(IB, PF=0.5)} / 100 \quad (57)$$

Phase error is

$$\text{Phase Error (°)} = -\text{Arcsin}\left(\frac{\text{Error}}{\sqrt{3}}\right) \quad (58)$$

The relationship between phase error and the PHCAL phase calibration register is

$$\text{PHCAL} = \text{INT}\left(\text{Phase Error (°)} \times \frac{\text{PERIOD}}{360^\circ}\right) + 0x0D \quad (59)$$

The expression for PHCAL can be simplified using the approximation that at small x:

$$\text{arcsin}(x) \approx x$$

The delay introduced in the voltage channel by PHCAL is

$$\text{Delay} = (\text{PHCAL} - 0x0D) \times 8 / \text{CLKIN} \quad (60)$$

The delay associated with the PHCAL register is a time delay if $(\text{PHCAL} - 0x0D)$ is positive but represents a time advance if the quantity is negative. There is no time delay if PHCAL = 0x0D.

Phase correction is in the opposite direction of the phase error.

$$\text{Phase Correction (°)} = -(\text{PHCAL} - 0x0D) \times \frac{360^\circ}{\text{PERIOD}} \quad (61)$$

Calibrating Phase Using a Reference Meter Example

A power factor of 0.5 inductive can be assumed if the pulse rate of the reference meter is half of its PF = 1 rate. Then the %ERROR between CF and the pulse output of the reference meter can be used to perform the preceding calculations.

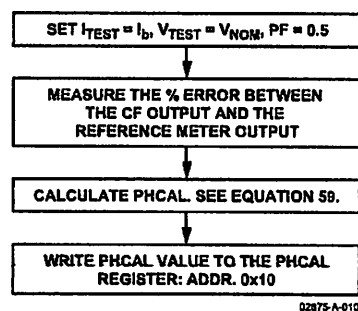


Figure 84. Calibrating Phase Using a Reference Meter

For this example:

CF % Error at PF = .5 Inductive: $\%ERROR_{CF(IB, PF=0.5)} = 0.215\%$

PERIOD Register Reading: $PERIOD = 8959$

Then PHCAL is 11 using Equations 57 through 59:

$$\text{Error} = 0.215\% / 100 = 0.00215$$

$$\text{Phase Error (°)} = -\text{Arcsin}\left(\frac{0.00215}{\sqrt{3}}\right) = -0.07^\circ$$

$$\text{PHCAL} = \text{INT}\left(-0.07^\circ \times \frac{8959}{360^\circ}\right) + 0x0D = -2 + 13 = 11$$

PHCAL can be expressed as follows:

$$\text{PHCAL} = \text{INT}\left(-\text{Arcsin}\left(\frac{\text{Error}}{\sqrt{3}}\right) \times \frac{\text{PERIOD}}{2\pi}\right) + 0x0D \quad (62)$$

Note that PHCAL is a signed two's complement register.

Setting the PHCAL register to 11 provides a phase correction of 0.08° to correct the phase lead:

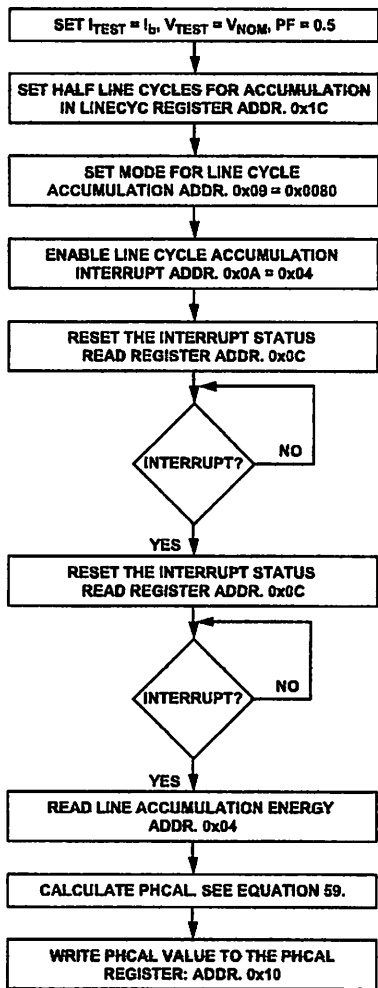
$$\text{Phase Correction (°)} = -(\text{PHCAL} - 0x0D) \times \frac{360^\circ}{\text{PERIOD}}$$

$$\text{Phase Correction (°)} = -(11 - 0x0D) \times \frac{360^\circ}{8960} = 0.08^\circ$$

LAENERGY_{IB, PF}

Calibrating Phase with an Accurate Source Example

With an accurate source, line cycle accumulation is a good method of calibrating phase error. The value of LAENERGY must be obtained at two power factors, PF = 1 and PF = 0.5 inductive.



02875-A-011

Figure 85. Calibrating Phase with an Accurate Source

or this example:

Meter Constant:	MeterConstant(imp/Wh)
3.2	
Line Voltage:	V _{nominal} = 220 V
Line Frequency:	f _i = 50 Hz
CF Numerator:	CFNUM = 0
CF Denominator:	CFDEN = 489
Base Current:	I _b = 10 A
Half Line Cycles Used at Base Current:	LINECYC _{IB} = 2000
PERIOD Register:	PERIOD = 8959
Expected Line Accumulation at Unity Power Factor (from Watt	LAENERGY _{IB(expected)} =
in Section:	
186	
Active Energy Reading at PF = .5 inductive:	

$\text{PF} = 0.5 = 9613$

The error using Equation 56 is

$$\text{Error} = \frac{9613 - 19186/2}{19186/2} = 0.0021$$

$$\text{Phase Error (}^\circ\text{)} = -\text{Arcsin}\left(\frac{0.0021}{\sqrt{3}}\right) = -0.07^\circ$$

Using Equation 59, PHCAL is calculated to be 11.

$$\text{PHCAL} = \text{INT}\left(-0.07^\circ \times \frac{8959}{360^\circ}\right) + 0x0D = -2 + 13 = 11$$

Note that PHCAL is a signed two's complement register.

The phase lead is corrected by 0.08° when the PHCAL register is set to 11:

$$\text{Phase Correction (}^\circ\text{)} = -(\text{PHCAL} - 0x0D) \times \frac{360^\circ}{\text{PERIOD}}$$

$$\text{Phase Correction (}^\circ\text{)} = -(11 - 0x0D) \times \frac{360^\circ}{8960} = 0.08^\circ$$

VRMS and IRMS Calibration

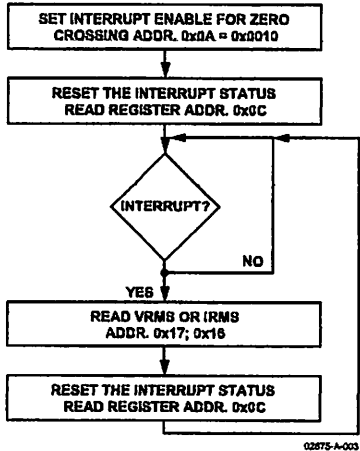
VRMS and IRMS are calculated by squaring the input in a digital multiplier.

$$v^2(t) = \sqrt{2} V \sin(\omega t) \times \sqrt{2} V \sin(\omega t) = V^2 - V^2 \times \cos(2\omega t) \quad (63)$$

The square of the rms value is extracted from $v^2(t)$ by a low-pass filter. The square root of the output of this low-pass filter gives the rms value. An offset correction is provided to cancel noise and offset contributions from the input.

There is ripple noise from the 2ω term because the low-pass filter does not completely attenuate the signal. This noise can be minimized by synchronizing the rms register readings with the zero crossing of the voltage signal. The IRQ output can be configured to indicate the zero crossing of the voltage signal.

This flowchart demonstrates how VRMS and IRMS readings are synchronized to the zero crossings of the voltage input.



02875-A-003

Figure 86. Synchronizing VRMS and IRMS Readings with Zero Crossings

Calibrating Phase with an Accurate Source Example

With an accurate source, line cycle accumulation is a good method of calibrating phase error. The value of LAENERGY must be obtained at two power factors, PF = 1 and PF = 0.5 inductive.

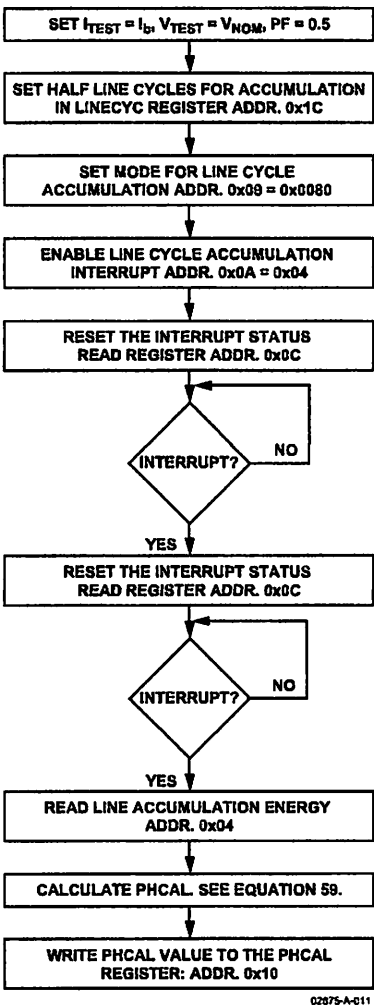


Figure 85. Calibrating Phase with an Accurate Source

For this example:

Meter Constant:	$MeterConstant(imp/Wh)$
Line Voltage:	$V_{nominal} = 220\text{ V}$
Line Frequency:	$f_l = 50\text{ Hz}$
CF Numerator:	$CFNUM = 0$
CF Denominator:	$CFDEN = 489$
Base Current:	$I_b = 10\text{ A}$
Half Line Cycles Used at Base Current:	$LINECYC_{IB} = 2000$
PERIOD Register:	$PERIOD = 8959$
Expected Line Accumulation at Unity Power Factor (from Watt	$LAENERGY_{IB(expected)} =$
in Section:	
186	
Active Energy Reading at PF = .5 inductive:	

$= .5 = 9613$

The error using Equation 56 is

$$Error = \frac{9613 - 19186/2}{19186/2} = 0.0021$$

$$Phase\ Error\ (^{\circ}) = -\text{Arcsin}\left(\frac{0.0021}{\sqrt{3}}\right) = -0.07^{\circ}$$

Using Equation 59, PHCAL is calculated to be 11.

$$PHCAL = INT\left(-0.07^{\circ} \times \frac{8959}{360^{\circ}}\right) + 0x0D = -2 + 13 = 11$$

Note that PHCAL is a signed two's complement register.

The phase lead is corrected by 0.08° when the PHCAL register is set to 11:

$$Phase\ Correction\ (^{\circ}) = -(PHCAL - 0x0D) \times \frac{360^{\circ}}{PERIOD}$$

$$Phase\ Correction\ (^{\circ}) = -(11 - 0x0D) \times \frac{360^{\circ}}{8960} = 0.08^{\circ}$$

VRMS and IRMS Calibration

VRMS and IRMS are calculated by squaring the input in a digital multiplier.

$$v^2(t) = \sqrt{2}\text{ V sin}(\omega t) \times \sqrt{2}\text{ V sin}(\omega t) = V^2 - V^2 \times \cos(2\omega t) \quad (63)$$

The square of the rms value is extracted from $v^2(t)$ by a low-pass filter. The square root of the output of this low-pass filter gives the rms value. An offset correction is provided to cancel noise and offset contributions from the input.

There is ripple noise from the 2ω term because the low-pass filter does not completely attenuate the signal. This noise can be minimized by synchronizing the rms register readings with the zero crossing of the voltage signal. The IRQ output can be configured to indicate the zero crossing of the voltage signal.

This flowchart demonstrates how VRMS and IRMS readings are synchronized to the zero crossings of the voltage input.

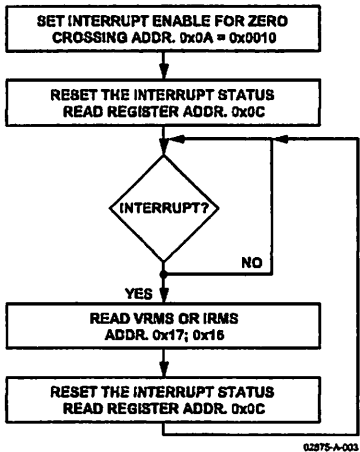


Figure 86. Synchronizing VRMS and IRMS Readings with Zero Crossings

rms compensation is done after the LPF3 filter (see 56).

$$RMS = VRMS0 + VRMSOS \tag{64}$$

0 is the rms measurement without offset correction. is linear from full-scale to full-scale/20.

ibrate the offset, two VRMS measurements are required, ample, at $V_{nominal}$ and $V_{nominal}/10$. $V_{nominal}$ is set at half of the ale analog input range so the smallest linear VRMS g is at $V_{nominal}/10$.

$$VRMSOS = \frac{V_1 \times VRMS_2 - V_2 \times VRMS_1}{V_2 - V_1} \tag{65}$$

$VRMS_1$ and $VRMS_2$ are rms register values without offset tion for input V_1 and V_2 , respectively.

range of the 12-bit, twos complement VRMSOS register is ough, the voltage channel offset register, CH2OS, can be to correct the VRMS offset.

nt rms compensation is performed before the square root:

$$RMS^2 = IRMS0^2 + 32768 \times IRMSOS \tag{66}$$

e $IRMS0$ is the rms measurement without offset correction. urrent rms calculation is linear from full-scale to full- 100.

ibrate this offset, two IRMS measurements are required, ample, at I_b and $I_{MAX}/50$. I_{MAX} is set at half of the full-scale ; input range so the smallest linear IRMS reading is at 0.

$$IRMSOS = \frac{1}{32768} \times \frac{I_1^2 \times IRMS_2^2 - I_2^2 \times IRMS_1^2}{I_2^2 - I_1^2} \tag{67}$$

$IRMS_1$ and $IRMS_2$ are rms register values without offset tion for input I_1 and I_2 , respectively.

Apparent Energy

Apparent energy gain calibration is provided for both meter-to-meter gain adjustment and for setting the VAh/LSB constant.

$$VAENERGY = VAENERGY_{initial} \times \frac{1}{VADIV} \times \left(1 + \frac{VAGAIN}{2^{12}}\right) \tag{68}$$

VADIV is similar to the CFDEN for the watt hour calibration. It should be the same across all meters and determines the VAh/LSB constant. VAGAIN is used to calibrate individual meters.

Apparent energy gain calibration should be performed before rms offset correction to make most efficient use of the current test points. Apparent energy gain and watt gain compensation require testing at I_b while rms and watt offset correction require a lower test current. Apparent energy gain calibration can be done at the same time as the watt-hour gain calibration using line cycle accumulation. In this case, LAENERGY and LVAENERGY, the line cycle accumulation apparent energy register, are both read following the line cycle accumulation interrupt. Figure 87 shows a flowchart for calibrating active and apparent energy simultaneously.

$$VAGAIN = INT \left(\left(\frac{LVAENERGY_{IB(expected)}}{LVAENERGY_{IB(nominal)}} - 1 \right) \times 2^{12} \right) \tag{69}$$

$$LVAENERGY_{IB(expected)} = INT \left(\frac{V_{nominal} \times I_B}{\frac{VAh}{LSB} constant \times 3600s/h} \times Accumulation\ time(s) \right) \tag{70}$$

The accumulation time is determined from Equation 37 and the line period can be determined from the PERIOD register according to Equation 38. The VAh represented by the VAENERGY register is

$$VAh = VAENERGY \times VAh/LSB\ constant \tag{71}$$

The VAh/LSB constant can be verified using this equation:

$$VAh/LSB\ constant = \frac{VA \times Accumulation\ time(s) / 3600}{LVAENERGY} \tag{72}$$

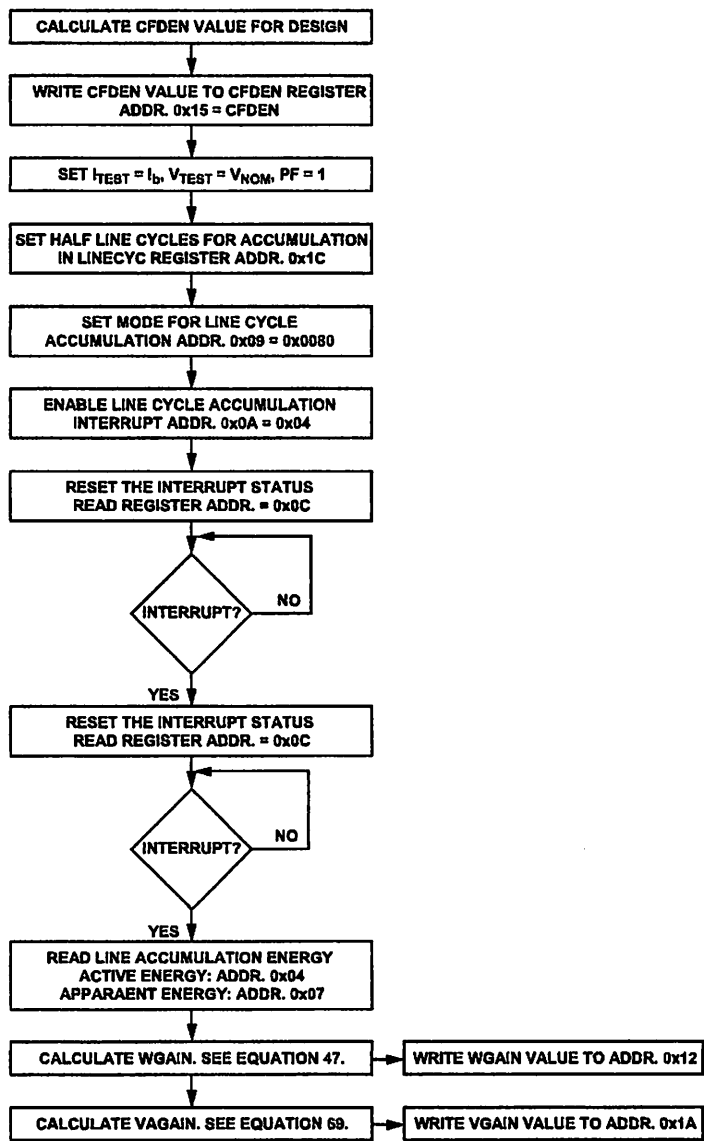


Figure 87. Active/Apparent Gain Calibration

Reactive Energy

Reactive energy is only available in line accumulation mode in the ADE7753. The accumulated reactive energy over LINECYC number of half line cycles is stored in the LVARENERGY register.

In the ADE7753, a low-pass filter at 2 Hz on the current channel is implemented for the reactive power calculation. This provides the 90 degree phase shift needed to calculate the reactive power. This filter introduces 1/f attenuation in the reactive energy accumulated. Compensation for this attenuation can be done externally in a microcontroller. The microcontroller can use the LVARENERGY register in order to produce a pulse output similar to the CF pulse for reactive energy.

To create a VAR pulse, an impulse/VARh constant must be determined. The 1/f attenuation correction factor is determined

by comparing the nominal reactive energy accumulation rate to the expected value. The attenuation correction factor is multiplied by the contents of the LVARENERGY register, with the ADE7753 in line accumulation mode.

mpulse/LSB ratio used to convert the value in the ENERGY register into a pulse output can be expressed in terms of impulses/VARh and VARh/LSB.

$$imp/LSB = imp / VARh \times VARh / LSB = \frac{VARCF_{IB(expected)}}{VARCF_{nominal}} \quad (73)$$

$$\frac{VARCF_{IB(expected)}}{VARCF_{nominal}} = \frac{1}{ARConstant(imp / VARh) \times V_{nominal} \times I_b} \times \sin(\varphi) \quad (74)$$

$$VARCF_{IB(nominal)} = \frac{LVARENERGY_{IB} \times PERIOD_{50\text{ Hz}}}{Accumulation\ time(s) \times PERIOD} \quad (75)$$

the accumulation time is calculated from Equation 37. The period can be determined from the PERIOD register using Equation 38. Then VAR can be determined from the ARENERGY register value:

$$VARh = \frac{LVARENERGY_{IB} \times VARh / LSB \times PERIOD_{50\text{ Hz}}}{PERIOD} \quad (76)$$

$$VAR = \frac{LVARENERGY_{IB} \times VARh / LSB \times 3600s/h \times PERIOD_{50\text{ Hz}}}{Accumulation\ time(s) \times PERIOD} \quad (77)$$

PERIOD_{50 Hz}/PERIOD factor in the preceding VAR equations is a correction factor for the 1/f frequency attenuation of the pass filter. The PERIOD_{50 Hz} term refers to the line period at 50 Hz and could represent a frequency other than 50 Hz.

MINIMUM FREQUENCY

On the data sheet, the characteristics of the ADE7753 are shown for a CLKIN frequency of 3.579545 MHz. However, the ADE7753 is designed to have the same accuracy at any CLKIN frequency within the specified range. If the CLKIN frequency is different from 3.579545 MHz, various timing and filter characteristics need to be redefined with the new CLKIN frequency. For example, the timing of digital filters such as LPF1, LPF2, or LPF3 shifts in proportion to the change in CLKIN frequency according to the following equation:

$$New\ Frequency = Original\ Frequency \times \frac{CLKIN\ Frequency}{3.579545\ MHz} \quad (78)$$

A change of CLKIN frequency does not affect the timing characteristics of the serial interface because the data transfer is synchronized with the serial clock signal (SCLK). But one needs to adjust the read/write timing of the serial data transfer—see the ADE7753 timing characteristics in Table 2. Table 11 lists the timing changes that are affected by CLKIN frequency.

Table 11. Frequency Dependencies of the ADE7753

Parameters	
Parameter	CLKIN Dependency
Nyquist Frequency for CH 1 and CH 2 ADCs	CLKIN/8
PHCAL Resolution (Seconds per LSB)	4/CLKIN
Active Energy Register Update Rate (Hz)	CLKIN/4
Waveform Sampling Rate (per Second)	
WAVSEL 1,0 = 0 0	CLKIN/128
0 1	CLKIN/256
1 0	CLKIN/512
1 1	CLKIN/1024
Maximum ZXTOUT Period	524,288/CLKIN

SUSPENDING ADE7753 FUNCTIONALITY

The analog and the digital circuit can be suspended separately. The analog portion of the ADE7753 can be suspended by setting the ASUSPEND bit (Bit 4) of the mode register to logic high—see the Mode Register (0x9) section. In suspend mode, all waveform samples from the ADCs are set to 0. The digital circuitry can be halted by stopping the CLKIN input and maintaining a logic high or low on the CLKIN pin. The ADE7753 can be reactivated by restoring the CLKIN input and setting the ASUSPEND bit to logic low.

CHECKSUM REGISTER

The ADE7753 has a checksum register (CHECKSUM[5:0]) to ensure the data bits received in the last serial read operation are not corrupted. The 6-bit checksum register is reset before the first bit (MSB of the register to be read) is put on the DOUT pin. During a serial read operation, when each data bit becomes available on the rising edge of SCLK, the bit is added to the checksum register. In the end of the serial read operation, the content of the checksum register is equal to the sum of all ones in the register previously read. Using the checksum register, the user can determine if an error has occurred during the last read operation. Note that a read to the checksum register also generates a checksum of the checksum register itself.

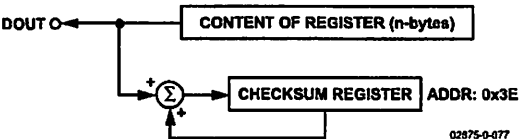


Figure 88. Checksum Register for Serial Interface Read

ADE7753 SERIAL INTERFACE

All ADE7753 functionality is accessible via several on-chip registers—see Figure 89. The contents of these registers can be updated or read using the on-chip serial interface. After power-up or toggling the RESET pin low or a falling edge on CS, the ADE7753 is placed in communications mode. In communications mode, the ADE7753 expects a write to its communications register. The data written to the communications register determines whether the next data transfer operation is a read or a write and also which register is accessed. Therefore all data transfer operations with the ADE7753, whether a read or a write, must begin with a write to the communications register.

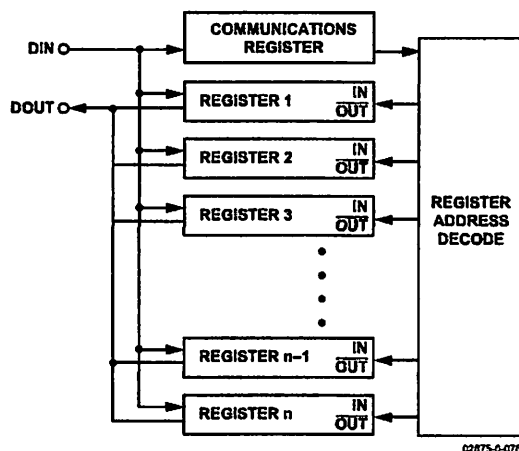


Figure 89. Addressing ADE7753 Registers via the Communications Register

The communications register is an 8-bit wide register. The MSB determines whether the next data transfer operation is a read or write. The six LSBs contain the address of the register to be accessed—see the Communications Register section for a more detailed description.

Figure 90 and Figure 91 show the data transfer sequences for a read and write operation, respectively. On completion of a data transfer (read or write), the ADE7753 once again enters communications mode. A data transfer is complete when the LSB of the ADE7753 register being addressed (for a write or a read) is transferred to or from the ADE7753.

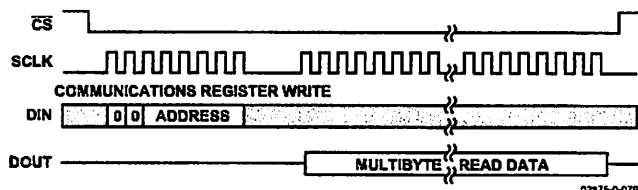


Figure 90. Reading Data from the ADE7753 via the Serial Interface

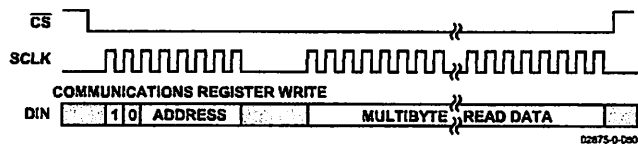


Figure 91. Writing Data to the ADE7753 via the Serial Interface

The serial interface of the ADE7753 is made up of four signals: SCLK, DIN, DOUT, and CS. The serial clock for a data transfer is applied at the SCLK logic input. This logic input has a Schmitt-trigger input structure that allows slow rising (and falling) clock edges to be used. All data transfer operations are synchronized to the serial clock. Data is shifted into the ADE7753 at the DIN logic input on the falling edge of SCLK. Data is shifted out of the ADE7753 at the DOUT logic output on a rising edge of SCLK. The CS logic input is the chip-select input. This input is used when multiple devices share the serial bus. A falling edge on CS also resets the serial interface and places the ADE7753 into communications mode. The CS input should be driven low for the entire data transfer operation. Bringing CS high during a data transfer operation aborts the transfer and places the serial bus in a high impedance state. The CS logic input can be tied low if the ADE7753 is the only device on the serial bus. However, with CS tied low, all initiated data transfer operations must be fully completed, i.e., the LSB of each register must be transferred because there is no other way of bringing the ADE7753 back into communications mode without resetting the entire device by using RESET.

753 Serial Write Operation

rial write sequence takes place as follows. With the 753 in communications mode (i.e., the $\overline{CS}$ input logic), write to the communications register first takes place. The MSB of this byte transfer is a 1, indicating that the data operation is a write. The LSBs of this byte contain the address of the register to be written to. The ADE7753 starts shifting in the register data on the next falling edge of SCLK. All remaining bits of register data are shifted in on the falling edge of subsequent SCLK pulses—see Figure 92. As explained earlier, a write is initiated by a write to the communications register, followed by the data. During a data write operation to the ADE7753, data is transferred to all on-chip registers one bit at a time. After a byte is transferred into the serial port, it takes a finite time before it is transferred to one of the ADE7753 on-chip registers. Although another byte transfer to the serial port can start while the previous byte is being transferred to an on-chip register, this second byte transfer

should not finish until at least 4 μs after the end of the previous byte transfer. This functionality is expressed in the timing specification t_6 —see Figure 92. If a write operation is aborted during a byte transfer ($\overline{CS}$ brought high), then that byte cannot be written to the destination register.

Destination registers can be up to 3 bytes wide—see the ADE7753 Register Description tables. Therefore the first byte shifted into the serial port at DIN is transferred to the MSB (most significant byte) of the destination register. If, for example, the addressed register is 12 bits wide, a 2-byte data transfer must take place. The data is always assumed to be right justified, therefore in this case, the four MSBs of the first byte would be ignored and the four LSBs of the first byte written to the ADE7753 would be the four MSBs of the 12-bit word. Figure 93 illustrates this example.

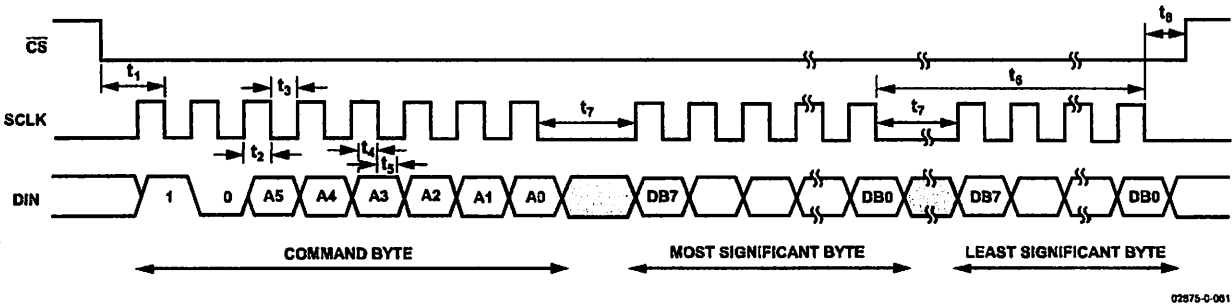


Figure 92. Serial Interface Write Timing

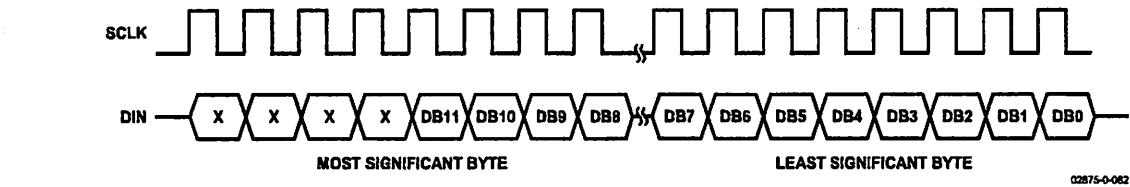


Figure 93. 12-Bit Serial Write Operation

ADE7753 Serial Read Operation

During a data read operation from the ADE7753, data is shifted out at the DOUT logic output on the rising edge of SCLK. As is the case with the data write operation, a data read must be preceded with a write to the communications register.

With the ADE7753 in communications mode (i.e., $\overline{CS}$ logic low), an 8-bit write to the communications register first takes place. The MSB of this byte transfer is a 0, indicating that the next data transfer operation is a read. The LSBs of this byte contain the address of the register that is to be read. The ADE7753 starts shifting out of the register data on the next rising edge of SCLK—see Figure 94. At this point, the DOUT logic output leaves its high impedance state and starts driving the data bus. All remaining bits of register data are shifted out on subsequent SCLK rising edges. The serial interface also returns communications mode again as soon as the read has been completed. At this point, the DOUT logic output enters a

high impedance state on the falling edge of the last SCLK pulse. The read operation can be aborted by bringing the $\overline{CS}$ logic input high before the data transfer is complete. The DOUT output enters a high impedance state on the rising edge of $\overline{CS}$.

When an ADE7753 register is addressed for a read operation, the entire contents of that register are transferred to the serial port. This allows the ADE7753 to modify its on-chip registers without the risk of corrupting data during a multibyte transfer.

Note that when a read operation follows a write operation, the read command (i.e., write to communications register) should not happen for at least 4 μs after the end of the write operation. If the read command is sent within 4 μs of the write operation, the last byte of the write operation could be lost. This timing constraint is given as timing specification t_9 .

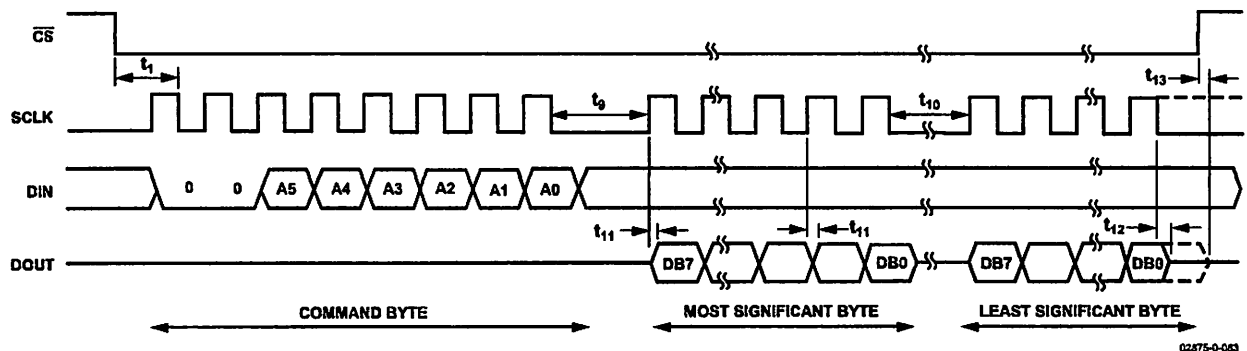


Figure 94. Serial Interface Read Timing

02875-0-063

ADE7753 REGISTERS

Table 12. Summary of Registers by Address

Address	Name	R/W	No. Bits	Default	Type ¹	Description
0x00	WAVEFORM	R	24	0x0	S	Waveform Register. This read-only register contains the sampled waveform data from either Channel 1, Channel 2, or the active power signal. The data source and the length of the waveform registers are selected by data Bits 14 and 13 in the mode register—see the Channel 1 Sampling and Channel 2 Sampling sections.
0x04	AENERGY	R	24	0x0	S	Active Energy Register. Active power is accumulated (integrated) over time in this 24-bit, read-only register—see the Energy Calculation section.
0x08	RAENERGY	R	24	0x0	S	Same as the active energy register except that the register is reset to 0 following a read operation.
0x0C	LAENERGY	R	24	0x0	S	Line Accumulation Active Energy Register. The instantaneous active power is accumulated in this read-only register over the LINECYC number of half line cycles.
0x10	VAENERGY	R	24	0x0	U	Apparent Energy Register. Apparent power is accumulated over time in this read-only register.
0x14	RVAENERGY	R	24	0x0	U	Same as the VAENERGY register except that the register is reset to 0 following a read operation.
0x18	LVAENERGY	R	24	0x0	U	Line Accumulation Apparent Energy Register. The instantaneous real power is accumulated in this read-only register over the LINECYC number of half line cycles.
0x1C	LVARENERGY	R	24	0x0	S	Line Accumulation Reactive Energy Register. The instantaneous reactive power is accumulated in this read-only register over the LINECYC number of half line cycles.
0x20	MODE	R/W	16	0x000C	U	Mode Register. This is a 16-bit register through which most of the ADE7753 functionality is accessed. Signal sample rates, filter enabling, and calibration modes are selected by writing to this register. The contents can be read at any time—see the Mode Register (0x9) section.
0x24	IRQEN	R/W	16	0x40	U	Interrupt Enable Register. ADE7753 interrupts can be deactivated at any time by setting the corresponding bit in this 16-bit enable register to Logic 0. The status register continues to register an interrupt event even if disabled. However, the IRQ output is not activated—see the ADE7753 Interrupts section.
0x28	STATUS	R	16	0x0	U	Interrupt Status Register. This is an 16-bit read-only register. The status register contains information regarding the source of ADE7753 interrupts—the see ADE7753 Interrupts section.
0x2C	RSTSTATUS	R	16	0x0	U	Same as the interrupt status register except that the register contents are reset to 0 (all flags cleared) after a read operation.
0x30	CH1OS	R/W	8	0x00	S ²	Channel 1 Offset Adjust. Bit 6 is not used. Writing to Bits 0 to 5 allows offsets on Channel 1 to be removed—see the Analog Inputs and CH1OS Register (0x0D) sections. Writing a Logic 1 to the MSB of this register enables the digital integrator on Channel 1, a Logic 0 disables the integrator. The default value of this bit is 0.
0x34	CH2OS	R/W	8	0x0	S ²	Channel 2 Offset Adjust. Bits 6 and 7 are not used. Writing to Bits 0 to 5 of this register allows any offsets on Channel 2 to be removed—see the Analog Inputs section. Note that the CH2OS register is inverted. To apply a positive offset, a negative number is written to this register.
0x38	GAIN	R/W	8	0x0	U	PGA Gain Adjust. This 8-bit register is used to adjust the gain selection for the PGA in Channels 1 and 2—see the Analog Inputs section.
0x3C	PHCAL	R/W	6	0x0D	S	Phase Calibration Register. The phase relationship between Channel 1 and 2 can be adjusted by writing to this 6-bit register. The valid content of this two's complement register is between 0x1D to 0x21. At a line frequency of 60 Hz, this is a range from -2.06° to $+0.7^{\circ}$ —see the Phase Compensation section.
0x40	APOS	R/W	16	0x0	S	Active Power Offset Correction. This 16-bit register allows small offsets in the active power calculation to be removed—see the Active Power Calculation section.

Address	Name	R/W	No. Bits	Default	Type ¹	Description
0x12	WGAIN	R/W	12	0x0	S	Power Gain Adjust. This is a 12-bit register. The active power calculation can be calibrated by writing to this register. The calibration range is $\pm 50\%$ of the nominal full-scale active power. The resolution of the gain adjust is 0.0244%/LSB—see the Calibrating an Energy Meter Based on the ADE7753 section.
0x13	WDIV	R/W	8	0x0	U	Active Energy Divider Register. The internal active energy register is divided by the value of this register before being stored in the AENERGY register.
0x14	CFNUM	R/W	12	0x3F	U	CF Frequency Divider Numerator Register. The output frequency on the CF pin is adjusted by writing to this 12-bit read/write register—see the Energy-to-Frequency Conversion section.
0x15	CFDEN	R/W	12	0x3F	U	CF Frequency Divider Denominator Register. The output frequency on the CF pin is adjusted by writing to this 12-bit read/write register—see the Energy-to-Frequency Conversion section.
0x16	IRMS	R	24	0x0	U	Channel 1 RMS Value (Current Channel).
0x17	VRMS	R	24	0x0	U	Channel 2 RMS Value (Voltage Channel).
0x18	IRMSOS	R/W	12	0x0	S	Channel 1 RMS Offset Correction Register.
0x19	VRMSOS	R/W	12	0x0	S	Channel 2 RMS Offset Correction Register.
0x1A	VAGAIN	R/W	12	0x0	S	Apparent Gain Register. Apparent power calculation can be calibrated by writing to this register. The calibration range is 50% of the nominal full-scale real power. The resolution of the gain adjust is 0.02444%/LSB.
0x1B	VADIV	R/W	8	0x0	U	Apparent Energy Divider Register. The internal apparent energy register is divided by the value of this register before being stored in the VAENERGY register.
0x1C	LINECYC	R/W	16	0xFFFF	U	Line Cycle Energy Accumulation Mode Line-Cycle Register. This 16-bit register is used during line cycle energy accumulation mode to set the number of half line cycles for energy accumulation—see the Line Cycle Energy Accumulation Mode section.
0x1D	ZXTOUT	R/W	12	0xFFF	U	Zero-Crossing Timeout. If no zero crossings are detected on Channel 2 within a time period specified by this 12-bit register, the interrupt request line (IRQ) is activated—see the Zero-Crossing Detection section.
0x1E	SAGCYC	R/W	8	0xFF	U	Sag Line Cycle Register. This 8-bit register specifies the number of consecutive line cycles the signal on Channel 2 must be below SAGLVL before the SAG output is activated—see the Line Voltage Sag Detection section.
0x1F	SAGLVL	R/W	8	0x0	U	Sag Voltage Level. An 8-bit write to this register determines at what peak signal level on Channel 2 the SAG pin becomes active. The signal must remain low for the number of cycles specified in the SAGCYC register before the SAG pin is activated—see the Line Voltage Sag Detection section.
0x20	IPKLVL	R/W	8	0xFF	U	Channel 1 Peak Level Threshold (Current Channel). This register sets the level of the current peak detection. If the Channel 1 input exceeds this level, the PKI flag in the status register is set.
0x21	VPKLVL	R/W	8	0xFF	U	Channel 2 Peak Level Threshold (Voltage Channel). This register sets the level of the voltage peak detection. If the Channel 2 input exceeds this level, the PKV flag in the status register is set.
0x22	IPEAK	R	24	0x0	U	Channel 1 Peak Register. The maximum input value of the current channel since the last read of the register is stored in this register.
0x23	RSTIPEAK	R	24	0x0	U	Same as Channel 1 Peak Register except that the register contents are reset to 0 after read.
0x24	VPEAK	R	24	0x0	U	Channel 2 Peak Register. The maximum input value of the voltage channel since the last read of the register is stored in this register.
0x25	RSTVPEAK	R	24	0x0	U	Same as Channel 2 Peak Register except that the register contents are reset to 0 after a read.
0x26	TEMP	R	8	0x0	S	Temperature Register. This is an 8-bit register which contains the result of the latest temperature conversion—see the Temperature Measurement section.

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ess	Name	R/W	No. Bits	Default	Type ¹	Description
	PERIOD	R	16	0x0	U	Period of the Channel 2 (Voltage Channel) Input Estimated by Zero-Crossing Processing. The MSB of this register is always zero. Reserved.
	TMODE	R/W	8	–	U	Test Mode Register.
	CHKSUM	R	6	0x0	U	Checksum Register. This 6-bit read-only register is equal to the sum of all the ones in the previous read—see the ADE7753 Serial Read Operation section.
	DIEREV	R	8	–	U	Die Revision Register. This 8-bit read-only register contains the revision number of the silicon.

1decoder: U = unsigned, S = signed by twos complement method, and S* = signed by sign magnitude method.

ADE7753 REGISTER DESCRIPTIONS

All ADE7753 functionality is accessed via the on-chip registers. Each register is accessed by first writing to the communications register and then transferring the register data. A full description of the serial interface protocol is given in the ADE7753 Serial Interface section.

COMMUNICATIONS REGISTER

The communications register is an 8-bit, write-only register which controls the serial data transfer between the ADE7753 and the host processor. All data transfer operations must begin with a write to the communications register. The data written to the communications register determines whether the next operation is a read or a write and which register is being accessed. Table 13 outlines the bit designations for the communications register.

B7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
I/R	0	A5	A4	A3	A2	A1	A0

Table 13. Communications Register

Bit Location	Bit Mnemonic	Description
A0 to A5	A0 to A5	The six LSBs of the communications register specify the register for the data transfer operation. Table 12 lists the address of each ADE7753 on-chip register.
	RESERVED W/R	This bit is unused and should be set to 0. When this bit is a Logic 1, the data transfer operation immediately following the write to the communications register is interpreted as a write to the ADE7753. When this bit is a Logic 0, the data transfer operation immediately following the write to the communications register is interpreted as a read operation.

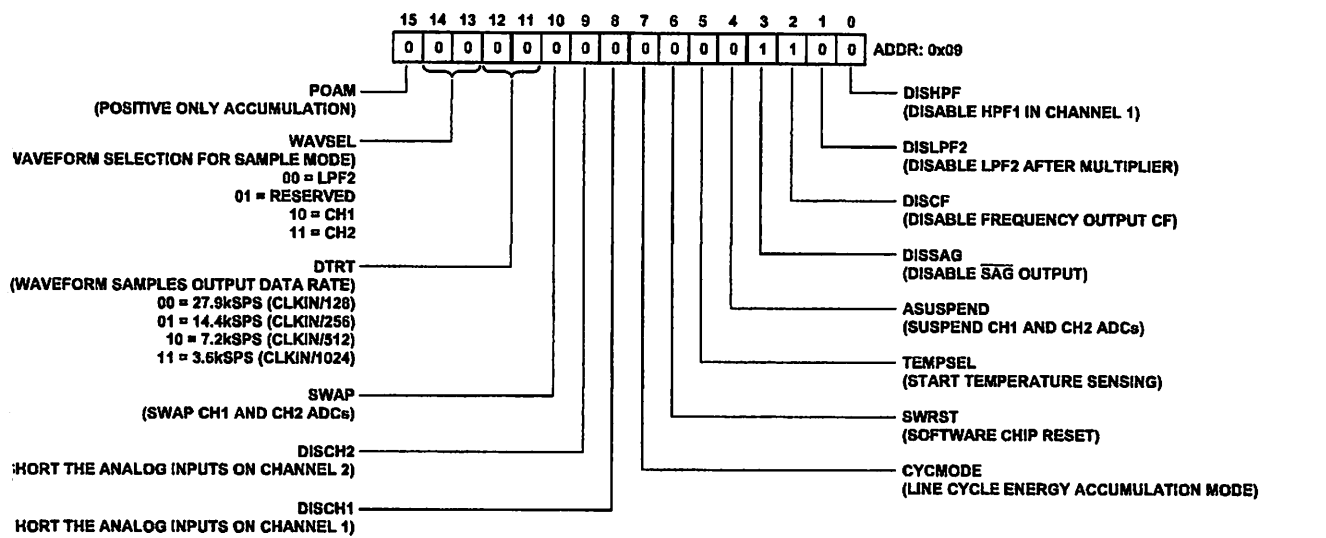
MODE REGISTER (0x09)

The ADE7753 functionality is configured by writing to the mode register. Table 14 describes the functionality of each bit in the register.

Table 14. Mode Register

Bit Location	Bit Mnemonic	Default Value	Description		
0	DISHPF	0	HPF (high-pass filter) in Channel 1 is disabled when this bit is set.		
	DISLPF2	0	LPF (low-pass filter) after the multiplier (LPF2) is disabled when this bit is set.		
	DISCF	1	Frequency output CF is disabled when this bit is set.		
	DISSAG	1	Line voltage sag detection is disabled when this bit is set.		
	ASUSPEND	0	By setting this bit to Logic 1, both ADE7753 A/D converters can be turned off. In normal operation, this bit should be left at Logic 0. All digital functionality can be stopped by suspending the clock signal at CLKIN pin.		
	TEMPSEL	0	Temperature conversion starts when this bit is set to 1. This bit is automatically reset to 0 when the temperature conversion is finished.		
	SWRST	0	Software Chip Reset. A data transfer should not take place to the ADE7753 for at least 18 μ s after a software reset.		
	CYCMODE	0	Setting this bit to Logic 1 places the chip into line cycle energy accumulation mode.		
	DISCH1	0	ADC 1 (Channel 1) inputs are internally shorted together.		
	DISCH2	0	ADC 2 (Channel 2) inputs are internally shorted together.		
0	SWAP	0	By setting this bit to Logic 1 the analog inputs V2P and V2N are connected to ADC 1 and the analog inputs V1P and V1N are connected to ADC 2.		
2, 11	DTRT1, 0	00	These bits are used to select the waveform register update rate.		
			DTRT 1	DTRT0	Update Rate
			0	0	27.9 kSPS (CLKIN/128)
			0	1	14 kSPS (CLKIN/256)
			1	0	7 kSPS (CLKIN/512)
			1	1	3.5 kSPS (CLKIN/1024)

Location	Bit Mnemonic	Default Value	Description
	WAVSEL1, 0	00	These bits are used to select the source of the sampled data for the waveform register.
			WAVSEL1, 0 Length Source
			0 0 24 bits active power signal (output of LPF2)
			0 1 Reserved
			1 0 24 bits Channel 1
	POAM	0	1 1 24 bits Channel 2
			Writing Logic 1 to this bit allows only positive active power to be accumulated in the ADE7753.



NOTE: REGISTER CONTENTS SHOW POWER-ON DEFAULTS

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Figure 95. Mode Register

INTERRUPT STATUS REGISTER (0x0B), RESET INTERRUPT STATUS REGISTER (0x0C),
INTERRUPT ENABLE REGISTER (0x0A)

The status register is used by the MCU to determine the source of an interrupt request ($\overline{\text{IRQ}}$). When an interrupt event occurs in the ADE7753, the corresponding flag in the interrupt status register is set to logic high. If the enable bit for this flag is Logic 1 in the interrupt enable register, the $\overline{\text{IRQ}}$ logic output goes active low. When the MCU services the interrupt, it must first carry out a read from the interrupt status register to determine the source of the interrupt.

Table 15. Interrupt Status Register, Reset Interrupt Status Register, and Interrupt Enable Register

Bit Location	Interrupt Flag	Description
	AEHF	Indicates that an interrupt occurred because the active energy register, AENERGY, is more than half full.
	SAG	Indicates that an interrupt was caused by a SAG on the line voltage.
	CYCEND	Indicates the end of energy accumulation over an integer number of half line cycles as defined by the content of the LINECYC register—see the Line Cycle Energy Accumulation Mode section.
	WSMP	Indicates that new data is present in the waveform register.
	ZX	This status bit is set to Logic 0 on the rising and falling edge of the the voltage waveform. See the Zero-Crossing Detection section.
	TEMP	Indicates that a temperature conversion result is available in the temperature register.
	RESET	Indicates the end of a reset (for both software or hardware reset). The corresponding enable bit has no function in the interrupt enable register, i.e., this status bit is set at the end of a reset, but it cannot be enabled to cause an interrupt.
	AEOF	Indicates that the active energy register has overflowed.
	PKV	Indicates that waveform sample from Channel 2 has exceeded the VPKLVL value.
	PKI	Indicates that waveform sample from Channel 1 has exceeded the IPKLVL value.
	VAEHF	Indicates that an interrupt occurred because the active energy register, VAENERGY, is more than half full.
	VAEOF	Indicates that the apparent energy register has overflowed.
	ZXTO	Indicates that an interrupt was caused by a missing zero crossing on the line voltage for the specified number of line cycles—see the Zero-Crossing Timeout section.
	PPOS	Indicates that the power has gone from negative to positive.
	PNEG	Indicates that the power has gone from positive to negative.
	RESERVED	Reserved.

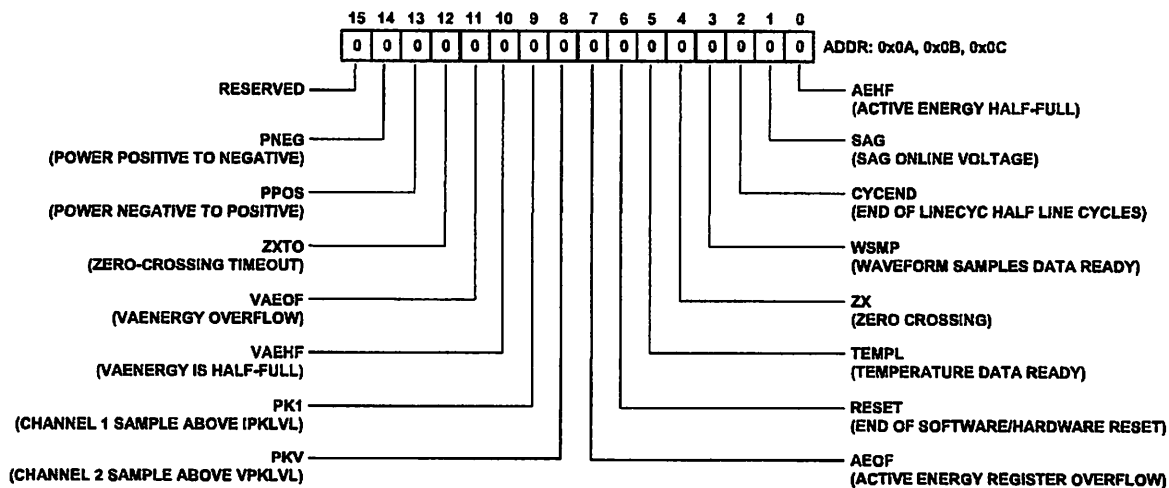


Figure 96. Interrupt Status/Interrupt Enable Register

02875-A-013

OS REGISTER (0x0D)

CH1OS register is an 8-bit, read/write enabled register. The MSB of this register is used to switch on/off the digital integrator in Channel 1, and Bits 0 to 5 indicates the amount of the offset correction in Channel 1. Table 16 summarizes the function of this register.

Table 16. CH1OS Register

Location	Bit Mnemonic	Description
	OFFSET	The six LSBs of the CH1OS register control the amount of dc offset correction in Channel 1 ADC. The 6-bit offset correction is sign and magnitude coded. Bits 0 to 4 indicate the magnitude of the offset correction. Bit 5 shows the sign of the offset correction. A 0 in Bit 5 means the offset correction is positive and a 1 indicates the offset correction is negative.
	Not Used	This bit is unused.
	INTEGRATOR	This bit is used to activate the digital integrator on Channel 1. The digital integrator is switched on by setting this bit. This bit is set to be 0 on default.

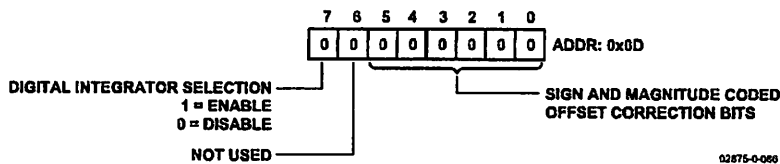


Figure 97. Channel 1 Offset Register

OUTLINE DIMENSIONS

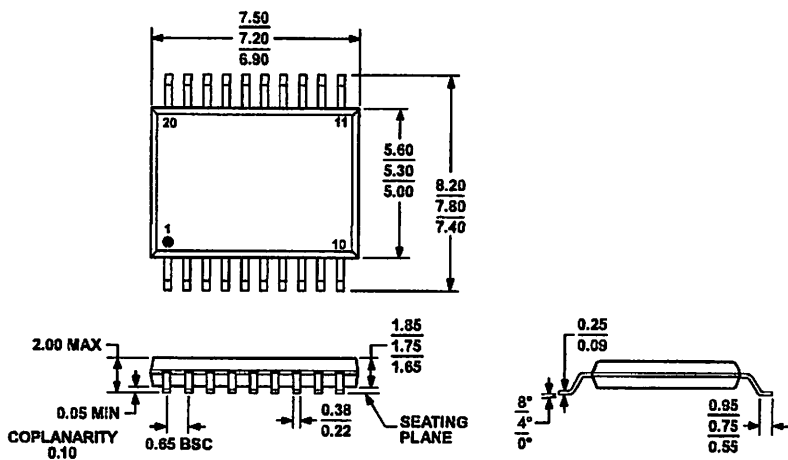


Figure 98. 20-Lead Shrink Small Outline Package [SSOP]
(RS-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
DE7753ARS	–40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
DE7753ARSRL	–40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
DE7753ARSZ	–40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
DE7753ARSZRL	–40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
VAL-ADE7753ZEB		Evaluation Board	

¹ = RoHS Compliant Part.

E7753

TES

BIOGRAFI PENULIS



Penulis lahir di Mojokerto pada tanggal 06 Agustus 1992 dari ayah Susetijono dan ibu Rr Sinta Tjawati. Penulis merupakan putra Ketiga dari 3 bersaudara. Penulis memulai pendidikan pada tahun 1998 di SDN Wates1 Kecamatan Magersari Kota Mojokerto. Pertengahan tahun 2005 penulis menempuh pendidikan di SMP Taman Siswa Kecamatan Magersari Kota Mojokerto sampai tahun 2008. Kemudian melanjutkan pendidikan di SMK Taman Siswa Kecamatan Magersari Kota Mojokerto mulai tahun 2008 dan lulus tahun 2011, kemudian pada tahun yang sama penulis melanjutkan studi di perguruan tinggi Institut Teknologi Nasional Malang. Penulis memilih Program Studi Teknik Elektro S-1, Konsentrasi Teknik Elektronika, Fakultas Teknologi Industri dan di wisuda tanggal 26 September 2015, dengan judul Skripsi "*Smart Meter Menggunakan IC ADE7753 dengan Koneksi Wireless untuk pengukur daya Listrik pada Sistem Smart Grid*". Selama menjadi mahasiswa, penulis menjadi asisten Laboratorium Sistem Kendali Industri pada tahun 2012 sampai 2015.