SKRIPSI

PEMBUATAN DAN PERANCANGAN ALAT PENGADUK PERMEN DENGAN FITUR PEMANAS PADA USAHA KECIL MENENGAH BERBASIS MIKROKONTROLLER AT89S51

Disusun Oleh :

SURYO ADI WIBOWO

05.12.201

INSTITUT TEKNOLOGI NASIONAL MALANG

FAKULTAS TEKNOLOGI INDUSTRI

JURUSAN TEKNIK ELEKTRO S-1

KONSENTRASI TEKNIK ELEKTRONIKA

2010

LEMBAR PERSETUJUAN

ALAT PENGADUK PERMEN DENGAN FITUR PEMANAS PADA USAHA KECIL MENENGAH BERBASIS MIKROKONTROLLER AT89S51

SKRIPSI

Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektro Strata Satu (S-1)

Disusun Oleh :

SURYO ADI WIBOWO
NIM : 05.12.201

Diperiksa dan Disetujui

Dosen Pembimbing

I. Komang Somawirata, ST, MT
NIP.P. 103 0100 361

Mengetahui,
Ketua Jurusan Teknik Elektro S-1

Ir. F. Yudi Limpraptono, MT.
NIP.Y. 103 9500 274

JURUSAN TEKNIK ELEKTRO S-1
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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
Jl. Karanglo km 2, Malang

BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

Nama : Suryo Adi Wibowo

NIM : 05.12.201

Jurusan : Teknik Elektro S-1

Konsentrasi : Teknik Elektronika

Judul Skripsi : **PEMBUATAN DAN PERANCANGAN ALAT PENGADUK PERMEN DENGAN FITUR PEMANAS PADA USAHA KECIL MENENGAH BERBASIS MIKROKONTROLLER AT89S51**

Dipertahankan di hadapan Majelis Penguji Skripsi Jenjang Strata Satu (S-1) pada :

Hari : Selasa

Tanggal : 09 februari 2010

Dengan Nilai : 87,15 (A)

Ketua Majelis Penguji	Sekretaris Majelis Penguji
Ir. H. Sidik Noertjahjono, MT.	Ir. F. Yudi Limpraptono, MT.
NIP.Y 102 8700 163	NIP.Y 103 9500 274

Penguji I	Penguji II
Joseph Dedy Irawan, ST,MT	Sotyohadi, ST
NIP. 132315178	NIP. Y. 1039700309

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
Jl. Karanglo Km. 2, Malang

BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

Nama : Supo Adi Wibowo

NIM : 05.12.201

Jurusan : Teknik Elektro S-1

Konsentrasi : Teknik Elektronika

Judul Skripsi : PEMBUATAN DAN PERANCANGAN ALAT PENGADUK
PERMEN DENGAN FITUR PEMANAS PADA USAHA KECIL
MENENGAH BERBASIS MIKROKONTROLLER ATMSS1

Dipertahankan di hadapan Majelis Penguji Skripsi jenjang Strata Satu (S-1) pada :

Hari : Selasa

Tanggal : 09 Februari 2010

Penilaian : 87,15 (A)

Ketua Majelis Penguji	Sekretaris Majelis Penguji
Ir. Widodo Noertjahjono, MT.	Ir. F. Yudi Limpraptono, MT.
NIP.Y 102 8700 163	NIP.Y 103 9500 274
Penguji I	Penguji II
Joseph Dedy Irawan, ST,MT	Sotyohadi, ST
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ABSTRAKSI

PEMBUATAN DAN PERANCANGAN ALAT PENGADUK PERMEN DENGAN FITUR PEMANAS PADA USAHA KECIL MENENGAH BERBASIS MIKROKONTROLLER AT89S51

Suryo Adi Wibowo.
Institut Teknologi Nasional Malang, Fakultas Teknologi Industri, Jurusan Teknik Elektro S-1, Kosentrasi Teknik Elektronika, *e-mail* :
norixx_adee@yahoo.com

Pada saat ini industri kecil-menengah berkembang sangat pesat seiring dengan kemajuan teknologi.Saat ini di kota-kota besar banyak mulai bermunculan industri kecil dan menengah. Di kota Malang sendiri saat ini banyak bermunculan industri kecil menengah dalam bidang hasil olahan pangan. Salah satunya industri kecil menengah yang memproduksi permen. Saat ini banyak perusahaan kecil yang membuat permen membutuhkan suatu alat yang berfungsi sebagai pengaduk dan memiliki fitur pemanas yang dapat membantu mempermudah proses produksi permen pada industri dengan skala kecil dan menengah.Maka dari itu di buatlah alat pengaduk permen dengan menggunakan mikrokontroller AT89S51 sebagai pengontrol utamanya yang berfungsi untuk mengontrol fitur-fitur yang ada pada alat pengaduk tersebut antara lain mengatur pengaduk yang menggunakan motor DC,mengontrol sensor suhu menggunakan sensor suhu LM 35 dan heater pemanas untuk memanaskan , memonitoring level air pada bejana pemanas air,serta fasilitas tambahan lain seperti timer untuk mengeset lama waktu pengadukan dan pengolahan.dari pembuatan alat pengaduk permen tersebut terdapat presentase error untuk pengujian timer dengan rata-rata error sebesar 0,84S% dan untuk pengujian sensor suhu denga presentase error rata-rata sebesar 4,27% .

Kata kunci: Alat Pengaduk Permen

KATA PENGANTAR

Dengan mengucap puji syukur kepada Tuhan Yang Maha Esa yang telah memberkati dan memberikan petunjuk serta jalan terbaik sehingga penulis dapat menyelesaikan skripsi dengan judul :

"PEMBUATAN DAN PERANCANGAN ALAT PENGADUK PERMEN DENGAN FITUR PEMANAS PADA USAHA KECIL MENENGAH BERBASIS MIKROKONTROLLER AT89S51"

Pembuatan skripsi ini disusun untuk memenuhi syarat akhir kelulusan pendidikan jenjang Strata I di Institut Teknologi Nasional Malang.

Terima kasih yang mendalam penulis haturkan kepada kakek dan nenek serta kedua orang tua yang telah berjasa membentuk kepribadian penulis, khususnya memberikan inspirasi yang kuat serta dukungan dan doa yang tiada henti. Terima kasih juga penulis sampaikan kepada :

1. Bapak Prof. Dr. Ir. Abraham Lomi, MSEE selaku rektor ITN Malang. .
2. Bapak Ir. H. Sidik Noertjahjono, MT selaku Dekan Fakultas Teknologi Industri ITN Malang.
3. Bapak Ir. F. Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro S-1 ITN Malang dan selaku Dosen Penguji I.
4. Bapak Ir. Yusuf Ismail Nakhoda, MT selaku Sekretaris Jurusan Teknik Elektro S-1 ITN Malang.
5. Bapak I.Komang Somawirata ST, MT selaku dosen pembimbing.
6. Semua pihak yang telah membantu penulis dalam menyelesaikan skripsi ini yang tidak bisa penulis sebutkan satu persatu.

Penulis menyadari bahwa skripsi ini masih banyak yang perlu disempurnakan. Oleh sebab itu kritik dan saran yang membangun sangat diharapkan.

Akhir kata penulis mohon maaf kepada semua pihak jika dalam proses pembuatan skripsi ini penulis melakukan kesalahan baik yang disengaja maupun tidak disengaja.

Semoga Tuhan Yang Yang Maha Esa selalu memberkati dan memberi jalan yang terbaik bagi kita semua. Amin.

Malang, Februari 2010

Penulis

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BAB I

PENDAHULUAN

1.1.Latar Belakang.

Perkembangan ilmu pengetahuan dan teknologi, khususnya teknologi yang berhubungan dengan elektronika telah mengalami perkembangan yang sangat pesat seiring dengan kemajuan zaman, dewasa ini perkembangan teknologi elektronika dapat di aplikasikan dan dimanfaatkan dalam berbagai bidang. Belakangan ini teknologi elektronika pada bidang industri berkembang sangat pesat.perkembangan ini meliputi alat-alat industri kecil yang di terapkan pada industri kecil menengah.pada saat ini industri kecil-menengah khususnya industri kecil menengah yang memproduksi permen membutuhkan alat pengaduk dan pemanas yang dapat membantu mempermudah proses industri. saat ini alat pengaduk permen yang memiliki fitur pemanas belum terlalu banyak tersedia di pasaran,dan bagaimana dapat memprogram sebuah Mikrokontroller agar bisa diaplikasikan pada alat pengaduk permen serta tampil pada LCD dan mengkondisikan sensor sesuai dengan kondisi yang di inginkan pada alat pengaduk permen.

1.2. Rumusan Masalah

Permasalahan yang ditangani pada pembuatan proyek akhir ini adalah karena saat ini alat pengaduk permen belum terlalu banyak tersedia di pasaran,dan

bagaimana dapat memprogram sebuah Mikrokontroller agar bisa diaplikasikan pada alat pengaduk permen serta ditampilkan pada LCD dan mengkondisikan sensor sesuai dengan kondisi yang di inginkan pada alat pengaduk permen. Masalah yang ditangani ialah pembuatan perangkat keras *(hardware)* adalah lebih mengfungsikan Mikrokontroller AT89S51 di kombinasikan dengan bahasa pemograman *bascom.*

Sehubungan dengan permasalahan diatas, maka dalam skripsi ini dipilih judul:

PEMBUATAN DAN PERANCANGAN ALAT PENGADUK PERMEN DENGAN FITUR PEMANAS PADA USAHA KECIL MENENGAH BERBASIS MIKROKONTROLLER AT89S51

1.3. Tujuan dan Manfaat

Adapun tujuan yang ingin dicapai dalam skripsi ini adalah

1. Mengurangi jumlah tenaga kerja untuk industri kecil dan menengah khususnya industri permen.
2. Mempermudah teknik pengadukan permen.
3. Mengaplikasikan Mikrokontroller AT89S51 sebagai alat pengaduk dan pemanas larutan karamel pada permen.

1.4. Batasan Masalah

Agar permasalahan tidak berkembang menjadi luas, oleh karena keterbatasan pengetahuan dan akibat timbulnya permasalahan baru, maka perlu dilakukan perbatasan masalah :

1. Tidak membahas software
2. Tidak membahas jaringan dan power supply .
3. suhu pada alat pemanas di batasi 100 derajat celcius

1.5. Metedologi

Untuk mencapai dari skripsi ini, maka metodologi dalam skripsi ini adalah sebagai berikut :

*a. **Studi Leteratur***

Dengan mempelajari beberapa kepustakaan yang mendukung, baik kepustakaan tentang perangkat keras dari sistem yang dibuat.

*b. **Perancangan Hardware dan Validasi Hardware***

Melakukan kegiatan pembuatan Alat dan Program *Assembly*.

*c. **Pengujian dan Analisa***

Setelah sistem selesai dibuat, maka diadakan pengujian untuk mendapat kekurangan dari sistem yang telah dirancang.

*d. **Penyusunan Laporan***

Penyusunan laporan dibuat dengan mengikuti sistematika pembahasan yang telah ditetapkan

1.6. Sistematika

sistematika penyusunan skripsi, sebagai berikut :

Bab I : **Pendahuluan**

Berisi latar belakang, tujuan, rumusan masalah, ruang lingkup, metodologi, serta sistematika penulisan.

Bab II : **Teori dasar**

Berisi tentang teori – teori dasar yang memiliki relevansi sebagai dasar perencanaan dan pembuatan alat.

Bab III: **Perencanaan dan Pembuatan**

Berisi tentang perencanaan hardware dan software

Bab IV: **Pengujian Alat**

Berisi tentang hasil pengujian peralatan yang telah di buat secara keseluruhan

Bab V : **Penutup**

Berisi kesimpulan dari hasil pengujian alat dan saran

BAB II

LANDASAN TEORI

Dalam merencanakan dan merealisasikan sistem ini dibutuhkan pemahaman mengenai pengetahuan yang berhubungan dengan aplikasi tersebut. Pemahaman tersebut akan sangat bermanfaat dalam perancangan perangkat keras maupun perangkat lunak. Adapun pengetahuan yang mendukung perencanaan dan realisasi alat antara lain bahan utama pada permen, sistem mikrokontroler AT89S51, Relay, adc, Transistor, LCD dan Motor DC.

2.1.Larutan Permen

2.1.1.Bahan Dasar Permen

Permen merupakan suatu olahan pangan yang sudah tdak dapat dipisahkan dalam kehidupan sehari-hari . Permen yang beredar di pasaran adalah jenis *hard candy* dan *soft candy.Hard candy* terbentuk jika gula atau sirup glukosa dimasak lebih lama,sedangkan *soft candy* adalah permen yang mengandung *gellatine* atau disebut *gummy candie.Hard candy* adalah permen yang teksturnya padat dan dimakan dengan cara menghisap.Sementara *soft candy* ditandai dengan teksturnya yang lunak.jenis permen ini ukan untuk diisap tetapi dikunyah.berdasarkan campurannya permen lunak terbagi menjadi dua jenis.yaitu *gummy candy* dan *chewy gum.*

Bahan baku dari *hard candy* atau permen keras biasanya terbuat dari *sukrosa* atau gula pasir.Ada juga yang menambahkan asam malat atau asam sitrat

untuk memunculkan rasa masam pada permen buah-buahan.rata-rata sebutir permen keras menghasilkan 20-30 kalori.

Sedangkan bahan baku dari *soft candy* tidak jauh berbeda dengan *hard candy* yaitu *glucose syrup*,gula,air .pewarna pemberi rasa atau asam sitrat,serta *gellatine*.Secara garis besar yang membedakan *hard candy* dan *soft candy* adalah *gellatine*.Fungsi dari *gelatine* sendiri ialah ntuk memberikan tekstur lunak pada *soft candy* dan memberikan sumbangan protein yang cukup besar pada *soft candy*.

2.2. Minimum Sistem AT89S51

2.2.1. Mikrokontroler AT89S51

Perbedaan mendasar antara mikrokontroller dan mikroprosesor adalah mikrokontroler selain memiliki CPU juga dilengkapi memori dan *input output* yang merupakan kelengkapan sebagai sistem minimum mikrokomputer sehingga sebuah mikrokontroller dapat dikatakan sebagai mikrokomputer dalam keping tunggal *(Single Chip Microcomputer)* yang dapat berdiri sendiri.

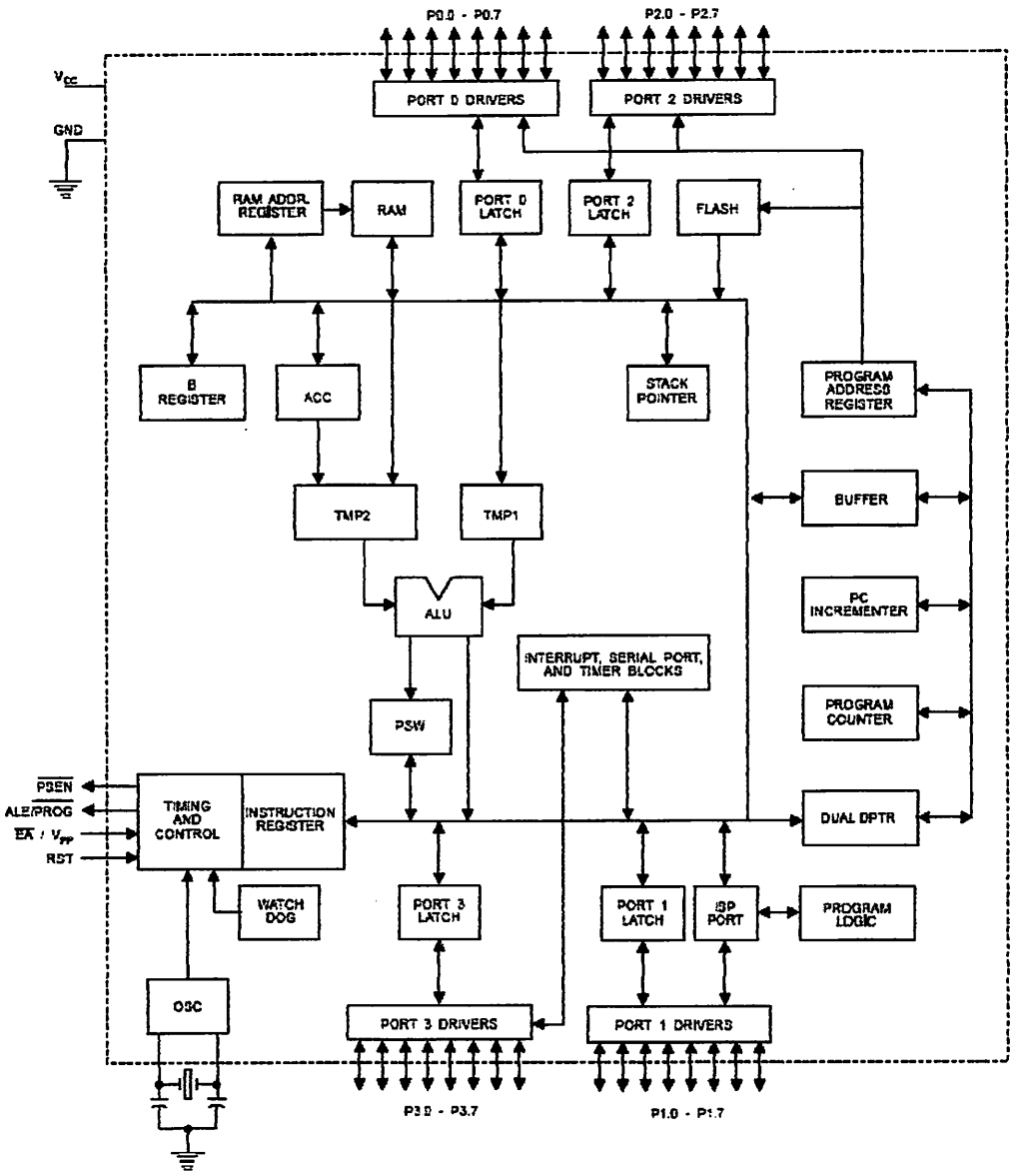
Mikrokontroller AT89S51 adalah mikrokontroler ATMEL yang kompatibel penuh dengan mikrokontroler keluarga MCS – 51, membutuhkan daya rendah, memiliki performance yang tinggi dan merupakan *microcomputer* 8 bit yang dilengkapi 4Kbyte EEPROM *(Electrical Erasable and Programmable Read Only Memory)* dan 128 *Byte* RAM *internal*. Program memori yang dapat diprogram ulang dalam sistem atau menggunakan programmer *Nonvolatile* memori konvensional. Dalam sistem mikrokontroler terdapat dua hal yang mendasar, yaitu: perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

2.2.2. Perangkat keras mikrokontroler AT89S51

Secara umum Mikrokontroller AT89S51 memiliki :

- CPU 8 bit termasuk keluarga MCS-51
- 4 Kb *Flash* memory
- 128 *byte Internal* RAM
  - 4 bank register, masing – masing berisi 8 register.
  - 16 byte yang dapat dialamati pada bit level.
  - 80 byte *general purpose memory data.*
- 32 buah Port I/O, tersusun atas P0 – P3, masing – masing 8 bit.
- 2 *Timer/ counter* 16 bit
- 2 *Serial Port Full Duplex*
- Kecepatan pelaksanaan intruksi per siklus 1 us pada frekuensi clock 12 Mhz
- 2 DPTR (*Data Pointer*)
- *Watchdog Timer*
- Fleksibel ISP Programming

Dengan keistimewaan Di atas pembuatan alat menggunakan AT89S51 menjadi lebih sederhana dan tidak memerlukan IC pendukung yang banyak. Adapun blok diagram dari Mikrokontroller AT89S51 adalah sebagai berikut :

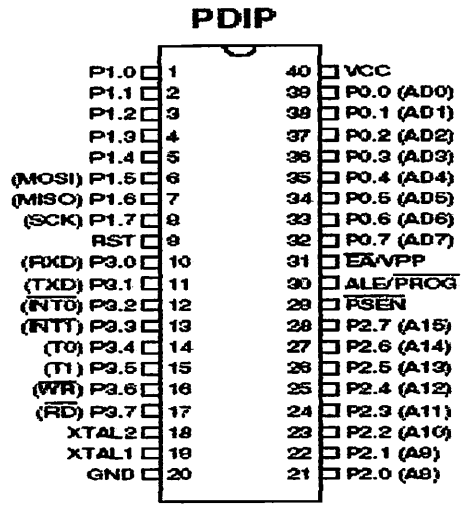


Gambar 2.1 Diagram Blok Mikrokontroller AT89S51

Sumber : Data Sheet Atmel AT89S51, halaman 3

2.2.3. Konfigurasi Pin Mikrokontroller AT89S51

Mikrokontroller AT89S51 terdiri dari 40 pin dengan konfigurasi sebagai berikut :



Gambar 2.2 IC AT89S51

Sumber : Data Sheet Atmel AT89S51, halaman 2

Fungsi tiap pin-nya adalah sebagai berikut :

1. Pin 1 sampai 8, **Port 1**

   Merupakan 8 bit I/O Bi-directional yang dilengkapi dengan internal Pull - Up. Ketika diberikan logika '1' pin ini akan di *Pull-Up* secara *internal* sehingga dapat digunakan sebagai *input*. Sebagai masukan jika pin – pin ini dihubungkan ke ground maka masing – masing pin ini dapat menghantarkan arus karena di *Pull-High* secara internal. Port 1 juga menerima *Low Order Address Bytes* selama melakukan verifikasi program.

   Pada *port* 1 di AT89S51 pin ini mempunyai alternatif seperti pada tabel berikut ini:

Tabel 2-1. Fungsi – Fungsi Alternative Port 1

Sumber : Data Sheet Atmel AT89S51,halaman 4

Port Pin	Alternative Functions
P1.5	MOSI (Master Output Sleve Input)
P1.6	MISO ((Master Input Sleve Output)
P1.7	SCK (Serial Clock)

2. Pin 9, **RST (*Reset*)**

   Merupakan pin yang aktif tinggi (*high*), pin ini aktif tinggi selama dua siklus mesin yang akan membuat mikrokontroler AT 89S51 menjalankan rutin *reset.*

3. Pin 10 sampai 17, **Port 3**

   Port 3 sebagai 8 bit I/O Bi-directional yang dilengkapi dengan *Pull-Up Internal.* Penyangga keluaran port 3 dapat memberikan atau menyerap arus empat masukan TTL (sekitar 1,6 mA). Jika diberikan logika '1' pada pin - pin port 3, maka masing – masing pin akan di *Pull High* oleh *Pull-Up internal* sehingga dapat digunakan sebagai *input*-an. Sebagai inputan, jika pin – pin port 3 dihubungkan ke *ground,* maka masing – masing kaki akan memberikan arus karena di *Pull High* secara internal, dimana Port 3 juga mempunyai fungsi-fungsi khusus yang dimiliki oleh keluarga MCS-51. Fungsi tersebut dapat dilihat dalam berikut ini :

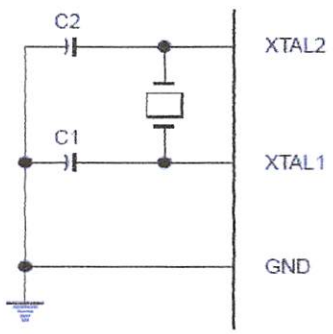
Tabel 2-2 Fungsi Khusus Pada Port 3

Sumber : Data Sheet Atmel AT89S51, halaman 5

Nama Penyemat	Fungsi Khusus
Port 3.0	RxD (port masukan serial)
Port 3.1	TxD (port keluaran serial)
Port 3.2	/INTO (masukan interupsi eksternal 0)
Port 3.3	/INT1 (masukan interupsi eksternal 1)
Port 3.4	T0 (masukan pewaktu eksternal 0)
Port 3.5	T1 (masukan pewaktu eksternal 1)
Port 3.6	/WR (sinyal tulis memori data eksternal)
Port 3.7	/RD (sinyal baca memori data eksternal)

4. Pin 18 sampai 19, ***X-TAL 1 dan X-TAL 2***

X-TAL 1 merupakan masukan ke rangkaian osilator *internal* sedangkan X-TAL 2 keluaran dari rangkaian osilator *internal*. Untuk keperluan ini diperlukan kapasitor penstabil sebesar 30pF. Dan nilai dari X-TAL tersebut antara 3 – 33 Mhz. Untuk lebih jelasnya dapat dilihat gambar pemasangan X-TAL serta kapasitor yang digunakannya.



Gambar 2.3 Osilator Eksternal AT89S51

5. Pin 20, **GND (*Ground*)**

   Dihubungkan dangan *ground* rangkaian.

6. Pin 21 sampai 28, **Port 2**

   Port 2 berfungsi sebagai 8 bit I/O Bi-directional yang dilengkapi dengan internal *Pull-Up* Penyangga keluaran port 2 dapat memberikan atau menyerap arus empat masukan TTL (sekitar 1,6 mA) Jika diberikan logika '1' pada pin – pin port 2, maka masing – masing pin akan di *Pull High* secara *internal* sehingga dapat digunakan sebagai *input*-an. Sebagai *input*-an jika pin – pin port 2 dihubungkan ke *ground* (di *Pull-Low*), maka, masing – masing pin dapat menghantarkan arus karena di *Pull High* secara *internal*. Port 2 mengeluarkan alamat bagian tinggi (A8-A15), selama pengambilan instruksi dari memori program eksternal dan selama pengaksesan memori data eksternal yang menggunakan perintah dengan alamat 16-bit (dengan perintah "MOVX @DPTR").

7. Pin 29, **$\overline{\text{PSEN}}$ (*Program Store Enable*)**

   Pin ini aktif rendah yang merupakan *strobe* pembacaan ke program memori eksternal.

8. Pin 30, **ALE (*Address Latch Enable*) / $\overline{\textit{PROG}}$**

   Keluaran ALE menghasilkan pulsa – pulsa untuk menahan alamat rendah (A0-A7) pada port 0, selama dilakukan proses baca atau tulis memori *external*. Pin ini juga berfungsi sebagai masukan pulsa program (*PROG*) selama pemrograman EEPROM *external*. Pada operasi normal, ALE akan

berpulsa dengan laju 1/6 dari frekuensi kristal dan dapat digunakan sebagai pewaktuan atau pendetakan (*clocking*).

9. Pin 31, $\overline{EA}$ / **VPP** (***External Access)***

   Dapat diberikan logika rendah (*ground*) atau logika tinggi (+5V). Jika diberikan logika tinggi maka mikrokontroller akan mengakses program dari ROM *internal* (EEPROM/*Flash Memori*), dan jika diberikan logika rendah maka mikrokontroler akan mengakses program dari memori *external* yang berlokasi 0000h sampai FFFFh.

10. Pin 32 sampai 32, **Port 0**

    Port 0 terdiri dari 8 saluran *input* atau *output* dua arah, tanpa internal *pull-up*. Port 0 merupakan bus alamat rendah ($A_0 - A_7$), yang dimultipleks dengan saluran bus data (D0-D7), yang digunakan pada saat mengakses memori data *external* dan memori program *external*.

11. Pin 40,**VCC**

    Merupakan masukan catu daya 5 volt dengan toleransi kurang lebih 10%.

2.2.4. Organisasi Memori

Organisasi yang dimiliki oleh AT89S51 yang terdiri atas :

1. RAM Internal

Memori sebesar 128 *byte* yang biasanya digunakan untuk menyimpan variabel atau data yang bersifat sementara. RAM *internal* terdiri atas :

- ***Register Banks***

  AT89S51 mempunyai delapan buah register yang terdiri atas R0 hingga R7. Kedelapan register ini selalu terletak pada alamat 00H hingga 07H pada setiap kali sistem direset. Namun posisi R0 hingga R7 dapat dipindah ke bank 1 (08 H hingga 0FH), bank 2 (10H hingga 17H) dan bank 3 (18H hingga 1FH), dengan mengatur bit RS0 dan RS1.

- ***Bit Addressable*** RAM

  RAM pada alamat 20H hingga 2FH dapat diakses secara pengalamatan *bit* (*bit addressable*) sehingga hanya dengan sebuah

  instruksi saja setiap *bit* dalam area ini dapat *diset, clear, AND, OR.*

- **RAM keperluan umum**

  RAM keperluan umum dimulai dari alamat 30H hingga 7FH dan dapat diakses dengan pengalamatan langsung maupun tak langsung. Pengalamatan langsung dilakukan ketika salah satu *operand* merupakan bilangan yang menunjukkan lokasi yang dialamati.

2. Special Function Register

Register fungsi khusus (*Special Function Register*) terletak pada 128 *byte* bagian atas memori data internal dan berisi *register-register* untuk pelayanan *latch port, timer, program status words, control peripheral* dan sebagainya. Alamat register fungsi khusus ditunjukkan pada Tabel 2-3.

Register-register ini hanya dapat diakses dengan pengalamatan langsung. Enam belas alamat pada register fungsi khusus dapat dialamati

per*bit* maupun per-*byte* dan terletak pada alamat 80_H-FF_H. Secara perangkat keras, register fungsi khusus ini dibedakan dengan memori data internal.

Tabel 2-3 Special Function Register

Sumber : Hafindo *Elektronic & Education*, Malang, 2001

Simbol	Nama Register	Nilai Pada Saat Reset	Alamat
ACC	Accumulator	00_H	$E0_H$
B	Register B	00_H	$F0_H$
PSW	Program Status Word	00_H	$D0_H$
SP	Stack Pointer	07_H	81_H
DPTR	Data Pointer 2 Byte		
DPL	Bit rendah	0000_H	82_H
DPH	Bit Tinggi	0000_H	83_H
P0	Port 0	$0FF_H$	80_H
P1	Port 1	$0FF_H$	90_H
P2	Port 2	$0FF_H$	$A0_H$
P3	Port 3	$0FF_H$	$B0_H$
IP	Interupt Periority Control	$XXX00000_B$	$D8_H$
IE	Interupt Enable Control	$0XX00000_B$	$A8_H$
TMOD	Timer/Counter Mode Control	00_H	89_H
TCON	Timer/Counter Control	00_H	88_H
TH0	Timer/Counter 0 High Control	00_H	$8C_H$
TL0	Timer/Counter 0 Low Control	00_H	$8A_H$
TH1	Timer/Counter 1 High Control	00_H	$8D_H$
TL1	Timer/Counter 1 Low Control	00_H	$8B_H$
SCON	Serial Control	00_H	98_H
SBUF	Serial Data Buffer	Independen	99_H
PCON	Power Control		87_H

Beberapa macam register fungsi khusus yang sering digunakan adalah sebagai berikut ini :

- *Accumulator* (ACC) merupakan register untuk penambahan dan pengurangan. Perintah *mnemonic* untuk mengakses akumulator disederhanakan sebagai A.
- Register B merupakan register khusus yang berfungsi melayani operasi perkalian dan pembagian.
- *Program Status Word* (PSW) yang terletak pada alamat D0H terdiri dari beberapa *bit* status yang menggambarkan kejadian di akumulator sebelumnya. Yaitu *carry bit*, *auxiliary carry*, dua *bit* pemilih bank, bendera *overflow*, *parity bit*, dan dua bendera yang dapat didefinisikan sendiri oleh pemakai. Keterangannya sebagai berikut :
  - Flag Carry

    Flag Carry (terletak pada alamat D7H) mempunyai fungsi sebagai pendeteksi terjadinya kelebihan pada operasi penjumlahan atau terjadi pinjam (*borrow*) pada operasi pengurangan. Misalnya jika data pada accumulator adalah FFH dan dijumlahkan dengan bilangan satu atau lebih, akan terjadi kelebihan dan membuat carry menjadi Set, sedangkan jika data pada accumulator adalah 00H dan dikurangkan dengan bilanagan satu atau lebih, akan terjadi pemimjaman dan membuat carry juga menjadi set.

  - Flag Auxilary Carry

Flag Auxilary Carry akan selalu Set pada saat proses penjumlahan terjadi carry dari bit ketiga hingga bit keempat.

- Flag 0

  Flag 0 digunakan untuk tujuan umum bergantung pada kebutuhan pemakai.

- Bit Pemilih Register Bank

  Register Bank Select Bits (RS0 dan RS1) atau Bit Pemilih Register Bank digunakan untuk menentukan lokasi dari Register Bank (R0 hingga R7) pada memori. RS0 dan RS1 selalu bernilai nol setiap kali system direset sehingga lokasi dari R0 hingga R7 akan berada di alamat 00H hingga 07H.

- Flag Overflow

  Flag Overflow akan diset jika pada operasi aritmatik menghasilkan bilangan yang lebih besar dari pada 128 atau lebih kecil dari – 128.

- Bit Pariti

  Bit Pariti akan diset jika jumlah bit 1 dalam accumulator adalah ganjil dan akan clear jika jumlah bit 1 dalam accumulator genap. Jika data dalam accumulator adalah 10101110b atau AEH pariti akan diset. Data AEH mempunyai lima bit yang berkondisi 1 atau dapat disebut mempunyai bit 1 dalam jumlah yang ganjil. Bit pariti ini digunakan untuk proses yang berhubungan dengan serial port yaitu sebagai *Check sum.*

- *Stack Pointer* (SP) merupakan register 8 bit yang dapat diletakkan di alamat manapun pada RAM *internal*. Isi *register* ini ditambah sebelum data disimpan, selama instruksi PUSH dan CALL. Pada saat *reset*, *register* SP diinisialisasi pada alamat 07_H, sehingga *stack* akan dimulai pada lokasi 08_H.
- *Data Pointer* (DPTR) terdiri dari dua register, yaitu untuk *byte* tinggi (*Data Pointer High*, DPH) dan byte rendah (*Data Pointer Low*, DPL) yang berfungsi untuk pengalamatan alamat 16 bit.
- Port 0 sampai Port 3 merupakan register yang berfungsi untuk membaca dan mengeluarkan data pada port 0, 1, 2, 3. Masing-masing register ini dapat dialamati per-*byte* maupun per-*bit*.
- *Serial data buffer* (SBUF) merupakan dua *register* yang terpisah, *register buffer* pengirim dan sebuah *register buffer* penerima. Meletakkan data pada SBUF berarti meletakkan pada *buffer* pengirim yang akan mengirimkan data melalui transmisi serial. Membaca data SBUF berarti menerima data dari *buffer* penerima
- *Control Register* terdiri dari register yang mempunyai fungsi kontrol. Untuk mengontrol sistem interupsi, terdapat dua register khusus, yaitu *register* IP (*Interupt Priority*) dan *register* IE (*Interupt Enable*). Untuk mengontrol pelayanan *timer/counter* terdapat *register* khusus, yaitu register TCON (*timer/counter control*) serta pelayanan port serial menggunakan register SCON (*Serial Port Control*).

- Register Timer

  AT89S51 mempunyai dua buah 16 bit Timer/Counter, yaitu Timer 0 dan Timer 1. Timer 0 terletak pada alamat 8AH untuk TL0 dan 8CH untuk TH0 dan Timer 1 terletak pada alamat 8BH untuk TL1 dan 8DH untuk TH1.

- Register Interupt

  89S51 mempunyai lima buah interupsi dengan sua level prioritas interupsi. Interupsi akan selalu nonaktif setiap kali system di – reset. Register – register yang berhubungan dengan interrupt adalah *Interrupt Enable Register* (IE) atau Register Pengaktif Interupsi pada alamat A8H untuk mengatur keaktifan tiap – tiap interrupt dan Interrupt Priority Register (IP) atau Register Prioritas Interupsi pada alamat B8H.

- Register Port Serial

  AT89S51 mempunyai sebuah *on chip serial port* (serial port dalam keping) yang dapat digunakan untuk berkomunikasi dengan peralatan lain yang menggunakan serial port juga seperti modem, shift register dan lain – lain.

  Buffer (Penyangga) untuk proses pengiriman maupun pengambilan data terletak pada register SBUF, yaitu pada alamat 99H. Sedangkan untuk mengatur mode serial dapat dilakukan dengan mengubah isi dari SCON yang terletak pada alamat 98H.

3. Flash PEROM

AT89S51 memiliki 4Kb *Flash* PEROM (*Programmable and Erassable Read Only Memori*), yaitu ROM yang dapat ditulis ulang atau dihapus menggunakan sebuah perangkat programmer hingga 1000 kali. Program yang ada pada *Flash* PEROM akan dijalankan jika pada saat sistem di-*reset*, pin EA/VP berlogika satu sehingga mikrokontroler aktif berdasarkan program yang ada pada *flash* PEROMnya. Namun, jika EA/VP berlogika nol, mikrokontroller aktif berdasarkan program yang berada pada memori *external*.

2.2.5. Mode Pengalamatan.

Mode pengalamatan yang digunakan pada AT89S51 adalah sebagai berikut:

a) Mode pengalamatan segera (*immediate addressing mode).*

   Cara ini menggunakan konstanta, misalnya: **MOV A, #20H.** Data konstanta merupakan data yang menyatu dengan instruksi, contoh instruksi tersebut diatas mempunyai arti bahwa data konstantanya yaitu 20H, (sebagai data konstanta harus diawali dengan '#') disalin ke akumulator A.

b) Mode pengalamatan langsung (*direct addressing mode*).

   Cara ini dipakai untuk menunjuk data yang berada di suatu lokasi memori dengan cara menyebut lokasi (alamat) memori tempat data tersebut berada, misalnya: **MOV A, 30H.** Instruksi ini mempunyai arti bahwa data yang berada di dalam memori dengan lokasi 30h disalin ke

akumulator. Bedanya dengan pengalamatan segera yaitu jika pada pengalamatan segera menggunakan tanda '#' yang menandai 20H sebagai data konstan, sedangkan pada instruksi ini tidak menggunakan '#' sehingga 30H diartikan sebagai suatu lokasi memori.

c) Mode pengalamatan tidak langsung (*indirect addressing mode*).

Cara ini dipakai untuk mengakses data yang berada di dalam memori, tetapi lokasi memori tidak disebut secara langsung tapi di-'titip'-kan ke register lain, misalnya: **MOV A, @R0.** R0 adalah register serba guna yang dipakai untuk menyimpan lokasi memori, sehingga instruksi ini mempunyai arti memori yang alamat lokasinya tersimpan dalam R0 isinya disalin ke akumulator A. Tanda '@' dipakai untuk menandai lokasi memori yang tersimpan di dalam R0. *Register* serba guna R0 berfungsi sebagai register penyimpan alamat (*indirect address*), selain R0 register serba guna lainnya, R1 juga bisa dipakai sebagai register penampung alamat.

d) Mode pengalamatan register (*register addressing mode*).

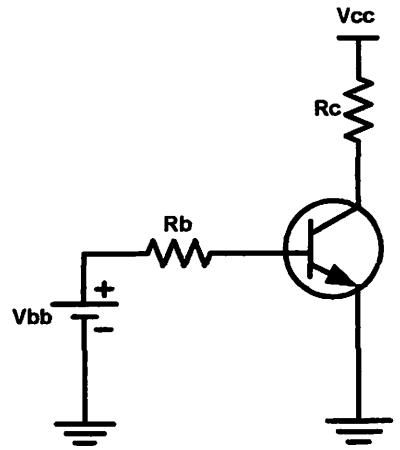
Misalnya: **MOV A, R5** ,instruksi ini mempunyai arti bahwa data dalam register serba guna R5 disalin ke akumulator A. Instruksi ini menjadikan register serba guna R0 sampai R7 sebagai tempat penyimpanan data yang praktis dan kerjanya sangat cepat.

e) Mode pengalamatan kode tidak langsung (*code indirect addressing mode*).

MCS51 mempunyai cara penyebutan data dalam memori program yang dilakukan secara tak langsung, misalnya: **MOVC A, @A+DPTR.** Instruksi MOV diganti dengan MOVC, tambahan huruf C tersebut dimaksud untuk membedakan bahwa instruksi ini digunakan untuk memori program (MOV tanpa huruf C artinya digunakan untuk memori data). Tanda '@' digunakan untuk menandai A+DPTR yang berfungsi untuk menyatakan lokasi memori yang isinya disalin ke Akumulator A, dalam hal ini nilai yang tersimpan dalam DPTR (*Data Pointer Register* – 2 byte) ditambah dengan nilai yang tersimpan dalam akumulator A (1 byte) sama dengan lokasi memori program yang diakses.

2.3. Transistor Sebagai Switching

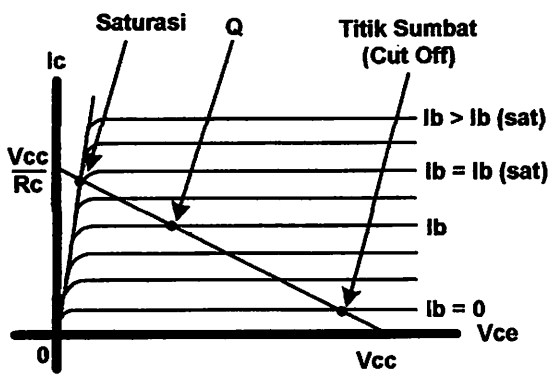
Transistor merupakan sebuah komponen semikonduktor yang banyak digunakan pada berbagai rangkaian elektronik baik sebagai penguat dan saklar. Asas kerja dari transistor adalah akan ada arus yang mengalir diantara terminal kolektor – emitor (I_C) hanya apabila ada arus yang mengalir diantara terminal basis – emitor (I_B). Jadi transistor harus dioperasikan pada daerah linier agar diperoleh sinyal keluaran yang tidak cacat (distorsi). Untuk dapat mengoperasikan secara tepat maka pengertian tentang titik kerja transistor amatlah penting dan harus pahami dan dimengerti dengan benar.



Gambar 2-4. Rangkaian Switching Transistor

Sumber : Prinsip-Prinsip Elektronika, halaman 201

Garis beban akan memotong sekelompok kurva arus basis constant I_B dengan I_B tertentu (yang diatur rangkaian bias), garis beban akan memotong kurva I_B tersebut dititik Q yang disebut titik kerja transistor. Titik kerja ini menjadi kondisi awal dari pengoperasian transistor kelak dimana transistor tersebut mempunyai tiga daerah kerja yaitu aktif (*active*), jenuh (*saturation*), dan tersumbat (*cut-off*).



Gambar 2.5. Karakteristik I_C-V_{CE} Transistor Bipolar

Sumber : Prinsip-Prinsip Elektronika, halaman 205

Pada gambar di atas dapat dilihat, titik dimana garis beban memotong kurva $I_B = 0$ disebut sebagai titik sumbat (cut-off). Pada titik ini arus kolektor (I_C) sangat kecil (hanya arus bocor) sehingga dapat diabaikan, di sini transistor kehilangan kerja normalnya. Di sini dapat dikatakan bahwa tegangan kolektor-emitor sama dengan ujung dari garis beban tersebut.

$$V_{CE(cut\text{-}off)} \cong V_{CC}$$

Perpotongan garis beban dengan kurva $I_B = I_{B(sat)}$ disebut titik jenuh (saturation). Pada titik ini arus kolektor maksimum atau dapat dikatakan bahwa arus kolektor sama dengan ujung dari garis beban.

$$I_{C(sat)} \cong \frac{V_{CC}}{R_C}$$

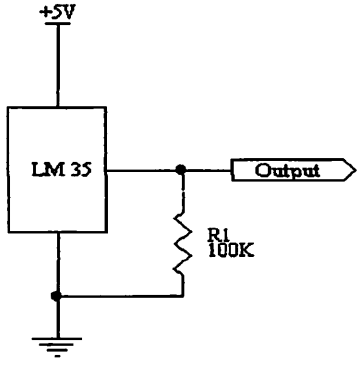
Jika arus basis I_B lebih kecil dari $I_{B(sat)}$ maka transistor akan beroperasi pada daerah aktif, yaitu titik kerjanya terletak di sepanjang garis beban.

Jadi disimpulkan bahwa transistor bipolar bekerja sebagai suatu sumber arus (penguat) dimana saja sepanjang garis beban, kecuali titik jenuh (*saturation*) atau titik sumbat (*cut-off*) yaitu transistor tidak lagi bekerja sebagai sumber arus (penguat) melainkan sebagai saklar (*switching*)

2.4. Tranduser Temperatur/Suhu (IC LM35)

IC LM35 series merupakan rangkaian integrasi untuk sensor temperatur yang mempunyai tegangan output seebanding dengan derajat celcius (^{0}C). IC LM35 menghasilkan kenaikan tegangan 10 mV pada outputnya pada setiap kenaikan 1 ^{0}C.

IC LM35 mempunyai keuntungan lebih linier dari sensor temperatur yang disesuaikan dengan ^{0}C, sehingga penggunaannya tidak perlu mengurangi besar tegangan dari outputnya. IC LM35 juga tidak perlu banyak mengkalibrasi eksternal / memberikan keakurasian khusus pada temperatur ruang ± ¼ ^{0}C dan ± ¾ ^{0}C, dengan range temperatur antara –55^{0}C sampai +150^{0}C.

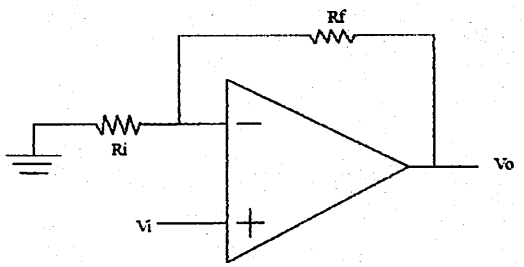


Gambar 2.6. Rangkaian LM 35

2.5. Penguat Operasional

Penguat operasional (op amp) adalah suatu rangkaian terintegrasi yang berisi beberapa tingkat dan konfigurasi penguat diferensial yang telah dijelaskan di atas. Penguat operasional memilki dua masukan dan satu keluaran serta memiliki penguatan DC yang tinggi. Untuk dapat bekerja dengan baik, penguat operasional memerlukan tegangan catu yang simetris yaitu tegangan yang berharga positif (+V) dan tegangan yang berharga negatif (-V) terhadap tanah (*ground*). Berikut ini adalah simbol dari penguat operasional:

Rangkaian yang digunakan dalam skripsi ini akan menggunakan penguat operasional yang bekerja sebagai penguat. Berikut ini adalah konfigurasi op amp yang bekerja sebagai penguat:



Gambar 2.7. Rangkaian Pengkondisi Sinyal

Gambar di atas adalah gambar sebuah penguatm non inverting. Penguat tersebut dinamakan penguat noninverting karena masukan dari penguat tersebut adalah masukan noninverting dari op amp. Sinyal keluaran penguat jenis ini sefasa dengan sinyal keluarannya. Adapun besar penguatan dari penguat ini dapat dihitung dengan rumus:

$$A_V = (Ri+Rf)/Ri$$

$$A_V = 1 + {}_{Rf/Ri}$$

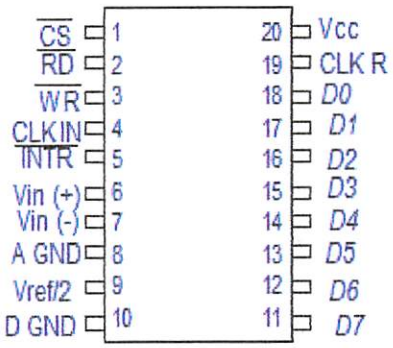
2.6. ADC 0804 (*Analog to Digital Conventer*)

Analog to Digital Conventer (ADC) adalah Rangkaian atau devais yang mengubah input analog menjadi output digital dalam bentuk biner yang ekivalen.

Dimana setiap perubahan pada output menyatakan beberapa kenaikkan dari tegangan atau arus input.

Spesifikasi lain selain ketelitian (akurasi) dan linearitas adalah waktu konversi (*convertion time*). Waktu konversi ADC adalah waktu yang diperlukan ADC untuk menghasilkan kode biner yang valid untuk tegangan masukkan yang diberikan. Semakin pendek waktu konversi berarti kecepatan konversi semakin tinggi.

ADC 0804 adalah ADC yang mempunyai resolusi 8-bit dengan keluaran data parallel yang telah dilengkapi dengan clock internal. ADC ini dapat menerima tegangan input sebesar 0 sampai 5 Volt.



Gambar 2.8. Konfigurasi pin – pin ADC 0804 [5)]

[5)] Albert Paul Malvino, *Elektronika Komputer Digital*, 1998, Halaman 35

Dalam proses konversi ADC, perlu diperhatikan beberapa parameter yang akan menentukan mutu sebuah ADC yaitu :

- kesalahan kuantitatis
- ketidaklinieran

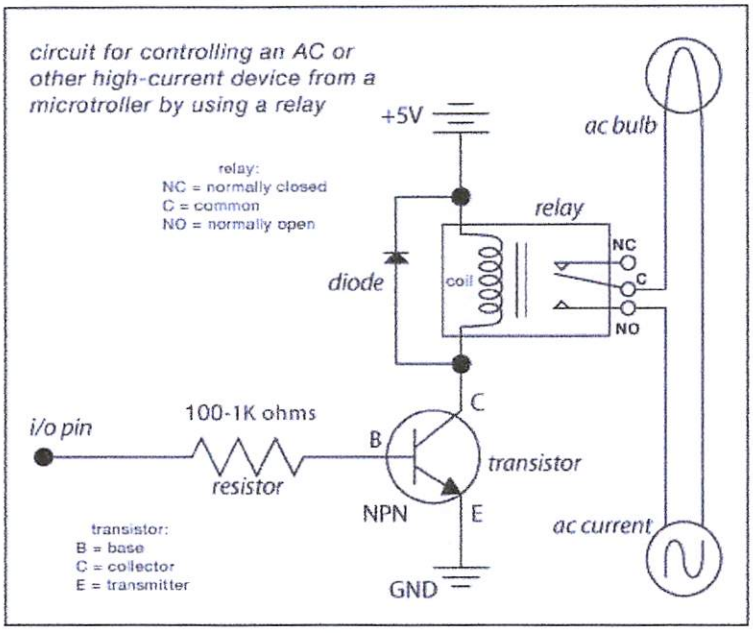
- kode tidak lengkap
- waktu konversi

Karakteristik yang linier didekati dengan karakteristik dalam bentuk anak tangga sehingga timbul kesalahan kuantisasi sebesar setengah dari anak tangga. Karena tinggi anak tangga adalah sama dengan bit paling terendah (least significant, LSB) dalam bilangan biner, maka kesalahan tersebut sama dengan ½LSB.

Kadang – kadang persediaan bit tertentu tidak tersedia dengan perkataan lain sebuah tangga dilompati. Kombinasi semacam itu disebut kode yang hilang (missing kode). Kode yang hilang tidak terjadi bila kesalahan linieritas kurang dari ± ½ LSB. Waktu yang dibutuhkan ADC untuk mengubah tegangan menjadi bit kombinasi disebut waktu konversi (convertion time).

2.7. Rangkaian Relay dan driver

Relay adalah komponen elektronika yang terdiri dari sebuah lilitan kawat (kumparan/koil) yang terlilit pada suatu inti besi lunak. Jika kumparan dialiri oleh arus listrik, maka inti besi akan menjadi magnet. *Relay* merupakan alat untuk membuka dan menutup kontak secara elektrik dengan tujuan menghubungkan fungsi dari rangkaian satu dengan rangkaian yang lainnya.



Gambar 2,9. Rangkaian relay dengan driver

Sumber : www.google.com

Kontak-kontak yang ada pada relay ada dua macam, yaitu *Normally Open* (relay yang kontaknya terbuka pada saat belum ada arus yang melalui kumparan dan tertutup pada saat ada arus) dan *Normally Closed* (relay yang kontaknya tertutup pada saat belum ada arus yang melalui kumparan dan terbuka pada saat ada arus).

Keuntungan memakai *relay* umumnya terletak pada pengaturan *switching*-nya, sehingga terjadi isolasi antara rangkaian catu daya rendah dengan catu daya beban yang tinggi yang akan diputus dan disambung. Kerugian relay umumnya terjadi tanggapan waktu yang *relative* lambat saat ON/OFF.

Cara kerja relay adalah sebagai berikut :

Jika ada arus yang masuk melalui kumparan, maka pada kumparan tersebut akan menghasilkan induksi magnet. Induksi magnet tersebut akan

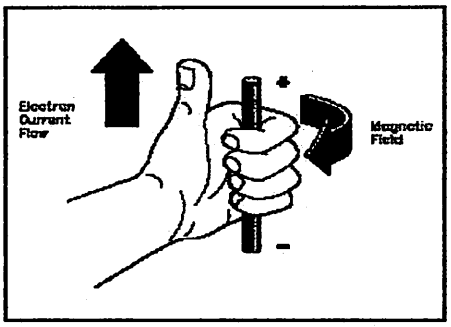
menarik pegas kontak, yang akan merubah posisi awalnya menjadi terhubung ke bagian yang lain. Setelah arus terhenti maka tidak ada induksi sehingga kontak kembali pada kondisi semula.

2.8. Motor Arus Searah (Motor DC)

Motor arus searah (dc) adalah devais mesin yang berfungsi mengubah tenaga listrik arus searah menjadi tenaga mekanik dimana tenaga gerak tersebut berupa putaran rotor. Dalam kehidupan sehari-hari motor arus searah sering dijumpai di mana-mana. Sebagai contoh adalah motor yang di pasang pada *starter* mobil, mainan anak-anak, *tape recorder* dan lain sebagainya. Sedangkan pada pabrik-pabrik, motor arus searah dapat dijumpai pada *elevator*, *conveyor* dan sebagainya.

2.8.1. Prinsip Dasar Motor Arus Searah (Motor DC)

Prinsip dasar dari motor arus searah adalah kalau sebuah kawat berarus diletakkan antara kutub magnet (U-S), maka pada kawat tersebut akan bekerja suatu gaya yang akan menggerakkan kawat tersebut. Arah gerak dari kawat tersebut dapat ditentukan dengan " Kaidah Tangan Kiri " yang berbunyi sebagai berikut : " Apabila tangan kiri dibiarkan terbuka dan diletakkan diantara kutub utara dan kutub selatan, sehingga garis-garis gaya yang keluar dari kutub utara menembus telapak tangan kiri dan arus di dalam kawat mengalir searah dengan keempat jari, maka kawat tersebut akan mendapat gaya yang jatuhnya sesuai dengan ibu jari ", seperti pada gambar 2-10.



Gambar 2.10. Kaidah Tangan Kiri

Sumber : www.google.com

Adapun besarnya gaya yang bekerja pada kawat tersebut dapat dirumuskan sebagai berikut :

F = B x I x L **(Newton)** dimana :

B = kerapatan fluks magnet (Weber)

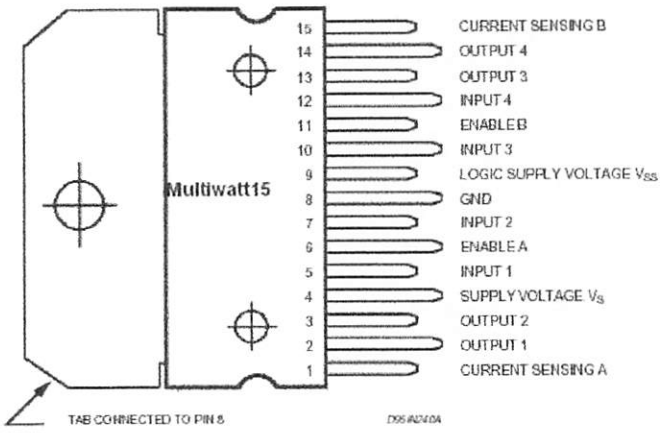
L = Panjang penghantar (meter)

I = Arus listrik (Ampere)

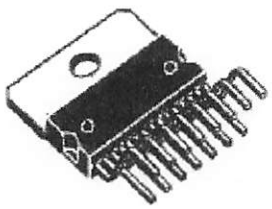
2.9. L 298N

L 298N merupakan driver berjembatan ganda yang memiliki tegangan serta arus yang tinggi. Dua input enable berfungsi mengkondisikan sinyal input pada komponen.Emitor pada transistor terendah di jembatan tergabung bersama-sama dan dikoneksikan pada hambatan luar.

L 298N mampu beroperasi pada tegangan supply hingga 46 V.Total arus DC hingga 4 A.Memiliki tegangan saturasi yang rendah serta tahan pada kondisi bertemperatur sangat tinggi.



Gambar 2.11. Pin – pin koneksi L 298N
www.data sheetcatalog.com



Gambar 2.12. Bentuk Fisik L 298N(Multiwatt 15)
www.data sheetcatalog.com

2.10 LCD (Liquid Crystal Display)

Liquid cristal display adalah modul tampilan yang mempunyai konsumsi daya yang relatif rendah dan terdapat sebuah controler CMOS didalamnya. Controler tersebut sebagai pembangkit ROM/RAM dan display data RAM. Semua fungsi tampilan di kontrol oleh suatu instruksi modul LCD dapat dengan mudah diinterfacekan dengan MPU. Ciri-ciri dari LCD LMB162A:

- Terdiri dari 32 karakter yang dibagi menjadi 2 baris dengan display dot matrik 5 X 7 ditambah cursor
- Karakter generator ROM dengan 192 karakter

- Karakter generator RAM dengan 8 tipe karakter
- 80 X 8 bit display data RAM
- Dapat diinterfacekan dengan MPU 8 atau 4 bit
- Dilengkapi fungsi tambahan : Display clear, cursor home, display ON/OFF, cursor ON/ OFF, display character blink, cursor shift dan display shift
- Internal data
- Internal otomatis dan reset pada power ON
- +5 V power supply tunggal

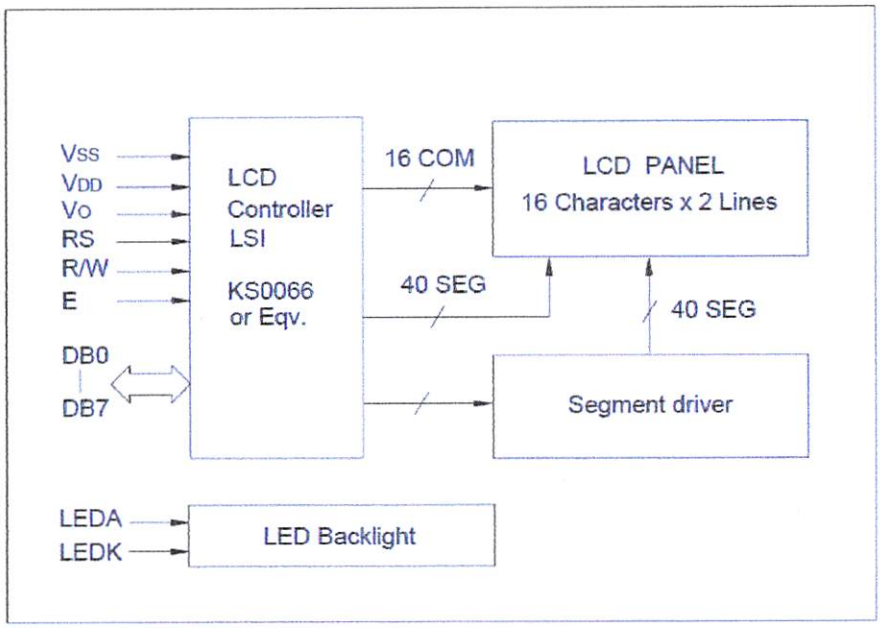
Tabel 2.7. merupakan pin-pin LCD berserta konfigurasinya:

Tabel 2.4.
Pin-Pin LCD Dan Konfigurasinya

PIN	Name	Function
1	VSS	Ground voltage
2	VCC	+5V
3	VEE	Contrast voltage
4	RS	Register Select 0 = Instruction Register 1 = Data Register
5	R/W	Read/ Write, to choose write or read mode 0 = write mode 1 = read mode
6	EN	Enable 0 = start to lacht data to LCD character 1= disable
7	DB0	LSB
8	DB1	-
9	DB2	-
10	DB3	-
11	DB4	-
12	DB5	-
13	DB6	-

14	DB7	MSB
15	BPL	Back Plane Light
16	GND	Ground voltage

2.8.1.Blog diagram dari LCD LMB162A



Gambar 2.13 Blog diagram dari LCD LMB162A

Register

Control LCD mempunyai 2 register 8 bit yaitu *Instruction register* (IR) dan *Data Register* (DR). Kedua register tersebut dipilih melalui *Register Select* (RS). IR menyimpan kode instruksi seperti *Display clear* dan *cursor shift*, dan alamat informasi dari *Display* Data RAM (DD RAM) dan karakter generator RAM (CG RAM).

DR menyimpan data sementara untuk ditulis ke DD RAM atau CG RAM, atau dibaca dari DD RAM atau CG RAM. Ketika data ditulis ke DD RAM atau CG RAM dari MPU, data di DR secara otomatis ditulis ke DD RAM atau CG RAM dengan operasi internal. Tetapi ketika data dibaca dari DD RAM atau CG RAM maka alamat data ditulis pada IR.Data tersebut akan dimasukkan ke DR dan

MPU akan membaca data dari DR, Setelah operasi pembacaan, alamat berikutnya diset data dari DD RAM atau CG RAM pada alamat tersebut akan dimasukkan ke DR untuk operasi berikutnya.

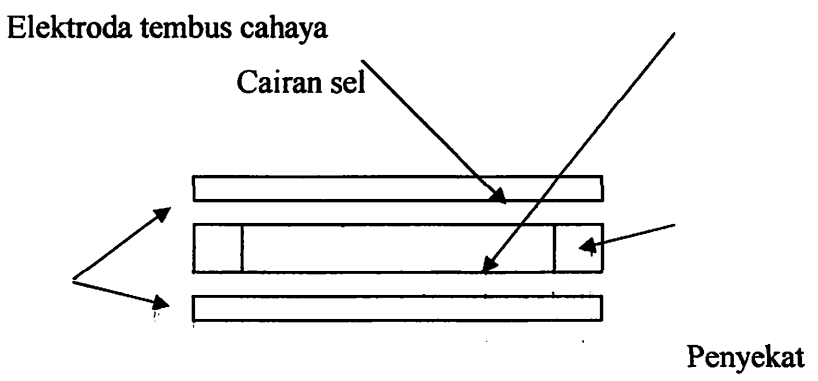
Display data RAM (DD RAM) mempunyai kapsitas area 80 X 8 bit. Beberapa area dari DDRAM yang tidak digunakan untuk display dapat digunakan sebagai General data RAM.

Pada LCD masing-masing pin mempunyai range alamat tersendiri, alamat itu diekspresikan dengan bilangan heksa. Untuk line 1 range alamat berkisar antara 00h-0fh sedangkan untuk line 2 alamat berkisar antara 40h-4fh

Encoder

Informasi atau data ada kalanya dikodekan dalam bentuk kode. Untuk mengkode data digital tersebut digunakan suatu encoder. Salah satu contoh dari encoder adalah encoder 16 to 4 line yang digunakan untuk mengkode 16 saluran data desimal menjadi 4 saluran data BCD. Keluaran encoder merupakan kode dari salah stu input yang diaktifkan. Endcoder mempunyai 2^N masukan dan N buah line keluaran.

Gambar 2.7. berikut ini merupakan konstruksi dari cairan sel kristal pada LCD :



Gambar 2.14. Konstruksi dari Cairan Sel Kristal

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

3.1. Umum

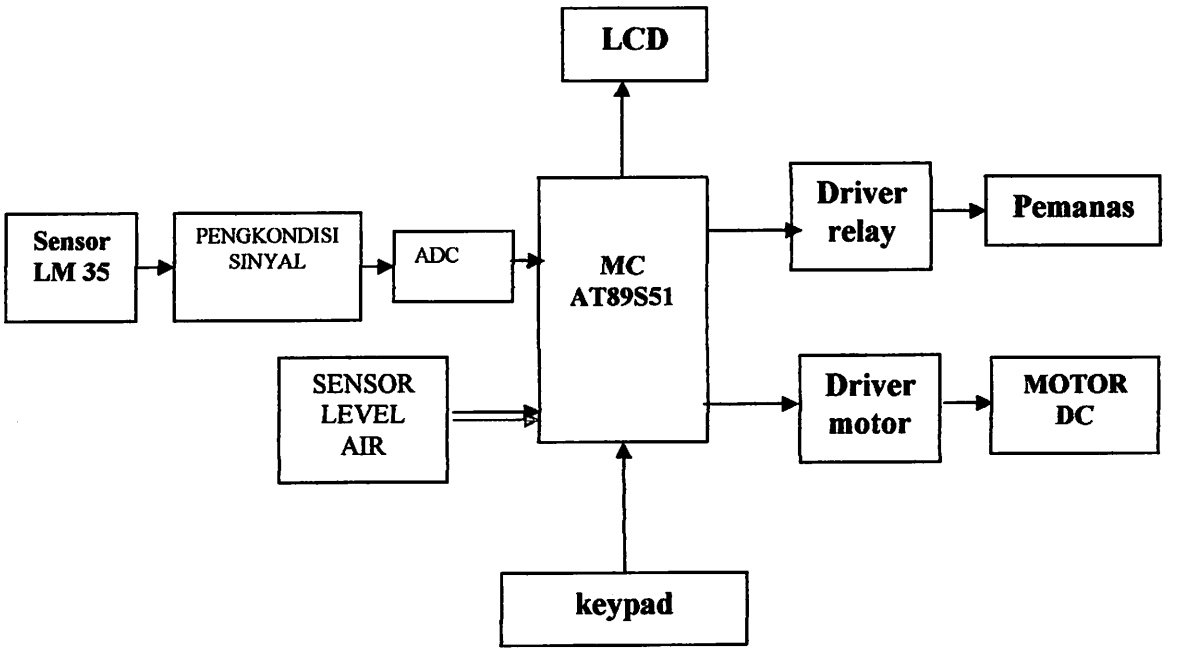
Pada pengerjaan skripsi ini, Mikrokontroller yang meliputi hardware dan software. Sebelum membahas tentang perencanaan dan pembuatan, maka perencanaan dibuat matang agar sistem dapat direalisasikan dengan baik sesuai target.

3.2 Perangkat Keras

Pada tahap ini akan menjelaskan mengenai perangkat keras apa saja yang akan digunakan dalam Alat.

3.2.1 Diagram Blok

Pada perancangan suatu hardware atau perangkat keras diperlukan digaram blok yang berfungsi sebagai pedoman untuk merancang atau membuat suatu alat sesuai dengan cara kerja alat dan sistem kerja alat yang dikehendaki.Pada pengerjaan skripsi ini juga dibuat diagram blok tentang keseluruhan cara kerja alat yang yang akan dirancang padas kripsi ini.Diagram blok dan perangkat keras (Hardware) yang direncanakan, diperlihatkan pada gambar 3.1.



Gambar 3.1 Blok diagram perancangan

Fungsi Dari Masing-masing blok

1. Sensor lm35 berfungsi sebagai sensor suhu tiap $1^{o}C$ mengalami perubahan sebesar 10_{mV}
2. Pengkondisi sinyal sebagai pengkondisi sinyal lm 35 yang masih lemah dikuatkan oleh pengkondisi sinyal ini
3. ADC mengkonversikan sinyal inputan yang berupa sinyal analog dari pengkondisi sinyal yang selanjutnya outputannya berupa sinyal digital
4. Mikrokontroler AT89S51 berfungsi sebagai pemroses sinyal dari inputan
5. Sensor level air berfungsi sebagai mengetahui level air yang ada apakah memenuhi syarat atau tidak.

6. LCD 16x2 adalah sebuah media tampilan yang nantinya akan menampilkan data Suhu secara digital dan inputn
7. Keypad berfungsi memberikan inputan suhu pada pemanas.
8. Driver relay berfungsi sebagai penggerak relay
9. Pemanas berfungsi untuk memberikan outputan berupa panas pada air sesuai dengan yang di kehendaki
10. Driver motor berfungsi sebagai penggerak motor DC
11. Motor DC berfungsi sebagai penggerak yang menggerakkan pengaduk atau Mixer.

3.2.2. Cara kerja Alat

Prinsip kerja dari pengaduk permen dengan fitur pemanas pada usaha kecil menengah yang berbasis mikrokontroller AT89S51 yaitu mulanya sensor level air akan membaca level air atau kondis air dalam bejana yang akan digunakan sebagai media pemanas.selanjutnya apabila level atu kondisi air telah memenuhi syarat maka alat akan bekerja pada progress selanjutnya tetapi apabila level air tidak memenuhi syarat maka tampilan apada LCD akan memvisualisasikan atau menampilkan perintah untuk menambahkan air yang berfungsi sebagai media pemanas.level air ini memanfaatkan salah satu sifat air yaitu sebagai penghantar listrik yang dapat menghantarkan listrik sehingga listrik atau Vcc dapat terhubung dengan blok rangkaian level air yang dalamnya berisi transistor yang berfungsi sebagai switching.

Pada progress selanjutnya setelah level air memenuhi syarat maka di LCD akan memvisualisasikan atau menampilkan tulisan bahwa level air sudah cukup.selanjutnya setelah proses tersebut maka beberapa saat kemudian pada LCD akan menampilkan/memvisualisasikan perintah untuk memberikan maasukan atau inputan suhu yang di inginkan dengan perintah "SET SUHU" selanjutnya kita akan memberikan inputan atau masukan suhu yang diinginkan melalui keypad 4 x 4.setelah inputan dari keypad dimasukkan maka mikrokontroller AT89S51 akan membandingkan suhu air dalam bejana yang berfungsi sebagai media pemanas dengan suhu inputan atau masukan dari keypad 4x4.apabila suhu air dalam bejana tidak memenuhi syarat atau kurang dari suhu yang di inputkan atau di set pada keypad maka mikrokontroller AT89S51 akan menyalakan driver relay yang terhubung dengan elemen pemanas atau heater.tetapi sebloknya apbila suhu dalam air dalam bejana leih besar daripada suhu yang di inputkan oleh keypad maka maka mikrokontroller AT89S51 akan mematikan driver relay yang terhubung dengan elemen pemanas atau heater sehingga driver relay yang terhubung dengan heater pada kondisi off.

Selanjutnya apabila sensor suhu telah bekerja dan suhu telah di set atau di inputkan maka progress selanjutnya adalah memasukkan inputan timer atau pewaktu dalam satuan menit.inputan timer ini juga di masukkan atau diinputkan melalui keypad 4 X 4.dengan waktu minimal 1 menit.untuk timer

pada alat ini memfungsikan fasilitas mikrokontroler AT89S51 yang memiliki fitur timer.

Selanjutnya setelah memberikan inputan timer atau pewaktu progress selanjutnya adalah memberikan inputan kecepatan motor dc melalui keypad 4 X 4 melalui tombol up and down ,progress ini dapat dilakukan sampai waktu hasil inputan timer habis.

3.2.3.Mikrokontroller AT89S51

3.2.3.1.Mikrokontroller sebagai sistem minimum

Pada bagian ini akan dibahas tentang perancangan perangkat keras yang terdiri dari Rangkaian Minimum AT89S51, Rangkaian Keypad, Rangkaian LCD, Rangkaian sensor level air,sensor suhu. Rangkaian mikrokontroller tersebut tersusun dari komponen-komponen 3 buah kapasitor, sebuah resistor dan sebuah kristal atau resonator keramik. Rangkaian kapasitor dan kristal atau resonator keramik digunakan sebagai rangkaian pembangkit internal clock generator yang terdapat pada AT89S51. Nilai kapasitansi ditentukan sesuai dengan jenis oscilator yang digunakan, yaitu:

C1 dan C2 = 20pF – 40pF untuk kristal

C1 dan C2 = 30pF – 50pF untuk resonator keramik.

Karena dalam rancangan digunakan oscilator kristal maka harga kapasitor yang di gunakan adalah sebesar 33pF.

Mikrokontroller AT89S51 mempunyai frekwensi maksimal 12 MHz, dimana 1 siklus mesin = 12 clock. Dalam rangkaian digunakan kristal dengan harga 12 MHz, maka program akan dijalankan pada setiap langkahnya selama 1 μs. Siklus tersebut diambil berdasarkan ketentuan mikrokontroller AT89S51 yaitu 12 clock = 1 siklus mesin, sedangkan frekwensi yang digunakan 12 MHz, maka waktu yang dipakai dalam setiap 1 siklus mesin adalah 1μs. Dengan demikian perhitungannya dapat dilihat sebagai berikut:

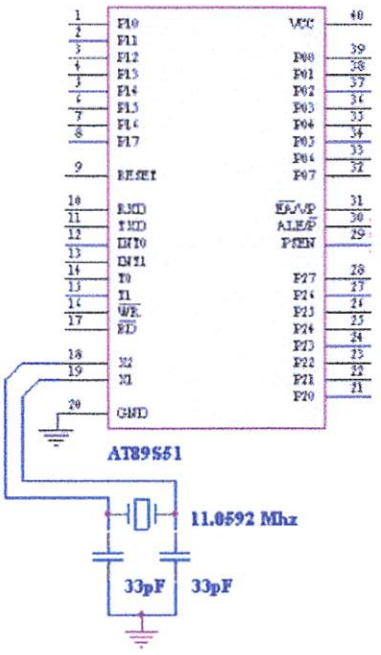
$f = 12$ MHz $\qquad T = \frac{1}{f} \qquad T = \frac{1}{12 \times 10^6}$

Karena 1 siklus mesin = 12T maka,

1 siklus mesin = $12 \text{ x } \frac{1}{12 \times 10^6} = 1$ μs.

3.2.3.2. Perencanaan Port-Port Pada Mikrokontoller AT89S51

Pada skripsi ini IC mikrokontroller AT89S51 digunakan sebagai pusat pengendali kerja dari alat yang dibuat karena pada IC inilah akan disimpan program-program *(software)* perintah serta alamat yang akan dituju program. Untuk melaksanakan fungsi tersebut diatas maka perlu dirancang port-port I/O serta sinyal-sinyal yang akan digunakan dengan seksama.



Gambar 3.2. Rangkaian Minimum Sistem Mikrokontroller AT89S51

Untuk fungsi masing-masing port pada AT89S51 yang digunakan penjelasannya sebagai berikut:

- **Port 0**

Port 0 merupakan port dua fungsi yang berada pada pin 32-39 dari IC AT89S51. Dalam perancangan, P0.0-P0.7 digunakan sebagai port keluaran ke LCD.

- **Port 1**

Port 1 disediakan sebagai port I/O dan menempati pin 1-8, dalam perancangan dengan fungsi sbb:

-.PORT 1.1 start adc

-.PORT 1.0 PWM driver

-.PORT 1.2 level air

-.PORT 1.3 driver heater

- **Port 2**

Port 2 disediakan sebagai I/O dan menempati pin 21-28. Dalam perancangan alat pin 21-28 digunakan sebagai input dari keypad 4x4.

- **Port 3**

Port 3 merupakan port dua fungsi, yaitu sebagai I/O. Port ini terletak pada pin 10-17. Dalam perancangan alat ini port tersebut terhubung dengan adc 0804 yang terubung Output dari sensor LM35 melalui rangkaian op amp.

- $\overline{PSEN}$ ***(Program Strore Enable)***

$\overline{PSEN}$ adalah suatu sinyal keluaran yang terdapat pada pin 29. Fungsinya adalah sebagai sinyal kontrol untuk memungkinkan mikrokontroller membaca program (code) dari memori eksternal. Jika eksekusi program dari ROM internal (8051/8052) atau dari flash memori AT89S51 , maka $\overline{PSEN}$ berada pada kondisi tidak aktif (high)

- **ALE *(Address Latch Enable)***

Sinyal output ALE yang berada pada pin 30 fungsinya untuk demultipleks bus alamat dan bus data. Sinyal ALE membangkitkan pulsa sebesar 1/6 frekwensi oscilator dan dapat dipakai sebagai clock yang dipergunakan secara umum.

- $\overline{EA}$ ***(External Access)***

Masukan sinyal $\overline{EA}$ terdapat pada pin 31 yang dapat diberikan logika rendah (pin terhubung ground) atau logika tinggi (pin terhubung Vcc). Jika $\overline{EA}$ diberikan logika tinggi, maka mikrokontroller akan mengakses program dari ROM internal (EPROM/flash memory). Jika $\overline{EA}$ diberikan logika rendah, maka mikrokontroller akan mengakses program dari memori eksternal. Pada skripsi ini $\overline{EA}$ dihubungkan ke Vcc.

- **RST** ***(Reset)***

Input reset pada pin 9 adalah reset master untuk AT89S51.

- **Oscilator**

Oscilator yang disediakan pada chip dikemudikan dengan XTAL yang dihubungkan pada pin 18 dan pin 19. Besar nilai XTAL yang digunakan sebesar 12 MHz untuk keluarga MCS-51, dan diperlukan dua buah kapasitor penstabil sebesar 33pF.

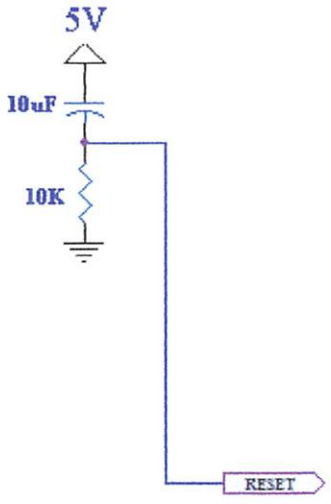
- **Vcc**

AT89S51 dioperasikan dengan tegangan supply +5V. Pin Vcc berada pada pin nomor 40 sedangkan Vss (ground) berada pada pin 20.

3.2.3.3.Rangkaian RESET

Untuk mereset Mikrokontroller AT89S51, maka pin reset di beri logika tinggi selama sekurangnya dua siklus mesin (24 periode). Untuk membangkitkan sinyal reset, kapasitor dihubungkan dengan vcc dan sebuah resistor yang

dihubungkan ke ground. Rangkaian reset ditunjukkan dalam Gambar 3.5. di bawah ini :



Gambar 3.3. Rangkaian Reset pada Mikrokontroller AT89S51

Rangkaian ini terbentuk oleh komponen R dan C yang sudah di tetapkan oleh ATMELL. Nilai R yang dipakai adalah 10kΩ dan untuk C sebesar 10μF.

$$Fo = \frac{1}{1{,}1.R.C}$$

$$Fo = \frac{1}{1{,}1.10.10^{3}.10.10^{-6}}$$

$$Fo = 9{,}09\ Hz$$

Maka periode clock : $\frac{1}{F}$

$$T = \frac{1}{9{,}09}$$

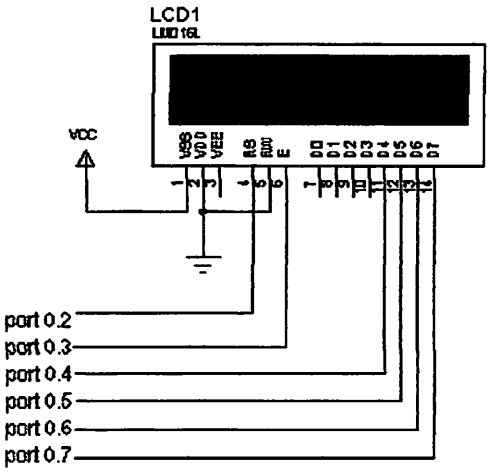
$$T = 0{,}11 \text{ detik}$$

3.2.3.4. Rangkaian LCD (Liquid Crystal Display)

Sebagai penampil data tentang menu inputa digunakan display LCD M1632 atau 2 X 16 karakter. Signal-signal yang dipergunakan oleh LCD adalah data bus, RS, R/W dan E. Signal E dihubungkan ke port 0.3 untuk mengaktifkan LCD. LCD akan aktif jika mikrokontroller memberi intruksi tulis pada alamat LCD. Sedang port 0.2 diberikan untuk memberikan signal RS yang membedakan data yang diberikan pada LCD. Signal RS diberikan pada LCD untuk membedakan signal antara instruksi program atau instruksi penulisan data.

Untuk pin R/W akan berlogika low (0) apabila dihubungkan dengan ground maka LCD difungsikan hanya untuk menuliskan program atau data ke display. Untuk mengambil data dari mikrokontroller maka pin-pin data dihubungkan dengan port 0.0 sampai 0.7 yang merupakan pin-pin data dari mikrokontroller.

LCD yang digunakan adalah LCD M1632 atau 16X2 Karakter. Adapun hubungan rangkaian LCD terhadap Controller (MCU) adalah sebagai berikut :



Gambar 3.4 Rangkaian LCD

Sumber : Perancangan

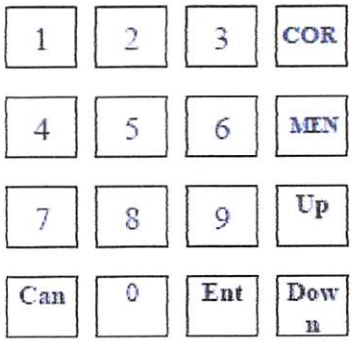
Potensio 10K pada rangakain LCD diatas merupakan pembagi tegangan yang dihubungkan ke pin VEE LCD. Pin ini berfungsi untuk mengatur kontras LCD sesuai keinginan. Untuk pin WR digorundkan karena sifatnya hanya menulis dari MCU ke LCD

3.2.3.5. Rangkaian Keypad

Pembuatan keypad, disini dimaksudkan untuk memberikan inputan dari konsumen. Scanning keypad yang dilakukan oleh Mikrokontroller AT89S51 harus mampu menentukan posisi dari tombol yang ditekan. Setelah posisi keypad yang aktif dapat ditemukan maka data tersebut diolah menjadi data tombol yang ditekan. Dalam aplikasi ini digunakan satu macam scanning yang digunakan untuk mendeteksi keypad 4x4. gambar 3.6 menunjukkan flowchart scanning keypad matriks yang digunakan dalam program. Scanning keypad ini

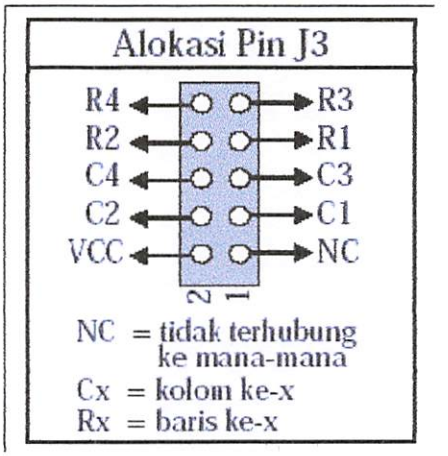
menggunakan metode polling. Yaitu scan terus menerus hingga ada tombol yang ditekan.

Keypad yang digunakan dalam aplikasi ini adalah keypad matriks 4x4 (4 baris dan 4 kolom). Berisikan angka 0 sampai 9. dan 6 tombol tyang tersisa dimanfaatkan untuk CAN,COR, ENT, MEN, UP, dan DOWN sedangkan 1 tombol lagi tidak dipakai. Untuk mengenali bagian kolom dan baris yang aktif maka keypad ini dihubungkan dengan minimum system AT89S51. kemudian dibuat program yang dapat mengenali tombol yang sedang ditekan. Program yang dibuat harus mampu mengenali setiap tombol yang ditekan sesuai perencanaan. Dan berikut merupakan bagian bagian dari keypad tersebut.



Gambar 3.5. Susunan tombol pada keypad

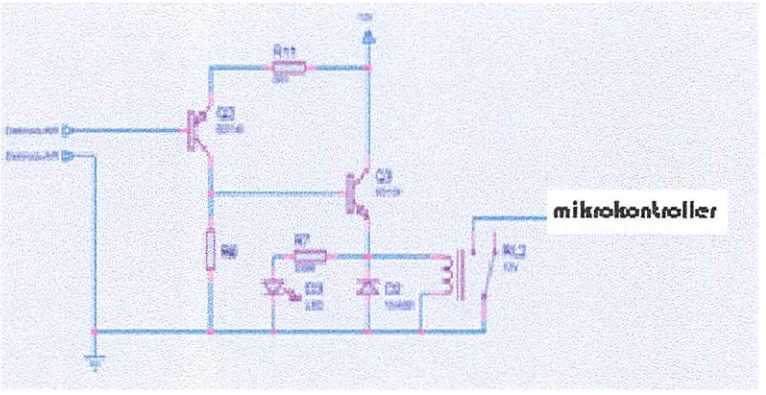
Berikut ini merupakan Gambar 3.6. alokasi pin pin output pada module keypad 4x4 beserta schematicnya tersebut.



Gambar 3.6. Alokasi Pin Pin Pada Keypad

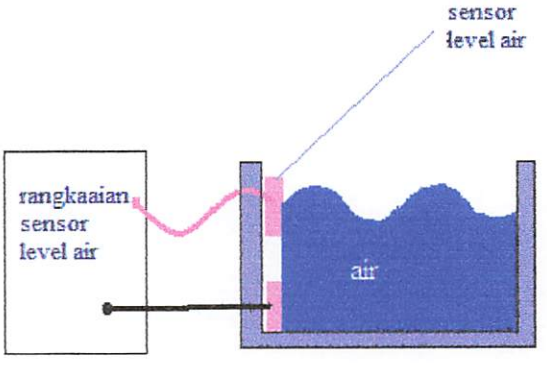
3.2.3.6. Sensor air

Pada sensor air ini sensor digunakan untuk melihat kondisi level air yang ada dalam bejana apakah memenuhi syarat atau tidak.karena dalam sekripsi ini ketersediaan air sangat berpengaruh pada kualitas hasil produk yang akan dibuat karenaair tersebut dalam proses produksi digunakan sebagai media pemanas dan untuk menghindari kerusakan elemen pada heater air yang sangat bergantung pada kondisi air.prinsip kerja dari sensor ini menggunakan sifat air yang dapat digunakan sebagai penghantar listrik.

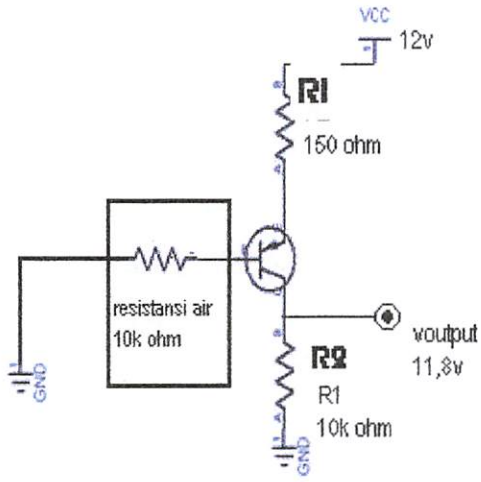


Gambar 3.7. Rangkaian sensor level air

Cara kerja sensor air ini adalah pada saat elektroda tersentuh air maka resistansi yang terdapat pada air terukur 10k ohm .karena resistansi dari elektroda tersebut diinputkan ke basis Q1 (PNP) maka akan terjadi aliran arus Ib menuju ground.



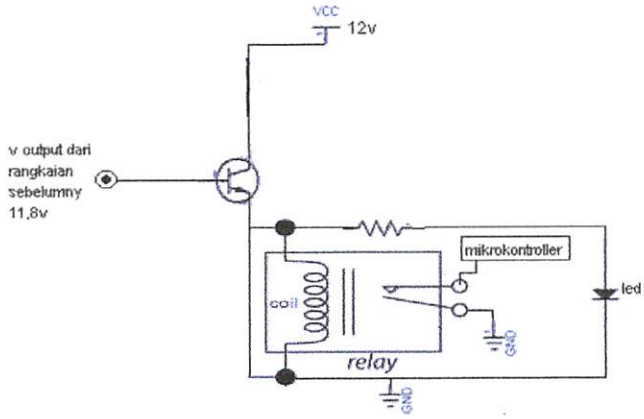
Gambar 3.8. Peletakan sensor air



Gambar 3. 9. Rangkaian PNP

Arus Ib ini akan mengalir dari R1menuju emitor Q1 kemudian melewati basis dan menuju ground melalui elektroda (dalam hal ini nilai Q1 nilainya minus (-))

Konisi tersebut akan menyebabkan transistor Q1 berada pada daerah aktif dan Ic mengalir dari emitor menuju colector Q1 sehingga pada titik colector nilainya positif.

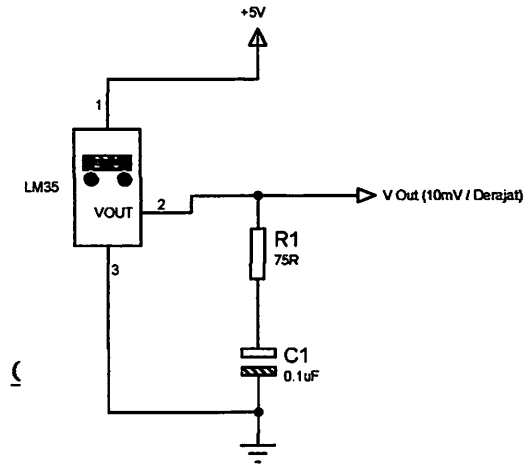


Gambar 3. 10. Rangkaian NPN ke 2

Dengan demikian maka arus Ic Q1 akan memicu transistor Q2 sehingga menyebabkan Q2 (NPN) berada pada daerah saturasi dan relay menjadi aktif hal ini dapat dilihat dari nyala led yang menandakan relay aktif.selanjutnya outputan relay selanjutnya dihubungkan dengan mikrokontroler.

3.2.3.7. Sensor Suhu LM35

Pada perancanan alat ini, Sensor suhu yang digunakan adalah LM35, dimana sensor ini mempunyai keluaran tegangan linear 10mV/derajat Celcius. Adapun rangkaian sensor Suhu LM35 adalah sebagai berikut :



Gambar 3. 11. Sensor LM35

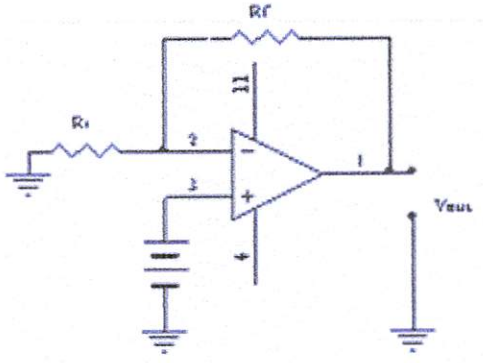
Nilai R1 dan C1 ditentukan berdasarkan datasheet LM35. dimana fungsi R dan C digunakan untuk menghilangkan gangguan elektromaghnetis yang dapat ditimbulkan oleh frekwensi pemancar, frekwensi Listrik ataupun gangguan luar lainnya. Sensor Suhu LM 35 terdapat 1 buah pada perancangan alat ini, sensor

tersebut berada dalam bejana yag memanaskan air .jika air dipanaskan oleh heater maka akan timbul perbedaan suhu pada sensor tersebut.

3.2.3.8. Penguat Tak Membalik (Non-inverting Amplifier)

Pengkondisi sinyal berfungsi untuk menguatkan tegangan keluaran sensor suhu LM35 agar mampu diproses pada peralatan selanjutnya dalam hal ini oleh ADC 0804.dan selanjutnya akan diproses oleh mikrokontroller AT89s51 untuk mengkondisikan status heater atau pemanas pada air

Diinginkan bahwa pengukuran suhu dapat dilakukan pada range 25°C - 100°C, sedangkan saat suhu kamar LM35 sudah mengeluarkan tegangan sebesar 0,3V, sehingga untuk dapat mengatur agar masukan ADC sebesar 0V pada suhu ruang,Penguat tak membalik merupakan suatu penguat dimana tegangan keluarannya atau Vo mempunyai polaritas yang sama dengan tegangan masukan atau Vi. Rangkaian penguat tak membalik ditunjukkan pada Gambar 2.



Gambar 3.12. Penguat tak membalik

Arus i mengalir ke Ri karena impedansi masukan op - amp sangat besar sehingga tidak ada arus yang mengalir pada kedua terminal masukannya. Tegangan pada Ri sama dengan Vi karena perbedaan tegangan pada kedua terminal masukannya mendekati 0 V.

$$i = \frac{Vi}{Ri} \qquad (2.5)$$

Tegangan pada R_f dapat dinyatakan sebagai

$$V_{Rf} = I\,R_f = \frac{Rf}{Ri} x Vi \qquad (2.6)$$

Tegangan keluaran Vo didapat dengan menambahkan tegangan pada Ri yaitu Vi dengan tegangan pada Rf yaitu V_{Rf}.

$$Vo = Vi + \frac{Rf}{Ri} x\ Vi \qquad (2.7)$$

$$\frac{Vo}{Vi} = \left(1 + \frac{Rf}{Ri}\right) \qquad (2.8)$$

$$\Delta v = \frac{vo}{vi}$$

$$\frac{Vo}{Vi} = \left(1 + \frac{Rf}{Ri}\right)$$

$$\Delta v = 1 + \frac{10k\Omega}{10k\Omega}$$

$$\Delta v = 2x$$

Jadi besarnya penguatan op- amp non inverting ini sebesar 2 kali.Op amp ini dirancang berdasarkan resolusi ADC sebesar 19,53 mV dan dibulatkan menjadi 20mV.hal ini dikarenakan karena karakteristik LM35 yang memiliki karakteristik tegangannya akan naik 10mV/derajat Celcius.sehingga untuk memenuhi resolusi ADC sebesat 20mV maka diperlukan penguatan sebesar 2 kali.

3.2.3.9. Analog to Digital Converter (ADC 0804)

Perancangan untuk rangkaian adc pada alat ini digunakan mode free running. Mode ini dipilih karena waktu konversi adc jauh lebih cepat terhadap tingkat perubahan suhu dari plant, sehingga setiap kali suhu berubah, adc selalu telah selesai melakukan konversi data sehingga data sudah valid untuk dicuplik.

Untuk ADC 0804 dengan jumlah bit sebesar 8 bit dan Vref = 5V maka resolusinya :

$$(\Delta V) = 5 \times (2^{-8}+1) = 19{,}53\text{mV}.$$

Masukan tegangan analog adc yang berasal dari keluaran pengkondisi sinyal saat full scale dengan nilai sebesar Vx dapat dihitung sebagai berikut:

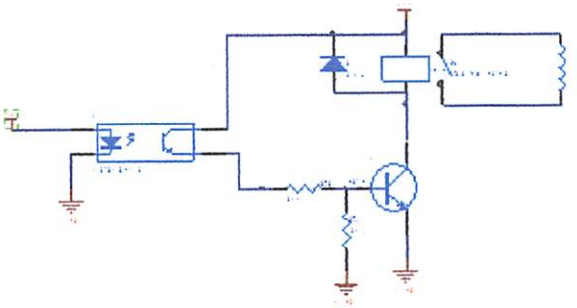
$$Vx = 5\left(\frac{1}{2^1}+\frac{1}{2^2}+\frac{1}{2^3}+\frac{1}{2^4}+\frac{1}{2^5}+\frac{1}{2^6}+\frac{1}{2^7}+\frac{1}{2^8}\right)$$
$$= 5\frac{255}{256} = 4{,}9804 \ v$$

dengan demikian saat tegangan masukan adc 4,9804 keluaran adc akan bernilai FFH.

3.2.3.10. Driver relay

Dalam pembuatan alat ini driver relay berfungsi sebagai penerjemah perintah dari mikrokontoller untuk menjalankan heater pemanas air dalam bejana apabila suhu dari air tidak memenuhi syarat dan mematikan heater pemanas air

bila suhu lebih dari yang diinginkan.berikut gambar rangkaian driver relay pada gambar 3.19 :



Gambar 3.13. Rangkaian driver relay

Jika led pada optocoupler dinyalakan.maka cahaya ari le akan memicu transistor pada optocoupler dan menyebabkan arus mengalir dari collector ke emitor (transistor pada optocoupler tersebut) .

Dengan demikian keluran emitor optocoupler akan memicu basis transistor Q1 dan menyebabkan transistor tersebut pada kondisi saturasi sehingga menyebabkan relay aktif.

Alasan pengunaan IC optocoupler ini adalah untuk pengisolasian rangkaian kontrol dengan beban supaya tidak terjadi gangguan (arus bocor dari beban dan hentakan pada saat on) pada saat sistem bekerja.

bila suhu lebih dari yang diinginkan.berikut gambar rangkaian driver relay pada gambar 3.19 :

Gambar 3.13. Rangkaian driver relay

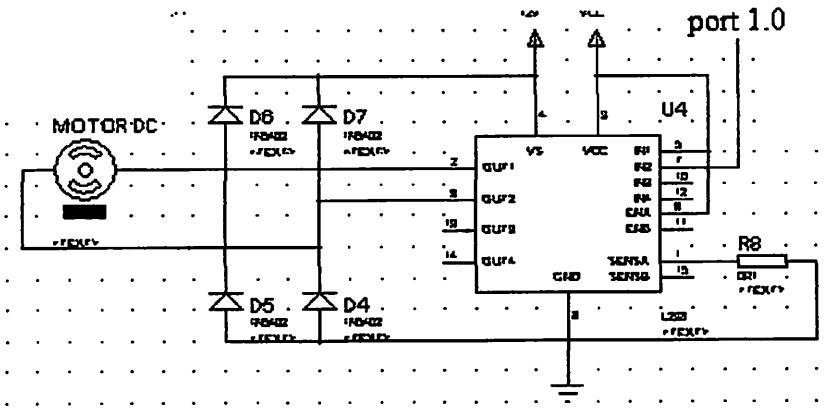
Jika led pada optocoupler dinyalakan,maka cahaya ari le akan menuju transistor pada optocoupler dan menyebabkan arus mengalir dari collector ke emitor (transistor pada optocoupler tersebut).

Dengan demikian keluran emitor optocoupler akan menuju basis transistor Q1 dan menyebabkan transistor tersebut pada kondisi saturasi sehingga menyebabkan relay aktif.

Alasan penggunaan IC optocoupler ini adalah untuk pengisolasian rangkaian kontrol dengan beban supaya tidak terjadi gangguan (arus bocor dari beban dan hentakan pada saat on) pada saat sistem bekerja.

3.2.3.11. Perancangan Driver Motor DC

Dalam pembuatan alat ini driver motor berfungsi sebagai penggerak motor sesuai dengan perintah mikrokontroller AT89S51. Dalam perancangan ini, driver L298 N yang digunakan untuk menggerakkan motor $12V_{DC}$ dengan memberi inputan logika " 1 "(high) atau" 0 "(Low).Agar timbul beda potensial, input harus berlogika " 1 " dan " 0 ",sedangkan Enable harus selalu berlogika " 1 " (High).



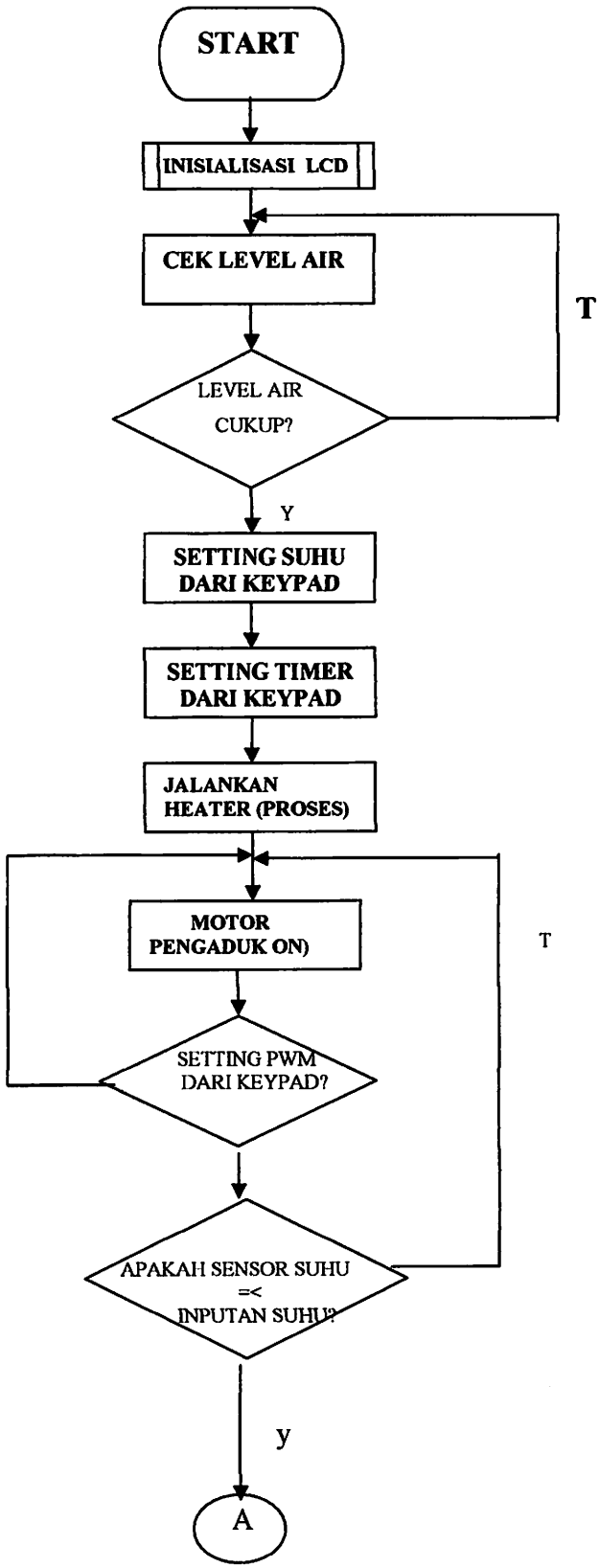
.Gambar 3.14 driver motor dc

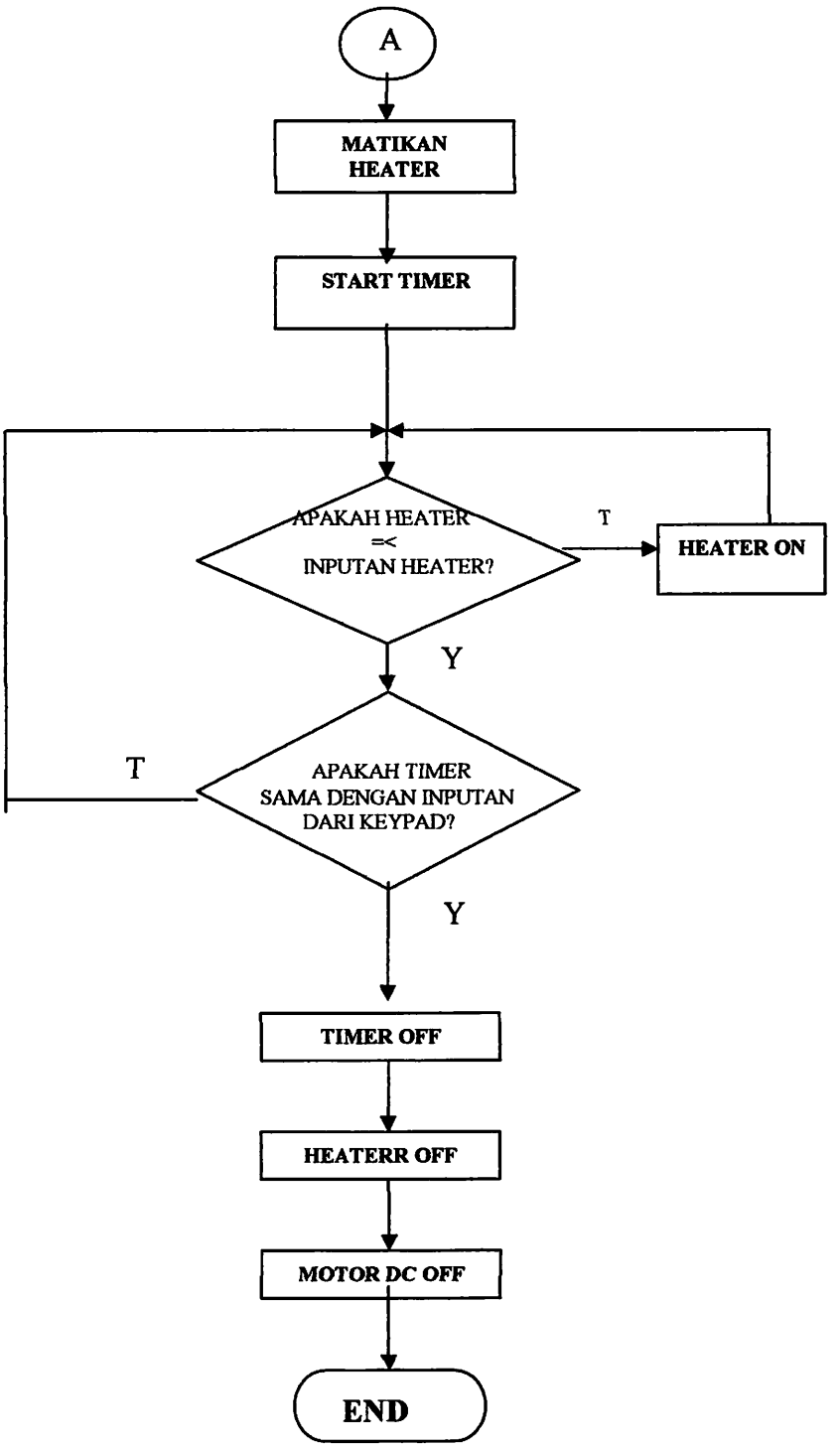
3.3. Perangkat Lunak Mikrokontroler

Untuk mendukung agar perangkat keras berfungsi sesuai dengan perencanaan, maka diperlukan perangkat lunak sebagai penunjangnya. Untuk mengatur dan mengendalikan keseluruhan sistem perangkat keras yang telah dibuat, harus dibantu dengan perangkat lunak. Sistem aplikasi Mikrokontroller AT89S851 ini dapat mengatur dan mengendalikan keseluruhan sistem apabila ada

urutan instruksi yang mendefenisikan secara jelas urutan tugas yang harus dikerjakannya .

Urutan instruksi ini sangat penting untuk didefenisikan, karena Mikrokontroller bekerja secara pasti berdasarkan urutan insruksi ini. Susunan logika perancangan yang salah tidak dapat diketahui oleh Mikrokontroller. Selama instruksi yang diterima sesuai dengan aturannya, Mikrokontroller tetap mengerjakan instruksi tersebut. Kesalahan seperti ini baru diketahui ketika kerja sistem aplikasi tidak sesuai dengan spesifikasi awal. Oleh karena itu, perancangan perangkat keras sangat menentukan dalam keberhasilan pembuatan perangkat lunak, sama pentingnya dengan perancangan perangkat keras. Sebuah Mikrokontroller tidak akan bekerja bila tidak diberikan program. Program tersebut memberitahukan apa yang harus dilakukan oleh Mikrokontroller.


START
INISIALISASI LCD
CEK LEVEL AIR
T
LEVEL AIR CUKUP?
Y
SETTING SUHU DARI KEYPAD
SETTING TIMER DARI KEYPAD
JALANKAN HEATER (PROSES)
MOTOR PENGADUK ON)
T
SETTING PWM DARI KEYPAD?
APAKAH SENSOR SUHU =< INPUTAN SUHU?
y
A

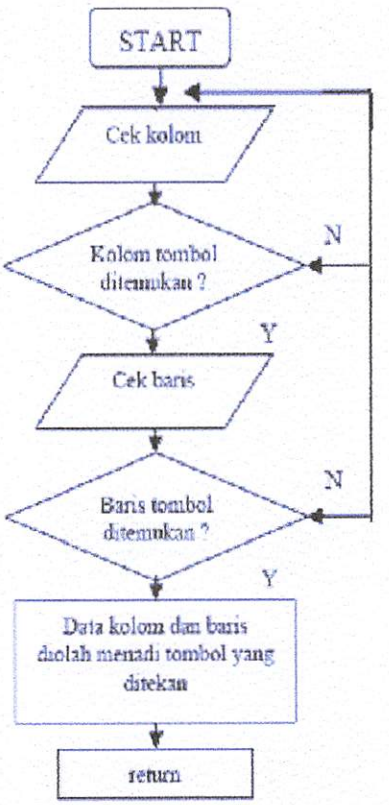


Gambar 3.15 .Diagram Alir Proses Jalannya Sistem

Diagram flowchart program utama yang disusun dengan menggunakan bahasa bascom suatu program yang dapat menerjemahkan bahasa basic ke pogram bahasa mesin yang mengandung kode-kode biner yang merupakan instruksi-instruksi yang mudah dipahami oleh prosesor seperti pada gambar 3.21 dapat dijelaskan sebagai berikut:

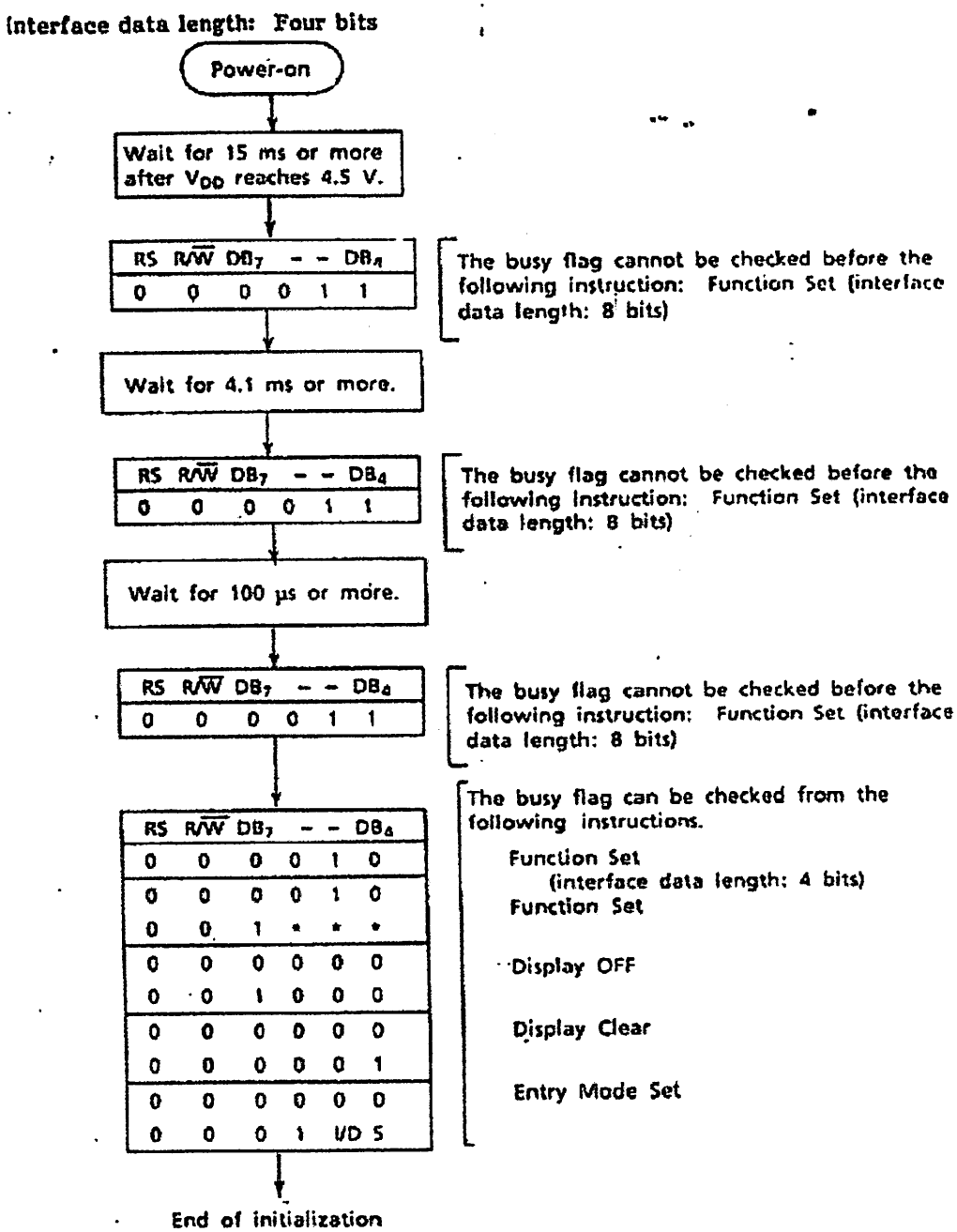
1. Start
2. Inisialisasi port yang digunakan pada mikrokontroller
3. Inisialisasi LCD
4. Mengecek kondisi level air
5. Menunggu sampai level air memenuhi syarat
6. Memasukkan inputan suhu dengan keypad
7. Memasukkan inputan timer pada keypad
8. Membandingkan suhu inputan dari keypad dengan sensor suhu
9. Motor pengaduk kondisi on
10. Setting PWM dengan keypad
11. Jika suhu inputan dari keypad sama dengan sensor suhu matikan heater
12. Start timer
13. Membandingkan lagi suhu inputan dari keypad dengan sensor suhu
14. jika "tidak"heater on
15. Membandingkan timer inputan dari keypad dengan timer
16. jika sama dengan timer maka timer akan off
17. jika timer telah off maka heater akan off
18. jika heater telah off motor akan off
19. Selesai

Flowchart scanning keypad



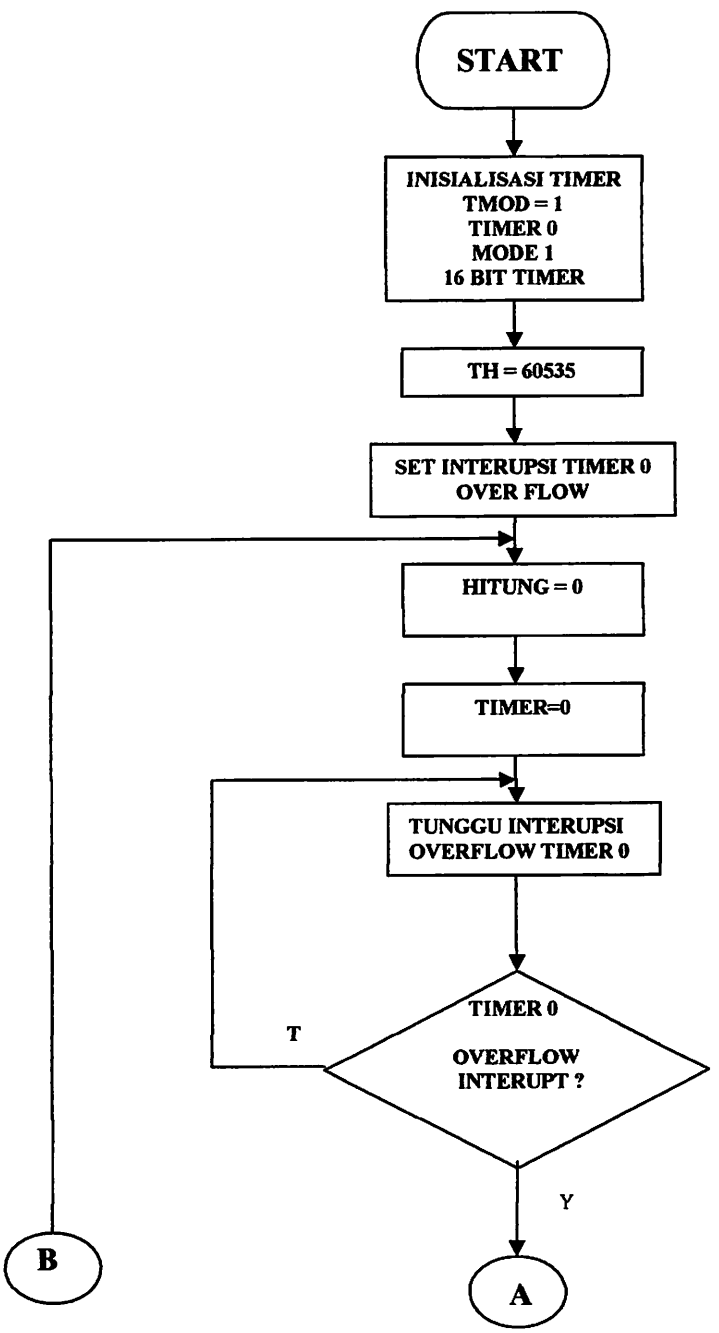
Gambar 3.16. Flowchart scanning keypad dengan metode polling

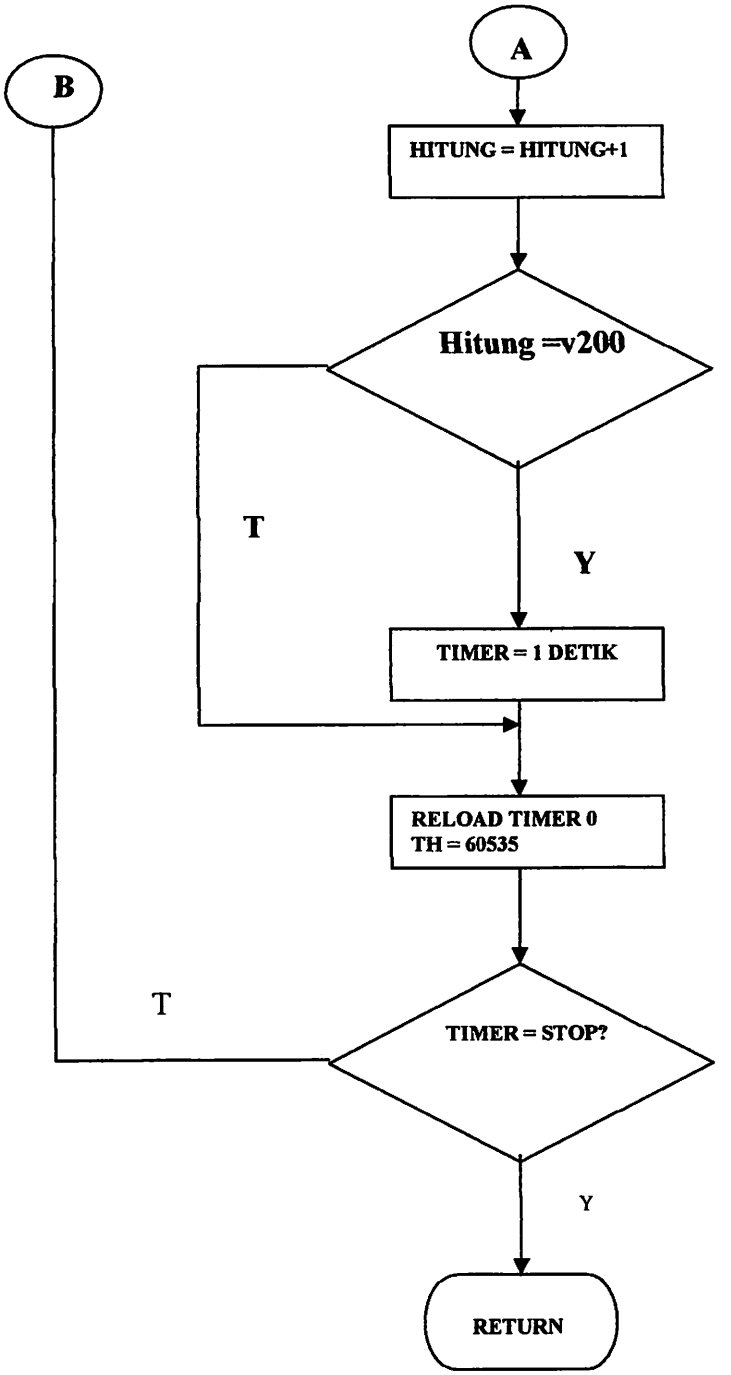
Flowchart inisialisasi LCD



Gambar 3.17 .Diagram Alir Proses inisialisasi LCD

Gambar flowchart timer





Gambar 3.18. Flowchart timer

BAB IV

PENGUJIAN ALAT DAN PEMBAHASAN HASIL

Pada bab ini membahas tentang pengukuran dan pengujian alat yang dirancang, dimana meliputi perangkat keras (hardware) dan perangkat lunak (software). Untuk mengetahui sistem yang dirancang sesuai dengan fungsi yang diharapkan, dilakukan pengujian terhadap sistem aplikasi tersebut baik secara keseluruhan atau subsistem. Berikut penjelasan mengenai prosedur pengukuran dan dan data hasil pengujian.

4.1. Pengujian rangkaian sensor air.

4.1.1. Tujuan

Bertujuan untuk mengetahui berapa besar tegangan yang dikeluarkan sensor, serta untuk mengetahui apakah tegangan yang dihasilkan sensor dalam keadaan *high* atau *low*.

4.1.2. Peralatan yang digunakan

- Multimeter digital
- Rangkaian sensor
- Catu daya 5 volt DC
- Kamera digital

4.1.3. Langkah-langkah Pengujian

1) Merangkai rangkaian driver seperti pada gambar dibawah ini:

BAB IV

PENGUJIAN ALAT DAN PEMBAHASAN HASIL

Pada bab ini membahas tentang pengukuran dan pengujian alat yang dirancang, dimana meliputi perangkat keras (hardware) dan perangkat lunak (software). Untuk mengetahui sistem yang dirancang sesuai dengan fungsi yang dilarapkan, dilakukan pengujian terhadap sistem aplikasi tersebut baik secara keseluruhan atau subsistem. Berikut penjelasan mengenai prosedur pengukuran dan dan data hasil pengujian.

4.1. Pengujian rangkaian sensor air.

4.1.1. Tujuan

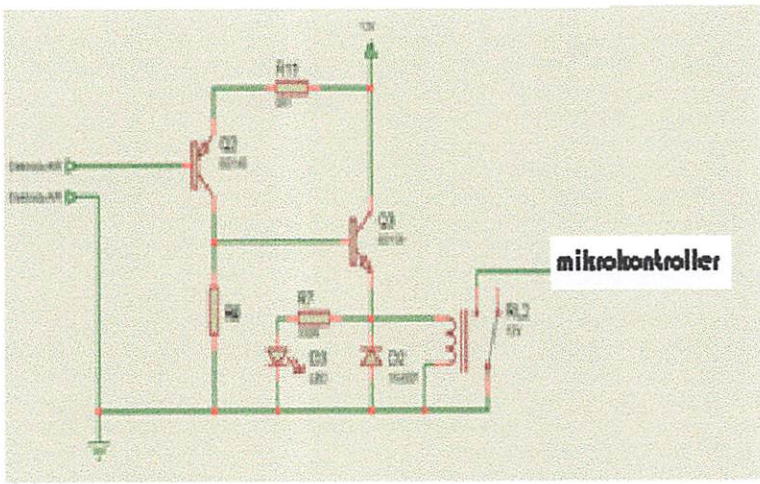
Berfujuan untuk mengetahui berapa besar tegangan yang dikeluarkan sensor, serta untuk mengetahui apakah tegangan yang dihasilkan sensor dalam keadaan hidup atau mati.

4.1.2. Peralatan yang digunakan

- Multimeter digital
- Rangkaian sensor
- Catu daya 5 volt DC
- Kamera digital

4.1.3. Langkah-langkah Pengujian

1) Menyiapkan rangkaian driver seperti pada gambar dibawah ini.



Gambar 4.1. Rangkaian sensor

2) Memberikan catu daya sebesar 5V pada sensor.
3) Mengukur tegangan yang dikeluarkan oleh sensor.
4) Memberikan inputan air dlm bejana yang telah terhubung dengan sensor
5) Mengukur kembali besar tegangan yang dikeluarkan oleh sensor.
6) Mencatat tegangan yang dihasilkan sensor dan di tabelkan.

4.1.4. Hasil Pengujian

Dari hasil pengujian Sensor air didapatkan didapat data sebagaimana tabel berikut:

Tabel 4.2 Tabel pengujian sensor air

Gambar 4.1. Rangkaian sensor

2) Memberikan catu daya sebesar 5 V pada sensor.
3) Mengukur tegangan yang dikeluarkan oleh sensor.
4) Memberikan inputan air dlm gelas yang telah terhubung dengan sensor
5) Mengukur kembali besar tegangan yang dikeluarkan oleh sensor.
6) Mencatat tegangan yang ditunjukkan sensor dan di tabelkan.

4.1.4. Hasil Pengujian

Dari hasil pengujian Sensor air didapatkan didapat data sebagaimana tabel berikut:

Tabel 4.2 Tabel pengujian sensor air

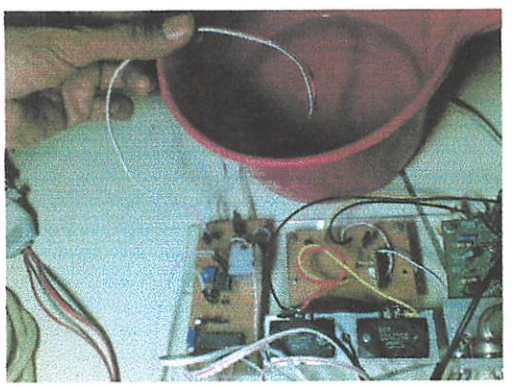
Tabel 4.1. Hasil pengujian sensor air

Pengujian	Tegangan yang dikeluarkan	
	Tanpa air	Dengan air
Pengujian ke 1	5,2v	0v
Pengujian ke 2	5,3v	0v
Pengujian ke 3	5,3v	0v
Pengujian ke 4	5,2v	0v
Pengujian ke 5	5,3v	0v

Sumber: pengukuran

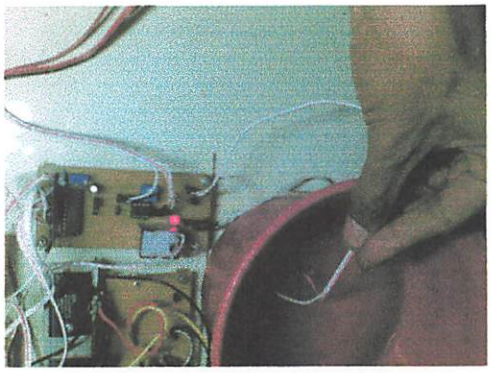
Gambar hasil pengujian:

1.saat kondisi tidak ada air



Gambar 4.2 Saat kondisi tidak ada air

2.kondisi saat ada air



Gambar 4.3 Saat kondisi ada air

4.1.5. Analisa

Dari hasil percobaan diatas maka dapat dilihat bahwa sensor air telah bekerja pada kondisi saat air ada dan pada kondisi saat tanpa air dalam bejana pemanas.

4.2. Pengukuran Sensor Suhu

4.2.1. Tujuan Pengukuran

1. Mengetahui nilai tegangan terhadap suhu yang terbaca.
2. Mengetahui perbandingan hasil pengukuran dengan datasheet.

4.2.2. Peralatan yang digunakan

1 Power Supply

2 Multimeter analog / digital

3 Sensor Suhu LM35

4 Termometer ruangan

4.2.3. Langkah-langkah pengukuran

1. Hubungkan Power Suplay 5V pada sensor LM35.
2. Hubungkan VoltMeter pada Output Sensor LM35
3. Baca Suhu menggunakan Termometer pembanding dan amati nilai tegangan terhadap Suhu terbaca saat tersebut

4.2.4. Pengujian Sensor LM35

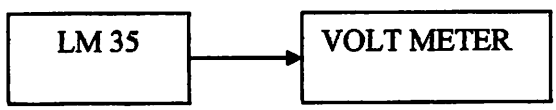


Diagram Pengukuran
Sumber: Pengujian

Untuk mengetahui nilai suhu yang terbaca pada saat pengujian, maka pada pengujian ini juga menggunakan termometer ruangan sebagai referensi suhu sekitar, **Gambar 4.4** dimana sensor termometer ruangan digandengkan dengan sensor LM35 agar suhu yang terbaca juga ikut terbaca oleh kedua sensor. Pada saat pengujian, suhu awal yang terbaca adalah 25° C dan untuk menaikkan suhu maka kedua sensor tersebut dipanasi dengan cara didekatkan pada solder hingga suhu sesuai keinginan kita saat pengukuran.

4.2.5. Hasil Pengukuran

Dari hasil pengujian Sensor suhu didapatkan didapat data sebagaimana tabel berikut:

Tabel 4.2 Tabel pengujian sensor suhu

Suhu Sensor	Output LM35 (V) Pada VoltMeter
25° C	251 mV
26° C	260 mV
27° C	273 mV
28° C	281 mV
29° C	291 mV
30° C	302 mV
31° C	314 mV
32° C	323 mV

Sumber: pengukuran

4.2.6. Analisa

Pada tabel pengujian diatas, diketahui hasil pengukuran output LM35 tidak sesuai dengan ketentuan yang tercantum pada datasheet, dimana pada datasheet nilai tegangan keluaran sensor suhu LM35 adalah linear dan mempunyai resolusi 10mV/ derajat Celcius, namun tidak menutup kemungkinan karena kepekaan pengukuran LM35 yang linear dan selain itu LM35 mempunyai tingkat akurasi data sebesar 0,5 %. Dengan demikian error dapat dihitung sebagai berikut :

$$\text{Error} = \frac{Hasil\_Ukur - Hasil\_Teori}{Hasil\_teori} \text{X100 \%}$$

Dari hasil analisa error pengukuran terhadap teory didapat data sebagaimana tabel 4.3 berikut:

Tabel 4.3 Tabel Error pengujian Rangkaian Pengkondisi

Suhu Sensor	Output pengukuran LM35	Hasil Teori	Error
25° C	251 mV	250 mV	0,004 %
26° C	260 mV	260 mV	0 %
27° C	273 mV	270 mV	0,011 %
28° C	281 mV	280 mV	0,003 %
29° C	291 mV	290 mV	0,003 %
30° C	302 mV	300 mV	0,006 %
31° C	311 mV	310 mV	0,003 %
32° C	321 mV	320 mV	0,003 %

Sumber: pengukuran

4.3. Pengujian Rangkaian Pengkondisi Sinyal

4.3.1. Tujuan Pengukuran

1 Mengetahui nilai penguatan tegangan input terhadap tegangan keluaran rangkaian pengondisi sinyal.

2 Mengetahui perbandingan hasil pengukuran dengan perencanaan

4.3.2. Peralatan Yang digunakan

1 Power Supply

2 Multimeter analog / digital

3 Oscilloscop

4 Rangkaian pengondisi sinyal

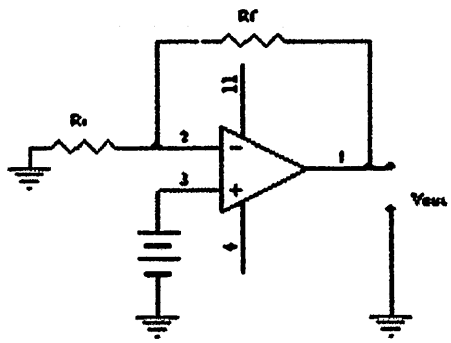
4.3.3. Langkah-langkah pengukuran:

1 Input rangkaian pengkondisi sinyal dihubungkan ke LM35

2 Voltmeter digital dihubungkan dengan output ADC

3 Baca data Voltmeter

4 Rangkaian Pengkondisi Sinyal dirangkai sebagaimana rangkaian berikut :



Gambar 4.5 rangkaian op amp

4.3.4. Hasil Pengukuran

Dari hasil pengukuran rangkaian Pengkondisi Sinyal didapatkan hasil pada tabel 4.4 sebagaimana berikut:

Tabel 4.4 Tabel pengujian Rangkaian Pengkondisi Sinyal

Pengujian ke	Vin pengukuran	V out pengukuran
1	0,29 V	0,57 V
2	0,30 V	0,59 V
3	0,32 V	0,63 V
4	0,34 V	0,67 V
5	0,35 V	0,69 V
6	0,37 V	0,73 V
7	0,39 V	0,77 V

Sumber: pengukuran

4.3.5. Analisa

Output opamp pada rangkaian pengkondisi sinyal berdasarkan hitungan teori adalah sebagai berikut :

$$\Delta v = \frac{vo}{vi}$$

$$\frac{Vo}{Vi} = \left(1 + \frac{Rf}{Ri}\right)$$

$$\Delta v = 1 + \frac{10k\Omega}{10k\Omega}$$

$$\Delta v = 2x$$

Dari hasil pengukuran Output terhadap input pada rangkaian Op-Amp mempunyai penguatan tegangan 2 kali. Namun jika dilihat pada hasil pengukuran menunjukkan adanya selisih tegangan pada penguatan Op-amp antara Teori dan Hasil ukur. Toleransi error pada pengukuran diatas dirumuskan sebagai berikut :

$$\text{Error} = \frac{Hasil\_Ukur - Hasil\_Teori}{Hasil\_teori} \text{X100 \%}$$

Dengan demikian hasil analisa pengukuran ditunjukkan sebagaimana tabel 4.5 berikut:

Tabel 4.5 Tabel Analisa pengujian Rangkaian Pengkondisi Sinyal

No.	Vin OpAmp (V)	Hasil pengujian Output Pengkondisi Sinyal (V)	Hasil Teori	Error
1	0,29 V	0,57 V	0,58	1,724%
2	0,30 V	0,59 V	0,60	1,666%
3	0,32 V	0,63V	0,64	1,562%
4	0,34 V	0,67 V	0,68	1,470%
5	0,35 V	0,69 V	0,70	1,428%
6	0,37 V	0,73 V	0,74	1,351%
7	0,39 V	0,77 V	0,78	1,282%

Sumber: pengukuran

Dari tabel diatas, didapatkan rata-rata presentase error sebesar 2% hal ini disebabkan karena nilai toleransi komponen yang dipakai pada rangkaian

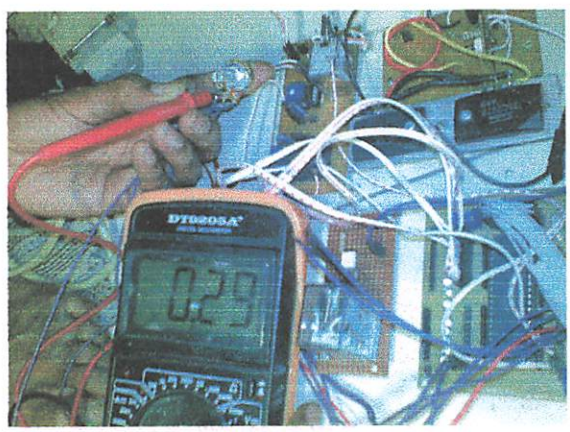
pengkondisi sinyal, dimana resistor yang digunakan mempunyai toleransi sebesar 5 %, selain itu faktor rugi-rugi dari power suplay juga amat berpengaruh, dimana Vcc pada rangkaian catu daya Op-amp yang menggunakan catu daya simetris tidak presisi pada saat diukur karena faktor komponen itu sendiri.

4.3.6. Kesimpulan

- Error yang didapat dari perbandingan hasil perhitungan dan hasil pengukuran dipengaruhi oleh toleransi dari komponen yang dipakai pada alat.
- Op-Amp mempunyai penguatan tegangan AV = 2.
- Op-Amp menguatkan sinyal inputan sehingga output pada Op-amp besarnya 2x dari hasil inputan op-amp

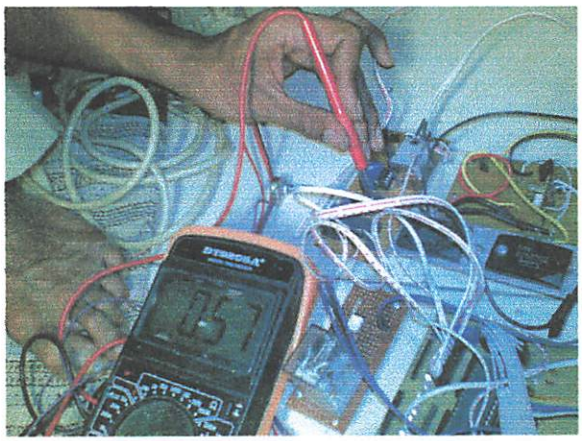
Gambar pengujian op-amp sebagai berikut:

Gambar hasil pengukuran inputan op amp:



Gambar 4.6 Pengukuran inputan op amp

Gmbar hasil pengukuran outputan op amp:



Gambar 4.7 Pengukuran outputan op amp

4.4 Pengujian Rangkaian ADC

4.4.1. Tujuan Pengukuran

Mengetahui perubahan tegangan output terhadap tegangan input.

4.4.2. Peralatan Yang digunakan

1 Power Supply

2 Multimeter analog / digital

3 Rangkaian ADC 0804

4.4.3. Langkah-langkah pengukuran:

1 Input ADC diberikan tegangan dan diatur secara linear mulai 0V s/d 5V.

2 Jalankan Program ADC

3 Amati data yang terbaca pada multimeter

Berdasarkan lembar datasheet ADC0804, resolusi ADC = 20mV dengan tegangan referensi ½ Vcc yaitu 2,5V. .

4.4.4. Hasil Pengukuran

Dari hasil pengukuran rangkaian ADC didapat hasil sebagaimana tabel 4.6 berikut :

Tabel 4.6 Tabel pengujian Rangkaian ADC

No	Vin	Vin ADC
1	0V	0
2	10 mV	20 mV
3	20 mV	40 mV
4	30 mV	60 mV
5	40 mV	80 mV
6	50 mV	100 mV

Sumber: pengukuran

4.4.5. Analisa

Dari hasil pengujian diatas, diketahui bahwa hasil keluaran data Vin terhadap tegangan input dinyatakan Valid dan sesuai spesifikasi pada datasheet ADC0804. perubahan data keluaran (biner) ADC terjadi pada saat kenaikan tegangan setiap 20mV, dimana resolusi ADC = VCC / 8bit = 5 / 255 = 20mV. Adapun rumusan untuk mencari Output ADC adalah sebagai berikut:

$$\text{Digital output} = \frac{Vin}{Vresolusi\_ADC}$$

$$= \frac{40mV}{20mV}$$

$$= 2$$

Sementara itu prosentase error yang didapat dalam pengukuran ditunjukkan pada tabel 4.5 berikut:

Tabel 4.7 Tabel analisa pengujian Rangkaian ADC

No	Vin ADC berdasarkan resolusi	Vin ADC	Error
1	0 $^{s}/_{d}$ <20mV = 00	0	0 %
2	20 mV $^{s}/_{d}$ <40mV =01	20 mV	0 %
3	40 mV $^{s}/_{d}$ <60mV =02	40 mV	0 %
4	60 mV $^{s}/_{d}$ <80mV=03	60 mV	0 %
5	80 mV $^{s}/_{d}$ <100mV=04	80 mV	0 %

Sumber: pengukuran

Gambar pengukuran ADC:

Gambar 4.8 Pengukuran ADC

Berikut ini merupakan cara yang dapat dalam pengukuran dimanfaatkan ini pada tabel 4.7 berikut:

Tabel 4.7 Tabel analisa pengujian Kumpulan ADC

No	Vin ADC Berdasarkan rencana	Vin ADC	Error
1	0 V	20mV – 0V	0	0 %
2	20 mV	40mV – 0V	20 mV	0 %
3	40 mV	60mV – 0V	40 mV	0 %
4	60 mV	80mV – 0V	60 mV	0 %
5	80 mV	100mV – 0V	80 mV	0 %

Jumlah pengukuran

Gambar pengukuran ADC

Gambar 4.8 Pengukuran ADC

4.5. Pengujian Rangkaian Driver Motor DC

4.5.1.Tujuan Pengujian

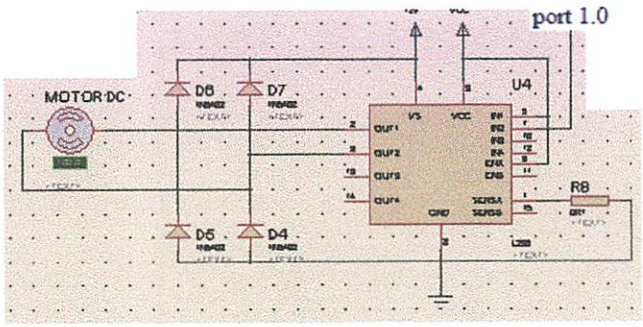
Untuk mengetahui apakah rangkaian driver Motor pada Driver Motor Pengaduk dapat bekerja sesuai dengan perencanaan

4.5.2 Peralatan yang digunakan

1. *Motor DC*
2. Mikrokontroller AT89S51
3. *Multimeter digital*
4. *Power Supply* driver Motor DC
5. *Power Supply* Motor DC

4.5.3 Langkah-langkah pengujian

1. Alat dirangkai seperti dalam Gambar 4.5 dan memberikan logika rendah pada rangkaian *ON/OFF driver Motor*
2. Mengukur nilai tegangan keluaran pada Motor.
3. Memberikan logika tinggi pada rangkaian ON/OFF driver Motor.
4. Mengukur kembali nilai tegangan keluaran pada Moto
5. Mengukur polaritas tegangan keluaran pada Motor



Gambar 4.9 Pengujian Rangkaian driver Motor DC

4.5.4 Hasil pengujian

Table 4.8.Hasil Pengujian Rangkaian Driver Motor DC

no	Kondisi level kecepatan Motor DC	V out Motor DC	Arus pada Motor DC
1	10	6,19V	0,14A
2	20	6,25V	0,14A
3	30	6,31V	0,14A
4	40	6,37V	0,14A
5	50	6,33V	0,14A

4.5.5 Analisa

Dari hasil pengkuran diatas dapat diketahui bahwa moor dapat begerak sesuai dengan yang dingikan dari hasil pengukuran pada saat kondisi motor dalam kecepatan minimum dengan beban dapat diketahui

bahwa Vout =3,51v dengan arus sebesar 0,78 A dan pada saat kecepatan maksimum Vout=5,6v dan arus sebear 2,13 A.

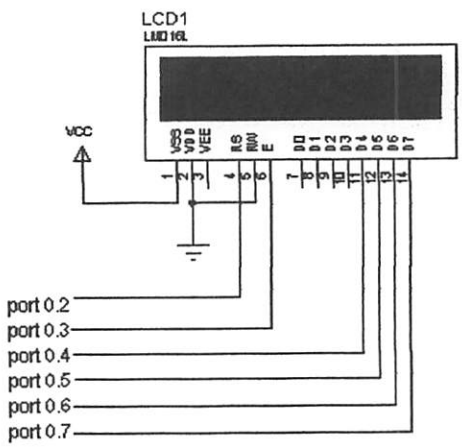
4.6. Rangkaian LCD

4.6.1. Tujuan

Tujuan dari pengujian rangkaian LCD ini adalah untuk mengetahui apakah rangkaian rangkaian display (LCD) yang dirancang dapat bekerja sesuai dengan apa yang direncanakan.

4.6.2. Peralatan yang digunakan

- Minimum sistem AT89S51
- Catu Daya sebesar 5 volt DC
- Rangkaian LCD.



Gambar 4.10. Rangkaian LCD 162A

- Tampilan LCD
- Tipe tampilan 2 Jalur 16 Digit
- Antarmuka modul 4 bit/8 bit

4.6.3. Langkah-langkah Pengujian

- Mempersiapkan *software* Mikrokontroller yang berfungsi untuk inisialisasi LCD. Sekaligus untuk menuliskan kalimat " SURYO ADI W. 05.12.201".
- Mengisi Mikrokontroller AT89S51 dengan *software* yang telah dipersiapkan di atas dengan menggunakan *downloader* AT89S51.
- Mempersiapkan rangkaian penguji seperti pada Gambar 4.2.

4.6.4. Hasil Pengujian

Setelah melakukan pengujian LCD di atas maka di dapatkan tulisan "SURYO ADI WIBOWO dan 0512201'

4.6.5.Cara pengoprasian alat

Hidupkan saklar ke posisi ON, maka akan muncul tulisan seperti gambar di bawah ini.

Gambar 4.11 tampilan lcd

4.7. Pengujian Rangkaian *Input Keypad*

4.7.1. Tujuan

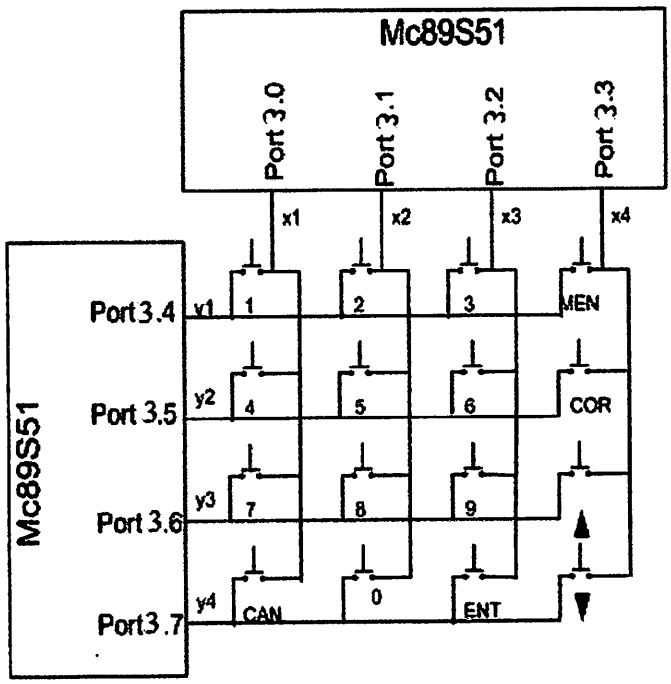
Pengujian ini bertujuan untuk mengetahui konfigurasi logika keluaran dari unit papan tombol saat tombol ditekan. . Dalam pengujian ini keluaran yang diamati adalah proses *scanning* yang terjadi pada lajur baris dan kolom. Lajur baris merupakan bagian output sedangkan lajur kolom merupakan bagian input. Untuk mengetahui kebenaran rangkaian keypad yang telah dibuat maka keluaran dari rangkaian keypad ini akan ditampilkan ke port 3 MCU 89C51.

4.7.2. Peralatan yang digunakan

1. *Keypad*
2. *Minimum system*
3. LCD
4. Catu daya 5 VDC

4.7.3. Pelaksanaan Pengujian

1. Alat – alat dirangkai seperti dalam gambar 4.12
2. Menekan tombol – tombol pada *keypad* dan mengamati serta mencatat keluaran yang ditampilkan ke LCD



Gambar 4.12 Diagram Blok Pengujian Pengkode *Keypad*

4.7.4. Hasil dan Analisis Pengujian

Dari hasil pengujian, didapatkan data seperti dalam Tabel 4.6 maka dapat diketahui bahwa saat tombol ditekan maka keluaran port 3 mikrokontroler 89S51 akan berlogika sesuai dengan tombol yang ditekan. Hasil pengujian dalam Tabel 4.6 terlihat bahwa rangkaian papan tombol yang telah direalisasikan sesuai dengan unjuk kerja perencanaan.

Tabel 4.9. Hasil Pengujian Pengkode *Keypad*

BUTTON	B4	B3	B2	B1	C4	C3	C2	C1
1	1	1	1	0	1	1	1	0
02	1	1	1	0	1	1	0	1
3	1	1	1	0	1	0	1	1
MEN	1	1	1	0	0	1	1	1
4	1	1	0	1	1	1	1	0
5	1	1	0	1	1	1	0	1
6	1	1	0	1	1	0	1	1
COR	1	1	0	1	0	1	1	1
7	1	0	1	1	1	1	1	0
8	1	0	1	1	1	1	0	1
9	1	0	1	1	1	0	1	1
↑	1	0	1	1	0	1	1	1
CAN	0	1	1	1	1	1	1	0
0	0	1	1	1	1	1	0	1
ENT	0	1	1	1	1	0	1	1
↓	0	1	1	1	0	1	1	1

Keterangan :

B1= Baris ke 1	C1= Kolom ke 1
B2= Baris ke 2	C2= Kolom ke 2
B3= Baris ke 3	C3= Kolom ke 3
B4= Baris ke 4	C4= Kolom ke 4

4.8 Pengujian Sistem Keseluruhan

4.8.1 Tujuan

Untuk mengetahui kerja alat secara keseluruhan baik itu dari *Hardware* dan *Sofware* dan penggabungan pada kerja mekanik alat yang telah dibuat.

4.8.2 Peralatan yang digunakan

Alat *pengaduk permen dengan fitur pemanas* menggunakan mikrokontroller AT89S51

4.8.3 Pelaksanaan Pengujian

1. Mengkondisikan kesiapan alat
2. Mengisi program pada *flash memory internal.*
3. Mengaktifkan alat dan menjalankan program sesuai dengan *Flowchart* program yang telah direncanakan.
4. Mengamati dan mencatat hasil kerja alat.

Hasil dan Analisis Pengujian Sensor Suhu

Table 4.10.Hasil Pengujian sensor suhu

Pengujian ke	Suhu yang ditanpilkan pada LCD	Suhu pada thermometer digital	%error
1	25	27	8 %
2	45	47	4,4%
3	50	52	4 %
4	60	72	3,3 %
5	70	72	2,8 %

- suhu = 25 Pengukuran = 27

$$=\frac{27-25}{25}\times 100\% \qquad = 8\%$$

- suhu = 45 Pengukuran = 47

$$=\frac{47-45}{45}\times 100\% \qquad = 4{,}44\%$$

- suhu = 50 Pengukuran = 52

$$=\frac{52-50}{50}\times 100\% \qquad = 4\%$$

- suhu = 60 Pengukuran = 62

$$=\frac{62-60}{60}\times 100\% \qquad = 3{,}3\%$$

- suhu = 70 Pengukuran = 72

$$=\frac{72-70}{70}\times 100\% \qquad = 2{,}8\%$$

4.8.5.Analisa

Dari hasil pengukuran diatas maka didapat rata-rata presentase error sebesar:

$$= \frac{8\% + 4{,}44\% + 4\% + 3{,}3\% + 2{,}8\%}{5} \qquad = 4{,}5\%$$

karena rata-rata persen error kurang dari 5 persen maka percobaan dikatakan berhasil

4.8.6. Hasil dan Analisis Pengujian TIMER

Table 4.11.Hasil Pengujian TIMER

Pengujian ke	Timer yang di inputkan pada alat	Pegukuran dengan stopwatch	%error
1	1 menit	1 menit 1detik	1,6
2	2 menit	2 menit 2 detik	1,6
3	5menit	5 menit 2 detik	0,6
4	10 menit	10 menit 1 detik	0,1
5	15 menit	15 menit 3 detik	0,3

- Timer inputan = 1 menit stopwatch = 1 menit 4 detik

$$= \frac{61s - 60s}{60} \times 100\% \qquad = 1{,}6\%$$

- Timer inputan = 2 menit stopwatch = 2 menit 7 detik

$$=\frac{122s-120s}{120s}\times 100\% \qquad = 1{,}6\%$$

- Timer inputan = 5 menit stopwatch = 5 menit 14 detik

$$=\frac{302-300}{300}\times 100\% \qquad = 0{,}6\%$$

- Timer inputan = 10 menit stopwatch = 10 menit 24 detik

$$=\frac{601-600}{600}\times 100\% \qquad = 0{,}1\ \%$$

- Timer inputan = 15 menit stopwatch = 15 menit 43 detik

$$=\frac{903-900}{900}\times 100\% \qquad = 0{,}3\%$$

4.8.7. Analisa

Dari hasil pengukuran diatas maka didapat rata-rata presentase error sebesar:

$$=\frac{1{,}6\%+1{,}6\%+0{,}6\%+0{,}1\%+0{,}3\%}{5} \qquad = 0{,}84\%$$

karena rata-rata persen error di bawah 5 persen maka percobaan dikatakan berhasil

4.9. Hasil Komparasi Proses Pembuatan Permen

Setelah alat pengaduk permen selesai di uji secara keseluruhan.Maka alat ini segera dicoba untuk mempraktekan proses pembuatan permen secara riil. Dengan cara membandingkan proses pembuatan permen dengan

menggunakan alat pengaduk permen ini dan proses pembuatan permen secara konvensional.

Setelah percobaan tersebut didapatkan hasil komparasi seperti pada tabel 4.12 .

Table 4.12. hasil komparasi Pembuatan Permen Jelly

No.	Dengan Alat Pengaduk	Secara konvensional.
1.	Bahan tercampur lebih homogen pada suhu 70°C.	Pada suhu 70°C bahan belum tercampur homogen, gelatin masih padat sehingga rasa permen seperti berpasir.
2.	Hasil permen setelah dibiarkan selama 24 jam pada cetakan lebih keras, berarti kadar air rendah.	Hasil permen setelah dibiarkan selama 24 jam pada cetakan masih basah, berarti kadar air lebih banyak.
3.	Karena kadar air lebih rendah, dimungkinkan permen yang dihasilkan lebih awet atau tahan lama sehingga hanya memerlukan waktu sterilisasi dingin sebentar.	Karena kadar air lebih banyak dimungkinkan permen yang dihasilkan kurang tahan lama sehingga perlu sterilisasi dingin lebih lama (dengan memakai penyinaran ultra violet dilemari steril).
4.	Dapat dipakai untuk membuat permen coklat yang memerlukan suhu rendah.	Untuk membuat permen coklat dengan cara ini (coklat dilelehkan dengan cara ditim menggunakan kompor listrik) tetapi coklat yang dihasilkan kurang bagus.

4.9.1. kesimpulan

Dengan dilakukannya percobaan diatas maka dapat diketahui kelebihan alat pengaduk permen ini sehingga alat ini layak untuk dipakai pada proses produksi pembuatan permen.

menggunakan alat pengaduk permen ini dan proses pembuatan permen secara konvensional.

Setelah percobaan tersebut didapatkan hasil komparasi seperti pada tabel 4.12.

Table 4.12. hasil komparasi Pembuatan Permen Jelly

No.	Dengan Alat Pengaduk	Secara konvensional
1.	Bahan tercampur lebih homogen pada suhu 70°C.	Pada suhu 70°C bahan belum tercampur homogen. gelatin masih padat sehingga rasa permen seperti berpasir.
2.	Hasil permen setelah dibiarkan selama 24 jam pada cetakan lebih keras, berarti kadar air rendah.	Hasil permen setelah dibiarkan selama 24 jam pada cetakan masih basah, berarti kadar air lebih banyak.
3.	Karena kadar air lebih rendah. dimungkinkan permen yang dihasilkan lebih awet atau tahan lama sehingga banyak waktu sterilisasi dingin sebentar.	Karena kadar air lebih banyak dimungkinkan permen yang dihasilkan kurang tahan lama sehingga perlu sterilisasi dingin lebih lama (dengan memakai penyinaran ultra violet dilemari steril).
4.	Dapat dipakai untuk membuat permen coklat yang monerlukan suhu rendah.	Untuk membuat permen coklat dengan cara ini (coklat dileleikan dengan dirim menggunakan kompor listrik) tetapi coklat yang dihasilkan kurang bagus.

4.9.1. kesimpulan

Dengan dilakukannya percobaan diatas maka dapat dikatakan kelebihan alat pengaduk permen ini sehingga alat ini layak untuk dipakai pada proses produksi pembuatan permen.

BAB V

KESIMPULAN DAN SARAN

5.1 Kesimpulan

Setelah dilakukan pengujian hasil perancangan alat *alat pengaduk permen dengan fitur pemanas* berbasis Mikrokontroller AT89S51, dapat diambil beberapa kesimpulan:

1. Rangkaian SENSOR SUHU yang terdiri dari SENSOR LM 35 dan rangkaian ADC telah dapat memberikan perbandingan data yang cukup akurat dengan prosentase error sebesar 0%
2. Dari hasil pengujian SENSOR SUHU oleh alat diperoleh eror rata-rata sebesar 4,27%.
3. Dari hasil pengujian timer oleh alat diperoleh eror rata-rata sebesar 0,84%.
4. Suhu air di dalam bejana pengaduk permen di set tidak bisa kurang dari 25 derajad celcius di karenakan suhu tersebut nerupakan suhu ruang.
5. Suhu air untuk memanaskan air harus di set tidak bole terlampau tinggi sekitar <70 derajad celcius untuk menghindari kerusakan produk.
6. Dengan dilakukannya percobaan komparasi pengoperasian alat pengaduk dengan proses pengadukan konvensional dapat diketahui kelebihan alat pengaduk permen ini sehingga alat ini layak untuk dipakai pada proses produksi pembuatan permen.
7. Setiap perangkat, baik itu *hardware* ataupun *software* pada perencanaan dan pembuatan alat pengaduk permen ini mempunyai peran penting yang saling berkesinambungan satu sama lain agar tercipta sistem kerja alat pengaduk permen secara maksimal

BAB V

KESIMPULAN DAN SARAN

5.1 Kesimpulan

Setelah dilakukan pengujian hasil perancangan alat alat pengaduk permen dengan *fitur pemanas* berbasis Mikrokontroller AT89S51, dapat diambil beberapa kesimpulan:

1. Rangkaian SENSOR SUHU yang terdiri dari SENSOR LM 35 dan rangkaian ADC telah dapat memberikan perbandingan data yang cukup akurat dengan prosentase error sebesar 0%
2. Dari hasil pengujian SENSOR SUHU oleh alat diperoleh eror rata-rata sebesar 4.27%.
3. Dari hasil pengujian timer oleh alat diperoleh eror rata-rata sebesar 0.84%.
4. Suhu air di dalam bejana pengaduk permen di set tidak bisa kurang dari 25 derajad celcius di karenakan suhu tersebut merupakan suhu ruang.
5. Suhu air untuk memanaskan air harus di set tidak bole terlampau tinggi sekitar <70 derajad celcius untuk menghindari kerusakan produk.
6. Dengan dilakukannya percobaan komparasi pengoperasian alat pengaduk dengan proses pengadukan konvensional dapat diketahui kelebihan alat pengaduk permen ini sehingga alat ini layak untuk dipakai pada proses produksi pembuatan permen.
7. Setiap perangkat, baik itu *hardware* ataupun *software* pada perencanaan dan pembuatan alat pengaduk permen ini mempunyai peran penting yang saling berkesinambungan satu sama lain agar tercipta sistem kerja alat pengaduk permen secara maksimal

5.2 Saran

Beberapa tambahan yang diperlukan dalam meningkatkan kemampuan alat ini adalah:

1. Untuk meringankan kerja motor DC desain pengaduk dapat dibuat lebih hidrodinamis agar kerja notor dc lebih ringan.
2. Untuk mendapatkan hasil yang lebih presisi dapat digunakan instrumen ukur yang lebih presisi dan akurat
3. Perancangan sensor level air pada pengenmbangan selanjutnya dapt menggunakan system pelampung agar dapat terhindar dari noise heater..
4. Untuk pengembangan lebih lanjut *alat pengaduk permen* tersebut dapat dilakukan dengan menambahkan volume tempat pengaduk,serta desain yang lebih sederhana agar bias diproduksi secara masal.

5.2 Saran

Beberapa tambahan yang diperlukan dalam meningkatkan kemampuan alat ini adalah:

1. Untuk meringankan kerja motor DC desain penggabuk dapat dibuat lebih hidrodinamis agar kerja motor dc lebih ringan
2. Untuk mendapatkan hasil yang lebih presisi dapat digunakan instrumen ukur yang lebih presisi dan akurat
3. Pemancangan sensor level air pada pengembangan selanjutnya dapt menggunakan system pelampung agar dapat terhindar dari noise louter..
4. Untuk pengembangan lebih lanjut alat penggabuk perwww terscbut dapat dilakukan dengan menambahkan volume tempat penggabuk.sesra desain yang lebih sederhana agar bias diproduksi secara masal.

Daftar Pustaka

1] www.datasheetcatalog.com

[2]WWW.tech-faq.com/fsk.

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[3] Datasheet Mikrokontroler At89s51.http://...

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[6] http://...

[7] http://...

[8] http://gedex.web.id/

LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura – gura No.2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Suryo Adi Wibowo
Nim : 05.12.201
Masa Bimbingan : 14 September 2009 s/d 14 Maret 2010
Judul Skripsi : Pembuatan Dan Perancangan Alat Pengaduk Permen Dengan Fitur Pemanas Pada Industri Kecil Menengah Berbasis Mikrokontroller AT89S51

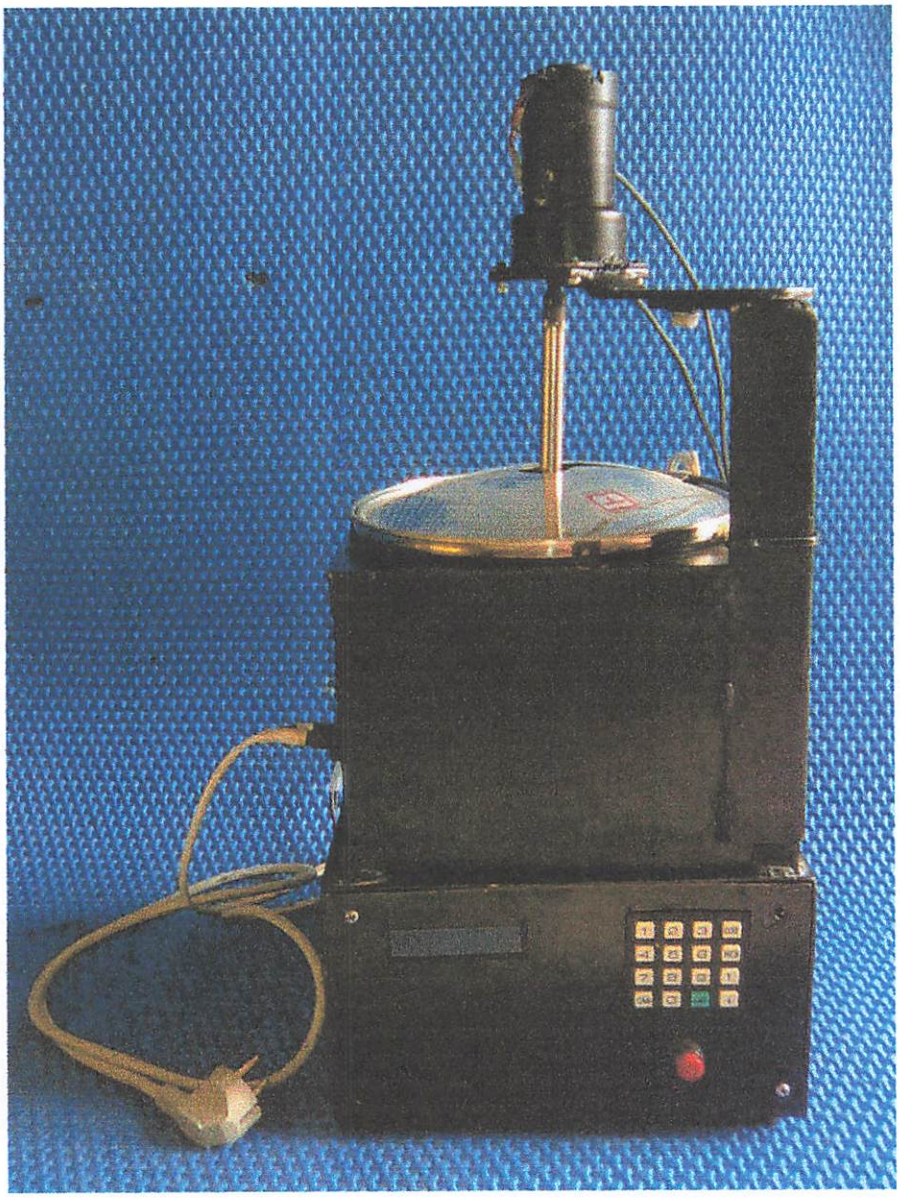
No	Tanggal	Uraian	Paraf Pembimbing
1	12-11-2009	Bab 1	
2	8-12-2009	Bab 1 revisi	
3	16-12-2009	Bab 2	
4	17-12-2009	Bab 3	
5	18-12-2009	Bab 3 revisi	
6	12-1-2010	Bab4 dan bab 5	
7	20-1-2010	Bab 4 dan bab 5 revisi	
8	23-1-2010	Makalah seminar hasil	
9	5-2-2010	Makalah seminar hasil revisi	
10			

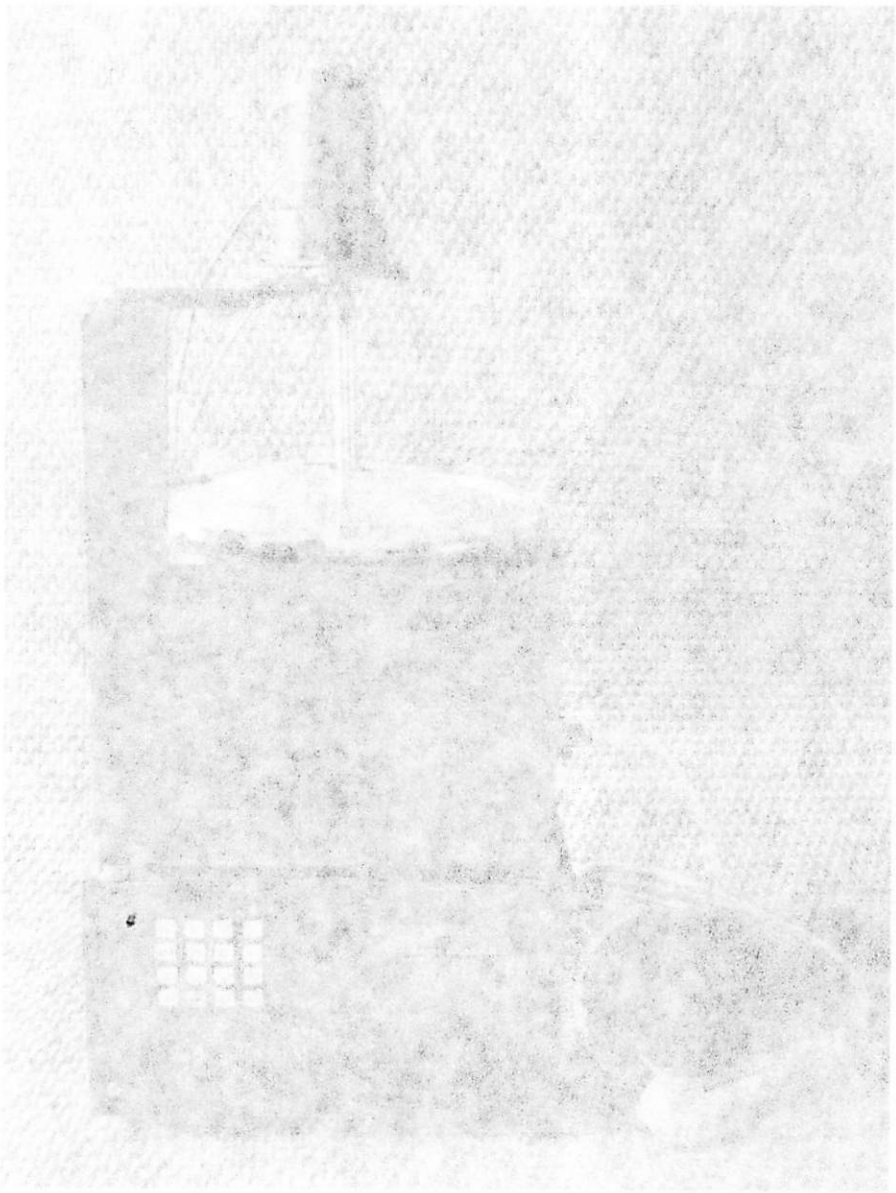
Malang,

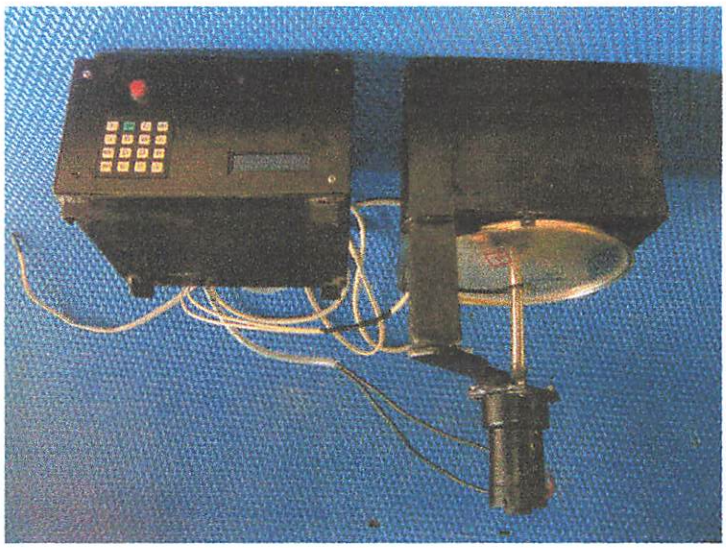
Dosen Pembimbing

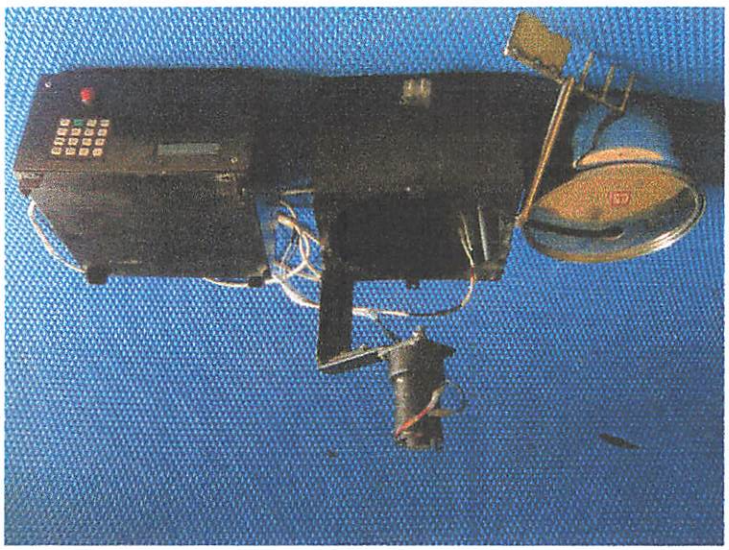
I KOMANG SOMAWIRATA,ST,MT
NIP.P 1030100361

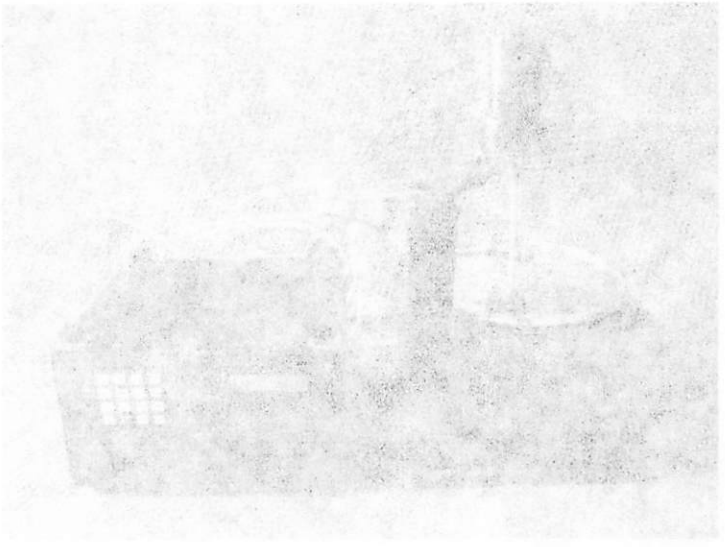
Form S-4b

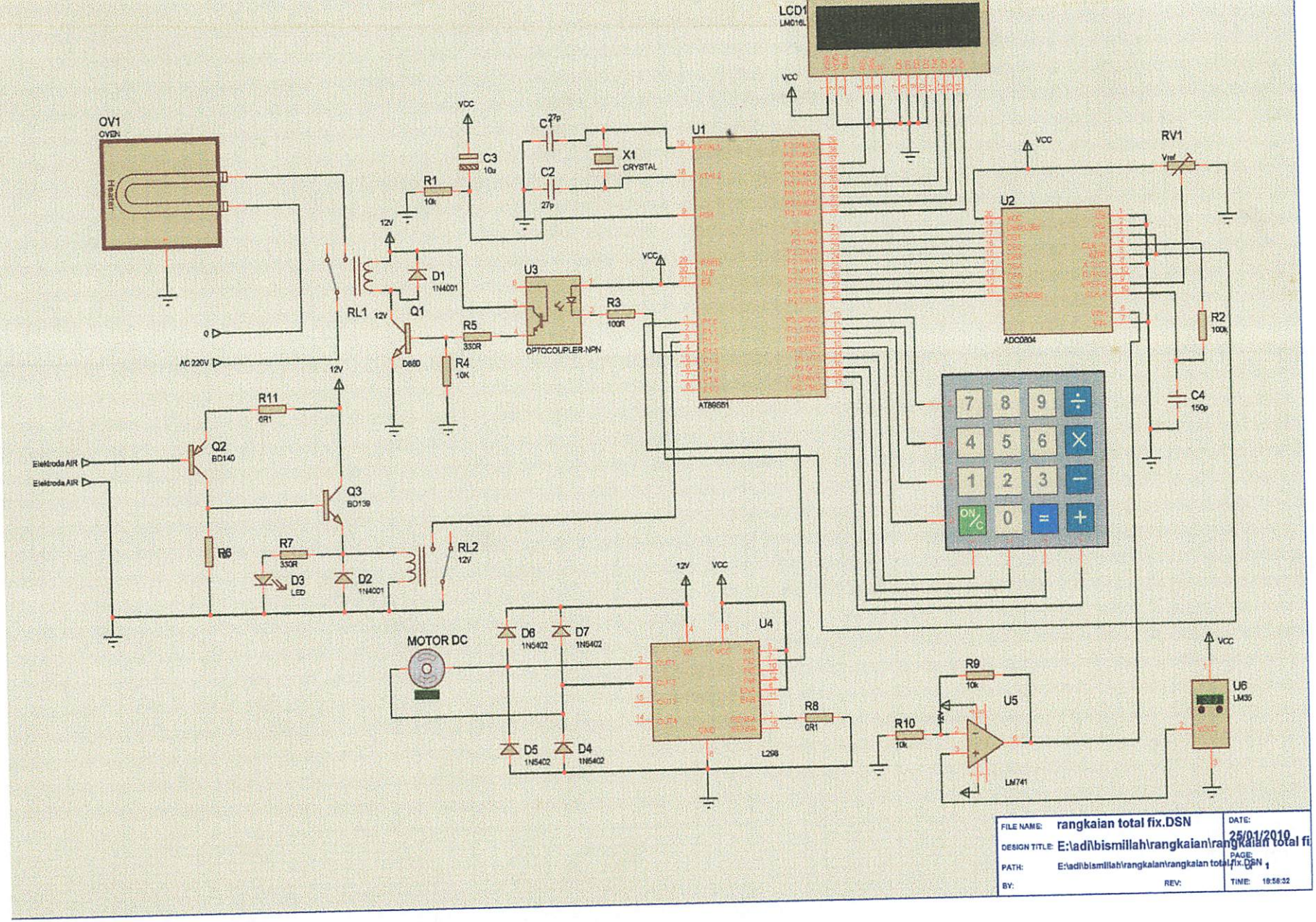











LCD1
LM016L
VCC
OV1
OVEN
Heater
C3
10u
R1
10k
12V
C1
27p
C2
27p
X1
CRYSTAL
U1
AT89S51
RV1
Vref
U2
ADC0804
R2
100k
C4
150p
D1
1N4001
RL1
Q1
D880
R5
330R
R4
10K
U3
OPTOCOUPLER-NPN
R3
100R
0
AC 220V
R11
6R1
Q2
BD140
Q3
BD139
Elektroda AIR
Elektroda AIR
R6
R7
330R
D3
LED
D2
1N4001
RL2
12V
MOTOR DC
D6
1N5402
D7
1N5402
D5
1N5402
D4
1N5402
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L298
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FILE NAME: rangkaian total fix.DSN
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res

- tible with MCS-51® Products
- s of In-System Programmable (ISP) Flash Memory
- durance: 1000 Write/Erase Cycles
- 5.5V Operating Range
- atic Operation: 0 Hz to 33 MHz
- evel Program Memory Lock
- -bit Internal RAM
- rammable I/O Lines
- -bit Timer/Counters
- rrupt Sources
- plex UART Serial Channel
- wer Idle and Power-down Modes
- t Recovery from Power-down Mode
- og Timer
- ta Pointer
- off Flag
- ogramming Time
- ISP Programming (Byte and Page Mode)

iption

9S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K n-system programmable Flash memory. The device is manufactured using igh-density nonvolatile memory technology and is compatible with the indus-ard 80C51 instruction set and pinout. The on-chip Flash allows the program to be reprogrammed in-system or by a conventional nonvolatile memory pro-. By combining a versatile 8-bit CPU with in-system programmable Flash on a ic chip, the Atmel AT89S51 is a powerful microcontroller which provides a xible and cost-effective solution to many embedded control applications.

9S51 provides the following standard features: 4K bytes of Flash, 128 bytes of I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-o-level interrupt architecture, a full duplex serial port, on-chip oscillator, and cuitry. In addition, the AT89S51 is designed with static logic for operation zero frequency and supports two software selectable power saving modes. Mode stops the CPU while allowing the RAM, timer/counters, serial port, and system to continue functioning. The Power-down mode saves the RAM con-freezes the oscillator, disabling all other chip functions until the next external or hardware reset.

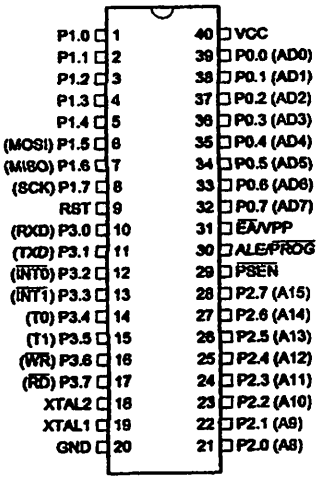
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

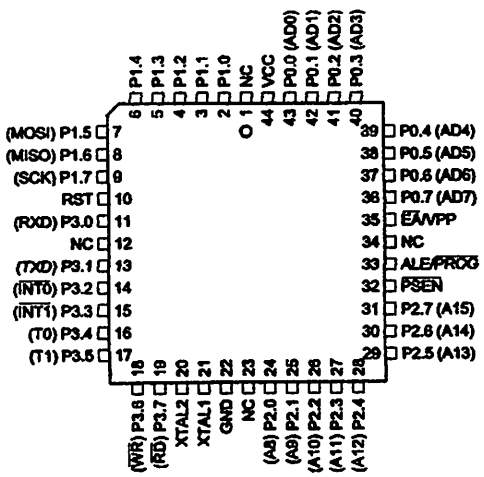
Rev. 2487A–10/01

nfigurations

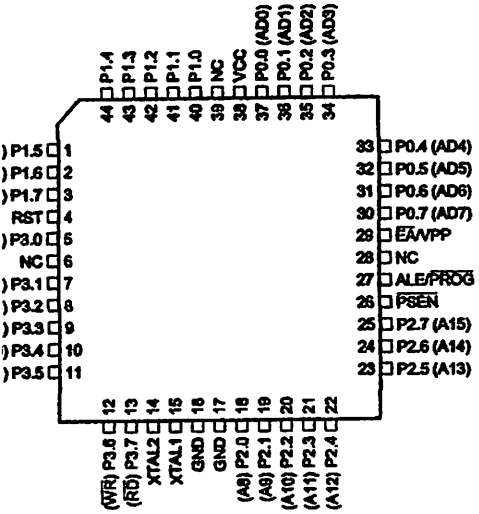
PDIP



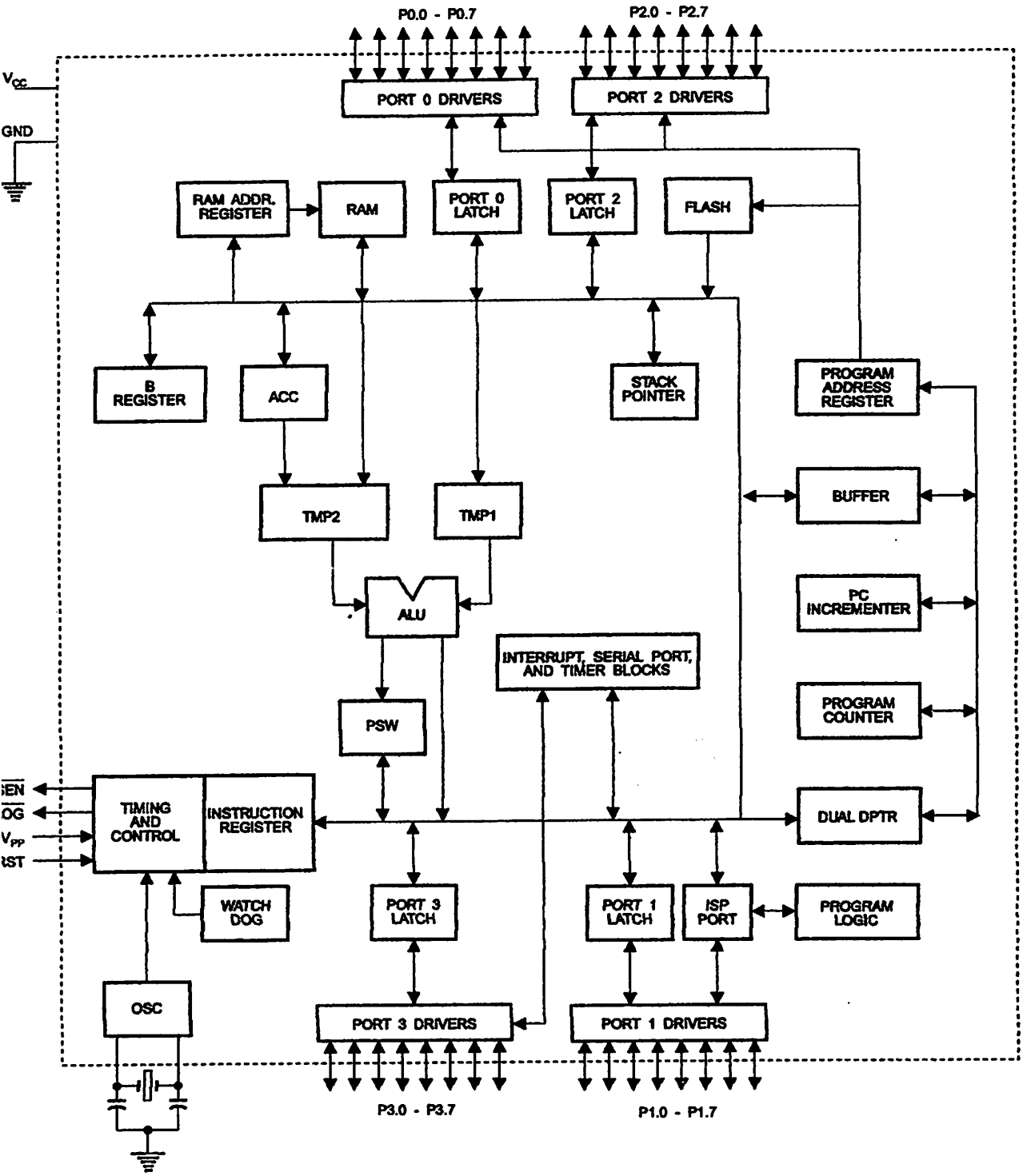
PLCC



TQFP



‹ Diagram


P0.0 - P0.7
P2.0 - P2.7
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PROGRAM COUNTER
PSW
TIMING AND CONTROL
INSTRUCTION REGISTER
DUAL DPTR
WATCH DOG
PORT 3 LATCH
PORT 1 LATCH
ISP PORT
PROGRAM LOGIC
OSC
PORT 3 DRIVERS
PORT 1 DRIVERS
P3.0 - P3.7
P1.0 - P1.7
GND

scription

Supply voltage.

Ground.

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{N}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

'PP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

_1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

_2

Output from the inverting oscillator amplifier

ecial nction gisters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

e 1. AT89S51 SFR Map and Reset Values

8H								0FFH
0H	B 00000000							0F7H
8H								0EFH
0H	ACC 00000000							0E7H
8H								0DFH
0H	PSW 00000000							0D7H
8H								0CFH
0H								0C7H
8H	IP XX000000							0BFH
0H	P3 11111111							0B7H
8H	IE 0X000000							0AFH
0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX	0A7H
0H	SCON 00000000	SBUF XXXXXXXX						9FH
0H	P1 11111111							97H
0H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0	8FH
0H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

ory inization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

ram Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

chdog er e-time bled with et-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

ng the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

uring down e

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

) and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

pts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

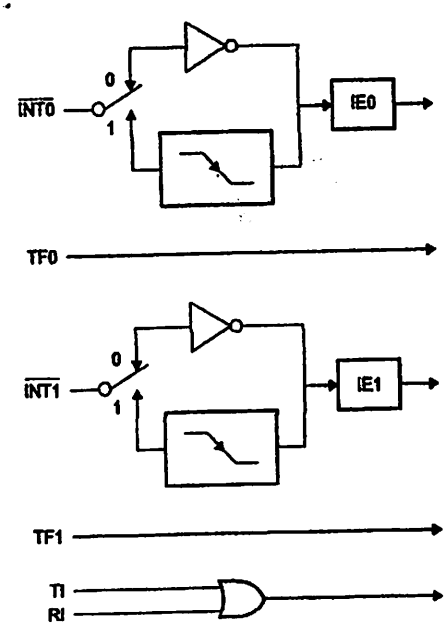
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

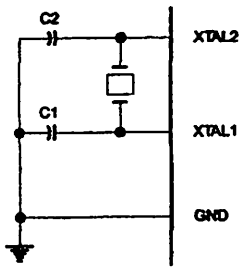
Figure 1. Interrupt Sources



llator acteristics

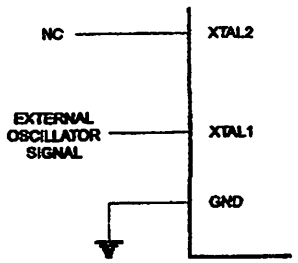
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

er-down e

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{INT0}$ or $\overline{INT1}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

ım ry Lock

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

ımming ısh – ıl Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

amming ash – Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

imming thm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between VCC and GND pins.
   Set RST pin to "H".
   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

$\overline{\text{Data}}$ Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

mming
tion Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

amming
ice –
el Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

	V_{CC}	RST	$\overline{\text{PSEN}}$	ALE/$\overline{\text{PROG}}$	$\overline{\text{EA}}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
ie Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
ie Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
k Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
k Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
k Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
k Bits	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
se	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
rel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
vice ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
vice ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

1. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{\text{BSY}}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

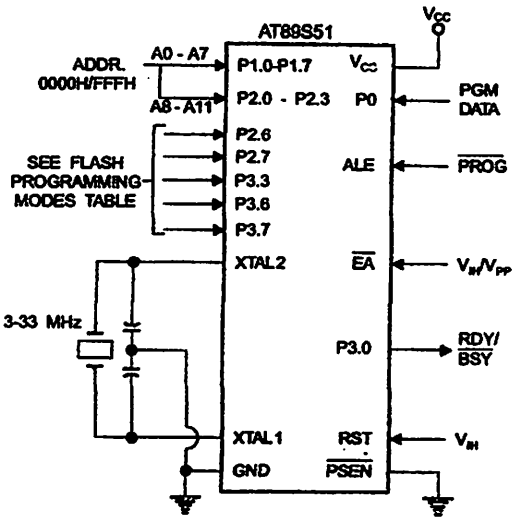
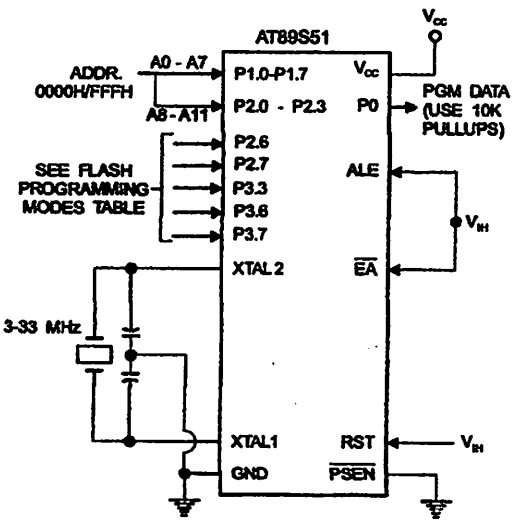


Figure 5. Verifying the Flash Memory (Parallel Mode)

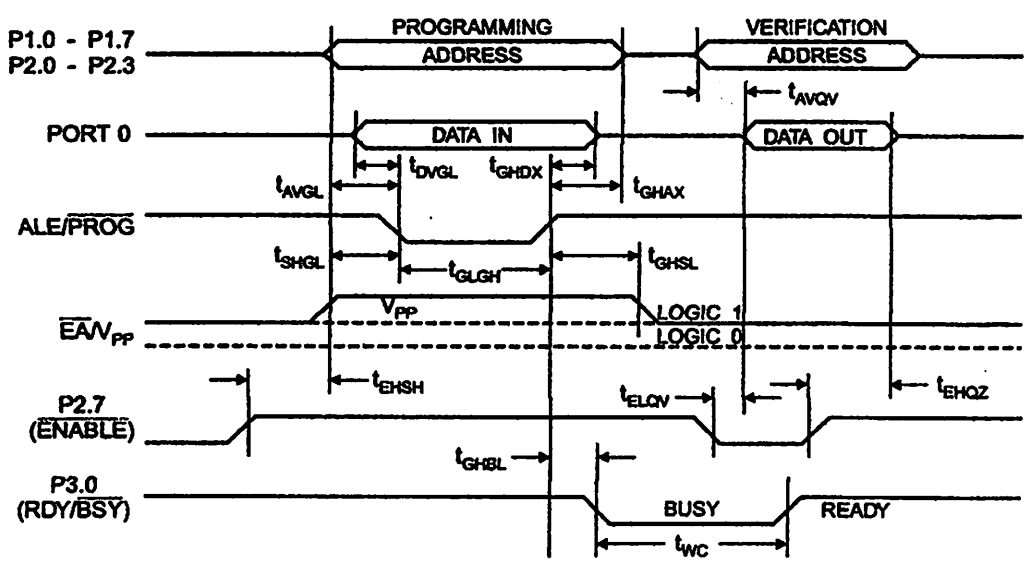


Programming and Verification Characteristics (Parallel Mode)

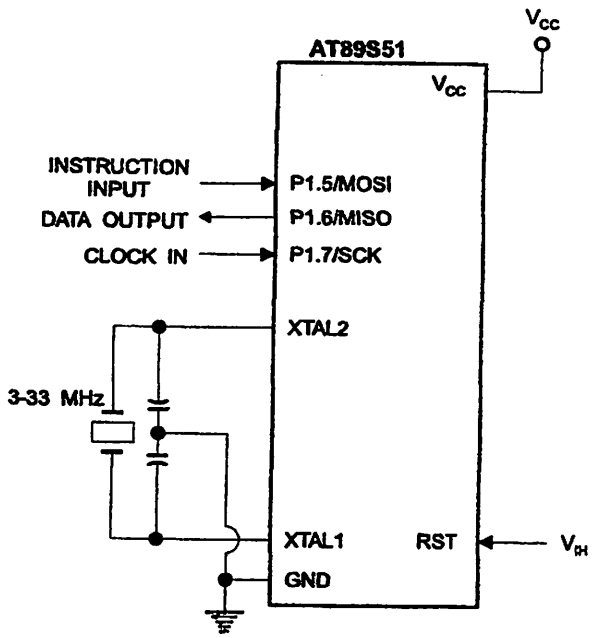
°C to 30°C, V_{CC} = 4.5 to 5.5V

	Parameter	Min	Max	Units
	Programming Supply Voltage	11.5	12.5	V
	Programming Supply Current		10	mA
	V_{CC} Supply Current		30	mA
	Oscillator Frequency	3	33	MHz
	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
	V_{PP} Hold After $\overline{PROG}$	10		µs
	$\overline{PROG}$ Width	0.2	1	µs
	Address to Data Valid		$48t_{CLCL}$	
	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		50	µs

Flash Programming and Verification Waveforms – Parallel Mode

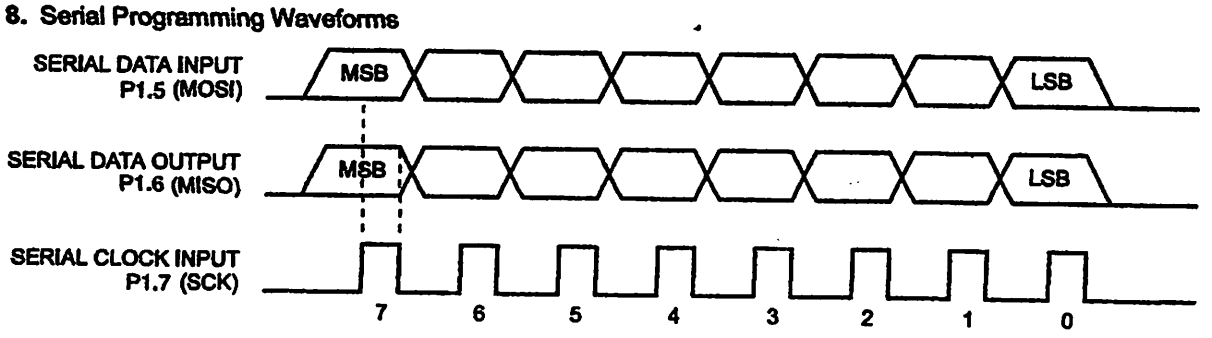


ure 7. Flash Memory Serial Downloading



sh Programming and Verification Waveforms – Serial Mode

re 8. Serial Programming Waveforms



Serial Programming Instruction Set

tion	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
nming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
ase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
rogram Memory ode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
ogram Memory ode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
ck Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
ck Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
ignature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
rogram Memory lode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
ogram Memory lode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

1. The signature bytes are not readable in Lock Bit Modes 3 and 4.
2. B1 = 0, B2 = 0 → Mode 1, no lock protection
   B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 → Mode 4, lock bit 3 activated

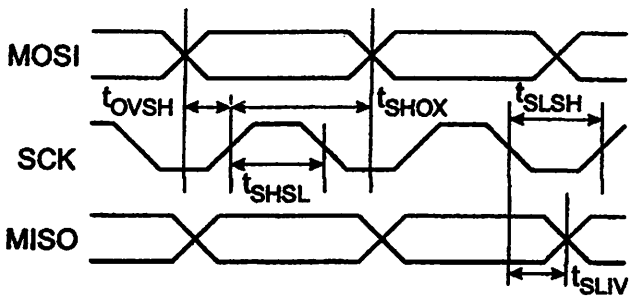
   } Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

ial Programming Characteristics

ıre 9. Serial Programming Timing



e 9. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

nbol	Parameter	Min	Typ	Max	Units
LCL	Oscillator Frequency	0		33	MHz
L	Oscillator Period	30			ns
L	SCK Pulse Width High	8 t_{CLCL}			ns
H	SCK Pulse Width Low	8 t_{CLCL}			ns
H	MOSI Setup to SCK High	t_{CLCL}			ns
X	MOSI Hold after SCK High	2 t_{CLCL}			ns
	SCK Low to MISO Valid	10	16	32	ns
SE	Chip Erase Instruction Cycle Time			500	ms
	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

olute Maximum Ratings*

iting Temperature	-55°C to +125°C
ge Temperature	-65°C to +150°C
e on Any Pin espect to Ground	-1.0V to +7.0V
ium Operating Voltage	6.6V
itput Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

lues shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

ol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
	Reset Pulldown Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

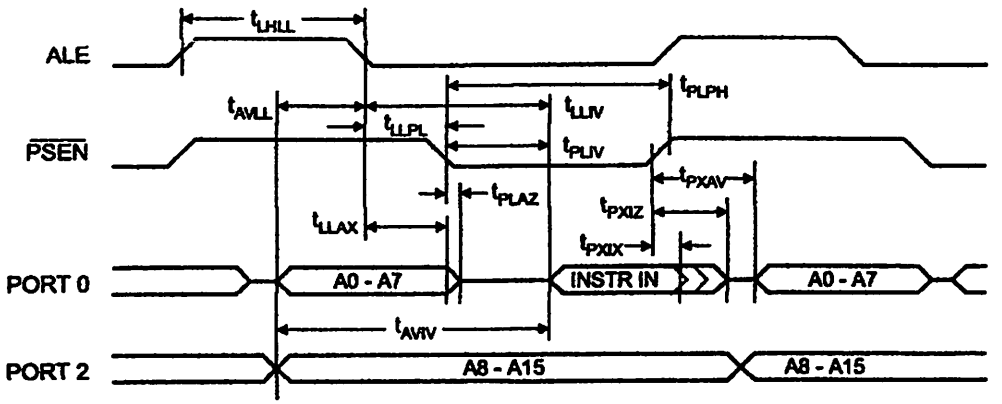
Characteristics

operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other s = 80 pF.

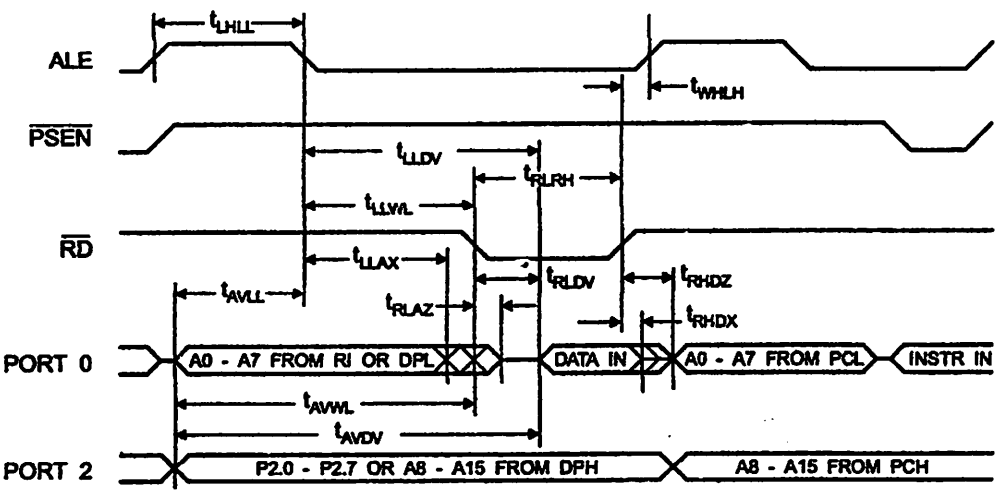
rnal Program and Data Memory Characteristics

ol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
L	Oscillator Frequency			0	33	MHz
	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
	Address Valid to ALE Low	43		t_{CLCL}-25		ns
	Address Hold After ALE Low	48		t_{CLCL}-25		ns
	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
	$\overline{PSEN}$ Low to Address Float		10		10	ns
	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
	Data Hold After $\overline{RD}$	0		0		ns
	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
	$\overline{RD}$ Low to Address Float		0		0	ns
	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

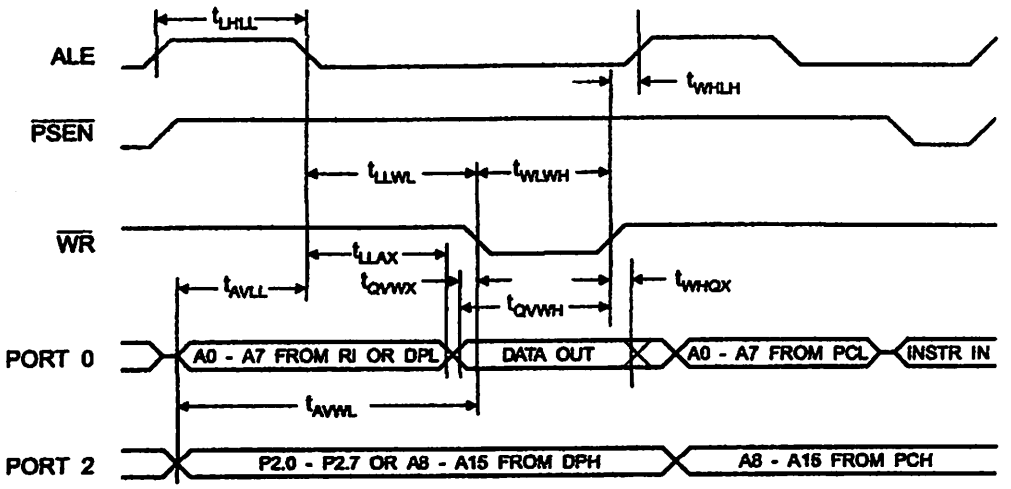
rnal Program Memory Read Cycle



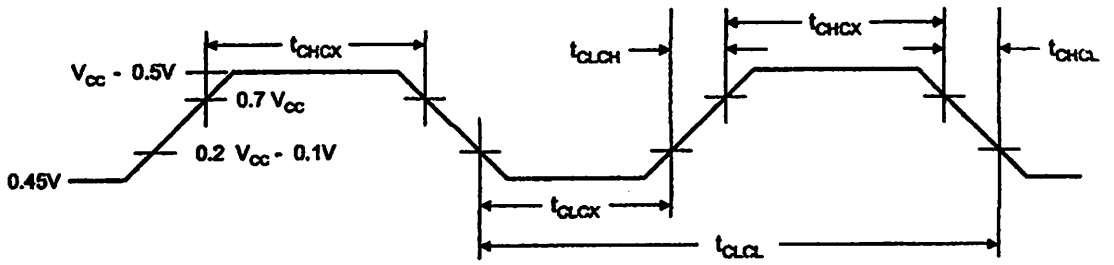
rnal Data Memory Read Cycle



nal Data Memory Write Cycle



nal Clock Drive Waveforms



nal Clock Drive

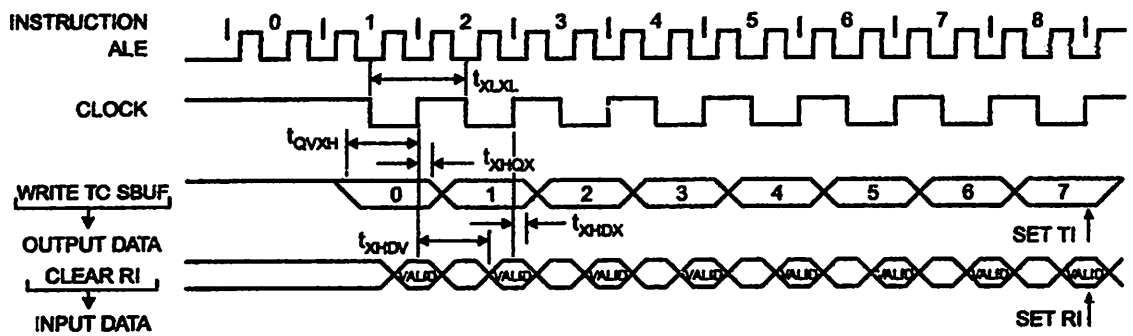
	Parameter	Min	Max	Units
	Oscillator Frequency	0	33	MHz
	Clock Period	30		ns
	High Time	12		ns
	Low Time	12		ns
	Rise Time		5	ns
	Fall Time		5	ns

Port Timing: Shift Register Mode Test Conditions

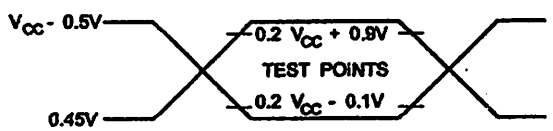
ues in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
	Input Data Hold After Clock Rising Edge	0		0		ns
	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Register Mode Timing Waveforms

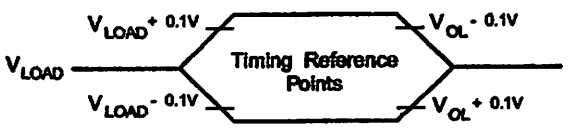


Testing Input/Output Waveforms[1]



1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Waveforms[1]



1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

ring Information

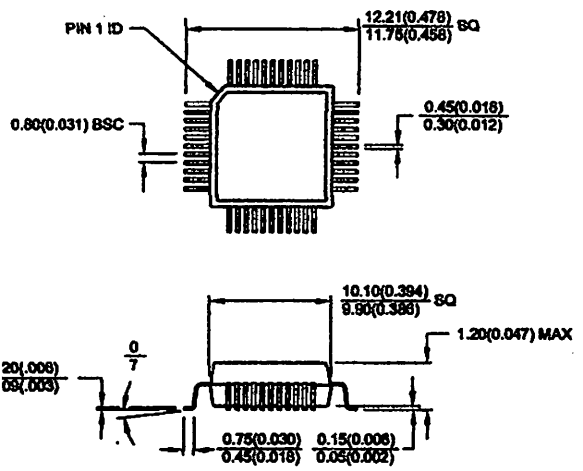
d t)	Power Supply	Ordering Code	Package	Operation Range
	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC	44A 44J 40P6	Commercial (0°C to 70°C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI	44A 44J 40P6	Industrial (-40°C to 85°C)
	[illegible]	[illegible]	[illegible]	[illegible]

= Preliminary Availability

Package Type	
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

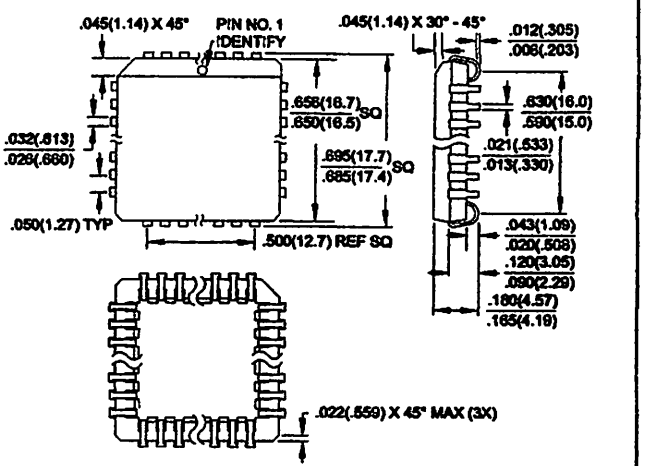
kaging Information

4A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad lat Package (TQFP)
imensions in Millimeters and (Inches)*

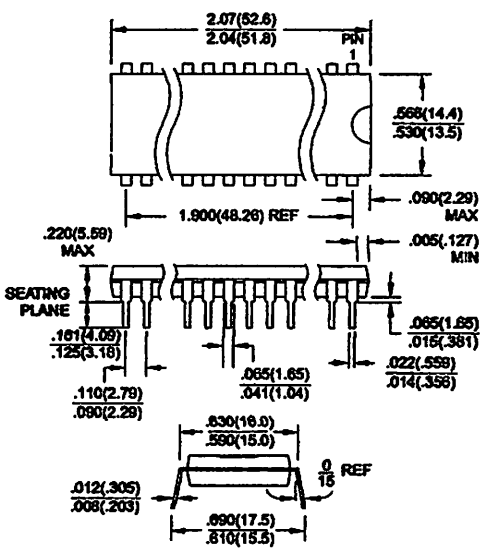


Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



DP6, 40-pin, 0.600" Wide, Plastic Dual Inline ackage (PDIP)
imensions in Inches and (Millimeters)
EDEC STANDARD MS-011 AC



l Headquarters

ate Headquarters
Orchard Parkway
lose, CA 95131
(408) 441-0311
(408) 487-2600

l SarL
s des Arsenaux 41
Postale 80
705 Fribourg
erland
41) 26-426-5555
(41) 26-426-5500

l Asia, Ltd.
1219
ichem Golden Plaza
ody Road Tsimhatsui
Kowloon
Kong
852) 2721-9778
852) 2722-1369

l Japan K.K.
onetsu Shinkawa Bldg.
8 Shinkawa
-ku, Tokyo 104-0033
81) 3-3523-3551
81) 3-3523-7581

Atmel Product Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-7658-3000
FAX (33) 4-7658-3480

Atmel Heilbronn
Theresienstrasse 2
POB 3535
D-74025 Heilbronn, Germany
TEL (49) 71 31 67 25 94
FAX (49) 71 31 67 24 23

Atmel Nantes
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 0 2 40 18 18 18
FAX (33) 0 2 40 18 19 60

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-357-000
FAX (44) 1355-242-743

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

2487A–10/01/xM

LIQUID CRYSTAL DISPLAY MODULE

M 1 6 3 2

USER MANUAL

Seiko Instruments Inc.

PREFACE

This manual describes technical informations on functions and instructions of M1632 from Seiko Instruments Inc. Please read this instruction manual carefully to understand all the module functions and make the best use of them. Description details may be changed without notice.

Revision Record

Edition	Revision	Date
1	Original	April 1985
2	Completely revised	Jan. 1987

1. GENERAL

1.1 General

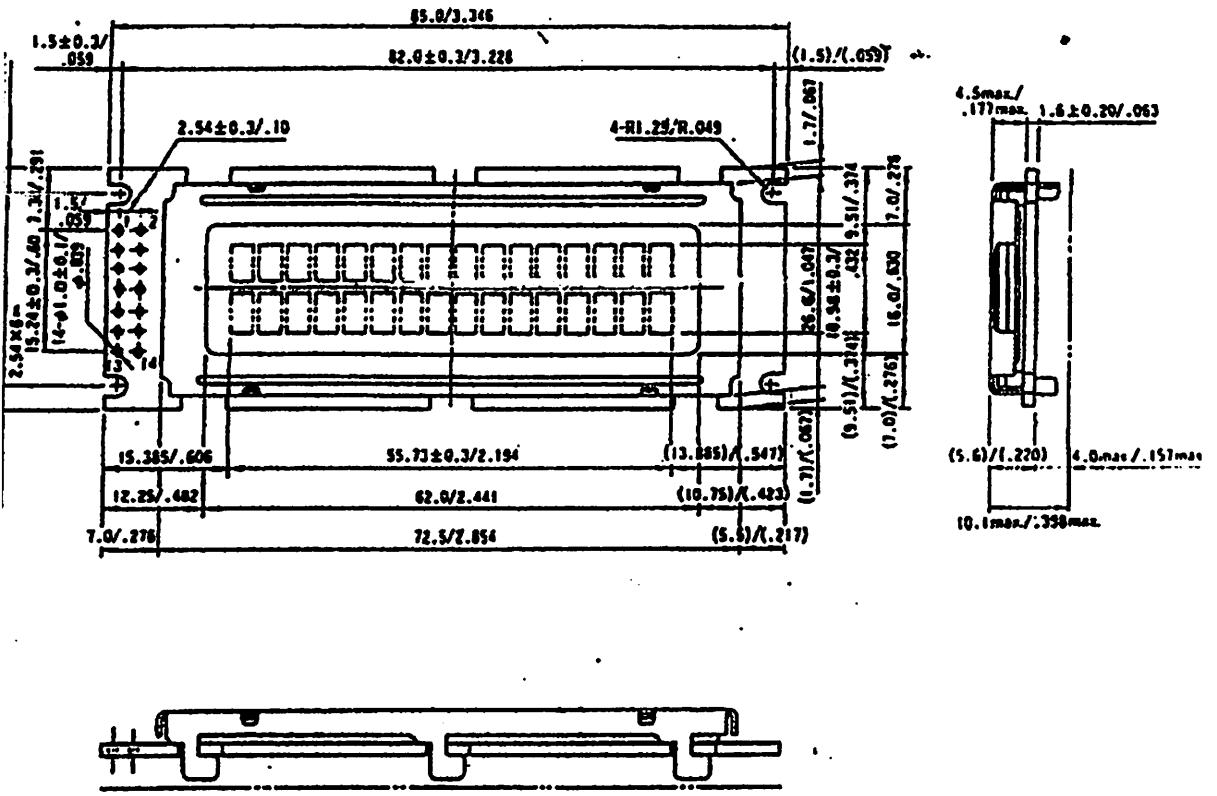
The M1632 is a low-power-consumption dot-matrix liquid crystal display (LCD) module with a high-contrast wide-view TN LCD panel and a CMOS LCD drive controller built in. The controller has a built-in character generator ROM/RAM, and display data RAM. All the display functions are controlled by instructions and the module can easily be interfaced with an MPU. This makes the module applicable to a wide range of purposes including terminal display units for microcomputers and display units for measuring gages.

1.2 Features

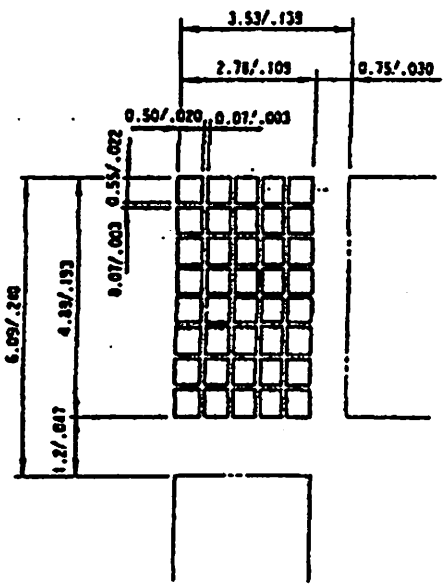
- 16-character, two-line TN liquid crystal display of 5 x 7 dot matrix + cursor
- Duty ratio: 1/16
- Character generator ROM for 192 character types.
  (character font: 5 x 7 dot matrix)
- Character generator RAM for eight character types (program write)
  (character font: 5 x 7 dot matrix)
- 80 x 8 bit display data RAM (80 characters maximum)
- Interface with four-bit and eight-bit MPUs possible
- Display data RAM and character generator RAM readable from MPU
- Many instruction functions

  Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, and Display Shift
- Built-in oscillator circuit
- +5 V single power supply
- Built-in automatic reset circuit at power-on
- CMOS process
- Operating temperature range: 0°C to 50°C

Dimensions Diagram



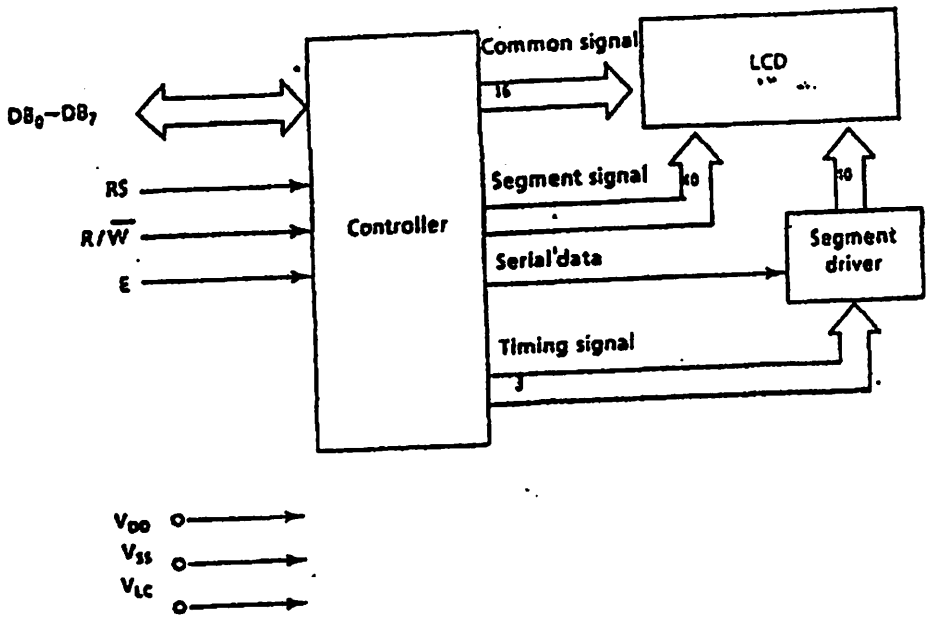
Unit : mm/inch
General tolerance : ± 0.5 mm



No.	Symbol	Level	Function	
1	Vss	-	Power Supply	0V (GND)
2	Vcc	-		5V ±10%
3	Vee	-		for LCD Drive
4	RS	H/L	H: Data Input L: Instruction Input	
5	R/W	H/L	H:READ L:WRITE	
6	E	H, ↓	Enable Signal	
7	DB0	H/L	Data Bus	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+ BL	-	Back Light Supply	4 - 4.2V 50-200mA
16	V- BL	-		0V (GND)

Figure 1 Dimensions diagran

Block Diagram



Absolute Maximum Ratings

V_{SS} = 0 V

Item	Symbol	Standard	Unit	Remarks
Power supply voltage	V_{DD}	− 0.3 to + 7.0	V	
	V_{LC}	V_{DD} − 13.5 to V_{DD} + 0.3	V	
Input voltage	V_{in}	− 0.3 to V_{DD} + 0.3	V	
Operating temperature	T_{opr}	0 to + 50	°C	
Storage temperature	T_{stg}	− 20 to + 60	°C	At 50% RH

Electrical Characteristics

V_{DD} = 5 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Conditions	Standard			Unit
				Min.	Typ.	Max.	
Input voltage	High	V_{IH1}		2.2	–	V_{DD}	V
	Low	V_{IL1}		0	–	0.6	V
Output voltage (TTL)	High	V_{OH1}	$-I_{OH}$ = 0.205 mA	2.4	–	–	V
	Low	V_{OL1}	I_{OL} = 1.2 mA	–	–	0.4	V
Output voltage (CMOS)	High	V_{OH2}	$-I_{OH}$ = 0.04 mA	0.9V_{DD}	–	–	V
	Low	V_{OL2}	I_{OL} = 0.04 mA	–	–	0.1V_{DD}	V
Power supply voltage		V_{DD}		4.75	5.00	5.25	V
		$-V_{LC}$	V_{DD} = 5 V, T_A = 25°C	–	0.25	–	V
Current consumption		I_{DD}		–	2.0	3.0	mA
		I_{LC}	V_{LC} = 0.25V	–	–	1.0	mA
Clock oscillation freq.		f_{osc}	Resistance oscillation	190	270	350	kHz

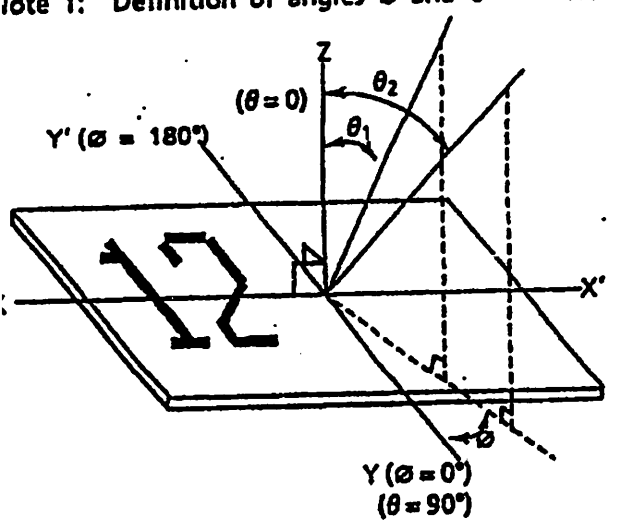
.7 Optical Characteristics

1.7.1 Optical characteristics

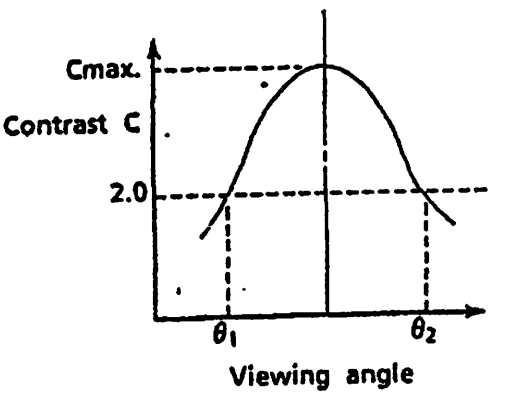
Maximum viewing angle: 6 o'clock (ϕ = 0°)
T_A = 25°C, V_{opr} = 4.75 V

Item	Symbol	Conditions	Min.	Typ.	Max.	Remarks
Viewing angle	$\theta_2 - \theta_1$	$C \geq 2.0$, $\phi = 0°$	35	–	–	See Notes 1 and 2.
Contrast	C	$\theta = 25°$, $\phi = 0°$	5	8	–	See Note 3.
Rise time	t_{on}	$\theta = 25°$, $\phi = 0°$	–	60 ms	70 ms	See Note 4.
Fall time	t_{off}	$\theta = 25°$, $\phi = 0°$	–	150 ms	170 ms	See Note 4.

Note 1: Definition of angles ϕ and θ

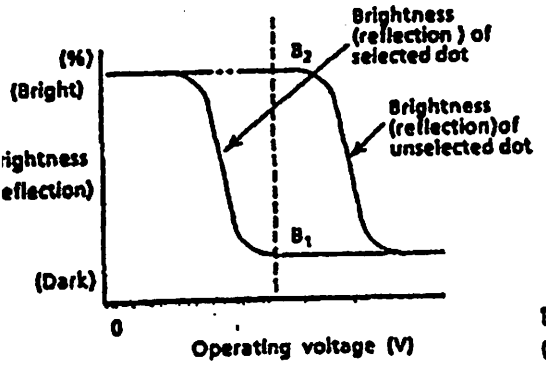


Note 2: Definition of viewing angles θ_1 and θ_2

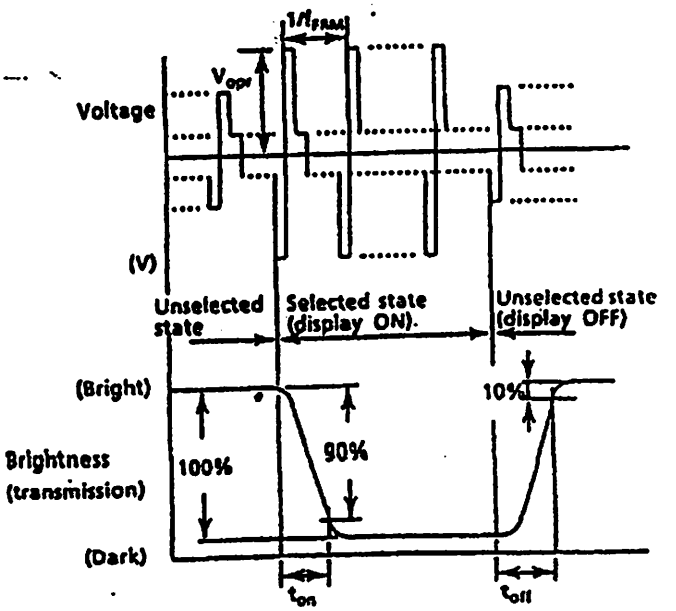


Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



V_{opr} : Operating voltage (V)
f_{FRM} : Frame frequency (Hz)
t_{on} : Response time (rise)(ms)
t_{off} : Response time (fall)(ms)

.2 Recommended operating voltage

The viewing angle and screen contrast of the LCD panel can be varied by changing the liquid crystal operating voltage (V_{opr}), that is V_{LC}.

The optical characteristics is influenced by an ambient temperature. The recommended value of V_{opr} for an ambient temperatures are shown below.

Temperature (℃)	0	10	25	40	50
Voltage V_{opr} (V)	5.00	4.90	4.75	4.60	4.50

$V_{opr} = V_{DD} - V_{LC}$

OPERATING INSTRUCTIONS

2.1 Terminal Functions

Table 1 Terminal functions

Signal name	No. of terminals	I/O	Destination	Function
DB_0 to DB_3	4	I/O	MPU	Tristate bidirectional lower four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. If the interface data is 4 bits, the signals are not used.
DB_4 to DB_7	4	I/O	MPU	Tristate bidirectional upper four data buses: Data is read from the module to the MPU or written to the module from the MPU through the buses. DB_7 is also used as a busy flag.
E	1	Input	MPU	Operation start signal: The signal activates data write or read.
$R/\overline{W}$	1	Input	MPU	Read (R) and Write ($\overline{W}$) selection signals 0 : Write 1 : Read
RS	1	Input	MPU	Register selection signals 0 : Instruction register (Write) Busy flag and address counter (Read) 1 : Data register (Write and Read)
V_{LC}	1	–	Power supply	Power supply terminal for driving liquid crystal display: The screen contrast can be varied by changing V_{LC}.
V_{DD}	1	–	Power supply	+5 V
V_{SS}	1	–	Power supply	Ground terminal: 0 V

Basic Operations

2.2.1 Registers

The controller has two kinds of eight-bit registers: the instruction register (IR) and the data register (DR). They are selected by the register select (RS) signal as shown in Table 2.

The IR stores instruction codes such as Display Clear and Cursor Shift, and the address information of display data RAM (DD RAM) and character generator RAM (CG RAM). They can be written from the MPU, but cannot be read to the MPU.

The DR temporarily stores data to be written into DD RAM or CG RAM, or read from DD RAM or CG RAM. When data is written into DD RAM or CG RAM from the MPU, the data in the DR is automatically written into DD RAM or CG RAM by internal operation. However, when data is read from DD RAM or CG RAM, the necessary data address is written into the IR. The specified data is read out to the DR and then the MPU reads it from the DR. After the read operation, the next address is set and DD RAM or CG RAM data at the address is read into the DR for the next read operation.

Table 2 Register selection

RS	$R/\overline{W}$	Operation
0	0	IR selection, IR write. Internal operation : Display clear
0	1	Busy flag (DB_7) and address counter (DB_0 to DB_6) read
1	0	DR selection, DR write. Internal operation : DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation : DD RAM or CG RAM to DR

2.2.2 Busy flag (BF)

The flag indicates whether the module is ready to accept the next instruction. As shown in Table 2, the signal is output to DB_7 if RS = 0 and $R/\overline{W}$ = 1. If the value is 1, the module is working internally and the instruction cannot be accepted. If the value is 0, the next instruction can be written. Therefore, the flag status needs to be checked before executing an instruction. If an instruction is executed without checking the flag status, wait for more than the execution time shown by 2.4 Instruction Outline.

2.3 Address counter (AC)

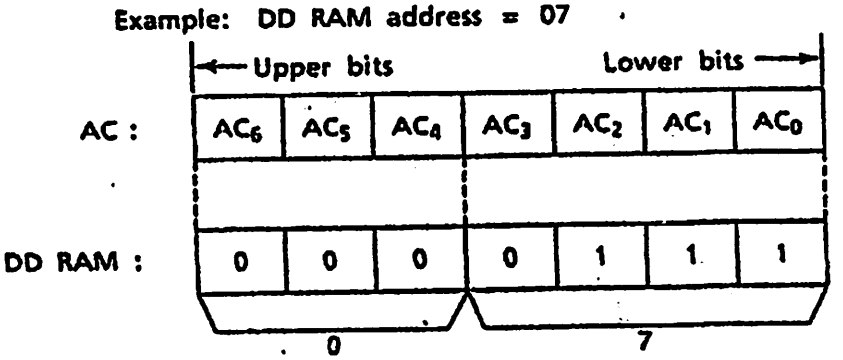
The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB_0 to DB_6 as shown in Table 2 if RS = 0 and $R/\overline{W} = 1$.

2.4 Display data RAM (DD RAM)

DD RAM has a capacity of up to 80 × 8 bits and stores display data of 80 eight-bit character codes. Some storage areas of DD RAM which are not used for display can be used as general data RAM.

A DD RAM address to be set in the AC is expressed in hexadecimal form as follows.

Example: DD RAM address = 07



00_H to $0F_H$ of the DD RAM address is set in the line 1, and 40_H to $4F_H$ in the line 2.

Note : The addresses in the digit 16 of line 1 and the digit 1 of line 2 are not consecutive.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM address
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

If the display is shifted, DD RAM address 00H to 27H are displayed in line 1 and 40H to 67H in line 2. The following figures are examples of display shifts.

*Left shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	DD RAM address
Line 2	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	

*Right shift

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	DD RAM address
Line 2	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

5 Character generator ROM (CG ROM)

Character generator ROM generates 192 types of 5 x 7 dot-matrix character patterns from eight-bit character codes.

Table 3 shows the correspondence between the CG ROM character codes and character patterns.

5 Character generator RAM (CG RAM)

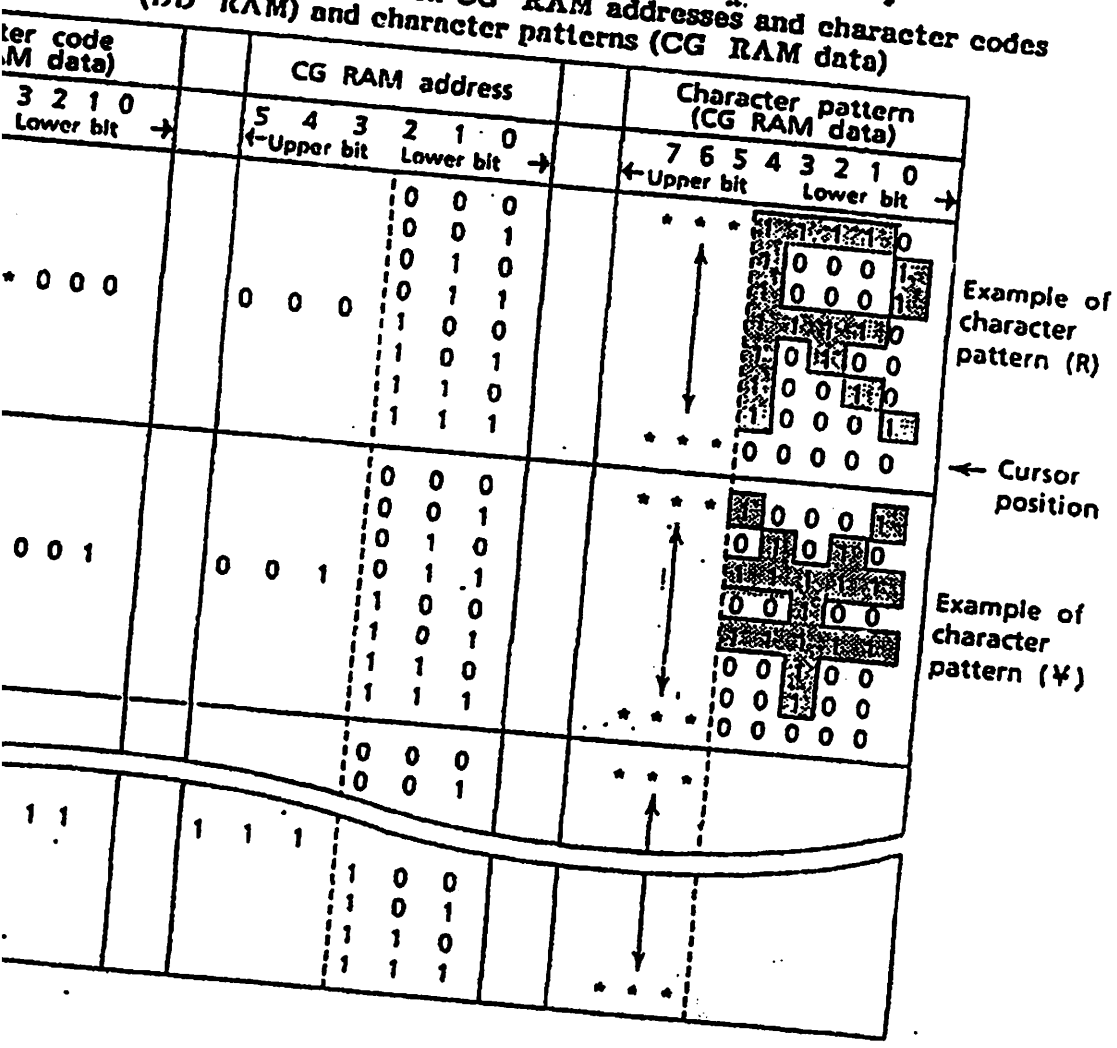
CG RAM is used to create character patterns freely by programming. Eight types of character patterns can be written.

Table 4 shows the character patterns created from CG RAM addresses and data. To display a created character pattern, the character code in the left column of the table is written into DD RAM corresponding to the display position (digit). The areas not used for display are available as general data RAM.

ble 3 Correspondence between character codes and character patterns

0 0000	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	1010	1011	1100	1101	1110	1111
CG RAM (1)												
(2)												
(3)												
(4)												
(5)												
(6)												
(7)												
(8)												
(1)												
(2)												
(3)												
(4)												
(5)												
(6)												
(7)												
(8)												

able 4 Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data)



n CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the isplay.

haracter code bits 0 to 2 and CG RAM address bits 3 to 5 correspond ith each other (three bits, eight types).

G RAM address bits 0 to 2 specify a line position for a character pattern. ne 8 of a character pattern is the cursor position where the logical sum the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to play the cursor. If the data is changed to 1, one bit lights, regardless of cursor.

The character pattern column positions correspond to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.

When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00_H and 08_H select the same character.

Timing Characteristics

3.1 Write timing characteristics

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		t_{CYCE}	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er}, t_{Ef}	–	25	ns
Setup time	RS, R/$\overline{W}$ — E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data setup time		t_{DSW}	195	–	ns
Data hold time		t_H	10	–	ns

Write operation

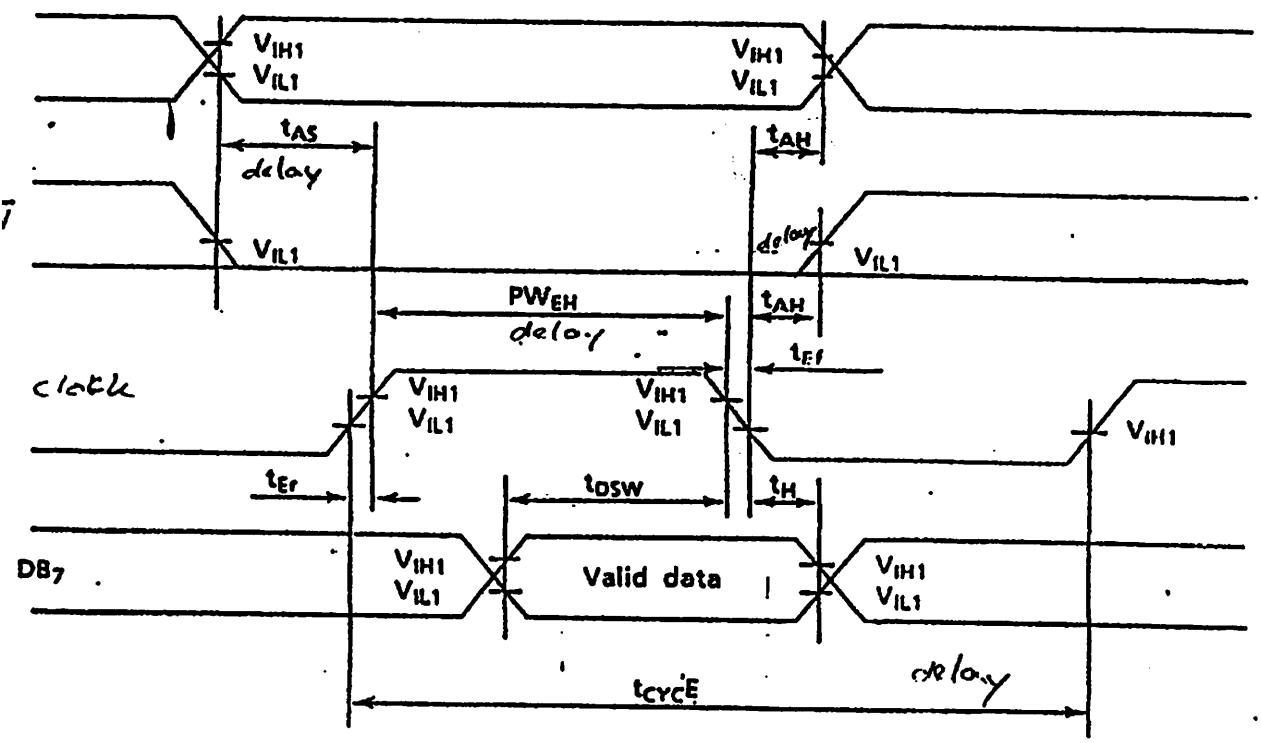


Figure 3 Data write from MPU to module

Read timing characteristics

V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0°C to 50°C

Item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		t_{CYCE}	1000	–	ns
Enable pulse width	High level	PW_{EH}	450	–	ns
Enable rise and fall time		t_{Er},t_{Ef}	–	25	ns
Setup time	RS, R/W—E	t_{AS}	140	–	ns
Address hold time		t_{AH}	10	–	ns
Data delay time		t_{DDR}	–	320	ns
Data hold time		t_{H}	20	–	ns

l operation

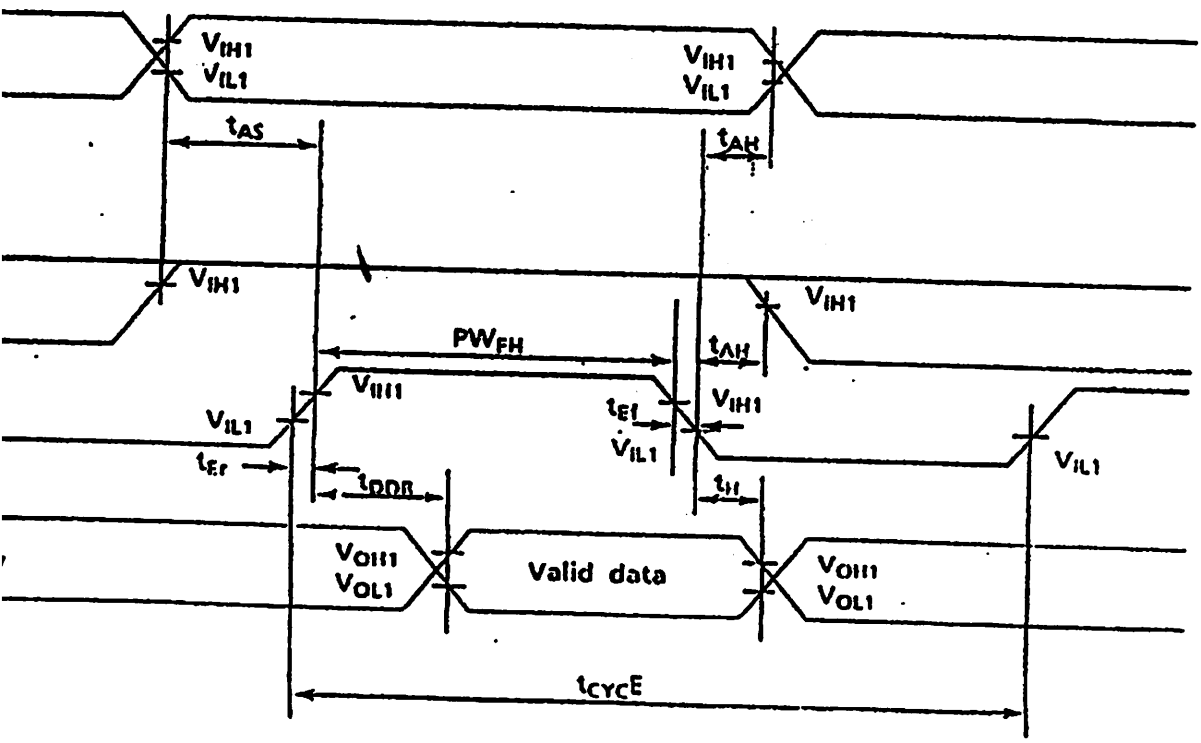


Figure 4 Data read from module to MPU

Instruction Outline

Table 5 List of instructions

Instruction	Code										Function	Execution time
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Display clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns cursor to home position (address 0)	1.64 ms
Cursor Home	0	0	0	0	0	0	0	0	1	*	Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change.	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets direction of cursor movement and whether display will be shifted when data is written or read	40 µs
Display ON / OFF control	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B)	40 µs
Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents	40 µs
Function Set	0	0	0	0	1	DL	1	*	*	*	Sets interface data length (DL)	40 µs
CG RAM Address Set	0	0	0	1	A_{CG}						Sets CG RAM address to start transmitting or receiving CG RAM data	40 µs
DD RAM Address Set	0	0	1	A_{DD}							Sets DD RAM address to start transmitting or receiving DD RAM data	40 µs
BF/Address Read	0	1	BF	AC							Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM)	0 µs
Data Write to CG RAM or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM	40 µs
Data Read from CG RAM or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM	40 µs

*: Invalid bit
ACG: CG RAM address
ADD: DD RAM address

I/D = 1 : Increment
I/D = 0 : Decrement

S = 1 : Display shift
S = 0 : No display shift

D = 1 : Display ON
D = 0 : Display OFF

C = 1 : Cursor ON
C = 0 : Cursor OFF

B = 1 : Blink ON
B = 0 : Blink OFF

S/C = 1 : Display shift
S/C = 0 : Cursor movement

R/L = 1 : Right shift
R/L = 0 : Left shift

DL = 1 : 8 bits
DL = 0 : 4 bits

BF = 1 : Internal operation in progress
BF = 0 : Instruction can be accepted

struction Details

Display Clear

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	0	1

Display Clear clears all display and returns cursor to home position (address 0).

Space code 20 (hexadecimal) is written into all the addresses of DD RAM, and DD RAM address 0 is set to the AC. If shifted, the display returns to the original position. After execution of the Display Clear instruction, the entry mode is incremented.

Note : When executing the Display Clear instruction, follow the restrictions listed in Table 6.

Cursor Home

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	0	1	*

* : Invalid bit

Cursor Home returns cursor to home position (address 0).

DD RAM address 0 is set to the AC. The cursor returns to the home position. If shifted, the display returns to the original position. The DD RAM contents do not change. If the cursor or blinking is ON, it returns to the left side.

Note : When executing the Cursor Home instruction, follow the restrictions listed in Table 6.

'able 6 Restrictions on execution of Display Clear and Cursor Home instructions

Conditions of use	Restrictions
hen executing the Display Clear or Cursor ome instruction when the display is ifted (after execution of Display Shift struction)	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{osc}$* second after the first execution. Example: 1.5 ms, 3 ms, 4.5 ms for f_{osc} = 270 kHz *f_{osc}: Oscillation frequency
hen 23_H, 77_H, 63_H, or 67_H is used as a DD \M address to execute Cursor Home struction	Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM.(This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)

) Entry Mode Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry Mode Set sets the direction of cursor movement and whether display will be shifted.

I/D : The DD RAM address is incremented or decremented by one when a character code is written into or read from DD RAM. This is also true for writing into or reading from CG RAM.

When I/D = 1, the address is incremented by one and the cursor or blink moves to the right.

When I/D = 0, the address is decremented by one and the cursor or blink moves to the left.

S : If S = 1, the entire display is shifted either to the right or left for writing into DD RAM. The cursor position does not change, only the display moves. There is no display shift for reading from DD RAM.

When S = 1 and I/D = 1, the display shifts to the left.
When S = 1 and I/D = 0, the display shifts to the right.

If S = 0, the display does not shift.

) Display ON/OFF Control

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display ON/OFF Control turns the total display and the cursor ON and OFF, and makes the cursor position start blinking. Cursor ON/OFF and blinking is done at the column indicated by the specified DD RAM address by the AC.

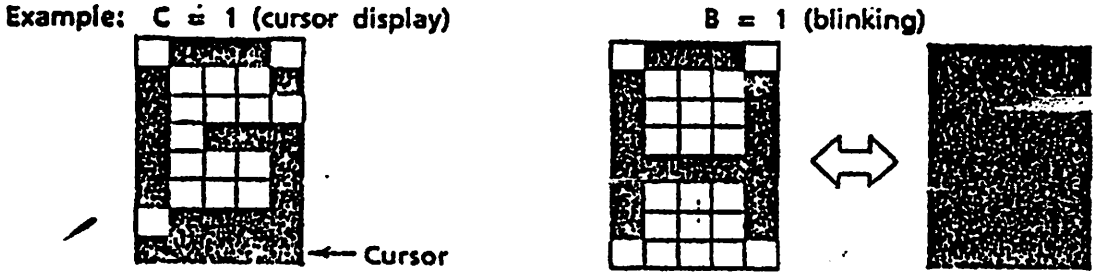
D : When D = 1, the display is turned ON.
When D = 0, the display is turned OFF.
If D = 0 is used, display data remains in DD RAM. Change 0 to 1 to display data.

C : When C = 1, the cursor is displayed.
When C = 0, the cursor is not displayed.

The cursor is displayed in the dot line below the 5 x 7 dot-matrix character fonts. If the cursor is OFF, display data is written into DD RAM in the order specified by I/D.

B : When B = 1, the character at the cursor position starts blinking.
When B = 0, it does not blink.

For blinking, all-black dots and the character are switched about every 0.4 seconds. The cursor and blinking can be set at the same time.



Cursor/Display Shift

	RS	R/$\overline{W}$	DB_7						DB_0	
Code	0	0	0	0	0	1	S/C	R/L	*	*

* :Invalid bit

Cursor/Display Shift moves the cursor and shifts the display without changing the DD RAM contents.

The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. Since the DD RAM capacity is 40-character and two lines, the cursor is shifted from digit 40 of line 1 to digit 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. Therefore, the display pattern of line 2 is not shifted to line 1.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one).
0	1	The cursor position is shifted to the right (the AC increments one).
1	0	The entire display is shifted to the left with the cursor.
1	1	The entire display is shifted to the right with the cursor.

Note: If only display shift is done, the AC contents do not change.

Function Set

	RS	R/$\overline{W}$	DB_7							DB_0
Code	0	0	0	0	1	DL	1	*	*	*

* : Invalid bit

Function Set sets the interface data length.

DL : Interface data length

When DL = 1, the data length is set at eight bits (DB_7 to DB_0).

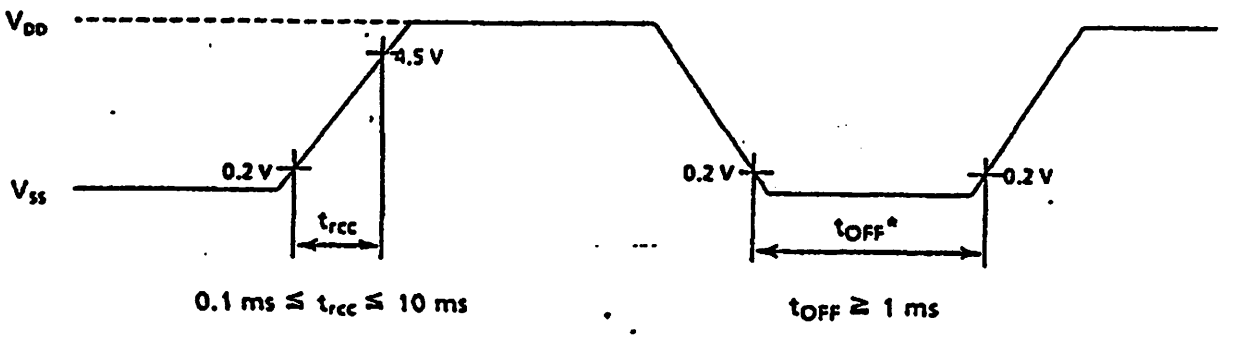
When DL = 0, the data length is set at four bits (DB_7 to DB_4).

The upper four bits are transferred first, then the lower four bits follow.

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

Remarks: Initialization

The system is automatically initialized at power-on if the following power supply conditions are satisfied.



$0.1\ ms \leq t_{rcc} \leq 10\ ms$ $\quad t_{OFF} \geq 1\ ms$

*t_{OFF}: Time when power supply is OFF if cut instantaneously or turned ON and OFF repeatedly

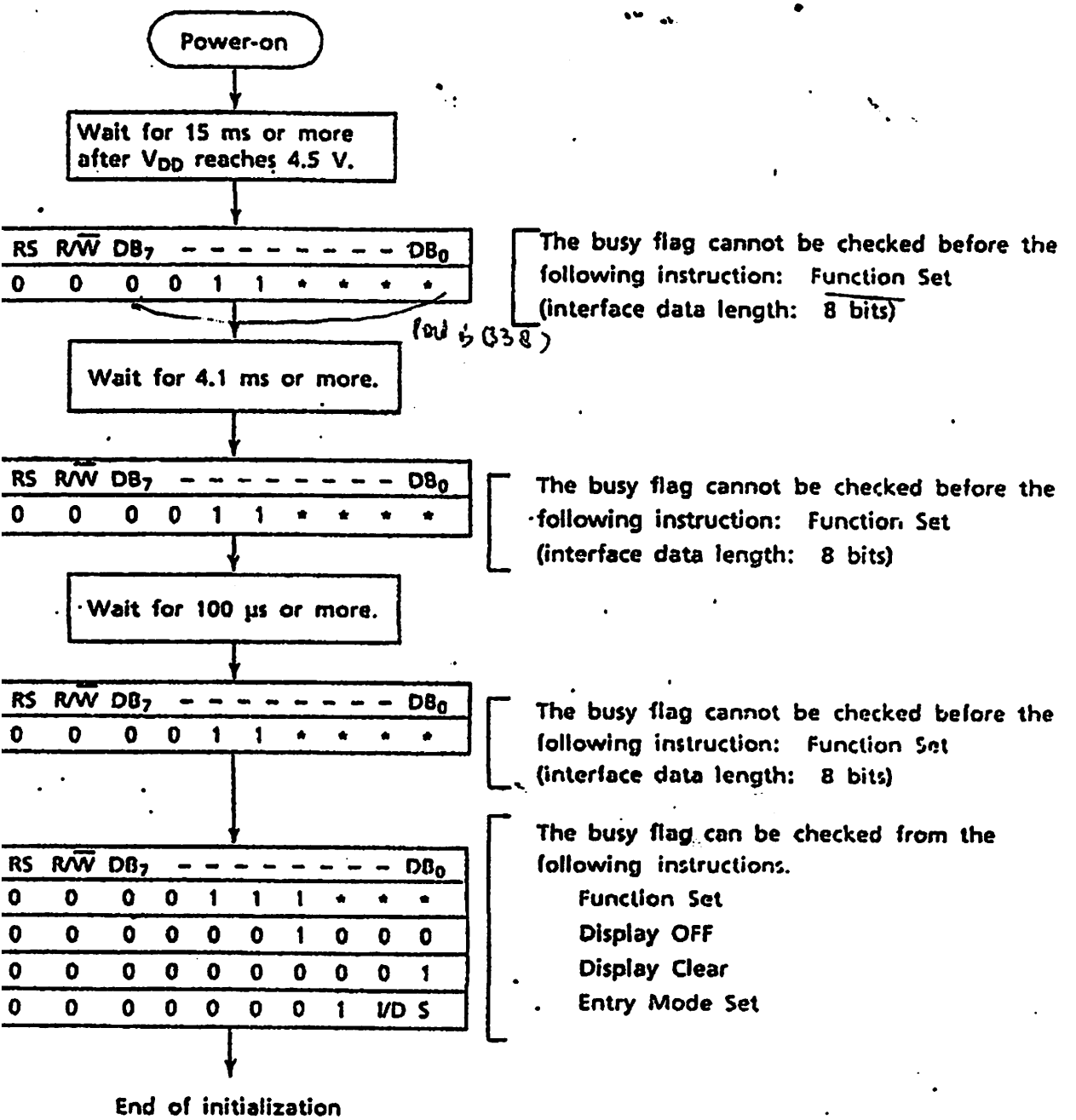
The following instructions are executed for initialization.

- 5 x 7 dot-matrix character font: 1/8 duty
- Display clear
- Function Set — DL = 1: Interface data length: 8 bits
- Display ON/OFF Control — D = 0: Display OFF; C = 0: Cursor OFF; B = 0: Blink OFF
- Entry mode — I/O = 1: Increment; S = 0: No display shift

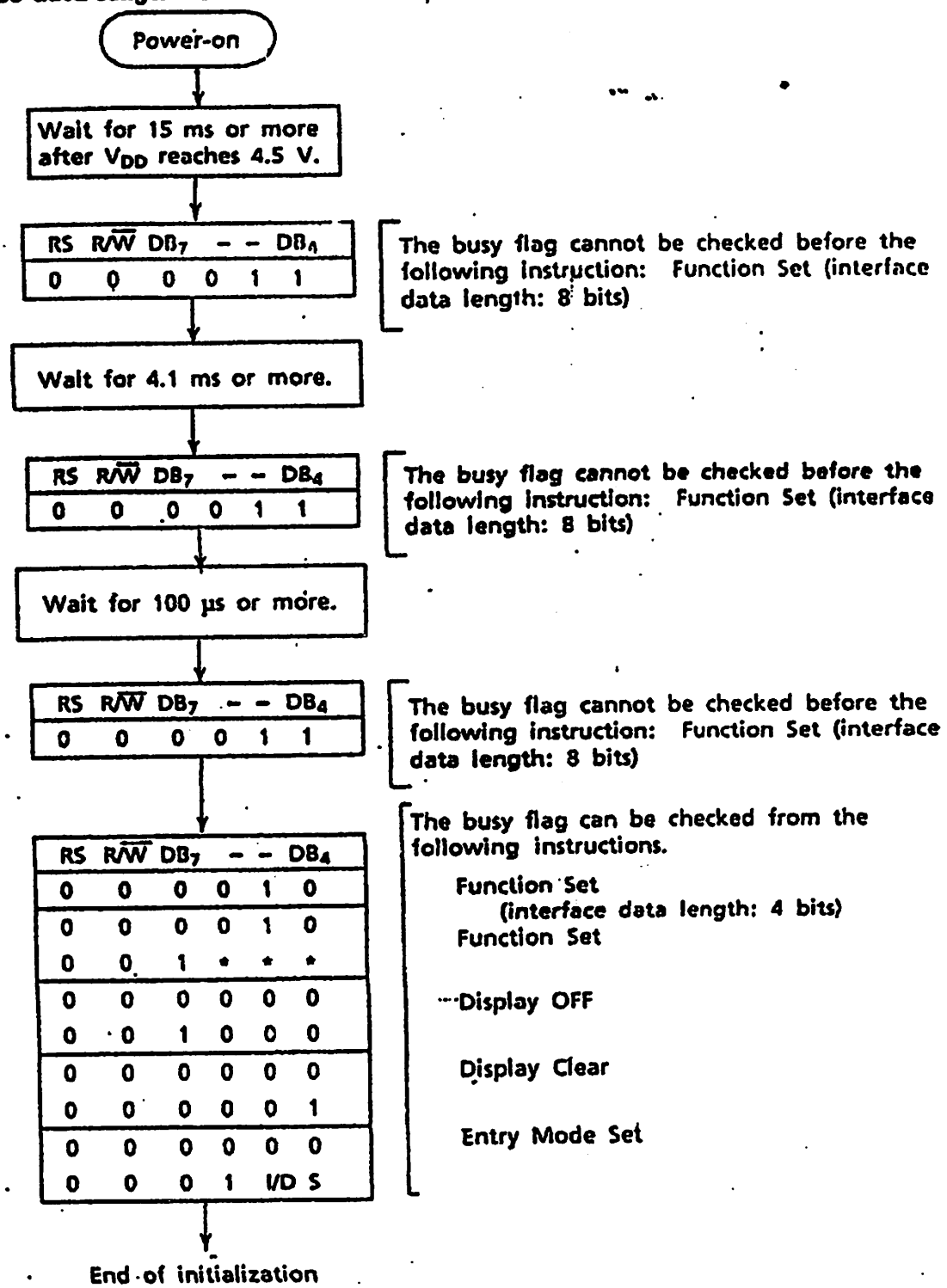
Since the condition is not suitable for the M1632, further function setting is necessary.

If automatic initialization is not executed because the above power supply conditions are not satisfied, use the instruction from next page on.

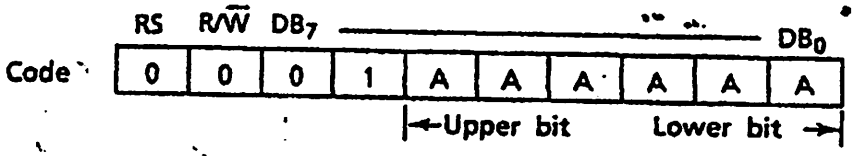
) **Interface data length : Eight bits**



Interface data length: Four bits

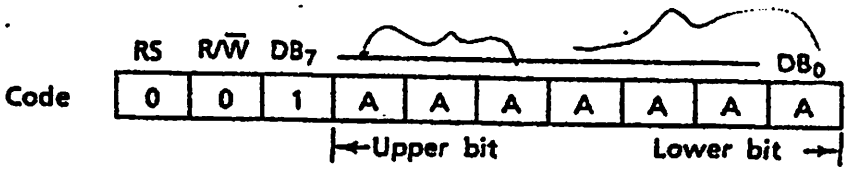


CG RAM Address Set



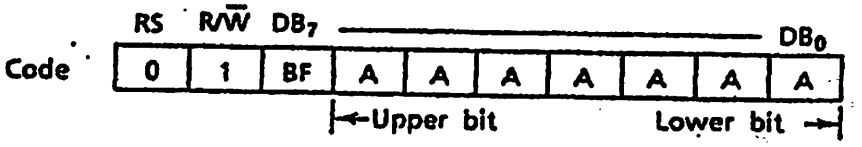
CG RAM addresses expressed as binary AAAAAA are set to the AC. Then data in CG RAM is written from or read to the MPU.

DD RAM Address Set



DD RAM addresses expressed as binary AAAAAAA are set to the AC. Then data DD RAM is written from or read to the MPU. The addresses used for display in ne 1 (AAAAAAA) are 00_H to 27_H and those for line 2 (AAAAAAA) are 40_H to 67_H.

usy Flag/Address Read



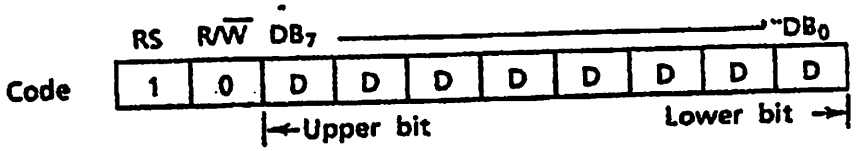
The BF signal is read out, indicating that the module is working internally because the previous instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

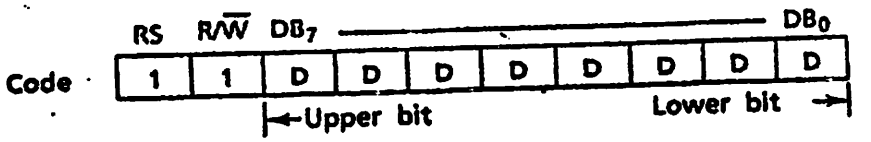
Therefore, make sure that BF = 0 before writing the next instruction. The AC lues of binary AAAAAAA are read out at the same time as reading the busy flag. ie AC addresses are used for both CG RAM and DD RAM but the address set fore execution of the instruction determines which address is to be used.

Data Write to CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is written into CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

Data Read from CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction of (7) or the DD RAM Address Set instruction of (8) before this instruction selects either RAM. In addition, either instruction (7) or (8) must be executed immediately before this instruction. If no address set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.
After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

Note : The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

Correct data is read out under the following conditions.

- An address set instruction is executed immediately before readout.
- For DD RAM, the Cursor Shift instruction is executed immediately before readout.
- The second, or later, instruction is executed in consecutive execution of read instructions.

xamples of Instruction Use

Interface data length: Eight bits

Instruction	Display	Operation
Power-on RS: —, R/W: —, DB_7 —— DB_0: —		The built-in reset circuit initializes the module.
Function Set ✓ RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 1 1 1 * * *		The interface data length is set to 8 bits. The character format becomes 5 x 7 dot-matrix at 1/16 duty cycle.
Display ON/OFF Control RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 0 0 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
Entry Mode Set RS: 0, R/W: 0, DB_7 —— DB_0: 0 0 0 0 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 0 1 1 0 0	L_	L is written. The AC is incremented by one and the cursor shifts to the right.
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 1 0 0 0 0 1 1	LC_	C is written.
⋮	⋮	
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB_7 —— DB_0: 0 0 1 1 0 0 1 0	LCD MODULE M1632	2 is written in digit 16. Cursor disappears.

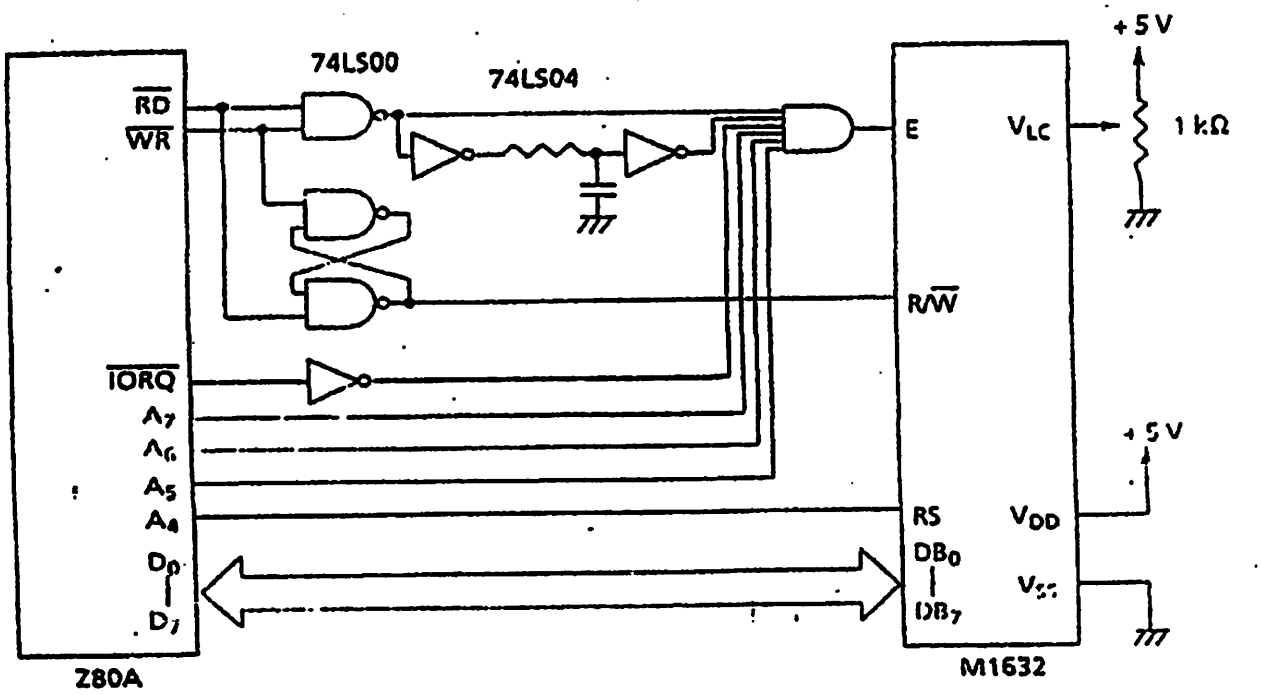
Instruction	Display	Operation
DD RAM address set RS: 0, R/W: 0, DB7 —— DB0: 1 1 0 0 0 0 0 0	LCD MODULE M1632 _	The DD RAM address is set so that the cursor appears at digit 1 of line 2.
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 —— DB0: 0 0 1 1 0 0 0 1	LCD MODULE M1632 1_	1 is written.
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 —— DB0: 0 0 1 1 0 1 1 0	LCD MODULE M1632 16_	6 is written.
⋮	⋮	
Write to CG RAM or DD RAM RS: 1, R/W: 0, DB7 —— DB0: 0 1 0 1 0 0 1 1	LCD MODULE M1632 16DIGITS,2LINES	S is written.
DD RAM address set RS: 0, R/W: 0, DB7 —— DB0: 1 0 0 0 0 0 0 0	LCD MODULE M1632 16DIGITS,2LINES	The cursor returns to the home position.
Display clear RS: 0, R/W: 0, DB7 —— DB0: 0 0 0 0 0 0 0 1	_	All the display disappears and the cursor remains at the home position.
⋮	⋮	

(2) Interface data length: Four bits

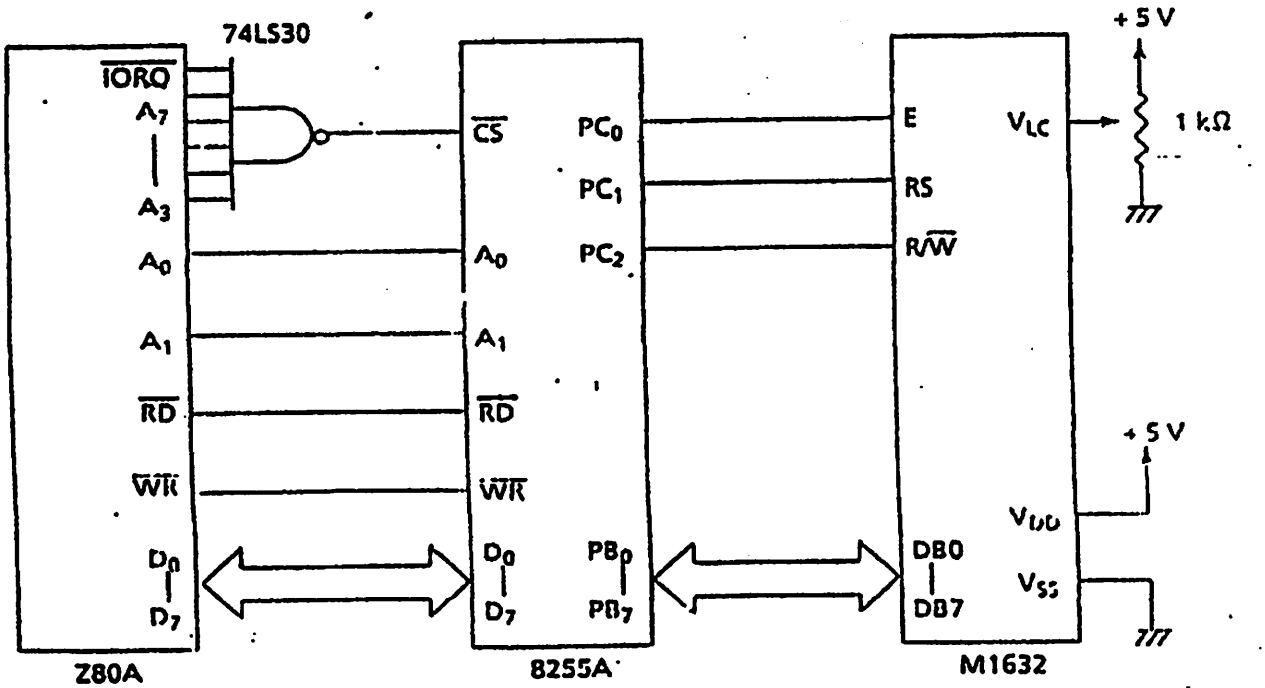
No.	Instruction	Display	Operation
1	**Power-on** RS: —, R/W: —, DB7 — DB4: —		The built-in reset circuit initializes the module.
2	**Function Set** RS: 0, R/W: 0, DB7 — DB4: 0 0 1 0		Four-bit operation mode is set. *Eight-bit operation mode is set by initialization, and the instruction is executed only once.
3	**Function Set** RS: 0, R/W: 0, DB7 — DB4: 0 0 1 0 RS: 0, R/W: 0, DB7 — DB4: 1 * * *		The 4-bit operation mode, 1/16 duty cycle, and 5 x 7 dot-matrix character format are selected. Then 4-bit operation mode starts.
4	**Display ON/OFF Control** RS: 0, R/W: 0, DB7 — DB4: 0 0 0 0 RS: 0, R/W: 0, DB7 — DB4: 1 1 1 0	_	The display and cursor are turned ON, but nothing is displayed.
5	**Entry Mode Set** RS: 0, R/W: 0, DB7 — DB4: 0 0 0 0 RS: 0, R/W: 0, DB7 — DB4: 0 1 1 0	_	The address is incremented by one and the cursor shifts to the right in a write operation to internal RAM. The display is not shifted.
6	**Write to CG RAM or DD RAM.** RS: 1, R/W: 0, DB7 — DB4: 0 1 0 0 RS: 1, R/W: 0, DB7 — DB4: 1 1 0 0	L_	L is written, the AC is incremented by one and the cursor shifts to the right.

CPU Connection Diagrams

1 Z80A



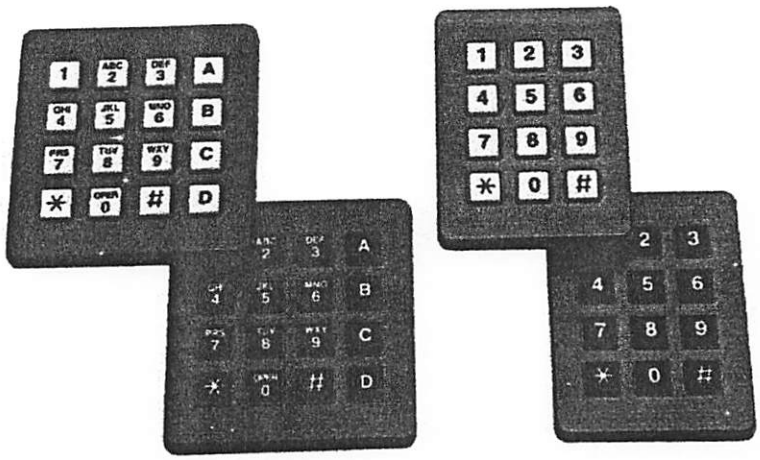
1.2 Z80A and 8255A



Grayhill

RIES 96
ductive Rubber

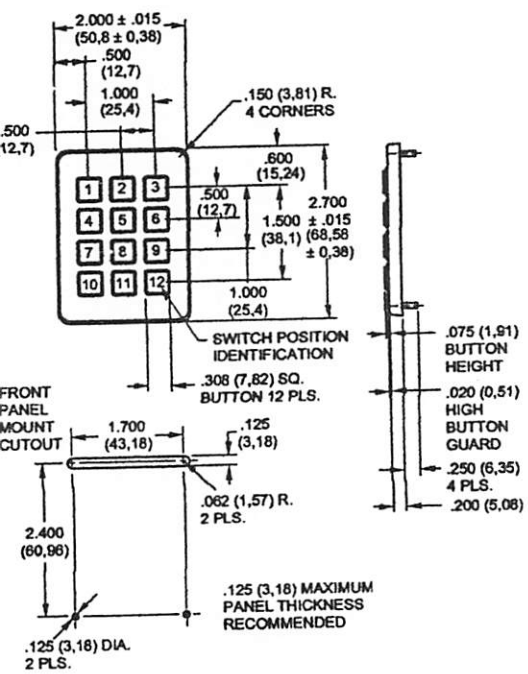
TURES
- ality, Economical Keyboards
- sily Customized Legends
- trix Circuitry
- cklit and Shielded Options
- ailable
- rmination Mates With Standard
- nnectors
- ctile Feedback to Operator
- 000,000 Operations per Button
- mpatible With High Resistance
- gic Inputs



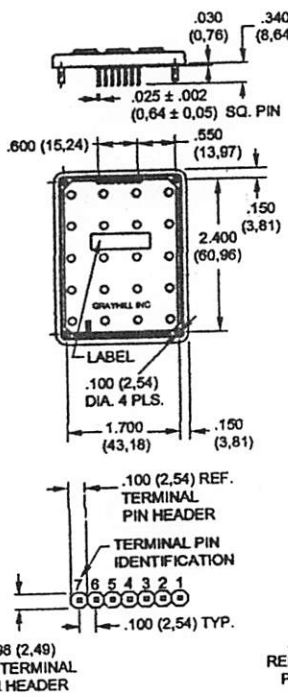
Series 96 is Grayhill's most economical 3x4 4x4 keypad family. The contact system zes conductive rubber to mate the opriate PC board traces. Offered in matrix itry, with shielded and backlit options. Built quality component parts, the Series 96 is ected to our rigid statistical process control sure that it meets our reliability standards.

MENSIONS In inches (and millimeters)

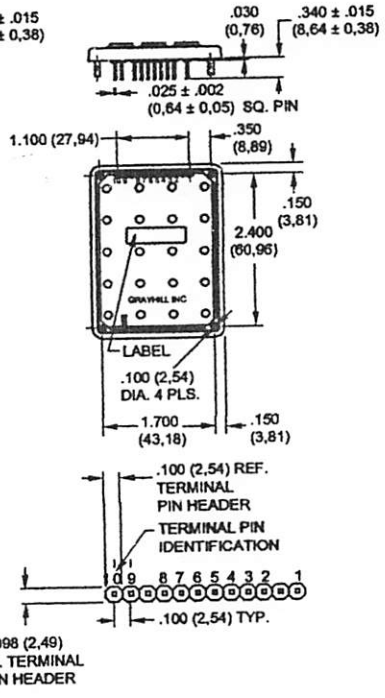
x4 Front Mount Keyboard



Standard Versions

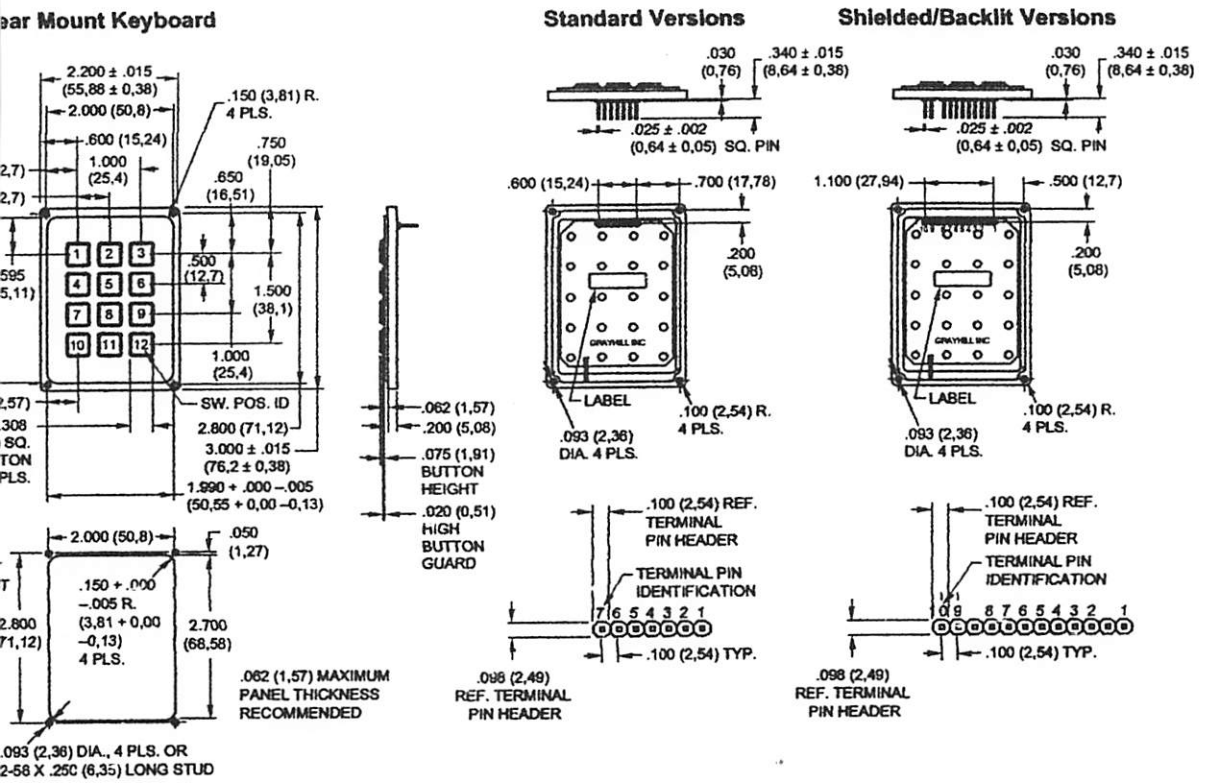


Shielded/Backlit Versions

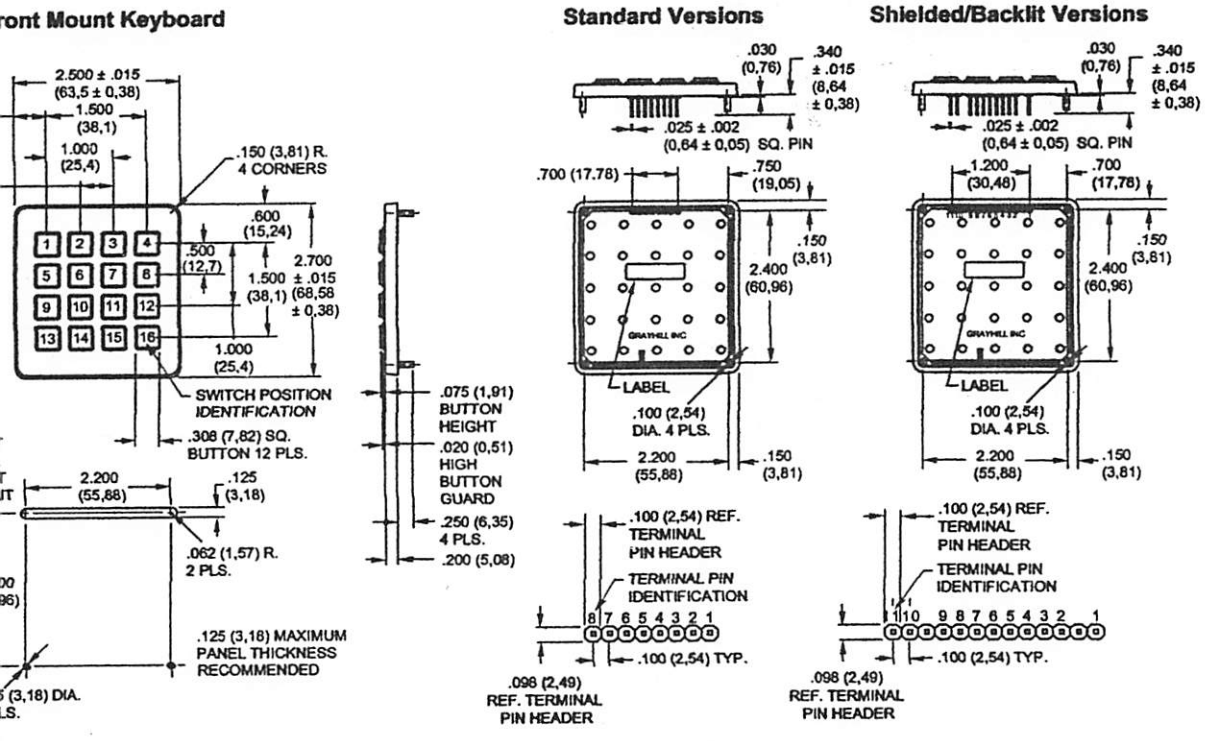


SIONS In inches (and millimeters)

ear Mount Keyboard

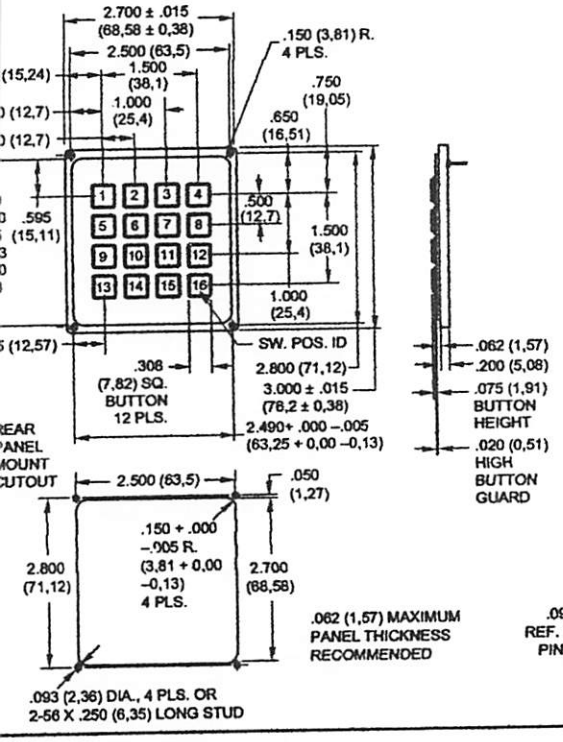


ront Mount Keyboard

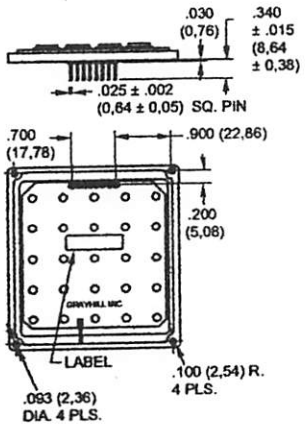


NSIONS In inches (and millimeters)

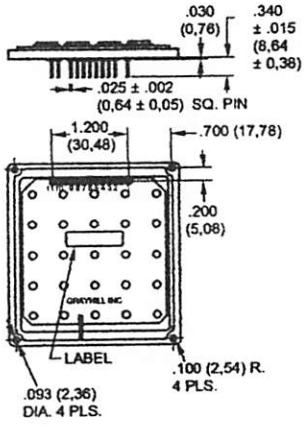
ear Mount Keyboard

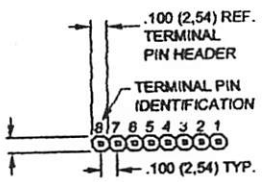


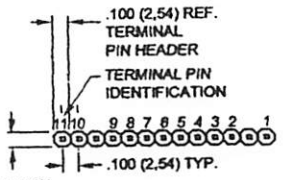
Standard Versions



Shielded/Backlit Versions



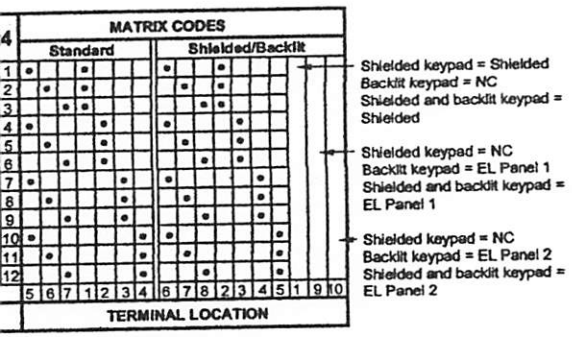




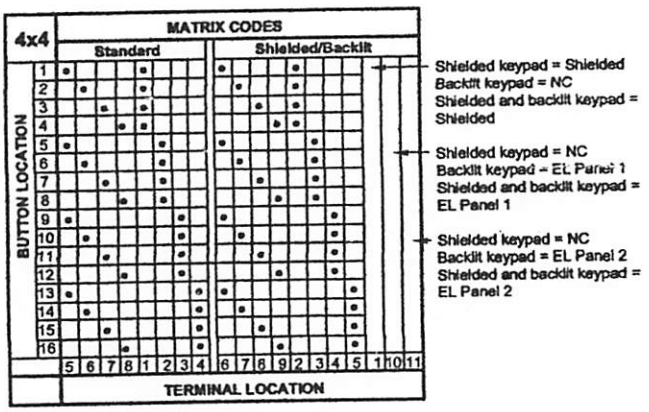
E AND TRUTH TABLES

in the chart indicate connected terminals when switch is closed.
minals are identified on the keyboard.

12 Button Keypads



16 Button Keypads



IFICATIONS

Criteria
at 12 Vdc: 5 milliamps for .5 seconds
t Bounce: < 12 milliseconds
t Resistance: < 100 ohms (at stated g force)
Breakdown: 250 Vac between ients
ical Operation Life: 1,000,000 ons per key
ion Resistance: > 10^{12} ohms @ 500 Vdc
ut Force Per Pin: 5 lbs.

ting Features
.040 minimum
ing Force: 175 ± 40 grams
ing Temperature: -30°C to +80°C

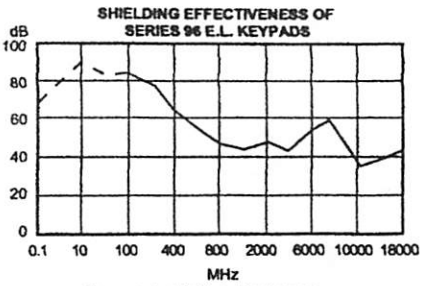
ial and Finishes
al Pin: Phosphor bronze, solder-plated
ard: FR-4 glass cloth epoxy
d: Silicone rubber, durometer 50 ± 5
g: ABS, cycolac "KJW"
g Color: Black

Shielding Effectiveness

Results shown are typical for a standard Grayhill Series 84S keyboard. A conductive gasket will generally increase the shielding, depending on the size and shape of the gasket and its material. Data derived for E-Field Radiation.

Test Method:
Measurements were made with the keyboard mounted to a brass plate, which in turn was mounted to a shielded enclosure containing the receiving equipment. A signal generator provided the frequency source that was radiated from the transmitting antenna to the enclosed receiving antenna. The spacing between antennas was maintained constant throughout the frequency range. The effectiveness rating is determined by establishing a reference reading without obstruction between the two antennas and determining the difference between that reading and the test setup reading.

Note:
When measured in actual equipment, shielding effectiveness is determined by many factors. This method accurately represents the shielding effectiveness of the Grayhill Series 84S under ideal test conditions.

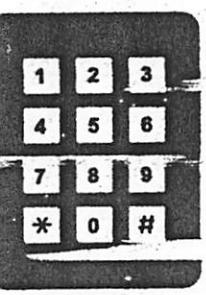


Frequency M Hz	Rating in dB
0.1	≥ 66.2
10	≥ 94.8
100	90.5
400	64.2
800	42.3
2,000	40.5
6,000	33.1
10,000	34.4
18,000	37.0

NDARD LEGENDS

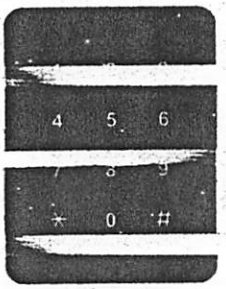
ilable through Grayhill Distributors

To order one of the configurations below, use the dash number shown here; select the keypad size and code, and order the part number with the appropriate legend dash number.

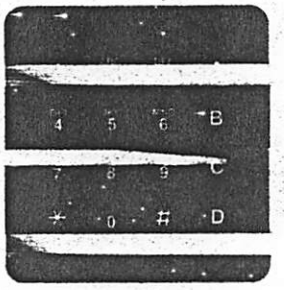


-102

-006



-152



-056

ERING INFORMATION

AB2-102-FS-EL

Grayhill Series Number
Keyboard Size: A = 3x4, B = 4x4
Circuitry: B2 = Matrix (terminal pin header)

E.L. Panel Backlighting Option
EL = Backlit, Blank = Non-backlit
EMI/RFI Shielding Option
S = Shielded, Blank = Non-shielded
Mounting Option: F = Front panel mount, R = Rear panel mount
Standard Legend Choices
12 Position legends
102 = Black legends on a white button
152 = White legends on a black button
16 Position legends
006 = Black legends on a white button
056 = White legends on a black button

Available from your local Grayhill Distributor. For prices and discounts, contact a local Sales Office, an authorized local Distributor or Grayhill.

National Semiconductor

November 2000

LM35
Precision Centigrade Temperature Sensors

General Description

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to +110°C range (−10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full −55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 µA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ω for 1 mA load

Typical Applications

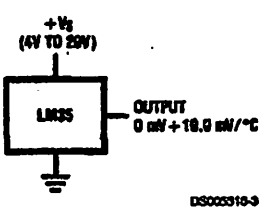
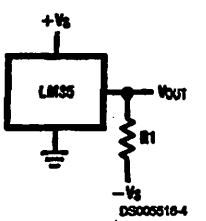


FIGURE 1. Basic Centigrade Temperature Sensor (+2°C to +150°C)

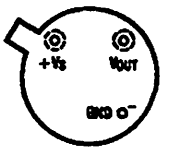


Choose $R_L = -V_S/50\ \mu A$
V_{OUT} = +1,500 mV at +150°C
= +250 mV at +25°C
= −550 mV at −55°C

FIGURE 2. Full-Range Centigrade Temperature Sensor

Connection Diagrams

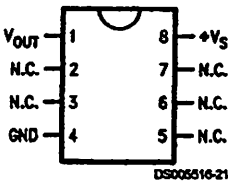
TO-46
Metal Can Package*



*Case is connected to negative pin (GND)

Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

SO-8
Small Outline Molded Package



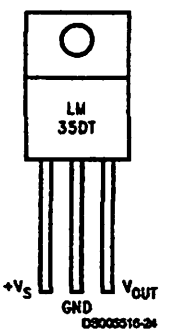
N.C. = No Connection

Top View
Order Number LM35DM
See NS Package Number M08A

TO-92
Plastic Package

Order Number LM35CZ, LM35CAZ or LM35DZ
See NS Package Number Z03A

TO-220
Plastic Package*



*Tab is connected to the negative pin (GND).
Note: The LM35DT pinout is different than the discontinued LM35DP.

Order Number LM35DT
See NS Package Number TA03F

solute Maximum Ratings (Note 10)

ilitary/Aerospace specified devices are required, se contact the National Semiconductor Sales Office/ ibutors for availability and specifications.

dy Voltage	+35V to −0.2V
ut Voltage	+6V to −1.0V
ut Current	10 mA
ge Temp.;	
-46 Package,	−60°C to +180°C
-92 Package,	−60°C to +150°C
-8 Package,	−65°C to +150°C
-220 Package,	−65°C to +150°C
Temp.:	
-46 Package, (Soldering, 10 seconds)	300°C
TO-92 and TO-220 Package, (Soldering, 10 seconds)	260°C
SO Package (Note 12)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	2500V
Specified Operating Temperature Range: T_{MIN} to T_{MAX} (Note 2)	
LM35, LM35A	−55°C to +150°C
LM35C, LM35CA	−40°C to +110°C
LM35D	0°C to +100°C

ctrical Characteristics

s 1, 6)

Parameter	Conditions	LM35A			LM35CA			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
acy	T_A=+25°C	±0.2	±0.5		±0.2	±0.5		°C
7)	T_A=−10°C	±0.3			±0.3		±1.0	°C
	T_A=T_{MAX}	±0.4	±1.0		±0.4	±1.0		°C
	T_A=T_{MIN}	±0.4	±1.0		±0.4		±1.5	°C
earity 8)	T_{MIN}≤T_A≤T_{MAX}	**±0.18**		**±0.35**	**±0.15**		**±0.3**	°C
r Gain ge Slope)	T_{MIN}≤T_A≤T_{MAX}	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°C
Regulation 3) 0≤I_L≤1 mA	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		mV/mA
	T_{MIN}≤T_A≤T_{MAX}	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
Regulation 3)	T_A=+25°C	±0.01	±0.05		±0.01	±0.05		mV/V
	4V≤V_S≤30V	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
cent Current 9)	V_S=+5V, +25°C	56	67		56	67		µA
	V_S=+5V	**105**		**131**	**91**		**114**	µA
	V_S=+30V, +25°C	56.2	68		56.2	68		µA
	V_S=+30V	**105.5**		**133**	**91.5**		**116**	µA
ge of cent Current 3)	4V≤V_S≤30V, +25°C	0.2	1.0		0.2	1.0		µA
	4V≤V_S≤30V	**0.5**		**2.0**	**0.5**		**2.0**	µA
erature icient of cent Current		**+0.39**		**+0.5**	**+0.39**		**+0.5**	µA/°C
num Temperature ated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
Term Stability	T_J=T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Electrical Characteristics

(Notes 1, 6)

Parameter	Conditions	LM35			LM35C, LM35D			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy, LM35, LM35C (Note 7)	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		°C
	T_A=−10°C	±0.5			±0.5		±1.5	°C
	T_A=T_{MAX}	±0.8	±1.5		±0.8		±1.5	°C
	T_A=T_{MIN}	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D (Note 7)	T_A=+25°C				±0.6	±1.5		°C
	T_A=T_{MAX}				±0.9		±2.0	°C
	T_A=T_{MIN}				±0.9		±2.0	°C
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	±0.3		±0.5	±0.2		±0.5	°C
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	+10.0	+9.8, +10.2		+10.0		+9.8, +10.2	mV/°C
Load Regulation (Note 3) $0 \le I_L \le 1$ mA	T_A=+25°C	±0.4	±2.0		±0.4	±2.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	±0.5		±5.0	±0.5		±5.0	mV/mA
Line Regulation (Note 3)	T_A=+25°C	±0.01	±0.1		±0.01	±0.1		mV/V
	$4V \le V_S \le 30V$	±0.02		±0.2	±0.02		±0.2	mV/V
Quiescent Current (Note 9)	V_S=+5V, +25°C	56	80		56	80		µA
	V_S=+5V	105		158	91		138	µA
	V_S=+30V, +25°C	56.2	82		56.2	82		µA
	V_S=+30V	105.5		161	91.5		141	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +25°C	0.2	2.0		0.2	2.0		µA
	$4V \le V_S \le 30V$	0.5		3.0	0.5		3.0	µA
Temperature Coefficient of Quiescent Current		+0.39		+0.7	+0.39		+0.7	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	T_J=T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Note 1: Unless otherwise noted, these specifications apply: $-55°C \le T_J \le +150°C$ for the LM35 and LM35A; $-40° \le T_J \le +110°C$ for the LM35C and LM35CA; and $0° \le T_J \le +100°C$ for the LM35D. V_S=+5Vdc and I_{LOAD}=50 µA, in the circuit of *Figure 2*. These specifications also apply from +2°C to T_{MAX} in the circuit of *Figure 1*. Specifications in boldface apply over the full rated temperature range.

Note 2: Thermal resistance of the TO-46 package is 400°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient. Thermal resistance of the small outline molded package is 220°C/W junction to ambient. Thermal resistance of the TO-220 package is 90°C/W junction to ambient. For additional thermal resistance information see table in the Applications section.

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in boldface apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

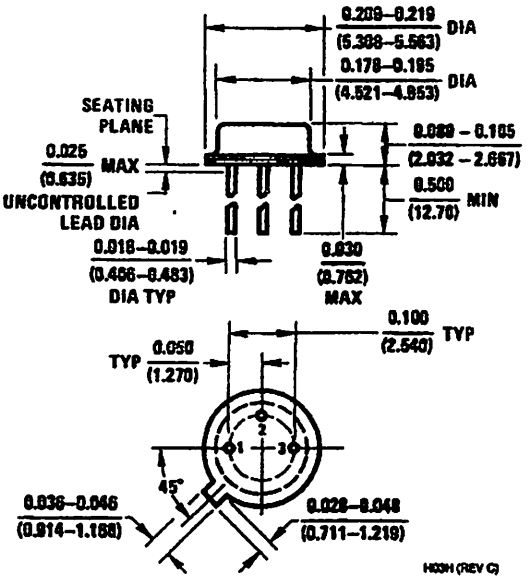
Note 9: Quiescent current is defined in the circuit of *Figure 1*.

Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

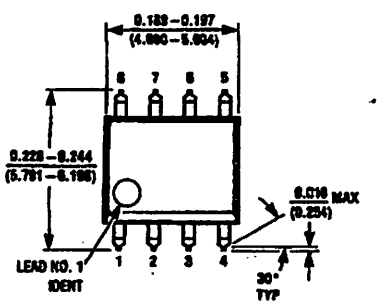
Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

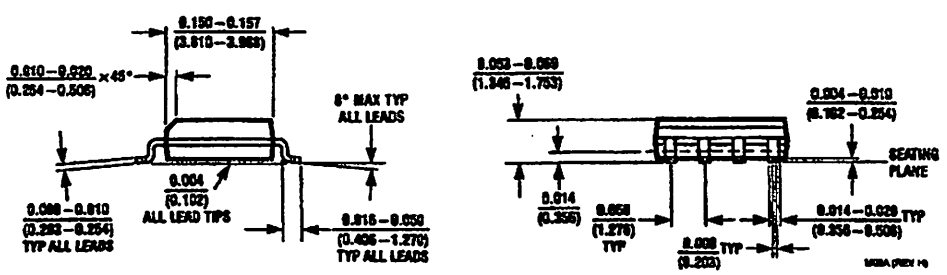
Note 12: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Physical Dimensions inches (millimeters) unless otherwise noted



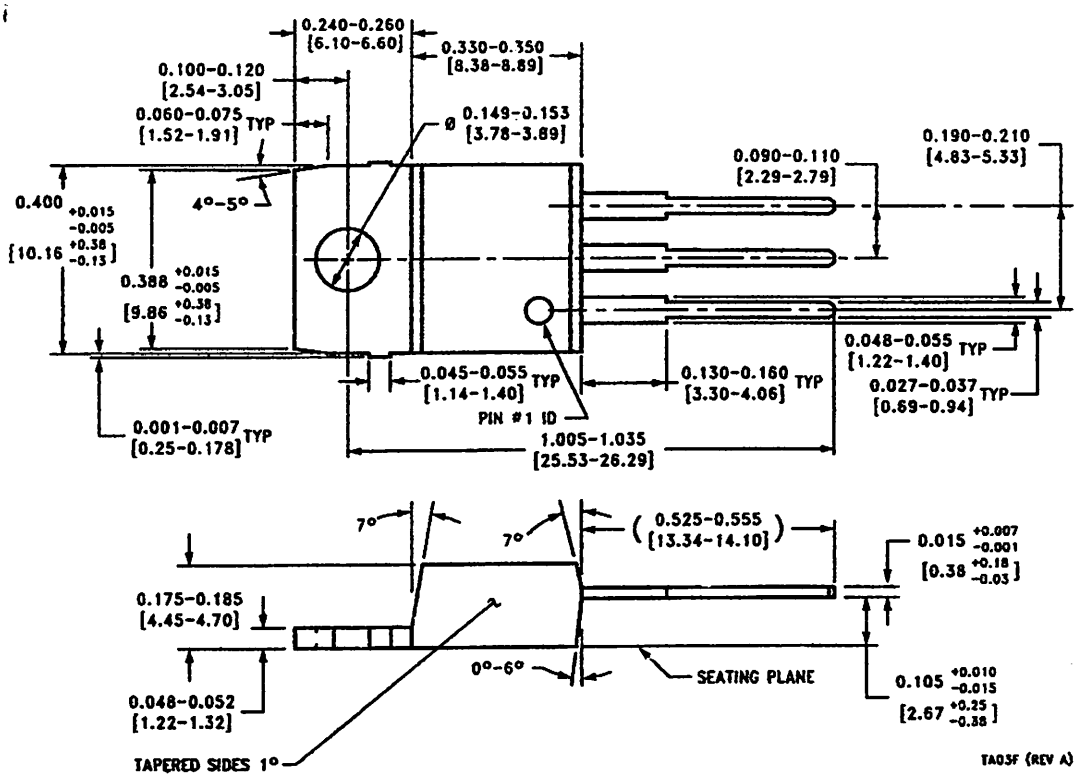
TO-46 Metal Can Package (H)
Order Number LM35H, LM35AH, LM35CH, LM35CAH, or LM35DH
NS Package Number H03H





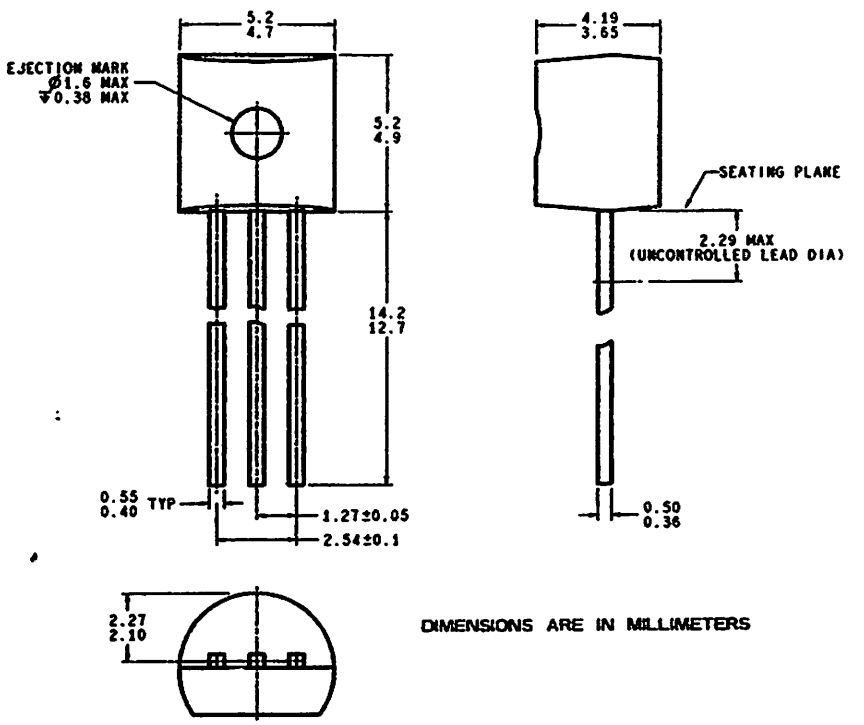
SO-8 Molded Small Outline Package (M)
Order Number LM35DM
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Power Package TO-220 (T)
Order Number LM35DT
NS Package Number TA03F

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Z03A (Rev G)

TO-92 Plastic Package (Z)
Order Number LM35CZ, LM35CAZ or LM35DZ
NS Package Number Z03A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor
Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
www.national.com

National Semiconductor
Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
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Response Group
Tel: 65-2544466
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Email: ap.support@nsc.com

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Tel: 81-3-5639-7560
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National Semiconductor

August 2000

LM741
Operational Amplifier

General Description

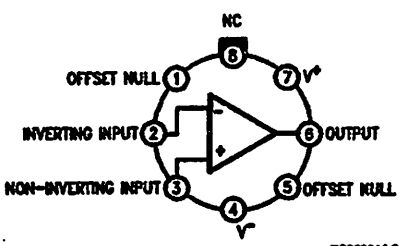
The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Connection Diagrams

Metal Can Package

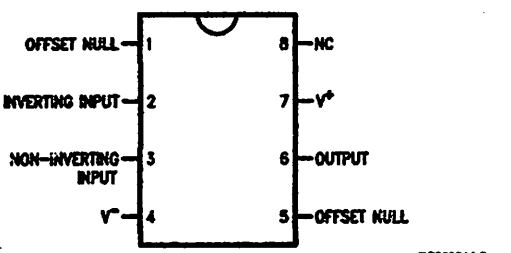


DS009341-2

Note 1: LM741H is available per JM38510/10101

Order Number LM741H, LM741H/883 (Note 1), LM741AH/883 or LM741CH
See NS Package Number H08C

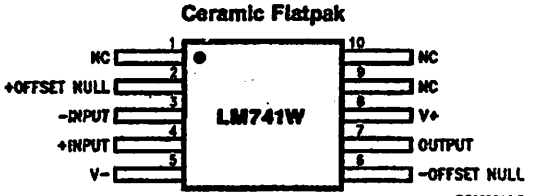
Dual-In-Line or S.O. Package



DS009341-3

Order Number LM741J, LM741J/883, LM741CN
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak

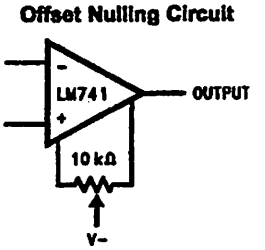


DS009341-6

Order Number LM741W/883
See NS Package Number W10A

Typical Application

Offset Nulling Circuit



DS009341-7

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 7)

	LM741A	LM741	LM741C
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V
Input Voltage (Note 4)	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	150°C	100°C
Soldering Information			
N-Package (10 seconds)	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C
M-Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 8)	400V	400V	400V

Electrical Characteristics (Note 5)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$										
	$R_S \le 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \le 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 50\Omega$			4.0							mV
	$R_S \le 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							µV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	$T_A = 25°C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V

lectrical Characteristics (Note 5) (Continued)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
e Signal Voltage Gain	T_A = 25°C, $R_L \geq 2$ kΩ										
	V_S = ±20V, V_O = ±15V	50									V/mV
	V_S = ±15V, V_O = ±10V				50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
	$R_L \geq 2$ kΩ,										
	V_S = ±20V, V_O = ±15V	32									V/mV
	V_S = ±15V, V_O = ±10V				25			15			V/mV
	V_S = ±5V, V_O = ±2V	10									V/mV
ut Voltage Swing	V_S = ±20V										
	$R_L \geq 10$ kΩ	±16									V
	$R_L \geq 2$ kΩ	±15									V
	V_S = ±15V										
	$R_L \geq 10$ kΩ				±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ				±10	±13		±10	±13		V
ut Short Circuit	T_A = 25°C	10	25	35		25			25		mA
ent	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
mon-Mode	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
ction Ratio	$R_S \leq 10$ kΩ, V_{CM} = ±12V				70	90		70	90		dB
	$R_S \leq 50$Ω, V_{CM} = ±12V	80	95								dB
ly Voltage Rejection	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
)	V_S = ±20V to V_S = ±5V										
	$R_S \leq 50$Ω	86	96								dB
	$R_S \leq 10$ kΩ				77	96		77	96		dB
sient Response	T_A = 25°C, Unity Gain										
se Time			0.25	0.8		0.3			0.3		µs
ershoot			6.0	20		5			5		%
dwidth (Note 6)	T_A = 25°C	0.437	1.5								MHz
Rate	T_A = 25°C, Unity Gain	0.3	0.7			0.5			0.5		V/µs
ly Current	T_A = 25°C					1.7	2.8		1.7	2.8	mA
er Consumption	T_A = 25°C										
	V_S = ±20V		80	150							mW
	V_S = ±15V					50	85		50	85	mW
M741A	V_S = ±20V										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
M741	V_S = ±15V										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

te 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is ctional, but do not guarantee specific performance limits.

Electrical Characteristics (Note 5) (Continued)

Note 3: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	25°C/W	N/A

Note 4: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

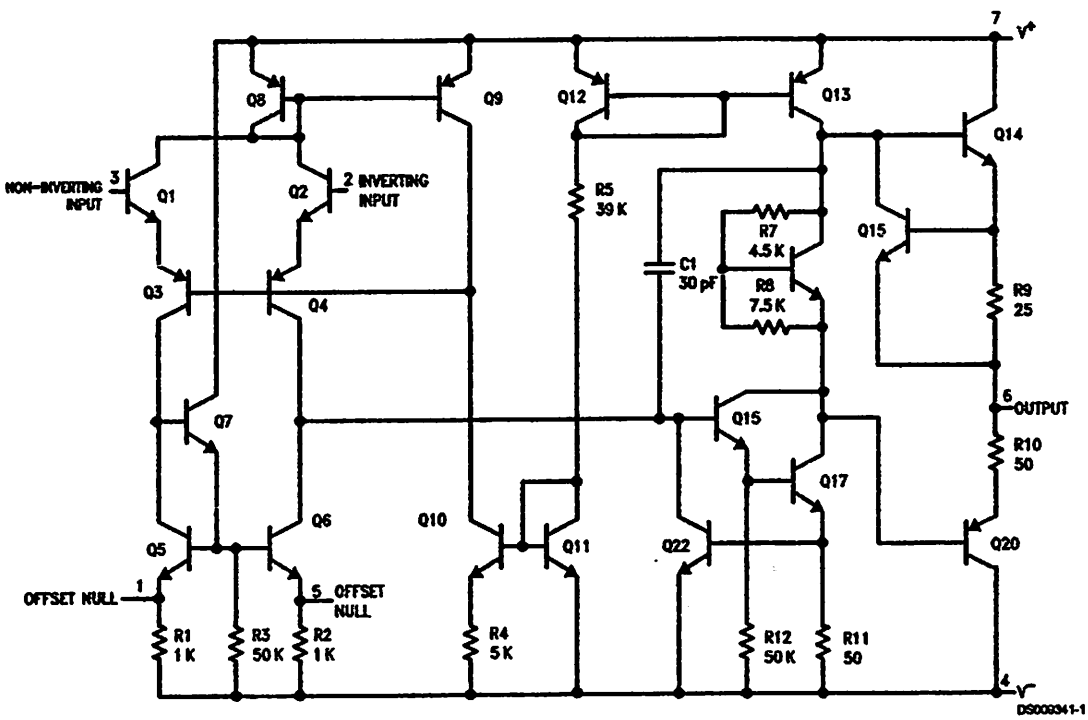
Note 5: Unless otherwise specified, these specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0°C ≤ T_A ≤ +70°C.

Note 6: Calculated value from: BW (MHz) = 0.35/Rise Time(µs).

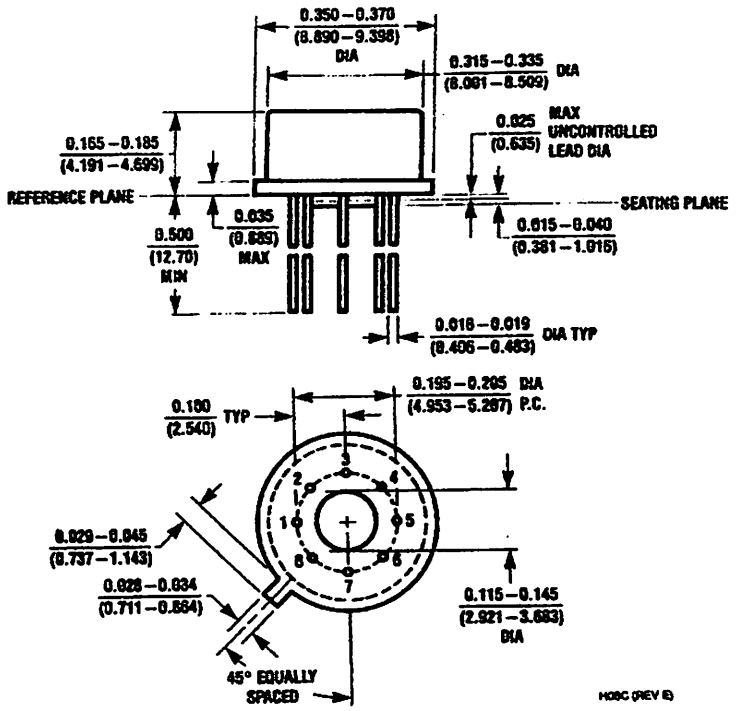
Note 7: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

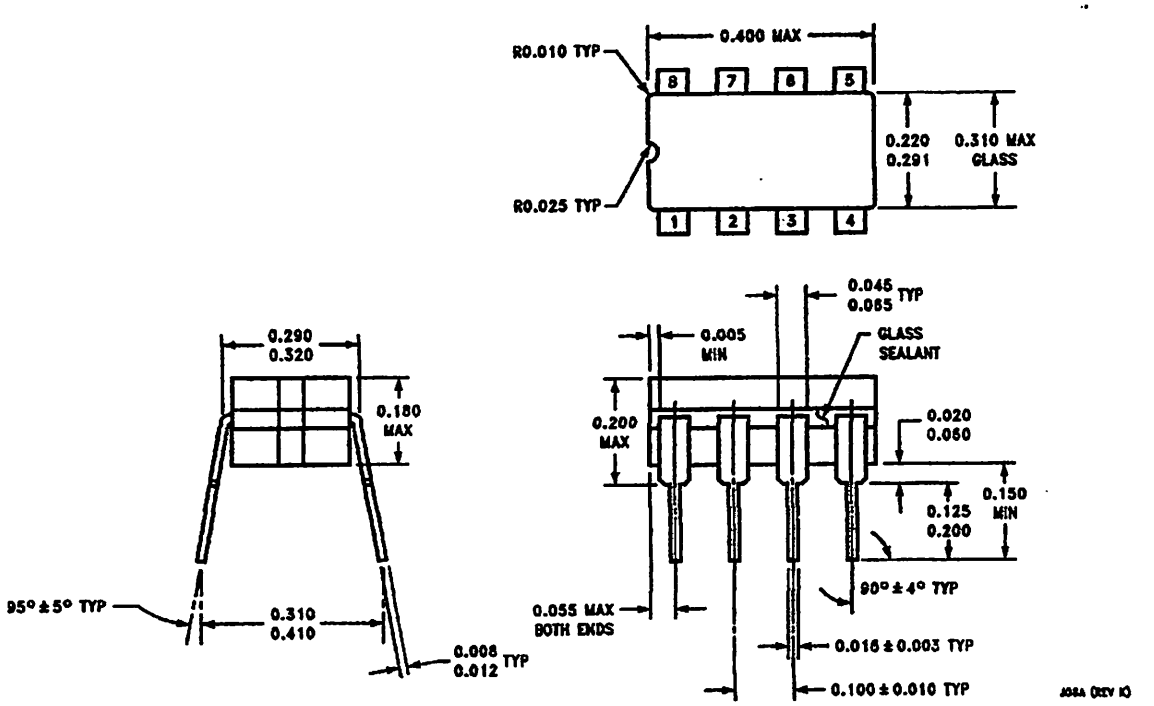
Schematic Diagram



Physical Dimensions inches (millimeters) unless otherwise noted

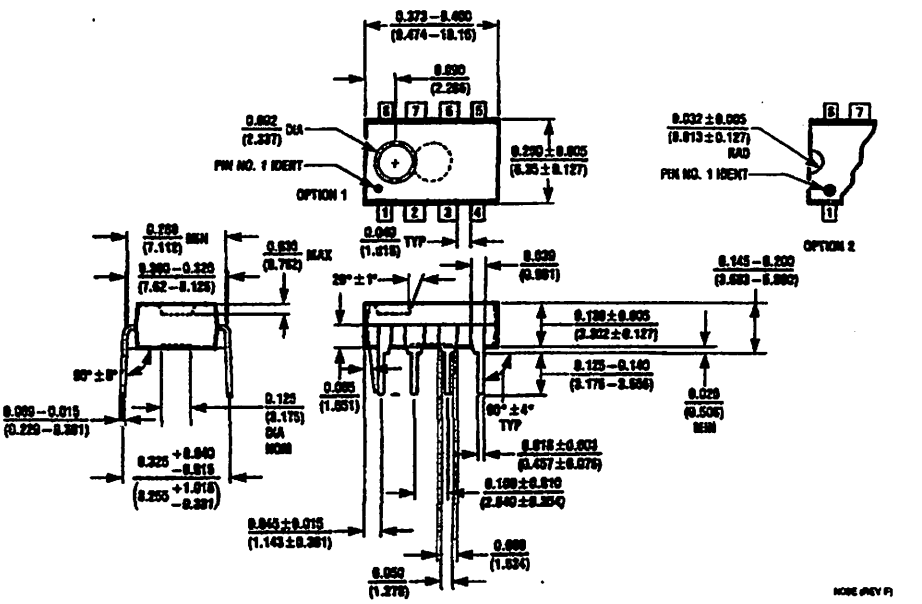


Metal Can Package (H)
Order Number LM741H, LM741H/883, LM741AH/883, LM741AH-MIL or LM741CH
NS Package Number H08C

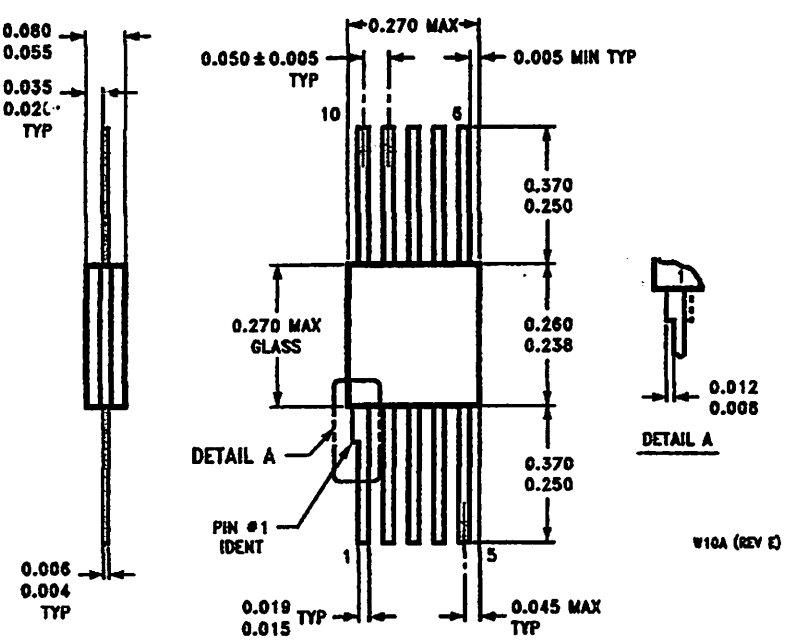


Ceramic Dual-In-Line Package (J)
Order Number LM741J/883
NS Package Number J08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Dual-In-Line Package (N)
Order Number LM741CN
NS Package Number N08E



10-Lead Ceramic Flatpak (W)
Order Number LM741W/883, LM741WG-MPR or LM741WG/883
NS Package Number W10A

Notes

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
national.com

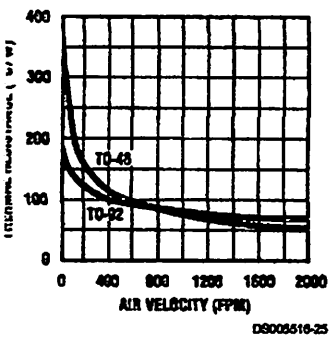
National Semiconductor
Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor
Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

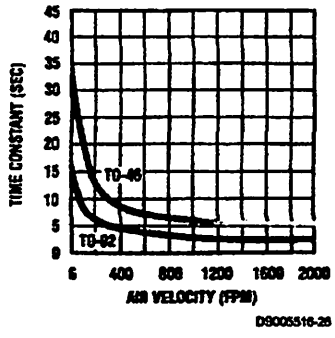
ypical Performance Characteristics

ermal Resistance
nction to Air



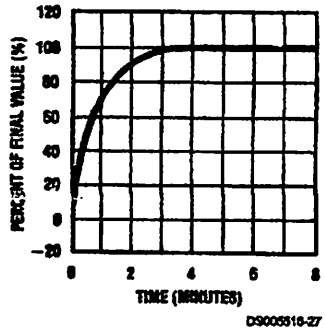
DS005516-25

Thermal Time Constant



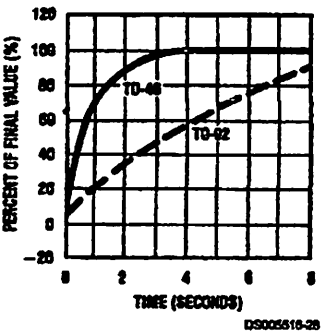
DS005516-26

Thermal Response
In Still Air



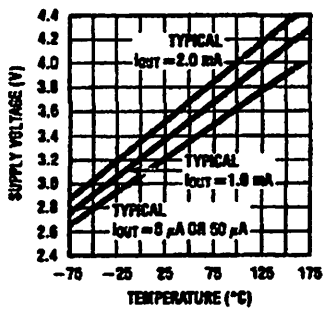
DS005516-27

ermal Response in
irred Oil Bath



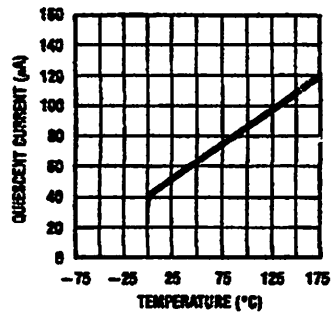
DS005516-28

Minimum Supply
Voltage vs. Temperature



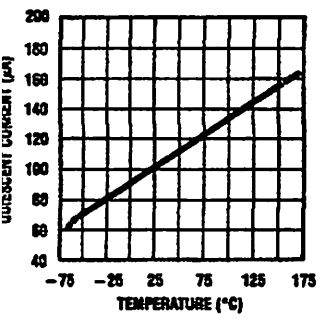
DS005516-29

Quiescent Current
vs. Temperature
(In Circuit of *Figure 1.*)



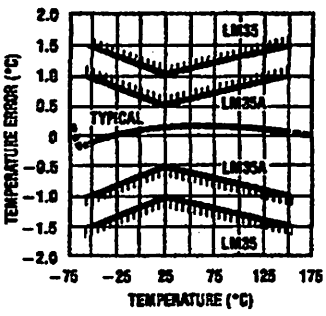
DS005516-30

lescent Current
. Temperature
Circuit of *Figure 2.*)



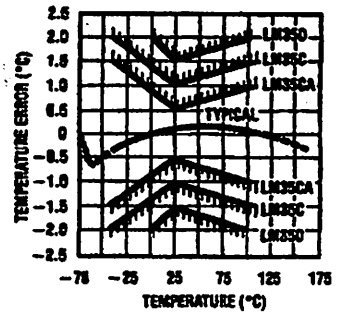
DS005516-31

Accuracy vs. Temperature
(Guaranteed)



DS005516-32

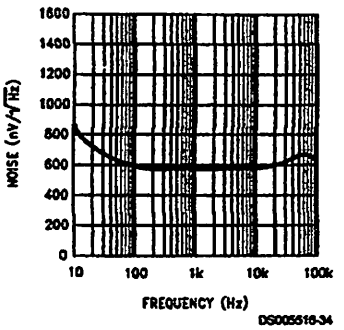
Accuracy vs. Temperature
(Guaranteed)



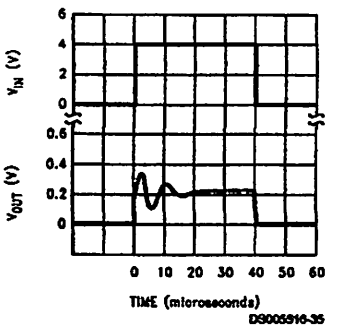
DS005516-33

Typical Performance Characteristics (Continued)

Noise Voltage



Start-Up Response



Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01°C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM35 die would be at an intermediate temperature between the surface temperature and the air temperature. This is especially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM35, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM35 die's temperature will not be affected by the air temperature.

The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course, in that case the V− terminal of the circuit will be grounded to that metal. Alternatively, the LM35 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM35 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM35 or its connections.

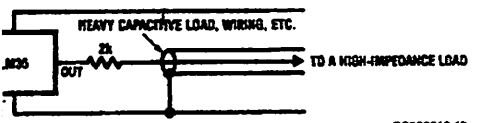
These devices are sometimes soldered to a small light-weight heat fin, to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor, to give the steadiest reading despite small deviations in the air temperature.

Temperature Rise of LM35 Due To Self-heating (Thermal Resistance, θ_{JA})

	TO-46, no heat sink	TO-46*, small heat fin	TO-92, no heat sink	TO-92**, small heat fin	SO-8 no heat sink	SO-8** small heat fin	TO-220 no heat sink
Still air	400°C/W	100°C/W	180°C/W	140°C/W	220°C/W	110°C/W	90°C/W
Moving air	100°C/W	40°C/W	90°C/W	70°C/W	105°C/W	90°C/W	26°C/W
Still oil	100°C/W	40°C/W	90°C/W	70°C/W			
Stirred oil	50°C/W	30°C/W	45°C/W	40°C/W			
(Clamped to metal, infinite heat sink)	(24°C/W)				(55°C/W)		

*Wakefield type 201, or 1" disc of 0.020" sheet brass, soldered to case, or similar.
**TO-92 and SO-8 packages glued and leads soldered to 1" square of 1/16" printed circuit board with 2 oz. foil or similar.

ical Applications



E 3. LM35 with Decoupling from Capacitive Load

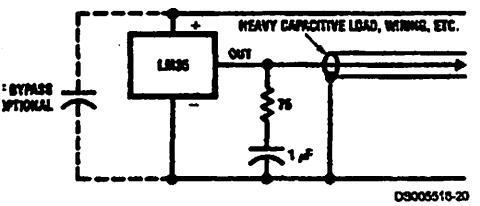
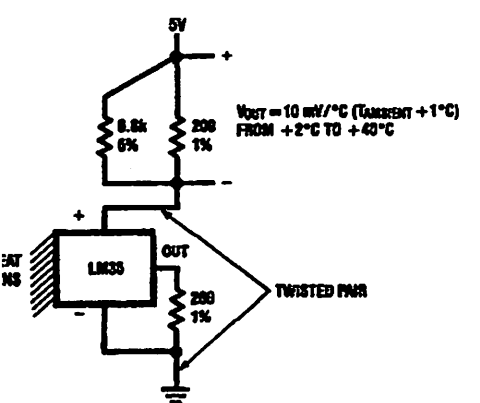


FIGURE 4. LM35 with R-C Damper

CITIVE LOADS

ost micropower circuits, the LM35 has a limited ability heavy capacitive loads. The LM35 by itself is able to 0 pf without special precautions. If heavier loads are ated, it is easy to isolate or decouple the load with a r; see *Figure 3*. Or you can improve the tolerance of tance with a series R-C damper from output to l; see *Figure 4*.

the LM35 is applied with a 200Ω load resistor as in *Figure 5*, *Figure 6* or *Figure 8* it is relatively immune ng capacitance because the capacitance forms a by- om ground to input, not on the output. However, as ny linear circuit connected to wires in a hostile envi- nt, its performance can be affected adversely by in- electromagnetic sources such as relays, radio trans- , motors with arcing brushes, SCR transients, etc, as ing can act as a receiving antenna and its internal ns can act as rectifiers. For best results in such cases, ass capacitor from V_{IN} to ground and a series R-C r such as 75Ω in series with 0.2 or 1 µF from output to l are often useful. These are shown in *Figure 13*, *14*, and *Figure 16*.



URE 5. Two-Wire Remote Temperature Sensor (Grounded Sensor)

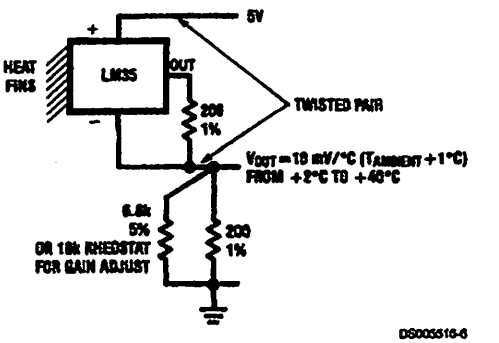


FIGURE 6. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

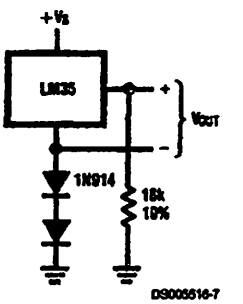


FIGURE 7. Temperature Sensor, Single Supply, −55° to +150°C

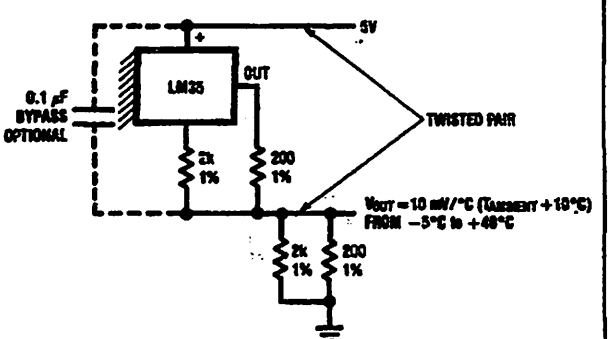


FIGURE 8. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

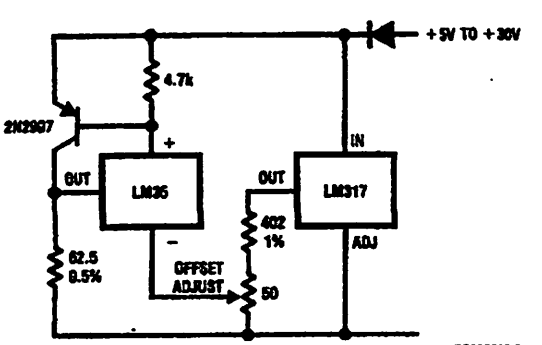


FIGURE 9. 4-To-20 mA Current Source (0°C to +100°C)

Typical Applications (Continued)

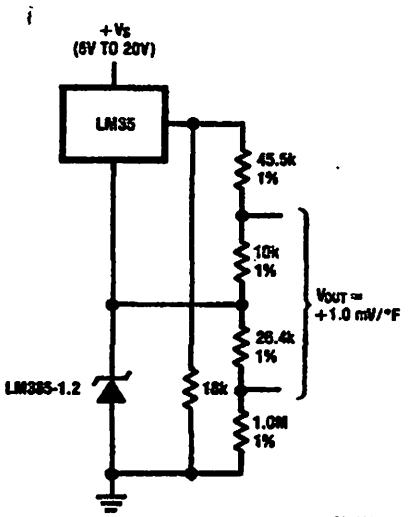


FIGURE 10. Fahrenheit Thermometer

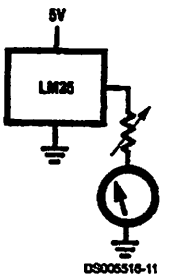


FIGURE 11. Centigrade Thermometer (Analog Meter)

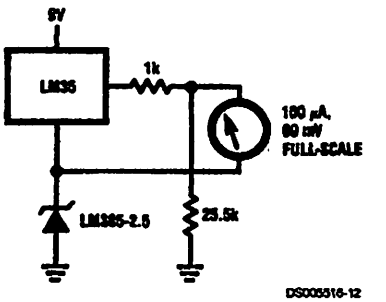


FIGURE 12. Fahrenheit ThermometerExpanded Scale Thermometer
(50° to 80° Fahrenheit, for Example Shown)

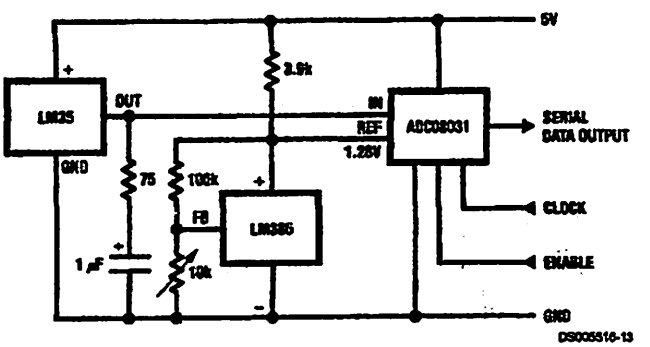


FIGURE 13. Temperature To Digital Converter (Serial Output) (+128°C Full Scale)

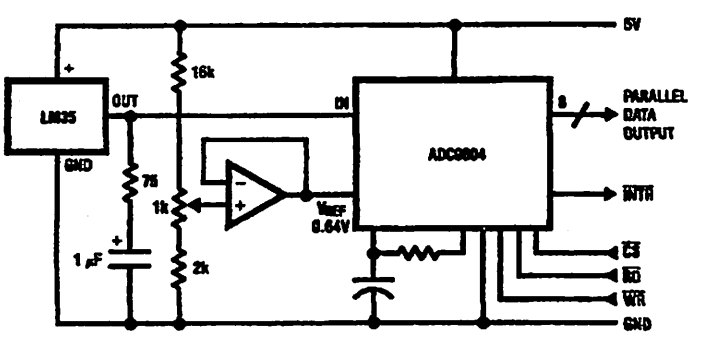
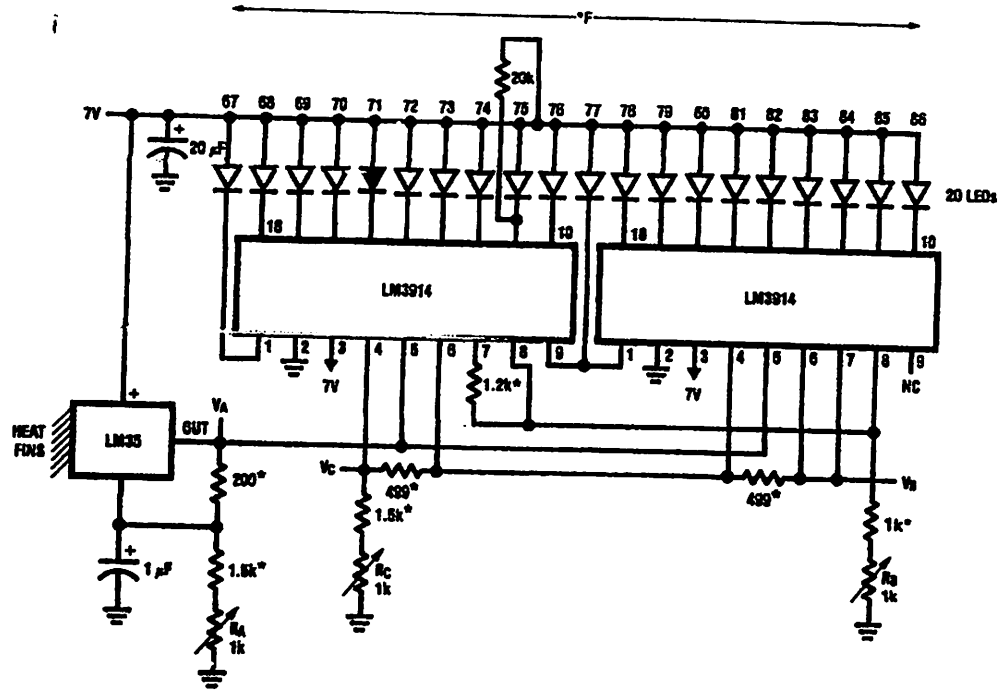


FIGURE 14. Temperature To Digital Converter (Parallel TRI-STATE™ Outputs for Standard Data Bus to µP Interface) (128°C Full Scale)

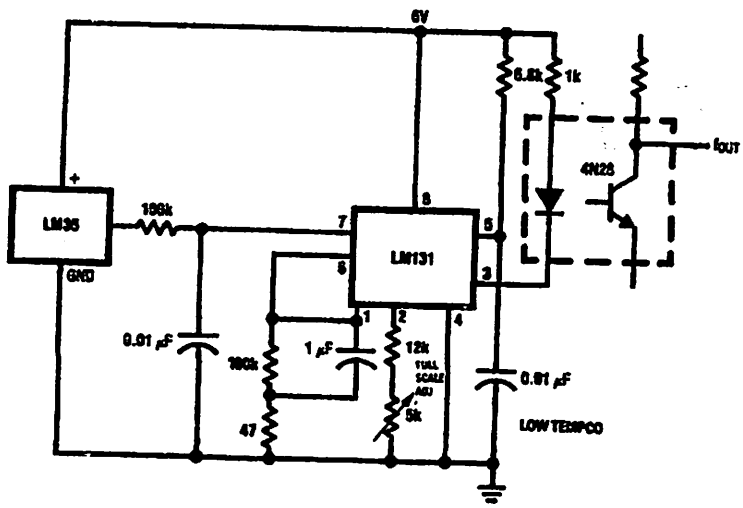
Typical Applications (Continued)



DS005516-16

*=1% or 2% film resistor
Trim R_B for V_B=3.075V
Trim R_C for V_C=1.955V
Trim R_A for V_A=0.075V + 100mV/°C x $T_{ambient}$
Example, V_A=2.275V at 22°C

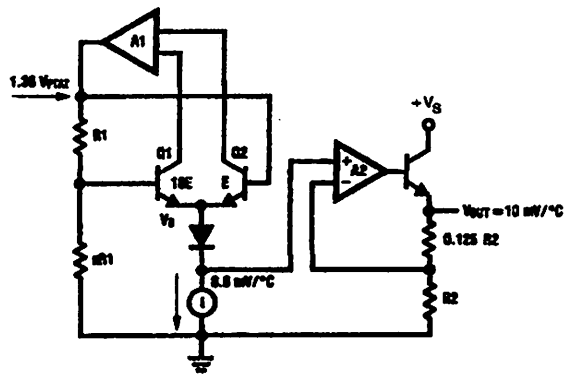
FIGURE 15. Bar-Graph Temperature Display (Dot Mode)



DS005516-15

FIGURE 16. LM35 With Voltage-To-Frequency Converter And Isolated Output (2°C to +150°C; 20 Hz to 1500 Hz)

Block Diagram



DS005516-23

National Semiconductor

December 1994

)C0801/ADC0802/ADC0803/ADC0804/ADC0805
Bit μP Compatible A/D Converters

neral Description

ADC0801, ADC0802, ADC0803, ADC0804 and 0805 are CMOS 8-bit successive approximation A/D erters that use a differential potentiometric ladder—ir to the 256R products. These converters are de-d to allow operation with the NSC800 and INS8080A ative control bus with TRI-STATE® output latches di-driving the data bus. These A/Ds appear like memory ons or I/O ports to the microprocessor and no inter-g logic is needed.

ential analog voltage inputs allow increasing the com-mode rejection and offsetting the analog zero input ge value. In addition, the voltage reference input can djusted to allow encoding any smaller analog voltage to the full 8 bits of resolution.

atures

mpatible with 8080 μP derivatives—no interfacing ic needed - access time - 135 ns

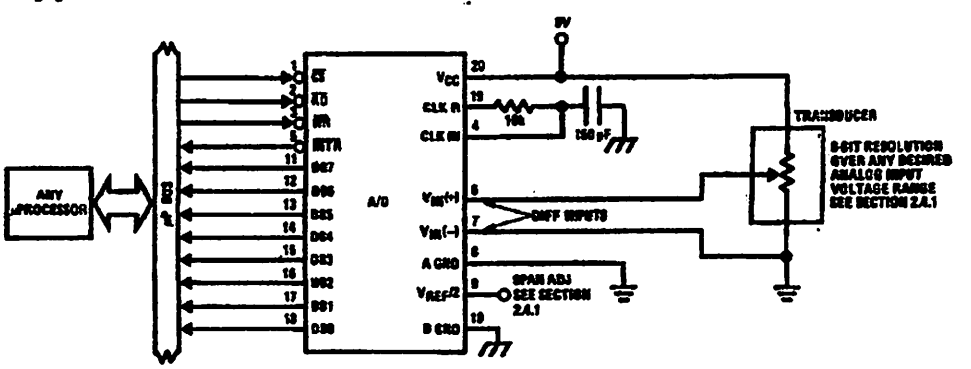
sy interface to all microprocessors, or operates tand alone"

- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

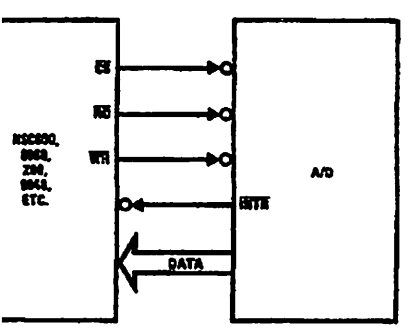
- Resolution — 8 bits
- Total error — ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time — 100 μs

ical Applications



TL/H/5671–1

8080 Interface



TL/H/5671–31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2$ = 2.500 V_{DC} (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ, ADC0802LJ/883	−55°C≤T_A≤+125°C
ADC0801/02/03/04LCJ	−40°C≤T_A≤+85°C
ADC0801/02/03/05LCN	−40°C≤T_A≤+85°C
ADC0804LCN	0°C≤T_A≤+70°C
ADC0802/03/04LCV	0°C≤T_A≤+70°C
ADC0802/03/04LCWM	0°C≤T_A≤+70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$=2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$=2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			±1	LSB
$R_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC}=5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$=0 V_{DC}, f_{CLK}=640 kHz	8770		9708	conv/s
$t_{W(WR)L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$=0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = 5V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 4.75 V_{DC}			0.8	V_{DC}
I_N (1)	Logical "1" Input Current (All Inputs)	V_{IN} = 5 V_{DC}		0.005	1	μA_{DC}
I_N (0)	Logical "0" Input Current (All Inputs)	V_{IN} = 0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T−	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O = 360 μA V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O = −360 μA V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT} = 1.6 mA, V_{CC} = 4.75 V_{DC} I_{OUT} = 1.0 mA, V_{CC} = 4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −360 μA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −10 μA, V_{CC} = 4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT} = 0 V_{DC} V_{OUT} = 5 V_{DC}	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A = 25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A = 25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	f_{CLK} = 640 kHz, $V_{REF}/2$ = NC, T_A = 25°C and $\overline{CS}$ = 5V		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, *see Figure 2 and section 2.0.*

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

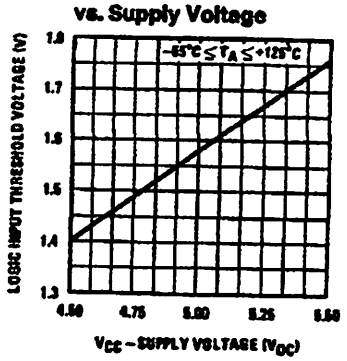
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5.*

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

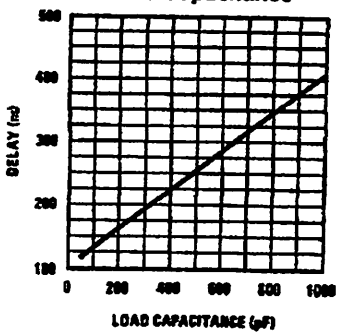
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

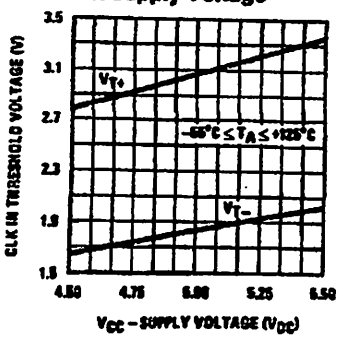
Logic Input Threshold Voltage vs. Supply Voltage



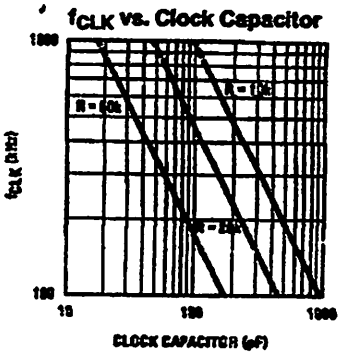
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



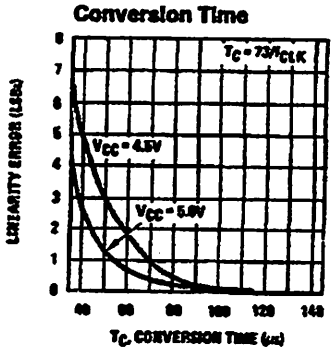
CLK IN Schmitt Trip Levels vs. Supply Voltage



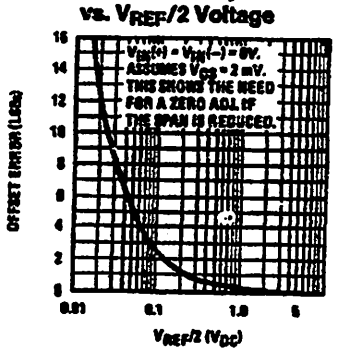
f_{CLK} vs. Clock Capacitor



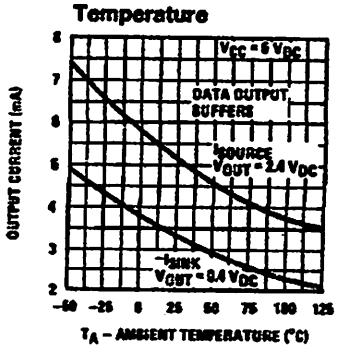
Full-Scale Error vs Conversion Time



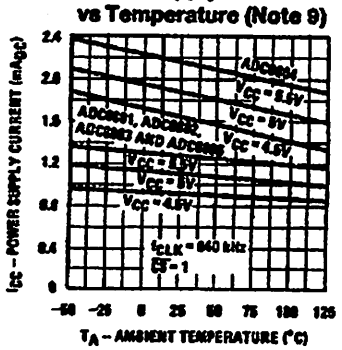
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



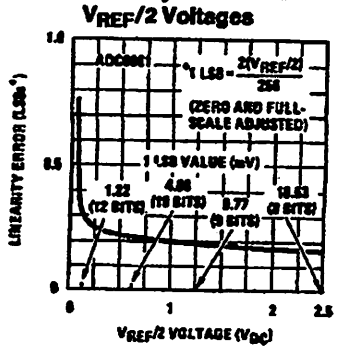
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)

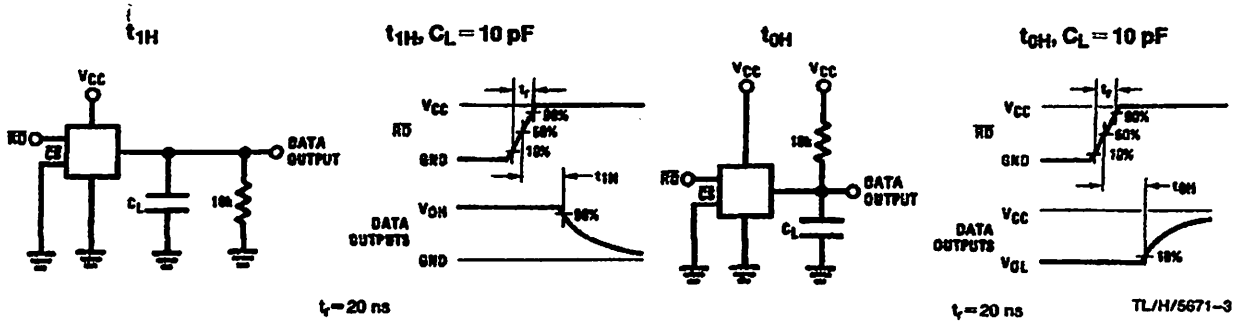


Linearity Error at Low $V_{REF}/2$ Voltages



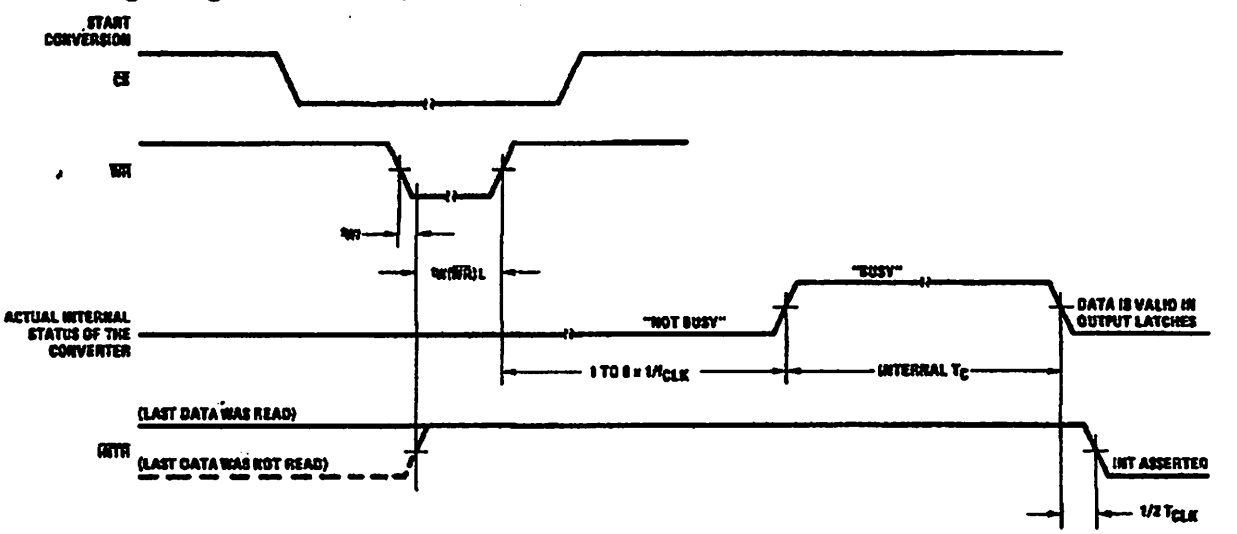
TL/H/5671–2

TRI-STATE Test Circuits and Waveforms

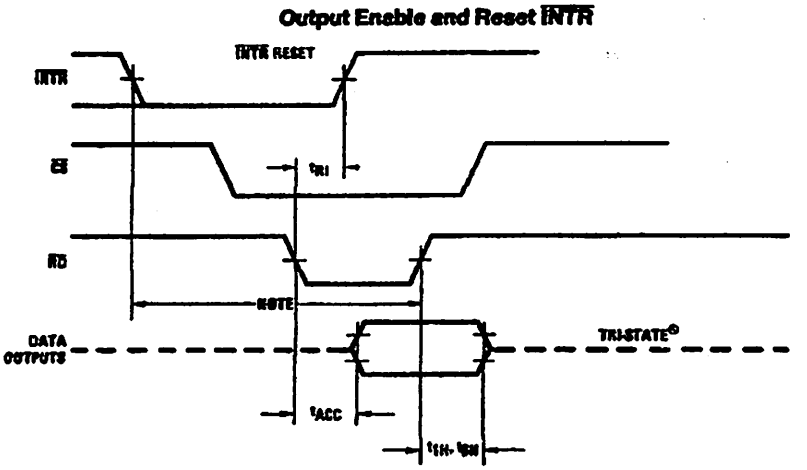


TL/H/5671–3

Timing Diagrams (All timing is measured from the 50% voltage points)



Output Enable and Reset $\overline{INTR}$

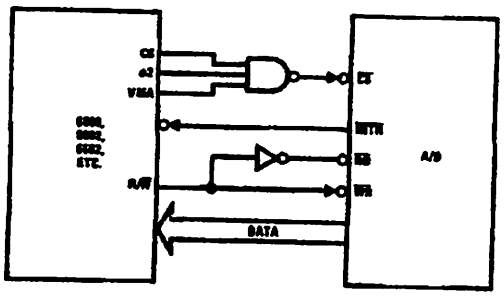


Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

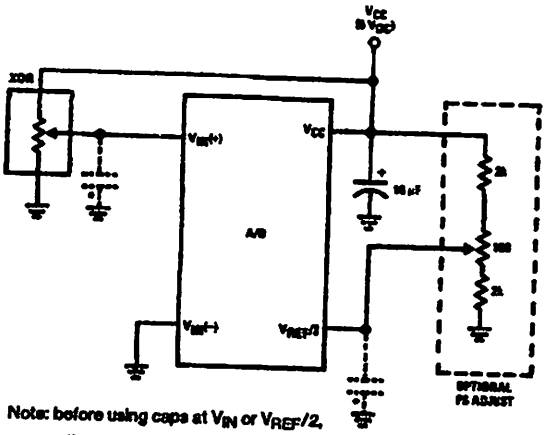
TL/H/5671–4

Typical Applications (Continued)

6800 Interface

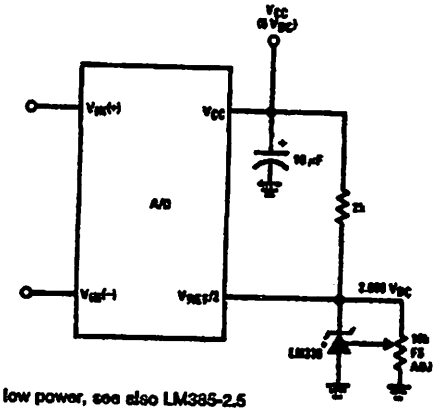


Ratiometric with Full-Scale Adjust



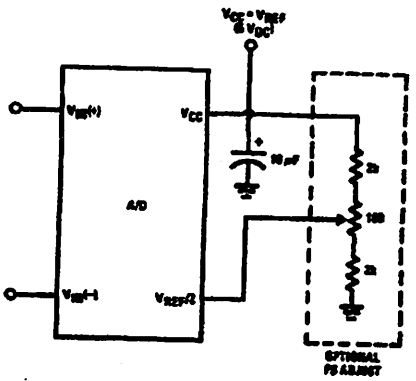
Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

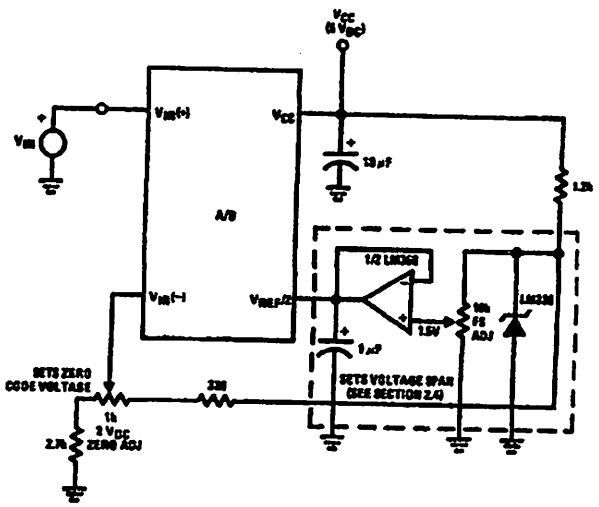


*For low power, see also LM385-2.5

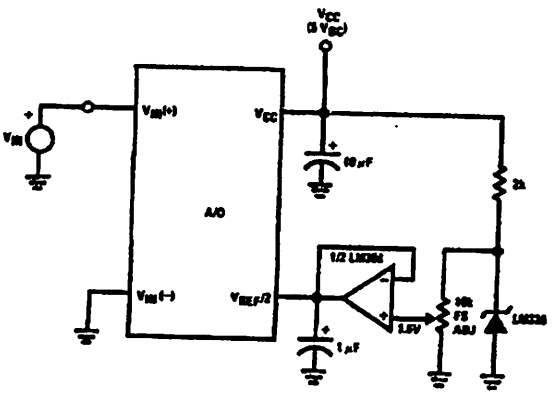
Absolute with a 5V Reference



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



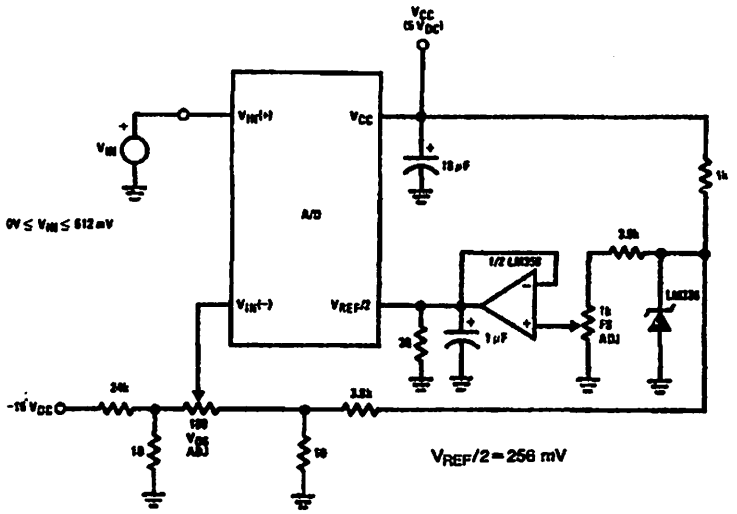
Span Adjust: $0V \leq V_{IN} \leq 3V$



TL/H/5671–5

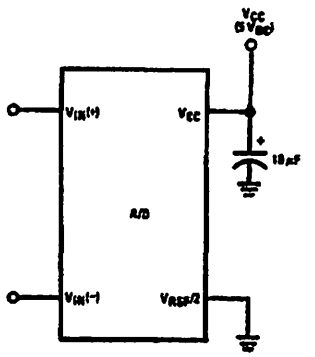
Typical Applications (Continued)

Directly Converting a Low-Level Signal



$V_{REF}/2 = 256$ mV

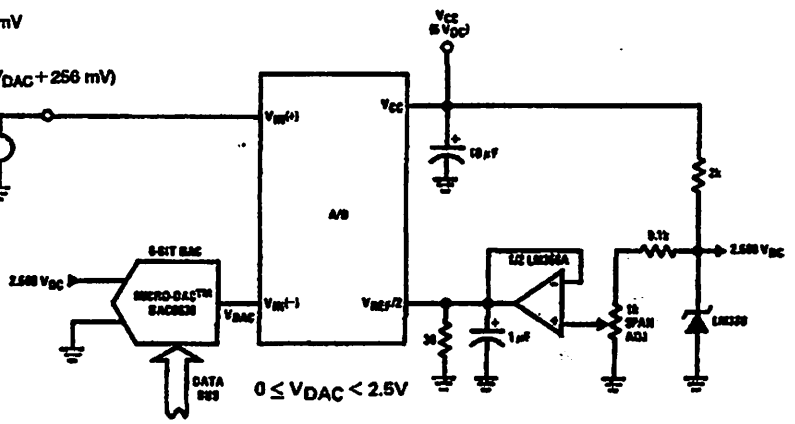
A µP Interfaced Comparator



For: $V_{IN}(+) > V_{IN}(-)$
Output = FF_{HEX}
For: $V_{IN}(+) < V_{IN}(-)$
Output = 00_{HEX}

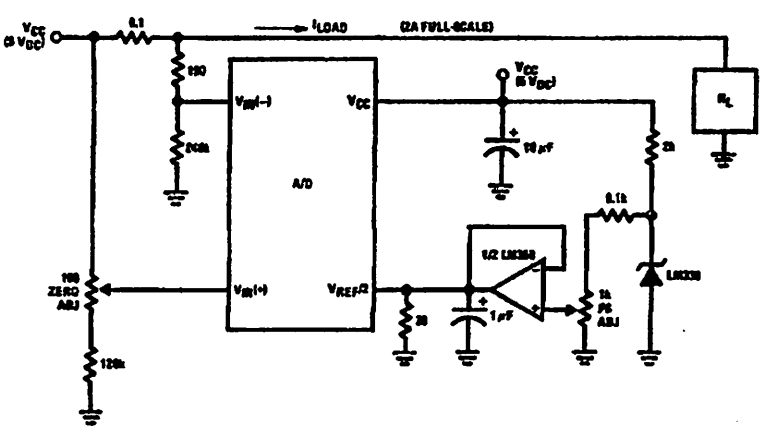
1 mV Resolution with µP Controlled Range

$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC} + 256$ mV)



$0 \leq V_{DAC} < 2.5V$

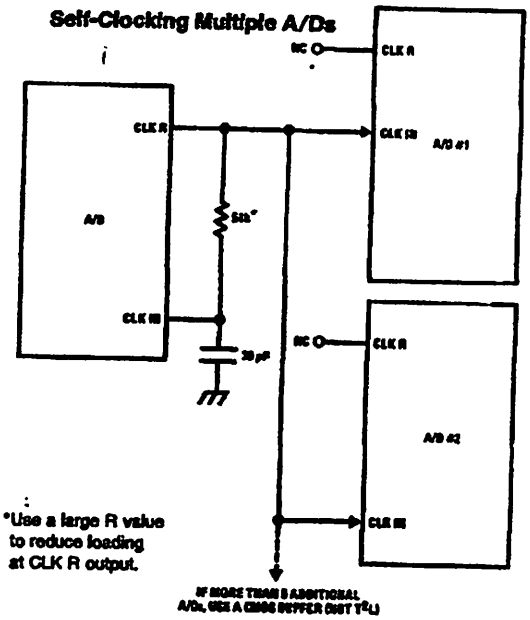
Digitizing a Current Flow



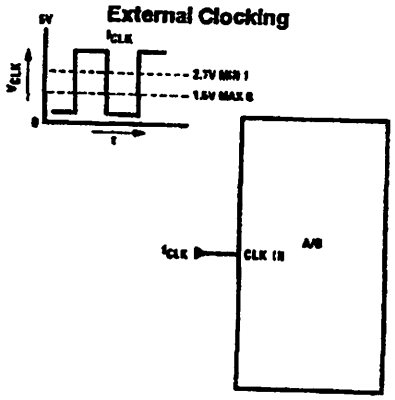
TL/H/5671–6

Typical Applications (Continued)

Self-Clocking Multiple A/Ds

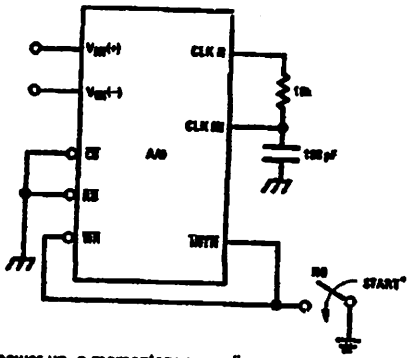


External Clocking



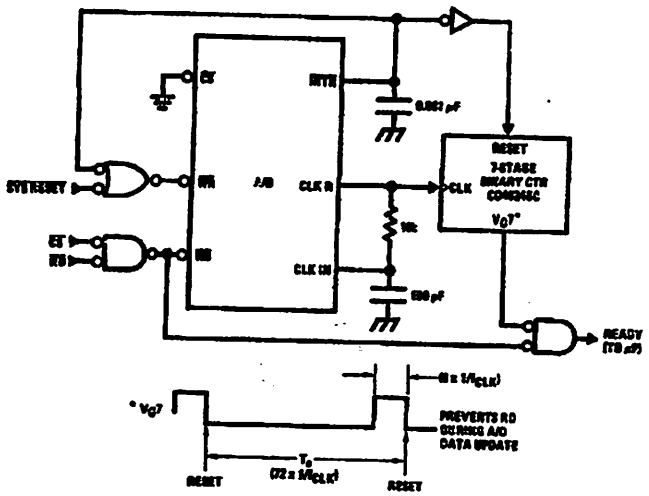
100 kHz ≤ f_{CLK} ≤ 1460 kHz

Self-Clocking in Free-Running Mode

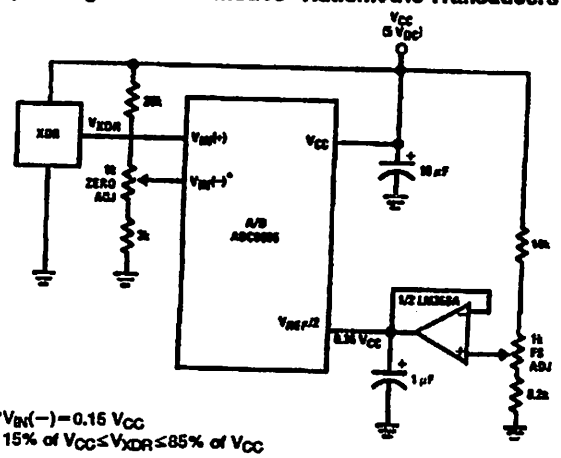


*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

µP Interface for Free-Running A/D

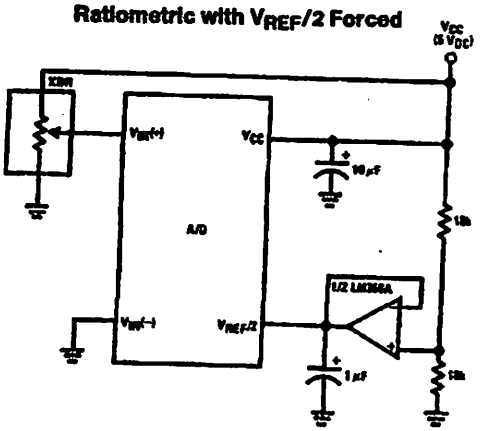


Operating with "Automotive" Ratiometric Transducers



*$V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

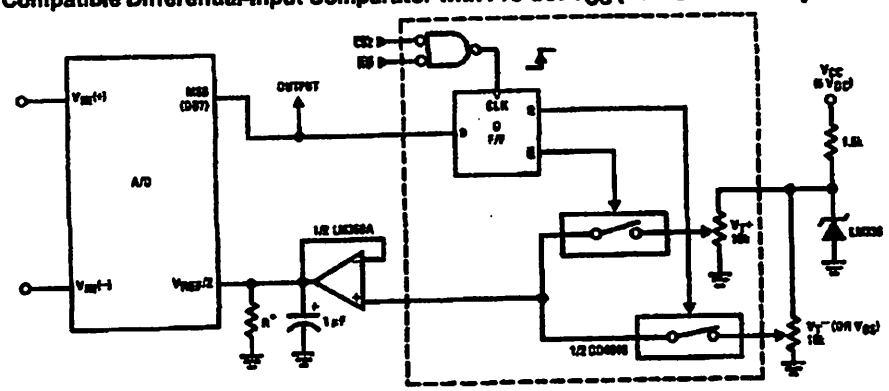
Ratiometric with $V_{REF}/2$ Forced



TL/H/5671–7

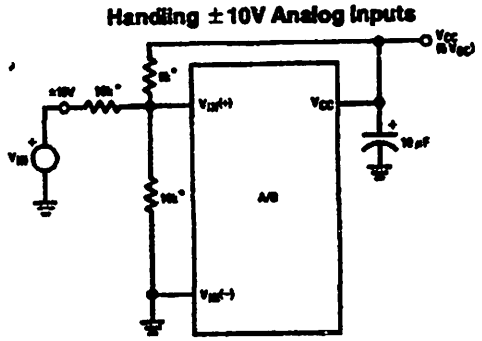
Typical Applications (Continued)

μP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)



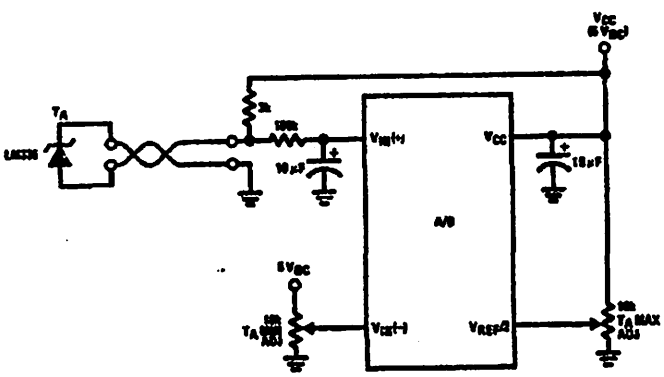
*See *Figure 5* to select R value
DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

Handling ±10V Analog Inputs

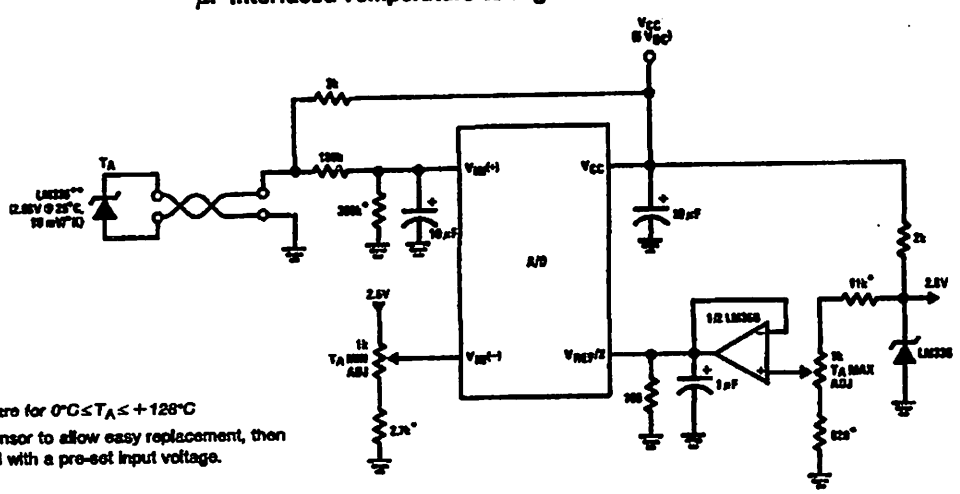


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, μP Interfaced, Temperature-to-Digital Converter



μP Interfaced Temperature-to-Digital Converter

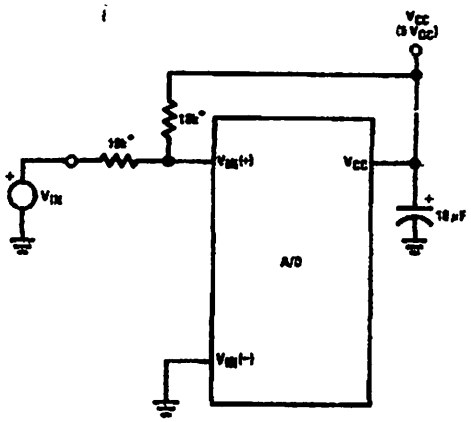


*Circuit values shown are for $0°C \leq T_A \leq +126°C$
**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

TL/H/5671–8

Typical Applications (Continued)

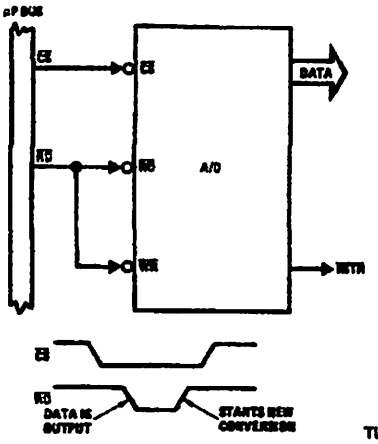
Handling ±5V Analog Inputs



TL/H/5671–33

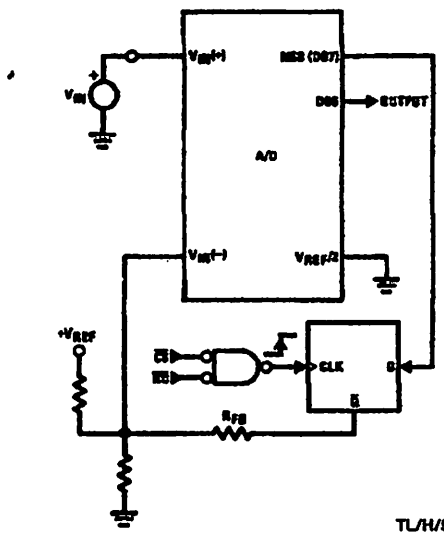
*Beckman Instruments #694-3-R10K resistor array

Read-Only Interface



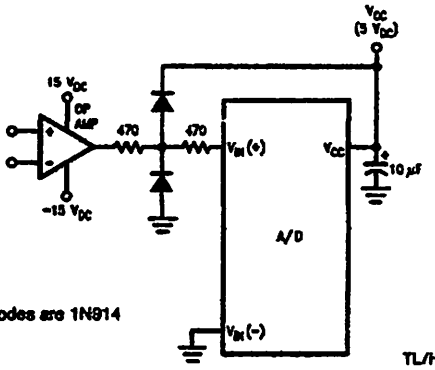
TL/H/5671–34

µP Interfaced Comparator with Hysteresis



TL/H/5671–35

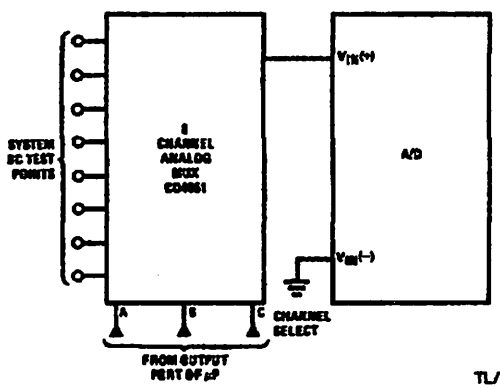
Protecting the Input



Diodes are 1N914

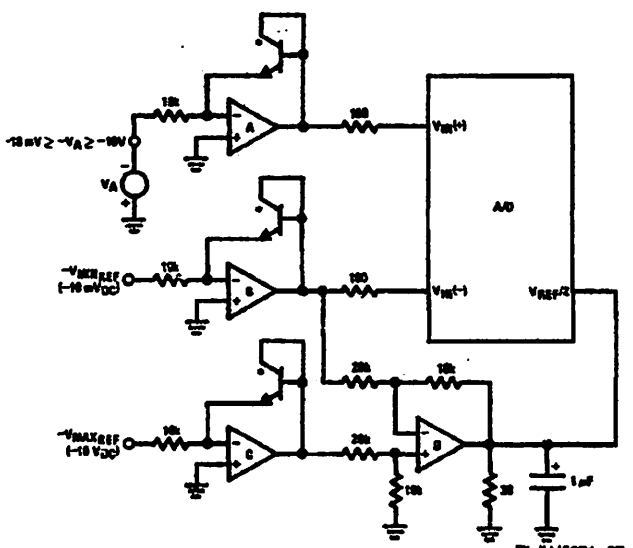
TL/H/5671–8

Analog Self-Test for a System



TL/H/5671–36

A Low-Cost, 3-Decade Logarithmic Converter



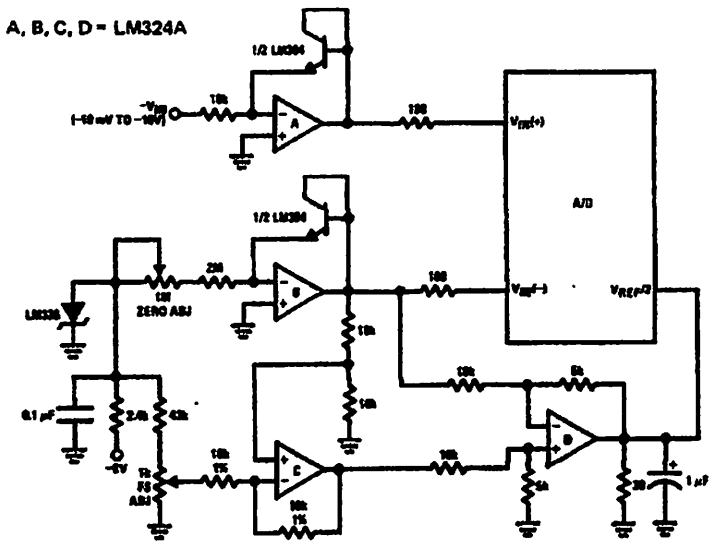
*LM389 transistors

A, B, C, D = LM324A quad op amp

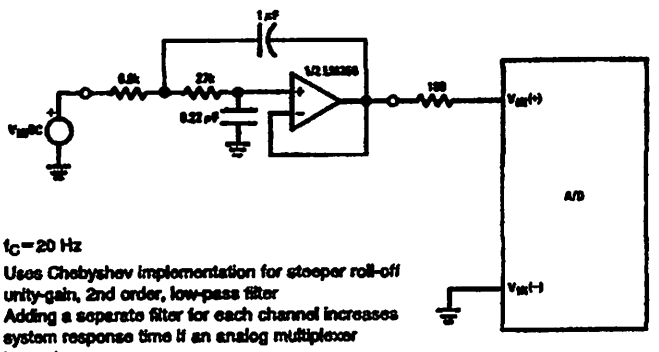
TL/H/5671–37

Typical Applications (Continued)

3-Decade Logarithmic A/D Converter



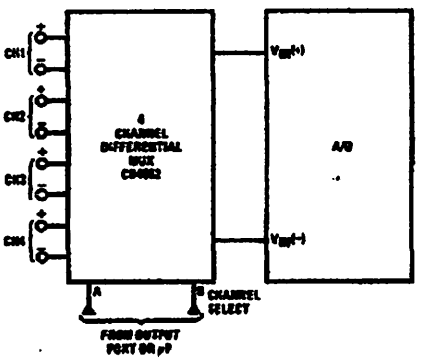
Noise Filtering the Analog Input



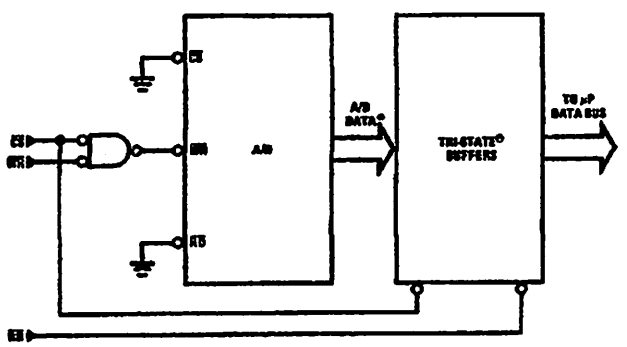
$f_C = 20$ Hz

Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter
Adding a seperate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

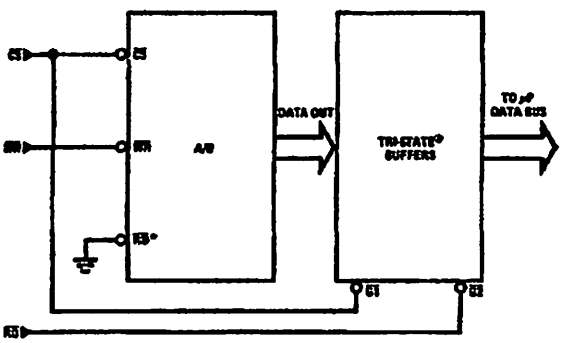


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

Increasing Bus Drive and/or Reducing Time on Bus

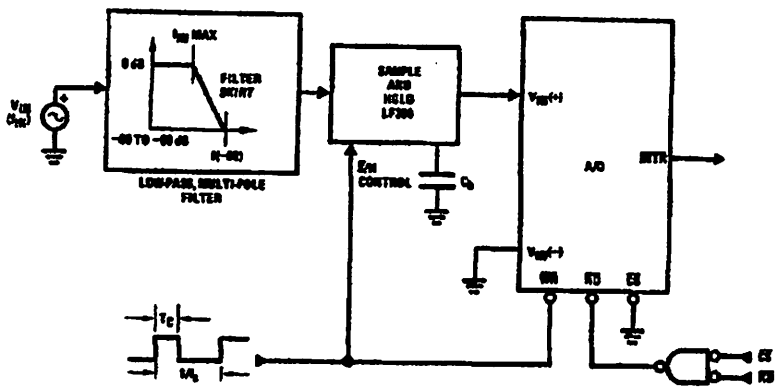


TL/H/5671–10

*Allows output data to set-up at falling edge of $\overline{CS}$

Typical Applications (Continued)

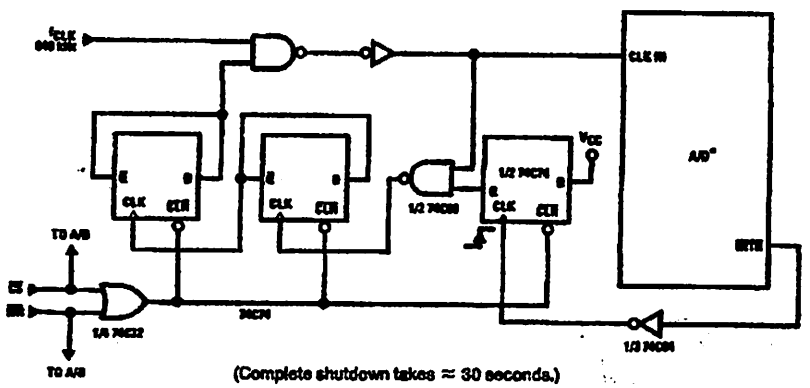
Sampling an AC Input Signal



Note 1: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

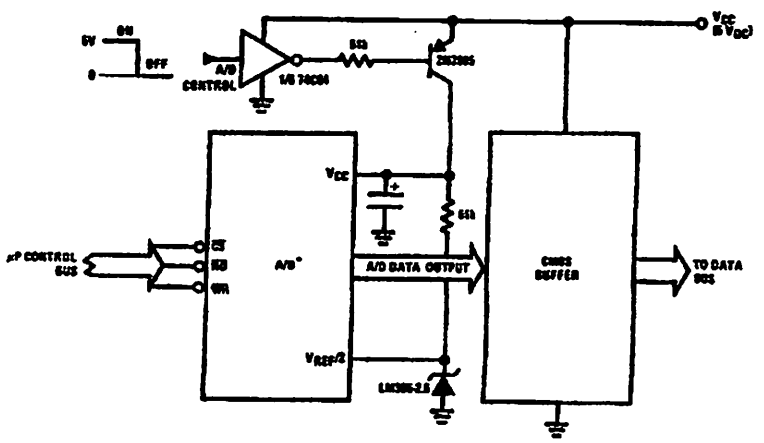
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



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*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

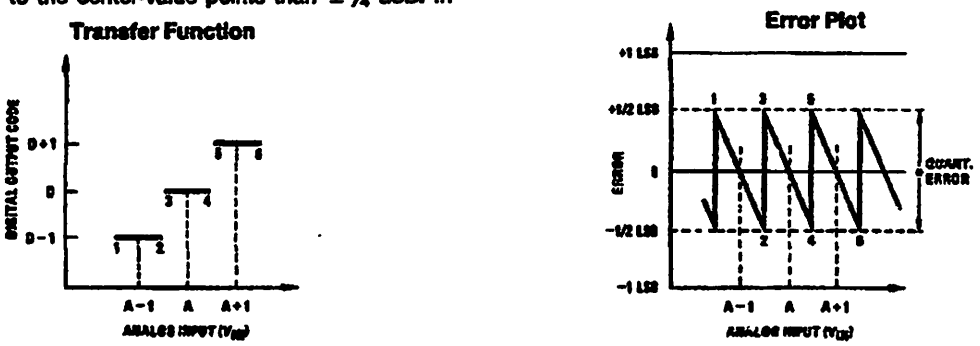
1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output ditigal codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend ±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

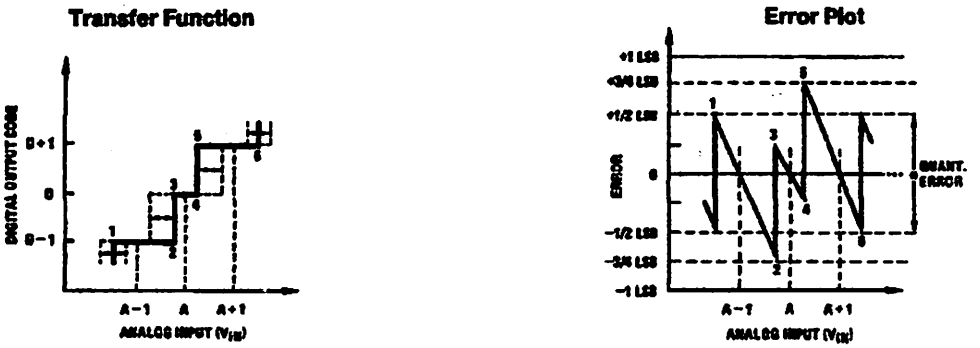
Figure 1b shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

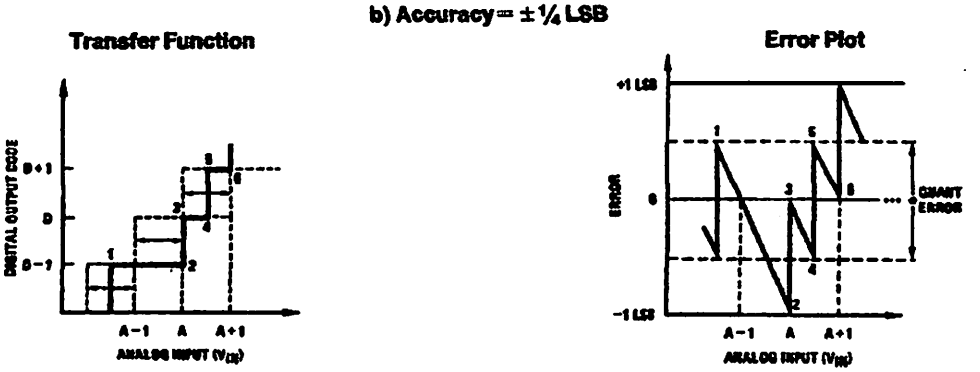
Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.



a) Accuracy = ±0 LSB: A Perfect A/D



b) Accuracy = ±¼ LSB



c) Accuracy = ±½ LSB

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FIGURE 1. Clarifying the Error Specs of an A/D Converter

unctional Description (Continued)

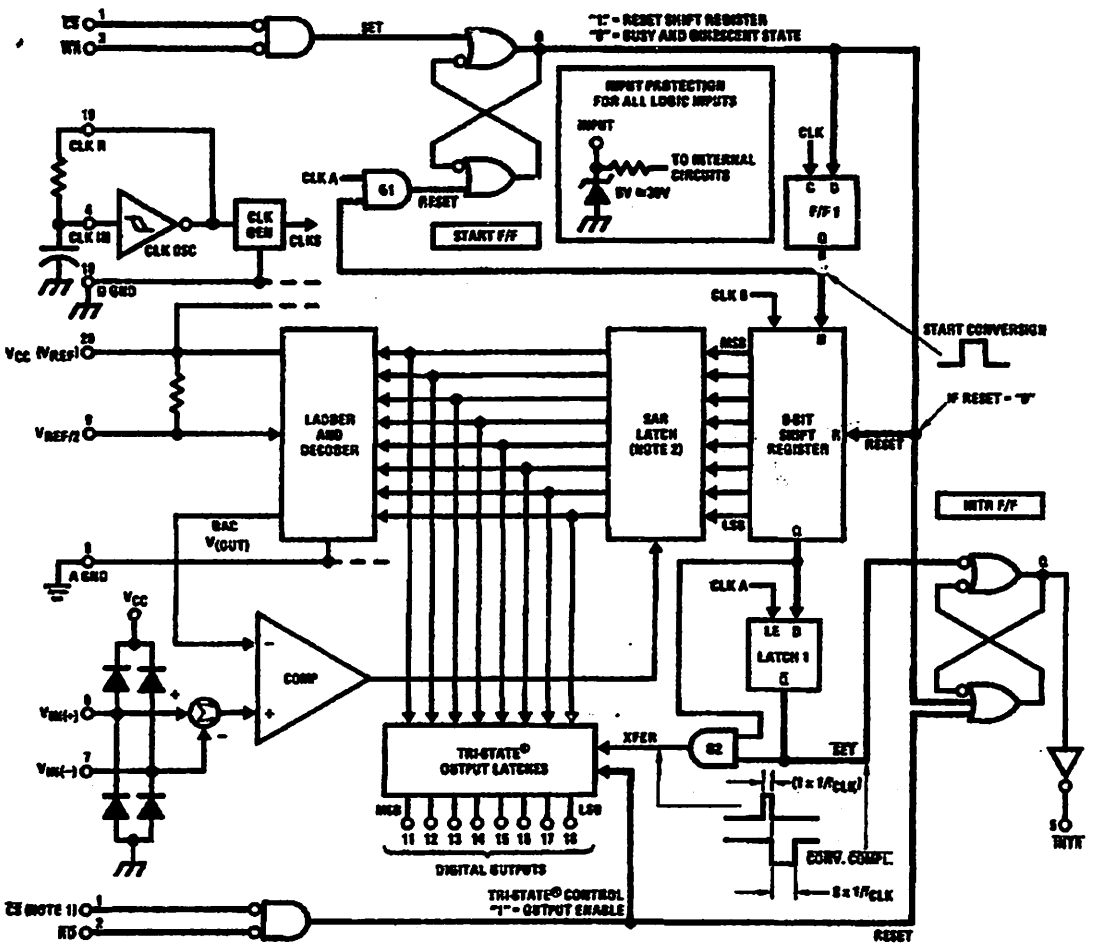
0 FUNCTIONAL DESCRIPTION

ıe ADC0801 series contains a circuit equivalent of the 56R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on ıe R network. The most significant bit is tested first and ter 8 comparisons (64 clock cycles) a digital 8-bit binary ode (1111 1111 = full-scale) is transferred to an output tch and then an interrupt is asserted ($\overline{INTR}$ makes a high-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be perated in the free-running mode by connecting $\overline{INTR}$ to ıe $\overline{WR}$ input with $\overline{CS}$ = 0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the st power-up cycle.

n the high-to-low transition of the $\overline{WR}$ input the internal AR latches and the shift register stages are reset. As long s the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock riods after at least one of these inputs makes a low-to-gh transition.*

A functional diagram of the A/D converter is shown in *Figure 2*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.



Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

Functional Description (Continued)

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard TTL logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-1/2 clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to 1/4 LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)}$$

which gives

$V_P \simeq 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

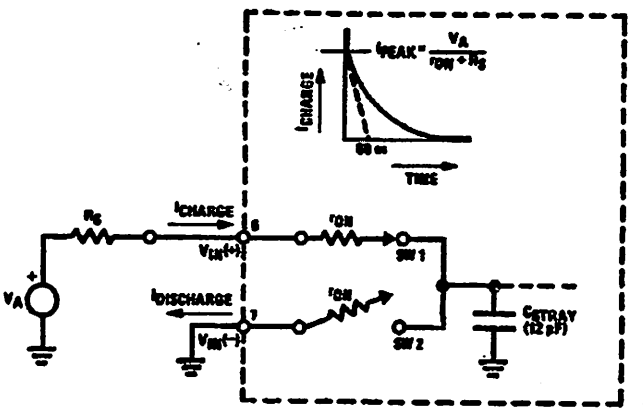
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



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r_{ON} of SW 1 and SW 2 = 5 kΩ

$\tau = r_{ON} C_{STRAY} \simeq 5\ k\Omega \times 12\ pF = 60\ ns$

FIGURE 3. Analog Input Impedance

Functional Description (Continued)

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of $V_{CC}+50$ mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pin 6 and 7) should be kept as short as possible to *minimize* input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.

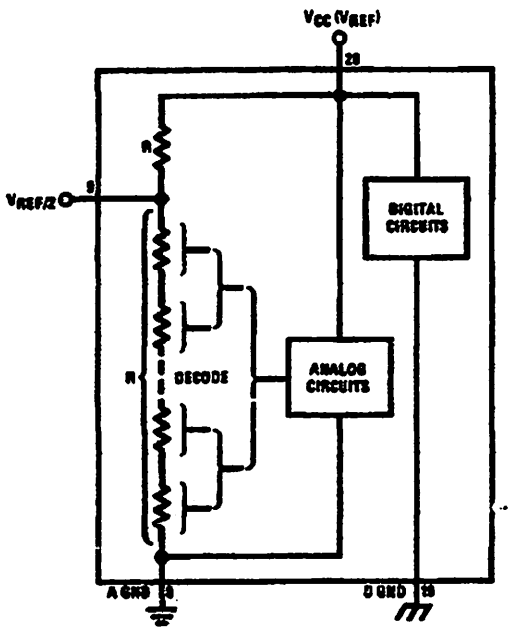

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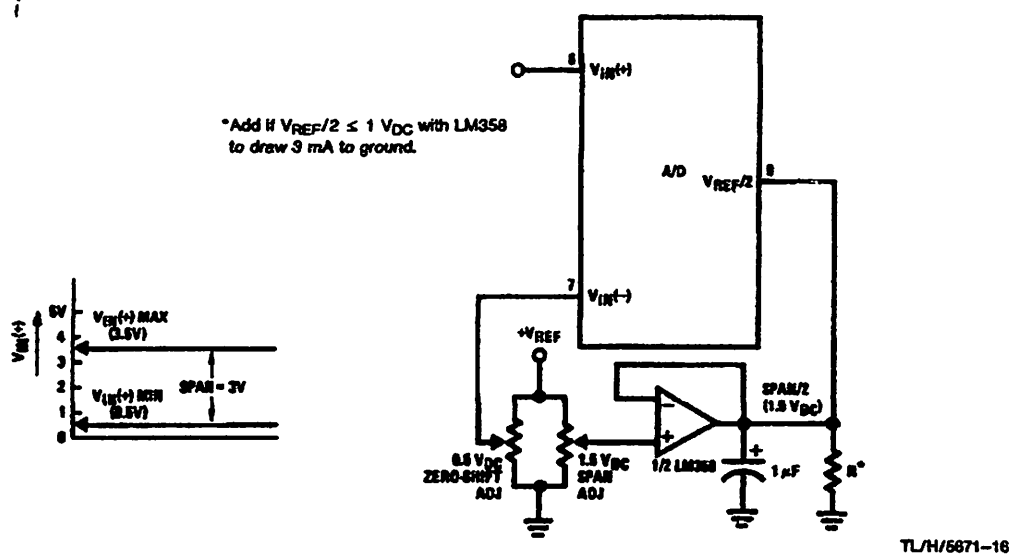
FIGURE 4. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

Functional Description (Continued)



a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5V (Digital Out = = 00_{HEX}) to 3.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

4.2 Reference Accuracy Requirements

ie converter can be operated in a ratiometric mode or an isolute mode. In ratiometric converter applications, the agnitude of the reference voltage is a factor in both the tput of the source transducer and the output of the A/D nverter and therefore cancels out in the final digital output de. The ADC0805 is specified particularly for use in ratio- etric applications with no adjustments required. In abso- e conversion applications, both the initial value and the mperature stability of the reference voltage are important ctors in the accuracy of the A/D converter. For $V_{REF}/2$ ltages of 2.4 V_{DC} nominal value, initial errors of ±10 V_{DC} will cause conversion errors of ±1 LSB due to the in of 2 of the $V_{REF}/2$ input. In reduced span applications, e initial value and the stability of the $V_{REF}/2$ input voltage come even more important. For example, if the span is duced to 2.5V, the analog input LSB voltage value is cor- spondingly reduced from 20 mV (5V span) to 10 mV and LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, s reduces the allowed initial tolerance of the reference ltage and requires correspondingly less absolute change th temperature variations. Note that spans smaller than 5V place even tighter requirements on the initial accuracy d stability of the reference source.

general, the magnitude of the reference voltage will re- ire an initial adjustment. Errors due to an improper value reference voltage appear as full-scale errors in the A/D nsfer function. IC voltage regulators may be used for ref- ences if the ambient temperature changes are not exces- e. The LM336B 2.5V IC reference diode (from National miconductor) has a temperature stability of 1.8 mV typ mV max) over $0°C \leq T_A \leq +70°C$. Other temperature nge parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

Functional Description (Continued)

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+) \text{ fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = The high end of the analog input range

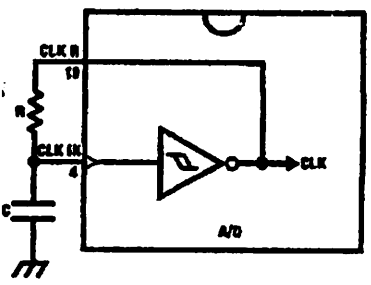
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6.*



$$f_{CLK} \cong \frac{1}{1.1\,RC}$$

$$R \cong 10\ k\Omega$$

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FIGURE 6. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

ınctional Description (Continued)

ingle point analog ground that is separate from the logic ound points should be used. The power supply bypass pacitor and the self-clocking capacitor (if used) should h be returned to digital ground. Any $V_{REF}/2$ bypass caitors, analog input filter capacitors, or input signal shield- should be returned to the analog ground point. A test for per grounding is to measure the zero error of the A/D verter. Zero errors in excess of ¼ LSB can usually be ed to improper board layout and wiring (see section .1 for measuring the zero error).

TESTING THE A/D CONVERTER

ere are many degrees of complexity associated with test- an A/D converter. One of the simplest tests is to apply a wn analog input voltage to the converter and use LEDs display the resulting digital output code as shown in *Fig- 7.*

ease of testing, the $V_{REF}/2$ (pin 9) should be supplied h 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} uld be used. This provides an LSB value of 20 mV.

l full-scale adjustment is to be made, an analog input tage of 5.090 V_{DC} (5.120–1½ LSB) should be applied to $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of $V_{REF}/2$ input voltage should then be adjusted until the ital output code is just changing from 1111 1110 to 1111 11. This value of $V_{REF}/2$ should then be used for all the ts.

e digital output LED display can be decoded by dividing 8 bits into 2 hex characters, the 4 most significant (MS) l the 4 least significant (LS). Table I shows the fractional ary equivalent of these two 4-bit groups. By adding the tages obtained from the "VMS" and "VLS" columns in ble I, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

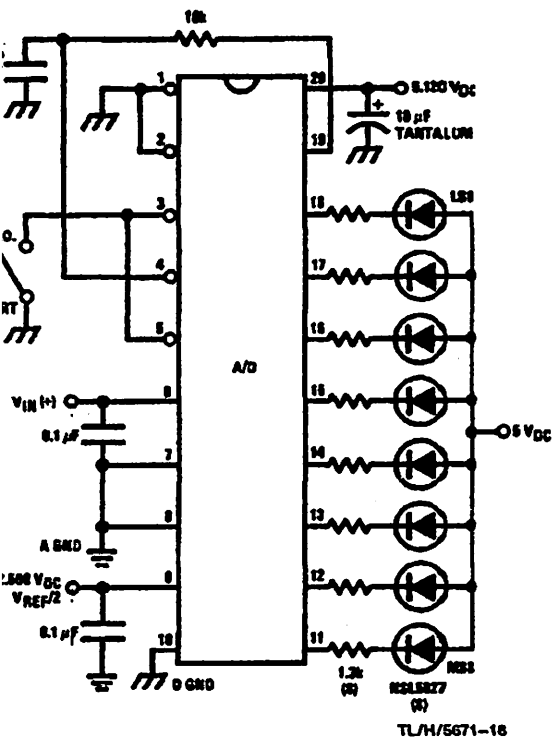

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FIGURE 7. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A–C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. *Using the I/O space provides 256 additional addresses and* may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10*.

Functional Description (Continued)

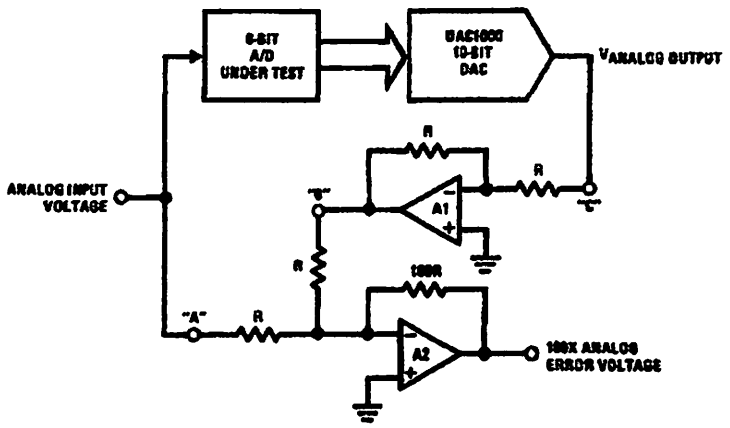

FIGURE 8. A/D Tester with Analog Error Output

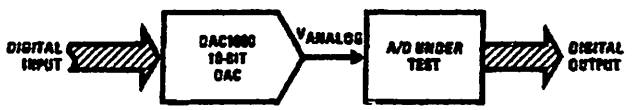

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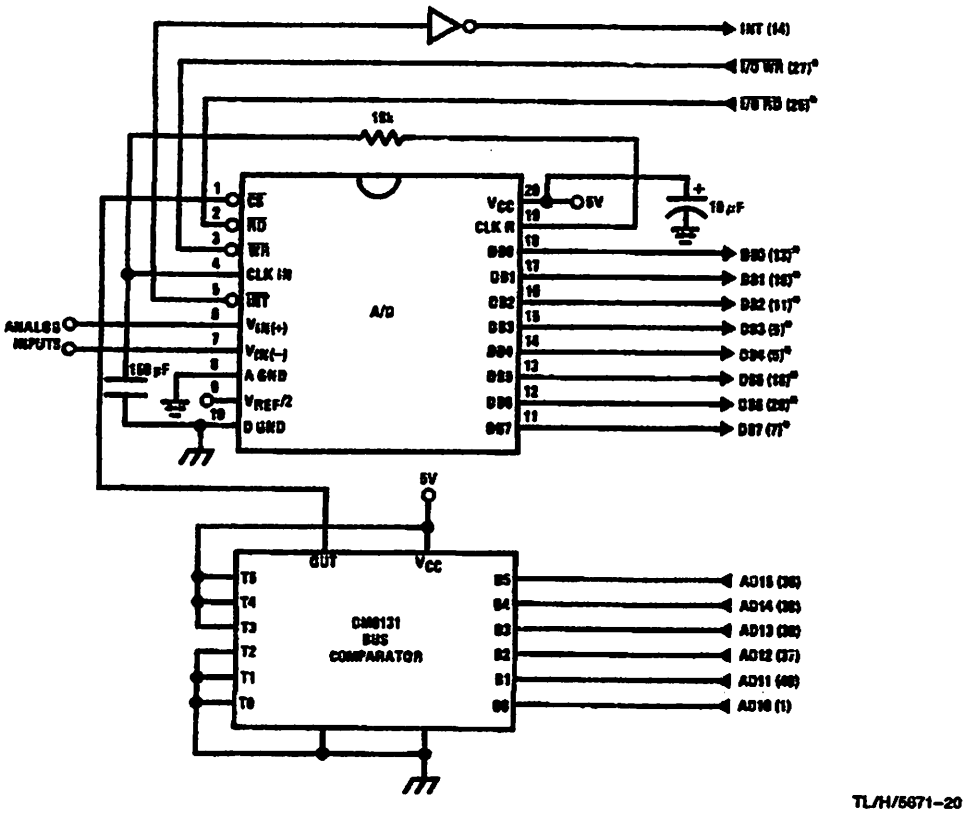
FIGURE 9. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

BINARY				FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$	
				MS GROUP	LS GROUP	VMS GROUP*	VLS GROUP*
1	1	1	1	15/16	15/256	4.800	0.300
1	1	1	0	7/8	7/128	4.480	0.280
1	1	0	1	13/16	13/256	4.160	0.260
1	1	0	0	3/4	3/64	3.840	0.240
1	0	1	1	11/16	11/256	3.520	0.220
1	0	1	0	5/8	5/128	3.200	0.200
1	0	0	1	9/16	9/256	2/880	0.180
1	0	0	0	1/2	1/32	2/560	0.160
0	1	1	1	7/16	7/256	2.240	0.140
0	1	1	0	3/8	3/128	1.920	0.120
0	1	0	1	5/16	2/256	1.600	0.100
0	1	0	0	1/4	1/64	1/280	0.080
0	0	1	1	3/16	3/256	0.960	0.060
0	0	1	0	1/8	1/128	0.640	0.040
0	0	0	1	1/16	1/256	0.320	0.020
0	0	0	0			0	0

*lay Output = VMS Group + VLS Group

Functional Description (Continued)



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Note 1: *Pin numbers for the DP8228 system controller, others are INS8080A.

Note 2: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 10. ADC0801–INS8080A CPU Interface

SAMPLE PROGRAM FOR *FIGURE 10* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:      JMP     LD DATA
  •       •           •
  •       •           •
0100    21 00 02    START:      LXI H 0200H         ;HL pair will point to
                                                    ;data storage locations
0103    31 00 04    RETURN:     LXI SP 0400H        ;Initialize stack pointer (Note 1)
0106    7D                      MOV A, L            ;Test # of bytes entered
0107    FE 0F                   CPI 0F H            ;If # = 16. JMP to
0109    CA 13 01                JZ CONT             ;user program
010C    D3 E0                   OUT E0 H            ;Start A/D
010E    FB                      EI                  ;Enable interrupt
010F    00          LOOP:       NOP                 ;Loop until end of
0110    C3 0F 01                JMP LOOP            ;conversion
0113      •         CONT:         •
  •       •           •           •
  •       •         (User program to  •
  •       •         process data)     •
  •       •           •           •
  •       •           •           •
0300    DB E0       LD DATA:    IN E0 H             ;Load data into accumulator
0302    77                      MOV M, A            ;Store data
0303    23                      INX H               ;Increment storage pointer
0304    C3 03 01                JMP RETURN
```

Note 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 2: All address used were arbitrarily chosen.

Functional Description (Continued)

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 10* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 11*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

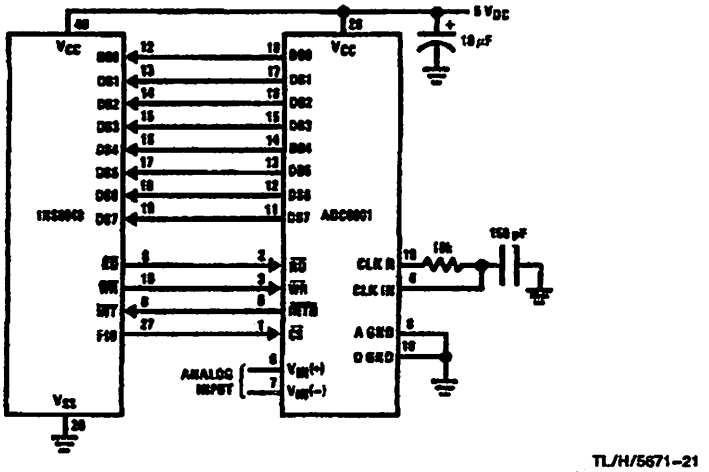

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FIGURE 11. INS8048 Interface

SAMPLE PROGRAM FOR *FIGURE 11* INS8048 INTERFACE

```
04 10                    JMP     10H          ;Program starts at addr 10
                         ORG     3H
04 50                    JMP     50H          ;Interrupt jump vector
                         ORG     10H          ;Main program
99 FE                    ANL     P1, #0FEH    ;Chip select
81                       MOVX    A, @R1       ;Read in the 1st data
                                              ;to reset the intr
89 01          START:    ORL     P1, #1       ;Set port pin high
B8 20                    MOV     R0, #20H     ;Data address
B9 FF                    MOV     R1, #0FFH    ;Dummy address
BA 10                    MOV     R2, #10H     ;Counter for 16 bytes
23 FF          AGAIN:    MOV     A, #0FFH     ;Set ACC for intr loop
99 FE                    ANL     P1, #0FEH    ;Send CS (bit 0 of P1)
91                       MOVX    @R1, A       ;Send WR out
05                       EN      I            ;Enable interrupt
96 21          LOOP:     JNZ     LOOP         ;Wait for interrupt
EA 1B                    DJNZ    R2, AGAIN    ;If 16 bytes are read
00                       NOP                  ;go to user's program
00                       NOP
                         ORG     50H
81             INDATA:   MOVX    A, @R1       ;Input data, CS still low
A0                       MOV     @R0, A       ;Store in memory
18                       INC     R0           ;Increment storage counter
89 01                    ORL     P1, #1       ;Reset CS signal
27                       CLR     A            ;Clear ACC to get out of
93                       RETR                 ;the interrupt loop
```

unctional Description (Continued)

2 Interfacing the Z-80

ıe Z-80 control bus is slightly different from that of the 180. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generated strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is at the CPU will automatically insert one wait state (the $\overline{RD}$ nd $\overline{WR}$ strobes are extended one clock period) to allow ore time for the I/O devices to respond. Logic to map the /D in I/O space is shown in *Figure 13.*

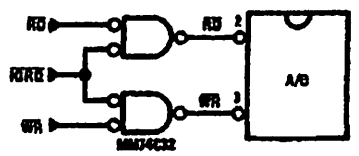


FIGURE 13. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

dditional I/O advantages exist as software DMA routines e available and use can be made of the output data transr which exists on the upper 8 address lines (A8 to A15) ıring I/O input instructions. For example, MUX channel lection for the A/D can be accomplished with this operatg mode.

3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

ıe control bus for the 6800 microprocessor derivatives oes not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it emoys a single R/$\overline{W}$ line and additional timing, if needed, can derived fom the $\phi 2$ clock. All I/O devices are memory apped in the 6800 system, and a special signal, VMA, dicates that the current address is valid. *Figure 14* shows interface schematic where the A/D is memory mapped in e 6800 system. For simplicity, the $\overline{CS}$ decoding is shown ing ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{475}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 15* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

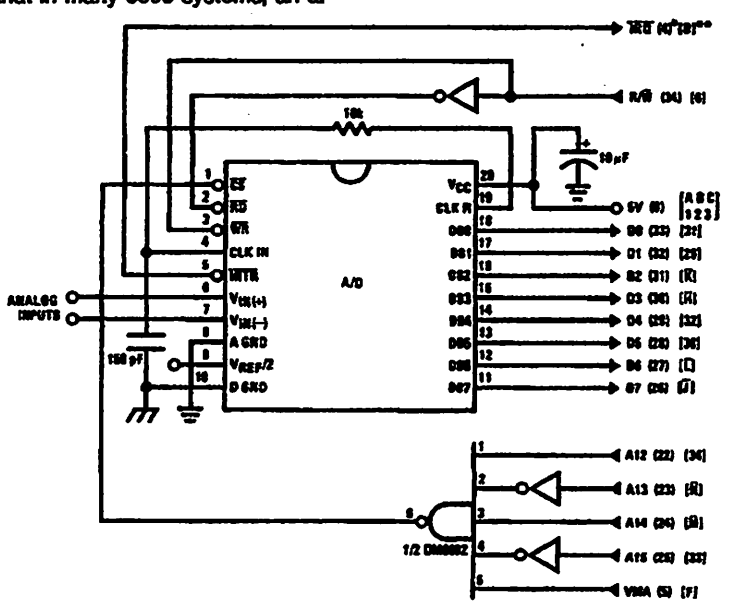
A sample interface program equivalent to the previous one is shown below *Figure 15*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 16*.



ıte 1: Numbers in parentheses refer to MC6800 CPU pin out.
ıte 2: Number or letters in brackets refer to standard M6800 system common bus code.

FIGURE 14. ADC0801-MC6800 CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 14* ADC0801-MC6800 CPU INTERFACE

```
0010    DF 36       DATAIN   STX    TEMP2      ;Save contents of X
0012    CE 00 2C             LDX    #$002C     ;Upon IRQ low CPU
0015    FF FF F8             STX    $FFF8      ;jumps to 002C
0018    B7 50 00             STAA   $5000      ;Start ADC0801
001B    0E                   CLI
001C    3E          CONVRT   WAI                ;Wait for interrupt
001D    DE 34                LDX    TEMP1
001F    8C 02 0F             CPX    #$020F     ;Is final data stored?
0022    27 14                BEQ    ENDP
0024    B7 50 00             STAA   $5000      ;Restarts ADC0801
0027    08                   INX
0028    DF 34                STX    TEMP1
002A    20 F0                BRA    CONVRT
002C    DE 34       INTRPT   LDX    TEMP1
002E    B6 50 00             LDAA   $5000      ;Read data
0031    A7 00                STAA   X          ;Store it at X
0033    3B                   RTI
0034    02 00       TEMP1    FDB    $0200      ;Starting address for
                                                ;data storage
0036    00 00       TEMP2    FDB    $0000
0038    CE 02 00    ENDP     LDX    #$0200     ;Reinitialize TEMP1
003B    DF 34                STX    TEMP1
003D    DE 36                LDX    TEMP2
003F    39                   RTS                ;Return from subroutine
                                                ;To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

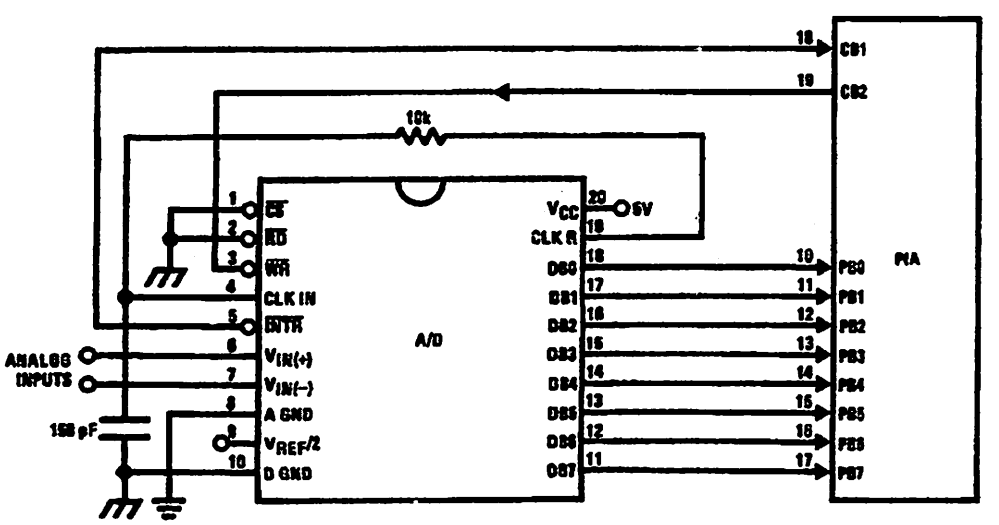


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FIGURE 15. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 15* ADC0801–MC6820 PIA INTERFACE

```
0010  CE 00 38   DATAIN   LDX   #$0038    ; Upon IRQ low CPU
0013  FF FF F8           STX   $FFF8      ; jumps to 0038
0016  B6 80 06           LDAA  PIAORB     ; Clear possible IRQ flags
0019  4F                 CLRA
001A  B7 80 07           STAA  PIACRB
001D  B7 80 06           STAA  PIAORB     ; Set Port B as input
0020  0E                 CLI
0021  C6 34              LDAB  #$34
0023  86 3D              LDAA  #$3D
0025  F7 80 07   CONVRT  STAB  PIACRB     ; Starts ADC0801
0028  B7 80 07           STAA  PIACRB
002B  3E                 WAI               ; Wait for interrupt
002C  DE 40              LDX   TEMP1
002E  8C 02 0F           CPX   #$020F      ; Is final data stored?
0031  27 0F              BEQ   ENDP
0033  08                 INX
0034  DF 40              STX   TEMP1
0036  20 ED              BRA   CONVRT
0038  DE 40   INTRPT     LDX   TEMP1
003A  B6 80 06           LDAA  PIAORB     ; Read data in
003D  A7 00              STAA  X          ; Store it at X
003F  3B                 RTI
0040  02 00    TEMP1     FDB   $0200      ; Starting address for
                                          ; data storage
0042  CE 02 00 ENDP      LDX   #$0200     ; Reinitialize TEMP1
0045  DF 40              STX   TEMP1
0047  39                 RTS               ; Return from subroutine
               PIAORB    EQU   $8006      ; to user's program
               PIACRB    EQU   $8007
```

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

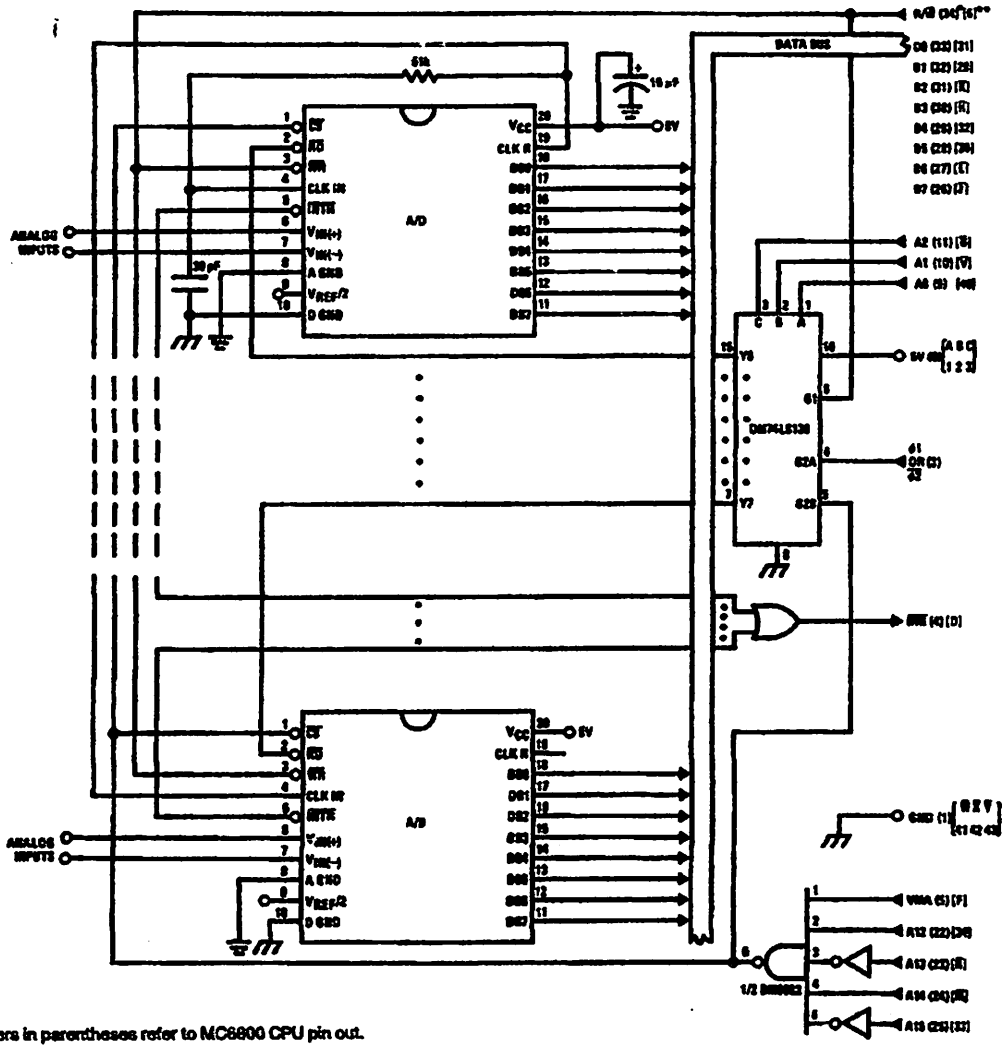
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers of letters in brackets refer to standard M6800 system common bus code.

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FIGURE 16. Interfacing Multiple A/Ds in an MC6800 System

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 17* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

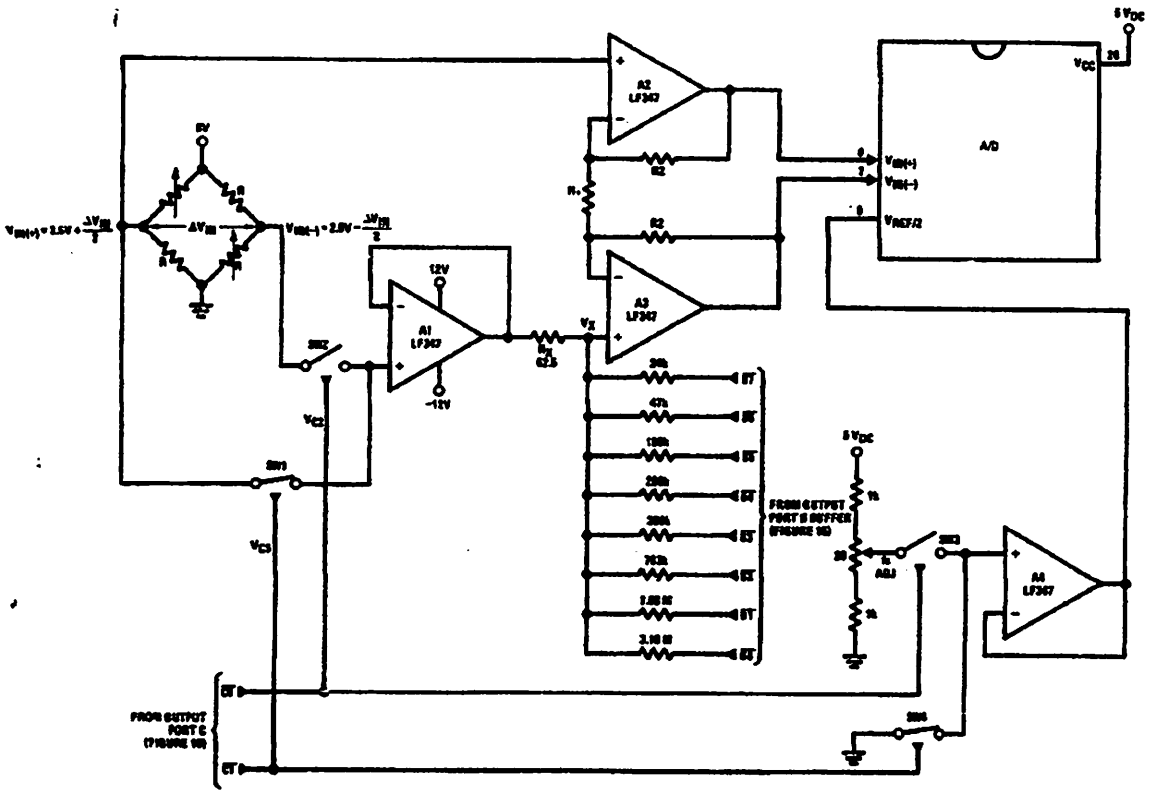
$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 18*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_X increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 μV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.

Functional Description (Continued)



Note 1: R2 = 49.5 R1

Note 2: Switches are LMC13334 CMOS analog switches.

Note 3: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 17. Gain of 100 Differential Transducer Preamp

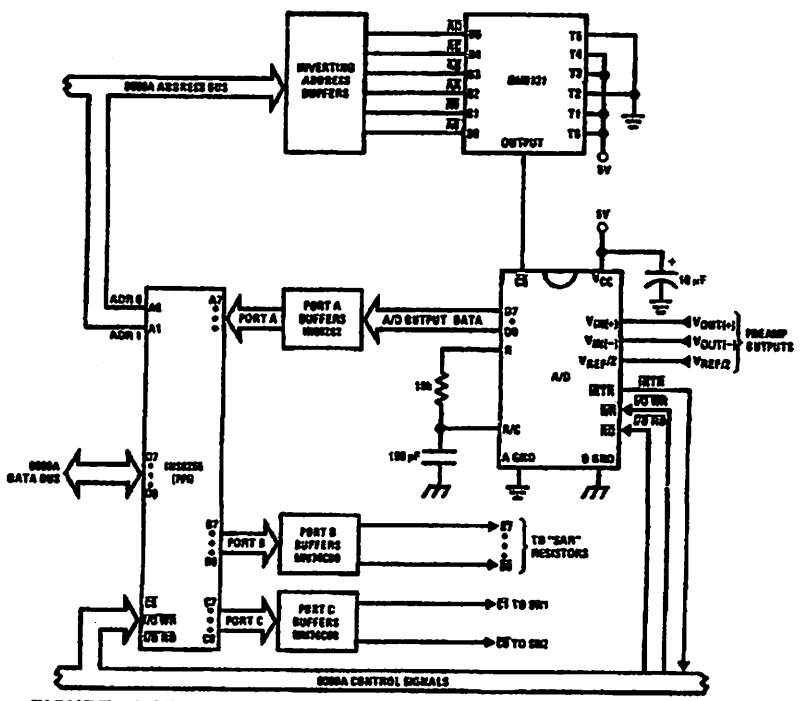


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FIGURE 18. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 19*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 20*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 21* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

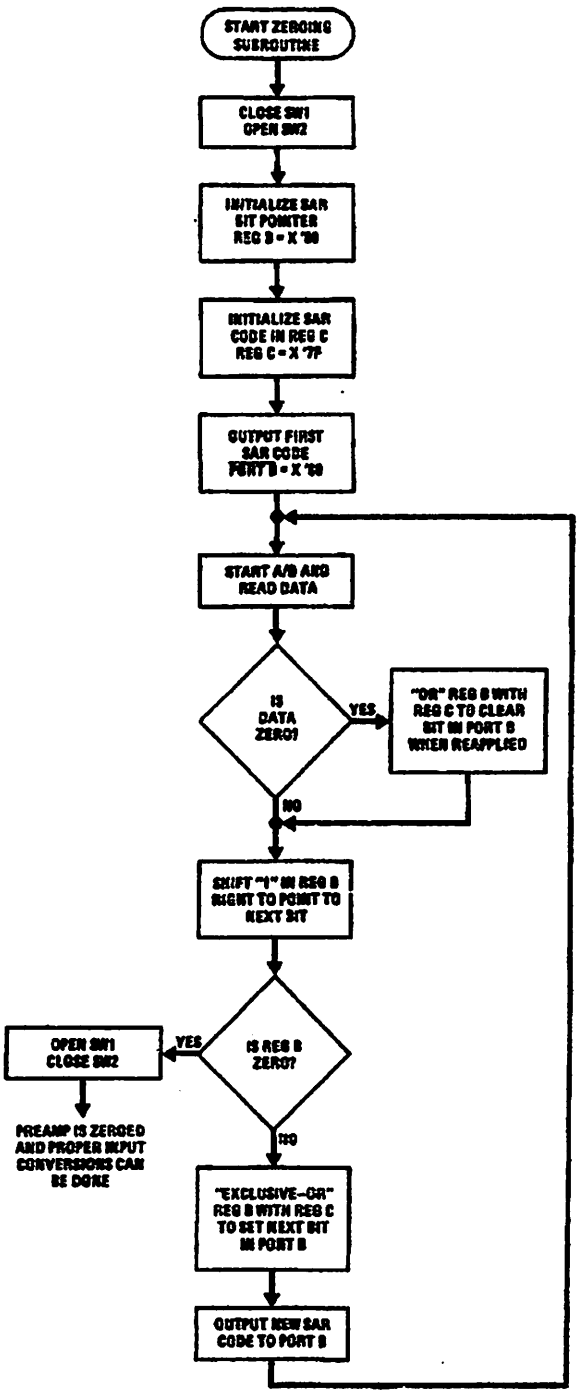

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FIGURE 19. Flow Chart for Auto-Zero Routine

```
3D00  3E90    MVI 90
3D02  D3E7    Out Control Port                    ;Program PPI
3D04  2601    MVI H 01          Auto-Zero Subroutine
3D06  7C      MOV A,H
3D07  D3E6    OUT C                              ;Close SW1 open SW2
3D09  0680    MVI B 80                           ;Initialize SAR bit pointer
3D0B  3E7F    MVI A 7F                           ;Initialize SAR code
3D0D  4F      MOV C,A           Return
3D0E  D3E5    OUT B                              ;Port B = SAR code
3D10  31AA3D  LXI SP 3DAA       Start              ;Dimension stack pointer
3D13  D3E4    OUT A                              ;Start A/D
3D15  FB      IE
3D16  00      NOP               Loop               ;Loop until INT asserted
3D17  C3163D  JMP Loop
3D1A  7A      MOV A,D           Auto-Zero
3D1B  C600    ADI 00
3D1D  CA2D3D  JZ Set C                           ;Test A/D output data for zero
3D20  78      MOV A,B           Shift B
3D21  F600    ORI 00                             ;Clear carry
3D23  1F      RAR                                ;Shift "1" in B right one place
3D24  FE00    CPI 00                             ;Is B zero? If yes last
3D26  CA373D  JZ Done                            ;approximation has been made
3D29  47      MOV B,A
3D2A  C3333D  JMP New C
3D2D  79      MOV A,C           Set C
3D2E  B0      ORA B                              ;Set bit in C that is in same
3D2F  4F      MOV C,A                            ;position as "1" in B
3D30  C3203D  JMP Shift B
3D33  A9      XRA C             New C            ;Clear bit in C that is in
3D34  C30D3D  JMP Return                         ;same position as "1" in B
3D37  47      MOV B,A           Done               ;then output new SAR code.
3D38  7C      MOV A,H                            ;Open SW1, close SW2 then
3D39  EE03    XRI 03                             ;proceed with program. Preamp
3D3B  D3E6    OUT C                              ;is now zeroed.
3D3D          •                 Normal
              •
              •
              Program for processing
              proper data values
3C3D  DBE4    IN A              Read A/D Subroutine ;Read A/D data
3C3F  EEFF    XRI FF                             ;Invert data
3C41  57      MOV D,A
3C42  78      MOV A,B                            ;Is B Reg = 0? If not stay
3C43  E6FF    ANI FF                             ;in auto zero subroutine
3C45  C21A3D  JNZ Auto-Zero
3C48  C33D3D  JMP Normal
```

Note: All numerical values are hexadecimal representations.

FIGURE 20. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80® Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

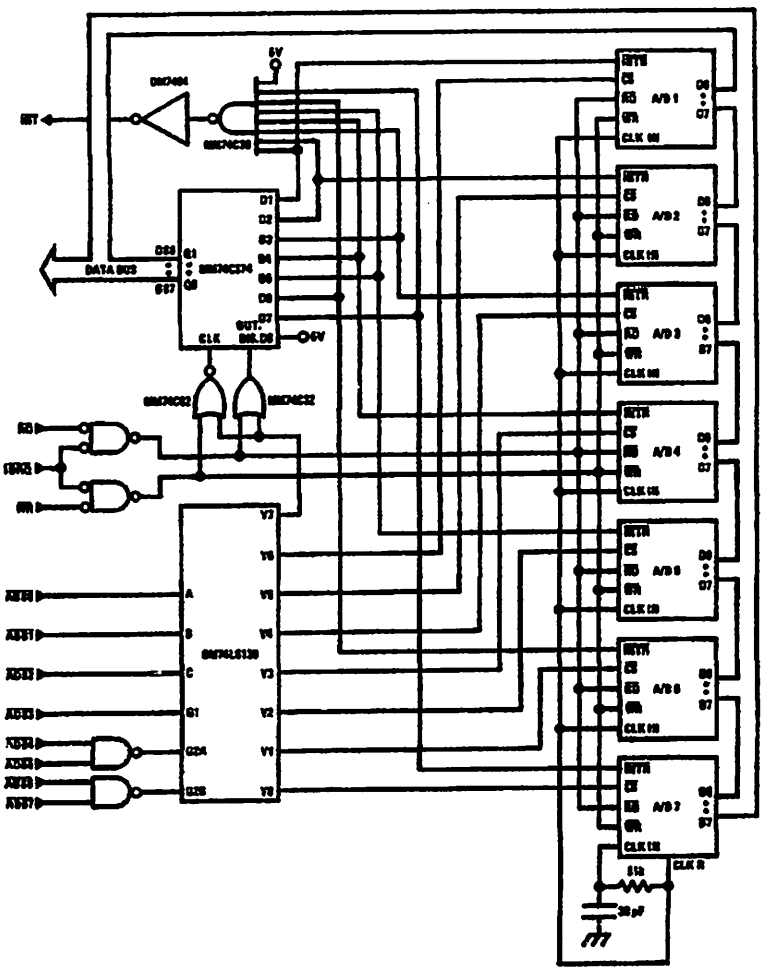

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FIGURE 21. Multiple A/Ds with Z-80 Type Microprocessor

INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE		SOURCE STATEMENT	COMMENT
0038	E5		PUSH HL	;Save contents of all registers affected by
0039	C5		PUSH BC	;this subroutine.
003A	F5		PUSH AF	;Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL),X3E00	;Initialize memory pointer where data will be stored.
003E	0E 01		LD C, X01	;C register will be port ADDR of A/D converters.
0040	D300		OUT X00, A	;Load peripheral status word into 8-bit latch.
0042	DB00		IN A, X00	;Load status word into accumulator.
0044	47		LD B,A	;Save the status word.
0045	79	TEST	LD A,C	;Test to see if the status of all A/D's have
0046	FE 08		CP, X08	;been checked. If so, exit subroutine
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	;Test a single bit in status word by looking for
004C	1F		RRA	;a "1" to be rotated into the CARRY (an $\overline{INT}$
004D	47		LD B,A	;is loaded as a "1"). If CARRY is set then load
004E	DA 5500		JPC, LOAD	;contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	;If CARRY is not set, increment C register to point
0052	C3 4500		JP,TEST	;to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	;Read data from interrupting A/D and invert
0057	EE FF		XOR FF	;the data.
0059	77		LD (HL),A	;Store the data
005A	2C		INC L	
005B	71		LD (HL),C	;Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP,NEXT	;Test next bit in status word.
0060	F1	DONE	POP AF	;Re-establish all registers as they were
0061	C1		POP BC	;before the interrupt.
0062	E1		POP HL	
0063	C9		RET	;Return to original program

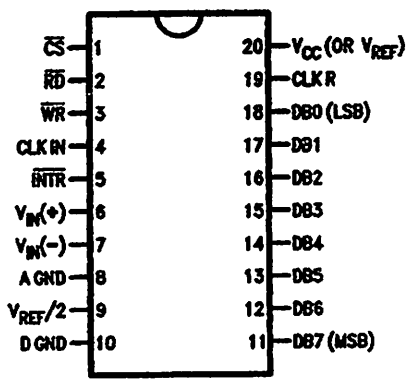
Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted				ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM	ADC0802LCV		ADC0802LCN
	±½ Bit Adjusted	ADC0803LCWM	ADC0803LCV		ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCV	ADC0804LCN	ADC0805LCN
PACKAGE OUTLINE		M20B—Small Outline	V20A—Chip Carrier	N20A—Molded DIP	

TEMP RANGE		−40°C TO +85°C	−55°C TO +125°C
ERROR	±¼ Bit Adjusted	ADC0801LCJ	ADC0801LJ
	±½ Bit Unadjusted	ADC0802LCJ	ADC0802LJ,
	±½ Bit Adjusted	ADC0803LCJ	ADC0802LJ/883
	±1Bit Unadjusted	ADC0804LCJ	
PACKAGE OUTLINE		J20A—Cavity DIP	J20A—Cavity DIP

Connection Diagrams

ADC080X
Dual-In-Line and Small Outline (SO) Packages



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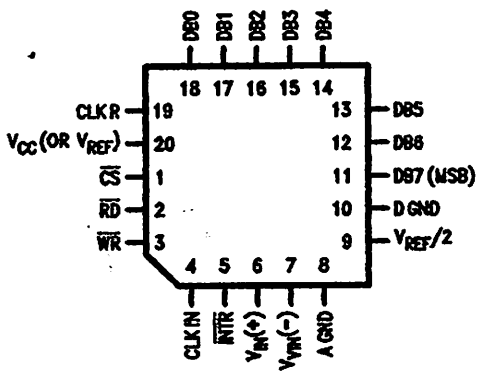
ADC080X
Molded Chip Carrier (PCC) Package



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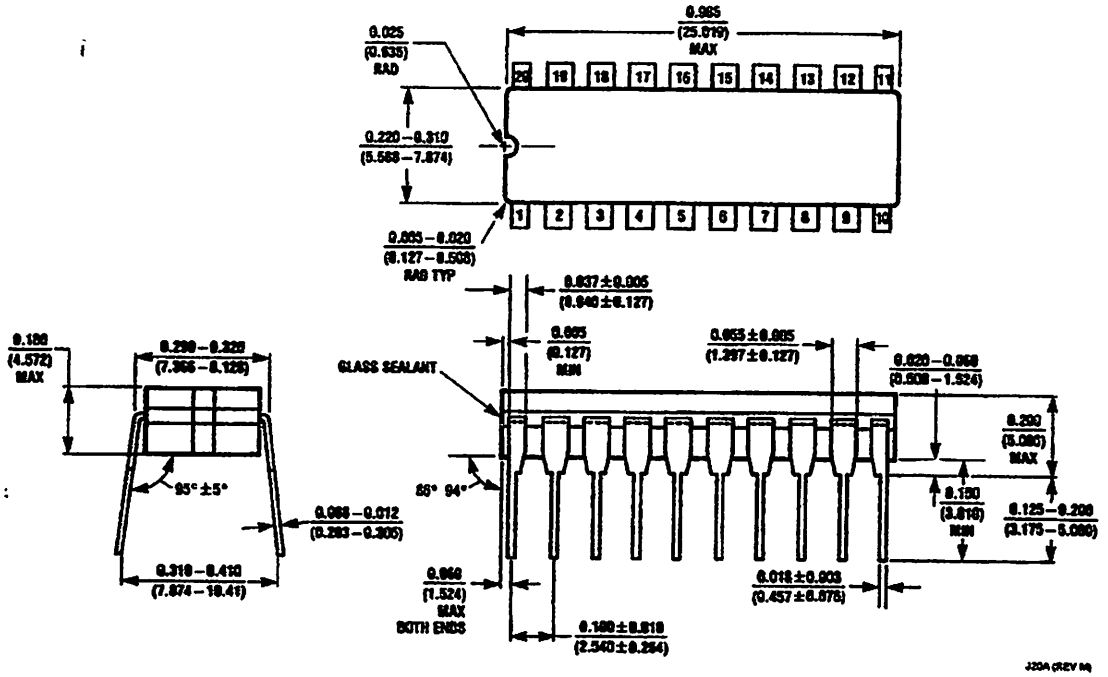
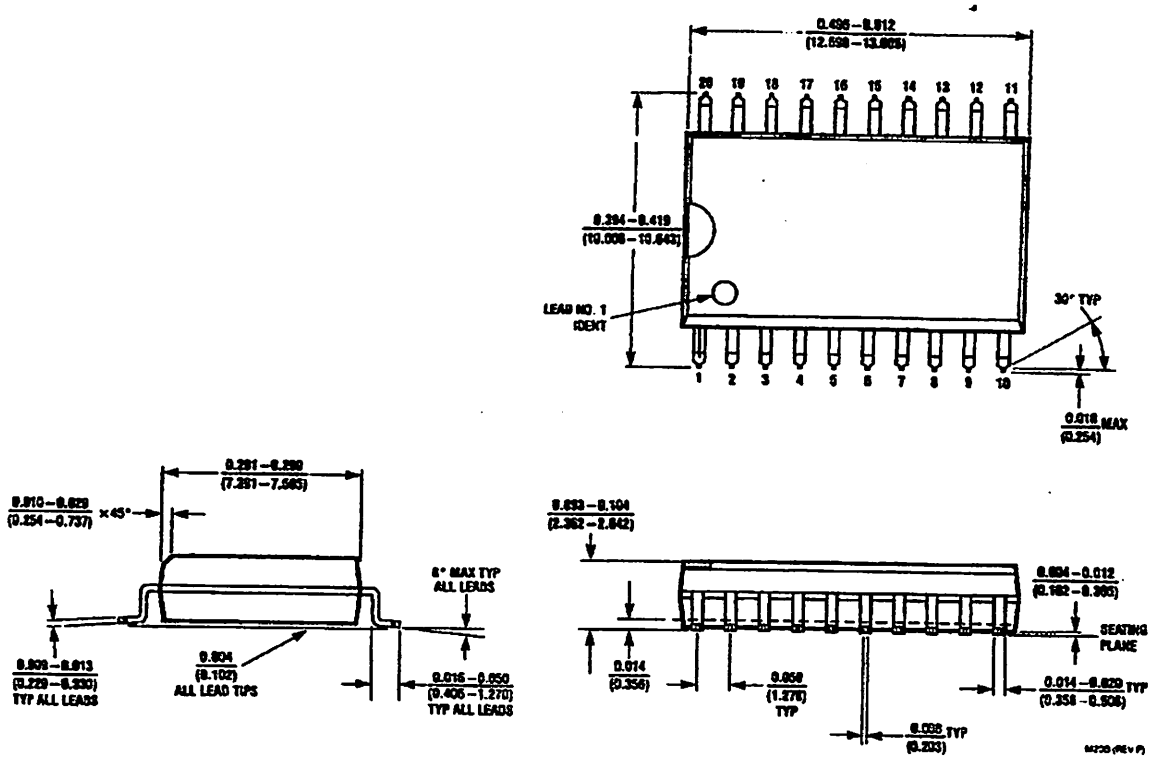
See Ordering Information

Physical Dimensions inches (millimeters)

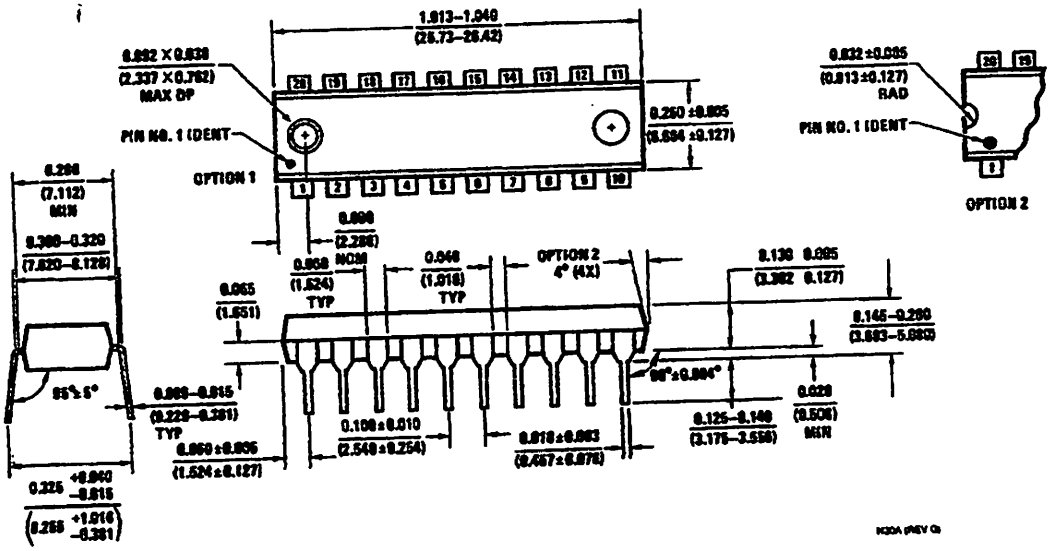


Dual-In-Line Package (J)
Order Number ADC0801LJ, ADC0802LJ, ADC0801LCJ, ADC0802LCJ, ADC0803LCJ or ADC0804LCJ
ADC0802LJ/883 or 5962-9096601MRA
NS Package Number J20A



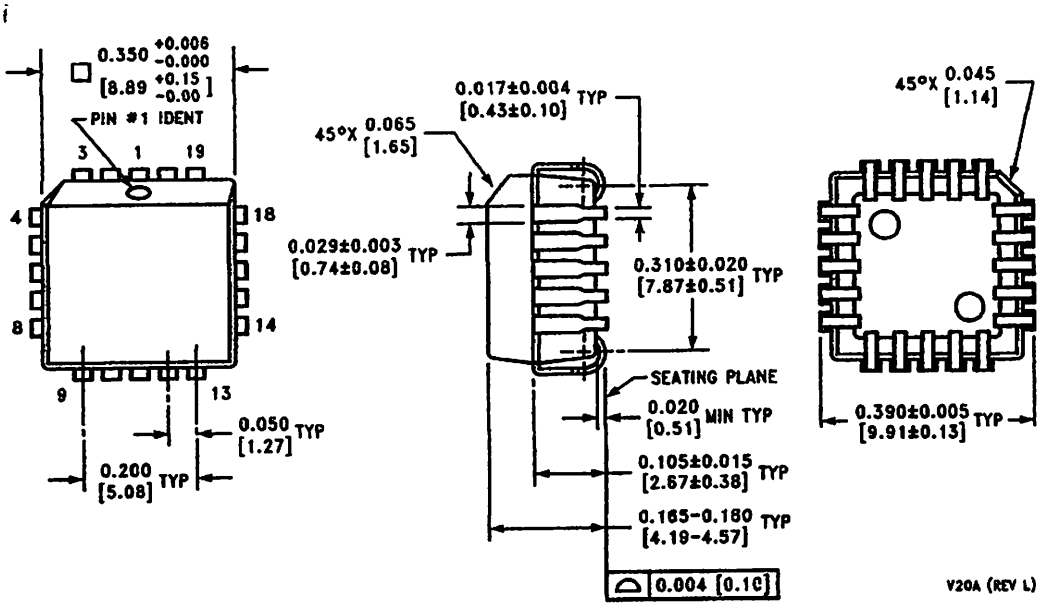
SO Package (M)
Order Number ADC0802LCWM, ADC0803LCWM or ADC0804LCWM
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number ADC0801LCN, ADC0802LCN,
ADC0803LCN, ADC0804LCN or ADC0805LCN
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



Molded Chip Carrier Package (V)
Order Number ADC0802LCV, ADC0803LCV or ADC0804LCV
NS Package Number V20A

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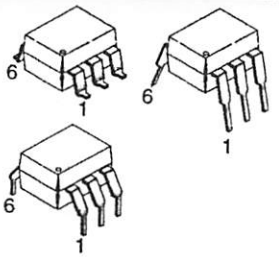
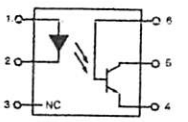
4N25 4N37	4N26 H11A1	4N27 H11A2	4N28 H11A3	4N35 H11A4	4N36 H11A5

WHITE PACKAGE (-M SUFFIX)

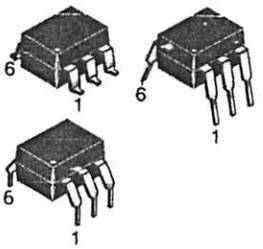


SCHEMATIC



PIN 1. ANODE
2. CATHODE
3. NO CONNECTION
4. EMITTER
5. COLLECTOR
6. BASE

BLACK PACKAGE (NO -M SUFFIX)



SCRIPTION

general purpose optocouplers consist of a gallium arsenide infrared emitting diode driving a silicon phototransistor in a 6-pin n-line package.

ATURES

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recognized (File # E90700)
DE recognized (File # 94766)
dd option V for white package (e.g., 4N25V-M)
dd option 300 for black package (e.g., 4N25.300)

PLICATIONS

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GENERAL PURPOSE 6-PIN PHOTOTRANSISTOR OPTOCOUPLERS

N25	4N26	4N27	4N28	4N35	4N36
N37	H11A1	H11A2	H11A3	H11A4	H11A5

SOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

ımeter	Symbol	Value	Units
AL DEVICE			
age Temperature	T_{STG}	-55 to +150	°C
rating Temperature	T_{OPR}	-55 to +100	°C
ı Solder Temperature	T_{SOL}	260 for 10 sec	°C
l Device Power Dissipation @ T_A = 25°C	P_D	250	mW
ıte above 25°C		3.3 (non-M), 2.94 (-M)	
TTER			
Average Forward Input Current	I_F	100 (non-M), 60 (-M)	mA
ərse Input Voltage	V_R	6	V
ward Current - Peak (300µs, 2% Duty Cycle)	I_F(pk)	3	A
Power Dissipation @ T_A = 25°C	P_D	150 (non-M), 120 (-M)	mW
ıte above 25°C		2.0 (non-M), 1.41 (-M)	mW/°C
ECTOR			
ector-Emitter Voltage	V_{CEO}	30	V
ector-Base Voltage	V_{CBO}	70	V
ter-Collector Voltage	V_{ECO}	7	V
ctor Power Dissipation @ T_A = 25°C	P_D	150	mW
ıte above 25°C		2.0 (non-M), 1.76 (-M)	mW/°C

ECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

DIVIDUAL COMPONENT CHARACTERISTICS

ameter	Test Conditions	Symbol	Min	Typ*	Max	Unit
ITTER :						
ut Forward Voltage	(I_F = 10 mA)	V_F		1.18	1.50	V
erse Leakage Current	(V_R = 6.0 V)	I_R		0.001	10	µA
TECTOR						
lector-Emitter Breakdown Voltage	(I_C = 1.0 mA, I_F = 0)	BV_{CEO}	30	100		V
lector-Base Breakdown Voltage	(I_C = 100 µA, I_F = 0)	BV_{CBO}	70	120		V
itter-Collector Breakdown Voltage	(I_E = 100 µA, I_F = 0)	BV_{ECO}	7	10		V
lector-Emitter Dark Current	(V_{CE} = 10 V, I_F = 0)	I_{CEO}		1	50	nA
lector-Base Dark Current	(V_{CB} = 10 V)	I_{CBO}			20	nA
pacitance	(V_{CE} = 0 V, f = 1 MHz)	C_{CE}		8		pF

OLATION CHARACTERISTICS

aracteristic	Test Conditions	Symbol	Min	Typ*	Max	Units
ut-Output Isolation Voltage	(Non '-M', Black Package) (f = 60 Hz, t = 1 min)	V_{ISO}	5300			Vac(rms)
	('-M', White Package) (f = 60 Hz, t = 1 sec)		7500			Vac(pk)
lation Resistance	(V_{I-O} = 500 VDC)	R_{ISO}	10^{11}			Ω
lation Capacitance	(V_{I-O} = &, f = 1 MHz)	C_{ISO}		0.5		pF
	('-M' White Package)			0.2	2	pF

ical values at T_A = 25°C

RANSFER CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

Characteristic	Test Conditions	Symbol	Device	Min	Typ*	Max	Unit
rrent Transfer Ratio, llector to Emitter	(I_F = 10 mA, V_{CE} = 10 V)	CTR	4N35 4N36 4N37	100			%
			H11A1	50			
			H11A5	30			
			4N25 4N26 H11A2 H11A3	20			
			4N27 4N28 H11A4	10			
	(I_F = 10 mA, V_{CE} = 10 V, T_A = -55°C)		4N35 4N36 4N37	40			
	(I_F = 10 mA, V_{CE} = 10 V, T_A = +100°C)		4N35 4N36 4N37	40			
llector-Emitter turation Voltage	(I_C = 2 mA, I_F = 50 mA)	$V_{CE (SAT)}$	4N25 4N26 4N27 4N28			0.5	V
	(I_C = 0.5 mA, I_F = 10 mA)		4N35 4N36 4N37			0.3	
			H11A1 H11A2 H11A3 H11A4 H11A5			0.4	
Characteristic							
n-Saturated rn-on Time	(I_F = 10 mA, V_{CC} = 10 V, R_L = 100Ω) (Fig.20)	T_{ON}	4N25 4N26 4N27 4N28 H11A1 H11A2 H11A3 H11A4 H11A5		2		µs
n Saturated rn-on Time	(I_C = 2 mA, V_{CC} = 10 V, R_L = 100Ω) (Fig.20)	T_{ON}	4N35 4N36 4N37		2	10	µs

TRANSFER CHARACTERISTICS (T_A = 25°C Unless otherwise specified.) (Continued)

AC Characteristic	Test Conditions	Symbol	Device	Min	Typ*	Max	Unit
Turn-off Time	(I_F = 10 mA, V_{CC} = 10 V, R_L = 100Ω) (Fig.20)	T_{OFF}	4N25 4N26 4N27 4N28 H11A1 H11A2 H11A3 H11A4 H11A5		2		µs
	(I_C = 2 mA, V_{CC} = 10 V, R_L = 100Ω) (Fig.20)		4N35 4N36 4N37		2	10	

*Typical values at T_A = 25°C

'PICAL PERFORMANCE CURVES

Fig. 1 LED Forward Voltage vs. Forward Current (Black Package)

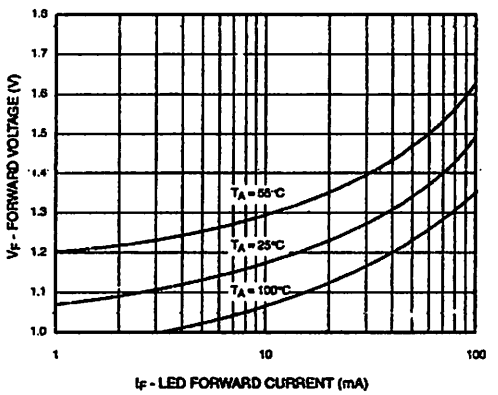


Fig. 2 LED Forward Voltage vs. Forward Current (White Package)

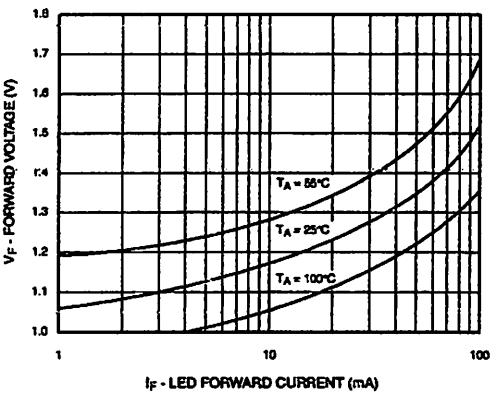


Fig.3 Normalized CTR vs. Forward Current (Black Package)

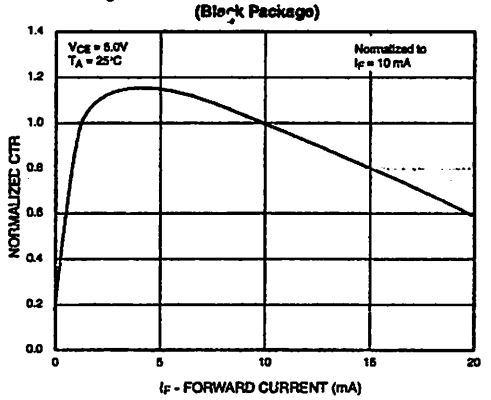


Fig.4 Normalized CTR vs. Forward Current (White Package)

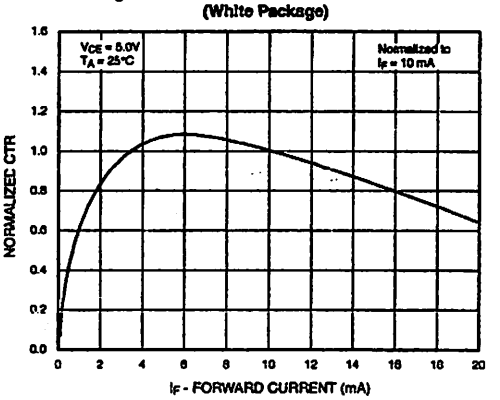


Fig. 5 Normalized CTR vs. Ambient Temperature (Black Package)

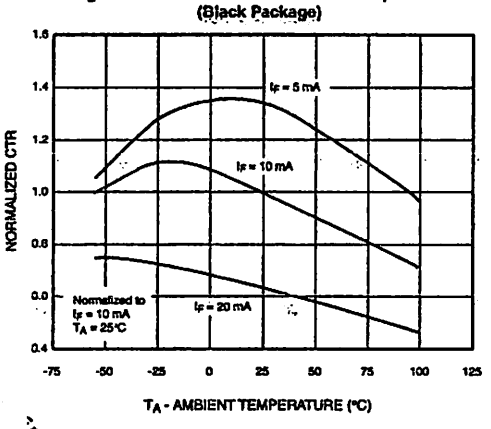


Fig. 6 Normalized CTR vs. Ambient Temperature (White Package)

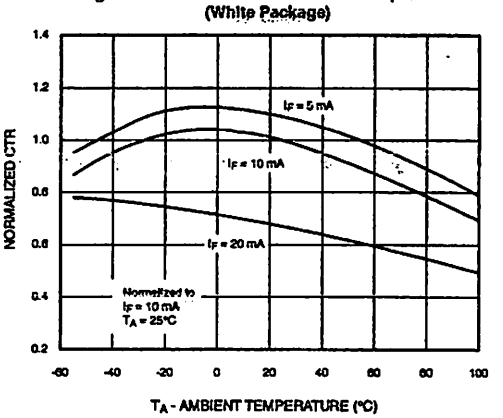


Fig. 7 CTR vs. RBE (Unsaturated)
(Black Package)

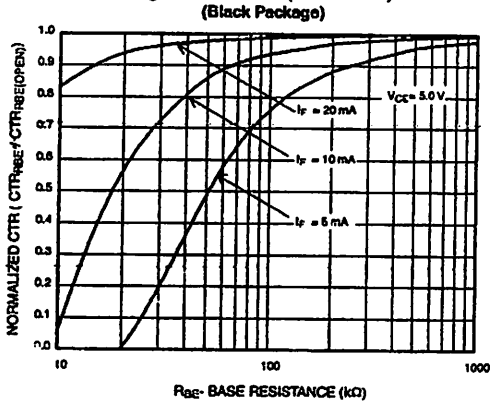


Fig. 8 CTR vs. RBE (Unsaturated)
(White Package)

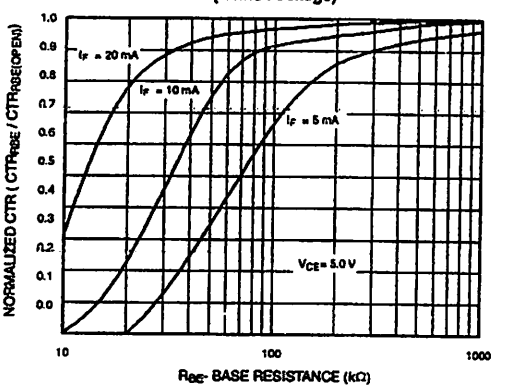


Fig. 9 CTR vs. RBE (Saturated)
(Black Package)

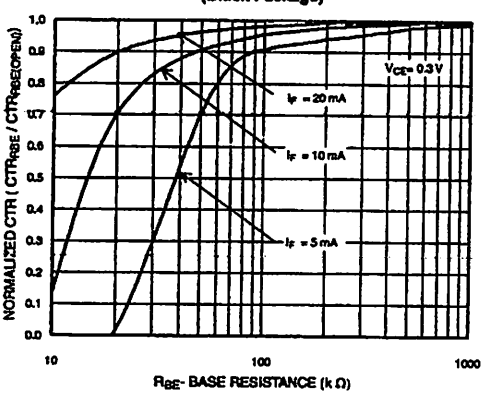


Fig. 10 CTR vs. RBE (Saturated)
(White Package)

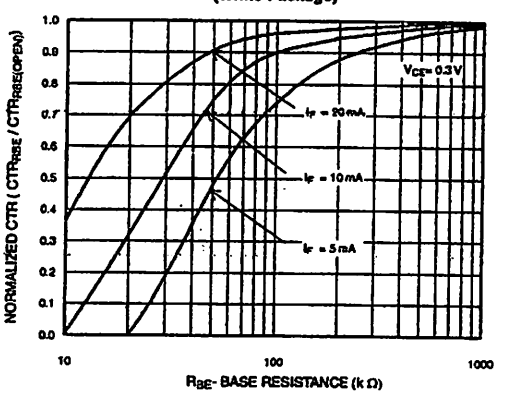


Fig. 11 Collector-Emitter Saturation Voltage vs Collector Current
(Black Package)

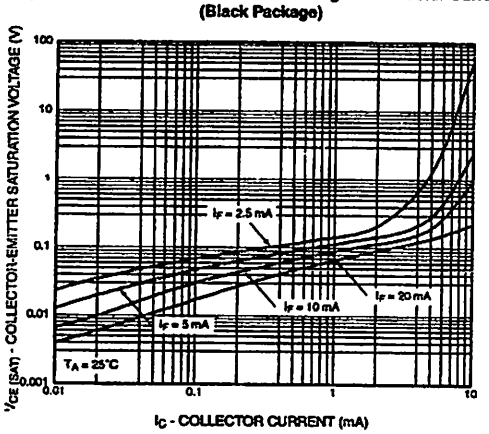


Fig. 12 Collector-Emitter Saturation Voltage vs Collector Current
(White Package)

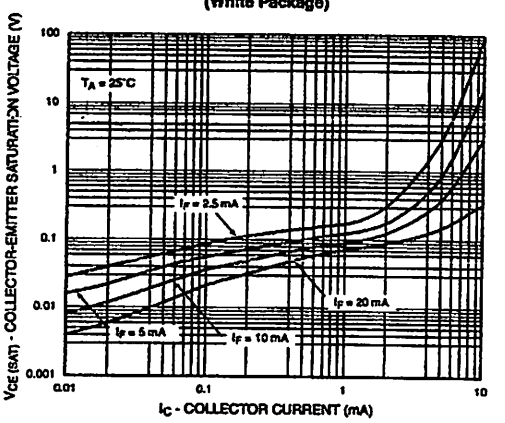


Fig. 13 Switching Speed vs. Load Resistor (Black Package)

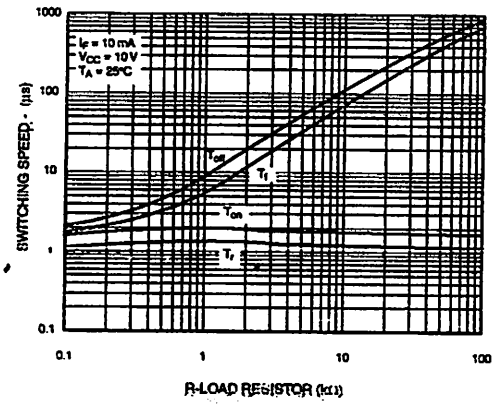


Fig. 14 Switching Speed vs. Load Resistor (White Package)

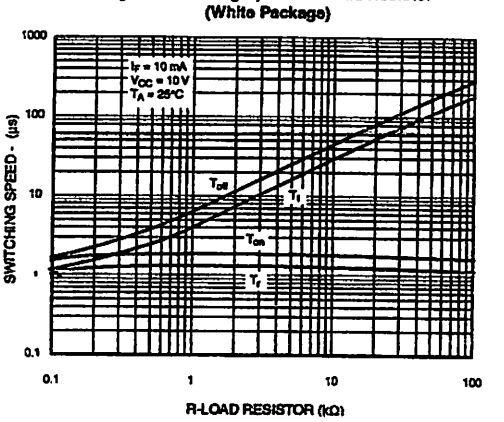


Fig. 15 Normalized t_{on} vs. R_{BE} (Black Package)

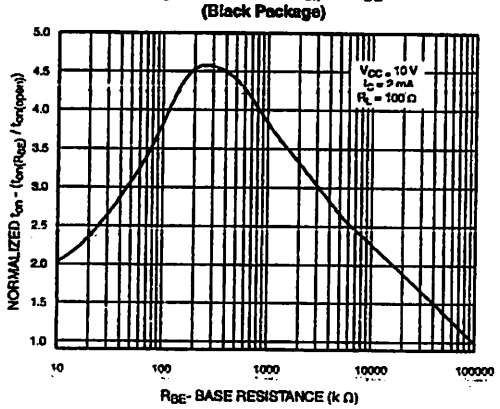


Fig. 16 Normalized t_{on} vs. R_{BE} (White Package)

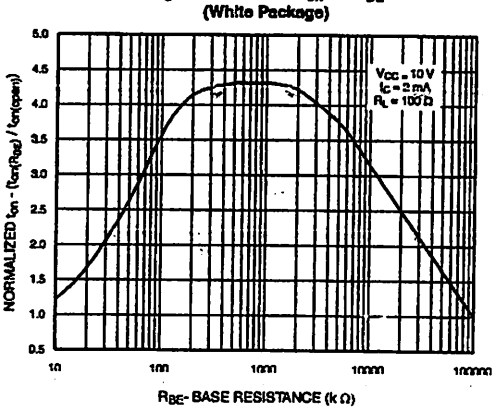


Fig. 17 Normalized t_{off} vs. R_{BE} (Black Package)

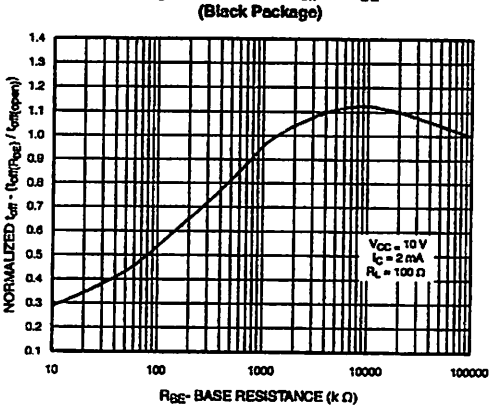


Fig. 18 Normalized t_{off} vs. R_{BE} (White Package)

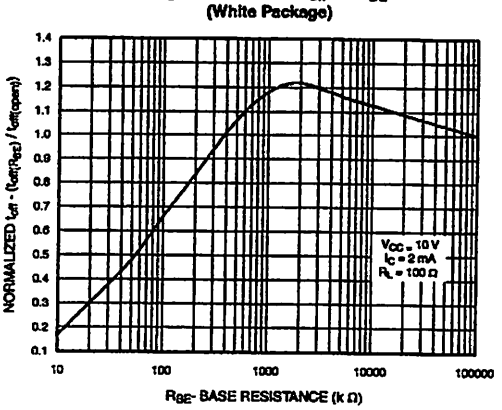
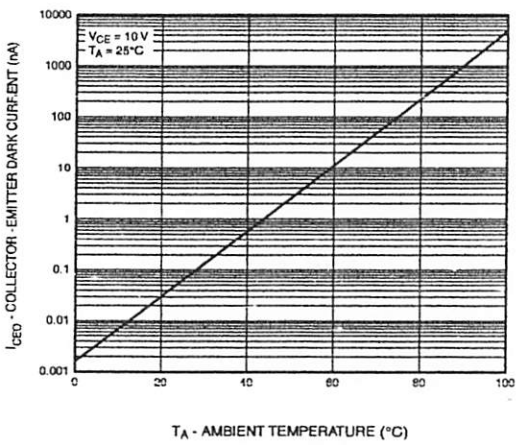


Fig. 19 Dark Current vs. Ambient Temperature



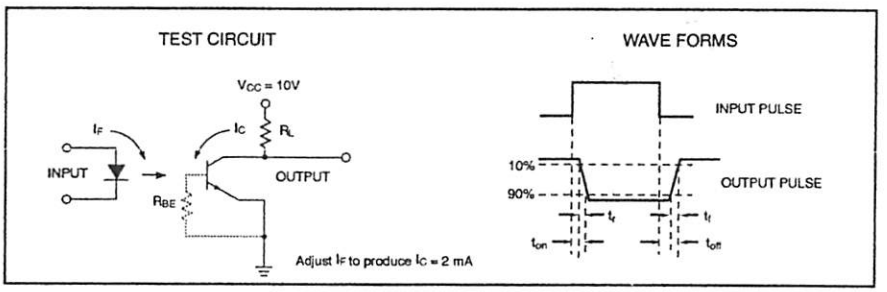


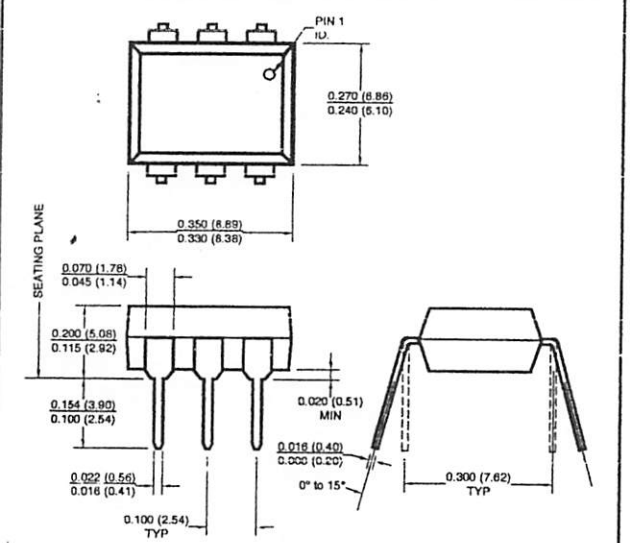
Figure 20. Switching Time Test Circuit and Waveforms

GENERAL PURPOSE 6-PIN PHOTOTRANSISTOR OPTOCOUPLERS

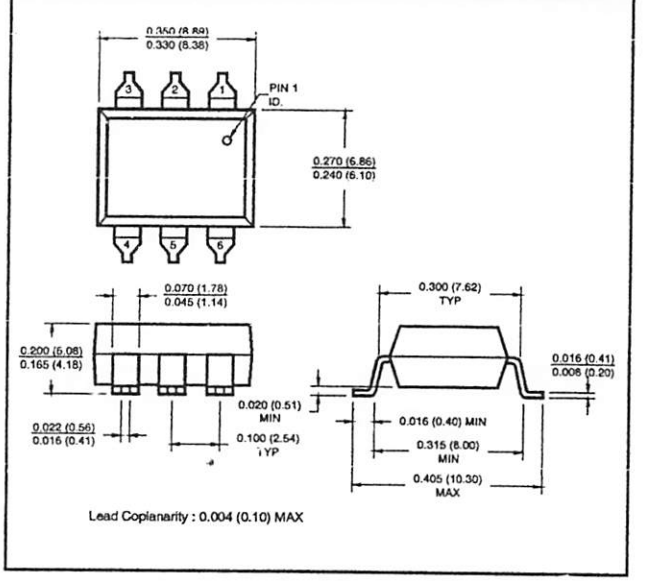
4N25	4N26	4N27	4N28	4N35	4N36
4N37	H11A1	H11A2	H11A3	H11A4	H11A5

Black Package (No -M Suffix)

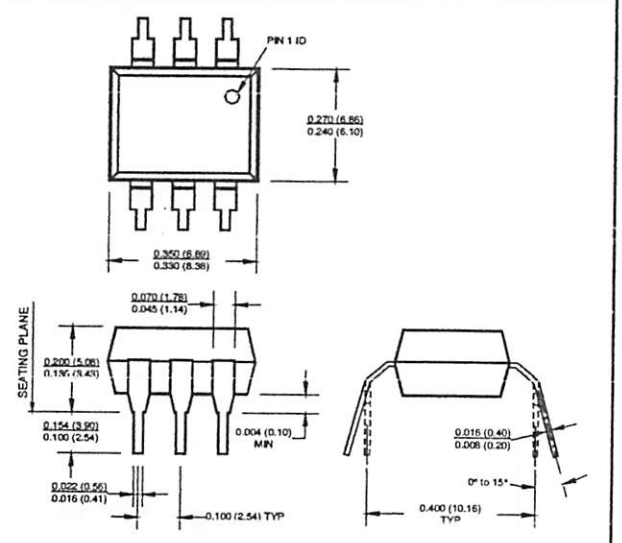
Package Dimensions (Through Hole)



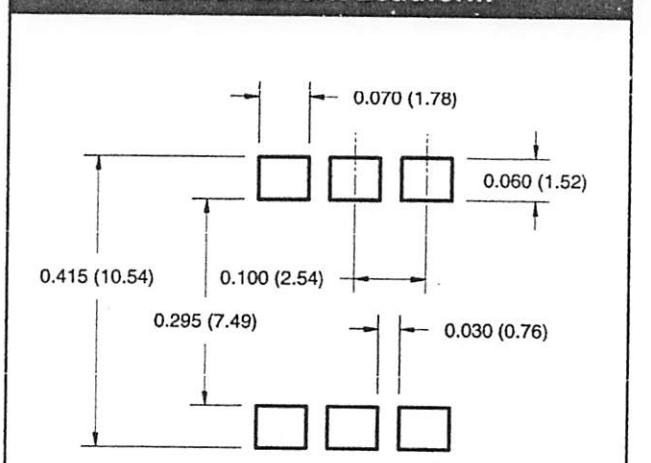
Package Dimensions (Surface Mount)



Package Dimensions (0.4" Lead Spacing)



Recommended Pad Layout for Surface Mount Leadform



NOTE
All dimensions are in inches (millimeters)

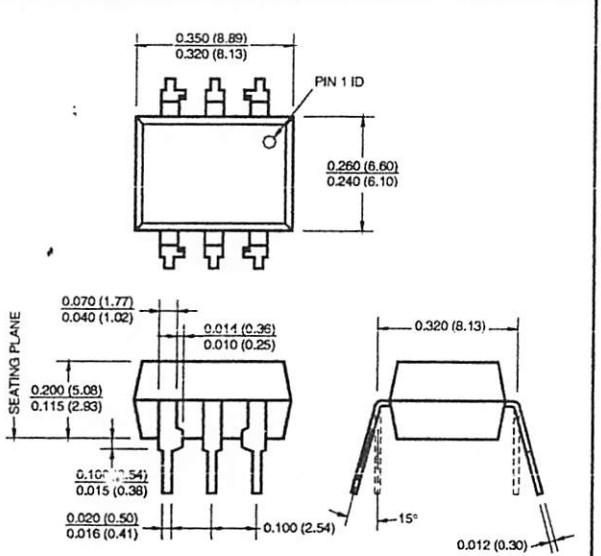
FAIRCHILD
SEMICONDUCTOR®

GENERAL PURPOSE 6-PIN PHOTOTRANSISTOR OPTOCOUPLERS

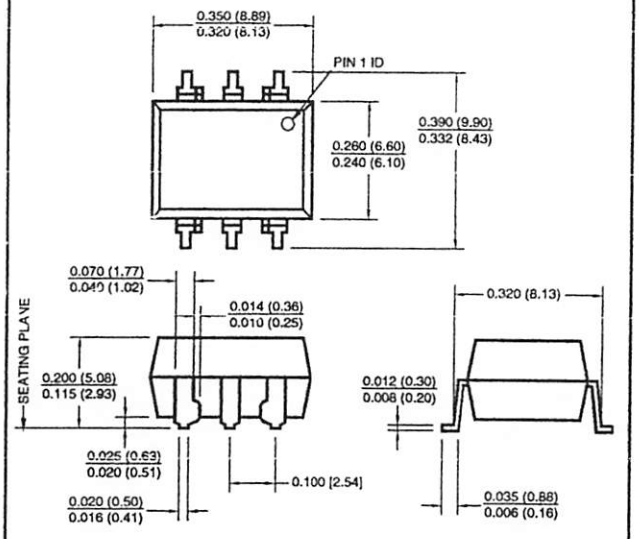
4N25	4N26	4N27	4N28	4N35	4N36
4N37	H11A1	H11A2	H11A3	H11A4	H11A5

White Package (-M Suffix)

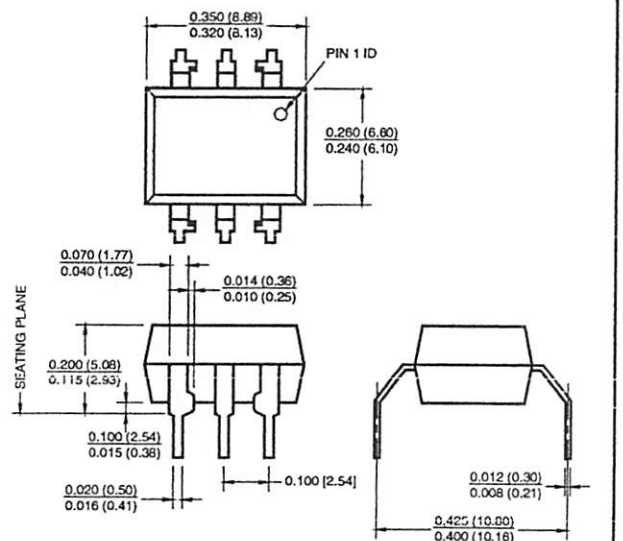
Package Dimensions (Through Hole)



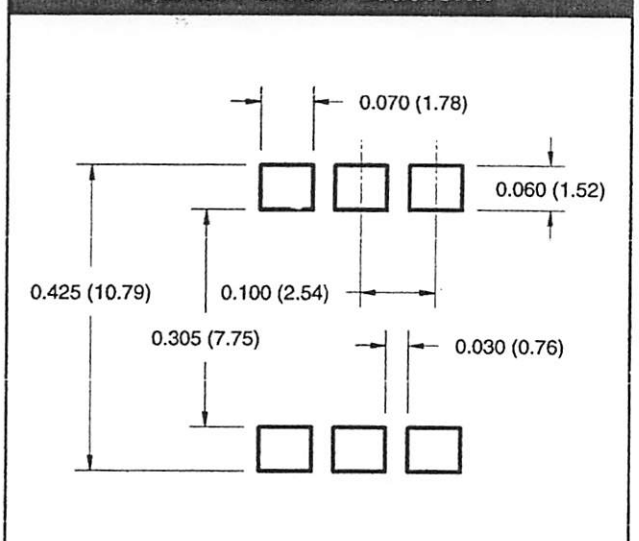
Package Dimensions (Surface Mount)



Package Dimensions (0.4" Lead Spacing)



Recommended Pad Layout for Surface Mount Leadform



NOTE

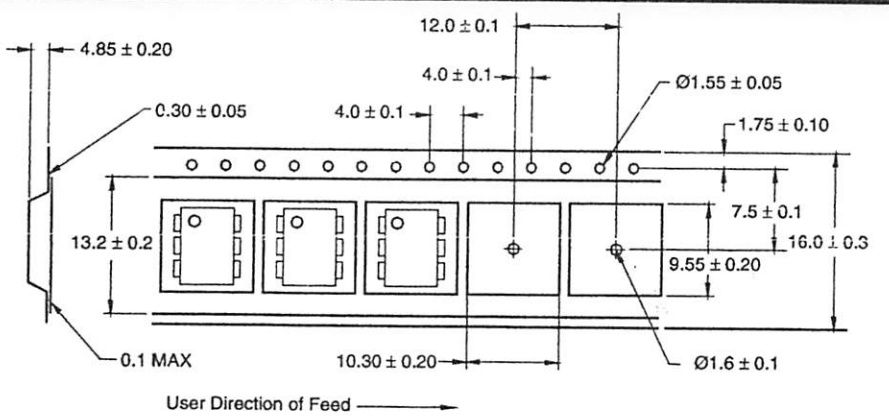
All dimensions are in inches (millimeters)

RDERING INFORMATION

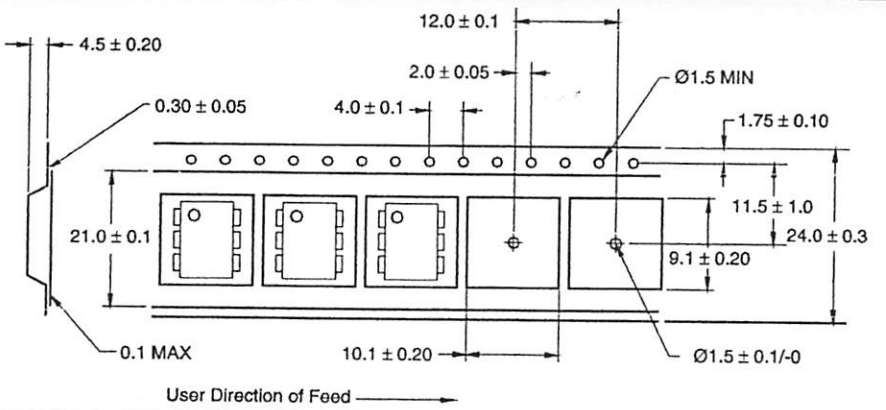
rder Entry Identifier

Black Package (No Suffix)	White Package (-M Suffix)	Option
.S	S	Surface Mount Lead Bend
.SD	SR2	Surface Mount; Tape and reel
.W	T	0.4" Lead Spacing
.300	V	VDE 0884
.300W	TV	VDE 0884, 0.4" Lead Spacing
.3S	SV	VDE 0884, Surface Mount
.3SD	SR2V	VDE 0884, Surface Mount, Tape & Reel

QT Carrier Tape Specifications (Black Package, No Suffix)



T Carrier Tape Specifications (White Package, -M Suffix)



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FAIRCHILD
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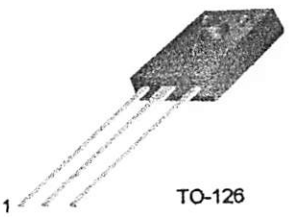
BD136/138/140

Medium Power Linear and Switching Applications

- Complement to BD135, BD137 and BD139 respectively



TO-126

1. Emitter 2.Collector 3.Base

PNP Epitaxial Silicon Transistor

Absolute Maximum Ratings T_C=25°C unless otherwise noted

Symbol	Parameter		Value	Units
V_{CBO}	Collector-Base Voltage	: BD136	- 45	V
		: BD138	- 60	V
		: BD140	- 80	V
V_{CEO}	Collector-Emitter Voltage	: BD136	- 45	V
		: BD138	- 60	V
		: BD140	- 80	V
V_{EBO}	Emitter-Base Voltage		- 5	V
I_C	Collector Current (DC)		- 1.5	A
I_{CP}	Collector Current (Pulse)		- 3.0	A
I_B	Base Current		- 0.5	A
P_C	Collector Dissipation (T_C=25°C)		12.5	W
P_C	Collector Dissipation (T_a=25°C)		1.25	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		- 55 ~ 150	°C

Electrical Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CEO}(sus)	* Collector-Emitter Sustaining Voltage					
	: BD136	I_C = - 30mA, I_B = 0	- 45			V
	: BD138		- 60			V
	: BD140		- 80			V
I_{CBO}	Collector Cut-off Current	V_{CB} = - 30V, I_E = 0			- 0.1	μA
I_{EBO}	Emitter Cut-off Current	V_{EB} = - 5V, I_C = 0			- 10	μA
h_{FE1}	* DC Current Gain	V_{CE} = - 2V, I_C = - 5mA	25			
h_{FE2}		V_{CE} = - 2V, I_C = - 0.5A	25			
h_{FE3}		V_{CE} = - 2V, I_C = - 150mA	40		250	
V_{CE}(sat)	* Collector-Emitter Saturation Voltage	I_C = - 500mA, I_B = - 50mA			- 0.5	V
V_{BE}(on)	* Base-Emitter ON Voltage	V_{CE} = - 2V, I_C = - 0.5A			- 1	V

* Pulse Test: PW=350μs, duty Cycle=2% Pulsed

h_{FE} Classificntion

Classification	6	10	16
h_{FE3}	40 ~ 100	63 ~ 160	100 ~ 250

Typical Characteristics

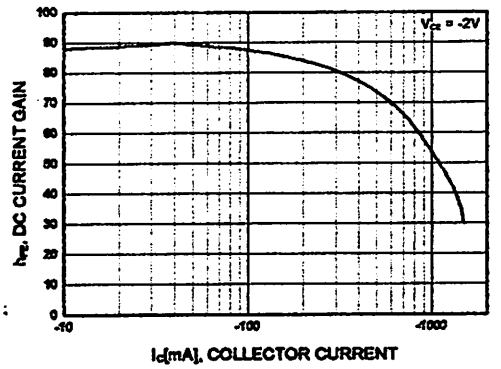


Figure 1. DC current Gain

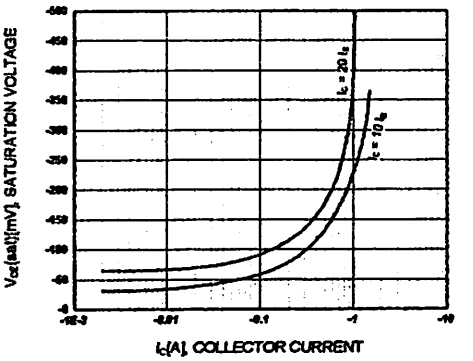


Figure 2. Collector-Emitter Saturation Voltage

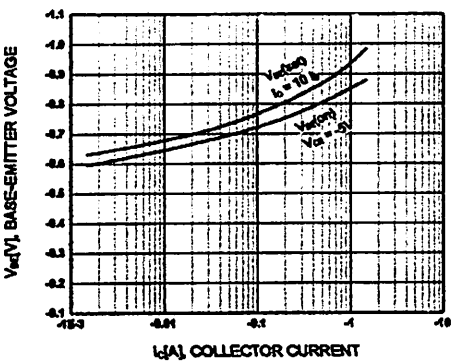


Figure 3. Base-Emitter Voltage

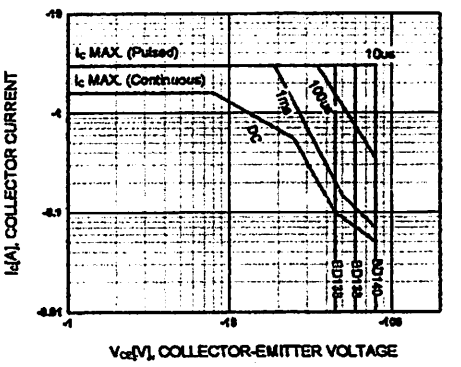


Figure 4. Safe Operating Area

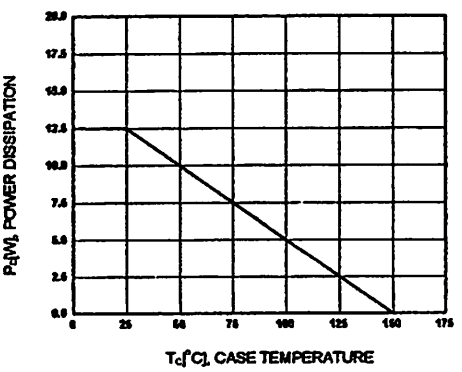
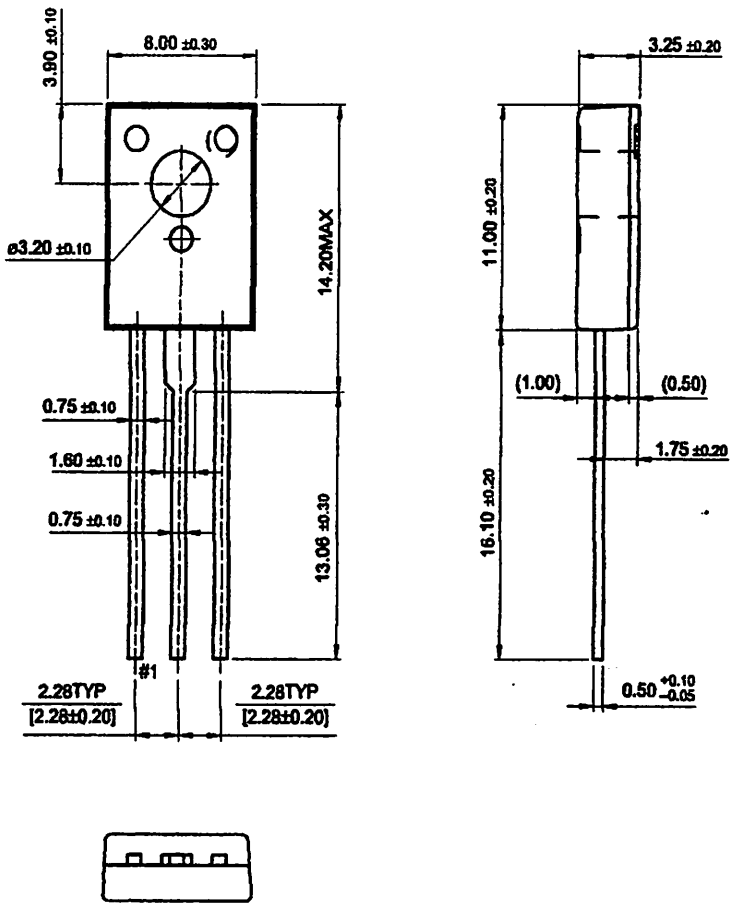


Figure 5. Power Derating

Package Demensions

TO-126



Dimensions in Millimeters

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POP™
PowerTrench®
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SuperSOT™-3
SuperSOT™-6
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

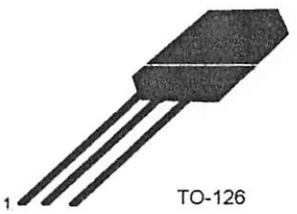
Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FAIRCHILD
SEMICONDUCTOR™

BD135/137/139

Medium Power Linear and Switching Applications

- Complement to BD136, BD138 and BD140 respectively



TO-126

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NPN Epitaxial Silicon Transistor

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		: BD137	60	V
		: BD139	80	V
V_{CEO}	Collector-Emitter Voltage	: BD135	45	V
		: BD137	60	V
		: BD139	80	V
V_{EBO}	Emitter-Base Voltage		5	V
I_C	Collector Current (DC)		1.5	A
I_{CP}	Collector Current (Pulse)		3.0	A
I_B	Base Current		0.5	A
P_C	Collector Dissipation (T_C=25°C)		12.5	W
P_C	Collector Dissipation (T_a=25°C)		1.25	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		- 55 ~ 150	°C

Electrical Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CEO}(sus)	Collector-Emitter Sustaining Voltage					
	: BD135	I_C = 30mA, I_B = 0	45			V
	: BD137		60			V
	: BD139		80			V
I_{CBO}	Collector Cut-off Current	V_{CB} = 30V, I_E = 0			0.1	µA
I_{EBO}	Emitter Cut-off Current	V_{EB} = 5V, I_C = 0			10	µA
h_{FE1}	DC Current Gain : ALL DEVICE	V_{CE} = 2V, I_C = 5mA	25			
h_{FE2}	: ALL DEVICE	V_{CE} = 2V, I_C = 0.5A	25			
h_{FE3}	: BD135	V_{CE} = 2V, I_C = 150mA	40		250	
	: BD137, BD139		40		160	
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C = 500mA, I_B = 50mA			0.5	V
V_{BE}(on)	Base-Emitter ON Voltage	V_{CE} = 2V, I_C = 0.5A			1	V

h_{FE} Classification

Classification	6	10	16
h_{FE3}	40 ~ 100	63 ~ 160	100 ~ 250

Typical Characteristics

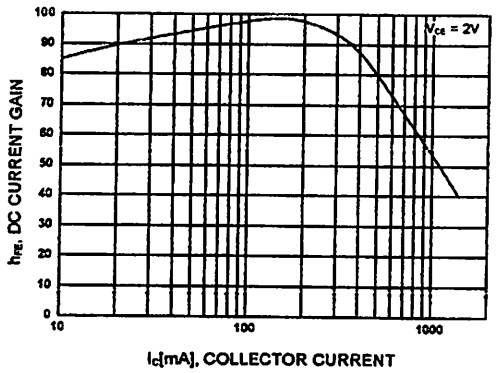


Figure 1. DC current Gain

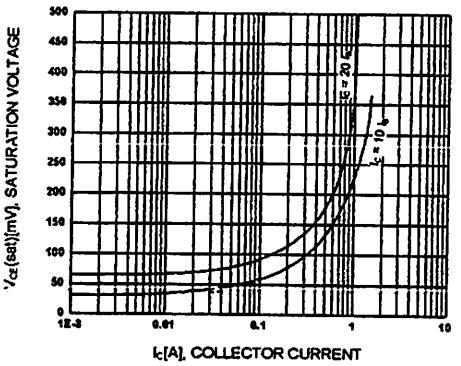


Figure 2. Collector-Emitter Saturation Voltage

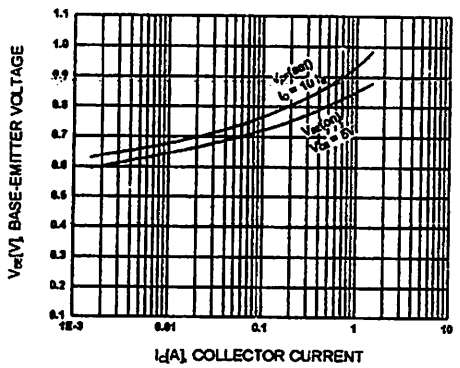


Figure 3. Base-Emitter Voltage

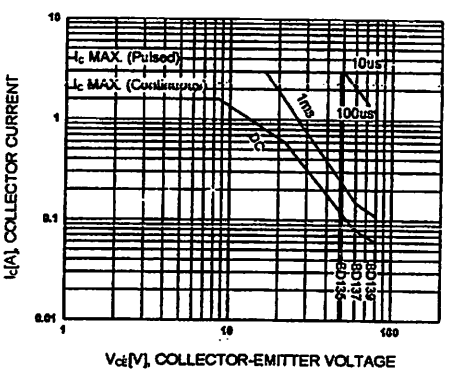


Figure 4. Safe Operating Area

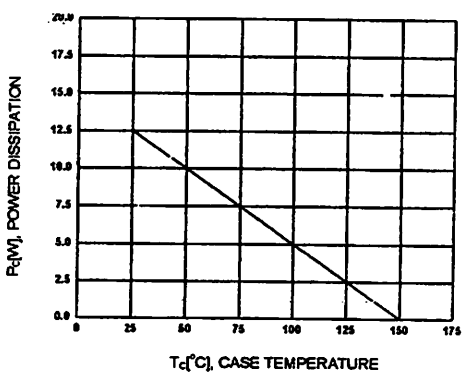
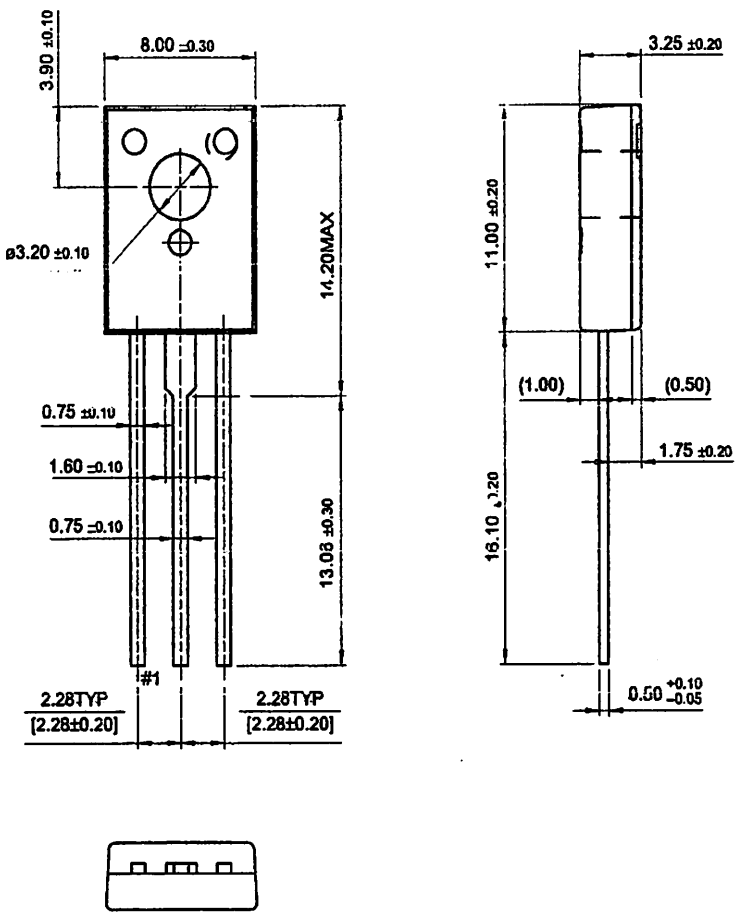


Figure 5. Power Derating

Package Demensions

TO-126



Dimensions in Millimeters

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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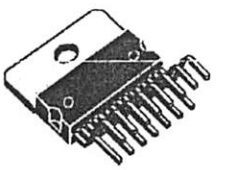
L298

DUAL FULL-BRIDGE DRIVER

- OPERATING SUPPLY VOLTAGE UP TO 46 V
- TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)



Multiwatt15

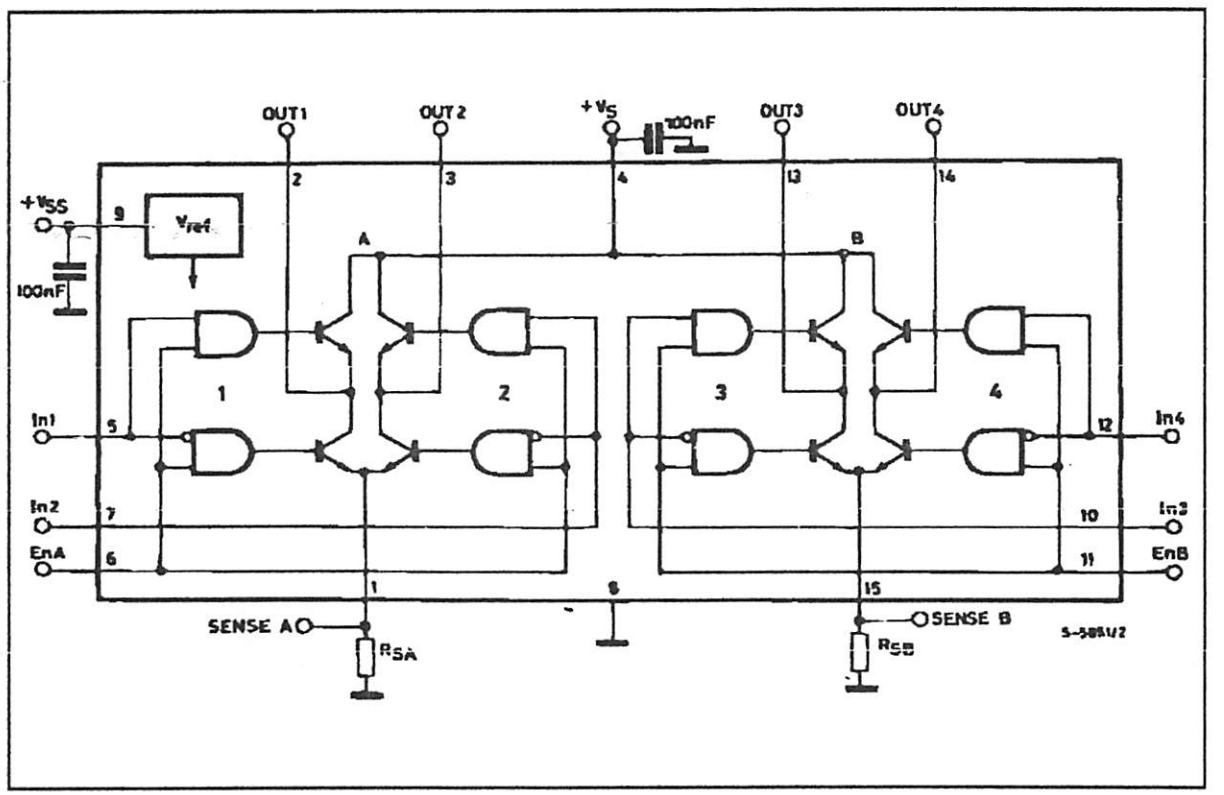
PowerSO20

ORDERING NUMBERS : L298N (Multiwatt Vert.)
L298HN (Multiwatt Horiz.)
L298P (PowerSO20)

DESCRIPTION

The L298 is an integrated monolithic circuit in a 15-lead Multiwatt and PowerSO20 packages. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

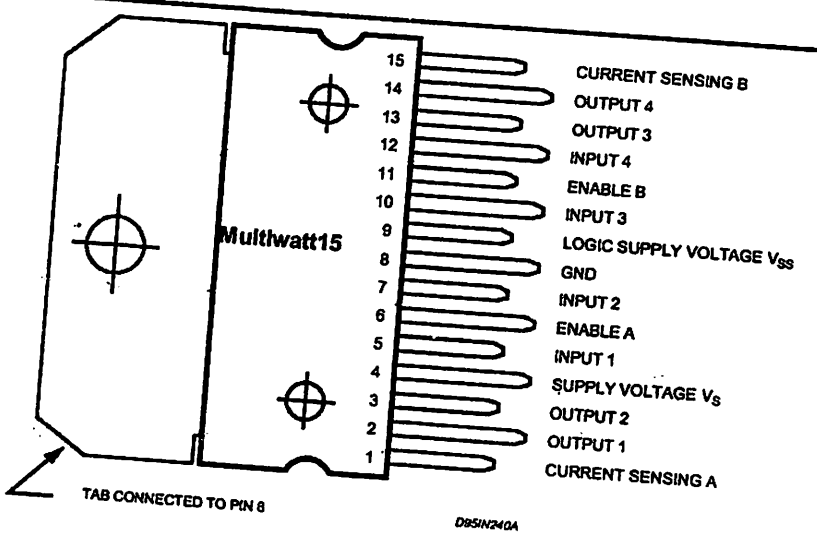
BLOCK DIAGRAM

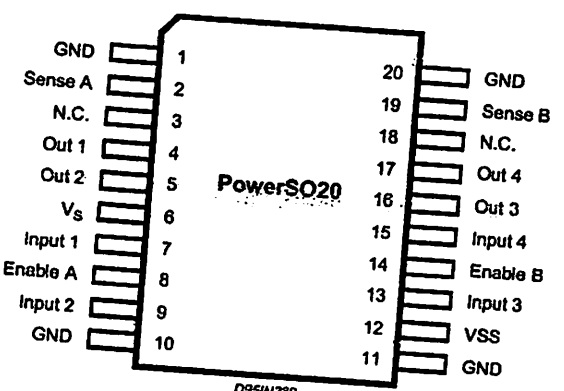


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply	50	V
V_{SS}	Logic Supply Voltage	7	V
V_I, V_{en}	Input and Enable Voltage	−0.3 to 7	V
I_O	Peak Output Current (each Channel) – Non Repetitive (t = 100µs) –Repetitive (80% on –20% off; t_{on} = 10ms) –DC Operation	 3 2.5 2	 A A A
V_{sens}	Sensing Voltage	−1 to 2.3	V
P_{tot}	Total Power Dissipation (T_{case} = 75°C)	25	W
T_{op}	Junction Operating Temperature	−25 to 130	°C
T_{stg}, T_j	Storage and Junction Temperature	−40 to 150	°C

PIN CONNECTIONS (top view)





THERMAL DATA

Symbol	Parameter		PowerSO20	Multiwatt15	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	–	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	13 (*)	35	°C/W

(*) Mounted on aluminum substrate

PIN FUNCTIONS (refer to the block diagram)

MW.15	PowerSO	Name	Function
1;15	2;19	Sense A; Sense B	Between this pin and ground is connected the sense resistor to control the current of the load.
2;3	4;5	Out 1; Out 2	Outputs of the Bridge A; the current that flows through the load connected between these two pins is monitored at pin 1.
4	6	V_S	Supply Voltage for the Power Output Stages. A non-inductive 100nF capacitor must be connected between this pin and ground.
5;7	7;9	Input 1; Input 2	TTL Compatible Inputs of the Bridge A.
6;11	8;14	Enable A; Enable B	TTL Compatible Enable Input: the L state disables the bridge A (enable A) and/or the bridge B (enable B).
8	1,10,11,20	GND	Ground.
9	12	VSS	Supply Voltage for the Logic Blocks. A100nF capacitor must be connected between this pin and ground.
10; 12	13;15	Input 3; Input 4	TTL Compatible Inputs of the Bridge B.
13; 14	16;17	Out 3; Out 4	Outputs of the Bridge B. The current that flows through the load connected between these two pins is monitored at pin 15.
–	3;18	N.C.	Not Connected

ELECTRICAL CHARACTERISTICS (V_S = 42V; V_{SS} = 5V, T_j = 25°C; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 4)	Operative Condition	V_{IH} +2.5		46	V
V_{SS}	Logic Supply Voltage (pin 9)		4.5	5	7	V
I_S	Quiescent Supply Current (pin 4)	V_{en} = H; I_L = 0 V_i = L		13	22	mA
		V_i = H		50	70	mA
		V_{en} = L V_i = X			4	mA
I_{SS}	Quiescent Current from V_{SS} (pin 9)	V_{en} = H; I_L = 0 V_i = L		24	36	mA
		V_i = H		7	12	mA
		V_{en} = L V_i = X			6	mA
V_{iL}	Input Low Voltage (pins 5, 7, 10, 12)		–0.3		1.5	V
V_{iH}	Input High Voltage (pins 5, 7, 10, 12)		2.3		VSS	V
I_{iL}	Low Voltage Input Current (pins 5, 7, 10, 12)	V_i = L			–10	µA
I_{iH}	High Voltage Input Current (pins 5, 7, 10, 12)	Vi = H ≤ V_{SS} –0.6V		30	100	µA
V_{en} = L	Enable Low Voltage (pins 6, 11)		–0.3		1.5	V
V_{en} = H	Enable High Voltage (pins 6, 11)		2.3		V_{SS}	V
I_{en} = L	Low Voltage Enable Current (pins 6, 11)	V_{en} = L			–10	µA
I_{en} = H	High Voltage Enable Current (pins 6, 11)	V_{en} = H ≤ V_{SS} –0.6V		30	100	µA
$V_{CEsat(H)}$	Source Saturation Voltage	I_L = 1A	0.95	1.35	1.7	V
		I_L = 2A		2	2.7	V
$V_{CEsat(L)}$	Sink Saturation Voltage	I_L = 1A (5)	0.85	1.2	1.6	V
		I_L = 2A (5)		1.7	2.3	V
V_{CEsat}	Total Drop	I_L = 1A (5)	1.80		3.2	V
		I_L = 2A (5)			4.9	V
V_{sens}	Sensing Voltage (pins 1, 15)		–1 (1)		2	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_1 (V_i)	Source Current Turn-off Delay	0.5 V_i to 0.9 I_L (2); (4)		1.5		µs
T_2 (V_i)	Source Current Fall Time	0.9 I_L to 0.1 I_L (2); (4)		0.2		µs
T_3 (V_i)	Source Current Turn-on Delay	0.5 V_i to 0.1 I_L (2); (4)		2		µs
T_4 (V_i)	Source Current Rise Time	0.1 I_L to 0.9 I_L (2); (4)		0.7		µs
T_5 (V_i)	Sink Current Turn-off Delay	0.5 V_i to 0.9 I_L (3); (4)		0.7		µs
T_6 (V_i)	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3); (4)		0.25		µs
T_7 (V_i)	Sink Current Turn-on Delay	0.5 V_i to 0.9 I_L (3); (4)		1.6		µs
T_8 (V_i)	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3); (4)		0.2		µs
fc (V_i)	Commutation Frequency	I_L = 2A		25	40	KHz
T_1 (V_{en})	Source Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (2); (4)		3		µs
T_2 (V_{en})	Source Current Fall Time	0.9 I_L to 0.1 I_L (2); (4)		1		µs
T_3 (V_{en})	Source Current Turn-on Delay	0.5 V_{en} to 0.1 I_L (2); (4)		0.3		µs
T_4 (V_{en})	Source Current Rise Time	0.1 I_L to 0.9 I_L (2); (4)		0.4		µs
T_5 (V_{en})	Sink Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (3); (4)		2.2		µs
T_6 (V_{en})	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3); (4)		0.35		µs
T_7 (V_{en})	Sink Current Turn-on Delay	0.5 V_{en} to 0.9 I_L (3); (4)		0.25		µs
T_8 (V_{en})	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3); (4)		0.1		µs

1) 1)Sensing voltage can be –1 V for t ≤ 50 µsec; in steady state V_{sens} min ≥ –0.5 V.
2) See fig. 2.
3) See fig. 4.
4) The load must be a pure resistor.

Figure 1 : Typical Saturation Voltage vs. Output Current.

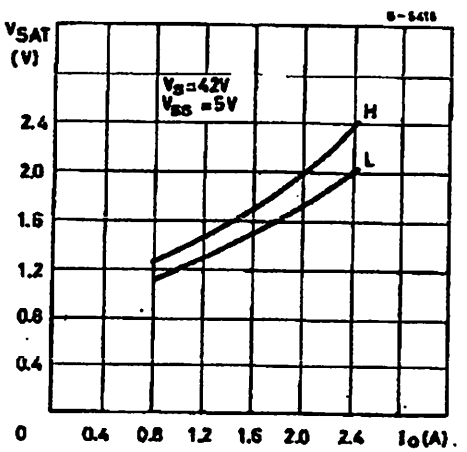
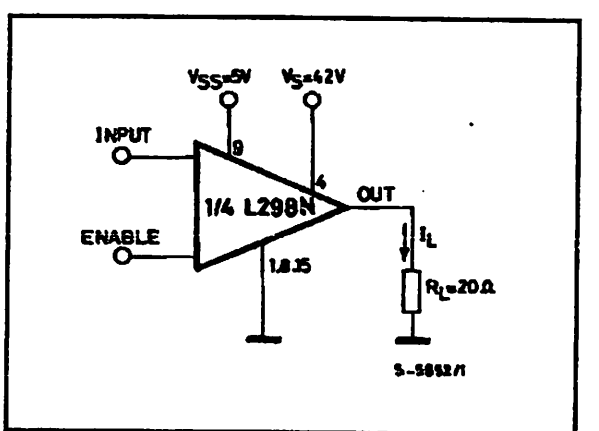


Figure 2 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = H

Figure 3 : Source Current Delay Times vs. Input or Enable Switching.

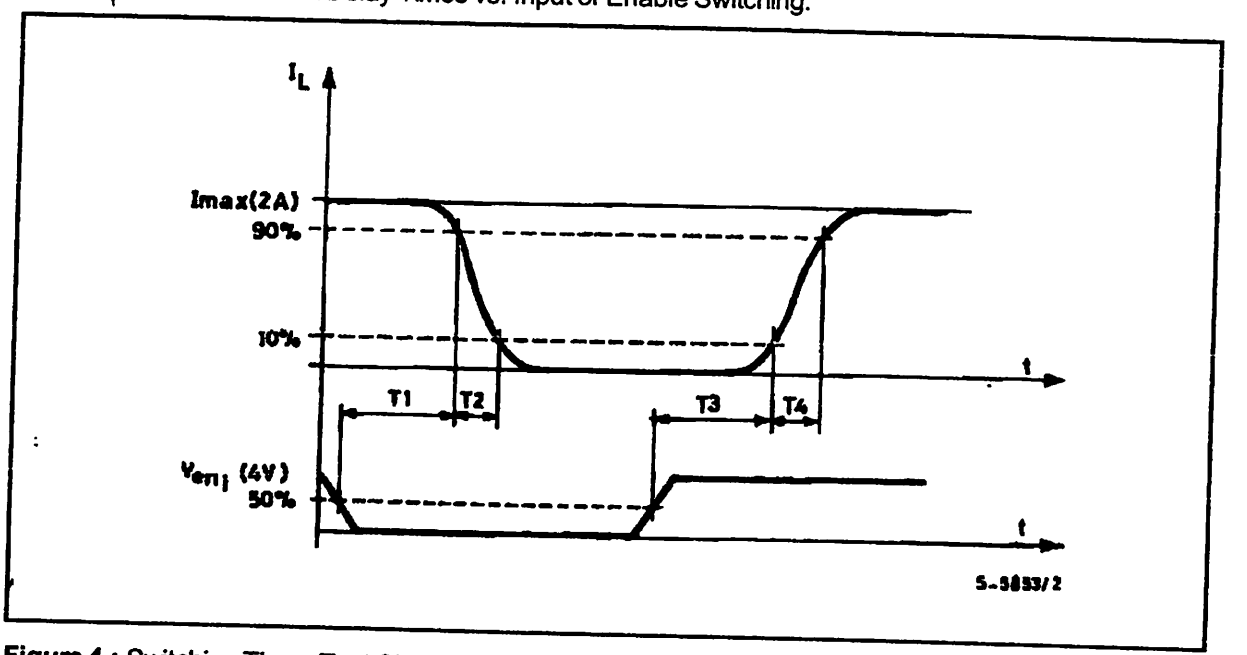
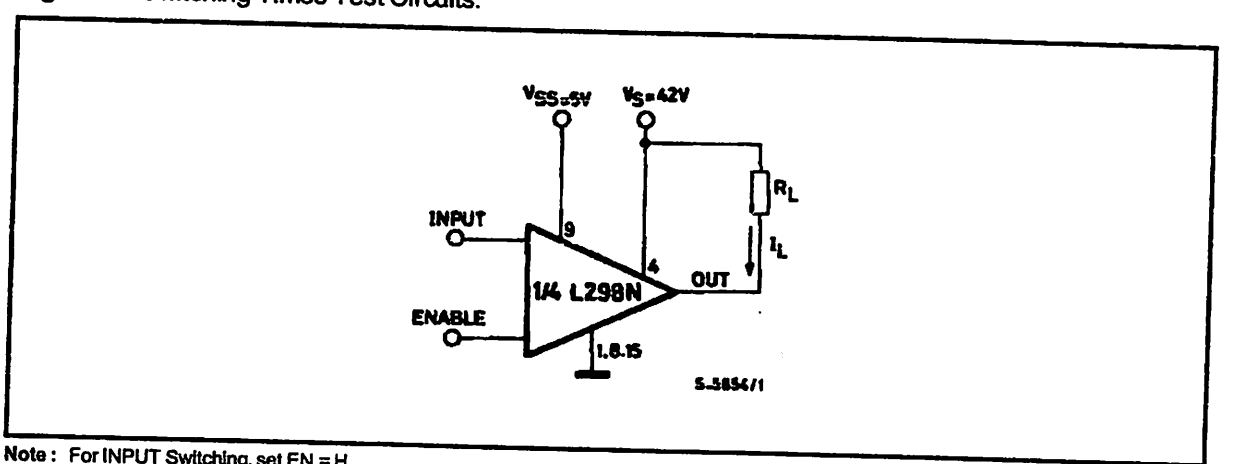


Figure 4 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = L

Figure 5 : Sink Current Delay Times vs. Input 0 V Enable Switching.

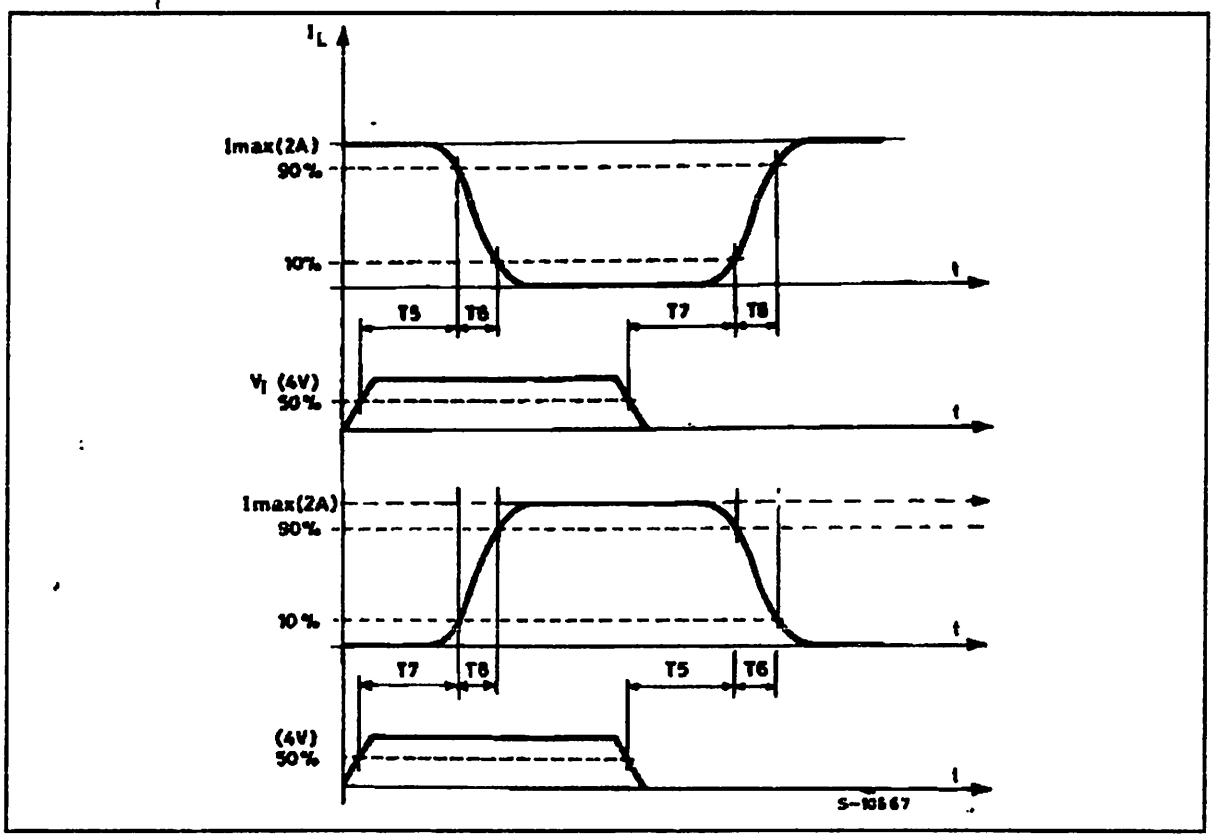
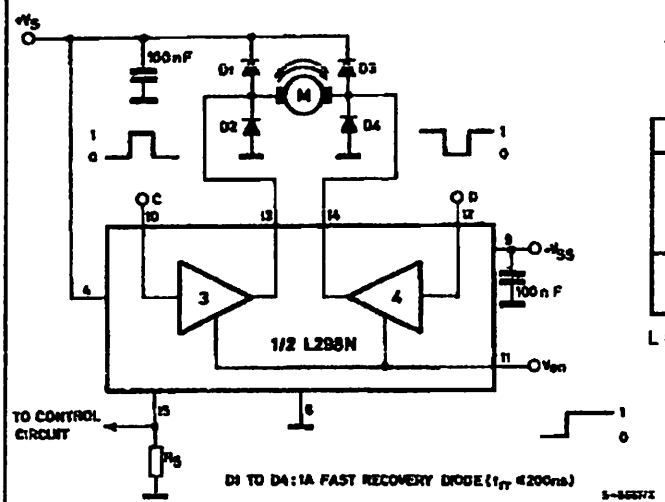


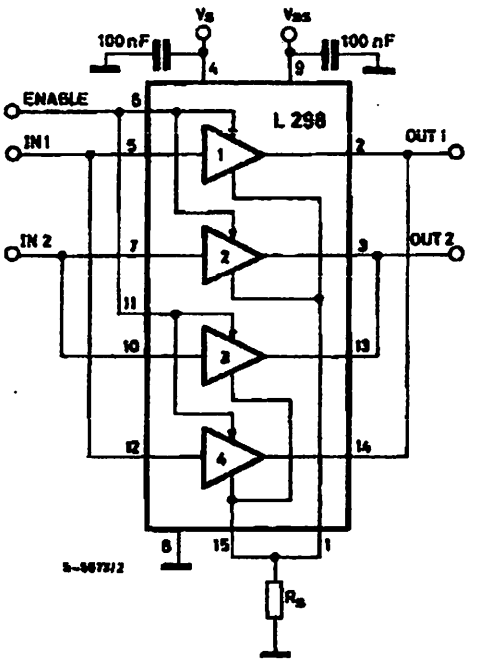
Figure 6 : Bidirectional DC Motor Control.



Inputs		Function
V_{en} = H	C = H ; D = L	Forward
	C = L ; D = H	Reverse
	C = D	Fast Motor Stop
V_{en} = L	C = X ; D = X	Free Running Motor Stop

L = Low H = High X = Don't care

Figure 7 : For higher currents, outputs can be paralleled. Take care to parallel channel 1 with channel 4 and channel 2 with channel 3.



APPLICATION INFORMATION (Refer to the block diagram)

1.1. POWER OUTPUT STAGE

The L298 integrates two power output stages (A; B). The power output stage is a bridge configuration and its outputs can drive an inductive load in common or differenzial mode, depending on the state of the inputs. The current that flows through the load comes out from the bridge at the sense output: an external resistor (R_{SA} ; R_{SB}.) allows to detect the intensity of this current.

1.2. INPUT STAGE

Each bridge is driven by means of four gates the input of which are In1 ; In2 ; EnA and In3 ; In4 ; EnB. The In inputs set the bridge state when The En input is high ; a low state of the En input inhibits the bridge. All the inputs are TTL compatible.

2. SUGGESTIONS

A non inductive capacitor, usually of 100 nF, must be foreseen between both Vs and Vss, to ground, as near as possible to GND pin. When the large capacitor of the power supply is too far from the IC, a second smaller one must be foreseen near the L298.

The sense resistor, not of a wire wound type, must be grounded near the negative pole of Vs that must be near the GND pin of the I.C.

Each input must be connected to the source of the driving signals by means of a very short path.

Turn-On and Turn-Off : Before to Turn-ON the Supply Voltage and before to Turn it OFF, the Enable input must be driven to the Low state.

3. APPLICATIONS

Fig 6 shows a bidirectional DC motor control Schematic Diagram for which only one bridge is needed. The external bridge of diodes D1 to D4 is made by four fast recovery elements ($t_{rr} \leq 200$ nsec) that must be chosen of a VF as low as possible at the worst case of the load current.

The sense output voltage can be used to control the current amplitude by chopping the inputs, or to provide overcurrent protection by switching low the enable input.

The brake function (Fast motor stop) requires that the Absolute Maximum Rating of 2 Amps must never be overcome.

When the repetitive peak current needed from the load is higher than 2 Amps, a paralleled configuration can be chosen (See Fig.7).

An external bridge of diodes are required when inductive loads are driven and when the inputs of the IC are chopped; Shottky diodes would be preferred.

This solution can drive until 3 Amps In DC operation and until 3.5 Amps of a repetitive peak current.

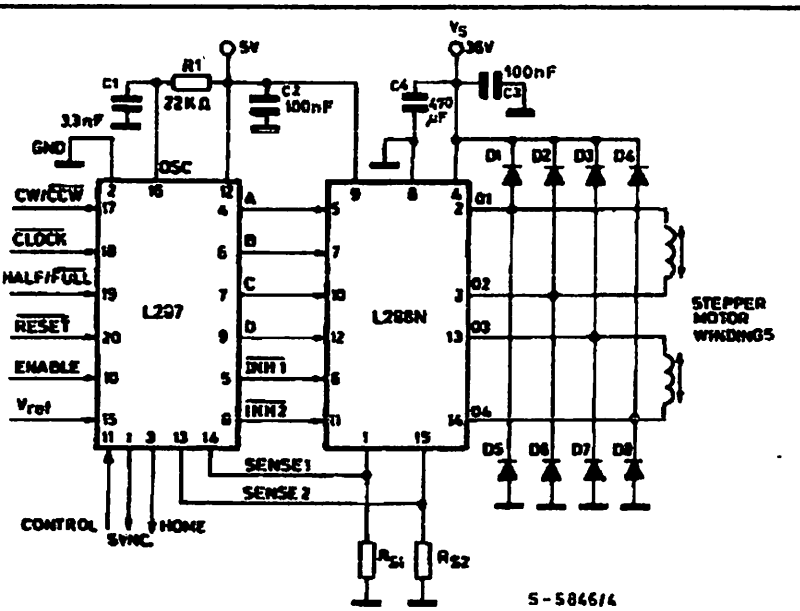
On Fig 8 it is shown the driving of a two phase bipolar stepper motor ; the needed signals to drive the inputs of the L298 are generated, in this example, from the IC L297.

Fig 9 shows an example of P.C.B. designed for the application of Fig 8.

Fig 10 shows a second two phase bipolar stepper motor control circuit where the current is controlled by the I.C. L6506.

Figure 8 : Two Phase Bipolar Stepper Motor Circuit.

This circuit drives bipolar stepper motors with winding currents up to 2 A. The diodes are fast 2 A types.



$R_{S1} = R_{S2} = 0.5\,\Omega$

D1 to D8 = 2 A Fast diodes { $V_F \leq 1.2\,V$ @ $I = 2\,A$; $t_{rr} \leq 200\,ns$

Figure 9 : Suggested Printed Circuit Board Layout for the Circuit of fig. 8 (1:1 scale).

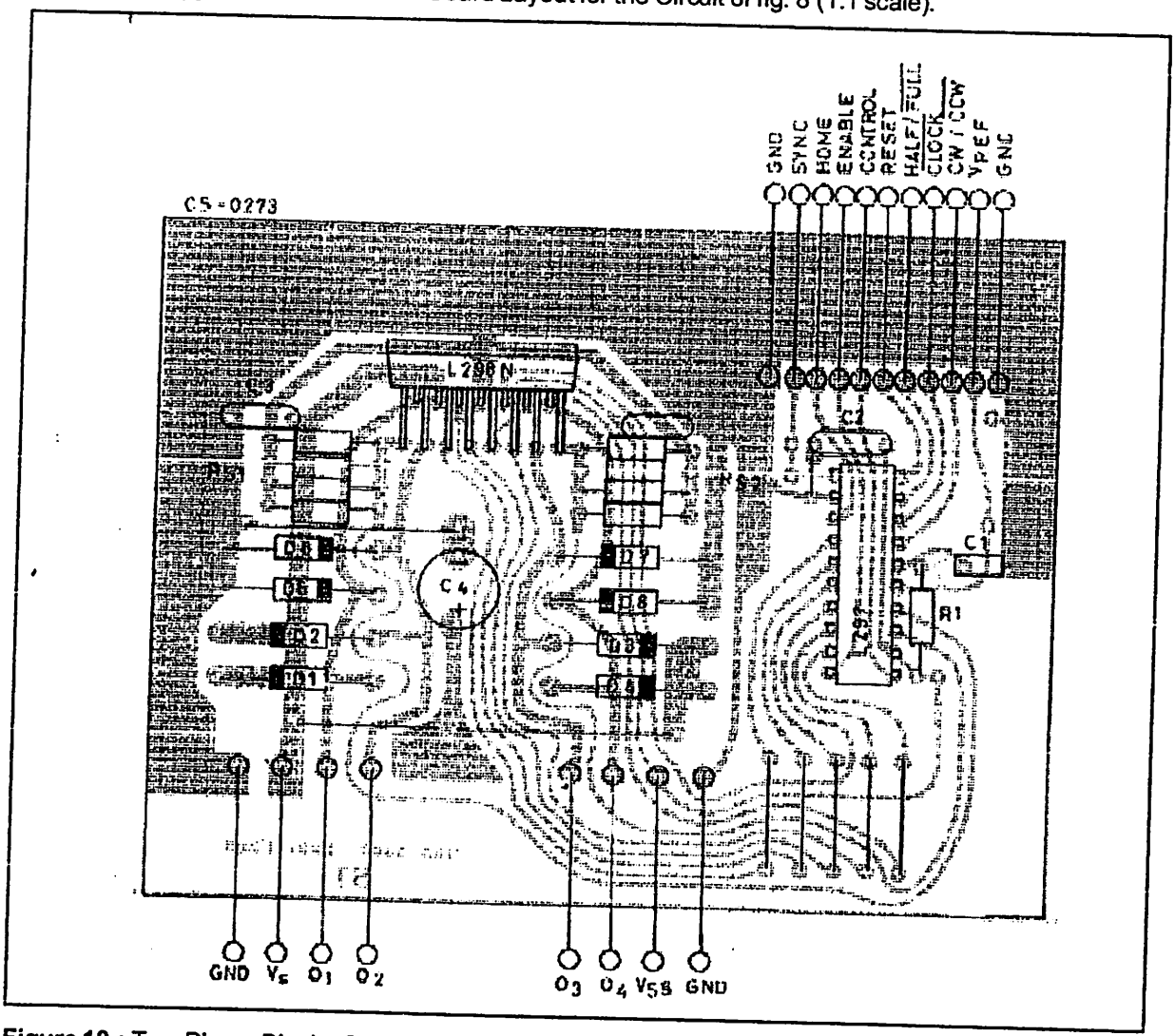
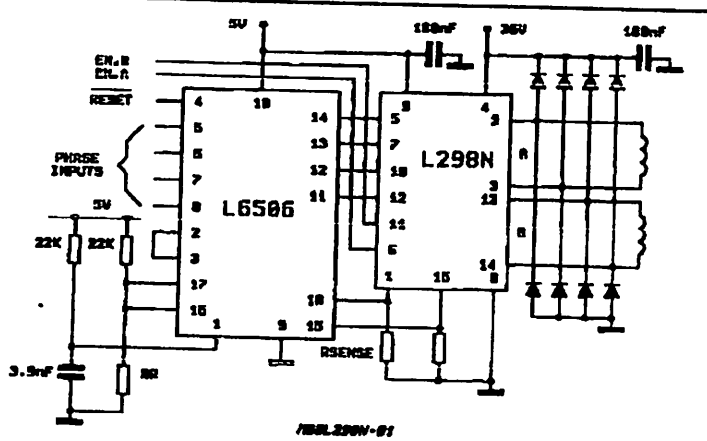


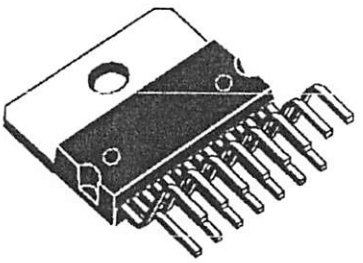
Figure 10 : Two Phase Bipolar Stepper Motor Control Circuit by Using the Current Controller L6506.



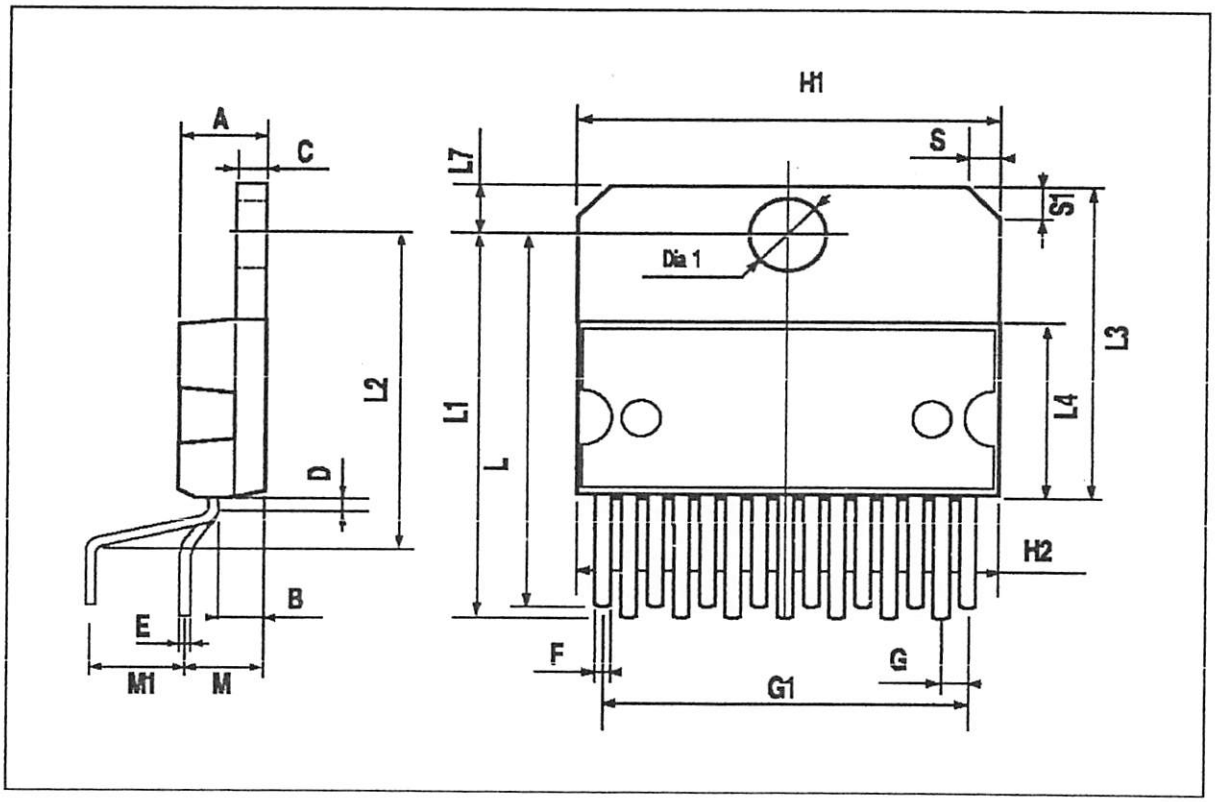
R_R and R_{sense} depend from the load current

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.870	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.63	5.08	5.53	0.182	0.200	0.218
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA

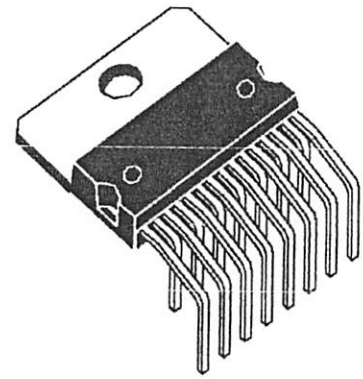


Multiwatt15 V

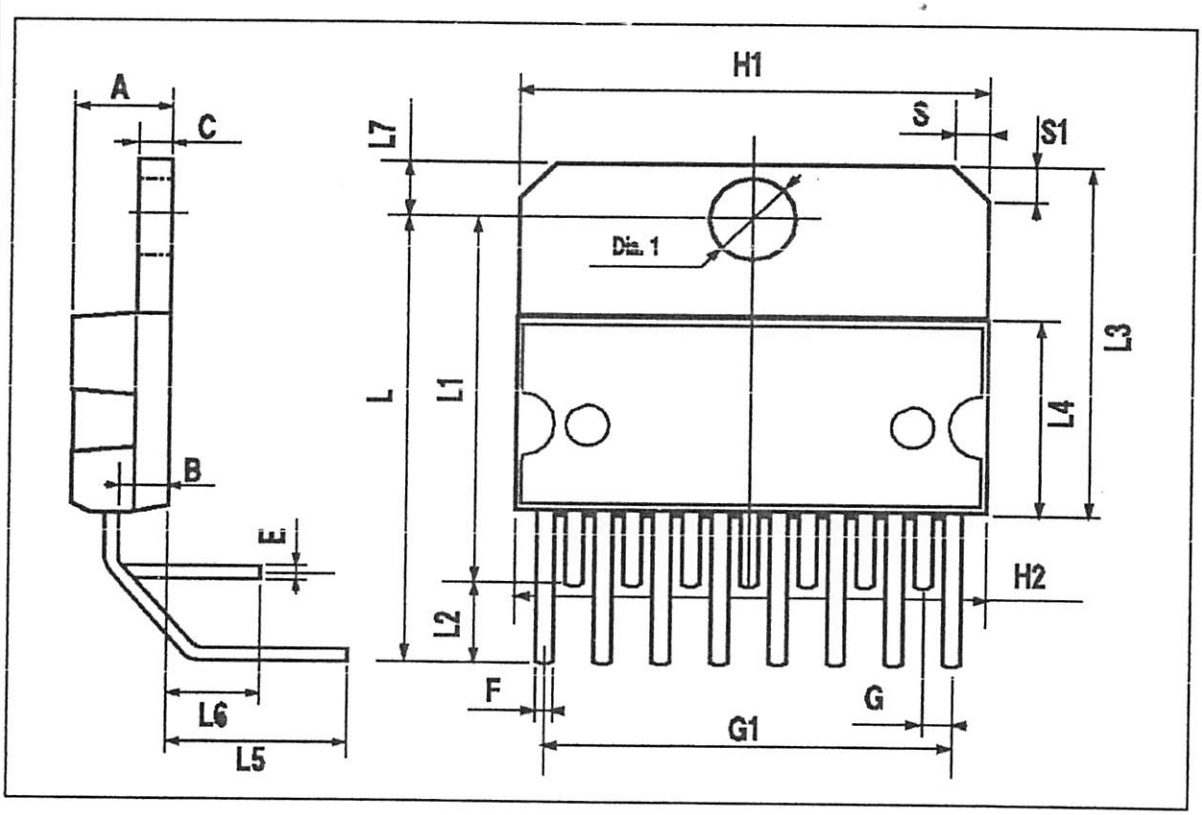


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L		20.57			0.810	
L1		18.03			0.710	
L2		2.54			0.100	
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L5		5.28			0.208	
L6		2.38			0.094	
L7	2.65		2.9	0.104		0.114
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



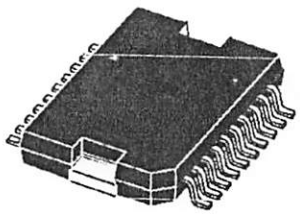
Multiwatt15 H



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	10° (max.)					
S	8° (max.)					
T		10			0.394	

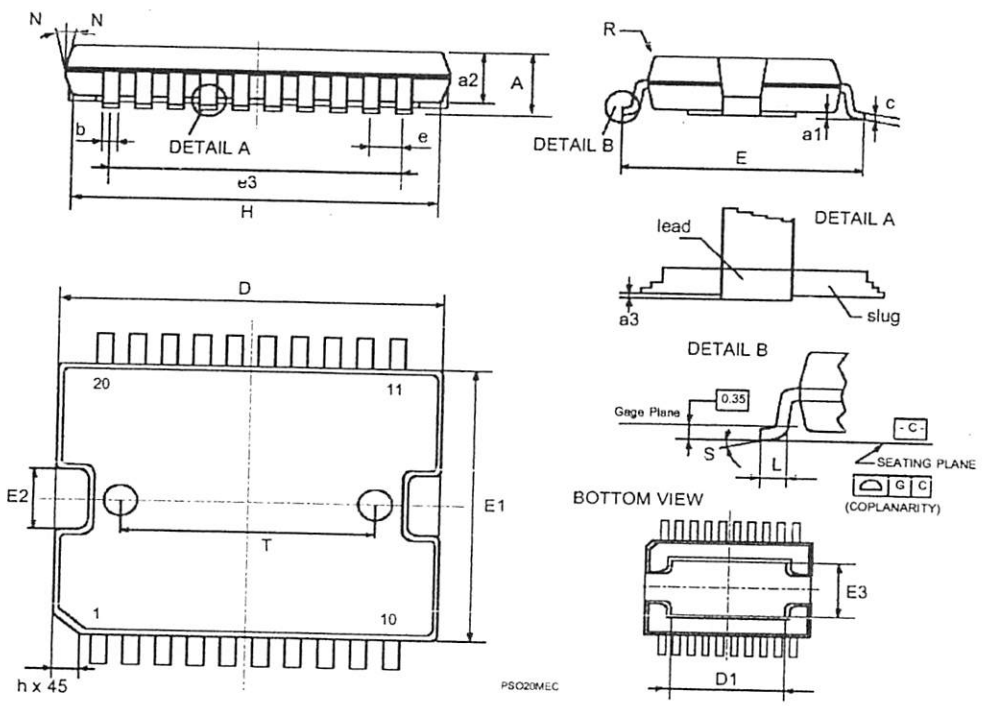
(1) "D and F" do not include mold flash or protrusions.
- Mold flash or protrusions shall not exceed 0.15 mm (0.006").
- Critical dimensions: "E", "G" and "a3"

OUTLINE AND MECHANICAL DATA



JEDEC MO-166

PowerSO20



```
'Port seting
'P1.3   = heter
'P2     = data adc
'P1.1   = start adc
'P1.0   = PWM driver
'P1.2   = level air
'Keypad  = port 3

$large
$crystal = 12000000
'$sim

Config Lcdpin = Pin , Db4 = P0.4 , Db5 = P0.5 , Db6 = P0.6 , Db7 = P0.7 , E = P0.3 , Rs = P0.2
Config Lcd = 16 * 2
Display On
Cursor Off
Cls

Start_adc Alias P1.1
Level_air Alias P1.2
Pwm Alias P1.0
Heater Alias P1.3

Kolom4 Alias P3.0
Kolom3 Alias P3.1
Kolom2 Alias P3.2
Kolom1 Alias P3.3

Dim Togle_bit As Boolean

Dim Key As Integer
Dim Finish As Integer

Dim Data_keypad As Integer
Dim Adc_suhu As Byte
Dim Seting_suhu As Byte
Dim Seting_waktu As Byte
Dim Waktu As Word
Dim Kursor As Integer
Dim Posisi As Integer
Dim Msb As Byte
Dim Lsb As Byte
Dim Hasil As Byte
Dim Tempo1 As Byte
Dim Tempo2 As Byte
Dim Detik As Byte
Dim Menit As Byte


Dim Data_pwm As Byte
Dim Temp As Byte

Const Cor = 10
Const Men = 20
Const Up = 30
Const Down = 40
Const Cancel = 50
Const Enter = 60
```

```
Waktu = 0
Pwm = 1

'Inisialisasi Timer 0
Config Timer0 = Timer , Gate = Internal , Mode = 1
'Timer0 = counter : timer0 dioperasikan sebagai counter
'Gate = Internal  : tanpa external gate control
'Mode = 1        : 16-bit

On Timer0 Timer_0_int
Load Timer0 , -1000                    'interupsi setiap 1000uS =1ms
Enable Interrupts                      'enable  interrupsi
Enable Timer0                          'enable  timer0

'Inisialisasi Timer 1
Config Timer1 = Timer , Gate = Internal , Mode = 2
'Timer0 = counter : timer0 dioperasikan sebagai counter
'Gate = Internal  : tanpa external gate control
'Mode = 2        : 8-bit auto reload (default)

On Timer1 Timer_1_int
Load Timer1 , 100                      'DATA PWM INTERVAL TIMER
Enable Interrupts                      'enable  interrupsi
Enable Timer1                          'enable  timer1

Upperline
Lcd "Nama:Suryo Adi W"
Lowerline
Lcd "NIM :0512201    "
Wait 3
Cls


Sensor_air:

Do

If P1.2 = 0 Then
  Goto Sensor_suhu

  Elseif P1.2 = 1 Then
  Cls
  Upperline
  Lcd "Air Tim Kurang"
  Lowerline
  Lcd "Tambah Air Lagi"
  Waitms 100
  Cls

End If

Loop Until P1.2 = 0


Sensor_suhu:
  Upperline
  Lcd "Air Cukup      "
  Lowerline
  Lcd "................"
Wait 1
```

```
'Menu Set Suhu Dari Keypad
Cls
Upperline
Lcd "Seting suhu  "
Lowerline
Lcd "Suhu:  C     "
Kursor = 6


Gosub Menu_keypad
Gosub Konversi_desimal
Seting_suhu = Hasil

Cls
Upperline
Lcd "Set Waktu Aduk  "
Lowerline
Lcd "Time:  Menit  "
Kursor = 6


Gosub Menu_keypad
Gosub Konversi_desimal
Seting_waktu = Hasil

Cls
Upperline
Lcd "Seting Selesai  "
Lowerline
Lcd "Loading....."
Wait 1

Heater = 0                              'heater ON
Cls
Upperline
Lcd "Start Proses...."
Lowerline
Lcd "Heater ON      "
Wait 1

Data_pwm = 16
Togle_bit = 0

Do
  If P1.2 = 1 Then Goto Sensor_air
  Gosub Baca_adc
  Upperline
  Lcd "Suhu: " ; Adc_suhu ; "       "
  Lowerline
  Lcd "Seting Suhu: "
  Lcd Seting_suhu ; "  "
  Lcd "    "
Loop Until Adc_suhu >= Seting_suhu
Heater = 1

Upperline
Lcd "Seting Suhu    "
Lowerline
Lcd "Telah tercapai  "
```

```
Wait 1

Upperline
Lcd "Motor Aduk ON   "
Lowerline
Lcd "----------"
Wait 1

Menit = 0
Detik = 0
Upperline
Lcd "Suhu:" ; Adc_suhu ; Chr(223) ; "C       "
Lowerline
Lcd "PWM:" ; Data_pwm ; "         "

Start Timer0                                'waktu dinyalakan
Do
  Start_adc = 1
  Waitms 1
  Start_adc = 0
  Adc_suhu = P2
  If Adc_suhu < Seting_suhu Then
    Heater = 0
  Else
  Heater = 1
  End If

  Upperline
  Lcd "Suhu:" ; Adc_suhu ; Chr(223) ; "C    "
  Lowerline

  Lcd "PWM:" ; Data_pwm ; " Waktu:" ; Menit
  Gosub Baca_keypad
  If Key = 1 Then
  Lowerline
      Temp = Data_pwm
     If Data_keypad = Up And Temp < 30 Then
      Temp = Temp + 1
      Data_pwm = Temp
     Elseif Data_keypad = Down And Temp > 5 Then
      Temp = Temp - 1
      Data_pwm = Temp
     End If
  End If

  Cpl Togle_bit
  If Togle_bit = True Then
    Temp = 31 - Data_pwm
    Pwm = 1
    Waitms Temp
  Else
    Pwm = 0
    Waitms Data_pwm
  End If
  If P1.2 = 1 Then Goto Sensor_air
Loop Until Menit = Seting_waktu
Heater = 1
Pwm = 1
Do
  Upperline
```

```
  Lcd "Proses Selesai !"
  Lowerline
  Lcd "              "
Loop

Konversi_desimal:
Tempo1 = 0
Tempo2 = 0

Cari:
If Tempo1 = Hasil Then
  Hasil = Tempo2
  Goto Keluar
End If

If Tempo1 = 9 Then
  mov acc,#h'10
  Goto Selesai
End If
If Tempo1 = 25 Then
  mov acc,#h'20
  Goto Selesai
End If
If Tempo1 = 41 Then
  mov acc,#h'30
  Goto Selesai
End If
If Tempo1 = 57 Then
  mov acc,#h'40
  Goto Selesai
End If
If Tempo1 = 73 Then
  mov acc,#h'50
  Goto Selesai
End If
If Tempo1 = 89 Then
  mov acc,#h'60
  Goto Selesai
End If
If Tempo1 = 105 Then
  mov acc,#h'70
  Goto Selesai
End If
If Tempo1 = 121 Then
  mov acc,#h'80
  Goto Selesai
End If
If Tempo1 = 137 Then
  mov acc,#h'90
  Goto Selesai
End If
If Tempo1 = 153 Then
  mov acc,#h'99
  Goto Selesai
Else
  add a,#1
End If
Selesai:
  Tempo1 = Acc
  Tempo2 = Tempo2 + 1
```

```
  Goto Cari
Keluar:
Return

Menu_keypad:
Locate 2 , Kursor
Cursor On Blink
Finish = 0
Do
  Ulang:
  Gosub Baca_keypad
  If Key = 1 Then
    If Data_keypad = Cor Or Data_keypad = Men Or Data_keypad = Up Or Data_keypad = Down
Then Goto Ulang
      If Data_keypad = Cancel Then

       If Kursor = 6 Then
         Locate 2 , Kursor
         Lcd " "                          'hapus karakter
         Locate 2 , Kursor
         Cursor On Blink
         Goto Ulang
       Elseif Kursor = 7 Then
         Locate 2 , 6
         Lcd " "                          'hapus karakter
         Locate 2 , 6
         Cursor On Blink
         Kursor = 6
         Goto Ulang
       Elseif Kursor = 8 Then
         Locate 2 , 7
         Lcd " "                          'hapus karakter
         Locate 2 , 7
         Cursor On Blink
         Kursor = 7
         Goto Ulang
       End If
      End If
      If Data_keypad = Enter Then
        If Kursor = 6 Then
        Goto Ulang
        Else
        Cursor Off Noblink
        If Kursor = 7 Then
          Lsb = Msb
          Msb = 0
        End If

        Gosub Konversi_ke_heksa

        Finish = 1
        End If
      End If

      If Kursor = 6 Then
        Locate 2 , Kursor
        Lcd "" ; Data_keypad
        Msb = Data_keypad
        Kursor = Kursor + 1
        Cursor Off Noblink
```

```
      Goto Ulang;
    Elseif Kursor = 7 Then
      Locate 2 , Kursor
      Lcd "" ; Data_keypad
      Lsb = Data_keypad
      Kursor = Kursor + 1
      Cursor Off Noblink
      Goto Ulang;

    Elseif Kursor = 8 Then
      Goto Ulang
    End If
  End If

Loop Until Finish = 1
Return

Konversi_ke_heksa:
  Acc = Msb
  anl a,#h'0f
  Rotate Acc , Left , 4
  Msb = Acc                          'baca nilai MSB

  Acc = Lsb
  anl a,#h'0f                        'baca nilai lsb
  Lsb = Acc
  Acc = Acc Or Msb                   'konversi ke heksa
  Hasil = Acc
  Return


'Rotine interupsi timer 0 pada vektor address
Timer_0_int:
  Stop Timer0
  Load Timer0 , -1000                'reload timer 1000uS =1ms
  Waktu = Waktu + 1
  If Waktu = 200 Then
    cpl p0.0
    Waktu = 0
    If Detik = 59 Then
      Menit = Menit + 1
      Detik = 0
    End If
    Detik = Detik + 1
  End If
  Start Timer0
Return

Timer_1_int:
  Stop Timer1
    push acc
    Cpl Togle_bit
  If Togle_bit = True Then
    Acc = Data_pwm
    cpl  a
    Th1 = Acc
    Tl1 = Acc
    Pwm = 1
  Else
    Acc = Data_pwm
```

```
    Th1 = Acc
    Tl1 = Acc
    Pwm = 0
  End If
  Start Timer1
  pop acc
Return

Baca_adc:
  Start_adc = 1
  Waitms 0.25
  Start_adc = 0
  Waitms 1
  If Start_adc = 0 Then Adc_suhu = P2
  Return

Baca_keypad:
  Key = 0
  mov p3,#h'7f              'scan baris 1
  If Kolom1 = 0 Then
  Data_keypad = 1
  Key = 1
  Goto Tahan
  End If

  If Kolom2 = 0 Then
  Data_keypad = 2
  Key = 1
  Goto Tahan
  End If

  If Kolom3 = 0 Then
  Data_keypad = 3
  Key = 1
  Goto Tahan
  End If

  If Kolom4 = 0 Then                    'tombol COR
  Data_keypad = Cor
  Key = 1
  Goto Tahan
  End If

  mov p3,#h'bf                          'scan baris 2
  If Kolom1 = 0 Then
  Data_keypad = 4
  Key = 1
  Goto Tahan
  End If

  If Kolom2 = 0 Then
  Data_keypad = 5
  Key = 1
  Goto Tahan
  End If

  If Kolom3 = 0 Then
  Data_keypad = 6
  Key = 1
  Goto Tahan
```

```
End If

If Kolom4 = 0 Then                    'tombol MEN
Data_keypad = Men
Key = 1
Goto Tahan
End If

mov p3,#h'df                  'scan baris 3
If Kolom1 = 0 Then
Data_keypad = 7
Key = 1
Goto Tahan
End If

If Kolom2 = 0 Then
Data_keypad = 8
Key = 1
Goto Tahan
End If

If Kolom3 = 0 Then
Data_keypad = 9
Key = 1
Goto Tahan
End If

If Kolom4 = 0 Then                    'tombol up
Data_keypad = Up
Key = 1
Goto Tahan
End If

mov p3,#h'ef                  'scan baris 4
If Kolom1 = 0 Then
Data_keypad = Cancel
Key = 1
Goto Tahan
End If

If Kolom2 = 0 Then
Data_keypad = 0
Key = 1
Goto Tahan
End If

If Kolom3 = 0 Then
Data_keypad = Enter                   'TOMBOL ENT
Key = 1
Goto Tahan
End If

If Kolom4 = 0 Then                    'tombol down
Data_keypad = Down
Key = 1
Goto Tahan
End If

Tahan:
```

```
  Do
  Loop Until Kolom1 = 1
  Do
  Loop Until Kolom2 = 1
  Do
  Loop Until Kolom3 = 1
  Do
  Loop Until Kolom4 = 1

  Return
End
```