SKRIPSI

PERANCANGAN DAN PEMBUATAN PENGENDALI GOKART ELEKTRIK MENGGUNAKAN SISTEM PWM BERBASIS MIKROKONTROLER

Disusun Oleh :

Heldin Rambo Siagian

04.12.246

JURUSAN TEKNIK ELEKTRO S-1

KONSENTRASI TEKNIK ELEKTRONIKA

FAKULTAS TEKNOLOGI INDUSTRI

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LEMBAR PERSETUJUAN

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SKRIPSI

Disusun dan Diajukan sebagai Salah Satu Syarat Untuk Memperoleh

Gelar Sarjana Teknik Elektro Strata Satu (S–1)

Disusun Oleh :

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Judul Skripsi : **PERANCANGAN DAN PEMBUATAN PENGENDALI GOKART ELEKTRIK MENGGUNAKAN SISTEM PWM BERBASIS MIKROKONTROLER**

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Tanggal : 20 Februari 2010

Dengan Nilai : 77,7 (B+)

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ABSTRAKSI

" PERANCANGAN DAN PEMBUATAN PENGENDALI GOKART ELEKTRIK MENGGUNAKAN SISTEM PWM BERBASISKAN MIKROKONTROLER"

HELDIN RAMBO SIAGIAN
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Gokart merupakan kendaraan permainan yang banyak dijumpai di pusat bermain anak-anak. Selain untuk melatih keberanian dan kecekatan anak, gokart juga dapat melatih hobi anak dalam berkendara khususnya kendaraan roda 4. Gokart sebenarnya menggunakan mesin dan daya yang dihasilkan besar, namun ada juga mesin yang berdaya kecil dilihat dari besar mesin atau biasa sering disebut 110cc, 70cc, dan 50cc. Penulis ingin membuat Gokart dengan menggunakan motor dc yang berdaya rendah dan memiliki pemindah gear untuk mengatur akselerasi/percepatan. Gokart ini untuk anak-anak yang ingin mengendarai permainan gokart dengan kecepatan yang rendah dan ramah lingkungan karna tidak menggunakan mesin. Metode, hasil pengujian adalah kecepatan gokart dapat diatur melalui sensor pengatur kecepatan dan pemindah gear dapat diatur melalui tombol *up* dan *down*.

Untuk pengontrolan kecepatan pada saat pedal gas (sensor pengatur kecepatan) di injak maksimum maka motor dc gear box berputar 578 RPM dan roda berputar 311 RPM. Untuk pengontrolan pemindah gear pada saat mencari posisi gear (gear 1, gear 2, sampai dengan gear 6) data ADC 0808 didapat dengan coba – coba atau *trail and error* dan data ADC dapat dilihat pada LCD.

Kata kunci : Gokart, Mikrokontroler AT 89S51, PWM, Motor DC

KATA PENGANTAR

Puji Syukur Kepada Tuhan Yesus Kristus yang telah memberikan berkat-Nya, sehingga dapat menyelesaikan skripsi yang berjudul "Perancangan dan Pembuatan Pengendali Gokart Elektrik Menggunakan Sistem PWM Berbasis Mikrokontroler" ini dengan lancar. Skripsi ini merupakan persyaratan kelulusan Studi di Jurusan Teknik Elektro S-1 Konsentrasi Teknik Elektronika ITN Malang dan untuk mencapai gelar Sarjana Teknik.

Keberhasilan peyelesaian laporan skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terima kasih kepada :

1. Bapak Prof. Dr. Eng. Ir. Abraham Lomi, MSEE selaku Rektor Insitut Teknologi Nasional Malang
2. Bapak Ir. Sidik Noertjahjono, MT selaku Dekan Fakultas Teknologi Industri ITN Malang
3. Bapak Ir. F. Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro S-1 dan sekaligus menjadi Dosen Pembimbing
4. Ayah dan Ibu serta saudara-saudara kami yang telah memberikan do'a restu, dorongan, semangat, dan biaya
5. Seluruh rekan Mahasiswa yang telah membantu dalam penyelesaian penulisan skripsi ini

Penyusun telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam menyelasaikan laporan ini. Untuk itu penyusun mengharapkan saran dan kritik yang membangun dari pembaca demi kesempurnaan laporan ini.

Harapan penyusun semoga laporan skripsi ini dapat memberikan manfaat bagi pengembangan pengetahuan pembaca.

Malang, Februari 2010

Penyusun

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BAB I

PENDAHULUAN

1.1 Latar Belakang

Kemajuan teknologi dibidang elektronika dewasa ini berkembang dengan cepat dan berpengaruh dalam pembuatan alat-alat canggih, yaitu alat yang dapat bekerja secara otomatis dan memiliki ketelitian tinggi dengan bantuan mikrokontroler. Pengunaan sebagai unit-unit kendali sudahlah sangat luas. Hal ini dikarenakan peralatan-peralatan yang dikontrol secara elektronik lebih banyak memberi kemudahan-kemudahan dalam pengunaannya, seperti dapat melakukan pengontrolan secara otomatis.

Gokart sebenarnya menggunakan mesin dan daya yang dihasilkan besar, namun ada juga mesin yang berdaya kecil dilihat dari besar mesin atau biasa sering disebut 110cc, 70cc, dan 50cc. Penulis ingin membuat Gokart dengan menggunakan motor dc yang berdaya rendah dan memiliki pemindah gear untuk mengatur akselerasi/percepatan. Gokart ini untuk anak-anak yang ingin mengendarai permainan gokart dengan kecepatan yang rendah dan ramah lingkungan karna tidak menggunakan mesin.

Dalam hal ini, akan membahas mengenai pengendali Gokart Elektrik menggunakan sistem PWM (Pulse Widh Modulation) berbasis mikrokontroler AT89S51, mesin Gokart tidak mempunyai tranmisi atau perpindahan gear, sehingga memiliki kelemahan pada akselerasi atau percepatan. Penulis membuat suatu alat

untuk menggerakkan atau menjalankan Gokart menggunakan Motor DC dengan sistem PWM serta menggunakan gear level (perpindahan gear) berbasis mikrokontroler AT89S51.

1.2 Rumusan Masalah

Dalam perancangan dan pembuatan pengendali Gokart elektrik ini, dapat dirumuskan permasalahannya sebagai berikut:

1. Bagaimana mengontrol kecepatan motor DC
2. Bagaimana cara kerja mengontrol perpindahan gear (Derailleur).

1.3 Tujuan

Tujuan yang ingin dicapai oleh penulis dari pembuatan dan penyusunan Skripsi ini adalah:

Merancang dan membuat Pengendali Gokart Elektrik menggunakan sistem PWM berbasis Mikrokontroler.

1.4 Batasan Masalah

Dalam menyusun skripsi ini diperlukan suatu batasan masalah agar tidak menyimpang dari ruang lingkup yang akan dibahas. Adapun batasan masalahnya adalah sebagai berikut :

1. Alat yang dibuat berbasis mikrokontroler AT89S51.
2. Motor yang digunakan adalah Motor DC.

3. Catu daya 24 volt.
4. Tidak membahas desain gear box.

1.5 Metodologi

Metodologi yang dipakai dalam pembuatan skripsi ini adalah:

1. Studi Literatur dengan mencari referensi-referensi yang berhubungan dengan perencanaan dan pembuatan alat yang akan dibuat.
2. Field Research

   Dengan melakukan penelitian secara langsung mengenai objek-objek yang berhubungan langsung dengan perencanaan alat yang akan dibuat.
3. Design dan Pembuatan Alat

   Yaitu meliputi pembuatan PCB, perakitan komponen serta penyolderan dan pembuatan perangkat lunak.
4. Pengujian Alat

   Dengan melakukan pengujian perblok rangkaian dan kerja seluruh sistem pada alat tersebut.

1.6 Sistematika Penyusunan Laporan

Dalam penulisan tugas akhir ini sistematika penulisan skripsi disusun sebagai berikut :

BAB I PENDAHULUAN

Membahas tentang latar belakang, rumusan masalah, tujuan, batasan masalah, metodologi dan sistematika penulisan pada penulisan skripsi ini.

BAB II LANDASAN TEORI

Berisikan tentang penjelasan dan teori-teori yang berhubungan dengan komponen-komponen yang digunakan dalam perancangan alat.

BAB III PERENCANAAN DAN PEMBUATAN ALAT

Membahas tentang perancangan alat yang terdiri dari perancangan perangkat keras dan perancangan perangkat lunak.

BAB IV PENGUJIAN ALAT

Membahas tentang pengujian peralatan secara keseluruhan dan analisa hasil pengujian.

BAB V PENUTUP

Berisikan kesimpulan yang didapat selama perancangan dan pembuatan alat serta saran-saran.

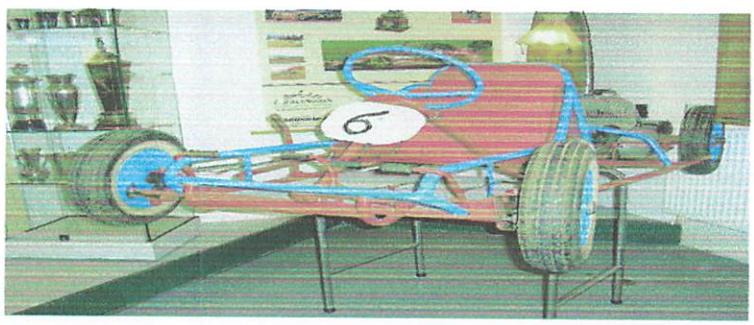
BAB II

LANDASAN TEORI

2.1 GOKART

Gokart adalah salah satu jenis olah raga otomotif beroda empat seperti halnya Formula, NASCAR, Speed Car, Rally, Offroad dan lain sebagainya. Namun, untuk bentuk fisik dari gokart mempunyai dimensi yang lebih kecil dan memiliki kapasitas daya mesin yang kecil pula sehingga untuk kebutuhan rangkaian mesin gokart, baik dari rangka, sistem penggerak sampai lintasan yang digunakan mempunyai dimensi yang lebih kecil pula.

Gokart pertama kali dirancang oleh Art Ingels pada tahun 1956 di California bagian selatan. Dia membuat gokart dari sisa potongan besi dan menggunakan mesin 2 langkah. Ketika itu dia adalah seorang perancang mobil balap di perusahaan Kurtis Kraft. Oleh karena itu dia dijuluki sebagai Father of Karting oleh para penggemar gokart sampai saat ini. Gambar 2.1 menunjukkan Gokart pertama dibuat di Swedia.



Gambar 2.1 Speedcar 1960 , pendahulu untuk karting di Swedia[4]

Gokart secara garis besar terdiri atas beberapa komponen, yang dapat dijabarkan sebagai berikut :

A. Rangka

Rangka gokart terbuat dari tabung baja. Tidak ada suspensi Oleh karena itu rangka harus cukup fleksibel untuk bekerja sebagai suspensi dan cukup kaku untuk tidak pecah atau memberi jalan pada tikungan. rangka Kart diklasifikasikan di Amerika Serikat sebagai 'Open', 'Caged', 'Straight' atau 'Offset'. Semua rangka yang disetujui oleh CIK-FIA adalah 'Straight' dan 'Open'.

1. Open roll karts tidak memiliki kandang.
2. Caged karts memiliki kandang gulung mengelilingi pengemudi yang sebagian besar digunakan pada trek tanah.
3. Dalam rangka Traight sopir duduk di tengah. chassis straight digunakan untuk balap sprint.
4. Dalam rangka Offset pengemudi duduk di sisi kiri. Rangka offset digunakan untuk balapan hanya berberbelok kiri *speedway racing*.

Kekakuan dari rangka memungkinkan karakteristik penanganan yang berbeda untuk situasi yang berbeda. Biasanya, untuk kondisi kering rangka lebih keras lebih baik, sedangkan di basah atau kondisi licin (traksi minimum) lainnya, rangka yang lebih fleksibel dapat bekerja lebih baik. rangka terbaik memungkinkan

untuk batang penegak kaku ditambahkan atau dihilangkan di bagian belakang, depan dan samping sesuai dengan kondisi balapan.

Gokart untuk profesional biasanya memiliki berat 75-79 kg, lengkap tanpa sopir. Avanti, Tony Kart, Trulli, Birel, CRG, Gillard, Intrepid, Kosmic, Zanardi atau FA Kart adalah beberapa contoh terkenal dari sekian banyak produsen rangka Eropa berkualitas. Margay adalah perusahaan Amerika yang memproduksi rangka kart.

B. Mesin

Gokart Taman hiburan dapat ditenagai oleh mesin 4-langkah atau motor listrik, sedangkan gokart balap menggunakan mesin 2-langkah kecil atau 4-langkah.

1. Gokart listrik berbiaya pemeliharaan rendah, hanya membutuhkan baterai timbal-asam dari mobil yang dipasang setelah disii dayanya. Karena mesin jenis ini bebas polusi dan tidak mengeluarkan asap, sirkuitnya dapat diletakan dalam ruangan tertutup. Sebuah gokart listrik yang dayanya terisi penuh dapat menjalankan lebih dari 20 menit sebelum turun kinerjanya.
2. Mesin gokart 2-langkah dikembangkan dan dibangun oleh produsen yang khusus memproduksi mesin jenis ini. Comer, IAME (Parilla, Komet), TM, Vortex, Titan, REFO, Yamaha dan Rotax adalah produsen2 mesin jenis ini. Mesin ini berdaya sekitar 8 tenaga kuda

untuk mesin satu-silinder 60 cc (MiniROK buatan Vortex) hingga 90 tenaga kuda untuk 250 cc dua silinder. Saat ini, kategori yang paling populer di seluruh dunia adalah unit Touch-dan-go (TAG) 125 cc . mesin Kf1 125 cc baru-baru ini dibatasi secara elektronik pada putaran mesin 16.000 rpm. Saat ini kebanyakan mesin adalah berpendingin air, namun sebelumnya mesin berpendingin udara yang mendominasi olahraga ini.

3. Mesin 4-langkah berpendingin udara berbasis mesin standar industri , kadang-kadang dengan sedikit modifikasi, berdaya dari sekitar 5-20 hp. Briggs & Stratton, Tecumseh, Kohler, Robin, dan Honda adalah produsen2 mesin jenis ini. Mesin-mesin produksi mereka memadai untuk balap dan menyenangkan dalam aplikasinya ke gokart. Ada juga mesin 4 langkah lebih kuat yang tersedia dari produsen seperti Yamaha, TKM, Biland atau Aixro (Wankel engine) , berdaya dari 15 tk hingga 48 tk. Mesin ini mampu mencapai putaran mesin sekitar 11.000 rpm dan dibuat khusus untuk karting. Mereka digunakan dalam beberapa kelas Kejuaraan Nasional seperti mesin dua langkah.

C. Transmisi

Gokart tidak memiliki diferential. Tidak adanya diferential berarti bahwa salah satu ban belakang harus tergelincir saat menikung, hal ini bisa dicapai dengan

merancang rangka sehingga dapat mengangkat sedikit ban belakang bagian dalam ketika kart menikung . Hal ini memungkinkan ban kehilangan sebagian dari cengkeraman dan tergelincir atau mengangkat dari tanah sepenuhnya.

Daya disalurkan dari mesin ke as roda belakang melalui rantai (beberapa penyewaan menggunakan sabuk). Baik puli mesin dan poros bisa dilepaskan, rasio mereka bisa disesuaikan sesuai dengan konfigurasi sirkuit untuk mendapatkan hasil maksimal.

Pada awal perkembangan gokart, daya akan langsung diteruskan ke roda, tapi untuk menutup beberapa ketidaknyamanan maka segera digunakan kopling sentrifugal. Kopling sentrifugal kering kini digunakan dalam banyak kategori (Rotax Max adalah salah satu contoh) dan telah menjadi sesuatu yang jamak ketika bagian kelas atas internasional harus beralih ke mesin 125 cc berkopling pada Januari 2007.

D. Ban

Roda dan ban yang digunakan jauh lebih kecil daripada yang digunakan pada mobil normal. Pelek terbuat dari magnesium alloy atau aluminium. Ban dapat mendukung kekuatan menikung melebihi dari 2 G (20 m / s ^{2}), tergantung pada rangka, mesin, dan setelan motor.

Serupa dengan olahraga motor lainnya, ban gokart memiliki jenis yang berbeda-beda untuk digunakan sesuai dengan kondisi lintasan:

1) Ban Mulus / Slick, untuk cuaca kering. Di tingkat internasional ban ini ada yang paling lembut dan ada yang paling keras. Beberapa produsen ban mobil seperti Bridgestone, Dunlop atau Maxxis, membuat ban untuk gokarts. Ada juga produsen ban gokart spesifik, yang meliputi MG, MOJO, dan Vega. Ban Slick gokart terdiri dari berbagai senyawa, dari yang sangat lembut (maksimum grip) yang sangat keras (gokart hiburan dan gokart sewaan, cengkeraman kurang tapi lebih awet).

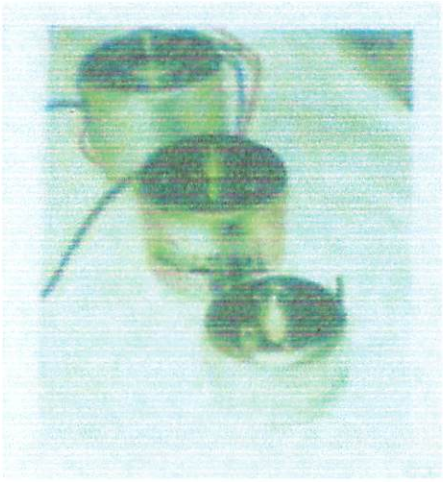
2) Ban Hujan atau "ban basah", untuk keadaan basah. Mereka beralur, terbuat dari senyawa lembut, dan lebih langsing daripada ban slicks. Tidak semua kelas balap memungkinkan ban hujan.

3) Ban Khusus, seperti ban berduri untuk kondisi es, atau "ban potong" bercengkeraman tinggi untuk kondisi sirkuit tanah liat. "ban potong" adalah ban slicks yang dimodifikasi menggunakan mesin bubut untuk mengoptimalkan cengkraman

2.2 MOTOR DC

Motor arus searah (DC) adalah suatu mesin yang berfungsi mengubah tenaga listrik arus searah menjadi tenaga mekanik dimana tenaga gerak berupa putaran rotor.

Dalam kehidupan sehari - hari metor arus searah sering dijumpai, sebagai contoh adalah motor yang dipasang untuk starter mobil, mainan anak, pada tape recorder dan lain – lain. Sedangkan pada industri, motor DC dapat dijumpai pada elevator, conveyor dan lain – lain. Gambar 2.2 menunjukkan Bentuk fisik Motor DC berbagai ukuran.

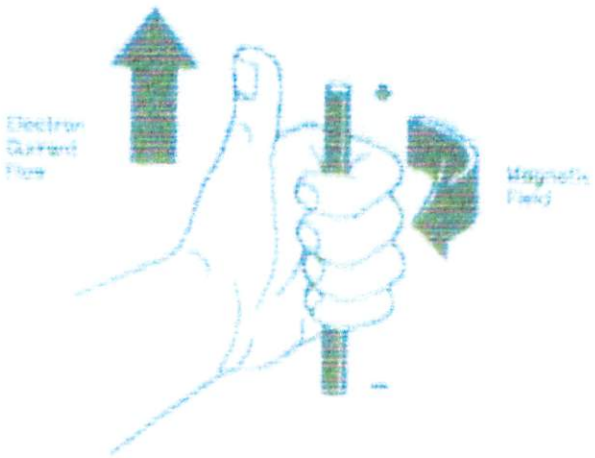


Gambar 2.2 Bentuk fisik Motor DC Berbagai Ukurun[9]

2.2.1 Prinsip Dasar Motor Arus Searah

Prinsip dasar motor arus searah adalah kalau sebuah kawat berarus diletakkan antara kutub magnet (U.S), maka pada kawat tersebut akan bekerja suatu gaya yang akan menggerakkan kawat tersebut. Arah gerak dari kawat tersebut dapat ditentukan dengan "kaidah tangan kiri" yang berbunyi sebagai berikut: "apabila tangan kiri dibiarkan terbuka dan diletakkan diantara kutub utara dan kutub selatan, sehingga garis – garis gaya yang keluar dari kutub utara menembus telapak tangan kiri dan arus didalam kawat mengalir searah dengan keempat jari, maka kawat

tersebut akan mendapat gaya yang jatuhnya sesuai dengan arah ibu jari". Gambar 2.3 menunjukkan kaidah tangan kiri.



Gambar 2.3 Kaidah Tangan Kiri[9]

Adapun besarnya gaya yang bekerja pada kawat tersebut dapat dirumuskan:

$$F = B . I . L$$

Keterangan:

F = Gaya Lorenz (Newton)

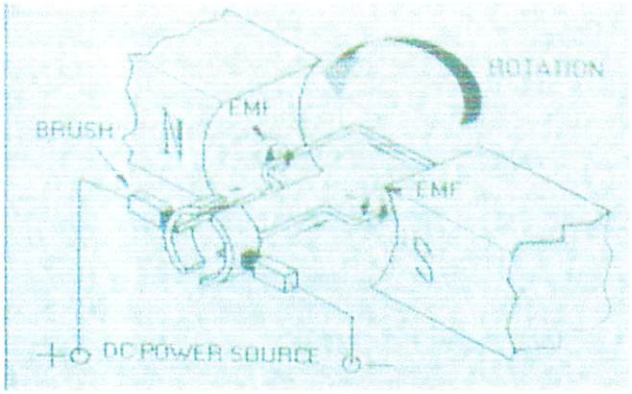
B = Kerapatan flux magnet (weber/m^2)

I = Arus listrik (ampere)

L = Panjang penghantar (meter)

Jika sebuah lilitan terletak dalam magnet yang homogen, maka kedua sisi belitan tersebut mempunyai arus yang daerahnya berlawanan.

Pada motor arus searah (DC) kumparan pada rotornya tidak satu, tapi terdiri dari kumparan dan komutator yang banyak dengan maksud untuk mendapatkan torsi yang kuat dan terus menerus. Gambar 2.4 menunjukkan kontruksi dasar motor dc.



Gambar 2.4 Kontruksi Dasar Motor DC[9]

2.2.2 Jenis – jenis Motor DC

Berdasarkan sumber arus penguat magnetnya, motor DC dibedakan menjadi dua, yaitu:

1. Motor arus searah penguatan terpisah (jika arus penguat magnet diperoleh dari sumberarus searah diluar motor tersebut).
2. Motor arus searah dengan penguat sendiri (jika arus penguat magnet diperoleh dari motor itu sendiri).

Berdasarkan hubungan lilitan penguat magnet tehadap lilitan jangkar, motor arus searah dibedakan menjadi:

1. Motor Shunt

Motor ini mempunyai kecepatan hampir konstan, motor ini punya putaran yang hampis konstan walaupun terjadi perubahan beban.

2. Motor Seri

   Merupakan arus searah yang mempunyai kecepatan putar yang tidak konstan, jika beban tinggi maka putaran akan melambat dan sebaliknya jika putaran rendah maka putaran akan cepat.

3. Motor Kompon

   Motor ini mempunyai sifat seperti motor seri dan shunt, tergantung lilitan mana yang kuat (kumparan seri/shunt).

2.2.3 Cara Memutar Balik Arah Putaran Motor DC

Untuk membalik arah putaran motor DC, dapat dilakukan dengan 2 cara, yaitu:

1. Membalik arah arus jangkar, sedangkan arah arus penguat tetap.
2. Membalik arah arus penguat, sedangkan arah arus jangkar tetap.

Jika keduanya dibalik (arah arus jangkar dan arus penguat) maka arah putaran motor akan tetap (tidak membalik). Gambar 2.5 menunjukkan arah putaran motor dc.

Gambar 2.5 Arah Putaran Motor DC[9]

2.3 MIKROKONTROLER AT 89S51

Mikrokontroler AT 89S51 Adalah merupakan pengembangan dari mikrokontroler standar MCS-51 juga berlaku untuk mikrokontroler ini. AT 89S51 merupakan memori nonvolatile yang bisa diisi ulang dan dihapus berulangkali. Memori ini digunakan untuk menyimpan intruksi-intruksi standard MCS-51 sehingga tidak memerlukan eksternal memori untuk menyimpan source code, karena bekerja dalam mode Single Chip Operation (Mode Operasi Keping Tunggal).

2.3.1 Arsitektur Mikrokontroler AT 89S51

- Central Processing Unit (CPU)

  CPU mempunyai kemampuan mengeksekusi instruksi, memanipulasi data, melakukan fungsi aritmatika dan logika (ALU). CPU juga melakukan pengendalian dan pengaturan seluruh aktivitas mesin.

- Bus Alamat

  Bus alamat berfungsi sebagai sejumlah lintasan saluran pengalamatan antara alat dengan sebuah komputer. Pengalamatan ini harus ditentukan terlebih dahulu untuk menghindari terjadinya kesalahan pengiriman sebuah intruksi serta menghindari terjadinya bentrok antara dua buah alat yang bekerja bersamaan.

- Bus Data

  Bus data merupakan sejumlah lintasan saluran keluar masuknya data dalam suatu mikrokontroler. Pada umumnya saluran data yang masuk sama dengan saluran data yang keluar.

- Memori

  Di dalam sebuah mikrokontroler terdapat suatu memori yang berfungsi untuk menyimpan data atau program. Ada beberapa jenis memori, antara lain RAM dan ROM. Ada beberapa tingkatan memori, diantaranya adalah register internal, memori utama, dn memori masal. Register internal adalah memori didalam ALU. Waktu akses register sangat cepat, umumnya kurang dari 100ns.

- RAM (Random Access Memory)

  RAM merupakan memori yang dapat dibaca dan ditulis. RAM biasanya digunakan untuk menyimpan data atau sering disebut dengan memori data saat bekerja. Data yang ada pada RAM akan hilang bila catu daya dari RAM dimatikan, Sehingga RAM hanya dapat digunakan untuk menyimpan data sementara.

- ROM (Read Only Memori)

  ROM merupakan memori yang hanya dapat dibaca. Data yang ada di dalam ROM tidak akan hilang meskipun tegangan catu daya dimatikan.

Dari sifat itu, maka ROM sering dipakai untuk menyimpan Program. ROM terdiri dari beberapa jenis, diantaranya ROM, PROM, EPROM, dan EEPROM.

- Clock

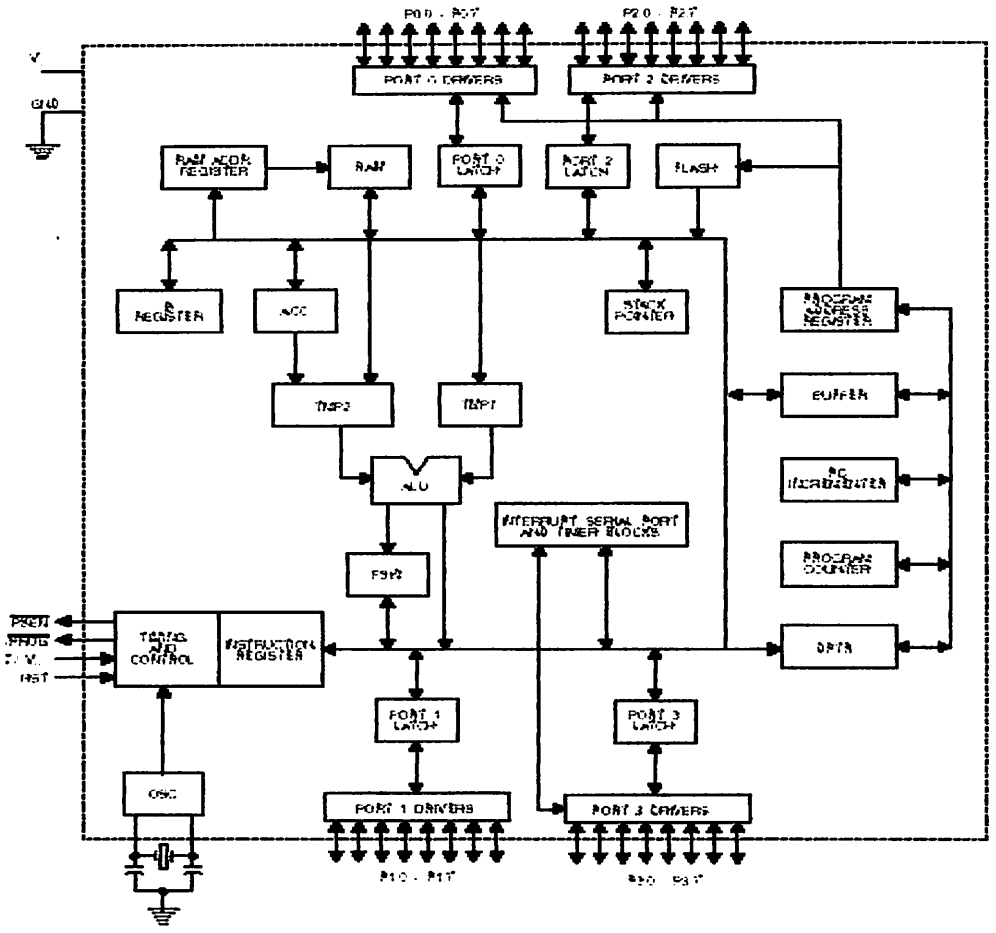
  Clock atau pewaktu berfungsi memberikan referensi waktu dan sinkronisasi antara elemen.

Mikrokontroler AT 89S51 adalah adalah keluarga dari MCS-51 dari Intel Corporation, berukuran kecil, berkecepatan tinggi dan dilengkapi dengan memori dalam chip, sehingga seolah-olah PC (Personal Computer) yang berdiri sendiri. Adapaun blok diagram dari Mikrokontroler AT 89S51 terlihat pada gambar 2.1.

AT 89S51 menyediakan berbagai fasilitas internal chip, seperti berikut :

1) 8-bit Central Prosessing Unit.
2) 256 bytes memori data internal.
3) 4K bytes of in-sistem programmable Flash memory.
4) Full Duplex serial port.
5) Dua buah counter 16 bit.
6) 32 jalur *I/0* (input /output).
7) Multiple mode.
8) On chip oscillator dan timer.
9) Memori data eksternal masing-masing 64 Kbytes

Gambar 2.6 menunjukkan blok diagram AT 89S51.

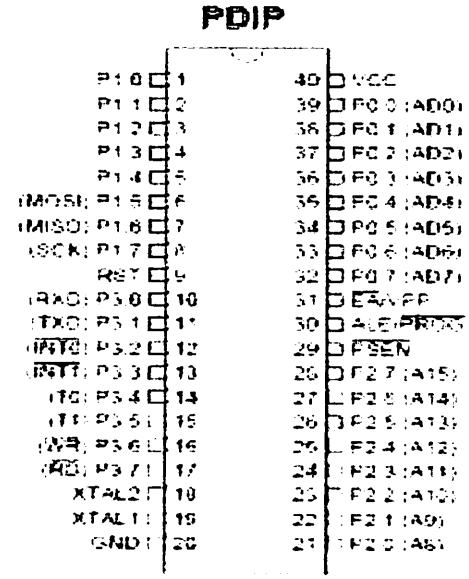


Gambar 2.6 Blok Diagram AT 89S51[2]

2.3.2 Susunan Pin AT 89S51

Mikrokontroler AT 89S51 mempunyai 40 kaki (pin) dimana 32 kaki diantaranya untuk keperluan port parallel. Satu port parallel terdiri dari 8 kaki, sehingga dari jumlah ini terbentuk 4 buah port parallel.

Gambar 2.7 menunjukkan susunan pin dari AT 89S51.



Gambar 2.7 Susunan Pin AT 89S51[2]

Keterangan:

1) Pin 40 (VCC). Merupakan pin catu daya dengan tegangan sebesar +5V (DC).
2) Pin 20 (GND). Merupakan pin ground yang terhubung dengan grounding rangkaian.
3) Pin 32 – 39 (port 0). Mempunyai fungsi sebagai port alamat data, maka jika mikrokontroler sedang mengakses alamat, P0 akan aktif sebagai pembawa alamat 8 bit yang (A0 – A8) dan ketika

mengakses data I/0, port ini berfungsi sebagai jalur data (D7 – D0).

4) Pin 1 – 8 (Port 1). Sebagai 8 bit I/0 Bidirectionnal yang dilengkapi dengan internal pull–up.
5) Pin 21 – 28 (Port 2). Berfungsi sebagai jalur alamat pembawa alamat 8 bit bagian atas yang dilengkapi dengan internal pull-up.
6) Pin 10 – 17 (Port 3), Port ini mempunyai fungsi alternative tiap pin seperti yang ditunjukan Pada table 2.1. dibawah ini:

Tabel 2.1 menunjukkan fungsi-fungsi alternatif port 3 pada AT 89S51

Pin	Nama	Fungsi
P3.0	RXD	Menerima (input) data untuk port serial
P3.1	TXD	Menerima (output) data untuk port serial
P3.2	INT.0	Interupsi luar 0
P3.3	INT.1	Interupsi luar 1
P3.4	T0	Masukan luar timer/counter 0
P3.5	T1	Masukan luar timer/counter 1
P3.6	WR	Kaki tulis memori data luar
P3.7	RD	Kaki baca memori data luar

Tabel 2.1. Fungsi-fungsi Alternatif Port 3 Pada AT 89S51[2]

7) Pin 30 ALE PROG (Addres Latch Enable/Programmable). Pin ini aktif high dengan mengeluarkan pulsa output untuk me-latch (mengunci/menahan) 1 byte alamat rendah selama mengakses ke alamat memori aksternal.

8) Pin 31 EA/VPP (External Access Enable). Pin ini harus ditahan pada kondisi rendah secara aksternal atau dihubungkan ke ground untuk mengakses eksternal memori dengan lokasi 0000H sampai FFFFH.

9) Pin 29 PSEN (Program Strobe Enable) merupakan sinyal baca untuk program memori eksternal.

10) Pin 9 (Reset). Pin ini aktif high '1' minimal dua kali siklus mesin bekerja (24 periode frekuensi clock) ditambah waktu Start On Osilator, maka akan me-reset peralatan.

11) Pin 19 XTAL1. Sebagai masukan kepenguat pembalik osilator dan masukan internal clock untuk operasi system.

12) Pin 18 XTAL2. Sebagai output dari penguat pembalik osilator.

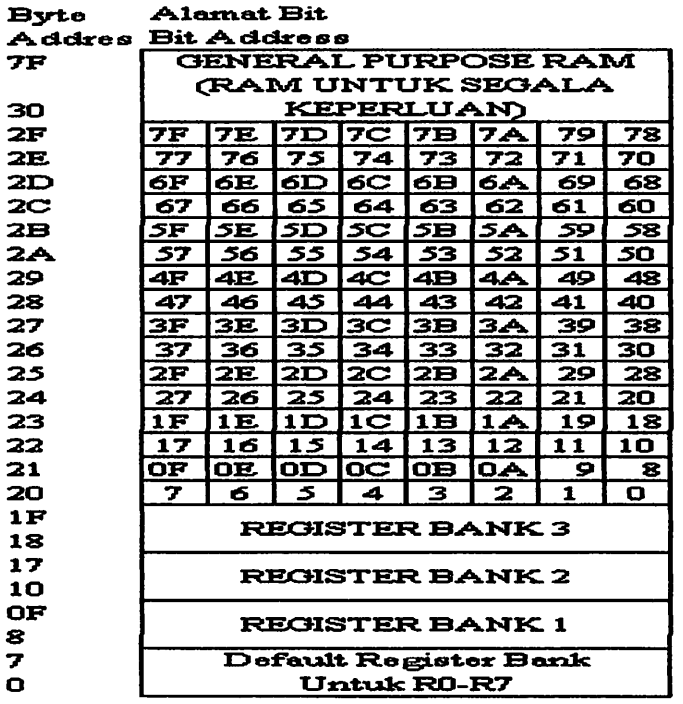
2.3.3 Organisasi Memori Mikrokontroler AT89S51

Organisasi memori mikrokontroler AT89S51 dapat dibagi menjadi 2 bagian yang berbeda, yaitu memori program dan memori data. Pembagian itu berdasarkan fungsinya dalam penyimpanan data atau program. Memori program

digunakan untuk instruksi yang akan dijalankan oleh mikrokontroler. Sedangkan memori data digunakan sebagai tempat penyimpanan data-data yang akan diakses oleh mikrokontroler.

Mikrokontroler AT89S51 memiliki program internal dan dapat menggunakan memori program *eksternal*. Memori program *eksternal* bisa berupa ROM/EPROM. Memori program internal sebesar 4 Kbyte EEPROM. Lebar jalur alamat yang dapat diakses adalah 16 bit mulai alamat 0000H sampai dengan FFFFH.

Gambar 2.8 menunjukkan Ram Mcs-51



Gambar 2.8 RAM MCS-51[2]

Mikrokontroler AT89S51 memiliki memori data berupa RAM internal sebesar 128 byte. Dari jumlah tersebut, 32 byte terendah dikelompokkan menjadi 4 bank. Tiap-tiap bank terdiri dari 8 register. Pemilihan bank dilakukan melalui register. Gambar 2.9 menunjukkan Spesial Function Register.

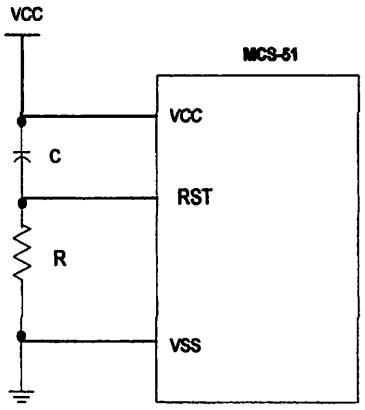
Byte Addres	Alamat Bit Bit Address								
FF									
F0	F7	F6	F5	F4	F3	F2	F1	F0	B
E0	E7	E6	E5	E4	E3	E2	E1	E0	Acc
D0	D7	D6	D5	D4	D3	D2	-	D0	PSW
B8	-	-	-	BC	BB	BA	B9	B8	IP
B0	B7	B6	B5	B4	B3	B2	B1	B0	P3
A8	AF	-	-	AC	AB	AA	A9	A8	IE
A0	A7	A6	A5	A4	A3	A2	A1	A0	P2
99	not bit adderssable								SBUF
98	9F	9E	9D	9C	9B	9A	99	98	SCON
90	97	96	95	94	93	92	91	90	P1
8D	not bit adderssable								TH1
8C	not bit adderssable								TH0
8B	not bit adderssable								TL1
8A	not bit adderssable								TL0
89	not bit adderssable								TMOD
88	8F	8E	8D	8C	8B	8A	89	88	TCON
87	not bit adderssable								PCON
83	not bit adderssable								DPH
82	not bit adderssable								DPL
81	not bit adderssable								SP
80	87	86	85	84	83	82	81	80	P0

Gambar 2.9 Spesial Function Register[2]

2.3.4 Reset

Rangkaian *Power On Reset* diperlukan untuk mereset mikrokontroler secara otomatis setiap catu daya dinyalakan. ketika catu daya diaktifkan, rangkaian

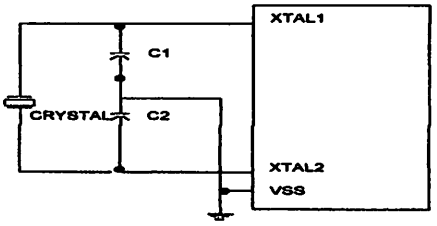
reset akan menahan logika tinggi pada penyemat RST dengan jangka waktu yang ditentukan oleh lamanya pengosongan muatan kapasitor. Untuk keabsahan reset, logika tinggi harus bertahan lebih lama dari dua siklus mesin ditambah waktu hidup *(start on)* oscilator. Gambar 2.10 menunjukkan Rangkaian Power On Reset.



Gambar 2.10 Rangkaian Power On Reset[2]

2.3.5 Pewaktuan

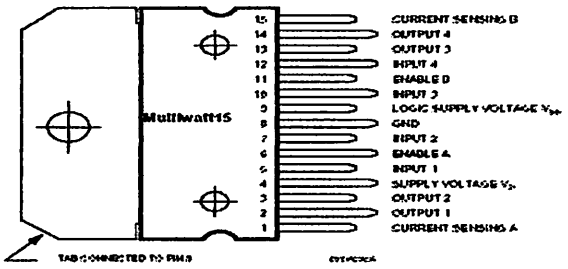
Mikrokontroler AT89S51 memiliki rangkaian osilator internal dengan mengacu referensi frekuensi pada penyemat XTAL1 dan XTAL2. Gambar 2.11 menunjukkan Rangkaian Pewaktuan dengan Osilator Internal.



Gambar 2.11 Rangkaian Pewaktuan dengan Osilator Internal[2]

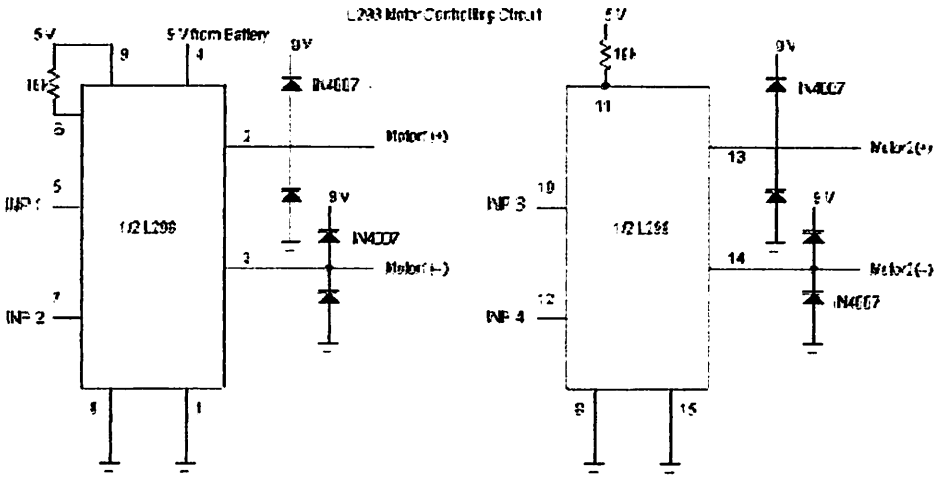
2.4 DRIVER MOTOR

Driver Motor yang digunakan adalah IC L 298 yang berfungsi memperkuat arus supaya motor dapat berputar dan dapat membalik fasa, motor dapat berputar dua arah. Driver Motor dengan IC L 298 untuk mengontrol perpindahan gear. Tegangan maksimum pada IC L 298 mencapai 46 volt dengan arus 4 A. Gambar 2.12 menunjukkan IC L298.



Gambar 2.12 IC L298[3]

Gambar 2.13 menunjukkan L 298 Motor Controlling Circuit.



Gambar 2.13 L 298 Motor Controlling Circuit[3]

Penjelasan masing-masing Pin L 298:

1) Pin 1. CURRENT SENSING A

Digunakan untuk mengontrol arus ke beban (motor A). Kita dapat terhubung ke GND melalui sebuah resistor dan VS / R akan dihubungkan kebeban. Jika tidak mengontrol arus, menghubungkannya ke GND secara langsung.

2) Pin 2. OUTPUT 1

Terhubung ke salah satu terminal (+) motor A, dan dioda terhubung ke pin ini (lihat di sirkuit untuk koneksi).

3) Pin 3. OUTPUT 2

Terhubung ke terminal (-) motor A. Hubungkan dioda seperti yang diberikan dalam rangkaian diagram.

4) Pin 4. SUPPLY VOLTAGE (VS)

Tegangan dapat dihasilkan sebesar 46V, batas tegangan terendah adalah 9V.

5) Pin 5. INPUT 1 TTL Compatible Inputs 1 to drive Motor A.

Harus logika tegangan (0V atau 5V). Menentukan apakah motor berjalan searah jarum jam atau berlawanan arah jarum jam.

6) Pin 6. ENABLE A TTL Compatible Enable Input for Motor A.

Untuk menjalankan motor, tegangan 5V dan untuk tidak menjalankan/ menghentikan motor, tegangan 0V.

7) Pin 7. INPUT 2 TTL Compatible Inputs 2 to drive Motor A..

Harus logika tegangan (0V atau 5V). Menentukan apakah motor berjalan searah jarum jam atau berlawanan arah jarum jam.

8) Pin 8. GND Ground

9) LOGIC SUPPLY VOLTAGE (VSS) 5-7 volts

10) INPUT 3 TTL Compatible Inputs 1 to drive Motor B.

Harus logika tegangan (0V atau 5V).

11) Pin 11. ENABLE B TTL Compatible Enable Input for Motor B.

Harus 5V untuk menjalankan motor dan 0 untuk tidak menjalankan / menghentikan motor.

12) Pin 12. INPUT 4 TTL Compatible Inputs 2 to drive Motor B.

Harus logika tegangan (0V atau 5V)

13) Pin 13. OUTPUT 3

Terhubung ke salah satu terminal (+) motor B, dan dioda terhubung ke pin ini (lihat di sirkuit untuk koneksi).

14) Pin 14. OUTPUT 4

Terhubung ke terminal (-) motor B. Hubungkan dioda seperti yang diberikan dalam rangkaian diagram.

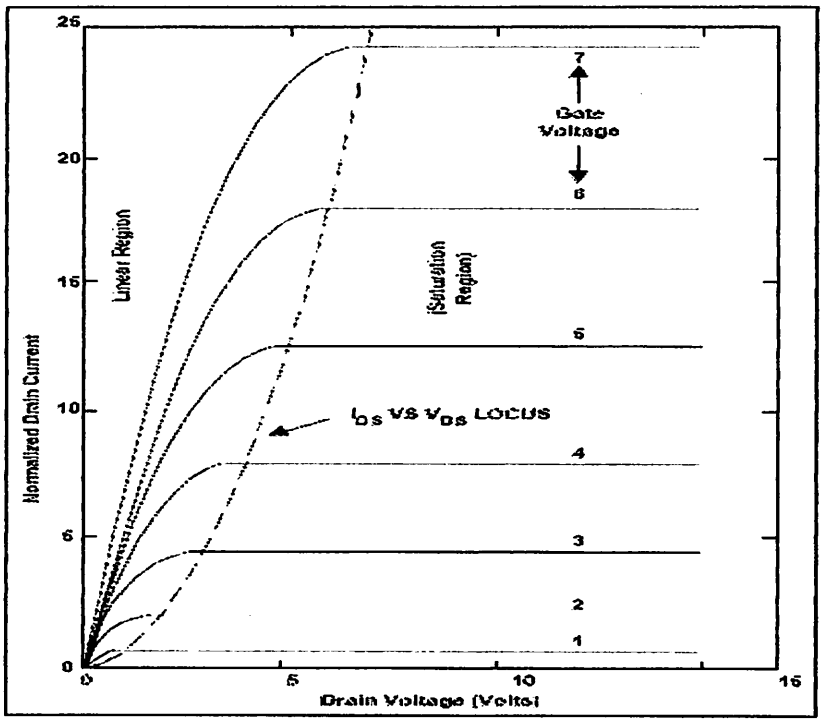
15) Pin 15. CURRENT SENSING B

Digunakan untuk mengontrol arus ke beban (motor B). Kita dapat terhubung ke GND melalui sebuah resistor dan VS / R akan dihubungkan kebeban. Jika tidak mengontrol arus, menghubungkannya ke GND secara langsung.

2.5 DRIVER MOTOR PWM

Driver Motor pwm yang digunakan adalah Mosfet IRFZ44N. Mosfet adalah Metal Oxide Semiconductor Field effect Transistor. Mosfet merupakan gabungan dari transistor dan dioda. Namun jika pada transistor, antara Basic dan Collector masih terdapat hubungan atau tidak terisolasi. Tetapi jika pada Mosfet, antara gate dan drain sudah terisolasi. Sehingga bila digunakan sebagai switch untuk arus dan tegangan yang besar, tetap aman dan tidak akan menimbulkan arus balik kerangkaian. Kelebihan dari Mosfet adalah hambatan dan source sangatlah kecil (hanya berorde milliohm). Mosfet dapat bertahan terhadap beberapa aplikasi dengan arus dan tegangan yang besar pada waktu bersamaan tanpa menimbulkan gangguan.

Mosfet dapat digunakan secara pararel dengan mudah, hal tersebut dikarenakan kenaikan forward voltage drop juga ikut menaikkan temperetur serta menjamin pembagian arus yang benardan merata kesemua komponen. Gambar 2.14 menunjukkan karakteristik arus-tegangan dari Mosfet.



Gambar 2.14 Current-Voltage Characteristic[10]

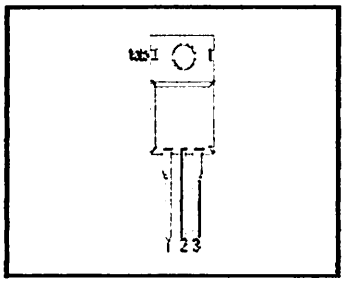
Mosfet yang akan dibahas adalah IRFZ44N. Besar dari R_{DS} adalah 17,5 m, kelebihan dari komponen ini adalah kecepatannya dalam switching.

Selain itu komponen ini dapat bekerja sampai dengan temperature tinggi. Jadi tidak perlu dikhawatirkan, jika bekerja terus-menerus dalam jangka waktu yang lama.

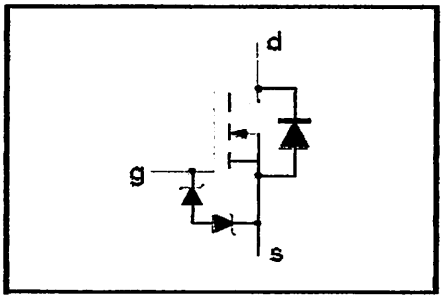
Gambar 2.15 s/d 2.17 menunjukkan Mosfet IRFZ44N.

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

Gambar 2.15 Pin Configuration IRFZ44N[10]



Gambar 2.16 Pinning IRFZ44N[10]



Gambar 2.17 Simbol IRFZ44N[10]

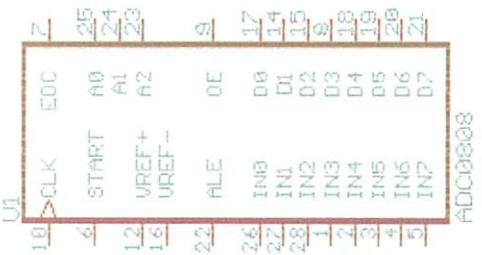
2.6 ADC 0808

ADC 0808 dikemas dalam IC monolitik dan merupakan ADC yang umum digunakan karena harganya yang relatif murah dan gampang dicari dipasaran. ADC ini menggunakan metode pengubah berturut-turut (Succesive Aproximation Register) dengan 8 saluran input analog dan dilengkapi beberapa kontrol logika yang sesuai dengan standart mikroprosesor.

ADC 0808 terdiri dari 3 bagian utama, yaitu :

1. MUX analog 8 Channels
2. Analog To Digital Converter (ADC)
3. Tri-state Lactch Buffer (penyangga terkunci 3 kanal)

Gambar 2.18 menunjukkan IC ADC 0808.

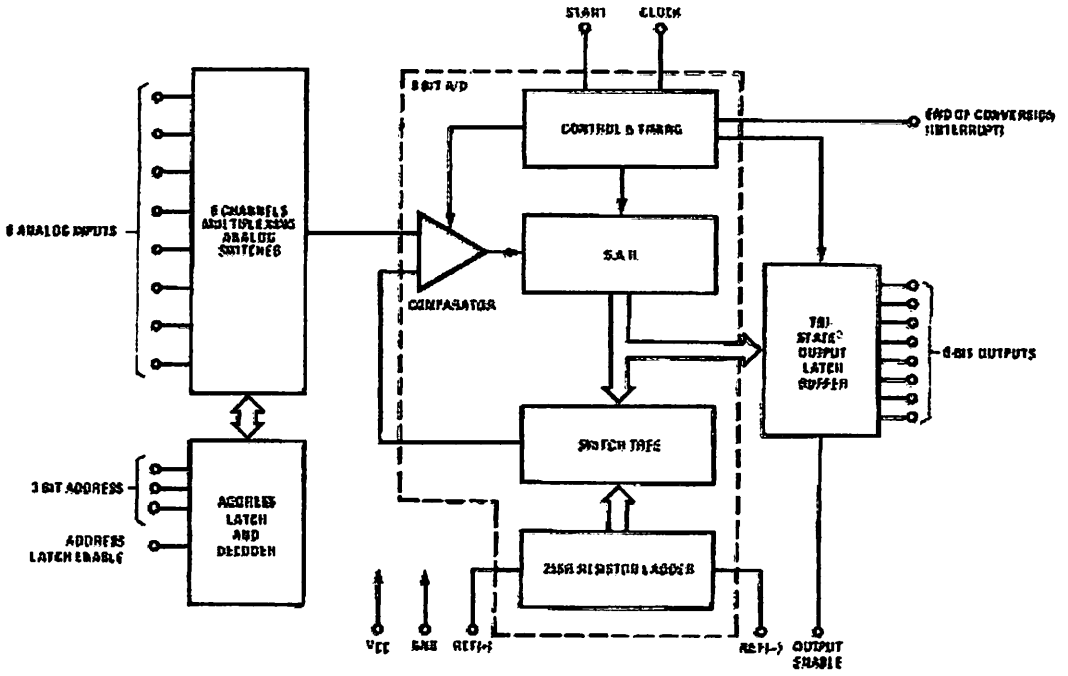


Gambar 2.18 IC ADC 0808[12]

Multiplexer analog 8 Channels berfungsi untuk mengolah 8 input data analog secara bergantian. Untuk memilih input mana yang dikehendaki pada output multiplexer disediakan 3 bit kontrol pemilih saluran input, yaitu ADD-A, ADD-B dan ADD-C dimana dalam perencanaan nantinya semua input ADC yang tersedia merupakan Succesive Aproximation Register 8 bit yang terdiri dari komparator, SAR dan Clock. Tri-state Latch Buffer berfungsi untuk menampung keluaran ADC 8 bit.

ADC ini mempunyai level tegangan terbatas untuk sinyal inputnya yang tergantung dari input referensi yang digunakan. Dalam hal ini yang membatasi adalah tegangan referensi positif Vref (+) dan tegangan referensi negatif Vref (-). Jika input referensi negatif diberi tegangan negatif dan input referensi positif diberi tegangan

positif sehingga besar tegangan input analog dapat berharga diantara kedua tegangan referensi tadi dan ini disebut bipolar, artinya kedua inputnya mempunyai polaritas positif dan negatif. Jika input referensi positif diberi tegangan positif dan referensi negatif diberi tegangan 0 volt (berharga positif saja) maka disebut unipolar. ADC yang dipakai dalam sistem ini dirancang untuk jenis unipolar. Blok diagram ADC dapat dilihat pada gambar 2-19 di bawah ini.

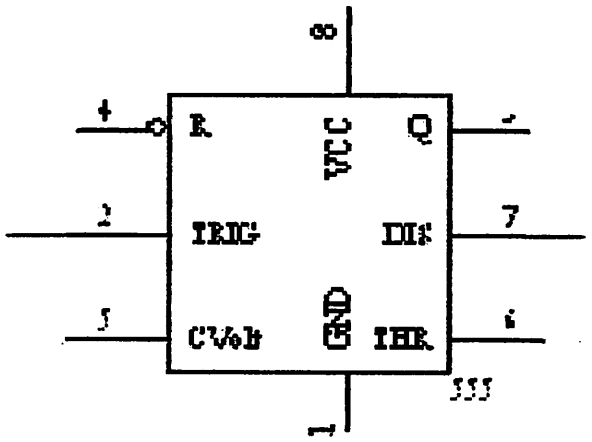


Gambar 2.19 Blok Diagram ADC 0808[12]

2.7 LM 555

IC ini digunakan untuk mengubah atau membangkitkan Frekuensi (Oscilator) bisa digunakan untuk menentukan waktu (Timer). Mempunyai tegangan sumber 200mA serta kompitable untuk dipakai bersama dengan mikrokontroller atau IC TTL. Mempunyai temperature kestabilan 0,005% per ° C, tingkat perhitungannya adalah sampai dengan microsecond.Berikut gambar susunan pin IC LM555:

Gambar 2.20 menunjukkan Konfigurasi Pin IC LM555.



Gambar 2.20 Konfigurasi Pin IC LM555[11]

IC 555 adalah salah satu rangkaian pewaktu terpadu yang diperkenlakan oleh signetic corporation serupa dengan op-amp. Pewaktu 555 dapat diandalkan, mudah dalam pengaplikasiannya.

Pewaktu 555 mempunyai 2 cara kerja, baik sebagai multivibrator astabil atau sebagai multivibrator monostabil. Untuk membangkitkan sinyal clock adalah

dengan cara trigger dan terminal threshold dihubungkan sehingga menjadi pemicuan sendiri. Ketika output timer 'high', membuat transistor discharge internal mati dan VC1 ditambah oleh fungsi exponensial dengan konstanta waktu (R1+R2)xC. Ketika VC1 atau tegangan threshold mencapai 2/3 VCC, output komparator pada terminal trigger menjadi high, dan mereset FF dan menyebabkan output menjadi Low. Dalam kondisi ini menyalakan transistor discharging dan C1 dilepas melalui chanel discharging dibentuk oleh R2 dan transistor disharge. Ketika VC1 turun dibawah VCC/3, output komparator pada terminal trigger menjadi high dan outputtimer menjadi high lagi. Transistor discharge mati dan VC1 naik lagi. Dalam proses tersebut, bagian dimana output timer high ini merupakan akibat dari VC1 bertambah dari VCC/3 ke 2/3 VCC, bagian dimanaoutput timer low ini merupakan akibat dari VC1 turun dari 2/3 VCC ke VCC/3. Pada operasi astabil rangkaian ini bekerja besar pada frekuensi yang ditentukan oleh nilai komponen Ra, Rb dan C. sedangkan frekuensinya dapat dihitung dengan persamaan berikut : *[National Semiconductor Corporation, www.national.com].*

Rumus frekuensi :

$$f = \frac{1}{(Ra + Rb).C}$$

BAB III

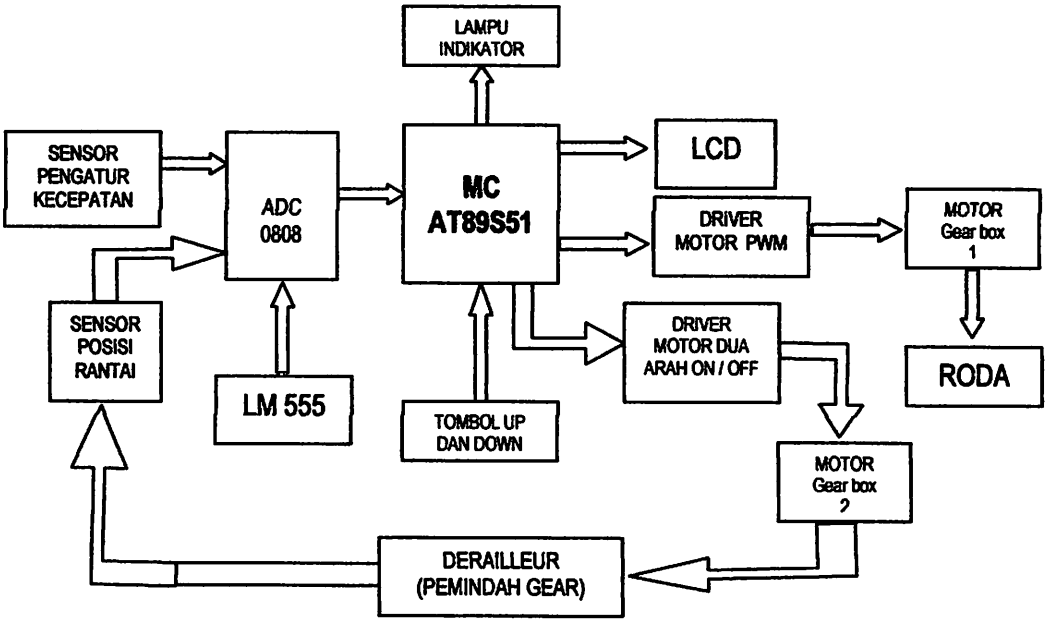
PERANCANGAN SISTEM

3.1 Pendahuluan

Bab ini akan membahas Perancangan dan Pembuatan Pengendali Gokart Elektrik Menggunakan Sistem PWM Berbasiskan Mikrokontroler. Meliputi perancangan perangkat keras (*Hardware*) dan perangkat lunak (*Software*) yang akan dijelaskan pada sub bab berikut ini.

3.2 Perancangan dan Pembuatan Perangkat Keras (Hardware)

Adapun blok diagram dari perencanaan dan pembuatan alat Pengendali Gokart Elektrik Menggunakan Sistem PWM Berbasiskan Mikrokontroler blok diagramnya seperti diperlihatkan pada gambar 3.1.



Gambar 3.1 Blok Diagram Sistem Pengendali Gokart

Fungsi masing-masing blok diagram diatas adalah sebagai berikut :

- **Sensor Pengatur Kecepatan (Potensiometer)** berfungsi memberikan perintah kepada mikrokontroler agar motor gear box 1 dapat mempercepat dan memperlambat kecepatan.
- **ADC 0808** berfungsi merubah dari analog Sensor Pengatur Kecepatan (Potensiometer) menjadi digital dan merubah dari analog sensor posisi rantai (potensiometer) menjadi digital.
- **LM 555** berfungsi memberikan clock pada ADC 0808 agar konversi analog to digital dapat terjadi.
- **Mikrokontroler AT89S51** berfungsi sebagai masukan *(input)* dari ADC 0808 dan mengeluarkan *(output)* untuk mengendalikan unit driver motor pwm mengendalikan unit driver motor dua arah on/off mengendalikan indikator kecepatan dan mengendalikan tombol tranmisi up dan down.
- **LCD** berfungsi sebagai tampilan yang dikeluarkan oleh mikrokontroler AT 89S51.
- **Driver Motor PWM** berfungsi untuk penguatan untuk motor gear box 1 yang terhubung ke roda.
- **Driver Motor Dua Arah ON/OFF** berfungsi penguatan motor gear box 2 yang terhubung pada pemindah gear.
- **Sensor Posisi Rantai (Potensiometer)** berfungsi sebagai penunjuk posisi rantai pada saat berpindah dari gear 1, ke gear 2, ke gear 3, ke gear 4, dan gear 5.

- **Tombol Up dan Down** berfungsi mengatur berpindahnya rantai pada gear level. Tombol Up untuk menaikkan rantai pada gear level dan Tombol Down untuk menurunkan rantai pada gear level.
- **Lampu Indikator** berfungsi untuk memberitahukan posisi rantai pada gear level.

3.2.1 Prinsip Kerja Alat

Secara ringkas dapat dijelaskan prinsip kerja alat Pengendali Gokart Elektrik Menggunakan Sistem PWM Berbasiskan Mikrokontroler adalah sebagai berikut :

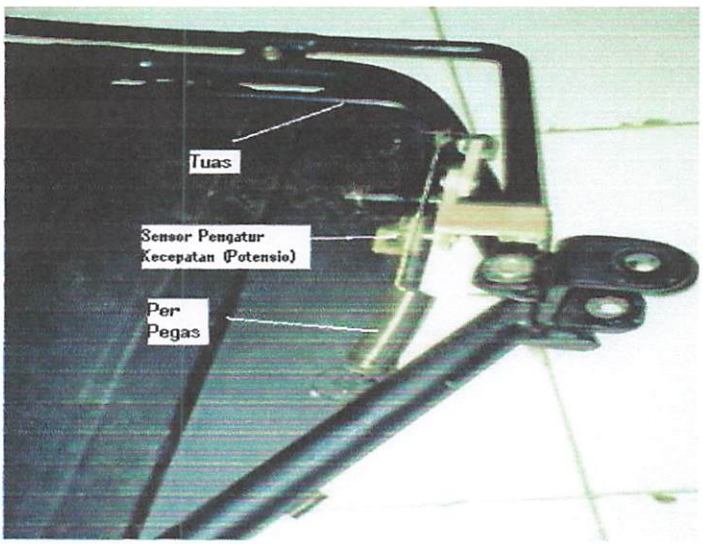
Pada saat menginjak tuas, gokart bergerak atau jalan. Untuk menambah kecepatan tekan tombol up yang ada di steer atau kemudi disebelah kiri maka gear akan berpindah turun ke gear lebih kecil dan pada saat menurunkan kecepatan tekan tombol down yang terdapat di steer juga yang berada disebelah kanan, maka gear akan berpindah naik ke gear lebih besar.

Pada gokart terdapat juga tuas rem yang terhubung dengan diskbreak pada roda belakang, Untuk menghentikan Gokart injak tuas rem.

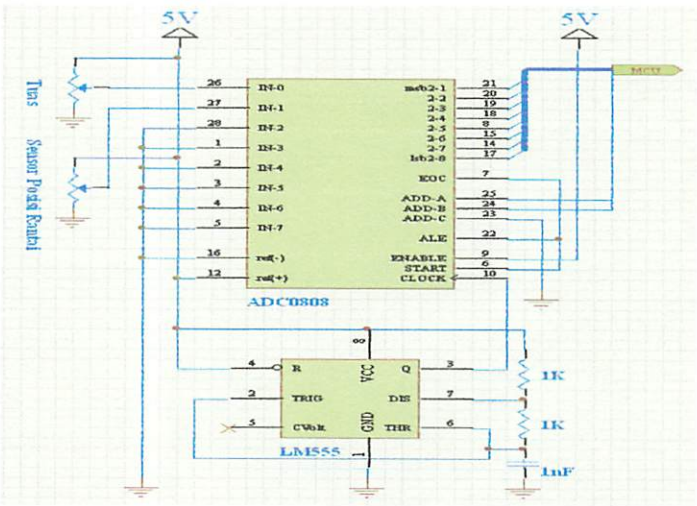
3.2.2 Sensor Pengatur Kecepatan (Potensiometer)

Pada perancangan rangkaian Sensor Pengatur Kecepatan yang dihubungkan dengan tuas pada saat tuas di injak maka potensiometer akan berputar sehingga akan berfungsi mengubah besaran-analog yang selanjutnya akan dimasukan atau sebagai inputan ke ADC 0808.

Gambar 3.2 menunjukkan perancangan hubungan sensor pengatur kecepatan (potensio) dengan tuas dan gambar 3.3 menunjukkan rangkaian sensor pengatur kecepatan (potensio).



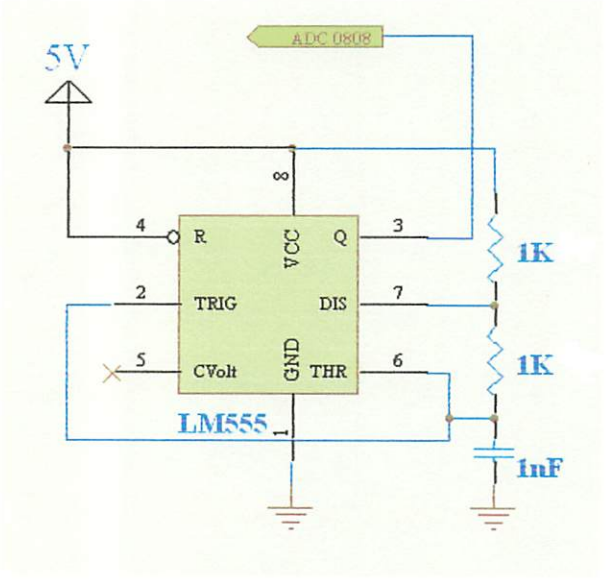
Gambar 3.2 Hubungan Sensor Pengatur Kecepatan (Potensio) Dengan Tuas



Gambar 3.3 Rangkaian Sensor Pengatur Kecepatan (Potensio)

3.2.3 Rangkaian Astable LM 555

Rangkaian astable dibuat dengan mengubah susunan resitor dan kapasitor luar pada IC 555. Gambar 3.4 menunjukkan Rangkaian astable.



Gambar 3.4 Rangkaian Astable[11]

Ada dua buah resistor Ra dan Rb serta satu kapasitor eksternal C yang diperlukan. Prinsipnya rangkaian astable dibuat agar memicu dirinya sendiri berulang-ulang sehingga rangkaian ini dapat menghasilkan sinyal osilasi pada keluarannya. Pada saat power supply rangkaian ini di hidupkan, kapasitor C mulai terisi melalui resistor Ra dan Rb sampai mencapai tegangan 2/3 VCC. Pada saat tegangan ini tercapai, dapat dimengerti komparator A dari IC 555 mulai bekerja mereset flip-flop dan seterusnya membuat transistor Q1 ON. Ketika transisor ON, resitor Rb seolah dihubung singkat ke ground sehingga kapasitor C membuang muatannya (discharging) melalui resistor Rb. Pada saat ini keluaran pin 3 menjadi 0 (GND). Ketika discharging, tegangan pada pin 2 terus turun sampai mencapai

1/3 VCC. Ketika tegangan ini tercapai, bisa dipahami giliran komparator B yang bekerja dan kembali memicu transistor Q1 menjadi OFF. Ini menyebabkan keluaran pin 3 kembali menjadi high (VCC). Demikian seterusnya berulang-ulang sehingga terbentuk sinyal osilasi pada keluaran pin3. Terlihat di sini sinyal pemicu (trigger) kedua komparator tersebut bekerja bergantian pada tegangan antara 1/3 VCC dan 2/3 VCC. Inilah batasan untuk mengetahui lebar pulsa dan periode osilasi yang dihasilkan.

Rumus frekuensi :

$$f = \frac{1}{(Ra + Rb).C}$$

Diketahui : Frekuensi clock pada ADC 0808 antara 10 Khz sampai dengan 640 Khz (referensi dari data sheet).

Maka :

Ferkuensi clock = 640 Khz

$$Ra + Rb = \frac{1/f}{C}$$

$$= \frac{1/640}{1.10^{-9}}$$

$$= \frac{1{,}56}{1.10^{-9}} = 1{,}56\ K\Omega$$

$$Ra = Rb = \frac{1,56}{2}$$

$$= 0,78\ K\Omega$$

Jadi : Ra = 0,78 dan Rb = 0,78. Karna dipasaran tidak dijual Resistor 0,78 KΩ maka dibulatkan jadi 1 KΩ.

Sedangkan nilai C difixkan dengan nilai 1nF, agar dapat mencari nilai Ra dan Rb.

Nilai frekuensi clock ADC 0808 :

$$f = \frac{1}{(Ra + Rb).C}$$

$$= \frac{1}{(1K\Omega + 1K\Omega).1nF}$$

$$= \frac{1}{2x10^{-6}} = 500000\ hz = 500\ Khz.$$

3.2.4 Mikrokontroler AT 89S51

3.2.4.1 Mikrokontroler Sebagai Sistem Minimum

Pada bagian ini akan dibahas tentang perancangan perangkat keras yang terdiri dari Rangkaian Minimum AT89S51, Rangkaian driver motor PWM, Rangkaian driver motor dua arah On/Off, Rangkaian lampu indicator, Rangkaian ADC 0808, dan Rangkaian tombol Up dan Down. Rangkaian tersebut tersusun dari komponen-komponen 3 buah kapasitor, sebuah resistor, dan sebuah kristal atau resonator keramik.Rangkaian kapasitor dan kristal atau resonator keramik digunakan sebagai rangkaian pembangkit internal clock generator yang terdapat pada AT89S51. Nilai kapasitasi ditentukan sesuai dengan jenis oscillator yang

digunakan, yaitu :

C1 dan C2 = 20pF – 40pF untuk kristal

C1 dan C2 = 30pF – 50pF untuk resonator keramik

Karena dalam rancangan digunakan oscillator kristal maka harga kapasitor yang digunakan adalah sebesar 33pF.

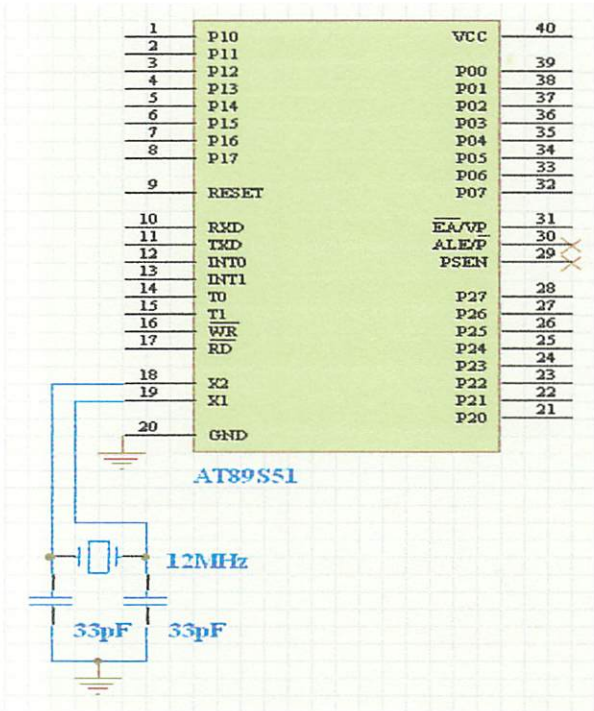
Mikrkontroler AT89S51 mempunyai frekuensi maksimal 12 MHz, dimana 1 siklus mesin = 12 clock. Dalam rangkaian digunakan kristal dengan harga 12 MHz, maka program akan dijalankan pada setiap langkahnya selama 1 μs. Siklus tersebut diambil berdasarkan ketentuan mikrokontroler AT89S51 yaitu 12 clock = 1 siklus mesin, sedangkan frekuensi yang digunakan 12 MHz, maka waktu yang dipakai dalam setiap 1 siklus mesin adalah 1 μs. Dengan demikian perhitungannya dapat dilihat sebagai berikut :

$f = 12000Hz \qquad T = \frac{1}{f} \qquad T = \frac{1}{12000X10^6}$

Karena 1 siklus meain = 12T maka,

$1\ Siklus\ mesin = 12 \times \frac{1}{12000X10^6} = 1\ \mu s$

Gambar 3.5 menunjukkan Rangkaian Minimum Sistem Mikrokontroler.

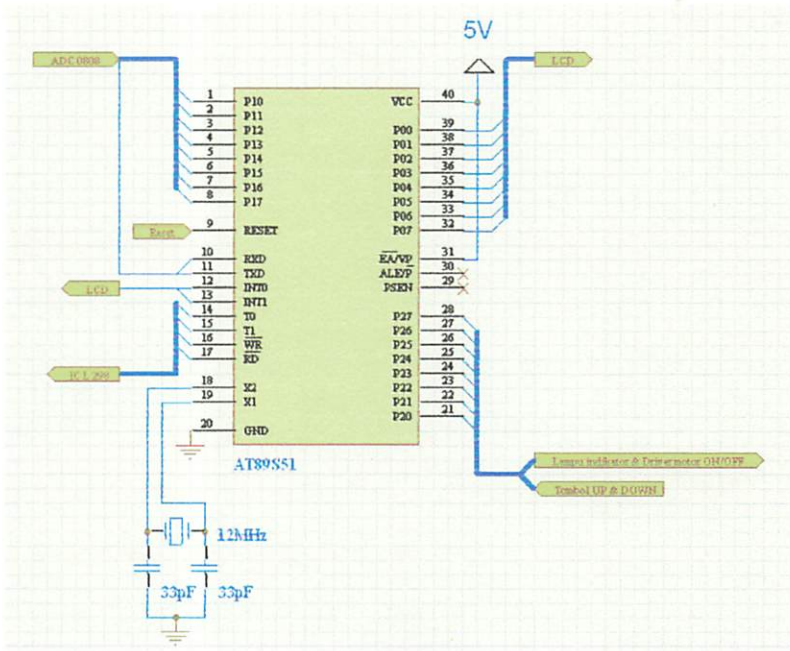


Gambar 3.5 Rangkaian Minimum Sistem Mikrokontroler AT89S51

3.2.4.2 Perancangan Port - Port Pada Mikrokontroler AT89S51

Pada perancangan rangkaian Mikrokontroler AT 89S51 digunakan sebagai pusat pengendali kerja dari alat yang dibuat karena pada IC inilah akan disimpan program-program (*software*) perintah serta alamat yang akan dituju program. Untuk melaksanakan fungsi tersebut diatas maka perlu dirancang port-port I/O serta sinyal-sinyal yang akan digunakan dengan seksama.

Gambar 3.6 menunjukkan rancangan port-port I/O serta sinyal-sinyal pada IC Mikrokontroler AT89S51.



Gambar 3.6 Rancangan Pemakaian Port-Port Mikrokontroler AT89S51

- **Port 0**

Port 0 merupakan port dua fungsi yang berada pada pin 32-39 dari IC AT89S51. Dalam perancangan P0.0 – P0.7 digunakan sebagai port keluaran ke LCD.

- **Port 1**

Port 1 disediakan sebagai port I/0 dan menempati pin 1 – 8, dalam perancangan alat pin 1 – 8 digunakan sebagai masukan dari ADC 0808.

- **Port 2**

Port 2 disediakan sebagai I/O dan menempati pin 21 – 28.Dalam perancangan alat pin 21 – 28 digunakan sebagai masukan dari driver motor pwm, tombol up dan down, dan indikator kecepatan.

- **Port 3**

Port 3 merupakan port dua fungsi, yaitu sebagai I/O. Port ini terletak pada pin 10 – 17. Dalam perancangan alat, pin 10 dan 11 terhubung dengan ADC 0808 pada output pin 24 dan 25. Pada pin 12 dan 13 terhubung dengan input dari LCD pada pin 4 dan 6. Pada pin 14 – 17 terhubung dengan input IC L 289 pada pin 11 dan 13.

- ***PSEN (Program Strore Enable)***

PSEN adalah suatu sinyal keluaran yang terdapat pada pin 29. Fungsinya adalah sebagai sinyal kontrol untuk memungkinkan mikrokontroler membaca program (code) dari memori eksternal. Jika eksekusi program dari ROM internal (8051/8052) atau dari flash memori AT89S51, maka *PSEN* berada pada kondisi tidak aktif (high).

- **ALE (*Addres latch Enable)***

Sinyal output ALE yang berada pada pin 30 fungsinya untuk demultipleks bus alamat dan bus data. Sinyal ALE membangkitkan pulsa sebesar 1/6 frekwensi oscilator dan dapat dipakai sebagai clock yang dipergunakan secara umum.

- ***EA (External Access)***

Masukan sinyal *EA* terdapat pada pin 31 yang dapat diberikan logika rendah (pin terhubung ground) atau logika tinggi (pin terhubung Vcc).

Jika *EA* diberikan logika tinggi, maka mikrokontroler akan mengakses program dari ROM internal (EPROM/flash memory). Jika *EA* diberikan logika rendah, maka mikrokontroler akan mengakses program dari memori eksternal. Pada perancangan ini EA dihubungkan ke VCC 5 Volt.

- **RST *(Reset)***

Input reset pada pin 9 adalah reset master untuk AT89S51.

- ***Oscilator***

Oscilator yang disediakan pada pin chip dikemudikan dengan XTAL, yang dihubungkan pada pin 18 dan pin 19. Besar nilai XTAL yang digunakan sebesar 11,0592 MHz untuk keluarga MCS-51, dan diperlukan dua buah kapasitor penstabil sebesar 33pF.

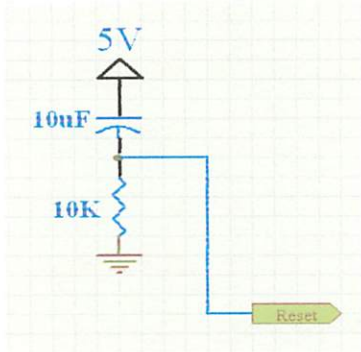
- **Vcc**

AT89S51 dioprasikan dengan tegangan supply +5V. Pin Vcc berada pada pin 40 sedangkan Vss (ground) berada pada pin 20.

3.2.4.3 Rangkaian RESET

Untuk mereset Mikrokontroler AT89S51, maka pin reset diberi logika tinggi selama sekurangnya dua siklus mesin (24 periode). Untuk membangkitkan sinyal reset, kapasitor dihubungkan dengan Vcc dan sebuah resistor yang dihubungkan ke ground.

Gambar 3.7 menunjukkan Rangkaian Reset Pada Mikrokontroler AT89S51.



Gambar 3.7 Rangkaian Reset Pada Mikrokontroler AT89S51

Karna kristal yang digunakan mempunyai frekuensi sebesar 12 Mhz, maka satu periode membutuhkan waktu sebesar:

$$T = \frac{1}{fxTAL} = \frac{1}{12Mhz} S = 8{,}333 \times 10^{-8} \text{ S.}$$

Sehingga waktu minimal logika tinggi yang dibutuhkan untuk mereset mikrokontroler adalah :

Reset (min) = T x periode yang dibutuhkan

$= 8{,}333 \times 10^{-8} \times 24 = 1{,}999$ µs.

Jadi mikrokontroler membutuhkan waktu minimal 1,999 µs untuk mereset. Waktu minimal inilah yang dijadikan pedoman untuk menentukan nilai R dan C. Dari persamaan konstanta waktu T = R x C (Malvino, 1984 : 152) dan jika nilai R ditentukan sebesar 10 KΩ (manual datasheet book AT89S51). Maka nilai C adalah :

$$C = \frac{T}{R}$$

$$= \frac{1{,}999x10^{-6}}{10x10^{3}} = 199{,}9 \times 10^{-12}$$

Kapasitor minimal yang dibutuhkan adalah 199,9 PF. Dengan menggunakan kapasitor sebesar 10 μF, maka akan menjamin waktu reset diatas nilai minimal waktu yang dibutuhkan untuk mereset mikrokontroler.

3.2.5 Driver Motor PWM

Pada perancangan rangkaian Driver Motor PWM (Pulse Width Modulation) akan menerima dan mengolah instruksi dari Mikrokontroler AT 89S51. Driver Motor PWM menggunakan Mosfet IRFZ44N dengan tegangan maksimun 55 volt dan arus maksimum 49 Ampere.

3.2.5.1 Analisa

Sfesifikasi Motor DC Gear box :

- Kosong tanpa beban = 3,88 A
- Beban 20 Kg = 7,87 A
- Beban 70 Kg = 8,98 A

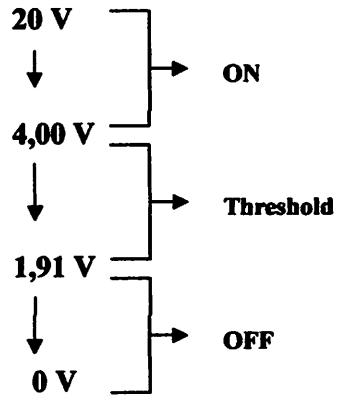
Diketahui arus max = 8,98 A dan tegangan = 24 V, maka Watt = Tegangan x Arus:

W = 24 V x 8,98 A = 215,52 Watt.

Karna pada Motor Gear Box tidak ada name plate atau keterangan sfesifikasi yang lengkap, Maka Motor Dc Gear Box di ukur untuk mengetahui beban maksimum dan tanpa beban menggunakan Avo meter Ampere, Sfesifikasi Motor Gear Box diatas adalah hasil pengukurannya.

Yaitu didapat 8,98 A pada beban 70 Kg Maka dirancang Mosfet

sebagai driver. Menggunakan Mosfet IRFZ 44N karena mempunyai power drssipation = 94 w dan arus 49 Ampere (sumber: datasheet) pada tegangan 1,91 Volt (Tegangan Threshold). Tegangan Threshold adalah dimana suatu tegangan dapat memutar motor pada tegangan terendah dari 0 Volt sampai 20 Volt dapat dilihat pada gambar 3.8 di bawah.



Gambar 3.8 Tegangan Off, Threshold, dan On

Transistor 9013 :

Analisa

Mikrokontroler memiliki output (keluaran) 'I' dan '0'. Pada saat 'I' transistor 9013 aktif, dikarenakan :

$$Ib = \frac{V - Vbc}{R} \qquad Ic = Ib \times Hfe$$

$$= \frac{5 - 0{,}7}{10} \qquad = 0{,}43 \times 60$$

$$= 0{,}43 \text{ mA.} \qquad = 25{,}8 \text{ mA}$$

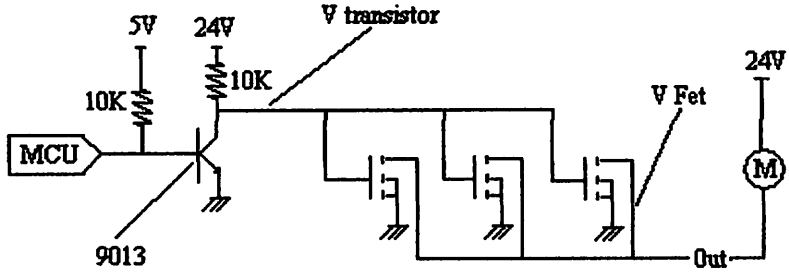
Transistor aktif dan Arus Ic langsung terhubung ke Ground pada transsistor 9013. Sedangkan mosfet mati karena transistor yang sebagai swith dalam keadaan aktif langsung mengalirkan arus ke ground.

Saat Mikrokontroler mengeluarkan '0' transistor Off, dikarenakan :

Ib = 0 mA.

Mosfet hidup karena transistor yang sebagai swith dalam keadaan mati, sehingga tegangan 24 v mengalir ke Mosfet melalui R = 10 KΩ dan menjalankan Motor DC.

Gambar 3.9 menunjukkan Transistor 9013 dan Mosfet Irfz 44n.



Gambar 3.9 Transistor 9013 dan Mosfet Irfz 44n

R = 10 KΩ Pada Transistor 9013 digunakan karena mampu menghasilkan Ib = 0,43 mA dan Ic = 25,8 mA, bisa melawan I Gate + pull Up = 2,4 mA ($\frac{24V}{10K\Omega}$ = 2,4 mA) pada mosfet.

Alasan menggunakan 9013 adalah sebagai Swicthing yang memiliki medium frekuensi switching 1-10 Mhz cukup untuk PWM 1 Khz.

Mosfet IRFZ 44N

Analisa:

Arus yang dihasilkan Mosfet pada I Gate = 0,01 mA, dan V Gate = ± 20 Volt. R = 10 KΩ pada Gate Mosfet Agar memberi Arus pada Gate sebesar $\frac{24}{10} = 2{,}4$ mA. Arus ini cukup untuk Mosfet.

Jika tegangan yang digunakan adalah 24 Volt :

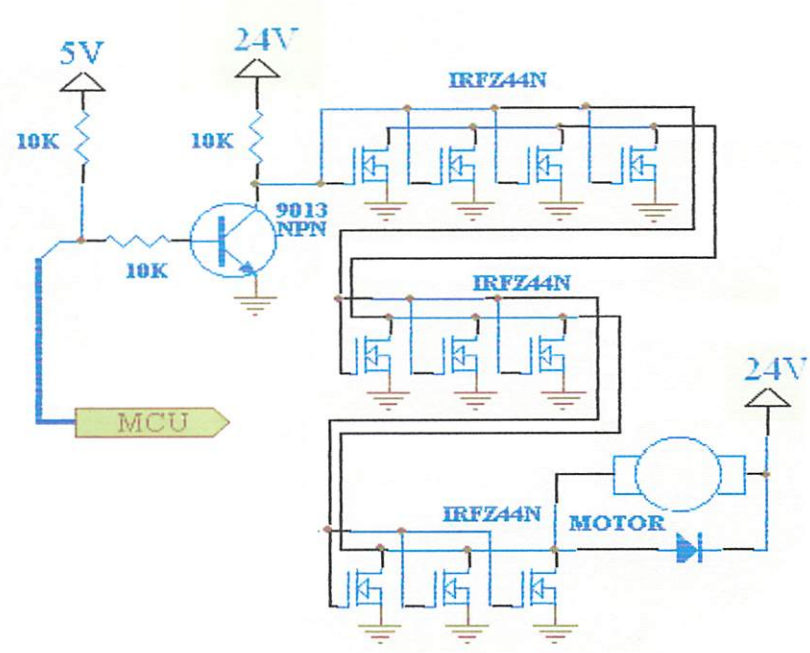
Maka Arus : $\frac{94watt}{24Volt} = 3{,}916$ Ampere

Dalam perancangan akan dipasang 10 Mosfet, maka Arus : 10 x 3,916Ampere = 39,16 Ampere.

Mosfet dirancang Agar mampu me-supply motor dengan beban 8,98 A yaitu Arus Mosfet 4x lebih besar dari Arus Motor sehingga motor tidak panas karena kurang Arus.

Alasan menggunakan Mosfet Irfz44n adalah sebagai switching dan memiliki I (arus) sangat besar sehingga motor dapat berputar kuat.

Gambar 3.10 menunjukkan rangkaian driver motor



Gambar 3.10 Rangkaian Driver Motor

Tabel 3.1 menunjukkan hubungan mikrokontroler AT89S51, transistor NPN 9013, dan mosfet IRFZ 44N.

Tabel 3.1 Hubungan mikrokontroler AT89S51, transistor NPN 9013, dan mosfet IRFZ 44N.

Logic	V µc	Transistor	V Transistor	Mosfet	V Mosfet	Motor
I	4,44 V	ON	0,05 V	OFF	11,99 V	OFF
O	0,01 V	OFF	12,00 V	ON	0,05 V	ON

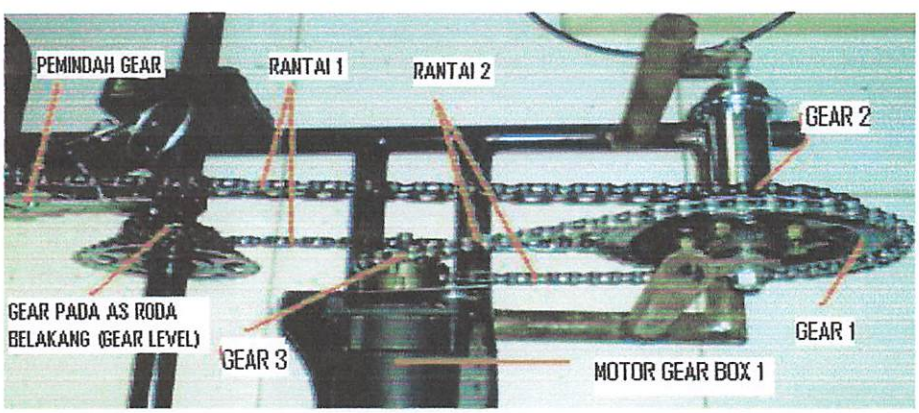
Penjelasan Tabel :

- Apabila Mikrokontroler logic "I" maka tegangan keluaran Mikrokontroler 4,99 V, transistor akan aktif atau on tegangan transistor 0,05 V mosfet akan off tegangan keluaran mosfet 11,99 V, maka motor akan mati atau tidak berputar.
- Apabila Mikrokontroler logic "O" maka maka tegangan keluaran Mikrokontroler 0,01 V, , transistor akan mati atau off tegangan transistor 12,00 V mosfet akan on atau aktif dan tegangan outputnya 0,05 V, maka motor akan hidup atau berputar.

3.2.6 Motor Gear Box 1

Pada perancangan unit motor gear box, motor yang terhubung dengan gear dan rantai akan berputar menghasilkan kecepatan yang dapat diubah.

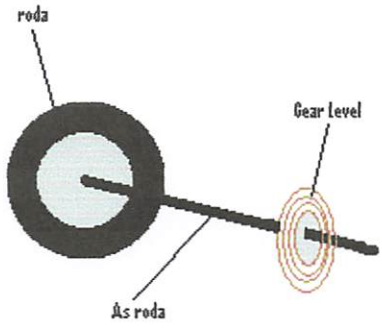
Gambar 3.11 menunjukkan Perancangan Motor Gear Box 1.



Gambar 3.11 Perancangan Motor Gear Box 1

3.2.7 Roda

Pada perancangan unit roda terdiri dari as roda, dan pada as roda terdapat 6 gear yang dapat melakukan 6 perubahan kecepatan Gambar 3.12 menunjukkan Sketsa Perancangan Roda Belakang.



Gambar 3.12 Sketsa Perancangan Roda Belakang

3.2.8 Driver Motor Dua Arah On/Off

Sfesifikasi Motor DC Gear box

- Arus motor 2 Ampere
- Tegangan 24 volt

Pada perancangan rangkaian Driver Motor Dua Arah ON/OFF terdiri dari IC L 298 yang akan menguatkan instruksi-instruksi dari Mikrokontroler AT 89S51 pada inputan IC L 298 pin 11 dan pin 13. Tegangan maksimum sampai dengan 46 volt dan arus maksimum 4 Ampere. Analisa driver motor dua arah

on/off dapat dijelaskan pada tabel logic berikut. Tabel 3.2 menunjukkan Analisa driver motor dua arah on/off logic IC L 298.

Tabel 3.2 Driver Motor Dua Arah On/Off Logic Ic L 298

In A	In B	Motor	Arah putaran
O	O	OFF	---
O	I	ON	Kiri
I	O	ON	Kanan
I	I	OFF	---

Penjelasan :

- Pada saat logic In A "O" dan logic In B "O", maka motor akan OFF atau tidak berputar.
- Pada saat logic In A "O" dan logic In B "I", maka motor akan berputar ke arah kiri.
- Pada saat logic In A "I" dan logic In B "O", maka motor akan berputar ke arah kanan.
- Pada saat logic In A "I" dan logic In B "I", maka motor akan OFF atau tidak berputar.

Rangkaian driver motor dua arah on/off dapat dilihat pada gambar 3.12 dibawah ini.

Perhitungan Posisi Gear

Tabel 3.3 Posisi Gear

Gear	Potensio 50 KΩ		% Potensio	V out potensio	Data ADC
	R1 KΩ	R2 KΩ			
1	28,42	21,58	56,84	2,842	145
2	32,34	17,66	64,68	3,234	165
3	34,3	15,7	68,6	3,43	175
4	37,24	12,76	74,48	3,724	190
5	40,18	9,82	80,36	4,018	205
6	43,12	6,88	86,24	4,312	220

1. Rumus untuk mencari V out potensio = Data ADC x 0,0196
   - *0,0196 di dapat dari, tegangan adc : jumlah pembacaan adc* $= \frac{5}{255}$
2. Rumus untuk mencari R1 pada potensio :
   - Maka: V out pot $= \frac{R1}{pot}$ x V

     $R1 = \frac{Voutxpot}{V}$
3. Rumus mencari R2 = 50 KΩ – R1
4. Rumus mencari % potensio $= \frac{R1}{pot}$ x 100%

Perhitungan Tabel 4.2 Posisi Gear

Posisi Gear "1" Untuk Data ADC 145 :

- V out pot = 145 x 0,0196 = 2,842 V

- $R1 = \frac{2{,}842x50}{5} = 28{,}42\ K\Omega$
- $R2 = 50\ K\Omega - 28{,}42\ K\Omega = 21{,}58\ K\Omega$
- $\%\ potensio = \frac{28{,}42K\Omega}{50K\Omega} x\ 100\% = 56{,}84\ \%$

Posisi Gear "2" Untuk Data ADC 165 :

- V out pot = 165 x 0,0196 = 3,234 V
- $R1 = \frac{3{,}234x50}{5} = 32{,}34\ K\Omega$
- $R2 = 50\ K\Omega - 32{,}34\ K\Omega = 17{,}66\ K\Omega$
- $\%\ potensio = \frac{32{,}34K\Omega}{50K\Omega} x\ 100\% = 64{,}68\ \%$

Posisi Gear "3" Untuk Data ADC 175 :

- V out pot = 175 x 0,0196 = 3,43 V
- $R1 = \frac{3{,}43x50}{5} = 34{,}3\ K\Omega$
- $R2 = 50\ K\Omega - 34{,}3\ K\Omega = 15{,}7\ K\Omega$
- $\%\ potensio = \frac{34{,}3K\Omega}{50K\Omega} x\ 100\% = 68{,}6\ \%$

Posisi Gear "4" Untuk Data ADC 190 :

- V out pot = 190 x 0,0196 = 3,724 V
- $R1 = \frac{3{,}724x50}{5} = 37{,}24\ K\Omega$
- $R2 = 50\ K\Omega - 37{,}24\ K\Omega = 12{,}76\ K\Omega$

- % potensio = $\frac{37{,}24K\Omega}{50K\Omega}$ x 100% = 74,48 %

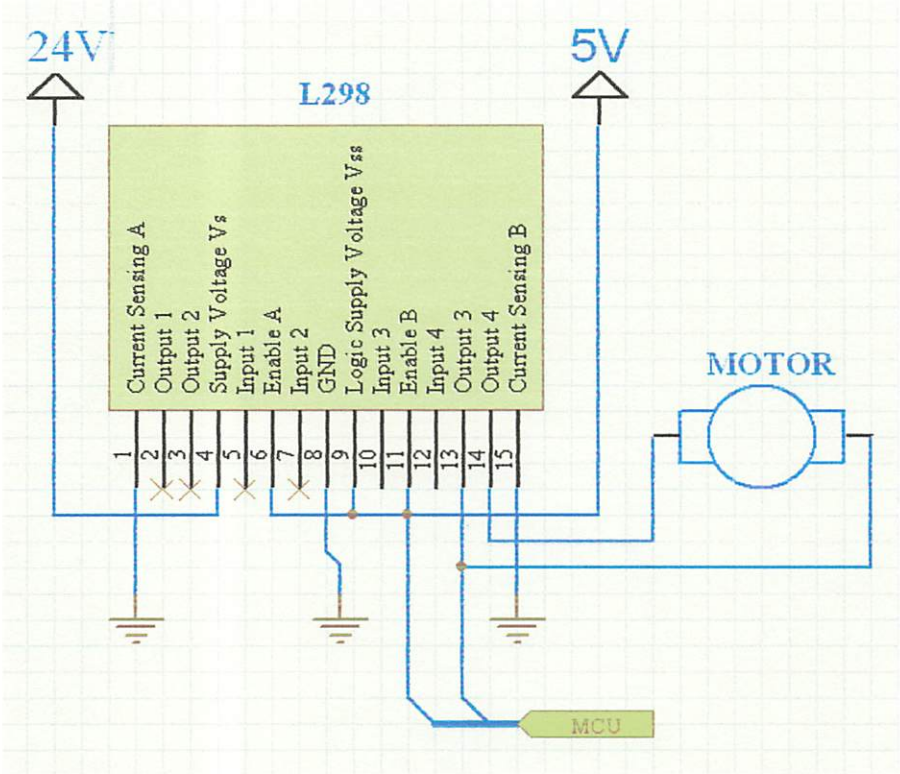
Posisi Gear "5" Untuk Data ADC 205 :

- V out pot = 205 x 0,0196 = 4,018 V
- R1 = $\frac{4{,}018x50}{5}$ = 40,18 KΩ
- R2 = 50 KΩ – 40,18 KΩ = 9,82 KΩ
- % potensio = $\frac{40{,}18K\Omega}{50K\Omega}$ x 100% = 80,36 %

Posisi Gear "6" Untuk Data ADC 220 :

- V out pot = 220 x 0,0196 = 4,312 V
- R1 = $\frac{4{,}312x50}{5}$ = 43,12 KΩ
- R2 = 50 KΩ – 43,12 KΩ = 6,88 KΩ
- % potensio = $\frac{43{,}12K\Omega}{50K\Omega}$ x 100% = 86,24 %

Gambar 3.13 menunjukkan Rangkaian Driver Motor Dua Arah On/Off



Gambar 3.13 Rangkaian Driver Motor Dua Arah On/Off

3.2.8.1 Analisa Driver Motor dua Arah On/Off

Tabel 3.4 menunjukkan Analisa Driver Motor dua Arah On/Off.

Tabel 3.4 Analisa Driver Motor dua Arah On/Off

Logic (Volt)	Vlogic (Volt)	V logic max	Vdriver (Volt)	Vdriver max	Power (Ampere)	Power max
0	0,02	7 volt	0	50 Volt	1,041	25 W
1	4,98		24			

Penjelasan Analisa

Untuk V logic max, V driver max dan Power max sumber dari datasheet.

Pada saat logic "0" V logic-nya 0,02 Volt dan saat logic "1" maka V logic-nya 4,98 Volt data ini di dapat dari pengukuran dengan Avometer.

Untuk perhitungan Power 1,041 A dengan menggunakan rumus daya :

Arus max yang digunakan pada tegangan 24 V

$$\Rightarrow I = \frac{W}{V}$$

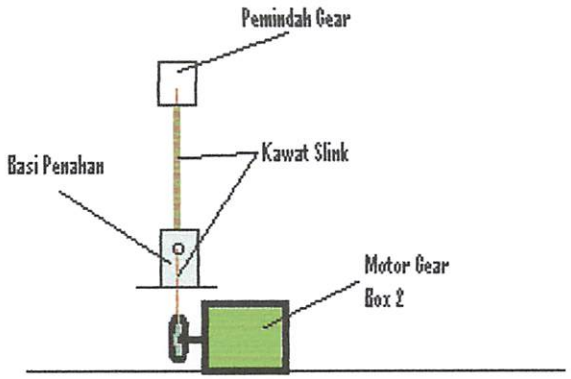
$$= \frac{25W}{24V}$$

= 1, 041 Ampere.

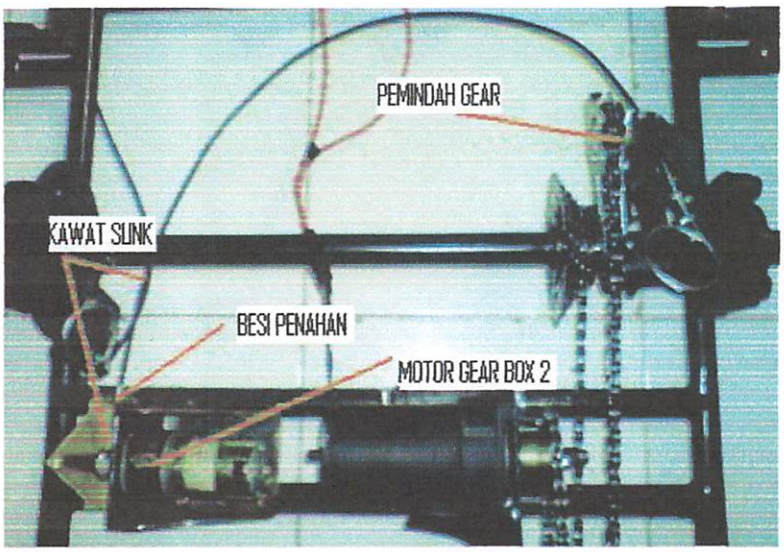
3.2.9 Motor Gear Box 2

Pada perancangan unit Motor Gear Box 2 akan menggerakkan kawat slink agar pemindah gear dapat bergeser kekiri dan kekanan. Pada saat motor gear box 2 berputar kekanan maka akan menarik kawat slink dan apabila motor gear box 2 berputar kekiri maka akan mengulur kawat slink.

Gambar 3.14 menunjukkan sketsa parancangan motor gear box 2 dan gambar 3.15 menunjukkan perancangan motor gear box 2.



Gambar 3.14 Sketsa Perancangan Motor Gear box 2



Gambar 3.15 Perancangan Motor Gear box 2

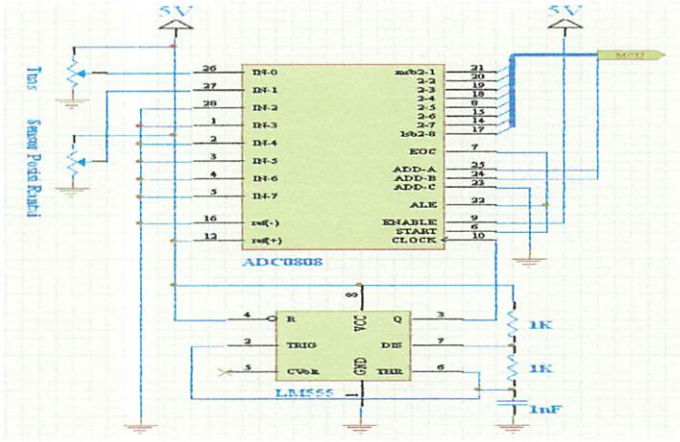
3.2.10 Pemindah Gear

Pada perancangan unit pemindah gear terdiri dari 2 gear yang terbuat dari pelastik berfungsi memindahkan rantai pada gear level dari as roda belakang. Seperti terlihat pada gambar 3.16.

Gambar 3.16 Pemindah Gear[17]

3.2.11 Sensor Posisi Rantai

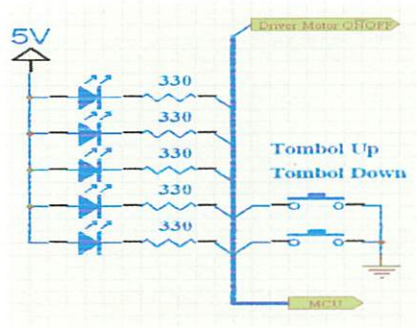
Pada perancangan rangkaian sensor posisi rantai terdiri dari gear, rantai, dan potensiometer yang akan melakukan fungsi sensor pemindahan posisi gear dari gear 1 sampai 5. Gambar 3.17 menunjukkan Rangkaian Sensor Posisi Rantai.



Gambar 3.17 Rangkaian Sensor Posisi Rantai

3.2.12 Tombol Up dan Down

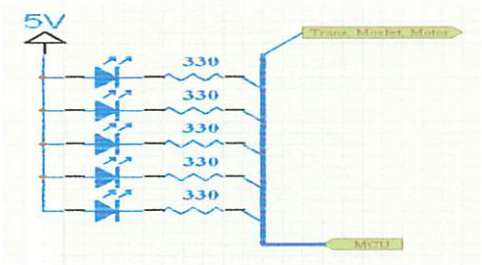
Pada perancangan unit tombol UP dan Down terdiri dari 2 tombol yakni sebagai tombol *down* berfungsi untuk menurunkan kecepatan pada gear yang besar sedangkan tombol *up* berfungsi untuk menaikkan kecepatan pada gear yang kecil. Gambar rangkaian tombol up dan down diperlihatkan pada gambar 3.18



Gambar 3.18 Rankaian Tombol Up dan Down

3.2.13 Lampu Indikator

Pada perancangan unit lampu Indicator terdiri dari enam LED (led emiting diode) yang mengindikasikan/ memberi informasi kecepatan gokart pada gear tertentu. Gambar rangkaian lampu indikator diperlihatkan pada gambar 3.19.



Gambar 3.19 Rangkaian Lampu Indikator

3.2.14 Analisa dari input ADC hingga mengeluarkan sinyal PWM

ADC 0808 memiliki Multiplexer analog 8 Channels berfungsi untuk mengolah 8 input data analog secara bergantian. Untuk memilih input mana yang dikehendaki pada output multiplexer disediakan 3 bit kontrol pemilih saluran input, yaitu ADD-A, ADD-B dan ADD-C dimana dalam perencanaan nantinya semua input ADC yang tersedia merupakan Succesive Aproximation Register 8 bit yang terdiri dari komparator, SAR dan Clock. Tri-state Latch Buffer berfungsi untuk menampung keluaran ADC 8 bit. Tabel 3.1 menunjukkan Data ADC yang diubah ke Biner.

Tabel 3.5 Data ADC yang diubah ke Biner

Data ADC	Volt (mV)	Biner	PWM
30	588	00011110	0FF
40	748	00101000	40
65	1274	01000001	65
95	1862	01011111	95

Penjelasan Tabel 3.5

Untuk data ADC 30 Volt-nya 588 mV (30 x 0,0196 $^{V}/_{data}$) dan biner-nya 00011110 pada saat data adc 40 Volt-nya 748 mV (40 x 0,0196 $^{V}/_{data}$), biner-nya 00101000 saat data adc 65 Volt-nya 1274 mV (65 x 0,0196 $^{V}/_{data}$), biner-nya 01000001 saat data adc maksimum 95 Volt-nya 1862 mV (95 x 0,0196 $^{V}/_{data}$), biner-nya 01011111.

Tabel 3.6 menunjukkan Hubungan Potensio dengan ADC 0808

Tabel 3.6 Hubungan Potensio dengan ADC 0808

% GAS	Potensio 50 KΩ		V 0ut potensio	Data ADC 0808
	R1 (KΩ)	R2 (KΩ)		
15,68	7,84	42,16	0,784	40
25,48	12,74	37,26	1,274	65
41,16	20,58	29,42	2,058	105

1. Rumus untuk mencari V out potensio = Data ADC x 0,0196
   - 0,0196 di dapat dari, tegangan adc : jumlah pembacaan adc = $\frac{5}{255}$
2. Rumus untuk mencari R1 pada potensio :
   - Maka: $V\ out\ pot = \frac{R1}{pot} \times Vin$

     $R1 = \frac{Voutxpot}{Vin}$
3. Rumus mencari R2 = 50 KΩ – R1
4. Rumus mencari % Gas = $\frac{R1}{pot}$ x 100%

Perhitungan analisa tabel 3.6 Hubungan Potensio dengan ADC 0808

1. Untuk data ADC 40 :

   - V out pot = 40 x 0,0196 = 0,784 V
   - $R1 = \frac{0.784x50}{5} = 7{,}84\ K\Omega$
   - $R2 = 50\ K\Omega - 7{,}84\ K\Omega = 42{,}16\ K\Omega$
   - $\%Gas = \frac{7{,}84K\Omega}{50K\Omega} x\ 100\% = 15{,}68\ \%$

2. Untuk data ADC 65 :

   - V out pot = 65 x 0,0196 = 1,274 V
   - $R1 = \frac{1{,}274x50}{5} = 12{,}74\ K\Omega$
   - $R2 = 50\ K\Omega - 12{,}74\ K\Omega = 37{,}26\ K\Omega$
   - $\%Gas = \frac{1{,}274\ K\Omega}{50K\Omega} x\ 100\% = 25{,}48\ \%$

3. Untuk data ADC 105 :
   - V out pot = 105 x 0,0196 = 2,058 V
   - $R1 = \frac{2{,}058x50}{5} = 20{,}58\ K\Omega$
   - $R2 = 50\ K\Omega - 20{,}58\ K\Omega = 29{,}42\ K\Omega$
   - $\%\ Gas = \frac{20{,}58K\Omega}{50K\Omega} = 41{,}16\ \%$

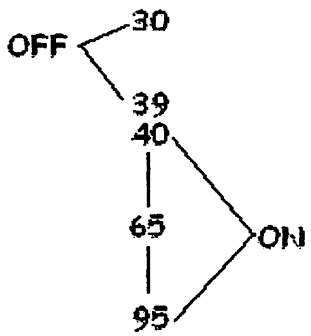
Penjelasan Analisa :

Pada saat tuas/gas (potensio) diinjak hingga mendapat nilai 15, 68% Data PWM dengan nilai 40, dan saat gas diinjak hingga 41,16 % Data PWM dengan nilai 105.

Pada Program mikrokontroler AT89S51 diberi rumus PWM = ADC – 10, artinya adalah data ADC dengan nilai 40 dikurangi 10 menjadi 30 sampai dengan data ADC dengan nilai 105 dikurangi 10 menjadi 95. PWM sendiri mempunyai range dari 0% sampai dengan 100%.

Data PWM menjadi 30 sampai dengan 95, karena pada data PWM 30 motor masih lemah hingga tidak dapat menggerakan gokart maka pada program mikrokontroler AT89S51 di buat rumus = $\frac{Dpwm}{40}$ = jika hasil = 0 , maka motor stop/Off dan jika hasil 1 dan 2 maka motor jalan/On.

Jadi PWM yang dihasilkan mempunyai range : Gambar 3.20 menunjukkan range PWM yang di gunakan.

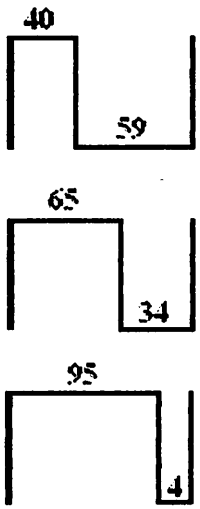


Gambar 3.20 Range Pwm Yang diGunakan

Penjelasan gambar 3.20

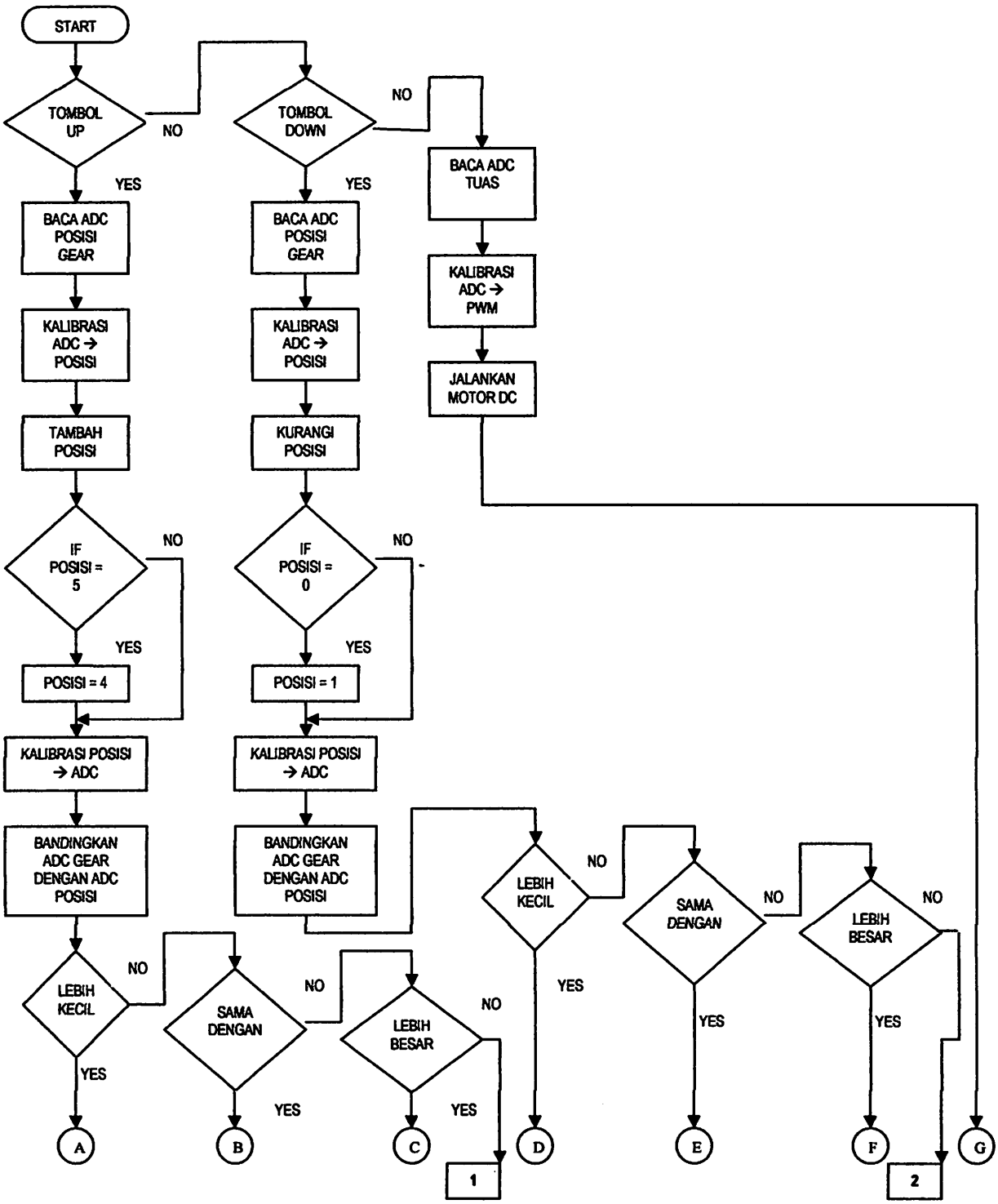
Pada angka 30 sampai 39 menunjukkan bahwa motor tidak berputar atau mati dan pada angka 40 sampai dengan 95 menunjukkan bahwa motor hidup atau berputar.

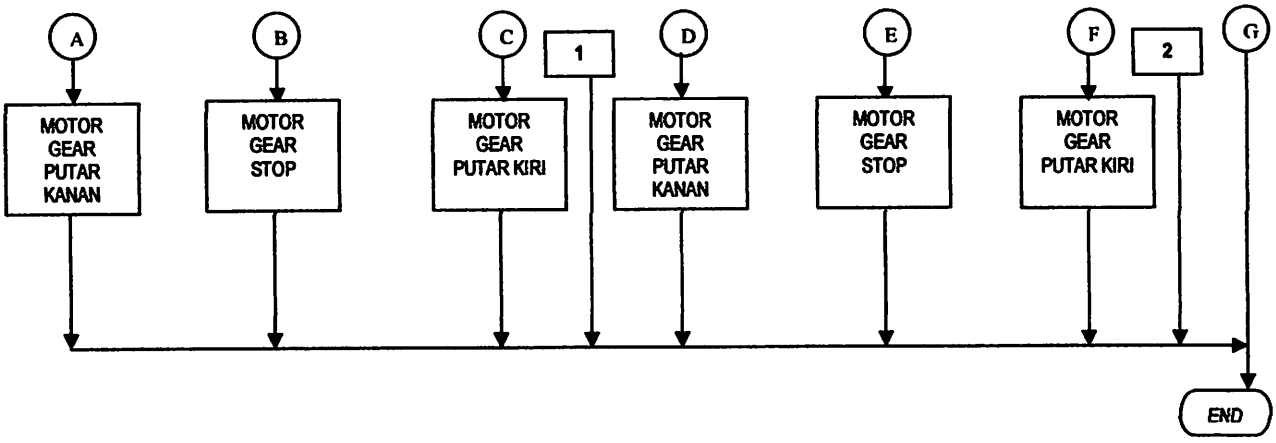
Gambar 3.21 menunjukkan Sinyal PWM



Gambar 3.21 Sinyal PWM

Flowchart


START
TOMBOL UP
NO
YES
TOMBOL DOWN
NO
YES
BACA ADC TUAS
KALIBRASI ADC → PWM
JALANKAN MOTOR DC
BACA ADC POSISI GEAR
KALIBRASI ADC → POSISI
TAMBAH POSISI
IF POSISI = 5
NO
YES
POSISI = 4
BACA ADC POSISI GEAR
KALIBRASI ADC → POSISI
KURANGI POSISI
IF POSISI = 0
NO
YES
POSISI = 1
KALIBRASI POSISI → ADC
KALIBRASI POSISI → ADC
BANDINGKAN ADC GEAR DENGAN ADC POSISI
BANDINGKAN ADC GEAR DENGAN ADC POSISI
LEBIH KECIL
NO
YES
SAMA DENGAN
NO
YES
LEBIH BESAR
NO
YES
LEBIH KECIL
NO
YES
SAMA DENGAN
NO
YES
LEBIH BESAR
NO
YES
A
B
C
D
E
F
G
1
2


A
B
C
1
D
E
F
2
G
MOTOR GEAR PUTAR KANAN
MOTOR GEAR STOP
MOTOR GEAR PUTAR KIRI
MOTOR GEAR PUTAR KANAN
MOTOR GEAR STOP
MOTOR GEAR PUTAR KIRI
END

BAB IV

PENGUJIAN ALAT

4.1 Pendahuluan

Untuk mengetahui cara kerja alat agar sesuai dengan apa yang diharapkan perlu dilakukan pengujian dari masing – masing bagian dari alat yang telah dirancang. Adapun bagian dari rangkaian yang akan di uji meliputi :

- Rangkaian Driver Motor PWM
- Rangkaian Driver Motor Dua Arah On/Off
- Motor Gear Box 1
- Motor Gear Box 2
- Rangkaian Tombol Up dan Down
- Rangkaian Lampu Indikator

Setelah subsistem dirangkai menjadi satu, maka pada bagian akhir akan diuji keseluruhan sistem.

4.2 Perangkat Keras (Hardware)

Driver Motor PWM

4.2.1.1 Tujuan

Untuk mengetahui besar tegangan keluaran dari sensor pengatur kecepatan (potensiometer) yang akan jadi masukan pada ADC 0808 kemudian dilanjutkan ke

mikrokontroler dan yang terakhir ke driver motor PWM.

4.2.1.2 Peralatan yang digunakan

- Catu Daya 12 V
- Tachometer
- Alat Perancangan Motor Gear Box 1

4.2.1.3 Langkah Pengujian

1. Hidupkan Catu Daya
2. Mengukur RPMmotor dan RPMroda

Gambar 4.1 menunjukkan Alat Perancangan Motor Gear Box 1.

Gambar 4.1 Alat Perancangan Motor Gear Box 1

Tabel 4.1 menunjukkan Pengujian Driver Motor PWM dan RPM motor

Tabel 4.1 Hasil Pengujian Pengujian Driver Motor PWM dan RPM motor

PWM	RPM motor
38 %	0
45 %	235
65 %	412
85 %	578

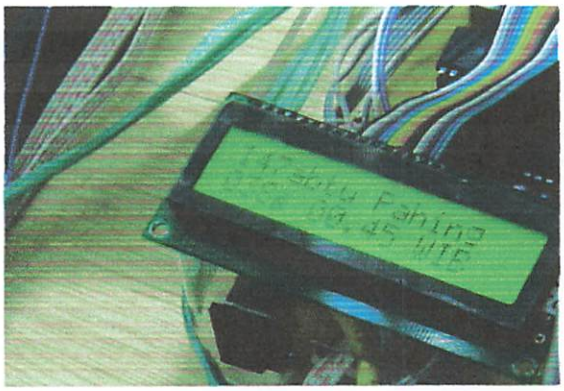
Tabel 4.2 menunjukkan Hasil Pengujian Rpm Roda

Tabel 4.2 Hasil Pengujian Untuk Rpm Roda

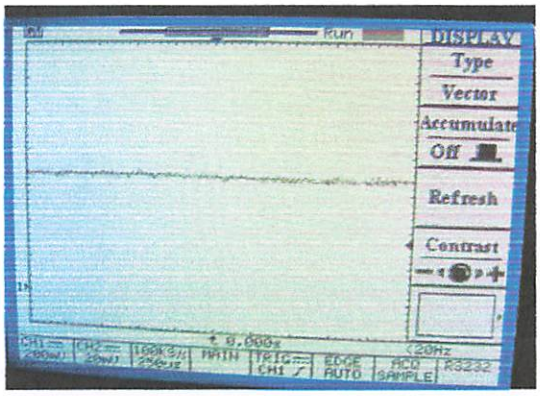
Posisi Gear	PWM	RPM Roda
1	45 %	235
2		240
3		265
4		290
5		301
6		311

- Sample yang diambil adalah 45 % PWM.

Hasil Pengujian

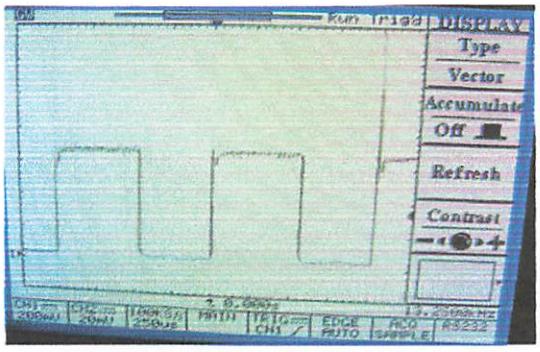


a) Gambar 4.2 Lcd Menjukkan 38%

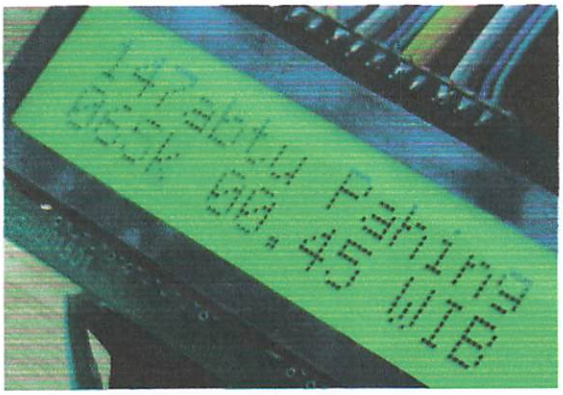


b) Gambar 4.3 Pada Osciloscop Sinyal Tidak Ada

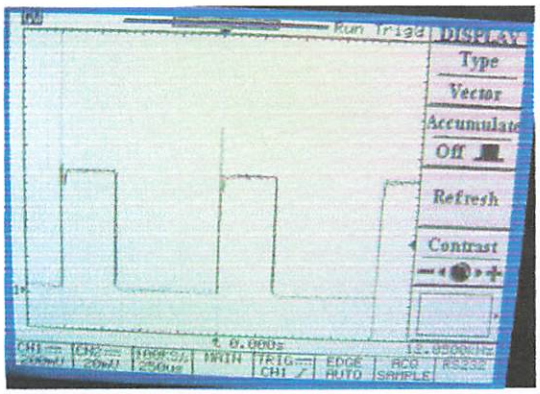
c) Gambar 4.4 Lcd Menjukkan 45%



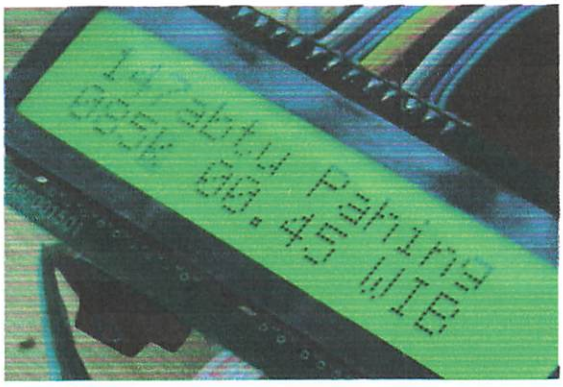
d) Gambar 4.5 pada Osciloscop Sinyal 45%



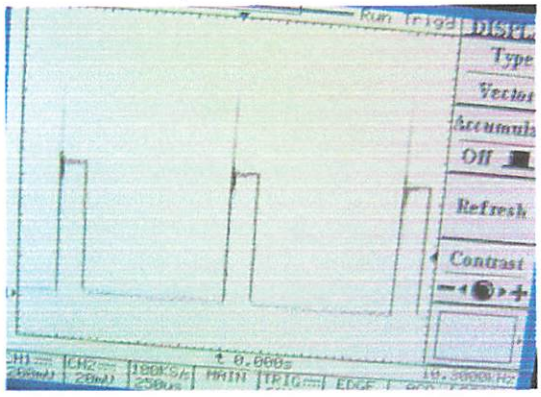
e) Gambar 4.6 Lcd Menjukkan 65%



f) Gambar 4.7 Pada Osciloscop Sinyal 65%



g) Gambar 4.8 Lcd Menjukkan 85%



h) Gambar 4.9 Pada Osciloscop Sinyal 85%

Pada Osciloscop terlihat tegangan DC tidak ada dikarenakan rangkaian pada driver motor aktif low yaitu positif lebih dulu berhubungan dengan motor sedangkan negatif terhubung apabila Mosfet bekerja.

Seperti pada gambar 4.10 menunjukkan Aktif Low.

Gambar 4.10 Aktif LOw

4.2.2 Driver Motor Dua Arah On/Off

4.2.2.1 TUJUAN

Agar dapat mengetahui nilai yang dikeluarkan oleh Vpotensio, % posisi potensio, data ADC dan posisi rantai pada gear level.

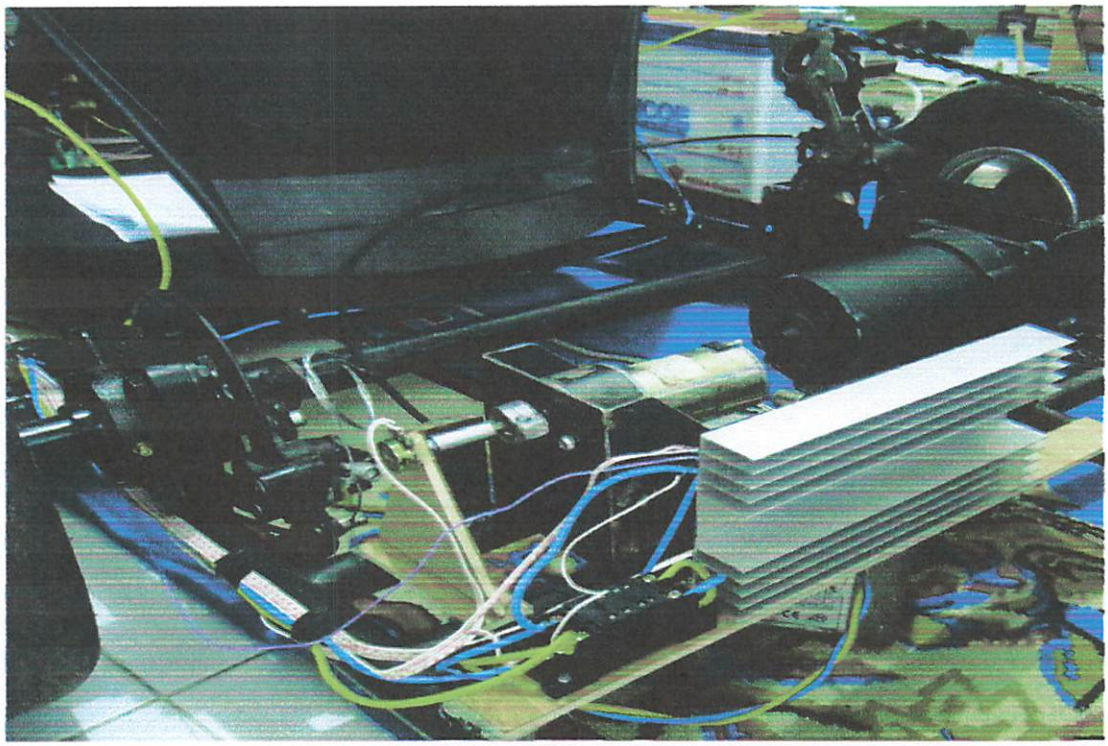
4.2.2.2 Peralatan yang digunakan

- LCD
- Alat Perancangan Motor Gear Box 2
- Catu Daya 24 V
- AVO meter Digital

4.2.2.3 Langkah pengujian

1. Hidupkan Catu Daya
2. Mencari data ADC dengan coba – coba memasukan data ADC sembarang sehingga menghasilkan posisi yang tepat pada gear 1, gear2, gear 3, gear 4, gear 5, dan gear 6.

Gambar 4.11 menunjukkan Alat Perancangan Motor Gear Box 2



Gambar 4.11 Alat Perancangan Motor Gear Box 2

4.2.2.4 Tabel Hasil perhitungan Posisi Gear

Tabel 4.3 menunjukkan hasil perhitungan posisi gear.

Tabel 4.3 Hasil Perhitungan Posisi Gear.

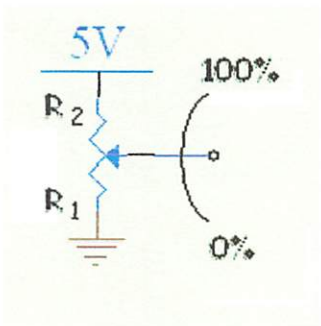
Gear	Potensio 50 KΩ		% Potensio	V out potensio	Data ADC
	R1 KΩ	R2 KΩ			
1	28,42	21,58	56,84	2,842	145
2	32,34	17,66	64,68	3,234	165
3	34,3	15,7	68,6	3,43	175
4	37,24	12,76	74,48	3,724	190
5	40,18	9,82	80,36	4,018	205
6	43,12	6,88	86,24	4,312	220

1. Rumus untuk mencari V out potensio = Data ADC x 0,0196

   - 0,0196 di dapat dari, tegangan adc : jumlah pembacaan adc = $\frac{5}{255}$

2. Rumus untuk mencari R1 pada potensio :

   Gambar 4.13 menunjukkan simbol potensio.



Gambar 4.12 Simbol Potensio

- Maka: $V\ out\ pot = \frac{R1}{pot} \times V$

$$R1 = \frac{Voutxpot}{V}$$

1. Rumus mencari R2 = 50 KΩ – R1

2. Rumus mencari % potensio = $\frac{R1}{pot}$ x 100%

4.2.2.5 Perhitungan Posisi Gear

Posisi Gear "1" Untuk Data ADC 145 :

- V out pot = 145 x 0,0196 = 2,842 V
- $R1 = \frac{2{,}842x50}{5} = 28{,}42\ K\Omega$
- R2 = 50 KΩ – 28,42 KΩ = 21,58 KΩ
- $\%\ potensio = \frac{28{,}42K\Omega}{50K\Omega} \times 100\% = 56{,}84\ \%$

Posisi Gear "2" Untuk Data ADC 165 :

- V out pot = 165 x 0,0196 = 3,234 V
- $R1 = \frac{3{,}234x50}{5} = 32{,}34\ K\Omega$
- R2 = 50 KΩ – 32,34 KΩ = 17,66 KΩ
- $\%\ potensio = \frac{32{,}34K\Omega}{50K\Omega} \times 100\% = 64{,}68$

Posisi Gear "3" Untuk Data ADC 175 :

- V out pot = 175 x 0,0196 = 3,43 V
- $R1 = \frac{3,43x50}{5} = 34,3\ K\Omega$
- R2 = 50 KΩ – 34,3 KΩ = 15,7 KΩ
- % potensio = $\frac{34,3K\Omega}{50K\Omega}$ x 100% = 68,6 %

Posisi Gear "4" Untuk Data ADC 190 :

- V out pot = 190 x 0,0196 = 3,724 V
- $R1 = \frac{3,724x50}{5} = 37,24\ K\Omega$
- R2 = 50 KΩ – 37,24 KΩ = 12,76 KΩ
- % potensio = $\frac{37,24K\Omega}{50K\Omega}$ x 100% = 74,48 %

Posisi Gear "5" Untuk Data ADC 205 :

- V out pot = 205 x 0,0196 = 4,018 V
- $R1 = \frac{4,018x50}{5} = 40,18\ K\Omega$
- R2 = 50 KΩ – 40,18 KΩ = 9,82 KΩ
- % potensio = $\frac{40,18K\Omega}{50K\Omega}$ x 100% = 80,36 %

Posisi Gear "6" Untuk Data ADC 220 :

- V out pot = 220 x 0,0196 = 4,312 V
- $R1 = \frac{4{,}312x50}{5} = 43{,}12\ K\Omega$
- R2 = 50 KΩ – 43,12 KΩ = 6,88 KΩ
- $\%\ potensio = \frac{43{,}12K\Omega}{50K\Omega} x\ 100\% = 86{,}24\ \%$

4.2.2.6 Penjelasan Analisa

1. Tombol ditekan merubah posisi led dari mati semua sampai dengan hidup semua terdiri dari 6 step yang mana setiap step memiliki suatu nilai acuan tertentu untuk posisi gear. Tabel 4.5 menunjukkan posisi gear, led posisi dan acuan

Tabel 4.4 Posisi Gear, Led Posisi Dan Acuan

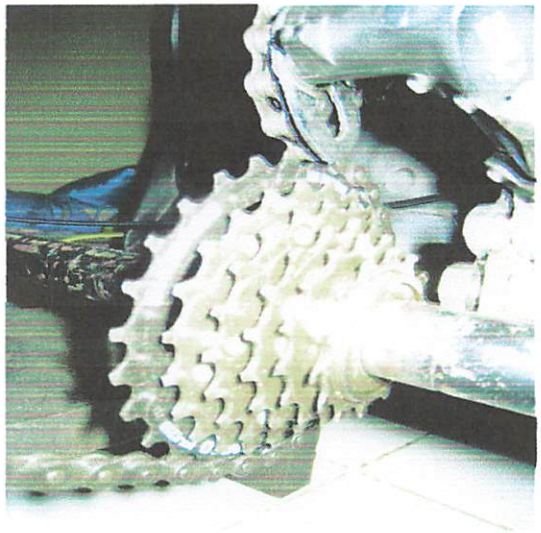
Posisi Gear	Led Posisi	Acuan
1	Semua Led Mati	145
2	Nyala Led 1	165
3	Nyala Led 2	175
4	Nyala Led 3	190
5	Nyala Led 4	205
6	Semua Led Nyala	220

2. Ketika tombol ditekan dan merubah posisi Led maka acuan pun berubah, Mikrokontroler membandingkan data posisi gear (ADC) dengan data acuan dari posisi

led jika data posisi gear (ADC) lebih kecil maka motor pemindah gear akan berputar ke kanan dan sebaliknya jika data posisi gear (ADC) lebih besar maka motor pemindah gear akan berputar ke kiri. Jika nilai sama maka mikrokontroler akan menghitung dan apabila tidak sama maka maka mikrokontroler tidak menghitung, dan jika hitungan sampai dengan 255 x maka program selesai untuk pemindahan posisi. Dapat dipastikan bahwa nilai sama sampai dengan 255 x menyebabkan posisi rantai tepat pada gear.

4.2.2.7 Hasil Pengujian

Gambar 4.13 menunjukkan posisi rantai pada gear 1

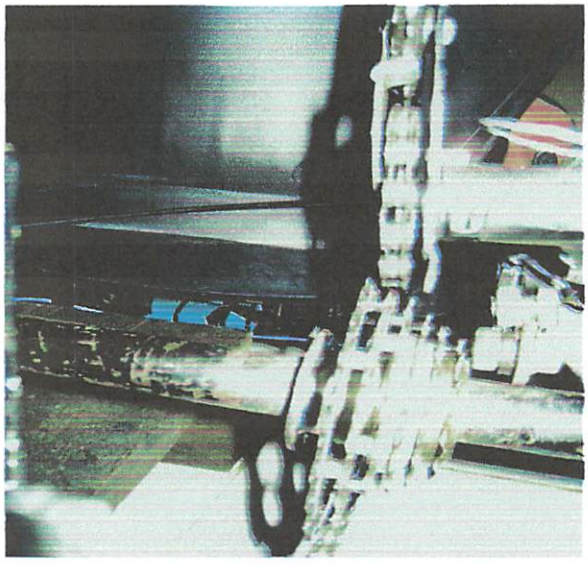


Gambar 4.13 Posisi Rantai Pada Gear 1

Gambar 4.14 menunjukkan lampu led semua mati

Gambar 4.14 Lampu Led Semua Mati

Gambar 4.15 menunjukkan posisi rantai pada gear 2

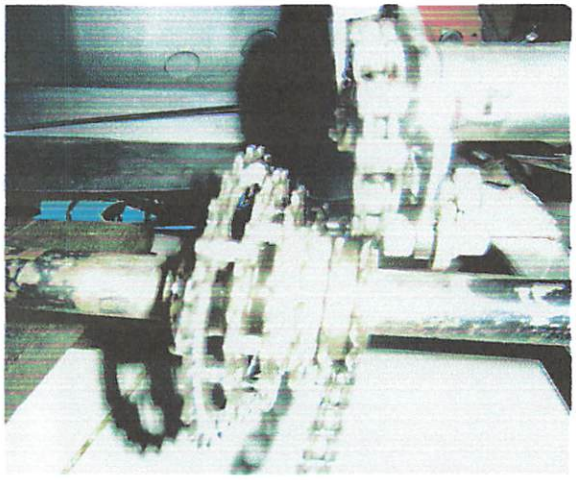


Gambar 4.15 Posisi Rantai Pada Gear 2

Gambar 4.16 menunjukkan lampu led 1 nyala

Gambar 4.16 Lampu Led 1 Nyala

Gamabr 4.17 menunjukkan posisi rantai pada gear 6



Gamabr 4.17 Posisi Rantai Pada Gear 6

Gambar 4.18 menunjukkan lampu led nyala semua

Gambar 4.18 Lampu Led Nyala Semua

4.2.3 Motor Gear Box 1

4.2.3.1 Tujuan

Motor gear box 1 bertujuan untuk menggerakkan gear – gear yang terhubung pada AS roda belakang sehingga gokart dapat bergerak.

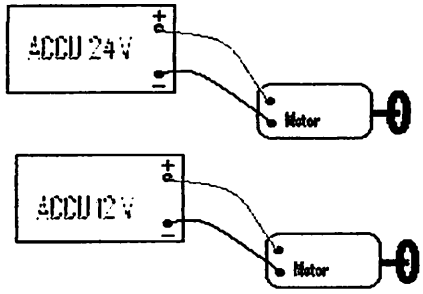
4.2.3.2 Peralatan yang digunakan

- Catu Daya 24
- Tachometer
- AVO meter Digital
- Motor Gear Box 1

4.2.3.3 Langkah Pengujian

1. Sistem dirangkai seperti gambar 4.19
2. Voltmeter Digital dikoneksikan seperti gambar 4.19
3. Tegangan disesuaikan dengan data referensi

Gambar 4.20 Menunjukkan Motor Gear Box 1.



Gambar 4.19 Motor Gear Box 1

4.2.3.4 Hasil Pengujian

Pada saat Motor dc dipasang sumber tegangan 12 V putaran motor 1650 RPM, dan saat motor dc dipasang sumber tegangan 24 V maka putaran motor 3300 RPM.

Tabel 4.6 menunjukkan Hasil Pengukuran Motor Gear Box 1.

Tabel 4.5 Hasil Pengukuran Motor Gear Box 1

Vmotor	RPMmotor
0	0
12	1650
24	3300

4.2.4 Motor Gear Box 2

4.2.4.1 Tujuan

Motor gear box 2 bertujuan untuk menarik pemindah gear menggunakan kawat slink agar pemindah gear dapat bergerak kekiri dan kekanan sehingga rantai dapat berpindah dari gear 1 sampai dengan gear 6.

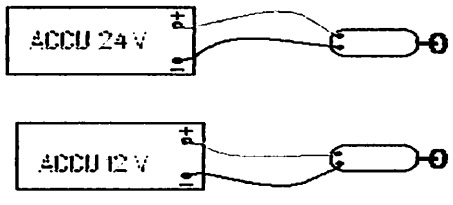
4.2.4.2 Peralatan Penunjang Pengujian

- Catu Daya 24 V
- Tachometer
- AVO meter Digital
- Gambar Perancangan Motor Gear Box 2

4.2.4.3 Langkah Pengujian

1. Sistem dirangkai seperti gambar 4.20
2. Voltmeter Digital dikoneksikan seperti gambar 4.20
3. Tegangan diesuaikan dengan data referensi

Gambar 4.21 menunjukkan Motor Gear Box 2.



Gambar 4.20 Motor Gear Box 2

4.2.4.4 Hasil Pengujian

Pada saat Motor dc dipasang sumber tegangan 12 V putaran motor 1300 RPM, dan saat motor dc dipasang sumber tegangan 24 V maka putaran motor 2800 RPM.

Tabel 4.7 menunjukkan Hasil Pengukuran Motor Gear Box 2.

Tabel 4.6 Hasil Pengukuran Motor Gear Box 2

Vmotor	RPMmotor
0	0
12	1300
24	2800

4.2.5 Tombol UP dan Down

4.2.5.1 Tujuan

Pengujian ini bertujuan untuk mengetahui tegangan pada saat tombol ditekan dan saat tombol dilepas.

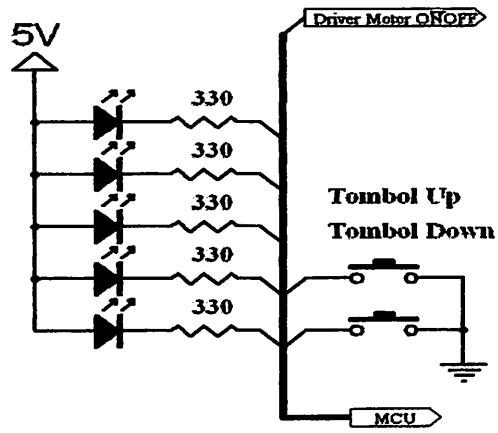
4.2.5.2 Peralatan Penunjang Pengujian

- Rangkaian Tombol Up dan Down seperti gambar 4.13
- AVO meter Digital
- Catu Daya 5 V

4.2.5.3 Langkah Pengujian

1. Sistem dirangkai pada gambar 4.13
2. Tombol Up ditekan kemudian ukur Volt-nya
3. Tombol Down ditekan kemudian ukur Volt-nya

Gambar 4.21 menunjukkan Rangkaian Tombol Up dan Down.



Gambar 4.21 Rangkaian Tombol Up dan Down

4.2.5.4 Hasil Pengujian

Pada saat tombol up ditekan tegangan 1,5 V logic-nya "0" dan saat tombol dilepas tegangan 4,94 V, logic-nya "1". Tombol down ditekan tegangan 1,5 V logic-nya 0 saat tombol dilepas tegangan 4,94 V logic-nya "1".

Tabel 4.8 menunjukkan Hasil Pengukuran Tombol Up dan Down.

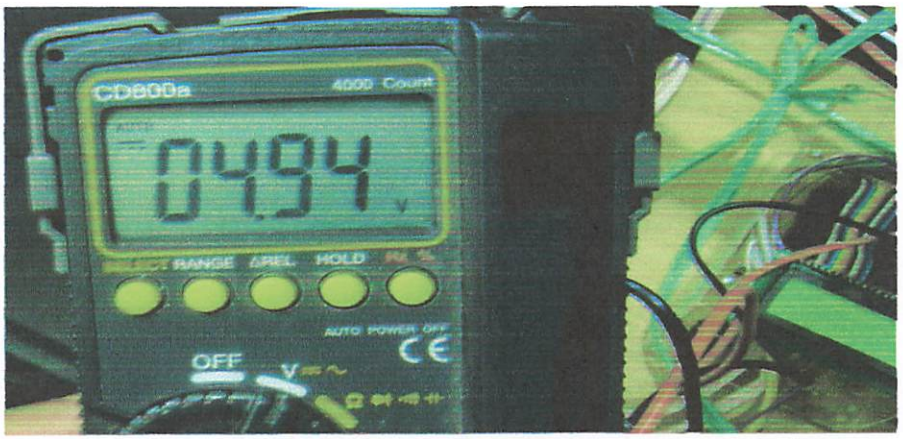
Tabel 4.7 Hasil Pengukuran Tombol Up dan Down

Tombol	Kondisi	Volt	Logic
UP	Ditekan	1,5	0
	Dilepas	4,94	1
Down	Ditekan	1,5	0
	Dilepas	4,94	1

Gambar 4.23 memperlihatkan hasil pengujian pada saat tombol ditekan yaitu tegangan 1,5 Volt.

Gambar 4.22 Hasil Pengujian Saat Tombol Ditekan

Gambar 4.24 memperlihatkan hasil pengujian pada saat tombol dilepas yaitu tegangan 4,94 Volt.



Gambar 4.23 Hasil Pengujian Saat Tombol Dilepas

4.2.6 Lampu Indikator

4.2.6.1 Tujuan

Pengujian ini bertujuan untuk mengetahui tegangan logic dan tegangan led pada saat led hidup dan saat led mati.

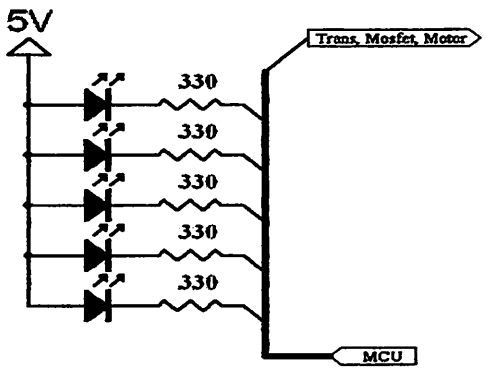
4.2.6.2 Peralatan Penunjang Pengujian

- Rangkaian Lampu Indikator seperti gambar 4.7
- AVO meter Digital
- Catu Daya 5 V

4.26.3 Langkah Pengujian

1. Sistem dirangkai pada gambar 4.7
2. Pada saat kondisi lampu led nyala ukur Volt-nya
3. Pada saat kondisi lampu led mati ukur Volt-nya

Gambar 4.25 menunjukkan Rangkaian Lampu Indikator



Gambar 4.24 Rangkaian Lampu Indikator

4.2.6.4 Hasil Pengujian

Pada saat led hidup tegangan-nya 1,96 V, tegangan logic 0,03 V dan logic-nya "0". Saat led mati tegangan-ny 0,2 V, tegangan logic 4,96 V dan logic-nya "1". Tabel 4.9 menunjukkan Hasil Pengukuran Rangkaian Lampu Indikator.

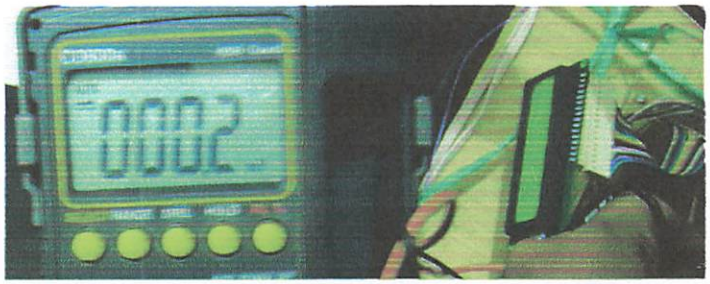
Tabel 4.8 Hasil Pengukuran Rangkaian Lampu Indikator

Logic	V logic	V led	Keterangan
0	0,03	1,96	Hidup
1	4,96	0,2	Mati

Gambar 4.26 menunjukkan pada saat lampu led hidup Volt yang masuk 1,96V.

Gambar 4.25 Hasil Pengujian Saat Lampu LED Hidup

Gambar 4.27 menunjukkan pada saat lampu led mati Volt yang masuk 0,2V.



Gambar 4.26 Hasil Pengujian Saat Lampu LED Mati

4.2.6.5 Analisa Perhitungan

Dari hasil pengujian diketahui bahwa V led 2,54 dan dari data referensi R = 0,33 KΩ, Maka dapat diketahui arus yang diterima untuk satu led :

$$1 \text{ led} = \frac{vled}{R}$$

$$= \frac{2{,}54}{0{,}33k\Omega}$$

$$= 7{,}5 \text{ mA}$$

4.2.7 Pengujian LM 555

4.2.7.1 Tujuan

Untuk mengetahui frekuensi yang keluar dari Pin 3 pada Ic LM 555

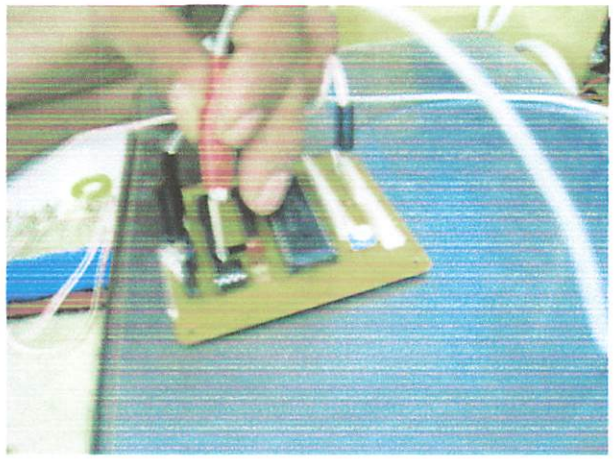
4.2.7.2 Peralatan yang digunakan

- Catu Daya 12V
- Osciloscop
- Rangkaian pada gambar 4. 1

4.2.7.3 Langkah Pengujian

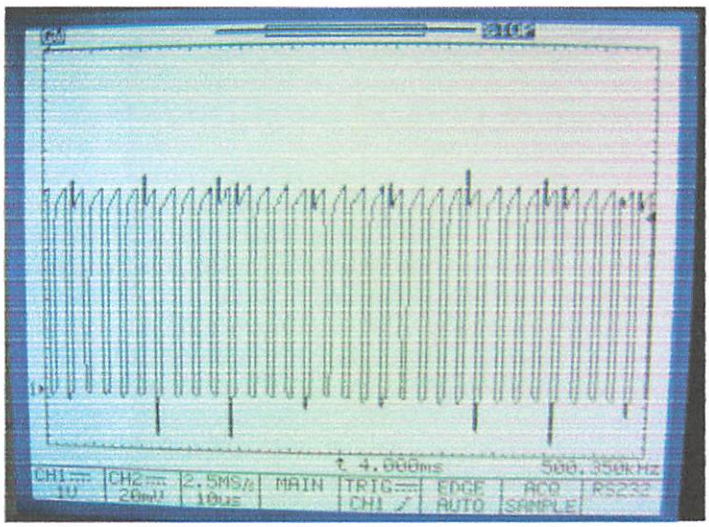
1. Hidupkan Catu Daya
2. Hubungkan catu daya 12 V pada rangkaian
3. Hubungkankan kabel Osciloskop pada rangkaian

Gambar 4.27 menunjukkan Rangkaian Ic LM 555



Gambar 4.27 Rangkaian Ic LM 555

Gambar 4.28 menunjukkan frekuensi yang keluar dari Ic LM 555



Gambar 4.28 Frekuensi Yang Keluar Dari Ic LM 555

$$^{v}/_{div} = 1 \text{ V}$$

$$^{T}/_{div} = 10 \ \mu \text{s}$$

BAB V

KESIMPULAN

5.1 Kesimpulan

Setelah melakukan pengujian dan pengukuran secara keseluruhan dapat disimpulkan :

1. Pada pengujian rangkaian driver motor pwm (Puls Width modulation) menghasilkan RPMmotor yang meningkat, pada saat PWM = 41% RPMmotor = 500 dan saat PWM = 95% RPMmotor = 1370.
2. Pada pengujian rangkaian driver motor dua arah on/off menghasilkan data pembacaan ADC 0808, sehingga posisi rantai berada pada gear yang sesuia urutan gear 1, gear 2, gear 3, gear 4, gear5 dan gear 6.
3. Pada pengujian Motor Gear Box 1 dapat diketahui RPMmaksimum dari motor pada tegangan maksimum 24 V adalah 3300 RPM.
4. Pada pengujian Motor Gear Box 2 dapat diketahui RPMmaksimum dari motor pada tegangan maksimum 24 V adalah 2800 RPM.
5. Pada pengujian Rangkaian Tombol Up dan Down dapat dikutahui pada saat tombol ditekan volt = 1,5 V dan logic = '0', saat tombol dilepas volt = 4,94 dan logic = '1'
6. Pada pengujian Rangkaian Lampu Indikator dapat diketahui pada saat lampu hidup V led = 1,94V dan logic = '0', saat lampu mati V led = 0,2V dan logic = '1'.

5.2 Saran

Pada alat pengontrol gokart ini motor gear box untuk PWM di sarankan yang lebih besar agar tenaga yang dihasilkan juga besar dan pada bagian AS roda belakang lebih baik menggunakan sistem differensial.

Differensial adalah dimana pada saat berbelok kekanan roda yang sebelah kiri akan berputar lebih cepat dari roda sebelah kanan dan sebaliknya saat berbelok kekiri roda yang sebelah kanan akan berputar lebih cepat dari roda sebelah kiri sehingga gokart dapat berbelok dengan baik tanpa ada ban yang tergelincir.

DAFTAR PUSTAKA

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LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

FORMULIR BIMBINGAN SKRIPSI

Nama : **HELDIN RAMBO SIAGIAN**
Nim : **04.12.246**
Masa Bimbingan : **15 AGUSTUS 2009 s/d 15 FEBRUARI 2010**
Judul Skripsi : **PERANCANGAN DAN PEMBUATAN PENGENDALI GOKART ELEKTRIK MENGGUNAKAN PWM BERBASISKAN MIKROKONTROLER**

NO	Tanggal	Uraian	Paraf Pembimbing
1	7/12 09	Bab I s/d III Perbaiki.	
2	15/12 09	Bab I s/d III Perbaiki.	
3	30/12 09	Bab I s/d III Perbaiki. Referensi dan daftar pustaka.	
4	9/1 2010	Bab III Revisi.	
5	19/1 2010	Bab IV diperbaiki.	
6			
7			
8			
9			
10			

Malang, 2010
Dosen Pembimbing,

Ir. F. Yudi Limpraptono, MT 1/6
Nip.Y.103 9500 274

Form.S-4b

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO
Jl. Karanglo KM.2 Malang

FORMULIR PERBAIKAN SKRIPSI

Nama : **HELDIN RAMBO SIAGIAN**
Nim : **04.12.246**
Jurusan : **Teknik Elektro S-1**
Konsentrasi : **Teknik Elektronika**
Judul Skripsi : **PERANCANGAN DAN PEMBUATAN PENGENDALI GOKART ELEKTRIK MENGGUNAKAN PWM BERBASISKAN MIKROKONTROLER**
Hari/Tanggal ujian Skripsi : **Kamis / 11 Februari 2010**

Penguji	Revisi	Paraf
Penguji 1	1. Daftar pustaka, pengantar pada gambar & tabel, revisi pengantar kalimat & gambar 2. Tabel hasil, datasheet, revisi gambar 3.8	
Penguji 2	1. Analisa + perhitungan LM 555, draiver pwm, driver motor 2 arah 2. Analisa ADC s/d sinyal PWM, tabel 4.1	

Disetujui

Penguji 1

M. Ibrahim Ashari ST, MT
NIP.Y.103.010.0358

Penguji 2

Sotyohadi ST, Msc
NIP.P.103.970.0309

Mengetahui

Dosen Pembimbing

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INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika / T.Infokom, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Haldin Rambo S
NIM : 0412246
Perbaikan meliputi :

1. Daftar pustaka utuk abstrak.
2. Tambahkan pengantar pd gbr dan tabel.
3. Revisi antara pengantar terhadap dgn gbr.
4. penulisan tabel benar.
5. Data sheet dilampirkan
6. gbr 3.8 direvisi

Malang, 20 Juli '10

(M. Ibrahim Ashari ST MT

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

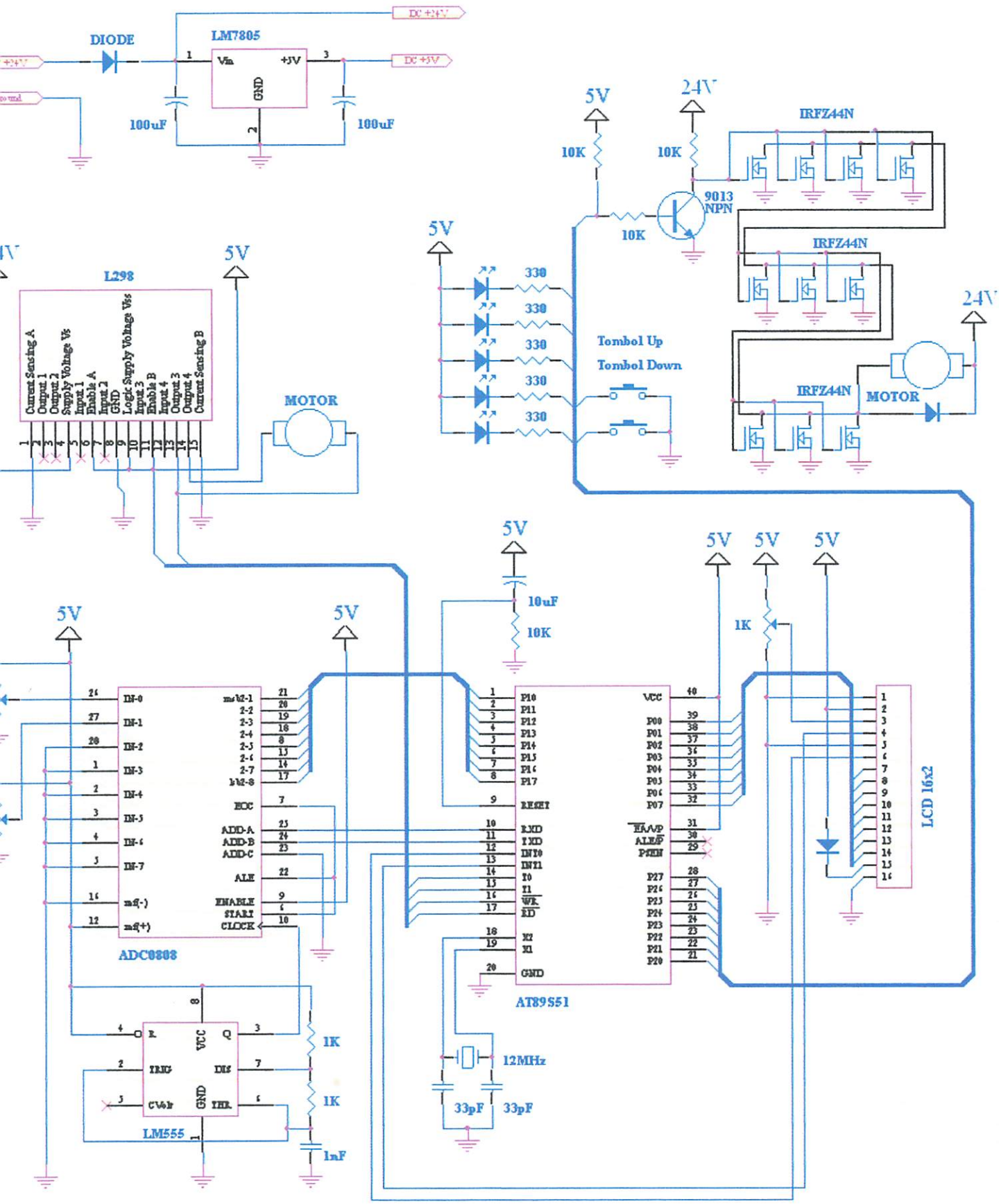
Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika / T.Infokom, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Heldin
NIM : 04.12.246
Perbaikan meliputi :

1). Analisa + Perhitungan. LM 555 Rangk. Clock.
2). Analisa + Perhitungan. Driver Motor PWM.
3). Analisa + Perhitungan. Driver Motor 2 Arah.
4). Analisa keria. & input dr ADC sampai dgn mengeluarkan sinyal PWM.
5). Hasil pengujian driver motor PWM ~~dst~~. tabel 4.1 Diperbaiki hasil perhitungannya.

Malang, 20/2 '10

(_____)
SOTEDHADI, ST


DIODE
LM7805
Vin
+5V
GND
100uF
100uF
DC +24V
DC +5V
5V
24V
10K
10K
10K
9013
NPN
IRFZ44N
IRFZ44N
IRFZ44N
MOTOR
330
330
330
330
330
Tombol Up
Tombol Down
L298
Current Sensing A
Output 1
Output 2
Supply Voltage Vs
Input 1
Enable A
Input 2
GND
Logic Supply Voltage Vss
Input 3
Enable B
Input 4
Output 3
Output 4
Current Sensing B
MOTOR
10uF
10K
1K
ADC0808
AT89S51
12MHz
33pF
33pF
LM555
1K
1K
1nF
LCD 16x2

Features

- Compatible with MCS-51® Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)

Description

The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

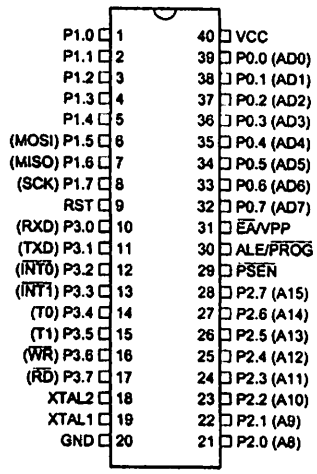
8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

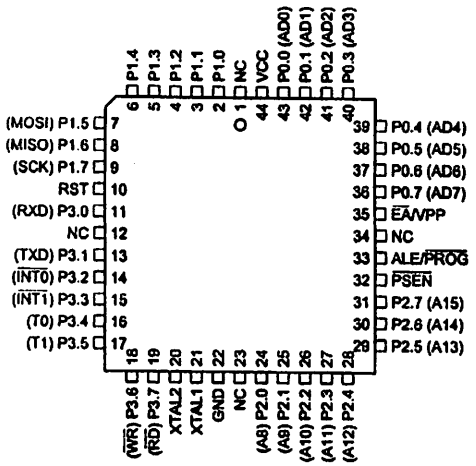
Rev. 2487A–10/01

Pin Configurations

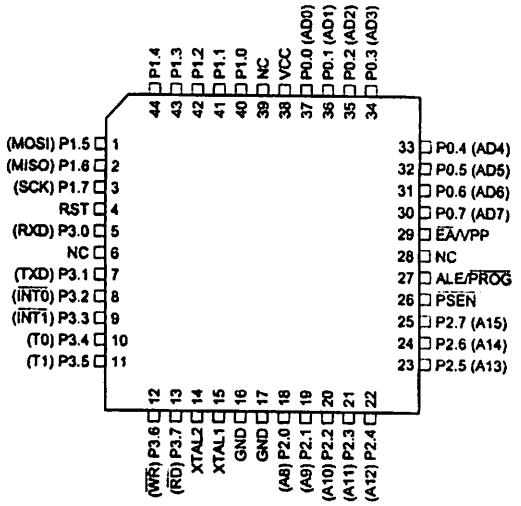
PDIP



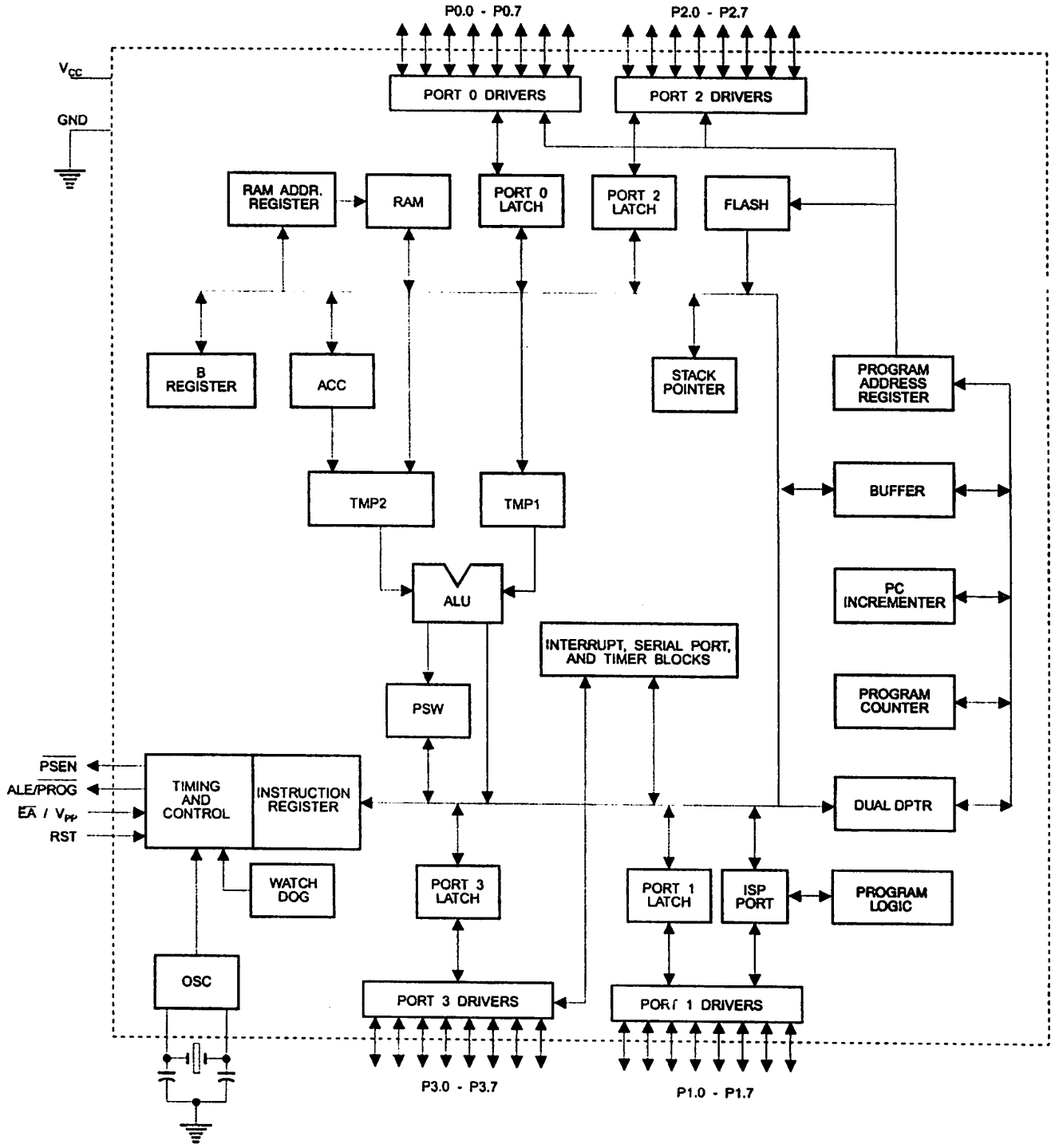
PLCC



TQFP



Block Diagram



Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 1. AT89S51 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H									0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1

Address = A2H

Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Data Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle

Table 4. Interrupt Enable (IE) Register

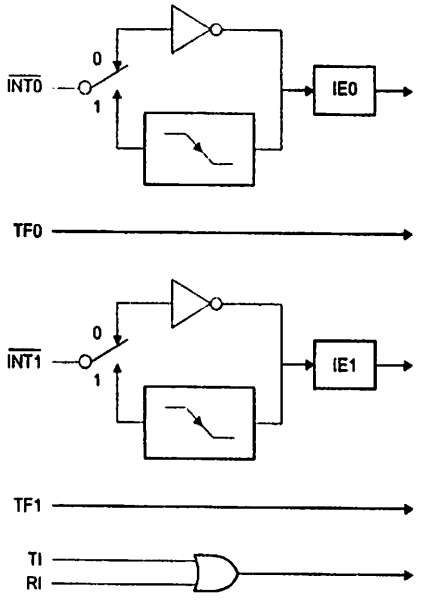
(MSB)							(LSB)
EA	–	–	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. if EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved
–	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

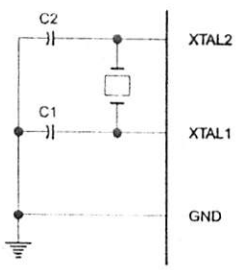
Figure 1. Interrupt Sources



Oscillator Characteristics

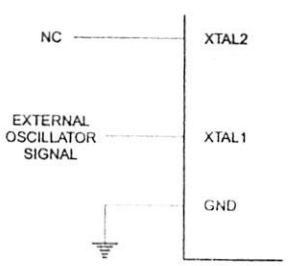
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into $\overline{INT0}$ or $\overline{INT1}$. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Programming the Flash – Parallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

Serial Programming Algorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 7. Flash Programming Modes

Mode	V_{CC}	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0 Address	P1.7-0 Address
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A11-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A11-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

Notes:
1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/BSY signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

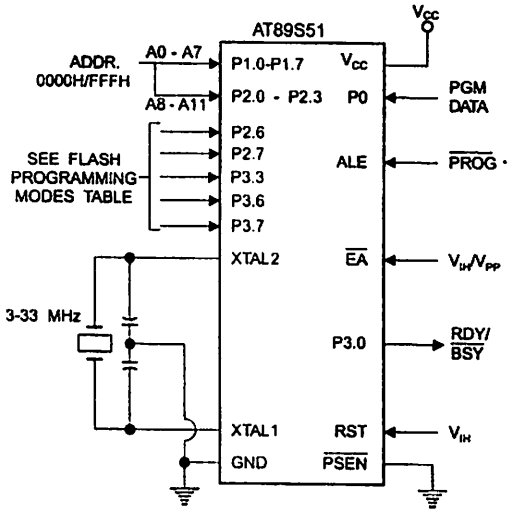
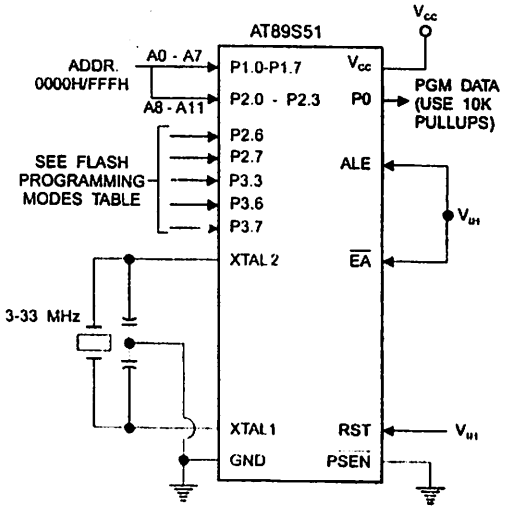


Figure 5. Verifying the Flash Memory (Parallel Mode)



Flash Programming and Verification Characteristics (Parallel Mode)

T_A = 20°C to 30°C, V_{CC} = 4.5 to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	0.2	1	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		50	µs

Figure 6. Flash Programming and Verification Waveforms – Parallel Mode

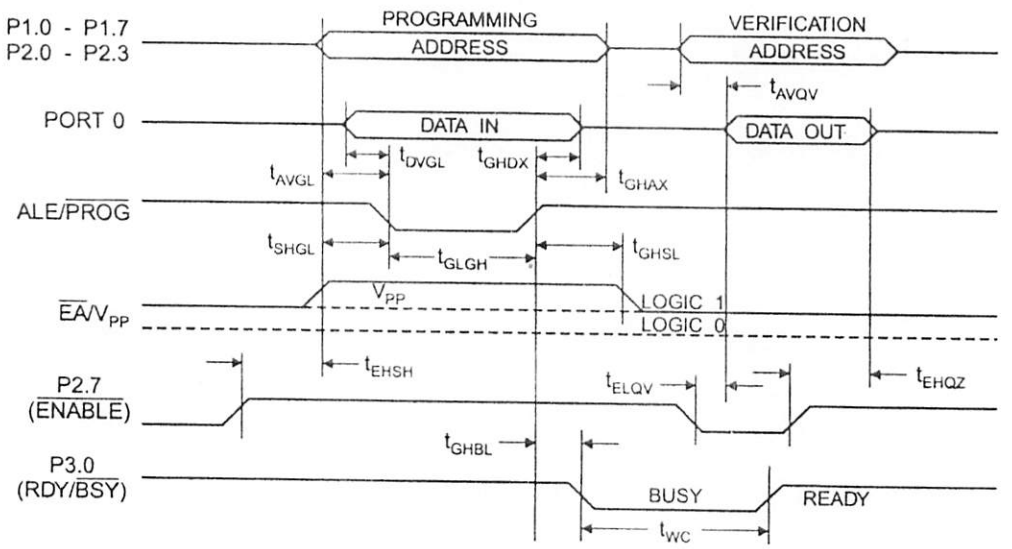
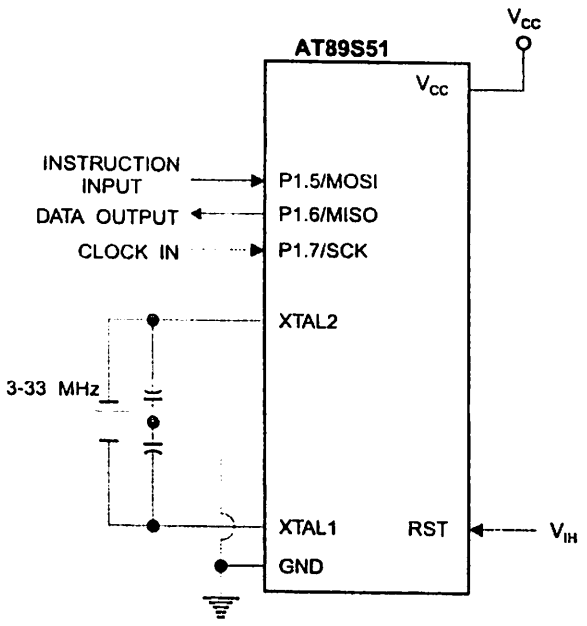


Figure 7. Flash Memory Serial Downloading



Flash Programming and Verification Waveforms – Serial Mode

Figure 8. Serial Programming Waveforms

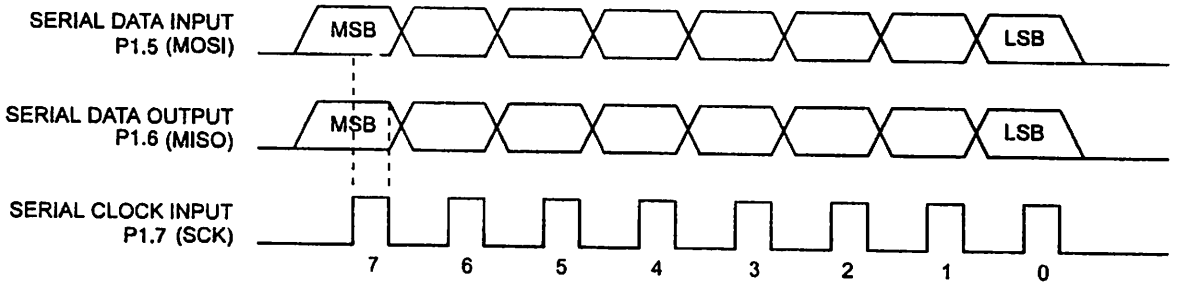


Table 8. Serial Programming Instruction Set

Instruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Write Lock Bits[2]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Read Signature Bytes[1]	0010 1000	xxx A5 A4 A3 A2 A1	A0 xxx xxxx	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Notes: 1. The signature bytes are not readable in Lock Bit Modes 3 and 4.

2. B1 = 0, B2 = 0 → Mode 1, no lock protection
   B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
   B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
   B1 = 1, B1 = 1 → Mode 4, lock bit 3 activated

   } Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Serial Programming Characteristics

Figure 9. Serial Programming Timing

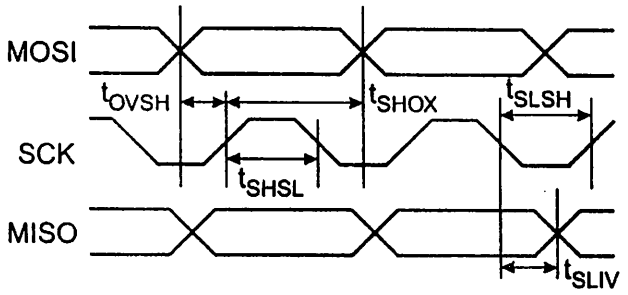


Table 9. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	8 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	8 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

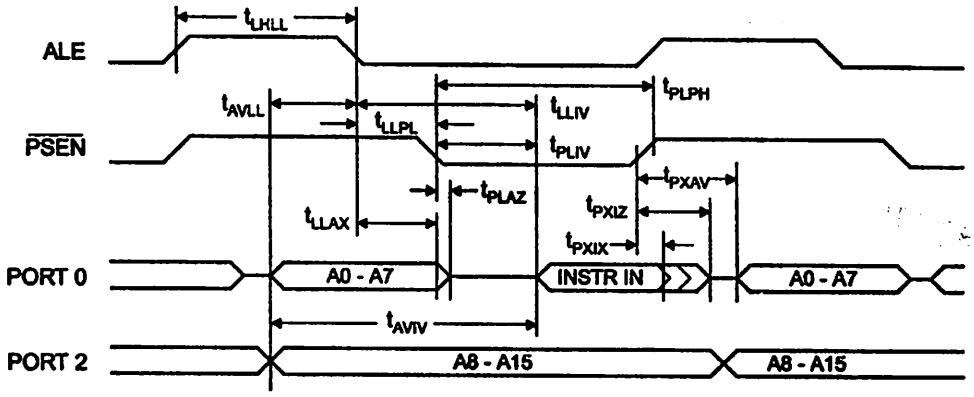
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

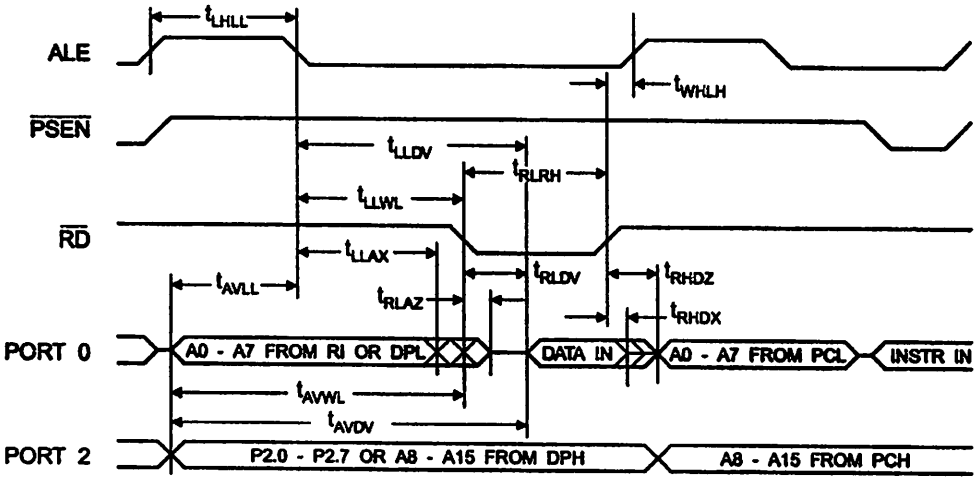
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-25		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-25		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

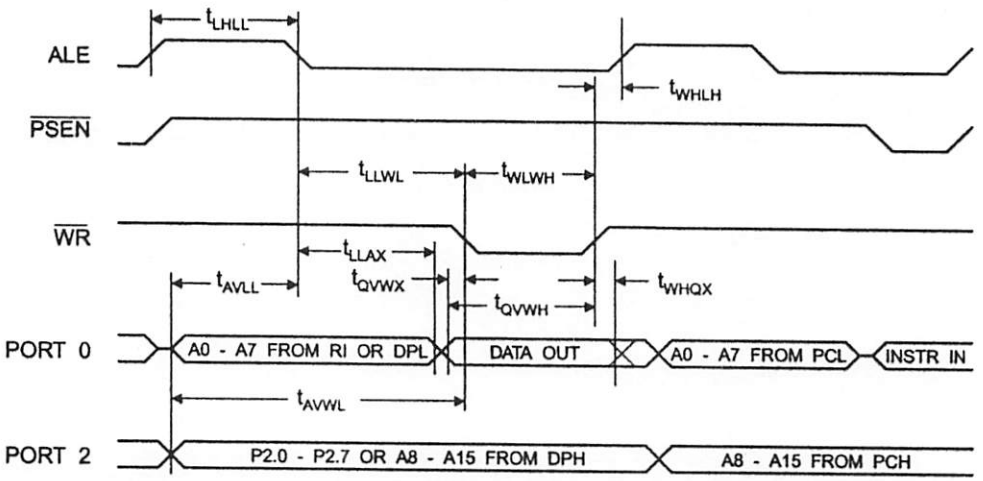
External Program Memory Read Cycle



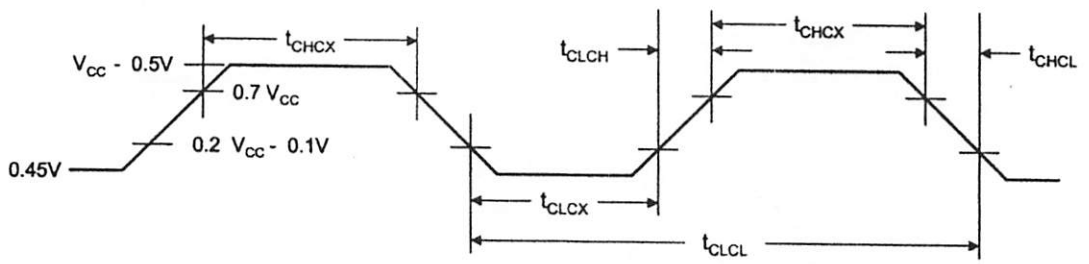
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

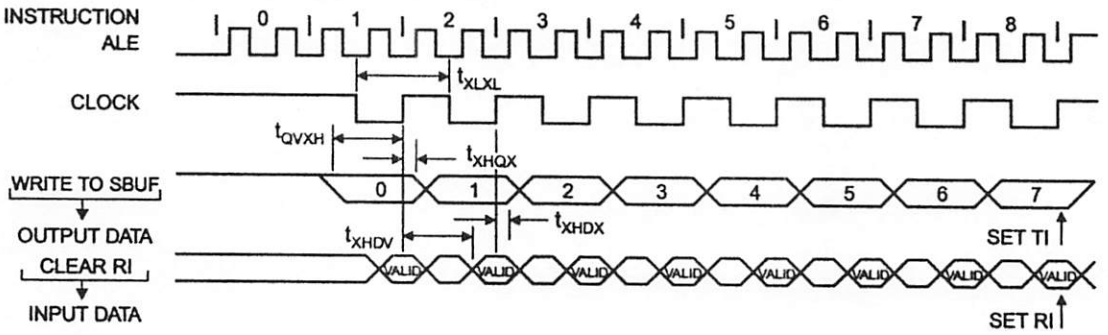
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	33	MHz
t_{CLCL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

Serial Port Timing: Shift Register Mode Test Conditions

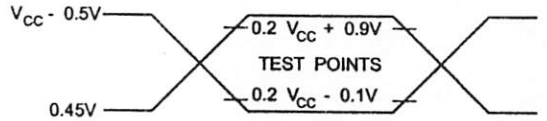
The values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

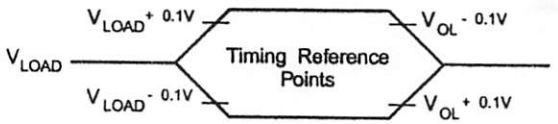


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

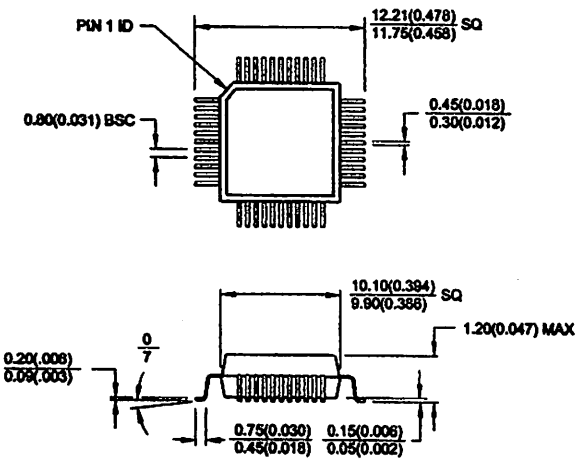
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S51-24AC AT89S51-24JC AT89S51-24PC	44A 44J 40P6	Commercial (0°C to 70°C)
		AT89S51-24AI AT89S51-24JI AT89S51-24PI	44A 44J 40P6	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S51-33AC AT89S51-33JC AT89S51-33PC	44A 44J 40P6	Commercial (0°C to 70°C)

[ ] = Preliminary Availability

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

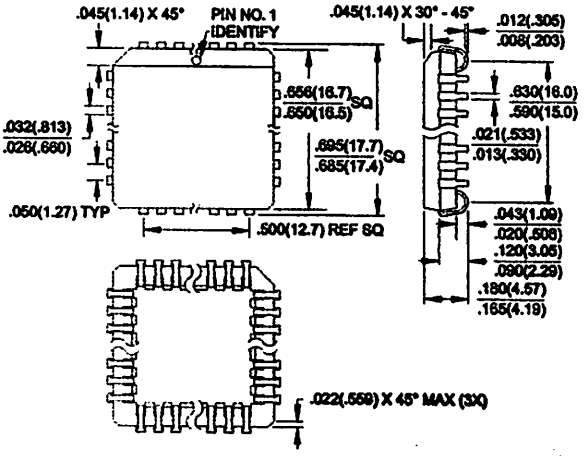
Packaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*

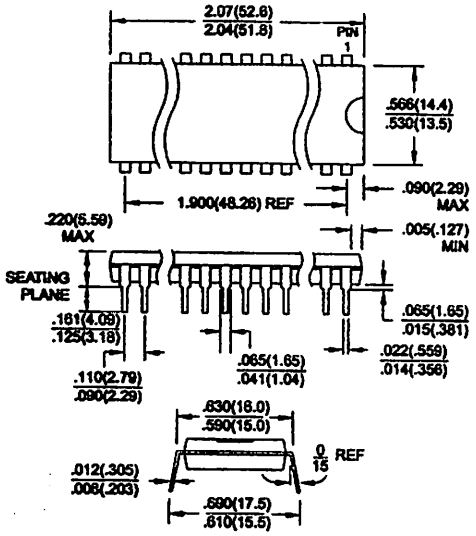


*Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



40P6, 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AC



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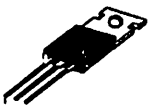
2487A–10/01/xM

LM78XX (KA78XX, MC78XX) FIXED VOLTAGE REGULATOR (POSITIVE)

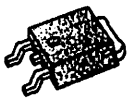
3-TERMINAL 1A POSITIVE VOLTAGE REGULATORS

The LM78XX series of three-terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

TO-220



D-PAK



1: Input 2: GND 3: Output

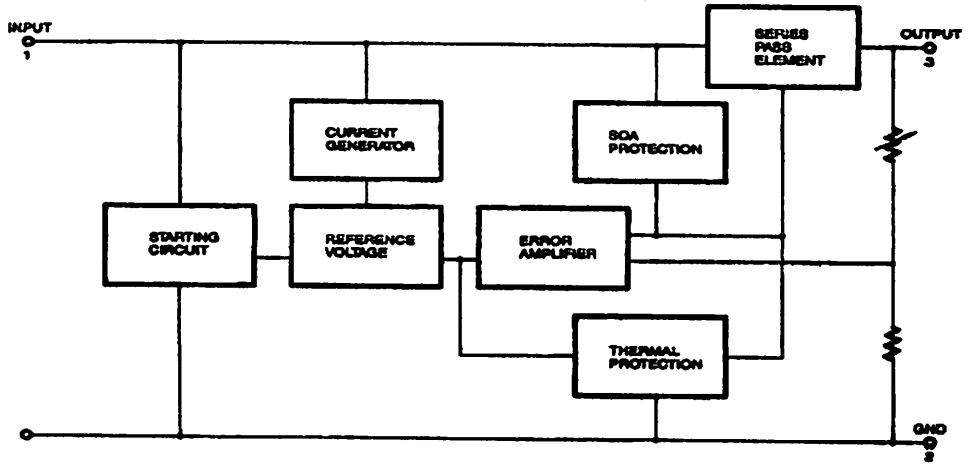
FEATURES

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 11, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor SOA Protection

ORDERING INFORMATION

Device	Output Voltage Tolerance	Packag	Operating Temperature
KA78XXCT	±4%	TO-220	0 ~ +125°C
KA78XXAT	±2%		
KA78XXIT	±4%		-40 ~ +125°C
KA78XXR		D-PAK	0 ~ +125°C
KA78XXAR	±2%		
KA78XXIR	±4%		-40 ~ +125°C

BLOCK DIAGRAM



FAIRCHILD SEMICONDUCTOR TM

Rev. B

LM78XX (KA78XX, MC78XX) FIXED VOLTAGE REGULATOR (POSITIVE)

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V) (for V_O = 24V)	V_I V_I	35 40	V V
Thermal Resistance Junction-Cases	$R_{\theta JC}$	5	°C/W
Thermal Resistance Junction-Air	$R_{\theta JA}$	65	°C/W
Operating Temperature Range KA78XX/A/R/RA KA78XXI/RI	T_{OPR}	0 ~ +125 -40 ~ +125	°C °C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

LM7805/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit, $T_{MIN} < T_J < T_{MAX}$, I_O = 500mA, V_I = 10V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM7805I			LM7805			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	T_J =+25°C		4.8	5.0	5.2	4.8	5.0	5.2	V
		5.0mA ≤ I_O ≤1.0A, P_O ≤ 15W V_I = 7V to 20V V_I = 8V to 20V		4.75	5.0	5.25	4.75	5.0	5.25	
Line Regulation	ΔV_O	T_J=+25°C	V_O = 7V to 25V		4.0	100		4.0	100	mV
			V_I = 8V to 12V		1.6	50		1.6	50	
Load Regulation	ΔV_O	T_J=+25°C	I_O = 5.0mA to1.5A		9	100		9	100	mV
			I_O =250mA to 750mA		4	50		4	50	
Quiescent Current	I_Q	T_J =+25°C			5.0	8		5.0	8	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A			0.03	0.5		0.03	0.5	mA
		V_I= 7V to 25V						0.3	1.3	
		V_I= 8V to 25V			0.3	1.3				
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O= 5mA			-0.8			-0.8		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100Khz, T_A=+25°C			42			42		μV/Vo
Ripple Rejection	RR	f = 120Hz V_O = 8 to 18V		62	73		62	73		dB
Dropout Voltage	V_O	I_O = 1A, T_J =+25°C			2			2		V
Output Resistance	R_O	f = 1KHz			15			15		mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A =+25°C			230			230		mA
Peak Current	I_{PK}	T_J =+25°C			2.2			2.2		A

* $T_{MIN} < T_J < T_{MAX}$
  LM78XXI/RI: T_{MIN}= - 40°C, T_{MAX} = +125°C
  LM78XX/R: T_{MIN}= 0°C, T_{MAX}= +125°C
* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 Quiescent Current

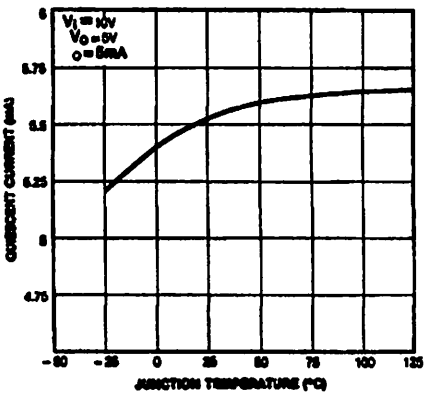


Fig. 2 Peak Output Current

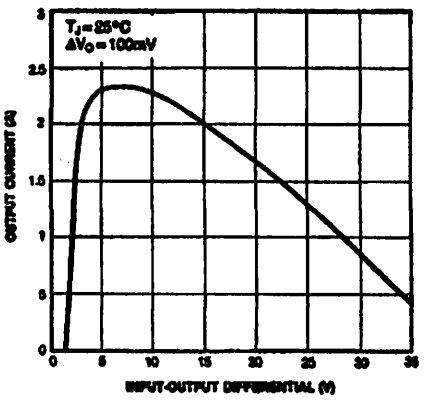


Fig. 3 Output Voltage

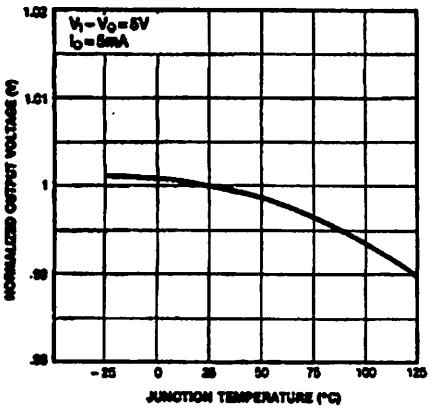
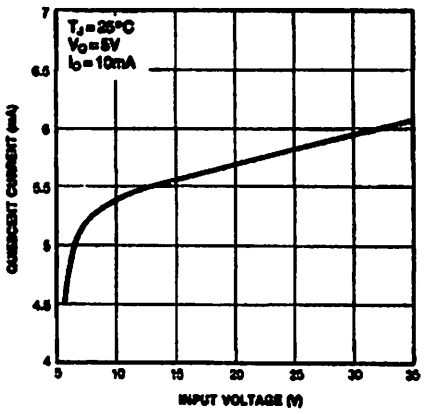


Fig. 4 Quiescent Current



TYPICAL APPLICATIONS

Fig. 5 DC Parameters

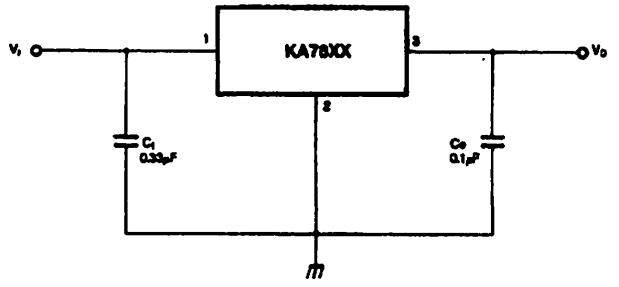


Fig. 6 Load Regulation

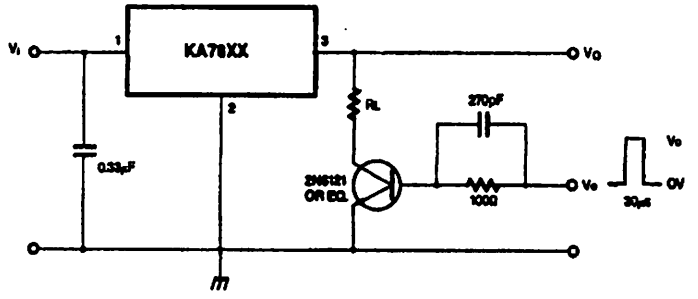
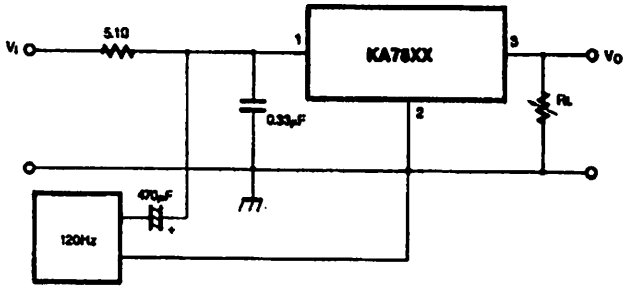


Fig. 7 Ripple Rejection



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TYPICAL APPLICATIONS (Continued)

Fig. 8 Fixed Output Regulator

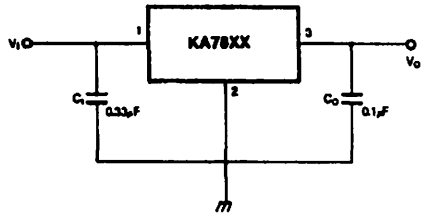
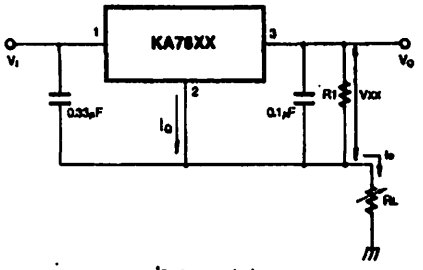


Fig. 9 Constant Current Regulator



$$I_o = \frac{}{R1} + I_Q$$

Notes:

(1) To specify an output voltage, substitute voltage value for "XX." A common ground is required between the input and the Output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.

(2) C_I is required if regulator is located an appreciable distance from power Supply filter.

(3) C_O improves stability and transient response.

Fig. 10 Circuit for Increasing Output Voltage

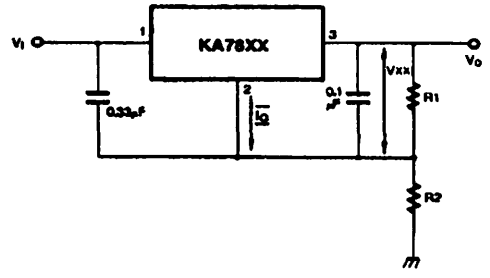
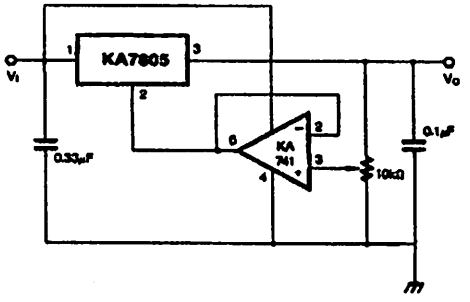


Fig. 11 Adjustable Output Regulator (7 to 30V)



$I_{R1} \geq 5\ I_Q$

$V_O = V_{XX}(1+R_2/R_1)+I_QR_2$

TYPICAL APPLICATIONS (Continued)

Fig. 12 High Current Voltage Regulator

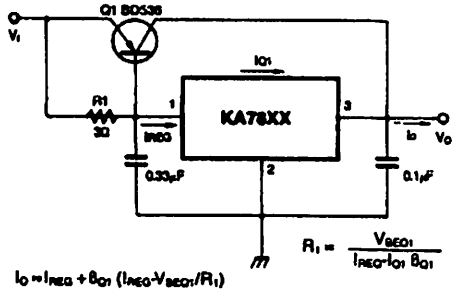


Fig. 13 High Output Current with Short Circuit Protection

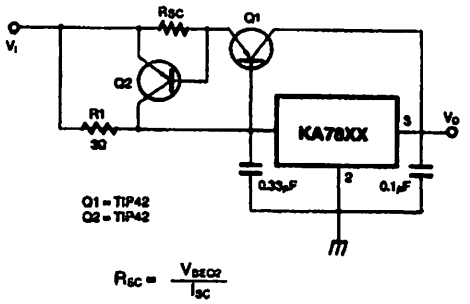


Fig. 14 Tracking Voltage Regulator

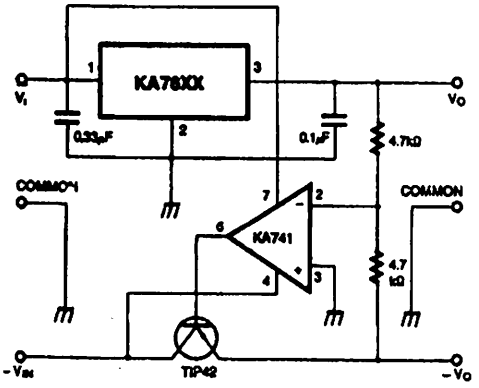
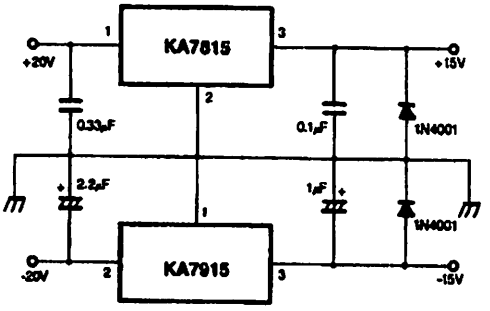


Fig. 15 Split Power Supply (±15V-1A)



TYPICAL APPLICATIONS (Continued)

Fig. 16 Negative Output Voltage Circuit

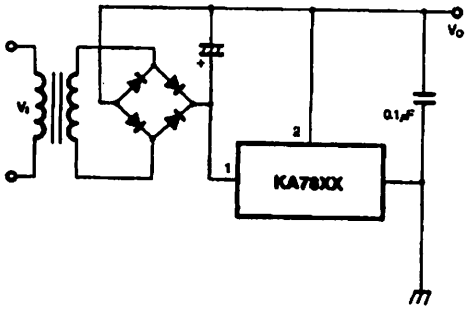
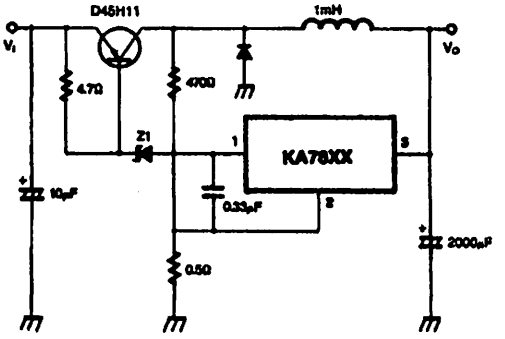


Fig. 17 switching Regulator



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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

National Semiconductor

February 1995

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

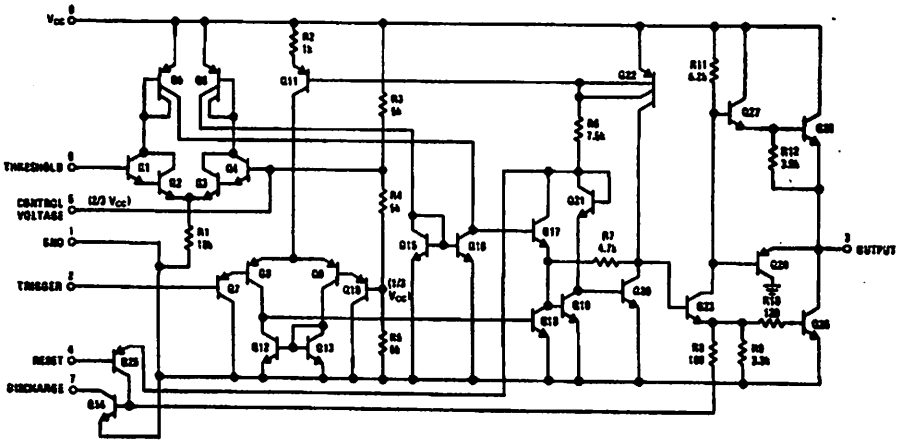
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



TL/H/7851–1

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 1)	
LM555H, LM555CH	760 mW
LM555, LM555CN	1180 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
LM555	−55°C to + 125°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Package	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		3 10	5 12		3 10	6 15	mA mA
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V V_{CC} = 5V	4.8 1.45	5 1.67	5.2 1.9		5 1.67		V V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V V_{CC} = 5V	9.6 2.9	10 3.33	10.4 3.8	9 2.6	10 3.33	11 4	V V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV

Electrical Characteristics T_A = 25°C, V_{CC} = +5V to +15V, (unless otherwise specified) (Continued)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 164°C/W (TO-5), 106°C/W (DIP) and 170°C/W (SO-8) junction to ambient.

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

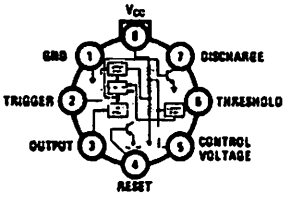
Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 6: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Connection Diagrams

Metal Can Package



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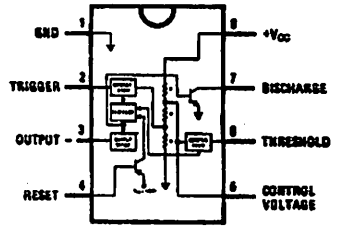
Top View

Order Number LM555H or LM555CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



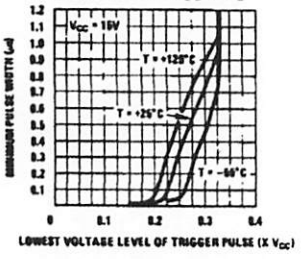
TL/H/7851–3

Top View

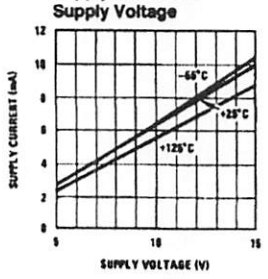
Order Number LM555J, LM555CJ, LM555CM or LM555CN
See NS Package Number J08A, M08A or N08E

Typical Performance Characteristics

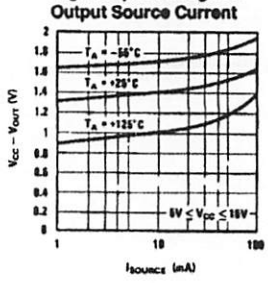
Minimum Pulse Width Required for Triggering



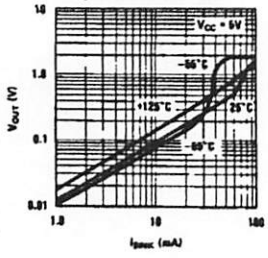
Supply Current vs Supply Voltage



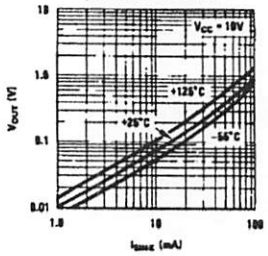
High Output Voltage vs Output Source Current



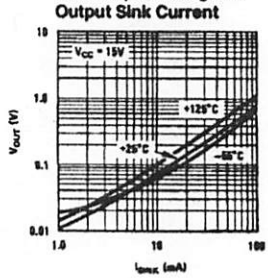
Low Output Voltage vs Output Sink Current



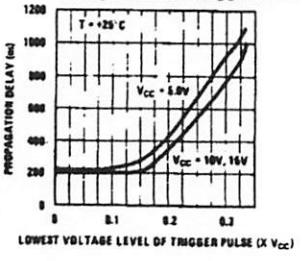
Low Output Voltage vs Output Sink Current



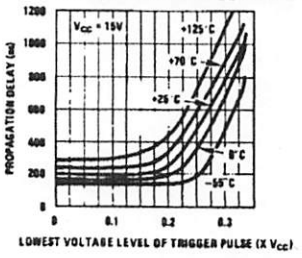
Low Output Voltage vs Output Sink Current



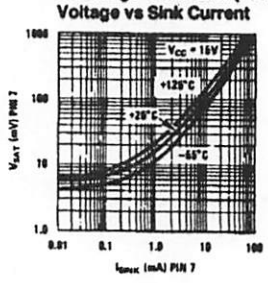
Output Propagation Delay vs Voltage Level of Trigger Pulse



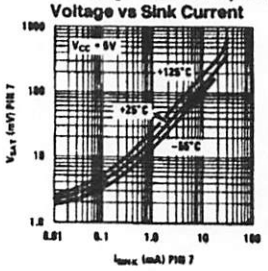
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs Sink Current



Discharge Transistor (Pin 7) Voltage vs Sink Current



TL/H/7851–4

Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot *(Figure 1)*. The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

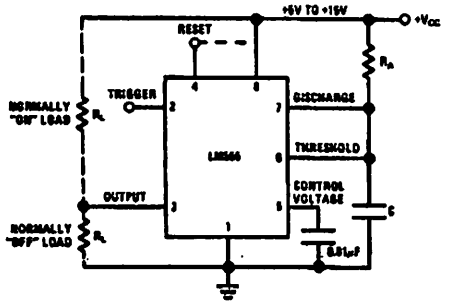


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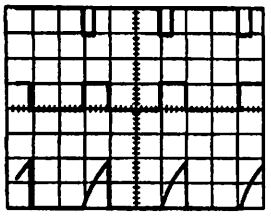
FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A\ C$, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



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V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 9.1 kΩ
C = 0.01 µF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

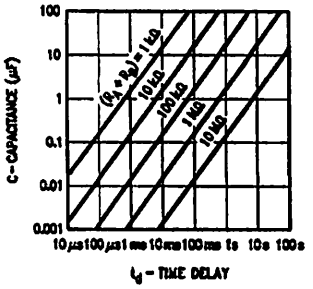
FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10 µs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

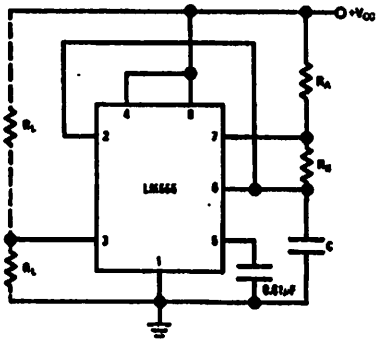


TL/H/7851–7

FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.



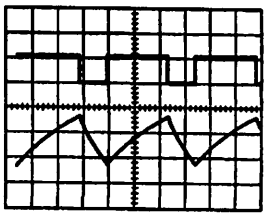
TL/H/7851–8

FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



TL/H/7851–9

V_{CC} = 5V
TIME = 20 µs/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 µF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693 (R_A + R_B) C$$

And the discharge time (output low) by:

$$t_2 = 0.693 (R_B) C$$

Thus the total period is:

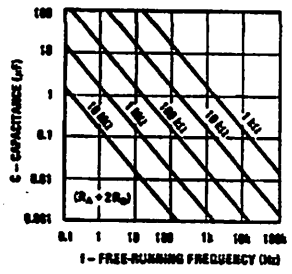
$$T = t_1 + t_2 = 0.693 (R_A + 2R_B) C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is: $D = \frac{R_B}{R_A + 2R_B}$

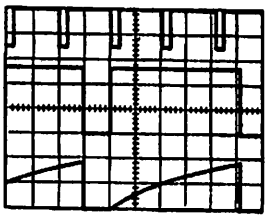


TL/H/7851–10

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



TL/H/7851–11

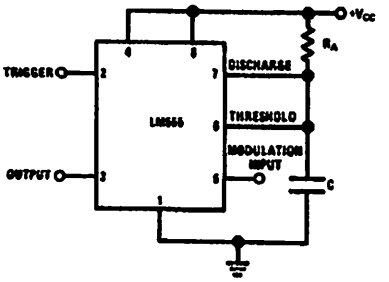
V_{CC} = 5V
TIME = 20 µs/DIV.
R_A = 9.1 kΩ
C = 0.01 µF

Top Trace: Input 4V/Div.
Middle Trace: Output 2V/Div.
Bottom Trace: Capacitor 2V/Div.

FIGURE 7. Frequency Divider

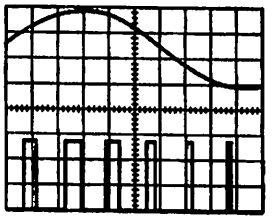
PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.



TL/H/7851–12

FIGURE 8. Pulse Width Modulator



TL/H/7851–13

V_{CC} = 5V
TIME = 0.2 ms/DIV.
R_A = 9.1 kΩ
C = 0.01 µF

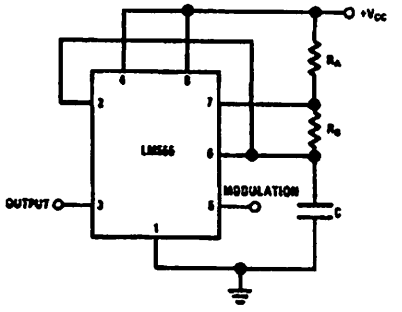
Top Trace: Modulation 1V/Div.
Bottom Trace: Output Voltage 2V/Div.

FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

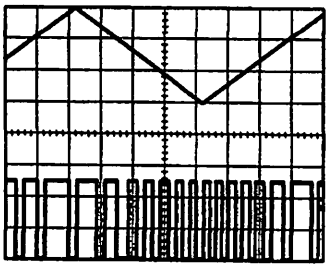
This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

Applications Information (Continued)



TL/H/7851–14

FIGURE 10. Pulse Position Modulator



TL/H/7851–15

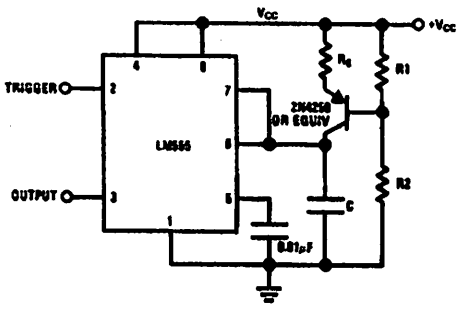
V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output 2V/Div.

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.



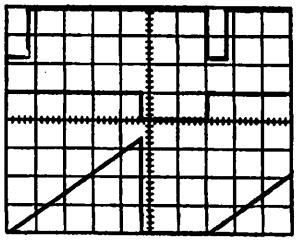
TL/H/7851–16

FIGURE 12

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$



TL/H/7851–17

V_{CC} = 5V
TIME = 20 μs/DIV.
R_1 = 47 kΩ
R_2 = 100 kΩ
R_E = 2.7 kΩ
C = 0.01 μF

Top Trace: Input 3V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

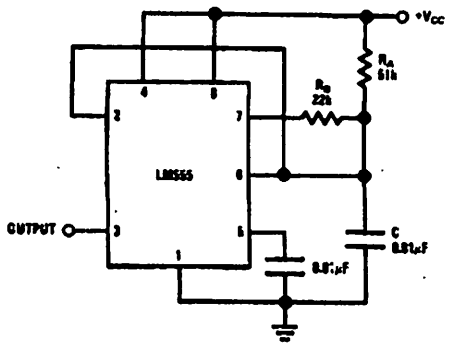
For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the out-

Applications Information (Continued)

put high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ ln\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$



TL/H/7851–16

FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

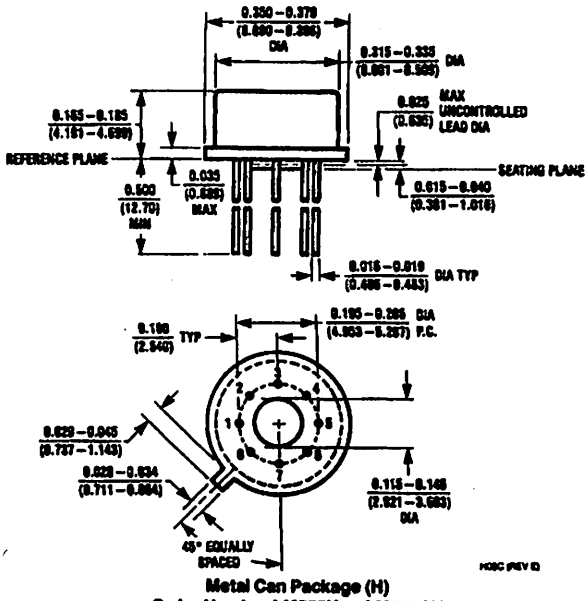
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1 μF in parallel with 1 μF electrolytic.

Lower comparator storage time can be as long as 10 μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10 μs minimum.

Delay time reset to output is 0.47 μs typical. Minimum reset pulse width must be 0.3 μs, typical.

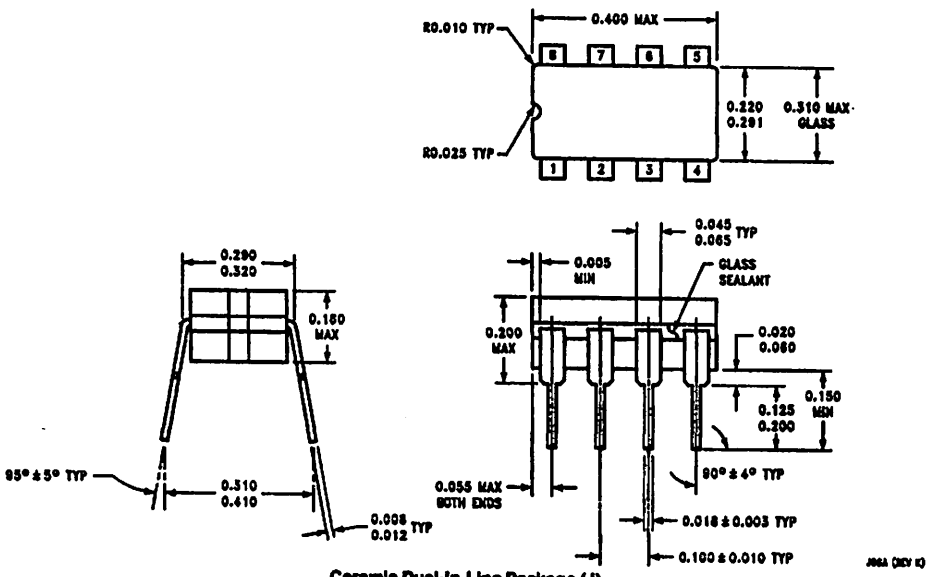
Pin 7 current switches within 30 ns of the output (pin 3) voltage.

Physical Dimensions inches (millimeters)

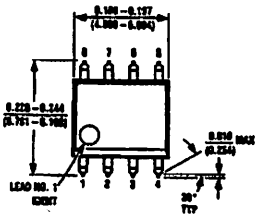


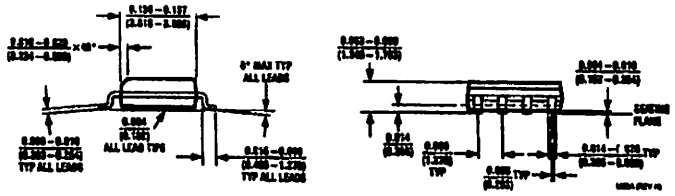
Metal Can Package (H)
Order Number LM555H or LM555CH
NS Package Number H08C

Physical Dimensions inches (millimeters) (Continued)



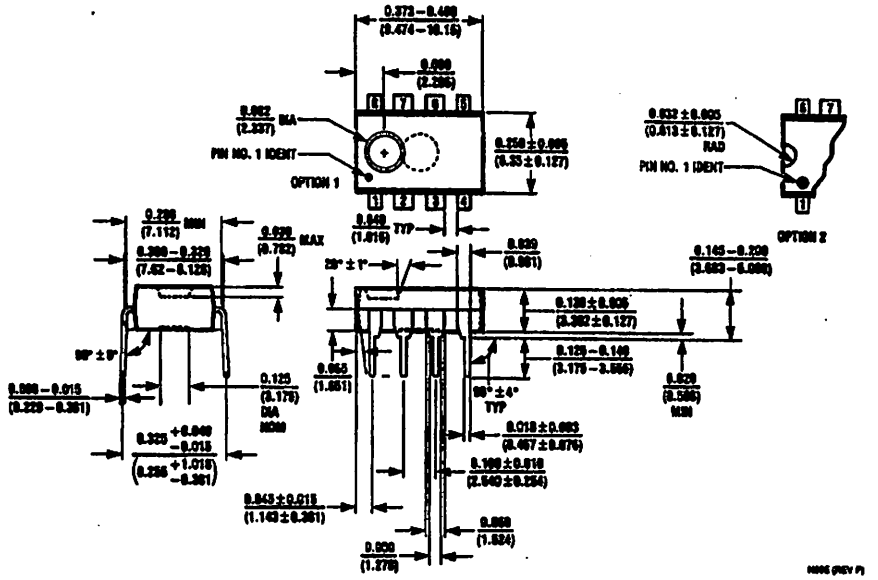
Ceramic Dual-In-Line Package (J)
Order Number LM556J or LM555CJ
NS Package Number J08A





Small Outline Package (M)
Order Number LM555CM
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LM555CN
NS Package Number N08E

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SS9013

1W Output Amplifier of Potable Radios in Class B Push-pull Operation.

- High total power dissipation. (P_T=625mW)
- High Collector Current. (I_C=500mA)
- Complementary to SS9012
- Excellent h_{FE} linearity.

TO-92

1. Emitter 2. Base 3. Collector

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{CBO}	Collector-Base Voltage	40	V
V_{CEO}	Collector-Emitter Voltage	20	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current	500	mA
P_C	Collector Power Dissipation	625	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C=100μA, I_E=0	40			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C=1mA, I_B=0	20			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E=100μA, I_C=0	5			V
I_{CBO}	Collector Cut-off Current	V_{CB}=25V, I_E=0			100	nA
I_{EBO}	Emitter Cut-off Current	V_{EB}=3V, I_C=0			100	nA
h_{FE1} h_{FE2}	DC Current Gain	V_{CE}=1V, I_C=50mA V_{CE}=1V, I_C=500mA	64 40	120 120	202	
V_{CE} (sat)	Collector-Emitter Saturation Voltage	I_C=500mA, I_B=50mA		0.16	0.6	V
V_{BE} (sat)	Base-Emitter Saturation Voltage	I_C=500mA, I_B=50mA		0.91	1.2	V
V_{BE} (on)	Base-Emitter On Voltage	V_{CE}=1V, I_C=10mA	0.6	0.67	0.7	V

h_{FE} Classification

Classification	D	E	F	G	H
h_{FE1}	64 ~ 91	78 ~ 112	96 ~ 135	112 ~ 166	144 ~ 202

Typical Characteristics

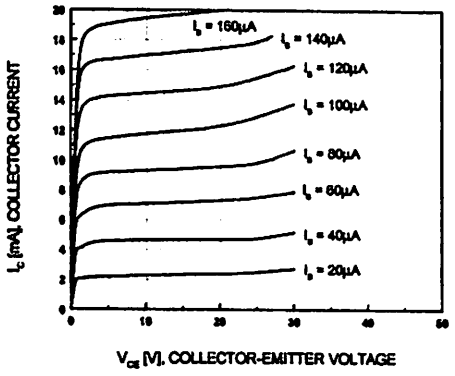


Figure 1. Static Characteristic

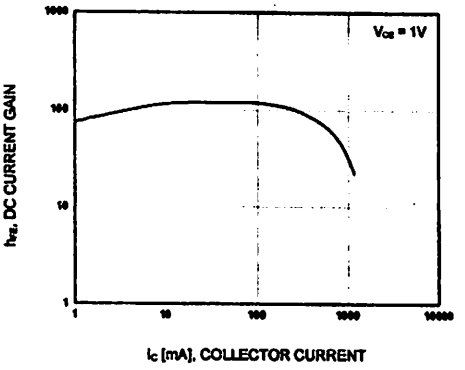


Figure 2. DC current Gain

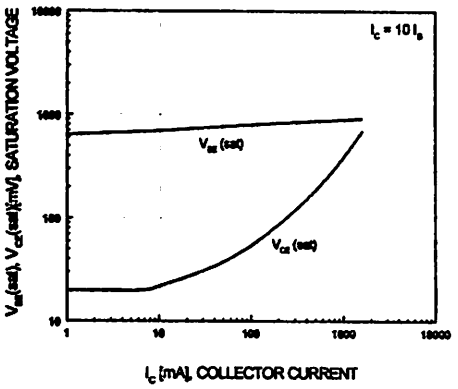


Figure 3. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

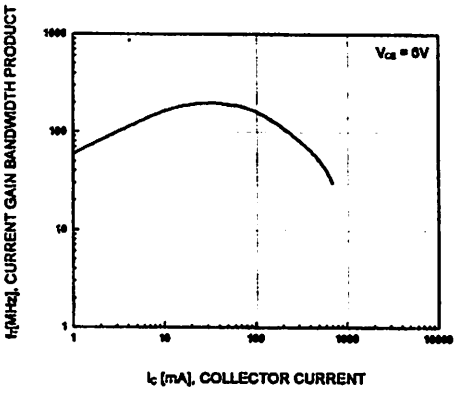
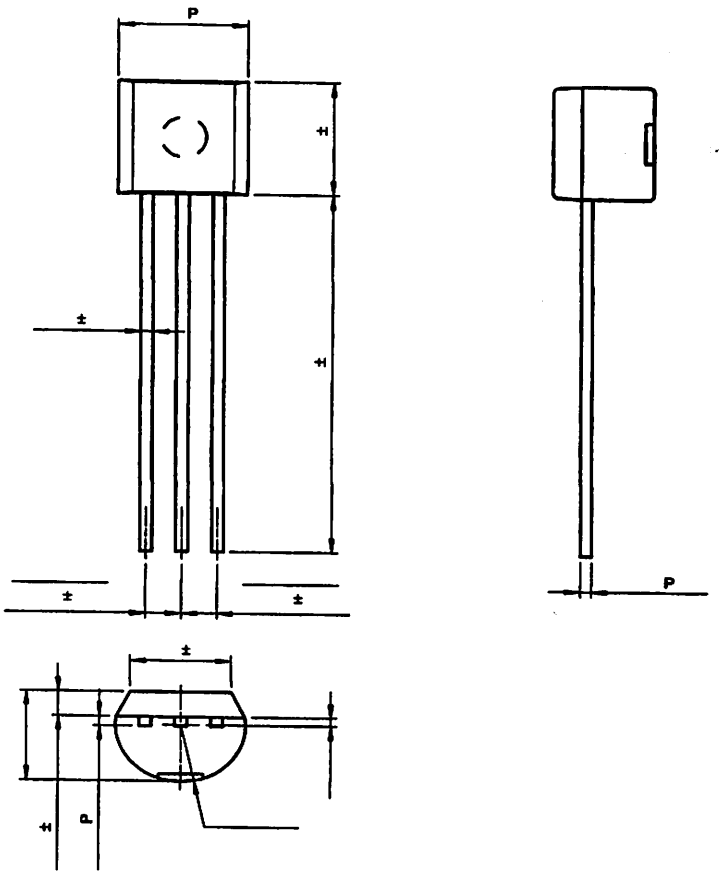


Figure 4. Current Gain Bandwidth Product

Package Dimensions

TO-92



Dimensions in Millimeters

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CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic™
E²CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	I²C™	OCX™	RapidConfigure™	UHC™
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The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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PD - 94053

IRFZ44N

HEXFET® Power MOSFET

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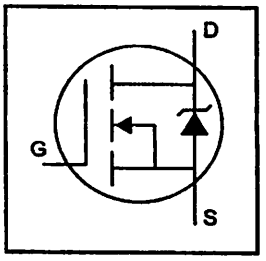
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 55V

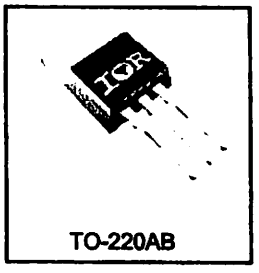
$R_{DS(on)}$ = 17.5mΩ

I_D = 49A

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	49	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	35	
I_{DM}	Pulsed Drain Current ①	160	
P_D @T_C = 25°C	Power Dissipation	94	W
	Linear Derating Factor	0.63	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current①	25	A
E_{AR}	Repetitive Avalanche Energy①	9.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.5	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.058	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	17.5	mΩ	V_{GS} = 10V, I_D = 25A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	19	—	—	S	V_{DS} = 25V, I_D = 25A④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	63	nC	I_D = 25A
Q_{gs}	Gate-to-Source Charge	—	—	14		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	23		V_{GS} = 10V, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	V_{DD} = 28V
t_r	Rise Time	—	60	—		I_D = 25A
$t_{d(off)}$	Turn-Off Delay Time	—	44	—		R_G = 12Ω
t_f	Fall Time	—	45	—		V_{GS} = 10V, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1470	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	360	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	88	—		f = 1.0MHz, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy②	—	530⑤	150⑥	mJ	I_{AS} = 25A, L = 0.47mH

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	49	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	—	—	160		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 25A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	63	95	ns	T_J = 25°C, I_F = 25A
Q_{rr}	Reverse Recovery Charge	—	170	260	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 0.48mH R_G = 25Ω, I_{AS} = 25A. (See Figure 12)

③ I_{SD} ≤ 25A, di/dt ≤ 230A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ This is a typical value at device destruction and represents operation outside rated limits.

⑥ This is a calculated value limited to T_J = 175°C .

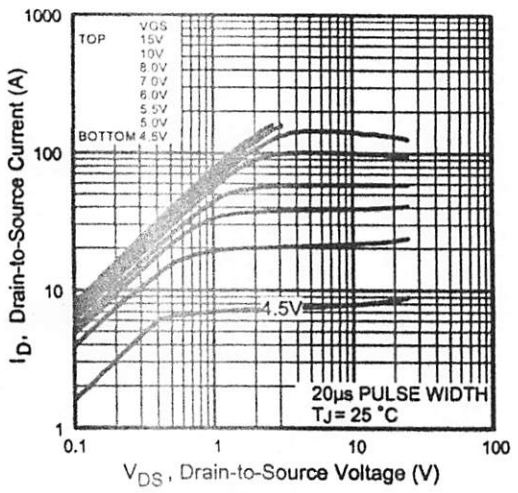


Fig 1. Typical Output Characteristics

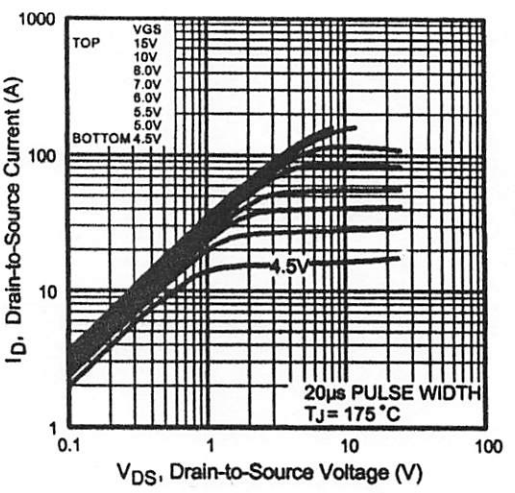


Fig 2. Typical Output Characteristics

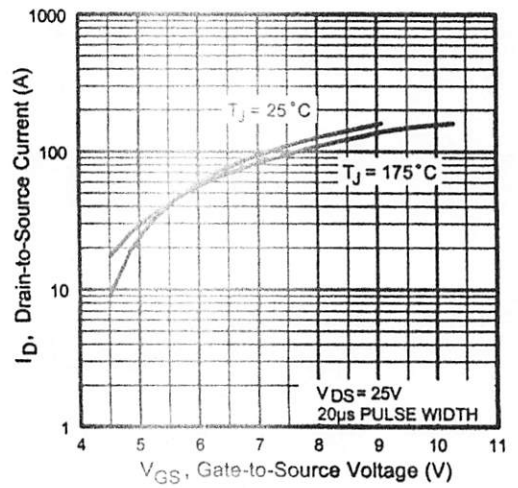


Fig 3. Typical Transfer Characteristics

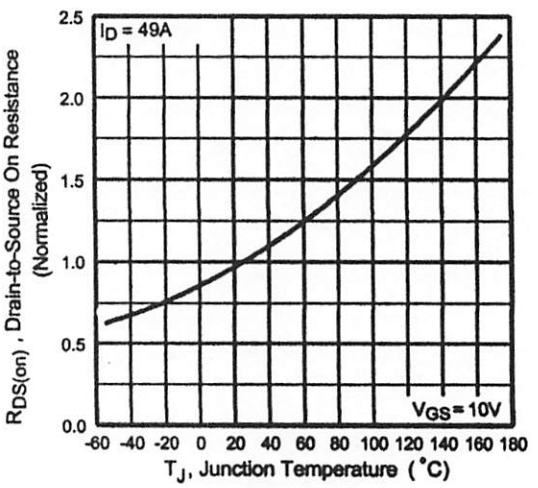


Fig 4. Normalized On-Resistance Vs. Temperature

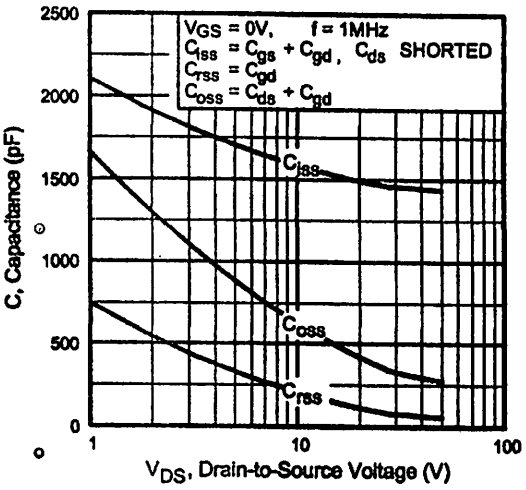


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

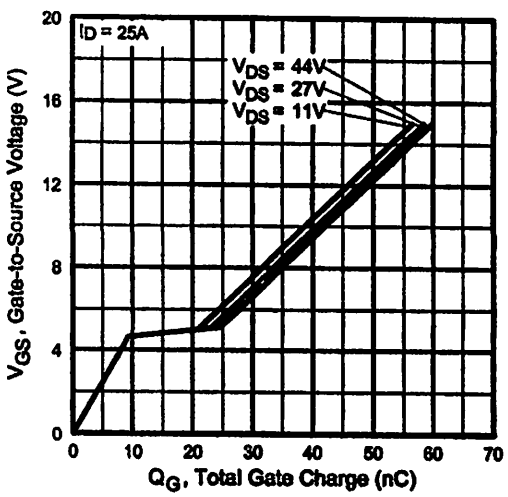


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

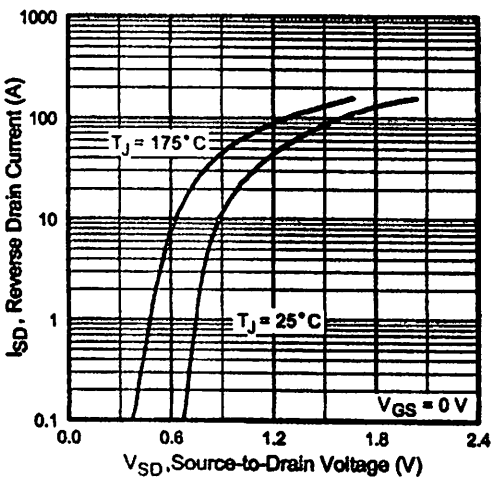


Fig 7. Typical Source-Drain Diode Forward Voltage

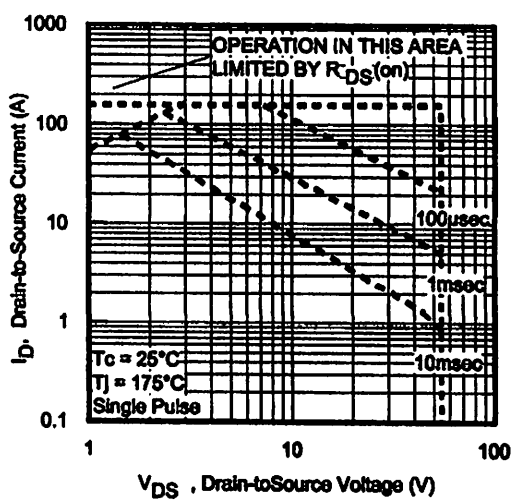


Fig 8. Maximum Safe Operating Area

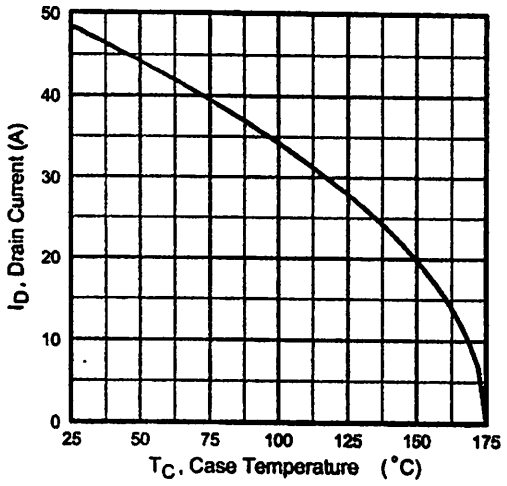


Fig 9. Maximum Drain Current Vs. Case Temperature

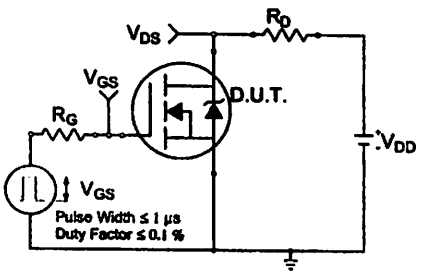


Fig 10a. Switching Time Test Circuit

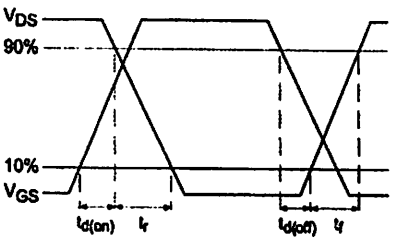


Fig 10b. Switching Time Waveforms

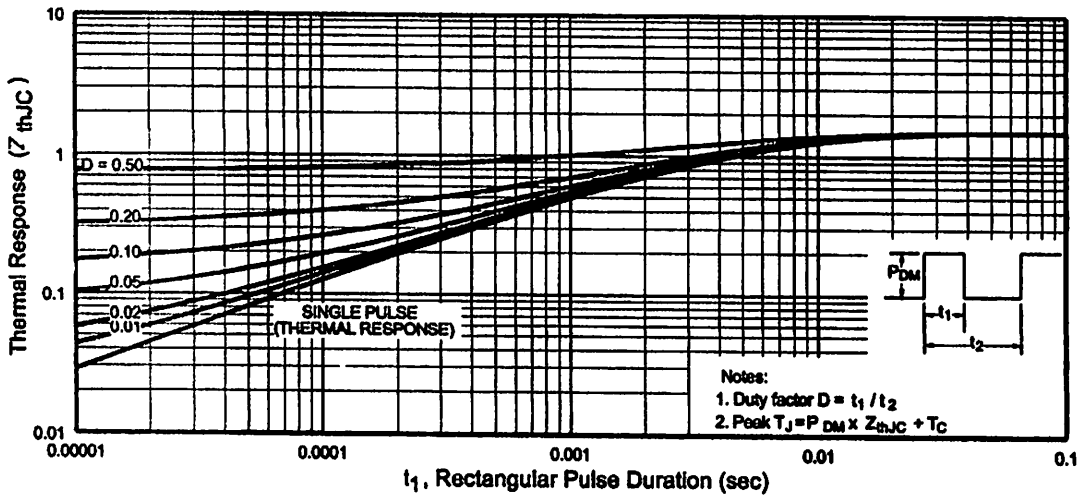


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

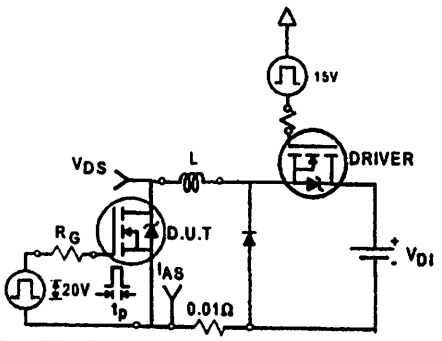


Fig 12a. Unclamped Inductive Test Circuit

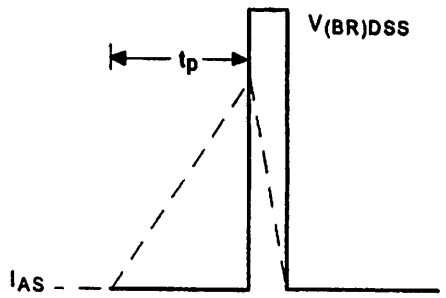


Fig 12b. Unclamped Inductive Waveforms

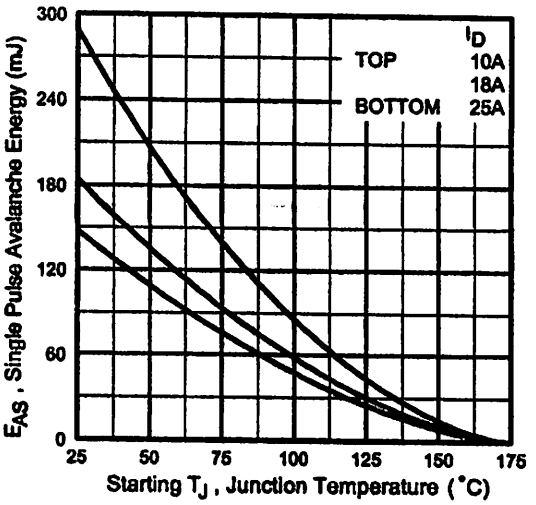


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

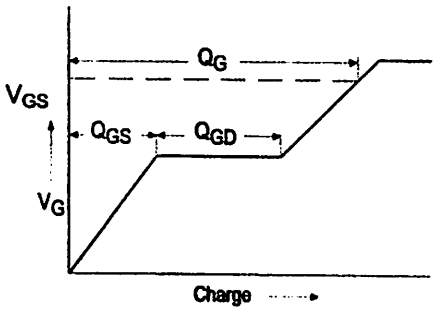


Fig 13a. Basic Gate Charge Waveform

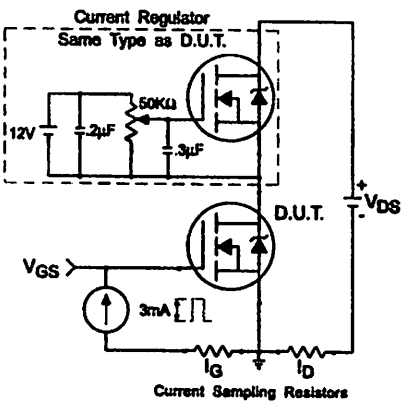
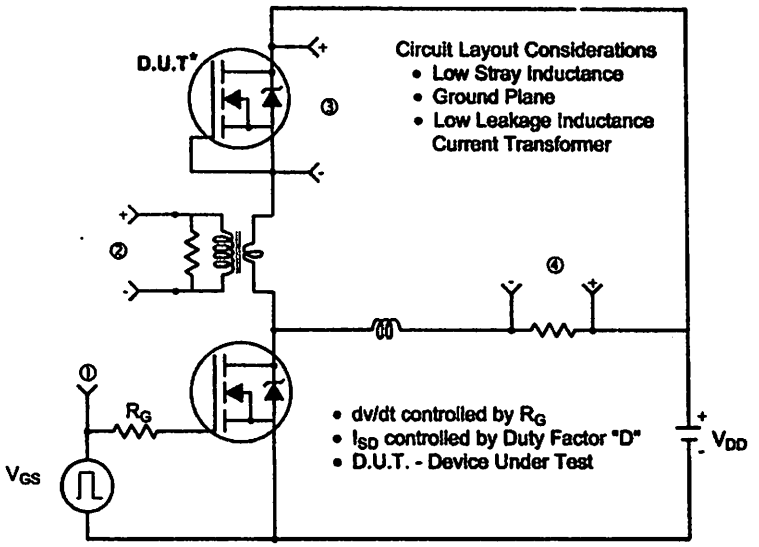
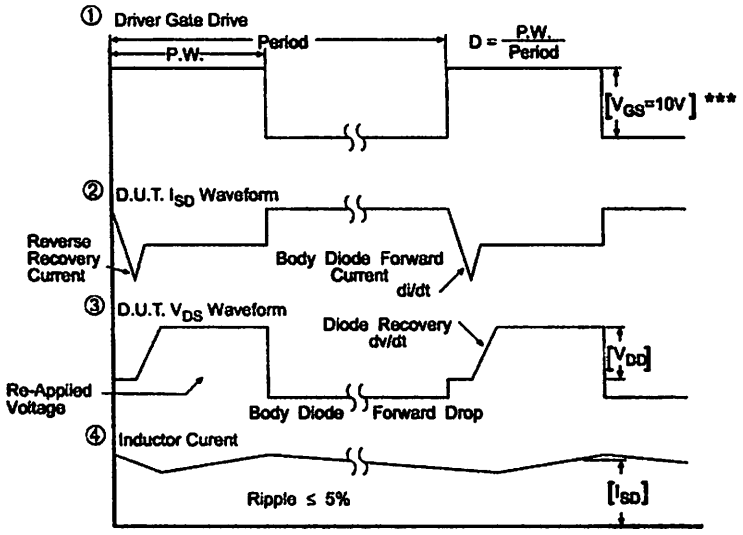


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



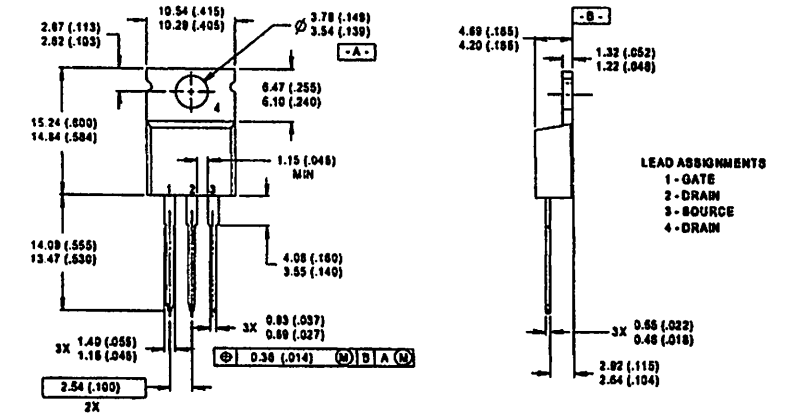
*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

Package Outline

TO-220AB

Dimensions are shown in millimeters (inches)



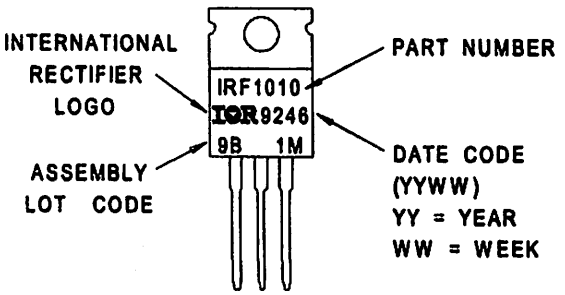
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
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National Semiconductor

July 8, 2009

ADC0808/ADC0809

8-Bit µP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

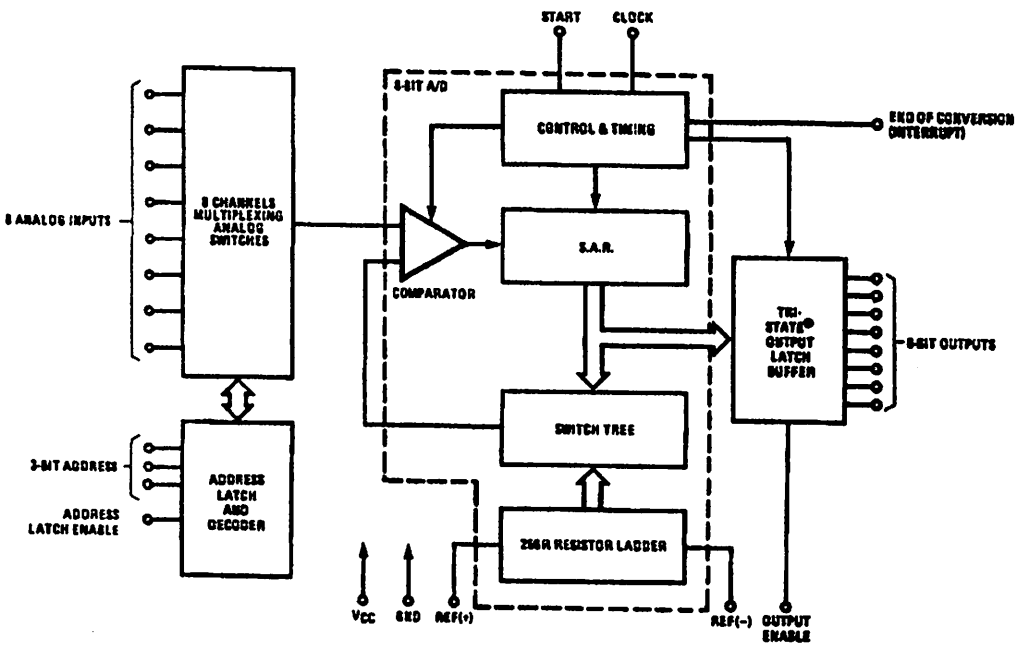
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to V_{CC} input range
- Outputs meet TTL voltage level specifications
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 µs

Block Diagram

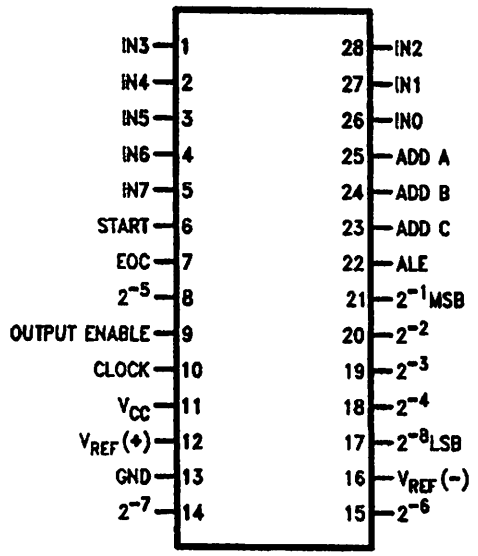


557201

See Ordering Information

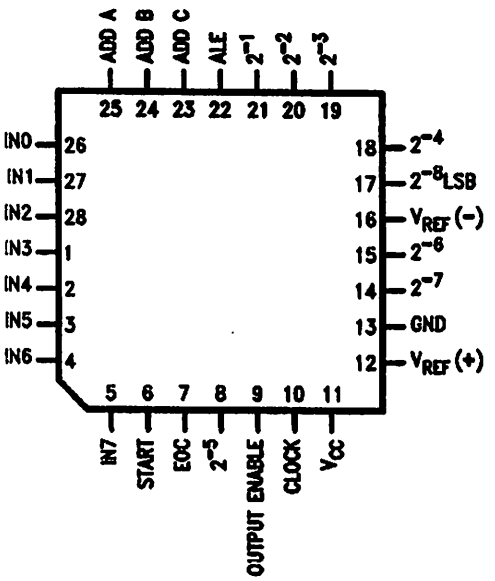
Connection Diagrams

Dual-In-Line Package



Order Number ADC0808CCN or ADC0809CCN
See NS Package NA28E

Molded Chip Carrier Package



Order Number ADC0808CCV or ADC0809CCV
See NS Package V28A

Ordering Information

Temperature Range		–40°C to +85°C		
Package Outline		NA28E Molded DIP	V28A Molded Chip Carrier	V28A Molded Chip Carrier (Tape and Reel)
Error	±½ LSB Unadjusted	ADC0808CCN	ADC0808CCV	ADC0808CCVX
	±1 LSB Unadjusted	ADC0809CCN	ADC0809CCV	ADC0809CCVX

Absolute Maximum Ratings

(Notes 2, 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin	−0.3V to (V_{CC} +0.3V)
Except Control Inputs	
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	−0.3V to +15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 8)	400V

Operating Conditions

(Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
	−40°C≤T_A≤+85°C
Range of V_{CC}	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics – Converter Specifications

Converter Specifications: V_{CC}=5 V_{DC}=V_{REF+}, $V_{REF(-)}$=GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			±½	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±¾	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			±1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±1¼	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND − 0.1		V_{CC} + 0.1	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC} + 0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		(V_{CC}/2) − 0.1	V_{CC}/2	(V_{CC}/2) + 0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
I_N	Comparator Input Current	f_c=640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics – Digital Levels and DC Specifications

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75≤V_{CC}≤5.25V, −40°C≤T_A≤+85°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=5V,				
		T_A=25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=0,				
		T_A=25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		(V_{CC} − 1.5)			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN}=15V			1.0	µA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN}=0	−1.0			µA
I_{CC}	Supply Current	f_{CLK}=640 kHz		0.3	3.0	mA
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V I_{OUT} = −360µA I_{OUT} = −10µA	 2.4 4.5			 V V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O=1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O=1.2 mA			0.45	V
I_{OUT}	TRI-STATE Output Current	V_O=5V V_O=0	 −3		3	µA µA

Electrical Characteristics – Timing Specifications

Timing Specifications V_{CC}=$V_{REF(+)}$=5V, $V_{REF(-)}$=GND, t_r=t_f=20 ns and T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{STCLK}	Start Time Delay from Clock	(*Figure 5*)	300		900	ns
t_{WS}	Minimum Start Pulse Width	(*Figure 5*)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(*Figure 5*)		100	200	ns
t_S	Minimum Address Set-Up Time	(*Figure 5*)		25	50	ns
t_H	Minimum Address Hold Time	(*Figure 5*)		25	50	ns
t_D	Analog MUX Delay Time From ALE	R_S=0Ω (*Figure 5*)		1	2.5	µs
t_{H1}, t_{H0}	OE Control to Q Logic State	C_L=50 pF, R_L=10k (*Figure 8*)		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	C_L=10 pF, R_L=10k (*Figure 8*)		125	250	ns
t_C	Conversion Time	f_C=640 kHz, (*Figure 5*) (Note 7)	90	100	116	µs
f_C	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(*Figure 5*)	0		8 + 2 µS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A Zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC}n supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0V_{DC} to 5V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (*Figure 6*). See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description

MULTIPLEXER

The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. *Table 1* shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1. Analog Channel Selection

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (*Figure 1*) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion start pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

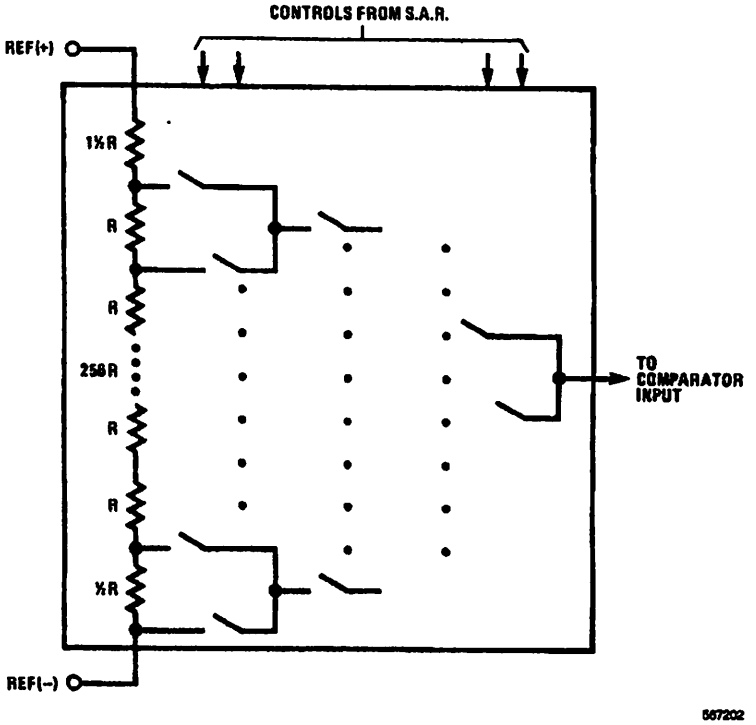


FIGURE 1. Resistor Ladder and Switch Tree

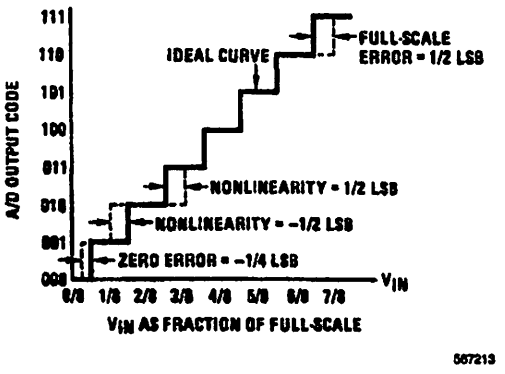


FIGURE 2. 3-Bit A/D Transfer Curve

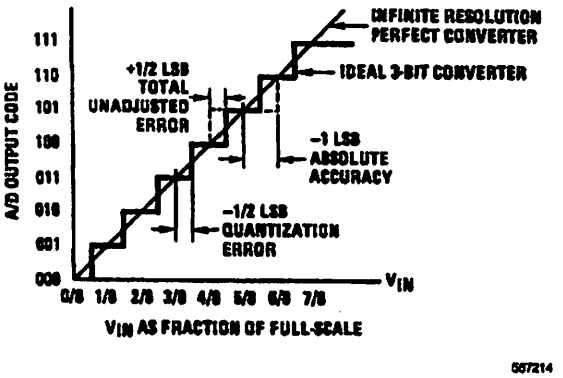


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

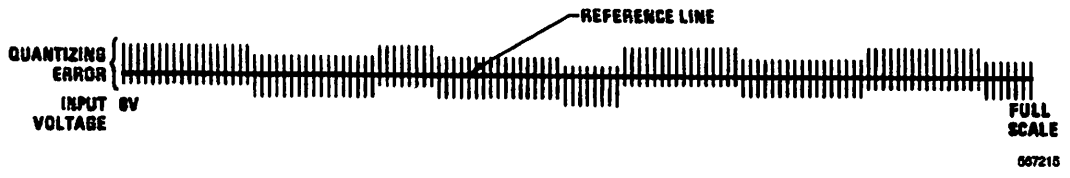


FIGURE 4. Typical Error Curve

Timing Diagram

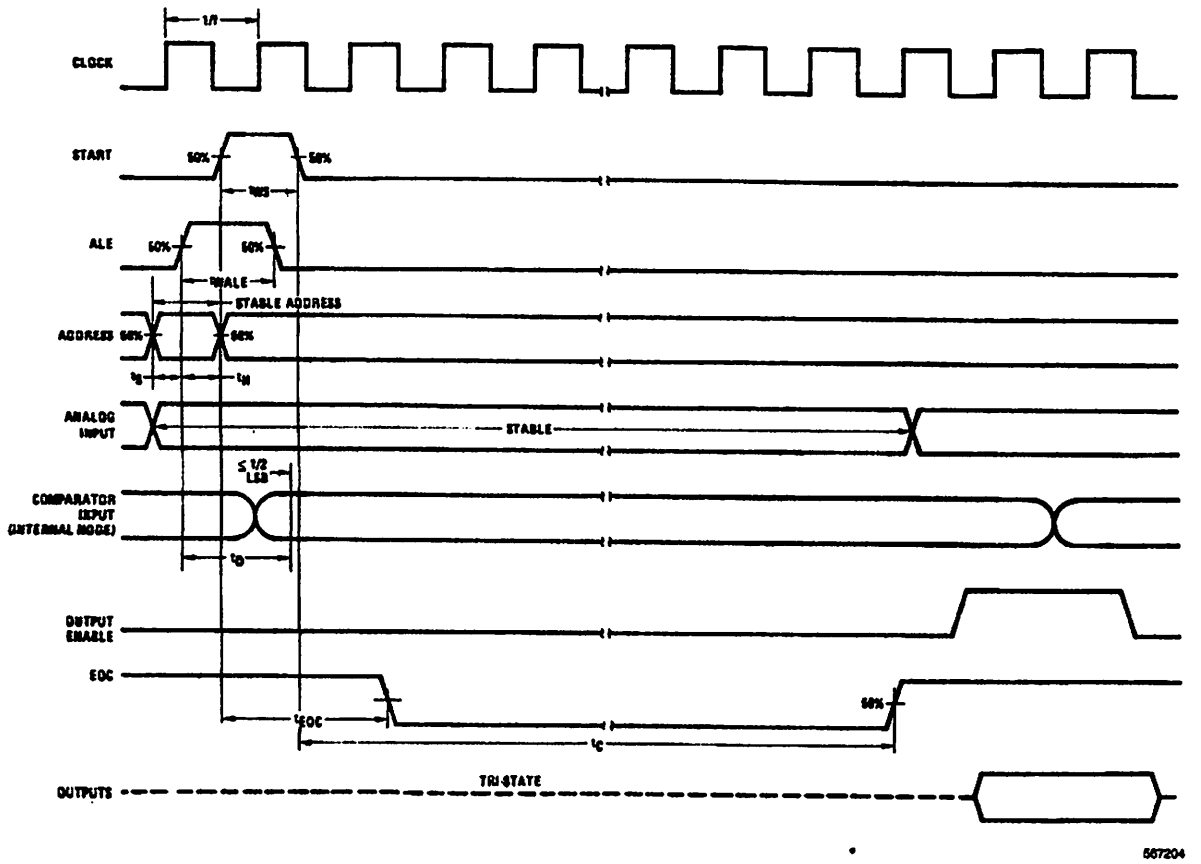


FIGURE 5.

Typical Performance Characteristics

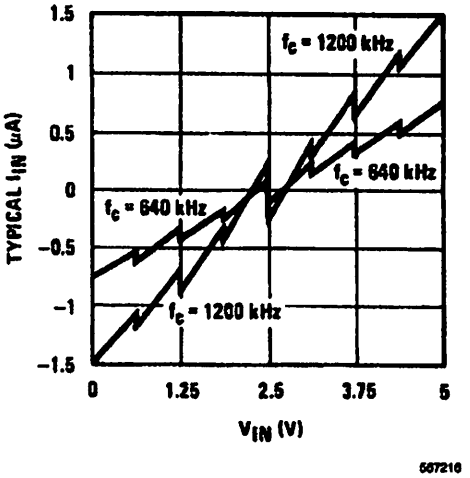


FIGURE 6. Comparator I_{IN} vs. V_{IN} (V_{CC}=V_{REF}=5V)

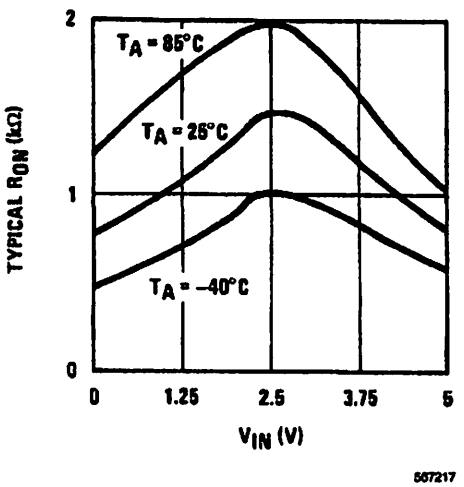


FIGURE 7. Multiplexer R_{ON} vs. V_{IN} (V_{CC}=V_{REF}=5V)

TRI-STATE Test Circuits and Timing Diagrams

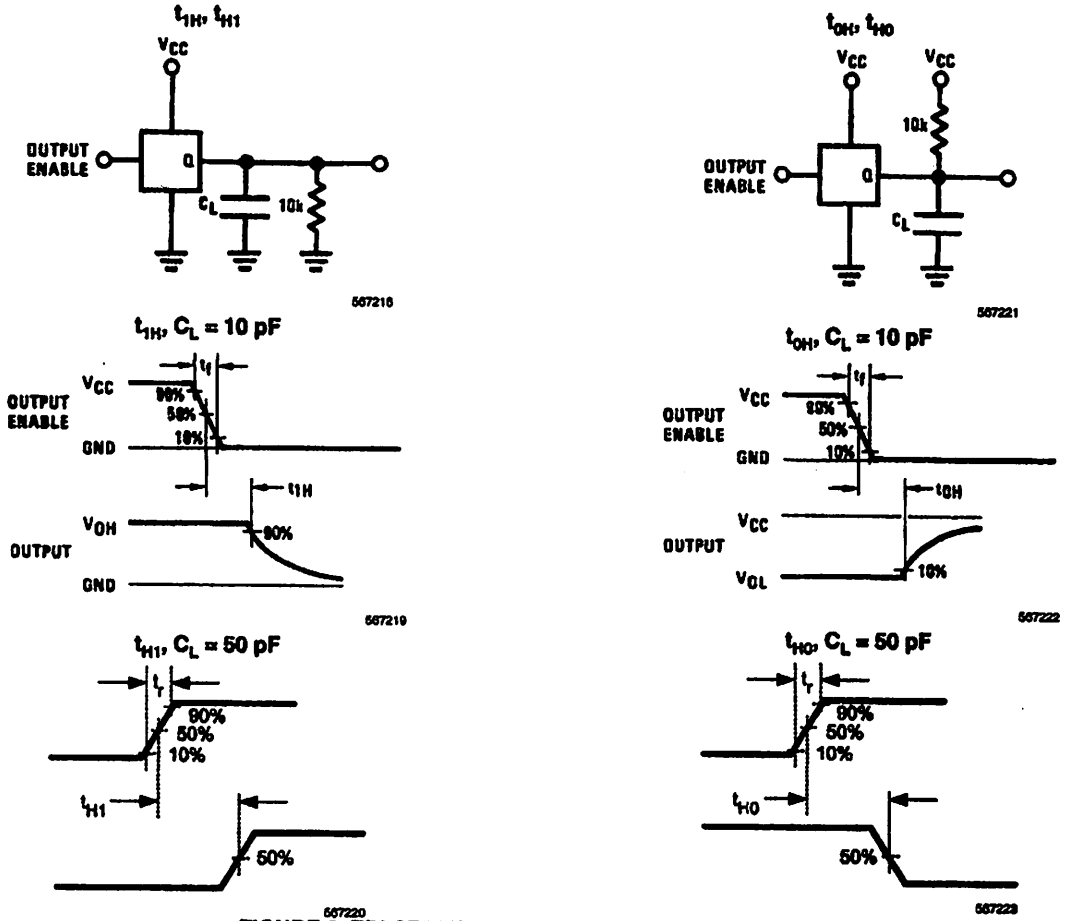


FIGURE 8. TRI-STATE Test Circuits and Timing Diagrams

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \qquad (1)$$

V_{IN}= Input voltage into the ADC0808
V_{fs}= Full-scale voltage
V_Z= Zero voltage
D_X= Data point being measured
D_{MAX}= Maximum data limit
D_{MIN}= Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (*Figure 9*).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if V_{CC}=V_{REF}=5.12V, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder volt-

age must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

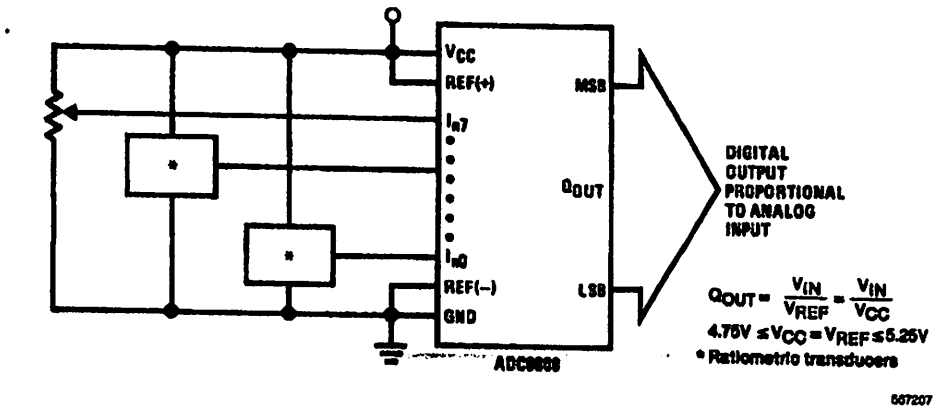
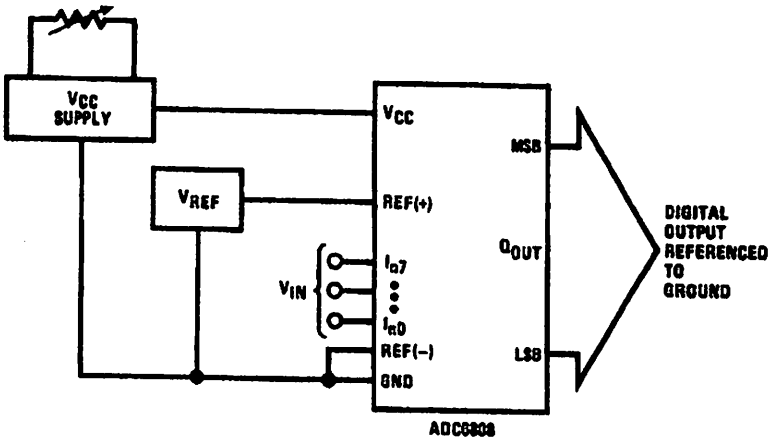


FIGURE 9. Ratiometric Conversion System

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 µF output capacitor.

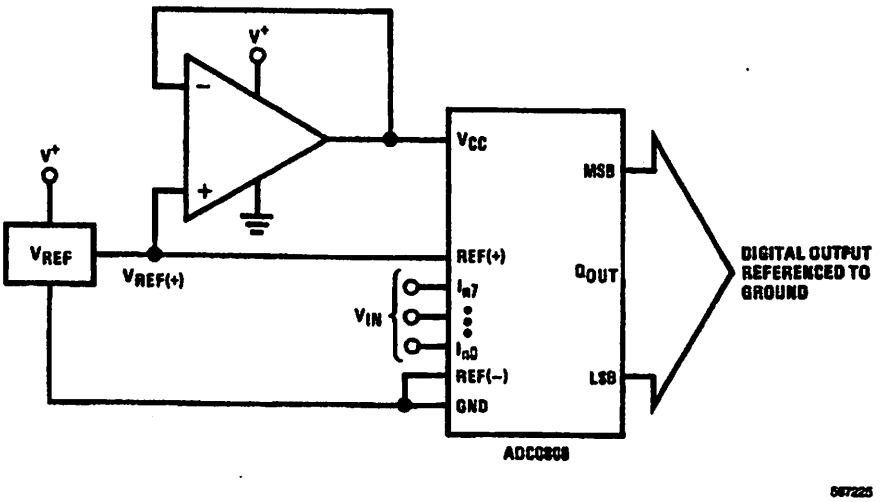
The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.



$$Q_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$$

FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply



$$D_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

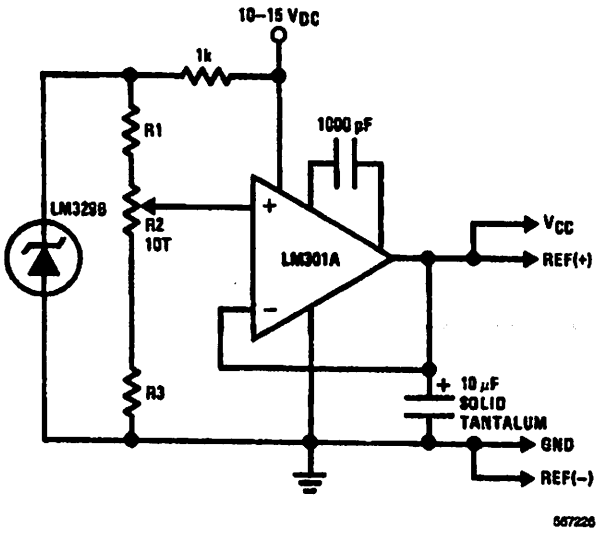
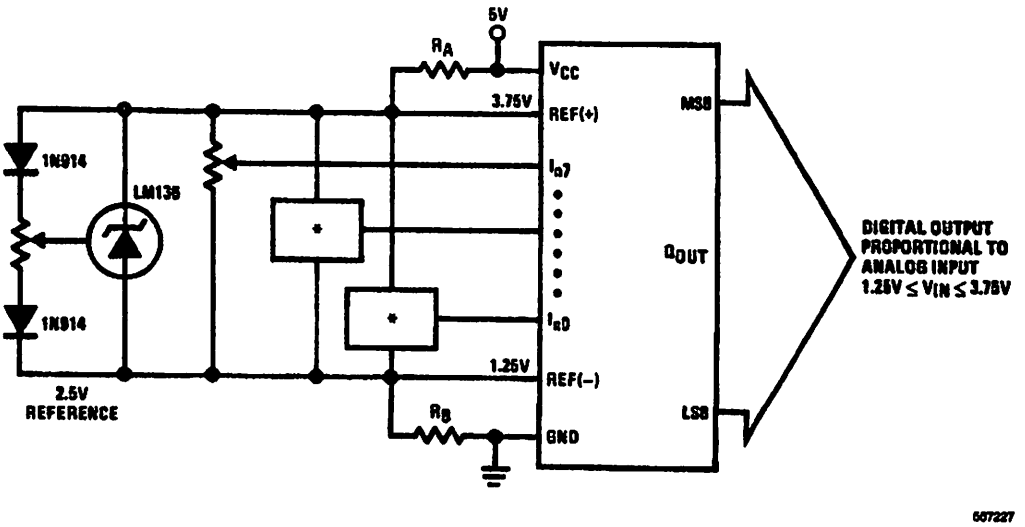


FIGURE 12. Typical Reference and Supply Circuit



$R_A=R_B$

*Ratiometric transducers

FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N+1 is given by:

$$V_{IN}=\left\{(V_{REF(+)}-V_{REF(-)})\left[\frac{N}{256}+\frac{1}{512}\right]\pm V_{TUE}\right\}+V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN}\left\{(V_{REF(+)}-V_{REF(-)})\left[\frac{N}{256}\right]\pm V_{TUE}\right\}+V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N=\frac{V_{IN}-V_{REF(-)}}{V_{REF(+)}-V_{REF(-)}}\times 256\pm \text{Absolute Accuracy} \quad (4)$$

Where: V_{IN}=Voltage at comparator input
$V_{REF(+)}$=Voltage at Ref(+)
$V_{REF(-)}$=Voltage at Ref(−)
V_{TUE}=Total unadjusted error voltage (typically $V_{REF(+)}$÷512)

4.0 ANALOG COMPARATOR INPUTS

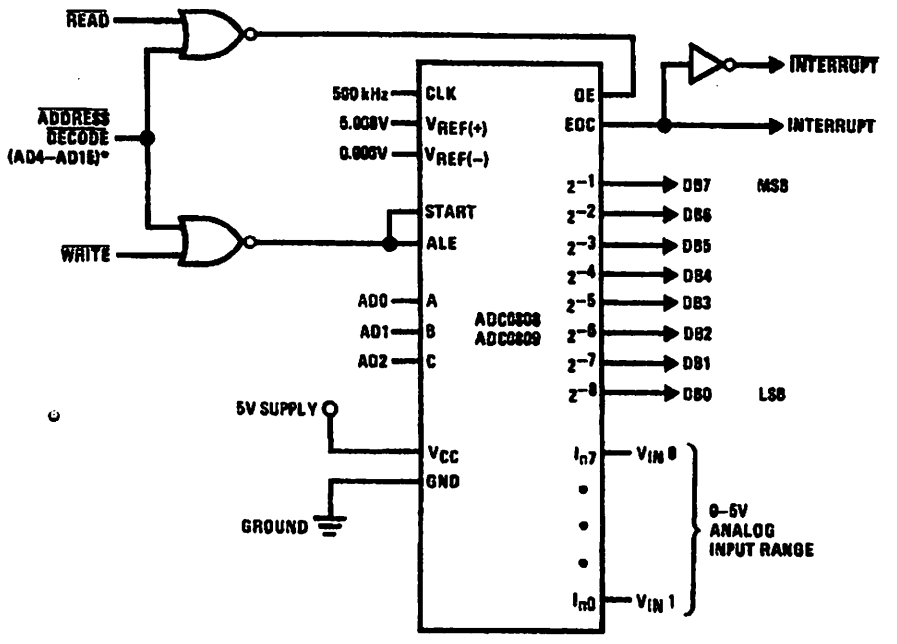
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6.*

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Typical Application



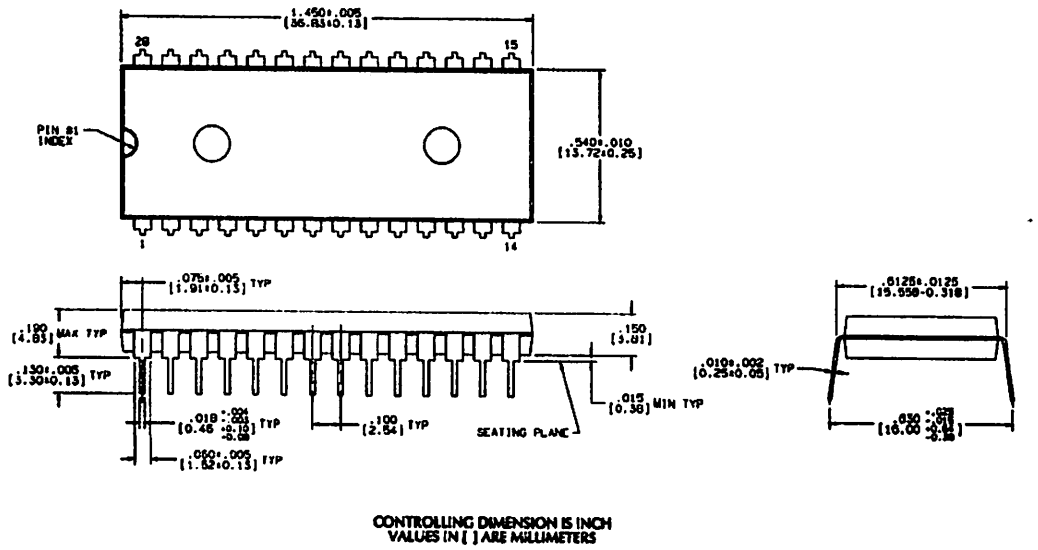
567210

*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

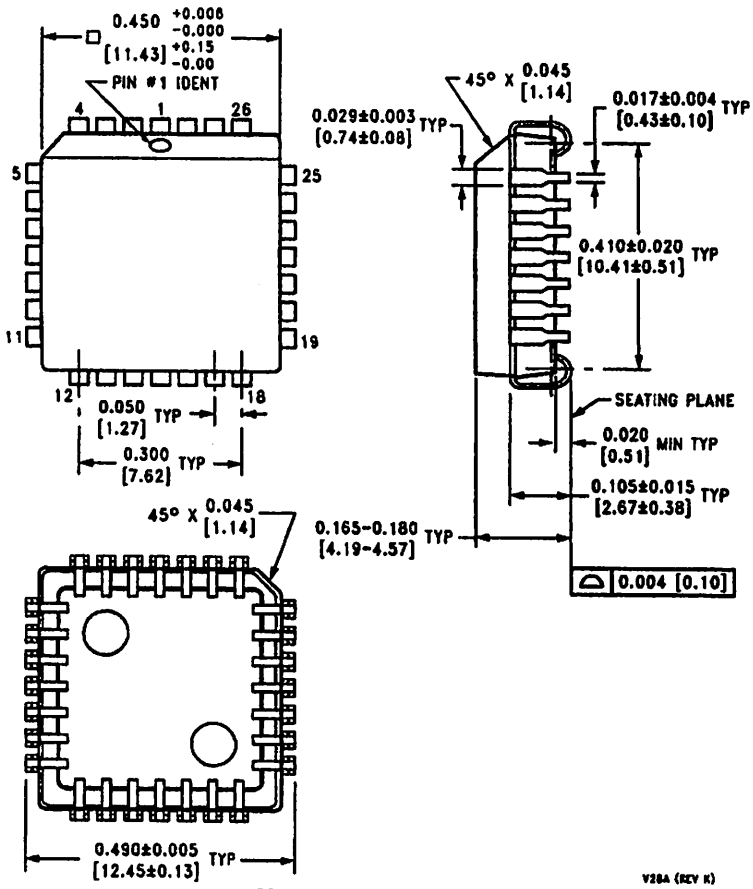
TABLE 2. Microprocessor Interface Table

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•φ2•R/W	VMA•φ•$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number ADC0808CCN or ADC0809CCN
NS Package Number NA28E



Molded Chip Carrier (V)
Order Number ADC0808CCV or ADC0809CCV
NS Package Number V28A

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Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
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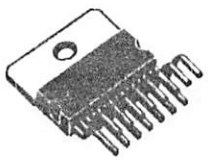
SGS-THOMSON MICROELECTRONICS

L298

DUAL FULL-BRIDGE DRIVER

- OPERATING SUPPLY VOLTAGE UP TO 46 V
- TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)



Multiwatt15

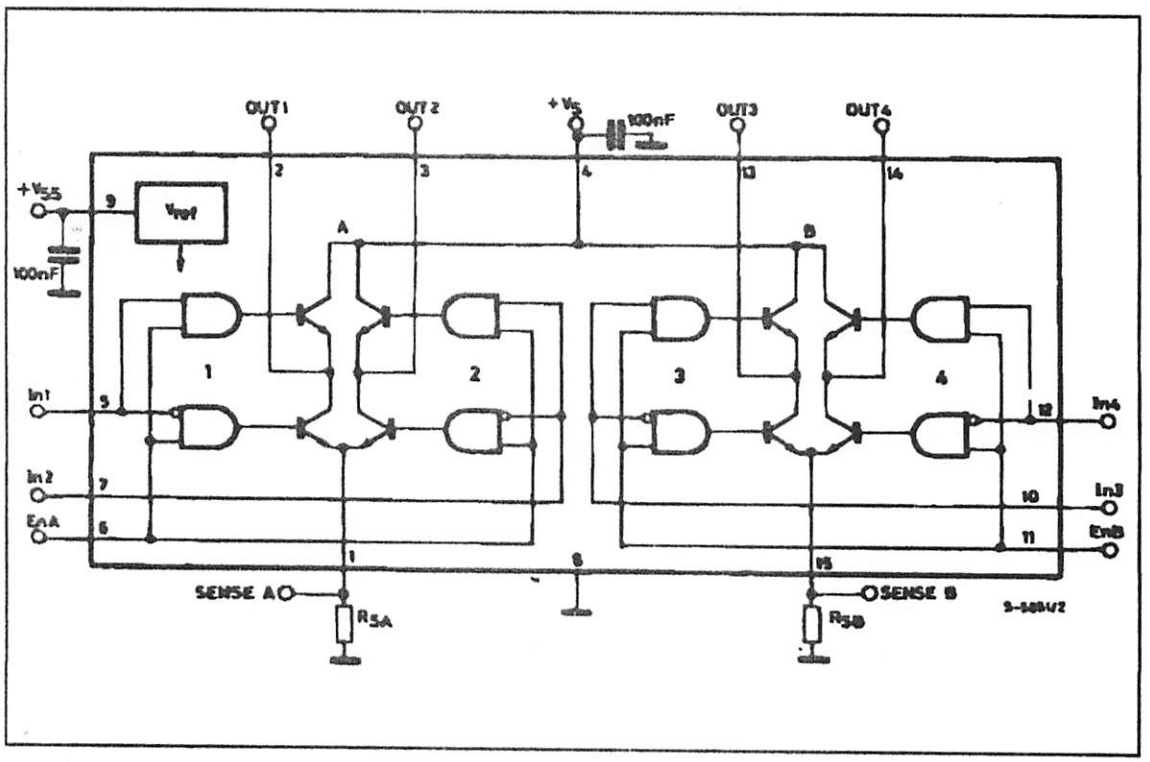
PowerSO20

ORDERING NUMBERS : L298N (Multiwatt Vert.)
L298HN (Multiwatt Horiz.)
L298P (PowerSO20)

DESCRIPTION

The L298 is an integrated monolithic circuit in a 15-lead Multiwatt and PowerSO20 packages. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

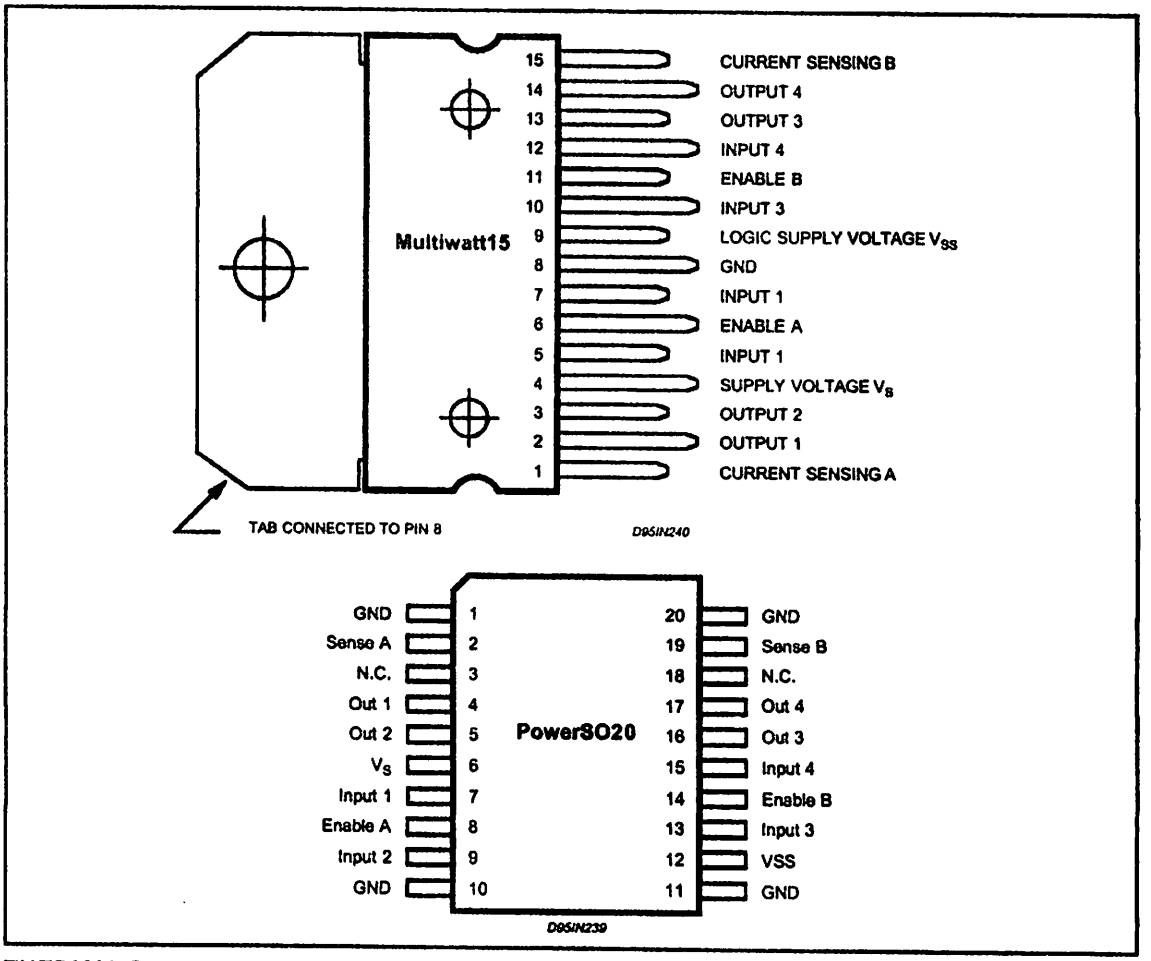
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply	50	V
V_{SS}	Logic Supply Voltage	7	V
V_i, V_{en}	Input and Enable Voltage	–0.3 to 7	V
I_O	Peak Output Current (each Channel) – Non Repetitive (t = 100µs) –Repetitive (80% on –20% off; t_{on} = 10ms) –DC Operation	 3 2.5 2	 A A A
V_{sens}	Sensing Voltage	–1 to 2.3	V
P_{tot}	Total Power Dissipation (T_{case} = 75°C)	25	W
T_{stg}, T_j	Storage and Junction Temperature	–40 to 150	°C

PIN CONNECTIONS (top view)



THERMAL DATA

Symbol	Parameter		PowerSO20	Multiwatt15	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	–	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	13 (*)	35	°C/W

(*) Mounted on aluminum substrate

PIN FUNCTIONS (refer to the block diagram)

MW.15	PowerSO	Name	Function
1;15	2;19	Sense A; Sense B	Between this pin and ground is connected the sense resistor to control the current of the load.
2;3	4;5	Out 1; Out 2	Outputs of the Bridge A; the current that flows through the load connected between these two pins is monitored at pin 1.
4	6	V_S	Supply Voltage for the Power Output Stages. A non-inductive 100nF capacitor must be connected between this pin and ground.
5;7	7;9	Input 1; Input 2	TTL Compatible Inputs of the Bridge A.
6;11	8;14	Enable A; Enable B	TTL Compatible Enable Input: the L state disables the bridge A (enable A) and/or the bridge B (enable B).
8	1,10,11,20	GND	Ground.
9	12	VSS	Supply Voltage for the Logic Blocks. A100nF capacitor must be connected between this pin and ground.
10; 12	13;15	Input 3; Input 4	TTL Compatible Inputs of the Bridge B.
13; 14	16;17	Out 3; Out 4	Outputs of the Bridge B. The current that flows through the load connected between these two pins is monitored at pin 15.
–	3;18	N.C.	Not Connected

ELECTRICAL CHARACTERISTICS (V_S = 42V; V_{SS} = 5V, T_j = 25°C; unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 4)	Operative Condition		V_{IH} +2.5		46	V
V_{SS}	Logic Supply Voltage (pin 9)			4.5	5	7	V
I_S	Quiescent Supply Current (pin 4)	V_{en} = H; I_L = 0	V_i = L V_i = H		13 50	22 70	mA mA
		V_{en} = L	V_i = X			4	mA
I_{SS}	Quiescent Current from V_{SS} (pin 9)	V_{en} = H; I_L = 0	V_i = L V_i = H		24 7	36 12	mA mA
		V_{en} = L	V_i = X			6	mA
V_{iL}	Input Low Voltage (pins 5, 7, 10, 12)			–0.3		1.5	V
V_{iH}	Input High Voltage (pins 5, 7, 10, 12)			2.3		VSS	V
I_{iL}	Low Voltage Input Current (pins 5, 7, 10, 12)	V_i = L				–10	µA
I_{iH}	High Voltage Input Current (pins 5, 7, 10, 12)	VI = H ≤ V_{SS} –0.6V			30	100	µA
V_{en} = L	Enable Low Voltage (pins 6, 11)			–0.3		1.5	V
V_{en} = H	Enable High Voltage (pins 6, 11)			2.3		V_{SS}	V
I_{en} = L	Low Voltage Enable Current (pins 6, 11)	V_{en} = L				–10	µA
I_{en} = H	High Voltage Enable Current (pins 6, 11)	V_{en} = H ≤ V_{SS} –0.6V			30	100	µA
$V_{CEsat(H)}$	Source Saturation Voltage	I_L = 1A I_L = 2A			1.35 2	1.7 2.7	V V
$V_{CEsat(L)}$	Sink Saturation Voltage	I_L = 1A (5) I_L = 2A (5)			1.2 1.7	1.6 2.3	V V
V_{CEsat}	Total Drop	I_L = 1A (5) I_L = 2A (5)				3.2 4.9	V V
V_{sens}	Sensing Voltage (pins 1, 15)			–1 (1)		2	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_1 (V_i)	Source Current Turn-off Delay	0.5 V_i to 0.9 I_L (2); (4)		1.5		µs
T_2 (V_i)	Source Current Fall Time	0.9 I_L to 0.1 I_L (2); (4)		0.2		µs
T_3 (V_i)	Source Current Turn-on Delay	0.5 V_i to 0.1 I_L (2); (4)		2		µs
T_4 (V_i)	Source Current Rise Time	0.1 I_L to 0.9 I_L (2); (4)		0.7		µs
T_5 (V_i)	Sink Current Turn-off Delay	0.5 V_i to 0.9 I_L (3); (4)		0.7		µs
T_6 (V_i)	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3); (4)		0.25		µs
T_7 (V_i)	Sink Current Turn-on Delay	0.5 V_i to 0.9 I_L (3); (4)		1.6		µs
T_8 (V_i)	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3); (4)		0.2		µs
fc (V_i)	Commutation Frequency	I_L = 2A		25	40	KHz
T_1 (V_{en})	Source Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (2); (4)		3		µs
T_2 (V_{en})	Source Current Fall Time	0.9 I_L to 0.1 I_L (2); (4)		1		µs
T_3 (V_{en})	Source Current Turn-on Delay	0.5 V_{en} to 0.1 I_L (2); (4)		0.3		µs
T_4 (V_{en})	Source Current Rise Time	0.1 I_L to 0.9 I_L (2); (4)		0.4		µs
T_5 (V_{en})	Sink Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (3); (4)		2.2		µs
T_6 (V_{en})	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3); (4)		0.35		µs
T_7 (V_{en})	Sink Current Turn-on Delay	0.5 V_{en} to 0.9 I_L (3); (4)		0.25		µs
T_8 (V_{en})	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3); (4)		0.1		µs
fc (V_{en})	Commutation Frequency	I_L = 2A		1		KHz

1) 1)Sensing voltage can be –1 V for t ≤ 50 µsec; in steady state V_{sens} min ≥ – 0.5 V.
2) See fig. 2.
3) See fig. 4.
4) The load must be a pure resistor.
5) PIN 1 and PIN 15 connected to GND.

Figure 1 : Typical Saturation Voltage vs. Output Current.

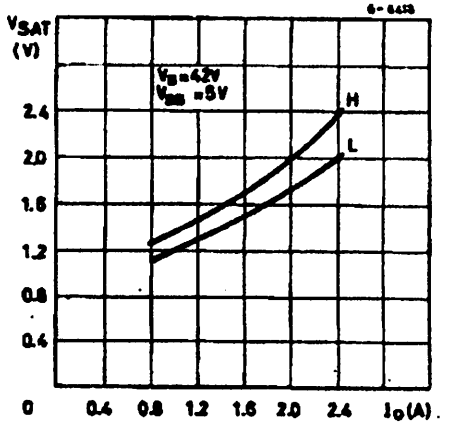
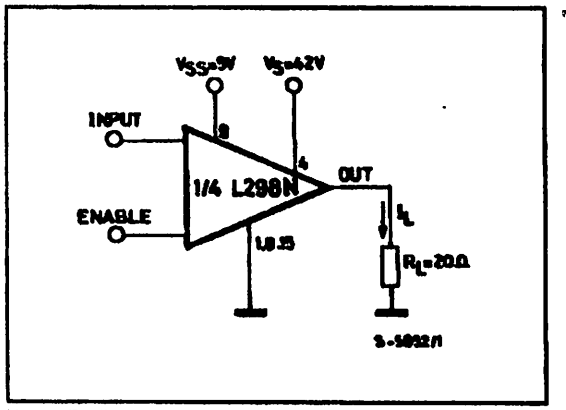


Figure 2 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = H

Figure 3 : Source Current Delay Times vs. Input or Enable Switching.

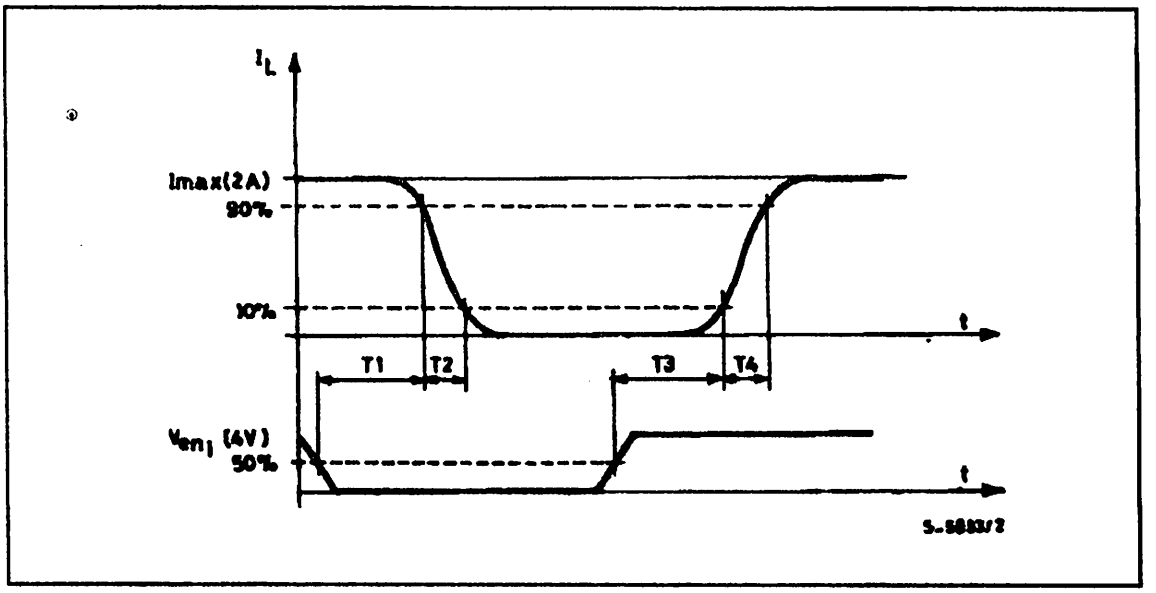
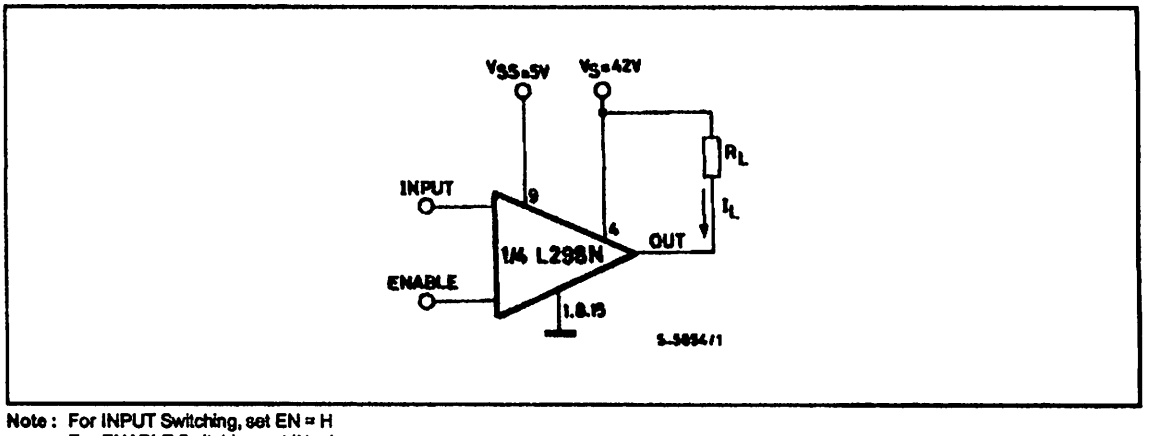


Figure 4 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = L

Figure 5 : Sink Current Delay Times vs. Input 0 V Enable Switching.

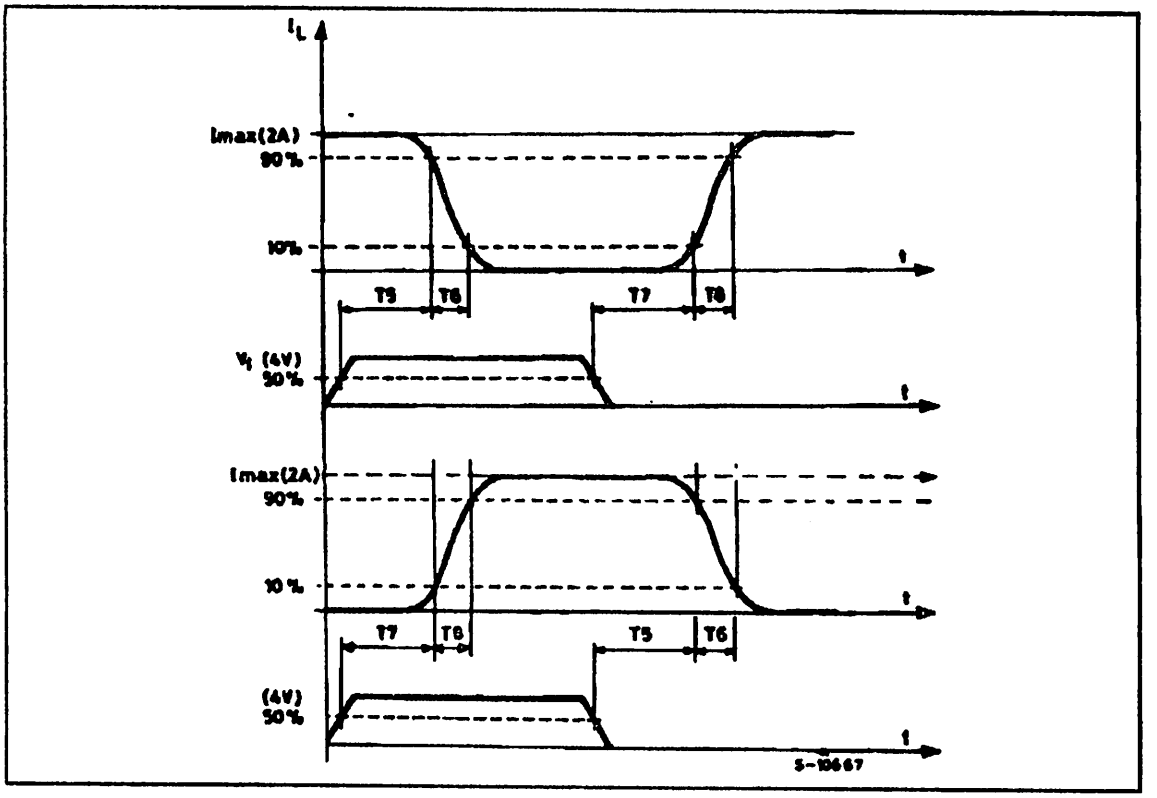
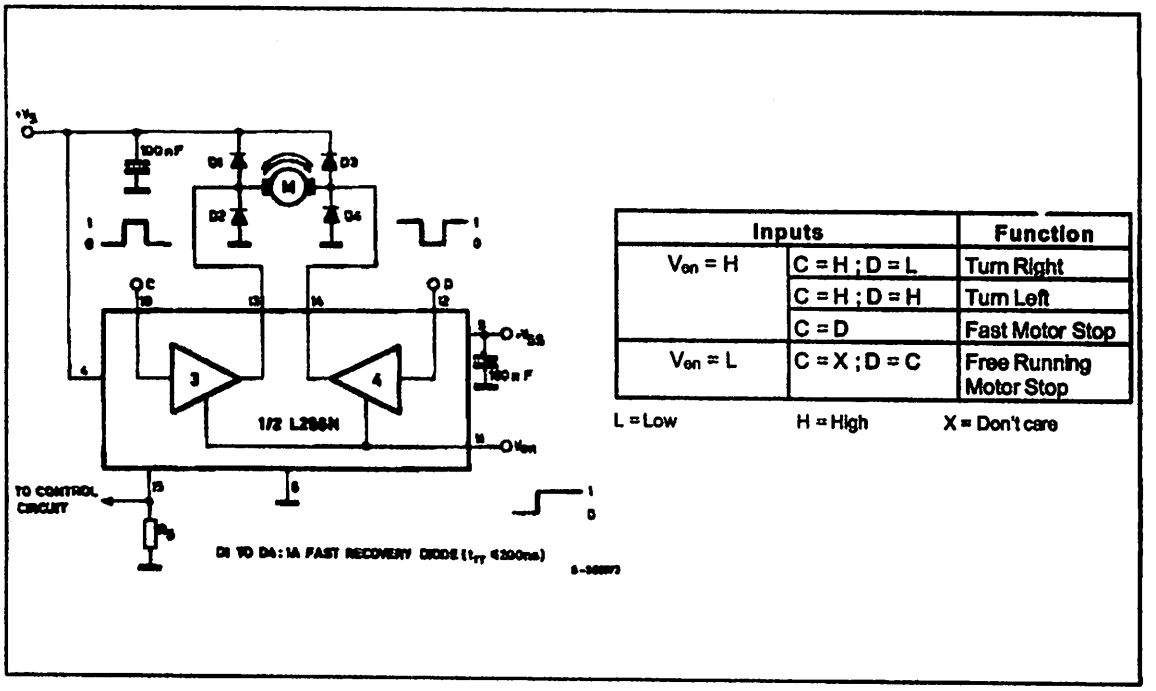


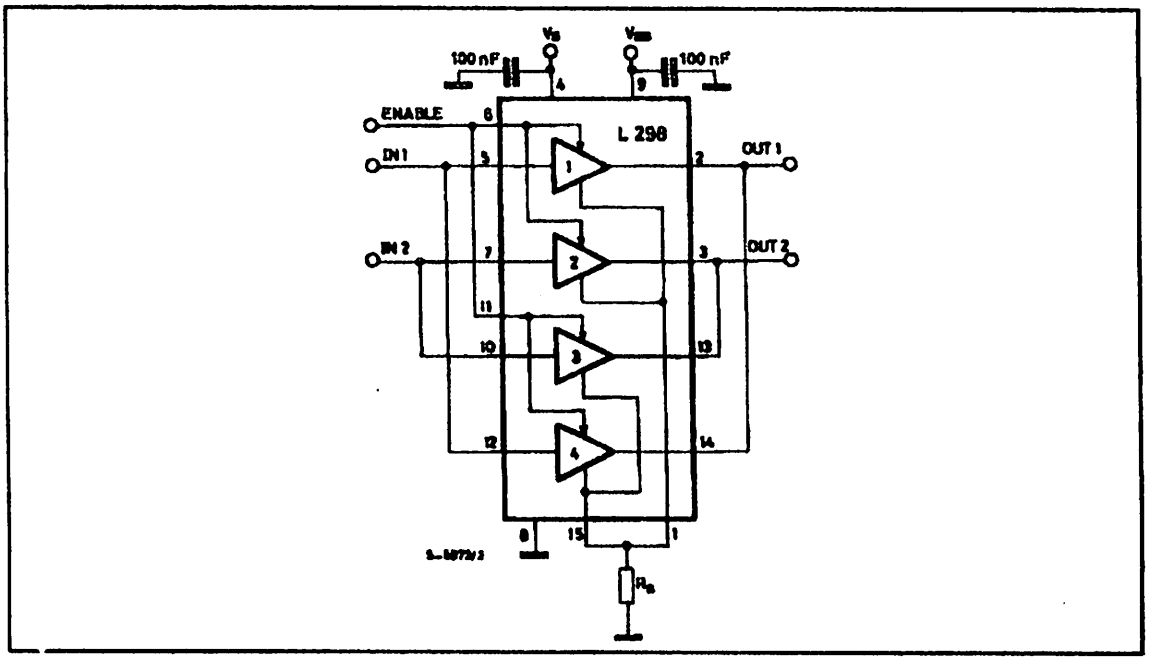
Figure 6 : Bidirectional DC Motor Control.



Inputs		Function
V_{en} = H	C = H ; D = L	Turn Right
	C = H ; D = H	Turn Left
	C = D	Fast Motor Stop
V_{en} = L	C = X ; D = C	Free Running Motor Stop

L = Low H = High X = Don't care

Figure 7 : For higher currents, outputs can be paralleled. Take care to parallel channel 1 with channel 4 and channel 2 with channel 3.



APPLICATION INFORMATION (Refer to the block diagram)

1.1. POWER OUTPUT STAGE

The L298 integrates two power output stages (A ; B). The power output stage is a bridge configuration and its outputs can drive an inductive load in common or differenzial mode, depending on the state of the inputs. The current that flows through the load comes out from the bridge at the sense output : an external resistor (R_{SA} ; R_{SB}.) allows to detect the intensity of this current.

1.2. INPUT STAGE

Each bridge is driven by means of four gates the input of which are In1 ; In2 ; EnA and In3 ; In4 ; EnB. The In inputs set the bridge state when The En input is high ; a low state of the En input inhibits the bridge. All the inputs are TTL compatible.

2. SUGGESTIONS

A non inductive capacitor, usually of 100 nF, must be foreseen between both Vs and Vss, to ground, as near as possible to GND pin. When the large capacitor of the power supply is too far from the IC, a second smaller one must be foreseen near the L298.

The se.,se resistor, not of a wire wound type, must be grounded near the negative pole of Vs that must be near the GND pin of the I.C.

Each input must be connected to the source of the driving signals by means of a very short path.

Turn-On and Turn-Off : Before to Turn-ON the Supply Voltage and before to Turn it OFF, the Enable input must be driven to the Low state.

3. APPLICATIONS

Fig 6 shows a bidirectional DC motor control Schematic Diagram for which only one bridge is needed. The external bridge of diodes D1 to D4 is made by four fast recovery elements ($t_{rr} \leq 200$ nsec) that must be chosen of a VF as low as possible at the worst case of the load current.

The sense output voltage can be used to control the current amplitude by chopping the inputs, or to provide overcurrent protection by switching low the enable input.

The brake function (Fast motor stop) requires that the Absolute Maximum Rating of 2 Amps must never be overcome.

When the repetitive peak current needed from the load is higher than 2 Amps, a paralleled configuration can be chosen (See Fig.7).

An external bridge of diodes are required when inductive loads are driven and when the inputs of the IC are chopped ; Shottky diodes would be preferred.

This solution can drive until 3 Amps In DC operation and until 3.5 Amps of a repetitive peak current.

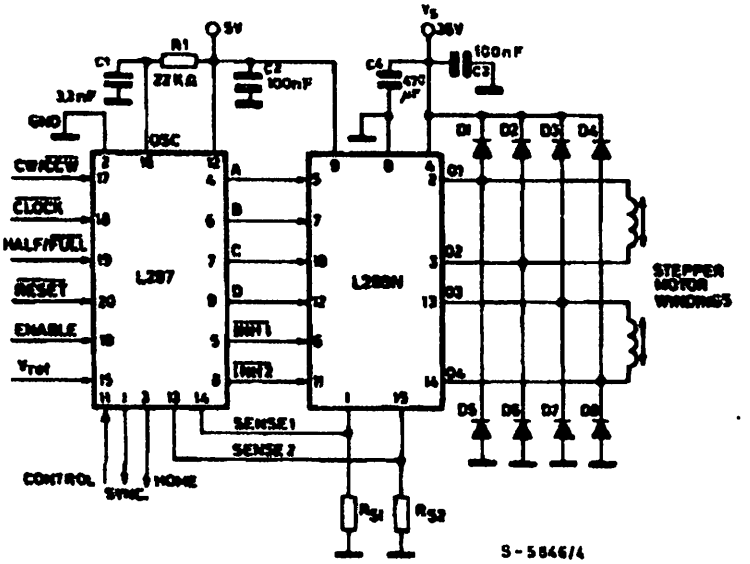
On Fig 8 it is shown the driving of a two phase bipolar stepper motor ; the needed signals to drive the inputs of the L298 are generated, in this example, from the IC L297.

Fig 9 shows an example of P.C.B. designed for the application of Fig 8.

Fig 10 shows a second two phase bipolar stepper motor control circuit where the current is controlled by the I.C. L6506.

Figure 8 : Two Phase Bipolar Stepper Motor Circuit.

This circuit drives bipolar stepper motors with winding currents up to 2 A. The diodes are fast 2 A types.



$R_{S1} = R_{S2} = 0.5\ \Omega$

D1 to D8 = 2 A Fast diodes { $V_F \leq 1.2$ V @ I = 2 A ; $t_{rr} \leq 200$ ns

Figure 9 : Suggested Printed Circuit Board Layout for the Circuit of fig. 8 (1:1 scale).

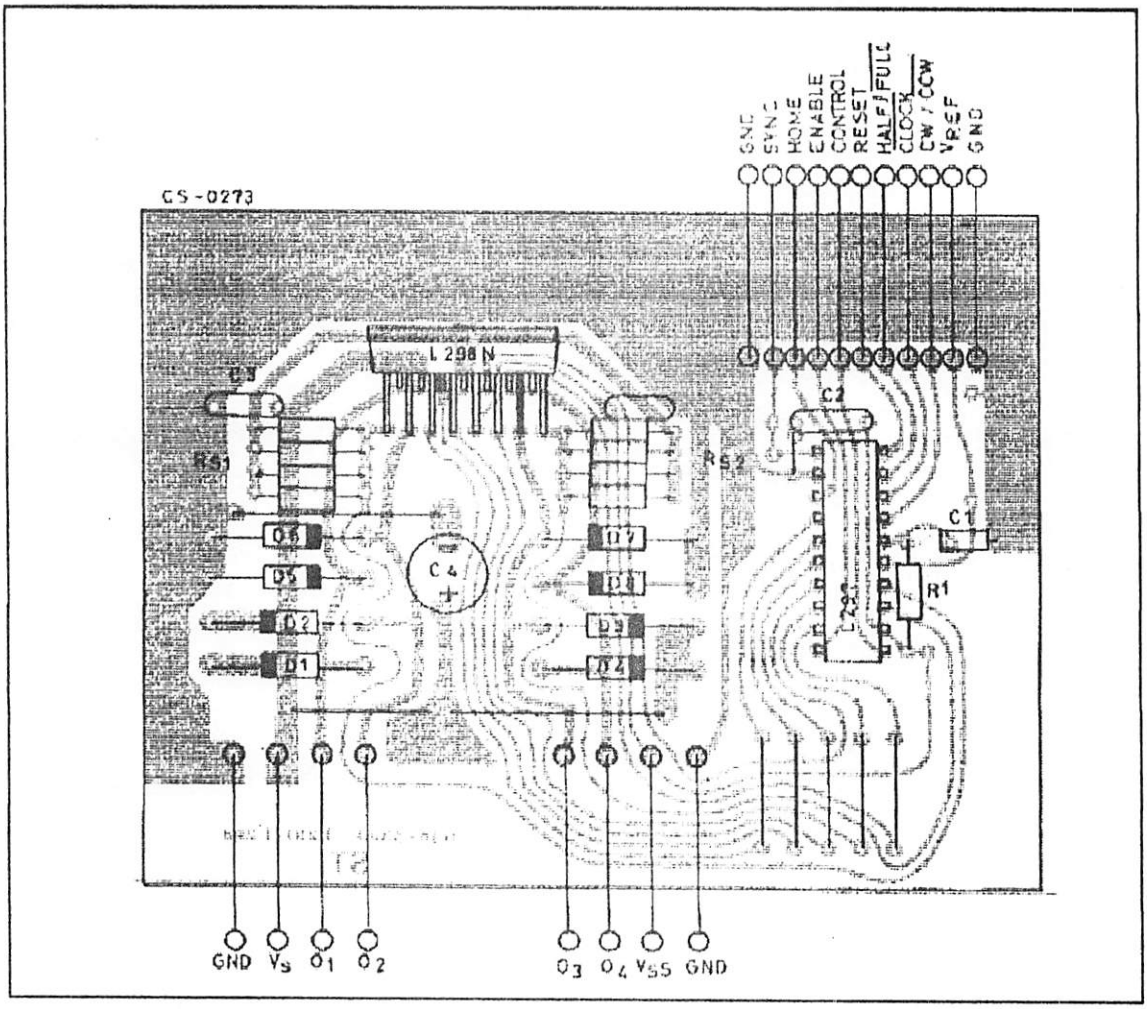
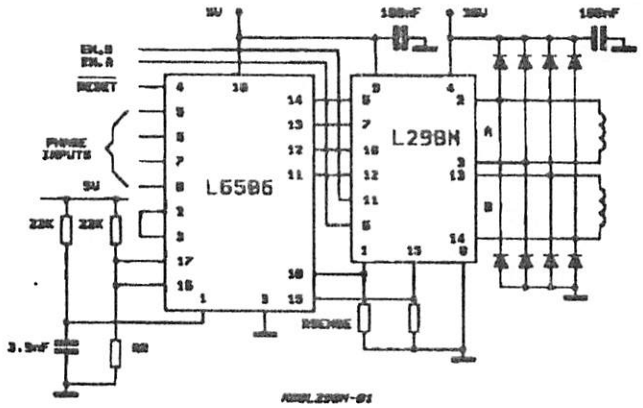


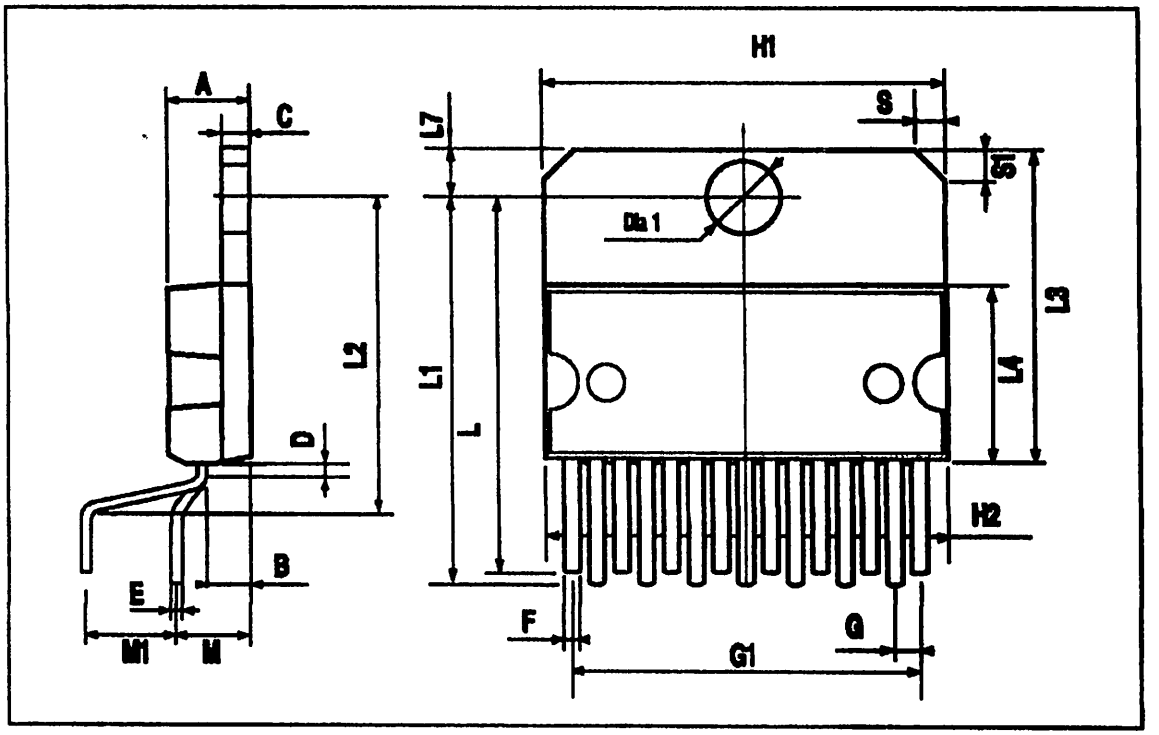
Figure 10 : Two Phase Bipolar Stepper Motor Control Circuit by Using the Current Controller L6506.



R_R and R_{sense} depend from the load current

MULTIWATT15 (VERTICAL) PACKAGE MECHANICAL DATA

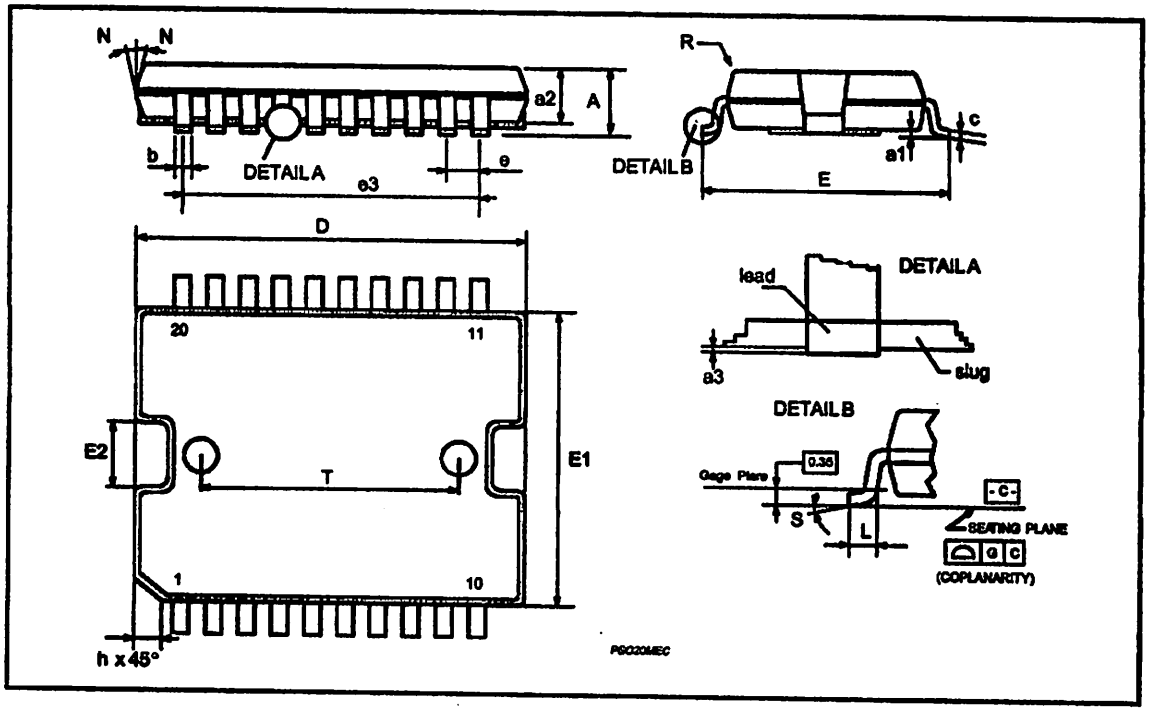
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152



PowerSO20 PACKAGE MECHANICAL DATA

DIM.	mm			Inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.40		0.53	0.0157		0.0209
c	0.23		0.32	0.009		0.0126
D (1)	15.80		16.00	0.6220		0.6299
E	13.90		14.50	0.5472		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.90		11.10	0.4291		0.437
E2			2.90			0.1141
G	0		0.10	0		0.0039
h			1.10			
L	0.80		1.10	0.0314		0.0433
N	10° (max.)					
S	8° (max.)					
T		10.0			0.3937	

(1) "D and E1" do not include mold flash or protrusions
- Mold flash or protrusions shall not exceed 0.15mm (0.006")



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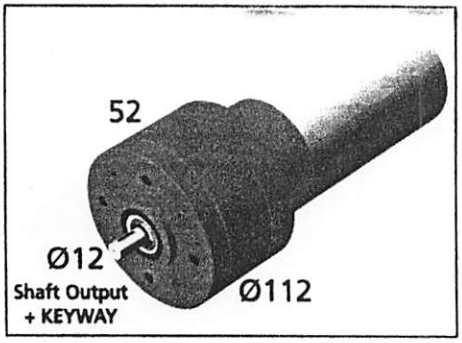

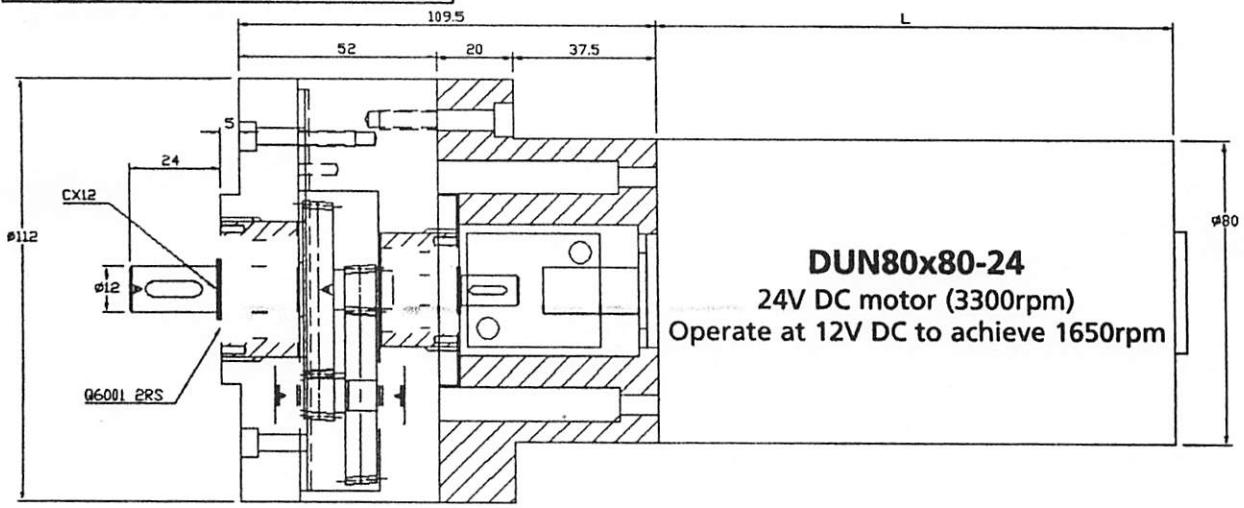

Discounts: 6+ -5% 20+ -10% 50+ -15% 100+ -20%

Part Number	Ratio	Output Torque at 1650 rpm Input Nm	L	Direction	DC Motor	Price Each 1 - 5
TG112-2ADC	2:1	1.14	175	Same	DUN80x80-24	£531.86
TG112-4ADC	4:1	2.28	175	Same	DUN80x80-24	£531.86
TG112-5ADC	5:1	2.85	175	Same	DUN80x80-24	£531.86
TG112-6ADC	6:1	3.42	175	Same	DUN80x80-24	£531.86
TG112-8ADC	8:1	4.56	175	Same	DUN80x80-24	£531.86
TG112-10ADC	10:1	5.00	175	Same	DUN80x80-24	£531.86
TG112-12ADC	12:1	5.00	175	Same	DUN80x80-24	£531.86
TG112-16ADC	16:1	4.50	175	Same	DUN80x80-24	£531.86

Performance

Weight: 3.5kg

Other Info.

Assembly includes:-
1 x Gearhead
1 x DC Motor
1 x Shaft Coupling
1 x Set of fixing screws for motor to plate
1 x Set of fixing screws for plate to gearbox
1 x Adaptor plate

Check motor data and gearbox chart for max. torque figures. Testing in your applications is necessary.
You will need to assess duty, cycles and confirm gearbox suitability with your own calculations. Torque figures are to be used for guidance only.

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