PERENCANAAN DAN PEMBUATAN OTOMATISASI PROSES GYNOGENESIS PADA PEMBIBITAN IKAN MAS *(Cyprinus Carpio)* BERBASIS ATMEGA8535

SKRIPSI

Diajukan Sebagai Salah Satu Syarat
Untuk Memperoleh Gelar Sarjana Teknik
Program Studi Teknik Elektronika

Disusun Oleh :

NAMA : Hadiansyah Noor Rochim
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JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG

2007

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PERANCANGAN DAN PEMBUATAN OTOMATISASI PROSES GYNOGENESIS PEMBIBITAN IKAN MAS (Cyprinus Carpio) BERBASIS ATMEGA 8535

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KATA PENGANTAR

Puji syukur kehadirat Tuhan Yang Maha Esa penulis panjatkan oleh karena telah terselesaikannya Skripsi ini. Skripsi ini dilaksanakan untuk memenuhi persyaratan memperoleh gelar Sarjana Teknik Elektro program studi Elektronika.

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Malang, Maret 2007

Penulis

ABSTRAK

Gynogenesis adalah proses produksi embrio dari telur-telur yang dibuahi oleh sperma tanpa sumbangan bahan genetik jantan. Dengan menggunakan metode gynogenesis bibit unggul dapat diperoleh dalam dua generasi. Sedangkan kalau dikombinasikan dengan program seleksi dan hibridisasi (kawin silang) akan dihasilkan peningkatan kualitas genetik ikan yang dapat dilakukan dalam waktu tiga generasi.

Secara teoritis dan riset metode pembibitan dengan metode gynogenesis telah dapat meningkatkan produktivitas, tetapi kenyataan di lapangan, ternyata realisasi dengan metode ini masih memakai teknologi yang sederhana sehingga hasilnya masih jauh dari yang diharapkan. Maka dari itu pada Skripsi ini dibuat alat memakai teknologi otomatisasi guna mengurangi kesalahan yang mungkin terjadi dan dapat meningkatkan hasil dari pem benihan ikan mas. Sistem ini dikendalikan sepenuhnya oleh mikrokontroller ATmega8535L dan sebagai keluaran akhir adalah berupa tampilan LCD, dengan suhu dapat dimonitoring di dalamnya dengan masukan melalui keypad.

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BAB I

PENDAULUAN

1.1. Lata belakang masalah

Pada akhir-akhir ini ikan mas punten sudah jarang diperoleh dipasaran dengan kemurniannya masih diragukan, hal ini berhubungan erat dengan sifat unggul ikan tersebut., schingga masalah kemurnian ras menjadi hal yang sangat penting untuk dapat menciptakan bibit-bibit baru yang unggul sehingga dapat membantu para petani dalam pembudidayaan. Program pemurnian ikan mas dapat dilakukan dengan metode pemuliaan ikan, baik secara konvensional maupun secara modern. Dengan cara konvensional pemurnian ikan dapat dilakukan dengan metode seleksi, dimana ikan-ikan yang baik disclcksi dan dikembangkan dengan cara *inbreeding*, kemudian benih ikan tersebut disclcksi kembali. Metode ini sangat tidak efisien karena bibit unggul baru bisa diperoleh dalam waktu kurang lebih 15 generasi.

Potensi ikan mas *(Cyprinus carpio)* sebagai ikan budidaya cukup besar, ikan ini memiliki beberapa kelebihan yaitu :

1. Mudah berkembang biak dalam lingkungan budidaya
2. Dapat dipelihara dengan kepadatan yang relatif tinggi
3. Dapat menerima makanan yang beragam (mulai dari makanan alami sampai dengan makanan buatan)

4. Toleran terhadap perubahan panas, keadaan makanan dan oksigen di lingkungannya
5. Pertumbuhannya relatif cepat.

Program pemurnian ikan mas dengan cara modern adalah dengan menggunakan metode gynogenesis. *Gynogenesis* adalah proses produksi embrio dari telur-telur yang dibuahi oleh sperma tanpa sumbangan bahan genetik jantan.

Secara teoritis dan riset metode pembibitan dengan metode gynogenesis mempunyai keunggulan, antara lain:

1. Dapat meningkatkan produktivitas
2. Dapat meningkatkan kualitas genetik ikan
3. Dapat meningkatkan generasi ikan murni dan unggul.

Dari keunggulan *gynogenesis* mempunyai kelemahan yang selama ini terjadi di lapangan, antara lain:

1. Teknologi digunakan masih sederhana sehingga hasilnya masih jauh dari yang diharapkan.
2. Dalam penggunaan masih banyak menggunakan tenaga manusia dalam pengawasan karena masih terpengaruh dalam *Human error* masih relative tinggi.

Dari kekurangan diatas bagaimana cara meminimalisasikan kesalahan atau kekurangan diatas. Dalam permasalahan yang digambarkan diatas maka perlu

dirancang rangkaian otomatisasi guna menguragi kesalahan dalam proses gynogenesis

.

1.2. Rumusan Masalah

Bagaimana merancang dan membuat alat otomatisasi untuk proses *gynogenesis* pada pembibitan ikan yang bermanfaat dan efisien dengan menggunakan Mikrokontroller ATMEGA8535.

1.3. Batasan Masalah

Penulisan Skripsi ini membahas tentang system bagaimana merancang sebuah alat otomatis dalam gynogenesisi pada pembibitan ikan yang bermanfaat dan efisien menggunakan mikrokontroller ATMEGA8535. Agar permasalahan lebih terfokus pada permasalahan yang dikaji, maka penulis membatasi permasalahan pada hal – hal berikut :

a. Alat yang dibuat berbasis mikrokontroller yang diimplementasikan dengan menggunakan ATMEGA8535
b. Penggunaan sensor suhu sebagai penstabil suhu air dengan mengontrol heater jika suhu air lebih dari 40° C
c. Tidak membahas *power supply*
d. Setiap bagian pengontrolan memasukkan data melalui *keypad*
e. Jenis telur Ikan yang diteliti adalah Ikan mas *(Cyprinus Carpio)* Punten.

f. Pengontrolan alat pada penyinaran radiasi menggunakan UV pada sperma dan saat *shocking* setelah *fertilisasi* pada *sperma* dan *ovum*

1.4. Tujuan

Perencanaan dan pembuatan alat ini bertujuan merencanakan dan membuatan otomatisasi proses gynogenesis pada pepembibitan ikan mas dengan mengontrol sinar UV dan magnetic stirrer, kemudian pengontrol suhu pada bak shock (pengejut) guna memaksimalkan kwalitas benih dibandingkan secara manual.

1.5. Metodologi Penulisan

Guna merealisasikan Tugas akhir sebagai tersebut diatas, maka metodologi penulisanya dilakukan sebagai berikut :

1. Kajian pustaka

   Bertujuan untuk mengumpulkan literatur berisikan teori yang berhubungan dengan perencanaan alat, dipadukan dengan teori yang didapat dibangku kuliah.

2. Perencanaan dan pembuatan alat

   Bertujuan untuk membuat diagram blok rangkaian yang sesuai dengan rencana kerja, yang kemudian direalisasikan dengan melaksanakan perencanaan dan pembuatan alat berdasarkan diagram blok rangkaian yang disusun.

3. Pengujian Alat

Dimaksudkan untuk melakukan analisa dan pengujian alat yang telah dirancang, apakah sesuai dengan fungsi kerja yang diharapkan atau tidak.

4. Penyusunan buku laporan

Bertujuan untuk menyusun data laporan berpedoman pada alat yang selesai dibuat berserta ksimpulan cara kerja dari alat tersebut

1.6.Sistematika Penulisan

Penulisan Skripsi ini terdiri atas 5 bab dengan susunan pembahasan sebagai berikut :

BAB I PENDAHULUAN

Meliputi beberapa uraian tentang latar belakang permasalahan, rumusan masalah, tujuan, batasan masalah, metodologi pembahasan dan sistematika penulisan dan yang mendukung dalam perencanaan pembuatan alat.

BAB II LANDASAN TEORI

Membahas tentang teori dasar yang berisikan teori penunjang dan pendukung sebagai dasar perencanaan dan pembuatan alat yang diajukan pada skripsi ini.

BAB III PERENCANAAN DAN PEMBUATAN ALAT

Pada bab ini membahas tentang perencanaan dan pembuatan perangkat keras, cara kerja serta diagram skematik rangkaian.

BAB IV PENGUJIAN ALAT

Pada bab ini membahas mengenai uji coba sistem, pengamatan pengukuran dan analisa serta kemungkinan pengembangan dari sistem yang telah dibuat.

BAB V PENUTUP

Berisikan tentang kesimpulan dan saran yang didapat selama perencanaan dan pembuatan alat serta kemungkinan pengembangan maupun aplikasi-aplikasi yang dapat dilakukan pada alat yang dirancang bangun.

BAB II

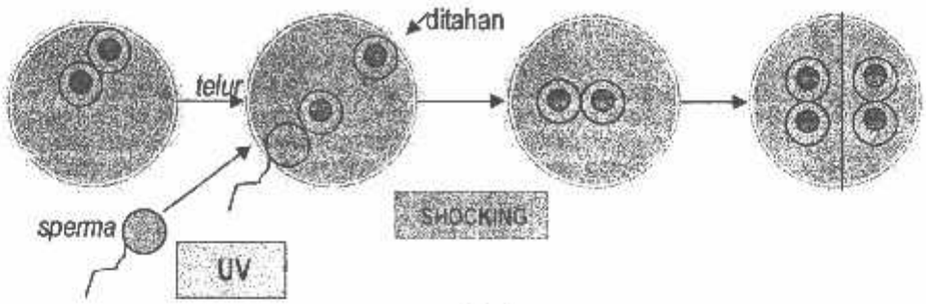
LANDASAN TEORI

2.1. Gynogenesis

Program pemurnian ikan mas dengan cara modern adalah dengan menggunakan metode *gynogenesis*. *Gynogenesis* adalah proses produksi *embrio* dari telur-telur yang dibuahi oleh sperma tanpa sumbangan bahan genetik jantan. Dengan menggunakan metode *gynogenesis* pembuatan populasi *monosex* betina dapat diproduksi dalam dalam satu generasi dan populasi *homozigot "inbreed line"* (ikan murni) dapat diproduksi hanya dalam dua generasi. Sedangkan kalau populasi *homozigot inbreed line* dikombinasikan dengan program seleksi dan *hibridisasi* akan dihasilkan peningkatan kualitas genetik ikan yang dapat dilakukan dalam waktu tiga generasi yang dapat menghasilkan ikan murni dan unggul.

2.1.1. Gynogenesis Meiosis

Apabila sebuah telur normal dibuahi dengan sperma yang diradiasi maka jumlah kromosom di dalam telur akan tetap 2N (kromosom sperma mati), pada proses selanjutnya pada saat sel telur mengalami *meiosis II* dan sebelum terjadi *polar body II* dilakukan kejutan suhu untuk menahan meloncatnya *polar body*. Dengan demikian jumlah kromosom di dalam telur tetap 2N, selanjutnya telur akan mengalami proses *mitosis* dan kemudian berkembang dan menetas menjadi ikan yang mempunyai 2N kromosom

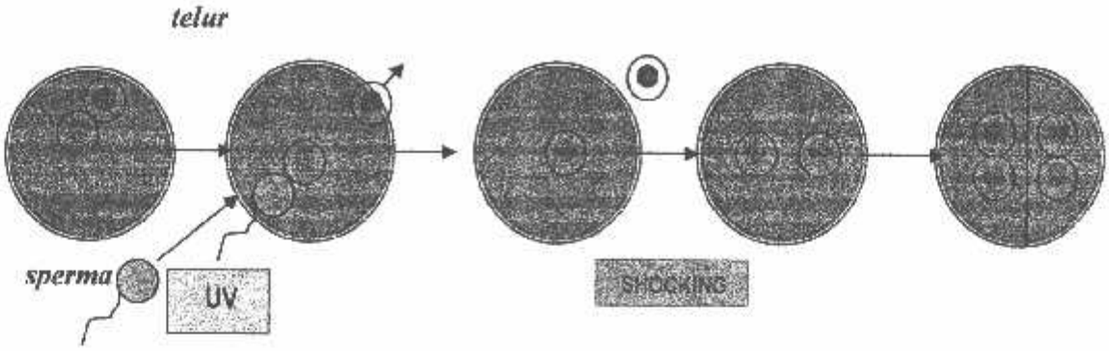


Gambar 2-1[1]
Proses Gynogenesis Meiosis

2.1.2. Gynogenesis Mitosis

Apabila sebuah telur yang normal dibuahi oleh sebuah sperma yang diradiasi maka di dalam telur akan terdapat 2N kromosom yang berasal dari sel telur. Selanjutnya telur akan mengalami *polar body II* sehingga di dalam telur terdapat 1N kromosom. Selanjutnya pada saat sel telur akan mengalami proses mitosis dilakukan kejutan suhu dengan demikian pembelahan hanya terjadi pada kromosomnya saja sedangkan selnya tetap sehingga di dalam sel telur akan terdapat 2N kromosom, kemudian sel akan mengalami mitosis dan selanjutnya menetas menjadi ikan yang mempunyai 2N kromosom.

[1] Optimalisasi waktu kejutan panas *Tetraploid* Ikan mas (*Cyprinus carpio L*),Dinas Perikanan Daerah Jawa Timur Balai Benih Ikan Punten



Gambar- 2-2[2]
Proses Gynogenesis Mitosis

2.2. SENSOR SUHU LM35

Sensor suhu LM 35 ini adalah sensor yang dikemas dalam satu package yang mana merespon perubahan suhu dari suhu -55°C sampai 150°C. Pada spesifikasi alat ini sensor suhu akan menstabilkan suhu 40°C. Dengan perubahan suhu 10mV/°C sensor mengontrol suhu pada bak *shock* (pengejut).

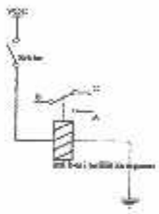
Berikut ini adalah bentuk fisik dan susunan pin – pin dari LM35 yang dapat dilihat pada gambar dibawah ini:

Gambar- 2-3[3]
Bentuk Fisik Sensor Suhu LM35

[2] Optimalisasi waktu kejutan panas *Tetraploid* Ikan mas (*Cyprinus carpio L*),Dinas Perikanan Daerah Jawa Timur Balai Benih Ikan Punten
[3] Datasheet IC LM35, National Semiconductor Corporation, September 1993

2.3. RELAY

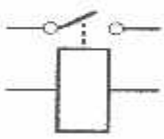
Relay adalah komponen elektronika yang terdiri dari sebuah lilitan kawat (kumparan/koil) yang terlilit pada sebuah besi lunak. Jika kumparan dialiri arus listrik maka inti besi akan menjadi magnet dan menarik pegas sehingga kotak AB terhubung dan BC terputus.



Gambar 2-4[4]
Cara Kerja Relay

Relay merupakan suatu alat untuk menghubungkan atau memerlukan kontak antara komponen yang satu dengan yang lain. Dalam memutus atau menghubungkan kontak digerakkan oleh *fluksi* yang ditimbulkan dari adanya medan magnet listrik yang dihasilkan oleh kumparan yang melilit pada besi lunak. Ada beberapa macam relay, antara lain:

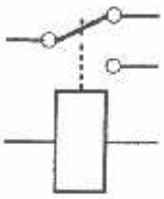
- SPST *(Single Pin Single Terminal)*



Gambar 2-5[5]
Relay SPST

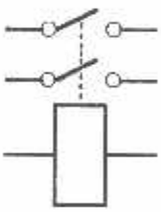
[4] Elektronika Dalam Industri
[5] Elektronika Dalam Industri

- SPDT *(Single Pin Dual Terminal)*



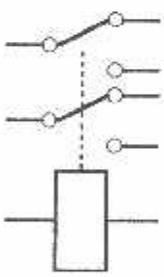
Gambar 2-6[6]
Relay SPDT

- DPST *(Dual Pin Single Terminal)*



Gambar 2-7[7]
Relay DPST

- DPDT *(Dual Pin Dual Terminal)*



Gambar 2-8[8]
Relay DPDT

[6] Elektronika Dalam Industri
[7] Elektronika Dalam Industri
[8] Elektronika Dalam Industri

2.4. Trimpot

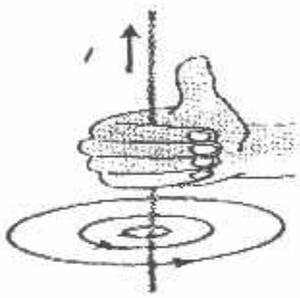
Trimpot termasuk kedalam kelas *variable resistor* yang nilai tahanannya dapat berubah-ubah sesuai dengan letak kontak gesek dengan terminal-terminal ujungnya. Sehingga dapat pula dikatakan bahwa potensiometer memiliki perubahan nilai resistansi sebagai fungsi rotasi kontak gesek. Trimpot dapat dibedakan menjadi dua jenis yaitu jenis linier dan jenis logaritmik. Nilai resistansi potensiometer ditandai dengan huruf A (untuk jenis linier) dan B (untuk jenis logaritmik), misalnya: A5 kΩ, B500 Ω.

Hal-hal yang perlu diperhatikan pada pemilihan Trimpot :

1. Resolusi, adalah perubahan terkecil dalam nilai resistansi yang dapat direalisasikan kalau kontak gesek diputar.
2. Perlawanan ujung, adalah harga perlawanan antara kontak gesek dan terminal-terminal ujung, sementara kontak gesek berada di titik ujung salah satu terminal yang akan diukur nilai resistansinya.
3. Perlawanan kontak, adalah perlawanan antara terminal kontak gesek dan unsur perlawanan yang saling berkontak.
4. Arus kontak-gesek *(wipper current)*, adalah arus maksimum yang boleh mengalir di terminal kontak gesek.
5. Stabilitas setelan *(setting stability)*, adalah kesamaan nilai resistansi pada perulangan *(repeatibility)* suatu setelan potensiometer pada suatu nilai resistansi.

2.5. Motor DC

Didalam teori medan magnet setiap arus yang mengalir melalui sebuah konduktor akan menimbulkan medan magnet. Arah medan magnet dapat ditentukan dengan kaidah tangan kanan. Ibu jari tangan menunjukkan arah aliran arus listrik sedangkan jari-jari yang lain menunjukkan arah medan magnet yang timbul, seperti yang ditunjukkan oleh gambar berikut ini:



Gambar 2-9[9]
Garis-Garis Medan Magnet disekitar Arus Listrik

Kaidah tangan kanan untuk motor menunjukkan arah arus yang mengalir didalam sebuah konduktor yang berada dalam medan magnet. Jari tengah menunjukkan arah arus yang mengalir pada konduktor, jari telunjuk menunjukkan arah medan magnet dan ibu jari menunjukkan arah gaya putar.

Adapun besarnya gaya yang bekerja pada konduktor tersebut dapat dirumuskan dengan :

$$\mathbf{F = B.I.L \sin \theta \quad (Newton)}$$

Dimana :

B = kerapatan *fluks* magnet (weber)

[9] Ir.Sulasno.Dasar Teknik Tenaga Listrik.1990

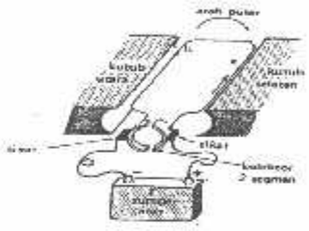
L = panjang konduktor (meter)

I = arus listrik (ampere)

Sin θ = sudut antara antara arus dengan garis-garis medan.

2.5.1. Cara Kerja Motor DC

Adapun cara kerja motor dc dapat dilihat pada gambar dibawah ini:

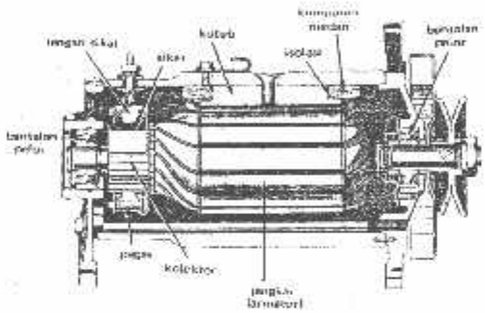


Gambar 2-10[10]
Cara Kerja Motor DC

Ada satu lilit kawat a – b berada di dalam medan magnet. Lilitan ini dapat berputar dengan bebas, lilitan ini bisasa disebut dengan jangkat (*armour*).
Pada jangkar dimasukkan arus yang berasal dari sumber (baterai) E. koneksi baterai dengan jangkar melalui sikat-sikat. Sikat-sikat ini terpasang pada sebuah cincin yang terbelah dua, yang disebut kolektor. Adapun tujuan dari kontruksi ini adalah agar lilitan kawat dapat berputar apabila ada arus listrik yang melewatinya. Pada kawat yang berada di kanan arus mengalir dari depan ke belakang . dalam kawat yang di kiri, arus mengalir dari belakang ke depan . kawat a dan b secara berganti-gantian berada di kiri dan kanan. Karena itu arah arus di a dan arah arus di b selalu membolak-balik. Pembalikan arah arus itu terjadi pada saat lilitan kawat melintasi possisi vertikal. Disini kolektor berfungsi bagaikan penyearah

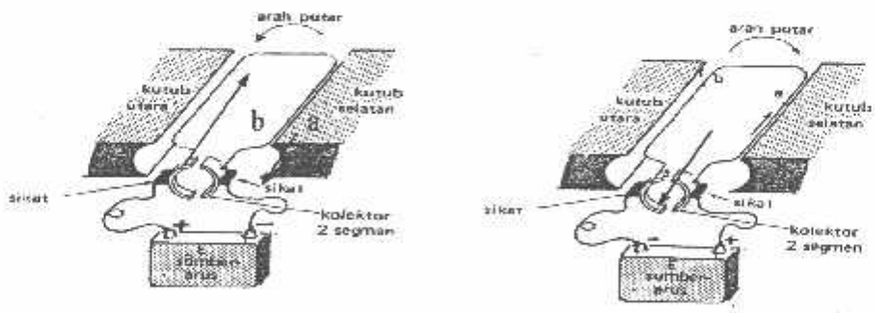
[10] Ir.Sulasno.Dasar Teknik Tenaga Listrik.1990

mekanik. *Flux* magnet yang ditimbulkan magnet permanen disebut medan magnetnya motor. Dalam gambar arah fluk magnetik adalah dari kiri ke kanan. Adapun gaya yang bekerja pada penghantar b adalah ke atas, sementara gaya yang bekerja pada penghantar a adalah ke bawah. Gaya-gaya yang bekerja sama kuatnya, jadi ada kopel yang bekerja pada kawat sehingga lilitan pun dapat berputar. Setelah berputar 90^0 arah arus berbalik, pada saat itu penghantar a dan penghantar b bertukar tempat. Akibatnya arah gerak putaran tidak berubah.



Gambar 2-11[11]
Sebuah Motor DC

2.5.2. Pengendalian Arah Putaran Motor DC



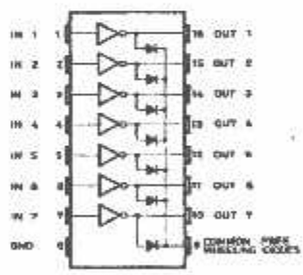
Gambar 2-12[12]
Pengendalian Arah Putaran Motor DC

[11] Ir.Sulasno.Dasar Teknik Tenaga Listrik.1990
[12]Ir.Sulasno.Dasar Teknik Tenaga Listrik,1990

Dari gambar diatas, agar arah putaran motor DC berubah, maka polaritas tegangan pada baterai harus dibalik

2.5.3. Driver Motor

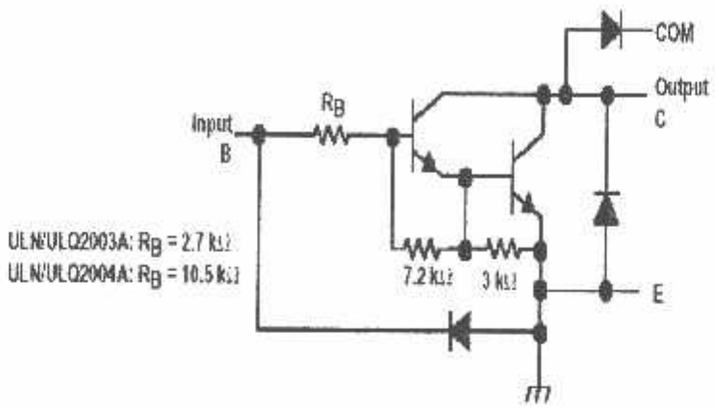
Pada IC ULN 2003A didalamnya terdapat rangkaian penguat Darlington. Untuk satu IC ULN2003A terdapat 7 pasang rangkaian Darlington NPN yang tersusun dalam rangkaian *common catoda*. Rangkaian Darlington ini digunakan sebagai saklar. Pada masing-masing rangkaian Darlington arus kolektornya sebesar 500mA. Rangkaian Darlington yang ada di dalam IC ULN 2003A dapat diparalel guna untuk kebutuhan arus yang besar. Karenanya IC ini dapat diaplikasikan untuk *driver* relay, *driver* lampu, *driver display* dan *logic buffer*. Pada skripsi ini rangkaian Darlington yang ada pada IC ULN 2003A digunakan sebagai *driver relay* yang digunakan untuk mengendalikan putaran motor. Adapun pin-pin koneksi yang ada dalam IC ULN 20003A dapat dilihat pada gambar di bawah ini:



Gambar 2-13[13]
Konfigurasi Pin IC ULN 2003A

[13]Datasheet IC ULN2003A,Texas Instrument Incorporated,Desember 2003

Berikut ini merupakan gambar untuk setiap rangkaian Darlington pada IC ULN 2003A :

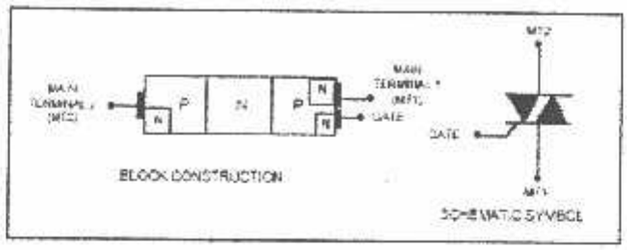


Gambar 2-14[14]
Rangkaian Darlington didalam IC ULN 2003A

2.6. Triac

Triac merupakan komponen semikonduktor dimana tegangan yang dapat melewati adalah tegangan AC yang mendapat control dari *Gate (G)*. Arus yang mengalir melalui terminal utama dan ke terminal ke dua diakibatkan karena bahan semikonduktor tipe N akan semakin besar dan akan mempersempit lebar tipe P yang akan mengakibatkan meloncatnya electron dari terminal satu ke terminal dua, dengan cara pemasangan terminal AC dapat dipasang secara bolak-balik.

[14] Datasheet IC ULN2003A,Texas Instrument Incorporated,Desember 2003



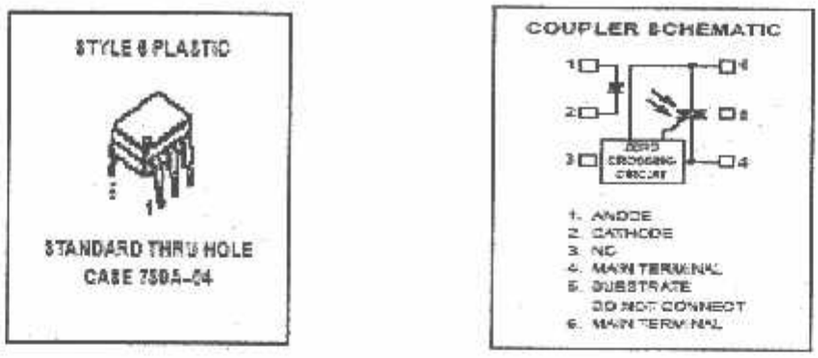
Gambar 2-15[15]
Kontruksi dan Simbol Triac

Gambar 2-16[16]
Konfigurasi Pin Triac

2.7. Optotriac

Optotriac pada dasarnya terdiri dari *phototriac* dan LED (*Light Emiting Diode*) yang digabung dalam satu paket. Bila arus yang mengalir pada LED, sinar yang dikeluarkan akan mengenai basis *phototriac* dan menyebabkan arus mengalir pada triac sehingga kopling ini dapat bekerja sebagai saklar yang akan on.

[15] Tyristor Product Catalog,Teccor Electronics,2003
[16] Tyristor Product Catalog,Teccor Electronics,2003

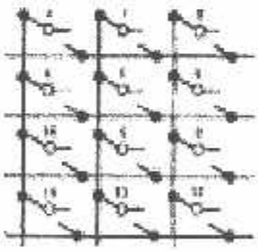


(a) (b)

Gambar 2-17[17]
(a) Bentuk Fisik *Optotriac*
(b) Konfigurasi Pin *Optotriac*

2.7. Keypad

Keypad merupakan komponen yang digunakan sebagai sarana untuk memasukkan data ke komputer atau minimum sistem. Untuk rangkaian *keypad* menggunakan keypad 4 x 4 yaitu 12 buah saklar tekan (*push button*) yang dirangkai dalam bentuk matrik. Gambar rangkaian *keypad* ditunjukkan pada gambar berikut :



Gambar 2-18[18]
Rangkaian Keypad

[17] Datsheet Optpisolators Triac Driver Output, Motorola Semiconductor,1995
[18] Datasheet IC LM74C922, National Semiconductor Corporation, Juli 1993

2.8. LCD (Liquid Cristal Display)

Liquid Cristal Display adalah modul tampilan yang mempunyi konsumsi daya yang relatif rendah dan terdapat sebuah kontroler CMOS didalamnya. Kontroler tersebut berfungsi sebagai pembangkit ROM / RAM dan *display* data RAM. Semua fungsi tampilan dikontrol oleh suatu instruksi, modul LCD dapat dengan mudah diinterfacekan dengan MPU.

LCD yang digunakan dalam Tugas Akhir ini adalah LCD yang memiliki kemampuan sebagai berikut :

- Meliputi 32 karakter yang dibagi menjadi 2 baris dengan *display dot matric* 5 x 7 ditambah *cursor*.
- Karakter generator ROM dengan 192 karakter.
- Karakter generator RAM dengan 8 tipe karakter.
- Dilengkapi fungsi tambahan yaitu *display clear, cursor home, display ON/OFF, cursor ON / OFF, displat character blink, cursor shift* dan *display shift*.
- Internal data.
- 80 x 8 bit display data RAM.
- Dapat diinterfacekan dengan MPU 8 atau 4 bit.
- Internal otomatis dan *reset* pada *power ON*.
- + 5 Volt *power supply* tunggal.

Gambar dibawah ini menunjukkan LCD beserta pin – pinnya :

Gambar 2-19[19]
Bentuk fisik dari LCD

Dimana untuk definisi pin-pin yang terdapat dalam LCD tersebut dapat dilihat pada tabel berikut ini :

Tabel 2.1[20]
Definisi pin-pin LCD

Nama pin	Jumlah	I/O	Tujuan	Fungsi
DB0 – DB3	4	I/O	MPU	Tristate bidirectional lower 4 data bus : data dibaca dari modul ke MPU ditulis ke modul melalui bus.
DB4 – DB7	4	I/O	MPU	Tristate bidirectional upper 4 data bus : data dibaca dari modul ke MPU atau dari MPU ditulis ke modul melaui bus.
E	1	Input	MPU	Sinyal operasi dimulai : sinyal aktif baca/tulis.

[19] Sumber : Seiko Instruments Inc.,LCD Module M1632 User Manual
[20] Sumber : Seiko Instruments Inc.,LCD Module M1632 User Manual

R/W	1	Input	MPU	Sinyal pilih data dan tulis (0 : tulis; 1 : baca).
RS	1	-	Power Supply	Sinyal pilih register : 0 : Instruction register (write) busy flag dan address counter (read) 1 : Data register (write dan read)
V_{LC}	1	-	Power Supply	Penyetelan kontras pada tampilan LCD
V_{DD}	1	-	Power Supply	+ 5 Volt
V_{SS}	1	-	Power Supply	Ground 0 Volt
V_{BL} -	1	-	-	Ground untuk lampu (back light)
V_{BL} +	1	-	-	+ 5 Volt untuk lampu (back light)

2.9. Mikrokontroller ATmega8535L

2.9.1. Teori Dasar Mikrokontroller ATmega8535L

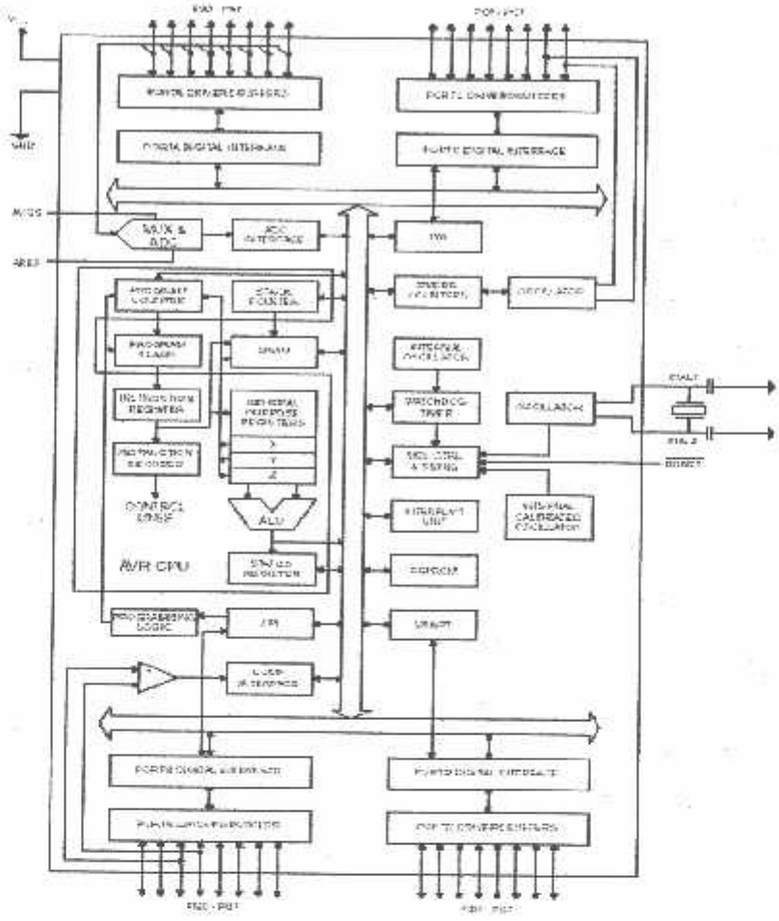
Secara sederhana mikrokontroler merupakan suatu IC yang didalamnya berisi CPU, ROM, RAM dan port I/O yang merupakan kelengkapan sebagai sistem minimum mikrokomputer sehingga sebuah mikrokontroler dapat dikatakan

sebagai mikrokomputer dalam kepingan tunggal (*single chip microcomputer*) yang dapat berdiri sendiri.

Mikrokontroller ATmega8535L merupakan mikrokontrol buatan ATMEL *Inc* yang merupakan mikrokontrol tipe terbaru buatan ATMEL dan memiliki beberapa kelebihan dari pada yang lainnya. Fitur-fitur yang ada pada ATmega8535L antara lain :

- 8 bit CPU (*Cental Proccessing Unit*).
- 8 Kbyte *self-programming flash program memory.*
- *SRAM* berukuran 512 *bytes.*
- *EEPROM* berkapasitas 512 *bytes.*
- Memiliki 32 pin *I/O.*
- Memiliki 8 channel ADC 10 bit.
- *Eksternal* dan *Internal* sumber *interrupt.*
- Programming lock for software security.
- Tegangan operasi 2.7 – 5.5 Volt.
- *Programmable serial USART.*

Arsitektur dasar dari mikrokontriler ATmega8535L dapat dilihat pada gambar dibawah ini :

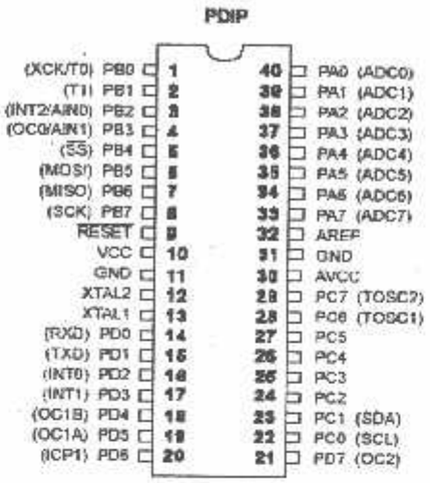


Gambar 2-20[21]
Block Diagram ATmega8535L

2.9.2. Susunan Kaki – kaki ATmega8535L

Berikut ini adalah bentuk fisik dan susunan pin - pin dari ATmega8535L yang dapat dilihat pada gambar dibawah ini :

[21] Data Sheet ATmega8535L, www.atmel.com , atmel AVR corporation, 2003



Gambar 2-21[22]
Konfigurasi pin ATmega8535L

Adapun fungsi dari tiap – tiap pin pada ATmega8535L berdasarkan gambar diatas adalah sebagai berikut :

1. VCC

   Pin – pin ini merupakan pin catu daya dengan level tegangan + 2.7 – 5.5 Volt DC untuk VCC.

2. GND

   Merupakan ground.

3. Port A (PA7 – PA0)

   Port A merupakan input analog untuk ADC, jika ADC tidak digunakan maka port A dapat berfungsi sebagai port I/O dua jalur. Port A merupakan port I/O 8 bit yang dapat menyediakan *internal pull up resistors* dan *buffer* pada outputnya mempunyai *symmetrical drive characteristics*.

[22] Data Sheet ATmega8535L, www.atmel.com , atmel AVR corporation, 2003

Jika PA_0 - PA_7 digunakan sebagai input dan *internal pull up resistors* dalam keadaan aktif maka *external pull low* port ini akan mengalirkan arus.

Selain fungsi diatas, port B juga mempunyai fungsi khusus yang lain seperti berikut :

Tabel 2.2[23]

Fungsi Alternatif dari Pin Port A

Pin	Fungsi Alternatif
PA7	ADC7 (ADC Input Channel 7)
PA6	ADC6 (ADC Input Channel 6)
PA5	ADC5 (ADC Input Channel 5)
PA4	ADC4 (ADC Input Channel 4)
PA3	ADC3 (ADC Input Channel 3)
PA2	ADC2 (ADC Input Channel 2)
PA1	ADC1 (ADC Input Channel 1)
PA0	ADC0 (ADC Input Channel 0)

4. Port B (PB7 – PB0)

Port B merupakan *bi-directional* port I/O 8 bit dengan *internal pull up resistors, buffer* pada output port ini juga memiliki *symmetrical drive*

[23] Data Sheet ATmega8535L, www.atmel.com , atmel AVR corporation, 2003

characteristics. Jika digunakan sebagai input dan jika resistor *pull up* dalam keadaan aktif, maka *external pull low* akan mengalirkan arus.

Selain fungsi diatas, port B juga mempunyai fungsi khusus yang lain seperti berikut :

Tabel 2.3[24]

Fungsi Alternatif dari pin port B

Pin	Fungsi Alternatif
PB7	SCK (SPI Bus Serial Clock)
PB6	MISO (SPI Bus Master Input / Slave Output)
PB5	MOSI (SPI Bus Master Output / Slave Input)
PB4	SS (SPI Slave Select Input)
PB3	AIN1 (Analog Comparator Negative Input)
	OC0 (Time/Counter 0 Output Compare Match Output)
PB2	AIN0 (Analog Comparator Positive Input)
	INT1 (External Interrupt 2 Input)
PB1	T1 (Timer / Counter 1 External Counter Input)
	T0 (Timer / Counter 0 External Counter Input)
PB0	XCK (USART External Clock Input / Output)

[24] Data Sheet ATmega8535L, www.atmel.com , atmel AVR corporation, 2003

5. Port C (PC7 – PC0)

   Port C merupakan port I/O 8 bit dengan *internal pull up resistor*. *buffer* pada output port ini juga memiliki *symmetrical drive characteristics*. Jika digunakan sebagai input, maka *external pull low* akan mengalirkan arus jika resistor *pull up* dalam keadaan aktif.

6. Port D (PD7 – PD0)

   Port D merupakan port I/O 8 bit dengan *internal pull up resistor*. *buffer* pada output port ini juga memiliki *symmetrical drive characteristics*. Jika digunakan sebagai input, maka *external pull low* akan mengalirkan arus jika resistor *pull up* dalam keadaan aktif.

   Selain fungsi diatas, port B juga mempunyai fungsi khusus yang lain seperti berikut :

Tabel 2.4[25]

Fungsi Khusus Dari Port D

Pin	Alternative Function
PD7	OC2 (Timer/Counter2 Output Compare Match Output)
PD6	ICP1 (Timer/Counter1 Input Capture pin)
PD5	OC1A (Timer/Counter1 Output Compare A Match Output)
	OC1B (Timer/Counter1 Output Compare B Match

[25] Data Sheet ATmega8535L, www.atmel.com , atmel AVR corporation, 2003

PD4	Output)
	INT1 (External Interrupt 1 Input)
PD3	INT0 (External Interrupt 0 Input)
PD2	TXD (USART Output Pin)
PD1	RXD (USART Input Pin)
PD0	RXD (USART Input Pin)

7. RESET

   Pin ini adalah untuk input *RESET*.

8. XTAL1

   Merupakan input untuk oscillator *inverting amplifier* dan input untuk *clock* internal pada operasi rangkaian.

9. XTAL2

   Output dari oscillator *inverting amplifier*.

10. AVCC

    Merupakan pin tegangan untuk port A dan ADC. Tegangan ini harus berbeda dengan tegangan VCC, jika ADC tidak digunakan. Dan jika ADC digunakan maka tegangan ini harus disambungkan dengan tegangan VCC melalui sebuah *low-pass filter*.

11. AREF

    Merupakan pin referensi untuk ADC

2.9.3. Organisasi Memori

Organisasi memori pada mikrokontroller ATmega8535L dibagi menjadi dua bagian utama yaitu memori program (*Flash Memori*) dan memori data. Pembagian tersebut didasarkan atas fungsi dari penyimpangan data maupun program. Mikrokontroller ATmega8535L telah dilengkapi dengan EEPROM yang digunakan sebagai media penyimpanan data.

Berikut ini adalah penjelasan memori pada Mikrokontroller ATmega8535L :

- Flash Memory

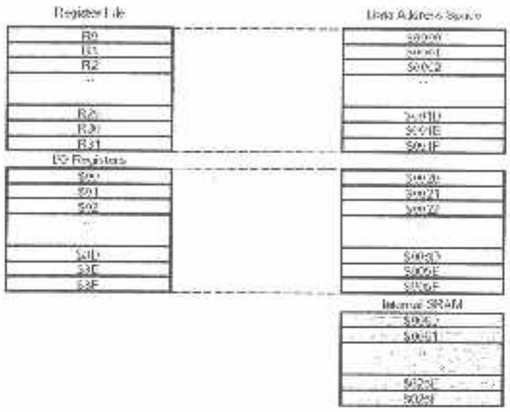
  Mikrokontroller ATmega8535L memiliki 8Kb *System Reprogrammable Flash Memory* untuk penyimpanan data, selama semua instruksi pada MCU ini menggunakan data 16 atau 32 bit maka *Flash Memory* terorganisasi atas 4K x 16. Untuk pengamanan program, *Flash Memory* ini terbagi menjadi 2 bagian yaitu *Boot Program dan Application Program.*

Gambar 2-22[26]
Map Program Flash Memori

[25] Data Sheet ATmega8535L, www.atmel.com , atmel AVR corporation, 2003

❖ Data Memory

Terdapat 608 l;okasi data memori yang dialamatkan pada *register file, I/O memory dan internal data SRAM,* 96 lokasi memori tersebut terletak pada *register file dan I/O memory* sedangkan sisanya terdapat pada *internal data SRAM.*



Gambar 2-23[27]
Map Program Data Memori

2.9.4. Sistem Reset

Mikrokontroller ATmega8535L mempunyai empat (4) sumber reset baik internal maupun eksternal, berikut ini adalah sumber reset dari ATmega8535L :

1. Eksternal Reset

MCU dalam kondisi reset apabila pin *reset* pada pin 9 diberikan sebuah input berupa pulsa low dalam waktu lama.

2. Power-On Reset

MCU akan mereset jika tegangan *power supply* menurun atau berada dibawah tegangan *power-on reset.*

[27] Data Sheet ATmega8535L, www.atmel.com , atmel AVR corporation, 2003

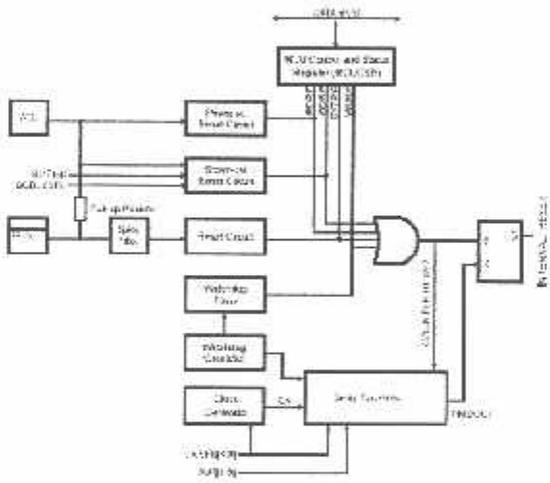
3. Watchdog Reset

MCU akan mereset apabila *watchdog timer* dalam kondisi *enable* dan periodenya telah habis.

4. Brown-Out Reset

MCU akan mereset apabila tegangan power supply Vcc berada dibawah atau mendekati tegangan *brown-out reset* dan ketika *detector brown-out* dalam keadaan *enable*.

Berikut ini akan menjelaskan sistem logika pe-*reset*-an mikrokontroller ATmega8535L :



Gambar 2-24[28]
Logika Reset Mikrokontroller ATmega8535L

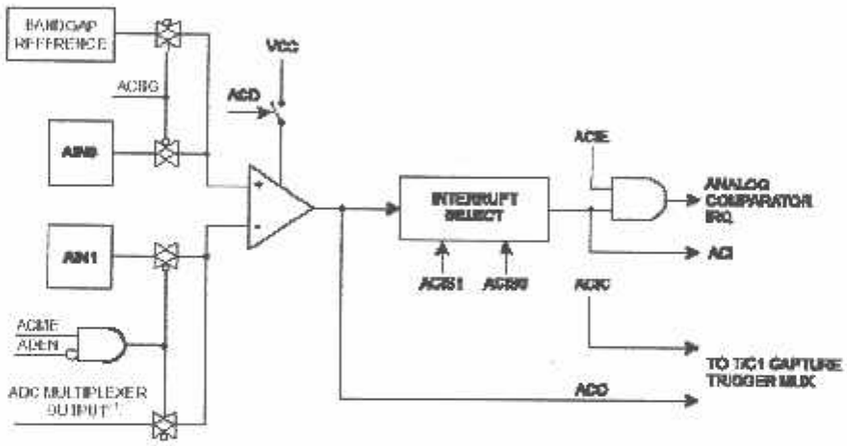
2.9.5. Analog Comparator

Analog Comparator ini akan membandingkan harga input pada pin positif *AIN0* dan pin negatif *AIN1*. Output *analog comparator* (*ACO*) akan berada

[28] Data Sheet ATmega8535L, www.atmel.com , atmel AVR corporation, 2003

dalam Kondisi *set* jika tegangan positif pada pin *AIN0* lebih tinggi dari pada tegangan negatif pada pin *AIN1*.

Output Comparator dapat digunakan men-*set trigger* untuk *timer* atau *counter*. Sebagai fungsi tambahan, *comparator* juga dapat digunakan untuk men-*set trigger* sebuah *interrupt* secara terpisah. Pada proses *intrrupt triggering, user* dapat memilih dua (2) pilihan yaitu *Fall* atau *Toggle* pada setiap kenaikan output dari *comparator*. Blok diagram *analog comparator* dapat dilihat pada gambar dibawah ini :



Gambar 2-25[29]
Blok Diagram Analog Comparator

2.9.6. Analog To Digital Converter (ADC)

Agar dapat mengolah suatu variable fisik yang umumnya berupa besaran analog maka dibutuhkan suatu komponen yang dapat merubah besaran analog

[29] Data Sheet ATmega8535., www.atmel.com , atmel AVR corporation, 2003

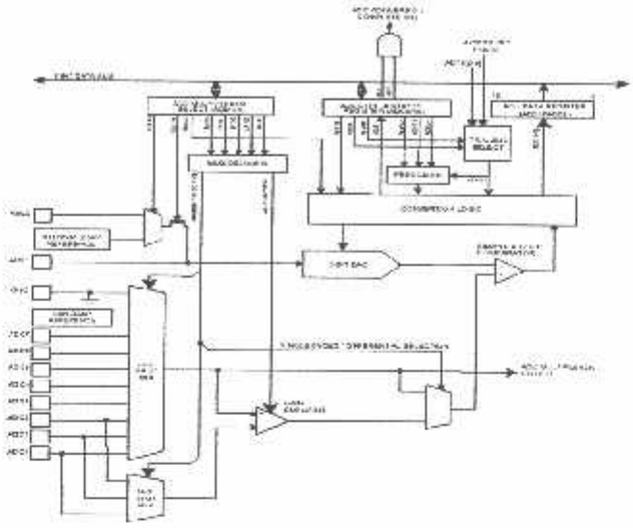
menjadi besaran digital supaya dapat diolah oleh mikrokontroller. Konversi ini dapat dilakukan oleh ADC yang merupakan konverter analog ke digital.

ADC internal pada MCU ATmega8535L ini termasuk tipe SAC (*Successive Approximation ADC*).

Berikut ini adalah fitur – fitur yang dimiliki oleh ADC internal pada MCU ATmega 8535L :

- 10 bit resolusi
- Waktu konversi yang singkat yaitu 65 – 260 µs
- 0.5 LSB *Integral Non-Liniarity*
- ± 2 LSB *Absolute Accuracy*
- 0 – Vcc Range Tegangan Input ADC
- V_{Ref} = 2.56 V
- *Single convertion mode*
- Resolusi maksimum 15 kSPS

Berikut ini adalah blok skematik system pengkonversian dari ADC internal Mikrokontroller ATmega8535L :



Gambar 2-26[30]
Blok Skematik ADC Internal

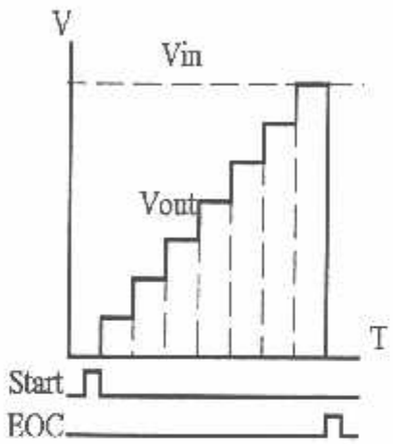
Dalam proses konversi ADC, ada beberapa parameter yang perlu diperhatikan karena parameter ini yang akan menentukan mutu hasil dari pembacaan sebuah ADC, yaitu :

- Kesalahan kuantitatis
- Ketidaklinieran
- Kode tidak lengkap *(missing code)*
- Waktu konversi

Karakteristik yang linier didekati dengan karakteristik dalam bentuk anak tangga sehingga timbul kesalahan kuantitas sebesar setengah dari anak tangga. Karena tinggi anak tangga adalah sama dengan bit paling rendah *(least significant, LSB)* dalam bilangan biner, maka kesalahan tersebut sama dengan ½ LSB. Kadang-kadang kombinasi bit-bit tertentu tidak tersedia, dengan perkataan

[30] Data Sheet ATmega8535L, www.atmel.com , atmel AVR corporation, 2003

lain sebuah tangga dilompati. Kombinasi semacam itu disebut kode yang hilang *(missing code)*. Kode hilang tidak akan terjadi bila kesalahan linieritas kurang dari ± ½ LSB.



Gambar 2-27[31]
Fungsi Linieritas ADC Dalam Bentuk Anak Tangga

Waktu konversi *(convertion time)* adalah waktu yang diperlukan oleh ADC untuk menghasilkan kode biner yang valid. Waktu konversi maksimum dari ADC dapat ditentukan dengan rumus sebagai berikut :

$$T = \frac{2^n}{f} \text{ detik}$$

$$f = \frac{1}{1{,}1RC} \text{ Hz}$$

dimana:

T : waktu konversi maksimum

[31] Data Sheet ATmega8535L, www.atmel.com , atmel AVR corporation, 2003

n : bit konverter

f : frekwensi clock ADC

R : nilai tahanan pada rangkaian clock ADC

C : nilai kapasitansi pada rangkaian clock ADC

Sedangkan untuk perhitungan resolusi dari ADC adalah sebagai berikut :

$$\text{Resolusi} = \frac{Vref}{(2^n - 1)}$$

Dengan:

V_{Ref} = 2,56 V

N = bit resolusi

BAB III

PERANCANGAN DAN PEMBUATAN ALAT

3.1. PENDAHULUAN

Pada bab ini akan dibahas mengenai peralatan yang direncanakan dan akan direalisasikan sebagaimana fungsinya. Adapun perencanaan dan pembuatan alat secara garis besar terdapat 2 (dua) bagian perangkat yang ada yaitu :

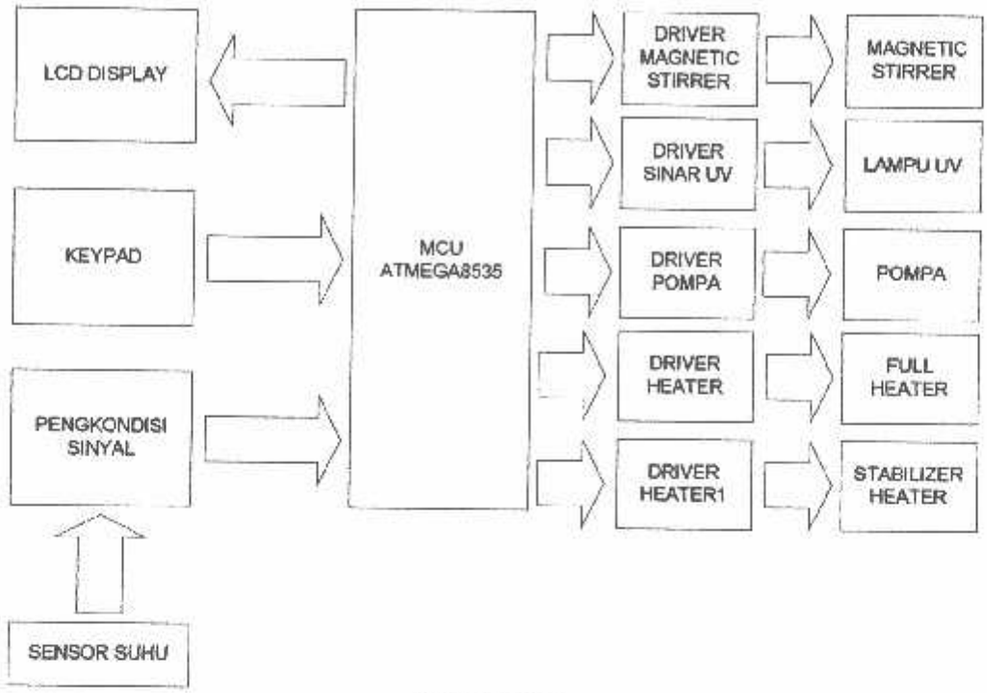
- Perencanaan dan pembuatan perangkat keras (*Hardware*)

  Meliputi penggunaan mikrokontroller, rangkaian sensor suhu, Keypad, dan LCD serta komponen pendukung lainnya.
- Perencanaan dan pembuatan perangkat lunak (*Software*)

Pada perencanaan perangkat keras akan meliputi seluruh periperal yang digunakan pada sistem ini. Pada perencanaan perangkat lunak akan meliputi flowchart dan software secara umum, *software* yang digunakan adalah *Atman Avr* Akan tetapi kedua perangkat tersebut dalam sistem kerjanya akan saling menunjang satu sama lain.

3.2. Perencanaan Blok Diagram

Secara garis besar prinsip kerja alat bagaimana sebuah sistem alat otomatis dalam gynogenesisi pada pembibitan ikan yang bermanfaat dan efisien menggunakan mikrokontroller ATMEGA8535.



Gambar 3-1
Block Diagram Rangkaian

Dari gambar blok diagram diatas, maka dapat dilihat bahwa prinsip kerja dari alat otomatisasi untuk proses *gynogenesis* pada pembibitan ikan yang bermanfaat dan efisien dengan menggunakan Mikrokontroller ATMEGA8535 adalah sebagai berikut :

1. *Keypad* digunakan untuk memasukkan proses yang akn dioperasikan yang diminta dan *keypad* yang digunakan adalah *keypad* matrik 4 x 4.
2. Sensor suhu digunakan untuk mensensor suhu air dalam besaran °C pada proses shocking yang terjadi pada bak shock guna mengontrol respon panas pada full heater dan penyetabil suhu.
3. Pengkondisi sinyal merupakan suatu rangkaian pengolah penguatan sinyal *(amplifier)* dari hasil perubahan dari sensor suhu ke tegangan.

3. Pengkondisi sinyal merupakan suatu rangkaian pengolah penguatan sinyal *(amplifier)* dari hasil perubahan dari sensor suhu ke tegangan.
4. *Driver* pengaduk yang digunakan untuk menggerakkan motor *magnetic stirrer* dimana pada *magnetic stirrer* menggunakan motor DC dengan kecepatan tetap atau dapat diatur melalui *keypad.*
5. Pengaduk digunakan untuk mengaduk atau mencampur sel sperma dan sel ovum.
6. Driver sinar ultraviolet digunakan untuk menyalakan neon ultraviolet dengan sumber tegangan melalui jala-jala listrik
7. Driver motor yang digunakan untuk menggerakkan motor pompa dimana pada motor ini menggunakan motor AC.
8. Pompa ini digunakan untuk meratakan kondisi suhu air agar merata pada bagian pada bak shocking.
9. Driver Heater yang digunakan untuk mengontrol pemanas dimana pada pemanas ini menggunakan full heater.
10. Full heater adalah heater untuk mempercepat pemanasan air pada bak shoking.
11. Driver Heater1 yang digunakan untuk mengontrol pemanas dimana pada pemanas ini menggunakan stabilizer heater.
12. Stabillizer Heater adalah heater untuk menstabilkan suhu air dengan perubahan panas yang sangat lambat dibandingkan dengan full heater.
13. LCD digunakan untuk menampilkan informasi alat yang dioperasikan dari *user* dan waktu yang ditampilkan dan yang diminta oleh *user*.

14. Unit kontrol yang digunakan adalah IC mikrokontroller ATmega8535L. Mikrokontrol ini memiliki ADC yang telah tertanam didalamnya sehingga tidak memerlukan sebuah rangkaian ADC luar dan hasil akhirnya adalah rangkaian minimum sistem akan terlihat lebih praktis.

3.3. Prinsip Kerja Alat.

Pada mulanya alat ini mempunyai dua fungsi yang pertama untuk penyinaran dan shocking (pengejut) suhu. Pertama kali yang digunakan adalah alat penyinaran dengan sinar UV dengan pengoperasian terlebih dahulu masukkan data waktu melalui keypad dan disimpan pada memory internal pada mikrokontroler. Setelah sel sperma dan sel ovum diletakkan pada cawan kemudian diletakkan pada pengaduk dalam kotak peyinaran, dan tekan start untuk memulai pengadukkan dan penyinaran selama seting waktu yang dimasukkan dengan hitungan mundur setelah setelah mencapai nol maka pengadukan dan penyinran selesai. Dengan data penghitungan akan ditampilkan dalam LCD display.

Setelah proses diatas selesai maka dilanjutkan dengan proses shocking (pengejutan) suhu, dengan prosedur yang sama masukkan data waktu dan set suhu pada suhu 40°C dengan tampilan pada LCD display. Pada saat alat kedua diaktifkan maka alat full heat, stabilizer heat, motor pompa akan aktif. Setelah suhu mencapai 40°C, alat dinyatakan siap untuk shocking suhu sel sperma dan sel ovum dengan penghitungan siap dimulai. Pada saat kondisi 40°C sudah dicapai full heat menyala secara berkala untuk menyetabilkan suhu dengan sensor suhu maka kondisi suhu air

dapat dideteksi. Dengan perhitungan mundur bila sudah mencapai hitungan 0 maka alat dinyatakan selesai dan benih diangkat kemudian dipindahkan ke wadah pemijahan dan siap ditetaskan.

3.4. Perancangan Perangkat Keras (Hardware)

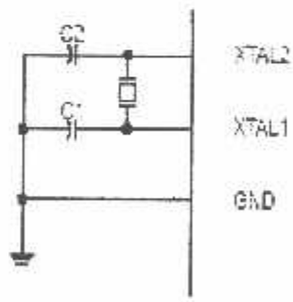
Dalam Skripsi ini, perancangan alat otomatisasi pembenihan ikan nila dengan menggunakan Mikrokontroller ATmega8535L sebagai pengontrol utama, dan menggunakan komponen-komponen lain sebagai komponen pendukungnya.

3.4.1 Perencanaan Rangkaian Mikrokontroller ATmega8535L

3.4.1.1. Perencanaan Rangkaian Clock

Mikrokontroller ATmega8535L memiliki *internal clock* pada pin 12 (XTAL2) dan pin 13 (XTAL1) yang berfungsi sebagai sumber *clock*, dan diperlukan rangkaian tambahan untuk membangkitkan *clock* tersebut.

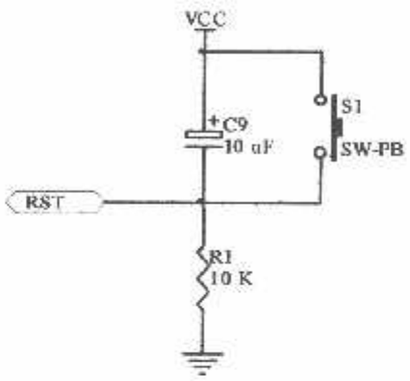
Dalam sistem ini digunakan 2 (dua) buah kapasitor sebesar 10 pF dan kristal 12 MHz, dan gambar rangkaian *clock* dapat dilihat pada gambar 3-2 dibawah ini:



Gambar 3-2
Perencanaan Rangkaian Clock ATmega8535L

3.4.1.2. Perencanaan Rangkaian Reset

Untuk melakukan *reset* sistem pada mikrokontroller dapat memanfaatkan pin *reset*. Pin tersebut dihubungkan dengan rangkaian *reset eksternal* yang ditunjukkan dibawah ini:



Gambar 3-3
Rangkaian Reset Eksternal

Selain menggunakan rangkaian *reset eksternal*, pe-*reset*-an pada MCU ATmega8535L juga dapat dilakukan dengan *internal reset* yang terdiri dari tiga macam cara yaitu :

- Power-On reset

  Mikrokonttroller akan dalam keadaan *reset* jika tegangan *power supply* berada dibawah tegangan ambang *Power-on reset*.

- Watchdog reset

  Mikrokonttroller dalam keadaan me-*reset* jika periode *Watchdog timer* berakhir dan *Watchdog* dalam kondisi *enable*.

- Brown-out reset

  Mikrokonttroller akan dalam keadaan *reset* jika tegangan *power supply* berada dibawah tegangan ambang *Brownout reset* dan detector *Brown-out* dalam kondisi *enable*.

3.4.1.3. Perencanaan ADC

Konverter analog ke digital yang digunakan dalam Skripsi ini adalah ADC internal dari Mikrokontroller ATmega8535L. ADC internal pada mikrokontrol terdapat pada PA0 – PA7. ADC ini merupakan *type ADC 8 bit*.

Untuk Operasi normal ADC dibutuhkan tegangan referensi dengan jangkauan *input analog* mulai dari 0 – 5V.

Karena tegangan yang diukur berubah-rubah maka diharapkan resolusi ADC harus sangat kecil, ADC internal mempunyai $V_{Ref} = 2.56$ V. Sehingga tingkat resolusi ADC internal dapat diketahui sebagai berikut :

$$\text{Resolusi} = \frac{V_{Ke}}{(2^n - 1)}$$

$$\text{Resolusi} = \frac{5}{(2^8 - 1)}$$

$$\text{Resolusi} = \frac{5}{(256 - 1)}$$

$$\text{Resolusi} = 0{,}019 \text{ V}$$

$$\text{Resolusi} = 20 \text{ mV}$$

Dengan kapasitor sebesar 100nF dan resistor Sebesar 10kΩ pada rangkaian *internal clock*, maka frekuensi dapat dihitung sebagai berikut :

$$F = \frac{1}{(1{,}1xRC)}$$

$$F = \frac{1}{(1{,}1x10.10^{3}x100.10^{-9})}$$

$F = 909{,}1$ Hz

$F = 0{,}9091$ KHz

Besarnya waktu konversi maksimum dapat dihitung sebagai berikut :

$$T = \frac{2^{n}}{F}$$

$$T = \frac{2^{10}}{909{,}1}$$

$$T = \frac{1024}{909{,}1}$$

$T = 1{,}126$ detik

ADC internal ATmega8535L merupakan ADC 8 *bit* sehingga didapat nilai ADC dalam kondisi sebagai berikut :

Nilai ADC $= 2^{n} - 1$

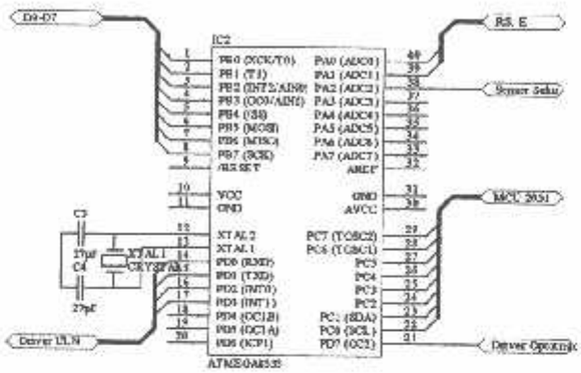
$= 2^{8} - 1$

$= 256 - 1$

$= 255$

3.4.1.4. Perencanaan Penggunaan Port Pada Mikrokontroller ATmega8535L

Mikrokontroller ATmega8535L merupakan mikrokontroller jenis AVR produksi dari Atmel yaitu sebuah *chip* IC yang terdiri dari 40 pin. Berikut ini adalah gambar perencanaan penggunaan port pada mikrokontroller AT8535L :



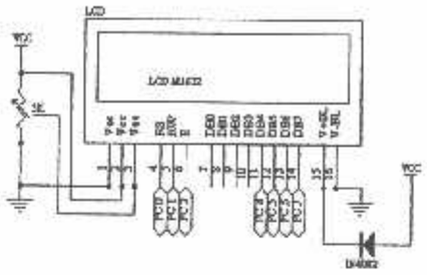
Gambar 3-4

Perencanaan Rangkaian Mikrokontroler

3.4.2. Perencanaan Rangkaian LCD

Untuk tampilan dipergunakan LCD Dot Matrik 2 x 16 karakter. Sinyal-sinyal yang diperlukan oleh LCD adalah *RS dan Enable*, *sinyal RS dan Enable* dipergunakan sebagai *input* yang outputnya dipakai untuk mengaktifkan LCD. LCD akan aktif apabila mikrokontroller memberikan instruksi tulis pada alamat LCD. Saat kondisi *RS don't care dan Enable "0"*, maka LCD tetap pada kondisi semula, pengiriman data ke LCD dilakukan saat RS berlogika "0" dan Enable berlogika "1". Instruksi dikirim pada LCD bila keadaan RS "1" dan Enable "1".

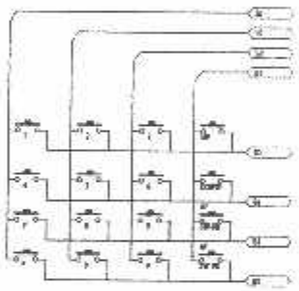
Gambar rangkaian LCD ditunjukkan pada gambar sebagai berikut :



Gambar 3-4
Perencanaan Rangkaian LCD

3.4.3. Keypad

Untuk rangkaian keypad menggunakan 4 x 4 yaitu 4 baris dan 4 kolom. Keypad ini digunakan sebagai inputan untuk operasi jumlah bensin yang diinginkan (dalam liter). Keypad yang digunakan jenis keypad 4 x 4 seperti yang diperlihatkan pada gambar berikut ini :



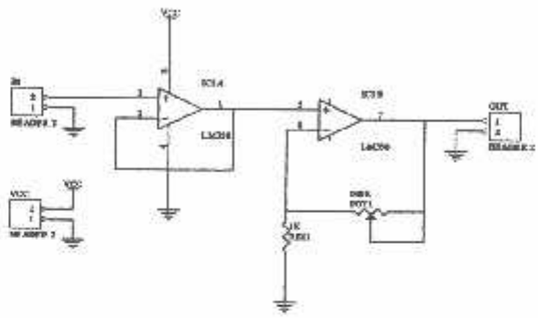
Gambar 3-5
Rangkaian Keypad Matrik 4 x 4

3.4.5. Perencanaan Rangkaian Pengkondisi Sinyal

Pengkondisi sinyal ini digunakan untuk menguatkan keluaran dari sensor suhu LM35 dengan outputan sebesar 10mV/°C dengan *range* suhu -55°C sampai 150°C. Rangkaian ini terdapat *buffer* dan penguat *non inverting* (tak pembalik), jenis

Op-amp yang digunakan yaitu IC dengan tipe LM358 dimana dalam satu IC terdapat dual Op-amp.

Gambar rangkaian pengkondisi sinyal yang digunakan untuk menguatkan tegangan output sensor suhu seperti gambar dibawah ini:



Gambar 3-6

Rangkaian Pengkondisi Sinyal

Pada Op-amp pertama menggunakan Penguat *buffer* digunakan untuk menyangga tegangan agar tidak terjadi penurunan tegangan dengan penguatan :

$$\frac{Vo}{Vi} = 1x$$

Dengan kenaikan 10mV/°C maka dapat dicari nilai Rref sebagai pembanding dalam penguatan :

$$V_0 = (1 + \frac{Rf}{R_1})E_1$$

Karena inputan pada ADC memerlukan 40 mV perstep maka:

$$20mV = (1 + \frac{Rf}{1})10mV$$

$$20mV = 10mV + \frac{10mV.Rf}{1k}$$

$$20mV - 10mV = \frac{10mV.Rf}{1k}$$

$$10mV = 0.0001mV.Rf$$

$$Rf = 1k$$

Range sensor LM35 : -55°C sampai dengan 150°C

Range operasi alat ukur : 25°C sampai 40°C

Karena hasil dari besaran temperatur besaran listrik masih dalam bentuk sinyal-sinyal analog, maka supaya dapat dibaca oleh mikrokontroler harus menggunakan pengubah sinyal analog ke digital/ADC

Tegangan keluaran yang diberikan sensor dan dikuatkan ketika proses pendeteksian temperatur adalah:

Vout = Temp x 20mV/°C

Dengan :

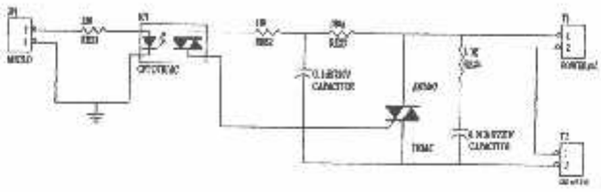
Vout = 40 x 20mV/°C

Vout = 800mV/°C

3.4.5. Perencanaan Rangkaian *Driver Stabilliser Heat*

Driver Stabilliser Heat merupakan rangkaian yang menggunakan Optotriac sebagai pemisah dua catu daya yang berbeda bentuk sinyalnya yang pertama dengan catu daya DC dan yang kedua AC. Dalam penggunaan pompa air menggunakan triac dikarenakan motor pompa menyala dengan berkala, bila menggunakan relay akan mudah rusak diakibatkan karena proses *switching* yang menimbulkan *spark* (bunga api).

Gambar rangkaian *driver Stabilliser heat* guna pengontrolan *heater* dengan pemanasan penuh seperti gambar dibawah ini:



Gambar 3-7

Rangkaian *Driver stabilliser heat*

Dalam perencanaan ini fungsi optotriac digunakan untuk mengisolasi antara kontrol catu daya DC dan AC. Penggunaan kontrol optotriac menggunakan MOC3021 dengan dihubungkan dengan 5V dengan kondisi aktif *low* (0) pada kaki mikrokontroler.

Dengan demikian dapat dicari untuk tahanan LED dengan catu daya V_{led} = 1 V dan I_{led} = 20mA sebagai berikut:

$$R_{led} = \frac{Vcc - V_{led}}{I_{led}}$$

$$R_{led} = \frac{5-1}{20m}$$

$R_{led} = 200\ \Omega$ atau $220\ \Omega$

Pada saat LED pada optotriac berlogika *high* (1) tegangan AC (V_{AC}) yang mengalir sebesar 220V dan Arus *gate* pada Triac (I_{GT}) sebesar 0,5 A, maka dapat dicari besar tahanan R sebagai berikut:

$$R_{AC} = \frac{V_{AC}}{I_{GT}}$$

$$R_{AC} = \frac{220V}{1}$$

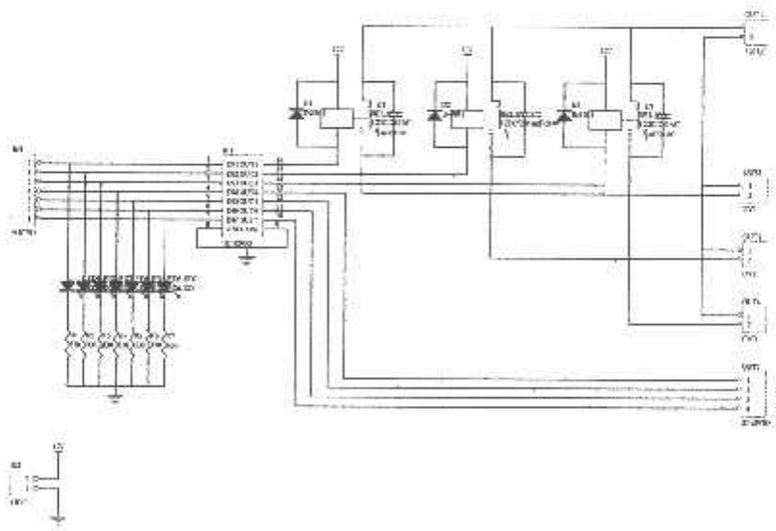
$R_{AC} = 220\,\Omega/1\text{W}$

Jadi untuk pemasangan R terpasang 220 Ω dengan daya 1 W

3.4.5. Perencanaan Rangkaian Driver Relay dan Switcing Motor DC

Driver sinar Ultraviolet, stabillizer heat, dan motor pompa merupakan rangkaian dengan menggunakan IC ULN2003A yang difungsikan sebagai saklar. *Relay* akan aktif apabila ada *output* dari ULN2003A berupa *logic high* atau "1". Sedangkan motor pengaduk menggunakan catu daya DC 12 V langsung ke ULN2003 sebagai pengontrol swicthing. Sinyal penggerak *driver relay* dan switching motor DC ini adalah keluaran dari port

Rangkaian *driver relay* dan motor DC yang digunakan untuk mengendalikan alat tersebut adalah sebagai berikut :



Gambar 3-8
Rangkaian Driver ULN2003

Untuk perhitungan R pada indikator dimana LED memerlukan $I_{led} = 20\text{mA}$ dan $V_{led} = 1\text{V}$

Sebagai berikut:

$$R_{led} = \frac{Vcc - V_{led}}{I_{led}}$$

$$R_{led} = \frac{5-1}{20m}$$

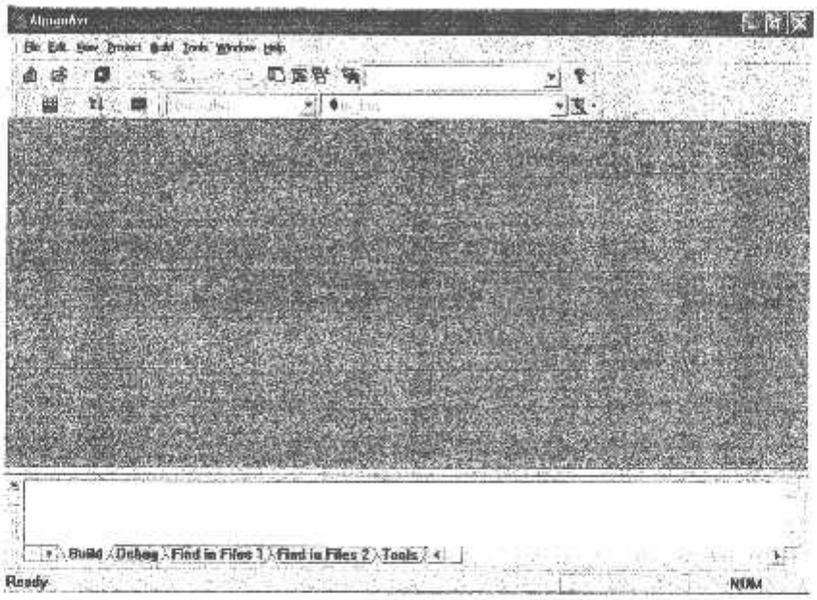
$R_{led} = 200\ \Omega$ atau $220\ \Omega$

3.6. Perancangan Software

Agar sistem dapat bekerja dengan semestinya maka diperlukan software (perangkat lunak) menggunakan AtmanAVR V5.5 yang akan mengatur kerja dari keseluruhan sistem.

Urutan kerja dalam penggunaan program Atman AVR V5.5 dapat dijelaskan sebagai berikut :

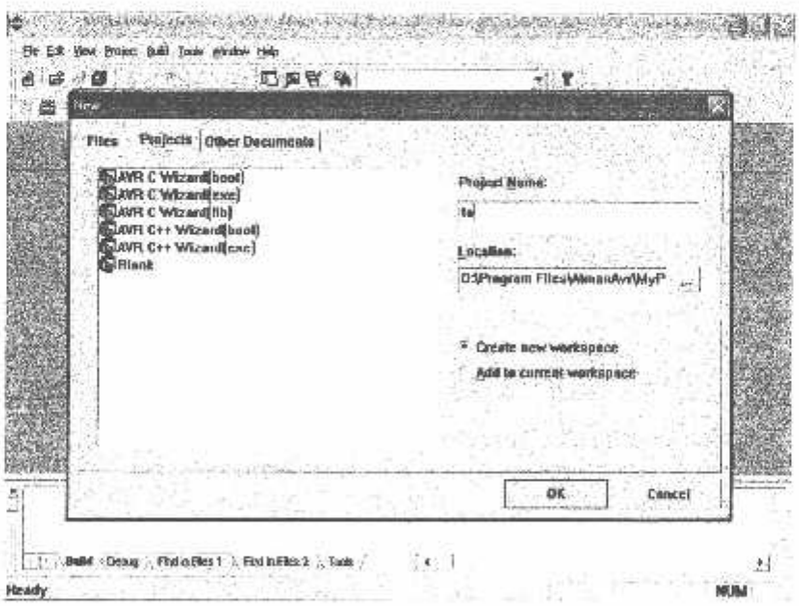
1. Install Program *Atman AVR V5.5* beserta *Up date* nya
2. Buka Program *Atman AVR V5.5*



Gambar 3-9
Layar kerja Atman V5.5

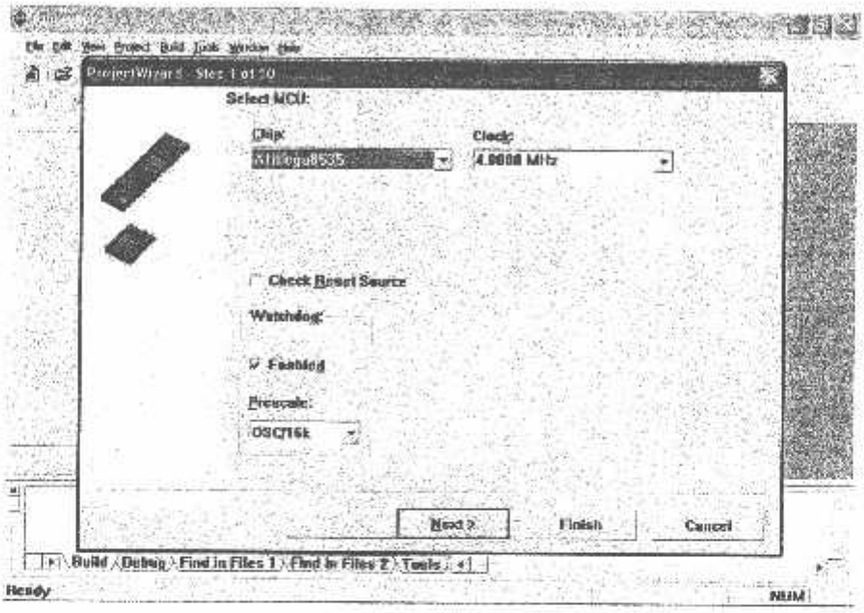
3. Buka *Toolbar File* Pilih *New* enter

   - Pilih *AVR Wizard(exe)*
   - Isi *Project Name* tekan *OK*



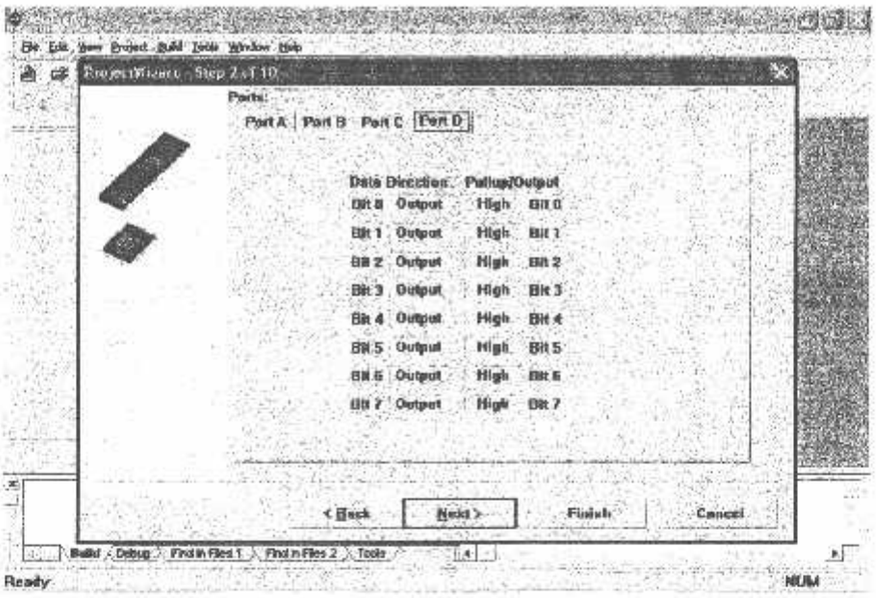
Gambar 3-10
Layar kerja New Atman V5.5

4. Kemudian pada *Project wizard step 1 of 10* Pilih *chip, prescale* dan *clock* yang digunakan



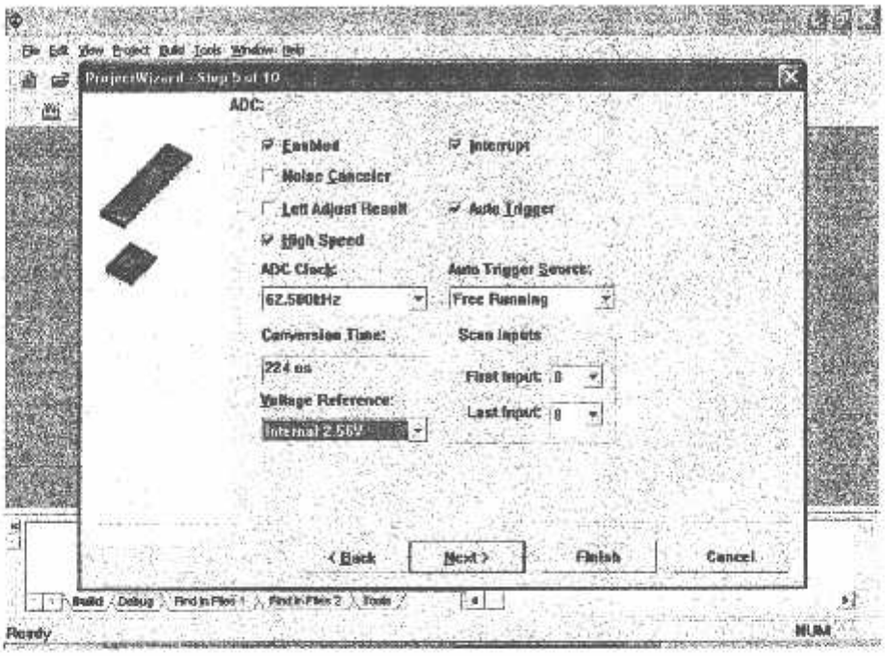
Gambar 3-11
Layar kerja Projectwizard step 1 of 10 Atman V5.5

5. Kemudian pada *Project wizard step 2 of 10* Pilih *Pin I/O* yang digunakan sesuai penggunaan



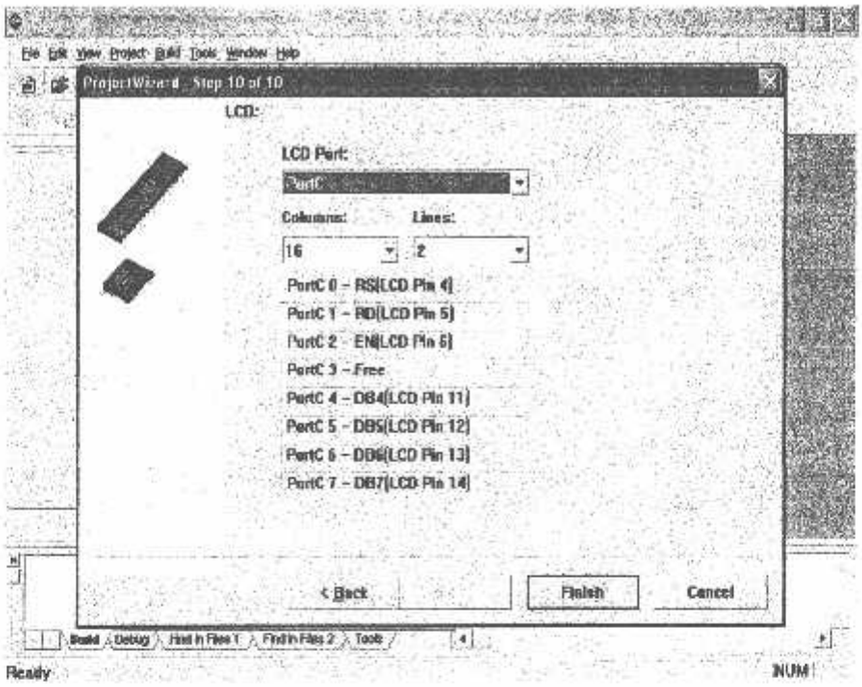
Gambar 3-12
Layar kerja Projectwizard step 2 of 10 Atman V5.5

6. Kemudian pada *Project wizard step 5 of 10* Pilih *enable* jika ADC digunakan dan tampil pilihan:
   - Pilih *Auto trigger* kemudian *free running scan input* sebagai pin kaki *microcontroller* yang digunakan sebagai *input ADC*
   - Pilih *High Speed* dan pilih *speed frequency* yang digunakan
   - Pilih *Voltage reference* dengan memilih internal 2,56 V



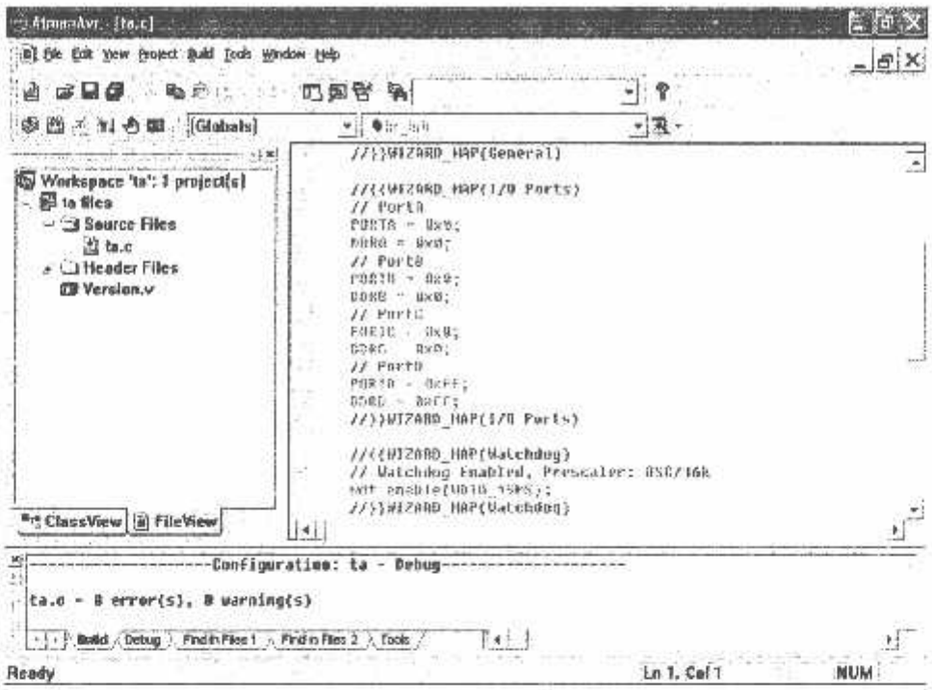
Gambar 3-13
Layar kerja Projectwizard step 5 of 10 Atman V5.5

7. Kemudian pada *Project wizard step 10 of 10* Pilih *LCD Port* yang digunakan akan tampil :
   - *Columns* pada LCD pilih 16 jika LCD yang digunakan *LCD 16 Column.*
   - *Lines* pada LCD pilih 2 jika LCD yang digunakan *LCD 16 line.*



Gambar 3-14
Layar kerja Projectwizard step 10 of 10 Atman V5.5

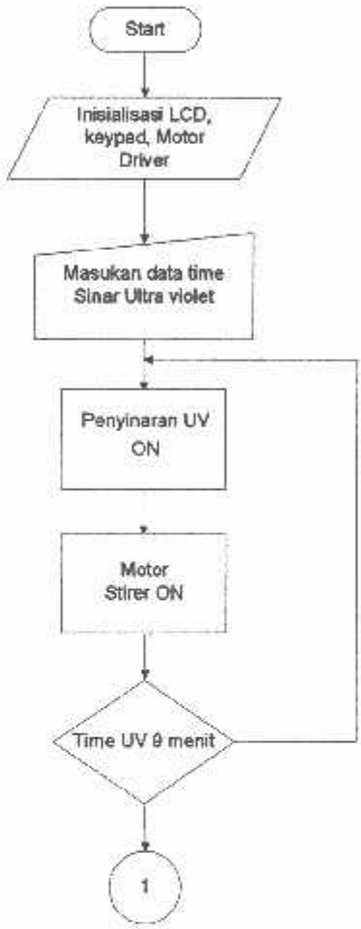
8. Kemudian siap menuliskan program
9. Untuk mengecek penulisan program pilih *Build* pada toolbar Jika laporan pada *build 0 error(2), 0 warning(s)* berarti tdk ada kesalahan

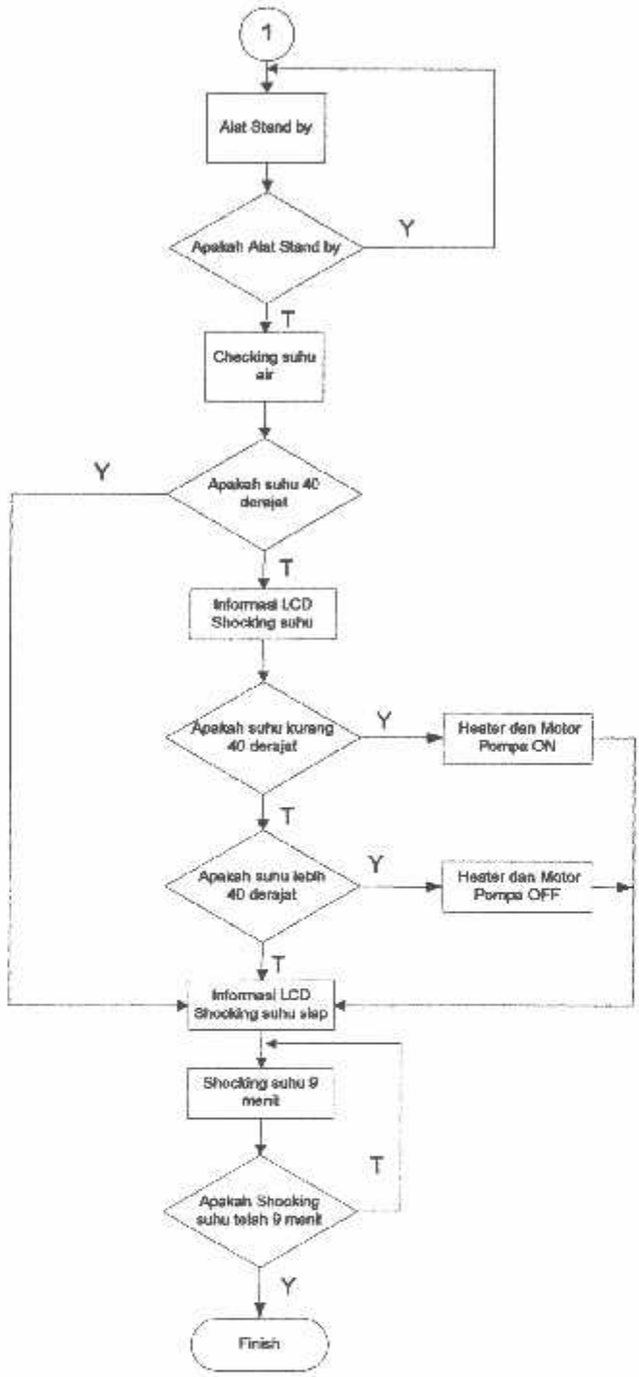


Gambar 3-15
Layar kerja Program Atman V5.5

Urutan kerja dari keseluruhan sistem dapat dijelaskan dalam *flowchart* sebagai berikut

Diagram Penyinaran Ultraviolet




1
Alat Stand by
Apakah Alat Stand by
Y
T
Checking suhu air
Apakah suhu 40 derajat
Y
T
Informasi LCD Shocking suhu
Apakah suhu kurang 40 derajat
Y
Heater dan Motor Pompa ON
T
Apakah suhu lebih 40 derajat
Y
Heater dan Motor Pompa OFF
T
Informasi LCD Shocking suhu siap
Shocking suhu 9 menit
Apakah Shocking suhu telah 9 menit
T
Y
Finish

BAB IV

PENGUJIAN ALAT

Untuk mendapatkan hasil yang maksimal setelah melakukan perencanaan dan pembuatan alat, maka perlu dilakukan pengujian terhadap alat yang telah dibuat. Pengujian pada alat ini dibagi menjadi dua bagian, yaitu pengujian untuk kerja perangkat keras dan pengujian keseluruhan. Pengujian ini bertujuan untuk mengetahui apakah alat yang telah dibuat dapat berkerja sesuai dengan yang diinginkan.Bagian –bagian yang perlu diuji pada alat ini meliputi :

1. Pengujian kerja perangkat keras
    - Pengujian IC LM35
    - Pengujian penguatan *non inverting* dan *buffer*
    - Pengujian *driver Heater Full*, motor pompa AC, *Ultraviolet*
    - Pengujian *driver Heater Stabilleser*
    - Pengujian *driver* Motor Stirrer.
    - Pengujian *Timer*
2. Pengujian Alat terhadap hasil Pembenihan Ikan

4.1. Pengujian IC LM35

4.1.1.Tujuan

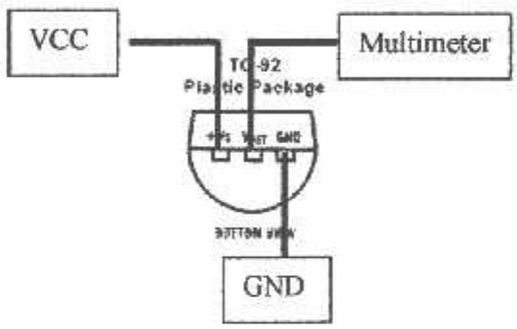
Sensor suhu menggunakan IC LM 35 dugunakan unutk memonitoring perubahan suhu yang terjadi pada bak shocking suhu selama 90 detik. Perubahan sensor suhu adalah 10 mV/°C dimana dengan batasan antara range suhu -55°C sampai dengan 150°C.

4.1.2. Peralatan yang digunakan

1. Catu daya supply 5V
2. Termometer
3. Sensor suhu IC LM35

4.1.3.Langkah-langkah Pengujian

1. Menyambungkan sensor suhu pada pin 1 dihubungkan dengan sumber tegangan, Vout dihubungkan dengan multi meter dan pin 3 dihubungkan dengan Gnd



Gambar 4-1
Rangkaian Pengujian Sensor IC LM35

2. Meletakkan thermometer sebagai pembanding.
3. Memanaskan sensor suhu
4. Hasil pengujian sensor suhu IC LM 35 adalah sebagai berikut :

Tabel 4-1
Tabel pengukuran suhu dan tegangan pada sensor LM 35

NO	Vdc	Tampilan Suhu	
		Thermometer	LCD display
1	25	24.5	25
2	26	25.5	26

3	27	26.5	27
4	28	27.5	28
5	29	28.5	29
6	30	29.5	30
7	31	30.5	31
8	32	31.5	32
9	33	32.5	33
10	34	33.5	34
11	35	34.5	35
12	36	35.5	36
13	37	36.5	37
14	38	37.5	38
15	39	38.5	39
16	40	39.5	40

Gambar 4-2
Tampilan Suhu pada LCD

Dari data pada tabel pengamatan dengan termometer dan dengan *LCD display* menggunakan IC LM35 didapat persentase *Error* adalah sebagai berikut :

$$\%\,Error = \frac{25-24{,}5}{25} x100\%$$

$$= \frac{0{,}5}{25} x100\%$$

$$= 2\,\%$$

$$\%\,\text{Ketelitian} = 100\% - \%\,Error$$

$$= 100\% - 2\,\%$$

$$= 98\%$$

4.1.4. Kesimpulan

Suhu yang ditampilkan pada LCD dan dibandingkan dengan termometer mempunyai tingkat prosentasi ketelitian sebesar 98% dan prosentasi kesalahan sebesar 2%

4.2.Pengujian Penguat *Non Inverting* dan *Buffer.*

4.2.1. Tujuan

Pengujian pada penguatan *non inferting* sangat diperlukan guna menguatkan tegangan rendah yang dihasilkan oleh sensor suhu agar dapat direspon oleh *ADC internal* pada mikrokontroler.

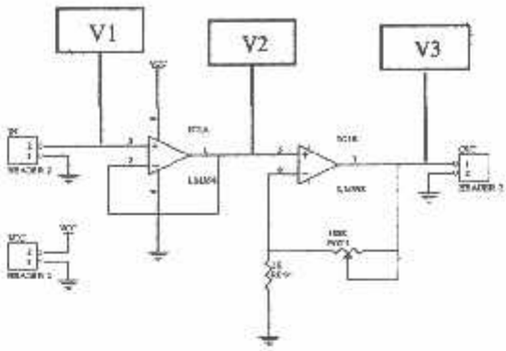
Untuk pengujian *buffer* berguna untuk menyangga tegangan hasil dari sensor suhu tidak drop atau turun akibat dari hambatan dalam pada rangkaian karena sangat berpengaruh pada penguatan.

4.2.2. Peralatan yang digunakan

1. Sensor suhu IC LM 35
2. Multimeter Digital
3. Catu daya DC 5 volt.
4. Thermometer

4.2.3. Langkah Pengujian

1. Membuat rangkaian IC ULN2003A sebagai saklar *relay* seperti gambar berikut:



Gambar 4-3
Rangkaian Penguat *Buffer* dan *Non Inverting* Sensor IC LM35

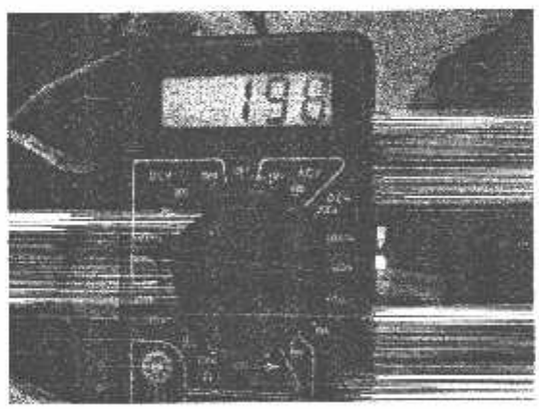
4. Menghubungkan IC LM 358 ke sumber tegangan 5 VDC
5. Memanaskan sensor suhu.
6. Mengukur tegangan pada titik V1,V2, dan V3
7. Hasil pengujian rangkaian penguat *non inverting* dan *buffer* adalah sebagai berikut:

Tabel 4-2
Tabel hasil percobaan I/O LM 358

NO	Suhu	Perhitungan pada I/O LM358			Pengukuran pada I/O LM358		
		V1 (Volt)	V2 (Volt)	V3 (Volt)	V1 (Volt)	V2 (Volt)	V3 (Volt)
1	25	0.2	0.2	0.24	0.2	0.201	0.244
2	26	0.201	0.201	0.28	0.201	0.202	0.285
3	27	0.202	0.202	0.32	0.202	0.203	0.326
4	28	0.203	0.203	0.36	0.203	0.204	0.367
5	29	0.204	0.204	0.4	0.204	0.205	0.408
6	30	0.205	0.205	0.44	0.205	0.206	0.449
7	31	0.206	0.206	0.48	0.206	0.207	0.49
8	32	0.207	0.207	0.52	0.207	0.208	0.531
9	33	0.208	0.208	0.56	0.208	0.209	0.572
10	34	0.209	0.209	0.6	0.209	0.21	0.613
11	35	0.21	0.21	0.64	0.21	0.21	0.654

12	36	0.211	0.211	0.68	0.211	0.211	0.695
13	37	0.212	0.212	0.72	0.212	0.212	0.736
14	38	0.213	0.213	0.76	0.213	0.213	0.777
15	39	0.214	0.214	0.8	0.214	0.214	0.818
16	40	0.215	0.215	0.84	0.215	0.215	0.859

Gambar 4-4
Tampilan tegangan *output* setelah penguatan pada multimeter



Gambar 4-5
Tampilan tegangan input sebelum penguatan pada multimeter

Dari data pada tabel tegangan penguat output *buffer* dan tegangan *output non inverting* dengan menggunakan IC LM358 didapat persentase *Error* adalah sebagai berikut :

1. Error pada penguat *buffer*

$$\%\ Error = \frac{0.201 - 0.200}{0.200} x100\%$$

$$= \frac{0{,}001}{0.200} x100\%$$

$$= 0{,}5\ \%$$

% Ketelitian = 100% - % *Error*

= 100% - 0.5 %

= 99,5%

2. Error pada penguat *non inverting*

$$\%\ Error = \frac{0.244 - 0.240}{0.240} x100\%$$

$$= \frac{0{,}004}{0.240} x100\%$$

$$= 1.67\ \%$$

% Ketelitian = 100% - % *Error*

= 100% - 1.67%

= 98,3%

4.2.3. Kesimpulan

Dari data dan keterangan diatas bahwa penguat *non inverting* dapat menguatkan sinyal dengan daya tidak melebihi sumber tegangan dan *buffer* berfungsi untuk menyangga tegangan agar tidak terjadi penurunan tegangan akibat beban dari komponen lain. Pada penguat buffer mempunyai prosentase tingkat kesalahan sebesar 0,5% dan prosentase tingkat ketelitian sebesar 99,5%.

Sedangkan untuk penguat non inverting tingkat kesalahan sebesar 1,67% dan prosentase tingkat ketelitian sebesar 98,3%.

4.3. Pengujian IC ULN2003A Sebagai *Driver relay*

4.3.1. Tujuan

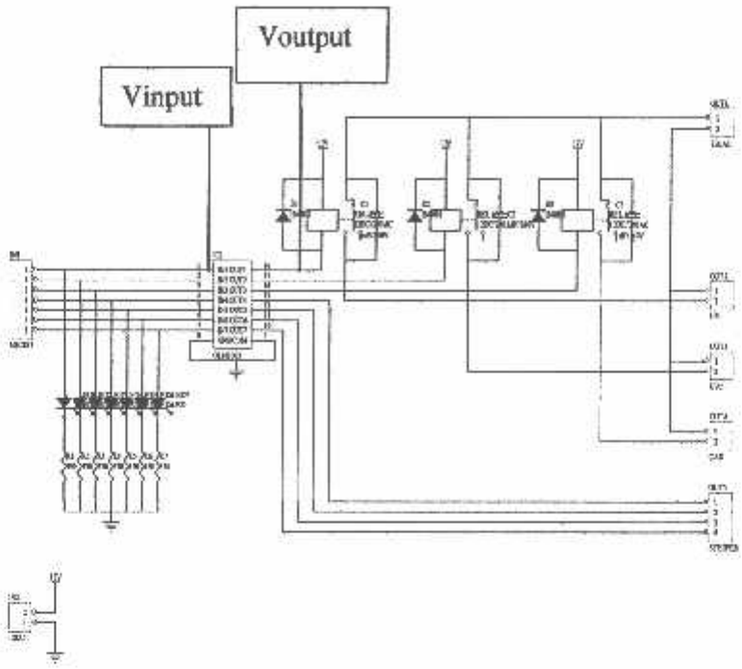
Pengujian *driver relay* bertujuan untuk mengetahui IC ULN2003A yang berfungsi sebagai *driver relay* untuk *heater full*, lampu *ultraviolet*

4.3.2. Peralatan Yang Digunakan

1. Heater full, Ultraviolet,
2. Rangkaian IC ULN2003A sebagai driver relay
3. Multimeter.
4. Catu daya DC 5 volt dan 12 volt.
5. Catu daya AC 220 volt

4.3.3. Langkah-langkah Pengujian

1. Membuat rangkaian IC ULN2003A sebagai saklar relay seperti gambar berikut :



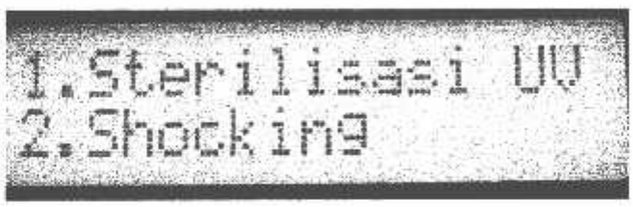
Gambar 4-6

Rangkaian pengujian Driver relay

2. Menguhubungkan rangkaian IC ULN 2003A sebagai driver relay ke catu daya 12 Volt DC.
3. Menghubungkan relay dengan catu daya 220 Volt AC.
4. Memberikan logika *control* berupa logika *high* dan logika *low* pada input rangkaian IC ULN2003A.
5. Hasil Pengujian rangkaian *driver relay* adalah sebagai berikut

Tabel 4-3
Data Hasil Pengujian IC ULN2003A Sebagai *Driver Relay*

V_{input} (Volt)	V_{out} (Volt)		Kondisi relay
	Perhitungan	Pengukuran	
5	0	0,12	OFF
0	12	11,6	ON

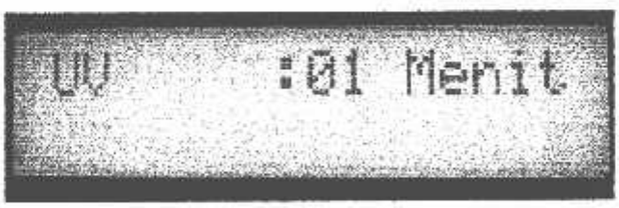


Gambar 4-7

Tampilan pilihan pada LCD

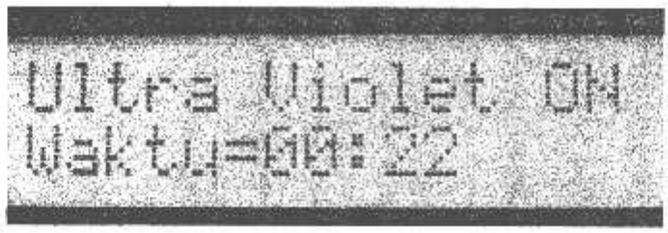
Gambar 4-8

Tampilan awal pada waktu *UV* dan *Motor Stirrer* pada LCD



Gambar 4-9

Tampilan pada waktu *UV* dan *Motor Stirrer* bekerja pada LCD



Gambar 4-10

Tampilan pada waktu *UV* bekerja pada LCD

Dari data pada tabel tegangan output driver heater dengan menggunakan IC ULN2003A didapat persentase *Error* adalah sebagai berikut :

$$\%\ Error = \frac{12-11,6}{12} x100\%$$

$$= \frac{0,4}{12} x100\%$$

$$= 3,3\ \%$$

% Ketelitian = 100% - % *Error*

= 100% - 3,3 %

= 96,7%

4.3.4. Kesimpulan

Dari keterangan diatas dapat disimpulkan bahwa IC ULN2003A merupakan driver relay yang dapat digunakan mengontrol swiching, tergantung pada logika *input* yang diberikan dengan tingkat kesalahan sebesar 3,3% dan tingkat ketelitian 96,7%.

4.4. Pengujian *Driver Heater Stabilliser*

4.4.1. Tujuan

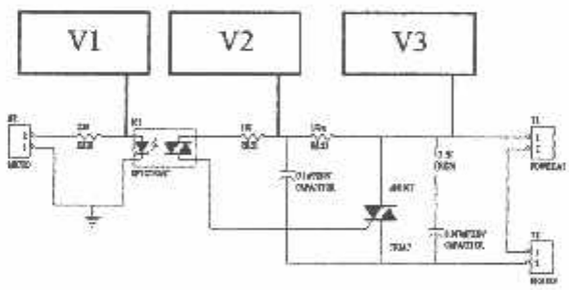
Pada penggunaan driver Motor AC bertujuan untuk meratakan sirkulasi suhu air pada saat shocking selama 90 detik. Jadi pengontrolan kecepatan dapat diatur mengunakan *keypad* dan yang diatur adalah *delay* program.

4.4.2.Peralatan yang digunakan

1. Rangkaian *Driver Triac*
2. Multimeter.
3. Catu daya DC 12 volt.
4. Catu daya AC 220 volt
5. *Heater*

4.4.3.Langkah Pengujian

1. Membuat rangkaian *Driver Triac* sebagai saklar *relay* seperti gambar berikut :



Gambar 4-11

Rangkaian pengujian *Driver Heater Stabilliser*

2. Menghubungkan masukan pada V1 dengan memberi tegangan 5VDC
3. Mengubungkan masukan pada V3 dengan memberi tegangan 220VDC
4. Menghubungkan titik-titik V1,V2,dan V3 pada multimeter
5. Memberikan logika *control* berupa logika *high* dan logika *low* pada input rangkaian IC ULN2003A
6. Hasil Pengujian rangkaian *driver relay* adalah sebagai berikut:

Tabel 4 - 4

Data Hasil Percobaan driver Triac

No	Perhitungan	Pengukuran
	Arus (A)	Arus (A)
1	1	0,6

Dari data pada tabel tegangan output triac dengan menggunakan Q4004 didapat persentase *Error* adalah sebagai berikut :

$$\%\,Error = \frac{1-0,6}{1} x100\%$$

$$= \frac{0,4}{1} x100\%$$

$$= 40\%$$

$$\%\,\text{Ketelitian} = 100\% - \%\,Error$$

$$= 100\% - 40\ \%$$

$$= 60\%$$

4.4.4. Kesimpulan

Pada pengaturan suhu agar stabil menggunakan triac karena pada *swicthing* yang terjadi saat logic High (1) dan Low (0) pada penggunaan swicting

swicting saat aman menggunakan triac dibandingkan dengan relay. Dengan Prosentasi error 40% dengan ketelitian 60%.

4.5. Pengujian IC ULN2003A Sebagai Driver Motor Stirrer DC

4.5.1.. Tujuan

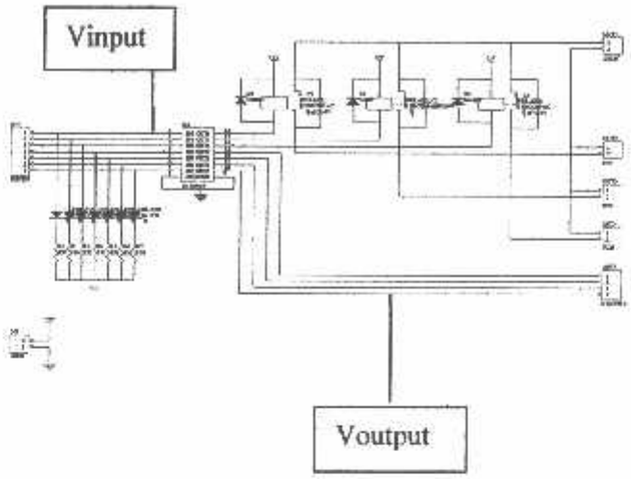
Pengujian driver motor Stirrer bertujuan untuk mengetahui IC ULN2003A yang berfungsi sebagai driver stirrer (pengaduk) sperma dan ovum

4.5.2. Peralatan Yang Digunakan

1. Motor DC
2. Rangkaian IC ULN2003A sebagai driver motor
3. Multimeter.
4. Catu daya DC 5 volt dan 12 volt.

4.5.3. Langkah-langkah Pengujian

1. Membuat rangkaian IC ULN2003A sebagai saklar motor seperti gambar berikut :



Gambar 4-12

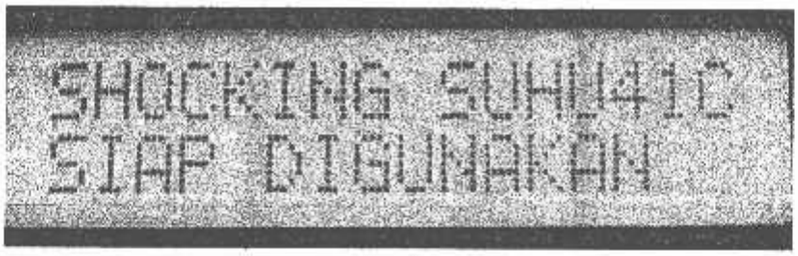
Rangkaian pengujian Motor Stirrer

2. Menguhubungkan rangkaian IC ULN 2003A sebagai driver motor ke catu daya 12 Volt DC.
3. Memberikan logika *control* berupa logika *high* dan logika *low* pada input rangkaian IC ULN2003A.
4. Hasil Pengujian rangkaian driver motor adalah sebagai berikut

Tabel 4-5

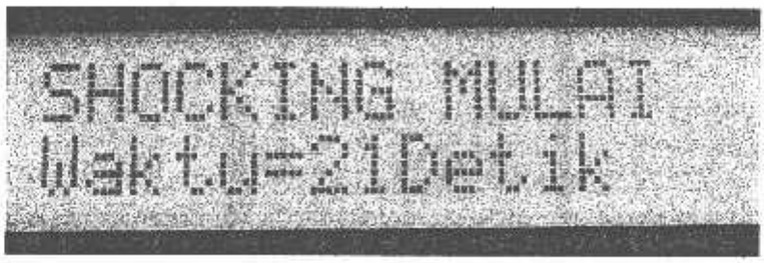
Data Hasil Pengujian IC ULN2003A Sebagai Driver motor

V_{input} (Volt)	V_{out} (Volt)		Kondisi motor
	Perhitungan	Pengukuran	
5	0	0,12	OFF
0	12	11,6	ON



Gambar 4-13

Tampilan pada waktu shocking suhu siap bekerja pada LCD



Gambar 4-14

Tampilan pada waktu shocking suhu bekerja pada LCD

Dari data pada tabel tegangan output driver motor dengan menggunakan IC ULN2003A didapat persentase *Error* adalah sebagai berikut :

$$\%\ Error = \frac{12 - 11{,}6}{12} x100\%$$

$$= \frac{0{,}4}{12} x100\%$$

$$= 3{,}3\ \%$$

$$\%\ \text{Ketelitian} = 100\% - \%\ Error$$

$$= 100\% - 3{,}3\ \%$$

$$= 96{,}7\%$$

4.5.4. Kesimpulan

Dari keterangan diatas dapat disimpulkan bahwa IC ULN2003A merupakan driver motor yang dapat digunakan mengontrol *swicthing*, tergantung pada logika *input* yang diberikan dengan tingkat kesalahan sebesar 3,3% dan tingkat ketelitian 96,7%.

4.6.Pengujian *Timer*

4.6.1. Tujuan

Pengujian *timer* ini bertujuan agar pewaktuan dalam proses pembenihan dapat tepat sesuai dan tidak melewati batas waktu yang telah ditentukan. Jika kurang atau lebih waktu yang telah ditentukan akan mengakibatkan cacat atau mati pada bibit ikan tersebut.

4.6.2. Peralatan yang diperlukan

1. Sistem pewaktuan Alat yang diujikan
2. *Stop Watch*

4.6.3. Langkah Pengujian

1. Stanby kan pewaktuan pada kedua alat
2. Tekan tombol start secara bersamaan
3. Hasil Pengujian timer adalah sebagai berikut:

Tabel 4 -7

Data Hasil Pengujian *Timer* pada Pembenihan

No	Kondisi	Pengukuran	
		Stopwatch	Alat pembenihan
1	Penyinaran UV	9 menit	9 menit
2	Motor Stirrer	9 menit	9 menit
3	Shocking suhu	90 detik	92 detik

Dari data pada tabel *Timer* didapat persentase *Error* adalah sebagai berikut :

1. Penyinaran UV

$$\%\,Error = \frac{0}{60} x100\%$$

$$= 0x100\%$$

$$= 0\%$$

$$\%\,\text{Ketelitian} = 100\% - \%\,Error$$

$$= 100\% - 0\ \%$$

$$= 100\%$$

2. Motor Stirrer

$$\%\,Error = \frac{0}{60} x100\%$$

$$= 0x100\%$$

$$= 0\%$$

$$\%\,\text{Ketelitian} = 100\% - \%\,Error$$

$$= 100\% - 0\ \%$$

$$= 100\%$$

3. Shocking suhu

$$\%\,Error = \frac{92-90}{90} x100\%$$

$$= \frac{2}{90} x100\%$$

$$= 2{,}2\ \%$$

% Ketelitian = 100% - % *Error*

= 100% - 2,2 %

= 97,8%

4.6.4. Kesimpulan

Dari data diatas *timer* yang digunakan pada alat pembenihan meliputi penyinaran UV dengan prosentasi kesalahan 1,85% dan ketelitian 98,15%. Kemudian Motor *stirrer* prosentasi ketelitian 100% dan *Shocking* suhu prosentasi kesalahan 2,2% dan ketelitian 97,8%.

4.7. Pengujian Alat terhadap hasil Pembenihan Ikan

4.7.1. Tujuan

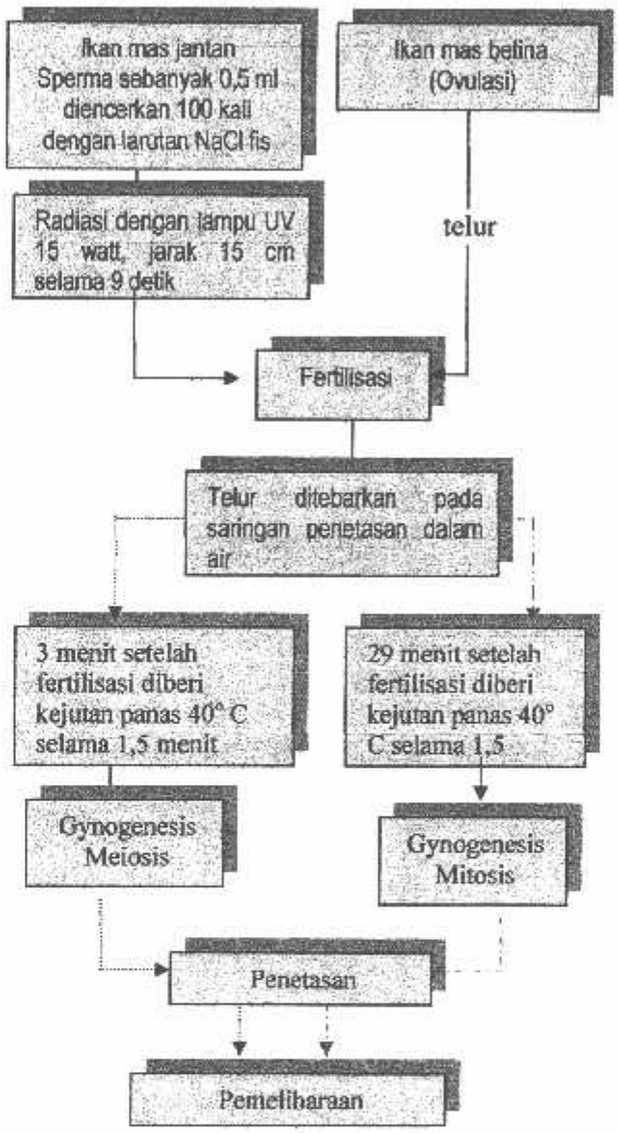
Dalam pegujian alat ini bertujuan agar dapat meningkatkan hasil pembenihan dengan cara meningkatkan hasil *larva* normal dan menekan hasil *larva* yang cacat. Dan dapat mengifisienkan cara pengerjaan dalam proses pembenihan.

4.7.2. Peralatan yang diperlukan

1. Alat pembenihan secara menyeluruh
2. Kompor
3. Cawan
4. *Sperma* dan *Ovum*
5. NaCl

4.7.3. Langkah pengujian

Dalam pengujian ini ada beberapa tahap yang perlu diujikan dan harus sesuai dengan ketentuan-ketentua dibawah ini:



Hasil pengujian alat terhadap pembenihan secara menyeluruh adalah sebagai berikut:

Tabel 4 -7

Data Hasil Pengujian Alat terhadap Pembenihan

NO	Alat Manual			Alat Otomatis		
	Jumlah Sampel	Larva Normal	Larva Cacat	Jumlah Sampel	Larva Normal	Larva Cacat
1	225	42	4	226	47	2
2	212	39	3	210	40	1

Dari pengujian alat secara manual dan secara otomatis didapat nilai pada tabel diatas dapat dicari nilai prosentasi masing larva nomal dan larva cacat sebagai berikut:

1. Alat manual

a. %Larva Normal $= \frac{42}{225} x100\%$

$= 18{,}6\%$

%Larva Cacat $= \frac{4}{225} x100\%$

$= 0{,}9\%$

b. %Larva Normal $= \frac{39}{212} x100\%$

$= 18{,}3\%$

%Larva Cacat $= \frac{3}{212} x100\%$

$= 1{,}4\%$

2. Alat Otomatis

a. %Larva Normal $= \frac{45}{223} x100\%$

$= 20{,}01\%$

%Larva Cacat $= \frac{2}{223} x100\%$

$= 0{,}8\%$

b. %Larva Normal $= \frac{40}{210} x100\%$

$= 19{,}0\%$

%Larva Cacat $= \frac{2}{210} x100\%$

$= 0{,}9\%$

Tabel 4 -7

Data Hasil Persentase keberhasilan Alat terhadap Pembenihan

NO	%Alat Manual		%Alat Otomatis	
	Larva Normal	Larva Cacat	Larva Normal	Larva Cacat
1	18,45	1,15	19,5	0.85

4.7.4.Kesimpulan

Dalam pengujian diatas bahwa alat otomatis cenderung dapat menekan jumlah larva cacat daripada alat manual sebesar 0,85% dan meningkatkan jumlah larva normal daripada alat manual sebesar 19,5%

BAB V

PENUTUP

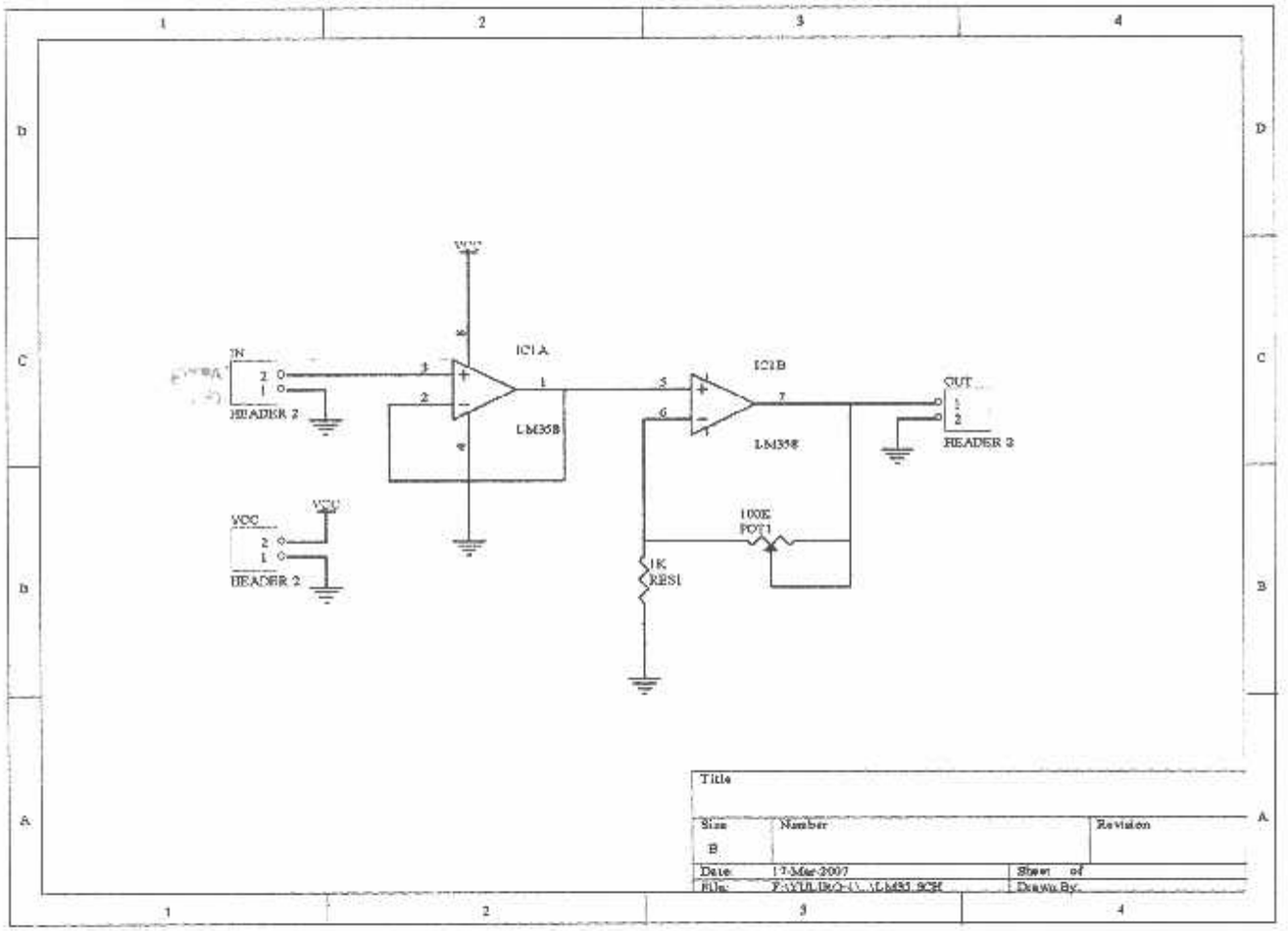
5.1. Kesimpulan

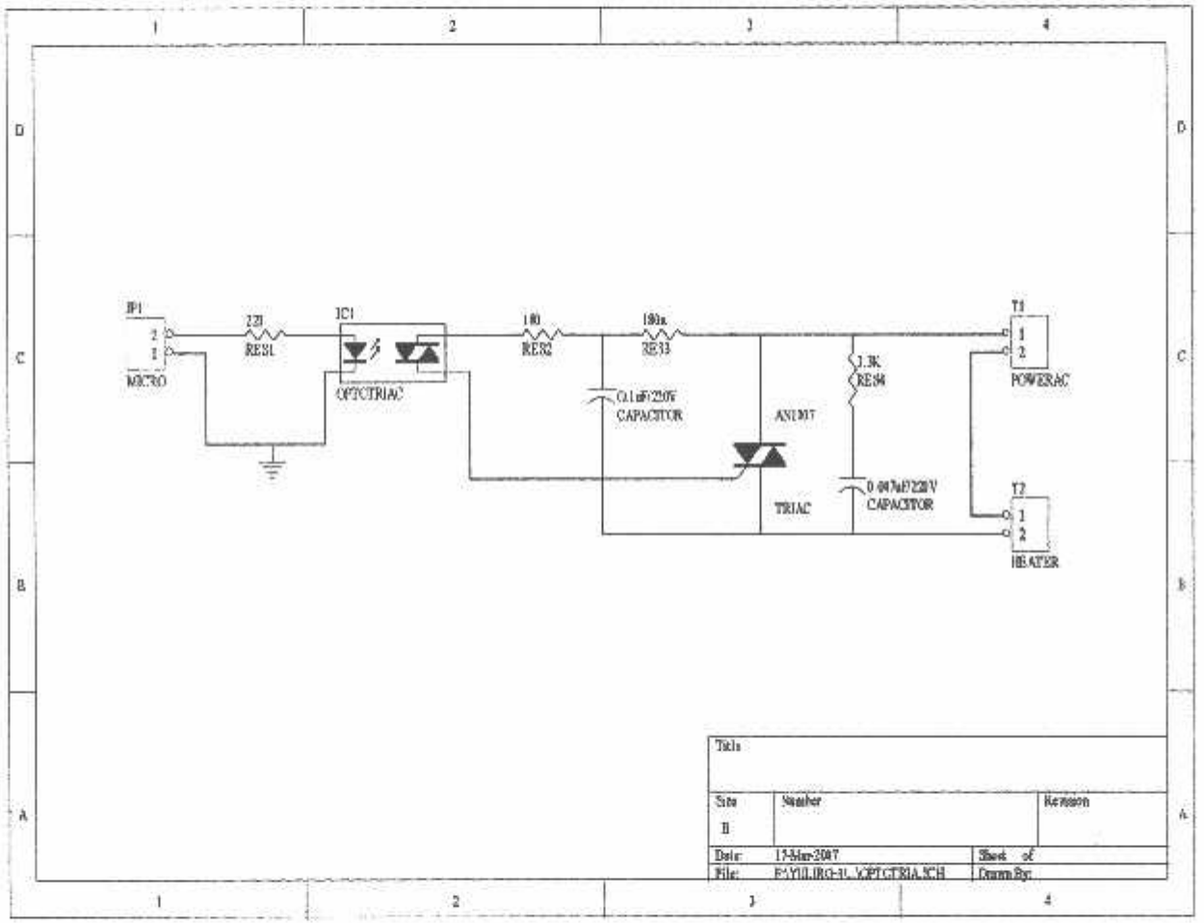
Dari hasil perancangan dan pembuatan serta pengukuran alat yang telah dilakukan, dapat disimpulkan bahwa :

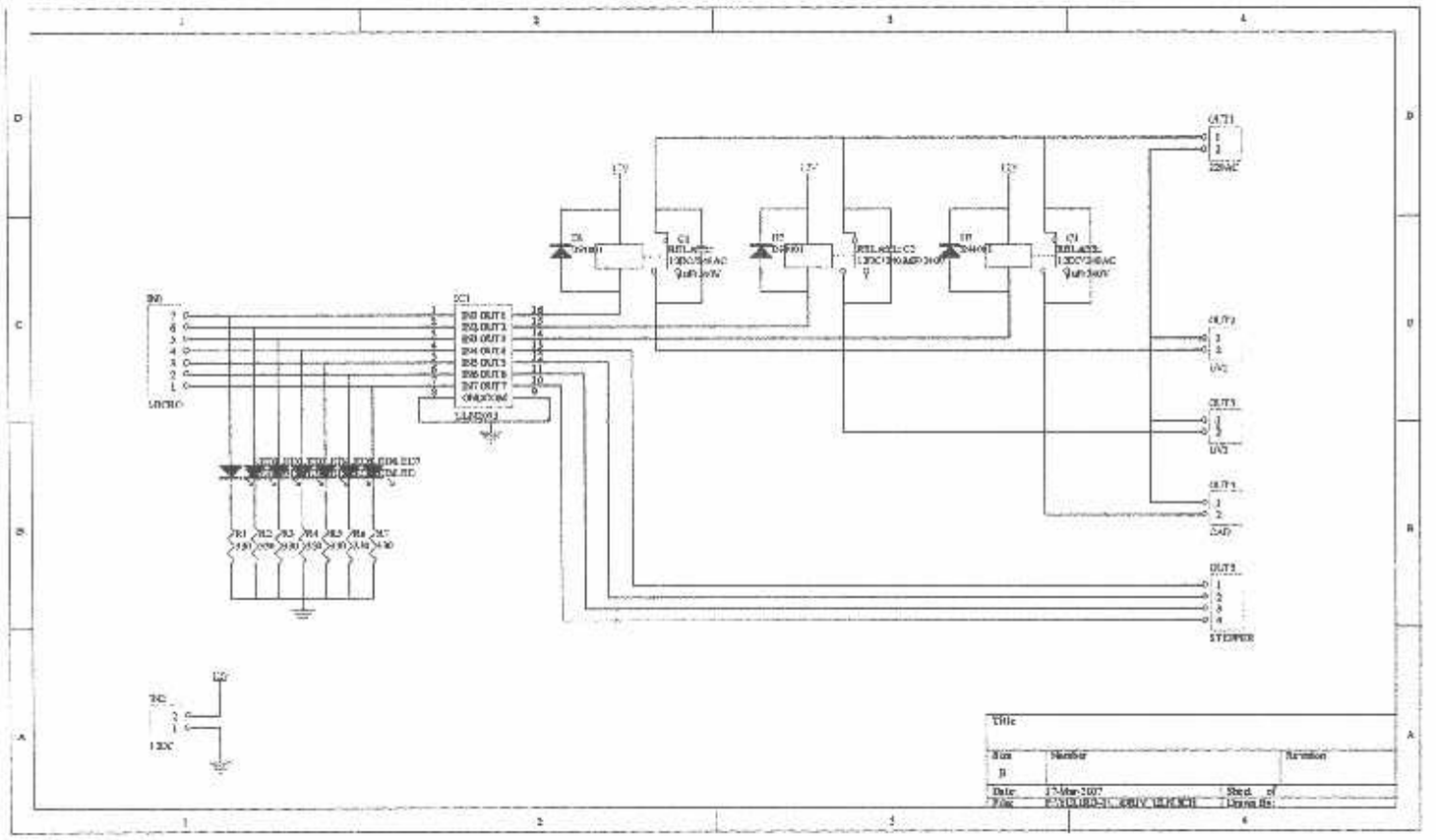
- Suhu yang ditampilkan pada LCD dan dibandingkan dengan termometer mempunyai tingkat prosentasi ketelitian sebesar 98% dan prosentasi kesalahan sebesar 2%
- Pada penguat buffer yang digunakan Untuk menyangga tegangan mempunyai prosentase tingkat kesalahan sebesar 0,5% dan prosentase tingkat ketelitian sebesar 99,5%. Sedangkan untuk penguat non inverting dengan penguatan 2X mempunyai tingkat kesalahan sebesar 1,67% dan prosentase tingkat ketelitian sebesar 98,3%.
- Penggunaan IC ULN2003A untuk driver relay yang dapat mengontrol swiching pada relay dan driver motor stirrer mempunyai tingkat kesalahan sebesar 3,3% dan tingkat ketelitian 96,7%.
- Pada pengaturan kecepatan motor sangat tepat menggunakan triac karena pada swiching dengan Prosentasi error 40% dengan ketelitian 60%.
- Timer dapat disimpulkan yang digunakan pada alat pembenihan meliputi penyinaran UV dengan prosentasi kesalahan 1,85% dan ketelitian 98,15%. Kemudian Motor stirrer prosentasi ketelitian 100% dan Shocking suhu prosentasi kesalahan 5,5% dan ketelitian 94,5%.

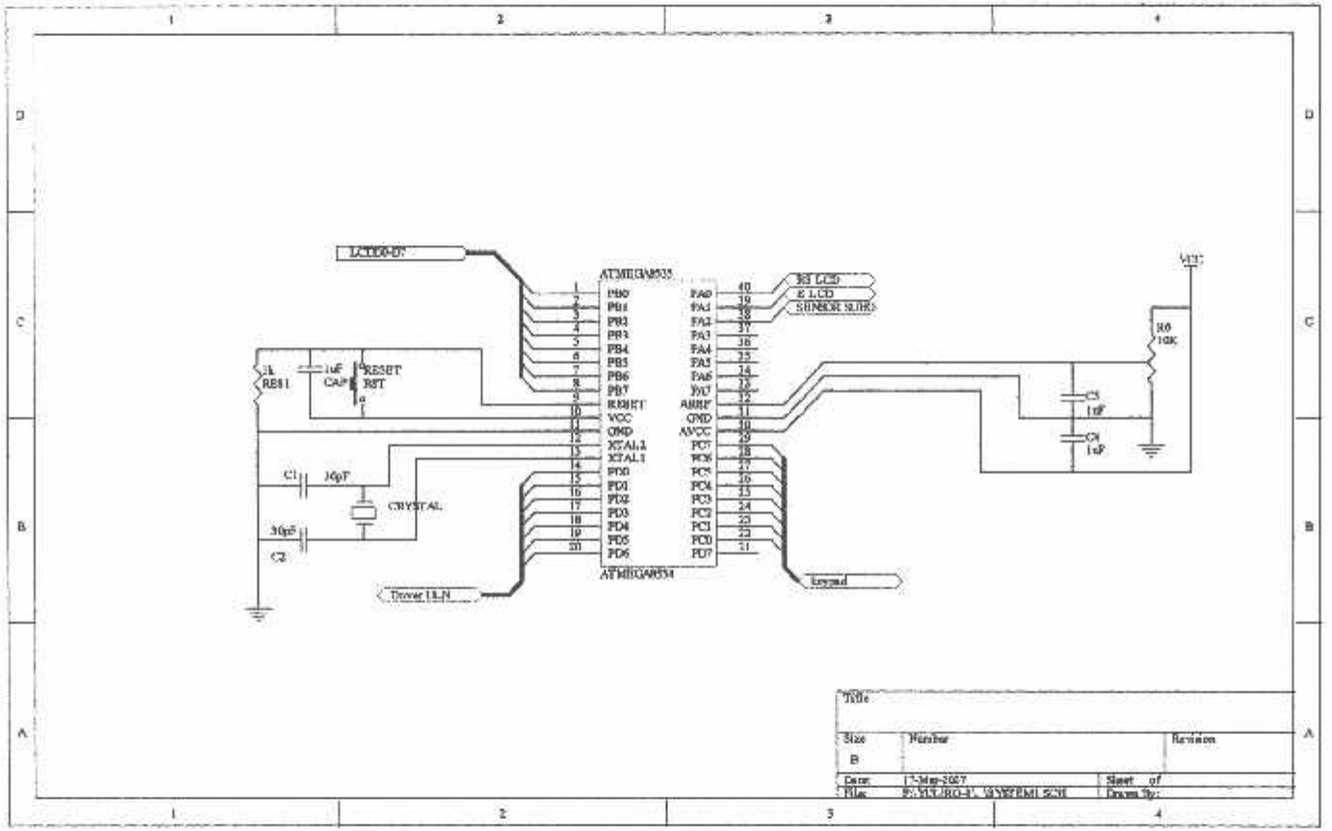
Lampiran A

Skema Rangkaian


IN
HEADER 2
IC1A
LM358
IC1B
LM358
OUT
HEADER 2
VCC
HEADER 2
100E
POT1
1K
RES1
Title
Size
B
Number
Revision
Date: 17-Mar-2007
Sheet of
File:
Drawn By:


1
2
3
4
A
B
C
D
JP1
2
1
MICRO
220
RES1
IC1
OPTOTRIAC
180
RES2
180a
RES3
0.1uF/250V
CAPACITOR
AN1007
TRIAC
1.3K
RES4
0.047uF/220V
CAPACITOR
T1
1
2
POWERAC
T2
1
2
HEATER
Title
Size
B
Number
Revision
Date: 17-Mar-2007
File: E:\YUL\RG-31_V\OPTOTRIA.SCH
Sheet of
Drawn By:




LCDD0-D7
ATMEGA8535
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
RESET
VCC
GND
XTAL2
XTAL1
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
AREF
GND
AVCC
PC7
PC6
PC5
PC4
PC3
PC2
PC1
PC0
PC7
ATMEGA8535
R81
1k
1uF
CAP
RESET
RST
C1
30pF
CRYSTAL
30pF
C2
Driver I.S.N
Keypad
R6
10K
C5
1nF
C4
1nF
Title
Size
B
Number
Revision
Date:
17-May-2007
Sheet of
File:
Drawn By:

Lampiran B

Listing Program

Syntac Program Mikrokontroler ATMEGA8535

```
//LCD8bit.c : source file for the LCD8bit project
//

#include "LCD8bit.h"
#include <delay.h>
////////////////////////////////////////////////////////////////////
//LCD8bit

#define d_in PINB;



unsigned char adcval;
unsigned char out;

static void io_init(void)
{
        //{{WIZARD_MAP(General)
        //}}WIZARD_MAP(General)

        //{{WIZARD_MAP(I/O Ports)
        // PortA

        PORTA = 0x0;
        DDRA = 0xff;
        // PortB


        PORTB = 0xff;
        DDRB = 0x0;

        // PortC
        PORTC = 0x0;
        DDRC = 0xff;
        // PortD
        PORTD = 0x0;
        DDRD = 0xff;

        //}}WIZARD_MAP(I/O Ports)

        //{{WIZARD_MAP(Watchdog)
        // Watchdog Disabled
        wdt_disable();
        //}}WIZARD_MAP(Watchdog)

        //{{WIZARD_MAP(Analog Comparator)
        // Analog Comparator Disabled
        ACSR = 0x80;
```

```
        //}}WIZARD_MAP(Analog Comparator)

        ADMUX=0x00;
        ADCSRA=0xed;

}

ISR(ADC_vect)
{
 adcval = ADCW;
}

/************************/
/*  RUTIN DELAY LCD  */
/************************/
static void lcddelay(void)
{
//  char i;
//  for (i=1;i<=250;i++){}

 delay(100,4);
}

void writetolcd(char n, char dt)
{
//  LCD_RS = n;

   if (n==0)cbi(PORTD,6);
   if (n==1)sbi(PORTD,6);

  outb(PORTC,dt);
  sbi(PORTD,7);
  lcddelay();
  cbi(PORTD,7);
  lcddelay();
}

void initlcd(void)
{
  writetolcd(0, 0x38);
  lcddelay();
  writetolcd(0, 0xC);
  lcddelay();
  writetolcd(0, 6);
  lcddelay();
  writetolcd(0, 1);
  lcddelay();
}

void clrscr(void)
```

```
{
  writetolcd(0, 0xC);
  lcddelay();
  writetolcd(0, 6);
  lcddelay();
  writetolcd(0, 1);
  lcddelay();
}

void blink(char i)
{
  if (i==0)
    writetolcd(0, 0xC);
  else
    writetolcd(0, 0xD);
  lcddelay();
}

void gotoxy(char x, char y)
{
  if (y==1)
    writetolcd(0, 0x80 + x - 1);
  else if (y==2)
    writetolcd(0, 0xC0 + x - 1);
}

void putch(char x, char y, char ch)
{
  gotoxy(x, y);
  lcddelay();
  writetolcd(1, ch);
  lcddelay();
}

void prints(char x, char y, char* s)
{
  char i = 0;

  while(s[i] != 0)
  {
    putch(x+i, y, s[i]);
    i++;
  }
}

void print_byte(char x, char y, unsigned char s){
   gotoxy(x,y);
   writetolcd(1, (s / 100) | 0x30);
   writetolcd(1, ((s % 100)/10) | 0x30);
   writetolcd(1, (s % 10) | 0x30);
```

```
}

void print_hex(char x, char y, unsigned char s){
   gotoxy(x,y);
   writetolcd(1, (s >> 4   ) | 0x30);
   writetolcd(1, (s  & 0x0f) | 0x30);
}

void print_time(char x, char y, unsigned char s,unsigned char t,unsigned char u, char
v){
   gotoxy(x,y);
   writetolcd(1, (s >> 4   ) | 0x30);
   writetolcd(1, (s  & 0x0f) | 0x30);

   writetolcd(1, v);

   writetolcd(1, (t >> 4   ) | 0x30);
   writetolcd(1, (t  & 0x0f) | 0x30);

   writetolcd(1, v);

   writetolcd(1, (u >> 4   ) | 0x30);
   writetolcd(1, (u  & 0x0f) | 0x30);
}


void print_int(char x, char y, unsigned long int s){
unsigned long int t;
unsigned char l;
   gotoxy(x,y);

   t = (s / 100);       l = t; writetolcd(1, l | 0x30);
   t = (s % 100) / 10; l = t; writetolcd(1, l | 0x30);
   t = (s % 10) /  1; l = t; writetolcd(1, l | 0x30);
}
void print_int2(char x, char y, unsigned long int s){
unsigned long int t;
unsigned char l;
   gotoxy(x,y);

   t = (s % 100) / 10; l = t; writetolcd(1, l | 0x30);
   t = (s % 10) /  1; l = t; writetolcd(1, l | 0x30);
}

void print_int5(char x, char y, unsigned long int s){
unsigned long int t;
unsigned char l;
   gotoxy(x,y);

   t = (s / 10000);       l = t; writetolcd(1, l | 0x30);
```

```
  t = (s % 10000) / 1000; l = t; writetolcd(1, l | 0x30);
  t = (s % 1000) / 100; l = t; writetolcd(1, l | 0x30);
  t = (s % 100) / 10; l = t; writetolcd(1, l | 0x30);
  t = (s % 10) / 1; l = t; writetolcd(1, l | 0x30);
}
void delayMSEC(unsigned int max)
{
  unsigned char j;
  unsigned int i;
  for(i=0;i !=max;i++)
      for(j=0;j!=131;j++);
}

void delaySEC(unsigned int max)
{
  unsigned char j;
  unsigned int i,k;
  for(i=0;i!=max;i++)
     for(j=0;j!=131;j++)
       for(k=0;k!=600;k++);
}

unsigned char ambilkey()
{
        unsigned char kbd,kpr,kpk;
                kbd=d_in;
                kpr=kbd & 0x10;
                if (kpr==0x10)
                {
                        kpk=kbd & 0x0f;
                        //delay(110,4000);
                        delayMSEC(100);
                        return kpk;

                } else
                {

                        return 0;
                }
}

unsigned char ambil2dg()
{
        unsigned char keluar,tmp,dg,ts,tm,tj;
        ts=0;
        tmp=0;
        dg=1;
        keluar=0;
                gotoxy(10,2);blink(1);
```

```
        while(keluar==0)
        {
         tmp=0;
         while (tmp==0) tmp=ambilkey();
         if (tmp==12)
         {
                keluar=1;      dg=0;
         }
         if (tmp==13)
         {
                dg=0;
                tmp=0;
                print_int2(10,2,0);
                gotoxy(10,2);

         }
         if (tmp==10) tmp=0;
         if (dg==2)
         {
                tn=tmp;
               tj=(ts*10)+tn;
                print_int2(10,2,tj);
                gotoxy(12,2);blink(1);

         }

         if (dg==1)
         {
                ts=tmp;
                print_int2(10,2,ts);
                gotoxy(11,2);
         }

         dg++;
      tmp=0;
         if (dg>=3) dg=1;

         }

         //while 1
         keluar=0;
         return tj;
}

void wait_enter()
{
        unsigned char tmp;
        tmp=0;
        while(tmp!=12) tmp=ambilkey();
}
```

```
void magnetic_pwm(unsigned int d_on, unsigned int  d_off)
{
        cbi(PORTD,4);
        delayMSEC(d_on);
        sbi(PORTD,4);
        delayMSEC(d_off);
}

void pompa_pwm(unsigned int d_on, unsigned int  d_off)
{
        cbi(PORTD,3);
        delayMSEC(d_on);
        sbi(PORTD,3);
        delayMSEC(d_off);
}

void waktu_uv_st()
{
        unsigned char waktu_uv,waktu_mn,tmp;
        unsigned int w_on,w_off,dtk,mdtk;

        w_on=5;
        w_off=70;
        tmp=0;
        dtk=0;
        mdtk=0;


          prints(1,1,"Magnetic Stirer  ");
              prints(1,2,"Waktu On:  Detik ");

              waktu_mn=ambil2dg();

          prints(1,1,"Ultra Violet     ");
              prints(1,2,"Waktu On:  Menit ");

              waktu_uv=ambil2dg();

              prints(1,1,"UV     :  Menit  ");
              prints(1,2,"Magnet :  Detik  ");

              print_int2(9,1,waktu_uv);
              print_int2(9,2,waktu_mn);
              wait_enter();
              clrscr();
              prints(1,1,"Magnetic Run  ");
              prints(1,2,"Remaining:   S");
```

```
blink(0);


while(dtk<=waktu_mn)
{

while(tmp==0)
 {
  tmp=ambilkey();
  magnetic_pwm(w_on,w_off);
  mdtk++;

  if (mdtk>=8)
  {
        dtk++;
        mdtk=0;
        if (dtk>=60) dtk=60;
  }
  print_int2(12,2,dtk);

 if (dtk>=waktu_mn) tmp=12;
 } //while tmp

if (tmp==1)w_on=w_on+5;
if (tmp==2)w_on=w_on-5;
if (tmp==15)w_on=w_on+5;
if (tmp==16)w_on=w_on-5;
if (tmp==3)w_off=w_off+5;
if (tmp==4)w_off=w_off-5;
if (tmp==12)
{
        tmp=12;
        dtk=200;
}else tmp=0;

if (w_on<=5) w_on=5;
if (w_off<=5) w_off=5;

}//while waktu_mn


prints(1,1,"Ultra Violet ON  ");
prints(1,2,"Waktu=  :      ");

cbi(PORTD,4); //stirer
sbi(PORTD,0);         //UV on

dtk=0;
mdtk=0;
while(mdtk<waktu_uv)
```

```
		{
			delayMSEC(500);
			dtk++;

			if (dtk>=60)
			{
				dtk=0;
				mdtk++;
			}
			print_int2(7,2,mdtk);
			print_int2(10,2,dtk);

		}

		cbi(PORTD,0);
		cbi(PORTD,0);
		cbi(PORTD,4);
		cbi(PORTD,4);

}


void shocking_suhu()
{
		unsigned char suhu,keadaan,siklus;
		unsigned menit,detik;
			unsigned char waktu_uv,waktu_mn,tmp;
	unsigned int w_on,w_off,dtk,mdtk;
	unsigned long mdet;
	mdet=0;
	siklus=0;
		clrscr();

	prints(1,1,"SHOCKING SUHU  ");
		prints(1,2,"SUHU:  C");
			suhu=0;
		sbi(PORTD,1);
		sbi(PORTD,2);
		while(suhu<40)
		{

		 suhu=(adcval*0.0196)/0.05;
		 print_int2(6,2,suhu);
		 delayMSEC(300);

		   sbi(PORTD,1);
			sbi(PORTD,2);
			//delaySEC(15);
		}
```

```
prints(1,1,"SHOCKING SUHU  ");
    prints(1,2,"SUHU:  C");
    suhu=0;
    keadaan=0;

    while(keadaan==0)
    {


          //tambahan

     suhu=(adcval*0.0196)/0.05;
     print_int2(6,2,suhu);
     delayMSEC(300);
          if (suhu>42)
          {

       cbi(PORTD,2);
           cbi(PORTD,1);
           delayMSEC(100);
          }

          if (suhu<40)
          {
                sbi(PORTD,2);
                cbi(PORTD,1);
                delayMSEC(100);
          }

          if ((suhu<42) && (suhu>39)) keadaan=1;


    }//while suhu


    cbi(PORTD,1);
    cbi(PORTD,2);
    cbi(PORTD,3);

    clrscr();
    prints(1,1,"SHOCKING SUHU  C");
    prints(1,2,"SIAP DIGUNAKAN ");
    print_int2(14,1,suhu);
    wait_enter();

    clrscr();
    prints(1,1,"SHOCKING MULAI  ");
    prints(1,2,"Waktu=  Detik   ");
    detik=0;
```

```
        menit=0;

        sbi(PORTD,2);

                w_on=5;
    w_off=70;
    siklus=0;
        while (detik<90)
        {

        tmp=ambilkey();
        pompa_pwm(w_on,w_off);

        if (tmp==1)w_on=w_on+5;
        if (tmp==2)w_on=w_on-5;

        if (tmp==15)w_on=w_on+5;
        if (tmp==16)w_on=w_on-5;
        if (tmp==3) siklus=1;
        if (tmp==4) {siklus=0;mdet=0;}

        if (w_on<=5) w_on=5;
        if (w_off<=5) w_off=5;

            //delayMSEC(550);
        //hitung siklus program sampai 1 detik.
        mdet++;
        if (mdet==6) { detik++; mdet=0;}

            print_int2(7,2,detik);
            //print_int5(1,2,mdet);
        }

        cbi(PORTD,3);
        clrscr();
        prints(1,1,"Proses SHOCKING  ");
        prints(1,2,"Sudah 90 Detik   ");

        cbi(PORTD,0);
        cbi(PORTD,1);
        cbi(PORTD,2);
        cbi(PORTD,3);
        cbi(PORTD,4);
        PORTD=0; //pastikan seluruh pemanas mati,
        wait_enter();


}

void pilihan()
```

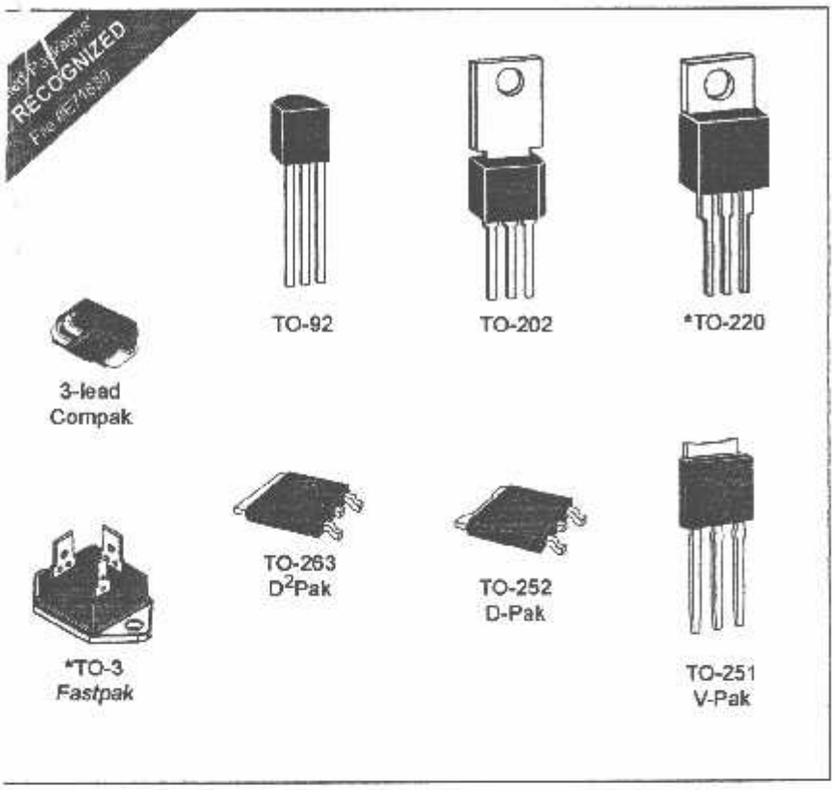
```
{
        unsigned char kbdhit;
        clrscr();
        prints(1,1,"1.Sterilisasi UV");
        prints(1,2,"2.Shocking     ");
        kbdhit=0;

        while (kbdhit==0)
        {
        kbdhit=0;
        while(kbdhit==0) kbdhit=ambilkey();

        if (kbdhit==1)
        {
                waktu_uv_st();
                clrscr();
                prints(1,1,"1.Sterilisasi UV");
                prints(1,2,"2.Shocking     ");
                kbdhit=0;
        }

        if (kbdhit==2)
        {
                //waktu_uv_st();
                shocking_suhu();
                clrscr();
                prints(1,1,"1.Sterilisasi UV");
                prints(1,2,"2.Shocking     ");
                kbdhit=0;
        }

        if (kbdhit==3)
        {
                kbdhit=3; //pastikan tetap 11 untuk keluar
        } else kbdhit=0; //biar keluar

        }


}


void main(void)
{
        unsigned char kbd,kpr,kpk;

        io_init();
        initlcd();
        clrscr();
        kbd=0;
```

```
        kpr=0;
        sei();
                prints(1,1,"SYSTEM STANDBY ");
                prints(1,2,"TA-IWAK 2007  ");
                wait_enter();

        while(1)
        {
                clrscr();
                pilihan();
        }
}
```

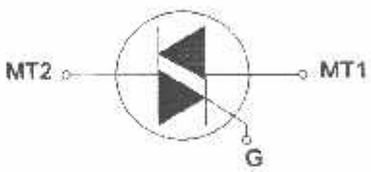
```
#include <reg51.h<
#include <stdio.h<
#include <delayW.h<
#include <keypad44i.h<
#//include <delayW.h<

sbit b1=P3^2;
sbit b2=P3^3;
sbit b3=P3^4;
sbit b4=P3^5;
sbit dibaca=P3^7;

void main()
}
 unsigned char kbhit;
 P3=0x00;

 while (1(
}
  kbhit=0;
//  dibaca=0;
  while (kbhit==0) kbhit=ambilkey;()
   switch(kbhit(
}
    case 1: {b1=1;b2=0;b3=0;b4=0; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 2: {b1=0;b2=1;b3=0;b4=0; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 3: {b1=1;b2=1;b3=0;b4=0; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 4: {b1=0;b2=0;b3=1;b4=0; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 5: {b1=1;b2=0;b3=1;b4=0; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 6: {b1=0;b2=1;b3=1;b4=0; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 7: {b1=1;b2=1;b3=1;b4=0; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 8: {b1=0;b2=0;b3=0;b4=1; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 9: {b1=1;b2=0;b3=0;b4=1; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 10:{b1=0;b2=1;b3=0;b4=1; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 11:{b1=1;b2=1;b3=0;b4=1; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 12:{b1=0;b2=0;b3=1;b4=1; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 13:{b1=1;b2=0;b3=1;b4=1; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 14:{b1=0;b2=1;b3=1;b4=1; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 15:{b1=1;b2=1;b3=1;b4=1; dibaca=1;delayMSEC(110);dibaca=0;}break;
    case 16:{b1=0;b2=0;b3=0;b4=0; dibaca=1;delayMSEC(110);dibaca=0;}break;
{

//   while (dibaca==0;(
   kbhit=0;

{

{
```

Lampiran C

Data Sheet



E2



Triacs

(0.8 A to 35 A)

ıeral Description

ıe gated triacs from Teccor Electronics are part of a broad of bidirectional semiconductors. The devices range in current gs from 0.8 A to 35 A and in voltages from 200 V to 1000 V.

triac may be gate triggered from a blocking to conduction for either polarity of applied voltage and is designed for AC thing and phase control applications such as speed and tem- ture modulation controls, lighting controls, and static switch- elays. The triggering signal is normally applied between the and MT1.

ted packages are offered with internal construction, having ıse or mounting tab electrically isolated from the semicon- or chip. This feature facilitates the use of low-cost assembly convenient packaging techniques. Tape-and-reel capability ailable. See "Packing Options" section of this catalog.

ccor triacs have glass-passivated junctions to ensure long- device reliability and parameter stability. Teccor's glass-pas- ed junctions offer a rugged, reliable barrier against junction amination.

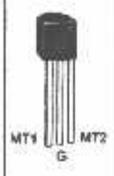
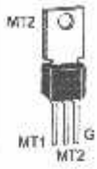
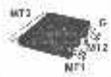
Variations of devices covered in this data sheet are available for custom design applications. Consult factory for more information.

Features

- **Electrically-isolated packages**
- **Glass-passivated junctions**
- **Voltage capability — up to 1000 V**
- **Surge capability — up to 200 A**

Compak Package

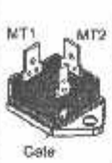
- **Surface mount package — 0.8 A and 1 A series**
- **New small profile three-leaded Compak package**
- **Packaged in embossed carrier tape with 2,500 devices per reel**
- **Can replace SOT-223**

Part Number									V_{DRM}	I_{GT}				
	Isolated			Non-isolated					(1)	(3) (7) (15)				
									Volts	mAmps				
	TO-92	TO-220	Compak	TO-202	TO-220	TO-252 D-Pak	TO-251 V-Pak	TO-263 D^2Pak		QI	QII	QIII	QIV	QIV
	See "Package Dimensions" section for variations. (11)								MIN	MAX				TYP
	Q2X8E3		Q2X3						200	10	10	10		25
	Q4X8E3		Q4X3						400	10	10	10		25
	Q6X8E3		Q6X3						600	10	10	10		25
	Q2X8E4		Q2X4						200	25	25	25		50
	Q4X8E4		Q4X4						400	25	25	25		50
	Q6X8E4		Q6X4						600	25	25	25		50
	Q201E3		Q2N3						200	10	10	10		25
	Q401E3		Q4N3						400	10	10	10		25
	Q601E3		Q6N3						600	10	10	10		25
	Q201E4		Q2N4						200	25	25	25		50
	Q401E4		Q4N4						400	25	25	25		50
	Q601E4		Q6N4						600	25	25	25		50
		Q2004L3		Q2004F31		Q2004D3	Q2004V3		200	10	10	10		25
		Q4004L3		Q4004F31		Q4004D3	Q4004V3		400	10	10	10		25
		Q6004L3		Q6004F31		Q6004D3	Q6004V3		600	10	10	10		25
		Q2004L4		Q2004F41		Q2004D4	Q2004V4		200	25	25	25		50
		Q4004L4		Q4004F41		Q4004D4	Q4004V4		400	25	25	25		50
		Q6004L4		Q6004F41		Q6004D4	Q6004V4		600	25	25	25		50
		Q8004L4				Q8004D4	Q8004V4		800	25	25	25		50
		QK004L4				QK004D4	QK004V4		1000	25	25	25		50
		Q2006L4		Q2006F41	Q2006R4			Q2006N4	200	25	25	25		50
		Q4006L4		Q4006F41	Q4006R4			Q4006N4	400	25	25	25		50
		Q6006L5		Q6006F51	Q6006R5			Q6006N5	600	50	50	50		75
		Q8006L5			Q8006R5			Q8006N5	800	50	50	50		75
		QK006L5			QK006R5			QK006N5	1000	50	50	50		75
		Q2008L4		Q2008F41	Q2008R4			Q2008N4	200	25	25	25		50
		Q4008L4		Q4008F41	Q4008R4			Q4008N4	400	25	25	25		50
		Q6008L5		Q6008F51	Q6008R5			Q6008N5	600	50	50	50		75
		Q8008L5			Q8008R5			Q8008N5	800	50	50	50		75
		QK008L5			QK008R5			QK008N5	1000	50	50	50		75

General Notes" on page E2 - 4 and "Electrical Specification Notes" on page E2 - 5

I_{DRM}			V_{TM}	V_{GT}	I_H	I_{GTM}	P_{GM}	$P_{G(AV)}$	I_{TSM}	dv/dt(c)	dv/dt		t_{gt}	I^2t	di/dt
(1) (16)			(1) (5)	(2) (6) (15) (18) (19)	(1) (8) (12)	(14)	(14)		(9) (13)	(1) (4) (13)	(1)		(10)		
mAmps			Volts	Volts					Amps		Volts/µSec				
°C = °C	T_C = 100 °C	T_C = 125 °C	T_C = 25 °C	T_C = 25 °C	mAmps	Amps	Watts	Watts	60/50 Hz	Volts/µSec	T_C= 100 °C	T_C= 125 °C	µSec	Amp^2Sec	Amps/µSec
MAX			MAX	MAX	MAX					TYP	MIN		TYP		
.02	0.5	1	1.6	2	15	1	10	0.2	10/8.3	1	40	30	2.5	0.41	20
.02	0.5	1	1.6	2	15	1	10	0.2	10/8.3	1	35	25	2.5	0.41	20
.02	0.5	1	1.6	2	15	1	10	0.2	10/8.3	1	25	15	2.5	0.41	20
.02	0.5	1	1.6	2.5	25	1	10	0.2	10/8.3	1	50	40	3	0.41	20
.02	0.5	1	1.6	2.5	25	1	10	0.2	10/8.3	1	45	35	3	0.41	20
.02	0.5	1	1.6	2.5	25	1	10	0.2	10/8.3	1	35	25	3	0.41	20
.02	0.5	1	1.6	2	15	1	10	0.2	20/16.7	1	40	30	2.5	1.6	30
.02	0.5	1	1.6	2	15	1	10	0.2	20/16.7	1	40	30	2.5	1.6	30
.02	0.5	1	1.6	2	15	1	10	0.2	20/16.7	1	30	20	2.5	1.6	30
.02	0.5	1	1.6	2.5	25	1	10	0.2	20/16.7	1	50	40	3	1.6	30
.02	0.5	1	1.6	2.5	25	1	10	0.2	20/16.7	1	50	40	3	1.6	30
.02	0.5	1	1.6	2.5	25	1	10	0.2	20/16.7	1	40	30	3	1.6	30
.05	0.5	2	1.6	2	20	1.2	15	0.3	55/46	2	50	40	2.5	12.5	50
.05	0.5	2	1.6	2	20	1.2	15	0.3	55/46	2	50	40	2.5	12.5	50
.05	0.5	2	1.6	2	20	1.2	15	0.3	55/46	2	40	30	2.5	12.5	50
.05	0.5	2	1.6	2.5	30	1.2	15	0.3	55/46	2	100	75	3	12.5	50
.05	0.5	2	1.6	2.5	30	1.2	15	0.3	55/46	2	100	75	3	12.5	50
.05	0.5	2	1.6	2.5	30	1.2	15	0.3	55/46	2	75	50	3	12.5	50
.05	0.5	2	1.6	2.5	30	1.2	15	0.3	55/46	2	60	40	3	12.5	50
.05	3		1.6	2.5	30	1.2	15	0.3	55/46	2	50		3	12.5	50
.05	0.5	2	1.6	2.5	50	1.6	18	0.5	80/65	4	200	120	3	26.5	70
.05	0.5	2	1.6	2.5	50	1.6	18	0.5	80/65	4	200	120	3	26.5	70
.05	0.5	2	1.6	2.5	50	1.6	18	0.5	80/65	4	150	100	3	26.5	70
.05	0.5	2	1.6	2.5	50	1.6	18	0.5	80/65	4	125	85	3	26.5	70
.05	3		1.6	2.5	50	1.6	18	0.5	80/65	4	100		3	26.5	70
.05	0.5	2	1.6	2.5	50	1.6	20	0.5	100/83	4	250	150	3	41	70
.05	0.5	2	1.6	2.5	50	1.6	20	0.5	100/83	4	250	150	3	41	70
.05	0.5	2	1.6	2.5	50	1.6	20	0.5	100/83	4	220	125	3	41	70
.05	0.5	2	1.6	2.5	50	1.6	20	0.5	100/83	4	150	100	3	41	70
.05	3		1.6	2.5	50	1.6	20	0.5	100/83	4	100		3	41	70

"General Notes" on page E2 - 4 and "Electrical Specification Notes" on page E2 - 5.

MS)	Part Number					V_{DRM}	I_{GT}					I_{DRM}		
	Isolated		Non-isolated											
:16)						(1)	(3) (7) (15)					(1) (16)		
							mAmps					mAmps		
	TO-3 Fastpak	TO-220	TO-202	TO-220	TO-263 D^2Pak	Volts	QI	QII	QIII	QIV	QIV	T_C = 25 °C	T_C = 100 °C	T_C = 125 °C
\X		See "Package Dimensions" section for variations. (11)				MIN	MAX				TYP	MAX		
		Q2010L4		Q2010R4	Q2010N4	200	25	25	25	50		0.05	1	
		Q4010L4		Q4010R4	Q4010N4	400	25	25	25	50		0.05	1	
		Q6010L4		Q6010R4	Q6010N4	600	25	25	25	50		0.05	1	
		Q8010L4		Q8010R4	Q8010N4	800	25	25	25	50		0.1	1	
A		QK010L4		QK010R4	QK010N4	1000	25	25	25	50		0.1	3	
		Q2010L5	Q2010F51	Q2010R5	Q2010N5	200	50	50	50		75	0.05	0.5	2
		Q4010L5	Q4010F51	Q4010R5	Q4010N5	400	50	50	50		75	0.05	0.5	2
		Q6010L5	Q6010F51	Q6010R5	Q6010N5	600	50	50	50		75	0.05	0.5	2
		Q8010L5		Q8010R5	Q8010N5	800	50	50	50		75	0.1	0.5	2
		QK010L5		QK010R5	QK010N5	1000	50	50	50		75	0.1	3	
		Q2015L5		Q2015R5	Q2015N5	200	50	50	50			0.05	0.5	2
i A		Q4015L5		Q4015R5	Q4015N5	400	50	50	50			0.05	0.5	2
		Q6015L5		Q6015R5	Q6015N5	600	50	50	50			0.05	0.5	2
		Q8015L5		Q8015R5	Q8015N5	800	50	50	50			0.1	1	3
		QK015L5		QK015R5	QK015N5	1000	50	50	50			0.1	3	
				Q2025R5	Q2025N5	200	50	50	50			0.1	1	3
				Q4025R5	Q4025N5	400	50	50	50			0.1	1	3
				Q6025R5	Q6025N5	600	50	50	50			0.1	1	3
5 A				Q8025R5	Q8025N5	800	50	50	50			0.1	1	3
				QK025R5	QK025N5	1000	50	50	50			0.1	3	
	Q6025P5					600	50	50	50		120	0.1		5
	Q8025P5					800	50	50	50		120	0.1		5
5 A	Q6035P5					600	50	50	50		120	0.1		5
	Q8035P5					800	50	50	50		120	0.1		5

ecific Test Conditions

t — Maximum rate-of-change of on-state current; I_{GT} = 200 mA with ≤0.1 µs rise time

lt — Critical rate-of-rise of off-state voltage at rated V_{DRM} gate open

lt(c) — Critical rate-of-rise of commutation voltage at rated V_{DRM} and $I_{T(RMS)}$ commutating di/dt = 0.54 rated $I_{T(RMS)}$/ms; gate unenergized

- RMS surge (non-repetitive) on-state current for period of 8.3 ms for fusing

I — Peak off-state current, gate open; V_{DRM} = maximum rated value

— DC gate trigger current in specific operating quadrants; V_D = 12 V dc

— Peak gate trigger current

- Holding current (DC); gate open

(S) — RMS on-state current conduction angle of 360°

— Peak one-cycle surge

(V) — Average gate power dissipation

— Peak gate power dissipation; $I_{GT} \le I_{GTM}$

– Gate controlled turn-on time; I_{GT} = 200 mA with 0.1 µs rise time

V_{DRM} — Repetitive peak blocking voltage

V_{GT} — DC gate trigger voltage; V_D = 12 V dc; R_L = 60 Ω

V_{TM} — Peak on-state voltage at maximum rated RMS current

General Notes

- All measurements are made at 60 Hz with a resistive load at an ambient temperature of +25 °C unless specified otherwise.
- Operating temperature range (T_J) is -65 °C to +125 °C for TO-92, -25 °C to +125 °C for Fastpak, and -40 °C to +125 °C for all other devices.
- Storage temperature range (T_S) is -65 °C to +150 °C for TO-92, -40 °C to +150 °C for TO-202, and -40 °C to +125 °C for all other devices.
- Lead solder temperature is a maximum of 230 °C for 10 seconds, maximum; ≥1/16" (1.59 mm) from case.
- The case temperature (T_C) is measured as shown on the dimensional outline drawings. See "Package Dimensions" section of this catalog.

V_{TM}	V_{GT}	I_H	I_{GTM}	P_{GM}	$P_{G(AV)}$	I_{TSM}	dv/dt(c)	dv/dt		t_{gt}	I^2t	di/dt
1) (5)	(2) (6) (15) (18) (19)	(1) (8) (12)	(14)	(14)		(9) (13)	(1) (4) (13)	(1)		(10) (17)		
Volts	Volts					Amps		Volts/µSec				
= 25 °C	T_C = 25 °C	mAmps	Ampa	Watts	Watts	60/50 Hz	Volts/µSec	T_C = 100 °C	T_C = 125 °C	µSec	$Amps^2Sec$	Amps/µSec
MAX	MAX	MAX					TYP	MIN		TYP		
1.6	2.5	35	1.8	20	0.5	120/100	2	150		3	60	70
1.6	2.5	35	1.8	20	0.5	120/100	2	150		3	60	70
1.6	2.5	35	1.8	20	0.5	120/100	2	100		3	60	70
1.6	2.5	35	1.8	20	0.5	120/100	2	75		3	60	70
1.6	2.5	35	1.8	20	0.5	120/100	2	50		3	60	70
1.6	2.5	50	1.8	20	0.5	120/100	4	350	225	3	60	70
1.6	2.5	50	1.8	20	0.5	120/100	4	350	225	3	60	70
1.6	2.5	50	1.8	20	0.5	120/100	4	300	200	3	60	70
1.6	2.5	50	1.8	20	0.5	120/100	4	250	175	3	60	70
1.6	2.5	50	1.8	20	0.5	120/100	4	150		3	60	70
1.6	2.5	70	2	20	0.5	200/167	4	400	275	4	166	100
1.6	2.5	70	2	20	0.5	200/167	4	400	275	4	166	100
1.6	2.5	70	2	20	0.5	200/167	4	350	225	4	166	100
1.6	2.5	70	2	20	0.5	200/167	4	300	200	4	166	100
1.6	2.5	70	2	20	0.5	200/167	4	200		4	166	100
1.8	2.5	100	2	20	0.5	200/167	5	400	275	4	166	100
1.8	2.5	100	2	20	0.5	200/167	5	400	275	4	166	100
1.8	2.5	100	2	20	0.5	200/167	5	350	225	4	166	100
1.8	2.5	100	2	20	0.5	200/167	5	300	200	4	166	100
1.8	2.5	100	2	20	0.5	200/167	5	200		4	166	100
1.4	2.75	50	2	20	0.5	250/220	5	550	475	3	260	100
1.4	2.75	50	2	20	0.5	250/220	5	450	400	3	260	100
1.5	2.75	50	2	20	0.5	350/300	5	550	475	3	508	100
1.5	2.75	50	2	20	0.5	350/300	5	450	400	3	508	100

ctrical Specification Notes

For either polarity of MT2 with reference to MT1 terminal

For either polarity of gate voltage (V_{GT}) with reference to MT1 terminal

See Gate Characteristics and Definition of Quadrants.

See Figure E2.1 through Figure E2.7 for current rating at specific operating temperature.

See Figure E2.8 through Figure E2.10 for i_T versus v_T.

See Figure E2.12 for V_{GT} versus T_C.

See Figure E2.11 for I_{GT} versus T_C.

See Figure E2.14 for I_H versus T_C.

See Figure E2.13 for surge rating with specific durations.

See Figure E2.15 for t_{gt} versus I_{GT}.

See package outlines for lead form configurations. When ordering special lead forming, add type number as suffix to part number.

Initial on-state current = 200 mA dc for 0.8 A to10 A devices, 400 mA dc for 15 A to 35 A devices

See Figure E2.1 through Figure E2.6 for maximum allowable case temperature at maximum rated current.

Pulse width ≤10 µs; $I_{GT} \leq I_{GTM}$

(15) R_L = 60 Ω for 0.8 A to10 A triacs; R_L = 30 Ω for 15 A to 35 A triacs

(16) $T_C = T_J$ for test conditions in off state

(17) I_{GT} = 300 mA for 25 A and 35 A devices

(18) Quadrants I, II, III only

(19) Minimum non-trigger V_{GT} at 125 °C is 0.2 V for all except 50 mA MAX QIV devices which are 0.2 V at 110 °C.

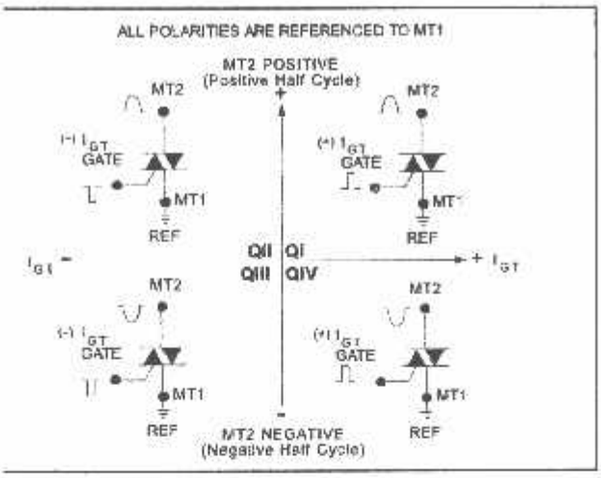
Gate Characteristics

Teccor triacs may be turned on between gate and MT1 terminals in the following ways:

- In-phase signals (with standard AC line) using Quadrants I and III
- Application of unipolar pulses (gate always positive or negative), using Quadrants II and III with negative gate pulses and Quadrants I and IV with positive gate pulses

  However, due to higher gate requirements for Quadrant IV, it is recommended that only negative pulses be applied. If positive pulses are required, see "Sensitive Triacs" section of this catalog or contact the factory. Also, see Figure AN1002.8, "Amplified Gate" Thyristor Circuit.

cases, if maximum surge capability is required, pulses
d be a minimum of one magnitude above I_{GT} rating with a
rising waveform (≤1 µs rise time).



tion of Quadrants

Electrical Isolation

Teccor's isolated triac packages will withstand a minimum high potential test of 2500 V ac rms from leads to mounting tab or base, over the operating temperature range of the device. The following isolation table shows standard and optional isolation ratings.

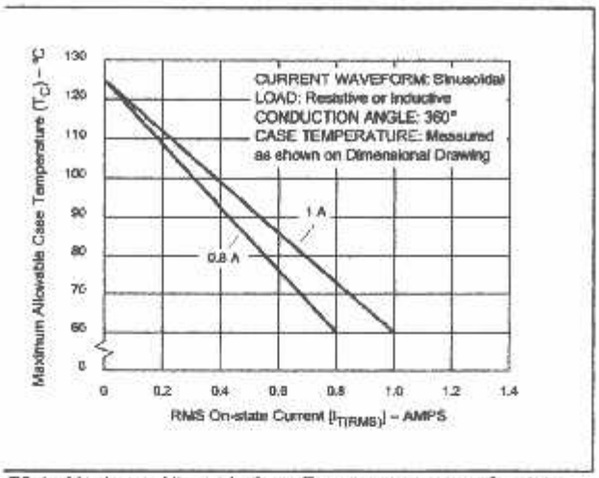
Electrical Isolation from Leads to Mounting Tab *		
V AC RMS	TO-220 Isolated	Fastpak Isolated
2500	Standard	Standard
4000	Optional **	N/A

* UL Recognized File E71639
** For 4000 V isolation, use V suffix in part number.

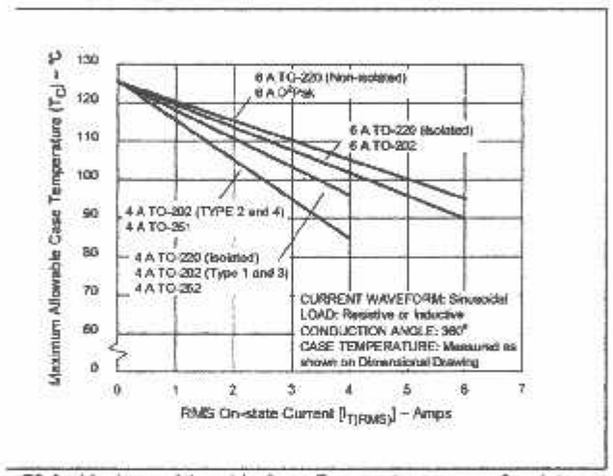
Thermal Resistance (Steady State)
$R_{\theta JC}$ [$R_{\theta JA}$] (TYP.) °C/W

age Code	P	E	C	F	F2	L	R	D	V	N
Type	 TO-3 Fastpak	 TO-92	 Compak	 TO-202 Type 1	 TO-202 Type 2	 TO-220 Isolated	 TO-220 Non-isolated	 TO-252 D-Pak	 TO-251 V-Pak	 TO-263 D^2Pak
0.8 A		60 [135]	60 *							
1 A		50 [95]	40 *							
4 A				3.5 [45]	6 [70]	3.6 [50]		3.5	5.0 [70]	
6 A				3.8		3.3	1.8 [45]			1.8
8 A				3.3		2.8	1.5			1.5
10 A				3.5		2.6	1.3			1.3
15 A						2.1	1.1			1.1
25 A	1.6						0.89			0.89
35 A	1.5									

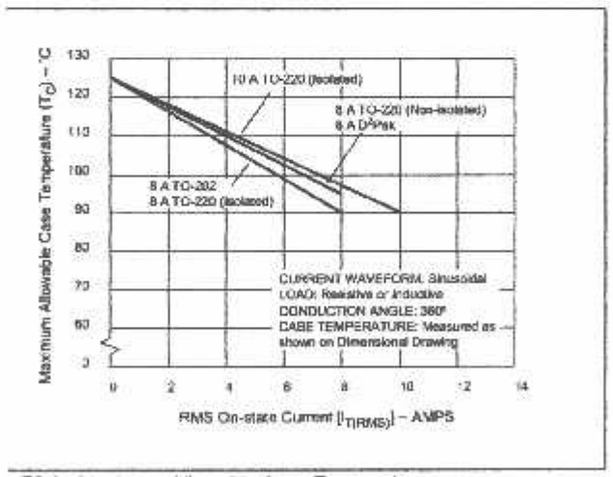
unted on 1 cm^2 copper foil surface; two-ounce copper foil



E2.1 Maximum Allowable Case Temperature versus On-state Current (0.8 A and 1 A)



a E2.2 Maximum Allowable Case Temperature versus On-state Current (4 A and 6 A)



a E2.3 Maximum Allowable Case Temperature versus On-state Current (8 A and 10 A)

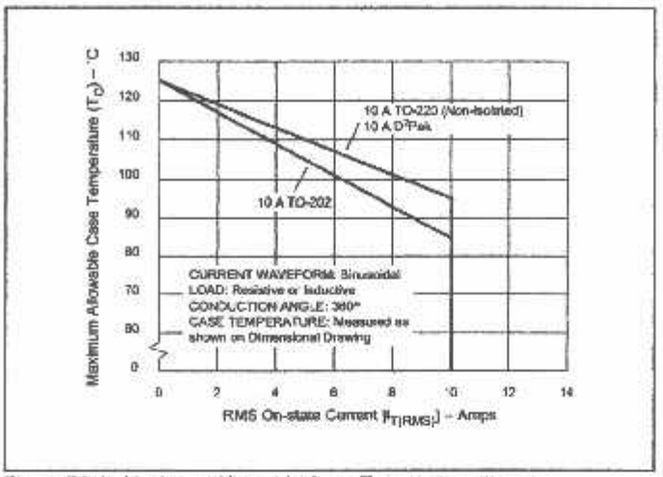


Figure E2.4 Maximum Allowable Case Temperature versus On-state Current (10 A)

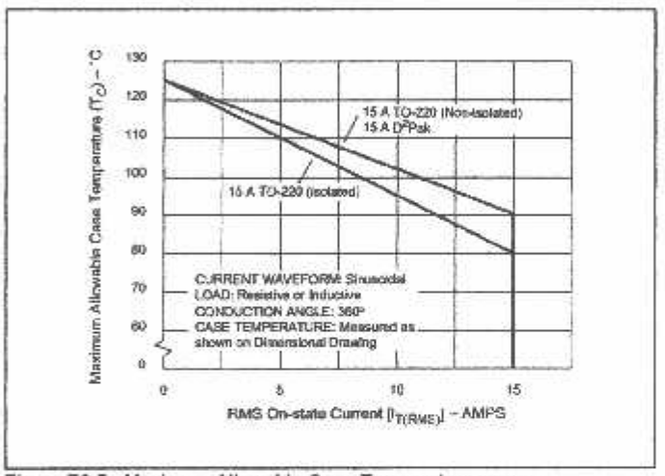


Figure E2.5 Maximum Allowable Case Temperature versus On-state Current (15 A)

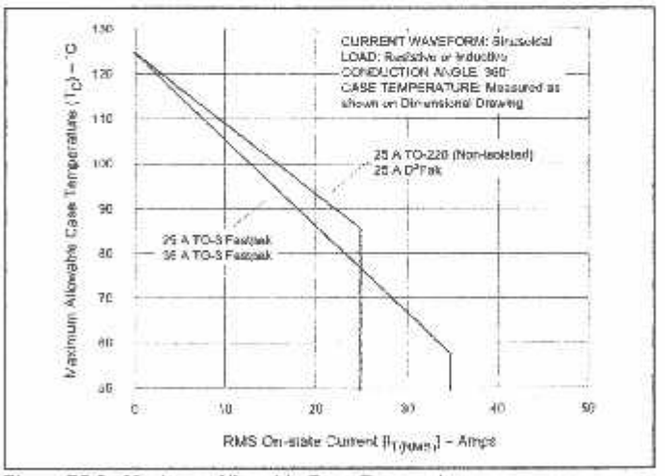
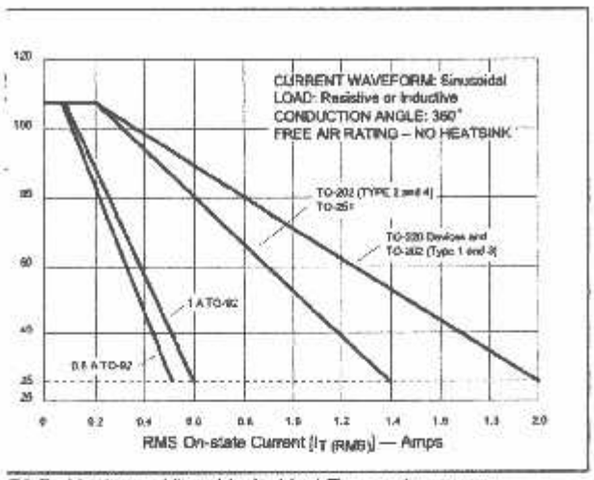


Figure E2.6 Maximum Allowable Case Temperature versus On-state Current (25 A and 35 A)



E2.7 Maximum Allowable Ambient Temperature versus On-state Current

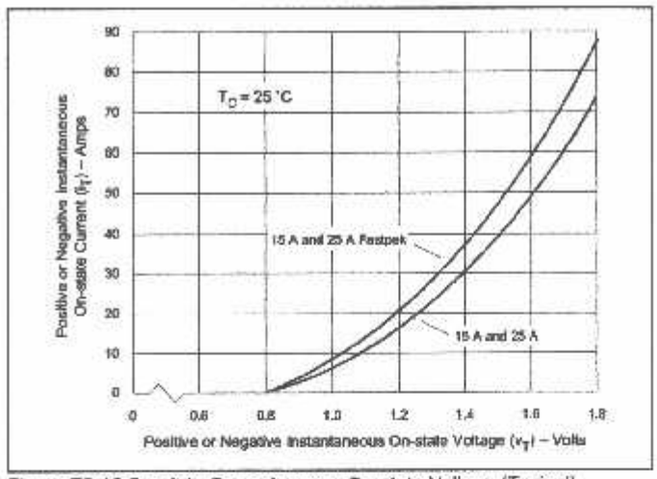
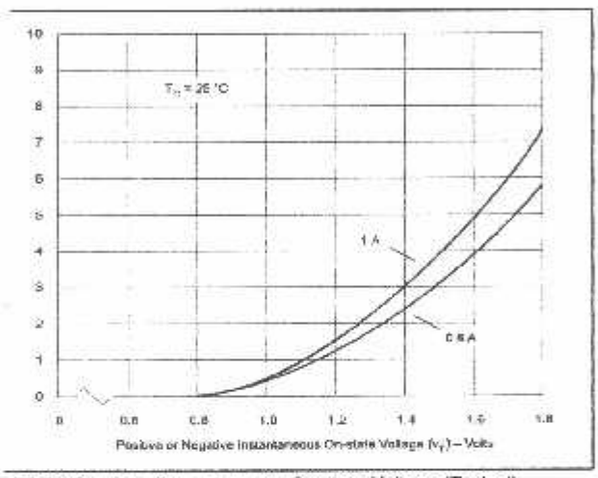


Figure E2.10 On-state Current versus On-state Voltage (Typical) (15 A and 25 A)



E2.8 On-state Current versus On-state Voltage (Typical) (0.8 A and 1 A)

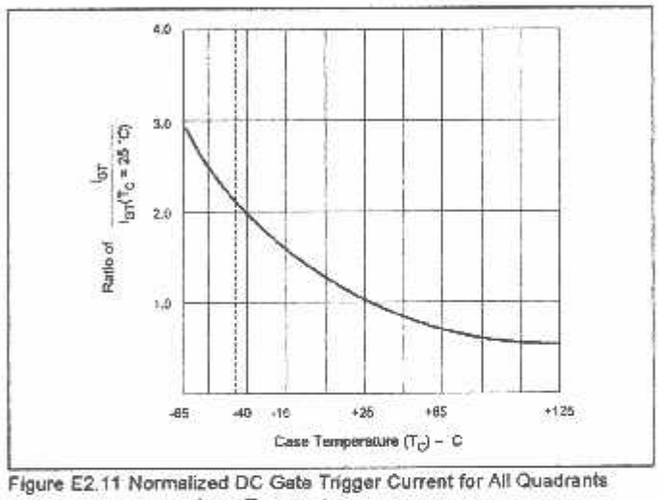
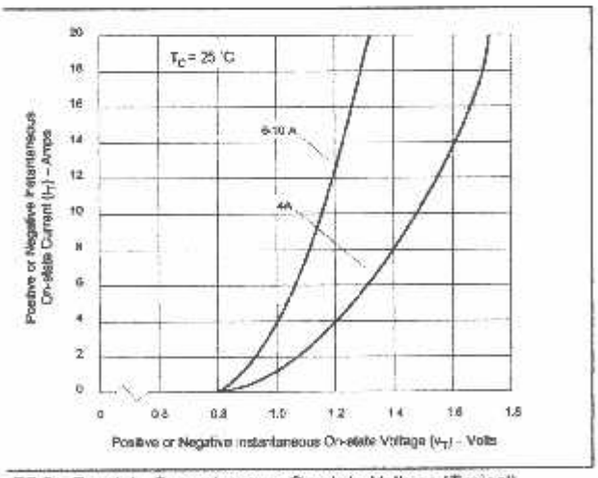


Figure E2.11 Normalized DC Gate Trigger Current for All Quadrants versus Case Temperature



E2.9 On-state Current versus On-state Voltage (Typical) (4 A, 6 A, 8 A, and 10 A)

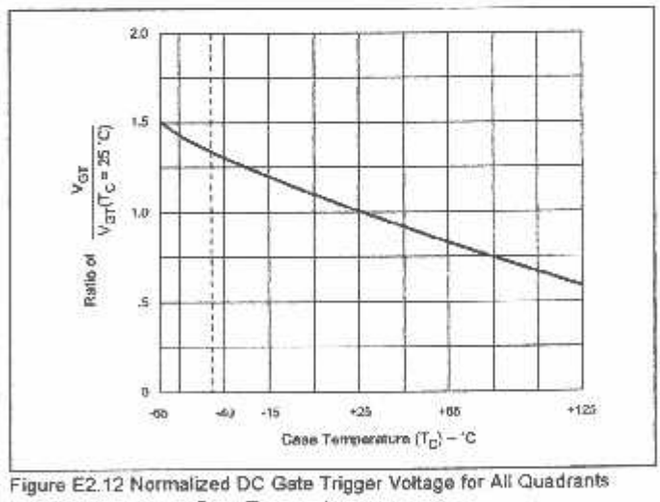
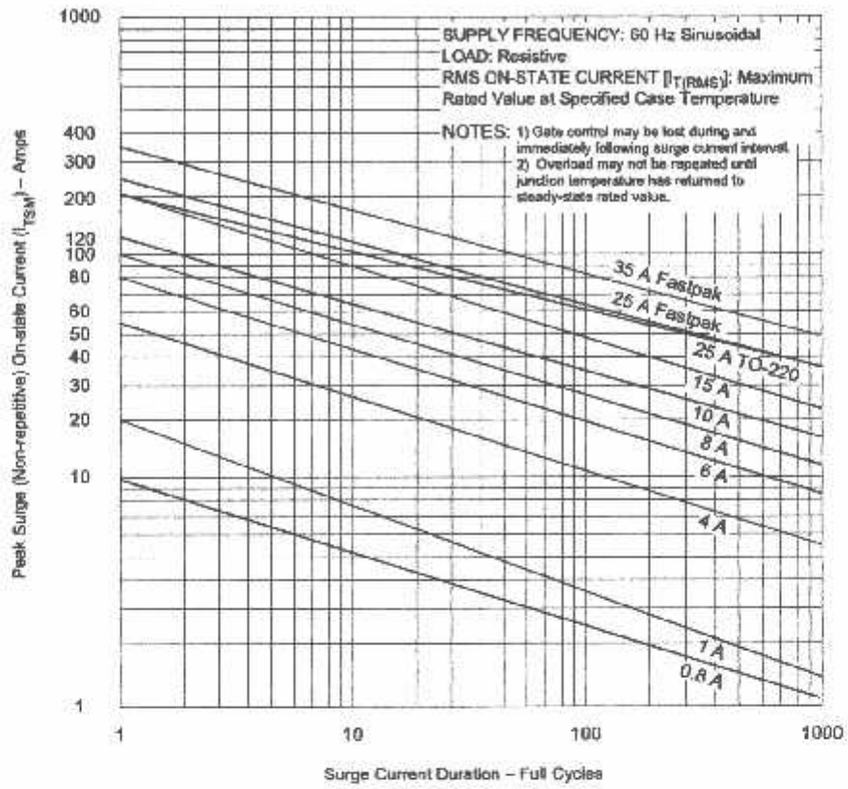
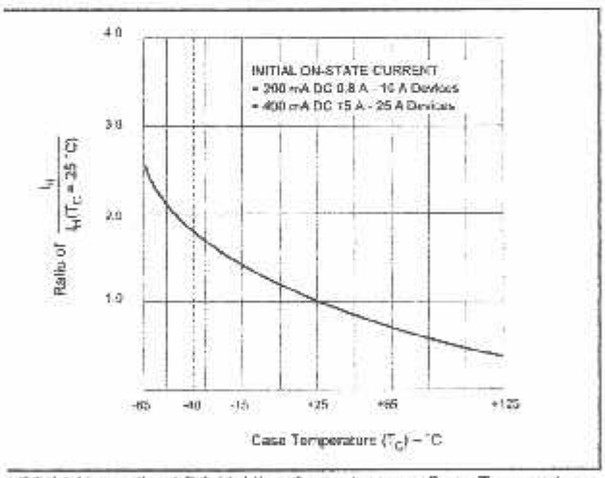


Figure E2.12 Normalized DC Gate Trigger Voltage for All Quadrants versus Case Temperature



e E2.13 Peak Surge Current versus Surge Current Duration



e E2.14 Normalized DC Holding Current versus Case Temperature

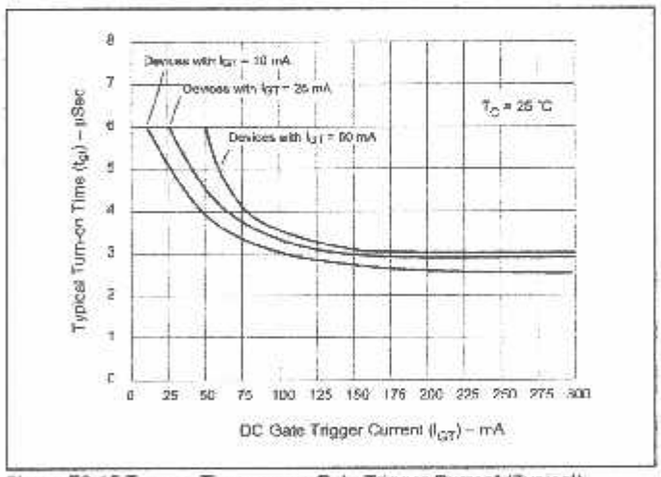
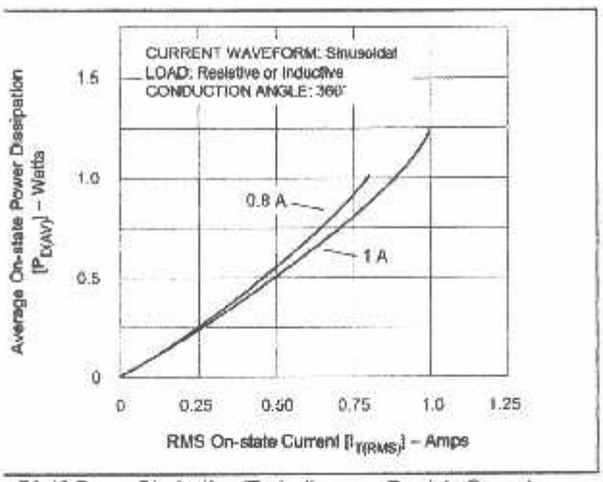


Figure E2.15 Turn-on Time versus Gate Trigger Current (Typical)



e E2.16 Power Dissipation (Typical) versus On-state Current (0 8 A and 1 A)

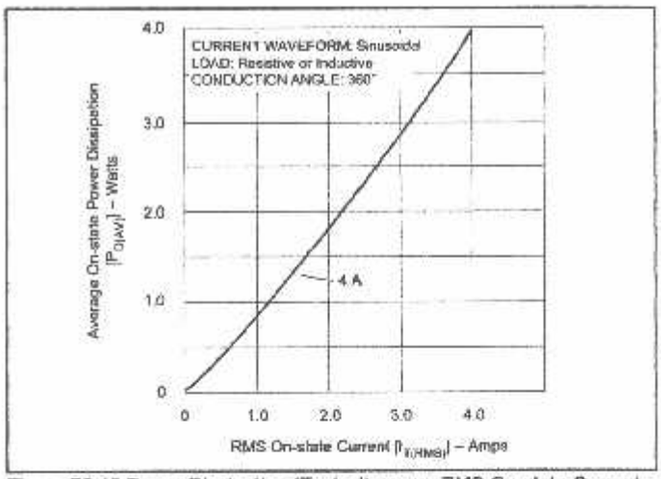
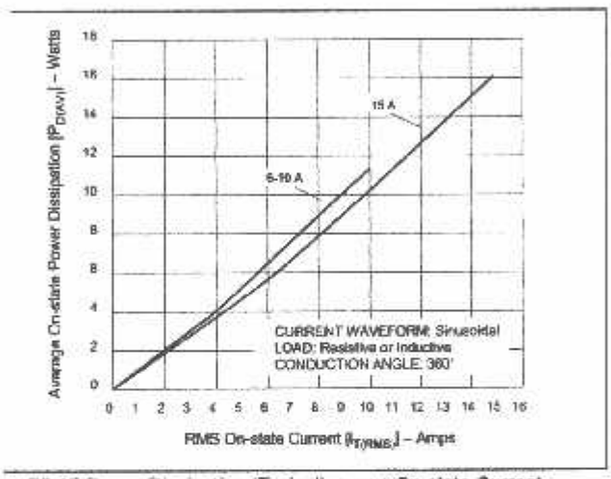
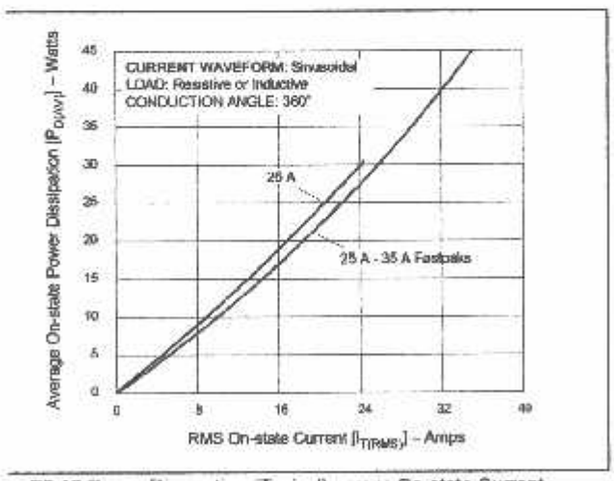


Figure E2.19 Power Dissipation (Typical) versus RMS On-state Current (4 A)



re E2.17 Power Dissipation (Typical) versus On-state Current (6 A to 10 A and 15 A)



re E2.18 Power Dissipation (Typical) versus On-state Current (25 A to 35 A)

GlobalOptoisolator™

VDE | UL | CSA | SETI | SEMKO | DEMKO | NEMKO | BABT

# MOC3021
[IFT = 15 mA Max]
# MOC3022
[IFT = 10 mA Max]
# MOC3023*
[IFT = 5 mA Max]

*Motorola Preferred Device

6-Pin DIP Random-Phase Optoisolators Triac Driver Output
(400 Volts Peak)

The MOC3020 Series consists of gallium arsenide infrared emitting diodes, optically coupled to a silicon bilateral switch.

- ***To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.***

They are designed for applications requiring isolated triac triggering.

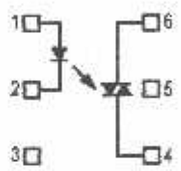
Recommended for 115/240 Vac(rms) Applications:

- Solenoid/Valve Controls
- Lamp Ballasts
- Interfacing Microprocessors to 115 Vac Peripherals
- Motor Controls
- Static ac Power Switch
- Solid State Relays
- Incandescent Lamp Dimmers

STYLE 6 PLASTIC

STANDARD THRU HOLE
CASE 730A–04

SCHEMATIC



1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE
   DO NOT CONNECT
6. MAIN TERMINAL

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE			
Reverse Voltage	V_R	3	Volts
Forward Current — Continuous	I_F	60	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Triac Driver Derate above 25°C	P_D	100 1.33	mW mW/°C
OUTPUT DRIVER			
Off-State Output Terminal Voltage	V_{DRM}	400	Volts
Peak Repetitive Surge Current (PW = 1 ms, 120 pps)	I_{TSM}	1	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 4	mW mW/°C
TOTAL DEVICE			
Isolation Surge Voltage(1) (Peak ac Voltage, 60 Hz, 1 Second Duration)	V_{ISO}	7500	Vac(pk)
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	330 4.4	mW mW/°C
Junction Temperature Range	T_J	−40 to +100	°C
Ambient Operating Temperature Range(2)	T_A	−40 to +85	°C
Storage Temperature Range(2)	T_{stg}	−40 to +150	°C
Soldering Temperature (10 s)	T_L	260	°C

1. Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.
2. Refer to Quality and Reliability Section in Opto Data Book for information on test conditions.

Preferred devices are Motorola recommended choices for future use and best overall value.
GlobalOptoisolator is a trademark of Motorola, Inc.

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
INPUT LED						
Reverse Leakage Current (V_R = 3 V)		I_R	—	0.05	100	µA
Forward Voltage (I_F = 10 mA)		V_F	—	1.15	1.5	Volts
OUTPUT DETECTOR (I_F = 0 unless otherwise noted)						
Peak Blocking Current, Either Direction (Rated V_{DRM}(1))		I_{DRM}	—	10	100	nA
Peak On–State Voltage, Either Direction (I_{TM} = 100 mA Peak)		V_{TM}	—	1.8	3	Volts
Critical Rate of Rise of Off–State Voltage (Figure 7, Note 2)		dv/dt	—	10	—	V/µs
COUPLED						
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3 V(3))	MOC3021	I_{FT}	—	8	15	mA
	MOC3022		—	—	10	
	MOC3023		—	—	5	
Holding Current, Either Direction		I_H	—	100	—	µA

1. Test voltage must be applied within dv/dt rating.
2. This is static dv/dt. See Figure 7 for test circuit. Commutating dv/dt is a function of the load–driving thyristor(s) only.
3. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (15 mA for MOC3021, 10 mA for MOC3022, 5 mA for MOC3023) and absolute max I_F (60 mA).

TYPICAL ELECTRICAL CHARACTERISTICS

T_A = 25°C

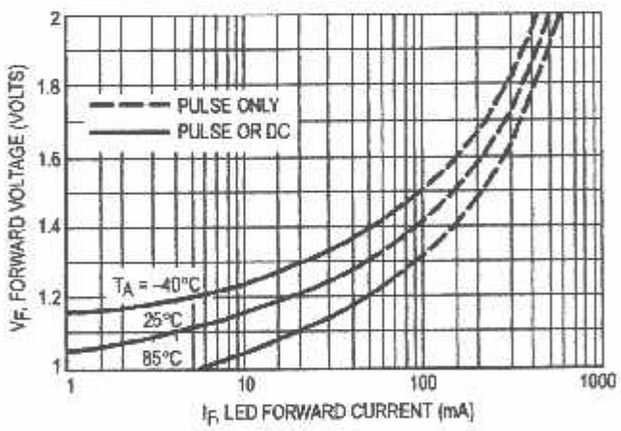


Figure 1. LED Forward Voltage versus Forward Current

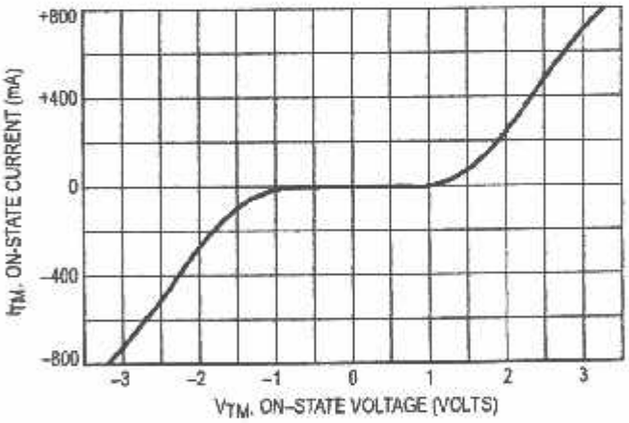


Figure 2. On–State Characteristics

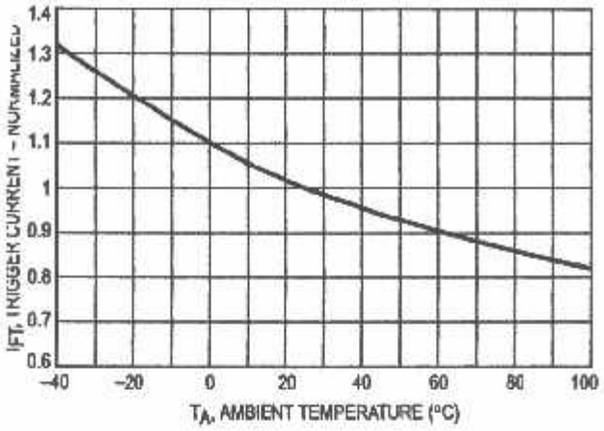


Figure 3. Trigger Current versus Temperature

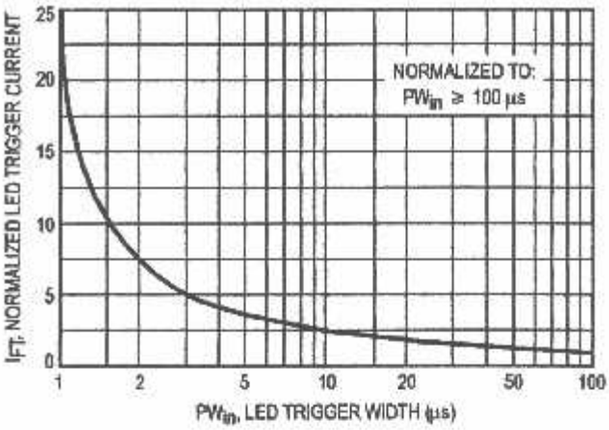


Figure 4. LED Current Required to Trigger versus LED Pulse Width

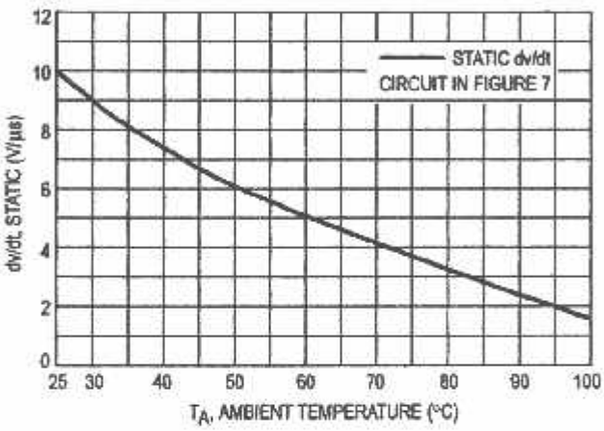


Figure 5. dv/dt versus Temperature

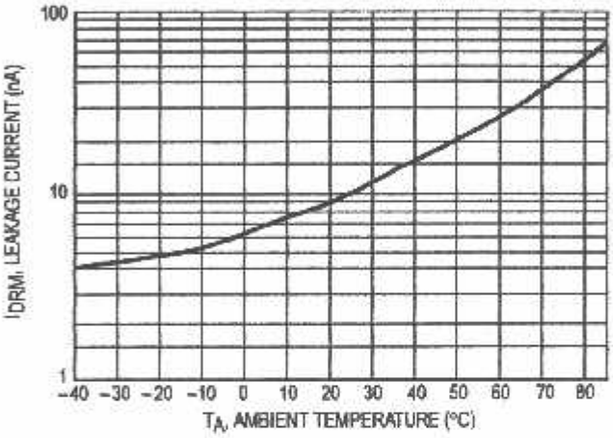
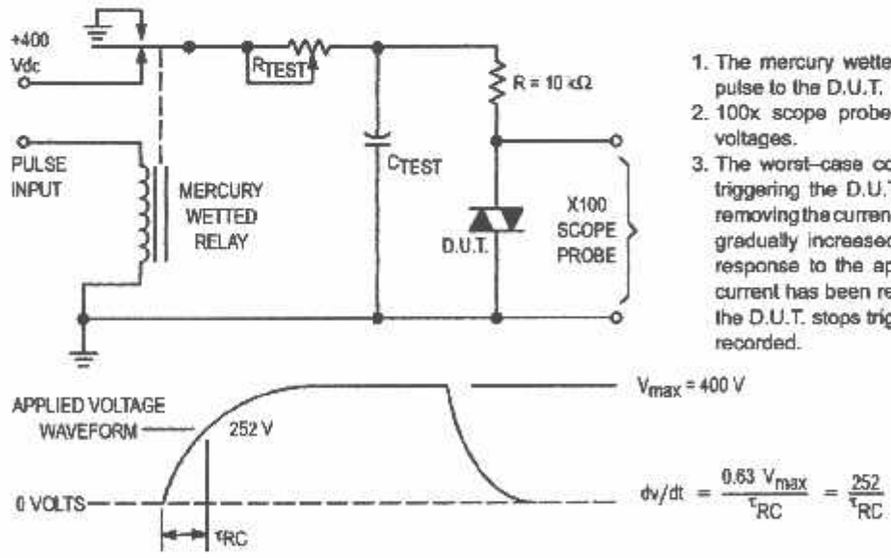
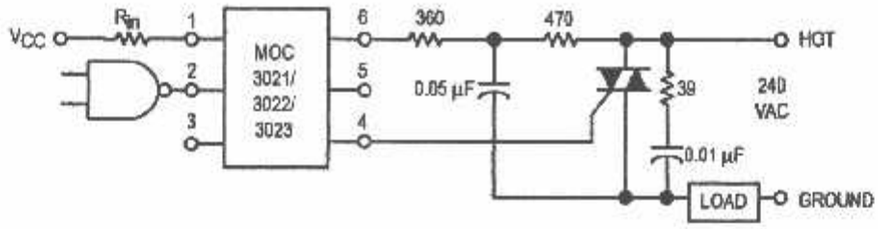


Figure 6. Leakage Current, I_{DRM} versus Temperature



1. The mercury wetted relay provides a high speed repeated pulse to the D.U.T.
2. 100x scope probes are used, to allow high speeds and voltages.
3. The worst–case condition for static dv/dt is established by triggering the D.U.T. with a normal LED input current, then removing the current. The variable R_{TEST} allows the dv/dt to be gradually increased until the D.U.T. continues to trigger in response to the applied voltage pulse, even after the LED current has been removed. The dv/dt is then decreased until the D.U.T. stops triggering. τ_{RC} is measured at this point and recorded.

Figure 7. Static dv/dt Test Circuit



his optoisolator should not be used to drive a load directly. It is in-nded to be a trigger device only.

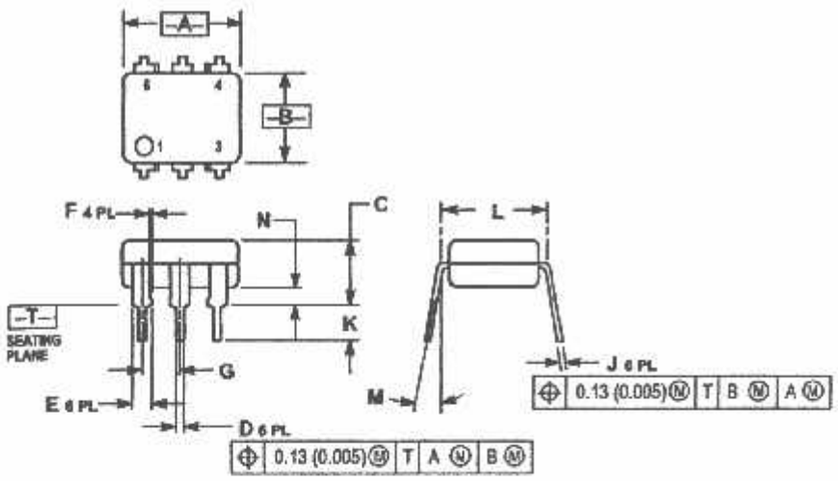
ditional information on the use of optically coupled triac /ers is available in Application Note AN–780A.

In this circuit the "hot" side of the line is switched and the load connected to the cold or ground side.

The 39 ohm resistor and 0.01 µF capacitor are for snubbing of the triac, and the 470 ohm resistor and 0.05 µF capacitor are for snubbing the coupler. These components may or may not be necessary depending upon the particular triac and load used.

Figure 8. Typical Application Circuit

PACKAGE DIMENSIONS

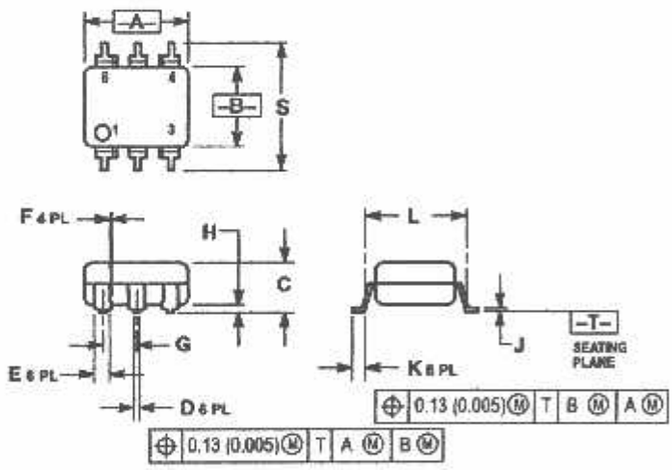


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.015	0.100	0.38	2.54

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE
6. MAIN TERMINAL

CASE 730A–04
ISSUE G



NOTES:
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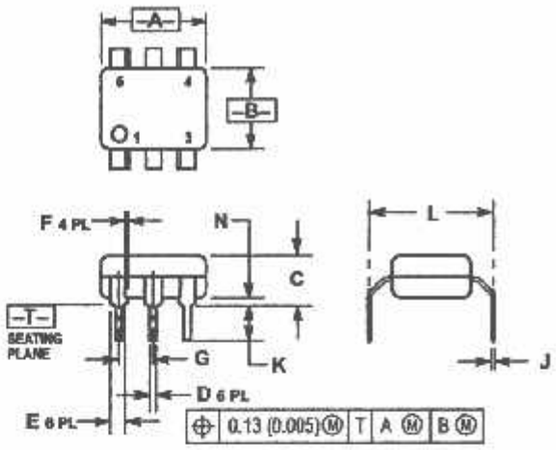
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
H	0.020	0.025	0.51	0.63
J	0.008	0.012	0.20	0.30
K	0.006	0.035	0.16	0.88
L	0.320 BSC		8.13 BSC	
S	0.332	0.390	8.43	9.90

***Consult factory for leadform option availability**

CASE 730C–04
ISSUE D



NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.92	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.400	0.425	10.16	10.80
N	0.015	0.040	0.38	1.02

***Consult factory for leadform option availability**

CASE 730D–05
ISSUE D

ow to reach us:
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HONG KONG: Motorola Semiconductors H.K. Ltd., 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

National Semiconductor

December 1994

LM158/LM258/LM358/LM2904
Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

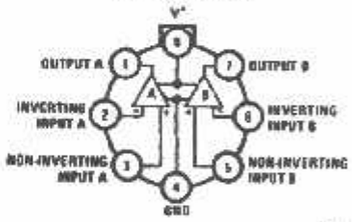
- Two internally compensated op amps in a single package
- Eliminates need for dual supplies
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) (temperature compensated) 1 MHz
- Wide power supply range:
  - Single supply 3V to 32V
  - or dual supplies ±1.5V to ±16V
- Very low supply current drain (500 μA)—essentially independent of supply voltage
- Low input offset voltage 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V^+ − 1.5V

Connection Diagrams (Top Views)

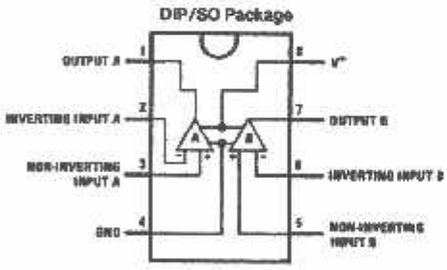
Metal Can Package



TL/H/7787–1

Order Number LM158AH, LM158AH/883*, LM158H, LM158H/883*, LM258H or LM358H
See NS Package Number H08C

DIP/SO Package



TL/H/7787–2

Order Number LM158J, LM158J/883*, LM158AJ or LM158AJ/883*
See NS Package Number J08A
Order Number LM358M, LM358AM or LM2904M
See NS Package Number M08A
Order Number LM358AN, LM358N or LM2904N
See NS Package Number N08E

*LM158 is available per SMD #5962-8771001
LM158A is available per SMD #5962-8771002

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 9)

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 1)		
Molded DIP	830 mW	830 mW
Metal Can	660 mW	
Small Outline Package (M)	590 mW	530 mW
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15V$ and $T_A = 25°C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3V$) (Note 3)	50 mA	50 mA

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Operating Temperature Range		
LM358	0°C to +70°C	−40°C to +85°C
LM258	−25°C to +85°C	
LM158	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature, DIP (Soldering, 10 seconds)	260°C	260°C
Lead Temperature, Metal Can (Soldering, 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics $V^+ = +5.0V$, unless otherwise stated

Parameter	Conditions	LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 5), $T_A = 25°C$		1	2		2	3		2	5		2	7		2	7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$, $V_{CM} = 0V$, (Note 6)		20	50		45	100		45	150		45	250		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		2	10		5	30		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range	$V^+ = 30V$, (Note 7) (LM2904, $V^+ = 26V$), $T_A = 25°C$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps $V^+ = 30V$ (LM2904 $V^+ = 26V$) $V^+ = 5V$		1 0.5	2 1.2		1 0.5	2 1.2		1 0.5	2 1.2		1 0.5	2 1.2		1 0.5	2 1.2	mA mA

Electrical Characteristics (Continued) $V^+ = +5.0V$, Note 4, unless otherwise stated

Parameter		Conditions	LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		$V^+ = 15V$, $T_A = 25°C$, $R_L \geq 2\ k\Omega$, (For $V_O = 1V$ to 11V)	50	100		25	100		50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio		$T_A = 25°C$, $V_{CM} = 0V$ to $V^+ - 1.5V$	70	85		65	85		70	85		65	85		50	70		dB
Power Supply Rejection Ratio		$V^+ = 5V$ to 30V (LM2904, $V^+ = 5V$ to 26V), $T_A = 25°C$	65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling		$f = 1$ kHz to 20 kHz, $T_A = 25°C$ (Input Referred), (Note 8)		−120			−120			−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		mA
	Sink	$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $T_A = 25°C$, $V_O = 2V$	10	20		10	20		10	20		10	20		10	20		mA
		$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $T_A = 25°C$, $V_O = 200$ mV, $V^+ = 15V$	12	50		12	50		12	50		12	50		12	50		µA
Short Circuit to Ground		$T_A = 25°C$, (Note 2), $V^+ = 15V$		40	60		40	60		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 5)			4			5			7			9			10	mV
Input Offset Voltage Drift		$R_S = 0\Omega$		7	15		7	20		7			7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			30			75			100			150		45	200	nA
Input Offset Current Drift		$R_S = 0\Omega$		10	200		10	300		10			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	200		40	300		40	500		40	500	nA

Electrical Characteristics (Continued) $V^+ = +5.0V$, Note 4, unless otherwise stated

Parameter		Conditions		LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Common-Mode Voltage Range		$V^+ = 30$ V, (Note 7) (LM2904, $V^+ = 26V$)		0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V
Large Signal Voltage Gain		$V^+ = +15V$ (V_O = 1V to 11V) $R_L \geq 2\ k\Omega$		25			15			25			15			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = +30V$ (LM2904, $V^+ = 26V$)	$R_L = 2\ k\Omega$	26			26			26			26			22			V
			$R_L = 10\ k\Omega$	27	28		27	28		27	28		27	28		23	24		V
	V_{OL}	$V^+ = 5V$, $R_L = 10\ k\Omega$			5	20		5	20		5	20		5	20		5	100	mV
Output Current	Source	$V_{IN}^+ = +1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$		10	20		10	20		10	20		10	20		10	20		mA
	Sink	$V_{IN}^- = +1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 2V$		10	15		5	8		5	8		5	8		5	8		mA

Note 1: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 120°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +18V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$ for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM358/LM358A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2904 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O \approx 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$) at 25°C. For LM2904, V^+ from 5V to 26V.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2904), independent of the magnitude of V^+.

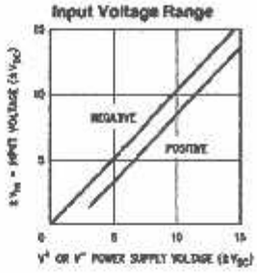
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

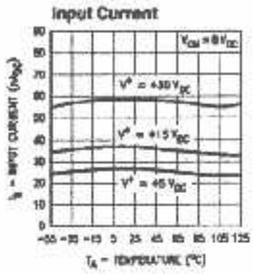
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

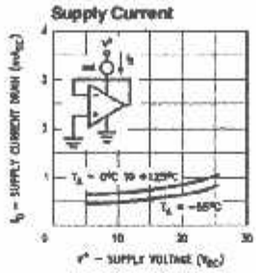
Input Voltage Range



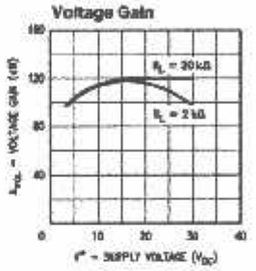
Input Current



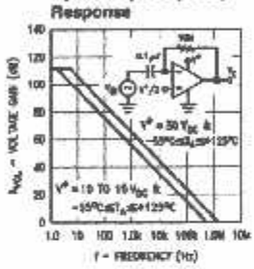
Supply Current



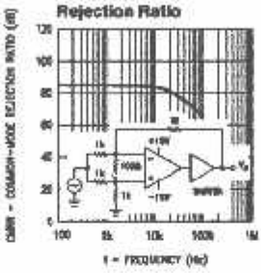
Voltage Gain



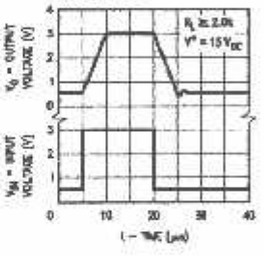
Open Loop Frequency Response



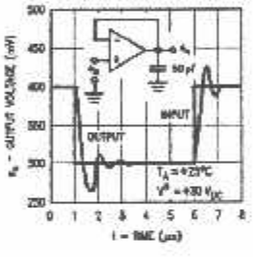
Common-Mode Rejection Ratio



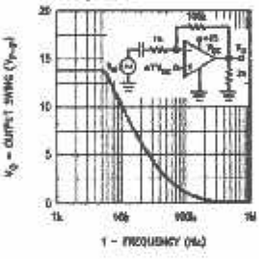
Voltage Follower Pulse Response



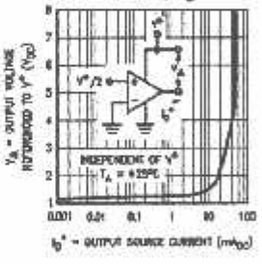
Voltage Follower Pulse Response (Small Signal)



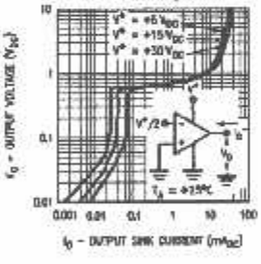
Large Signal Frequency Response



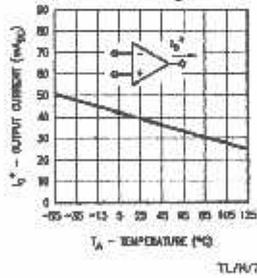
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



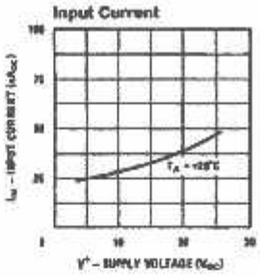
Current Limiting



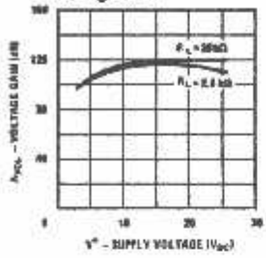
TL/H/7787-4

Typical Performance Characteristics (Continued) (LM2902 only)

Input Current



Voltage Gain



TL/H/7787–6

Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accomodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accomodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

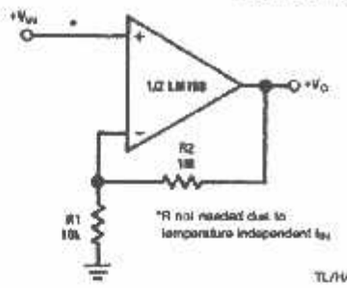
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

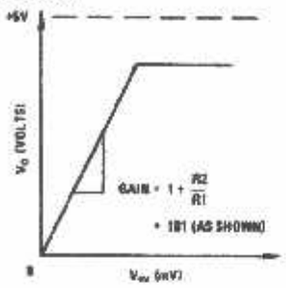
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Non-Inverting DC Gain (0V Input = 0V Output)

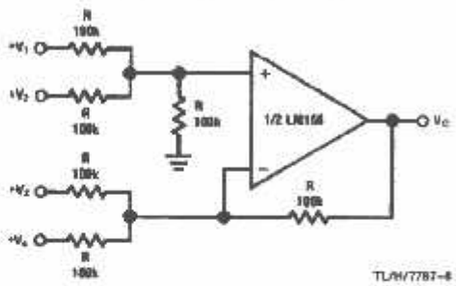


TL/H/7787–6



TL/H/7787–7

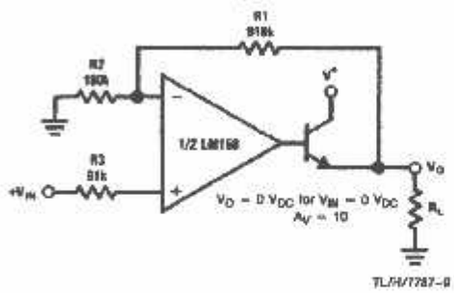
DC Summing Amplifier
(V_{IN}'s ≥ 0 V_{DC} and V_O ≥ 0 V_{DC})



TL/H/7787–8

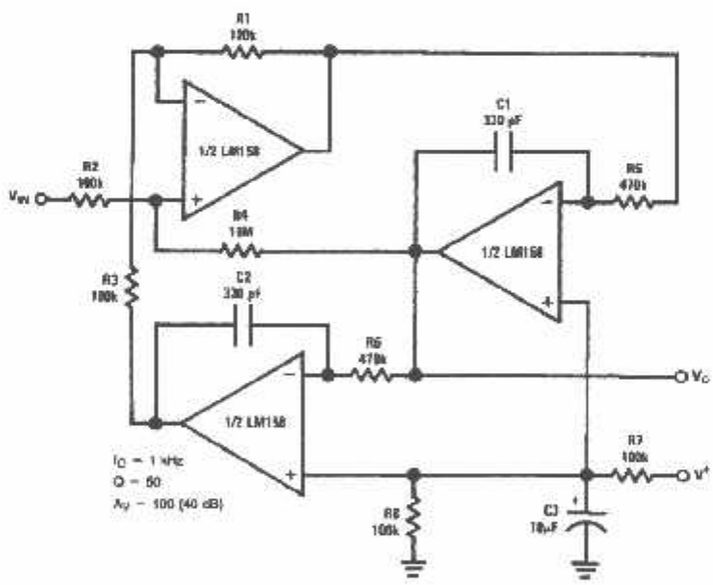
Where: $V_O = V_1 + V_2 + V_3 + V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O \geq 0\ V_{DC}$

Power Amplifier



TL/H/7787–9

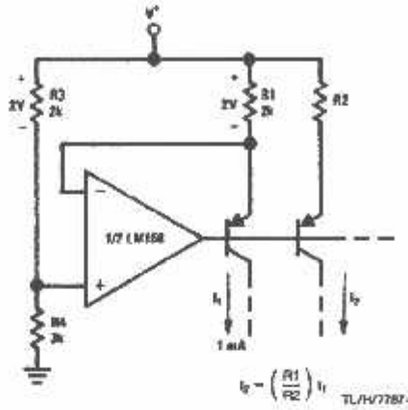
"Bi-QUAD" RC Active Bandpass Filter



TL/H/7787–10

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

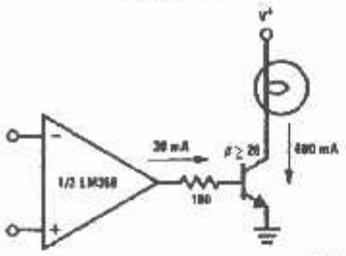
Fixed Current Sources



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

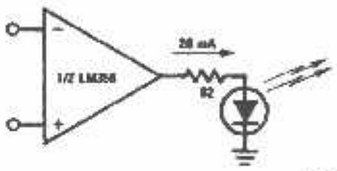
TL/H/7787–11

Lamp Driver



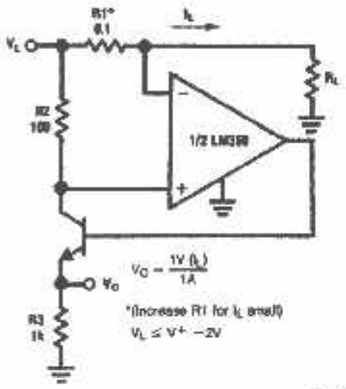
TL/H/7787–12

LED Driver



TL/H/7787–13

Current Monitor



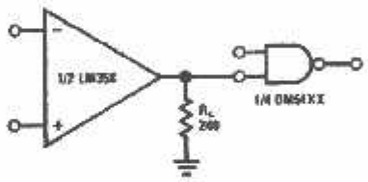
$$V_O = \frac{1V\ (I_L)}{1A}$$

*(Increase R1 for I_L small)

$V_L \leq V^+ - 2V$

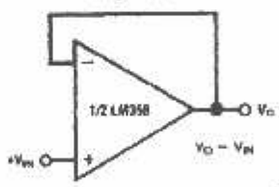
TL/H/7787–14

Driving TTL



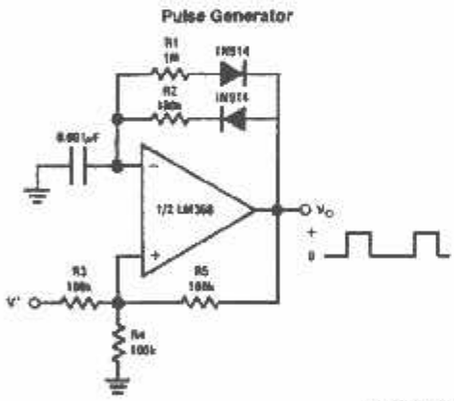
TL/H/7787–15

Voltage Follower



TL/H/7787–17

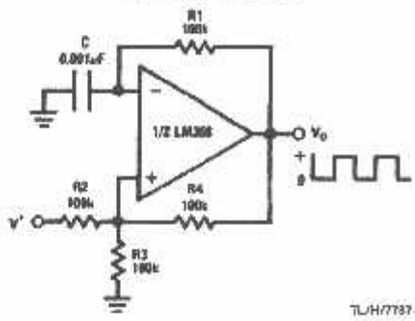
Pulse Generator



TL/H/7787–16

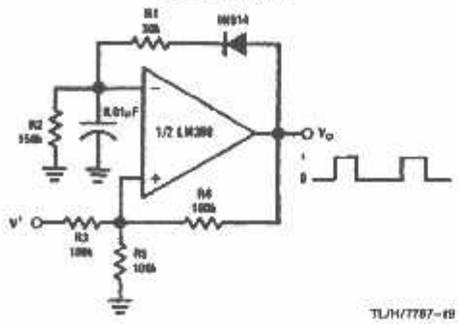
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Squarewave Oscillator



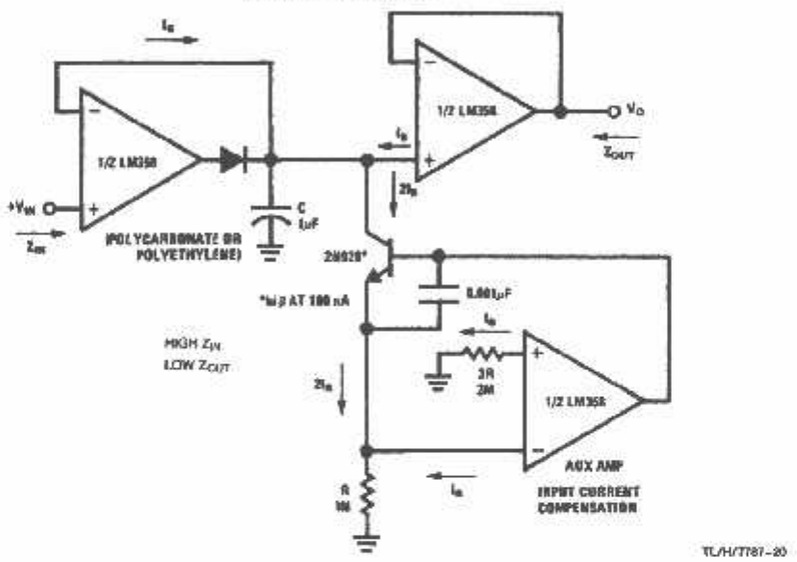
TL/H/7787–18

Pulse Generator



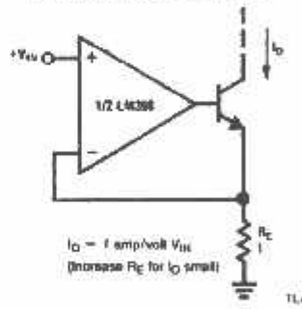
TL/H/7787–19

Low Drift Peak Detector



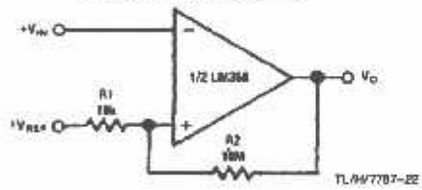
TL/H/7787–20

High Compliance Current Sink



TL/H/7787–21

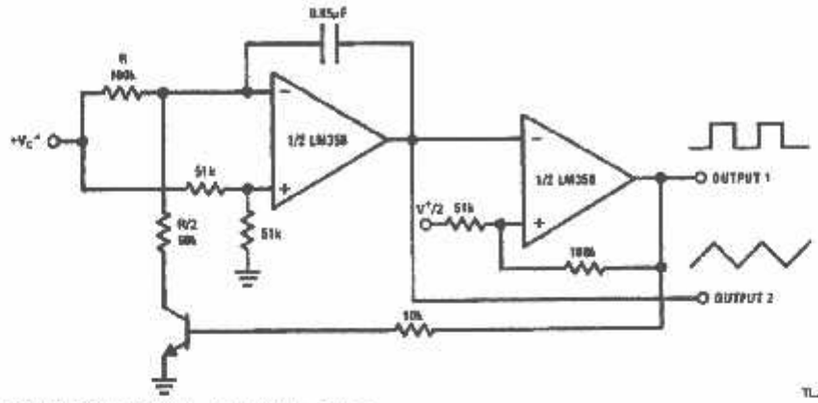
Comparator with Hysteresis



TL/H/7787–22

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

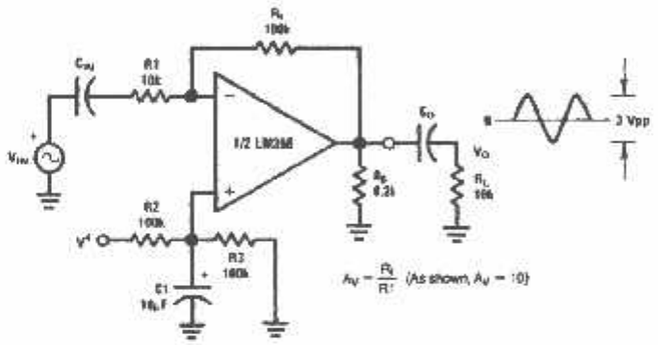
Voltage Controlled Oscillator (VCO)



TL/H/7787–23

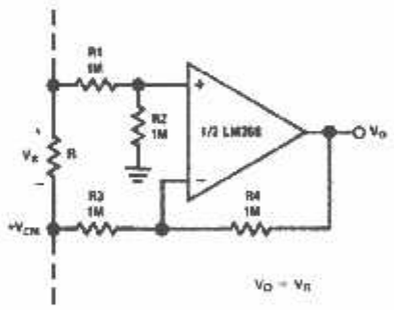
*WIDE CONTROL VOLTAGE RANGE: 0 $V_{DC} \leq V_C \leq 8$ ($V^+ - 1.5V_{DC}$)

AC Coupled Inverting Amplifier



TL/H/7787–24

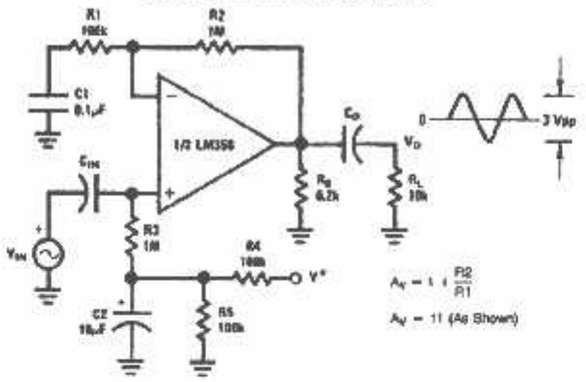
Ground Referencing a Differential Input Signal



TL/H/7787–25

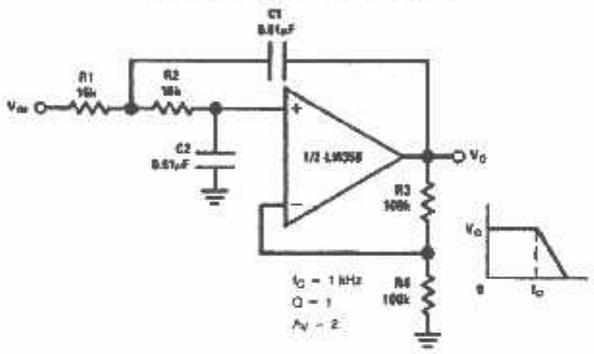
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

AC Coupled Non-Inverting Amplifier



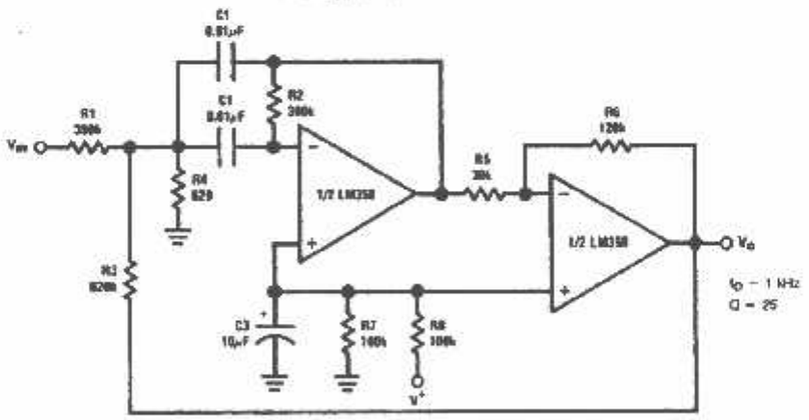
TL/H/7787–26

DC Coupled Low-Pass RC Active Filter



TL/H/7787–27

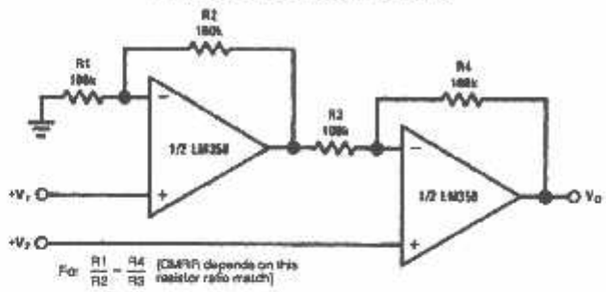
Bandpass Active Filter



TL/H/7787–28

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

High Input Z, DC Differential Amplifier



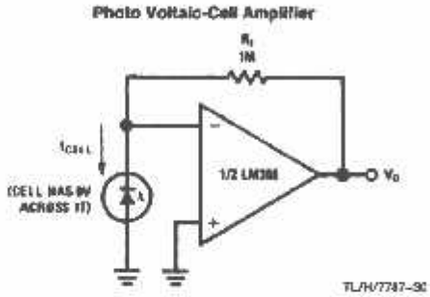
TL/H/7787–29

For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

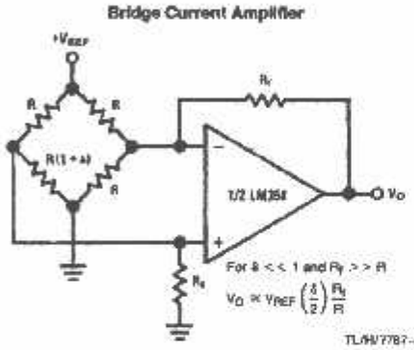
As Shown $V_O = 2(V_2 - V_1)$

Photo Voltaic-Cell Amplifier



TL/H/7787–30

Bridge Current Amplifier

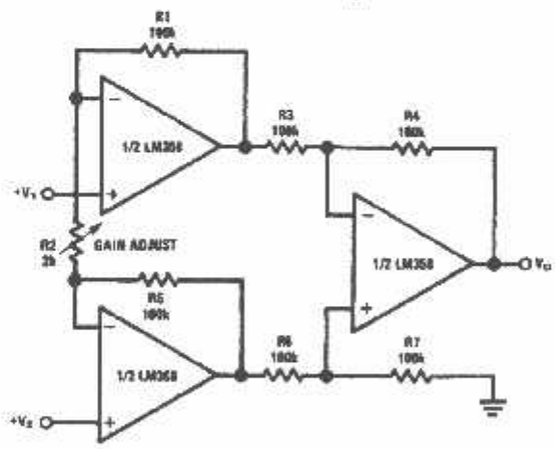


For $\delta << 1$ and $R_F >> R$

$V_O \propto V_{REF}\left(\frac{\delta}{2}\right)\frac{R_F}{R}$

TL/H/7787–33

High Input Z Adjustable-Gain DC Instrumentation Amplifier



TL/H/7787–31

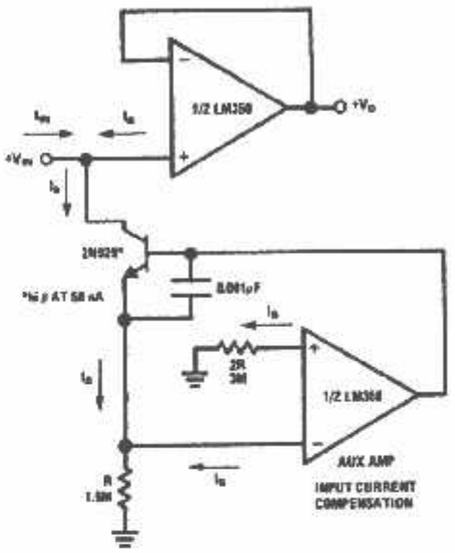
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$

As shown $V_O = 101(V_2 - V_1)$

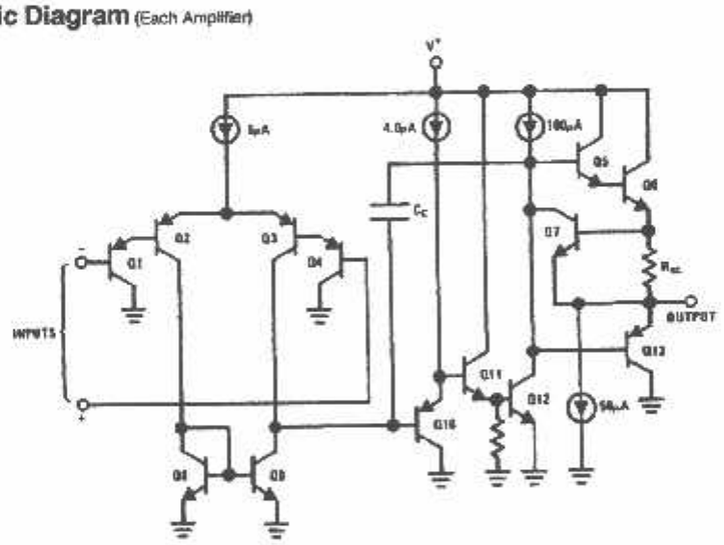
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



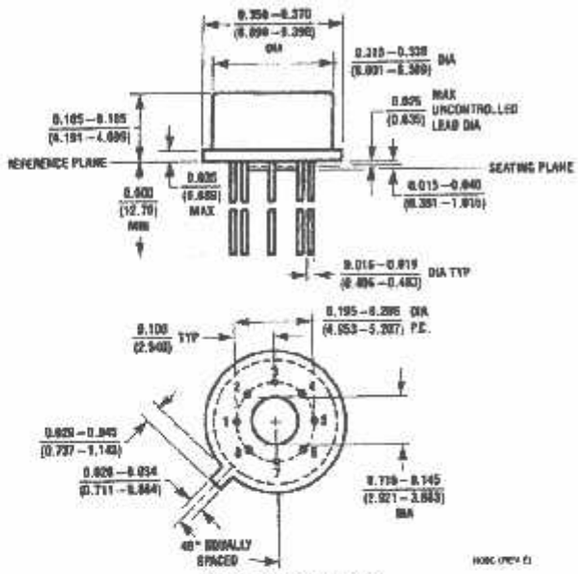
TL/H/7787–32

Schematic Diagram (Each Amplifier)



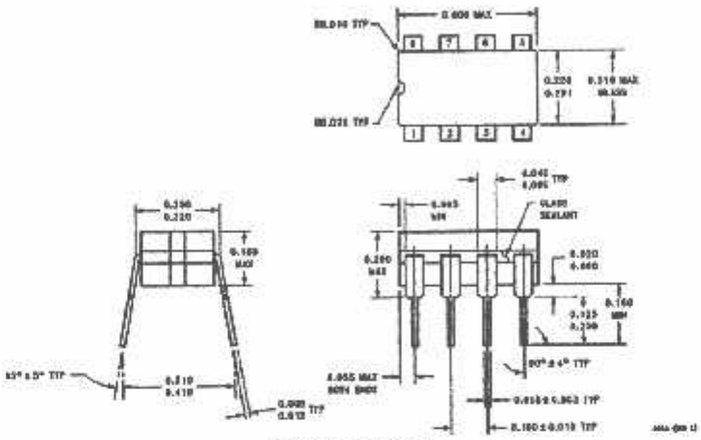
TL/H/7787–3

Physical Dimensions inches (millimeters)

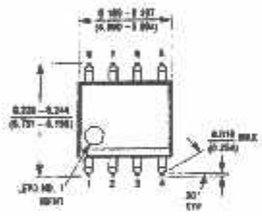


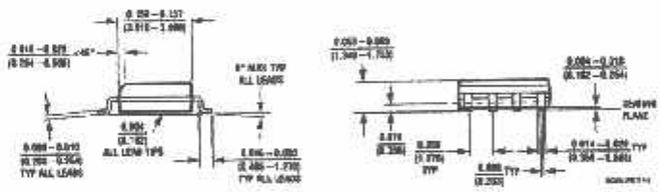
Metal Can Package (H)
Order Number LM158AH, LM158AH/883, LM158H, LM158H/883, LM258H or LM358H
NS Package Number H08C

Physical Dimensions inches (millimeters) (Continued)



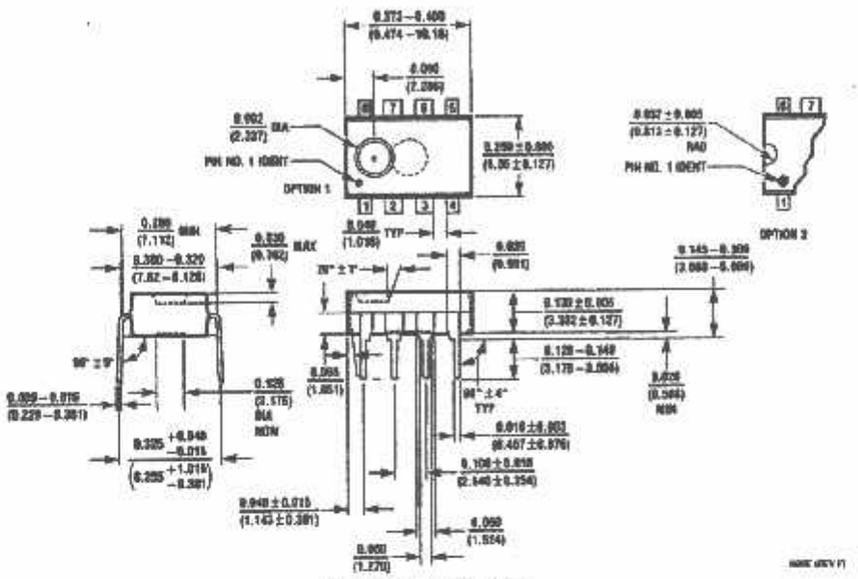
Cerdip Package (J)
Order Number LM158J, LM158J/883, LM158AJ or LM158AJ/883
NS Package Number J08A





S.O. Package (M)
Order Number LM358M, LM358AM or LM2904M
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dip Package (N)
Order Number LM358AN, LM358N or LM2904N
NS Package Number N08E

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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November 2000

National Semiconductor

LM35
Precision Centigrade Temperature Sensors

General Description

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to +110°C range (−10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full −55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 µA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ω for 1 mA load

Typical Applications

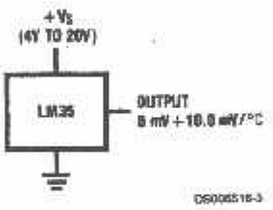
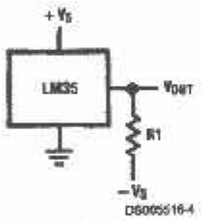


FIGURE 1. Basic Centigrade Temperature Sensor (+2°C to +150°C)

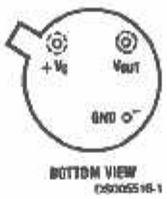


Choose $R_1 = -V_S/50\ \mu A$
V_{OUT} = +1,500 mV at +150°C
= +250 mV at +25°C
= −550 mV at −55°C

FIGURE 2. Full-Range Centigrade Temperature Sensor

Connection Diagrams

TO-46
Metal Can Package*



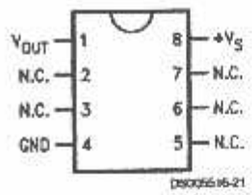
*Case is connected to negative pin (GND)

Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

TO-92
Plastic Package

Order Number LM35CZ, LM35CAZ or LM35DZ
See NS Package Number Z03A

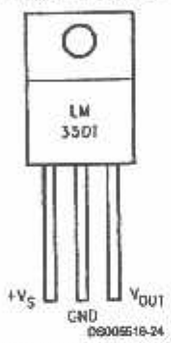
SO-8
Small Outline Molded Package



N.C. = No Connection

Top View
Order Number LM35DM
See NS Package Number M08A

TO-220
Plastic Package*



*Tab is connected to the negative pin (GND).
Note: The LM35DT pinout is different than the discontinued LM35DP.

Order Number LM35DT
See NS Package Number TA03F

bsolute Maximum Ratings (Note 10)

Military/Aerospace specified devices are required, ease contact the National Semiconductor Sales Office/ stributors for availability and specifications.

pply Voltage	+35V to −0.2V
itput Voltage	+6V to −1.0V
tput Current	10 mA
torage Temp.;	
TO-46 Package,	−60°C to +180°C
TO-92 Package,	−60°C to +150°C
SO-8 Package,	−65°C to +150°C
TO-220 Package,	−65°C to +150°C
ead Temp.:	
TO-46 Package, (Soldering, 10 seconds)	300°C
TO-92 and TO-220 Package, (Soldering, 10 seconds)	260°C
SO Package (Note 12)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	2500V
Specified Operating Temperature Range: T_{MIN} to T_{MAX} (Note 2)	
LM35, LM35A	−55°C to +150°C
LM35C, LM35CA	−40°C to +110°C
LM35D	0°C to +100°C

lectrical Characteristics

lotes 1, 6)

Parameter	Conditions	LM35A			LM35CA			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
curacy	T_A=+25°C	±0.2	±0.5		±0.2	±0.5		°C
ote 7)	T_A=−10°C	±0.3			±0.3		±1.0	°C
	T_A=T_{MAX}	±0.4	±1.0		±0.4	±1.0		°C
	T_A=T_{MIN}	±0.4	±1.0		±0.4		±1.5	°C
nlinearity ote 8)	T_{MIN}≤T_A≤T_{MAX}	**±0.18**		**±0.35**	**±0.15**		**±0.3**	°C
nsor Gain verage Slope)	T_{MIN}≤T_A≤T_{MAX}	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°C
ad Regulation	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		mV/mA
ote 3) 0≤I_L≤1 mA	T_{MIN}≤T_A≤T_{MAX}	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
e Regulation	T_A=+25°C	±0.01	±0.05		±0.01	±0.05		mV/V
ote 3)	4V≤V_S≤30V	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
iescent Current	V_S=+5V, +25°C	56	67		56	67		µA
ote 9)	V_S=+5V	**105**		**131**	**91**		**114**	µA
	V_S=+30V, +25°C	56.2	68		56.2	68		µA
	V_S=+30V	**105.5**		**133**	**91.5**		**116**	µA
ange of iescent Current ote 3)	4V≤V_S≤30V, +25°C	0.2	1.0		0.2	1.0		µA
	4V≤V_S≤30V	**0.5**		**2.0**	**0.5**		**2.0**	µA
mperature efficient of iescent Current		**+0.39**		**+0.5**	**+0.39**		**+0.5**	µA/°C
imum Temperature Rated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
ng Term Stability	T_J=T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Electrical Characteristics

(Notes 1, 6)

Parameter	Conditions	LM35			LM35C, LM35D			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy, LM35, LM35C (Note 7)	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		°C
	T_A=−10°C	±0.5			±0.5		±1.5	°C
	T_A=T_{MAX}	±0.8	±1.5		±0.8		±1.5	°C
	T_A=T_{MIN}	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D (Note 7)	T_A=+25°C				±0.6	±1.5		°C
	T_A=T_{MAX}				±0.9		±2.0	°C
	T_A=T_{MIN}				±0.9		±2.0	°C
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.3**		**±0.5**	**±0.2**		**±0.5**	°C
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°C
Load Regulation (Note 3) $0 \le I_L \le 1$ mA	T_A=+25°C	±0.4	±2.0		±0.4	±2.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±5.0**	**±0.5**		**±5.0**	mV/mA
Line Regulation (Note 3)	T_A=+25°C	±0.01	±0.1		±0.01	±0.1		mV/V
	$4V \le V_S \le 30V$	**±0.02**		**±0.2**	**±0.02**		**±0.2**	mV/V
Quiescent Current (Note 9)	V_S=+5V, +25°C	56	80		56	80		µA
	V_S=+5V	**105**		**158**	**91**		**138**	µA
	V_S=+30V, +25°C	56.2	82		56.2	82		µA
	V_S=+30V	**105.5**		**161**	**91.5**		**141**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +25°C	0.2	2.0		0.2	2.0		µA
	$4V \le V_S \le 30V$	**0.5**		**3.0**	**0.5**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.7**	**+0.39**		**+0.7**	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	T_J=T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Note 1: Unless otherwise noted, these specifications apply: $-55°C \le T_J \le +150°C$ for the LM35 and LM35A; $-40°C \le T_J \le +110°C$ for the LM35C and LM35CA; and $0°C \le T_J \le +100°C$ for the LM35D. V_S=+5Vdc and I_{LOAD}=50 µA, in the circuit of *Figure 2*. These specifications also apply from +2°C to T_{MAX} in the circuit of *Figure 1*. Specifications in **boldface** apply over the full rated temperature range.

Note 2: Thermal resistance of the TO-46 package is 400°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient. Thermal resistance of the small outline molded package is 220°C/W junction to ambient. Thermal resistance of the TO-220 package is 90°C/W junction to ambient. For additional thermal resistance information see table in the Applications section.

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in **boldface** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mV/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

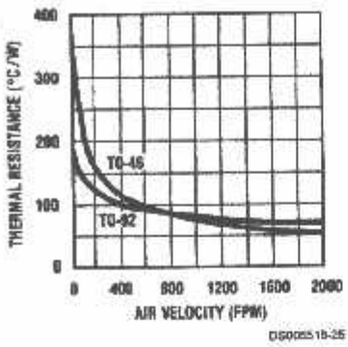
Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 12: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

ypical Performance Characteristics

hermal Resistance
unction to Air



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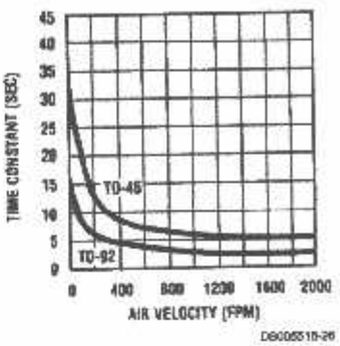
Thermal Time Constant



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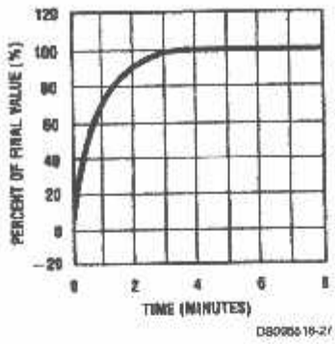
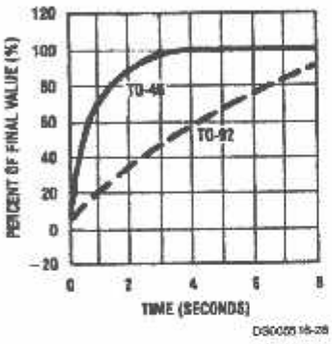
Thermal Response
In Still Air



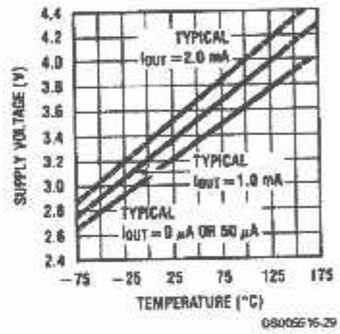
DS005516-27

hermal Response In
tirred Oil Bath



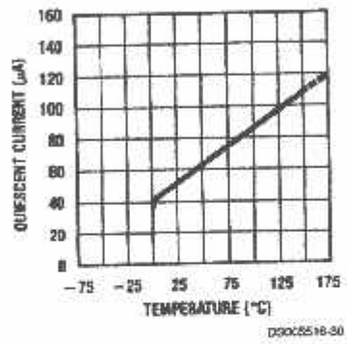
DS005516-28

Minimum Supply
Voltage vs. Temperature



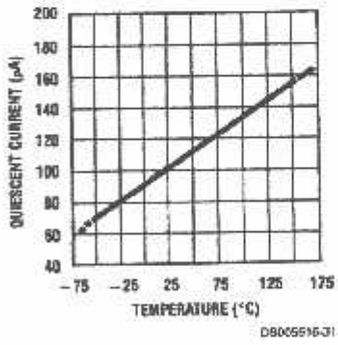
DS005516-29

Quiescent Current
vs. Temperature
(In Circuit of *Figure 1.*)



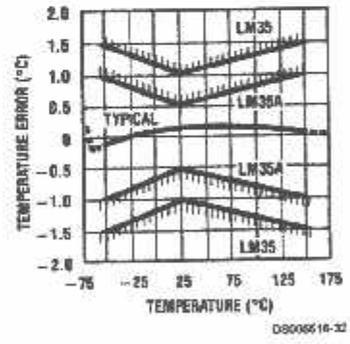
DS005516-30

Quiescent Current
vs. Temperature
(In Circuit of *Figure 2.*)



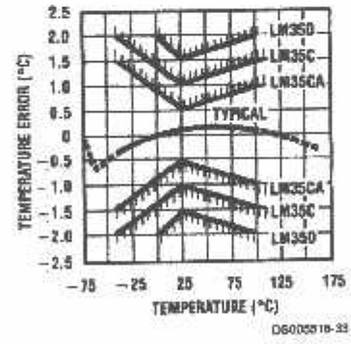
DS005516-31

Accuracy vs. Temperature
(Guaranteed)



DS005516-32

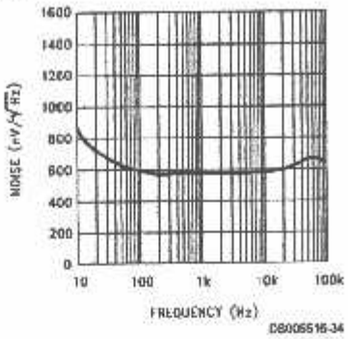
Accuracy vs. Temperature
(Guaranteed)



DS005516-33

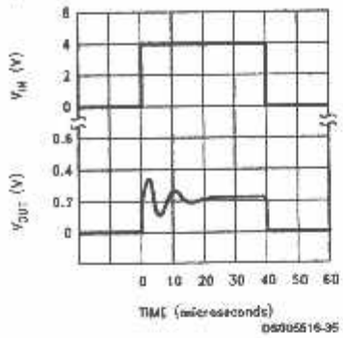
Typical Performance Characteristics (Continued)

Noise Voltage



DS005516-34

Start-Up Response



DS005516-35

Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01°C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM35 die would be at an intermediate temperature between the surface temperature and the air temperature. This is especially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM35, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM35 die's temperature will not be affected by the air temperature.

The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course, in that case the V− terminal of the circuit will be grounded to that metal. Alternatively, the LM35 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM35 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM35 or its connections.

These devices are sometimes soldered to a small light-weight heat fin, to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor, to give the steadiest reading despite small deviations in the air temperature.

Temperature Rise of LM35 Due To Self-heating (Thermal Resistance, θ_{JA})

	TO-46, no heat sink	TO-46*, small heat fin	TO-92, no heat sink	TO-92**, small heat fin	SO-8 no heat sink	SO-8** small heat fin	TO-220 no heat sink
Still air	400°C/W	100°C/W	180°C/W	140°C/W	220°C/W	110°C/W	90°C/W
Moving air	100°C/W	40°C/W	90°C/W	70°C/W	105°C/W	90°C/W	26°C/W
Still oil	100°C/W	40°C/W	90°C/W	70°C/W			
Stirred oil	50°C/W	30°C/W	45°C/W	40°C/W			
(Clamped to metal, infinite heat sink)	(24°C/W)				(55°C/W)		

*Wakefield type 201, or 1" disc of 0.020" sheet brass, soldered to case, or similar.
**TO-92 and SO-8 packages glued and leads soldered to 1" square of 1/16" printed circuit board with 2 oz. foil or similar.

Typical Applications

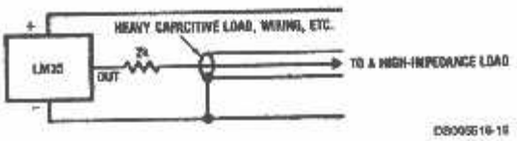


FIGURE 3. LM35 with Decoupling from Capacitive Load

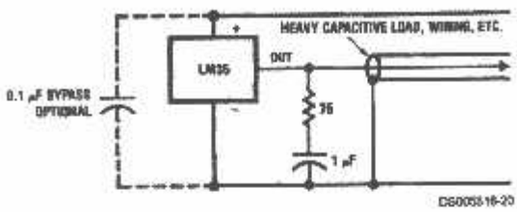


FIGURE 4. LM35 with R-C Damper

CAPACITIVE LOADS

Like most micropower circuits, the LM35 has a limited ability to drive heavy capacitive loads. The LM35 by itself is able to drive 50 pf without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure 3*. Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure 4*.

When the LM35 is applied with a 200Ω load resistor as shown in *Figure 5*, *Figure 6* or *Figure 8* it is relatively immune to wiring capacitance because the capacitance forms a bypass from ground to input, not on the output. However, as with any linear circuit connected to wires in a hostile environment, its performance can be affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR transients, etc, as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from V_{IN} to ground and a series R-C damper such as 75Ω in series with 0.2 or 1 µF from output to ground are often useful. These are shown in *Figure 13*, *Figure 14*, and *Figure 16*.

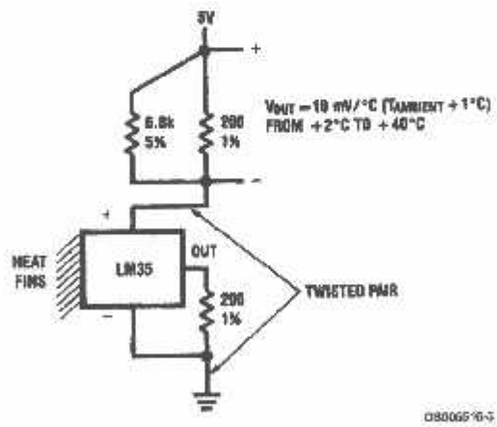


FIGURE 5. Two-Wire Remote Temperature Sensor (Grounded Sensor)

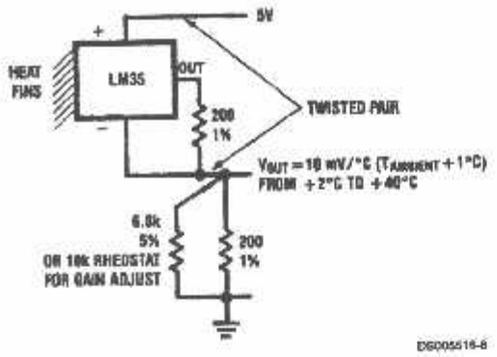


FIGURE 6. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

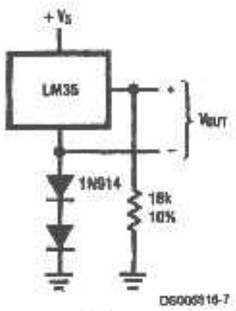


FIGURE 7. Temperature Sensor, Single Supply, −55° to +150°C

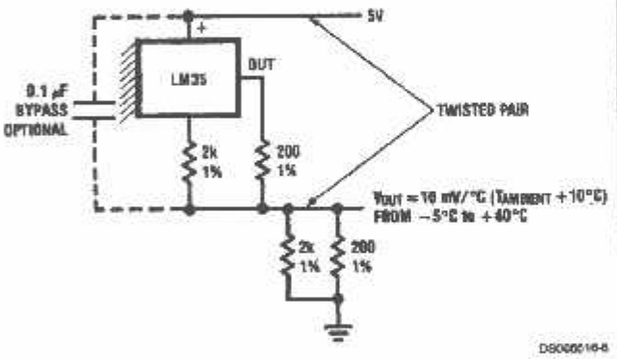


FIGURE 8. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

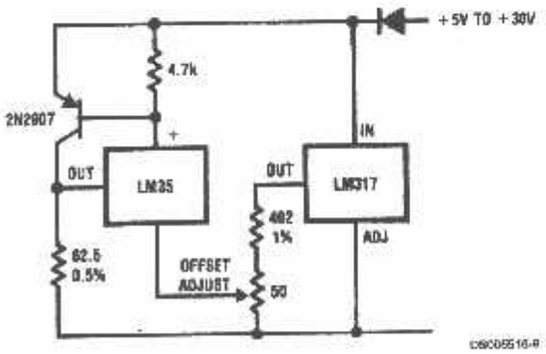


FIGURE 9. 4-To-20 mA Current Source (0°C to +100°C)

Typical Applications (Continued)

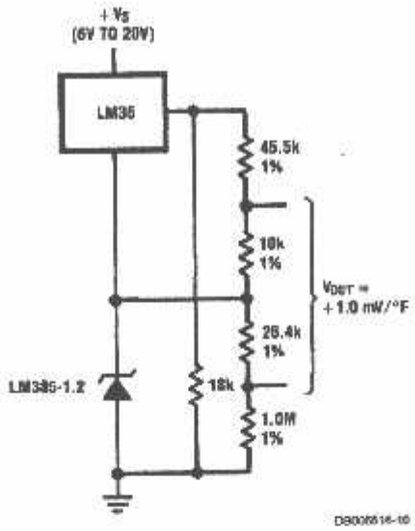


FIGURE 10. Fahrenheit Thermometer

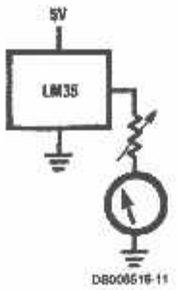


FIGURE 11. Centigrade Thermometer (Analog Meter)

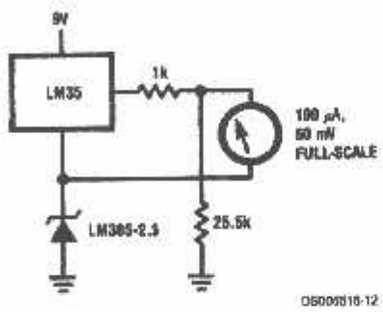


FIGURE 12. Fahrenheit ThermometerExpanded Scale Thermometer
(50° to 80° Fahrenheit, for Example Shown)

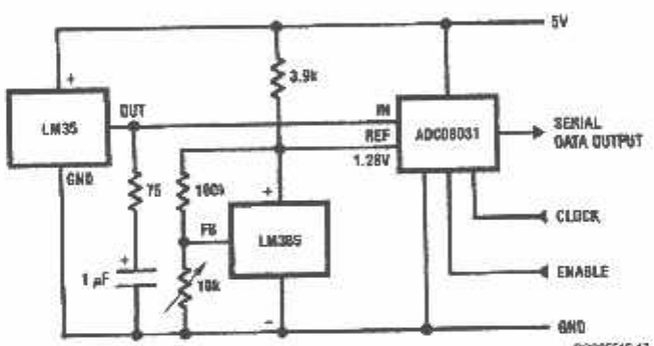


FIGURE 13. Temperature To Digital Converter (Serial Output) (+128°C Full Scale)

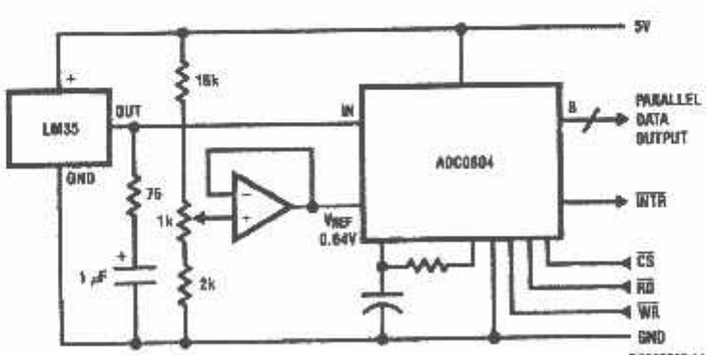
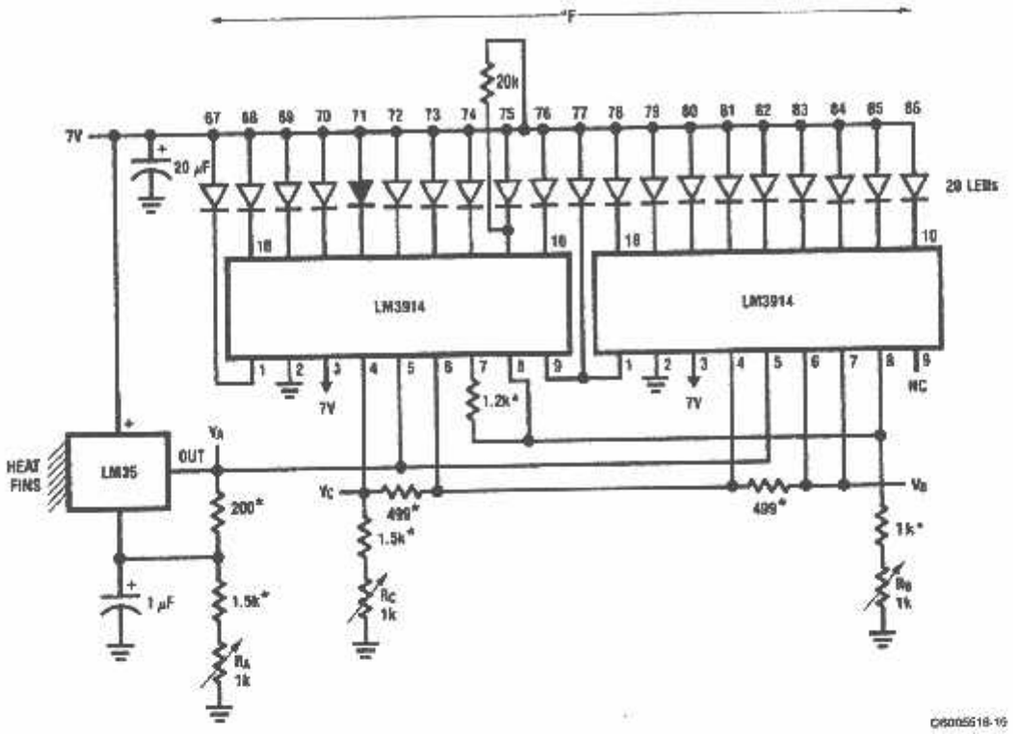


FIGURE 14. Temperature To Digital Converter (Parallel TRI-STATE™ Outputs for Standard Data Bus to µP Interface) (128°C Full Scale)

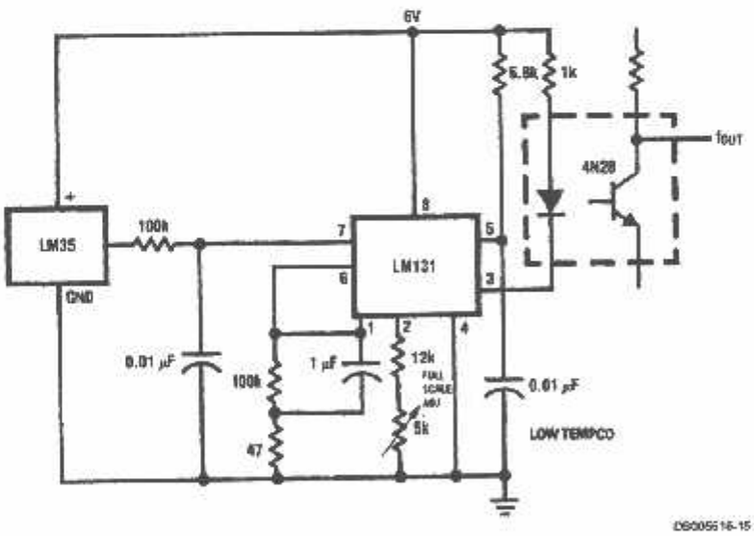
pical Applications (Continued)



DS005516-16

% or 2% film resistor
1. R_B for V_B=3.075V
2. R_C for V_C=1.955V
3. R_A for V_A=0.075V + 10mV/°C x $T_{ambient}$
ample, V_A=2.275V at 22°C

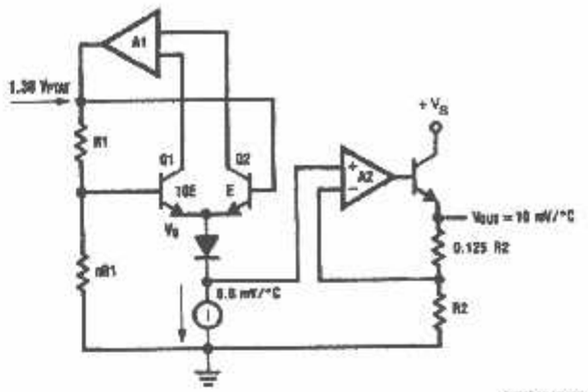
FIGURE 15. Bar-Graph Temperature Display (Dot Mode)



DS005516-15

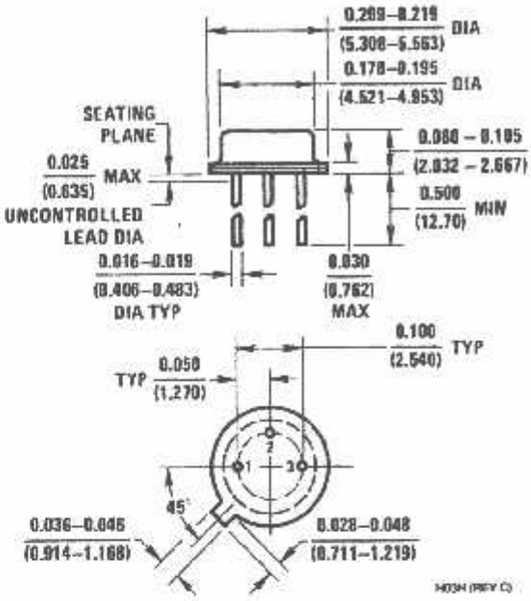
FIGURE 16. LM35 With Voltage-To-Frequency Converter And Isolated Output (2°C to +150°C; 20 Hz to 1500 Hz)

Block Diagram

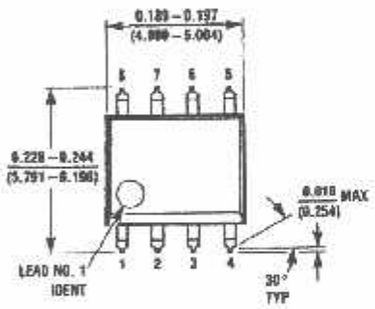


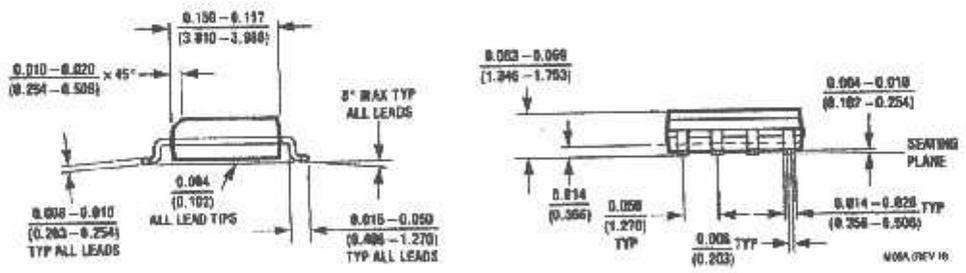
DS005516-23

/sical Dimensions inches (millimeters) unless otherwise noted



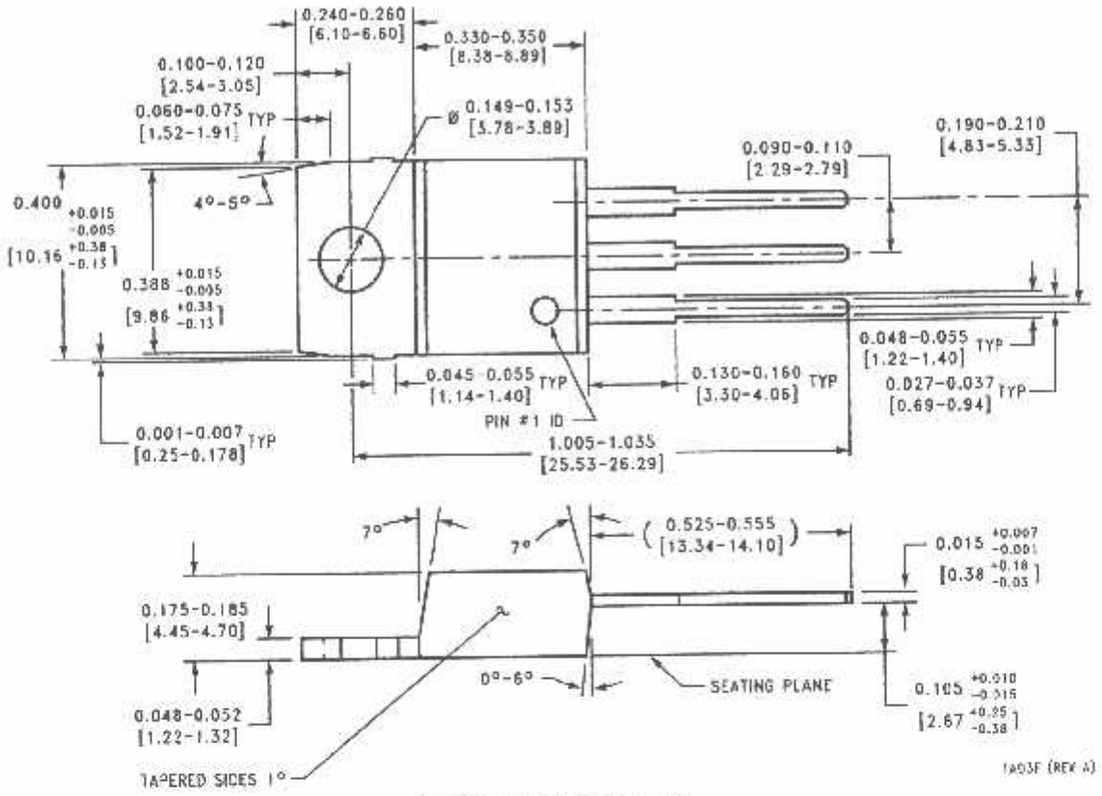
TO-46 Metal Can Package (H)
Order Number LM35H, LM35AH, LM35CH, LM35CAH, or LM35DH
NS Package Number H03H





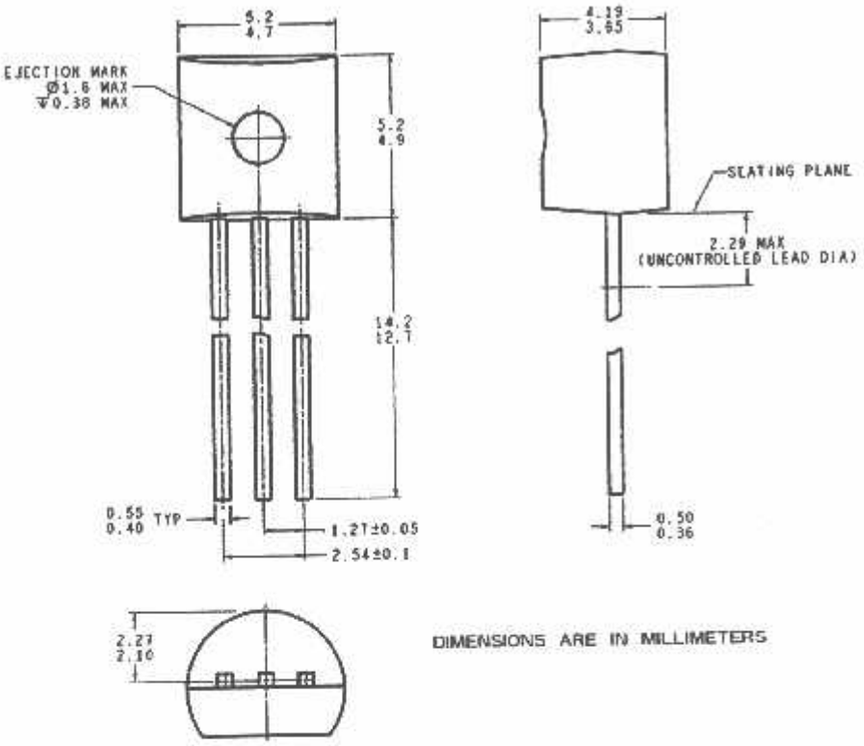
SO-8 Molded Small Outline Package (M)
Order Number LM35DM
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Power Package TO-220 (T)
Order Number LM35DT
NS Package Number TA03F

/sical Dimensions inches (millimeters) unless otherwise noted (Continued)



TO-92 Plastic Package (Z)
Order Number LM35CZ, LM35CAZ or LM35DZ
NS Package Number Z03A

E SUPPORT POLICY

TIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT VICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL UNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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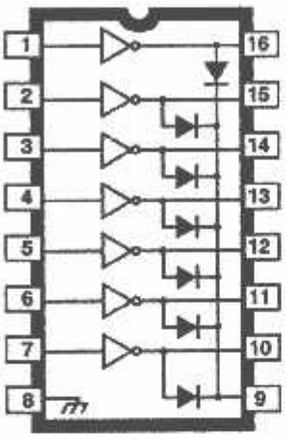
2003 THRU 2024

Data Sheet 29304F

HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS



Dwg. No. A-9594

that the ULN20xxA series (dual in-line age) and ULN20xxL series (small-outline ckage) are electrically identical and share mmon terminal number assignment.

OLUTE MAXIMUM RATINGS

at Voltage, V_{CE}
LN200xA and ULN200xL) ..... **50 V**
LN202xA and ULN202xL) ..... **95 V**
Voltage, V_{IN} ..... **30 V**
nuous Output Current,
..... **500 mA**
nuous Input Current, I_{IN} ..... **25 mA**
r Dissipation, P_D
ic Darlington pair)..... **1.0 W**
tal package)..... **See Graph**
ating Temperature Range,
..... **-20°C to +85°C**
ge Temperature Range,
..... **-55°C to +150°C**

Ideally suited for interfacing between low-level logic circuitry and multiple peripheral power loads, the Series ULN20xxA/L high-voltage, high-current Darlington arrays feature continuous load current ratings to 500 mA for each of the seven drivers. At an appropriate duty cycle depending on ambient temperature and number of drivers turned ON simultaneously, typical power loads totaling over 230 W (350 mA x 7, 95 V) can be controlled. Typical loads include relays, solenoids, stepping motors, magnetic print hammers, multiplexed LED and incandescent displays, and heaters. All devices feature open-collector outputs with integral clamp diodes.

The ULN2003A/L and ULN2023A/L have series input resistors selected for operation directly with 5 V TTL or CMOS. These devices will handle numerous interface needs — particularly those beyond the capabilities of standard logic buffers.

The ULN2004A/L and ULN2024A/L have series input resistors for operation directly from 6 to 15 V CMOS or PMOS logic outputs.

The ULN2003A/L and ULN2004A/L are the standard Darlington arrays. The outputs are capable of sinking 500 mA and will withstand at least 50 V in the OFF state. Outputs may be paralleled for higher load current capability. The ULN2023A/L and ULN2024A/L will withstand 95 V in the OFF state.

These Darlington arrays are furnished in 16-pin dual in-line plastic packages (suffix "A") and 16-lead surface-mountable SOICs (suffix "L"). All devices are pinned with outputs opposite inputs to facilitate ease of circuit board layout. All devices are rated for operation over the temperature range of -20°C to +85°C. Most (see matrix, next page) are also available for operation to -40°C; to order, change the prefix from "ULN" to "ULQ".

FEATURES

- TTL, DTL, PMOS, or CMOS-Compatible Inputs
- Output Current to 500 mA
- Output Voltage to 95 V
- Transient-Protected Outputs
- Dual In-Line Plastic Package or Small-Outline IC Package

x = digit to identify specific device. Characteristic shown applies to family of devices with remaining digits as shown. See matrix on next page.

3 THRU 2024
iH-VOLTAGE,
iH-CURRENT
RLINGTON ARRAYS

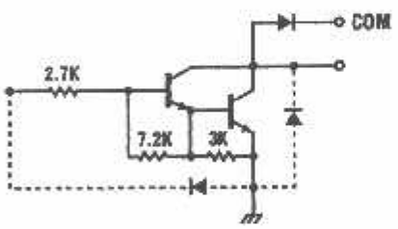
DEVICE PART NUMBER DESIGNATION

$V_{CE(MAX)}$	50 V	95 V
$I_{C(MAX)}$	500 mA	500 mA
Logic	**Part Number**	
5V TTL, CMOS	ULN2003A* ULN2003L*	ULN2023A* ULN2023L
6-15 V CMOS, PMOS	ULN2004A* ULN2004L*	ULN2024A ULN2024L

*Also available for operation between -40°C and +85°C. To order, change prefix from "ULN" to "ULQ".

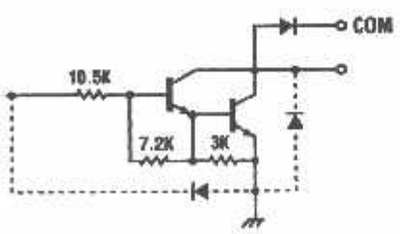
PARTIAL SCHEMATICS

20x3A/L (Each Driver)

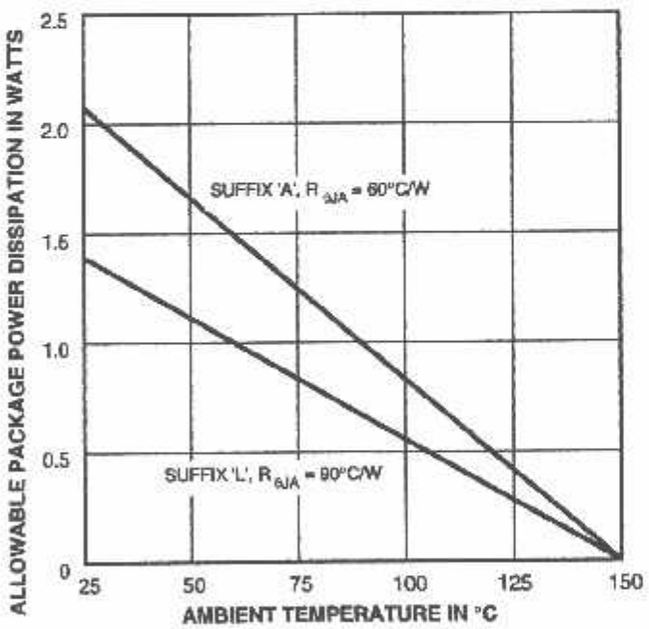


Dwg. No. A-9651

120x4A/L (Each Driver)



Dwg. No. A-9698A



Dwg. GP-006A

X = Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown. See matrix above.

Allegro MicroSystems, Inc.

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s ULN2003A, ULN2003L, ULN2004A, and ULN2004L
:TRICAL CHARACTERISTICS at +25°C (unless otherwise noted).

acteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			Units
					Min.	Typ.	Max.	
t Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	< 1	50	µA
				V_{CE} = 50 V, T_A = 70°C	—	< 1	100	µA
		1B	ULN2004A/L	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	< 5	500	µA
tor-Emitter ation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 µA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 µA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 µA	—	1.3	1.6	V
Current	$I_{IN(ON)}$	3	ULN2003A/L	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN2004A/L	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 µA, T_A = 70°C	50	65	—	µA
Voltage	$V_{IN(ON)}$	5	ULN2003A/L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN2004A/L	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
Capacitance	C_{IN}	—	All		—	15	25	pF
On Delay	t_{PLH}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Off Delay	t_{PHL}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Diode ge Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	µA
				V_R = 50 V, T_A = 70°C	—	—	100	µA
Diode rd Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

ete part number includes suffix to identify package style: A = DIP, L = SOIC.

ULN2023A, ULN2023L, ULN2024A, and ULN2024L
TRICAL CHARACTERISTICS at +25°C (unless otherwise noted).

teristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Leakage Current	I_{CEX}	1A	All	V_{CE} = 95 V, T_A = 25°C	—	< 1	50	µA
				V_{CE} = 95 V, T_A = 70°C	—	< 1	100	µA
		1B	ULN2024A/L	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 1.0 V	—	< 5	500	µA
r-Emitter ion Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 µA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 µA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 µA	—	1.3	1.6	V
urrent	$I_{IN(ON)}$	3	ULN2023A/L	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN2024A/L	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 µA, T_A = 70°C	50	65	—	µA
oltage	$V_{IN(ON)}$	5	ULN2023A/L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN2024A/L	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
apacitance	C_{IN}	—	All		—	15	25	pF
n Delay	t_{PLH}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
ff Delay	t_{PHL}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Diode e Current	I_R	6	All	V_R = 95 V, T_A = 25°C	—	—	50	µA
				V_R = 95 V, T_A = 70°C	—	—	100	µA
Diode d Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

ete part number includes suffix to identify package style: A = DIP, L = SOIC.

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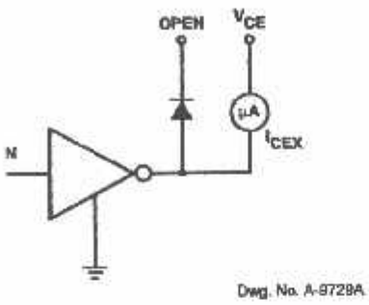
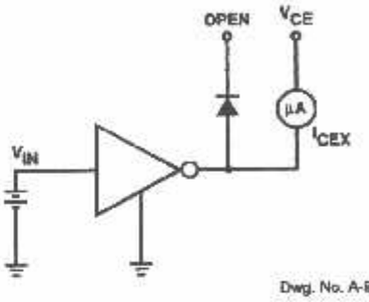
TEST FIGURES

FIGURE 1A



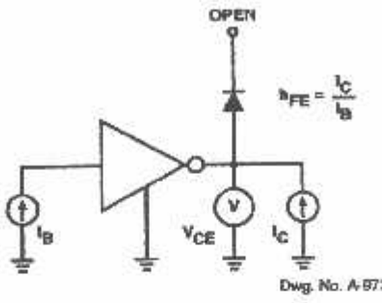
Dwg. No. A-9729A

FIGURE 1B



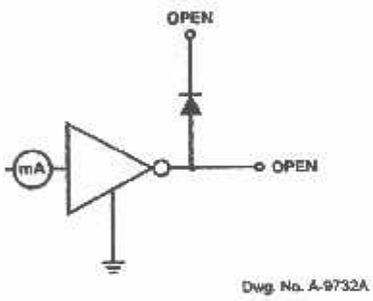
Dwg. No. A-9730A

FIGURE 2



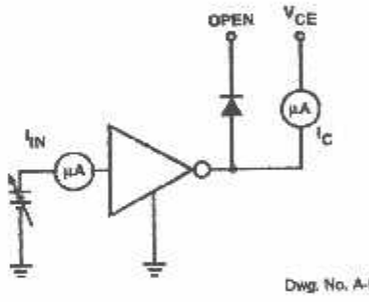
Dwg. No. A-9731A

FIGURE 3



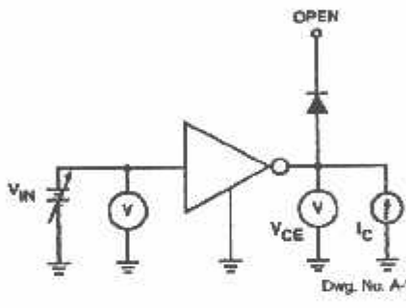
Dwg. No. A-9732A

FIGURE 4



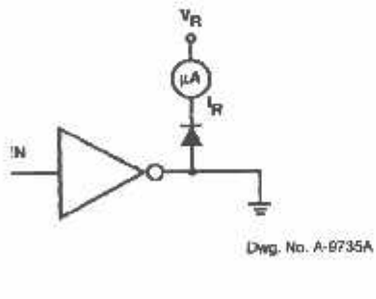
Dwg. No. A-9733A

FIGURE 5



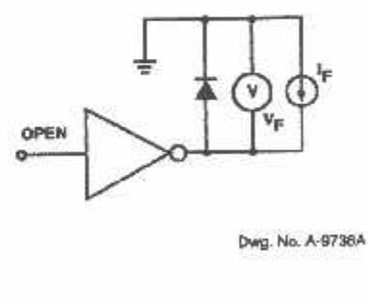
Dwg. No. A-9734A

FIGURE 6



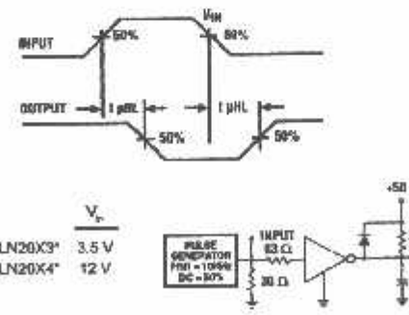
Dwg. No. A-9735A

FIGURE 7



Dwg. No. A-9736A

FIGURE 8



	V_{in}
ULN20X3*	3.5 V
ULN20X4*	12 V

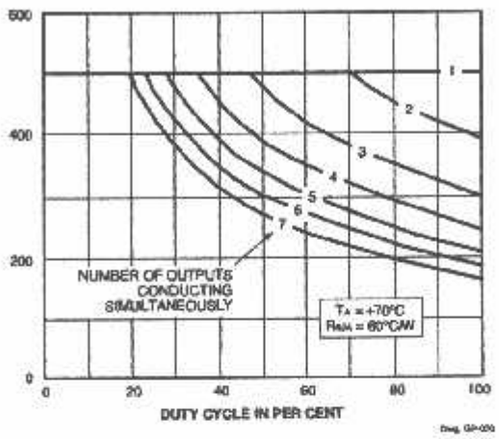
plete part number includes a final letter to indicate package.

git to identify specific device. Specification shown applies to family of devices with remaining digits as shown.

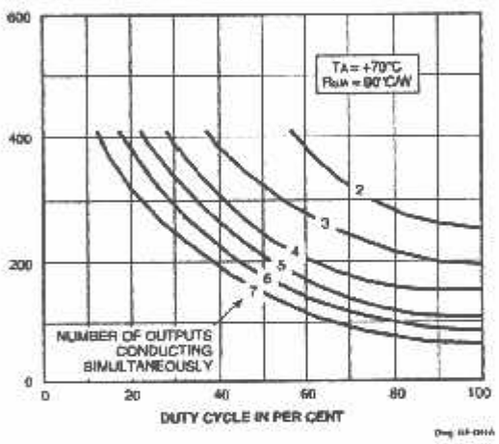
3 THRU 2024
;H-VOLTAGE,
;H-CURRENT
RLINGTON ARRAYS

LOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

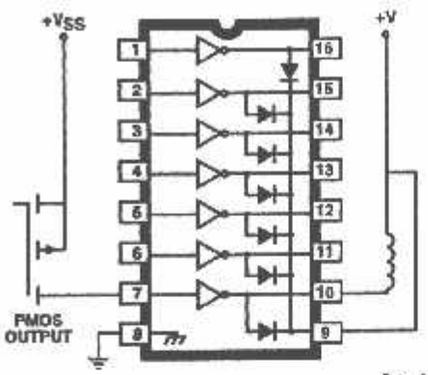
Dual In-line-Packaged Devices, Suffix 'A')



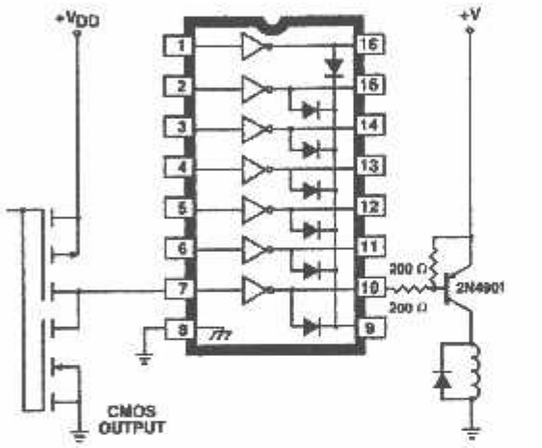
Small-Outline-Packaged Devices, Suffix 'L')



TYPICAL APPLICATIONS

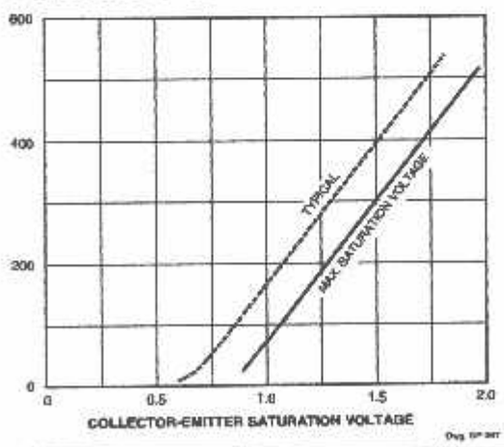


Dwg. No. A-9652

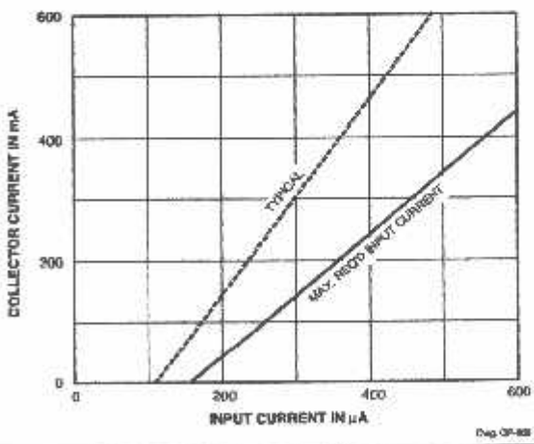


Dwg. No. A-9654A

SATURATION VOLTAGE FUNCTION OF COLLECTOR CURRENT



COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



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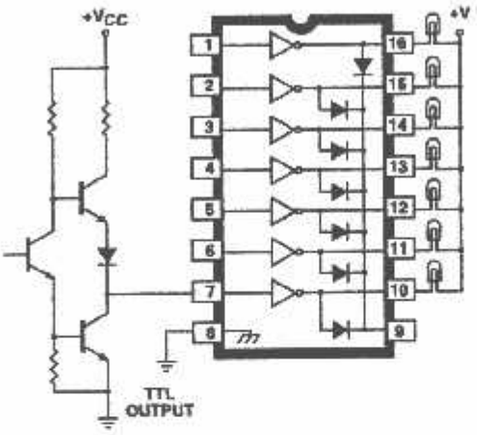
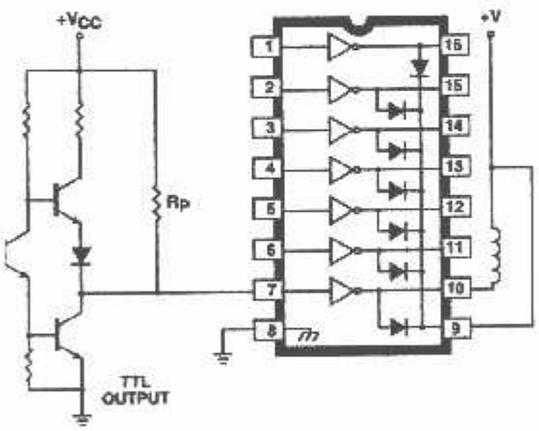
TYPICAL APPLICATIONS



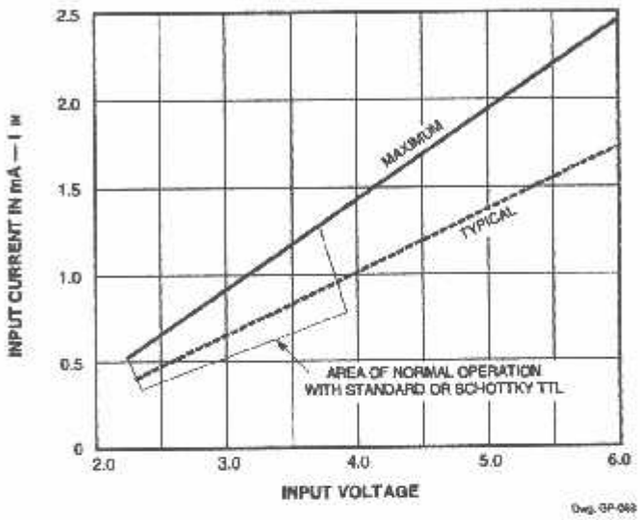
Dwg. No. A-9653A



Dwg. No. A-10,175

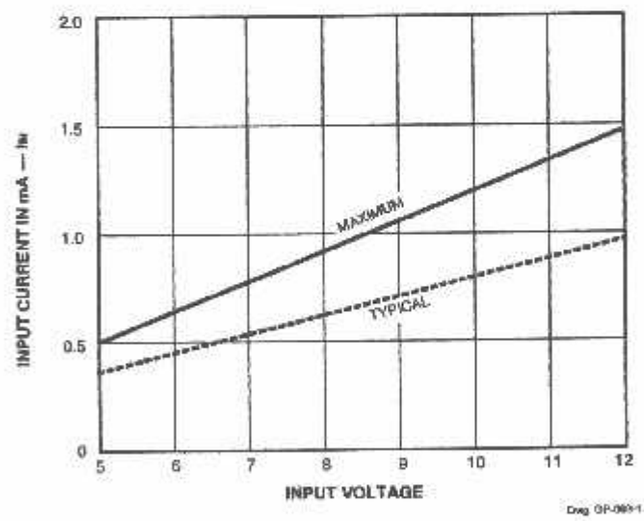
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

Types ULN2003A, ULN2003L, ULN2023A, and ULN2023L



Dwg. GP-068

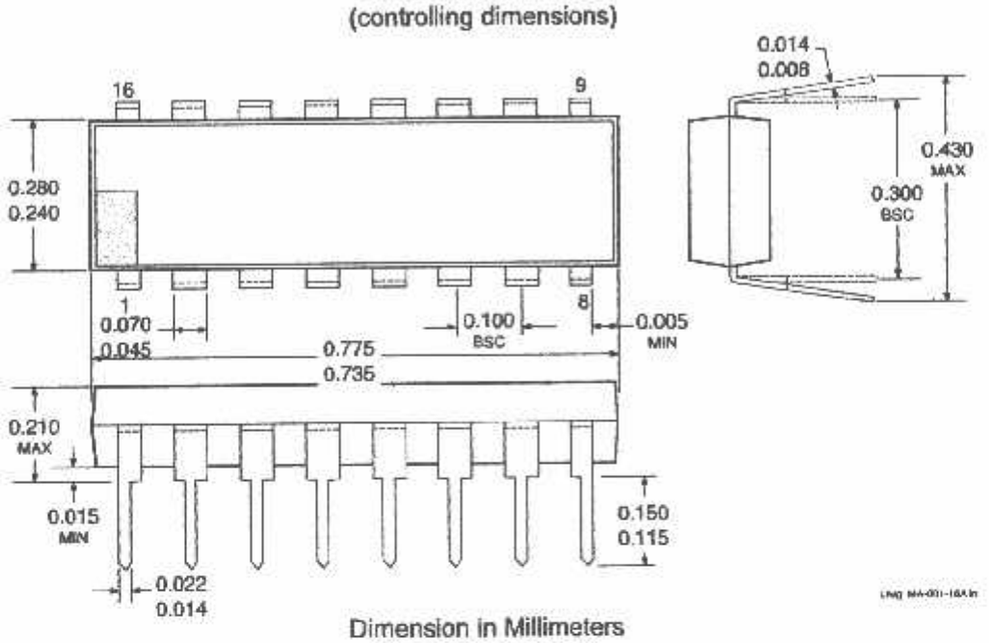
Types ULN2004A, ULN2004L, ULN2024A, and ULN2024L



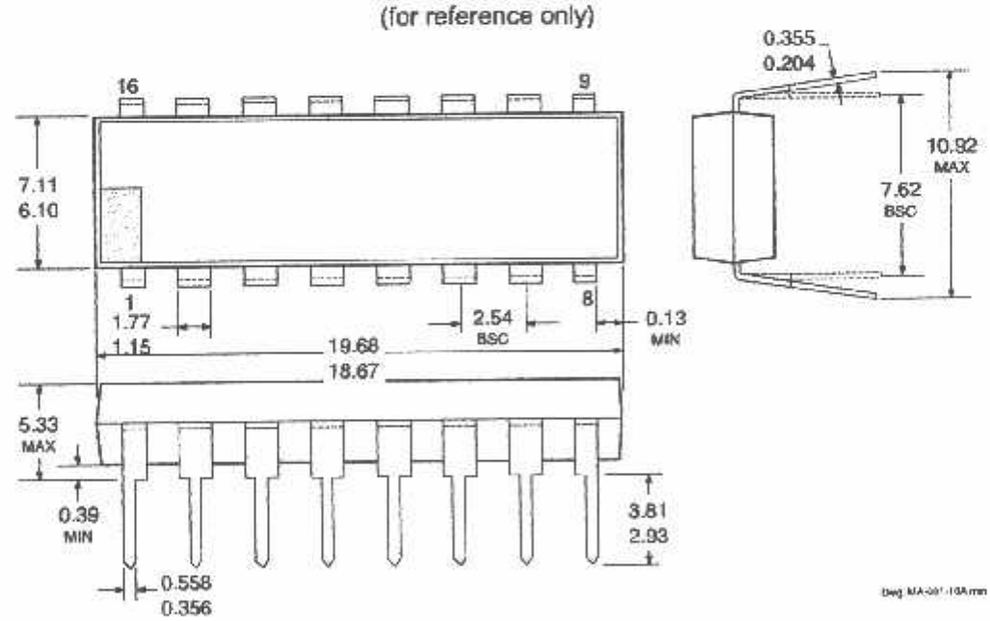
Dwg. GP-069-1

PACKAGE DESIGNATOR "A"

Dimensions in Inches
(controlling dimensions)



Dimension in Millimeters
(for reference only)



1. Leads 1, 8, 9, and 16 may be half leads at vendor's option.
2. Lead thickness is measured at seating plane or below.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown.

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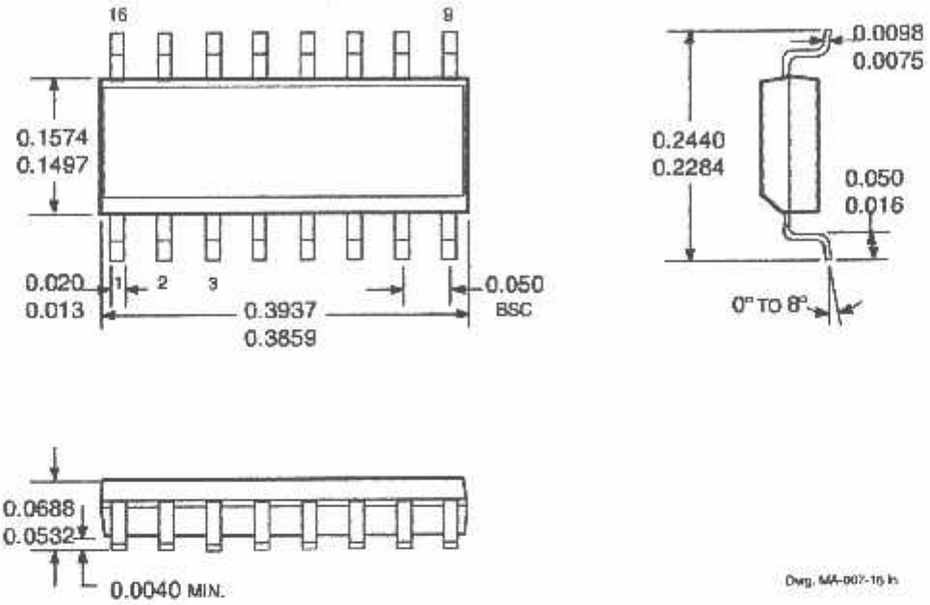
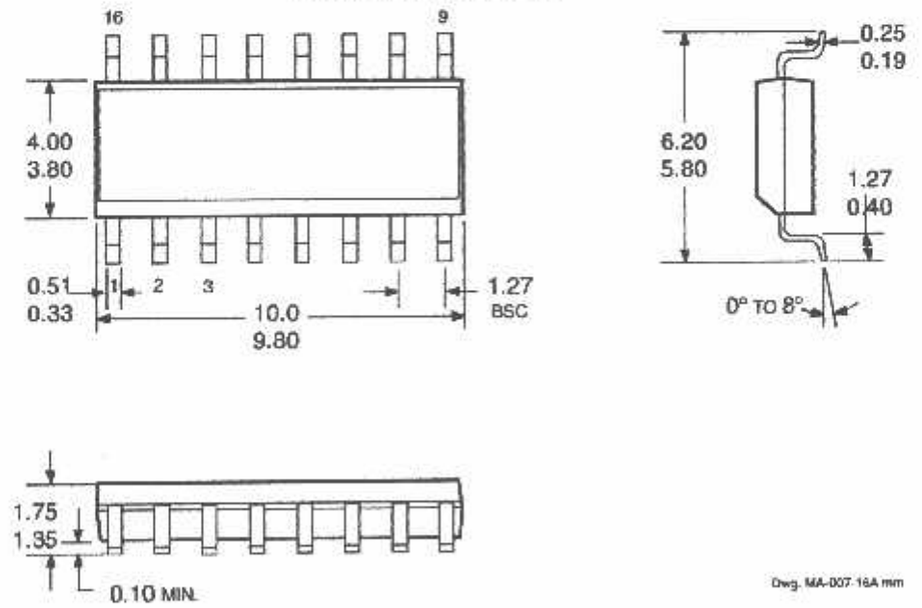
PACKAGE DESIGNATOR "L"

Dimensions in Inches
(for reference only)



Dwg. MA-007-16 In

Dimension in Millimeters
(controlling dimensions)



Dwg. MA-007-16A mm

S: 1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.

THRU 2024
H-VOLTAGE,
H-CURRENT
RLINGTON ARRAYS

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atures

VR® - High Performance and Low Power RISC Architecture
- 118 Powerful Instructions - Most Single Clock Cycle Execution
- 32 x 8 General Purpose Working Registers
- Up to 8 MIPS Throughput at 8 MHz

on-Volatile Program and Data Memories
- 8K bytes of In-System Programmable Flash AT90S/LS8535
- 4K bytes of In-System Programmable Flash AT90S/LS4434
  SPI Serial Interface for In-System Programming
  Endurance: 1,000 Write/Erase Cycles
- 512 bytes EEPROM AT90S/LS8535
- 256 bytes EEPROM AT90S/LS4434
  Endurance: 100,000 Write/Erase Cycles
- 512 bytes Internal SRAM AT90S/LS8535
- 256 bytes Internal SRAM AT90S/LS4434
- Programming Lock for Software Security

eripheral Features
- 8-Channel, 10-Bit ADC
- Programmable Serial UART
- Two 8-Bit Timer/Counters with Separate Prescaler and Compare Mode
- One 16-Bit Timer/Counter with Separate Prescaler and Compare and Capture Modes
- Programmable Watchdog Timer with On-Chip Oscillator
- On-Chip Analog Comparator
- 3 PWM channels

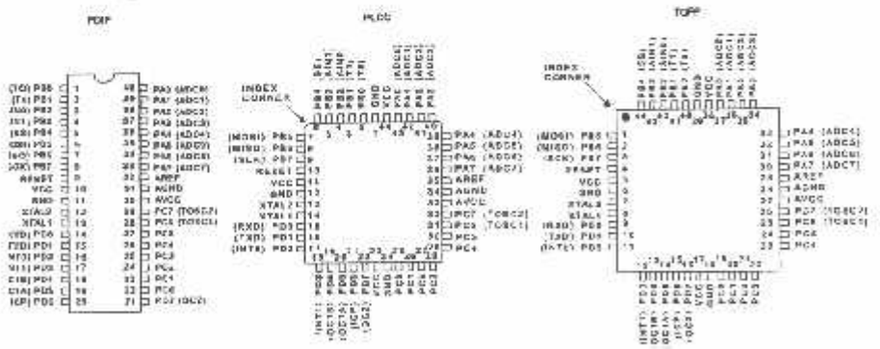
pecial Microcontroller Features
- Power-On Reset Circuit
- RTC with Separate Oscillator and Counter Mode
- External and Internal Interrupt Sources
- Three Sleep Modes: Idle, Power Save, and Power Down

O and Packages
- 32 Programmable I/O Lines

perating Voltages
- V_{CC}: 4.0 - 6.0V AT90S4434/AT90S8535
- V_{CC}: 2.7 - 6.0V AT90LS4434/AT90LS8535

peed Grades:
- 0 - 8 MHz AT90S4434/AT90S8535
- 0 - 4 MHz (AT90LS4434/AT90LS8535

n Configurations



8-Bit AVR® Microcontroller with 4K/8K Bytes In-System Programmable Flash

AT90S4434
AT90LS4434
AT90S8535
AT90LS8535

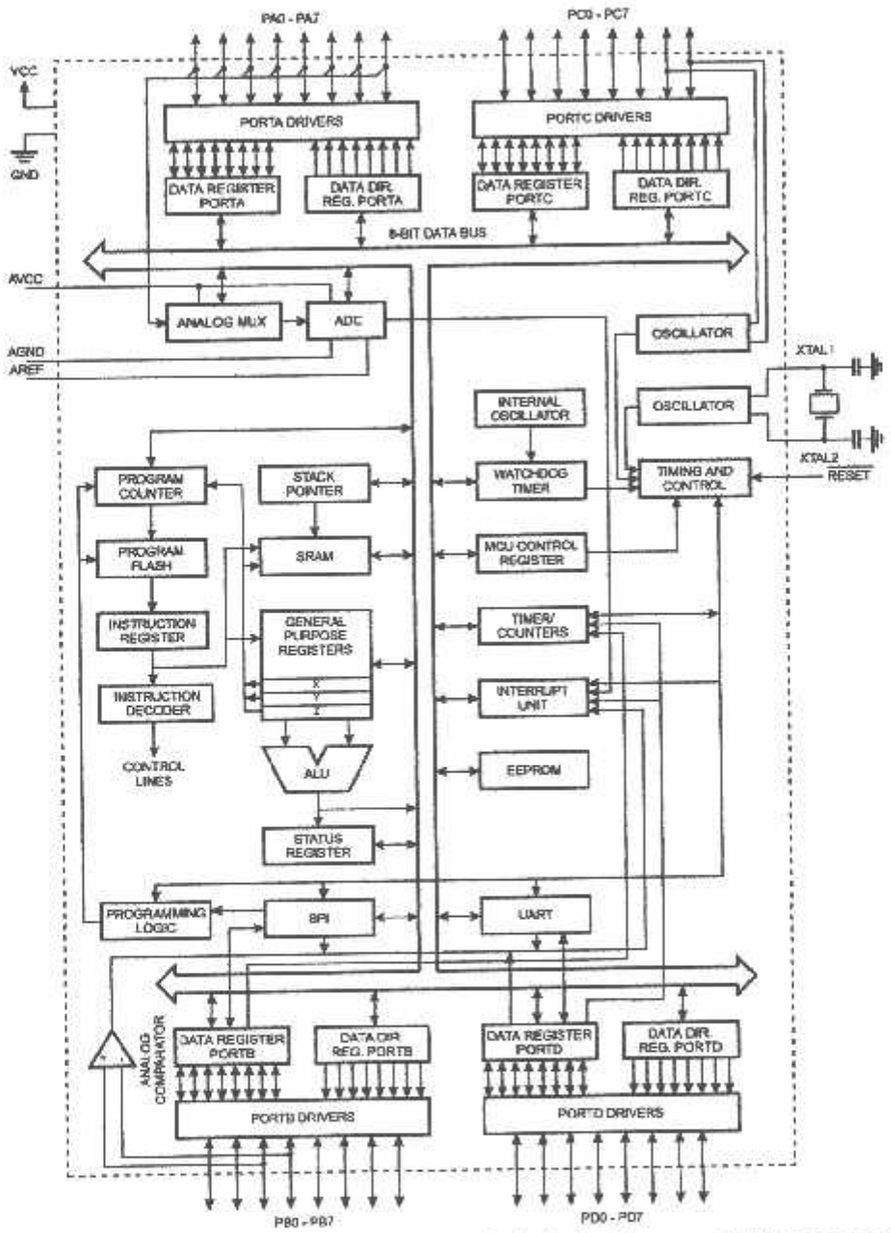
Advance Information

Rev. 1041C–11/98

scription

AT90S4434/8535 is a low-power CMOS 8-bit micro-troller based on the AVR enhanced RISC architecture. executing powerful instructions in a single clock cycle, the AT90S4434/8535 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

ock Diagram



e AVR core combines a rich instruction set with 32 gen-al purpose working registers. All the 32 registers are ectly connected to the Arithmetic Logic Unit (ALU), owing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving through-puts up to ten times faster than conventional CISC micro-controllers.

e AT90S4434/8535 provides the following features: /8K bytes of In-System Programmable Flash, 256/512 es EEPROM, 256/512 bytes SRAM, 32 general purpose lines, 32 general purpose working registers, RTC, three ible timer/counters with compare modes, internal and ernal interrupts, a programmable serial UART, 8-chan-, 10-bit ADC, programmable Watchdog Timer with inter- oscillator, an SPI serial port and three software ectable power saving modes. The Idle mode stops the U while allowing the SRAM, timer/counters, SPI port d interrupt system to continue functioning. The Power wn mode saves the register contents but freezes the illator, disabling all other chip functions until the next errupt or hardware reset. In Power Save mode, the timer illator continues to run, allowing the user to maintain a er base while the rest of the device is sleeping.

e device is manufactured using Atmel's high density n-volatile memory technology. The on-chip ISP Flash ows the program memory to be reprogrammed in-system ough an SPI serial interface or by a conventional nonvol- le memory programmer. By combining an 8-bit RISC PU with In-System Programmable Flash on a monolithic ip, the Atmel AT90S4434/8535 is a powerful microcon- ller that provides a highly flexible and cost effective solu- n to many embedded control applications.

e AT90S4434/8535 AVR is supported with a full suite of ogram and system development tools including: C com- ers, macro assemblers, program debugger/simulators, circuit emulators, and evaluation kits.

mparison between AT90S4434 and AT90S8535

e AT90S4434 has 4K bytes of In-System Programmable ish, 256 bytes of EEPROM, and 256 bytes of internal AM.

e AT90S8535 has 8K bytes of In-System Programmable ish, 512 bytes of EEPROM, and 512 bytes of internal AM.

ble 1 summarizes the different memory sizes for the two vices.

ble 1. Memory Size Summary

art	Flash	EEPROM	SRAM
T90S4434	4K bytes	256 bytes	256 bytes
T90S8535	8K bytes	512 bytes	512 bytes

n Descriptions

C

gital supply voltage

ID

gital ground

Port A (PA7..PA0)

Port A is an 8-bit bi-directional I/O port. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers can sink 20mA and can drive LED displays directly. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

Port A also serves as the analog inputs to the A/D Converter.

Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O pins with internal pull-up resistors. The Port B output buffers can sink 20 mA. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated.

Port B also serves the functions of various special features of the AT90S4434/8535 as listed on page 53.

Port C (PC7..PC0)

Port C is an 8-bit bi-directional I/O port with internal pullup resistors. The Port C output buffers can sink 20 mA. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. Two Port C pins can alternatively be used as oscillator for Timer/Counter2.

Port D (PD7..PD0)

Port D is an 8-bit bidirectional I/O port with internal pull-up resistors. The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated.

Port D also serves the functions of various special features of the AT90S4434/8535 as listed on page 60.

$\overline{\text{RESET}}$

Reset input. A low on this pin for two machine cycles while the oscillator is running resets the device.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier

AVCC

This is the supply voltage pin for the A/D Converter. It should be externally connected to V_{CC} via a low-pass filter. See page 48 for details on operation of the ADC.

AREF

This is the analog reference input for the A/D Converter. For ADC operations, a voltage in the range AGND to AV_{CC} must be applied to this pin.

AGND

Analog ground. If the board has a separate analog ground plane, this pin should be connected to this ground plane. Otherwise, connect to GND.

rstal Oscillators

.L1 and XTAL2 are input and output, respectively, of an erting amplifier which can be configured for use as an chip oscillator, as shown in Figure 1. Either a quartz tal or a ceramic resonator may be used. To drive the ice from an external clock source, XTAL2 should be left onnected while XTAL1 is driven as shown in Figure 2. the Timer Oscillator pins, PC6(OSC1) and PC7(OSC2), crystal is connected directly between the pins. No rnal capacitors are needed. The oscillator is optimized use with a 32,768 Hz watch crystal. An external clock al applied to this pin goes through the same amplifier ing a bandwidth of 256 kHz. The external clock signal uld therefore be in the interval 0 Hz - 256 kHz.

ure 1. Oscillator Connections

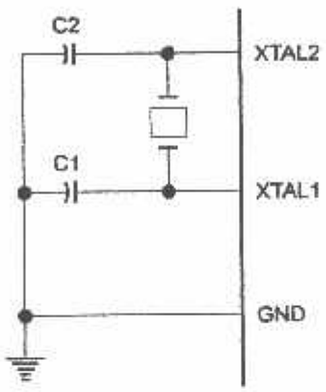
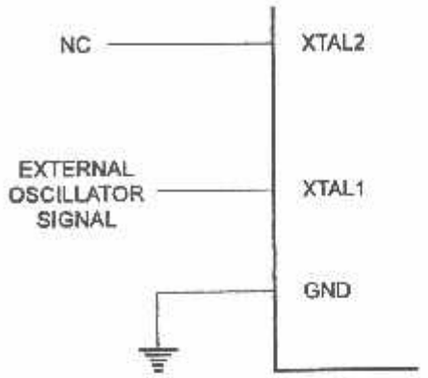


Figure 2. External Clock Drive Configuration

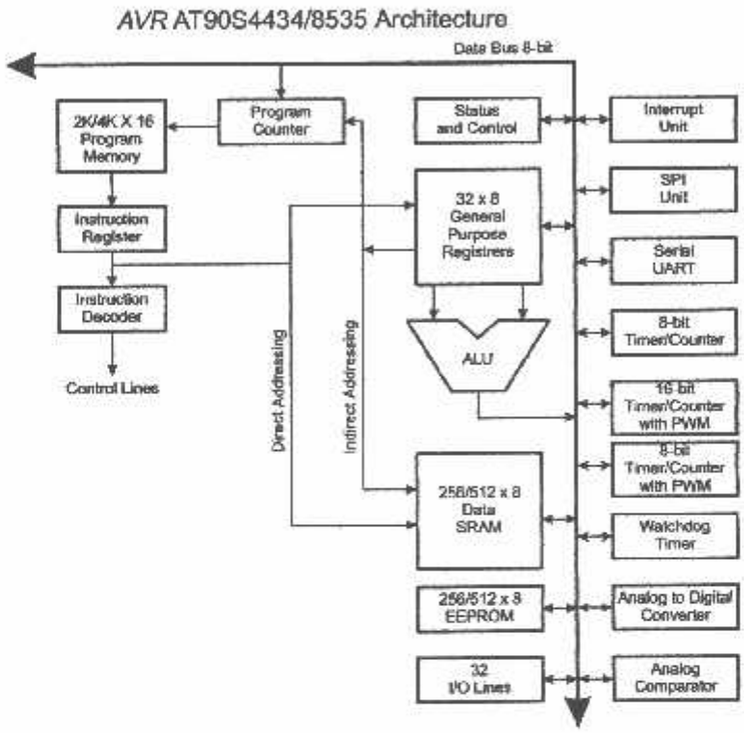


chitectural Overview

e fast-access register file concept contains 32 x 8-bit ieral purpose working registers with a single clock cycle ess time. This means that during one single clock cycle, e Arithmetic Logic Unit (ALU) operation is executed. Two rands are output from the register file, the operation is cuted, and the result is stored back in the register file - ne clock cycle.

Six of the 32 registers can be used as three 16-bits indirect address register pointers for Data Space addressing - enabling efficient address calculations. One of the three address pointers is also used as the address pointer for the constant table look up function. These added function registers are the 16-bits X-register, Y-register and Z-register.

ure 3. The AT90S4434/8535 *AVR* Enhanced RISC Architecture



e ALU supports arithmetic and logic functions between isters or between a constant and a register. Single reg- r operations are also executed in the ALU. Figure 3 ws the AT90S4434/8535 AVR Enhanced RISC micro- troller architecture.

ddition to the register operation, the conventional mem- addressing modes can be used on the register file as ll. This is enabled by the fact that the register file is signed the 32 lowermost Data Space addresses ($00 - F), allowing them to be accessed as though they were inary memory locations.

e I/O memory space contains 64 addresses for CPU ipheral functions as Control Registers, Timer/Counters,)-converters, and other I/O functions. The I/O Memory n be accessed directly, or as the Data Space locations owing those of the register file, $20 - $5F.

The AVR uses a Harvard architecture concept - with separate memories and buses for program and data. The program memory is executed with a two stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system downloadable Flash memory.

With the relative jump and call instructions, the whole 2K/4K address space is directly accessed. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

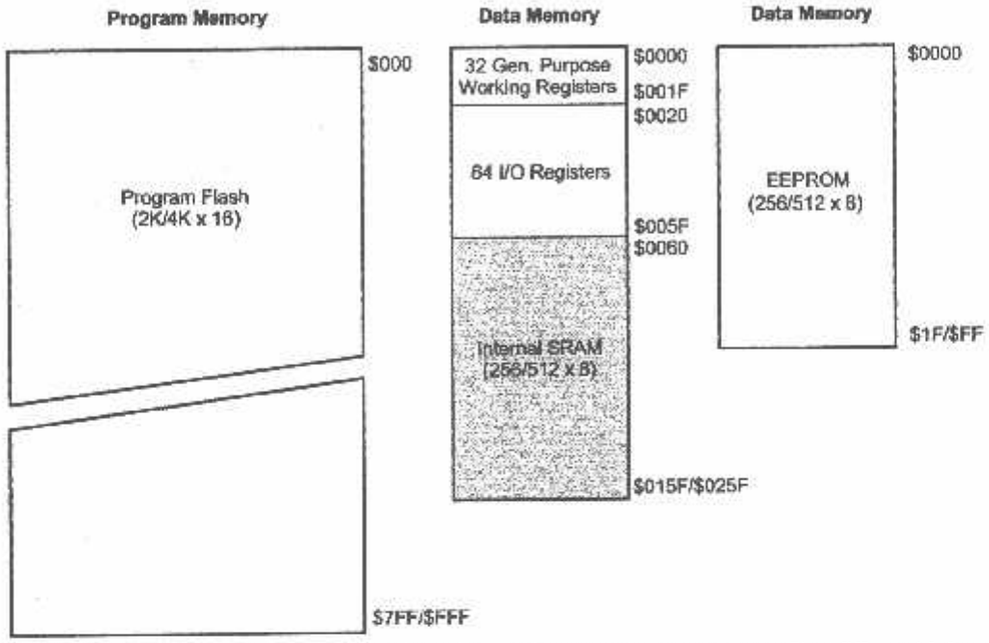
During interrupts and subroutine calls, the return address program counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initial-

the SP in the reset routine (before subroutines or interts are executed). The 9-bit stack pointer SP is read/write essible in the I/O space.

The 256/512 bytes data SRAM can be easily accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

ure 4. Memory Maps

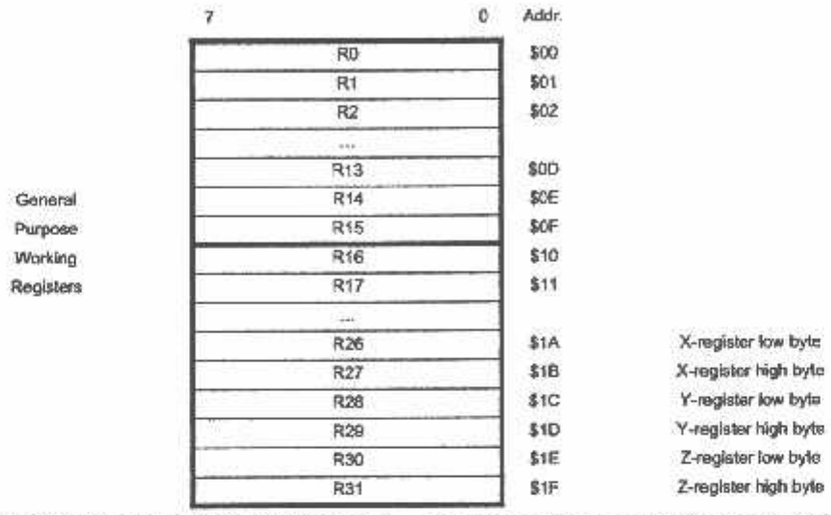


xible interrupt module has its control registers in the I/O ace with an additional global interrupt enable bit in the tus register. All the different interrupts have a separate errupt vector in the interrupt vector table at the beginning of the program memory. The different interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

e General Purpose Register File

ure 5 shows the structure of the 32 general purpose working registers in the CPU.

ıure 5. AVR CPU General Purpose Working Registers



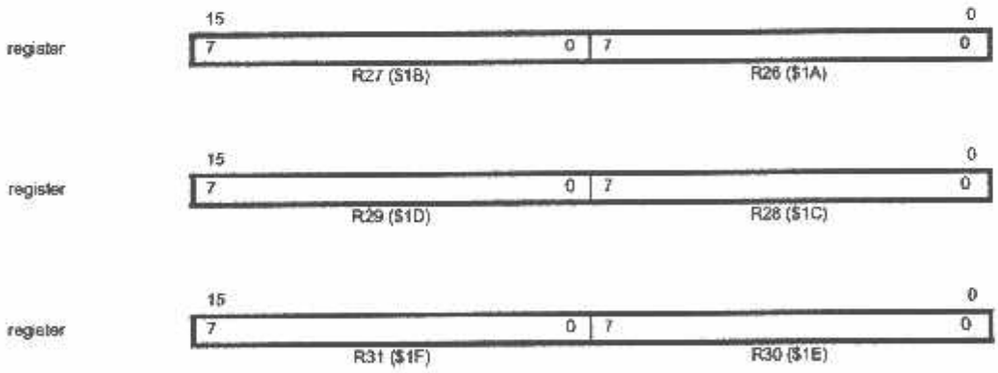
the register operating instructions in the instruction set ve direct and single cycle access to all registers. The ly exception is the five constant arithmetic and logic ıstructions SBCI, SUBI, CPI, ANDI and ORI between a nstant and a register and the LDI instruction for load mediate constant data. These instructions apply to the ɔond half of the registers in the register file - R16..R31. e general SBC, SUB, CP, AND and OR and all other ɛrations between two registers or on a single register ɔly to the entire register file.

shown in Figure 5, each register is also assigned a data mory address, mapping them directly into the first 32 locations of the user Data Space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X, Y and Z registers can be set to index any register in the file.

The X-register, Y-register And Z-register

The registers R26..R31 have some added functions to their general purpose usage. These registers are address pointers for indirect addressing of the Data Space. The three indirect address registers X, Y and Z are defined as:

ıure 6. The X, Y and Z Registers



he different addressing modes these address registers ɛ functions as fixed displacement, automatic increment and decrement (see the descriptions for the different instructions).

e ALU - Arithmetic Logic Unit

: high-performance AVR ALU operates in direct connec- : with all the 32 general purpose working registers. hin a single clock cycle, ALU operations between regis- ; in the register file are executed. The ALU operations divided into three main categories - arithmetic, logical, l bit-functions.

e In-System Programmable Flash Program :mory

: AT90S4434/8535 contains 4K/8K bytes on-chip In- :tem Programmable Flash memory for program storage. ce all instructions are 16-or 32-bit words, the Flash is anized as 2K/4K x 16. The Flash memory has an endur- ce of at least 1000 write/erase cycles. The AT90S4434/8535 Program Counter (PC) is 11/12 bits wide, thus addressing the 2048/4096 program memory addresses.

See page 71 for a detailed description on Flash data downloading.

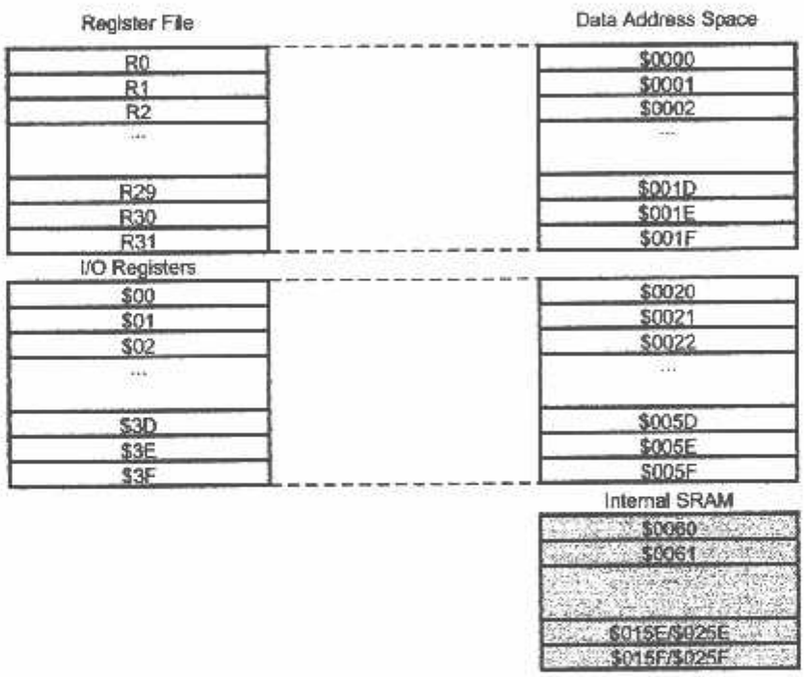
Constant tables must be allocated within the address 0-2K/4K(see the LPM - Load Program Memory instruction description).

See page 9 for the different program memory addressing modes.

The SRAM Data Memory

The following figure shows how the AT90S4434/8535 SRAM Memory is organized:

ure 7. SRAM Organization



: lower 352/608 Data Memory locations address the gister file, the I/O Memory, and the internal data SRAM. : first 96 locations address the Register File + I/O Mem- , and the next 256/512 locations address the internal a SRAM.

: five different addressing modes for the data memory /er: Direct, Indirect with Displacement, Indirect, Indirect h Pre-Decrement and Indirect with Post-Increment. In register file, registers R26 to R31 feature the indirect dressing pointer registers.

: direct addressing reaches the entire data space.

The Indirect with Displacement mode features a 63 address locations reach from the base address given by the Y or Z-register.

When using register indirect addressing modes with automatic pre-decrement and post-increment, the address registers X, Y and Z are decremented and incremented.

The 32 general purpose working registers, 64 I/O registers and the 256/512 bytes of internal data SRAM in the AT90S4434/8535 are all accessible through all these addressing modes.

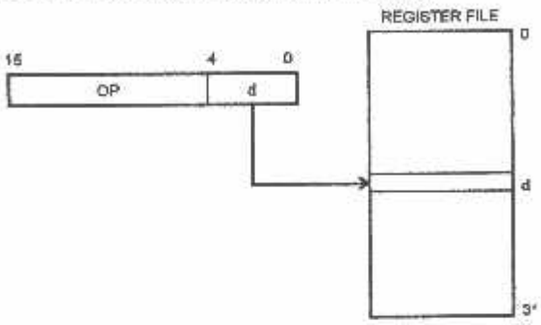
See the next section for a detailed description of the different addressing modes.

e Program and Data Addressing Modes

AT90S4434/8535 AVR Enhanced RISC microcontrol- supports powerful and efficient addressing modes for ess to the program memory (Flash) and data memory AM, Register File and I/O Memory). This section cribes the different addressing modes supported by the R architecture. In the figures, OP means the operation e part of the instruction word. To simplify, not all figures w the exact location of the addressing bits.

ister Direct, Single Register Rd

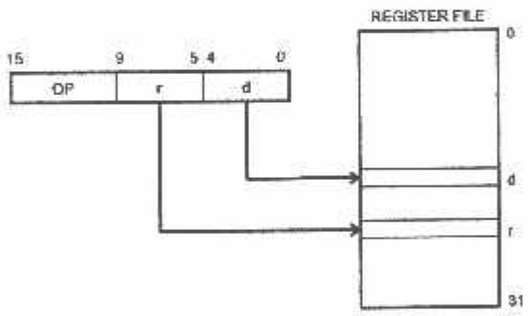
ure 8. Direct Single Register Addressing



e operand is contained in register d (Rd).

gister Direct, Two Registers Rd And Rr

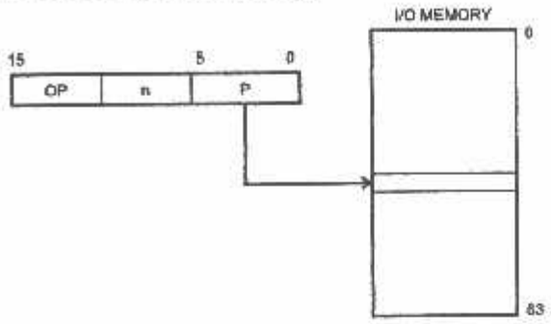
ure 9. Direct Register Addressing, Two Registers



erands are contained in register r (Rr) and d (Rd). The ult is stored in register d (Rd).

I/O Direct

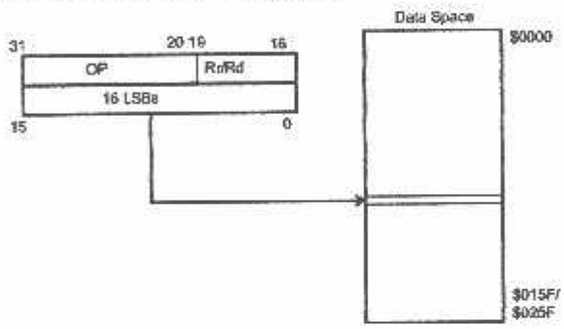
Figure 10. I/O Direct Addressing



Operand address is contained in 6 bits of the instruction word. n is the destination or source register address.

Data Direct

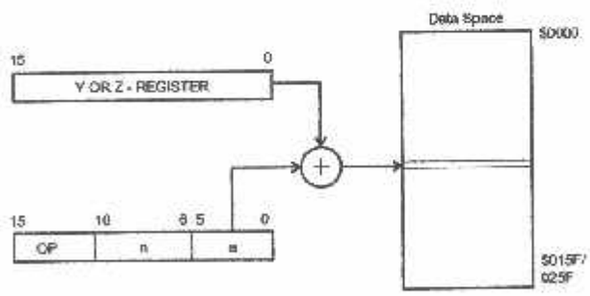
Figure 11. Direct Data Addressing



A 16-bit Data Address is contained in the 16 LSBs of a two-word instruction. Rd/Rr specify the destination or source register.

Data Indirect With Displacement

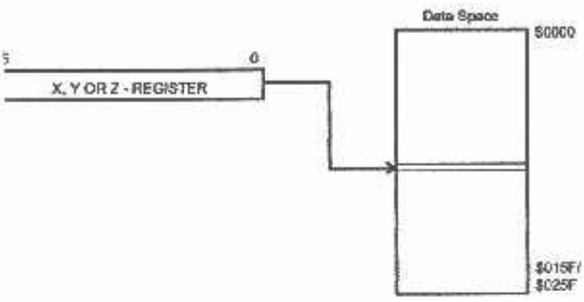
Figure 12. Data Indirect with Displacement



Operand address is the result of the Y or Z-register contents added to the address contained in 6 bits of the instruction word.

:a Indirect

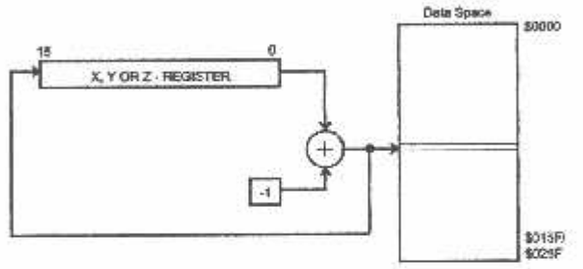
ure 13. Data Indirect Addressing



erand address is the contents of the X, Y or the Z-regis-

ta Indirect With Pre-Decrement

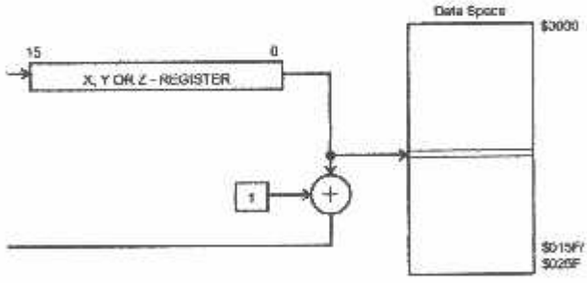
ure 14. Data Indirect Addressing With Pre-Decrement



e X, Y or the Z-register is decremented before the opera-
n. Operand address is the decremented contents of the Y or the Z-register.

ta Indirect With Post-Increment

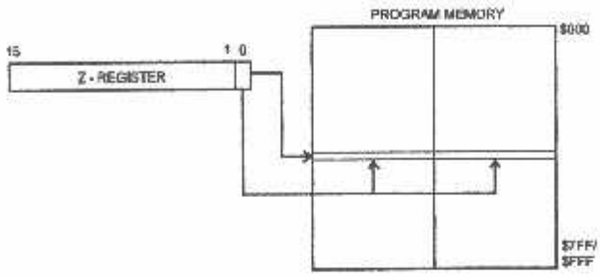
ure 15. Data Indirect Addressing With Post-Increment



e X, Y or the Z-register is incremented after the opera-
n. Operand address is the content of the X, Y or the Z-ister prior to incrementing.

Constant Addressing Using the LPM Instruction

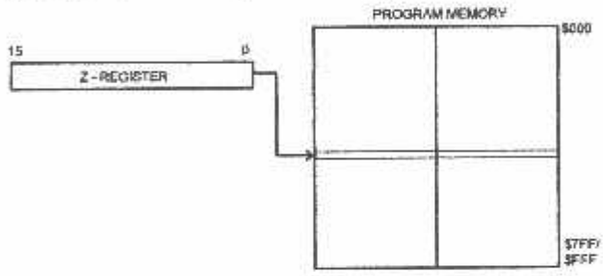
Figure 16. Code Memory Constant Addressing



Constant byte address is specified by the Z-register contents. The 15 MSBs select word address (0 - 2K/4K) and LSB, select low byte if cleared (LSB = 0) or high byte if set (LSB = 1).

Indirect Program Addressing, IJMP and ICALL

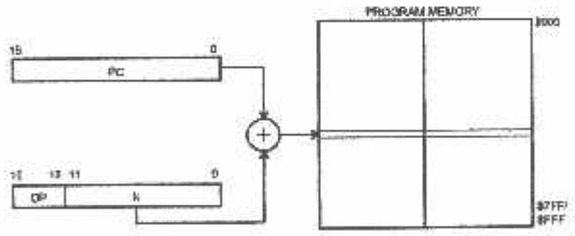
Figure 17. Indirect Program Memory Addressing



Program execution continues at address contained by the Z-register (i.e. the PC is loaded with the contents of the Z-register).

Relative Program Addressing, RJMP and RCALL

Figure 18. Relative Program Memory Addressing



Program execution continues at address PC + k + 1. The relative address k is from -2048 to 2047.

e EEPROM Data Memory

e AT90S4434/8535 contains 256/512 bytes of data PROM memory. It is organized as a separate data ace, in which single bytes can be read and written. The PROM has an endurance of at least 100,000 write/erase les. The access between the EEPROM and the CPU is scribed on page 37 specifying the EEPROM Address gisters, the EEPROM Data Register, and the EEPROM ntrol Register.

the SPI data downloading, see page 71 for a detailed scription.

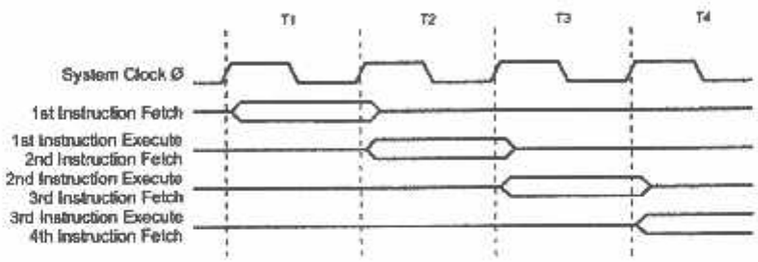
Memory Access Times and Instruction Execution Timing

This section describes the general access timing concepts for instruction execution and internal memory access.

The AVR CPU is driven by the System Clock Ø, directly generated from the external clock crystal for the chip. No internal clock division is used.

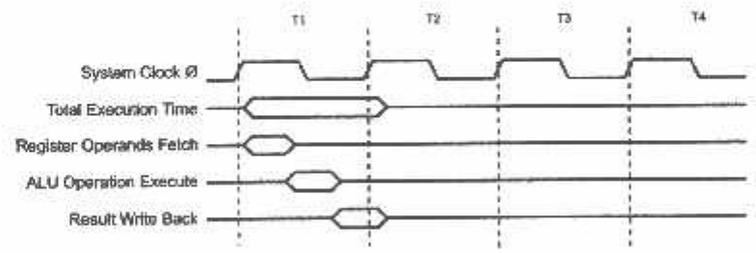
Figure 19 shows the parallel instruction fetches and instruction executions enabled by the Harvard architecture and the fast-access register file concept. This is the basic pipelining concept to obtain up to 1 MIPS per MHz with the corresponding unique results for functions per cost, functions per clocks, and functions per power-unit.

ure 19. The Parallel Instruction Fetches and Instruction Executions



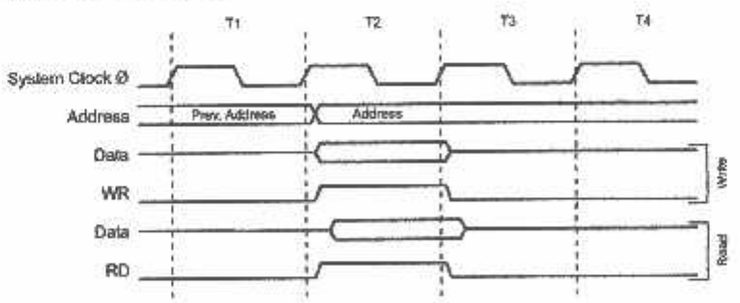
jure 20 shows the internal timing concept for the register . In a single clock cycle an ALU operation using two register operands is executed, and the result is stored back to the destination register.

jure 20. Single Cycle ALU Operation



e internal data SRAM access is performed in two System Clock cycles as described in Figure 21.

ure 21. On-Chip Data SRAM Access Cycles



Memory

I/O space definition of the AT90S4434/8535 is shown in the following table:

le 2. AT90S4434/8535 I/O Space

I/O Address (SRAM Address)	Name	Function
$3F ($5F)	SREG	Status REGister
$3E ($5E)	SPH	Stack Pointer High
$3D ($5D)	SPL	Stack Pointer Low
$3B ($5B)	GIMSK	General Interrupt MaSK register
$3A ($5A)	GIFR	General Interrupt Flag Register
$39 ($59)	TIMSK	Timer/Counter Interrupt MaSK register
$38 ($58)	TIFR	Timer/Counter Interrupt Flag register
$35 ($55)	MCUCR	MCU general Control Register
$34 ($45)	MCUSR	MCU general Status Register
$33 ($53)	TCCR0	Timer/Counter0 Control Register
$32 ($52)	TCNT0	Timer/Counter0 (8-bit)
$2F ($4F)	TCCR1A	Timer/Counter1 Control Register A
$2E ($4E)	TCCR1B	Timer/Counter1 Control Register B
$2D ($4D)	TCNT1H	Timer/Counter1 High Byte
$2C ($4C)	TCNT1L	Timer/Counter1 Low Byte
$2B ($4B)	OCR1AH	Timer/Counter1 Output Compare Register A High Byte
$2A ($4A)	OCR1AL	Timer/Counter1 Output Compare Register A Low Byte
$29 ($49)	OCR1BH	Timer/Counter1 Output Compare Register B High Byte
$28 ($48)	OCR1BL	Timer/Counter1 Output Compare Register B Low Byte
$27 ($47)	ICR1H	T/C 1 Input Capture Register High Byte
$26 ($46)	ICR1L	T/C 1 Input Capture Register Low Byte
$25 ($45)	TCCR2	Timer/Counter2 Control Register
$24 ($44)	TCNT2	Timer/Counter2 (8-bit)
$23 ($43)	OCR2	Timer/Counter2 Output Compare Register
$22 ($42)	ASSR	Asynchronous Mode Status Register
$21 ($41)	WDTCR	Watchdog Timer Control Register
$1F ($3E)	EEARH	EEPROM Address Register High Byte
$1E ($3E)	EEARL	EEPROM Address Register Low Byte
$1D ($3D)	EEDR	EEPROM Data Register
$1C ($3C)	EECR	EEPROM Control Register
$1B ($3B)	PORTA	Data Register, Port A
$1A ($3A)	DDRA	Data Direction Register, Port A
$19 ($39)	PINA	Input Pins, Port A
$18 ($38)	PORTB	Data Register, Port B

ıle 2. AT90S4434/8535 I/O Space (Continued)

I/O Address (SRAM Address)	Name	Function
$17 ($37)	DDRB	Data Direction Register, Port B
$16 ($36)	PINB	Input Pins, Port B
$15 ($35)	PORTC	Data Register, Port C
$14 ($34)	DDRC	Data Direction Register, Port C
$13 ($33)	PINC	Input Pins, Port C
$12 ($32)	PORTD	Data Register, Port D
$11 ($31)	DDRD	Data Direction Register, Port D
$10 ($30)	PIND	Input Pins, Port D
$0F ($2F)	SPDR	SPI I/O Data Register
$0E ($2E)	SPSR	SPI Status Register
$0D ($2D)	SPCR	SPI Control Register
$0C ($2C)	UDR	UART I/O Data Register
$0B ($2B)	USR	UART Status Register
$0A ($2A)	UCR	UART Control Register
$09 ($29)	UBRR	UART Baud Rate Register
$08 ($28)	ACSR	Analog Comparator Control and Status Register
$07 ($27)	ADMUX	ADC Multiplexer Select Register
$06 ($26)	ADCSR	ADC Control and Status Register
$05 ($25)	ADCH	ADC Data Register High
$04 ($24)	ADCL	ADC Data Register Low

te: Reserved and unused locations are not shown in the table.

the different AT90S4434/8535 I/Os and peripherals are ıced in the I/O space. The different I/O locations are ɔessed by the IN and OUT instructions transferring data lween the 32 general purpose working registers and the space. I/O registers within the address range $00 - $1F directly bit-accessible using the SBI and CBI instruc-ıs. In these registers, the value of single bits can be ɔcked by using the SBIS and SBIC instructions. Refer to instruction set chapter for more details.

When using the I/O specific commands, IN, OUT,SBIS and SBIC, the I/O addresses $00 - $3F must be used. When addressing I/O registers as SRAM, $20 must be added to this address. All I/O register addresses throughout this document are shown with the SRAM address in parentheses.

The different I/O and peripherals control registers are explained in the following sections.

e Status Register - SREG

e *AVR* status register - SREG - at I/O space location $3F iF) is defined as:

	7	6	5	4	3	2	1	0	
F ($5F)	I	T	H	S	V	N	Z	C	SREG
ead/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
tial value	0	0	0	0	0	0	0	0	

Bit 7 - I: Global Interrupt Enable

e global interrupt enable bit must be set (one) for the errupts to be enabled. The individual interrupt enable ntrol is then performed in the interrupt mask registers - GIMSK and TIMSK. If the global interrupt enable register is cleared (zero), none of the interrupts are enabled independent of the GIMSK and TIMSK values. The I-bit is cleared

ardware after an interrupt has occurred, and is set by RETI instruction to enable subsequent interrupts.

t 6 - T: Bit Copy Storage

bit copy instructions BLD (Bit LoaD) and BST (Bit re) use the T bit as source and destination for the oper- l bit. A bit from a register in the register file can be cop- into T by the BST instruction, and a bit in T can be ed into a bit in a register in the register file by the BLD uction.

t 5 - H: Half Carry Flag

half carry flag H indicates a half carry in some arith- ic operations. See the Instruction Set Description for ailed information.

t 4 - S: Sign Bit, S = N ⊕ V

S-bit is always an exclusive or between the negative N and the two's complement overflow flag V. See the ruction Set Description for detailed information.

- **Bit 3 - V: Two's Complement Overflow Flag**

The two's complement overflow flag V supports two's complement arithmetics. See the Instruction Set Description for detailed information.

- **Bit 2 - N: Negative Flag**

The negative flag N indicates a negative result after the different arithmetic and logic operations. See the Instruction Set Description for detailed information.

- **Bit 1 - Z: Zero Flag**

The zero flag Z indicates a zero result after the different arithmetic and logic operations. See the Instruction Set Description for detailed information.

- **Bit 0 - C: Carry Flag**

The carry flag C indicates a carry in an arithmetic or logic operation. See the Instruction Set Description for detailed information.

The Stack Pointer - SP

The AT90S4434/8535 Stack Pointer is implemented as two 8-bit registers in the I/O space locations $3E ($5E) and $3D ($5D). As the AT90S4434/8535 data memory has $25F locations, 10 bits are used.

	15	14	13	12	11	10	9	8	
E ($5E)	-	-	-	-	-	-	SP9	SP8	SPH
D ($5D)	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SPL
	7	6	5	4	3	2	1	0	
ad/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
tial value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

e Stack Pointer points to the data SRAM stack area ere the Subroutine and Interrupt Stacks are located. s Stack space in the data SRAM must be defined by the gram before any subroutine calls are executed or inter- ts are enabled. The Stack Pointer is decremented by e when data is pushed onto the Stack with the PUSH truction, and it is decremented by two when data is pushed onto the Stack with subroutine CALL and interrupt. The Stack Pointer is incremented by one when data is popped from the Stack with the POP instruction, and it is incremented by two when data is popped from the Stack with return from subroutine RET or return from interrupt IRET.

set and Interrupt Handling

e AT90S4434/8535 provides 16 different interrupt irces. These interrupts and the separate reset vector, h have a separate program vector in the program mem- space. All interrupts are assigned individual enable bits ch must be set (one) together with the I-bit in the status ister in order to enable the interrupt.

The lowest addresses in the program memory space are automatically defined as the Reset and Interrupt vectors. The complete list of vectors is shown in Table 3. The list also determines the priority levels of the different interrupts. The lower the address the higher is the priority level. RESET has the highest priority, and next is INT0 - the External Interrupt Request 0, etc.

le 3. Reset and Interrupt Vectors

Vector No.	Program Address	Source	Interrupt Definition
1	$000	RESET	Hardware Pin and Watchdog Reset
2	$001	INT0	External Interrupt Request 0
3	$002	INT1	External Interrupt Request 1
4	$003	TIMER2 COMP	Timer/Counter2 Compare Match
5	$004	TIMER2 OVF	Timer/Counter2 Overflow
6	$005	TIMER1 CAPT	Timer/Counter1 Capture Event
7	$006	TIMER1 COMPA	Timer/Counter1 Compare Match A
8	$007	TIMER1 COMPB	Timer/Counter1 Compare Match B
9	$008	TIMER1 OVF	Timer/Counter1 Overflow
10	$009	TIMER0 OVF	Timer/Counter0 Overflow
11	$00A	SPI, STC	Serial Transfer Complete
12	$00B	UART, RX	UART, Rx Complete
13	$00C	UART, UDRE	UART Data Register Empty
14	$00D	UART, TX	UART, Tx Complete
15	$00E	ADC	ADC Conversion Complete
16	$00F	EE_RDY	EEPROM Ready
17	$010	ANA_COMP	Analog Comparator

most typical and general program setup for the Reset Interrupt Vector Addresses are:

```
Address     Labels   Code            Comments
$000                 rjmp   RESET    ; Reset Handler
$001                 rjmp   EXT_INT0 ; IRQ0 Handler
$002                 rjmp   EXT_INT1 ; IRQ1 Handler
$003                 rjmp   TIM2_COMP ; Timer2 Compare Handler
$004                 rjmp   TIM2_OVF ; Timer2 Overflow Handler
$005                 rjmp   TIM1_CAPT ; Timer1 Capture Handler
$006                 rjmp   TIM1_COMPA ; Timer1 CompareA Handler
$007                 rjmp   TIM1_COMPB ; Timer1 CompareB Handler
$008                 rjmp   TIM1_OVF ; Timer1 Overflow Handler
$009                 rjmp   TIM0_OVF ; Timer0 Overflow Handler
$00a                 rjmp   SPI_STC; ; SPI Transfer Complete Handler
$00b                 rjmp   UART_RXC ; UART RX Complete Handler
$00c                 rjmp   UART_DRE ; UDR Empty Handler
$00d                 rjmp   UART_TXC ; UART TX Complete Handler
$00e                 rjmp   ADC      ; ADC Conversion Complete interrupt Handler
$00f                 rjmp   EE_RDY   ; EEPROM Ready Handler
$010                 rjmp   ANA_COMP ; Analog Comparator Handler
;
$011    MAIN:        <instr>  xxx    ; Main program start
...     ...          ...      ...
```

set Sources

e AT90S4434/8535 has three sources of reset:

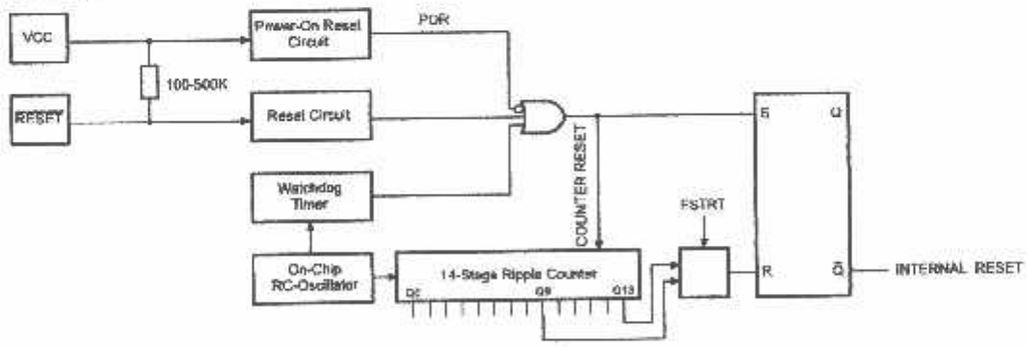
Power-On Reset. The MCU is reset when a supply voltage is applied to the V_{CC} and GND pins.

External Reset. The MCU is reset when a low level is present on the $\overline{\text{RESET}}$ pin for more than two XTAL cycles

Watchdog Reset. The MCU is reset when the Watchdog Timer period expires, and the Watchdog is enabled.

During reset, all I/O registers are then set to their initial values, and the program starts execution from address $000. The instruction placed in address $000 must be an RJMP - relative jump - instruction to the reset handling routine. If the program never enables an interrupt source, the interrupt vectors are not used, and regular program code can be placed at these locations. The circuit diagram in Figure 22 shows the reset logic. Table 4 defines the timing and electrical parameters of the reset circuitry.

ure 22. Reset Logic



ıle 4. Reset Characteristics (V_{CC} = 5.0V)

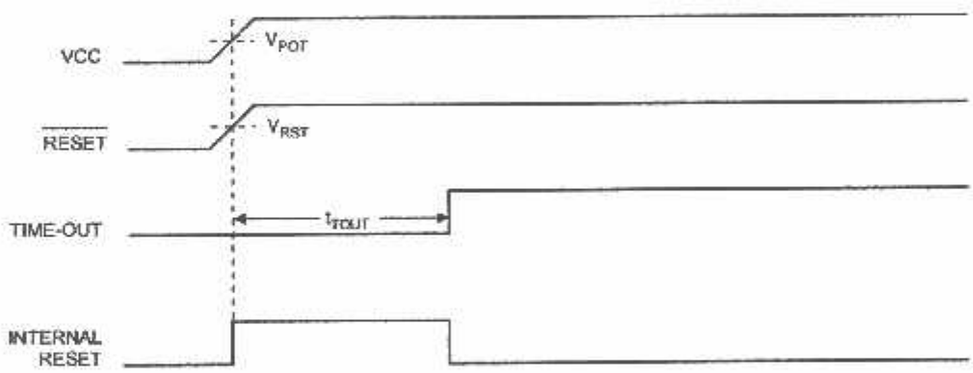
Symbol	Parameter	Min	Typ	Max	Units
V_{POT}	Power-On Reset Threshold Voltage	1.4	1.6	1.8	V
V_{RST}	$\overline{\text{RESET}}$ Pin Threshold Voltage		$0.6V_{CC}$		V
t_{TOUT}	Reset Delay Time-Out Period FSTRT Unprogrammed	11	16	21	ms
t_{TOUT}	Reset Delay Time-Out Period FSTRT Programmed	1.0	1.1	1.2	ms

ıer-On Reset

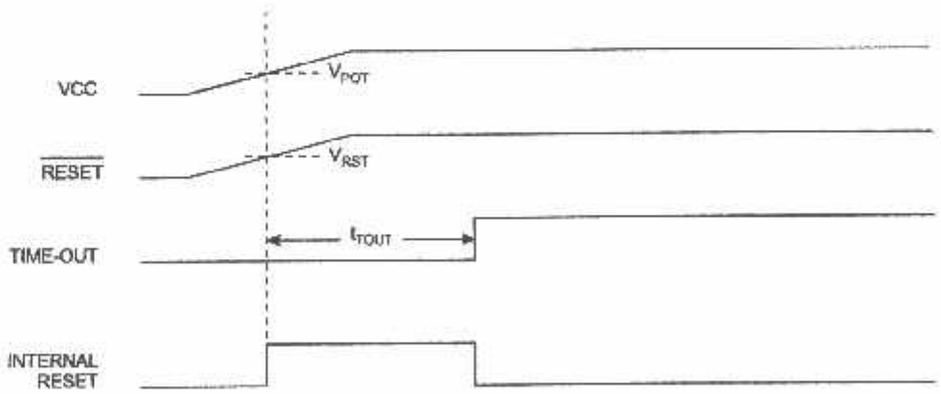
'ower-On Reset (POR) circuit ensures that the device is started until V_{CC} has reached a safe level. As shown in ure 22, an internal timer clocked from the Watchdog er oscillator prevents the MCU from starting until after a tain period after V_{CC} has reached the Power-On Threshvoltage - V_{POT}, regardless of the V_{CC} rise time (see Fig-23 and Figure 24). The FSTRT fuse bit in the Flash can programmed to give a shorter start-up time if a ceramic resonator or any other fast-start oscillator is used to clock the MCU.

If the built-in start-up delay is sufficient, $\overline{\text{RESET}}$ can be connected to V_{CC} directly or via an external pull-up resistor. By holding the pin low for a period after V_{CC} has been applied, the Power-On Reset period can be extended. Refer to Figure 25 for a timing example on this.

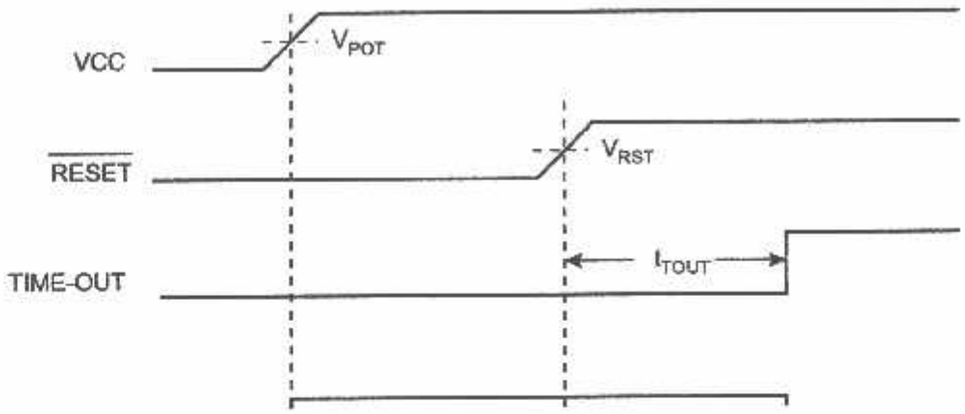
ıure 23. MCU Start-Up, $\overline{\text{RESET}}$ Tied to V_{CC}, Rapidly Rising V_{CC}



ure 24. MCU Start-Up, $\overline{\text{RESET}}$ Tied to V_{CC}, Slowly Rising V_{CC}



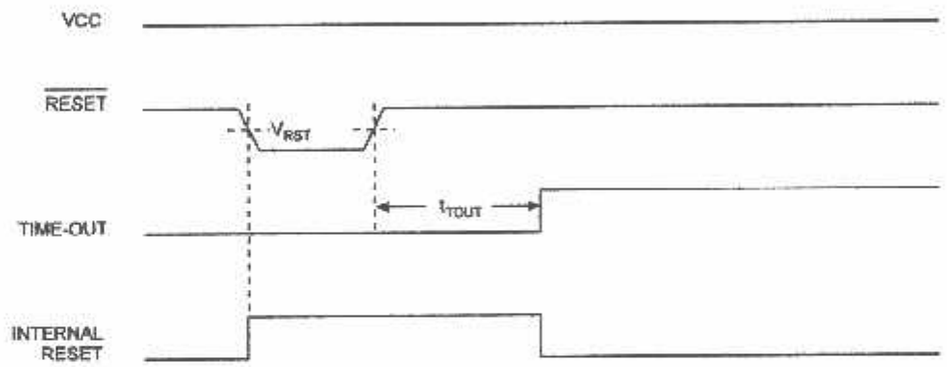
ure 25. MCU Start-Up, $\overline{\text{RESET}}$ Controlled Externally



ternal Reset

external reset is generated by a low level on the $\overline{\text{RESET}}$. The $\overline{\text{RESET}}$ pin must be held low for at least two crys- clock cycles. When the applied signal reaches the Reset Threshold Voltage - V_{RST} on its positive edge, the delay timer starts the MCU after the Time-out period t_{TOUT} has expired.

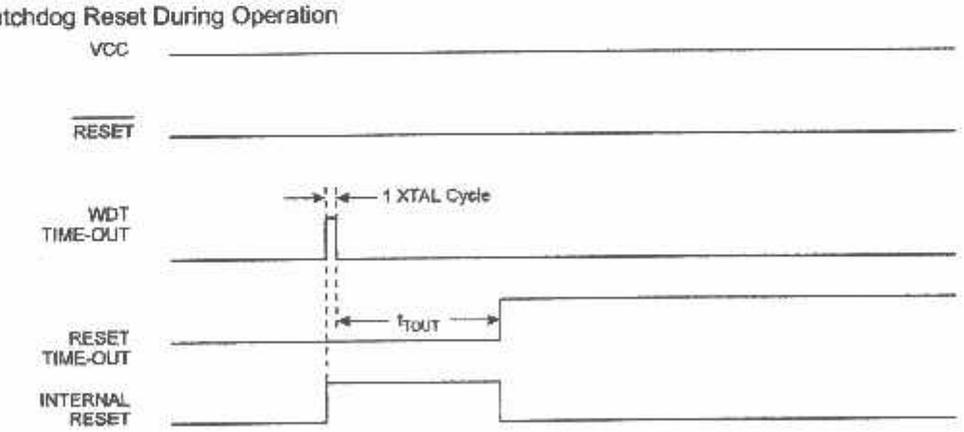
ure 26. External Reset During Operation



tchdog Reset

len the Watchdog times out, it will generate a short reset se of 1 XTAL cycle duration. On the falling edge of this pulse, the delay timer starts counting the Time-out period t_{TOUT}. Refer to page 36 for details on operation of the Watchdog.

ure 27. Watchdog Reset During Operation



:U Status Register - MCUSR

e MCU Status Register provides information on which set source caused an MCU reset.

t	7	6	5	4	3	2	1	0	
4 ($54)	-	-	-	-	-	-	EXTRF	PORF	MCUSR
ad/Write	R	R	R	R	R	R	R/W	R/W	
tial value	0	0	0	0	0	0	See bit description		

Bits 7..2 - Res: Reserved Bits

ese bits are reserved bits in the AT90S4434/8535 and ays read as zero.

Bit 1 - PORF: Power On Reset Flag

is bit is only cleared by a power on reset. A watchdog set or an external reset will leave this bit unchanged.

Bit 2 - EXTRF: External Reset Flag

er a power on reset, this bit is undefined (X). It can only cleared by an external reset. A watchdog reset will leave s bit unchanged.

summarize, the following table shows the value of these o bits after the three modes of reset:

ble 5. PORF and EXTRF Values after Reset

teset Source	PORF	EXTRF
ower On Reset	1	undefined
External Reset	unchanged	1
Watchdog Reset	unchanged	unchanged

make use of these bits to identify a reset condition, the er software should set both the PORF and EXTRF bits early as possible in the program. Checking the PORF d EXTRF values is done before the bits are set. If the bit comes set before an external or watchdog reset occurs, the source of reset can be found by using the following truth table:

Table 6. Reset Source Identification

PORF	EXTRF	Reset Source
0	0	Watchdog Reset
0	1	External Reset
1	0	Power-On Reset
1	1	Power-On Reset

Interrupt Handling

The AT90S4434/8535 has two 8-bit Interrupt Mask control registers: GIMSK - General Interrupt Mask register and TIMSK - Timer/Counter Interrupt Mask register.

When an interrupt occurs, the Global Interrupt Enable I-bit is cleared (zero) and all interrupts are disabled. The user software must set (one) the I-bit to enable interrupts.

When the Program Counter is vectored to the actual interrupt vector in order to execute the interrupt handling routine, hardware clears the corresponding flag that generated the interrupt. Some of the interrupt flags can also be cleared by writing a logic one to the flag bit position(s) to be cleared.

e General Interrupt Mask Register - GIMSK

t	7	6	5	4	3	2	1	0	
B ($5B)	INT1	INT0	-	-	-	-	-	-	GIMSK
ad/Write	R/W	R/W	R	R	R	R	R	R	
tial value	0	0	0	0	0	0	0	0	

Bit 7 - INT1: External Interrupt Request 1 Enable

ıen the INT1 bit is set (one) and the I-bit in the Status gister (SREG) is set (one), the external pin interrupt is ivated. The Interrupt Sense Control bits 1/0 (ISC11 and C10) in the MCU general Control Register (MCUCR) fine whether the external interrupt is activated on rising falling edge of the INT1 pin or level sensed. Activity on pin will cause an interrupt request even if INT1 is con- ured as an output. The corresponding interrupt of Exter- l Interrupt Request 1 is executed from program memory dress $002. See also "External Interrupts".

- **Bit 6 - INT0: External Interrupt Request 0 Enable**

When the INT0 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the external pin interrupt is activated. The Interrupt Sense Control bits 1/0 (ISC01 and ISC00) in the MCU general Control Register (MCUCR) define whether the external interrupt is activated on rising or falling edge of the INT0 pin or level sensed. Activity on the pin will cause an interrupt request even if INT0 is configured as an output. The corresponding interrupt of External Interrupt Request 0 is executed from program memory address $001. See also "External Interrupts."

- **Bits 5..0 - Res: Reserved bits**

These bits are reserved bits in the AT90S4434/8535 and always read as zero.

General Interrupt Flag Register - GIFR

	7	6	5	4	3	2	1	0	
($5A)	INTF1	INTF0	-	-	-	-	-	-	GIFR
ad/Write	R/W	R/W	R	R	R	R	R	R	
ial value	0	0	0	0	0	0	0	0	

it 7 - INTF1: External Interrupt Flag1
en an event on the INT1 pin triggers an interrupt uest, INTF1 becomes set (one). If the I-bit in SREG and INT1 bit in GIMSK are set (one), the MCU will jump to interrupt vector at address $002. The flag is cleared en the interrupt routine is executed. Alternatively, the can be cleared by writing a logical one to it.

- **Bit 6 - INTF0: External Interrupt Flag0**

When an event on the INT0 pin triggers an interrupt request, INTF0 becomes set (one). If the I-bit in SREG and the INT0 bit in GIMSK are set (one), the MCU will jump to the Interrupt vector at address $001. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical one to it.

- **Bits 5..0 - Res: Reserved bits**

These bits are reserved bits in the AT90S4434/8535 and always read as zero.

Timer/Counter Interrupt Mask Register - TIMSK

	7	6	5	4	3	2	1	0	
($59)	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	-	TOIE0	TIMSK
ad/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
ial value	0	0	0	0	0	0	0	0	

3it 7 - OCIE2: Timer/Counter2 Output Compare Match nterrupt Enable
ıen the OCIE1A bit is set (one) and the I-bit in the Status igister is set (one), the Timer/Counter2 Compare Match errupt is enabled. The corresponding interrupt (at vector 03) is executed if a compare match in Timer/Counter2 curs. The compare flag in Timer/Counter2 is set (one) in Timer/Counter Interrupt Flag Register - TIFR.

3it 6 - TOIE2: Timer/Counter2 Overflow Interrupt Enable
ıen the TOIE2 bit is set (one) and the I-bit in the Status gister is set (one), the Timer/Counter2 Overflow interrupt enabled. The corresponding interrupt (at vector $004) is ecuted if an overflow in Timer/Counter2 occurs. The ner/Counter2 Overflow Flag is set (one) in the ner/Counter Interrupt Flag Register - TIFR. When ner/Counter1 is in PWM mode, the Timer Overflow flag set when the counter changes counting direction at $00.

3it 5 - TICIE1: Timer/Counter1 Input Capture Interrupt Enable
ıen the TICIE1 bit is set (one) and the I-bit in the Status gister is set (one), the Timer/Counter1 Input Capture ent Interrupt is enabled. The corresponding interrupt (at ctor $005) is executed if a capture-triggering event curs on pin 20, PD6 (ICP). The Input Capture Flag in ner/Counter1 is set (one) in the Timer/Counter Interrupt ig Register - TIFR.

3it 4- OCE1A: Timer/Counter1 Output CompareA Match nterrupt Enable
ıen the OCIE1A bit is set (one) and the I-bit in the Status igister is set (one), the Timer/Counter1 CompareA Match errupt is enabled. The corresponding interrupt (at vector 06) is executed if a CompareA match in Timer/Counter1 occurs. The CompareA Flag in Timer/Counter1 is set (one) in the Timer/Counter Interrupt Flag Register - TIFR.

- **Bit 3 - OCIE1B: Timer/Counter1 Output CompareB Match Interrupt Enable**

When the OCIE1B bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 CompareB Match interrupt is enabled. The corresponding interrupt (at vector $007) is executed if a CompareB match in Timer/Counter1 occurs. The CompareB Flag in Timer/Counter1 is set (one) in the Timer/Counter Interrupt Flag Register - TIFR.

- **Bit 2 - TOIE1: Timer/Counter1 Overflow Interrupt Enable**

When the TOIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Overflow interrupt is enabled. The corresponding interrupt (at vector $008) is executed if an overflow in Timer/Counter1 occurs. The Overflow Flag (Timer/Counter1) is set (one) in the Timer/Counter Interrupt Flag Register - TIFR. When Timer/Counter1 is in PWM mode, the Timer Overflow flag is set when the counter changes counting direction at $0000.

- **Bit 1 - Res: Reserved bit**

This bit is a reserved bit in the AT90S4434/8535 and always reads zero.

- **Bit 0 - TOIE0: Timer/Counter0 Overflow Interrupt Enable**

When the TOIE0 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter0 Overflow interrupt is enabled. The corresponding interrupt (at vector $009) is executed if an overflow in Timer/Counter0 occurs. The Overflow Flag (Timer0) is set (one) in the Timer/Counter Interrupt Flag Register - TIFR.

e Timer/Counter Interrupt Flag Register - TIFR

	7	6	5	4	3	2	1	0	
i6 ($58)	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	-	TOV0	TIFR
ead/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
tial value	0	0	0	0	0	0	0	0	

3it 7 - OCF2: Output Compare Flag 2

e OCF2 bit is set (one) when compare match occurs tween the Timer/Counter2 and the data in OCR2 - Out- t Compare Register2. OCF2 is cleared by hardware en executing the corresponding interrupt handling vec- . Alternatively, OCF2 is cleared by writing a logic one to e flag. When the I-bit in SREG, and OCIE2 mer/Counter2 Compare match Interrupt Enable), and OCF2 are set (one), the Timer/Counter2 Compare tch Interrupt is executed.

3it 6 - TOV2: Timer/Counter0 Overflow Flag

e TOV2 bit is set (one) when an overflow occurs in ner/Counter2. TOV2 is cleared by hardware when exe- ting the corresponding interrupt handling vector. Alterna- ely, TOV2 is cleared by writing a logic one to the flag. nen the SREG I-bit, and TOIE2 (Timer/Counter2 Over- w Interrupt Enable), and TOV2 are set (one), the ner/Counter2 Overflow interrupt is executed. In PWM de, this bit is set when Timer/Counter2 changes count- direction at $00.

Bit 5 - ICF1: Input Capture Flag 1

e ICF1 bit is set (one) to flag an input capture event, indi- ting that the Timer/Counter1 value has been transferred the input capture register - ICR1. ICF1 is cleared by rdware when executing the corresponding interrupt han- g vector. Alternatively, ICF1 is cleared by writing a logic e to the flag.

3it 4 - OCF1A: Output Compare Flag 1A

e OCF1A bit is set (one) when compare match occurs tween the Timer/Counter1 and the data in OCR1A - Out- t Compare Register 1A. OCF1A is cleared by hardware en executing the corresponding interrupt handling vec- . Alternatively, OCF1A is cleared by writing a logic one to e flag. When the I-bit in SREG, and OCIE1A mer/Counter1 Compare match InterruptA Enable), and the OCF1A are set (one), the Timer/Counter1A Compare match Interrupt is executed.

- **Bit 3 - OCF1B: Output Compare Flag 1B**

The OCF1B bit is set (one) when compare match occurs between the Timer/Counter1 and the data in OCR1B - Output Compare Register 1B. OCF1B is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, OCF1B is cleared by writing a logic one to the flag. When the I-bit in SREG, and OCIE1B (Timer/Counter1 Compare match InterruptB Enable), and the OCF1B are set (one), the Timer/Counter1B Compare match Interrupt is executed.

- **Bit 2 - TOV1: Timer/Counter1 Overflow Flag**

The TOV1 is set (one) when an overflow occurs in Timer/Counter1. TOV1 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, TOV1 is cleared by writing a logic one to the flag. When the I-bit in SREG, and TOIE1 (Timer/Counter1 Overflow Interrupt Enable), and TOV1 are set (one), the Timer/Counter1 Overflow Interrupt is executed. In PWM mode, this bit is set when Timer/Counter1 changes counting direction at $0000.

- **Bit 1 - Res: Reserved bit**

This bit is a reserved bit in the AT90S4434/8535 and always reads zero.

- **Bit 0 - TOV0: Timer/Counter0 Overflow Flag**

The bit TOV0 is set (one) when an overflow occurs in Timer/Counter0. TOV0 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, TOV0 is cleared by writing a logic one to the flag. When the SREG I-bit, and TOIE0 (Timer/Counter0 Overflow Interrupt Enable), and TOV0 are set (one), the Timer/Counter0 Overflow interrupt is executed.

:ernal Interrupts

: external interrupts are triggered by the INT1 and INT0 s. Observe that, if enabled, the interrupts will trigger :n if the INT0/INT1 pins are configured as outputs. This ture provides a way of generating a software interrupt. : external interrupts can be triggered by a falling or ris- edge or a low level. This is set up as indicated in the :cification for the MCU Control Register - MCUCR. :en the external interrupt is enabled and is configured as :l triggered, the interrupt will trigger as long as the pin is d low.

: external interrupts are set up as described in the spec- ation for the MCU Control Register - MCUCR.

:rrupt Response Time

: interrupt execution response for all the enabled *AVR* :rrupts is 4 clock cycles minimum. 4 clock cycles after interrupt flag has been set, the program vector address the actual interrupt handling routine is executed. During : 4 clock cycle period, the Program Counter (2 bytes) is shed onto the Stack, and the Stack Pointer is decre- :nted by 2. The vector is a relative jump to the interrupt routine, and this jump takes 2 clock cycles. If an interrupt occurs during execution of a multi-cycle instruction, this instruction is completed before the interrupt is served.

A return from an interrupt handling routine (same as for a subroutine call routine) takes 4 clock cycles. During these 4 clock cycles, the Program Counter (2 bytes) is popped back from the Stack, and the Stack Pointer is incremented by 2. When the *AVR* exits from an interrupt, it will always return to the main program and execute one more instruction before any pending interrupt is served.

Note that the Status Register - SREG - is not handled by the *AVR* hardware, neither for interrupts nor for subroutines. For the interrupt handling routines requiring a storage of the SREG, this must be performed by user software.

For interrupts triggered by events that can remain static (e.g. the Output Compare Register1 A matching the value of Timer/Counter1) the interrupt flag is set when the event occurs. If the interrupt flag is cleared and the interrupt condition persists, the flag will not be set until the event occurs the next time.

:U Control Register - MCUCR

: MCU Control Register contains control bits for general :U functions.

	7	6	5	4	3	2	1	0	
35 ($55)	-	SE	SM1	SM0	ISC11	ISC10	ISC01	ISC00	MCUCR
ead/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
itial value	0	0	0	0	0	0	0	0	

Bit 7 - Res: Reserved bit

is bit is a reserved bit in the AT90S4434/8535 and ways reads zero.

Bit 6 - SE: Sleep Enable

: SE bit must be set (one) to make the MCU enter the ep mode when the SLEEP instruction is executed. To oid the MCU entering the sleep mode unless it is the pro- ammers purpose, it is recommended to set the Sleep able SE bit just before the execution of the SLEEP truction.

Bits 5,4 - SM1/SM0: Sleep Mode Select bits 1 and 0

is bit selects between the three available sleep modes shown in the following table.

ble 7. Sleep Mode Select

SM1	SM0	Sleep Mode
0	0	Idle Mode
0	1	Reserved
1	0	Power Down
1	1	Power Save

- **Bits 3, 2 - ISC11, ISC10: Interrupt Sense Control 1 bit 1 and bit 0**

The External Interrupt 1 is activated by the external pin INT1 if the SREG I-flag and the corresponding interrupt mask in the GIMSK is set. The level and edges on the external INT1 pin that activate the interrupt are defined in the following table.

Table 8. Interrupt 1 Sense Control

ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Reserved
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.

Note: When changing the ISC11/ISC10 bits, INT1 must be disabled by clearing its Interrupt Enable bit in the GIMSK Register. Otherwise an interrupt can occur when the bits are changed.

ıit 1, 0 - ISC01, ISC00: Interrupt Sense Control 0 bit 1 and it 0

ə External Interrupt 0 is activated by the external pin T0 if the SREG I-flag and the corresponding interrupt sk is set. The level and edges on the external INT0 pin t activate the interrupt are defined in the following table:

ble 9. Interrupt 0 Sense Control

SC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Reserved
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

ıe: When changing the ISC10/ISC00 bits, INT0 must be disabled by clearing its Interrupt Enable bit in the GIMSK Register. Otherwise an interrupt can occur when the bits are changed.

eep Modes

ı enter any of the three sleep modes, the SE bit in CUCR must be set (one) and a SLEEP instruction must executed. The SM1 and SM0 bits in the MCUCR register select which sleep mode (Idle, Power Down, or Power ve) will be activated by the SLEEP instruction.

ın enabled interrupt occurs while the MCU is in a sleep ıde, the MCU awakes, executes the interrupt routine, d resumes execution from the instruction following EEP. If a reset occurs during sleep mode, the MCU kes up and executes from the Reset vector. The conıts of the register file, SRAM, and I/O memory are unaled when the device wakes up from sleep. See Table 7 how to select sleep mode.

te that if a level triggered interrupt is used for wake-up n power down or power save, the low level must be held a time longer than the reset delay time-out period t_{TOUT}. ıerwise, the device will not wake up.

ə Mode

ıen the SM1/SM0 bits are set to 00, the SLEEP instruction forces the MCU into the Idle Mode stopping the CPU but allowing Timer/Counters, Watchdog and the interrupt system to continue operating. This enables the MCU to wake up from external triggered interrupts as well as internal ones like the Timer Overflow and UART Receive Complete interrupts. If wake-up from the Analog Comparator interrupt is not required, the analog comparator can be powered down by setting the ACD-bit in the Analog Comparator Control and Status register - ACSR. This will reduce power consumption in Idle Mode. When the MCU wakes up from Idle mode, the CPU starts program execution immediately.

Power Down Mode

When the SM1/SM0 bits are 10, the SLEEP instruction forces the MCU into the Power Down Mode. In this mode, the external oscillator is stopped. The user can select whether the watchdog shall be enabled during power-down mode. If the watchdog is enabled, it will wake up the MCU when the Watchdog Time-out period expires. If the watchdog is disabled, only an external reset or an external level triggered interrupt can wake up the MCU.

Power Save Mode

When the SM1/SM0 bits are 11, the SLEEP instruction forces the MCU into the Power Save Mode. This mode is identical to Power Down, with one exception:

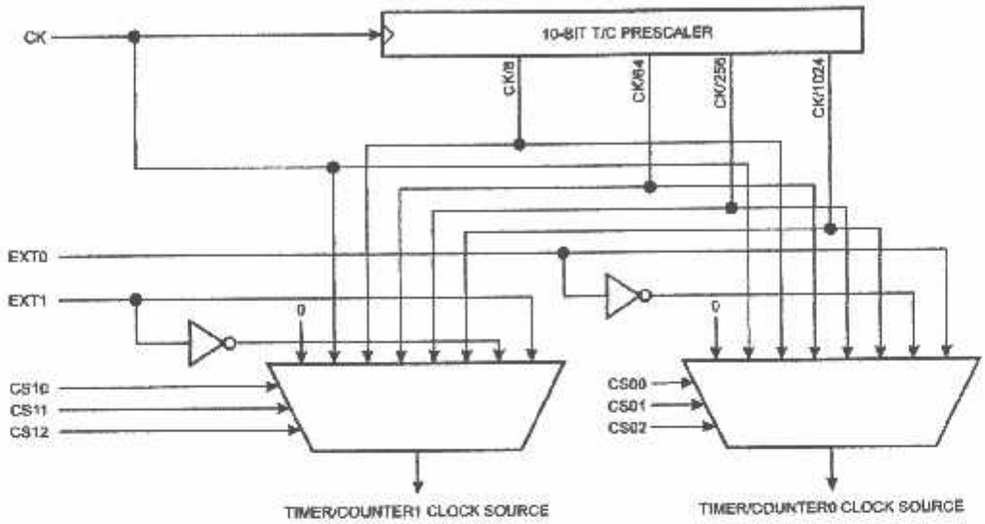
If Timer/Counter2 is clocked asynchronously, i.e. the AS2 bit in ASSR is set, Timer/Counter2 will run during sleep. The device can wake up from either Timer Overflow or Output Compare interrupt from Timer/Counter2.

Timer / Counters

The AT90S4434/8535 provides three general purpose Timer/Counters - two 8-bit T/Cs and one 16-bit T/C. Timer/Counter2 can as an option be asynchronously clocked from an external oscillator. This oscillator is optimized for use with a 32.768 kHz watch crystal, enabling use of Timer/Counter2 as a Real Time Clock (RTC). Timer/Counters 0 and 1 have individual prescaling selection from the same 10-bit prescaling timer. Timer/Counter2 has its own prescaler. These Timer/Counters can either be used as a timer with an internal clock timebase or as a counter with an external pin connection which triggers the counting.

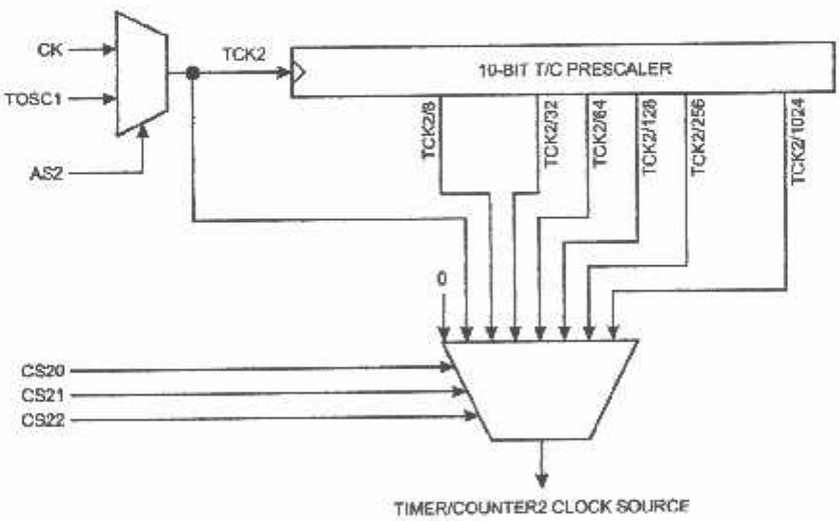
e Timer/Counter Prescalers

ure 28. Prescaler for Timer/Counter0 and 1



r Timer/Counters 0 and 1, the four different prescaled ections are: CK/8, CK/64, CK/256 and CK/1024, where is the oscillator clock. For the two Timer/Counters 0 and 1, CK, external source, and stop, can also be selected as clock sources.

ure 29. Timer/Counter2 Prescaler



e clock source for Timer/Counter2 is named TCK2. K2 is by default connected to the main system clock CK. setting the AS2 bit in ASSR, Timer/Counter2 is asyn- onously clocked from the PC6(TOSC1) pin. This ables use of Timer/Counter2 as a Real Time Clock TC). When AS2 is set, pins PC6(TOSC1) and 7(TOSC2) are disconnected from Port C and connected a crystal oscillator. A crystal can then be connected between the PC6(TOSC1) and PC7(TOSC2) pins to serve as an independent clock source for Timer/Counter2. The oscillator is optimized for use with a 32.768 kHz crystal. Alternatively, an external clock signal can be applied to PC6(TOSC1). The frequency of this clock must be lower than one fourth of the CPU clock and not higher than 256 kHz.

ıe 8-Bit Timer/Counter0

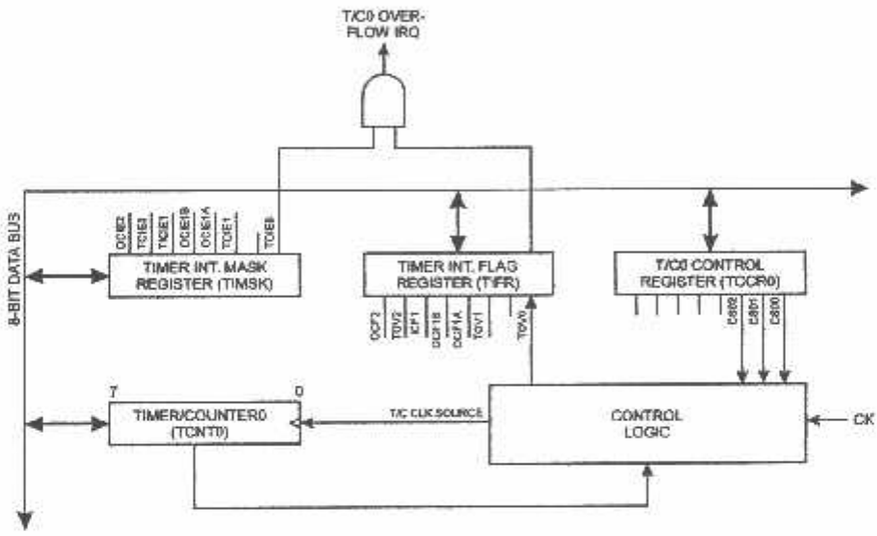
ıure 30 shows the block diagram for Timer/Counter0.

e 8-bit Timer/Counter0 can select clock source from CK, escaled CK, or an external pin. In addition it can be opped as described in the specification for the ner/Counter0 Control Register - TCCR0. The overflow tus flag is found in the Timer/Counter Interrupt Flag gister - TIFR. Control signals are found in the ner/Counter0 Control Register - TCCR0. The interrupt able/disable settings for Timer/Counter0 are found in the ner/Counter Interrupt Mask Register - TIMSK.

When Timer/Counter0 is externally clocked, the external signal is synchronized with the oscillator frequency of the CPU. To assure proper sampling of the external clock, the minimum time between two external clock transitions must be at least one internal CPU clock period. The external clock signal is sampled on the rising edge of the internal CPU clock.

The 8-bit Timer/Counter0 features both a high resolution and a high accuracy usage with the lower prescaling opportunities. Similarly, the high prescaling opportunities make the Timer/Counter0 useful for lower speed functions or exact timing functions with infrequent actions.

ıure 30. Timer/Counter0 Block Diagram



e Timer/Counter0 Control Register - TCCR0

	7	6	5	4	3	2	1	0	
ı ($53)	-	-	-	-	-	CS02	CS01	CS00	TCCR0
ad/Write	R	R	R	R	R	R/W	R/W	R/W	
ial value	0	0	0	0	0	0	0	0	

ilts 7..3 - Res: Reserved bits

ese bits are reserved bits in the AT90S4434/8535 and ays read zero.

ilts 2,1,0 - CS02, CS01, CS00: Clock Select0, bit 2,1 and 0

e Clock Select0 bits 2,1 and 0 define the prescaling ırce of Timer0.

ıle 10. Clock 0 Prescale Select

CS02	CS01	CS00	Description
0	0	0	Stop, Timer/Counter0 is stopped.
0	0	1	CK
0	1	0	CK / 8
0	1	1	CK / 64
1	0	0	CK / 256
1	0	1	CK / 1024
1	1	0	External Pin T0, falling edge
1	1	1	External Pin T0, rising edge

ɜ Stop condition provides a Timer Enable/Disable func-
ı. The prescaled CK modes are scaled directly from the
. oscillator clock. If the external pin modes are used, the corresponding setup must be performed in the actual data direction control register (cleared to zero gives an input pin).

e Timer Counter 0 - TCNT0

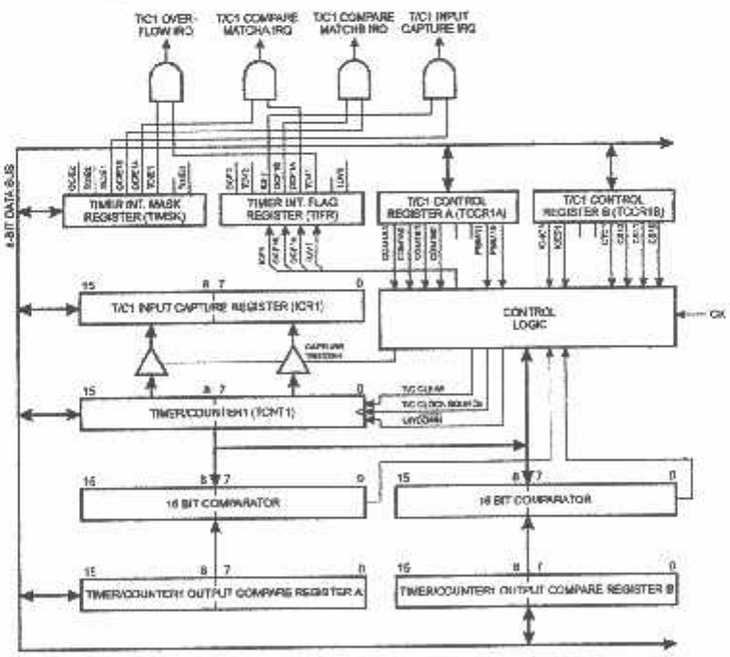
	7	6	5	4	3	2	1	0	
ı2 ($52)	MSB							LSB	TCNT0
ead/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
itial value	0	0	0	0	0	0	0	0	

e Timer/Counter0 is realized as an up-counter with read
d write access. If the Timer/Counter0 is written and a clock source is present, the Timer/Counter0 continues counting in the clock cycle following the write operation.

ıe 16-Bit Timer/Counter1

ɟure 31 shows the block diagram for Timer/Counter1.

ɟure 31. Timer/Counter1 Block Diagram



ə 16-bit Timer/Counter1 can select clock source from , prescaled CK, or an external pin. In addition it can be ɔpped as described in the specification for the ner/Counter1 Control Registers - TCCR1A and CR1B. The different status flags (overflow, compare ıtch and capture event) and control signals are found in Timer/Counter1 Control Registers - TCCR1A and CR1B. The interrupt enable/disable settings for ıer/Counter1 are found in the Timer/Counter Interrupt sk Register - TIMSK.

ıen Timer/Counter1 is externally clocked, the external nal is synchronized with the oscillator frequency of the U. To assure proper sampling of the external clock, the ıimum time between two external clock transitions must at least one internal CPU clock period. The external ck signal is sampled on the rising edge of the internal U clock.

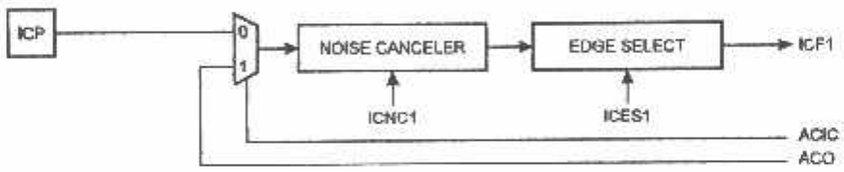
ə 16-bit Timer/Counter1 features both a high resolution d a high accuracy usage with the lower prescaling oppor- ıities. Similarly, the high prescaling opportunities makes Timer/Counter1 useful for lower speed functions or act timing functions with infrequent actions.

The Timer/Counter1 supports two Output Compare functions using the Output Compare Register 1 A and B - OCR1A and OCR1B as the data sources to be compared to the Timer/Counter1 contents. The Output Compare functions include optional clearing of the counter on compareA match, and actions on the Output Compare pins on both compare matches.

Timer/Counter1 can also be used as a 8, 9 or 10-bit Pulse With Modulator. In this mode the counter and the OCR1A/OCR1B registers serve as a dual glitch-free standalone PWM with centered pulses. Refer to page 30 for a detailed description on this function.

The Input Capture function of Timer/Counter1 provides a capture of the Timer/Counter1 contents to the Input Capture Register - ICR1, triggered by an external event on the Input Capture Pin - ICP. The actual capture event settings are defined by the Timer/Counter1 Control Register - TCCR1B. In addition, the Analog Comparator can be set to trigger the Input Capture. Refer to the section, "The Analog Comparator", for details on this. The ICP pin logic is shown in Figure 32.

ɟure 32. ICP Pin Schematic Diagram



ACIC: COMPARATOR IC ENABLE
ACO: COMPARATOR OUTPUT

he noise canceler function is enabled, the actual trigger ıdition for the capture event is monitored over 4 samples before the capture is activated. The input pin signal is sampled at XTAL clock frequency.

ə Timer/Counter1 Control Register A - TCCR1A

	7	6	5	4	3	2	1	0	
F ($4F)	COM1A1	COM1A0	COM1B1	COM1B0	-	-	PWM11	PWM10	TCCR1A
ıad/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W	
tial value	0	0	0	0	0	0	0	0	

ɨits 7,6 - COM1A1, COM1A0: Compare Output Mode1A, ɨits 1 and 0

ə COM1A1 and COM1A0 control bits determine any out- t pin action following a compare match in ıer/Counter1. Any output pin actions affect pin OC1A - tput CompareA pin 1. Since this is an alternative func- ı to an I/O port, the corresponding direction control bit st be set (one) to control an output pin. The control con- ıration is shown in Table 10.

- **Bits 5,4 - COM1B1, COM1B0: Compare Output Mode1B, bits 1 and 0**

The COM1B1 and COM1B0 control bits determine any output pin action following a compare match in Timer/Counter1. Any output pin actions affect pin OC1B - Output CompareB. Since this is an alternative function to an I/O port, the corresponding direction control bit must be set (one) to control an output pin. The following control configuration is given:

ble 11. Compare 1 Mode Select

COM1X1	COM1X0	Description
0	0	Timer/Counter1 disconnected from output pin OC1X
0	1	Toggle the OC1X output line.
1	0	Clear the OC1X output line (to zero).
1	1	Set the OC1X output line (to one).

e: X = A or B.

PWM mode, these bits have a different function. Refer to ble 15 for a detailed description. When changing the M1X1/COM1X0 bits, Output Compare Interrupts 1 must disabled by clearing their Interrupt Enable bits in the TIMSK Register. Otherwise an interrupt can occur when the bits are changed.

- **Bits 3..2 - Res: Reserved bits**

These bits are reserved bits in the AT90S4434/8535 and always read zero.

- **Bits 1..0 - PWM11, PWM10: Pulse Width Modulator Select Bits**

These bits select PWM operation of Timer/Counter1 as specified in Table 12. This mode is described on page 30.

Table 12. PWM Mode Select

PWM11	PWM10	Description
0	0	PWM operation of Timer/Counter1 is disabled
0	1	Timer/Counter1 is an 8-bit PWM
1	0	Timer/Counter1 is a 9-bit PWM
1	1	Timer/Counter1 is a 10-bit PWM

e Timer/Counter1 Control Register B - TCCR1B

t	7	6	5	4	3	2	1	0	
E ($4E)	ICNC1	ICES1	-	-	CTC1	CS12	CS11	CS10	TCCR1B
ead/Write	R/W	R/W	R	R	R/W	R/W	R/W	R/W	
itial value	0	0	0	0	0	0	0	0	

Bit 7 - ICNC1: Input Capture1 Noise Canceler (4 CKs)

hen the ICNC1 bit is cleared (zero), the input capture trig- r noise canceler function is disabled. The input capture is gered at the first rising/falling edge sampled on the ICP - ut capture pin - as specified. When the ICNC1 bit is set e), four successive samples are measures on the ICP - ut capture pin, and all samples must be high/low accord- to the input capture trigger specification in the ICES1 . The actual sampling frequency is XTAL clock fre- ency.

Bit 6 - ICES1: Input Capture1 Edge Select

ile the ICES1 bit is cleared (zero), the Timer/Counter1 ntents are transferred to the Input Capture Register - R1 - on the falling edge of the input capture pin - ICP. ile the ICES1 bit is set (one), the Timer/Counter1 con- ts are transferred to the Input Capture Register - ICR1 - the rising edge of the input capture pin - ICP.

Bits 5, 4 - Res: Reserved bits

ese bits are reserved bits in the AT90S4434/8535 and ays read zero.

Bit 3 - CTC1: Clear Timer/Counter1 on Compare Match

en the CTC1 control bit is set (one), the Timer/Counter1 eset to $0000 in the clock cycle after a compareA tch. If the CTC1 control bit is cleared, Timer/Counter1 ntinues counting and is unaffected by a compare match. ce the compare match is detected in the CPU clock cle following the match, this function will behave differ- ly when a prescaling higher than 1 is used for the timer. When a prescaling of 1 is used, and the compareA register is set to C, the timer will count as follows if CTC1 is set:

... | C-1 | C | C+1 | 0 | 1 |...

When the prescaler is set to divide by 8, the timer will count like this:

... | C-1, C-1, C-1, C-1, C-1, C-1, C-1, C-1 | C, C, C, C, C, C, C, C | C+1, 0, 0, 0, 0, 0, 0, 0, 0 |1,1,1,1,1,1,1,1|...

In PWM mode, this bit has no effect.

- **Bits 2,1,0 - CS12, CS11, CS10: Clock Select1, bit 2,1 and 0**

The Clock Select1 bits 2,1 and 0 define the prescaling source of Timer/Counter1.

Table 13. Clock 1 Prescale Select

CS12	CS11	CS10	Description
0	0	0	Stop, the Timer/Counter1 is stopped.
0	0	1	CK
0	1	0	CK / 8
0	1	1	CK / 64
1	0	0	CK / 256
1	0	1	CK / 1024
1	1	0	External Pin T1, falling edge
1	1	1	External Pin T1, rising edge

e Stop condition provides a Timer Enable/Disable func-
ı. The CK down divided modes are scaled directly from
CK oscillator clock. If the external pin modes are used,

e Timer/Counter1 - TCNT1H AND TCNT1L

	15	14	13	12	11	10	9	8	
D ($4D)	MSB								TCNT1H
C ($4C)								LSB	TCNT1L
	7	6	5	4	3	2	1	0	
ad/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ial value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

s 16-bit register contains the prescaled value of the 16-
Timer/Counter1. To ensure that both the high and low
es are read and written simultaneously when the CPU
esses these registers, the access is performed using an
it temporary register (TEMP). This temporary register is
o used when accessing OCR1A, OCR1B and ICR1. If
main program and also interrupt routines perform
ess to registers using TEMP, interrupts must be dis-
ed during access from the main program.

NT1 Timer/Counter1 Write:

When the CPU writes to the high byte TCNT1H, the written data is placed in the TEMP register. Next, when the CPU writes the low byte TCNT1L, this byte of data is combined with the byte data in the TEMP register, and all 16 bits are written to the TCNT1 Timer/Counter1 register simultaneously. Consequently, the high byte TCNT1H must be accessed first for a full 16-bit register write operation.

- **TCNT1 Timer/Counter1 Read:**

  When the CPU reads the low byte TCNT1L, the data of the low byte TCNT1L is sent to the CPU and the data of the high byte TCNT1H is placed in the TEMP register. When the CPU reads the data in the high byte TCNT1H, the CPU receives the data in the TEMP register. Consequently, the low byte TCNT1L must be accessed first for a full 16-bit register read operation.

The Timer/Counter1 is realized as an up or up/down (in PWM mode) counter with read and write access. If Timer/Counter1 is written to and a clock source is selected, the Timer/Counter1 continues counting in the timer clock cycle after it is preset with the written value.

ner/Counter1 Output Compare Register - OCR1AH AND OCR1AL

	15	14	13	12	11	10	9	8	
B ($4B)	MSB								OCR1AH
A ($4A)								LSB	OCR1AL
	7	6	5	4	3	2	1	0	
ad/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ial value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

ner/Counter1 Output Compare Register - OCR1BH AND OCR1BL

	15	14	13	12	11	10	9	8	
3 ($49)	MSB								OCR1BH
3 ($48)								LSB	OCR1BL
	7	6	5	4	3	2	1	0	
ad/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ial value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

e output compare registers are 16-bit read/write regis-
s.

e Timer/Counter1 Output Compare Registers contain data to be continuously compared with Timer/Counter1. Actions on compare matches are specified in the Timer/Counter1 Control and Status register. A compare match does only occur if Timer/Counter1 counts to the OCR value. A software write that sets TCNT1 and OCR1A

OCR1B to the same value does not generate a compare
itch.

:ompare match will set the compare interrupt flag in the
'U clock cycle following the compare event. Writing to
'RTD5 and PORTD4 sets the OC1A and OC1B values
respondingly.

ice the Output Compare Registers - OCR1A and
:R1B - are 16-bit registers, a temporary register TEMP is
ed when OCR1A/B are written to ensure that both bytes
updated simultaneously. When the CPU writes the high byte, OCR1AH or OCR1BH, the data is temporarily stored in the TEMP register. When the CPU writes the low byte, OCR1AL or OCR1BL, the TEMP register is simultaneously written to OCR1AH or OCR1BH. Consequently, the high byte OCR1AH or OCR1BH must be written first for a full 16-bit register write operation.

The TEMP register is also used when accessing TCNT1, and ICR1. If the main program and also interrupt routines perform access to registers using TEMP, interrupts must be disabled during access from the main program.

e Timer/Counter1 Input Capture Register - ICR1H AND ICR1L

	15	14	13	12	11	10	9	8	
7 ($47)	MSB								ICR1H
6 ($46)								LSB	ICR1L
	7	6	5	4	3	2	1	0	
ad/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
tial value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

e input capture register is a 16-bit read-only register.

ıen the rising or falling edge (according to the input cap-
e edge setting - ICES1) of the signal at the input capture
n - ICP - is detected, the current value of the
ner/Counter1 is transferred to the Input Capture Register
CR1. At the same time, the input capture flag - ICF1 - is
t (one).

ıce the Input Capture Register - ICR1 - is a 16-bit regis-
, a temporary register TEMP is used when ICR1 is read
ensure that both bytes are read simultaneously. When
: CPU reads the low byte ICR1L, the data is sent to the
'U and the data of the high byte ICR1H is placed in the
MP register. When the CPU reads the data in the high
e ICR1H, the CPU receives the data in the TEMP regis-
. Consequently, the low byte ICR1L must be accessed
t for a full 16-bit register read operation.

e TEMP register is also used when accessing TCNT1,
:R1A and OCR1B. If the main program and also interrupt routines perform access to registers using TEMP, interrupts must be disabled during access from the main program.

Timer/Counter1 In PWM Mode

When the PWM mode is selected, Timer/Counter1 and the Output Compare Register1A - OCR1A and the Output Compare Register1B - OCR1B, form a dual 8, 9 or 10-bit, free-running, glitch-free and phase correct PWM with outputs on the PD5(OC1A) and PD4(OC1B) pins. Timer/Counter1 acts as an up/down counter, counting up from $0000 to TOP (see Table 14), when it turns and counts down again to zero before the cycle is repeated. When the counter value matches the contents of the 10 least significant bits of OCR1A or OCR1B, the PD5(OC1A)/PD4(OC1B) pins are set or cleared according to the settings of the COM1A1/COM1A0 or COM1B1/COM1B0 bits in the Timer/Counter1 Control Register TCCR1A. Refer to Table 15 for details.

ole 14. Timer TOP Values and PWM Frequency

PWM Resolution	Timer TOP value	Frequency
8-bit	$00FF (255)	$f_{TC1}/510$
9-bit	$01FF (511)	$f_{TC1}/1022$
10-bit	$03FF(1023)	$f_{TC1}/2046$

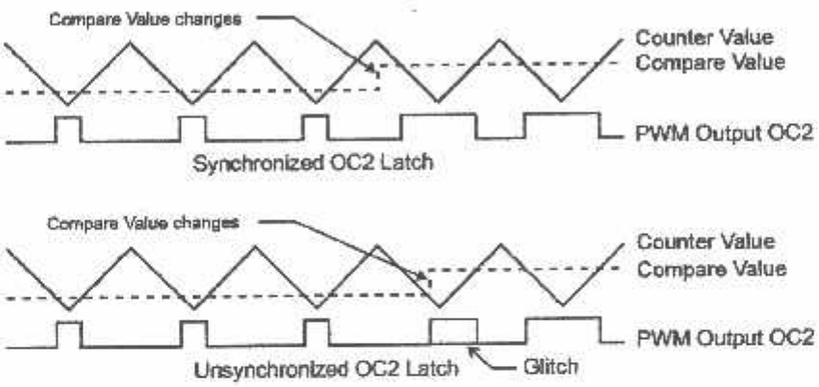
ble 15. Compare1 Mode Select in PWM Mode

OM1X1	COM1X0	Effect on OCX1
0	0	Not connected
0	1	Not connected
1	0	Cleared on compare match, upcounting. Set on compare match, downcounting (non-inverted PWM).
1	1	Cleared on compare match, downcounting. Set on compare match, upcounting (inverted PWM).

e: X = A or B

Note that in the PWM mode, the 10 least significant OCR1A/OCR1B bits, when written, are transferred to a temporary location. They are latched when Timer/Counter1 reaches the value TOP. This prevents the occurrence of odd-length PWM pulses (glitches) in the event of an unsynchronized OCR1A/OCR1B write. See Figure 33 for an example.

jure 33. Effects of Unsynchronized OCR1 Latching



ring the time between the write and the latch operation, ead from OCR1A or OCR1B will read the contents of the nporary location. This means that the most recently writ- value always will read out of OCR1A/B.

nen OCR1 contains $0000 or TOP, the output C1A/OC1B is held low or high according to the settings of)M1A1/COM1A0 or COM1B1/COM1B0. This is shown in ble 16.

ble 16. PWM Outputs OCR1X = $0000 or TOP

COM1X1	COM1X0	OCR1X	Output OC1X
1	0	$0000	L
1	0	TOP	H
1	1	$0000	H
1	1	TOP	L

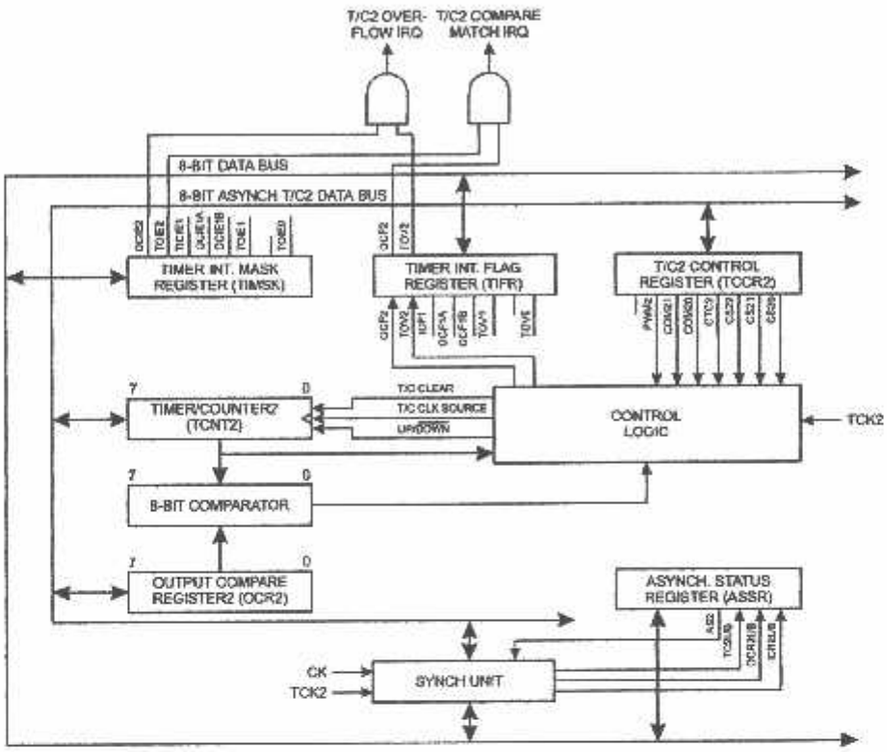
e: X = A

PWM mode, the Timer Overflow Flag1, TOV1, is set en the counter changes direction at $0000. Timer Over- w Interrupt1 operates exactly as in normal Timer/Counter de, i.e. it is executed when TOV1 is set provided that ner Overflow Interrupt1 and global interrupts are enabled. This does also apply to the Timer Output Compare1 flags and interrupts.

ıe 8-Bit Timer/Counter 2

ure 34 shows the block diagram for Timer/Counter2.

ıure 34. Timer/Counter2 Block Diagram



e 8-bit Timer/Counter2 can select clock source from K2 or prescaled TCK2. It can also be stopped as scribed in the specification for the Timer/Counter Control gister TCCR2.

e different status flags (overflow, compare match, and oture event) are found in the Timer/Counter Interrupt g Register - TIFR. Control signals are found in the ner/Counter Control Register TCCR2. The interrupt able/disable settings are found in the Timer/Counter errupt Mask Register - TIMSK.

s module features a high resolution and a high accuracy ige with the lower prescaling opportunities. Similarly, the h prescaling opportunities make this unit useful for lower speed functions or exact timing functions with infrequent actions.

The Timer/Counter supports an Output Compare function using the Output Compare Register OCR2 as the data source to be compared to the Timer/Counter contents. The Output Compare function includes optional clearing of the counter on compare match, and action on the Output Compare Pin - PD7(OC2) - on compare match. Writing to PORTD7 sets the OC2 value correspondingly.

Timer/Counter2 can also be used as an 8-bit Pulse Width Modulator. In this mode, Timer/Counter2 and the output compare register serve as a glitch-free, stand-alone PWM with centered pulses. Refer to page 35 for a detailed description on this function.

e Timer/Counter2 Control Register - TCCR2

t	7	6	5	4	3	2	1	0	
:5 ($45)	-	PWM2	COM21	COM20	CTC2	CS22	CS21	CS20	TCCR2
ead/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
itial value	0	0	0	0	0	0	0	0	

Bit 7 - Res: Reserved Bit
iis bit is a reserved bit in the AT90S4434/8535 and vays reads as zero.

Bit 6 - PWM2: Pulse Width Modulator Enable
hen set (one) this bit enables PWM mode for ner/Counter2. This mode is described on page 36.

Bits 5,4 - COM21, COM20: Compare Output Mode, bits 1 and 0
e COMn1 and COMn0 control bits determine any output action following a compare match in Timer/Counter2. itput pin actions affect pin PD7(OC2). Since this is an ernative function to an I/O port, the corresponding direc- control bit must be set (one) to control an output pin. e control configuration is shown in Table 17.

ble 17. Compare Mode Select

OM21	COM20	Description
0	0	Timer/Counter disconnected from output pin OC2
0	1	Toggle the OC2 output line.
1	0	Clear the OC2 output line (to zero).
1	1	Set the OC2 output line (to one).

te: In PWM mode, these bits have a different function. Refer to Table 19 for a detailed description.When changing the COM21/COM20 bits, the Output Compare 2 Interrupt must be disabled by clearing its Interrupt Enable bit in the TIMSK Register. Otherwise an interrupt can occur when the bits are changed.

Bit 3 - CTC2: Clear Timer/Counter on Compare Match
hen the CTC2 control bit is set (one), Timer/Counter2 is set to $00 in the CPU clock cycle after a compare match. he control bit is cleared, Timer/Counter2 continues unting and is unaffected by a compare match. Since the compare match is detected in the CPU clock cycle following the match, this function will behave differently when a prescaling higher than 1 is used for the timer. When a prescaling of 1 is used, and the compareA register is set to C, the timer will count as follows i CTC2 is set:

... | C-1 | C | C+1 | 0 | 1 |...

When the prescaler is set to divide by 8, the timer will count like this:

... | C-1, C-1, C-1, C-1, C-1, C-1, C-1, C-1 | C, C, C, C, C, C, C | C+1, 0, 0, 0, 0, 0, 0, 0, 0 | 1, 1, 1,...

In PWM mode, this bit has no effect.

- **Bits 2,1,0 - CS22, CS21, CS20: Clock Select bits 2,1 and 0**

The Clock Select bits 2,1 and 0 define the prescaling source of Timer/Counter2.

Table 18. Timer/Counter2 Prescale Select

CS22	CS21	CS20	Description
0	0	0	Timer/Counter2 is stopped.
0	0	1	TCK2
0	1	0	TCK 2/ 8
0	1	1	TCK 2/ 32
1	0	0	TCK 2/ 64
1	0	1	TCK2 / 128
1	1	0	TCK2 / 256
1	1	1	TCK2 / 1024

The Stop condition provides a Timer Enable/Disable function. The prescaled CK modes are scaled directly from the CK oscillator clock.

e Timer/Counter2 - TCNT2

t	7	6	5	4	3	2	1	0	
24 ($44)	MSB							LSB	TCNT2
ead/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
itial value	0	0	0	0	0	0	0	0	

s 8-bit register contains the value of Timer/Counter2.

ner/Counters2 is realized as an up or up/down (in PWM ode) counter with read and write access. If the Timer/Counter2 is written to and a clock source is selected, it continues counting in the timer clock cycle following the write operation.

ner/Counter2 Output Compare Register - OCR2

t	7	6	5	4	3	2	1	0	
23 ($43)	MSB							LSB	OCR2
ead/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
itial value	0	0	0	0	0	0	0	0	

e output compare register is an 8-bit read/write register. The Timer/Counter Output Compare Register contains the data to be continuously compared with Timer/Counter2.

ions on compare matches are specified in TCCR2. A npare match does only occur if Timer/Counter2 counts he OCR2 value. A software write that sets TCNT2 and :R2 to the same value does not generate a compare tch.

ompare match will set the compare interrupt flag in the U clock cycle following the compare event.

caution must be taken when Timer/Counter2 operates Asynchronous mode, i.e. the AS2 bit in ASSR is [one). When writing OCR2, the value is transferred to register on the TCK2 clock following the write opera-

ıer/Counter 2 in PWM mode

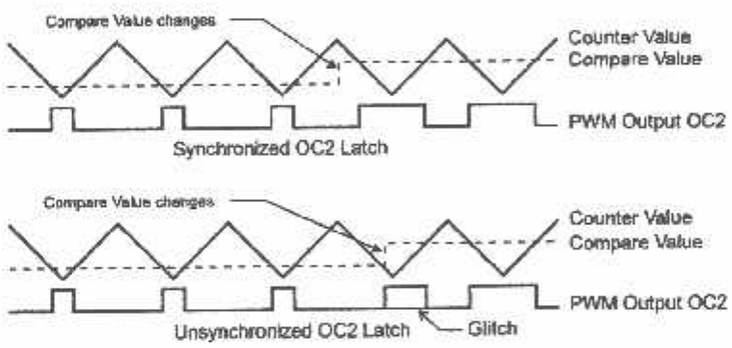
en the PWM mode is selected, Timer/Counter2 and the tput Compare Register - OCR2 form an 8-bit, free-run-g, glitch-free and phase correct PWM with outputs on PD7(OC2) pin. Timer/Counter2 acts as an up/down ınter, counting up from $00 to $FF, when it turns and ınts down again to zero before the cycle is repeated. ıen the counter value matches the contents of the Out-: Compare register, the PD7(OC2) pin is set or cleared :ording to the settings of the COM21/COM20 bits in the Timer/Counter2 Control Registers TCCR2. Refer to Table 19 for details.

Table 19. Compare Mode Select in PWM Mode

COMn1	COMn0	Effect on Compare Pin
0	0	Not connected
0	1	Not connected
1	0	Cleared on compare match, upcounting. Set on compare match, downcounting (non-inverted PWM).
1	1	Cleared on compare match, downcounting. Set on compare match, upcounting (inverted PWM).

Note that in PWM mode, the Output Compare register is transferred to a temporary location when written. The value is latched when the Timer/Counter reaches $FF. This prevents the occurrence of odd-length PWM pulses (glitches) in the event of an unsynchronized OCR2 write. See Figure 35 for an example.

ıure 35. Effects of Unsynchronized OCR Latching



ring the time between the write and the latch operation, ead from OCR2 will read the contents of the temporary ation. This means that the most recently written value ays will read out of OCR2.

When OCR2 contains $00 or $FF, the output PD7(OC2) is held low or high according to the settings of COM21/COM20. This is shown in Table 20.

ble 20. PWM Outputs OCR2 = $00 or $FF

COM21	COM20	OCR2	Output PWMn
1	0	$00	L
1	0	$FF	H
1	1	$00	H
1	1	$FF	L

PWM mode, the Timer Overflow Flag - TOV2, is set en the counter changes direction at $00. Timer Overflow errupt2 operates exactly as in normal Timer/Counter ıde, i.e. it is executed when TOV2 is set provided that ıer Overflow Interrupt and global interrupts are enabled. is does also apply to the Timer Output Compare flag and errupt.

e frequency of the PWM will be Timer Clock Frequency ided by 510.

ynchronous Operation of Timer/Counter2

ıen Timer/Counter2 operates asynchronously, some nsiderations must be taken.

Warning: When switching between asynchronous and synchronous clocking of Timer/Counter2, the timer registers; TCNT2, OCR2 and TCCR2 might get corrupted. A safe procedure for switching clock source is:

1. Disable the time 2 interrupts OCIE2 and TOIE2.
2. Select clock source by setting AS2 as appropriate.
3. Write new values to TCNT2, OCR2 and TCCR2.
4. To switch to asynchronous operation: Wait for TCN2UB, OCR2UB and TCR2UB.
5. Enable interrupts, if needed.

The oscillator is optimized for use with a 32,768 Hz watch crystal. An external clock signal applied to this pin goes through the same amplifier having a bandwidth of 256 kHz. The external clock signal should therefore be in the interval 0 Hz - 256 kHz. The frequency of the clock signal applied to the TOSC1 pin must be lower than one fourth of the CPU main clock frequency.

When writing to one of the registers TCNT2, OCR2, or TCCR2, the value is transferred to a temporary register, and latched after two positive edges on TOSC1. The user should not write a new value before the contents of the temporary register have been transferred to its destination. Each of the three mentioned registers have their individual temporary register, which means that e.g. writing to TCNT2 does not disturb an OCR2 write in progress. To detect that a transfer to the destination register has taken place, a Asynchronous Status Register - ASSR has been implemented.

- When entering a sleep mode after having written to TCNT2, OCR2 or TCCR2, the user must wait until the written register has been updated if Timer/Counter2 is used to wake up the device. Otherwise, the MCU will go to sleep before the changes have had any effect. This is extremely important if the Output Compare2 interrupt is used to wake up the device; Output compare is disabled during write to OCR2 or TCNT2. If the write cycle is not finished (i.e. the user goes to sleep before the OCR2UB bit returns to zero), the device will never get a compare match and the MCU will not wake up.
- If Timer/Counter2 is used to wake up the device from Power Save mode, precautions must be taken if the user wants to re-enter Power Save mode: The interrupt logic needs one TOSC1 cycle to be reset. If the time between wake up and re-entering Power Save mode is less than one TOSC1 cycle, the interrupt will not occur and the device will fail to wake up. If the user is in doubt whether the time before re-entering Power Save is sufficient, the following algorithm can be used to ensure that one TOSC1 cycle has elapsed:
  1. Write a value to TCCR2, TCNT2 or OCR2
  2. Wait until the corresponding Update Busy flag in ASSR returns to zero.
  3. Enter Power Save mode
- When asynchronous operation is selected, the 32 kHz oscillator for Timer/Counter2 is always running, except in power down mode. After a power up reset or wakeup from power down, the user should be aware of the fact that this oscillator might take as long as one second to stabilize. The user is advised to wait for at least one second before using Timer/Counter2 after power-up or wake-up from power down.
- Description of wake up from power save mode when the timer is clocked asynchronously: When the interrupt condition is met, the wake up process is started on the following cycle of the timer clock, that is, the timer is always advanced by at least one before the processor can read the counter value. The interrupt flags are updated 3 processor cycles after the processor clock has started. During these cycles, the processor executes instructions, but the interrupt condition is not readable, and the interrupt routine has not started yet.
- During asynchronous operation, the synchronization of the interrupt flags for the asynchronous timer takes 3 processor cycles plus one timer cycle. The timer is therefore advanced by at least one before the processor can read the timer value causing the setting of the interrupt flag. The output compare pin is changed on the timer clock and is not synchronized to the processor clock.

ynchronous Status Register - ASSR

t	7	6	5	4	3	2	1	0	
22 ($22)	-	-	-	-	AS2	TCN2UB	OCR2UB	TCR2UB	ASSR
ead/Write	R	R	R	R	R/W	R	R	R	
itial value	0	0	0	0	0	0	0	0	

Bit 7..4 - Res: Reserved Bits
ese bits are reserved bits in the AT90S4434/8535 and rays read as zero.

Bit 3 - AS2: Asynchronous Timer/Counter2
hen AS2 is set(one), Timer/Counter2 is clocked from the SC1 pin. Pins PC6 and PC7 become connected to a stal oscillator and cannot be used as general I/O pins. hen cleared (zero) Timer/Counter2 is clocked from the ernal system clock, CK. When the value of this bit is anged the contents of TCNT2, OCR2 and TCCR2 might corrupted.

Bit 2 - TCN2UB: Timer/Counter2 Update Busy
hen Timer/Counter2 operates asynchronously and :NT2 is written, this bit becomes set (one). When the ue written to TCNT2 has been updated from the tempo- y storage register, this bit is cleared (zero) by hardware. ogical zero in this bit indicates that TCNT2 is ready to be dated with a new value.

Bit 1 - OCR2UB: Output Compare Register2 Update Busy
hen Timer/Counter2 operates asynchronously and OCR2 written, this bit becomes set (one). When the value writ- n to OCR2 has been updated from the temporary storage gister, this bit is cleared (zero) by hardware. A logical ro in this bit indicates that OCR2 is ready to be updated h a new value.

Bit 0 - TCR2UB: Timer/Counter Control Register2 Update Busy
hen Timer/Counter2 operates asynchronously and CR2 is written, this bit becomes set (one). When the ue written to TCCR2 has been updated from the tempo- y storage register, this bit is cleared (zero) by hardware. ogical zero in this bit indicates that TCCR2 is ready to be dated with a new value.

write is performed to any of the three Timer/Counter2 isters while its update busy flag is set (one), the updated ue might get corrupted and cause an unintentional inter- t to occur.

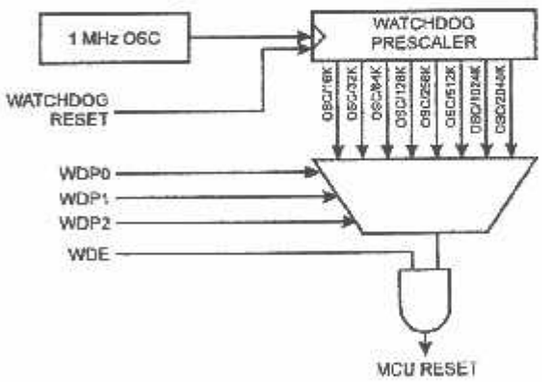
The mechanisms for reading TCNT2, OCR2, and TCCR2 are different. When reading TCNT2, the actual timer value is read. When reading OCR2 or TCCR2, the value in the temporary storage register is read.

The Watchdog Timer

The Watchdog Timer is clocked from a separate on-chip oscillator which runs at 1MHz This is the typical value at V_{CC} = 5V. See characterization data for typical values at other V_{CC} levels. By controlling the Watchdog Timer prescaler, the Watchdog reset interval can be adjusted from 16K to 2,048K cycles (nominally 16 - 2048 ms). The WDR - Watchdog Reset - instruction resets the Watchdog Timer. Eight different clock cycle periods can be selected to determine the reset period. If the reset period expires without another Watchdog reset, the AT90S4434/8535 resets and executes from the reset vector. For timing details on the Watchdog reset, refer to page 18.

To prevent unintentional disabling of the watchdog, a special turn-off sequence must be followed when the watchdog is disabled. Refer to the description of the Watchdog Timer Control Register for details.

Figure 36. Watchdog Timer



e Watchdog Timer Control Register - WDTCR

1 ($41)	7	6	5	4	3	2	1	0	
	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	WDTCR
ad/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
tial value	0	0	0	0	0	0	0	0	

Bits 7..5 - Res: Reserved bits
ese bits are reserved bits in the AT90S4434/8535 and always read as zero.

- **Bit 4 - WDTOE: Watch Dog Turn-Off Enable**
This bit must be set (one) when the WDE bit is cleared. Otherwise, the watchdog will not be disabled. Once set,

ardware will clear this bit to zero after four clock cycles. efer to the description of the WDE bit for a watchdog dis- ble procedure.

Bit 3 - WDE: Watch Dog Enable

'hen the WDE is set (one) the Watchdog Timer is abled, and if the WDE is cleared (zero) the Watchdog mer function is disabled. WDE can only be cleared if the 'DTOE bit is set(one). To disable an enabled watchdog ner, the following procedure must be followed:

In the same operation, write a logical one to WDTOE and WDE. A logical one must be written to WDE even though it is set to one before the disable operation starts.

2. Within the next four clock cycles, write a logical 0 to WDE. This disables the watchdog.

- **Bits 2..0 - WDP2, WDP1, WDP0: Watch Dog Timer Prescaler 2, 1 and 0**

The WDP2, WDP1, and WDP0 bits determine the Watchdog Timer prescaling when the Watchdog Timer is enabled. The different prescaling values and their corresponding Timeout Periods are shown in Table 21.

ible 21. Watch Dog Timer Prescale Select

WDP2	WDP1	WDP0	Timeout Period
0	0	0	16K cycles
0	0	1	32K cycles
0	1	0	64K cycles
0	1	1	128K cycles
1	0	0	256K cycles
1	0	1	512K cycles
1	1	0	1,024K cycles
1	1	1	2,048K cycles

EEPROM Read/Write Access

ne EEPROM access registers are accessible in the I/O ace.

ne write access time is in the range of 2.5 - 4ms, depend- g on the V_{CC} voltages. A self-timing function lets the user ftware detect when the next byte can be written. A spe- al EEPROM Ready interrupt can be set to trigger when e EEPROM is ready to accept new data.

In order to prevent unintentional EEPROM writes, a specific write procedure must be followed. Refer to the description of the EEPROM Control Register for details on this.

When the EEPROM is read or written, the CPU is halted for two clock cycles before the next instruction is executed.

ie EEPROM Address Register - EEARH and EEARL

it	15	14	13	12	11	10	9	8	
IF ($3F)	-	-	-	-	-	-	-	EEAR8	EEARH
IE ($3E)	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	EEARL
	7	6	5	4	3	2	1	0	
ead/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
itial value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

e EEPROM Address Registers - EEARH and EEARL ecify the EEPROM address in the 256/512 bytes EEPROM space. The EEPROM data bytes are addressed linearly between 0 and 255/511.

e EEPROM Data Register - EEDR

	7	6	5	4	3	2	1	0	
D ($3D)	MSB							LSB	EEDR
ead/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
tial value	0	0	0	0	0	0	0	0	

Bits 7..0 - EEDR7.0: EEPROM Data

r the EEPROM write operation, the EEDR register con- ns the data to be written to the EEPROM in the address given by the EEAR register. For the EEPROM read operation, the EEDR contains the data read out from the EEPROM at the address given by EEAR.

e EEPROM Control Register - EECR

	7	6	5	4	3	2	1	0	
C ($3C)	-	-	-	-	EERIE	EEMWE	EEWE	EERE	EECR
ead/Write	R	R	R	R	R/W	R/W	R/W	R/W	
tial value	0	0	0	0	0	0	0	0	

Bit 7..4 - Res: Reserved bits

ese bits are reserved bits in the AT90S4434/8535 and l always read as zero.

Bit 3 - EERIE: EEPROM Ready Interrupt Enable

hen the I bit in SREG and EERIE are set (one), the EPROM Ready Interrupt is enabled. When cleared (zero), e interrupt is disabled. The EEPROM Ready Interrupt nerates a constant interrupt when EEWE is cleared ero).

Bit 2 - EEMWE: EEPROM Master Write Enable

ie EEMWE bit determines whether setting EEWE to one uses the EEPROM to be written. When EEMWE is t(one) setting EEWE will write data to the EEPROM at e selected address If EEMWE is zero, setting EEWE will ve no effect. When EEMWE has been set (one) by soft- re, hardware clears the bit to zero after four clock cycles. e the description of the EEWE bit for a EEPROM write ocedure.

Bit 1 - EEWE: EEPROM Write Enable

e EEPROM Write Enable Signal EEWE is the write obe to the EEPROM. When address and data are cor- tly set up, the EEWE bit must be set to write the value o the EEPROM. The EEMWE bit must be set when the ical one is written to EEWE, otherwise no EEPROM te takes place. The following procedure should be fol- ed when writing the EEPROM (the order of steps 2 and s unessential):

1. Wait until EEWE becomes zero.
2. Write new EEPROM address to EEARL and EEARH (optional).
3. Write new EEPROM data to EEDR (optional).
4. Write a logical one to the EEMWE bit in EECR.
5. Within four clock cycles after setting EEMWE, write a logical one to EEWE.

When the write access time (typically 2.5 ms at V_{CC} = 5V or 4 ms at V_{CC} = 2.7V) has elapsed, the EEWE bit is cleared (zero) by hardware. The user software can poll this bit and wait for a zero before writing the next byte. When EEWE has been set, the CPU is halted for two cycles before the next instruction is executed.

• Bit 0 - EERE: EEPROM Read Enable

The EEPROM Read Enable Signal EERE is the read strobe to the EEPROM. When the correct address is set up in the EEAR register, the EERE bit must be set. When the EERE bit is cleared (zero) by hardware, requested data is found in the EEDR register. The EEPROM read access takes one instruction and there is no need to poll the EERE bit. When EERE has been set, the CPU is halted for four cycles before the next instruction is executed.

The user should poll the EEWE bit before starting the read operation. If a write operation is in progress when new data or address is written to the EEPROM I/O registers, the write operation will be interrupted, and the result is undefined.

Prevent EEPROM Corruption

During periods of low V_{CC}, the EEPROM data can be corrupted because the supply voltage is too low for the CPU and the EEPROM to operate properly. These issues are the same as for board level systems using the EEPROM, and the same design solutions should be applied.

An EEPROM data corruption can be caused by two situations when the voltage is too low. First, a regular write sequence to the EEPROM requires a minimum voltage to operate correctly. Secondly, the CPU itself can execute instructions incorrectly, if the supply voltage for executing instructions is too low.

EEPROM data corruption can easily be avoided by following these design recommendations (one is sufficient):

Keep the AVR RESET active (low) during periods of insufficient power supply voltage. This is best done by an external low V_{CC} Reset Protection circuit, often referred to as a Brown-Out Detector (BOD). Please refer to application notes AVR 190 and AVR 180 for design considerations regarding power-on reset and low voltage detection.

Keep the AVR core in Power Down Sleep Mode during periods of low V_{CC}. This will prevent the CPU from attempting to decode and execute instructions, effectively protecting the EEPROM registers from unintentional writes.

3. Store constants in Flash memory if the ability to change memory contents from software is not required. Flash memory can not be updated by the CPU, and will not be subject to corruption.

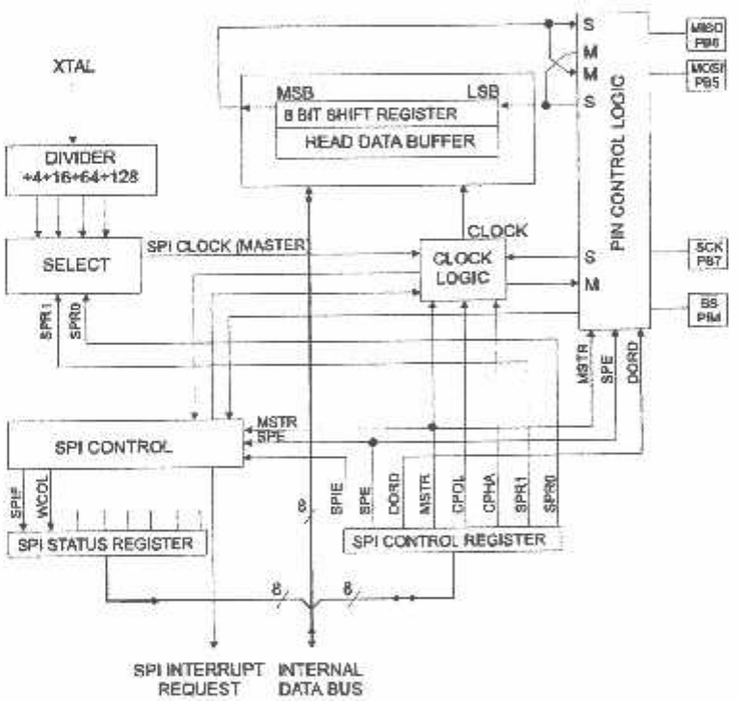
ıe Serial Peripheral Interface - SPI

ɜ Serial Peripheral Interface (SPI) allows high-speed ıchronous data transfer between the AT90S4434/8535 d peripheral devices or between several 90S4434/8535 devices. The AT90S4434/8535 SPI fea-ɜs include the following:

Full-Duplex, 3-Wire Synchronous Data Transfer

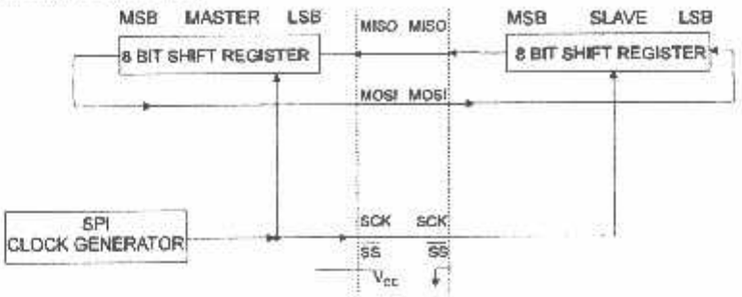
- Master or Slave Operation
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode

ɟure 37. SPI Block Diagram



ɜ interconnection between master and slave CPUs with I is shown in Figure 38. The PB7(SCK) pin is the clock put in the Master mode and is the clock input in the ve mode. Writing to the SPI Data Register of the master U starts the SPI clock generator, and the data written fts out of the PB5(MOSI) pin and into the PB5(MOSI) pin he slave CPU. After shifting one byte, the SPI clock gen-tor stops, setting the end of transmission flag (SPIF). If SPI interrupt enable bit (SPIE) in the SPCR register is set, an interrupt is requested. The Slave Select input, PB4($\overline{SS}$), is set low to select an individual SPI device as a slave. The two shift registers in the Master and the Slave can be considered as one distributed 16-bit circular shift register. This is shown in Figure 38. When data is shifted from the master to the slave, data is also shifted in the opposite direction, simultaneously. During one shift cycle, data in the master and the slave is interchanged.

ure 38. SPI Master-Slave Interconnection



e system is single buffered in the transmit direction and uble buffered in the receive direction. This means that aracters to be transmitted cannot be written to the SPI ta Register before the entire shift cycle is completed. ıen receiving data, however, a received character must read from the SPI Data Register before the next charac- has been completely shifted in. Otherwise, the first char- ter is lost.

hen the SPI is enabled, the data direction of the MOSI, SO, SCK and $\overline{SS}$ pins is overridden according to the fol- wing table:

ble 22. SPI Pin Overrides

Pin	Direction, Master SPI	Direction, Slave SPI
MOSI	User Defined	Input
MISO	Input	User Defined
SCK	User Defined	Input
$\overline{SS}$	User Defined	Input

$\overline{S}$ Pin Functionality

ıen the SPI is configured as a master (MSTR in SPCR is t), the user can determine the direction of the $\overline{SS}$ pin. If $\overline{S}$ is configured as an output, the pin is a general output ı which does not affect the SPI system. If $\overline{SS}$ is config- ed as an input, it must be held high to ensure Master SPI eration. If, in master mode, the $\overline{SS}$ pin is input, and is driven low by peripheral circuitry, the SPI system interprets this as another master selecting the SPI as a slave and starting to send data to it. To avoid bus contention, the SPI system takes the following actions:

1. The MSTR bit in SPCR is cleared and the SPI system becomes a slave. As a result of the SPI becoming a slave, the MOSI and SCK pins become inputs.
2. The SPIF flag in SPSR is set, and if the SPI interrupt is enabled, the interrupt routine will be executed.

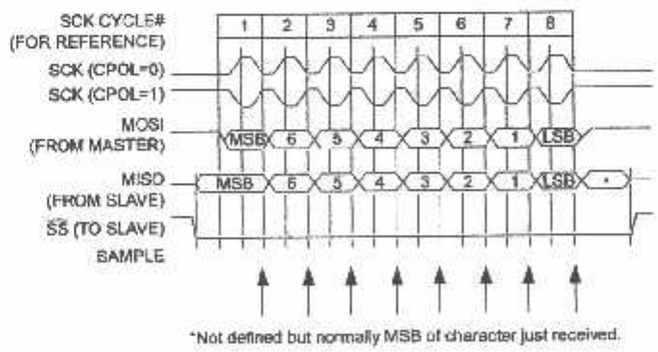
Thus, when interrupt-driven SPI transmission is used in master mode, and there exists a possibility that $\overline{SS}$ is driven low, the interrupt should always check that the MSTR bit is still set. Once the MSTR bit has been cleared by a slave select, it must be set by the user.

When the SPI is configured as a slave, the $\overline{SS}$ pin is always input. When $\overline{SS}$ is held low, the SPI is activated and MISO becomes an output if configured so by the user. All other pins are inputs. When $\overline{SS}$ is driven high, all pins are inputs, and the SPI is passive, which means that it will not receive incoming data.

Data Modes

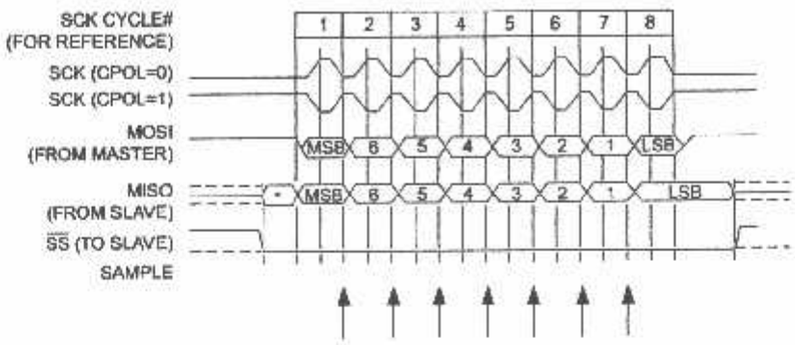
There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 39 and Figure 40.

ure 39. SPI Transfer Format with CPHA = 0



*Not defined but normally MSB of character just received.

ıure 40. SPI Transfer Format with CPHA = 1



*Not defined but normally LSB of previously transmitted character.

e SPI Control Register - SPCR

t	7	6	5	4	3	2	1	0	
ID ($2D)	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
ssd/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
itial value	0	0	0	0	0	0	0	0	

3it 7 - SPIE: SPI Interrupt Enable
is bit causes setting of the SPIF bit in the SPSR register execute the SPI interrupt provided that global interrupts e enabled.

Bit 6 - SPE: SPI Enable
nen the SPE bit is set (one), the SPI is enabled. This bit ust be set to enable any SPI operations.

3it 5 - DORD: Data Order
nen the DORD bit is set (one), the LSB of the data word ransmitted first.

nen the DORD bit is cleared (zero), the MSB of the data rd is transmitted first.

3it 4 - MSTR: Master/Slave Select
is bit selects Master SPI mode when set (one), and ive SPI mode when cleared (zero). If $\overline{SS}$ is configured as input and is driven low while MSTR is set, MSTR will be ared, and SPIF in SPSR will become set. The user will n have to set MSTR to re-enable SPI master mode.

- **Bit 3 - CPOL: Clock Polarity**

When this bit is set (one), SCK is high when idle. When CPOL is cleared (zero), SCK is low when idle. Refer to Figure 40 and Figure 41 for additional information.

- **Bit 2 - CPHA: Clock Phase**

Refer to Figure 40 or Figure 41 for the functionality of this bit.

- **Bits 1,0 - SPR1, SPR0: SPI Clock Rate Select 1 and 0**

These two bits control the SCK rate of the device configured as a master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the Oscillator Clock frequency f_{cl} is shown in the following table:

Table 23. Relationship Between SCK and the Oscillator Frequency

SPR1	SPR0	SCK Frequency
0	0	f_{cl} / 4
0	1	f_{cl} / 16
1	0	f_{cl} / 64
1	1	f_{cl} / 128

e SPI Status Register - SPSR

	7	6	5	4	3	2	1	0	
E ($2E)	SPIF	WCOL	-	-	-	-	-	-	SPSR
ad/Write	R	R	R	R	R	R	R	R	
tial value	0	0	0	0	0	0	0	0	

3it 7 - SPIF: SPI Interrupt Flag
ıen a serial transfer is complete, the SPIF bit is set (one) d an interrupt is generated if SPIE in SPCR is set (one) d global interrupts are enabled. If $\overline{SS}$ is an input and is driven low when the SPI is in master mode, this will also set the SPIF flag. SPIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, the SPIF bit is cleared by first reading the SPI status regis-

with SPIF set (one), then accessing the SPI Data Register (SPDR).

Bit 6 - WCOL: Write Collision flag

The WCOL bit is set if the SPI data register (SPDR) is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to SPDR will have no effect. The WCOL bit (and the SPIF bit) are cleared (zero) by first reading the SPI Status Register with WCOL set (one), and then accessing the SPI Data Register.

- **Bit 5..0 - Res: Reserved bits**

These bits are reserved bits in the AT90S4434/8535 and will always read as zero.

The SPI interface on the AT90S4434/8535 is also used for program memory and EEPROM downloading or uploading. See page 71 for serial programming and verification.

The SPI Data Register - SPDR

	7	6	5	4	3	2	1	0	
F ($2F)	MSB							LSB	SPDR
ead/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
tial value	0	0	0	0	0	0	0	0	

The SPI Data Register is a read/write register used for data transfer between the register file and the SPI Shift register. Writing to the register initiates data transmission. Reading the register causes the Shift Register Receive buffer to be read.

The UART

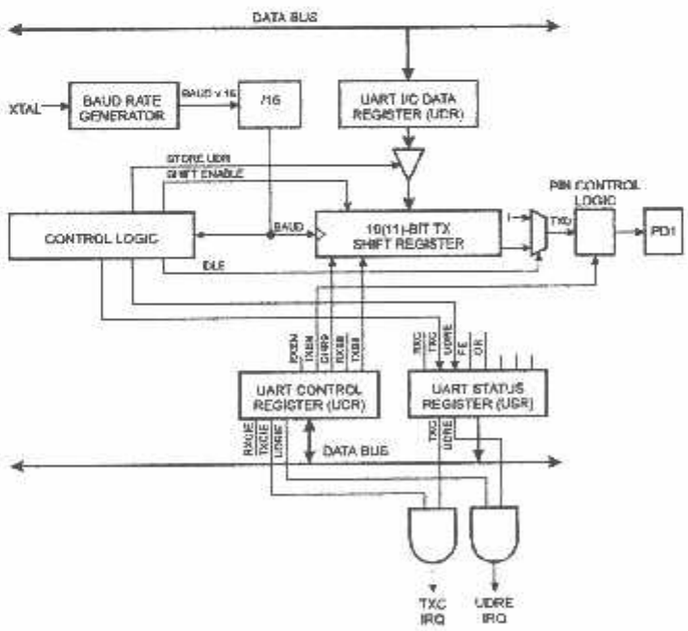
The AT90S4434/8535 features a full duplex Universal Asynchronous Receiver and Transmitter (UART). The main features are:

- Baud rate generator generates any baud rate
- High baud rates at low XTAL frequencies
- 8 or 9 bits data
- Noise filtering
- Overrun detection
- Framing Error detection
- False Start Bit detection
- Three separate interrupts on TX Complete, TX Data Register Empty and RX Complete
- Buffered Transmit and Receive.

Data Transmission

A block schematic of the UART transmitter is shown in Figure 41.

Figure 41. UART Transmitter



ıta transmission is initiated by writing the data to be nsmitted to the UART I/O Data Register, UDR. Data is nsferred from UDR to the Transmit shift register when:

A new character has been written to UDR after the stop bit from the previous character has been shifted out. The shift register is loaded immediately.

A new character has been written to UDR before the stop ɔit from the previous character has been shifted out. The shift register is loaded when the stop bit of the character currently being transmitted has been shifted out.

he 10(11)-bit Transmitter shift register is empty or when, ta is transferred from UDR to the shift register. At this ie the UDRE (UART Data Register Empty) bit in the ART Status Register, USR, is set. When this bit is set ie), the UART is ready to receive the next character. At same time as the data is transferred from UDR to the (11)-bit shift register, bit 0 of the shift register is cleared art bit) and bit 9 or 10 is set (stop bit). If 9 bit data word is lected (the CHR9 bit in the UART Control Register, UCR set), the TXB8 bit in UCR is transferred to bit 9 in the ansmit shift register.

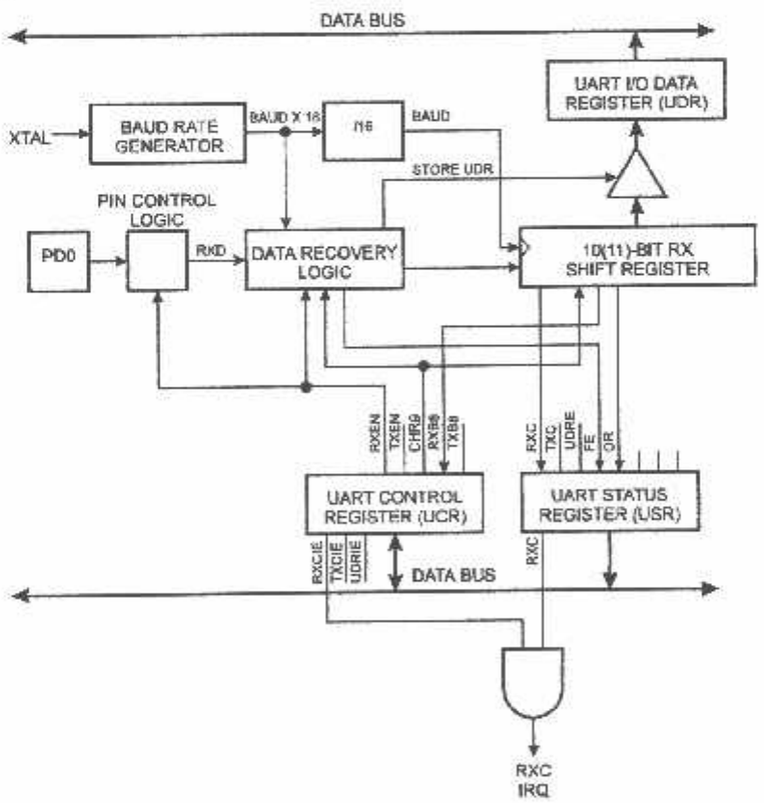
On the Baud Rate clock following the transfer operation to the shift register, the start bit is shifted out on the TXD pin. Then follows the data, LSB first. When the stop bit has been shifted out, the shift register is loaded if any new data has been written to the UDR during the transmission. During loading, UDRE is set. If there is no new data in the UDR register to send when the stop bit is shifted out, the UDRE flag will remain set until UDR is written again. When no new data has been written, and the stop bit has been present on TXD for one bit length, the TX Complete Flag, TXC, in USR is set.

The TXEN bit in UCR enables the UART transmitter when set (one). When this bit is cleared (zero), the PD1 pin can be used for general I/O. When TXEN is set, the UART Transmitter will be connected to PD1, which is forced to be an output pin regardless of the setting of the DDD1 bit in DDRD.

Data Reception

Figure 42 shows a block diagram of the UART Receiver.

gure 42. UART Receiver

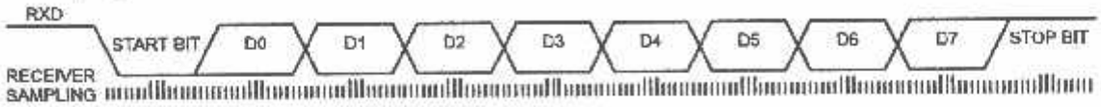


e receiver front-end logic samples the signal on the RXD i at a frequency 16 times the baud rate. While the line is e, one single sample of logical zero will be interpreted as the falling edge of a start bit, and the start bit detection sequence is initiated. Let sample 1 denote the first zero-sample. Following the 1 to 0-transition, the receiver sam-

s the RXD pin at samples 8, 9 and 10. If two or more of se three samples are found to be logical ones, the start is rejected as a noise spike and the receiver starts look- for the next 1 to 0-transition.

owever, a valid start bit is detected, sampling of the data following the start bit is performed. These bits are also sampled at samples 8, 9 and 10. The logical value found in at least two of the three samples is taken as the bit value. All bits are shifted into the transmitter shift register as they are sampled. Sampling of an incoming character is shown in Figure 43.

ure 43. Sampling Received Data



en the stop bit enters the receiver, the majority of the e samples must be one to accept the stop bit. If two or re samples are logical zeros, the Framing Error (FE) flag he UART Status Register (USR) is set. Before reading UDR register, the user should always check the FE bit detect Framing Errors.

ether or not a valid stop bit is detected at the end of a aracter reception cycle, the data is transferred to UDR the RXC flag in USR is set. UDR is in fact two physi- ly separate registers, one for transmitted data and one received data. When UDR is read, the Receive Data gister is accessed, and when UDR is written, the Trans- t Data register is accessed. If 9 bit data word is selected e CHR9 bit in the UART Control Register, UCR is set), RXB8 bit in UCR is loaded with bit 9 in the Transmit ft register when data is transferred to UDR.

If, after having received a character, the UDR register has not been read since the last receive, the OverRun (OR) flag in UCR is set. This means that the last data byte shifted into to the shift register could not be transferred to UDR and has been lost. The OR bit is buffered, and is updated when the valid data byte in UDR is read. Thus, the user should always check the OR bit after reading the UDR reg- ister in order to detect any overruns.

When the RXEN bit in the UCR register is cleared (zero), the receiver is disabled. This means that the PD0 pin can be used as a general I/O pin. When RXEN is set, the UART Receiver will be connected to PD0, which is forced to be an input pin regardless of the setting of the DDD0 bit in DDRD. When PD0 is forced to input by the UART, the PORTD0 bit can still be used to control the pull-up resistor on the pin.

RT Control

e UART I/O Data Register - UDR

	7	6	5	4	3	2	1	0	
C ($2C)	MSB							LSB	UDR
ad/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
tial value	0	0	0	0	0	0	0	0	

e UDR register is actually two physically separate regis- s sharing the same I/O address. When writing to the reg- er, the UART Transmit Data register is written. When reading from UDR, the UART Receive Data register is read.

e UART Status Register - USR

	7	6	5	4	3	2	1	0	
B ($2B)	RXC	TXC	UDRE	FE	OR	-	-	-	USR
ad/Write	R	R/W	R	R	R	R	R	R	
tial value	0	0	1	0	0	0	0	0	

e USR register is a read-only register providing informa- n on the UART Status.

it 7 - RXC: UART Receive Complete

s bit is set (one) when a received character is trans- ed from the Receiver Shift register to UDR. The bit is regardless of any detected framing errors. When the CIE bit in UCR is set, the UART Receive Complete errupt will be executed when RXC is set(one). RXC is ared by reading UDR. When interrupt-driven data recep- tion is used, the UART Receive Complete Interrupt routine must read UDR in order to clear RXC, otherwise a new interrupt will occur once the interrupt routine terminates.

• Bit 6 - TXC: UART Transmit Complete

This bit is set (one) when the entire character (including the stop bit) in the Transmit Shift register has been shifted out and no new data has been written to UDR. This flag is especially useful in half-duplex communications interfaces, where a transmitting application must enter receive mode

d free the communications bus immediately after com-
ıting the transmission.

ıen the TXCIE bit in UCR is set, setting of TXC causes
ı UART Transmit Complete interrupt to be executed.
:C is cleared by hardware when executing the corre-
onding interrupt handling vector. Alternatively, the TXC
is cleared (zero) by writing a logical one to the bit.

3it 5 - UDRE: UART Data Register Empty
is bit is set (one) when a character written to UDR is
nsferred to the Transmit shift register. Setting of this bit
licates that the transmitter is ready to receive a new
aracter for transmission.

ıen the UDRIE bit in UCR is set, the UART Transmit
mplete interrupt to be executed as long as UDRE is set.
)RE is cleared by writing UDR. When interrupt-driven
ta transmission is used, the UART Data Register Empty
errupt routine must write UDR in order to clear UDRE,
ıerwise a new interrupt will occur once the interrupt rou-
e terminates.

ıe UART Control Register - UCR

lt	7	6	5	4	3	2	1	0	
)A ($2A)	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8	UCR
ead/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	W	
itial value	0	0	0	0	0	0	0	0	

Bit 7 - RXCIE: RX Complete Interrupt Enable
hen this bit is set (one), a setting of the RXC bit in USR
ll cause the Receive Complete interrupt routine to be
ecuted provided that global interrupts are enabled.

3it 6 - TXCIE: TX Complete Interrupt Enable
ıen this bit is set (one), a setting of the TXC bit in USR
l cause the Transmit Complete interrupt routine to be
ecuted provided that global interrupts are enabled.

3it 5 - UDRIE: UART Data Register Empty Interrupt Enable
ıen this bit is set (one), a setting of the UDRE bit in USR
cause the UART Data Register Empty interrupt routine
ɔe executed provided that global interrupts are enabled.

3it 4 - RXEN: Receiver Enable
s bit enables the UART receiver when set (one). When
ı receiver is disabled, the TXC, OR and FE status flags
ıot become set. If these flags are set, turning off RXEN
es not cause them to be cleared.

3it 3 - TXEN: Transmitter Enable
is bit enables the UART transmitter when set (one).
ıen disabling the transmitter while transmitting a charac-
, the transmitter is not disabled before the character in
shift register plus any following character in UDR has
en completely transmitted.

3it 2 - CHR9: 9 Bit Characters
ıen this bit is set (one) transmitted and received charac-
s are 9 bit long plus start and stop bits. The 9th bit is
ıd and written by using the RXB8 and TXB8 bits in UCR,
UDRE is set (one) during reset to indicate that the transmitter is ready.

- **Bit 4 - FE: Framing Error**

This bit is set if a Framing Error condition is detected, i.e. when the stop bit of an incoming character is zero.

The FE bit is cleared when the stop bit of received data is one.

- **Bit 3 - OR: OverRun**

This bit is set if an Overrun condition is detected, i.e. when a character already present in the UDR register is not read before the next character has been shifted into the Receiver Shift register. The OR bit is buffered, which means that it will be set once the valid data still in UDR is read.

The OR bit is cleared (zero) when data is received and transferred to UDR.

- **Bits 2..0 - Res: Reserved bits**

These bits are reserved bits in the AT90S4434/8535 and will always read as zero.

respectively. The 9th data bit can be used as an extra stop bit or a parity bit.

- **Bit 1 - RXB8: Receive Data Bit 8**

When CHR9 is set (one), RXB8 is the 9th data bit of the received character.

- **Bit 0 - TXB8: Transmit Data Bit 8**

When CHR9 is set (one), TXB8 is the 9th data bit in the character to be transmitted.

The Baud Rate Generator

The baud rate generator is a frequency divider which generates baud-rates according to the following equation:

$$BAUD = \frac{f_{CK}}{16(UBRR + 1)}$$

- BAUD = Baud-Rate
- f_{CK}= Crystal Clock frequency
- UBRR = Contents of the UART Baud Rate register, UBRR (0-255)

For standard crystal frequencies, the most commonly used baud rates can be generated by using the UBRR settings in Table 24. UBRR values which yield an actual baud rate differing less than 2% from the target baud rate, are bold in the table.

ble 24. UBRR Settings at Various Crystal Frequencies (Examples)

Baud Rate	1 MHz		%Error	1.8432 MHz		%Error	2 MHz		%Error	2.4576 MHz		%Error
2400	UBRR=	25	0.2	UBRR=	47	0.0	UBRR=	51	0.2	UBRR=	63	0.0
4800	UBRR=	12	0.2	UBRR=	23	0.0	UBRR=	25	0.2	UBRR=	31	0.0
9600	UBRR=	6	7.5	UBRR=	11	0.0	UBRR=	12	0.2	UBRR=	15	0.0
14400	UBRR=	3	7.8	UBRR=	7	0.0	UBRR=	8	3.7	UBRR=	10	3.1
19200	UBRR=	2	7.8	UBRR=	5	0.0	UBRR=	6	7.5	UBRR=	7	0.0
28800	UBRR=	1	7.8	UBRR=	3	0.0	UBRR=	3	7.8	UBRR=	4	6.3
38400	UBRR=	1	22.9	UBRR=	2	0.0	UBRR=	2	7.8	UBRR=	3	0.0
57600	UBRR=	0	7.8	UBRR=	1	0.0	UBRR=	1	7.8	UBRR=	2	12.5
76800	UBRR=	0	22.9	UBRR=	1	33.3	UBRR=	1	22.9	UBRR=	1	0.0
115200	UBRR=	0	84.3	UBRR=	0	0.0	UBRR=	0	7.8	UBRR=	0	25.0

Baud Rate	3.2768 MHz		%Error	3.6864 MHz		%Error	4 MHz		%Error	4.608 MHz		%Error
2400	UBRR=	84	0.4	UBRR=	95	0.0	UBRR=	103	0.2	UBRR=	119	0.0
4800	UBRR=	42	0.8	UBRR=	47	0.0	UBRR=	51	0.2	UBRR=	59	0.0
9600	UBRR=	20	1.6	UBRR=	23	0.0	UBRR=	25	0.2	UBRR=	29	0.0
14400	UBRR=	13	1.6	UBRR=	15	0.0	UBRR=	16	2.1	UBRR=	19	0.0
19200	UBRR=	10	3.1	UBRR=	11	0.0	UBRR=	12	0.2	UBRR=	14	0.0
28800	UBRR=	6	1.6	UBRR=	7	0.0	UBRR=	8	3.7	UBRR=	9	0.0
38400	UBRR=	4	6.3	UBRR=	5	0.0	UBRR=	6	7.5	UBRR=	7	6.7
57600	UBRR=	3	12.5	UBRR=	3	0.0	UBRR=	3	7.8	UBRR=	4	0.0
76800	UBRR=	2	12.5	UBRR=	2	0.0	UBRR=	2	7.8	UBRR=	3	6.7
115200	UBRR=	1	12.5	UBRR=	1	0.0	UBRR=	1	7.8	UBRR=	2	20.0

Baud Rate	7.3728 MHz		%Error	8 MHz		%Error	9.216 MHz		%Error	11.059 MHz		%Error
2400	UBRR=	191	0.0	UBRR=	207	0.2	UBRR=	239	0.0	UBRR=	287	-
4800	UBRR=	95	0.0	UBRR=	103	0.2	UBRR=	119	0.0	UBRR=	143	0.0
9600	UBRR=	47	0.0	UBRR=	51	0.2	UBRR=	59	0.0	UBRR=	71	0.0
14400	UBRR=	31	0.0	UBRR=	34	0.8	UBRR=	39	0.0	UBRR=	47	0.0
19200	UBRR=	23	0.0	UBRR=	25	0.2	UBRR=	29	0.0	UBRR=	35	0.0
28800	UBRR=	15	0.0	UBRR=	16	2.1	UBRR=	19	0.0	UBRR=	23	0.0
38400	UBRR=	11	0.0	UBRR=	12	0.2	UBRR=	14	0.0	UBRR=	17	0.0
57600	UBRR=	7	0.0	UBRR=	8	3.7	UBRR=	9	0.0	UBRR=	11	0.0
76800	UBRR=	5	0.0	UBRR=	6	7.5	UBRR=	7	6.7	UBRR=	8	0.0
115200	UBRR=	3	0.0	UBRR=	3	7.8	UBRR=	4	0.0	UBRR=	5	0.0

ıximum Baud rate to each frequency.

e UART Baud Rate Register - UBRR

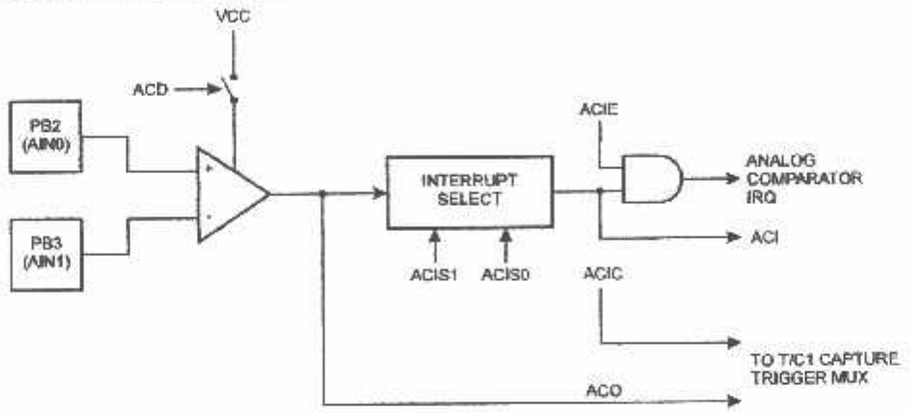
t	7	6	5	4	3	2	1	0	
›9 ($29)	MSB							LSB	UBRR
eadWrite	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
itial value	0	0	0	0	0	0	0	0	

e UBRR register is an 8-bit read/write register which specifies the UART Baud Rate according to the equation on the evious page.

ıe Analog Comparator

e analog comparator compares the input values on the sitive pin PB2 (AIN0) and negative pin PB3 (AIN1). ıen the voltage on the positive pin PB2 (AIN0) is higher ın the voltage on the negative pin PB3 (AIN1), the Ana- Comparator Output, ACO is set (one). The compara- 's output can be set to trigger the Timer/Counter1 Input Capture function. In addition, the comparator can trigger a separate interrupt, exclusive to the Analog Comparator. The user can select Interrupt triggering on comparator output rise, fall or toggle. A block diagram of the comparator and its surrounding logic is shown in Figure 44.

ıure 44. Analog Comparator Block Diagram



ıe Analog Comparator Control And Status Register - ACSR

it	7	6	5	4	3	2	1	0	
38 ($28)	ACD	-	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	ACSR
ead/Write	R/W	R	R	R/W	R/W	R/W	R/W	R/W	
itial value	0	0	0	0	0	0	0	0	

3it 7 - ACD: Analog Comparator Disable
ıen this bit is set(one), the power to the analog compara- is switched off. This bit can be set at any time to turn off ı analog comparator. When changing the ACD bit, the alog Comparator Interrupt must be disabled by clearing ı ACIE bit in ACSR. Otherwise an interrupt can occur ıen the bit is changed.

3it 6 - Res: Reserved bit
is bit is a reserved bit in the AT90S4434/8535 and will ways read as zero.

3it 5 - ACO: Analog Comparator Output
:O is directly connected to the comparator output.

3it 4 - ACI: Analog Comparator Interrupt Flag
is bit is set (one) when a comparator output event trig- rs the interrupt mode defined by ACI1 and ACI0. The alog Comparator Interrupt routine is executed if the :IE bit is set (one) and the I-bit in SREG is set (one). ACI :leared by hardware when executing the corresponding interrupt handling vector. Alternatively, ACI is cleared by writing a logic one to the flag.

- **Bit 3 - ACIE: Analog Comparator Interrupt Enable**
When the ACIE bit is set (one) and the I-bit in the Status Register is set (one), the analog comparator interrupt is activated. When cleared (zero), the interrupt is disabled.

- **Bit 2 - ACIC: Analog Comparator Input Capture Enable**
When set (one), this bit enables the Input Capture function in Timer/Counter1 to be triggered by the analog comparator. The comparator output is in this case directly connected to the Input Capture front-end logic, making the comparator utilize the noise canceler and edge select features of the Timer/Counter1 Input Capture interrupt. When cleared (zero), no connection between the analog comparator and the Input Capture function is given. To make the comparator trigger the Timer/Counter1 Input Capture interrupt, the TICIE1 bit in the Timer Interrupt Mask Register (TIMSK) must be set (one).

its 1,0 - ACIS1, ACIS0: Analog Comparator Interrupt Mode elect

ese bits determine which comparator events that trigger Analog Comparator interrupt. The different settings are wn in Table 25.

le 25. ACIS1/ACIS0 Settings

CIS1	ACIS0	Interrupt Mode
0	0	Comparator Interrupt on Output Toggle
0	1	Reserved
1	0	Comparator Interrupt on Falling Output Edge
1	1	Comparator Interrupt on Rising Output Edge

e: When changing the ACIS1/ACIS0 bits, The Analog Comparator Interrupt must be disabled by clearing its Interrupt Enable bit in the ACSR register. Otherwise an interrupt can occur when the bits are changed.

The Analog to Digital Converter

Feature list:

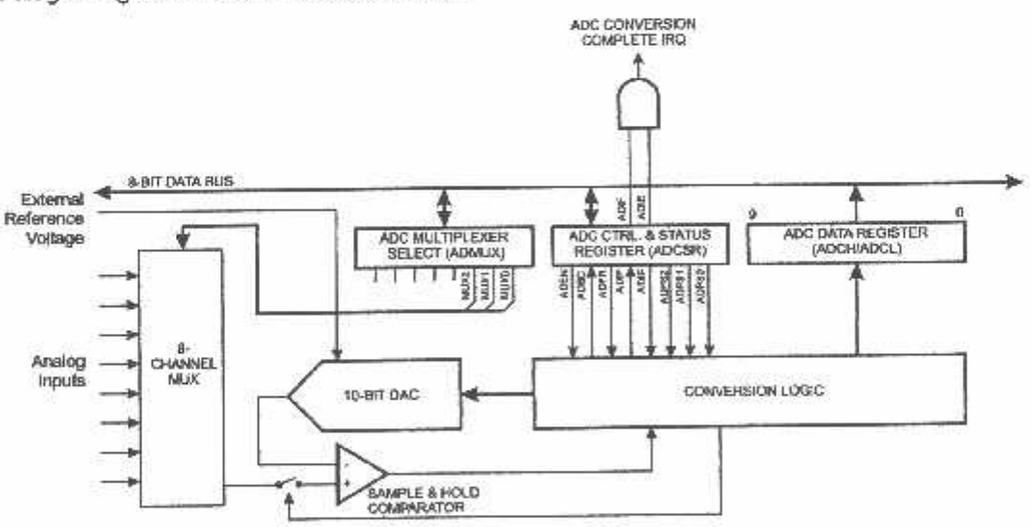
- 10-bit Resolution
- ±½ LSB Accuracy
- 65 - 260 µs Conversion Time
- 8 Multiplexed Input Channels
- Rail-to-Rail Input Range
- Free Run or Single Conversion Mode
- Interrupt on ADC Conversion Complete
- Sleep Mode Noise Canceler

The AT90S4434/8535 features a 10-bit successive approximation ADC. The ADC is connected to an 8-channel Analog Multiplexer which allows each pin of Port A to be used as an input for the ADC. The ADC contains a Sample and Hold Amplifier which ensures that the input voltage to the ADC is held at a constant level during conversion. A block diagram of the ADC is shown in Figure 45.

The ADC has two separate analog supply voltage pins, AV_{CC} and AGND. AGND must be connected to GND, and the voltage on AV_{CC} must not differ more than ±0.3V from V_{CC}. See the paragraph ADC Noise Canceling Techniques on how to connect these pins.

An external reference voltage must be applied to the AREF pin. This voltage must be in the range AGND - AV_{CC}.

gure 45. Analog to Digital Converter Block Schematic



Operation

The ADC can operate in two modes - Single Conversion and Free Running Mode. In Single Conversion Mode, each conversion will have to be initiated by the user. In Free Running Mode, the ADC is constantly sampling and updating the ADC Data Register. The ADFR bit in ADCSR selects between the two available modes.

The ADC is enabled by writing a logical one to the ADC Enable bit, ADEN in ADCSR. The first conversion that is started after enabling the ADC, will be preceded by a dummy conversion to initialize the ADC. To the user, the only difference will be that this conversion takes 25 clock pulses instead of the normal 14.

onversion is started by writing a logical one to the ADC rt Conversion bit, ADSC. This bit stays high as long as conversion is in progress and will be set to zero by dware when the conversion is completed. If a different a channel is selected while a conversion is in progress, ADC will finish the current conversion before perform- the channel change.

the ADC generates a 10-bit result, two data registers, CH and ADCL, must be read to get the result when the version is complete. Special data protection logic is d to ensure that the contents of the data registers ong to the same conversion when they are read. This chanism works as follows:

an reading data, ADCL must be read first. Once ADCL ead, ADC access to data registers is blocked. This ans that if ADCL has been read, and a conversion com- tes before ADCH is read, none of the registers are lated and the result from the conversion is lost. When CH is read, ADC access to the ADCH and ADCL regis- is re-enabled.

ADC has its own interrupt which can be triggered when onversion completes. When ADC access to the data isters is prohibited between reading of ADCH and CL, the interrupt will trigger even if the result gets lost.

escaling

ADC accepts input clock frequencies in the range 50 -) kHz. In free running mode, the ADC needs 13 clock pulses to perform a conversion, which means that the conversion time range is 65 - 260 µs. In single conversion mode, the conversion time is 14 clock cycles. The output of the ADC is not guaranteed to be correct if the input clock is out of range. The ADPS0 - ADPS2 bits are used to generate a proper ADC clock input frequency from any XTAL frequency above 100 kHz.

ADC Noise Canceler Function

The ADC features a noise canceler that enables conversion during idle mode to reduce noise induced from the CPU core. To make use of this feature, the following procedure should be used:

1. Make sure that the ADC is enabled and is not busy converting. Single Conversion Mode must be selected and the ADC conversion complete interrupt must be enabled.
   ADEN = 1
   ADSC = 0
   ADFR = 0
   ADIE = 1
2. Enter idle mode. The ADC will start a conversion once the CPU has been halted.
3. If no other interrupts occur before the ADC conversion completes, the ADC interrupt will wake up the MCU and execute the ADC conversion complete interrupt routine.

ADC Multiplexer Select Register - ADMUX

	7	6	5	4	3	2	1	0	
($27)	-	-	-	-	-	MUX2	MUX1	MUX0	ADMUX
ad/Write	R	R	R	R	R	R/W	R/W	R/W	
ial value	0	0	0	0	0	0	0	0	

Bits 7..3 - Res: Reserved Bits

These bits are reserved bits in the AT90S4434/8535 and ays read as zero.

Bits 2..0 - MUX2..MUX0: Analog Channel Select Bits 2-0

The value of these three bits selects which analog input 7-0 is connected to the ADC.

ADC Control and Status Register - ADCSR

	7	6	5	4	3	2	1	0	
6 ($26)	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSR
ad/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
tial value	0	0	0	0	0	0	0	0	

Bit 7 - ADEN: ADC Enable

ting a logical '1' to this bit enables the ADC. By clearing bit to zero, the ADC is turned off. Turning the ADC off le a conversion is in progress, will terminate this conver-).

Bit 6 - ADSC: ADC Start Conversion

Single Conversion Mode, a logical '1' must be written to bit to start each conversion. In Free Run Mode, a logi- '1' must be written to this bit to start the first conversion. The first time ADSC has been written after the ADC has been enabled, or if ADSC is written at the same time as the ADC is enabled, a dummy conversion will precede the initiated conversion. This dummy conversion performs initialization of the ADC.

ADSC will read as one as long as a conversion is in progress. When the conversion is complete, it returns to zero. When a dummy conversion precedes a real conver-

ın, ADSC will stay high until the real conversion com-
ɨtes.

ɨiting a 0 to this bit has no effect.

3it 5 - ADFR: ADC Free Run Select

ıen this bit is set (one) the ADC operates in Free Run-
ıg mode. In this mode, the ADC samples and updates
› data registers continuously. Clearing this bit (zero) will
ıminate Free Running mode.

3it 4 -ADIF: ADC Interrupt Flag

is bit is set (one) when an ADC conversion completes
d the data registers are updated. The ADC Conversion
ımplete Interrupt is executed if the ADIE bit and the I-bit
SREG are set (one). ADIF is cleared by hardware when
ecuting the corresponding interrupt handling vector.
ernatively, ADIF is cleared by writing a logical one to the
g. Beware that if doing a read-modify-write on ADCSR, a
nding interrupt can be disabled. This also applies if the
il and CBI instructions are used.

- **Bit 3 - ADIE: ADC Interrupt Enable**

When this bit is set (one) and the I-bit in SREG is set (one), the ADC Conversion Complete Interrupt is activated.

- **Bits 2..0 - ADPS2..ADPS0: ADC Prescaler Select Bits**

These bits determine the division factor between the XTAL frequency and the input clock to the ADC.

Table 26. ADC Prescaler Selections

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ıe ADC Data Register - ADCL AND ADCH

ıl	15	14	13	12	11	10	9	8	
05 ($25)	-	-	-	-	-	-	ADC9	ADC8	ADCH
04 ($24)	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	ADCL
	7	6	5	4	3	2	1	0	
ead/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
itial value	8	0	0	0	0	0	0	0	
	8	0	0	0	0	0	0	0	

ıen an ADC conversion is complete, the result is found in
ɜse two registers. In free-run mode, it is essential that
th registers are read, and that ADCL is read before
)CH.

ɜanning Multiple Channels

ıce change of analog channel always is delayed until a
ıversion is finished, the free running mode can be used
scan multiple channels without interrupting the con-
ɵter. Typically, the ADC Conversion Complete interrupt
l be used to perform the channel shift. However, the user
ɔuld take the following fact into consideration:

e interrupt triggers once the result is ready to be read. In
e running mode, the next conversion will start immedi-
ɜly when the interrupt triggers. If ADMUX is changed
ɜr the interrupt triggers, the next conversion has already
ırted, and the old setting is used.

)C Noise Canceling Techniques

ɟital circuitry inside and outside the AT90S4434/8535
nerates EMI which might affect the accuracy of analog measurements. If conversion accuracy is critical, the noise level can be reduced by applying the following techniques:

1. The analog part of the AT90S4434/8535 and all analog components in the application should have a separate analog ground plane on the PCB. This ground plane is connected to the digital ground plane via a single point on the PCB.

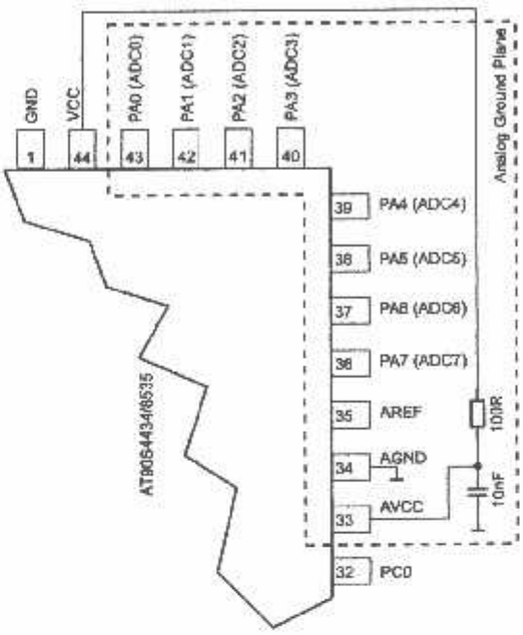
2. Keep analog signal paths as short as possible. Make sure analog tracks run over the analog ground plane, and keep them well away from high-speed switching digital tracks.

3. The AV_{CC} pin on the AT90S4434/8535 should be connected to the digital V_{CC} supply voltage via an RC network as shown in Figure 46.

4. Use the ADC noise canceler function to reduce induced noise from the CPU.

5. If some Port A pins are used as digital outputs, it is essential that these do not switch while a conversion is in progress.

jure 46. ADC Power Connections



ıte that since AV_{CC} feeds the Part A output drivers, the RC network shown should not be employed if any Port A serve as tputs.

DC Characteristics

= -40°C to 85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution			10		Bits
	Integral Non-Linearity	V_{REF} > 2V		0.2	0.5	LSB
	Differential Non-Linearity	V_{REF} > 2V		0.2	0.5	LSB
	Zero Error (Offset)			1		LSB
	Conversion Time		65		260	ms
	Clock Frequency		50		200	KHz
AV_{CC}	Analog Supply Voltage		V_{CC} - 0.3(1)		V_{CC} + 0.3(2)	V
V_{REF}	Reference Voltage		AGND		AV_{CC}	V
R_{REF}	Reference Input Resistance		6	10	13	KΩ
R_{AIN}	Analog Input Resistance			100		MΩ

tes: 1. Minimum for AV_{CC} is 2.7V.
2. Maximum for AV_{CC} is 6.0V.

D-Ports

ırt A

rt A is an 8-bit bi-directional I/O port.

ree data memory address locations are allocated for rt A, one each for the Data Register - PORTA, $1B($3B), Data Direction Register - DDRA, $1A($3A) and the Port A Input Pins - PINA, $19($39). The Port A Input Pins address is read only, while the Data Register and the Data Direction Register are read/write.

port pins have individually selectable pull-up resistors. › PORT A output buffers can sink 20mA and thus drive D displays directly. When pins PA0 to PA7 are used as uts and are externally pulled low, they will source cur- t If the internal pull-up resistors are activated.

't A has an alternate function as analog inputs for the C. If some Port A pins are configured as outputs, it is essential that these do not switch when a conversion is in progress. This might corrupt the result of the conversion.

During powerdown mode, the schmitt trigger of the digital input is disconnected. This allows analog signals that are close to $V_{CC}/2$ to be present during powerdown without causing excessive power consumption.

› Port A Data Register - PORTA

	7	6	5	4	3	2	1	0	
; ($3B)	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	PORTA
ad/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ial value	0	0	0	0	0	0	0	0	

› Port A Data Direction Register - DDRA

	7	6	5	4	3	2	1	0	
A ($3A)	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
ad/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ial value	0	0	0	0	0	0	0	0	

e Port A Input Pins Address - PINA

	7	6	5	4	3	2	1	0	
9 ($39)	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	PINA
ead/Write	R	R	R	R	R	R	R	R	
itial value	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	

e Port A Input Pins address - PINA - is not a register, d this address enables access to the physical value on ch Port A pin. When reading PORTA the PORTA Data tch is read, and when reading PINA, the logical values ısent on the pins are read.

RT A as General Digital I/O

8 bits in PORT A are equal when used as digital I/O s.

PAn, General I/O pin: The DDAn bit in the DDRA register selects the direction of this pin, if DDAn is set (one), PAn is configured as an output pin. If DDAn is cleared (zero), PAn is configured as an input pin. If PORTAn is set (one) when the pin configured as an input pin, the MOS pull up resistor is activated. To switch the pull up resistor off, the PORTAn has to be cleared (zero) or the pin has to be configured as an output pin.

›le 27. DDAn Effects on PORTA Pins

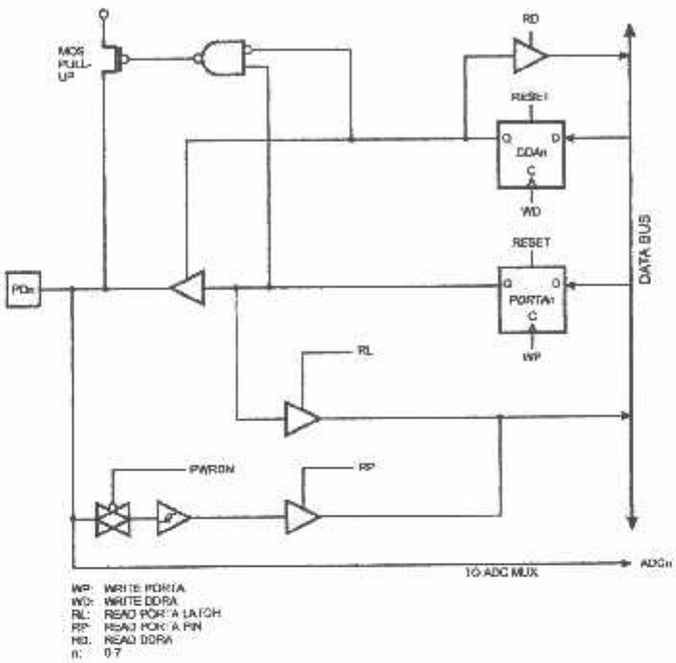
DDAn	PORTAn	I/O	Pull Up	Comment
0	0	Input	No	Tri-state (Hi-Z)
0	1	Input	Yes	PAn will source current if ext. pulled low.
1	0	Output	No	Push-Pull Zero Output
1	1	Output	No	Push-Pull One Output

',6...0, pin number.

RT A Schematics

le that all port pins are synchronized. The synchroniza-
ı latch is however, not shown in the figure.

ure 47. PORTA Schematic Diagrams (Pins PA0 - PA7)



ırt B

rt B is an 8-bit bi-directional I/O port.

ee data memory address locations are allocated for the
t B, one each for the Data Register - PORTB, $18($38),
ta Direction Register - DDRB, $17($37) and the Port B
ut Pins - PINB, $16($36). The Port B Input Pins address
ead only, while the Data Register and the Data Direction
gister are read/write.

port pins have individually selectable pull-up resistors.
e Port B output buffers can sink 20mA and thus drive
D displays directly. When pins PB0 to PB7 are used as
uts and are externally pulled low, they will source cur-
t if the internal pull-up resistors are activated.

The Port B pins with alternate functions are shown in the following table:

Table 28. Port B Pins Alternate Functions

Port Pin	Alternate Functions
PB0	T0 (Timer/Counter 0 external counter input)
PB1	T1 (Timer/Counter 1 external counter input)
PB2	AIN0 (Analog comparator positive input)
PB3	AIN1 (Analog comparator negative input)
PB4	$\overline{SS}$ (SPI Slave Select input)
PB5	MOSI (SPI Bus Master Output/Slave Input)
PB6	MISO (SPI Bus Master Input/Slave Output)
PB7	SCK (SPI Bus Serial Clock)

When the pins are used for the alternate function, the DDRB and PORTB registers have to be set according to the alternate function description.

Port B Data Register - PORTB

	7	6	5	4	3	2	1	0	
(38)	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	PORTB
Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
value	0	0	0	0	0	0	0	0	

Port B Data Direction Register - DDRB

	7	6	5	4	3	2	1	0	
(37)	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
value	0	0	0	0	0	0	0	0	

Port B Input Pins Address - PINB

	7	6	5	4	3	2	1	0	
(36)	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	PINB
Write	R	R	R	R	R	R	R	R	
value	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	

Port B Input Pins address - PINB - is not a register, his address enables access to the physical value on Port B pin. When reading PORTB, the PORTB Data is read, and when reading PINB, the logical values ent on the pins are read.

B As General Digital I/O

bits in Port B are equal when used as digital I/O pins.

PBn, General I/O pin: The DDBn bit in the DDRB register selects the direction of this pin, if DDBn is set (one), PBn is configured as an output pin. If DDBn is cleared (zero), PBn is configured as an input pin. If PORTBn is set (one) when the pin configured as an input pin, the MOS pull up resistor is activated. To switch the pull up resistor off, the PORTBn has to be cleared (zero) or the pin has to be configured as an output pin.

e 29. DDBn Effects on Port B Pins

DDBn	PORTBn	I/O	Pull Up	Comment
0	0	Input	No	Tri-state (Hi-Z)
0	1	Input	Yes	PBn will source current if ext. pulled low.
1	0	Output	No	Push-Pull Zero Output
1	1	Output	No	Push-Pull One Output

...0, pin number.

nate Functions Of PORTB

lternate pin configuration is as follows:

K - PORTB, Bit 7

: Master clock output, slave clock input pin for SPI nel. When the SPI is enabled as a slave, this pin is gured as an input regardless of the setting of DDB7. the SPI is enabled as a master, the data direction of in is controlled by DDB7. When the pin is forced to be put, the pull-up can still be controlled by the PORTB7 ee the description of the SPI port for further details.

O - PORTB, Bit 6

): Master data input, slave data output pin for SPI nel. When the SPI is enabled as a master, this pin is gured as an input regardless of the setting of DDB6. the SPI is enabled as a slave, the data direction of in is controlled by DDB6. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB6 bit. See the description of the SPI port for further details.

- **MOSI - PORTB, Bit 5**

MOSI: SPI Master data output, slave data input for SPI channel. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB5. When the SPI is enabled as a master, the data direction of this pin is controlled by DDB5. When the pin is forced to be an input, the pull-up can still be controlled by the PORTB5 bit. See the description of the SPI port for further details.

- **$\overline{SS}$ - PORTB, Bit 4**

$\overline{SS}$: Slave port select input. When the SPI is enabled as a slave, this pin is configured as an input regardless of the setting of DDB4. As a slave, the SPI is activated when this pin is driven low. When the SPI is enabled as a master, the data direction of this pin is controlled by DDB4. When the pin is forced to be an input, the pull-up can still be con-

d by the PORTB4 bit. See the description of the SPI for further details.

i1 - PORTB, Bit 3

, Analog Comparator Negative Input. When config- as an input (DDB3 is cleared (zero)) and with the ıal MOS pull up resistor switched off (PB3 is cleared)), this pin also serves as the negative input of the on- analog comparator. During power down mode, the ıitt trigger of the digital input is disconnected. This /s analog signals which are close to $V_{CC}/2$ to be ənt during power down without causing excessive r consumption.

• AIN0 - PORTB, Bit 2

AIN0, Analog Comparator Positive Input. When configured as an input (DDB2 is cleared (zero)) and with the internal MOS pull up resistor switched off (PB2 is cleared (zero)), this pin also serves as the positive input of the on-chip analog comparator. During power down mode, the schmitt trigger of the digital input is disconnected. This allows analog signals which are close to $V_{CC}/2$ to be present during power down without causing excessive power consumption.

• T1 - PORTB, Bit 1

T1, Timer/Counter1 counter source. See the timer description for further details

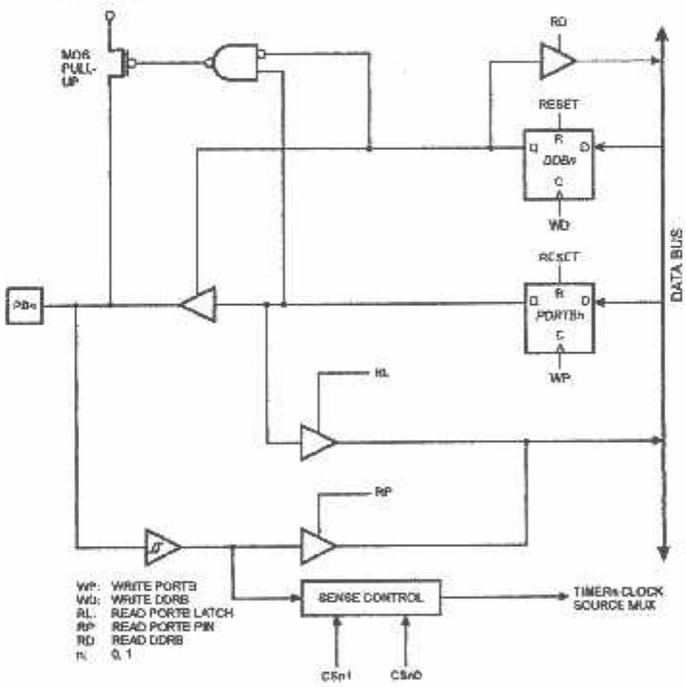
• T0 - PORTB, Bit 0

T0: Timer/Counter0 counter source. See the timer description for further details.

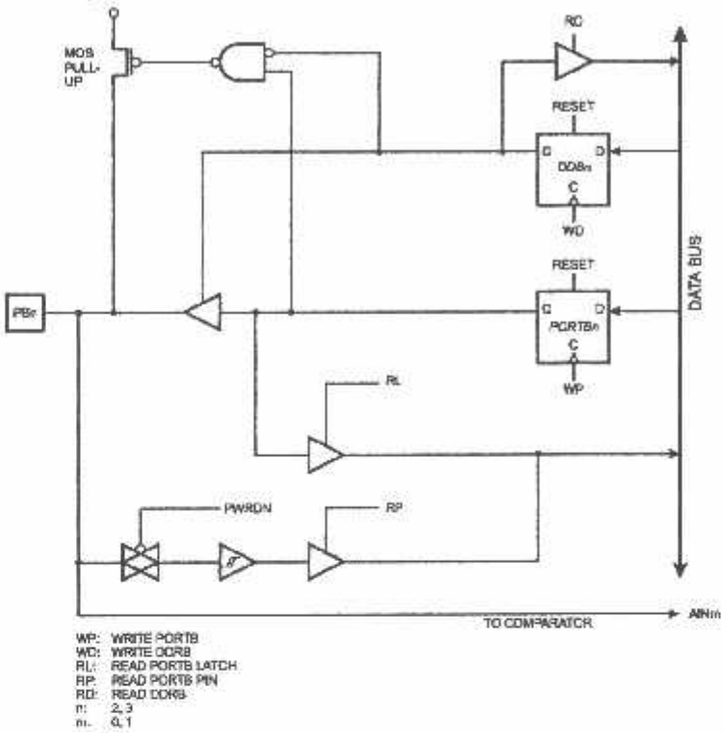
B Schematics

that all port pins are synchronized. The synchroniza- atches are however, not shown in the figures.

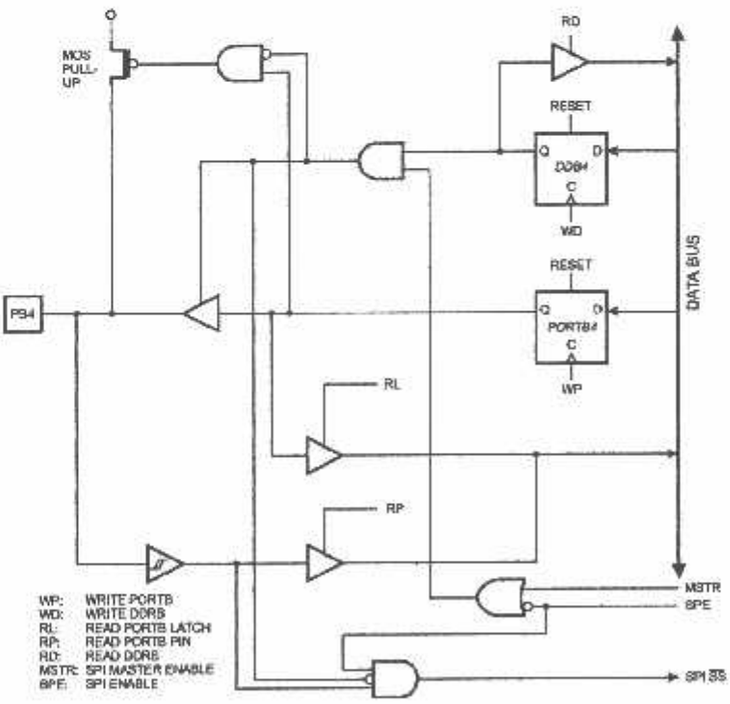
re 48. PORTB Schematic Diagram (Pins PB0 and PB1)



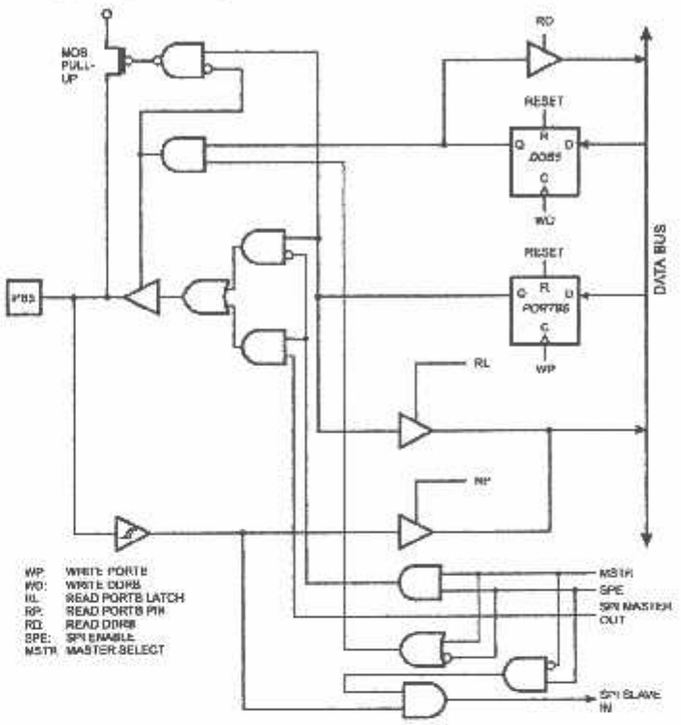
re 49. PORTB Schematic Diagram (Pins PB2 and PB3)



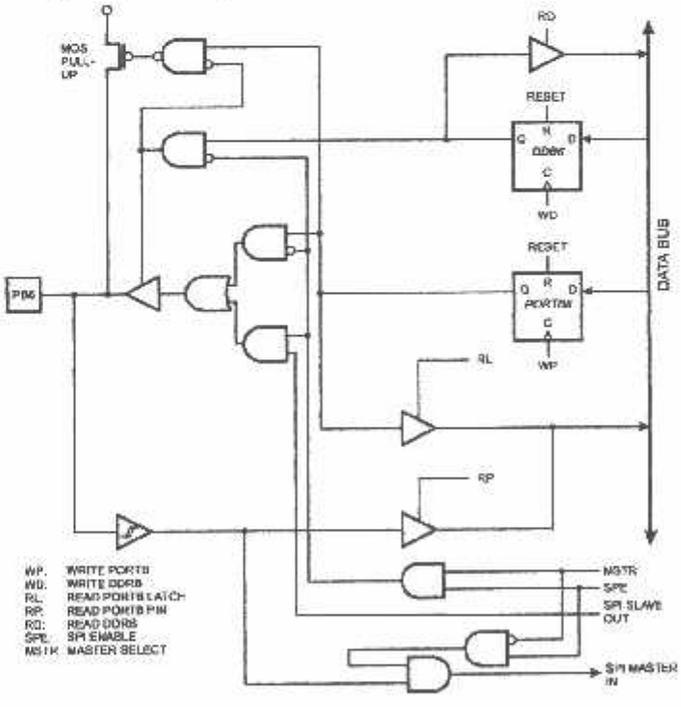
re 50. PORTB Schematic Diagram (Pin PB4)



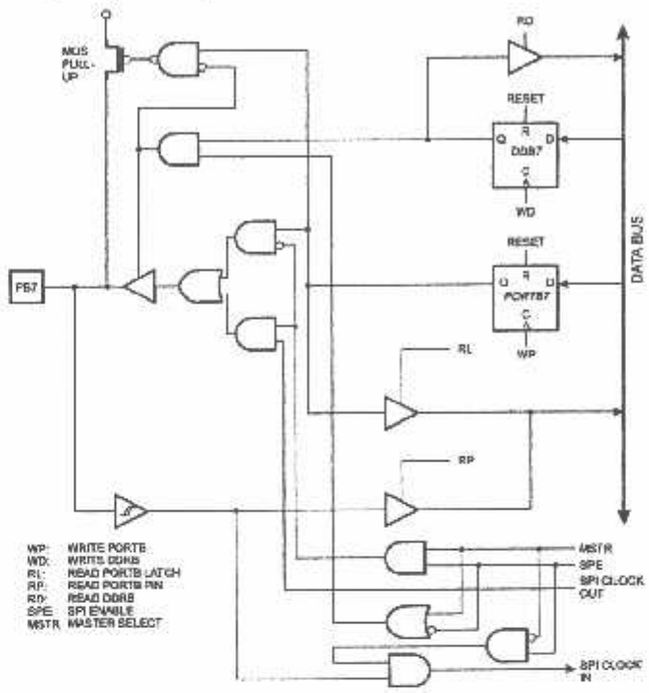
re 51. PORTB Schematic Diagram (Pin PB5)



re 52. PORTB Schematic Diagram (Pin PB6)



re 53. PORTB Schematic Diagram (Pin PB7)



t C

C is an 8-bit bi-directional I/O port.

e data memory address locations are allocated for the C, one each for the Data Register - PORTC, $15($35), Direction Register - DDRC, $14($34) and the Port C ! Pins - PINC, $13($33). The Port C Input Pins address ad only, while the Data Register and the Data Direction ster are read/write.

All port pins have individually selectable pull-up resistors. The PORT C output buffers can sink 20mA and thus drive LED displays directly. When pins PC0 to PC7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

Port C Data Register - PORTC

	7	6	5	4	3	2	1	0	
$35)	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	PORTC
/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
value	0	0	0	0	0	0	0	0	

Port C Data Direction Register - DDRC

	7	6	5	4	3	2	1	0	
$34)	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
value	0	0	0	0	0	0	0	0	

Port C Input Pins Address - PINC

	7	6	5	4	3	2	1	0	
$33)	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	PINC
/Write	R	R	R	R	R	R	R	R	
value	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	

Port C Input Pins address - PINC - is not a register, his address enables access to the physical value on Port C pin. When reading PORTC, the PORTC Data ı is read, and when reading PINC, the logical values ınt on the pins are read.

C As General Digital I/O

bits in PORT C are equal when used as digital I/O

PCn, General I/O pin: The DDCn bit in the DDRC register selects the direction of this pin, if DDCn is set (one), PCn is configured as an output pin. If DDCn is cleared (zero), PCn is configured as an input pin. If PORTCn is set (one) when the pin configured as an input pin, the MOS pull up resistor is activated. To switch the pull up resistor off, PORTCn has to be cleared (zero) or the pin has to be configured as an output pin.

30. DDCn Effects on PORT C Pins

DDCn	PORTCn	I/O	Pull Up	Comment
0	0	Input	No	Tri-state (Hi-Z)
0	1	Input	Yes	PCn will source current if ext. pulled low.
1	0	Output	No	Push-Pull Zero Output
1	1	Output	No	Push-Pull One Output

.0, pin number

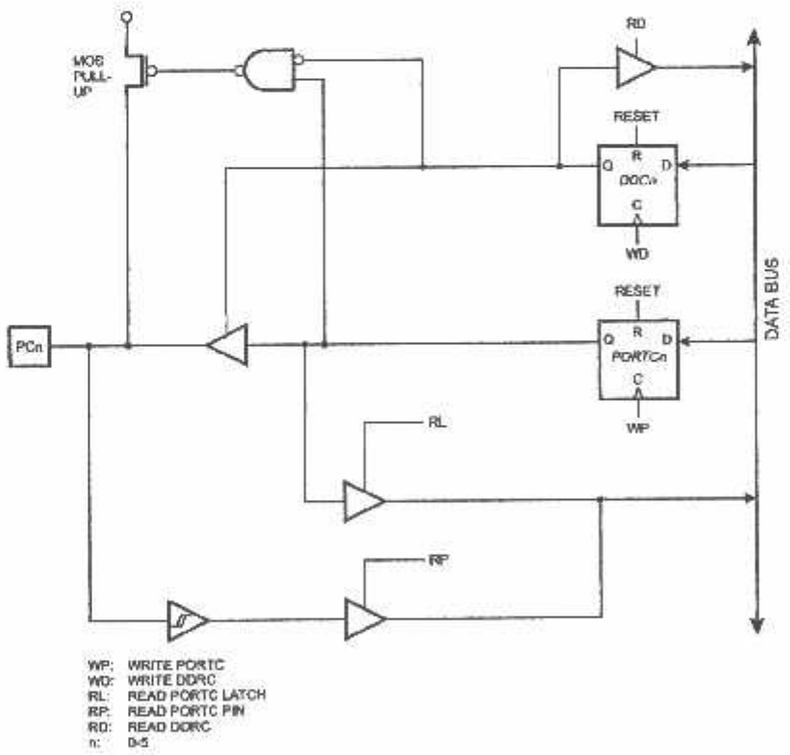
nate Functions of PORTC

n the AS2 bit in ASSR is set (one) to enable asynchro- clocking of Timer/Counter2, pins PC6 and PC7 are nnected from the port. In this mode, a crystal oscillator is connected to the pins, and the pins can not be used as I/O pins.

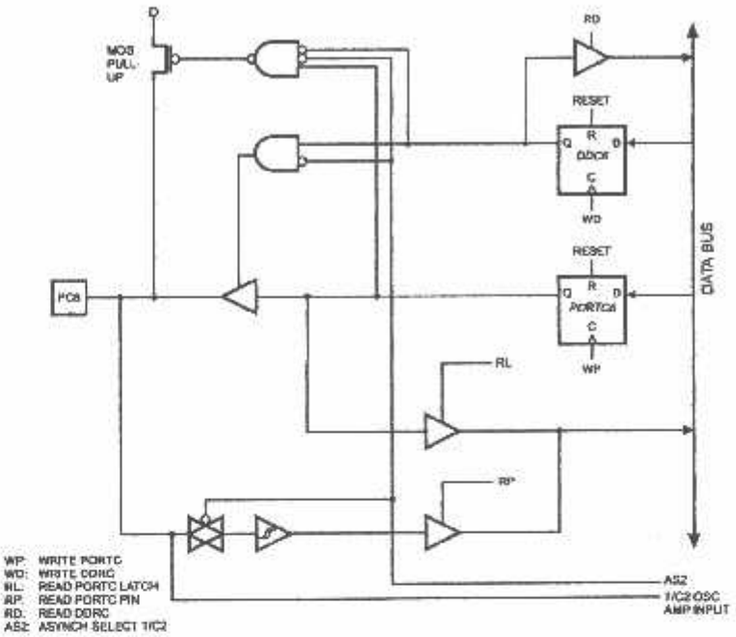
Port C Schematics

Note that all port pins are synchronized. The synchronization latch is however, not shown in the figure.

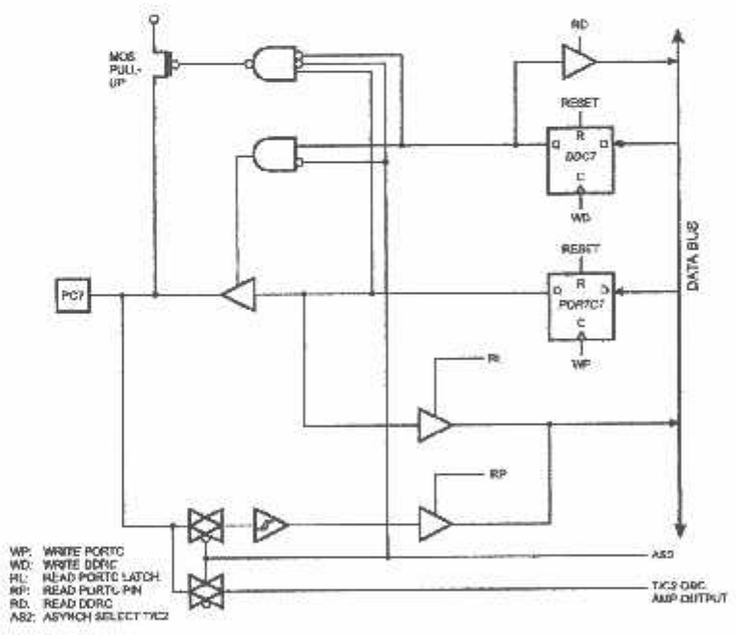
re 54. PORTC Schematic Diagram (Pins PC0 - PC5)



e 55. PORTC Schematic Diagram (Pins PC6)



re 56. PORTC Schematic Diagram (Pins PC7)



D

) is an 8 bit bi-directional I/O port with internal pull-up ors.

e data memory address locations are allocated for), one each for the Data Register - PORTD, $12($32), Data Direction Register - DDRD, $11($31) and the Port D Input Pins - PIND, $10($30). The Port D Input Pins address is read only, while the Data Register and the Data Direction Register are read/write.

?ort D output buffers can sink 20 mA. As inputs, Port D that are externally pulled low will source current if the ıp resistors are activated.

Some Port D pins have alternate functions as shown in the following table:

1 31. Port D Pins Alternate Functions

Port Pin	Alternate Function
PD0	RDX (UART Input line)
PD1	TDX (UART Output line)
PD2	INT0 (External Interrupt 0 Input)
PD3	INT1 (External interrupt 1 input)
PD4	OC1B (Timer/Counter1 output compareB match output)
PD5	OC1A (Timer/Counter1 output compareA match output)
PD6	ICP (Timer/Counter1 input capture pin)
PD7	OC2 (Timer/Counter2 output compare match output]

Port D Data Register - PORTD

	7	6	5	4	3	2	1	0	
$32)	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	PORTD
/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
l value	0	0	0	0	0	0	0	0	

Port D Data Direction Register - DDRD

	7	6	5	4	3	2	1	0	
$31)	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
value	0	0	0	0	0	0	0	0	

Port D Input Pins Address - PIND

	7	6	5	4	3	2	1	0	
$30)	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	PIND
/Write	R	R	R	R	R	R	R	R	
value	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	

?ort D Input Pins address - PIND - is not a register, his address enables access to the physical value on Port D pin. When reading PORTD, the PORTD Data ı is read, and when reading PIND, the logical values ınt on the pins are read.

Port D As General Digital I/O

PDn, General I/O pin: The DDDn bit in the DDRD register selects the direction of this pin. If DDDn is set (one), PDn is configured as an output pin. If DDDn is cleared (zero), PDn is configured as an input pin. If PDn is set (one) when configured as an input pin the MOS pull up resistor is activated. To switch the pull up resistor off the PDn has to be cleared (zero) or the pin has to be configured as an output pin.

1 32. DDDn Bits on Port D Pins

DDDn	PORTDn	I/O	Pull Up	Comment
0	0	Input	No	Tri-state (Hi-Z)
0	1	Input	Yes	PDn will source current if ext. pulled low.
1	0	Output	No	Push-Pull Zero Output
1	1	Output	No	Push-Pull One Output

ı...0, pin number.

ernate Functions Of PORTD

)C2- PORTD, Bit 7

:2, Timer/Counter2 output compare match output: The)7 pin can serve as an external output for the ner/Counter2 output compare. The pin has to be config- id as an output (DDD7 set (one)) to serve this function. e the timer description on how to enable this function. e OC2 pin is also the output pin for the PWM mode timer ction.

CP - PORTD, Bit 6

P - Input Capture Pin: The PD6 pin can act as an input ture pin for Timer/Counter1. The pin has to be config- d as an input (DDD6 cleared(zero)) to serve this func- 1. See the timer description on how to enable this ction.

)C1A- PORTD, Bit 5

:1A, Output compare matchA output: The PD5 pin can ve as an external output for the Timer/Counter1 output mpareA. The pin has to be configured as an output DD5 set (one)) to serve this function. See the timer scription on how to enable this function. The OC1A pin is o the output pin for the PWM mode timer function.

)C1B- PORTD, Bit 4

:1B, Output compare matchB output: The PD4 pin can rve as an external output for the Timer/Counter1 output mpareB. The pin has to be configured as an output DD4 set (one)) to serve this function. See the timer description on how to enable this function. The OC1B pin is also the output pin for the PWM mode timer function.

- **INT1 - PORTD, Bit 3**

INT1, External Interrupt source 1: The PD3 pin can serve as an external interrupt source to the MCU. See the interrupt description for further details, and how to enable the source.

- **INT0 - PORTD, Bit 2**

INT0, External Interrupt source 0: The PD2 pin can serve as an external interrupt source to the MCU. See the interrupt description for further details, and how to enable the source.

- **TXD - PORTD, Bit 1**

Transmit Data (Data output pin for the UART). When the UART transmitter is enabled, this pin is configured as an output regardless of the value of DDD1.

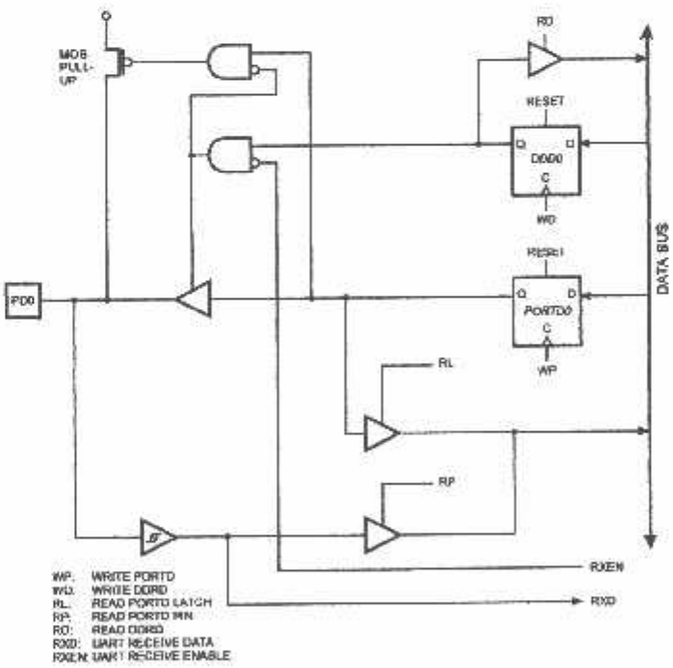
- **RXD - PORTD, Bit 0**

Receive Data (Data input pin for the UART). When the UART receiver is enabled this pin is configured as an output regardless of the value of DDRD0. When the UART forces this pin to be an input, a logical one in PORTD0 will turn on the internal pull-up.

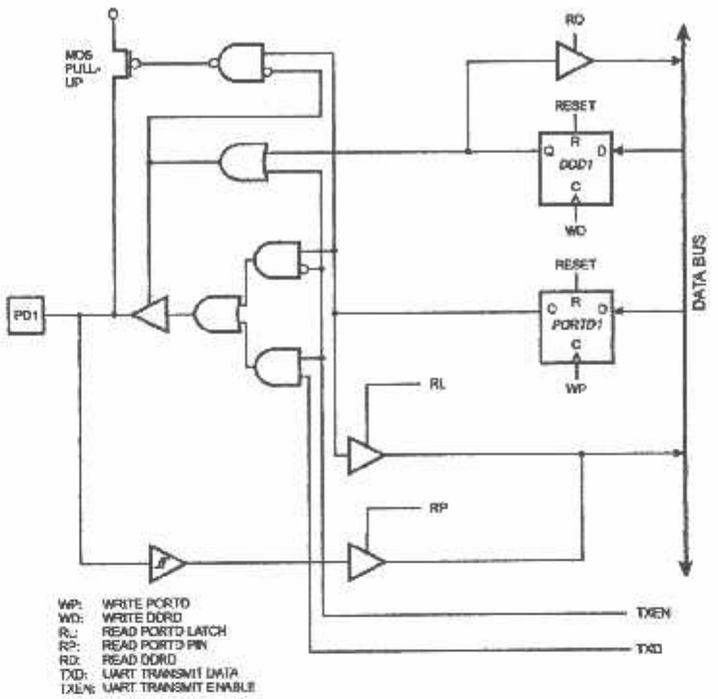
Port D Schematics

Note that all port pins are synchronized. The synchronization latches are however, not shown in the figures.

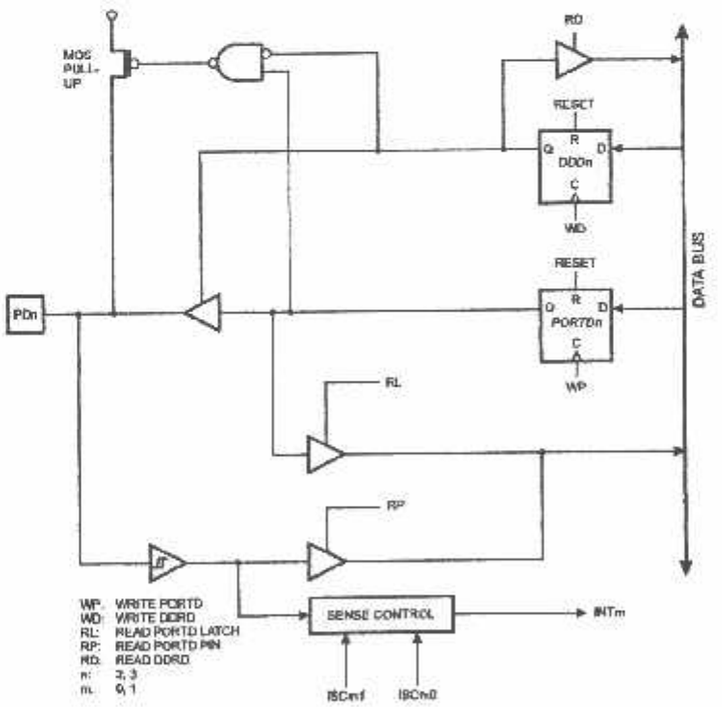
gure 57. PORTD Schematic Diagram (Pin PD0)



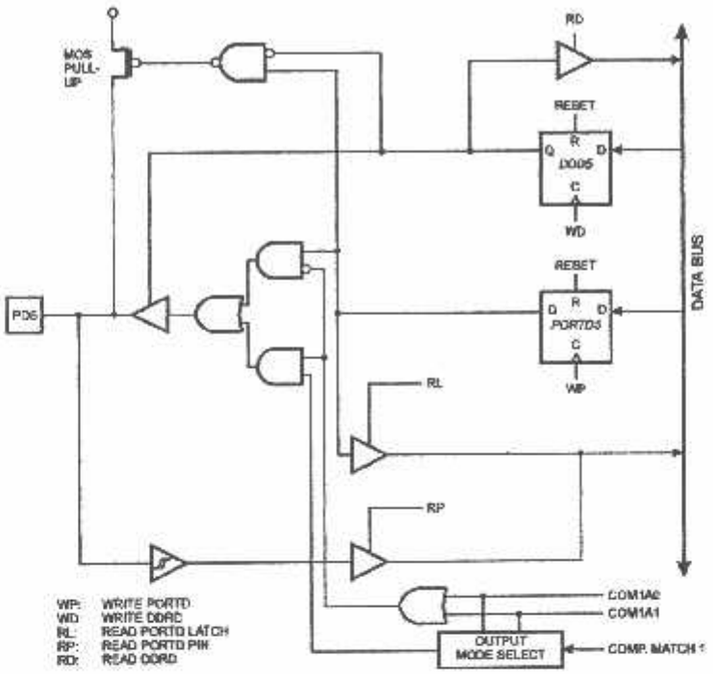
ure 58. PORTD Schematic Diagram (Pin PD1)



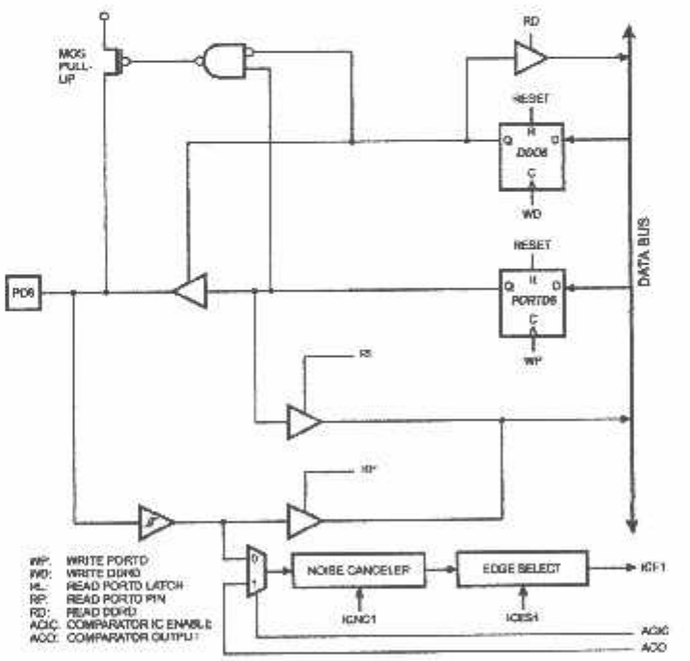
jure 59. PORTD Schematic Diagram (Pins PD2 and PD3)



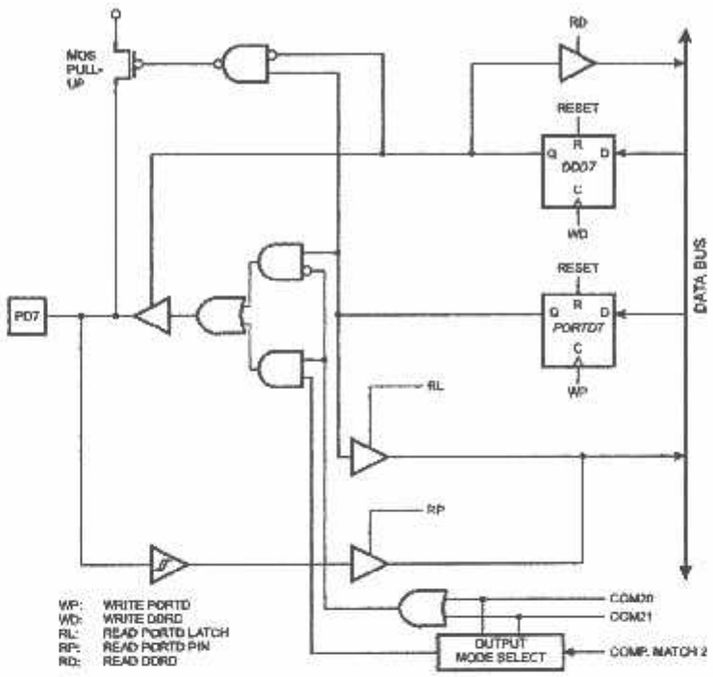
ure 60. PORTD Schematic Diagram (Pins PD4 and PD5)



ure 61. PORTD Schematic Diagram (Pin PD6)



ure 62. PORTD Schematic Diagram (Pin PD7)



emory Programming

ogram Memory Lock Bits

e AT90S4434/8535 MCU provides two lock bits which n be left unprogrammed ('1') or can be programmed ('0') obtain the additional features listed in Table 33.

ble 33. Lock Bit Protection Modes

Program Lock Bits			Protection Type
ode	LB1	LB2	
1	1	1	No program lock features
2	0	1	Further programming of the Flash and EEPROM is disabled
3	0	0	Same as mode 2, but verify is also disabled.

e: The Lock Bits can only be erased with the Chip Erase operation.

se Bits

e AT90S4434/8535 has two fuse bits, SPIEN and TRT.

When SPIEN is programmed ('0'), Serial Program Downloading is enabled. Default value is programmed ('0'). This bit is not accessible in serial programming mode.

When FSTRT is programmed ('0'), the short start-up lime is selected. This bit is accessible through serial programming.

e status of the fuse bits is not affected by a chip erase.

gnature Bytes

Atmel microcontrollers have a three-byte signature code ich identifies the device. This code can be read in both ial[1] and parallel mode. The three bytes reside in a sep- ite address space.

- the AT90S4434, they are:
  1. $00: $1E (indicates manufactured by Atmel)
  2. $01: $92 (indicates 4kB Flash memory)
  3. $02: $03 (indicates 90S4434 device when $001 is $92)
- the AT90S8535, they are:
  1. $00: $1E (indicates manufactured by Atmel)
  2. $01: $93 (indicates 8kB Flash memory)
  3. $02: $03 (indicates 90S8535 device when $001 is $93)

e: 1. When both lock bits are programmed (lock mode 3), the signature bytes can not be read in serial mode.

Programming the Flash and EEPROM

Atmel's AT90S4434/8535 offers 4K/8K bytes of in-system reprogrammable Flash Program memory and 256/512 bytes of EEPROM Data memory.

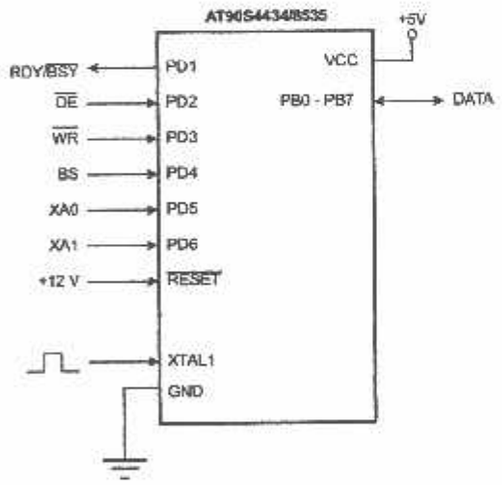
The AT90S4434/8535 is normally shipped with the on-chip Flash Program and EEPROM Data memory arrays in the erased state (i.e. contents = $FF) and ready to be programmed. This device supports a High-Voltage (12V) Parallel programming mode and a Low-Voltage Serial programming mode. The +12V is used for programming enable only, and no current of significance is drawn by this pin. The serial programming mode provides a convenient way to download the Program and Data into the AT90S4434/8535 inside the user's system.

The Program and Data memory arrays on the AT90S4434/8535 are programmed byte-by-byte in either programming modes. For the EEPROM, an auto-erase cycle is provided with the self-timed programming operation in the serial programming mode.

Parallel Programming

This section describes how to parallel program and verify Flash Program memory, EEPROM Data memory + Program Memory Lock bits and Fuse bits in the AT90S4434/8535.

Figure 63. Parallel Programming



ınal Names

ihis section, some pins of the AT908535 are referenced signal names describing their functionality during paral- programming rather than their pin names. Pins not described in the following table are referenced by pin names.

ble 34. Pin Name Mapping

Signal Name in Programming Mode	Pin Name	I/O	Function
RDY / $\overline{BSY}$	PD1	O	0: Device is busy programming, 1: Device is ready for new command
$\overline{OE}$	PD2	I	Output Enable (Active Low)
$\overline{WR}$	PD3	I	Write Pulse (Active Low)
BS	PD4	I	Byte Select
XA0	PD5	I	XTAL Action Bit 0
XA1	PD6	I	XTAL Action Bit 1

e XA1/XA0 bits determine the action taken when the AL1 pin is given a positive pulse. The bit settings are own in the following table:

ble 35. XA1 and XA0 Coding

XA1	XA0	Action when XTAL1 is Pulsed
0	0	Load Flash or EEPROM Address (High or Low address byte for Flash determined by BS)
0	1	Load Data (High or Low data byte for Flash determined by BS)
1	0	Load Command
1	1	No Action, Idle

hen pulsing $\overline{WR}$ or $\overline{OE}$, the command loaded determines e action on input or output. The command is a byte where the different bits are assigned functions as shown in the following table:

ble 36. Command Byte Bit Coding

Bit#	Meaning when Set
7	Chip Erase
6	Write Fuse Bits. Located in the data byte at the following bit positions:D5: SPIEN Fuse, D0: FSTRT Fuse (Note: Write '0' to program, '1' to erase)
5	Write Lock Bits. Located in the data byte at the following bit positions: D1: LB1, D0: LB2 (Note: write '0' to program)
4	Write Flash or EEPROM (determined by bit 0)
3	Read signature row
2	Read Lock and Fuse Bits. Located in the data byte at the following bits positions: D7: LB1, D6: LB2, D5: SPIEN Fuse, D0: FSTRT Fuse (Note: '0' means programmed)
1	Read from Flash or EEPROM (determined by bit 0)
0	0: Flash Access, 1: EEPROM Access

er Programming Mode

› following algorithm puts the device in parallel program-
ıg mode:

Apply 4.5 - 5.5 V between V_{CC} and GND.

Set $\overline{\text{RESET}}$ and BS pins to '0' and wait at least 100 ns.

Apply 11.5 - 12.5V to $\overline{\text{RESET}}$. Any activity on BS within 100 ns after +12V has been applied to $\overline{\text{RESET}}$, will cause the device to fail entering programming mode.

ip Erase

› chip erase will erase the Flash and EEPROM memo-
ı plus Lock bits. The lock bits are not reset until the pro-
m memory has been completely erased. The Fuse bits
not changed. A chip erase must be performed before
Flash is programmed.

ıd Command "Chip Erase"

Set XA1, XA0 to '10'. This enables command loading.

Set BS to '0'.

Set PB(7:0) to '1000 0000'. This is the command for Chip erase.

Give XTAL1 a positive pulse. This loads the command, and starts the erase of the Flash and EEPROM arrays. After pulsing XTAL1, give $\overline{\text{WR}}$ a negative pulse to enable lock bit erase at the end of the erase cycle, then wait for at least 10 ms. Chip erase does not generate any activity on the RDY/$\overline{\text{BSY}}$ pin.

ɔgramming the Flash

ıd Command "Program Flash"

Set XA1, XA0 to '10'. This enables command loading.

Set BS to '0'

Set PB(7:0) to '0001 0000'. This is the command for Flash programming.

Give XTAL1 a positive pulse. This loads the command.

ıd Address Low byte

Set XA1, XA0 to '00'. This enables address loading.

Set BS to '0'. This selects Low address.

3. Set PB(7:0) = Address Low byte ($00 - $FF)
4. Give XTAL1 a positive pulse. This loads the Address Low byte.

Load Address High byte

1. Set XA1, XA0 to '00'. This enables address loading.
2. Set BS to '1'. This selects High address.
3. Set PB(7:0) = Address High byte ($00 - $07/$0F)
4. Give XTAL1 a positive pulse. This loads the Address High byte.

Load Data byte

1. Set XA1, XA0 to '01'. This enables data loading.
2. Set PB(7:0) = Data Low byte ($00 - $FF)
3. Give XTAL1 a positive pulse. This loads the Data byte.

Write Data Low byte

1. Set BS to ('0').
2. Give $\overline{\text{WR}}$ a negative pulse. This starts programming of the data byte. RDY/$\overline{\text{BSY}}$ goes low.
3. Wait until RDY/$\overline{\text{BSY}}$ goes high to program the next byte.

Load Data byte

1. Set XA1, XA0 to '01'. This enables data loading.
2. Set PB(7:0) = Data High byte ($00 - $FF)
3. Give XTAL1 a positive pulse. This loads the Data byte.

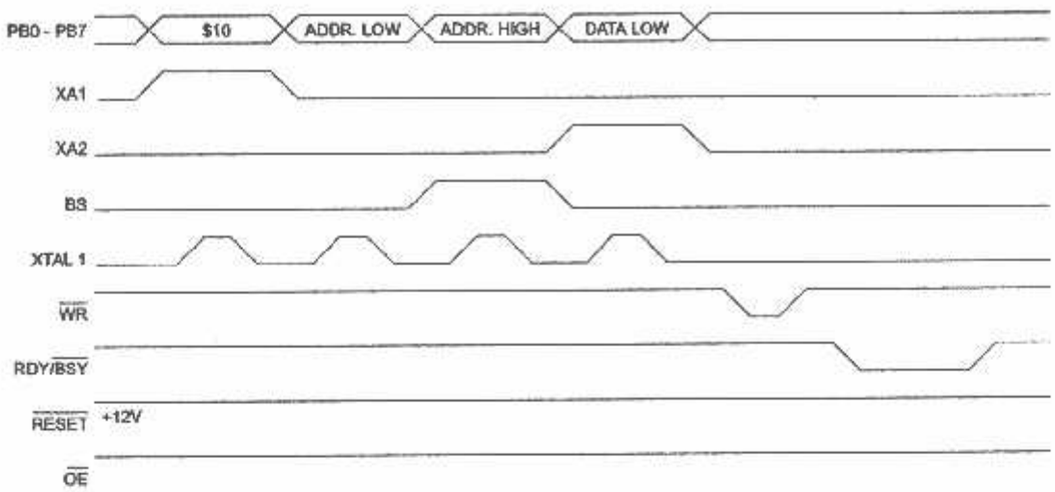
Write Data High byte

1. Set BS to '1'.
2. Give $\overline{\text{WR}}$ a negative pulse. This starts programming of the data byte. RDY / $\overline{\text{BSY}}$ goes low.
3. Wait until RDY / $\overline{\text{BSY}}$ goes high to program the next byte.

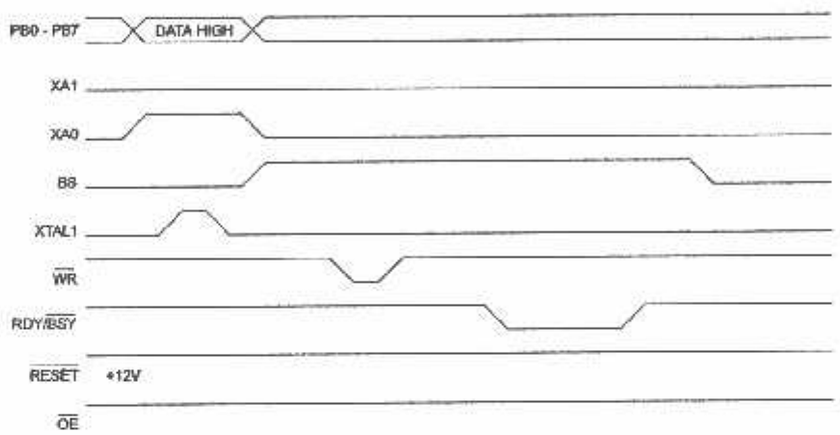
The loaded command and address are retained in the device during programming. To simplify programming, the following should be considered.

- The command for Flash programming needs only be loaded before programming of the first byte.
- Address High byte needs only be loaded before programming a new 256 word page in the Flash.

ure 64. Programming Flash Low Byte



ure 65. Programming Flash High Byte



›gramming the EEPROM

› programming algorithm for the EEPROM data memory ıs follows (refer to Flash Programming for details on ımmand, Address and Data loading):

Load Command '0001 0001'.

Load Low EEPROM Address ($00 - $FF)

Load High EEPROM Address ($00 - $01). Only needed for AT90S8535.

Load Low EEPROM Data ($00 - $FF)

Give $\overline{WR}$ a negative pulse and wait for RDY/$\overline{BSY}$ to go high.

› Command needs only be loaded before programming first byte.

Reading the Flash

The algorithm for reading the Flash memory is as follows (refer to Flash Programming for details on Command, Address and Data loading):

1. Load Command '0000 0010'.
2. Load Low Address ($00 - $FF)
3. Load High Address ($00 - $07/$0F)
4. Set $\overline{OE}$ to '0', and BS to '0'. The Low Data byte can now be read at PB(7:0)
5. Set BS to '1'. The High Data byte can now be read from PB(7:0)
6. Set $\overline{OE}$ to '1'.

The Command needs only be loaded before reading the first byte.

ıding the EEPROM

ɜ algorithm for reading the EEPROM memory is as fol-
ʻs (refer to Flash Programming for details on Command,
dress and Data loading):

Load Command '0000 0011'.

Load Low EEPROM Address ($00 - $FF)

Load High EEPROM Address ($00 - $01). Only needed for AT90S8535.

Set $\overline{OE}$ to '0', and BS to '0'. The EEPROM Data byte can now be read at PB(7:0)

Set $\overline{OE}$ to '1'.

ɜ Command needs only be loaded before reading the l byte.

ıgramming the Fuse Bits

ɜ algorithm for programming the Fuse bits is as follows fer to Flash Programming for details on Command, dress and Data loading):

Load Command '0100 0000'.

Load Data.
Bit 5 = '0' programs the SPIEN Fuse bit. Bit 5 = '1' erases the SPIEN Fuse bit.
Bit 0 = '0' programs the FSTRT fuse bit. Bit 5 = '1' erases the FSTRT fuse bit.

Give $\overline{WR}$ a negative pulse, 1 ms wide.

ogramming the Lock Bits

e algorithm for programming the Lock bits is as follows ıfer to Flash Programming for details on Command, dress and Data loading):

Load Command '0010 0000'.

Load Data.
Bit 2 ='0' programs Lock Bit2
Bit 1 ='0' programs Lock Bit1

3. Give $\overline{WR}$ a negative pulse and wait for RDY/$\overline{BSY}$ to go high.

The lock bits can only be cleared by executing a chip erase.

Reading the Fuse and Lock Bits

The algorithm for reading the Fuse and Lock bits is as follows (refer to Flash Programming for details on Command, Address and Data loading):

1. Load Command '0000 0100'.
2. Set $\overline{OE}$ to '0', and BS to '1'. The Status of Fuse and Lock bits can now be read at PB(7:0)
   Bit 7: Lock Bit1 ('0' means programmed)
   Bit 6: Lock Bit2 ('0' means programmed)
   Bit 5: SPIEN Fuse ('0' means programmed)
   Bit 0: FSTRT Fuse ('0' means programmed)
3. Set $\overline{OE}$ to '1'.

Observe especially that BS needs to be set to '1'.

Reading the Signature Bytes

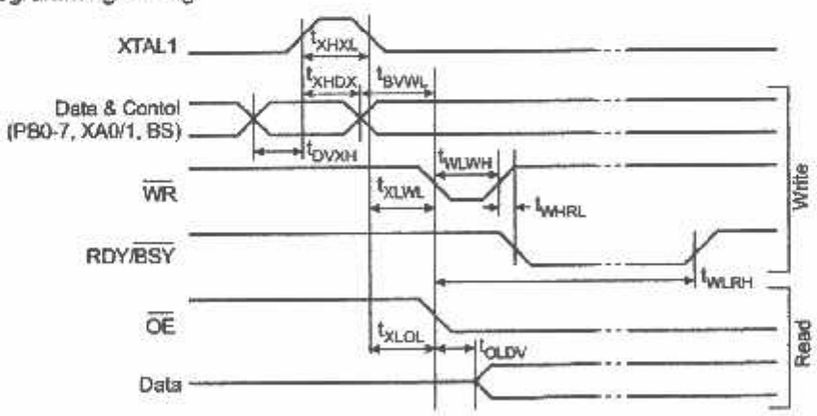
The algorithm for reading the Signature Bytes bits is as follows (refer to Flash Programming for details on Command, Address and Data loading):

1. Load Command '0000 1000'.
2. Load Low address ($00 - $02)
3. Set $\overline{OE}$ to '0', and BS to '0'. The Selected Signature byte can now be read at PB(7:0)
4. Set $\overline{OE}$ to '1'.

The command needs only be programmed before reading the first byte.

rallel Programming Characteristics

ıure 66. Parallel Programming Timing



ɔle 37. Parallel Programming Characteristics
= 21°C to 27°C, V_{CC} = 4.5 - 5.5V

Symbol	Parameter	Min	Typ	Max	Units
t_{DVXH}	Data and Control Setup before XTAL1 High	67			ns
t_{XHXL}	XTAL1 Pulse Width High	67			ns
t_{XLDH}	Data and Control Hold after XTAL1 High	67			ns
t_{BVWL}	BS Valid to $\overline{WR}$ Low	67			ns
t_{WLWH}	$\overline{WR}$ Pulse Width Low	67			ns
t_{WHRL}	$\overline{WR}$ High to RDY/$\overline{BSY}$ Low[1]		20		ns
t_{XLOL}	XTAL1 Low to $\overline{OE}$ Low	67			ns
t_{OLDV}	$\overline{OE}$ Low to Data Valid		20		ns
t_{WLRH}	$\overline{WR}$ Low to RDY/$\overline{BSY}$ High[1]	0.5	0.7	0.9	ms

te: 1. If t_{WPWL} is held longer than t_{WLRH}, no RDY/$\overline{BSY}$ pulse will be seen.

ɔrial Downloading

ɔth the Flash and EEPROM memory arrays can be pro-ɔmmed using the serial SPI bus while $\overline{RESET}$ is pulled to ND. The serial interface consists of pins SCK, MOSI put) and MISO (output). After $\overline{RESET}$ is set low, the Pro-ɔmming Enable instruction needs to be executed first fore program/erase operations can be executed.

hen programming the EEPROM, an auto-erase cycle is ilt into the self-timed programming operation (in the rial mode ONLY) and there is no need to first execute the ip Erase instruction. The Chip Erase operation turns the ntent of every memory location in both the Program and PROM arrays into $FF.

e Program and EEPROM memory arrays have separate dress spaces:

000 to $07FF/$0FFF for Program memory and $0000 to 0FF/$01FF for EEPROM memory.

her an external system clock is supplied at pin XTAL1 or rystal needs to be connected across pins XTAL1 and AL2.The minimum low and high periods for the serial ck (SCK) input are defined as follows:

w:> 2 XTAL1 clock cycles

gh:> 2 XTAL1 clock cycles

ta Polling

ɔen a new byte has been written and is being pro-ɔmmed into the Flash or EEPROM, reading the address ation being programmed will give the value $FF. At the e the device is ready for a new byte, the programmed ue will read correctly. This is used to determine when next byte can be written. This will not work for the value F, but the user should have the following in mind: As a p-erased device contains $FF in all locations, program-ɔg of addresses that are meant to contain $FF, can be skipped. This does not apply if the EEPROM is re-programmed without chip-erasing the device. In this case, data polling cannot be used for the value $FF, and the user will have to wait at least 4ms before programming the next byte.

Serial Programming Algorithm

To program and verify the AT90S4434/8535 in the serial programming mode, the following sequence is recommended (See four byte instruction formats in Table 38):

1. Power-up sequence:

   Apply power between V_{CC} and GND while $\overline{RESET}$ and SCK are set to '0'. If a crystal is not connected across pins XTAL1 and XTAL2, apply a clock signal to the XTAL1 pin. In some systems, the programmer can not guarantee that SCK is held low during power-up. In this case, $\overline{RESET}$ must be given a positive pulse of at least two XTAL1 cycles duration after SCK has been set to '0'.
2. Wait for at least 20 ms and enable serial programming by sending the Programming Enable serial instruction to pin MOSI/PB5.
3. When issuing the third byte in Programming Enable, the value sent as byte number two ($53), will echo back during transmission of byte number three. In any case, all four bytes in programming enable must be transmitted. If the $53 did not echo back, give SCK a positive pulse and issue a new Programming Enable command. If the $53 is not seen within 32 attempts, there is no functional device connected.
4. If a chip erase is performed (must be done to erase the Flash), wait 10 ms, give $\overline{RESET}$ a positive pulse, and start over from Step 2.

The Flash or EEPROM array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. An EEPROM memory location is first automatically erased before new data is written. Use Data Polling to detect when the next byte in the Flash or EEPROM can be written. In a chip erased device, no $FFs in the data file(s) need to be programmed.

6. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/PB6.
7. At the end of the programming session, $\overline{\text{RESET}}$ can be set high to commence normal operation.
8. Power-off sequence (if needed):
   Set XTAL1 to '0' (if a crystal is not used).
   Set $\overline{\text{RESET}}$ to '1'.
   Turn V_{CC} power off

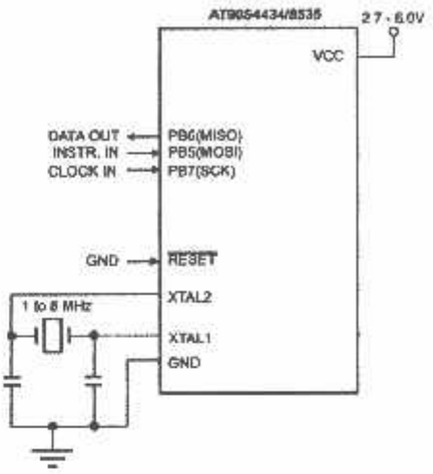
ble 38. Serial Programming Instruction Set

struction	Instruction Format				Operation
	Byte 1	Byte 2	Byte 3	Byte4	
rogramming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx	Enable Serial Programming after $\overline{\text{RESET}}$ goes low.
hip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip erase EEPROM and Flash
ead Program Memory	0010 H000	xxxx aaaa	bbbb bbbb	oooo oooo	Read H(high or low) data o from Program memory at word address a:b
Vrite Program Memory	0100 H000	xxxx aaaa	bbbb bbbb	iiii iiii	Write H(high or low) data i to Program memory at word address a:b
tead EEPROM Memory	1010 0000	xxxx xxxa	bbbb bbbb	oooo oooo	Read data o from EEPROM memory at address a:b
Vrite EEPROM Memory	1100 0000	xxxx xxxa	bbbb bbbb	iiii iiii	Write data i to EEPROM memory at address a:b
ead Lock and Fuse Bits	0101 1000	xxxx xxxx	xxxx xxxx	12Sx xxxF	Read lock and fuse bits. '0': Programmed, '1': Unprogrammed
'rite Lock Bits	1010 1100	111x x21x	xxxx xxxx	xxxx xxxx	Write lock bits. Set bits 1,2='0' to program lock bits.
ead Signature Byte	0011 0000	xxxx xxxx	xxxx xxbb	oooo oooo	Read Signature Byte o at address b
'rite FSTRT Bit	1010 1100	101x xxxF	xxxx xxxx	xxxx xxxx	Write FSTRT fuse. Set bit F='0' to program fuse, '1' to unprogram

e: a = address high bits
b = address low bits
H = 0 - Low byte, 1 - High Byte
o = data out
i = data in

x = don't care
1 = lock bit 1
2 = lock bit 2
F = FSTRT fuse
S = SPIEN fuse

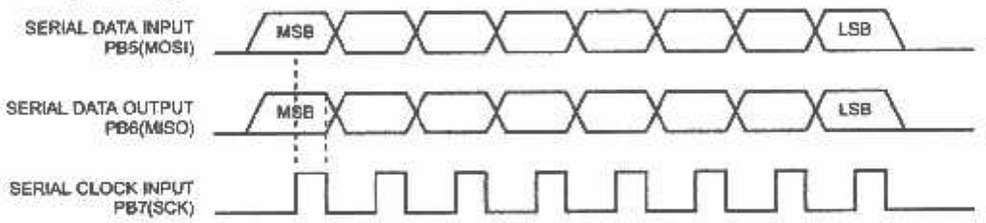
ure 67. Serial Programming and Verify



hen writing serial data to the AT90S4434/8535, data is cked on the rising edge of SCK.

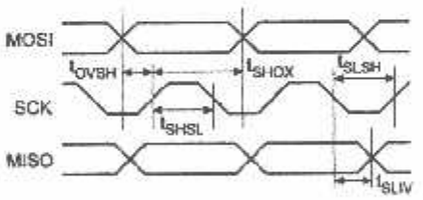
When reading data from the AT90S4434/8535, data is clocked on the falling edge of SCK. See Figure 68 for an explanation.

gure 68. Serial Programming Waveforms



erial Programming Characteristics

gure 69. Serial Programming Timing



ole 39. Serial Programming Characteristics

= -40°C to 85°C, V_{CC} = 2.7 - 6.0V (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency (V_{CC} = 2.7 - 4.0V)	0		4	MHz
t_{CLCL}	Oscillator Period (V_{CC} = 2.7 - 4.0V)	250			ns
$1/t_{CLCL}$	Oscillator Frequency (V_{CC} = 4.0 - 6.0V)	0		8	MHz
t_{CLCL}	Oscillator Period (V_{CC} = 4.0 - 6.0V)	125			ns
t_{SHSL}	SCK Pulse Width High	$2\,t_{CLCL}$			ns
t_{SLSH}	SCK Pulse Width Low	$2\,t_{CLCL}$			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	$2\,t_{CLCL}$			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns

bsolute Maximum Ratings*

)perating Temperature	-40°C to +105°C
torage Temperature	-65°C to +150°C
/oltage on any Pin except $\overline{\text{RESET}}$ with respect to Ground	-1.0V to +7.0V
Aaximum Operating Voltage	6.6V
'O Pin Maximum Current	40.0 mA
Aaximum Current V_{CC} and GND	140.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C Characteristics

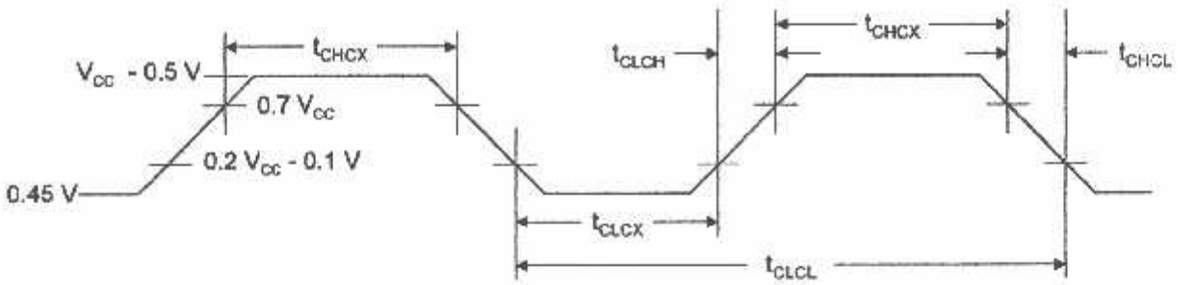
= -40°C to 85°C, V_{CC} = 2.7V to 6.0V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage		-0.5		$0.3V_{CC}$	V
V_{IL1}	Input Low Voltage	XTAL	-0.5		$0.2\ V_{CC}$	V
V_{IH}	Input High Voltage	Except (XTAL, RESET)	$0.6\ V_{CC}$		V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	XTAL	$0.8\ V_{CC}$		V_{CC} + 0.5	V
V_{IH2}	Input High Voltage	RESET	V_{CC}		V_{CC}+0.5	V
V_{OL}	Output Low Voltage (Ports A, B, C, D)	I_{OL} = 20 mA, V_{CC} = 5V I_{OL} = 10 mA, V_{CC} = 3V			0.6 0.5	V V
V_{OH}	Output High Voltage (Ports A, B, C, D)	I_{OH} = 3 mA, V_{CC} = 5V I_{OH} = 1.5 mA, V_{CC} = 3V	4.2 2.3			V V
I_{IL}	Input Leakage (Ports A, B, C, D)	V_{CC} = 6V, pin low	-8.0		8.0	µA
I_{IH}	Input Leakage Current I/O pin	V_{CC} = 6V, pin high	-8.0		8.0	µA
RRST	Reset Pull-Up		100		500	KΩ
$R_{I/O}$	I/O Pin Pull-Up Resistor		35		120	KΩ
I_{CC}	Power Supply Current	Active 4 MHz, 3 V_{CC}			3.0	mA
		Idle 4 MHz, 3 V_{CC}		1.0	1.2	mA
		Power Down 4 MHz, 3 V_{CC} WDT enabled		8.5	15.0	µA
		Power Down 4 MHz, 3 V_{CC} WDT disabled		<1	2.0	µA
V_{ACIO}	Analog Comparator Input Offset Voltage	V_{CC} = 5V			40	mV
I_{ACLK}	Analog Comparator Input Leakage A	V_{CC} = 5V V_{IN} = V_{CC}/2	-50		50	nA
t_{ACPD}	Analog Comparator Propagation Delay	V_{CC} = 2.7V V_{CC} = 4.0V		750 500		ns

tes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 20 mA
Maximum total I_{OL} for all output pins: 80 mA
Port A: 26 mA
Ports A, B, D: 15 mA
Maximum total I_{OL} for all output pins: 70 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V.

.ternal Clock Drive Waveforms



:ternal Clock Drive

ymbol	Parameter	V_{CC} = 2.7V to 4.0V		V_{CC} = 4.0V to 6.0V		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	4	0	8	MHz
t_{CLCL}	Clock Period	250		125		ns
t_{CHCX}	High Time	115		58.3		ns
t_{CLCX}	Low Time	115		58.3		ns
t_{CLCH}	Rise Time		10		4.15	ns
t_{CHCL}	Fall Time		10		4.15	ns

Lampiran D

Surat Pendukung

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

FORMULIR BIMBINGAN SKRIPSI

lama : HADIANSYAH NOOR ROCHIM
IIM : 00.17098
fasa Bimbingan : 03 November 2006 s/d 03 April 2007
udul Skripsi : PERENCANAAN DAN PEMBUATAN OTOMATISASI PROSES *GYNOGENESIS* PADA PEMBIBITAN IKAN MAS (*Cyprinus Carpio*) BERRBASIS ATMEGA 8535

NO	Tanggal	Uraian	Paraf Pembimbing
1	1/2 2007	Bab I — III	
2	28/2 2007	Bab IV + Demo	
3	3/3 2007	Bab V	
4	5/3 2007	Bab V + Lainnya.	
5	17/3 2007	Persiapan Kompre	
6			
7			
8			
9			
10			

Malang,
Dosen Pembimbing I

Ir.F. Yudi Limpraptono,MT.
NIP.Y.1039500274

Form. S – 4b

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

FORMULIR BIMBINGAN SKRIPSI

lama : HADIANSYAH NOOR ROCHIM
IIM : 00.17098
fasa Bimbingan : 03 November 2006 s/d 03 April 2007
udul Skripsi : PERENCANAAN DAN PEMBUATAN OTOMATISASI PROSES *GYNOGENESIS* PADA PEMBIBITAN IKAN MAS (*Cyprinus Carpio*) BERRBASIS ATMEGA 8535

NO	Tanggal	Uraian	Paraf Pembimbing
1		Bab I	
2		Bab II	
3	1/3 '07	Bab III	
4		Bab IV → °C / V	
5		Bab V → Perbaikan.	
6			
7			
8			
9			
10			

Malang,
Dosen Pembimbing II

Soeparno Hadi, ST. MSc.
NIP.Y

Form. S – 4b

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNIK INDUSTRI
JURUSAN TEKNIK ELEKTRO

LEMBAR PERBAIKAN SKRIPSI

Nama Mahasiswa : Hadiansyah Noor Rochim
NIM : 0017098
Jurusan : Teknik Elektro S1
Konsentrasi : Teknik Elektronika
Hari / Tanggal Ujian Skripsi : Jum'at / 23 Maret 2007

No	Materi Perbaikan	Paraf
1.	Jelaskan tentang penggunaan clock 4 M Hz untuk Mikrokontroler ATMEGA	
2.	Integrasikan Nama menjadi satu skematic	
3.	Beri keterangan yang betul untuk schematic	
4.	Tambahkan nama dalam schematic	

Diperiksa / Disetujui :

Penguji II

Dr.Cahyo Crysdianto, MSc
NIP.

Mengetahui :

Pembimbing I

(Ir. F. Yudi Limpraptono, MT)
NIP.1039500274

Pembimbing II

14/4 '07

(Sotyohadi, ST, Msc)
NIP.

PEMERINTAH PROPINSI JAWA TIMUR
DINAS PERIKANAN DAN KELAUTAN

BALAI BENIH IKAN PUNTEN

Jl. Mawar Putih No. 86 Kotak Pos 19 Telp. 591322
KOTA BATU KP. 65301

Batu, 16 Maret 2007

Nomor : 423.4/ 73 /118.056/2007
Sifat : Penting.
Perihal : Pengesahan

Kepada
Yth. Bpk. Ir. F. Yudi Limpraptono MT
Ketua Jurusan Tehnik Elektro S-1
di
MALANG

Dengan hormat

Sesuai dengan hasil penelitian dan Uji coba Alai di Balai Benih Ikan Punten sebagai syarat Ujian skripsi atas mahasiswa :

Nama	: HADIANSYAH NOOR RACHIM
NIM	: 0017098
Fakutas	: Tehnologi Industri
Jurusan	: Tehnik Elektro S-1
Konsentrasi	: Tehnik Elektronika S-1

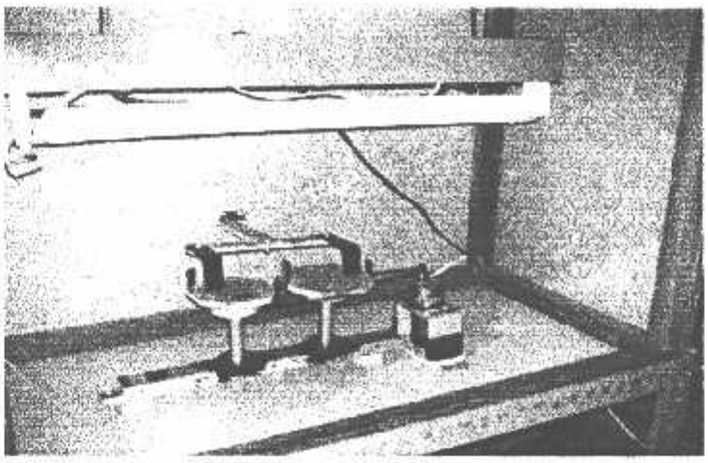
Bahwa penelitian dan uji alat yang diujikan mendukung dama PROSES GYNOGENESIS PADA PEMBIBITAN IKAN MAS *(Cyprinus carpio)* sesuai kalayakan dalam pengujian system alat menyeluruh dapat menekan jumlah larva ikan cacat sebesar 0,85 % dan meningkatkan jumlah larva ikan normal 19,5 %

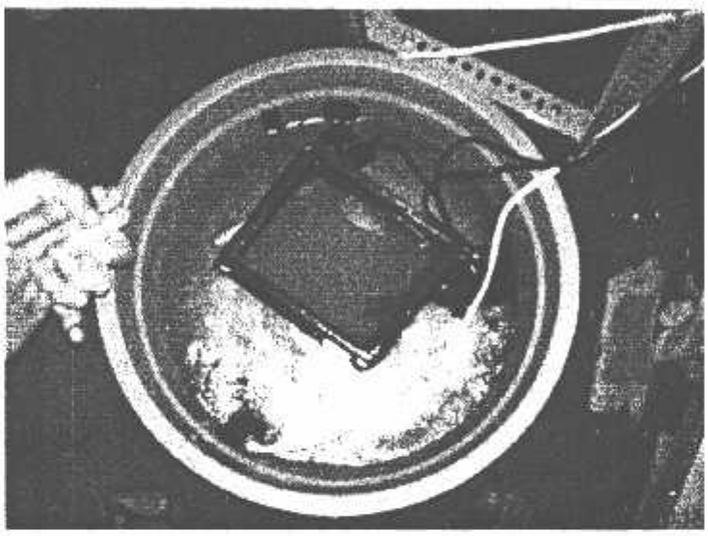
Demikian kami sampaikan untuk menjadikan periksa dan atas perhatiannya diucapkan terima kasih.

KEPALA BALAI BENIH IKAN PUNTEN
KOTA BATU

PEMERINTAH PROPINSI JAWA TIMUR
DINAS PERIKANAN DAN KELAUTAN
BALAI BENIH IKAN PUNTEN
KOTA BATU

Dewi Nur Setyorini, S.Pi
Pembina Muda TK I
NIP : 080 127 177



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