

**INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA**



**PERENCANAAN DAN PEMBUATAN ALAT IROLICS (INTEGRATED
ROAD LIGHTING CONTROL SYSTEM) PADA JALAN TOL BERBASIS
MICROCONTROLLER AT89S51**

SKRIPSI

**Disusun Oleh :
M . RYADMOKO
00.17.104**

SEPTEMBER 2005

LEMBAR PERSETUJUAN



PERENCANAAN DAN PEMBUATAN ALAT IROLICS (INTEGRATED
ROAD LIGHTING CONTROL SYSTEM) PADA JALAN TOL BERBASIS
MICROCONTROLLER AT89S51

SKRIPSI

*Disusun dan diajukan sebagai salah satu syarat untuk memperoleh gelar
Sarjana Teknik Elektronika Strata Satu (S-1)*

Disusun Oleh :

M . RYADMOKO

00.17.104

Diperiksa dan disetujui :

Dosen Pembimbing

(Joseph Dedy Irawan, ST, MT)

NIP. 132315178



Mengetahui :

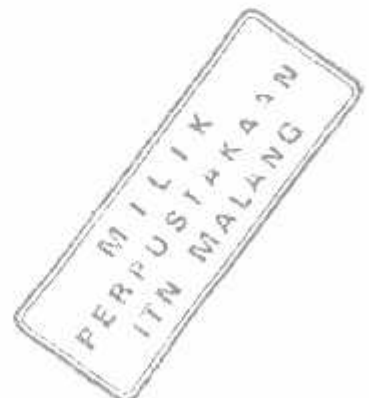
Ketua Jurusan Teknik Elektro S-1

(P. E. Yudi Limpraptono, MT)

NIP. 1 039 500 274

**JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL**

2005





INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO
Jl. Bendungan Sigura-gura No.2
MALANG

**BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI**

Nama : M . Ryadmoko
Nim : 00.17.104
Jurusan : Teknik Elektro
Kosentrasi : Teknik Elektronika S-1
Judul Skripsi : PERENCANAAN DAN PEMBUATAN ALAT
IROLICS (*INTEGRATED ROAD LIGHTING
CONTROL SYSTEM*) PADA JALAN TOL
BERBASIS MICROCONTROLLER AT89S51

Dipertahankan dihadapan Team Penguji Skripsi Jenjang Strata Satu (S – 1) pada :

Hari : RABU
Tanggal : 7 OKTOBER 2005
Nilai : 82 (A)

Panitia Majelis Penguji :

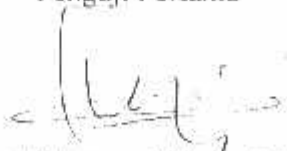
Ketua

(Ir. Mochtar Asroni, MSME)

Sekretaris

(Ir. F. Yudi Kimpriptono, MT)

Anggota Penguji

Penguji Pertama

(Ir. Sidik Noertjahjono, MT)

Penguji Kedua

(Cahyo Crysdian, Msc)

ABSTRAKSI

PERENCANAAN DAN PEMBUATAN ALAT IROLICS (INTEGRATED ROAD LIGHTING CONTROL SYSTEM) PADA JALAN TOL BERBASIS MICROCONTROLLER AT89S51

(M . Ryadmoko, NIM : 0017104, Teknik Elektro/Elektronika S-1, 61 halaman)

(Dosen Pembimbing : Joseph Dedy Irawan, ST, MT)

Kata Kunci : *Microcontroller AT89S51, Jalan tol.*

Dalam skripsi ini dibahas suatu perencanaan dan pembuatan alat pengatur lampu sekaligus pemonitor kondisi lampu jalan pada jalan tol dengan menggunakan teknologi mikrokontroller dari keluarga ATMEL AT89S51. Dengan menggunakan teknologi ini diharapkan dapat membuat suatu sistem kendali dan monitor kondisi lampu dan keadaan cuaca (khususnya cahaya disekitar lampu tersebut) yang terintegrasi dengan pihak pengelola jalan tol.

Perencanaan alat yang direncanakan meliputi sensor cahaya berupa LDR, pengkondisi sinyalnya berupa IC OP-AMP dan IC ADC 0804, Microcontroller AT89S51 sebagai pusat pengontrolnya, transistor BD 139 sebagai buffer penggerak relay, RS-485 sebagai komunikasi serial antara Microcontroller dengan PC. Dan Sebagai monitoring sytem-nya adalah berupa program PC berbahasa DELPHI yang berada pada kantor pengelola jalan tol, PT. JASA MARGA.

KATA PENGANTAR

Alhamdulillah, dengan memanjatkan puji syukur kehadiran Allah SWT, yang telah memberikan rahmat, hidayah serta karunia-Nya, tak lupa sholawat dan salam kepada nabi Muhammad saw. dan keluarganya, akhirnya penyusun dapat dapat menyelesaikan skripsi ini yang berjudul **“PERENCANAAN DAN PEMBUATAN ALAT IROLICS (INTEGRATED ROAD LIGHTING CONTROL SYSTEM) PADA JALAN TOL BERBASIS MICROCONTROLLER AT89S51”**, laporan skripsi ini merupakan salah satu persyaratan kelulusan Program Strata 1 Teknik Elektro Konsentrasi Elektronika Institut Teknologi Nasional Malang.

Keberhasilan penyusunan laporan skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terimakasih kepada:

1. Bapak dan Ibu tercinta yang selalu memberikan kasih sayang, do’a restu, dukungan dan bantuan secara moril maupun materiil kepada penyusun, semenjak penyusun dilahirkan didunia ini.
2. Bapak Dr. Ir. Abraham Lomi, MSFE. selaku Rektor Institut Teknologi Nasional Malang.
3. Bapak Ir. F. Yudi Limpraptono, MT. selaku Ketua Jurusan Teknik Elektro S-1 Institut Teknologi Nasional Malang
4. Bapak Joseph Dedy Irawan, ST, MT. selaku Dosen Pembimbing.
5. Teman-teman yang telah memberikan motifasi serta bantuan baik berupa tenaga maupun fikiran dalam proses penyelesaian skripsi ini.

Penyusun telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam penyelesaian laporan ini. Untuk itu penyusun mengharapkan saran dan kritik yang bersifat membangun demi kesempurnaan laporan ini.

Malang, September 2005

Penyusun

DAFTAR ISI

HALAMAN JUDUL.....	i
LEMBAR PENGESAHAN.....	ii
ABSTRAKSI.....	iii
KATA PENGANTAR.....	iv
DAFTAR ISI.....	vi
DAFTAR GAMBAR.....	xi
DAFTAR TABEL.....	xiii
BAB I PENDAHULUAN.....	1
1.1 Latar Belakang.....	1
1.2 Rumusan Masalah.....	2
1.3 Batasan Masalah.....	2
1.4 Tujuan.....	3
1.5 Metodologi.....	3
1.6 Sistematika Pembahasan.....	3
 BAB II LANDASAN TEORI.....	5
2.1 LDR.....	5
2.2 TRANSISTOR.....	7
2.3 OP - AMP (LM-324).....	9
2.4 ADC 0804 (Analog to Digital Converter).....	12
2.5 IC MICROCONTROLLER (AT89S51).....	13

2.5.1	Perangkat Keras Microcontroller AT89S51.....	15
2.5.2	Arsitektur Microcontroller AT89S51.....	16
2.5.3	Konfigurasi Pena-pena Microcontroller AT89S51.....	17
2.5.4	Organisasi memori.....	22
2.5.5	Special Function Register.....	26
2.5.6	Program Status Word.....	27
2.5.7	Power Control Register.....	28
2.5.8	Metode Pengalamatan.....	29
2.5.9	Siklus Mesin (Machine Cycle).....	30
2.5.10	Pewaktuan CPU.....	33
2.6	<i>Standart Interface RS-485 (IC SN751176)</i>	34
2.7	IC MAX 232.....	35
2.8	RELAY.....	37

BAB III PERENCANAAN DAN PEMBUATAN ALAT..... 38

3.1	Perancangan Perangkat Keras.....	38
3.2	Rangkaian Sensor.....	40
3.3	Rangkaian OP-AMP Sebagai Komparator.....	41

3.4	Rangkaian OP- AMP sebagai BUFFER (penyangga)	42
3.5	Rangkaian ADC 0804	43
3.6	Rangkaian Minimum System Microcontroller AT89S51	43
3.6.1	Rangkaian Clock	44
3.6.2	Rangkaian Reset	45
3.6.3	Konfigurasi Kaki Microcontroller AT89S51	46
3.7	Rangkaian Driver Bagi Relay	48
3.8	Rangkaian RS-485 (IC SN75176)	49
3.9	Rangkaian IC MAX 232	49
3.10	Perencanaan Software	50
3.10.1	Perencanaan Software Pada Unit IROLICS	50
3.10.2	Perencanaan Sotware Pada Pusat IROLLICS	53
BAB IV PENGUJIAN DAN ANALISA ALAT		54
4.1	Pengujian Rangkaian Senor Cahaya	54
4.2	Pengujian Pengkondisi Sinyal	56
4.2.1	Op-Amp sebagai Buffer	56
4.2.2	Pengujian Op-Amp Sebagai Komparator	57

4.3. Pengujian Rangkaian Driver Relay	58
4.4. Pengujian Secara Keseluruhan	58
BAB V PENUTUP	60
5.1 Kesimpulan	60
5.2 Saran	60
DAFTAR PUSTAKA	61
LAMPIRAN-LAMPIRAN	

DAFTAR GAMBAR

2.1	Bentuk Fisik LDR.....	6
2.2	Simbol LDR	6
2.3	Rangkaian Transistor Sederhana.....	7
2.4	Karakteristik Ic-Vce Transistor Bipolar.....	8
2.5	Transistor BD 139.....	9
2.6	Konfigurasi LM 324.....	11
2.7	A D C 0804	12
2.8	Blok Diagram Microcontroller AT89S51	16
2.9	Konfigurasi Pena-pena Microcontroller AT 89S51	17
2.10	Organisasi Program Memory.....	23
2.11	Data Memori.....	26
2.12	Urutan siklus keadaan Duty Cycle.....	31
2.13	Siklus bus pada pengaksesan memori Program Eksternal.....	32
2.14	Menggunakan Oscilator Internal.....	33
2.15	Menggunakan Sumber Clock Eksternal	34
2.16	Konfigurasi pin IC SN751176	35
2.17	Konfigurasi pin IC MAX 232	36
2.18	Jenis-jenis relay	37
3.1	Diagram Blok Rangkaian keseluruhan.....	39
3.2	Rangkaian Sensor.....	40
3.3	O P – Amp sebagai komparator.....	41
3.4	OP – AMP sebagai buffer.....	42
3.5	Rangkaian ADC 0804	43
3.6	Rangkaian Clock	44

3.7	Rangkaian Reset.....	45
3.8	Konfigurasi kaki-kaki AT89S51 pada IROLICS.....	47
3.9	Rangkaian Driver bagi relay	48
3.10	Rangkaian IC SN75176.....	49
3.11	Rangkaian IC MAX 232.....	49
3.12	Flowchart Pemograman Microcontroller 1.....	51
3.13	Flowchart Pemograman Microcontroller 2.....	52
3.14	Flowchart Pemograman Delphi	53
4.1	Rangkaian Tes sensor.....	54
4.2	Rangkain Uji Buffer.....	56
4.3	Data Out Put Komparator.....	57
4.4	Rangkaian Driver Relay	58

DAFTAR TABEL

2.1	Data Karakteristik LDR	6
2.2	<i>Register Bank</i>	26
2.3	<i>Special Function Register (SFR)</i>	27
4.1	Hasil Pengukuran Rangkaian sensor	55
4.2	Hasil pengujian OP AMP sebagai buffer	56
4.3	Data output Komparator	57
4.4	Hasil Pengujian Untuk Mengetahui Respon Dari Driver Relay	58
4.5	Hasil Pengujian unit IROLICS	59
4.6	Hasil Pengujian Pusat IROLICS	59

BAB 1

PENDAHULUAN

1.1. Latar Belakang

Seiring dengan makin banyaknya kendaraan bermotor, khususnya kendaraan roda empat maka lalu lintas jalan raya akan menjadi semakin macet. Oleh sebab itu, jalan tol merupakan salah satu jalan alternatif yang bebas hambatan bagi para pengguna kendaraan roda empat sebagai akses ke suatu daerah tertentu yang dijangkau oleh jalan tol tersebut. Kenyamanan yang diberikan kepada para pengguna kendaraan oleh jalan tol selain sebagai jalan bebas hambatan adalah lampu penerangan jalan pada khususnya pada malam hari. Meskipun kelihatan sepele, tetapi hal tersebut sangatlah berpengaruh terhadap kelancaran berkendara. Dan apabila hal tersebut tidak diperhatikan maka akan meningkatkan resiko kecelakaan bagi para pengguna jalan tol.

Berdasarkan hal tersebut, maka perlu dipasang suatu alat sistem pemantau padam atau tidaknya lampu penerangan jalan pada jalan tol secara otomatis. Yang mana sistem tersebut akan terintegrasi dengan pihak pengelola jalan tol. Sistem tersebut akan memberitahu pihak pengelola jalan tol, lampu jalan nomer berapa (posisi mana) yang masih menyala atau padam.

1.2. Rumusan Masalah

Berdasarkan permasalahan tersebut diatas, maka bagaimana cara membuat suatu alat yang dapat memberikan fasilitas untuk memantau padam atau tidaknya lampu penerangan pada jalan tol secara otomatis.

1.3. Batasan Masalah

Untuk memberikan pembahasan yang jelas maka diberikan ruang lingkup pembatasan masalah sebagai berikut :

- Perencanaan perangkat keras (hardware) yang meliputi LDR, OP-AMP LM324 dan ADC 0804 sebagai pengkondisi sinyal, RS 485 sebagai komunikasi serial dan kontrol dari IC Microcontroller AT89S51.
 - Perencanaan dan pembuatan perangkat lunak (software) untuk IC Microcontroller AT89S51 dengan menggunakan bahasa Assambler dan bahasa Delphi untuk PC (Personal Komputer).
 - Dalam rangkaian dianggap catu daya konstan dan tidak akan dibahas.
 - Tidak membahas Software.
 - Tidak membahas REPEATER .
 - Tidak membahas komunikasi serial.
-

1.4. Tujuan

- Tujuan dari perencanaan dan pembuatan alat IROLICS (Integrated Road Lighting Control System) pada jalan tol berbasis microcontroller AT89S51 ini adalah untuk memberikan efisiensi kerja pihak pengelola jalan tol khususnya PT. Jasa Marga.
- Untuk menambah keamanan dan kenyamanan bagi pengguna jalan tol.

1.5. Metodologi

Untuk mencapai tujuan dari skripsi ini, maka metodologi dalam skripsi ini adalah sebagai berikut :

1. Studi Literatur.
2. Studi Lapangan.
3. Perencanaan dan pembuatan perangkat keras (*hardware*) dan perangkat lunak (*software*).
4. Pengujian dan analisa alat yang dibuat.
5. Penyusunan laporan skripsi.

1.6. Sistematika Pembahasan

Dalam penyusunan skripsi ini, sistematika pembahasan yang digunakan adalah sebagai berikut :

BAB I PENDAHULUAN

Bab ini membahas mengenai latar belakang, rumusan masalah, batasan masalah, tujuan, metodologi dan sistematika pembahasan.

BAB II LANDASAN TEORI

Bab ini membahas mengenai dasar – dasar teori sebagai teori penunjang pada alat yang akan dirancang. Disamping itu juga sebagai pelengkap pemahaman mengenai bagian – bagian atau keseluruhan sistem.

BAB III PERENCANAAN DAN PEMBUATAN ALAT

Bab ini membahas mengenai perencanaan dan pembuatan alat yang terdiri dari perangkat keras (*hardware*) dan perangkat lunak (*software*).

BAB IV PENGUJIAN DAN ANALISA ALAT

Bab ini mengulas tentang hasil pengujian dan analisa alat yang telah dibuat.

BAB V PENUTUP

Bab ini berisikan kesimpulan akhir dari keseluruhan alat yang telah dibuat dan saran dari penyusun demi pengembangan selanjutnya dari alat yang telah dibuat.

BAB II

LANDASAN TEORI

Untuk dapat memahami alat yang akan dirancang ini maka dalam bab II ini dijelaskan mengenai teori dasar yang berkaitan dengan sistem ini, diantaranya meliputi: LDR, TRANSISTOR (BD 139), IC OP-AMP (LM 324), IC ADC (0804), IC MICROCONTROLLER (AT89S51), IC SN75176, IC MAX 232 serta RELAY.

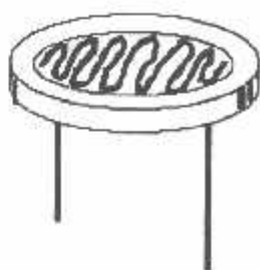
2.1. LDR

LDR adalah suatu komponen elektronika yang bersifat variable resistif, dimana nilai resistansinya dipengaruhi oleh intensitas cahaya yang diterimanya.

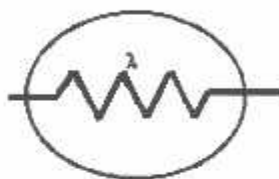
Bila LDR dibawa dari ruangan dengan intensitas cahaya tinggi ke ruangan dengan intensitas cahaya yang lemah atau sebaliknya, maka nilai resistansinya akan berubah secara perlahan-lahan dalam selang waktu tertentu .

Laju perubahan merupakan ukuran yang paling tepat untuk menunjukkan perubahan resistansi dalam selang waktu tertentu. Besar laju perubahan yang diberikan dinyatakan dalam satuan $K\Omega/\text{detik}$..

Dalam aplikasi rangkaian elektronika, LDR banyak dipakai sebagai alat pengindra cahaya. Penggunaannya antara lain sebagai saklar cahaya, mengukur intensitas cahaya dan lain-lain.



Gambar 2-1. Bentuk fisik LDR



Gambar 2-2. Simbol LDR

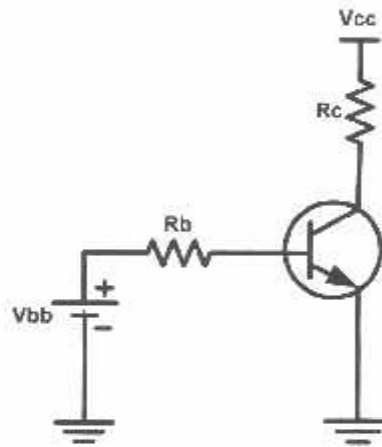
Tabel 2-1. Data karakteristik LDR

Spesifikasi	Nilai
1. Resiatansi gelap (RD)	>10 MΩ
2. Resistansi terang	75-300 Ω
3. Laju perubahan	>200 KΩ/detik
4. Disipasi daya	0,1 Watt
5. Jangkauan temperatur lingkungan	-30°C - 60°C

Sumber : TEDC Bandung, Teknologi komponen I, Hal 7, 15

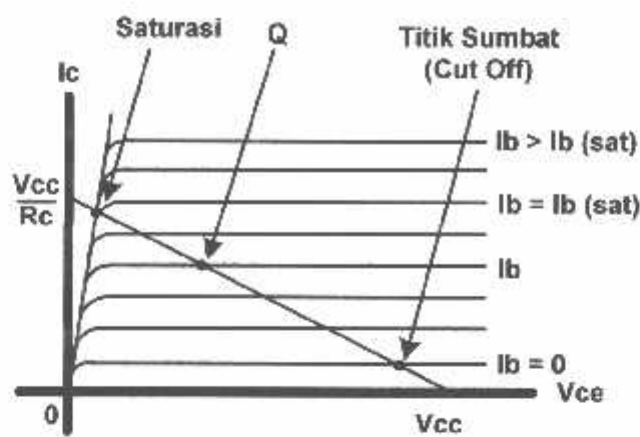
2.2. TRANSISITOR (BD 139)

Transistor merupakan sebuah komponen semikonduktor yang banyak digunakan pada berbagai rangkaian elektronik baik sebagai penguat, saklar, dan lain-lain. Asas kerja dari transistor adalah akan ada arus yang mengalir diantara terminal kolektor – emitor (I_C) hanya apabila ada arus yang mengalir diantara terminal basis – emitor (I_B). Jadi transistor harus dioperasikan pada daerah linier agar diperoleh sinyal keluaran yang tidak cacat (distorsi). Untuk dapat mengoperasikan secara tepat maka pengertian tentang titik kerja transistor amatlah penting dan harus pahami dan dimengerti dengan benar.



Gambar 2-3. Rangkaian Switching Transistor

Garis beban akan memotong sekelompok kurva arus basis constant I_B dengan I_B tertentu (yang diatur rangkaian bias), garis beban akan memotong kurva I_B tersebut di titik Q yang disebut titik kerja transistor. Titik kerja ini menjadi kondisi awal dari pengoperasian transistor kelak dimana transistor tersebut mempunyai tiga daerah kerja yaitu aktif (*active*), jenuh (*saturation*), dan tersumbat (*cut-off*).



Gambar 2-4. Karakteristik I_C - V_{CE} Transistor Bipolar

Pada gambar diatas dapat dilihat, titik dimana garis beban memotong kurva $I_B = 0$ disebut sebagai titik sumbat (*cut-off*). Pada titik ini arus kolektor(I_C) sangat kecil (hanya arus bocor) sehingga dapat diabaikan, disini transistor kehilangan kerja normalnya. Disini dapat dikatakan bahwa tegangan kolektor-emitor sama dengan ujung dari garis beban tersebut.

$$V_{CE(cut-off)} \cong V_{CC}$$

Perpotongan garis beban dengan kurva $I_B = I_{B(sat)}$ disebut titik jenuh (*saturation*). Pada titik ini arus kolektor maksimum atau dapat dikatakan bahwa arus kolektor sama dengan ujung dari garis beban.

$$I_{C(sat)} \cong \frac{V_{CC}}{R_C}$$

Jika arus basis I_B lebih kecil dari $I_{B(sat)}$ maka transistor akan beroperasi pada daerah aktif, yaitu titik kerjanya terletak disepanjang garis beban.

Jadi disimpulkan bahwa transistor bipolar bekerja sebagai suatu sumber arus (penguat) dimana saja sepanjang garis beban, kecuali titik jenuh (*saturation*)

atau titik sumbat (*cut-off*) dimana transistor tidak lagi bekerja sebagai sumber arus (penguat) melainkan sebagai saklar (*switching*).



Gambar 2-5. Transistor BD 139

2.3. OP-AMP (LM 324)

Op-Amp IC adalah perangkat *solid-state* yang mampu mengindera dan memperkuat sinyal masukan baik sinyal DC maupun AC. Op-Amp yang khas terdiri dari tiga rangkaian dasar, yaitu penguat diferensial impedansi masukan tinggi, penguat tegangan penguatan tinggi, dan penguat keluaran impedansi rendah (*common emitter push-pull*). Keluarannya dapat berayun positif atau negatif karena catu dayanya *dual trace*.

Op-Amp yang ideal mempunyai karakteristik sebagai berikut:

- Penguatnya terkopel langsung.
- Impedansi masukannya (Z_i) sangat tinggi dapat dikatakan tak terhingga. Lazimnya berkisar 1 Mohm.
- Impedansi keluarannya (Z_o) = 0. namun pada kenyataanya berkisar antara 100-200 ohm.
- Penguatan arusnya sangat tinggi, sckitar 10^5 atau 100 dB.
- Tegangan keluaran = 0, jika tegangan masukan = 0

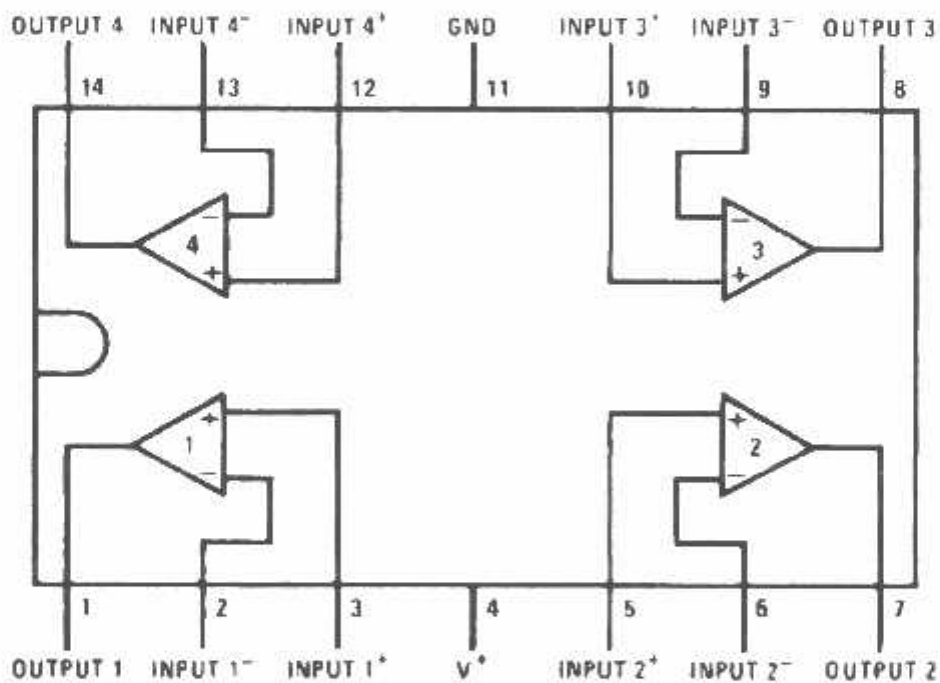
- Tegangan keluran dapat berayun kearah positif atau negatif.

OP-AMP dapat dihubungkan dalam lingkaran terbuka atau tertutup. Dalam lingkaran terbuka OP-AMP memiliki orde penguatan sampai seratusribu kali. OP-AMP dibuat dalam bentuk IC (integrated circuit) sehingga praktis dan mudah penggunaannya.

OP-AMP memiliki dua inputan inverting(membalik) dan non-inverting(tak membalik) yang saling berlawanan. Jika isyarat masukan dihubungkan ke masukan inverting maka pada daerah frekuensi tengah isyarat keluaran berlawanan fasa dengan isyarat masukan. Sebaliknya jika isyarat masukan dihubungkan ke masukan non-inverting maka isyarat keluaran akan sefasa dengan isyarat masukan. Jika OP-AMP sebagai penguat maka harus menghubungkan OP-AMP dengan lingkaran tertutup dengan memasang R_f yaitu tahanan feedback. Seri LM 324 ini terdiri dari empat buah Op-Amp dalam satu keping IC, mempunyai penguatan yang tinggi, dan dikhususkan untuk single power supply yang diperluas range tegangannya. Aplikasinya digunakan sebagai penguat transduser, blok penguat DC, dan semua rangkaian konvensional Op-Amp, yang sekarang lebih mudah diterapkan dalam sistem single power, seperti contohnya pada seri LM324 ini dapat dioperasikan pada tegangan ± 5 volt dc yang biasanya dipakai pada sistem digital.

Kelebihan LM 324 antara lain :

- ❖ hanya membutuhkan satu power supply
- ❖ jangkauan power supply yang lebar :
 - untuk single : 3 V – 32 V
 - untuk dual : ± 1.5 V - ± 16 V
- ❖ empat buah op-amp dalam satu keping IC
- ❖ kompatibel dengan semua jenis logika
- ❖ arus drain rendah (700 μ A)
- ❖ arus bias rendah 400 nA



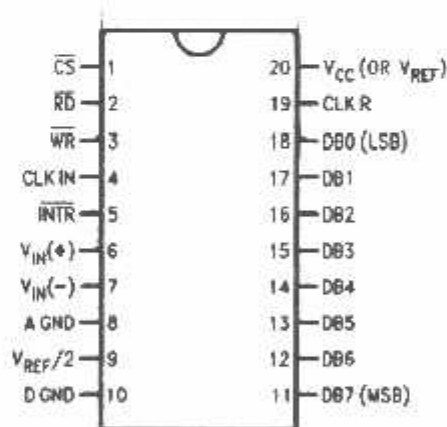
Gambar 2-6. konfigurasi LM-324

2.4. ADC 0804 (Analog to Digital Converter)

Analog to Digital Converter (ADC) adalah rangkaian atau devais yang mengubah input analog menjadi output digital dalam bentuk biner yang ekuivalen. Dalam setiap perubahan pada output menyatakan beberapa kenaikan dari tegangan atau arus input.

Spesifikasi penting lain selain ketelitian (akurasi) dan linieritas adalah waktu konversi (conversion time). Waktu konversi ADC adalah waktu yang diperlukan ADC untuk menghasilkan kode biner yang valid untuk tegangan masukan yang diberikan. Semakin pendek waktu konversi berarti kecepatan konversi semakin tinggi.

ADC 0804 adalah ADC yang mempunyai resolusi 8 bit dengan keluaran data paralel dan telah dilengkapi dengan clock internal. ADC ini dapat menerima tegangan input antara 0 – 5 volt.



Gambar 2-7. ADC0804

Dalam proses konversi ADC, perlu diperhatikan beberapa parameter yang akan menentukan mutu sebuah ADC, yaitu :

- Kesalahan kuantitas
- Ketidaklinieran
- Kode tidak lengkap (hilang)
- Waktu konversi

Karakteristik yang linier didekati dengan karakteristik dalam bentuk anak tangga sehingga timbul kesalahan kuantitasi sebesar setengah dari anak tangga. Karena tinggi anak tangga adalah sama dengan bit paling terendah (least significant, LSB) dalam bilangan biner, maka kesalahan tersebut sama $\frac{1}{2}$ LSB.

Kadang-kadang kombinasi bit tertentu tidak tersedia dengan perkataan lain sebuah tangga dilompati. Kombinasi semacam itu disebut kode yang hilang (missing code). Kode yang hilang terjadi bila kesalahan linieritas kurang dari $\frac{1}{2}$ LSB. Waktu yang dibutuhkan oleh ADC untuk mengubah tegangan menjadi bit kombinasi disebut waktu konversi (conversion time).

2.5. IC MICROCONTROLLER (AT89S51)

Perbedaan yang mendasar antara mikrokontroler dan mikroprosesor adalah mikrokontroler selain memiliki CPU (*Central Processing Unit*) juga dilengkapi dengan memori dan port I/O (*Input/Output*) yang merupakan kelengkapan sebagai sistem minimum mikrokomputer sehingga sebuah mikrokontroler dapat dikatakan sebagai mikro komputer dalam keping tunggal (*Single Chip Microcomputer*). Mikroprosesor adalah bagian dari CPU dari sebuah

komputer, tanpa memori, tanpa perangkat I/O dan tanpa periferal yang dibutuhkan oleh suatu sistem lengkap. Untuk dapat bekerja, mikroproscsor membutuhkan perangkat pendukung yang dapat berupa RAM (*Random Access Memory*), ROM (*Read Only Memory*) dan perangkat I/O.

Mikrokontroller AT89S51 adalah mikrokontroller keluaran Atmel yang kompatibel penuh dengan mikrokontroler keluarga MCS-51 lainnya. Mikrokontroler AT89S51 merupakan hasil pengembangan dan penyempurnaan dari mikrokontroler AT89C51. Mikrokontroler AT89S51 merupakan CMOS yang mengkonsumsi daya relatif rendah, performa tinggi dan dilengkapi dengan *4K byte Flash PEROM (Programmable and Erasable Read Only Memory)* menggunakan *Atmel's High Density Non Volatile Technology* (memori dengan teknologi *non-volatile*), isi memori tersebut dapat diisi ulang ataupun dihapus sampai dengan 1000 kali proses hapus/tulis.

Memory ini biasa digunakan untuk menyimpan instruksi (perintah) berstandar *MCS-51 code* sehingga memungkinkan mikrokontroller ini untuk bekerja dalam mode *single chip operation* (mode operasi keping tunggal) yang tidak memerlukan *external memory* (memori luar) untuk menyimpan *source code* tersebut.

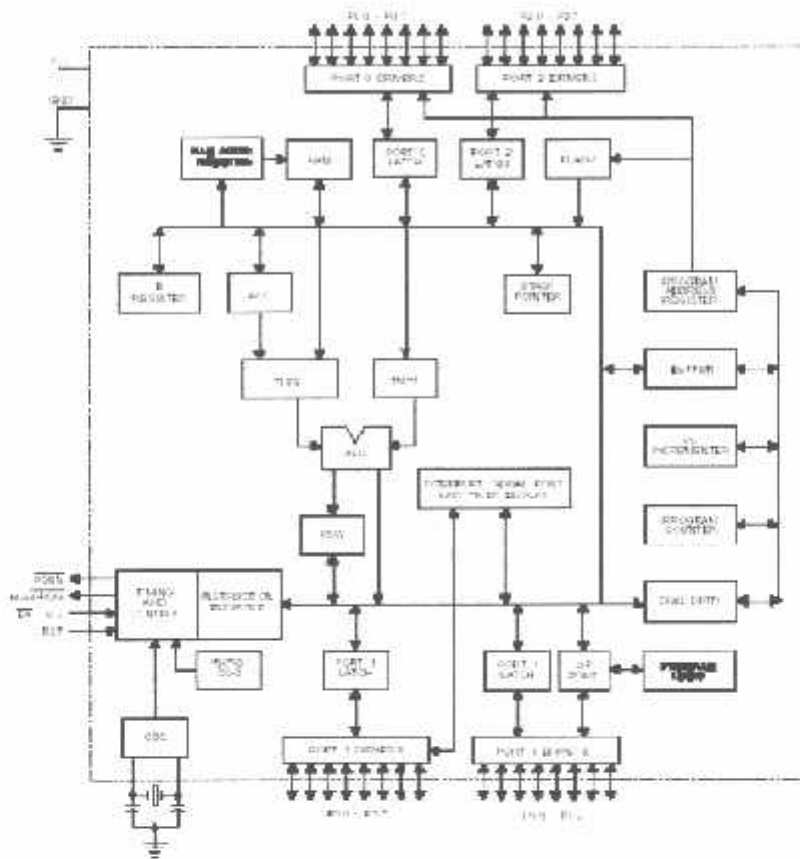
Dalam sistem mikrokontroller terdapat dua hal yang mendasar, yaitu perangkat keras dan perangkat lunak yang mana keduanya saling terkait dan saling mendukung.

2.5.1. Perangkat Keras Mikrokontroller AT89S51

Mikrokontroller AT89S51 secara umum memiliki spesifikasi data teknis dan fasilitas sebagai berikut :

- a. CPU 8-bit berstandart MCS-51.
- b. RAM internal 128 byte (128 X 8 bit), *on chip*
- c. 4 buah port I/O yang dapat diprogram.
- d. Dua *timer* dan *counter* 16 bit.
- e. Enam *Interrupt Sources*.
- f. Port *serial interface* yang dapat diprogram.
- g. Terdapat *Low Power Idle* dan *Power Down Modes*.
- h. *Boolean Processor* (dapat melakukan operasi bit).
- i. 210 bit *addressable locations*.
- j. Clock dan Osilator internal 0 – 24 Hz.
- k. Memori 4 Kbyte (*In-system Reprogramable Flash Memory*).

Memungkinkan untuk 1000 kali proses hapus / tulis.



Gambar 2-8. Blok Diagram Mikrokontroler AT89S51

2. 5. 2. Arsitektur Mikrokontroler AT89S51

Arsitektur mikrokontroler AT89S51 adalah sebagai berikut :

- CPU 8-bit dengan register A (*Accumulator*) dan register B, yang optimal untuk aplikasi kontrol.
- 16 bit PC (*Program Counter*) dan DPTR (*Data Pointer*).
- 8 bit PSW (*Program Status Word*).
- 8 bit SP (*Stack Pointer*).
- 4 Kbyte EPROM internal.
- 128 byte RAM internal.

- 4 bank register, masing-masing berisi 8 register.
 - 16 byte yang dapat dialamati pada *bit level*.
 - 80 byte *general purpose memory data*.
- g. 32 pin input – output tersusun atas Port 0 – Port 3, masing-masing 8 bit.
- h. 2 buah *Timer / Counter* 16 bit.
- i. *Receiver / Transmitter* data serial *Full Duplex* : SBUF.
- j. *Control Register*, yaitu TCON, TMOD, SCON, PCON, IP dan IE.
- k. 5 buah sumber interrupt (2 buah sumber interrupt external dan 3 buah interrupt internal).
- l. Osilator dan Clock Internal.

2. 5. 3. Konfigurasi Pena-pena Mikrokontroller AT89S51

Mikrokontroller AT89S51 terdiri atas 40 pin, dengan konfigurasi sebagai berikut :



Gambar 2-9. Konfigurasi Pena-pena Mikrokontroller AT89S51

Fungsi tiap-tiap pin adalah sebagai berikut :

1. VCC (*Supply Tegangan*)

Terhubung pada catu daya + 5 Volt .

2. GND (*Ground*)

Dihubungkan dengan *ground* rangkaian.

3. Port 0 (P0.0 – P0.7)

Port 0 merupakan port I/O serbaguna 8 bit dua arah fungsi ganda yang berada pada pin 32-39 dari mikrokontroler AT89S51. Port ini dapat digunakan sebagai *Low Order Multiplex Address* (A0 – A7) / Data (multipleks bus alamat rendah dan bus data selama pengaksesan ke memori eksternal) ataupun menerima kode byte pada saat *Flash Programming* berlangsung.

Pada fungsi sebagai I/O biasa port ini dapat memberikan output *sink* ke delapan buah TTL input atau dapat diubah sebagai input dengan memberikan logika '1' pada port tersebut.

Pada fungsi *low order multiplex address/data port* ini akan mempunyai *internal pull-up* dan pada saat *Flash Programming* berlangsung diperlukan *external pull-up* terutama pada saat verifikasi program.

4. Port 1 (P1.0 – P1.7)

Merupakan port I/O dua arah biasa atau menerima *low order address byte* selama pada saat *Flash Programming* berlangsung.

Port ini dilengkapi dengan *internal pull-up* dan berfungsi sebagai input dengan memberikan logika '1'.

Sebagai output port ini dapat memberikan *output sink* keempat buah input TTL. Port ini berfungsi sebagai input atau output dan bekerja baik untuk operasi bit maupun byte, tergantung dari pengaturan *software* dan berada pada pin 1-8.

5. Port 2 (P2.0 – P2.7)

Merupakan port I/O dua arah biasa atau sebagai *high order address* (A8-A15) selama pengambilan (*fetching*), pada saat mengakses memori secara 16 bit (MOVX @DPTR) dari memori eksternal dan menerima beberapa sinyal kontrol selama pemrograman dan verifikasi.

Pada saat mengakses memori secara 8 bit, (MOVX @RN) port ini akan mengeluarkan isi dari P2 *Special Function Register*.

Port ini mempunyai *internal pull-up* dan berfungsi sebagai input dengan memberikan logika '1'. Sebagai output port ini dapat memberikan *output sink* keempat buah input TTL, dengan *internal pull-up*. Port 2 mengeluarkan *high order* selama pengambilan (*fetching*) program memori eksternal dan selama mengakses data memori eksternal. Port 2 juga menerima *high order address bit*.

6. Port 3 (P3.0 – P3.1)

Port 3 selain memiliki fungsi dan sifat yang sama sebagai I/O dengan *internal pull-up* sama dengan port 1 maupun port 2, juga mempunyai fungsi khusus port 3 ini adalah sebagai berikut :

- RD (P3.7) : *Strobe* baca data memori eksternal
 - WR (P3.6) : *Strobe* tulis data memori eksternal
-

- T1 (P3.5) : Input eksternal timer 1
- T0 (P3.4) : Input eksternal timer 0
- INT1 (P3.3) : Interrupt 1 eksternal
- INT0 (P3.2) : Interrupt 0 eksternal
- TXD (P3.1) : Port output serial
- RXD (P3.0) : Port input serial

7. RST

Input reset pada pin 9 adalah *reset master* untuk AT89S51, reset akan aktif dengan memberikan input high selama 2 *cycle*.

8. ALE (Address Latch Enable) / PROG

Pulsa output ALE digunakan untuk proses *latching byte* adalah address rendah (A0 – A7) selama pengaksesan ke memori eksternal. Pin ini juga merupakan input pulsa program yang aktif rendah (PROG) selama *Flash Programming*.

Sinyal output ALE yang berada pada pin 30 fungsinya dipergunakan untuk demultiplex bus alamat dan bus data. Pada kondisi normal ALE membangkitkan sinyal pulsa sebesar 1/16 frekuensi osilator kecuali pada saat mengakses memori eksternal sinyal clock pada pin ini dapat pula di-*disable* dengan men-set bit 0 dari *Special Function Register* di alamat 8EH.

ALE akan aktif pada saat mengakses memori eksternal (MOVX & MOVC). Juga dapat digunakan sebagai clock dalam aplikasi secara

umum. Jika clock pada mikrokontroler menggunakan x'tal 12 Mhz maka frekuensi sinyal osilator ALE sebesar 1/6 frekuensi sinyal x'tal (2 Mhz).

9. PSEN (*Program Strobe Enable*)

PSEN adalah sebuah sinyal keluaran yang terdapat pada pin 29. Fungsinya adalah sebagai sinyal kontrol untuk memungkinkan mikrokontroler membaca program (*code*) dari memori eksternal. Biasanya pin ini dihubungkan ke pin OE EPROM. Jika eksekusi program dari ROM internal atau *flash memory*, maka PSEN akan berada pada kondisi tidak aktif (*high*). PSEN akan aktif dua kali pada setiap detiknya.

10. XTAL 1 (*Input Oscillator*)

Pin XTAL1 merupakan pin input *inverting oscillator amplifier* dan input rangkaian *internal clock operating*.

11. XTAL 2 (*Output Oscillator*).

Sedangkan pin XTAL2 merupakan pin output dari *inverting oscillator amplifier*.

12. EA / Vpp (*External Access / Programming Supply Voltage*)

Pada kondisi *low* (*di-hold* rendah secara eksternal atau dihubungkan ke *ground*), pin ini akan berfungsi sebagai EA yaitu mikrokontroler akan menjalankan program yang ada pada memori eksternal (0000H – FFFFH) setelah sistem di-*reset*.

Jika berkondisi *high* (pin ini dihubungkan ke VCC), pin ini akan berfungsi untuk menjalankan program yang ada pada memori internal. Pada saat *Flash Programming* berlangsung pin ini akan mendapatkan tegangan 12 volt (VP).

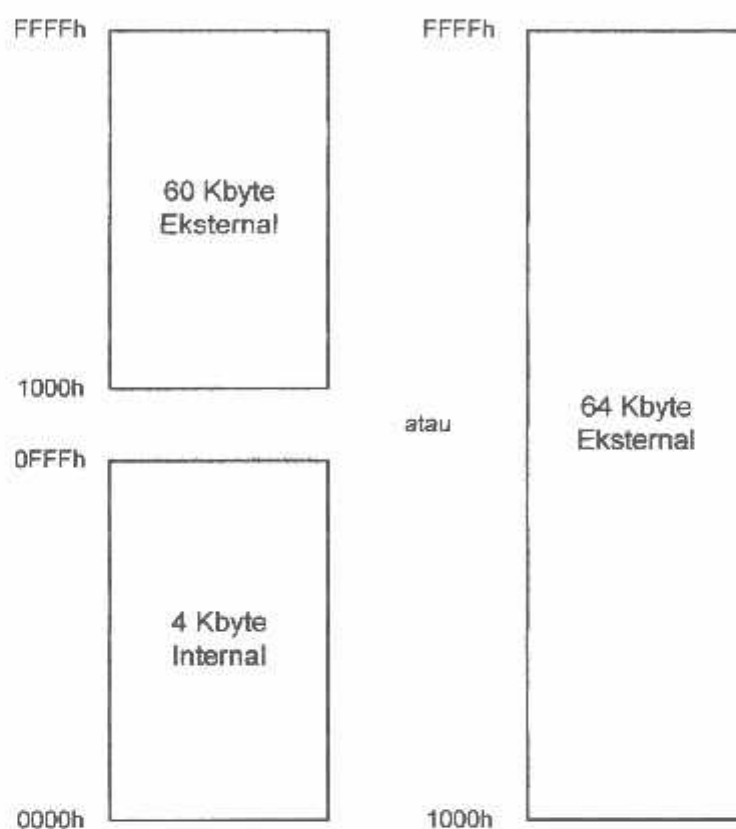
2. 5. 4. Organisasi Memori

Produk mikrokontroler Flash AT89S51 dari Atmel ini memiliki ruang alamat (*address space*) memori data dan memori program yang terpisah. Pemisahan memori data dan memori program tersebut membolehkan memori data diakses dengan alamat 8-bit sehingga dapat dengan cepat dan mudah disimpan dan dimanipulasi oleh CPU 8-bit. Namun demikian, alamat memori data 16-bit bisa juga dihasilkan melalui register DPTR (*Data Pointer Register*).

Memori program hanya dapat dibaca saja tidak bisa ditulisi (karena disimpan dalam EPROM). Terdapat memori program yang bisa diakses langsung hingga 64 Kbyte. Sedangkan *strobe* (tanda) untuk akses program memori eksternal melalui sinyal PSEN (*Program Store Enable*).

Memori data menempati suatu ruang alamat yang terpisah dari memori program. Memori eksternal dapat diakses secara langsung hingga 64 Kbyte dalam ruang memori data eksternal. CPU akan memberikan sinyal baca dan tulis, (RD dan WR), selama pengaksesan memori data eksternal. Memori data eksternal dan memori program eksternal dapat dikombinasi dengan cara menggabung sinyal RD dan PSEN melalui gerbang AND dan keluarannya sebagai tanda baca ke memori data / program eksternal. Mikrokontroler AT89S51 memiliki internal program memori 4 Kbyte dan dapat diperluas (*expant*) dengan memori luar menjadi 64

Kbyte memori program dan 64 Kbyte memori data. Secara otomatis jika alamat program lebih besar dari 0FFFh akan mengeksekusi *address byte* dari program memori.



Gambar 2–10. Oganisasi Program Memory

Memori internal terdiri dari ROM/*Flash Memory* dan RAM data di dalam *chip*. RAM berisi susunan *general purpose storage*, *bit addressable storage*, *register bank* dan *special function register*. Gambar di atas menampilkan secara detil memori data didalam *chip* mikrokontroller AT89S51 (MCS-51). Ruang memori internal dibagi menjadi:

- *Register Bank* (00H-1FH)
- *Bit Addressable RAM* (20H-2FH)
- *General Purpose RAM* (30H-7FH)
- *Special Function Register* (80H-FFH)

Untuk data memori dibagi menjadi dua bagian yaitu register khusus yang dipergunakan oleh mikrokontroller adalah SFR (*Special Function Register*) dan 4 bank atau 8 register (R0-R7) yang dapat dipakai oleh pengguna. Untuk alamat bawah yang pertama yaitu 00H sampai 7FH sebanyak 128 byte terbagi dalam tiga bagian besar berdasarkan kegunaannya sebagai berikut :

a. *Register Banks.*

Mikrokontroler AT89S51 mempunyai delapan buah register yang terdiri atas R0 hingga R7.

- Lokasi *register bank* dimulai dari alamat 00H – 1FH terdiri dari 32 byte
- *Register bank* ini terdiri dari 4 buah 8 byte yang dapat dipilih melalui pengaturan RS0 dan RS1 yang merupakan bit ke-3 dari *Program Status Word Register*.

b. *Bit Addressable RAM.*

Mikrokontroller AT89S51 memiliki 210 lokasi bit *addressable*, dimana 128 lokasi mempunyai alamat byte mulai Terdiri dari 16 byte yang dimulai dari 20h – 2Fh. Masing-masing dari 128 byte lokasi ini dapat dialamati secara langsung.

c. **General Purpose RAM.**

Lokasi memori pada *General Purpose RAM* dapat diakses secara langsung dengan mode *direct* maupun *indirect addressing*. Sebagai contoh, untuk membaca dan meng-copy isi RAM internal dengan alamat 5FH kedalam *Accumulator* dapat menggunakan instruksi:

MOV A, 5FH

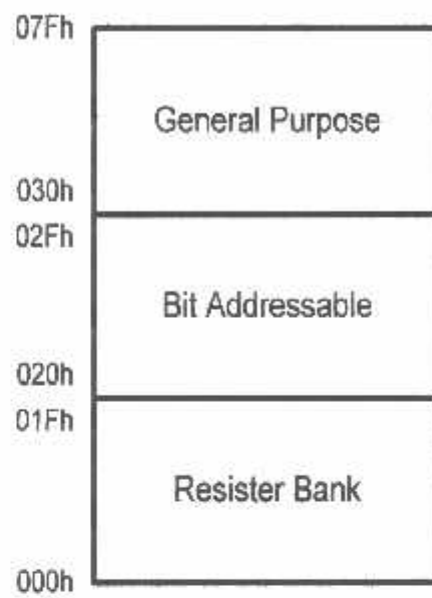
Instruksi ini memindahkan byte data secara *direct addressing* dengan sumber yang beralamat 5FH.

RAM internal dapat juga diakses menggunakan *indirect addressable* melalui R0 atau R1. Sebagai contoh, dua instruksi berikut ini:

MOV R0, #5FH

MOV A, @R0

Instruksi pertama dipakai sebagai *immediate addressable* yang memindahkan nilai 5FH kedalam register R0 dan instruksi kedua dipakai sebagai *indirect addressing* untuk memindahkan data yang ditunjuk oleh R0 kedalam *Accumulator*.



Gambar 2-11. Data Memory

Tabel 2-2. Register Bank

RS1	RS0	Register Bank	Address
0	0	0	00h – 07h
0	1	1	08h – 0Fh
1	0	2	10h – 17h
1	1	3	18h – 1Fh

2. 5. 5. Special Function Register (SFR)

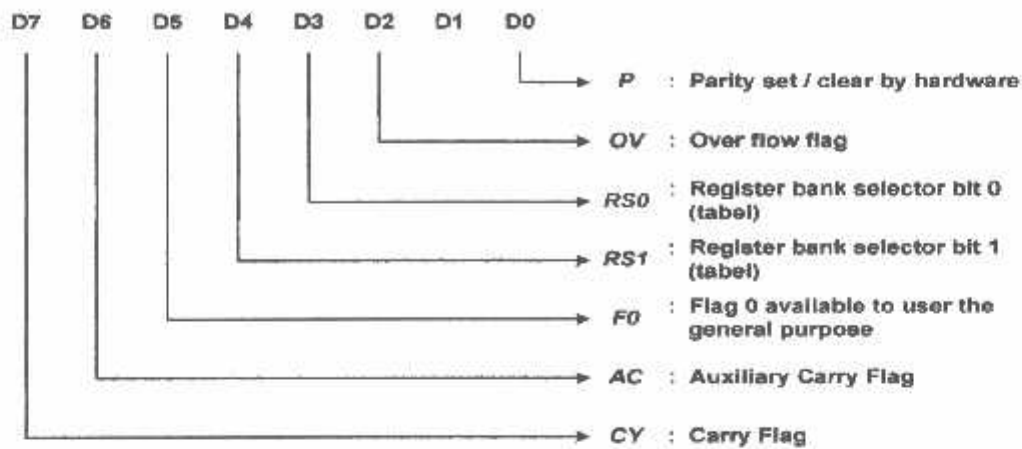
SFR terletak pada alamat memori internal 80h – FFh. Tetapi tidak semua alamat tersebut digunakan sebagai SFR, melainkan alamat tertentu seperti tabel berikut :

Tabel 2-3. Special Function Register

Simbol	Nama	Address
ACC	ACCUMULATOR	0E0h
B	BV REGISTER	0F0h
PSW	PROGRAM STATUS WORD	0D0h
SP	STACK POINTER	81h
DPTR	DATA POINTER	
DPL	LOW BYTE	82h
DPH	HIGH BYTE	83h
P0	PORT 0	80h
P1	PORT 1	90h
P2	PORT 2	0A0h
P3	PORT 3	0B0h
IP	INTERRUPT PRIORITY CONTROL	0B8h
IE	INTERRUPT ENABLE CONTROL	0A8h
TMOD	TIMER/COUNTER MODE CONTROL	89h
TCON	TIMER/COUNTER CONTROL	88h
TH0	TIMER/COUNTER 0 HIGH CONTROL	8Ch
TL0	TIMER/COUNTER 0 LOW CONTROL	8Ah
TH1	TIMER/COUNTER 1 HIGH CONTROL	8Dh
TL1	TIMER/COUNTER 1 LOW CONTROL	8Bh
SCON	SERIAL CONTROL	98h
SBUF	SERIAL DATA BUFFER	99h
PCON	POWER CONTROL	87h

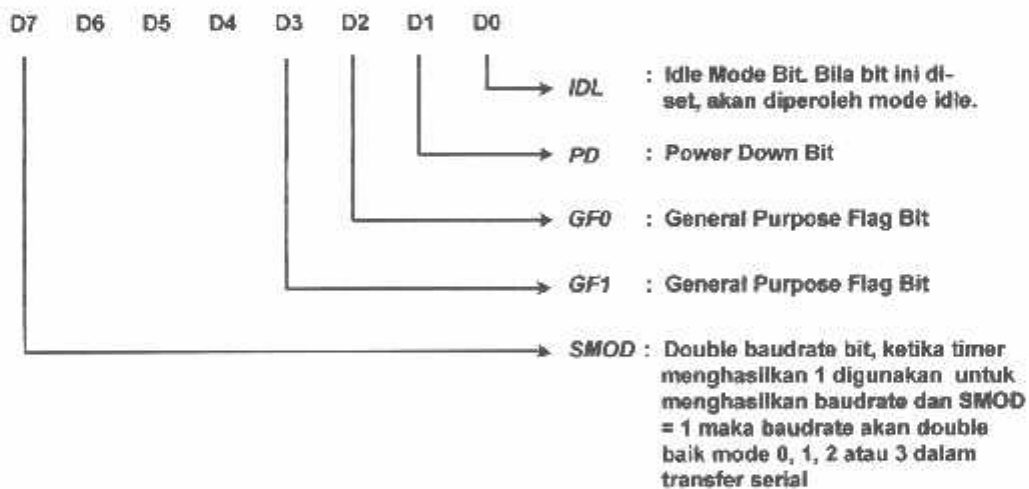
2. 5. 6. Program Status Word

Untuk pedefinisian *Program Status Word* ini dapat dilakukan per bit maupun secara keseluruhan dari register ini. Register ini terletak pada alamat D0H. Cara mendefinikannya adalah sebagai berikut :



2.5.7. Power Control Register

Register ini terletak pada alamat 87H. Cara mendefinisikannya adalah sebagai berikut:



2. 5. 8. Metode Pengalamatan

Metode pengalamatan pada AT89S51 adalah sebagai berikut :

a. Pengalamatan Tak Langsung

Operand pengalamatan tak langsung menunjuk ke arah sebuah register yang berisi lokasi alamat memori yang akan digunakan di dalam operasi. Lokasi yang nyata tergantung pada isi register saat instruksi dijalankan. Untuk melaksanakan pengalamatan tak langsung digunakan simbol @.

ADD A,@R0 ; Tambahkan isi RAM yang lokasinya
ditunjukkan oleh register R0 ke akumulator.

DEC @R1 ; Kurangi satu isi RAM yang
alamatnya ditunjukkan oleh register R1

MOVX @DPTR,A ; Pindahlan isi akumulator ke memori
luar yang lokasinya ditunjukkan oleh *data
pointer* (DPTR)

b. Pengalamatan Langsung

Pengalamatan langsung dilakukan dengan memberi nilai suatu register secara langsung. Untuk melaksanakan hal tersebut digunakan tanda #.

MOV A,#01H ; Isi akumulator dengan bilangan 01H

MOV DPTR,#19ABH ; Isi register DPTR dengan bilangan
19ABH.

Pengalamatan data langsung dari 0 sampai 127 akan mengakses RAM internal, sedang pengalamatan dari 128 sampai 255 akan mengakses register perangkat keras.

MOV P3,A ; Pindahkan isi akumulator ke alamat data
B0H (B0H adalah alamat Port 3)

INC 50 ; Naikkan lokasi 50 (desimal) dalam memori.

c. Pengalamatan Bit

Pengalamatan bit adalah penunjukkan alamat lokasi bit baik dalam RAM internal (byte 32 sampai 47) atau perangkat keras. Untuk melakukan pengalamatan bit digunakan simbol titik (.), misalnya :

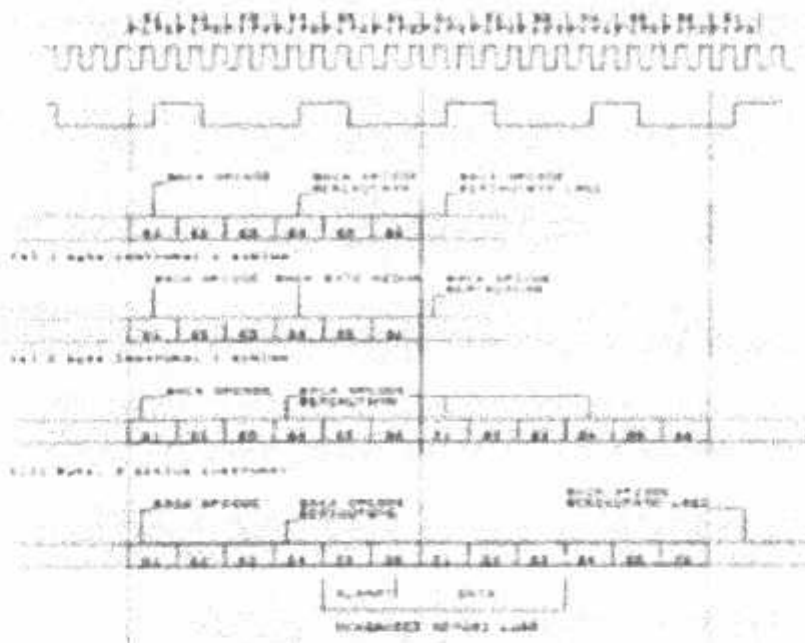
SETB P1.1 ; Ubah bit ke 1 pada Port 1 menjadi *high*

d. Pengalamatan Kode

Ada tiga macam instruksi yang dibutuhkan dalam pengalamatan kode, yaitu *relative jump*, *in-block jump* atau *call* dan *long jump*.

2. 5. 9. Siklus Mesin (Machine Cycle)

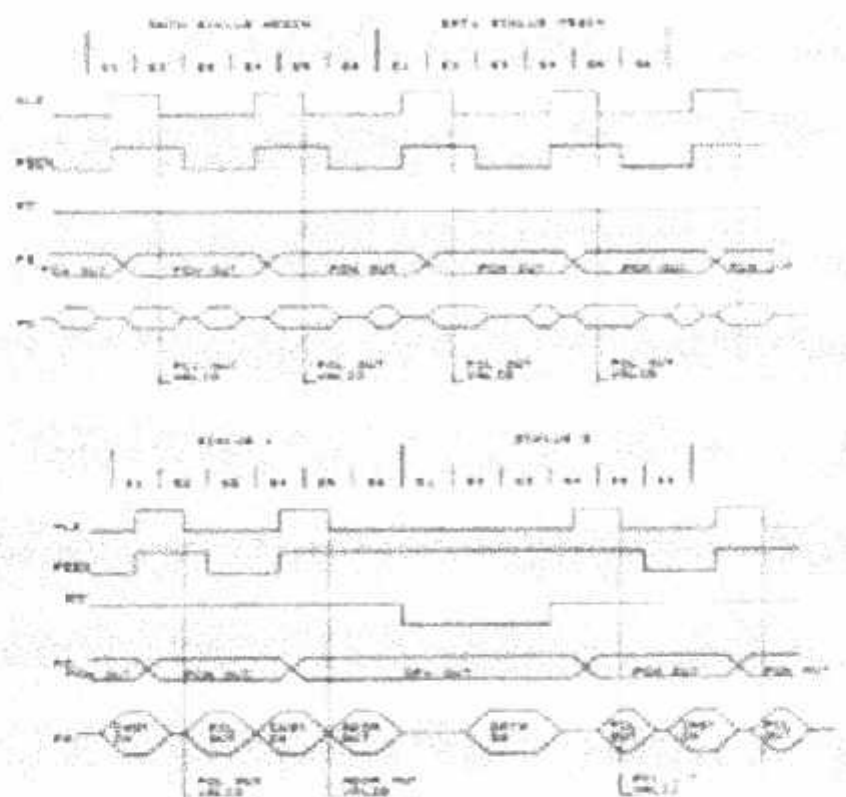
Satu siklus mesin (*machine cycle*) berisi urutan 6 keadaan , diberi nomor S1 sampai S6. Setiap keadaan waktu adalah sepanjang dua perioda osilator atau satu mikrodetik jika frekuensi osilator 12 MHz. Gambar 2-12 memperlihatkan urutan pengambilan/eksekusi program untuk beberapa instruksi.



Gambar 2-12. Urutan Siklus Keadaan *Duty Cycle*

Eksekusi satu siklus instruksi dimulai selama keadaan 1 (*state 1*) dari siklus mesin, saat kode operasi (*opcode*) ditahan dalam register instruksi (*IP, instruction register*). Pengambilan kedua terjadi selama S4 pada siklus mesin yang sama. Eksekusi secara lengkap selesai pada akhir keadaan S6 dari siklus mesin.

Urutan eksekusi adalah sama untuk program memori eksternal maupun internal. Waktu eksekusi tidak tergantung pada memori program internal dan eksternal.

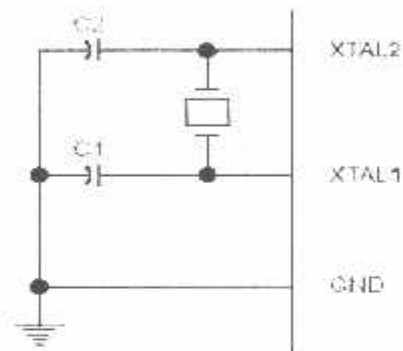


Gambar 2-13. Siklus Bus pada Pengaksesan Memori Program Eksternal

Gambar 2-13.a memperlihatkan sinyal dan pewartuan dalam mengambil program jika memakai memori program eksternal, sinyal PSEN diaktifkan dua kali setiap siklus mesin. Apabila terjadi akses pada memori data eksternal, sinyal PSEN terlihat seperti pada gambar 2-13.b

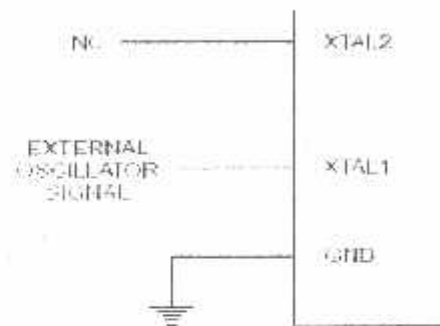
2.5.10. Pewaktuan CPU

Mikrokontroler AT89S51 memiliki osilator internal (*on chip oscillator*) yang dapat digunakan yang dapat digunakan sebagai sumber clock bagi CPU. Untuk menggunakan isolator internal diperlukan sebuah kristal atau resonator keramik antara pena XTAL1 dan XTAL2 dan sebuah kapasitor ke *ground* seperti yang terlihat pada gambar 2-14. berikut ini:



Gambar 2-14. Menggunakan Osilator Internal

Untuk kristalnya dapat digunakan frekuensi dari 6 sampai 12 MHz. Sedangkan untuk kapasitor dapat bernilai antara 27 pF sampai 33 pF. Bila menggunakan clock eksternal, maka rangkaianya dihubungkan seperti pada gambar 2-15. berikut ini:



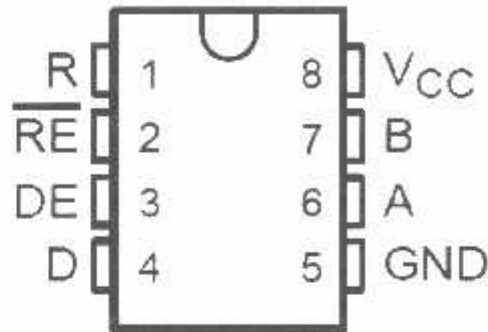
Gambar 2-15. Menggunakan Sumber Clock Eksternal

2.6. Standart Interface RS-485 (IC SN75176)

RS-485 biasa digunakan untuk menyediakan sinyal serial yang kuat sehingga sanggup mentransmisikan data hingga jarak 4000 ft (1200 m). Mampu melalui kabel transmisi yang cukup panjang pada *baud rate* yang tinggi dalam lingkungan listik yang potensial menimbulkan *noise* atau interferensi elektromagnetik yang tinggi.

RS-485 dapat menangani 128 titik cabang ada satu saluran bersama dan bekerja dengan metode *half duplex*. Dalam setiap *chip* terdapat satu unit pengirim (D) dan satu unit pengaktif penerima RE (*Receive Enable*), RO (*Receive Output*) merupakan data output, DE (*Driver Enable*) merupakan pengaktif unit pengirim

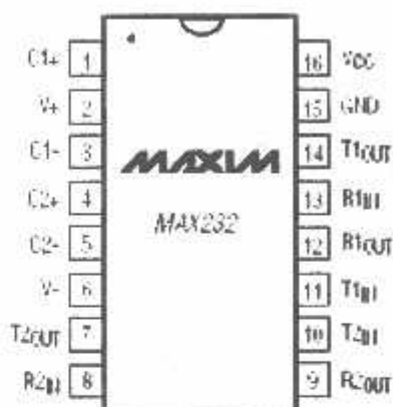
data, DI (*Data Input*) merupakan inputan data yang akan dikirimkan, A adalah pin pengirim data menuju pin B RS-485 lawan komunikasi dan B adalah pin penerima data dari pin A RS-485 lawan komunikasi.



Gambar 2-16 . Konfigurasi pin IC SN75176(RS 485)

2.7. IC MAX 232

IC RS 232 ini merupakan penghubung antara *personal computer* (PC) dengan unit perangkat kontroler baik itu mikrokontroler ataupun perangkat kontrol lainnya. IC ini berfungsi untuk mengubah level TTL dari mikrokontroller menjadi level RS-232 sehingga data dapat dikirim dalam format serial ke PC. Untuk keperluan ini tegangan +5V untuk media pengiriman data diterima oleh komputer dari perangkat kontroler melalui pin 11 'TX' (*data transmits*), sedangkan perangkat kontroler menerima data dari komputer melalui pin 10 'RX' (*data receive*).



Gambar 2-17. konfigurasi pin IC MAX 232

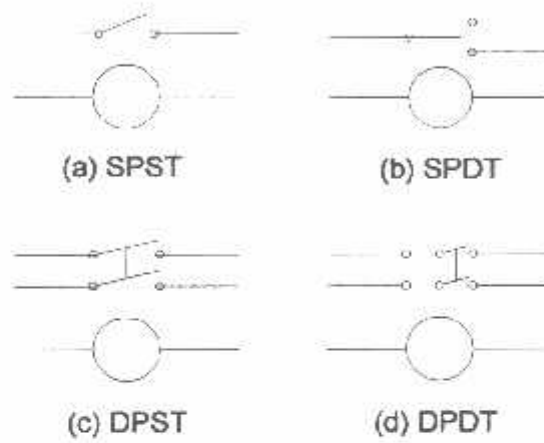
2.8. Relay

Relay adalah suatu perangkat saklar (*switch*) yang dioperasikan oleh gaya elektromagnetik yang dihasilkan oleh kumparan yang berada didalamnya.

Relay ini pada umumnya digunakan untuk menyambung dan memutuskan hubungan antara suatu bagian dengan bagian lainnya dalam suatu rangkaian elektronik, selain itu juga dimaksudkan untuk megisolasi *switching* antara tegangan catu tinggi dengan catu rendah. Kerugian yang ditemui pada relay yaitu adanya waktu tanggapan (*respons time*) saat on maupun saat *off*, yang relatif lambat dan serta adanya efek induksi balik sesaat setelah relay *off*. Oleh sebab itu maka antara rangkaian pengendali dan relay perlu di-isolasi dengan rangkaian peng-isolasi

Relay terdiri dari 4 jenis relay, yaitu:

- DPDT (*Double Pole, Double Throw*)
- SPDT (*Single Pole, Double Throw*)
- DPST (*Double Pole, Single Throw*)
- SPST (*Single Pole, Single Throw*)



Gambar 2-18. Jenis-jenis Relay

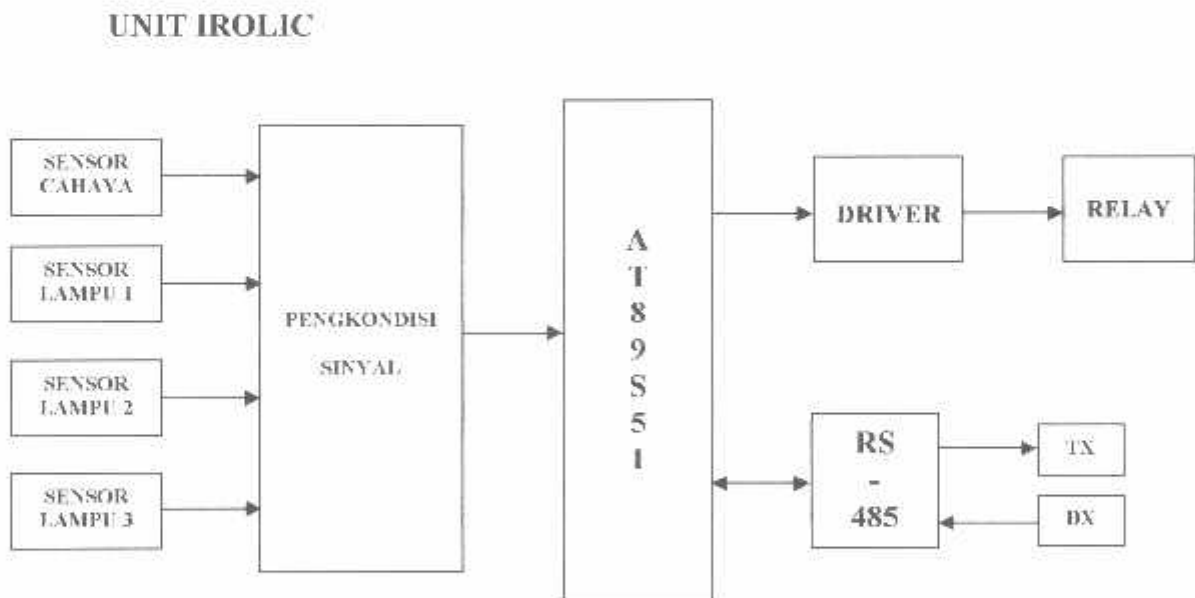
BAB III

PERENCANAAN DAN PEMBUATAN ALAT

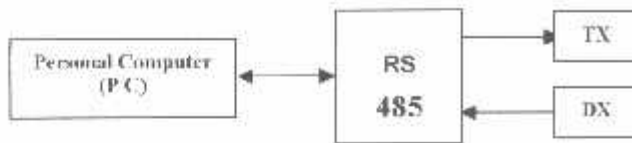
Pada Bab ini dibahas perencanaan dan pembuatan alat yang dibagi menjadi dua bagian yaitu : bagian perencanaan dan pembuatan perangkat keras, dan bagian perencanaan dan pembuatan perangkat lunak.

3.1. Perencanaan perangkat keras

Blok diagram dari perencanaan perangkat keras secara keseluruhan adalah sebagai berikut:



PUSAT IROLIC



Gambar 3-1. Diagram blok rangkaian keseluruhan

Fungsi dari tiap-tiap blok akan dijelaskan dibawah ini :

1. Sensor Cahaya (Luar).
Untuk mengetahui keadaan cahaya diluar, apakah itu dalam keadaan cerah atau mendung.
2. Sensor Cahaya (Lampu).
Untuk mengetahui keadaan lampu 1 sampai lampu 3, apakah itu dalam keadaan hidup atau mati.
3. Pengkondisi Sinyal
Berfungsi sebagai linearisasi dan penguatan sinyal keluaran dari sensor cahaya dan sensor lampu yang masih lemah.
4. Mikrokontroler
Berfungsi sebagai pengolah data dan juga sebagai kontrol utama dari sistem.
5. Driver
Berfungsi sebagai penguat keluaran dari mikrokontroler yang digunakan sebagai inputan bagi relay.

6. Relay

Berfungsi sebagai pengubah sinyal listrik menjadi saklar yang digunakan untuk menyalakan lampu

7. RS485

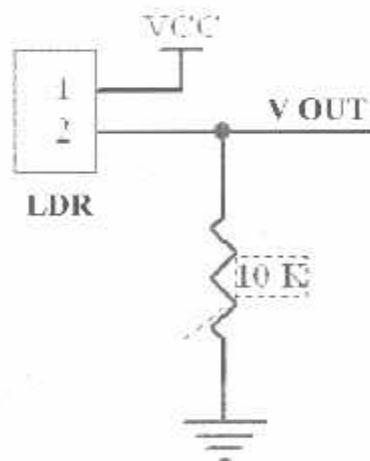
Berfungsi sebagai sarana komunikasi antara pusat IROLICS dengan unit IROLICS.

8. PC

Berfungsi sebagai penerima, pengolah dan penampil data dari keadaan cahaya luar dan keadaan lampu 1, lampu 2, lampu 3.

3.2. Rangkaian Sensor

Sensor yang digunakan adalah LDR yang diseri dengan resistor bernilai 10 k Ohm sebagai pembagi tegangan sekaligus pelindung bagi LDR tersebut dari shock voltage. Rangkaiannya adalah seperti gambar di bawah ini :



Gambar 3-2. Rangkaian sensor

3.3. Rangkaian OP -Amp Sebagai Komparator

Untuk mendapatkan Perubahan V_{out} dengan konstan (hanya kondisi Low(0) atau High(5)), maka ditentukan tegangan referensi 2.5 volt berdasarkan nilai tengah V_{cc} .

Untuk mendapatkan nilai V referensi, maka R referensi dapat di cari dengan persamaan :

$$V = I \times R$$

$$I = \frac{V}{R}$$

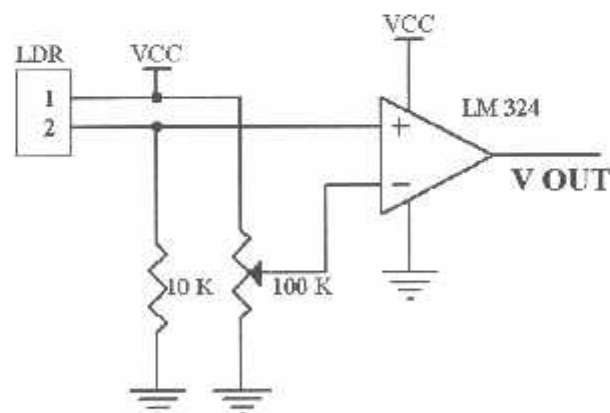
$$I = \frac{5}{100 \text{ K Ohm}}$$

$$I = 0.05 \text{ mA}$$

$$R = \frac{V}{I}$$

$$R = \frac{2.5V}{0.05mA}$$

$$R = 50 \text{ K OHM}$$



Gambar 3-3. OP-AMP sebagai pembanding tegangan (komparator)

3.4. Rangkaian OP-AMP LM 324 sebagai BUFFER (penyangga).

Rangkaian ini dipakai untuk rangkaian sensor cahaya luar dan outputnya diinputkan ke ADC 0804 karena outputnya masih berupa perubahan tegangan analog.

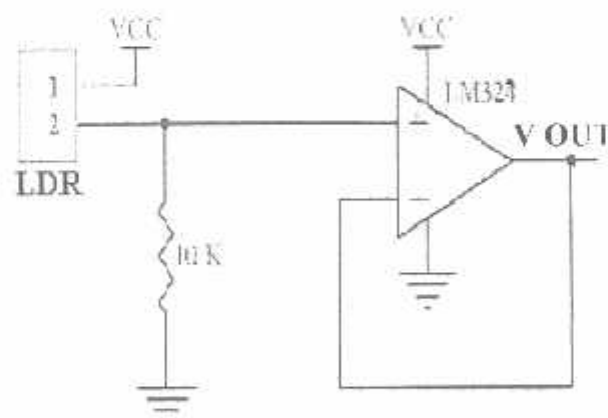
Buffer (penyangga) biasanya didefinisikan sebagai rangkaian dengan penguatan satu atau dengan keluaran mengikuti masukan. Diantara masukan dan keluaran terdapat isolasi impedansi. Sehingga keluaran dari penguat jenis ini adalah sesuai dengan tegangan masukannya, yaitu :

$$V_{out} = V_{in}$$

$$A_v = \left(\frac{R_f}{R_{in}} + 1 \right)$$

$$= \frac{0}{R_{in}} + 1$$

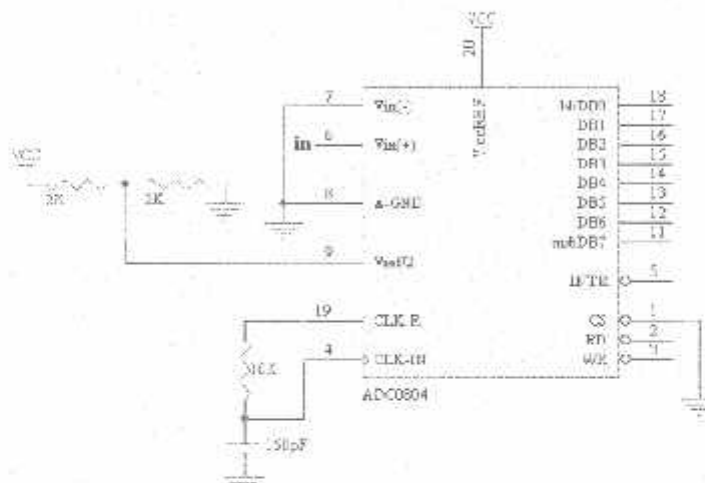
$$= 1$$



gambar 3-4. OP-AMP sebagai BUFFER (penyangga)

3.5. Rangkaian ADC 0804

Rangkaian ini mendapat input dari output rangkaian OP-AMP sebagai Buffer, keluaran 8 bitnya dipakai oleh port 2 pada Microcontroller. Kegunaan dari rangkaian ini adalah untuk mengubah sinyal tegangan dari buffer menjadi sinyal digital 8 bit agar PC dapat mendeteksi perubahan cahaya di luar secara lebih halus.



Gambar 3-5. Rangkaian ADC 0804

3.6. Rangkaian Minimum System Microcontroller AT89S51

Penggunaan Mikrokontroller AT89S51 harus didukung oleh beberapa rangkaian penunjang agar dapat melakukan fungsinya, antara lain rangkaian *clock* dan *reset*. Selain itu juga harus ditentukan penggunaan *port – port*-nya dan sinyal yang digunakan untuk mendukung proses yang ingin dilakukan

3.6.1. Rangkaian Clock

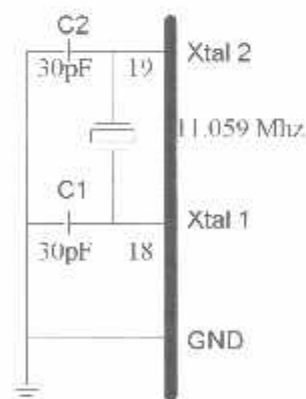
Kecepatan proses pengolahan data pada mikrokontroller ditentukan oleh *Clock* (pewaktu) yang dikendalikan oleh mikrokontroller tersebut. Pada Mikrokontroller AT89S51 terdapat *internal clock* generator yang berfungsi sebagai sumber *clock*, tapi masih memerlukan rangkaian tambahan untuk membangkitkan *clock* yang diperlukan.

Rangkaian *clock* ini terdiri atas dua buah kapasitor, dan sebuah Kristal yang terangkai sedemikian rupa dan kemudian dihubungkan dengan chip yang tersedia pada AT89S51.

Dalam perencanaan ini menggunakan :

- ✓ C = 30 pF. Penentuan besarnya kapasitansi disesuaikan dengan spesifikasi lembar data AT89S51
- ✓ X-Tal 12 MHz. Pemilihan X-Tal 11.059 MHz ini karena dalam penghitungan lebih mudah.

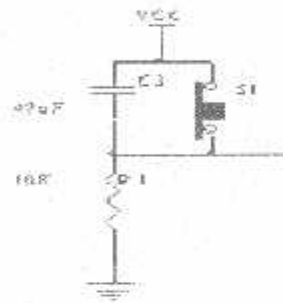
Adapun gambar rangkaian *clock* dapat dilihat pada gambar dibawah ini :



Gambar 3-6. Rangkaian Clock
Sumber : Atmel : 2000 : 4

3.6.2. Rangkaian Reset

Rangkaian *reset* diperlukan untuk mereset mikrokontroller ke alamat 0000 Hex. Untuk *me-reset* mikrokontroller pada pin RST harus diberi logika tinggi selama sekurang – kurangnya dua siklus mesin (24 periode osilator) Untuk membangkitkan sinyal *reset* pada saat awal catu daya dihidupkan, maka perlu menghubungkan pin RST dengan catu daya dengan kapasitor. Seperti dalam gambar 3.3 :



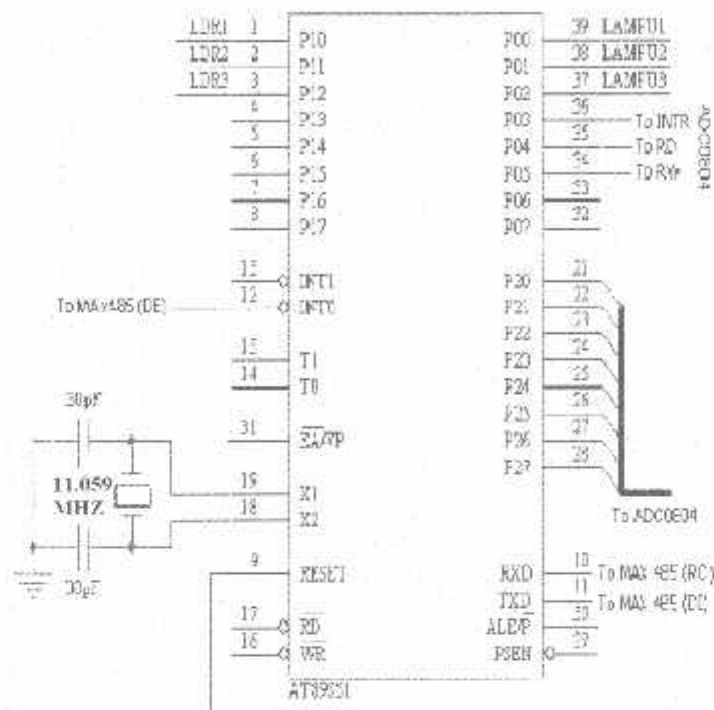
Gambar 3-7. Rangkaian Reset

Sehingga ketika catu daya dinyalakan kapasitor akan menahan pin RST dalam kondisi logika tinggi selama beberapa saat tergantung nilai kapasitor dan kecepatan pengisian muatannya. Pemberian catu daya pada mikrokontroller tanpa suatu sinyal *reset* dapat menyebabkan mikrokontroller memulai eksekusi instruksinya dari lokasi yang tak menentu. Ini di sebabkan karena *Program Counter* tidak terinisialisasi.

3.6.3. Konfigurasi Kaki Microcontroller AT89S51

Konfigurasi pin yang digunakan pada rangkaian IROLICS :

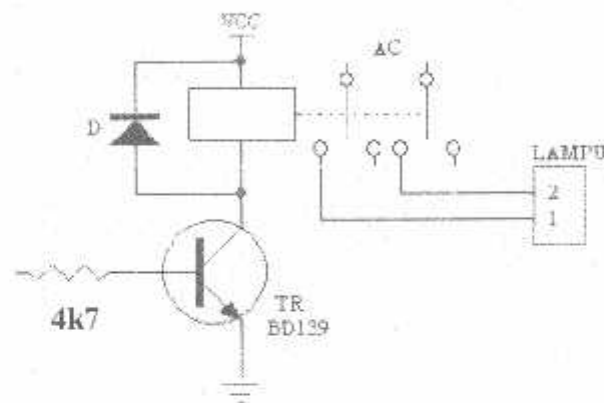
- Pin 1,2,3 dihubungkan dengan sensor cahaya.
 - Pin 9 dihubungkan dengan rangkaian reset.
 - Pin 10 dihubungkan dengan IC MAX 485 Pin 1.
 - Pin 11 dihubungkan dengan IC MAX 485 Pin 4.
 - Pin 12 dihubungkan dengan MAX 485 pin 3
 - Pin 18, 19 dihubungkan dengan kristal.
 - Pin 21, 22, 23, 24, 25, 26, 27, 28 dihubungkan dengan ADC0804
Pin 11, 12, 13, 14, 15, 16, 17, 18.
 - Pin 34 dihubungkan dengan ADC0804 Pin 3
 - Pin 35 dihubungkan dengan ADC0804 Pin 2.
 - Pin 36 dihubungkan dengan ADC0804 Pin 5.
 - Pin 37, 38, 39 dihubungkan dengan rangkaian driver relay
 - Pin 40 digunakan sebagai Vcc.
 - Pin 20 digunakan sebagai Ground.
-



Gambar 3-8. Konfigurasi kaki –kaki AT89S51 Pada IROLICS

3.7. Rangkaian Driver Bagi Relay

Untuk menggerakkan relay untuk menyalakan atau mematikan lamapu dibutuhkan rangkaian driver. Rangkaian ini menggunakan Transistor BD 139 sebagai elektrik switch. BD 139 merupakan jenis transistor NPN sehingga dapat digunakan sebagai saklar bila ada inputan pada basisnya. Dan untuk relaynya dipakai jenis DPDT (Double Pole Double Throw).



Gambar 3-9. Rangkaian driver bagi relay.

Untuk mencari nilai R_b digunakan persamaan :

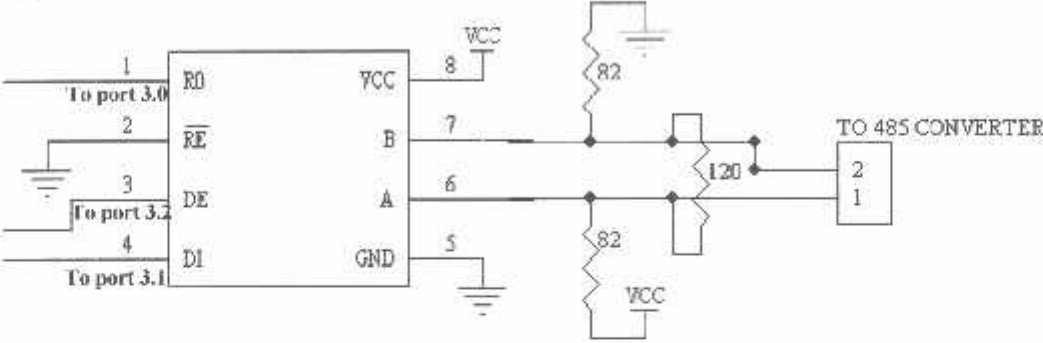
$$I_c \text{ max} = h_{fe} \times I_b$$

$$I_b = \frac{I_c \text{ max}}{h_{fe}} = \frac{100}{100} = 1 \text{ mA}$$

$$R_b = \frac{V_{CC} - V_{BE}}{I_b} = \frac{5 - 0.7}{1} = 4.3 \text{ k Ohm}$$

3.8. Rangkaian RS-485 (IC SN75176)

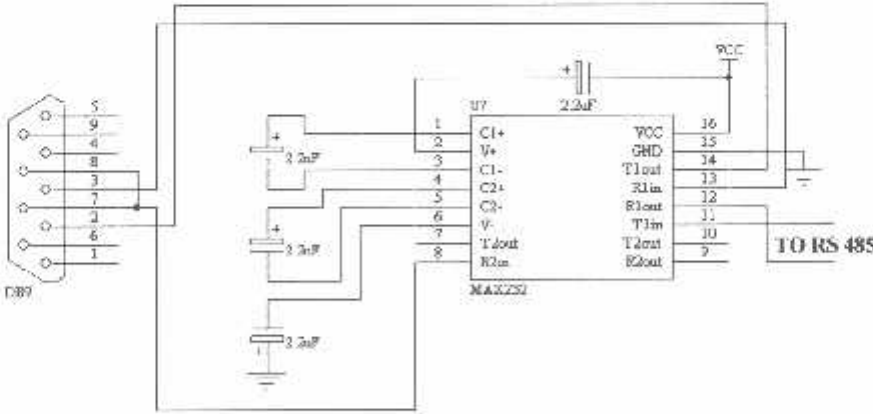
Rangkaian ini digunakan untuk saluran Komunikasi data serial agar Micocontroller dapat berhubungan dengan PC. Gambar konfigurasi pin dari IC ini yang dihubungkan dengan system adalah sebagai berikut :



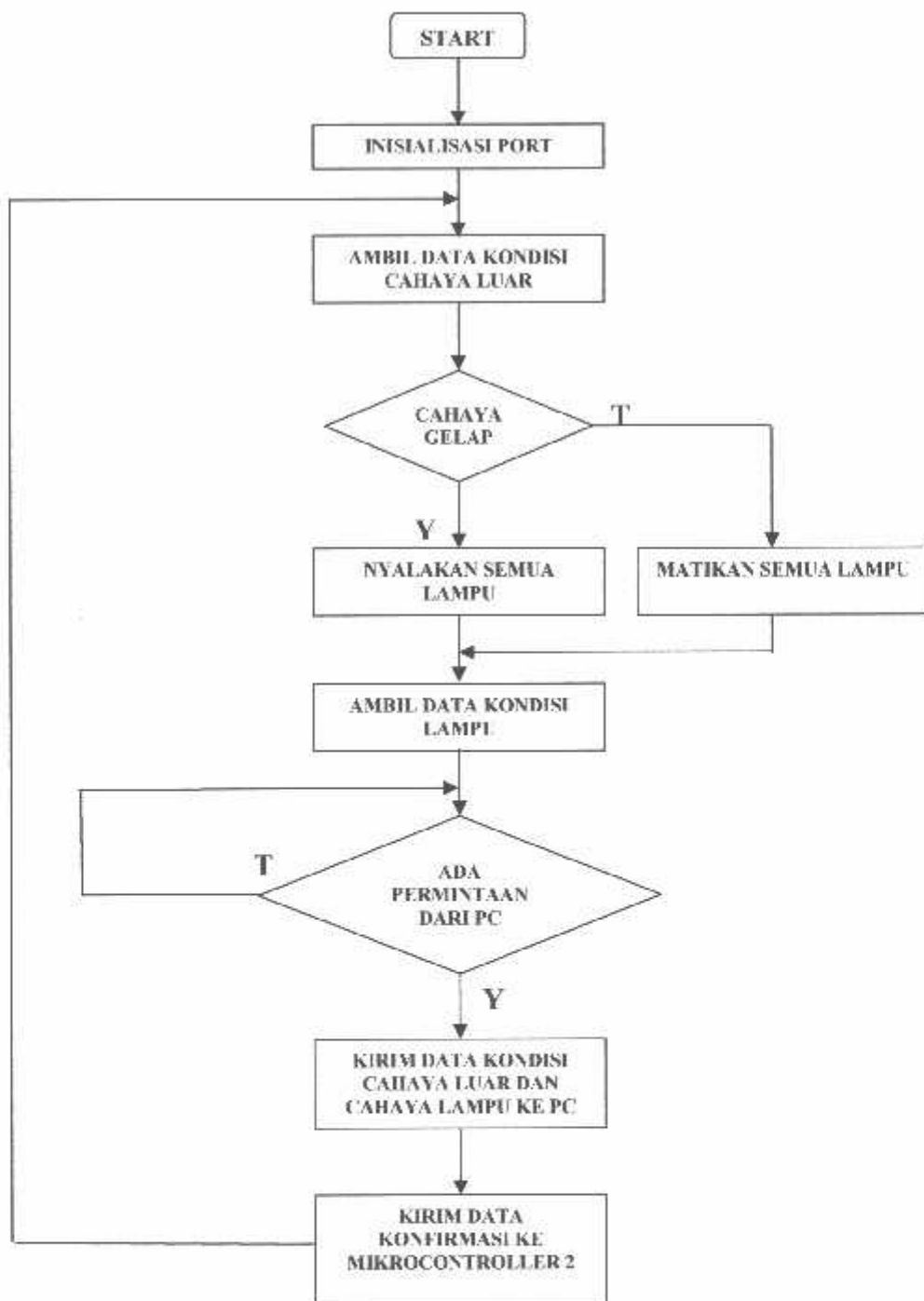
Gambar 3-10 Rangkaian IC SN75176

3.9. Rangkaian IC MAX 232

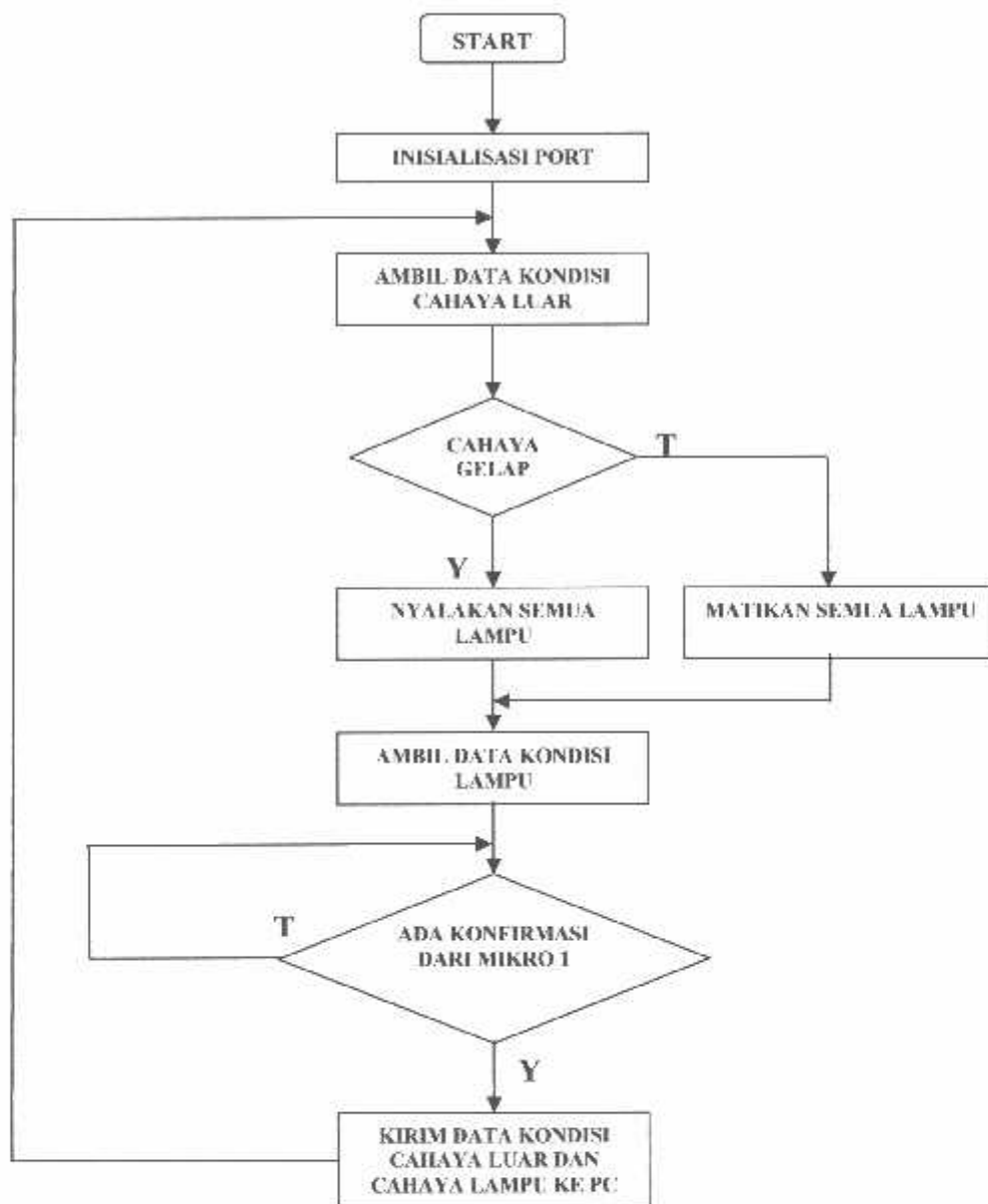
Rangkaian ini digunakan untuk merubah level tegangan TTL yang digunakan oleh Microcontroller menjadi level tegangan RS-232 pada serial port PC. Gambar rangkaian adalah sebagai berikut :



Gambar 3-11. Rangkaian IC MAX 232



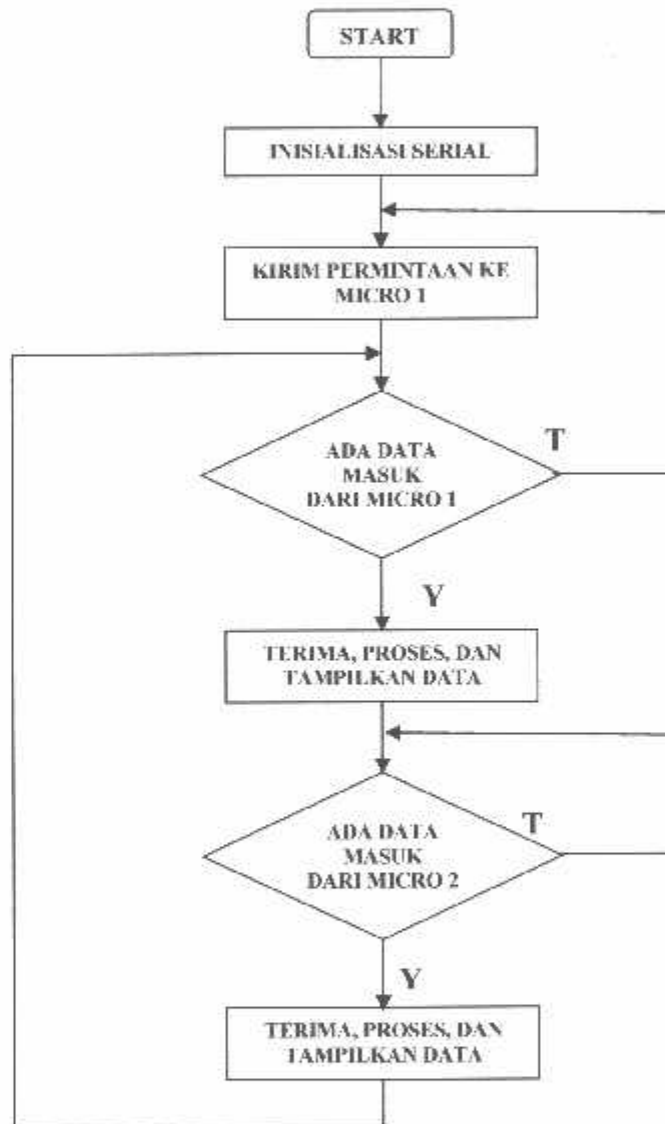
Gambar 3-12. Flowchart Pemograman Microcontroller 1.



Gambar 3-13. Flowchart Pemrograman Microcontroller 2.

3.10.2. Perancangan software pada PUSAT IROLICS

Perancangan software pada PUSAT IROLICS ini menggunakan bahasa Delphi yang merupakan produk dari Borland Corp. fungsi dari software pada Pusat IROLICS adalah sebagai pemonitor keadaan cuaca dan keadaan lampu di masing-masing UNIT IROLICS. Berikut ini adalah diagram alirnya:



Gambar 3-14. Flowchart Pemograman DELPHI.

BAB IV

PENGUJIAN DAN ANALISA ALAT

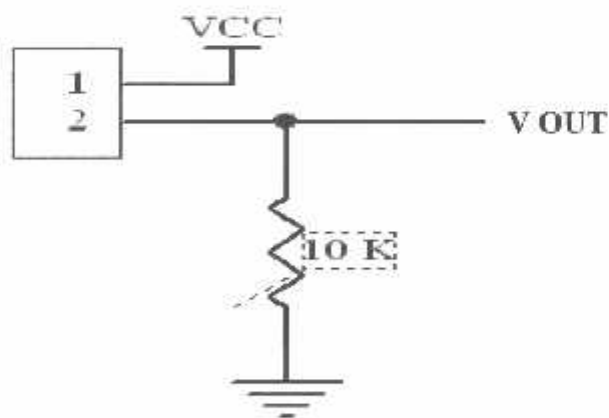
Dalam bab ini membahas tentang pengujian dan pengukuran dari peralatan yang dibuat. Secara umum pengujian ini bertujuan untuk mengetahui apakah piranti yang telah direalisasikan dapat bekerja sesuai dengan perencanaan yang telah direncanakan.

Peralatan yang digunakan :

- Project board
- Multimeter digital model DT 9205B
- Catu daya 12 dan 5 volt

4.1. Pengujian Rangkaian Sensor Cahaya

Bertujuan untuk mengetahui apakah sensor bekerja dengan baik atau tidak dan juga untuk mengetahui tegangan output dari sensor yang digunakan dalam skripsi ini.



Gambar 4-1. Rangkaian test sensor

Pengujian di bagi dua tahap yaitu :

- ~ Pertama adalah saat kondisi gelap, LDR ditutupi sedemikian rupa agar tidak terkena cahaya sama sekali.
- ~ kedua adalah saat kondisi terang, LDR didekatkan kepada lampu meja (NEON), Dan hasilnya adalah sebagai berikut :

TABEL 4-1.Hasil Pengukuran Rangkaian Sensor

TEGANGAN OUT PUT (VOLT)		RESISTANSI (OHM)	
TERANG	GELAP	TERANG	GELAP
4 . 8 0	0 . 8 5	1 8 0	~ *

* multimeter yang digunakan mempunyai nilai pengukuran resistansi maksimal sebesar 2 M Ohm.

Sedangkan menurut perhitungan hasilnya adalah sebagai berikut :

Kondisi terang :

$$V_o = R_1 / (R_1 + R_{LDR}) \times V_{cc}$$

$$= 10 \text{ k ohm} / (10 \text{ k ohm} + 180 \text{ ohm}) \times 5 \text{ Volt}$$

$$= 4 . 91 \text{ Volt}$$

Kondisi Gelap :

$$V_o = R_1 / (R_1 + R_{LDR})$$

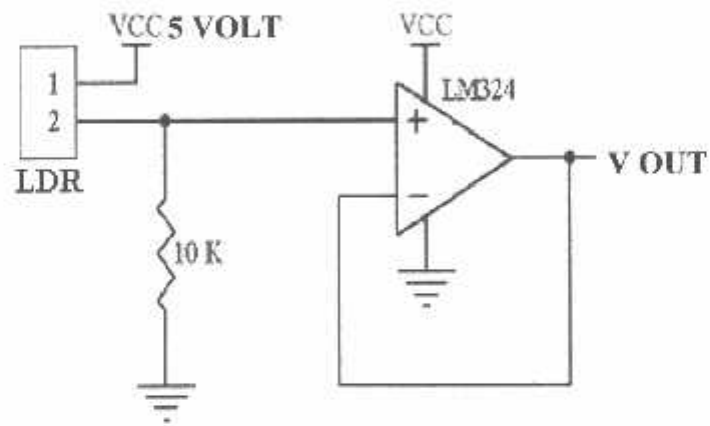
$$= 10 \text{ K Ohm} / (10 \text{ K Ohm} + \sim) \times v_{cc}$$

$$= 0 \text{ Volt}$$

4.2. Pengujian Pengkondisi sinyal

4.2.1. Op-Amp sebagai buffer :

Untuk mengetahui apakah buffer bekerja sesuai dengan fungsinya, yaitu tanpa penguatan atau penguatan satu kali. V_i dirubah dengan merubah intensitas cahaya yang diterima oleh LDR.



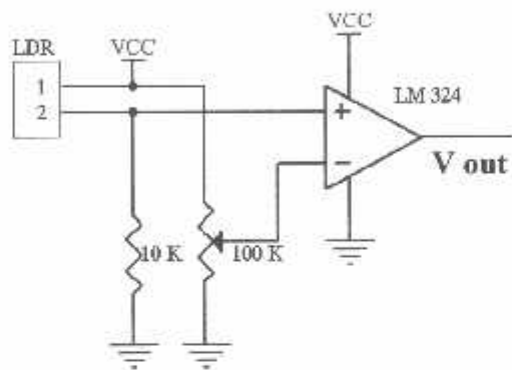
Gambar 4-2. Rangkaian uji buffer

Tabel 4-2. Hasil Pengujian OP-AMP sebagai Buffer

V in (VOLT)	V out (VOLT)
0.85	0.85
4.80	4.80

4.2.2. Pengujian Op-Amp sebagai Komparator

Pengujian ini dilakukan untuk mengetahui keadaan V_o dengan V_{in} yang berbeda- beda. Dengan mengubah intensitas cahaya yang diterima oleh LDR.



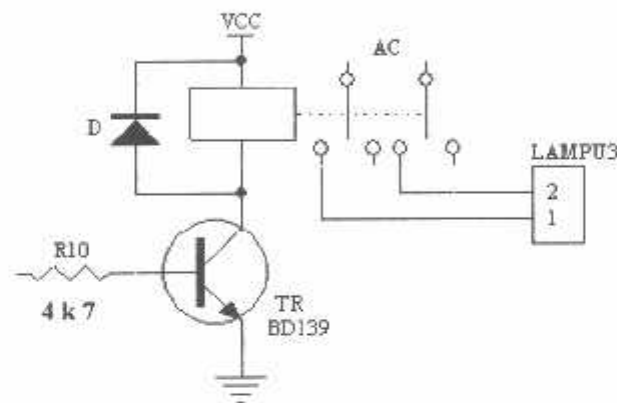
Gambar 4-3. Rangkaian uji Komparator

Tabel 4-3. Hasil pengujian output pada Komparator

Vi (volt)	Vo (Volt)
0.5	0.03
1.4	0.03
2.7	4.89
3.5	4.89

4.3. Pengujian Rangkaian Driver Relay

Pengujian ini dilakukan untuk mengetahui respon dari driver relay pada saat diberi inputan oleh MCU. Apabila input driver diberi logika *high* maka, transistor akan menjadi jenuh. Hal ini mengakibatkan relay dalam keadaan ON. Dan apabila inputan driver diberi logika *low* maka, transistor akan menjadi *cut-off*. Hal ini mengakibatkan relay dalam keadaan OFF.



Gambar 4-4.rangkaian Driver Relay

Tabel 4-4. Hasil Pengujian Untuk Mengetahui Respon Driver Relay

V in	Logika	Relay
0.8 Volt	Low	Mati
3.65 volt	High	Aktif

4.4. Pengujian secara Keseluruhan.

Bertujuan untuk mengetahui kerja dari seluruh SYSTEM IROLICS baik itu berupa proses Hardware maupun berupa kerja software. Dari pengujian didapatkan data sebagai berikut :

Tabel 4-5. Hasil Pengujian Unit Irolics

SENSOR CAHAYA	SENSOR LAMPU 1	SENSOR LAMPU 2	SENSOR LAMPU 3	DRIVER RELAY 1	DRIVER RELAY 2	DRIVER RELAY 3
LOW	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
HIGH	LOW	LOW	LOW	LOW	LOW	LOW

Tabel 4-6. Hasil Pengujian Pusat IROLICS berdasarkan kondisi Unit

IROLICS seperti Tabel 4.5.

Display Cahaya	Display lampu 1	Display lampu 2	Display 3
MIN	ON	ON	ON
MAX	OFF	OFF	OFF

BAB V

PENUTUP

5.1. Kesimpulan

- Perangkat PC dan Microcontroller AT 89S51 dapat dipergunakan untuk mengendalikan dan mengontrol lampu jalan.
- Microcontroller AT 89S51 dapat berkomunikasi dengan PC dengan bantuan IC MAX 232 untuk merubah level tegangan TTL (Mikrokontroler) ke level tegangan RS – 232 (PC).
- Terdapat faktor error yang menyebabkan adanya sedikit perbedaan antara hasil teori dengan hasil praktek

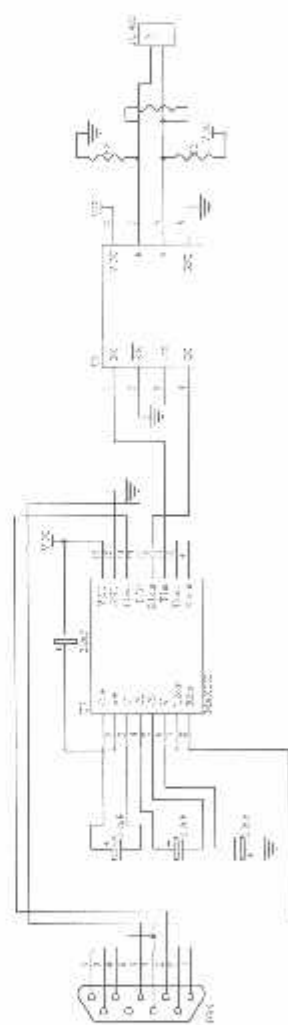
5.2.Saran

- Untuk mendapatkan hasil yang maksimal sebaiknya menggunakan komponen yang berkualitas.
 - Untuk mengatasi apabila listrik padam maka perlu digunakan catu daya lain sebagai Back-up Power Supply.
-

DAFTAR PUSTAKA

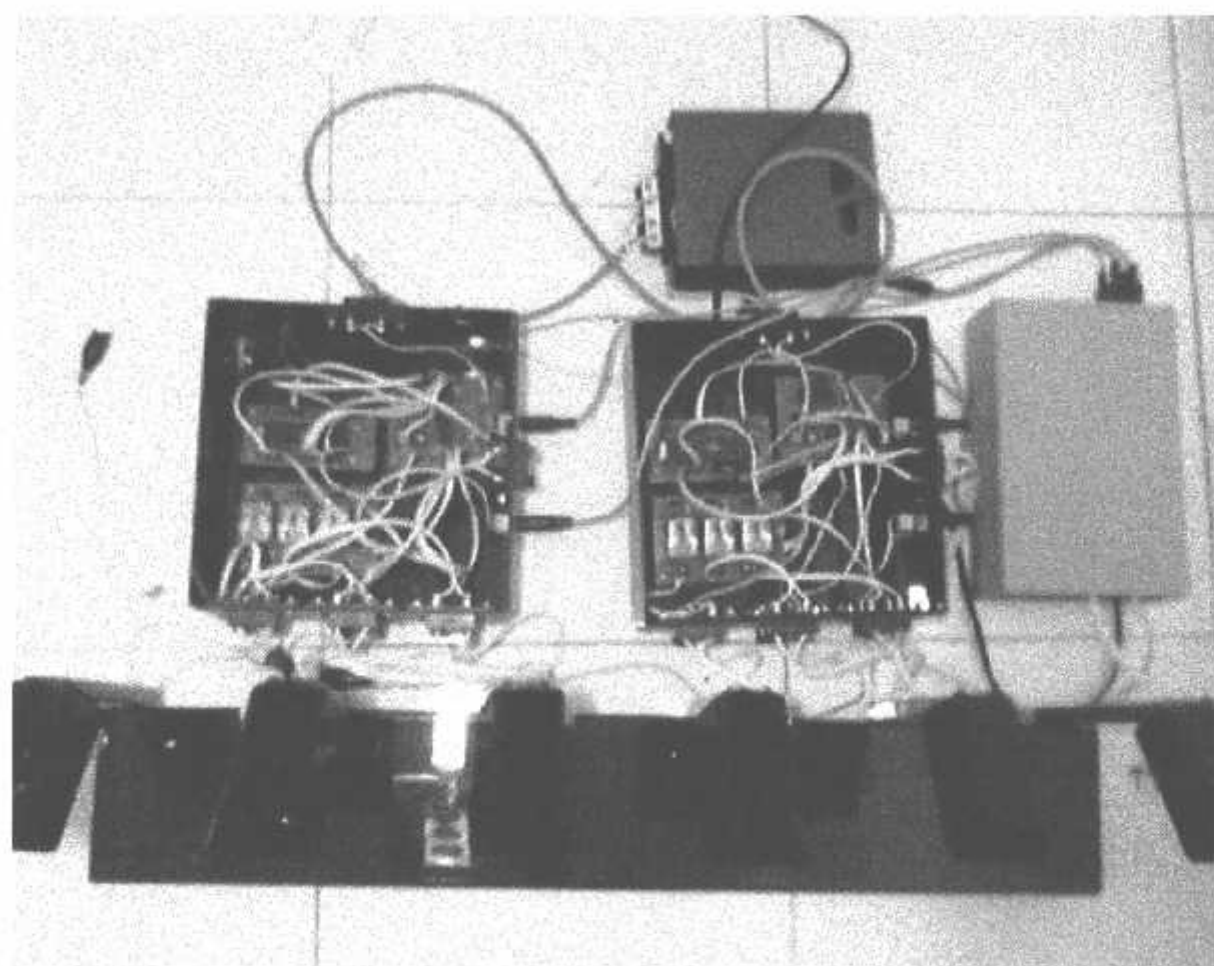
- [1] *Data Sheet Mikrokontroller AT89S51*
 - [2] *Data Sheet ADC0804*
 - [3] *Data Sheet LDR*
 - [4] *Data Sheet LM324*
 - [5] *Data Sheet BD 139*
 - [6] *Data Sheet RS 232*
 - [7] *Data Sheet SN75176*
 - [8] David E. Johnson & V. Jayakumar. *Operational Amplifier Circuits*
 - [9] Wasito S. 1985. *Vademekum Elektronika*. Jakarta: PT Gramedia
 - [10] Dirksen, AJ. 2001. *Buku Delphi 6.0*. Jakarta: Erlangga
-

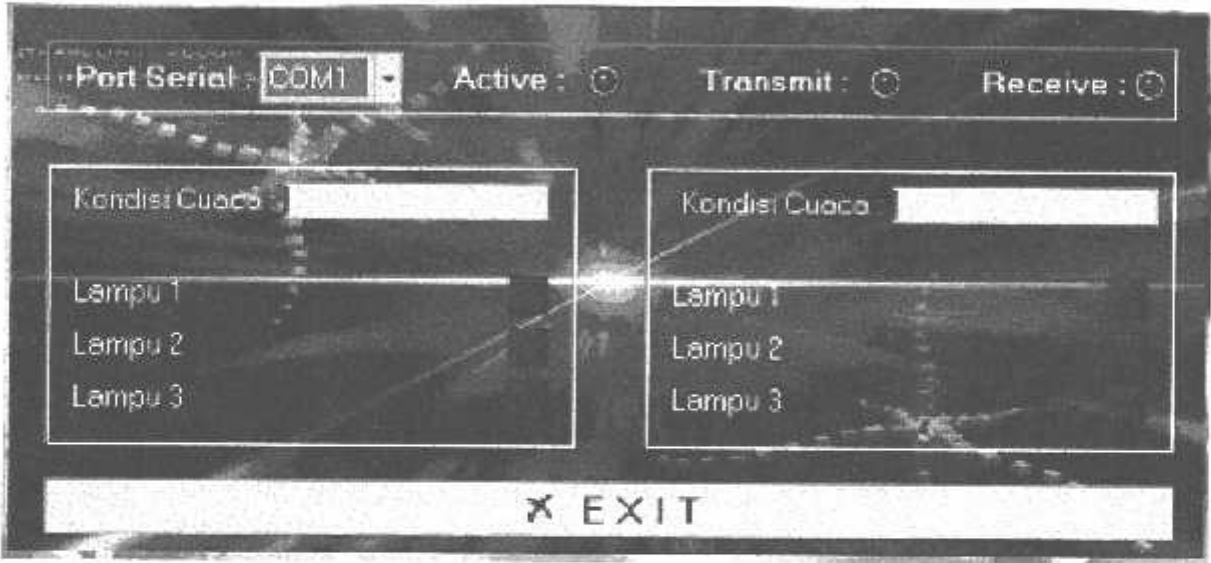
LAMPIRAN



RS-485 to RS-232 CONVERTER

Rev	Rev 1	Rev 2	Rev 3	Rev 4
1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20
21	22	23	24	25
26	27	28	29	30
31	32	33	34	35
36	37	38	39	40
41	42	43	44	45
46	47	48	49	50
51	52	53	54	55
56	57	58	59	60
61	62	63	64	65
66	67	68	69	70
71	72	73	74	75
76	77	78	79	80
81	82	83	84	85
86	87	88	89	90
91	92	93	94	95
96	97	98	99	100





;PINGIRIMAN ALAMAT PERTAMA

```
CALL    KIRIM_ALAMAT
CALL    WAKTU

;1
JNB     LDR_1,MATI_1
MOV     R4,#'B'           ;SATU MATI
CALL    KIRIM
CALL    WAKTU

;2
echo_1: JNB     LDR_2,MATI_2
MOV     R4,#'B'           ;DUA MATI
CALL    KIRIM
CALL    WAKTU

;3
echo_2: JNB     LDR_3,MATI_3
MOV     R4,#'B'           ;TIGA MATI
CALL    KIRIM
LJMP    gamma

MATI_1:  MOV     R4,#'A'           ;SATU HIDUP
CALL    KIRIM
CALL    WAKTU
LJMP    echo_1

MATI_2:  MOV     R4,#'A'           ;DUA HIDUP
CALL    KIRIM
CALL    WAKTU
LJMP    echo_2

MATI_3:  MOV     R4,#'A'           ;TIGA HIDUP
CALL    KIRIM
CALL    WAKTU
```

```
;=====
;
gamma:   MOV     R1,#00
clr     ADC_WR ; start of conversion
setb    ADC_WR
elasy:   djnz    R2,$
djnz    R3,elasy
djnz    R3,$
mov     A,P0
mov     R4,A

MOV     A,#10
MOV     B,A
MOV     A,R4
DIV     AB
MOV     DITI,A
MOV     A,B
MOV     SATUAN,A

;
MOV     A,#10
MOV     B,A
MOV     A,DITI
DIV     AB
MOV     RATUSAN,A
MOV     A,B
MOV     PULUHAN,A

mov     dptr,#angka
MOV     A,SATUAN
MOVC    A,@A+DPTR
mov     satuan,a
```

```

MOV      A,puluhan
MOVC     A,@A+DPTR
mov      puluhan,a

MOV      A,ratusan
MOVC     A,@A+DPTR
mov      ratusan,a

MOV      R4,RATUSAN
CALL     KIRIM
CALL     WAKTU
MOV      R4,PULUHAN
CALL     KIRIM
CALL     WAKTU
MOV      R4,SATUAN
CALL     KIRIM
CALL     WAKTU
LJMP     MULAI

mov      r4,#'Z'
call     kirim
call     waktu
CALL     INTAL
CLR      RE
CLR      DE
SETB     ES
cjne     r1,#'Z',S
mov      r1,#00h
clr      es
call     waktu
LJMP     MULAT

KIRIM_ALAMAT:
setb     EA
setb     RE
setb     DE
call     waktu
mov      TMOD,#20h
mov      TH1,#0FDH
setb     TR1
mov      SCON,#50h
clr      ES
clr      ti
MOV      A,#'k'           ;ALAMAT SATU MICRO
mov      sbuf,A           ;
jnb      ti,$
clr      ti
RET

; PROGRAM UNTUK TRASFER DATA SERIAL
;
INIAL:
setb     EA
mov      TMOD,#20h
mov      TH1,#0FDH
setb     TR1
mov      SCON,#50h
RET

KIRIM:
setb     EA
setb     RE
setb     DE
call     waktu
mov      TMOD,#20h
mov      TH1,#0FDH
setb     TR1
mov      SCON,#50h
clr      ti
clr      ES
MOV      A,R4             ;R4 DATA UNTUK YG DIKIRIM

```

```

        mov     sbuf,A           ;
        jnb     ti,$
        clr     ti
        RET
;PROGRAM INI ADALAH PROGRAM DELAY ANTAR BYTE

waktu:  MOV     R7,#200
        MOV     R6,#150
zulu:   DJNZ    R7,$
        MOV     R7,#200
        DJNZ    R6,zulu
        RET

angka:  DB      '0123456789ABCDEF'

END

```

; LISTING PROGRAM DELPHI UNTUK PUSAT IROLICS ;

```
unit Unit2;

interface

uses
  Windows, Messages, SysUtils, Variants, Classes, Graphics,
  Controls, Forms,
  Dialogs, OleCtrls, ShockwaveFlashObjects_TLB, ExtCtrls,
  AppEvents,
  OutlookBtn;

type
  TSPLASH = class(TForm)
    flash: TShockwaveFlash;
    ApplicationEvents1: TApplicationEvents;
    OutlookBtn1: TOutlookBtn;
    Panel1: TPanel;
    procedure FormCreate(Sender: TObject);
    procedure ApplicationEvents1Message(var Msg: tagMSG;
      var Handled: Boolean);
    procedure OutlookBtn1Click(Sender: TObject);
  private
    { Private declarations }
  public
    { Public declarations }
  end;

var
  SPLASH: TSPLASH;
  S: STRING;
implementation
uses unit1;
{$R *.dfr}

procedure TSPLASH.FormCreate(Sender: TObject);
begin
  getdir(0,s);
  flash.Movie:=s+'/INTRO.swf';
end;

procedure TSPLASH.ApplicationEvents1Message(var Msg: tagMSG;
  var Handled: Boolean);
begin
  if Msg.message = WM_BUTTONDOWN then Handled := True;
end;

procedure TSPLASH.OutlookBtn1Click(Sender: TObject);
begin
  FLASH.Stop;
  HIDE;
  FORM1.Show;
end;

end.
```

```

unit Unit1;

interface

uses
  Windows, Messages, SysUtils, Variants, Classes, Graphics,
  Controls, Forms,
  Dialogs, CPort, StdCtrls, TFlatComboBoxUnit, jpeg, ExtCtrls,
  AVLabelPack,
  CPortCtl, TFlatHintUnit, TFlatProgressBarUnit, TFlatButtonUnit,
  OleCtrls, WavePlay;

type
  TForm1 = class(TForm)
    cb1: TFlatComboBox;
    ComPort1: TComPort;
    pb1: TFlatProgressBar;
    pb2: TFlatProgressBar;
    ComLed1: TComLed;
    ComLed2: TComLed;
    ComLed3: TComLed;
    Label1: TLabel;
    Label2: TLabel;
    Label3: TLabel;
    Label4: TLabel;
    Label5: TLabel;
    Label6: TLabel;
    Bevel1: TBevel;
    Bevel2: TBevel;
    Bevel3: TBevel;
    Image1: TImage;
    L1: TAVLedLabel;
    L2: TAVLedLabel;
    L3: TAVLedLabel;
    L4: TAVLedLabel;
    L5: TAVLedLabel;
    L6: TAVLedLabel;
    LER1: TLabel;
    LER2: TLabel;
    LER3: TLabel;
    LER6: TLabel;
    LER5: TLabel;
    LER4: TLabel;
    PLAYER: TPlayerWave;
    FlatButton1: TFlatButton;
    procedure cb1Change(Sender: TObject);
    procedure ComPort1AfterOpen(Sender: TObject);
    procedure ComPort1RxChar(Sender: TObject; Count: Integer);
    procedure FormClose(Sender: TObject; var Action:
      TCloseAction);
    procedure Button2Click(Sender: TObject);
    procedure FormCreate(Sender: TObject);
    procedure FlatButton1Click(Sender: TObject);
  private
    { Private declarations }
  public

```

```

    { Public declarations }
end;

var
    Form1: TForm1;
    data, i: byte;
    datastr: array [1..7] of string;
    APP: STRING;
implementation
{$R *.dfm}

procedure delay(delt: integer);
var tempo: dword;
begin
    temp:=gettickcount+delt;
    repeat
        application.ProcessMessages;
    until gettickcount>temp;
end;

procedure TForm1.cb1Change(Sender: TObject);
begin
    comport1.Close;
    try
        case cb1.ItemIndex of
            0:begin
                comport1.Port:='COM1';
                comport1.Open;
            end;
            1:begin
                comport1.Port:='COM2';
                comport1.Open;
            end;
        end;
    except
        application.MessageBox('Serial Port
Error', 'Error', mb_ok|mb_iconerror);
    end;

end;

procedure TForm1.ComPort1AfterOpen(Sender: TObject);
begin
    delay(1000);
    comport1.SetDTR(false);
    comport1.WriteStr('c');
    comport1.SetDTR(true);
    i:=0;
end;

procedure TForm1.ComPort1RxChar(Sender: TObject; Count: Integer);
var dat: byte;
begin
    inc(i);
    comport1.ReadStr(datastr[i], 1);
    comport1.ClearBuffer(true, true);

```

```

if i=7 then
begin
//=====mikro 1=====//
IF DATASTR[1]='k' THEN
BEGIN
  dat:=strtoint(datastr[5]+datastr[6]+datastr[7]);
  pbl.Position:=round(dat*0.392);
  //lampu 1
  if datastr[2]='B' then
    l1.Lit:=true
  else
    if datastr[2]='A' then
      l1.Lit:=false
    else
      if (datastr[2]='A') AND (PB1.Position <= 50) then
        BEGIN
          PLAYER.Play;
          LER1.Visible:=TRUE;
        END ELSE
        BEGIN
          LER1.Visible:=FALSE;
          PLAYER.Stop;
        END;

  //lampu 2
  if datastr[3]='B' then
    l2.Lit:=true
  else
    if datastr[3]='A' then
      l2.Lit:=false
    else
      if (datastr[3]='A') AND (PB1.Position <= 50) then
        BEGIN
          PLAYER.Play;
          LER2.Visible:=TRUE;
        END ELSE
        BEGIN
          LER2.Visible:=FALSE;
          PLAYER.Stop;
        END;

  //lampu 3
  if datastr[4]='B' then
    l3.Lit:=true
  else
    if datastr[4]='A' then
      l3.Lit:=false
    else
      if (datastr[4]='A') AND (PB1.Position <= 50) then
        BEGIN
          PLAYER.Play;
          LER3.Visible:=TRUE;
        END ELSE
        BEGIN
          LER3.Visible:=FALSE;
          PLAYER.Stop;
        END;

```

```

END;
DELAY(500);
//panggil data mikro 2
comport1.SetDTR(false);
comport1.Writestr('2');
comport1.SetDTR(true);
i:=0;
end;

//=====mikro 1=====//
IF DATASTR[1]='1' THEN
BEGIN
  dat:=strtoint(datastr[5]+datastr[6]+datastr[7]);
  pb2.Position:=round(dat*0.392);
  //lampu 1
  if datastr[2]='B' then
    l4.Lit:=true
  else
    if datastr[2]='A' then
      l4.Lit:=false
    else
      if (datastr[2]='A') AND (PB2.Position < 50) then
        BEGIN
          PLAYER.Play;
          LER4.Visible:=TRUE;
        END ELSE
        BEGIN
          LER4.Visible:=FALSE;
          PLAYER.Stop;
        END;

      //lampu 2
      if datastr[3]='B' then
        l5.Lit:=true
      else
        if datastr[3]='A' then
          l5.Lit:=false
        else
          if (datastr[3]='A') AND (PB2.Position <= 50) then
            BEGIN
              PLAYER.Play;
              LER5.Visible:=TRUE;
            END ELSE
            BEGIN
              LER5.Visible:=FALSE;
              PLAYER.Stop;
            END;

            //lampu 3
            if datastr[4]='B' then
              l6.Lit:=true
            else
              if datastr[4]='A' then
                l6.Lit:=false
              else
                if (datastr[4]='A') AND (PB2.Position <= 50) then

```

```

    BEGIN
        PLAYER.Play;
        LER6.Visible:=TRUE;
    END ELSE
    BEGIN
        LER6.Visible:=FALSE;
        PLAYER.Stop;
    END;
    DELAY(500);
    //panggil data mikro 1
    comport1.SetDTR(false);
    comport1.Writestr('e');
    comport1.SetDTR(true);
    i:=0;
end;
i:=0;
end;
end;

procedure TForm1.FormClose(Sender: TObject; var Action:
TCloseAction);
begin
    application.Terminate;
end;

procedure TForm1.Button2Click(Sender: TObject);
begin
    application.Terminate;
end;

procedure TForm1.FormCreate(Sender: TObject);
begin
    GETDIR(0,APP);
    PLAYER.WaveName:=APP+'\ERROR.WAV';
end;

procedure TForm1.FlatButton1Click(Sender: TObject);
begin
    APPLICATION.Terminate;
end;

end.

```

LM124/LM224/LM324/LM2902

Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional $\pm 15V$ power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

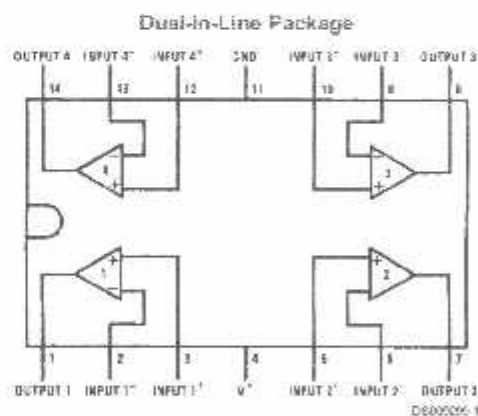
Advantages

- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz (temperature compensated)
- Wide power supply range:
Single supply: 3V to 32V
or dual supplies: $\pm 1.5V$ to $\pm 16V$
- Very low supply current drain (700 μA)—essentially independent of supply voltage
- Low input biasing current: 45 nA (temperature compensated)
- Low input offset voltage: 2 mV and offset current: 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing: 0V to $V^+ - 1.5V$

Connection Diagram



Order Number LM124J, LM124AJ, LM124J/883 (Note 2), LM124AJ/883 (Note 1), LM224J, LM224AJ, LM324M, LM324MX, LM324AM, LM324AMX, LM2902M, LM2902MX, LM324N, LM324AN, LM324MT, LM324MTX or LM2902N LM124AJRQML and LM124AJRQMLV (Note 3)

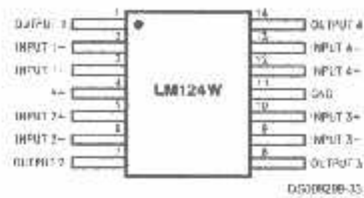
See NS Package Number J14A, M14A or N14A

Note 1: LM124A available per JANS510/1100C

Note 2: LM124 available per JANS510/1100C

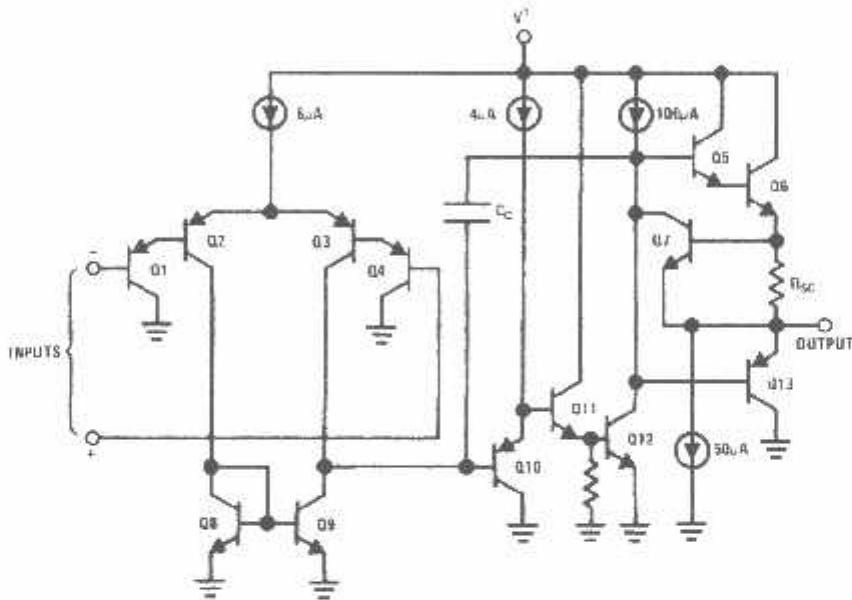
Connection Diagram (Continued)

Note 3: See STD M01WG/8862R98524 for Radiation Tolerant Design



Order Number LM124AW/883, LM124AWG/883, LM124W/883 or LM124WG/883
LM124AWRQML and LM124AWRQMLV(Note 3)
See NS Package Number W14B
LM124AWGRQML and LM124AWGRQMLV(Note 3)
See NS Package Number WG14A

Schematic Diagram (Each Amplifier)



Absolute Maximum Ratings (Note 12)

Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	+0.3V to +32V	-0.3V to +26V
Input Current ($V_{in} \leq -0.3V$) (Note 6)	50 mA	50 mA
Power Dissipation (Note 4)		
Molded DIP	1130 mW	1130 mW
Cavity DIP	1260 mW	1260 mW
Small Outline Package	800 mW	800 mW
Output Short-Circuit to GND (One Amplifier) (Note 5)		
$V^+ \leq 15V$ and $T_A = 25^\circ C$	Continuous	Continuous
Operating Temperature Range		-40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	-25°C to +85°C	
LM124/LM124A	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD Tolerance (Note 13)	250V	250V

Electrical Characteristics

$V^+ = +5.0V$, (Note 7), unless otherwise stated

Parameter	Conditions	LM124A			LM224A			LM324A			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Offset Voltage	(Note 8); $T_A = 25^\circ C$	1	2		1	3		2	3		mV
Output Bias Current (Note 9)	I_{BQ1} or I_{BQ2} ; $V_{CM} = 0V$, $T_A = 25^\circ C$	20	50		30	80		45	100		nA
Output Offset Current	I_{BQ1} or I_{BQ2} ; $V_{CM} = 0V$, $T_A = 25^\circ C$	2	10		2	15		5	30		nA
Output Common-Mode Voltage Range (Note 10)	$V^+ = 30V$ (LM2902; $V^+ = 26V$), $T_A = 25^\circ C$	0	$V^+ - 1.5$		0	$V^+ - 1.5$		0	$V^+ - 1.5$		V
Supply Current	Over Full Temperature Range I_{B1} or I_{B2} On All Op Amps $V^+ = 30V$ (LM2902; $V^+ = 26V$) $V^+ = 5V$		1.5 0.7	3 1.2		1.5 0.7	3 1.2		1.5 0.7	3 1.2	mA
Open-Loop Voltage Gain	$V^+ = 10V$, $R_L \geq 2k\Omega$, ($V_{OS} = 1V$ to $11V$); $T_A = 25^\circ C$	50	100		50	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, $V_{CM} = 0V$ to $V^+ - 1.5V$, $T_A = 25^\circ C$	70	85		70	85		65	85		dB

Electrical Characteristics (Continued)

 $V^+ = +5.0V$, (Note 7), unless otherwise stated

Parameter	Conditions	LM124A			LM224A			LM324A			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply Rejection Ratio	$V^+ = 5V$ to $30V$ (LM2902, $V^+ = 5V$ to $26V$), $T_A = 25^\circ C$	65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling (Note 11)	$f = 1 kHz$ to $20 kHz$, $T_A = 25^\circ C$ (Input Referred)			-120			-120			-120	dB
Output Current	Source $V_{in}^+ = 1V$, $V_{in}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25^\circ C$	20	40		20	40		20	40		mA
	Sink $V_{in}^+ = +1V$, $V_{in}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25^\circ C$	10	20		10	20		10	20		mA
	$V_{in}^+ = 1V$, $V_{in}^- = 0V$, $V^+ = 15V$, $V_O = 200 mV$, $T_A = 25^\circ C$	12	50		12	50		12	50		μA
Short Circuit to Ground	(Note 5) $V^+ = 15V$, $T_A = 25^\circ C$		40	60		40	60		40	60	mA
Input Offset Voltage	(Note 8)			4			4			6	mV
V_{OS} Drift	$R_S = 0\Omega$		7	20		7	20		7	30	$\mu V/^\circ C$
Input Offset Current	$I_{B1} = I_{B2}$, $V_{OS} = 0V$			30			30			75	nA
I_{OS} Drift	$R_S = 0\Omega$		10	200		10	200		10	300	pA/°C
Input Bias Current	I_{B1} or I_{B2}		40	100		40	100		40	200	nA
Input Common-Mode Voltage Range (Note 10)	$V^+ = +30V$ (LM2902, $V^+ = 26V$)	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V
Large Signal Voltage Gain	$V^+ = +15V$ (V_O Swing = $1V$ to $+11V$) $R_L \geq 2 k\Omega$		25			25			15		V/mV
Output Voltage Swing	V_{OH} $V^+ = 30V$, $R_L = 2 k\Omega$ (LM2902, $V^+ = 26V$)		26			20			26		V
	V_{OL} $V^+ = 30V$, $R_L = 10 k\Omega$		5	20		5	20		5	20	mV
Output Current	Source $V_O = 2V$		10	20		10	20		10	20	mA
	Sink $V_O = 2V$		10	15		5	8		5	8	mA

Electrical Characteristics

 $V^+ = +5.0V$, (Note 7), unless otherwise stated

Parameter	Conditions	LM124/LM224			LM324			LM2902			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 8) $T_A = 25^\circ C$		2	5		2	7		2	7	mV
Input Bias Current (Note 9)	I_{B1} or I_{B2} , $V_{CM} = 0V$, $T_A = 25^\circ C$		45	150		45	250		45	250	nA
Input Offset Current	$I_{B1} = I_{B2}$, $V_{CM} = 0V$, $T_A = 25^\circ C$		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range (Note 10)	$V^+ = 30V$, (LM2902, $V^+ = 26V$), $T_A = 25^\circ C$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	Over Full Temperature Range $R_L = 750\Omega$ A ⁻¹ Op.Amps. $V^+ = 50V$ (LM2902 $V^+ = 26V$) $V^+ = 5V$		1.5	3		1.5	3		1.5	3	mA
			0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain	$V^+ = 15V$, $R_L > 2k\Omega$ ($V_O = 1V$ to $11V$), $T_A = 25^\circ C$		60	100		25	100		25	100	V/mV
Common-Mode Rejection Ratio	DC, $V_{CM} = 0V$ to $V^+ - 1.5V$, $T_A = 25^\circ C$		70	85		65	85		50	70	dB
Power Supply Rejection Ratio	$V^+ = 5V$ to $30V$ (LM2902, $V^+ = 5V$ to $26V$)		65	100		65	100		50	100	dB

Electrical Characteristics (Continued)

* $V^+ = +5.0V$ (Note 7), unless otherwise stated.

Parameter		Conditions	LM124/LM224			LM324			LM2902			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		$T_A = 25^\circ\text{C}$										
Input-to-Amplifier Coupling (Note 11)		$f = 1\text{ kHz to } 20\text{ kHz}$, $T_A = 25^\circ\text{C}$ (Input Referred)		-120			-120			-120		dB
Output Current	Source	$V_{IN} = 1\text{V}$, $V_{IN} = 0\text{V}$, $V^+ = 15\text{V}$, $V_O = 2\text{V}$, $T_A = 25^\circ\text{C}$	20	40		20	40		20	40		mA
	Sink	$V_{IN} = 1\text{V}$, $V_{IN} = 0\text{V}$, $V^+ = 15\text{V}$, $V_O = 2\text{V}$, $T_A = 25^\circ\text{C}$	10	20		10	20		10	20		
			$V_{IN} = 1\text{V}$, $V_{IN} = 0\text{V}$, $V^+ = 15\text{V}$, $V_O = 200\text{ mV}$, $T_A = 25^\circ\text{C}$	12	50		12	50		12	50	
Output Circuit to Ground		(Note 5) $V^+ = 15\text{V}$, $T_A = 25^\circ\text{C}$		40	60		40	60		40	60	nA
Output Offset Voltage		(Note 8)			7			0			10	mV
V_O Drift		$R_G = 0\Omega$		7			7			7		$\mu\text{V}/^\circ\text{C}$
Output Offset Current		$I_{BQ1} = I_{BQ2}$, $V_{CM} = 0\text{V}$			100			150		45	200	nA
V_O Drift		$R_G = 0\Omega$		10			10			10		$\mu\text{A}/^\circ\text{C}$
Output Bias Current		I_{BQ1} or I_{BQ2}		40	300		40	500		40	500	nA
Output Common-Mode Voltage Range (Note 10)		$V^+ = +50\text{V}$ (LM2902, $V^+ = 28\text{V}$)	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V
Input Signal Voltage (Gain)		$V^+ = +15\text{V}$, V_O Swing = 1V to 11V , $R_L \geq 2\text{ k}\Omega$		25			15			15		V _{rms}
Input Voltage Slew	V_{OH}	$V^+ = 30\text{V}$ (LM2902, $V^+ = 25\text{V}$)	$R_L = 2\text{ k}\Omega$			26			$R_L = 10\text{ k}\Omega$			V
	V_{OL}	$V^+ = 5\text{V}$, $R_L = 10\text{ k}\Omega$	27			26			23			
Input Current	Source	$V_O = 2\text{V}$	$V_{IN} = +1\text{V}$, $V_{IN} = 0\text{V}$, $V^+ = 15\text{V}$			10			$V_{IN} = +1\text{V}$, $V_{IN} = 0\text{V}$, $V^+ = 15\text{V}$			mA
	Sink		$V_{IN} = +1\text{V}$, $V_{IN} = 0\text{V}$, $V^+ = 15\text{V}$			5			$V_{IN} = +1\text{V}$, $V_{IN} = 0\text{V}$, $V^+ = 15\text{V}$			

note 4: For operation at high temperatures, the LM224/LM244/LM2902 must be derated based on a $+25^\circ C$ maximum junction temperature and a thermal resistance of $88^\circ C/W$ which applies for the device soldered in a printed circuit board operating in a still air ambient. The LM224/LM244 and LM124/LM124A can be derated based on a $+150^\circ C$ maximum junction temperature. This dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the on-chip filter to saturate or to reduce the power which is dissipated in the integrated circuit.

note 5: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+ . At values of supply voltage in excess of $+15V$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

note 6: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also internal NPN parasitic transistor action on the chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that a input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V$ (at $25^\circ C$).

note 7: These specifications are limited to $-55^\circ C \leq T_A \leq +125^\circ C$ for the LM124/LM124A. With the LM224/LM244, all temperature specifications are limited to $-25^\circ C \leq T_A \leq +85^\circ C$, the LM244/LM244A temperature specifications are limited to $0^\circ C \leq T_A \leq +70^\circ C$, and the LM2902 specifications are limited to $-40^\circ C \leq T_A \leq +85^\circ C$.

note 8: $V_O = 1.4V$, $R_G = 0\Omega$ with V^+ from $5V$ to $30V$; and over the full input common-mode range ($0V$ to $V^+ - 1.5V$) for LM2902, V^+ from $5V$ to $28V$.

note 9: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

note 10: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than $0.3V$ (at $25^\circ C$). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at $25^\circ C$), but either or both inputs can go to $-42V$ without damage ($+25V$ for LM2902), independent of the magnitude of V^+ .

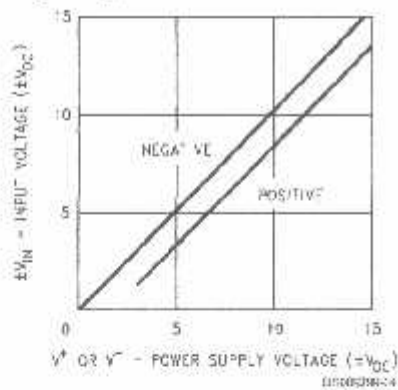
note 11: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be expected as this type of capacitance increases at higher frequencies.

note 12: Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124 military specifications.

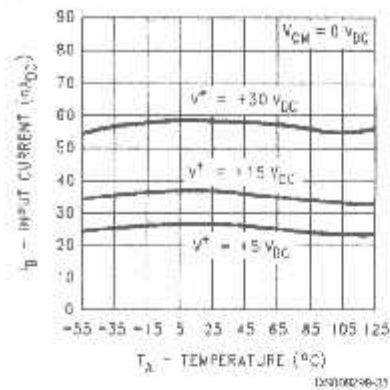
note 13: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Typical Performance Characteristics

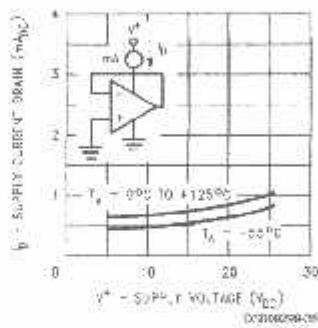
Input Voltage Range



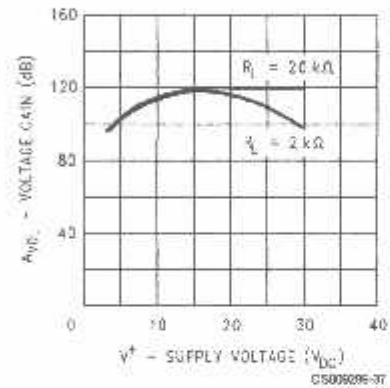
Input Current



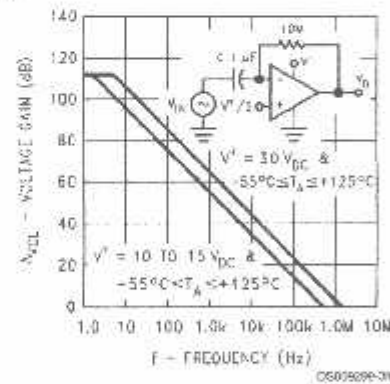
Supply Current



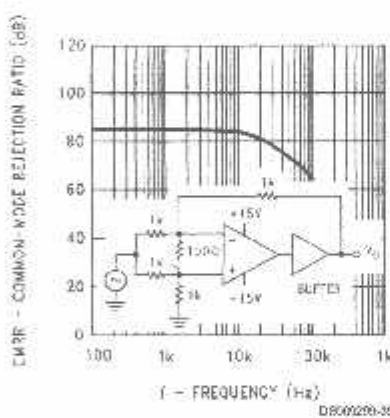
Voltage Gain



Open Loop Frequency Response

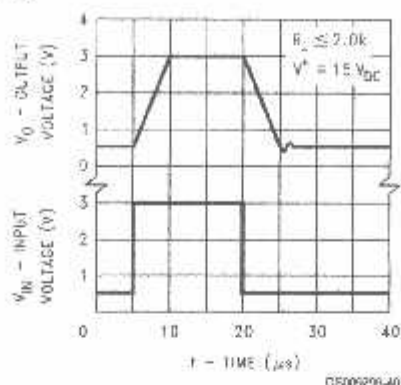


Common Mode Rejection Ratio

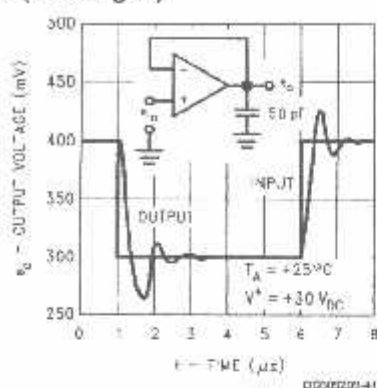


Typical Performance Characteristics (Continued)

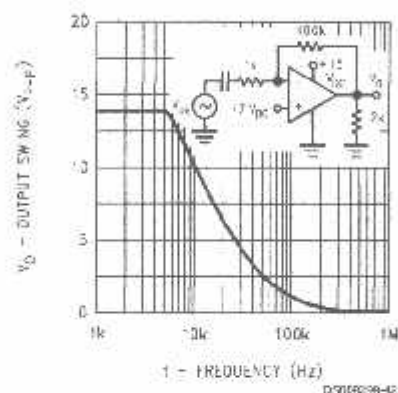
Voltage Follower Pulse Response



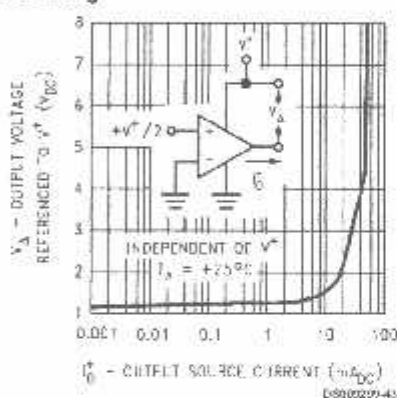
Voltage Follower Pulse Response (Small Signal)



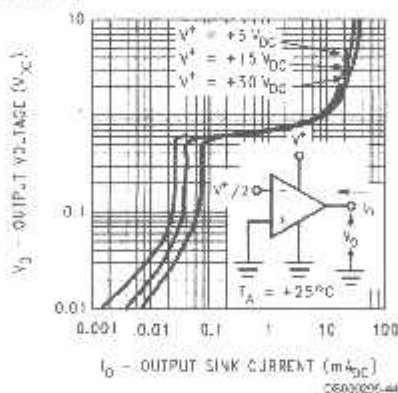
Large Signal Frequency Response



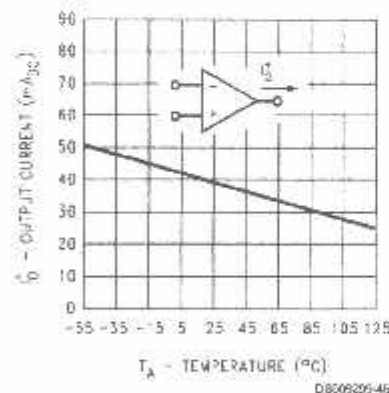
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

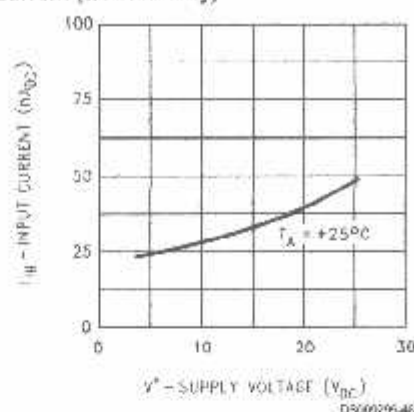


Current Limiting

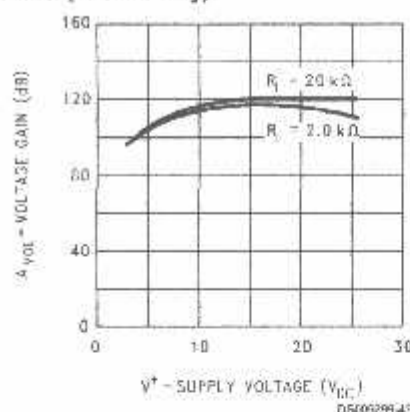


Typical Performance Characteristics (Continued)

Input Current (LM2902 only)



Voltage Gain (LM2902 only)



Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{CC} . These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{CC} .

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V_{CC} without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{CC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

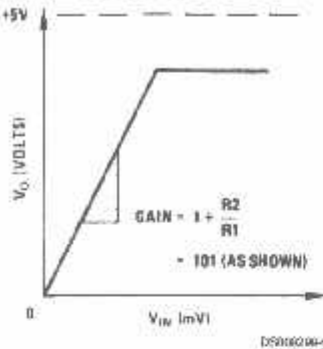
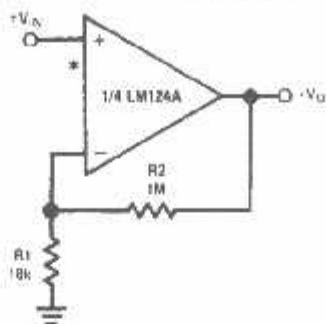
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{CC} to 30 V_{CC} .

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels. If not properly protected with external dissipation limiting resistors in series with the output loads of the amplifiers, the larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V_{CC}/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{\text{DC}}$)

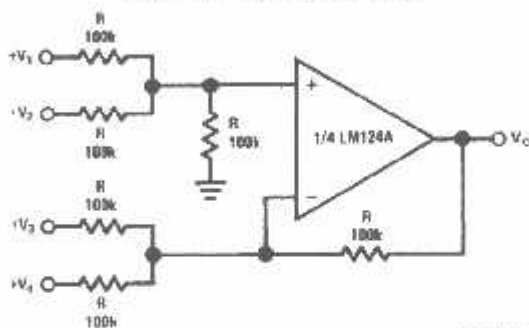
Non-Inverting DC Gain (0V Input = 0V Output)



DS000094-5

R not needed due to temperature independent I_{IH}

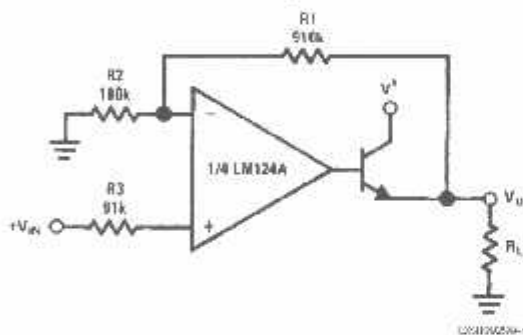
DC Summing Amplifier ($V_{\text{IN}15} \geq 0\text{ V}_{\text{DC}}$ and $V_O \geq V_{\text{DC}}$)



DS000094-5

Here: $V_O = V_1 + V_2 - V_3 - V_4$
 $(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O \geq 0\text{ V}_{\text{DC}}$

Power Amplifier

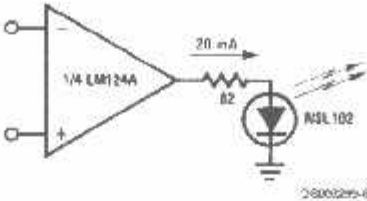


DS000094-5

$V_O = 0\text{ V}_{\text{DC}}$ for $V_{\text{IN}} = 0\text{ V}_{\text{DC}}$
 $A_V = 10$

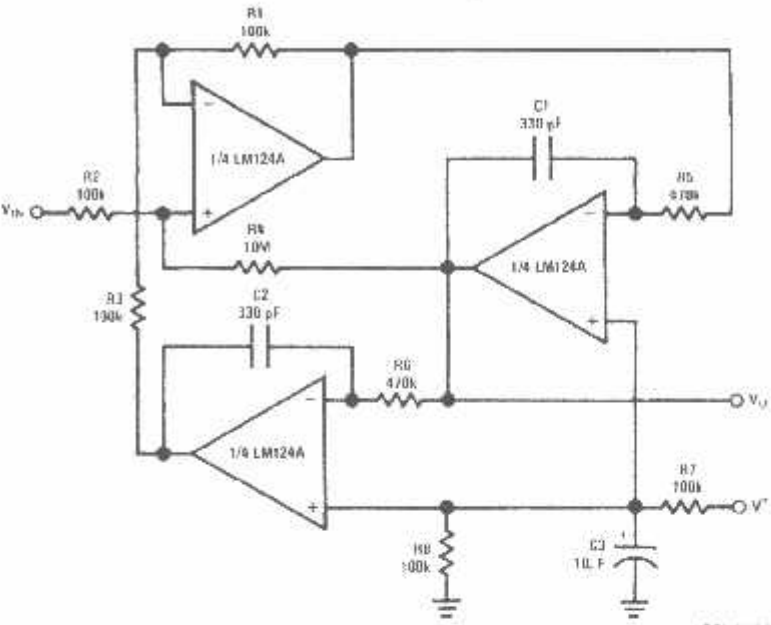
Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{DC}$) (Continued)

LED Driver



D5000295-8

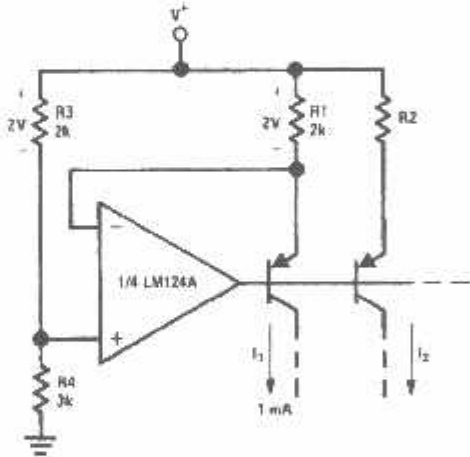
"BI-QUAD" RC Active Bandpass Filter



D5004298-9

$f_0 = 1\text{ kHz}$
 $Q = 50$
 $A_v = 100\text{ (40 dB)}$

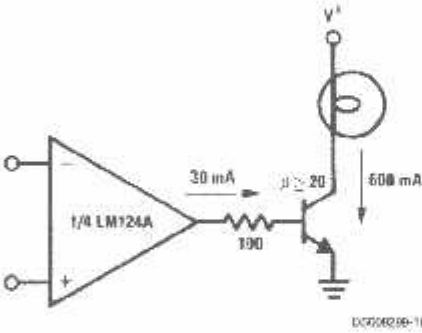
Fixed Current Sources



D5000298-10

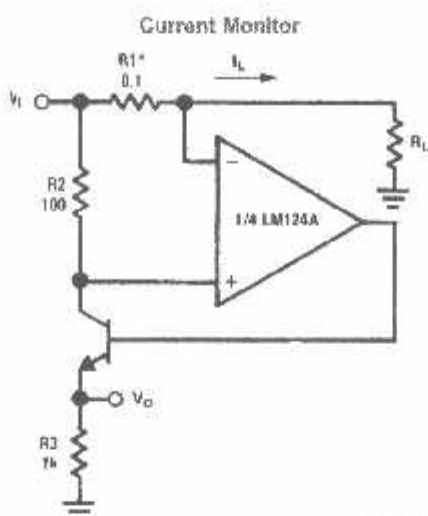
$$I_2 = \left(\frac{R1}{R2} \right) I_1$$

Lamp Driver



D5000298-11

Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{OC}$) (Continued)

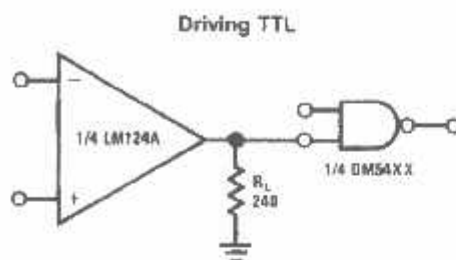


DS000295-12

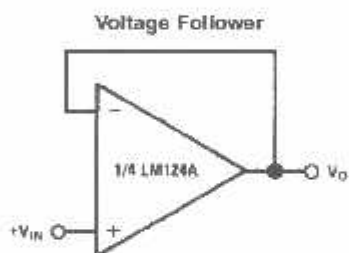
$$V_O = \frac{1V^+ I_L}{1A}$$

$$V_L < V^+ - 2V$$

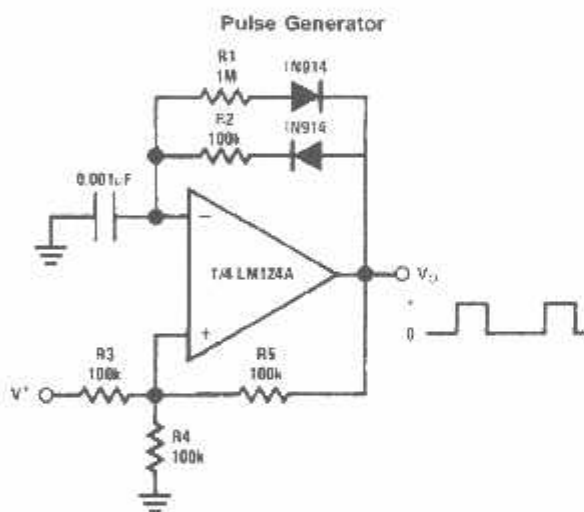
(Increase R1 for I_L small)



DS000295-13



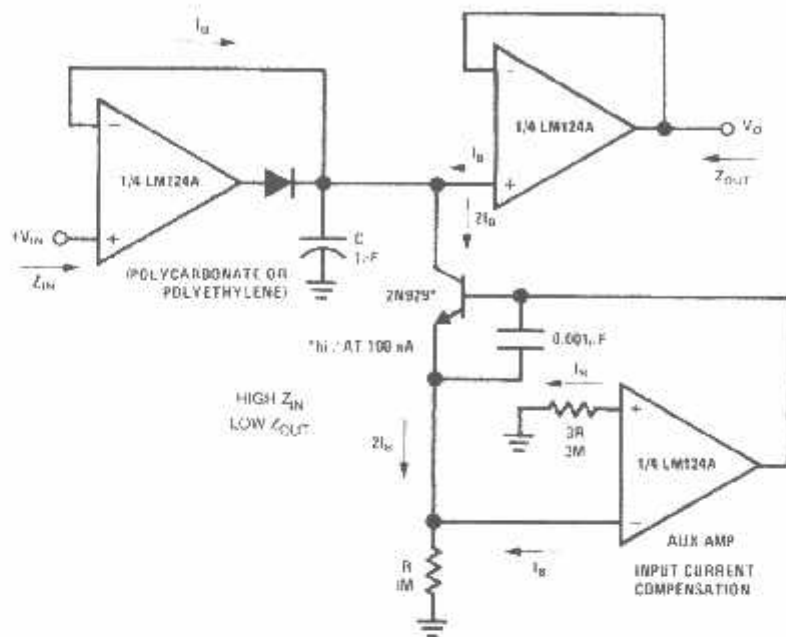
DS000295-14



DS000295-15

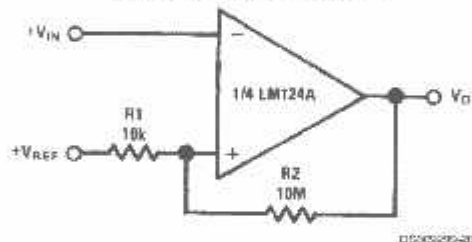
Typical Single-Supply Applications ($V^+ = 5.0 V_{DD}$) (Continued)

Low Drift Peak Detector



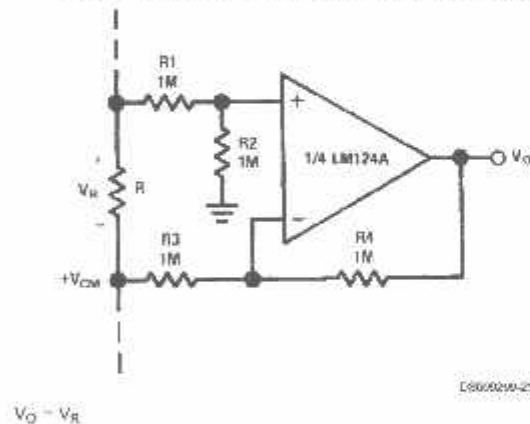
CS000219-19

Comparator with Hysteresis



CS000219-20

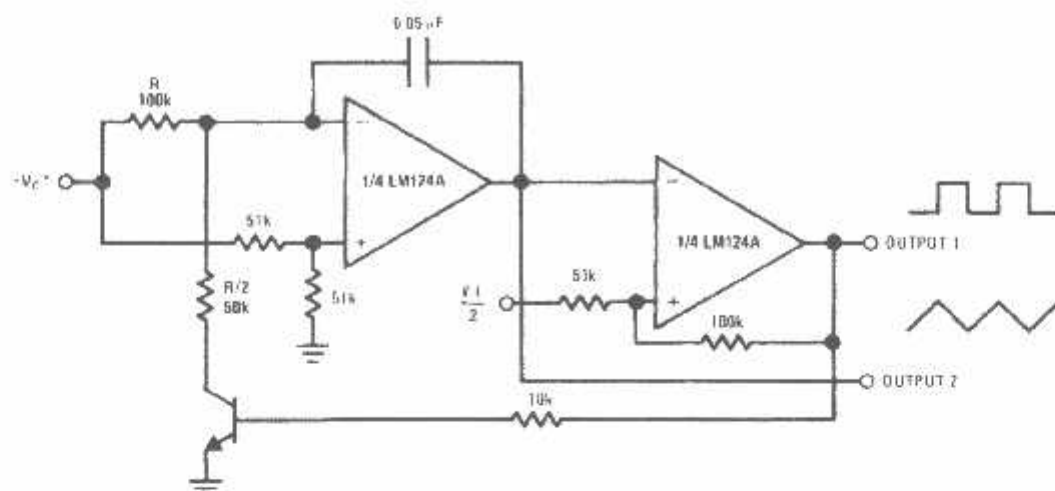
Ground Referencing a Differential Input Signal



CS000219-21

Typical Single-Supply Applications $(V^+ = 5.0 V_{DC})$ (Continued)

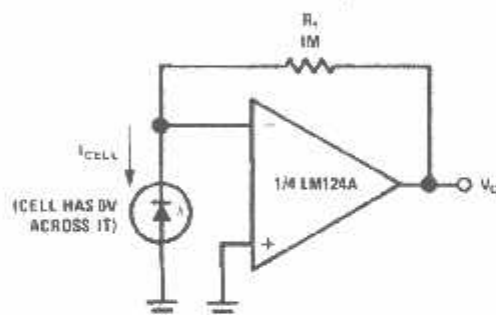
Voltage Controlled Oscillator Circuit



DS009299-22

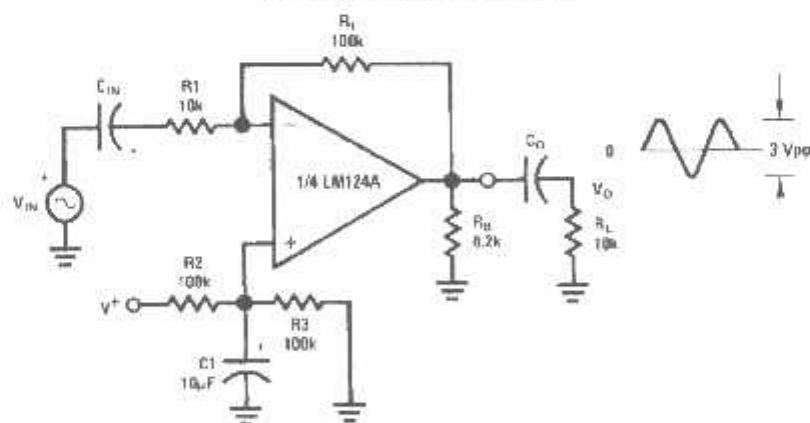
*Wide control voltage range: $0 V_{DC} < V_C < 2 (V^+ - 1.5 V_{DC})$

Photo Voltaic-Cell Amplifier



DS009299-23

AC Coupled Inverting Amplifier

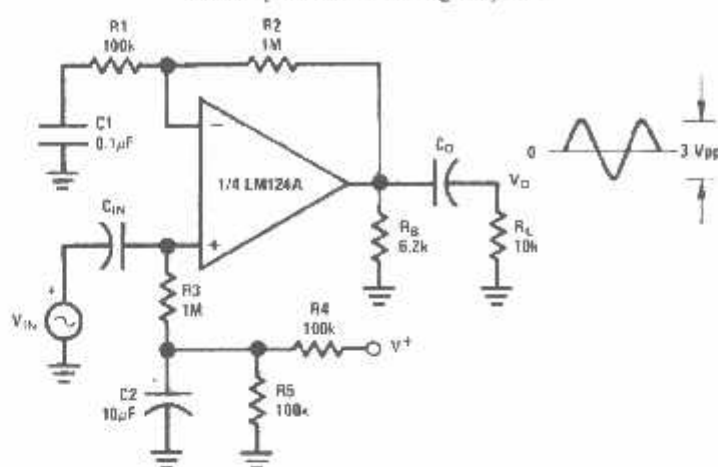


DS009299-24

$$A_V = \frac{R_F}{R_1} \text{ (As shown, } A_V = 10 \text{)}$$

Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{\text{DC}}$) (Continued)

AC Coupled Non-Inverting Amplifier

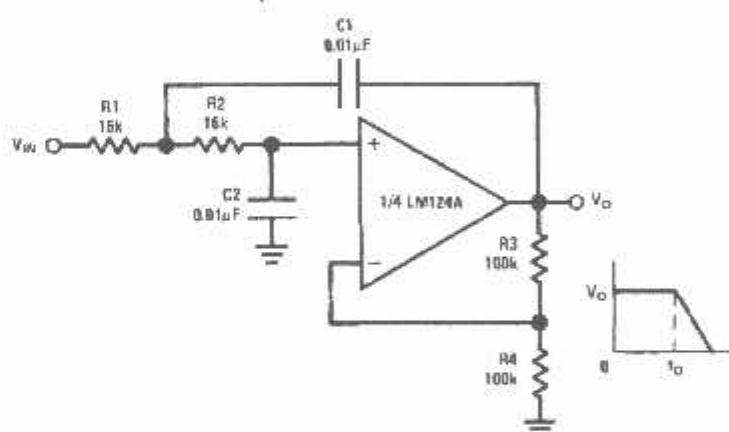


DS900295-2c

$$A_V = 1 + \frac{R2}{R1}$$

 $A_V = 11$ (As shown)

DC Coupled Low-Pass RC Active Filter



DS900295-2b

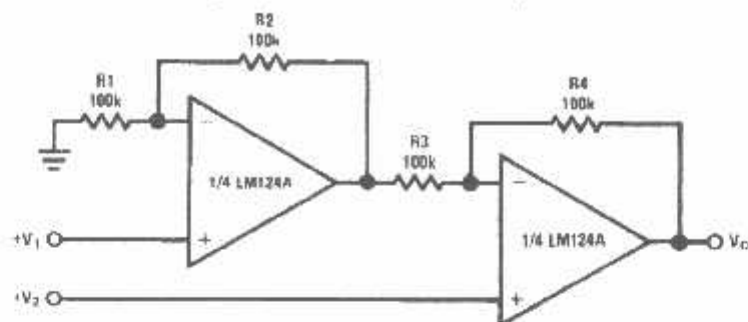
$$\omega = 1\text{ kHz}$$

$$\omega = 1$$

$$\omega = 2$$

Typical Single-Supply Applications $(V^+ = 5.0 V_{CC})$ (Continued)

High Input Z, DC Differential Amplifier



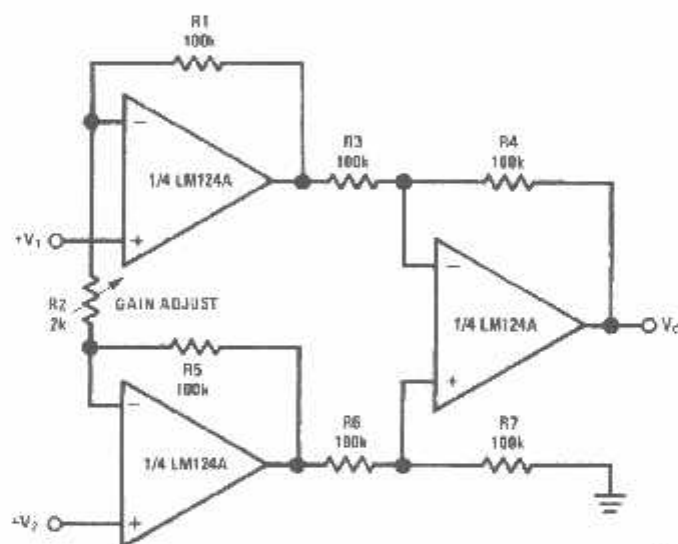
DS000200-22

For $\frac{R^+}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$$V_O = 1 + \frac{R4}{R3} (V_2 - V_1)$$

As shown: $V_O = 2(V_2 - V_1)$

High Input Z Adjustable-Gain DC Instrumentation Amplifier



DS000200-23

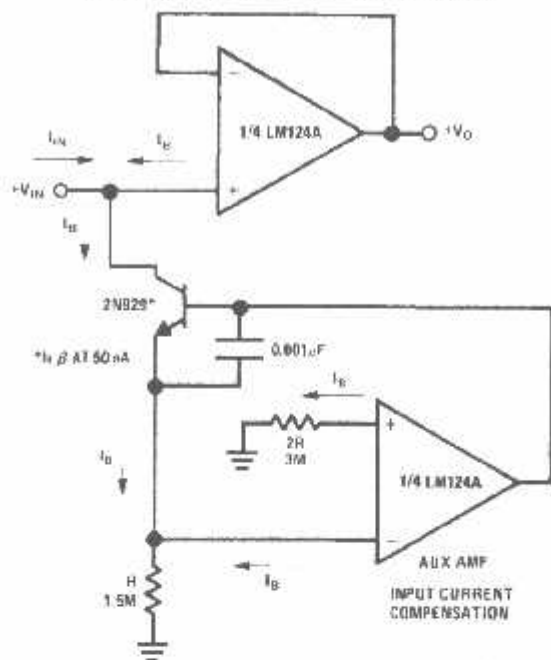
If $R1 = R5$ & $R3 = R4 = R6 = R7$ (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2} (V_2 - V_1)$$

As shown: $V_O = 101 (V_2 - V_1)$

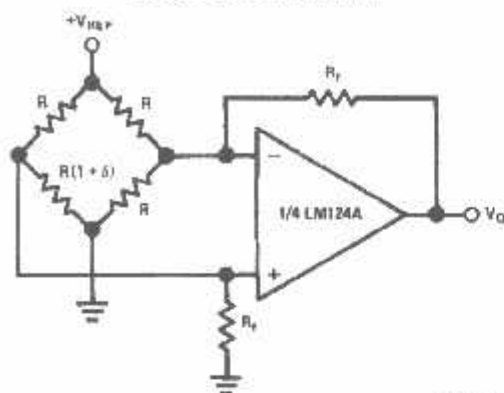
Typical Single-Supply Applications ($V^+ = 5.0 V_{CC}$) (Continued)

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



D0200298-29

Bridge Current Amplifier

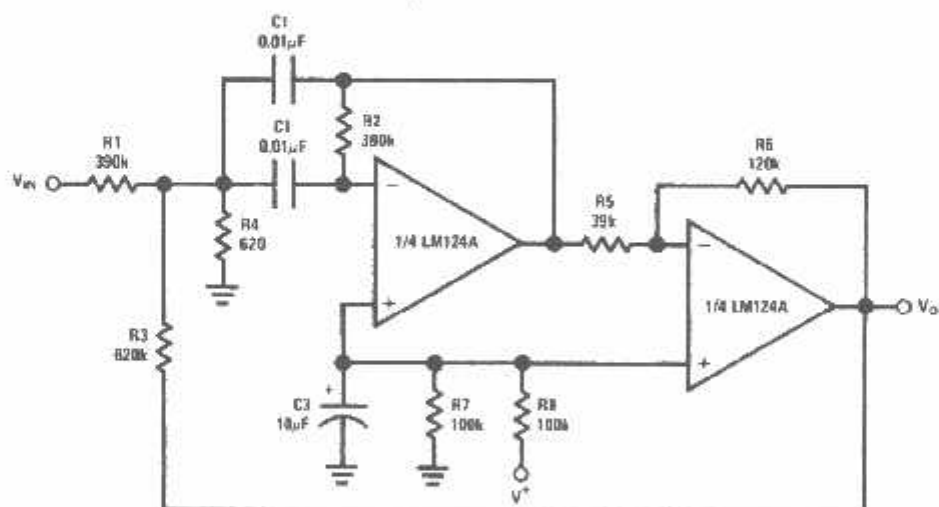


D0000294-30

For $\delta \ll 1$ and $R_f \gg R$

$$V_O \approx V_{REF} \left(\frac{5}{2} \right) \frac{R_f}{R}$$

Bandpass Active Filter

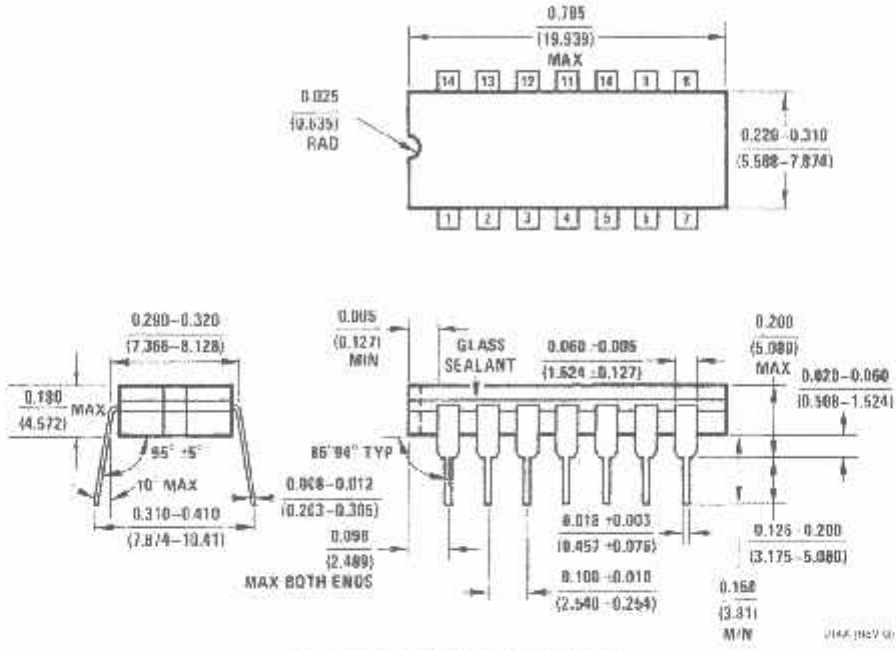


D3000298-31

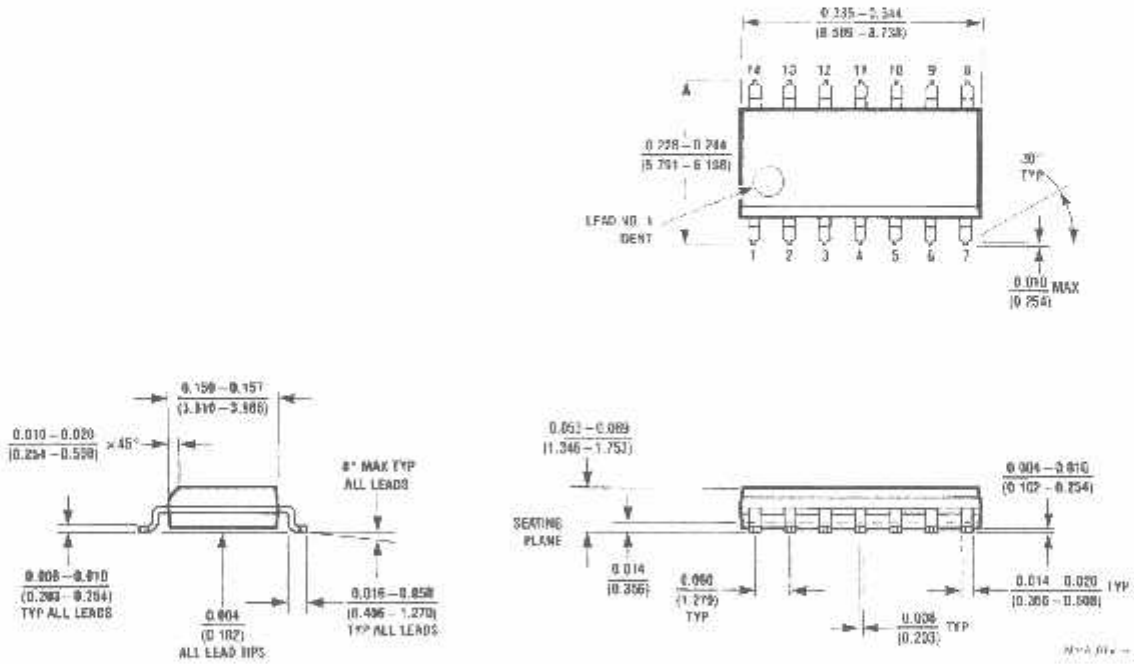
$f_c = 1 \text{ kHz}$
 $Q = 25$

Physical Dimensions

inches (millimeters) unless otherwise noted

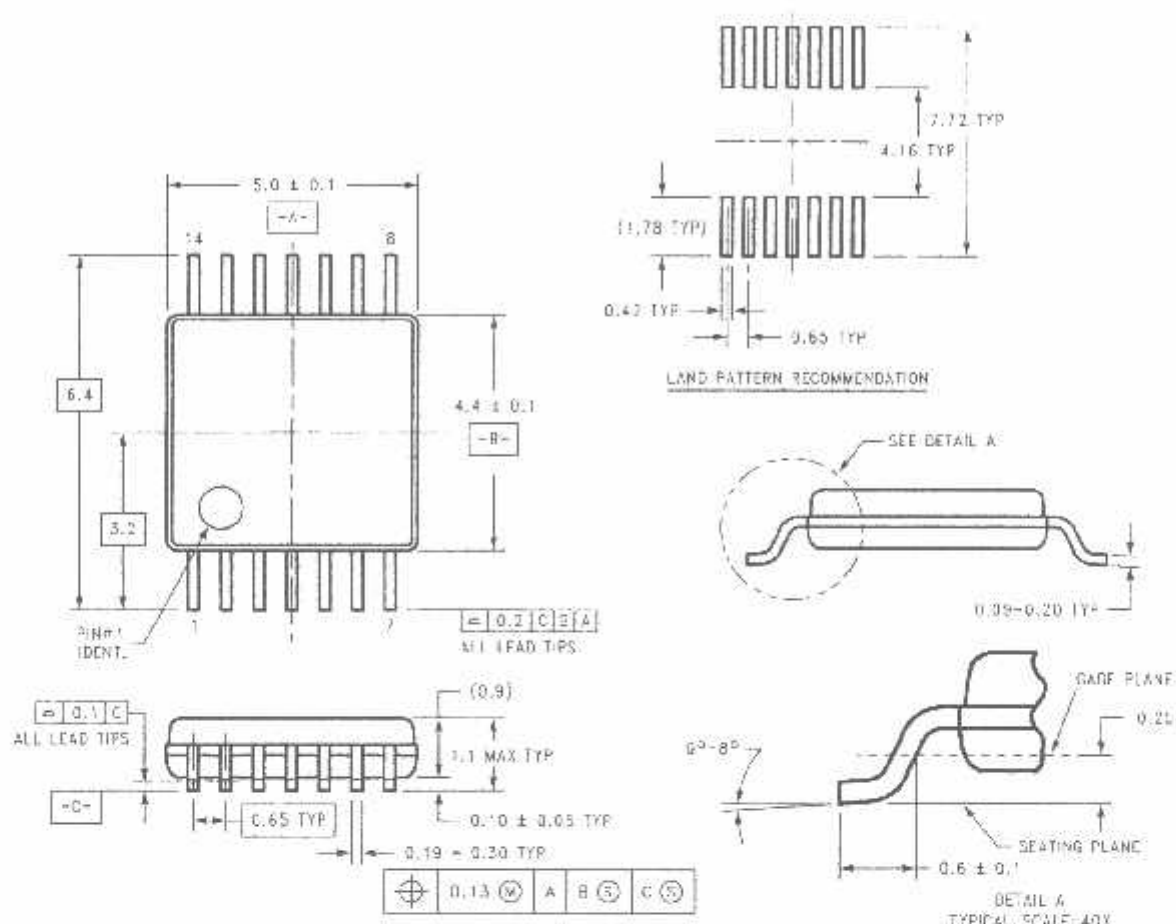


Ceramic Dual-In-Line Package (J)
 Order Number JL124ABCA, JL124BCA, JL124ASCA, JL124SCA, LM124J,
 LM124AJ, LM124AJ/883, LM124J/883, LM224J, LM224AJ or LM324J
 NS Package Number J14A



MX S.O. Package (M)
 Order Number LM324M, LM324MX, LM324AM, LM324AMX, LM2902M or LM2902MX
 NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



BD135/137/139

Medium Power Linear and Switching Applications

• Complement to BD136, BD138 and BD140 respectively

TO-18
1. Emitter 2. Collector 3. Base

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings $T_C=25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CB0}	Collector-Base Voltage : BD135	45	V
	: BD137	60	V
	: BD139	80	V
V_{CE0}	Collector-Emitter Voltage : BD135	45	V
	: BD137	60	V
	: BD139	80	V
V_{EB0}	Emitter-Base Voltage	5	V
I_C	Collector Current (DC)	1.5	A
I_{CP}	Collector Current (Pulse)	3.0	A
I_B	Base Current	0.5	A
P_C	Collector Dissipation ($T_C=25^{\circ}\text{C}$)	12.5	W
P_C	Collector Dissipation ($T_J=25^{\circ}\text{C}$)	1.25	W
T_J	Junction Temperature	150	$^{\circ}\text{C}$
T_{STG}	Storage Temperature	-55 ~ 150	$^{\circ}\text{C}$

Electrical Characteristics $T_C=25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$V_{CE0(sus)}$	Collector-Emitter Sustaining Voltage	$I_C = 30\text{mA}, I_B = 0$				
	: BD135		45		V	
	: BD137		60		V	
	: BD139		80		V	
I_{CB0}	Collector Cut-off Current	$V_{CB} = 30\text{V}, I_E = 0$			0.1	μA
I_{EB0}	Emitter Cut-off Current	$V_{EB} = 5\text{V}, I_C = 0$			10	μA
h_{FE1}	DC Current Gain : ALL DEVICE	$V_{CE} = 2\text{V}, I_C = 5\text{mA}$	25			
h_{FE2}		$V_{CE} = 2\text{V}, I_C = 0.5\text{A}$	25			
h_{FE3}		$V_{CE} = 2\text{V}, I_C = 150\text{mA}$	40		250	
			40		160	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 500\text{mA}, I_E = 50\text{mA}$			0.5	V
$V_{BE(on)}$	Base-Emitter ON Voltage	$V_{CE} = 2\text{V}, I_C = 0.5\text{A}$			1	V

h_{FE} Classification

Classification	6	10	16
h_{FE3}	40 ~ 100	63 ~ 160	100 ~ 250

Typical Characteristics

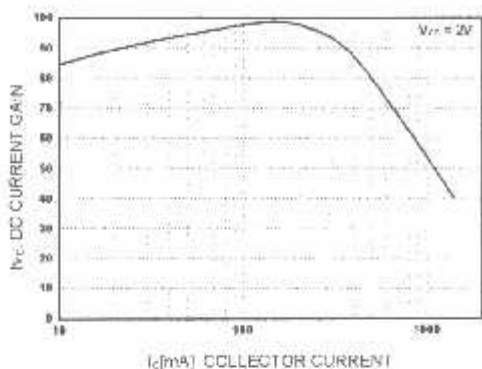


Figure 1. DC current Gain

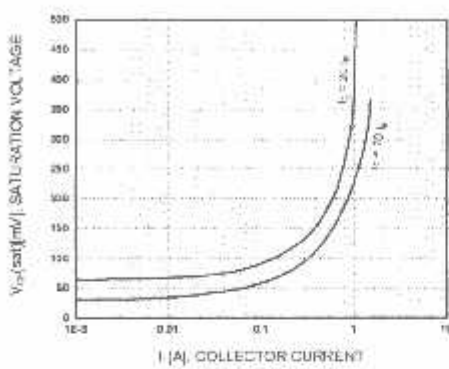


Figure 2. Collector-Emitter Saturation Voltage

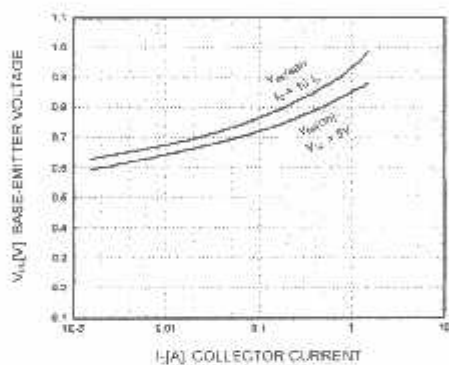


Figure 3. Base-Emitter Voltage

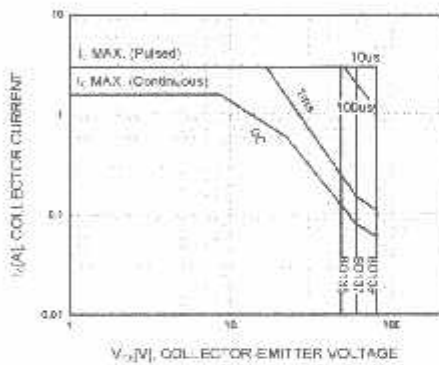


Figure 4. Safe Operating Area

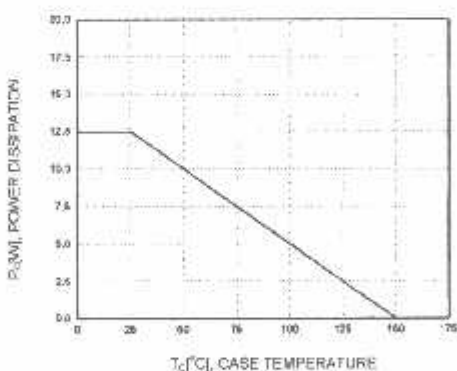
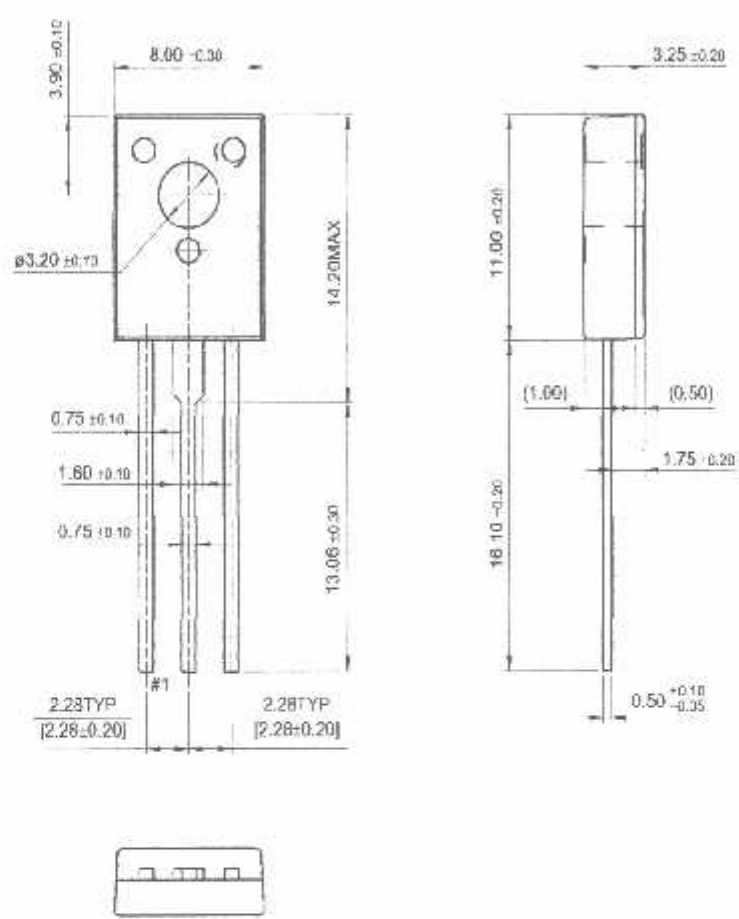


Figure 5. Power Derating

Package Demensions

BD135/137/139

TO-126



Dimensions in Millimeters

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE [™]	HiSeC [™]	SuperSOT [™] -8
Bottomless [™]	ISOPLANAR [™]	SyncFET [™]
CoolFET [™]	MICROWIRE [™]	TinyLogic [™]
CROSSVOLT [™]	POP [™]	UHC [™]
E ² CMOS [™]	PowerTrench [®]	VCX [™]
FACT [™]	QFET [™]	
FACT Quiet Series [™]	QS [™]	
FAST [®]	Quiet Series [™]	
FAST [™]	SuperSOT [™] -3	
GTO [™]	SuperSOT [™] -6	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR INTERNATIONAL.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

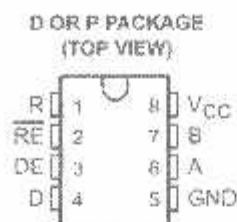
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

SN75176A DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1985

- Bidirectional Transceiver
- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and ITU Recommendation V.11
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ± 60 mA Max
- Thermal-Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedance . . . 12 k Ω Min
- Receiver Input Sensitivity . . . +200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From Single 5-V Supply
- Low Power Requirements



description

The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11.

The SN75176A combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 k Ω , an input sensitivity of +200 mV, and a typical input hysteresis of 50 mV.

The SN75176A can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

The SN75176A is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications on the basis of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655313 • DALLAS, TEXAS 75265

Copyright © 1985, Texas Instruments Incorporated

i75176A
FFERENTIAL BUS TRANSCEIVER

S100A — JUNE 1984 — REVISED MAY 1985

Function Tables

DRIVER

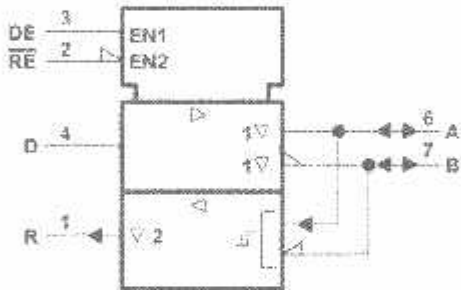
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A - B	ENABLE RE	OUTPUT R
$V_{ID} > 0.2\text{ V}$	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	?
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
Open	L	?

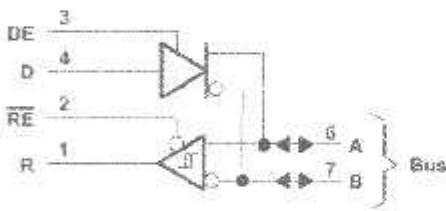
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol



This symbol is in accordance with ANSI/IEEE Std 91-1984
and IEC Publication 617-12.

logic diagram (positive logic)



SLLS100A - JUNE 1984 - REVISED MAY 1995

EQUIVALENT OF EACH INPUT

Driver Input: $R_{(eq)} = 3 \text{ k}\Omega \text{ NOM}$
 Enable inputs: $R_{(eq)} = 8 \text{ k}\Omega \text{ NOM}$
 $R_{(eq)} = \text{equivalent resistor}$

TYPICAL OF A AND B I/O PORTS

Input/Output Port

TYPICAL OF RECEIVER OUTPUT

Output

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage range at any bus terminal	-10 V to 15 V
Enable input voltage, V_i	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 105^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	484 mW	261 mW
P	1150 mW	8.3 mW/°C	704 mW	396 mW

175176A
DIFFERENTIAL BUS TRANSCEIVER

5100A JUNE 1984 REVISED MAY 1995

Recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		-7		12	V
High-level input voltage, V_{IH}	D, DE, and RE	2			V
Low-level input voltage, V_{IL}	D, DE, and RE			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			-60	mA
	Receiver			-400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	mA
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

SN75176A DIFFERENTIAL BUS TRANSCEIVER

SELS100A—JUNE 1984—REVISED MAY 1995

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -16 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{IH} = 2 \text{ V}$ $I_{OH} = -33 \text{ mA}$ $V_{IL} = 0.8 \text{ V}$		2.7		V
V_{OL} Low-level output voltage	$V_{IH} = 2 \text{ V}$ $I_{OH} = 33 \text{ mA}$ $V_{IL} = 0.8 \text{ V}$		1.1		V
$ V_{OD1} $ Differential output voltage	$I_O = 0$			$2V_{OD2}$	V
$ V_{OD2} $ Differential output voltage	$R_L = 100 \Omega$, See Figure 1	2	2.7		V
	$R_L = 54 \Omega$, See Figure 1	1.5	2.4		
$\Delta V_{OD} $ Change in magnitude of differential output voltage‡				±0.2	V
V_{OC} Common-mode output voltage§	$R_L = 54 \Omega$ or 100Ω , See Figure 1			3	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage‡				±0.2	V
I_O Output current	Output disabled, See Note 3	$V_O = 12 \text{ V}$		1	mA
		$V_O = -7 \text{ V}$		-0.8	
I_{IH} High-level input current†	$V_I = 2.4 \text{ V}$			20	μA
I_{IL} Low-level input current†	$V_I = 0.4 \text{ V}$			-400	μA
I_{OS} Short-circuit output current	$V_O = -7 \text{ V}$			-250	mA
	$V_O = V_{OC}$			250	
	$V_O = 12 \text{ V}$			500	
I_{CC} Supply current (total package)	No load	Outputs enabled	35	59	mA
		Outputs disabled	26	40	

† All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

§ In ANSI Standard EIA/TIA 422-B, V_{OC} , which is the average of the two output voltages with respect to GND, is called output offset voltage, V_{OS} .

NOTE 3: This applies for both power on and off; refer to ANSI Standard EIA/TIA 422-B for exact conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$ Differential-output delay time	$R_L = 60 \Omega$, See Figure 3		40	60	ns
$t_{r(OD)}$ Differential-output transition time			65	95	
t_{pZH} Output enable time to high level	$R_L = 110 \Omega$, See Figure 4		55	90	ns
t_{pZL} Output enable time to low level	$R_L = 110 \Omega$, See Figure 5		30	50	ns
t_{pHZ} Output disable time from high level	$R_L = 110 \Omega$, See Figure 4		85	130	ns
t_{pLZ} Output disable time from low level	$R_L = 110 \Omega$, See Figure 5		20	40	ns



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

75176A
DIFFERENTIAL BUS TRANSCEIVER

7500A - JUNE 1984 - REVISED MAY 1995

RECEIVER SECTION

critical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Positive-going input threshold voltage	$V_{IO} = 2.7\text{ V}$, $I_O = -0.4\text{ mA}$			0.2	V
Negative-going input threshold voltage	$V_{IO} = 0.5\text{ V}$, $I_O = 8\text{ mA}$	-0.24			V
Input hysteresis voltage ($V_{IT+} - V_{IT-}$)			50		mV
Enable clamp voltage	$I_I = -18\text{ mA}$			-1.5	V
High-level output voltage	$V_{IO} = 200\text{ mV}$, See Figure 2	$I_{OH} = -400\text{ }\mu\text{A}$	2.7		V
Low-level output voltage	$V_{IO} = -200\text{ mV}$, See Figure 2	$I_{OL} = 8\text{ }\mu\text{A}$		0.45	V
High-impedance-state output current	$V_{IO} = 0.4\text{ V to }2.4\text{ V}$			± 20	μA
Line input current	Other input = 0 V, See Note 3	$V_I = 12\text{ V}$ $V_I = -7\text{ V}$		1 -0.8	mA
High-level enable input current	$V_{IH} = 2.7\text{ V}$			20	μA
Low-level enable input current	$V_{IL} = 0.4\text{ V}$			-100	μA
Input resistance		12			k Ω
Short-circuit output current		-15		-85	mA
Supply current (total package)	No load				
		Outputs enabled	35	60	mA
		Outputs disabled	25	40	mA

† Typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.
† The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
† E 3† This applies for both power on and power off. Refer to ANSI Standard EIA/TIA-422-B for exact conditions.

switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay time, low-to-high-level output	$V_{IO} = -1.5\text{ V to }1.5\text{ V}$ See Figure 6		21	35	ns
Propagation delay time, high-to-low-level output			23	35	ns
Output enable time to high level†	See Figure 7		10	30	ns
Output enable time to low level†			12	30	ns
Output disable time from high level†	See Figure 7		20	35	ns
Output disable time from low level†			17	25	ns

PARAMETER MEASUREMENT INFORMATION

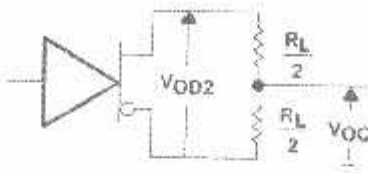


Figure 1. Driver V_{OH} and V_{OL}

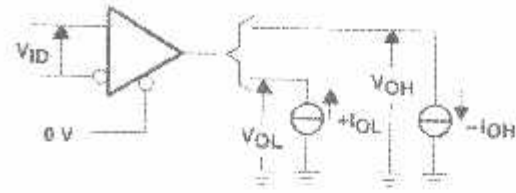
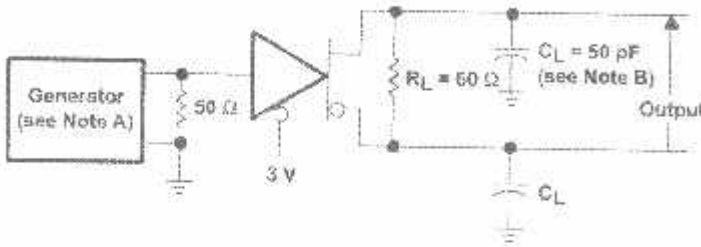
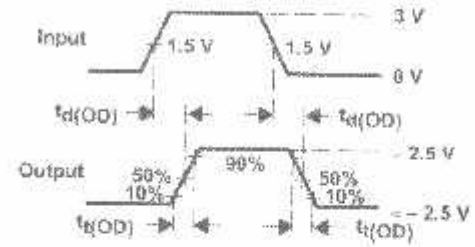


Figure 2. Receiver V_{OH} and V_{OL}



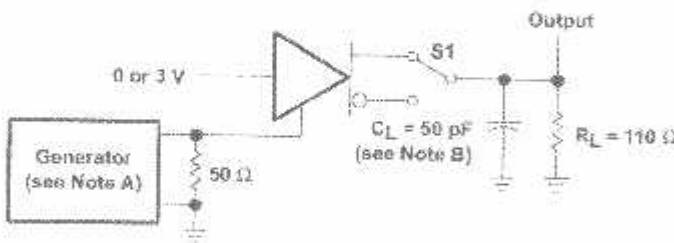
TEST CIRCUIT



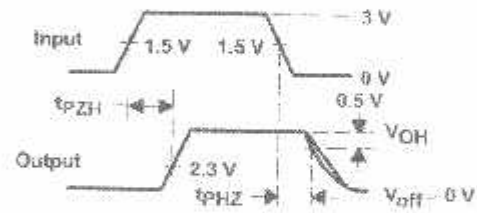
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



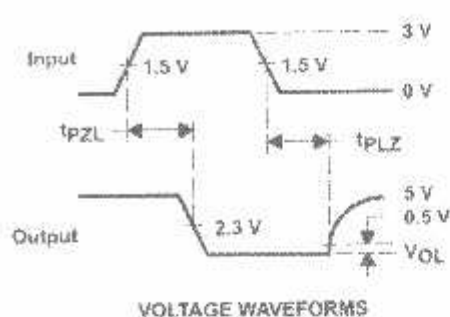
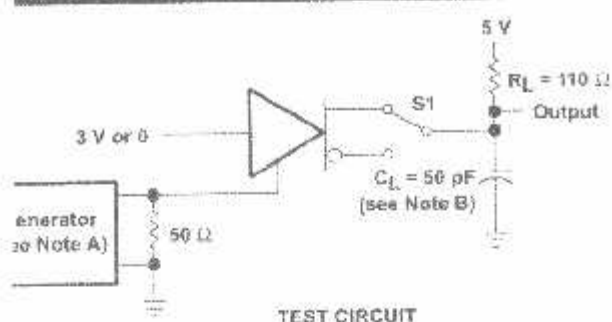
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

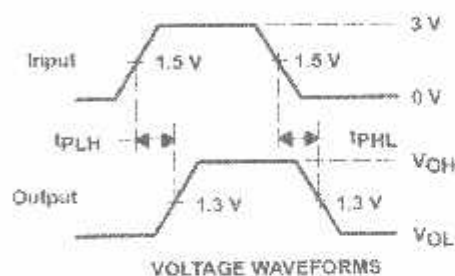
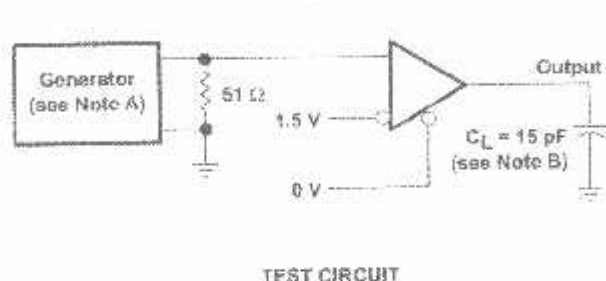
5176A DIFFERENTIAL BUS TRANSCEIVER

00A - JUNE 1984 - REVISED MAY 1995



- TEST: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms



- TEST: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.
B. C_L includes probe and jig capacitance.

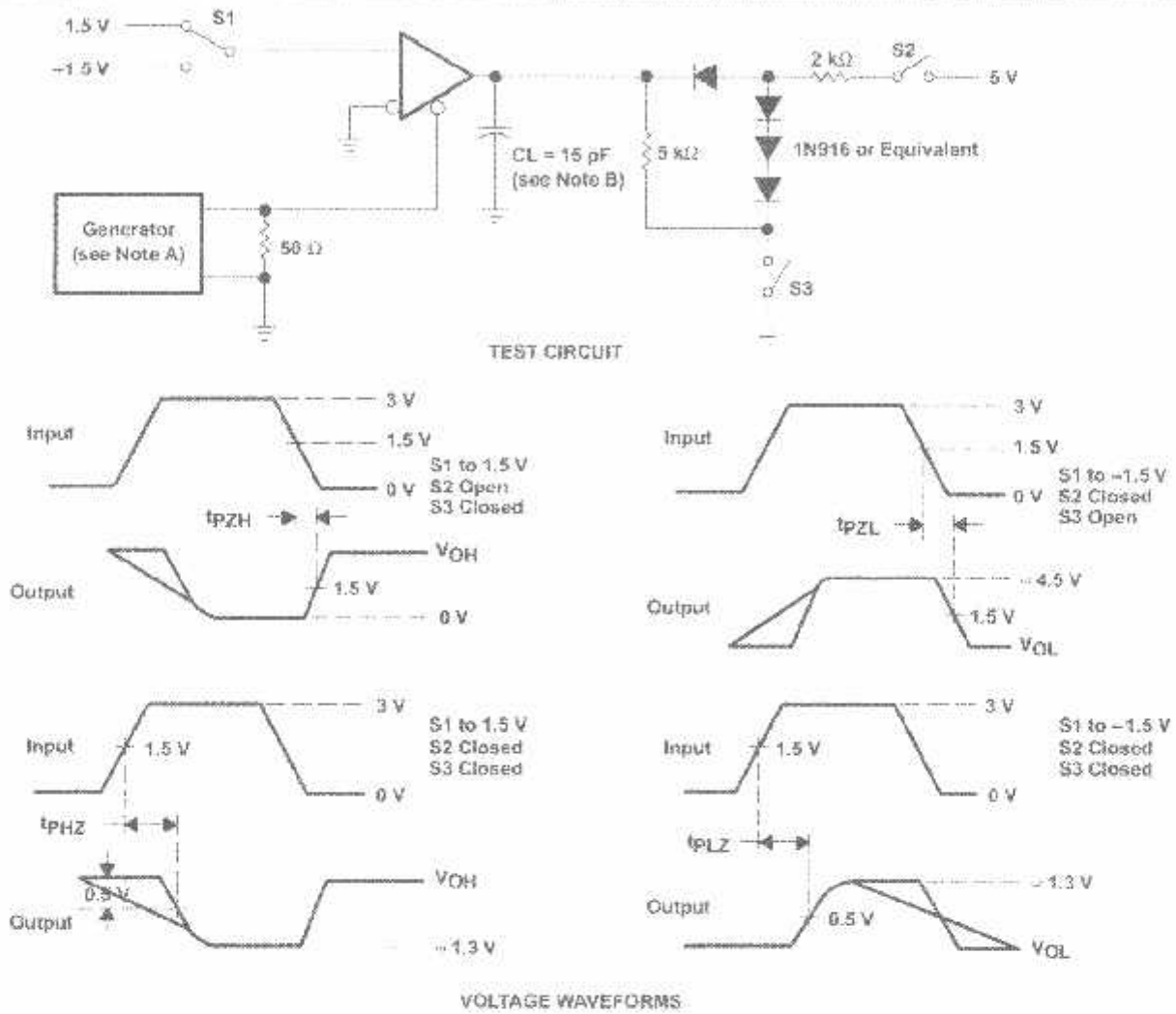
Figure 6. Receiver Test Circuit and Voltage Waveforms



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN75176A DIFFERENTIAL BUS TRANSCEIVER

SLLS150A – JUNE 1994 – REVISED MAY 1995



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r < 0.5$ ns, $t_f < 0.5$ ns, $Z_0 = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

175176A
DIFFERENTIAL BUS TRANSCEIVER

1100A - JUNE 1984 - REVISED MAY 1995

TYPICAL CHARACTERISTICS

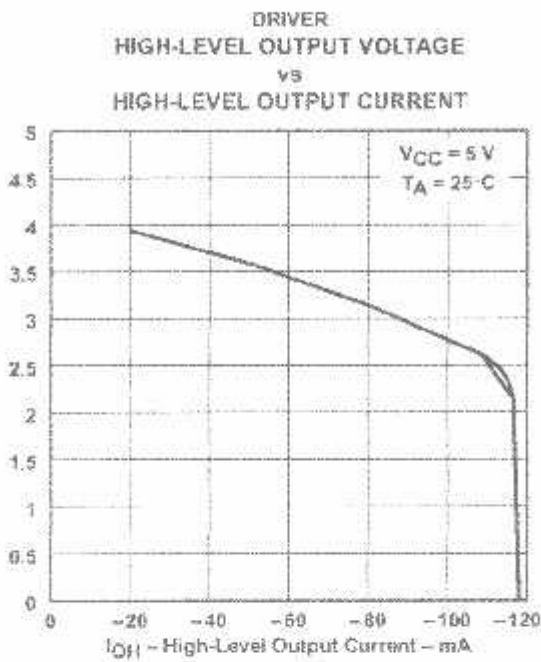


Figure 8

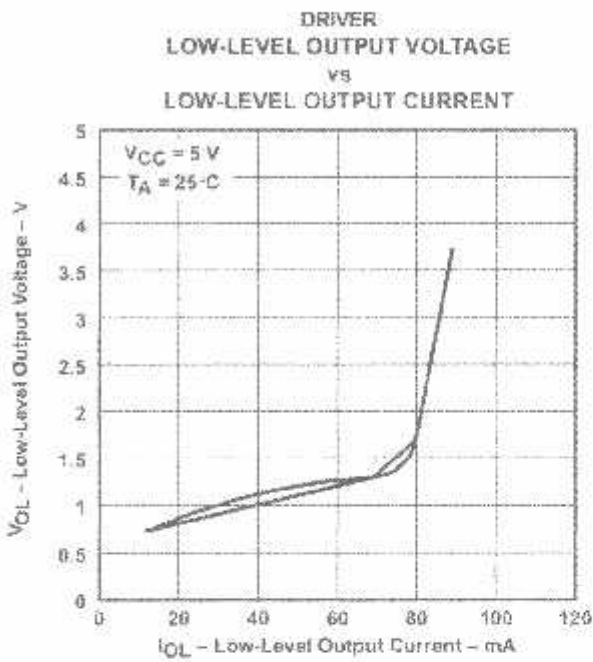


Figure 9

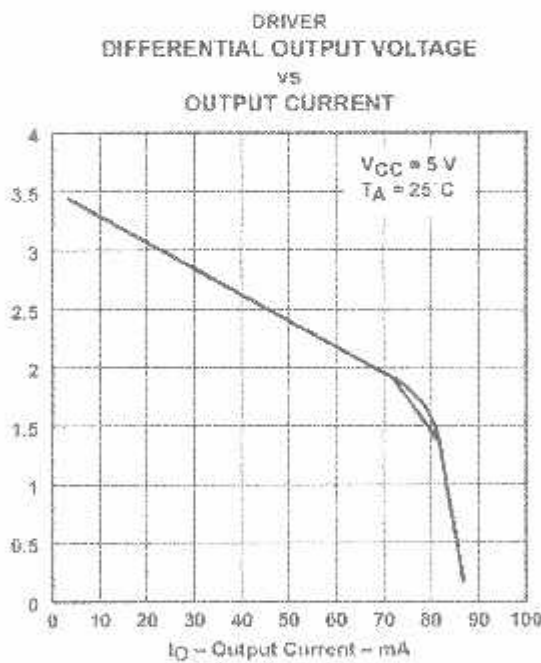


Figure 10

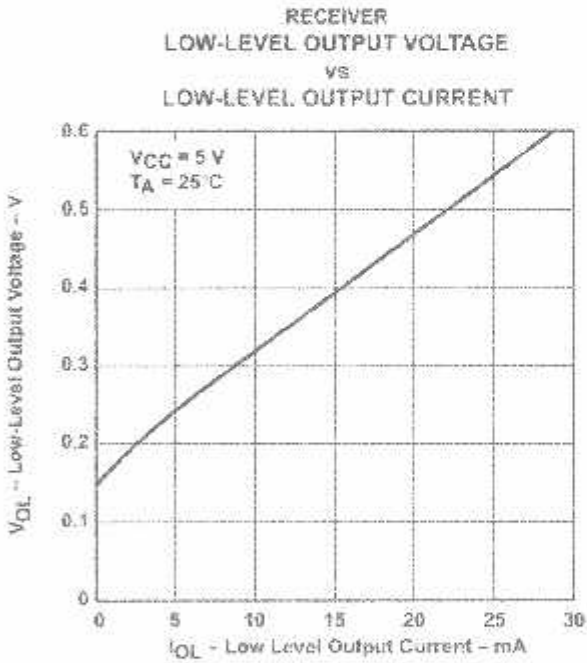


Figure 11

TYPICAL CHARACTERISTICS

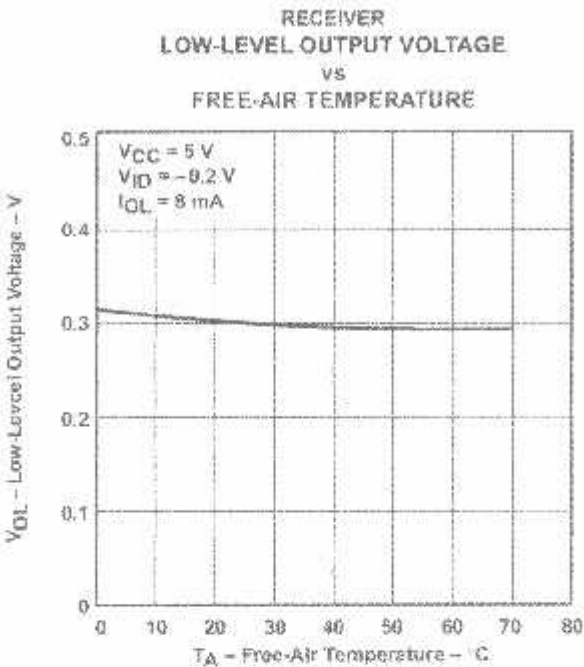


Figure 12

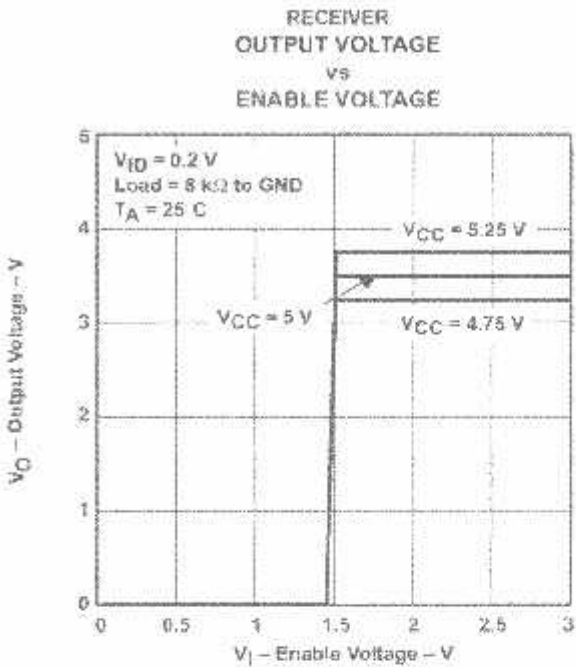


Figure 13

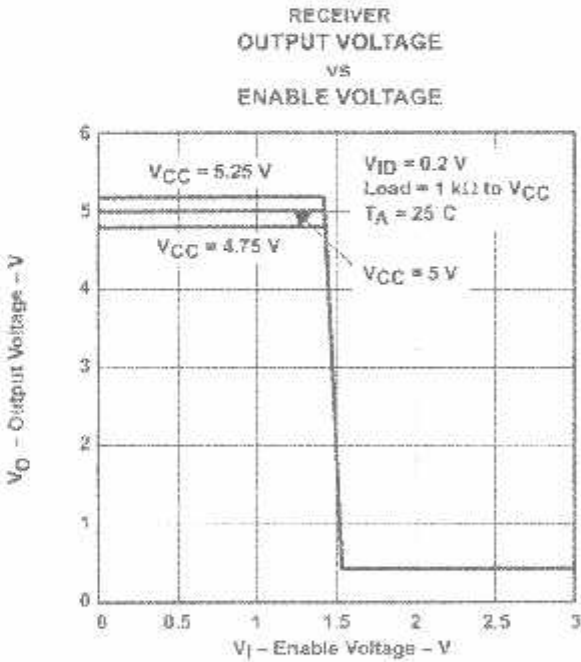
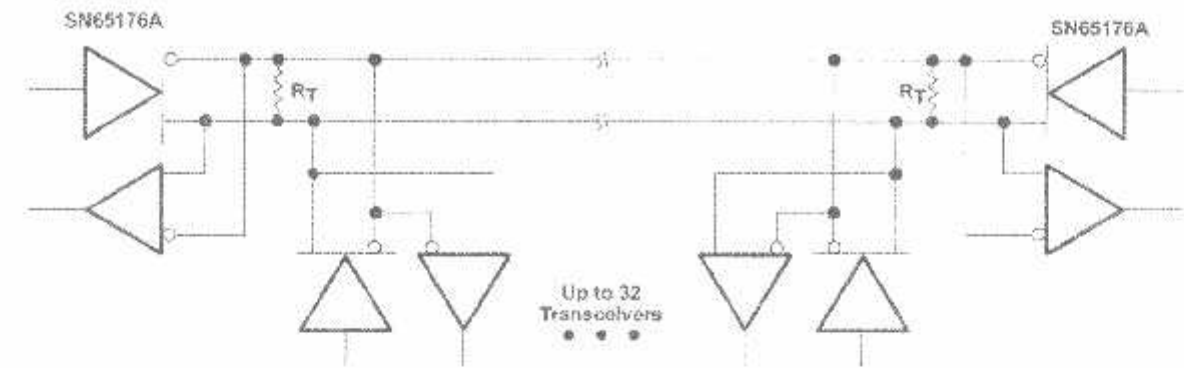


Figure 14

SN65176A
DIFFERENTIAL BUS TRANSCEIVER

SN100A - JUNE 1984 - REVISED MAY 1993

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 15. Typical Application Circuit

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.



Data Sheet

Light dependent resistors

NORP12 RS stock number 651-507
NSL19-M51 RS stock number 596-141

Two cadmium sulphide (cdS) photoconductive cells with spectral responses similar to that of the human eye. The cell resistance falls with increasing light intensity. Applications include smoke detection, automatic lighting control, batch counting and burglar alarm systems.

Guide to source illuminations

Light source	Illumination (Lux)
Moonlight	0.1
60W bulb at 1m	50
1W MES bulb at 0.1m	100
Fluorescent lighting	500
Bright sunlight	30,000

Circuit symbol



Light memory characteristics

Light dependent resistors have a particular property in that they remember the lighting conditions in which they have been stored. This memory effect can be minimised by storing the LDRs in light prior to use. Light storage reduces equilibrium time to reach steady resistance values.

NORP12 (RS stock no. 651-507)

Absolute maximum ratings

Voltage - ac or dc peak	320V
Current	75mA
Power dissipation at 30°C	250mW
Operating temperature range	-60°C to +75°C

Electrical characteristics

$T_A = 25^\circ\text{C}$, 2854°K tungsten light source

Parameter	Conditions	Min.	Typ.	Max.	Units
Cell resistance	1000 lux	-	400	-	Ω
	10 lux	-	9	-	k Ω
Dark resistance		1.0	-	-	M Ω
Dark capacitance	-	-	3.5	-	pF
Rise time 1	1000 lux	-	2.8	-	ms
	10 lux	-	18	-	ms
Fall time 2	1000 lux	-	48	-	ms
	10 lux	-	120	-	ms

1. Dark to 100% R_L

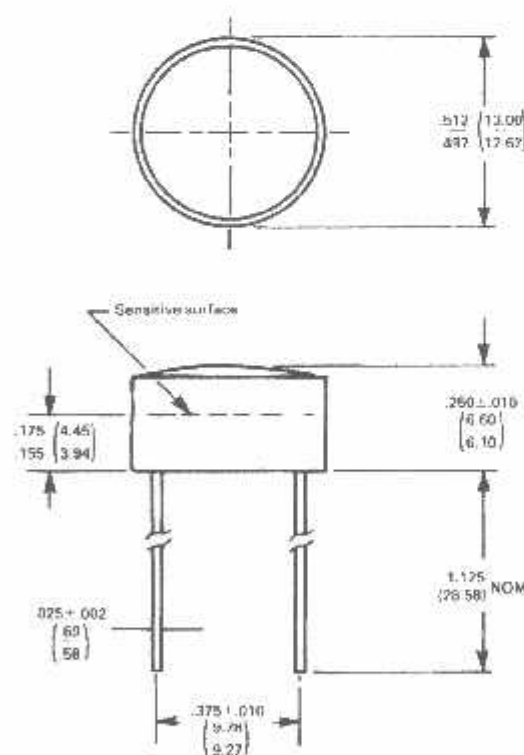
2. To $10 \times R_L$

R_L = photocell resistance under given illumination.

Features

- Wide spectral response
- Low cost
- Wide ambient temperature range.

Dimensions



Units in inches (millimetres)

Figure 1 Power dissipation derating

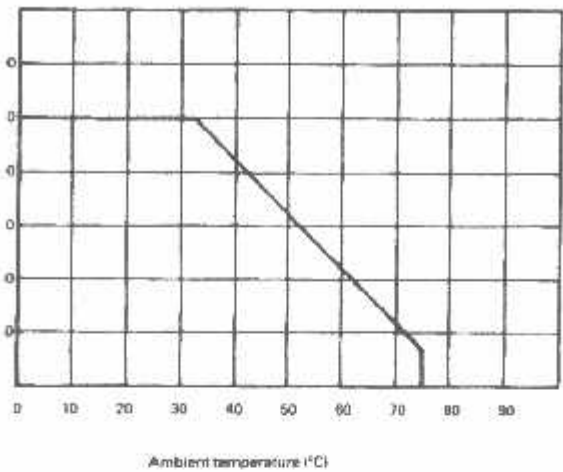
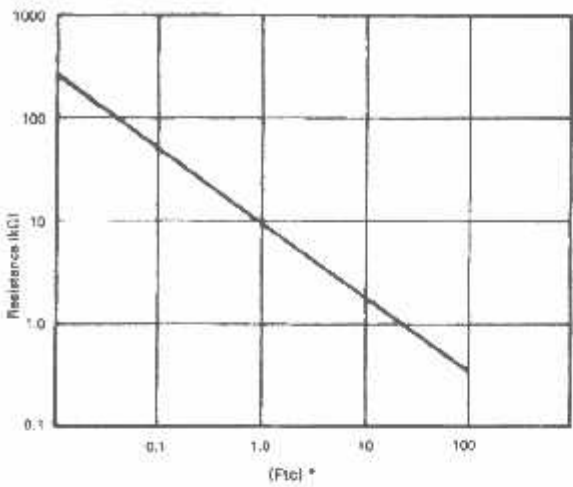
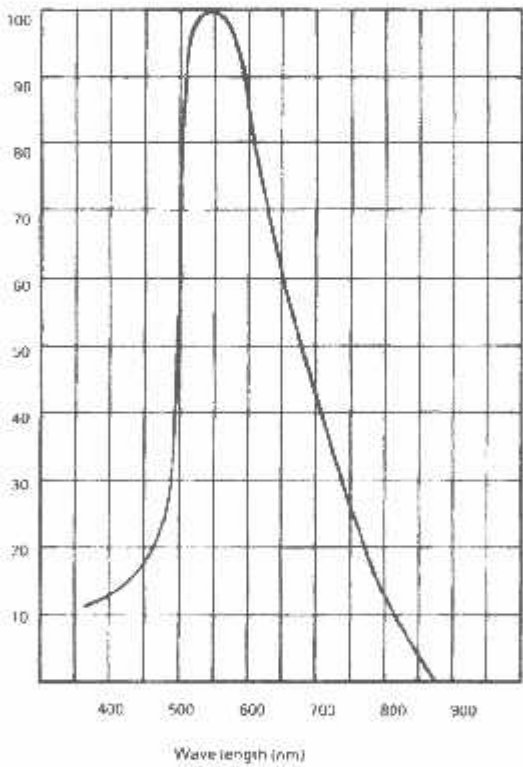


Figure 3 Resistance as a function of illumination



*1Fic=10.764 lumens

Figure 2 Spectral response



Absolute maximum ratings

Voltage, ac or dc peak _____ 100V
Current _____ 5mA
Power dissipation at 25°C _____ 50mW*
Operating temperature range _____ 25°C - 75°C

*Derate linearly from 50mW at 25°C to 0W at 75°C.

Electrical characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Cell resistance	10 lux	20	-	100	kΩ
	100 lux	-	5	-	kΩ
Dark resistance	10 lux after 10 sec	20			MΩ
Spectral response	-		550	-	nm
Rise time	10Hz	-	45		ms
Fall time	10Hz		55	-	ms

Figure 4 Resistance as a function illumination

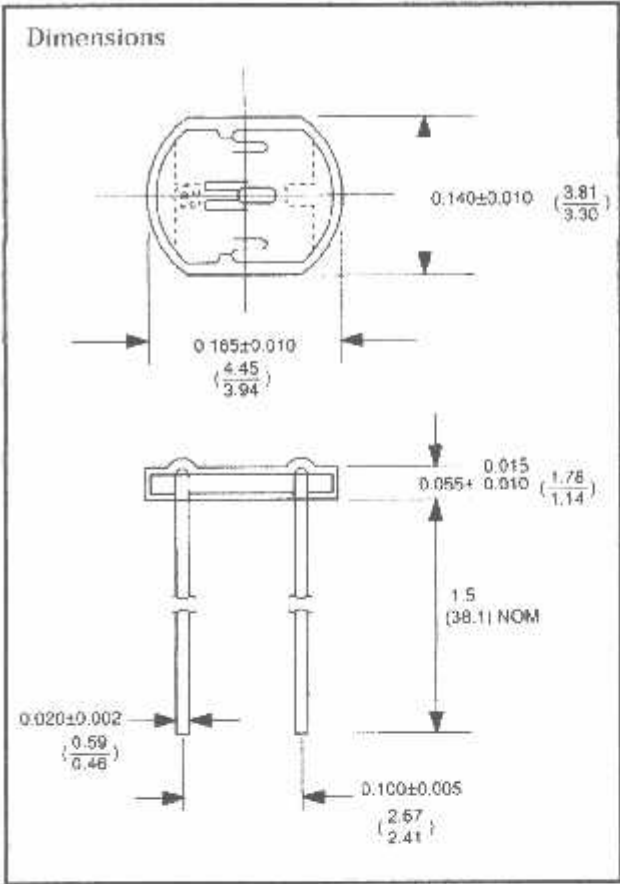
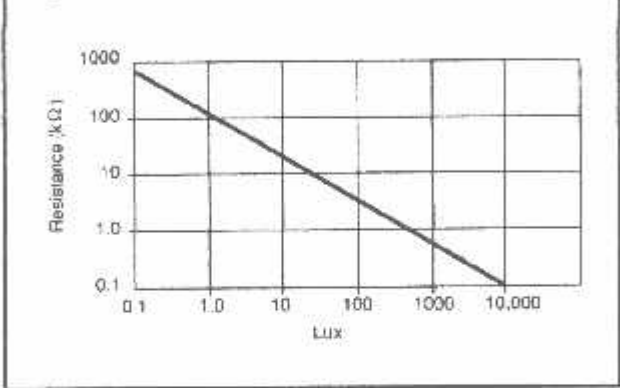
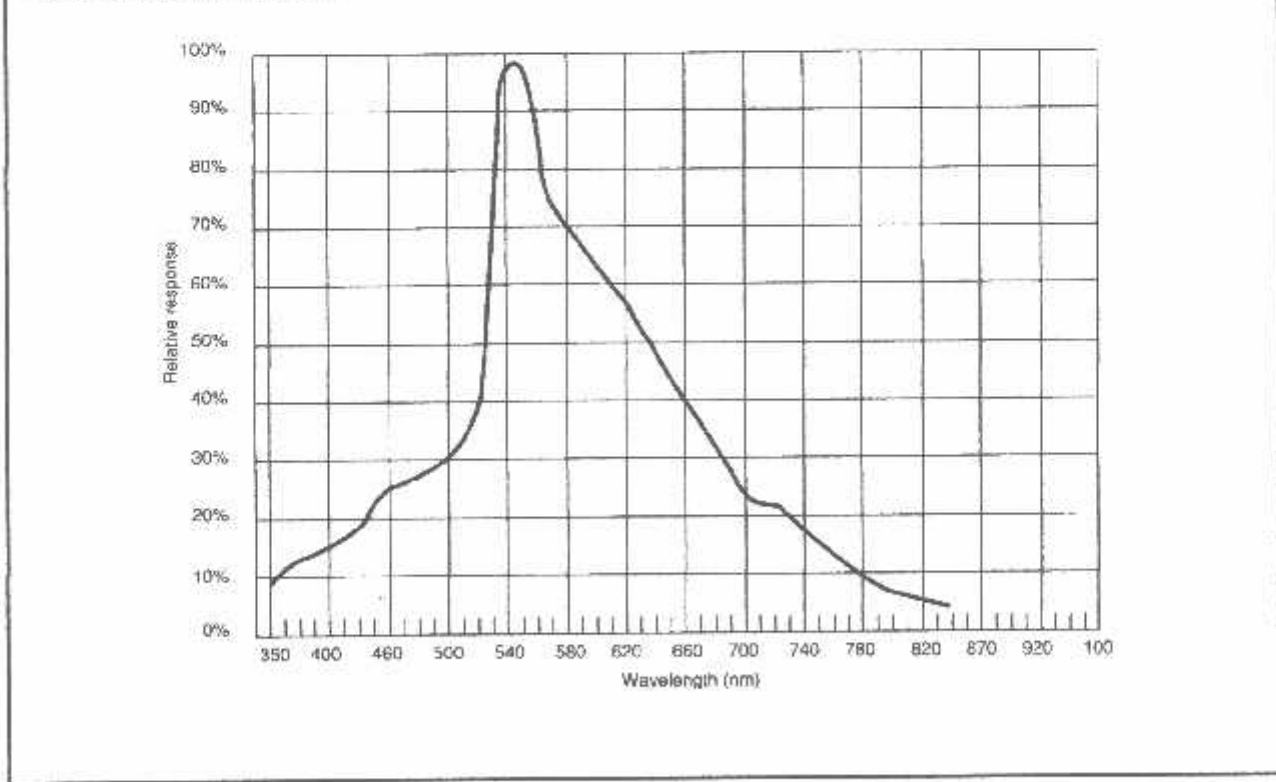
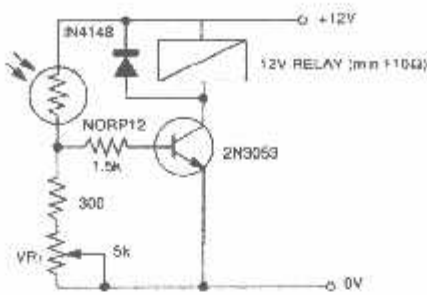


Figure 5 Spectral response



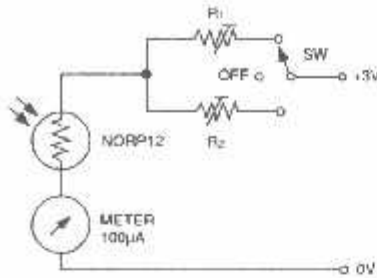
Typical application circuits

Figure 6 Sensitive light operated relay



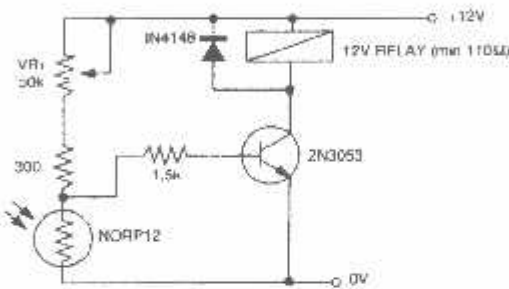
Relay energised when light level increases above the level set by VR₁

Figure 9 Logarithmic law photographic light meter



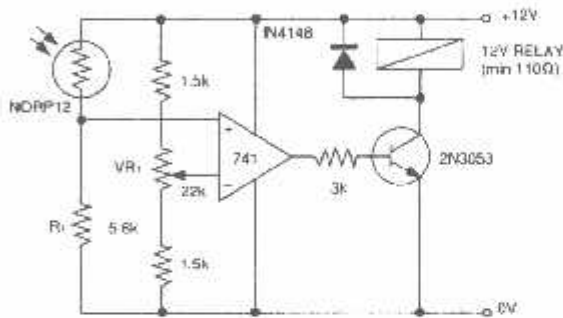
Typical value R₁ = 100kΩ
R₂ = 200kΩ preset to give two overlapping ranges.
(Calibration should be made against an accurate meter.)

Figure 7 Light interruption detector



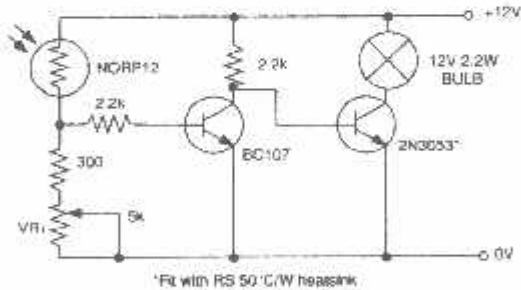
As Figure 6 relay energised when light level drops below the level set by VR₁

Figure 10 Extremely sensitive light operated relay



(Relay energised when light exceeds preset level.)
Incorporates a balancing bridge and op-amp. R₁ and NORP12 may be interchanged for the reverse function.

Figure 8 Automatic light circuit



Adjust turn-on point with VR₁

All information provided in RS technical literature is believed to be accurate and reliable; however, RS Components assumes no responsibility for inaccuracies, omissions, or for the use of this information, and all use of such information shall be entirely at the user's own risk. Responsibility is assumed by RS Components for any infringements of patents or other rights of third parties which may result from its use. Solutions shown in RS Components technical literature are subject to change without notice.

ADC0802, ADC0803 ADC0804

8-Bit, Microprocessor-
Compatible, A/D Converters

July 1997

Features

- 80C48 and 80C80/85 Bus Compatible - No Interfacing Logic Required
- Conversion Time < 100 μ s
- Easy Interface to Most Microprocessors
- Will Operate in a "Stand Alone" Mode
- Differential Analog Voltage Inputs
- Works with Bandgap Voltage References
- TTL Compatible Inputs and Outputs
- On-Chip Clock Generator
- 0V to 5V Analog Voltage Input Range (Single +5V Supply)
- No Zero-Adjust Required

Description

The ADC0802 family are CMOS 8-Bit, successive-approximation A/D converters which use a modified potentiometric ladder and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, and hence no interfacing logic is required.

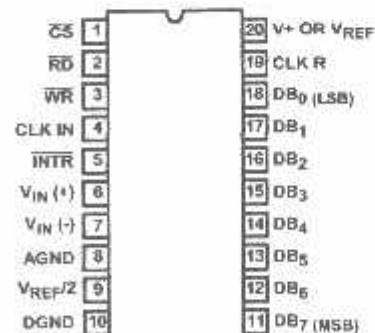
The differential analog voltage input has good common-mode-rejection and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Ordering Information

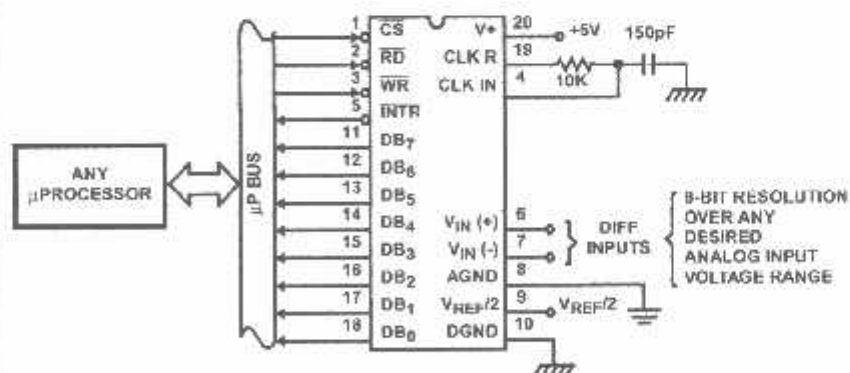
PART NUMBER	ERROR	EXTERNAL CONDITIONS	TEMP. RANGE (°C)	PACKAGE	PKG. NO
ADC0802LCN	$\pm 1/2$ LSB	$V_{REF}/2 = 2.500V_{DC}$ (No Adjustments)	0 to 70	20 Ld PDIP	E20.3
ADC0802LCD	$\pm 3/4$ LSB		-40 to 85	20 Ld Cerdip	F20.3
ADC0802LD	± 1 LSB		-55 to 125	20 Ld Cerdip	F20.3
ADC0803LCN	$\pm 1/2$ LSB	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	0 to 70	20 Ld PDIP	E20.3
ADC0803LCD	$\pm 3/4$ LSB		-40 to 85	20 Ld Cerdip	F20.3
ADC0803LCWM	± 1 LSB		-40 to 85	20 Ld SOIC	M20.3
ADC0803LD	± 1 LSB		-55 to 125	20 Ld Cerdip	F20.3
ADC0804LCN	± 1 LSB	$V_{REF}/2 = 2.500V_{DC}$ (No Adjustments)	0 to 70	20 Ld PDIP	E20.3
ADC0804LCD	± 1 LSB		-40 to 85	20 Ld Cerdip	F20.3
ADC0804LCWM	± 1 LSB		-40 to 85	20 Ld SOIC	M20.3

Pinout

ADC0802, ADC0803, ADC0804
(PDIP, Cerdip)
TOP VIEW



Typical Application Schematic

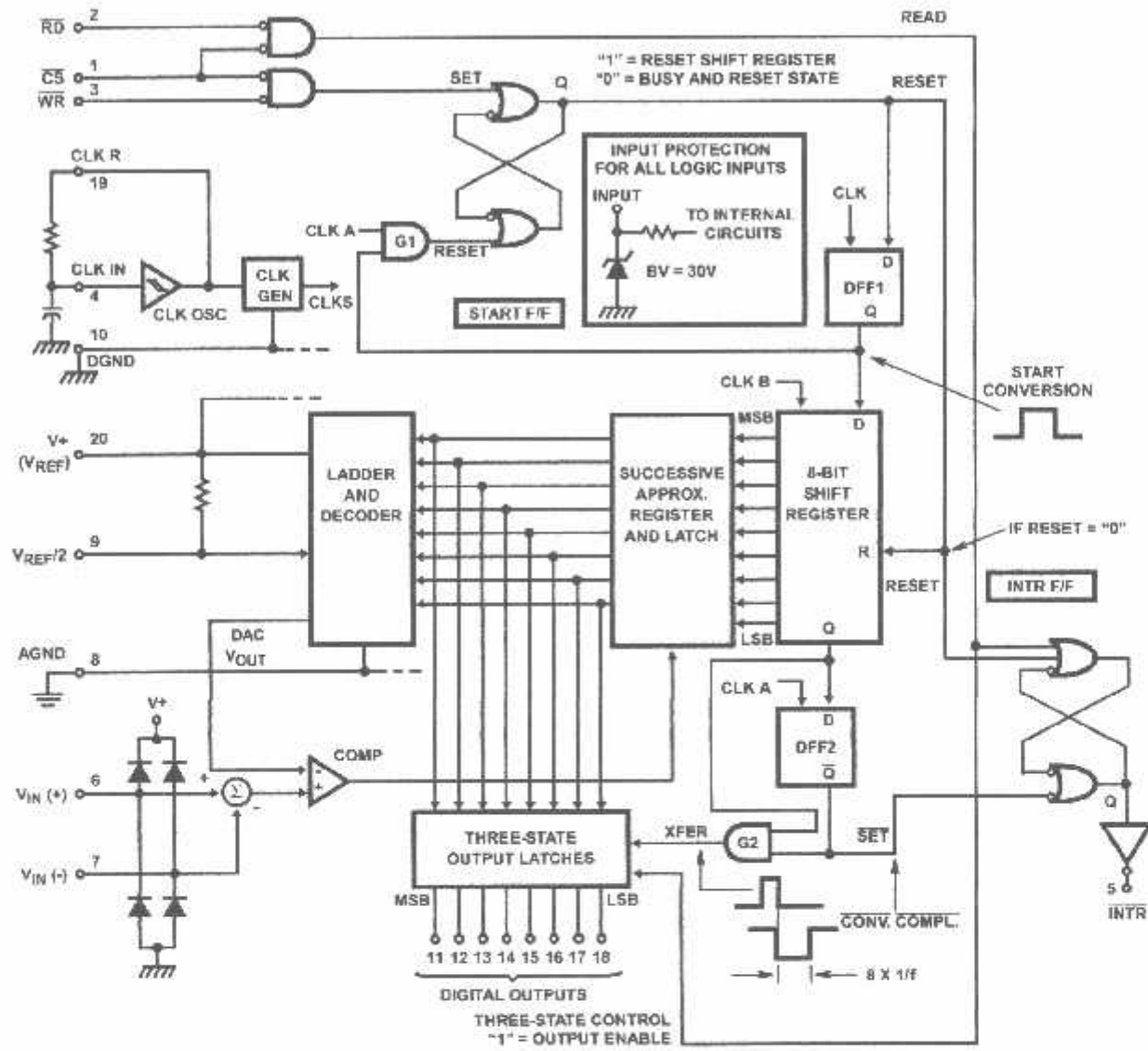


NOTE: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Copyright © Harris Corporation 1997

File Number 3094.1

Functional Diagram



ADC0802, ADC0803, ADC0804

Absolute Maximum Ratings

Supply Voltage	6.5V
Voltage at Any Input	-0.3V to (V ⁺ + 0.3V)

Operating Conditions

Temperature Range	
ADC0802/03LD	-55°C to 125°C
ADC0802/03/04LCD	-40°C to 85°C
ADC0802/03/04LCN	-20°C to 70°C
ADC0803/04LCWM	-40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	125	N/A
CERDIP Package	80	20
SOIC Package	120	N/A
Maximum Junction Temperature		
Hermetic Package		175°C
Plastic Package		150°C
Maximum Storage Temperature Range		-65°C to 150°C
Maximum Lead Temperature (Soldering, 10s)		300°C (SOIC: Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications (Notes 1, 7)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CONVERTER SPECIFICATIONS V ⁺ = 5V, T _A = 25°C and f _{CLK} = 640kHz, Unless Otherwise Specified					
Total Unadjusted Error					
ADC0802	V _{REF/2} = 2.500V	-	-	±1/2	LSB
ADC0803	V _{REF/2} Adjusted for Correct Full Scale Reading	-	-	±1/2	LSB
ADC0804	V _{REF/2} = 2.500V	-	-	±1	LSB
V _{REF/2} Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V ⁺) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	±1/16	±1/8	LSB
Power Supply Sensitivity	V ⁺ = 5V ±10% Over Allowed Input Voltage Range	-	±1/16	±1/8	LSB
CONVERTER SPECIFICATIONS V ⁺ = 5V, 0°C to 70°C and f _{CLK} = 640kHz, Unless Otherwise Specified					
Total Unadjusted Error					
ADC0802	V _{REF/2} = 2.500V	-	-	±1/2	LSB
ADC0803	V _{REF/2} Adjusted for Correct Full Scale Reading	-	-	±1/2	LSB
ADC0804	V _{REF/2} = 2.500V	-	-	±1	LSB
V _{REF/2} Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V ⁺) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	±1/8	±1/4	LSB
Power Supply Sensitivity	V ⁺ = 5V ±10% Over Allowed Input Voltage Range	-	±1/16	±1/8	LSB
CONVERTER SPECIFICATIONS V ⁺ = 5V, -25°C to 85°C and f _{CLK} = 640kHz, Unless Otherwise Specified					
Total Unadjusted Error					
ADC0802	V _{REF/2} = 2.500V	-	-	±5/4	LSB
ADC0803	V _{REF/2} Adjusted for Correct Full Scale Reading	-	-	±3/4	LSB
ADC0804	V _{REF/2} = 2.500V	-	-	±1	LSB
V _{REF/2} Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V ⁺) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	±1/8	±1/4	LSB
Power Supply Sensitivity	V ⁺ = 5V ±10% Over Allowed Input Voltage Range	-	±1/16	±1/8	LSB

ADC0802, ADC0803, ADC0804

Electrical Specifications (Notes 1, 7) (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CONVERTER SPECIFICATIONS $V_+ = 5V$, $-55^{\circ}C$ to $125^{\circ}C$ and $f_{CLK} = 640kHz$, Unless Otherwise Specified					
Total Unadjusted Error					
ADC0802	$V_{REF}/2 = 2.500V$	-	-	± 1	LSB
ADC0803	$V_{REF}/2$ Adjusted for Correct Full Scale Reading	-	-	± 1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	k Ω
Analog Input Voltage Range	(Note 2)	GND-0.05	-	$(V_+) + 0.05$	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm 1/8$	$\pm 1/4$	LSB
Power Supply Sensitivity	$V_+ = 5V \pm 10\%$ Over Allowed Input Voltage Range	-	$\pm 1/8$	$\pm 1/4$	LSB
AC TIMING SPECIFICATIONS $V_+ = 5V$, and $T_A = 25^{\circ}C$, Unless Otherwise Specified					
Clock Frequency: f_{CLK}	$V_+ = 6V$ (Note 3)	100	640	1280	kHz
	$V_+ = 5V$	100	640	800	kHz
Clock Periods per Conversion (Note 4): t_{CONV}		62	-	73	Clocks/Conv
Conversion Rate In Free-Running Mode, CR	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS} = 0V$, $f_{CLK} = 640kHz$	-	-	8888	Conv/s
Width of $\overline{WR}$ Input (Start Pulse Width): $t_{W(WR)}$	$\overline{CS} = 0V$ (Note 5)	100	-	-	ns
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid): t_{ACC}	$C_L = 100pF$ (Use Bus Driver IC for Larger C_L)	-	135	200	ns
Three-State Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State): t_{H-Z} , t_{OH}	$C_L = 10pF$, $R_L = 10K$ (See Three-State Test Circuits)	-	125	250	ns
Delay from Falling Edge of $\overline{WR}$ to Reset of $\overline{INTR}$: t_{WZ} , t_{RZ}		-	300	450	ns
Input Capacitance of Logic Control Inputs, C_{IN}		-	5	-	pF
Three-State Output Capacitance (Data Buffers), C_{OUT}		-	5	-	pF
DC DIGITAL LEVELS AND DC SPECIFICATIONS $V_+ = 5V$, and T_{MIN} to T_{MAX} , Unless Otherwise Specified					
CONTROL INPUTS (Note 6)					
Logic "1" Input Voltage (Except Pin 4 CLK IN): V_{INH}	$V_+ = 5.25V$	2.0	-	V_+	V
Logic "0" Input Voltage (Except Pin 4 CLK IN): V_{INL}	$V_+ = 4.75V$	-	-	0.8	V
CLK IN (Pin 4) Positive Going Threshold Voltage: V_{+CLK}		2.7	3.1	3.5	V
CLK IN (Pin 4) Negative Going Threshold Voltage: V_{-CLK}		1.5	1.8	2.1	V
CLK IN (Pin 4) Hysteresis: V_H		0.6	1.3	2.0	V
Logic "1" Input Current (All Inputs): I_{INH}	$V_{IN} = 5V$	-	0.005	1	μA
Logic "0" Input Current (All Inputs): I_{INLO}	$V_{IN} = 0V$	-1	-0.005	-	μA
Supply Current (Includes Ladder Current), I_+	$f_{CLK} = 640kHz$, $I_A = 25^{\circ}C$ and $\overline{CS} = HI$	-	1.3	2.5	mA
DATA OUTPUTS AND INTR					
Logic "0" Output Voltage: V_{OL}	$I_O = 1.6mA$, $V_+ = 4.75V$	-	-	0.4	V

ADC0802, ADC0803, ADC0804

Electrical Specifications (Notes 1, 7) (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Logic '1' Output Voltage, V_{OH}	$I_O = -360\mu A$, $V^+ = 4.75V$	2.4	-	-	V
Three-State Disabled Output Leakage (All Data Buffers), I_{IO}	$V_{OUT} = 0V$	-3	-	-	μA
	$V_{OUT} = 5V$	-	-	3	μA
Output Short Circuit Current, I_{SOURCE}	V_{OUT} Short to Gnd $T_A = 25^\circ C$	4.5	6	-	mA
Output Short Circuit Current, I_{SINK}	V_{OUT} Short to V^+ $T_A = 25^\circ C$	9.0	16	-	mA

NOTES:

1. All voltages are measured with respect to GND, unless otherwise specified. The separate AGND point should always be wired to the DGND, being careful to avoid ground loops.
2. For $V_{IN(-)} \geq V_{IN(-)}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V^+ supply. Be careful, during testing at low V^+ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct - especially at elevated temperatures, and cause errors for analog inputs near full scale. As long as the analog V_{IN} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance and loading.
3. With $V^+ = 6V$, the digital logic interfaces are no longer TTL compatible.
4. With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.
5. The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input so that timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see Timing Diagrams).
6. CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.
7. None of these A/Ds requires a zero-adjust. However, if an all zero code is desired for an analog input other than 0V, or if a narrow full scale span exists (for example: 0.5V to 4V full scale) the $V_{IN(-)}$ input can be adjusted to achieve this. See the Zero Error description in this data sheet.

Timing Waveforms

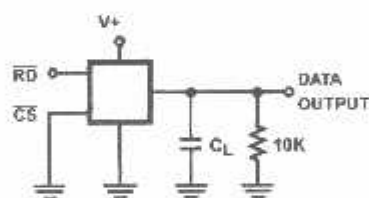


FIGURE 1A. t_{1H}

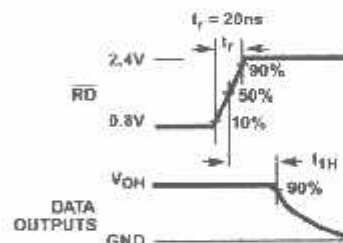


FIGURE 1B. t_{1H} , $C_L = 10pF$

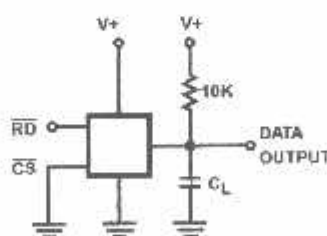


FIGURE 1C. t_{0H}

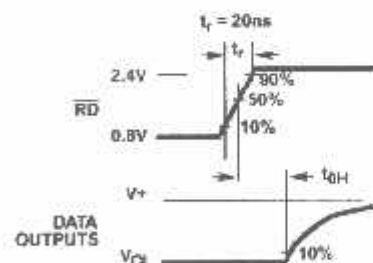


FIGURE 1D. t_{0H} , $C_L = 10pF$

FIGURE 1. THREE-STATE CIRCUITS AND WAVEFORMS

Typical Performance Curves

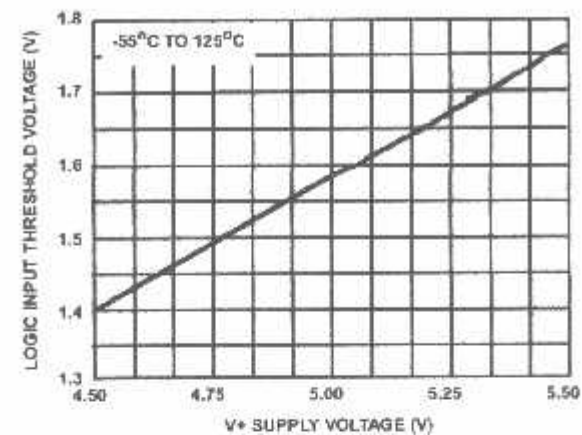


FIGURE 2. LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

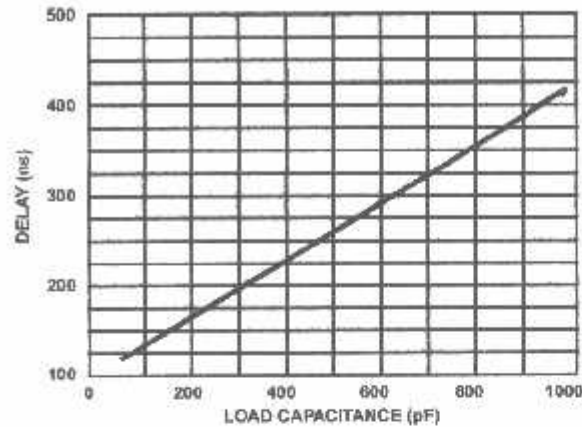


FIGURE 3. DELAY FROM FALLING EDGE OF $\overline{RD}$ TO OUTPUT DATA VALID vs LOAD CAPACITANCE

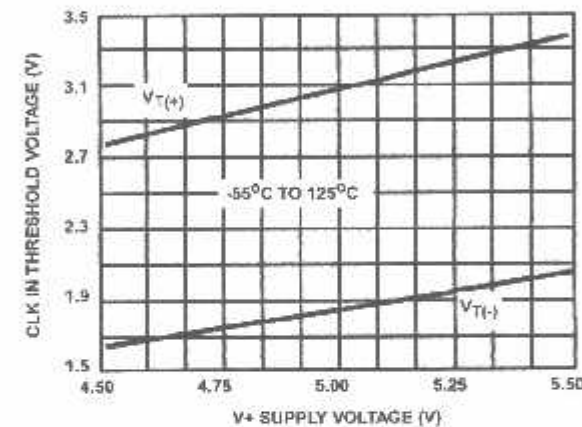


FIGURE 4. CLK IN SCHMITT TRIP LEVELS vs SUPPLY VOLTAGE

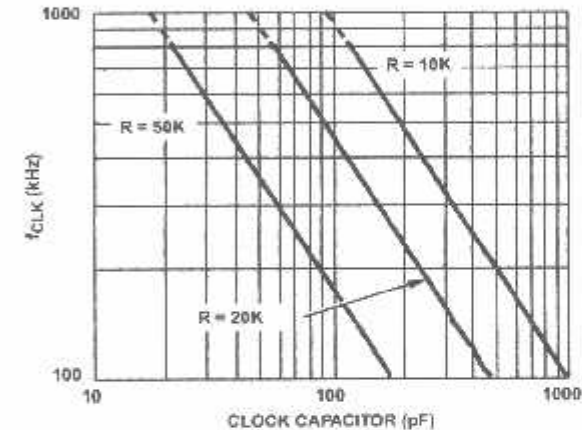


FIGURE 5. f_{CLK} vs CLOCK CAPACITOR

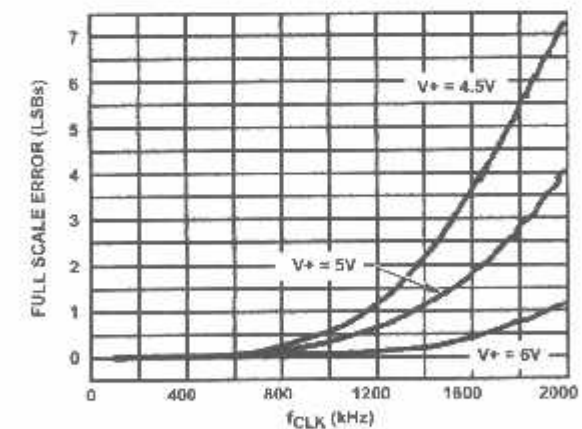


FIGURE 6. FULL SCALE ERROR vs f_{CLK}

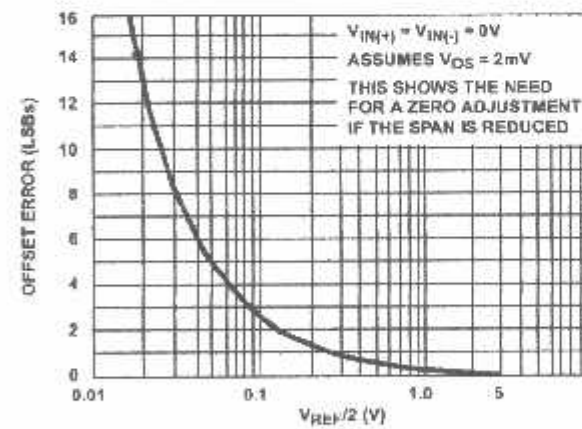


FIGURE 7. EFFECT OF UNADJUSTED OFFSET ERROR

Typical Performance Curves (Continued)

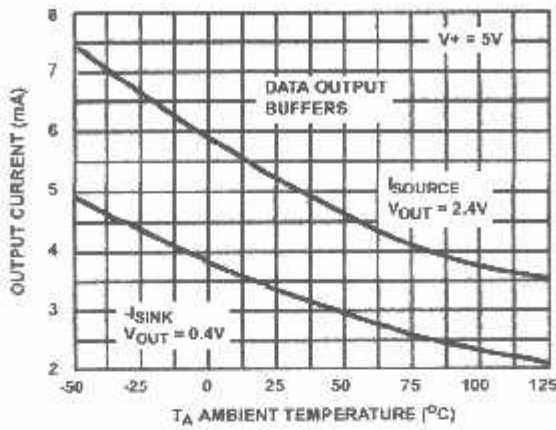


FIGURE 8. OUTPUT CURRENT vs TEMPERATURE

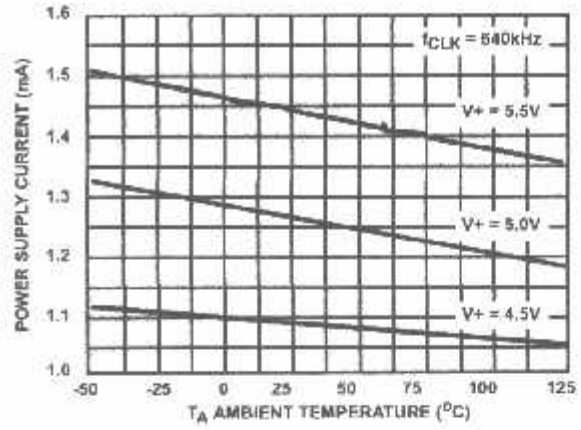


FIGURE 9. POWER SUPPLY CURRENT vs TEMPERATURE

Timing Diagrams

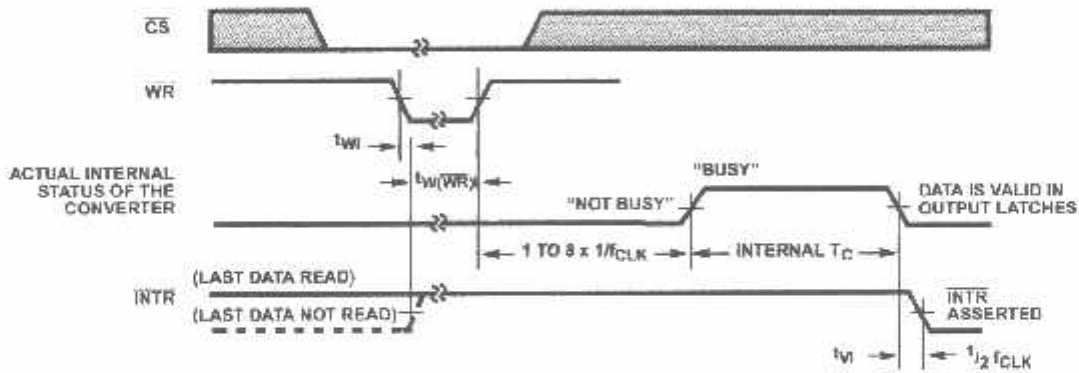


FIGURE 10A. START CONVERSION

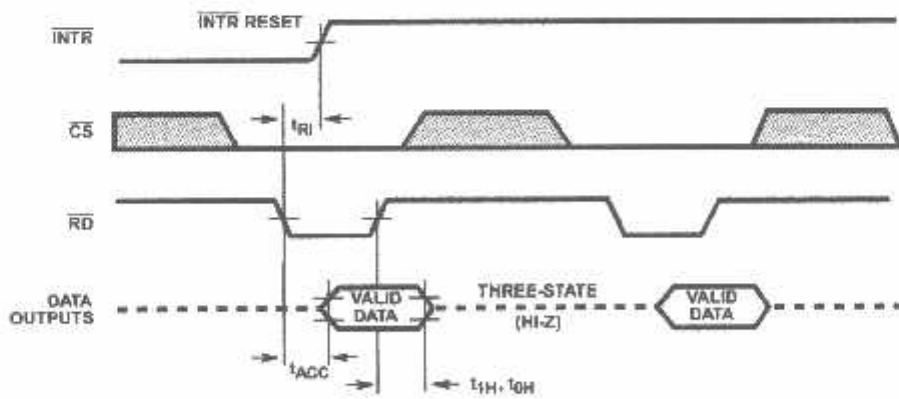


FIGURE 10B. OUTPUT ENABLE AND RESET INTR

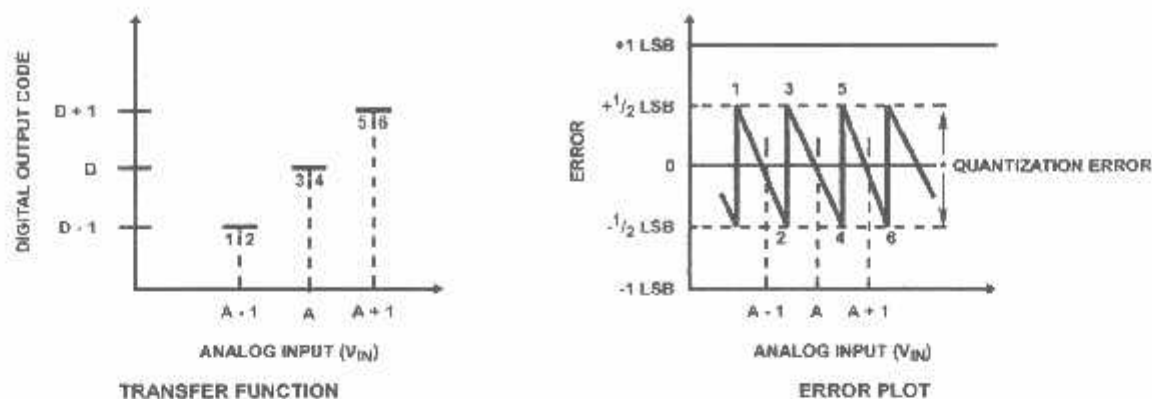
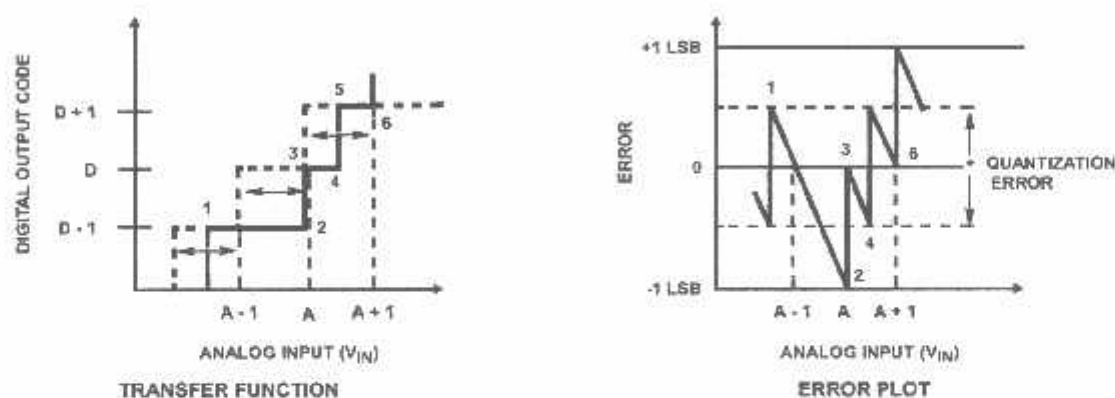
FIGURE 11A. ACCURACY = ± 0 LSB; PERFECT A/DFIGURE 11B. ACCURACY = $\pm 1/2$ LSB

FIGURE 11. CLARIFYING THE ERROR SPECS OF AN A/D CONVERTER

Understanding A/D Error Specs

A perfect A/D transfer characteristic (staircase wave-form) is shown in Figure 11A. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53mV with 2.5V tied to the $V_{REF/2}$ pin). The digital output codes which correspond to these inputs are shown as $D-1$, D , and $D+1$. For the perfect A/D, not only will center-value ($A-1$, A , $A+1$, ...) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located $\pm 1/2$ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend $\pm 1/2$ LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1 LSB wide.

The error curve of Figure 11B shows the worst case transfer function for the ADC0802. Here the specification guarantees that if we apply an analog input equal to the LSB analog voltage center-value, the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Notice that the error includes the quantization uncertainty of the A/D. For example, the error at point 1 of Figure 11A is $+1/2$ LSB because the digital code appeared $1/2$ LSB in advance of the center-value of the tread. The error plots always have a

constant negative slope and the abrupt upside steps are always 1 LSB in magnitude, unless the device has missing codes.

Detailed Description

The functional diagram of the ADC0802 series of A/D converters operates on the successive approximation principle (see Application Notes AN016 and AN020 for a more detailed description of this principle). Analog switches are closed sequentially by successive-approximation logic until the analog differential input voltage [$V_{IN(+)} - V_{IN(-)}$] matches a voltage derived from a tapped resistor string across the reference voltage. The most significant bit is tested first and after 8 comparisons (64 clock cycles), an 8-bit binary code (1111 1111 = full scale) is transferred to an output latch.

The normal operation proceeds as follows. On the high-to-low transition of the WR input, the internal SAR latches and the shift-register stages are reset, and the INTR output will be set high. As long as the CS input and WR input remain low, the A/D will remain in a reset state. Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition. After the requisite number of clock pulses to complete the conversion, the INTR pin will make a high-to-low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion. A RD operation (with CS low) will clear the INTR line high again.

The device may be operated in the free-running mode by connecting INTR to the WR input with CS = 0. To ensure start-up under all possible conditions, an external WR pulse is required during the first power-up cycle. A conversion-in-process can be interrupted by issuing a second start command.

Digital Operation

The converter is started by having CS and WR simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the interrupt (INTR) F/F and inputs a "1" to the D flip-flop, DFF1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of DFF1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either WR or CS is a "1"), the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This allows for asynchronous or wide CS and WR signals.

After the "1" is clocked through the 8-bit shift register (which completes the SAR operation) it appears as the input to DFF2. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the Three-State output latches. When DFF2 is subsequently clocked, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the INTR output signal.

When data is to be read, the combination of both CS and RD being low will cause the INTR F/F to be reset and the three-state output latches will be enabled to provide the 8-bit digital outputs.

Digital Control Inputs

The digital control inputs (CS, RD, and WR) meet standard TTL logic voltage levels. These signals are essentially equivalent to the standard A/D Start and Output Enable control signals, and are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the CS input (pin 1) can be grounded and the standard A/D Start function obtained by an active low pulse at the WR input (pin 3). The Output Enable function is achieved by an active low pulse at the RD input (pin 2).

Analog Operation

The analog comparisons are performed by a capacitive charge summing circuit. Three capacitors (with precise ratioed values) share a common node with the input to an auto-zeroed comparator. The input capacitor is switched between $V_{IN(+)}$ and $V_{IN(-)}$, while two ratioed reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the current total value set by the successive approximation register. A correction is made to offset the comparison by $1/2$ LSB (see Figure 11A).

Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D gains considerable applications flexibility from the analog differential voltage input. The $V_{IN(-)}$ input (pin 7) can be used

to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4mA - 20mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is $4^{1/2}$ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_E(\text{MAX}) = (V_{\text{PEAK}})(2\pi f_{\text{CM}}) \left[\frac{4.5}{f_{\text{CLK}}} \right]$$

where:

ΔV_E is the error voltage due to sampling delay,

V_{PEAK} is the peak value of the common-mode voltage,

f_{CM} is the common-mode frequency.

For example, with a 60Hz common-mode frequency, f_{CM} , and a 640kHz A/D clock, f_{CLK} , keeping this error to $1/4$ LSB ($\sim 5\text{mV}$) would allow a common-mode voltage, V_{PEAK} , given by:

$$V_{\text{PEAK}} = \frac{[\Delta V_E(\text{MAX})(f_{\text{CLK}})]}{(2\pi f_{\text{CM}})(4.5)}$$

or

$$V_{\text{PEAK}} = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)} \approx 1.9\text{V}.$$

The allowed range of analog input voltage usually places more severe restrictions on input common-mode voltage levels than this.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see Reference Voltage Span Adjust).

Analog Input Current

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance to ground is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These current transients occur at the leading edge of the internal clocks. They rapidly decay and do not inherently cause errors as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage at full scale. For a 640kHz clock frequency with the $V_{IN(+)}$ input at 5V, this DC current is at a maximum of approximately $5\mu\text{A}$. Therefore, **bypass capacitors should not be used at the analog inputs or the $V_{\text{REF}}/2$ pin** for high resistance sources ($>1\text{k}\Omega$). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the effects of the voltage drop across this input resistance, due to the average value of the input current, can be compensated by a full scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage at a constant conversion rate.

Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used will not cause errors since the input currents settle out prior to the comparison time. If a low-pass filter is required in the system, use a low-value series resistor ($\leq 1k\Omega$) for a passive RC section or add an op amp RC active low-pass filter. For low-source-resistance applications ($\leq 1k\Omega$), a $0.1\mu F$ bypass capacitor at the inputs will minimize EMI due to the series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the R and C are placed outside the feedback loop) from the output of an op amp, if used.

Stray Pickup

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize stray signal pickup (EMI). Both EMI and undesired digital-clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below $5k\Omega$. Larger values of source resistance can cause undesired signal pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate this pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see Analog Input Current). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be compensated by a full scale adjustment of the A/D (see Full Scale Adjustment) with the source resistance and input bypass capacitor in place, and the desired conversion rate.

Reference Voltage Span Adjust

For maximum application flexibility, these A/Ds have been designed to accommodate a 5V, 2.5V or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 12.

Notice that the reference voltage for the IC is either $1/2$ of the voltage which is applied to the $V+$ supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a pseudo-ratiometric voltage reference using, for the $V+$ supply, a 5V reference voltage. Alternatively, a voltage less than 2.5V can be applied to the $V_{REF}/2$ input. The internal gain to the $V_{REF}/2$ input is 2 to allow this factor of 2 reduction in the reference voltage.

Such an adjusted reference voltage can accommodate a reduced span or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5V to 3.5V, instead of 0V to 5V, the span would be 3V. With 0.5V applied to the $V_{IN(-)}$ pin to absorb the offset, the reference voltage can be made equal to $1/2$ of the 3V span or 1.5V. The A/D now will encode the $V_{IN(+)}$ signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5V input corresponding to full scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range. The requisite connections are shown in Figure 13. For expanded scale inputs, the circuits of Figures 14 and 15 can be used.

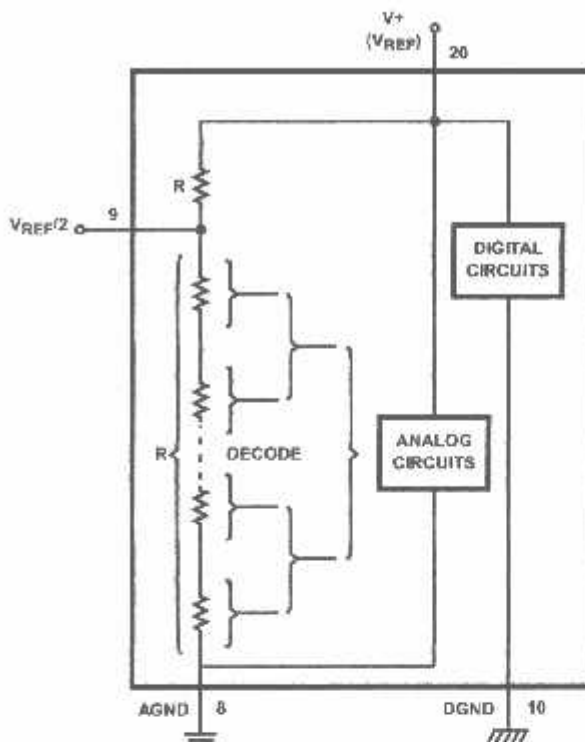


FIGURE 12. THE $V_{REFERENCE}$ DESIGN ON THE IC

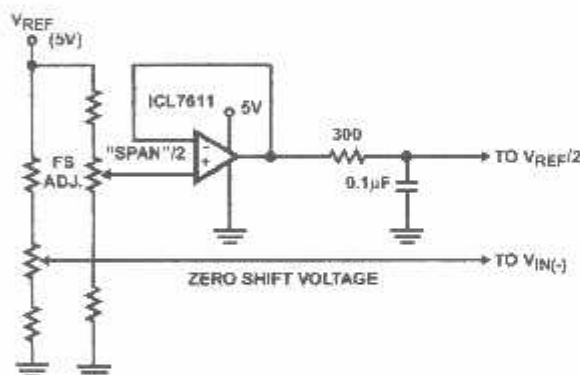


FIGURE 13. OFFSETTING THE ZERO OF THE ADC0802 AND PERFORMING AN INPUT RANGE (SPAN) ADJUSTMENT

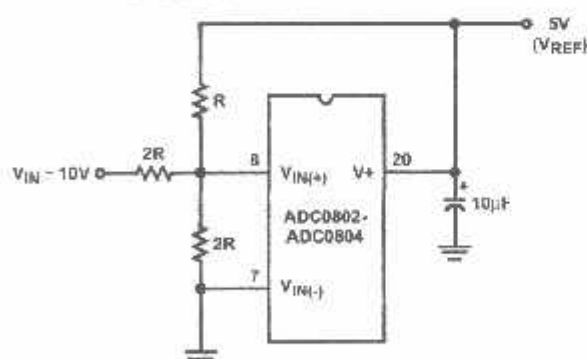


FIGURE 14. HANDLING $\pm 10V$ ANALOG INPUT RANGE

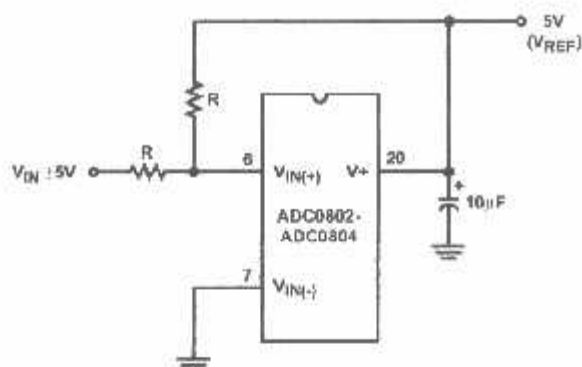


FIGURE 15. HANDLING ±5V ANALOG INPUT RANGE

Reference Accuracy Requirements

The converter can be operated in a pseudo-ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5V nominal value, initial errors of $\pm 10\text{mV}$ will cause conversion errors of ± 1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20mV (5V span) to 10mV and 1 LSB at the $V_{REF}/2$ input becomes 5mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive.

Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN(-)}$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal $1/2$ LSB value ($1/2$ LSB = 9.8mV for $V_{REF}/2 = 2.500\text{V}$).

Full Scale Adjust

The full scale adjustment can be made by applying a differential input voltage which is $1\frac{1}{2}$ LSB down from the desired analog full scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span-adjusted $V_{REF}/2$ voltage, the full scale adjustment is made by inputting V_{MIN} to the $V_{IN(-)}$ input of the A/D and applying a voltage to the $V_{IN(+)}$ input which is given by:

$$V_{IN(+)} f_{SADJ} = V_{MAX} + 1.5 \left[\frac{V_{MAX} - V_{MIN}}{256} \right],$$

where:

V_{MAX} = the high end of the analog input range,

and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

Clocking Option

The clock for the A/D can be derived from an external source such as the CPU clock or an external RC network can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 16.

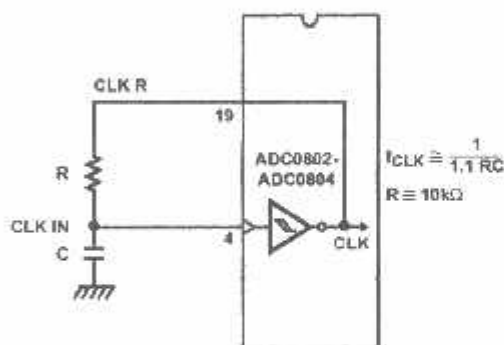


FIGURE 16. SELF-CLOCKING THE A/D

Heavy capacitive or DC loading of the CLK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF, such as driving up to 7 A/D converter clock inputs from a single CLK R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin (do not use a standard TTL buffer).

Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in progress is not completed. The data from the previous conversion remain in this latch.

Continuous Conversions

In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the INTR output. This $\overline{WR}$ and INTR node should be momentarily forced to logic low following a power-up cycle to insure circuit operation. See Figure 17 for details.

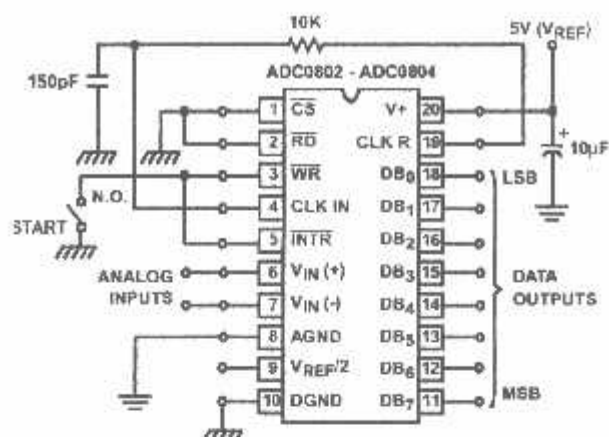


FIGURE 17. FREE-RUNNING CONNECTION

Driving the Data Bus

This CMOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in three-state (high-impedance mode). Back plane busing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see Typical Performance Curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock-extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be three-state buffers (low power Schottky is recommended, such as the 74LS240 series) or special higher-drive-current products which are designed as bus drivers. High-current bipolar bus drivers with PNP inputs are recommended.

Power Supplies

Noise spikes on the V+ supply line can cause conversion errors as the comparator will respond to this noise. A low-inductance tantalum filter capacitor should be used close to the converter V+ pin, and values of 1μF or greater are recommended. If an unregulated voltage is available in the system, a separate 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V+ supply. An ICL7663 can be used to regulate such a supply from an input as low as 5.2V.

Wiring and Hook-Up Precautions

Standard digital wire-wrap sockets are not satisfactory for breadboarding with this A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped and kept as far away as possible from the analog

signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup; therefore, shielded leads may be necessary in many applications.

A single-point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any VREF/2 bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of 1/4 LSB can usually be traced to improper board layout and wiring (see Zero Error for measurement). Further information can be found in Application Note AN018.

Testing the A/D Converter

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 18.

For ease of testing, the VREF/2 (pin 9) should be supplied with 2.560V and a V+ supply voltage of 5.12V should be used. This provides an LSB value of 20mV.

If a full scale adjustment is to be made, an analog input voltage of 5.090V (5.120 - 1/2 LSB) should be applied to the VIN(+) pin with the VIN(-) pin grounded. The value of the VREF/2 input voltage should be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of VREF/2 should then be used for all the tests.

The digital-output LED display can be decoded by dividing the 8 bits into 2 hex characters, one with the 4 most-significant bits (MS) and one with the 4 least-significant bits (LS). The output is then interpreted as a sum of fractions times the full scale voltage:

$$V_{OUT} = \left(\frac{MS}{16} + \frac{LS}{256} \right) 5.12V$$

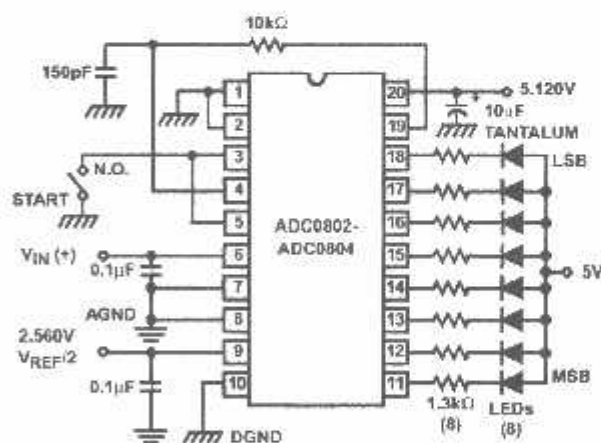


FIGURE 18. BASIC TESTER FOR THE A/D

For example, for an output LED display of 1011 0110, the MS character is hex B (decimal 11) and the LS character is hex (and decimal) 6, so:

$$V_{OUT} = \left(\frac{11}{16} + \frac{6}{256} \right) 5.12V = 3.64V$$

Figures 19 and 20 show more sophisticated test circuits.

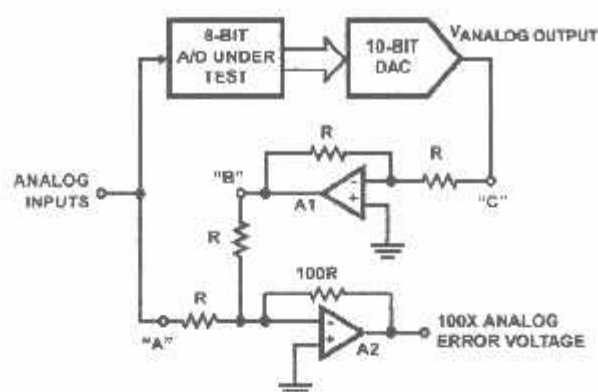


FIGURE 19. AD TESTER WITH ANALOG ERROR OUTPUT. THIS CIRCUIT CAN BE USED TO GENERATE "ERROR PLOTS" OF FIGURE 11.



FIGURE 20. BASIC "DIGITAL" A/D TESTER

Typical Applications

nterfacing 8080/85 or Z-80 Microprocessors

This converter has been designed to directly interface with 8080/85 or Z-80 Microprocessors. The three-state output capability of the A/D eliminates the need for a peripheral interface device, although address decoding is still required to generate the appropriate $\overline{CS}$ for the converter. The A/D can be mapped into memory space (using standard memory-address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{IOR}$ and $\overline{IOW}$ strobes and decoding the address bits A0 $\rightarrow$ A7 (or address bits A8 $\rightarrow$ A15, since they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 3-bit address decoder, but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. See AN020 for more discussion of memory-mapped vs I/O-mapped interfaces. An example of an A/D in I/O space is shown in Figure 21.

The standard control-bus signals of the 8080 ($\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the ΔD , since the bus timing requirements, to allow both starting the converter, and outputting the data onto the data bus, are met. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100pF.

It is useful to note that in systems where the A/D converter is 1 of 8 or fewer I/O-mapped devices, no address-decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as CS inputs, one for each I/O device.

Interfacing the Z-80 and 8085

The Z-80 and 8085 control buses are slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals have to be combined with the generalized strobes to provide the appropriate signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 22. By using $\overline{MREQ}$ in place of $\overline{IORQ}$, a memory-mapped configuration results.

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

The 8085 also provides a generalized $\overline{RD}$ and $\overline{WR}$ strobe, with an $IO/\overline{M}$ line to distinguish I/O and memory requests. The circuit of Figure 22 can again be used, with $IO/\overline{M}$ in place of $\overline{IORQ}$ for a memory-mapped interface, and an extra inverter (or the logic equivalent) to provide $\overline{IO/\overline{M}}$ for an I/O-mapped connection.

Interfacing 6800 Microprocessor Derivatives (6502, etc.)

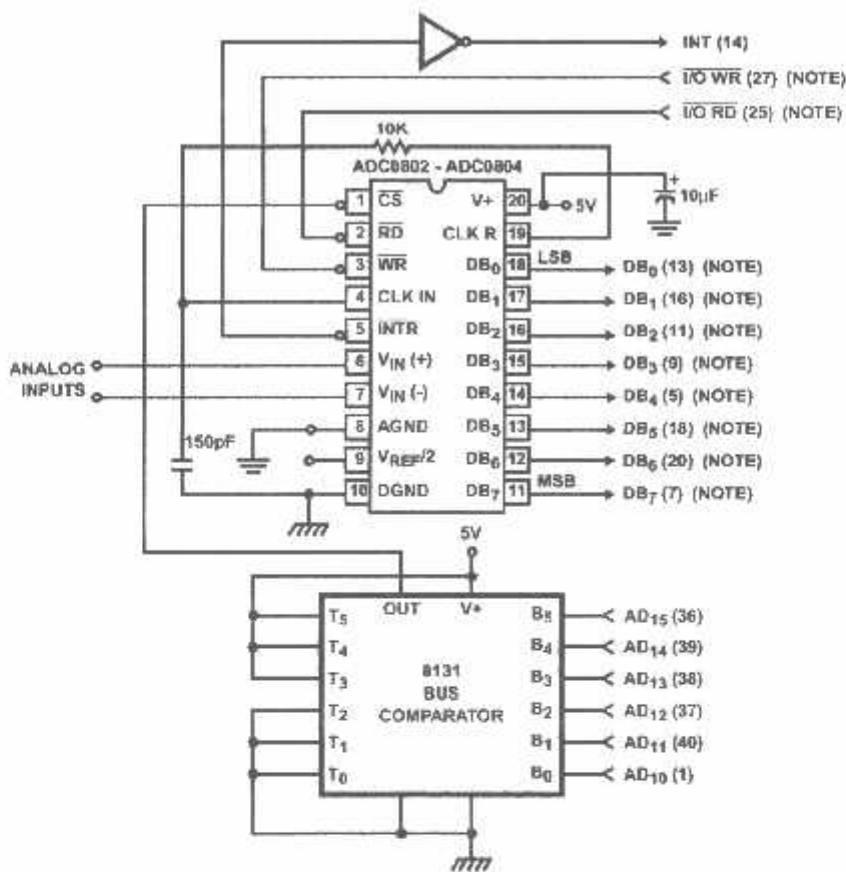
The control bus for the 6800 microprocessor derivatives does not use the RD and WR strobe signals. Instead it employs a single R/W line and additional timing, if needed, can be derived from the $\phi 2$ clock. All I/O devices are memory-mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 23 shows an interface schematic where the A/D is memory-mapped in the 6800 system. For simplicity, the CS decoding is shown using $1\frac{1}{2}$ DM8092. Note that in many 6800 systems, an already decoded 4/5 line is brought out to the common bus at pin 21. This can be tied directly to the CS pin of the A/D, provided that no other devices are addressed at HEX ADDR: 40XX or 5XXX.

In Figure 24 the ADC0802 series is interfaced to the MC6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter (PIA). Here the CS pin of the A/D is grounded since the PIA is already memory-mapped in the MC6800 system and no CS decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D RD pin can be grounded.

Application Notes

NOTE #	DESCRIPTION	AnswerFAX DOC. #
AN016	"Selecting A/D Converters"	9016
AN018	"Do's and Don'ts of Applying A/D Converters"	9018
AN020	"A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"	9020
AN030	"The ICL7104 - A Binary Output A/D Converter for Microprocessors"	9030

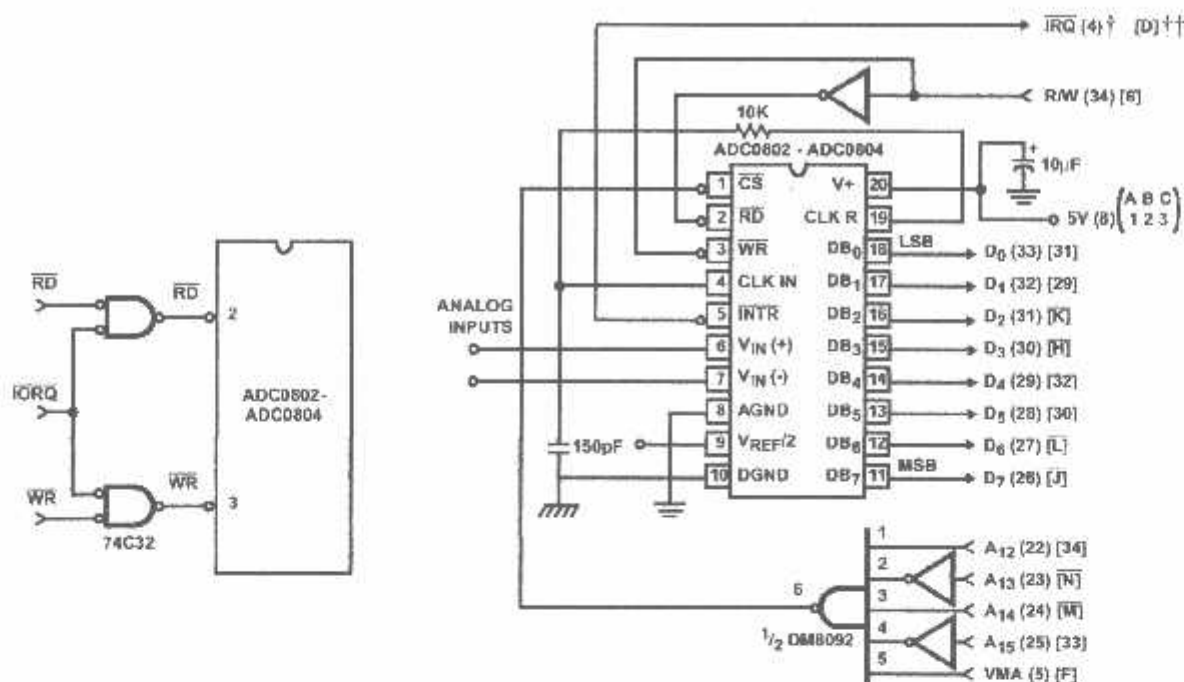
ADC0802, ADC0803, ADC0804



NOTE: Pin numbers for 8228 System Controller: Others are 8080A.

FIGURE 21. ADC0802 TO 8080A CPU INTERFACE

ADC0802, ADC0803, ADC0804



[‡] Numbers in parentheses refer to MC6800 CPU Pinout.

†† Numbers or letters in brackets refer to standard MCG800 System Common Bus Code.

FIGURE 22. MAPPING THE A/D AS AN I/O DEVICE FOR USE WITH THE Z-80 CPU

FIGURE 23. ADC0802 TO MC6800 CPU INTERFACE

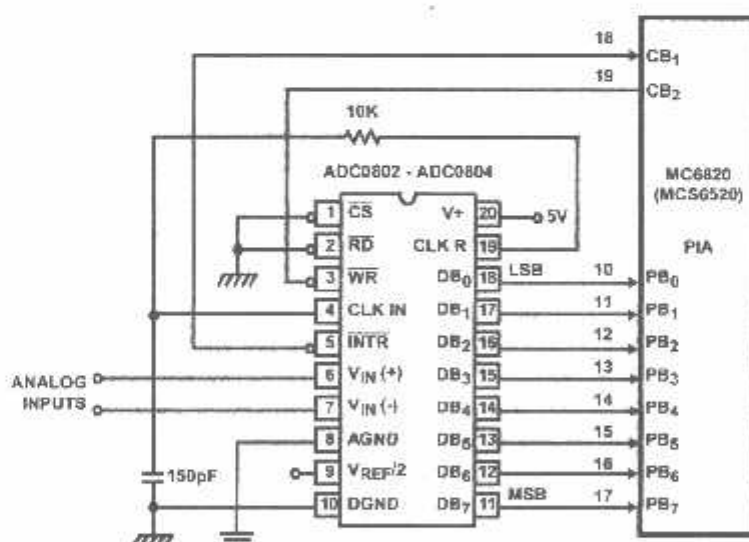


FIGURE 24. ADC0802 TO MC6820 PIA INTERFACE

ADC0802, ADC0803, ADC0804

Die Characteristics

DIE DIMENSIONS:

(101 mils x 93 mils) x 525µm x 25µm

METALLIZATION:

Type: Al

Thickness: 10kÅ ± 1kÅ

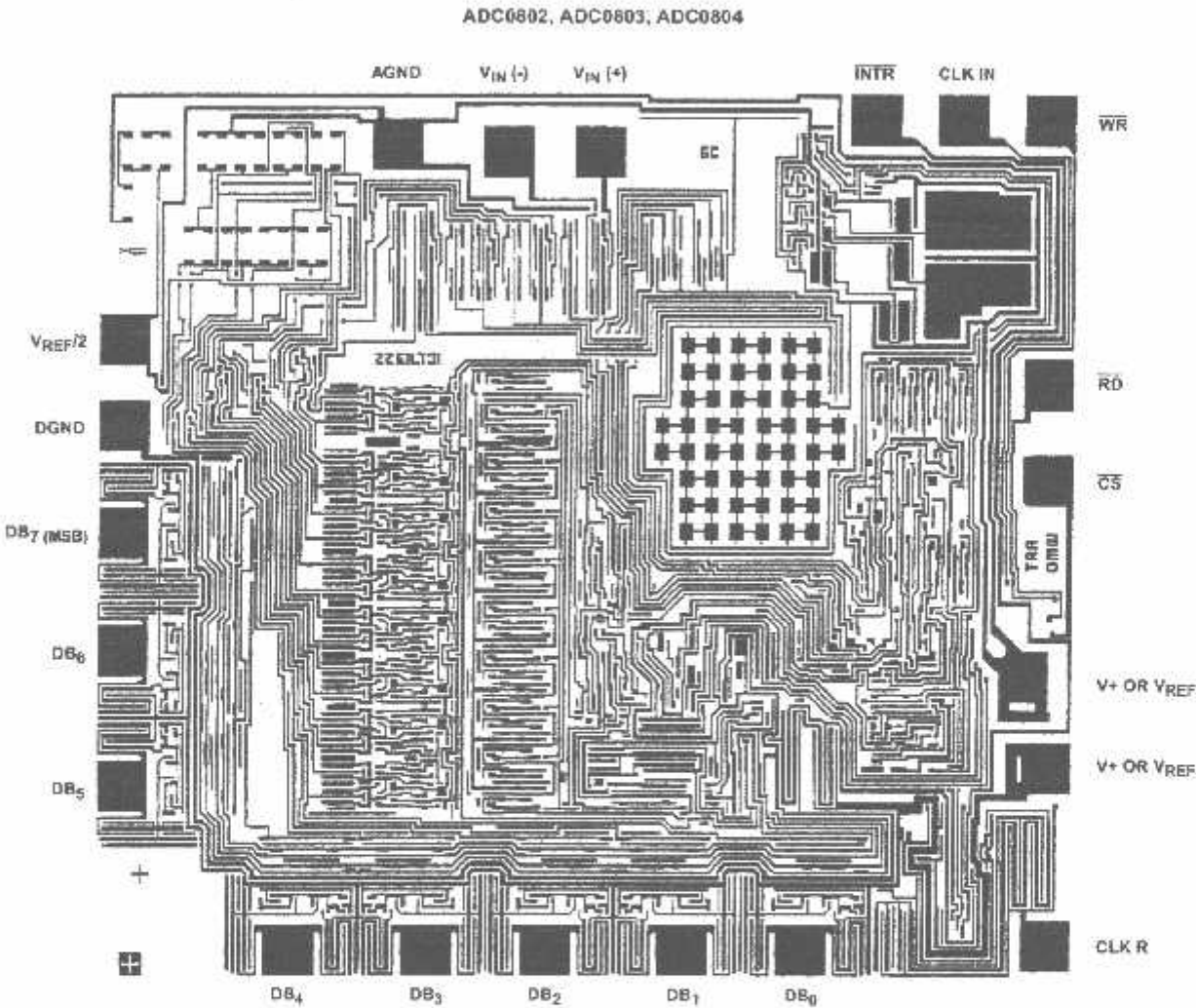
PASSIVATION:

Type: Nitride over Silox

Nitride Thickness: 8kÅ

Silox Thickness: 7kÅ

Metallization Mask Layout



MAXIM**+5V-Powered, Multichannel RS-232 Drivers/Receivers****General Description**

The MAX220-MAX249 family of line drivers/receivers is designed for all CIA/TIA-232E and V.28/V.24 communications interfaces, particularly applications where $\pm 12V$ is unavailable.

These parts are especially useful in battery-powered systems, since their low-power shutdown mode reduces power dissipation to less than 15 μ W. The MAX220, MAX233, MAX235, and MAX245/MAX246/MAX247 use no external components and are recommended for applications where printed circuit board space is critical.

Applications

Portable Computers
Low-Power Modems
Interface Translation
Battery-Powered RS-232 Systems
Multidrop RS-232 Networks

Next-Generation Device Features

- For Low-Voltage, Integrated ESD Applications:
MAX3222E/MAX3232E/MAX3237E/MAX3241E/
MAX3246E: +3.0V to +6.5V, Low-Power, Up to
1Mbps, True RS-232 Transceivers Using Four
0.1 μ F External Capacitors (MAX3246E Available in
a UCSP™ Package)
- For Low-Cost Applications:
MAX221E: $\pm 15kV$ ESD-Protected, +5V, 1 μ A, Single
RS-232 Transceiver with AutoShutdown™

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX220CPE	0°C to +70°C	16 Plastic DIP
MAX220CSE	0°C to +70°C	16 Narrow SO
MAX220CWE	0°C to +70°C	16 Wide SO
MAX220C77	0°C to +77°C	16Pac
MAX220EPE	-40°C to +85°C	16 Plastic DIP
MAX220EPE	-40°C to +85°C	16 Narrow SO
MAX220EWE	-40°C to +85°C	16 Wide SO
MAX220EJE	-40°C to +85°C	16 CERDIP
MAX220MJE	-55°C to +125°C	16 CERDIP

Ordering Information continued at end of data sheet.

*Contact factory for direct specifications.

Selection Table

Part Number	Power Supply (V)	No. of RS-232 Drivers/Rx	No. of Ext. Caps	Nominal Cap. Value (μ F)	SHDN & Three-State	Rx Active In SHDN	Data Rate (kbps)	Features
MAX220	+5	2/2	4	0.1	No	—	120	Ultra-low-power, industry-standard pinout
MAX222	+5	2/2	4	0.1	Yes	—	200	Low-power, standard pinout
MAX221 (MAX221)	+5	4/0	—	1.0 (0.1)	Yes	✓	120	MAX241 and MAX242, AutoShutdown™
MAX225	+5	5/0	0	—	Yes	✓	120	Available in SO
MAX230 (MAX230)	+5	1/0	—	1.0 (0.1)	Yes	—	120	5-pin version with shutdown
MAX231 (MAX231)	+5 and -15 to +15.2	2/2	2	1.0 (0.1)	No	—	120	Standard $\pm 12V$ or battery supplies, same functions as MAX232
MAX232 (MAX232)	+5	2/2	4	1.0 (0.1)	No	—	120 (5.4)	Industry standard
MAX232A	+5	2/2	4	0.1	No	—	120	Higher slew rate, small caps
MAX233 (MAX233)	+5	2/2	0	—	No	—	120	No external caps
MAX234	+5	2/2	0	—	No	—	120	No external caps, high slew rate
MAX235 (MAX235)	+5	4/0	—	1.0 (0.1)	No	—	120	Replaces 1480
MAX236 (MAX236)	+5	5/0	0	—	Yes	—	120	No external caps
MAX237 (MAX237)	+5	4/0	—	1.0 (0.1)	Yes	—	120	Shutdown, three caps
MAX237 (MAX237)	+5	0/0	—	1.0 (0.1)	No	—	120	Conformer to EIA232-D and E
MAX238 (MAX238)	+5	4/0	—	1.0 (0.1)	No	—	120	Replaces 1480 and 1482
MAX239 (MAX239)	+5 and -15 to +15.2	0/0	2	1.0 (0.1)	No	—	120	Standard $\pm 12V$ or battery supplies, same functions as MAX232
MAX240	+5	5/0	—	1.0	Yes	—	120	DIP or ballpack package
MAX241 (MAX241)	+5	4/0	—	1.0 (0.1)	Yes	—	120	On-chip 100 μ F RC capacitor
MAX242	+5	0/0	4	0.1	Yes	✓	200	Separate shutdown and enable
MAX242	+5	2/2	4	0.1	No	—	200	Open line, resolution complies with EIA
MAX244	+5	5/10	0	—	No	—	120	High slew rate
MAX246	+5	5/10	0	—	Yes	✓	120	High slew rate, 10 caps, two shutdown modes
MAX246	+5	5/10	0	—	Yes	✓	120	High slew rate, 10 caps, three shutdown modes
MAX247	+5	5/0	0	—	Yes	✓	120	High slew rate, 10 caps, three shutdown modes
MAX248	+5	0/0	4	1.0	Yes	✓	120	High slew rate, selective on-chip analysis
MAX248	+5	0/10	0	1.0	Yes	✓	1.0*	Available in green temp. package

MAXIM

Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 888-629-4642, or visit Maxim's website at www.maxim-ic.com.

MAX220-MAX249

5V-Powered, Multichannel RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS—MAX220/222/232A/233A/242/243

Supply Voltage (V _{CC})	0.3V to +6V
I _O Voltages	
I _{OL} (Except MAX220)	-0.3V to (V _{CC} + 0.5V)
I _{OH} (Except MAX220)	+0.3V to (V _{CC} + 0.5V)
I _{OL} (Except MAX220) (Note 1)	+13V
I _{OH} (MAX220)	+13.0V
Input Voltages	
V _{IL}	-0.3V to (V _{CC} + 0.5V)
V _{IH}	(V _{CC} - 0.3V) to (V _{CC} + 0.5V)
Receiver Output Short-Circuited to GND (Note 2)	Continuous
Maximum Power Dissipation (T _A = +70°C)	
16-Pin Plastic DIP (derate 10.58mW/°C above +70°C)	840mW
34-Pin Plastic DIP (derate 10.58mW/°C above +70°C)	800mW

20-Pin Plastic DIP (derate 8.00mW/°C above +70°C)	740mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C)	896mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C)	762mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C)	762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C)	800mW
20-Pin SSOP (derate 8.00mW/°C above +70°C)	640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C)	800mW
10-Pin CERDIP (derate 10.00mW/°C above +70°C)	842mW
Operating Temperature Ranges	
MAX220, MAX222	-40°C to +75°C
MAX222, MAX223	-40°C to +125°C
MAX223, MAX224	-55°C to +125°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Input voltage measured with I_{OL} in high-impedance state, SHDN = V_{CC} or V_{CC} = 5V.
Note 2: For the MAX220, V_L and V_H can have a maximum magnitude of 7V, but their absolute difference cannot exceed 10V.
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Maximum stress ratings are for absolute maximum values only. Exceeding these ratings may affect device reliability and performance. These ratings are not intended to be used for extended periods of time. Exceeding these ratings may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243

V_{CC} = +5V ±10%, C1-C4 = 0.1μF, MAX220, C1 = 0.047μF, C2-C4 = 0.33μF, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS					
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND	±5	±5		V
Input Logic Threshold Low			1.4	0.0	V
Input Logic Threshold High	All devices except MAX220 MAX220: V _{CC} = 3.0V	2.4	4		V
Output Pull-Up/Down Current	All except MAX220, normal operation SHDN = 0V, MAX222/242, shutdown, MAX220		5	40	μA
Output Leakage Current	V _{CC} = 5.5V, SHDN = 0V, V _{OUT} = ±15V, MAX222/242 V _{CC} = SHDN = 0V, V _{OUT} = ±15V	±0.01	±10		μA
Logic Rate			200	116	kbaud
Receiver Output Resistance	V _{CC} = V _L = V _H = 0V, V _{OUT} = ±2V	500	100		Ω
Output Short-Circuit Current	V _{OUT} = 0V	±7	±22		mA
RS-232 RECEIVERS					
RS-232 Input Voltage Operating Range				±30	V
RS-232 Input Threshold Low	V _{CC} = 5V	All except MAX243 R2in MAX243 R2in (Note 2)	0.8	1.3	V
RS-232 Input Threshold High	V _{CC} = 5V	All except MAX243 R2in MAX243 R2in (Note 2)	1.8	2.4	V
RS-232 Input Hysteresis	All except MAX243: V _{CC} = 5V, no hysteresis in input MAX243	0.2	0.5	1	V
RS-232 Input Resistance		3	5	7	kΩ
TLCMOS Output Voltage Low	I _{OUT} = 3.2mA		0.2	0.4	V
TLCMOS Output Voltage High	I _{OUT} = -1.0mA	3.5	V _{CC} - 0.2		V
TLCMOS Output Short-Circuit Current	Sourcing V _{OUT} = GND Sinking V _{OUT} = V _{CC}	2	10	30	mA

MAXIM

+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220-MAX249

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243 (continued)

$V_{CC} = +5V \pm 10\%$, C_1 – $C_4 = 0.1\mu F$, MAX220, $C_1 = 0.047\mu F$, C_2 – $C_4 = 0.33\mu F$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

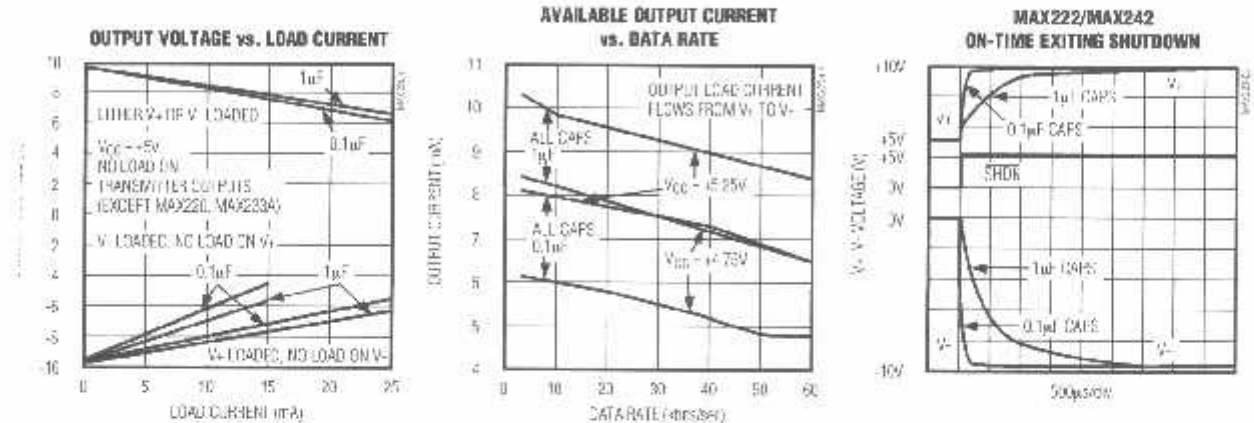
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TL/CMOS Output Leakage Current:	SHDN = V_{CC} or EN = V_{CC} (SHDN = 0V for MAX222), 0V $\leq V_{OUT} \leq V_{CC}$			± 0.05	± 10	μA
$\overline{N}$ Input Threshold Low	MAX242			1.4	0.9	V
$\overline{N}$ Input Threshold High	MAX242		2.0	1.4		V
Operating Supply Voltage			4.5		5.5	V
I_{CC} Supply Current (SHDN = V_{CC}), Figures 5, 6, 11, 19	No load	MAX220		0.5	2	mA
		MAX222/232A/233A/242/243		4	10	
	3k Ω load both inputs	MAX220		12		
		MAX222/232A/233A/242/243		15		
Shutdown Supply Current:	MAX222/242	$T_A = +25^\circ C$		0.1	10	μA
		$T_A = 0^\circ C$ to $+70^\circ C$		2	50	
		$T_A = -40^\circ C$ to $-85^\circ C$		2	50	
		$T_A = -55^\circ C$ to $-125^\circ C$		35	100	
HCN Input Leakage Current:	MAX222/242				± 1	μA
HCN Threshold Low	MAX222/242			1.4	0.8	V
HCN Threshold High	MAX222/242		2.0	1.4		V
Transition Slew Rate	$C_L = 50pF$ to $2500pF$, $R_L = 3k\Omega$ to $7k\Omega$, $V_{CC} = 5V$, $T_A = -25^\circ C$, measured from +3V to -3V or -3V to +3V	MAX222/232A/233A/242/243	6	12	30	V/ μs
		MAX220	1.5	3	30	
Transmitter Propagation Delay TTL to RS-232 (Normal Operation), Figure 1	t_{PHLT}	MAX222/232A/233A/242/243		1.3	3.5	μs
		MAX220		4	10	
	t_{PLHT}	MAX222/232A/233A/242/243		1.5	3.5	
		MAX220		5	10	
Receiver Propagation Delay RS-232 to TTL (Normal Operation), Figure 2	t_{PHLR}	MAX222/232A/233A/242/243		0.5	1	μs
		MAX220		0.6	3	
	t_{PLHR}	MAX222/232A/233A/242/243		0.6	1	
		MAX220		0.8	3	
Receiver Propagation Delay RS-232 to TTL (Shutdown), Figure 2	t_{PHLS}	MAX242		0.5	10	μs
	t_{PLLS}	MAX242		2.5	10	
Receiver-Output Enable Time, Figure 3	t_{OE}	MAX242		125	500	ns
Receiver-Output Disable Time, Figure 3	t_{OD}	MAX242		160	500	ns
Transmitter-Output Enable Time SHDN Goes High, Figure 4	t_{ET}	MAX222/242, 0.1 μF caps (includes charge-pump start-up)		250		μs
Transmitter-Output Disable Time SHDN Goes Low, Figure 4	t_{DT}	MAX222/242, 0.1 μF caps		600		ns
Transmitter + to - Propagation Delay Difference (Normal Operation)	$t_{PHLT} - t_{PLHT}$	MAX222/232A/233A/242/243		300		ns
		MAX220		2000		
Receiver + to - Propagation Delay Difference (Normal Operation)	$t_{PHLR} - t_{PLHR}$	MAX222/232A/233A/242/243		100		ns
		MAX220		225		

Note 3: MAX243 R2OUT is guaranteed to be low when R2IN is $\geq 0V$ or is floating.

5V-Powered, Multichannel RS-232 Drivers/Receivers

Typical Operating Characteristics

MAX220/MAX222/MAX232A/MAX233A/MAX242/MAX243



+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220-MAX249

ABSOLUTE MAXIMUM RATINGS—MAX223/MAX230-MAX241

V _{CC}	-0.3V to +6V	20-Pin Wide SO (derate 10.00mW/°C above +70°C)	800mW
V _{CE}	(V _{CC} - 0.3V) to +14V	24-Pin Wide SO (derate 11.76mW/°C above +70°C)	941mW
V _{EE}	+0.3V to -14V	28-Pin Wide SO (derate 12.50mW/°C above +70°C)	1W
Input Voltages			
V _I	-0.3V to (V _{CC} + 0.3V)	44-Pin Plastic FP (derate 11.11mW/°C above +70°C)	839mW
V _{IN}	+30V	14-Pin CERDIP (derate 9.09mW/°C above +70°C)	727mW
Output Voltages			
V _{OUT}	(V ₊ + 0.3V) to (V ₋ - 0.3V)	16-Pin CERDIP (derate 10.00mW/°C above +70°C)	800mW
V _{OUT}	-0.3V to (V _{CC} + 0.3V)	20-Pin CERDIP (derate 11.11mW/°C above +70°C)	839mW
Short-Circuit Duration, I _{OUT}			
Continuous			
Power Dissipation (T _A = +70°C)			
1-Pin Plastic DIP (derate 10.00mW/°C above +70°C)			
800mW			
8-Pin Plastic DIP (derate 10.53mW/°C above +70°C)			
842mW			
9-Pin Plastic DIP (derate 11.11mW/°C above +70°C)			
889mW			
4-Pin Narrow Plastic DIP			
(derate 13.33mW/°C above +70°C)			
1.07W			
4-Pin Plastic DIP (derate 9.09mW/°C above +70°C)			
500mW			
5-Pin Wide SO (derate 9.52mW/°C above +70°C)			
762mW			
24-Pin Narrow CERDIP			
(derate 12.50mW/°C above +70°C)			
1W			
24-Pin Sidebrazed (derate 20.0mW/°C above +70°C)			
1.6W			
28-Pin SSOP (derate 9.52mW/°C above +70°C)			
762mW			
Operating Temperature Ranges			
MAX220-C			
0°C to +70°C			
MAX220-E			
-40°C to +85°C			
MAX220-M			
-55°C to +125°C			
Storage Temperature Range			
-65°C to +160°C			
Lead Temperature (soldering, 10s)			
+300°C			

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX223/MAX230-MAX241

MAX223/230/232/234/236/237/238/240/241, V_{CC} = 15V ±10%; MAX233/MAX235, V_{CC} = 5V ±5%, C1-C4 = 1.0μF; MAX231/MAX239, C = 5V ±10%; V₊ = 7.5V to 13.2V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground	±5.0	±7.3		V
CC Power-Supply Current	No load, T _A = +25°C	MAX223/233		5	mA
		MAX223/230/234-238/240/241		7	
		MAX231/239		0.4	
- Power-Supply Current		MAX231		1.8	mA
		MAX239		5	
		MAX223		15	
Shutdown Supply Current	T _A = +25°C	MAX230/235/236/240/241		1	μA
				10	
Input Logic Threshold Low	T _{IN} ; EN, SHDN (MAX233); EN, SHDN (MAX230/235-241)			0.8	V
Input Logic Threshold High	T _{IN}	2.0			V
	EN, SHDN (MAX223); EN, SHDN (MAX230/235/236/240/241)	2.4			
Logic Pull-Up Current	T _{IN} = 0V		1.5	200	μA
Receiver Input Voltage Operating Range		-30		30	V

5V-Powered, Multichannel RS-232 Drivers/Receivers

ELECTRICAL CHARACTERISTICS—MAX223/MAX230–MAX241 (continued)

MAX223/230/232/234/236/237/238/240/241, VCC = +5V ±10%; MAX233/MAX235, VCC = 5V ±5%; C1, C2 = 1.0µF; MAX231/MAX239, VCC = 5V ±10%; V+ = 7.5V to 13.2V; TA = TMIN to TMAX; unless otherwise noted.)

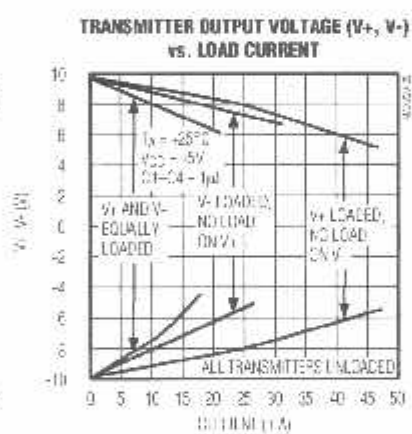
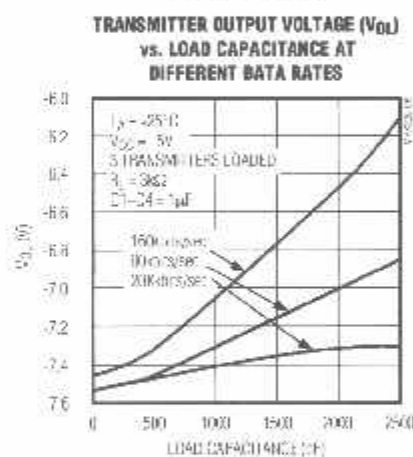
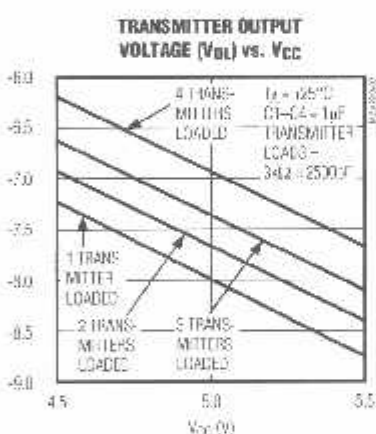
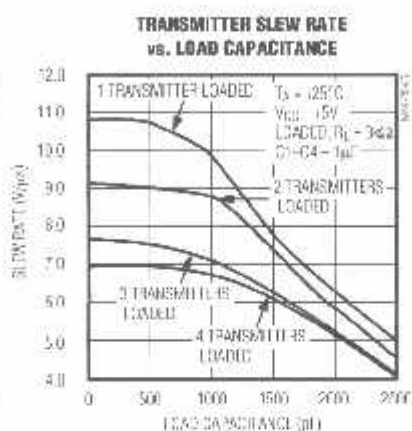
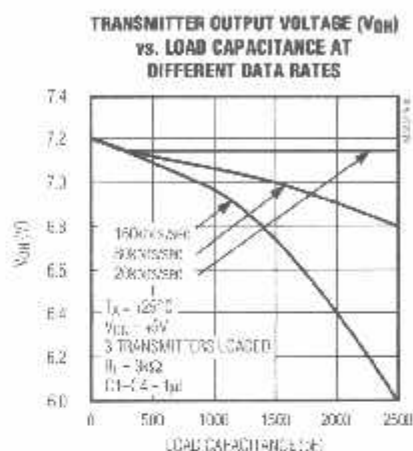
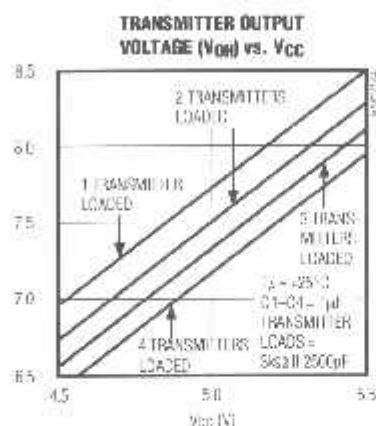
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
3-232 Input Threshold Low	T _A = +25°C, V _{CC} = 5V	Normal operation SHDN = 5V (MAX223) SHDN = 0V (MAX235/236/240/241)	0.8	1.2		V
		Shutdown (MAX223) SHDN = 0V, EN = 5V (R4 _{IN} , R5 _{IN})	0.6	1.5		
3-232 Input Threshold High	T _A = +25°C, V _{CC} = 5V	Normal operation SHDN = 5V (MAX223) SHDN = 0V (MAX235/236/240/241)		1.7	2.4	V
		Shutdown (MAX223) SHDN = 0V, EN = 5V (R4 _{IN} , R5 _{IN})		1.5	2.4	
3-232 Input Hysteresis	V _{CC} = 5V; no hysteresis in shutdown		0.2	0.5	1.0	V
3-232 Input Resistance	T _A = +25°C, V _{CC} = 5V		3	5	7	kΩ
TTL/CMOS Output Voltage Low	I _{OUT} = 1.6mA (MAX231/232/233, I _{OL1} = 3.2mA)				0.4	V
TTL/CMOS Output Voltage High	I _{OUT} = -1mA		3.5	V _{CC} - 0.4		V
TTL/CMOS Output Leakage Current	0V ≤ R _{OUT} ≤ V _{CC} , EN = 0V (MAX223); EN = V _{CC} (MAX235-241)			0.05	±10	μA
Receiver Output Enable Time	Normal operation	MAX223		600		ns
		MAX235/236/239/240/241		400		
Receiver Output Disable Time	Normal operation	MAX223		900		ns
		MAX235/236/239/240/241		250		
Propagation Delay	RS-232 IN to TTL/CMOS OUT, C _L = 150pF	Normal operation		0.5	10	μs
		SHDN = 0V (MAX223)	t _{PHLS}	4	40	
			t _{PLLS}	6	40	
Transition Region Slew Rate	MAX223/MAX230/MAX234-241, T _A = +25°C, V _{CC} = 5V, R _L = 3kΩ to 7kΩ, C _L = 50pF to 2500pF, measured from -3V to -3V or -3V to +3V		3	5.1	30	V/μs
	MAX231/MAX232/MAX233, T _A = +25°C, V _{CC} = 5V, R _L = 3kΩ to 7kΩ, C _L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V			4	30	
Transmitter Output Resistance	V _{CC} = V ₊ = V ₋ = 0V, V _{OUT} = ±2V		300			Ω
Transmitter Output Short-Circuit Current				+10		mA

+5V-Powered, Multichannel RS-232 Drivers/Receivers

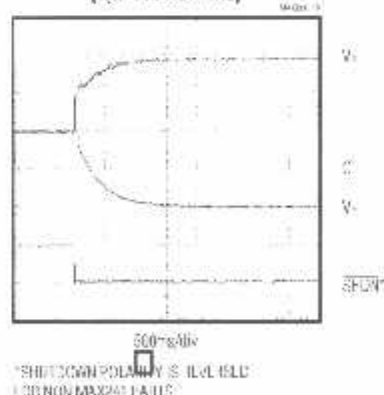
Typical Operating Characteristics

MAX223/MAX230-MAX241

MAX220-MAX249



V_+ , V_- WHEN EXITING SHUTDOWN (1µF CAPACITORS)



SHUTDOWN POLARITY IS ILV15LC
(OR NON-MAX241 PARTS)

-5V-Powered, Multichannel RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS—MAX225/MAX244—MAX249

Supply Voltage (V_{CC})	-0.3V to +6V	Continuous Power Dissipation ($T_A = +70^{\circ}\text{C}$)	
Output Voltages		28-Pin Wide SO (derate 12.50mW/ $^{\circ}\text{C}$ above $+70^{\circ}\text{C}$)	1W
$\overline{FNA}$, $\overline{FNB}$, $\overline{ENR}$, $\overline{ENT}$, $\overline{ENRA}$, $\overline{NRS}$, $\overline{FNTA}$, $\overline{ENTB}$	-0.3V to ($V_{CC} + 0.3\text{V}$)	40-Pin Plastic DIP (derate 11.11mW/ $^{\circ}\text{C}$ above $+70^{\circ}\text{C}$)	611mW
I_{IN}	$\pm 25\text{V}$	44-Pin PLCC (derate 13.33mW/ $^{\circ}\text{C}$ above $+70^{\circ}\text{C}$)	1.07W
I_{OUT} (Note 3)	$\pm 15\text{V}$	Operating Temperature Ranges	
I_{OUT}	-0.3V to ($V_{CC} + 0.3\text{V}$)	MAX225C__, MAX24__C	-0°C to $+70^{\circ}\text{C}$
Port Circuit (one output at a time)		MAX225E__, MAX24__E	-40°C to $+85^{\circ}\text{C}$
Output to GND	Continuous	Storage Temperature Range	-65°C to $+160^{\circ}\text{C}$
Output to GND	Continuous	Lead Temperature (soldering, 10s)	$+300^{\circ}\text{C}$

Note 4: Input voltage measured with transmitter output in a high-impedance state, shutdown, or $V_{CC} = 0\text{V}$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX225/MAX244—MAX249

MAX225, $V_{CC} = 5.0\text{V} \pm 5\%$; MAX244, MAX249, $V_{CC} = -5.0\text{V} \pm 10\%$, external capacitors C1-C4 = 1 μF ; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS					
Output Logic Threshold Low			1.4	0.8	V
Output Logic Threshold High		2	1.4		V
Logic Pull-Up/Input Current	Tables 1a-1d, Normal operation		10	50	μA
	Shutdown		± 0.01	± 1	
Data Rate	Tables 1a-1d, normal operation		120	64	kbps
Output Voltage Swing	All transmitter outputs loaded with 3k Ω to GND	± 5	± 7.5		V
Output Leakage Current (Shutdown)	Tables 1a-1n, $\overline{FNA}$, $\overline{FNB}$, $\overline{ENT}$, $\overline{FNTA}$, $\overline{ENTB} = V_{CC}$, $V_{OUT} = \pm 15\text{V}$		± 0.01	± 25	μA
	$V_{CC} = 0\text{V}$, $V_{OUT} = \pm 15\text{V}$		± 0.01	± 25	
Transmitter Output Resistance	$V_{CC} = V+ = V- = 0\text{V}$, $V_{OUT} = \pm 2\text{V}$ (Note 4)	300	10M		Ω
Output Short-Circuit Current	$V_{OUT} = 0\text{V}$	± 7	± 30		mA
RS-232 RECEIVERS					
RS-232 Input Voltage Operating Range				± 25	V
RS-232 Input Threshold Low	$V_{CC} = 5\text{V}$	0.8	1.5		V
RS-232 Input Threshold High	$V_{CC} = 5\text{V}$		1.8	2.4	V
RS-232 Input Hysteresis	$V_{CC} = 5\text{V}$	0.2	0.5	1.0	V
RS-232 Input Resistance		3	5	7	k Ω
TTL/CMOS Output Voltage Low	$I_{OUT} = 3.2\text{mA}$		0.2	0.4	V
TTL/CMOS Output Voltage High	$I_{OUT} = -1.0\text{mA}$	3.5	$V_{CC} - 0.2$		V
TTL/CMOS Output Short-Circuit Current	Sourcing $V_{OUT} = \text{GND}$	-2	-10		mA
	Sinking $V_{OUT} = V_{CC}$	10	50		
TTL/CMOS Output Leakage Current	Normal operation, outputs disabled, Tables 1a-1d, $0\text{V} \leq V_{OUT} \leq V_{CC}$, $\overline{ENRL} = V_{CC}$		± 0.05	± 0.10	μA

MAXIM

+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220-MAX249

ELECTRICAL CHARACTERISTICS—MAX225/MAX244-MAX249 (continued)

MAX225, $V_{CC} = 5.0V \pm 5\%$; MAX244-MAX249, $V_{CC} = +5.0V \pm 10\%$, external capacitors C1-C4 = 1 μF ; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY AND CONTROL LOGIC					
Operating Supply Voltage	MAX225	4.75		5.25	V
	MAX244-MAX249	4.5		5.5	
(cc) Supply Current (Normal Operation)	No load		10	20	mA
			11	30	
	3k Ω loads on all outputs		40		
			57		
Shutdown Supply Current	$T_A = +25^\circ C$		8	25	μA
	$T_A = T_{MIN}$ to T_{MAX}			60	
Control Input	Leakage current			± 1	μA
	Threshold low		1.4	0.8	V
	Threshold high	2.4	1.4		

IC CHARACTERISTICS

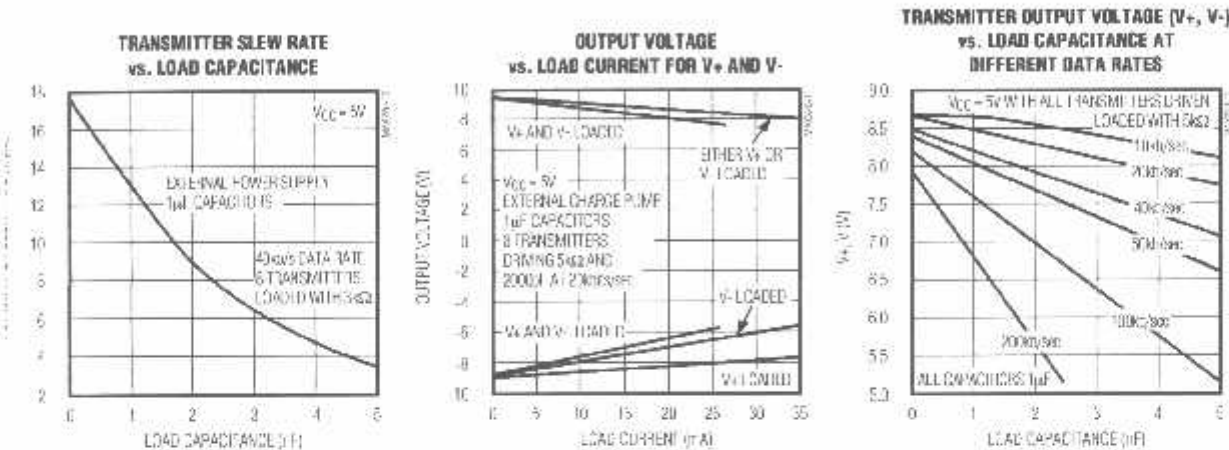
Transition Slow Rate	$C_L = 50pF$ to $2500pF$, $R_L = 3k\Omega$ to $7k\Omega$, $V_{CC} = 5V$, $T_A = +25^\circ C$, measured from +3V to -3V or -2V to +3V		5	10	30	V/ μs
Transmitter Propagation Delay (TL) to RS-232 (Normal Operation), Figure 1	t_{PHLT}		1.3	3.0		μs
			1.5	3.5		
Receiver Propagation Delay (TL) to RS-232 (Normal Operation), Figure 2	t_{PHLR}		0.6	1.5		μs
	t_{PLHR}		0.6	1.5		
Receiver Propagation Delay (TL) to RS-232 (Low-Power Mode), Figure 2	t_{PHLS}		0.6	10		μs
	t_{PLHS}		3.0	10		
Transmitter + to - Propagation Delay Difference (Normal Operation)	$t_{PHLT} - t_{PLHT}$		350			ns
Receiver + to - Propagation Delay Difference (Normal Operation)	$t_{PHLR} - t_{PLHR}$		350			ns
Receiver-Output Enable Time, Figure 3	t_{EH}		100	500		ns
Receiver-Output Disable Time, Figure 3	t_{DH}		100	500		ns
Transmitter Enable Time	t_{EH}	MAX246-MAX249 (excludes charge-pump startup)	5			μs
		MAX225/MAX245-MAX249 (includes charge-pump startup)	10			ms
Transmitter Disable Time, Figure 4	t_{DH}		100			ns

Note 5: The 300 Ω minimum specification complies with EIA/TIA-232E, but the actual resistance when in shutdown mode or $V_{CC} = 0V$ is 10M Ω as is implied by the leakage specification.

**±5V-Powered, Multichannel RS-232
Drivers/Receivers**

Typical Operating Characteristics

MAX225/MAX244–MAX249



+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220-MAX249

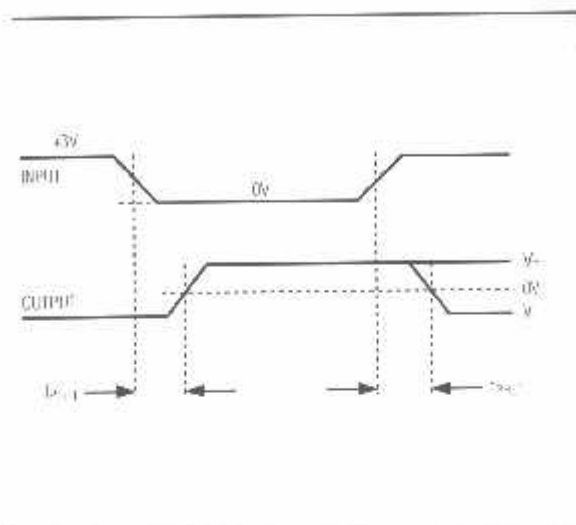


Figure 1 Transmitter Propagation-Delay Timing

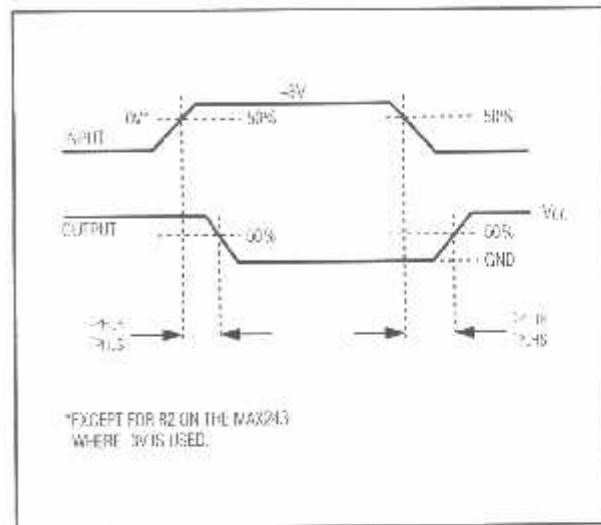


Figure 2 Receiver Propagation-Delay Timing

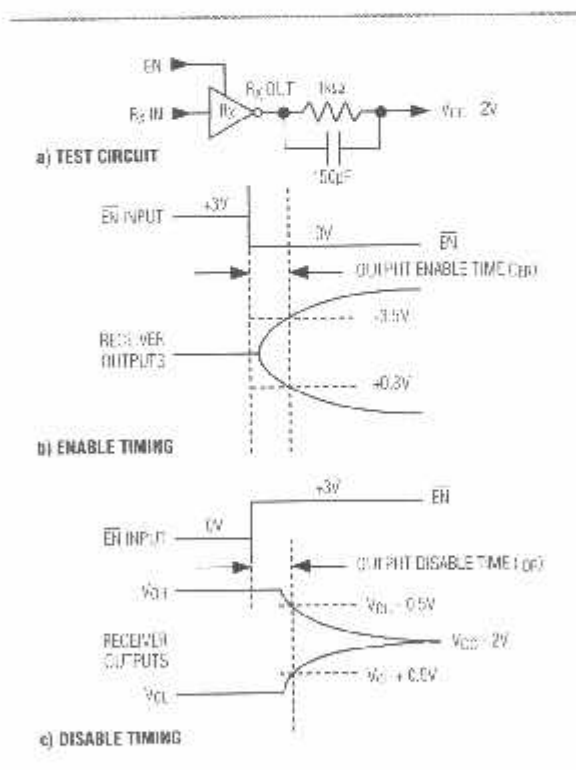


Figure 3 Receiver-Output Enable and Disable Timing

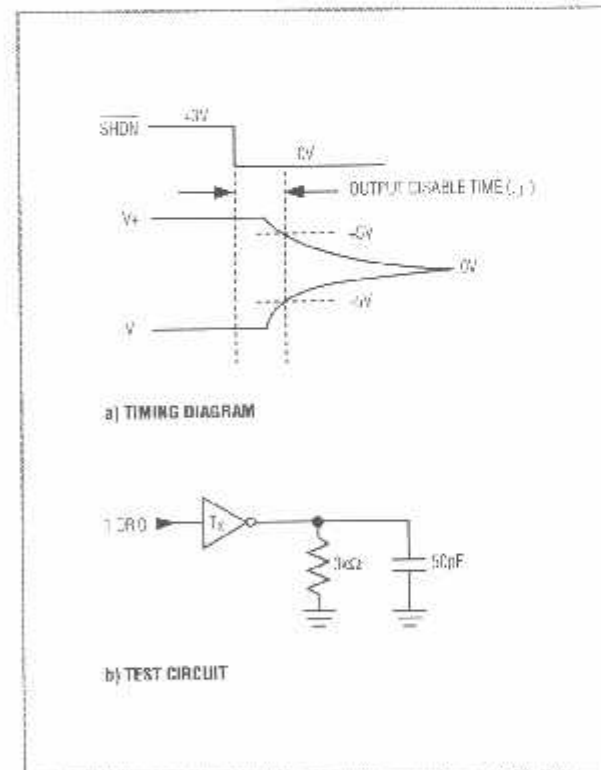


Figure 4 Transmitter-Output Disable Timing

5V-Powered, Multichannel RS-232 Drivers/Receivers

Table 1a. MAX245 Control Pin Configurations

ENT	ENR	OPERATION STATUS	TRANSMITTERS	RECEIVERS
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All 3-State
1	0	Shutdown	All 3-State	All Low-Power Receive Mode
1	1	Shutdown	All 3-State	All 3-State

Table 1b. MAX245 Control Pin Configurations

ENT	ENR	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1-TA4	TB1-TB4	RA1-RA5	RB1-RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All Active	RA1-RA4 3-State, RA5 Active	RB1-RB4 3-State, RB5 Active
1	0	Shutdown	All 3-State	All 3-State	All Low-Power Receive Mode	All Low-Power Receive Mode
1	1	Shutdown	All 3-State	All 3-State	RA1-RA4 3-State, RA5 Low-Power Receive Mode	RB1-RB4 3-State, RB5 Low-Power Receive Mode

Table 1c. MAX246 Control Pin Configurations

ENA	ENB	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1-TA4	TB1-TB4	RA1-RA5	RB1-RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All 3-State	All Active	RB1-RB4 3-State, RB5 Active
1	0	Shutdown	All 3-State	All Active	RA1-RA4 3-State, RA5 Active	All Active
1	1	Shutdown	All 3-State	All 3-State	RA1-RA4 3-State, RA5 Low-Power Receive Mode	RB1-RB4 3-State, RB5 Low-Power Receive Mode

+5V-Powered, Multichannel RS-232 Drivers/Receivers

Table 1d. MAX247/MAX248/MAX249 Control Pin Configurations

VTA	ENTB	ENRA	ENRB	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
					MAX247	TA1-TA4	TB1-TB4	RA1-RA4
					MAX248	TA1-TA4	TB1-TB4	RA1-RA4
					MAX249	TA1-TA3	TB1-TB3	RA1-RA5
0	0	0	0	Normal Operation		All Active	All Active	All Active
0	0	0	1	Normal Operation		All Active	All Active	All 3-State, except RB5 stays active on MAX247
0	0	1	0	Normal Operation		All Active	All Active	All 3-State
0	0	1	1	Normal Operation		All Active	All Active	All 3-State, except RB5 stays active on MAX247
0	1	0	0	Normal Operation		All Active	All 3-State	All Active
0	1	0	1	Normal Operation		All Active	All 3-State	All 3-State, except RB5 stays active on MAX247
0	1	1	0	Normal Operation		All Active	All 3-State	All 3-State
0	1	1	1	Normal Operation		All Active	All 3-State	All 3-State, except RB5 stays active on MAX247
1	0	0	0	Normal Operation		All 3-State	All Active	All Active
1	0	0	1	Normal Operation		All 3-State	All Active	All 3-State, except RB5 stays active on MAX247
1	0	1	0	Normal Operation		All 3-State	All Active	All 3-State
1	0	1	1	Normal Operation		All 3-State	All Active	All 3-State, except RB5 stays active on MAX247
1	1	0	0	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode
1	1	0	1	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode, All 3-State, except RB5 stays active on MAX247
1	1	1	0	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode
1	1	1	1	Shutdown		All 3-State	All 3-State	All 3-State, except RB5 stays active on MAX247

MAX220-MAX249

5V-Powered, Multichannel RS-232 Drivers/Receivers

Detailed Description

The MAX220-MAX249 contain four sections: dual charge-pump DC-DC voltage converters, RS-232 drivers, RS-232 receivers, and receiver and transmitter enable control inputs.

Dual Charge-Pump Voltage Converter

The MAX220-MAX249 have two internal charge pumps that convert +5V to $\pm 10V$ (unloaded) for RS-232 driver operation. The first converter uses capacitor C1 to double the +5V input to +10V on C3 at the V+ output. The second converter uses capacitor C2 to invert +10V to -10V on C4 at the V- output.

A small amount of power may be drawn from the +10V (V+) and -10V (V-) outputs to power external circuitry (see the Typical Operating Characteristics section). Except on the MAX225 and MAX245-MAX247, where these pins are not available, V+ and V- are not regulated; the output voltage drops with increasing load current. Not loaded, V+ and V- is a point that violates the minimum $\pm 5V$ EIA/TIA-232E driver output voltage when loading current from V+ and V- to external circuitry.

When using the shutdown feature on the MAX222, MAX225, MAX230, MAX235, MAX236, MAX240, MAX241, and MAX245-MAX249, avoid using V+ and V- to power external circuitry. When these parts are shutdown, V+ falls to 0V, and V- falls to +5V. For applications where a +10V external supply is applied to the V+ (instead of using the internal charge pump to generate +10V), the C1 capacitor must not be installed and SHDN pin must be tied to VCC. This is because V+ is internally connected to VCC in shutdown mode.

RS-232 Drivers

A typical driver output voltage swing is $\pm 8V$ when loaded with a nominal 5k Ω RS-232 receiver and VCC = V+. Output swing is guaranteed to meet the EIA/TIA-232 and V.28 specification, which calls for $\pm 5V$ minimum driver output levels under worst-case conditions. These include a minimum 3k Ω load, VCC = +4.5V, and maximum operating temperature. Unloaded driver output voltage ranges from (V+ -1.3V) to (V- +0.5V).

Input thresholds are both TTL and CMOS compatible; i.e., inputs of unused drivers can be left unconnected (or 40k Ω input pull-up resistors to VCC are built in except for the MAX220). The pull-up resistors force the inputs of unused drivers low because all drivers invert. External input pull-up resistors typically source 12 μA (except in shutdown mode where the pull-ups are disabled). Driver outputs turn off and enter a high-impedance state—where leakage current is typically transpires (maximum 25 μA)—when in shutdown

mode. In three-state mode, or when power is removed, outputs can be driven to $\pm 15V$. The power-supply current typically drops to 5 μA in shutdown mode. The MAX220 does not have pull-up resistors to force the outputs of the unused drivers low. Connect unused inputs to GND or VCC.

The MAX239 has a receiver three-state control line, and the MAX223, MAX225, MAX235, MAX236, MAX240, and MAX241 have both a receiver three-state control line and a low-power shutdown control. Table 2 shows the effects of the shutdown control and receiver three-state control on the receiver outputs.

The receiver TTL/CMOS outputs are in a high-impedance, three-state mode whenever the three-state enable line is high (or the MAX225/MAX235/MAX236/MAX239/MAX241), and are also high-impedance whenever the shutdown control line is high.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1 μA with the driver output pulled to ground. The driver output leakage remains less than 1 μA , even if the transmitter output is backdriven between 0V and (VCC + 6V). Below -0.5V, the transmitter is diode clamped to ground with 1k Ω series impedance. The transmitter is also zero-clamped to approximately VCC + 6V, with a series impedance of 1k Ω .

The driver output slew rate is limited to less than 30V/ μs as required by the EIA/TIA-232E and V.28 specifications. Typical slew rates are 24V/ μs unloaded and 10V/ μs loaded with 30pF and 2500pF.

RS-232 Receivers

EIA/TIA-232E and V.28 specifications define a voltage level greater than 3V as a logic 0, so all receivers invert. Input thresholds are set at 0.8V and 2.4V, so receivers respond to TTL level inputs as well as EIA/TIA-232E and V.28 levels.

The receiver inputs withstand an input overvoltage up to +25V and provide input terminating resistors with

Table 2. Three-State Control of Receivers

PART	SHDN	SHDN	EN	EN(R)	RECEIVERS
MAX225	—	Low High High	X Low High	—	High Impedance Active High Impedance
MAX226	—	—	—	Low High	High Impedance Active
MAX235 MAX236 MAX240	Low Low High	—	—	Low High X	High Impedance Active High Impedance

MAXIM

+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220-MAX249

ninal 5k Ω values. The receivers implement Type 1 interpretation of the fault conditions of V.28 and V.232E.

Each receiver input hysteresis is typically 0.5V with a guaranteed minimum of 0.2V. This produces clear output transitions with slow-moving input signals, even in moderate amounts of noise and ringing. The receiver propagation delay is typically 600ns and is independent of input swing direction.

Low-Power Receive Mode

A low-power receive-mode feature of the MAX223, MAX242, and MAX245-MAX249 puts the IC into shutdown mode but still allows it to receive information. This is important for applications where systems are periodically awakened to look for activity. Using low-power receive mode, the system can still receive a signal that activates it on command and prepare it for communication at faster data rates. This operation conserves system power.

Negative Threshold—MAX243

The MAX243 is pin compatible with the MAX232A, differing only in that RS-232 cable fault protection is removed on one of the two receiver inputs. This means that controls such as CTS and RTS can either be driven or floating without interrupting communication. Different pins are not needed to interface with different pieces of equipment.

The input threshold of the receiver without cable fault protection is -0.8V rather than +1.4V. Its output goes sensitive only if the input is connected to a control line that is actively driven negative. If not driven, it defaults to the 0 or "OK to send" state. Normally, the MAX243's low receiver (-1.4V threshold) is used for the data line (D or RD), while the negative threshold receiver is connected to the control line (DTR, DTS, CTS, RTS, etc.).

Other members of the RS-232 family implement the optional cable fault protection as specified by EIA/TIA-232E specifications. This means a receiver output goes high whenever its input is driven negative, left floating, or shorted to ground. The high output tells the serial communications IC to stop sending data. To avoid this, the control lines must either be driven or connected to jumpers to an appropriate positive voltage level.

Shutdown—MAX222-MAX242

On the MAX222, MAX235, MAX236, MAX240, and MAX241, all receivers are disabled during shutdown. On the MAX223 and MAX242, two receivers continue to operate in a reduced power mode when the chip is in shutdown. Under these conditions, the propagation delay increases to about 2.5 μ s for a high-to-low input transition. When in shutdown, the receiver acts as a CMOS inverter with no hysteresis. The MAX223 and MAX242 also have a receiver output enable input (EN for the MAX242 and EN for the MAX223) that allows receiver output control independent of SHDN (SHDN for MAX241). With all other devices, SHDN (SHDN for MAX241) also disables the receiver outputs.

The MAX225 provides five transmitters and five receivers, while the MAX245 provides ten receivers and eight transmitters. Both devices have separate receiver and transmitter-enable controls. The charge pumps turn off and the devices shut down when a logic high is applied to the ENT input. In this state, the supply current drops to less than 25 μ A and the receivers continue to operate in a low-power receive mode. Driver outputs enter a high-impedance state (three-state mode). On the MAX225, all five receivers are controlled by the ENR input. On the MAX245, eight of the receiver outputs are controlled by the ENR input, while the remaining two receivers (RA5 and RB5) are always active. RA1-RA4 and RB1-RB4 are put in a three-state mode when ENR is a logic high.

Receiver and Transmitter Enable Control Inputs

The MAX225 and MAX245-MAX249 feature transmitter and receiver enable controls.

The receivers have three modes of operation: full-speed receive (normal active), three-state (disabled), and low-power receive (enabled receivers continue to function at lower data rates). The receiver enable inputs control the full-speed receive and three-state modes. The transmitters have two modes of operation: full-speed transmit (normal active) and three-state (disabled). The transmitter enable inputs also control the shutdown mode. The device enters shutdown mode when all transmitters are disabled. Enabled receivers function in the low-power receive mode when in shutdown.

1.5V-Powered, Multichannel RS-232 Drivers/Receivers

Tables 1a–1d define the control states. The MAX244 has no control pins and is not included in these tables.

The MAX246 has ten receivers and eight drivers with two control pins, each controlling one side of the device. A logic high at the A-side control input ($\overline{\text{ENA}}$) causes the four A-side receivers and drivers to go into three-state mode. Similarly, the B-side control input ($\overline{\text{ENB}}$) causes the four B-side drivers and receivers to go into a three-state mode. As in the MAX245, one A-side and one B-side receiver (RA5 and RB5) remain active at all times. The entire device is put into shutdown mode when both the A and B sides are disabled ($\overline{\text{ENA}} = \overline{\text{ENB}} = 1.5\text{V}$).

The MAX247 provides nine receivers and eight drivers with four control pins. The $\overline{\text{ENRA}}$ and $\overline{\text{ENRB}}$ receiver enable inputs each control four receiver outputs. The $\overline{\text{ENTA}}$ and $\overline{\text{ENTB}}$ transmitter enable inputs each control four drivers. The ninth receiver (RB5) is always active. The device enters shutdown mode with a logic high on both $\overline{\text{ENTA}}$ and $\overline{\text{ENTB}}$.

The MAX248 provides eight receivers and eight drivers with four control pins. The $\overline{\text{ENRA}}$ and $\overline{\text{ENRB}}$ receiver enable inputs each control four receiver outputs. The $\overline{\text{ENTA}}$ and $\overline{\text{ENTB}}$ transmitter enable inputs control four drivers each. This part does not have an always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{\text{ENTA}}$ and $\overline{\text{ENTB}}$.

The MAX249 provides ten receivers and six drivers with four control pins. The $\overline{\text{ENRA}}$ and $\overline{\text{ENRB}}$ receiver enable inputs each control five receiver outputs. The $\overline{\text{ENTA}}$ and $\overline{\text{ENTB}}$ transmitter enable inputs control three drivers each. There is no always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{\text{ENTA}}$ and $\overline{\text{ENTB}}$. In shutdown mode, active receivers operate in a low-power receive mode at data rates up to 20kbits/sec.

Applications Information

Figures 5 through 25 show pin configurations and typical operating circuits. In applications that are sensitive to power-supply noise, VCC should be decoupled to ground with a capacitor of the same value as C1 and C2 connected as close as possible to the device.

+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220-MAX249

TOP VIEW



DIP/SO

CAPACITANCE (pF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	4.7	4.7	10	10	4.7
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1

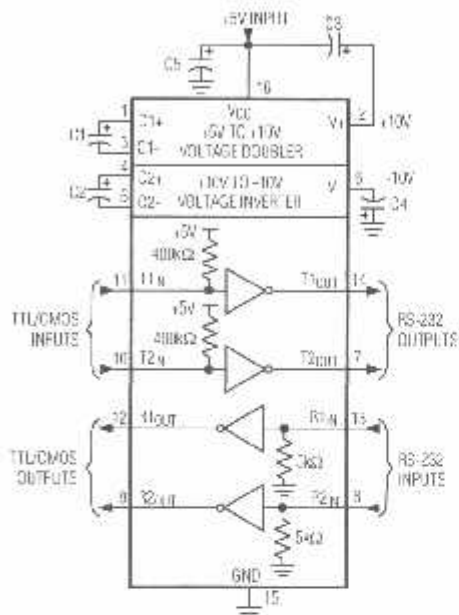
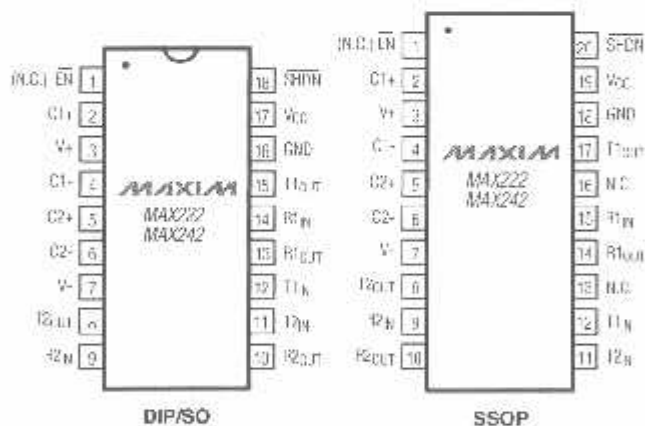


Figure 5. MAX220/MAX232/MAX232A Pin Configuration and Typical Operating Circuit

TOP VIEW



DIP/SO

SSOP

1. A IL FOR MAX222 ONLY.
PIN NUMBERS IN TYPICAL OPERATING CIRCUIT ARE FOR DIP/SO PACKAGES ONLY.

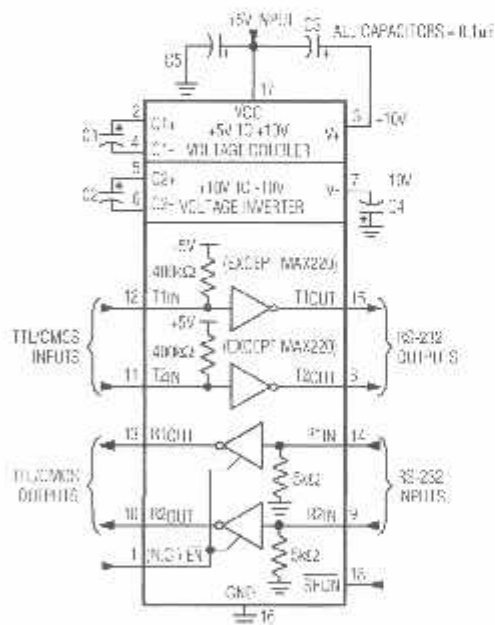
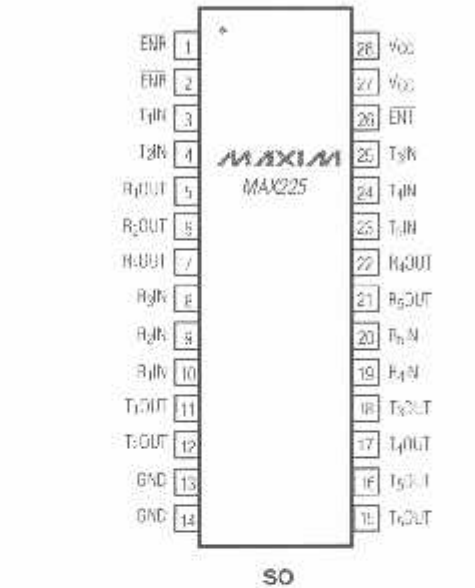


Figure 6. MAX222/MAX242 Pin Configurations and Typical Operating Circuit

-5V-Powered, Multichannel RS-232 Drivers/Receivers

TOP VIEW



MAX225 FUNCTIONAL DESCRIPTION

- 5 RECEIVERS
- 5 TRANSMITTERS
- 2 CONTROL PINS
 - 1 RECEIVER ENABLE (ENR)
 - 1 TRANSMITTER ENABLE (ENT)

PINS (ENR, GND, VCC, T6OUT) ARE INTERNALLY CONNECTED. CONNECT EITHER OR BOTH EXTERNALLY; T6OUT IS A SINGLE DRIVER.

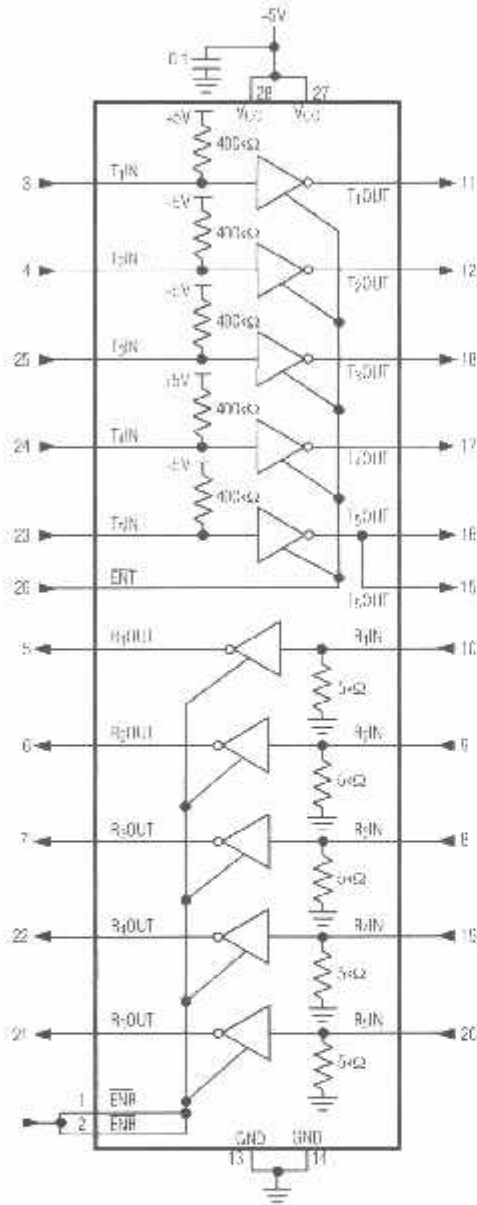
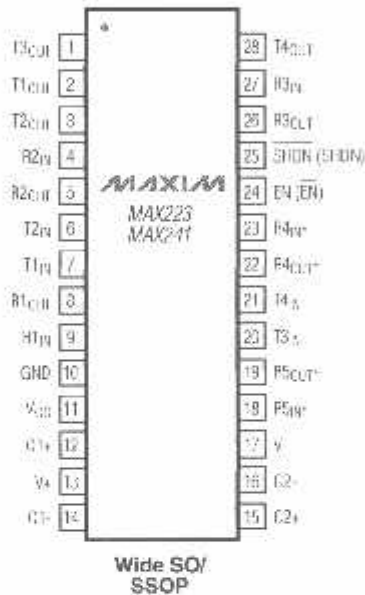


Figure 7. MAX225 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220-MAX249

TOP VIEW



*T4 AND R5 IN MAX223 REMAIN ACTIVE IN SHUTDOWN
NOTE: PIN LABELS IN () ARE FOR MAX241

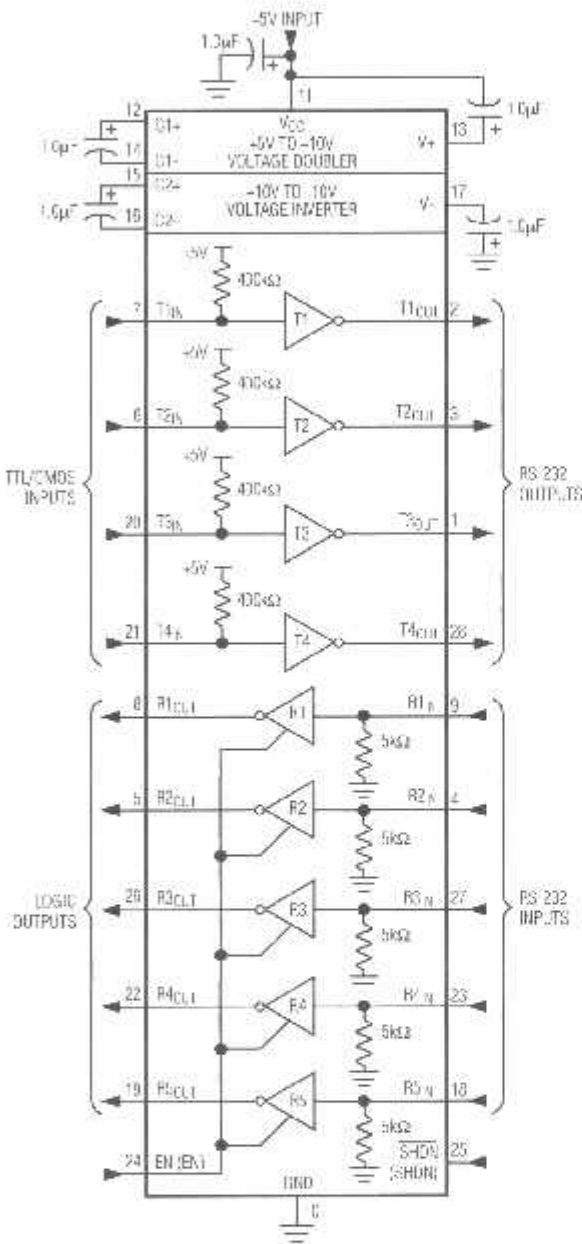


Figure 8. MAX223/MAX241 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multichannel RS-232 Drivers/Receivers

TOP VIEW



DIP/50

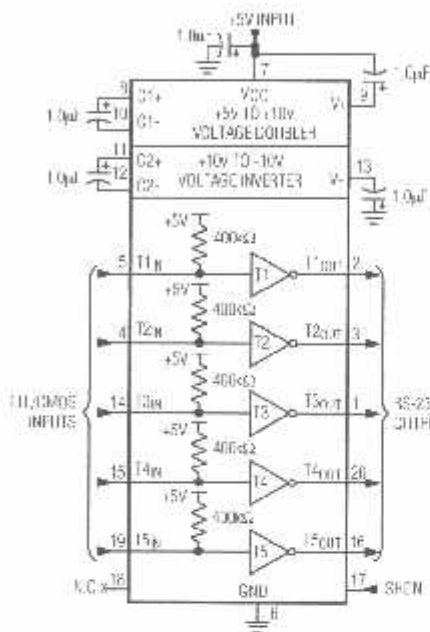
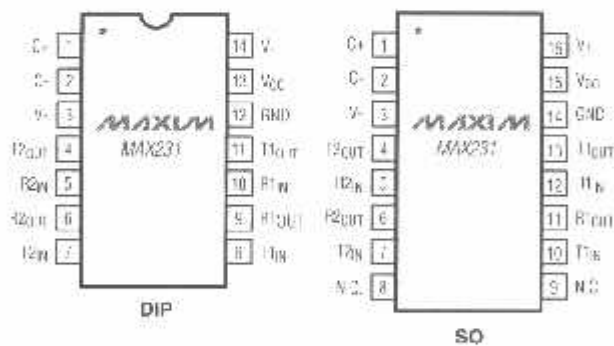


Figure 9. MAX236 Pin Configuration and Typical Operating Circuit

TOP VIEW



PIN NUMBERS IN PARETH ARE FOR SQ PACKAGE

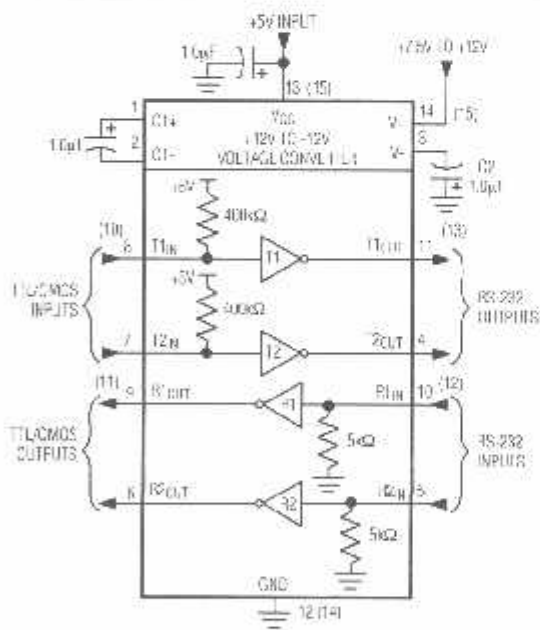
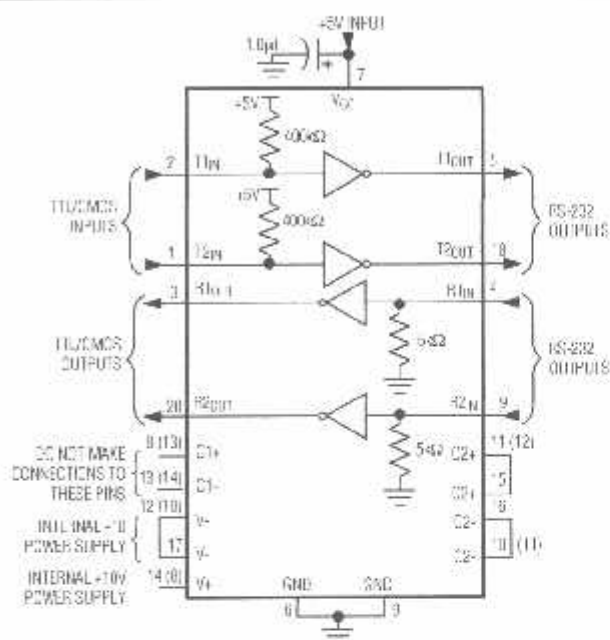


Figure 10. MAX231 Pin Configurations and Typical Operating Circuit

+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220-MAX249

TOP VIEW



(1) ARE FOR SO PACKAGE ONLY.

Figure 11. MAX233/MAX233A Pin Configuration and Typical Operating Circuit

TOP VIEW

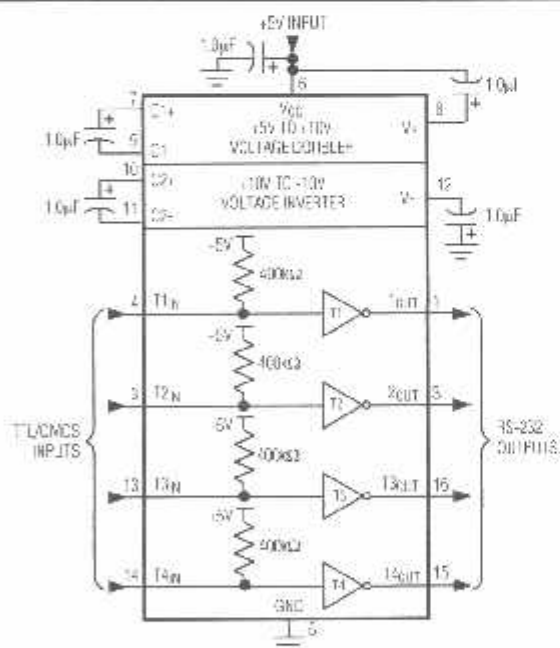
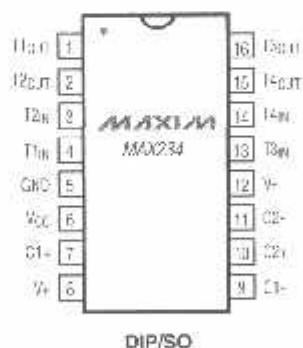


Figure 12. MAX234 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multichannel RS-232 Drivers/Receivers

TOP VIEW

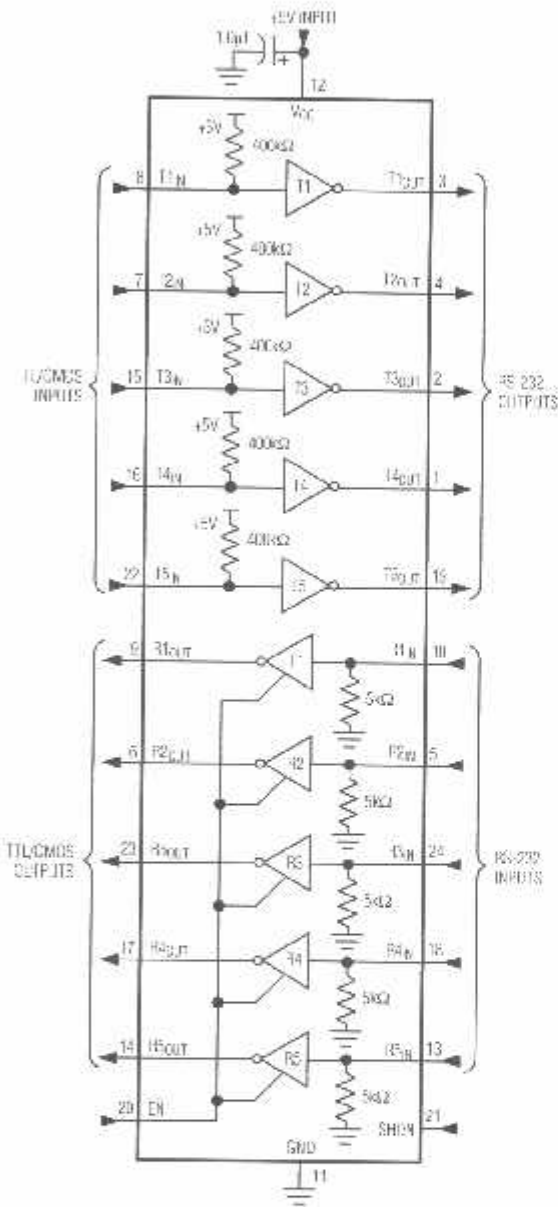


Figure 13. MAX235 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220-MAX249

TOP VIEW

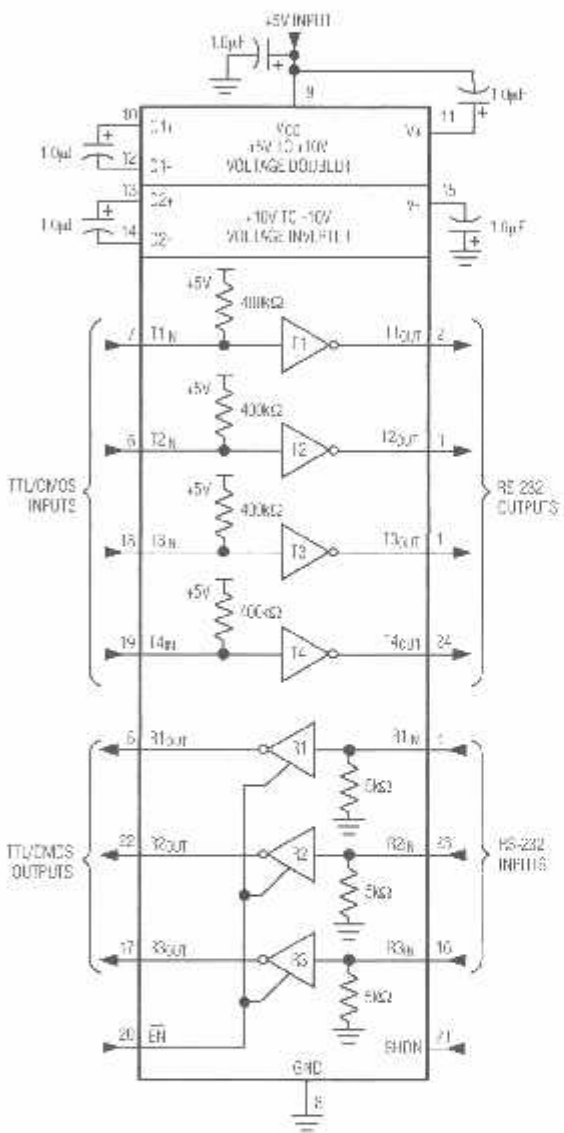


Figure 14. MAX236 Pin Configuration and Typical Operating Circuit

-5V-Powered, Multichannel RS-232 Drivers/Receivers

TOP VIEW

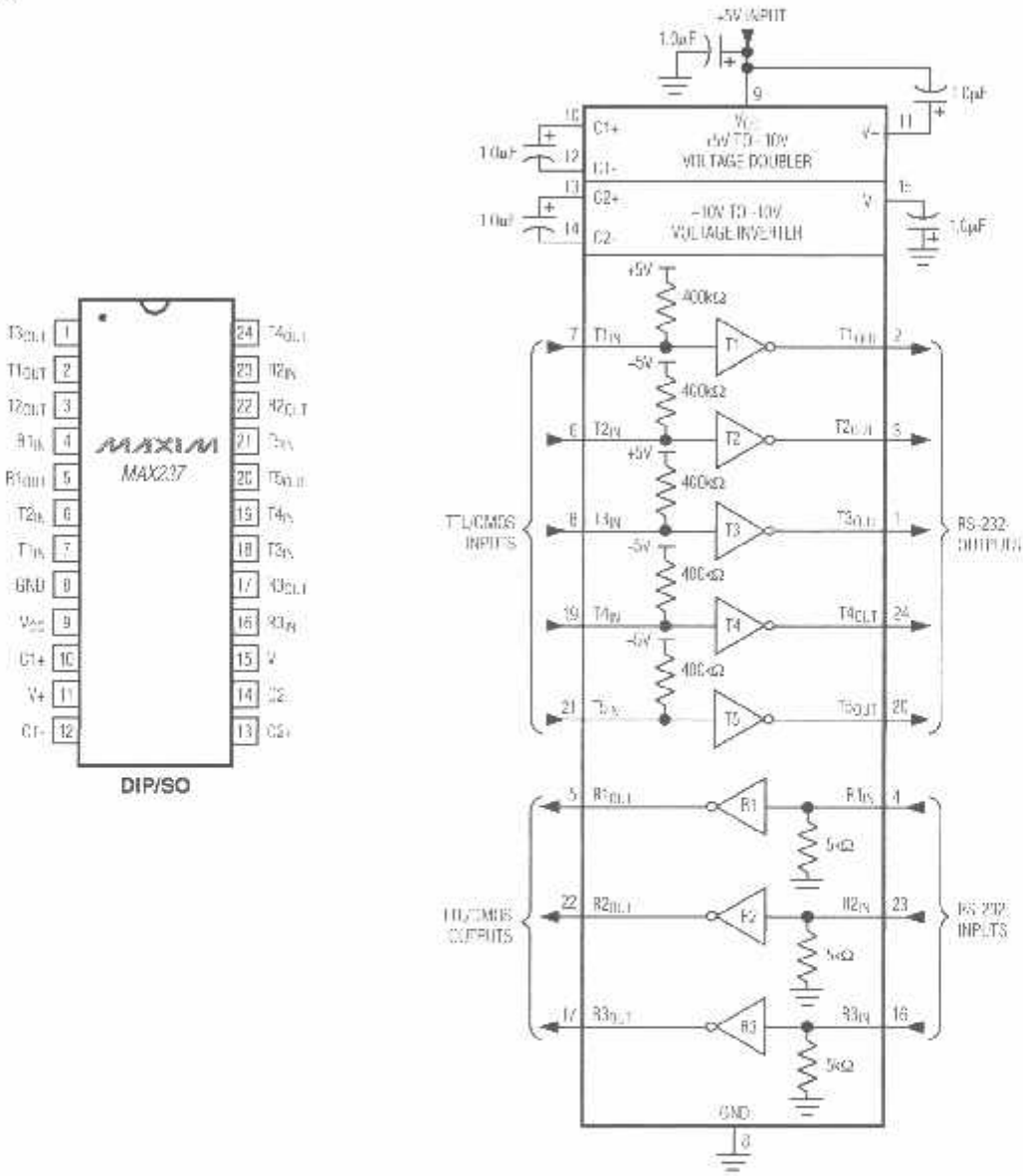


Figure 15. MAX232 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220-MAX249

TOP VIEW

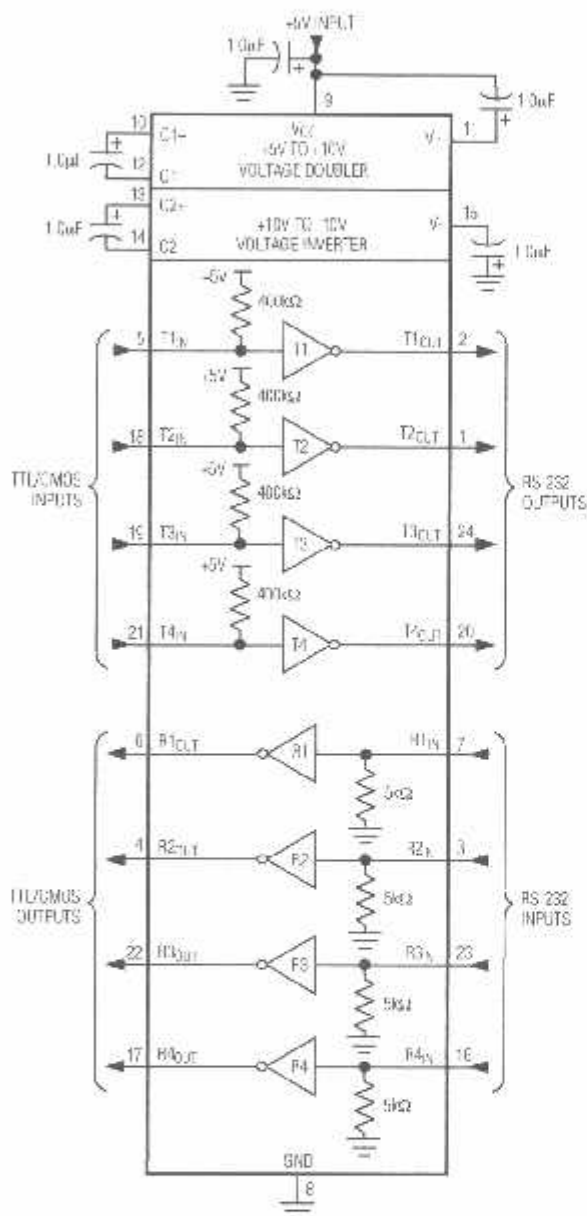
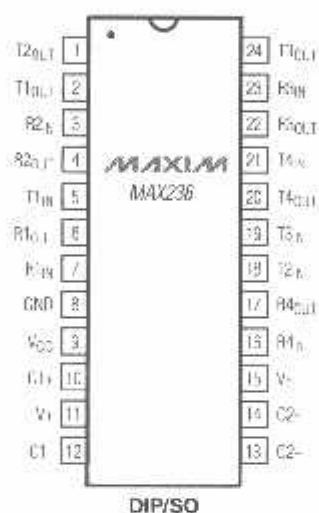
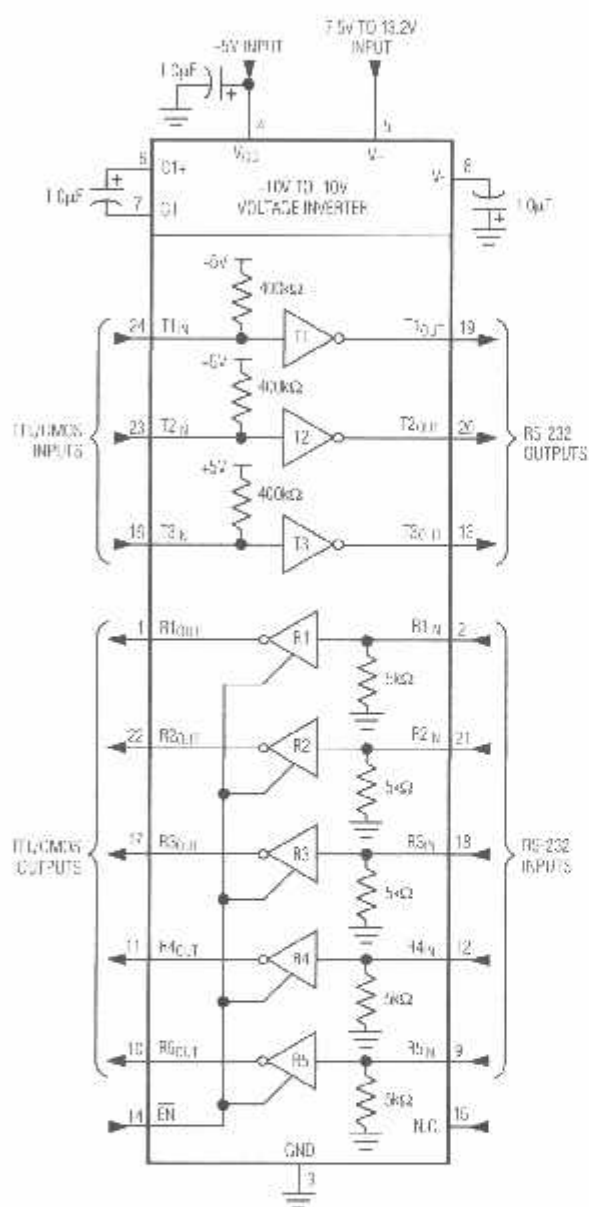
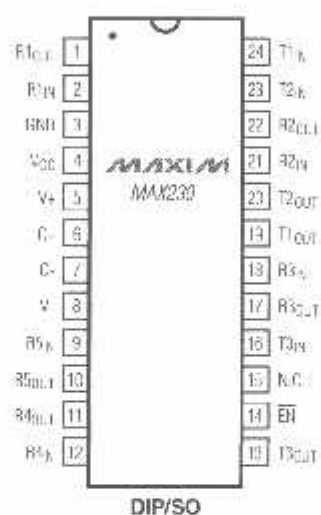


Figure 16: MAX238 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multichannel RS-232 Drivers/Receivers

TCP VIEW



+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220-MAX249

TOP VIEW

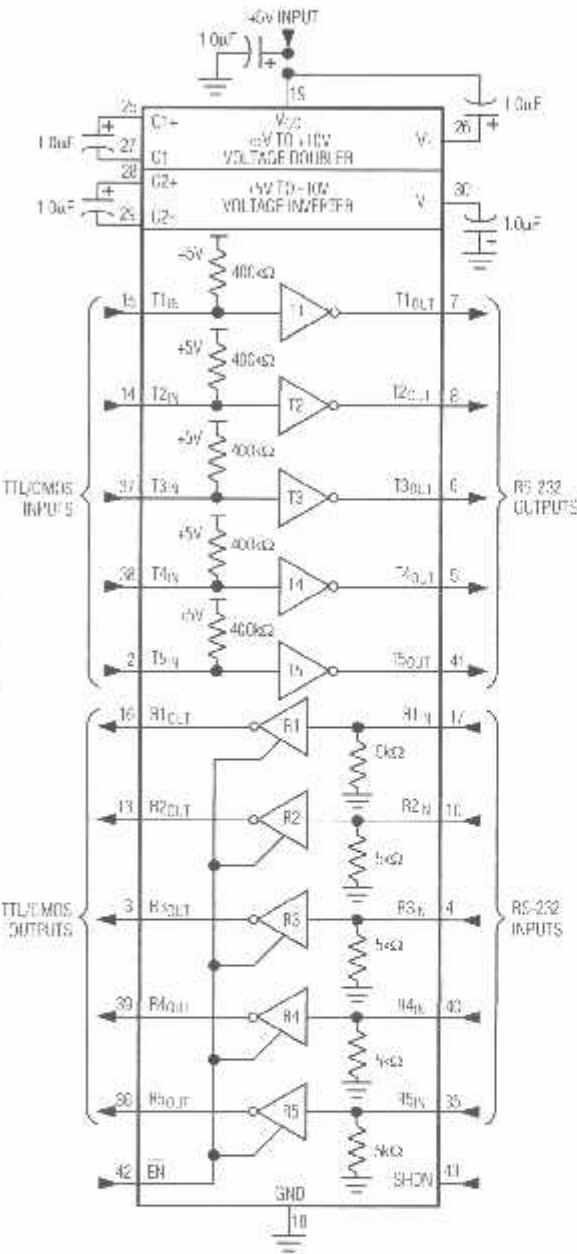
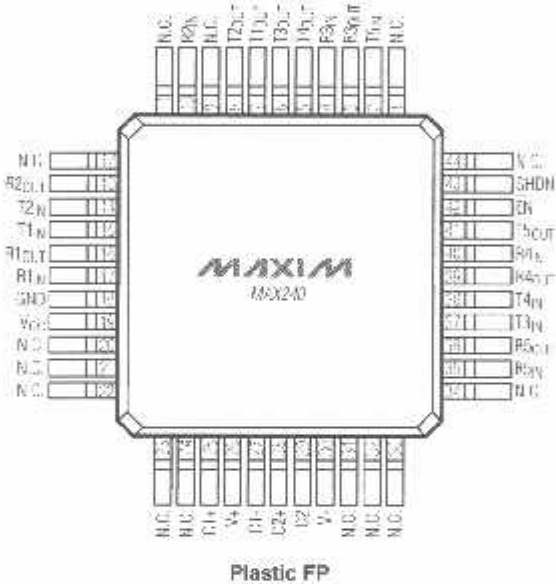


Figure 18. MAX240 Pin Configuration and Typical Operating Circuit

-5V-Powered, Multichannel RS-232 Drivers/Receivers

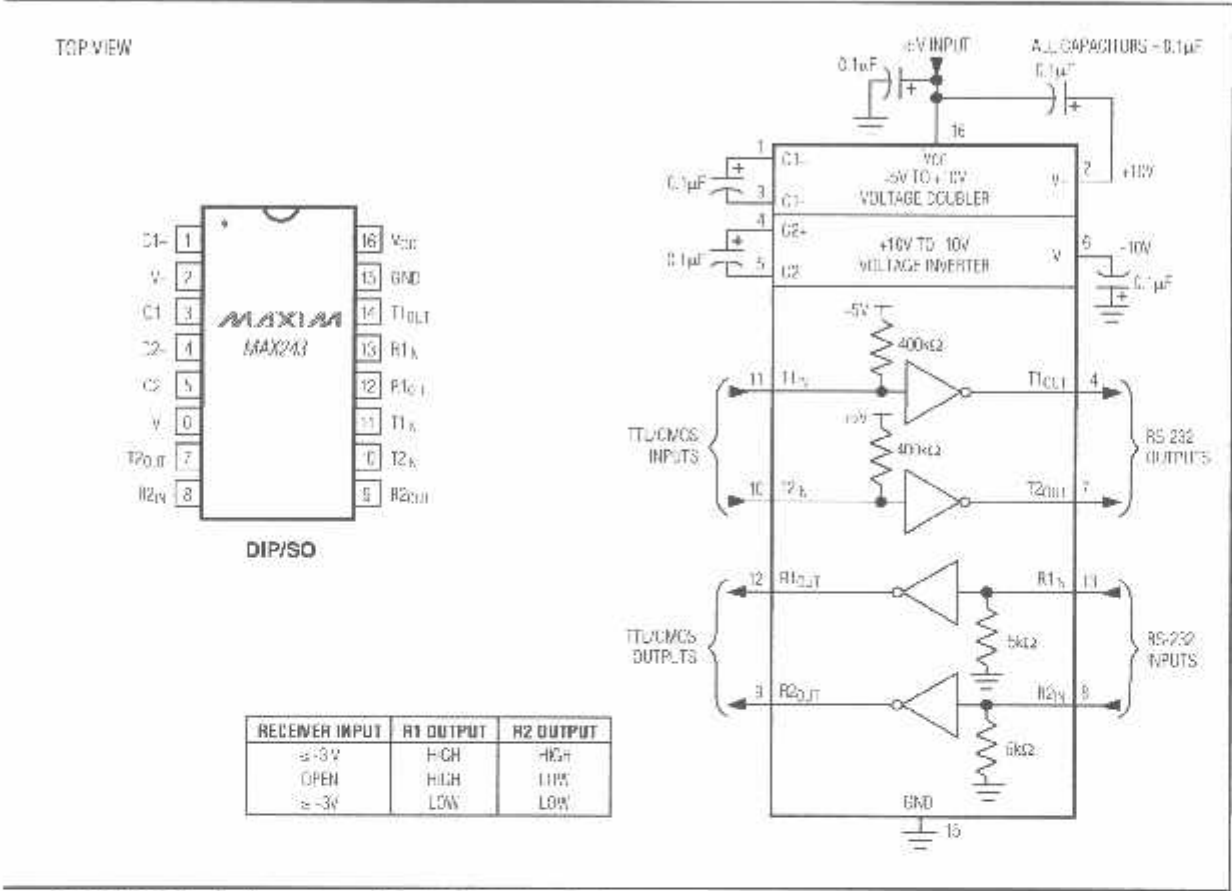
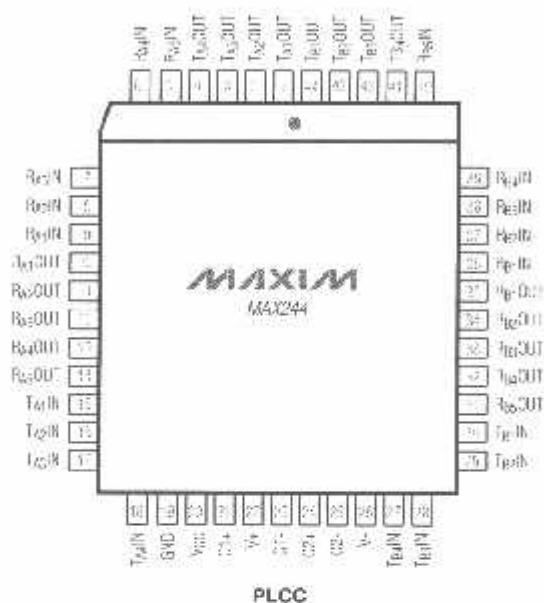


Figure 19. MAX243 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220-MAX249

TOP VIEW



MAX249 FUNCTIONAL DESCRIPTION

- 10 RECEIVERS
- 5 A-SIDE RECEIVER
- 5 B-SIDE RECEIVER
- 8 TRANSMITTERS
- 4 A-SIDE TRANSMITTERS
- 4 B-SIDE TRANSMITTERS
- NO CONTROL PINS

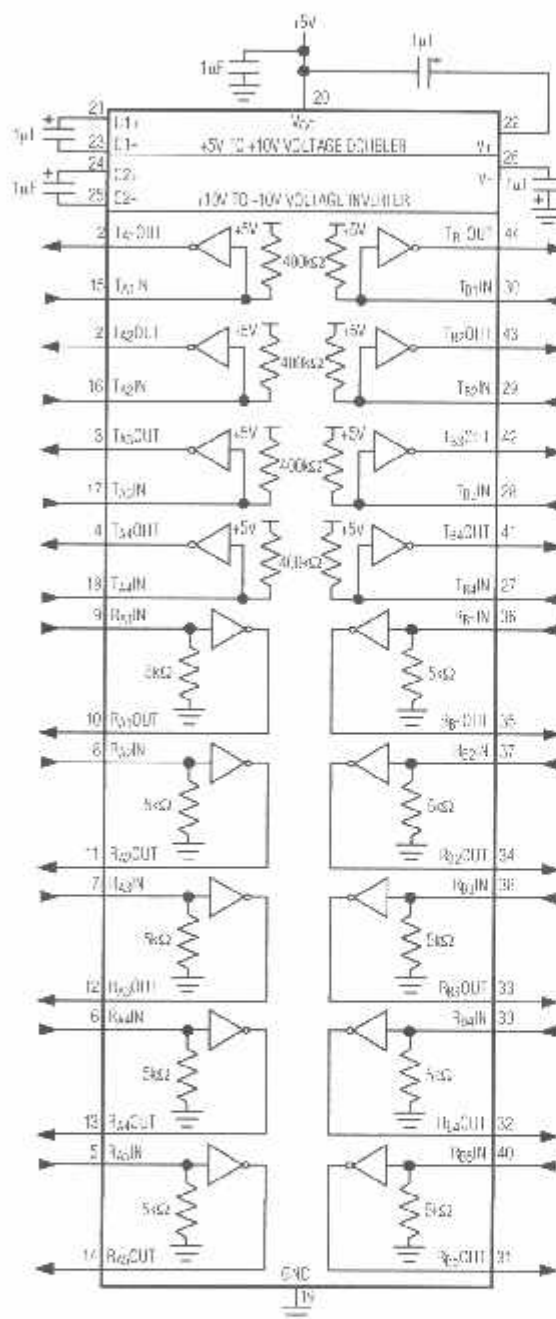


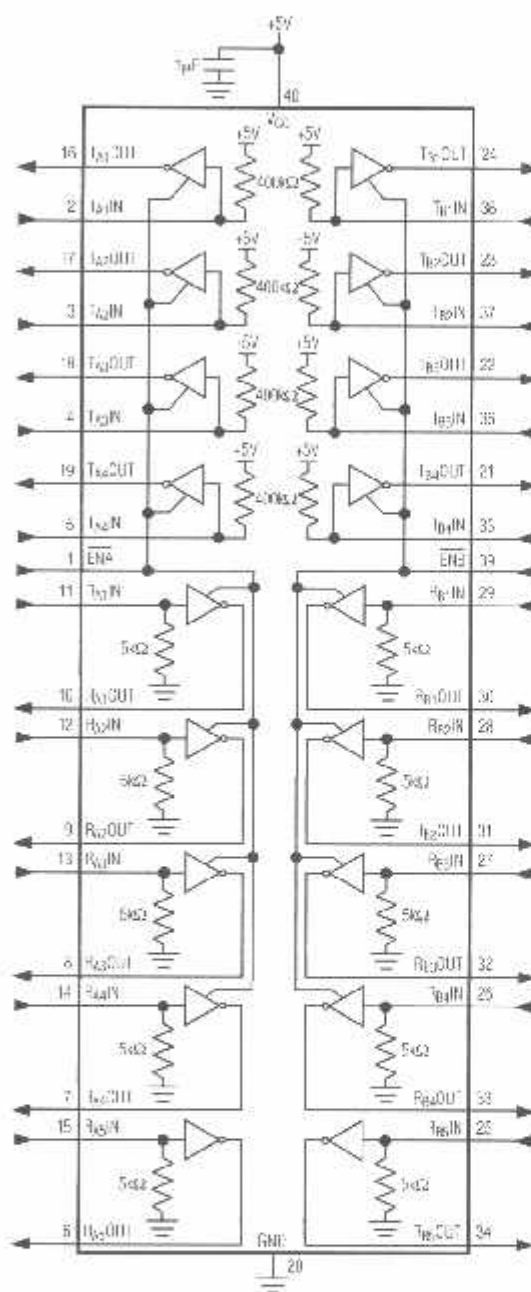
Figure 20. MAX244 Pin Configuration and Typical Operating Circuit

MAX220-MAX249

ENA	1		43	VDD
T ₀ IN	2		39	ENB
T ₀ IN	3		38	T ₀ IN
T ₀ IN	4		37	T ₀ IN
T ₀ IN	5		36	T ₀ IN
R ₀ OUT	6	MAXIM	35	T ₀ IN
R ₀ OUT	7	MAX246	34	R ₀ OUT
R ₀ OUT	8		33	R ₀ OUT
R ₀ OUT	9		32	R ₀ OUT
R ₀ OUT	10		31	R ₀ OUT
R ₀ IN	11		30	R ₀ OUT
R ₀ IN	12		29	R ₀ IN
R ₀ IN	13		28	R ₀ IN
R ₀ IN	14		27	R ₀ IN
R ₀ IN	15		26	R ₀ IN
T ₀ OUT	16		25	R ₀ IN
T ₀ OUT	17		24	T ₀ OUT
T ₀ OUT	18		23	T ₀ OUT
T ₀ OUT	19		22	T ₀ OUT
GND	20		21	T ₀ OUT

DIP

ENABLE A-SIDE (ENA)
ENABLE B-SIDE (ENB)



31

1.5V-Powered, Multichannel RS-232 Drivers/Receivers

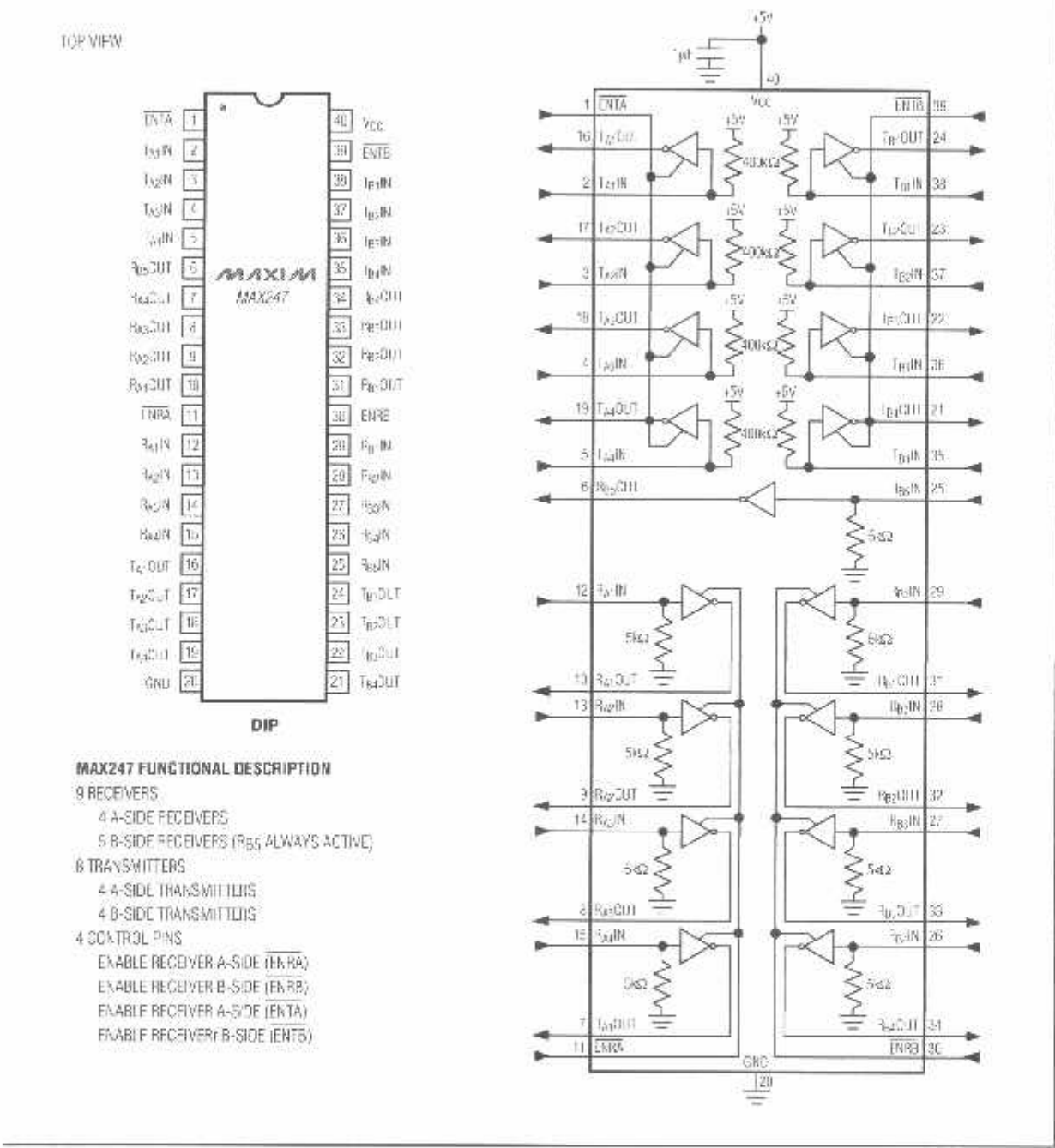
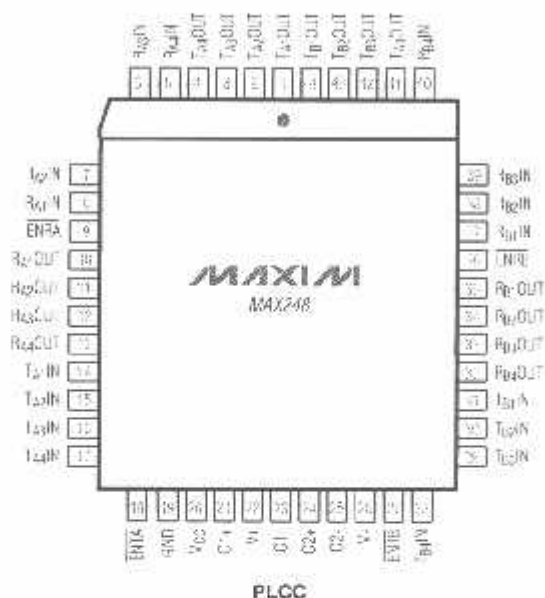


Figure 28. MAX247 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220-MAX249

TOP VIEW



MAX248 FUNCTIONAL DESCRIPTION

8 RECEIVERS

- 4 A-SIDE RECEIVERS
- 4 B-SIDE RECEIVERS

8 TRANSMITTERS

- 4 A-SIDE TRANSMITTERS
- 4 B-SIDE TRANSMITTERS

4 CONTROL PINS

- ENABLE RECEIVER A-SIDE (EN1A)
- ENABLE RECEIVER B-SIDE (EN1B)
- ENABLE RECEIVER A-SIDE (EN1A)
- ENABLE RECEIVER B-SIDE (EN1B)

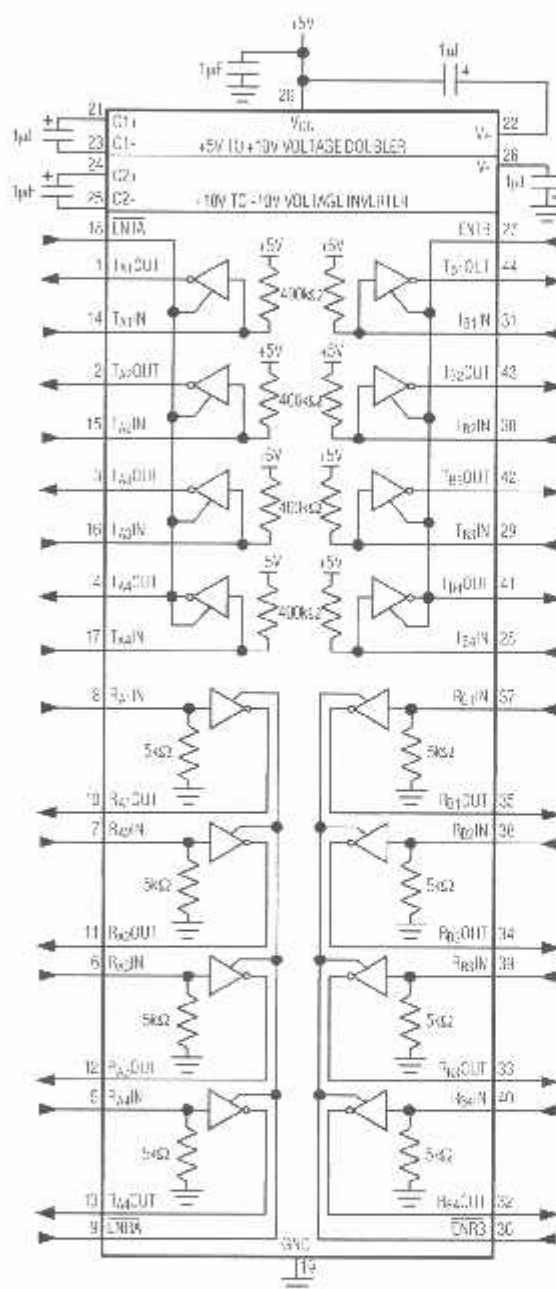
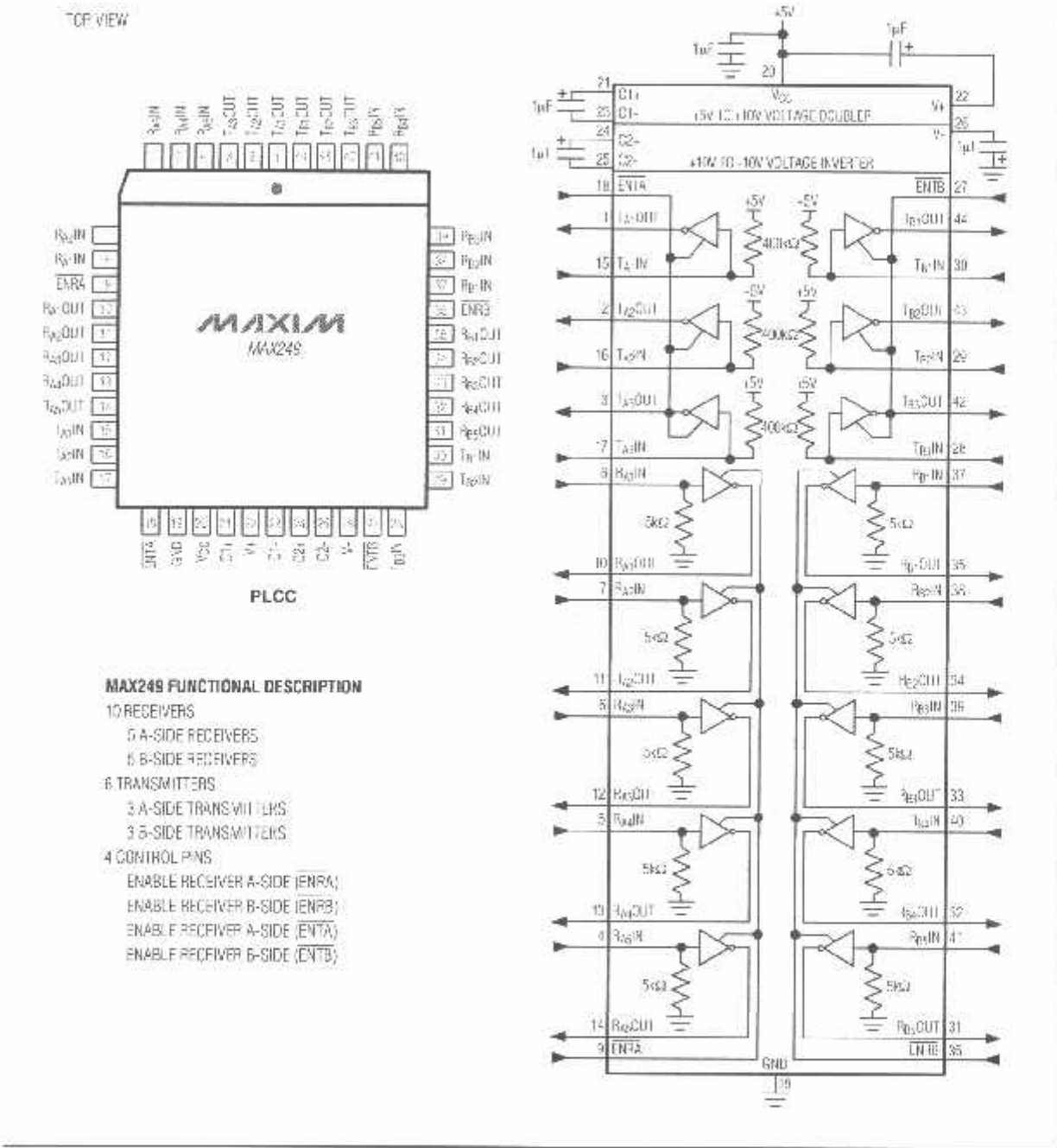


Figure 24. MAX248 Pin Configuration and Typical Operating Circuit

-5V-Powered, Multichannel RS-232 Drivers/Receivers



+5V-Powered, Multichannel RS-232 Drivers/Receivers

Ordering Information (continued)

MAX220-MAX249

PART	TEMP RANGE	PIN-PACKAGE
MAX222 CPN	0°C to +70°C	16 Plastic DIP
MAX222CWN	0°C to +70°C	16 Wide SO
MAX222C/D	0°C to +70°C	Dice*
MAX222EPN	-40°C to +85°C	16 Plastic DIP
MAX222EWN	-40°C to +85°C	16 Wide SO
MAX222EJN	-40°C to +85°C	16 CERDIP
MAX222MJN	-55°C to +125°C	16 CERDIP
MAX223 CAI	0°C to +70°C	28 SSOP
MAX223CWI	0°C to +70°C	28 Wide SO
MAX223C/D	0°C to +70°C	Dice*
MAX223EAI	-40°C to +85°C	28 SSOP
MAX223EWI	-40°C to +85°C	28 Wide SO
MAX225 CWI	0°C to +70°C	28 Wide SO
MAX225EWI	-40°C to +85°C	28 Wide SO
MAX230 CPP	0°C to +70°C	20 Plastic DIP
MAX230CWP	0°C to +70°C	20 Wide SO
MAX230C/D	0°C to +70°C	Dice*
MAX230EPP	-40°C to +85°C	20 Plastic DIP
MAX230EWP	-40°C to +85°C	20 Wide SO
MAX230EJP	-40°C to +85°C	20 CERDIP
MAX230MJP	-55°C to +125°C	20 CERDIP
MAX231 CPD	0°C to +70°C	14 Plastic DIP
MAX231CWE	0°C to +70°C	16 Wide SO
MAX231CJD	0°C to +70°C	14 CERDIP
MAX231C/D	0°C to +70°C	Dice*
MAX231EPD	-40°C to +85°C	14 Plastic DIP
MAX231EWE	-40°C to +85°C	16 Wide SO
MAX231EJD	-40°C to +85°C	14 CERDIP
MAX231MJD	-55°C to +125°C	14 CERDIP
MAX232 CPE	0°C to +70°C	16 Plastic DIP
MAX232CSF	0°C to +70°C	16 Narrow SO
MAX232CWF	0°C to +70°C	16 Wide SO
MAX232C/D	0°C to +70°C	Dice*
MAX232FPF	-40°C to +85°C	16 Plastic DIP
MAX232FSF	-40°C to +85°C	16 Narrow SO
MAX232FWF	-40°C to +85°C	16 Wide SO
MAX232FJF	-40°C to +85°C	16 CERDIP
MAX232MJF	-55°C to +125°C	16 CERDIP
MAX232MJP	-55°C to +125°C	20 LCC
MAX232A CPE	0°C to +70°C	16 Plastic DIP
MAX232ACSE	0°C to +70°C	16 Narrow SO
MAX232ACWE	0°C to +70°C	16 Wide SO

PART	TEMP RANGE	PIN-PACKAGE
MAX232AC/D	0°C to +70°C	Dice*
MAX232AEPE	-40°C to +85°C	16 Plastic DIP
MAX232AESE	-40°C to +85°C	16 Narrow SO
MAX232AEWE	-40°C to +85°C	16 Wide SO
MAX232AEJE	-40°C to +85°C	16 CERDIP
MAX232AMJE	-55°C to +125°C	16 CERDIP
MAX232AMLH	-55°C to +125°C	20 LCC
MAX233 CPP	0°C to +70°C	20 Plastic DIP
MAX233EPP	-40°C to +85°C	20 Plastic DIP
MAX233A CPP	0°C to +70°C	20 Plastic DIP
MAX233ACWP	0°C to +70°C	20 Wide SO
MAX233AEJP	-40°C to +85°C	20 Plastic DIP
MAX233AEWP	-40°C to +85°C	20 Wide SO
MAX234 CPE	0°C to +70°C	16 Plastic DIP
MAX234CWE	0°C to +70°C	16 Wide SO
MAX234C/D	0°C to +70°C	Dice*
MAX234EPE	-40°C to +85°C	16 Plastic DIP
MAX234EWE	-40°C to +85°C	16 Wide SO
MAX234EJE	-40°C to +85°C	16 CERDIP
MAX234MJE	-55°C to +125°C	16 CERDIP
MAX235 CPG	0°C to +70°C	24 Wide Plastic DIP
MAX235EPG	-40°C to +85°C	24 Wide Plastic DIP
MAX235EDG	-40°C to +85°C	24 Ceramic SS
MAX235MDG	-55°C to +125°C	24 Ceramic SS
MAX236 CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX236CWG	0°C to +70°C	24 Wide SO
MAX236C/D	0°C to +70°C	Dice*
MAX236ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX236EWG	-40°C to +85°C	24 Wide SO
MAX236ERG	-40°C to +85°C	24 Narrow CERDIP
MAX236MRG	-55°C to +125°C	24 Narrow CERDIP
MAX237 CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX237CWG	0°C to +70°C	24 Wide SO
MAX237C/D	0°C to +70°C	Dice*
MAX237ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX237EWG	-40°C to +85°C	24 Wide SO
MAX237ERG	-40°C to +85°C	24 Narrow CERDIP
MAX237MRG	-55°C to +125°C	24 Narrow CERDIP
MAX238 CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX238CWG	0°C to +70°C	24 Wide SO
MAX238C/D	0°C to +70°C	Dice*
MAX238ENG	-40°C to +85°C	24 Narrow Plastic DIP

* Contact factory for dice specifications.

-5V-Powered, Multichannel RS-232 Drivers/Receivers

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX238EWG	-40°C to +85°C	24 Wide SO
MAX238ERG	-40°C to +85°C	24 Narrow CERDIP
MAX238MRG	-55°C to +125°C	24 Narrow CERDIP
MAX239CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX239CWG	0°C to +70°C	24 Wide SO
MAX239C/D	0°C to +70°C	Dice*
MAX239ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX239EWG	-40°C to +85°C	24 Wide SO
MAX239ERG	-40°C to +85°C	24 Narrow CERDIP
MAX239MRG	-55°C to +125°C	24 Narrow CERDIP
MAX240CMH	0°C to +70°C	44 Plastic FP
MAX240C/D	0°C to +70°C	Dice*
MAX241CAI	0°C to +70°C	28 SSOP
MAX241CWI	0°C to +70°C	28 Wide SO
MAX241C/D	0°C to +70°C	Dice*
MAX241EAI	-40°C to +85°C	28 SSOP
MAX241EWI	-40°C to +85°C	28 Wide SO
MAX242CAP	0°C to +70°C	20 SSOP
MAX242CPN	0°C to +70°C	18 Plastic DIP
MAX242CWN	0°C to +70°C	18 Wide SO
MAX242C/D	0°C to +70°C	Dice*
MAX242EPN	-40°C to +85°C	18 Plastic DIP
MAX242EWN	-40°C to +85°C	18 Wide SO
MAX242FJN	-40°C to +85°C	18 CERDIP
MAX242MJN	-55°C to +125°C	18 CERDIP

PART	TEMP RANGE	PIN-PACKAGE
MAX243CPE	0°C to +70°C	16 Plastic DIP
MAX243CSE	0°C to +70°C	16 Narrow SO
MAX243CWE	0°C to +70°C	16 Wide SO
MAX243C/D	0°C to +70°C	Dice*
MAX243CPE	-40°C to +85°C	16 Plastic DIP
MAX243CSE	-40°C to +85°C	16 Narrow SO
MAX243CWE	-40°C to +85°C	16 Wide SO
MAX243FJE	-40°C to +85°C	16 CERDIP
MAX243MJE	-55°C to +125°C	16 CERDIP
MAX244CQH	0°C to +70°C	44 PLCC
MAX244C/D	0°C to +70°C	Dice*
MAX244EQH	-40°C to +85°C	44 PLCC
MAX245CPL	0°C to +70°C	40 Plastic DIP
MAX245C/D	0°C to +70°C	Dice*
MAX245EPL	-40°C to +85°C	40 Plastic DIP
MAX246CPL	0°C to +70°C	40 Plastic DIP
MAX246C/D	0°C to +70°C	Dice*
MAX246EPL	-40°C to +85°C	40 Plastic DIP
MAX247CPL	0°C to +70°C	40 Plastic DIP
MAX247C/D	0°C to +70°C	Dice*
MAX247EPL	-40°C to +85°C	40 Plastic DIP
MAX248CQH	0°C to +70°C	44 PLCC
MAX248C/D	0°C to +70°C	Dice*
MAX248EQH	-40°C to +85°C	44 PLCC
MAX249CQH	0°C to +70°C	44 PLCC
MAX249EQH	-40°C to +85°C	44 PLCC

* Contact factory for dice specifications.

Package Information

For the latest package outline information, go to:
www.maxim-ic.com/packages

We cannot assume responsibility for use of any circuitry other than circuitry actively endorsed in a Maxim product. No circuit patent licenses are held. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 (408) 737-7600

©2007 Maxim Integrated Products

Printed in USA

MAXIM is a registered trademark of Maxim Integrated Products.

Features

- Compatible with MCS-51[®] Products
- Bytes of In-System Programmable (ISP) Flash Memory
- Endurance: 1000 Write/Erase Cycles
- V_{CC} to 5.5V Operating Range
- Low Power Static Operation: 0 Hz to 33 MHz
- Two-Level Program Memory Lock
- 16 x 8-bit Internal RAM
- 8 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Multiple Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Two Data Pointers
- Power-off Flag
- Fast Programming Time
- Optional ISP Programming (Byte and Page Mode)

Description

AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a cost-effective and flexible solution to many embedded control applications.

AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of internal data memory, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-level interrupt architecture, a full duplex serial port, on-chip oscillator, and support circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM content but freezes the oscillator, disabling all other chip functions until the next external reset or hardware reset.



8-bit Microcontroller with 4K Bytes In-System Programmable Flash

AT89S51

Rev. 2487A-10/01

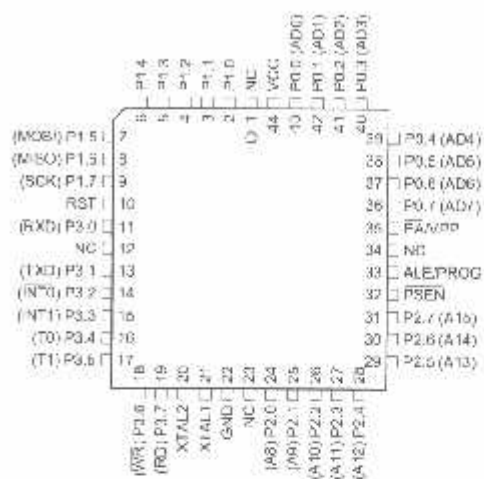


Configurations

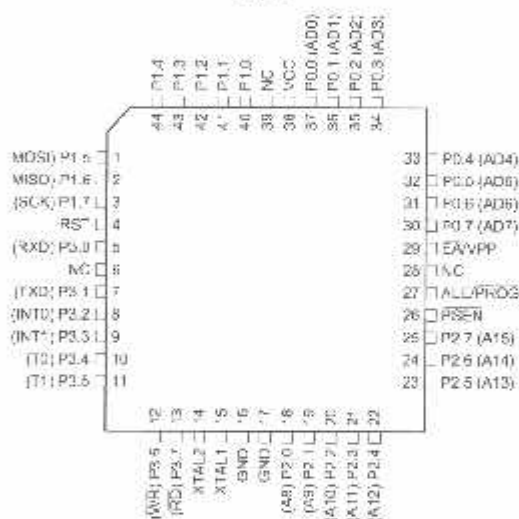
PDIP



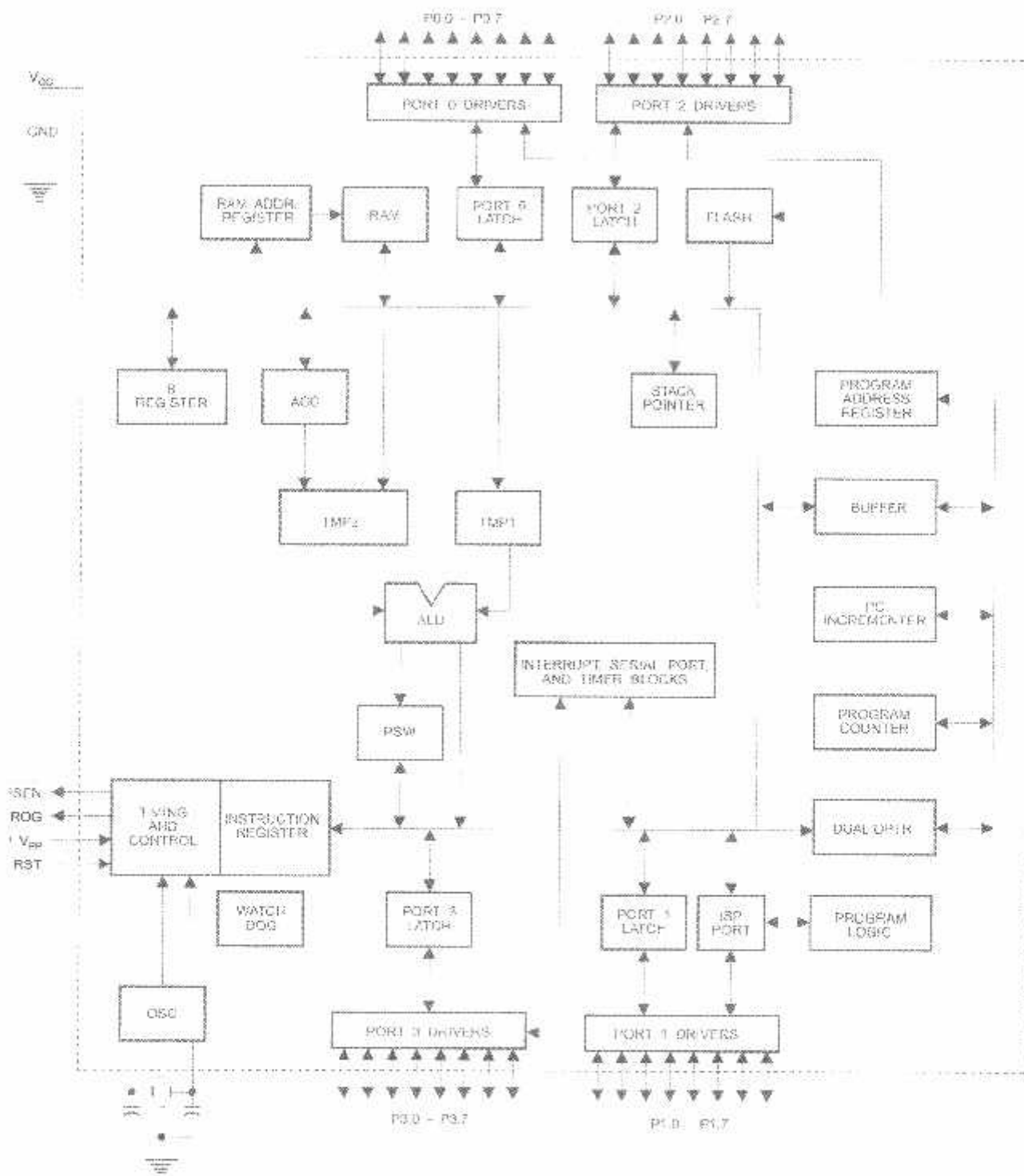
PLCC



TQFP



Block Diagram





Description

Supply voltage.

Ground.

- 0** Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.
- Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.
- Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

- 1** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.
- Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

- 2** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.
- Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.
- Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.
- 3** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.
- Port 3 receives some control signals for Flash programming and verification.
- Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

PROG

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN

Program Store Enable (PSEN) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

EA should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier



cial
ction
isters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

1. AT89S51 SFR Map and Reset Values

14							0FFH		
13	B 00000000						0F7H		
12							0EFH		
11	ACC 00000000						0E7H		
10							0DFH		
9	PSW 00000000						0D7H		
8							0CFH		
7							0C7H		
6	IP XX000000						0BFH		
5	P3 11111111						0B7H		
4	IE 0X000000						0AFH		
3	P2 11111111		AUXR1 XXXXXXXX0		WDTRST XXXXXXXXX		0A7H		
2	SCON 00000000		SBUF XXXXXXXXX				9FH		
1	P1 11111111						97H		
0	TCON 00000000		TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0	8FH
	P0 11111111		SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR		Address = 8EH				Reset Value = XXX00XX0B			
Not Bit Addressable		—	—	—	WDIDLE	DISRTO	—	—	DISALE
Bit		7	6	5	4	3	2	1	0
—		Reserved for future expansion							
DISALE		Disable/Enable ALE							
		DISALE							
		Operating Mode							
		0 ALE is emitted at a constant rate of 1/6 the oscillator frequency							
		1 ALE is active only during a MOVX or MOVC instruction							
DISRTO		Disable/Enable Reset out							
		DISRTO							
		0 Reset pin is driven High after WDT times out							
		1 Reset pin is input only							
WDIDLE		Disable/Enable WDT in IDLE mode							
WDIDLE									
0		WDT continues to count in IDLE mode							
1		WDT halts counting in IDLE mode							

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.



Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1								
Address = A2H								
Reset Value = XXXXXX0B								
Not Bit Addressable								
Bit	7	6	5	4	3	2	1	DPS 0
–								
DPS	Data Pointer Register Select							
DPS								
0	Selects DPTR Registers DP0L, DP0H							
1	Selects DPTR Registers DP1L, DP1H							

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

External Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory. On the AT89S51, if $\overline{EA}$ is connected to V_{CC} , program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Internal Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

Watchdog Timer (enabled with reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC=1/FOSC. To make the best use of the WDT, it

should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

During Power-down Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the ATMEL Web site (<http://www.atmel.com>). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the ATMEL Web site (<http://www.atmel.com>). From the home page, select 'Products', then '8051-Architecture Flash Microcontroller', then 'Product Overview'.

Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit position IE.6 is unimplemented. In the AT89S51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

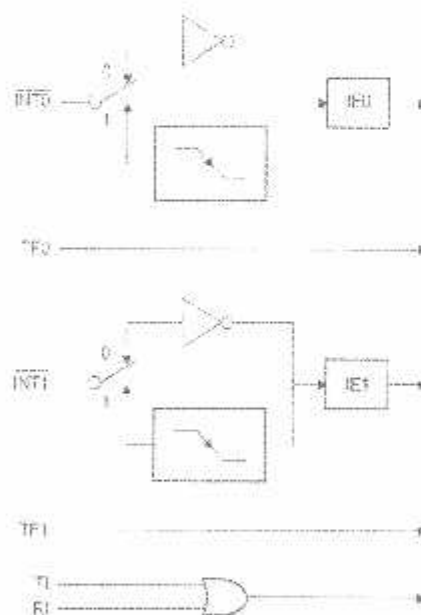
Table 4. Interrupt Enable (IE) Register

(MSB)				(LSB)			
EA	—	—	ES	ET1	EX1	ET0	EX0
Enable Bit = 1 enables the interrupt.							
Enable Bit = 0 disables the interrupt.							

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Reserved
—	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit

User software should never write 1s to reserved bits, because they may be used in future AT89 products.

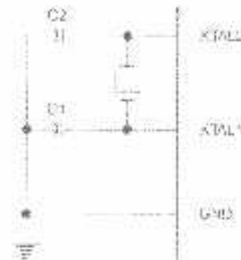
Figure 1. Interrupt Sources



Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF $\pm$ 10 pF for Crystals = 40 pF $\pm$ 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt into INT0 or INT1. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.



Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Program Memory Lock

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features
2	P	U	U	MOVX instructions executed from external program memory are disabled from fetching code bytes from internal memory. EA is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{\text{EA}}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of EA must agree with the current logic level at that pin in order for the device to function properly.

Programming Flash – Parallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{\text{EA}}/\text{V}_{\text{PP}}$ to 12V.
5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 μs . Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89S51 features Data Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.0 is pulled low after ALE goes high during programming to indicate BUSY. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates 89S51
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/PROG low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase Instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming Flash – al Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC} . The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

Programming rithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
Apply power between VCC and GND pins.
Set RST pin to "H".
If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.





Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8 on page 18.

Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

7. Flash Programming Modes

	V_{CC}	RST	PSEN	ALE/ PROG	$\overline{EA}/$ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0	P1.7-0
												Address	
Code Data	5V	H	L		12V	L	H	H	H	H	D_{IH}	A11-8	A7-0
Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OLT}	A11-8	A7-0
Lock Bit 1	5V	H	L		12V	H	H	H	H	H	X	X	X
Lock Bit 2	5V	H	L		12V	H	H	H	L	L	X	X	X
Lock Bit 3	5V	H	L		12V	H	L	H	H	L	X	X	X
Lock Bits	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Erase	5V	H	L		12V	H	L	H	L	L	X	X	X
Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
Device ID	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
Device ID	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.
2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.
3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/BSY signal is output on P3.0 during programming.
5. X = don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

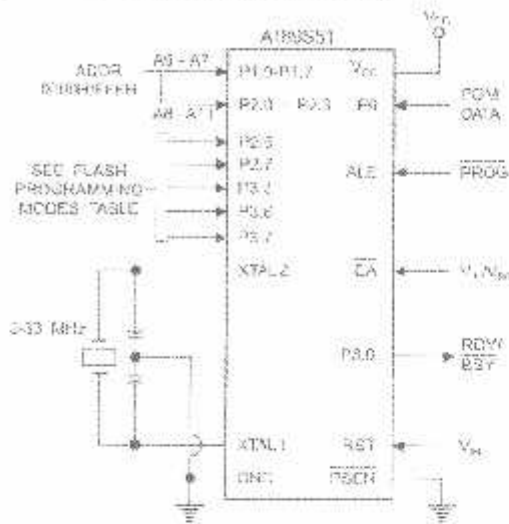
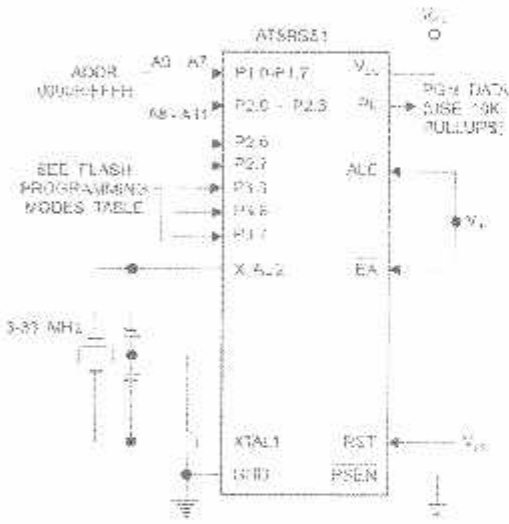


Figure 5. Verifying the Flash Memory (Parallel Mode)

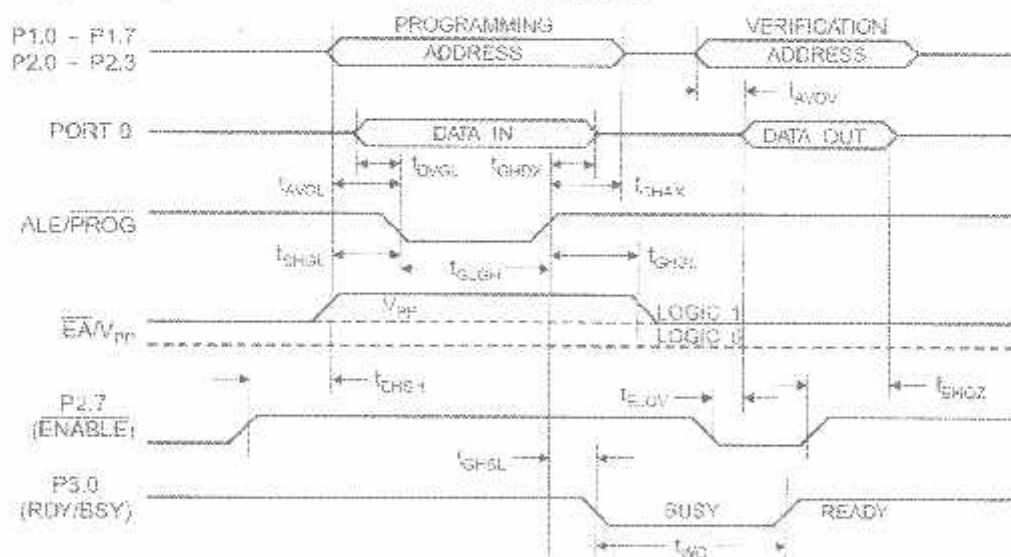


Flash Programming and Verification Characteristics (Parallel Mode)

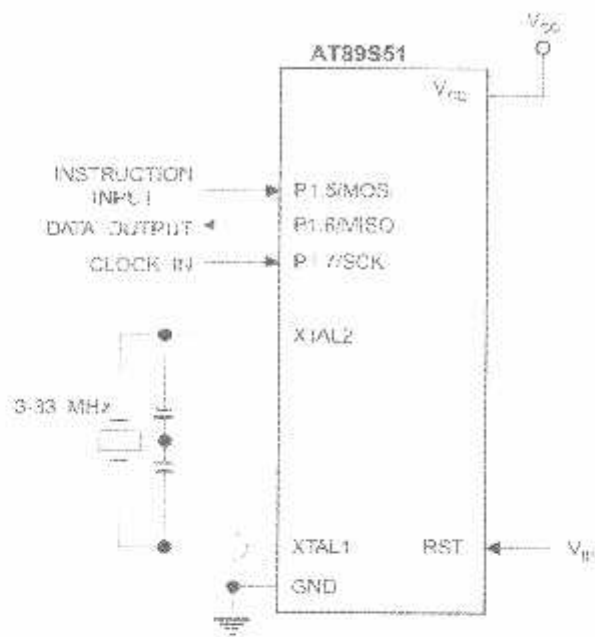
0°C to 30°C, $V_{CC} = 4.5$ to 5.5V

Symbol	Parameter	Min	Max	Units
	Programming Supply Voltage	11.5	12.5	V
	Programming Supply Current		10	mA
	V_{CC} Supply Current		30	mA
f	Oscillator Frequency	3	33	MHz
	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
	P2.7 (ENABLE) High to V_{DD}	$48t_{CLCL}$		
	V_{DD} Setup to $\overline{PROG}$ Low	10		μs
	V_{DD} Hold After $\overline{PROG}$	10		μs
	$\overline{PROG}$ Width	0.2	1	μs
	Address to Data Valid		$48t_{CLCL}$	
	ENABLE Low to Data Valid		$48t_{CLCL}$	
	Data Float After ENABLE	0	$48t_{CLCL}$	
	$\overline{PROG}$ High to BUSY Low		1.0	μs
	Byte Write Cycle Time		50	μs

6. Flash Programming and Verification Waveforms – Parallel Mode

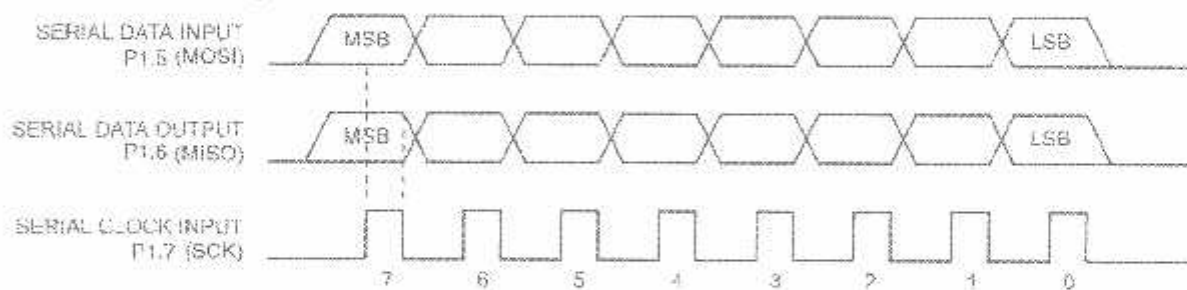


7. Flash Memory Serial Downloading



h Programming and Verification Waveforms – Serial Mode

8. Serial Programming Waveforms



8. Serial Programming Instruction Set

Instruction Format					Operation
Action	Byte 1	Byte 2	Byte 3	Byte 4	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output)	Enable Serial Programming while RST is high
Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Program Memory (Mode)	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	A15 A14 A13 A12 A11 A10 A9 A8	Read data from Program memory in the byte mode
Program Memory (Mode)	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	A15 A14 A13 A12 A11 A10 A9 A8	Write data to Program memory in the byte mode
Lock Bits ⁽²⁾	1010 1100	1110 00 B2 B1	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (2).
Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xx B2 B1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Signature Bytes ⁽¹⁾	0010 1000	xxx A5 A4 A3 A2 A1 A0	A15 A14 A13 A12 A11 A10 A9 A8	Signature Byte	Read Signature Byte
Program Memory (Mode)	0011 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Program Memory (Mode)	0101 0000	xxxx A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

1. The signature bytes are not readable in Lock Bit Modes 3 and 4.

2. B1 = 0, B2 = 0 → Mode 1, no lock protection
 B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
 B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
 B1 = 1, B2 = 1 → Mode 4, lock bit 3 activated

Each of the lock bits needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Serial Programming Characteristics

Figure 9. Serial Programming Timing

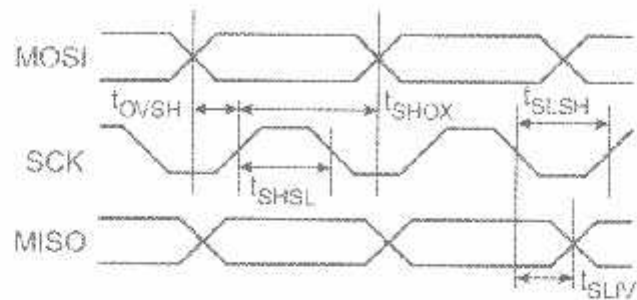


Table 9. Serial Programming Characteristics, $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 4.0 - 5.5\text{V}$ (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
f _{CL}	Oscillator Frequency	0		33	MHz
T _{CL}	Oscillator Period	30			ns
t _{SL}	SCK Pulse Width High	8 t _{CLCL}			ns
t _{SH}	SCK Pulse Width Low	8 t _{CLCL}			ns
t _{SH}	MOSI Setup to SCK High	t _{CLCL}			ns
t _{SH}	MOSI Hold after SCK High	2 t _{CLCL}			ns
t _{SLV}	SCK Low to MISO Valid	10	16	32	ns
t _{SE}	Chip Erase Instruction Cycle Time			500	ms
t _{WC}	Serial Byte Write Cycle Time			64 t _{CLCL} + 400	μs

Absolute Maximum Ratings*

Operating Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin Respect to Ground.....	-1.0V to +7.0V
Maximum Operating Voltage.....	6.6V
Output Current.....	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

Values shown in this table are valid for $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 4.0\text{V}$ to 5.5V , unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{\text{EA}}$)	-0.5	$0.2 V_{CC} - 0.1$	V
	Input Low Voltage ($\overline{\text{EA}}$)		-0.5	$0.2 V_{CC} - 0.3$	V
	Input High Voltage	(Except XTAL1, RST)	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V
	Input High Voltage	(XTAL1, RST)	$0.7 V_{CC}$	$V_{CC} + 0.5$	V
	Output Low Voltage ⁽¹⁾ (Ports 1,2,3)	$I_{OL} = 1.6 \text{ mA}$		0.45	V
	Output Low Voltage ⁽¹⁾ (Port 0, ALE, PSEN)	$I_{OL} = 3.2 \text{ mA}$		0.45	V
		$I_{OH} = -60 \mu\text{A}$, $V_{CC} = 5\text{V} \pm 10\%$	2.4		V
	Output High Voltage	$I_{OH} = -25 \mu\text{A}$	$0.75 V_{CC}$		V
	(Ports 1,2,3, ALE, PSEN)	$I_{OH} = -10 \mu\text{A}$	$0.9 V_{CC}$		V
		$I_{OH} = -800 \mu\text{A}$, $V_{CC} = 5\text{V} \pm 10\%$	2.4		V
	Output High Voltage	$I_{OH} = -300 \mu\text{A}$	$0.75 V_{CC}$		V
	(Port 0 in External Bus Mode)	$I_{OH} = -80 \mu\text{A}$	$0.9 V_{CC}$		V
	Logical 0 Input Current (Ports 1,2,3)	$V_{IN} = 0.45\text{V}$		-50	μA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	$V_{IN} = 2\text{V}$, $V_{CC} = 5\text{V} \pm 10\%$		-650	μA
	Input Leakage Current (Port 0, $\overline{\text{EA}}$)	$0.45 < V_{IN} < V_{CC}$		± 10	μA
	Reset Pulldown Resistor		50	300	$\text{K}\Omega$
	Pin Capacitance	Test Freq. = 1 MHz, $T_A = 25^{\circ}\text{C}$		10	pF
		Active Mode, 12 MHz		25	mA
	Power Supply Current	Idle Mode, 12 MHz		6.5	mA
	Power-down Mode ⁽²⁾	$V_{CC} = 5.5\text{V}$		50	μA

- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- Minimum V_{CC} for Power-down is 2V.

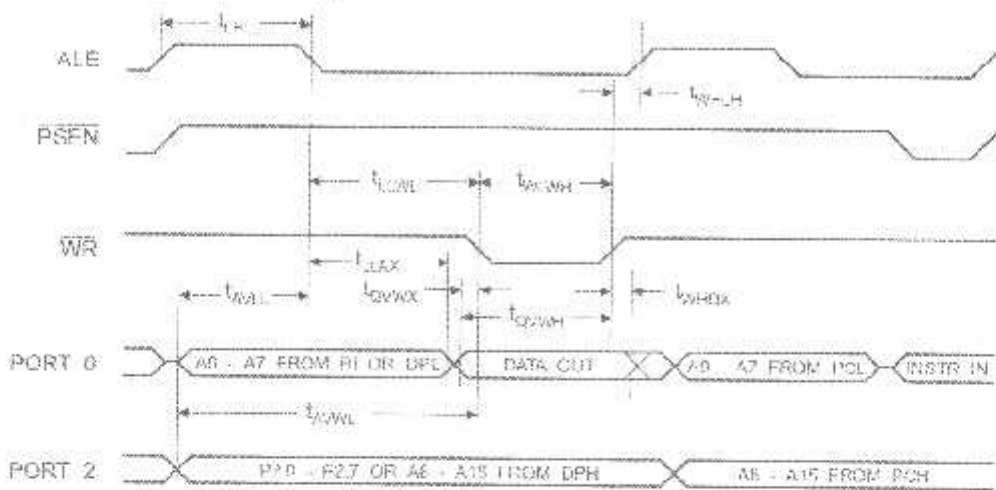
Characteristics

Operating conditions, load capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; load capacitance for all other pins = 80 pF.

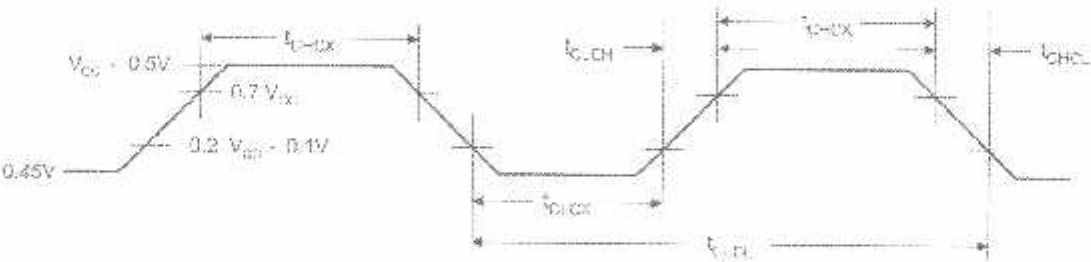
Internal Program and Data Memory Characteristics

No.	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1	Oscillator Frequency			0	33	MHz
2	ALE Pulse Width	127		$2t_{CLCL}-40$		ns
3	Address Valid to ALE Low	43		$t_{CLCL}-25$		ns
4	Address Hold After ALE Low	48		$t_{CLCL}-25$		ns
5	ALE Low to Valid Instruction In		233		$4t_{CLCL}-65$	ns
6	ALE Low to PSEN Low	43		$t_{CLCL}-25$		ns
7	PSEN Pulse Width	205		$3t_{CLCL}-45$		ns
8	PSEN Low to Valid Instruction In		145		$3t_{CLCL}-60$	ns
9	Input Instruction Hold After PSEN	0		0		ns
10	Input Instruction Float After PSEN		59		$t_{CLCL}-25$	ns
11	PSEN to Address Valid	75		$t_{CLCL}-8$		ns
12	Address to Valid Instruction In		312		$5t_{CLCL}-80$	ns
13	PSEN Low to Address Float		10		10	ns
14	RD Pulse Width	400		$6t_{CLCL}-100$		ns
15	WR Pulse Width	400		$6t_{CLCL}-100$		ns
16	RD Low to Valid Data In		252		$5t_{CLCL}-90$	ns
17	Data Hold After RD	0		0		ns
18	Data Float After RD		97		$2t_{CLCL}-28$	ns
19	ALE Low to Valid Data In		517		$8t_{CLCL}-150$	ns
20	Address to Valid Data In		585		$9t_{CLCL}-165$	ns
21	ALE Low to RD or WR Low	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
22	Address to RD or WR Low	203		$4t_{CLCL}-75$		ns
23	Data Valid to WR Transition	23		$t_{CLCL}-30$		ns
24	Data Valid to WR High	433		$7t_{CLCL}-130$		ns
25	Data Hold After WR	33		$t_{CLCL}-25$		ns
26	RD Low to Address Float		0		0	ns
27	RD or WR High to ALE High	43	123	$t_{CLCL}-25$	$t_{CLCL}+25$	ns

Internal Data Memory Write Cycle



Internal Clock Drive Waveforms



Internal Clock Drive

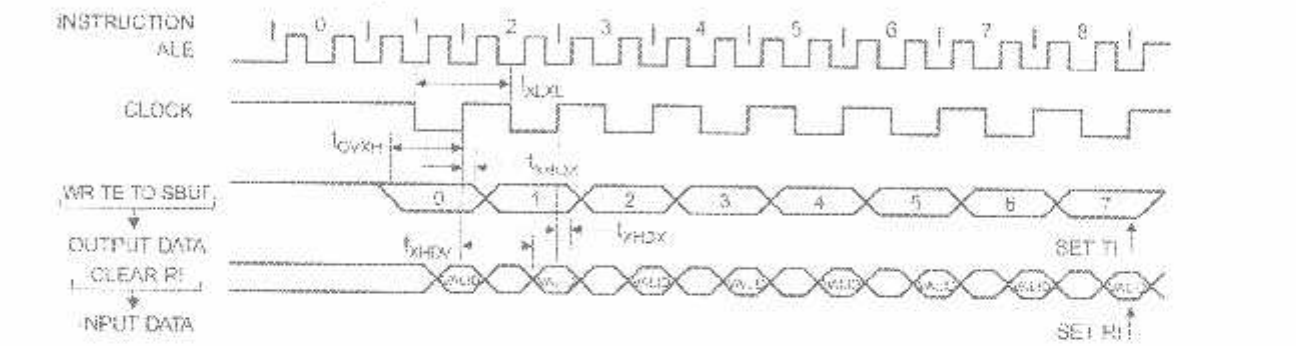
ol	Parameter	Min	Max	Units
-	Oscillator Frequency	0	33	MHz
-	Clock Period	30		ns
-	High Time	12		ns
-	Low Time	12		ns
-	Rise Time		5	ns
-	Fall Time		5	ns

al Port Timing: Shift Register Mode Test Conditions

alues in this table are valid for $V_{CC} = 4.0V$ to $5.5V$ and Load Capacitance = 80 pF .

bol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		μs
	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}-133$		ns
	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}-80$		ns
	Input Data Hold After Clock Rising Edge	0		0		ns
	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}-133$	ns

t Register Mode Timing Waveforms



Testing Input/Output Waveforms⁽¹⁾



- AC Inputs during testing are driven at $V_{OH} = 0.5V$ for a logic 1 and $0.45V$ for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

t Waveforms⁽¹⁾



- For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

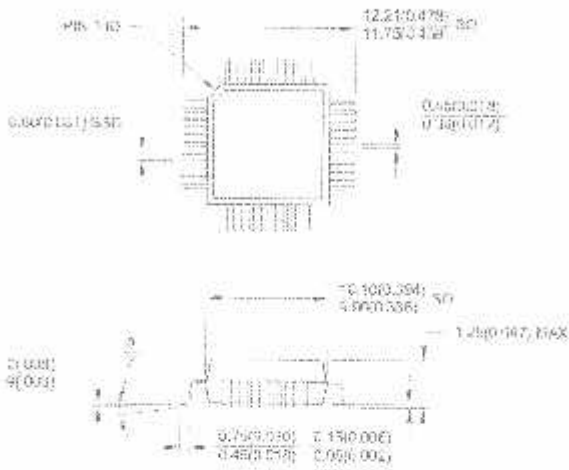
Speed (Hz)	Power Supply	Ordering Code	Package	Operation Range
4	4.0V to 5.5V	AT89S51-24AC	44A	Commercial (0° C to 70° C)
		AT89S51-24JC	44J	
		AT89S51-24PC	40P6	
		AT89S51-24AI	44A	Industrial (-40° C to 85° C)
		AT89S51-24JI	44J	
		AT89S51-24PI	40P6	
3	4.5V to 5.5V	AT89S51-33AC	44A	Commercial (0° C to 70° C)
		AT89S51-33JC	44J	
		AT89S51-33PC	40P6	

 = Preliminary Availability

Package Type	
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

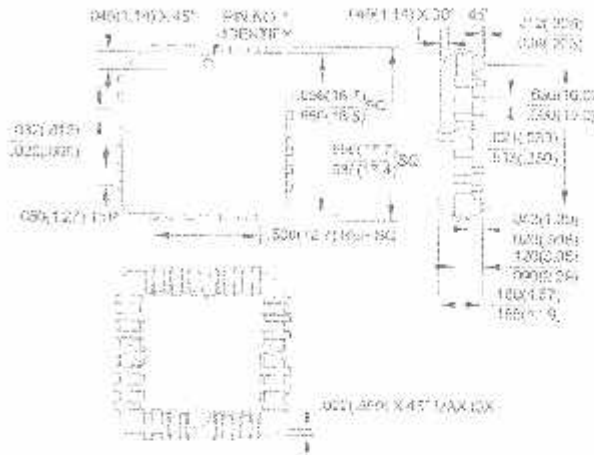
Packaging Information

1A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Millimeters and (Inches)*

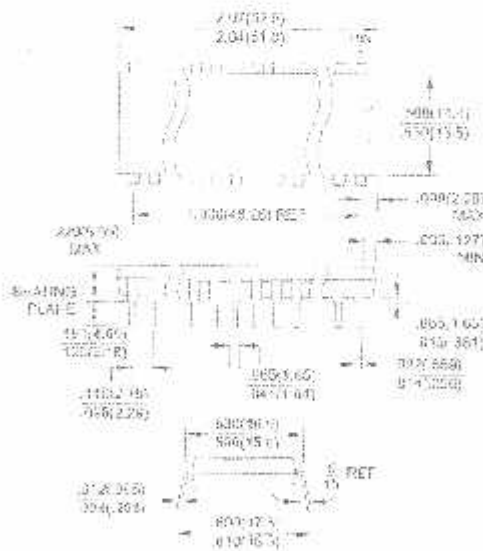


Controlling dimension: millimeters

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



P6, 40-pin, 0.600" Wide, Plastic Dual In-line Package (PDIP)
Dimensions in Inches and (Millimeters)
DEC STANDARD MS-011 AC





Atmel Headquarters

Corporate Headquarters
5 Orchard Parkway
Framingham, MA 01901
Tel: (508) 441-0311
Fax: (508) 487-2600

Atmel Europe
Atmel Europe Ltd.
The Courtyard
1000 Old London Road
Barnet, London EN4 8JF, UK
Tel: (44) 20-426-5555
Fax: (44) 20-426-5500

Atmel Asia, Ltd.
Room 1219
Nanchang Golden Plaza
Mody Road Tsimhatsui
Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Japan K.K.
Tonetsu Shinkawa Bldg.
4-1-1 Shinkawa
Chiyoda-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Product Operations

Atmel Colorado Springs
1150 E. Cheyenne Min. Blvd.
Colorado Springs, CO 80906
Tel: (719) 576-3300
Fax: (719) 540-1759

Atmel Grenoble
Avenue de Rochepierre
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-7658-3000
Fax: (33) 4-7658-3100

Atmel Heilbronn
Theresienstrasse 2
D-74025 Heilbronn, Germany
Tel: (49) 71 31 67 25 94
Fax: (49) 71 31 67 24 23

Atmel Nantes
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 0 2 40 18 16 18
Fax: (33) 0 2 40 18 19 60

Atmel Roussel
Zone Industrielle
13106 Roussel Cedex, France
Tel: (33) 4-4253-6000
Fax: (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
Tel: (44) 1355-357-000
Fax: (44) 1355-242-743

e-mail
literature@atmel.com

Web Site
<http://www.atmel.com>

© Corporation 2001.

Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty detailed in Atmel's Terms and Conditions located on the Company's web site. The Company assumes no responsibility for any errors that may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

Atmel is the registered trademark of Atmel.

Intel is the registered trademark of Intel Corporation. Terms and product names in this document may be the trademarks of others.



Printed on recycled paper.

2407A-01/01/01

