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SKRIPSI

PERANCANGAN AKUISISI DAN PEMROSESAN SINYAL ELEKTROKARDIOGRAFI (EKG) PORTABEL DENGAN MENGGUNAKAN RANGKAIAN MATRIK LED SEBAGAI PENAMPIL

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ABSTRAKSI

PERANCANGAN AKUISISI DAN PEMROSESAN SINYAL ELEKTROKARDIOGRAFI (EKG) PORTABEL DENGAN MENGGUNAKAN MATRIK LED SEBAGAI PENAMPIL

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Skripsi ini bertujuan untuk merancang dan membuat alat yang dapat mengakuisisi dan memproses sinyal jantung (EKG) secara portabel dengan menggunakan matrik LED sebagai penampil. Untuk dapat memperoleh sinyal jantung diperlukan 3 (tiga) buah elektroda yang berfungsi sebagai sensor dan rangkaian pengkondisi sinyal serta sebuah alat peraga atau penampil.

Dalam perancanganan alat ini penulis menggunakan IC AD620AN sebagai penguat instrumentasi dan IC LT1114CN serta IC TL072 sebagai filter. Kemudian output dari filter sebagai output EKG amplifier dihubungkan kerangkaian matrik LED yang dikendalikan oleh 3 (tiga) IC, yaitu IC LM3914 *dot/bar display driver* dan IC HCF4017 *decade counter with 10 decoded output* serta IC LM555 *timer*. IC penguat instrumentasi (IA) AD620AN adalah IC yang didalamnya sudah terdapat rangkaian penguat instrumentasi klasik tiga OP-Amp yang merupakan rangkaian utama dalam pemrosesan sinyal bioelektrik jantung. Prinsip kerjanya adalah pada saat terjadi selisih tegangan bioelektrik antara dua bagian sisi tubuh yang melalui elektroda-elektroda maka selisih tegangan tersebut akan dikuatkan oleh diferensial amplifier. Akan tetapi agar tegangan yang akan dikuatkan tidak drop atau hilang sebelum dikuatkan maka tegangan tersebut harus dilewatkan melalui penguat penyangga. Tegangan ini adalah tegangan AC yang memiliki amplitudo yang besarnya anatara 0.5-10mV. Untuk pemrosesan selanjutnya tegangan keluaran dari penguat instrumentasi akan dilewatkan ke filter karena tegangan tersebut pasti membawa tegangan atau sinyal lain selain jantung seperti misalnya sinyal otot (EMG), frekwensi jala-jala 50Hz, gerakan-gerakan tubuh, dan lain-lain. Alat ini juga dapat dirancang ulang untuk digunakan sebagai penguat sinyal bioelektrik lainnya seperti EMG, EEG, ERG, dan pendeteksi tekanan darah yang tentunya berdasarkan prinsip yang serupa dengan EKG/ECG.

Agar hasil pemrosesan sinyal bioelektrik jantung ini dapat dilihat atau dianalisa maka sinyal tersebut harus ditampilkan melalui sebuah penampil atau peraga. Dalam perancangan ini alat peraga tersebut menggunakan matrik LED yang berfungsi layaknya osiloskop sederhana yang hanya memerlukan catu daya baterai. Tetapi dalam pengujian matrik LED itu sendiri sinyal yang ditampilkan kurang jelas dan sukar untuk dianalisa, namun fungsinya berjalan dengan cukup baik. Pada saat pengujian keseluruhan alat ini ternyata belum mampu menangkap sinyal bioelektrik jantung. Dan dari beberapa kali pengujian dapat disimpulkan bahwa kemungkinan ketidakmampuan alat ini dalam menangkap sinyal jantung dikarenakan masalah sumber masukkan dan sensivitas elektroda dan juga pemakaian kabel *input*.

Kata kunci : ECG, elektroda, filter, penguat instrumentasi, matrik LED

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Di dalam bidang kedokteran tidak dapat dipungkiri bahwa jantung adalah hal yang paling vital bagi manusia. Oleh karenanya kondisi jantung harus dipantau terus setiap saat. Salah satu caranya adalah dengan melakukan *monitoring* di Rumah Sakit yang menyediakan fasilitas tersebut. Namun bagi puskesmas atau klinik/balai kesehatan didaerah akan keberatan untuk melengkapi peralatan tersebut karena dirasakan besarnya biaya yang akan dikeluarkan.

Berangkat dari permasalahan diatas, maka timbul gagasan untuk membuat suatu perangkat EKG yang dapat memonitor kondisi jantung secara ekonomis dan terjangkau harganya serta mudah dibawa kemana-mana.

1.2. Tujuan.

Tujuan dari penulisan skripsi ini adalah merancang sistim akuisisi dan pemrosesan sinyal elektrokardiografi portabel dengan menggunakan rangkaian matrik LED sebagai penampil.

1.3. Rumusan Masalah.

Dalam perancangan akuisisi dan pemrosesan sinyal elektrokardiografi portabel ini dapat dirumuskan beberapa masalah yang akan dibahas antara lain :

1. Bagaimana merancang dan membuat alat yang dapat menampilkan sinyal biopotensial menjadi sinyal elektrokardiografi (ECG/EKG) tanpa interferensi sinyal-sinyal yang lainnya.
2. Bagaimana cara mengubah ion-ion dalam tubuh menjadi sinyal listrik yang dapat diukur oleh instrumen amplifier untuk ECG.
3. Bagaimana membuat alat ini menjadi sebuah alat dalam bentuk *mobile* yang dapat dibawa kemana-mana *(portabel)* yang dapat dibaca melalui sebuah penampil/peraga matrik LED.

1.4. Batasan Masalah.

Sehubungan dengan permasalahan yang dibahas dalam skripsi ini, maka penulis membatasi permasalahan ini untuk mencegah terjadinya perluasan dan penyimpangan pembahasan dari fokus permasalahan mengingat akan keterbatasan waktu dan biaya dengan batas-batas berikut :

1. Tidak membahas tentang kelainan atau penyakit jantung.
2. Tidak membahas elektroda selain elektroda disposabel.
3. Hanya membahas rangkaian ECG yang terdiri dari :
    - Rangkaian instrumentasi amplifier
    - Rangkaian filter (filter analog)
    - Rangkaian matrik LED
4. Tidak membahas *power supply*.

1.5. Metodologi Penelitian.

Metodologi penelitian yang dipakai dalam pembuatan skripsi ini adalah :

1. Studi literatur yang mempelajari teori-teori yang berkaitan mengenai cara kerja komponen-komponen yang digunakan dalam Perancangan Akuisisi dan Pemrosesan Sinyal Elektrokardiografi Portabel Dengan Menggunakan Rangkaian Matrik LED Sebagai Penampil.
2. Studi lapangan yang mana dilakukan di Instansi Rumah Sakit untuk melakukan perbandingan antara perangkat ECG yang akan dibuat dengan perangkat ECG yang ada di Rumah Sakit.
3. Pelaksanaan uji coba alat dari hasil Perancangan Akuisisi dan Pemrosesan Sinyal Elektrokardiografi Portabel Dengan Menggunakan Rangkaian Matrik LED Sebagai Penampil.
4. Penyusunan laporan skripsi dan menyimpulkan hasil perancangan dan pembuatan alat.

1.6. Sistematika Penulisan

Sistem penulisan yang akan digunakan untuk membahas masalah dalam Tugas Akhir ini diperlukan gambaran susunan alat secara keseluruhan yang selanjutnya ditentukan komponen-komponen utama dan pendukung yang digunakan dan kemungkinan untuk disederhanakan baik untuk bentuk, biaya pembuatanya agar didapatkan susunan yang se-efisien dan se-efektif mungkin.

Adapun pembahasan Tugas Akhir ini dibagi menjadi beberapa bab sebagai berikut:

BAB I **Pendahuluan**, yang memuat latar belakang, Rumusan Masalah, Tujuan, Batasan Masalah, Metodologi serta Sistematika Penulisan.

BAB II **Teori Dasar,** berisi tentang teori penunjang yang berhubungan dengan biopotensial jantung dan semua sistem instrumentasi medika.

BAB III **Perencanaan,** membahas tentang perencanaan dan pembuatan alat.

BAB IV **Analisa dan Pengujian Alat,** berisikan tentang pengujian alat yang telah dibuat, pengoperasian dan spesifikasi alat.

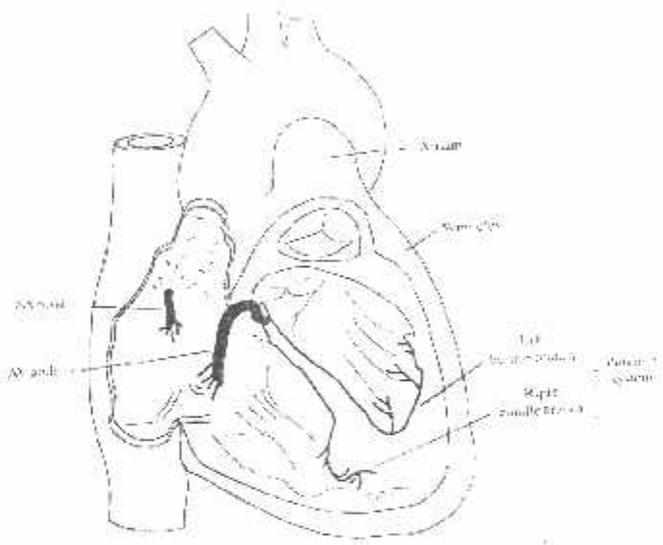
BAB V **Penutup,** yang berisi kesimpulan dan Saran.

BAB II

TEORI DASAR

2.1. Aktivitas Dalam Jantung

Jantung terdiri dari dua (2) bagian otot yang halus, yaitu *atrium* dan *ventricle*. Urutan dari sel-sel yang terdepolarisasi dalam jantung diperlihatkan pada gambar di bawah ini :



Gambar 2.1 Depolarisasi Sel Dalam Jantung [2)]

2.1.1. Sinuatrial (SA) Node

Simpul Sinuatrial berdenyut pada tempo dari 70 sampai 80 denyutan per-menit (*beat per-minute* : bpm) pada saat kondisi jantung tenang atau istirahat.

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[1] Richard Aston,"Principles of Biomedical Instrumentation and Measurement", An Imprint of Macmillan Publishing Company, New York : 45

SA node biasanya yang menentukan detak jantung sehingga dapat dikatakan bahwa SA node adalah sebagai pemicu detak jantung [1].

2.1.2. Atrioventricular (AV) Node

Simpul Atrioventricular berdenyut pada tempo 40 sampai 60 denyutan per-menit (*beat per-minute* : bpm), sedangkan *bundle branch* berisolasi pada 15 sampai 40 bpm. Depolarisasi (penyebaran) dari SA node tersebar melalui atrium dan sampai pada AV node sekitar 40ms. Karena rendahnya kecepatan sifat konduksi dari jaringan AV node sehingga membutuhkan waktu sekitar 110ms untuk depolarisasi untuk mencapai *bundle branch* yang disebut sebagai *purkinje system* [1]. Kemudian ventrikel berkontraksi sehingga ventrikel yang kanan mendorong atau memaksa darah ke paru-paru, sedangkan ventrikel kiri mendorong darah ke pembuluh darah *aorta* dan berikutnya melalui sistim peredaran darah. Waktu pada saat jantung berkontraksi disebut *systole*, sedangkan pada saat jantung kembali pada keadaan tenangnya / kondisi istirahat disebut *diastole* [1]. Dari kejadian - kejadian diatas inilah maka dapat diukur sinyal elektrokardiogramnya.

2.2. Biopotensial Pada Jantung

Pada saat *diastole*, ketika jantung dalam kondisi istirahat, seluruh sel terpolarisasi sehingga potensial didalam tiap sel adalah negatif jika dilihat dari luar sel. Biasanya depolarisasi terjadi pertama kali di SA node yang mengakibatkan bagian luar dari jaringan negatif jika dilihat dari dalam sel [2].

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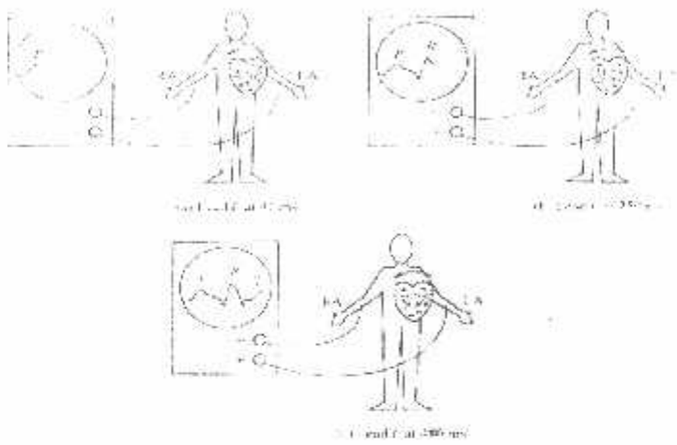
[2] Richard Aston,"Principles of Biomedical Instrumentation and Measurement", An Imprint of Macmillan Publishing Company, New York : 46

Hasil yang tidak setimbang ini dalam arus ion I menyebabkan tangan kiri (LA) terukur positif jika terukur dengan tangan kanan (RA), seperti yang diperlihatkan pada gambar dibawah :



Gambar 2.2 Arus Ionik Sebagai Sumber Dari Elektrokardiogram [3)]

Dari proses yang terjadi pada gambar .a. inilah akan muncul *P - Wave*. Setelah sekitar 90ms, *atrium* secara penuh terdepolarisasi dan arus ion diukur dengan *lead* I menurun sampai nol. Depolarisasi kemudian lewat melalui jaringan otot simpul atrioventricular yang menyebabkan waktu tunda sekitar 110ms. Depolarisasi kemudian lewat melalui jaringan otot ventrikular yang kanan yang membuat menjadi lebih negatif jika dibandingkan dengan polarisasi yang diam pada jaringan otot ventrikular kiri seperti yang diperlihatkan pada gambar .b. sehingga arah dari I menyebabkan tegangan dari positif (+) dan negatif (-) dari LA ke RA yang disebut sebagai *R – Wave* [3)]. Sedangkan sinyal *T - Wave* (gambar .c.) muncul dari repolarisasi dari jaringan otot ventrikel.

[3] Richard Aston,"Principles of Biomedical Instrumentation and Measurement". An Imprint of Macmillan Publishing Company, New York : 47

Bentuk gelombang dari elektrokardiografi secara lengkap digambarkan seperti gambar dibawah yang mana dikenal dengan gelombang P, Q, R, S, dan T.

Gambar 2.3 Gelombang Sinyal Elektrokardigrafi [4)]

Interval :

P-R *Beginning of P-Waveto beginning of QRS complex.*

S-T *End of S-Wave to end of T-Wave.*

Q-T *Beginning of Q-Wave to end of T-Wave*

Segment :

P-R *End of P-Wave to beginning of Q-Wave.*

S-T *End of S-Wave to beginning of T-Wave.*

Complex :

QRS *Beginning of Q-Wave to end of S-Wave.*

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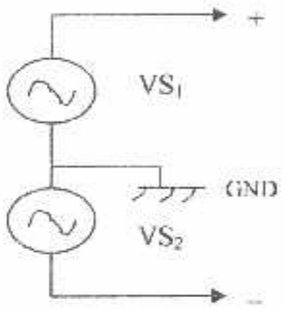
[4] Richard Aston,"Principles of Biomedical Instrumentation and Measurement", An Imprint of Macmillan Publishing Company, New York : 48

Duration :

Average duration shown on drawing in second.

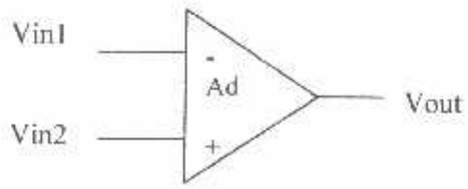
2.3. Biopotensial Amplifier

Elektrokardiograf terukur sebagai beda potensial diantara dua anggota tubuh. Jika digambarkan equivalennya maka beda potensial ini seperti ada dua sumber tegangan.



Gambar 2.4 Dua Potensial Berbeda Yang Terukur ECG

Sehingga dengan adanya dua sumber tegangan yang berbeda ini maka diffirensial amplifiernya adalah yang ideal untuk mengukur beda potensial ini dan sering kali dipakai untuk aplikasi instrumentasi medika. Suatu differensial amplifier sangatlah penting pada perancangan sistem penguat instrumentasi karena differensial amplifier dapat menghilangkan interferensi *Common Mode Voltage (Vcm)*. Idealnya, jika kedua input differensial *amplifiier* memiliki masukkan yang sama maka outputnya cenderung mengarah menjadi nol, sehingga dengan demikian tegangan keluaran dari suatu differensial *amplifier* adalah penguatan dari selisih tegangan antara kedua input diffrensial *amplifier* (*inverting* dan *non inverting*).



Gambar 2.5 Simbol Differensial Amplifier

Penulisan secara matematisnya untuk differensial amplifiernya adalah :

$$Vout = Ad\ (\ Vin2 - Vin1\ ) \quad \text{..... (2-1)}$$

Dimana :

1. Vin1 dan Vin2 adalah tegangan input jika terukur terhadap ground.
2. Vout adalah tegangan output.
3. Ad adalah tegangan differensial gain.

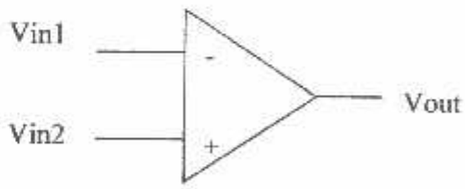
Commond mode voltage adalah apapun yang memiliki nilai yang sama pada semua input terminal differensial amplifier. Maksudnya adalah jika Vin1 dan Vin2 adalah *common mode voltage* (CMV), maka Vin1=Vin2, dan Vout –nya adalah nol. Sehingga tegangan output cenderung mengarah atau menjadi nol karena *commond mode interference*. Differensial amplifier dapat diproduksi atau dibuat dalam bentuk rangkaian *Integrated Circuit* (IC) dengan biaya yang sangat murah sehingga hal ini memungkinkan untuk membuat suatu amplifier dengan *input impedance* yang sangat tinggi sehingga memungkinkan juga untuk membuat *gain amplifier* yang sangat tinggi pula. Semuanya ini dapat dibuat dengan dengan biaya yang murah jika kebutuhan untuk daya (*power requirement*) rendah dan kisaran frekwensi (*frequency range*) berada pada yang diperlukan untuk biopotensial amplifier sehingga menjadi ekonomis dan praktis untuk

mendifinisikan suatu differensial amplifier yang ideal sebagai suatu komponen untuk analisis rangkaiannya.

2.4. Analisis Operasional Amplifier (*Op- Amp*)

Amplifier yang digunakan sebagai ideal differensial amplifier bersama komponen-komponen R, L, C lainnya disebut *Operasional Amplifier* atau dikenal dengan singkatan *Op-Amp*. Kata "*operasional* " dipakai karena rangkaian-rangkaian ini membentuk suatu operasi-operasi matematik di tegangan masukannya. *Op-Amp* sebenarnya merupakan sebuah penguat tegangan DC differensial yang mana karakteristik idealnya didefinisikan sebagai berikut :

- Setiap *input*-nya memiliki impedansi yang tak terhingga, sehingga $Z = \infty$.
- Penguatan (*gain*)adalah tak terhingga, $Ad = 0$.
- Lebar pita yang tak terhingga (*infinite bandwidht*).
- Impedansi masukan yang tak terhingga (*infinite input impedance*)
- Impedansi keluaran sama dengan nol



Gambar 2.6 Simbol Op-Amp

Tegangan keluaran suatu *Op-Amp* (*Vout*) dapat dikatakan sebagai suatu nilai yang dalam bentuk fisik dan harus tetap terhingga, sehingga dapat dirumuskan :

$$Vin1 = Vin2 = \frac{Vout}{Ad} = \frac{Vout}{\infty} = 0 \quad \text{..... (2-2)}$$

Implikasinya yang dapat segera dilihat untuk asumsi yang ideal bahwa : $Vin2 \approx Vin1$

Dengan demikian dikarenakan kedua impedansi masukkan adalah tak terhingga (infinite) $I1 \neq 0$ dan $I1 \approx 0$ dan karena persamaan untuk tegangan keluaran :

$$Vout = Ad\,(\,Vin2 - Vin1\,) \quad \text{..... (2-3)}$$

dapat dianggap suatu yang benar, tegangan keluaran Vout tetap konstan jika dilihat dari beban yang dihubungkan, sehingga dapat diambil kesimpulan bahwa differensial amplifier yang ideal mempunyai impedansi keluaran = 0.

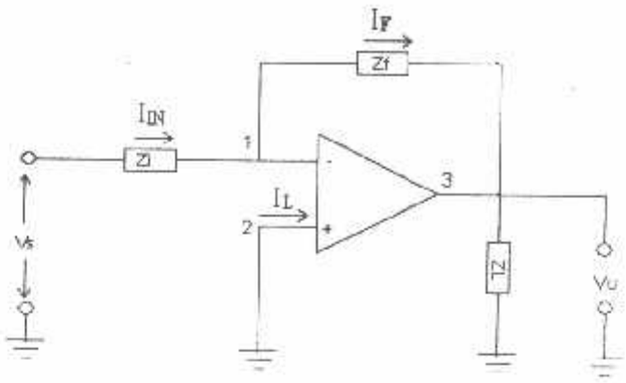
$$Zout = 0$$

Ada beberapa aturan yang berhubungan dengan gambar 2-7, yaitu :

Aturan #1 $V1 \approx V2$

Aturan #2 $I1 \neq 0$, $I2 \neq 0$

Aturan-aturan ini adalah tambahan untuk hukum kirchoff untuk tegangan dan arus (Kirchoff Voltage Low-KVL dan Kirchoff Current Low-KCL), dengan hukum dimana V = I . R untuk komponen-komponen R, L, dan C yang semuanya dibutuhkan untuk menganalisa setiap jaringan yang mengandung komponen-komponen ideal



Gambar 2.7 Suatu Op Amp Yang Dibebani Dengan Impedansi Z_L[5]

Gambar diatas memperlihatkan Op-Amp yang sederhana yang dianalisa dengan menggunakan aturan-aturan #1 dan #2.

Zi dan Zf pada gambar adalah impedansi yang kompleks karena V2 dihubungkan ke ground, V2 = 0, dan dengan melihat aturan #1 maka V1 = 0.

Dengan menggunakan KCL pada simpul 1 maka dapat ditulis :

$$I_{IN} = I_F + I_L$$

Dan dengan aturan #2, I1 = 0, sehingga :

$$I_{IN} = I_F$$

Maka dengan menambahkan hukum Ohm ke cabang inputnya :

$$\frac{Vs - Vi}{Zi} = I_{IN} = -\frac{Vs}{Zi} \quad \text{..... (2-4)}$$

Karena V1 = 0, maka hukum Ohm dipakai untuk cabang umpan baliknya sehingga :

$$\frac{Vs - Vout}{Zi} = I_F = -\frac{Vout}{Zi} \quad \text{..... (2-5)}$$

Kombinasi dengan persamaan 2-4 maka dapat dituliskan :

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[5] Richard Aston."Principles of Biomedical Instrumentation and Measurement". An Imprint of

$$\frac{Vs}{Zi} = -\frac{Vout}{Zf} \quad \text{..... (2-6)}$$

Voltage gain A dari rangkaian diatas adalah $A = -\frac{Vout}{Vs}$

$$A = -\frac{Zf}{Zi} \quad \text{..... (2-7)}$$

Impedansi input dari amplifier ini, Z_{IN} di definisikan :

$$Z_{IN} = \frac{Vs}{I_{IN}} \quad \text{..... (2-8)}$$

Dari persamaan 2-4 didapatkan :

$$\frac{I_{IN} \cdot Zi}{I_{IN}} = Z_{IN} = Zi \quad \text{..... (2-9)}$$

Pada gambar 2.6 telihat bahwa *Op-Amp* memiliki dua masukan, yaitu masukan non-inversi atau disebut juga masukkan tak membalik (+) dan masukan inversi (-) atau disebut juga membalik (-). Perbedaan antara kedua masukan *Op-Amp* tersebut dapat dijelaskan sebagai berikut :

- Jika sinyal melalui non-inversi / tak membalik maka keluarannya akan sefase (*in phase*) dengan masukannya, sehingga jika masukannya positif maka keluarannya juga positif [6].
- Jika sinyal melalui masukan inversi / membalik maka keluarannya berbeda fasa 180° (*out of phase by 180°*) atau keluarannya negatif, demikian juga sebaliknya [6].

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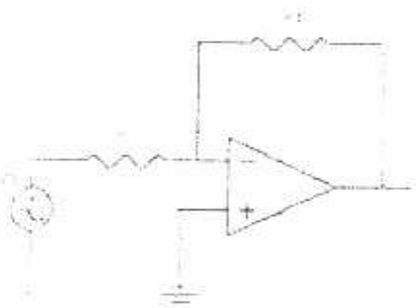
[6] "Penapis Aktif Elektronika", Teori dan Praktek, Hal : 4

Yang sangat penting dari susunan *Op-amp* differensial amplifier adalah susunan-susunan kombinasi inversi dan non inversi yang memiliki suatu karakteristik unik pada rangkaiannya itu sendiri. Pada saat menguatkan sinyal bioelektrik dari *ECG*, rangkaian penguat differensial dapat me-*reject* interferensi sinyal frekwensi 60Hz. Biasanya *Op-amp* diberi catu daya (*power supply*) dengan polaritas ganda atau simetris dengan kisaran ± 5V sampai ± 18V. Namun ada juga yang diberi catu daya tunggal atau *single supply* dengan kisaran 1.5V sampai 32V.

2.4.1 Penguat Inversi (*Inverting Amplifier*)

Seperti yang sudah dijelaskan diatas bahwa apabila pada suatu penguat inversi diberikan sinyal masukan positif maka keluarannya akan negatif karena penguatan inversinya adalah penguatan yang membalik yang mana keluarannya berbalik fasa 180° dengan masukannya [5].



Gambar 2.8 Rangkaian Penguat Inversi [5]

Keterangan gambar :

- Ri : Resistor masukkan

- Rf : Resistor umpan balik

Pada rangkaian penguat inversi, masukkan positif dihubungkan dengan *ground* atau *common ground*, sedangkan masukkan negatifnya digunakan sebagai masukkan sinyal yang akan dikuatkan.

Dari gambar diatas didapatkan persamaan tegangan output (Vo) :

$$\frac{Vo}{Ri} = -\frac{Vo}{Rf} \triangleright \frac{Vo}{Vi} = -\frac{Rf}{Ri} \quad \text{..... (2-10)}$$

Sehingga ;

$$Vo = -\frac{Rf}{Ri} Vi \quad \text{..... (2-11)}$$

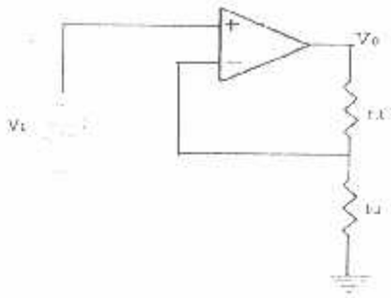
Sedangkan penguatannya (*gain*) :

$$A_i = \frac{Vo}{Vi} = -\frac{Rf}{Ri} \quad \text{..... (2-12)}$$

2.4.2 Penguat Non-Inversi (*Non-inverting Amplifier*)

Prinsip rangkaian penguat non-inversi (tak membalik) merupakan kebalikan dari penguat inversi sehingga konstruksi rangkaiannya pun juga berbeda. Dari gambar dibawah dapat disimpulkan bahwa penguat non-inversi menggunakan prinsip pembagi tegangan (*voltage divider*) sehingga dapat dituliskan persamaan tegangan output (Vo) [7] :

[7] "Penapis Aktif Elektronika",Teori dan Praktek, Hal : 4



Gambar 2.9 Rangkaian Penguat Non-Inversi (Tak Membalik) [7]

$$Vi = \frac{RiVo}{Ri + Rf} \quad \text{..... (2-13)}$$

$$\frac{Vo}{Vi} = \frac{Ri + Rf}{Ri} \quad \text{..... (2-14)}$$

Sehingga ;

$$Vo = 1 + \frac{Rf}{Ri} Vi \quad \text{..... (2-15)}$$

Sedangkan penguatannya (*gain*) :

$$A = \frac{Vo}{Vi} = 1 + \frac{Rf}{Ri} \quad \text{..... (2-16)}$$

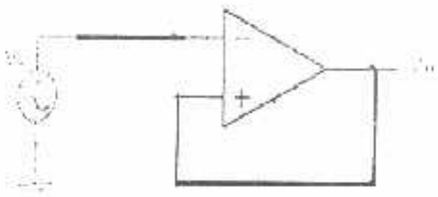
2.4.3 Pengikut Tegangan (*Voltage Follower*)

Rangkaian pengikut tegangan kadang disebut juga sebagai rangkaian penyangga (*buffer amplifier*) dan memiliki fungsi yang sama seperti pengikut

[7] "Penapis Aktif Elektronika",Teori dan Praktek, Hal : 4

emiter (*emither follower*) atau pengikut katoda (*cathode follower*) [8]. Ciri-ciri rangkain pengikut tegangan adalah :

- Memiliki impedansi masukkan yang sangat tinggi ; (lebih dari 100kΩ).
- Memiliki impedansi keluaran yang sangat rendah ; (kurang dari 75Ω).



Gambar 2.10 Rangkaian Pengikut Tegangan [8]

Jika dibandingkan dengan rangkaian penguat non inversi (gambar 2-11) maka rangkaian pengikut tegangan adalah sama, dengan Ri = ∞ dan Rf = 0.
Dengan demikian penguatan tegangan selalu – 1. Sinyal keluaran sama persis (identik) dengan sinyal masukkan atau keluaran mengikuti masukkan, sehingga Vin = Vout. Fungsi utama dari rangkaian pengikut tegangan adalah sebagai penyangga atau mengisolasi beban dari sumber [8].

2.5 Rangkaian Penapis (*Filter*)

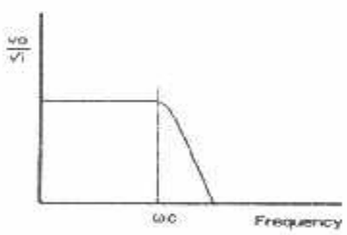
Rangkaian penapis (*filter*) adalah sebuah rangkaian yang dapat melewatkan atau meloloskan sinyal dan menahan sinyal yang tidak diinginkan pada frekwensi tertentu. Rangkaian penapis ada dua jenis, yaitu penapis analog dan penapis digital, sedangkan penapis analog itu sendiri ada dua macam tipe, yaitu penapis aktif dan penapis pasif. Rangkaian penapis aktif maupun pasif

memiliki karakteristik sinyal yang sama hanya saja pada penapis aktif terdapat penguatan *passband*-nya. Ini dikarenakan penapis aktif menggunakan komponen aktif sebagai pembangun dasarnya yang mana dalam hal ini komponen aktif tersebut adalah IC *Op-Amp*.

Penapis digital sangat berbeda dengan rangkaian elektronik digital atau program komputer yang memroses sinyal untuk melaksanakan fungsi yang serupa seperti pada penapis analog. Tidak seperti penapis analog, penapis digital beroperasi berdasarkan jumlah nomor urutan yang lebih baik pada suatu gelombang kontinyu [9]. Namun dalam penulisan skripsi ini tidak akan membahas penapis digital karena pada perencanaan alatnya tidak menggunakan *digital filter*.

2.5.1 *Low Pass Filter*

Rangkaian *low pass filter* adalah rangkaian filter yang meloloskan sinyal dengan frekwensi dibawah *frekwensi cutoff* dan menahan sinyal sinyal diatas *frekwensi cutoff*. Ada bemacam-macam rangkaian *low pass filter*, tetapi karakteristik maupun fungsinya adalah sama. Pada rangkaian *low pass filter* aktif memiliki penguatan yang disebut penguatan *passband* [10].



Gambar 2.11 Kurva karakteristik *low pass filter* [10]

Keterangan :

[9] Willis J. Thompskin and John G. Wester,"Design of Micro Computer Based Medical Instrumentation",Prentice HALL, New Jersey : 99
[10] "Penapis Aktif Elektronika",Teori dan Praktek, Hal : 27

$\frac{Vo}{Vi}$ (dB) = Tanggapan amplitudo

$$\omega c = \frac{1}{\tau} = \frac{1}{RC}$$ (dalam *radian per second*)

Persamaan equivalennya :

fco = frekwensi cuttof

$$fco = \frac{1}{2 \pi f c} \quad \text{..... (2-17)}$$

Sedangkan penguatan *passband*-nya adalah :

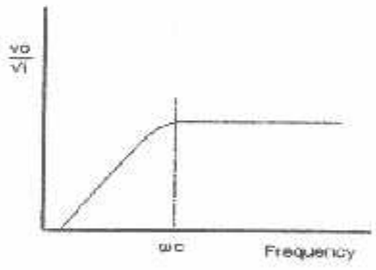
$$dB = -20 \log 10 \frac{Vo}{Vi} \quad \text{..... (2-18)}$$

Jika Vo > Vi, maka terjadi penguatan karena nilainya positif.

Jika Vo < Vi, maka terjadi pelemahan (*atenuasi*) karena nilainya negatif.

2.5.2 *High Pass Filter*

High pass filter merupakan kebalikan dari *low pass filter* yang mana pada rangkaian ini akan meloloskan sinyal dengan frekwensi diatas frekwensi *cutoff*.



Gambar 2.12 Kurva karakteristik *high pass filter* [11]

[11] "Penapis Aktif Elektronika", Teori dan Praktek, Hal : 32

Selain dapat meloloskan sinyal pada frekwensi tertentu, *high pass filter* juga dapat memblok sinyal DC yang lewat baik yang berasal dari noise sinyal tegangan yang yang akan di filter maupun yang berasal dari keluaran *Op-amp* itu sendiri. Seperti halnya *low pass filter* maka pada *high pass filter* pun juga menggunakan persamaan :

$$f_o = \frac{1}{2\pi RC} \quad \text{..... (2-19)}$$

Sedangkan penguatan *passband*-nya adalah :

$$dB = -20 \log 10 \frac{Vo}{Vi} \quad \text{..... (2-20)}$$

Jika Vo > Vi, maka terjadi penguatan karena nilainya positif.

Jika Vo < Vi, maka terjadi pelemahan (*atenuasi*) karena nilainya negatif.

2.5.3 *Band Pass Filter*

Band pass filter merupakan gabungan antara *high pass filter* dan *low pass filter*. Dari gabungan dua filter ini akan meloloskan sinyal-sinyal dengan frekwensi antara (*high pass filter* dan *low pass filter* = *median frequency*) dan menahan frekwensi dibawah dan median tersebut. Untuk filter jenis ini dikenal dengan istilah frekwensi tengah (fo) dan lebar pita (*bandwidht* = BW) dengan pengertian sebagai berikut :

- Frekwensi tengah merupakan titik munculnya penguatan tegangan paling besar atau maksimum[12].

[12] "Penapis Aktif Elektronika",Teori dan Praktek, Hal : 33

- Lebar pita dari suatu *band pass filter* adalah perbedaan antara frekwensi atas (F_H) dan frekwensi bawah (F_L) dibawah penguatan tegangannya, yaitu 0,707 kali dari nilai maksimum atau 3dB lebih rendah dari penguatan tegangan frekwensi tengah atau [12] :

$$BW = F_H - F_L \quad \text{..... (2-21)}$$

Karena semua tanggapan frekwensi digambar dengan skala log, maka terlihat bahwa seolah-olah band pass filter simetri pada frekwensi tengahnya.

Sehingga jika ada yang menyimpulkan bahwa fo adalah ditengah-tengah F_H dan F_L maka hal tersebut adalah salah. Ternyata frekwensi tengah (fo) sama dengan rata-rata geometrik atau dapat dituliskan sebagai berikut :

$$fo = 0{,}5(F_H.F_L) \quad \text{..... (2-22)}$$

Lebar pita (BW) dan frekwensi tengah (fo) memiliki hubungan satu sama lainnya dengan faktor kualitas (Q), sehingga :

$$Q = \frac{fo}{BW} \quad \text{..... (2-23)}$$

$$Q = \frac{fo}{F_H - F_L} \quad \text{..... (2-24)}$$

Sedangkan untuk frekwensi *cutoff* dirumuskan :

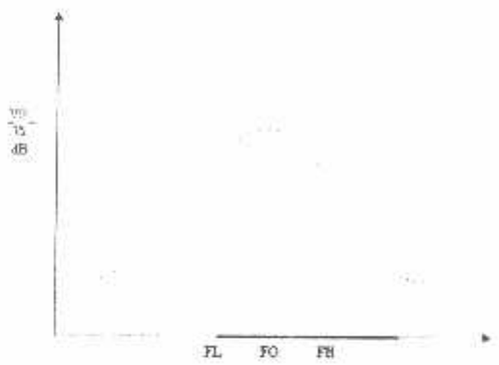
$$fc_o = \frac{1}{2\pi RC} \quad \text{..... (2-25)}$$

Persamaan ini berlaku untuk frekwensi atas maupun frekwensi bawah.

Dalam perancangan elektrokardiograf (EKG) *band pass filter* digunakan untuk mendapatkan range sinyal EKG yang diinginkan yang mana nantinya untuk

[12] "Penapis Aktif Elektronika", Teori dan Praktek, Hal : 33

frekwensi bawahnya (F_L) berkisar 0,16Hz dan untuk frekwensi atasnya (F_H) berkisar 234Hz.

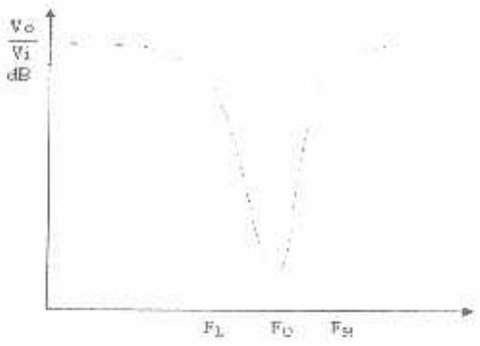


Gambar 2.13 Karakteristik Band Pass Filter [12]

2.5.4 *Band Reject Filter*

Band Reject Filter merupakan kebalikan dari *band pass filter*. Dari gambar karakteristiknya terlihat bahwa filter ini akan menahan sinyal-sinyal dengan frekwensi antara/median dan akan meneruskan sinyal-sinyal dengan frekwensi dibawah dan diatas frekwensi antara. Definisi lebar pita (BW) sama seperti pada *band pass filter*. Demikian juga dengan frekwensi atas (F_H) dan frekwensi bawah (F_L) sama dengan yang ada pada *band pass filter*. Banyak sekali jenis notch filter yang digunakan dalam perancangan instrumentasi elektronika. *Notch filter* disebut juga *band stop filter* atau *band reject filter* atau *band elimination*. Dalam perancangan instrumentasi bioelektrik *notch filter* digunakan untuk menekan noise sinyal dengan frekwensi 50Hz yang berasal dari jala-jala listrik PLN.

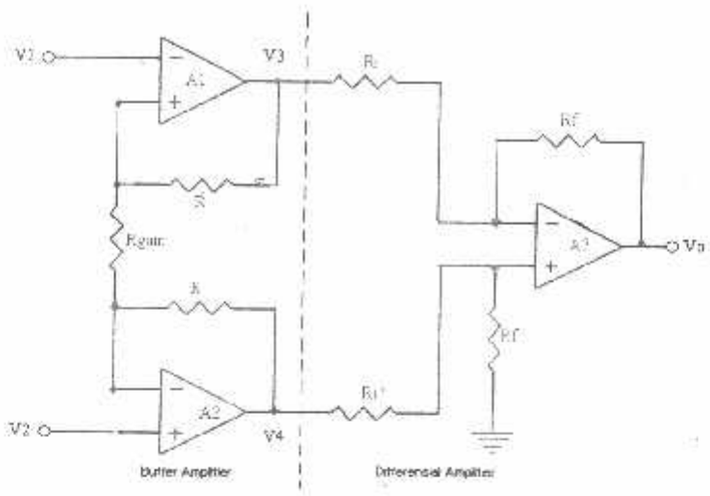
[12] "Penapis Aktif Elektronika", Teori dan Praktek, Hal : 33



Gambar 2.16 Karakteristik *Band Reject Filter*

2.6 Instrumentasi Amplifier

Penguat instrumentasi adalah salah satu penguat yang paling bermanfaat, cermat, dan serba guna yang ada pada saat ini. Penguat ini dibuat dari tiga penguat dan tujuh tahanan. Untuk menyerdehanakan analisis rangkaiannya, maka perlu diketahui bahwa sesungguhnya penguat instrumentasi dibuat dengan menghubungkan sebuah penguat penyangga (*buffer amplifier*) ke sebuah penguat differensial dasar. Suatu *Op-Amp* differensial amplifier memiliki input impedansi yang rendah yang mana dapat terpenuhi untuk sumber impedansi yang rendah seperti sebuah rangkaian jembatan pada strain gage. Tetapi sayangnya hal itu tidak dapat terpenuhi apabila sumber impedansi yang tinggi. Solusi yang dapat mengatasi masalah ini adalah dengan membuat rangkaian penguat instrumentasi seperti yang ditunjukkan pada gambar dibawah.



Gambar 2.15 Rangkaian Penguat Instrumentasi

Pada gambar diatas dapat dilihat bahwa V_3 dan V_4 adalah tegangan keluaran dari penguat penyangga yang dikerjakan oleh *Op-amp* A1 dan A_2, yang mana besarnya V_3 dan V_4 dapat dihitung dengan asumsi V3 = V4 yang mengakibatkan penguatannya selalu 1, sehingga :

$$V3,4=(V2-V1)(1+\frac{2R}{Rgain}) \quad \text{..... (2-26)}$$

Sedangkan penguatannya adalah :

$$A=1+\frac{2R}{Rgain} \quad \text{..... (2-27)}$$

Rangkaian penyangga diatas bekerja seperti *impedance converter* karena sinyal masukannya adalah sinyal AC yang mana disitu terdapat suatu impedansi Z yang rendah yang bila diberi beban akan mengalami tegangan drop/hilang sehingga dengan melewatkan sinyal tersebut pada rangkaian penyangga maka impedansi

sinyal masukan akan menjadi tinggi dan tidak akan terjadi drop/hilang bila diberi beban.

Oleh karena penguat differensial ini adalah penguatan bersama yang mana terdapat dua masukkan yang dikuatkan secara bersama-sama schingga ada dua penguatan yang mana perhitungannya adalah :

1. Penguatan *non-inverting* $\Rightarrow A = 1 + \frac{Rf}{Ri}$ ..... (2-28)

   Tegangan keluaran *non-inverting* $\Rightarrow Vo = V3\left(1 + \frac{Rf}{Ri}\right)$ ..... (2-29)

2. Penguatan *inverting* $\Rightarrow A = -\frac{Rf}{Ri}$ ..... (2-30)

   Tegangan keluaran *inverting* $\Rightarrow Vo = V4\left(-\frac{Rf}{Ri}\right)$ ..... (2-31)

2.7 Transduser

Transduser dalam instrumentasi medis adalah sangat penting karena mereka mengalami kontak langsung dengan pasien. Pada sebagian besar kasus, fungsi transduser untuk mengkonversi suatu parameter fisiologis yang dapat berupa suatu potensial lemah, tekanan, tingkatan aliran suatu fluida, temperatur, konsentrasi zat kimia dan jarak kedalam tegangan. Tegangan ini harus cukup besar untuk di analisa dan diproses oleh perangkat elektronik.

Berdasarkan dengan jenisnya transduser dapat dikelompokkan menjadi dua macam antara lain:

1. Transduser Pasif.

Transducer ini ini tidak dapat menghasilkan tegangan sendiri tetapi dapat menghasilkan perubahan nilai resistansi, kapasitansi, atau induktansi apabila mengalami perubahan kondisi sekeliling.

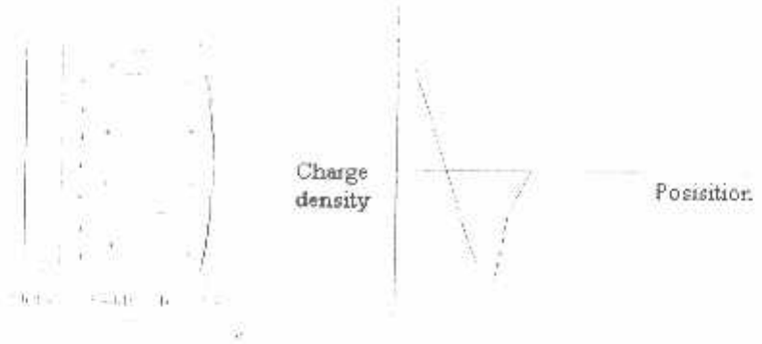
Jika transduser ini mengalami perubahan kondisi pada lingkungan sekelilingnya maka nilai resistnsinya akan berubah. Perubahan ini selanjutnya menyebabkan perubahan besar tegangan atau kuat arus yang dihasilkan trnsducer. Perubahan ini dapat bernilai positif (nilai resistansi bertambah) berarti tegangannya juga meningkat atau negatif (nilai resistansi berkurang) berarti tegangannya berkurang. Perubahan tegangan inilah yang dimanfaatkan untuk mengetahui keadaan yang ingin diukur.

2. Transduser Aktif.

Transducer ini tidak memerlukan catu daya eksternal. Transducer ini malah dapat menghasilkan energi listrik.

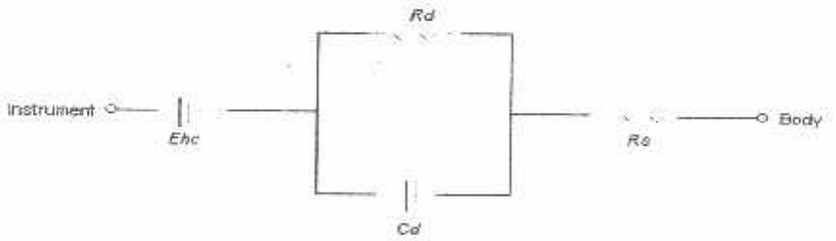
2.7.1 Prinsip Kerja Elektroda

Untuk dapat memahami prinsip kerja elektrode permukaan metal elektrolit maka kita perhatikan gambar 2-21. Potensial elektrode metal dibentuk oleh elektron-elektron yang meninggalkan cairan elektrolit dan masuk ke plat metal, peninggalan muatan elektron-elektron tersebut bervariasi seperti fungsi suatu posisi. Distribusi muatan ini serupa pada distribusi muatan pada kapasitor yang mana positif pada permukaan yang satu dan negatif pada permukaan yang lain [3].



Gambar 2.16 Distribusi Muatan Pada Elektroda Permukaan [13]

Oleh karena itu, rangkaian ekuivalen listrik untuk hubungan ini mengandung kapasitor, *Cd*. Distribusi muatan elektron-elektron ini juga menyebabkan suatu potensial listrik yang disebut *half-cell potential* (E_{hc}). Resistansi bocor *Rd* muncul disebcrang ekuivalen kapasitansi. Sebuah resistansi seri pada rangkaian ekuivalen *Rs* mengakibatkan aliran cairan elektrolit pada kesetimbangan muatan [13]. Rangkaian equivalen untuk elektroda permukaan ditunjukkan gambar dibawah :



Ehc - half-cell potential
Cd - electrode capacitance
Rd - leakage resistance
Rs - Series electrolyte and skin resistance

Gambar 2.17 Rangkaian Ekuivalen Elektroda Permukaan[14]

Impedansi elektrode pada rangkaian ekuivalen diatas diberikan oleh rumus untuk kombinasi impedansi, seperti berikut:

[13] Richard Aston,"Principles of Biomedical Instrumentation and Measurement", An Imprint of Macmillan Publishing Company, New York : 92
[14] Richard Aston,"Principles of Biomedical Instrumentation and Measurement", An Imprint of

$$Z = Rs + \frac{\frac{Rd}{j\,2\pi f\,Cd}}{Rd + \frac{1}{j\,\pi f\,Cd}}$$

Dari rumus diatas dapat di sederhanakan, sehingga :

$$Z = Rs + \frac{Rd}{1 + j\,2\pi f\,Cd\,Rd}$$

Rumusan impedansi ini memberikan suatu uraian yang tepat tentang perilaku listrik pada elektroda permukaan. Hal ini sangat penting untuk dicatat bahwa suatu impedansi adalah fungsi dari frekwensi.

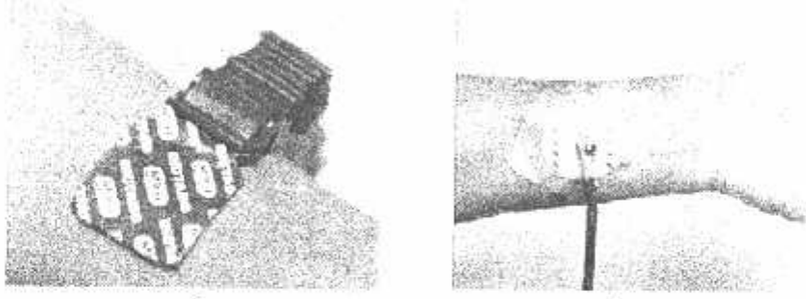
2.7.2 Elektroda Disposabel

Elektroda adalah transduser yang biasa digunakan pada sebuah instrumen amplifier bioelektrik. Elektroda bekerja dengan cara menarik potensial ion-ion tubuh melalui permukaan tubuh dan mengubah potensial ion-ion tersebut menjadi sinyal tegangan yang nantinya akan dikuatkan oleh rangkaian penguat instrumentasi. Suatu elektroda sebenarnya adalah transduser yang mengkopel potensial tegangan pada permukaan tubuh ke suatu perangkat elektronik (*instrument amplifier*) yang mana potensial pada tubuh berkisar antara 1μV untuk tengkorak atas, 1mV untuk bagian lengan dan 0.1V untuk bagian *exposed viscera* [15].

Pemakaian elektroda ada yang menembus kulit (*invasive*) seperti elektroda jarum dan ada elektroda permukaan yang tidak menembus kulit (*non invasive*). Jenis elektroda yang terakhir ini sering dipakai dalam lingkungan klinis karena memiliki resiko yang kecil seperti resiko infeksi penyakit maupun infeksi

[15] Richard Aston,"Principles of Biomedical Instrumentation and Measurement", An Imprint of Macmillan Publishing Company, New York : 89

akibat pemakaian elektroda itu sendiri. Permukaan elektroda ada yang terdiri dari plat metal yang dilapisi oleh cairan elektrolit atau berupa suatu plat metal yang yang terpisah dari permukaan tubuh oleh suatu insulator yang mana fungsinya menyerupai sebuah pengkopel [5]. Dalam perancangan akuisisi dan pemrosesan sinyal elektrokardiograf ini menggunakan elektroda *disposable*. Pemakaian elektroda ini ada yang direkatkan atau ditempelkan pada permukaan tubuh seperti stiker dan ada pula yang menggunakan penjepit/klip. Biasanya elektroda *disposable* yang direkatkan seperti stiker hanya dapat digunakan untuk sekali pemakaian saja karena perekatnya tidak tahan lama.



a b

Gambar 2.18 a. Elektroda Disposabel Dengan Penjepit
b. Elektroda Disposabel Dengan Perekat

2.8 Rangkaian Matrik LED

Terdapat banyak contoh dari penggunaan sistem matriks misalnya untuk menampilkan karakter-karakter, penggunaan pada tampilan layar CRT dan pada printer dot matrik. Beberapa tampilan informasi komersial menggunakan karakter matrik, dengan penambahan berupa lampu-lampu, tanda baca dan grafik-grafik.

Dalam perancangan Elektrokardiograf (*ECG*) ini rangkaian matrik LED digunakan sebagai penampil sinyal Elektrokardiografi pengganti osiloskop karena dengan penggunaan matrik LED memungkinkan untuk membuat suatu perangkat *ECG* secara portabel [15].

Umumnya semua matrik LED harus menggunakan sistem *scan form* untuk melengkapi tampilannya, untuk menghindari arus berlebihan. Faktor penyebab lainnya apabila LED tersebut menggunakan sistem *scan form* adalah dapat dikurangi jumlah port keluarannya. Pada saat LED-nya berjalan dalam sistem ini maka keseluruhan LED akan disapu secara bergantian dan sebenarnya semua LED mengalami saat padam dan saat nyala secara periodik akan tetapi mata manusia tidak dapat menangkap kedipan tersebut karena kecepatannya atau disebut fenomena optik. Pada saat terjadi *scan* maka hanya satu kolom saja yang akan diaktifkan pada suatu saat. Untuk dapat menampilkan secara lengkap maka *scan* tersebut harus diulang secara terus menerus secara bergantian dengan kecepatan tertentu, inilah yang disebut proses *scanning* [16].

Waktu *scanning* adalah waktu yang diperlukan untuk satu kali *scanning* bersama-sama antara data yang sinkron dengan sinyal scan, sehingga pada tampilan matrik LED akan tampak suatu karakter yang dimaksud. Namun penggunan matrik LED dalam perancangan ECG tidak digunakan untuk menampilkan suatu karakter melainkan suatu garis-garis yang membentuk gelombang secara kontinyu yang pada dasarnya gelombang tersebut sudah di proses oleh rangkaian penguat instrumentasi. Dengan waktu scan yang sangat cepat maka terlihat nyala LED yang konstan akan tetapi waktu tunda juga

[16] Buku Laporan Praktikum Mikroprosesor. Lab. Elka Digital. ITN Malang

diperlukan untuk setiap satu sinyal tersebut pada saat scanning agar LED tersebut dapat menyala dalam jangka waktu tertentu [6].

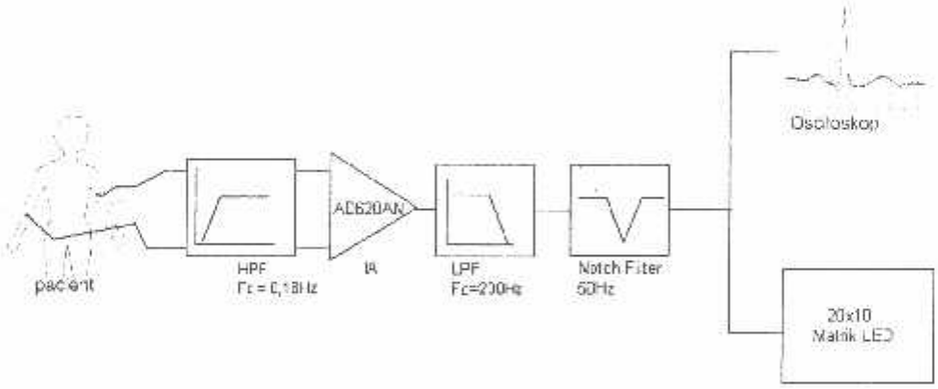
BAB III

PERANCANGAN DAN PEMBUATAN ALAT

Dalam bab ini akan dijelaskan mengenai perancangan dan pembuatan alat peng-akuisisi dan pemrosesan sinyal elektrokardiografi secara portabel dengan tampilan matrik LED. Dalam perancangan ini hanya membahas hardware dan tidak membahas software karena tidak menggunakan komponen – komponen elektronik yang mendukung pemakaian software.

3.1 Perancangan Alat

Perancangan alat yang akan dibuat ini dapat digambarkan secara blok diagram yang ditunjukkan oleh gambar dibawah.



Gambar 3.1 Blok Diagram Elektrokardiograf (EKG)

Keterangan Blok Diagram :

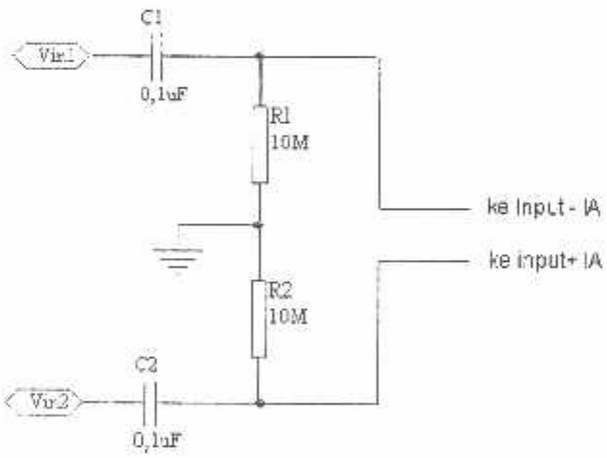
1. **Elektrode**. Berfungsi sebagai sensor yang bekerja dengan cara merubah potensial ionik akibat gerakan jantung melalui permukaan tubuh menjadi sinyal listrik yang berupa tegangan.

2. **HPF filter.** Rangkaian HPF berfungsi untuk menghilangkan atau memblok sinyal DC.
3. **Instrument Amplifier (IA).** Rangkaian ini merupakan rangkaian utama yang terdiri dari rangkaian *Impedance Converter* dan *Diffirensial Amplifier*. *Impedance converter* berfungsi seperti *buffer amplifier* yang mana memiliki impedansi input yang sangat tinggi sehingga dapat mengukur biopotensial jantung tanpa membebani tegangan yang diukur. *Differensial amplifier* berfungsi untuk mengambil dan menguatkan sinyal EKG dengan cara mengukur selisih tegangan antara dua sisi tubuh serta menghilangkan interferensi tegangan mode bersama (*common mode voltage*).
4. ***Low Pass Filter.*** Rangkaian ini berfungsi untuk membatasi frekwensi tinggi dan menahan frekwensi diatas frekwensi *cutoff*
5. **Band Reject Filter.** Rangkaian filter ini berfungsi untuk mereduksi/menekan noise dari frekwensi 50/60 Hz yang berasal dari jala-jala PLN.
6. **Rangkaian Matrik LED.** Blok ini terdiri rangkaian Matrik LED yang berfungsi untuk menggerakkan matrik LED secara bergantian sehingga dapat menampilkan data yang diinginkan (*output* dari IA). Matrik LED yang di gunakan adalah Matrik LED 20x10.

3.1.1. Perancangan *High Pass Filter*

Hal-hal yang mungkin perlu diperhatikan pada perancangan ini bahwa selain masukkan sinyal AC 1mV terdapat juga masukkan sinyal DC dari potensial offset elektroda yang besarnya sekitar ± 400mV dan noise elektroda yang menghasilkan frekwensi rendah 0,16Hz. Oleh karena terdapat juga sinyal masukkan DC dari potensial offset elektroda yang lebih besar dari sinyal bioelektrik jantung yang mana mungkin akan menyebabkan keluaran Op-Amp terjadi saturasi maka sinyal DC tersebut harus diblok/dibuang dengan menggunakan rangkaian *High Pass Filter (HPF)* dengan nilai R yang harus besar untuk menjaga arus DC kembali.

Dengan asumsi bahwa nilai R adalah 10M dan C1 = C2 = C maka rangkaian hasil perancangan HPF seperti gambar dibawah ini :



Gambar 3.2 Hasil Perancangan HPF Untuk *Input Instrument Amplifier*

Dari gambar diatas dapat dicari nilai kapasitor pengkopelnya dengan rumus :

$$f_c = \frac{1}{2\pi RC}$$

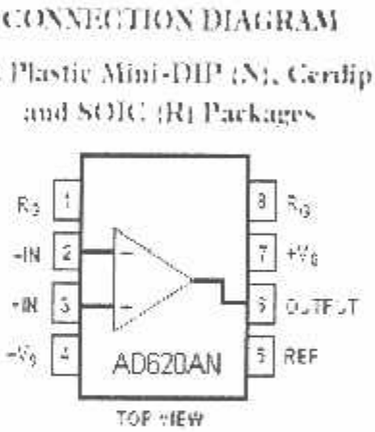
Sehingga,

$$C = \frac{1}{2\pi f_c R}$$

$$C = \frac{1}{2\pi . 0{,}16\text{Hz} . 10\text{M}}$$

$$C = 0{,}1\,\text{uF}$$

3.1.2 IC Instrumentasi Amplifier AD620AN

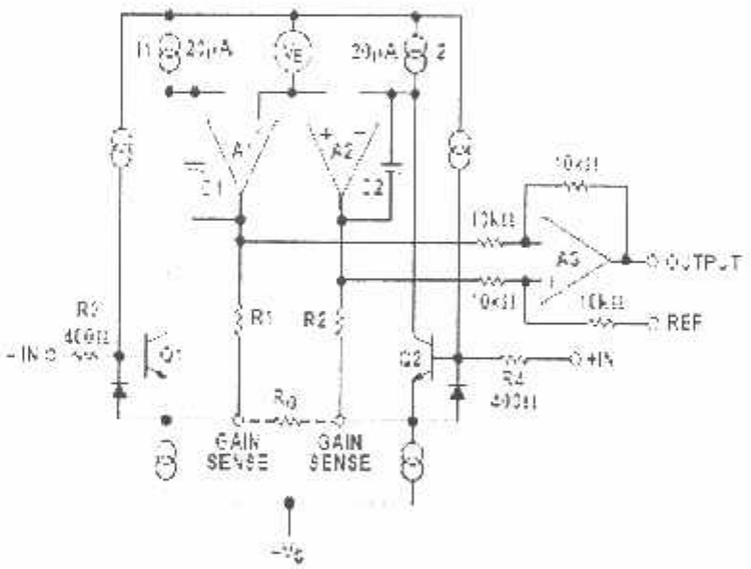


Gambar 3.3 Pin – pin IC AD620AN

AD620AN adalah IC monolitik yang dirancang khusus untuk melakukan tugas sebagai penguat instrumentasi yang presisi dan akurasi tinggi. Selain harganya cukup murah dan juga memiliki akurasi yang tinggi yang mana hanya membutuhkan eksternal resistor untuk penguatan 1 – 1000 kali dan memiliki

performa yang lebih baik daripada penguat instrumentasi 3 Op-Amp biasa. Beberapa kelebihan lain yang dimiliki IC IA AD620AN adalah memiliki noise yang rendah, arus bias input rendah dan konsumsi daya yang rendah (suplai arus maks 1,3mA) sehingga memungkinkan untuk membuat perangkat sistem akuisisi yang presisi seperti aplikasi medika (ECG, EEG, EMG, EOG dan pengukur tekanan darah) secara portabel dengan menggunakan baterai sebagai catu daya.

Oleh karena AD620AN adalah IC penguat instrumentasi maka dalam perancangan ini tidak perlu membuat rangkaian penguat instrumentasi biasa karena IC AD620AN telah dirancang khusus sebagai penguat instrumentasi dengan dasar rangkaian penguat instrumentasi klasik 3 Op-Amp.



Gambar 3.4 Skematik Sederhana IC AD620AN

Pada gambar diatas, diketahui dalam data sheet AD620 bahwa resistor internal R1 dan R2 sudah di set dengan nilai 24,7K Ohm, sehingga penguatan

pada buffer ditentukan dengan memberikan nilai R_G dengan perhitungan rumus sebagai berikut :

$$\text{Gain} = 1 + \frac{49.4K}{R_G}$$

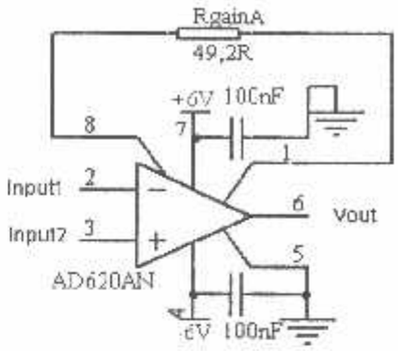
$$R_G = \frac{49,4K}{\text{Gain} - 1}$$

Untuk pedoman perancangan penguat instrumentasi dengan menggunakan AD620AN maka harus memperhatikan juga tabel yang telah diberikan produsen didalam data sheet AD620AN untuk menentukan nilai R_G pada penguatan yang diperlukan, seperti tabel berikut dibawah ini :

Tabel 3.1 Nilai RG dan Penguatannya Yang Disarankan Produsen AD620AN

1% Std Table Value of R_G, Ω	Calculated Gain	0.1% Std Table Value of R_G, Ω	Calculated Gain
49.9 k	1.990	49.3 k	2.002
12.4 k	4.984	12.4 k	4.984
5.49 k	9.998	5.49 k	9.998
2.61 k	19.93	2.61 k	19.93
1.00 k	50.40	1.01 k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003

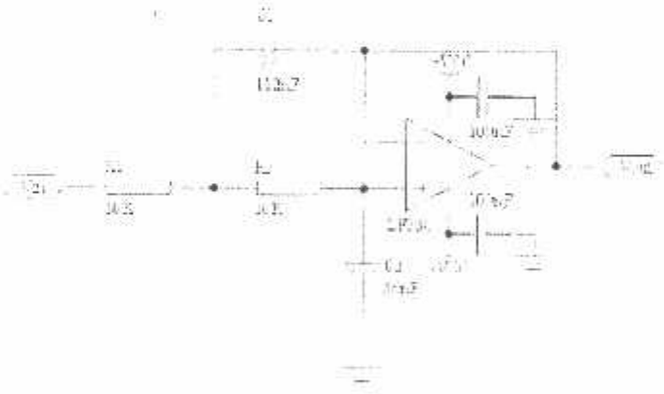
Adapun skema rangkaian hasil perancangan penguat instrumentasi ditunjukkan oleh gambar dibawah :



Gambar 3.5 Rangkaian Hasil Perancangan Penguat Instrumentasi

3.1.3. *Low Pass Filter*

Low Pass Filter dirancang untuk mendapatkan frekwensi *cutoff* (fc) atas dan menahan frekwensi diatas frekwensi *cutoff* tersebut. Rangkaian filter ini dirancang berdasarkan rangkaian *Sallen-Key Low Pass Filter* agar didapatkan landaian yang tajam dan *noise* yang lebih rendah



Gambar 3.6 Hasil Perancangan *Sallen-Key Low Pass Filter*

Untuk nilai komponen-komponen rangkaian diatas, R1 = R2 ; C1 = 2C2, sehingga dengan menetapkan nilai R1 = 10K dan nilai C2 = 56nF dan C3 = 112nF maka frekwensi *cutoff*-nya dapat dihitung dengan rumus :

$$fc = \frac{1}{2\pi\sqrt{R_1.R_2.C_1.C_2}}$$

$$fc = \frac{1}{2\pi\sqrt{R_1.R_2.C_1.C_2}}$$

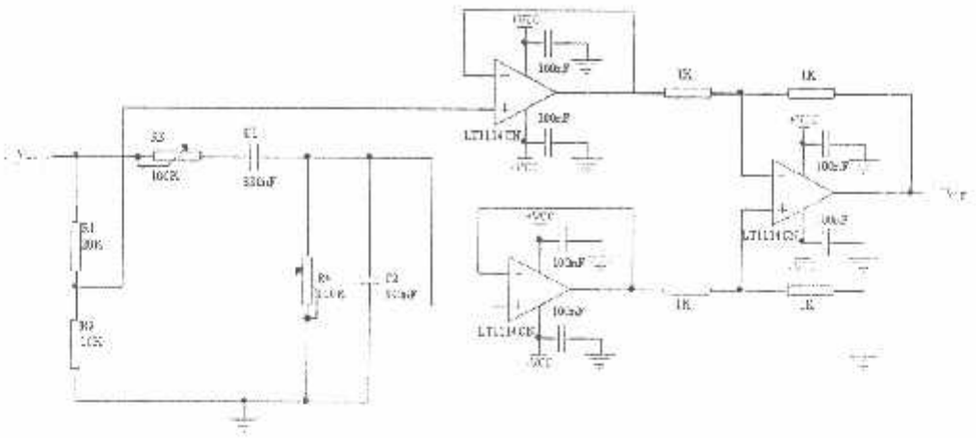
$$fc = \frac{1}{6.28\sqrt{10K.10K.56nF.112nF}}$$

$$fc = 201Hz = 200Hz$$

Dengan demikian dari rangkaian *high pass filter* yang telah dirancang sebelumnya maka rangkaian ECG ini memiliki *bandwidth* 0,16Hz – 200Hz.

3.1.4. *Band Reject Filter*

Sering kali pada saat menguji suatu alat elektronik muncul sinyal yang tidak diinginkan yang berasal dari jala-jala listrik PLN dengan frekwensi 50Hz, sehingga sinyal yang akan diukur bercampur dengan sinyal 50Hz. Meskipun sumber daya dari rangkaian elektronik yang digunakan menggunakan baterai namun interferensi frekwensi 50Hz ada dimana-mana tanpa kita sadari, terutama jika berdekatan dengan jala-jala listrik PLN. Rangkaian *Band Reject Filter* berfungsi untuk menekan *noise* frekwensi 50Hz yang berasal dari jala-jala PLN tersebut tanpa mengganggu bentuk gelombang sinyal ECG yang mempunyai range frekwensi hingga diatas 100Hz. Rangkaian *Band Reject Filter* dapat dibuat dengan rangkaian jembatan R dan C untuk mendapatkan frekwensi *null*-nya yang nantinya menggunakan sebuah *differensial amplifier* untuk mengukur frekwensi *null* tersebut. Adapun rangkaian dari *Band Reject Filter* hasil perancangan ditunjukkan pada gambar dibawah :



Gambar 3.7 Hasil Perancangan Rangkaian *Band Reject Filter*

Dari gambar diatas dapat dihitung frekwensi null-nya dengan rumus :

$$F_N = \frac{1}{2\pi R_3 C_1}$$

Dimana :

$R_3 = R_4$, $C_1 = C_2$

$R_2 = 0{,}5\ R_1$

Dengan asumsi bahwa nilai R1 = 20K maka R2 = 10K dan C1 = C2 = 0,33uF, sehingga dapat dicari nilai R3 =R4 dengan rumus diatas :

$$F_N = \frac{1}{2\pi R_3 C_1}$$

$$R_{3,4} = \frac{1}{2\pi F_N R1}$$

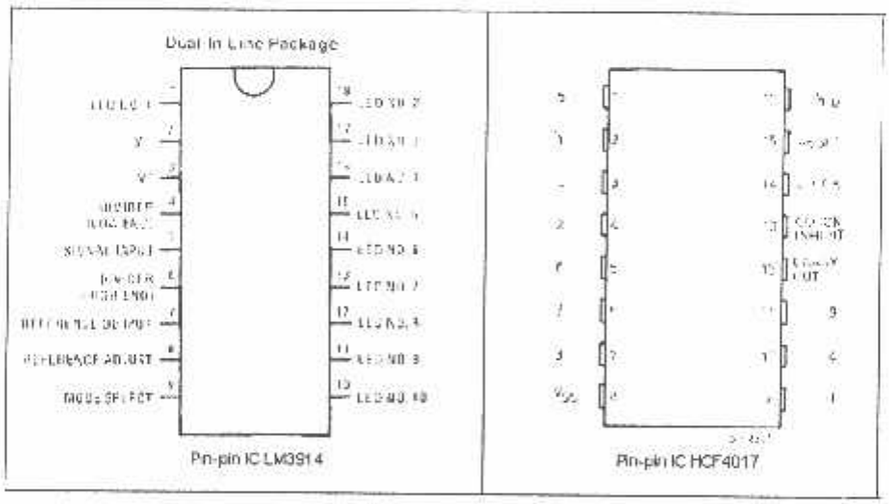
$$R_{3,4} = \frac{1}{6{,}28.50\text{Hz}.0{,}33\text{uF}}$$

$$R_{3,4} = 9{,}65\text{K}$$

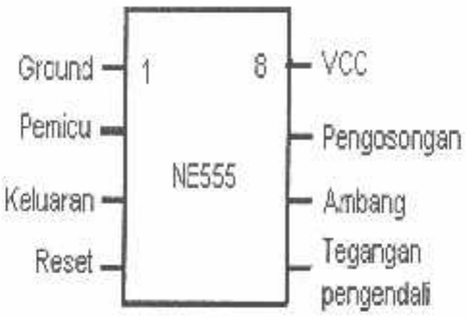
Untuk mendapatkan frekwensi null yang benar-benar pada 50Hz maka R3 dan R4 dibuat variabel agar dapat disetel frekwensinya (*adjustable frequency*). Penguatan rangkaian filter diatas adalah -1.

3.1.5. Rangkaian Matrik LED

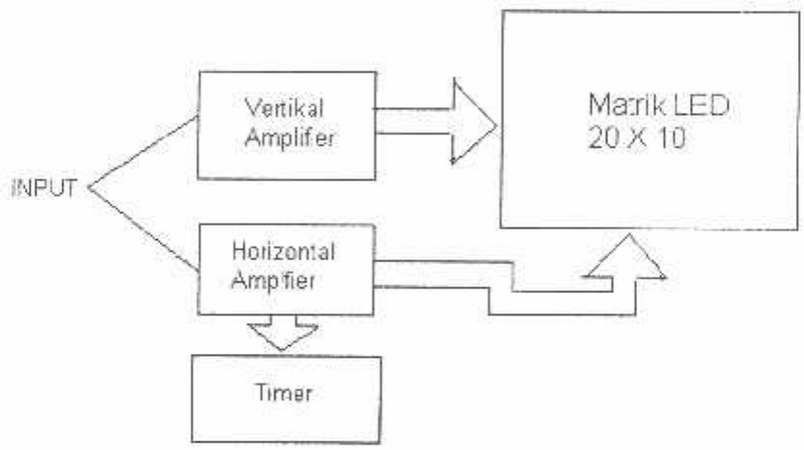
Dalam perancangan dan pembuatan ECG ini, matrik LED digunakan untuk menampilkan sinyal ECG yang fungsinya layaknya *oscilloscope*. Maksudnya adalah bahwa alat yang hendak dirancang ini dapat dibuat secara portabel dan lebih sederhana. Agar dapat berfungsi dengan baik maka matrik LED digerakkan oleh 3 buah IC driver yang terdiri dari IC *10 Dot/Bar display driver* LM3914, *Decade counter 10 Decoded Output* HCF4017, dan *timmer* NE555. Konfigurasi dari kaki-kaki IC LM3914 dan HCF4017 digambarkan seperti gambar dibawah :



Gambar 3.8 Konfigurasi Pin-pin IC LM3914 dan IC HCF4017

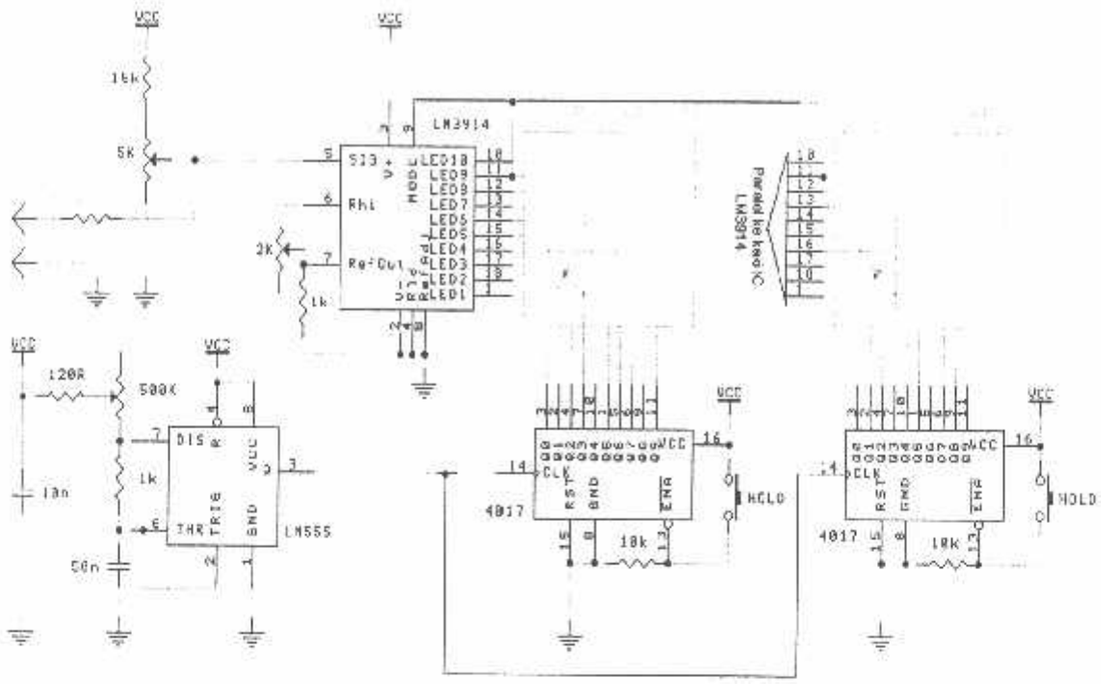


Gambar 3.9 Konfigurasi Pin-pin IC NE555



Gambar 3.10 Blok Diagram Rangkaian Matrik LED

Adapun skema rangkaian osilloskop matrik LED secara lengkap digambarkan seperti gambar dibawah :



Gambar 3.11 Hasil Perancangan Osiloskop Matrik LED

Secara singkat dapat dijelaskan prinsip kerja dari rangkaian diatas bahwa setiap sinyal yang masuk melalui *probe* maka keluaran dari IC LM3914 akan memberikan level-level tegangan sinyal keluaran melalui pin 1-10 secara vertikal ke kaki anoda LED-LED. Resistor variabel (VR) 2K di setel untuk mengatur amplitudo sinyal. Kemudian level-level tegangan tadi akan di geser berurutan secara horizontal satu persatu oleh IC HCF4017 melalui kaki katode LED. Agar level-level tegangan tadi dapat dilihat maka matrik LED ini harus mengalami proses *scanning* secara kontinyu, sedangkan proses penggeseran dikendalikan oleh sebuah rangkaian *astable multivibrator* IC NE555 melalui pin *clock* IC HCF4017

Kecepatan scanning ini berpengaruh pada perubahan frekwensi osilasi dan dapat diatur dengan memutar resistor variabel 500K pada rangkaian *astabel*

multivibrator 555. Dengan demikian sinyal yang dimaksud akan dapat ditampilkan oleh matrik LED. Untuk menjaga agar rangkaian matrik LED tidak rusak karena arus masukkan yang besar maka pada masukkanya diseri dengan resistor 10K, selain itu resistor tersebut untuk memberi impedansi masukkan yang dimaksudkan untuk mengurangi efek pembebanan. Rangkaian pembagi tegangan yang terhubung dengan resistor masukkan akan menjaga agar sinyal masukkan tetap berada didaerah positif. Rangkaian matrik LED ini memiliki resolusi yang rendah sehingga penampilan sinyal mungkin tidak sejelas osiloskop yang asli. Namun demikian didalam uji coba rangkaian ini mampu menampilkan sinyal hingga pada frekwensi 500Hz tanpa masalah berarti sehingga masih memungkinkan untuk dapat menampilkan sinyal ECG. Sesuai data sheet LM555 untuk rangkaian *astable multivibrator* maka VR 500K sebagai nilai R_A dan resistor 1K sebagai R_B dan nilai C = 50nF sehingga frekwensi osilasi dapat dicari dengan rumus :

$$F = \frac{1,44}{(R_A + 2R_B)C}$$

Oleh karena nilai R_A dibuat variabel maka besarnya frekwensi osilasi sangat bergantung pada pengaturan nilai R_A tersebut.

BAB IV
PENGUJIAN DAN ANALISA

Bab ini akan membahas pengukuran dan pengujian alat yang telah dibuat. Pengukuran dan pengujian dilakukan pada setiap blok-blok rangkaian ECG dan kemudian dianalisa.

4.1. Pengukuran Penguat Instrumentasi

Pengukuran penguat instrumentasi ini meliputi pengukuran *diffrential mode* (DM) dan pengukuran *common mode* (CM) serta mengetahui besarnya *common mode rejection ratio* (CMRR).

4.1.1. Tujuan

Pengukuran ini bertujuan apakah penguat instrumentasi bekerja sesuai yang diharapkan atau tidak

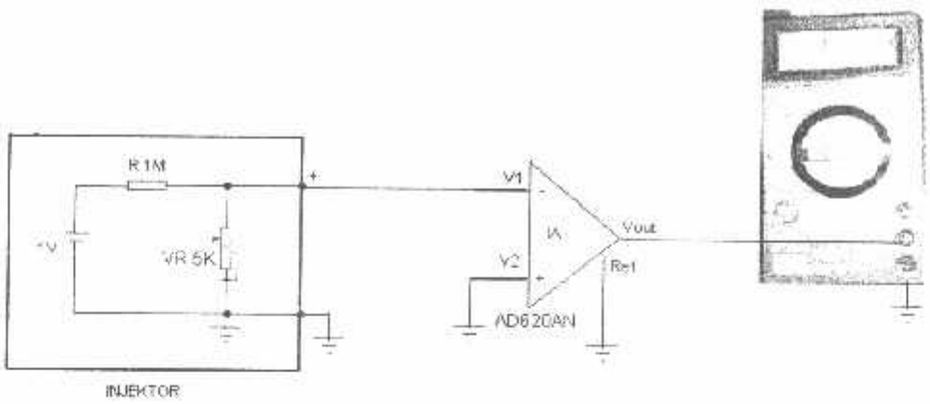
4.1.2. Peralatan Yang Digunakan

1. Multimeter
2. Catu daya DC simetris 6V
3. Rangkaian penguat instrumentasi
4. Injektor

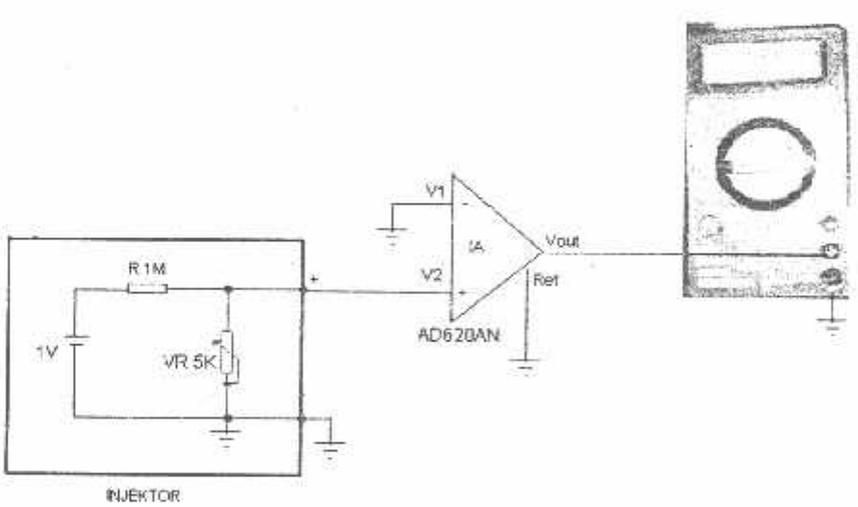
4.1.3. Prosedur Pengukuran

1. Mengukur keluaran injektor
2. Merangkai peralatan seperti pada gambar 4-1 sampai 4-4
3. Mengamati keluaran penguat instrumentasi pada multimeter

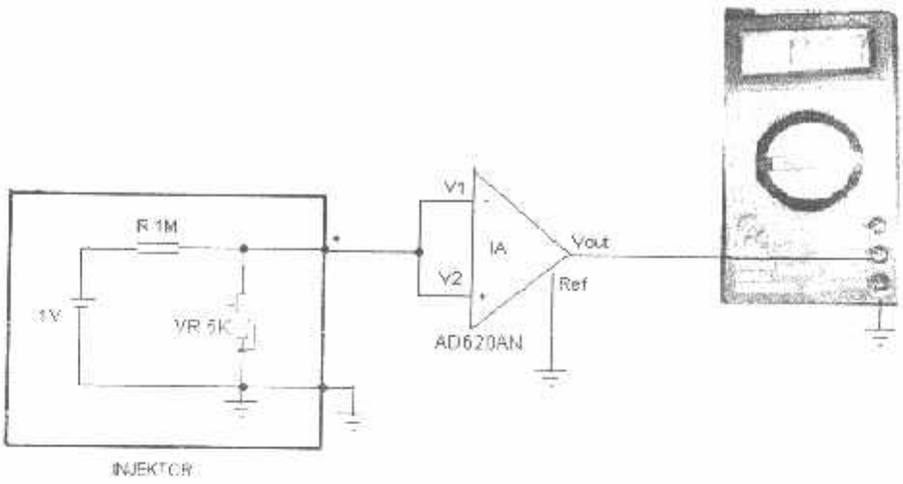
4. Mencatat tegangan yang tertera pada multimeter



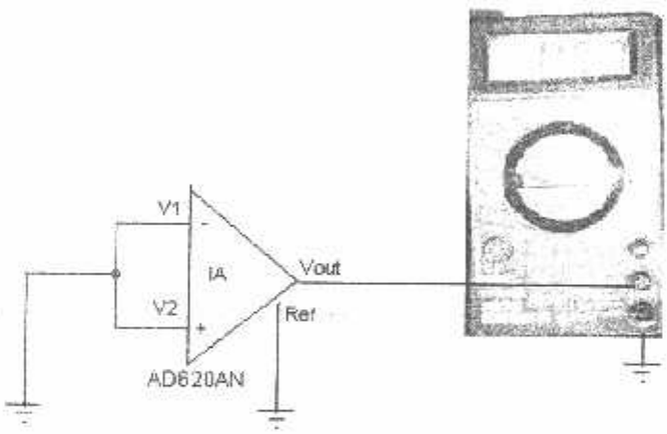
Gambar 4.1 Rangkaian Pengukuran *Differential Mode* (DM) Penguat Instrumentasi Dengan Masukkan + Diground



Gambar 4.2 Rangkaian Pengukuran *Differential Mode* (DM) Penguat Instrumentasi Dengan Masukkan – Diground



Gambar 4.3 Rangkaian Pengukuran Penguat Instrumentasi Tegangan Masukkan Sama (*Common Mode* (CM))



Gambar 4.4 Rangkaian Pengukuran Penguat Instrumentasi dengan 2 Masukkan Terground (0V) (*Common Mode* (CM))

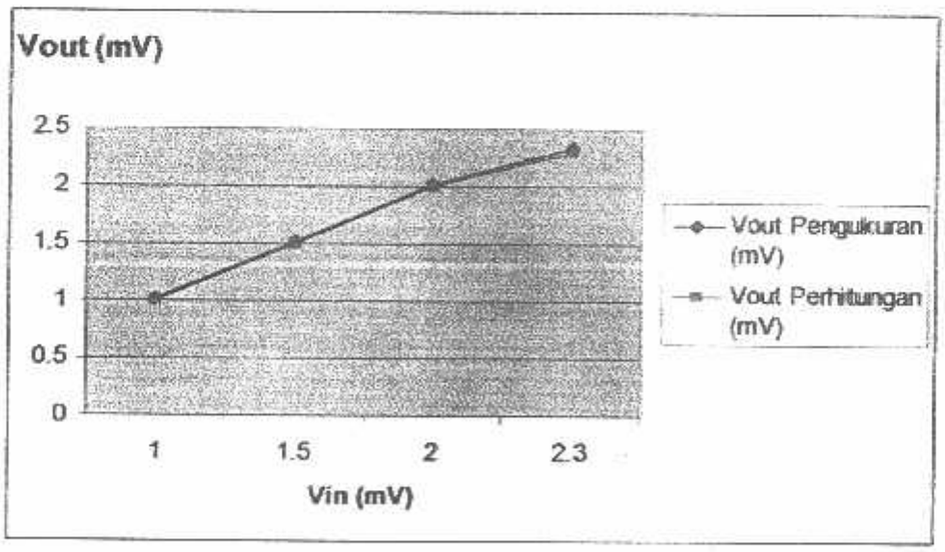
4.1.4. Hasil Pengukuran

Hasil pengukuran penguat instrumentasi tertera pada tabel berikut ini :

Tabel 4.1 Hasil Pengukuran dan Pengujian Penguat Instrumentasi

$-V_1$ (mV)	$+V_2$ (mV)	GAIN (kali)	Vout Perhitungan (mV)	Vout Pengukuran (mV)
1	0	1000	1	-1.01*
1.5	0	1000	1.5	-1.51*
2	0	1000	2	-2.02*
2.3	0	1000	2.3	-2.33*
0	2.3	1000	2.3	2.34
0	2	1000	2	2.04
0	1.5	1000	1.5	1.52
0	1	1000	1	1.02
0	0	1000	0	0.0075

* Menandakan inputnya inversi



Grafik 4.1 Karakteristik Vin Terhadap Vout Pengukuran dan Vout Perhitungan

4.1.5. Perhitungan Tegangan Keluaran *Differensial Mode* (*DM*)

$$Vout = (V2 - V1)\,\text{Gain}$$

Sehingga dari data pengukuran diatas dapat dihitung Vout-nya dengan perhitungan berikut :

* Untuk $V_1 = 0V$, $V_2 = 1mV$

$$Vout = (0V - 1mV)1000$$
$$= -1V$$

* Untuk $V_1 = 0V$, $V_2 = 1.5mV$

$$Vout = (0V - 1.5mV)1000$$
$$= -1.5V$$

* Untuk $V_1 = 0V$, $V_2 = 2mV$

$$Vout = (0V - 2mV)1000$$
$$= -2V$$

* Untuk $V_1 = 0V$, $V_2 = 2.3mV$

$$Vout = (0V - 2.3mV)1000$$
$$= -2.3V$$

4.1.6. Perhitungan Tegangan Keluaran *Common Mode* (CM)

* Untuk $V_1 = 0V$, $V_2 = 2.3mV$

$$Vout = (0V - 0V)1000$$
$$= 0V$$

4.1.7. Perhitungan Prosentase *Error* Pengujian dan Pengukuran Penguat Instrumentasi

$$\%\,Error = \frac{Vout\ \text{pengukuran} - Vout\ \text{perhitungan}}{Vout\ \text{pengukuran}} \times 100\%$$

Sehingga dari data pengukuran diatas didapatkan besar *error* dengan perhitungan berikut :

* Untuk $+V_1 = 1mV$, $-V_2 = 0V$

$$\%\ Error = \frac{1.01V - 1V}{1.01V} \times 100\%$$
$$= 0.009\%$$

* Untuk $+V_1 = 1.5mV$, $-V_2 = 0V$

$$\%\ Error = \frac{1.51V - 1.5V}{1.51V} \times 100\%$$
$$= 0.006\%$$

* Untuk $+V_1 = 2mV$, $-V_2 = 0V$

$$\%\ Error = \frac{2.02V - 2V}{2.02V} \times 100\%$$
$$= 0.009\%$$

* Untuk $-V_1 = 2.3mV$, $-V_2 = 0V$

$$\%\ Error = \frac{2.33V - 2.3V}{2.33V} \times 100\%$$
$$= 0.01\%$$

* Untuk $+V_1 = 0V$, $-V_2 = 2.3mV$

$$\%\ Error = \frac{2.34V - 2.3V}{2.34V} \times 100\%$$
$$= 0.01\%$$

* Untuk $+V_1 = 0V$, $-V_2 = 2mV$

$$\%\ Error = \frac{2.04V - 2V}{2.04V} \times 100\%$$
$$= 0.01\%$$

* Untuk $+V_1 = 0V$, $-V_2 = 1.5mV$

$$\%\ Error = \frac{1.52V - 1.5V}{1.52V} \times 100\%$$
$$= 0.01\%$$

* Untuk $+V_1 = 0V$, $-V_2 = 1mV$

$$\%\ Error = \frac{1.02V - 1V}{1.02V} \times 100\%$$
$$= 0.01\%$$

4.1.8. Perhitungan *Common Mode Rejection Ratio* (CMRR)

Pengukuran *Common Mode Rejection Ratio* (CMRR) bertujuan untuk mengetahui seberapa baik penguat instrumentasi me-*reject* suatu *common mode signal*. Perhitungan CMRR dapat dirumuskan dengan rumus berikut :

$$CMRR = 20\ Log\ \frac{Ad}{Common\ Mode\ /\ Differential\ Mode}\ dB$$

Sehingga dari data pengukuran diatas maka dapat dihitung besar CMRR dengan perhitungan berikut :

* Untuk $+V_1 = 1mV$, $-V_2 = 0V$

$$CMRR = 20\ Log\ \frac{1000}{0.0075 / 1.01}\ dB$$
$$= 102\ dB$$

* Untuk $+V_1 = 1.5mV, -V_2 = 0V$

$$CMRR = 20\ Log\ \frac{1000}{0.0075/1.51}\ dB$$
$$= 106\ dB$$

* Untuk $+V_1 = 2mV, -V_2 = 0V$

$$CMRR = 20\ Log\ \frac{1000}{0.0075/2.02}\ dB$$
$$= 108.6\ dB$$

* Untuk $+V_1 = 2.3mV, -V_2 = 0V$

$$CMRR = 20\ Log\ \frac{1000}{0.0075/2.33}\ dB$$
$$= 109.8\ dB$$

* Untuk $+V_1 = 0V, -V_2 = 2.3mV$

$$CMRR = 20\ Log\ \frac{1000}{0.0075/2.34}\ dB$$
$$= 109.8\ dB$$

* Untuk $+V_1 = 0V, -V_2 = 2mV$

$$CMRR = 20\ Log\ \frac{1000}{0.0075/2.04}\ dB$$
$$= 108.8\ dB$$

* Untuk $+V_1 = 0V, -V_2 = 1.5mV$

$$CMRR = 20\ Log\ \frac{1000}{0.0075/1.52}\ dB$$
$$= 106\ dB$$

* Untuk $+V_1 = 0V, -V_2 = 1mV$

$$CMRR = 20\ Log\ \frac{1000}{0.0075/1.02}\ dB$$
$$= 102\ dB$$

Untuk selanjutnya, dari perhitungan diatas maka dapat dibuat tabel hasil perhitungan seperti berikut :

Tabel 4.2 Hasil Perhitungan Penguat Instrumentasi

$-V_1$ (mV)	$+V_2$ (mV)	GAIN (kali)	Vout Perhitungan (mV)	Vout Pengukuran (mV)	Error (%)	CMRR (dB)
1	0	1000	1	-1.01*	0.009	102
1.5	0	1000	1.5	-1.51*	0.006	106
2	0	1000	2	-2.02*	0.009	108.8
2.3	0	1000	2.3	-2.33*	0.01	109.8
0	2.3	1000	2.3	2.34	0.01	109.8
0	2	1000	2	2.04	0.01	108.8
0	1.5	1000	1.5	1.52	0.01	106
0	1	1000	1	1.02	0.01	102
0	0	1000	0	0.0075	-	-
		Jumlah	**13.6**	**13.80**	**0.074**	**853.2**

Dari data tabel diatas, maka dapat dihitung Vout rata-rata, yaitu :

$$\textit{Vout}\ \text{pengukuran rata - rata} = \frac{13.80\text{V}}{9} = 1.53\text{V}$$

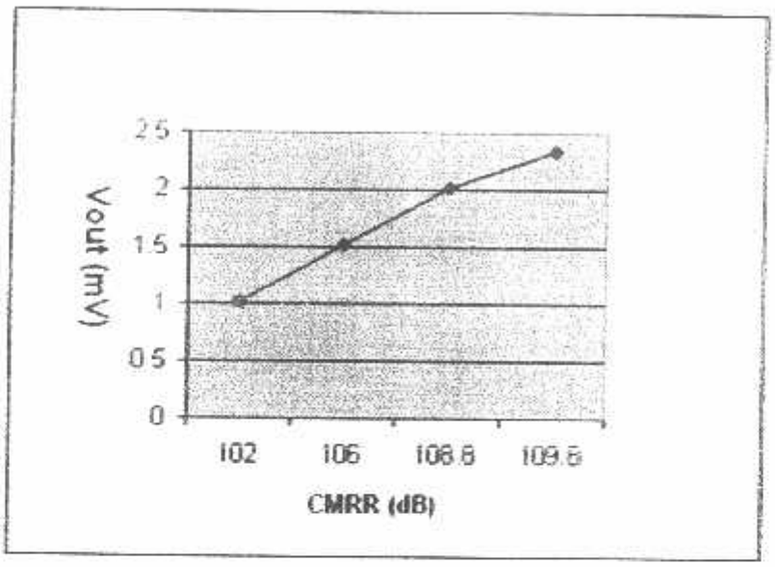
$$\textit{Vout}\ \text{perhitungan rata - rata} = \frac{13.6\text{V}}{9} = 1.51\text{V}$$

Sedangkan prosentase *error* rata-rata adalah :

$$\%\ \textit{error}\ \text{rata - rata} = \frac{1.53\text{V} - 1.51\text{V}}{1.53\text{V}}\ 100\,\% = 0.01\%$$

Untuk CMRR rata rata adalah :

$$\text{CMRR rata - rata} = \frac{853.2\text{dB}}{8}$$
$$= 106,65\text{ dB}$$



Grafik 4.2 Karakteristik CMRR Penguat Instrumentasi Terhadap Vout Pengukuran

4.2. Pengujian Rangkaian *LowPass Filter*

4.2.1. Tujuan

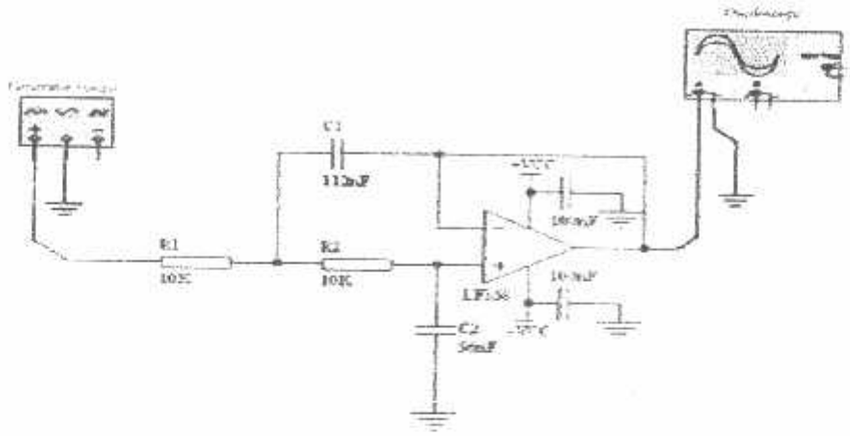
Tujuan dari pengujian rangkaian *low pass filter* adalah untuk mengetahui hasil dari pemguatan sinyal yang dihasilkan

4.2.2. Peralatan Yang Digunakan

1. *Power supply*
2. Generator fungsi
3. *Osciloscope*

4.2.3. Prosedur Pengujian

1. Rangkaian dibuat seperti pada gambar 4-5
2. Mengamati hasil keluaran pada *low pass filter*

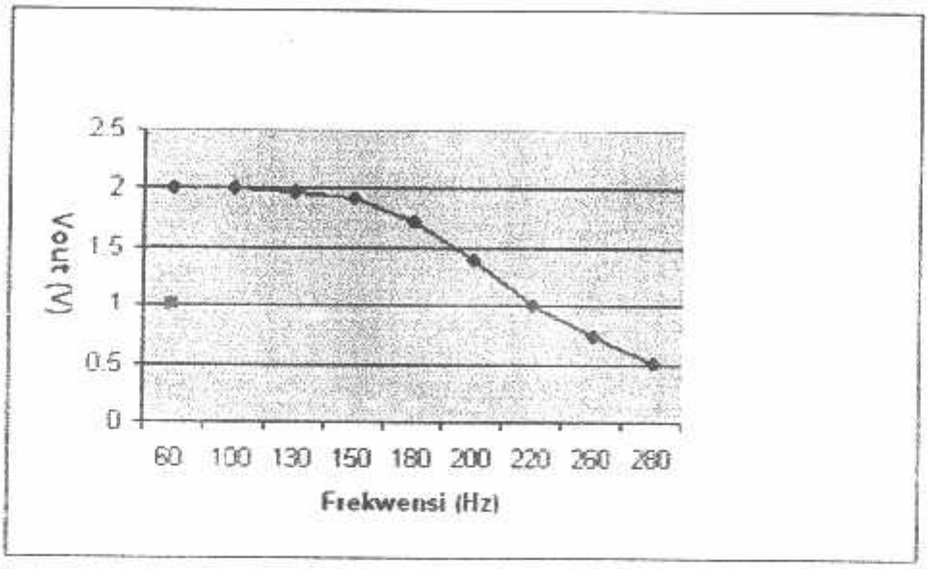


Gambar 4.5 Rangkaian Pengujian *Low Pass Filter*

4.2.4. Hasil Pengujian

Tabel 4.3 Hasil Pengukuran *Low Pass Filter*

Frekwensi (Hz)	Vin (V)	Vout (V)	V/Div (V)	T/Div (ms)
60	2	2	1	10
100	2	2	1	10
130	2	1.98	1	10
150	2	1.92	1	10
180	2	1.73	1	10
200	2	1.39	1	10
220	2	1	1	10
260	2	0.743	1	10
280	2	0.518	1	10



Grafik 4.2 Karakteristik *Low Pass Filter*

4.3. Pengujian Rangkaian *Band Reject Filter*

4.3.1. Tujuan

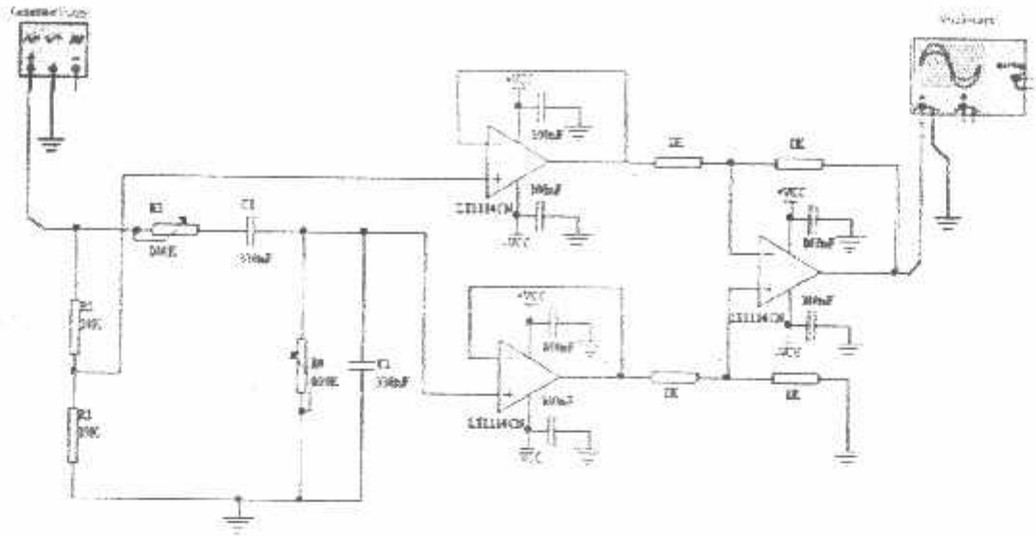
Tujuan dari pengujian rangkaian *band reject filter* adalah mengetahui apakah dapat menekan frekwensi 50Hz

4.3.2. Peralatan Yang Digunakan

1. *Power supply*
2. Generator fungsi
3. *Osciloscope*

4.2.3. Prosedur Pengujian

1. Rangkaian dibuat seperti pada gambar 4-6.
2. Mengamati hasil keluaran pada *band reject filter*



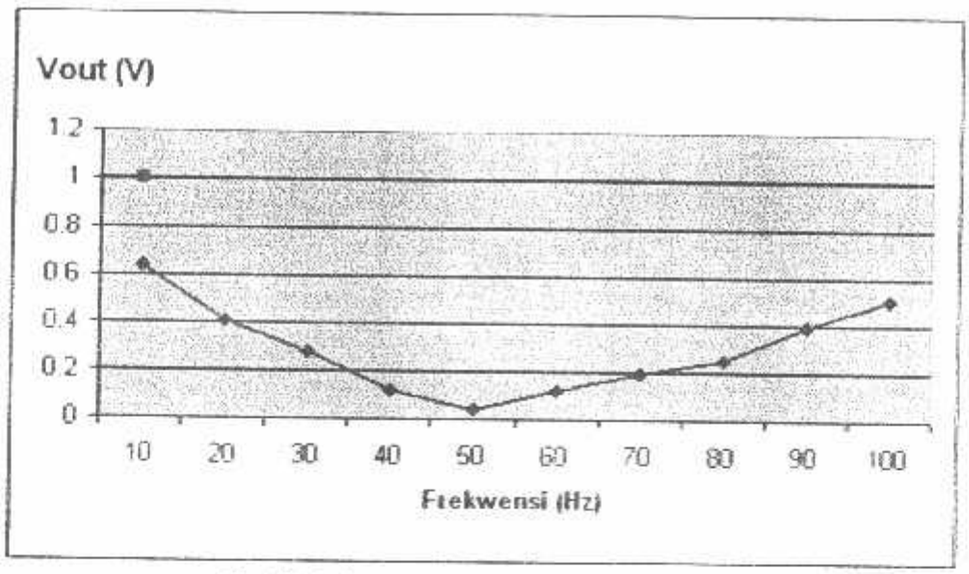
Gambar 4.6 Rangkaian Pengujian *Band Reject Filter*

4.2.4. Hasil Pengujian

Hasil pengujian rangkaian *band reject filter* ditunjukkan tabel dibawah :

Tabel 4.4 Hasil Pengukuran *Band Reject Filter*

Frekwensi (Hz)	Vin (V)	Vout (V)	V/Div (V)	T/Div (ms)
10	1	0.643	1	10
20	1	0.406	1	10
30	1	0.281	1	10
40	1	0.121	1	10
50	1	0.044	1	10
60	1	0.121	1	10
70	1	0.191	1	10
80	1	0.252	1	10
90	1	0.391	1	10
100	1	0.506	1	10



Grafik 4-3. Tanggapan *Band Reject Filter*

4.3. Pengujian Rangkaian Matrik LED

4.3.1 Tujuan

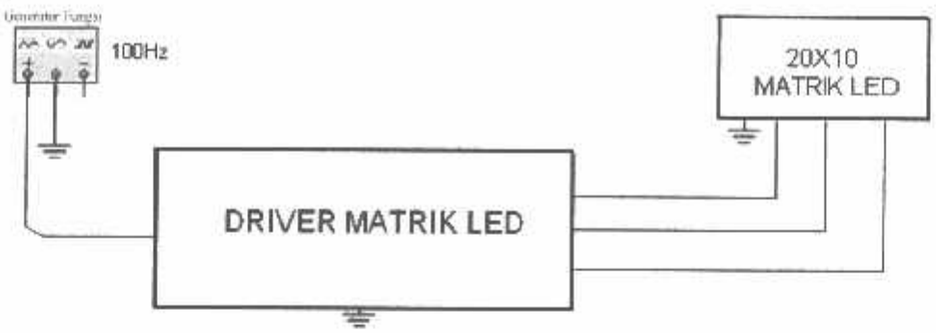
Tujuan dari pengujian rangkaian matrik LED ini adalah untuk mengetahui apakah matrik LED dapat menampilkan sinyal tegangan.

4.3.2. Peralatan Yang Digunakan

1. Power supply
2. Osilloskop
3. Generator fungsi

4.3.3. Prosedur Pengujian

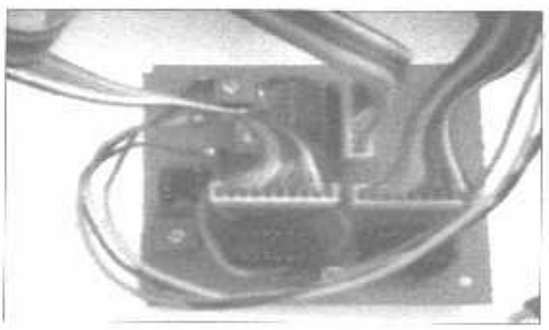
3. Rangkaian dibuat seperti pada gambar 4-10.
4. Mengamati sinyal yang ditampilkan matrik LED



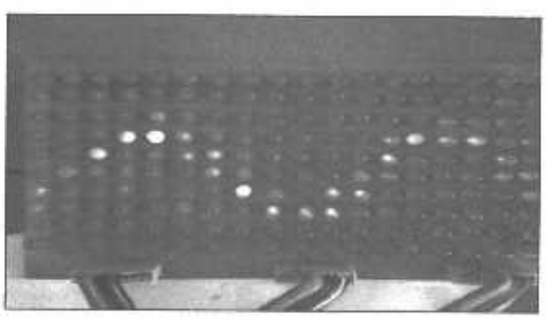
Gambar 4.7 Rangkaian Pengujian Matrik LED

4.3.4. Hasil Pengujian

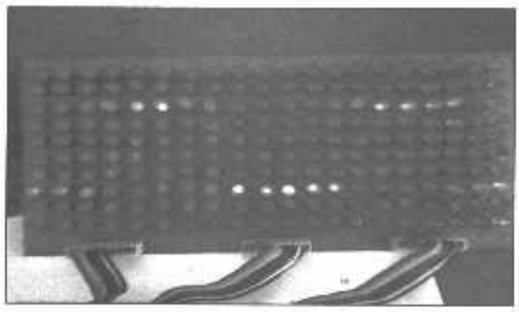
Hasil pengujian matrik LED ditunjukkan gambar dibawah :



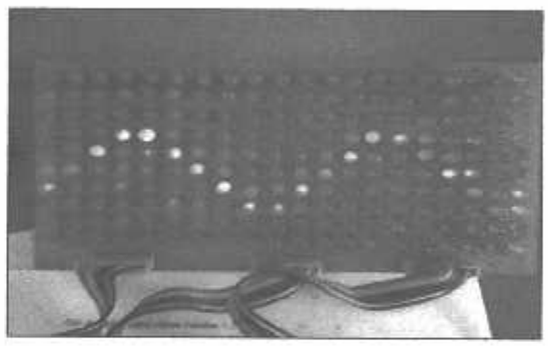
Gambar 4.8 Rangkaian Driver Matrik LED



Gambar 4.9 Hasil Pengujian Matrik LED Dengan Sinyal Masukkan Segitiga Pada Frekwensi 100Hz



Gambar 4.10 Hasil Pengujian Matrik LED Dengan Sinyal Masukkan Kotak Pada Frekwensi 100Hz



Gambar 4.11 Hasil Pengujian Matrik LED Dengan Sinyal Masukkan Sinus Pada Frekwensi 100Hz

4.5. Pengujian Rangkaian Secara Keseluruhan

Pengujian ini adalah pengujian utama dalam perancangan dan pembuatan alat pengakuisisi sinyal ECG.

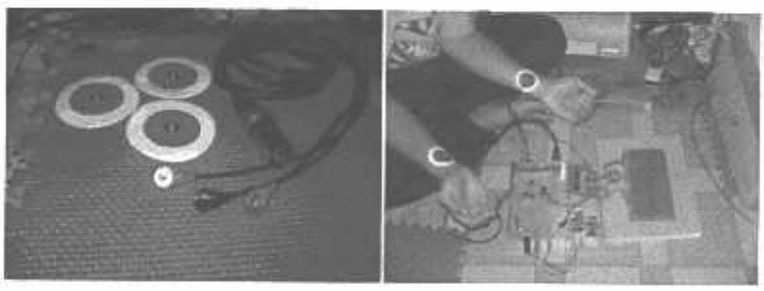
4.5.1 Tujuan

Mendapatkan sinyal ECG dengan menggunakan penguat yang telah dirancang sehingga mengetahui apakah alat tersebut dapat bekerja sesuai

rancangan. Pertama-tama alat ini akan di uji dengan menggunakan penampil osilloskop.

4.5.2 Prosedur Pengujian :

1. Membersihkan bagian kulit yang akan ditempati elektroda dengan alkohol.
2. Setelah kulit kering, tempelkan elektroda dikulit yang telah dibersihkan.
3. Menghubungkan kabel input yang sudah terhubung dengan rangkaian ECG ke pin elektroda.
4. Mengidupkan power supply
5. Menunggu beberapa detik sampai tidak berubah-ubah
6. Memperhatikan layar osiloskop dan mengamati sinyal yang tertampil pada matrik LED.
7. Coba mengidentifikasi sinyal ECG .



Gambar 4.12 Pemasangan Elektroda Dan Alat

4.5.2 Hasil Pengujian

Setelah diadakan pengujian secara keseluruhan, alat ini belum dapat menangkap sinyal ECG. Dari beberapa kali percobaan maka dapat dianalisa bahwa penyebab tidak dapatnya alat ini menangkap sinyal bioelektrik jantung dikarenakan permasalahan masukkan dari alat ECG, misalnya cara-cara pemasangan elektroda yang tidak benar atau pemilihan kabel input yang kurang tepat. Selain itu, kualitas elektroda juga sangat mempengaruhi sensivitas dalam penangkapan sinyal bioelektrik.

4.6 Spesifikasi Alat

- Catu Daya Masukkan : DC ±6V, Baterai
- Kisaran Tegangan Masukkan : 0.5 – 10mV AC
- Penguatan *Amplifier* : 1000x
- Respon Frekwensi : 0.16 – 200Hz
- Kisaran Tegangan Keluaran : 0.5 – 5V AC
- Tipe Masukkan : Elektrokardiograf (ECG/EKG)
- CMRR (dB) : 110dB Pada Vcm = DC ± 2,2mV
- Tipe *Amplifier* : *3 Op Amp IA AD620AN*
- Catu Daya Maksimal : DC ±18V
- Tipe *Display* : 20x10 Matrik LED + *driver*

BAB V

PENUTUP

5.1 Kesimpulan

1. Dari pengujian per-blok rangkaian yang dilakukan maka dapat disimpulkan bahwa :

   - Untuk pengujian *high pass filter* ada beberapa kesulitan yaitu frekwensi yang diukur sangat rendah sehingga alat ukur yang digunakan kurang akurat sehingga data yang didapatkan juga kurang valid. Tetapi pada pengujian dengan simulasi EWB, rangkaian *high pass filter* yang dirancang menghasilkan karakteristik *high pass filter* yang diinginkan.
   - Pada pengujian penguat instrumentasi (IA), jika kedua input IA diberi tegangan masukkan ($V_1 = V_2$) yang sama maka tegangan keluarannya akan cenderung mengarah ke nol dan jika salah satu inputnya di-*ground*-kan dan yang satunya diberi tegangan masukkan (V1 = 0, V2 = 1mV) maka tegangan keluarannya adalah hasil kali penguatan IA dengan selisih kedua input IA atau dapat dirumuskan : $Vo - (V_1 - V_2)1 + \frac{49,4K}{49,2Ohm}$
   - Pada pengujian *low pass filter*, jika frekwensi inputnya dibawah 200Hz maka tegangan keluarannya akan mendekati tegangan masukkannya, tetapi jika frekwensi inputnya diatas 200Hz maka tegangan *output*-nya akan semakin mengecil dan mendekati nol.

- Pada pengujian *band reject filter*, nilai tegangan keluaran yang paling kecil adalah pada saat frekwensi inputnya pada 50Hz. Ini disebabkan karena filter ini dirancang untuk menekan frekwensi 50Hz sehingga jika filter ini diberi frekwensi input dibawah 50Hz maka tegangan outputnya akan mendekati tegangan inputnya, demikian juga jika diberi frekwensi input diatas 50Hz. Dari pengujian, filter ini memiliki pita yang lebar.

2. Secara keseluruhan alat ini belum dapat menangkap sinyal jantung. Adapun penyebabnya diduga ada bebrapa faktor, yaitu :
   - Sensivitas elektroda kurang memadai, mungkin dari jenis bahannya.
   - Pemilihan kabel input yang kurang tepat dan kurang sesuai standard pengukuran ECG.
   - Metode penempatan elektroda tidak sesuai metode yang disarankan untuk pengukuan ECG.
   - Ada kemungkinan komponen yang digunakan mengalami kerusakkan sehingga tidak berfungsi dengan baik.
   - Adanya dugaan bahwa pada saat mengukur ECG, rangkaian ECG harus dihubungkan ke bumi untuk membuang noise.

5.2 Saran

1. Untuk aplikasi selanjutnya diharapkan menggunakan penampil LCD karena dengan LCD sinyal yang ditampilkan akan lebih jelas.

2. Pada perancangan ECG selanjutnya pengiriman sinyal ECG lebih baik secara *wireless*, seperti menggunakan aplikasi *bluetooth, infra red*, dll.
3. Untuk pemasangan komponen lebih baik menggunakan PCB jenis *fiberglass* karena kemungkinan *noise* lebih sedikit.
4. Pada saat pengujian keseluruhan sebaiknya menggunakan simulator ECG agar diketahui bahwa rangkaian yang dibuat benar-benar berfungsi dengan baik.

DAFTAR PUSTAKA

1. Willis J. Tomkins and John G. Webster. *Design of Microcomputer Based Medical Instrumentation*. Upper Saddle Ripple, New Jersey 07458 : Prentice Hall, 1994
2. Richard Asthon. *Principles of Biomedical Instrumentation and Measurement*. Pennsylvania State University Wilkes-Bare. MERRIL-An Imprint of Macmilan Publishing Company New York.
3. Robert F. Caughlin - Frederick F. Driscoll. *Penguat Operasional dan Rangkaian Terpadu Linear*, Erlangga, Jakarta.
4. www.datasheetcatalog.com

LAMPIRAN

Low Cost, Low Power Instrumentation Amplifier

AD620

FEATURES
EASY TO USE
Gain Set with One External Resistor
(Gain Range 1 to 1000)
Wide Power Supply Range (±2.3 V to ±18 V)
Higher Performance than Three Op Amp IA Designs
Available in 8-Lead DIP and SOIC Packaging
Low Power, 1.3 mA max Supply Current

EXCELLENT DC PERFORMANCE ("B GRADE")
50 μV max, Input Offset Voltage
0.6 μV/°C max, Input Offset Drift
1.0 nA max, Input Bias Current
100 dB min Common-Mode Rejection Ratio (G = 10)

LOW NOISE
9 nV/√Hz, @ 1 kHz, Input Voltage Noise
0.28 μV p-p Noise (0.1 Hz to 10 Hz)

EXCELLENT AC SPECIFICATIONS
120 kHz Bandwidth (G = 100)
15 μs Settling Time to 0.01%

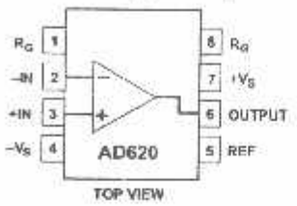
APPLICATIONS
Weigh Scales
ECG and Medical Instrumentation
Transducer Interface
Data Acquisition Systems
Industrial Process Controls
Battery Powered and Portable Equipment

ODUCT DESCRIPTION

AD620 is a low cost, high accuracy instrumentation ampli- that requires only one external resistor to set gains of 1 to

CONNECTION DIAGRAM

8-Lead Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



1000. Furthermore, the AD620 features 8-lead SOIC and DIP packaging that is smaller than discrete designs, and offers lower power (only 1.3 mA max supply current), making it a good fit for battery powered, portable (or remote) applications.

The AD620, with its high accuracy of 40 ppm maximum nonlinearity, low offset voltage of 50 μV max and offset drift of 0.6 μV/°C max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias current, and low power of the AD620 make it well suited for medical applications such as ECG and noninvasive blood pressure monitors.

The low input bias current of 1.0 nA max is made possible with the use of Superβeta processing in the input stage. The AD620 works well as a preamplifier due to its low input voltage noise of 9 nV/√Hz at 1 kHz, 0.28 μV p-p in the 0.1 Hz to 10 Hz band, 0.1 pA/√Hz input current noise. Also, the AD620 is well suited for multiplexed applications with its settling time of 15 μs to 0.01% and its cost is low enough to enable designs with one in-amp per channel.

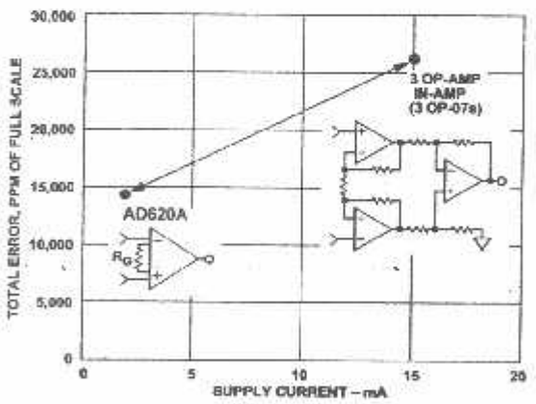


Figure 1. Three Op Amp IA Designs vs. AD620

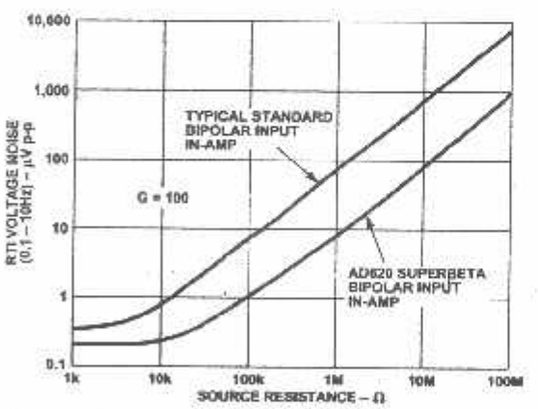


Figure 2. Total Voltage Noise vs. Source Resistance

V. E

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

20–SPECIFICATIONS (Typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted)

	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
	G = 1 + (49.4 kΩ/R_G)										
inge		1		10,000	1		10,000	1		10,000	
ror[2]	V_{OUT} = ±10 V										
1			0.01	0.10		0.01	0.02		0.03	0.10	%
10			0.15	0.30		0.10	0.15		0.15	0.30	%
100			0.15	0.30		0.10	0.15		0.15	0.30	%
1000			0.40	0.70		0.35	0.50		0.40	0.70	%
arity,	V_{OUT} = −10 V to +10 V,										
1–1000	R_L = 10 kΩ		10	40		10	40		10	40	ppm
1–100	R_L = 2 kΩ		10	95		10	95		10	95	ppm
Temperature											
	G = 1			10			10			10	ppm/°C
	Gain >1[3]			−50			−50			−50	ppm/°C
S OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)										
ffset, V_{OSI}	V_S = ±5 V to ±15 V		30	125		15	50		30	125	μV
Temperature	V_S = ±5 V to ±15 V			185			85			225	μV
age TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	μV/°C
Offset, V_{OSO}	V_S = ±15 V		400	1000		200	500		400	1000	μV
	V_S = ±5 V			1500			750			1500	μV
Temperature	V_S = ±5 V to ±15 V			2000			1000			2000	μV
age TC	V_S = ±5 V to ±15 V		5.0	15		2.5	7.0		5.0	15	μV/°C
Referred to the											
I vs.											
ply (PSR)	V_S = ±2.3 V to ±18 V										
= 1		80	100		80	100		80	100		dB
= 10		95	120		100	120		95	120		dB
= 100		110	140		120	140		110	140		dB
= 1000		110	140		120	140		110	140		dB
URRENT											
ias Current			0.5	2.0		0.5	1.0		0.5	2	nA
Temperature				2.5			1.5			4	nA
age TC			3.0			3.0			8.0		pA/°C
Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
Temperature				1.5			0.75			2.0	nA
age TC			1.5			1.5			8.0		pA/°C
mpedance											
erential			10|2			10|2			10|2		GΩ|pF
mmon-Mode			10|2			10|2			10|2		GΩ|pF
oltage Range[3]	V_S = +2.3 V to +5 V	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	V
Temperature		$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	V
Temperature		$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.3		$+V_S$ − 1.4	V
m-Mode Rejection											
DC to 60 Hz with											
Source Imbalance	V_{CM} = 0 V to ±10 V										
= 1		73	90		80	90		73	90		dB
= 10		93	110		100	110		93	110		dB
= 100		110	130		120	130		110	130		dB
= 1000		110	130		120	130		110	130		dB
Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	V
Temperature		$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.6		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	V
Temperature		$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 2.3		$+V_S$ − 1.5	V
urrent Circuit			±18			±18			±18		mA

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
DYNAMIC RESPONSE											
Small Signal −3 dB Bandwidth											
G = 1			1000			1000			1000		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			12			12			12		kHz
Slew Rate	10 V Step	0.75	1.2		0.75	1.2		0.75	1.2		V/μs
Settling Time to 0.01%											
G = 1–100			15			15			15		μs
G = 1000			150			150			150		μs
NOISE											
Voltage Noise, 1 kHz	Total RTI Noise = $\sqrt{(e_{ni}^2) + (e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			9	13		9	13		9	13	nV/√Hz
Output, Voltage Noise, e_{no}			72	100		72	100		72	100	nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0	6.0		3.0	6.0	μV p-p
G = 10			0.55			0.55	0.8		0.55	0.8	μV p-p
G = 100–1000			0.28			0.28	0.4		0.28	0.4	μV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
0.1 Hz to 10 Hz			10			10			10		pA p-p
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		+50	+60		+30	+60		+50	+60	μA
Voltage Range		$-V_S + 1.6$		$+V_S - 1.6$	$-V_S + 1.6$		$+V_S - 1.6$	$-V_S + 1.6$		$+V_S - 1.6$	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range[1]		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
Over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance			−40 to +85			−40 to +85			−55 to +125		°C

NOTES

[1] See Analog Devices military data sheet for 883B tested specifications.

Specifications not include effects of external resistor R_G.

Offset input grounded. G = 1.

This is defined as the same supply range which is used to specify PSR.

Specifications subject to change without notice.

0

UTE MAXIMUM RATINGS[1]

Voltage ..... ±18 V
Power Dissipation[2] ..... 650 mW
oltage (Common Mode) ..... $\pm V_S$
rial Input Voltage ..... ±25 V
Short Circuit Duration ..... Indefinite
Temperature Range (Q) ..... –65°C to +150°C
Temperature Range (N, R) ..... –65°C to +125°C
ıg Temperature Range
0 (A, B) ..... –40°C to +85°C
0 (S) ..... 55°C to +125°C
emperature Range
ering 10 seconds) ..... +300°C

bove those listed under Absolute Maximum Ratings may cause perma-
age to the device. This is a stress rating only; functional operation of the
these or any other conditions above those indicated in the operational
f this specification is not implied. Exposure to absolute maximum rating
s for extended periods may affect device reliability.
tion is for device in free air.
Plastic Package: θ_{JA} = 95°C/W
Cerdip Package: θ_{JA} = 110°C/W
SOIC Package: θ_{JA} = 155°C/W

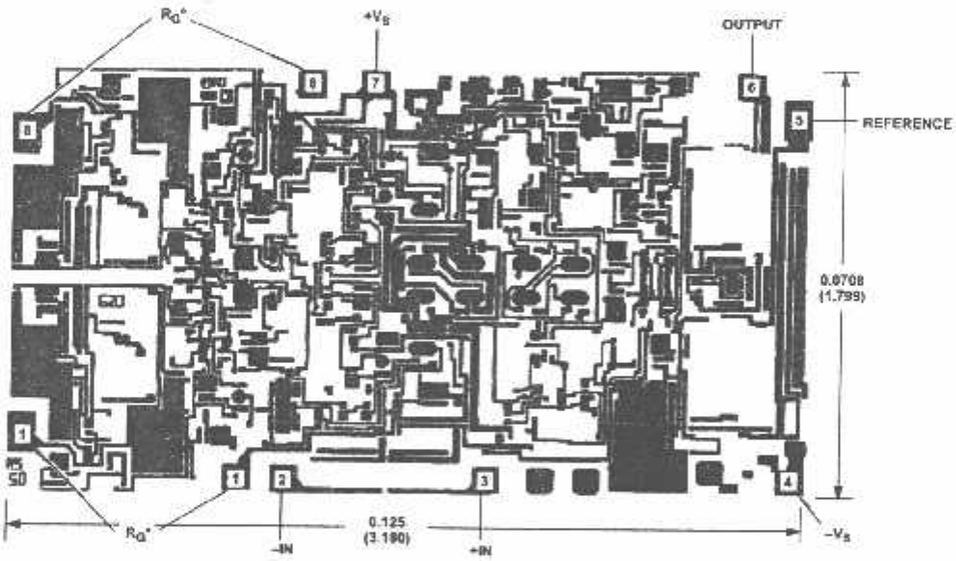
ORDERING GUIDE

Model	Temperature Ranges	Package Options*
AD620AN	–40°C to +85°C	N-8
AD620BN	–40°C to +85°C	N-8
AD620AR	–40°C to +85°C	SO-8
AD620AR-REEL	–40°C to +85°C	13" REEL
AD620AR-REEL7	–40°C to +85°C	7" REEL
AD620BR	–40°C to +85°C	SO-8
AD620BR-REEL	–40°C to +85°C	13" REEL
AD620BR-REEL7	–40°C to +85°C	7" REEL
AD620ACHIPS	–40°C to +85°C	Die Form
AD620SQ/883B	–55°C to +125°C	Q-8

*N = Plastic DIP, Q = Cerdip, SO = Small Outline.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



*FOR CHIP APPLICATIONS: THE PADS $1R_G$ AND $8R_G$ MUST BE CONNECTED IN PARALLEL TO THE EXTERNAL GAIN REGISTER R_G. DO NOT CONNECT THEM IN SERIES TO R_G. FOR UNITY GAIN APPLICATIONS WHERE R_G IS NOT REQUIRED, THE PADS $1R_G$ MAY SIMPLY BE BONDED TOGETHER, AS WELL AS THE PADS $8R_G$.

ON

ctrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily
ate on the human body and test equipment and can discharge without detection.
the AD620 features proprietary ESD protection circuitry, permanent damage may
devices subjected to high energy electrostatic discharges. Therefore, proper ESD
ons are recommended to avoid performance degradation or loss of functionality.

pical Characteristics (@ +25°C, V_S = ±15 V, R_L = 2 kΩ, unless otherwise noted)

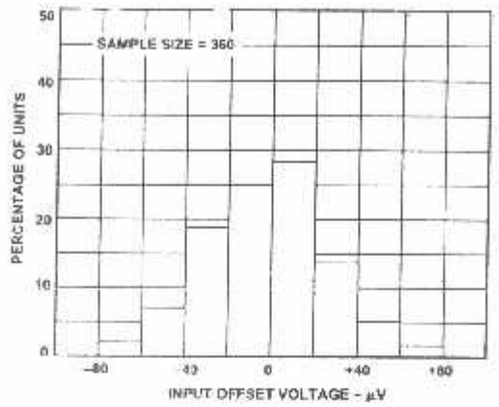


Figure 3. Typical Distribution of Input Offset Voltage

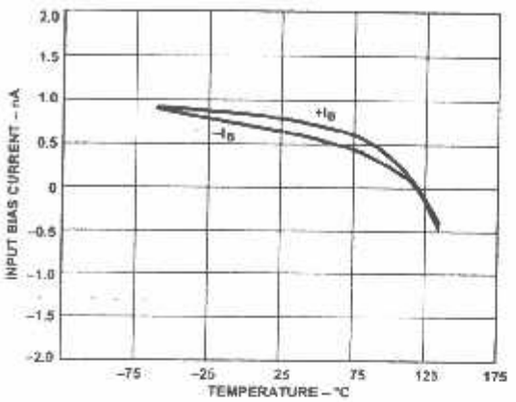


Figure 6. Input Bias Current vs. Temperature

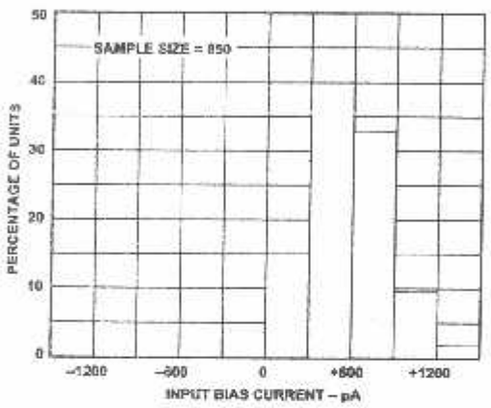


Figure 4. Typical Distribution of Input Bias Current

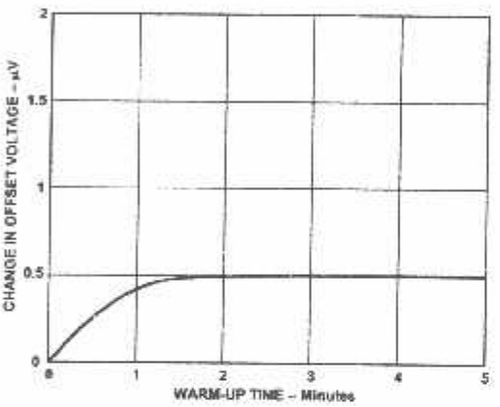


Figure 7. Change in Input Offset Voltage vs. Warm-Up Time

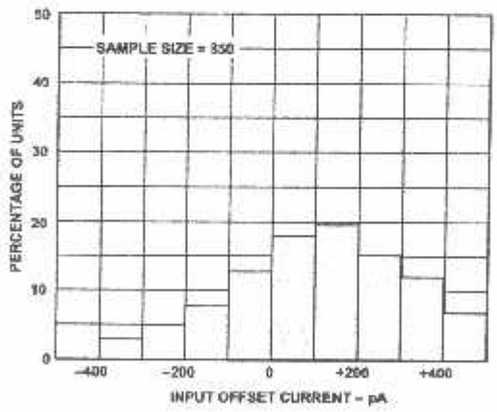


Figure 5. Typical Distribution of Input Offset Current

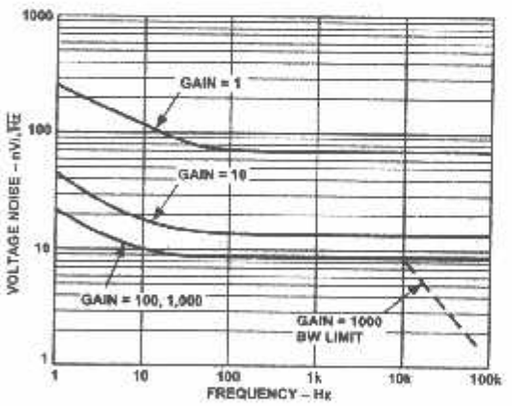
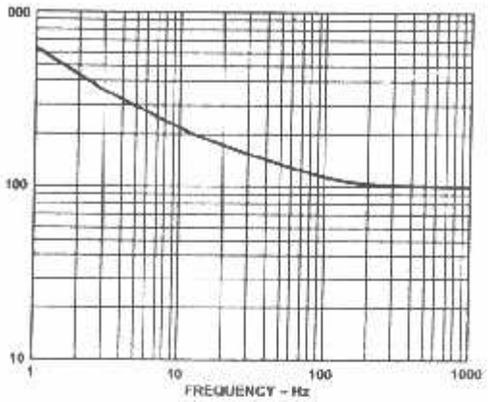


Figure 8. Voltage Noise Spectral Density vs. Frequency, (G = 1–1000)

0–Typical Characteristics



e 9. Current Noise Spectral Density vs. Frequency

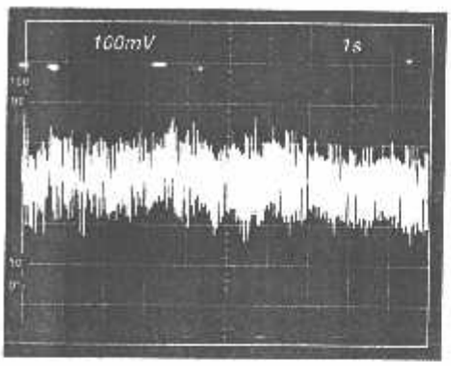
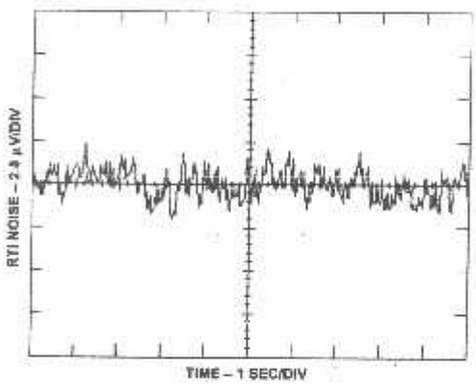


Figure 11. 0.1 Hz to 10 Hz Current Noise, 5 pA/Div



re 10a. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

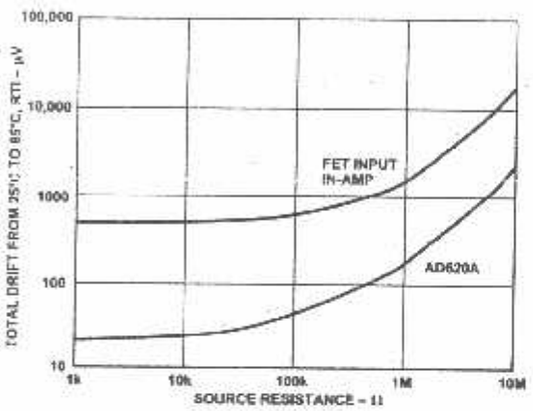
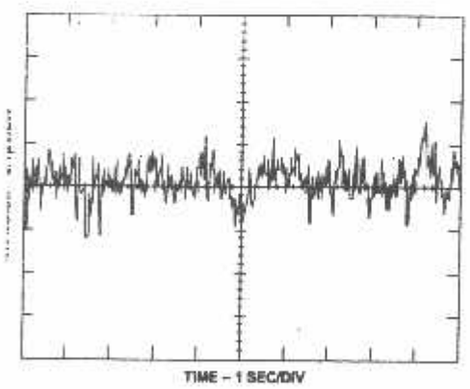


Figure 12. Total Drift vs. Source Resistance



10b. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

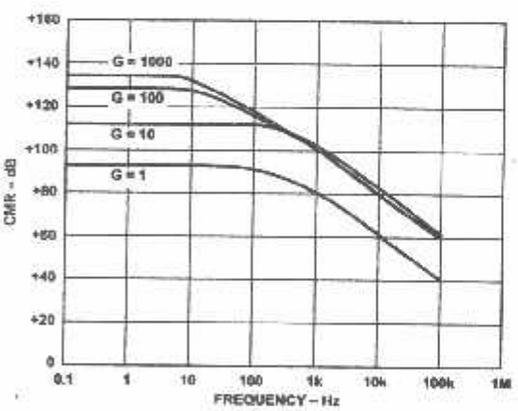
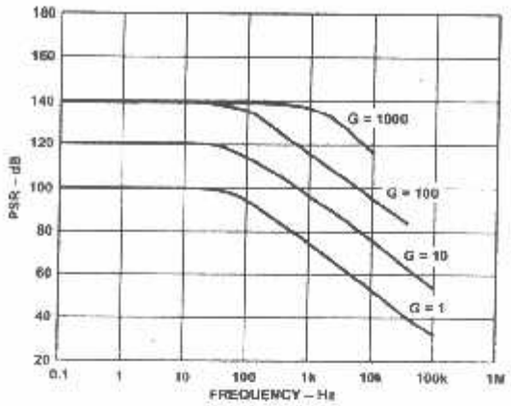


Figure 13. CMR vs. Frequency, RTI, Zero to 1 kΩ Source Imbalance



igure 14. Positive PSR vs. Frequency, RTI (G = 1–1000)

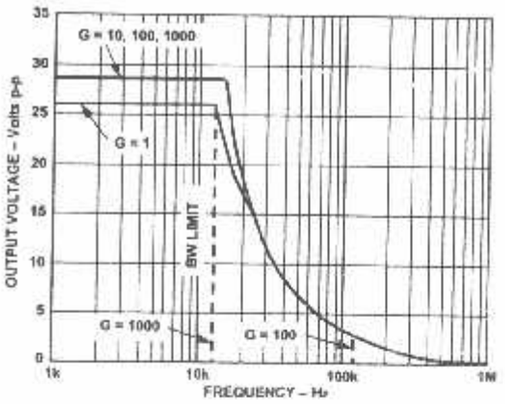
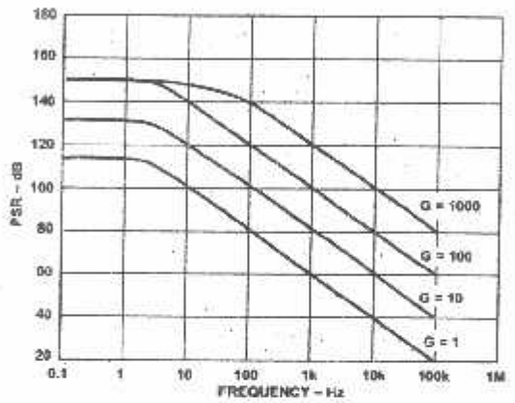


Figure 17. Large Signal Frequency Response



gure 15. Negative PSR vs. Frequency, RTI (G = 1–1000)

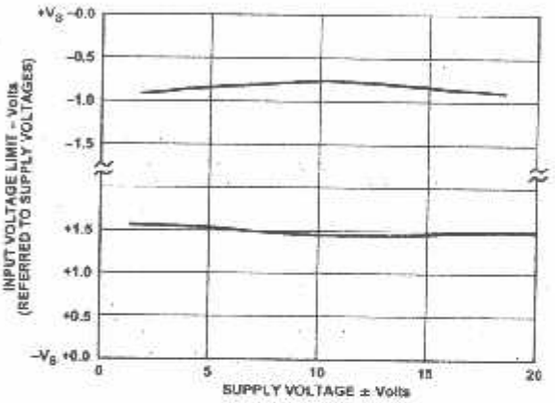


Figure 18. Input Voltage Range vs. Supply Voltage, G = 1

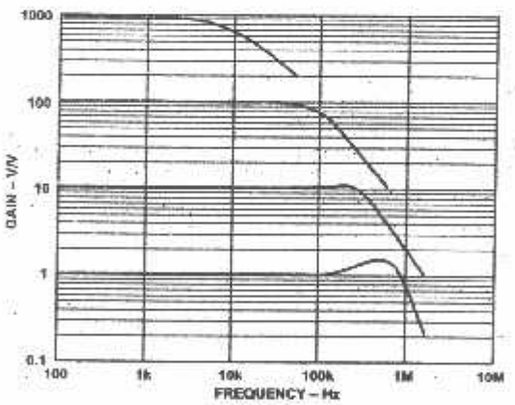


Figure 16. Gain vs. Frequency

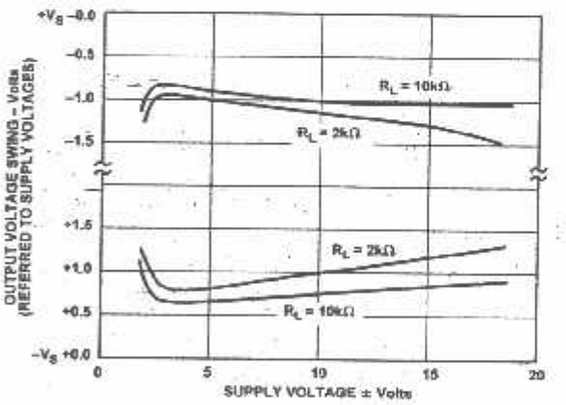
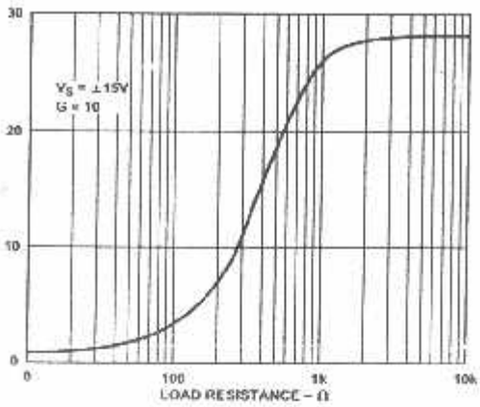


Figure 19. Output Voltage Swing vs. Supply Voltage, G = 10



re 20. Output Voltage Swing vs. Load Resistance

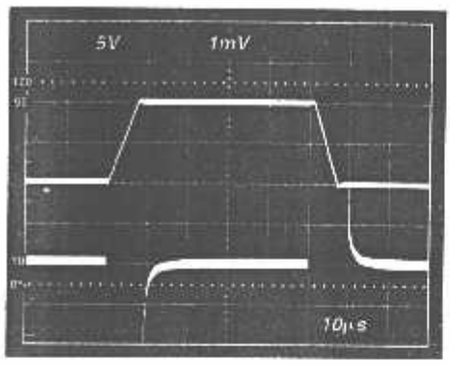
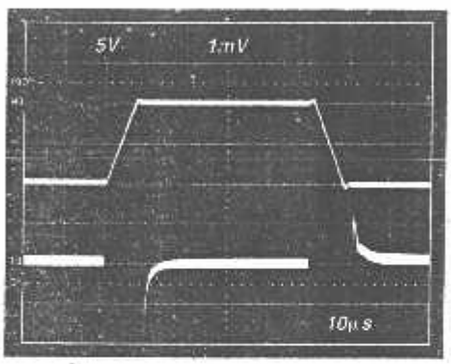


Figure 23. Large Signal Response and Settling Time, G = 10 (0.5 mV = 001%)



21. Large Signal Pulse Response and Settling Time .5 mV = 0.01%)

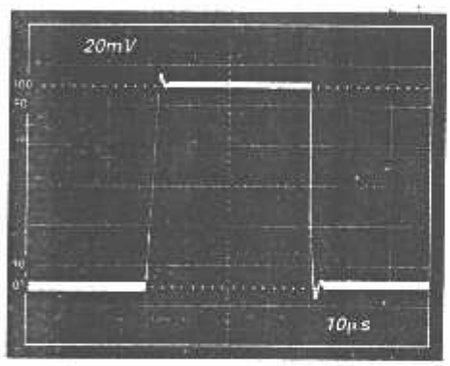
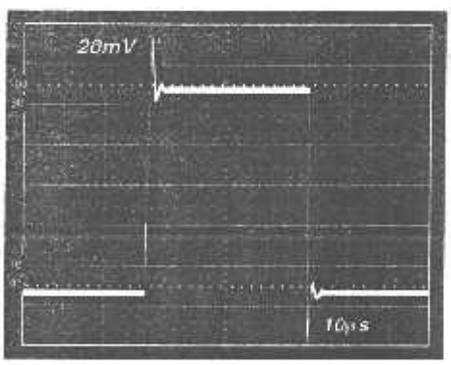


Figure 24. Small Signal Response, G = 10, R_L = 2 kΩ, C_L = 100 pF



ıre 22. Small Signal Response, G = 1, R_L = 2 kΩ, = 100 pF

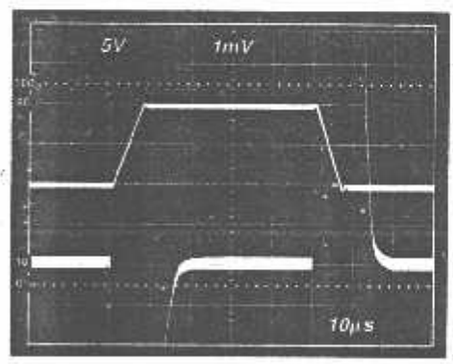


Figure 25. Large Signal Response and Settling Time, G = 100 (0.5 mV = 0.01%)

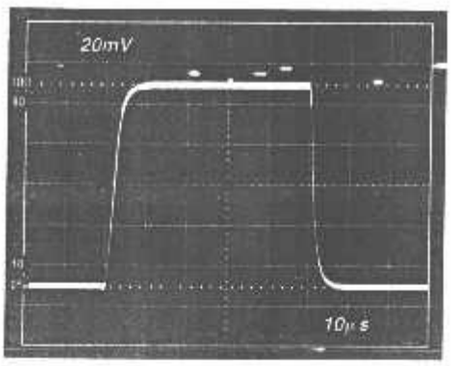


Figure 26. Small Signal Pulse Response, G = 100, R_L = 2 kΩ, C_L = 100 pF

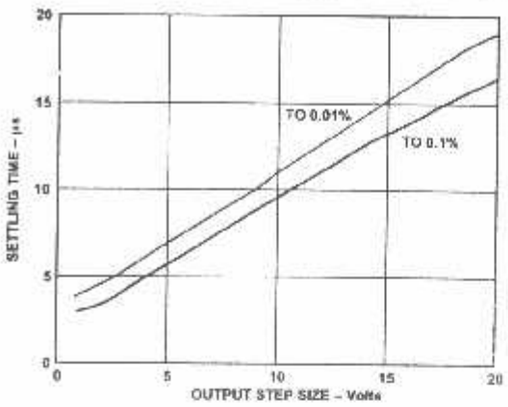
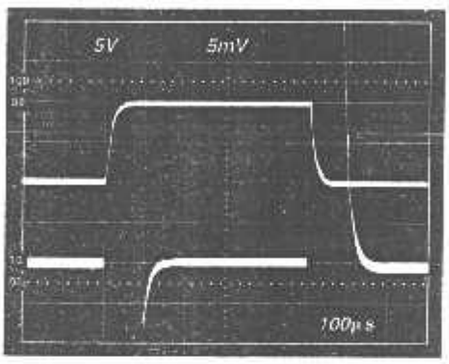


Figure 29. Settling Time vs. Step Size (G = 1)



igure 27. Large Signal Response and Settling Time, = 1000 (0.5 mV = 0.01%)

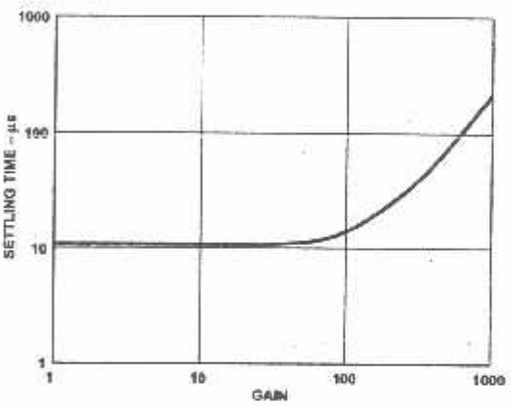


Figure 30. Settling Time to 0.01% vs. Gain, for a 10 V Step

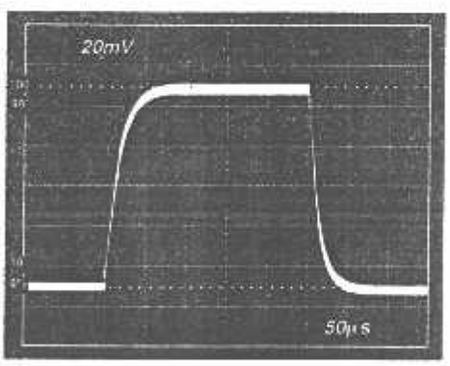


Figure 28. Small Signal Pulse Response, G = 1000, R_L = 2 kΩ, C_L = 100 pF

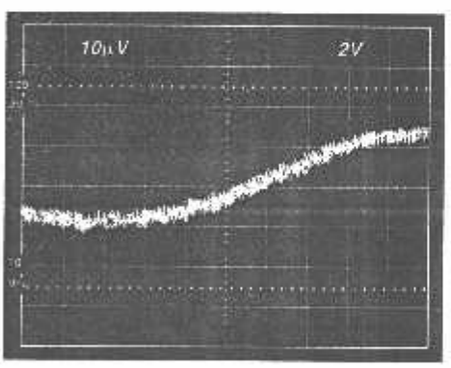
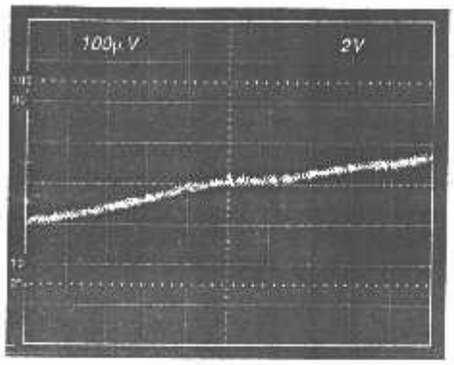
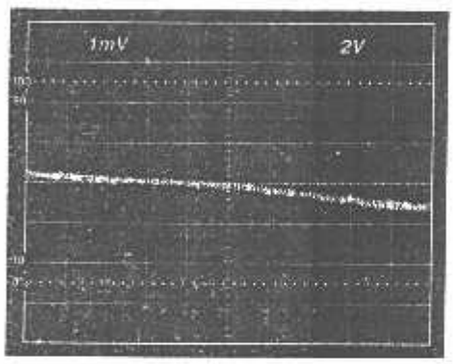


Figure 31a. Gain Nonlinearity, G = 1, R_L = 10 kΩ (10 μV = 1 ppm)



ıre 31b. Gain Nonlinearity, G = 100, R_L = 10 kΩ
7µV = 10 ppm)



ıre 31c. Gain Nonlinearity, G = 1000, R_L = 10 kΩ
)V = 100 ppm)

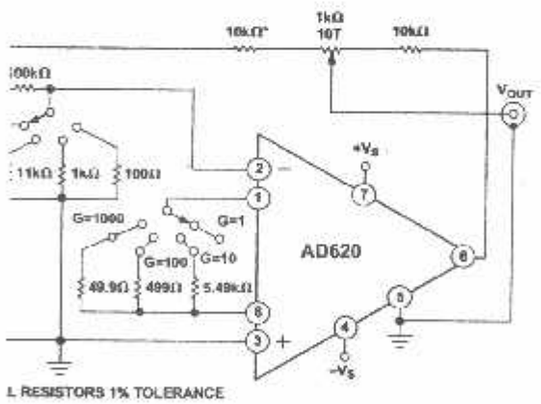


Figure 32. Settling Time Test Circuit

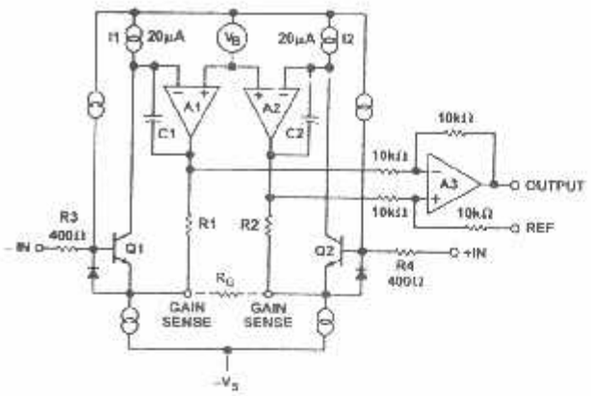


Figure 33. Simplified Schematic of AD620

THEORY OF OPERATION

The AD620 is a monolithic instrumentation amplifier based on a modification of the classic three op amp approach. Absolute value trimming allows the user to program gain *accurately* (to 0.15% at G = 100) with only one resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components, thus ensuring the high level of performance inherent in this circuit.

The input transistors Q1 and Q2 provide a single differential-pair bipolar input for high precision (Figure 33), yet offer 10× lower Input Bias Current thanks to Superβeta processing. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains constant collector current of the input devices Q1, Q2 thereby impressing the input voltage across the external gain setting resistor R_G. This creates a differential gain from the inputs to the A1/A2 outputs given by $G = (R1 + R2)/R_G + 1$. The unity-gain subtracter A3 removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: (a) Open-loop gain is boosted for increasing programmed gain, thus reducing gain-related errors. (b) The gain-bandwidth product (determined by C1, C2 and the preamp transconductance) increases with programmed gain, thus optimizing frequency response. (c) The input voltage noise is reduced to a value of 9 nV/√Hz, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor.

The gain equation is then

$$G = \frac{49.4\ k\Omega}{R_G} + 1$$

so that

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

ke vs. Buy: A Typical Bridge Application Error Budget

AD620 offers improved performance over "homebrew" e op amp IA designs, along with smaller size, fewer compots and 10× lower supply current. In the typical application, wn in Figure 34, a gain of 100 is required to amplify a bridge put of 20 mV full scale over the industrial temperature range -40°C to +85°C. The error budget table below shows how to ulate the effect various error sources have on circuit accuracy.

gardless of the system in which it is being used, the AD620 vides greater accuracy, and at low power and price. In simple systems, absolute accuracy and drift errors are by far the most significant contributors to error. In more complex systems with an intelligent processor, an autogain/autozero cycle will remove all absolute accuracy and drift errors leaving only the resolution errors of gain nonlinearity and noise, thus allowing full 14-bit accuracy.

Note that for the homebrew circuit, the OP07 specifications for input voltage offset and noise have been multiplied by $\sqrt{2}$. This is because a three op amp type in-amp has two op amps at its inputs, both contributing to the overall input error.

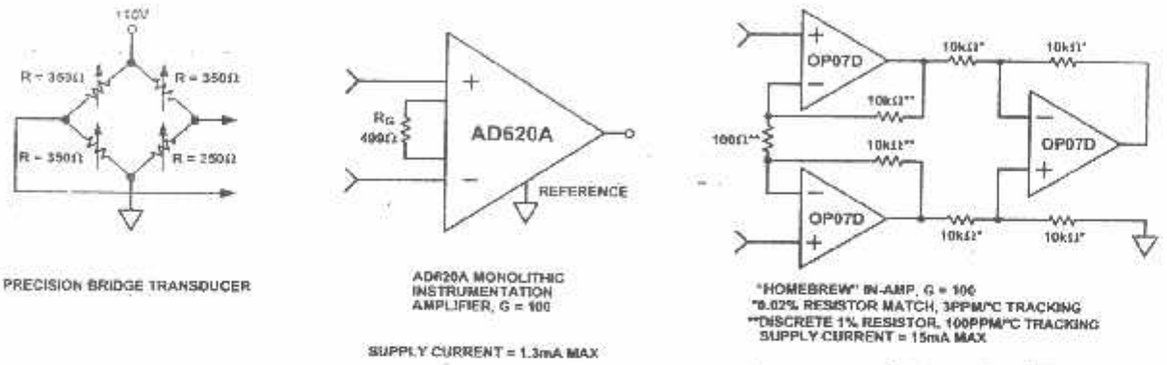


Figure 34. Make vs. Buy

Table I. Make vs. Buy Error Budget

or Source	AD620 Circuit Calculation	"Homebrew" Circuit Calculation	Error, ppm of Full Scale AD620	Homebrew
OLUTE ACCURACY at T_A = +25°C				
ıput Offset Voltage, µV	125 µV/20 mV	(150 µV × √2)/20 mV	6,250	10,607
utput Offset Voltage, µV	1000 µV/100/20 mV	((150 µV × 2)/100)/20 mV	500	150
ıput Offset Current, nA	2 nA × 350 Ω/20 mV	(6 nA × 350 Ω)/20 mV	18	53
MR, dB	110 dB→3.16 ppm, × 5 V/20 mV	(0.02% Match × 5 V)/20 mV/100	791	500
		Total Absolute Error	7,558	11,310
FT TO +85°C				
ain Drift, ppm/°C	(50 ppm + 10 ppm) × 60°C	100 ppm/°C Track × 60°C	3,600	6,000
put Offset Voltage Drift, µV/°C	1 µV/°C × 60°C/20 mV	(2.5 µV/°C × √2 × 60°C)/20 mV	3,000	10,607
utput Offset Voltage Drift, µV/°C	15 µV/°C × 60°C/100/20 mV	(2.5 µV/°C × 2 × 60°C)/100/20 mV	450	150
		Total Drift Error	7,050	16,757
OLUTION				
ain Nonlinearity, ppm of Full Scale	40 ppm	40 ppm	40	40
p 0.1 Hz–10 Hz Voltage Noise, µV p-p	0.28 µV p-p/20 mV	(0.38 µV p-p × √2)/20 mV	14	27
		Total Resolution Error	54	67
		Grand Total Error	14,662	28,134

100, V_S = ±15 V.

errors are min/max and referred to input.)

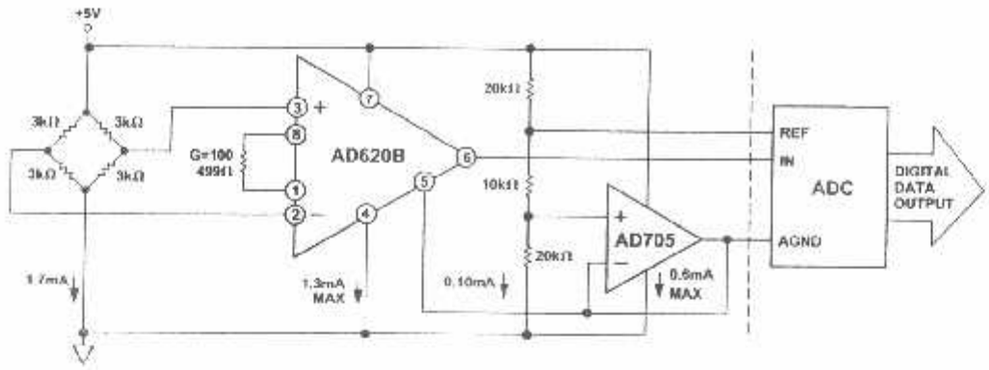


Figure 35. A Pressure Monitor Circuit which Operates on a +5 V Single Supply

'e Measurement

h useful in many bridge applications such as weigh
he AD620 is especially suitable for higher resistance
: sensors powered at lower voltages where small size and
/er become more significant.

)5 shows a 3 kΩ pressure transducer bridge powered
' V. In such a circuit, the bridge consumes only 1.7 mA.
the AD620 and a buffered voltage divider allows the
› be conditioned for only 3.8 mA of total supply current.

ze and low cost make the AD620 especially attractive for
output pressure transducers. Since it delivers low noise
t, it will also serve applications such as diagnostic non-
blood pressure measurement.

Medical ECG

The low current noise of the AD620 allows its use in ECG monitors (Figure 36) where high source resistances of 1 MΩ or higher are not uncommon. The AD620's low power, low supply voltage requirements, and space-saving 8-lead mini-DIP and SOIC package offerings make it an excellent choice for battery powered data recorders.

Furthermore, the low bias currents and low current noise coupled with the low voltage noise of the AD620 improve the dynamic range for better performance.

The value of capacitor C1 is chosen to maintain stability of the right leg drive loop. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

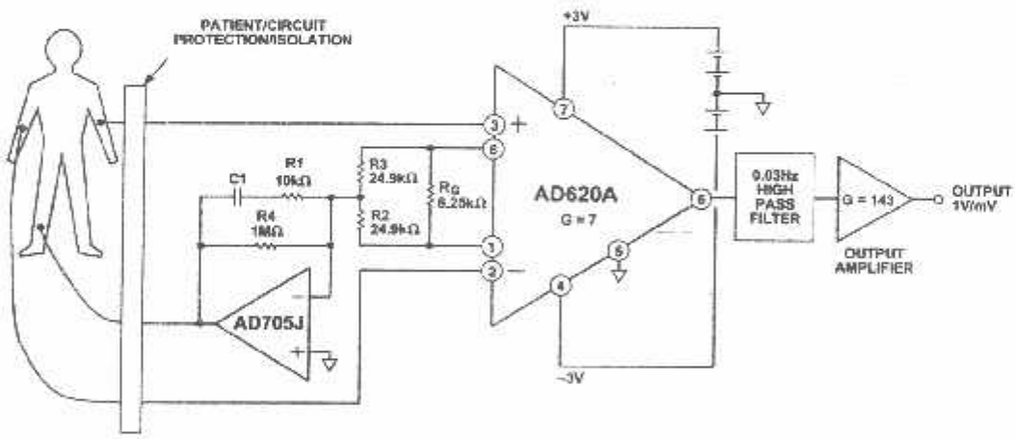


Figure 36. A Medical ECG Monitor Circuit

ecision V-I Converter

e AD620, along with another op amp and two resistors, makes recision current source (Figure 37). The op amp buffers the erence terminal to maintain good CMR. The output voltage of the AD620 appears across R1, which converts it to a rent. This current less only, the input bias current of the op p, then flows out to the load.

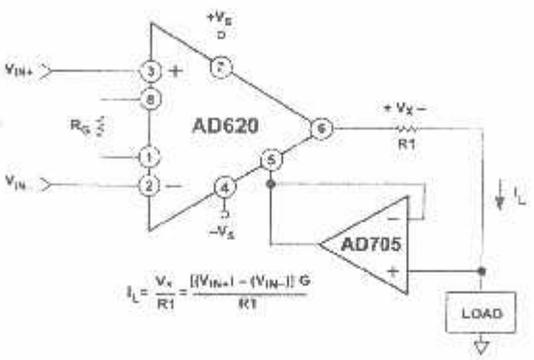


Figure 37. Precision Voltage-to-Current Converter (Operates on 1.8 mA, ±3 V)

AIN SELECTION

e AD620's gain is resistor programmed by R_G, or more pre- ely, by whatever impedance appears between Pins 1 and 8. e AD620 is designed to offer accurate gains using 0.1%–1% istors. Table II shows required values of R_G for various gains. te that for G = 1, the R_G pins are unconnected ($R_G = \infty$). For r arbitrary gain R_G can be calculated by using the formula:

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

minimize gain error, avoid high parasitic resistance in series h R_G; to minimize gain drift, R_G should have a low TC—less n 10 ppm/°C—for the best performance.

Table II. Required Values of Gain Resistors

Std Table ue of R_G, Ω	Calculated Gain	0.1% Std Table Value of R_G, Ω	Calculated Gain
9.9 k	1.990	49.3 k	2.002
2.4 k	4.984	12.4 k	4.984
.49 k	9.998	5.49 k	9.998
.61 k	19.93	2.61 k	19.93
.00 k	50.40	1.01 k	49.91
99	100.0	499	100.0
:49	199.4	249	199.4
00	495.0	98.8	501.0
:9.9	991.0	49.3	1,003

INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD620 are attributed to two sources, input and output errors. The output error is divided by G when referred to the input. In practice, the input errors dominate at high gains and the output errors dominate at low gains. The total V_{OS} for a given gain is calculated as:

Total Error RTI = input error + (output error/G)

Total Error RTO = (input error × G) + output error

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage, and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

INPUT PROTECTION

The AD620 features 400 Ω of series thin film resistance at its inputs, and will safely withstand input overloads of up to ±15 V or ±60 mA for several hours. This is true for all gains, and power on and off, which is particularly important since the signal source and amplifier may be powered separately. For longer time periods, the current should not exceed 6 mA ($I_{IN} \le V_{IN}/400\ \Omega$). For input overloads beyond the supplies, clamping the inputs to the supplies (using a low leakage diode such as an FD333) will reduce the required resistance, yielding lower noise.

RF INTERFERENCE

All instrumentation amplifiers can rectify out of band signals, and when amplifying small signals, these rectified voltages act as small dc offset errors. The AD620 allows direct access to the input transistor bases and emitters enabling the user to apply some first order filtering to unwanted RF signals (Figure 38), where RC = 1/(2 πf) and where f ≥ the bandwidth of the AD620; C ≤ 150 pF. Matching the extraneous capacitance at Pins 1 and 8 and Pins 2 and 3 helps to maintain high CMR.

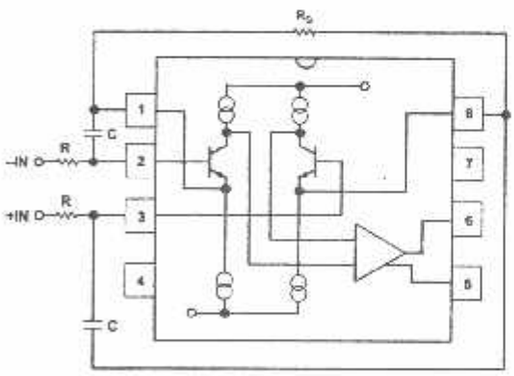


Figure 38. Circuit to Attenuate RF Interference

ION-MODE REJECTION

rentation amplifiers like the AD620 offer high CMR, s a measure of the change in output voltage when both ate changed by equal amounts. These specifications are given for a full-range input voltage change and a specirce imbalance.

imal CMR the reference terminal should be tied to a low nce point, and differences in capacitance and resistance be kept to a minimum between the two inputs. In many tions shielded cables are used to minimize noise, and for MR over frequency the shield should be properly driven. 39 and 40 show active data guards that are configured ove ac common-mode rejections by "bootstrapping" the ances of input cable shields, thus minimizing the capaciismatch between the inputs.

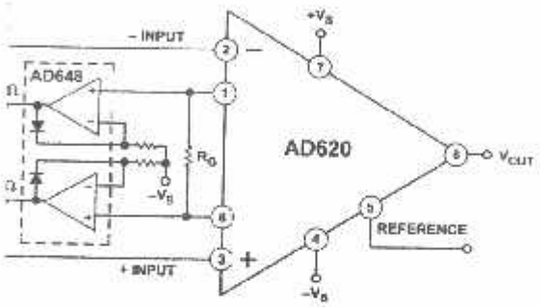


Figure 39. Differential Shield Driver

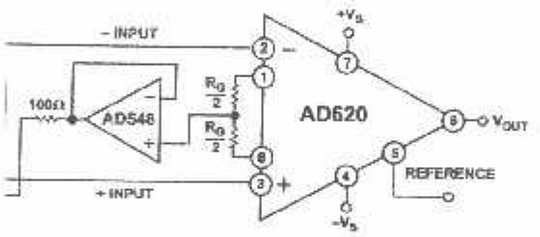


Figure 40. Common-Mode Shield Driver

GROUNDING

Since the AD620 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems by simply tying the REF pin to the appropriate "local ground."

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground pins (Figure 41). It would be convenient to use a single ground line; however, current through ground wires and PC runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground. These ground returns must be tied together at some point, usually best at the ADC package as shown.

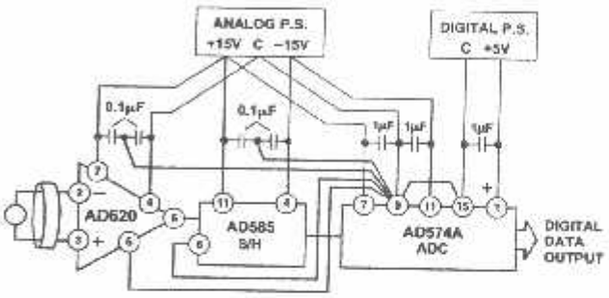


Figure 41. Basic Grounding Practice

ROUND RETURNS FOR INPUT BIAS CURRENTS

put bias currents are those currents necessary to bias the input insistors of an amplifier. There must be a direct return path these currents; therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 42. Refer to the *Instrumentation Amplifier Application Guide* (free from Analog Devices) for more information regarding in amp applications.

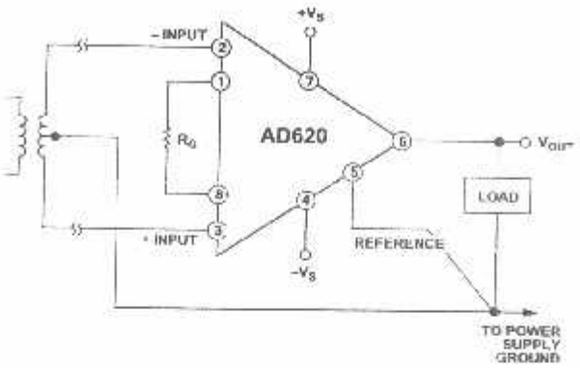


Figure 42a. Ground Returns for Bias Currents with Transformer Coupled Inputs

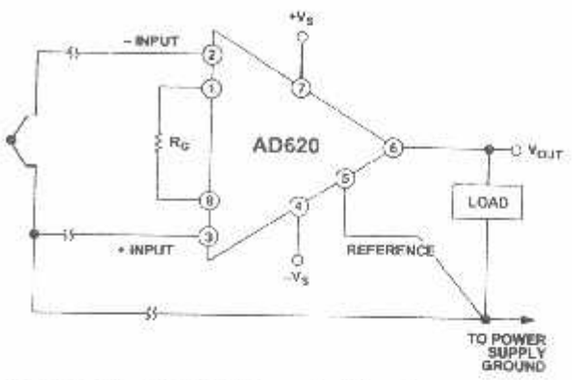


Figure 42b. Ground Returns for Bias Currents with Thermocouple Inputs

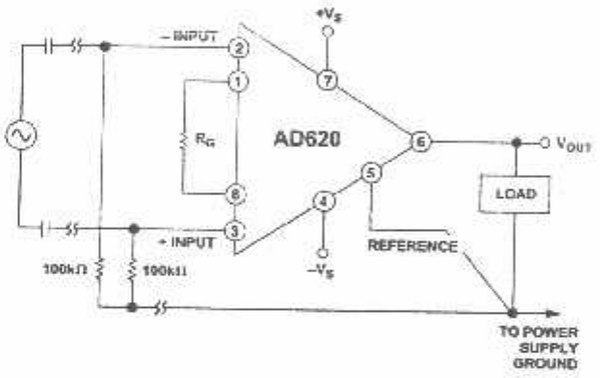
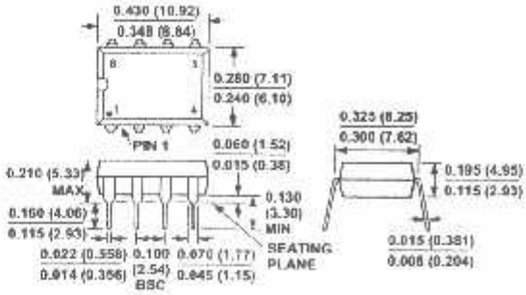


Figure 42c. Ground Returns for Bias Currents with AC Coupled Inputs

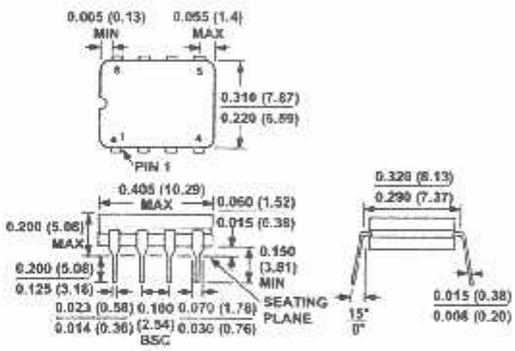
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

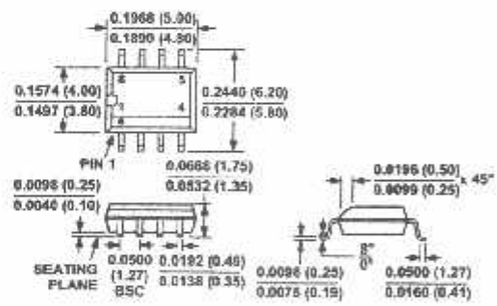
Plastic DIP (N-8) Package



Cerdip (Q-8) Package



SOIC (SO-8) Package



C1599c-0-7/89

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National Semiconductor

December 1995

LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

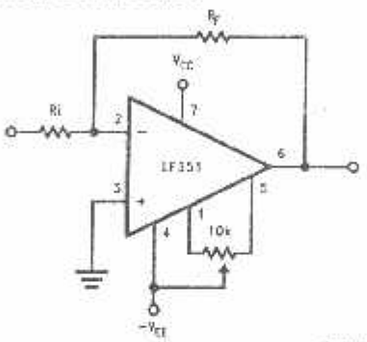
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

Features

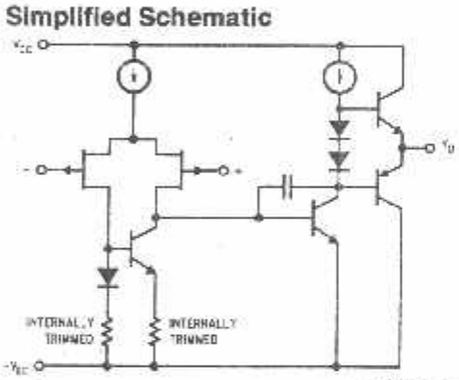
■ Internally trimmed offset voltage	10 mV
■ Low input bias current	50 pA
■ Low input noise voltage	25 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



TL/H/5648–11

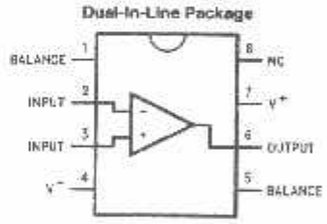
Simplified Schematic



TL/H/5648–12

Connection Diagrams

Dual-In-Line Package



TL/H/5648–13

Order Number LF351M or LF351N
See NS Package Number M08A or N08E

RRD-B30M105/Printed in U.S.A.

AC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13		V/μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, $f = 1000$ Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, $f = 1000$ Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on the thermal resistance, θ_{JA}.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C < T_A < +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

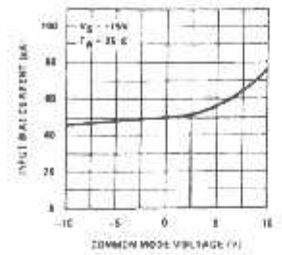
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from $\pm 12V$ to $\pm 15V$.

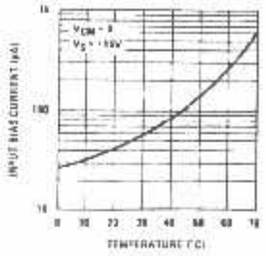
Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

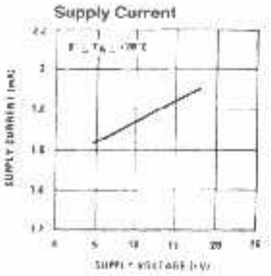
Input Bias Current



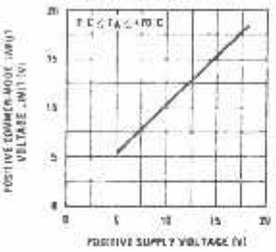
Input Bias Current



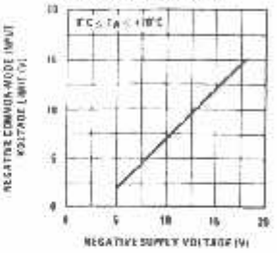
Supply Current



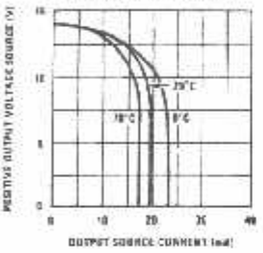
Positive Common-Mode Input Voltage Limit



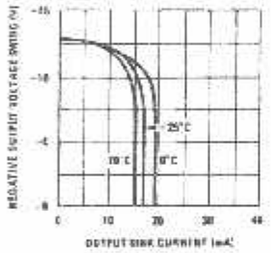
Negative Common-Mode Input Voltage Limit



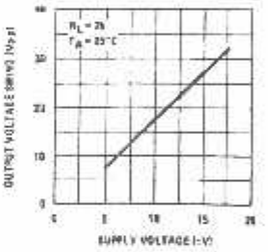
Positive Current Limit



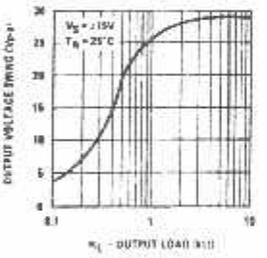
Negative Current Limit



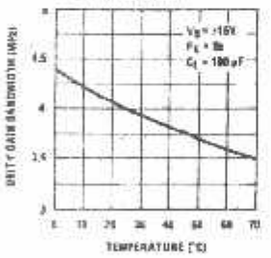
Voltage Swing



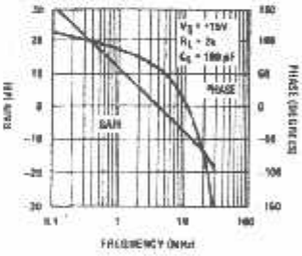
Output Voltage Swing



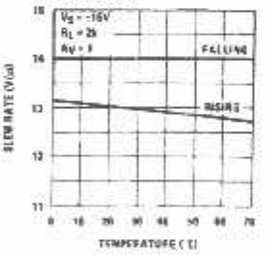
Gain Bandwidth



Bode Plot



Slew Rate



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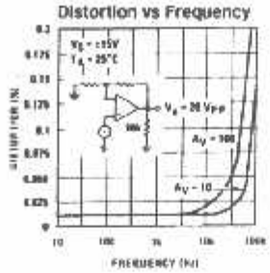
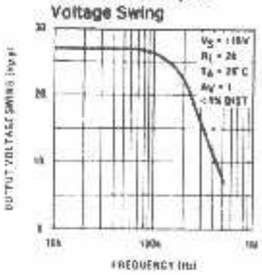
Typical Performance Characteristics (Continued)

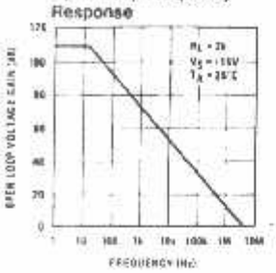
Distortion vs Frequency



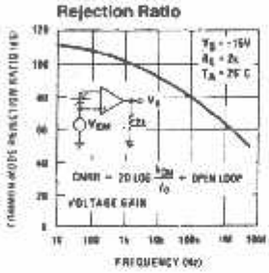
Undistorted Output Voltage Swing



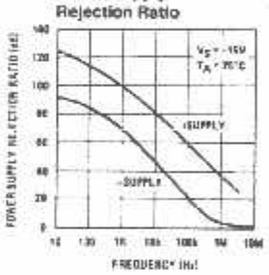
Open Loop Frequency Response



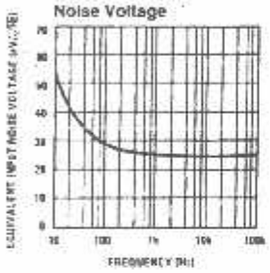
Common-Mode Rejection Ratio



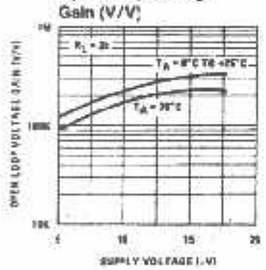
Power Supply Rejection Ratio



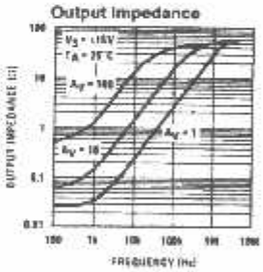
Equivalent Input Noise Voltage



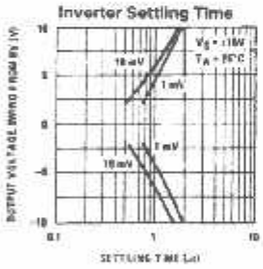
Open Loop Voltage Gain (V/V)



Output Impedance



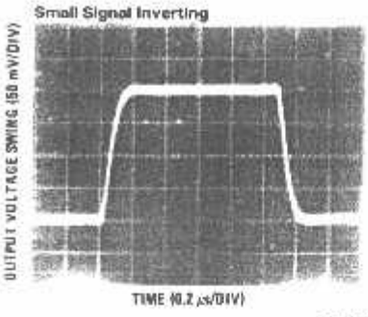
Inverter Settling Time



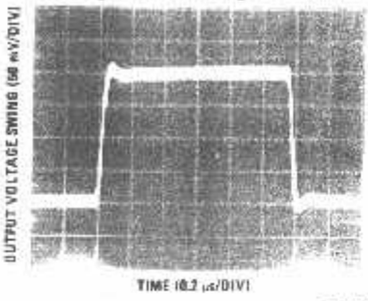
TL/H/5848–3

Pulse Response

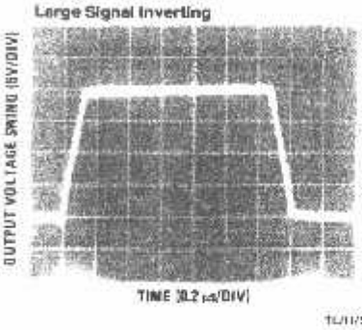
Small Signal Inverting



Small Signal Non-Inverting

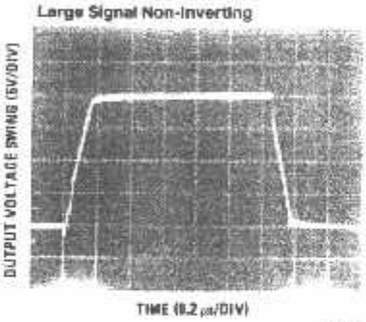


Large Signal Inverting

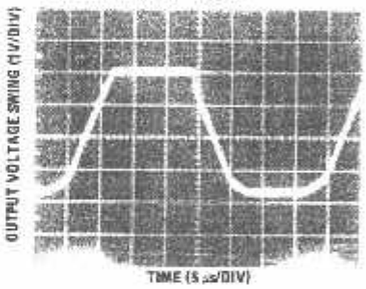


TL/H/5648–6

Large Signal Non-Inverting



Current Limit (R_L = 100Ω)



TL/H/5648–8

Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positve supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

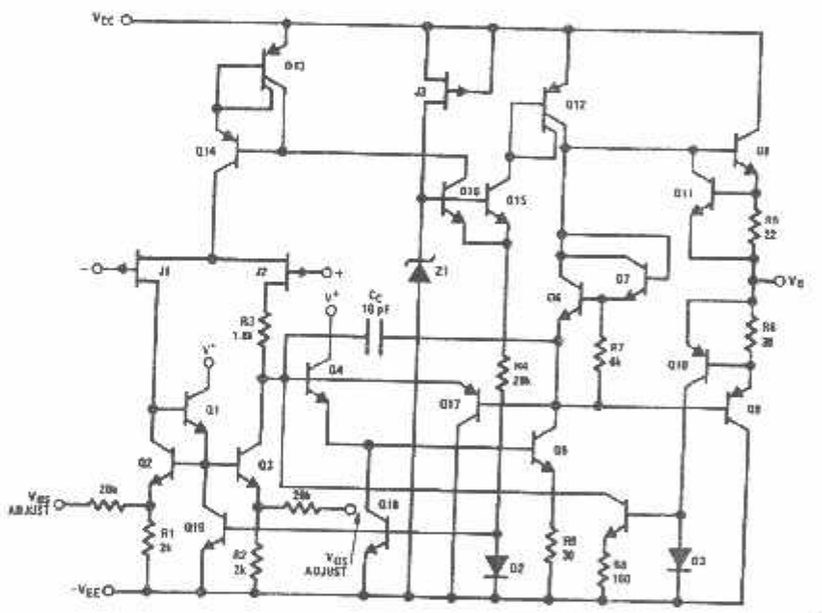
The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

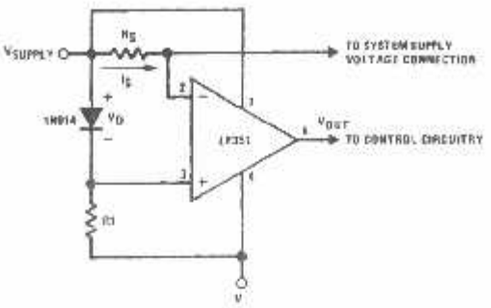
Detailed Schematic



TL/H/5546-9

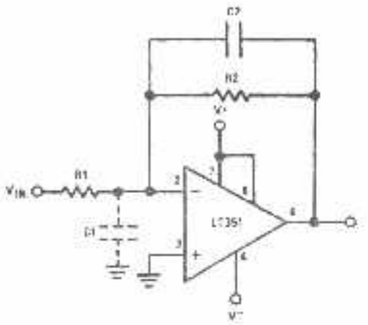
Typical Applications

Supply Current Indicator/Limiter



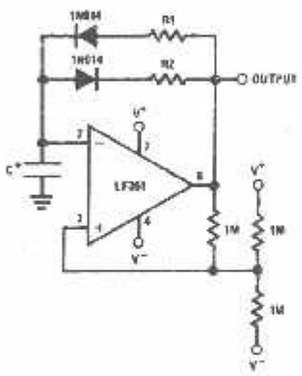
* V_{OUT} switches high when $R_S I_S = V_D$

Hi-Z_{IN} Inverting Amplifier



Parasitic input capacitance C1 ≈ (3 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that R2C2 ≈ R1C1

Ultra-Low (or High) Duty Cycle Pulse Generator



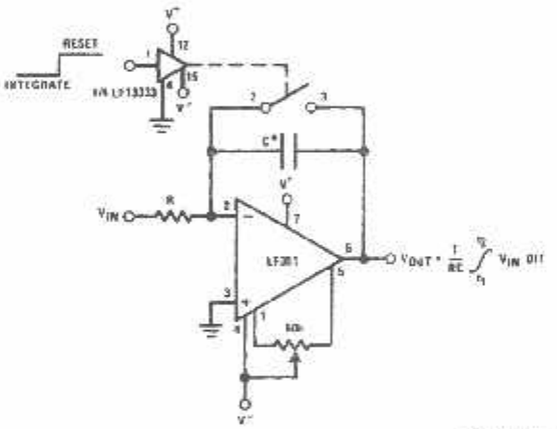
$$* t_{OUTPUT\ HIGH} = R_1 C \ln \frac{4.8 - 2V_S}{4.8 - V_S}$$

$$* t_{OUTPUT\ LOW} \approx R_2 C \ln \frac{2V_S - 7.8}{V_S - 7.8}$$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

Long Time Integrator

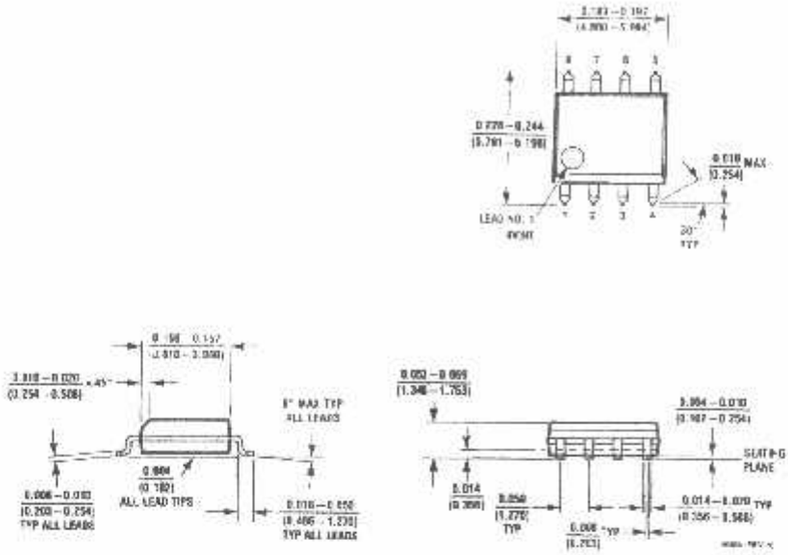


TL/H/5645–10

*Low leakage capacitor

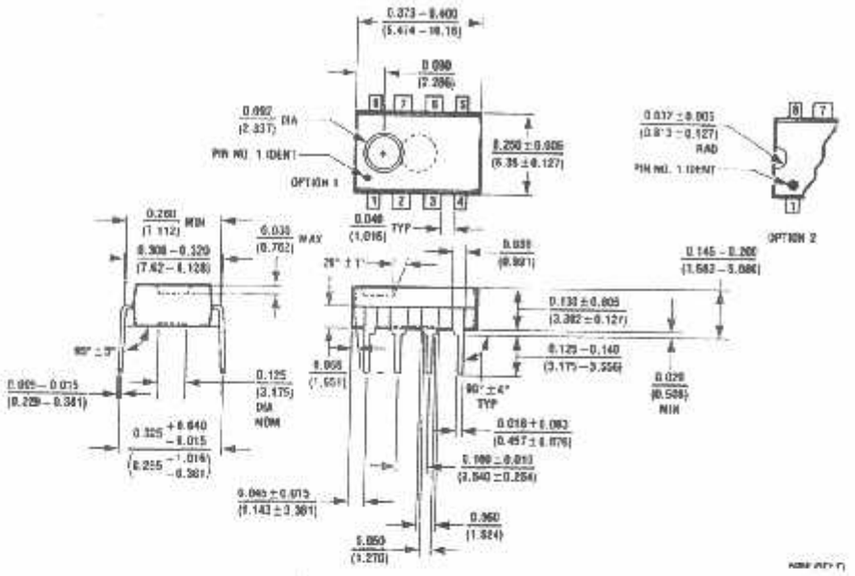
* 50k pot used for less sensitive V_{OS} adjust

Physical Dimensions inches (millimeters)



SO Package (M)
Order Number LF351M
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LF351N
NS Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Dual/Quad Low Power Precision, Picoamp Input Op Amps

ITURES

ffset Voltage – Prime Grade: 60µV Max
ffset Voltage – Low Cost Grade
ncluding Surface Mount Dual/Quad): 75uV Max
tset Voltage Drift: 0.5µV/°C Max
put Bias Current: 250pA Max
1Hz to 10Hz Noise: 0.3µV_{P-P}, 2.2pA_{P-P}
pply Current per Amplifier: 400µA Max
MRR: 120dB Min
oltage Gain: 1 Million Min
uaranteed Specs with ±1.0V Supplies
uaranteed Matching Specifications
-8 Package – Standard Pinout
T1114 in Narrow Surface Mount Package

PLICATIONS

coampere/Microvolt Instrumentation
o and Three Op Amp Instrumentation Amplifiers
ermocouple and Bridge Amplifiers
w Frequency Active Filters
oto Current Amplifiers
ttery-Powered Systems

DESCRIPTION

The LT1112 dual and LT1114 quad op amps achieve a new standard in combining low cost and outstanding precision specifications.

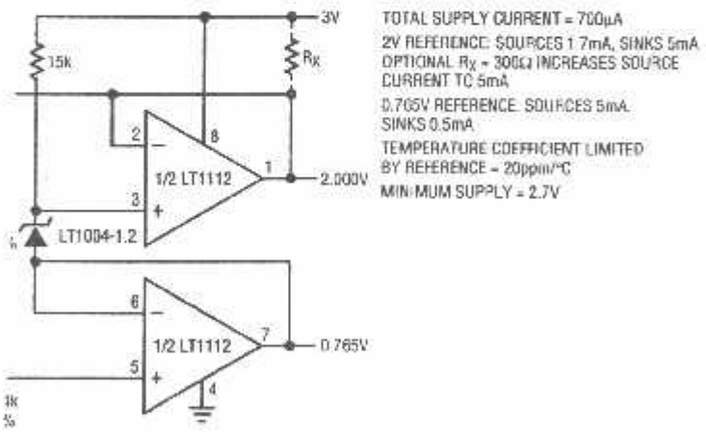
The performance of the selected pinouts equals or exceeds competitive devices. In the design of the LT1112, LT1114 however, particular emphasis has been placed on optimizing performance in the low cost plastic and SO packages. For example, the 75µV maximum offset voltage in these low cost packages is the lowest on any dual or quad non-chopper op amp.

The LT1112/LT1114 also provide a full set of matching specifications, facilitating their use in such matching dependent applications as two and three op amp instrumentation amplifiers.

Another set of specifications is furnished at ±1V supplies. This, combined with the low 320µA supply current per amplifier, allows the LT1112/LT1114 to be powered by two nearly discharged AA cells.

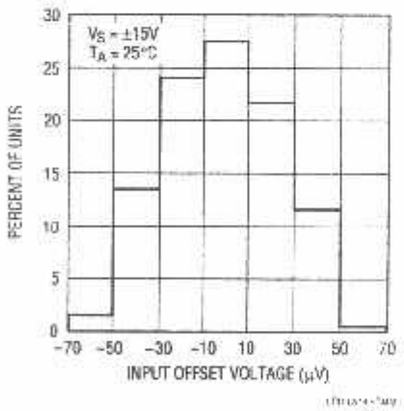
ICAL APPLICATION

Dual Output, Buffered Reference (On Single 3V Supply)



TOTAL SUPPLY CURRENT = 700µA
2V REFERENCE: SOURCES 1.7mA, SINKS 5mA
OPTIONAL R_X = 300Ω INCREASES SOURCE CURRENT TO 5mA
0.765V REFERENCE: SOURCES 5mA, SINKS 0.5mA
TEMPERATURE COEFFICIENT LIMITED BY REFERENCE = 20ppm/°C
MINIMUM SUPPLY = 2.7V

Distribution of Input Offset Voltage (In All Packages)



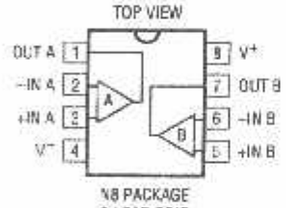
SOLUTE MAXIMUM RATINGS (Note 1)

Voltage ..... +20V
ential Input Current (Note 2) 10mA
Voltage (Equal to Supply Voltage) 20V
ut Short-Circuit Duration ..... Indefinite
ge Temperature Range ..... –65°C to 150°C
Temperature (Soldering, 10 sec) ..... 300°C
ating Temperature Range (Note 11)
1112AM/LT1112M
1114AM/LT1114M (OBSOLETE) .. –55°C to 125°C
1112AC/ T1112C/LT1112S8
1114AC/LT1114C/LT1114S ..... –40°C to 85°C
1112I/LT1114I ..... –40°C to 85°C
1112MPS8 ..... –55°C to 125°C

Specified Temperature Range (Note 12)
LT1112AM/LT1112M
LT1114AM/LT1114M (OBSOLETE) ..... –55°C to 125°C
LT1112AC/LT1112C/LT1112S8
LT1114AC/LT1114C/LT1114S ..... –40°C to 85°C
LT1112I/LT1114I ..... –40°C to 85°C
LT1112MPS8 ..... –55°C to 125°C

CKAGE/ORDER INFORMATION

TOP VIEW



N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 150°C, θ_{JA} = 130°C/W

J8 PACKAGE 8-LEAD CERDIP
T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1112ACN8
LT1112CN8
LT1112IN8

LT1112AMJ8
LT1112MJ8

OBSOLETE PACKAGE
Consider the N8 Package for Alternate Source

TOP VIEW

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 190°C/W

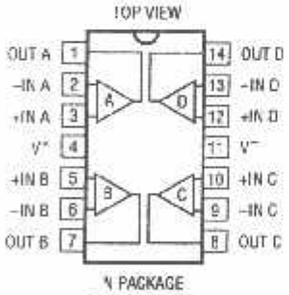
ORDER PART NUMBER

LT1112CS8
LT1112IS8
LT1112MPS8

S8 PART MARKING

1112
1112I
1112MP

TOP VIEW



N PACKAGE
14-LEAD PDIP

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

J PACKAGE 14-LEAD CERDIP
T_{JMAX} = 150°C, θ_{JA} = 80°C/W (J)

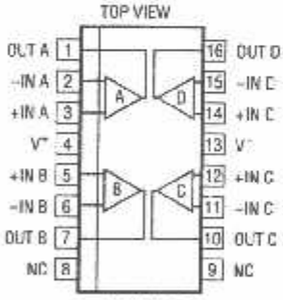
ORDER PART NUMBER

LT1114ACN
LT1114CN
LT1114IN

LT1114AMJ
LT1114MJ

OBSOLETE PACKAGE
Consider the N Package for Alternate Source

TOP VIEW



S PACKAGE
16-LEAD PLASTIC SO (NARROW)

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER

LT1114S
LT1114IS

TC Marketing for parts specified with wider operating temperature ranges.

CTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, T_A = 25°C, unless otherwise noted.

BL	PARAMETER	CONDITIONS (Note 3)	LT1112AM/AC LT1114AM/AC MIN	TYP	MAX	LT1112M/C/I LT1114M/C/I MIN	TYP	MAX	UNITS
	Input Offset Voltage			20	60		25	75	µV
				40	110		45	90	µV
	Long Term Input Offset Voltage Stability			0.1			0.2		µV/Mo
	Input Offset Current			50	130		60	150	pA
							70	200	pA
	Input Bias Current			1.0	2.8		1.0	3.5	nA
							1.05	3.45	nA
	Input Noise Voltage			0.3	0.6		0.3	0.6	µVp-p
	Input Noise Voltage Density			16	28		16	32	nV/√Hz
				13	18		13	22	nV/√Hz
	Input Noise Current			0.2			0.2		pAp-p
	Input Noise Current Density			0.030			0.030		pA/√Hz
				0.008			0.008		pA/√Hz
	Input Voltage Range		±13.5	±14.3		±13.5	±14.3		V
	Common Mode Rejection Ratio	V_{CM} = ±13.5V	120	136		115	126		dB
	Power Supply Rejection Ratio	V_S = ±1.5V to ±20V	116	126		114	126		dB
	Minimum Supply Voltage	(Note 5)	±1.2			±1.2			V
	Input Resistance Differential Mode	(Note 4)	90	50		15	40		MΩ
	Common Mode			300			700		GΩ
	Large Signal Voltage Gain	V_O = ±12V, R_L = 10kΩ	1000	5000		300	5000		V/mV
		V_O = ±10V, R_L = 2kΩ	800	1500		600	1300		V/mV
	Output Voltage Swing	R_L = 10kΩ	±13.0	±14.0		±13.0	±14.0		V
		R_L = 2kΩ	±11.0	±13.4		±11.0	±12.4		V
	Slew Rate		0.16	0.30		0.16	0.30		V/µs
	Gain-Bandwidth Product	f_O = 10kHz	450	750		450	750		kHz
	Supply Current per Amplifier			350	430		350	450	µA
		V_S = ±1.5V		320	370		320	420	µA
	Channel Separation	f_O = 10Hz		150			150		dB
	Offset Voltage Match	(Note 6)		35	100		40	130	µV
	Noninverting Bias Current Match (Notes 6, 7)	LT1114S/LT1114IS		100	450		100	500	pA
							120	650	pA
	Common Mode Rejection Match	(Notes 6, 8)	117	136		115	136		dB
	Power Supply Rejection Match	(Notes 6, 8)	114	130		112	130		dB

ECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating erature range of –55°C ≤ T_A ≤ 125°C, otherwise specifications are at T_A = 25°C. V_S = ±15V, unless otherwise noted.

IOL	PARAMETER	CONDITIONS (Note 3)		LT1112AMJ8 LT1114AMJ MIN	TYP	MAX	LT1112MJ8/8PS8 LT1114MJ MIN	TYP	MAX	UNITS
	Input Offset Voltage		●		35	100		45	150	µV
		LT1112MPS8	●					45	150	µV
		V_S = ±1.2V	●		60	220		70	300	µV
	Average Input Offset Voltage Drift	(Note 9)	●		0.15	0.5		0.2	0.7	µV/°C
P		LT1112MPS8	●					0.2	0.7	µV/°C
	Input Offset Current		●		30	400		100	500	pA
	Input Bias Current		●		±150	±600		±200	±700	pA
	Input Voltage Range		●	±13.5	±14.1		±13.5	±14.1		V
	Common Mode Rejection Ratio	V_{CM} = ±13.5V	●	115	130		111	130		dB
	Power Supply Rejection Ratio	V_S = ±1.2V to ±20V	●	112	124		110	124		dB
	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10kΩ	●	500	2500		400	2500		V/mV
		V_O = ±10V, R_L = 2kΩ	●	300	1200		270	1200		V/mV
	Output Voltage Swing	R_L = 10kΩ	●	±13.0	±13.65		±13.0	±13.65		V
	Slew Rate		●	0.17	0.22		0.12	0.22		V/µs
	Supply Current per Amplifier		●		380	460		380	510	µA
	Offset Voltage Match (Note 6)		●		55	200		70	250	µV
		LT1112VPS8	●					70	275	µV
	Offset Voltage Match Drift (Notes 5, 9)		●		0.2	0.7		0.3	1.0	µV/°C
		LT1112MPS8	●					0.3	1.0	µV/°C
	Noninverting Bias Current Match	(Notes 6, 7)	●		150	750		170	850	pA
R	Common Mode Rejection Ratio	(Notes 6, 8)	●	112	130		108	130		dB
	Power Supply Rejection Ratio	(Notes 6, 8)	●	109	126		105	126		dB

● denotes the specifications which apply over the full operating temperature range of 0°C ≤ T_A ≤ 70°C, otherwise specifications T_A = 25°C. V_S = ±15V, unless otherwise noted.

OL	PARAMETER	CONDITIONS (Note 3)		LT1112ACN8 LT1114ACN MIN	TYP	MAX	LT1112CN8/S8/IS8 LT1114CN/S/IS MIN	TYP	MAX	UNITS
	Input Offset Voltage	LT1112CN8	●		77	190		90	225	µV
		LT1112S8, LT1114CN/S	●		35	125		45	150	µV
		V_S = ±1.2V	●		50	175		65	210	µV
	Average Input Offset Voltage Drift (Note 9)	LT1112CN8	●		0.15	0.5		0.2	0.75	µV/°C
		LT1112S8, LT1114CN/S	●		0.3	1.1		0.4	1.5	µV/°C
	Input Offset Current		●		50	220		75	300	pA
		LT1114S	●					90	425	pA
	Input Bias Current		●		±80	±300		±90	±350	pA
		LT1114S	●					±115	±550	pA
	Input Voltage Range		●	±13.5	±14.2		±13.5	±14.2		V
	Common Mode Rejection Ratio	V_{CM} = ±13.5V	●	118	133		115	133		dB
	Power Supply Rejection Ratio	V_S = ±1.2V to ±20V	●	114	125		112	125		dB
	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10kΩ	●	800	4000		650	4000		V/mV
		V_O = ±10V, R_L = 2kΩ	●	500	1300		400	1300		V/mV
	Output Voltage Swing	R_L = 2kΩ	●	±13.0	±13.9		±13.0	±13.9		V
	Slew Rate		●	0.14	0.27		0.14	0.27		V/µs

CTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating rature range of 0°C ≤ T_A ≤ 70°C, otherwise specifications are at T_A = 25°C. V_S = ±15V, unless otherwise noted.

OL	PARAMETER	CONDITIONS (Note 3)		LT1112ACN8 LT1114ACN MIN	TYP	MAX	LT1112CN8/S8/IS8 LT1114CN/S/IS MIN	TYP	MAX	UNITS
	Supply Current per Amplifier		●		370	440		370	450	μA
	Offset Voltage Match (Note 6)	LT1112CN8 LT1112S8, LT1114CN/S	● ●		45 55	170 220		60 70	225 270	μV μV
	Offset Voltage Match Drift (Notes 6, 9)	LT1112CN8 LT1112S8, LT1114CN/S	● ●		0.2 0.4	0.7 1.6		0.3 0.5	1.0 1.8	μV/°C μV/°C
	Noninverting Bias Current Match (Notes 6, 7)	LT1114S	● ●		120	660		150 190	770 1300	nA nA
3	Common Mode Rejection Ratio	(Notes 6, 8)	●	114	134		109	134		dB
4	Power Supply Rejection Ratio	(Notes 6, 8)	●	110	125		107	125		dB

denotes the specifications which apply over the full operating temperature range of −40°C ≤ T_A ≤ 85°C, otherwise specifications T_A = 25°C, V_S = ±15V, unless otherwise noted. **(Note 12)**

OL	PARAMETER	CONDITIONS (Note 3)		LT1112ACN8 LT1114ACN MIN	TYP	MAX	LT1112CN8/IN8/S8/IS8 LT1114CN/S/IS MIN	TYP	MAX	UNITS
	Input Offset Voltage	LT1112CN8/IN8 LT1112S8/IS8, LT1114CN/S/IS V_S = ±1.2V	● ● ●		40 40 55	170 135 200		55 45 60	250 160 240	μV μV μV
	Average Input Offset Voltage Drift	LT1112CN8/IN8 LT1112S8/IS8, LT1114CN/S/IS	● ●		0.35 0.30	0.50 1.10		0.35 0.40	0.75 1.35	μV/°C μV/°C
	Input Offset Current	LT1114S/IS	● ●		70	330		85 110	430 630	nA nA
	Input Bias Current	LT1114S/IS	● ●		−210	−530		−120 −150	−350 −600	nA nA
	Input Voltage Range		●	±13.5	±14.1		±13.5	±14.1		V
	Common Mode Rejection Ratio	V_{CM} = ±13.5V	●	117	132		112	132		dB
	Power Supply Rejection Ratio	V_S = ±1.2V to ±20V	●	113	125		111	125		dB
	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10kΩ V_O = ±10V, R_L = 2kΩ	● ●	700 400	3300 1100		600 300	3300 900		V/mV V/mV
	Output Voltage Swing	R_L = 10kΩ	●	±13.0	±13.55		±13.0	±13.55		V
	Slew Rate		●	0.15	0.24		0.13	0.24		V/μs
	Supply Current per Amplifier		●		370	450		370	510	μA
	Offset Voltage Match (Note 6)	LT1112CN8/IN8 LT1112S8/IS8, LT1114CN/S/IS	● ●		50 60	180 230		60 70	225 270	μV μV
	Offset Voltage Match Drift (Notes 6)	LT1112CN8/IN8 LT1112S8/IS8, LT1114CN/S/IS	● ●		0.2 0.4	0.7 1.6		0.3 0.5	1.0 1.8	μV/°C μV/°C
	Noninverting Bias Current Match (Notes 6, 7)	LT1114S/IS	● ●		140	660		150 190	770 1300	nA nA
3	Common Mode Rejection Ratio	(Notes 6, 8)	●	113	133		109	133		dB
	Power Supply Rejection Ratio	(Notes 6, 8)	●	110	127		107	127		dB

Stresses beyond those listed under Absolute Maximum Ratings use permanent damage to the device. Exposure to any Absolute Im Rating condition for extended periods may affect device ty and lifetime.

: Differential input voltages greater than ±0.7V cause excessive to flow through the input protection diodes unless limiting ice is used.

Note 3: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers, i.e., out of 100 LT1114s, 130 LT1112s typically 240 op amps for 120) will be better than the indicated specification.

Note 4: [illegible]

1112 1416

ECTRICAL CHARACTERISTICS

[illegible] Offset voltage, [illegible] rejection [illegible] the [illegible] supply voltage.

[illegible] Matching [illegible] between amplifiers A and [illegible] between B and C [illegible] the two amplifiers on the [illegible]

[illegible] This parameter is [illegible] between [illegible] noninverting input [illegible]

[illegible] ΔCMRR and ΔPSRR [illegible] CMRR and PSRR [illegible] the difference [illegible]

[illegible]

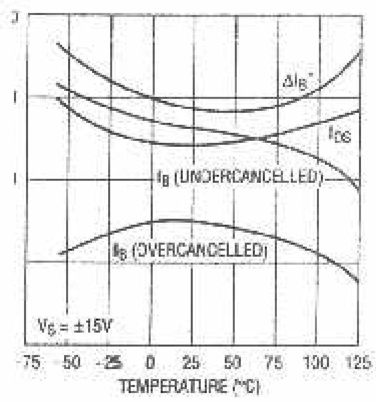
Note 10: These parameters are not tested. [illegible] op amps [illegible] limits. [illegible] at 1kHz.

Note 11: [illegible] LT1112AC/LT1112C [illegible] LT1114AC/ [illegible] are guaranteed functional over the temperature range of −40°C to 85°C.

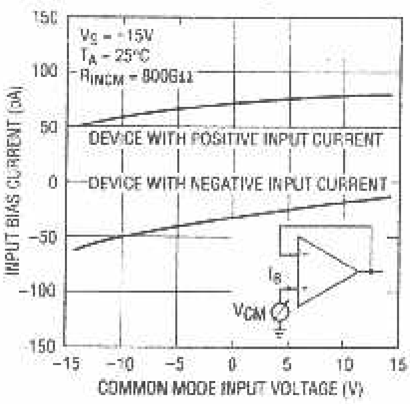
Note 12: The LT1112AC/LT1112C [illegible] are guaranteed to meet specified performance from 0°C to 70°C and are designed, characterized and expected to meet specified performance from −40°C to 85°C, but are not tested or QA sampled at these temperatures. The LT1112I/LT1114I are guaranteed to meet specified performance from −40°C to 85°C.

PICAL PERFORMANCE CHARACTERISTICS

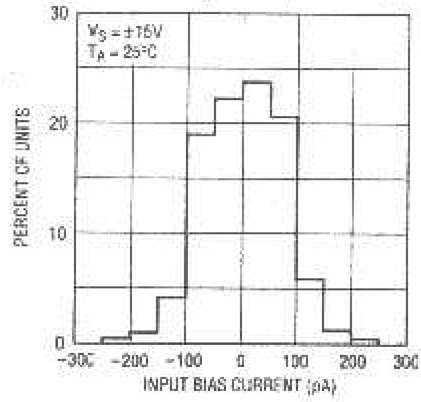
Input Bias and Offset Current, Noninverting Bias Current Match vs Temperature



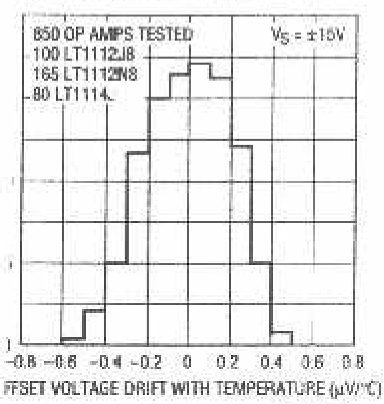
Input Bias Current Over Common Mode Range



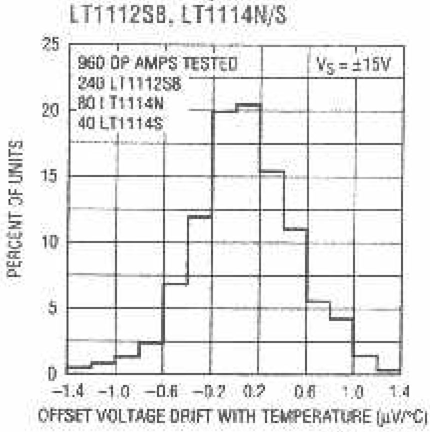
Distribution of Input Bias Current (In All Packages Except LT1114S)



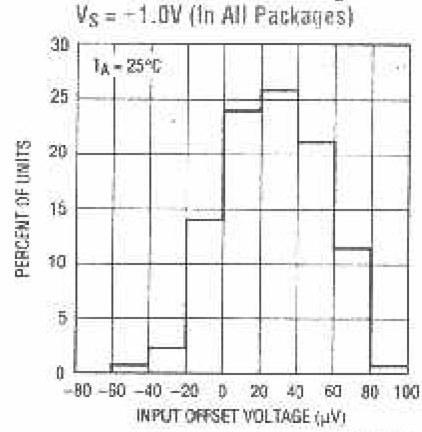
Drift with Temperature LT1112N8/J8, LT1114J



Drift with Temperature LT1112S8, LT1114N/S

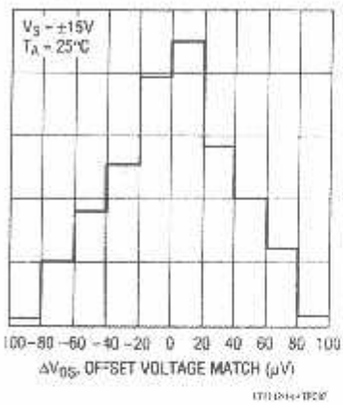


Distribution of Offset Voltage at $V_S = \pm1.0V$ (In All Packages)

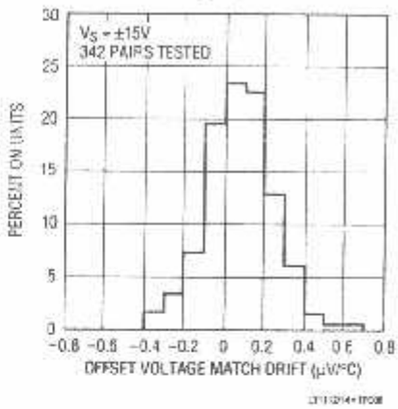


ICAL PERFORMANCE CHARACTERISTICS

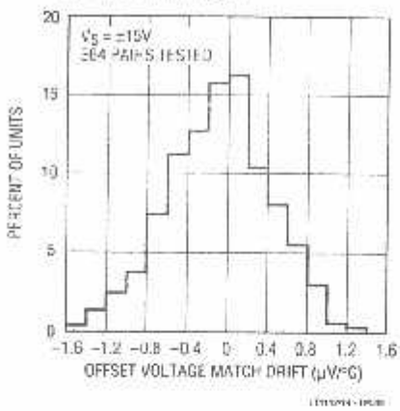
Distribution of Offset Voltage Match



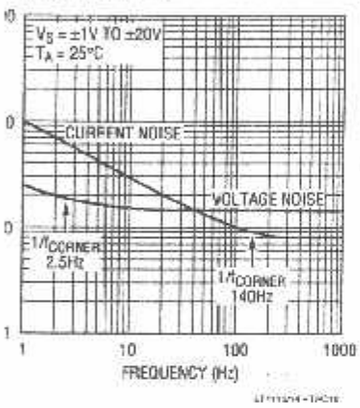
Distribution of Offset Voltage Match Drift (LT1112J8, LT1112N8, LT1114J Packages)



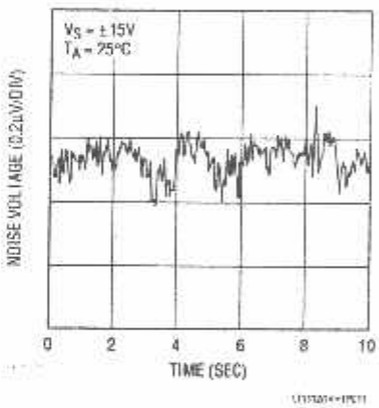
Distribution of Offset Voltage Match Drift (LT1112S8, LT1114N, LT1114S Packages)



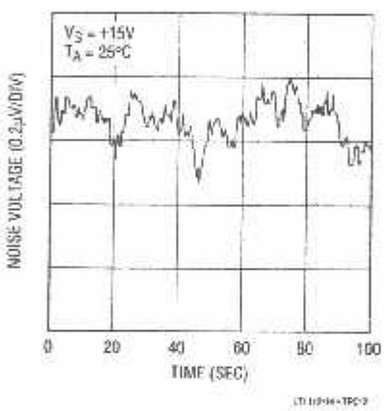
Noise Spectrum



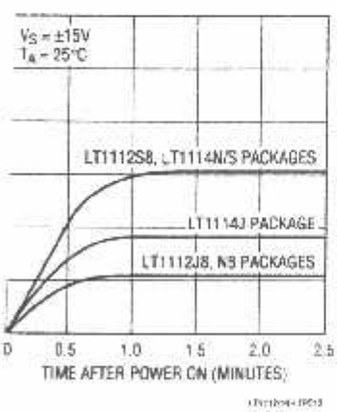
0.1Hz to 10Hz Noise



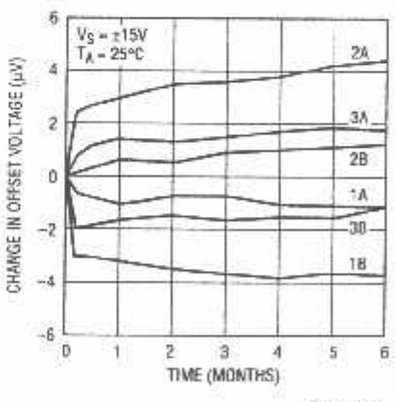
0.01Hz to 1Hz Noise



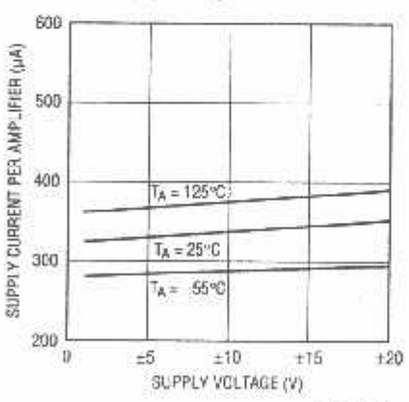
Warm-Up Drift



Long Term Stability of Three Representative Units

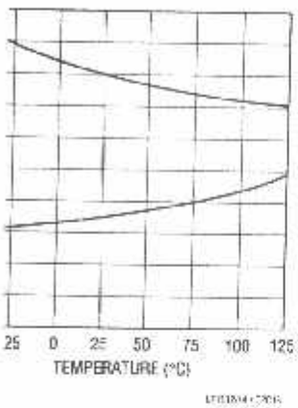


Supply Current per Amplifier vs Supply Voltage

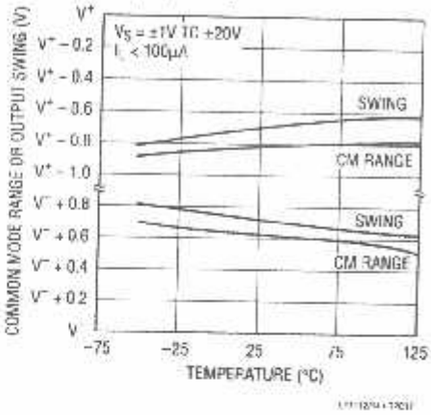


'AL PERFORMANCE CHARACTERISTICS

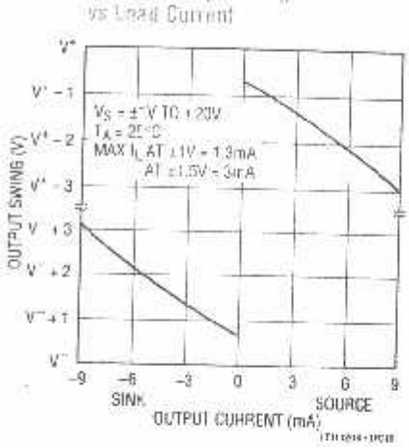
imum Supply Voltage vs Temp
age Gain at Minimum Supply
age



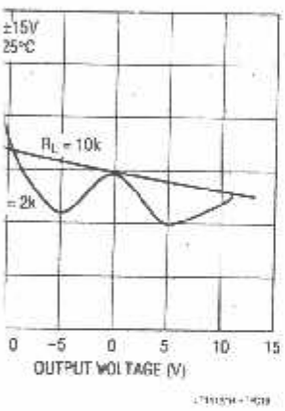
Common Mode Range and Voltage Swing with Respect to Supply Voltages



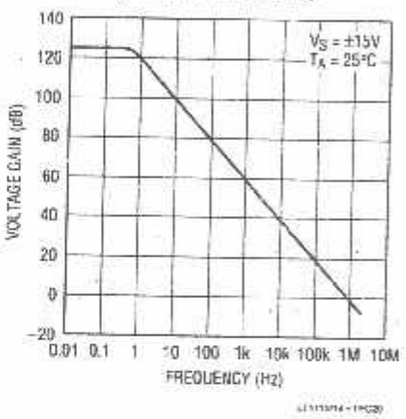
Output Voltage Swing vs Load Current



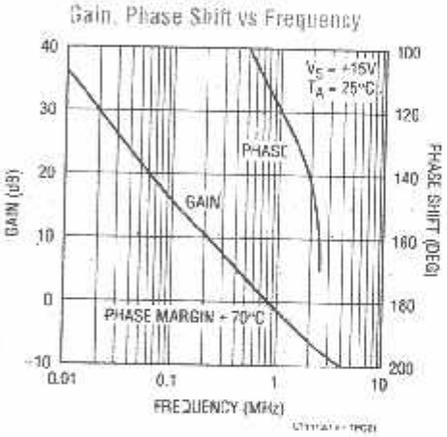
ige Gain



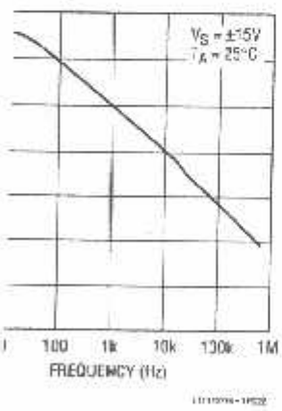
Voltage Gain vs Frequency



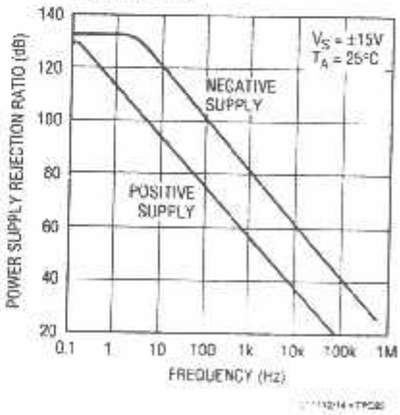
Gain, Phase Shift vs Frequency



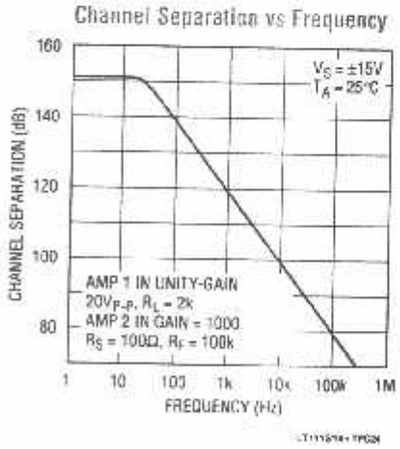
on Mode Rejection
quency



Power Supply Rejection vs Frequency

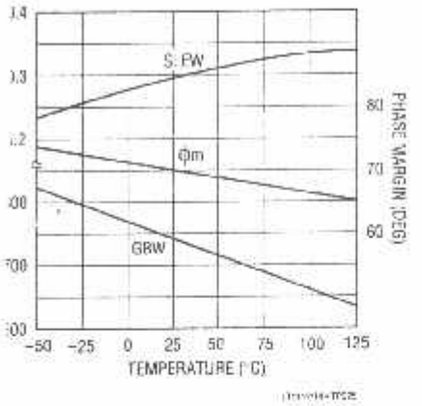


Channel Separation vs Frequency

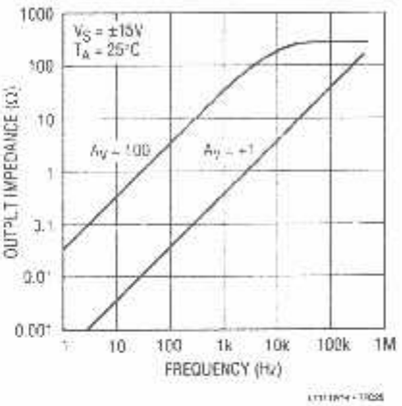


ICAL PERFORMANCE CHARACTERISTICS

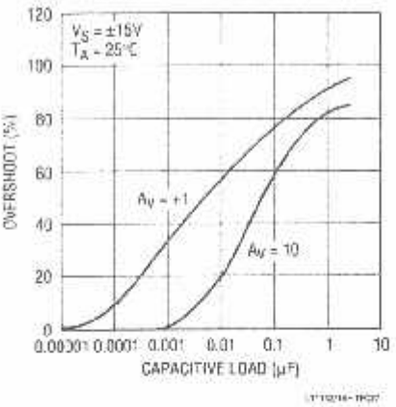
Slew Rate, Gain-Bandwidth Product and Phase Margin vs Temperature



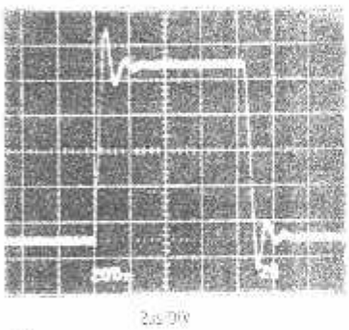
Closed-Loop Output Impedance



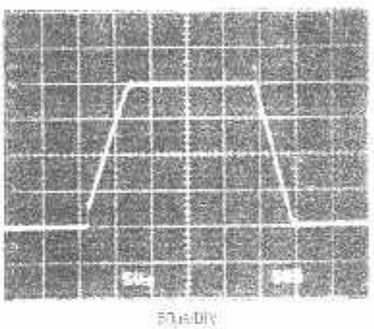
Capacitive Loading Handling



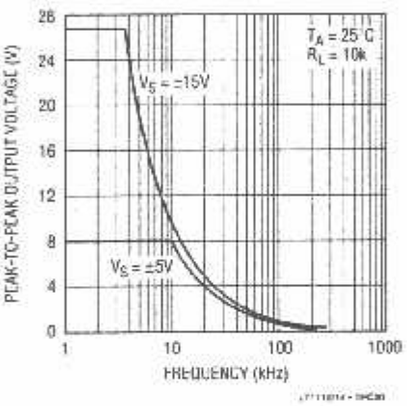
Small-Signal Transient Response



Large-Signal Transient Response



Undistorted Output Voltage vs Frequency



CATIONS INFORMATION

112 dual and LT1114 quad in the plastic and DIP packages are pin compatible to and directly uch precision op amps as the OP-200, OP-297 uals and OP-400, OP-497, AD704 quads with l price/performance.

112 in the S8 surface mount package has the pin configuration i.e. the same configuration as c and ceramic DIP packages.

114 quad is offered in the narrow 16-pin surface ackage. All competitors are in the wide 16-pin which occupies 1.8 times the area of the narrow The wide package is also 1.8 times thicker than w package.

s of the LT1112/1114 are protected with back-to-tes. In the voltage follower configuration, when is driven by a fast large signal pulse (>1V), the tection diodes effectively short the output to the ing slewing, and a current, limited only by the hort-circuit protection, will flow through the

f a feedback resistor is recommended because tor keeps the current below the short-circuit lting in faster recovery and settling of the output.

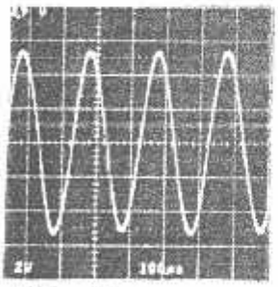
voltage of the LT1112/1114 should never ex-supply voltages by more than a diode drop. the example below shows that as the input ceeds the common mode range, the LT1112's output clips cleanly, without any glitches or phase reversal. The OP-297 exhibits phase reversal. The photos also illustrate that both the input and output ranges of the LT1112 are within 800mV of the supplies. The effect of input and output overdrive on the other amplifiers in the LT1112 or LT1114 packages is negligible, as each amplifier is biased independently.

Advantages of Matched Dual and Quad Op Amps

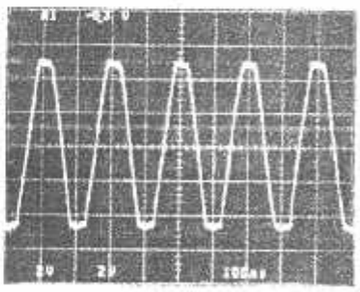
In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the LT1112. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two noninverting input currents (I_B^+). The difference between these two currents (ΔI_B^+) is the offset current of the instrumentation amplifier. Common mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

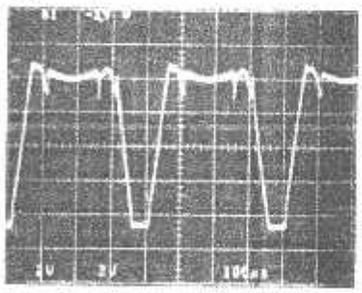
Voltage Follower with Input Exceeding the Common Mode Range (V_S = ±5V)



INPUT 5V/DIV 5ms/DIV



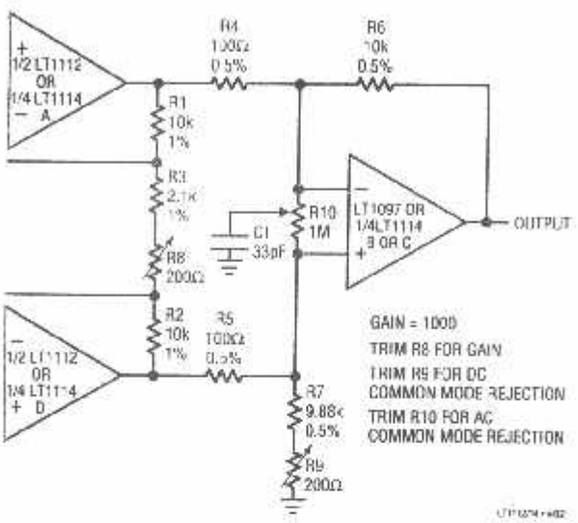
LT1112 OUTPUT



OP-297 OUTPUT

PLICATIONS INFORMATION

Three Op Amp Instrumentation Amplifier



oncepts of common mode and power supply rejec-ratio match (ΔCMRR and ΔPSRR) are best demon-ed with a numerical example:

sume $CMRR_A$ = +1μV/V or 120dB
d $CMRR_B$ = +0.75μV/V or 122.5dB,
en ΔCMRR = 0.25μV/V or 132dB;
$CMRR_B$ = −0.75μV/V which is still 122.5dB,
en ΔCMRR = 1.75μV/V or 115dB.

ly the LT1112/LT1114, by specifying and guarantee-l of these matching parameters, can significantly ove the performance of matching-dependent ts.

Typical performance of the instrumentation amplifier:

Input offset voltage = 35μV
Offset voltage drift = 0.3μV/°C
Input bias current = 80pA
Input offset current = 100pA
Input resistance = 300GΩ
Input noise = 0.42μV_{P-P}

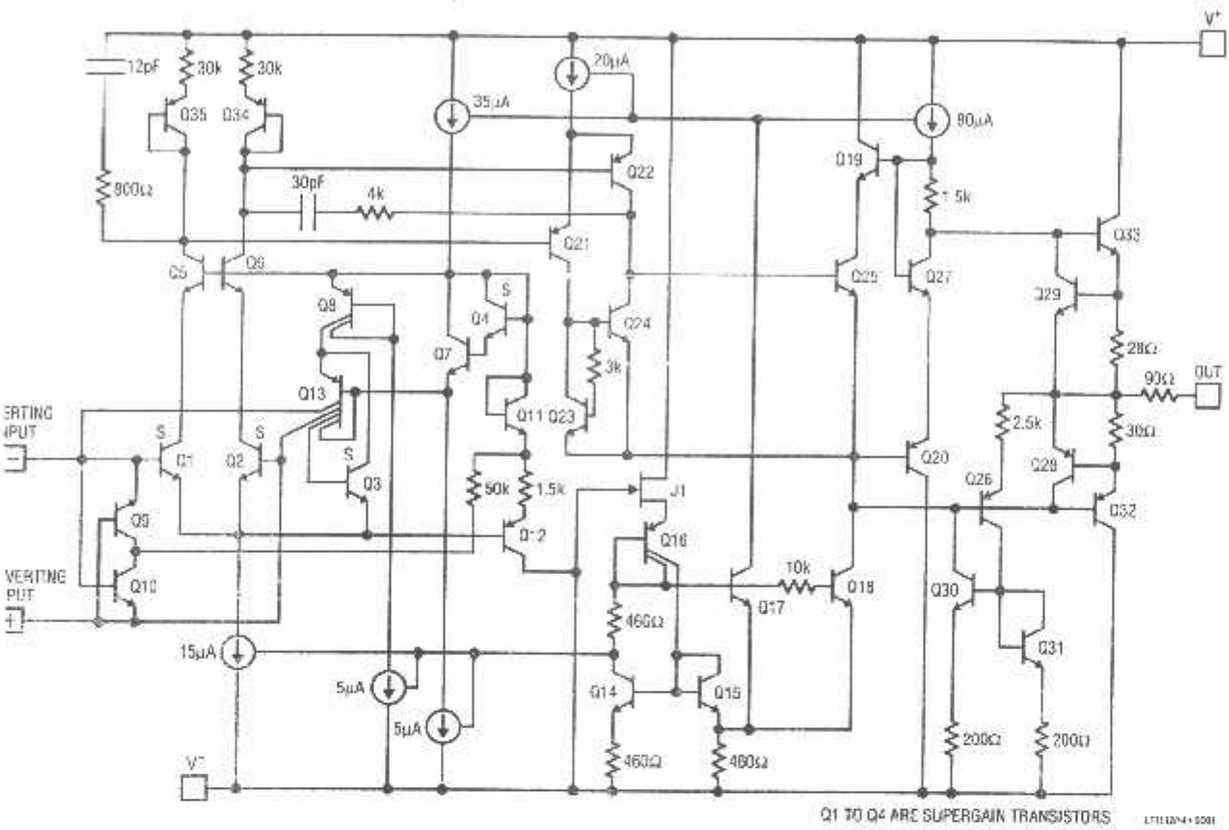
When the instrumentation amplifier is used with high impedance sources, the LT1114 is recommended because its CMRR vs. frequency performance is better than the LT1112's. For example, with two matched 1MΩ source resistors, CMRR at 100Hz is 100dB with the LT1114, 76dB with the LT1112.

This difference is explained by the fact that capacitance between adjacent pins on an IC package is about 0.25pF (including package, socket and PC board trace capacitances).

On the dual op amp package, positive input A is next to the V^- pin (AC ground), while positive input B has no AC ground pin adjacent to it, resulting in a 0.25pF input capacitance mismatch. At 100Hz, 0.25pF represents a $6.4 \cdot 10^9$ input impedance mismatch, which is only 76dB higher than the 1MΩ source resistors.

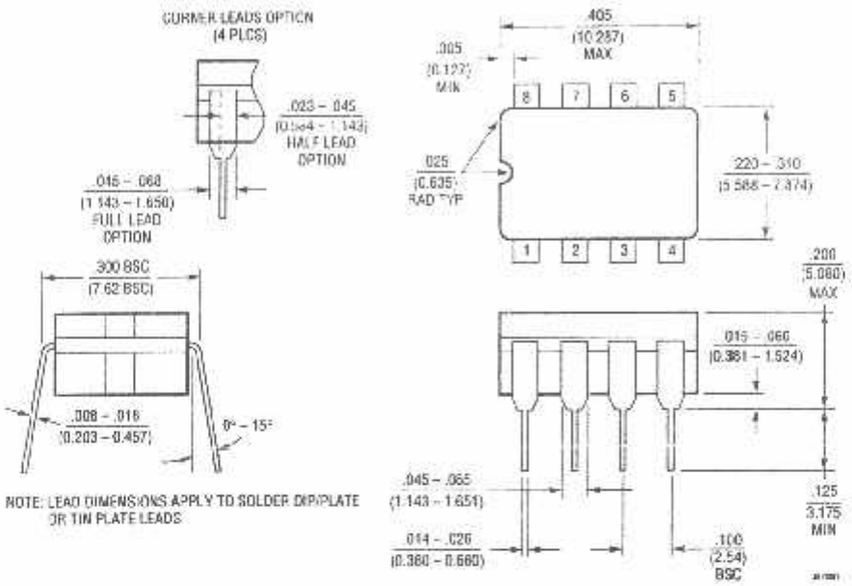
On the quad package, all four inputs are adjacent to a power supply terminal—therefore, there is no mismatch.

!EMATIC DIAGRAM (1/2 LT1112, 1/4 LT1114)

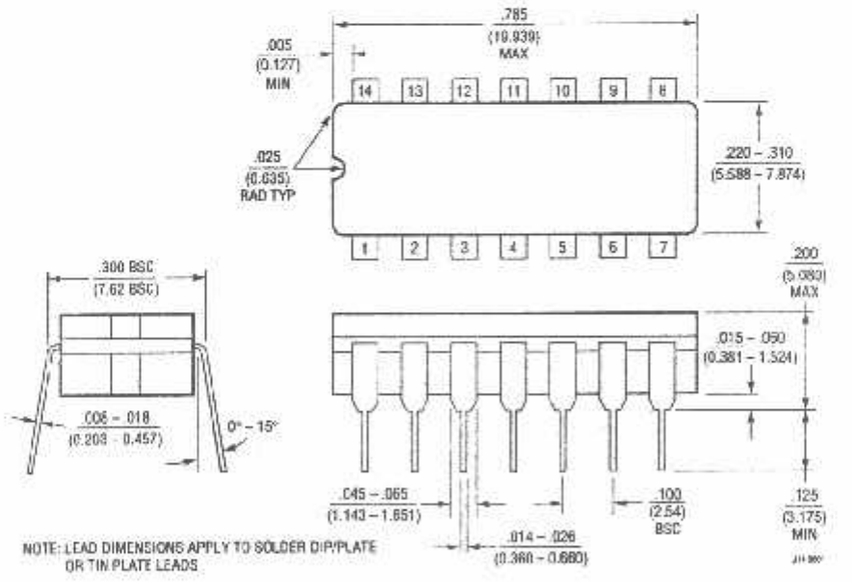


CKAGE DESCRIPTION

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



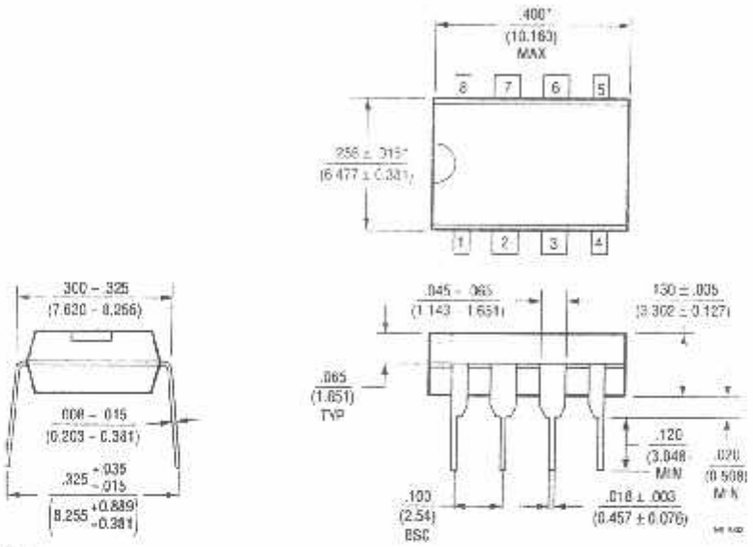
J Package
14-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGES

CKAGE DESCRIPTION

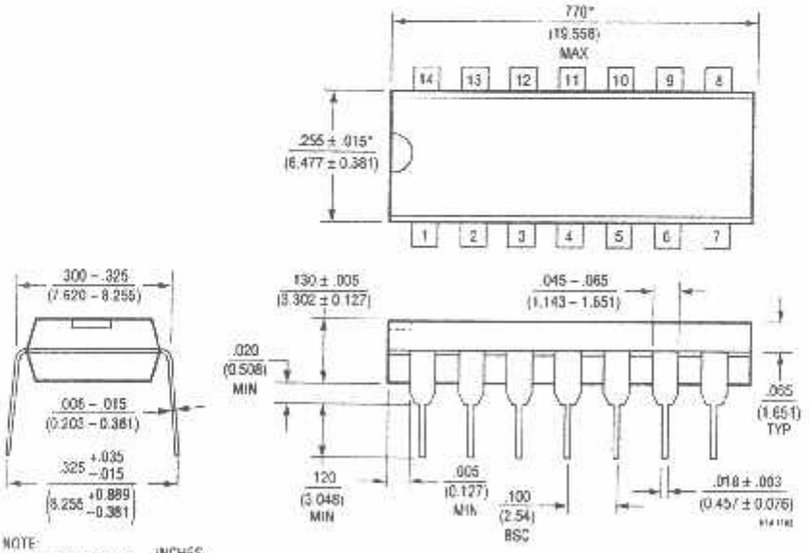
N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

N Package
14-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

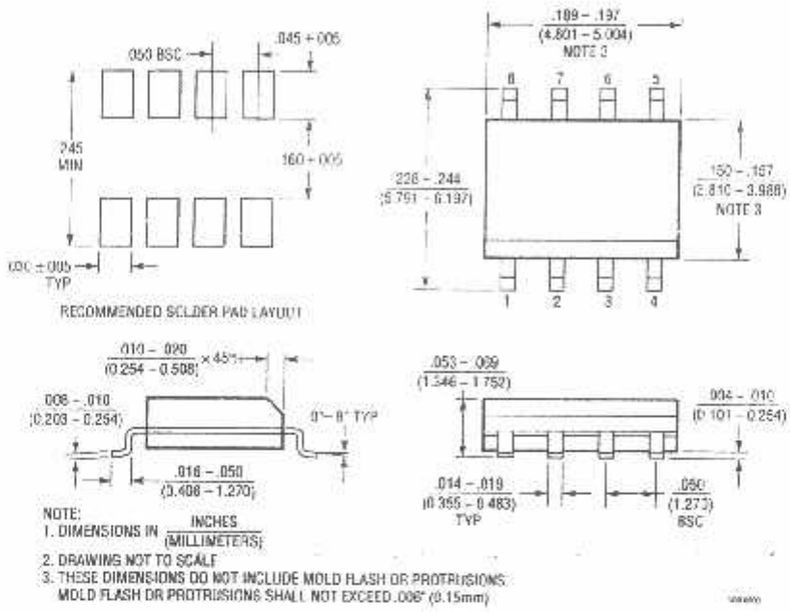


NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

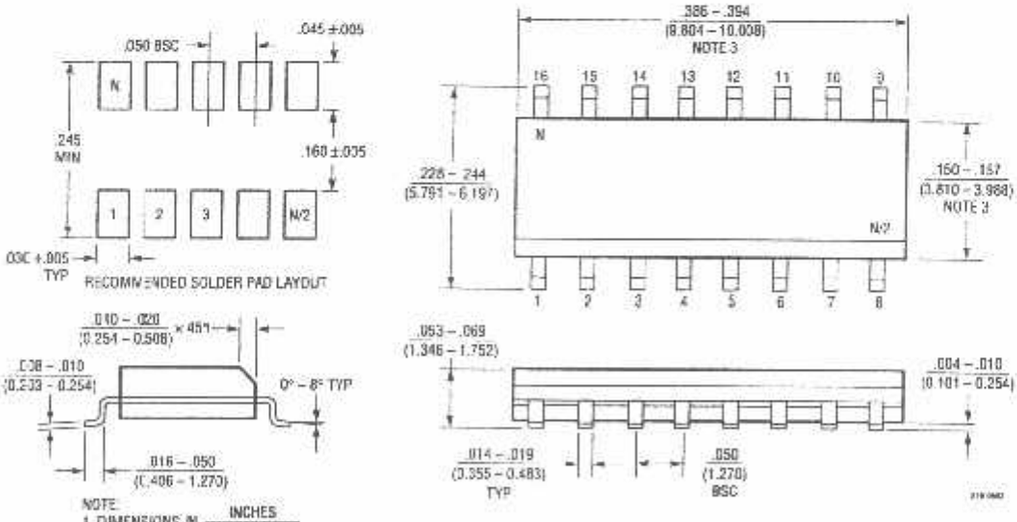
CKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

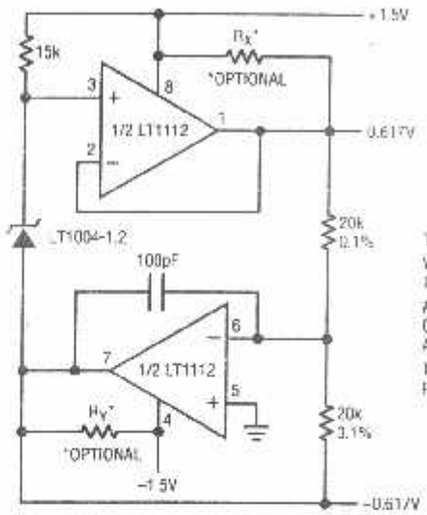
S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

ICAL APPLICATION

Dual Buffered 1.617V Reference Powered by Two AA Batteries



TOTAL SUPPLY CURRENT = 730µA
WORKS WITH BATTERIES DISCHARGED TO 1.3V
AT ±1.5V: MAXIMUM LOAD CURRENT = 800µA
CAN BE INCREASED WITH OPTIONAL R_X, R_Y
AT $R_X = R_Y = 750\Omega$ LOAD CURRENT = 2mA
TEMPERATURE COEFFICIENT LIMITED BY REFERENCE = 20ppm/°C

ATED PARTS

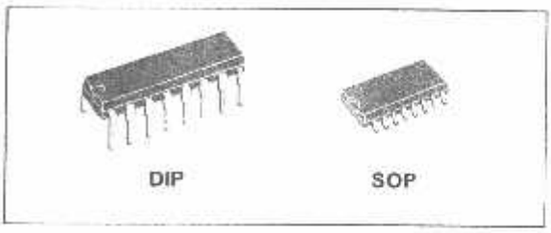
UMBER	DESCRIPTION	COMMENTS
	Rail-to-Rail Output, Picoamp Input Precision Op Amp	SOT-23
LT1882	Dual/Quad Rail-to-Rail Output, Picoamp Input Precision Op Amp	C_{LOAD} Up to 1000pF
LT1885	Dual/Quad Rail-to-Rail Output, Picoamp Input Precision Op Amp	9.5nV/√Hz Input Noise
LT6012	Dual/Quad Rail-to-Rail Output, Picoamp Input Precision Op Amp	35uA Supply Current, 14nV/√Hz

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0297 REV B • PRINTED IN USA
LINEAR TECHNOLOGY CORPORATION 1992

HCF4017B

DECADE COUNTER WITH 10 DECODED OUTPUTS

- MEDIUM SPEED OPERATION : 10 MHz (Typ.) at V_{DD} = 10V
- FULLY STATIC OPERATION
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



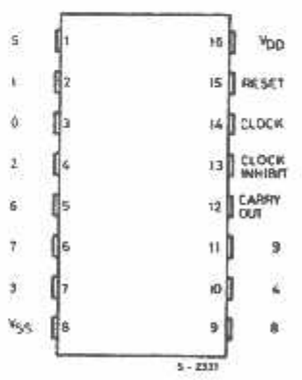
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4017BEY	
SOP	HCF4017BM1	HCF4017M013TR

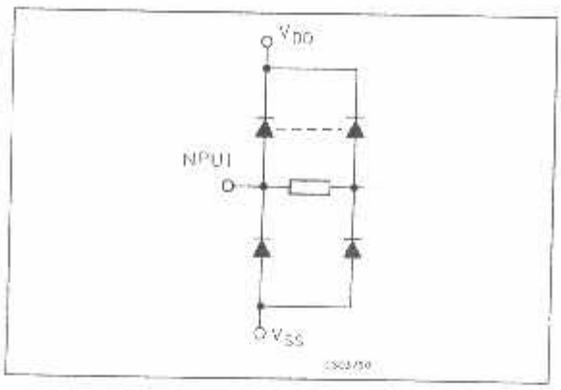
DESCRIPTION

The HCF4017B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
The HCF4017B is 5-stage Johnson counter having 10 decoded outputs. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the clock input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times. This counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advanced via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson decade-counter configuration permits high speed operation, 2-input decimal decode gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY - OUT signal completes one cycle every 10 clock input cycles and is used to ripple-clock the succeeding device in a multi-device counting chain.

PIN CONNECTION



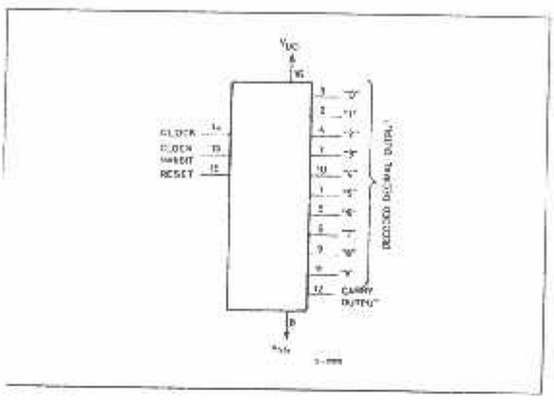
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 2, 4, 7, 10, 1, 5, 6, 9, 11	0 to 9	Decoded Decimal Output
14	CLOCK	Clock Input
13	CLOCK INHIBIT	Clock Inhibit Input
15	RESET	Reset Input
12	CARRY OUT	Carry Output
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM



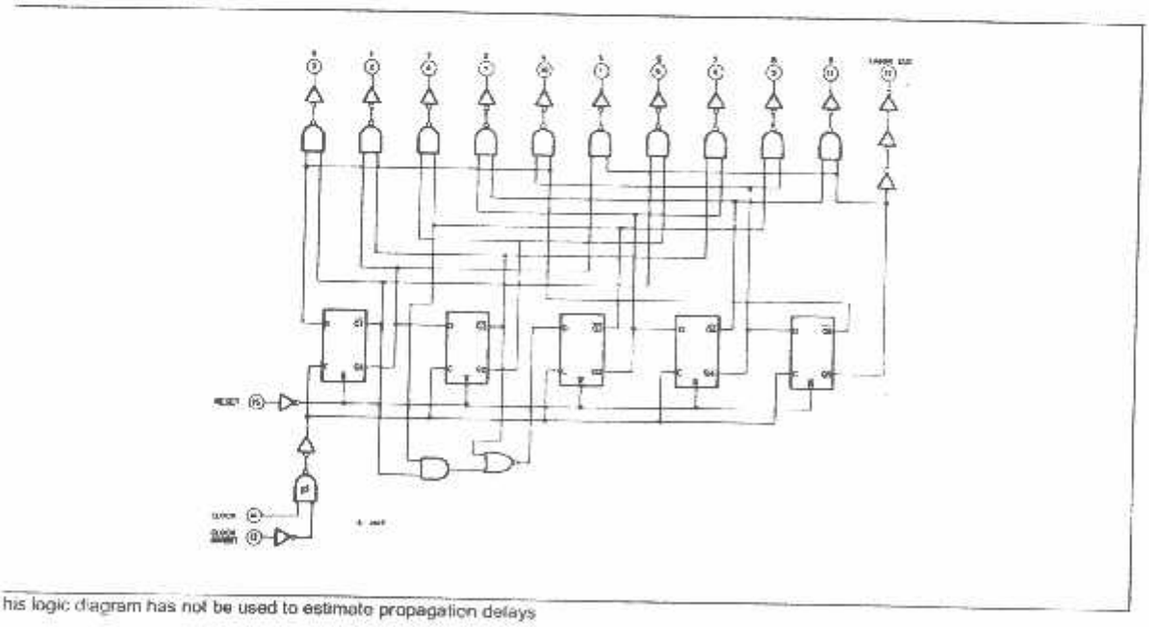
TRUTH TABLE

CLOCK	CLOCK INHIBIT	RESET	DECODED OUTPUT
X	X	H	Q_0
L	X	L	Q_n
X	H	L	Q_n
⌐	L	L	Q_{n+1}
¬	L	L	Q_n
H	⌐	L	Q_n
H	¬	L	Q_{n+1}

X : Don't Care

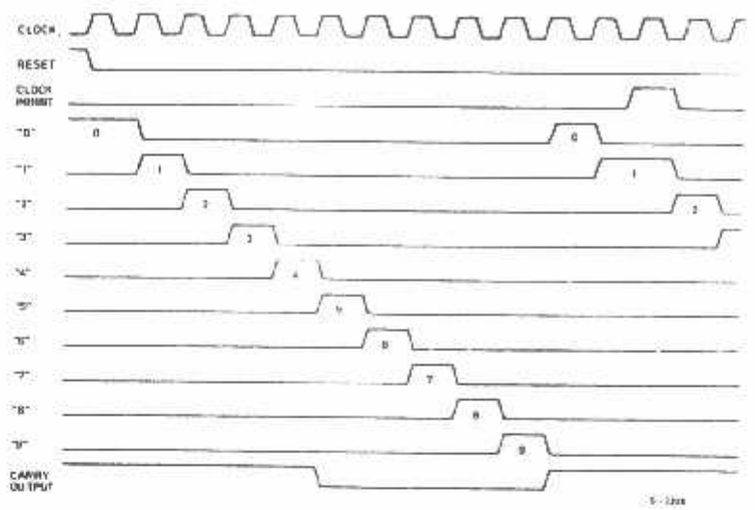
Qn : No Change

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (µA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	µA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	µA
C_I	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

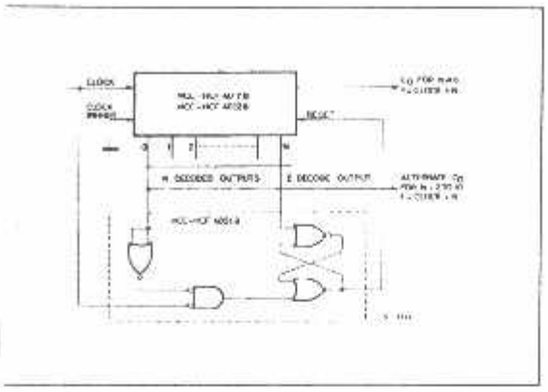
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition V_{DD} (V)	Value (*) Min.	Typ.	Max.	Unit
CLOCKED OPERATION						
t_{PLH} t_{PHL}	Propagation Delay Time (decode out)	5		325	650	ns
		10		135	270	
		15		85	170	
	Propagation Delay Time (carry out)	5		300	600	ns
		10		125	250	
		15		80	160	
t_{THL} t_{TLH}	Transition Time (carry out or decoded out lines)	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL} (1)	Maximum Clock Input Frequency	5	2.5	5	5	MHz
		10	5	10		
		15	5.5	11		
t_w	Minimum Clock Pulse Width	5		100	200	ns
		10		45	90	
		15		30	60	
t_r, t_f	Clock Input Rise or Fall Time	5	unlimited			µs
		10				
		15				
t_{setup}	Data Setup Time Minimum Clock Inhibit	5		115	230	ns
		10		50	100	
		15		35	75	
RESET OPERATION						
t_{PLH}, t_{PHL}	Propagation Delay Time (carry out or decoded out lines)	5		265	530	ns
		10		115	230	
		15		85	170	
t_w	Minimum Reset Pulse Width	5		130	260	ns
		10		55	110	
		15		30	60	
t_{REM}	Minimum Reset Removal Time	5		200	400	ns
		10		140	280	
		15		75	150	

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.
(1) Measured with respect to carry out line.

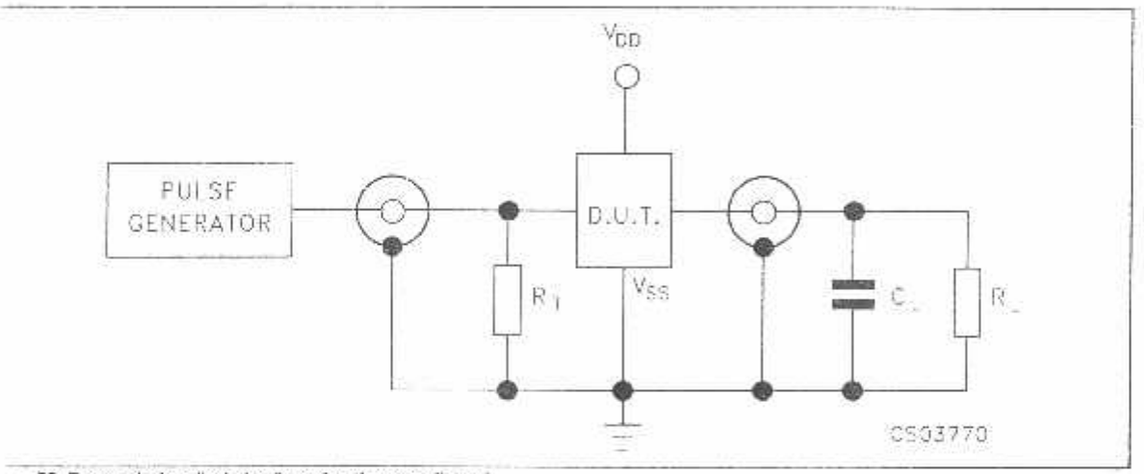
TYPICAL APPLICATIONS

DIVIDE BY N COUNTER(N ≤ 10) WITH DECODED OUTPUTS



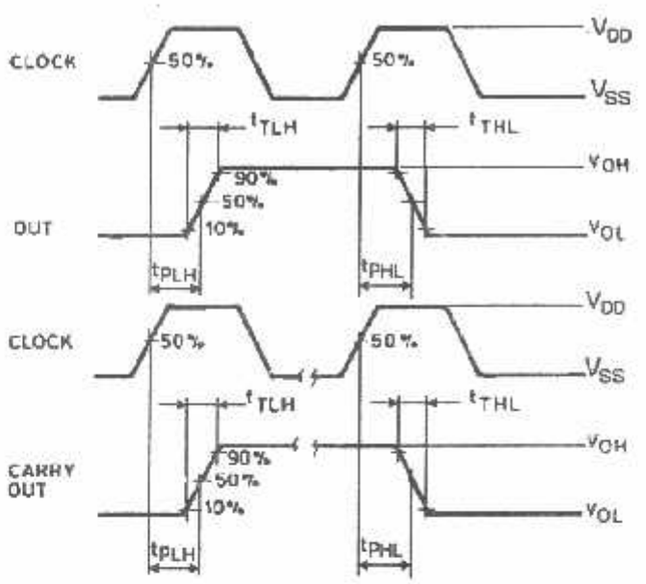
When the N^{th} decoded output is reached (N^{th} clock pulse) the S-R flip-flop (constructed from two NOR gates of the HCF4001B) generates a reset pulse which clears the HCF4017B to its zero count. At this time, if the N^{th} decoded output is greater than or equal to 6, the C_{OUT} line goes high to clock the next HCF4017B counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output high resets the S-R flip-flop to enable the HCF4017B. If the N^{th} decoded output is less than 6, the COUT line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

TEST CIRCUIT

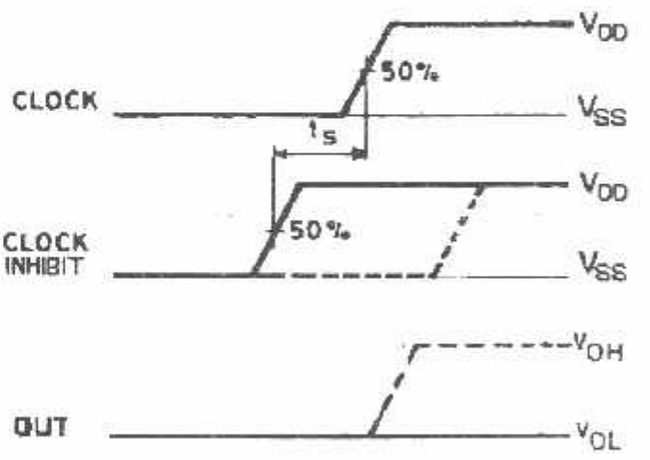


C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

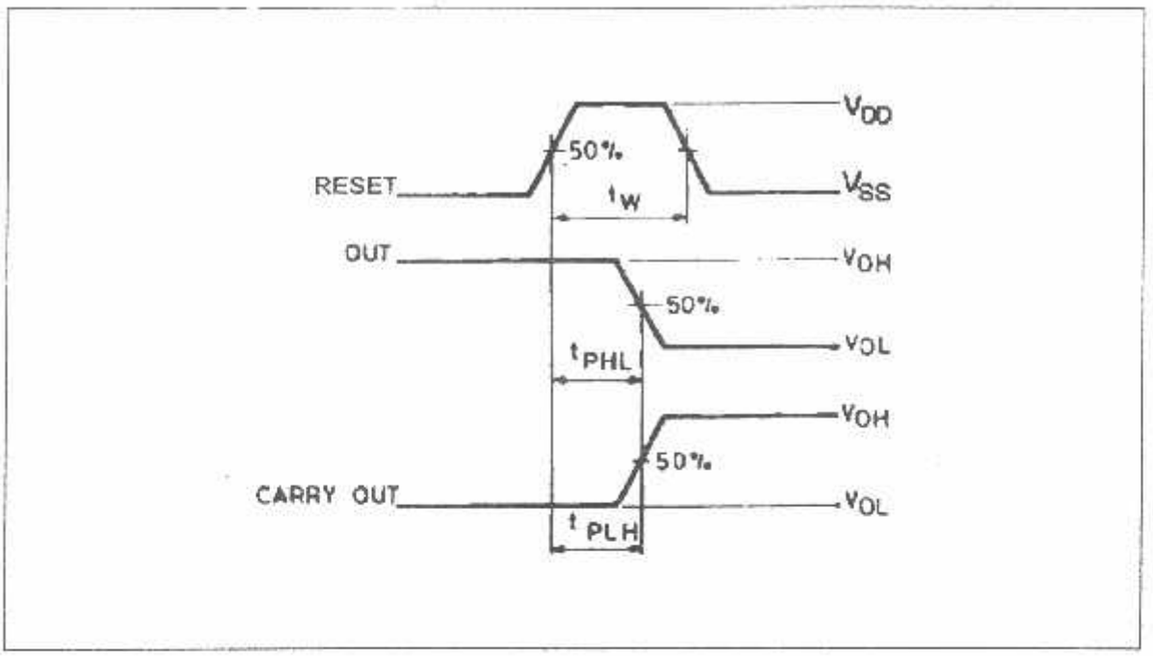
WAVEFORM 1 : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



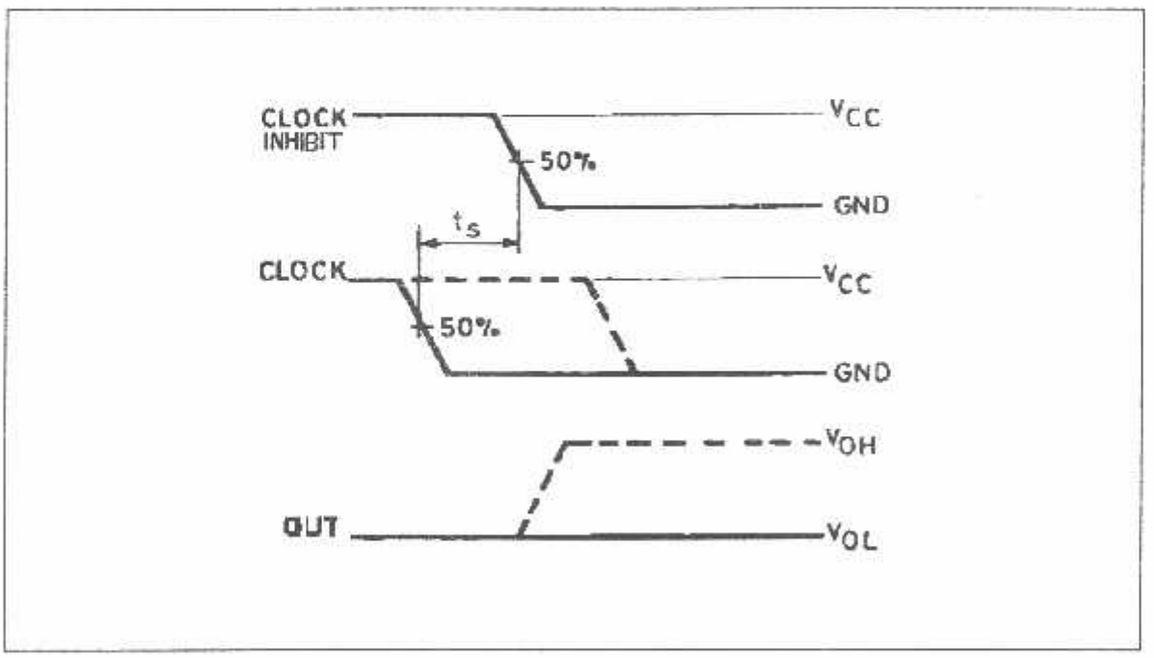
WAVEFORM 2 : MINIMUM SETUP TIME (CLOCK INHIBIT TO CLOCK) (f=1MHz; 50% duty cycle)



WAVEFORM 3 : PROPAGATION DELAY TIMES, MINIMUM RESET PULSE WIDTH (f=1MHz; 50% duty cycle)

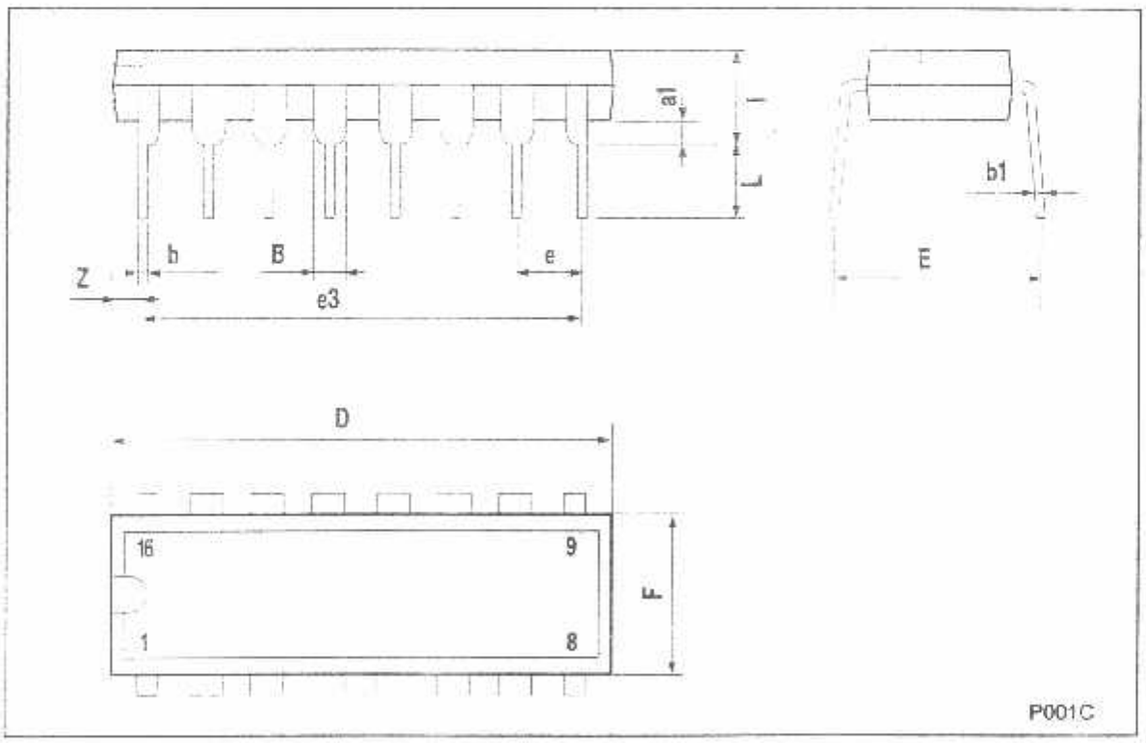


WAVEFORM 4 : MINIMUM SETUP TIME (CLOCK TO CLOCK INHIBIT) (f=1MHz; 50% duty cycle)



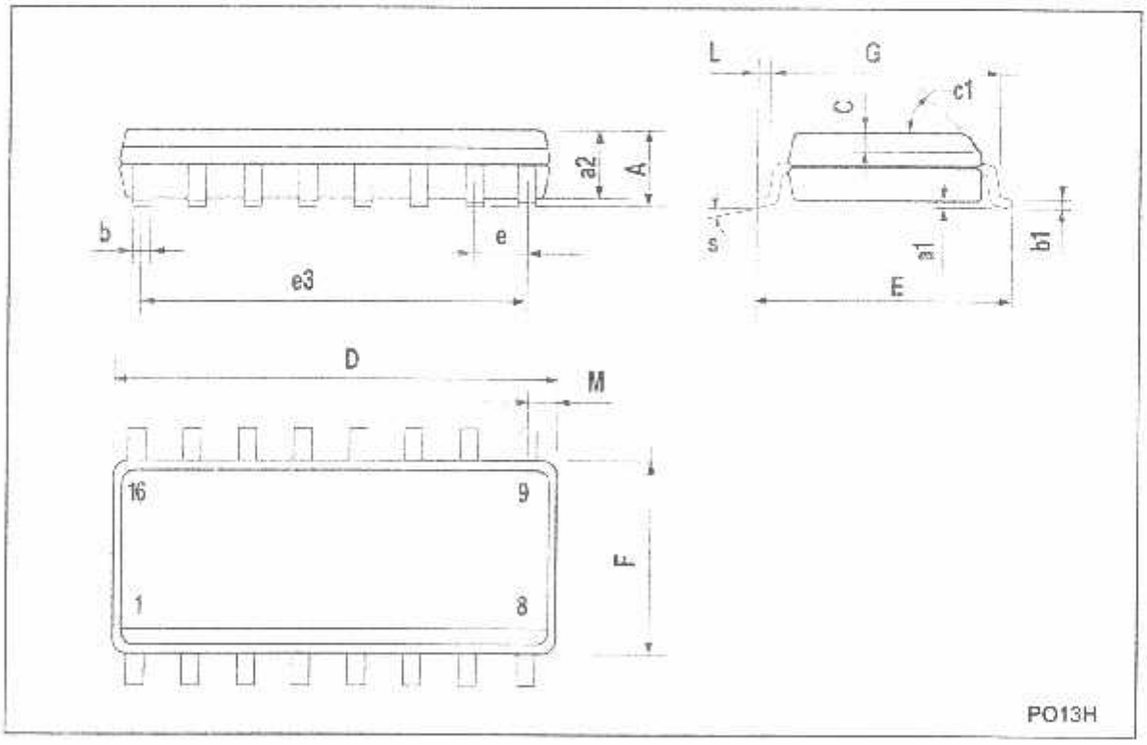
Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

National Semiconductor

February 2000

LM555
Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

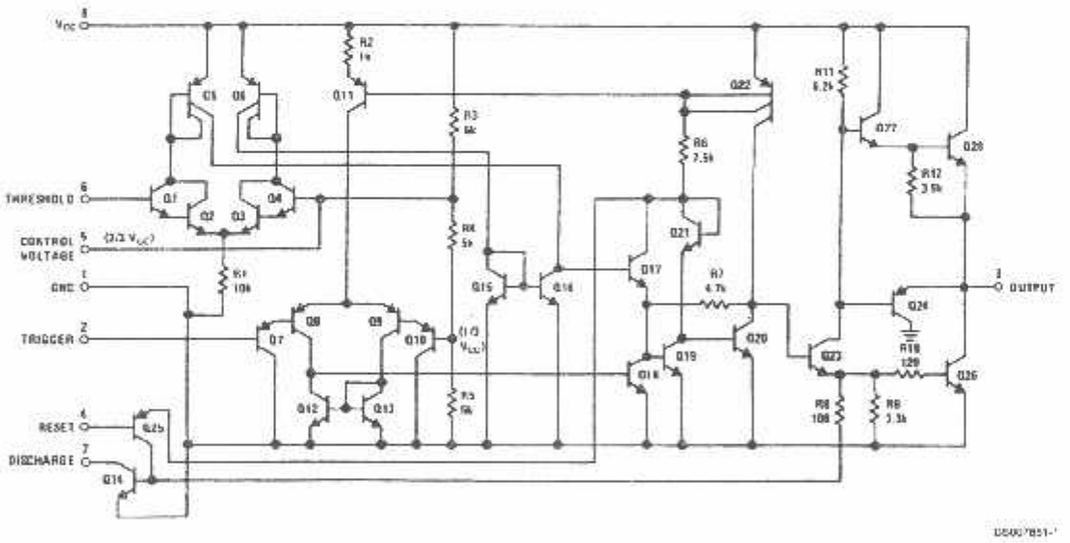
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

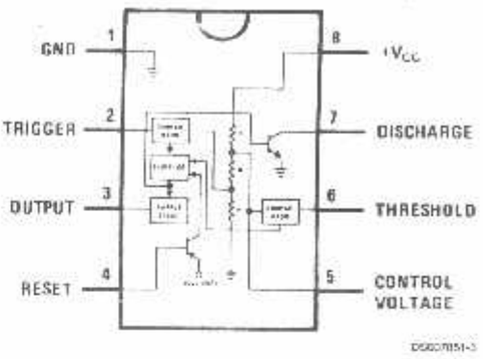
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Connection Diagram

Dual-In-Line, Small Outline
and Molded Mini Small Outline Packages



DS007851-3

Top View

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

solute Maximum Ratings (Note 2)

ilitary/Aerospace specified devices are required, se contact the National Semiconductor Sales Office/ ributors for availability and specifications.

y Voltage	18V
er Dissipation (Note 3)	
V555CM, LM555CN	1160 mW
M555CMM	613 mW
rating Temperature Ranges	
M555C	0°C to +70°C
age Temperature Range	-65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Packages	
(SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ectrical Characteristics (Notes 1, 2)

..., 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
pply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 4)		10	12	mA
ing Error, Monostable					
itial Accuracy			1		%
ift with Temperature	R_A = 1k to 100kΩ, C = 0.1µF, (Note 5)		50		ppm/°C
ccuracy over Temperature			1.5		%
rift with Supply			0.1		%/V
ng Error, Astable					
tial Accuracy			2.25		%
ift with Temperature	R_A, R_B = 1k to 100kΩ, C = 0.1µF, (Note 5)		150		ppm/°C
ccuracy over Temperature			3.0		%
ift with Supply			0.30		%/V
shold Voltage			0.667		x V_{CC}
ger Voltage	V_{CC} = 15V		5		V
	V_{CC} = 5V		1.67		V
ger Current			0.5	0.9	µA
r Voltage		0.4	0.5	1	V
t Current			0.1	0.4	mA
shold Current	(Note 6)		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V	9	10	11	V
	V_{CC} = 5V	2.6	3.33	4	
Leakage Output High			1	100	nA
Sat (Note 7)					
utput Low	V_{CC} = 15V, I_L = 15mA		180		mV
utput Low	V_{CC} = 4.5V, I_L = 4.5mA		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	Limits LM555C			Units
		Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V				
	I_{SINK} = 10mA		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.75	V
	I_{SINK} = 100mA		2	2.5	V
	I_{SINK} = 200mA		2.5		V
	V_{CC} = 5V				
	I_{SINK} = 8mA				V
	I_{SINK} = 5mA		0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200mA, V_{CC} = 15V		12.5		V
	I_{SOURCE} = 100mA, V_{CC} = 15V	12.75	13.3		V
	V_{CC} = 5V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 106°C/W (DIP), 170°C/W (SO-8), and 204°C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

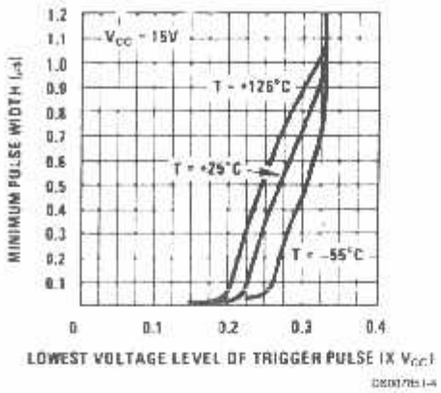
Note 6: This will determine the maximum value of R_A + R_B for 15V operation. The maximum total (R_A + R_B) is 20MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

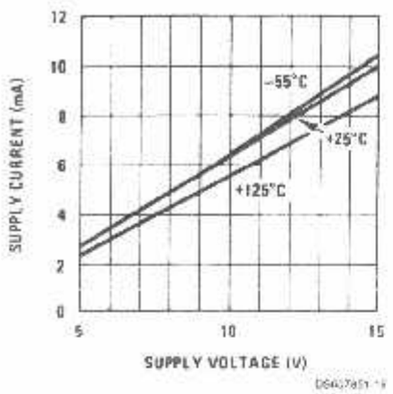
Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

ɔical Performance Characteristics

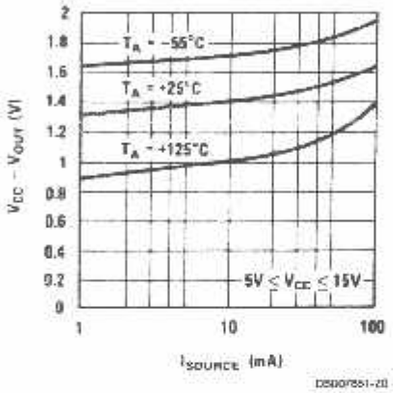
muim Pulse Width
ɹired for Triggering



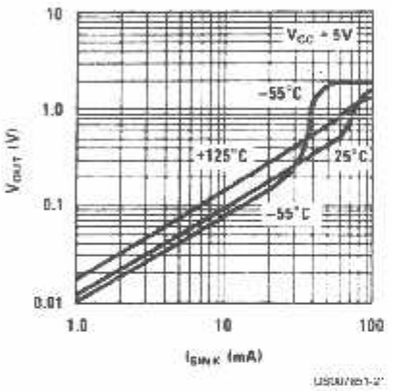
**Supply Current vs.
Supply Voltage**



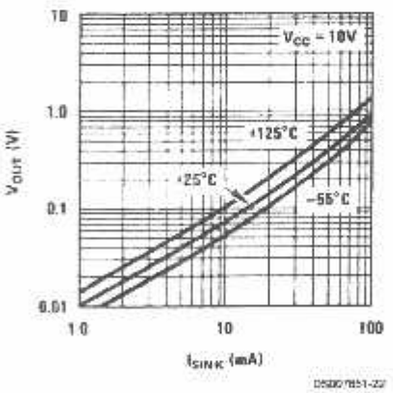
**ı Output Voltage vs.
ɲut Source Current**



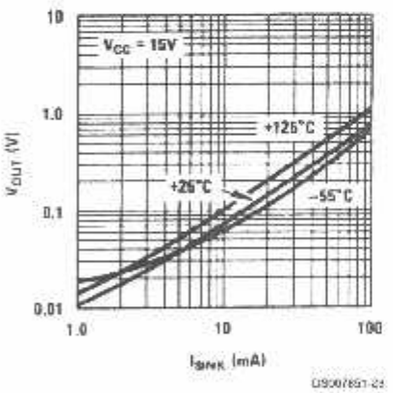
**Low Output Voltage vs.
Output Sink Current**



**Output Voltage vs.
ut Sink Current**

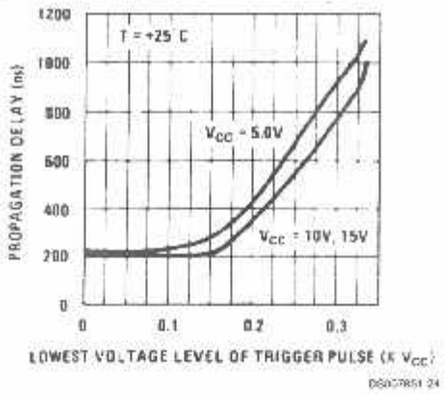


**Low Output Voltage vs.
Output Sink Current**

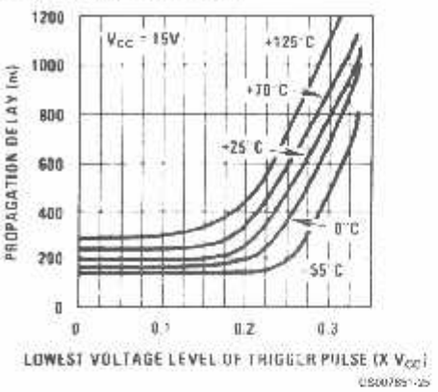


Typical Performance Characteristics (Continued)

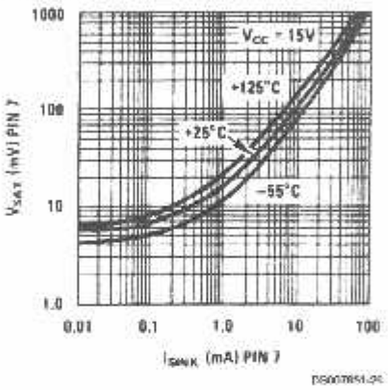
Output Propagation Delay vs.
Voltage Level of Trigger Pulse



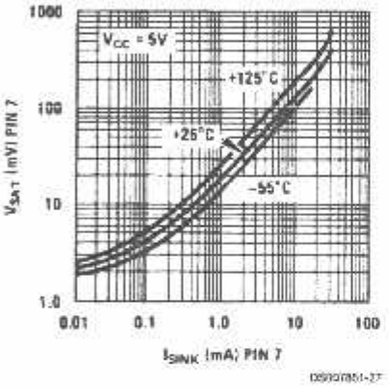
**Output Propagation Delay vs.
Voltage Level of Trigger Pulse**



**Discharge Transistor (Pin 7)
Voltage vs. Sink Current**



**Discharge Transistor (Pin 7)
Voltage vs. Sink Current**



olications Information

OSTABLE OPERATION

mode of operation, the timer functions as a one-shot re 1). The external capacitor is initially held discharged transistor inside the timer. Upon application of a nega- igger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set, both releases the short circuit across the capacitor, drives the output high.

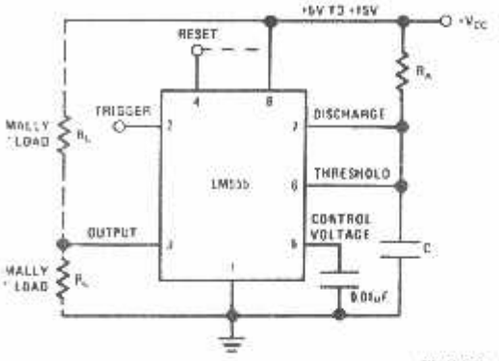
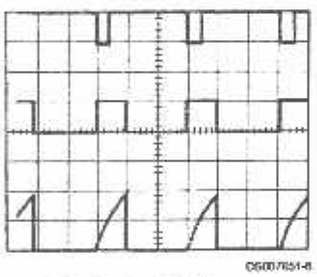


FIGURE 1. Monostable

oltage across the capacitor then increases exponen- ol a period of t = 1.1 R_A C, at the end of which time the ge equals 2/3 V_{CC}. The comparator then resets the p which in turn discharges the capacitor and drives the to its low state. *Figure 2* shows the waveforms gener- n this mode of operation. Since the charge and the old level of the comparator are both directly propor- to supply voltage, the timing interval is independent of .



V
0.1 ms/DIV.
1kΩ
1µF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

FIGURE 2. Monostable Waveforms

the timing cycle when the output is high, the further ation of a trigger pulse will not effect the circuit so long trigger input is returned high at least 10µs before the the timing interval. However the circuit can be reset this time by the application of a negative pulse to the terminal (pin 4). The output will then remain in the low until a trigger pulse is again applied.

the reset function is not in use, it is recommended that connected to V_{CC} to avoid any possibility of false trig- g.

e 3 is a nomograph for easy determination of R, C val- or various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

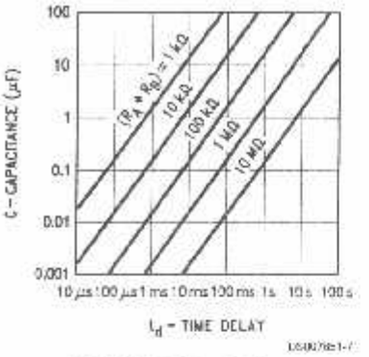


FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

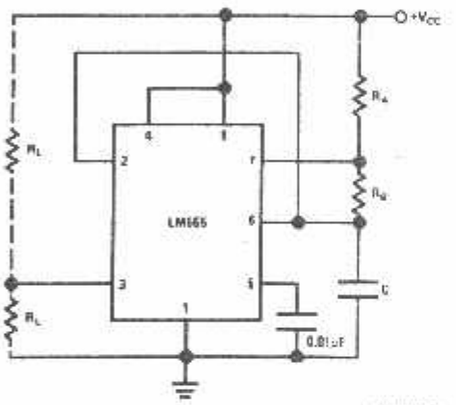
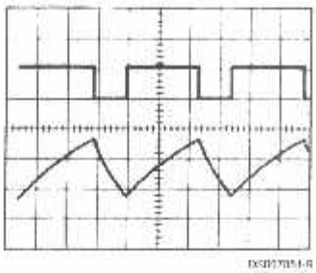


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



V_{CC} = 5V — Top Trace: Output 5V/Div.
TIME = 20μs/DIV. — Bottom Trace: Capacitor Voltage 1V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01μF

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

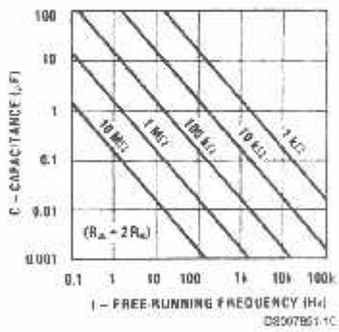
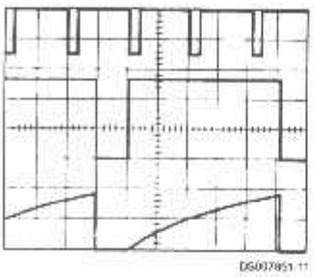


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



V_{CC} = 5V — Top Trace: Input 4V/Div.
TIME = 20μs/DIV. — Middle Trace: Output 2V/Div
R_A = 9.1kΩ — Bottom Trace: Capacitor 2V/Div
C = 0.01μF

FICURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

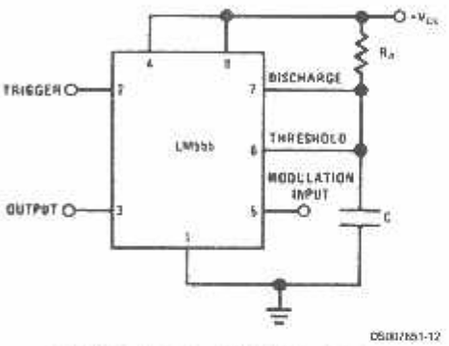
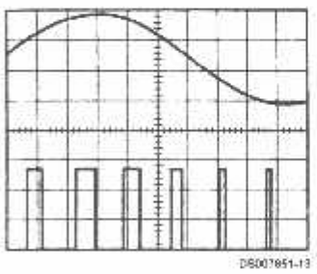


FIGURE 8. Pulse Width Modulator



V_{CC} = 5V — Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. — Bottom Trace: Output Voltage 2V/Div
R_A = 9.1kΩ
C = 0.01μF

FIGURE 9. Pulse Width Modulator

lications Information (Continued)

E POSITION MODULATOR

plication uses the timer connected for astable operas in *Figure 10*, with a modulating signal again applied control voltage terminal. The pulse position varies with odulating signal, since the threshold voltage and hence me delay is varied. *Figure 11* shows the waveforms ated for a triangle wave modulation signal.

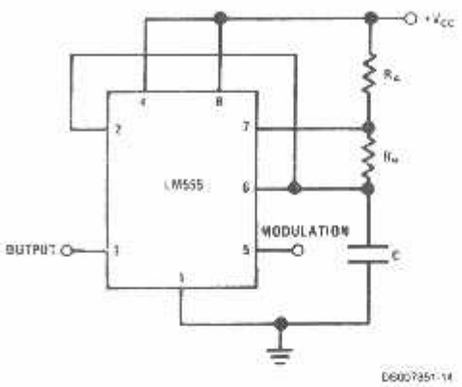
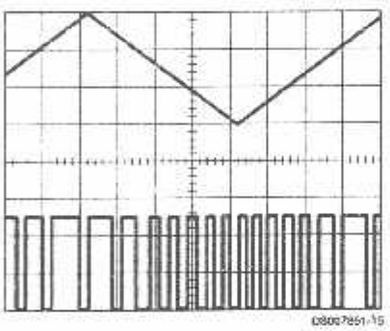


FIGURE 10. Pulse Position Modulator



V
0.1 ma/DIV.
kΩ
Ω
μF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output 2V/Div.

FIGURE 11. Pulse Position Modulator

R RAMP

the pull-up resistor, R_A, in the monostable circuit is re- by a constant current source, a linear ramp is gener- *Figure 12* shows a circuit configuration that will perform nction.

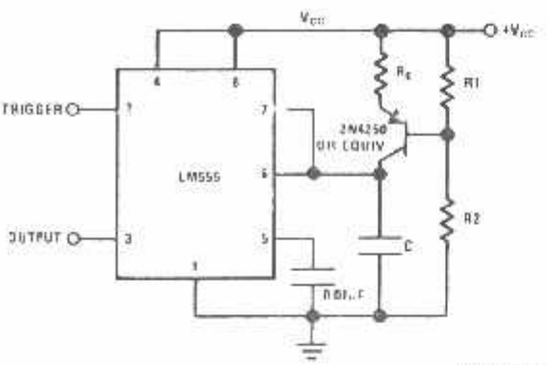


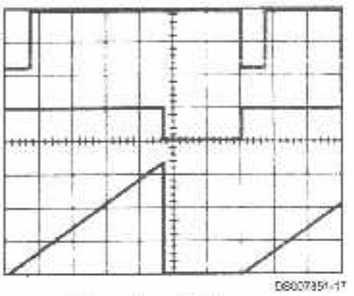
FIGURE 12.

Figure 13 shows waveforms generated by the circuit of *Figure 12*. The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 - R_2)\, C}{R_1\, V_{CC} - V_{BE}\,(R_1 + R_2)}$$

$$V_{BE} \simeq 0.6V$$

$$V_{RE} \simeq 0.6V$$



V_{CC} = 5V
TIME = 20μs/DIV.
R_1 = 47kΩ
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 μF

Top Trace: Input 3V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 13. Linear Ramp

Applications Information (Continued)

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A C$. For the output low it is $t_2 =$

$$\left[(R_A R_B)/(R_A + R_B)\right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$

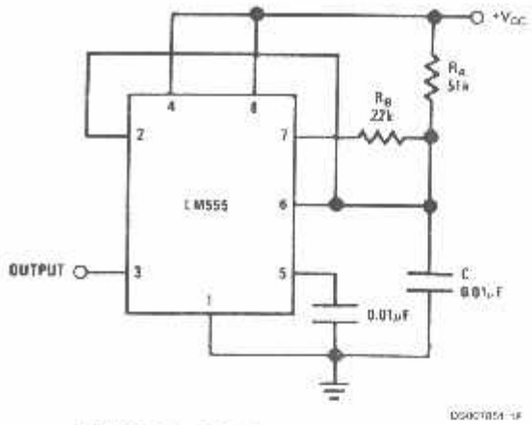


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

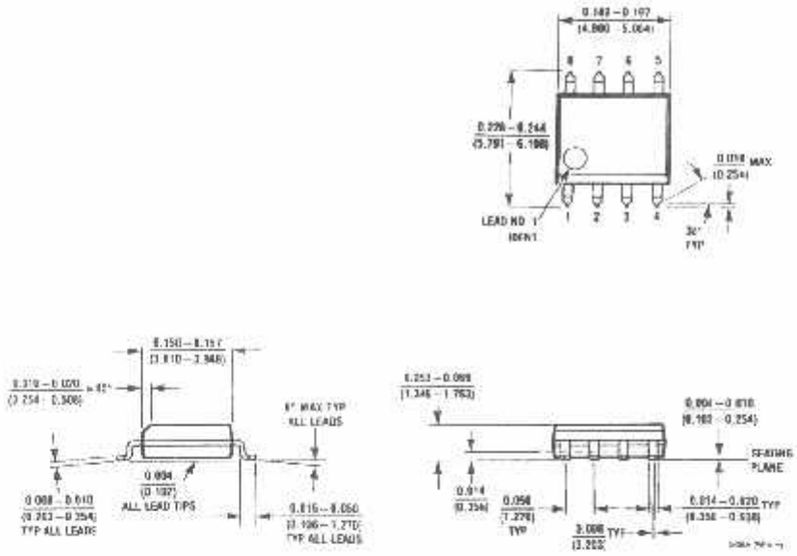
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

Lower comparator storage time can be as long as 10µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10µs minimum.

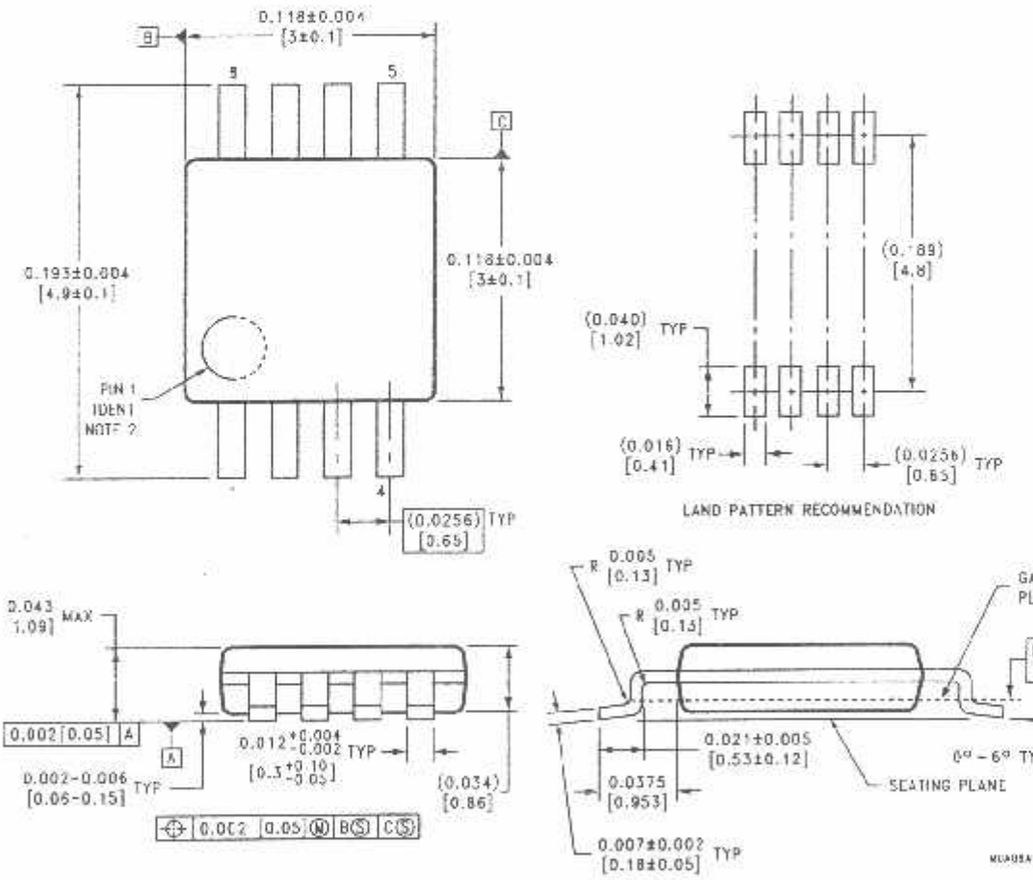
Delay time reset to output is 0.47µs typical. Minimum reset pulse width must be 0.3µs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

/sical Dimensions inches (millimeters) unless otherwise noted

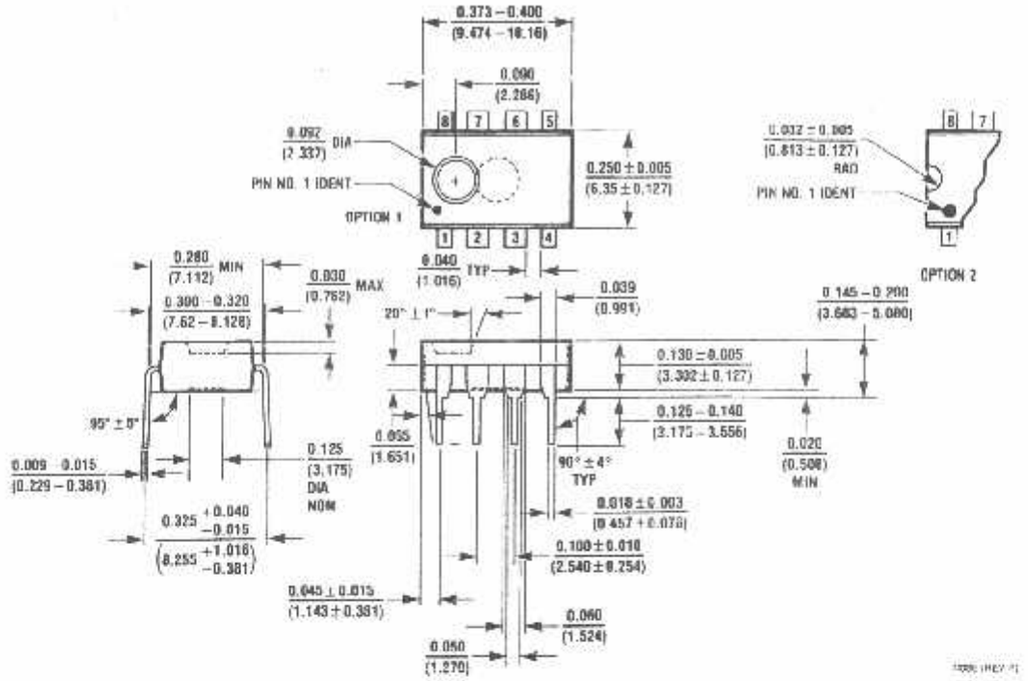


Small Outline Package (M)
NS Package Number M08A



8-Lead (0.118" Wide) Molded Mini Small Outline Package
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
NS Package Number N08E

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National Semiconductor

February 1995

LM3914 Dot/Bar Display Driver

General Description

The LM3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating the need for resistors. This feature is one that allows operation of the whole system from less than 3V.

The circuit contains its own adjustable reference and accurate 10-step voltage divider. The low-bias-current input buffer accepts signals down to ground, or V^-, yet needs no protection against inputs of 35V above or below ground. The buffer drives 10 individual comparators referenced to the precision divider. Indication non-linearity can thus be held typically to ½%, even over a wide temperature range.

Versatility was designed into the LM3914 so that controller, visual alarm, and expanded scale functions are easily added on to the display system. The circuit can drive LEDs of many colors, or low-current incandescent lamps. Many LM3914s can be "chained" to form displays of 20 to over 100 segments. Both ends of the voltage divider are externally available so that 2 drivers can be made into a zero-center meter.

The LM3914 is very easy to apply as an analog meter circuit. A 1.2V full-scale meter requires only 1 resistor and a single 3V to 15V supply in addition to the 10 display LEDs. If the 1 resistor is a pot, it becomes the LED brightness control. The simplified block diagram illustrates this extremely simple external circuitry.

When in the dot mode, there is a small amount of overlap or "fade" (about 1 mV) between segments. This assures that at no time will all LEDs be "OFF", and thus any ambiguous display is avoided. Various novel displays are possible.

Much of the display flexibility derives from the fact that all outputs are individual, DC regulated currents. Various effects can be achieved by modulating these currents. The individual outputs can drive a transistor as well as a LED at the same time, so controller functions including "staging" control can be performed. The LM3914 can also act as a programmer, or sequencer.

The LM3914 is rated for operation from 0°C to +70°C. The LM3914N is available in an 18-lead molded (N) package.

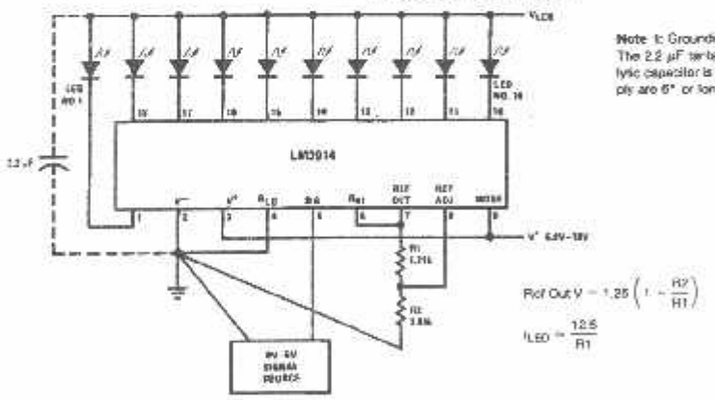
The following typical application illustrates adjusting of the reference to a desired value, and proper grounding for accurate operation, and avoiding oscillations.

Features

- Drives LEDs, LCDs or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 100 steps
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of less than 3V
- Inputs operate down to ground
- Output current programmable from 2 mA to 30 mA
- No multiplex switching or interaction between outputs
- Input withstands ±35V without damage or false outputs
- LED driver outputs are current regulated, open-collectors
- Outputs can interface with TTL or CMOS logic
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

Typical Applications

0V to 5V Bar Graph Meter



Note 1: Grounding method is typical of µP uses. The 2.2 µF tantalum or 10 uF aluminum electrolytic capacitor is needed if leads to the LED supply are 6" or longer.

$$\text{Ref Out V} = 1.25\left(1 + \frac{R2}{R1}\right)$$

$$I_{LED} = \frac{12.5}{R1}$$

TL/H/7970–1

  RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Dissipation (Note 5)	
Molded D.I.P. (N)	1365 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (Note 3)	±35V
Divider Voltage	−100 mV to V+
Reference Load Current	10 mA
Storage Temperature Range	−55°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Plastic Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1 and 3)

Parameter	Conditions (Note 1)		Min	Typ	Max	Units
COMPARATOR						
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} - V_{RH} \le 12V$, $I_{LED} = 1$ mA			3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} - V_{RH} \le 12V$, $I_{LED} = 1$ mA			3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)} = 2$ mA, $I_{LED} = 10$ mA		3	5		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le V^+ - 1.5V$			25	100	nA
Input Signal Overvoltage	No Change in Display		−35		35	V
VOLTAGE-DIVIDER						
Divider Resistance	Total, Pin 6 to 4		8	12	17	kΩ
Accuracy	(Note 2)			0.5	2	%
VOLTAGE REFERENCE						
Output Voltage	0.1 mA $\le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$		1.2	1.28	1.34	V
Line Regulation	$3V \le V^+ \le 18V$			0.01	0.03	%/V
Load Regulation	0.1 mA $\le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$			0.4	2	%
Output Voltage Change with Temperature	$0°C \le T_A \le +70°C$, $I_{L(REF)} = 1$ mA, $V^+ = 5V$			1		%
Adjust Pin Current				75	120	µA
OUTPUT DRIVERS						
LED Current	$V^+ - V_{LED} = 5V$, $I_{L(REF)} = 1$ mA		7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	$V_{LED} = 5V$	$I_{LED} = 2$ mA		0.12	0.4	mA
		$I_{LED} = 20$ mA		1.2	3	
LED Current Regulation	$2V \le V_{LED} \le 17V$	$I_{LED} = 2$ mA		0.1	0.25	mA
		$I_{LED} = 20$ mA		1	3	
Dropout Voltage	$I_{LED(ON)} = 20$ mA, $V_{LED} = 5V$, $\Delta I_{LED} = 2$ mA				1.5	V
Saturation Voltage	$I_{LED} = 2.0$ mA, $I_{L(REF)} = 0.4$ mA			0.15	0.4	V
Output Leakage, Each Collector	(Bar Mode) (Note 4)			0.1	10	µA

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 1)		Min	Typ	Max	Units
OUTPUT DRIVERS (Continued)						
Output Leakage	(Dot Mode) (Note 4)	Pins 10–18		0.1	10	μA
		Pin 1	60	150	450	μA
SUPPLY CURRENT						
Standby Supply Current (All Outputs Off)	$V^+ = 5V$, $I_{L(REF)} = 0.2$ mA			2.4	4.2	mA
	$V^+ = 20V$, $I_{L(REF)} = 1.0$ mA			6.1	9.2	mA

Note 1: Unless otherwise noted, all specifications apply with the following conditions:
$3\ V_{DC} \le V^+ \le 20\ V_{DC}$; V_{REF}, V_{ADJ}, $V_{RLO} \le (V^+ - 1.5V)$
$3\ V_{DC} \le V_{LED} \le V^+$; $0V \le V_{RLO} \le V^+ - 1.5V$
$-0.15V \le V_{RLO} \le 12\ V_{DC}$; $T_A = +25°C$, $I_{L(REF)} = 0.2$ mA, $V_{LED} = 3.0V$, pin 9 connected to pin 3 (Dot Mode)
$-0.15V \le V_{RHI} \le 12\ V_{DC}$

For higher power dissipations, pulse testing is used.

Note 2: Accuracy is measured referred to + 10.000 V_{DC} at pin 6, with 0.000 V_{DC} at pin 4. At lower full scale voltages, buffer and comparator offset voltage may add significant error.

Note 3: Pin 6 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 6 allows ± 100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+ or left open circuit. LED No. 10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

Note 5: The maximum junction temperature of the LM391< is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 55°C/W for the molded DIP (N package).

Definition of Terms

Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference adjust pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

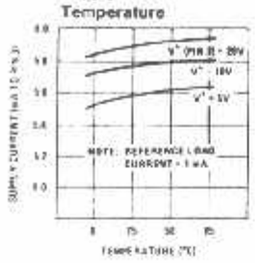
Line Regulation: The average change in reference output voltage over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage (V_{REF}) over the specified range of load current ($I_{L(REF)}$).

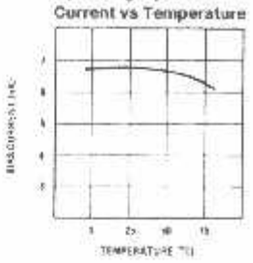
Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Typical Performance Characteristics

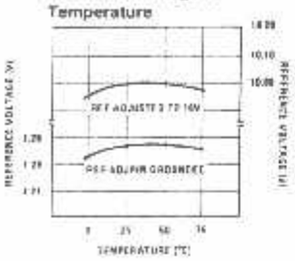
Supply Current vs Temperature



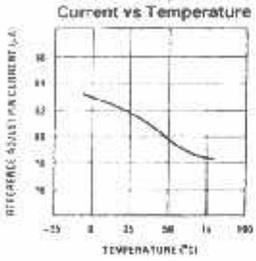
Operating Input Bias Current vs Temperature



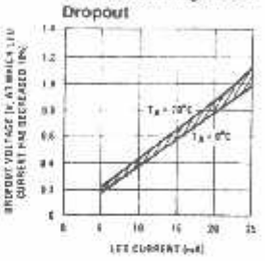
Reference Voltage vs Temperature



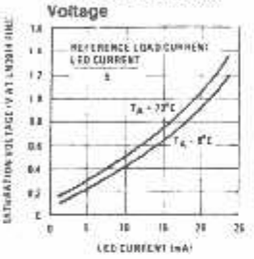
Reference Adjust Pin Current vs Temperature



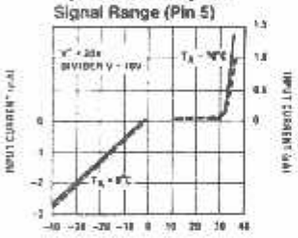
LED Current-Regulation Dropout



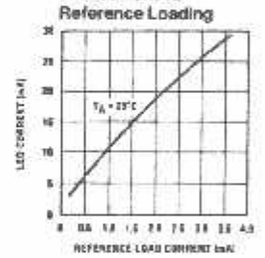
LED Driver Saturation Voltage



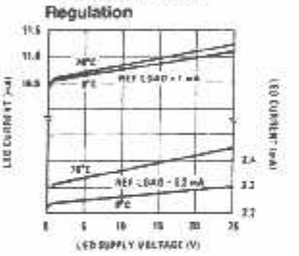
Input Current Beyond Signal Range (Pin 5)



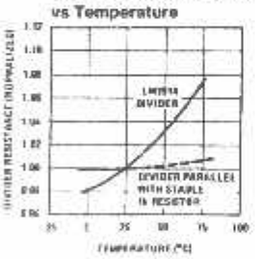
LED Current vs Reference Loading



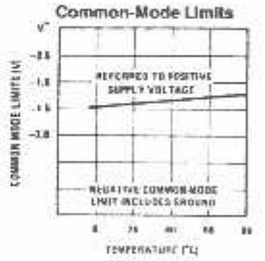
LED Driver Current Regulation



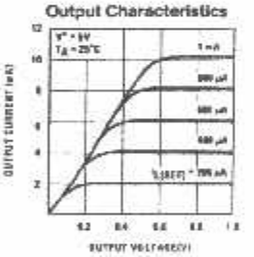
Total Divider Resistance vs Temperature



Common-Mode Limits

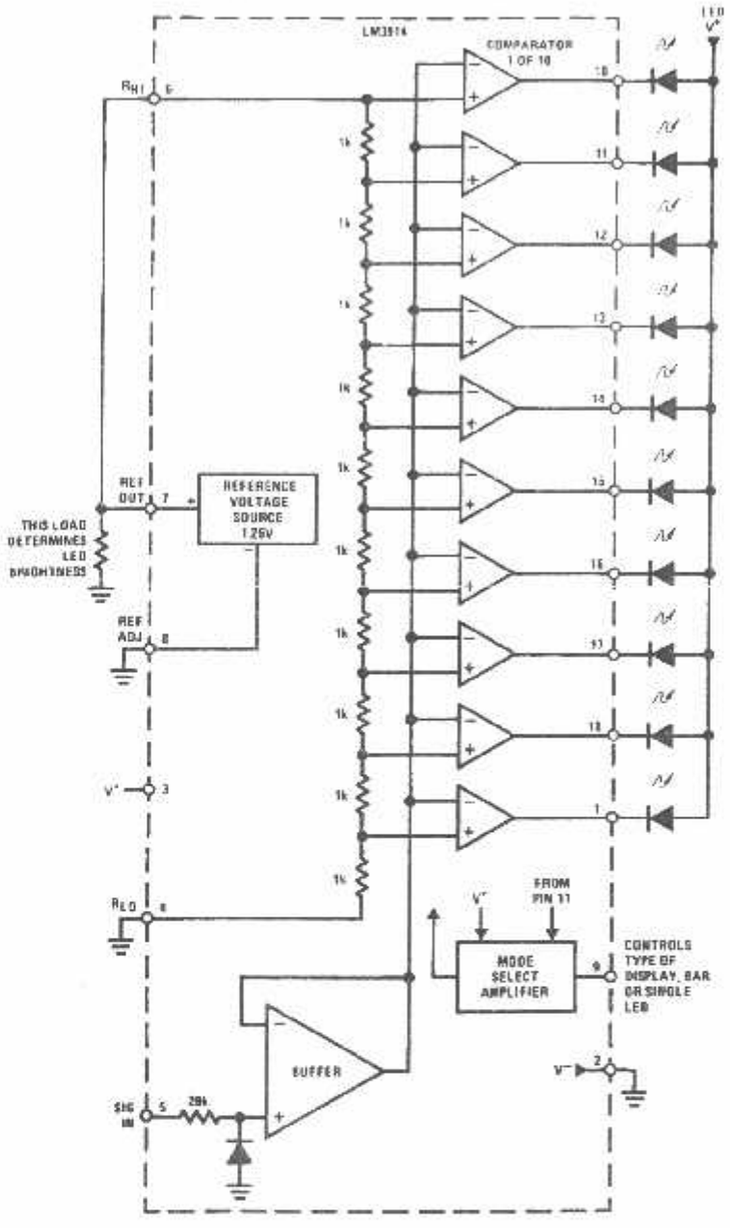


Output Characteristics



TL/H/7970-2

Block Diagram (Showing Simplest Application)



TL/H/7970-3

Functional Description

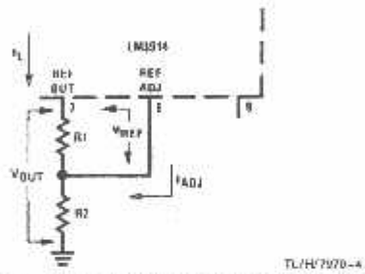
The simplified LM3914 block diagram is to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators, each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 125 mV that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are 1.5V below V^+ and no less than V^-. If an expanded scale meter display is desired, the total divider voltage can be as little as 200 mV. Expanded-scale meter displays are more accurate and the segments light uniformly only if bar mode is used. At 50 mV or more per step, dot mode is usable.

INTERNAL VOLTAGE REFERENCE

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$



TL/H/7970–4

Since the 120 µA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes.

CURRENT PROGRAMMING

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

MODE PIN USE

Pin 9, the Mode Select input controls chaining of multiple LM3914s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

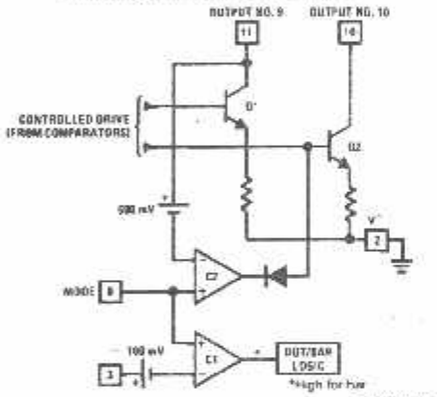
Dot Display, Single LM3914 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3914 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30, 40, or more LED displays. The last LM3914 driver in the chain will have pin 9 wired to pin 11. All previous drivers should have a 20k resistor in parallel with LED No. 9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function



TL/H/7970–5

Mode Pin Functional Description (Continued)

DOT OR BAR MODE SELECTION

The voltage at pin 9 is sensed by comparator C1, nominally referenced to ($V^+ - 100$ mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

DOT MODE CARRY

In order for the display to make sense when multiple LM3914s are cascaded in dot mode, special circuitry has been included to shut off LED No. 10 of the first device when LED No. 1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted below.

As long as the input signal voltage is below the threshold of the second LM3914, LED No. 11 is off. Pin 9 of LM3914 No. 1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED No. 11, pin 9 of LM3914 No. 1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED No. 10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 µA) that is diverted from LED No. 9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 µA flowing through LED No. 11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of LM3914 No. 1 is held low enough to force LED No. 10 off when *any* higher LED is illuminated. While 100 µA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED No. 11 with a 10k resistor. The 1V IR drop is more than the 900 mV worst case required to hold off LED No. 10 yet small enough that LED No. 11 does not conduct significantly.

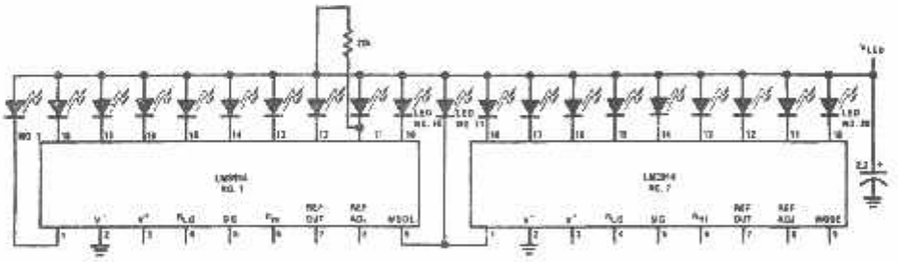
OTHER DEVICE CHARACTERISTICS

The LM3914 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA (2.5 mA max). However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3914 with a 1 mA reference pin load (1.3k), would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time between segments are all LEDs completely OFF in the dot mode. Generally 1 LED fades in while the other fades out over a mV or more of range (Note 2). The change may be much more rapid between LED No. 10 of one device and LED No. 1 of a *second* device "chained" to the first.

The LM3914 features individually current regulated LED driver transistors. Further internal circuitry detects when any driver transistor goes into saturation, and prevents other circuitry from drawing excess current. This results in the ability of the LM3914 to drive and regulate LEDs powered from a pulsating DC power source, i.e., largely unfiltered. (Due to possible oscillations at low voltages a nominal bypass capacitor consisting of a 2.2 µF solid tantalum connected from the pulsating LED supply to pin 2 of the LM3914 is recommended.) This ability to operate with low or fluctuating voltages also allows the display driver to interface with logic circuitry, opto-coupled solid-state relays, and low-current incandescent lamps.

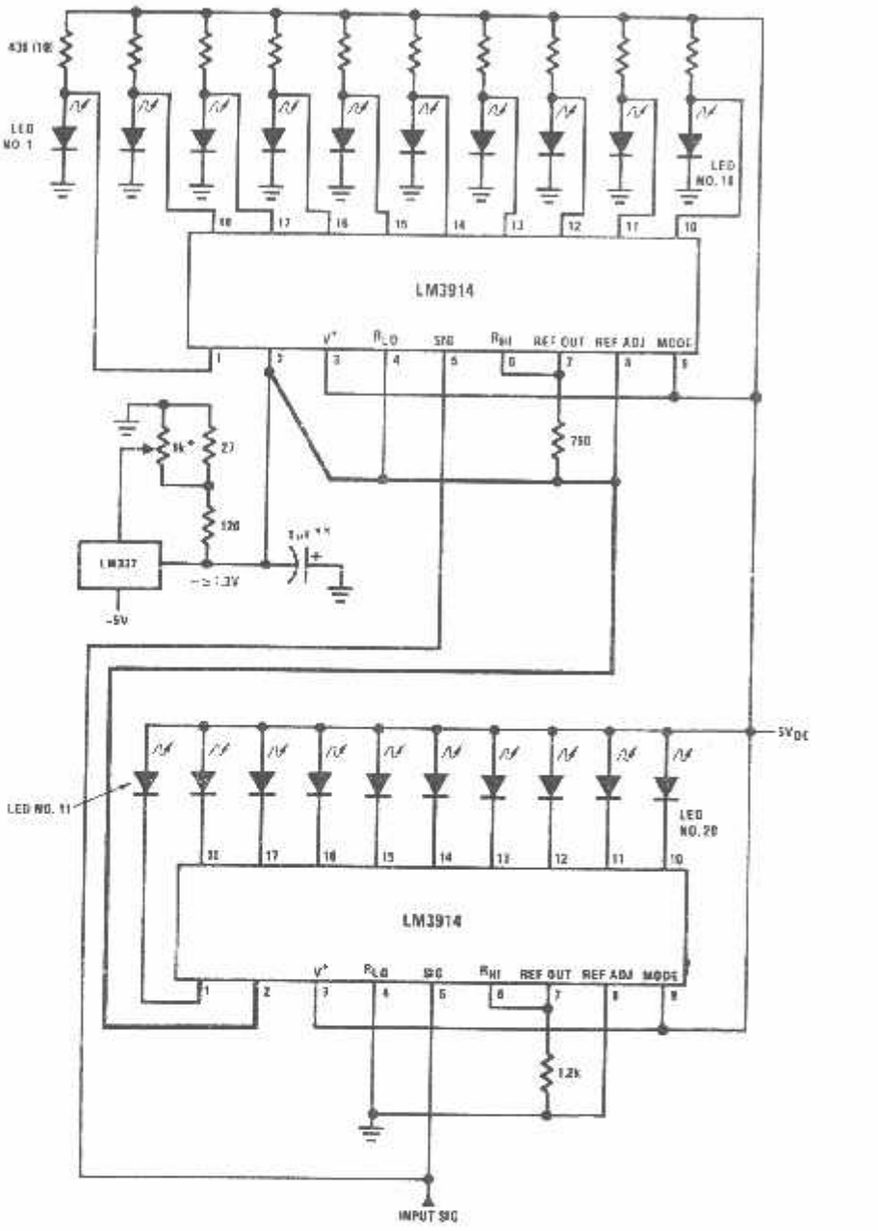
Cascading LM3914s in Dot Mode



TL/H/7870–5

Typical Applications (Continued)

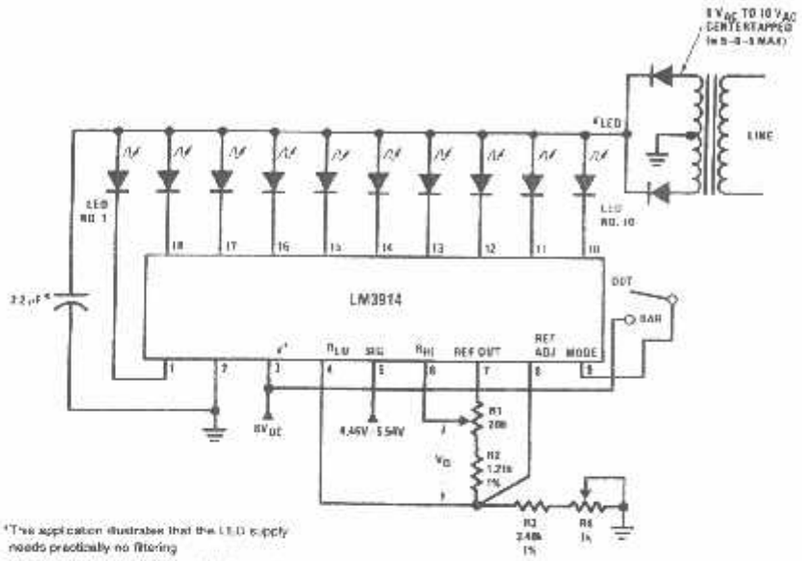
Zero-Center Meter, 20-Segment



TL/H/7370–7

Typical Applications (Continued)

Expanded Scale Meter, Dot or Bar



*This application illustrates that the LED supply needs practically no filtering

Calibration: With a precision meter between pins 4 and 6 adjust R1 for voltage V_D of 1.20V. Apply 4.64V to pin 5, and adjust R4 until LED No. 5 just lights. The adjustments are non-interacting.

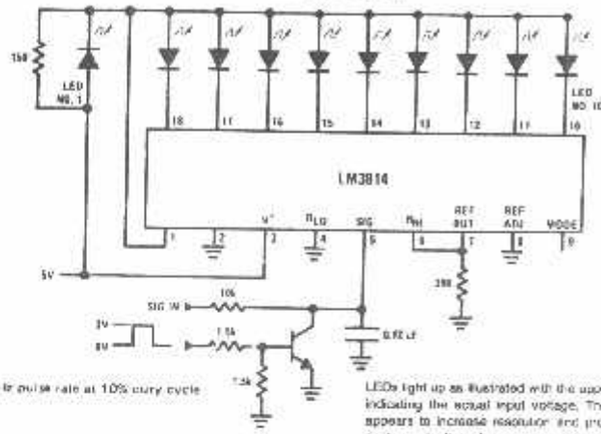
TL/H/7970–8

Application Example: Grading 5V Regulators

Highest No. LED on	Color	$V_{OUT(MIN)}$
10	Red	5.54
9	Red	5.42
8	Yellow	5.30
7	Green	5.18
6	Green	5.06
5V		
5	Green	4.94
4	Green	4.82
3	Yellow	4.7
2	Red	4.58
1	Red	4.46

Typical Applications (Continued)

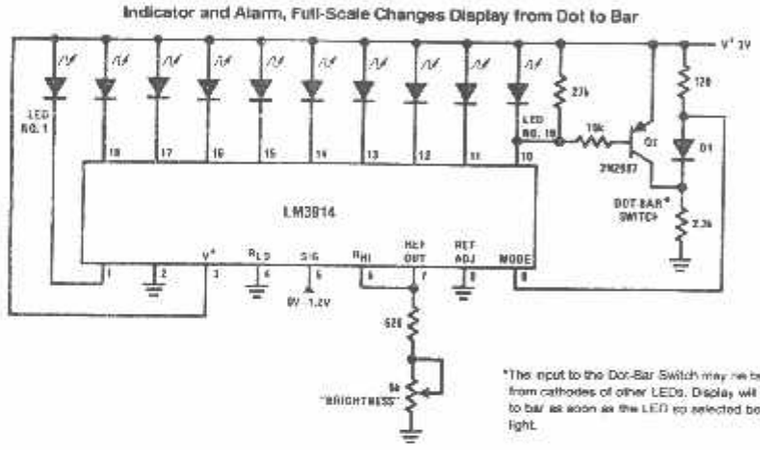
"Exclamation Point" Display



LEDs light up as illustrated with the upper LED indicating the actual input voltage. The display appears to increase resolution and provides an analog indication of overrange.

TL/H/7970–9

Indicator and Alarm, Full-Scale Changes Display from Dot to Bar

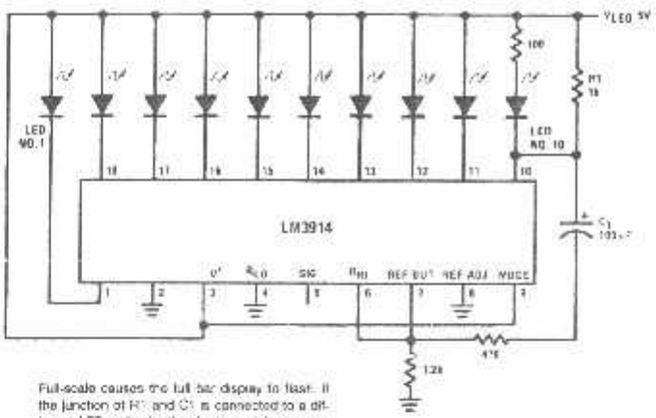


*The input to the Dot-Bar Switch may be taken from cathodes of other LEDs. Display will change to bar as soon as the LED so selected begins to light.

TL/H/7970–10

Typical Applications (Continued)

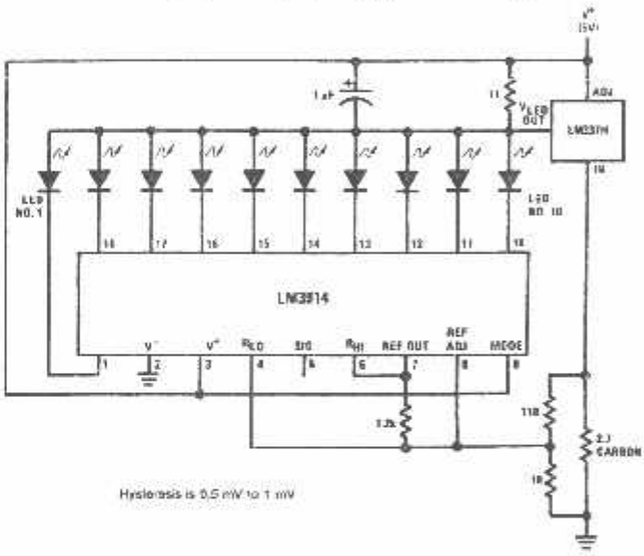
Bar Display with Alarm Flasher



Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

TL/H/7970–11

Adding Hysteresis (Single Supply, Bar Mode Only)

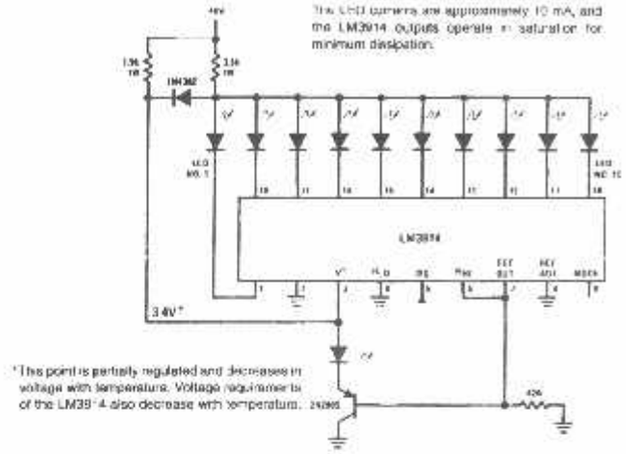


Hysteresis is 0.5 mV to 1 mV

TL/H/7970C–12

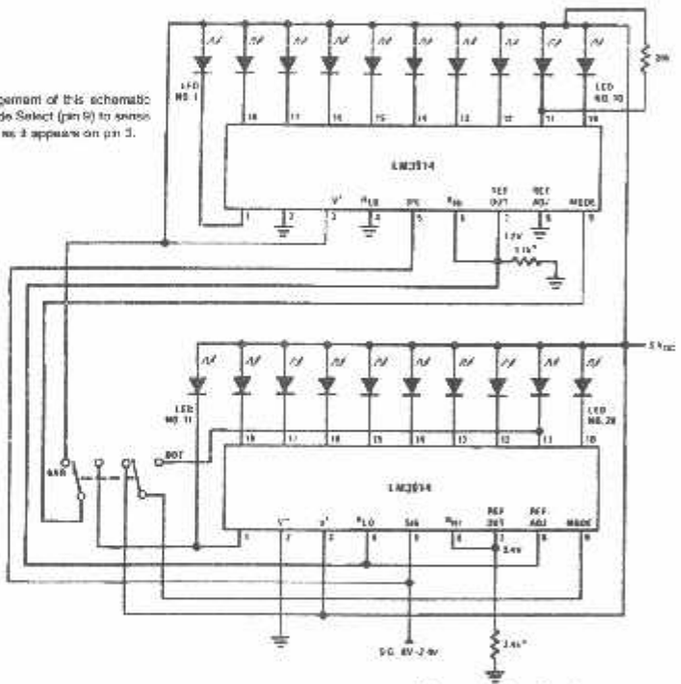
Typical Application (Continued)

Operating with a High Voltage Supply (Dot Mode Only)



*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3914 also decrease with temperature.

20-Segment Meter with Mode Switch



*The exact wiring arrangement of this schematic shows the need for Mode Select (pin 9) to sense the V+ voltage exactly as it appears on pin 3.

*Programs LEDs to 10 mA

Application Hints

Three of the most commonly needed precautions for using the LM3914 are shown in the first typical application drawing (see page 9-106) showing a 0V–5V bar graph meter. The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string (as illustrated) to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. Depending on the severity of the problem 0.05 μF to 2.2 μF decoupling capacitors from LED anode common to pin 2 will damp the circuit. If LED anode line wiring is inaccessible, often similar decoupling from pin 1 to pin 2 will be sufficient.

If LED turn ON seems slow (bar mode) or several LEDs light (dot mode), oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits (see Note 2, page 9-108). Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with at least a 0.001 μF capacitor, or up to 0.1 μF in noisy environments.

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 μF solid tantalum capacitor to pin 2 of the LM3914.

Turning OFF of most of the internal current sources is accomplished by pulling positive on the reference with a current source or resistance supplying 100 μA or so. Alternately, the input signal can be gated OFF with a transistor switch.

Other special features and applications characteristics will be illustrated in the following applications schematics. Notes have been added in many cases, attempting to cover any special procedures or unusual characteristics of these applications. A special section called "Application Tips for the LM3914 Adjustable Reference" has been included with these schematics.

APPLICATION TIPS FOR THE LM3914 ADJUSTABLE REFERENCE

GREATLY EXPANDED SCALE (BAR MODE ONLY)

Placing the LM3914 internal resistor divider in parallel with a section (≃230Ω) of a stable, low resistance divider greatly reduces voltage changes due to IC resistor value changes with temperature. Voltage V_1 should be trimmed to 1.1V first by use of R2. Then the voltage V_2 across the IC divider string can be adjusted to 200 mV, using R5 without affecting V_1. LED current will be approximately 10 mA.

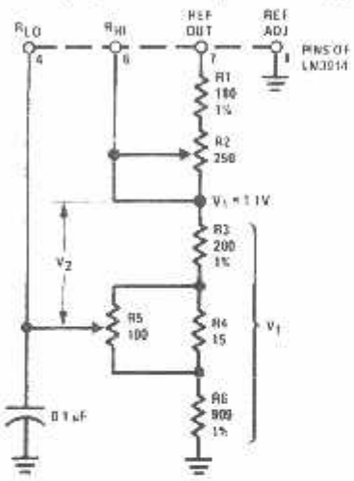
NON-INTERACTING ADJUSTMENTS FOR EXPANDED SCALE METER (4.5V to 5V, Bar *or* Dot Mode)

This arrangement allows independent adjustment of LED brightness regardless of meter span and zero adjustments.

First, V_1 is adjusted to 5V, using R2. Then the span (voltage across R4) can be adjusted to exactly 0.5V using R6 without affecting the previous adjustment.

R9 programs LED currents within a range of 2.2 mA to 20 mA after the above settings are made

Greatly Expanded Scale (Bar Mode Only)



TL/H/7870–15

ADJUSTING LINEARITY OF SEVERAL STACKED DIVIDERS

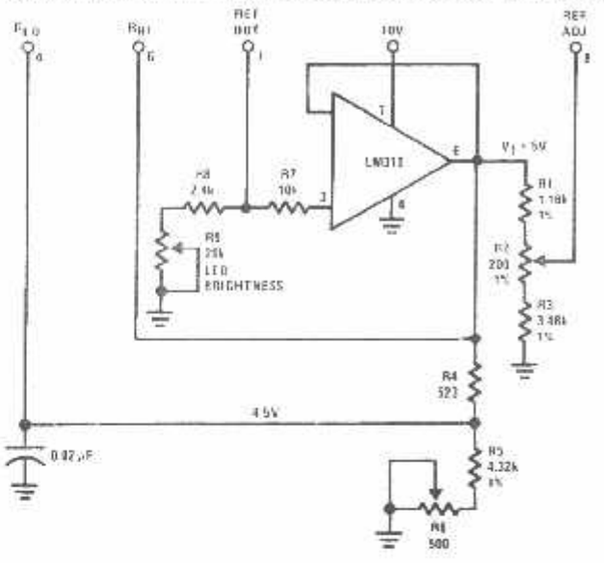
Three internal voltage dividers are shown connected in series to provide a 30-step display. If the resulting analog meter is to be accurate and linear the voltage on each divider must be adjusted, preferably without affecting any other adjustments. To do this, adjust R2 first, so that the voltage across R5 is exactly 1V. Then the voltages across R3 and R4 can be independently adjusted by shunting each with selected resistors of 6 kΩ or higher resistance. This is possible because the reference of LM3914 No. 3 is acting as a constant current source.

The references associated with LM3914s No. 1 and No. 2 should have their Ref Adj pins (pin 8) wired to ground, and their Ref Outputs loaded by a 620Ω resistor to ground. This makes available similar 20 mA current outputs to all the LEDs in the system.

If an independent LED brightness control is desired (as in the previous application), a unity gain buffer, such as the LM310, should be placed between pin 7 and R1, similar to the previous application.

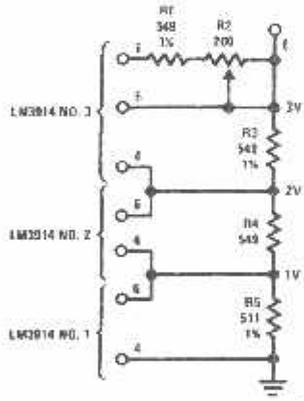
Application Hints (Continued)

Non-Interacting Adjustments for Expanded Scale Meter (4.5V to 5V, Bar or Dot Mode)



TL/H/7970–16

Adjusting Linearity of Several Stacked Dividers



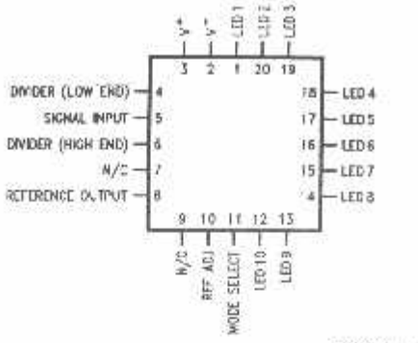
TL/H/7970–17

Other Applications

- "Slow"—fade bar or dot display (doubles resolution)
- 20-step meter with single pot brightness control
- 10-step (or multiples) programmer
- Multi-step or "staging" controller
- Combined controller and process deviation meter
- Direction and rate indicator (to add to DVMs)
- Exclamation point display for power saving
- Graduations can be added to dot displays. Dimly light every other LED using a resistor to ground
- Electronic "meter-relay"—display could be circle or semi-circle
- Moving "hole" display—indicator LED is dark, rest of bar lit
- Drives vacuum-fluorescent and LCDs using added passive parts

Connection Diagrams

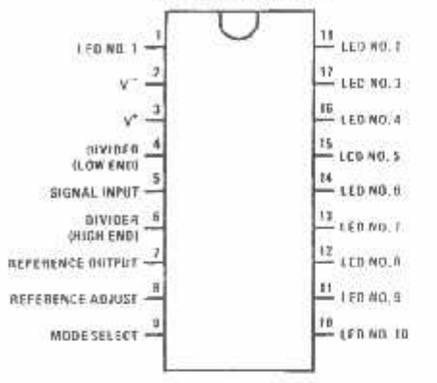
Plastic Chip Carrier Package



Top View

Order Number LM3914V
See NS Package Number V20A

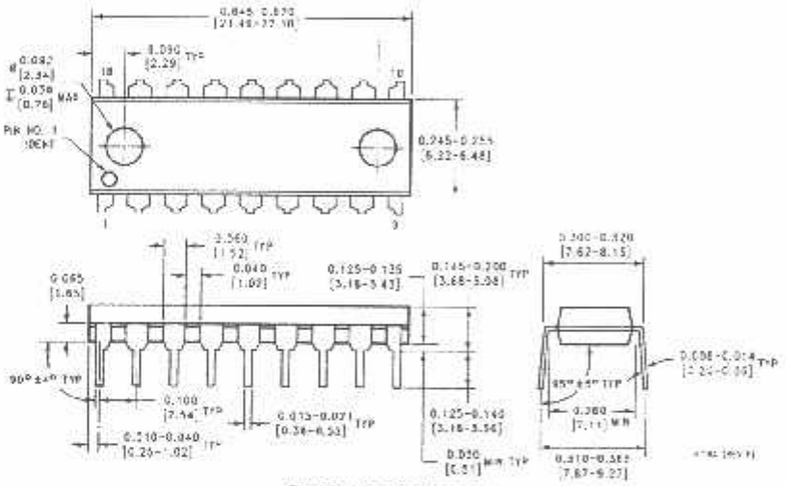
Dual-In-Line Package



Top View

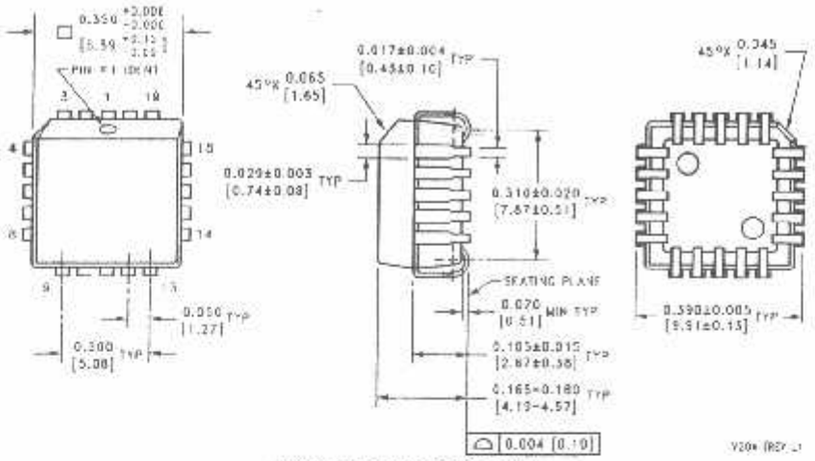
Order Number LM3914N
See NS Package Number N18A

Physical Dimensions inches (millimeters)



Dual-In-Line Package (N)
Order Number LM3914N
NS Package Number N18A

Physical Dimensions inches (millimeters) (Continued)



Plastic Chip Carrier Package (V)
Order Number LM3914V
NS Package Number V20A

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MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Gondo Nobianto

NIM : 00.17.122

Masa Bimbingan : 13 Agustus 2007 – 13 Febuari 2008

Judul skripsi : Perancangan Akuisisi Dan Pemrosesan Sinyal Elektrokardiografi (EKG) Portabel Dengan Menggunakan Rangkaian Matrik LED Sebagai Penampil

No	Tanggal	Uraian	Paraf Pembimbing
1.			
2.			
3.			
4.			
5.			
6.			
7.			
8.			
9.			
10.			

Malang.

Dosen Pembimbing I

Ir. Usman Juanda. MM
NIP.Y : 1039500247

INSTITUT TEKNOLOGI NASIONAL
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No	Tanggal	Uraian	Paraf Pembimbing
1.	10/4 '07	Bab I x II Revisi Penulisan	
2.	19/4 '07	Acc bab I x II	
3.	8/3 '08	Acc bab III, IV, V	
4.			
5.			
6.			
7.			
8.			
9.			
10.			

Malang, 08 - 03 - 2008

Dosen Pembimbing II

Satyohadi, MSc

NIP :

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MALANG

FORMULIR BIMBINGAN SKRIPSI

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2. Nim : 0017122
3. Jurusan : Teknik Elektro S-1
4. Konsentrasi : Teknik Elektronika
5. Judul Skripsi : Perancangan Akuisisi Dan Pemrosesan Sinyal Elektrokardiografi (EKG) Portabel Dengan Menggunakan Matrik LED Sebagai Penampil
6. Tanggal Pengajuan Skripsi : 13 Agustus 2007
7. Selesai Pengajuan Skripsi : 13 Febuari 2008
8. Dosen Pembimbing : Pembimbing I :Ir. Usman Juanda, MM
   Pembimbing II :Sotyohadi, ST.,Msc
9. Telah Dievaluasi Dengan Nilai : 79 (Tujuh Puluh Sembilan)

Diperiksa dan Disetujui

Dosen Pembimbing I	Dosen Pembimbing II
Ir. Usman Juanda, MM	Sotyohadi, ST.,Msc
NIP. 1018700143	NIP :

Mengetahui,
Ketua Jurusan Teknik Elektro S-1

Ir. F Yudi Limpraptono, MT
NIP. 103 9500 274

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Formulir Perbaikan Ujian Skripsi

alam pelaksanaan Ujian Skripsi Jenjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi
strik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

AMA : Gondo Nugroho
IM : 00.17.122
erbaikan meliputi :

Cara pakai :
① Di ambil dari hasil & pengujian
sebanyak kali.
② Berikan penjelasan kenapa
terjadi kegagalan.

Malang, 28-03-2008

(Ir. Choirul Saleh, MT)

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FAKULTAS TEKNOLOGI INDUSTRI
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KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Dari hasil ujian komprehensip jenjang strata Satu (S-1) Jurusan Teknik Elektro, Konsentrasi Elektronika yang diselenggarakan pada:

Hari : Selasa
Tanggal : 18 Maret 2008

Telah dilakukan perbaikan skripsi oleh :

Nama : Gondo Nobianto
N.I.M : 00.17.122
Masa Bimbingan : 13 Agustus 2007 – 13 Febuari 2008
Judul : Perancangan Akuisisi Dan Pemrosesan Sinyal Elektrokardiografi (EKG) Portabel Dengan Menggunakan Matrik LED Sebagai Penampil

Perbaikan Meliputi :

No	Tanggal	Materi Perbaikan	Paraf Dosen Penguji
1.	18 Maret 2008	Kesimpulan: 1. Diambil dari pengujian per-blok tiap rangkaian. 2. Penjelasan mengapa terjadi kegagalan.	

Disetujui Oleh:

(Ir. Abdul Hamid, MT)
Penguji Pertama

(I. Komang Somawirata, ST. MT)
Penguji Kedua

Mengetahui

Dosen Pembimbing I

Ir. Usman Juanda, MM
NIP.Y :1018700143

Dosen Pembimbing II

Sotyohadi, ST
NIP :