SKRIPSI

PERANCANGAN DAN PEMBUATAN ALAT PENG-AKUISISI DAN PEMROSESAN SINYAL ELEKTROKARDIOGRAFI (EKG) DENGAN *PERSONAL COMPUTER* (PC) SEBAGAI PENAMPIL

Disusun Oleh:

Alex Walesa Butarbutar
0017135

JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG

MARET 2008

LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN ALAT PENG-AKUISISI DAN PEMROSESAN SINYAL *ELEKTROKARDIOGRAFI* (ECG) DENGAN *PERSONAL COMPUTER* (PC) SEBAGAI PENAMPIL

SKRIPSI

Disusun dan diajukan sebagai salah satu syarat untuk memperoleh gelar Sarjana Teknik Elektronika Strata Satu (S-I)

Disusun Oleh :
ALEX WALESA BUTARBUTAR
00.17.135

Diperiksa dan disetujui,

Dosen Pembimbing I	Dosen Pembimbing II
Ir. F. Yudi Limpraptono, MT	Sotyohadi, ST
NIP. P. 1039500274	NIP.Y. 1039700309

Mengetahui,
Ketua Jurusan Teknik Elektro S-1

Ir. F. Yudi Limpraptono, MT
NIP. P. 1039500274

JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
2008

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura-gura No. 2
MALANG

BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

Nama	: Alex Walesa Butarbutar
Nim	: 00.17.135
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Judul Skripsi	: Perancangan dan Pembuatan Alat Peng-Akuisisi Dan Pemrosesan Sinyal Elektrokardiografi (EKG) Dengan *Personal Computer* (PC) Sebagai Penampil.

Dipertahankan Dihadapan Majelis Penguji Skripsi Jenjang Strata Satu (S-1) Pada:

Hari : Senin
Tanggal : 17 Maret 2008
Dengan Nilai : 73,1 (B+)

Panitia Ujian Skripsi

Ir. Mochtar Asroni, MSME	Ir. F Yudi Limpraptono, MT
Ketua	Sekretaris

Anggota Penguji

(DR. Cahyo Crisdian, Msc.)	(Ir. Yoseph Dedy Irawan, MT.)
Penguji I	Penguji II

ABSTRAKSI

(Alex Walesa Butarbutar, 00.17.135, Jurusan Teknik Elektronika S-1)

(Dosen Pembimbing: Ir. F. Yudi Limpraptono,MT.,Sotyohadi, ST.)

Kata kunci : Sinyal, ECG, Filter, Amplifier, ADC, DB-25.

Skripsi ini bertujuan untuk merancang alat untuk meng-akuisisi dan memproses sinyal ECG dan ditampilkan di Personal Computer (PC). Alat ini terdiri dari instrumentasi amplifer dan filter-filter sebagai pemroses sinyal jantung. Prinsip kerjanya dengan mengukur selisih tegangan antara dua sisi tubuh yang yang dikirim oleh jantung manusia dan kemudian memprosesnya untuk bisa ditampilkan ke Personal Computer (PC). Sinyal Elektrokardiogram (ECG) diukur oleh sebuah ECG amplifier, yaitu sebuah amplifier bioelectric yang biasanya memiliki penguatan 1000 kali. Sebuah ECG amplifier terdiri dari sebuah instrumentation amplifier (IA) diikuti bandpass filter (BPF), dan amplifier driver kaki kanan (RL). Perancangan dan implementasi dari single-channel ECG circuit dengan bandwidth of 0.16-100Hz untuk keperluan monitoring pasien. Dengan menggunakan ADC 0804 8bit, sinyal yang dihasilkan akan dikonversikan ke besaran analog dan melalui port DB-25 dikirimkan untuk ditampilkan di PC dengan mengunakan Software hasil perancangan. Softwarc yang digunakan adalah Visual Basic, dengan bahasa pemrograman menggunakan bahasa Pascal.

KATA PENGANTAR

Dengan memanjatkan puji syukur kehadirat Allah, yang telah memberikan rahmat, hidayah serta segala karunia-Nya, akhirnya penyusun dapat menyelesaikan skripsi ini yang berjudul **"Perancangan dan Pembuatan Alat Peng—akuisisi dan Pemrosesan Sinyal Elektrokardiografi (ECG) Dengan Personal Computer (PC)** Laporan skripsi ini merupakan salah satu persyaratan kelulusan Strata 1 Jurusan Teknik Elektro Program Studi Elektronika, Institut Teknologi Nasional Malang.

Keberhasilan penyusunan laporan skripsi ini tidak lepas dari dukungan dan bantuan berbagai pihak. Untuk itu penyusun menyampaikan terima kasih kepada :

1. Bapak Prof. DR. Ir. Abraham Lomi, MSEE selaku Rektor Institut Teknologi Nasional Malang.
2. Bapak Ir. Mochtar Asroni, MSME, selaku Dekan Institut Teknoligi Nasional Malang.
3. Bapak Ir. Yudi Limpraptono, MT, selaku Ketua Jurusan Teknik Elektro S-1 dan Dosen Pembimbing I.
4. Bapak Sotyohadi, ST. selaku Dosen Pembimbing II
5. Kedua orangtua atas dukungan moril dan spiritual serta do'a restunya dan juga materinya.
6. Teman-teman yang telah membantu terselesainya skripsi ini.

Dengan segala itikad, kemampuan dan saran yang ada, laporan skripsi ini dapat terselesaikan dengan sebaik-baiknya. Namun karena keterbatasan waktu dan

DAFTAR ISI

Halaman

DAFTAR GAMBAR

DAFTAR TABEL

DAFTAR GRAFIK

BAB I

PENDAHULUAN

1.1. Latar Belakang

Perkembangan teknologi sangatlah pesat di berbagai bidang, baik itu di bidang industri, penelitian, kedokteran & kesehatan, militer hingga keperluan rumah tangga. Namun dengan adanya teknologi terbaru, harganya sangatlah mahal. Sedangkan kita tahu bahwa teknologi dibuat diciptakan untuk membantu pekerjaan manusia atau untuk menjadikan suatu pekerjaan lebih mudah dan efisien sekaligus bernilai ekonomis.

Tidak dapat dipungkiri bahwa saat ini masyarakat sangat berhati-hati terhadap kondisi kesehatan mereka. Baik itu masyarakat di perkotaan maupun yang berada di pedesaan. Kalau di perkotaan sudah terdapat fasilitas kesehatan yang memiliki peralatan lengkap untuk memeriksa kondisi dari pasien, sedangkan di pedesaan hanya terdapat puskesmas dengan fasilitas penunjang yang terkadang tidak lengkap.

Berangkat dari permasalahan diatas, maka timbul gagasan untuk membuat suatu perangkat yang dapat mengetahui sinyal jantung pada tubuh sesara digital dengan sebuah penampil, yang bernilai ekonomis, sehingga kondisi jantung dari pasien tersebut dapat dipantau. Sehingga dapat dideteksi sejak dini kelainan jantung apa yang diderita oleh si pasien, yang pada umumnya turut serta menekan angka kematian masyarakat akibat gangguan jantung.

1.2. Tujuan.

Tujuan dari penulisan sripsi ini adalah merancang dan membuat perangkat yang dapat mengakuisisi dan memproses sinyal elektrokardiografi dua kanal (*channel*) dengan menggunakan PC (*Personal Computer*) sebagai penampil sinyal EKG tersebut. Sehingga kita dapat memonitor sinyal jantung dari si pasien.

1.3. Rumusan Masalah.

Dalam perancangan dan pembuatan alat untuk mengakuisisi dan memproses sinyal elektrokardiografi ini dapat dirumuskan beberapa masalah yang akan dibahas antara lain :

1. Bagaimana cara merancang dan membuat perangkat yang dapat membedakan sinyal yang dihasilkan oleh jantung dengan sinyal lainnya yang dihasilkan oleh tubuh manusia.
2. Bagaimana cara mengubah besaran dari sinyal jantung manusia menjadi besaran digital.
3. Bagaimana cara menampilkan sinyal jantung tersebut pada *Personal Computer* (PC).

1.4. Batasan Masalah.

Sehubungan dengan permasalahan yang dibahas dalam skripsi ini, maka penulis akan membatasi permasalahan tersebut dengan tujuan untuk mencegah kemungkinan terjadinya perluasan dan penyimpangan pembahasan dari fokus permasalahan, mengingat akan keterbatasan waktu dan biaya.

Berikut ini penulis uraikan batasan masalahnya :

Berikut ini penulis uraikan batasan masalahnya :

- Sinyal yang ditampilkan adalah sinyal EKG dari jantung pasien saat diadakan pengukuran.
- Alat ini tidak menentukan adanya suatu penyakit yang mungkin diderita oleh si pasien.
- Tidak membahas cara kerja jantung.
- Tidak membahas tentang kesehatan dari si pasien.
- Tidak membahas catu daya

1.5. Metodologi Penelitian.

Pembuatan skripsi ini dilakukan dengan pendekatan pada studi lapangan dan perangkat keras untuk mendapatkan hasil yang diinginkan.

Metodologi penelitian yang dipakai dalam pembuatan skripsi ini adalah :

1. Studi literatur yang mempelajari teori-teori yang berkaitan mengenai cara kerja komponen-komponen yang digunakan dalam Akuisisi Dan Pemrosesan Sinyal EKG (Elektrokardiogram) Yang Ditampilkan Pada *Personal Computer* (PC).
2. Perancangan alat dilakukan dengan mengacu pada beberapa literatur yang menyertakan skematik rangkaian EKG. Dan juga dilakukan dengan mempelajari semua perangkat yang diperlukan dalam sistem beserta pengaplikasiannya selanjutnya menurut kebutuhan.

3. Selanjutnya pada pembuatan alat, dibuatlah sebuah alat yang dapat mengakuisisi dan memproses sinyal elektrokardiogram sehingga dapat ditampilkan pada *Personal Computer* (PC).
4. Kemudian dilakukan pengujian terhadap alat yang dirancang. Pengujian ini dilakukan dengan mengkalibrasi alat tersebut dengan alat yang sudah ada pada sebuah rumah sakit. Sehingga didapat suatu alat yang kita inginkan (praktis dan ekonomis).
5. Dari tahap-tahap yang sudah dilakukan di atas, dapat sebuah kesimpulan akhirnya disusun laporan skripsi ini dimana di dalamnya mencakup semua langkah dalam pembuatan alat tersebut.

1.6. Sistematika Penulisan.

Sistem penulisan yang akan digunakan untuk membahas masalah dalam Tugas Akhir ini diperlukan gambaran susunan alat secara keseluruhan yang selanjutnya ditentukan komponen-komponen utama dan pendukung yang digunakan dan kemungkinan untuk disederhanakan baik untuk bentuk, biaya pembuatanya agar didapatkan susunan yang seefisien dan seefektif mungkin.

Sistematika penulisan Laporan Akhir ini adalah :

BAB I **Pendahuluan,** yang memuat latar belakang, Rumusan Masalah, Tujuan, Batasan Masalah, Metodologi serta Sistematika Penulisan.

BAB II **Teori Dasar,** berisi tentang teori penunjang yang berhubungan dengan semua perangkat lunak dan perangkat keras dalam sistem.

BAB III **Perancangan dan Pembuatan Alat,** membahas tentang perencanaan dan pembuatan alat.

BAB IV **Analisa dan Pengujian Alat,** berisikan tentang pengujian alat yang telah dibuat, pengoperasian dan spesifikasi alat.

BAB V **Penutup,** yang berisi kesimpulan dan Saran.

BAB II

TEORI DASAR

2.1. Biopotensial

Biopotensial adalah sinyal-sinyal berupa potensial ionik yang dihasilkan oleh aktivitas biokimia dari sel-sel tertentu dalam tubuh mahluk hidup. Sinyal-sinyal ini dihasilkan ketika tubuh melakukan aktivitas. Dengan menggunakan transducer yang sesuai, tegangan ionik ini dapat dikonversikan menjadi tegangan listrik, sehingga dapat dianalisa lebih lanjut dengan peralatan kedokteran.

Ada beberapa biopotensial yang dihasilkan oleh tubuh manusia bergantung dari organ tubuh yang menghasilkannya, antara lain:

- ECG (*Electrocardiography*) atau sinyal yang dihasilkan karena adanya aktivitas jantung.
- EEG (*Electroencephalography*) atau sinyal yang dihasilkan karena adanya aktivitas otak.
- EMG (*Electromyography*) atau sinyal yang dihasilkan karena adanya aktivitas otot.
- Dll.

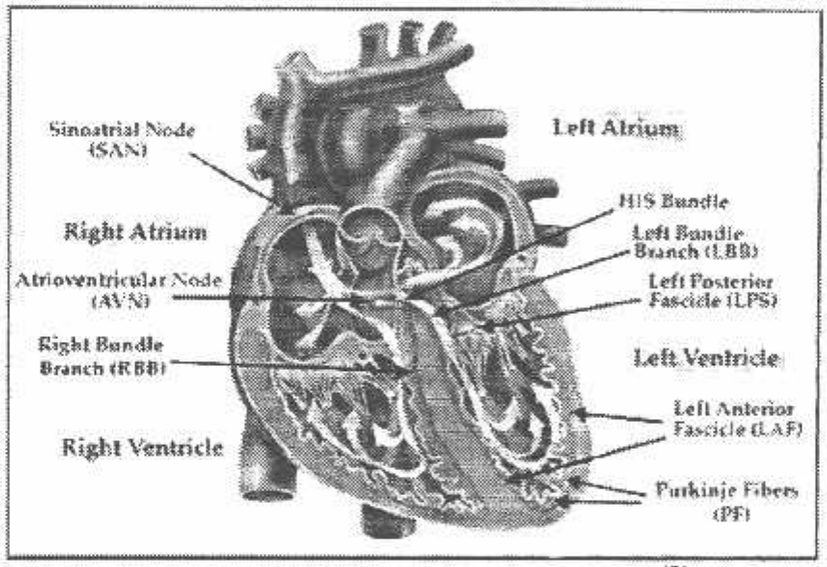
Signal	Frequency range (Hz)	Amplitude Range (mV)
ECG	0,1–300	0,05–3
EEG	0,1–100	0,001–1
EOG	0,1–10	0,001–0,3
EMG	50–3000	0,001–100

Tabel 2.1. Frekuensi Biopotensial[1]

Pada kesempatan ini yang akan dibahas hanyalah sinyal ECG (*Electrocardiography*) atau sinyal yang dihasilkan karena adanya aktivitas pada jantung.

2.2. Biopotensial pada jantung

Jantung manusia terdiri dari 4 bagian utama, yaitu: 2 serambi/*ventricle* (serambi kanan dan serambi kiri), dan 2 bilik/*atrium* (bilik kanan dan bilik kiri), dan beberapa bagian lainnya seperti yang tampak pada **gambar 2.1.** di bawah ini.



Gambar 2.1. Penampang Jantung Manusia[2]

2.2.1. Sinoatrial (SA) Node

Sinoatrial Node yang normal akan menentukan bagaimana jantung berdetak, karena Sinoatrial Node berdetak dengan cepat dan memberikan rangsangan pada jaringan yang lain sebelum mencapai keadaan istirahat sehingga dapat dikatakan bahwa Sinoatrial node adalah sebagai pemicu detak jantung.

Sinoatrial Node berdenyut dengan kecepatan dari 70 sampai 80 denyutan per-menit (*beat per-minute:* bpm) pada saat kondisi jantung tenang atau istirahat[3].

2.2.2. Atrioventricular (AV) Node.

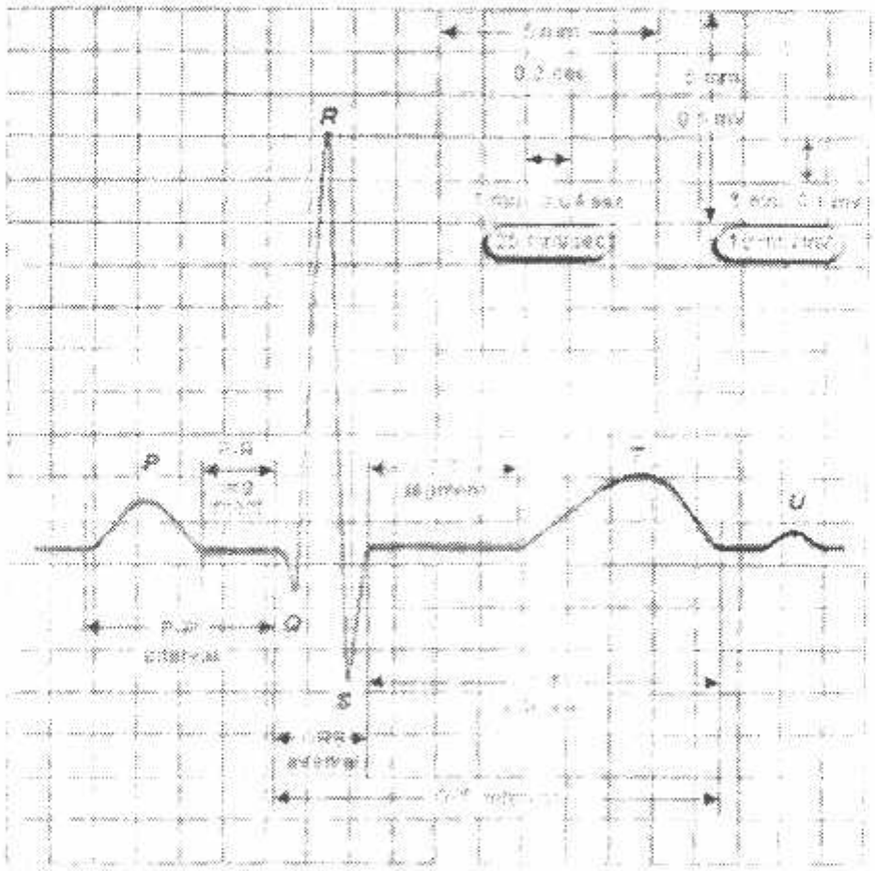
Antrioventricular (AV) Node berdenyut dengan kecepatan 40 s/d 60 denyutan per menit (*beat per-minute: bpm*). Depolarisation Sinoatrial Node menyebar ke seluruh serambi jantung/*atrium* dan menjangkau Atrioventricular dalam 40ms. Oleh karena rendahnya kecepatan sifat konduksi dari Atrioventricular Node, memerlukan sekitar 110ms untuk depolarisasi untuk menjangkau *Bundle of HIS*, yang dikenal sebagai sistem Purkinje. Bilik jantung/*ventricle* kemudian berkontraksi, *ventricle* kanan menekan darah masuk ke paru-paru, *ventricle* kiri yang menekan darah ke dalam aorta dan sesudah itu melewati sistem peredaran darah. Kontraksi jantung ini disebut *Systole*.

Kontraksi pada bilik jantung/*ventricle* ini memerlukan 200 s/d 250ms. Waktu yang relatif lama ini menyempatkan Atrioventricular untuk mengosongkan jantung dari darah dan mengirimkan darah ke Pembuluh Arteri. Jantung mengalami repolarisasi selama waktu istirahat jantung ini, hal ini disebut *diastole*[3].

2.3. ECG (*Electrocardiography)*

Suatu *electrocardiography* (ECG atau EKG) adalah sebuah grafik yang menggambarkan aktivitas listrik jantung dari waktu ke waktu. ECG atau EKG ini memegang peranan penting dalam menganalisa jantung dan menjadi kunci dalam

diagnosa dari suatu penyakit yang mungkin diderita oleh si pasien, dimana aktifitas listrik jantung ini didapat dengan suatu pengukuran potensial listrik menggunakan sebuah *transducer* (berupa elektrode) yang ditempelkan pada permukaan tubuh di titik-titik tertentu. Arus yang mengalir, dalam bentuk ion, merupakan signal listrik dari serabut otot jantung yang mengarah ke jantung pada saat jantung memompa darah. Karakteristik sinyal ECG dilambangkan oleh enam puncak dan lembah ditandai dengan huruf yang berurutan yaitu P, Q, R, S, T, dan U. Seperti tampak pada gambar **2.2** di bawah ini.



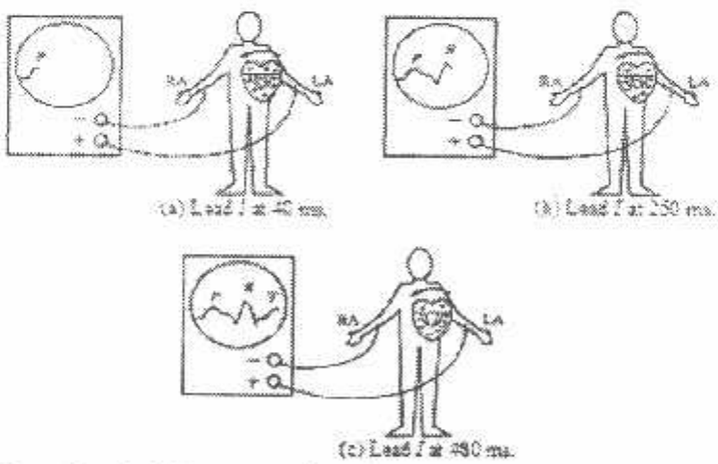
Gambar 2.2. Bentuk Sinyal ECG/EKG Normal

Interval :
P-R *Beginning of P-Wave to beginning of QRS complex.*
S-T *End of S-Wave to end of T-Wave.*
Q-T *Beginning of Q-Wave to end of T-Wave*

Segment :
P-R *End of P-Wave to beginning of Q-Wave.*
S-T *End of S-Wave to beginning of T-Wave.*

Complex :
QRS *Beginning of Q-Wave to end of S-Wave.*

Saat diastole, ketika jantung dalam kondisi istirahat, seluruh sel terpolarisasi sehingga menyebabkan potensial di dalam masing-masing sel bersifat negatif jika dibandingkan dengan yang di luar sel. Keadaan tidak seimbang ini mengakibatkan arus ion, **I**, pada lengan kiri (LA) akan terukur positif dibandingkan dengan lengan tangan kanan (RA), seperti yang tampak pada **gambar 2.3. (a)** Menghasilkan Gelombang-P.



Gambar 2.3. Ion arus sebagai sumber Elektrokardiogram

Setelah sekitar 90 ms kemudian, atrium dengan sepenuhnya terpolarisasi, dan arus ion yang terukur oleh Lead *I* berkurang hingga bernilai nol. Depolarisasi

kemudian melewati simpul *atrioventricular*, menyebabkan penundaan sekitar 110 ms. Depolarisasi kemudian melewati otot ventricular kanan, men-depolarisasi-kannya dan menyebabkan otot ventricular kanan ini bernilai negatif jika dibandingkan dengan otot ventricular kiri yang masih ter-polarisasi, seperti yang tampak pada **gambar 2.3. (b)**. Arah arus menyebabkan tegangan bernilai positif-ke-negatif dari (lengan kiri) LA ke (lengan kanan) RA yang disebut gelombang-R.

Sinyal ECG mungkin akan terganggu oleh berbagai macam noise. Noise-noise ini bersumber dari:

- Adanya Interferensi dari PLN: 50-60 Hz.
- Noise dari electrode: variabel antara electrode dan kulit.
- Kontraksi otot: masuknya sinyal Electromyogram (EMG) dan menyatu dengan sinyal ECG tersebut.

2.4. Transducer.

Diperlukan sebuah transducer untuk menghubungkan tubuh dengan alat pengukur pada saat melakukan pengukuran tegangan dan arus yang dihasilkan oleh tubuh. Transducer adalah sebuah alat yang bila digerakkan oleh energi di dalam sebuah sistem transmisi, menyalurkan energi tersebut kedalam bentuk yang sama atau dalam bentuk yang lain ke sistem transmisi yang lain. Transmisi energi ini bisa berupa energi listrik, mekanik, kimia, optik/radiasi, atau termal/panas.

Berdasarkan dengan jenisnya transducer dapat dikelompokkan menjadi dua macam antara lain:

1. Transducer Pasif[4].

Transducer ini ini tidak dapat menghasilkan tegangan sendiri tetapi dapat menghasilkan perubahan nilai resistansi, kapasitansi, atau induktansi apabila mengalami perubahan kondisi sekeliling.

Jika transduser ini mengalami perubahan kondisi pada lingkungan sekelilingnya maka nilai resistansinya akan berubah. Perubahan ini selanjutnya menyebabkan perubahan besar tegangan atau kuat arus yang dihasilkan trnsducer. Perubahan ini dapat bernilai positif (nilai resistansi bertambah) berarti tegangannya juga meningkat atau negatif (nilai resistansi berkurang) berarti tegangannya berkurang. Perubahan tegangan inilah yang dimanfaatkan untuk mengetahui keadaan yang ingin diukur.

2. Transducer Aktif.

Transducer ini tidak memerlukan catu daya eksternal. Transducer ini malah dapat menghasilkan energi listrik.

2.4.1. Elektrode Untuk Mendapatkan Sinyal Biopotensial.

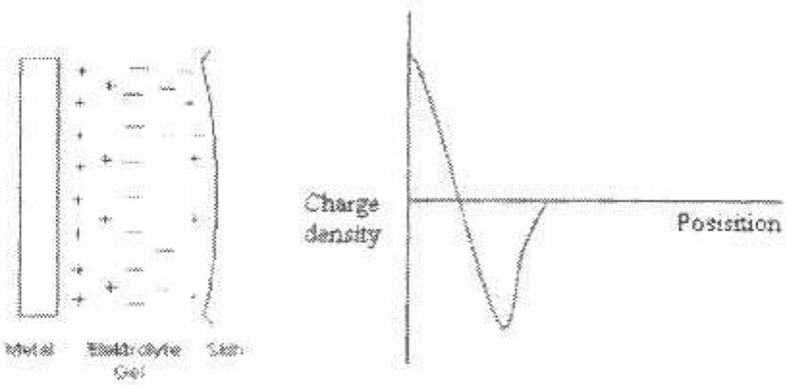
Elektrode merupakan salah satu jenis transducer yang digunakan untuk mengukur biopotensial pada tubuh (ECG, EEG, EOG, EMG, dll).

Pada umumnya dikenal dengan elektrode Ag/AgCl. Electrode mengkonversi arus ion yang diproduksi oleh tubuh ke dalam bentuk tegangan, dan rangkaian instrumentasi memperkuat sinyal voltase ini, karena potensial pada

tubuh hanya berkisar antara 1μV untuk tengkorak atas, 1mV untuk bagian lengan dan 0.1V untuk bagian *exposed viscera* (*viscera*=jeroan).

2.4.2. Prinsip Kerja Elektroda.

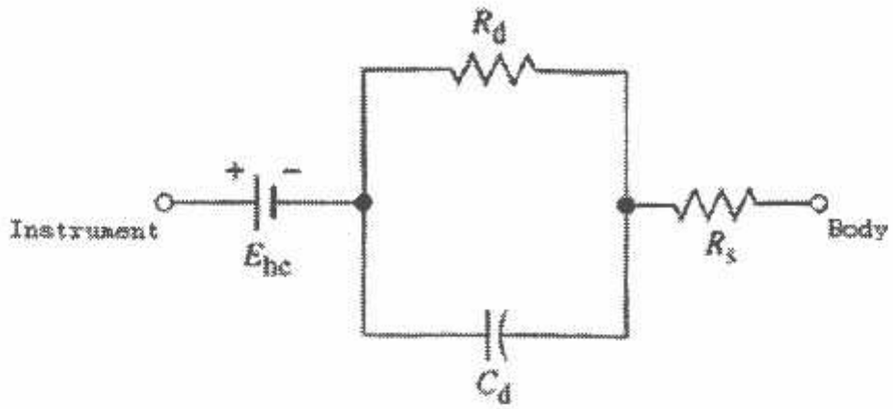
Untuk dapat memahami prinsip kerja elektrode permukaan metal elektrolit maka kita perhatikan **Gambar 2.6.** di bawah ini. Potensial elektrode metal dibentuk oleh elektron-elektron yang terkandung dalam cairan elektrolit dan ditinggalkan oleh cairan elekrolit tersebut sehingga masuk ke plat metal, peninggalan muatan elektron-elektron tersebut bervariasi seperti fungsi suatu posisi. Distribusi muatan ini serupa pada distribusi muatan pada kapasitor yang mana positif pada permukaan yang satu dan negatif pada permukaan yang lain.



Gambar 2.4. Distribusi Muatan Pada Elektroda Permukaan

Oleh karena itu, rangkaian ekuivalen listrik untuk hubungan ini mengandung kapasitor, *Cd*. Distribusi muatan elektron-elektron ini juga menyebabkan suatu potensial listrik yang disebut *half-cell potential* (E_h). Resistansi bocor *Rd* muncul di seberang ekuivalen kapasitansi. Sebuah resistansi seri pada rangkaian ekuivalen *Rs* mengakibatkan aliran cairan elektrolit pada

keseimbangan muatan. Rangkaian equivalen untuk elektroda permukaan ditunjukkan gambar dibawah:



Ehc - half-cell potential
Cd - electrode capacitance
Rd - leakage resistance
Rs - Series electrolyte and skin resistance

Gambar 2.5. Rangkaian Ekuivalen Elektroda Permukaan

Impedansi elektrode pada rangkaian ekuivalen diatas diberikan oleh rumus untuk kombinasi impedansi, seperti berikut:

$$Z = Rs + \frac{Rd}{j\,2\pi f\,Cd} \Big/ \left(Rd + \frac{1}{j\,\pi f\,Cd}\right) \qquad \text{..... (2.1)}$$

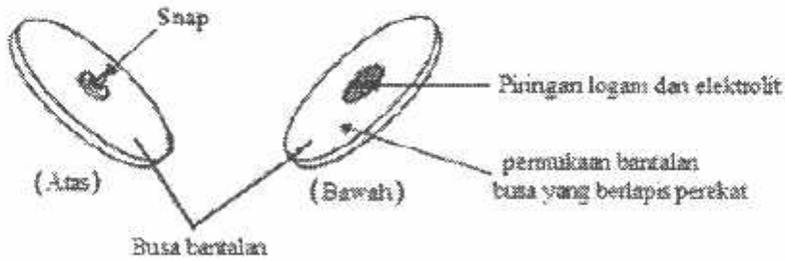
Dari rumus di atas dapat disederhanakan, sehingga :

$$Z = Rs + \frac{Rd}{1 + j\,2\pi f\,Cd\,Rd} \qquad \text{..... (2.2)}$$

Rumusan impedansi ini memberikan suatu uraian yang tepat tentang perilaku listrik pada elektroda permukaan. Hal ini sangat penting untuk dicatat bahwa suatu impedansi adalah fungsi dari frekwensi.

2.4.3. Elektroda Disposabel.

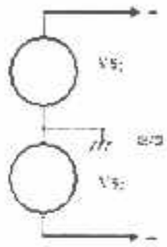
Pemakaian elektroda ada yang menembus kulit (*invasive*) seperti elektroda jarum dan ada elektroda permukaan yang tidak menembus kulit (*non invasive*). Jenis elektroda yang terakhir ini sering dipakai dalam lingkungan klinis karena memiliki resiko yang kecil seperti resiko infeksi penyakit maupun infeksi akibat pemakaian elektroda itu sendiri. Permukaan elektroda ada yang terdiri dari plat metal yang dilapisi oleh cairan elektrolit atau berupa suatu plat metal yang yang terpisah dari permukaan tubuh oleh suatu insulator yang mana fungsinya menyerupai sebuah pengkopel. Dalam perancangan akuisisi dan pemrosesan sinyal elektrokardiograph ini menggunakan elektroda *disposable*. Pemakaian elektroda ini ada yang direkatkan atau ditempelkan pada permukaan tubuh seperti stiker dan ada pula yang menggunakan penjepit/klip. Biasanya elektroda *disposable* yang direkatkan seperti stiker hanya dapat digunakan untuk sekali pemakaian saja karena perekatnya tidak tahan lama. Seperti yang dijelaskan pada **Gambar 2.6.** di bawah ini.



Gambar 2.6. Elektroda Disposabel dengan bantalan busa, biasa digunakan untuk ECG[5]

2.5. Biopotensial Amplifier.

Elektrokardiograf terukur sebagai beda potensial antara dua anggota tubuh. Jika digambarkan equivalennya, maka beda potensial ini seperti ada dua sumber tegangan.

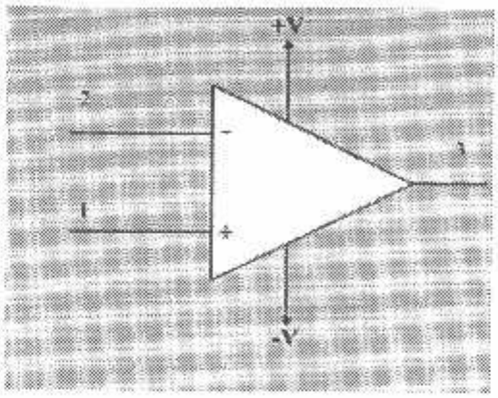


Gambar 2.7. Dua Potensial Berbeda Yang Teruku- ECG

Sehingga dengan adanya dua sumber tegangan yang berbeda ini maka diffirensial amplifiernya adalah yang ideal untuk mengukur beda potensial ini dan sering kali dipakai untuk aplikasi instrumentasi medika.

Salah satu keunggulan yang ada pada differensial amplifier adalah cenderung untuk menghilangkan interferensi *commond mode voltage* (CMV). *Commond mode voltage* adalah apapun yang memiliki nilai yang sama pada semua input terminal differensial amplifier. Maksudnya adalah jika Vin1 dan Vin2 adalah *common mode voltage* (CMV), maka Vin1=Vin2, dan Vout –nya adalah nol. Sehingga tegangan output cenderung mengarah atau menjadi nol karena *commond mode interference*.

2.6. Penguat Kerja (Op-Amp).



Gambar 2.8. Simbol Penguat Kerja (OP-Amp)[6]

Op-amp mempunyai beberapa karakteristik yang paling diketahui oleh seorang perancang, tetapi model op-amp yang ideal hanya mempunyai dua sifat yang diperlukan dalam analisa rangkaian yaitu :

- Arus yang masuk ke kedua kutub masukannya sama dengan 0.
- Tegangan diantara dua kutub masukannya sama dengan 0.

Berikut ini akan dibahas bagaimana Differensial Amplifier yang ideal, penguat pembalik, penguat tak-membalik, fungsi Op-amp sebagai penguat instrumentasi, dan pengikut tegangan. Op-Amp memiliki persamaan sebagai berikut:

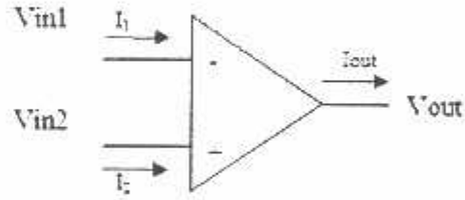
$$V_{Out} = A_d(V_{in2} - V_{in1}) \quad \text{..... (2.3)}$$

Dimana :

1. Vin1 dan Vin2 adalah tegangan input jika terukur terhadap ground.
2. Vout adalah tegangan output.
3. Ad adalah tegangan differensial gain.

2.6.1. Ideal Differensial Amplifier

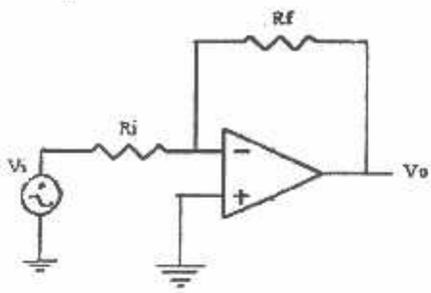
Differensial amplifier dapat diproduksi atau dibuat dalam bentuk rangkaian *Integrated Circuit* (IC) dengan biaya yang sangat murah sehingga hal ini memungkinkan untuk membuat suatu amplifier dengan *input impedance* yang sangat tinggi sehingga memungkinkan juga untuk membuat *gain amplifier* yang sangat tinggi pula. Semuanya ini dapat dibuat dengan dengan biaya yang murah jika kebutuhan untuk daya (*power requirement*) rendah dan kisaran frekwensi (*frequency range*) berada pada kisaran yang diperlukan untuk biopotensial amplifier sehingga menjadi ekonomis dan praktis untuk mendefinisikan suatu differensial amplifier yang ideal sebagai suatu komponen untuk analisis rangkaiannya.



Gambar 2.9. Simbol Differensial Amplifier Yang Semua Tegangannya Terukur Dengan Referensi Terhadap *Common Ground*

2.6.2. Penguat Pembalik (*Inverting Amplifier*).

Seperti yang sudah dijelaskan di atas bahwa apabila pada suatu penguat inversi diberikan sinyal masukan positif maka keluarannya akan negatif karena penguatan inversinya adalah penguatan pembalik yang keluarannya berbalik fasa 180° dengan masukannya.



Gambar 2.10. Rangkaian Penguat Inversi[7]

Keterangan gambar :

- Ri : Resistor masukkan
- Rf : Resistor umpan balik

Pada rangkaian penguat inversi, masukkan positif dihubungkan dengan *ground* atau *common ground*, sedangkan masukkan negatifnya digunakan sebagai masukkan sinyal yang akan dikuatkan.

Dari gambar diatas didapatkan persamaan tegangan output (Vo):

$$\frac{Vo}{Ri} = -\frac{Vi}{Rf} \triangleright \frac{Vo}{Vi} = -\frac{Rf}{Ri} \quad \text{..... (2.4)}$$

Sehingga ;

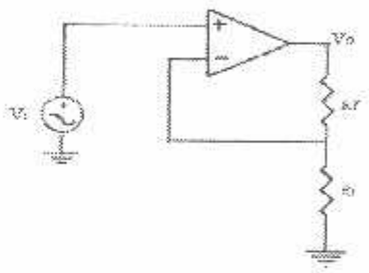
$$Vo = -\frac{Rf}{Ri} Vi \quad \text{..... (2.5)}$$

Sedangkan penguatannya (*gain*) :

$$A = \frac{Vo}{Vi} = -\frac{Rf}{Ri} \quad \text{..... (2.6)}$$

2.6.3. Penguat Tak Pembalik (*Non-inverting Amplifier*).

Prinsip rangkaian penguat non-inversi (tak membalik) merupakan kebalikan dari penguat inversi sehingga konstruksi rangkaiannya pun juga berbeda. Dari gambar di bawah dapat disimpulkan bahwa penguat non-inversi menggunakan prinsip pembagi tegangan (*voltage divider*) sehingga dapat dituliskan persamaan tegangan output (Vo):



Gambar 2.11. Rangkaian Penguat Non-Inversi (Tak Membalik)

$$Vi = \frac{RiVo}{Ri + Rf} \quad \text{..... (2.7)}$$

$$\frac{Vo}{Vi} = \frac{Ri + Rf}{Ri} \quad \text{..... (2.8)}$$

Sehingga ;

$$Vo = 1 + \frac{Rf}{Ri} Vi \quad \text{..... (2.9)}$$

Sedangkan penguatannya (*gain*) :

$$A = \frac{Vo}{Vi} = 1 + \frac{Rf}{Ri} \quad \text{..... (2.10)}$$

2.6.4. Op-Amp Sebagai Penguat Instrumentasi.

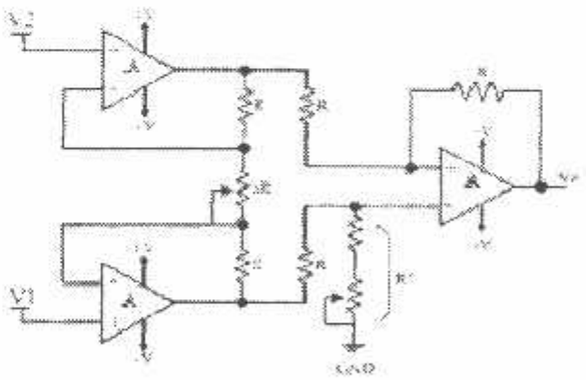
Penguat instrumentasi dibuat dari tiga op-amp dan tujuh hambatan, seperti dalam **Gambar 2.12.** Penguat instrumentasi sesungguhnya dibuat dengan menghubungkan penguat differensial dasar ke sebuah penguat penyangga (*Buffer*).

Jika tegangan masukan dari setiap op-amp besarnya 0 V, maka tegangan di titik 1 dan titik 2 sama dengan V_1 dan V_2. Bila V_1 lebih besar dari V_2 maka besar tegangan antara titik 1 dan 2 adalah $V_1 - V_2$. Arus yang melalui hambatan aR yaitu:

$$I = \frac{V_1 - V_2}{aR} \quad \text{..... (2.11)}$$

besar tegangan keluaran op-amp A_2 yaitu :

$$V_{A2} = V_2 - \frac{V_1 - V_2}{a} \quad \text{..... (2.12)}$$



Gambar 2.12. Penguat Instrumentasi

Besar tegangan keluaran op-amp A_1 adalah :

$$V_{A1} = V_1 + \frac{V_1 - V_2}{a} \quad \text{..... (2.13)}$$

Besarnya tegangan keluaran op-amp A_3 yaitu :

$$V_o = (V_1 - V_2)\left(1 + \frac{2}{a}\right) \quad \text{..... (2.14)}$$

Besar Penguatan dari rangkaian penguat instrumentasi yaitu :

$$\frac{V_o}{(V_1 - V_2)} = \left(1 + \frac{2}{a}\right) \quad \text{..... (2.15)}$$

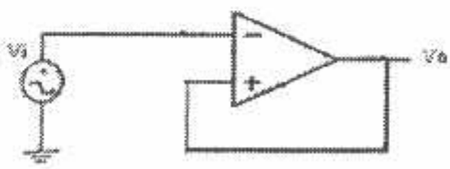
Dari persamaan (2.15) dapat diubah guna mendapatkan nilai a yaitu :

$$a = \frac{2}{\left(\frac{V_o}{(V_1 - V_2)}\right) - 1} \quad \text{..... (2.16)}$$

2.6.5. Pengikut Tegangan (*Voltage Follower*).

Rangkaian pengikut tegangan kadang disebut juga sebagai rangkaian penyangga (*buffer amplifier*) dan memiliki fungsi yang sama seperti pengikut emiter (*emither follower*) atau pengikut katoda (*cathode follower*). Ciri-ciri rangkaian pengikut tegangan adalah :

- Memiliki impedansi masukkan yang sangat tinggi ; (lebih dari 100kΩ).
- Memiliki impedansi keluaran yang sangat rendah ; (kurang dari 75Ω).



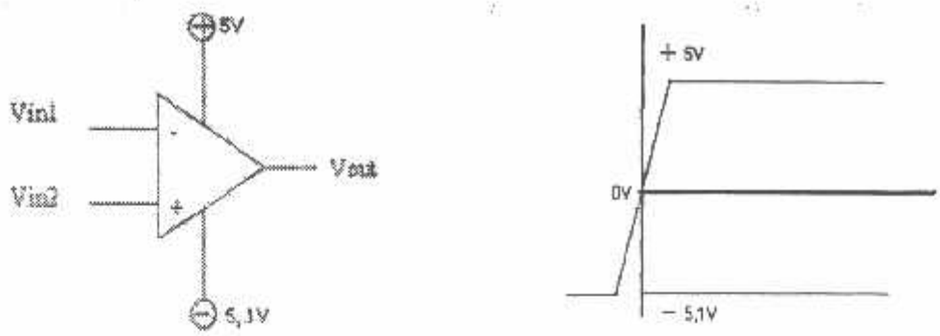
Gambar 2.13. Pengikut Tegangan

Jika dibandingkan dengan rangkaian penguat non inversi (**gambar 2.11**) maka rangkaian pengikut tegangan adalah sama, dengan Ri = ∞ dan Rf = 0.

Dengan demikian penguatan tegangan selalu = 1. Sinyal keluaran sama persis (identik) dengan sinyal masukkan atau keluaran mengikuti masukkan, sehingga Vin= Vout. Fungsi utama dari rangkaian pengikut tegangan adalah sebagai penyangga atau mengisolasi beban dari sumber.

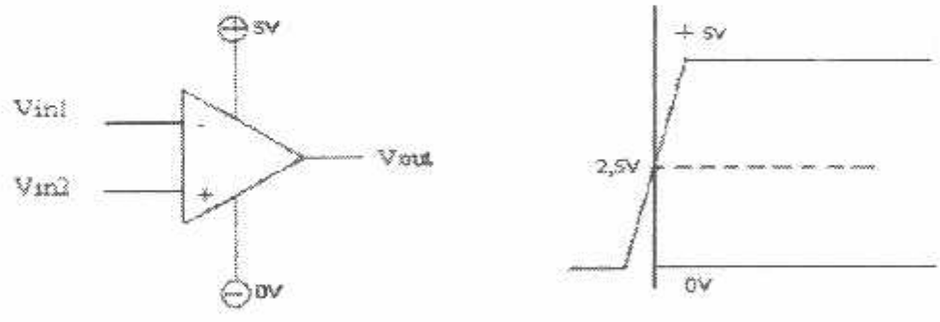
2.6.6. *Referensial Amplifier.*

Seperti yang telah kita ketahui bahwa setiap *Op-Amp* yang digunakan dalam rangkaian instrumentasi atau rangkaian yang lainnya dapat menggunakan dua tipe catu daya, yaitu catu daya simetris dan catu daya tunggal. Namun dalam beberapa kasus, jika menggunakan *Op-Amp* yang di catu daya simetris kadang-kadang atau malah seringkali tegangan yang dikeluarkan catu daya tersebut tidak seimbang (tegangan antara +, 0 dan -). Hal ini dapat mempengaruhi kinerja *Op-Amp* karena akan menghasilkan sinyal dengan amplitudo yang tidak sama dan menyebabkan *Op-Amp* tidak ideal. Pada **Gambar 2.14** di bawah menunjukkan *Op Amp* yang diberi catu daya simetris yang mana tegangan antara positif dan negatifnya tidak sama dan kurva karakteristik yang menunjukkan akibat dari selisih kedua tegangan tersebut.



Gambar 2.14. Op-Amp yang menggunakan catu daya simetris

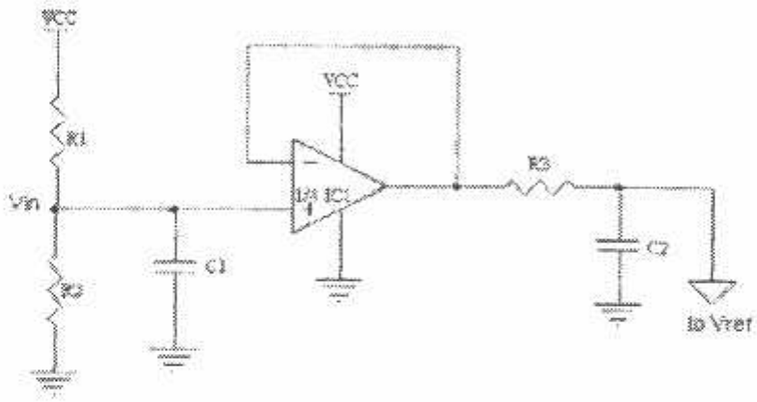
Dari contoh gambar diatas terlihat adanya beda tegangan sebesar 0,1V sehingga garis referensial untuk 0V tidak berada tepat ditengah. Untuk mengatasi hal tersebut alangkah baiknya jika menggunakan Op-Amp yang dicatu daya tunggal sehingga nantinya titik referensinya berada pada 2,5V. Gambar dibawah menunjukkan contoh Op-Amp yang yang menggunakan catu daya tunggal dengan tegangan 0V dan 5V.



Gambar 2.15. Op-Amp yang menggunakan catu daya tunggal

Tapi perlu diketahui juga bahwa didalam menggunakan catu daya tunggal khususnya dalam instrumentasi amplifier untuk *ECG*, sinyal *ECG* bisa dalam kondisi positif maupun negatif yang artinya dalam kondisi positif sinyal *ECG* ada

yang berada diatas pada daerah tegangan positif, ada pula sinyal *ECG* yang berada dibawah pada daerah tegangan negatif sehingga karena catu dayanya adalah tunggal maka sinyal *ECG* yang berada dibawah akan hilang. Untuk mengatasi hal ini diperlukan suatu rangkaian yang dapat mengangkat sinyal *ECG* tersebut agar berada pada kondisi antara 0V dan 5V, sehingga titik referensinya berada pada 2,5V seperti yang terlihat pada **Gambar 2.15**. Sedangkan rangkaian yang yang dapat mengangkat sinyal ECG tersebut dikenal dengan sebutan *referensial amplifier*. Adapun rangkaiannya ditunjukkan pada gambar dibawah :



Gambar 2.16. *Referensial Amplifier*

Perlu sedikit dijelaskan bahwa cara kerja rangkaian *referensial amplifier* berdasarkan pada prinsip pembagi tegangan (*voltage divider*) yang dilakukan oleh R1 dan R2. Kedua resistor tersebut bekerja pada daerah tegangan antara 0V dan 5V sehingga tegangan diantara R1 dan R2 (Vin) menjadi titik referensi 2,5V karena harga Vin adalah setengah harga Vcc. Titik inilah yang menjadi titik acuan sinyal *ECG* nantinya. Sedangkan *buffer amplifier* digunakan untuk mendapatkan

tegangan keluaran yang sama dengan tegangan masukkannya dengan impedansi masukkan yang tinggi dan impedansi keluaran yang rendah.

2.7. Rangkaian Penapis (*Filter*)

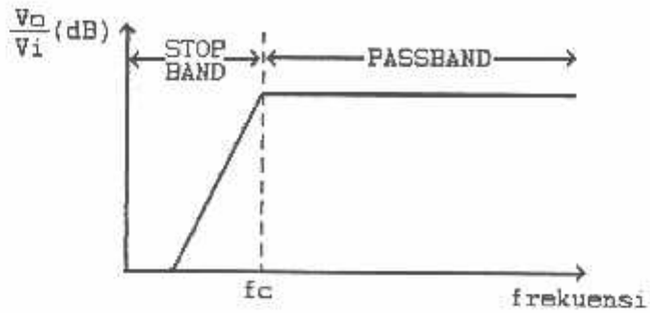
Rangkaian penapis (*filter*) adalah sebuah rangkaian yang dapat melewatkan atau meloloskan sinyal dan menahan sinyal yang tidak diinginkan pada frekwensi tertentu. Rangkaian penapis ada dua jenis, yaitu penapis analog dan penapis digital, sedangkan penapis analog itu sendiri ada dua macam tipe, yaitu penapis aktif dan penapis pasif. Rangkaian penapis aktif maupun pasif memiliki karakteristik sinyal yang sama hanya saja pada penapis aktif terdapat penguatan *passband*-nya. Ini dikarenakan penapis aktif menggunakan komponen aktif sebagai pembangun dasarnya yang mana dalam hal ini komponen aktif tersebut adalah IC *Op-Amp*.

Penapis digital sangat berbeda dengan rangkaian elektronik digital atau program komputer yang memroses sinyal untuk melaksanakan fungsi yang serupa seperti pada penapis analog. Tidak seperti penapis analog, penapis digital beroperasi berdasarkan jumlah nomor urutan yang lebih baik pada suatu gelombang kontinyu. Namun dalam penulisan skripsi ini tidak akan membahas penapis digital karena pada perencanaan alatnya tidak menggunakan *digital filter*.

2.7.1. High Pass Filter.

High Pass Filter adalah sebuah rangkaian yang memeperlemah semua sinyal di bawah suatu prekuensi *cut-off* tertentu ω_c dan melewatkan semua sinyal

yang frekuensi nya di atas frekuensi cutt off tersebut. Di bawah ini adalah karakteristik dari *High Pass Filter.*



Gambar 2.17. Karakteristik High Pass Filter

High pass filter menggunakan persamaan :

$$fc_o = \frac{1}{2\pi RC} \quad \text{..... (2.17)}$$

Sedangkan penguatan *passband*-nya adalah :

$$dB = -20 \log 10 \frac{Vo}{Vi} \quad \text{..... (2.18)}$$

Jika Vo > Vi, maka terjadi penguatan karena nilainya positif.

Jika Vo < Vi, maka terjadi pelemahan (*atenuasi*) karena nilainya negatif.

2.7.2. Band-pass Filter.

Band-pass filter adalah sebuah rangkaian yang dirancang hanya untuk melewatkan isyarat dalam suatu pita frekuensi tertentu seraya menolak semua isyarat diluar pita ini. Pada **Gambar 2.18(a)**. Memperlihatkan tanggapan frekuensi dari sebuah band-pass filter. Jenis filter ini mempunyai tegangan keluaran maksimum V_{max} , atau gain tegangan maksimum A_c , pada suatu

frekuensi resonan ω_r , jika frekuensi diubah-ubah dari resonansinya, tegangan keluarannya turun. Ada satu frekuensi diatas ω_r dan satu dibawah ω_r dimana gain tegangannya adalah 0,707 A_r. Frekuensi ini diberi tanda dengan ω_h , frekuensi *cutoff* atas dan ω_l , frekuensi *cutoff* bawah. Pita frekuensi antara ω_h dan ω_l adalah lebar pita, B:

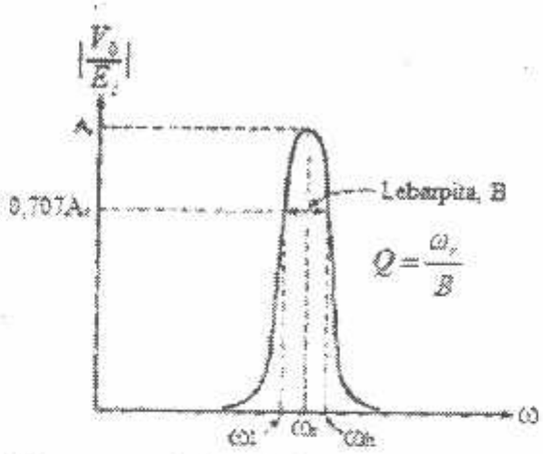
$$B = \omega_h - \omega_l \quad \text{..... (2.19)}$$

Filter-filter band-pass digolongkan sebagai pita-sempit atau pita-lebar. Pita-sempit adalah sebuah filter yang mempunyai lebarpita lebih kecil dari sepersepuluh frekuensi resonannya ($B < 0{,}1\ \omega_r$). Jika lebarpitanya lebih besar sepersepuluh frekuensi resonannya ($B > 0{,}1\ \omega_r$), filter tersebut merupakan sebuah filter pita-lebar. Perbandingan frekuensi resonan terhafap lebar pita dikenal sebagai faktor kualitas, Q, dari rangkaiannya. Q menunjukkan selektifitas rangkaiannya. Makin tinggi harga Q, makin selektif rangkaiannya. Dalam bentuk persamaan:

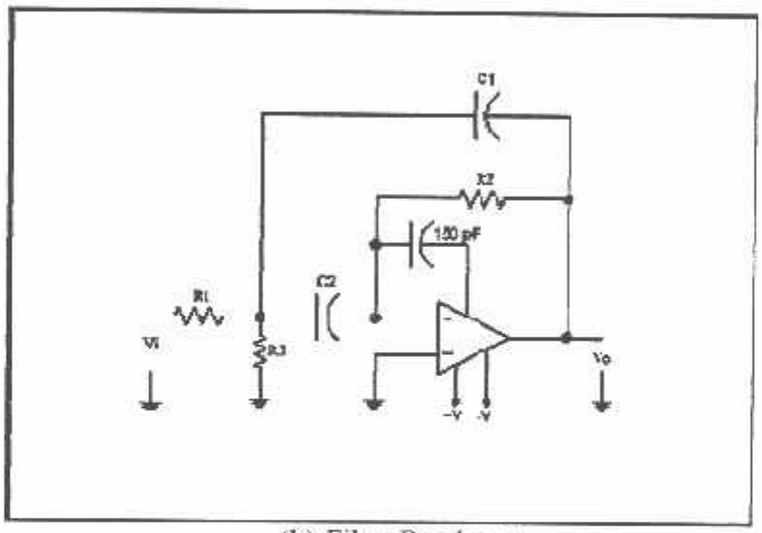
$$Q = \frac{\omega_r}{B} \quad \text{..... (2.20)}$$

atau:

$$B = \frac{\omega_r}{Q} \quad \text{rad/s} \quad \text{..... (2.21)}$$



(a) Tanggapan frekuensi dari sebuah band-pass filter



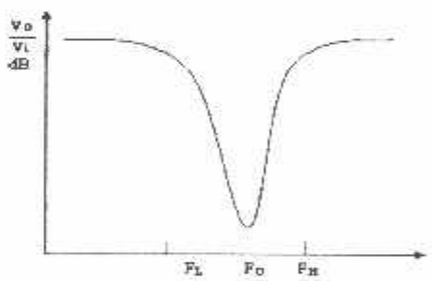
(b) Filter Band-pass

Gambar 2.18. Filter Band-pass dan Tanggapan Frekuensi

Untuk filter-filter pita-sempit, Q dari rangkaian lebih besar dari 10, dan untul filter-filter pita-lebar, Q lebih kecil dari 10.

2.8. *Band Reject Filter.*

Band Reject Filter merupakan kebalikan dari *band pass filter*. Dari gambar karakteristiknya terlihat bahwa filter ini akan menahan sinyal-sinyal dengan frekwensi antara/median dan akan meneruskan sinyal-sinyal dengan frekwensi dibawah dan diatas frekwensi antara. Definisi lebar pita (*Band Width*) sama seperti pada *band pass filter*. Demikian juga dengan frekwensi atas (F_H) dan frekwensi bawah (F_L) sama dengan yang ada pada *band pass filter*. Banyak sekali macam-macam *Band Reject Filter* yang digunakan dalam perancangan instrumentasi elektronika. Dalam perancangan instrumentasi bioelektrik *Band Reject Filter* digunakan untuk menekan noise sinyal dengan frekwensi 50Hz-60Hz yang berasal dari jala-jala listrik PLN.



Gambar 2.19. Karakteristik *Band Reject Filter.*

2.9. ADC (Analog to Digital Converter)[8].

Agar tegangan yang dikeluarkan oleh rangkaian penguat instrumentasi dan rangkaian filter dapat dibaca oleh *(PC) Personal Computer*, maka nilai tegangan tersebut harus diubah menjadi bentuk data digital. Untuk itu digunakan Konverter Analog Ke Digital (ADC). ADC yang digunakan dalam perancangan in adalah ADC 0804 (Produksi National Semiconductor Coorporation) yang merupakan

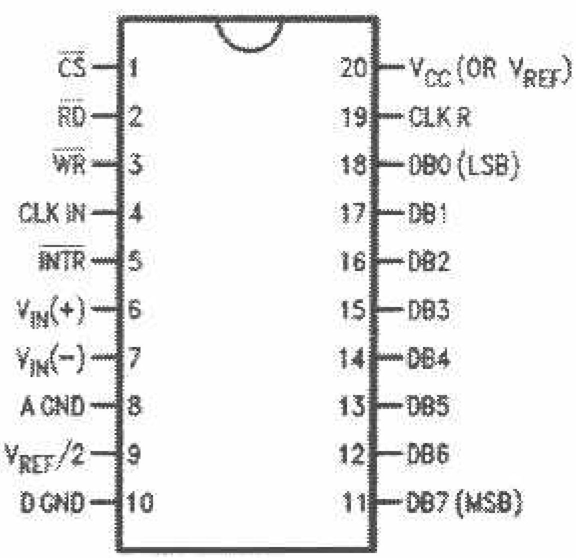
ADC dengan 2 masukan analog yang di multipleks menjadi data digital 8 bit. ADC 0804 membutuhkan sampai dengan 100μs untuk menkonversikan sebuah tegangan masukan analog ke dalam kode keluaran digital. Dalam perancangan alat ini digunakan dua buah input analog yaitu $V_{IN}(+)$ dan $V_{IN}(-)$. Dikarenakan tegangan yang terukur cukup kecil maka tingkat resolusi ADC 0804 yang diharapkan cukup besar, sehingga pada ADC 0804 menggunakan V_{ref} sebesar 5V (jika $V_{ref}/2$ tidak digunakan), dimana tingkat resolusi ADC 0804 ini adalah:

$$\text{Resolusi} = \frac{V_{referensi}}{(2^8 - 1)} \quad \text{.......} \quad (2.22)$$

Jadi besarnya resolusi adalah sebesar :

$$\text{Resolusi} = \frac{5\,V}{(2^8 - 1)} = 0{,}0196V = 19{,}6\ mV$$

Sehingga dengan perubahan inputan analog 19,6 mV maka output dari ADC akan mengalami perubahan 1 bit.



Gambar 2.20. Konfigurasi pin ADC 0804

Penjelasan dari masing-masing pin adalah sebagai berikut:

Vcc (OR VREF)	Power supply -/+ 5VDC.
D GND, A GND	Ground.
VIN(+), VIN(-)	Input besaran Analog yang ingin dikonversi ke dalam besaran Digital. Maksimal 5V, dihubungkan dari sebuah penguat operasional dalam dan masukkan-masukkan difernsial.
Port DB (DB0..DB7)	Port DB (DB0..DB7) merupakan port Output 8-bit data Digital hasil konversi dari data Analog.
VREF/2	Port VREF/2 merupakan port masukan untuk tegangan referensi, tidak digunakan apabila **Vcc (OR VREF)** digunakan.
CLK R	Pin ini dihubungkan dengan Resistor yang diseri dengan Kapasitor, berfungsi sebagai Clock/Counter.
CLK IN	Berfungsi sebagai Input Clock/Counter. Dihubungkan dengan rangkaian **CLK R** di antara Resistor dan Kapasitor.

2.9.1. Sistem Kerja ADC 0804.

Untuk mengoperasikan converter, pin$\overline{WR}$ diberi pulsa dengan $\overline{CS}$ yang dihubungkan dengan Ground untuk mulai memulai proses pengkonversian. Ada dua masukkan analog terhadap ADC 0804: VIN(-) dan VIN(+). Masukkan-

masukkan ini dihubungkan dengan penguat operasional (Op-Amp) dan masukkan-masukkan diferensial. Masukkan-masukan diferensial dijumlahkan dengan penguat operasional untuk menghasilkan sebuah sinyal untuk converter analog ke digital.

2.9.2. Membangkitkan Sinyal Clock.

ADC 0804 membutuhkan sebuah sumber clock untuk melakukan operasinya. Clock ini dapat sebuah clock dari luar (*external clock*) yang diterapkan ke pin **CLK IN** atau clock yang dapat dibangkitkan dengan rangkaian RC (Resisansi dan Capasitansi). Ketika hubungan ini digunakan, referensi clock (*clock reference*) dihitung dengan persamaan:

$$F_{clk} = \frac{1}{1{,}1RC} \quad \text{..... (2.23)}$$

Kelebihan dari ADC 0804:

- Waktu konversi dari data input analog ke data output digital memerlukan waktu 100μs
- Logika input dan output memenuhi syarat level tegangan untuk spesifikasi MOS dan TTL.
- Bekerja dengan tegangan referensi 2.5V.
- Pembangkit clock/counter terdapat pada chip.
- 0V s/d 5V input tegangan analog dengan catu daya tunggal 5V.
- Lebar chip 0.3 inchi dengan kemasan 20-pin DIP.

2.10. DB 25 *Connector.*

Konektor DB-25 (dinamakan demikian karena seukuran huruf "B", tetapi berbentuk huruf "D" dan memiliki 25 pin) banyak digunakan pada industri elektronik. Konekor DB-25 digunakan untuk beberapa tujuan. Dua aplikasi yang umum adalah koneksi RS-232/EIA-232 (serial), dan antarmuka *printer* parallel pada *PC* (*Personal Computer*). Konektor DB-25 juga digunakan pada **SCSI** (***Small Computer System Interface***) koneksi. **SCSI** adalah sebuah standar untuk secara fisik menghubungkan dan mentransfer data antara komputer dan perangkat antarmuka.

DB25 adalah *Connector* sebuah perangkat antarmuka (*interface*) dalam hal ini rangkaian ECG dengan PC (*Personal Computer*). Memiliki 25 pin seperti yang tampak pada **Gambar 2.21.** di bawah ini. DB-25 ini juga dapat digunakan untuk menghubungkan printer dengan *PC* (*Personal Computer*).

Gambar 2.21. Konfigurasi Pin Port DB-25

Tabel 2.2. Fungsi pin-pin pada DB-25.

Pin No (D-Type 25)	Pin No (Centronics)	SPP Signal	Direction In/out	Register	Hardware Inverted
1	1	nStrobe	In/Out	Control	Yes
2	2	Data 0	Out	Data	
3	3	Data 1	Out	Data	
4	4	Data 2	Out	Data	
5	5	Data 3	Out	Data	
6	6	Data 4	Out	Data	
7	7	Data 5	Out	Data	
8	8	Data 6	Out	Data	
9	9	Data 7	Out	Data	
10	10	nAck	In	Status	
11	11	Busy	In	Status	Yes
12	12	Paper-Out PaperEnd	In	Status	
13	13	Select	In	Status	
14	14	nAuto-Linefeed	In Out	Control	Yes
15	32	nError / nFault	In	Status	
16	31	nInitialize	In Out	Control	
17	36	nSelect-Printer nSelect-In	In Out	Control	Yes
18 - 25	19-30	Ground	Gnd		

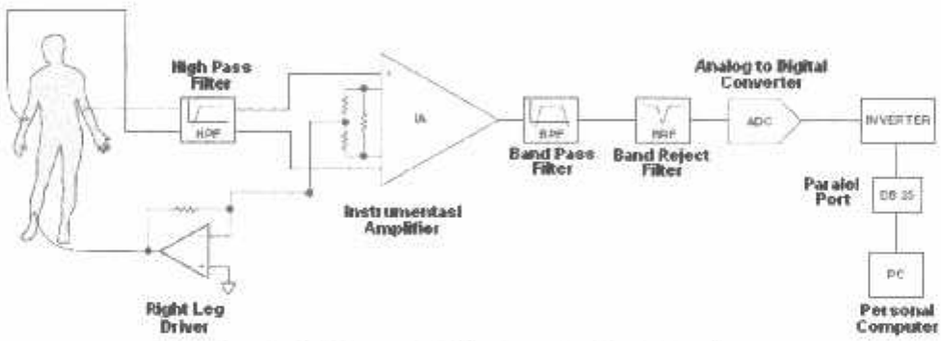
BAB III

PERANCANGAN DAN PEMBUATAN ALAT

Dalam bab ini akan dijelaskan mengenai perencanaan dan pembuatan alat *ECG Monitoring* Yang Ditampilkan Pada *PC* (*Personal* Computer), baik perancangan *hardware* maupun perancangan *software*-nya.

3.1. Perancangan *Hardware*

Secara diagram blok perencanaan perangkat keras alat ini ditunjukkan dalam **Gambar 3.1**:



Gambar 3.1. Diagram Blok Pengakuisisi Sinyal ECG.

KETERANGAN:

- Elektroda

Berfungsi sebagai sensor yang bekerja dengan cara merubah potensial ionik akibat gerakan jantung melalui permukaan tubuh menjadi sinyal listrik yang berupa tegangan.

- HPF (*High Pass Filter*)

HPF (*High Pass Filter*) adalah rangkaian yang berguna untuk meloloskan frekuensi tinggi dimana dirancang dengan frekuensi *cutoff* 0,15Hz. HPF juga berguna untuk memblok sinyal DC.

- (IA) Instrumentasi Amplifier

Rangkaian ini merupakan rangkaian utama yang terdiri dari rangkaian *Impedance Converter* dan *Differencial Amplifier*. *Impedance converter* berfungsi seperti *buffer amplifier* dengan impedansi *input* yang sangat tinggi sehingga dapat mengukur biopotensial jantung tanpa membebani tegangan yang diukur. *Differensial amplifier* berfungsi untuk mengambil sinyal EKG dengan cara mengukur selisih tegangan antara dua sisi tubuh (dalam hal ini kedua input-an Instrumentasi Amplifier) serta menghilangkan interferensi tegangan mode bersama (*common mode voltage*). Instrumentasi Amplifier diperlukan karena sinyal listrik yang diukur adalah sinyal listrik pada dua permukaan tubuh, sehingga nantinya sinyal listrik yang terukur adalah selisih antara kedua sinyal listrik tersebut.

- BPF (*Band Pass Filter*)

Rangkaian filter ini terdiri dari HPF (*High Pass Filter)* yang akan meloloskan frekuensi di atas 0,15Hz dan LPF (*Low Pass Filter)* yang akan meloloskan frekuensi di bawah 100Hz. Sehingga *filter* ini berfungsi untuk membatasi lebar frekuensi yang akan diloloskan, dengan frekuensi *cutoff* 0,15-100Hz. Karena *Bandwidth* untuk *monitoring* ECG adalah 0,15-100Hz.

- (BRF) *Band Reject Filter*

Band Reject filter berfungsi untuk menekan sinyal interferensi dari jala-jala PLN dengan frekuensi 50-60 Hz. Karena dengan adanya sinyal interferensi 50-60Hz, akan mengganggu pengukuran sinyal ECG yang akan diukur sehingga perlu ditekan.

- ADC (*Analog to Digital Converter*)

ADC berfungsi meng-konversi besaran analog kedalam besaran digital sehingga dapat diproses dan hasilnya dapat ditampilkan ke dalam PC (*Personal Computer*). Jadi, besaran analog dari sinyal ECG akan dikonversikan oleh ADC ini kedalam besaran digital.

- *Inverter*

Jika kita menghubungkan input secara langsung dengan port (sebagai contoh sebuah ADC0804), akan terjadi pertentangan jika input dalam kondisi *high* sedangkan port sendiri mencoba menjadikannya *low*. Untuk mengatasi hal ini kita menggunakan inverter[9].

- DB-25 *Parallel Port*

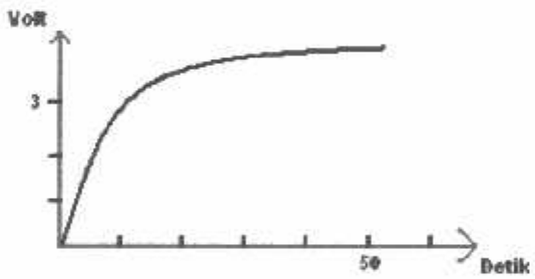
Berfungsi sebagai *Interface Port* agar hasil keluaran dapat diproses dan ditampilkan di PC. Karena walaupun besaran analog sinyal ECG sudah dikonversi ke besaran digital, tidak dapat diterima oleh PC kalau tidak melalui *Parallel Port* sebagai alat komunikasi antara ECG Amplifier dan PC.

- PC (*Personal Computer*)

Berfungsi sebagai *display* dari sinyal ECG yang telah didapat dari hasil pengukuran.

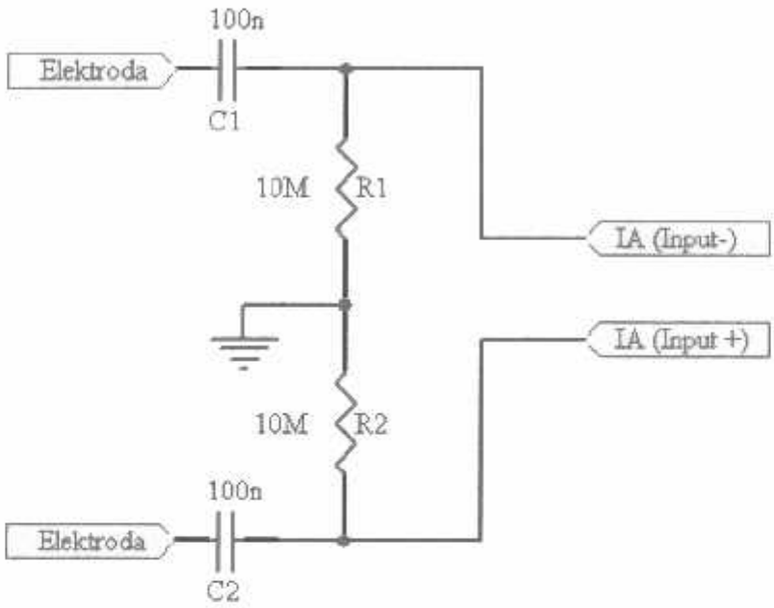
3.1.1. (HPF) *HIGH PASS FILTER*

Hal-hal yang mungkin perlu diperhatikan pada perancangan ini bahwa selain masukkan sinyal AC 1mV terdapat juga masukkan sinyal DC dari potensial offset elektroda yang besarnya sekitar ± 400mV dan noise elektroda yang menghasilkan frekuensi rendah 0,151Hz. Oleh karena terdapat juga sinyal masukkan DC dari potensial offset elektroda yang lebih besar dari sinyal bioelektrik jantung yang mungkin akan menyebabkan keluaran Op-Amp terjadi saturasi maka sinyal DC tersebut harus diblok/dibuang dengan menggunakan rangkaian *High Pass Filter* (HPF) dengan nilai R yang harus besar untuk menjaga arus DC kembali. Kita dapat mengetahui suatu rangkaian adalah rangkaian High Pass Filter karena terdapat sebuah Kapasitor di depan sebuah resistor yang terhubung ke ground. Dimana kemampuan kapasitor untuk menyimpan muatan listrik adalah salah satu karakteristik terpentingnya seperti yang terlihat pada **Gambar 3.2.** di bawah.



Gambar 3.2. Karakteristik Kapasitor

HPF dirancang dengan menggunakan Resistor dan Kapasitor seperti yang terlihat pada gambar di bawah ini.



Gambar 3.3. Rangkaian *High Pass Filter*

Dengan menggunakan R=10MΩ, maka nilai C dapat dicari dengan perhitungan:

$$f_O = \frac{1}{2\pi RC}, \text{ maka}$$

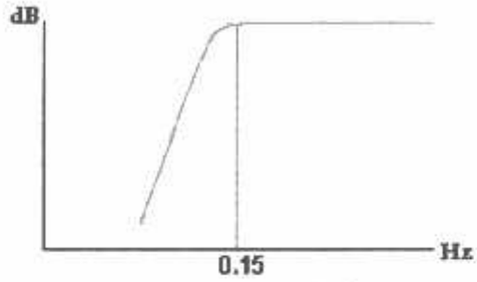
$$C = \frac{1}{2\pi R f_O} = \frac{1}{2x3{,}14x10x10^6 x0{,}15}$$

$$= \frac{1}{6{,}28x10x10^6 x0{,}15} \quad = \frac{1}{942x10^4}$$

$$= 1{,}06x10^{-7}\text{F} = 106x10^{-9}\text{F}$$

$= 106nF \approx 100nF.$

Maka digunakanlah Capasitor dengan nilai 100nF.



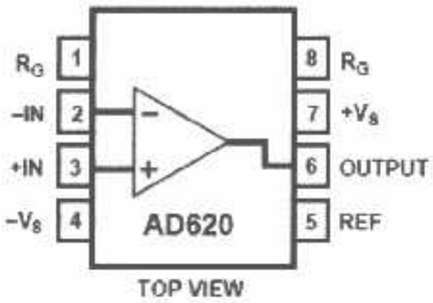
Gambar 3.3. Karakteristik HPF
dengan Frekuensi Cutoff 0,15Hz

3.1.2. (IA) *Instrumentasi Amplifier*

Digunakan IC AD620AN (**Gambar 3.4.**) sebagai Instrumentasi Amplifier Disamping lebih praktis, karena hanya menggunakan 1 IC Instrumentasi Amplifier daripada menggunakan 3 IC Op-Amp untuk membuat rangkaian Instrumentasi Amplifier.

CONNECTION DIAGRAM

8-Lead Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



Gambar 3.4. Tampak Atas dari AD620AN

AD620AN juga lebih presisi dengan penguatan yang dapat di-set dari penguatan 1x (satu kali) sampai penguatan 1000x (seribu kali) dengan menambahkan resistor eksternal sebagai RG (*Resistor Gain*) seperti yang tampak pada **Tabel 3.1.** di bawah ini.

Tabel 3.1. Nilai RG untuk masing-masing penguatan.

Required Values of Gain Resistors

1% Std Table Value of R_G, Ω	Calculated Gain	0.1% Std Table Value of R_G, Ω	Calculated Gain
49.9 k	1.990	49.3 k	2.002
12.4 k	4.984	12.4 k	4.984
5.49 k	9.998	5.49 k	9.998
2.61 k	19.93	2.61 k	19.93
1.00 k	50.40	1.01 k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003

Seperti yang terlihat pada **Gambar 3.5.** di bawah. Oleh produsen AD620AN, R1 dan R2 dirancang sedemikian rupa sehingga bernilai 24,7KΩ, sehingga nilai 2R = 49,4KΩ.

Sehingga:

Untuk G (Penguatan) 1000 kali, $R_G = \frac{49{,}4K\Omega}{G-1} = \frac{49{,}4K\Omega}{1000-1} = \frac{49{,}4K}{999} = 49{,}44\Omega$

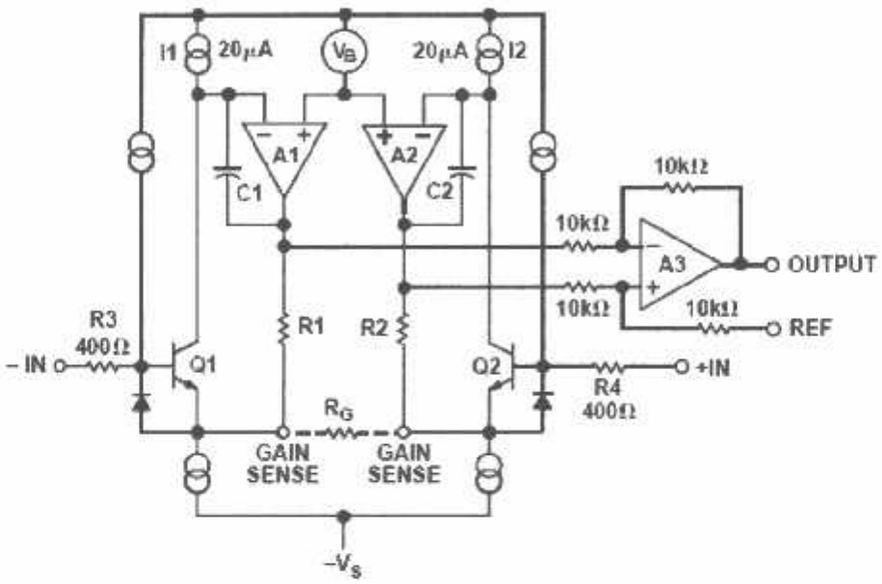
Dan,

Untuk G (Penguatan) 1 kali, $R_G = \frac{49{,}4K\Omega}{G-1} = \frac{49{,}4K\Omega}{1-1} = \infty$,

Maka untuk penguatan 1 kali digunakan R_G sebesar 50KΩ sehingga:

$G = \frac{49{,}4K\Omega}{R_G} + 1 = \frac{49{,}4K\Omega}{50K\Omega} + 1 = 0{,}988 + 1 = 1{,}988$ kali.

Jadi pada perancangan, penguatan AD620AN di-set dengan penambahan Resistor Variabel sebesar 50KΩ. Dengan demikian penguatan pada AD620AN dapat diset dari 1-1000 kali.



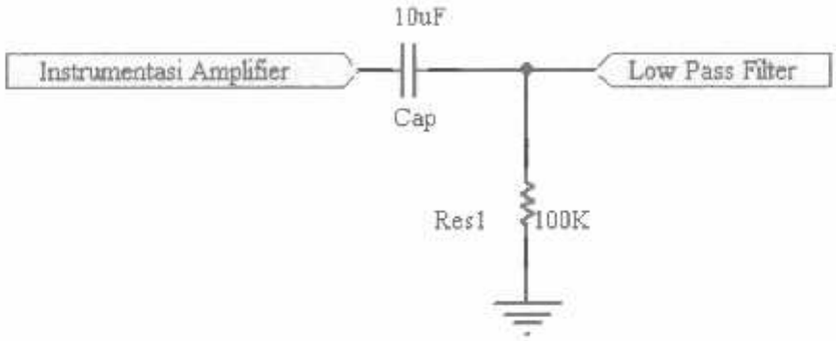
Gambar 3.5. Skema Sederhana dari AD620AN

3.1.3. (BPF) *Band Pass Filter*

Untuk keperluan *monitoring*, sinyal ECG dibatasi dalam frekuensi 0,15-100Hz. Dengan demikian maka dirancang sebuah filter band pass dengan frekuensi *cutoff* 0,15 -100 Hz. Untuk merancang sebuah *Band Pass Filter*, sebuah rangkaian *Low Pass Filter* dengan frekuensi *cutoff* 100Hz dirangkaikan secara seri dengan sebuah rangkaian *High Pass Filter* dengan frekuensi *cutoff* 0,15Hz. Maka rangkaian *Band Pass Filter* akan didapat dengan frekuensi *cutoff* sesuai dengan frekuensi *cutoff* *Low Pass Filter* dan *High Pass Filter*.

3.1.3.1. HPF (*High Pass Filter*).

Digunakan sebuah *High Pass Filter* seperti yang terlihat pada **Gambar 3.6.** di bawah ini dengan frekuensi *cutoff* 0,15 Hz sebagai bagian dari *Band Pass Filter* yang telah direncanakan di atas.



Gambar 3.6. Rangkaian *High Pass Filter* dengan *Cutoff* 0,15 Hz

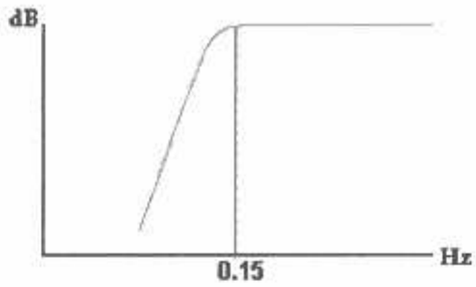
Dengan menggunakan R=100KΩ, maka nilai C dapat dicari dengan perhitungan:

$$f_C = \frac{1}{2\pi RC}, \text{ maka}$$

$$C = \frac{1}{2\pi R f_C} = \frac{1}{2x3{,}14x100x10^{3}x0{,}15}$$

$$= 10{,}6x10^{-6}\text{F} \approx 10\text{uF}.$$

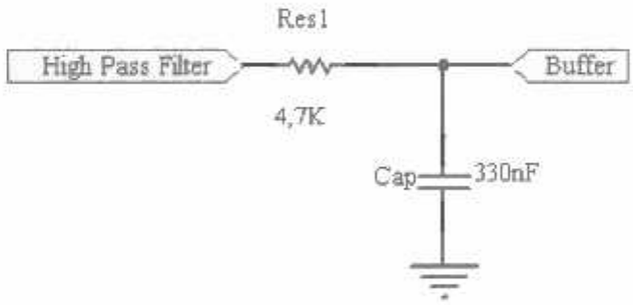
Maka digunakanlah Capasitor dengan nilai 10uF.



Gambar 3.7. Karakteristik HPF
dengan Cutoff 0,15Hz.

3.1.3.2. LPF (*Low Pass Filter*)

Seperti yang telah dirancanakan, sebuah *Low Pass Filter* digunakan bersama *High Pass Filter* untuk membentuk sebuah *Band Pass Filter*. Untuk merancang sebuah *Low Pass Filter* (tampak pada **Gambar 3.8.** di bawah ini) dengan frekuensi *cutoff* 100Hz, penulis menggunakan Resistor bernilai 4,7KΩ.



Gambar 3.8. Rangkaian *Low Pass Filter*
dengan *Cutoff* 100 Hz

Sehingga dengan perhitungan, akan didapat nilai Capasitor:

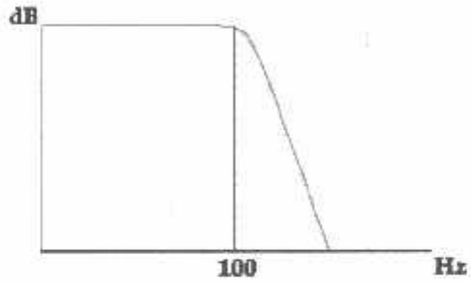
$$F_C = \frac{1}{2\pi RC}, \text{ maka}$$

$$C = \frac{1}{2\pi x R x f_C} = \frac{1}{2x3{,}14x4{,}7x10^{3}\,x100}$$

$$= 3{,}38x10^{-7}F = 338x10^{-9}F$$

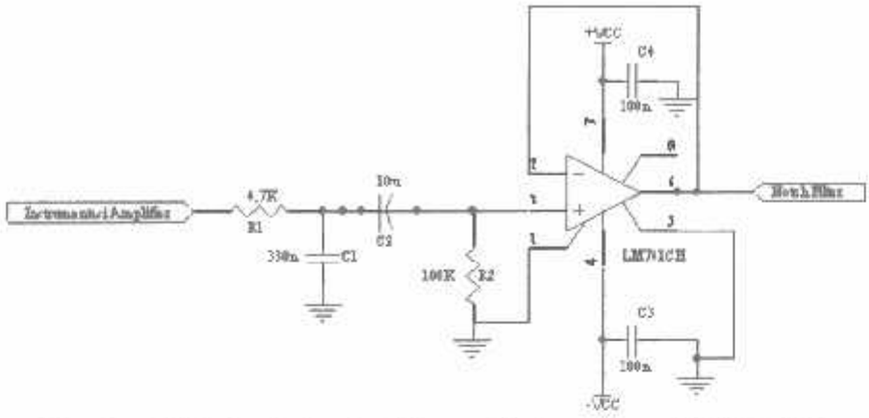
$$\approx 330x10^{-9} = 330nF.$$

Maka digunakanlah Capasitor dengan nilai 330nF.

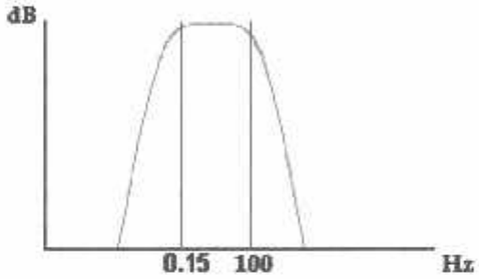


Gambar 3.9. Karakteristik LPF dengan Frekuensi *cutoff* 100 Hz.

Maka rangkaian *Band Pass Filter* (Seperti yang tampak pada **Gambar 3.10.** di bawah ini) akan didapat dengan frekuensi *cutoff* sesuai dengan frekuensi *cutoff* *Low Pass Filter* dan *High Pass Filter*.



Gambar 3.10. Rangkaian BPF dengan Frekuensi *cutoff* 0,15-100Hz

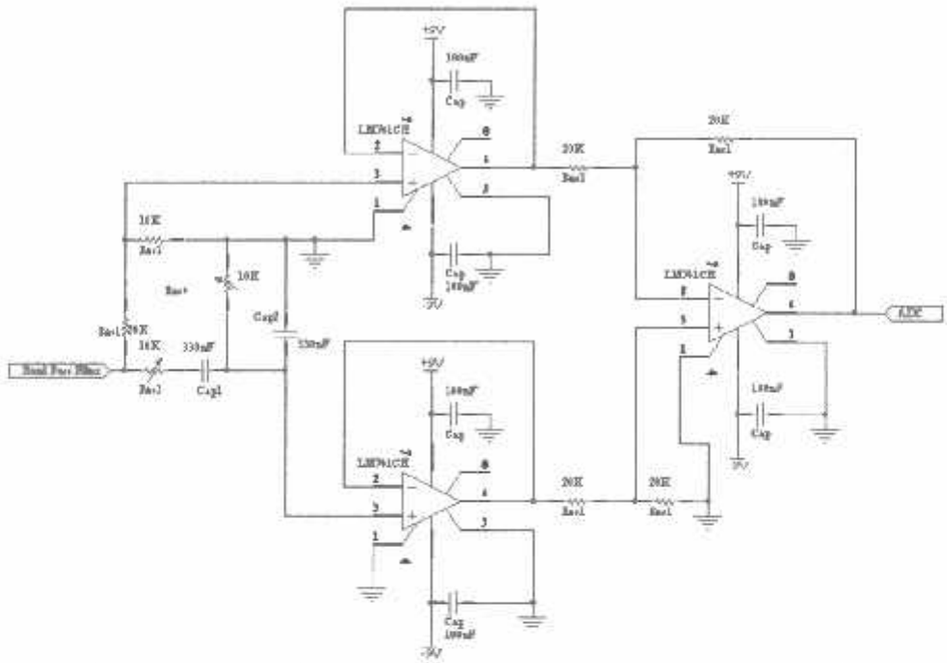


Gambar 3.11. Karakteristik BPF dengan Frekuensi 0,15-100Hz

3.1.4. BRF (*Band Reject Filter*)

Sering kali pada saat menguji suatu alat elektronik muncul sinyal yang tidak diinginkan yang berasal dari jala-jala listrik PLN dengan frekwensi 50Hz, schingga sinyal yang akan diukur bercampur dengan sinyal 50Hz. Meskipun sumber daya dari rangkaian elektronik yang digunakan menggunakan baterai namun interferensi frekwensi 50Hz ada di mana-mana tanpa kita sadari, terutama jika berdekatan dengan jala-jala listrik PLN. Rangkaian *Band Reject Filter* berfungsi untuk menekan noise dari frekwensi 50Hz yang berasal dari jala-jala

PLN tersebut. Adapun rangkaian dari *Band Reject Filter* hasil perancangan ditunjukkan pada gambar dibawah :



Gambar 3.12. Rangkaian *Band Reject Filter* dengan Frekuensi *cutoff* 50Hz[3]

Dengan perhitungan untuk frekuensi *null*-nya dapat dicari menggunakan rumus:

$$F_N = \frac{1}{2\pi R_3 C_1}$$

Dimana :

$R_3 = R_4$, $C_1 = C_2$, $R_2 = 0{,}5\ R_1$

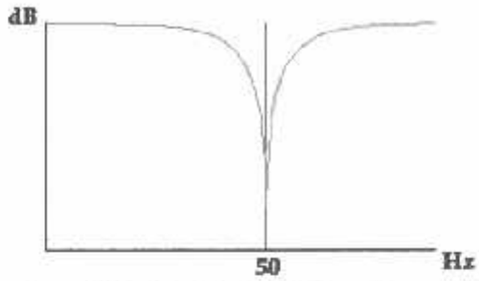
Untuk perhitungan Frekuensi *Null*-nya:

Digunakan R_3=R_4=9,65KΩ, dan digunakan C_1=C_2=330nF.

$$F_N = \frac{1}{2\pi R_1 C_1} = \frac{1}{6{,}28x9{,}65x10^{3}x330x10^{-9}}$$

$= 50{,}0033\text{Hz} \approx 50\text{Hz}$

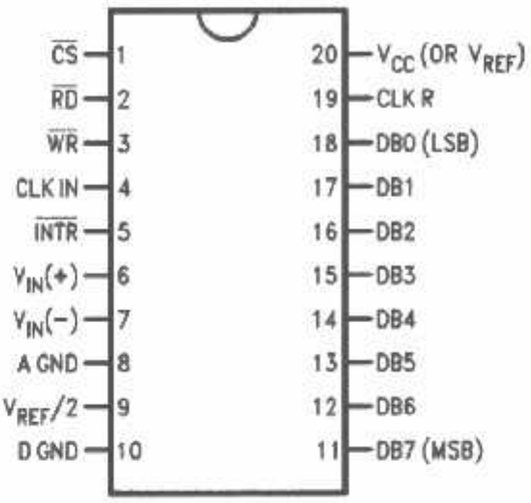
Maka akan didapatkan frekuensi *Null* dari *Band Reject Filter* pada 50Hz.



Gambar 3.13. Karakteristik *Band Reject Filter* dengan Frekuensi 50Hz.

3.1.5. ADC (*Analog to Digital Converter*)

Agar tegangan yang dikeluarkan oleh Rangkaian *Band Reject Filter* dapat dibaca dan ditampilkan oleh PC (*Personal Computer*), tegangan tersebut harus dirubah menjadi bentuk data digital. Untuk itu digunakan sebuah *Analog to Digital Converter* (ADC). ADC yang digunakan dalam perancangan ini adalah ADC0804 dari National SemiConductor (**Gambar 3.14**) yang merupakan ADC dengan 2 masukkan analog dan 8 bit keluaran digital. Dalam perancangan alat ini digunakan hanya satu buah inputan analog yaitu V_{IN+}, sedangkan input analog V_{IN-} tidak digunakan dan dihubungkan ke ground bersama pin lain yang tidak diperlukan pada ADC0804 National Semiconductor.



Gambar 3.14. Diagram Koneksi dari ADC 0804 National Semiconductor

Dikarenakan tegangan yang terukur cukup kecil maka tingkat resolusi ADC 0804 diharapkan cukup besar, jadi ADC 0804 National Semiconductor menggunakan VREF sebesar 5V, dimana tingkat resolusi ADC 0804 National Semiconductor ini adalah:

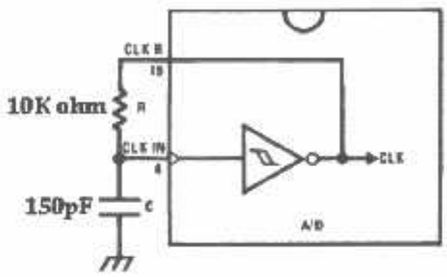
$$\text{Resolusi ADC} = \frac{V_{referensi}}{(2^n - 1)}, \text{ dimana n= banyaknya bit ADC.}$$

Jadi, besarnya resolusi ADC 8 bit adalah sebesar:

$$\text{Resolusi} = \frac{5}{(2^8 - 1)} = 0{,}0196\text{V} = 19{,}6\text{mV}.$$

Sehingga dengan perubahan inputan analog 19,6mV, maka output dari ADC akan mengalami perubahan sebesar 1 bit. Agar ADC0804 National Semiconductor dapat bekerja, maka perlu diberikan pembangkit pulsa. Rangkaian pembangkit pulsa diberikan dengan menambahkan rangkaian R dan C pada pin 19 dan pin 4

dari ADC. R yang digunakan bernilai 10K sedangkan C yang digunakan bernilai 150pF. Seperti yang tampak pada **Gambar 3.1.5** dibawah ini.



Gambar 3.15. Rangkaian Pembangkit Pulsa ADC 0804.

Sehingga Frekuensi pulsa yang diberikan adalah:

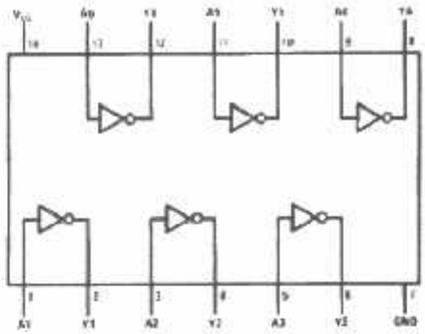
$$F = \frac{1}{1,1xRxC} = \frac{1}{1,x10x10^{3}x150x10^{-12}}$$

$$= 606060,6061\text{Hz} = 606,060\text{KHz}.$$

ADC 0804 National Semiconductor sendiri memiliki waktu konversi 100us.

3.1.6. *Inverter*

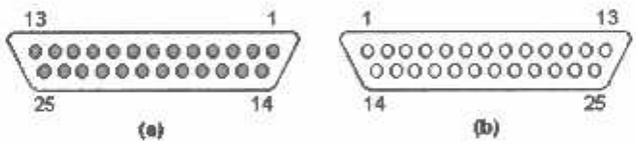
Seperti yang telah dijelaskan pada keterangan blok diagram perancangan alat ini, sebuah *inverter* (tampak pada **Gambar 3.16.** di bawah ini) digunakan untuk mencegah pertentangan kondisi *low* dan *high* input-an pada port DB-25.



Gambar 3.16. Konfigurasi pin pada *Inverter* DM74LS04

3.1.7. DB-25 *Parallel Port*

Hasil pengukuran sinyal ECG akan ditampilkan pada PC (*Personal Computer*), maka digunakan *Port Interface* DB-25 (**Gambar 3.17.** di bawah) sebagai jembatan antara keluaran *inverter* dan *PC*, sehingga data yang dikirimkan ke PC akan diproses dan ditampilkan.

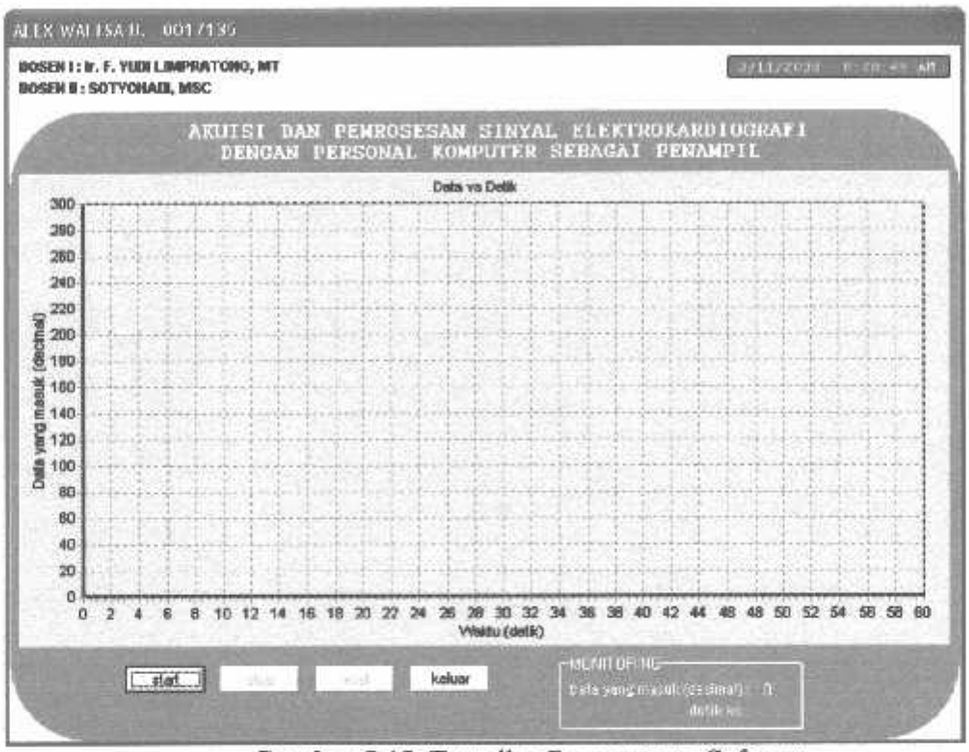


Gambar 3.17. Konfigurasi pin pada konektor DB-25.
(a) *Female* dan (b) *Male*

3.2. Perancangan *Software*.

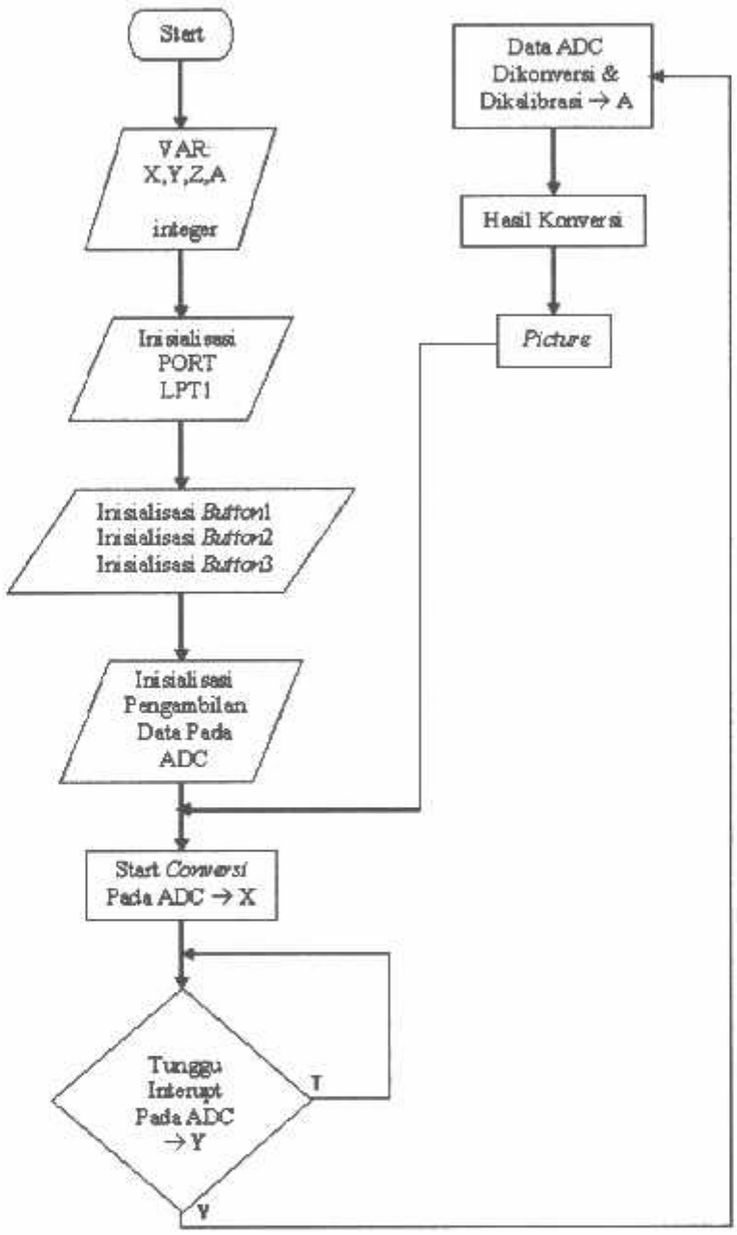
Agar sistem dapat bekerja sesuai dengan apa yang diharapkan, maka diperlukan suatu program yang akan mengolah data inputan sehingga dapat ditampilkan. Metode yang digunakan dalam pembuatan perangkat lunak ini didasarkan pada studi literatur dari buku-buku dan literatur Visual Basic. Program ditulis dengan menggunakan bahasa Pascal, untuk memudahkan perancangan

program. Setelah penulisan secara efisien, selanjutnya dievaluasi dan akan didapat tampilan seperti yang tampak pada **Gambar 3.18.** di bawah ini.



Gambar 3.18. Tampilan Perancangan *Software*

Jalannya program alat ini dapat dilihat dalam *flowchart* yang terdapat dibawah ini:



Gambar 3.19. Flowchart *Software*.

BAB IV

HASIL PENGUJIAN DAN ANALISA ALAT

Bab ini akan membahas pengujian dan analisa alat beserta piranti antarmuka yang telah dibuat. Pengujian meliputi Pengujian perangkat keras yaitu berupa blok-blok alat yang dibuat serta Pengujian perangkat lunak pendukungnya. Hasil pengujian kemudian dibandingkan dengan hasil perencanaan. Hasil perbandingan ini selanjutnya dianalisa.

4.1. Pengukuran Rangkaian Instrumentasi Amplifier

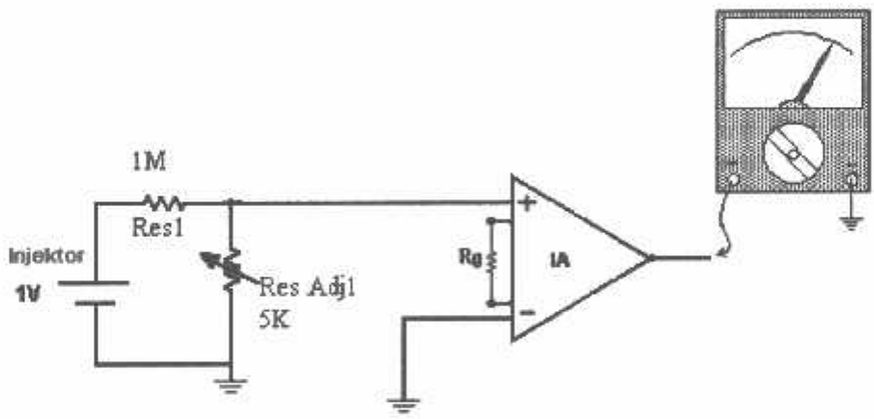
- Tujuan

Pengukuran ini bertujuan untuk mengetahui apakah rangkaian Instrumentasi Amplifier yang telah dirancang ini dapat bekerja dengan baik atau sebaliknya. Pengukuran penguat instrumentasi ini meliputi pengukuran *diffrential mode* (DM) dan pengukuran *common mode* (CM) serta mengetahui besarnya *common mode rejection ratio* (CMRR) tegangan yang tertera pada multimeter.

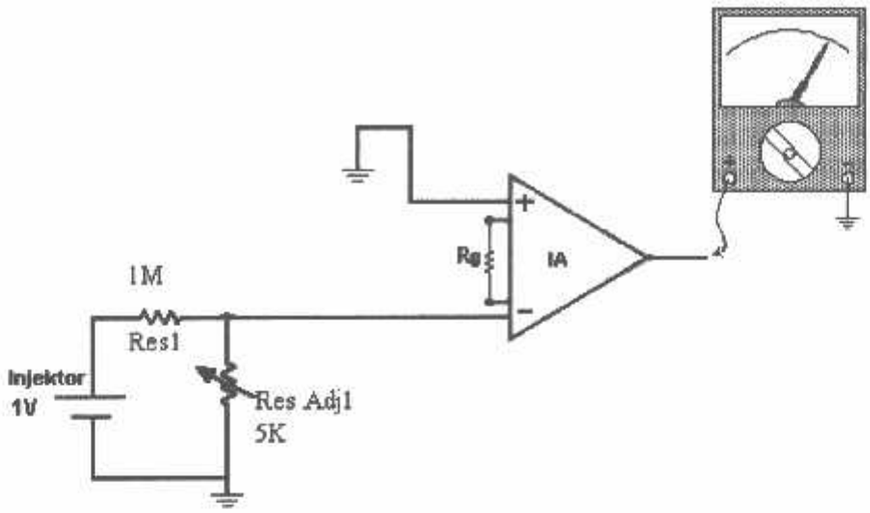
- Peralatan yang digunakan:
  1. Power supply.
  2. Fungsi Generator.
  3. Osciloskop.
  4. Alat ukur AVO meter.

- Prosedur pengukuran

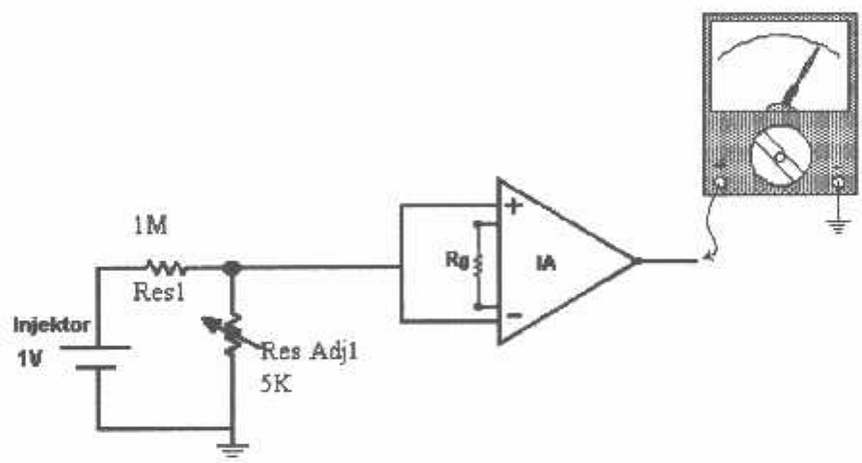
1. Merangkai peralatan seperti **Gambar 4.1.-Gambar 4.4.**
2. Memberikan inputan dari Fungsi Generator
3. Menghubungkan output-an rangkaian Instrumentasi Amplifier dengan osciloskop.
4. Mengamati secara bersamaan bentuk gelombang sinus pada input-an dan output-an.
5. Mengukur hasil output-an rangkaian Instrumentasi Amplifier menggunakan alat ukur AVO meter, mengamati dan mencatat hasil output-an rangkaian Instrumentasi Amplifier yang tertera pada alat ukur AVO meter.



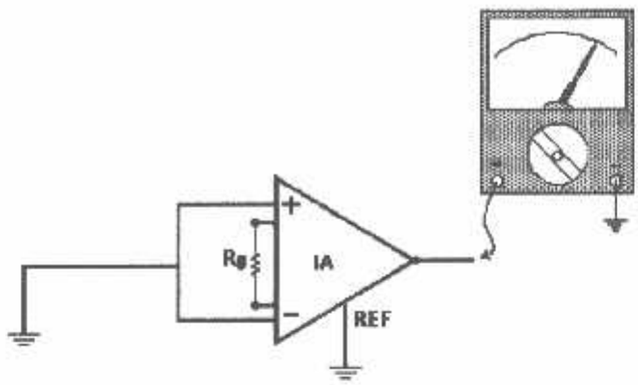
Gambar 4.1. Rangkaian Pengukuran *Differential Mode* (DM) Penguat Instrumentasi dengan masukkan (-) dihubungkan dengan *ground.*



Gambar 4.2. Rangkaian Pengukuran *Differential Mode* (DM) Penguat Instrumentasi dengan masukkan (+) dihubungkan dengan *ground.*



Gambar 4.3. Rangkaian Pengukuran *Common Mode Voltage* (CMV) Instrumentasi Amplifier



Gambar 4.4. Rangkaian Pengukuran *Common Mode* (CM) Instrumentasi Amplifier dengan 2 masukkan terground (0V)

Tabel 4.1. Hasil Pengukuran dan Pengujian Instrumentasi Amplifier

V1 (-) mV	V2 (+) mV	GAIN (kali)	Vout	
			Perhitungan (mV)	Pengukuran (mV)
1	0	20	20	-20,6
2	0	20	40	-40,8
3	0	20	60	-60,3
4	0	20	80	-80,5
5	0	20	100	-100,4
0	1	20	20	19,9
0	2	20	40	39,9
0	3	20	60	60,2
0	4	20	80	79,7
0	5	20	100	99,8

Tanda min (-) berarti Inversi.

- Perhitungan tegangan keluaran *differensial mode* :

$$Vout = (V2 - V1)\,\text{Gain}$$

Schingga dari data pengukuran di atas dapat dihitung Vout-nya dengan perhitungan berikut :

* Untuk $V_1 = 1mV$, $V_2 = 0V$

$$Vout = (0V - 1mV) \times 20$$
$$= -20mV$$

* Untuk $V_1 = 2mV$, $V_2 = 0V$

$$Vout = (0V - 2mV) \times 20$$
$$= -40mV$$

* Untuk $V_1 = 3mV$, $V_2 = 0V$

$$Vout = (0V - 4mV) \times 20$$
$$= -60mV$$

* Untuk $V_1 = 4mV$, $V_2 = 0V$

$$Vout = (0V - 4mV) \times 20$$
$$= -80mV$$

*Untuk $V_1 = 5V$, $V_2 = 0mV$

$$Vout = (0V - 5mV) \times 20$$
$$= -100mV$$

- Perhitungan tegangan keluaran *common mode*

* Untuk $V_1 = 0V$, $V_2 = 0V$

$$Vout = (0V - 0V) \times 20$$
$$= 0V$$

- Pengukuran tegangan keluaran *common mode*

* Untuk $V_1 = 0V$, $V_2 = 0V \rightarrow V_{out} = 0,00015V$

$$= 0,15mV$$

- Perhitungan prosentase *error* dalam pengujian dan pengukuran dihitung dengan rumus :

$$\%\ Error = \frac{Vout\ \text{pengukuran} - Vout\ \text{perhitungan}}{Vout\ \text{pengukuran}} \times 100\%$$

Sehingga dari data pengukuran di atas didapatkan besar *error* dengan perhitungan berikut :

* Untuk $-V_1 = 1mV$, $+V_2 = 0V$

$$\%\ Error = \frac{20{,}6mV - 20mV}{20{,}6mV} \times 100\%$$
$$= 2{,}9\%$$

* Untuk $-V_1 = 2mV$, $+V_2 = 0V$

$$\%\ Error = \frac{40{,}8mV - 40mV}{40{,}8mV} \times 100\%$$
$$= 1{,}96\%$$

* Untuk $-V_1 = 3mV$, $+V_2 = 0V$

$$\%\ Error = \frac{60{,}3mV - 60mV}{60{,}3mV} \times 100\%$$
$$= 0{,}49\%$$

* Untuk $-V_1 = 4mV, +V_2 = 0V$

$$\%\ Error = \frac{80,5mV - 80mV}{80,5mV} \times 100\%$$
$$= 0,62\%$$

* Untuk $-V_1 = 5mV, +V_2 = 0V$

$$\%\ Error = \frac{100,4mV - 100mV}{100,4mV} \times 100\%$$
$$= 0,39\%$$

* Untuk $-V_1 = 0V, +V_2 = 1mV$

$$\%\ Error = \frac{19,9mV - 20mV}{19,9mV} \times 100\%$$
$$= 0,5\%$$

* Untuk $-V_1 = 0V, +V_2 = 2mV$

$$\%\ Error = \frac{39,9mV - 40mV}{39,9mV} \times 100\%$$
$$= 0,25\%$$

* Untuk $-V_1 = 0V, +V_2 = 3mV$

$$\%\ Error = \frac{60,2mV - 60mV}{60,2mV} \times 100\%$$
$$= 0,33\%$$

* Untuk $-V_1 = 0V, +V_2 = 4mV$

$$\%\ Error = \frac{79{,}7mV - 80mV}{79{,}7mV} \times 100\%$$
$$= 0{,}37\%$$

* Untuk $-V_1 = 0V, +V_2 = 5mV$

$$\%\ Error = \frac{99{,}8mV - 100mV}{99{,}8mV} \times 100\%$$
$$= 0{,}2\%$$

- Perhitungan *Common Mode Rejection Ratio* (CMRR)

  Pengukuran *Common Mode Rejection Ratio* (CMRR) bertujuan untuk mengetahui seberapa baik penguat instrumentasi me-*reject* suatu *common mode signal.* Perhitungan CMRR dapat dirumuskan dengan rumus berikut :

$$CMRR = 20\ Log\ \frac{Ad}{Common\ Mode\ /\ Differential\ Mode}\ dB$$

Sehingga dari data pengukuran diatas maka dapat dihitung besar CMRR dengan perhitungan berikut :

* Untuk $-V_1 = 1mV, +V_2 = 0V$

$$CMRR = 20\ Log\ \frac{20}{0{,}15/20{,}6}\ dB$$
$$= 68{,}77dB$$

* Untuk $-V_1 = 2mV, +V_2 = 0V$

$$CMRR = 20\ Log\ \frac{20}{0,15/40,8}\ dB$$
$$= 74,71\,dB$$

* Untuk $-V_1 = 3mV, +V_2 = 0V$

$$CMRR = 20\ Log\ \frac{20}{0,15/60,3}\ dB$$
$$= 78,1\,dB$$

* Untuk $-V_1 = 4mV, +V_2 = 0V$

$$CMRR = 20\ Log\ \frac{20}{0,15/80,5}\ dB$$
$$= 80,61\,dB$$

* Untuk $-V_1 = 5mV, +V_2 = 0V$

$$CMRR = 20\ Log\ \frac{20}{0,15/100,4}\ dB$$
$$= 82,53\,dB$$

* Untuk $-V_1 = 0V, +V_2 = 1mV$

$$CMRR = 20\ Log\ \frac{20}{0,15/19,9}\ dB$$
$$= 68,47\,dB$$

* Untuk $-V_1 = 0V, +V_2 = 2mV$

$$CMRR = 20\ Log\ \frac{20}{0,15/39,9}\ dB$$
$$= 74,51\,dB$$

* Untuk $-V_1 = 0V$, $+V_2 = 3mV$

$$CMRR = 20\ Log\ \frac{20}{0{,}15 / 60{,}2}\ dB$$
$$= 78{,}09\ dB$$

* Untuk $-V_1 = 0V$, $+V_2 = 4mV$

$$CMRR = 20\ Log\ \frac{20}{0{,}15 / 79{,}7}\ dB$$
$$= 80{,}52\ dB$$

* Untuk $-V_1 = 0V$, $+V_2 = 5mV$

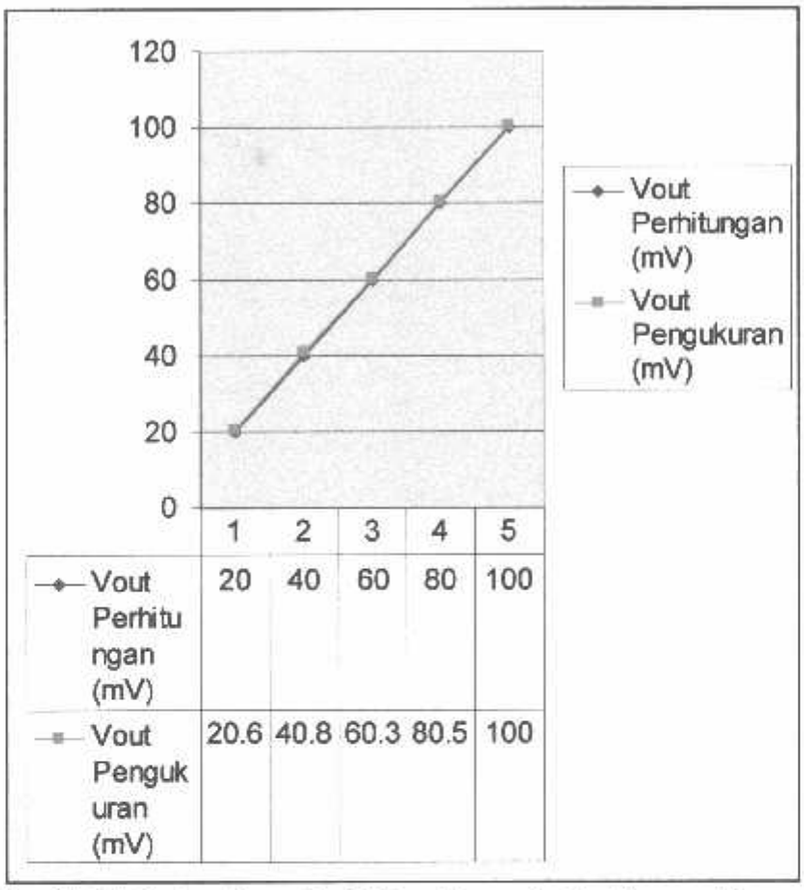
$$CMRR = 20\ Log\ \frac{20}{0{,}15 / 99{,}8}\ dB$$
$$= 82{,}48dB$$

Untuk selanjutnya, dari perhitungan diatas maka dapat dibuat tabel hasil perhitungan seperti berikut :

Tabel 4.2. Hasil Pengujian dan perhitungan

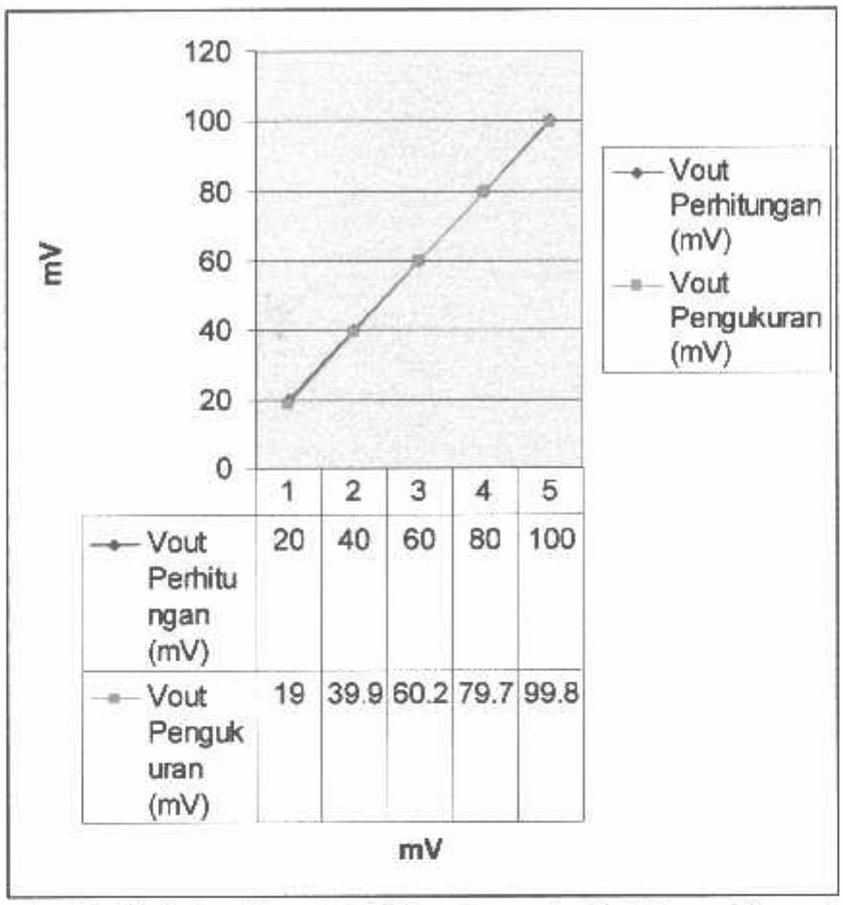
$-V_1$ (mV)	$+V_2$ (mV)	GAIN (kali)	Vout Perhitungan (mV)	Vout Pengukuran (mV)	Error (%)	CMRR (dB)
1	0	20	20	-20,6	2.9	68.77
2	0	20	40	-40,8	1.96	74.71
3	0	20	60	-60,3	0.49	78.1
4	0	20	80	-80,5	0.62	80.61
5	0	20	100	-100,4	0.39	82.53
0	1	20	20	19,9	0.5	68.47
0	2	20	40	39,9	0.25	74.51
0	3	20	60	60,2	0.33	78.09
0	4	20	80	79,7	0.37	80.52
0	5	20	100	99,8	0.2	82.48

0	0	1000	0	0.15	-	-
		Rata-rata	60	60.21	0.762	76.879



	1	2	3	4	5
Vout Perhitungan (mV)	20	40	60	80	100
Vout Pengukuran (mV)	20.6	40.8	60.3	80.5	100

Grafik 4.1. Perbandingan Hasil Pengukuran dan Perhitungan Penguat Instrumentasi Untuk $V_1=V_{IN}$, $V_2=0$



Grafik 4.2. Perbandingan Hasil Pengukuran dan Perhitungan Penguat Instrumentasi Untuk $V_1=0$, $V_2= V_{IN}$

4.2. Pengujian Rangkaian *Band Pass Filter*

- Tujuan

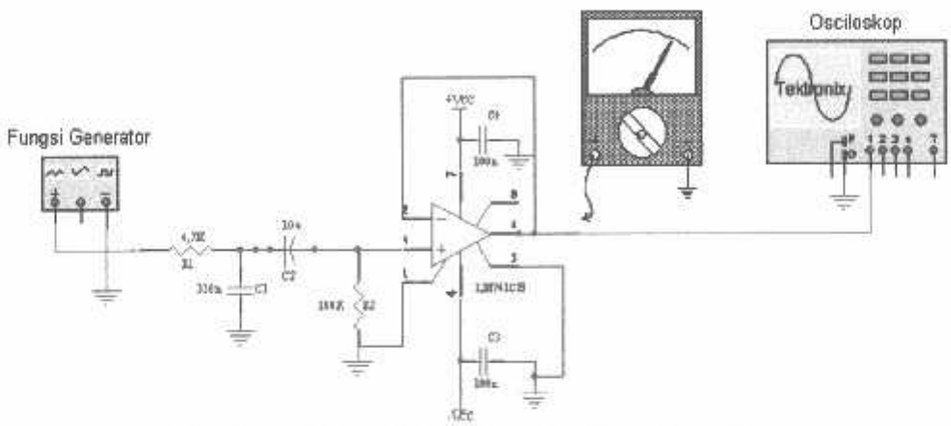
  Tujuan dari pengujian rangkaian Band-pass filter adalah untuk mengetahui hasil dari pernguatan sinyal yang dihasilkan

- Peralatan yang digunakan

  1. Power supply
  2. Generator fungsi
  3. Osciloscope.

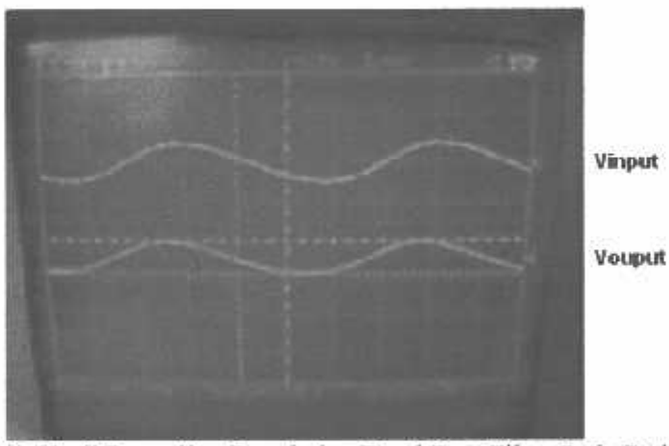
- Prosedur Pengujian

1. Rangkaian dibuat seperti pada **Gambar 4.5.**
2. Mengamati hasil keluaran pada band-pass filter

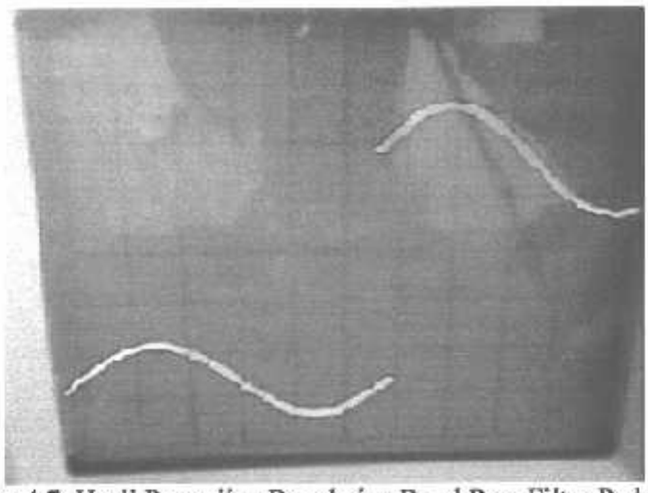


Gambar 4.5. Rangkaian Pengujian *Band Pass Filter*

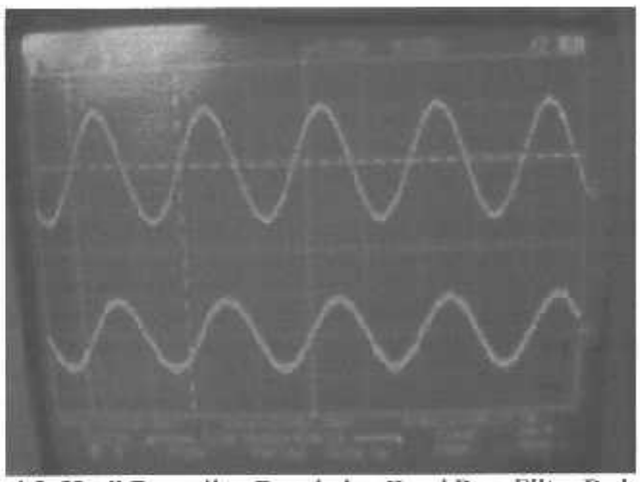
- Hasil Pengujian



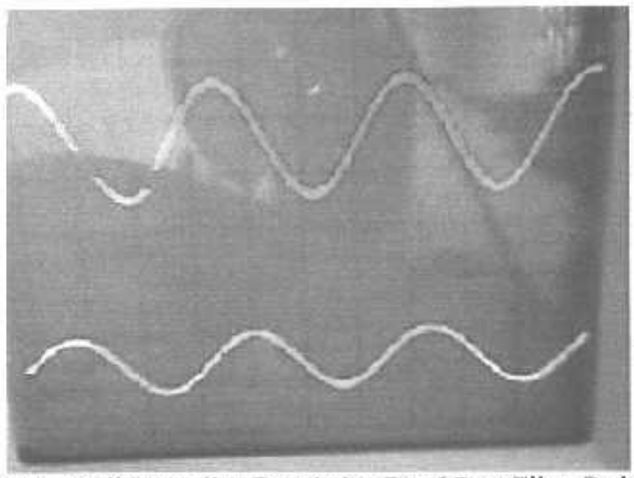
Gambar 4.6. Hasil Pengujian Rangkaian Band Pass Filter Pada Frekuensi 0,2Hz Dengan V/Div=2V dan T/Div=2s.



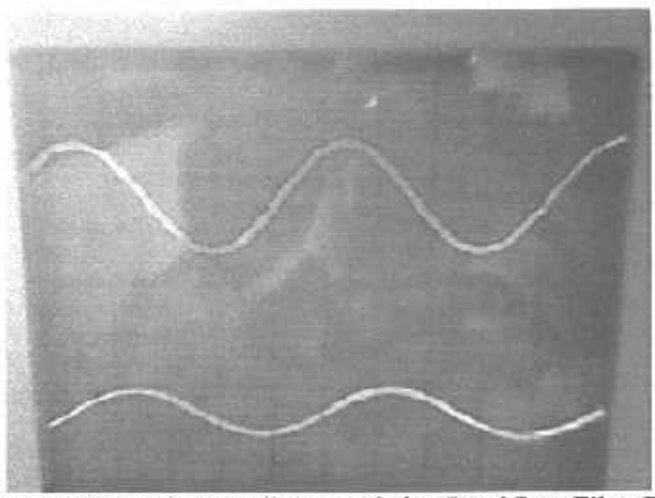
Gambar 4.7. Hasil Pengujian Rangkaian Band Pass Filter Pada Frekuensi 80Hz Dengan V/Div=500mV dan T/Div=2ms.



Gambar 4.8. Hasil Pengujian Rangkaian Band Pass Filter Pada Frekuensi 100Hz Dengan V/Div=50mV dan T/Div=2ms.



Gambar 4.9. Hasil Pengujian Rangkaian Band Pass Filter Pada Frekuensi 150Hz Dengan V/Div=500mV dan T/Div=2ms.

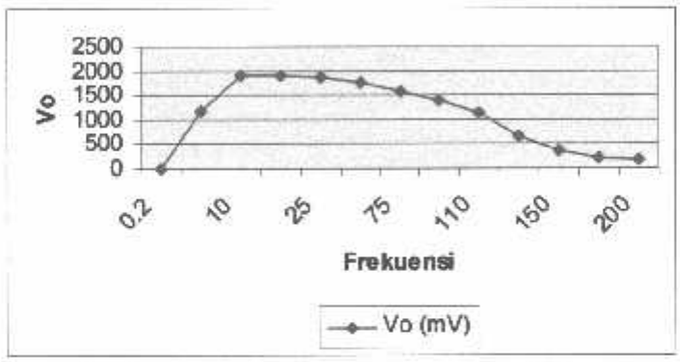


Gambar 4.10. Hasil Pengujian Rangkaian Band Pass Filter Pada Frekuensi 200Hz Dengan V/Div=500mV dan T/Div=1ms.

Dengan melakukan langkah-langkah pengukuran di atas, maka didapat hasil pengujian pada **Tabel 4.3.** di bawah ini.

Tabel 4.3. Hasil Pengujian Rangkaian Band Pass Filter

f (Hz)	Vi (mV)	Vo (mV)
0.2	19.2	17.4
1	1100	1190
10	2000	1930
15	2000	1920
25	2000	1890
50	2000	1750
75	2000	1580
100	2000	1410
110	2000	1140
125	2000	674
150	2000	381
175	2000	215
200	2000	169



Grafik 4.3. Hasil Pengujian Rangkaian *Band Pass Filter*

4.3. Pengujian Rangkaian *Band Reject Filter*

- Tujuan

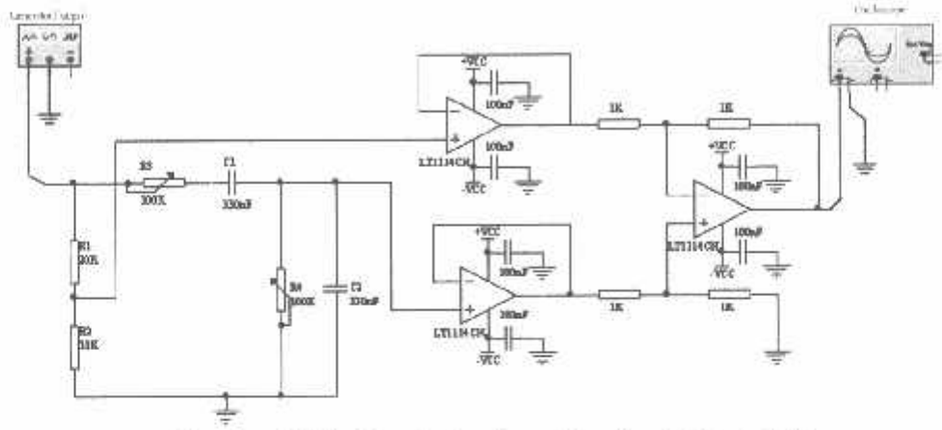
  Tujuan dari pengujian rangkaian *Band reject filterr* adalah mengetahui apakah dapat menekan frekwensi 50Hz

- Peralatan yang digunakan

  1. *Power supply*
  2. Generator fungsi
  3. *Osciloscope*

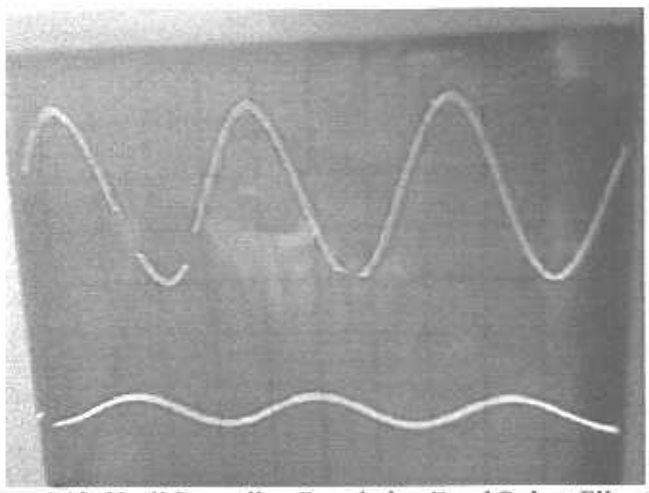
- Prosedur Pengujian

  1. Rangkaian dibuat seperti pada **Gambar 4-11.**
  2. Mengamati hasil keluaran pada *band reject filter*

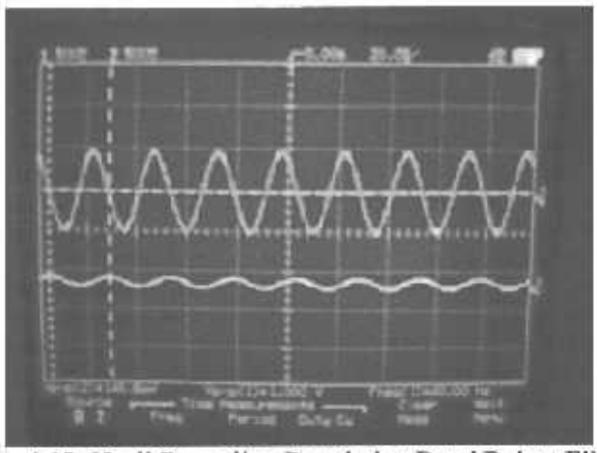


Gambar 4-11. Rangkaian Pengujian *Band Reject Filter*

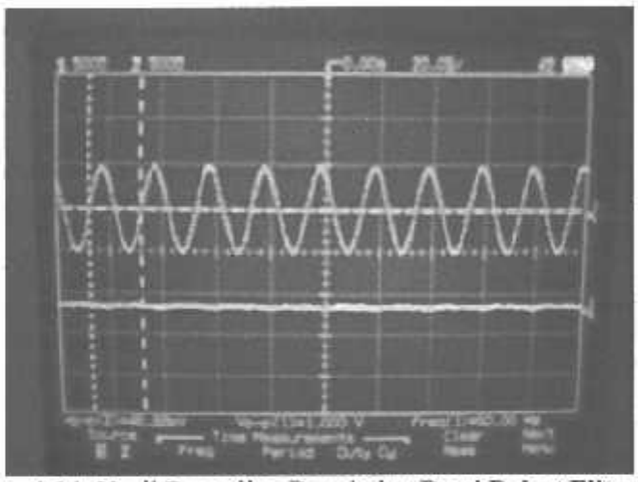
- Hasil pengujian



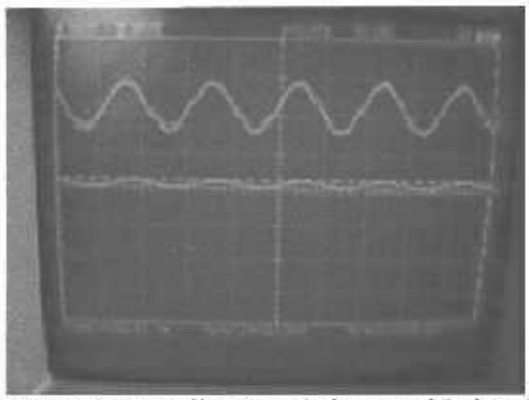
Gambar 4.12. Hasil Pengujian Rangkaian Band Reject Filter Pada Frekuensi 20Hz Dengan V/Div=200mV dan T/Div=2ms.



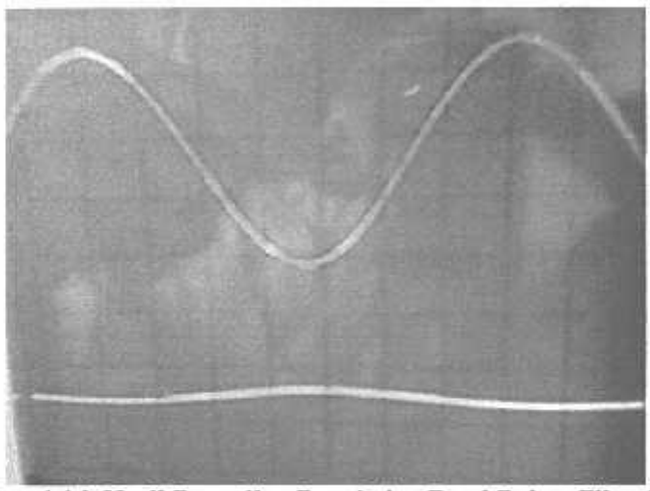
Gambar 4.13. Hasil Pengujian Rangkaian Band Reject Filter Pada Frekuensi 40Hz Dengan V/Div=500mV dan T/Div=20ms.



Gambar 4.14. Hasil Pengujian Rangkaian Band Reject Filter Pada Frekuensi 50Hz Dengan V/Div=500mV dan T/Div=20ms.



Gambar 4.15. Hasil Pengujian Rangkaian Band Reject Filter Pada Frekuensi 60Hz dengan V/Div=1v dan T/Div=2s.



Gambar 4.16. Hasil Pengujian Rangkaian Band Reject Filter Pada Frekuensi 80Hz Dengan V/Div=200V dan T/Div=1ms.

Hasil pengujian rangkaian *band reject filter* ditunjukkan tabel dibawah :

Tabel 4-4. Hasil Pengukuran *Band Reject Filter*

Frekwensi (Hz)	Vin (V)	Vout (V)	V/Div (V)	T/Div (ms)
40	2	0.0982	1	5
42	2	0.0767	1	5
45	2	0.0561	1	5
46	2	0.0461	1	5
48	2	0.0363	1	5
50	2	0.0174	1	5
52	2	0.000656	1	5

BAB V

PENUTUP

5.1. Kesimpulan

1. Jika diuji per blok rangkaian, alat ini dapat bekerja dengan baik. Namun apabila disatukan dan diberikan input dari elektroda, maka masih terdapat noise.

5.2. Kesulitan

1. Kesulitan pada perancangan alat ini adalah susahnya menekan interferensi 50 Hz dari jaringan PLN, dan adanya interferensi gelombang dari barang-barang elektronik.
2. Pada inputan terdapat kelemahan yaitu sangat sensitif nya elektroda yang digunakan.

5.3. Saran

1. Amplifier ini dapat dikembangkan menjadi ECG amplifier untuk pengukuran multi-channel dengan system 12 lead.
2. Untuk hasil ECG yang paling akurat dan paling dapat diandalkan, pemilihan bagian yang akan diukur dan persiapan dari bagian yang akan diukur haruslah lebih baik. Di mana dan bagaimana elektroda dipasangkan memberikan pengaruh sangat besar pada sensitifitas pengukuran ECG.

Daftar Pustaka

1. Lecture 6: Integrated Electronics Biopotensial Measurement, Kartik. http://engineering.rowan.edu/~polikar/CLASSES/ECE404
2. Princples of Biomedical Systems & Devices: Lab I electrocardiogram. [enrique.combos@analog.com] [eckart.hartmann@analog.com]
3. Ashton, Richard, Principles of Biomedical Instrumentation and Measurement, New York: Pennsylvania State University.
4. Sugiharto, Agus, 2002, Penerapan Dasar Tansducer dan Sensor, Yogyakarta: Penerbit Kanisius (Anggota IKAPI).
5. Princple of Biomedical Systems & Devices: Lecture 6 Biopotensial Electrode. http://engineering.rowan.edu/~polikar/CLASSES/ECE404
6. Robert F. Coughlin and Frederick F. Driscoll, 1983, Penguat Operasional dan Rangkaian Terpadu linear.
7. Eko Putra, Agfianto, 2002, Penapis Aktif Elektronika Teori dan Praktek, Yogyakarta, C.V. Gava Media.
8. B. Brey, Barry, 2000, Mikroprosesor Intel 8086/8088, 80156/80188, 80286, 80386, 80486, *Pentium, dan Pentium-Pro:* Arsitektur, Pemrograman, Antarmuka, Jakarta, Erlangga.
9. PC BASED ECG MONITORING SYSTEM tianwei@natriumtech.com, fohc@starhub.net.sg
10. Interfacing the Standard Parallel Port http://www.senet.com.au/~cpeacock.
11. Craig Peacock's Interfacing the PC. http://www.senet.com.au/~cpeacock
12. AD620 Datasheet, www.datasheetcatalog.com

13. *CA741, CA741C, CA1458, CA1558,LM741, LM741C, LM1458 Datasheet.* www.intersil.com

14. 54LS04/DM54LS04/DM74LS04 Hex Inverting Gates Datasheet, www.datasheetcatalog.com

15. ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit µP Compatible A/D Converters. www.national.com

16. Laboratory 1: Design of an EKG PREAmplifier University of Washington Electrical Engineering

LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL
JL. RAYA KARANGLO, KM 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Alex Walesa B

NIM : 00.17.135

Masa Bimbingan : 06 September 07 s/d 06 Maret 08

Judul skripsi : Akuisisi Dan Pemrosesan Sinyal Elektrokardiografi (EKG) Yang Ditampilkan Pada PC (*Personal Computer*)

No	Tanggal	Uraian	Paraf Pembimbing
1.	19-05-07	KONSULTASI BAB I & II	Jadi
2.	06-03-08	PENGUKURAN ALAT	Jadi
3.	10-03-08	KONSULTASI BAB III & IV	Jadi
4.	17-03-08	ACC BAB I, II, III, IV, V	Jadi
5.			
6.			
7.			
8.			
9.			
10.			

Malang,

Dosen Pembimbing II

Sotyohadi Msc.

NIP.Y :

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Alex Wolter
N I M : 00.17.135
Perbaikan meliputi :

(1) Gambar diagram blok lebih jelas lengkapi dg fungsi dan masing² blok & alasan kenapa diperlukan.

(2) untuk diagram blok [illegible] blk [illegible] 29, bukankah kedua itu adalah [illegible] blk.

(3) Jelaskan fungsi dan masing² blok dan penjelasan anda / di diagram blok, kenapa [illegible] ada blk ?

Malang,

(________________)

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura-gura No. 2
MALANG

FORMULIR PERBAIKAN SKRIPSI

Nama : Alex Walesa Butarbutar

Nim : 0017135

Masa Bimbingan : 06 September 2007 s/d 06 Maret 2008

Judul Skripsi : Perancangan dan Pembuatan Alat Peng-Akuisisi dan Pemrosesan Sinyal Elektrokardiografi Dengan *Personal Computer* (PC) Sebagai Penampil.

No	Tanggal	Uraian	Paraf
1.	17–03–2008	Gambar diagram blok lebih jelas, lengkapi dengan fungsi dari masing-masing blok dan alasan kenapa diperlukan.	
2.	17–03–2008	Untuk diagram *High Pass Filter* hal. 39, buktikan kalau itu adalah High Pass Filter.	
3.	17–03–2008	Jelaskan fungsi dari masing-masing filter di rangkaian anda/di diagram blok, kenapa harus ada filter?	

Disetujui:
Penguji I

(DR. Cahyo Crysdian, Msc.)
NIP.Y. 103040412

Mengetahui:

Dosen Pembimbing I

(Ir. F. Yudi Limpraptono, MT)
NIP.Y. 1039500274

Dosen Pembimbing II

(Sotyohadi, ST)
NIP.

INSTITUT TEKNOLOGI NASIONAL
Jl. Bendungan Sigura-gura No. 2
MALANG

FORMULIR PERBAIKAN SKRIPSI

Nama : Alex Walesa Butarbutar

Nim : 0017135

Masa Bimbingan : 06 September 2007 s/d 06 Maret 2008

Judul Skripsi : Perancangan Dan Pembuatan Alat Peng-Akuisisi Dan Pemrosesan Sinyal Elektrokardiografi (EKG) Dengan Personal Computer (PC) Sebagai Penampil.

No	Tanggal	Uraian	Paraf
1.	17 – 03 – 2008	Foto Pengujian-pengujian	

Disetujui

Penguji II

(Ir. Yoseph Dedy Irawan, MT.)
NIP. 132315178

Mengetahui

Dosen Pembimbing I

(Ir. F. Yudi Limpraptono, MT.)
NIP.Y. 1039500274

Dosen Pembimbing II

(Sotyohadi, ST.)
NIP.

```
object fdata: Tfdata
  Left = 269
  Top = 103
  AutoScroll = False
  BorderIcons = []
  Caption = ' >> Data Log'
  ClientHeight = 363
  ClientWidth = 305
  Color = clBtnFace
  Font.Charset = DEFAULT_CHARSET
  Font.Color = clWindowText
  Font.Height = -11
  Font.Name = 'MS Sans Serif'
  Font.Style = []
  OldCreateOrder = False
  Position = poDesktopCenter
  OnShow = FormShow
  PixelsPerInch = 96
  TextHeight = 13
  object bthapus: TspSkinButton
    Left = 16
    Top = 320
    Width = 75
    Height = 25
    TabOrder = 0
    DrawDefault = True
    SkinData = Form1.spSkinData1
    SkinDataName = 'button'
    AlphaBlend = False
    AlphaBlendValue = 200
    UseSkinCursor = False
    DefaultFont.Charset = DEFAULT_CHARSET
    DefaultFont.Color = clWindowText
    DefaultFont.Height = 14
    DefaultFont.Name = 'Arial'
    DefaultFont.Style = []
    UseSkinFont = True
    DefaultWidth = 0
    DefaultHeight = 0
    RepeatMode = False
    RepeatInterval = 100
    AllowAllUp = False
    TabStop = True
    CanFocused = True
    Down = False
    GroupIndex = 0
```

```
  Caption = '&Hapus'
  Glyph.Data = {
4E010000424D4E010000000000007600000028000000120000001200000001000
400000000000D800000000000000000000000100000000000000000000000000000
C00000C0000000C0C000C0000000C000C000C0C00000C0C0C0008080800000
00
FF0000FF000000FFFF00FF000000FF00FF00FFFF0000FFFFFF0077777777FB
FB
FB777700000077777777777BFB777770000007777777777BF777770000007777
777777BFB077770000007777777777FBFB077700000077777777777B7B770770
0
0000777777777F777707770000007777777777777077770000007777777770777
07777700000077777770C000777777000000777777C0777777777000000077777
70C07777777777000000777770C077777777777000000777C077777777777700
0000770C077777777777777000000778077777777777777000000777777777777
  77777700000077777777777777777777000000}
  NumGlyphs = 1
  Spacing = 5
  Enabled = False
  OnClick = bthapusClick
 end
 object bttutup: TspSkinButton
  Left = 216
  Top = 320
  Width = 75
  Height = 25
  TabOrder = 1
  DrawDefault = True
  SkinData = Form1.spSkinData1
  SkinDataName = 'button'
  AlphaBlend = False
  AlphaBlendValue = 200
  UseSkinCursor = False
  DefaultFont.Charset = DEFAULT_CHARSET
  DefaultFont.Color = clWindowText
  DefaultFont.Height = 14
```

```
  DefaultFont.Name = 'Arial'
  DefaultFont.Style = []
  UseSkinFont = True
  DefaultWidth = 0
  DefaultHeight = 0
  RepeatMode = False
  RepeatInterval = 100
  AllowAllUp = False
  TabStop = True
  CanFocused = True
  Down = False
  GroupIndex = 0
  Caption = '&Tutup'
  Glyph.Data = {

4E010000424D4E010000000000007600000028000000120000001200000001 00

040000000000D800000000000000000000000010000000000000000000000000000000

C00000C0000000C0C000C0000000C000C000C0C00000C0C0C0008080800000
00

FF0000FF000000FFFF00FF000000FF00FF00FFFF0000FFFFFF0077777777777
7

7777770000007777777777777777770000007777777777777777770000007777

7887777777777700000077777008777777777700000077777090777778077700

0000777770907777780777000000777770908777908777000000777777700877

9077770000007777777890900777770000007777777790907777770000007777

7890909087777700000077777890909087777700000077779090879008777700

0000777777777777908777000000777777777777700887000000777777777777
    77777700000077777777777777777777000000}
  NumGlyphs = 1
  Spacing = 5
  OnClick = bttutupClick
 end
 object DBGrid1: TDBGrid
  Left = 16
  Top = 24
  Width = 273
  Height = 289
```

```
    Color = cl3DDkShadow
    DataSource = DataSource1
    FixedColor = clInactiveCaption
    Font.Charset = DEFAULT_CHARSET
    Font.Color = clYellow
    Font.Height = -11
    Font.Name = 'MS Sans Serif'
    Font.Style = []
    Options = [dgTitles, dgIndicator, dgColLines, dgRowLines, dgTabs,
dgConfirmDelete, dgCancelOnExit]
    ParentFont = False
    TabOrder = 2
    TitleFont.Charset = DEFAULT_CHARSET
    TitleFont.Color = clWindowText
    TitleFont.Height = -11
    TitleFont.Name = 'MS Sans Serif'
    TitleFont.Style = []
    Columns = <
     item
       Expanded = False
       FieldName = 'tgl'
       Title.Alignment = taCenter
       Title.Caption = 'Tanggal'
       Width = 75
       Visible = True
     end
     item
       Expanded = False
       FieldName = 'waktu'
       Title.Alignment = taCenter
       Title.Caption = 'Jam'
       Width = 70
       Visible = True
     end
     item
       Expanded = False
       FieldName = 'tinggi'
       Title.Alignment = taCenter
       Title.Caption = 'Ketinggian (m)'
       Width = 84
       Visible = True
     end>
  end
  object spDynamicSkinForm1: TspDynamicSkinForm
    UseFormCursorInNCArea = False
    MaxMenuItemsInWindow = 0
```

```
ClientWidth = 0
ClientHeight = 0
HideCaptionButtons = False
AlwaysShowInTray = False
LogoBitMapTransparent = False
AlwaysMinimizeToTray = False
UseSkinFontInMenu = True
ShowIcon = False
MaximizeOnFullScreen = False
ShowObjectHint = False
UseDefaultObjectHint = True
UseSkinCursors = False
DefCaptionFont.Charset = DEFAULT_CHARSET
DefCaptionFont.Color = clBtnText
DefCaptionFont.Height = 14
DefCaptionFont.Name = 'Arial'
DefCaptionFont.Style = [fsBold]
DefInActiveCaptionFont.Charset = DEFAULT_CHARSET
DefInActiveCaptionFont.Color = clBtnShadow
DefInActiveCaptionFont.Height = 14
DefInActiveCaptionFont.Name = 'Arial'
DefInActiveCaptionFont.Style = [fsBold]
DefMenuItemHeight = 20
DefMenuItemFont.Charset = DEFAULT_CHARSET
DefMenuItemFont.Color = clWindowText
DefMenuItemFont.Height = 14
DefMenuItemFont.Name = 'Arial'
DefMenuItemFont.Style = []
UseDefaultSysMenu = True
SupportNCArea = True
AlphaBlendAnimation = False
AlphaBlendValue = 200
AlphaBlend = False
MenusAlphaBlend = False
MenusAlphaBlendAnimation = False
MenusAlphaBlendValue = 200
SkinData = Form1.spSkinData1
MenusSkinData = Form1.spSkinData1
MinHeight = 0
MinWidth = 0
MaxHeight = 0
MaxWidth = 0
Sizeable = False
DraggAble = True
Magnetic = False
MagneticSize = 10
```

```
  BorderIcons = [biSystemMenu, biRollUp]
  Left = 200
  Top = 160
 end
 object DataSource1: TDataSource
  DataSet = Form1.Table1
  Left = 88
  Top = 280
 end
end
```

Low Cost, Low Power Instrumentation Amplifier

AD620

FEATURES

EASY TO USE
- Gain Set with One External Resistor (Gain Range 1 to 1000)
- Wide Power Supply Range (±2.3 V to ±18 V)
- Higher Performance than Three Op Amp IA Designs
- Available in 8-Lead DIP and SOIC Packaging
- Low Power, 1.3 mA max Supply Current

EXCELLENT DC PERFORMANCE ("B GRADE")
- 50 μV max, Input Offset Voltage
- 0.6 μV/°C max, Input Offset Drift
- 1.0 nA max, Input Bias Current
- 100 dB min Common-Mode Rejection Ratio (G = 10)

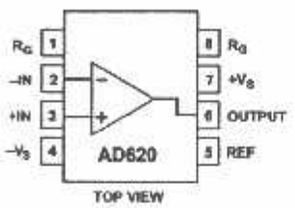
LOW NOISE
- 9 nV/√Hz, @ 1 kHz, Input Voltage Noise
- 0.28 μV p-p Noise (0.1 Hz to 10 Hz)

EXCELLENT AC SPECIFICATIONS
- 120 kHz Bandwidth (G = 100)
- 15 μs Settling Time to 0.01%

APPLICATIONS
- Weigh Scales
- ECG and Medical Instrumentation
- Transducer Interface
- Data Acquisition Systems
- Industrial Process Controls
- Battery Powered and Portable Equipment

CONNECTION DIAGRAM

8-Lead Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



PRODUCT DESCRIPTION

The AD620 is a low cost, high accuracy instrumentation amplifier that requires only one external resistor to set gains of 1 to 1000. Furthermore, the AD620 features 8-lead SOIC and DIP packaging that is smaller than discrete designs, and offers lower power (only 1.3 mA max supply current), making it a good fit for battery powered, portable (or remote) applications.

The AD620, with its high accuracy of 40 ppm maximum nonlinearity, low offset voltage of 50 μV max and offset drift of 0.6 μV/°C max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias current, and low power of the AD620 make it well suited for medical applications such as ECG and noninvasive blood pressure monitors.

The low input bias current of 1.0 nA max is made possible with the use of Superβeta processing in the input stage. The AD620 works well as a preamplifier due to its low input voltage noise of 9 nV/√Hz at 1 kHz, 0.28 μV p-p in the 0.1 Hz to 10 Hz band, 0.1 pA/√Hz input current noise. Also, the AD620 is well suited for multiplexed applications with its settling time of 15 μs to 0.01% and its cost is low enough to enable designs with one in-amp per channel.

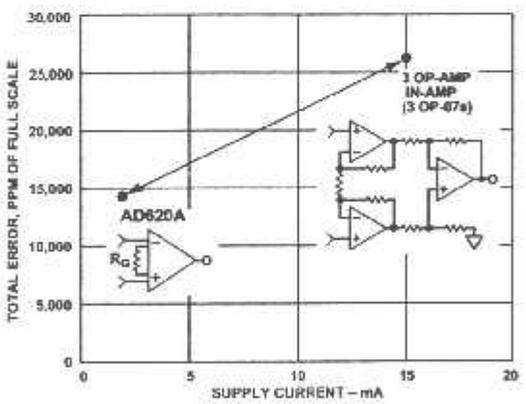


Figure 1. Three Op Amp IA Designs vs. AD620

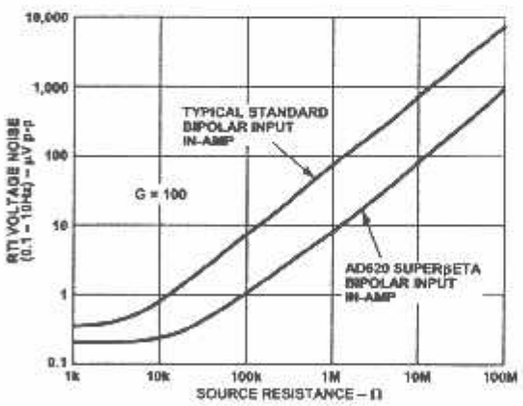


Figure 2. Total Voltage Noise vs. Source Resistance

REV. E

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

620–SPECIFICATIONS (Typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted)

	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
Range	G = 1 + (49.4 kΩ/R_G)	1		10,000	1		10,000	1		10,000	
Error[2]	V_{OUT} = ±10 V										
= 1			0.03	0.10		0.01	0.02		0.03	0.10	%
= 10			0.15	0.30		0.10	0.15		0.15	0.30	%
= 100			0.15	0.30		0.10	0.15		0.15	0.30	%
= 1000			0.40	0.70		0.35	0.50		0.40	0.70	%
linearity,	V_{OUT} = –10 V to +10 V,										
= 1–1000	R_L = 10 kΩ		10	40		10	40		10	40	ppm
= 1–100	R_L = 2 kΩ		10	95		10	95		10	95	ppm
vs. Temperature											
	G = 1			10			10			10	ppm/°C
	Gain >1[2]			–50			–50			–50	ppm/°C
AGE OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)										
ut Offset, V_{OSI}	V_S = ±5 V to ±15 V		30	125		15	50		30	125	µV
ver Temperature	V_S = ±5 V to ±15 V			185			85			225	µV
verage TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
put Offset, V_{OSO}	V_S = ±15 V		400	1000		200	500		400	1000	µV
	V_S = ±5 V			1500			750			1500	µV
ver Temperature	V_S = ±5 V to ±15 V			2000			1000			2000	µV
verage TC	V_S = ±5 V to ±15 V		5.0	15		2.5	7.0		5.0	15	µV/°C
et Referred to the put vs.											
upply (PSR)	V_S = ±2.3 V to +18 V										
G = 1		80	100		80	100		80	100		dB
G = 10		95	120		100	120		95	120		dB
G = 100		110	140		120	140		110	140		dB
G = 1000		110	140		120	140		110	140		dB
T CURRENT											
at Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
ver Temperature				2.5			1.5			4	nA
verage TC			3.0			3.0			8.0		pA/°C
at Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
ver Temperature				1.5			0.75			2.0	nA
verage TC			1.5			1.5			8.0		pA/°C
T											
ut Impedance											
Differential			10|2			10|2			10|2		GΩ|pF
Common-Mode			10|2			10|2			10|2		GΩ|pF
ut Voltage Range[3]	V_S = ±2.3 V to ±5 V	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	V
Over Temperature		$–V_S$ + 2.1		$+V_S$ – 1.3	$–V_S$ + 2.1		$+V_S$ – 1.3	$–V_S$ + 2.1		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$–V_S$ + 1.9		$+V_S$ – 1.4	$–V_S$ + 1.9		$+V_S$ – 1.4	$–V_S$ + 1.9		$+V_S$ – 1.4	V
Over Temperature		$–V_S$ + 2.1		$+V_S$ – 1.4	$–V_S$ + 2.1		$+V_S$ – 1.4	$–V_S$ + 2.3		$+V_S$ – 1.4	V
mmon Mode Rejection Ratio DC to 60 Hz with kΩ Source Imbalance	V_{CM} = 0 V to ±10 V										
G = 1		73	90		80	90		73	90		dB
G = 10		93	110		100	110		93	110		dB
G = 100		110	130		120	130		110	130		dB
G = 1000		110	130		120	130		110	130		dB
PUT											
utput Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	V
Over Temperature		$–V_S$ + 1.4		$+V_S$ – 1.3	$–V_S$ + 1.4		$+V_S$ – 1.3	$–V_S$ + 1.6		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$–V_S$ + 1.2		$+V_S$ – 1.4	$–V_S$ + 1.2		$+V_S$ – 1.4	$–V_S$ + 1.2		$+V_S$ 1.4	V
Over Temperature		$–V_S$ + 1.6		$+V_S$ – 1.5	$–V_S$ + 1.6		$+V_S$ – 1.5	$–V_S$ + 2.3		$+V_S$ – 1.5	V
hort Current Circuit			±18			±18			±18		mA

del	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
/NAMIC RESPONSE											
Small Signal –3 dB Bandwidth											
G = 1			1000			1000			1000		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			12			12			12		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/μs
Settling Time to 0.01%	10 V Step										
G = 1–100			15			15			15		μs
G = 1000			150			150			150		μs
OISE											
Voltage Noise, 1 kHz	*Total RTI Noise* = $\sqrt{(e_{ni}^2)+(e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			9	13		9	13		9	13	nV/√Hz
Output, Voltage Noise, e_{no}			72	100		72	100		72	100	nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0	6.0		3.0	6.0	μV p-p
G = 10			0.55			0.55	0.8		0.55	0.8	μV p-p
G = 100–1000			0.28			0.28	0.4		0.28	0.4	μV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
0.1 Hz to 10 Hz			10			10			10		pA p-p
EFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		+50	+60		+50	+60		+50	+60	μA
Voltage Range		$-V_S$ + 1.6		$+V_S$ – 1.6	$-V_S$ + 1.6		$+V_S$ – 1.6	$-V_S$ + 1.6		$+V_S$ – 1.6	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
OWER SUPPLY											
Operating Range[4]		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
Over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance			–40 to +85			–40 to +85			–55 to +125		°C

OTES
See Analog Devices military data sheet for 883B tested specifications.
Does not include effects of external resistor R_G.
One input grounded. G = 1.
This is defined as the same supply range which is used to specify PSR.
pecifications subject to change without notice.

LUTE MAXIMUM RATINGS[1]

' Voltage	±18 V
al Power Dissipation[2]	650 mW
Voltage (Common Mode)	$\pm V_S$
ential Input Voltage	±25 V
ıt Short Circuit Duration	Indefinite
ge Temperature Range (Q)	−65°C to +150°C
ge Temperature Range (N, R)	−65°C to +125°C
ıting Temperature Range	
620 (A, B)	−40°C to +85°C
620 (S)	−55°C to +125°C
Temperature Range	
ldering 10 seconds)	+300°C

S

es above those listed under Absolute Maximum Ratings may cause perma- lamage to the device. This is a stress rating only; functional operation of the : at these or any other conditions above those indicated in the operational n of this specification is not implied. Exposure to absolute maximum rating tions for extended periods may affect device reliability.

ication is for device in free air:

d Plastic Package: θ_{JA} = 95°C/W

d Cerdip Package: θ_{JA} = 110°C/W

d SOIC Package: θ_{JA} = 155°C/W

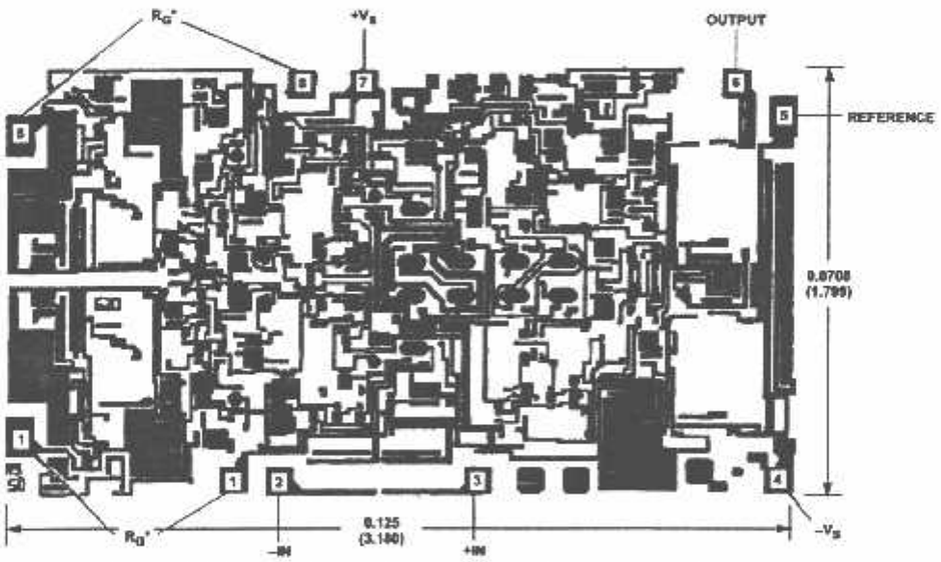
ORDERING GUIDE

Model	Temperature Ranges	Package Options*
AD620AN	−40°C to +85°C	N-8
AD620BN	−40°C to +85°C	N-8
AD620AR	−40°C to +85°C	SO-8
AD620AR-REEL	−40°C to +85°C	13" REEL
AD620AR-REEL7	−40°C to +85°C	7" REEL
AD620BR	−40°C to +85°C	SO-8
AD620BR-REEL	−40°C to +85°C	13" REEL
AD620BR-REEL7	−40°C to +85°C	7" REEL
AD620ACHIPS	−40°C to +85°C	Die Form
AD620SQ/883B	−55°C to +125°C	Q-8

*N = Plastic DIP; Q = Cerdip; SO = Small Outline.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



*FOR CHIP APPLICATIONS: THE PADS $1R_G$ AND $8R_G$ MUST BE CONNECTED IN PARALLEL TO THE EXTERNAL GAIN REGISTER R_G. DO NOT CONNECT THEM IN SERIES TO R_G. FOR UNITY GAIN APPLICATIONS WHERE R_G IS NOT REQUIRED, THE PADS $1R_G$ MAY SIMPLY BE BONDED TOGETHER, AS WELL AS THE PADS $8R_G$.

UTION

D (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily umulate on the human body and test equipment and can discharge without detection. hough the AD620 features proprietary ESD protection circuitry, permanent damage may ur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD cautions are recommended to avoid performance degradation or loss of functionality.

/pical Characteristics (@ +25°C, $V_S = \pm 15$ V, $R_L = 2\ k\Omega$, unless otherwise noted)

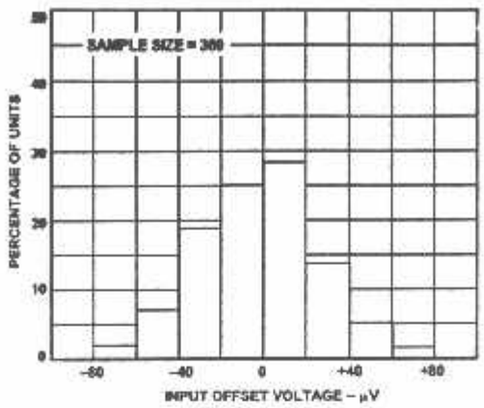


Figure 3. Typical Distribution of Input Offset Voltage

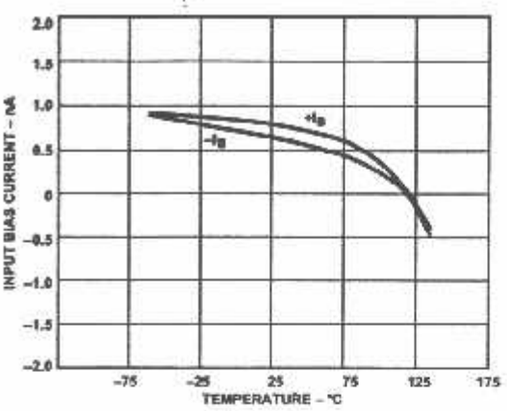


Figure 6. Input Bias Current vs. Temperature

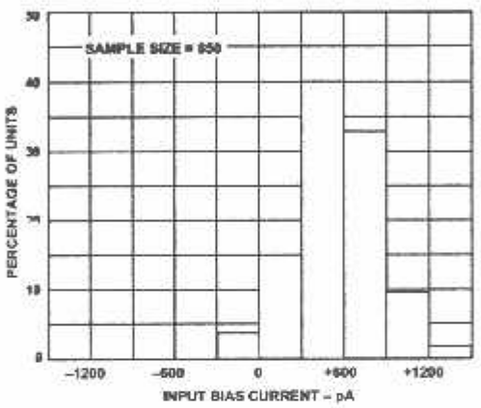


Figure 4. Typical Distribution of Input Bias Current

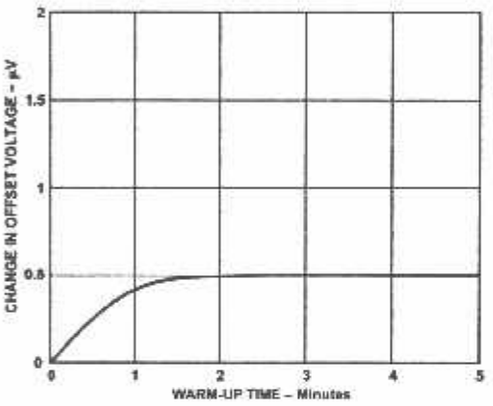


Figure 7. Change in Input Offset Voltage vs. Warm-Up Time

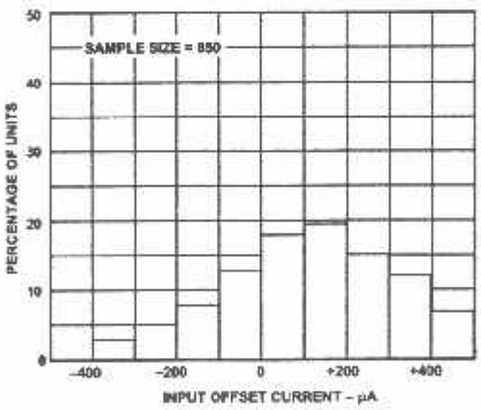


Figure 5. Typical Distribution of Input Offset Current

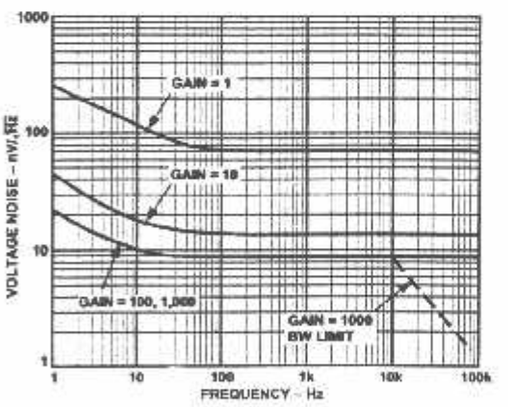
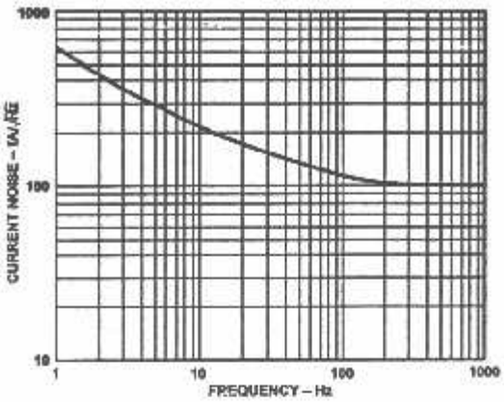


Figure 8. Voltage Noise Spectral Density vs. Frequency, (G = 1–1000)

20–Typical Characteristics



ıure 9. Current Noise Spectral Density vs. Frequency

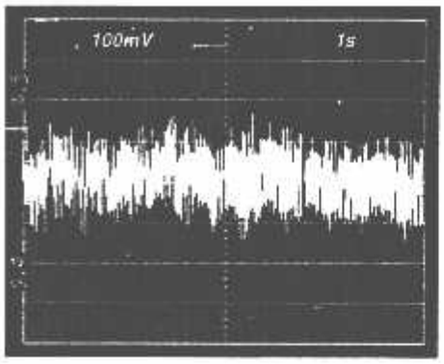
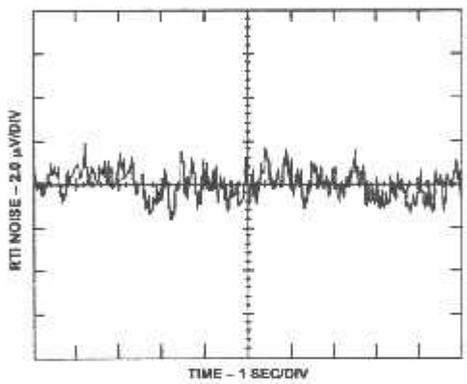


Figure 11. 0.1 Hz to 10 Hz Current Noise, 5 pA/Div



igure 10a. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

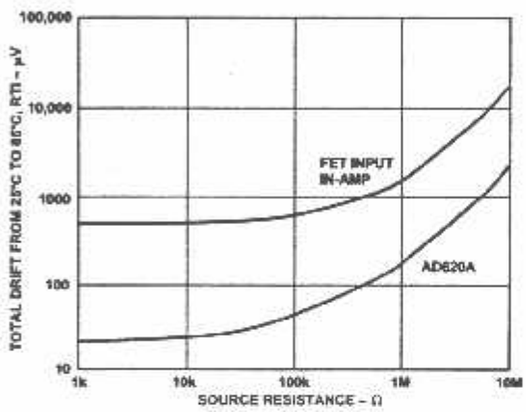
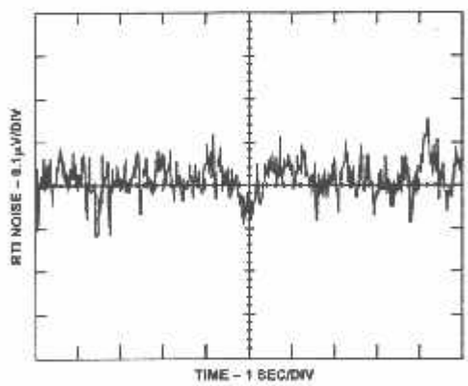


Figure 12. Total Drift vs. Source Resistance



igure 10b. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

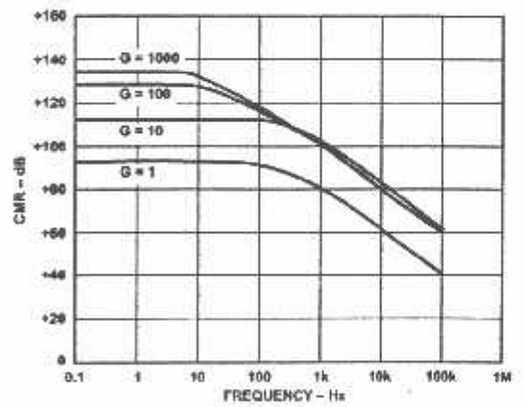


Figure 13. CMR vs. Frequency, RTI, Zero to 1 kΩ Source Imbalance

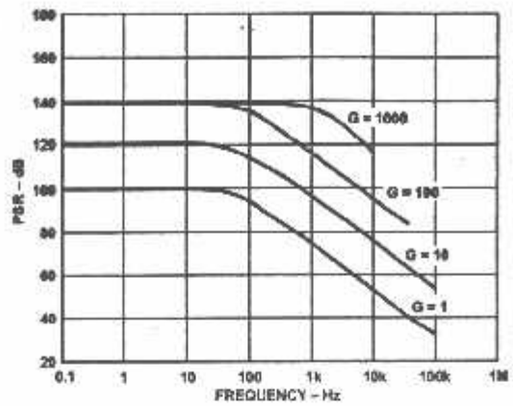


Figure 14. Positive PSR vs. Frequency, RTI (G = 1–1000)

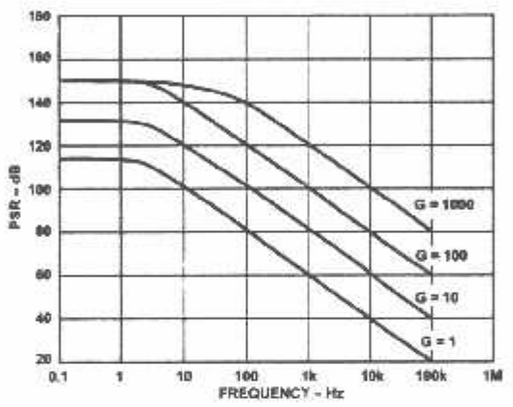


Figure 15. Negative PSR vs. Frequency, RTI (G = 1–1000)

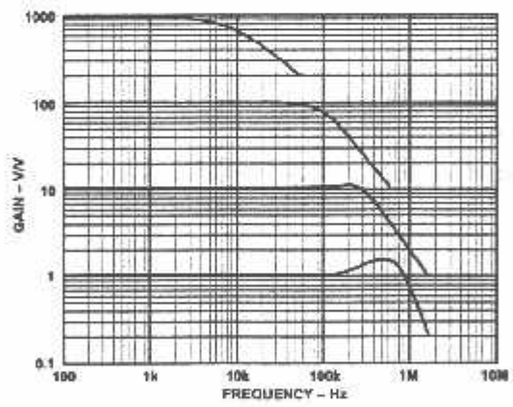


Figure 16. Gain vs. Frequency

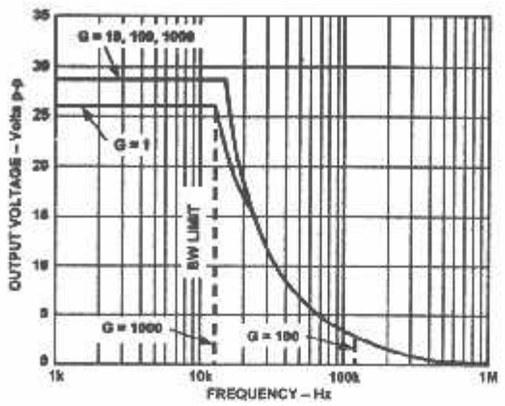


Figure 17. Large Signal Frequency Response

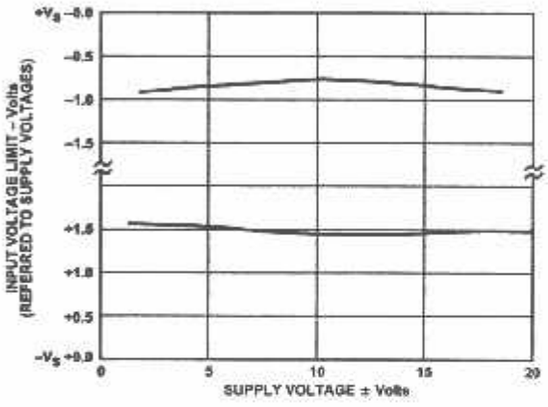


Figure 18. Input Voltage Range vs. Supply Voltage, G = 1

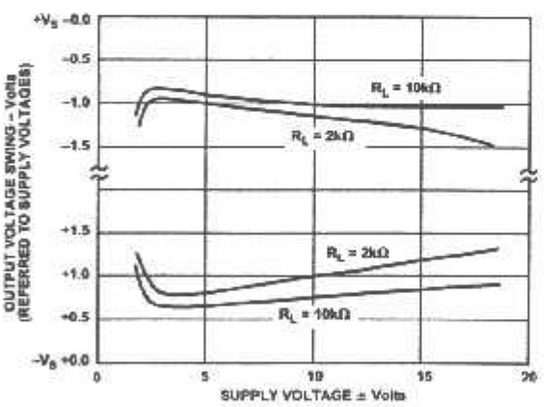
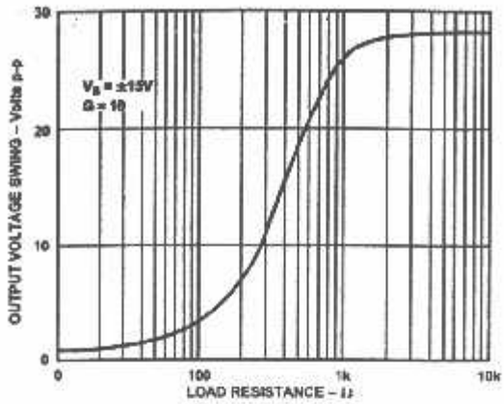


Figure 19. Output Voltage Swing vs. Supply Voltage, G = 10



'igure 20. Output Voltage Swing vs. Load Resistance

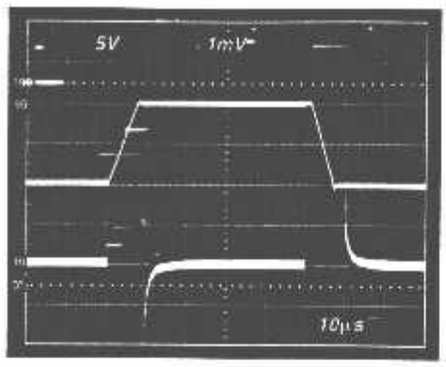
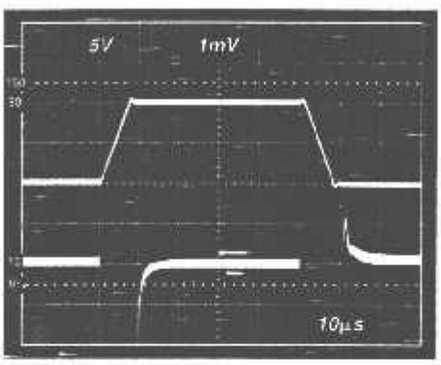


Figure 23. Large Signal Response and Settling Time, G = 10 (0.5 mV = 001%)



ıre 21. Large Signal Pulse Response and Settling Time 1 (0.5 mV = 0.01%)

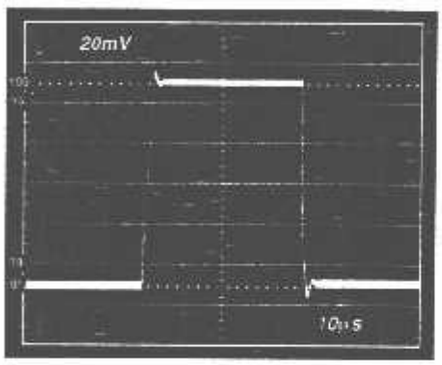


Figure 24. Small Signal Response, G = 10, R_L = 2 kΩ, C_L = 100 pF

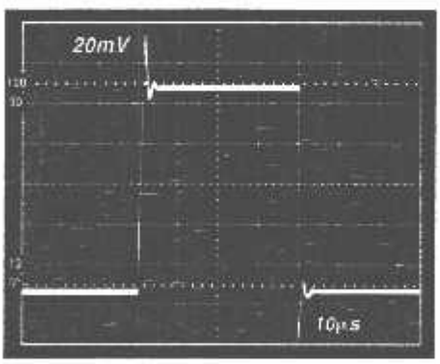


Figure 22. Small Signal Response, G = 1, R_L = 2 kΩ, C_L = 100 pF

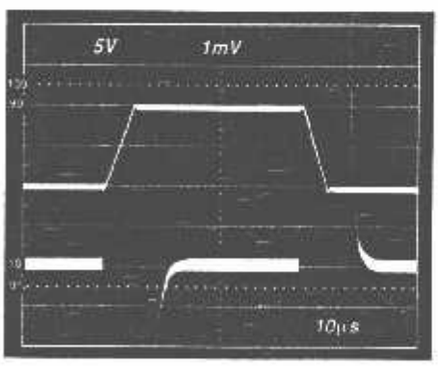


Figure 25. Large Signal Response and Settling Time, G = 100 (0.5 mV = 0.01%)

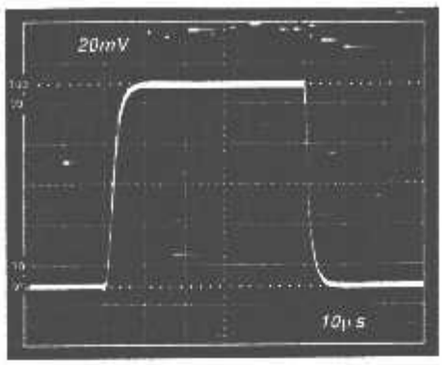


Figure 26. Small Signal Pulse Response, G = 100, R_L = 2 kΩ, C_L = 100 pF

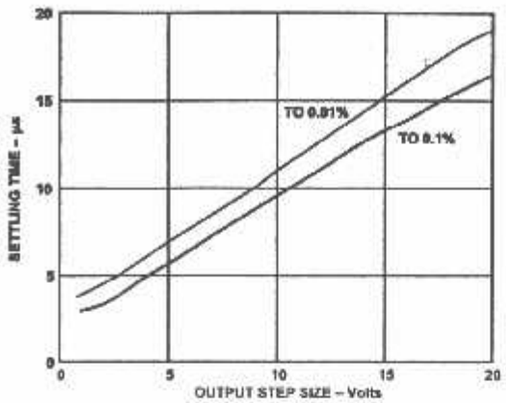


Figure 29. Settling Time vs. Step Size (G = 1)

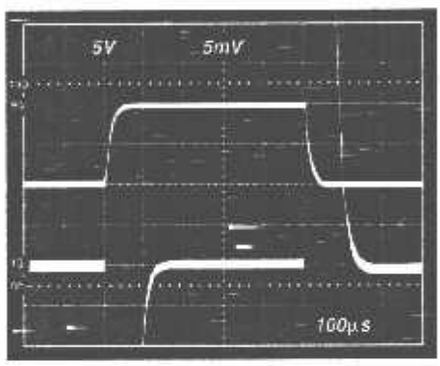


Figure 27. Large Signal Response and Settling Time, G = 1000 (0.5 mV = 0.01%)

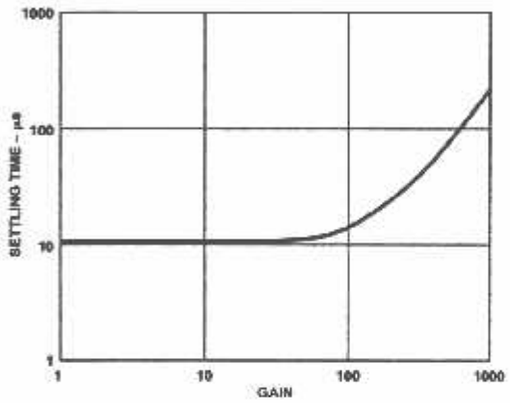


Figure 30. Settling Time to 0.01% vs. Gain, for a 10 V Step

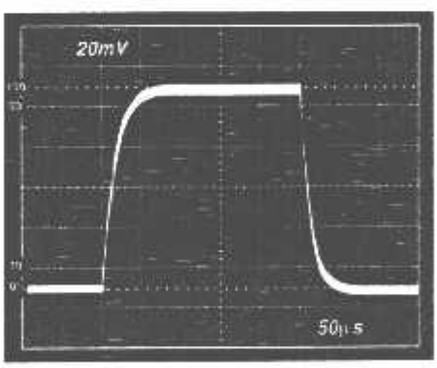


Figure 28. Small Signal Pulse Response, G = 1000, R_L = 2 kΩ, C_L = 100 pF

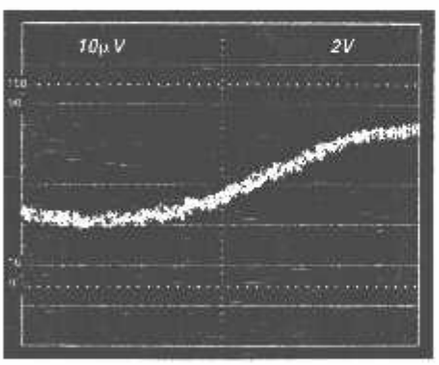
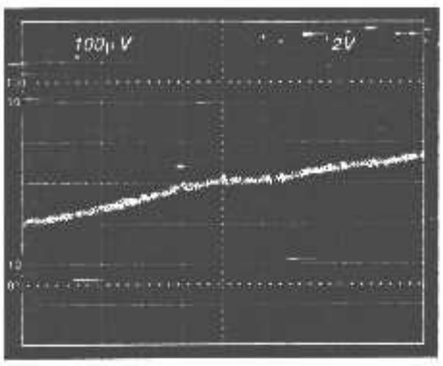
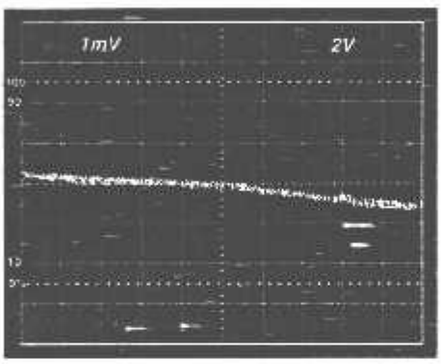


Figure 31a. Gain Nonlinearity, G = 1, R_L = 10 kΩ (10 µV = 1 ppm)



igure 31b. Gain Nonlinearity, G = 100, R_L = 10 kΩ 100 μV = 10 ppm)



igure 31c. Gain Nonlinearity, G = 1000, R_L = 10 kΩ 1 mV = 100 ppm)

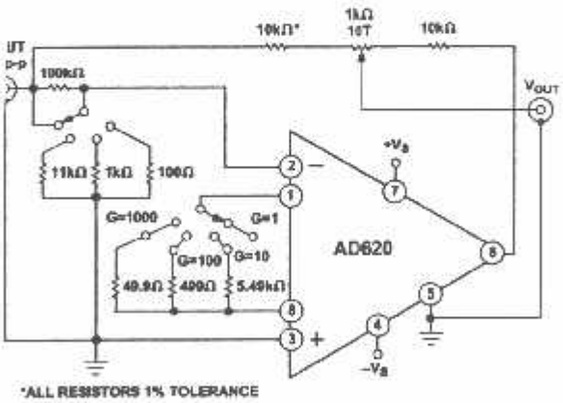


Figure 32. Settling Time Test Circuit

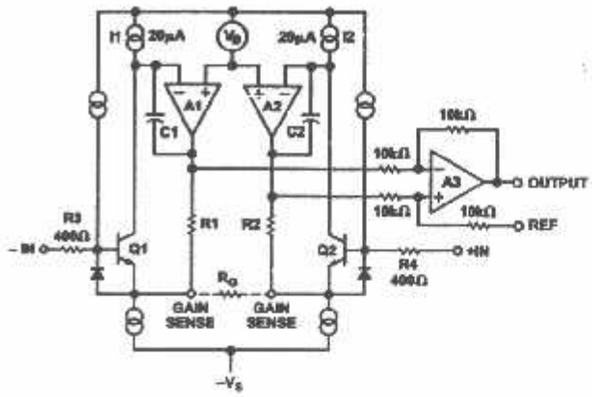


Figure 33. Simplified Schematic of AD620

THEORY OF OPERATION

The AD620 is a monolithic instrumentation amplifier based on a modification of the classic three op amp approach. Absolute value trimming allows the user to program gain *accurately* (to 0.15% at G = 100) with only one resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components, thus ensuring the high level of performance inherent in this circuit.

The input transistors Q1 and Q2 provide a single differential-pair bipolar input for high precision (Figure 33), yet offer 10× lower Input Bias Current thanks to Superβeta processing. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains constant collector current of the input devices Q1, Q2 thereby impressing the input voltage across the external gain setting resistor R_G. This creates a differential gain from the inputs to the A1/A2 outputs given by G = (R1 + R2)/R_G + 1. The unity-gain subtracter A3 removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: (a) Open-loop gain is boosted for increasing programmed gain, thus reducing gain-related errors. (b) The gain-bandwidth product (determined by C1, C2 and the preamp transconductance) increases with programmed gain, thus optimizing frequency response. (c) The input voltage noise is reduced to a value of 9 nV/$\sqrt{\text{Hz}}$, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor.

The gain equation is then

$$G = \frac{49.4\ k\Omega}{R_G} + 1$$

so that

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

Make vs. Buy: A Typical Bridge Application Error Budget
The AD620 offers improved performance over "homebrew" three op amp IA designs, along with smaller size, fewer components and 10× lower supply current. In the typical application, shown in Figure 34, a gain of 100 is required to amplify a bridge output of 20 mV full scale over the industrial temperature range of –40°C to +85°C. The error budget table below shows how to calculate the effect various error sources have on circuit accuracy.

Regardless of the system in which it is being used, the AD620 provides greater accuracy, and at low power and price. In simple systems, absolute accuracy and drift errors are by far the most significant contributors to error. In more complex systems with an intelligent processor, an autogain/autozero cycle will remove all absolute accuracy and drift errors leaving only the resolution errors of gain nonlinearity and noise, thus allowing full 14-bit accuracy.

Note that for the homebrew circuit, the OP07 specifications for input voltage offset and noise have been multiplied by $\sqrt{2}$. This is because a three op amp type in-amp has two op amps at its inputs, both contributing to the overall input error.

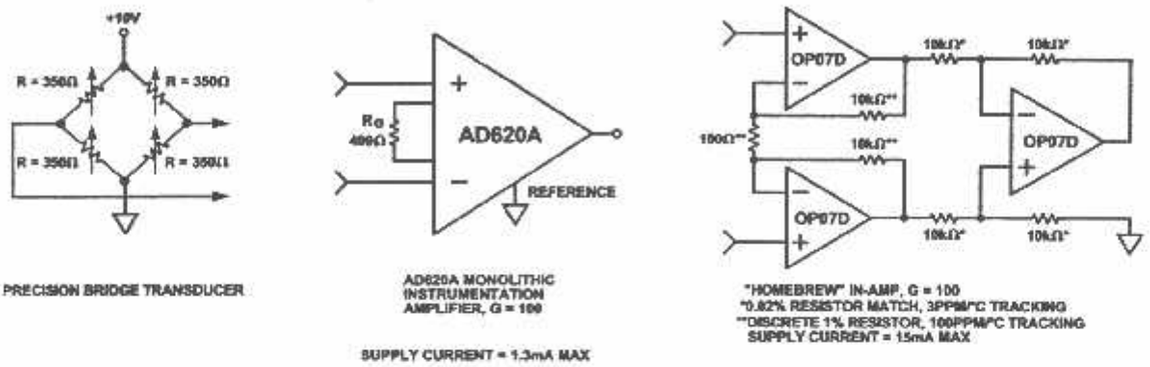


Figure 34. Make vs. Buy

Table I. Make vs. Buy Error Budget

Error Source	AD620 Circuit Calculation	"Homebrew" Circuit Calculation	Error, ppm of Full Scale AD620	Homebrew
ABSOLUTE ACCURACY at T_A = +25°C				
Input Offset Voltage, µV	125 µV/20 mV	(150 µV × $\sqrt{2}$)/20 mV	6,250	10,607
Output Offset Voltage, µV	1000 µV/100/20 mV	((150 µV × 2)/100)/20 mV	500	150
Input Offset Current, nA	2 nA × 350 Ω/20 mV	(6 nA × 350 Ω)/20 mV	18	53
CMR, dB	110 dB→3.16 ppm, × 5 V/20 mV	(0.02% Match × 5 V)/20 mV/100	791	500
		Total Absolute Error	7,558	11,310
DRIFT TO +85°C				
Gain Drift, ppm/°C	(50 ppm + 10 ppm) × 60°C	100 ppm/°C Track × 60°C	3,600	6,000
Input Offset Voltage Drift, µV/°C	1 µV/°C × 60°C/20 mV	(2.5 µV/°C × $\sqrt{2}$ × 60°C)/20 mV	3,000	10,607
Output Offset Voltage Drift, µV/°C	15 µV/°C × 60°C/100/20 mV	(2.5 µV/°C × 2 × 60°C)/100/20 mV	450	150
		Total Drift Error	7,050	16,757
RESOLUTION				
Gain Nonlinearity, ppm of Full Scale	40 ppm	40 ppm	40	40
Typ 0.1 Hz–10 Hz Voltage Noise, µV p-p	0.28 µV p-p/20 mV	(0.38 µV p-p × $\sqrt{2}$)/20 mV	14	27
		Total Resolution Error	54	67
		Grand Total Error	14,662	28,134

G = 100, V_S = ±15 V.

(All errors are min/max and referred to input.)

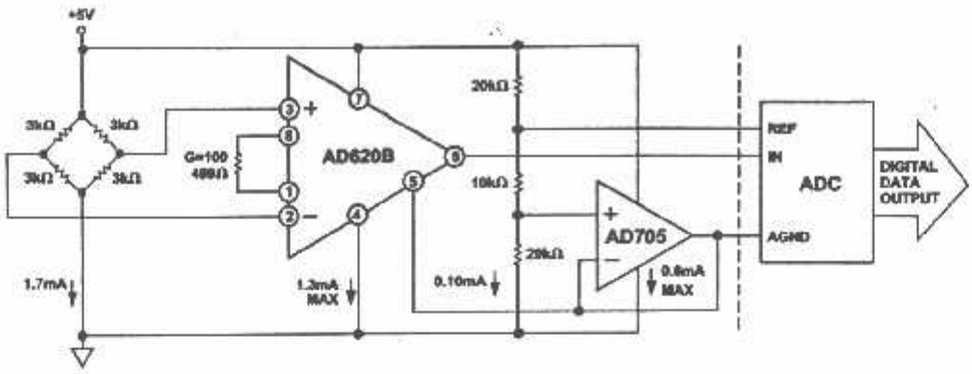


Figure 35. A Pressure Monitor Circuit which Operates on a +5 V Single Supply

sure Measurement

ough useful in many bridge applications such as weigh s, the AD620 is especially suitable for higher resistance sure sensors powered at lower voltages where small size and power become more significant.

re 35 shows a 3 kΩ pressure transducer bridge powered . +5 V. In such a circuit, the bridge consumes only 1.7 mA. ing the AD620 and a buffered voltage divider allows the al to be conditioned for only 3.8 mA of total supply current.

ll size and low cost make the AD620 especially attractive for ge output pressure transducers. Since it delivers low noise drift, it will also serve applications such as diagnostic non-sive blood pressure measurement.

Medical ECG

The low current noise of the AD620 allows its use in ECG monitors (Figure 36) where high source resistances of 1 MΩ or higher are not uncommon. The AD620's low power, low supply voltage requirements, and space-saving 8-lead mini-DIP and SOIC package offerings make it an excellent choice for battery powered data recorders.

Furthermore, the low bias currents and low current noise coupled with the low voltage noise of the AD620 improve the dynamic range for better performance.

The value of capacitor C1 is chosen to maintain stability of the right leg drive loop. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

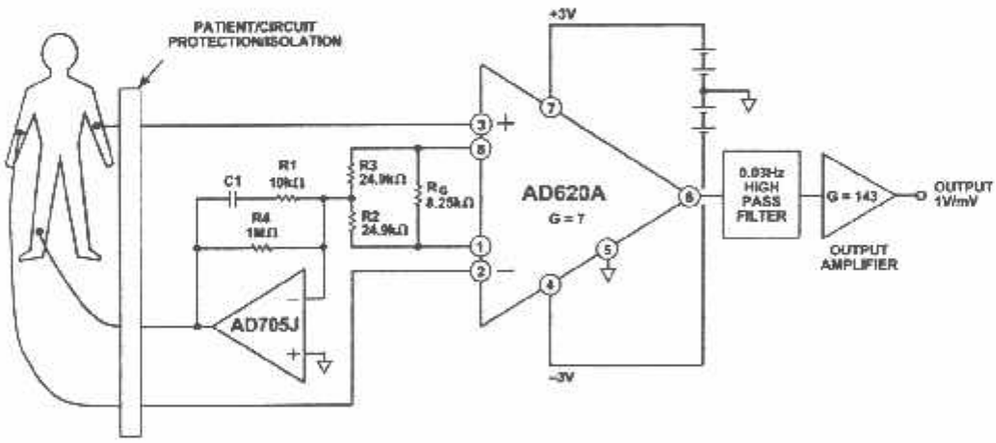


Figure 36. A Medical ECG Monitor Circuit

ecision V-I Converter

ıe AD620, along with another op amp and two resistors, makes ›recision current source (Figure 37). The op amp buffers the ference terminal to maintain good CMR. The output voltage x of the AD620 appears across R1, which converts it to a ırrent. This current less only, the input bias current of the op np, then flows out to the load.

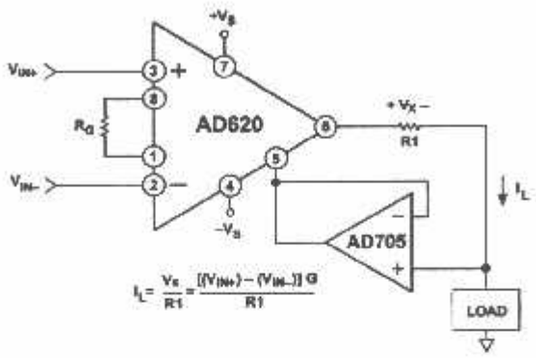


Figure 37. Precision Voltage-to-Current Converter (Operates on 1.8 mA, ±3 V)

;AIN SELECTION

The AD620's gain is resistor programmed by R_G, or more precisely, by whatever impedance appears between Pins 1 and 8. The AD620 is designed to offer accurate gains using 0.1%–1% esistors. Table II shows required values of R_G for various gains. Jote that for G = 1, the R_G pins are unconnected ($R_G = \infty$). For ny arbitrary gain R_G can be calculated by using the formula:

$$R_G = \frac{49.4\ k\Omega}{G-1}$$

To minimize gain error, avoid high parasitic resistance in series vith R_G; to minimize gain drift, R_G should have a low TC—less han 10 ppm/°C—for the best performance.

Table II. Required Values of Gain Resistors

1% Std Table Value of R_G, Ω	Calculated Gain	0.1% Std Table Value of R_G, Ω	Calculated Gain
49.9 k	1.990	49.3 k	2.002
12.4 k	4.984	12.4 k	4.984
5.49 k	9.998	5.49 k	9.998
2.61 k	19.93	2.61 k	19.93
1.00 k	50.40	1.01 k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003

INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD620 are attributed to two sources, input and output errors. The output error is divided by G when referred to the input. In practice, the input errors dominate at high gains and the output errors dominate at low gains. The total V_{OS} for a given gain is calculated as:

Total Error RTI = input error + (output error/G)

Total Error RTO = (input error × G) + output error

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage, and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

INPUT PROTECTION

The AD620 features 400 Ω of series thin film resistance at its inputs, and will safely withstand input overloads of up to ±15 V or ±60 mA for several hours. This is true for all gains, and power on and off, which is particularly important since the signal source and amplifier may be powered separately. For longer time periods, the current should not exceed 6 mA ($I_{IN} \le V_{IN}/400\ \Omega$). For input overloads beyond the supplies, clamping the inputs to the supplies (using a low leakage diode such as an FD333) will reduce the required resistance, yielding lower noise.

RF INTERFERENCE

All instrumentation amplifiers can rectify out of band signals, and when amplifying small signals, these rectified voltages act as small dc offset errors. The AD620 allows direct access to the input transistor bases and emitters enabling the user to apply some first order filtering to unwanted RF signals (Figure 38), where $RC \approx 1/(2\pi f)$ and where $f \ge$ the bandwidth of the AD620; $C \le 150$ pF. Matching the extraneous capacitance at Pins 1 and 8 and Pins 2 and 3 helps to maintain high CMR.

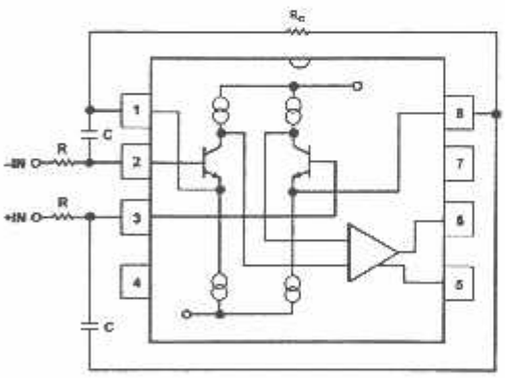


Figure 38. Circuit to Attenuate RF Interference

MON-MODE REJECTION

mentation amplifiers like the AD620 offer high CMR, i is a measure of the change in output voltage when both s are changed by equal amounts. These specifications are ly given for a full-range input voltage change and a speci- ource imbalance.

optimal CMR the reference terminal should be tied to a low dance point, and differences in capacitance and resistance ld be kept to a minimum between the two inputs. In many cations shielded cables are used to minimize noise, and for CMR over frequency the shield should be properly driven. res 39 and 40 show active data guards that are configured prove ac common-mode rejections by "bootstrapping" the citances of input cable shields, thus minimizing the capaci- e mismatch between the inputs.

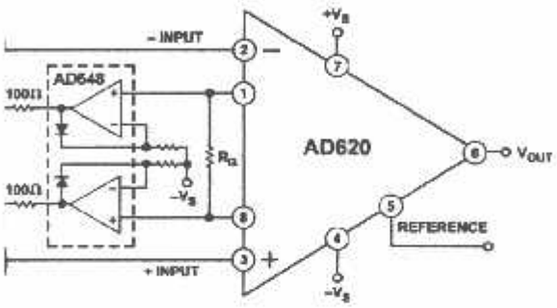


Figure 39. Differential Shield Driver

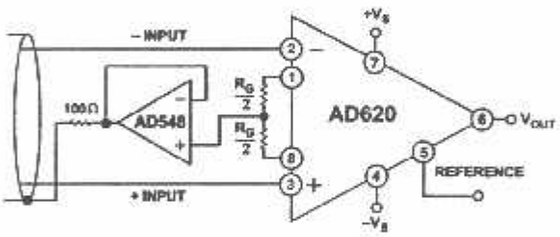


Figure 40. Common-Mode Shield Driver

GROUNDING

Since the AD620 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems by simply tying the REF pin to the appropriate "local ground."

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground pins (Figure 41). It would be convenient to use a single ground line; however, current through ground wires and PC runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground. These ground returns must be tied together at some point, usually best at the ADC package as shown.

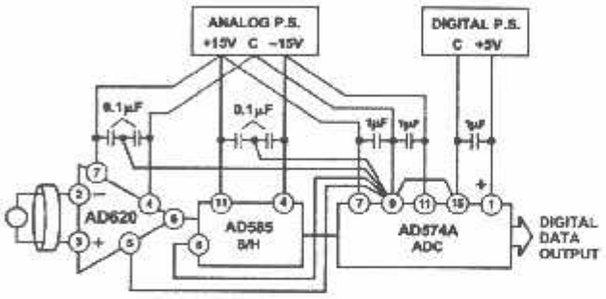


Figure 41. Basic Grounding Practice

ROUND RETURNS FOR INPUT BIAS CURRENTS

ıput bias currents are those currents necessary to bias the input ansistors of an amplifier. There must be a direct return path ɔr these currents; therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 42. Refer to the *Instrumentation Amplifier Application Guide* (free from Analog Devices) for more information regarding in amp applications.

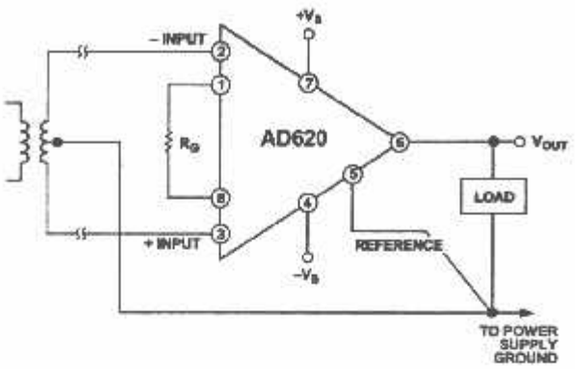


Figure 42a. Ground Returns for Bias Currents with Transformer Coupled Inputs

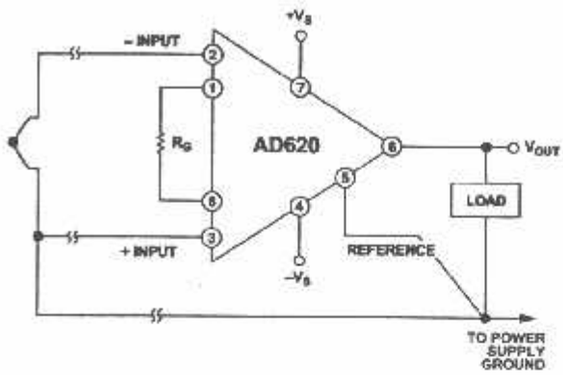


Figure 42b. Ground Returns for Bias Currents with Thermocouple Inputs

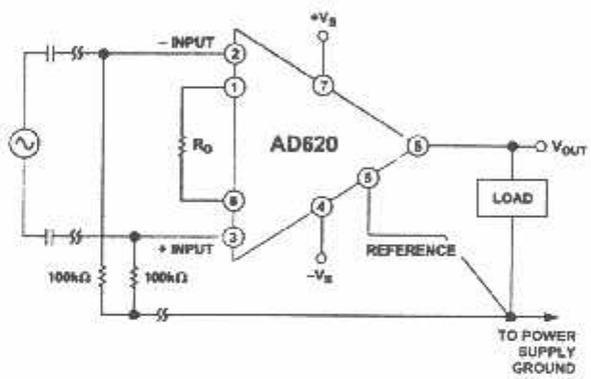
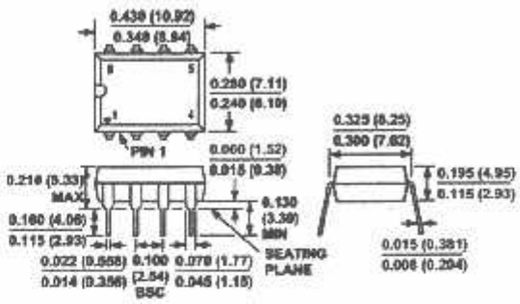


Figure 42c. Ground Returns for Bias Currents with AC Coupled Inputs

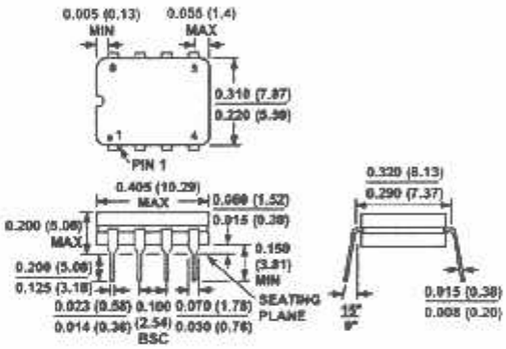
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

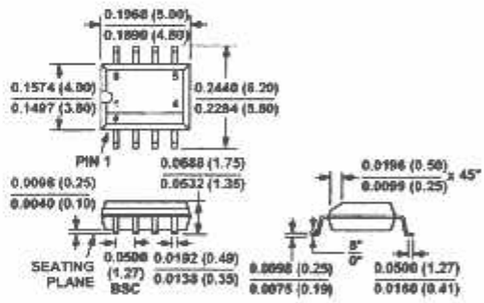
Plastic DIP (N-8) Package



Cerdip (Q-8) Package



SOIC (SO-8) Package



C1599c–0–7/99

PRINTED IN U.S.A.

intersil

OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT

CA741, CA741C, CA1458, CA1558, LM741, LM741C, LM1458

Data Sheet | May 2001 | File Number 531.5

9MHz Single and Dual, High Gain perational Amplifiers for Military, dustrial and Commercial Applications

e CA1458, CA1558 (dual types); CA741C, CA741 (single pes); high-gain operational amplifiers for use in military, dustrial, and commercial applications.

iese monolithic silicon integrated circuit devices provide itput short circuit protection and latch-free operation. iese types also feature wide common mode and ferential mode signal ranges and have low offset voltage illing capability when used with an appropriately valued tentiometer. A 10kΩ potentiometer is used for offset illing types CA741C, CA741 (see Figure 1). Types \1458, CA1558 have no specific terminals for offset illing. Each type consists of a differential input amplifier at effectively drives a gain and level shifting stage having complementary emitter follower output.

ie manufacturing process make it possible to produce IC erational amplifiers with low burst "popcorn" noise aracteristics.

chnical Data on LM Branded types is identical to the rresponding CA Branded types.

Features

- Input Bias Current . . . . . 500nA (Max)
- Input Offset Current . . . . . .200nA (Max)

Applications

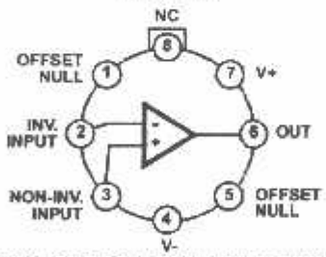
- Comparator
- Multivibrator
- DC Amplifier
- Summing Amplifier
- Integrator or Differentiator
- Narrow Band or Band Pass Filter

Part Number Information

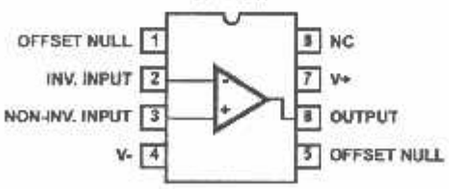
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA0741E	-55 to 125	8 Ld PDIP	E8.3
CA0741CE	0 to 70	8 Ld PDIP	E8.3
CA1458E	0 to 70	8 Ld PDIP	E8.3
CA1558E	-55 to 125	8 Ld PDIP	E8.3
CA0741T	-55 to 125	8 Pin Metal Can	T8.C
CA0741CT	0 to 70	8 Pin Metal Can	T8.C
CA1558T	-55 to 125	8 Pin Metal Can	T8.C
LM741N	-55 to 125	8 Ld PDIP	E8.3
LM741CN	0 to 70	8 Ld PDIP	E8.3
LM1458N	0 to 70	8 Ld PDIP	E8.3

'inouts

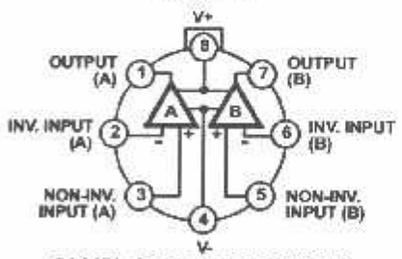
CA741, CA741C (CAN)
TOP VIEW



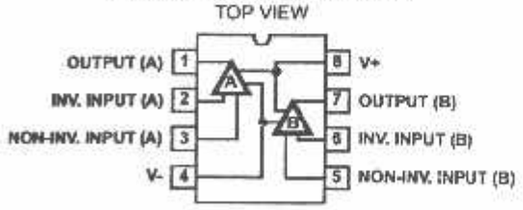
CA741, CA741C, LM741, LM741C (PDIP)
TOP VIEW



CA1558 (METAL CAN)
TOP VIEW



CA1458, CA1558, LM1458 (PDIP)
TOP VIEW



ɔolute Maximum Ratings

ɔly Voltage
A741C, CA1458, LM741C, LM1458 (Note 1) 36V
A741, CA1558, LM741 (Note 1) 44V
ɛrential Input Voltage 30V
ɹt Voltage . . . . . $\pm V_{SUPPLY}$
ɜet Terminal to V- Terminal Voltage (CA741C, CA741). . . . ±0.5V
ɹput Short Circuit Duration. . . . . Indefinite

Thermal Information

Thermal Resistance (Typical; Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	130	N/A
Can Package	155	67

Maximum Junction Temperature (Can Package). . . . . 175°C
Maximum Junction Temperature (Plastic Package). . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

ɔerating Conditions

ɲperature Range
ɔA741, CA1558, LM741 . . . . . -55°C to 125°C
ɔA741C, CA1458, LM741C, LM1458 (Note 2) . . . . 0°C to 70°C

UTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the ɛice at these or any other conditions above those indicated in the operational sections of this specification is not implied.

ITES:

Values apply for each section of the dual amplifiers.

All types in any package style can be operated over the temperature range of -55°C to 125°C, although the published limits for certain electrical specification apply only over the temperature range of 0°C to 70°C.

θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

ɛctrical Specifications

Typical Values Intended Only for Design Guidance, $V_{SUPPLY} = \pm 15V$

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUE (ALL TYPES)	UNITS
ɲput Capacitance	C_I		1.4	pF
ɟfset Voltage Adjustment Range			±15	mV
ɹtput Resistance	R_O		75	Ω
ɹtput Short Circuit Current			25	mA
ansient Response		Unity Gain, V_I = 20mV, R_L = 2kΩ, $C_L \leq 100pF$		
Rise Time	t_r		0.3	µs
Overshoot	O.S.		5.0	%
ɛw Rate (Closed Loop)	SR	$R_L \geq 2k\Omega$	0.5	V/µs
ɜin Bandwidth Product	GBWP	R_L = 12kΩ	0.9	MHz

ɛctrical Specifications

For Equipment Design, $V_{SUPPLY} = \pm 15V$

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 4) CA741, CA1558, LM741			(NOTE 4) CA741C, CA1458, LM741C, LM1458			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ɲput Offset Voltage	$R_S \leq 10k\Omega$	25	-	1	5	-	2	6	mV
		Full	-	1	6	-	-	7.5	mV
ɲput Common Mode Voltage Range		25	-	-	-	±12	±13	-	V
		Full	±12	±13	-	-	-	-	V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	25	-	-	-	70	90	-	dB
		Full	70	90	-	-	-	-	dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	25	-	-	-	-	30	150	µV/V
		Full	-	30	150	-	-	-	µV/V
Input Resistance		25	0.3	2	-	0.3	2	-	MΩ

ctrical Specifications For Equipment Design, $V_{SUPPLY} = \pm 15V$ **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 4) CA741, CA1558, LM741			(NOTE 4) CA741C, CA1458, LM741C, LM1458			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
put Bias Current		25	-	80	500	-	80	500	nA
		Full	-	-	-	-	-	800	nA
		-55	-	300	1500	-	-	-	nA
		125	-	30	500	-	-	-	nA
put Offset Current		25	-	20	200	-	20	200	nA
		Full	-	-	-	-	-	300	nA
		-55	-	85	500	-	-	-	nA
		125	-	7	200	-	-	-	nA
arge Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25	50,000	200,000	-	20,000	200,000	-	V/V
		Full	25,000	-	-	15,000	-	-	V/V
utput Voltage Swing	$R_L \geq 10k\Omega$	25	-	-	-	±12	+14	-	V
		Full	±12	±14	-	-	-	-	V
	$R_L \geq 2k\Omega$	25	-	-	-	±10	±13	-	V
		Full	±10	±13	-	±10	±13	-	V
upply Current		25	-	1.7	2.8	-	1.7	2.8	mA
		-55	-	2	3.3	-	-	-	mA
		125	-	1.5	2.5	-	-	-	mA
evice Power Dissipation		25	-	50	85	-	50	85	mW
		-55	-	60	100	-	-	-	mW
		125	-	45	75	-	-	-	mW

OTE:

1. Values apply for each section of the dual amplifiers.

Test Circuits

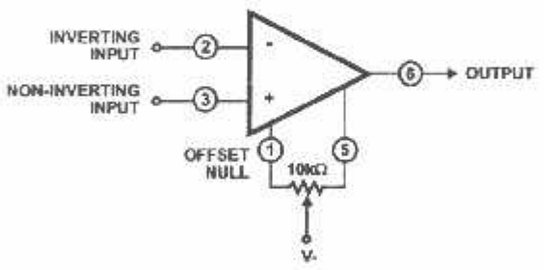


FIGURE 1. OFFSET VOLTAGE NULL CIRCUIT FOR CA741C, CA741, LM741C, AND LM741

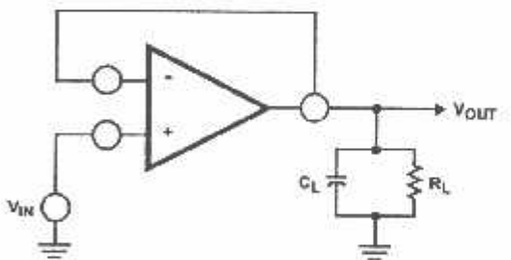
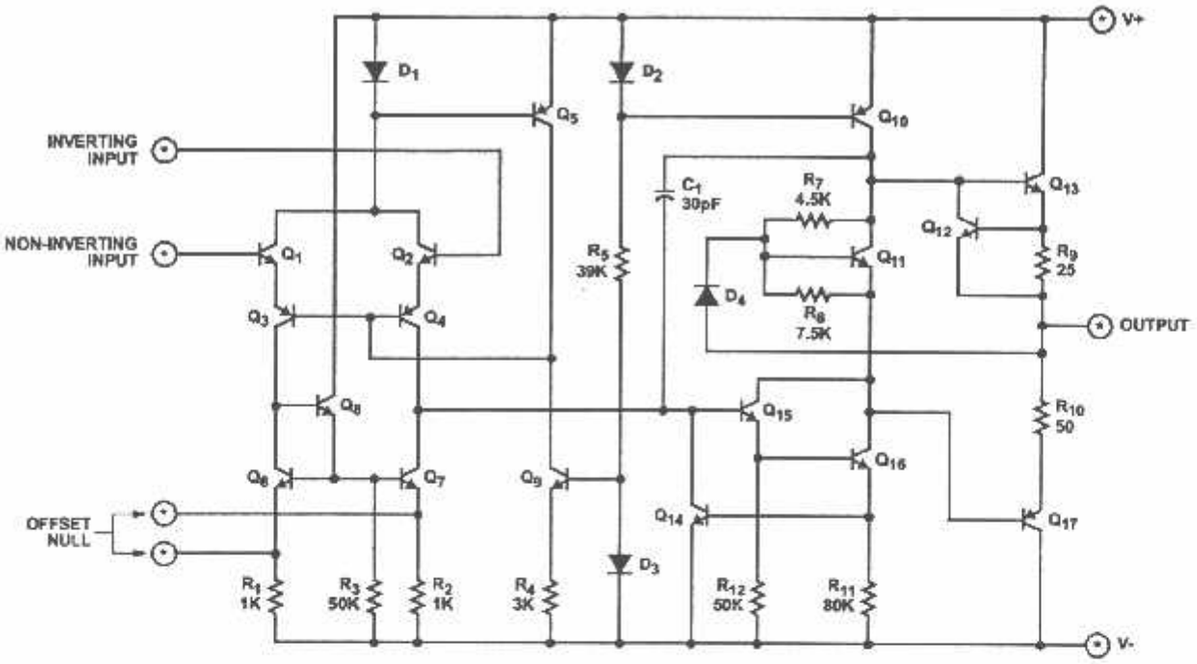


FIGURE 2. TRANSIENT RESPONSE TEST CIRCUIT FOR ALL TYPES

Schematic Diagram (Notes 5, 6)

CA741C, CA741, LM741C, LM741 AND FOR EACH AMPLIFIER OF THE CA1458, CA1558, AND LM1458



NOTES:

5. See Pinouts for Terminal Numbers of Respective Types.
6. All Resistance Values are in Ohms.

Typical Performance Curves

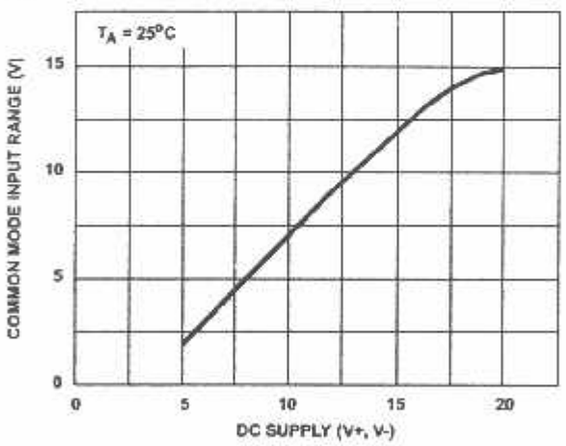


FIGURE 3. COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE FOR ALL TYPES

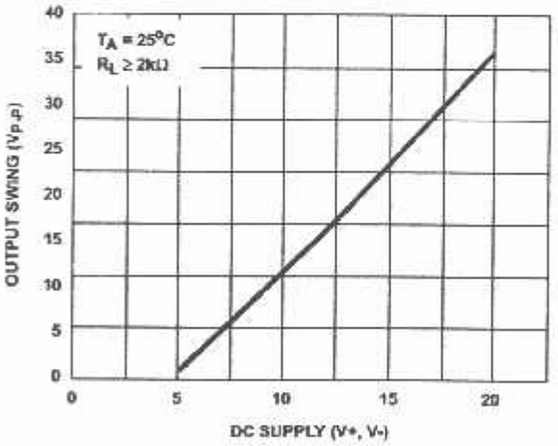


FIGURE 4. OUTPUT VOLTAGE vs SUPPLY VOLTAGE FOR ALL TYPES

ypical Performance Curves (Continued)

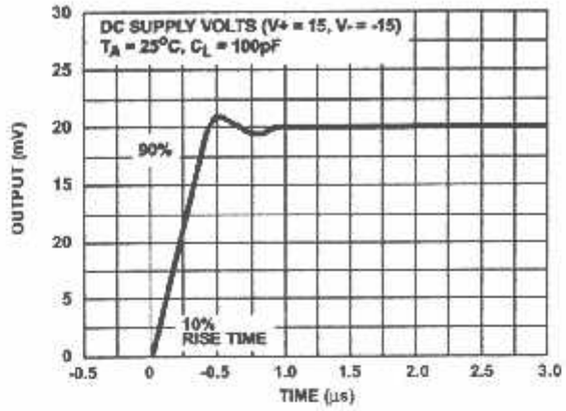
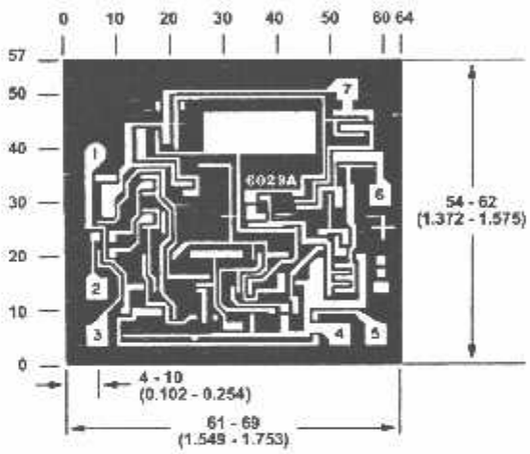


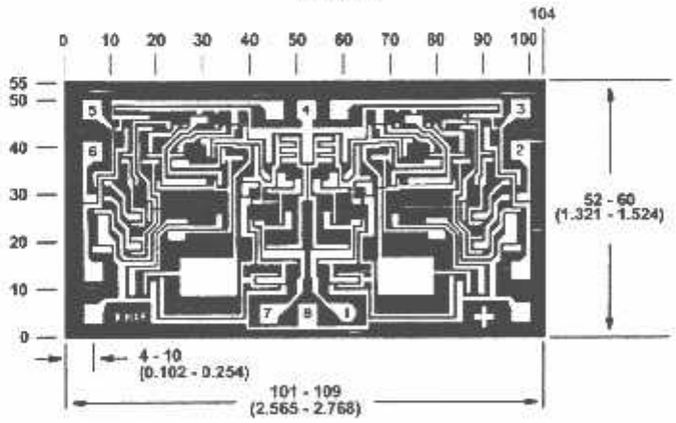
FIGURE 5. TRANSIENT RESPONSE FOR CA741C AND CA741

Metallization Mask Layout

CA741CH



CA1458H



NOTE: Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
2401 Palm Bay Rd.
Palm Bay, FL 32905
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX. (32) 2.724.22.05

ASIA
Intersil Ltd
8F-2, 96, Sec. 1, Chien-kuo North,
Taipei, Taiwan 104
Republic of China
TEL: 886-2-2515-8508
FAX. 886-2-2515-8369

National Semiconductor

November 1999

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805
8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

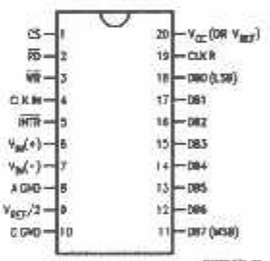
- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 µs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages



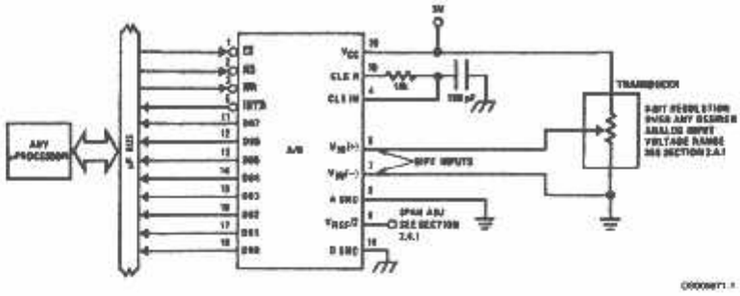
See Ordering Information

Ordering Information

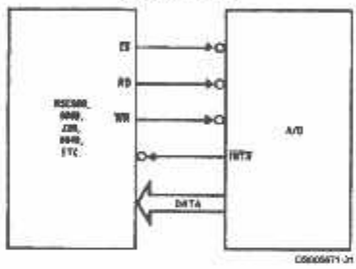
TEMP RANGE		0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted			ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM		ADC0802LCN
	±½ Bit Adjusted			ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCN	ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B—Small Outline	N20A—Molded DIP	

TRI-STATE® is a registered trademark of National Semiconductor Corp.
Z-80® is a registered trademark of Zilog Corp.

Typical Applications



8080 Interface



Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2$=2.500 V_{DC} (No Adjustments)	$V_{REF}/2$=No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±⅛ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0804LCJ	−40°C≤T_A≤+85°C
ADC0801/02/03/05LCN	−40°C≤T_A≤+85°C
ADC0804LCN	0°C≤T_A≤+70°C
ADC0802/04LCWM	0°C≤T_A≤+70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$=2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$=2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			±1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05	2.5	8.0		kΩ
	ADC0804 (Note 9)	0.75	1.1		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Notes 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency	V_{CC}=5V, (Note 5)	100	640	1460	kHz
	Clock Duty Cycle		40		60	%
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ =0 V_{DC}, f_{CLK}=640 kHz	8770		9708	conv/s
$t_{W(WR)L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ =0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN}=0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T−	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis (V_T+)−(V_T−)		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O=360 µA V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O=−360 µA V_{CC}=4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT}=1.6 mA, V_{CC}=4.75 V_{DC} I_{OUT}=1.0 mA, V_{CC}=4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−360 µA, V_{CC}=4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−10 µA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0 V_{DC} V_{OUT}=5 V_{DC}	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A=25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A=25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCWM	f_{CLK}=640 kHz, $V_{REF}/2$=NC, T_A=25°C and $\overline{CS}$ =5V		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause the input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see Figure 4 and section 2.0.

AC Electrical Characteristics (Continued)

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

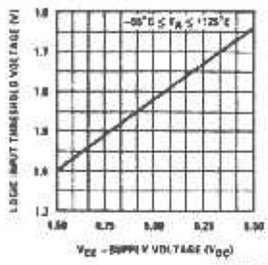
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 7*.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

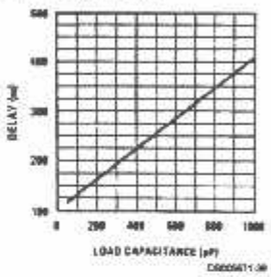
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

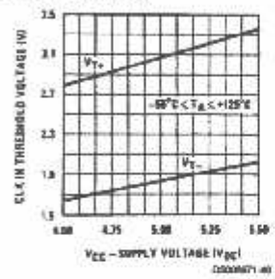
Logic Input Threshold Voltage vs. Supply Voltage



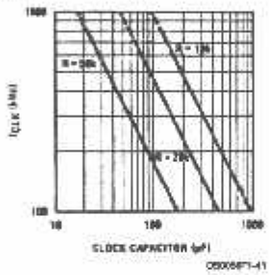
Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance



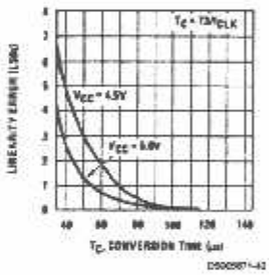
CLK IN Schmitt Trip Levels vs. Supply Voltage



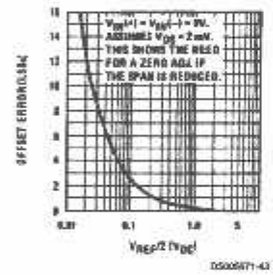
f_{CLK} vs. Clock Capacitor



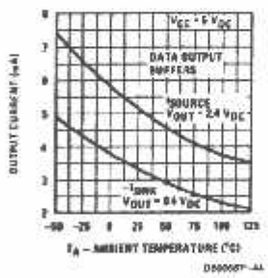
Full-Scale Error vs Conversion Time



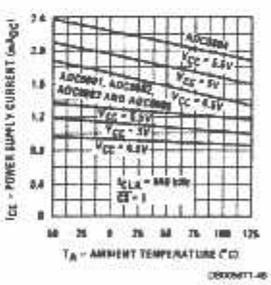
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



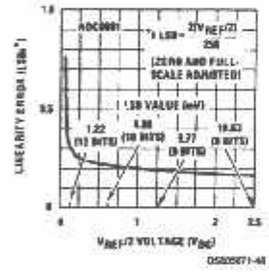
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)

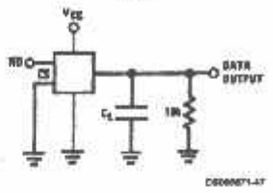


Linearity Error at Low $V_{REF}/2$ Voltages

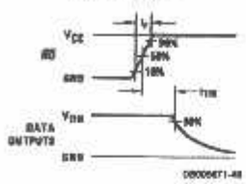


TRI-STATE Test Circuits and Waveforms

t_{1H}

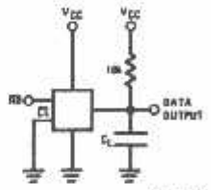


t_{1H}, C_L=10 pF

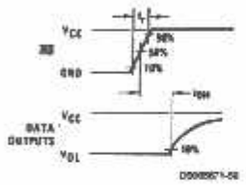


t_r=20 ns

t_{0H}

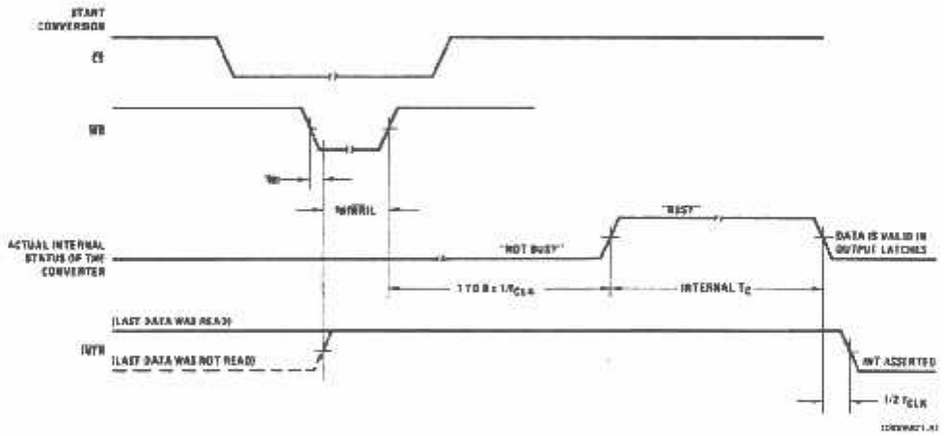


t_{0H}, C_L=10 pF



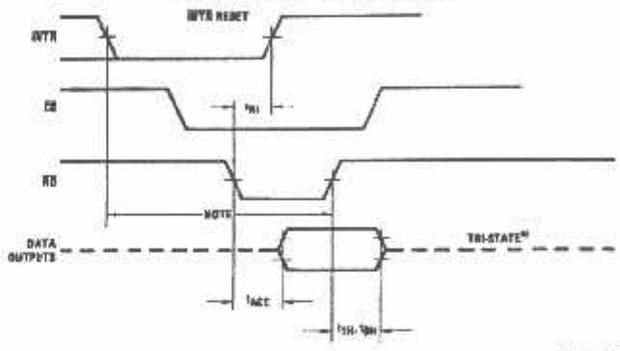
t_r=20 ns

Timing Diagrams (All timing is measured from the 50% voltage points)



Timing Diagrams (All timing is measured from the 50% voltage points) (Continued)

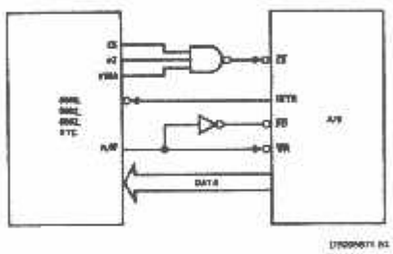
Output Enable and Reset with $\overline{INTR}$



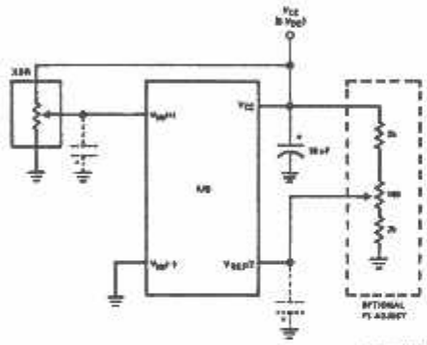
Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

Typical Applications

6800 Interface



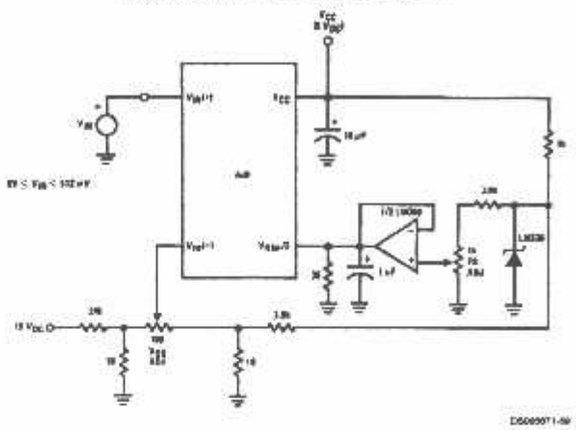
Ratiometeric with Full-Scale Adjust



Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

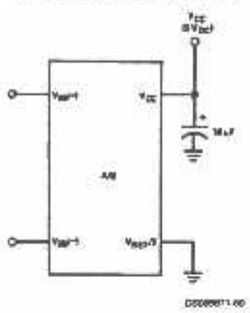
Typical Applications (Continued)

Directly Converting a Low-Level Signal



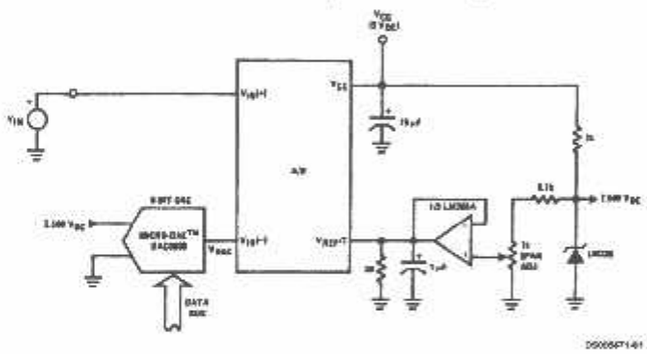
$V_{REF}/2 = 256$ mV

A µP Interfaced Comparator



For:
$V_{IN}(+) > V_{IN}(-)$
Output = FF_{HEX}
For:
$V_{IN}(+) < V_{IN}(-)$
Output = 00_{HEX}

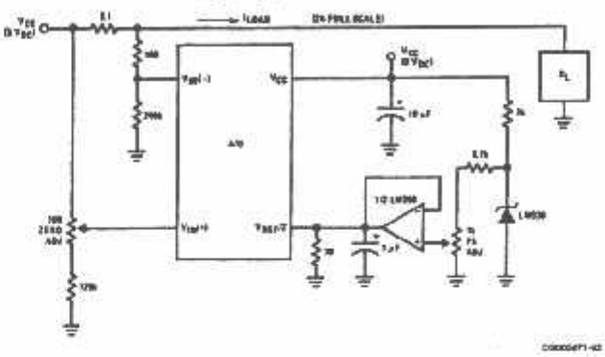
1 mV Resolution with µP Controlled Range



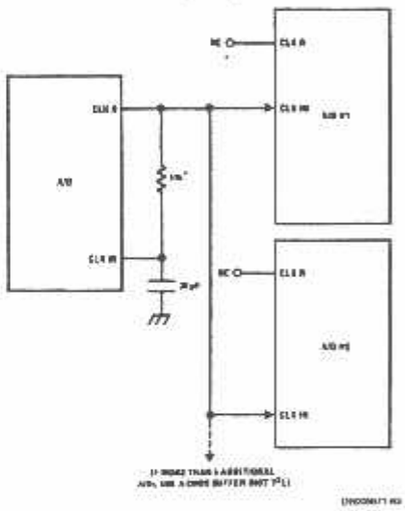
$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} = V_{IN} - (V_{DAC} + 256$ mV)
$0 \le V_{DAC} < 2.5$V

Typical Applications (Continued)

Digitizing a Current Flow

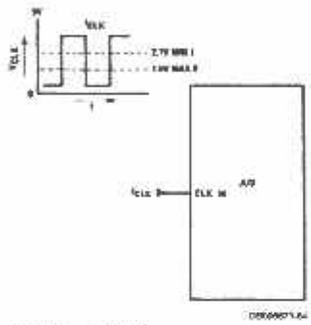


Self-Clocking Multiple A/Ds



* Use a large R value to reduce loading at CLK R output.

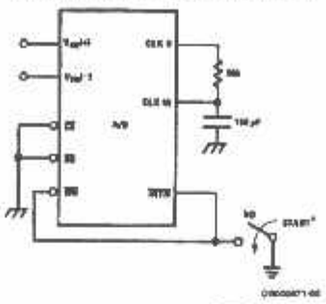
External Clocking



100 kHz≤f_{CLK}≤1460 kHz

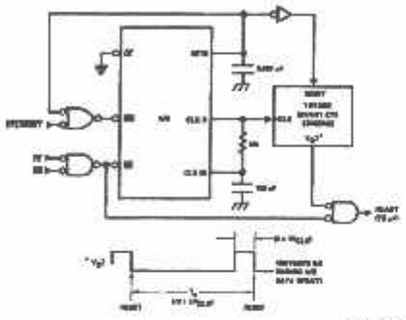
Typical Applications (Continued)

Self-Clocking in Free-Running Mode

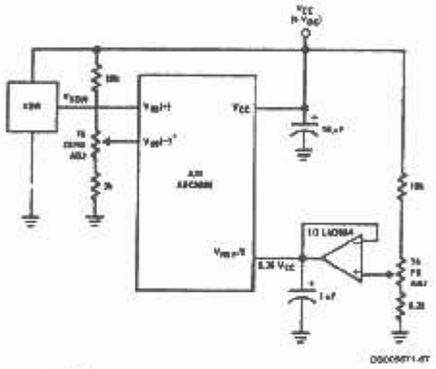


*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

µP Interface for Free-Running A/D

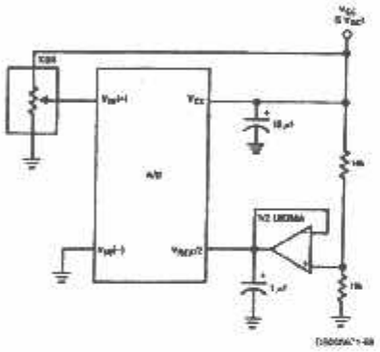


Operating with "Automotive" Ratiometric Transducers

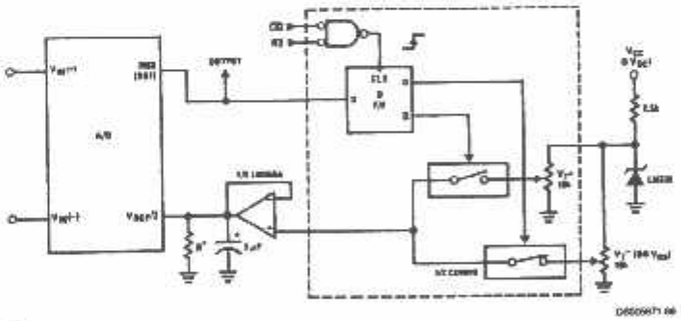


*$V_{IN}(-)=0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDCR} \leq 85\%$ of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



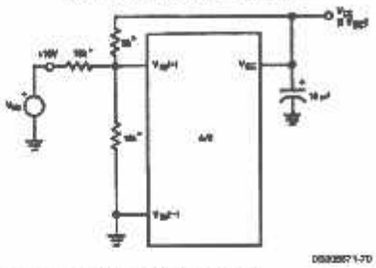
µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)



*See Figure 5 to select R value
DB7="1" for $V_{IN}(+) > V_{IN}(-)+(V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

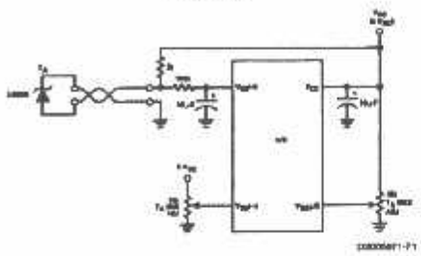
Typical Applications (Continued)

Handling ±10V Analog Inputs

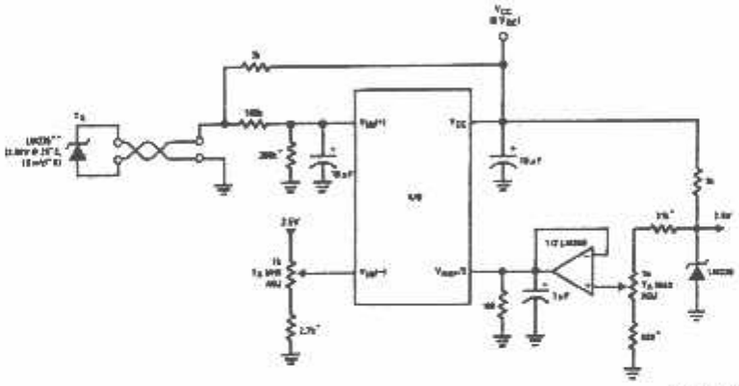


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



µP Interfaced Temperature-to-Digital Converter

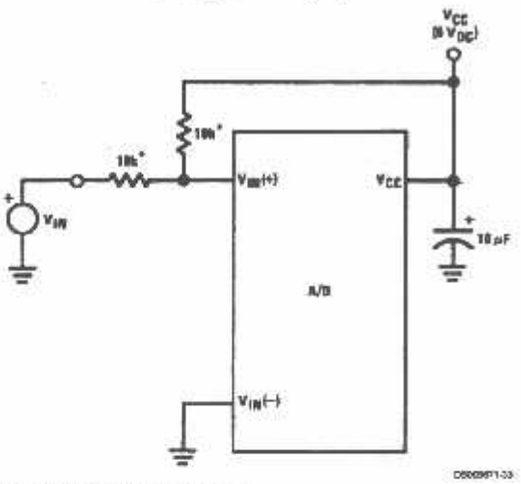


*Circuit values shown are for 0°C≤T_A≤+125°C

**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

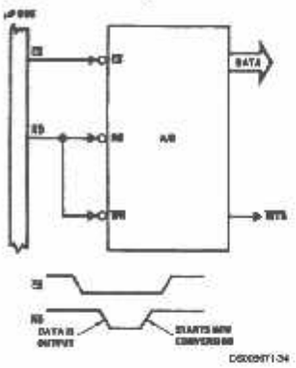
Typical Applications (Continued)

Handling ±5V Analog Inputs

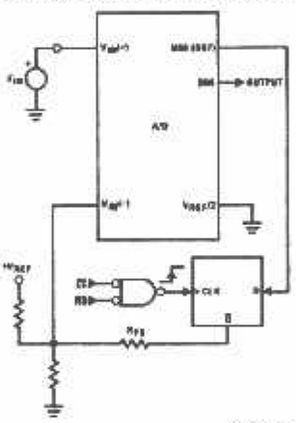


*Beckman Instruments #694-3-R10K resistor array

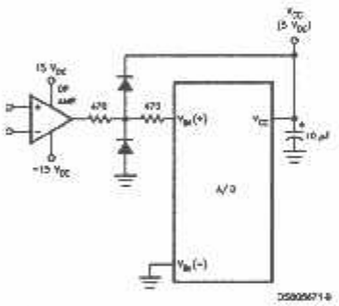
Read-Only Interface



µP Interfaced Comparator with Hysteresis



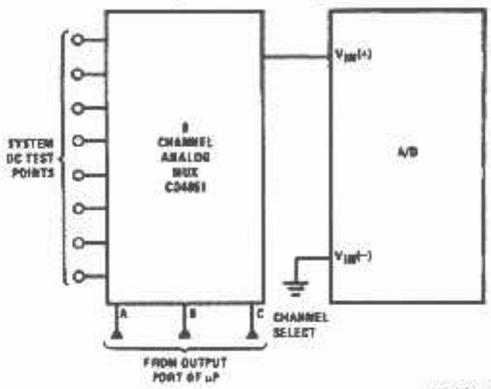
Protecting the Input



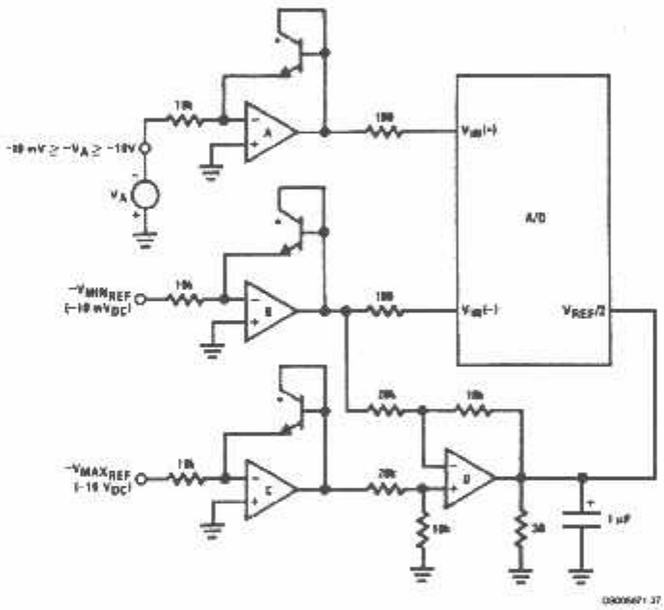
Diodes are 1N914

Typical Applications (Continued)

Analog Self-Test for a System



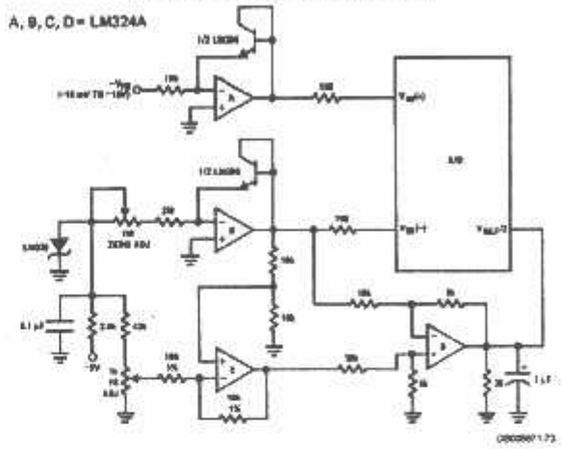
A Low-Cost, 3-Decade Logarithmic Converter



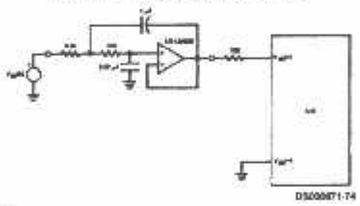
*LM389 transistors
A, B, C, D = LM324A quad op amp

Typical Applications (Continued)

3-Decade Logarithmic A/D Converter



Noise Filtering the Analog Input

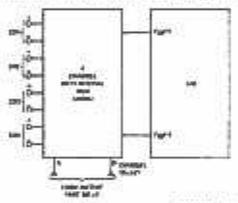


f_C = 20 Hz

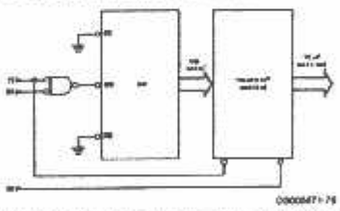
Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter

Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

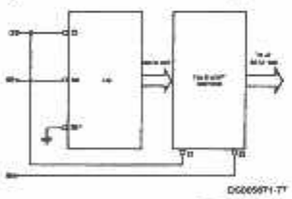


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

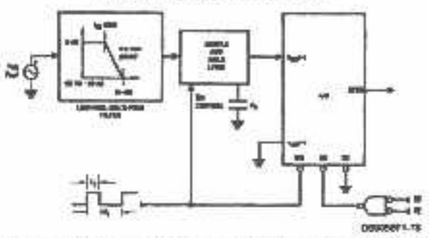
Increasing Bus Drive and/or Reducing Time on Bus



*Allows output data to set-up at falling edge of $\overline{CS}$

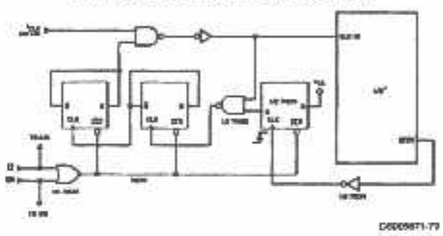
Typical Applications (Continued)

Sampling an AC Input Signal



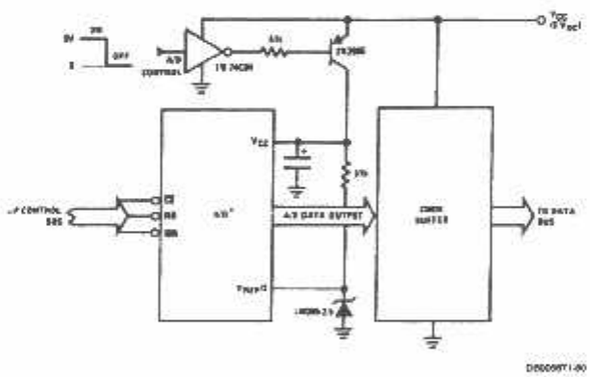
Note 11: Oversample whenever possible (keep fs > 2[f+60]) to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.
Note 12: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



*Use ADC0801, 02, 03 or 05 for lowest power consumption.
Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.
Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend ±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Functional Description (Continued)

Figure 2 shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 3* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.

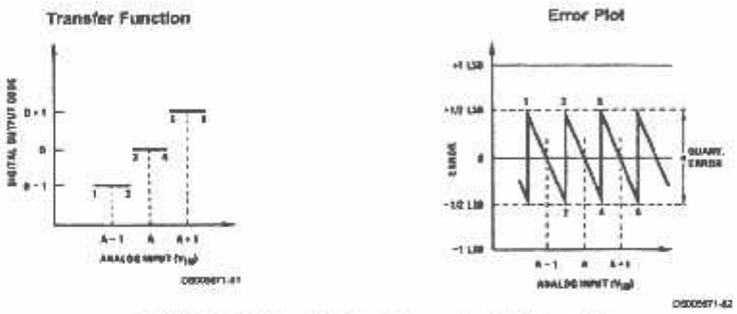


FIGURE 1. Clarifying the Error Specs of an A/D Converter Accuracy=±0 LSB: A Perfect A/D

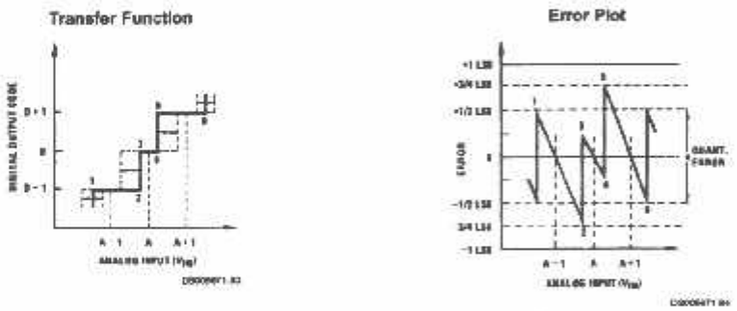


FIGURE 2. Clarifying the Error Specs of an A/D Converter Accuracy=±¼ LSB

Functional Description (Continued)

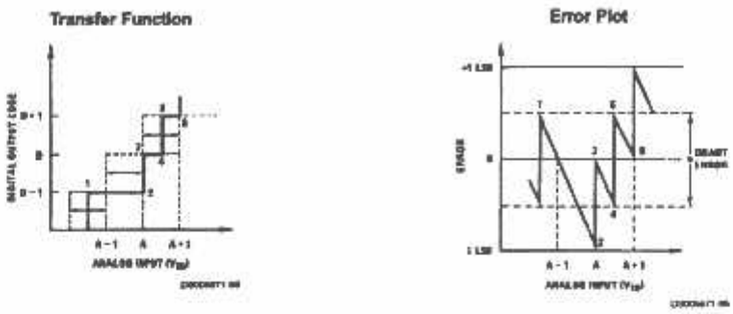


FIGURE 3. Clarifying the Error Specs of an A/D Converter
Accuracy=±½ LSB

2.0 FUNCTIONAL DESCRIPTION

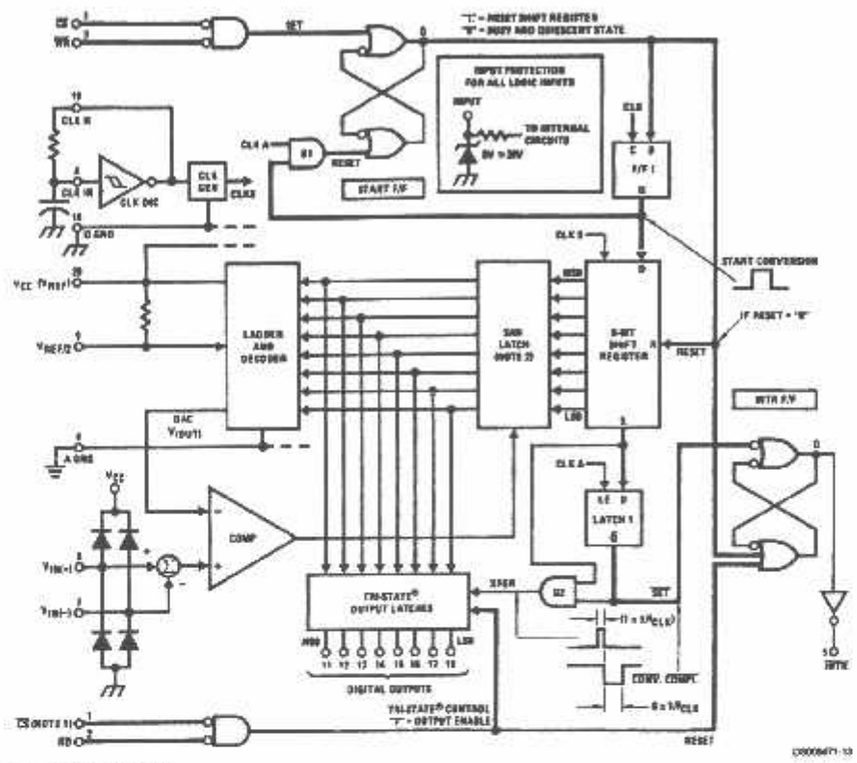
The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ =0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 4*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

Functional Description (Continued)



Note 13: $\overline{CS}$ shown twice for clarity.

Note 14: SAR = Successive Approximation Register

FIGURE 4. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low — see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

Functional Description (Continued)

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_{e}(MAX) = (V_P)\,(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right)$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}\,(f_{CLK})]}{(2\pi f_{cm})\,(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})\,(640 \times 10^{3})}{(6.28)\,(60)\,(4.5)}$$

which gives

V_P=1.9V.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

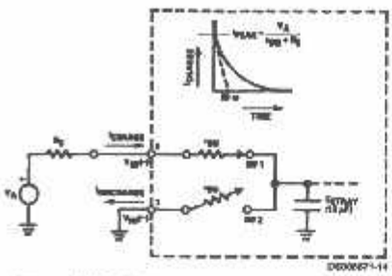
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3 1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 5*.



r_{ON} of SW 1 and SW 2 = 5 kΩ

$r_{ON} C_{STRAY}$ = 5 kΩ x 12 pF = 60 ns

FIGURE 5. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of V_{CC}+50 mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 µA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 µF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A

Functional Description (Continued)

100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 6*.

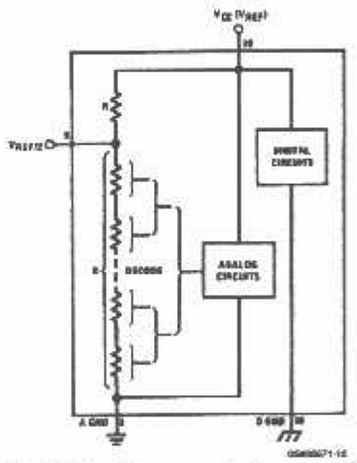


FIGURE 6. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

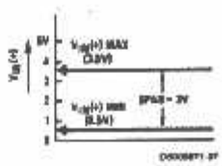
An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 7*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

2.4.2 Reference Accuracy Requirements

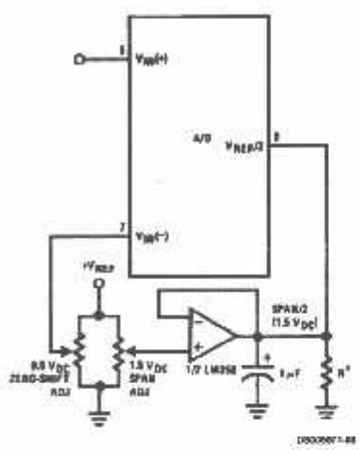
The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$. Other temperature range parts are also available.

Functional Description (Continued)



a) Analog Input Signal Example



*Add if $V_{REF}/2 \leq 1\ V_{DC}$ with LM358 to draw 3 mA to ground

b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 3.5V (Digital Out=FF_{HEX})

FIGURE 7. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB=analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX}=The high end of the analog input range

and

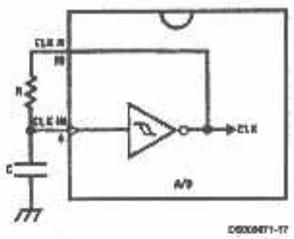
V_{MIN}=the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 8*.

Functional Description (Continued)



$$f_{CLK} \approx \frac{1}{1.1\,RC}$$

$R \approx 10\ k\Omega$

FIGURE 8. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 µF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 9*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120–1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). *Table 1* shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in *Table 1*, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of **1011** 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

Functional Description (Continued)

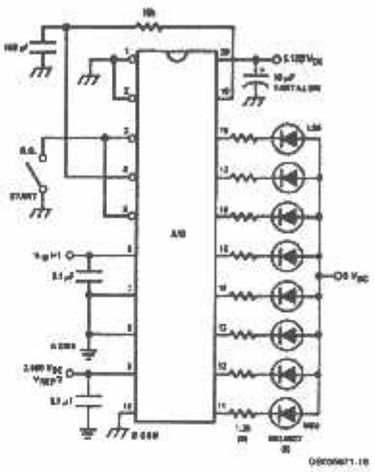


FIGURE 9. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A–C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 11*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 12*.

Functional Description (Continued)

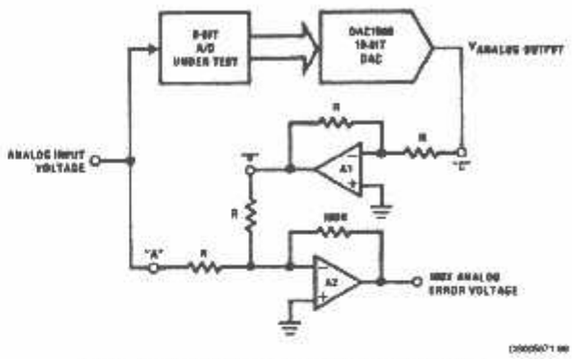


FIGURE 10. A/D Tester with Analog Error Output

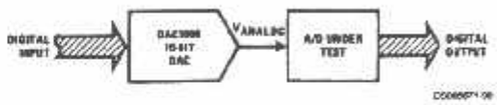


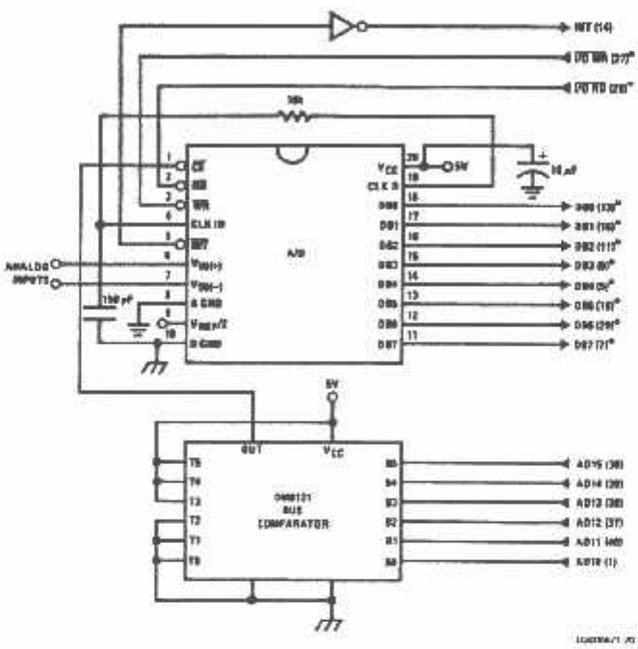
FIGURE 11. Basic "Digital" A/D Tester

TABLE 1. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY				FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2=2.560\ V_{DC}$	
					MS GROUP	LS GROUP	VMS GROUP (Note 15)	VLS GROUP (Note 15)
F	1	1	1	1	15/16	15/256	4.800	0.300
E	1	1	1	0	7/8	7/128	4.480	0.280
D	1	1	0	1	13/16	13/256	4.160	0.260
C	1	1	0	0	3/4	3/64	3.840	0.240
B	1	0	1	1	11/16	11/256	3.520	0.220
A	1	0	1	0	5/8	5/128	3.200	0.200
9	1	0	0	1	9/16	9/256	2.880	0.180
8	1	0	0	0	1/2	1/32	2.560	0.160
7	0	1	1	1	7/16	7/256	2.240	0.140
6	0	1	1	0	3/8	3/128	1.920	0.120
5	0	1	0	1	5/16	2/256	1.600	0.100
4	0	1	0	0	1/4	1/64	1.280	0.080
3	0	0	1	1	3/16	3/256	0.960	0.060
2	0	0	1	0	1/8	1/128	0.640	0.040
1	0	0	0	1	1/16	1/256	0.320	0.020
0	0	0	0	0			0	0

Note 15: Display Output = VMS Group + VLS Group

Functional Description (Continued)



Note 16: *Pin numbers for the DP8228 system controller, others are INS8080A.

Note 17: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 12. ADC0801_INS8080A CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 12* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:      JMP     LD DATA
  .         .           .
  .         .           .
0100    21 00 02    START:      LXI H 0200H     ;HL pair will point to
                                                ;data storage locations
0103    31 00 04    RETURN:     LXI SP 0400H    ;Initialize stack pointer (Note 1)
0106    7D                      MOV A, L        ;Test # of bytes entered
0107    FE 0F                   CPI 0F H        ;If #=16, JMP to
0109    CA 13 01                JZ CONT         ;user program
010C    D3 E0                   OUT E0 H        ;Start A/D
010E    FB                      EI              ;Enable interrupt
010F    00          LOOP:       NOP             ;Loop until end of
0110    C3 0F 01                JMP LOOP        ;conversion
0113      .         CONT:         .
  .       .           .           .
  .       .         (User program to            .
  .       .         process data)               .
  .       .           .           .
  .       .           .           .
0300    DB E0       LD DATA:    IN E0 H         ;Load data into accumulator
0302    77                      MOV M, A        ;Store data
0303    23                      INX H           ;Increment storage pointer
0304    C3 03 01                JMP RETURN
```

Note 18: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 19: All address used were arbitrarily chosen

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 12* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs — one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 13*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

Functional Description (Continued)

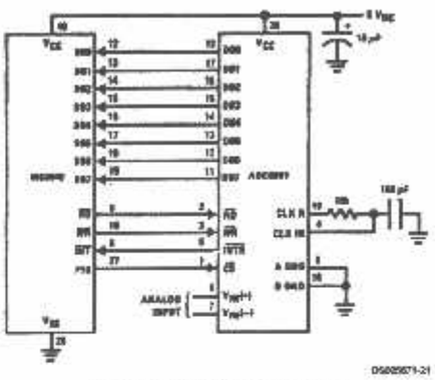


FIGURE 13. INS8048 Interface

SAMPLE PROGRAM FOR *Figure 13* INS8048 INTERFACE

```
04 10                  JMP     10H          ;Program starts at addr 10
                       ORG     3H
04 50                  JMP     50H          ;Interrupt jump vector
                       ORG     10H          ;Main program
99 FE                  ANL     P1, #0FEH    ;Chip select
81                     MOVX    A, @R1       ;Read in the 1st data
                                            ;to reset the intr
89 01        START:    ORL     P1, #1       ;Set port pin high
B8 20                  MOV     R0, #20H     ;Data address
B9 FF                  MOV     R1, #0FFH    ;Dummy address
BA 10                  MOV     R2, #10H     ;Counter for 16 bytes
23 FF        AGAIN:    MOV     A, #0FFH     ;Set ACC for intr loop
99 FE                  ANL     P1, #0FEH    ;Send CS (bit 0 of P1)
91                     MOVX    @R1, A       ;Send WR out
05                     EN      I            ;Enable interrupt
96 21        LOOP:     JNZ     LOOP         ;Wait for interrupt
EA 1E                  DJNZ    R2, AGAIN    ;If 16 bytes are read
00                     NOP                  ;go to user's program
00                     NOP
                       ORG     50H
81           INDATA:   MOVX    A, @R1       ;Input data, CS still low
A0                     MOV     @R0, A       ;Store in memory
18                     INC     R0           ;Increment storage counter
89 01                  ORL     P1, #1       ;Reset CS signal
27                     CLR     A            ;Clear ACC to get out of
93                     RETR                 ;the interrupt loop
```

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 14*.

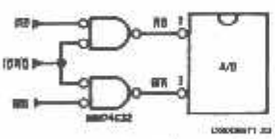


FIGURE 14. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) dur-

Functional Description (Continued)

ing I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived form the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 15* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4}/5$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 16* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

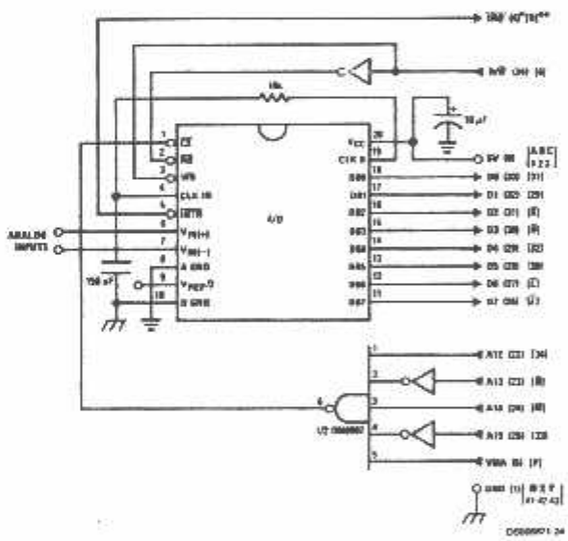
A sample interface program equivalent to the previous one is shown below *Figure 16*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 17*.



Note 20: Numbers in parentheses refer to MC6800 CPU pin out.

Note 21: Number or letters in brackets refer to standard M6800 system common bus code.

FIGURE 15. ADC0801-MC6800 CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 15* ADC0801-MC6800 CPU INTERFACE

```
0010  DF 36    DATAIN  STX   TEMP2   ; Save contents of X
0012  CE 00 2C        LDX   #$002C  ; Upon IRQ low CPU
0015  FF FF F8        STX   $FFF8   ; jumps to 002C
0018  B7 50 00        STAA  $5000   ; Start ADC0801
001B  0E              CLI
001C  3E      CONVRT  WAI           ; Wait for interrupt
001D  DE 34           LDX   TEMP1
001F  8C 02 0F        CPX   #$020F  ; Is final data stored?
0022  27 14           BEQ   ENDF
0024  B7 50 00        STAA  $5000   ; Restarts ADC0801
0027  08              INX
0028  DF 34           STX   TEMP1
002A  20 F0           BRA   CONVRT
002C  DE 34   INTHPT  LDX   TEMP1
002E  B6 50 00        LDAA  $5000   ; Read data
0031  A7 00           STAA  X       ; Store it at X
0033  3B              RTI
0034  02 00   TEMP1   FDB   $0200   ; Starting address for
                                    ; data storage
0036  00 00   TEMP2   FDB   $0000
0038  CE 02 00 ENDF   LDX   #$0200  ; Reinitialize TEMP1
003B  DF 34           STX   TEMP1
003D  DE 36           LDX   TEMP2
003F  39              RTS           ; Return from subroutine
                                    ; to user's program
```

Note 22: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

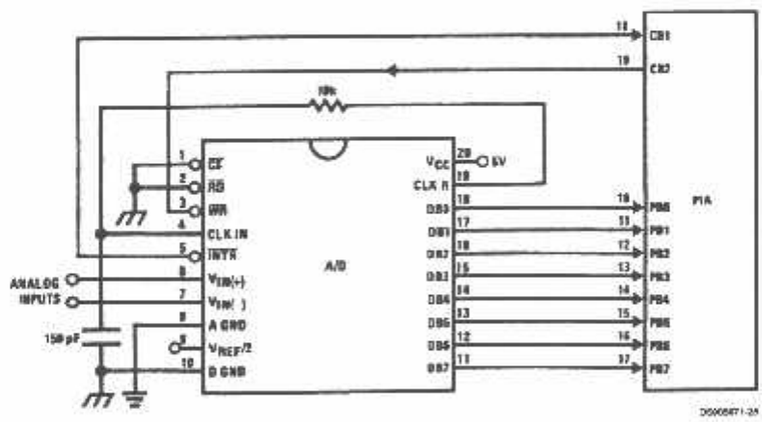


FIGURE 16. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 16* ADC0801–MC6820 PIA INTERFACE

```
0010  CE 00 38   DATAIN  LDX   #$0038   ; Upon IRQ low CPU
0013  FF FF F8           STX   $FFF8   ; jumps to 0038
0016  B6 80 06           LDAA  PIAORB  ; Clear possible IRQ flags
0019  4F                 CLRA
001A  B7 80 07           STAA  PIACRB
001D  B7 80 06           STAA  PIAORB  ; Set Port B as input
0020  0E                 CLI
0021  C6 34              LDAB  #$34
0023  86 3D              LDAA  #$3D
0025  F7 80 07   CONVRT  STAB  PIACRB  ; Starts ADC0801
0028  B7 80 07           STAA  PIACRB
002B  3E                 WAI           ; Wait for interrupt
002C  DE 40              LDX   TEMP1
002E  8C 02 0F           CPX   #$020F  ; Is final data stored?
0031  27 0F              BEQ   ENDP
0033  08                 INX
0034  DF 40              STX   TEMP1
0036  20 ED              BRA   CONVRT
0038  DE 40   INTRPT     LDX   TEMP1
003A  B6 80 06           LDAA  PIAORB  ; Read data in
003D  A7 00              STAA  X       ; Store it at X
003F  3B                 RTI
0040  02 00   TEMP1      FDB   $0200   ; Starting address for
                                       ; data storage
0042  CE 02 00   ENDP    LDX   #$0200  ; Reinitialize TEMP1
0045  DF 40              STX   TEMP1
0047  39                 RTS           ; Return from subroutine
                PIAORB   EQU   $8006   ; To user's program
                PIACRB   EQU   $8007
```

D005671-A2

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

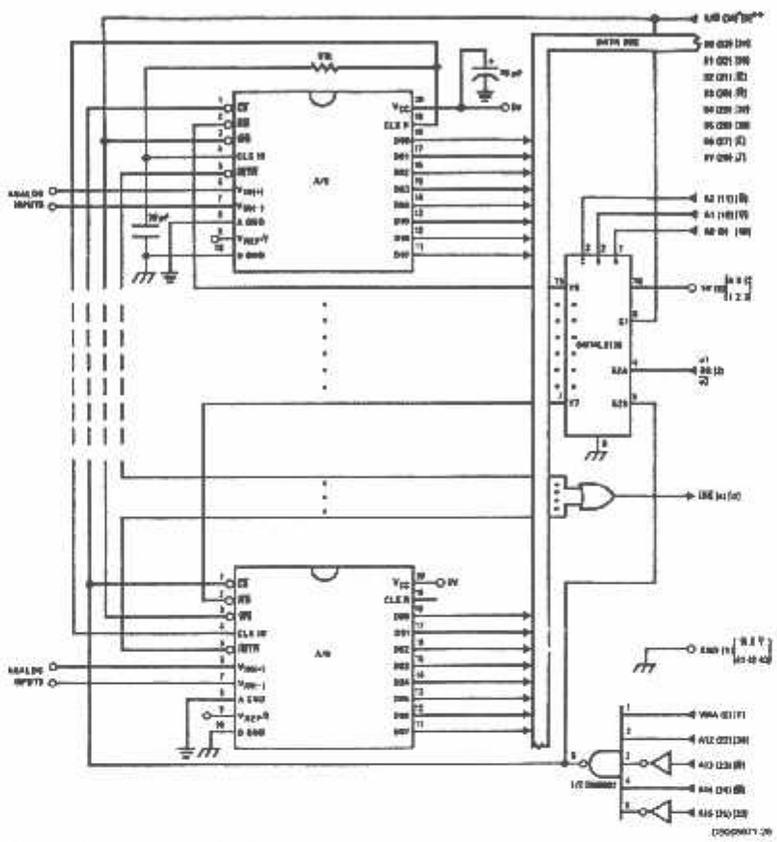
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)



Note 23: Numbers in parentheses refer to MC6800 CPU pin out.

Note 24: Numbers of letters in brackets refer to standard M6800 system common bus code.

FIGURE 17. Interfacing Multiple A/Ds in an MC6800 System

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE	MNEMONICS			COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE	MNEMONICS			COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

Note 25: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 18* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 µV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

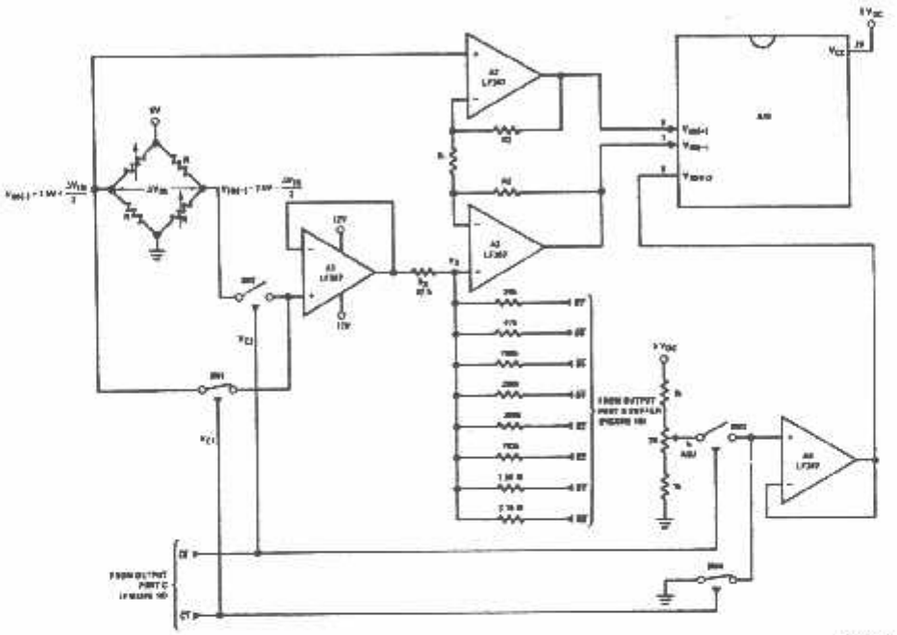
where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programmable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 19*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_x increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on

Functional Description (Continued)

any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 µV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



Note 26: R2 = 49.5 R1

Note 27: Switches are LMC13334 CMOS analog switches.

Note 28: The 9 resistors used in the auto-zero section can be ±5% tolerance

FIGURE 18. Gain of 100 Differential Transducer Preamp

Functional Description (Continued)

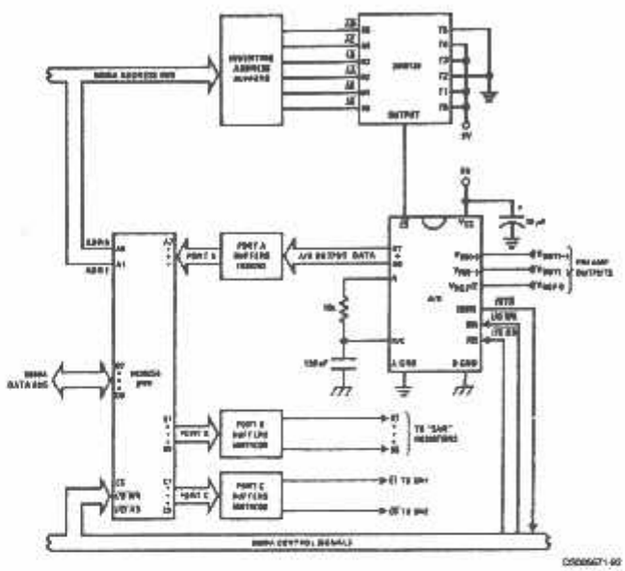


FIGURE 19. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 20*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input ($V_{IN}(-) \geq V_{IN}(+)$). Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 21*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 22* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

Functional Description (Continued)

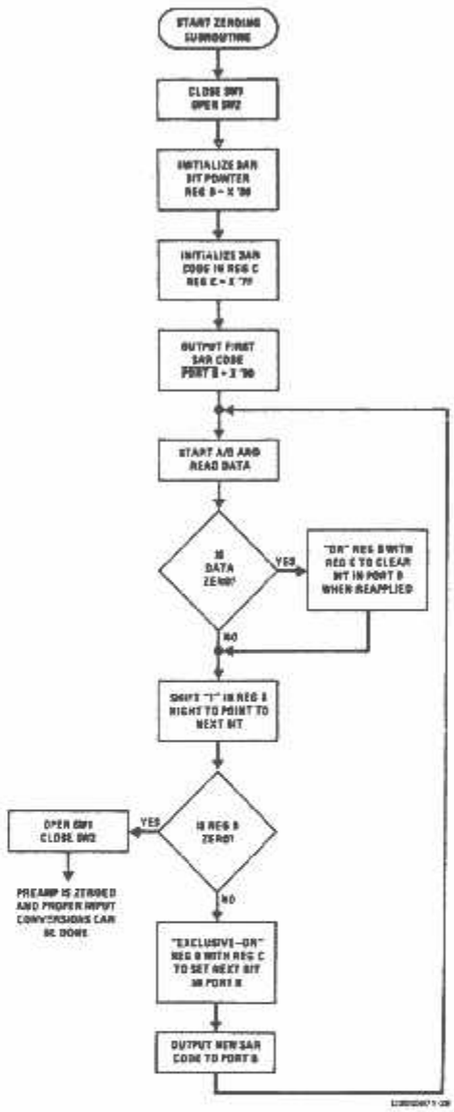


FIGURE 20. Flow Chart for Auto-Zero Routine

Functional Description (Continued)

```
3D00  3E90    MVI 90
3D02  D3E7    Out Control Port                    ;Program PPI
3D04  2601    MVI H 01          Auto-Zero Subroutine
3D06  7C      MOV A,H
3D07  D3E6    OUT C                              ;Close SW1 open SW2
3D09  0680    MVI B 80                           ;Initialize SAR bit pointer
3D0B  3E7F    MVI A 7F                           ;Initialize SAR code
3D0D  4F      MOV C,A           Return
3D0E  D3E5    OUT B                              ;Port B = SAR code
3D10  31AA3D  LXI SP 3DAA       Start            ;Dimension stack pointer
3D13  D3E4    OUT A                              ;Start A/D
3D15  FB      IE
3D16  00      NOP               Loop             ;Loop until INT asserted
3D17  C3163D  JMP Loop
3D1A  7A      MOV A,D           Auto-Zero
3D1B  C600    ADI 00
3D1D  CA2D3D  JZ Set C                           ;Test A/D output data for zero
3D20  78      MOV A,B           Shift B
3D21  F600    ORI 00                             ;Clear carry
3D23  1F      RAR                                ;Shift "1" in B right one place
3D24  FE00    CPI 00                             ;Is B zero? If yes last
3D26  CA373D  JZ Done                            ;approximation has been made
3D29  47      MOV B,A
3D2A  C3333D  JMP New C
3D2D  79      MOV A,C           Set C
3D2E  B0      ORA B                              ;Set bit in C that is in same
3D2F  4F      MOV C,A                            ;position as "1" in B
3D30  C3203D  JMP Shift B
3D33  A9      XRA C             New C            ;Clear bit in C that is in
3D34  C30D3D  JMP Return                         ;same position as "1" in B
3D37  47      MOV B,A           Done             ;then output new SAR code.
3D38  7C      MOV A,H                            ;Open SW1, close SW2 then
3D39  EE03    XRI 03                             ;proceed with program. Preamp
3D3B  D3E6    OUT C                              ;is now zeroed.
3D3D          *                 Normal
              *
              *
              Program for processing
              proper data values
3C3D  DBE4    IN A              Read A/D Subroutine  ;Read A/D data
3C3F  EEFF    XRI FF                             ;Invert data
3C41  57      MOV D,A
3C42  78      MOV A,B                            ;Is B Reg = 0? If not stay
3C43  E6FF    ANI FF                             ;in auto zero subroutine
3C45  C21A3D  JNZ Auto-Zero
3C48  C33D3D  JMP Normal
```

TL/H/5607-46

Note 29: All numerical values are hexadecimal representations.

FIGURE 21. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

- It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.
- The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.
- A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.
- The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.
- The peripherals of concern are mapped into I/O space with the following port assignments:

Functional Description (Continued)

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

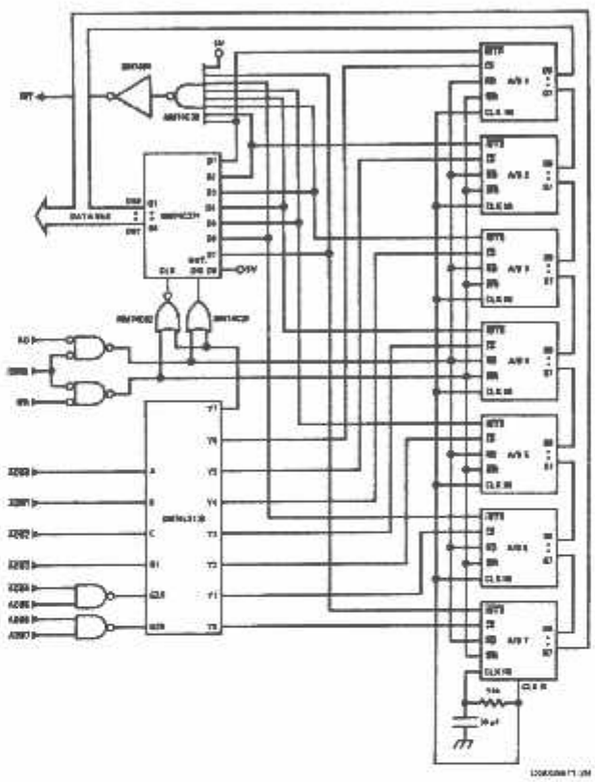


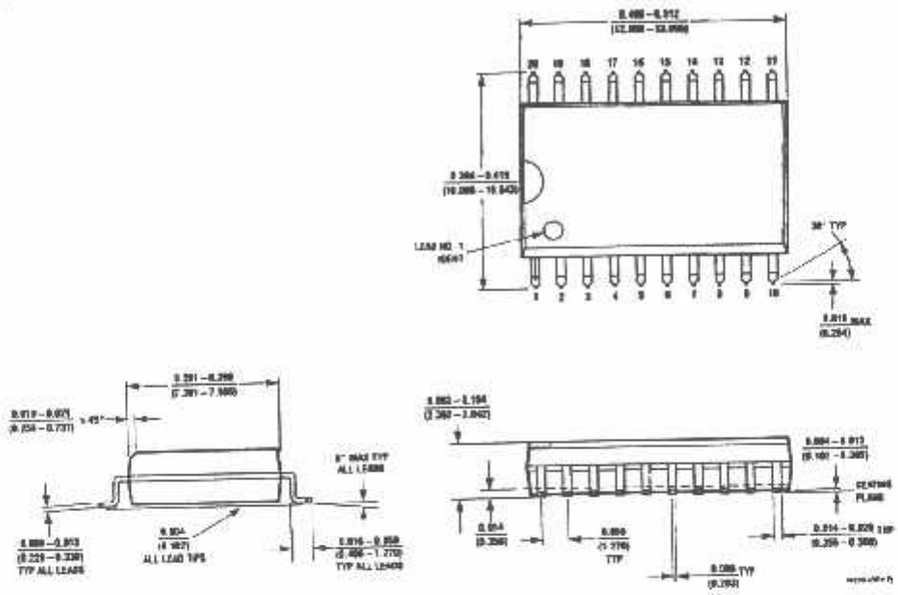
FIGURE 22. Multiple A/Ds with Z-80 Type Microprocessor

Functional Description (Continued)

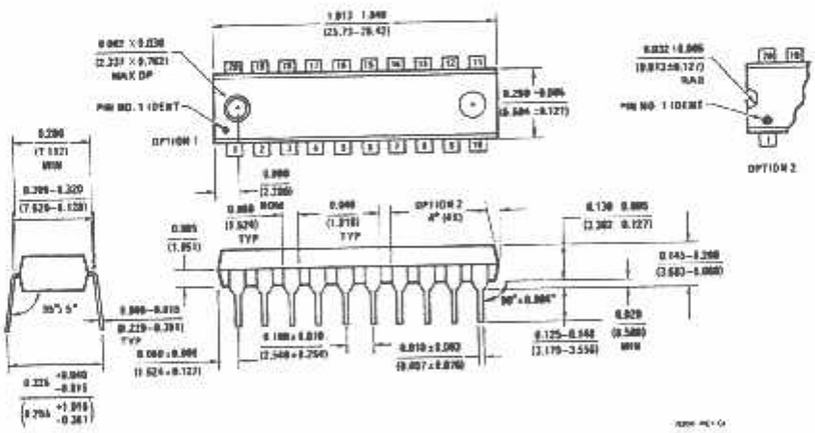
INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE		SOURCE STATEMENT	COMMENT
0038	E5		PUSH HL	;Save contents of all registers affected by
0039	C5		PUSH BC	;this subroutine.
003A	F5		PUSH AF	;Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL),X3E00	;Initialize memory pointer where data will be stored.
003E	0E 01		LD C, X01	;C register will be port ADDR of A/D converters.
0040	D300		OUT X00, A	;Load peripheral status word into 8-bit latch.
0042	DB00		IN A, X00	;Load status word into accumulator.
0044	47		LD B,A	;Save the status word.
0045	79	TEST	LD A,C	;Test to see if the status of all A/D's have
0046	FE 08		CP, X08	;been checked. If so, exit subroutine
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	;Test a single bit in status word by looking for
004C	1F		RRA	;a "1" to be rotated into the CARRY (an $\overline{INT}$
004D	47		LD B,A	;is loaded as a "1"). If CARRY is set then load
004E	DA 5500		JPC, LOAD	;contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	;If CARRY is not set, increment C register to point
0052	C3 4500		JP,TEST	;to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	;Read data from interrupting A/D and invert
0057	EE FF		XOR FF	;the data.
0059	77		LD (HL),A	;Store the data
005A	2C		INC L	
005B	71		LD (HL),C	;Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP,NEXT	;Test next bit in status word.
0060	F1	DONE	POP AF	;Re-establish all registers as they were
0061	C1		POP BC	;before the interrupt.
0062	E1		POP HL	
0063	C9		RET	;Return to original program

Physical Dimensions inches (millimeters) unless otherwise noted



SO Package (M)
Order Number ADC0802LCWM or ADC0804LCWM
NS Package Number M20B



Molded Dual-In-Line Package (N)
Order Number ADC0801LCN, ADC0802LCN,
ADC0803LCN, ADC0804LCN or ADC0805LCN
NS Package Number N20A

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

National Semiconductor

June 1989

54LS04/DM54LS04/DM74LS04 Hex Inverting Gates

General Description

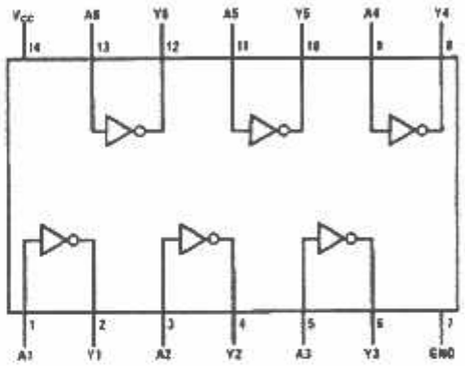
This device contains six independent gates each of which performs the logic INVERT function.

Features

- Alternate Military/Aerospace device (54LS04) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6345–1

Order Number 54LS04DMQB, 54LS04FMQB, 54LS04LMQB, DM54LS04J, DM54LS04W, DM74LS04M or DM74LS04N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

  RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM54LS04			DM74LS04			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

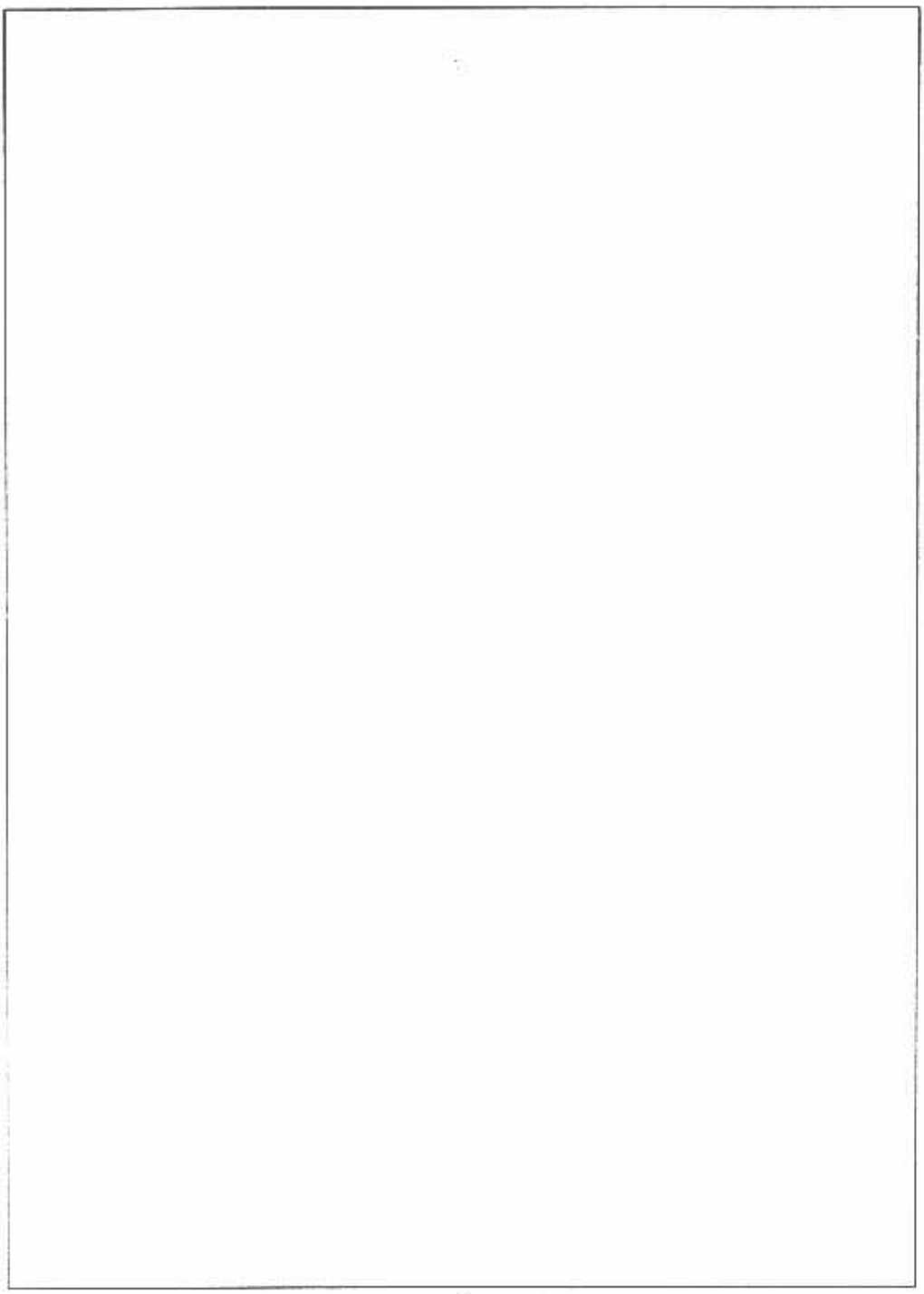
Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.2	2.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3.6	6.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

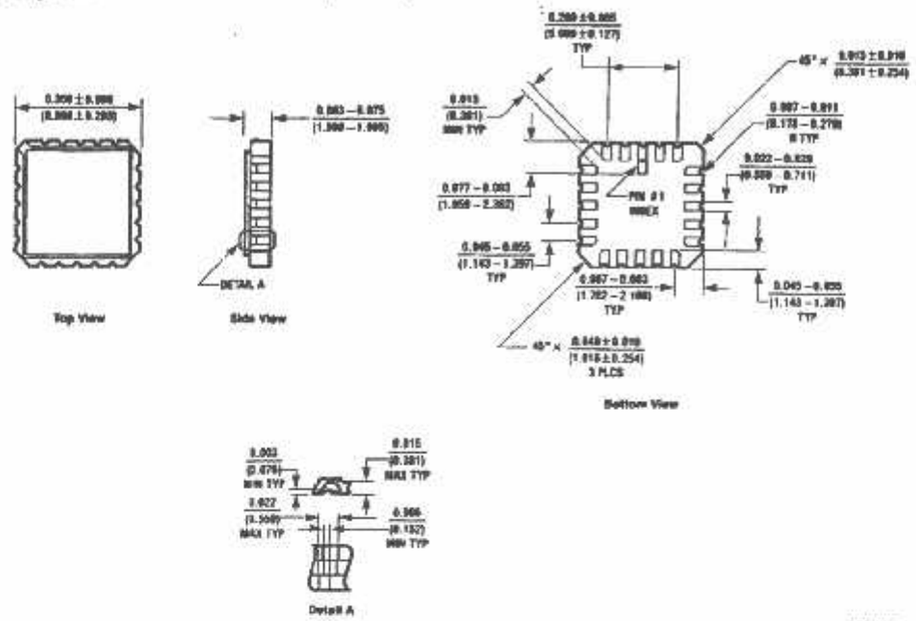
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

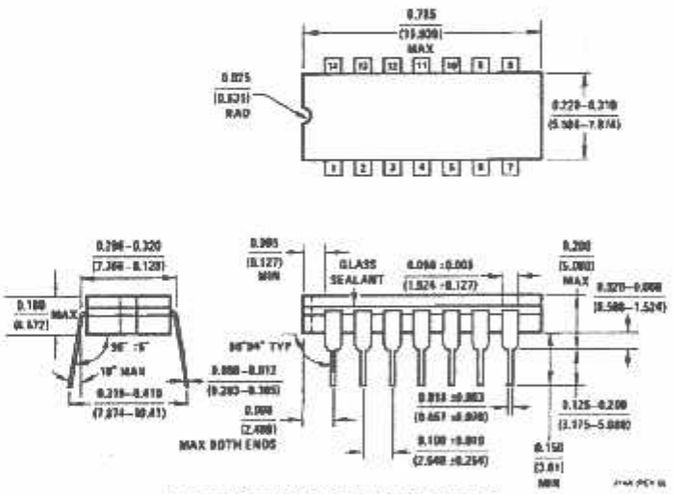
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.



Physical Dimensions inches (millimeters)

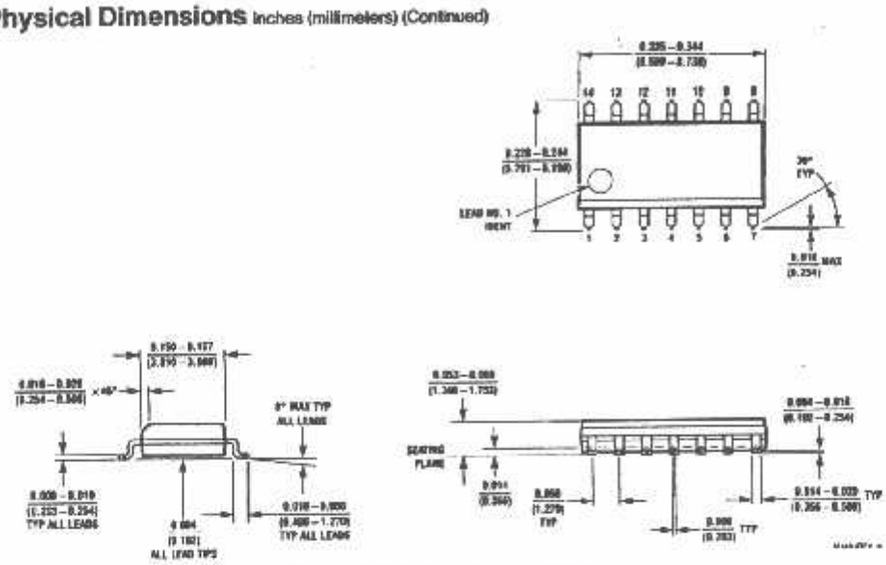


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS04LMQB
NS Package Number E20A

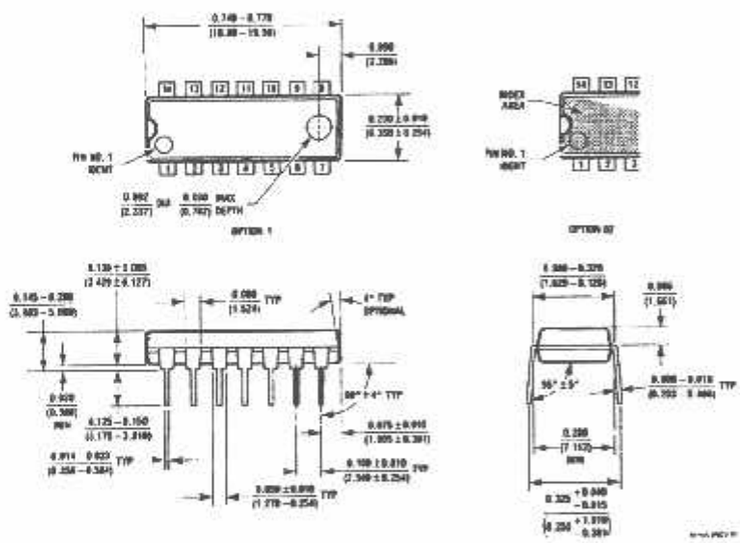


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS04DMQB or DM54LS04J
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)

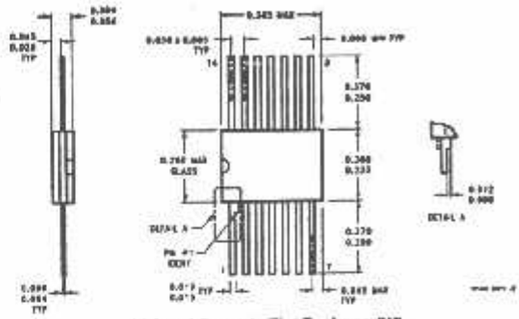


14-Lead Small Outline Molded Package (M)
Order Number DM74LS04M
NS Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS04N
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS04FMQB or DM54LS04W
NS Package Number W14B

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

Interfacing the Standard Parallel Port

Table of Contents

Introduction to Parallel Ports

The Parallel Port is the most commonly used port for interfacing home made projects. This port will allow the input of up to 9 bits or the output of 12 bits at any one given time, thus requiring minimal external circuitry to implement many simpler tasks. The port is composed of 4 control lines, 5 status lines and 8 data lines. It's found commonly on the back of your PC as a D-Type 25 Pin female connector. There may also be a D-Type 25 pin male connector. This will be a serial RS-232 port and thus, is a totally incompatible port.

Newer Parallel Port's are standardized under the IEEE 1284 standard first released in 1994. This standard defines 5 modes of operation which are as follows,

1. Compatibility Mode.
2. Nibble Mode. *(Protocol not Described in this Document)*
3. Byte Mode. *(Protocol not Described in this Document)*
4. EPP Mode *(Enhanced Parallel Port).*
5. ECP Mode *(Extended Capabilities Port).*

The aim was to design new drivers and devices which were compatible with each other and

also backwards compatible with the Standard Parallel Port (SPP). Compatibility, Nibble & Byte modes use just the standard hardware available on the original Parallel Port cards while EPP & ECP modes require additional hardware which can run at faster speeds, while still being downwards compatible with the Standard Parallel Port.

Compatibility mode or "Centronics Mode" as it is commonly known, can only send data in the forward direction at a typical speed of 50 kbytes per second but can be as high as 150+ kbytes a second. In order to receive data, you must change the mode to either Nibble or Byte mode. Nibble mode can input a nibble *(4 bits)* in the reverse direction. E.g. from device to computer. Byte mode uses the Parallel's bi-directional feature *(found only on some cards)* to input a byte *(8 bits)* of data in the reverse direction.

Extended and Enhanced Parallel Ports use additional hardware to generate and manage handshaking. To output a byte to a printer (or anything in that matter) using compatibility mode, the software must.

1. *Write the byte to the Data Port.*
2. *Check to see is the printer is busy. If the printer is busy, it will not accept any data, thus any data which is written will be lost.*
3. *Take the Strobe (Pin 1) low. This tells the printer that there is the correct data on the data lines. (Pins 2-9)*
4. *Put the strobe high again after waiting approximately 5 microseconds after putting the strobe low. (Step 3)*

This limits the speed at which the port can run at. The EPP & ECP ports get around this by letting the hardware check to see if the printer is busy and generate a strobe and /or appropriate handshaking. This means only one I/O instruction need to be performed, thus increasing the speed. These ports can output at around 1-2 megabytes per second. The ECP port also has the advantage of using DMA channels and FIFO buffers, thus data can be shifted around without using I/O instructions.

Hardware Properties

On the next page is a table of the "Pin Outs" of the D-Type 25 Pin connector and the Centronics 34 Pin connector. The D-Type 25 pin connector is the most common connector found on the Parallel Port of the computer, while the Centronics Connector is commonly found on printers. The IEEE 1284 standard however specifies 3 different connectors for use with the Parallel Port. The first one, 1284 Type A is the D-Type 25 connector found on the back of most computers. The 2nd is the 1284 Type B which is the 36 pin Centronics Connector found on most printers.

IEEE 1284 Type C however, is a 36 conductor connector like the Centronics, but smaller. This connector is claimed to have a better clip latch, better electrical properties and is easier to assemble. It also contains two more pins for signals which can be used to see whether the other device connected,

has power. 1284 Type C connectors are recommended for new designs, so we can look forward on seeing these new connectors in the near future.

Pin No (D-Type 25)	Pin No (Centronics)	SPP Signal	Direction In/out	Register	Hardware Inverted
1	1	nStrobe	In/Out	Control	Yes
2	2	Data 0	Out	Data	
3	3	Data 1	Out	Data	
4	4	Data 2	Out	Data	
5	5	Data 3	Out	Data	
6	6	Data 4	Out	Data	
7	7	Data 5	Out	Data	
8	8	Data 6	Out	Data	
9	9	Data 7	Out	Data	
10	10	nAck	In	Status	
11	11	Busy	In	Status	Yes
12	12	Paper-Out PaperEnd	In	Status	
13	13	Select	In	Status	
14	14	nAuto-Linefeed	In/Out	Control	Yes
15	32	nError / nFault	In	Status	
16	31	nInitialize	In/Out	Control	
17	36	nSelect-Printer nSelect-In	In/Out	Control	Yes
18 - 25	19-30	Ground	Gnd		

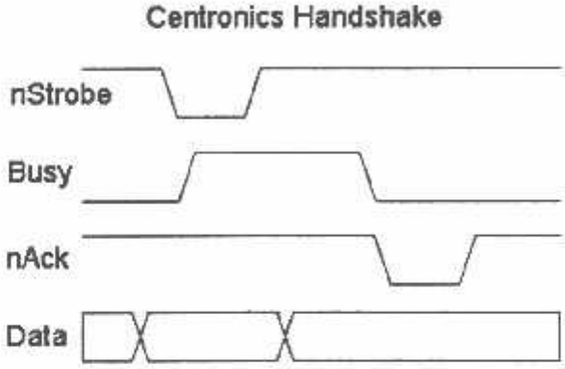
Table 1. Pin Assignments of the D-Type 25 pin Parallel Port Connector.

The above table uses "n" in front of the signal name to denote that the signal is active low. e.g. nError. If the printer has occurred an error then this line is low. This line normally is high, should the printer be functioning correctly. The "Hardware Inverted" means the signal is inverted by the Parallel card's hardware. Such an example is the Busy line. If +5v (Logic 1) was applied to this pin and the status register read, it would return back a 0 in Bit 7 of the Status Register.

The output of the Parallel Port is normally TTL logic levels. The voltage levels are the easy part. The current you can sink and source varies from port to port. Most Parallel Ports implemented in ASIC, can sink and source around 12mA. However these are just some of the figures taken from Data sheets, Sink/Source 6mA, Source 12mA/Sink 20mA, Sink 16mA/Source 4mA, Sink/Source 12mA. As you can see they vary quite a bit. The best bet is to use a buffer, so the least current is drawn from the Parallel Port.

Centronics?

Centronics is an early standard for transferring data from a host to the printer. The majority of printers use this handshake. This handshake is normally implemented using a Standard Parallel Port under software control. Below is a simplified diagram of the 'Centronics' Protocol.



Data is first applied on the Parallel Port pins 2 to 7. The host then checks to see if the printer is busy. i.e. the busy line should be low. The program then asserts the strobe, waits a minimum of 1µS, and then de-asserts the strobe. Data is normally read by the printer/peripheral on the rising edge of the strobe. The printer will indicate that it is busy processing data via the Busy line. Once the printer has accepted data, it will acknowledge the byte by a negative pulse about 5µS on the nAck line.

Quite often the host will ignore the nAck line to save time. Latter in the Extended Capabilities Port, you will see a Fast Centronics Mode, which lets the hardware do all the handshaking for you. All the programmer must do is write the byte of data to the I/O port. The hardware will check to see if the printer is busy, generate the strobe. Note that this mode commonly doesn't check the nAck either.

Port Addresses

The Parallel Port has three commonly used base addresses. These are listed in table 2, below. The 3BCh base address was originally introduced used for Parallel Ports on early Video Cards. This address then disappeared for a while, when Parallel Ports were later removed from Video Cards. They has now reappeared as an option for Parallel Ports integrated onto motherboards, upon which their configuration can be changed using BIOS.

LPT1 is normally assigned base address 378h, while LPT2 is assigned 278h. However this may not always be the case as explained later. 378h & 278h have always been commonly used for Parallel Ports. The lower case h denotes that it is in hexadecimal. These addresses may change from machine to machine.

Address	Notes:
3BCh - 3BFh	Used for Parallel Ports which were incorporated in to Video Cards and now, commonly an option for Ports controlled by BIOS. - Doesn't support ECP addresses.
378h - 37Fh	Usual Address For LPT 1
278h - 27Fh	Usual Address For LPT 2

Table 2 Port Addresses

When the computer is first turned on, BIOS (Basic Input/Output System) will determine the number of ports you have and assign device labels LPT1, LPT2 & LPT3 to them. BIOS first looks at address 3BCh. If a Parallel Port is found here, it is assigned as LPT1, then it searches at location 378h. If a Parallel card is found there, it is assigned the next free device label. This would be LPT1 if a card wasn't found at 3BCh or LPT2 if a card was found at 3BCh. The last *port of call*, is 278h and follows the same procedure than the other two ports. Therefore it is possible to have a LPT2 which is at 378h and not at the expected address 278h.

What can make this even confusing, is that some manufacturers of Parallel Port Cards, have jumpers which allow you to set your Port to LPT1, LPT2, LPT3. Now what address is LPT1? - On the majority of cards LPT1 is 378h, and LPT2, 278h, but some will use 3BCh as LPT1, 378h as LPT1 and 278h as LPT2. *Life wasn't meant to be easy.*

The assigned devices LPT1, LPT2 & LPT3 should not be a worry to people wishing to interface devices to their PC's. Most of the time the base address is used to interface the port rather than LPT1 etc. However should you want to find the address of LPT1 or any of the Line PrinTer Devices, you can use a lookup table provided by BIOS. When BIOS assigns addresses to your printer devices, it stores the address at specific locations in memory, so we can find them.

Start Address	Function
0000:0408	LPT1's Base Address
0000:040A	LPT2's Base Address
0000:040C	LPT3's Base Address
0000:040E	LPT4's Base Address (Note 1)

Table 3 - LPT Addresses in the BIOS Data Area

Note 1 : Address 0000:040E in the BIOS Data Area may be used as the Extended Bios Data Area in PS/2 and newer Bioses, and thus this field may be invalid.

The above table, table 3, shows the address at which we can find the Printer Port's addresses in the BIOS Data Area. Each address will take up 2 bytes. The following sample program in C, shows how you can read these locations to obtain the addresses of your printer ports.

```
#include <stdio.h>
#include <dos.h>

void main(void)
{
 unsigned int far *ptraddr;  /* Pointer to location of Port Addresses */
 unsigned int address;       /* Address of Port */
 int a;

 ptraddr=(unsigned int far *)0x00000408;

 for (a = 0; a < 3; a++)
   {
    address = *ptraddr;
    if (address == 0)
          printf("No port found for LPT%d \n",a+1);
    else
          printf("Address assigned to LPT%d is %Xh\n",a+1,address);
    *ptraddr++;
   }
}
```

Software Registers - Standard Parallel Port (SPP)

Offset	Name	Read/Write	Bit No.	Properties
Base + 0	Data Port	Write (Note-1)	Bit 7	Data 7 (Pin 9)
			Bit 6	Data 6 (Pin 8)
			Bit 5	Data 5 (Pin 7)
			Bit 4	Data 4 (Pin 6)
			Bit 3	Data 3 (Pin 5)
			Bit 2	Data 2 (Pin 4)
			Bit 1	Data 1 (Pin 3)
			Bit 0	Data 0 (Pin 2)

Table 4 Data Port

Note 1 : If the Port is bi-directional then Read and Write Operations can be performed on the Data Register.

The base address, usually called the Data Port or Data Register is simply used for outputting data on the Parallel Port's data lines (Pins 2-9). This register is normally a write only port. If you read from the port, you should get the last byte sent. However if your port is bi-directional, you can receive data on this address. See *Bi-directional Ports* for more detail.

Base + 1	Status Port	Read Only	Bit 7	Busy
			Bit 6	Ack
			Bit 5	Paper Out
			Bit 4	Select In
			Bit 3	Error
			Bit 2	IRQ (Not)
			Bit 1	Reserved
			Bit 0	Reserved

Table 5 Status Port

The Status Port (base address + 1) is a read only port. Any data written to this port will be ignored. The Status Port is made up of 5 input lines (Pins 10,11,12,13 & 15), a IRQ status register and two reserved bits. Please note that Bit 7 (Busy) is a active low input. E.g. If bit 7 happens to show a logic 0, this means that there is +5v at pin 11. Likewise with Bit 2. (nIRQ) If this bit shows a '1' then an interrupt has not occurred.

Base + 2	Control Port	Read/Write	Bit 7	Unused
			Bit 6	Unused
			Bit 5	Enable bi-directional Port
			Bit 4	Enable IRQ Via Ack Line
			Bit 3	Select Printer
			Bit 2	Initialize Printer (Reset)
			Bit 1	Auto Linefeed
			Bit 0	Strobe

Table 6 Control Port

The Control Port (base address + 2) was intended as a write only port. When a printer is attached to the Parallel Port, four "controls" are used. These are Strobe, Auto Linefeed, Initialize and Select Printer, all of which are inverted except Initialize.

The printer would not send a signal to initialize the computer, nor would it tell the computer to use auto linefeed. However these four outputs can also be used for inputs. If the computer has placed a pin high (e.g. +5v) and your device wanted to take it low, you would effectively short out the port, causing a conflict on that pin. Therefore these lines are "open collector" outputs *(or open drain for CMOS devices)*. This means that it has two states. A low state (0v) and a high impedance state (open circuit).

Normally the Printer Card will have internal pull-up resistors, but as you would expect, not all will. Some may just have open collector outputs, while others may even have normal totem pole outputs. In order to make your device work correctly on as many Printer Ports as possible, you can use an external resistor as well. Should you already have an internal resistor, then it will act in Parallel with it, or if you have Totem pole outputs, the resistor will act as a load.

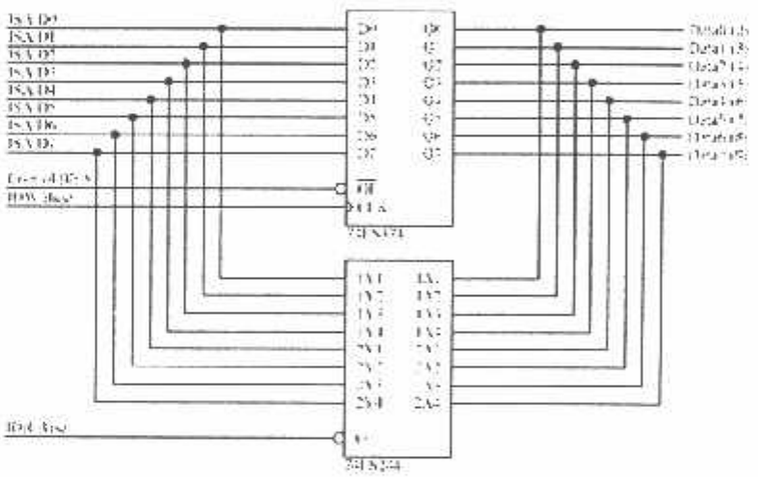
An external 4.7k resistor can be used to pull the pin high. I wouldn't use anything lower, just in case you do have an internal pull up resistor, as the external resistor would act in parallel giving effectively, a lower value pull up resistor. When in high impedance state the pin on the Parallel Port is high (+5v). When in this state, your external device can pull the pin low and have the control port change read a different value. This way the 4 pins of the Control Port can be used for bi-directional data transfer. However the Control Port must be set to xxxx0100 to be able to read data, that is all pins to be +5v at the port so that you can pull it down to GND (logic 0).

Bits 4 & 5 are internal controls. Bit four will enable the IRQ *(See Using the Parallel Ports IRQ)* and Bit 5 will enable the bi-directional port meaning that you can input 8 bits using (DATA0-7). This mode is only possible if your card supports it. Bits 6 & 7 are reserved. Any writes to these two bits will be ignored.

Bi-directional Ports

The schematic diagram below, shows a simplified view of the Parallel Port's Data Register. The original Parallel Port card's implemented 74LS logic. These days all this is crammed into one ASIC, but the theory of operation is still the same.

Standard Parallel Port Bi-Directional Operation



The non bi-directional ports were manufactured with the 74LS374's output enable tied permanent low, thus the data port is always output only. When you read the Parallel Port's data register, the data comes from the 74LS374 which is also connected to the data pins. Now if you can overdrive the '374 you can effectively have a Bi-directional Port. *(or a input only port, once you blow up the latches output!)*

What is very concerning is that people have actually done this. I've seen one circuit, a scope connected to the Parallel Port distributed on the Internet. The author uses an ADC of some type, but finds the ADC requires transistors on each data line, to make it work! No wonder why. Others have had similar trouble, the 68HC11 cannot sink enough current (30 to 40mA!)

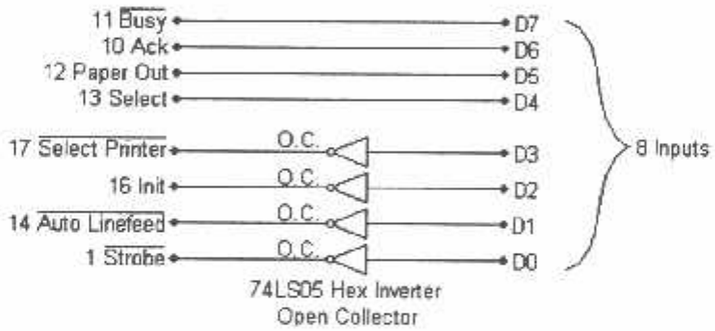
Bi-directional ports use Control Bit 5 connected to the 374's OE so that it's output drivers can be turned off. This way you can read data present on the Parallel Port's Data Pins, without having bus conflicts and excessive current drains.

Bit 5 of the Control Port enables or disables the bi-directional function of the Parallel Port. This is only available on true bi-directional ports. When this bit is set to one, pins 2 to 9 go into high impedance state. Once in this state you can enter data on these lines and retrieve it from the Data Port (base address). Any data which is written to the data port will be stored but will not be available at the data pins. To turn off bi-directional mode, set bit 5 of the Control Port to '0'.

However not all ports behave in the same way. Other ports may require setting bit 6 of the Control Port to enable Bi-directional mode and setting of Bit 5 to dis-enable Bi-directional mode, Different manufacturers implement their bi-directional ports in different ways. If you wish to use your Bi-directional port to input data, test it with a logic probe or multimeter first to make sure it is in bi-directional mode.

Using The Parallel Port to Input 8 Bits.

If your Parallel Port doesn't support bi-directional mode, don't despair. You can input a maximum of 9 bits at any one given time. To do this you can use the 5 input lines of the Status Port and the 4 inputs (open collector) lines of the Control Port.



The inputs to the Parallel Port has be chosen as such, to make life easier for us. Busy just happens to be the MSB (Bit 7) of the Status Port, then in ascending order comes Ack, Paper Out and Select, making up the most significant nibble of the Control Port. The Bars are used to represent which inputs are Hardware inverted, i.e. +5v will read 0 from the register, while GND will read 1. The Status Port only has one inverted input.

The Control port is used to read the least significant nibble. As described before, the control port has open collector outputs, i.e. two possible states, high impedance and GND. If we connect our inputs directly to the port *(For example an ADC0804 with totem pole outputs)* , a conflict will result if the input is high and the port is trying to pull it down. Therefore we use open collector inverters.

However this is not always entirely necessary. If we were connecting single pole switches to the port with a pull up resistor, then there is no need to bother with this protection. Also if your software initializes the control port with xxxx0100 so that all the pins on the control port are high,

then it may be unnecessary. If however you don't bother and your device is connected to the Parallel Port before your software has a chance to initialize then you may encounter problems.

Another problem to be aware of is the pull up resistors on the control port. The average pull-up resistor is 4.7k. In order to pull the line low, your device will need to sink 1mA, which some low powered devices may struggle to do. Now what happens if I suggest that some ports have 1K pull up resistors? Yes, there are such cards. Your device now has to sink 5mA. More reason to use the open collector inverters.

Open collector inverters were chosen over open collector buffers as they are more popular, and thus easier to obtain. There is no reason, however why you can't use them. Another possibility is to use transistors.

The input, D3 is connected via the inverter to Select Printer. Select Printer just happens to be bit 3 of the control port. D2, D1 & D0 are connected to Init, Auto linefeed and strobe, respectively to make up the lower nibble. Now this is done, all we have to do is assemble the byte using software. The first thing we must do is to write xxxx0100 to the Control Port. This places all the control port lines high, so they can be pulled down to input data.

```
outportb(CONTROL, inportb(CONTROL) & 0xF0 | 0x04);
```

Now that this is done, we can read the most significant nibble. This just happens to be the most significant nibble of the status port. As we are only interested in the MSnibble we will AND the results with 0xF0, so that the LSnibble is clear. Busy is hardware inverted, but we won't worry about it now. Once the two bytes are constructed, we can kill two birds with one stone by toggling Busy and Init at the same time.

```
a = (inportb(STATUS) & 0xF0); /* Read MSnibble */
```

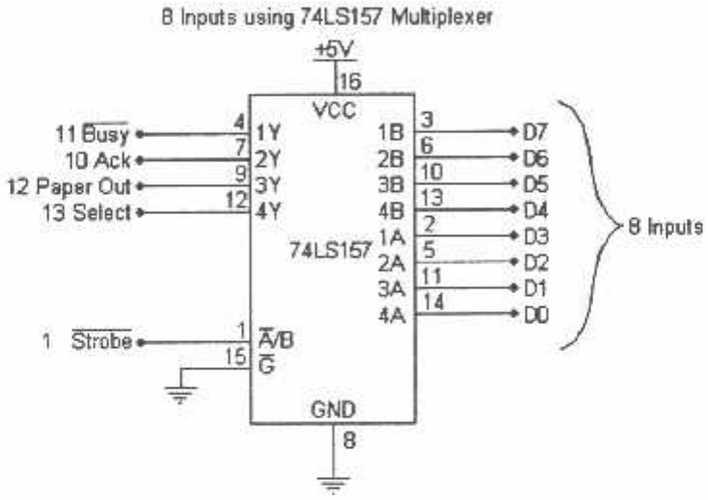
We can now read the LSnibble. This just happens to be LSnibble of the control port - How convenient! This time we are not interested with the MSnibble of the port, thus we AND the result with 0x0F to clear the MSnibble. Once this is done, it is time to combine the two bytes together. This is done by OR'ing the two bytes. This now leaves us with one byte, however we are not finished yet. Bits 2 and 7 are inverted. This is overcome by XOR'ing the byte with 0x84, which toggles the two bits.

```
a = a |(inportb(CONTROL) & 0x0F); /* Read LSnibble */
a = a ^ 0x84; /* Toggle Bit 2 & 7 */
```

Note: Some control ports are not open collector, but have totem pole outputs. This is also the case with EPP and ECP Ports. Normally when you place a Parallel Port in ECP or EPP mode, the control port becomes totem pole outputs only. Now what happens if you connect your device to the Parallel Port in this mode? Therefore, in the interest of portability I recommend using the next circuit, reading a nibble at a time.

Nibble Mode

Nibble mode is the preferred way of reading 8 bits of data without placing the port in reverse mode and using the data lines. Nibble mode uses a Quad 2 line to 1 line multiplexer to read a nibble of data at a time. Then it "switches" to the other nibble and reads its. Software can then be used to construct the two nibbles into a byte. The only disadvantage of this technique is that it is slower. It now requires a few I/O instructions to read the one byte, and it requires the use of an external IC.



The operation of the 74LS157, Quad 2 line to 1 line multiplexer is quite simple. It simply acts as four switches. When the A/B input is low, the A inputs are selected. E.g. 1A passes through to 1Y, 2A passes through to 2Y etc. When the A/B is high, the B inputs are selected. The Y outputs are connected up to the Parallel Port's status port, in such a manner that it represents the MSnibble of the status register. While this is not necessary, it makes the software easier.

To use this circuit, first we must initialize the multiplexer to switch either inputs A or B. We will read the LSnibble first, thus we must place A/B low. The strobe is hardware inverted, thus we must set Bit 0 of the control port to get a low on Pin 1.

```
outportb(CONTROL, inportb(CONTROL) | 0x01); /* Select Low Nibble (A)*/
```

Once the low nibble is selected, we can read the LSnibble from the Status Port. Take note that the Busy Line is inverted, however we won't tackle it just yet. We are only interested in the MSnibble of the result, thus we AND the result with 0xF0, to clear the LSnibble.

```
a = (inportb(STATUS) & 0xF0); /* Read Low Nibble */
```

Now it's time to shift the nibble we have just read to the LSnibble of variable a,

```
a = a >> 4; /* Shift Right 4 Bits */
```

We are now half way there. It's time to get the MSnibble, thus we must switch the multiplexer to select inputs B. Then we can read the MSnibble and put the two nibbles together to make a byte,

```
outportb(CONTROL, inportb(CONTROL) & 0xFE); /* Select High Nibble (B)*/
a = a |(inportb(STATUS) & 0xF0); /* Read High Nibble */
byte = byte ^ 0x88;
```

The last line toggles two inverted bits which were read in on the Busy line. It may be necessary to add delays in the process, if the incorrect results are being returned.

Using the Parallel Port's IRQ

The Parallel Port's interrupt request is not used for printing under DOS or Windows. Early versions of OS-2 used them, but don't anymore. Interrupts are good when interfacing monitoring devices such as high temp alarms etc, where you don't know when it is going to be activated. It's more efficient to have an interrupt request rather than have the software poll the ports regularly to see if something has changed. This is even more noticeable if you are using your computer for other tasks, such as with a multitasking operating system.

The Parallel Port's interrupt request is normally IRQ5 or IRQ7 but may be something else if these are in use. It may also be possible that the interrupts are totally disabled on the card, if the card was only used for printing. The Parallel Port interrupt can be disabled and enabled using bit 4 of the control register, *Enable IRQ Via Ack Line*. Once enabled, an interrupt will occur upon a low to high transition (rising edge) of the nACK. However like always, some cards may trigger the interrupt on the high to low transition.

The following code is an Interrupt Polarity Tester, which serves as two things. It will determine which polarity your Parallel Port interrupt is, while also giving you an example for how to use the Parallel Port's Interrupt. It checks if your interrupt is generated on the rising or falling edge of the nACK line. To use the program simply wire **one of** the Data lines (Pins 2 to 9) to the Ack Pin (Pin 10). The easiest way to do this is to bridge some solder from DATA7 (Pin 9) to ACK (Pin 10) on a male DB25 connector.

```
/*  Parallel Port Interrupt Polarity Tester                    */
/*  2nd February 1998                                          */
/*  Copyright 1997 Craig Peacock                               */
/*  WWW     - http://www.senet.com.au/~cpeacock                */
/*  Email   - cpeacock@senet.com.au                            */

#include <dos.h>

#define PORTADDRESS 0x378  /* Enter Your Port Address Here */
#define IRQ 7              /* IRQ Here */

#define DATA PORTADDRESS+0
#define STATUS PORTADDRESS+1
#define CONTROL PORTADDRESS+2

#define PIC1 0x20
#define PIC2 0xA0

int interflag; /* Interrupt Flag */
int picaddr;   /* Programmable Interrupt Controller (PIC) Base Address */
```

```
void interrupt (*oldhandler)();

void interrupt parisr()  /* Interrupt Service Routine (ISR) */
{
  interflag = 1;
  outportb(picaddr,0x20); /* End of Interrupt (EOI) */
}

void main(void)
{
 int c;
 int intno;    /* Interrupt Vector Number */
 int picmask;  /* PIC's Mask */

 /* Calculate Interrupt Vector, PIC Addr & Mask. */

 if (IRQ >= 2 && IRQ <= 7) {
                           intno = IRQ + 0x08;
                           picaddr = PIC1;
                           picmask = 1;
                           picmask = picmask << IRQ;
                          }
 if (IRQ >= 8 && IRQ <= 15) {
                            intno = IRQ + 0x68;
                            picaddr = PIC2;
                            picmask = 1;
                            picmask = picmask << (IRQ-8);
                           }
 if (IRQ < 2 || IRQ > 15)
       {
        printf("IRQ Out of Range\n");
        exit();
       }

 outportb(CONTROL, inportb(CONTROL) & 0xDF); /* Make sure port is in Forward Direction */
 outportb(DATA,0xFF);
 oldhandler = getvect(intno); /* Save Old Interrupt Vector */
 setvect(intno, parisr);      /* Set New Interrupt Vector Entry */
 outportb(picaddr+1,inportb(picaddr+1) & (0xFF - picmask)); /* Un-Mask Pic */
 outportb(CONTROL, inportb(CONTROL) | 0x10); /* Enable Parallel Port IRQ's */

 clrscr();
 printf("Parallel Port Interrupt Polarity Tester\n");
 printf("IRQ %d : INTNO %02X : PIC Addr 0x%X : Mask 0x%02X\n",IRQ,intno,picaddr,picmask);
 interflag = 0; /* Reset Interrupt Flag */
 delay(10);
 outportb(DATA,0x00); /* High to Low Transition */
 delay(10);           /* Wait */
 if (interflag == 1) printf("Interrupts Occur on High to Low Transition of ACK.\n");
 else
   {
    outportb(DATA,0x??); /* Low to High Transition */
    delay(10);           /* wait */
    if (interflag == 1) printf("Interrupts Occur on Low to High Transition of ACK.\n");
    else printf("No Interrupt Activity Occurred. \nCheck IRQ Number, Port Address "
                "and Wiring.");
    }

 outportb(CONTROL, inportb(CONTROL) & 0xEF); /* Disable Parallel Port IRQ's */
 outportb(picaddr+1,inportb(picaddr+1) | picmask); /* Mask Pic */
 setvect(intno, oldhandler); /* Restore old Interrupt Vector Before Exit */
}
```

At compile time, the above source may generate a few warnings, *condition always true, condition always false, unreachable code* etc. These are perfectly O.K. They are generated as some of the condition structures test which IRQ you are using, and as the IRQ is defined as a constant some outcomes will never change. While they would of been better implemented as a preprocessor directive, I've done this so you can cut and paste the source code in your own programs which may use command line arguments, user input etc instead of a defined IRQ.

To understand how this example works, the reader must have an assumed knowledge and understanding of Interrupts and Interrupt Service Routines (ISR). If not, see *Using Interrupts*[1] for a quick introduction.

The first part of the mainline routine calculates the Interrupt Vector, PIC Addr & Mask in order to use the Parallel Port's Interrupt Facility. After the Interrupt Service Routine (ISR) has been set up and the Programmable Interrupt Controller (PIC) set, we must enable the interrupt on the Parallel Port. This is done by setting bit 4 of the Parallel Port's Control Register using `outportb(CONTROL, inportb(CONTROL) | 0x10);`

Before enabling the interrupts, we wrote 0xFF to the Parallel Port to enable the 8 data lines into a known state. At this point of the program, all the data lines should be high. The interrupt service routine simply sets a flag (*interflag*), thus we can determine when an IRQ occurs. We are now in a position to write 0x00 to the data port, which causes a high to low transition on the Parallel Port's Acknowledge line as it's connected to one of the data lines.

If the interrupt occurs on the high to low transition, the interrupt flag (*interflag*) should be set. We now test this, and if this is so the program informs the user. However if it is not set, then an interrupt has not yet occurred. We now write 0xFF to the data port, which will cause a low to high transition on the nAck line and check the interrupt flag again. If set, then the interrupt occurs on the low to high transition.

However if the interrupt flag is still reset, then this would suggest that the interrupts are not working. Make sure your IRQ and Base Address is correct and also check the wiring of the plug.

Parallel Port Modes in BIOS

Today, most Parallel Ports are mulimode ports. They are normally software configurable to one of many modes from BIOS. The typical modes are,

Printer Mode (Sometimes called Default or Normal Modes))

Standard & Bi-directional (SPP) Mode

EPP1.7 and SPP Mode

EPP1.9 and SPP Mode

ECP Mode

ECP and EPP1.7 Mode

ECP and EPP1.9 Mode

Printer Mode is the most basic mode. It is a Standard Parallel Port in forward mode only. It has no bi-directional feature, thus Bit 5 of the Control Port will not respond. *Standard & Bi-directional (SPP) Mode* is the bi-directional mode. Using this mode, bit 5 of the Control Port will reverse the direction of the port, so you can read back a value on the data lines.

EPP1.7 and SPP Mode is a combination of EPP 1.7 (Enhanced Parallel Port) and SPP Modes. In this mode of operation you will have access to the SPP registers (Data, Status and Control) and access to the EPP Registers. In this mode you should be able to reverse the direction of the port using bit 5 of the control register. EPP 1.7 is the earlier version of EPP. This version, version 1.7, may not have the time-out bit. See *Interfacing the Enhanced Parallel Port*[2] for more information.

EPP1.9 and SPP Mode is just like the previous mode, only it uses EPP Version 1.9 this time. As in the other mode, you will have access to the SPP registers, including Bit 5 of the control port. However this differs from EPP1.7 and SPP Mode as you should have access to the EPP Timeout bit.

ECP Mode will give you an Extended Capabilities Port. The mode of this port can then be set using the ECP's Extended Control Register (ECR). However in this mode from BIOS the EPP Mode (100) will not be available. We will further discuss the ECP's Extended Control Register in this document, but if you want further information on the ECP port, consult *Interfacing the Extended Capabilities Port*[3].

ECP and EPP1.7 Mode & ECP and EPP1.9 Mode will give you an Extended Capabilities Port, just like the previous mode. However the EPP Mode in the ECP's ECR will now be available. Should you be in *ECP and EPP1.7 Mode* you will get an EPP1.7 Port, or if you are in *ECP and EPP1.9 Mode*, an EPP1.9 Port will be at your disposal.

The above modes are configurable via BIOS. You can reconfigure them by using your own software, but this is **not recommended**. These software registers, typically found at 0x2FA, 0x3F0, 0x3F1 etc are only intended to be accessed by BIOS. There is no set standard for these configuration registers, thus if you were to use these registers, your software would not be very portable. With today's multitasking operating systems, its also not a good idea to change them when it suits you.

A better option is to select *ECP and EPP1.7 Mode* or *ECP and EPP1.9 Mode* from BIOS and then use the ECP's Extended Control Register to select your Parallel Port's Mode. The EPP1.7 mode had a few problems in regards to the Data and Address Strobes being asserted to start a cycle regardless of the wait state, thus this mode if not typically used now. Best set your Parallel Port to *ECP and EPP1.9 Mode*.

Parallel Port Modes and the ECP's Extended Control Register

As we have just discussed, it is better to set the Parallel Port to *ECP and EPP1.9 Mode* and use the ECP's Extended Control Register to select different modes of operation. The ECP Registers are standardized under Microsoft's **Extended Capabilities Port Protocol and ISA Interface Standard**, thus we don't have that problem of every vendor having their own register set.

When set to ECP Mode, a new set of registers become available at Base + 0x400h. A discussion of these registers are available in *Interfacing the Extended Capabilities Port*[3]. Here we are only interested in the Extended Control Register (ECR) which is mapped at Base + 0x402h. It should be stated that the ECP's registers are not available for port's with a base address of 0x3BCh.

Bit	Function	
7:5	*Selects Current Mode of Operation*	
	000	Standard Mode
	001	Byte Mode
	010	Parallel Port FIFO Mode
	011	ECP FIFO Mode
	100	EPP Mode
	101	Reserved
	110	FIFO Test Mode
	111	Configuration Mode
4	ECP Interrupt Bit	
3	DMA Enable Bit	
2	ECP Service Bit	
1	FIFO Full	
0	FIFO Empty	

Table 7 ECR - Extended Control Register

The table above is of the Extended Control Register. We are only interested in the three MSB of the Extended Control Register which selects the mode of operation. There are 7 possible modes of operation, but not all ports will support all modes. The EPP mode is one such example, not being available on some ports.

Modes of Operation

Standard mode — Selecting this mode will cause the ECP port to behave as a Standard Parallel Port, without bi-directional functionality.

Byte Mode / PS/2 mode — Behaves as a SPP in bi-directional mode. Bit 5 will place the port in reverse mode.

Parallel Port FIFO mode — In this mode, any data written to the Data FIFO will be sent to the peripheral using the SPP Handshake. The hardware will generate the handshaking required. Useful with non-ECP devices such as printers. You can have some of the features of ECP like FIFO buffers and hardware generation of handshaking but with the existing SPP handshake (Centronics) instead of the ECP Handshake.

ECP FIFO mode — Standard mode for ECP use. This mode uses the ECP Handshake described in *Interfacing the Extended Capabilities Port*[3]

When in ECP Mode though BIOS, and the ECR register is set to ECP FIFO Mode (011), the SPP registers may disappear.

EPP mode/*Reserved* — This will enable EPP Mode, if available. Under BIOS, if *ECP mode* is set then it's more than likely, this mode is not an option. However if BIOS is set to *ECP and EPP1.x Mode*, then EPP 1.x will be enabled.

*Under Microsoft's **Extended Capabilities Port Protocol and ISA Interface Standard** this mode is Vendor Specified.*

Reserved	Currently Reserved. *Under Microsoft's **Extended Capabilities Port Protocol and ISA Interface Standard** this mode is Vendor Specified.*
FIFO Test Mode	While in this mode, any data written to the Test FIFO Register will be placed into the FIFO and any data read from the Test FIFO register will be read from the FIFO buffer. The FIFO Full/Empty Status Bits will reflect their true value, thus FIFO depth, among other things can be determined in this mode.
Configuration Mode	In this mode, the two configuration registers, cnfgA & cnfgB become available at their designated Register Addresses.

If you are in *ECP Mode* under BIOS, or if your card is jumpered to use ECP then it is a good idea to initialize the mode of your ECP port to a pre-defined state before use. If you are using SPP, then set the port to Standard Mode as the first thing you do. Don't assume that the port will already be in Standard (SPP) mode.

Under some of the modes, the **SPP registers may disappear or not work correctly**. If you are using SPP, then set the ECR to Standard Mode. This is one of the most common mistakes that people make.

Notes

*Note[1] **Using Interrupts** is available in PDF from*
http://www.geocities.com/SiliconValley/Bay/8302/interupt.pdf (62kb)

*Note[2] **Interfacing the Enhanced Parallel Port** is available in PDF from*
http://www.geocities.com/SiliconValley/Bay/8302/epp.pdf (33kb)

Note[3] ***Interfacing the Extended Capabilities Port** is available in PDF from*
http://www.geocities.com/SiliconValley/Bay/8302/ecp.pdf (53kb)

Craig Peacock's Interfacing the PC

http://www.senet.com.au/~cpeacock

http://www.geocities.com/SiliconValley/Bay/8302/

Any errors, ideas, criticisms or problems, please contact the author at cpeacock@senet.com.au