SKRIPSI

PERENCANAAN DAN PEMBUATAN INVERTER BERBASIS MIKROKONTROLER AT89852 DENGAN MENGGUNAKAN ALGORITMA *DIRECT DIGITAL SYNTHESIS* (DDS)

Disusun Oleh:

SAIFUL FANANI

NIM 0017156

JURUSAN TEKNIK ELEKTRO S1

KONSENTRASI TEKNIK ELEKTRONIKA

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

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LEMBAR PERSETUJUAN

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SKRIPSI

Disusun dan diajukan sebagai salah satu syarat untuk memperoleh gelar Sarjana Teknik Elektronika Strata Satu (S-1)

Disusun Oleh :

SAIFUL FANANI
00.17.156

Diperiksa dan disetujui,

Dosen Pembimbing I	Dosen Pembimbing II
Ir. F. Yudi Limpraptono, MT	**Ir. M. Abdul Hamid, MT**
NIP. P. 1039500274	**NIP. Y. 1018800188**

Mengetahui,
Ketua Jurusan Teknik Elektro S-1

Ir. F. Yudi Limpraptono,MT.
NIP.P. 103 950 0274

JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI

Nama Mahasiswa	: Saiful fanani
NIM	: 00.17.156
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Judul Skripsi	: Perecanaan dan Pembuatan Inverter Berbasis Mikrokontroler AT89S52 Dengan Menggunakan Algoritma DDS *(Direct Digital Synthesis)*

Dipertahankan dihadapan Team Penguji Skripsi Jenjang Strata Satu (S-1) Pada :

Hari	: Senin
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Dengan Nilai	: 76,3 (B+)

Panitia Ujian Skripsi

Ketua	Sekretaris
(Ir.Mochtar Asroni, MSME)	**(Ir.F.Yudi Limpraptono, MT)**
NIP.Y. 1018100036	**NIP.Y. 1039500274**

Anggota Penguji

Penguji Pertama	Penguji Kedua
(Dr. Cahyo Crysdian, MSc.)	**(Joseph Dedy Irawan, ST, MT.)**
NIP.Y. 1030400412	**NIP.Y. 132315178**

ABSTRAKSI

PERENCANAAN DAN PEMBUATAN INVERTER BERBASIS MIKROKONTROLLER AT89S52 DENGAN MENGGUNAKAN ALGORITMA DDS (*Direct Digital Synthesis*)

Saiful Fanani, 00.17.156, Jurusan Teknik Elektro S-1, Dosen Pembimbing I : Ir. F. Yudi Limpraptono, MT., Dosen Pembimbing II : Ir. M Abdul Hamid, MT.

Aplikasi mikrokontroler sebagai interface sangat membantu dalam mengotomatisasi suatu system control untuk mempermudah dan mempercepat proses kinerja suatu alat yang digunakan, sehingga dewasa ini sudah banyak desain interface yang memakai mikrokontroler sebagai pengontrol utama. Salah satunya adalah perencanaan dan pembuatan inverter berbasis mikrokontroler AT89S52 dengan menggunakan algoritma DDS (Direct Digital Synthesis). Dengan cara menggunakan mikrokontroler sebagai pemrosesan data sesuai dengan metode DDS (Direct Digital Synthesis) dimana keluaran dari Mikrokontroler berupa sinyal digital menjadi masukan untuk DAC (digital Analog Converter), output dari DAC merupakan sampel dari bentuk analog yang kemudian akan difilter untuk menghasilkan sinyal sinusoida yang sempurna. Setelah pengujian, dapat diambil kesimpulkan bahwa alat ini masih memiliki error yang besar karena Tegangan yang keluar dari transformator tidak maksimal dikarenakan adanya rugi tegangan yang terdapat pada transformator dan tegangan yang keluar 90 volt AC.

ABSTRACT

Microcontroller aplication as interface very support in automatically control system to simplify and to speed up perform used some utensil, so nowdays it is very much interface design to use microcontroller as exellent controller. Anything is the project and inverter production based AT89S52 Microcontroller to apply algorithm DDS (Direct Digital Synthesis). By microcontroller method such data process to fit with DDS (Direct Digital Synthesis) method which product from microcontroller to appear digital signal to became included in for DAC (Digital Analog Converter). Output from DAC to shape simple from analog type and than the filter to result perfect sinussoida signal. After the test, it can take a conclusion that this system still have a lot of error because many to suffer a loss at transformator end out put voltage just 90 volt AC.

KATA PENGANTAR

"ALHAMDULILLAH....."

Puji Syukur kehadirat Allah S.W.T. Dengan Rahmat dan Hidayah-NYA penulis dapat menyelesaikan laporan tugas akhir dengan judul :

" Perancangan dan Pembuatan Inverter Berbasis Mikrokontroller AT89S52 Dengan Menggunakan Algoritma DDS (Direct Digital Synthesis)"

Pembuatan tugas akhir ini disusun guna memenuhi syarat akhir kelulusan pendidikan jenjang Strata-1 di Institut Teknologi Nasional Malang. Laporan tugas akhir ini merupakan tanggung jawab tertulis atas ilmu pengetahuan yang didapat selama penyusun mengikuti kuliah.

Atas selesainya tugas akhir ini, penyusun mengucapkan ucapan terimakasih kepada :

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- Bapak Ir. F. Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro S-1 dan selaku Dosen pembimbing I
- Bapak Ir. M. Abdul Hamid, MT selaku Dosen Pembimbing II atas bantuan ilmu, arahan, serta dukungan yang diberikan.
- Teman-teman yang telah membantu terselesainya skripsi ini.

Penyusun menyadari bahwa laporan ini masih banyak yang perlu disempurnakan. Oleh sebab itu kritik dan saran yang membangun sangat diharapkan.

Akhir kata, penyusun mohan maaf kepada semua pihak bilamana selama penyusunan skripsi ini penyusun membuat kesalahan secara tidak sengaja dan semoga skripsi ini dapat bermanfaat bagi kita semua.

Malang, Maret 2008

Penyusun

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BAB I
PENDAHULUAN

1.1. Latar Belakang

Penggunaan instrumen elektronika yang menggunakan system mikrokontroler sebagai pengontrol, dewasa ini sudah demikian luas didalam bidang kehidupan. System mikrokontroler ini menggunakan komponen memori untuk penyimpanan data selama proses berlangsung. Selain itu komponen ini juga berguna untuk menyimpan program dan data untuk dapat memfungsikan system mikrokontroler.

Aplikasi mikrokontroler sebagai interface sangat membantu dalam mengotomatisasi suatu system control untuk mempermudah dan mempercepat proses kinerja suatu alat yang digunakan, sehingga dewasa ini sudah banyak desain interface yang memakai mikrokontroler sebagai pengontrol utama. Penerapan mikrokontroler untuk berbagai system control tentunya memerlukan software yang berbeda sesuai dengan alat yang akan dikontrol oleh mikrokontroler.

System DDS (Direct Digital Synthesis) adalah salah satu cara untuk mensintesis sinyal kontinu sinusoida. Semua parameter control system DDS berada dalam bentuk besaran digital. System DDS pada dasarnya terdiri atas akumulator phasa, LUP (look up table), dan osilator sebagai pembangkit frekuesi

referensi (Clock). Sedangkan DAC (digital to analog converter) dan LPF (low pass filter) merupakan komponen-komponen penunjang system DDS.

1.2. Rumusan Masalah

Dalam perencanaan dan pembuatan alat pengontrol peralatan rumah dengan output suara dapat dirumuskan beberapa masalah seperti berikut ini:

- Proses yang dilakukan sebelum membuat alat, merencanakan alat bagaimana merancang dan membuat alat yang dapat mengubah tegangan DC menjadi tegangan AC
- Bagaimana mengatur tegangan DC menjadi tegangan AC menggunakan mikrokontroller

1.3. Tujuan

Tujuan dari skripsi ini adalah merancang dan membuat alat inverter berbasis mikrokontroler AT89S52 dengan menggunakan algoritma DDS.

1.4. Batasan Masalah

Schubungan dengan masalah yang dihadapi dalam pembuatan skripsi ini, permasalahan hanya dibatasi dengan tujuan untuk mencegah kemungkinan meluasnya masalah dan penyimpangan dari permasalahan. Pembatasan tersebut antara lain :

- Perangkat keras yang digunakan IC Mikrokontroler AT89S52.

- Menggunakan algoritma DDS (Direct Digital Sinthesis) untuk menghasilkan sinusoida
- Menggunakan ADC 0804 untuk mengubah data analog to digital dan DAC 0808 untuk mengubah data digital to analog
- Menggunakan trafo step up untuk penaik tegangan

1.5. Metodologi Penelitian

Dalam penulisan skripsi ini penulis menggunakan metode-metode yang sering digunakan. Adapun metode tersebut adalah sebagai berikut :

- Study literature, dengan mempelajari teori serta aplikasi sistem kontrol menggunakan Mikrokontroler AT89S52

  Study literature disini akan mempelajari hal-hal sebagai berikut:

  - Mikrokontroler AT89S52
    - Arsitektur Mikrokontroller AT89S52
    - Karakteristik umum
    - Interface dengan Input/Output (I/O) Mikrokontroller.

- Perencanaan dan pembuatan alat.

  Dalam pembuatan alat ini menggunakan konsep sebagai berikut:

    - Perencanaan sistem secara keseluruhan (Pembuatan Blok Diagram Sistem dan Fungsi masing-masing Blok Diagram).

- Membuat perangkat keras (Hardware) dan perangkat lunaknya (Software).

1.6. Sistematika Penulisan

Dalam pengerjaan laporan skripsi ini kami menggunkan sistematika sebagai berikut :

BAB I Pendahuluan

Pada pendahuluan ini berisikan tentang latar belakang masalah,rumusan masalah, tujuan pembuatan alat, batasan masalah, metode pembahasan dan sistematika pembahasan dari skripsi ini.

BAB II Landasan Teori

Pada landasan teori ini akan dibahas mengenai teori-teori yang mendasari pembuatan alat ini.

BAB III Perencanaan dan Pembuatan Alat

Berisi tentang perencanaan dan pembuatan Hardware dan Software.

BAB IV Pengujian Alat

Berisi tentang data hasil pengujian alat yang telah dibuat secara keseluruhan.

BAB V Penutup

Merupakan kesimpulan dari pembahasan pada bab-bab sebelumnya dan kemungkinan pengembangan alat.

BAB II

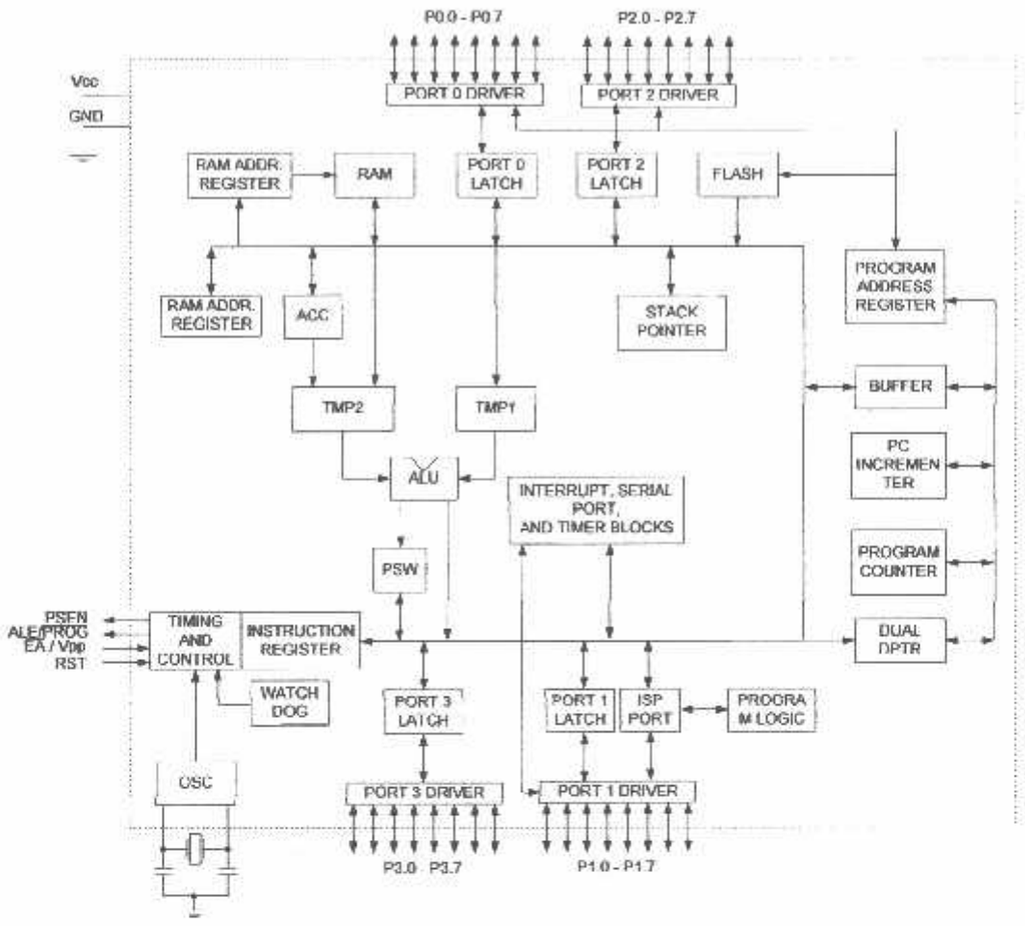
LANDASAN TEORI

2.1. Mikrokontroler AT89S52

Mikrokontroler AT89S52 merupakan IC mikrokontroler dengan konsumsi daya rendah dengan performansi tinggi dan compatible dengan produk MCS-52, memiliki struktur sebagai berikut :

1. 8 bit CPU (central processing unit) / merupakan mikrokontroler 8 bit.
2. 8 Kbyte Flash Programmable And Erasable Read Only Memory (PEROM).
3. 256 x 8 bit Internal RAM.
4. 32 pin I/O yang tersusun dalam 4 port (P0, P1, P2, P3) dengan setiap port terdiri dari 8 bit.
5. Memiliki 6 sumber interupsi.
6. 3 Timer / Counter 16 bit
7. Full Duplex serial port yang dapat diprogram.
8. On Chip Oscilator.
9. Watchdog Timer
10. Dual data pointer.
11. Flexible ISP Programming.

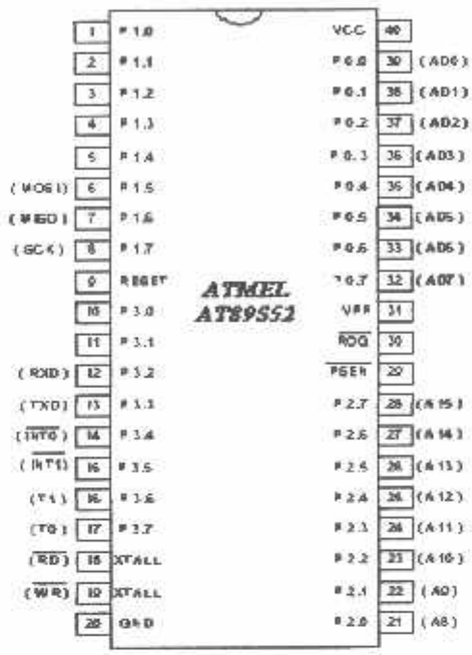
Secara lengkap struktur dari mikrokontroler AT89S52 dapat ditunjukan pada gambar berikut :



Gambar 2-1 Blok Diagram Mikrokontroler AT89S52[1]

2.1.1. Definisi Pin Mikrokontroler AT89S52

Mikrokontroler AT89S52 memiliki 40 Pin yang didefinisikan seperti pada gambar 2-5 berikut :



Gambar 2-2 Konfigurasi pin AT89S52[21]

1. Vcc : Catu daya (supply tegangan).
2. Gnd : Ground.
3. Port 0 : Port 0 merupakan port 8 bit yang bersifat open drain dua arah. Sebagai port keluaran, tiap pin dapat menerima 8 masukan TTL. Saat logika 1 dituliskan pada port, pin port dapat digunakan sebagai masukan dengan impedansi tinggi.
4. Port 1 : Port ini merupakan port I/O biderectional dengan internal pull-up. Out put Port ini dapat mendayai atau menerima 4 masukan TTL. Jika suatu logika 1 dituliskan pada port ini, maka port akan dibuat tinggi oleh *pull-up* internal dan dapat digunakan sebagai masukan. Pada saat sebagai port

masukan, port ini akan dibuat rendah dan port ini akan mendayai karena adanya *pull-up* internal.

5. Port 2 : Port ini merupakan port I/O biderectional dengan internal pull-up. Penyangga pada port ini mampu menangani 4 masukan TTL. Jika logika 1 dituliskan pada port ini, maka port akan dibuat tinggi oleh *pull-up* internalnya.

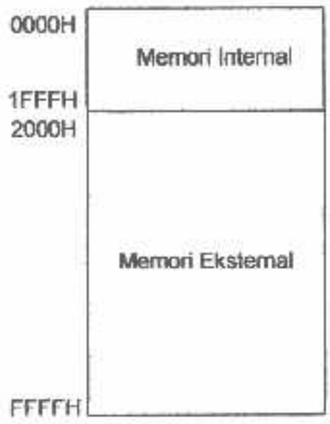
6. Port 3 : Port ini merupakan port I/O bidirectional dengan internal pull-up. Out put Port ini dapat mendayai atau menerima 4 masukan TTL. Jika suatu logika 1 dituliskan pada port ini, maka port akan dibuat tinggi oleh *pull-up*. Selain sebagai port parallel port ini juga mempunyai fungsi khusus yaitu :

Tabel 2-1 Fungsi khusus Port 3

Port Pin	Fungsi Khusus
P3.0	RXD (masukan port serial (UART))
P3.1	TXD (keluaranan port serial (UART))
P3.2	INT0 (masukan interupsi luar 0)
P3.3	INT1 (masukan interupsi luar1)
P3.4	T0 (masukan luar Timer / Counter 0)
P3.5	T1 (masukan luar Tmer)
P3.6	WR (pulsa penulisan data memori luar)
P3.7	RD (pulsa pembacaan memori luar)

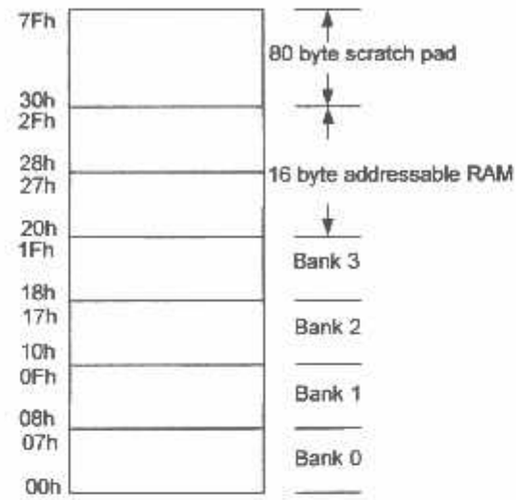
7. Reset : Masukan untuk reset. Suatu logika high selama dua siklus pada pin reset akan menyebabkan terjadinya proses reset.

8. ALE : Addres latch enable merupakan suatu pulsa keluaran untuk mengaitkan (latch) byte bawah dari alamat selama mengakses memori luar.



Gambar 2-3 Organisasi Program memori[13]

Sedangkan untuk data memori AT89S52 memiliki RAM internal yang berkapasitas 256 byte, kapasitas ini dapat dinaikan menjadi maximal 64 Kbyte dengan menambah memori eksternal. Data memori dibagi menjadi dua bagian yaitu register khusus yang digunakan oleh mikrokontroler (SFR) dan register yang dapat dipakai oleh pengguna. RAM (Random Access Memori) merupakan memori yang bersifat mudah terhapus isinya jika aliran listrik diputus, karena itu RAM tidak digunakan untuk menyimpan program tetapi untuk menyimpan data sementara. Peta dari RAM internal pada MCS-52 dapat ditunjukan pada gambar sebagai berikut :



Gambar 2-4 Peta memori RAM internal [4]

Pada gambar diatas terlihat bahwa RAM internal 256 byte terbagi menjadi beberapa bagian. Untuk alamat bawah yang pertama yaitu 00h sampai 7Fh sebanyak 256 byte yang terbagi dalam tiga besar berdasarkan kegunaanya yaitu :

a. Register Bank 0 – 3

- Lokasi register bank dimulai dari 00h – 1Fh terdiri dari 32 byte.
- Register bank ini terdiri dari empat buah register 8 bit yang dapat dipilih melalui pengaturan RS0 dan RS1 yang merupakan bit ke 3 dari program status word register.

b. Bit Addressable

- Lokasi register ini dimulai dari 20h – 2Fh
- Register ini bersifat Addressable, artinya bahwa perubahan dapat dilakukan per bit, tidak perlu per byte (8 bit). Fitur ini sangat berguna untuk meng-on-off kan suatu bit. Lokasi ini juga dapat dialamati secara langsung untuk 256 byte yang tersedia.

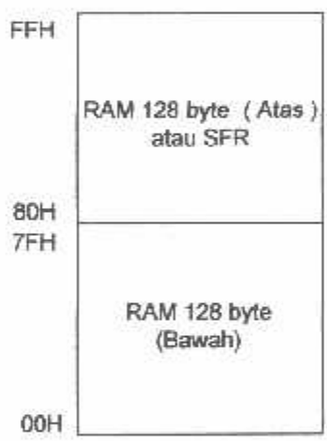
c. Scratch Pad

Lokasi register ini dimulai dari 30h – 7Fh yang digunakan untuk keperluan apa saja termasuk untuk alokasi stack pointer.

Tabel 2-2 Register Bank

RS0	RS1	Register Bank	Address
0	0	0	00H - 07H
0	1	1	08H - 09H
1	0	2	10H - 17H
1	1	3	18H - 1FH

Setelah RAM 256 byte yang pertama, diatasnya diletakkan alamat untuk SFR (Special Function Register), perlu diingat bahwa RAM 256 byte atas sama dengan alamat SFR yaitu 80H – FFH, seperti ditunjukan pada gambar berikut :



Gambar 2-5 Memori internal (RAM) dan SFR[5]

2.1.2.1.Special Function register (SFR)

SFR merupakan register dengan fungsi khusus. SFR pada mikrokontroler MCS-52 memiliki alamat 80H - FFH sehingga terdapat 256 lokasi untuk alamat SFR. Dari alamat-alamat ini hanya beberapa saja yang digunakan oleh SFR.

Tabel 2-3

Byte Special Function Register

Simbol	Nama	Address
ACC	Accumulator	0E0H
B	B Register	0F0H
PSW	Program status Word	0D0H
SP	Stack Pointer	81H
DPTR	Data Pointer	
DPL	Low Byte	82H
DPH	High Byte	83H
P0	Port 0	80H
P1	Port 1	90H
P2	Port 2	0A0H
P3	Port 3	0B0H
IP	Interrupt Priority Control	0B8H
IE	Interrupt Enable Control	0A8H
TMOD	Timer/Counter Mode Control	89H
TCON	Timer/Counter Control	88H
TH0	Timer/Counter 0 High Control	8CH
TL0	Timer/Counter 0 Low Control	8AH

2.1.2.2.Program status Word (PSW)

Program status word berguna untuk memilih bank memori yang aktif, selain itu PSW juga memiliki kegunaan yang lain. Kegunaan lain itu dapat dilihat dari masing-masing bit penyusun PSW. PSW ini bersifat *bit-addressable* artinya bit-bitnya masing-masing dapat dirubah tanpa harus merubah satu kesatuan byte. Berikut adalah bit-bit penyusun PSW :

Posisi	PSW.7	PSW.6	PSW.5	PSW.4	PSW.3	PSW.2	PSW.1	PSW.0
Bit	CY	AC	F0	RS1	RS0	OV	-	P

Keterangan :

Bit CY : Bit Carry Flag

Bit AC : Bit Auxiliary Carry Flag

Bit F0 : Flag 0 untuk kegunaan umum

Bit RS1 : Bit pemilih bank memori

Bit RS0 : Bit pemilih bank memori

Bit OV : Bit Overflow Flag

Bit PAW.1 : Bit didefinisikan pemakai

Bit P : Bit Parity. Menunjukan jumlah bit 1 pada accumulator

2.1.2.3.Power Control Register (PCON)

Register Power Control beralamat di 87H berguna untuk mengatur kebutuhan daya mikrokontroler. Dengan adanya register pengatur daya ini memungkinkan mikrokontroler ke mode "*idle*" atau "*sleep*" yang mana akan menghemat pemakaian daya. Selain itu ada bit-bit pada register PCON ini untuk mengatur Baud Rate pada serial port. Bit-bit pada PCON adalah sebagai berikut :

MSB							LSB
SMOD	-	-	-	GF1	GF0	PD	IDL

Keterangan :

Bit SMOD : Digunakan untuk membuat dobel (2 kali) baud rate pada timer 1

Bit - : Tidak digunakan, untuk pengembangan selanjutnya

Bit GF1 : Bit Flag serbaguna

Bit GF0 : Bit Flag serbaguna

Bit PD : Bit power down. Bila berlogika 1 mode power down aktif

Bit IDL : Bit idle mode. Aktif jika berlogika 1

2.1.2.4.Accumulator

Dari namanya dapat diketahui bahwa fungsi dari accumulator adalah pengumpul. SFR. Register ini merupakan register yang banyak dipakai. Untuk semua operasi aritmatika biasanya menggunakan/melibatkan accumulator. Alamat dari accumulator adalah E0H.

2.1.2.5.B Register

B Register beralamat di F0H. Register ini digunakan untuk operasi perkalian dan pembagian. Contoh instruksi yang menggunakan register ini adalah:

Mul AB ; kalikan isi pada accumulator dan pada B register

Div AB ; membagi isi accumulator dengan isi B register, accumulator akan berisi hasil bagi dan B register akan berisi sisa pembagian.

2.1.2.6.Stack Pointer (SP)

Stack pointer adalah penunjuk stack yang memiliki alamat di 81H. Isi register ini mengindikasikan dimana nilai selanjutnya yang harus diambil oleh stack pada RAM internal. Jika anda memasukan (*PUSH*) suatu nilai ke stack, maka nilai tersebut akan dituliskan pada alamat SP+1 (alamat SP ditambah satu). Jika SP berisi 07H kemudian suatu instruksi *PUSH* dijalankan, maka nilai yang

dimasukan akan dituliskan pada alamat 08H. Nilai default untuk stack pointer adalah berada pada alamat 07H.

2.1.2.7.Data Pointer (DPTR)

Data Pointer (DPTR) yang berukuran 16 bit terdiri dari dua register yaitu DPL (Data Pointer Low byte) yang beralamat di 82H dan DPH (Data Pointer High byte) yang beralamat di 83H. Data Pointer digunakan untuk membentuk alamat berukuran 16 bit untuk mengakses memori luar.

2.1.3. Timer / Counter

Pada mikrokontroler keluarga MCS-52 terdapat dua buah Timer/Counter. Dengan adanya timer/counter menambah fungsionalitas dari mikrokontroler ini. Sebagaimana peralatan lain pada mikrokontroler ini, timer/counter juga diatur oleh SFR (Special Function Register) yaitu Timer/Counter Control (TCON alamat 88H), dan Timer/Counter Mode Control (TMOD alamat 89H). Selain itu nilai byte bawah dan byte atas dari Timer/Counter disimpan dalam register TL dan TH. Jika difungsikan sebagai timer maka akan menggunakan sistem clock sebagai sumber masukan pulsanya, kemudian jika difungsikan sebagai counter (penghitung) maka akan menggunakan pulsa dari eksternal sebagai masukan pulsanya. Sebagaimana diketahui port 3 pada fungsi khususnya terdapat T0 (masukan luar untuk Timer/Counter 0) dan T1 (masukan luar untuk Timer/Counter 1).

2.1.3.1.Register TMOD

Register TMOD dibagi menjadi 2 bagian secara simetris, yaitu bit 0 – 3 register TMOD (TMOD bit 0..TMOD bit 3) dipakai untuk mengatur timer 0, dan bit 4 sampai 7 register TMOD (TMOD bit 4..TMOD bit 7) dipakai untuk mengatur timer 1, susunan bit dapat dilihat dibawah ini :

MSB LSB

Timer/Counter 1				Timer/Counter 0			
GATE	C/T	M1	M0	GATE	C/T	M1	M0

Keterangan :

Bit GATE = Jika bit ini diset timer akan berjalan hanya jika INT1 (P3.3) sedang tinggi. Jika bit ini diclear timer akan berjalan tanpa mempertimbangkan kondisi INT1.

Bit C/T = Saat bit ini diset timer akan menghitung kejadian pada T1 (P3.5) sebagai fungsi counter. Jika bit ini diclear maka timer akan menghitung tiap siklus mesin (sebagai fungsi timer).

Bit M0 dan M1 bit mode Timer/Counter

Tabel 2-4 Bit pemilih mode timer

M1	M0	Timer Mode	Keterangan
0	0	0	13 bit timer
0	1	1	16 bit timer
1	0	2	8 bit auto reload
1	1	3	split mode

2.1.3.2.Register TCON

Register TMOD dibagi menjadi 2 bagian secara simetris, bit 0 sampai 3 register TMOD (TMOD bit 0 .. TMOD bit 3) dipakai untuk mengatur Timer 0, bit 4 sampai bit 7 register TMOD (TMOD bit 4 .. TMOD bit 7) dipakai untuk mengatur timer 1, susunan bit dapat dilihat dibawah ini :

MSB							LSB
bit 7	bit 6	bit 5	bit 4	bit 3	bit2	bit 1	bit 0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Keterangan :

Bit (7) TF1 – Timer 1 overflow, diset oleh Mikrokontroler jika hitungan timer 1 melimpah (overflow).

Bit (6) TR1 = Timer 1 Run, jika bit ini diset maka timer 1 on, jika bit ini diclear maka timer 1 off.

Bit (5) TF0 = Timer 0 overflow, bit ini diset oleh Mikrokontroler saat timer 0 melimpah.

Bit (4) TR0 = Timer 0 Run, jika bit ini diset maka timer 0 on, jika diclear maka timer 0 off.

Bit (3) IE1 = Interupt 1 edge flag. Diset oleh hardware jika sisi suatu sela luar terdeteksi. Diclear jika instruksi RET1 dijalankan.

Bit (2) IT1 = Interupt 1 type. Berhubungan dengan sela luar 1. Fungsinya sama dengan IT0.

Bit (1) IE0 = Interupt 0 edge flag. Diset oleh hardware jika sisi suatu sela luar terdeteksi. Diclear jika instruksi RET1 dijalankan.

Bit (0) IT0 = Interupt 0 type. Sela luar 0 diterima melalui bit 2 pada port 3. Jika bit ini diset, maka INT0 dikenali pada sisi turun sinyal. Jika bit ini diclear maka suatu sela akan dikenali pada saat suatu sinyal low.

2.1.4. Metode Pengalamatan

Metode pengalamatan dengan menggunakan bahasa pemrograman assembler pada Mikrokontroler keluarga MCS-52 adalah sebagai berikut :

a. Pengalamatan Tak Langsung

Operand pengalamatan tak langsung menunjuk kearah sebuah register yang berisi lokasi alamat memori yang akan digunakan didalam operasi. Lokasi yang nyata tergantung pada isi register saat instruksi dijalankan . Untuk melaksanakan pengalamatan tak langsung digunakan simbol @.

```
ADD A,@R0       ; Tambahkan isi RAM yang lokasinya
                ; ditunjukan oleh register R0 ke Accumulator
DEC @R1         ; Kurangi satu isi Ram yang alamatnya
                ; oleh register R1
MOVX @DPTR,A    ; Pindahkan isi dari accumulator ke memori luar
                ; yang lokasinya ditunjukkan oleh data pointer
```

b. Pengalamatan Langsung

Pengalamatan langsung dilakukan dengan memberikan nilai ke suatu register secara langsung. Untuk melaksanakannya digunakan tanda #.

```
MOV A,#01H      ; Isi accumulator dengan bilangan 01H.
MOV DPTR,#20CDH ; Isi register DPTR dengan bilangan 20CDH.
```

Pengalamatan data langsung dari 0 sampai dengan 127 akan mengakses RAM internal, sedangkan pengalamatan dari 128 sampai 255 akan mengakses register perangkat keras.

```
MOV P3,A        ; Pindahkan isi accumualtor ke alamat data.
B0H             ; ( B0H adalah alamat port 3 ).
INC 60          ; Naikkan lokasi 60 (desimal) menjadi bernilai high.
```

c. Pengalamatan Bit.

Pengalamatan bit adalah penunjukan alamat lokasi bit baik dalam lokasi RAM internal (byte 32 sampai 37) maupun bit perangkat keras. Untuk melakukan pengalamatan bit digunakan simbol titik (.),

```
SET P1.3        ; Ubah bit ke 3 pada port 1 menjadi bernilai high
```

d. Pengalamatan Kode

Terdapat tiga macam yang dibutuhkan dalam pengalamatan kode, yaitu relative jump, in-block jump atau call dan long jump.

2.2. ADC (Analog Digital Converter) 0804

Agar dapat mengukur atau mengolah suatu variabel fisik yang umumnya dalam besaran analog dengan piranti digital, variabel tersebut harus diubah dahulu menjadi variabel digital yang nilainya proporsional dengan nilai variabel yang akan diukur atau diolah. Konversi ini dilakukan oleh konverter analog ke digital, ADC (*Analog to Digital Converter*).

Resolusi ADC didefinisikan sebagai voltage input yang diperlukan untuk 1 bit output dan dapat dinyatakan dengan persamaan berikut :

$$\text{Res} = \frac{\mathbf{E}}{\mathbf{2^N - 1}}$$

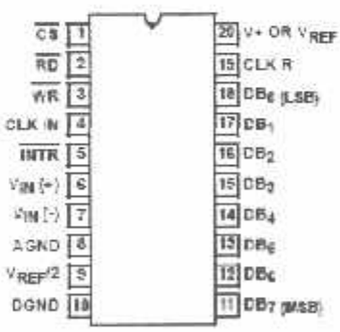
Atau jika dinyatakan dalam % Resolusi :

$$\%\ \text{Res} = \frac{\mathbf{E}}{\mathbf{2^N - 1}} \text{ x } 100\ \%$$

Resolusi ADC mengacu pada jumlah bit dalam keluaran biner ADC. Resolusi ADC 8-bit sama dengan $\left(\frac{1}{255}\right)$ x 100 %.

Spesifikasi penting selain ketelitian (akurasi) dan linearitas adalah waktu konversi (*converse time*). Waktu konversi ADC adalah waktu yang diperlukan ADC untuk menghasilkan kode biner yang valid untuk tegangan masukan yang diberikan. Semakin pendek waktu konversi, maka kecepatan konverter itu semakin tinggi. ADC yang banyak digunakan adalah :

1. *Counting* atau *Counter* ADC
2. *Successive Approximation* ADC (SAC)
3. *Paralel-Comparatoe* atau flash ADC
4. *Dual slope* atau ratiometrik ADC



Gambar 2-6 Konfigurasi PIN ADC 0804[6]
Sumber : Data sheet ADC 0804, www.alldatasheet.com

Fitur ADC 0804 :

- Kompatibel dengan mikroprosesor atau mikrokontroller tanpa memerlukan rangkaian *interfacing.*
- Dapat beroperasi dalam mode *stand alone* atau diinterfacekan ke mikroprosesor atau mikrokontroller
- Input tegangan analog yang differensial
- Generator clock on chip
- Tegangan input analog 0-5 V

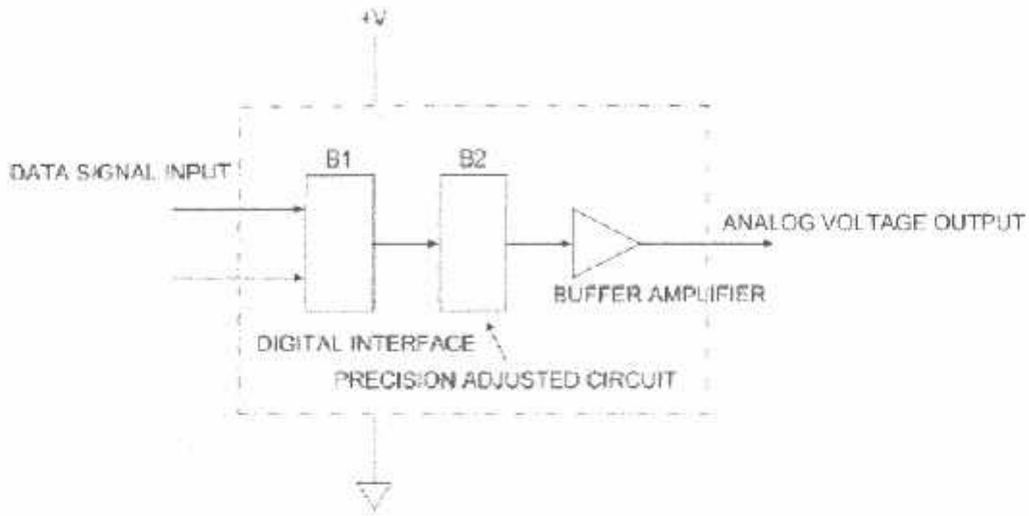
Spesifikasi :

- Resolusi 8 bit
- Error total ± 1 LSB
- Waktu konversi 100 µs
- Supply tegangan 5 V
- Bekerja pada temperatur 0° C sampai 70° C

2.3. DAC (Digital Analog Converter) 0808

Digital To Analog Converter (D/A) merubah N bit bilangan biner menjadi output tegangan analog yang memiliki 2^N nilai tegangan yang terpisah. Pada umumnya hubungan antara inputan digital dan output analognya adalah linier tetapi ada juga yang hubungan antara input dan outputnya berupa logaritmik.

Diagram blok sebuah konverter digital ke analog (DAC), ditunjukan pada gambar berikut :



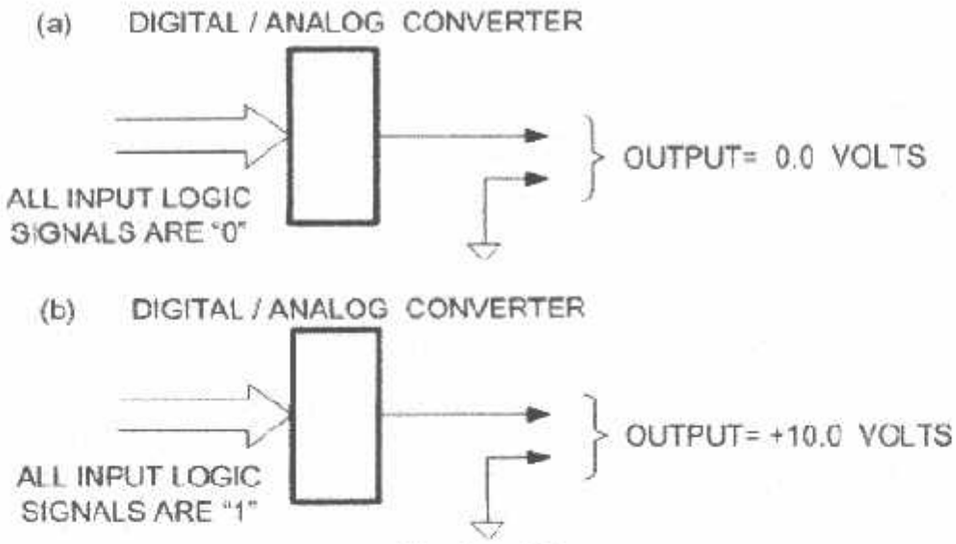
Gambar 2-7 . Diagram Blok DAC[7]

Blok diagram diatas terdiri atas 3 bagian, yaitu :

1. Perantara Digital
2. Rangkaian Pengatur Presisi
3. Penguat Baffer

Perantara digital akan menerima sinyal digital kemudian rangkaian pengatur presisi akan mengubah sinyal digital tersebut menjadi analog dan kemudian diperkuat oleh penguat baffer sebelum dikeluarkan.

Rangkaian pengatur presisi merupakan bagian terpenting dari konverter ini. Setting konverter ditentukan oleh tegangan acuan yang digunakan. Sebagai contoh, pada tegangan acuan = + 10 Volt jika input berlogika '1', maka tegangan output menjadi + 10 Volt, sedangkan jika logika semua input '0' maka tegangan output adalah 0 Volt. Pada konversi D/A semakin banyak bit-bit input maka akan semakin baik resolusi dan kecepatanya.



Gambar 2-8.

Hubungan Antara Sinyal – Sinyal Digital dan Output Tegangan Analog[8]

Dengan menggunakan metode numerik untuk menunjukan secara jelas, jika pada bagian input memiliki 10 jalur maka akan terdapat 2^{10} (1024) kombinasi, dimana kombinasi-kombinasi tersebut akan mengeluarkan output yang berbeda-beda sehingga berlaku :

1. Perubahan tegangan output minimum sama dengan besar perubahan tegangan maksimum dibagi dengan status maksimum kurang satu.
2. Perubahan tegangan output maksimum = $\text{Volt}_{(maks)} - \text{Volt}_{(min)}$

   $\text{Volt}_{(maks)}$ = 10 Volt

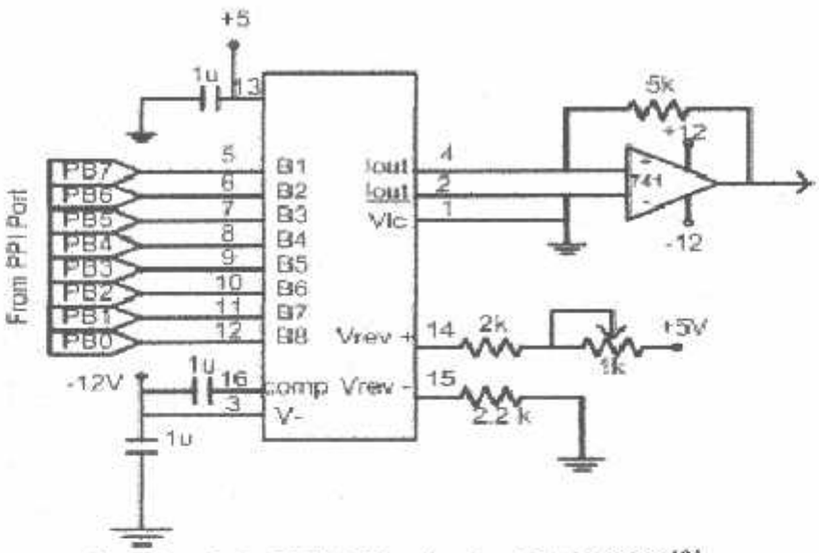
   $\text{Volt}_{(min)}$ = 0 Volt

   (Tegangan Referensi = 10 Volt), maka :

   Perubahan tegangan output maksimum = 10 – 0 = 10 Volt

   Status maksimum : status maksimum – 1 = 1024 – 1 = 1023

Perubahan tegangan output minimum $= \frac{10V}{1023} = 0{,}00975$



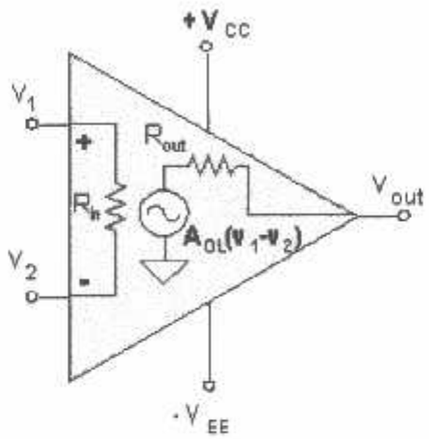
Gambar 2-9 . Digital To Analog (DAC) 0808[9]

2.4. Penguat (Op-amp)

Amplifier atau lazim disebut penguat dalam suatu rangkaian dapat difungsikan dalam suatu rangkaian penguat sinyal input, rangkaian penjumlahan tegangan input, rangkaian pembanding antara 2 sinyal input, rangkaian filter dan masih banyak lagi.

Rangkaian penguat ini sangat sederhana dalam pemakaianya baik secara merangkainya maupun dalam penggunaanya. Rangkaian ini terdiri dari kombinasi antara pengutan operasional yang dirangkai bersama kompenen pasif tahanan atau kondensator. Dengan kombinasi ini dapat dikembangkan lagi menjadi rangkaian yang mempunyai spesifikasi khusus seperti rangkaian instrumentasi, rangkaian isolator, dan lain sebagaianya. Gambar 2-7 menunjukan simbol dari op-amp

dengan lima terminal dasar terdiri dari 2 terminal catu daya, 2 terminal input atau masukan yaitu (+) dan (-) dan terminal output atau keluaran dari op-amp.



Gambar 2-10. Simbol Op-Amplifier[10]

2.5. Transistor

Prinsip kerja transistor adalah arus bias base - emitter yang kecil mengatur besar arus besar kolektor – emitter. Bagian penting berikutnya adalah bagaimana caranya memberi arus bias yang tepat sehingga transistor dapat bekerja optimal.

2.5.1 Arus Bias

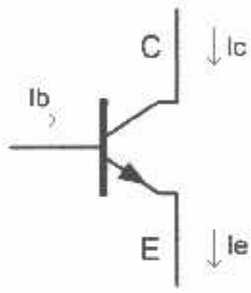
Ada tiga cara yang umum untuk memberi arus bias pada transistor, yaitu rangkaian CE (Common Emitter), CC (Common Colector, CB (Common Base). Namun saat ini akan lebih detil jika dijelaskan bias transistor rangkaian CE. Dengan menganalisa rangkaian CE akan dapat diketahui beberapa parameter penting dan berguna, terutama untuk memilih transistor yang tepat untuk aplikasi

tertentu. Misalnya untuk aplikasi pengolahan sinyal audio tentu saja tidak menggunakan transistor power.

2.5.2 Arus Emitor

Dari Hukum Kirchoff diketahui bahwa jumlah arus yang masuk ke satu titik akan sama dengan arus yang keluar. Jika teorema tersebut diaplikasikan pada transistor, maka hukum itu menjelaskan hubungan :

$$I_E = I_C + I_B$$



Gambar 2–11 Arus Emitor[11]
Sumber: www.electroniclab.com, rubrik elka analog, aswan hamonangan

Persamaan di atas mengatakan arus emitor I_E adalah jumlah dari arus kolektor I_C dengan arus base I_B. karena arus I_B sangat kecil sekali atau disebutkan $I_B << I_C$, maka dapat dinyatakan :

$$I_E = I_C$$

2.5.3 Daerah Aktif

Daerah kerja transistor yang normal adalah pada daerah aktif, dimana arus I_C konstan terhadap berapapun nilai V_{CE}. Dari kurva ini diperlihatkan bahwa arus

I_C hanya bergantung pada besar arus I_B. dacrah kerja ini biasa disebut juga daerah linear (*linear region*).

Jika Hukum Kirchoff mengenai tegangan dan arus diterapkan pada loop kolektor (rangkaian CE), maka dapat diperoleh hubungan :

$$V_{CE} = V_{CC} - I_C \cdot R_C$$

Dapat dihitung dissipasi daya transistor adalah :

$$P_D = V_{CE} \cdot I_C$$

Rumus ini mengatakan jumlah dissipasi daya transistor adalah tegangan kolektor – emitter dikalikan dengan jumlah arus yang melewatinya. Dissipasi daya ini berupa panas yang menyebabkan naiknya temperature transistor. Umumnya untuk transistor power sangat perlu untuk mengetahui spesifikasi P_{Dmax}. Spesifikasi ini menunjukkan temperatur kerja maksimum yang diperbolehkan agar transistor masih bekerja normal. Sebab jika transistor bekerja melebihi kapasitas daya P_{Dmax}, maka transistor dapat rusak atau terbakar.

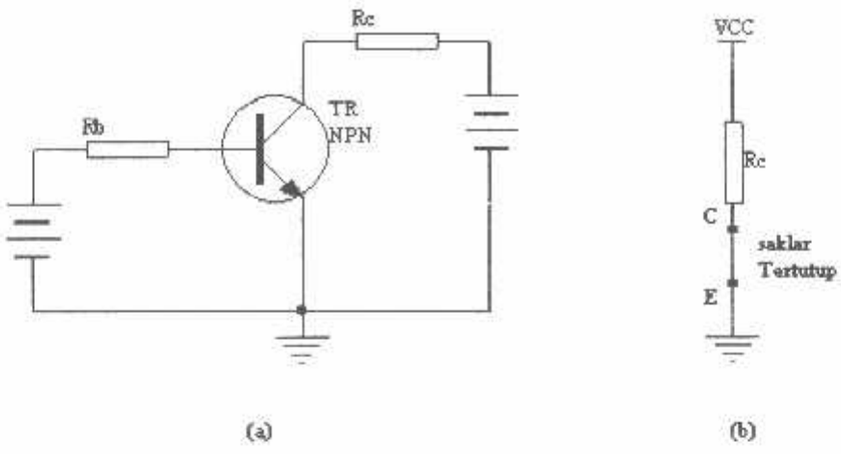
2.5.4 Daerah Saturasi (Dalam Keadaan Jenuh)

Daerah Saturasi adalah mulai dari V_{CE} = 0 Volt sampai dengan kira - kira 0,7 Volt (transistor silikon), yaitu akibat dari efek dioda kolektor - base yang mana tegangan V_{CE} belum mencukupi untuk dapat menyebabkan aliran elektron.

Transistor dalam keadaan jenuh (saturasi), maka berlaku :

- Kuat arus (I_c) mencapai maksimum
- V_{ce} sama dengan 0 volt
- Tegangan pada beban sama dengan tegangan sumber (V_{cc}=V_{Rc})

Untuk lebih jelasnya dapat dilihat pada gambar dibawah ini :



Gambar 2-12 (a) Transistor dalam keadaan saturasi (b) Rangkaian ekuivalen[12]
Sumber: www.electroniclab.com, rubrik elka dasar, aswan hamonangan

Untuk menghitung resistansi pada basis menggunakan rumus :

$$V_{CC} - I_C.R_C - V_{CE} = 0$$

Karena keadaan saturasi $V_{ce} = 0$ maka rumurnya menjadi :

$$V_{CC} - I_C.R_C = 0$$

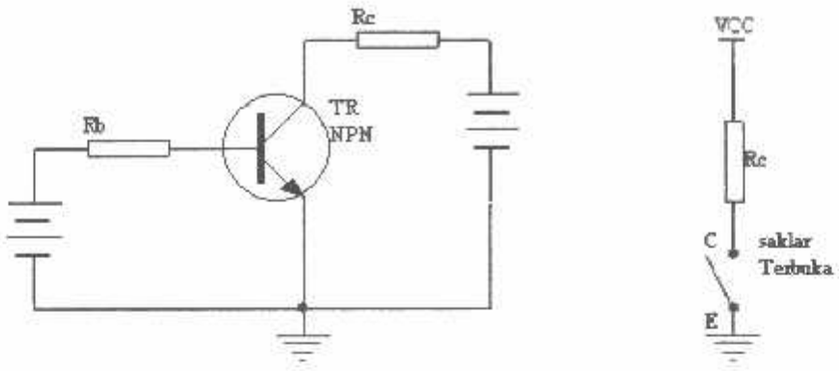
$$I_C = \beta_{dc}.\ I_B$$

$$I_B = \frac{(V_{CC} - V_{BE})}{R_B}$$

2.5.5 Daerah Cut-Off (Sumbat)

Transistor dalam keadaan cut off (sumbat) berlaku hal-hal sebagai berikut :

- Arus I_b sama dengan 0 volt
- Arus I_c sangat kecil sekali sehingga dapat diabaikan
- V_{cc} sama V_{ce}

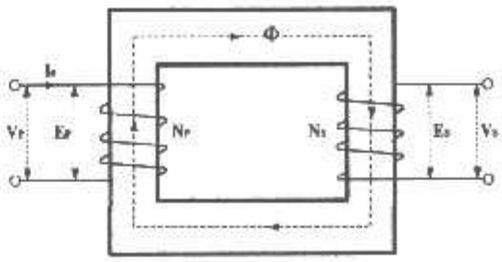


Gambar 2-13 (a) Transistor dalam Keadaan Cutt Off (b) Rangkaian ekuivalen[13]
Sumber: www.electroniclab.com, rubrik elka dasar, aswan hamonangan

Jika kemudian tegangan V_{CC} dinaikkan perlahan - lahan sampai tegangan V_{CE} tertentu tiba - tiba arus I_C mulai konstan. Pada saat perubahan ini, daerah kerja transistor berada pada daerah *cut-off*, yaitu dari keadaan saturasi (OFF) lalu menjadi aktif (ON). Perubahan ini dipakai pada sistem digital yang hanya mengenal angka biner 0 dan 1 yang tidak lain dapat direpresentasikan oleh status transistor OFF dan ON.

2.6 Transformator

Transformator adalah suatu alat listrik yang dapat memindahkan dan mengubah energi listrik dari satu atau lebih rangkaian listrik ke rangkaian listrik yang lain melalui suatu gandengan magnet dan berdasarkan prinsip induksi elektromagnet. Prinsip kerja transformator berdasarkan induksi magnet antara rangkaian primer dan rangkaian sekunder. Gandengan magnet berupa inti besi tempat melakukan fluks bersama-sama. Seperti ditunjukkan pada gambar beriikut:



Gambar 2-14 Transformator[14]
Sumber: Zuhal, Dasar Tenaga Listrik, ITB Bandung, 1991 [p.4]

Dalam bidang tenaga listrik pemakaian transformator dikelompokkan menjadi:

1. Transformator daya.
2. Transformator distribusi.
3. Transformator pengukuran, yaitu terdiri dari: transformator arus dan transformator tegangan.

Cara kerja transformator berdasarkan induksi elektromagnetik, yaitu:

Apabila kumparan primer dihubungkan dengan tegangan bolak-balik, maka akan mengalirkan arus bolak-balik (I_1) pada kumparan tersebut. Oleh karena kumparan mempunyai inti, maka arus I_1 akan menimbulkan fluks magnet yang berubah-ubah pada intinya. Sehingga kumparan primer akan timbul GGL induksi E_p. Besarnya GGL induksi pada kumparan primer (E_p) adalah:

$$E_p = - N_p \frac{d\phi}{dt} \text{ Volt}$$

$$E_p = - N_p \frac{d(\phi_{max} . Sin\omega t)}{dt} = - N_p . \omega\phi_{maks} . \text{Cos } \omega t$$

Harga Efektifnya:

$$E_p = \frac{N_p . 2\pi . f . \phi_{max}}{\sqrt{2}} = 4{,}44 \; N_p . f . \phi_{maks}$$

Pada rangkaian sekunder, fluks (Φ) bersama tadi menimbulkan:

$$E_s = - N_s \frac{d\phi}{dt} \text{ Volt}$$

$$E_s = - N_s \frac{d(\phi_{maks}.Sin\omega t)}{dt} = N_s.\omega\phi_{maks}.\text{Cos } \omega t$$

$$E_s = \frac{N_s.2\pi.f.\phi_{maks}}{\sqrt{2}} = 4{,}44\ N_s.f.\phi_{maks}$$

Apabila transformator dianggap ideal, maka dianggap tidak terdapat kerugian daya. Perbandingan antara EMF pada primer dan sekunder adalah:

$$A = \frac{E_p}{E_s} = \frac{V_p}{V_s} = \frac{N_p}{N_s} = \frac{I_p}{I_s}$$

Sumber: Zuhal, Dasar Tenaga Listrik, ITB Bandung, 1991 [p.4]

Keterangan:

a = Perbandingan ratio transformasi EMF pada primer dan sekunder.

E_p = Tegangan induksi yang dibangkitkan oleh lilitan primer (Volt).

E_s = Tegangan induksi yang dibangkitkan oleh lilitan sekunder (Volt).

N_p = Banyaknya lilitan pada sisi primer.

N_s = Banyaknya lilitan pada sisi sekunder.

I_P = Arus pada sisi primer (Ampere).

I_s = Arus pada sisi sekunder (Ampere).

V_p = Tegangan sumber yang masuk pada sisi primer (Volt)

V_s = Tegangan sekunder ke beban (Volt).

2.6.1 Sensor Tegangan (Transformator Tegangan)

Transformator tegangan berguna untuk menurunkan tegangan dari jala-jala menjadi tegangan yang dibutuhkan oleh ADC dan mikrokontroller untuk bisa bekerja, yaitu sebesar 0 – 5 Volt. Karena tegangan yang diukur adalah tegangan +220volt, maka diperlukan adanya transformator penurun tegangan (transformator stepdown). Tegangan ini kemudian disearahkan atau diubah menjadi tegangan DC agar dapat diterjemahkan menjadi tegangan digital oleh rangkaian ADC 0804. Dengan mengetahui N_1 dan N_2, membaca tegangan V_2, serta menganggap transformator ideal maka tegangan V_1 adalah:

$$V_1 = \frac{N_1}{N_2} \times V_2$$

Pentanahan rangkaian sekunder diperlukan untuk mencegah adanya beda potensial yang besar antara kumparan primer dan kumparan sekunder.

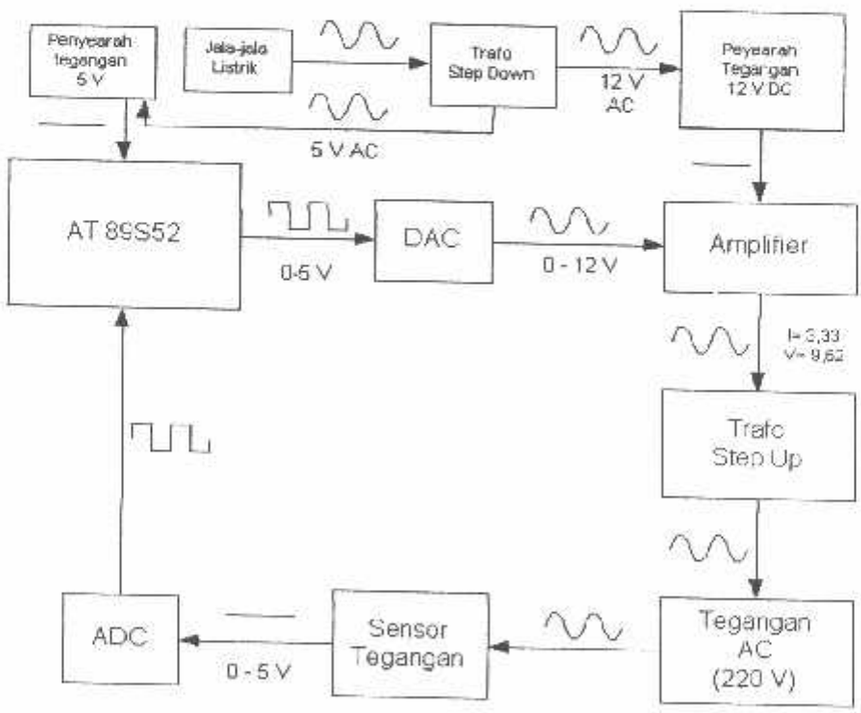
BAB III

PERENCANAAN DAN PEMBUATAN ALAT

Bab ini akan membahas tentang perencanaan dan pembuatan inverter berbasis mikrokontroler AT89S52 yang meliputi perancangan perangkat keras (*hardware*) dan perangkat lunak (*software*), untuk lebih detailnya akan dijelaskan pada sub bab berikut ini :

3.1.Diagram Blok Rangkaian

Secara garis besar, prinsip kerja alat ini dapat digambarkan melalui blok diagram dibawah ini:



Gambar 3-1 Blok Diagram Rangkaian

Prinsip kerja dari blok diagram diatas adalah :

- ***Jala-jala Listrik***, berfungsi sebagai sumber tegangan
- ***Penyearah Tegangan***, berfungsi untuk meyearahkan tegangan yang tegangan 220 Volt (AC) menjadi 12 Volt dan 5 Volt (DC).
- ***Mikrokontroler AT89S52***, berfungsi untuk pengendalian dari kescluruan sistem.
- ***Digital Analog Converter (DAC)*** berfungsi untuk mengubah data digital menjadi data analog.
- ***Amplifier*** berfungsi sebagai penguat tegangan.
- ***Trafo Step Up*** berfungsi untuk menaikan tegangan dari 12 Volt menjadi 220 Volt (AC).
- ***Tegangan AC 220 Volt / Output*** hasil dari inverter tegangan DC menjadi tegangan AC.
- ***Sensor Tegangan*** berfungsi untuk mengetahui apakah tegangan sudah 220 Volt (AC).
- ***Analog Digital Converter (ADC)*** befungsi untuk mengubah data analog menjadi data digital.

3.2. Perencanaaan Hardware

Dalam perencanaan ini rancangan *hardware* yang dibuat bertujuan guna mendukung dan memberikan kemudahan pada proses kerja perancangan *software* agar nantinya sesuai dengan kondisi yang diinginkan, untuk perancangan *hardware* sendiri dibagi menjadi 9 bagian yaitu :

1. Minimum System AT89S52
2. Digital Analog Converter (DAC) 0808
3. Amplifier
4. Sensor Tegangan
5. Analog Digital Converter (ADC) 0804

3.2.1 Perancangan minimum sistem mikrokontroller AT89S52

Penggunaan mikrokontroller AT89S52 harus didukung oleh beberapa rangkaian penunjang agar dapat melakukan fungsinya, antara lain rangkaian *clock* dan rangkaian reset. Selain itu juga harus ditentukan penggunaan port-portnya untuk rangkaian pendukung yang lain.

3.2.1.1 Rangkaian *clock*

Kecepatan proses pengolahan data pada mikrokontroller ditentukan oleh *clock* (pewaktu) yang dikendalikan oleh mikrokontroller tersebut. Pada mikrokontroller AT89S52 terdapat *internal clock generator* yang berfungsi sebagai sumber *clock*, tapi masih memerlukan rangkaian tambahan untuk membangkitkan *clock* yang diinginkan.

Rangkaian tambahan ini terdiri atas 2 buah kapasitor dan sebuah kristal yang terangkai sedemikian rupa dan kemudian dihubungkan dengan port yang khusus tersedia pada mikrokontroller.

Dalam perancangan rangkaian ini menggunakan :

- 2 Kapasitor 30 pF. Penentuan besarnya kapasitansi disesuaikan dengan spesifikasi pada data sheet.

- Kristal 11,0592 MHz.

Dengan demikian perhitungannya dapat dilihat sebagai berikut :

f = 11,0592 MHz

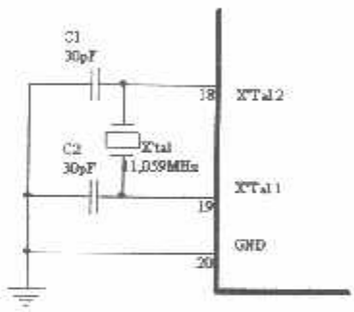
$$T = \frac{1}{f}$$

$$T = \frac{1}{11{,}0592x10^{6}}$$

karena 1 siklus mesin = 12T maka

$$1 \text{ siklus mesin} = 12 \text{ x } \frac{1}{11{,}0592x10^{6}} = 1{,}085 \ \mu s$$

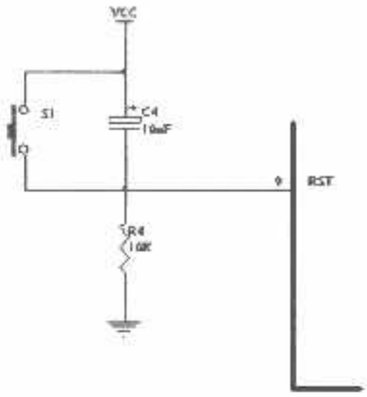
Adapun gambar rangkaian *clock* sebagai berikut :



Gambar 3-2 Rangkaian *clock*

3.2.1.2 Rangkaian *reset*

Reset pada mikrokontroller merupakan masukan aktif *high* '1' pulsa transisi dari rendah '0' ketinggi akan me-*reset* mikrokontroller menuju alamat 0000H. Pin *reset* dihubungkan dengan rangkaian *power-on reset* seperti pada gambar berikut :



Gambar 3-3 Rangkaian *Reset*

Rangkaian *reset* bertujuan agar mikrokontroller dapat menjalankan proses dari awal. Rangkaian *reset* untuk mikrokontroller dirancang agar mempunyai kemampuan *power on reset*, yaitu *reset* yang terjadi pada saat sistem dinyalakan untuk pertama kalinya. *Reset* juga bias dilakukan secara manual dengan menekan tombol *reset* yang berupa *switch push button.*

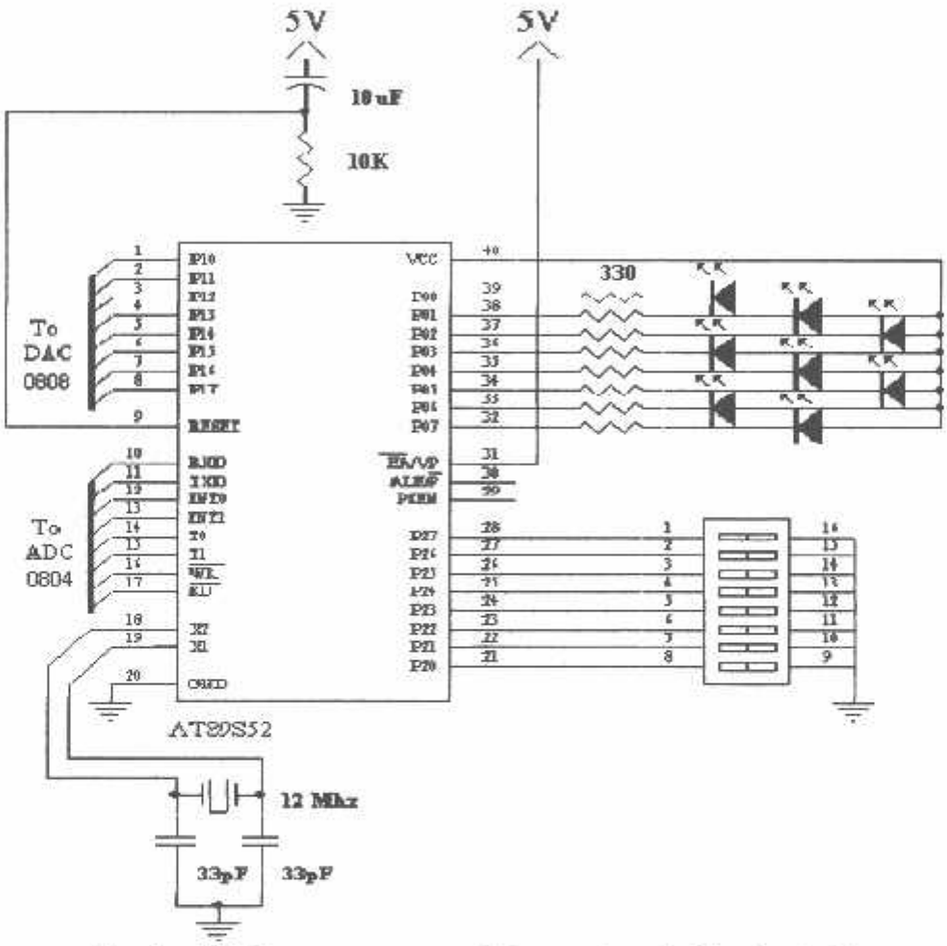
Rangkaian *reset* terbentuk oleh komponen Resistor dan kapasitor yang sudah baku (ditetapkan oleh perusahaan pembuat IC AT89S52). Nilai Resistor yang dipakai adalah 10KΩ dan kapasitor 10µF. Besar nilai tahanan dan kapasitor pada rangkaian tersebut akan menentukan lama waktu pulsa *reset.*

3.2.1.3 Perancangan penggunaan port-port pada mikrokontroller AT89S52

Pada skripsi ini mikrokontroller AT89S52 digunakan sebagai pusat pengendali kerja dari alat yang dibuat kerena disinilah tersimpan program-program *(software)* perintah serta alamat yang akan dituju program. Untuk

melaksanakan fungsi tersebut diatas maka perlu dirancang port-port I/O yang akan digunakan.

Gambar 3-6 menunjukkan rancangan port-port I/O pada mikrokontroller AT89S52 yang dimanfaatkan pada skripsi :



Gambar 3-4 Perancangan pemakaian port-port mikrokontroller

1. Port 0

   Port 0.0 – Port 0.7 (pin 32 – 39) digunakan sebagai port keluaran untuk lampu led.

2. Port 1

   Port 1.0 – Port 1.7 (pin 1 – 8) digunakan sebagai outputan data yang dikirim untuk DAC

3. Port 2

   Port 2.0 – Port 2.7 (pin 21 – 28) digunakan sebagai output data yang dikirim untuk saklar dip swit.

4. Port 3

   Port 3.0 – Port 3.7 (pin 10 – 17) digunakan sebagai inputan data yang diterima dari ADC

5. Pin 9 (*reset)* dihibungkan dengan rangkaian reset

6. Pin 18 dan pin 19 dihubungkan dengan rangkaian rangkaian *clock* atau *Oscillator external*

7. Pin 31 (EA) diberi logika tinggi (*high)* atau dihubungkan dengan Vcc maka mikrokontroller akan mengakses program dari ROM internal (EPROM atau *flash memory*)

8. Pin 29 dan pin 30 (ALE/PROG dan PSEN) tidak digunakan karena pada pembuatan alat ini tidak menggunakan atau mengakses *memory eksternal*

9. Pin 40 (Vcc) dihubungkan dengan tegangan *supply* +5V

10. Pin 20 (GND) dihubungkan dengan tegangan *supply ground*

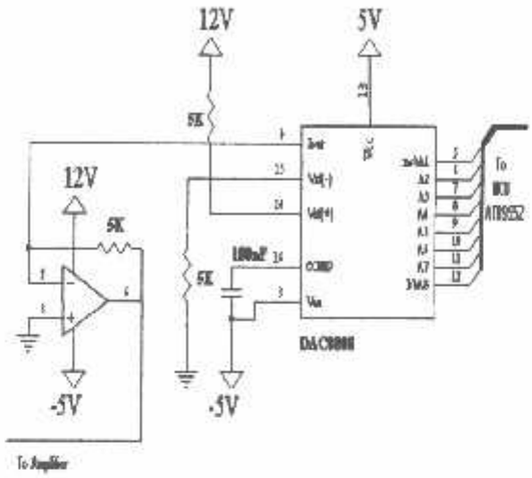
3.3. Rangkaian Digital Analog Converter (DAC) 0808

Digital To Analog Converter (D/A) merubah N bit bilangan biner menjadi output tegangan analog yang memiliki 2^N nilai tegangan yang terpisah. Pada umumnya hubungan antara inputan digital dan output analognya adalah linier tetapi ada juga yang hubungannya antara input dan outputnya berupa logaritmik.

Untuk N bit linier D/A converter, output analog yang idial adalah V(n) yang merupakan fungsi linier dari digital input n antara dua tegangan reverensi $V_{ref(-)}$ dan $V_{ref(+)}$

Gambar 3-5 menunjukkan rancangan port-port pada Digital Analog Converter (DAC) 0808.

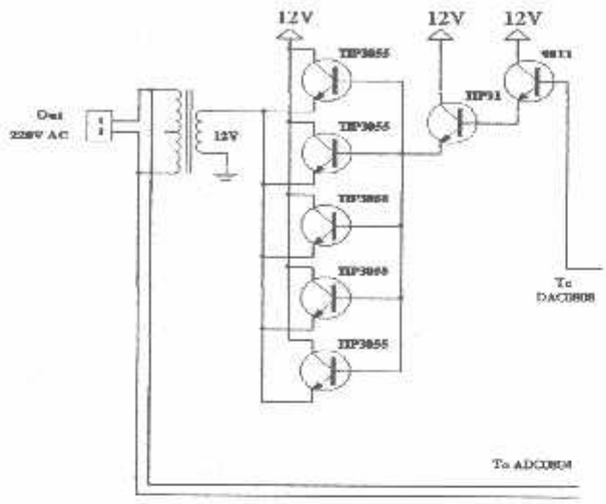
1. Pin 5 – 12 digunakan sebagai port keluaran dari mikrokontroler AT89S52
2. Pin 4 diguanakan sebagai port inputan untuk rangkaian penguat
3. Pin 3 dan 16 dihubungkan dengan tegangan *supply* – 5 Volt
4. Pin 14 (Vrf +) dihubungkan dengan tegangan *supply* 12 Volt
5. Pin 15 (Vrf -) dihubungkan dengan tegangan *supply ground*
6. Pin 13 (VCC) dihubungkan dengan tegangan *supply* + 5 Volt



Gambar 3-5 Rangkaian DAC 0808 (Digital Analog Converter)

3.4. Rangkaian Amplifier

Rangakaian amplifier disini menggunakan transistor sebagai penguat, selain sebagai saklar transistor juga digunakan sebagai penguat. Setelah membias transistor dalam daerah aktif, kita dapat memasang tegangan AC pada dioda emitor untuk menimbulkan fluktuasi dalam arus kolektor. Jika arus kolektor ini mengalir melalui resistor luar, pembesaran sinyal ini disebut penguatan. Jika menggunakan transistor sebagai penguat untuk mengukur tegangan transistor ke tanah sering digunakan voltmeter. Karena alasan ini maka harus memperkirakan berapa tegangan AC yang ada dalam penguat. Tiga tegangan Ac dasar dalam penguat transistor adalah tegangan kolektor ketanah Vc, tegangan emitor ke tanah Ve dan tegangan basis ke bawah Vb.



Gambar 3-6 Rangkaian Amplifier

Transistor yang digunakan pada amplifier salah satunya adalah 9013 diketahui dari data sheet transistor 9013 besarnya Ic = 100mA, hfe = 110, V_{BE} = 0,7 Volt, sehingga :

$$R_B = \frac{V_{BE} - V_{BE}}{I_B} \quad \text{.....(1.1)}$$

$$I_B = \frac{I_C}{hfe} \quad \text{.....(1.2)}$$

$$I_C = I_E - I_B \quad \text{.....(1.3)}$$

maka I_B pada transistor 9013

$$I_B = \frac{100mA}{110} = 0{,}909mA$$

Maka R_B adalah :

$$R_B = \frac{5-0,7}{0,909} = 4,73 \times 10^3 \Omega$$

R_B sebesar $4,73 \times 10^3 \Omega \approx 5k\,\Omega$

Pada Transistor Tip 31 diketahui dari data sheet besarnya Ic = 500mA, hfe = 135

Maka I_B pada transistor TIP 31

$$I_B = \frac{500}{135} = 3,7mA$$

$I_E = 500 + 3,7$

$I_E = 503,7$ mA

Pada transistor Tip 3055 diketahui dari data sheet besarnya Ic = 1A, dan hfe = 45

Maka I_B pada transistor TIP 3055

$$I_B = \frac{1}{45} = 0,022A$$

$I_E = 1 + 0,022$

$I_E = 1,022$A

3.5. Rangkaian Sensor Tegangan dan Analog Digital Converter (ADC) 0804

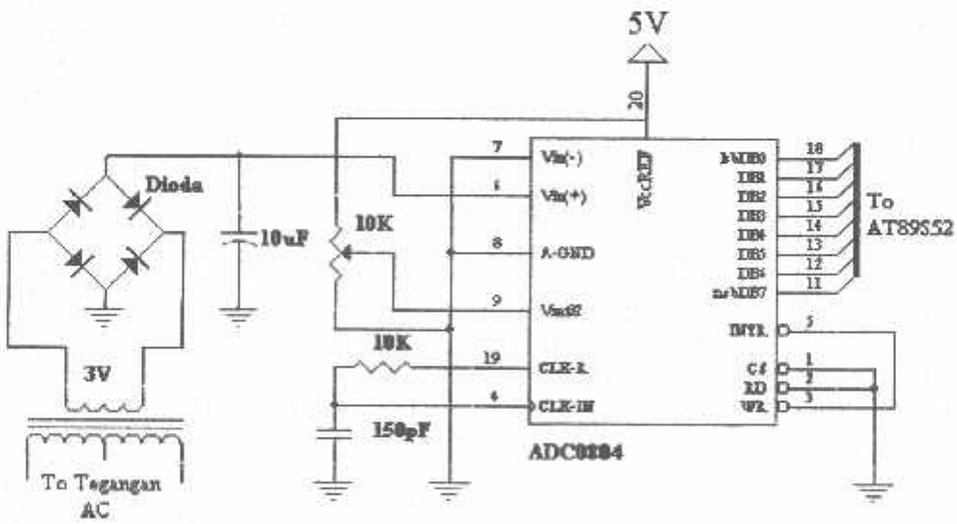
Transformator tegangan berguna untuk menurunkan tegangan dari jala-jala menjadi tegangan yang dibutuhkan oleh ADC dan mikrokontroller untuk bisa bekerja, yaitu sebesar 0 – 5 Volt. Karena tegangan yang diukur adalah tegangan ±220volt, maka diperlukan adanya transformator penurun tegangan (transformator stepdown). Tegangan ini kemudian disearahkan atau diubah menjadi tegangan DC

agar dapat diterjemahkan menjadi tegangan digital oleh rangkaian ADC 0808. Dengan mengetahui N_1 dan N_2, membaca tegangan V_2, serta menganggap transformator ideal maka tegangan V_1 adalah:

$$V_1 = \frac{N_1}{N_2} \times V_2$$

Pentanahan rangkaian sekunder diperlukan untuk mencegah adanya beda potensial yang besar antara kumparan primer dan kumparan sekunder.

ADC yang digunakan adalah ADC 0804 yang merupakan ADC satu kanal input dengan output pararel 8 bit. Agar ADC dapat bekerja secara optimal maka diberi catu daya 5 volt. ADC 0804 telah dilengkapi *clock internal* yang dapat diaktifkan dengan menghubungkan dengan tahanan dan kapasitor *eksternal.*



Gambar 3-7 Rangkaian sensor tegangan dan Analog Digital Converter (ADC) 0804

Nilai tahanan R2 ditentukan sebesar 10 KΩ dan nilai kapasitor C2 sebesar 150 pF, sehingga memberikan frekuensi *clock* sebesar :

$$F = \frac{1}{1{,}1RC} = \frac{1}{1{,}1x10K\Omega x150pF} = 606{,}06\ KHz$$

Berdasarkan frekuensi *clock* diatas, maka waktu konversi maksimum yang dibutuhkan ADC adalah :

$$T = \frac{2^n}{f} = \frac{2^8}{606{,}06x10^3} = 0{,}42\ ms$$

ADC ini dirancang agar dapat menerima tegangan input antara 0 – 4,5 Volt. Pada perencanaan ini diberikan tegangan reverensi (Vref/2) pada pin 9 sebesar 2,25 volt. Untuk mendapatkan Vref/2 digunakan rangkaian resistor pembagi tegangan yang terdiri dari 2 buah resistor yang terhubung secara seri, Pada perancangan, salah satu resistor digunakan *variable* resistor sebesar 10KΩ sehingga tegangan keluarannya dapat diatur sesuai dengan kebutuhan.

Dengan Vref/2 sebesar 2,25 Volt maka ADC akan memiliki resolusi sebesar

$$\text{Resolusi} = 2 \text{ x } \frac{Vref/2}{2^n - 1} \text{ Volt / step}$$

$$= 2 \text{ x } \frac{2{,}25}{2^8 - 1} \text{ Volt / step } = 17{,}65 \text{ mV / step}$$

3.6. Sistem DDS (Direct digital Synthesis)

Sistem DDS (Direct digital Synthesis) merupakan salah satu cara untuk menghasilkan sinyal sinusoida secara langsung. Inti dari sistem ini adalah arsitektur akumulator dengan resolusi mencapai mili Hertz dan frekuensi sinyal

yang dihasilkan dapat diatur tergantung dari sinyal frekuesi referensi dan metode perancangan. Keluaran sistem DDS yang diproses oleh mikrokontroler berupa sinyal digital kemudian menjadi masukan untuk DAC (D/A converter) dan LPF (Low Pass Filter) untuk menghasilkan sinyal sinusoida yang sempurna.

Semua parameter kontrol sistem DDS berada dalam bentuk digital. Sistem DDS pada dasarnya terdiri atas akumulator phasa, LUT (Look Up Table), dan osilator sebagai pembangkit frekuensi referensi (clock). Sedangkan DAC (Digital To Analog Converter) dan LPF (Low Pass Filter) merupakan komponen-komponen penunjang sistem DDS

3.7. Kelebihan Dan Flesibilitas DDS

Kelebihan penggunaan Sistem DDS adalah karateristik sistem DDS itu sendiri, dimana keutamaan dari sistem ini adalah memiliki setting time/kecepatan yang cepat dan memiliki resulusi frekuensi yang halus terhadap frekuensi keluaran, operasi atas suatu sepektrum frekuensi yang lebar dan dengan kemajuan dalam desain teknologi proses. Serta sangat ringkas dan sedikit membutuhkan daya. Sehingga sangat memungkinkan sistem DDS bisa lebih dikembangkan untuk desain alat yang berkaitan dengan aplikasi-aplikasi frekuensi hopping serta sistem-sistem yang berkaitan dengan peralatan pemancar radio,TV,peralatan test, dll.

Figure 1-4. Signal flow through the DDS architecture

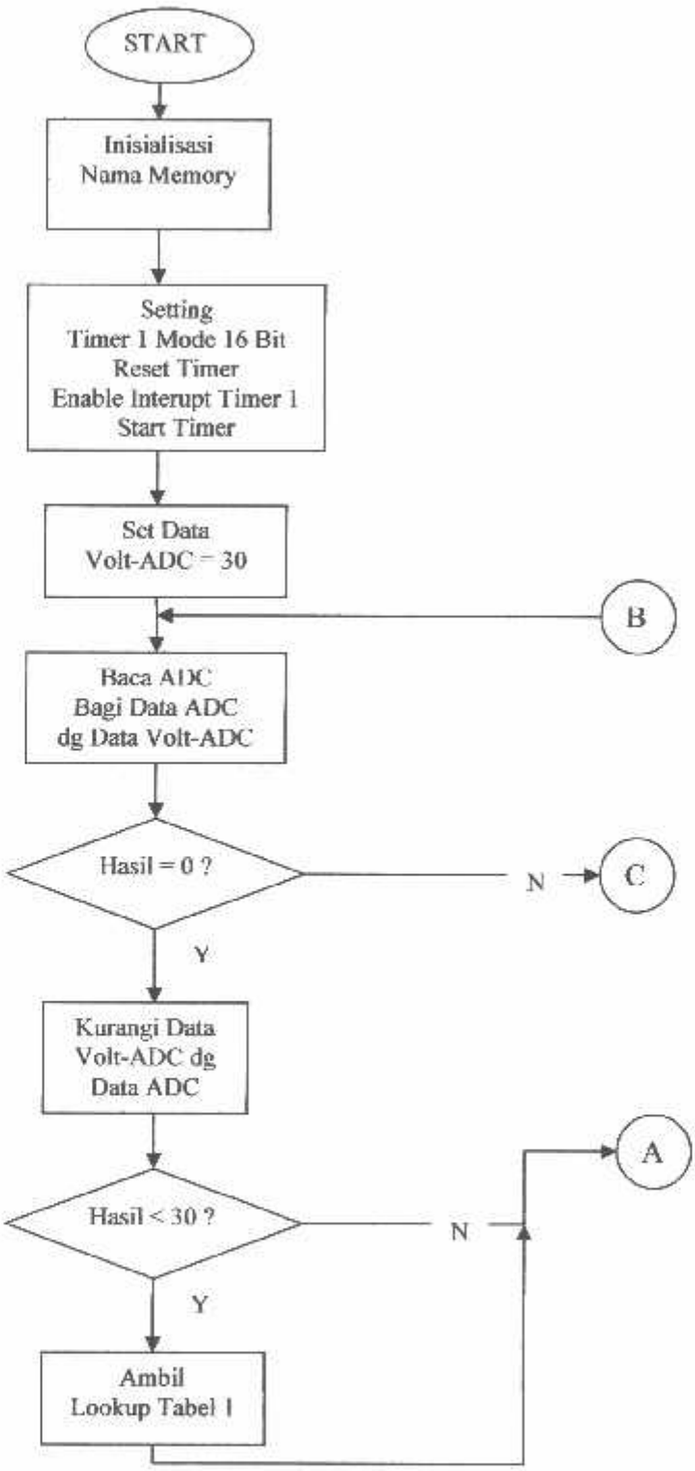
Gambar 3-8 Signal Sinusoida Direct Digital Synthesis (DDS)

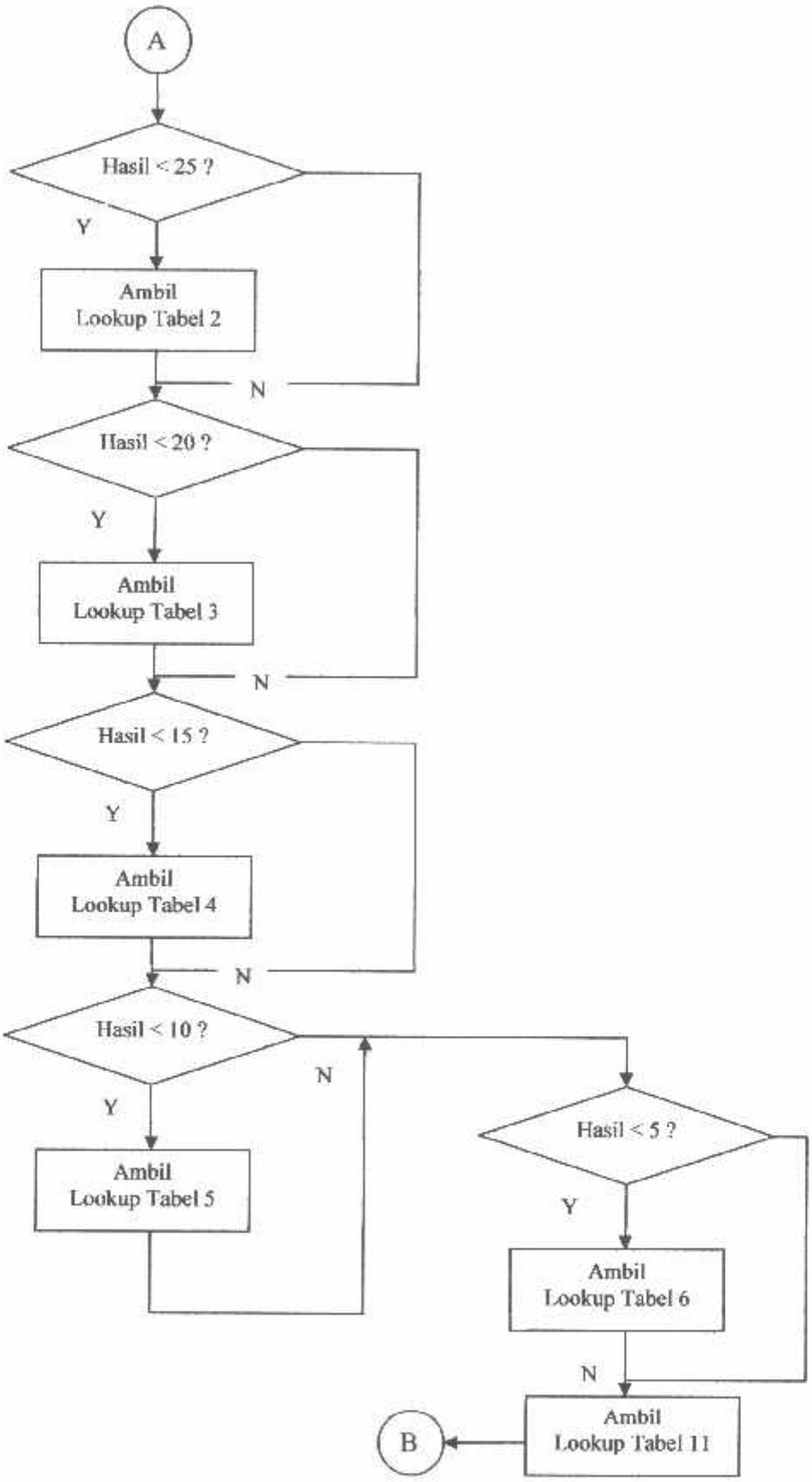
3.8. Perancangan Perangkat Lunak

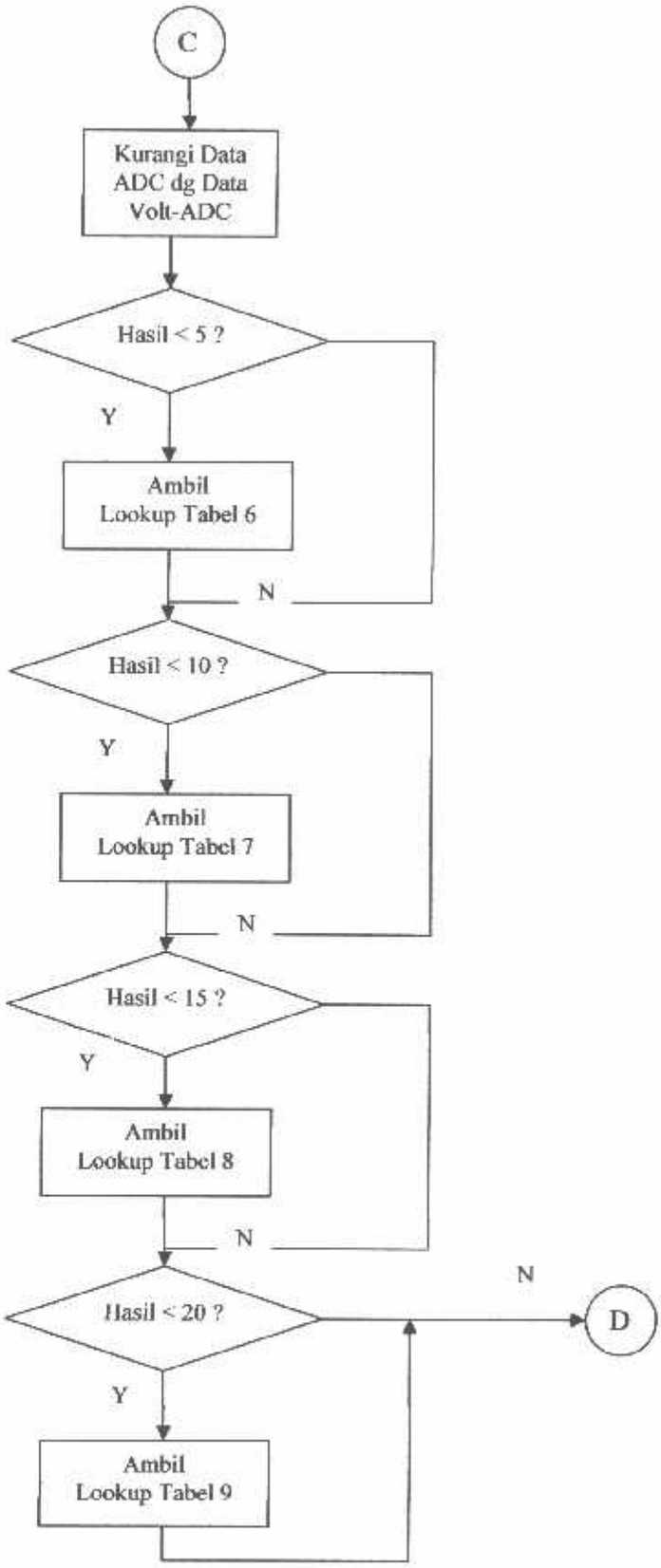
Dalam menunjang kerja sistem secara keseluruhan diperlukan suatu perangkat lunak (*software*). *Software* yang digunakan untuk AT89S52 disini menggunakan bahasa *assembler* keluarga MCS52. Program yang ditulis dengan bahasa assembly terdiri dari *label; kode mnemonic* dan lain sebagainya yang pada umumnya dinamakan sebagai program sumber (*source code*) yang belum bisa diterima oleh prosesor untuk dijalankan sebagai program, tetapi harus dijalankan dulu menjadi bahasa mesin dalam bentuk *kode biner*.

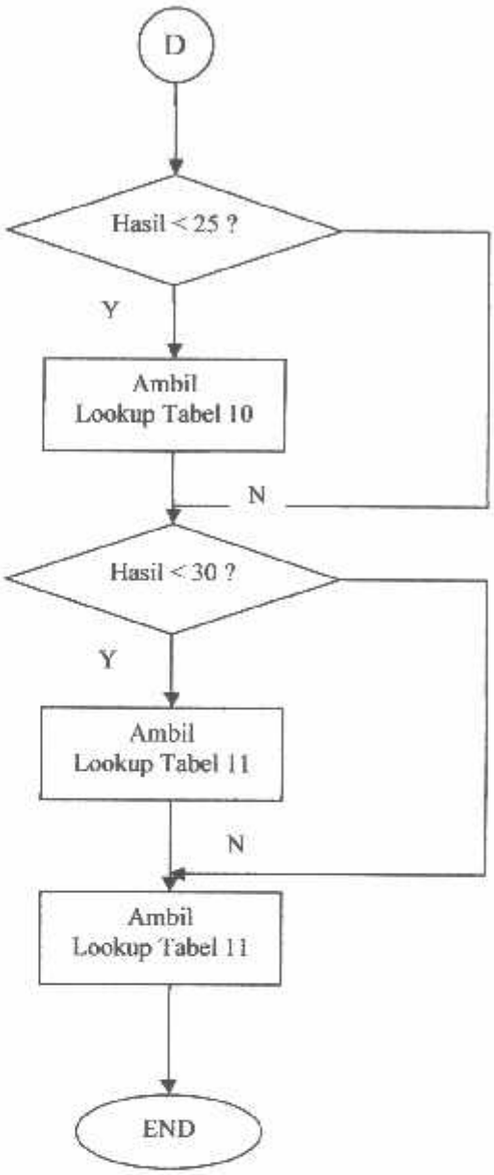
- Penulisan program dengan menggunakan teks editor dan disimpan dengan ekstensi *Asm*.
- Meng-compile program yang telah ditulis dengan menggunakan Compiler MCS52 sehingga didapatkan file dengan ekstensi *Hex*.
- Mengubah file berekstensi *Hex* menjafi file berekstensi *Bin*.
- Men-download file berekstensi Bin ke dalam EPROM Mikrokontroler AT89S52.

3.8.1. Flow Chart Kerja Rangkaian

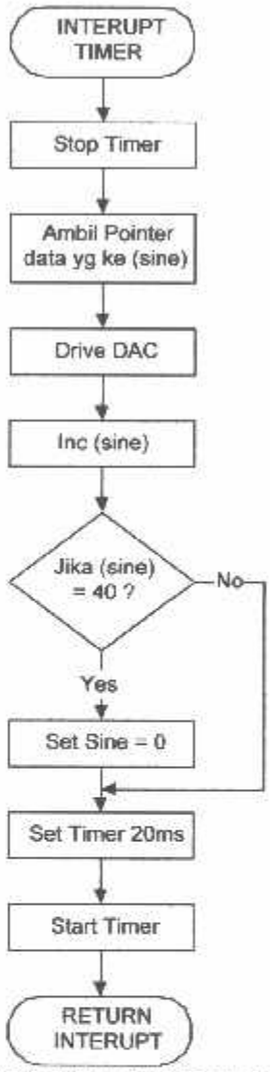



A
Hasil < 25 ?
Y
Ambil
Lookup Tabel 2
N
Hasil < 20 ?
Y
Ambil
Lookup Tabel 3
N
Hasil < 15 ?
Y
Ambil
Lookup Tabel 4
N
Hasil < 10 ?
N
Y
Ambil
Lookup Tabel 5
Hasil < 5 ?
Y
Ambil
Lookup Tabel 6
N
Ambil
Lookup Tabel 11
B


C
Kurangi Data ADC dg Data Volt-ADC
Hasil < 5 ?
Y
Ambil Lookup Tabel 6
N
Hasil < 10 ?
Y
Ambil Lookup Tabel 7
N
Hasil < 15 ?
Y
Ambil Lookup Tabel 8
N
Hasil < 20 ?
N
D
Y
Ambil Lookup Tabel 9



Gambar 3-9 *Flowchart* program utama



Gambar 3-10 *Flowchart* Data Loc up table

BAB IV

PENGUJIAN ALAT

Bab ini akan membahas pengujian alat yang telah dirancang, dirakit serta direalisasikan. Tujuan pengujian alat ini adalah mengetahui kerja dari masing-masing sistem yang dibuat secara per-blok. Dengan demikian dapat diketahui kepresisian kerja dari alat yang direncanakan dan dibuat. Secara umum tujuan dari pengujian alat tersebut adalah sebagai berikut :

1. Mengetahui proses kerja dari masing-masing rangkaian (blok).
2. Memudahkan pendataan spesifikasi alat.
3. Mengetahui hasil dari suatu perencanaan yang telah dibuat.
4. Memudahkan perawatan dan perbaikan apabila sewaktu-waktu terjadi kerusakan.

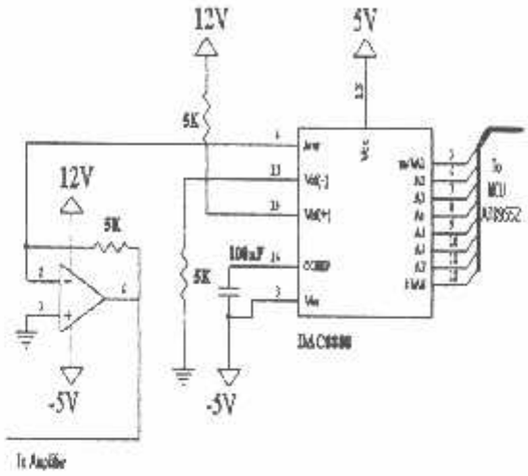
4.1. Pengujian Rangkaian DAC 0808

4.1.1. Tujuan

Pengujian rangkaian DAC (Digital Analog Converter) 0808 ini bertujuan untuk mengetahui bagaimana kondisi sinyal sinusoida pada saat dijalankan.

4.1.2. Langkah- Langkah Pengujian

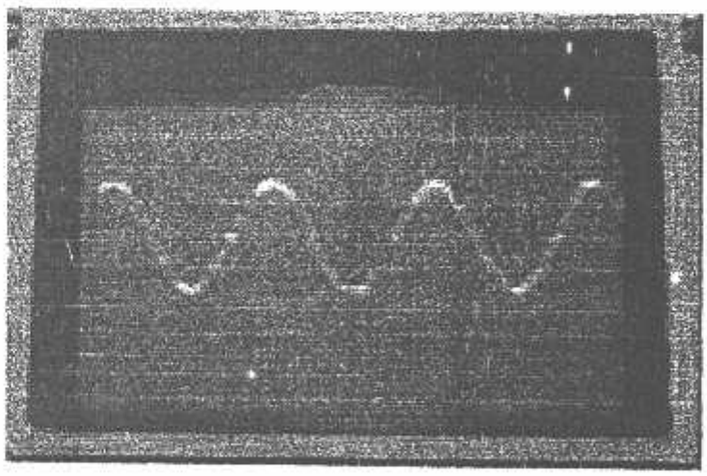
1. Menyusun rangkaian DAC 0808 seperti pada gambar 4-1.
2. Menghubungkan rangkaian DAC 0808 dengan tegangan Vcc (5V).
3. Mengamati hasil pengujian.



Gambar 4-1 Rangkaian DAC (Digital Analog Converter) 0808

4.1.3. Hasil dan Analis

Setelah melakukan pengujian DAC (Digital Analog Converter)0808 maka hasil yang diperoleh adalah sebagai berikut :



Gambar 4-2 hasil pengujian sinusoida pada rangkain DAC 0808

Pada pengujian DAC 0808 ini digunakan V_{Ref} = 12 V artinya jika semua inputan berlogika maka tegangannya 12 V dan apabila semua input berlogika 0 maka, tegangannya 0 V. Jadi untuk V_{Ref} = 12 V maka V_{max} = 12 V dan V_{min} = 0 V. IC DAC 0808 mendapat inputan 8 bit berarti terdapat 2^8 kombinasi = 256 kombinasi, schingga didapat :

Status maksimum = status maksimum – 1

= 256 – 1 – 255

perubahan tegangan output minimum = 12 / 255 = 0,047 V

input – 30 hek = 48 desimal : output analog = 48 * 0,047 = 2,256 Volt

No	Inputan Data Digital (Heksa Desimal)	Desimal	Output cData Analog (Volt)	
			Pengukuran (Volt)	Perhitungan (Volt)
1	00	0	1 mv	0
2	30	48	2,174	2,256
3	65	101	4,602	4,747
4	95	149	6,868	7,003
5	BB	187	8,632	8,789
6	FF	255	11,751	11,985

Tabel 4 – 1 Hasil perhitungan dan Pengukuran Konversi Digital to Analog

4.1.4. Analisa Data

Dari data yang ada pada hasil pengujian, maka output dari rangkaian DAC 0808 memiliki bentuk gelombang sinus dengan frekuensi 50Hz .

Tegangan analog yang dihasilkan DAC 0808 dengan menggunakan AT89S52 sebanding dengan input digitalnya. Error yang didapat 0,12%

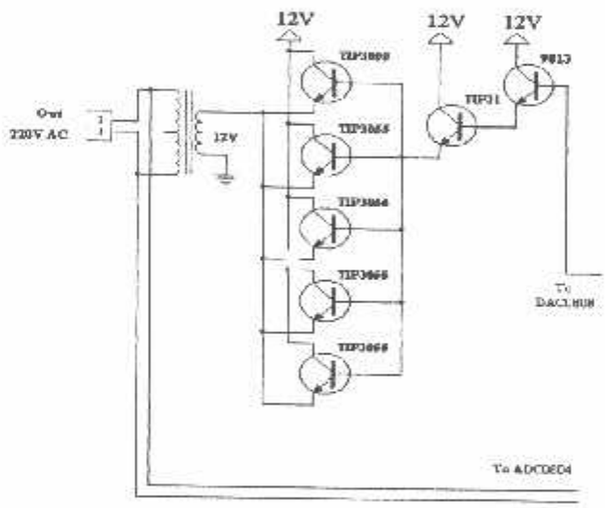
4.2. Pengujian rangkaian amplifier

4.2.1. Tujuan

Pengujian ini bertujuan untuk mengetahui apakah rangkaian amplifier yang digunakan berkerja dengan baik.

4.2.2. Langkah-Langkah Pengujian

1. Menyusun rangkaian amplifier seperti pada gambar 4-3
2. Menghubungkan rangkaian amplifier dengan tegangan Vcc (12V).
3. Mengamati hasil yang ditunjukan pada ampermeter.

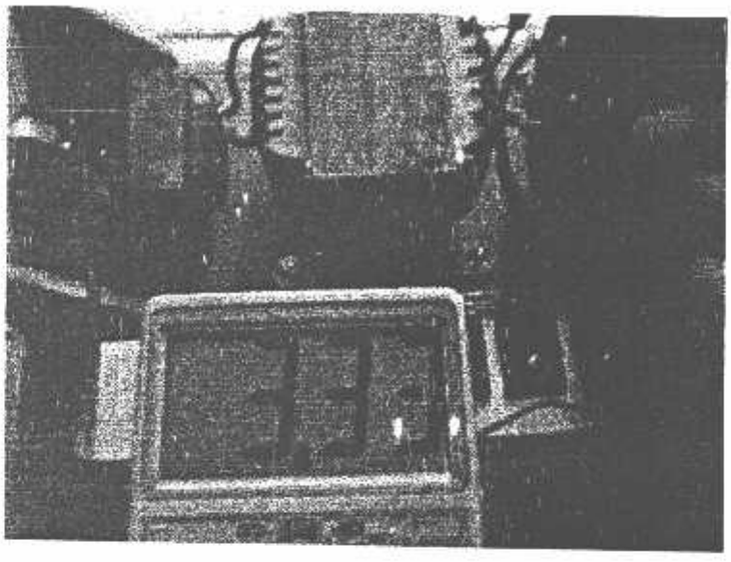


Gambar 4-3 Rangkaian Amplifier

4.2.3. Hasil dan Analisa

Setelah melakukan pengujian rangkaian amplifier maka hasil yang di perolch adalah sebagai berikut :

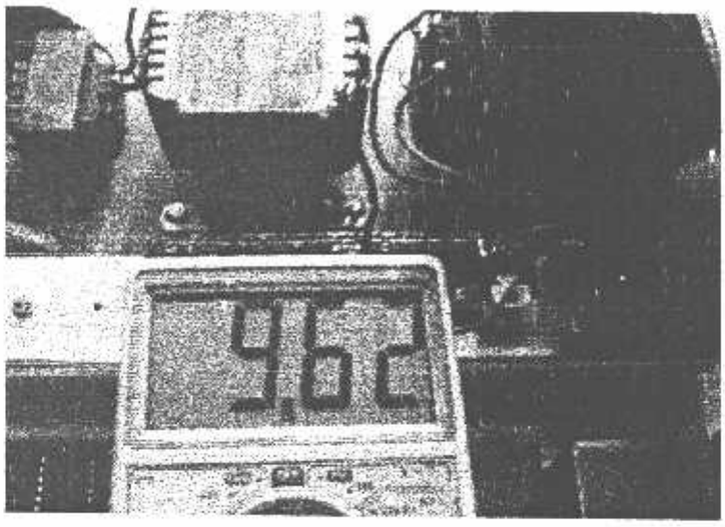
➢ Hasil dari pengukuran arus untuk rangkaian amplifier adalah sebagai berikut :



Gambar 4-4 Hasil Pengujian Arus Pada Rangkaian Amplifier

Dapat disimpulkan bahwa untuk mendrive transistor agar mencapai kondisi saturasi maka arus yang masuk kekaki basis harus sesuai, agar transistor tidak terlalu jenuh.

- Hasil dari pengukuran tegangan untuk rangkaian amplifier adalah sebagai berikut :



Gambar 4-5 Hasil Pengujian Tegangan Pada Rangkaian Amplifier

No	Arus (A)		Tegangan (V)	
	Pengukuran	Perhitungan	Pengukuran	Perhitungan
1	3,33	4,5	9,62	12

Tabel 4 – 2 Hasil Pengukuran dan Perhitungan Rangkaian amplifier

4.2.4. Analisa Data

Dari data yang ada pada hasil pengujian, maka output dari rangkaian amplifier memiliki arus sebesar 3,33 A dan Tegangan sebesar 9,62 Volt itu dikarenakan adanya V_{BE} = 0,7 Volt.

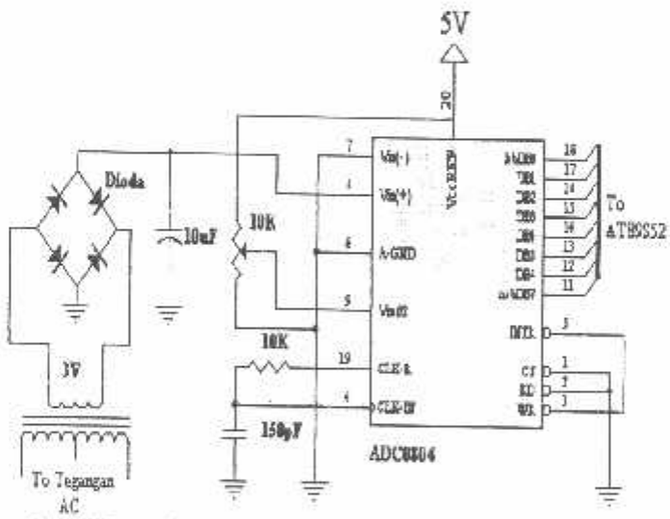
4.3. Pengujian Rangkaian Sensor Tegangan dan ADC 0804

4.3.1. Tujuan

Pengujian ini bertujuan untuk mengetahui kinerja perangkat keras secara keseluruhan apabila dijalankan.

4.3.2. Langkah-Langkah Pengujian

1. Menyusun rangkaian sensor tegangan dan ADC 0804 seperti pada gambar 4-6
2. Menghubungkan sensor tegangan dengan tegangan 220 V
3. Menghubungkan rangkaian ADC 0804 dengan tegangan 5 V
4. Mengamati hasil yang ditunjukan pada multimeter



Gambar 4 – 6 Rangkaian Sensor Tegangan Dan ADC 0804

4.3.3. Hasil dan Analisa

Setelah melakukan pengujian rangkaian sensor tegangan maka hasil yang di peroleh adalah sebagai berikut :

- Hasil pengukuran dan perhitungan rangkaian sensor tegangan didapat sebagai berikut :

No	Tegangan Input (Volt)	Tegangan Output (Volt)	
		pengukuran	perhitungan
1	90	2,3	2,6
2	110	2,9	3
3	220	4,7	5

Tabel 4 – 3 Hasil Pengukuran Rangkaian sensor Tegangan

- Hasil pengukuran dan perhitungan rangkaian ADC 0804 didapat sebagai berikut :

No	Input Data Analog (Volt)	Output Data Digital (Heksa Desimal)	
		Pengukuran	Perhitungan
1	0,00	00	00
2	1,22	3F	30
3	2,20	71	6E
4	3,50	B4	AF
5	4,10	D2	CD
6	4,64	EE	E8

Tabel 4 – 4 Hasil Pengukuran dan perhitungan Rangkaian ADC 0804

4.3.4. Analisa Data

Dari data yang ada pada hasil pengujian, maka output dari rangkaian sensor tegangan mempunyai error sebesar 2%

Dari data yang ada pada hasil pengujian rangkaian ADC 0804 didapat error yang angat kecil.

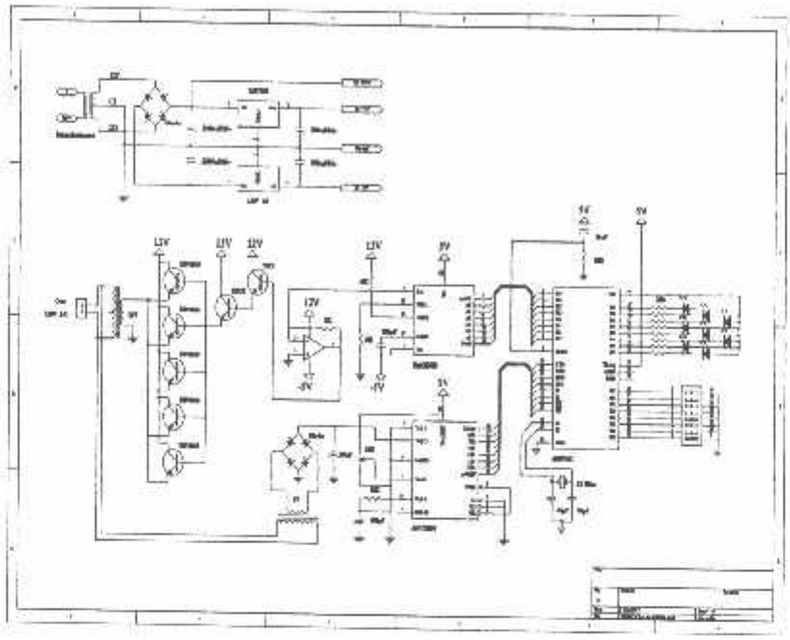
4.4. Pengujian Rangkaian keseluruan

4.4.1. Tujuan

Pengujian ini bertujuan untuk mengetahui kinerja perangkat keras secara keseluruhan apabila dijalankan.

4.4.2. Langkah-Langkah Pengujian

1. Menyusun rangkaian keseluruan seperti pada gambar 4-6
2. Menghubungkan rangkaian keseluruan dengan jala-jala listrik.
3. Menekan tombol start
4. Mengamati hasil yang ditunjukan pada multimeter digital.

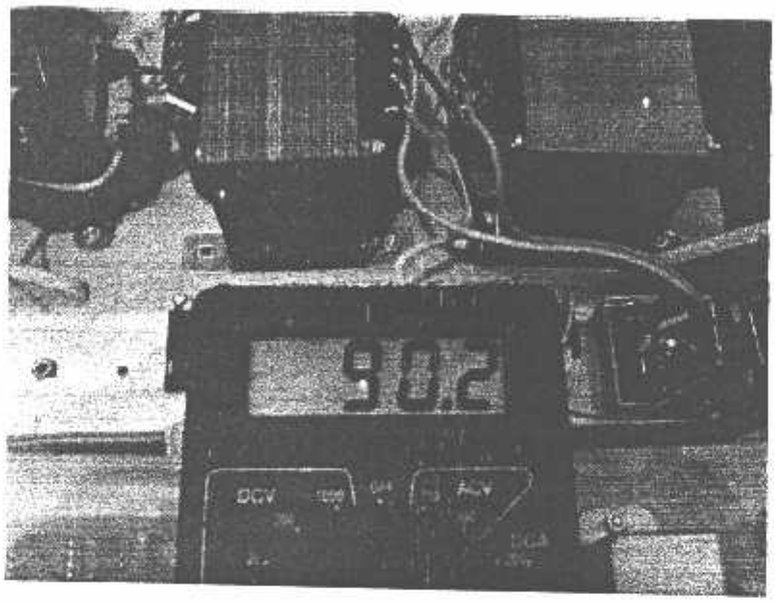


Gambar 4-6 Rangkaian Keseluruan

4.4.3. Hasil dan Analisa

Pengujian sistem secara keseluruhan dilakukan dengan menggabungkan semua blok rangkaian dan menjalankan perangkat lunak yang telah dibuat untuk menjalankan peralatan. Pengujian ini dimaksudkan untuk mengetahui kerja sistem keseluruhan.

- Hasil dari pengukuran tegangan tanpa beban untuk rangkaian keseluruan adalah sebagai berikut :



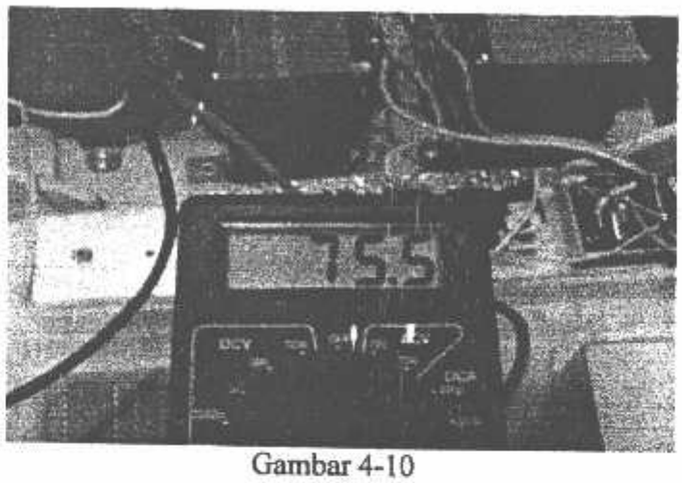
Gambar 4-7 Hasil Pengujian Tegangan tanpa beban Pada Rangkaian keseluruan

Dapat disimpulkan bahwa untuk tegangan keluaran dari rangkaian keseluruan hanya dihasilkan tegangan 90,2 Volt itu dikarenakan adanya drop tegangan pada transformator.

NO	Pengukuran	Perhitungan
1	90,2 Volt	220 Volt

Table 4-5 Hasil Dari Pengukuran Rangkaian Keseluruan

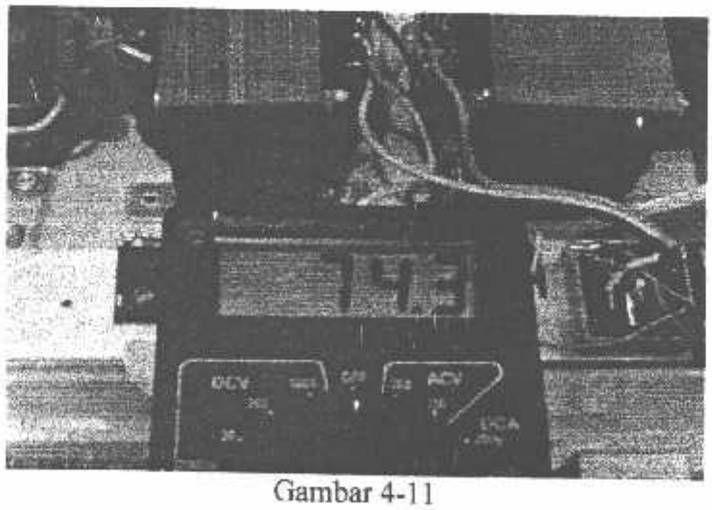
- Hasil dari pengukuran tegangan berbeban 15 watt untuk rangkaian keseluruan adalah sebagai berikut :



Gambar 4-10

Hasil Pengujian Tegangan berbeban 15 watt Pada Rangkaian keseluruan

- Hasil dari pengukuran tegangan berbeban 25 watt untuk rangkaian keseluruan adalah sebagai berikut :



Gambar 4-11

Hasil Pengujian Tegangan berbeban 15 watt Pada Rangkaian keseluruan

Dapat disimpulkan bahwa untuk tegangan keluaran berbeban dari rangkaian keseluruan dapat dilihat ditabel dibawah ini :

NO	BEBAN	TEGANGAN (Volt)
1	5 watt	79,4
2	10 watt	77,6
3	15 watt	75,5
4	25 watt	74,3

Table 4-6 Hasil Dari Pengukuran Rangkaian Keseluruan Berbeban

4.4.4. Analisa Data

Setelah dilakukan beberapa kali pengujian maka hasil percobaan tidak sesuai dengan yang di harapkan dikarenakan tegangan yang keluar tidak maksimal karena adanya rugi tegangan yang terdapat pada transformator yang mempunyai eror sekitar 51% dikarenakan tegangan yang di hasilkan 90 Volt

BAB V

PENUTUP

5.1 Kesimpulan

Dari pengamatan dan analisa selama proses perancangan dan pembuatan alat dapat diambil beberapa kesimpulan sebagai berikut :

1. Dalam merancang dan membuat sinyal sinusoida dapat menggunakan rangkaian DAC 0808 dimana sinyal keluarannya berupa sinyal sinus.
2. Dalam merancang rangkaian amplifier kita dapat menggunakan rangkaian volted follower.
3. Tegangan yang keluar pada pengujian 90 volt AC
4. Tegangan yang keluar dari transformator tidak maksimal dikarenakan adanya rugi tegangan yang terdapat pada transformator.
5. Daya maksimum 40 watt
6. Arus yang keluar dari rangkaian amplifier 3,33 A

5.2 Saran- saran

Ada beberapa hal yang perlu diperhatikan dalam pengembangan alat ini, antara lain :

1. Agar alat ini dapat bekerja dengan baik, diharapkan untuk mengikuti petunjuk pengoperasian alat dengan benar
2. Dalam mengembangkan alat ini lebih lanjut bisa ditambahkan LCD dan keypad dimana nantinya dapat mengetahui tegangan yang dihasilkan.

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www.DataSheetCatalog.com

LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL
JL. Bendungan Sigura-gura No. 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : SAIFUL FANANI
Nim : 0017156
Masa Bimbingan : 25 DESEMBER 2007 s/d 25 JUNI 2008
Judul Skripsi : Perencanaan dan Pembuatan Inverter Berbasis Mikrokontroler AT89S52 Dengan Menggunakan Algoritma DDS (*Direct Digital Systensis*)

No	Tanggal	Uraian	Paraf Pembimbing
1	4/12 2008	Bab I, II tolong dipertajam	
2	11/12 2008	Bab I, II Oke	
3	12/12 2008	Bab III perbaiki flowchart	
4	18/12 2008	Bab III	
5	8/1 08	Bab IV	
6	14/1 08	tac allin	
7			
8			
9			
10			

Malang, - - 2008
Dosen Pembimbing I

Ir.F. Yudi Limpraptono,MT
NIP: P.1039500274

From S-4a

NSTITUT TEKNOLOGI NASIONAL
JL. Bendungan Sigura-gura No. 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : SAIFUL FANANI
Nim : 0017156
Masa Bimbingan : 25 DESEMBER 2007 s/d 25 JUNI 2008
Judul Skripsi : Perencanaan dan Pembuatan Inverter Berbasis Mikrokontroler AT89S52 Dengan Menggunakan Algoritma DDS (*Direct Digital Synthesis*)

No	Tanggal	Uraian	Paraf Pembimbing
1	5/2 '08	BAB I, II, III. tolong perbaiki BAB I, II, III.	
2	12/2 '08	Acc BAB I, II, III. Bimbingan BAB IV & V.	
3	14/2 '08	Acc. BAB IV & V.	
4	16/2 '08	Bimbingan Untuk Seminar Hasil.	
5	17/2 '08	Acc Seminar hasil	
6	4/3 '08	Acc ujian sekripsi	
7			
8			
9			
10			

Malang, 4 MAR 2008
Dosen Pembimbing II

Ir.M. Abdul Hamid, MT
NIP. Y. 1018800188

From S-4a

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Syaiful Fauzani
N I M : 08.17.156.
Perbaikan meliputi :

1. Buat diagram blok. Dr rangkaian ada, disesuaikan dg implementasi alat. Yg akan buat.
2. Lengkapi diagram blok yg ada buat :
   a. Letak signal di masing² titik
   b. Besaran input arus & tegangan

Malang,

(____________________)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Jenjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : SAIFUL ANAM
NIM : 0017152
Perbaikan meliputi :

2) CARI CARA PENGUJIAN LAGI, DIBUAT LEBIH LENGKAP

Malang,

(_____)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
Jl. Karanglo KM. 2 Malang

FORMULIR PERBAIKAN SKRIPSI

Dalam pelaksanaan Ujian Skripsi Jenjang Strata Satu (S-1) Jurusan Teknik Elektro Konsentrasi Teknik Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

Nama	: Saiful Fanani
NIM	: 00 17 156
Jurusan	: Teknik Elektro S-1
Konsentrasi	: Teknik Elektronika
Masa Bimbingan	: 25 Desember 2007 s/d 25 Juni 2008
Judul Skripsi	: Perecanaan dan Pembuatan Inverter Berbasis Mikrokontroler AT89S52 Dengan Menggunakan Algoritma DDS *(Direct Digital Synthesis)*

Penguji/Tanggal	Uraian	Paraf
Penguji I 17 Maret 2008	Buat diagram blok dari rangkaian disesuaikan dengan implementasi alat yang dibuat	
	Lengkapi diagram blok : ➢ Bentuk signal di masing-masing titik ➢ Keluaran atau inputan arus dan tegangan	
Penguji II 17 Maret 2008	Pengujian dibuat lebih lengkap	

Mengetahui,

Dosen Pembimbing I

(Ir. F. Yudi Limpraptono, MT.)
NIP.Y. 1039500274

Dosen Pembimbing II

(Ir. M. Abdul Hamid, MT.)
NIP.Y. 1018800188

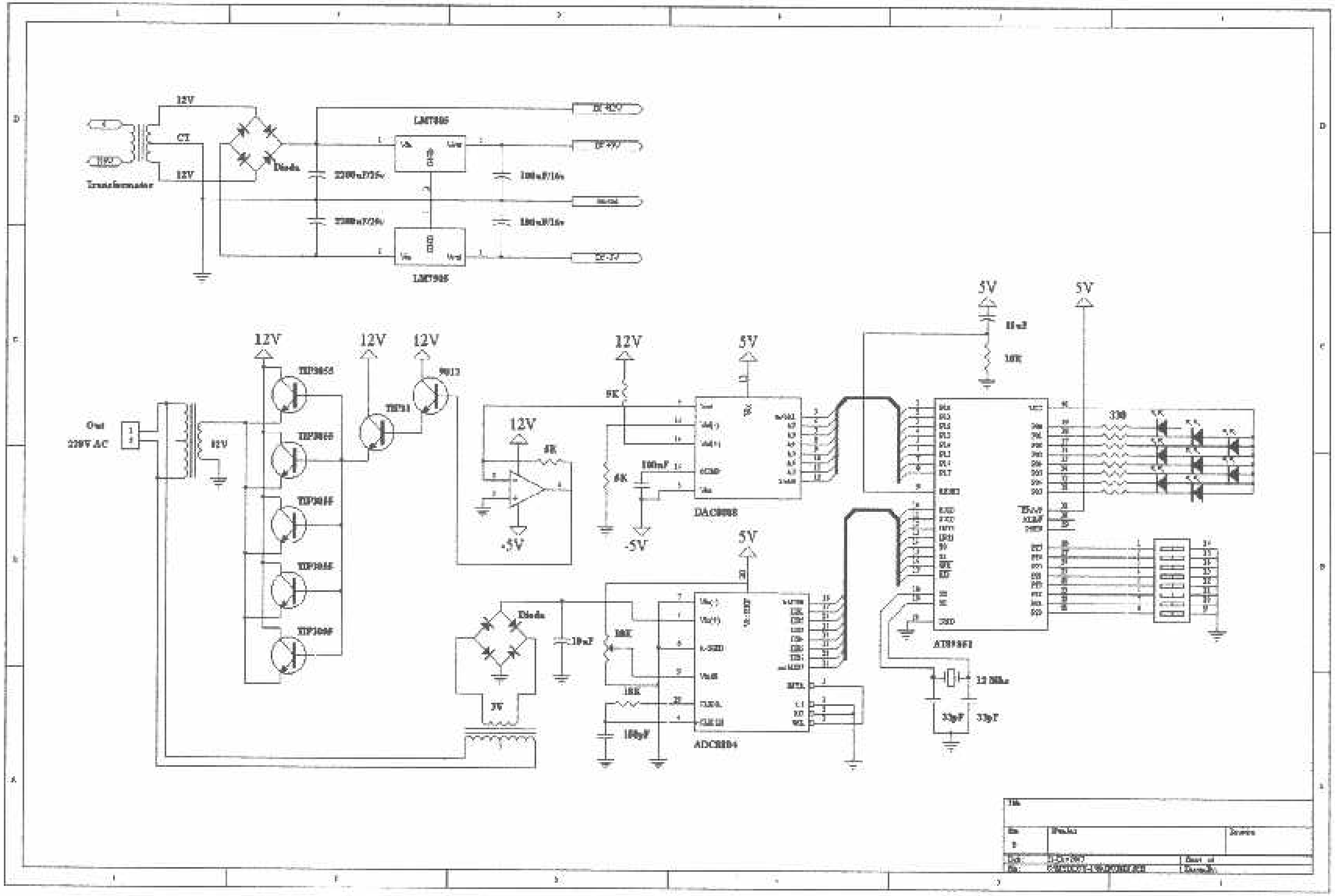
Dosen Penguji,

Penguji I

(Dr. Cahyo Crysdian, MSc.)
NIP.Y. 1030400412

Penguji II

(Joseph Dedy Irawan, ST, MT.)
NIP.Y. 132315178



Transformator
12V
CT
12V
Diode
LM7805
LM7905
2200uF/25v
100uF/16v
12V
12V
12V
TIP3055
TIP3055
TIP3055
TIP3055
TIP3055
TIP31
9013
Out
220V AC
12V
3V
Diode
10uF
10K
10K
100pF
ADC0804
12V
8K
8K
-5V
100nF
-5V
9K
DAC0808
5V
5V
5V
5V
10uF
10K
330
AT89S51
12 Mhz
33pF
33pF

```
        org     00h
        ljmp    init
;
        org     0Bh                 ; interupt timer1 overflow
        ljmp    graph
;
        Sine    Equ 30h
        Dvlt    Equ 31h
        Dslh    Equ 32h
        Dly0    Equ 33h
        Dly1    Equ 34h
        Dly2    Equ 35h
;
init:   lcall   tmr_in
        mov     Sine,#0
        mov     A,P2
manual: cjne    A,#01111111b,manu01
        mov     DPTR,#lokup0
sine00: ljmp    sine00
;
manu01: cjne    A,#01111110b,manu02
        mov     DPTR,#lokup1
sine01: ljmp    sine01
;
manu02: cjne    A,#01111101b,manu03
        mov     DPTR,#lokup2
sine02: ljmp    sine02
;
manu03: cjne    A,#01111100b,manu04
        mov     DPTR,#lokup3
sine03: ljmp    sine03
;
manu04: cjne    A,#01111011b,manu05
        mov     DPTR,#lokup4
sine04: ljmp    sine04
;
manu05: cjne    A,#01111010b,manu06
        mov     DPTR,#lokup5
sine05: ljmp    sine05
;
manu06: cjne    A,#01111001b,manu07
        mov     DPTR,#lokup6
sine06: ljmp    sine06
;
manu07: cjne    A,#01111000b,manu08
        mov     DPTR,#lokup7
sine07: ljmp    sine07
;
manu08: cjne    A,#01110111b,manu09
        mov     DPTR,#lokup8
sine08: ljmp    sine08
;
manu09: cjne    A,#01110110b,manu10
        mov     DPTR,#lokup9
sine09: ljmp    sine09
;
manu10: cjne    A,#01110101b,manu11
        mov     DPTR,#lokupA
```

```
sine10: ljmp    sine10
;
manu11: cjne    A,#01110100b,otmtis
        mov     DPTR,#lokupB
sine11: ljmp    sine11
;
otmtis: mov     Dvlt,#30          ; set data volt-adc 30
;
mulai:  clr     A
        mov     A,P3
        mov     B,Dvlt
        div     AB
        cjne    A,#0,turn
        ljmp    naik
turn:   ljmp    turun
;
naik:   mov     A,Dvlt
        mov     B,P3
        subb    A,B
        mov     Dslh,A
naik00: mov     A,Dslh
        mov     B,#30
        div     AB
        cjne    A,#0,naik01
        mov     DPTR,#lokup1
        ljmp    ulang
naik01: mov     A,Dslh
        mov     B,#25
        div     AB
        cjne    A,#0,naik02
        mov     DPTR,#lokup2
        ljmp    ulang
naik02: mov     A,Dslh
        mov     B,#20
        div     AB
        cjne    A,#0,naik03
        mov     DPTR,#lokup3
        ljmp    ulang
naik03: mov     A,Dslh
        mov     B,#15
        div     AB
        cjne    A,#0,naik04
        mov     DPTR,#lokup4
        ljmp    ulang
naik04: mov     A,Dslh
        mov     B,#10
        div     AB
        cjne    A,#0,naik05
        mov     DPTR,#lokup5
        ljmp    ulang
naik05: mov     A,Dslh
        mov     B,#5
        div     AB
        cjne    A,#0,naik06
        mov     DPTR,#lokup6
        ljmp    ulang
naik06: mov     DPTR,#lokupB
;
```

```
turun:  mov     A,P3
        mov     B,Dvlt
        subb    A,B
        mov     Dslh,A
turn00: mov     A,Dslh
        mov     B,#5
        div     AB
        cjne    A,#0,turn01
        mov     DPTR,#lokup6
        ljmp    ulang
turn01: mov     A,Dslh
        mov     B,#10
        div     AB
        cjne    A,#0,turn02
        mov     DPTR,#lokup7
        ljmp    ulang
turn02: mov     A,Dslh
        mov     B,#15
        div     AB
        cjne    A,#0,turn03
        mov     DPTR,#lokup8
        ljmp    ulang
turn03: mov     A,Dslh
        mov     B,#20
        div     AB
        cjne    A,#0,turn04
        mov     DPTR,#lokup9
        ljmp    ulang
turn04: mov     A,Dslh
        mov     B,#25
        div     AB
        cjne    A,#0,turn05
        mov     DPTR,#lokupA
        ljmp    ulang
turn05: mov     A,Dslh
        mov     B,#30
        div     AB
        cjne    A,#0,turn06
        mov     DPTR,#lokupB
        ljmp    ulang
turn06: mov     DPTR,#lokupB
;
ulang:  ljmp    mulai
;
tmr_in: lcall   delays
        mov     TMOD,#01h           ; timer0 mode counter, timer1 mode 16
bit
        mov     TL0,#000h           ; reset timer 0 high
        mov     TH0,#000h           ; reset timer 0 low
        setb    EA                  ; enable acknowledge
        setb    ET0                 ; enable interupt timer 0 overflow
        clr     TF0                 ; matikan flag timer0
        setb    TR0
        lcall   delays
        ret
;
graph:  mov     A,Sine
        movc    A,@A+DPTR
```

```
        mov     P1,A
        inc     Sine
        mov     A,Sine
        cjne    A,#40,graph0
        mov     Sine,#0
        mov     A,P3
        cpl     A
        mov     P0,A
graph0: clr     TR0
        mov     TL0,#00Ch           ; set timer 0 high
        mov     TH0,#0FEh           ; set timer 0 low
        clr     TF0                 ; matikan flag timer0
        setb    TR0
        reti
;
jeda:   djnz    Dly0,jeda
        ret
;
delays: lcall   jeda
        djnz    Dly1,delays
        ret
;
delay1: mov     Dly2,#5
dly1:   lcall   delays
        djnz    Dly2,dly1
        ret
;
lokup0: DB      000,001,003,006,011,017,026,036,051,072         ; 000-009
        DB      128,183,204,219,230,238,244,249,252,254         ; 010-019
        DB      255,254,252,249,244,238,230,219,204,183         ; 020-029
        DB      128,072,051,036,026,017,011,006,003,001         ; 030-039
;
lokup1: DB      000,001,002,005,009,015,023,032,045,063         ; 000-009
        DB      113,162,180,193,203,210,216,220,223,224         ; 010-019
        DB      225,224,223,220,216,210,203,193,180,162         ; 020-029
        DB      113,063,045,032,023,015,009,005,002,001         ; 030-039
;
lokup2: DB      000,001,002,005,008,013,020,029,040,056         ; 000-009
        DB      100,144,160,171,180,187,192,195,198,199         ; 010-019
        DB      200,199,198,195,192,187,180,171,160,144         ; 020-029
        DB      100,056,040,029,020,013,008,005,002,001         ; 030-039
;
lokup3: DB      000,000,002,004,008,012,018,026,036,051         ; 000-009
        DB      090,129,144,154,162,168,172,176,178,180         ; 010-019
        DB      180,180,178,176,172,168,162,154,144,129         ; 020-029
        DB      090,051,036,026,018,012,008,004,002,000         ; 030-039
;
lokup4: DB      000,000,002,004,007,011,016,023,032,045         ; 000-009
        DB      080,115,128,137,144,149,153,156,158,160         ; 010-019
        DB      160,160,158,156,153,149,144,137,128,115         ; 020-029
        DB      080,045,032,023,016,011,007,004,002,000         ; 030-039
;
lokup5: DB      000,000,001,003,006,009,014,020,028,039
        DB      070,101,112,120,126,131,134,137,139,140
        DB      140,140,139,137,134,131,126,120,110,101
        DB      070,039,028,020,014,009,006,003,001,000
;
lokup6: DB      000,000,001,003,005,008,012,017,024,034
```

```
        DB      060,086,098,103,108,112,115,117,119,120
        DB      120,120,119,117,115,112,108,103,098,086
        DB      060,034,024,017,012,008,005,003,001,000
;
lokup7: DB      000,000,001,002,004,007,010,014,020,028
        DB      050,072,080,086,090,093,096,098,099,100
        DB      100,100,099,098,096,093,090,086,080,072
        DB      050,028,020,014,010,007,004,002,001,000
;
lokup8: DB      000,000,001,002,003,005,008,011,016,023
        DB      040,057,064,069,072,075,077,078,079,080
        DB      080,080,079,078,077,075,072,069,064,057
        DB      040,023,016,011,008,005,003,002,001,000
;
lokup9: DB      000,000,001,001,003,004,006,009,012,017
        DB      030,043,048,051,054,056,057,059,059,060
        DB      060,060,059,059,057,056,054,051,048,043
        DB      030,017,012,009,006,004,003,001,001,000
;
lokupA: DB      000,000,000,001,002,003,004,006,008,011
        DB      020,029,032,034,036,037,038,039,040,040
        DB      040,040,040,039,038,037,036,034,032,029
        DB      020,011,008,006,004,003,002,001,000,000
;
lokupB: DB      000,000,000,000,001,001,002,003,004,006
        DB      010,014,016,017,018,019,019,020,020,020
        DB      020,020,020,020,019,019,018,017,016,014
        DB      010,006,004,003,002,001,001,000,000,000
;
        end
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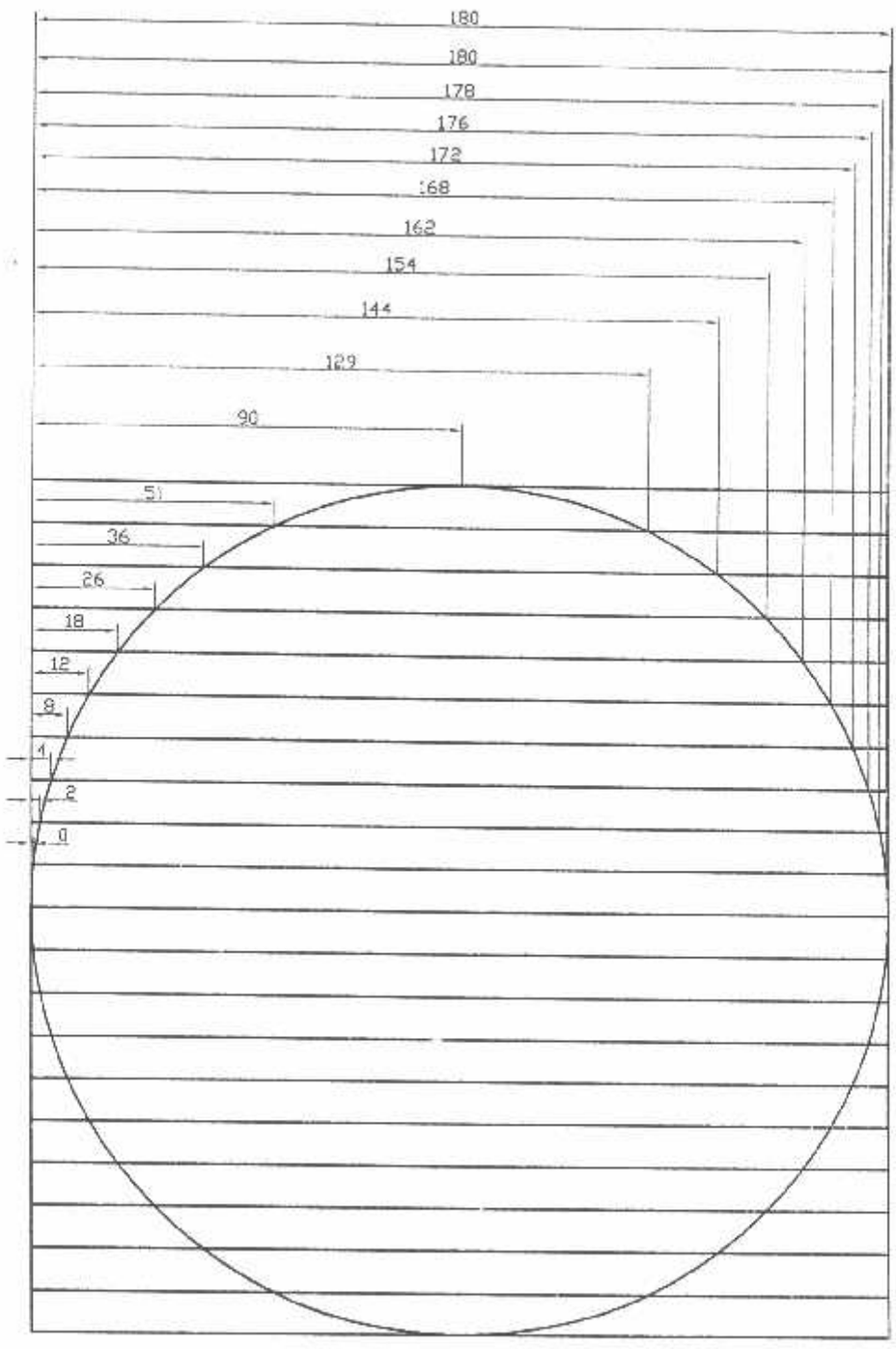
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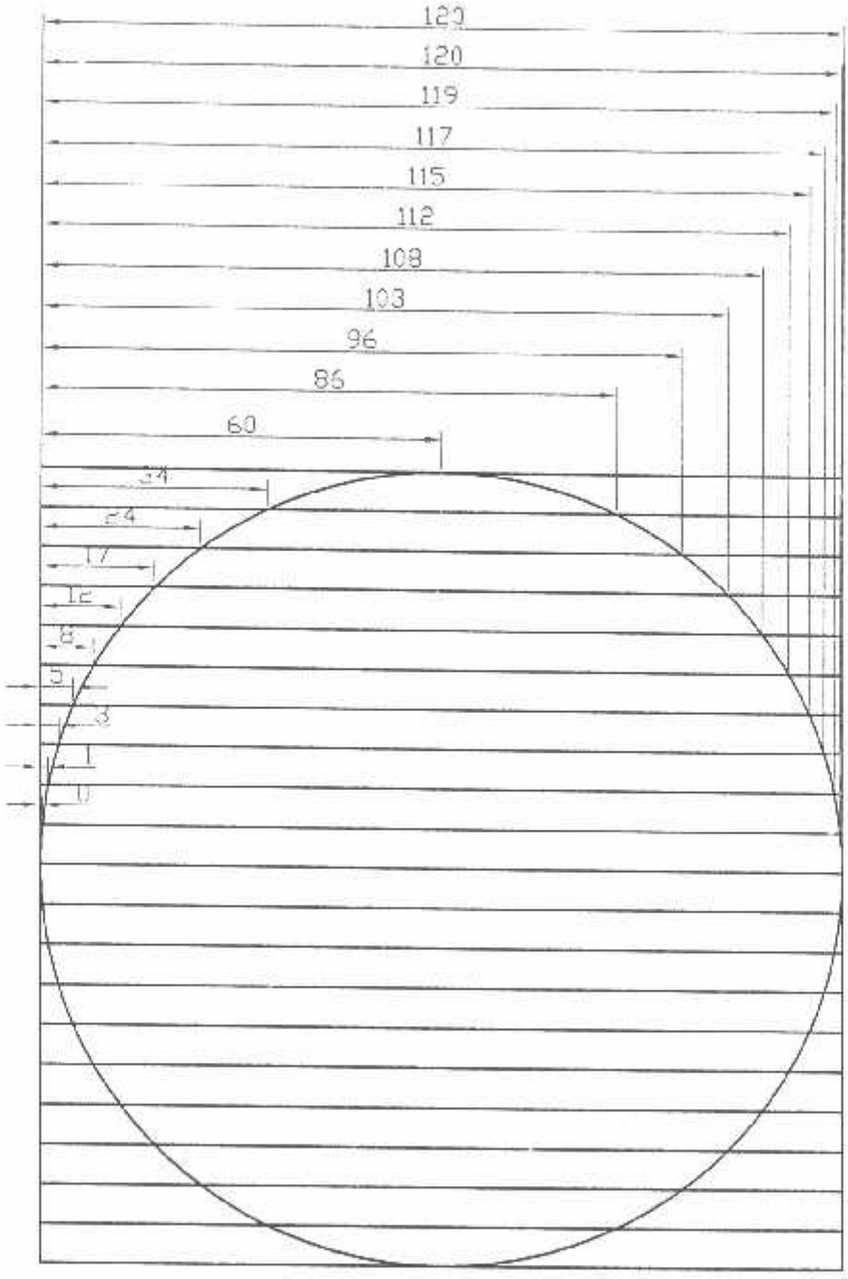
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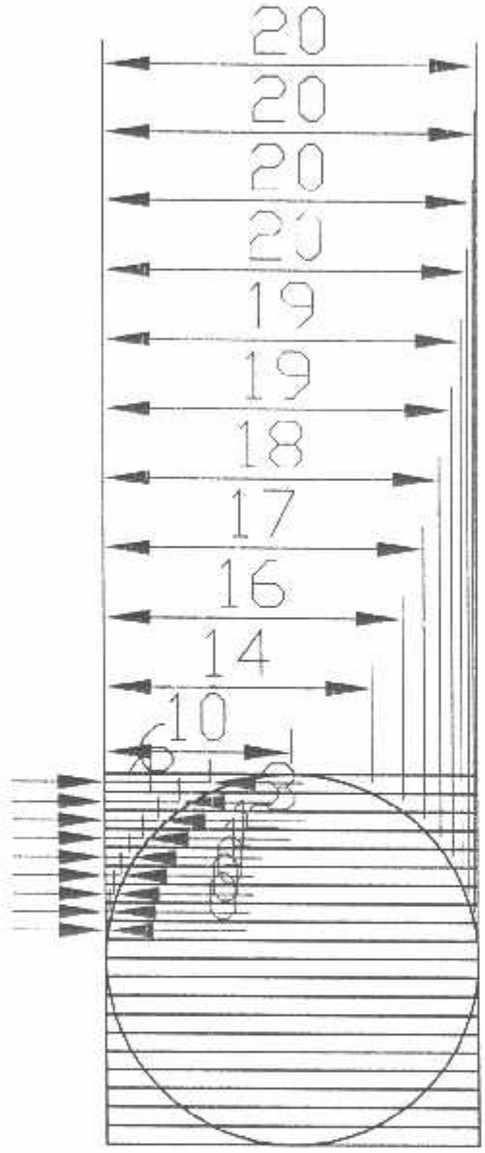
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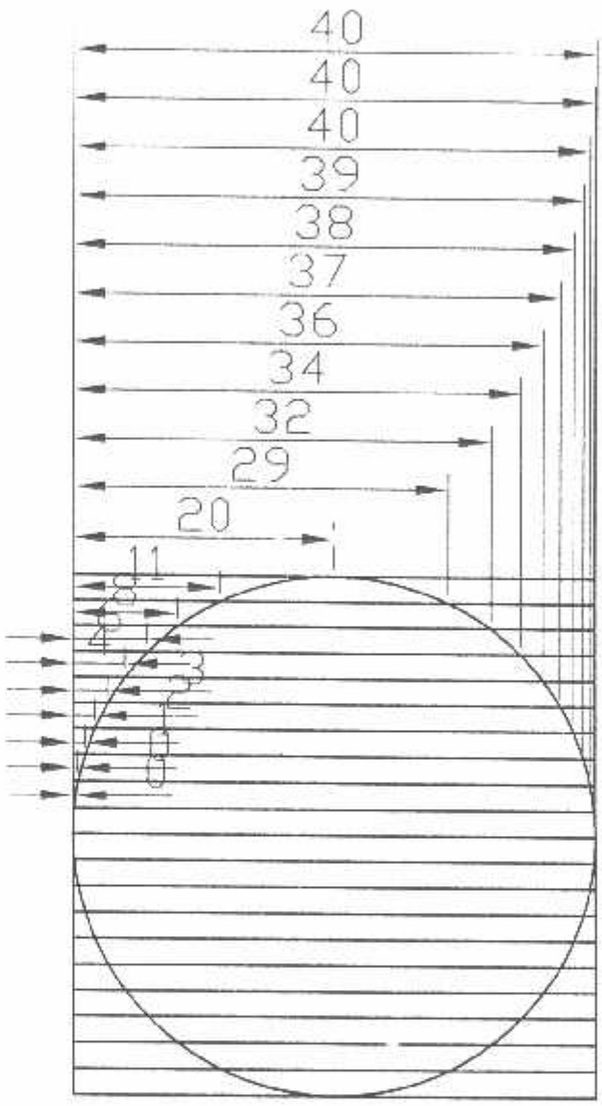
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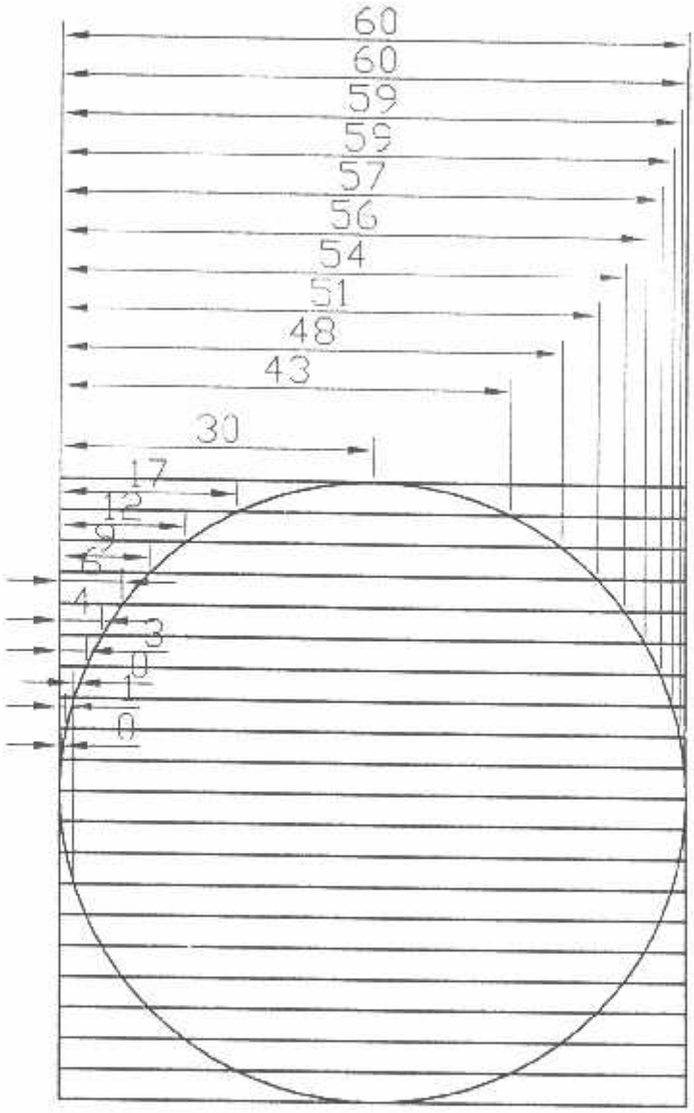
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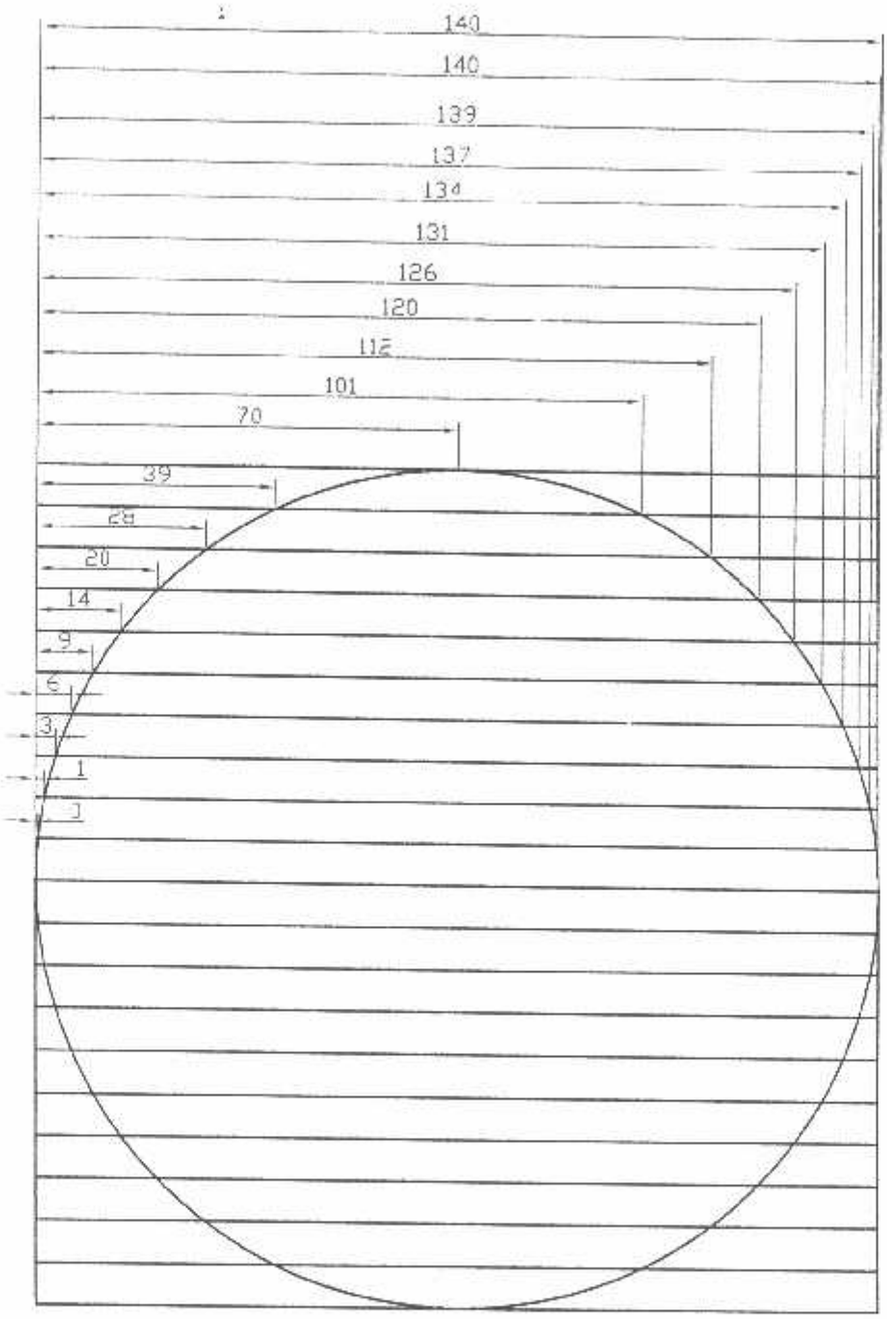
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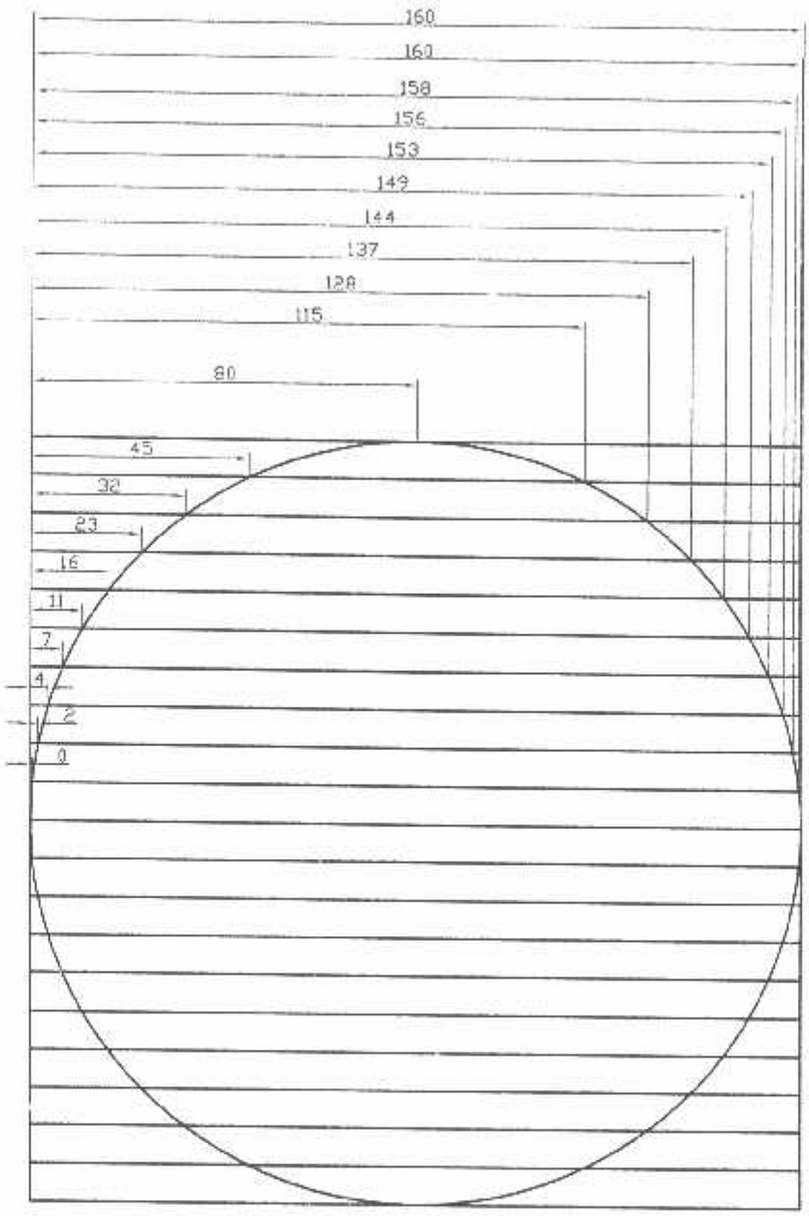
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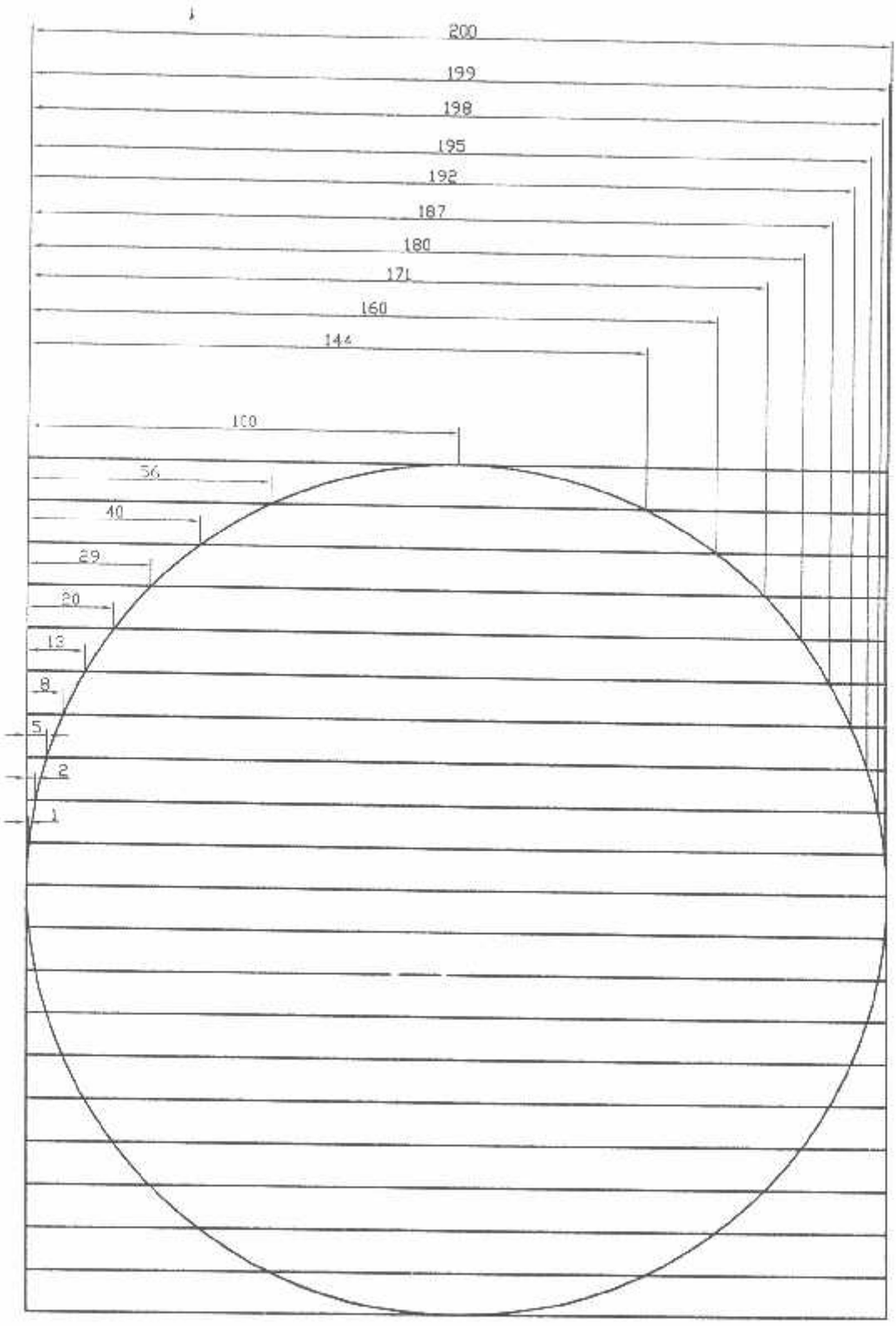
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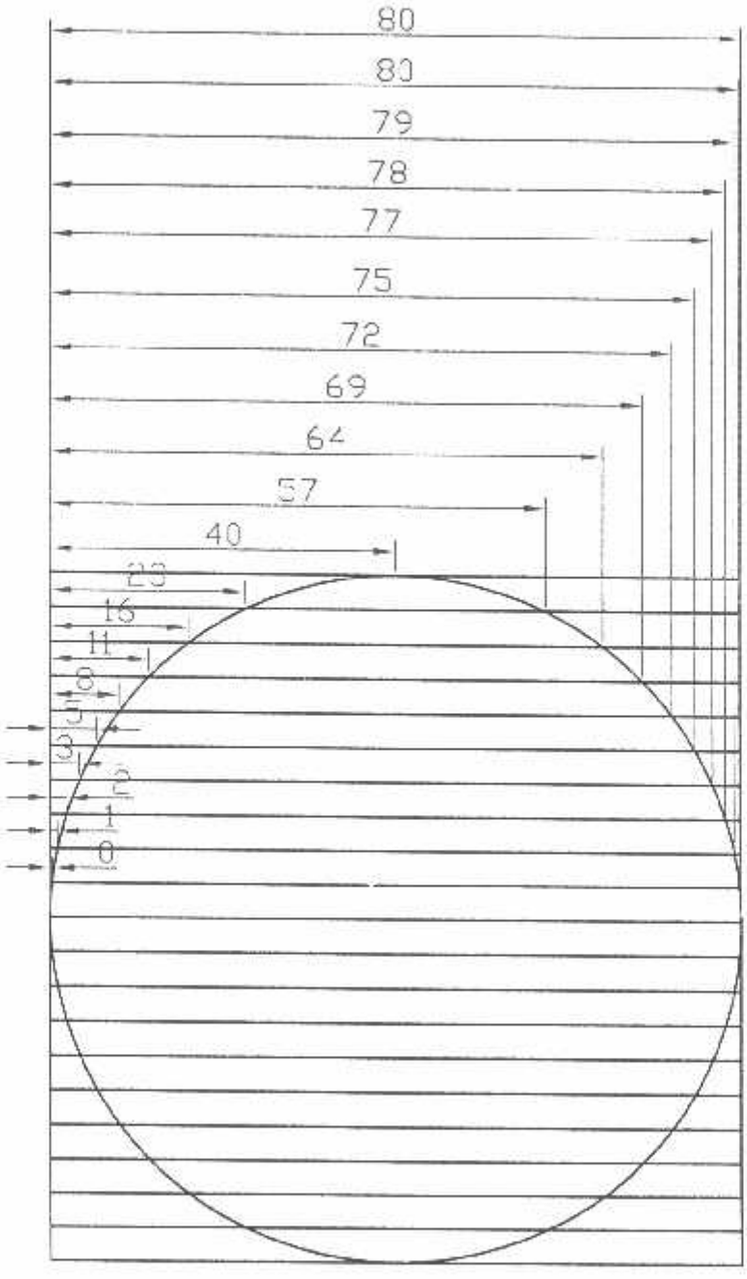
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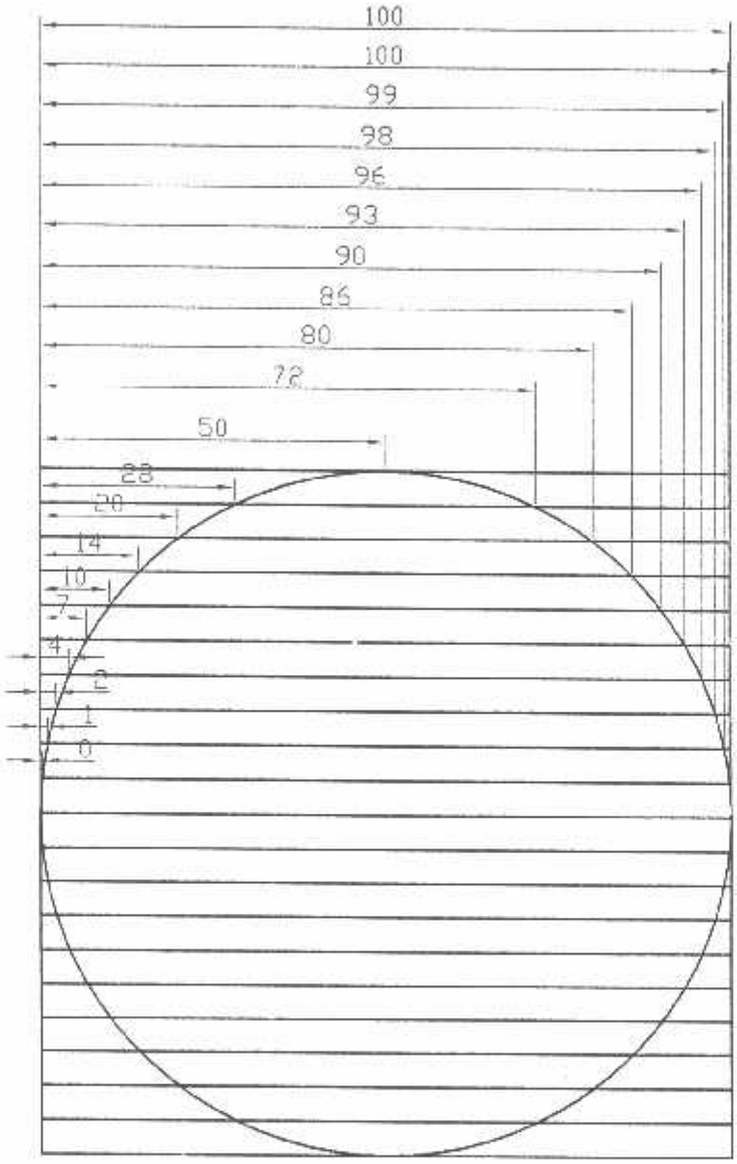
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Features

- Compatible with MCS-51® Products
- 8K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)

Description

The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

8-bit Microcontroller with 8K Bytes In-System Programmable Flash

AT89S52

1919B–MICRO–11/03

Pin Configurations

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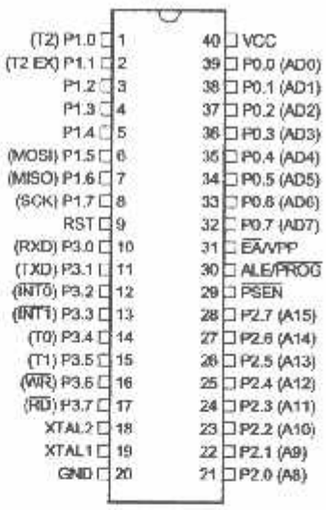

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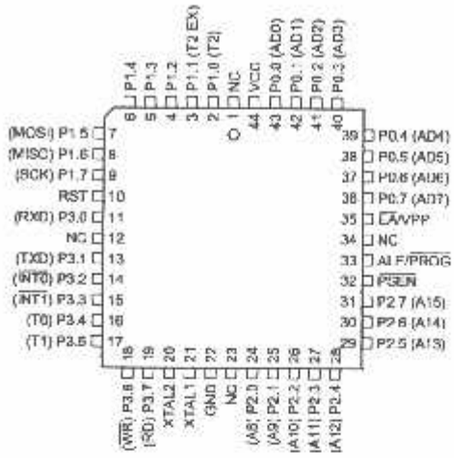

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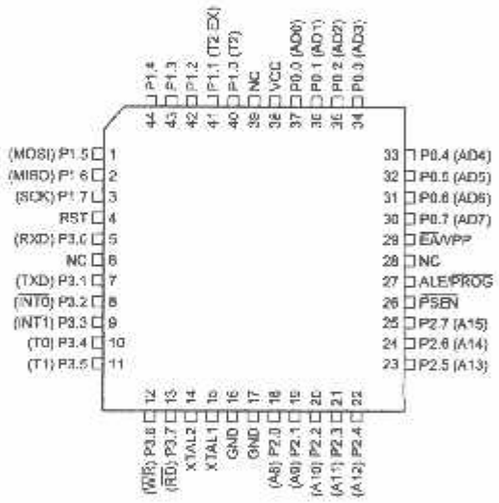

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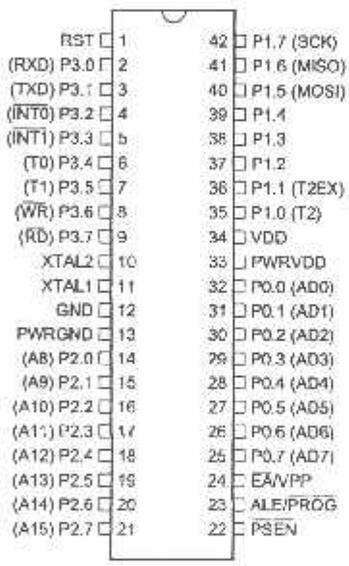
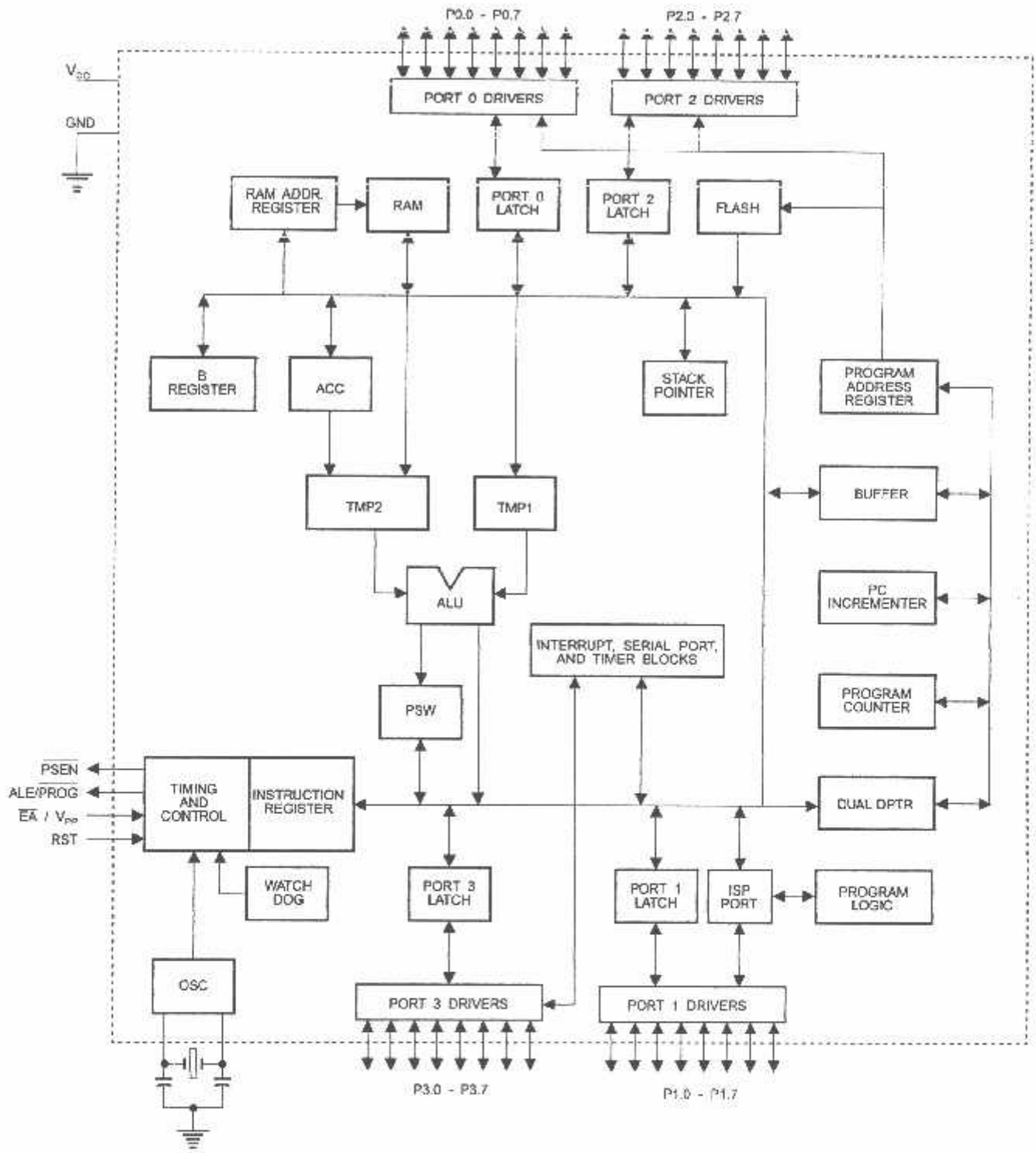


Block Diagram



Pin Description

VCC Supply voltage.

GND Ground.

Port 0 Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

Port 1 Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2 Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3 Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives high for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S52 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 6) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 1. AT89S52 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

Table 2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/T2	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 3. AUXR: Auxiliary Register

AUXR — Address = 8EH — Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE	Operating Mode
0	ALE is emitted at a constant rate of 1/6 the oscillator frequency
1	ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO	
0	Reset pin is driven High after WDT times out
1	Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 4. AUXR1: Auxiliary Register 1

AUXR1 — Address = A2H — Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S52, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are to external memory.

Data Memory

The AT89S52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S52 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S52 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S52 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select "Products", then "8051-Architecture Flash Microcontroller", then "Product Overview".

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S52 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers" operation, refer to the ATMEL Web site (http://www.atmel.com). From the home page, select "Products", then "8051-Architecture Flash Microcontroller", then "Product Overview".

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 5. Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Table 5. Timer 2 Operating Modes

RCLK +TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 6). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 1. Timer in Capture Mode

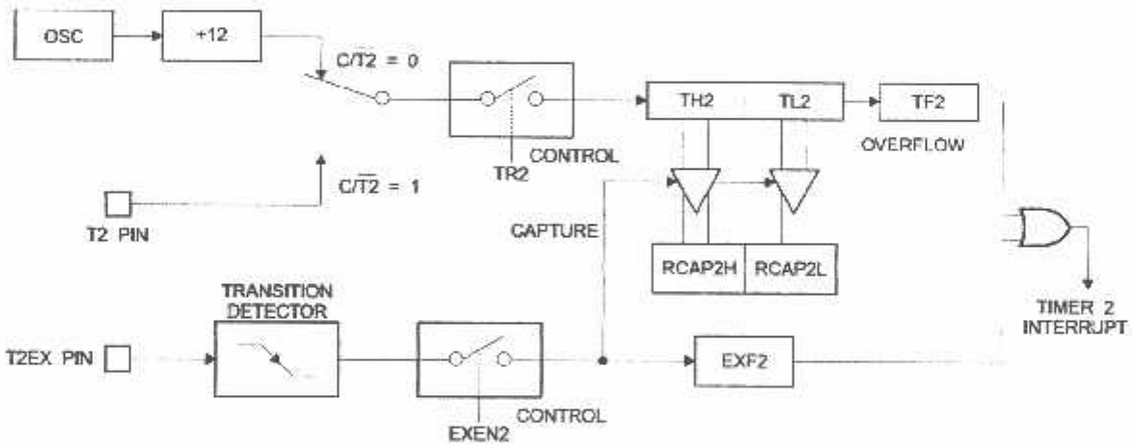


Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in Timer in Capture ModeRCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 2. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 2. Timer 2 Auto Reload Mode (DCEN = 0)

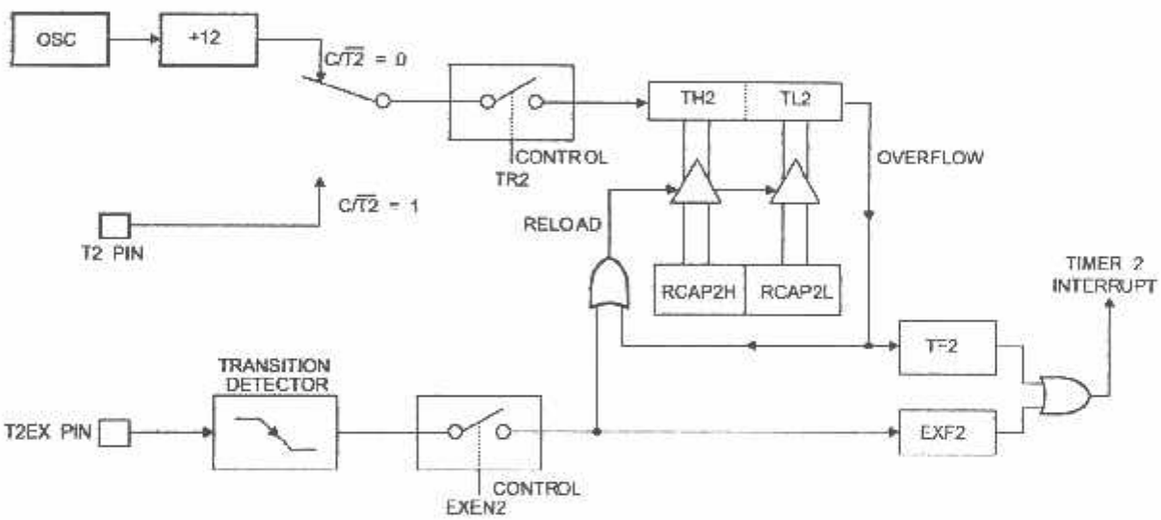


Table 6. T2MOD – Timer 2 Mode Control Register

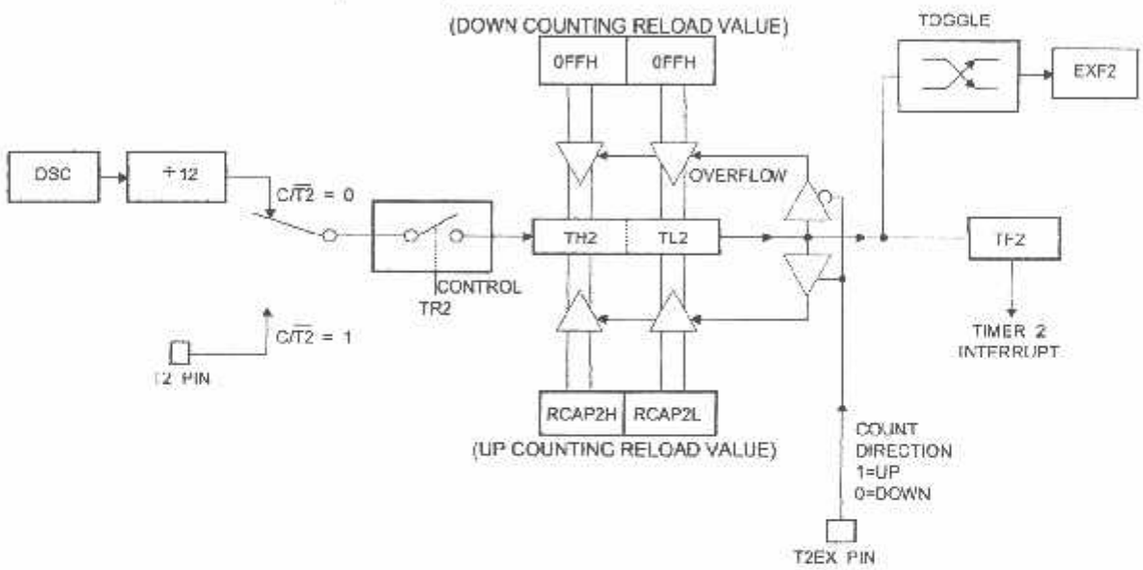
T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	T2OE	DCEN

Symbol	Function
–	Not implemented, reserved for future
T2OE	Timer 2 Output Enable bit
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

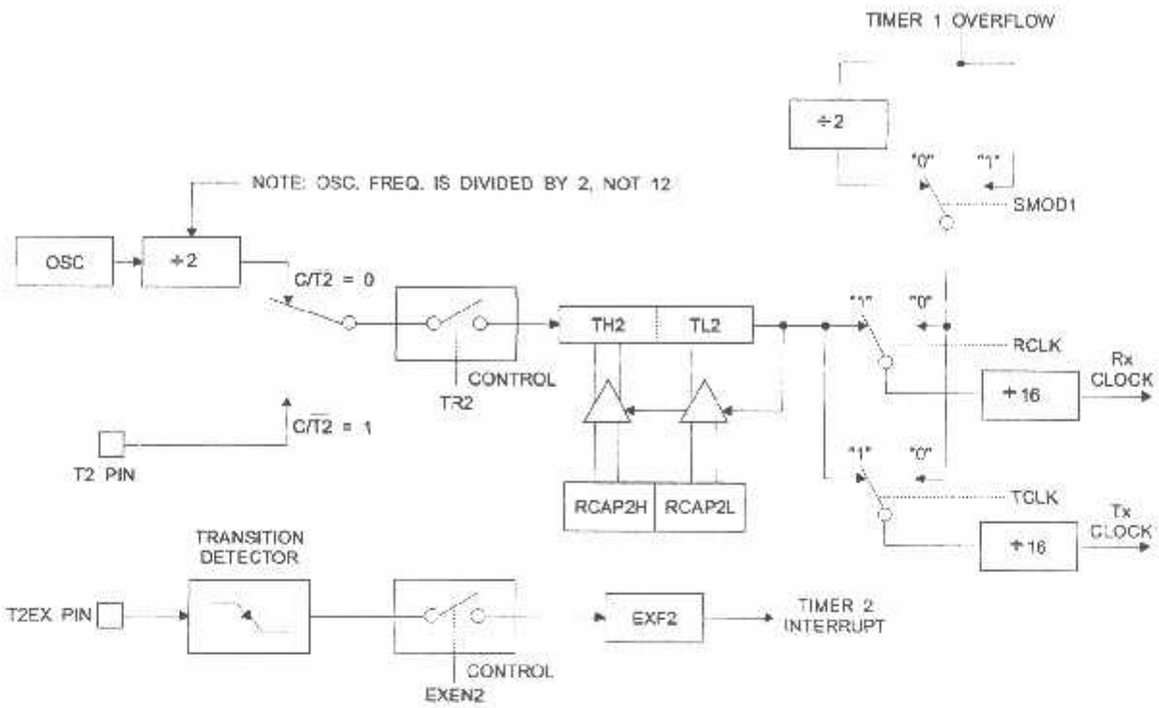
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - \text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus, when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Figure 4. Timer 2 in Baud Rate Generator Mode



Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

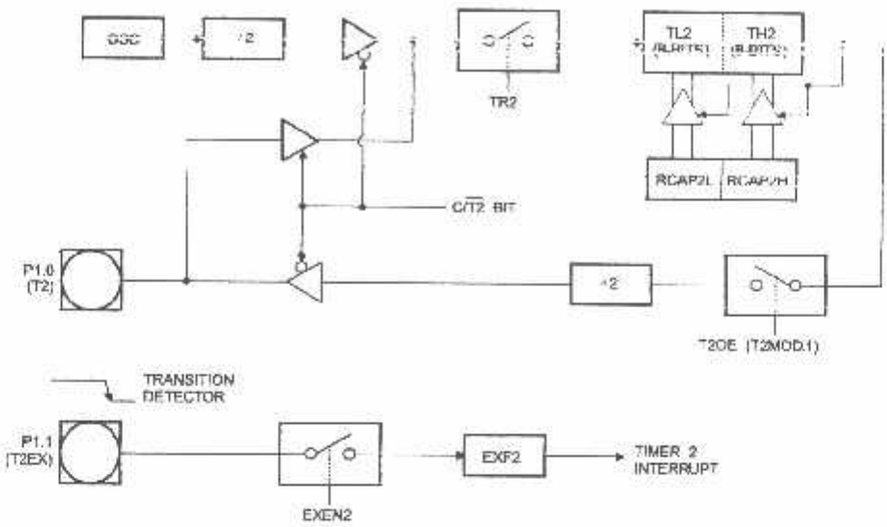
To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536-(\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Figure 5. Timer 2 in Clock-Out Mode



Interrupts

The AT89S52 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 6.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 5 shows that bit position IE.6 is unimplemented. User software should not write a 1 to this bit position, since it may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 7. Interrupt Enable (IE) Register

(MSB) (LSB)

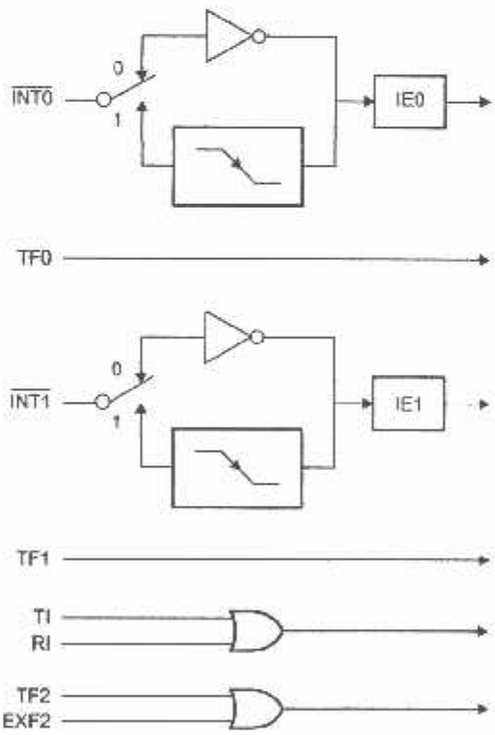
EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

Figure 6. Interrupt Sources



Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 7. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 8. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

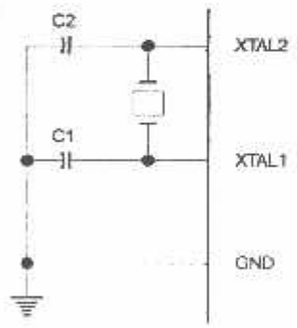
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 7. Oscillator Connections



Note: 1. C1, C2 – 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 8. External Clock Drive Configuration

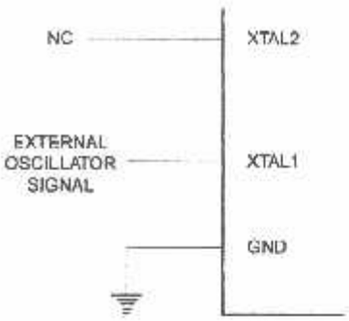


Table 8. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 9. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Programming the Flash – Parallel Mode

The AT89S52 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S52 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S52, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S52, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{pp}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S52 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 52H indicates AT89S52
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

Serial Programming Algorithm

To program and verify the AT89S52 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 11.

Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 10. Flash Programming Modes

Mode	V_{CC}	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.4-0 Address	P1.7-0 Address
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A12-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A12-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	X 0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	52H	X 0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	X 0010	00H

Notes:
1. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{BSY}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 9. Programming the Flash Memory (Parallel Mode)

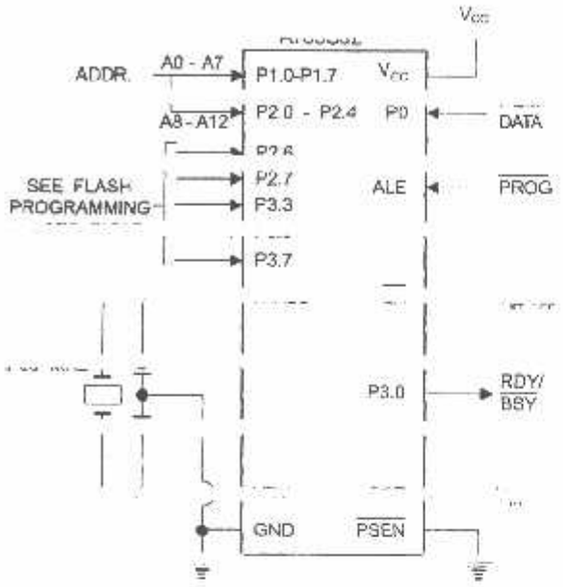
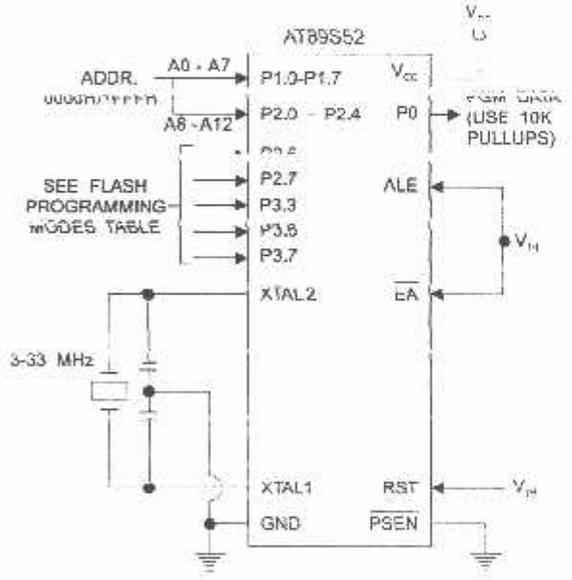


Figure 10. Verifying the Flash Memory (Parallel Mode)



Flash Programming and Verification Characteristics (Parallel Mode)

T_A = 20°C to 30°C, V_{CC} = 4.5 to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	0.2	1	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		50	µs

Figure 11. Flash Programming and Verification Waveforms – Parallel Mode

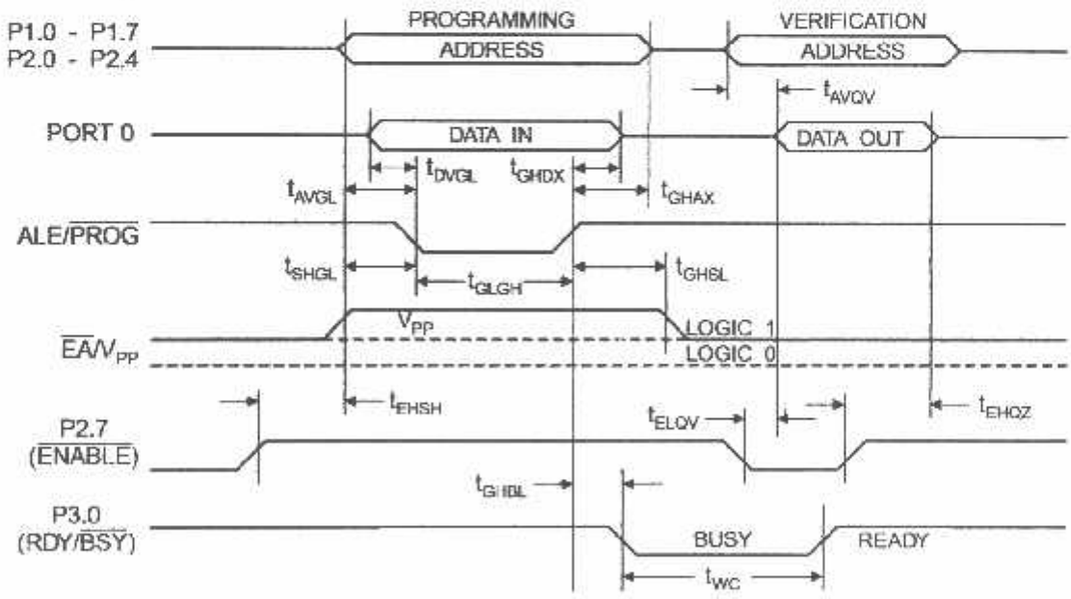
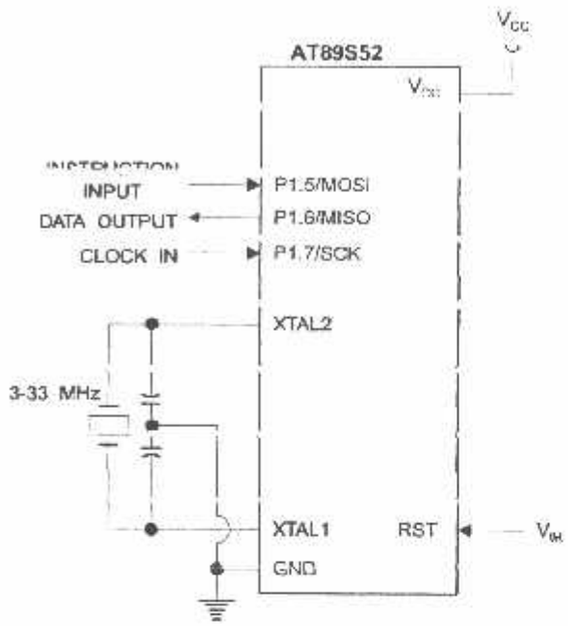


Figure 12. Flash Memory Serial Downloading



Flash Programming and Verification Waveforms – Serial Mode

Figure 13. Serial Programming Waveforms

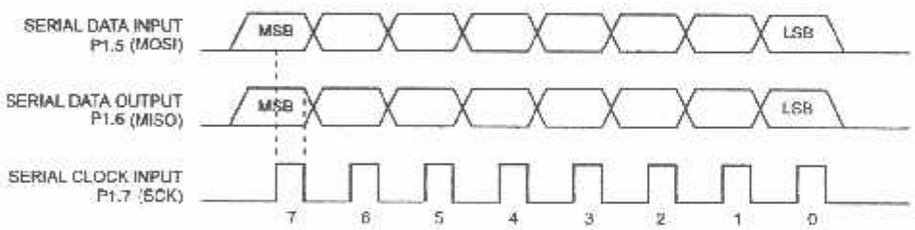


Table 11. Serial Programming Instruction Set

Instruction	Instruction Format Byte 1	Byte 2	Byte 3	Byte 4	Operation
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Write Lock Bits[1]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xxx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Reac Signature Bytes	0010 1000	xxx A12 A11 A10 A9 A8	A7 xxx xxx0	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Note: 1. B1 = 0, B2 = 0 —> Mode 1, no lock protection
B1 = 0, B2 = 1 —> Mode 2, lock bit 1 activated
B1 = 1, B2 = 0 —> Mode 3, lock bit 2 activated
B1 = 1, B2 = 1 —> Mode 4, lock bit 3 activated

} Each of the lock bit modes needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Serial Programming Characteristics

Figure 14. Serial Programming Timing

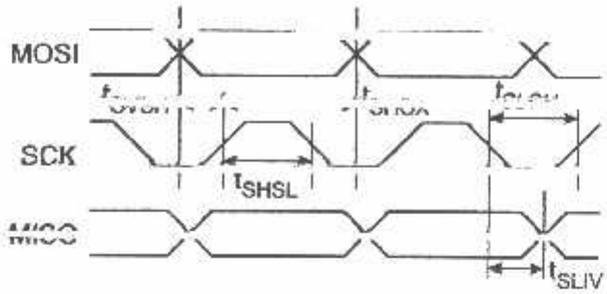


Table 12. Serial Programming Characteristics, T_A = -40° C to 85° C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	3		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	8 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	8 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[1]	V_{CC} = 5.5V		50	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

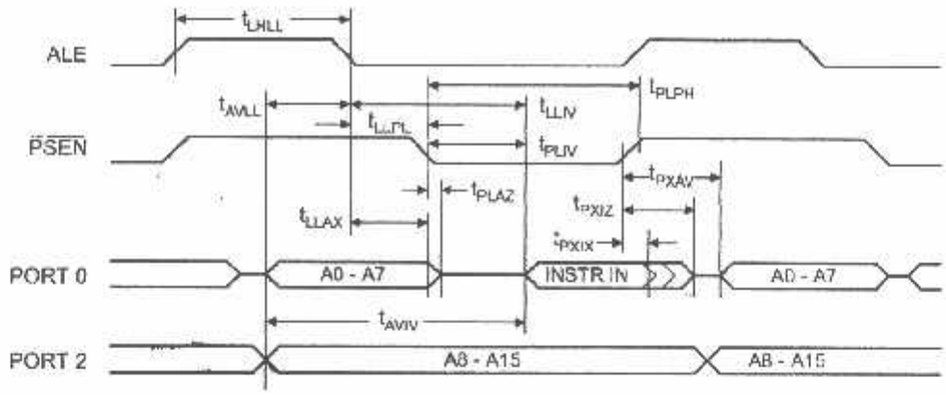
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

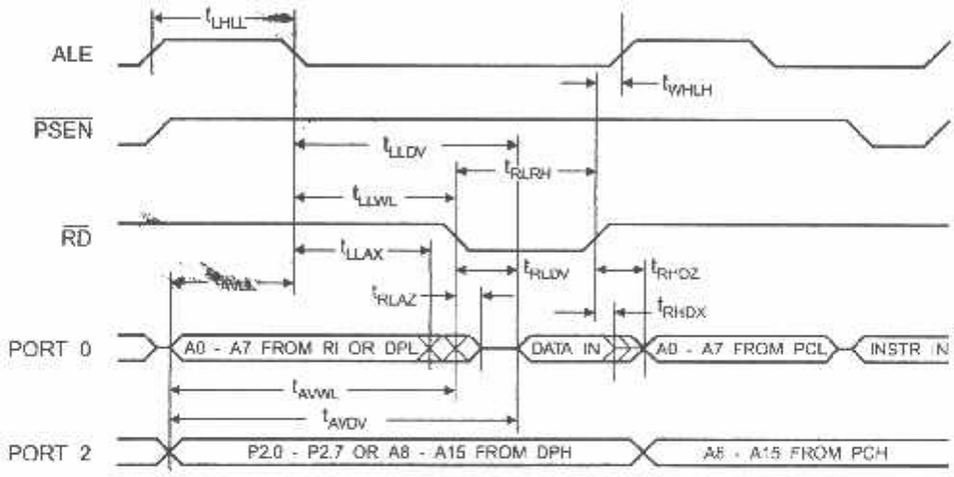
External Program and Data Memory Characteristics

		12 MHz Oscillator		Variable Oscillator		
Symbol	Parameter	Min	Max	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-25		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-25		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

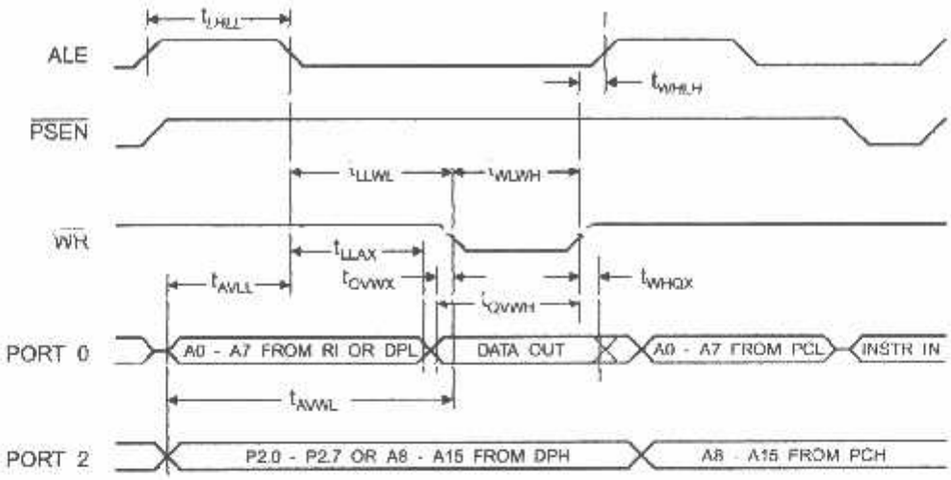
External Program Memory Read Cycle



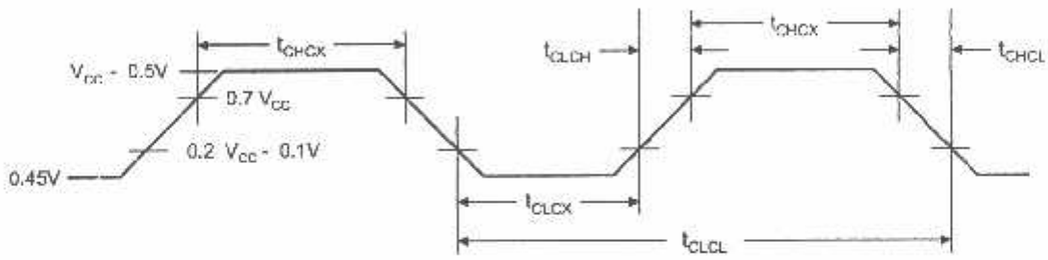
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

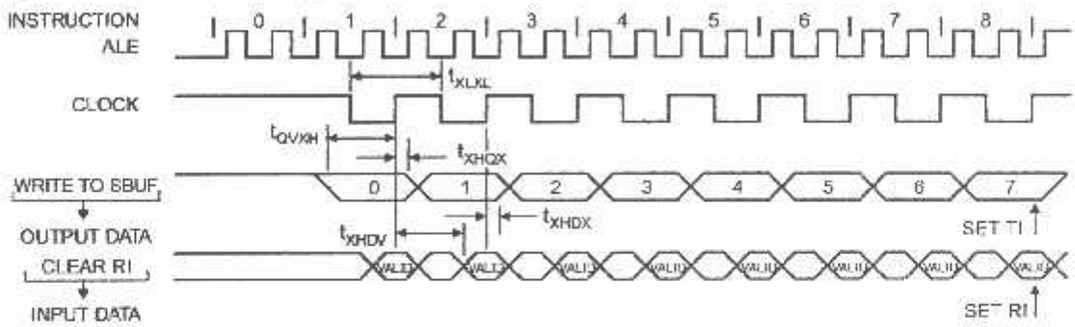
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	33	MHz
t_{CLCL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

Serial Port Timing: Shift Register Mode Test Conditions

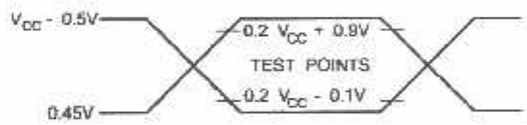
The values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-80		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

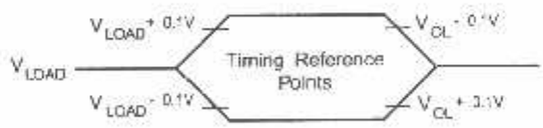


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

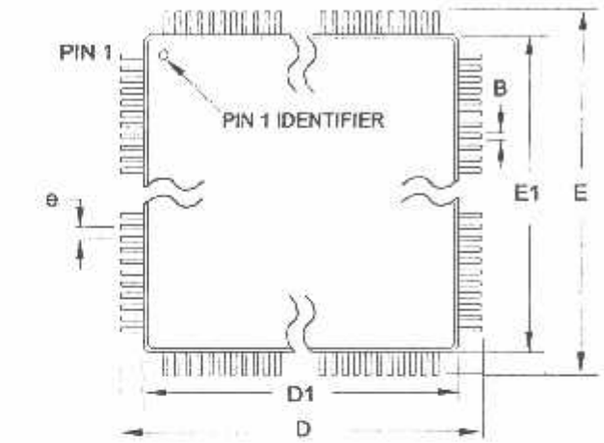
Ordering Information

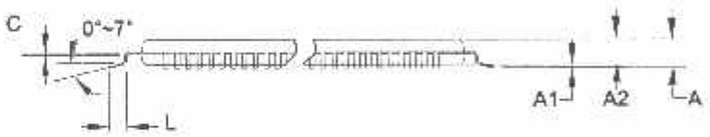
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S52-24AC AT89S52-24JC AT89S52-24PC AT89S52-24SC	44A 44J 40P6 42PS6	Commercial (0° C to 70° C)
		AT89S52-24AI AT89S52-24JI AT89S52-24PI AT89S52-24SI	44A 44J 40P6 42PS6	Industrial (-40° C to 85° C)
33	4.5V to 5.5V	AT89S52-33AC AT89S52-33JC AT89S52-33PC AT89S52-33SC	44A 44J 40P6 42PS6	Commercial (0° C to 70° C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leadec Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
42PS6	42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Packaging Information

44A – TQFP





COMMON DIMENSIONS
(Unit of Measure = mm)

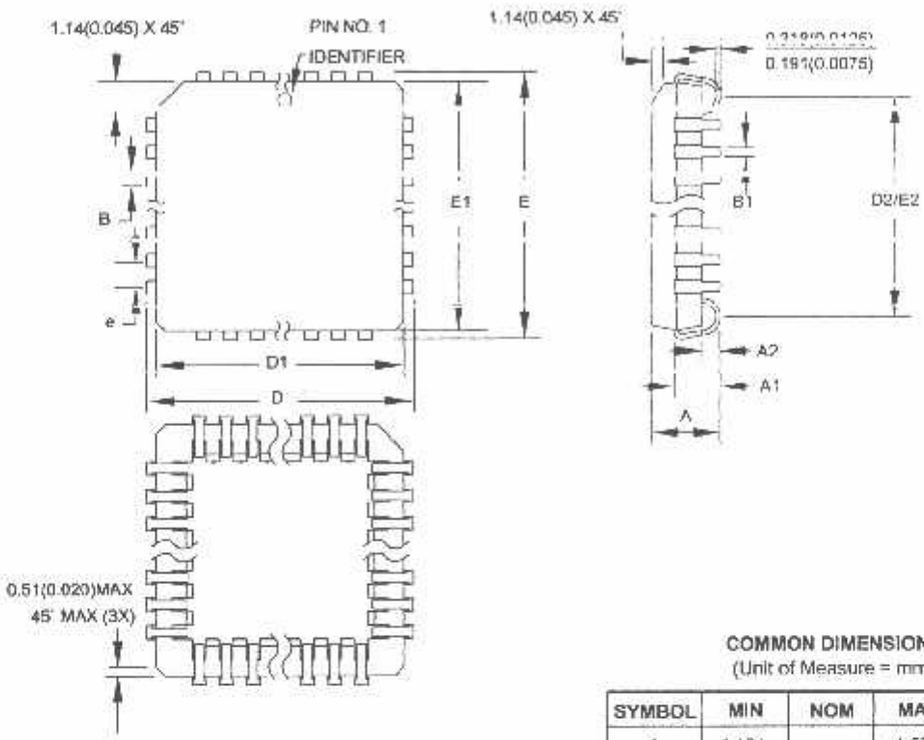
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A**, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

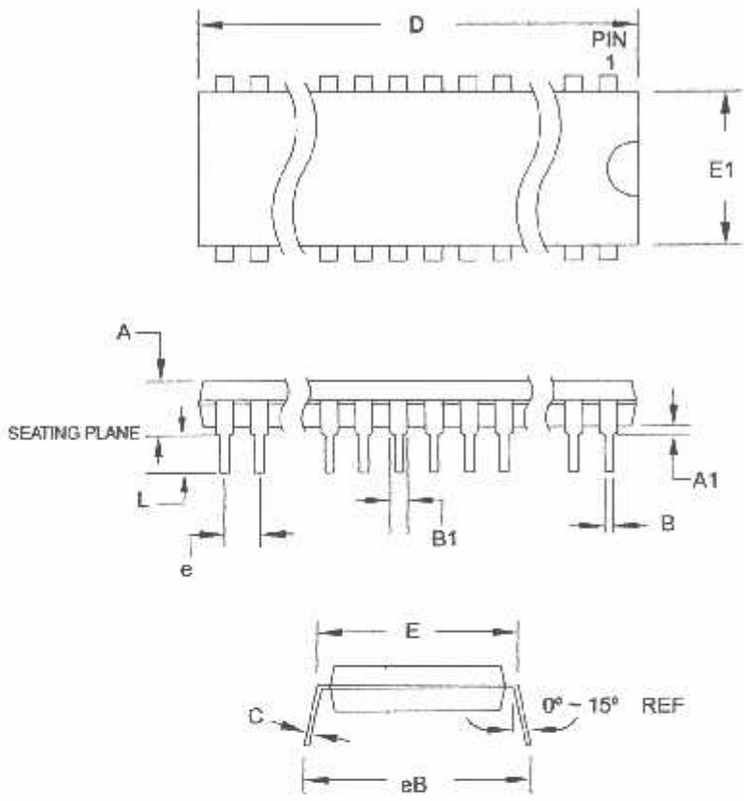
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

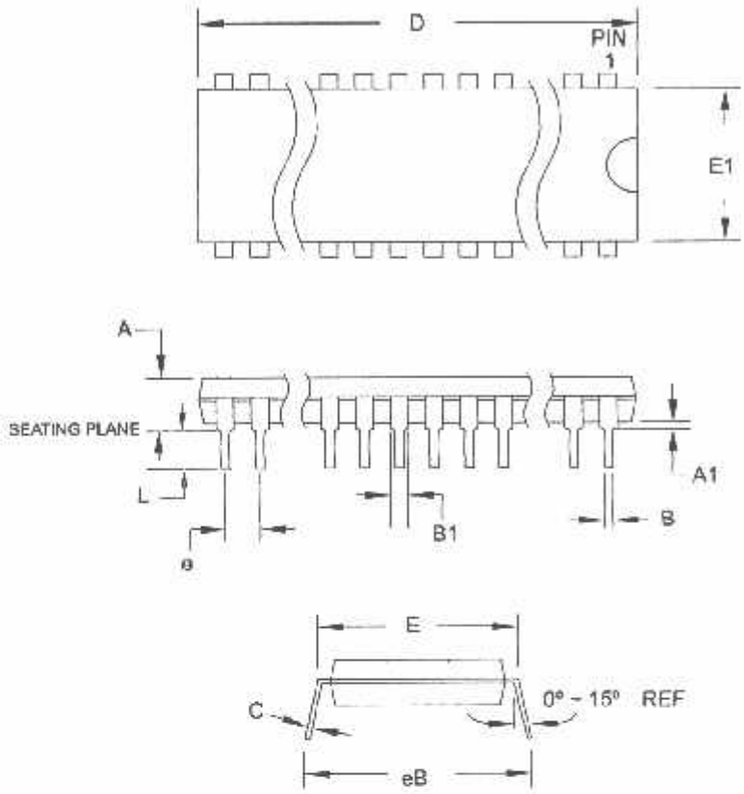
SYMBOL	MIN	NOM	MAX	NOTE
A	–		4.826	
A1	0.381	–	–	
D	52.070		52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041		1.651	
L	3.048		3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

2325 Orchard Parkway San Jose, CA 95131	**TITLE** **40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	**DRAWING NO.** 40P6	**REV.** B

42PS6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.83	
A1	0.51	–	–	
D	36.70	–	36.96	Note 2
E	15.24	–	15.88	
E1	13.46	–	13.97	Note 2
B	0.38	–	0.56	
B1	0.76	–	1.27	
L	3.05	–	3.43	
C	0.20	–	0.30	
eB	–	–	18.55	
e	1.78 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/6/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**42PS6**, 42-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	42PS6	A

National Semiconductor

December 1994

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

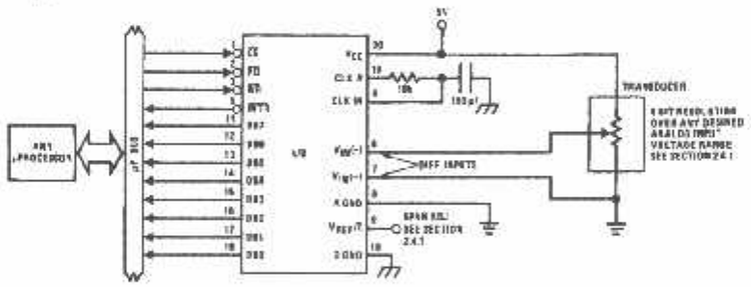
Features

- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

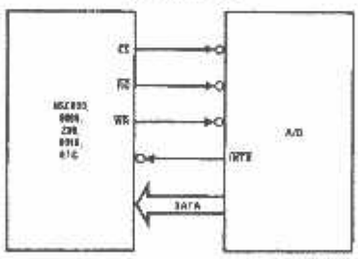
- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 μs

Typical Applications



TL/H/5671–1

8080 Interface



TL/H/5671–31

Part Number	Full-Scale Adjusted	Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity) $V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC} +0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ, ADC0802LJ/883	−55°C ≤ T_A ≤ +125°C
ADC0801/02/03/04LCJ	−40°C ≤ T_A ≤ +85°C
ADC0801/02/03/05LCN	−40°C ≤ T_A ≤ +85°C
ADC0804LCN	0°C ≤ T_A ≤ +70°C
ADC0802/03/04LCV	0°C ≤ T_A ≤ +70°C
ADC0802/03/04LCWM	0°C ≤ T_A ≤ +70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			±1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC} = 5 V_{DC} ±10% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC} = 5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of WR Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of RD to Output Data Valid)	C_L = 100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of RD to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS (Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately)						
V_{IN}(1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = 5V_{DC} and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN} = 5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN} = 0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+) - (V_T-)$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O = 360 µA V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O = −360 µA V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND INTR						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs INTR Output	 I_{OUT} = 1.6 mA, V_{CC} = 4.75 V_{DC} I_{OUT} = 1.0 mA, V_{CC} = 4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −360 µA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O = −10 µA, V_{CC} = 4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT} = 0 V_{DC} V_{OUT} = 5 V_{DC}	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A = 25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A = 25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	f_{CLK} = 640 kHz, $V_{REF}/2$ = NC, T_A = 25°C and $\overline{CS}$ = 5V		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

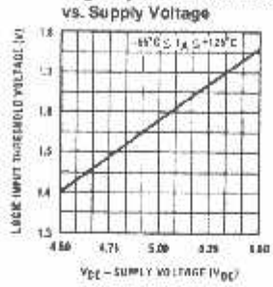
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 3*.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803 and ADC0805, and in the ADC0804LCJ, each resistor is typically 15 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

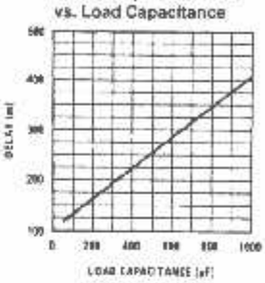
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

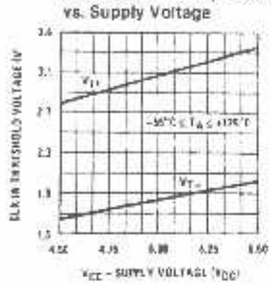
Logic Input Threshold Voltage vs. Supply Voltage



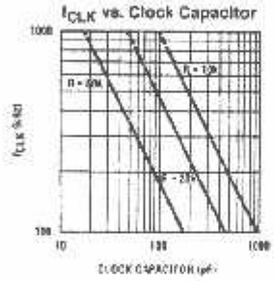
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



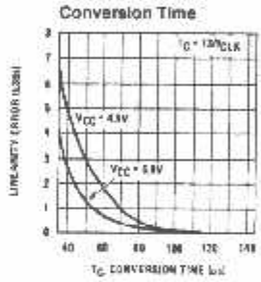
CLK IN Schmitt Trip Levels vs. Supply Voltage



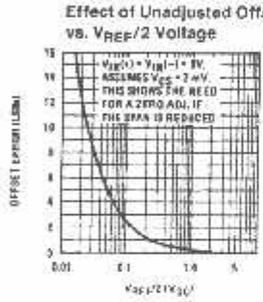
I_{CLK} vs. Clock Capacitor



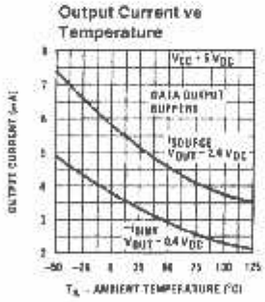
Full-Scale Error vs Conversion Time



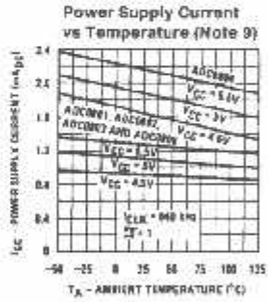
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



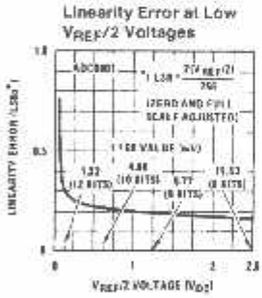
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)



Linearity Error at Low $V_{REF}/2$ Voltages



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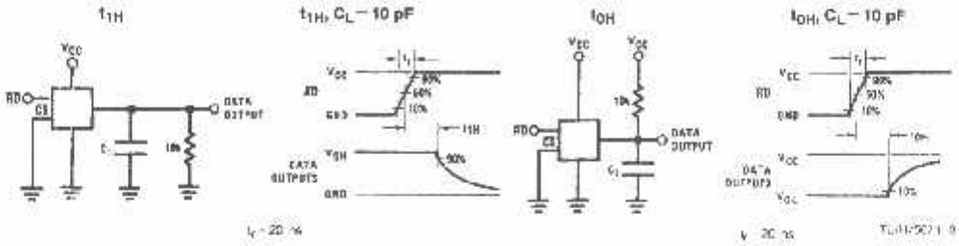
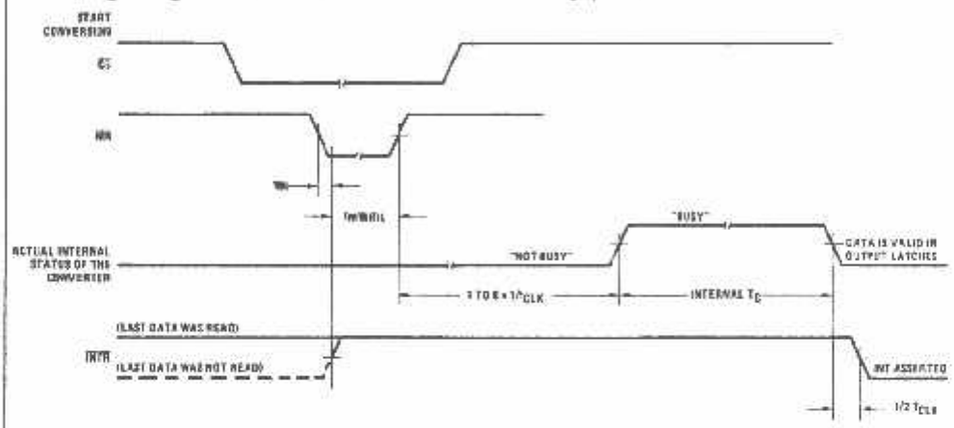
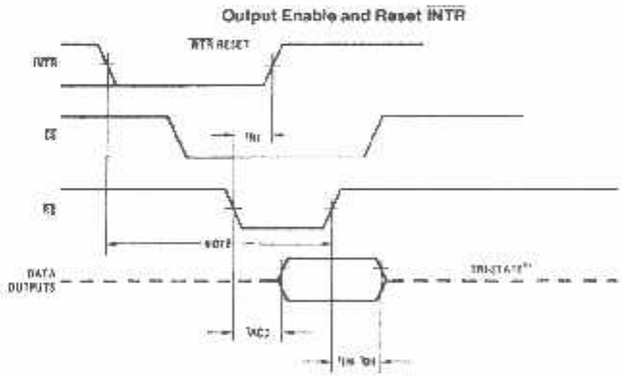
TRI-STATE Test Circuits and Waveforms



Timing Diagrams (All timing is measured from the 50% voltage points)



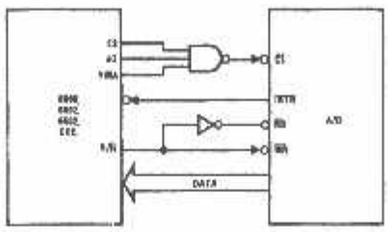
Output Enable and Reset $\overline{INTR}$



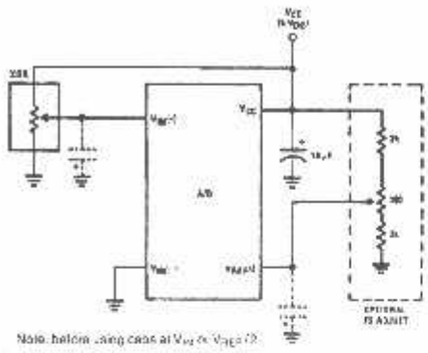
Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of $\overline{INTR}$ in order to guarantee reset of $\overline{INTR}$.

Typical Applications (Continued)

6800 Interface

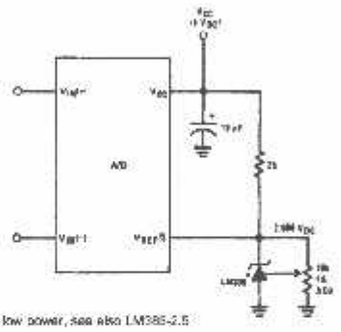


Ratiometric with Full-Scale Adjust



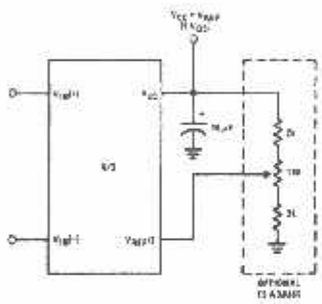
Note, before using caps at V_{cc} or $V_{REF}/2$ see section 2.0 Input Bypass Capacitors

Absolute with a 2.500V Reference

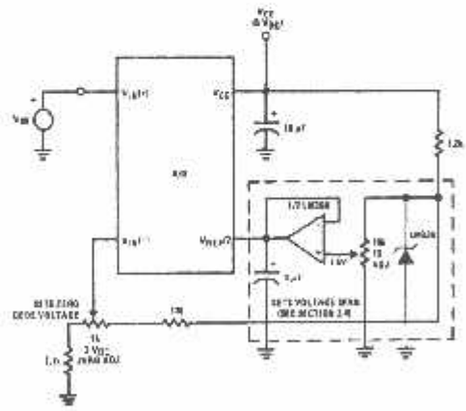


*For low power, see also LM385-2.5

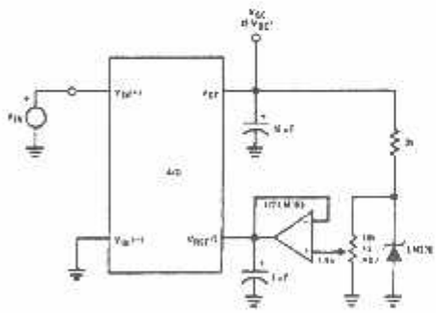
Absolute with a 5V Reference



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$

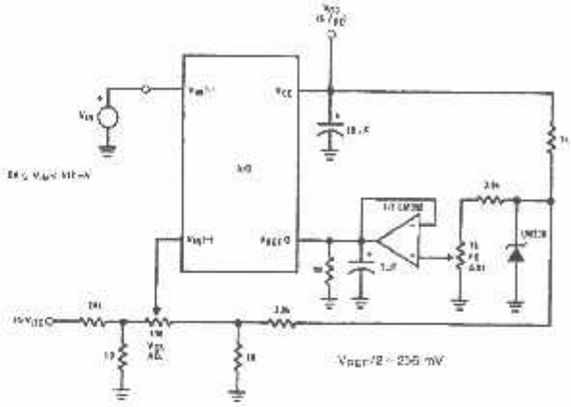


Span Adjust: $0V \leq V_{IN} \leq 3V$



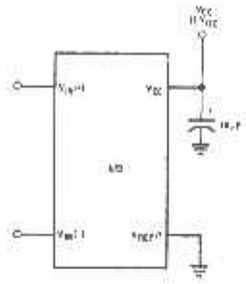
Typical Applications (Continued)

Directly Converting a Low-Level Signal



$V_{REF}/2 = 256$ mV

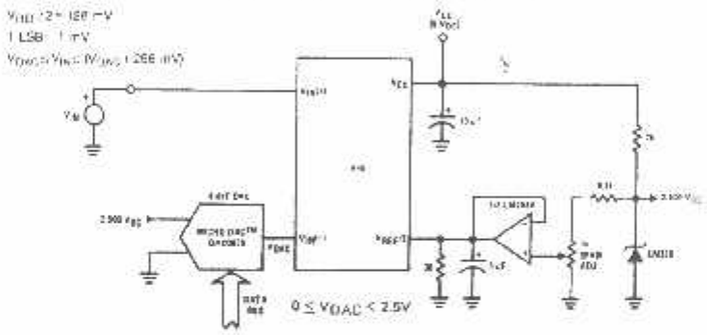
A µP Interfaced Comparator



For $V_{IN}(+) > V_{IN}(-)$
Output = FF_{HEX}
For $V_{IN}(+) < V_{IN}(-)$
Output = 00_{HEX}

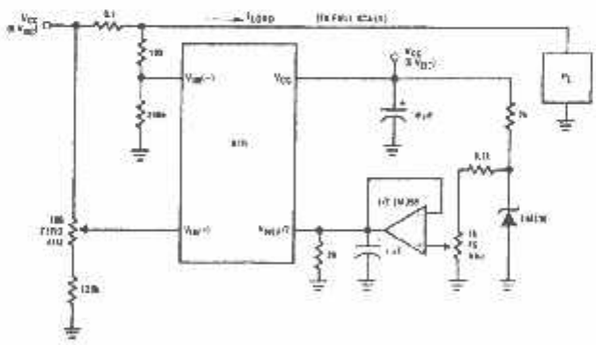
1 mV Resolution with µP Controlled Range

$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} = V_{IN} \pm (V_{REF}/2)$ (mV)



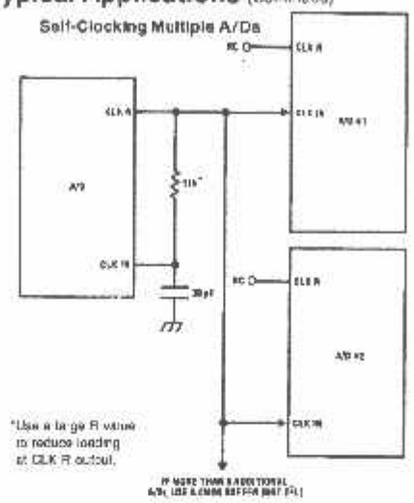
$0 \le V_{DAC} < 2.5V$

Digitizing a Current Flow



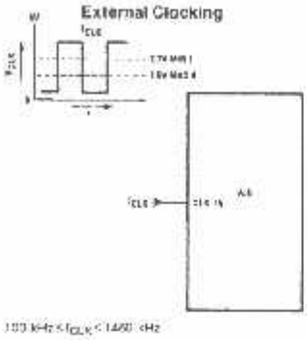
Typical Applications (Continued)

Self-Clocking Multiple A/Ds



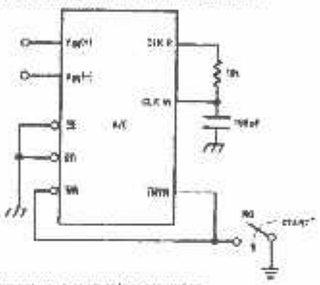
*Use a large R value to reduce loading at CLK R output.

External Clocking



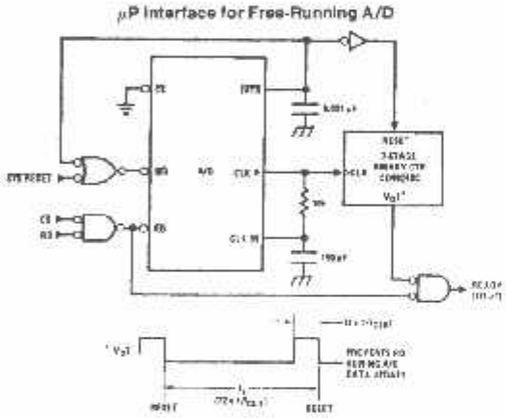
100 kHz ≤ f_{CLK} ≤ 1460 kHz

Self-Clocking in Free-Running Mode

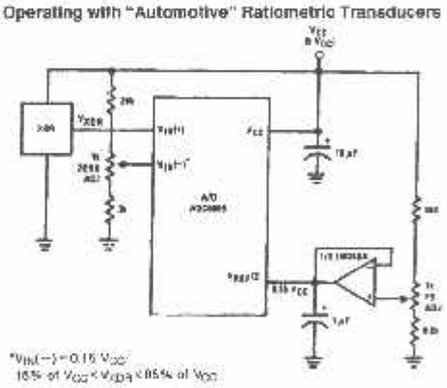


*After powerup, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

µP Interface for Free-Running A/D

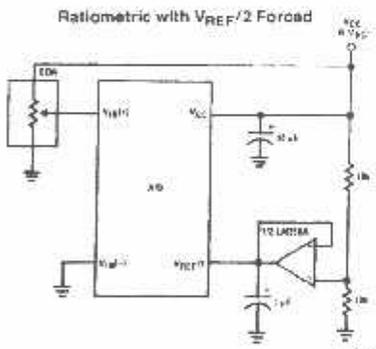


Operating with "Automotive" Ratiometric Transducers



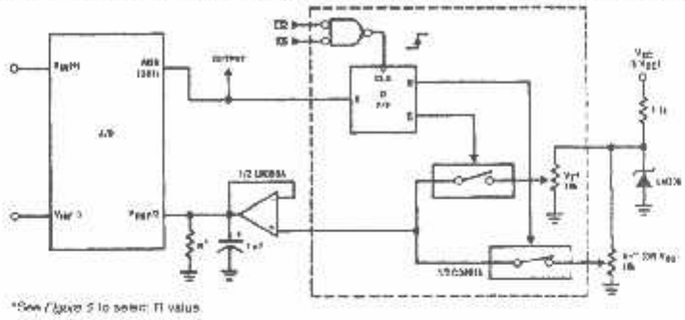
*$V_{IN}(-)$ = 0.15 V_{CC}
15% of V_{CC} < V_{XDR} < 85% of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



Typical Applications (Continued)

µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)

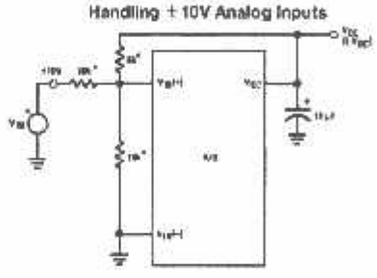


*See Figure 5 to select R value

DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$

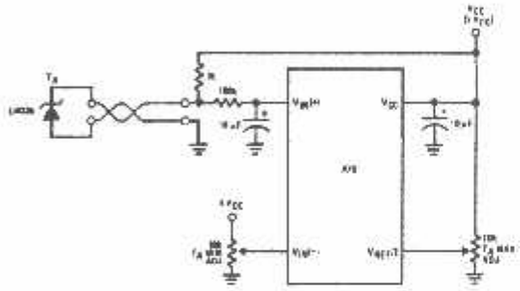
Omit circuitry within the dotted area if hysteresis is not needed

Handling ±10V Analog Inputs

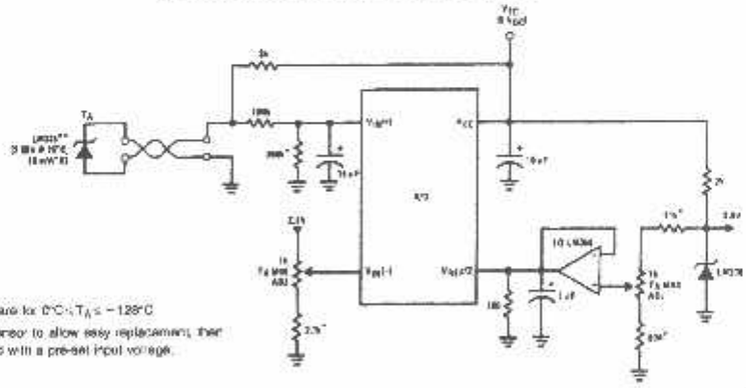


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



µP Interfaced Temperature-to-Digital Converter

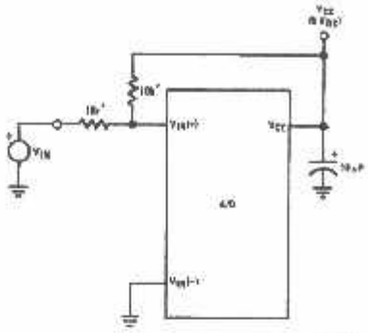


*Circuit values shown are for 0°C ≤ T_A ≤ +125°C

**Can calibrate each sensor to allow easy replacement; then A/D can be calibrated with a pre-set input voltage.

Typical Applications (Continued)

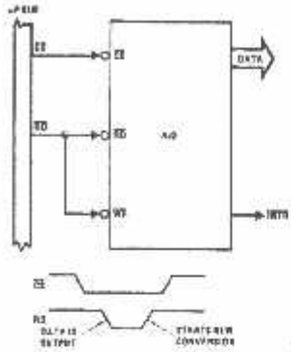
Handling ±5V Analog Inputs



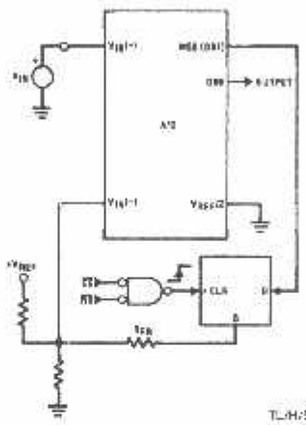
TL/H/5671–33

*Beckman Instruments #694-3-R10K resistor array

Read-Only Interface

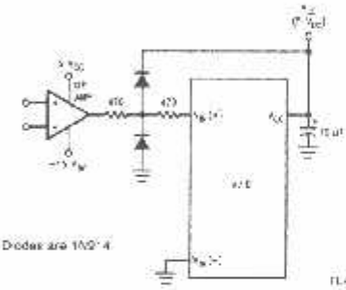


µP Interfaced Comparator with Hysteresis



TL/H/5671–35

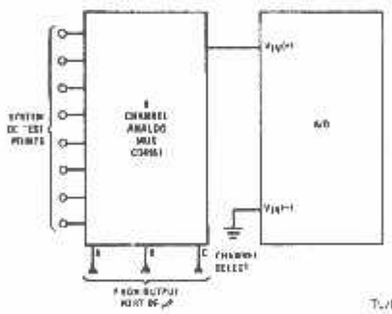
Protecting the Input



Diodes are 1N914

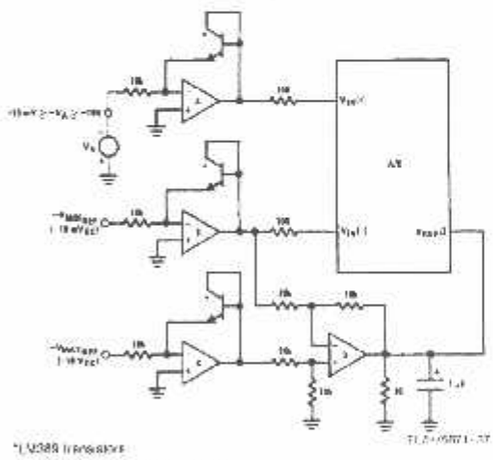
TL/H/5671–36

Analog Self-Test for a System



TL/H/5671–38

A Low-Cost, 3-Decade Logarithmic Converter

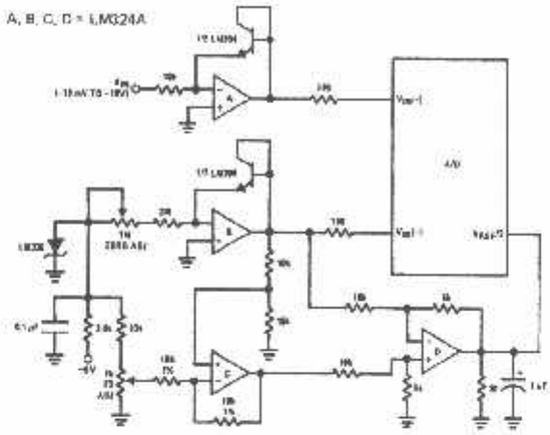


*LM389 transistors

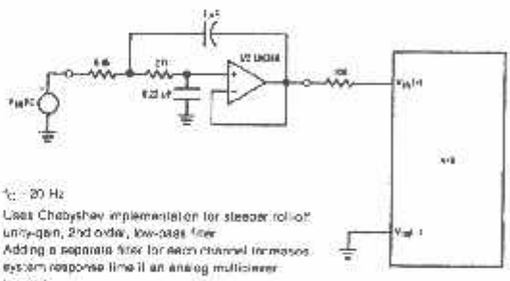
A, B, C, D = LM324 A op amps

Typical Applications (Continued)

3-Decade Logarithmic A/D Converter



Noise Filtering the Analog Input

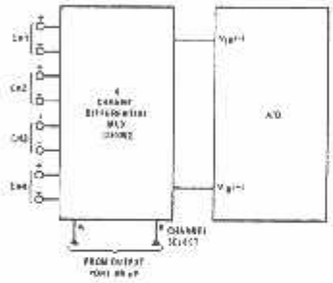


f_C = 20 Hz

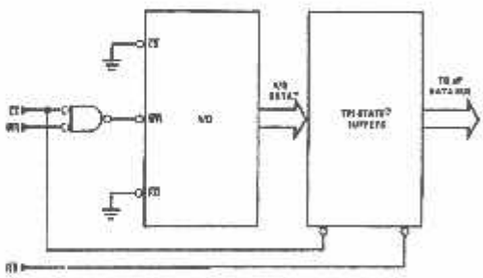
Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter

Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

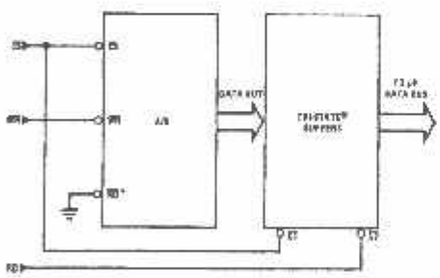


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of INTR

Increasing Bus Drive and/or Reducing Time on Bus



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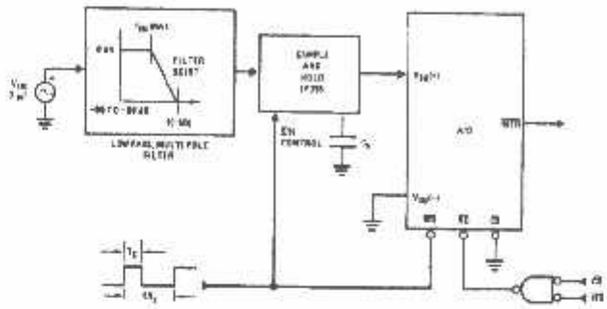
*Allows output data to set up at falling edge of CS

Typical Applications (Continued)

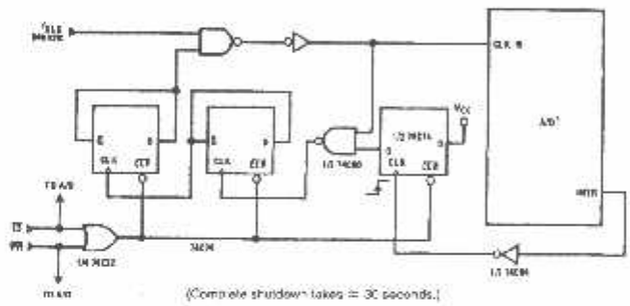
Sampling an AC Input Signal



Note 1: Oversample whenever possible (f_{clock} is > 2(f − 80)) to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

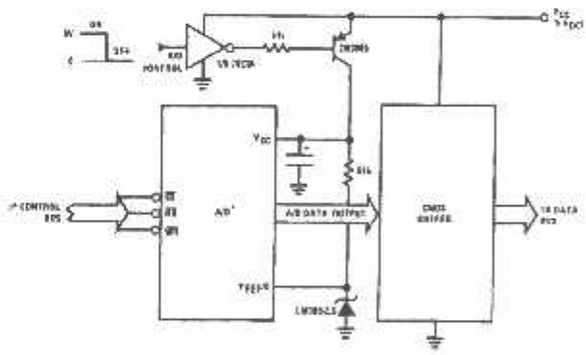
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes = 3C seconds.)

Power Savings by A/D and V_{REF} Shutdown



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*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-values (A−1, A, A+1, ...) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ± ½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend ± ½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

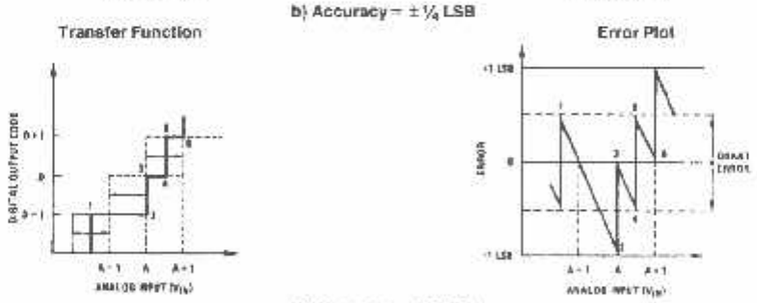
Figure 1b shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than +¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is −½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.

a) Accuracy = ±0 LSB: A Perfect A/D

b) Accuracy = ±¼ LSB



c) Accuracy = ½ LSB

TL/H/5271-12

FIGURE 1. Clarifying the Error Specs of an A/D Converter

Functional Description (Continued)

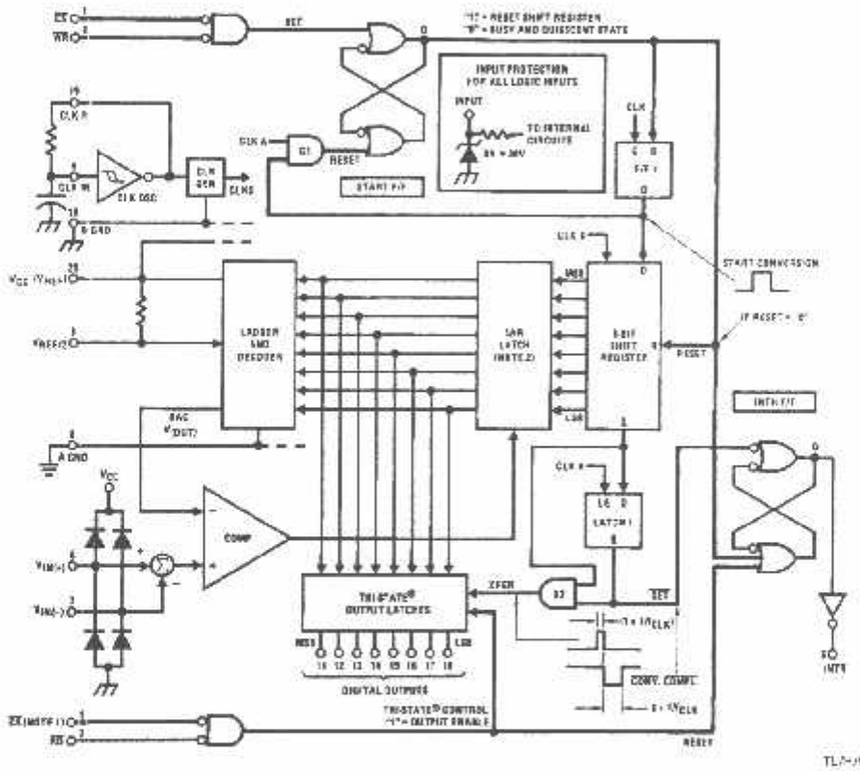
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage $[V_{IN}(+) - V_{IN}(-)]$ to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS} = 0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 2*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt ($\overline{INTR}$) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, the reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.



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Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

Functional Description (Continued)

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard I^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(-)$ and $V_{IN}(-)$ is 4-1/2 clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to 1/4 LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)}$$

or

$$V_P \approx 1.3V$$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

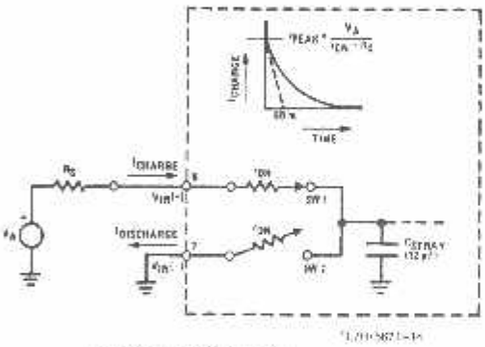
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



R_{ON} of SW 1 and SW 2 = 5 kΩ

$(=)\tau_{ON}\, C_{STRAY} = 5\,k\Omega \times 12\,pF = 60\,ns$

FIGURE 3. Analog Input Impedance

Functional Description (Continued)

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of V_{CC} +50 mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(-)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 µA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 µF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

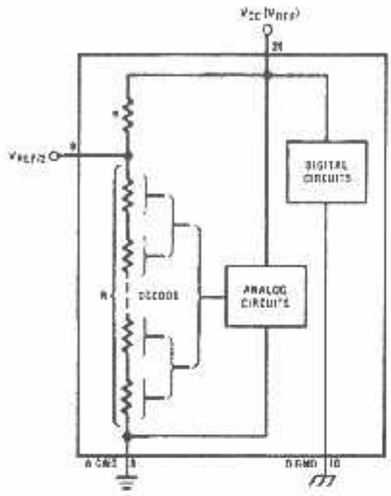
2.3.4 Noise

The leads to the analog inputs (pin 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a "full-scale adjustment" of the A/D (adjust $V_{REF}/2$ for a proper full scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.



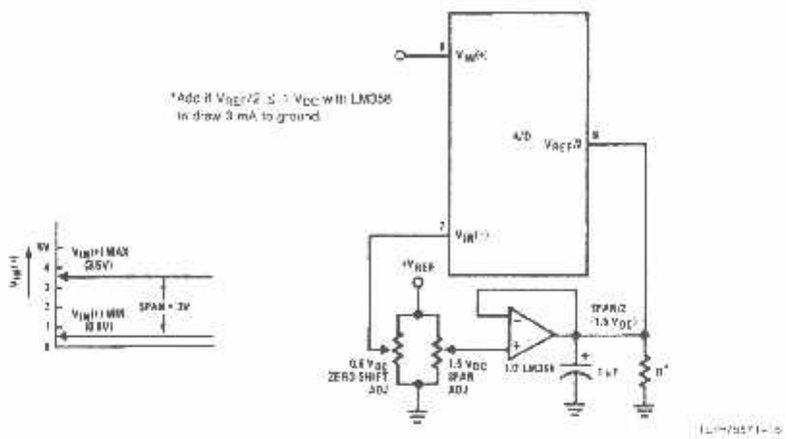
TL/H/5671–15

FIGURE 4. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC} instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

Functional Description (Continued)



a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 3.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500$ V_{DC}).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

Functional Description (Continued)

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\text{fs adj} = V_{MAX} + 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX} = The high end of the analog input range

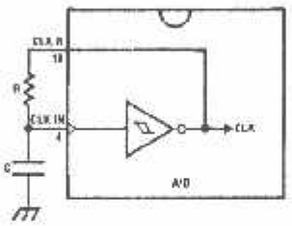
and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6*.



$$f_{CLK} = \frac{1}{1.1\ RC}$$

$R \approx 10\ k\Omega$

TL/H/5611-11

FIGURE 6. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in the latch. The INTR output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. The $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 µF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

Functional Description (Continued)

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120−1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in Table I, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A−C" directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

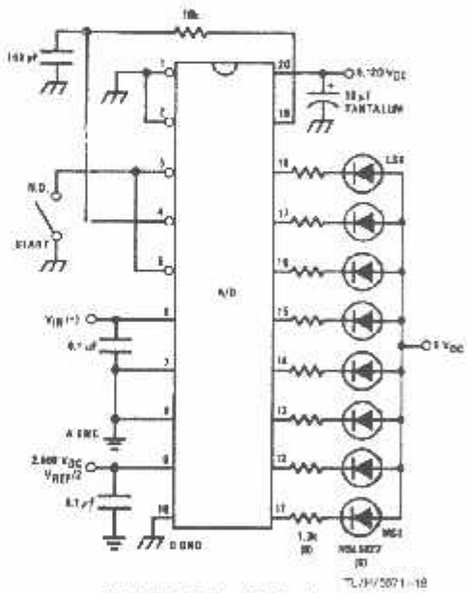


FIGURE 7. Basic A/D Tester

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10*.

Functional Description (Continued)

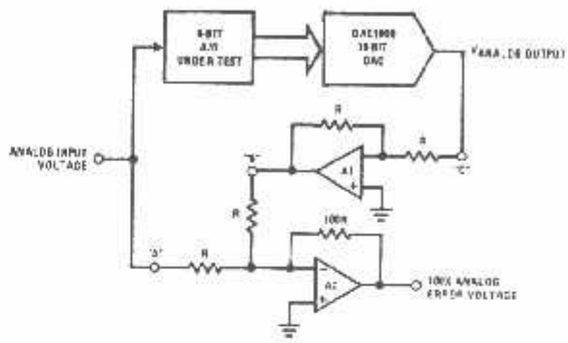
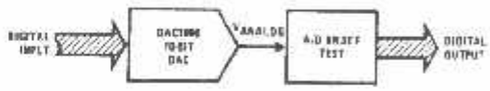


FIGURE 8. A/D Tester with Analog Error Output



TL/H/5671-15

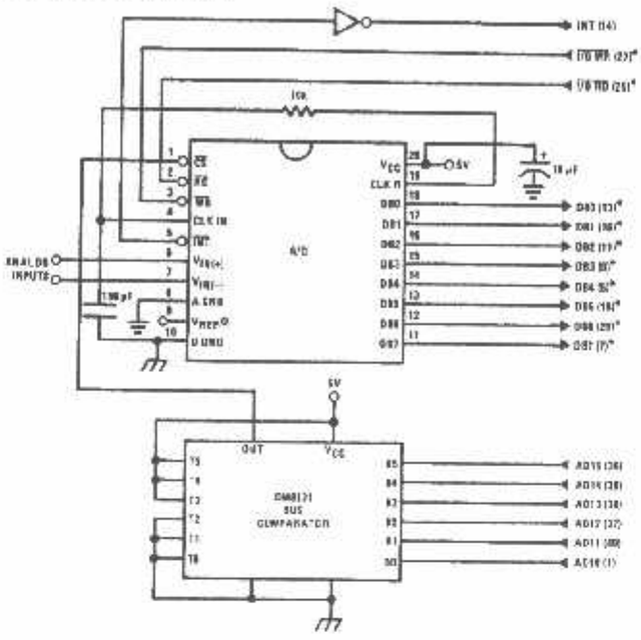
FIGURE 9. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$	
		MS GROUP	LS GROUP	VMS GROUP*	VLS GROUP*
F	1 1 1 1	15/16	15/256	4.800	0.300
E	1 1 1 0	7/8	7/128	4.480	0.280
D	1 1 0 1	13/16	13/256	4.160	0.260
C	1 1 0 0	3/4	3/64	3.840	0.240
B	1 0 1 1	11/16	11/256	3.520	0.220
A	1 0 1 0	5/8	5/128	3.200	0.200
9	1 0 0 1	9/16	9/256	2.880	0.180
8	1 0 0 0	1/2	1/32	2.560	0.160
7	0 1 1 1	7/16	7/256	2.240	0.140
6	0 1 1 0	3/8	3/128	1.920	0.120
5	0 1 0 1	5/16	2/256	1.600	0.100
4	0 1 0 0	1/4	1/64	1/280	0.080
3	0 0 1 1	3/16	3/256	0.960	0.060
2	0 0 1 0	1/8	1/128	0.640	0.040
1	0 0 0 1	1/16	1/256	0.320	0.020
0	0 0 0 0			0	0

*Display Output = VMS Group + VLS Group

Functional Description (Continued)



TL/H/5071–19

Note 1: *Pin numbers for the DP8228 system controller, others are INS8080A.

Note 2: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 10. ADC0801–INS8080A CPU Interface

SAMPLE PROGRAM FOR *FIGURE 10* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:      JMP     LD DATA
   *        *          *
   *        *          *
0100    21 00 02    START:      LXI H 020CH     ;HL pair will point to
                                                ;data storage locations
0103    31 00 04    RETURN:     LXI SP 04C0H    ;Initialize stack pointer (Note 1)
0106    7D                      MOV A, L        ;Test # of bytes entered
0107    FE 0F                   CPI 0F H        ;If # = 16, JMP to
0109    CA 13 01                JZ CONT         ;user program
010C    D3 E0                   OUT E0 H        ;Start A/D
010E    FB                      EI              ;Enable interrupt
010F    00          LOOP:       NOP             ;Loop until end of
0110    C3 0F 01                JMP LOOP        ;conversion
0113       *        CONT:          *
   *        *          *            *
   *        *       (User program to   *
   *        *       process data)      *
   *        *          *            *
   *        *          *            *
0300    DB E0       LD DATA:    IN E0 H         ;Load data into accumulator
0302    77                      MOV M, A        ;Store data
0303    23                      INX H           ;Increment storage pointer
0304    C3 03 01                JMP RETURN
```

Note 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 2: All address used were arbitrarily chosen.

Functional Description (Continued)

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

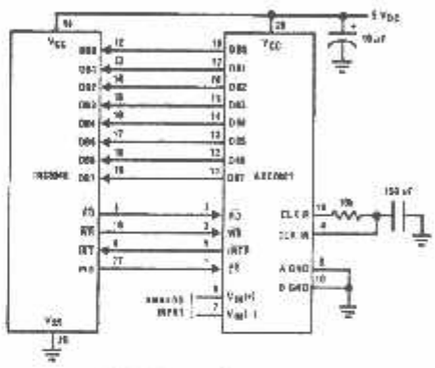
4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 10* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs - one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 11*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.



TL/H/5571-31

FIGURE 11. INS8048 Interface

SAMPLE PROGRAM FOR *FIGURE 11* INS8048 INTERFACE

```
04 10                   JMP     10H             ;Program starts at addr 10
                        ORG     3H
04 50                   JMP     50H             ;Interrupt jump vector
                        ORG     10H             ;Main program
99 FE                   ANL     P1, #0FEH       ;Chip select
81                      MOVX    A, @R1          ;Read in the 1st data
                                                ;to reset the intr
B9 01           START:  ORL     P1, #1          ;Set port pin high
B8 20                   MOV     R0, #20H        ;Data address
B9 FF                   MOV     R1, #0FFH       ;Dummy address
BA 10                   MOV     R2, #10H        ;Counter for 16 bytes
23 FF           AGAIN:  MOV     A, #0FFH        ;Set ACC for intr loop
99 FE                   ANL     P1, #0FEH       ;Send CS (bit 0 of P1)
91                      MOVX    @R1, A          ;Send WR out
05                      EN      I               ;Enable interrupt
96 21           LOOP:   JNZ     LOOP            ;Wait for interrupt
EA 1B                   DJNZ    R2, AGAIN       ;If 16 bytes are read
00                      NOP                     ;go to user's program
00                      NOP
                        ORG     50H
81              INDATA: MOVX    A, @R1          ;Input data, CS still low
A0                      MOV     @R0, A          ;Store in memory
18                      INC     R0              ;Increment storage counter
B9 01                   ORL     P1, #1          ;Reset CS signal
27                      CLR     A               ;Clear ACC to get out of
93                      RETR                    ;the interrupt loop
```

Functional Description (Continued)

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 13*.

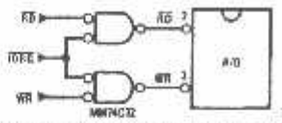


FIGURE 13. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived form the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 14* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded 4/5 line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR. 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 15* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

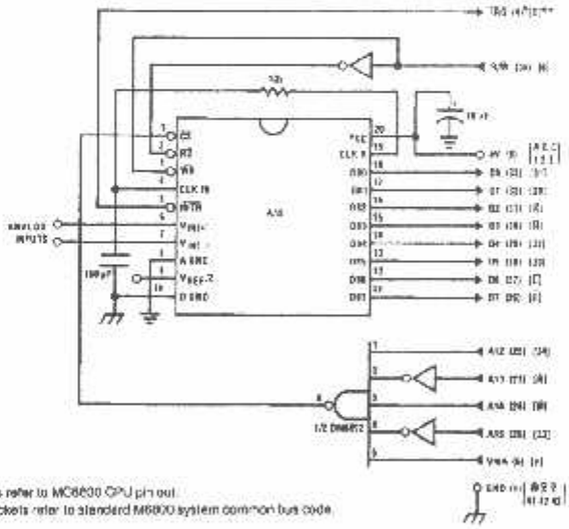
A sample interface program equivalent to the previous one is shown below *Figure 15*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 16*.



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.
Note 2: Number or letters in brackets refer to standard M6800 system common bus code.

FIGURE 14. ADC0801-MC6800 CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 14* ADC0801-MC6800 CPU INTERFACE

```
0010    DF 30       DATAIN  STX     TEMP2       ;Save contents of X
0012    CE 00 2C            LDX     #$002C      ;Upon IRQ low CPU
0015    FF FF F8            STX     $FFF8       ;jumps to 002C
0018    B7 50 00            STAA    $5000       ;Start ADC0801
001B    0E                  CLI
001C    3E          CONVRT  WAI                 ;Wait for interrupt
001D    DE 34               LDX     TEMP1
001F    8C 02 0F            CPX     #$020F      ;Is final data stored?
0022    27 14               BEQ     ENDP
0024    B7 50 00            STAA    $5000       ;Restarts ADC0801
0027    08                  INX
0028    DF 34               STX     TEMP1
002A    20 F0               BRA     CONVRT
002C    DE 34       INTRPT  LDX     TEMP1
002E    B6 50 00            LDAA    $5000       ;Read data
0031    A7 00               STAA    X           ;Store it at X
0033    3B                  RTI
0034    02 00       TEMP1   FDB     $0200       ;Starting address for
                                                ;data storage
0036    00 00       TEMP2   FDB     $0000
0038    CE 02 00    ENDP    LDX     #$0200      ;Reinitialize TEMP1
003B    DF 34               STX     TEMP1
003D    DE 36               LDX     TEMP2
003F    39                  RTS                 ;Return from subroutine
                                                ;To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

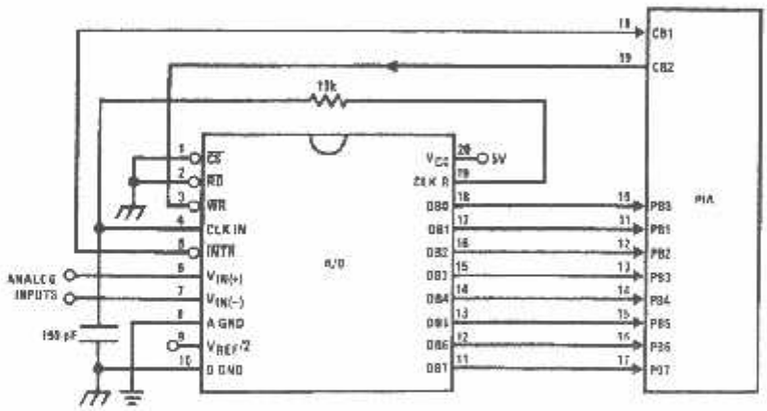


FIGURE 15. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 15* ADC0801–MC6820 PIA INTERFACE

```
0010  CE 00 38   DATAIN  LDX   #$0038    ;Upon IRQ low CPU
0013  FF FF F8           STX   $FFF8     ;jumps to 0038
0016  B6 80 06           LDAA  PIAORB    ;Clear possible IRQ flags
0019  4F                 CLRA
001A  B7 80 07           STAA  PIACR3
001D  B7 80 06           STAA  PIACR3    ;Set Port B as input
0020  0E                 CLI
0021  C6 34              LDAB  #$34
0023  86 3C              LDAA  #$3C
0025  F7 80 07   CONVRT  STAB  PIACR8    ;Start ADC0801
0028  B7 80 07           STAA  PIACR8
002B  3E                 WAI             ;Wait for interrupt
002C  D3 40              LDX   TEMP1
002E  8C 02 0F           CPX   #$020F    ;Is final data stored?
0031  27 0F              BEQ   ENDP
0033  08                 INX
0034  DF 40              STX   TEMP1
0036  20 ED              BRA   CONVRT
0038  D3 40      INTRPT  LDX   TEMP1
003A  B6 80 06           LDAA  PIAOR3    ;Read data in
003D  A7 00              STAA  X         ;Store it at X
003F  3B                 RTI
004C  02 00      TEMP1   FDB   $0200     ;Starting address for
                                         ;data storage
0042  CE 02 C0   ENDP    LDX   #$020C    ;Reinitialize TEMP1
0045  DF 40              STX   TEMP1
0047  39                 RTS             ;Return from subroutine
                 PIAORB  EQU   $8006     ;To user's program
                 PIACRB  EQU   $8007
```

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

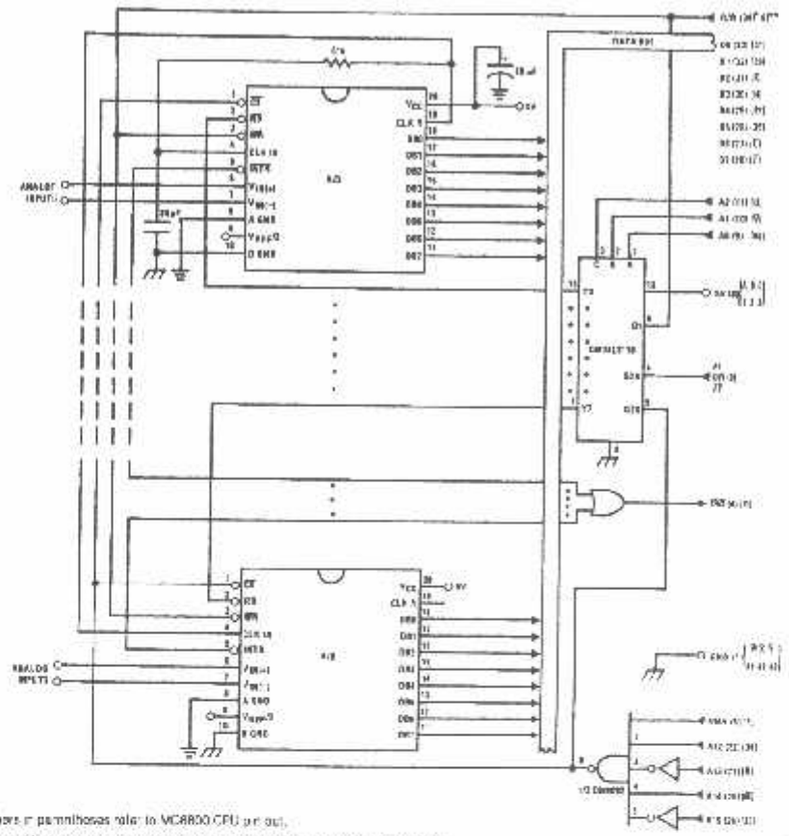
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007); and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers at wires in overview refer to standard MS80C system common bus code.

FIGURE 16. Interfacing Multiple A/Ds to an MC6800 System

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon IRQ LOAD CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$020C	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from Subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

Functional Description (Continued)

SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes; branch to RETURN
003A	08		INX		; No; increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 0028
003F	3B	RETURN	RTI		
0040	80 00	INDEX1	FDB	$8000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 17* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

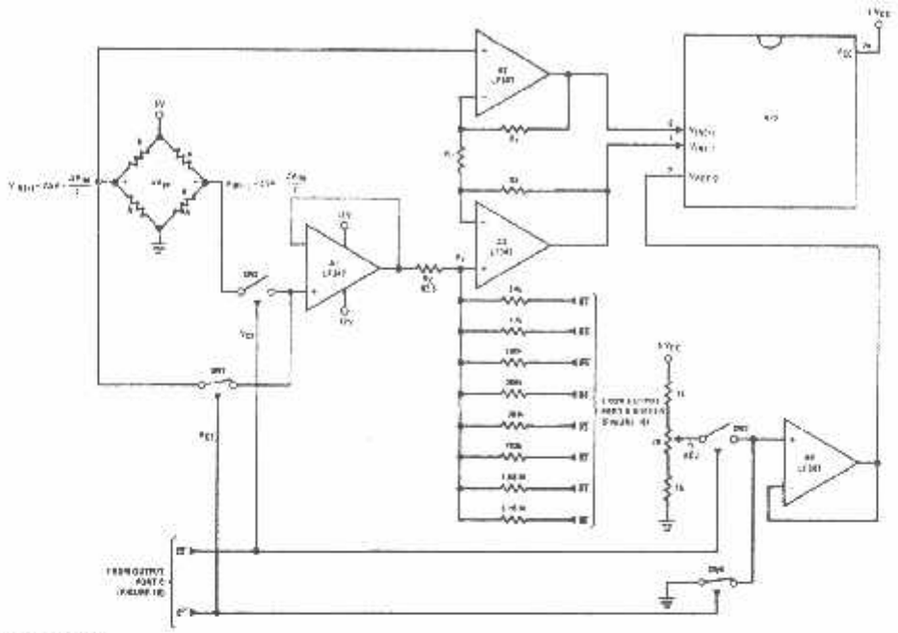
$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} + I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 18*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_X increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ± 12 mV with a resolution of 50 μV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.

Functional Description (Continued)

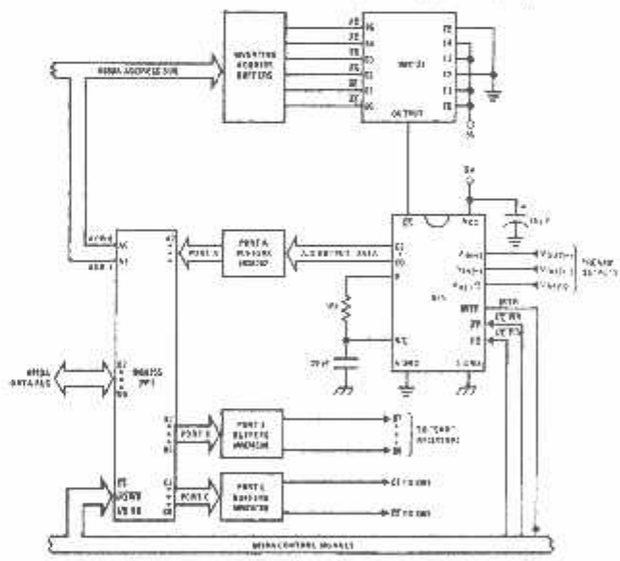


Note 1: R2 = 49.5 R1

Note 2: Switches are LMC13334 CMOS analog switches.

Note 3: The 9 resistors used in the auto-zero section can be ± 5% tolerance.

FIGURE 17. Gain of 100 Differential Transducer Preamp



TL/H/9811-21

FIGURE 18. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 19*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 20*. All addresses used are compatible with the SLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

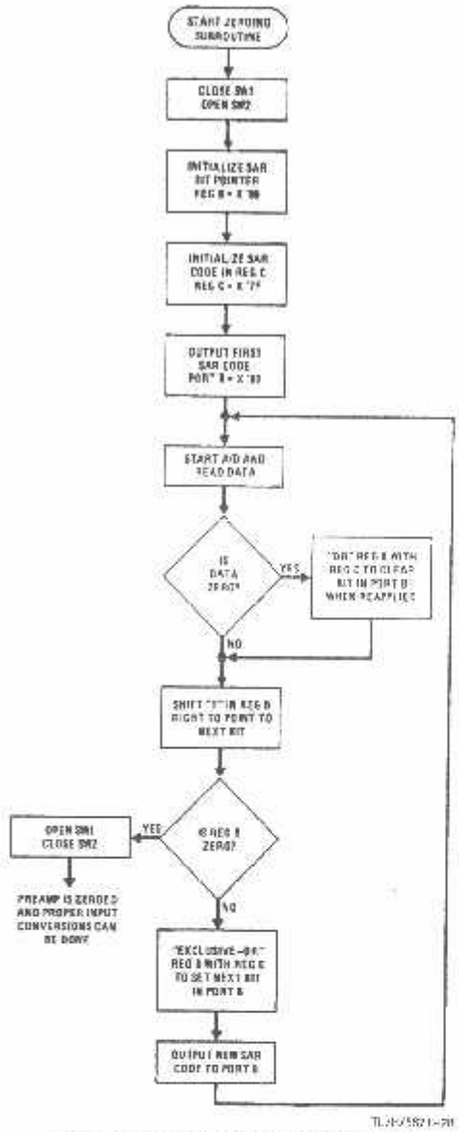
PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C30 upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 21* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose $\overline{INT}$ is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.



TL/H/5821-20

FIGURE 19. Flow Chart for Auto-Zero Routine

```
3D00  3E90      MVI 90
3D02  D337      Out Control Port              ;Program PPI
3D04  2601      MVI H 01          Auto-Zero Subroutine
3D06  7C        MOV A,H
3D07  D3E6      OUT C                        ;Close SW1 open SW2
3D09  0620      MVI B 80                     ;Initialize SAR bit pointer
3D0B  337F      MVI A 7F                     ;Initialize SAR code
3D0D  4F        MOV C,A           Return
3D0E  D3E5      OUT B                        ;Port B = SAR code
3D10  31AA3D    LXI SP 3DAA       Start      ;Dimension stack pointer
3D13  D3E4      OUT A                        ;Start A/D
3D15  FB        IE
3D16  00        NOP               Loop       ;Loop until INT asserted
3D17  C3163D    JMP Loop
3D1A  7A        MOV A,D           Auto-Zero
3D1B  C600      ADI 00
3D1D  CA2D3D    JZ Set C                     ;Test A/D output date for zero
3D20  78        MOV A,B           Shift B
3D21  F600      ORI 00                       ;Clear carry
3D23  1F        RAR                          ;Shift "1" in B right one place
3D24  FE00      CPI 00                       ;Is B zero? If yes last
3D26  CA373D    JZ Done                      ;approximation has been made
3D29  47        MOV B,A
3D2A  C3333D    JMP New C
3D2D  79        MOV A,C           Set C
3D2E  B0        ORA B                        ;Set bit in C that is in same
3D2F  4F        MOV C,A                      ;position as "1" in B
3D30  C3203D    JMP Shift B
3D33  A9        XRA C             New C      ;Clear bit in C that is in
3D34  C30D3D    JMP Return                   ;Same position as "1" in B
3D37  47        MOV B,A           Done       ;then output new SAR code.
3D38  79        MOV A,C                      ;Open SW1, close SW2 then
3D39  EE02      XRI 03                       ;proceed with program. Preamp
3D3B  D3E5      OUT C                        ;is now zeroed.
3D3D            *                 Normal
                *
                *
                Program for processing
                proper data values
3C3D  D3E4      IN A              Read A/D Subroutine  ;Read A/D data
3C3F  EEFF      XRI FF                       ;Invert data
3C41  57        MOV D,A
3C42  78        MOV A,B                      ;Is B Reg = 0? If not stay
3C43  E67F      ANI FF                       ;in auto zero subroutine
3C45  C21A3D    JNZ Auto-Zero
3C48  C3303D    JMP Normal
```

Note: All numerical values are hexadecimal representations.

FIGURE 20. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80® Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

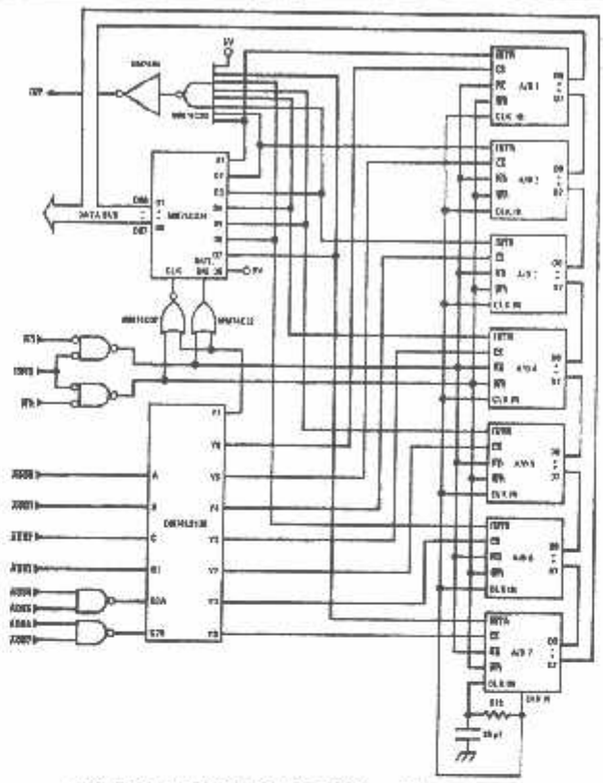
3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.



TL/H/5811-29

FIGURE 21. Multiple A/Ds with Z-80 Type Microprocessor

INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE	SOURCE STATEMENT		COMMENT
0038	E5		PUSH HL	;Save contents of all registers affected by
0039	C5		PUSH BC	;this subroutine.
003A	F5		PUSH AF	;Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL),X3E00	;Initialize memory pointer where data will be stored.
003E	0E 01		LD C, E01	;C register will be port ADDR of A/D converters.
0040	D300		OUT X00, A	;Load peripheral status word into 8-bit latch.
0042	DB00		IN A, X00	;Load status word into accumulator.
0044	47		LD B,A	;Save the status word.
0045	79	TEST	LD A,C	;Test to see if the status of all A/D's have
0046	FE 08		CP, X08	;been checked. If so, exit subroutine
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	;Test a single bit in status word by looking for
004C	1F		RRA	;a "1" to be rotated into the CARRY (an INT
004D	47		LD B,A	;is loaded as a "1"). If CARRY is not then load
004E	DA 5500		JPC, LOAD	;contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	;If CARRY is not set, increment C register to point
0052	C3 4500		JP,TEST	;to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	;Read data from interrupting A/D and invert
0057	EE FF		XOR FF	;the data.
0059	77		LD (HL),A	;Store the data
005A	2C		INC L	
005B	71		LD (HL),C	;Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP,NEXT	;Test next bit in status word.
0060	F1	DONE	POP AF	;Re-establish all registers as they were
0061	C1		POP BC	;before the interrupt.
0062	E1		POP HL	
0063	C9		RET	;Return to original program

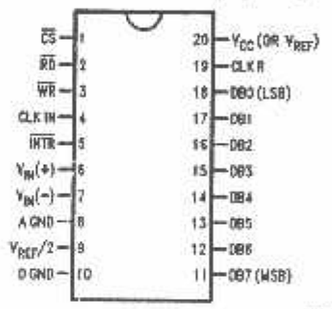
Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted				ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM	ADC0802LCV		ADC0802LCN
	±½ Bit Adjusted	ADC0803LCWM	ADC0803LCV		ADC0803LCN
	±1 Bit Unadjusted	ADC0804LCWM	ADC0804LCV	ADC0804LCN	ADC0805LCN
PACKAGE OUTLINE		M20B—Small Outline	V20A—Chip Carrier	N20A—Molded DIP	

TEMP RANGE		−40°C TO +85°C	−55°C TO +125°C
ERROR	±¼ Bit Adjusted	ADC0801LCJ	ADC0801LJ
	±½ Bit Unadjusted	ADC0802LCJ	ADC0802LJ, ADC0802LJ/883
	±½ Bit Adjusted	ADC0803LCJ	
	±1 Bit Unadjusted	ADC0804LCJ	
PACKAGE OUTLINE		J20A—Cavity DIP	J20A—Cavity DIP

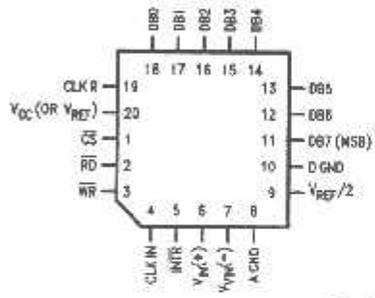
Connection Diagrams

ADC080X
Dual-In-Line and Small Outline (SO) Packages



TL/H/5871–3C

ADC080X
Molded Chip Carrier (PCC) Package



TL/H/5871–12

See Ordering Information

National Semiconductor

May 1999

DAC0808
8-Bit D/A Converter

General Description

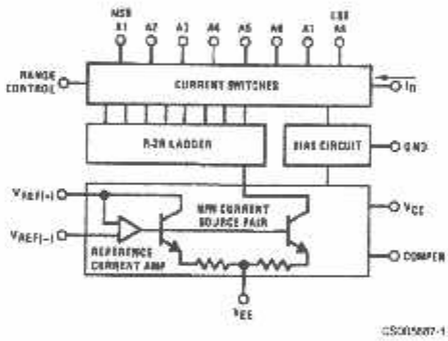
The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 µA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

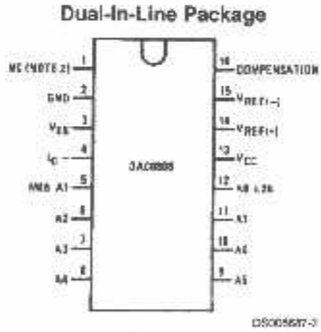
- Relative accuracy: ±0.19% error maximum
- Full scale current match: ±1 LSB typ
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/µs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

Block and Connection Diagrams



DS005687-1

Dual-In-Line Package

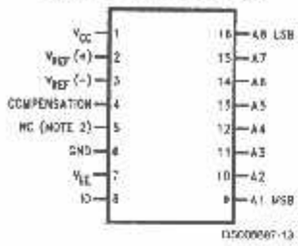


DS005687-2

Top View
Order Number DAC0808
See NS Package M16A or N16A

Block and Connection Diagrams (Continued)

Small-Outline Package



Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	N PACKAGE (N16A) (Note 1)		SO PACKAGE (M16A)
8-bit	$0°C \leq T_A \leq +75°C$	DAC0808LCN	MC1408P8	DAC0808LCM

Note 1: Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	+18 V_{DC}
V_{EE}	−18 V_{DC}
Digital Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Applied Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Note 4)	1000 mW
ESD Susceptibility (Note 5)	TBD
Storage Temperature Range	−65°C to −150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC0808	$0 \le T_A \le +75°C$

Electrical Characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, V_{REF}/R14 = 2 mA, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	(*Figure 4*)				%
	DAC0808LC (LM1408-8)				**±0.19**	%
	Settling Time to Within ½ LSB (Includes t_{PLH})	T_A=25°C (Note 7), (*Figure 5*)		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, (*Figure 5*)		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	(*Figure 3*)				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	(*Figure 3*)				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	(*Figure 3*)		−1	−3	µA
	Output Current Range	(*Figure 3*)				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω, (*Figure 3*)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	(*Figure 3*)		0	4	µA
	Output Voltage Compliance (Note 3)	$E_r \le 0.19\%$, T_A = 25°C				
	V_{EE}=−5V, I_{REF}=1 mA				−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}
SRI_{REF}	Reference Current Slew Rate	(*Figure 6*)	4	8		mA/µs
	Output Current Power Supply Sensitivity	$-5V \le V_{EE} \le -16.5V$		0.05	2.7	µA/V
	Power Supply Current (All Bits Low)	(*Figure 3*)				
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C, (*Figure 3*)				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					

Electrical Characteristics (Continued)

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, V_{REF}/R14 = 2 mA, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 3: Range control is not required.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{JMAX} = 125°C, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is 100°C/W. For the dual-in-line N package, this number increases to 175°C/W and for the small outline M package this number is 100°C/W.

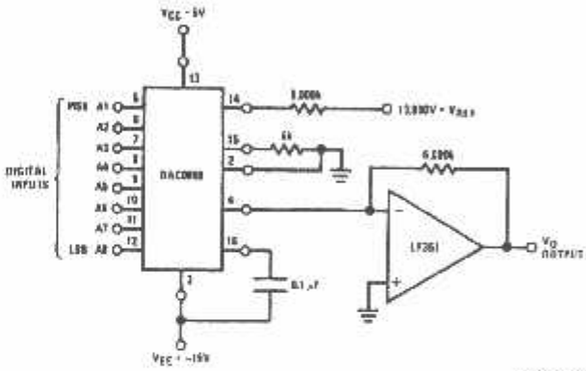
Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: All current switches are tested to guarantee at least 50% of rated current.

Note 7: All bits switched.

Note 8: Pin-out numbers for the DAL0808X represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.

Typical Application



$$V_O = 10V\left(\frac{A1}{2} + \frac{A2}{4} + \ldots \frac{A8}{256}\right)$$

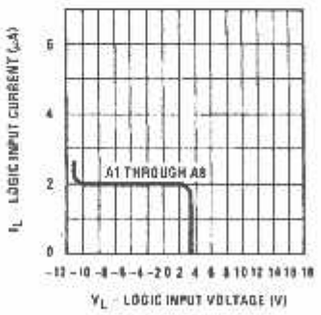
D5005687-23

D5005687-3

FIGURE 1. +10V Output Digital to Analog Converter (Note 8)

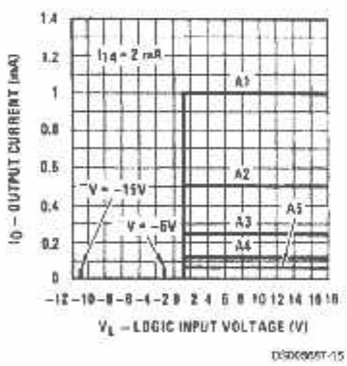
Typical Performance Characteristics V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted

Logic Input Current vs Input Voltage



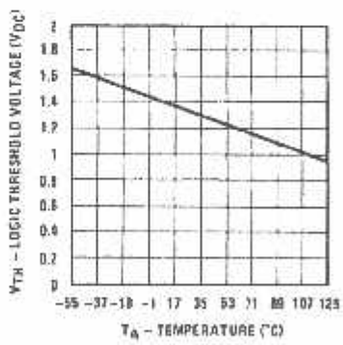
D5005687-14

Bit Transfer Characteristics



D5005687-15

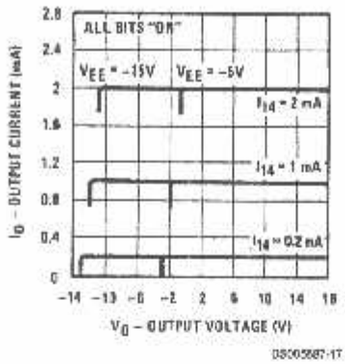
Logic Threshold Voltage vs Temperature



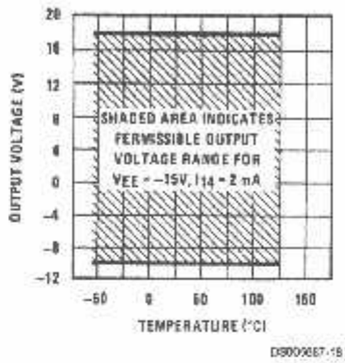
D5005687-16

Typical Performance Characteristics V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted (Continued)

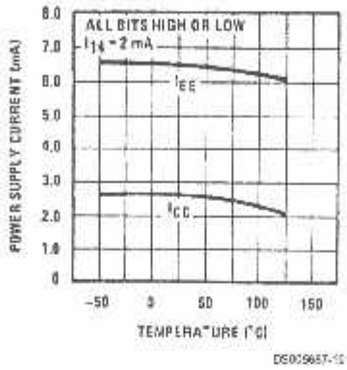
Output Current vs Output Voltage (Output Voltage Compliance)



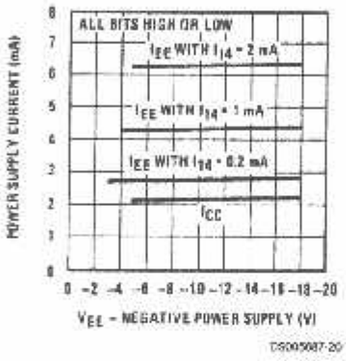
Output Voltage Compliance vs Temperature



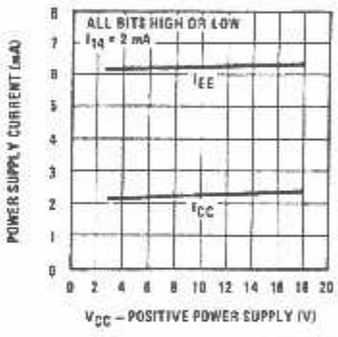
Typical Power Supply Current vs Temperature



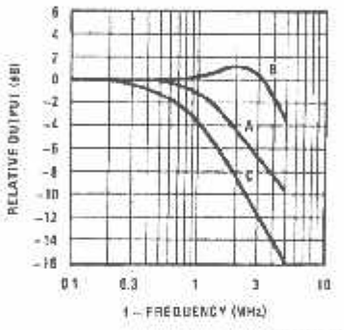
Typical Power Supply Current vs V_{EE}



Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}, R_L = 50Ω, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1V above ground.

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

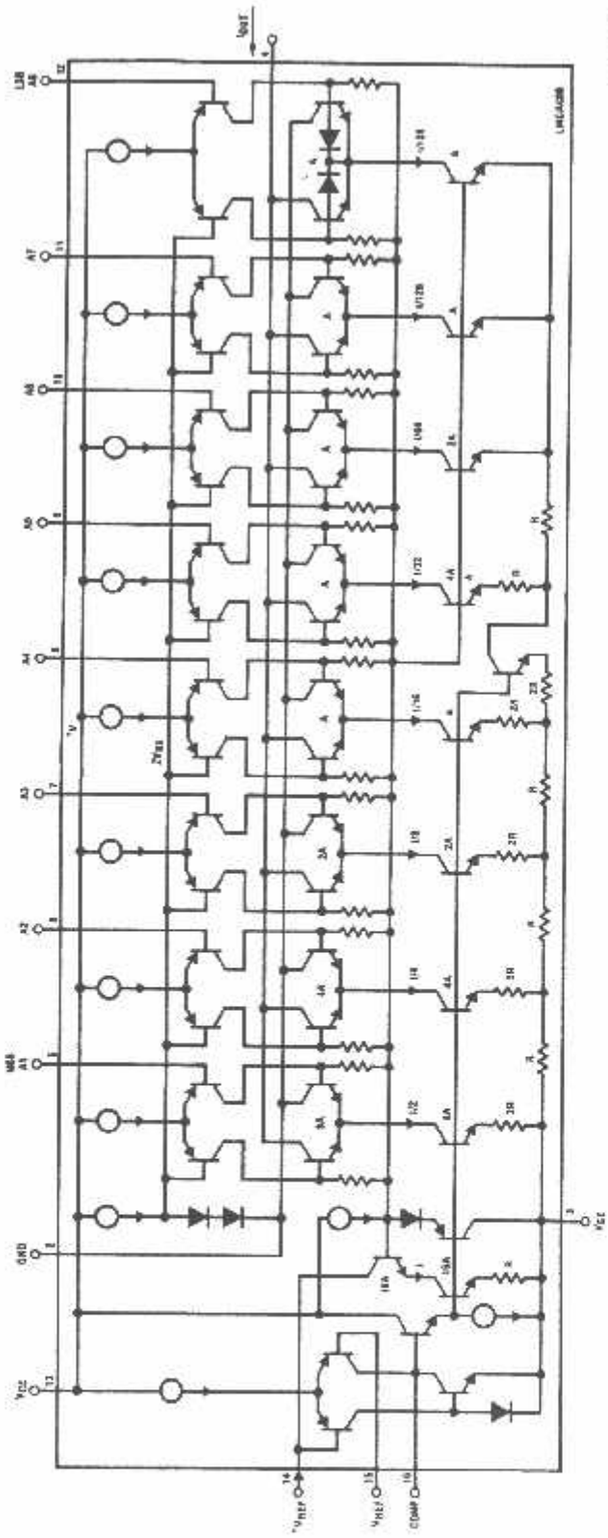
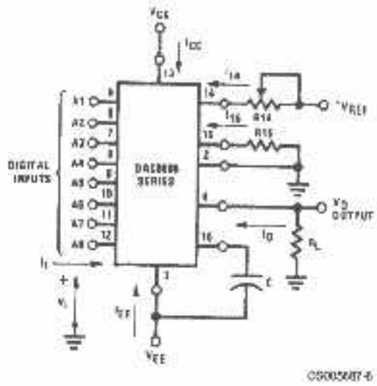


FIGURE 2. Equivalent Circuit of the DAC0808 Series (Note 6)

Test Circuits



V_I and I_I apply to inputs A1–A8.
The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right)$$

$$\text{where } K \simeq \frac{V_{REF}}{R14}$$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 3. Notation Definitions Test Circuit (Note 8)

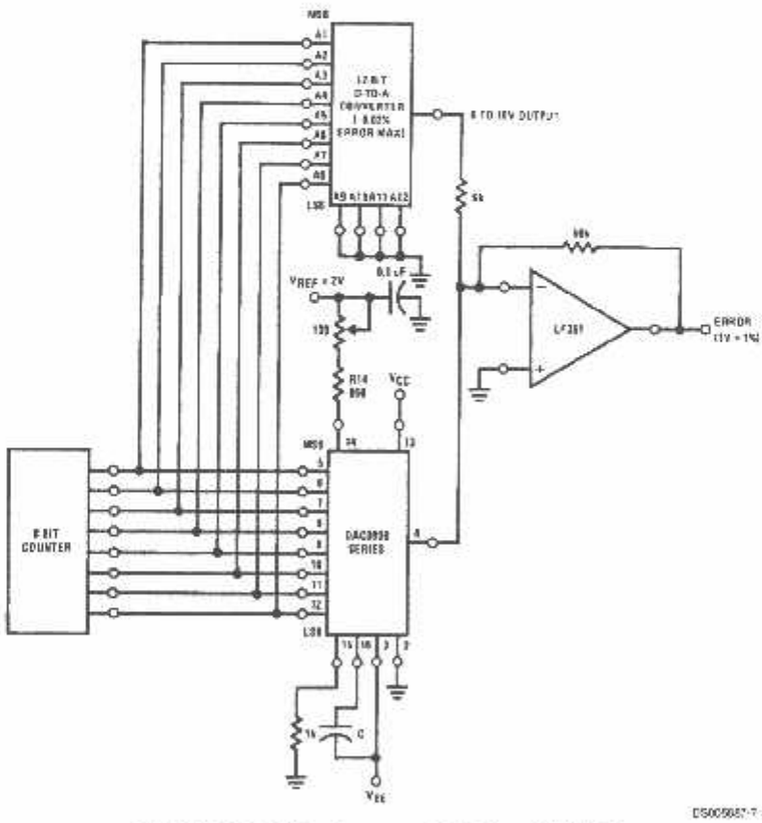


FIGURE 4. Relative Accuracy Test Circuit (Note 8)

Test Circuits (Continued)

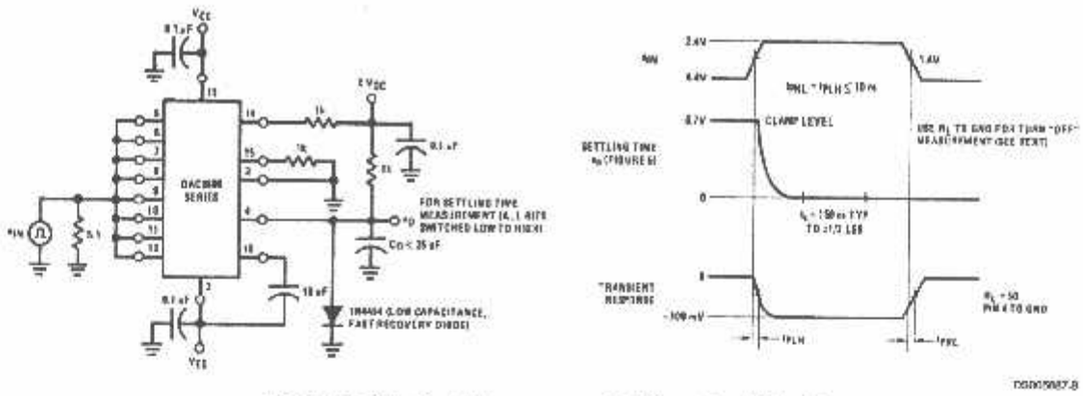


FIGURE 5. Transient Response and Settling Time (Note 8)

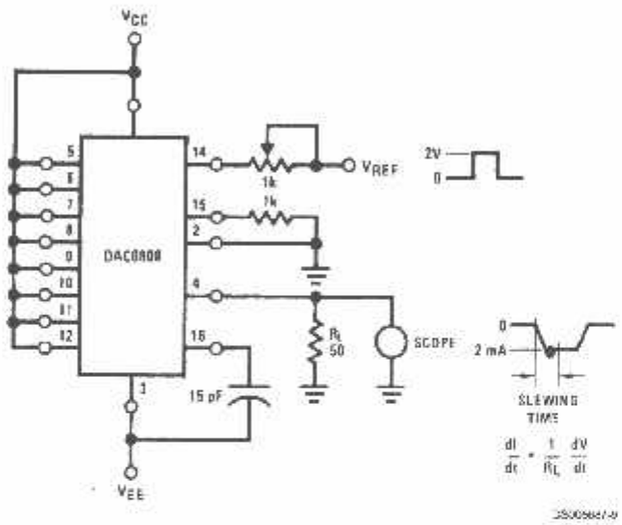


FIGURE 6. Reference Current Slew Rate Measurement (Note 8)

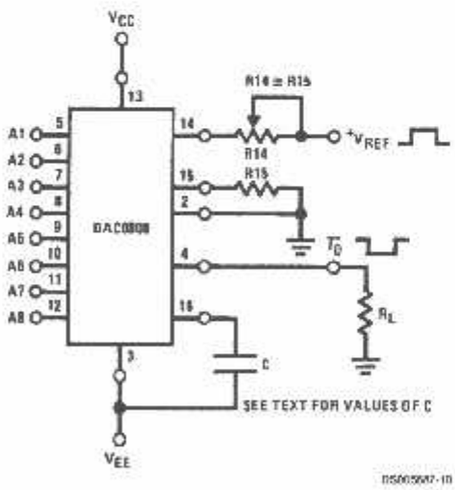


FIGURE 7. Positive V_{REF} (Note 8)

Test Circuits (Continued)

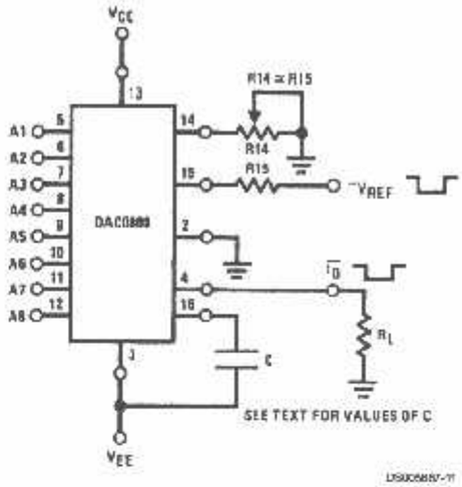


FIGURE 8. Negative V_{REF} (Note 8)

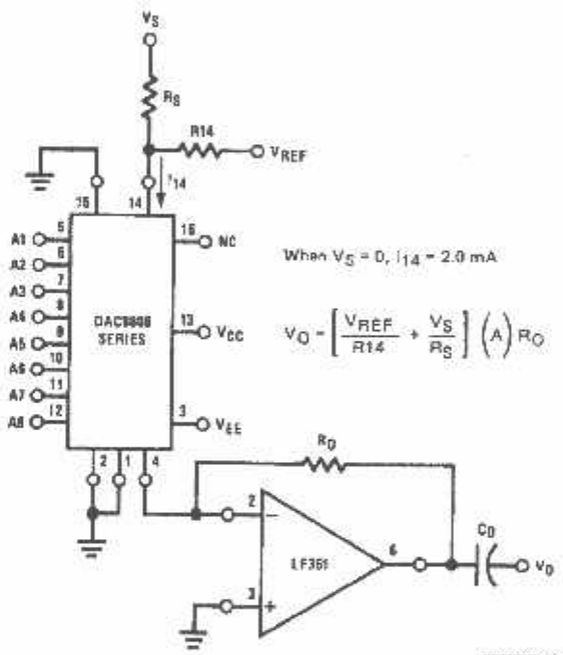


FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit (Note 8)

Application Hints

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 7*. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 8*. A high input impedance is the main

Application Hints (Continued)

advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 µF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.55 to 0.4V when V_{EE} = −5V due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to −5V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case settling time to 1.2 µs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −8V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±½ LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 µA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in *Figure 4*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±½ of one part in 65,536 or ±0.00076%, which is much more accurate than the ±0.019% specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 µA to 4 mA, the additional error contributions are less than 1.6 µA. This is well within 8-bit accuracy when referred to full-scale.

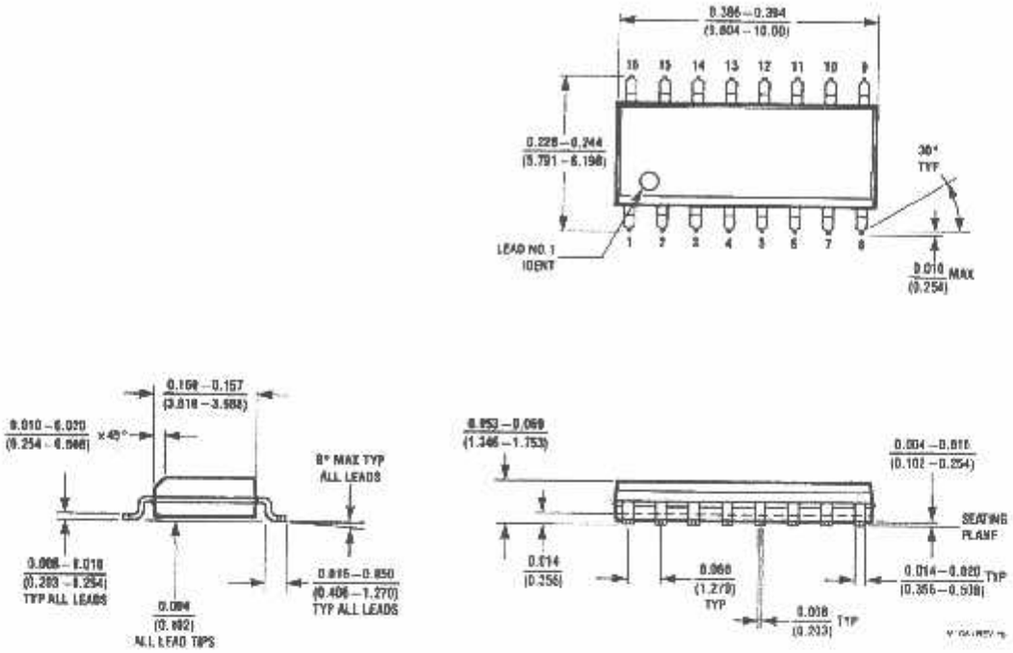
A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

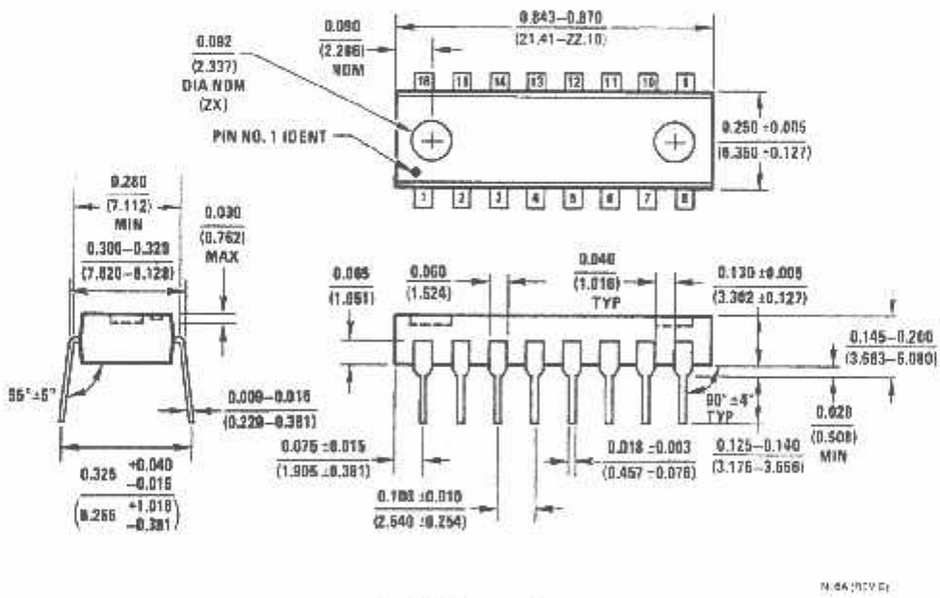
The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within ±½ LSB, for 8-bit accuracy, and 100 ns to ½ LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25$ pF.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 µF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

Physical Dimensions Inches (millimeters) unless otherwise noted



Small Outline Package
Order Number DAC0808LCM
NS Package Number M16A



Dual-In-Line Package
Order Number DAC0808
NS Package Number N16A

SGS-THOMSON MICROELECTRONICS

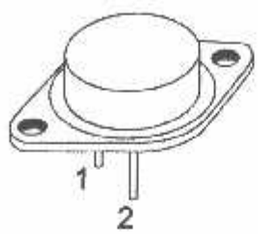
2N3055

SILICON NPN TRANSISTOR

- SGS-THOMSON PREFERRED SALESTYPE
- NPN TRANSISTOR

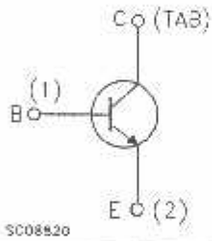
DESCRIPTION

The 2N3055 is a silicon epitaxial-base NPN transistor in Jedec TO-3 metal case. It is intended for power switching circuits, series and shunt regulators, output stages and high fidelity amplifiers.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	100	V
V_{CER}	Collector-Emitter Voltage (R_{BE} = 100Ω)	70	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	60	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	7	V
I_C	Collector Current	15	A
I_B	Base Current	7	A
P_{tot}	Total Dissipation at $T_c \leq 25$ °C	115	W
T_{stg}	Storage Temperature	-65 to 200	°C
T_j	Max. Operating Junction Temperature	200	°C

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.5	°C/W

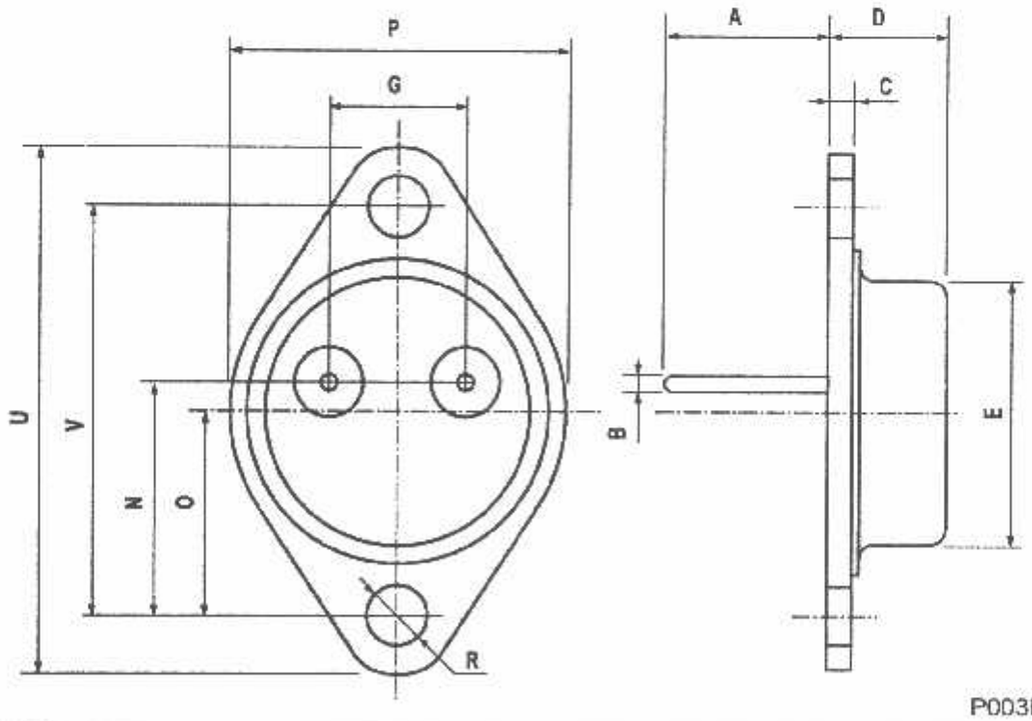
ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CEV}	Collector Cut-off Current (V_{BE} = -1.5V)	V_{CE} = 100 V V_{CE} = 100 V T_j = 150 °C			1 5	mA mA
I_{CEO}	Collector Cut-off Current (I_B = 0)	V_{CE} = 30 V			0.7	mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 7 V			5	mA
$V_{CEO(sus)}$*	Collector-Emitter Sustaining Voltage	I_C = 200 mA	60			V
$V_{CER(sus)}$*	Collector-Emitter Sustaining Voltage	I_C = 200 mA R_{BE} = 100 Ω	70			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 4 A I_B = 400 mA I_C = 10 A I_B = 3.3 A			1 3	V V
V_{BE}*	Base-Emitter Voltage	I_C = 4 A V_{CE} = 4 V			1.5	V
h_{FE}*	DC Current Gain	I_C = 0.5 A V_{CE} = 4 V Group 4 I_C = 0.5 A V_{CE} = 4 V Group 5 I_C = 0.5 A V_{CE} = 4 V Group 6 I_C = 0.5 A V_{CE} = 4 V Group 7 I_C = 4 A V_{CE} = 4 V I_C = 10 A V_{CE} = 4 V	20 35 60 120 20 5		50 75 145 250 70	
h_{FE1}/h_{FE1}*	DC Current Gain	I_C = 0.5 A V_{CE} = 4 V			1.6	
f_T	Transition frequency	I_C = 1 A V_{CE} = 4 V	2.5			MHz
$I_{s/b}$*	Second Breakdown Collector Current	V_{CE} = 40 V	2.87			A

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

TO-3 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.00		13.10	0.433		0.516
B	0.97		1.15	0.038		0.045
C	1.50		1.65	0.059		0.065
D	8.32		8.92	0.327		0.351
E	19.00		20.00	0.748		0.787
G	10.70		11.10	0.421		0.437
N	16.50		17.20	0.649		0.677
P	25.00		26.00	0.984		1.023
R	4.00		4.09	0.157		0.161
U	38.50		39.30	1.515		1.547
V	30.00		30.30	1.187		1.193



P003F

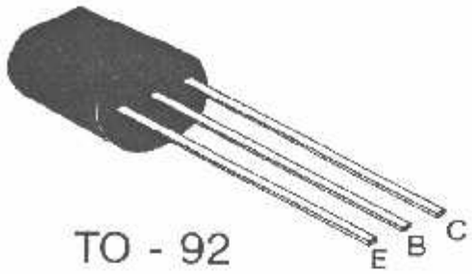
KT525-5
(9013)

NPN Epitaxial Silicon Transistor

revised October 1999

1W OUTPUT AMPLIFIER OF PORTABLE RADIOS IN CLASS B PUSH-PULL OPERATION

- High total power dissipation (PT=625mW)
- High Collector Current (I_C =500mA)
- Excellent h_{FE} linearity.



TO - 92

CLASSIFICATION h_{FE} (1)

Classification	D	E	F	G	H
h_{FE} (1)	64-91	78-112	96-135	112-166	144-202

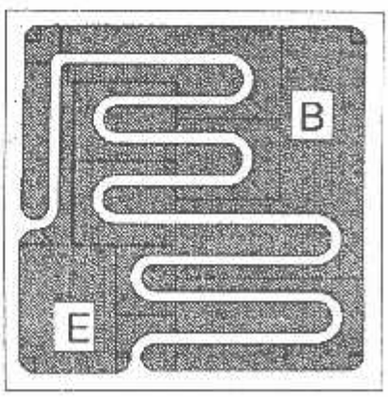
Absolute Maximum Ratings (Ta=25°C)

Symbol	Parameter	Rating	Units
V_{CBO}	Collector-Base Voltage	40	V
V_{CEO}	Collector-Emitter Voltage	20	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current	500	mA
P_C	Collector Dissipation	625	mW
T_j	Junction Temperature	150	°C
Tstg	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics (T_a = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C =100μA, I_E =0	40			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C =1mA, I_B =0	20			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E =100μA, I_C =0	5			V
I_{CBO}	Collector Cutoff Current	V_{CB}=25V, I_E =0			100	nA
I_{EBO}	Emitter Cutoff Current	V_{EB}=3V, I_C =0			100	nA
$h_{FE}1$	DC Current Gain	V_{CE}=1V, I_C =50mA	64	120	202	
$h_{FE}2$		V_{CE}=1V, I_C =500mA	40	120		
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C =500mA, I_B =50mA		0.16	0.6	V
V_{BE}(sat)	Base-Emitter Saturation Voltage	I_C =500mA, I_B =50mA		0.91	1.2	V
$V_{BE(on)}$	Base-Emitter On Voltage	V_{CE}=1V, I_C =10mA	0.6	0.67	0.7	V

Pad Location



- DIE SIZE 495 X 495μm
- DIE THICKNESS Typ. 470 μm

- BONDING PAD SIZE
  Emitter 85 x 114 μm
  Base 85 x 154 μm

FAIRCHILD
SEMICONDUCTOR™

TIP31 Series(TIP31/31A/31B/31C)

Medium Power Linear Switching Applications

- Complementary to TIP32/32A/32B/32C

1 TO-220

1.Base 2.Collector 3.Emitter

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_C=25°C unless otherwise noted

Symbol	Parameter		Value	Units
V_{CBO}	Collector-Base Voltage	: TIP31	40	V
		: TIP31A	60	V
		: TIP31B	80	V
		: TIP31C	100	V
V_{CEO}	Collector-Emitter Voltage	: TIP31	40	V
		: TIP31A	60	V
		: TIP31B	80	V
		: TIP31C	100	V
V_{EBO}	Emitter-Base Voltage		5	V
I_C	Collector Current (DC)		3	A
I_{CP}	Collector Current (Pulse)		5	A
I_B	Base Current		1	A
P_C	Collector Dissipation (T_C=25°C)		40	W
P_C	Collector Dissipation (T_a=25°C)		2	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		- 65 ~ 150	°C

Electrical Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
V_{CEO}(sus)	* Collector-Emitter Sustaining Voltage				
	: TIP31	I_C = 30mA, I_B = 0	40		V
	: TIP31A		60		V
	: TIP31B		80		V
	: TIP31C		100		V
I_{CEO}	Collector Cut-off Current				
	: TIP31/31A	V_{CE} = 30V, I_B = 0		0.3	mA
	: TIP31B/31C	V_{CE} = 60V, I_B = 0		0.3	mA
I_{CES}	Collector Cut-off Current				
	: TIP31	V_{CE} = 40V, V_{EB} = 0		200	μA
	: TIP31A	V_{CE} = 60V, V_{EB} = 0		200	μA
	: TIP31B	V_{CE} = 80V, V_{EB} = 0		200	μA
	: TIP31C	V_{CE} = 100V, V_{EB} = 0		200	μA
I_{EBO}	Emitter Cut-off Current	V_{EB} = 5V, I_C = 0		1	mA
h_{FE}	* DC Current Gain	V_{CE} = 4V, I_C = 1A	25		
		V_{CE} = 4V, I_C = 3A	10	50	
V_{CE}(sat)	* Collector-Emitter Saturation Voltage	I_C = 3A, I_B = 375mA		1.2	V
V_{BE}(sat)	* Base-Emitter Saturation Voltage	V_{CE} = 4V, I_C = 3A		1.8	V
f_T	Current Gain Bandwidth Product	V_{CE} = 10V, I_C = 500mA	3.0		MHz

* Pulse Test: PW≤300μs, Duty Cycle≤2%

Typical Characteristics

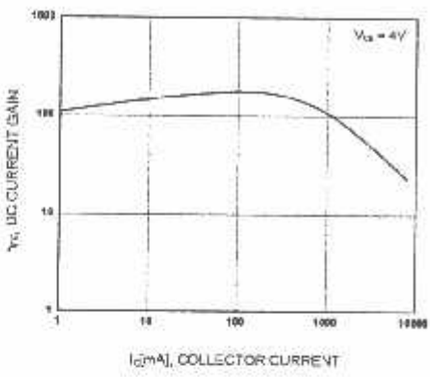


Figure 1. DC current Gain

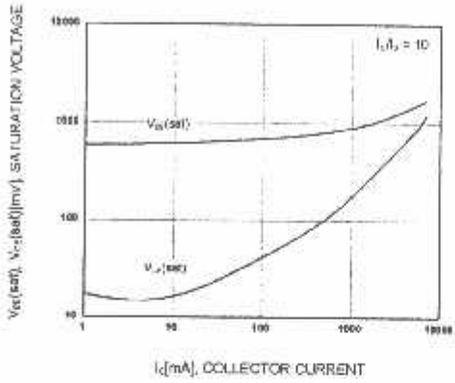


Figure 2. Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage

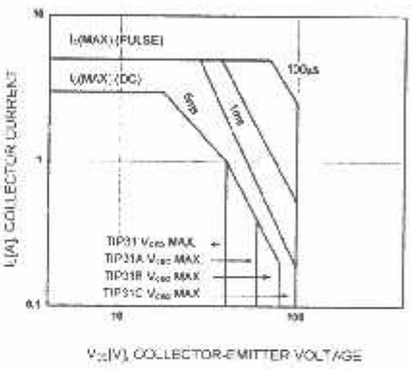


Figure 3. Safe Operating Area

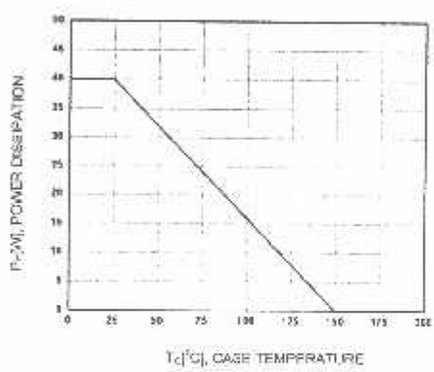
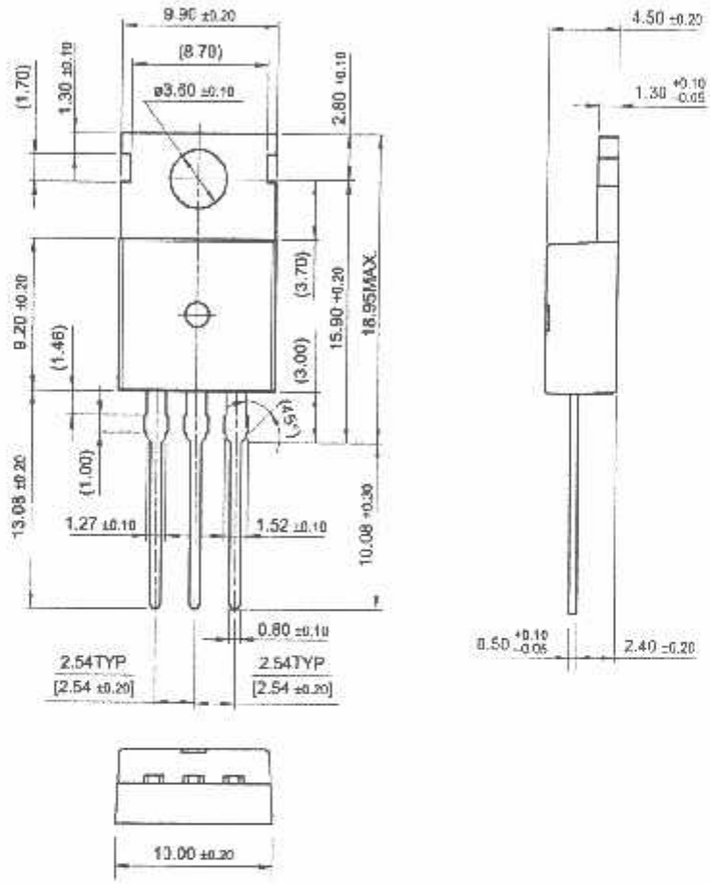


Figure 4. Power Derating

Package Demensions

TO-220



Dimensions in Millimeters

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Bottomless™
CoolFET™
CROSSVOLT™
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FACT™
FACT Quiet Series™
FAST®
FASTr™
GTO™
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ISOPLANAR™
MICROWIRE™
POP™
PowerTrench®
QFET™
QS™
Quiet Series™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TinyLogic™
UHC™
VCX™

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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Section 1. Fundamentals of DDS Technology

Overview

Direct digital synthesis (DDS) is a technique for using digital data processing blocks as a means to generate a frequency- and phase-tunable output signal referenced to a fixed-frequency precision clock source. In essence, the reference clock frequency is "divided down" in a DDS architecture by the scaling factor set forth in a programmable binary tuning word. The tuning word is typically 24-48 bits long which enables a DDS implementation to provide superior output frequency tuning resolution.

Today's cost-competitive, high-performance, functionally-integrated, and small package-sized DDS products are fast becoming an alternative to traditional frequency-agile analog synthesizer solutions. The integration of a high-speed, high-performance, D/A converter and DDS architecture onto a single chip (forming what is commonly known as a *Complete-DDS* solution) enabled this technology to target a wider range of applications and provide, in many cases, an attractive alternative to analog based PLL synthesizers. For many applications, the DDS solution holds some distinct advantages over the equivalent agile analog frequency synthesizer employing PLL circuitry.

DDS advantages:

- Micro-Hertz tuning resolution of the output frequency and sub-degree phase tuning capability, all under complete digital control.
- Extremely fast "hopping speed" in tuning output frequency (or phase), phase-continuous frequency hops with no over/undershoot or analog-related loop settling time anomalies.
- The DDS digital architecture eliminates the need for the manual system tuning and tweaking associated with component aging and temperature drift in analog synthesizer solutions.
- The digital control interface of the DDS architecture facilitates an environment where systems can be remotely controlled, and minutely optimized, under processor control.
- When utilized as a quadrature synthesizer, DDS afford unparalleled matching and control of I and Q synthesized outputs.

Theory of Operation

In its simplest form, a direct digital synthesizer can be implemented from a precision reference clock, an address counter, a programmable read only memory (PROM), and a D/A converter (see Figure 1-1).

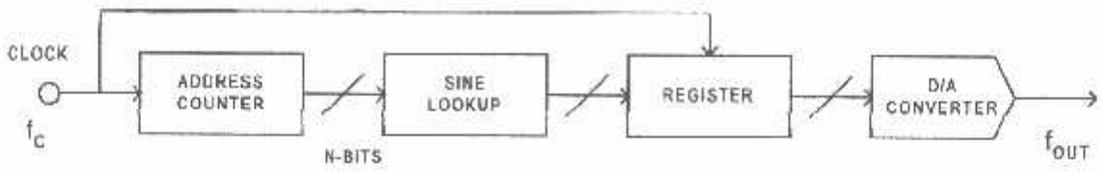


Figure 1-1. Simple Direct Digital Synthesizer

In this case, the digital amplitude information that corresponds to a complete cycle of a sinewave is stored in the PROM. The PROM is therefore functioning as a sine lookup table. The address counter steps through and accesses each of the PROM's memory locations and the contents (the equivalent sine amplitude words) are presented to a high-speed D/A converter. The D/A converter generates an analog sinewave in response to the digital input words from the PROM. The output frequency of this DDS implementation is dependent on 1.) the frequency of the reference clock, and 2.) the sinewave step size that is programmed into the PROM. While the analog output fidelity, jitter, and AC performance of this simplistic architecture can be quite good, it lacks tuning flexibility. The output frequency can only be changed by changing the frequency of the reference clock or by reprogramming the PROM. Neither of these options support high-speed output frequency hopping.

With the introduction of a phase accumulator function into the digital signal chain, this architecture becomes a numerically-controlled oscillator which is the core of a highly-flexible DDS device. As figure 1-2 shows, an N-bit variable-modulus counter and phase

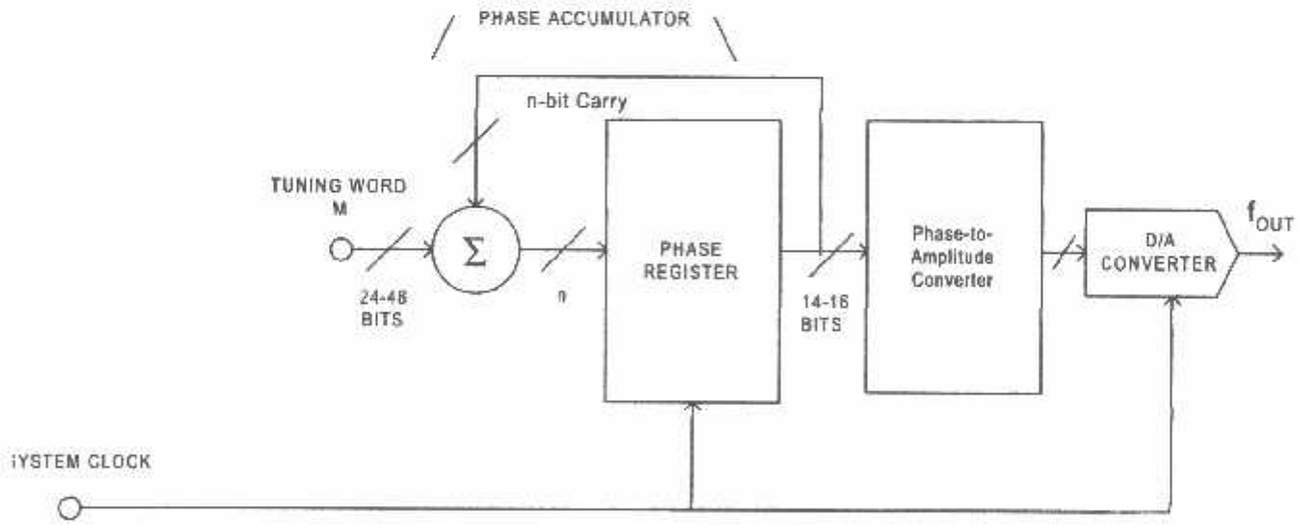
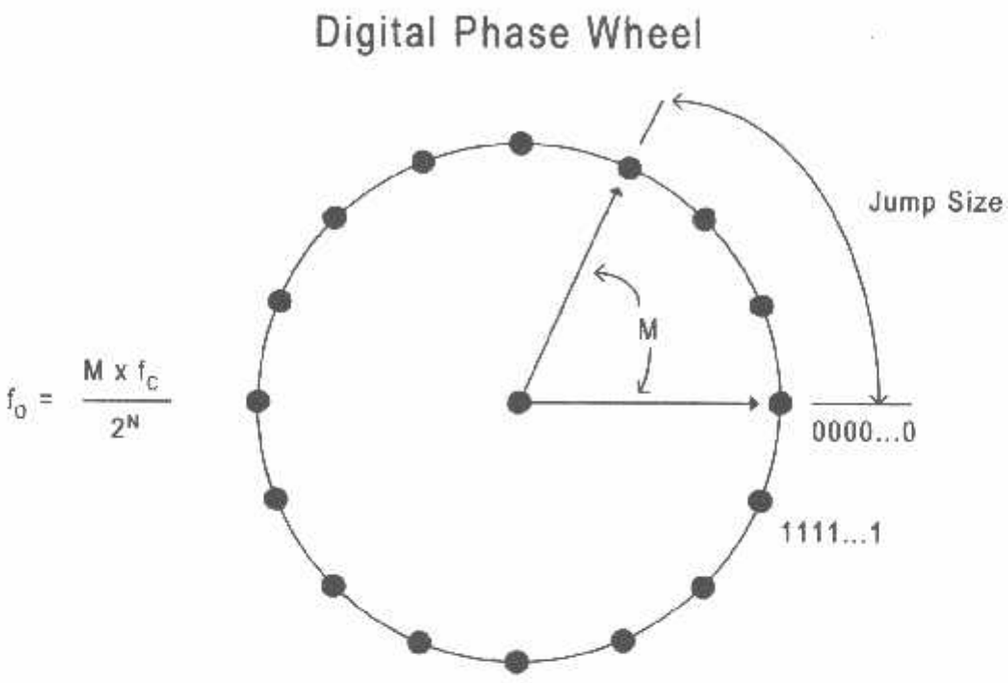


Figure 1-2. Frequency-tunable DDS System

register are implemented in the circuit before the sine lookup table, as a replacement for the address counter. The carry function allows this function as a "phase wheel" in the DDS architecture. To understand this basic function, visualize the sinewave oscillation as a vector

rotating around a phase circle (see Figure 1-3). Each designated point on the phase wheel corresponds to the equivalent point on a



n	NUMBER OF POINTS
8	256
12	4096
16	65535
20	1048576
24	16777216
28	268435456
32	4294967296
48	281474976710656

Figure 1-3. Digital Phase Wheel

cycle of a sine waveform. As the vector rotates around the wheel, visualize that a corresponding output sinewave is being generated. One revolution of the vector around the phase wheel, at a constant speed, results in one complete cycle of the output sinewave. The phase accumulator is utilized to provide the equivalent of the vector's linear rotation around the phase wheel. The contents of the phase accumulator correspond to the points on the cycle of the output sinewave. The number of discrete phase points contained in the "wheel" is determined by the resolution, N, of the phase accumulator. The output of the phase accumulator is linear and cannot directly be

used to generate a sinewave or any other waveform except a ramp. Therefore, a phase-to-amplitude lookup table is used to convert a truncated version of the phase accumulator's instantaneous output value into the sinewave amplitude information that is presented to the D/A converter. Most DDS architectures exploit the symmetrical nature of a sinewave and utilize mapping logic to synthesize a complete sinewave cycle from ¼ cycle of data from the phase accumulator. The phase-to-amplitude lookup table generates all the necessary data by reading forward then back through the lookup table.

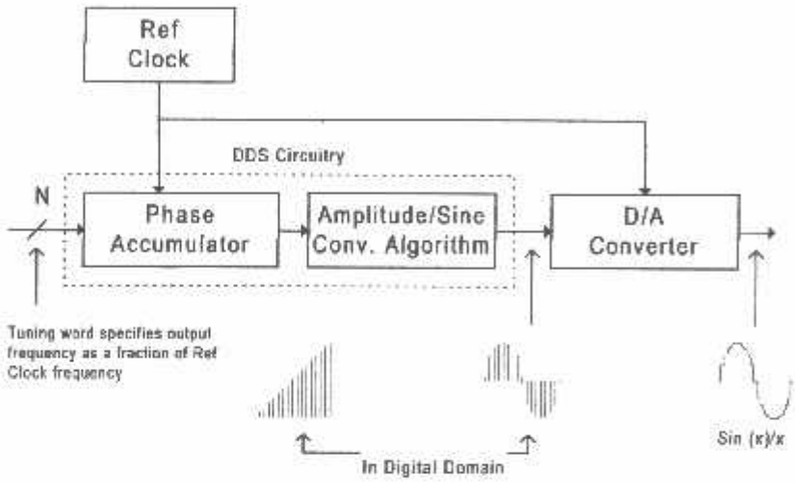


Figure 1-4. Signal flow through the DDS architecture

The phase accumulator is actually a modulus M counter that increments its stored number each time it receives a clock pulse. The magnitude of the increment is determined by a digital word M contained in a "delta phase register" that is summed with the overflow of the counter. The word in the delta phase register forms the phase step size between reference clock updates; it effectively sets how many points to skip around the phase wheel. The larger the jump size, the faster the phase accumulator overflows and completes its equivalent of a sinewave cycle. For a N=32-bit phase accumulator, an M value of 0000...0001(one) would result in the phase accumulator overflowing after 2^{32} reference clock cycles (increments). If the M value is changed to 0111...1111, the phase accumulator will overflow after only 2^{1} clock cycles, or two reference clock cycles. This control of the jump size constitutes the frequency tuning resolution of the DDS architecture.

The relationship of the phase accumulator and delta phase accumulator form the basic tuning equation for DDS architecture:

$$F_{OUT} = (M\ (REFCLK))\ /2^{N}$$

Where: F_{OUT} = the output frequency of the DDS
M = the binary tuning word
REFCLK = the internal reference clock frequency (system clock)
N = The length in bits of the phase accumulator

Changes to the value of M in the DDS architecture result in immediate and phase-continuous changes in the output frequency. In practical application, the M value, or frequency tuning word, is loaded into an internal serial or byte-loaded register which precedes the parallel-output delta phase register. This is generally done to minimize the package pin count of the DDS device. Once the buffer register is loaded, the parallel-output delta phase register is clocked and the DDS output frequency changes. Generally, the only speed limitation to changing the output frequency of a DDS is the maximum rate at which the buffer register can be loaded and executed. Obviously, a parallel byte load control interface enhances frequency hopping capability.

Trends in Functional Integration

One of the advantages to the digital nature of DDS architecture is that digital functional blocks can readily be added to the core blocks to enhance the capability and feature set of a given device. For general purpose use, a DDS device will include an integrated D/A converter function to provide an analog output signal. This "complete-DDS" approach greatly enhances the overall usefulness and "user-friendliness" associated with the basic DDS devices. DDS devices are readily available with integrated 10-bit D/A converters supporting internal REFCLK speeds to 180 MHz. The present state of the art for a complete-DDS solution is at 300 MHz clock speeds with an integrated 12-bit D/A converter.

Along with the integrated D/A converter, DDS solutions normally contain additional digital blocks that perform various operations on the signal path. These blocks provide a higher level of functionality in the DDS solution and provide an expanded set of user-controlled features. The block diagram of an expanded-feature DDS device is shown in Figure 1-5.

The individual functional blocks are described below:

- (A) A programmable REFCLK Multiplier function include at the clock input, multiplies the frequency of the external reference clock, thereby reducing the speed requirement on the precision reference clock. The REFCLK Multiplier function also enhances the ability of the DDS device to utilize available system clock sources.

- (B) The addition of an adder after the phase accumulator enables the output sinewave to be phase-delayed in correspondence with a phase tuning word. The length of the adder circuit determines the number of bits in the phase tuning word, and therefore, the resolution of the delay. In this architecture, the phase tuning word is 14-bits.

- (C) An Inverse SINC block inserted before the D/A converter compensates for the SIN(X)/X response of the quantized D/A converter output, and thereby provides a constant amplitude output over the Nyquist range of the DDS device

- (D) A digital multiplier inserted between the Sine look-up table and the D/A converter enables amplitude modulation of the output sinewave. The width of the digital multiplier word determines the resolution of the output amplitude step size.