INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

SKRIPSI

PERANCANGAN DAN PEMBUATAN ALAT PENGISIAN DAN PENGEPRESAN GULA PASIR DALAM KEMASAN SECARA OTOMATIS DENGAN MENGGUNAKAN MIKROKONTROLLER AT89S8252

Disusun Oleh :
ADY KRISTIANTO
00. 17. 184

MARET 2006

LEMBAR PERSETUJUAN

PERANCANGAN DAN PEMBUATAN ALAT PENGISIAN DAN PENGEPRESAN GULA PASIR DALAM KEMASAN SECARA OTOMATIS DENGAN MENGGUNAKAN MIKROKONTROLLER AT89S8252

SKRIPSI

Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektro Konsentrasi Teknik Elektronika

Disusun Oleh :

ADY KRISTIANTO

00.17.184

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Judul Skripsi	: *Perancangan Dan Pembuatan Alat Pengisian Dan Pengepresan Gula Pasir Dalam Kemasan Secara Otomatis Dengan Menggunakan Mikrokontroller AT89S8252*

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Hari	: Kamis
Tanggal	: 26 Maret 2006
Dengan Nilai	: 78,25 (B+)

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ABSTRAKSI

PERANCANGAN DAN PEMBUATAN ALAT PENGISIAN DAN PENGEPRESAN GULA PASIR DALAM KEMASAN SECARA OTOMATIS DENGAN MENGGUNAKAN MIKROKONTROLLER AT89S8252

(Ady Kristianto, 00.17.184, Jurusan Teknik Elektro S-1/Elektronika)

(Dosen Pembimbing : Ir. Eko Nurcahyo)

Kata Kunci : Mikrokontroller AT89S8252, Sensor Berat, Motor dc *pres*, Sensor *Infra red*, Motor dc *konveyor* dan Sistem timbangan digital

Alat ini dirancang dan dibuat dengan tujuan untuk mempermudah pekerjaan manusia khususnya pedagang dan indusri kecil dalam melakukan penimbangan dan pengepresan (pengepakan) gula pasir dalam kemasan secara otomatis.

Pada perancangan alat ini, Mikrokontroller AT89S8252 merupakan basis kontrolnya. Alat yang dibuat meliputi perancangan perangkat keras dan perangkat lunak. Perancangan perangkat keras meliputi perancangan rangkaian keypad, perancangan rangkaian sensor berat, perancangan ADC0804, perancangan rangkaian LCD, perancangan driver motor DC, perancangan rangkaian sensor , dan perancangan minimum sistem AT89S8252. Perancangan perangkat lunak berupa *flow chart* cara kerja alat. Setting keypad merupakan langkah awal dari sistem kerja alat ini. Sensor berat berfungsi sebagai penimbang berat gula pasir yang telah disetting, membandingkan berat setting dengan berat aksi pada alat adalah proses kerja alat control. setelah proses ini konveyor bergerak membawa gula dalam plastik kemasan menuju proses pengepresan untuk menutup kemasan plastik.

Adapun spesifikasi alat adalah sebagai berikut :

Dimensi Alat

Panjang	: 120 cm
Lebar	: 50 cm
Tinggi	: 80 cm

KATA PENGANTAR

Puji syukur dipanjatkan kehadirat Allah SWT karena berkat limpahan rahmat dan hidayah-Nya penyusun dapat menyelesaikan skripsi ini dengan baik. Skripsi ini berjudul "***Perancangan Dan Pembuatan Alat Pengisian Dan Pengepresan Gula Pasir Dalam Kemasan Secara Otomatis Dengan Menggunakan Mikrokontroller At89s8252***".

Skripsi ini merupakan suatu persyaratan akademis untuk menyelesaikan studi strata-1 (S_1), jurusan Teknik Elektro Konsentrasi Teknik Elektronika pada Fakultas Teknologi Industri, Institut Teknologi Nasional Malang.

Disadari bahwa skripsi ini dapat terselesaikan dengan baik karena adanya bantuan dari berbagai pihak. Oleh karena itu, pada kesempatan ini penyusun mengucapkan terima kasih kepada :

1. Dr. Ir. Abraham Lomi, MSEE, selaku Rektor ITN Malang.
2. Ir. Mochtar Asroni, MSME, selaku Dekan Fakultas Teknologi Industri ITN Malang.
3. Ir. F. Yudi Limpraptono, MT, selaku Ketua Jurusan Teknik Elektronika.
4. Ir. Eko Nurcahyo, selaku Dosen pembimbing.
5. Keluargaku tercinta dan teman-temanku, yang selalu memberikan doa dan dorongannya baik moril maupun spirituil..
6. Semua pihak yang telah ikut membantu terselesaikannya skripsi ini.

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Berkembangnya ilmu pengetahuan dan teknologi diberbagai bidang telah menjadikan pekerjaan manusia menjadi sangat mudah. Hal ini disebabkan karena sesuatu yang dulu dikerjakan secara manual sekarang dikerjakan secara otomatis. Hal tersebut dipicu oleh perkembangan teknologi khususnya kemajuan teknologi dibidang IC menghasilkan chip mikrokontroller yang makin kecil dan memungkinkan untuk merancang peralatan baru dalam bidang pengontrolan. Keadaan itu sangat memungkinkan membantu bentuk – bentuk kegiatan otomatisasi dibidang industri baik itu industri kecil maupun industri berskala besar. Namun tidak menutup kemungkinan masih banyak kegiatan industri yang belum mepergunakan alat – alat kontrol dalam melakukan pekerjaannya. Hal tersebut bisa saja terjadi karena mungkin ada anggapan bahwa sesuatu yang bersifat otomatis itu mahal harganya. Padahal jika mau mempertimbangkan lagi manfaat yang didapat dari kehadiran alat – alat tersebut sangat membantu tentu akan lain keadaannya. Pada suatu usaha dagang yang dilakukan oleh sebagian besar masyarakat pedagang disekitar kita yang menjual gula dengan ukuran berat tertentu pada proses pengisian dan penimbangannya masih menggunakan cara konvensional yaitu dengan mengambil dari karung gula kemasan besar kemudian diisikan dan ditimbang ulang kedalam plastik kemasan sampai mencapai ukuran yang diinginkan. Dengan menggunakan cara konvensional ini ukuran gula

kemasan yang diinginkan kadang tidak sesuai dengan berat yang diinginkan disebahkan oleh beberapa faktor antara lain: karena kelalaian manusia dan alat penimbang yang kurang valid. Dari keadaan diatas penyusun akan mencoba untuk mengangkat judul "***Perancangan Dan Pembuatan Alat Pengisian Dan Pengepresan Gula Pasir Dalam Kemasan Secara Otomatis Dengan Menggunakan Mikrokontroller AT89S8252*** " yang nantinya diharapkan bisa menggantikan proses pengisian dan pengepakan gula pasir dalam plastik kemasan secara manual dilingkungan masyarakat maupun industri kecil.

1.2. Tujuan

Tujuan dari penulisan skripsi ini adalah untuk mengetahui fungsi dari mikrokontroller sebagai pengontrol alat pengisi dan pengepres gula dalam plastik kemasan dengan menggunakan mikrokontroller AT89S8252.

1.3. Rumusan Masalah

Rumusan masalah yang diangkat dalam penyusunan skripsi ini adalah :

- Bagaimana merencanakan dan membuat alat pengisi dan pengepres gula pasir dalam kemasan .
- Bagaimana merencanakan dan membuat rangkaian pengontrol mesin pengisi gula dan pengepresannya..
- Bagaimana membuat instalasi hardware dan software dengan menggunakan mikrokontroller AT89S8252 yang berfungsi sebagai pengontrol alat pengisi dan pengepres.

1.4. Batasan Masalah

Sehubungan dengan masalah yang dihadapi dalam pembuatan skripsi ini, permasalahan hanya dibatasi dengan tujuan untuk mencegah kemungkinan meluasnya masalah dan menyimpang dari permasalahan . Pembatasan tersebut antara lain :

- Menggunakan Software dan Hardware pendukung AT89S8252.
- Dalam rangkaian ini catu daya dianggap konstan dan tidak akan dibahas.
- Tidak membahas secara mendetail kontruksi mekanik mesin berserta motor penggeraknya (motor dc).
- Hanya menimbang gula dengan batasan berat 1000gr dan 1500gr.
- Alat yang dibuat dalam bentuk simulasi.

1.5. Metodologi Penulisan

Metode yang digunakan dalam penulisan skripsi ini adalah :

1. Studi Pustaka

   Memperoleh data dengan cara membaca dan mempelajari buku *literatur* yang ada hubungannya dengan penyusunan skripsi ini.

2. Studi Lapangan

   Memperoleh data dengan cara praktek langsung dalam perencanaan dan pembuatan alat.

3. Pengolahan Data

   Mengolah data dengan jalan membuat analisa dan menarik kesimpulan dari hasil pengujian data yang ada.

1.6. Sistematika Penulisan

Pada penulisan laporan skripsi ini ditulis sedemikian rupa sehingga diperoleh hubungan yang jelas antara bagaian yang satu dengan yang lainnya.

Sistematika penulisan dari laporan ini adalah sebagai berikut :

BAB I Pendahuluan

Meliputi Latar Belakang, Tujuan, Rumusan Masalah, Batasan Masalah, Metodologi Penulisan dan Sistematika Penulisan.

BAB II Landasan Teori

Berisi tentang teori penunjang yang membantu dalam pembuatan alat.

BAB III Perencanaan Dan Pembuatan Alat

Meliputi berbagai hal yang berkenaan dengan perencanaan dan pembuatan alat yang berupa perangkat keras dan perangkat lunak.

BAB IV Pengujian Alat

Meliputi proses pengujian alat yang terdiri dari peralatan yang digunakan, langkah kerja dan analisa hasil pengujian.

BAB V Peunutup

Meliputi kesimpulan dan saran yang didapat selama perancangan dan pembuatan alat.

DAFTAR PUSTAKA

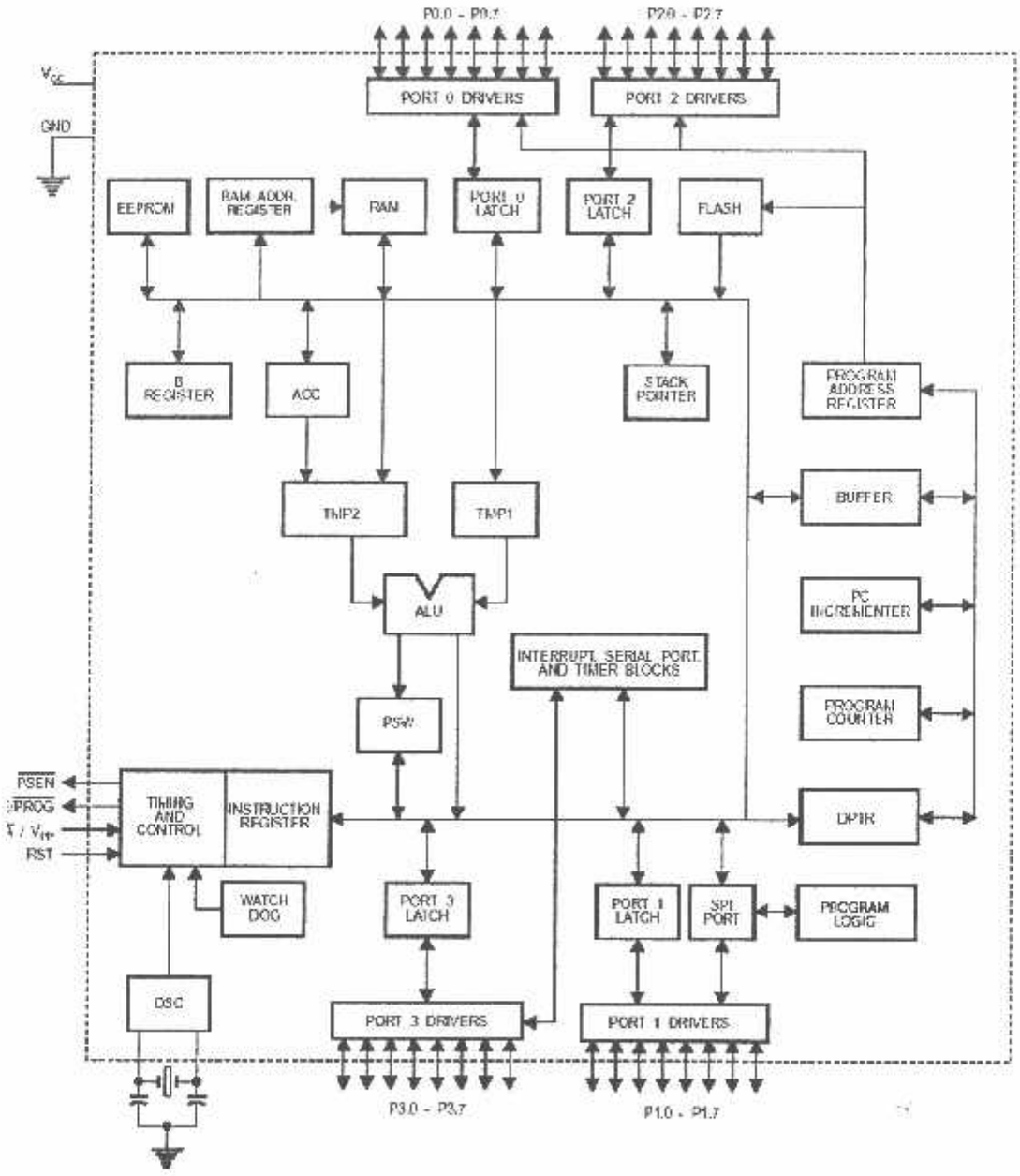
LAMPIRAN

BAB II

LANDASAN TEORI

2.1. Mikrokontroller AT89S8252

2.1.1. Arsitektur AT89S8252



Gambar 2.1. Blok Diagram AT89S8252[1]

Arsitektur Mikrokontroler AT89S8252 adalah sebagai berikut:

1. CPU (*Central Processing Unit*) 8 bit dengan *register* A (*Accumulator*) & B.
2. 16-bit *Program Counter* (PC) dan (*Data Pointer*) DTPR.
3. 8-bit *Program Status Word* (PSW).
4. 8-bit *Stack Pointer* (SP).
5. 8 K*byte* Flash PEROM *internal*.
6. 256 *byte internal* RAM.
   - 4 *bank register*, masing-masing berisi 8 *register*
   - 16 *byte* yang dapat dialamati pada bit level
   - 208 byte *general purpose memory data*
7. 32 pin *input-output* tersusun atas P0-P3. masing-masing 8-bit.
8. 3 buah *timer* (T0 & T1) dengan masing-masing 16-bit t*imer/ counter*.
9. *Receiver/transmiter data* secara *serial full duplex*: *Serial buffer* (SBUF).
10. *Control register* : (TCON, TMOD, SCON, PCON, IP & IE)
11. 9 buah *sumber* interupsi (2 buah sumber interupsi *external* dan 3 buah sumber interupsi *internal*).
12. *Oscillator* dan *clock internal*

Mikrokontroller AT89S8252 menyediakan fungsi standar sebagai berikut :

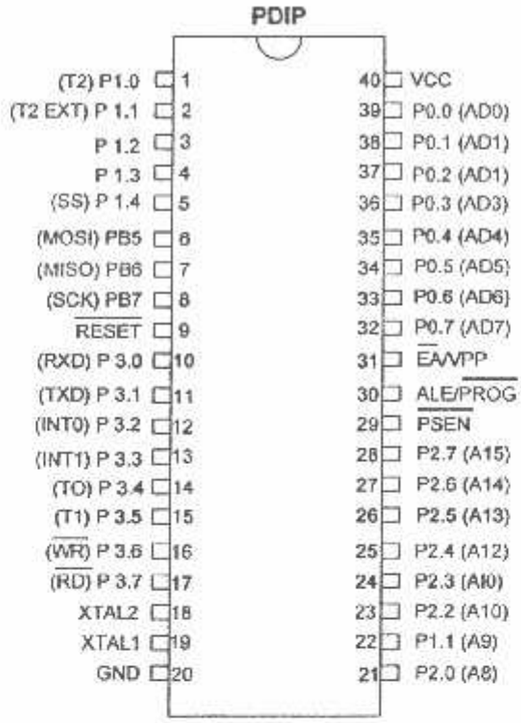
- ❖ 8K Bytes memori yang dapat diprogram ulang
- ❖ *Memory* 256 x 8 bit *Internal* RAM
- ❖ 32 jalur I/O (Input dan Output) yang dapat diprogram
- ❖ Tiga buah 16 Bit Timer dan Counter
- ❖ Dual Data Pointer (DPTR)
- ❖ Programable Watchdog Timer

- ❖ Waktu pemrograman yang singkat
- ❖ Memiliki internal memori (EEPROM) sebesar 2KByte
- ❖ 9 Sumber Interupsi
- ❖ ISP Port
- ❖ Oscillator dan clock 12 - 24 MHz
- ❖ Programmable UART Serial Chanel
- ❖ Power-Off Flag

Sebagai tambahan AT89S8252 dirancang menggunakan logika yang statis untuk mode pengoperasian yang menuju ke frekwensi dasar dan pendukungan terhadap dua Software, serta dapat memilih model power savingnya. *Mode idle* akan berhenti ketika CPU sedang menjalankan RAM, *Timer/Counter*, Serial Port dan *Interupt Sistem* untuk terus melanjutkan fungsinya. Model power down akan menyimpan isi dari RAM tapi akan memberhentikan osilator dan akan menghentikan semua *chip* lain yang sedang berfungsi sampai terdapat adanya gangguan dari luar atau hardware di reset.

2.1.2. Konfigurasi Pin - pin Mikrokontroller

Konfigurasi kaki-kaki Mikrokontroller terdiri dari 40 pena (pin), seperti pada gambar dibawah ini :



Gambar 2.2. Pin – pin AT89S8252 [1]

Fungsi dari tiap-tiap pena adalah sebagai berikut :

VCC : Power Supply (sumber tegangan).

GND : Ground.

Port 0 : Merupakan *port input* dua arah dan dikonfigurasikan sebagai *multipleks* dua bus alamat rendah (A0-A7) dan data selama pengaksesan program memori dan data internal.

Port 1 : Merupakan *port input* dua arah dengan pull-up dan juga menerima *Low-order address byte* selama memprogram dan verifikasi dari *flash*. Pada mikrokontroller AT89S8252 port 1 memikili 3 pin dengan fungsi khusus.

Tabel 2.1. Fungsi Alternatif Port 1

Port Pin	Fungsi Alternatif
P1.5	MOSI (*Master Output Slave Input*)
P1.6	MISO (*Master Input Slave Output*)
P1.7	SCK (*Serial Clock*)

Port 2 : Merupakan *port I/O* dengan *internal pull-up*. Mengeluarkan *address* tinggi selama pengambilan (*fetching*) program memori eksternal. Selama pengaksesan ke eksternal data memori, port 2 mengeluarkan isi SFR (*Special Function Register*). Menerima *address* dan beberapa sinyal kontrol selama pemrograman.

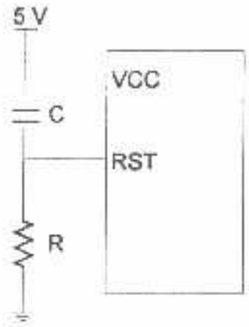
Port 3 : Merupakan *port I/O* dengan *internal pull-up*. Port 3 juga memiliki fungsi khusus, yaitu:

Tabel 2.2. Funsi – fungsi Alternatif Port 3

Port Pin	Fungsi Alternatif
Pin 3.0	RXD (Serial Input Port)
Pin 3.1	TXD (Serial Output Port)
Pin 3.2	INT0 (Eksternal Interrupt 0)
Pin 3.3	INT1 (Eksternal Interrupt 1)
Pin 3.4	T0 (Timer 0 Eksternal Input)
Pin 3.5	T1 (Timer 1 Eksternal Input)
Pin 3.6	WR (Eksternal Data Memory Write Strobe)
Pin 3.7	RD (Eksternal Data Memory Read Strobe)

Reset : Inputan reset akan memberikan logika High '1' pada pin ini dengan jangka waktu yang ditentukan oleh lamanya pengosongan data muatan kapasitor. Jangka waktu minimal adalah 2 siklus

mesin (24 periode frekwensi clok) ditambah waktu start On Osilator.



Gambar 2.3. Rangkaian Power On Reset [1]

ALE/$\overline{\text{PROG}}$: Keluaran ALE (*Address Latch Enable*) menghasilkan pulsa – pulsa untuk menutup byte rendah (*Low Bite*) alamat selama mengakses memori eksternal. Pin ini juga berfungsi sebagai inputan pulsa program (The Program Pulse Input) atau PROG selama melakukan Flash Program. Pada operasi normal, ALE akan berpulsa dengan laju 1/6 dari frekwensi kristal dan dapat digunakan sebagai pewaktuan (*Timing*) atau pedetakan (*clocking*) rangkaian eksternal. Sebagai catatan ada sebuah pulsa yang dilewati selama pengaksesan memori data eksternal. Jika dikehendaki operasi ALE dapat dinonaktifkan dengan cara mengatur bit 0 dari SFR (*Special Function Register*) lokasi 8Eh..

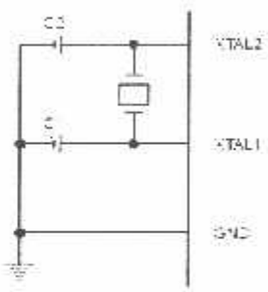
$\overline{\text{PSEN}}$: **$\overline{\text{PSEN}}$** (*Program Store Enable*) merupakan sinyal baca untuk memori program eksternal. Ketika mikrokontroller AT89S8252 menjalankan kode dari program eksternal, **$\overline{\text{PSEN}}$** akan diaktifkan

sebanyak 2 kali per siklusnya, kecuali dua aktifasi $\overline{\text{PSEN}}$ dilompati (diabaikan) saat mengakses memori data eksternal.

$\overline{\text{EA}}$/VPP : **EA/$\overline{\text{VPP}}$** (*Eksternal Access Enable*). $\overline{\text{EA}}$ harus selalu dihubungkan ke ground jika digunakan untuk mengakses eksternal memori. Dan $\overline{\text{EA}}$ dihubungkan ke Vcc jika digunakan untuk menjalankan program secara internal.

XTAL1 : Merupakan input ke penguat pembalik osilator dan ke rangkaian operasi *Clock Internal*.

XTAL2 : Keluaran dari penguat pembalik osilator.



Gambar 2.4. Rangkaian Crystal [1]

Mikrokontroller AT89S8252 memiliki rangkaian osilator internal dengan mengacu pada frekwensi referensi pada pin XTAL1 dan XTAL2.

Programable Wacthdog Timer (WDT) :

Fungsi dari PWDT sebenarnya adalah untuk melakukan peresetan secara otomatis. Dimana dia akan me - reset mikrokontroler jika mikrokontroler hang. Oleh sebab itu user harus selalu me – reset WDT sebelum WDT mereset mikrokontroler, jika WDT tidak direset oleh mikrokontroler dalam jangka waktu yang telah ditentukan maka secara otomatis WDT – lah yang akan mereset

mikrokontroler. PWDT terdiri dari suatu 14-bit counter dan *Watchdog Timer Reset* (WDTRST) SFR. WDT diset default untuk menonaktifkan reset yang ada. Tidak ada jalan lain untuk menonaktifkan WDT kecuali melalui reset (baik Hardware reset atau *WDT Overlow reset*). Jika *WDT Overlow*, itu akan membuat suatu keluaran Reset High di pin RST.

Dual DPTR (*Data Pointer Register*) :

DPTR sebenarnya digunakan untuk melakukan transaksi dengan memori eksternal. Ini dikarenakan dalam keluarga MCS – 51 tidak dapat melakukan pemindahan data secara langsung dari RAM Internal dengan memori Eksternal. Pemindahan data semacam ini memerlukan DPTR untuk memberitahukan dimana alamat tepatnya data akan dipindahkan dari RAM Internal atau dari RAM Internal ke Memori Eksternal.

ISP Port :

ISP Port digunakan untuk melakukan pemrograman secara langsung tanpa harus melepaskan IC dari tempatnya, cara ini agar lebih efisien pada waktu melakukan pemrograman ada terjadi kesalahan maka kita tidak perlu melepaskan IC tersebut untuk kembali memprogramnya di downloader AT89S8252.

2.1.3. Organisasi Memori

Dalam mikrokontroler AT89S8252 ruang alamat telah dibedakan untuk program memori dan data memori.

2.1.3.1. Internal Program Memory

Mikrokontroler AT89S8252 memiliki program memori *internal* sebesar 4Kbyte dengan ruang alamat 0000H-0FA0H. Jika alamat-alamat program lebih tinggi dari pada 0FA0H dimana melebihi kapasitas ROM *internal*, menyebabkan AT89S8252 secara otomatis mengambil kode byte dari program memori *external*. Kode *byte* juga dapat diambil hanya dari memori *external* dengan alamat 0000H-FFFFH dengan cara menghubungkan pin EA ke *ground*.

2.1.3.2. Random Access Memory (RAM)

Ruangan alamat memory data *internal* (RAM) dengan kapasitas 256 *byte* yaitu: 00H-FFH yang terbagi atas 3 daerah, yaitu:

1. Empat *bank register*

   Setiap *bank* terdiri dari 8 *register* (R0-R7) sehingga jumlah *register* untuk ke-empat *bank register* menjadi 32 buah *register* yang menempati ruang alamat 00H-1FH. Mengaktifkan salah satu *bank register* dapat dilakukan dengan mengatur RS0-RS1 pada *Program Status Word* (PSW).

2. Bit Addressable

   Terdiri dari *16 byte* yang berada pada alamat 20H-2FH. Masing-masing bit dalam 128 bit yang lokasinya dapat dialamati secara langsung.

3. RAM Keperluan Umum

   Terdiri atas 208 *byte* yang menempati alamat 30H-FFH, dan dapat dialamati secara langsung maupun tak langsung dalam penggunaan untuk keperluan umum (*general purpose*).

Tabel 2.3

***Pengaturan RS0-RS1* Bank Register**

RS1	*RS0*	Register Bank Select Bits
0	0	*Bank* 0
0	1	*Bank* 1
1	0	*Bank* 2
1	1	*Bank* 3

2.1.4. SFR (*Special Function Register*)

Untuk operasi AT89S8252 yang menggunakan alamat internal RAM (00H-7FH). Beberapa dari *register-register* ini juga mampu dengan pengalamatan bit sehingga dapat dioperasikan seperti yang ada pada RAM.

❖ ***PSW (Program Status Word)***

Register ini terletak di alamat D0H. Cara mendefenisikannya ditunjukkan pada tabel 2.2. berikut ini :

Tabel 2.4
Pengaturan RS0-RS1 *Bank Register*

Alamat	Data	Simbol	Posisi	Fungsi /Arti
D0H	D0	P	PSW.0	*Parity flag*
	D1	-	PSW.1	*Flag* didefinisikan oleh pemakai.
	D2	OV	PSW.2	*OverflowFlag*
	D3	RS0	PSW.3	Bit pemilih *bank register.*
	D4	RS1	PSW.4	Bit pemilih *bank register.*
	D5	F0	PSW.5	*Flag 0*
	D6	AC	PSW.6	*Auxiliary CarryFlag*
	D7	CY	PSW.7	*Carry Flag*

❖ ***PCON (Power Control)***

Register ini terletak pada alamat 87H. Cara mendefenisikannya ditunjukkan pada tabel 2.3 berikut ini :

Tabel 2.5
Skema Medefinisikan PCON

Alamat	**Data**	**Simbol**	**Fungsi /Arti**
87H	D0	IDL	*Idle* mode bit
	D1	PD	*Power Down* bit
	D2	GF0	Bit *flag* serbaguna.
	D3	GF1	Bit *flag* serbaguna.
	D4	-	Tidak dipakai.
	D5	-	Tidak dipakai.
	D6	-	Tidak dipakai.
	D7	SMOD	Digunakan untuk menghasilkan *baudrate* dan SMOD_1, maka *baudrate* akan *double* baik mode 0,1,2 atau 3.

❖ ***Sistem Interupsi***

Mikrokontroler AT89S8252 mempunyai 9 buah sumber interupsi yang dapat mengakibatkan permintaan interupsi, yaitu: INT0, INT1, T0, T1 port serial dan beberapa port lainnya. Saat terjadi interupsi mikrokontroler secara otomatis akan menuju ke *subrutin* pada alamat tersebut. Setelah interupsi *service* selesai dikerjakan, Mikrokontroler akan mengerjakan program semula. Sumber interupsi *external* adalah INT0, INT1, dimana kedua interupsi *external* ini akan aktif pada transisi rendah selain itu juga ada *Timer/Counter 0, Timer/Counter 0* dan interupsi dari port serial (*receiver*). Interupsi serial dibangkitkan dengan melakukan operasi OR pada R1 dan T1. Tiap-tiap sumber interrupsi dapat di-*enable* atau di-*disable* secara *software*. Tingkat prioritas semua sumber interupsi dapat diprogram sendiri-sendiri dengan *set* atau *clear* bit pada SFRS IP (*Interrupt Priority*).

Tabel 2.6
Alamat Sumber Interupsi

Sumber Interupsi	***Alamat Awal***
Power On Reset	0000h
Interrupt luar 0 (INT 0)	0003h
Pewaktu/ pencacah 0 (T0)	000Bh
Interrupt luar 1 (INT 1)	0013h
Pewaktu/ pencacah 1 (T1)	001Bh
Port I/O *Serial*	0023h

Register yang berperan dalam mengatur aktif tidaknya interupsi adalah *interrupt enable register*, susunan dari bit-bit beserta kegunaannya adalah:

Tabel 2.7
Kegunaan *Interrupt Enable Register*

Alamat	**Data**	**Simbol**	**Posisi**	**Fungsi /Arti**
A8H	D0	EX0	IE.0	Diatur secara *software* untuk interupsi dari INT1.
	D1	ET0	IE.1	Diatur secara *software* untuk interupsi dari *timer/counter* 1.
	D2	EX1	IE.2	Diatur secara *software* untuk interupsi dari INT1.
	D3	ET1	IE.3	Diatur secara *software* untuk interupsi dari *timer/counter* 1.
	D4	ES	IE.4	Untuk mengatur *enable* atau *disables* uatu interupsi R1/T1.
	D5	-	IE.5	Kosong
	D6	-	IE.6	Kosong
	D7	EA	IE.7	Jika diatur 0 maka semua interupsi di-*disable*, jika diatur 1 maka interupsi diatur di-*disable* atau di-*enable* menurut masing-*masing* bit.

❖ ***Timer/Counter***

Pengendalian kerja dari *timer/counter* dilakukan dengan pengaturan register yang berhubungan dengan kerja dari *timer/counter* yaitu melalui sebuah *timer/counter mode control*. Untuk mengaktifkan *timer/counter* yang meliputi penentuan fungsi sebagai *timer* atau sebagai *counter* serta pemilihan *mode* operasi

dapat diatur melalui TMOD yang beralamat pada 89H. Konfigurasi dari *register* TMOD seperti yang ditunjukkan pada Tabel 2.8. berikut ini :

Tabel 2.8
***Register* TMOD**

Alamat	Data	Simbol	Posisi	Fungsi /Arti
88H	D0	IT0	TCON.0	*Interrupt* 0 *type control bit.*
	D1	IE0	TCON.1	*External interrupt* 0 *edge flag.*
	D2	IT1	TCON.2	*Interrupt type* 1 *control bit.* Diatur oleh *software* untuk menentukan aktif *low* atau *high trigger* dari *external.*
	D3	IE1	TCON.3	*External interrupt* 1 *edge flag.* Diatur oleh *hardware* ketika *external interrupt* terdeteksi dan nol-kan melalui *software* ketika *interrupt* diproses.
	D4	TR0	TCON.4	*Timer* 0 *control bit.* Diatur oleh *software* ketika *timer/ counter 0.*
	D5	TF0	TCON.5	*Timer* 0 *overflow flag control bit.* Diatur oleh *software* ketika *timer/counter 0 oferflow.*
	D6	TR1	TCON.6	*Timer* 1 *control bit.* Diatur oleh *software* ketika *timer/ counter 0.*
	D7	TF1	TCON.7	*Timer* 1 *overflow flag control bit.* Diatur oleh *software* ketika *timer/counter* 0 *oferflow.*

Tabel 2.9
Timer/Counter Mode Control Register

Alamat	Data	Simbol	Fungsi /Arti
89H	D0	*Timer* 0; M0 (0)	Untuk memilih mode *timer.*
	D1	*Timer* 0; M1 (0)	Untuk memilih mode *timer.*
	D2	*Timer* 0; C/T (0)	1 = *Counter* & 0 = *Timer*
	D3	*Timer* 0; GATE (0)	*Timer* akan berjalan jika bit di *set* dan INT0 (untuk *Timer* 0) atau INT1 (untuk *Timer* 1)
	D4	*Timer* 1; M0 (1)	Untuk memilih mode *timer.*
	D5	*Timer* 1; M1 (1)	Untuk memilih mode *timer.*
	D6	*Timer* 1; C/T (0)	1 = *Counter* & 0 = *Timer*
	D7	*Timer* 1; GATE (1)	*Timer* akan berjalan jika bit di *set* dan INT0 (untuk *Timer* 0) atau INT1 (untuk *Timer* 1)

Tabel 2.10
Mode Operasi Timer/Counter

M1	M0	Operating Mode
0	0	*Timer* 13 bit
0	1	*Timer/Counter* 16 bit
1	0	8 bit *Auto reload Timer /Counter*
1	1	TL0 dari *Timer* adalah 8 Bit *Timer/Counter* dikendalikan oleh kontrol bit *Timer* 0. TH0 adalah 8 bit yang dikendalikan oleh *Timer* 1 *control* bit.

2.1.5. Metode Pengalamatan

1. Pengalamatan bit (*Direct Bit Addressing*) :

   Pengalamatan langsung tiap bit ini hanya dilakukan pada lokasi RAM *internal* yaitu 20H-2FH, dan sebagian SFR yaitu: port 0, port 1, port 2, port 3, TCON *register*, SCON *register*, IE *register*, PSW *register*, ACC dan B *register*.

2. Pengalamatan tak langsung (*Indirect Bit Addressing*):

   Pada *pengalamatan* tak langsung, instruksi menunjukkan suatu *register* yang isinya adalah alamat dari *operand, eksternal* dan *internal* RAM dapat dialamati secara tidak langsung. *Register* alamat untuk data dengan lebar 8 bit dapat berupa R0 dan R1 yang digunakan untuk memilih angka *register* atau *stack pointer*. *Register* alamat untuk data, dengan lebar 16 bit digunakan *Data Pointer* (DPTR).

3. Pengalamatan ber-indeks :

   Yang dapat diakses dengan pengalamatan berindeks hanya *memory program*. Mode ini dimaksudkan untuk membaca *look-up table program*.

4. Konstanta *immediet* :

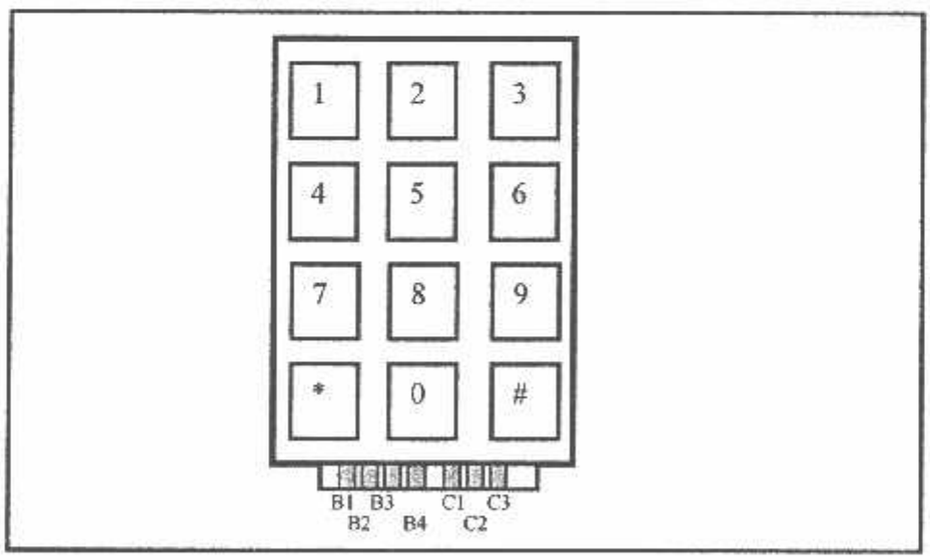
   Pengalamatan langsung dilakukan dengan memberikan nilai ke *register* secara langsung, dilakukan dengan menggunakan tanda #,Contoh: Mov A, #100

2.2. Keypad

Papan tombol ini digunakan untuk memasukkan data referensi dan mengubah data bila diinginkan. Untuk menterjemahkan informasi yang diterima dari papan tombol, maka *keypad* dihubungkan dengan *port* pada Mikrokontroller.

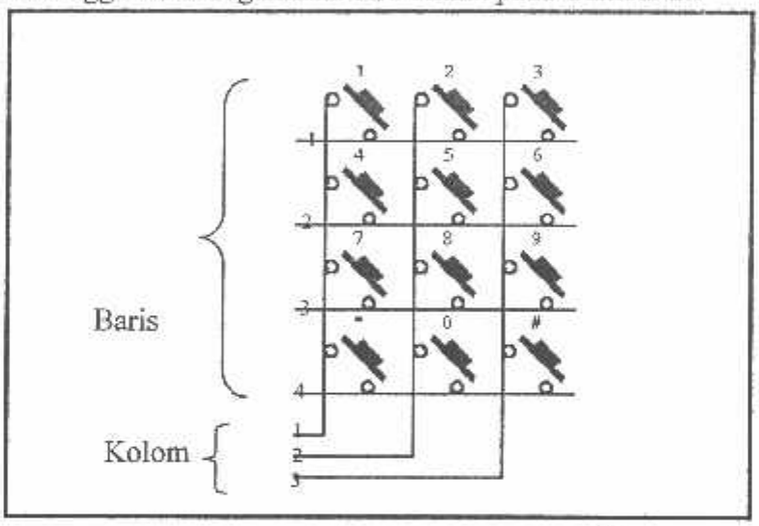
Papan tombol tersebut mempunyai matrik 4 baris dan 3 kolom. Deretan baris dan kolom dari papan tombol dihubungkan dengan *port* pada Mikrokontroller yang difungsikan sebagai masukan dan keluaran.

Matrik keypad 4 X 3 memungkinkan untuk membuat kombinasi tombol sebanyak 12 buah dengan menggunakan 7 buah kawat yang dibagi menjadi 4 baris dan 3 kolom. Setiap tombol mewakili sebuah baris dan sebuah kolom, sehingga dengan menekan sebuah tombol, maka akan hanya ada sebuah baris dan sebuah kolom yang terhubung, sebagaimana ditunjukkan pada Gambar 2.9. Dengan demikian keypad matriks 4 X 3 mampu melakukan penghematan saluran dua kali dari pada dengan menggunakan satu kawat untuk satu tombol. Prinsipnya, dengan penekanan sebuah tombol, akan ada dua buah kawat yang terhubung. Terhubungnya dua buah kawat ini kemudian akan menjadi kode untuk masing-masing tombol yang menandakan bahwa suatu tombol yang diidentifikasi oleh kode tersebut telah ditekan.



Gambar 2.5. Keypad Matriks 4 x 3 [2]

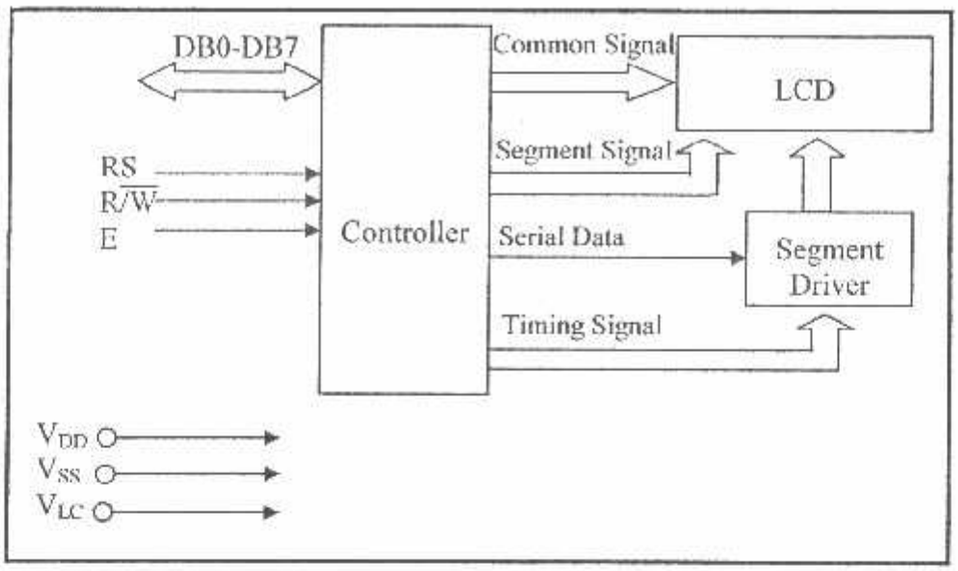
Untuk mendeteksi penekanan itu, maka diadakan *scanning* sebanyak 4 kali, setiap kali *scanning* diadakan pengecekan sebanyak 3 kali. *Scanning* dan pengecekan ini dilakukan secara berulang-ulang hingga ada penekanan tombol. Baris di jadikan *scanner*. Metode *scanning* dilakukan dengan cara membuat logik 0 pada salah satu baris secara bergantian. Sedangkan kolom dijadikan sebagai obyek pengecekan.. Pengecekan dilakukan dengan melihat apakah terdapat logik 0 diantara salah satu kolom. Jika ada, berarti ada tombol yang ditekan. Dengan demikian akan ada 16 kombinasi kode untuk mewakili tiap-tiap tombol yang ada, yaitu tombol 1.1 hingga 4.3 sebagaimana bisa dilihat pada Gambar 2.9



Gambar 2.6. Penampang Dasar Keypad [2]

2.3. LCD (Liquid Cristal Display)

Liquid cristal display (LCD) adalah modul tampilan yang mempunyai konsumsi daya yang relatif rendah dan terdapat sebuah kontroller CMOS didalamnya. Kontroller tersebut sebagai pembangkit ROM/RAM dan display data. Semua fungsi tampilan di kontrol oleh suatu instruksi modul LCD yang dapat dengan mudah diinterfacekan dengan MPU.



Gambar 2.7. Diagram Blok LCD M1632 [3]

Fungsi-fungsi yang ada dalam Diagram Blok diatas adalah sebagai berikut :

1. $DB_0 - DB_3$

   Empat bit bus data tertinggi dua arah dengan logika tiga keadaan.

2. $DB_4 - DB_7$

   Empat bit bus data terendah dua arah dengan logika tiga keadaan.

3. E (*Enable*)

   Sinyal yang menandakan permulaan operasi. Sinyal ini mengaktifkan data tulis atau baca.

4. R/W

   Sinyal operasi tulis dan baca. 0 untuk operasi tulis, dan 1 untuk baca.

5. RS

   Sinyal pemilih register. 0 untuk register data, dan 1 untuk register instruksi.

6. V_{LC}

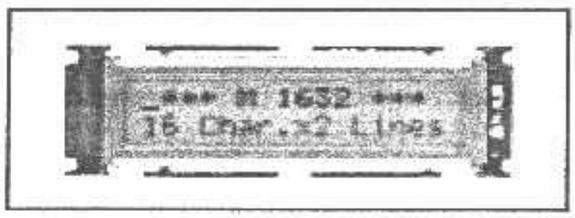
Terminal *supply* untuk mengatur contras LCD.

7. V_{DD}

Dihubungkan ke sumber tegangan +5 volt.

8. V_{SS}

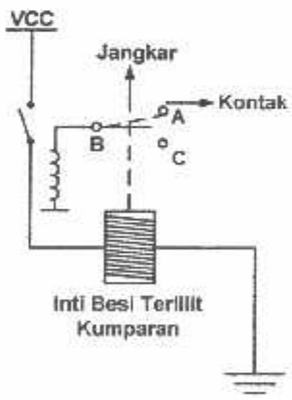
Dihubungkan ke ground rangkaian.



Gambar 2.8. Bentuk Fisik LCD M1632[3]

2.4 Relay

Relay adalah komponen elektronika yang terdiri dari sebuah lilitan kawat (kumparan/koil) yang terlilit pada sebuah besi lunak. Jika kumparan dialiri arus listrik maka inti besi akan menjadi magnet dan menarik pegas sehingga kotak AB terhubung dan BC terputus.



Gambar 2. 9. Cara Kerja Relay [4]

Relay merupakan suatu alat untuk menghubungkan atau memerlukan kontak antara komponen yang satu dengan yang lain. Dalam memutus atau menghubungkan kontak digerakkan oleh *fluksi* yang ditimbulkan dari adanya medan magnet listrik yang dihasilkan oleh kumparan yang melilit pada besi lunak. Ada beberapa jenis susunan kontak relay dimana semuanya terisolasi terhadap arus listrik yang ada didalam kumparan. Jenis susunan kontak sebagai berikut:

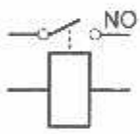
- *Normally Open (Normal Terbuka)*

  Yaitu kontak-kontak tertutup pada saat kumparan relay dialiri arus
- *Normally Close (Normal Tertutup)*

  Yaitu kontak-kontak terbuka pada saat kumparan relay dialiri arus

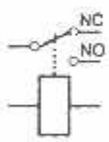
Ada beberapa macam relay, antara lain:

1. **SPST *(Single Pin Single Terminal)***



Gambar 2.10. Relay SPST [4]

2. **SPDT *(Single Pin Dual Terminal)***

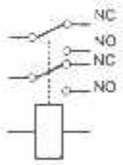


Gambar 2.11. Relay SPDT [4]

3. DPST *(Dual Pin Single Terminal)*

Gambar 2.12. Relay DPST [4]

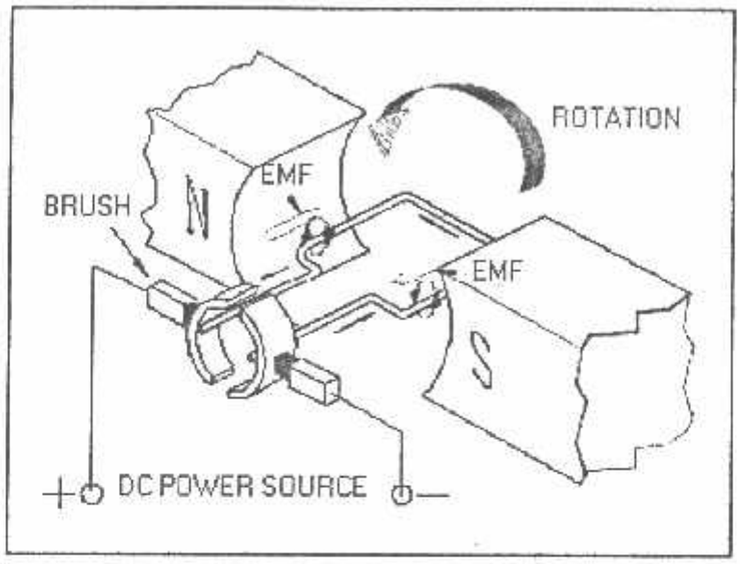
4. DPDT *(Dual Pin Dual Terminal)*



Gambar 2.13. Relay DPDT [4]

2.5. Motor DC

2.5.1. Kontruksi Dasar Motor DC

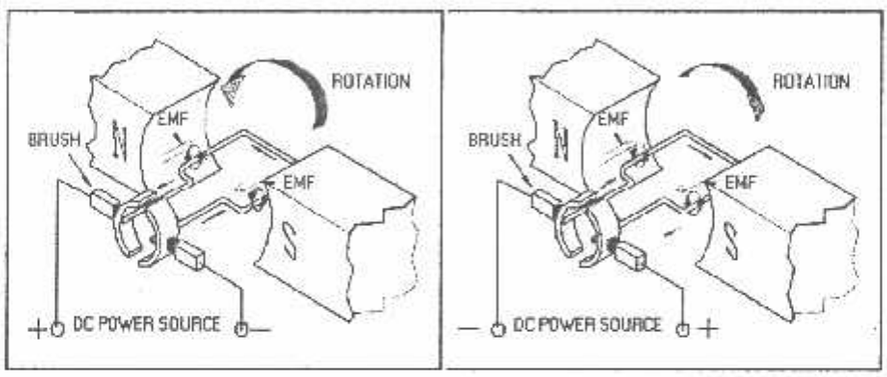


Gambar 2.14. Kontruksi Dasar Motor DC [5]

Pada gambar diatas tampak sebuah konstruksi dasar motor dc, pada gambar diatas terlihat bahwa pada saat terminal motor diberi tegangan dc, maka arus elektron akan mengalir melalui konduktor dari terminal negatif menuju ke terminal positif. Karena konduktor berada diantara medan magnet, maka akan timbul medan magnet juga pada konduktor yang arahnya seperti terlihat pada gambar diatas. Arah garis gaya medan magnet yang dihasilkan oleh magnet permanen adalah dari kutub utara menuju ke selatan. Sementara pada konduktor yang dekat dengan kutub selatan, arah garis gaya magnet disisi sebelah bawah searah dengan garis gaya magnet permanen sedangkan di sisi sebelah atas arah garis gaya magnet berlawanan arah dengan garis gaya magnet permanen. Ini menyebabkan medan magnet disisi sebelah bawah lebih rapat daripada sisi sebelah atas. Dengan demikian konduktor akan terdorong ke arah atas. Sementara

pada konduktor yang dekat dengan kutub utara, arah garis gaya magnet disisi sebelah atas searah dengan garis gaya magnet permanen sedangkan di sisi sebelah bawah arah garis gaya magnet berlawanan arah dengan garis gaya magnet permanen. Ini menyebabkan medan magnet disisi sebelah atas lebih rapat daripada sisi sebelah bawah. Dengan demikian konduktor akan terdorong ke arah bawah. Pada akhirnya konduktor akan membentuk gerakan berputar berlawanan dengan jarum jam seperti terlihat pada gambar diatas.

2.5.2. Pengendalian Motor DC



Gambar 2.15. Pengendalian Motor DC [5]

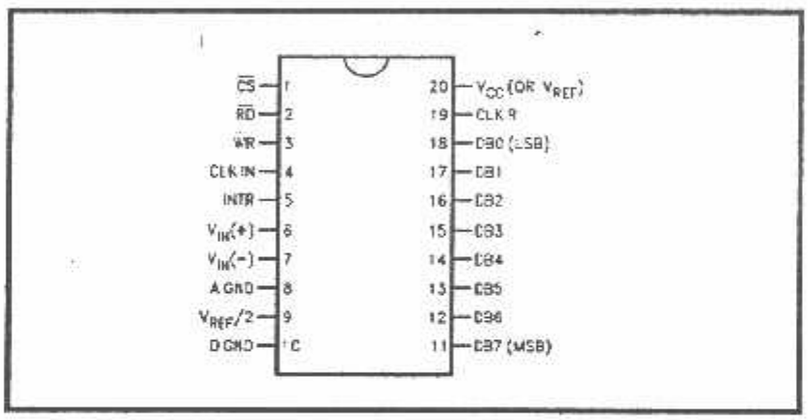
Dari gambar diatas, agar arah putaran motor dc berubah, maka polaritas tegangan pada terminal motor harus dibalik.

2.6. ADC 0804

Kebanyakan besaran yang dihadapi sehari-hari berubah secara beraturan (kontinyu). Perubahan tersebut tidak sekonyong-konyong melompat dari satu harga ekstrim ke harga ekstrim yang lain, melainkan berubah dengan melewati harga-harga yang ada diantara harga ekstrim tersebut. Besaran besaran tersebut digolongkan sebagai besaran analog.

Disamping besaran analog juga dikenal besaran digital. Sebagai contoh bila kita menghitung sesuatu, maka dalam menghitung tersebut kita melompat dari 1 ke 2, kemudian ke 3 dan sebagainya. Pengubahan bentuk analog ke dalam bentuk digital diperlukan karena mikrokontroller hanya dapat menerima besaran digital.

Piranti elektronika yang berfungsi untuk merubah besaran analog menjadi besaran digital dinamakan ADC (*Analog to Digital Conversion*). IC 0804 merupakan salah satu IC yang berfungsi sebagai pengubah analog menjadi 8 bit bentuk digital. Dengan demikian IC akan dapat merubah bentuk analog menjadi 255 step bentuk digital persamaannya. Bentuk fisik dari IC 0804 ditunjukkan pada gambar berikut :



Gambar 2.16. Susunan Pin IC 0804 [6]

Sedangkan rumus perubahan tiap step ADC dirumuskan sebagai berikut :

$$V_{Step} = \frac{2 \times V_{REF}}{2^N - 1}$$

Keterangan : Vs_{tep} : Perubahan tegangan tiap step

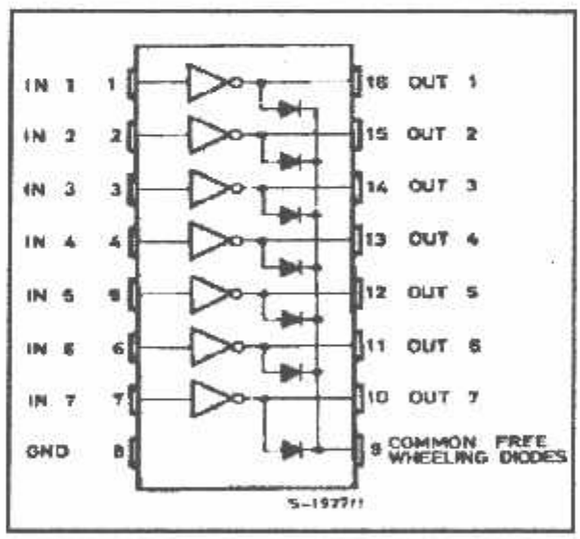
V_{REF} : Tegangan pada pin 9 ADC

N : Jumlah bit ADC

2.7. IC ULN 2003A

Pada IC ULN 2003A didalamnya terdapat rangkaian penguat Darlington. Untuk satu IC ULN2003A terdapat 7 pasang rangkaian Darlington NPN yang tersusun dalam rangkaian *common catoda*. Rangkaian Darlington ini digunakan sebagai saklar. Pada masing-masing rangkaian Darlington arus kolektornya sebesar 500mA. Rangkaian Darlington yang ada di dalam IC ULN 2003A dapat diparalel guna untuk kebutuhan arus yang besar. Karenanya IC ini dapat diaplikasikan untuk *driver* relay, *driver* lampu, *driver display* dan *logic buffer*. Pada skripsi ini rangkaian Darlington yang ada pada IC ULN 2003A digunakan sebagai *driver* relay yang digunakan untuk mengendalikan putaran motor dc.

Adapun pin-pin koneksi yang ada dalam IC ULN 20003A dapat dilihat pada gambar di bawah ini:



Gambar 2.17. Pin-Pin Koneksi Dalam IC ULN 2003A [7]

2.8. Sensor Berat

Untuk mengukur besaran berat maka dibutuhkan suatu tranducer yang dapat mengubah suatu besaran berat menjadi besaran listrik. Tranducer yang sering digunakan adalah *strain gage*. Tetapi oleh karena tranducer ini memiliki bentuk fisik yang sangat kecil, maka dalam skripsi ini untuk menghindari kerusakan yang permanent (akibat posisi pemasangan yang sulit dan menghindari gesekan belt konveyor) pada *strain gage* maka penulis menggunakan alternative lain yaitu berupa tranducer posisi (potensiometer).

Potensiometer merupakan komponen elektronika yang memiliki nilai resistansi yang variable. Perubahan resistansi tersebut dapat dilakukan secara mekanis. Berdasarkan sistem mekanis perubahan nilai resistansinya, potensio meter dibedakan menjadi potensiometer jenis putar dan potensiometer jenis geser. Nilai-nilai potensio meter yang terdapat dipasaran antara lain adalah 500 Ω, 1K, 5K,10K, 50K, 100K, 1M dan lain sebagainya. Simbol dari potensiometer adalah sebagai berikut :

Gambar 2.18. Simbol Dari Potensiometer

2.9. LED Inframerah Dan Photodioda

Dalam aplikasi, led infra merah digunakan bersama dengan photodioda dimana led sebagai pemancar (Tx) dan photodioda sebagai penerima (Rx) atau

sensornya. Rangkaian sensor ini biasanya dioperasikan dalam uji kondisi dua keadaan, yaitu ada atau tidak adanya cahaya infra merah. Pada prinsipnya photodioda adalah mengkombinasikan kemampuan untuk mendeteksi jumlah cahaya yang masuk padanya dan menghasilkan penguatan berupa tegangan.

Adapun konstruksi dari sebuah photodioda hampir sama dengan transistor BJT biasa, kecuali bagian atasnya terdapat sebuah jendela/lensa, seperti terlihat pada gambar 2.12 dibawah ini:

Gambar 2.19 Simbol LED Infra Merah Dan Photo Dioda

Timbulnya *photon* menggerakkan sepasang *hole electron* dalam pertemuan kolektor-basis. Tegangan *reverse* bias antara kolektor-basis akan menarik *hole* yang diinduksikan ke basis dan kolektor area. *Forward* bias dari basis emitor akan menyebabkan *hole-hole* mengalir dari basis ke emitor seperti juga elektron mengalir dari emitor ke basis

Pada titik ini transistor biasa akan mengambil alih yaitu dengan emitor *infected electron* bagian basis yang sempit dan ditarik kearah kolektor yang lebih positif. Aliran elektron menuju sumber cahaya yang diinduksikan oleh sepasang *hole electron* menyokong arus basis dan apabila transistor dihubungkan dalam konfigurasi *common emitor*, arus cahaya yang diinduksikan dikalikan dengan Hfe dari transistor dan akan muncul arus kolektor.

Makin tinggi intensitas cahaya yang mengenai photodioda maka tahanan photodioda akan makin rendah, sehingga menyebabkan tegangan output menjadi kecil. Sedangkan bila sinar dari led infra merah sebagai sumber cahaya tidak mengenai photodioda, maka keluaran akan sama dengan tegangan input (VCC).

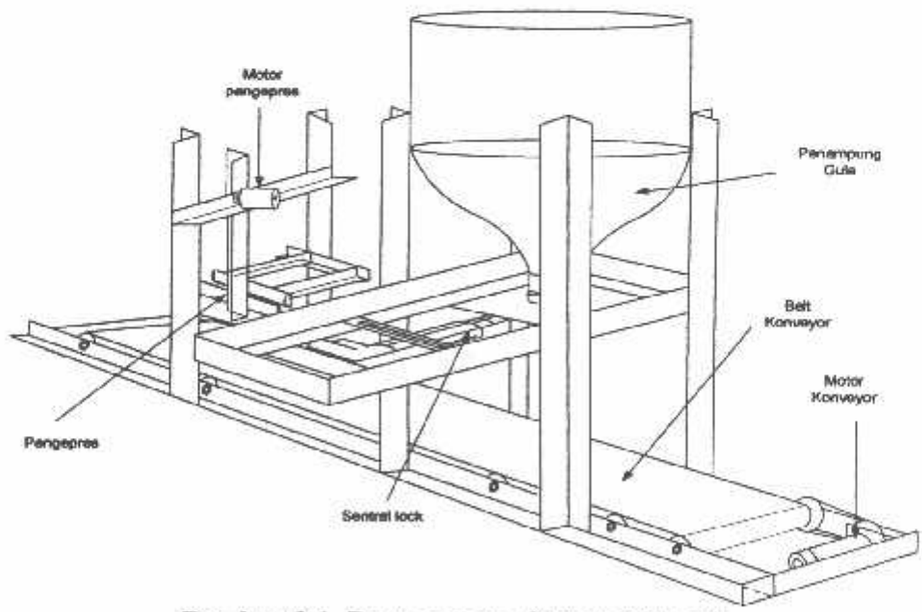
BAB III

PERANCANGAN DAN PEMBUATAN ALAT

Bab ini membahas tentang perencanaan dan pembuatan alat. Pada awalnya akan dibahas gambaran umum mengenai fungsi dan proses kerja sistem yang dirancang, kemudian dilanjutkan dengan pembahasan mengenai perancangan sistem mekanis alat dan sistem kontrol elektronika yang deterapkan pada alat tersebut.

3.1. Gambaran Umum Fungsi dan Proses Kerja Sistem

Sistem yang dirancang ini adalah simulasi dalam otomatisasi proses penetuan berat gula hingga pengepresan gula dalam plastik kemasannya. Mekanis sistem dirancang sebagai berikut :



Gambar 3.1. Perancangan Sistem Mekanis
* Sumber : Perancangan

Proses kerja sistem dirancang sebagai berikut :

Pada penggunaan awal, operator harus memasukkan berat gula yang di butuhkan. Berat gula yang dapat dipilih sebesar 1 Kg dan 1,5 Kg. Setelah itu operator memasukkan variable jumlah kantong gula yang ingin di hasilkan.

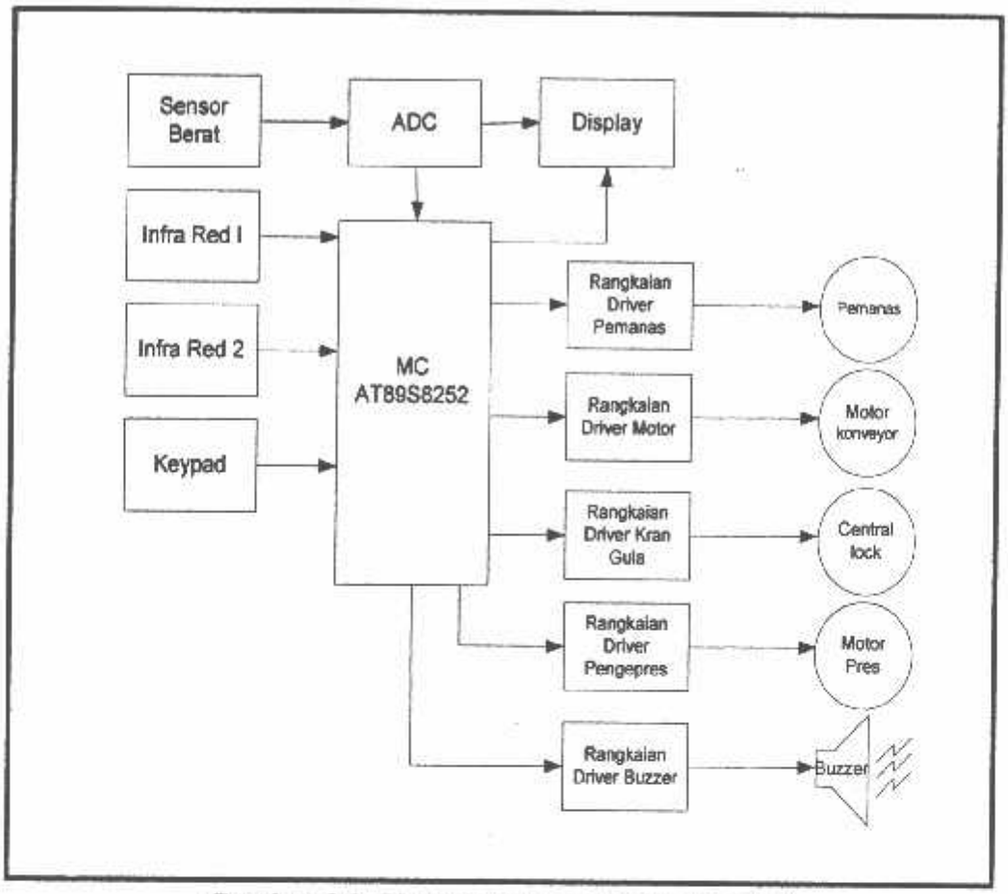
Dengan menekan tombol enter proses sistem akan mulai aktif, ditandai dengan bergeraknya konveyor. Operator dapat meletakkan kantung plastik pada konveyor yang sedang berjalan. Jika kantung plastik telah berada di bawah bak penampung gula, maka konveyor akan berhenti bergerak.

Proses selanjutnya adalah proses pengisian gula pada kantung dengan berat yang telah ditetapkan sebelumnya, melalui keypad. Proses ini diawali dengan membukanya kran pembuka sehingga gula yang berada pada bak penampung mengucur pada kantong. Berat gula akan di deteksi oleh sensor berat. Ketika berat telah sesuai, kran pembuka akan langsung menutup dan konveyor akan kembali bergerak.

Suatu saat kantung plastik yang telah berisi gula akan berada pada mekanis pengepres. Pada saat tersebut konveyor akan kembali berhenti, dan proses pengepresan kantong gula berlangsung. Setelah proses tersebut kantong gula telah terbungkus. Proses ini akan berlangsung sejumlah variable banyaknya kantung plastik yang telah tersetting sebelumnya. Buzer akan berbunyi ketika seluruh proses telah selesai.

3.2. Perancangan Sistem Kontrol Elektrik Alat

Agar sistem mekanis yang dirancang dapat bekerja sesuai yang diharapkan maka sistem kontrol elektronika akan dirancang seperti blok diagram sebagai berikut :



Gambar 3.2. Blok diagram perancangan alat

* Sumber : Perancangan

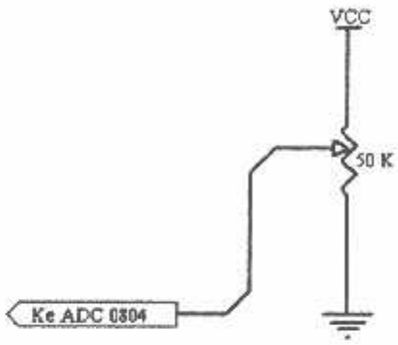
Pada blok diagram diatas sistem memiliki input yang bersumber dari sensor berat, dua buah sensor infra merah, dan keypad. Sedangkan output sistem berupa satu buah display, pemanas, motor konveyor, sentralock sebagai kran pembuka, motor pengepres, dan buzzer yang difungsikan sebagai indikator.

3.2.1. Sensor Berat

Sensor yang digunakan pada perencanaan alat ini adalah potensiometer geser. Setiap keluaran yang berasal dari sensor yang berupa V (sensor) atau

tegangan sensor yang diperoleh dari pengolahan dari nilai resistansi sensor akan dijadikan V (input) ADC.

Adapun perencanaan sensor berat adalah seperti pada gambar berikut :



Gambar 3.3. Sensor Berat
*Sumber : Perancangan

Pada rangkaian didapat arus awal sebesar 100 μA yang didapat dengan:

$$I \text{ disensor} = \frac{V_{cc}}{Rs}$$

Dimana : Vcc = Tegangan masuk sensor

Rs = Tahanan sensor

I sensor = Arus yang melewati sensor

Diketahui :Vcc = 5 volt

Rs = 50 KΩ

$$I \text{ sensor} = \frac{5volt}{50k\Omega} \quad \text{.....(3.1)}$$

I sensor = 100 μA

Ketika sensor berada pada kondisi normal (tanpa beban), nilai R1 = 50 KΩ dan nilai R2 = 0 KΩ, dengan demikian tegangan output sensor sebesar :

$$\text{V output min} = \frac{R2}{R1 + R2} x5Volt$$

$$\text{V output min} = \frac{0}{50K + 0} x5Volt \quad \text{.....(3.2)}$$

$$\text{V output min} = 0 \text{ Volt}$$

Dan ketika sensor berada pada kondisi beban dengan berat 2000 gram (beban ini merupakan beban maksimal yang disesuaikan dengan besar alat) nilai R1 = 30 KΩ dan nilai R2 = 20 KΩ, dengan demikian tegangan output sensor sebesar :

$$\text{V output max} = \frac{R2}{R1 + R2} x5Volt$$

$$\text{V output max} = \frac{20K}{30K + 20K} x5Volt \quad \text{.....(3.3)}$$

$$\text{V output max} = 2 \text{ Volt (2000 mV)}$$

Dengan demikian maka sensitivitas (S) dari sensor yang dirancang adalah sebesar:

$$\text{S} = \frac{V \text{ max} - V \text{ min}}{Berat \text{ max} - Berat \text{ min}}$$

$$\text{S} = \frac{2000 - 0}{2000 - 0} \quad \text{.....(3.4)}$$

$$\text{S} = 1 \; mV/gram$$

Jadi setiap perubahan 1 gram diwakili dengan perubahan tegangan sebesar 1 mV. Dan pada perancangan alat ini perubahan berat yang direncanakan adalah per - 10 gram dengan perubahan tegangan sebesar 10 mV.

3.2.2. ADC (*Analog to Digital Convertion*)

Penggunaan ADC pada perancangan alat ini digunakan untuk merubah besaran analog yang bersumber pada sensor berat menjadi besaran digital yang dapat dikenali oleh mikrokontroller.

ADC yang digunakan merupakan ADC dengan tipe 0804 yang memiliki output sebesar 8 bit. Rangkaian ADC memerlukan pewaktu (*clock*) untuk mengatur kerjanya. Dalam hal ini untuk frekwensi clock ADC dapat dihitung sebesar :

Diketahui : R = 10 K
C = 150 pF

$$\text{Frekwensi clock} = \frac{1}{1{,}1(RC)}$$

$$= \frac{1}{1{,}1(10K.150pF)} \quad \text{.....(3.5)}$$

$$= 606 \text{ KHz}$$

Dengan frekwensi clock sebesar 606 KHz, maka waktu konversi yang diperlukan internal ADC adalah:

Frekwensi clock = 606 KHz

$$\text{Maka periode clock} = \frac{1}{F}$$

$$= \frac{1}{606KHz} \quad \text{.....(3.6)}$$

$$= 1{,}65 \ \mu s$$

Pengujian terhadap rangkaian ADC dilakukan untuk mengetahui output dari ADC 0804 untuk berbagai variasi tegangan masukan. Besarnya resolusi dapat dihitung dengan menggunakan rumus :

$$\text{Resolusi (R)} = \frac{2xVref/_2}{2^N - 1}$$

Di mana N = jumlah bit

Vref/2 yang digunakan dalam perencanaan alat ini adalah sebesar 1,3 Volt, hal ini digunakan untuk mendapatkan perubahan tegangan tiap step (resolusi) dari ADC sebesar :

$$\text{Resolusi} = \frac{2x1,3}{255} \quad \text{.....(3.7)}$$

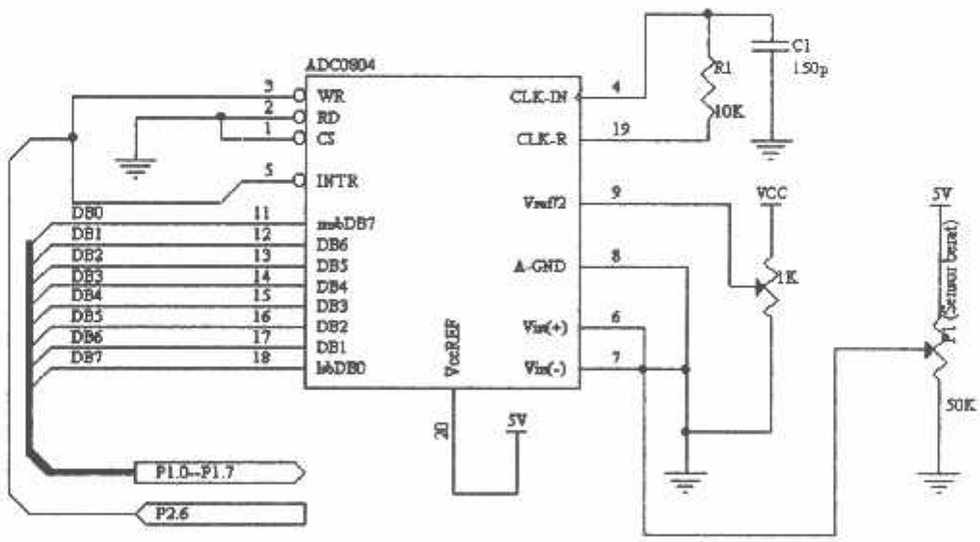
$$= \frac{2,6}{255}$$

$$= 0,01 \text{ Volt}$$

Jadi kenaikan atau perubahan per step ADC sebesar 0,01 Volt atau 10 mV.

Sehingga data output dari ADC dapat dihitung :

$$\text{Output ADC} = \frac{Vin}{\text{Re}solusi} \quad \text{.....(3.8)}$$



Gambar 3.4. Rangkaian ADC 0804

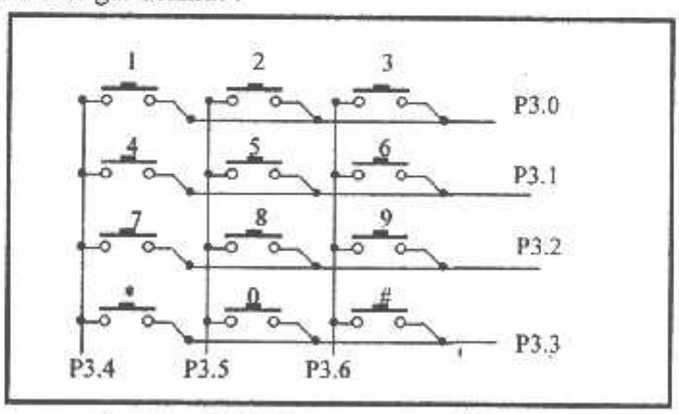
* Sumber : Perancangan

3.2.3. Keypad

Keypad berfungsi untuk menentukan berat gula yang akan ditimbang dan jumlah yang diinginkan. Keypad yang digunakan disini merupakan keypad 3 kolom X 4 baris yang memiliki tombol angka 0 sampai 9, *, dan #. Tombol 0-9 berfungsi untuk menentukan berat dan jumlah gula sedangkan # difungsikan sebagai tombol enter.

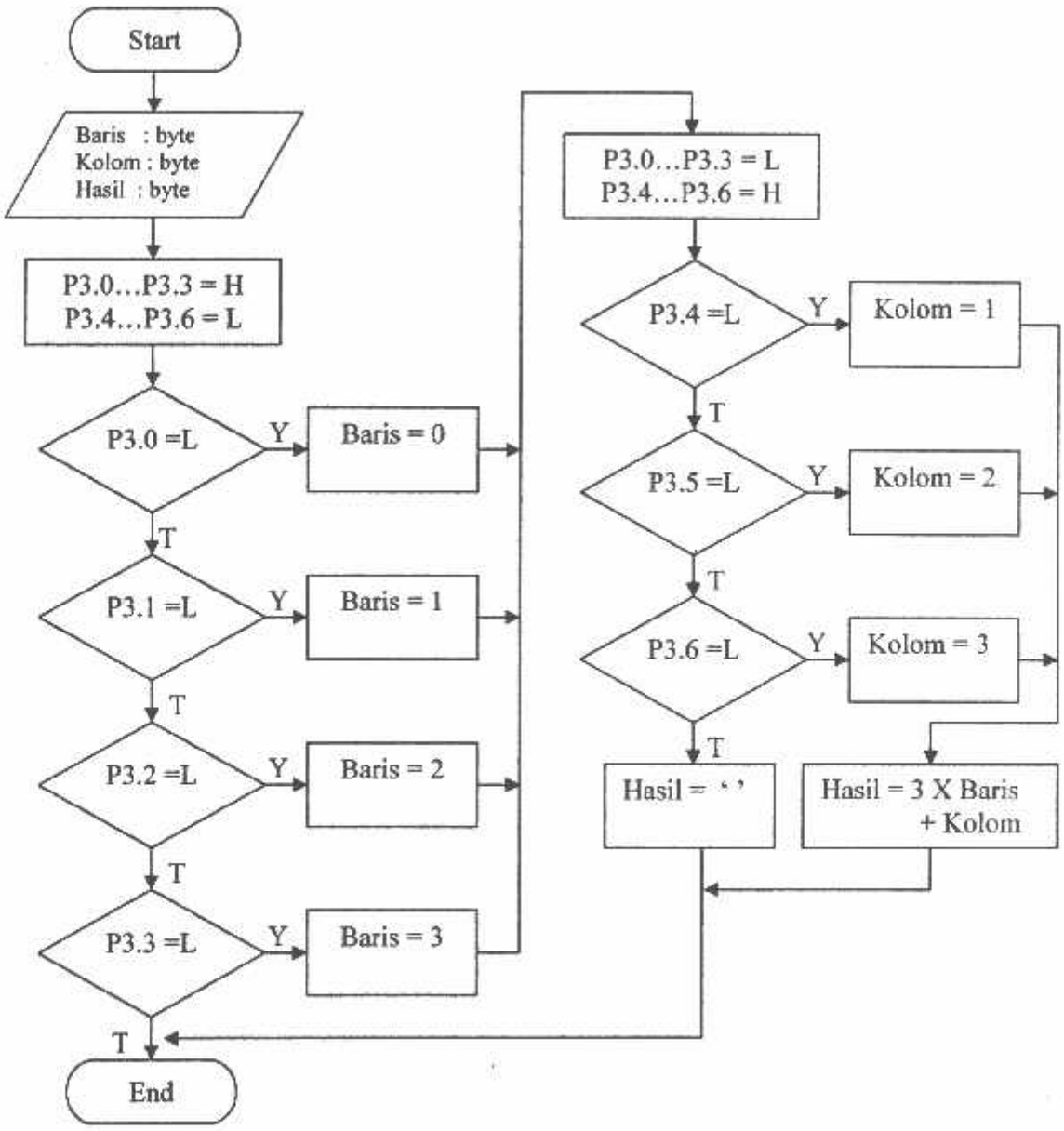
Untuk mengetahui posisi tombol mana yang ditekan software pendeteksi keypad disusun menggunakan algoritma sebagai berikut:

1. Buat semua baris berlogika H, dan buat kolom berlogika L
2. Periksa kondisi logika pada baris keypad. Jika ada penekanan salah-satu tombol keypad maka salah-satu baris akan berlogika L.
3. Membuat semua baris berlogika L, dan kolom berlogika H.
4. Periksa kondisi kolom, jika salah satu tombol keypad ditekan maka salah-satu kolom akan berlogika L.
5. Dengan demikian posisi penekanan setiap tombol keypad dapat diketahui melalui pemeriksaan baris dan kolom keypad. Perancangan keypad digambarkan sebagai berikut :



Gambar 3.5. Perancangan Keypad
*Sumber : Perancangan

Proses pengidentifikasian keypad tersebut digambarkan pada diagram alir sebagai berikut :



Gambar 3.6. Flowchart Pengidentifikasian Keypad
*Sumber : Perancangan

Dari gambar flowchart diatas hasil pengidentifikasian keypad dituliskan pada tabel 3.1:

Tabel 3.1. Fungsi dari setiap tombol keypad

Tombol	Hasil	Fungsi		Tombol	Hasil	Fungsi
1	1	Angka		7	7	Angka
2	2	Angka		8	8	Angka
3	3	Angka		9	9	Angka
4	4	Angka		*	10	Refres
5	5	Angka		0	11	Angka
6	6	Angka		#	12	Run (enter)
				Tidak ditekan	Spasi	-

* Sumber : Perancangan

3.2.4. MC AT89S8252

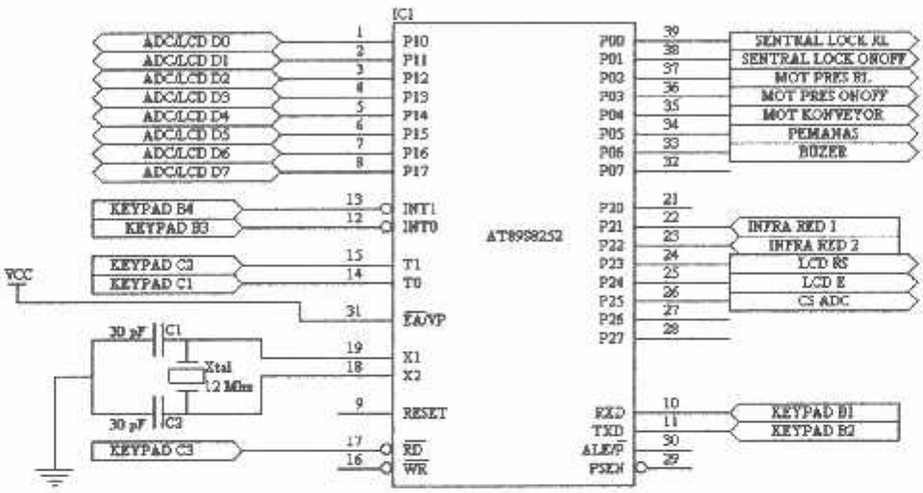
Rangkaian mikrokontroller merupakan unit utama yang mengontrol proses kerja sistem. Perancangan mikrokontroller AT89S8252 ini dilengkapi dengan penggunaan Xtal 12 Mhz sebagai penggerak oscilator internalnya.

Mikrokontroller ini mendapatkan input yang bersumber dari blok ADC ,sensor infra merah, dan keypad. Perancangan ADC memiliki 8 bit data dan dan 1 buah bit kontrol. Ke-8 bit data masuk pada port P1.0 sampai P1.7, sedangkan pin kontrolnya ditempatkan pada P2.6. Penanganan keypad membutuhkan 7 buah port mikrokontroller yang kesemuanya dikontrol pada port P3.0 sampai P3.6. Selain itu mikrokontroller juga menerima inputan yang bersumber dari 2 buah rangkaian penerima inframerah, melalui port P2.1, dan P2.2.

Mikrokontroller ini juga melakukan kontrol pada bagian output yaitu Display yang berupa LCD M1632 dan rangkaian driver-driver beban. Rangkaian Display

membutuhkan 8 bit data dan 2 bit kontrol (RS,E). Delapan bit data dikontrol pada P1.0 sampai P1.7, sedangkan ke-2 bit kontrol dilakukan oleh P2.4 dan P2.5.

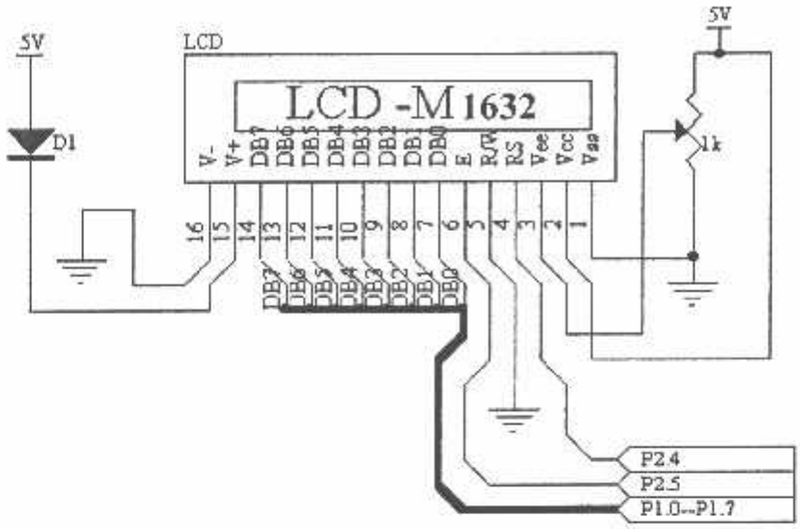
Output lain dari rangkaian mikrokontroller adalah beberapa output driver beban, yaitu : pemanas, pengepres, sentrallock sebagai pembuka kran, dan motor konveyor. Untuk lebih jelasnya perancangan unit mikrokontroller AT89S8252, dijelaskan sebagai berikut:



Gambar 3.7. Perancangan Unit pengontrol Mikrokontroller AT89S8252.
* Sumber : Perancangan

3.2.5. Display

Display digunakan untuk menampilkan berat gula yang akan ditimbang dan jumlah gula yang ingin diproses. Perancangan display digunakan sebuah LCD M1632 yang dapat menambilkan 32 karakter dalam 16 kolom dan 2 baris. Perancangan bagian display digambarkan sebagai berikut :

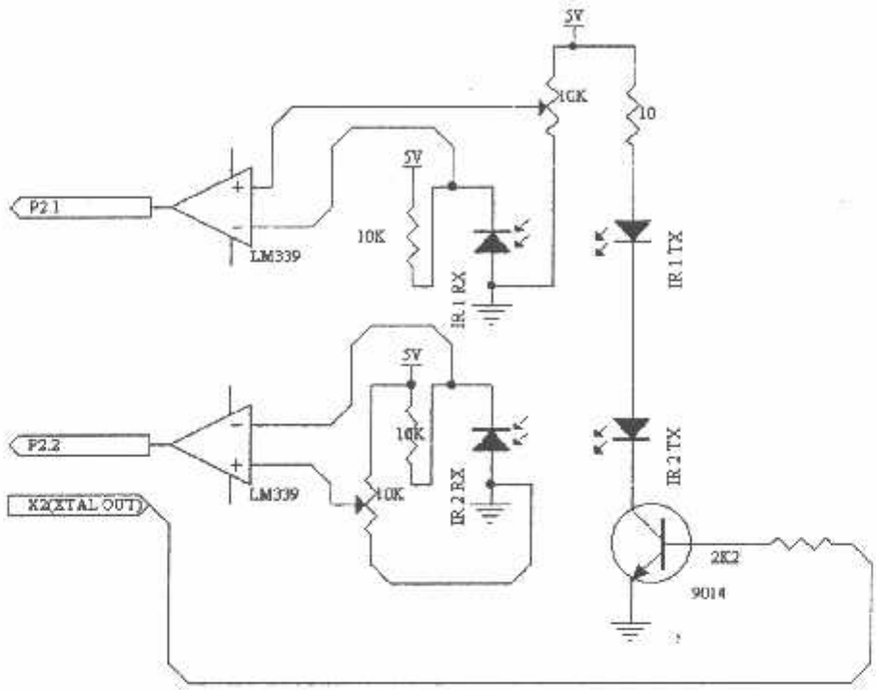


Gambar 3.8. Perancangan rangkaian LCD
* Sumber : Perancangan

Dari Gambar 3.8 diatas pin data dikontrol oleh P1.0...P1.7 dari mikrokontroller. Sedangkan pin kontrol LCD yaitu RS dan E, dikontrol oleh pin P2.4, dan P2.5. Penggunaan nilai Vr sebesar 1 K merupakan ketetapan dari *datasheet book* dan Diode (germanium) pada pin 15 (Vcc +), bertujuan sebagai pengurang tegangan sebesar 0,7 volt.

3.2.6. Rangkaian Sensor Infra Merah

Rangkaian sensor infra merah berfungsi untuk mendeteksi keberadaan kantung gula. sehingga sistem dapat mengetahui kapan proses pengisian kantung gula dan waktu pengepresan terjadi. Rangkaian infra merah ini terdiri dari 2 buah led infra merah sebagai pemancar inframerah dan 2 buah photo diode sebagai penerima infra merah. Gambar perancangan rangkaian infra merah adalah sebagai berikut :



Gambar 3.9. Perancangan rangkaian sensor infra merah
* Sumber : Perancangan

Pada perancangan diatas, rangkaian sensor inframerah terdiri dari 2 buah pengirim dan 2 buah penerima. Rangkaian pemancar bersumber dari 2 buah led pemancar infra merah yang dirangkai seri dan di driver melalui transistor 9014. kontrol rangkaian pemancar dilakukan oleh x2, yang berarti mempunyai frekuensi sebesar 12Mhz. Penjelasan mengenai perhitungan driver pemancar infra merah adalah sebagai berikut :

$$R_c = \frac{Vcc - 2V\,\text{inf}\,merah}{2I\,\text{inf}\,merah}$$

$$R_c = \frac{5 - 2(1{,}5)}{2(100mA)}$$

$$R_c = \frac{2}{200mA}$$

$$R_c = 10ohm$$

Dengan demikian nilai Rc yang digunakan adalah sebesar 10 ohm.

Nilai Rb dapat di cari sebagai berikut :

$$I_b = \frac{I_c}{hfe}$$
$$I_b = \frac{100mA}{200}$$
$$I_b = 0{,}5mA$$

agar transistor dapat mengalami kondisi hard saturasi nilai $I_{b\,max}$ yang berikan harus 10 kali lebih tinggi dari nilai I_b

$$I_{b\max} = 10 \times I_b$$
$$I_{b\max} = 10 \times 0{,}5mA$$
$$I_{b\max} = 5mA$$

$$R_{b\min} = \frac{V_{in} - V_{BE}}{I_{b\max}}$$
$$R_{b\min} = \frac{4{,}7 - 0{,}7}{5mA}$$
$$R_{b\min} = \frac{4}{5mA}$$
$$R_{b\min} = 800ohm$$

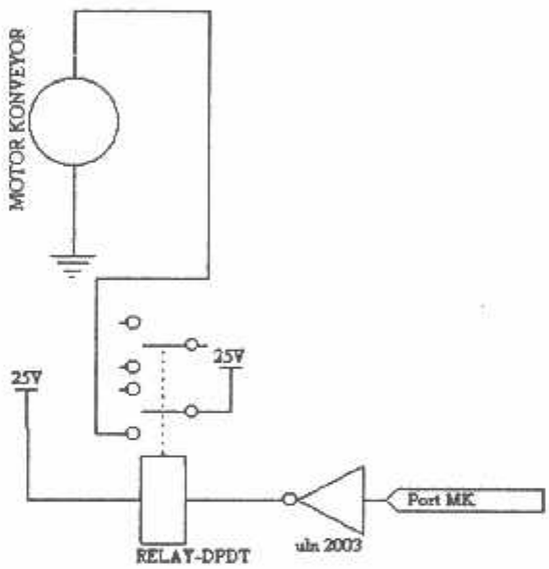
Dengan nilai $R_{b\,min}$ sebesar 800 ohm dan nilai $R_{b\,max}$ adalah 10 kali $R_{b\,min}$ maka dipilih nilai nilai Rb sebesar 2K2 ohm.

Sedangkan perancangan penerima infra merah, terdiri dari photo diode dan sebuah resistor pul-up. Photo diode mempunyai sifat yang hambatannya akan turun jika menerima cahaya inframerah. Perubahan resistansi yang terjadi akan menyebabkan perubahan tegangan. Dan perubahan tegangan ini akan dibandingkan dengan tegangan referensi dari IC LM339. untuk merubah menjadi logika high atau low.

3.2.7. Rangkaian Driver

Rangkaian driver berfungsi untuk memperkuat logika yang terdapat pada mikrokontroller sehingga mampu untuk menggerakkan beban yang di inginkan. Rangkaian driver disini dibedakan menjadi 2 buah yaitu driver yang pembalik polaritas dan driver switch.

Driver switch terdiri dari 1 buah relay dan 1 buah driver relay. Schingga driver switch dapat menerima logika dari pin mikrokontroller dan meneruskan logika tersebut pada beban yang dimaksud. Gambar driver switch adalah sebagai berikut:

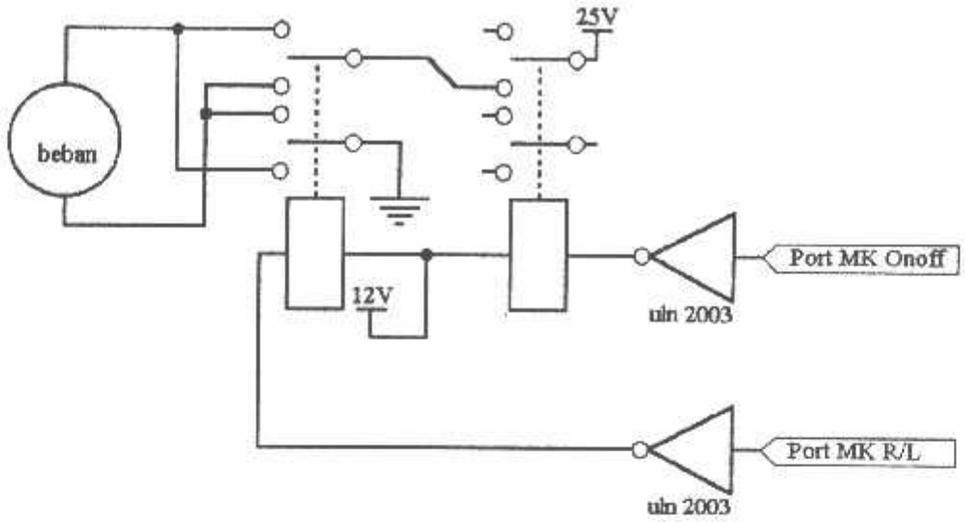


Gambar 3.10. Rangkaian driver switch

* Sumber : Perancangan

Driver switch digunakan untuk melakukan pengontrolan pada beban motor konveyor, pemanas, dan buzzer.

Sedangkan driver pembalik polaritas memiliki dua buah input untuk mengontrol arah gerak beban dan untuk mengaktif atau non aktif beban. Perancangan driver pembalik polaritas adalah sebagai berikut:



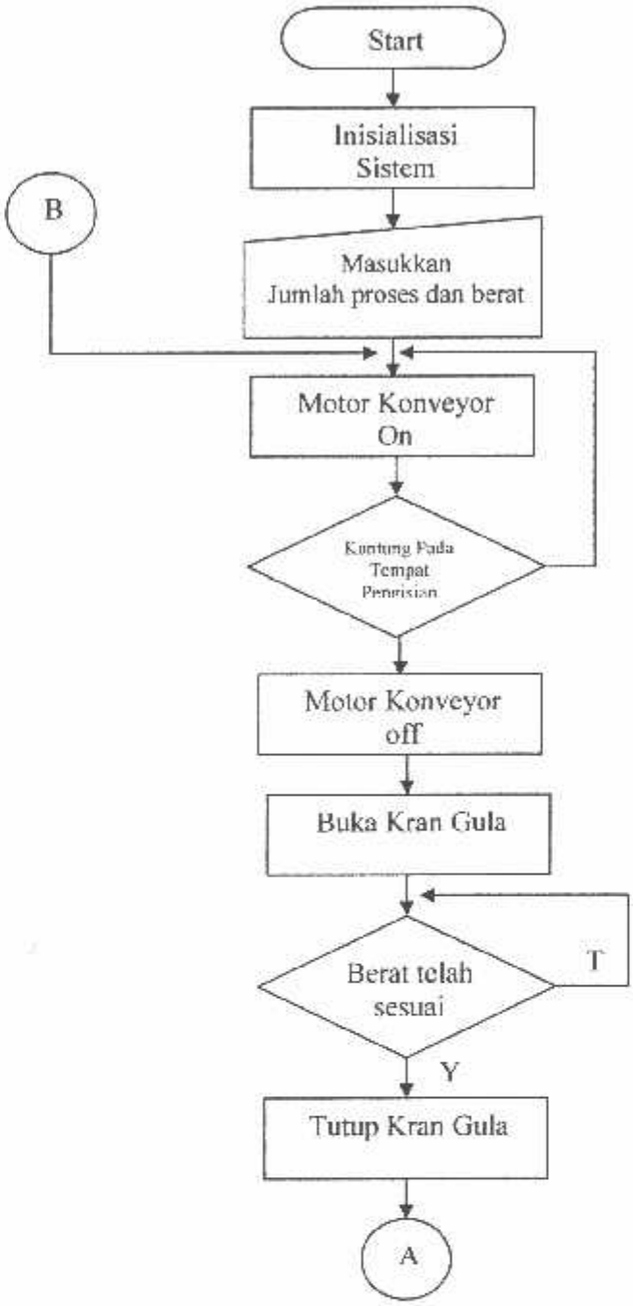
Gambar 3.11. Rangkaian driver pembalik polaritas

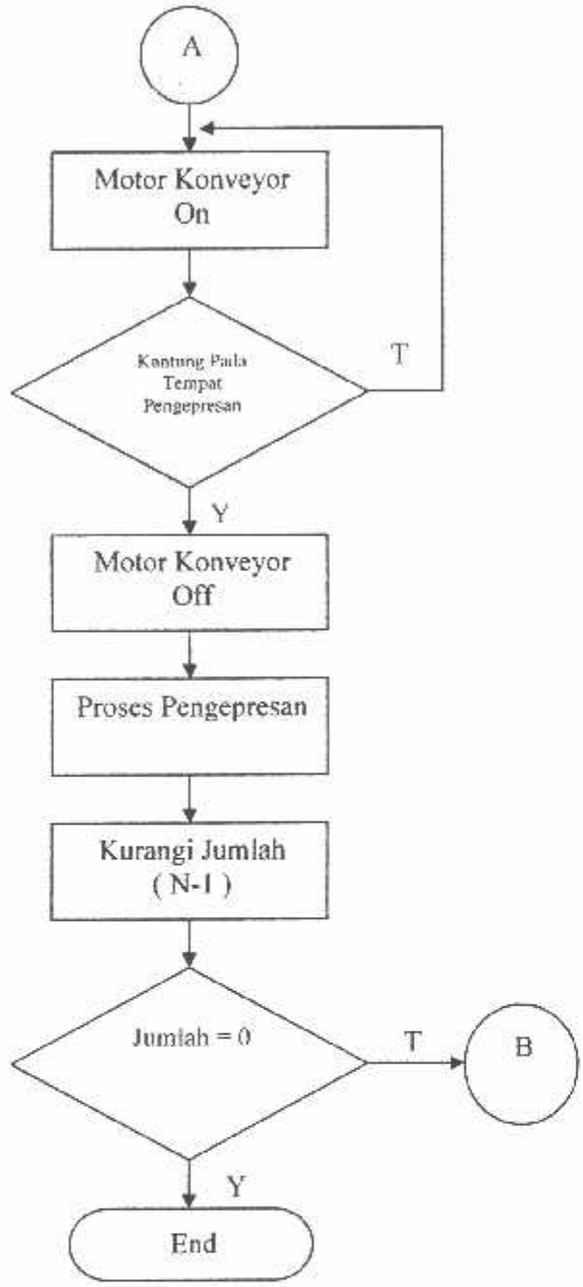
* Sumber : Perancangan

Beban yang membutuhkan pengontrolan driver pembalik polaritas adalah motor pengepres, dan motor sentral lock.

3.2.8. Flowchart Alat

Dengan perancangan sistem mekanis dan sistem kontrol elektris yang diterapkan pada alat, agar alat dapat bekerja sesuai dengan yang diinginkan maka algoritma perancangan software alat digambarkan berdasarkan flowchart sebagai berikut :


Start
Inisialisasi Sistem
B
Masukkan Jumlah proses dan berat
Motor Konveyor On
Kantung Pada Tempat Pengisian
Motor Konveyor off
Buka Kran Gula
Berat telah sesuai
T
Y
Tutup Kran Gula
A



Gambar 3.12 Diagram Alir Sistem

BAB IV

PENGUJIAN DAN ANALISA ALAT

4.1. Umum

Pengujian alat ini dilakukan untuk mengetahui kinerja dari keseluruhan sistem rangkaian. Jadi pada tahap ini akan diketahui nilai-nilai serta parameter-parameter dari setiap bagian yang menyusun sistem secara keseluruhan.

4.2. Pengujian Rangkaian Mikrokontroller

4.2.1. Tujuan

Tujuan dari pengujian rangkaian mikrokontroller ini adalah untuk mengetahui apakah rangkaian yang telah dirancang dapat bekerja sesuai dengan yang direncanakan.

4.2.2. Alat dan Bahan

1. Power Supply
2. 8 buah LED peraga
3. Downloader AT89S8252
4. Rangkaian Mikrokontroller AT89S8252

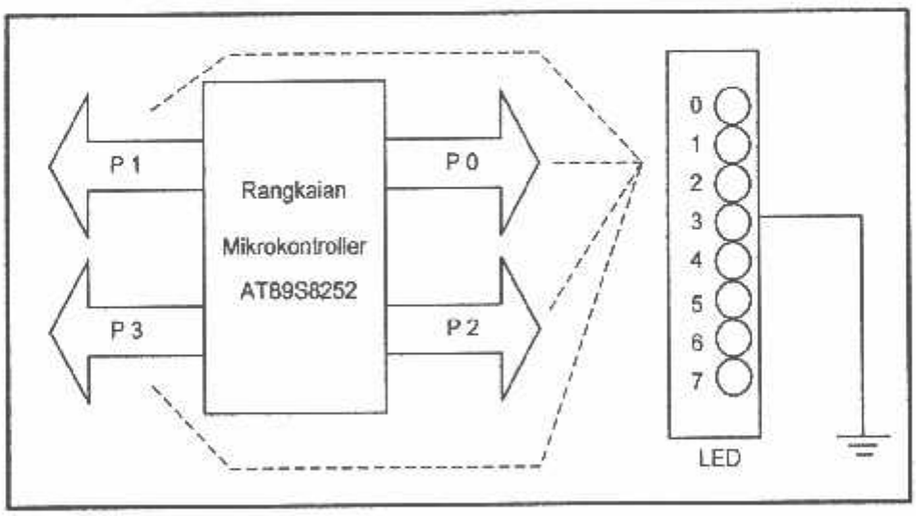
4.2.3. Langkah Pengujian

1. Merancang Software Pengujian sebagai berikut :

```
        org     0H
Mulai:  mov     P1,#0FH         ;kondisi satu
        call    Delay
        mov     P1,# 0F0H       ;kondisi dua
```

```
        call    Delay
        jmp     Mulai
Delay:  mov     R0,#0
Delay1: mov     R5,#50H
        djnz    R5,$
        djnz    R0,Delay1
        end
```

2. Melakukan load software pada langkah 1 kedalam Mikrokontroller AT89S8252 dengan bantuan komputer dan downloader AT89S8252.
3. Mempersiapkan blok pengujian seperti pada gambar 4 – 1.
4. Mengaktifkan sistem mikokontroller, display LED, dan memasang catu daya sebesar 5 volt serta mengamati hasil nyala LED.



Gambar 4.1. Blok Diagram Pengujian Rangkaian Mikrokontroler AT89S8252

* Sumber : Pengujian

Pada pengujian ini led"0" di umpamakan sebagai motor konveyor,led"1 dan 2" sebagai central lock,led "3dan4" sebagai motor pengepres dan led "5" sebagai buzzer.

4.3. Pengujian Rangkaian Keypad

4.3.1. Tujuan

Tujuan dari pengujian rangkaian keypad ini adalah untuk mengetahui apakah rangkaian keypad dapat bekerja sesuai dengan yang direncanakan.

4.3.2. Alat dan Bahan

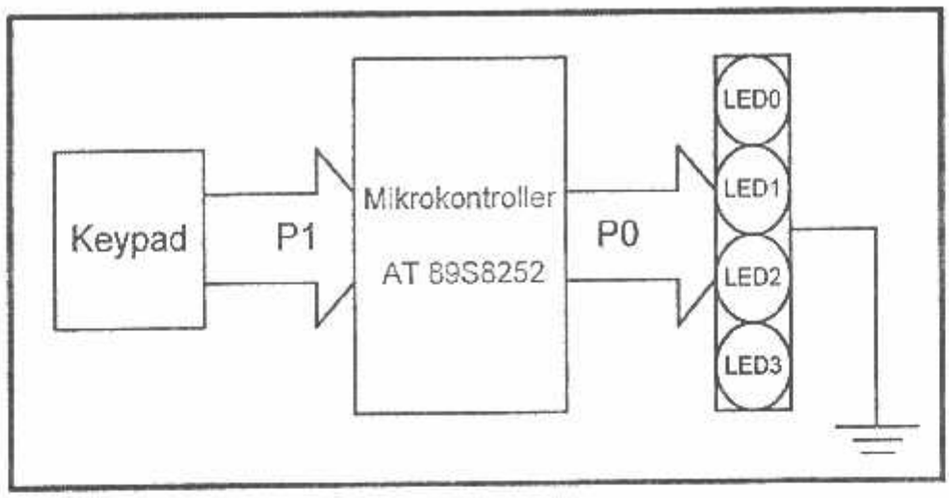
1. Power Supply
2. 4 buah LED peraga
3. Downloader AT89S8252
4. Rangkaian Keypad dan Mikrokontroller AT89S8252
5. Software proses scaning keypad 3 X 4 yang telah dirancang (Software ini dapat dilihat pada lampiran program baris 704 - 830)

4.3.3. Langkah Pengujian

1. Mempersiapkan dan melakukan download software pengujian keypad sebagai berikut :

```
ULANG:
        LCALL   AMBIL_KEYPAD
        MOV     R4,HASIL_KEYPAD
        CJNE    R4,#'N',DITEKAN
        JMP     ULANG
DITEKAN:
        MOV     P1,R4
        JMP     ULANG
        END
```

2. Mempersiapkan blok pengujian seperti pada gambar 4 – 2.
3. Menekan tombol keypad dan mengamati kondisi nyala LED.



Gambar 4.3. Blok Diagram Pengujian Keypad
* Sumber : Pengujian

4.3.4. Hasil dan Analisa

Setelah melakukan pengujian sesuai dengan langkah – langkah pengujian diatas didapatkan hasil pengujian seperti dalam tabel 4 – 2 :

Tabel 4.2. Hasil Pengujian Keypad

TOMBOL	LED 3	LED 2	LED 1	LED 0
1	on	on	on	off
2	on	on	off	on
3	on	on	off	off
4	on	off	on	on
5	on	off	on	off
6	on	off	off	on
7	on	off	off	off
8	off	on	on	on
9	off	on	on	off
*	off	on	off	on
0	off	on	off	off
#	off	off	on	on

Sumber : Pengujian

Pemasangan LED pada pengujian diatas menggunakan common anoda, schingga LED akan menyala jika port mikrokontroller berlogika rendah. Dengan memperhatikan kombinasi nyala LED pada saat tombol 2 ditekan, nilai biner yang yang ditunjukkan adalah 0010, dan pada saat tombol 6 ditekan nilai biner yang ditunjukkan 0110. Dengan demikian kombinasi nyala LED tersebut telah mewakili penekanan tiap tombol keypad yang dirancang.

4.4. Pengujian Rangkaian LCD

4.4.1. Tujuan

Tujuan dari pengujian rangkaian LCD ini adalah untuk mengetahui apakah rangkaian display (LCD) yang telah dirancang dapat bekerja sesuai dengan yang direncanakan.

4.4.2. Alat dan Bahan

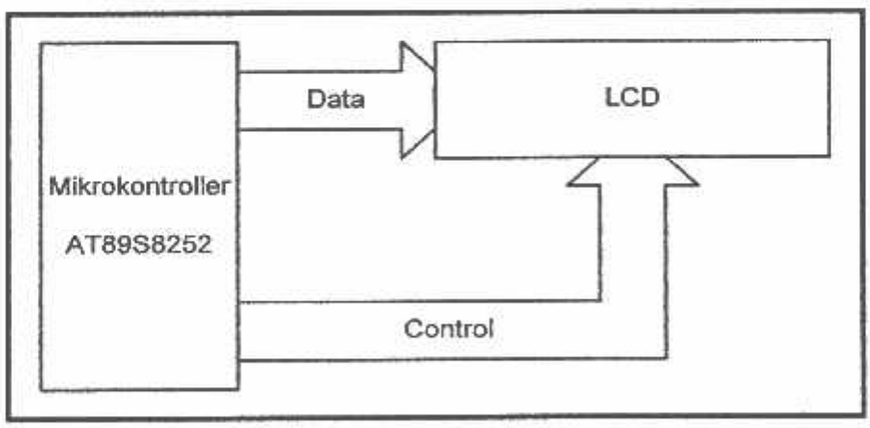
1. Data Sheet LCD type M1632
2. Rangkaian LCD
3. Rangkaian Mikrokontroller AT89S8252
4. Downloader AT89S8252
5. Power Supply
6. Software Pemanfaatan LCD, dari proses inisialisasi hingga proses penulisan suatu string ke LCD. (Program ini dapat dilihat pada lampiran program pada baris 480 sampai baris 702)

4.4.3. Langkah Pengujian

1. Mempersiapkan software Pemanfaatan LCD. Program ini terdapat pada program keseluruhan. Adapun software pemanfaatan dari LCD adalah sebagai berikut :

```
        LCALL   INISIALISASI_LCD
        MOV     BARIS,#1
        MOV     KOLOM,#0
        LCALL   TEMPATKAN_KURSOR
        MOV     DPTR,#COBA_LCD
        LCALL   TULIS_STRING
        JMP $
COBA_LCD:   DB ' COBA LCD '
        END
```

2. Mengisi mikrokontroller AT89S8252 dengan software yang telah dipersiapkan diatas menggunakan downloader AT89S8252.
3. Mempersiapkan rangkaian pengujian seperti pada Blok diagram pengujian LCD pada gambar 4 – 4.
4. Menghubungkan rangkaian dengan power supply.
5. Mengamati hasil pengujian LCD.



Gambar 4.4. Blok Diagram Pengujian LCD
* Sumber : Pengujian

4.4.4. Hasil dan Analisa

Setelah melakukan pengujian LCD diatas, dari hasil pengujian didapatkan bahwa rangkaian LCD dapat menampilkan karakter-karakter, sesuai dengan data yang dikirimkan. Tampilan berupa tulisan " COBA LCD " pada baris pertama LCD, dari hasil pengujian diatas menandakan bahwa proses penulisan ke LCD berhasil dilakukan dengan benar.

Gambar 4.5. Foto hasil pengujian LCD

4.5. Pengujian Rangkaian Sensor Berat

4.5.1. Tujuan

Tujuan dari pengujian rangkaian sensor berat ini adalah untuk mengetahui apakah sensor berat yang dirancang dapat bekerja sesuai dengan yang direncanakan.

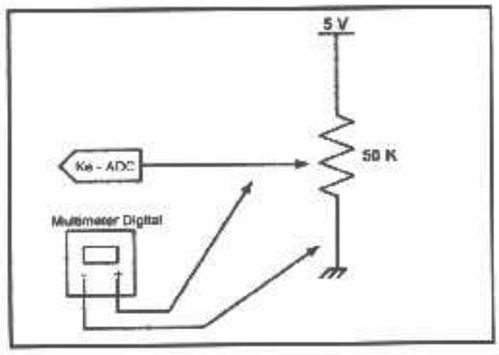
4.5.2. Alat dan Bahan

1. Power Supply
2. Digital Multimeter
3. Beban Berat

4.5.3. Langkah Pengujian

1. Melakukan pembebanan pada sensor berat yang telah dirancang.

2. Mengamati nilai tegangan (V) disensor pada multimeter digital dan memasukkan hasilnya kedalam tabel 4 – 3.
3. Mengulangi langkah 1 dan 2 untuk beban yang berbeda.



Gambar 4.6. Blok Diagram Pengujian Sensor Berat
* Sumber : Pengujian

4.5.4. Hasil dan Analisa

Dari pengujian sensor berat diatas dengan melakukan pembebanan acak, hasil yang diperoleh adalah sebagi berikut :

4.5.4. Hasil dan Analisa

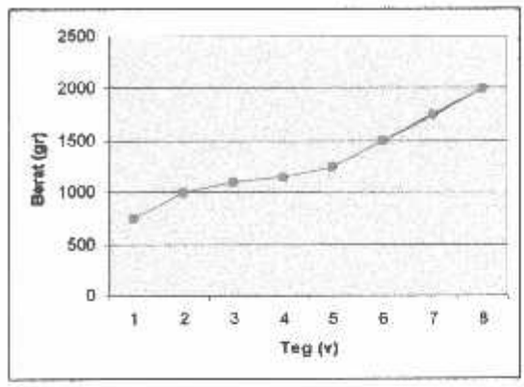
Dari pengujian sensor berat diatas dengan melakukan pembebanan acak, hasil yang diperoleh adalah sebagi berikut :

Tabel 4.3. Hasil Pengujian Sensor Berat

No	Berat (gram)	Tegangan (V) pada sensor (Volt)
1	750	0,76
2	1000	1,03
3	1100	1,14
4	1150	1,19
5	1250	1,28
6	1500	1,52
7	1750	1,79
8	2000	2,08

Sumber : Pengujian

(a).



(b).

Gambar 4.7.

a. Foto hasil pengujian linieritas sensor berat pada beban 1000 gram

b. Grafik linieritas sensor berat

4.6. Pengujian Rangkaian ADC0804

4.6.1. Tujuan

Tujuan dari pengujian rangkaian ADC 0804 ini adalah untuk mengetahui apakah rangkaian ADC dapat bekerja sesuai dengan yang direncanakan.

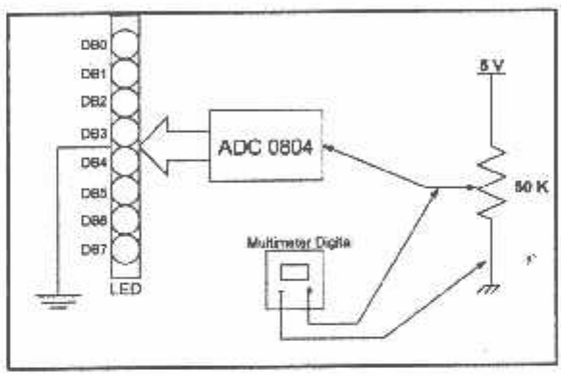
4.6.2. Alat dan Bahan

1. Power Supply
2. Sensor Berat
3. Digital Multimeter
4. Rangkaian ADC 0804 yang akan diuji
5. 8 LED peraga

4.6.3. Langkah Pengujian

1. Menghubungkan pin – pin keluaran ADC 0804 dengan rangkaian LED.

2. Menghubungkan rangkaian pengujian ADC 0804 dengan tegangan power supply 5 Volt DC.
3. Memberikan tegangan input ADC 0804 yang bervariasi (hasil dari tegangan keluaran pada sensor berat).
4. Mengamati nyala LED dan memasukkan hasilnya kedalam tabel 4 – 4.



Gambar 4.8. Blok Diagram Pengujian ADC 0804
* Sumber : Pengujian

4.6.4. Hasil dan Analisa

Dari pengujian ADC 0804 hasil yang diperoleh adalah sebagai berikut :

Tabel 4.4. Hasil Pengujian ADC 0804

No	Input Analog (Volt)	OUTPUT DIGITAL ADC 0804								DEC
		DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	
1	0,76	0	1	0	0	1	1	0	0	76
2	1,03	0	1	1	0	0	1	1	1	103
3	1,14	0	1	1	1	0	0	1	0	114
4	1,19	0	1	1	1	0	1	1	1	119
5	1,28	1	0	0	0	0	0	0	0	128
6	1,52	1	0	0	1	1	0	0	0	152
7	1,79	1	0	1	1	0	0	1	1	179
8	2,08	1	1	0	1	0	0	0	0	208

Sumber : Pengujian

Pengukuran ke-1 : $Vin = \frac{76}{255} \times 2{,}6 \text{ Volt} = 0{,}774 \text{ Volt}$

$= 0{,}77 \text{ Volt}$

$\%E = \frac{0{,}77 - 0{,}76}{0{,}77} \times 100\% = 1{,}29\ \%$

Pengukuran ke-2 : $Vin = \frac{103}{255} \times 2{,}6 \text{ Volt} = 1{,}050 \text{ Volt}$

$\%E = \frac{1{,}05 - 1{,}03}{1{,}05} \times 100\% = 1{,}90\ \%$

Pengukuran ke-3 : $Vin = \frac{114}{255} \times 2{,}6 \text{ Volt} = 1{,}162 \text{ Volt}$

$= 1{,}16 \text{ Volt}$

$\%E = \frac{1{,}16 - 1{,}14}{1{,}16} \times 100\% = 1{,}72\ \%$

Pengukuran ke-4 : $Vin = \frac{119}{255} \times 2{,}6 \text{ Volt} = 1{,}213 \text{ Volt}$

$= 1{,}21 \text{ Volt}$

$\%E = \frac{1{,}21 - 1{,}19}{1{,}21} \times 100\% = 1{,}65\ \%$

Pengukuran ke-5 : $Vin = \frac{128}{255} \times 2{,}6 \text{ Volt} = 1{,}305 \text{ Volt}$

$= 1{,}30 \text{ Volt}$

$\%E = \frac{1{,}30 - 1{,}28}{1{,}30} \times 100\% = 1{,}53\ \%$

Pengukuran ke-6 : $Vin = \frac{152}{255} \times 2{,}6 \text{ Volt} = 1{,}549 \text{ Volt}$

$= 1{,}55 \text{ Volt}$

$$\%E = \frac{1,55 - 1,52}{1,55} \times 100\ \% \quad = 1,93\ \%$$

Pengukuran ke-7 : $Vin = \frac{179}{255} \times 2,6$ Volt $= 1,825$ Volt

$= 1,82$ Volt

$$\%E = \frac{1,82 - 1,79}{1,82} \times 100\ \% \quad = 1,64\ \%$$

Pengukuran ke- 8 : $Vin = \frac{208}{255} \times 2,6$ Volt $= 2,120$ Volt

$$\%E = \frac{2,12 - 2,08}{2,12} \times 100\ \% \quad = 1,88\ \%$$

$$\%E \text{ rata} - \text{rata} = \frac{\Sigma(\%KesalahanPengukuran)}{BanyaknyaData}$$

$$\%E \text{ rata} - \text{rata} = \frac{1,29 + 1,90 + 1,72 + 1,65 + 1,53 + 1,93 + 1,64 + 1,88}{8}$$

$$= \frac{13,54}{8} = 1,692\ \%$$

Sehingga dapat diperoleh kesalahan rata-ratanya sebesar 1,692 %

Jadi untuk pengujian rangkaian ADC 0804 ini presentasi ketelitiannya adalah :

Presentasi Ketelitian $= 100\ \% - 1,692\ \%$

$= 98,30\ \%$

Setelah melakukan pengujian sistem timbangan diatas maka dengan melihat hasil pengujian dapat disimpulkan dalam pengisian gula seberat 1000gram dibutuhkan waktu selama 15 detik dan untuk 1500 gram dibutuhkan waktu selama 24 detik. Sehingga rangkaian sistem timbangan digital dapat bekerja sebagaimana yang di harapkan.

4.7. Pengujian Sistem Timbangan Digital

4.7.1. Tujuan

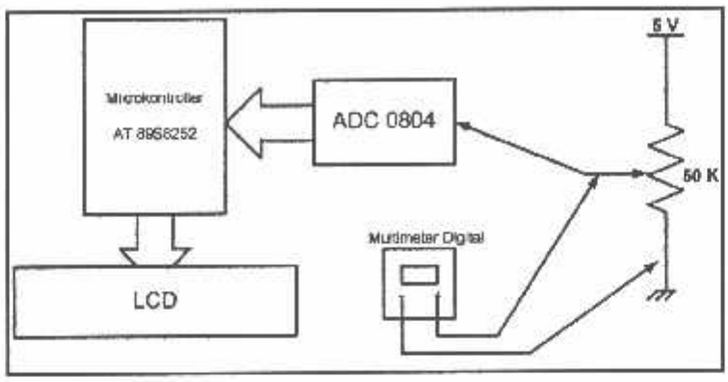
Tujuan pengujian ini adalah untuk membandingkan hasil pengukuran timbangan digital dengan timbangan konvensional. Pengujian ini dilakukan beberapa kali untuk mengetahui error rata – rata sistem.

4.7.2. Alat dan Bahan

1. Power Supply
2. Sensor Berat
3. Rangkaian ADC 0804
4. Rangkaian Mikrokontroller AT89S8252
5. LCD M1632
6. Digital Multimeter

4.7.3. Langkah Pengujian

1. Melakukan penimbangan secara kovensional dan mencatat hasilnya kedalam tabel 4 – 5.
2. Menghubungkan Rangkaian Sensor Berat dan ADC 0804 dengan rangkaian Mikrokontroller AT89S8252 dan LCD.
3. Menghubungkan keseluruhan rangkaian diatas dengan power supply.
4. Melakukan pembebanan pada sensor berat sesuai dengan berat yang telah diukur atau ditimbang secara konvensional dan mencatat hasilnya kedalam tabel 4 – 5.



Gambar 4.9. Blok Diagram Pengujian Sistem Timbangan Digital
+ Sumber : Pengujian

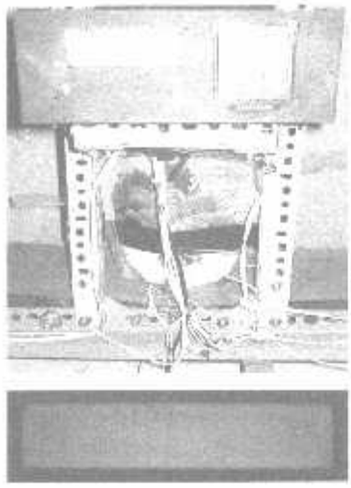
4.7.4. Hasil dan Analisa

Dari pengujian sistem timbangan digital diperoleh hasil sebagai berikut :

Tabel 4.3. Hasil Pengujian Perbandingan Timbangan Digital dan Timbangan Konvensional

No	DISPLAY TIMBANGAN	
	Timbangan Konvensional (gram)	Timbangan Digital (gram)
1	760	750
2	1030	1000
3	1140	1100
4	1190	1150
5	1280	1250
6	1520	1500
7	1790	1750
8	2080	2000

Sumber : Pengujian



Gambar 4.10. Foto hasil pengujian timbangan digital dan konvensional

Dari data diatas dapat dicari persentasi kesalahannya yaitu dengan menggunakan rumus :

$$\%E = \frac{(x-y)}{x} x100\% \quad \text{..... (4.2)}$$

dengan : %E = persentasi kesalahan

x = berat timbangan konvensional

y = berat timbangan digital

1. $\%E = \frac{(760-750)}{760} x100\%$

$= \frac{10}{760} x100\%$

$= 1.3\ \%$

2. $\%E = \frac{(1030-1000)}{1030} x100\%$

$= \frac{30}{1030} x100\%$

$= 2{,}91\ \%$

3. $\%E = \frac{(1140-1100)}{1140} x100\%$

$= \frac{40}{1140} x100\%$

$= 3,5\ \%$

4. $\%E = \frac{(1190-1150)}{1190} x100\%$

$= \frac{40}{1190} x100\%$

$= 3,4\ \%$

5. $\%E = \frac{(1280-1250)}{1280} x100\%$

$= \frac{30}{1280} x100\%$

$= 2,3\ \%$

6. $\%E = \frac{(1520-1500)}{1520} x100\%$

$= \frac{20}{1520} x100\%$

$= 1,3\ \%$

7. $\%E = \frac{(1790-1750)}{1790} x100\%$

$= \frac{40}{1790} x100\%$

$= 2,2\ \%$

8. $\%E = \frac{(2080-2000)}{2080} x100\%$

$= \frac{80}{2080} x100\%$

$= 3,8\ \%$

$\sum \%E = 1,3+2,9+3,5+3,4+2,3+1,3+2,2+3,8$

$= 20,71$

Sehingga dapat diperoleh kesalahan rata-ratanya :

$$\frac{\sum \%E}{n} = \frac{(20,71)\%}{8}$$

$$= 2,588\ \%$$

Untuk persentasi ketelitian rata – ratanya $= 100\ \% - 2,588\ \%$

$= 97,412\ \%$

Setelah melakukan pengujian sistem timbangan diatas maka dengan melihat hasil pengujian dapat disimpulkan bahwa rangkaian sistem timbangan digital dapat bekerja sesuai yang direncanakan

4.8. Pengujian Motor DC

4.8.1. Tujuan

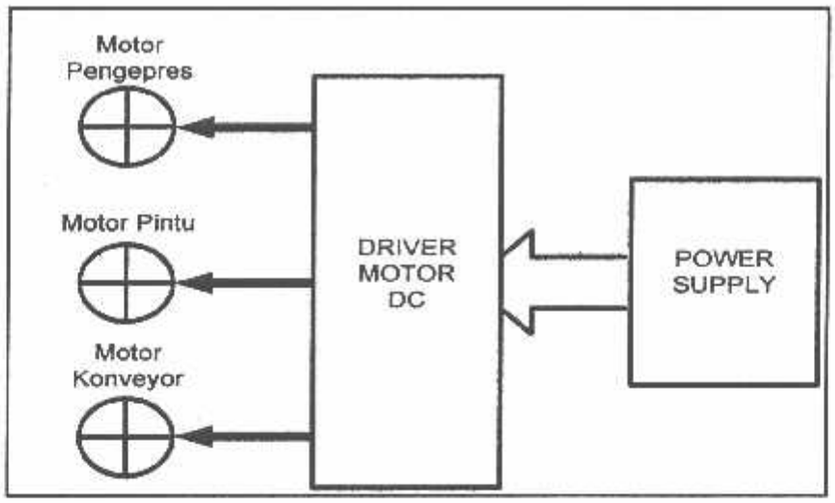
Tujuan dari pengujian ini adalah untuk mengetahui arah putaran motor dc sekaligus apakah driver motor dc dapat bekerja sesuai dengan yang direncanakan.

4.8.2. Alat dan Bahan

1. Power Supply 24 Volt untuk motor dc,12 Volt untuk driver motor dc, 5 Volt untuk input driver High dan 0 Volt untuk input driver Low,
2. Rangkaian driver motor dc.
3. Motor DC.

4.8.3. Langkah Pengujian

1. Menghubungkan motor dc dengan rangkaian driver motor dc.
2. Menghubungkan motor dc dengan power supply 24 Volt DC.
3. Menghubungkan VCC driver motor dc dengan power supply 12 Volt DC.
4. Menghubungkan input driver motor dc dengan power supply 5 Volt DC.
5. Menghubungkan input driver motor dc dengan power supply 0 Volt DC.
6. Memberikan inputan driver motor dc seperti pada langkah 4 dan 5 secara bervariasi dan mengamati arah putarannya lalu memasukkan hasilnya ke dalam tabel 4 – 6.



Gambar 4.11. Blok Diagram Pengujian Motor DC
* Sumber : Pengujian

4.8.4. Hasil dan Analisa

Dari pengujian motor dc dapat diperoleh data sebagai berikut :

Tabel 4.6. Hasil Pengujian Motor DC

Motor DC	Input Driver		Kondisi relay		Kondisi Motor
	In 1	In 2	R 1	R 2	
Pengepres	L	H	Off	On	Diam
	L	L	Off	Off	Diam
	H	L	On	Off	Berputar searah jarum jam
	H	H	On	On	Berlawan arah jarum jam
Pintu gula (central lock)	L	H	Off	On	Diam
	L	L	Off	Off	Diam
	H	L	On	Off	Berputar searah jarum jam
	H	H	On	On	Berlawan arah jarum jam

* Sumber : Pengujian

Tabel 4.7. Hasil Pengujian Motor DC konveyor

Motor DC	Input Driver	Kondisi relay	Kondisi Motor
Konveyor	H	Off	Diam
	L	On	Berputar searah jarum jam

* Sumber : Pengujian

Pada proses pengepresan di gunakan motor DC untuk menggerakkan kawat pemanas dengan lama pengepresan 10 detik. Dengan melihat tabel diatas dapat disimpulkan bahwa rangkaian motor dc dapat bekerja sebagaimana mestinya sesuai dengan yang direncanakan.

4.9. Pengujian Rangkaian Sensor *Infra Red*

4.9.1. Tujuan

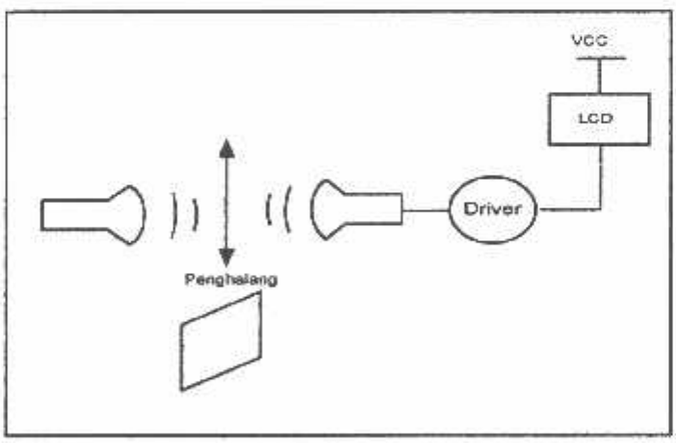
Pengujian *Infra Red* ini bertujuan untuk mengetahui bagaiamana kondisi *Infra Red* pada saat rangkaian ini digunakan sebagai sensor

4.9.2. Alat dan Bahan

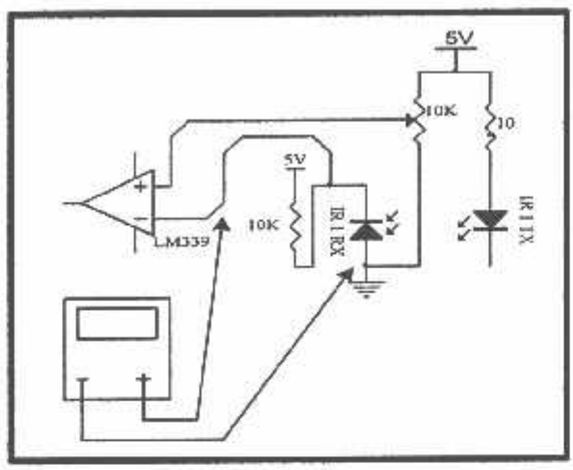
1. Power Supply 5 Volt DC.
2. Rangkaian *Infra Red* yang akan diuji.

4.9.3. Langkah Pengujian

1. Membuat rangkaian pengujian seperti blok diagram dibawah ini :



Gambar . 4.12. Blok Diagram Pengujian Rangkaian Infra Red
* Sumber : Pengujian



Gambar. 4.13. Pengujian Infra Red

2. Menghubungkan rangkaian *Infra Red*, driver dan LCD dengan power supply 5 Volt DC.
3. Menghalangi *Infra Red* dengan penghalang dan mencatat hasilnya kedalam tabel 4 – 8.
4. Melepas penghalang dan mencatat hasilnya kedalam tabel 4 – 8.

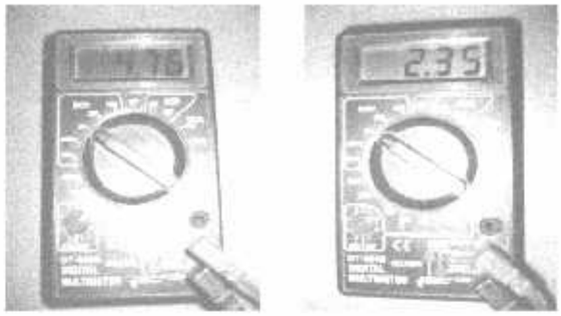
4.9.4. Hasil dan Analisa

Setelah melakukan pengujian sensor *infra red* maka hasil yang didapatkan adalah sebagai berikut :

Tabel 4.8. Hasil Pengujian Sensor Infra Red

Kondisi Sensor	V Out Sensor (Volt)
Terhalang	4,76
Tak Terhalang	2,35

Sumber : Pengujian



Gambar. 4.14. Foto hasil pengukuran

Dengan mengetahui kondisi sensor *infra red* maka dapat disimpulkan bahwa rangkaian sensor infra red dapat bekerja sebagaimana mestinya sesuai dengan yang direncanakan.

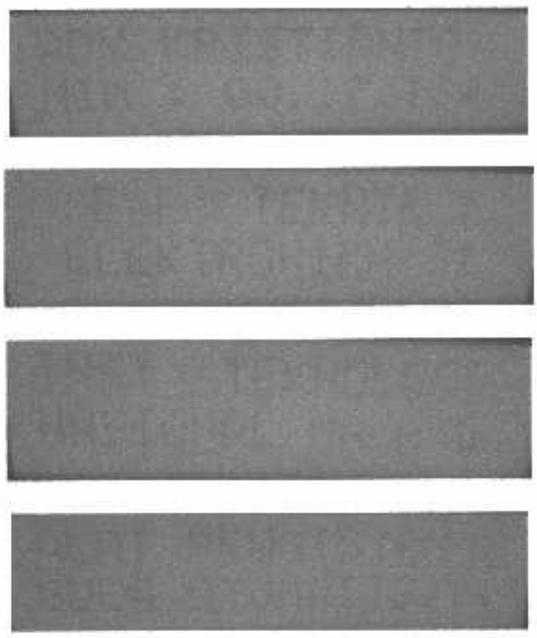
4.10. Pengujian Perangkat Lunak

Program yang digunakan ialah program *assembly*. Pengujian program *assembly* ini dilakukan pada saat mengkompile program sumber *assembly*, yang merupakan kumpulan baris-baris perintah dan telah disimpan dengan *extention* .ASM. Program ini ditulis menggunakan UltraEdit-32 yang dihubungkan langsung dengan HB2000W *Programmer & Evaluation Board For* AT89S/C/51/52. Pada bagian proses *assembly*, program .ASM akan dikompile menjadi dua bagian, yaitu *listing assembly* *.LST dan program obyek *.HEX yang berisikan kode-kode yang hanya dikenali mikrokontroller. Program inilah yang akan di*download*kan ke mikrokontroller.

4.11. Pengujian Sistem Keseluruhan

Pada bagian ini komponen – komponen yang telah diuji sebelumnya seperti Keypad, LCD, Sensor Berat, Driver Motor DC,Motor DC, Sensor *Infra*

Red dan Mikrokontroller dihubungkan sesuai dengan perancangan sistem. Tampilan awal dalam pengujian sistem ini berupa tampilan pada LCD sebagai berikut:



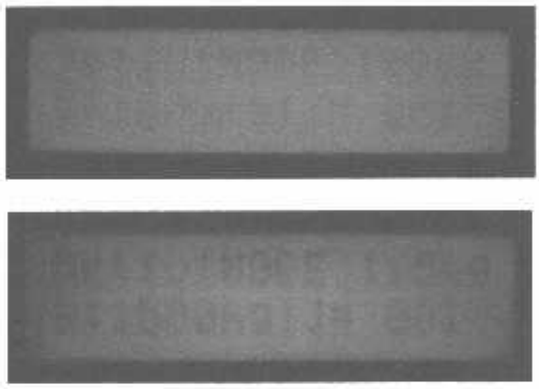
Gambar. 4.15. Tampilan Awal Pada LCD

Dalam pengujian ini untuk melakukan pengesetan yaitu dengan menekan tombol pada keypad dan akan tampil pada unit tampilan menu utama yang terdiri dari berat gula pasir yang ingin ditimbang. Tampilan pada LCD seperti pada gambar berikut :

Gambar. 4.16. Tampilan Awal Perintah Pengisian Berat

Gambar. 4.17. Tampilan jumlah yang diinginkan

Setelah proses pengesetan selesai maka selanjutnya melakukan set untuk menjalankan sistem yaitu dengan menekan tanda (#) pada keypad. Pada proses selanjutnya pada LCD akan ditampilkan berat yang diinginkan dan berat aktual pada saat penimbangan.

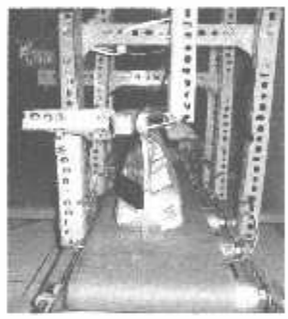


Gambar. 4.18. Tampilan Berat Setting dan Aktual

Tampilan setting merupakan acuan berat aktual, sehingga pada saat berat aktual sudah mencapai berat seperti pada gambar 4.12,maka proses pengisian selesai.

Gambar . 4.19. Tampilan Proses Pengisian dan Penimbangan Gula

Seperti yang terdapat pada gambar 4.13. Setelah proses penimbangan selesai selanjutnya akan menuju step berikutnya dimana gula yang telah dimasukkan kedalam plastik kemasan akan diprcs.



Gambar. 4.20. Tampilan Proses Pengepresan

Apabila seluruh proses telah selesai maka buzzer akan memberikan tanda peringatan, dengan tampilan pada LCD melakukan proses kembali atau tidak.

Gambar. 4.21. Tampilan Akhir Dari Proses

BAB V

PENUTUP

5.1. Kesimpulan

Dari hasil pengujian dan analisa dari alat yang telah dibuat maka dapat disimpulkan :

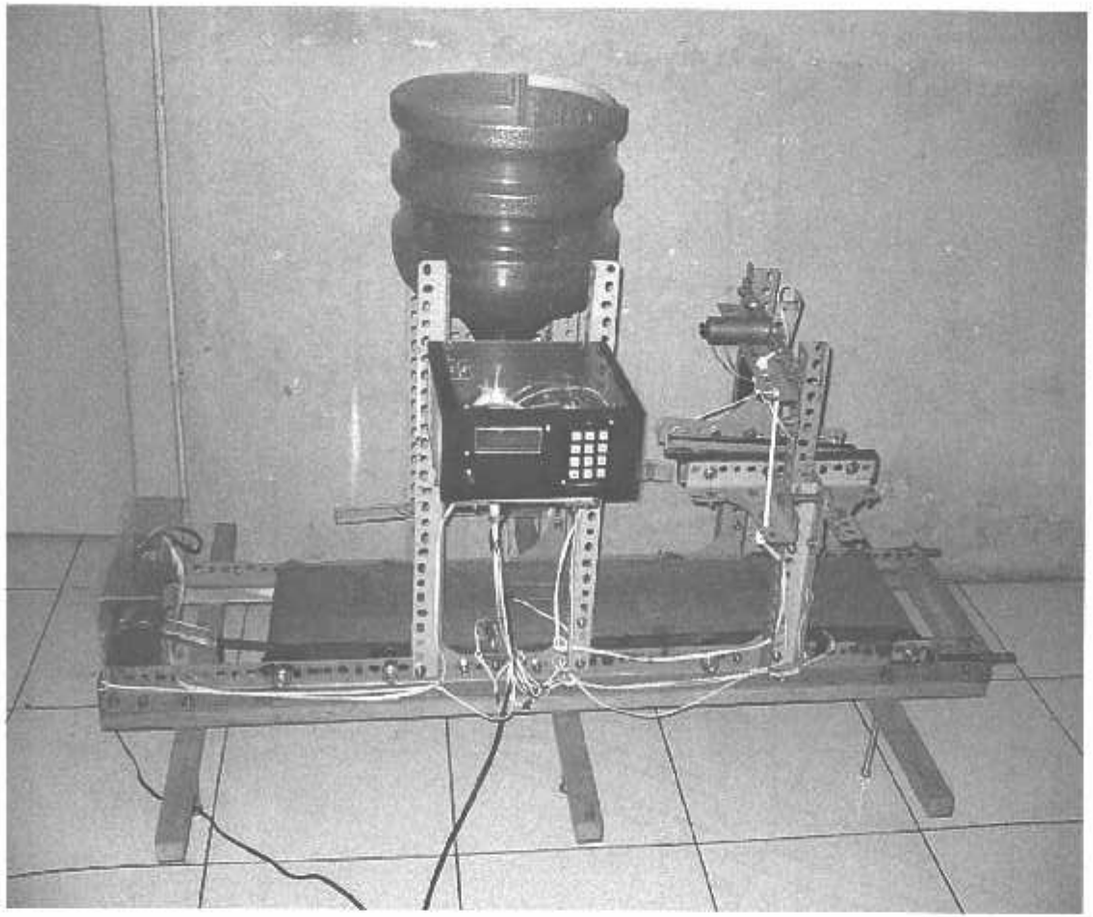
1. Pada pengujian rangkaian mikrokontroller AT89S8252, mikrokontroller dapat berfungsi mengendalikan sistem keseluruhan.
2. Pada pengujian keypad, rangkaian dapat digunakan sebagai masukan perintah berupa pilihan proses berat 1000 gram,1500 gram dan banyak nya jumlah gula yang akan diproses.
3. Pada pengujian LCD, rangkaian dapat digunakan sebagai penampil proses.
4. Pada pengujian sensor berat dengan melakukan beberapa kali percobaan dengan nilai berat yang berbeda didapat penyimpangan hasil yang bervariasi. Hal ini disebabkan karena tingkat linearitas sensor berat yang menggunakan potensiometer geser yang dihubungkan dengan pegas timbangan konvensional tidak dapat bekerja 100 %. Pada pengujian sistem timbangan digital dapat diketahui nilai persentasi kesalahan rata – ratanya, yaitu sebesar 2,588 %. Dan dapat diketahui pula persentasi ketelitiannya, yaitu sebesar 97,412 %.
5. Pada pengujian ADC 0804, dapat diketahui nilai persentasi kesalahan rata – ratanya, yaitu sebesar 1,692 %. Sehingga dapat diketahui persentasi ketelitiannya, yaitu sebesar 98,085 %

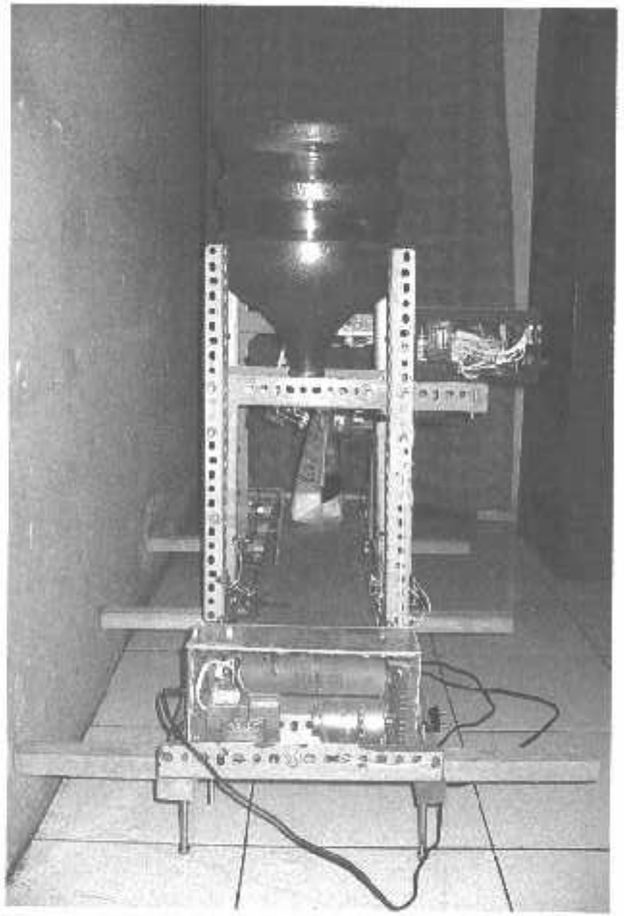
6. Dalam pengujian pengisian gula dalam kantung diperlukan waktu selama 15 detik untuk pilihan berat 1000gr dan 24 detik untuk berat gula 1500 gr, sedangkan untuk proses pengepresan plastik memerlukan waktu 10 detik

5.2. Saran

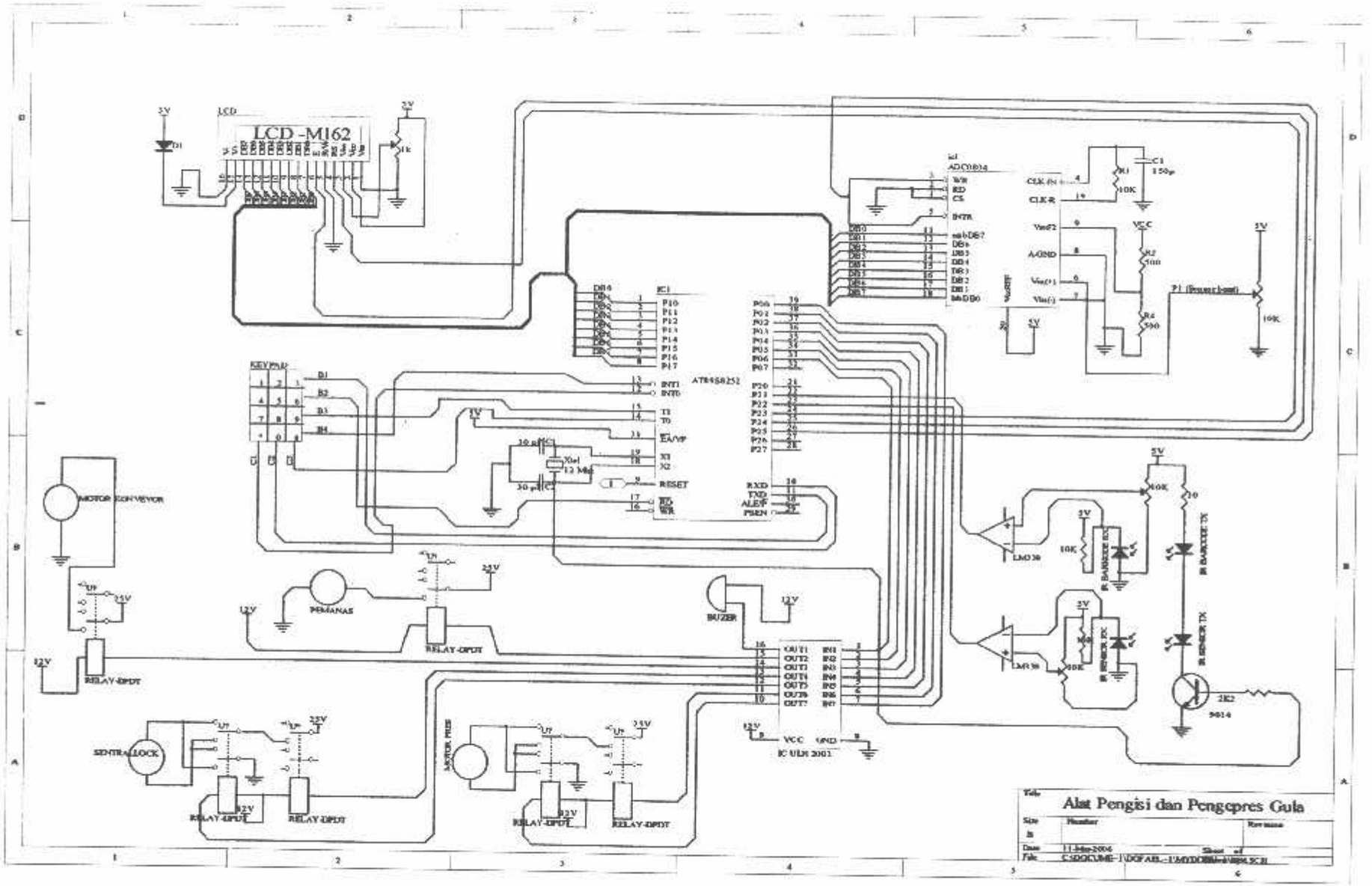
Untuk mengembangkan alat pengisian dan pengepresan gula pasir dalam kemasan ini, maka yang perlu diperhatikan antara lain:

1. Pada sensor berat hendaknya menggunakan sensor yang mempunyai tingkat linearitas yang baik, misalnya menggunakan sensor LVDT.
2. Pada saat proses penimbangan berat yang diinginkan sering berubah-ubah dikarenakan beberapa faktor antara lain kelenturan belt konveyor dan penempatan plastik kemas
3. Perlu membuat jalur untuk membantu penempatan plastik kemasan agar tepat berada pada pintu gula dan pada proses pengepresannya.





GAMBAR ALAT


LCD -M162
ADC0804
AT89S8252
IC ULN 2003
MOTOR CONVEYOR
PEMANAS
BUZZER
RELAY-DPDT
SENTRALLOCK
LM 358
Alat Pengisi dan Pengepres Gula

LAMPIRAN

INSTITUT TEKNOLOGI NASIONAL MALANG
JL. BENDUNGAN SIGURA-GURA 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Ady Kristianto
Nim : 0017184
Masa Bimbingan : 15-Sep-2005 s/d 18-Mar-1006
Judul Sripsi : Perancangan Dan Pembuatan Alat Pengisian Dan Pengepresan Gula Pasir Dalam Kemasan Secara Otomatis Dengan Menggunakan Mikrokontroller AT89S8252

NO	Tanggal	Uraian	Paraf Pembimbing
1	5 -01- 2006	ACC BAB I	
2	13 -01-2006	ACC BAB II	
3	24-01-2006	Revisi BAB III	
4	3-02-2006	ACC BAB III	
5	20-02-2006	Revisi BAB IV	
6	27-02-2006	ACC BAB V	
7	10-03-2006	ACC Maju Seminar Hasil	
8	13-03-2006	Demo Alat	
9	20-03-2006	ACC Ujian Skripsi	
10			

Malang, 20 Maret 2006
Dosen Pembimbing

Ir. Eko Nucahyo

INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama : Ady Kristianto
Nim : 00.17.184
Masa Bimbingan : 15 September 2005 – 18 Maret 2006
Judul : *Perancangan Dan Pembuatan Alat Pengisian Dan Pengepresan Gula Pasir Dalam Kemasan Secara Otomatis Dengan Menggunakan Mikrokontroller AT89S8252*

No	Tanggal	Materi Perbaikan	Paraf Penguji
1	4 April 2006	▪ Pengujian linieritas sensor berat	

Disetujui :

Penguji I

Ir. Yusuf Ismail Nakhoda, MT
NIP.Y 1018800189

Penguji II

Ir. F. Yudi Limpraptono, MT
NIP.Y 1039500274

Mengetahui,
Dosen Pembimbing

Ir. Eko Nurcahyo
NIP.Y 1028700172

LISTING PROGARAM : PERANCANGAN DAN PEMBUATAN ALAT PENGISIAN DAN PENGEPRESAN GULA PASIR DALAM KEMASAN SECARA OTOMATIS DENGAN MENGGUNAKAN MIKROKONTROLLER AT 89S8252

```
1.    ;addres memori kontrol
2.    MODE_PROSES EQU   2FH
3.    BUFFDAT1    EQU   30H
4.    BUFFDAT2    EQU   31H
5.    BUFFDAT3    EQU   32H
6.    JUMLAH1B    EQU   40H
7.    JUMLAH2B    EQU   41H
8.    JUMLAH3B    EQU   42H
9.    DATAPERIKSA EQU   38H
10.   ANGKA       EQU   33H
11.   ;
12.   SATUAN            EQU   35H
13.   PULUAN            EQU   36H
14.   RATUSAN           EQU   37H
15.   ;
16.   PORT_ADC    EQU   P1
17.   DATA_ADC    EQU   34H
18.   ENABEL_ADC  EQU   P2.5
19.   ;
20.   PROSES_ISIAN            BIT   18H
21.   DALAM_PROSES_PRES       BIT   19H
22.   BARU_SLESAI       BIT   1AH
23.   SUDAH_PERNAH            BIT   1BH
24.   HIGUNGAN_HABIS          BIT   1CH
25.   ;
26.   ;addres data bit kontrol
27.   sentral_kankir          BIT   P0.0
28.   sentral_OnOff           BIT   P0.1
29.   motorpres_kankir  BIT   P0.2
30.   motorpres_OnOff         BIT   P0.3
31.   Motor_gerak       BIT   P0.4
32.   pemanas                 BIT   P0.5
33.   Buzer             BIT   P0.6
34.   IR_RX1                  BIT   P2.1
35.   IR_RX2                  BIT   P2.2
36.   ;
37.   ;
38.   ORG   00h
39.   JMP   Start
40.   ;-----------------------------------------
41.   ;           INISIALISASI
42.   ;-----------------------------------------
43.   START:
44.   MOV   P0,#00H
45.   CALL  tunda_lama
46.   CALL  tunda_lama
47.   CALL  tunda_lama
48.   LCALL INISIALISASI_LCD  ;INISIALISASI LCD
49.   ;
```

```
50.   MOV   BARIS,#1H
51.   MOV   KOLOM,#0H
52.   CALL  TEMPATKAN_KURSOR
53.   MOV   DPTR,#NAMA          ;TULIS NAMA
54.   LCALL TULIS_STRING
55.   ;
56.   MOV   BARIS,#2H
57.   MOV   KOLOM,#0H
58.   CALL  TEMPATKAN_KURSOR
59.   MOV   DPTR,#NIM           ;TULIS NIM
60.   LCALL TULIS_STRING
61.   CALL  TUNDA_LAMA_SEKALI
62.   ;
63.   MOV   BARIS,#1H
64.   MOV   KOLOM,#0H
65.   CALL  TEMPATKAN_KURSOR
66.   MOV   DPTR,#FAK           ;TULIS FAKULTAS
67.   LCALL TULIS_STRING
68.   ;
69.   MOV   BARIS,#2H
70.   MOV   KOLOM,#0H
71.   CALL  TEMPATKAN_KURSOR
72.   MOV   DPTR,#JUR           ;TULIS JURUSAN
73.   LCALL TULIS_STRING
74.   CALL  TUNDA_LAMA_SEKALI
75.   ;
76.   MOV   BARIS,#1H
77.   MOV   KOLOM,#0H
78.   CALL  TEMPATKAN_KURSOR
79.   MOV   DPTR,#UNIV          ;TULIS UNIVERSITAS
80.   LCALL TULIS_STRING
81.   ;
82.   MOV   BARIS,#2H
83.   MOV   KOLOM,#0H
84.   CALL  TEMPATKAN_KURSOR
85.   MOV   DPTR,#MALANG              ;TULIS KOTA MALANG
86.   LCALL TULIS_STRING
87.   CALL  TUNDA_LAMA_SEKALI
88.   ;
89.   MOV   BARIS,#1H
90.   MOV   KOLOM,#0H
91.   CALL  TEMPATKAN_KURSOR
92.   MOV   DPTR,#JUDUL         ;JUDUL SKRIPSI BARIS PERTAMA
93.   LCALL TULIS_STRING
94.   ;
95.   MOV   BARIS,#2H
96.   MOV   KOLOM,#0H
97.   CALL  TEMPATKAN_KURSOR
98.   MOV   DPTR,#JUDUL1              ;JUDUL BARIS KE DUA
99.   LCALL TULIS_STRING
100.  CALL  TUNDA_LAMA_SEKALI
101.  ;
102.  AWAL_SETING:
103.  TDK_ULANGI_PROSES:
104.  MOV   P0,#00H                   ;
105.  MOV   BARIS,#1H
```

```
106.  MOV   KOLOM,#0H
107.  CALL  TEMPATKAN_KURSOR
108.  MOV   DPTR,#BERAT
109.  LCALL TULIS_STRING
110.  ;
111.  MOV   BARIS,#2H
112.  MOV   KOLOM,#0H
113.  CALL  TEMPATKAN_KURSOR
114.  MOV   DPTR,#BERAT1
115.  LCALL TULIS_STRING
116.  CALL  TUNDA_LAMA
117.  ;
118.  BACA_KEYPAD_LAGI:
119.  LCALL AMBIL_KEYPAD            ;DETEKSI KEYPAD
120.  MOV   R4,HASIL_KEYPAD

121.  CJNE  R4,#1,BUKAN_SATU  ;JIKA 1 MODE PROSES =1
122.  MOV   MODE_PROSES,#1          ;BERAT 1 KG
123.  MOV   BARIS,#2H
124.  MOV   KOLOM,#0H
125.  CALL  TEMPATKAN_KURSOR  ;TULIS MODE 1 KG
126.  MOV   DPTR,#mode2       ;PADA LCD
127.  LCALL TULIS_STRING
128.  SJMP  LONCAT_PROSES
129.  BUKAN_SATU:
130.  CJNE  R4,#2,BUKAN_DUA         ;JIKA 2 MODE PRES = 2
131.  MOV   MODE_PROSES,#2          ;BERAT 1,5 KG
132.  MOV   BARIS,#2H
133.  MOV   KOLOM,#0H
134.  CALL  TEMPATKAN_KURSOR
135.  MOV   DPTR,#mode1       ;TULIS MODE 1,5 KG
136.  LCALL TULIS_STRING            ;PADA LCD
137.  SJMP  LONCAT_PROSES
138.  BUKAN_DUA:
139.  JMP   BACA_KEYPAD_LAGI
140.  LONCAT_PROSES:
141.  LCALL AMBIL_KEYPAD
142.  MOV   R4,HASIL_KEYPAD         ;TUNGGU KEYPAD DILEPAS
143.  CJNE  R4,#'N',LONCAT_PROSES
144.  ;
145.  ;
146.  ULANGI_PROSES:
147.  SETING_JUMLAH:
148.  MOV   BARIS,#1H
149.  MOV   KOLOM,#0H
150.  CALL  TEMPATKAN_KURSOR  ;MASUKKAN JUMLAH
151.  MOV   DPTR,#JUMLAH
152.  LCALL TULIS_STRING
153.  ;
154.  MOV   BARIS,#2H
155.  MOV   KOLOM,#0H
156.  CALL  TEMPATKAN_KURSOR
157.  MOV   DPTR,#JUMLAH1
158.  LCALL TULIS_STRING
159.  ;
160.  CALL  KEYPAD_3_ANGKA          ;PENANGANAN KEYPAD 3 DIGIT
```

```
161.  ;
162.  MOV   R3,mode_proses
163.  CJNE  R3,#1,bkan_tulis_model
164.  MOV   BARIS,#1H
165.  MOV   KOLOM,#0H
166.  CALL  TEMPATKAN_KURSOR  ;mulai proses mesin 0kg
167.  MOV   DPTR,#runa
168.  LCALL TULIS_STRING
169.  SJMP  loncat_tulis_mode
170.  bkan_tulis_model:
171.  MOV   BARIS,#1H
172.  MOV   KOLOM,#0H
173.  CALL  TEMPATKAN_KURSOR  ;mulai proses mesin 1,5kg
174.  MOV   DPTR,#runb
175.  LCALL TULIS_STRING
176.  loncat_tulis_mode:
177.  ;
178.  MOV   BARIS,#2H         ;tulis berat dan jumlah yang tersetting
179.  MOV   KOLOM,#0H
180.  CALL  TEMPATKAN_KURSOR
181.  MOV   DPTR,#run1
182.  LCALL TULIS_STRING
183.  ;
184.  ;
185.  CLR   dalam_proses_pres ;inisial awal pres
186.  CLR   proses_isian
187.  CLR   sudah_pernah
188.  CLR   BARU_SLESAI
189.  ;
190.  ;
191.  ;
192.  MULAI_PROSES:
a.          CALL  TAMPIL_NILAI_ADC  ;AMBIL DAN TAMPIL ADC
193.  ;
194.  MOV   BARIS,#2H         ;TULIS NILAI JUMLAH
195.  MOV   KOLOM,#12
196.  CALL  TEMPATKAN_KURSOR
197.  ;
198.  MOV   A,JUMLAH1B
199.  ORL   A,#30H
200.  MOV   DATALCD,A
201.  CALL  WRITE_DATA
202.  MOV   A,JUMLAH2B
203.  ORL   A,#30H
204.  MOV   DATALCD,A
205.  CALL  WRITE_DATA
206.  MOV   A,JUMLAH3B
207.  ORL   A,#30H
208.  MOV   DATALCD,A
209.  CALL  WRITE_DATA
210.  ;JMP  MULAI_PROSES
a.          ;
b.          JB    PROSES_ISIAN,DALAM_PROSES_ISI_GULA  ;APAKAH
TERDAPAT PROSES
211.  JB    DALAM_PROSES_PRES,ADA_PROSES        ;TERJADI PENGEPRESAN
212.  SETB  MOTOR_GERAK                    ;ON MOTOR KONVEYOR
```

```
213.  CALL  tunda_lama
214.  CALL  tunda_lama
215.  CALL  tunda_lama
216.  ADA_PROSES:
217.  SETB  HIGUNGAN_HABIS
218.  JB    IR_RX1,BLUM_NGISI ;PERIKSA SENSOR SENTRALOCK
219.  SETB  PROSES_ISIAN            ;BUKA SENTRALOCK
220.  CLR   MOTOR_GERAK        ;UNTUK MENGISI GULA
221.  CALL  tunda_lama
222.  CALL  tunda_lama
223.  CALL  tunda_lama
224.  CALL  tunda_lama
225.  CALL  BUKA_SENTRALOCK
226.  JMP   MULAI_PROSES
227.  ;
228.  BLUM_NGISIM:
229.  SJMP  LANGSUNG_BACALAGI
230.  ;
231.  DALAM_PROSES_ISI_GULA:
232.  JB    BARU_SLESAI,SLESAI_NGISI      ;AMBIL NILAI BERAT
233.  LANGSUNG_BACALAGI:
234.  CALL  TAMPIL_NILAI_ADC              ;ADC  SEBAGAI  SUMBER  DATA
BERAT
235.  MOV   R3,MODE_PROSES
236.  MOV   A,DATA_ADC
237.  CJNE  R3,#1,DATA1KG                 ;MODE 1 ATAU 1,5
238.  CJNE  A,#100,BLM_SATUkg       ;MODE 1 APA SUDAH 1KG
239.  JMP   USAI_NGISI
240.  BLM_SATUkg:
241.  JC    BLUM_NGISIM
242.  JMP   USAI_NGISI
243.  DATA1KG:
a.          CJNE  A,#150,BLM_STENGAH            ;MODE  2  APA  SUDAH
1,5KG
b.          JMP   USAI_NGISI
244.  BLM_STENGAH:
245.  JC    BLUM_NGISIM
246.  USAI_NGISI:
a.          CALL  TUTUP_SENTRALOCK        ;TELAH TERISI
b.          SETB  BARU_SLESAI             ;TUTUP SENTRALLOCK
247.  JMP   BLUM_NGISI
248.  SLESAI_NGISI:
249.  JB    DALAM_PROSES_PRES,ADA_PROSES1 ;UNTUK  MENJALANKAN  MOTOR
KOVEYOR
250.  SETB  MOTOR_GERAK             ;TUNGGU SAMPAI TIDAK ADA PROSES
251.  CALL  TUNDA_LAMA
252.  CALL  TUNDA_LAMA
253.  CALL  TUNDA_LAMA
254.  CALL  TUNDA_LAMA
255.  ADA_PROSES1:
256.  JNB   IR_RX1,MASI_ADA_TEMPAT        ;PLASTIK    MASI    MENUTUP
INFRA MERAH
257.  CALL  TUNDA_LAMA
258.  CALL  TUNDA_LAMA
259.  JNB   IR_RX1,MASI_ADA_TEMPAT
260.  CLR   BARU_SLESAI
```

```
261.   CLR    PROSES_ISIAN
262.   MASI_ADA_TEMPAT:
263.   ;
264.   ;
265.   ;
266.   ;
267.   BLUM_NGISI:
268.   SETB   HIGUNGAN_HABIS
269.   JB     IR_RX2,BLUM_NGISI2              ;TUNGGU  INFRA  MERAH  YANG
KE 2
270.   JB     SUDAH_PERNAH,BLUM_NGISI2
271.   CLR    motor_gerak
272.   CALL   TUNDA_LAMA
273.   CALL   TUNDA_LAMA
274.   CALL   TUNDA_LAMA
275.   SETB   DALAM_PROSES_PRES         ;DALAM PROSES
276.   CALL   PROSES_PRES               ;FUNGSI UNTUK PROSES PRES
277.   CALL   TUNDA_STABIL
278.   CLR    DALAM_PROSES_PRES
279.   SETB   SUDAH_PERNAH
280.   JB     PROSES_ISIAN,BLUM_NGISI2
281.   SETB   MOTOR_GERAK
282.   CALL   TUNDA_LAMA
283.   CALL   TUNDA_LAMA
284.   CALL   TUNDA_LAMA
285.   CALL   TUNDA_LAMA
286.   BLUM_nGISI2:
287.   JB     IR_RX2,SUDAH_KOSONG              ;MASI MENDAPAT BUNGKUS
288.   SETB   SUDAH_PERNAH
289.   SJMP   GOOOO
290.   SUDAH_KOSONG:
291.   CLR    SUDAH_PERNAH
292.   GOOOO:
293.   JB     HIGUNGAN_HABIS,BLM_HABIS
294.   CLR    MOTOR_GERAK
295.   MOV    BARIS,#1
296.   MOV    KOLOM,#0
297.   CALL   TEMPATKAN_KURSOR
298.   MOV    DPTR,#AKHIR
299.   CALL   TULIS_STRING
300.   MOV    BARIS,#2
301.   MOV    KOLOM,#0
302.   CALL   TEMPATKAN_KURSOR
303.   MOV    DPTR,#AKHIR1
304.   CALL   TULIS_STRING
305.   SETB   buzer
306.   ;
307.   TUROS_KE_KEYPAD:
308.   CALL   AMBIL_KEYPAD
309.   MOV    R4,HASIL_KEYPAD
310.   CJNE   R4,#5,BKNA_YA
311.   CLR    buzer
312.   JMP    ULANGI_PROSES
313.   BKNA_YA:
314.   CJNE   R4,#6,BKNA_TDK
315.   CLR    buzer
```

```
316.  JMP   TDK_ULANGI_PROSES
317.  BKNA_TDK:
318.  SJMP  TURUS_KE_KEYPAD
319.  BLM_HABIS:
320.  CALL  AMBIL_KEYPAD
321.  MOV   R4,HASIL_KEYPAD
322.  CJNE  R4,#'*',BKNCANCELyA
323.  JMP   TDK_ULANGI_PROSES
324.  BKNCANCELyA:
325.  JMP   MULAI_PROSES
326.  ;
327.  ;
328.  ;
329.  NAMA: DB  'ADY KRISTIANTO  $'
330.  NIM:  DB  'NIM : C0.17.184 $'
331.  FAK:  DB  '  Fak  TEKNIK   $'
332.  JUR:  DB  ' ELEKTRONIKA S1 $'
333.  UNIV: DB  'INST  TEKNOLOGI $'
334.  MALANG: DB  'NASIONAL MALANG $'
335.  JUDUL:      DB  'ALAT PENGISIAN  $'
336.  JUDUL1: DB  'GULA OTOMATIS...$'
337.  BERAT:      DB  'BERAT PNGISIAN  $'
338.  BERAT1:     DB  '(1)1Kg (2)1,5Kg $'
339.  MODE1:  DB  'MODE 1,5 KG.....$'
340.  MODE2:      DB  'MODE  1 KG......$'
341.  JUMLAH: DB  'MASUKKAN JUMLAH:$'
342.  JUMLAH1:DB  '=                $'
343.  RUNA:   DB  'Aktif!MODE 1,0kg$'
344.  RUNb:   DB  'Aktif!MODE 1,5kg$'
345.  RUN1: DB  'W:0000mg!J=     $'
346.  AKHIR:      DB  'SLESAI! ULANGI? $'
347.  AKHIR1:     DB  '(5)YA (6)TIDAK  $'
348.  ;
349.  ;
350.  ;
351.  BUKA_SENTRALOCK:
352.  CLR   SENTRAL_ONOFF
353.  CALL  TUNDA_LAMA
354.  CALL  tunda_lama
355.  CALL  tunda_lama
356.  CLR   SENTRAL_KANKIR
357.  CALL  TUNDA_LAMA
358.  CALL  tunda_lama
359.  CALL  tunda_lama
360.  SETB  SENTRAL_ONOFF
361.  CALL  TUNDA_LAMA
362.  CALL  tunda_lama
363.  CALL  tunda_lama
364.  CALL  TUNDA_LAMA
365.  CLR   SENTRAL_ONOFF
366.  RET
367.  TUTUP_SENTRALOCK:
368.  CLR   SENTRAL_ONOFF
369.  CALL  TUNDA_LAMA
370.  CALL  tunda_lama
371.  CALL  tunda_lama
```

```
372.  SETB  SENTRAL_KANKIR
373.  CALL  TUNDA_LAMA
374.  CALL  tunda_lama
375.  CALL  tunda_lama
376.  CALL  TUNDA_LAMA
377.  CALL  tunda_lama
378.  CALL  tunda_lama
379.  SETB  SENTRAL_ONOFF
380.  CALL  TUNDA_LAMA
381.  CALL  tunda_lama
382.  CALL  tunda_lama
383.  CLR   SENTRAL_ONOFF
384.  CALL  tunda_lama
385.  CALL  tunda_lama
386.  CALL  TUNDA_LAMA
387.  CLR   SENTRAL_KANKIR
388.  RET
389.  PROSES_PRES:
390.  CLR   MOTORPRES_ONOFF
391.  CALL  KURANGI_DATA_BCDK3_BYTE
392.  CALL  TUNDA_LAMA
393.  CALL  tunda_lama
394.  CALL  tunda_lama
395.  CLR   MOTORPRES_KANKIR
396.  CALL  TUNDA_LAMA
397.  CALL  tunda_lama
398.  CALL  tunda_lama
399.  SETB  MOTORPRES_ONOFF
400.  CALL  TUNDA_LAMA
401.  CALL  TUNDA_LAMA
402.  SETB  pemanas
403.  MOV   R0,#2
404.  putar_tunda_preset:
405.  CALL  TUNDA_LAMA
406.  CALL  TUNDA_LAMA
407.  CALL  TUNDA_LAMA
408.  CALL  TUNDA_LAMA
409.  CALL  TUNDA_LAMA
410.  CALL  TUNDA_LAMA
411.  CALL  TUNDA_LAMA
412.  CALL  TUNDA_LAMA
413.  CALL  TUNDA_LAMA
414.  CALL  TUNDA_LAMA
415.  CALL  TUNDA_LAMA
416.  CALL  TUNDA_LAMA
417.  CALL  TUNDA_LAMA
418.  CALL  TUNDA_LAMA
419.  CALL  TUNDA_LAMA
420.  CALL  TUNDA_LAMA
421.  CALL  TUNDA_LAMA
422.  CALL  TUNDA_LAMA
423.  CALL  TUNDA_LAMA
424.  CALL  TUNDA_LAMA
425.  CALL  TUNDA_LAMA
426.  CALL  TUNDA_LAMA
427.  CALL  TUNDA_LAMA
```

```
428.  CALL  TUNDA_LAMA
429.  DJNZ  00h,putar_tunda_preset
430.  CLR   pemanas
431.  CALL  TUNDA_LAMA
432.  CALL  TUNDA_LAMA
433.  CALL  TUNDA_LAMA
434.  CALL  TUNDA_LAMA
435.  CALL  TUNDA_LAMA
436.  CALL  TUNDA_LAMA
437.  CALL  TUNDA_LAMA
438.  CALL  TUNDA_LAMA
439.  CALL  TUNDA_LAMA
440.  CALL  TUNDA_LAMA
441.  CALL  TUNDA_LAMA
442.  CALL  TUNDA_LAMA
443.  CALL  TUNDA_LAMA
444.  CALL  TUNDA_LAMA
445.  CALL  TUNDA_LAMA
446.  CALL  TUNDA_LAMA
447.  CALL  TUNDA_LAMA
448.  CALL  TUNDA_LAMA
449.  CLR   MOTORPRES_ONOFF
450.  CALL  TUNDA_LAMA
451.  CALL  TUNDA_LAMA
452.  CALL  TUNDA_LAMA
453.  CALL  TUNDA_LAMA
454.  SETB  MOTORPRES_KANKIR
455.  CALL  TUNDA_LAMA
456.  CALL  TUNDA_LAMA
457.  CALL  TUNDA_LAMA
458.  SETB  MOTORPRES_ONOFF
459.  CALL  TUNDA_LAMA
460.  CALL  TUNDA_LAMA
461.  CALL  TUNDA_LAMA
462.  CALL  TUNDA_LAMA
463.  CLR   motorpres_onoff
464.  CALL  TUNDA_LAMA
465.  CALL  TUNDA_LAMA
466.  RET
467.  ;
468.  ;
469.  ;
470.  ;
471.  ;---------------------------------
472.  ; RUTIN PENUNDAAN YANG LAMA
473.  ;---------------------------------
474.  TUNDA_LAMA_SEKALI:
475.  MOV   7BH,#20
476.  PUTAR_TUNDA:
477.  CALL  TUNDA_LAMA
478.  DJNZ  7BH,PUTAR_TUNDA
479.  RET
480.  ;---------------------------------
481.  ;PEMANFAATAN LCD M1632 8BIT DATA
482.  ;---------------------------------
483.  DATALCD     EQU   P1
```

```
484.  ID          BIT   P1.1
485.  SI          BIT   P1.0
486.  DI          BIT   P1.2
487.  CI          BIT   P1.1
488.  BI          BIT   P1.0
489.  SCI         BIT   P1.3
490.  RLI         BIT   P1.2
491.  DLB         BIT   P1.4
492.  RS          BIT   P2.4
493.  E           BIT   P2.3
494.  ;
495.  ;
496.  DISPLAY_CLEAR:
497.  MOV   DATALCD,#01H
498.  JMP   KIRIM_PERINTAH_LCD
499.  CURSOR_HOME:
500.  MOV   DATALCD,#02H
501.  JMP   KIRIM_PERINTAH_LCD
502.  ENTRI_MODE_SET:
503.  PUSH  ACC
504.  ;MOV  DATALCD,#0H
505.  MOV   A,#04H
506.  ORL   DATALCD,A
507.  POP   ACC
508.  JMP   KIRIM_PERINTAH_LCD
509.  ON_OFF:
510.  PUSH  ACC
511.  ;MOV  DATALCD,#0H
512.  MOV   A,#08H
513.  ORL   DATALCD,A
514.  POP   ACC
515.  JMP   KIRIM_PERINTAH_LCD
516.  CURSOR_SIFT:
517.  PUSH  ACC
518.  ;MOV  DATALCD,#0H
519.  MOV   A,#10H
520.  ORL   DATALCD,A
521.  POP   ACC
522.  JMP   KIRIM_PERINTAH_LCD
523.  FUNGSI_SET:
524.  PUSH  ACC
525.  ;MOV  DATALCD,#0H
526.  MOV   A,#38H
527.  ORL   DATALCD,A
528.  POP   ACC
529.  JMP   KIRIM_PERINTAH_LCD
530.  CGRAM_ADDR:
531.  PUSH  ACC
532.  ;MOV  DATALCD,#0H
533.  MOV   A,#40H
534.  ORL   DATALCD,A
535.  POP   ACC
536.  JMP   KIRIM_PERINTAH_LCD
537.  DDRAM_ADDR:
538.  PUSH  ACC
539.  MOV   A,#80H
```

```
540.  ORL   DATALCD,A
541.  POP   ACC
542.  JMP   KIRIM_PERINTAH_LCD
543.  WRITE_DATA:
544.  JMP   KIRIM_DATA_LCD
545.  READ_DATA:
546.  JMP   BACA_DATA_LCD
547.  ;
548.  ;
549.  ;------
550.  KIRIM_PERINTAH_LCD:
551.  CLR   RS
552.  SJMP  LONCATLCD
553.  KIRIM_DATA_LCD:
554.  SETB  RS
555.  LONCATLCD:
556.  ; CLR RW
557.  SETB  E
558.  NOP
559.  NOP
560.  NOP
561.  CLR   E
562.  CALL  TUNDALCD
563.  RET
564.  BACA_DATA_LCD:
565.  SETB  RS
566.  ;SETB RW
567.  SETB  E
568.  MOV   A,DATALCD
569.  CLR   E
570.  CALL  TUNDALCD
571.  RET
572.  ;
573.  ;
574.  BACA_POSISI_CURSOR:
575.  MOV   DATALCD,#0FFH
576.  CLR   RS
577.  ;SETB RW
578.  SETB  E
579.  MOV   A,DATALCD
580.  ANL   A,#7FH
581.  CLR   E
582.  RET
583.  ;
584.  ;

585.  ;------------
586.  TUNDALCD:
587.  ;------------
588.  MOV   8CH,#0FFH
589.  DJNZ  8CH,$
590.  RET
591.  ;
592.  ;
593.  ;-------------------------------------
594.  ; TULIS SUATU STRING PADA LCD
```

```
595.  ;   SIAPKAN DPTR PADA ALAMAT LABEL
596.  ;-------------------------------------
597.  TULIS_STRING:
598.  PUSH  ACC
599.  TERUSKAN:
600.  CLR   A
601.  MOVC  A,@A+DPTR
602.  CJNE  A,#'S',TERUS_TULIS
603.  POP   ACC
604.  RET
605.  TERUS_TULIS:
606.  MOV   DATALCD,A
607.  CALL  WRITE_DATA
608.  INC   DPTR
609.  SJMP  TERUSKAN
610.  ;
611.  ;
612.  ;-------------------------------------
613.  ;SETING KURSOR LCD
614.  ;  TEMPATKAN 'BARIS' DAN 'COLOM' DULU
615.  ;-------------------------------------
616.  BARIS        EQU   7BH
617.  KOLOM        EQU   7CH
618.  BUFKURSOR    EQU   7FH
619.  ;
620.  ;
621.  TEMPATKAN_KURSOR:
622.  PUSH  ACC
623.  MOV   A,BARIS
624.  CJNE  A,#01H,BARIS_DUA
625.  MOV   BUFKURSOR,KOLOM
626.  SJMP  TEMPAT_KUR
627.  BARIS_DUA:
628.  MOV   A,KOLOM
629.  ADD   A,#40H
630.  MOV   BUFKURSOR,A
631.  TEMPAT_KUR:
632.  POP   ACC
633.  POSISI:
634.  MOV   DATALCD,BUFKURSOR
635.  CALL  DDRAM_ADDR
636.  RET
637.  ;
638.  ;
639.  ;-------------------------------------
640.  ;SETING INISIALISASI LCD
641.  ;-------------------------------------
642.  INISIALISASI_LCD:
643.  MOV   DATALCD,#00
644.  SETB  DLB
645.  CALL  FUNGSI_SET  ;1
646.  CALL  TUNDA_LAMA
647.  CALL  FUNGSI_SET  ;2
648.  CALL  TUNDA_LAMA
649.  CALL  FUNGSI_SET  ;3
650.  CALL  TUNDA_LAMA
```

```
651.  CALL  FUNGSI_SET
652.  MOV   DATALCD,#00
653.  SETB  DI
654.  CLR   CI
655.  CLR   BI
656.  CALL  ON_OFF
657.  CALL  DISPLAY_CLEAR
658.  CALL  TUNDA_LAMA
659.  MOV   DATALCD,#0C
660.  SETB  ID
661.  CLR   SI
662.  CALL  ENTRI_MODE_SET
663.  RET
664.  ;
665.  ;---------------
666.  ;TUNDA LAMA
667.  ;---------------
668.  TUNDA_LAMA:
669.  MOV   7AH,#0FFH
670.  PUTARTERUS:
671.  MOV   79H,#0FFH
672.  DJNZ  79H,$
673.  DJNZ  7AH,PUTARTERUS
674.  RET
675.  ;
676.  TUNDA_STABIL:
677.  MOV   7AH,#10
678.  JMP   PUTARTERUS
679.  ;
680.  ;-----------------------------------
681.  ; MENULIS 2 ANGKA BINER KE LCD
682.  ;  ANGKA DISIAPKAN PADA A
683.  ;-----------------------------------
684.  BUF_ANGKA   EQU   7EH
685.  ;
686.  TULIS_2_ANGKA:
687.  MOV   B,#10
688.  DIV   AB
689.  SWAP  A
690.  ADD   A,B
691.  MOV   BUF_ANGKA,A
692.  ANL   A,#0F0H
693.  SWAP  A
694.  ADD   A,#30H
695.  MOV   DATALCD,A
696.  CALL  WRITE_DATA
697.  MOV   A,BUF_ANGKA
698.  ANL   A,#0FH
699.  ADD   A,#30H
700.  MOV   DATALCD,A
701.  CALL  WRITE_DATA
702.  RET
703.  ;
704.  ;-----------------------------------
705.  ; PROGRAM PELAYANAN KEYPAD MATRIK
706.  ;  3 BARIS X 4 COLOM
```

```
707.  ;-----------------------------------
708.  BARISK              EQU   76H
709.  COLOM        EQU    78H
710.  HASIL_KEYPAD        EQU   77H
711.  C2           BIT    P3.0
712.  B1           BIT    P3.1
713.  C1           BIT    P3.2
714.  B4           BIT    P3.3
715.  C3           BIT    P3.4
716.  B3           BIT    P3.5
717.  B2           BIT    P3.6
718.  ;
719.  ;
720.  AMBIL_KEYPAD:
721.  CLR   B1
722.  CLR   B2
723.  CLR   B3
724.  CLR   B4
725.  SETB  C1
726.  SETB  C2
727.  SETB  C3
728.  ;
729.  ;
730.  CALL  TUNDA_KEYPAD
731.  MOV   A,#00H
732.  MOV   C,C1
733.  MOV   ACC.0,C
734.  MOV   C,C2
735.  MOV   ACC.1,C
736.  MOV   C,C3
737.  MOV   ACC.2,C
738.  ;
739.  CJNE  A,#00000110B,BUKAN_1
740.  MOV   BARISK,#1
741.  JMP   LONCAT_BARIS_KEYPAD
742.  BUKAN_1:
743.  CJNE  A,#00000101B,BUKAN_2
744.  MOV   BARISK,#2
745.  JMP   LONCAT_BARIS_KEYPAD
746.  BUKAN_2:
747.  CJNE  A,#00000011B,BUKAN_3
748.  MOV   BARISK,#3
749.  JMP   LONCAT_BARIS_KEYPAD
750.  BUKAN_3:
751.  LJMP  LONCAT_NO_TEKAN
752.  ;
753.  LONCAT_BARIS_KEYPAD:
754.  CLR   C1
755.  CLR   C2
756.  CLR   C3
757.  ;
758.  SETB  B1
759.  SETB  B2
760.  SETB  B3
761.  SETB  B4
762.  ;
```

```
763.  CALL  TUNDA_KEYPAD
764.  MOV   A,#00H
765.  MOV   C,B1
766.  MOV   ACC.0,C
767.  MOV   C,B2
768.  MOV   ACC.1,C
769.  MOV   C,B3
770.  MOV   ACC.2,C
771.  MOV   C,B4
772.  MOV   ACC.3,C
773.  ;
774.  CJNE  A,#00001110B,BUKAN_1C
775.  MOV   COLOM,#0
776.  JMP   LONCAT_BARIS_KEYPADC
777.  BUKAN_1C:
778.  CJNE  A,#00001101B,BUKAN_2C
779.  MOV   COLOM,#1
780.  JMP   LONCAT_BARIS_KEYPADC
781.  BUKAN_2C:
782.  CJNE  A,#00001011B,BUKAN_3C
783.  MOV   COLOM,#2
784.  JMP   LONCAT_BARIS_KEYPADC
785.  BUKAN_3C:
786.  CJNE  A,#00000111B,BUKAN_4C
787.  MOV   COLOM,#3
788.  JMP   LONCAT_BARIS_KEYPADC
789.  BUKAN_4C:
790.  LONCAT_BARIS_KEYPADC:
791.  ;
792.  ;
793.  MOV   P3,#0FFH
794.  MOV   B,#3
795.  MOV   A,COLOM
796.  MUL   AB
797.  ADD   A,BARISK
798.  ;
799.  CJNE  A,#10,LON10
800.  MOV   A,#'*'
801.  JMP   LON12
802.  LON10:
803.  CJNE  A,#11,LON11
804.  MOV   A,#0
805.  JMP   LON12
806.  LON11:
807.  CJNE  A,#12,LON12
808.  MOV   A,#'#'
809.  LON12:
810.  MOV   HASIL_KEYPAD,A
811.  RET
812.  ;
813.  LONCAT_NO_TEKAN:
814.  MOV   A,#'N'
815.  MOV   P3,#0FFH
816.  MOV   HASIL_KEYPAD,A
817.  RET
818.  ;
```

```
819.  ;
820.  TUNDA_KEYPAD:
821.  PUSH  07
822.  PUSH  06
823.  MOV   R7,#0FFH
824.  TUNDA_KEYPAD1:
825.  MOV   R6,#20H
826.  DJNZ  R6,$
827.  DJNZ  R7,TUNDA_KEYPAD1
828.  POP   06
829.  POP   07
830.  RET
831.  ;
832.  ;
833.  ;
834.  ;-----------------------------------------------
835.  KEYPAD_3_ANGKA:
836.  ;-----------------------------------------------
837.  MOV   BARIS,#2
838.  MOV   KOLOM,#1
839.  CALL  TEMPATKAN_KURSOR
840.  ;
841.  MOV   BUFFDAT1,#00H
842.  MOV   BUFFDAT2,#00H
843.  MOV   BUFFDAT3,#00H
844.  MOV   ANGKA,#1
845.  MOV   R0,#30h
846.  TERUS1:
847.  LCALL AMBIL_KEYPAD
848.  MOV   R4,HASIL_KEYPAD
849.  CJNE  R4,#'N',BUKANY1
850.  JMP   TERUS1
851.  BUKANY1:
852.  LCALL AMBIL_KEYPAD
853.  MOV   A,HASIL_KEYPAD
854.  CJNE  A,#'N',BUKANY1
855.  ;
856.  CJNE  R4,#'#',BUKANKR
857.  JMP   KELUARA
858.  ;
859.  BUKANKR:
860.  CJNE  R4,#'*',BUKANB
861.  MOV   ANGKA,#1
862.  MOV   BARIS,#2
863.  MOV   KOLOM,#1
864.  CALL  TEMPATKAN_KURSOR
865.  MOV   R0,#30H
866.  MOV   DATALCD,#30H
867.  LCALL WRITE_DATA
868.  LCALL WRITE_DATA
869.  LCALL WRITE_DATA
870.  ;
871.  MOV   BUFFDAT1,#00H
872.  MOV   BUFFDAT2,#00H
873.  MOV   BUFFDAT3,#00H
874.  ;
```

```
875.  MOV   ANGKA,#1
876.  MOV   BARIS,#2
877.  MOV   KOLOM,#1
878.  CALL  TEMPATKAN_KURSOR
879.  ;
880.  JMP   TERUS1
881.  BUKANB:
882.  CJNE  R4,#'N',BUKANN1
883.  JMP   TERUS1
884.  BUKANN1:
a.          MOV   A,R4
b.          MOV   @R0,A
c.          INC   R0
d.          ADD   A,#30H
e.          MOV   DATALCD,A
885.  CALL  WRITE_DATA
886.  INC   ANGKA
887.  MOV   A,ANGKA
888.  CJNE  A,#4,MASIH_1
889.  MOV   ANGKA,#1
890.  MOV   BARIS,#2
891.  MOV   KOLOM,#1
892.  CALL  TEMPATKAN_KURSOR
893.  MOV   R0,#30H
894.  MASIH_1:
895.  JMP   TERUS1
896.  KELUARA:
897.  MOV   JUMLAH1B,BUFFDAT1
898.  MOV   JUMLAH2B,BUFFDAT2
899.  MOV   JUMLAH3B,BUFFDAT3
900.  RET
901.  ;
902.  ;
903.  ;
904.  ;
905.  COUNTER_PERIKSA         EQU   60H
906.  ;
907.  ;
908.  PERIKSA_LOGIK_HIGT:
909.  MOV   COUNTER_PERIKSA,#0FFH
910.  MASI_HIGHT:
911.  JB    IR_RX1,SDH_HIGT
912.  SJMP  PERIKSA_LOGIK_HIGT
913.  SDH_HIGT:
914.  NOP
915.  NOP
916.  DJNZ  COUNTER_PERIKSA,MASI_HIGHT
917.  RET
918.  ;
919.  ;
920.  ;
921.  PERIKSA_LOGIK_LOW:
922.  MOV   COUNTER_PERIKSA,#0FFH
923.  MASI_LOW:
924.  JNB   IR_RX1,SDH_LOW
925.  SJMP  PERIKSA_LOGIK_LOW
```

```
926.  SDH_LOW:
927.  NOP
928.  NOP
929.  DJNZ  COUNTER_PERIKSA,MASI_LOW
930.  RET
931.  ;
932.  ;
933.  ;
934.  PERIKSA_LOGIK_HIGT_SENSOR:
935.  MOV   COUNTER_PERIKSA,#0FFH
936.  MASI_HIGHTS:
937.  JB    IR_RX2,SDH_HIGTS
938.  SJMP  PERIKSA_LOGIK_HIGT_SENSOR
939.  SDH_HIGTS:
940.  NOP
941.  NOP
942.  DJNZ  COUNTER_PERIKSA,MASI_HIGHTS
943.  RET
944.  ;
945.  ;
946.  ;
947.  PERIKSA_LOGIK_LOW_SENSOR:
948.  MOV   COUNTER_PERIKSA,#0FFH
949.  MASI_LOWS:
950.  JNB   IR_RX2,SDH_LOWS
951.  SJMP  PERIKSA_LOGIK_LOW_SENSOR
952.  SDH_LOWS:
953.  NOP
954.  NOP
955.  DJNZ  COUNTER_PERIKSA,MASI_LOWS
956.  RET
957.  ;
958.  ;
959.  TAMPIL_NILAI_ADC:
960.  MOV   BARIS,#2H
961.  MOV   KOLOM,#2H
962.  CALL  TEMPATKAN_KURSOR
a.          MOV   PORT_ADC,#0FFH
b.          CLR   ENABEL_ADC        ;ambil data ADC
963.  CALL  tunda_stabil
964.  MOV   DATA_ADC,PORT_ADC
965.  SETB  ENABEL_ADC
966.  ;
967.  MOV   A,data_adc
968.  MOV   B,#100
969.  DIV   AB
970.  ;
971.  ORL   A,#30H
972.  MOV   DATALCD,A         ;TAMPILKAN NILAI ADC
973.  CALL  WRITE_DATA
974.  MOV   A,B
975.  MOV   B,#10
976.  DIV   AB
977.  ORL   A,#30H
978.  MOV   DATALCD,A
979.  CALL  WRITE_DATA
```

```
980.  MOV   A,B
981.  ORL   A,#30H
982.  MOV   DATALCD,A
983.  CALL  WRITE_DATA
984.  RET
985.  ;
986.  ;
987.  KURANGI_DATA_BCDK3_BYTE:
988.  SETB  HIGUNGAN_HABIS
989.  MOV   A,JUMLAH3B
990.  JNZ   BKNNOL_DAT3
991.  MOV   A,JUMLAH2B
992.  JNZ   BKNNOL_DAT2
993.  MOV   A,JUMLAH1B
994.  JNZ   BKNNOL_DAT1
995.  CLR   HIGUNGAN_HABIS
996.  RET
997.  BKNNOL_DAT1:
998.  MOV   JUMLAH3B,#09
999.  MOV   JUMLAH2B,#09
1000. DEC   JUMLAH1B
1001. SJMP  BILSATUAN
1002. BKNNOL_DAT2:
1003. MOV   JUMLAH3B,#09
1004. DEC   JUMLAH2B
1005. SJMP  BILSATUAN
1006. BKNNOL_DAT3:
1007. DEC   JUMLAH3B
1008. ;
1009. BILSATUAN:
1010. MOV   A,JUMLAH3B
1011. ORL   A,JUMLAH2B
1012. ORL   A,JUMLAH1B
1013. JNZ   BLM_ENTEK_REK
1014. CLR   HIGUNGAN_HABIS
1015. BLM_ENTEK_REK:
1016. RET
1017. END
```

Features

- Compatible with MCS-51™ Products
- 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 1,000 Write/Erase Cycles
- 2K Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- 4.0V to 6V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Nine Interrupt Sources
- Programmable UART Serial Channel
- SPI Serial Interface
- Low Power Idle and Power Down Modes
- Interrupt Recovery From Power Down
- Programmable Watchdog Timer
- Dual Data Pointer
- Power Off Flag

Description

The AT89S8252 is a low-power, high-performance CMOS 8-bit microcomputer with 8K bytes of Downloadable Flash programmable and erasable read only memory and 2K bytes of EEPROM. The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard 80C51 instruction set and pinout. The on-chip Downloadable Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Downloadable Flash on a monolithic chip, the Atmel AT89S8252 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

The AT89S8252 provides the following standard features: 8K bytes of Downloadable Flash, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog timer, two Data Pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S8252 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

The Downloadable Flash can be changed a single byte at a time and is accessible through the SPI serial interface. Holding RESET active forces the SPI bus into a serial programming interface and allows the program memory to be written to or read from unless Lock Bit 2 has been activated.

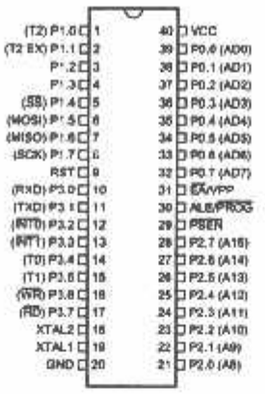
8-Bit Microcontroller with 8K Bytes Flash

AT89S8252

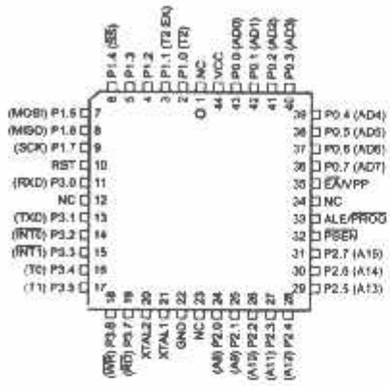
0401D-A-12/97

Pin Configurations

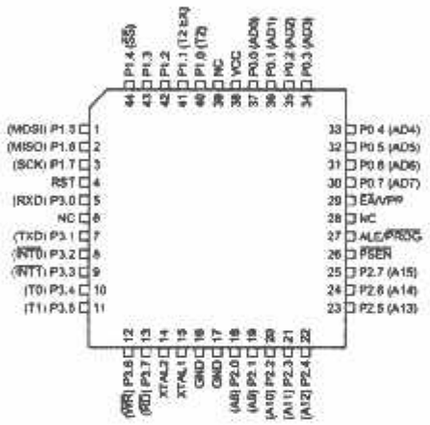
PDIP



PLCC



PQFP/TQFP



Pin Description

VCC
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

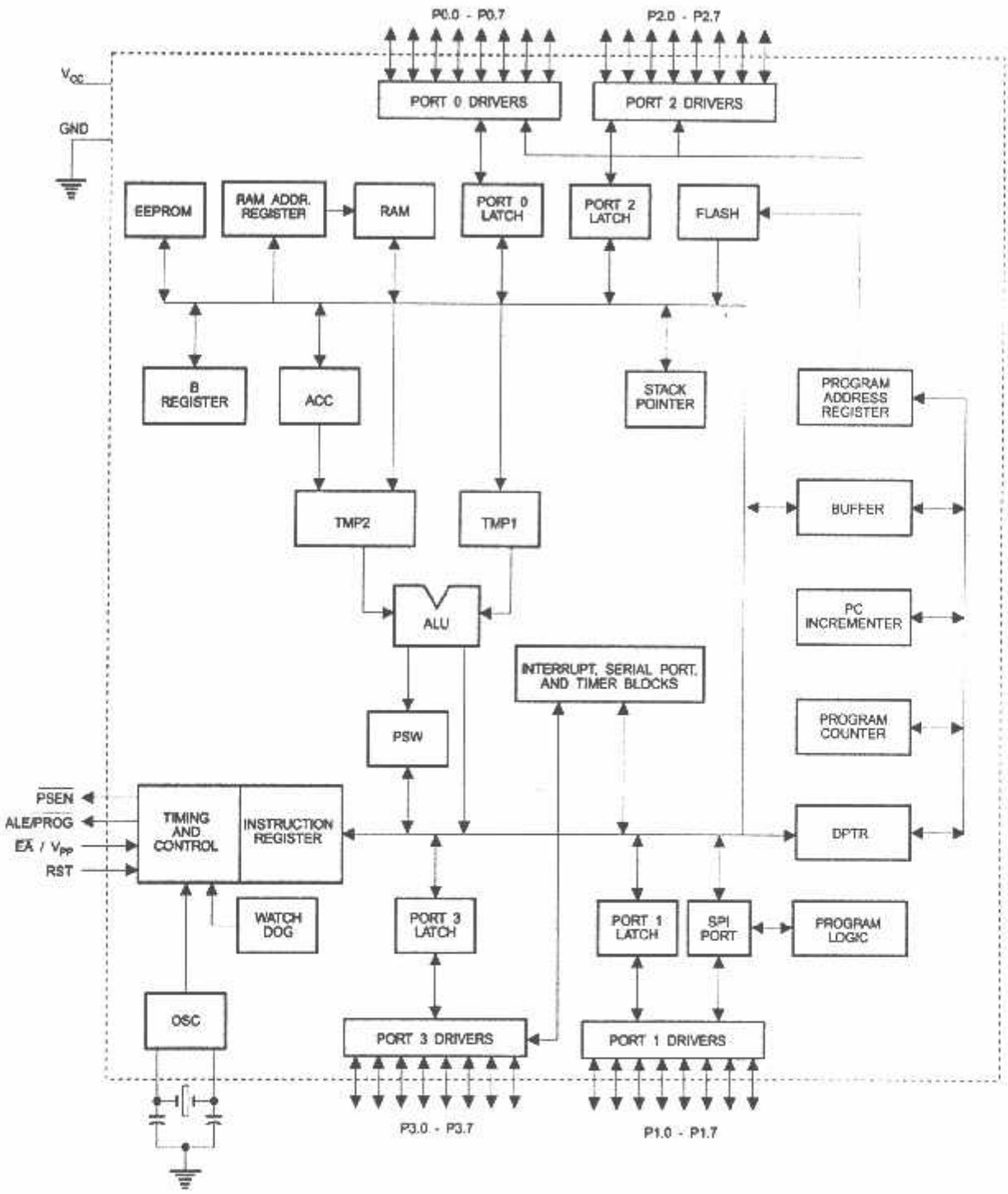
Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Block Diagram



Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8 bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/V_{PP}

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

XTAL1
Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2
Output from the inverting oscillator amplifier.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 1. AT89S8252 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 000001XX			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX						0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						WMCON 00000010		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16 bit capture mode or 16-bit auto-reload mode.

Watchdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in Table 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 2. T2CON—Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

ıual Data Pointer Registers To facilitate accessing both ıternal EEPROM and external data memory, two banks of 6 bit Data Pointer Registers are provided: DP0 at SFR ddress locations 82H-83H and DP1 at 84H-85H. Bit DPS 0 in SFR WMCON selects DP0 and DPS = 1 selects)P1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

able 3. WMCON—Watchdog and Memory Control Register

WMCON Address = 96H — Reset Value = 0000 0010B

Bit	PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
	7	6	5	4	3	2	1	0

Symbol	Function
PS2 PS1 PS0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EEMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EEMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
DPS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
WDTRST RDY/$\overline{BSY}$	Watchdog Timer Reset and EEPROM Ready/$\overline{Busy}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{BSY}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed the RDY/$\overline{BSY}$ bit equals "0" and is automatically reset to "1" when programming is completed.
WDTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

Table 4. SPCR—SPI Control Register

SPCR Address = D5H — Reset Value = 0000 01XXB

Bit	7	6	5	4	3	2	1	0
	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

Symbol	Function
SPIE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
CPOL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
CPHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
SPR0 SPR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{osc.}$, is as follows: SPR1 SPR0 SCK = $F_{osc.}$ divided by 0 0 4 0 1 16 1 0 64 1 1 128

Table 5. SPSR—SPI Status Register

SPSR Address = AAH — Reset Value = 00XX XXXXB

Bit	7	6	5	4	3	2	1	0
	SPIF	WCOL	—	—	—	—	—	—

Symbol	Function
SPIF	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then accessing the SPI data register.
WCOL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

Table 6. SPDR—SPI Data Register

SPDR Address = 86H — Reset Value = unchanged

Bit	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
	7	6	5	4	3	2	1	0

Data Memory—EEPROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM or data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. RDY/$\overline{BSY}$ = 0 means programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power Down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			Period (nominal)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-45, section titled, "Timer/Counters."

Timer 2

Timer 2 is a 16 bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-Reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

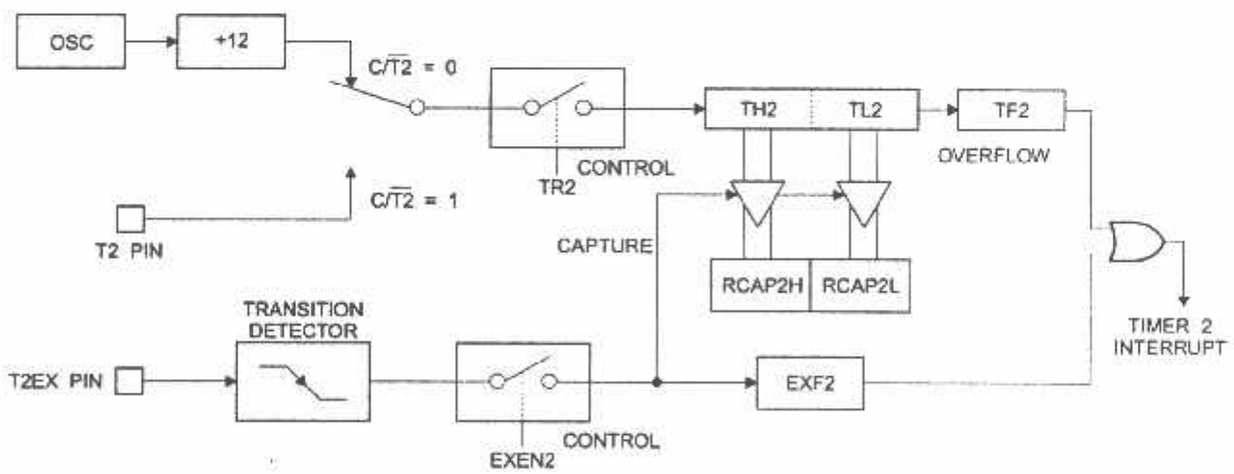
In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16 bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Auto-Reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16 bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to

Figure 1. Timer 2 in Capture Mode



0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16 bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16 bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16 bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 2. Timer 2 in Auto Reload Mode (DCEN = 0)

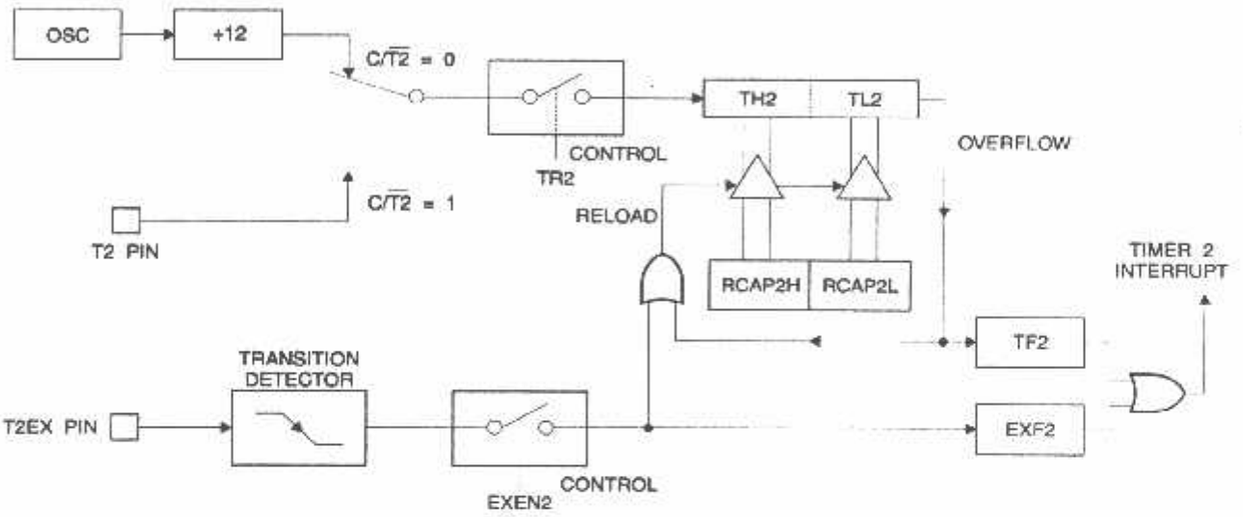


Table 9. T2MOD—Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

	—	—	—	—	—	—	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

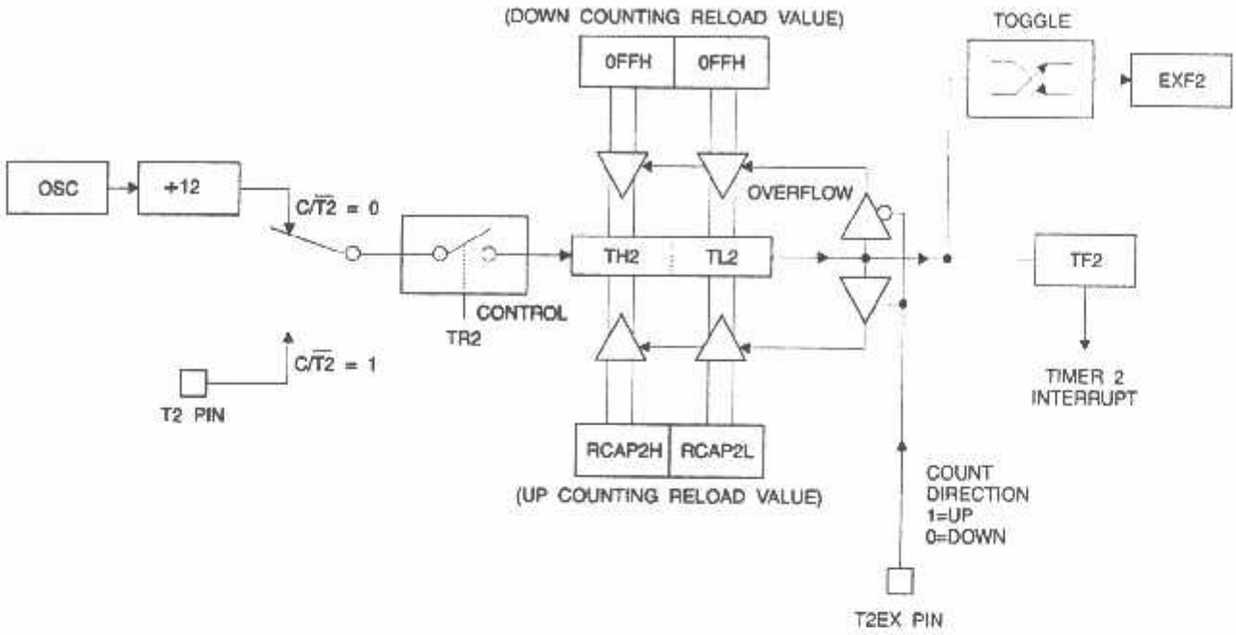
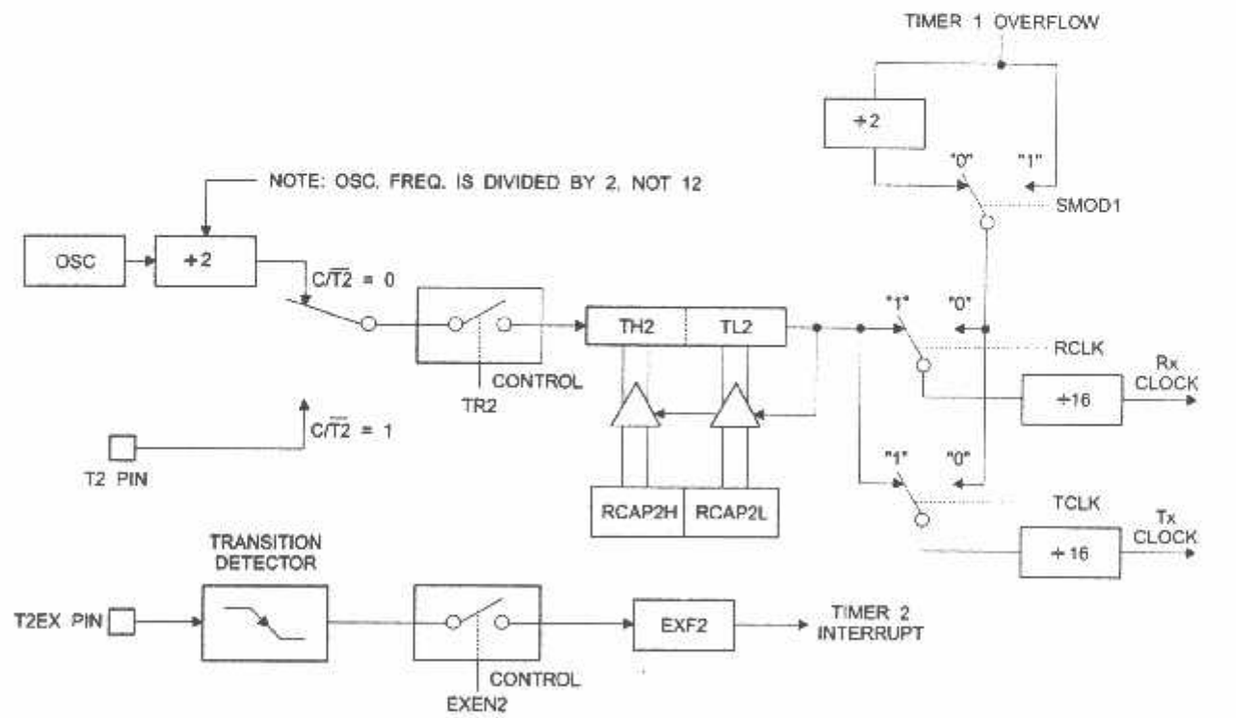


Figure 4. Timer 2 In Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16 bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation (CP/$\overline{T2}$ = 0). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

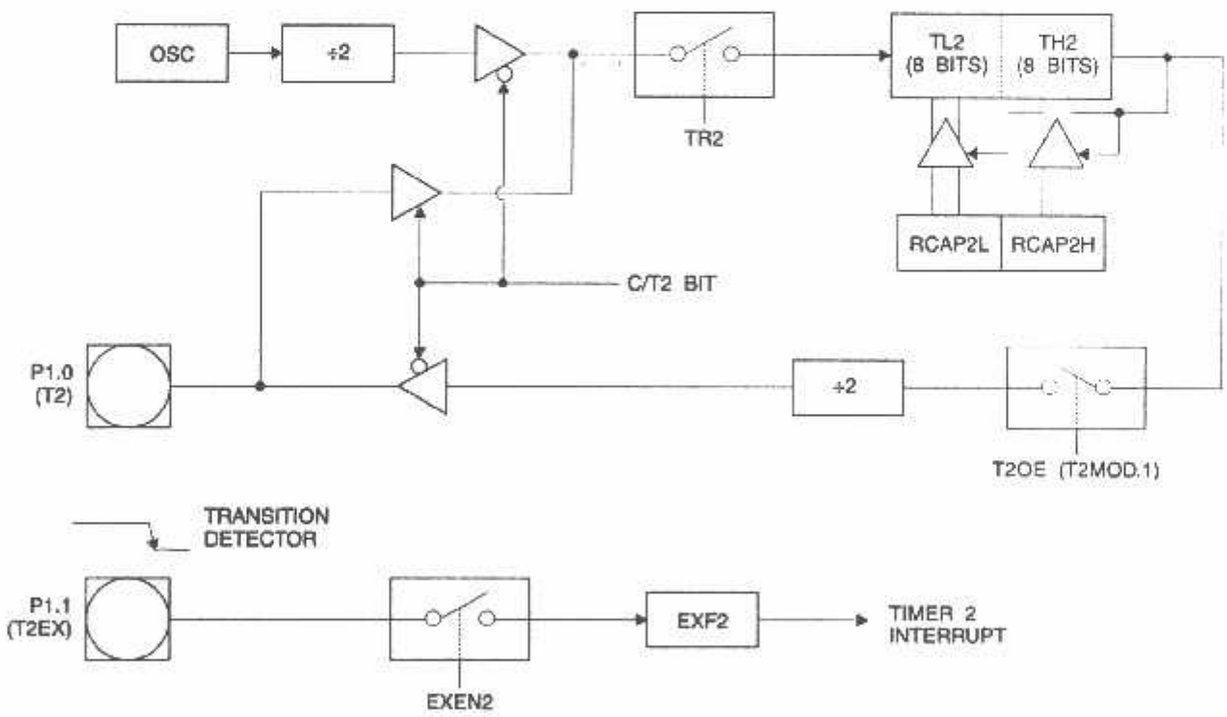
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16 bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Figure 5. Timer 2 in Clock-Out Mode



Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

UART

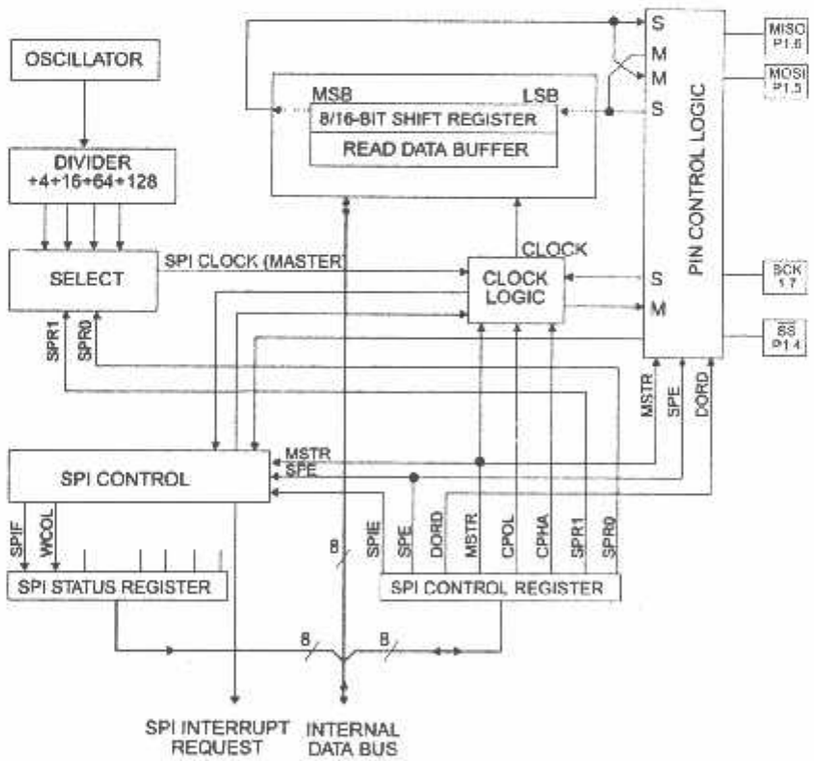
The UART in the AT89S8252 operates the same way as the UART in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-49, section titled, "Serial Interface."

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5-MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

Figure 6. SPI Block Diagram



The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figures 8 and 9.

Figure 7. SPI Master-Slave Interconnection

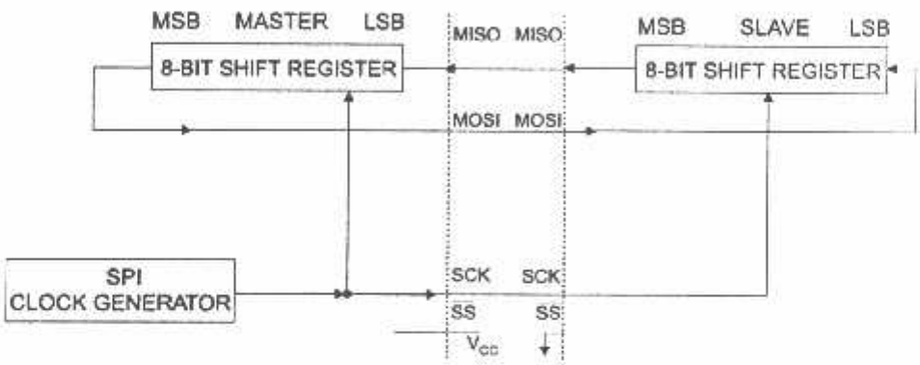
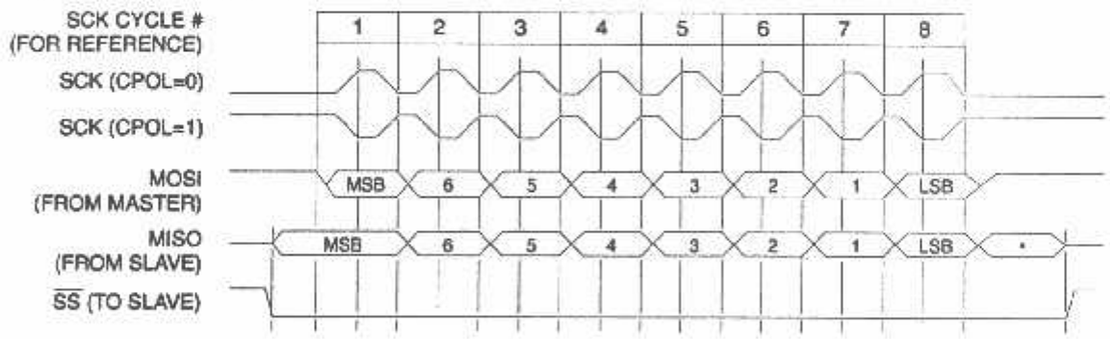
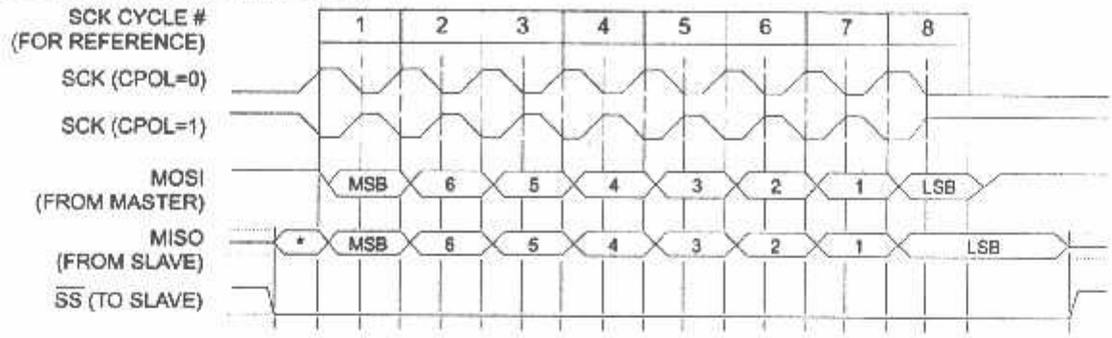


Figure 8. SPI transfer Format with CPHA = 0



Not defined but normally MSB of character just received

Figure 9. SPI Transfer Format with CPHA = 1



*Not defined but normally LSB of previously transmitted character

Interrupts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 10. Interrupt Enable (IE) Register

(MSB)							(LSB)
EA	—	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.

Figure 10. Interrupt Sources

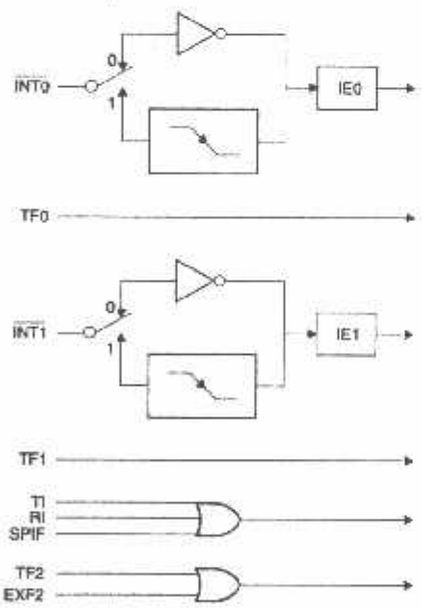


Figure 11. Oscillator Connections

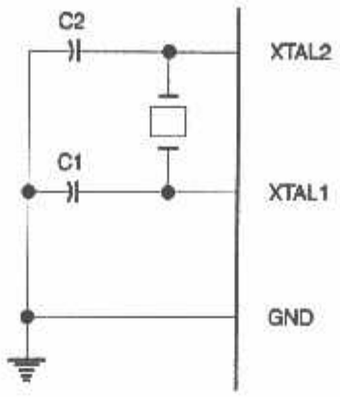
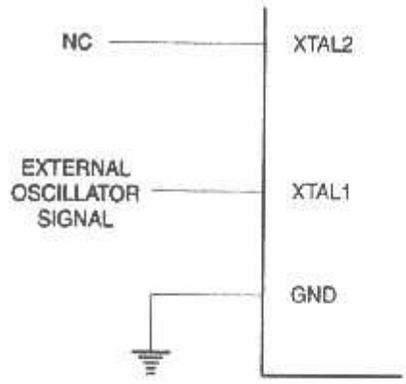


Figure 12. External Clock Drive Configuration



Note: Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power Down Mode

In the power down mode, the oscillator is stopped and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. Exit from power down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power down via an interrupt, the external interrupt must be enabled as level sensitive before entering power down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Lock Bit Protection Modes[1][2]

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

Notes: 1. U = Unprogrammed
2. P = Programmed

Programming the Flash and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-Voltage (12V) Parallel programming mode and a Low-Voltage (5V) Serial programming mode. The serial programming mode provides a convenient way to download the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm

To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between V_{CC} and GND pins.

   Set RST pin to "H".

   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{PSEN}$ pin to "L"

   ALE pin to "H"

   $\overline{EA}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.

   Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.

8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:

   Set XTAL1 to "L".

   Set RST and $\overline{EA}$ pins to "L".

   Turn V_{CC} power off.

n the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs o use the Chip Erase operation first to erase both arrays.

DATA Polling

The AT89S8252 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin any time after a write cycle has been initiated.

Ready/Busy

The progress of byte programming in the parallel programming mode can also be monitored by the RDY/$\overline{BSY}$ output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate $\overline{BUSY}$. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify

If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase

Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse

A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

Programming Interface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Serial Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Algorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between V_{CC} and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.

3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.

4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.

5. At the end of a programming session, RST can be set low to commence normal operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

nstruction Set

Instruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Chip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
Read Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Write Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
Read Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Write Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Write Lock Bits	1010 1100	LB1 LB2 LB3 x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

otes: 1. $\overline{\text{DATA}}$ polling is used to indicate the end of a write cycle which typically takes less than 2.5 ms at 5V.

2. "aaaaa" = high order address.

3. "x" = don't care.

Flash and EEPROM Parallel Programming Modes

Mode	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
Serial Prog. Modes	H	h[1]	h[1]	x						
Chip Erase	H	L	⌐‾⌐ (2)	12V	H	L	L	L	X	X
Write (10K bytes) Memory	H	L	⌐‾⌐	12V	L	H	H	H	DIN	ADDR
Read (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
Write Lock Bits:	H	L	⌐‾⌐	12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
Read Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
Read Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
Read Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Serial Prog. Enable	H	L	⌐‾⌐ (2)	12V	L	H	L	H	P0.0 = 0	X
Serial Prog. Disable	H	L	⌐‾⌐ (2)	12V	L	H	L	H	P0.0 = 1	X
Read Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

Notes:
1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10-ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{BSY}$.
4. "X" = don't care

'igure 14. Programming the Flash/EEPROM Memory

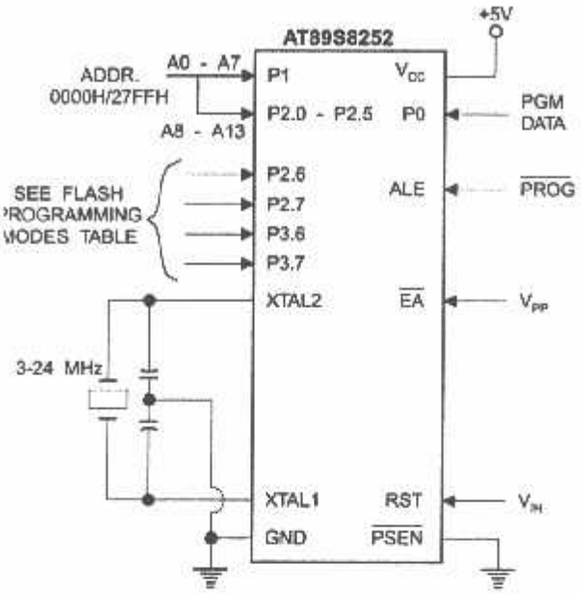
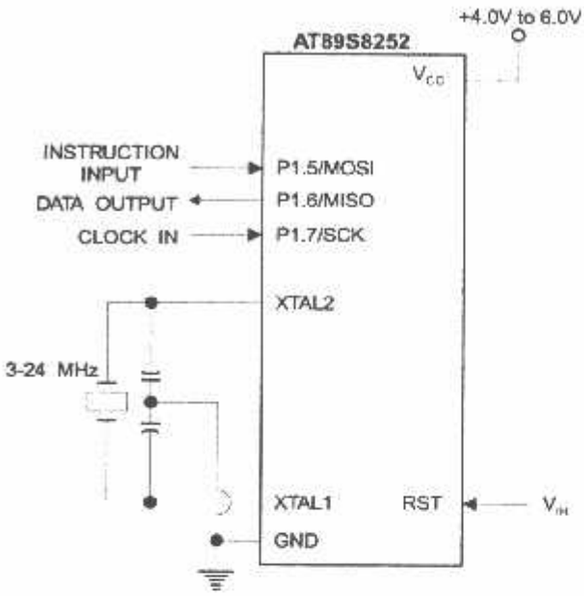
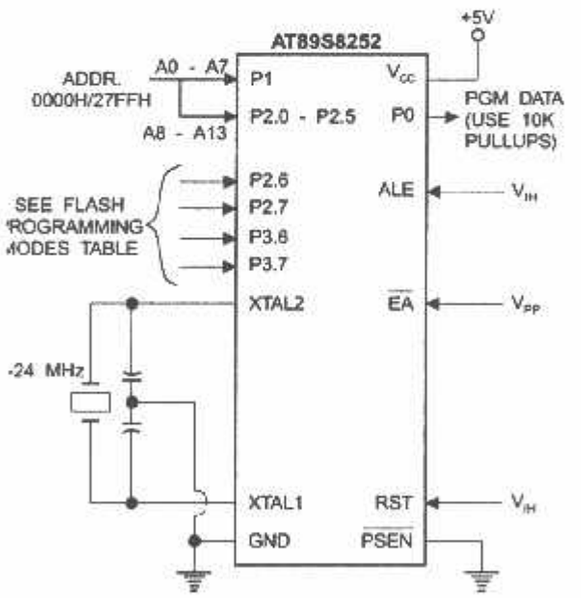


Figure 15. Flash/EEPROM Serial Downloading



gure 16. Verifying the Flash/EEPROM Memory

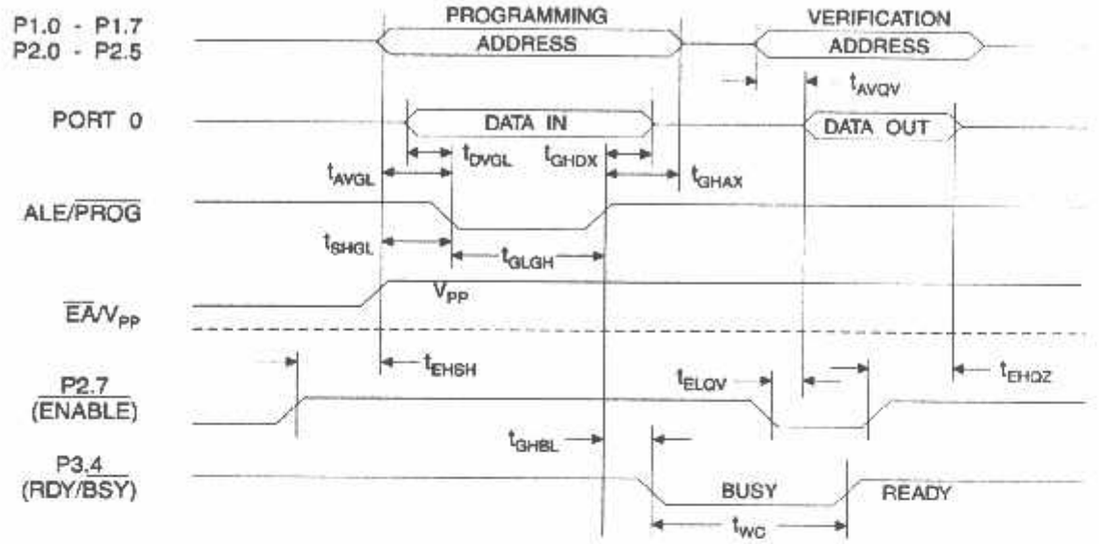


'lash Programming and Verification Characteristics-Parallel Mode

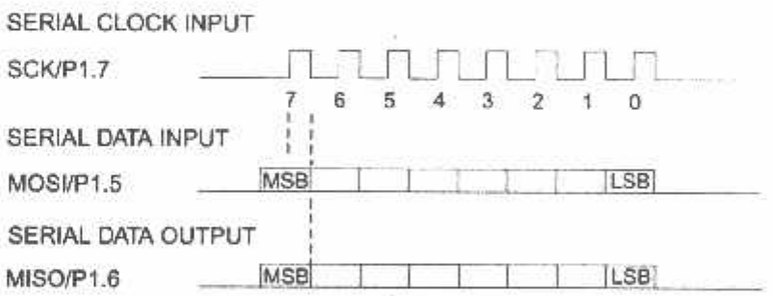
$_A$ = 0°C to 70°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
PP	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
AVGL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHAX	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
DVGL	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
GHDX	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
EHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
SHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
GLGH	$\overline{PROG}$ Width	1	110	µs
AVQV	Address to Data Valid		$48t_{CLCL}$	
ELQV	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
EHQZ	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
GHBL	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
WC	Byte Write Cycle Time		2.0	ms

Flash/EEPROM Programming and Verification Waveforms - Parallel Mode



Serial Downloading Waveforms



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage (1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
V_{OL1}	Output Low Voltage (1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
R_{RST}	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power Down Mode (2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V

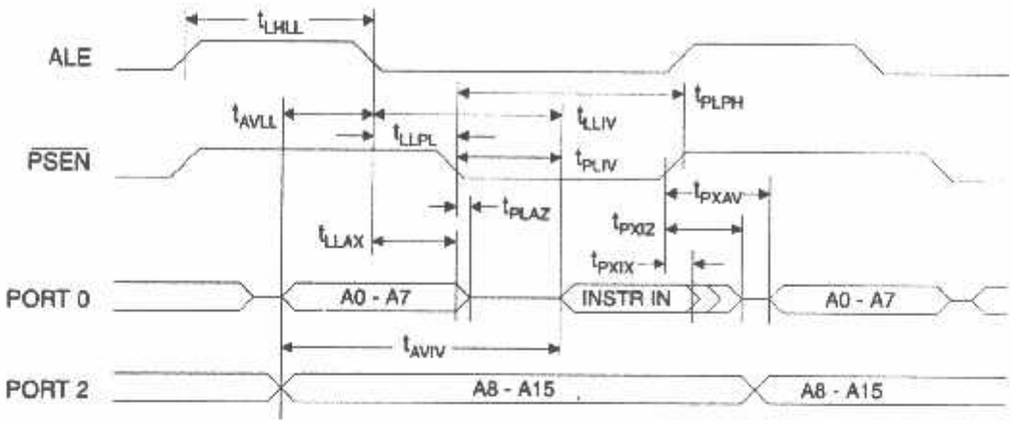
C Characteristics

ıder operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other tputs = 80 pF.

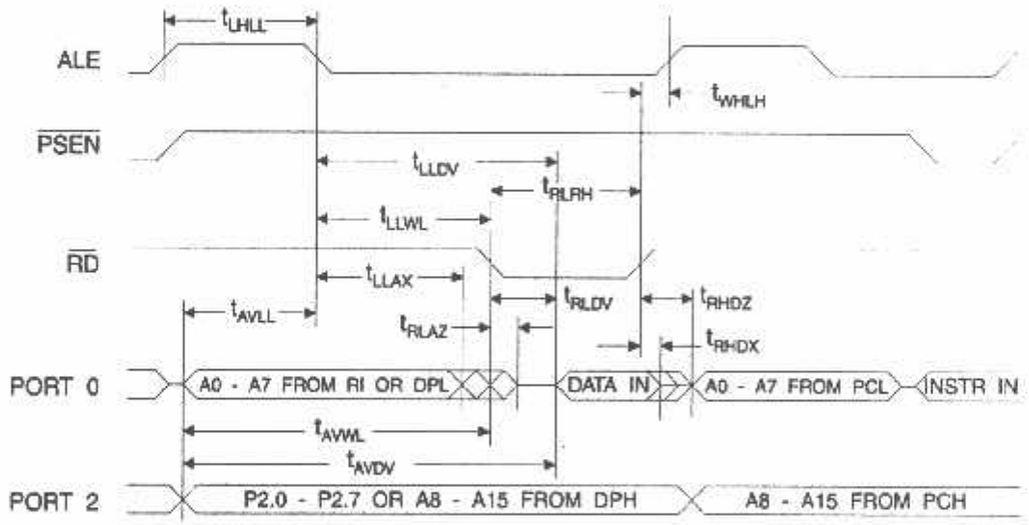
xternal Program and Data Memory Characteristics

ymbol	Parameter	Variable Oscillator		Units
		Min	Max	
/t_{CLCL}	Oscillator Frequency	0	24	MHz
HLL	ALE Pulse Width	$2t_{CLCL}$ - 40		ns
WLL	Address Valid to ALE Low	t_{CLCL} - 13		ns
LAX	Address Hold After ALE Low	t_{CLCL} - 20		ns
LIV	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
LPL	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
PLPH	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
PLIV	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
PXIX	Input Instruction Hold After $\overline{PSEN}$	0		ns
PXIZ	Input Instruction Float After $\overline{PSEN}$		t_{CLCL} - 10	ns
PXAV	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
AVIV	Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
PLAZ	$\overline{PSEN}$ Low to Address Float		10	ns
RLRH	$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
WLWH	$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
RLDV	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
RHDX	Data Hold After $\overline{RD}$	0		ns
RHDZ	Data Float After $\overline{RD}$		$2t_{CLCL}$ - 28	ns
LDV	ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
AVDV	Address to Valid Data In		$9t_{CLCL}$ - 165	ns
LWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
AVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
QVWX	Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
QVWH	Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
WHQX	Data Hold After $\overline{WR}$	t_{CLCL} - 20		ns
RLAZ	$\overline{RD}$ Low to Address Float		0	ns
WHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

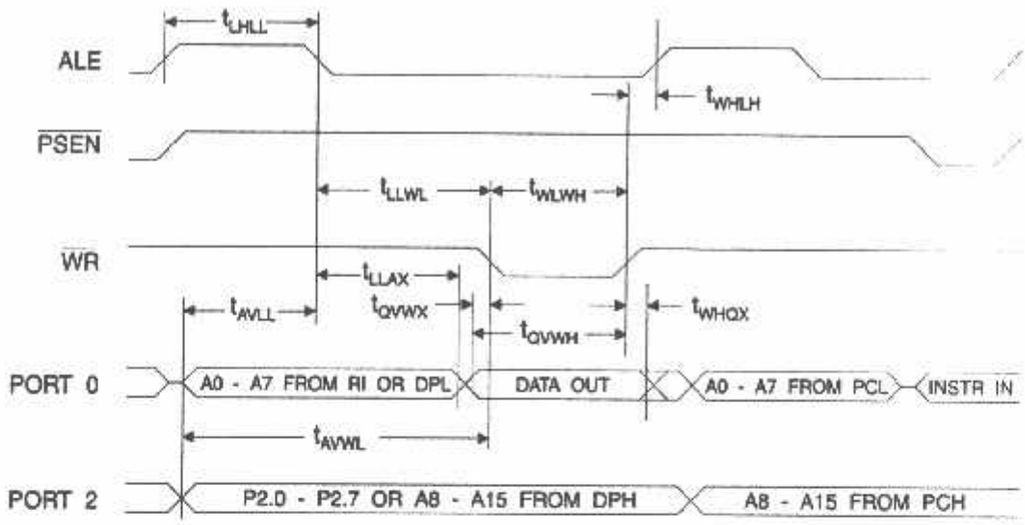
External Program Memory Read Cycle



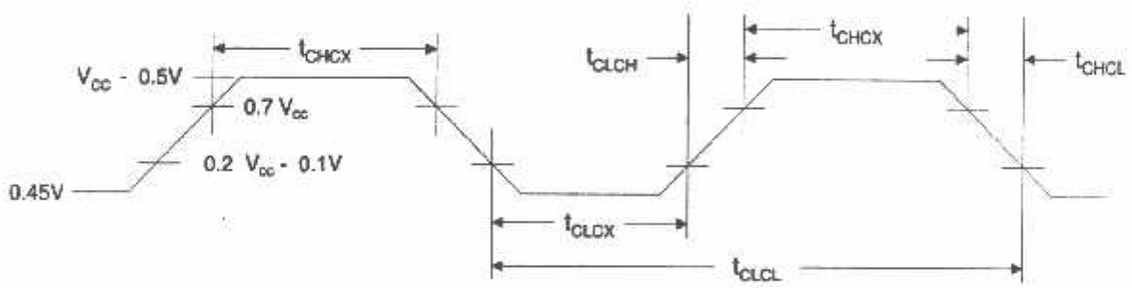
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

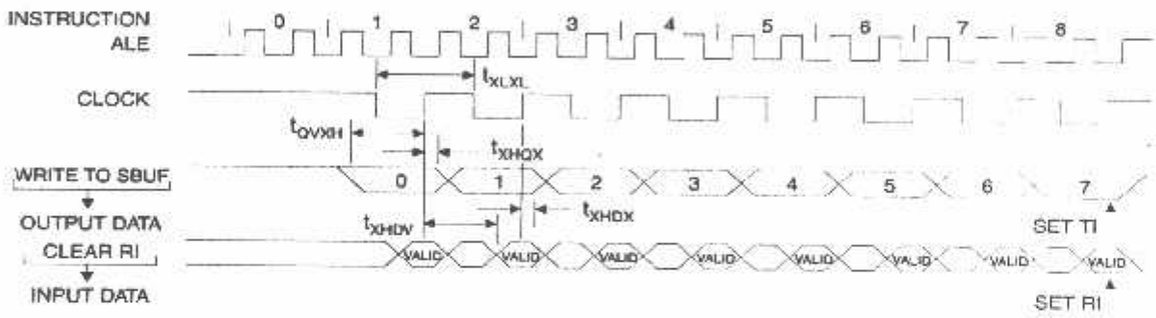
Symbol	Parameter	V_{CC} = 4.0V to 6.0V		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

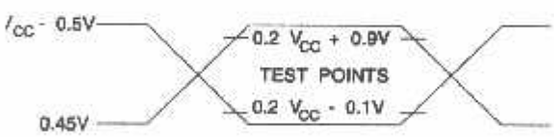
The values in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	$2t_{CLCL}$ - 117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

Shift Register Mode Timing Waveforms

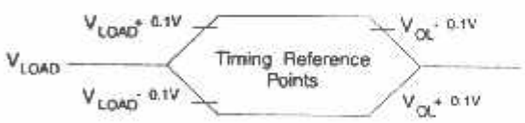


AC Testing Input/Output Waveforms(1)



Notes: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

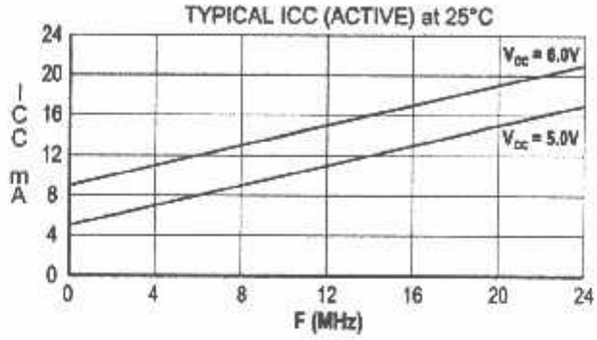
Float Waveforms(1)



Notes: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

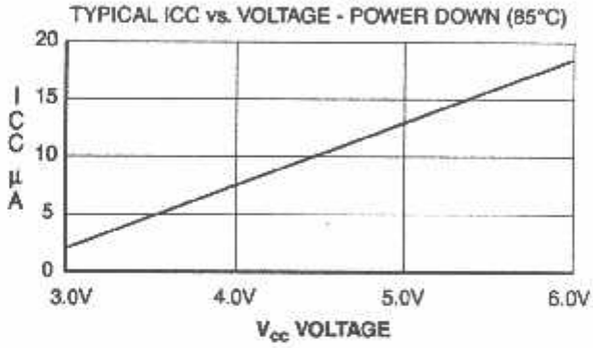
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



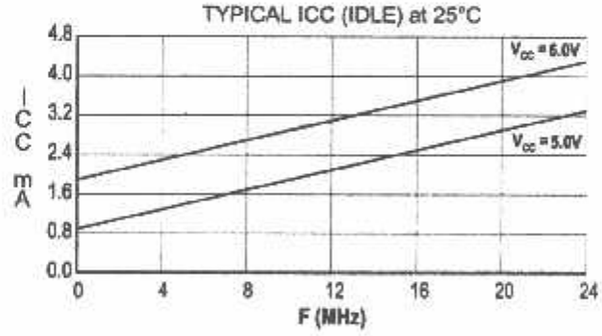
AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



AT89S8252

TYPICAL ICC (IDLE) at 25°C



ıtes: 1. XTAL1 tied to GND for Icc (power down)

2. Lock bits programmed

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
16	4.0V to 6.0V	AT89S8252-16AA AT89S8252-16JA AT89S8252-16PA AT89S8252-16QA	44A 44J 40P6 44Q	Automotive (-40°C to 105°C)
24	4.0V to 6.0V	AT89S8252-24AC AT89S8252-24JC AT89S8252-24PC AT89S8252-24QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
	4.0V to 6.0V	AT89S8252-24AI AT89S8252-24JI AT89S8252-24PI AT89S8252-24QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S8252-33AC AT89S8252-33JC AT89S8252-33PC AT89S8252-33QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)

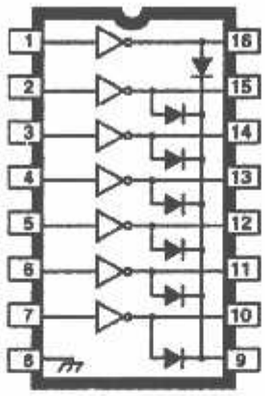
= Preliminary Information

	Package Type
4A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
4J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
0P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
4Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

2003 THRU 2024

Data Sheet 29304F

HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS



Dwg. No. A-9504

Note that the ULN20xxA series (dual in-line package) and ULN20xxL series (small-outline IC package) are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE}
(ULN200xA and ULN200xL) ..... **50 V**
(ULN202xA and ULN202xL) ..... **95 V**
Input Voltage, V_{IN} ..... **30 V**
Continuous Output Current, I_C ..... **500 mA**
Continuous Input Current, I_{IN} ..... **25 mA**
Power Dissipation, P_D
(one Darlington pair) ..... **1.0 W**
(total package) ..... **See Graph**
Operating Temperature Range, T_A ..... **-20°C to +85°C**
Storage Temperature Range, T_S ..... **-55°C to +150°C**

Ideally suited for interfacing between low-level logic circuitry and multiple peripheral power loads, the Series ULN20xxA/L high-voltage, high-current Darlington arrays feature continuous load current ratings to 500 mA for each of the seven drivers. At an appropriate duty cycle depending on ambient temperature and number of drivers turned ON simultaneously, typical power loads totaling over 230 W (350 mA x 7, 95 V) can be controlled. Typical loads include relays, solenoids, stepping motors, magnetic print hammers, multiplexed LED and incandescent displays, and heaters. All devices feature open-collector outputs with integral clamp diodes.

The ULN2003A/L and ULN2023A/L have series input resistors selected for operation directly with 5 V TTL or CMOS. These devices will handle numerous interface needs — particularly those beyond the capabilities of standard logic buffers.

The ULN2004A/L and ULN2024A/L have series input resistors for operation directly from 6 to 15 V CMOS or PMOS logic outputs.

The ULN2003A/L and ULN2004A/L are the standard Darlington arrays. The outputs are capable of sinking 500 mA and will withstand at least 50 V in the OFF state. Outputs may be paralleled for higher load current capability. The ULN2023A/L and ULN2024A/L will withstand 95 V in the OFF state.

These Darlington arrays are furnished in 16-pin dual in-line plastic packages (suffix "A") and 16-lead surface-mountable SOICs (suffix "L"). All devices are pinned with outputs opposite inputs to facilitate ease of circuit board layout. All devices are rated for operation over the temperature range of -20°C to +85°C. Most (see matrix, next page) are also available for operation to -40°C; to order, change the prefix from "ULN" to "ULQ".

FEATURES

- TTL, DTL, PMOS, or CMOS-Compatible Inputs
- Output Current to 500 mA
- Output Voltage to 95 V
- Transient-Protected Outputs
- Dual In-Line Plastic Package or Small-Outline IC Package

x = digit to identify specific device. Characteristic shown applies to family of devices with remaining digits as shown. See matrix on next page.

Allegro MicroSystems, Inc.

2003 THRU 2024
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

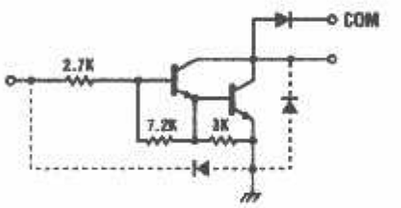
DEVICE PART NUMBER DESIGNATION

$V_{CE(MAX)}$	50 V	95 V
$I_{C(MAX)}$	500 mA	500 mA
Logic	**Part Number**	
5V TTL, CMOS	ULN2003A* ULN2003L*	ULN2023A* ULN2023L
6-15 V CMOS, PMOS	ULN2004A* ULN2004L*	ULN2024A ULN2024L

*Also available for operation between -40°C and +85°C. To order, change prefix from "ULN" to "ULQ".

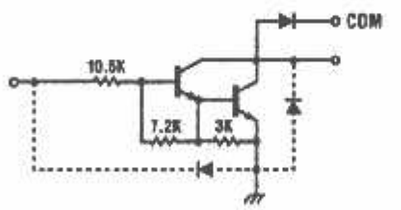
PARTIAL SCHEMATICS

ULN20x3A/L (Each Driver)

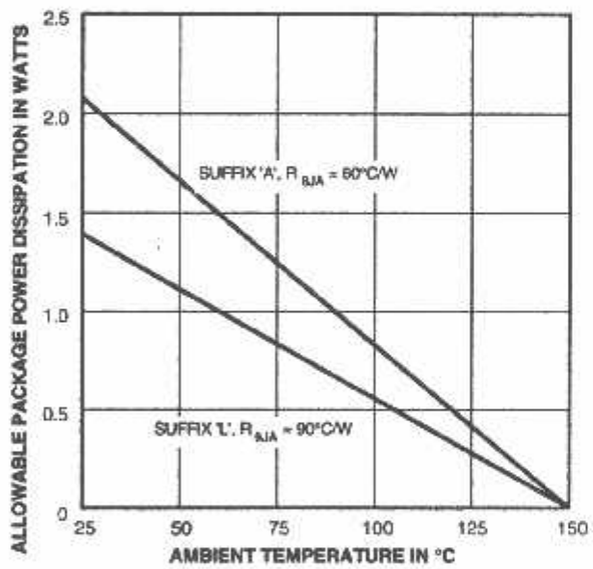


Dwg. No. A-9651

ULN20x4A/L (Each Driver)



Dwg. No. A-9696A



Dwg. GP-006A

X = Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown. See matrix above.

Allegro MicroSystems, Inc.

115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

Types ULN2003A, ULN2003L, ULN2004A, and ULN2004L
ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted).

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			
					Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	< 1	50	µA
				V_{CE} = 50 V, T_A = 70°C	—	< 1	100	µA
		1B	ULN2004A/L	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	< 5	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 µA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 µA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 µA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN2003A/L	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN2004A/L	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 µA, T_A = 70°C	50	65	—	µA
Input Voltage	$V_{IN(ON)}$	5	ULN2003A/L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN2004A/L	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{PLH}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Turn-Off Delay	t_{PHL}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	µA
				V_R = 50 V, T_A = 70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

Complete part number includes suffix to identify package style: A = DIP, L = SOIC.

ypes ULN2023A, ULN2023L, ULN2024A, and ULN2024L
LECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted).

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			
					Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 95 V, T_A = 25°C	—	< 1	50	µA
				V_{CE} = 95 V, T_A = 70°C	—	< 1	100	µA
		1B	ULN2024A/L	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 1.0 V	—	< 5	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 µA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 µA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 µA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN2023A/L	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN2024A/L	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 µA, T_A = 70°C	50	65	—	µA
Input Voltage	$V_{IN(ON)}$	5	ULN2023A/L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN2024A/L	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{PLH}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Turn-Off Delay	t_{PHL}	8	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Clamp Diode Leakage Current	I_R	6	All	V_R = 95 V, T_A = 25°C	—	—	50	µA
				V_R = 95 V, T_A = 70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

Complete part number includes suffix to identify package style: A = DIP, L = SOIC.

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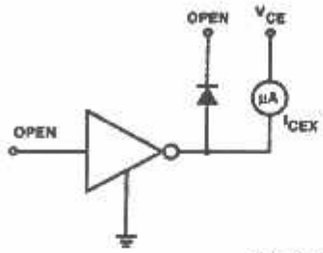
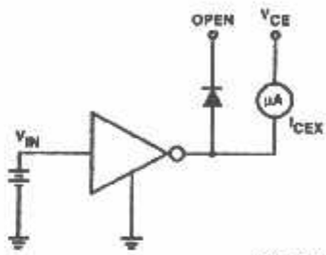
TEST FIGURES

FIGURE 1A



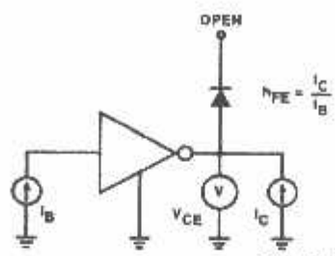
Dwg. No. A-9729A

FIGURE 1B



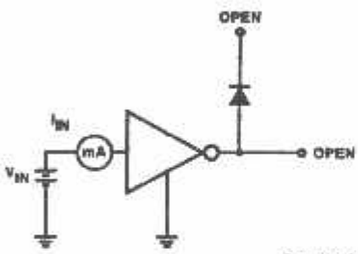
Dwg. No. A-9730A

FIGURE 2



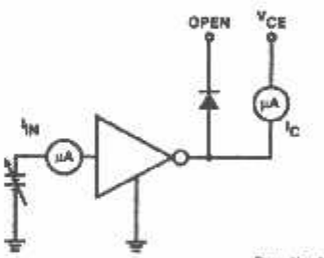
Dwg. No. A-9731A

FIGURE 3



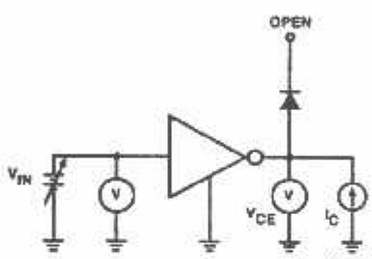
Dwg. No. A-9732A

FIGURE 4



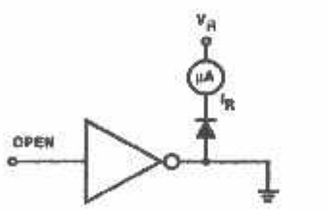
Dwg. No. A-9733A

FIGURE 5



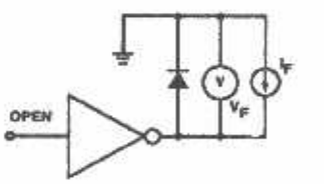
Dwg. No. A-9734A

FIGURE 6



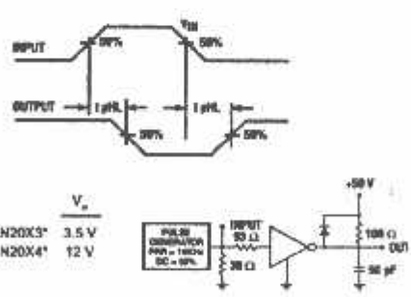
Dwg. No. A-9735A

FIGURE 7



Dwg. No. A-9736A

FIGURE 8



	V_{in}
ULN20X3*	3.5 V
ULN20X4*	12 V

Complete part number includes a final letter to indicate package.

* = Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown.

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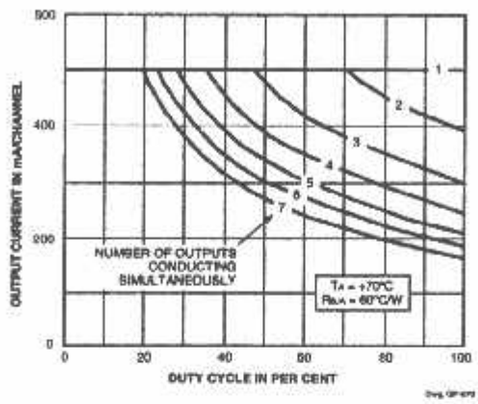
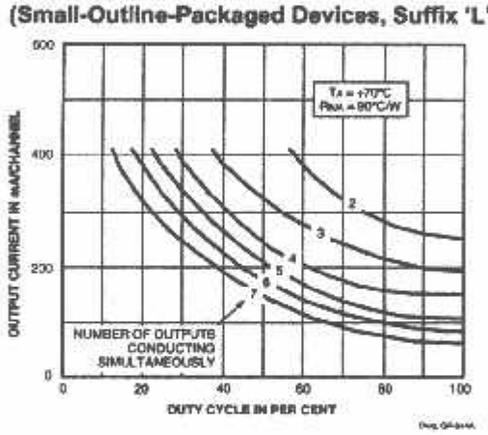
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

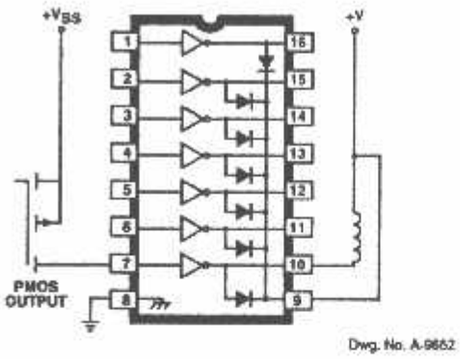
(Dual In-line-Packaged Devices, Suffix 'A')



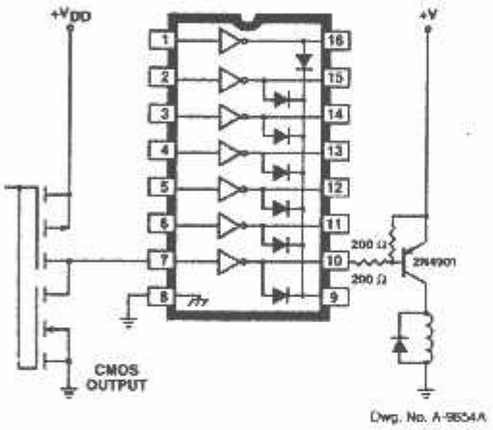
(Small-Outline-Packaged Devices, Suffix 'L')



TYPICAL APPLICATIONS

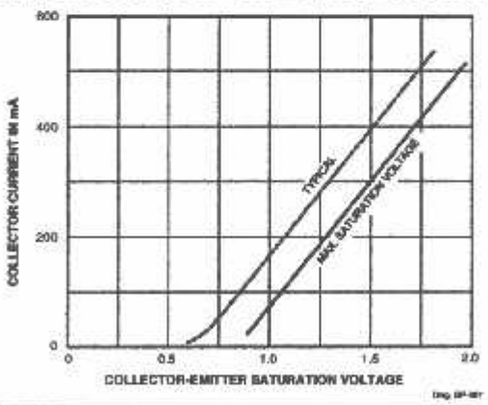


Dwg. No. A-9852

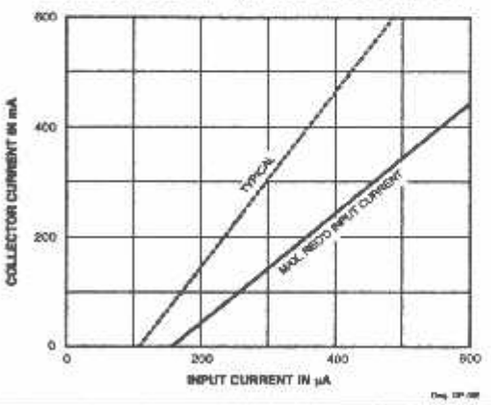


Dwg. No. A-9854A

SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



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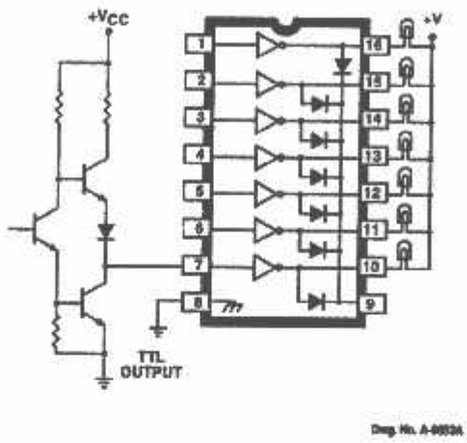
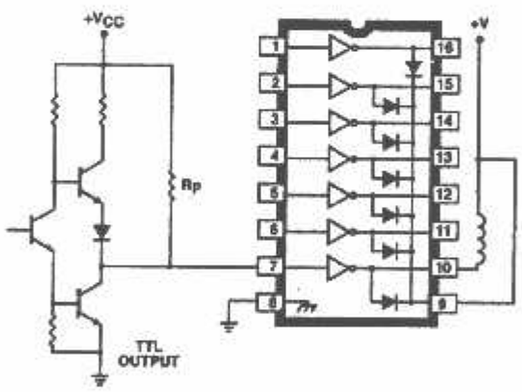
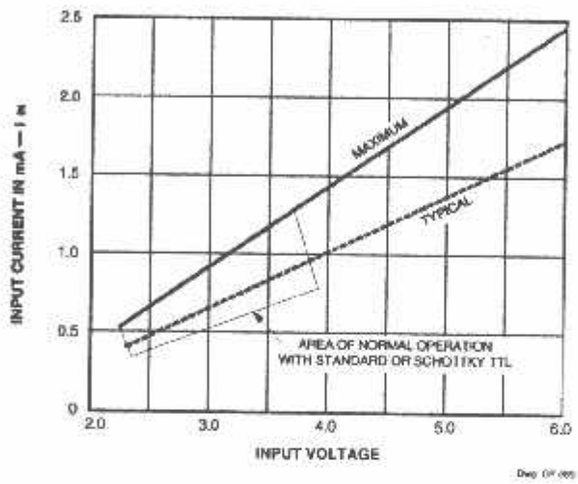
TYPICAL APPLICATIONS



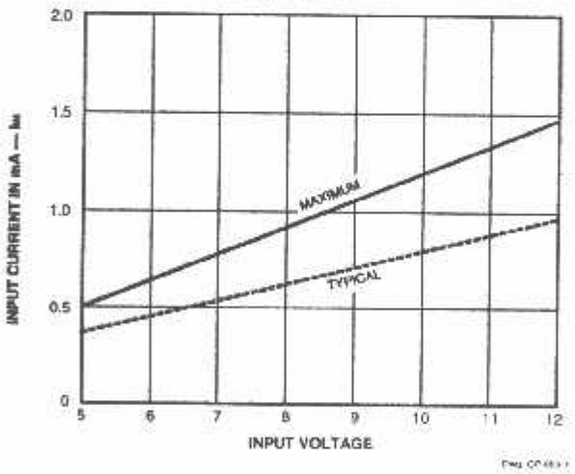


INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

Types ULN2003A, ULN2003L, ULN2023A, and ULN2023L

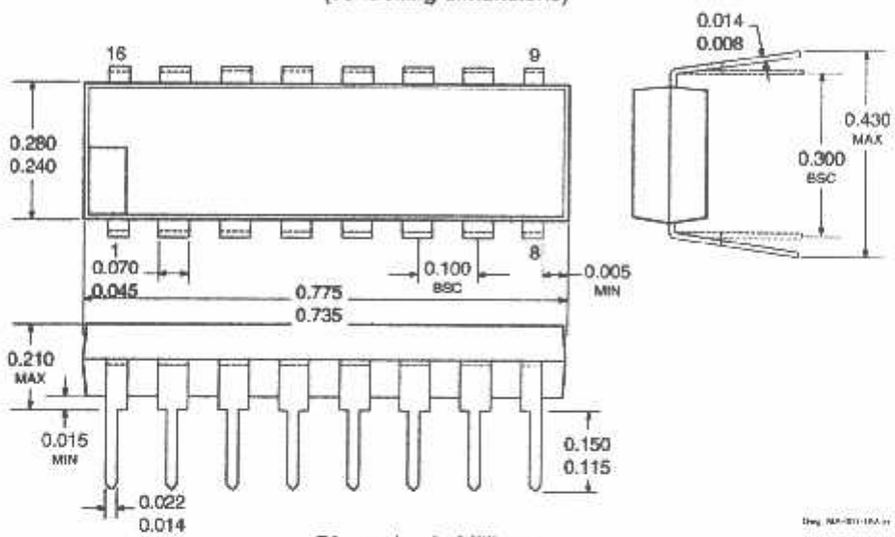


Types ULN2004A, ULN2004L, ULN2024A, and ULN2024L

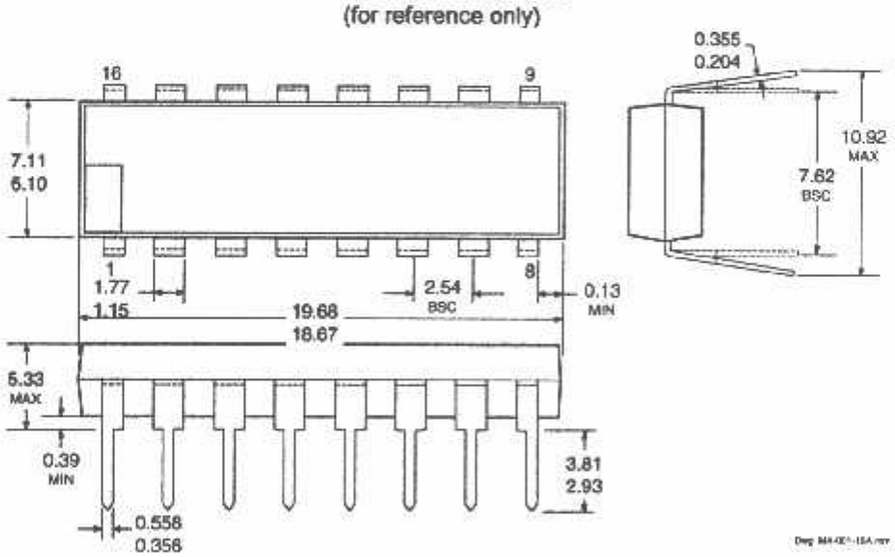


PACKAGE DESIGNATOR "A"

Dimensions in Inches
(controlling dimensions)



Dimension in Millimeters
(for reference only)



NOTES: 1. Leads 1, 8, 9, and 16 may be half leads at vendor's option.
2. Lead thickness is measured at seating plane or below.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown.

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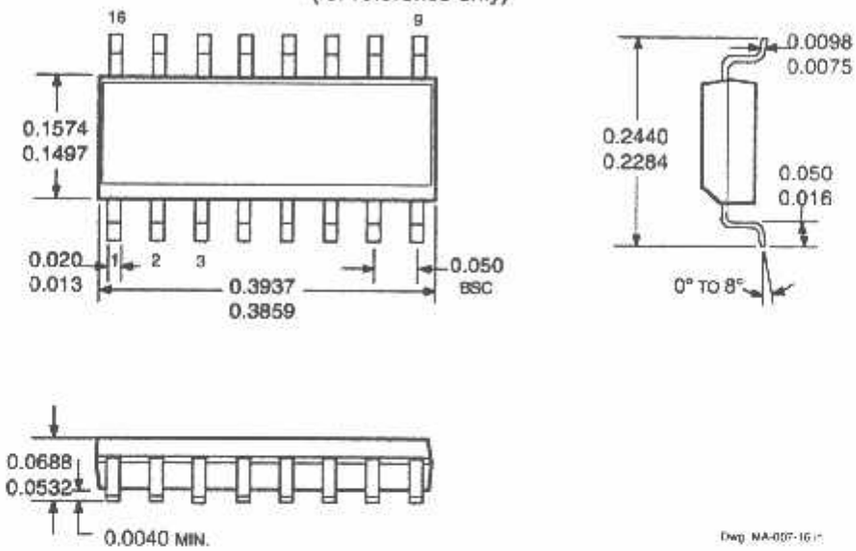
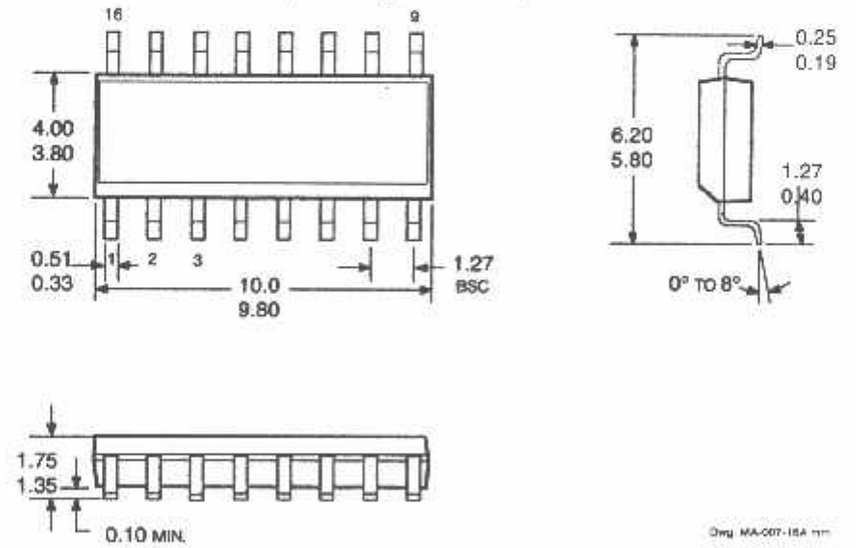
PACKAGE DESIGNATOR "L"

Dimensions in Inches
(for reference only)



Dwg. MA-007-16

Dimension in Millimeters
(controlling dimensions)



Dwg. MA-007-16A mm

NOTES: 1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.

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National Semiconductor

November 1999

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

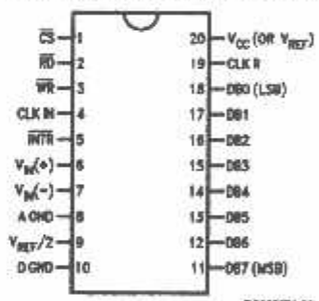
- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 µs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages



DS005671-30

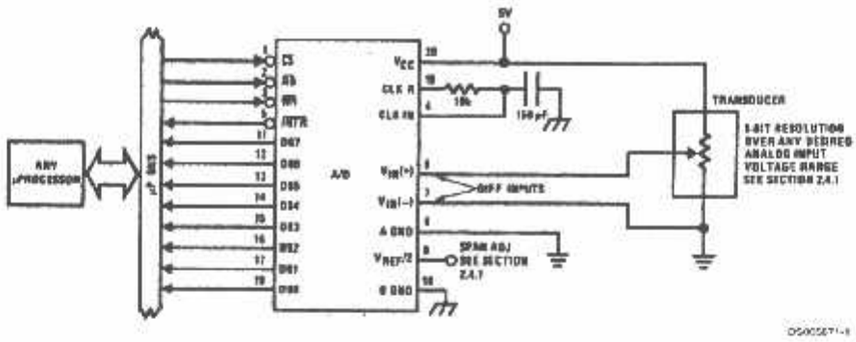
See Ordering Information

Ordering Information

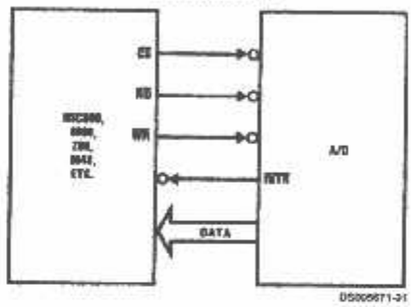
TEMP RANGE		0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted			ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM		ADC0802LCN
	±½ Bit Adjusted			ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCN	ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B—Small Outline	N20A—Molded DIP	

Z-80® is a registered trademark of Zilog Corp.

Typical Applications



8080 Interface



Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2$=2.500 V_{DC} (No Adjustments)	$V_{REF}/2$=No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0804LCJ	−40°C ≤ T_A ≤ +85°C
ADC0801/02/03/05LCN	−40°C ≤ T_A ≤ +85°C
ADC0804LCN	0°C ≤ T_A ≤ +70°C
ADC0802/04LCWM	0°C ≤ T_A ≤ +70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2$=2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2$=2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			±1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05	2.5	8.0		kΩ
	ADC0804 (Note 9)	0.75	1.1		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_C	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Notes 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency	V_{CC}=5V, (Note 5)	100	640	1460	kHz
	Clock Duty Cycle		40		60	%
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ =0 V_{DC}, f_{CLK}=640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ =0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN}=0 V_{DC}	-1	-0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis (V_T+)-(V_T-)		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O=360 µA V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O=-360 µA V_{CC}=4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT}=1.6 mA, V_{CC}=4.75 V_{DC} I_{OUT}=1.0 mA, V_{CC}=4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=-360 µA, V_{CC}=4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=-10 µA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0 V_{DC} V_{OUT}=5 V_{DC}	-3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A=25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A=25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCWM	f_{CLK}=640 kHz, $V_{REF}/2$=NC, T_A=25°C and $\overline{CS}$ =5V		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct--especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 4* and section 2.0.

AC Electrical Characteristics (Continued)

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

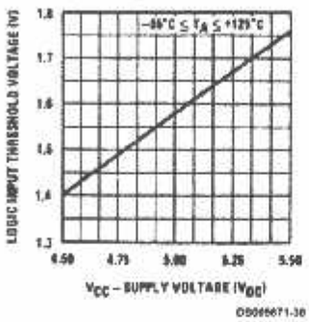
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 7*.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

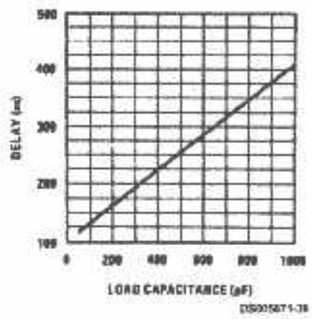
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

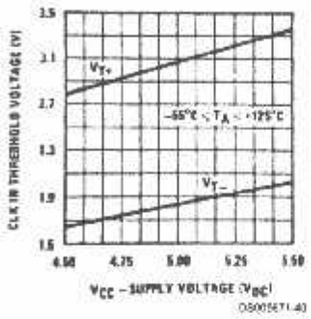
Logic Input Threshold Voltage vs. Supply Voltage



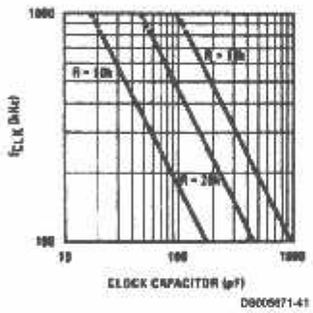
Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance



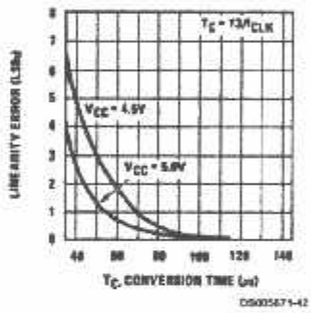
CLK IN Schmitt Trip Levels vs. Supply Voltage



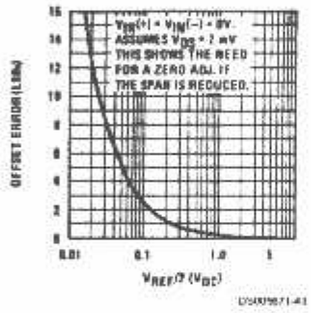
f_{CLK} vs. Clock Capacitor



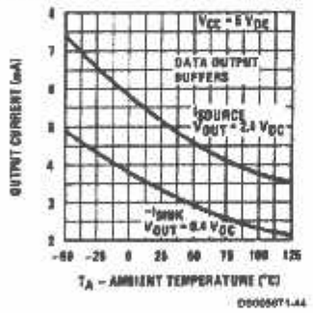
Full-Scale Error vs Conversion Time



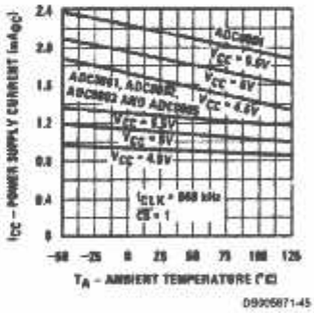
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



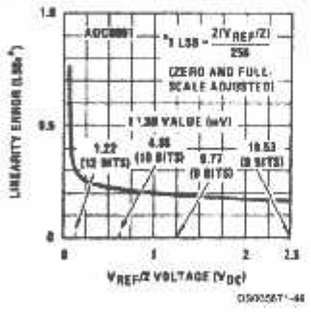
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)

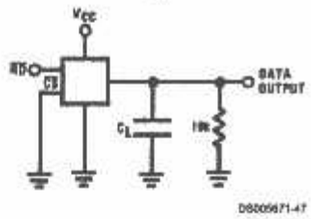


Linearity Error at Low $V_{REF}/2$ Voltages

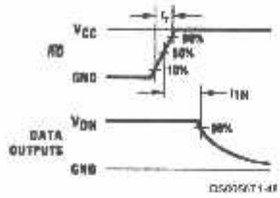


TRI-STATE Test Circuits and Waveforms

t_{1H}

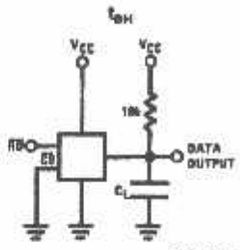


t_{1H}, C_L=10 pF

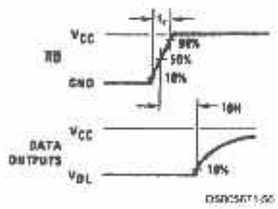


t_r=20 ns

t_{0H}

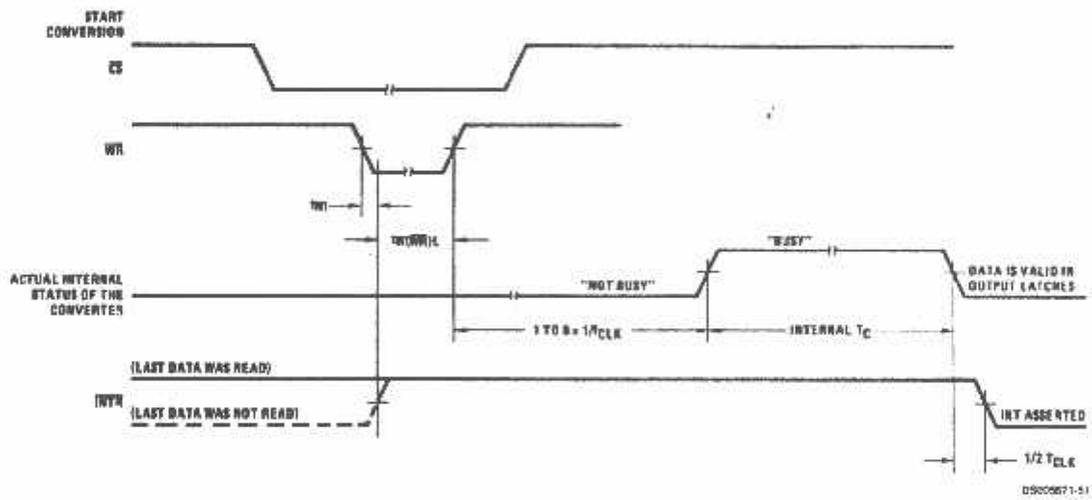


t_{0H}, C_L=10 pF



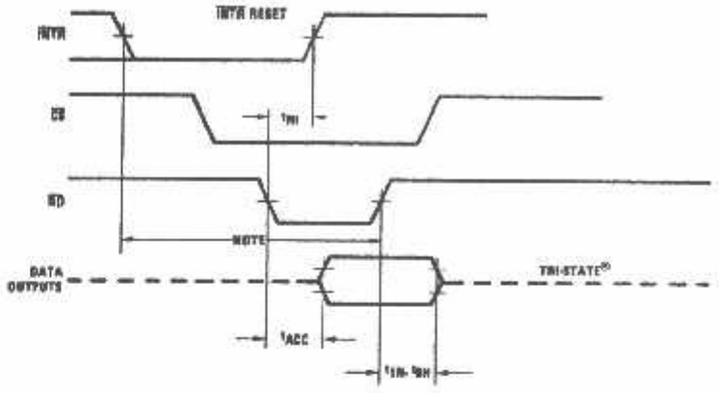
t_r=20 ns

Timing Diagrams (All timing is measured from the 50% voltage points)



Timing Diagrams (All timing is measured from the 50% voltage points) (Continued)

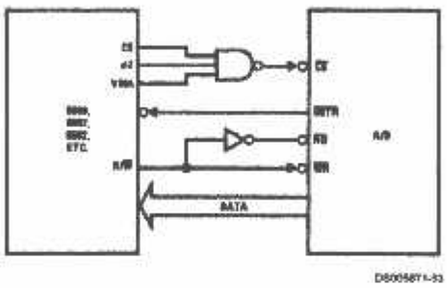
Output Enable and Reset with $\overline{INTR}$



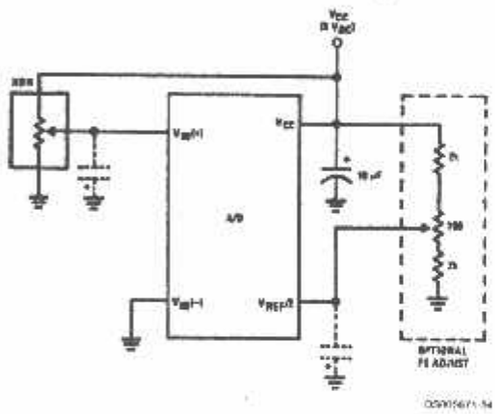
Note: Read strobe must occur 8 clock periods ($8t_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

Typical Applications

6800 Interface



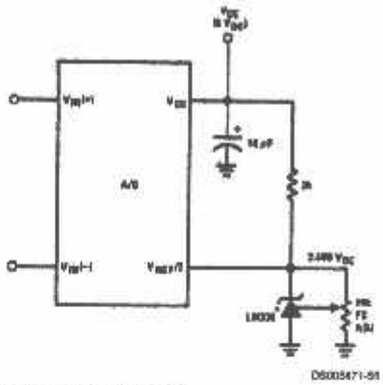
Ratiometeric with Full-Scale Adjust



Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

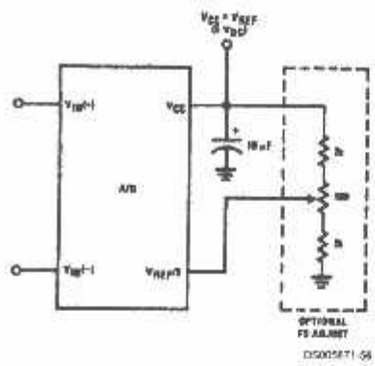
Typical Applications (Continued)

Absolute with a 2.500V Reference

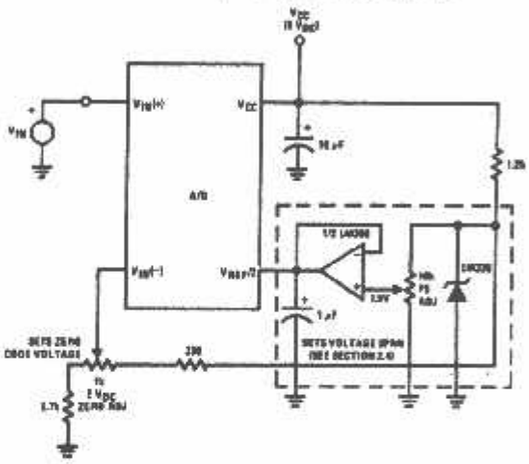


*For low power, see also LM385–2.5

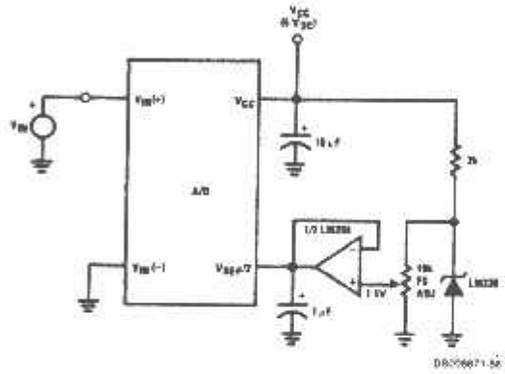
Absolute with a 5V Reference



Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V

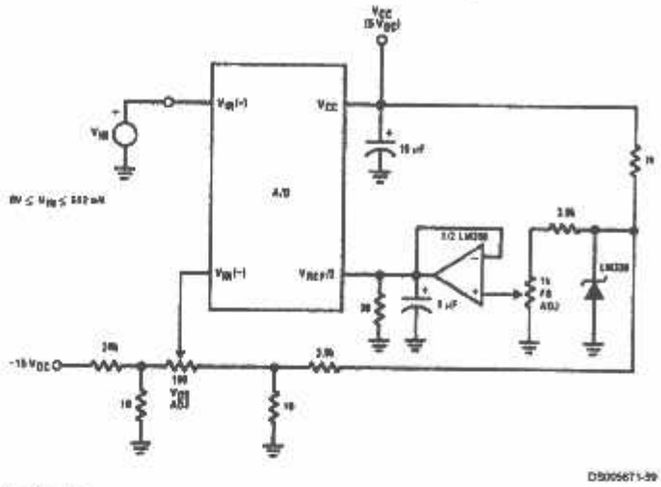


Span Adjust: 0V ≤ V_{IN} ≤ 3V



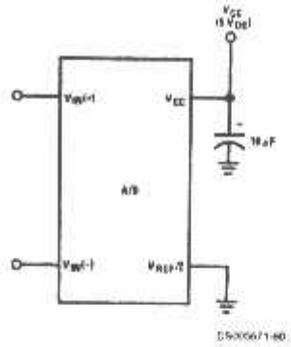
Typical Applications (Continued)

Directly Converting a Low-Level Signal



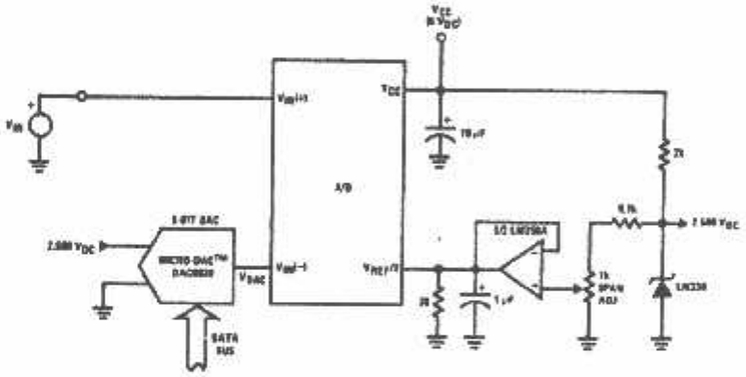
$V_{REF}/2$=256 mV

A µP Interfaced Comparator



For
$V_{IN}(+) > V_{IN}(-)$
Output=FF_{HEX}
For
$V_{IN}(+) < V_{IN}(-)$
Output=00_{HEX}

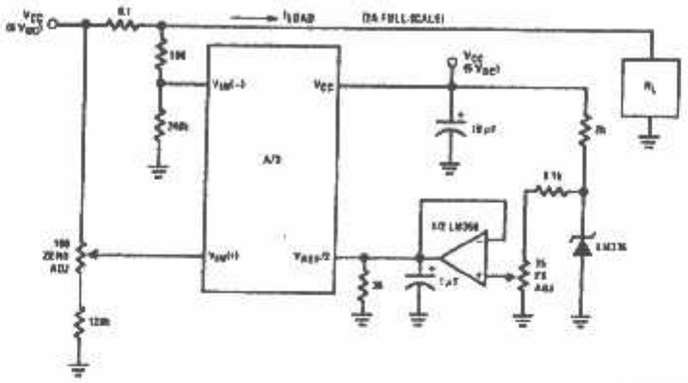
1 mV Resolution with µP Controlled Range



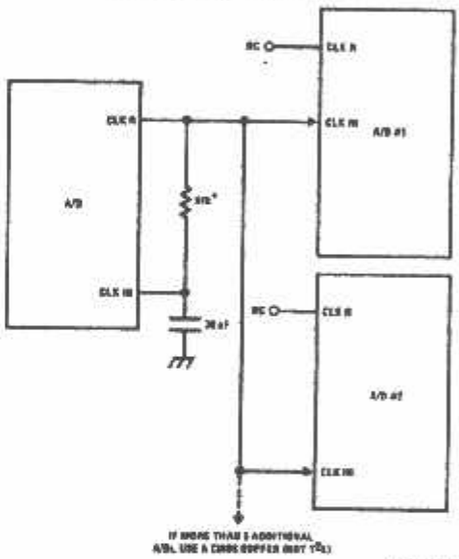
$V_{REF}/2$=128 mV
1 LSB=1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC}+256\ mV)$
$0 \leq V_{DAC} < 2.5V$

Typical Applications (Continued)

Digitizing a Current Flow

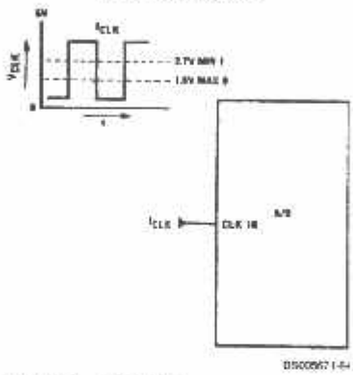


Self-Clocking Multiple A/Ds



* Use a large R value to reduce loading at CLK R output.

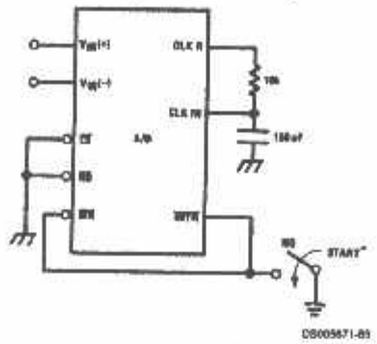
External Clocking



100 kHz≤f_{CLK}≤1460 kHz

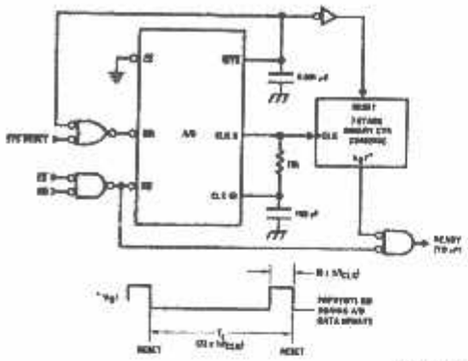
Typical Applications (Continued)

Self-Clocking in Free-Running Mode

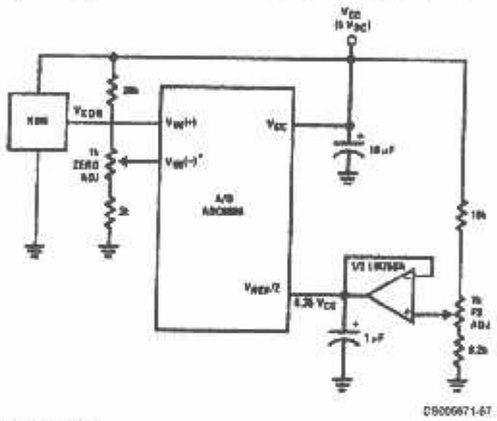


*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

µP Interface for Free-Running A/D

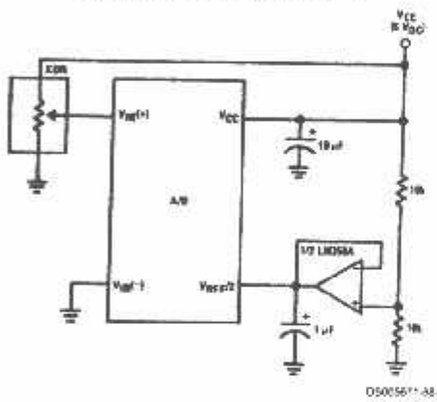


Operating with "Automotive" Ratiometric Transducers

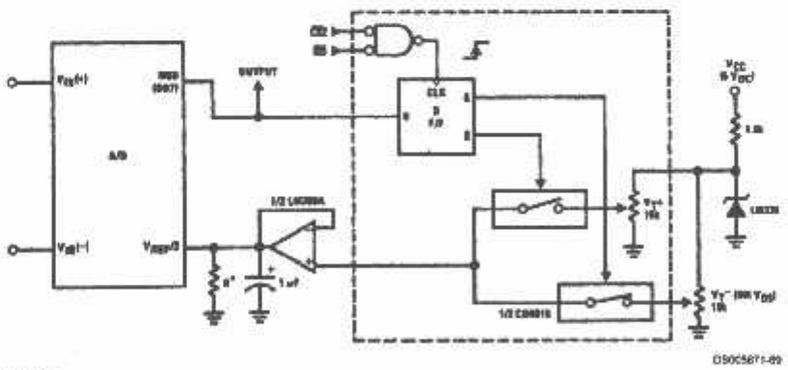


*$V_{IN}(-)=0.15\ V_{CC}$
$15\%\ of\ V_{CC} \le V_{REF} \le 85\%\ of\ V_{CC}$

Ratiometric with $V_{REF}/2$ Forced



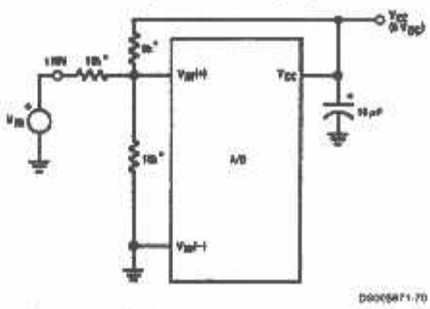
µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)



*See *Figure 5* to select R value
DB7="1" for $V_{IN}(+) > V_{IN}(-)+(V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

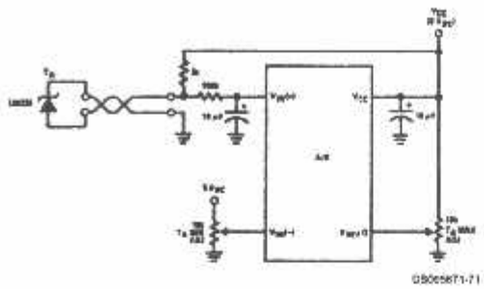
Typical Applications (Continued)

Handling ±10V Analog Inputs

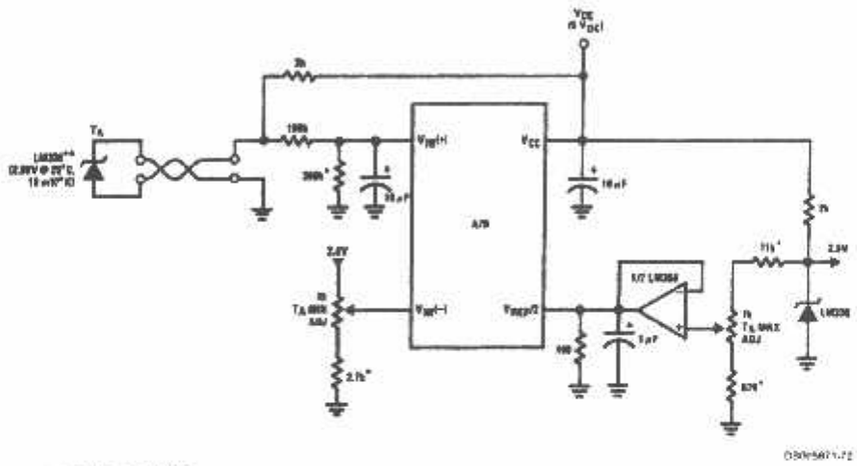


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



µP Interfaced Temperature-to-Digital Converter

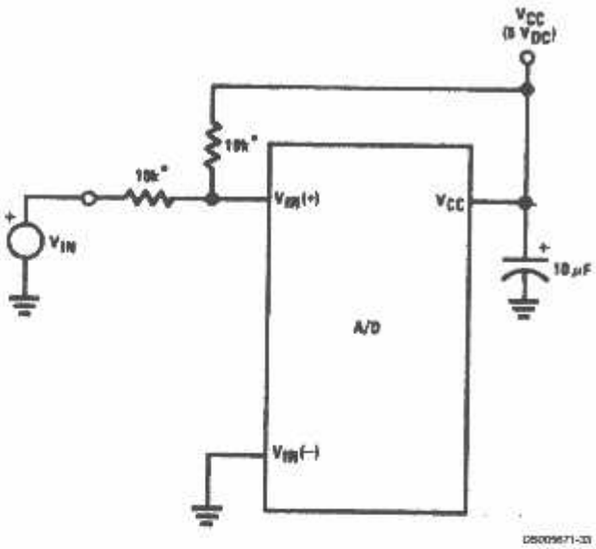


*Circuit values shown are for $0°C \leq T_A \leq +126°C$

**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

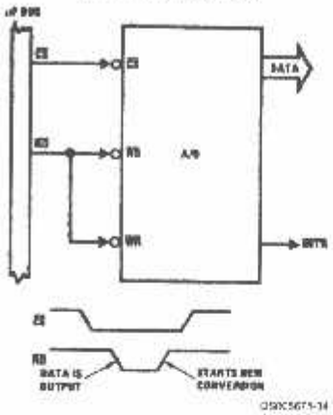
Typical Applications (Continued)

Handling ±5V Analog Inputs

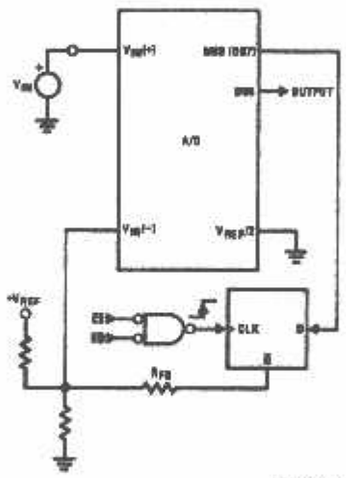


*Beckman Instruments #894-3-R10K resistor array

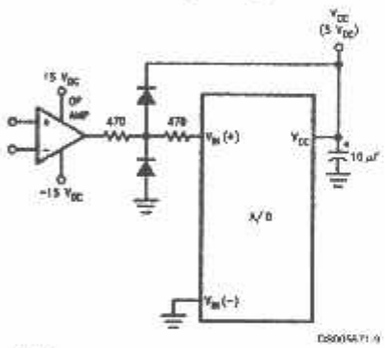
Read-Only Interface



µP Interfaced Comparator with Hysteresis



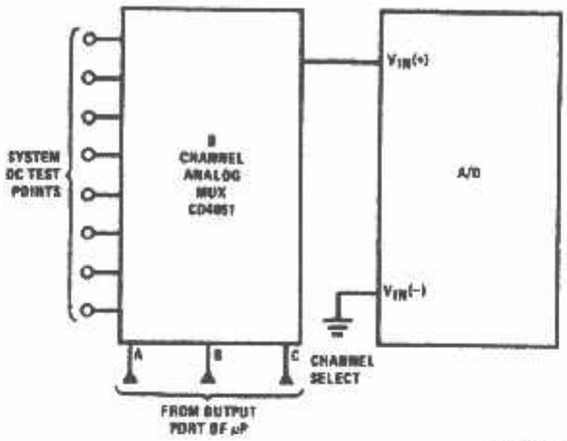
Protecting the Input



Diodes are 1N914

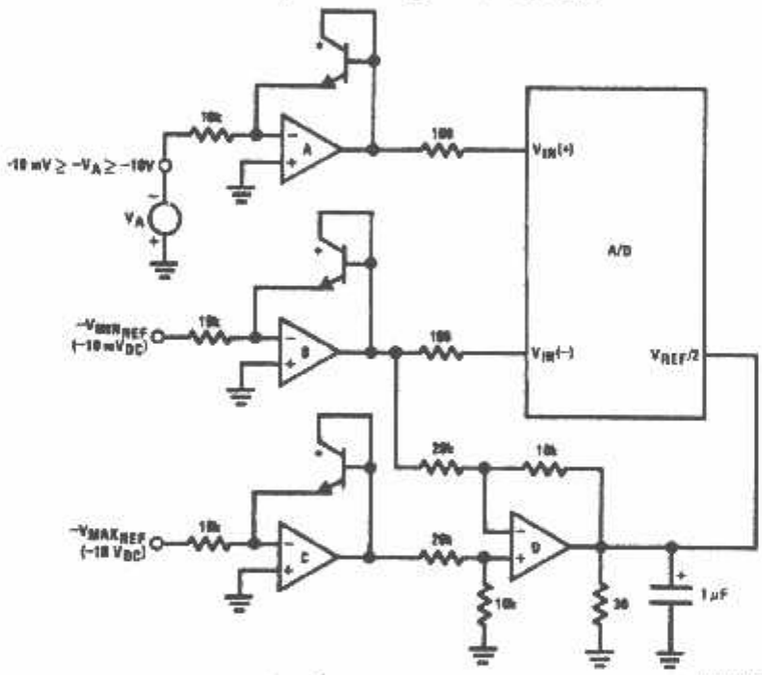
Typical Applications (Continued)

Analog Self-Test for a System



DS005671-36

A Low-Cost, 3-Decade Logarithmic Converter



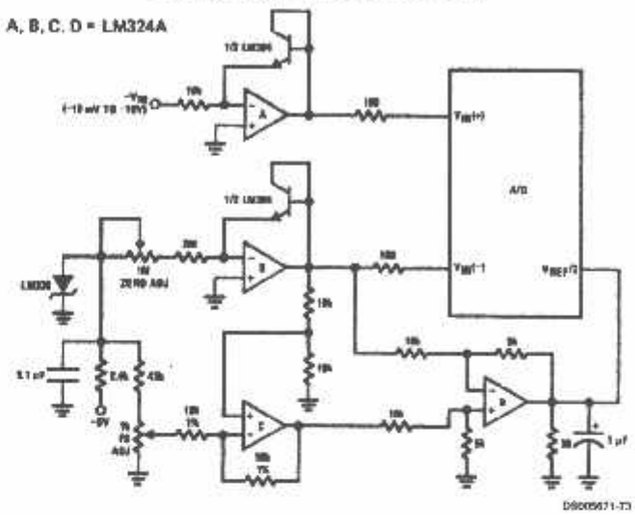
DS005671-37

*LM389 transistors
A, B, C, D = LM324A quad op amp

Typical Applications (Continued)

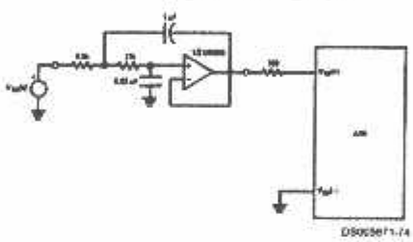
3-Decade Logarithmic A/D Converter

A, B, C, D = LM324A



DS005671-73

Noise Filtering the Analog Input



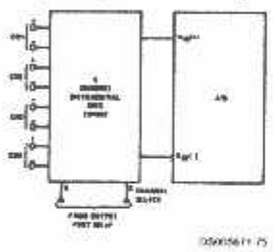
DS005671-74

f_C = 20 Hz

Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter

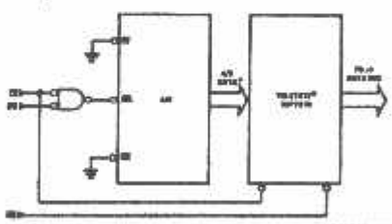
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs



DS005671-75

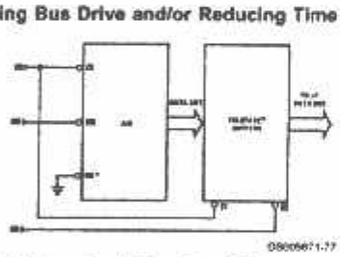
Output Buffers with A/D Data Enabled



DS005671-76

*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

Increasing Bus Drive and/or Reducing Time on Bus

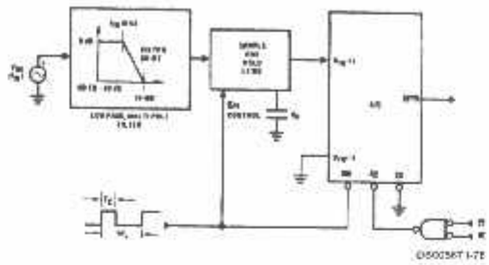


DS005671-77

*Allows output data to set-up at falling edge of $\overline{CS}$

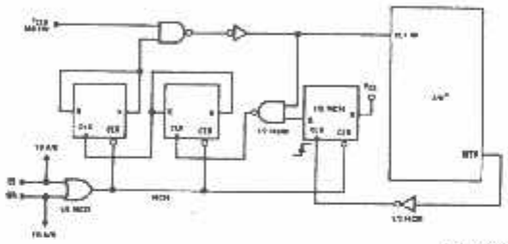
Typical Applications (Continued)

Sampling an AC Input Signal



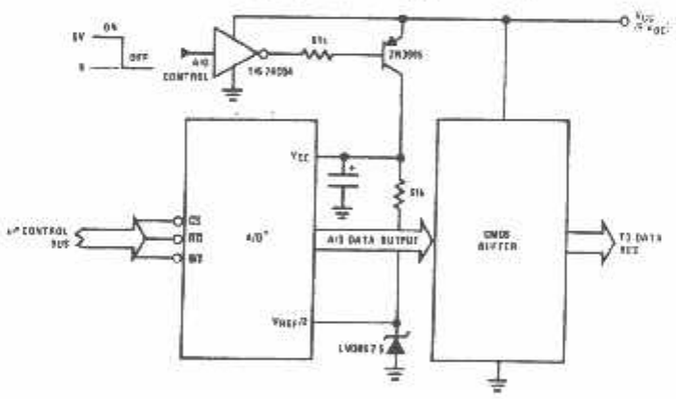
Note 11: Oversample whenever possible (keep fs > 2(f−BW)) to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.
Note 12: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes > 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



*Use ADC0801, 02, 03 or 05 for lowest power consumption.
Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.
Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as

0-1, 1, and 0-1. For the center-value (A 1, A, A+) the correct output digital code transitions between adjacent ±½ LSB away from each ... are ideal and have no width. ... be provided for a range of ...

Functional Description (Continued)

±¼ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Figure 2 shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, we *guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 3* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is [illegible] error plot. Many people may be [illegible] than transfer functions. The analog [illegible] is provided by either a linear ramp or [illegible] steps of a high resolution DAC. [illegible] continuously displayed and includes the [illegible] tainty of the A/D. For example the error [illegible] LSB [illegible] side steps are always 1 LSB in magnitude [illegible]

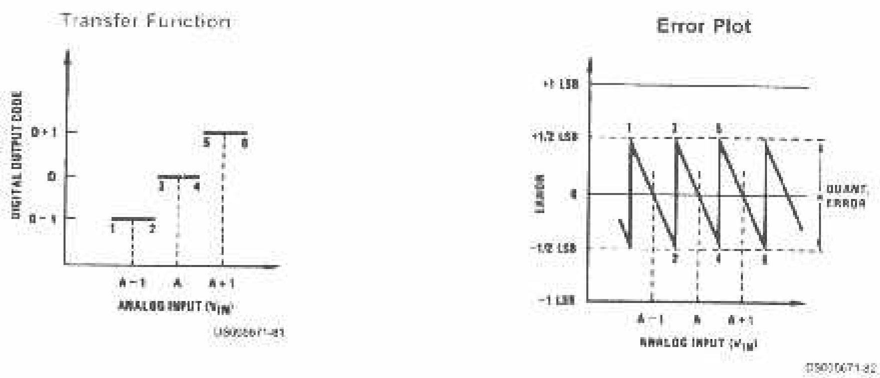


FIGURE 1. Clarifying the Error Specs of an A/D Converter Accuracy=±0 LSB: A Perfect A/D

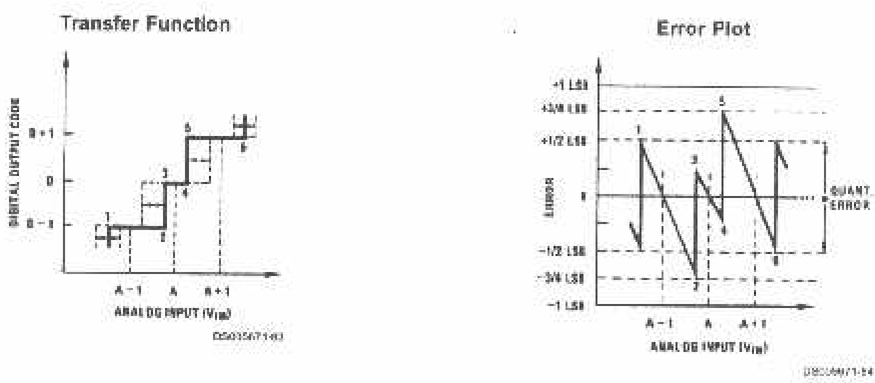


FIGURE 2. Clarifying the Error Specs of an A/D Converter Accuracy=±¼ LSB

Functional Description (Continued)

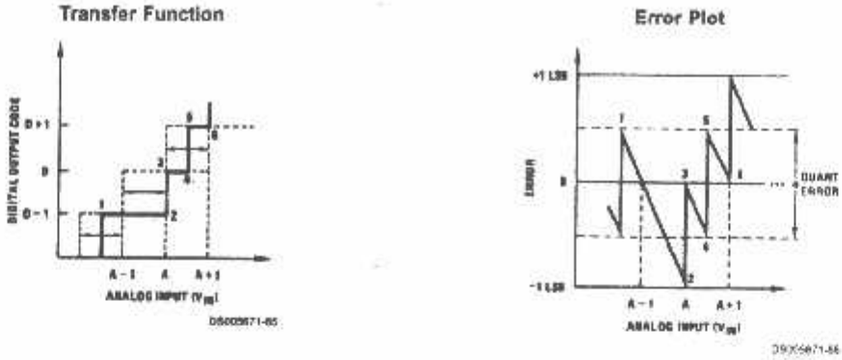


FIGURE 3. Clarifying the Error Specs of an A/D Converter
Accuracy = ±½ LSB

2.0 FUNCTIONAL DESCRIPTION

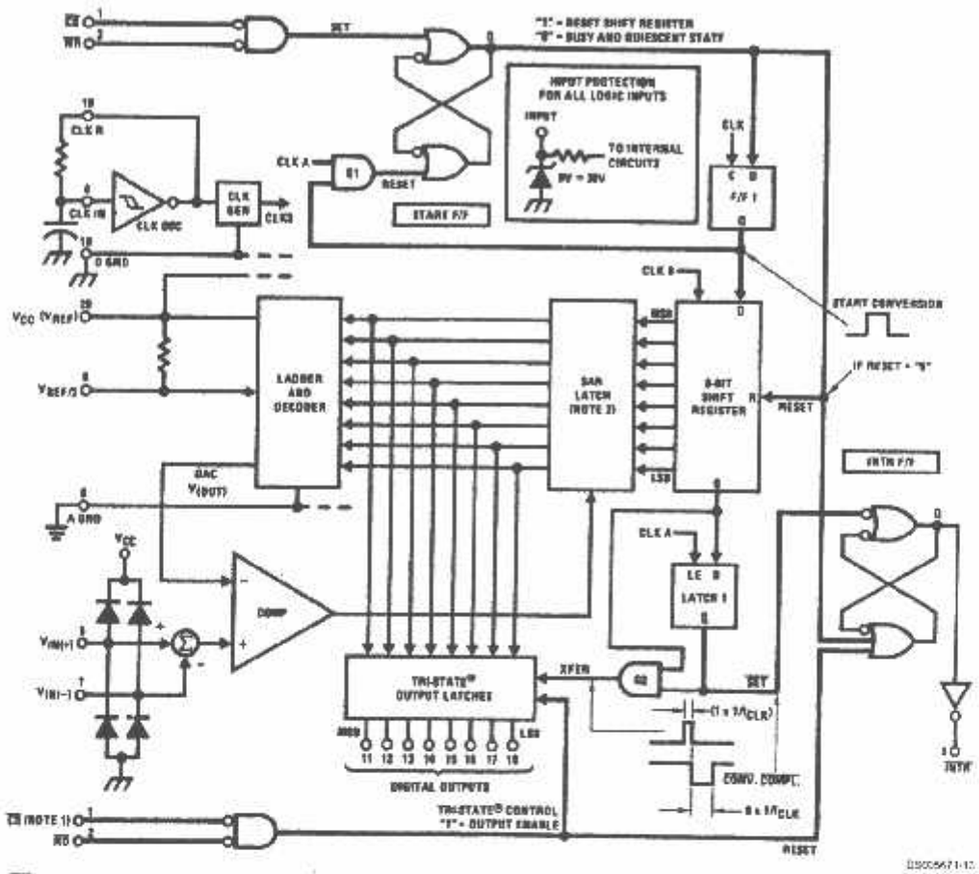
The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage $[V_{IN}(+) - V_{IN}(-)]$ to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ =0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 4*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the interrupt (INTR) F/F and inputs a "1" to the D flop, F/F 1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F 1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

Functional Description (Continued)



Note 13: $\overline{CS}$ shown twice for clarity.

Note 14: SAR = Successive Approximation Register.

FIGURE 4. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

Functional Description (Continued)

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right)$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)}$$

which gives

$V_P \approx 1.9V$.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

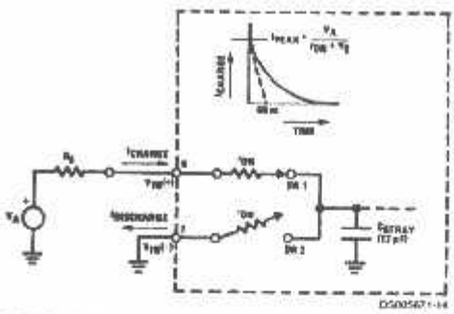
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3 1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 5*.



r_{ON} of SW 1 and SW 2 = 5 kΩ
$\tau = r_{ON} C_{STRAY}$ = 5 kΩ x 12 pF = 60 ns

FIGURE 5. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of V_{CC}+50 mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(-)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 µA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 µF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long

Functional Description (Continued)

wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 6*.

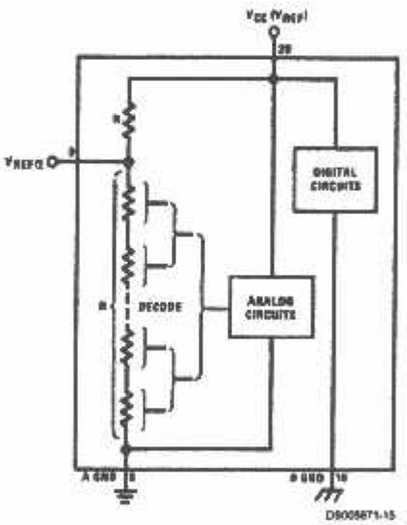


FIGURE 6. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply. a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

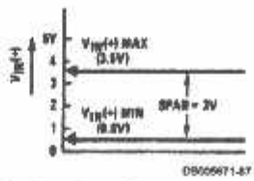
An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 7*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

2.4.2 Reference Accuracy Requirements

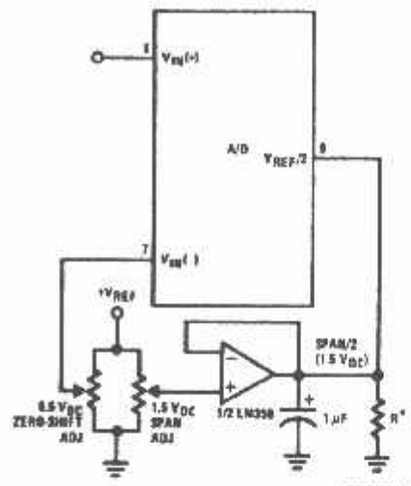
The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \le T_A \le +70°C$. Other temperature range parts are also available.

Functional Description (Continued)



a) Analog Input Signal Example



*Add if $V_{REF}/2 \leq 1\ V_{DC}$ with LM358 to draw 3 mA to ground.

b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 3.5V (Digital Out=FF_{HEX})

FIGURE 7. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2$=2.500 V_{DC}).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB=analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\ fs\ adj = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX}=The high end of the analog input range

and

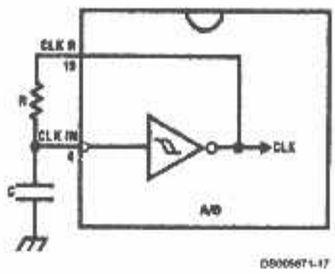
V_{MIN}=the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 8*.

Functional Description (Continued)



$$f_{CLK} \cong \frac{1}{1.1\,RC}$$

$R \cong 10\ k\Omega$

FIGURE 8. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 µF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 9*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120−1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). *Table 1* shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in *Table 1*, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

Functional Description (Continued)

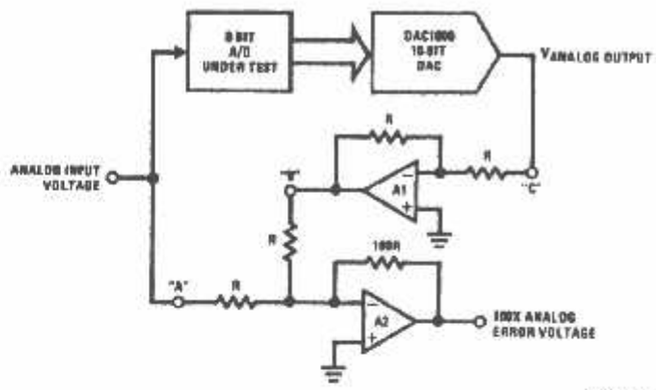


FIGURE 10. A/D Tester with Analog Error Output

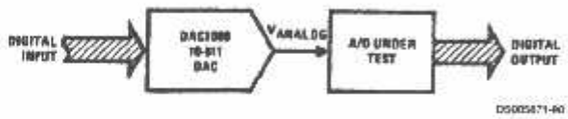


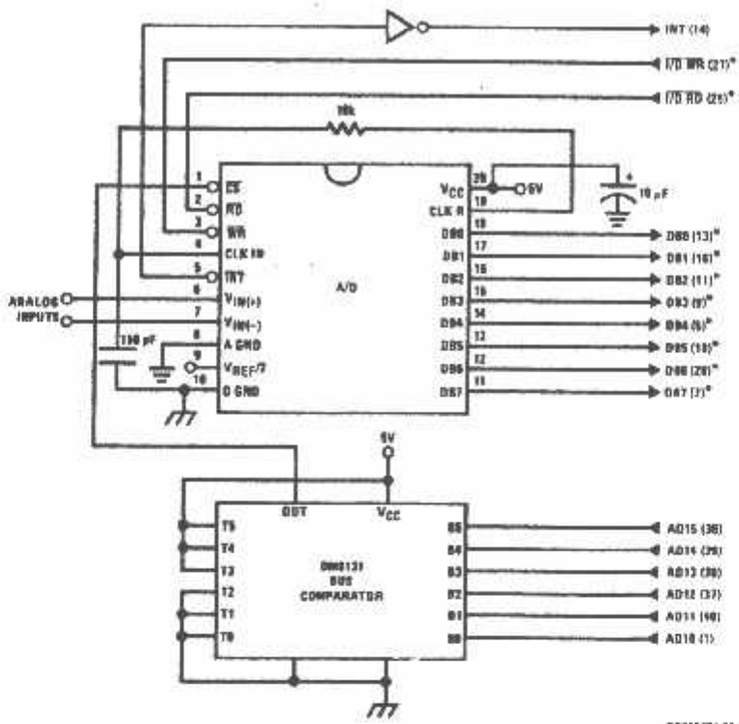
FIGURE 11. Basic "Digital" A/D Tester

TABLE 1. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY				FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2=2.560\ V_{DC}$	
					MS GROUP	LS GROUP	VMS GROUP (Note 15)	VLS GROUP (Note 15)
F	1	1	1	1	15/16	15/256	4.800	0.300
E	1	1	1	0	7/8	7/128	4.480	0.280
D	1	1	0	1	13/16	13/256	4.160	0.260
C	1	1	0	0	3/4	3/64	3.840	0.240
B	1	0	1	1	11/16	11/256	3.520	0.220
A	1	0	1	0	5/8	5/128	3.200	0.200
9	1	0	0	1	9/16	9/256	2.880	0.180
8	1	0	0	0	1/2	1/32	2.560	0.160
7	0	1	1	1	7/16	7/256	2.240	0.140
6	0	1	1	0	3/8	3/128	1.920	0.120
5	0	1	0	1	5/16	2/256	1.600	0.100
4	0	1	0	0	1/4	1/64	1.280	0.080
3	0	0	1	1	3/16	3/256	0.960	0.060
2	0	0	1	0	1/8	1/128	0.640	0.040
1	0	0	0	1	1/16	1/256	0.320	0.020
0	0	0	0	0			0	0

Note 15: Display Output=VMS Group + VLS Group

Functional Description (Continued)



Note 16: *Pin numbers for the DP8228 system controller, others are INS8080A.

Note 17: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 12. ADC0801_INS8080A CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 12* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:      JMP     LD DATA
  •       •           •
  •       •           •
0100    21 00 02    START:      LXI H 0200H     ;HL pair will point to
                                                ;data storage locations
0103    31 00 04    RETURN:     LXI SP 0400H    ;Initialize stack pointer (Note 1)
0106    7D                      MOV A, L        ;Test # of bytes entered
0107    FE 0F                   CPI 0F H        ;If # = 16. JMP to
0109    CA 13 01                JZ CONT         ;user program
010C    D3 E0                   OUT E0 H        ;Start A/D
010E    FB                      EI              ;Enable interrupt
010F    00          LOOP:       NOP             ;Loop until end of
0110    C3 0F 01                JMP LOOP        ;conversion
0113      •         CONT:         •
  •       •           •           •
  •       •           (User program to          •
  •       •           process data)             •
  •       •           •           •
  •       •           •           •
0300    DB E0       LD DATA:    IN E0 H         ;Load data into accumulator
0302    77                      MOV M, A        ;Store data
0303    23                      INX H           ;Increment storage pointer
0304    C3 03 01                JMP RETURN
```

DS005671-99

Note 18: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 19: All address used were arbitrarily chosen.

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 12* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs — one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 13*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

Functional Description (Continued)

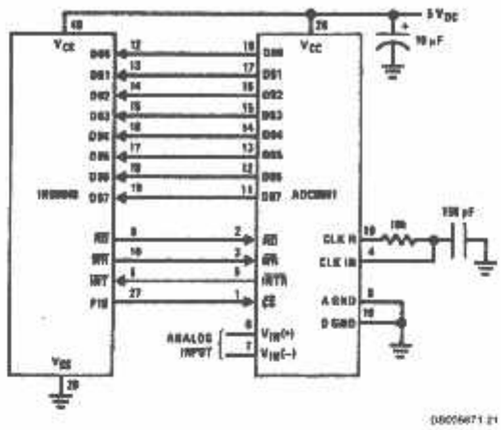


FIGURE 13. INS8048 Interface

SAMPLE PROGRAM FOR *Figure 13* INS8048 INTERFACE

```
04 10                    JMP     10H          ; Program starts at addr 10
                         ORG     3H
04 50                    JMP     50H          ; Interrupt jump vector
                         ORG     10H          ; Main program
99 FE                    ANL     P1, #0FEH    ; Chip select
81                       MOVX    A, @R1       ; Read in the 1st data
                                              ; to reset the intr
89 01          START:    ORL     P1, #1       ; Set port pin high
B8 20                    MOV     R0, #20H     ; Data address
B9 FF                    MOV     R1, #0FFH    ; Dummy address
BA 10                    MOV     R2, #10H     ; Counter for 16 bytes
23 FF          AGAIN:    MOV     A, #0FFH     ; Set ACC for intr loop
99 FE                    ANL     P1, #0FEH    ; Send CS (bit 0 of P1)
91                       MOVX    @R1, A       ; Send WR out
05                       EN      I            ; Enable interrupt
96 21          LOOP:     JNZ     LOOP         ; Wait for interrupt
EA 1B                    DJNZ    R2, AGAIN    ; If 16 bytes are read
00                       NOP                  ; go to user's program
00                       NOP
                         ORG     50H
81             INDATA:   MOVX    A, @R1       ; Input data, CS still low
A0                       MOV     @R0, A       ; Store in memory
18                       INC     R0           ; Increment storage counter
89 01                    ORL     P1, #1       ; Reset CS signal
27                       CLR     A            ; Clear ACC to get out of
93                       RETR                 ; the interrupt loop
```

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 14*.

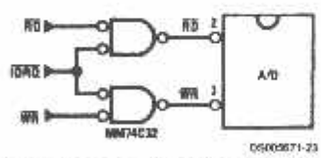


FIGURE 14. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to

Functional Description (Continued)

A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived fom the ϕ2 clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 15* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 16* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

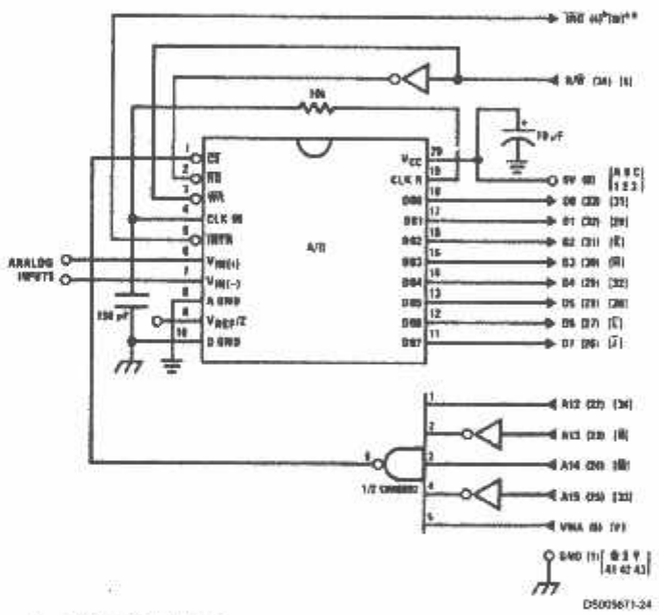
A sample interface program equivalent to the previous one is shown below *Figure 16*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 17*.



Note 20: Numbers in parentheses refer to MC6800 CPU pin out.

Note 21: Number or letters in brackets refer to standard M6800 system common bus code.

FIGURE 15. ADC0801-MC6800 CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 15* ADC0801-MC6800 CPU INTERFACE

```
0010  DF 36     DATAIN  STX   TEMP2   ; Save contents of X
0012  CE 00 2C         LDX   #$002C  ; Upon IRQ low CPU
0015  FF FF F8         STX   $FFF8   ; jumps to 002C
0018  B7 50 00         STAA  $5000   ; Start ADC0801
001B  0E               CLI
001C  3E       CONVRT  WAI           ; Wait for interrupt
001D  DE 34            LDX   TEMP1
001F  8C 02 0F         CPX   #$020F  ; Is final data stored?
0022  27 14            BEQ   ENDP
0024  B7 50 00         STAA  $5000   ; Restarts ADC0801
0027  08               INX
0028  DF 34            STX   TEMP1
002A  20 F0            BRA   CONVRT
002C  DE 34     INTRPT  LDX   TEMP1
002E  B6 50 00         LDAA  $5000   ; Read data
0031  A7 00            STAA  X       ; Store it at X
0033  3B               RTI
0034  02 00     TEMP1   FDB   $0200   ; Starting address for
                                      ; data storage
0036  00 00     TEMP2   FDB   $0000
0038  CE 02 00  ENDP    LDX   #$0200  ; Reinitialize TEMP1
003B  DF 34            STX   TEMP1
003D  DE 36            LDX   TEMP2
003F  39               RTS           ; Return from subroutine
                                      ; To user's program
```

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Note 22: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

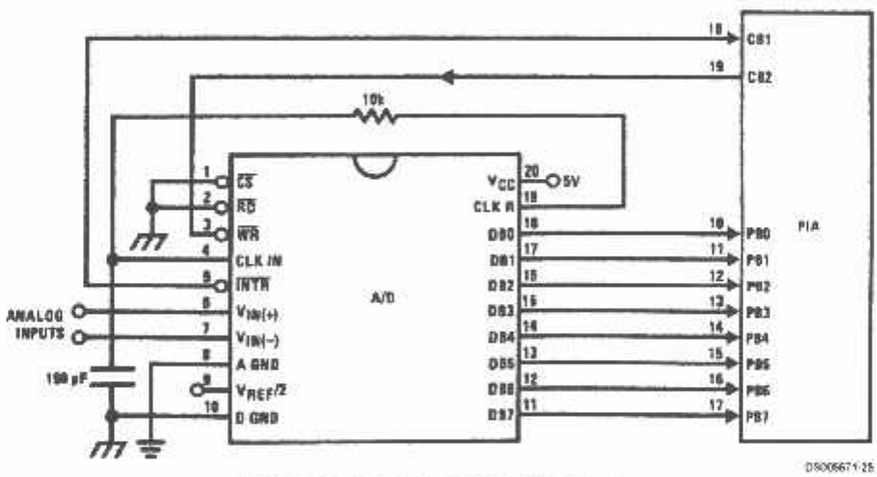

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FIGURE 16. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 16* ADC0801–MC6820 PIA INTERFACE

```
0010  CE 00 38   DATAIN  LDX   #$0038   ; Upon IRQ low CPU
0013  FF FF F8           STX   $FFF8   ; jumps to 0038
0016  B6 80 06           LDAA  PIAORB  ; Clear possible IRQ flags
0019  4F                 CLRA
001A  B7 80 07           STAA  PIACRB
001D  B7 80 06           STAA  PIAORB  ; Set Port B as input
0020  0E                 CLI
0021  C6 34              LDAB  #$34
0023  86 3D              LDAA  #$3D
0025  F7 80 07   CONVRT  STAB  PIACRB  ; Starts ADC0801
0028  B7 80 07           STAA  PIACRB
002B  3E                 WAI           ; Wait for interrupt
002C  DE 40              LDX   TEMP1
002E  8C 02 0F           CPX   #$020F  ; Is final data stored?
0031  27 0F              BEQ   ENDP
0033  08                 INX
0034  DF 40              STX   TEMP1
0036  20 ED              BRA   CONVRT
0038  DE 40   INTRPT     LDX   TEMP1
003A  B6 80 06           LDAA  PIAORB  ; Read data in
003D  A7 00              STAA  X       ; Store it at X
003F  3B                 RTI
0040  02 00   TEMP1     FDB   $0200   ; Starting address for
                                       ; data storage
0042  CE 02 00   ENDP    LDX   #$0200  ; Reinitialize TEMP1
0045  DF 40              STX   TEMP1
0047  39                 RTS           ; Return from subroutine
                PIAORB   EQU   $8006   ; To user's program
                PIACRB   EQU   $8007
```

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The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

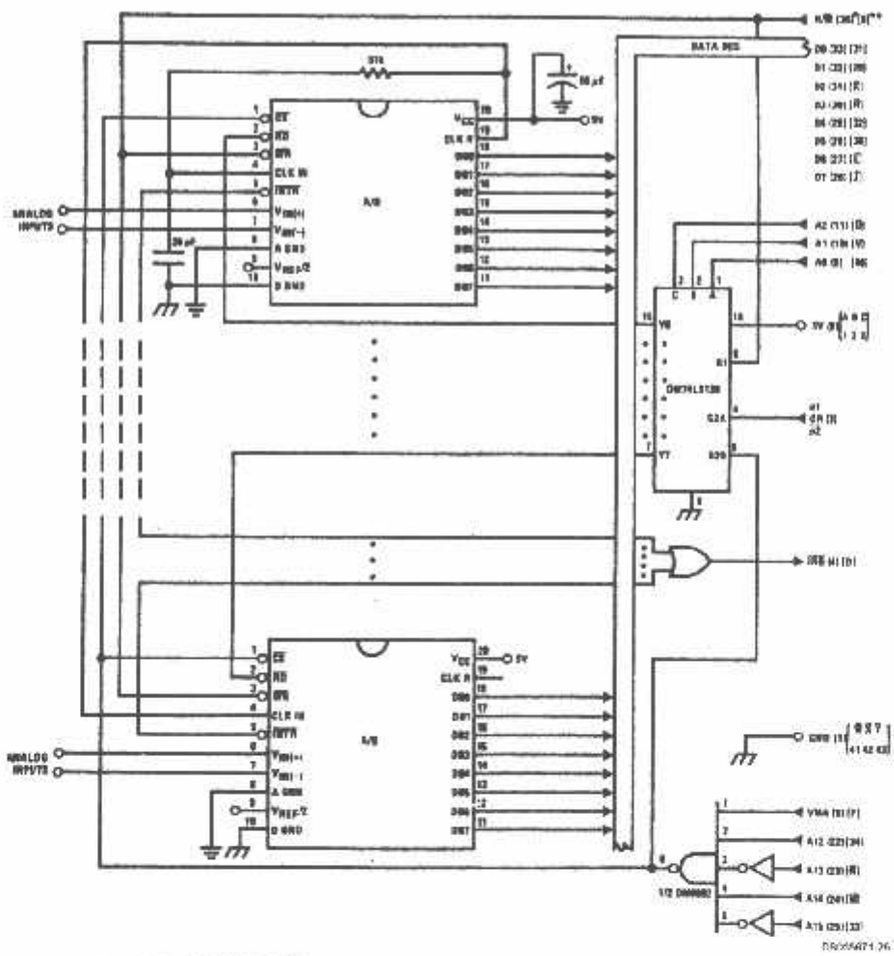
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)



Note 23: Numbers in parentheses refer to MC6800 CPU pin out.

Note 24: Numbers of letters in brackets refer to standard M6800 system common bus code.

FIGURE 17. Interfacing Multiple A/Ds in an MC6800 System

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

Note 25: In order for the microprocessor to service subroutines and interrupts the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 18* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 µV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

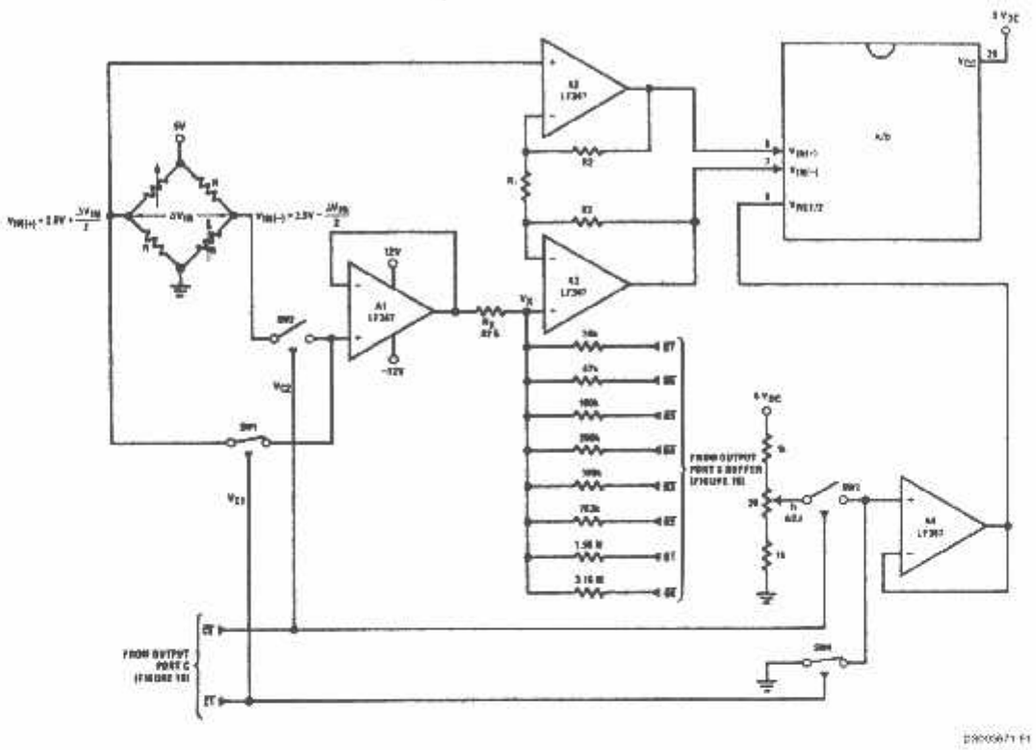
where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 19*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_x increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on

Functional Description (Continued)

any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 µV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



Note 26: R2 = 49.5 R1

Note 27: Switches are LMC13334 CMOS analog switches.

Note 28: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 18. Gain of 100 Differential Transducer Preamp

Functional Description (Continued)

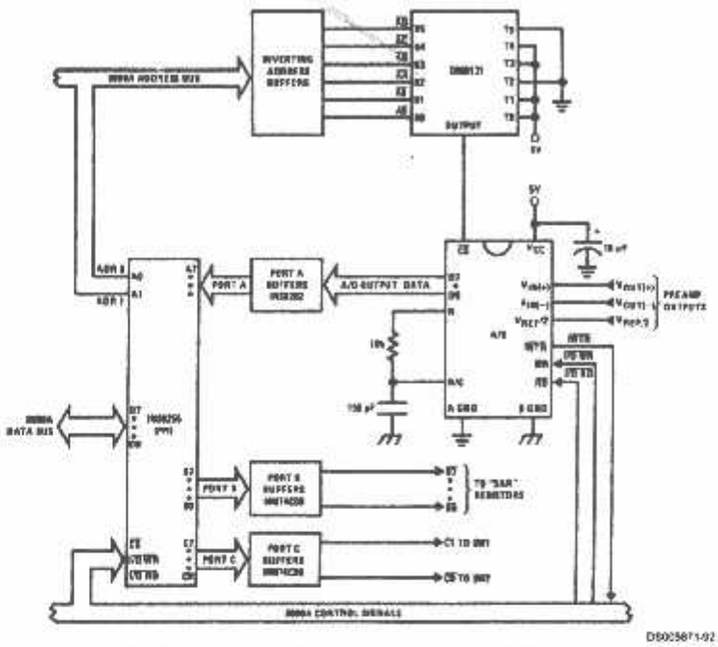


FIGURE 19. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 20*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(-) > V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 21*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 22* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

Functional Description (Continued)

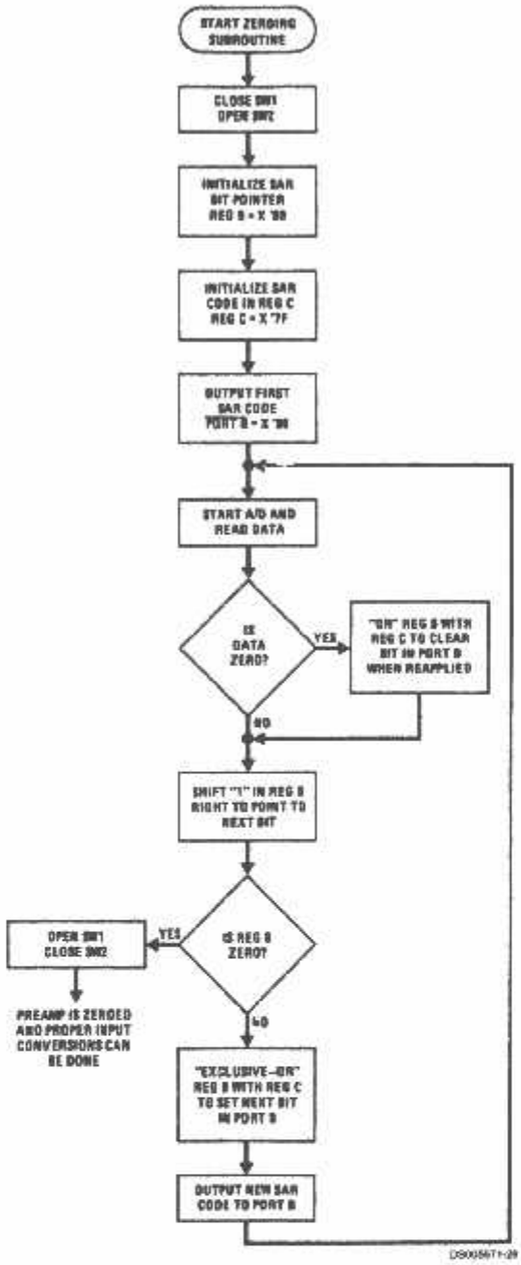


FIGURE 20. Flow Chart for Auto-Zero Routine

Functional Description (Continued)

```
3D00   3E90     MVI 90
3D02   D3E7     Out Control Port                    ;Program PPI
3D04   2601     MVI H 01          Auto-Zero Subroutine
3D06   7C       MOV A,H
3D07   D3E6     OUT C                              ;Close SW1 open SW2
3D09   0680     MVI B 80                           ;Initialize SAR bit pointer
3D0B   3E7F     MVI A 7F                           ;Initialize SAR code
3D0D   4F       MOV C,A           Return
3D0E   D3E5     OUT B                              ;Port B = SAR code
3D10   31AA3D   LXI SP 3DAA       Start            ;Dimension stack pointer
3D13   D3E4     OUT A                              ;Start A/D
3D15   FB       IE
3D16   00       NOP               Loop             ;Loop until INT asserted
3D17   C3163D   JMP Loop
3D1A   7A       MOV A,D           Auto-Zero
3D1B   C600     ADI 00
3D1D   CA2D3D   JZ Set C                           ;Test A/D output data for zero
3D20   78       MOV A,B           Shift B
3D21   F600     ORI 00                             ;Clear carry
3D23   1F       RAR                                ;Shift "1" in B right one place
3D24   FE00     CPI 00                             ;Is B zero? If yes last
3D26   CA373D   JZ Done                            ;approximation has been made
3D29   47       MOV B,A
3D2A   C3333D   JMP New C
3D2D   79       MOV A,C           Set C
3D2E   B0       ORA B                              ;Set bit in C that is in same
3D2F   4F       MOV C,A                            ;position as "1" in B
3D30   C3203D   JMP Shift B
3D33   A9       XRA C             New C            ;Clear bit in C that is in
3D34   C30D3D   JMP Return                         ;same position as "1" in B
3D37   47       MOV B,A           Done             ;then output new SAR code.
3D38   7C       MOV A,H                            ;Open SW1, close SW2 then
3D39   EE03     XRI 03                             ;proceed with program. Preamp
3D3B   D3E6     OUT C                              ;is now zeroed.
3D3D            •                 Normal
                •
                •
                Program for processing
                proper data values
3C3D   DBE4     IN A              Read A/D Subroutine  ;Read A/D data
3C3F   EEFF     XRI FF                             ;Invert data
3C41   57       MOV D,A
3C42   78       MOV A,B                            ;Is B Reg = 0? If not stay
3C43   E6FF     ANI FF                             ;in auto zero subroutine
3C45   C21A3D   JNZ Auto-Zero
3C48   C33D3D   JMP Normal
```

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Note 29: All numerical values are hexadecimal representations.

FIGURE 21. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

- It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.
- The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.
- A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.
- The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.
- The peripherals of concern are mapped into I/O space with the following port assignments:

Functional Description (Continued)

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

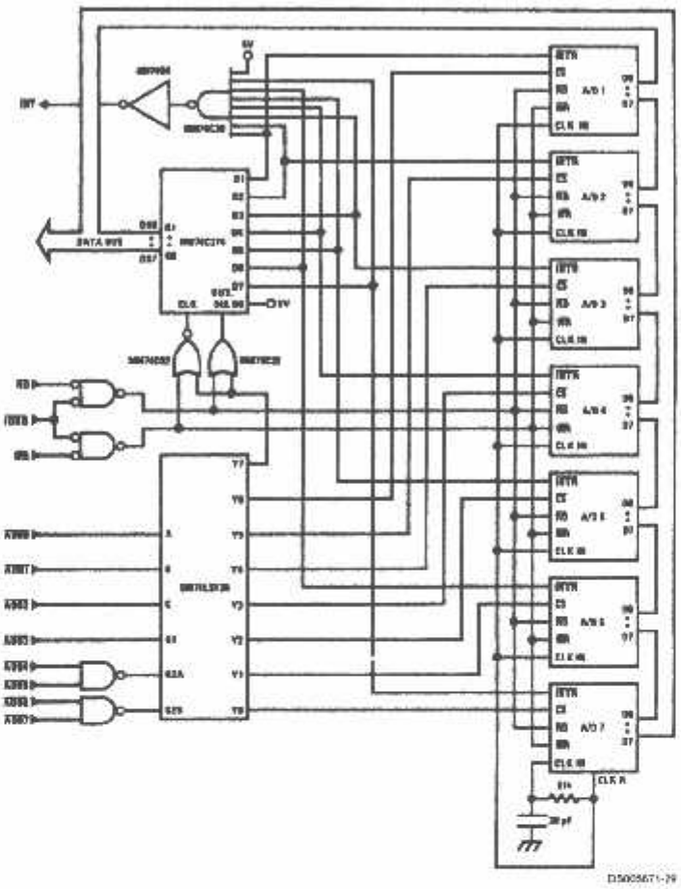


FIGURE 22. Multiple A/Ds with Z-80 Type Microprocessor

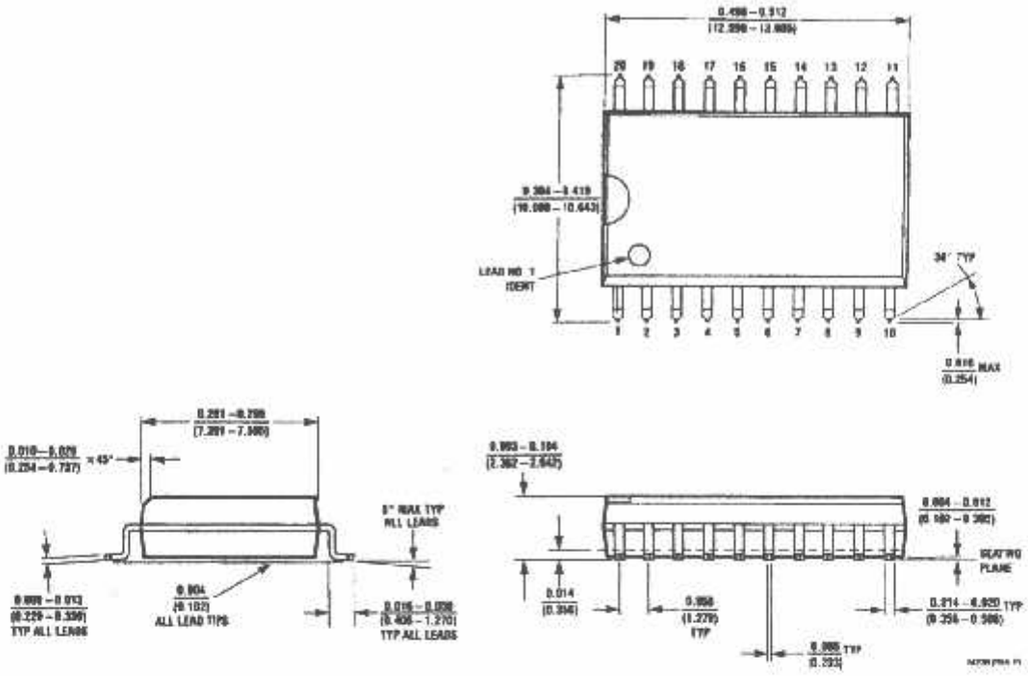
Functional Description (Continued)

INTERRUPT SERVICING SUBROUTINE

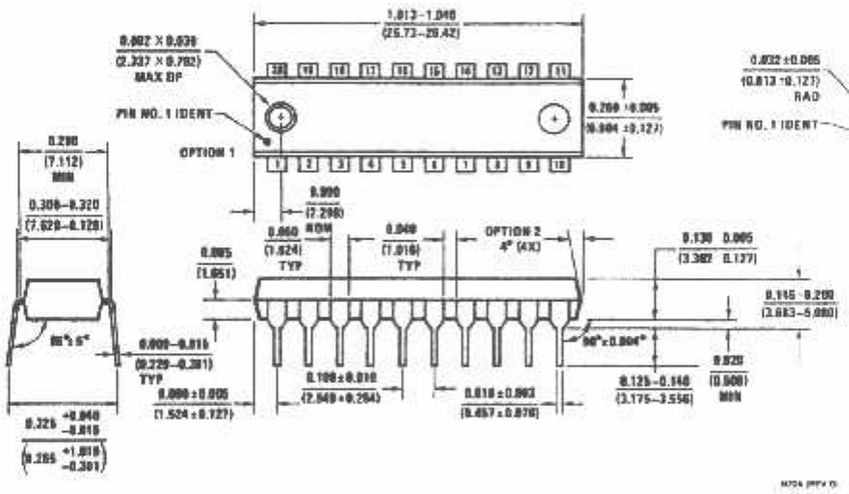
LOC	OBJ CODE		SOURCE STATEMENT	COMMENT
0038	E5		PUSH HL	;Save contents of all registers affected by
0039	C5		PUSH BC	;this subroutine.
003A	F5		PUSH AF	;Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL),X3E00	;Initialize memory pointer where data will be stored.
003E	0E 01		LD C, X01	;C register will be port ADDR of A/D converters.
0040	D300		OUT X00, A	;Load peripheral status word into 8-bit latch.
0042	DB00		IN A, X00	;Load status word into accumulator.
0044	47		LD B,A	;Save the status word.
0045	79	TEST	LD A,C	;Test to see if the status of all A/D's have
0046	FE 08		CP, X08	;been checked. If so, exit subroutine
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	;Test a single bit in status word by looking for
004C	1F		RRA	;a "1" to be rotated into the CARRY (an $\overline{INT}$
004D	47		LD B,A	;is loaded as a "1"). If CARRY is set then load
004E	DA 5500		JPC, LOAD	;contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	;If CARRY is not set, increment C register to point
0052	C3 4500		JP,TEST	;to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	;Read data from interrupting A/D and invert
0057	EE FF		XOR FF	;the data.
0059	77		LD (HL),A	;Store the data
005A	2C		INC L	
005B	71		LD (HL),C	;Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP,NEXT	;Test next bit in status word.
0060	F1	DONE	POP AF	;Re-establish all registers as they were
0061	C1		POP BC	;before the interrupt.
0062	E1		POP HL	
0063	C9		RET	;Return to original program

D5005671-A6

Physical Dimensions inches (millimeters) unless otherwise noted



SO Package (M)
Order Number ADC0802LCWM or ADC0804LCWM
NS Package Number M20B



Molded Dual-In-Line Package (N)
Order Number ADC0801LCN, ADC0802LCN,
ADC0803LCN, ADC0804LCN or ADC0805LCN
NS Package Number N20A

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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- 16 Characters x 2 line
- 5 x 7 Dot Matrix + Cursor
- 1/16 Duty
- 5V single Power Supply
- Available in EL and LED Backlight type

■ Absolute Maximum Ratings

Vss=0V, Ta=25°C

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply	V_{DD}		-0.3	6.0	V
voltage	V_{LC}		-0.3	V_{DD}	V
Input voltage	Vin		-0.3	V_{DD} +0.3	V
Operating temperature					
Normal	Topr		0	+50	°C
Wide	Topr		-20	+70	°C
Storage temperature					
Normal	Tstg		-20	+60	°C
Wide	Tstg		-30	+80	°C
Storage humidity		< 48 hrs	+20	+85	%RH
		<1000 hrs	+20	+65	%RH

■ Mechanical Characteristics

Item		Specifications	Unit
Module size (H x V)		85.0 x 30.0	mm
Thickness	Reflective/EL	10.1	mm
	LED	15.8	mm
Viewing area (H x V)		62.0 x 16.0	mm
Character size with cursor (H x V)		2.78 x 4.89	mm
Mounting hole distance (H x V)		82.0 x 24.0	mm
Weight	Reflective	25	g
	EL backlight	30	g
	LED backlight	40	g

H : Horizontal, V : Vertical

■ Electrical Characteristics

V_{DD}=5V± 5%, V_{SS}=0V, Ta=0 ~ 50°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}		4.75	5.00	5.25	V
	V_{DD} - V_{LC}		3.0	-	6.3	V
Input voltage High	V_{IH1}		2.2	-	V_{DD}	V
Low	V_{IL1}		0	-	0.6	V
Output voltage High	V_{OH1}	-I_{OH}=0.205mA	2.4	-	-	V
Low	V_{LH1}	-I_{OL}=1.2mA	-	-	0.4	V
Current consumption *						
Normal Temp type	I_{DD}	Ta=25°C	-	1.6	2.5	mA
	I_{LC}	V_{LC}=0.25V	-	0.2	1.0	mA
Wide Temp. type	I_{DD}	Ta=25°C	-	1.6	2.5	mA
	I_{LC}	V_{LC}=-0.6V	-	0.3	1.0	mA

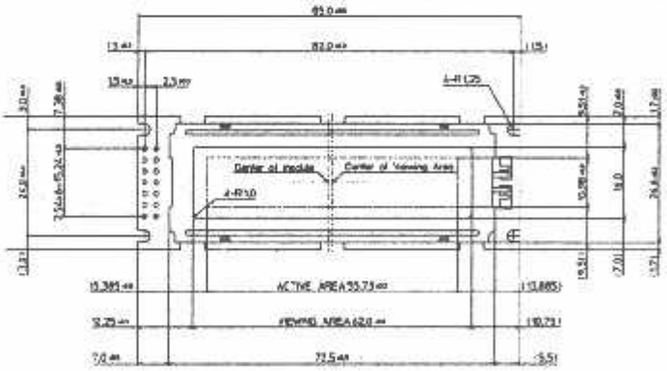
* test pattern : check board pattern

■ Pin Function

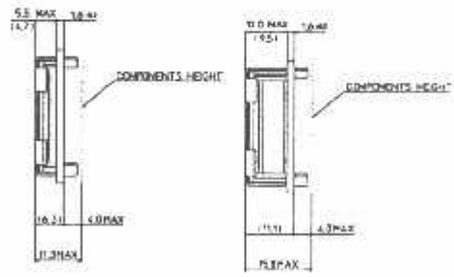
No.	Name	Function
1	VSS	GND
2	VDD	Power supply voltage +5V
3	VLC	Liquid crystal driving voltage
4	RS	L : Instruction code input H: Data input
5	R/W	L : Data write from MPU to LCM H : Data read from LCM to MPU
6	E	Enable
7	DB0	Data bus line
8	DB1	Data bus line
9	DB2	Data bus line
10	DB3	Data bus line
11	DB4	Data bus line
12	DB5	Data bus line
13	DB6	Data bus line
14	DB7	Data bus line
(15)	A	Anode (+) for LED backlight
(16)	K	Cathode (-) for LED backlight

■ Dimensions

M1632 (2x16) Unit: mm, General tolerance ±0.5 mm

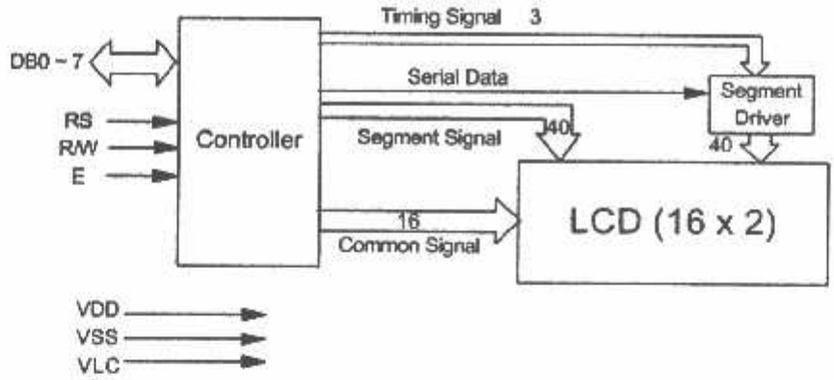


Reflective/EL Backlight LED Backlight



Note : Only dimension changes between Reflective/EL and LED backlight is the thickness.

■ Circuit Block diagram



■ Recommended Operating Voltage

The recommended value (Vopr) for an ambient temperature is as follows. Vopr=VDD - VLC

Temperature (°C)		-20	0	+25	+50	+70
Vopr (V)	Normal	-	5.00	4.75	4.50	-
	Wide	6.20	5.90	5.60	5.40	5.20

■ Optical Characteristics

1. Normal Temperature Range Type

Ta=21°C, 1/16 Duty, Vopr=4.75V

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Viewing angle	θ 1	C≥2	-	-	-15	deg.
	θ 2	Φ = 0°	55	-	-	
	θ 2- θ 1		70	-	-	
Contrast	C	θ =+25°, Φ = 0°	-	5	-	-
Response time	ton (rise)	θ =0°	-	150	200	msec
	toff (fall)	Φ =0°	-	200	220	msec
	ton (rise)	θ =0°, Φ = 0°	-	750	800	msec
	toff (fall)	Ta = 0°C, Vopr=5.0V	-	600	700	msec

Measuring equipment : Canon illuminater LC-4SR

2.Wide Temperature Range Type

Ta=21°C, 1/16 Duty, Vopr=VDD - VLC

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Viewing angle	θ 1	C≥2	-	-	-15	deg.
	θ 2	Φ = 0°	55	-	-	
	θ 2- θ 1	Vop=5,6v	70	-	-	
Contrast	C	θ =+20°, Φ = 0° Vop=5,6v	-	5	-	-
Response time	ton (rise)	θ =0°, Φ = 0°	-	150	200	msec
	toff (fall)	Ta = 21°C, Vopr=5.6V	-	200	220	msec
	ton (rise)	θ =0°, Φ = 0°	-	750	800	msec
	toff (fall)	Ta = 0°C, Vopr=5.9V	-	600	700	msec

Measuring equipment : Canon illuminater LC-4SR

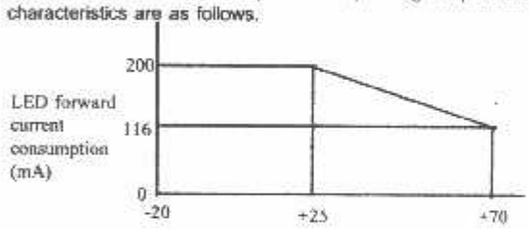
■ LED Backlight

1. Absolute Maximum Ratings

Ta=25°C

Item	Symbol	Specifications	Unit
LED forward current consumption *	IF	200	mA
LED reverse voltage	VR	8	V
Allowable loss	PD	0.92	W
Operating Temperature	Topr	- 20 ~ +70	°C
Storage Temperature	Tstg	- 40 ~ + 80	°C

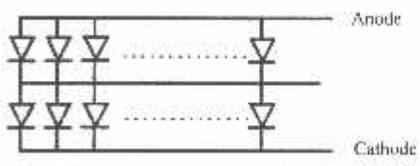
* LED forward current consumption and operating temperature characteristics are as follows.



2. Electrical Characteristics

Ta=25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
LED forward input voltage	VF	IF=112mA	3.8	4.1	4.4	V
LED reverse current	IR	VR=8V	-	-	0.16	mA
Brightness	L	IF=112mA*	40	50	-	cd/m²



total number of LED chips =2 x 8 = 16 pcs

■ EL Backlight

1.Absolute Maximum Ratings

Item	Symbol	Standard	Unit
Operating voltage	Vopr	AC 150V, 1KHz Sinew ave	V
Operating temperature	Topr	-10 ~ +50	°C
Storage temperature	Tstg	-20 ~ + 60	°C
Storage humidity		0 ~ 10 % RH (60 °C) 0 ~ 30 % RH (40 °C)	

2. Brightness, Current, Life Characteristics

Item	Conditions	Specifications	Unit
Brightness	100V, 400Hz Sinew ave	30 min. 35 typ.	cd/m²
Current	100V, 400Hz Sinew ave	1.2 typ. 1.7 max	mA
Life *	100V, 400Hz, Sinew ave 25°C,50%RH	1,500	hrs
	Using 5S Inverter 25°C,50%RH	4,000	

* Definition of Life : Used continuously dow n to 10 cd/m²

3. Suitable Inverter 5S

3.1 Electrical Characteristics (When combined with EL lamp)

Ta=25°C

Item	Symbol	Conditions	Specifications	Unit
Oscillating frequency	f_{INV}	V_{IN}=5VDC	550 typ.	Hz
Output voltage	V_{OUT}	V_{IN}=5VDC	100 typ.	V
Output current	I_{OUT}	V_{IN}=5VDC	1.5 typ.	mA
Input current	V_{IN}		5 typ	VDC
Voltage	I_{IN}	V_{IN}=5VDC	10 typ	mA
Initial brightness	B	V_{IN}=5VDC	35 typ.	cd/m²
Surface brightness (panel upper side)	Bp	V_{IN}=5VDC Vopr=0V	7 typ.	cd/m²

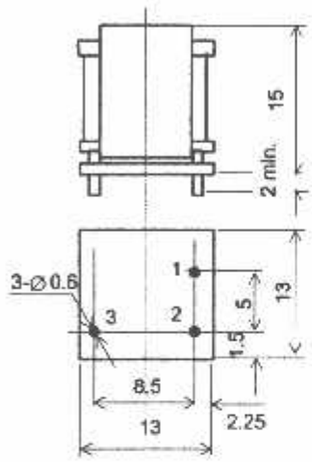
3.2 Tolerance (Inverter only)

Item	Specifications	Unit
Input voltage	3.0 to 6.0	V
Load range	5 to 15	cm²

3.3 Maximum Ratings (Inverter only)

Item	Specifications	Unit
Input voltage	7.0	V
Load range	50	cm²
Operating temperature	-10 to +60	°C
Storage temperature	-20 to +70	°C

3.4 Inverter Dimensions (unit : mm)



Pin No.	Function
1	Input : 5V DC
2	Common : GND
3	Output

tyco Electronics Authorized Distributor — NEW! I/O Modules

...= Industry standard package and pin-out • Color coded by function • 4,000Vrms optical isolation • High immunity to false operation • Output modules can be controlled using sinking or sourcing logic

Dim. in mm

Input Voltage	Input I (mA)	Output Current	Output Voltage	Package Color	Turn On Time	Turn Off Time	Digi-Key Part No.	Price Each 1	Price Each 25	Price Each 50	Potter & Brumfield Part No.
~ 140VAC/DC	8	50mA	30VDC	Yellow	20	30	PB537-ND	11.76	10.32	9.33	IAC-5
3.3 ~ 32VDC	1 ~ 20	50mA	30VDC	White	1	1	PB538-ND	11.76	10.32	9.33	IDC-5
3 ~ 8VDC	5 ~ 20	3A	24 ~ 280VAC	Black	8.3	8.3	PB539-ND	11.76	10.32	9.33	OAC-5
3 ~ 8VDC	1 ~ 20	3A	3 ~ 60VDC	Red	1	75	PB540-ND	11.76	10.32	9.33	ODC-5
18 ~ 32VDC	1 ~ 13	3A	3 ~ 60VDC	Red	1	75	PB540-ND	12.43	10.88	9.85	ODC-24

NEW! Solid State Relays

...ter & Brumfield Models SSR and SRS "Hockey Puck" style solid state relays for general ...ver switching applications. These feature a dual, back to back SCR, Zero-Cross switching ...tput for most inductive and high inrush loads. Parts ending in "R" are random turn-on outputs ...ehase control applications. SSRD (Dual) and SSRQ (Quad) are multiple output relays ...ere each output is controlled separately. SSRT are SPST "Hockey Puck" style relays with ...ptoriless Triac Outputs for inductive switching and high inrush applications. Enhanced ...se immunity (designed to meet level 3 requirements of European EMC Directive). Includes ...D indicator and floating terminal design.

Fig. 1 — SSR/SSRI Style

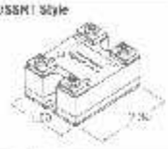


Fig. 2 — Dual or Quad Style

Dim. in mm

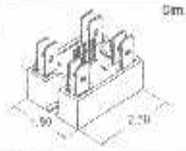


Fig.	Input Voltage	Operate Voltage	Release Voltage	Output Voltage	Output Current (Arms)	Digi-Key Part No.	Price Each 1	Price Each 25	Price Each 50	Potter & Brumfield Part No.
				SSR Series — SCR Output						
1	3 ~ 32VDC	3VDC	1VDC	24 ~ 240VAC	1 ~ 25	PB545-ND	38.88	36.62	27.71	SSR-240D25
	3 ~ 32VDC	3VDC	1VDC	24 ~ 240VAC	.1 ~ 25	PB546-ND	38.21	33.44	30.25	SSR-240D25R
	3 ~ 32VDC	3VDC	1VDC	24 ~ 240VAC	.1 ~ 50	PB547-ND	51.00	44.63	40.38	SSR-240D50
	3 ~ 32VDC	3VDC	1VDC	24 ~ 240VAC	.1 ~ 125	PB548-ND	92.88	81.27	73.53	SSR-240D125
	90 ~ 280VAC	90VAC	10VAC	24 ~ 240VAC	1 ~ 25	PB542-ND	41.42	36.25	32.80	SSR-240A25
	90 ~ 280VAC	90VAC	10VAC	24 ~ 240VAC	.1 ~ 50	PB543-ND	57.41	50.24	45.45	SSR-240A50
				SSRT Series — Triac Output						
1	3 ~ 32VDC	3VDC	1VDC	24 ~ 240VAC	05 ~ 10	PB553-ND	27.14	23.78	21.49	SSRT-240D10
	3 ~ 32VDC	3VDC	1VDC	24 ~ 240VAC	05 ~ 25	PB554-ND	31.87	27.88	25.24	SSRT-240D25
	90 ~ 280VAC	90VAC	10VAC	24 ~ 240VAC	05 ~ 25	PB552-ND	38.21	33.44	30.25	SSRT-240A25
				SSRD Series — Dual Output						
2	3 ~ 32VDC	3VDC	1VDC	24 ~ 240VAC	05 ~ 25	PB548-ND	63.72	55.76	50.45	SSRD-240D25
	4 ~ 15VDC	4VDC	1VDC	24 ~ 240VAC	05 ~ 25	PB549-ND	68.50	59.84	54.23	SSRD-240D25R
	3 ~ 32VDC	3VDC	1VDC	24 ~ 240VAC	05 ~ 40	PB550-ND	79.98	69.70	63.07	SSRD-240D40
				SSRQ Series — Quad AC Output						
2	4 ~ 15VDC	4VDC	1VDC	24 ~ 280VAC	05 ~ 20	PB551-ND	102.00	89.25	80.75	SSRQ-240D20

NEW! Timers/Time Delay

Potter & Brumfield Timer relays are versatile multifunction adjustable relays for industrial and time delay type applications. By setting the timing mode, selecting the time duration and applying 120VAC to power the timing circuitry, a dry contact relay will trip On or Off at the end of the set time. Delay-On or Delay-Off modes will start upon power up and delay turning the relay output On or Off for the user selected time. Using the Cycle or Repeat Mode will cut the timer in a continuous On and Off cycle where the time On and time Off are equal lengths. Model CRB relays enable separate On and Off adjustable times for Cycle timing.

Fig. 1 — CNMG Series

Fig. 2 — CNS Series

Fig. 3 — CNT Series

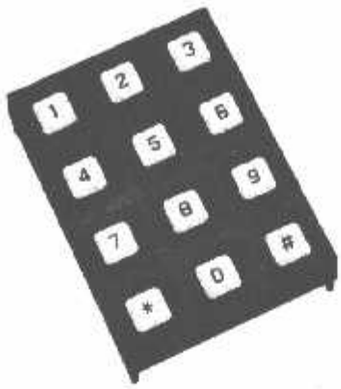
Fig. 4 — CLB and CLF Series

Fig. 5 — CB, CHB, CHD, CDB Series

Fig. 6 — CRB Series

Fig.	Description	Digi-Key Part No.	Price Each 1	Price Each 25	Price Each 50	Potter & Brumfield Part No.
1	Thumbwheel Selectable, Time Delay Relay, 1 Sec. ~ 9.98K Hours, DPDT, 10A, 120VAC, 11 Octal	PB535-ND	86.71	72.68	65.65	CNMG
2	Dial Adjustable, Time Delay Relay, 4 Function, DPDT, 10A, 120VAC, 8 Octal	PB556-ND	68.47	56.92	54.21	CNS-35-72
	Dial Adjustable, Time Delay Relay, 6 Function, DPDT, 10A, 120VAC, 11 Octal	PB557-ND	80.54	70.48	63.77	CNS-35-76
	Dial Adjustable, Time Delay Relay, 4 Function, DPDT, 10A, 24 ~ 240VAC/VDC, 8 Octal	PB675-ND	97.22	85.08	76.97	CNS-35-92
	Dial Adjustable, Time Delay Relay, 6 Function, DPDT, 10A, 24 ~ 240VAC/VDC, 11 Octal	PB558-ND	90.98	79.67	72.09	CNS-35-96
3	Thumbwheel Selectable, Digital Time Delay Relay, DPDT, 10A, 12VDC, 11 Octal	PB559-ND	131.26	114.85	103.92	CNT-35-26
	Thumbwheel Selectable, Digital Time Delay Relay, DPDT, 10A, 120VAC, 11 Octal	PB560-ND	118.13	103.37	93.52	CNT-35-76
	Thumbwheel Selectable, Digital Time Delay Relay, DPDT, 10A, 24 ~ 240VAC/VDC, 11 Octal	PB561-ND	137.04	119.91	108.49	CNT-35-96
4	Knob Adjustable, Delay-On Relay, .1 ~ 10 Sec., 10A, 120VAC for Socket use 27E883	PB562-ND	100.85	88.25	79.84	CLH-51-70010
	Resistor Adjustable, Delay-On Relay, .1 ~ 10 Sec., 10A, 120VAC for Socket use 27E883	PB563-ND	99.65	87.20	78.89	CLF-41-70010
5	Knob Adjustable, Delay-On Relay, .1 ~ 1 Sec., 120VAC, 8 Octal	PB564-ND	92.30	80.77	73.08	CB-1001B-70
	Knob Adjustable, Delay-On Relay, .1 ~ 5 Sec., 120VAC, 8 Octal	PB571-ND	92.30	80.77	73.08	CB-1002B-70
	Knob Adjustable, Delay-On Relay, .1 ~ 10 Sec., 120VAC, 8 Octal	PB565-ND	92.30	80.77	73.08	CB-1003B-70
	Knob Adjustable, Delay-On Relay, 6 ~ 60 Sec., 120VAC, 8 Octal	PB566-ND	92.30	80.77	73.08	CB-1004B-70
	Knob Adjustable, Delay-On Relay, 0.6 ~ 180 Sec., 120VAC, 8 Octal	PB567-ND	92.30	80.77	73.08	CB-1005B-70
	Knob Adjustable, Delay-On Relay, 1 ~ 10 Min., 120VAC, 8 Octal	PB568-ND	92.30	80.77	73.08	CB-1006B-70
	Knob Adjustable, Delay-On Relay, 10 ~ 100 Min., 120VAC, 8 Octal	PB569-ND	92.30	80.77	73.08	CB-1007B-70
	Knob Adjustable, Delay-On Relay, .1 ~ 10 Sec., 24VDC, 8 Octal	PB570-ND	92.30	80.77	73.08	CB-1025D-30
	Knob Adjustable, Delay-On Relay, .1 ~ 10 Sec., 12VDC, 8 Octal	PB571-ND	92.30	80.77	73.08	CB-1041D-20
6	Knob Adjustable, Delay-On Relay, 1 ~ 10 Sec., DPDT, 10A, 24VAC, 8 Octal	PB572-ND	114.48	100.17	90.63	CHB-38-30001
	Knob Adjustable, Delay-On Relay, 1 ~ 180 Sec., DPDT, 10A, 24VAC, 8 Octal	PB573-ND	114.48	100.17	90.63	CHB-38-30003
	Knob Adjustable, Delay-On Relay, 1 ~ 10 Sec., DPDT, 10A, 120VAC, 8 Octal	PB574-ND	114.48	100.17	90.63	CHB-38-70001
	Knob Adjustable, Delay-On Relay, 1 ~ 60 Sec., DPDT, 10A, 120VAC, 8 Octal	PB575-ND	114.48	100.17	90.63	CHB-38-70002
	Knob Adjustable, Delay-On Relay, 1 ~ 180 Sec., DPDT, 10A, 120VAC, 8 Octal	PB576-ND	114.48	100.17	90.63	CHB-38-70003
	Knob Adjustable, Delay-On Relay, 1 ~ 60 Sec., DPDT, 10A, 24VDC, 8 Octal	PB577-ND	114.48	100.17	90.63	CHD-38-30002
	Knob Adjustable, Delay-On Operate Relay, 1 ~ 10 Sec., 10A, 120VAC, 8 Octal	PB578-ND	203.36	177.96	161.01	CDB-38-70009
	Knob Adjustable, Delay-On Release Relay, .1 ~ 10 Sec., 10A, 120VAC, 11 Octal	PB579-ND	203.36	177.96	161.01	CDB-38-70014
6	Recycle Time Delay Relay, 0.1 ~ 10 Sec., On-Off Time Adjustments, DPDT, 10A, 120VAC, 8 Octal	PB580-ND	224.23	196.21	177.52	CRB-48-70010
	Recycle Time Delay Relay, 0.3 ~ 30 Sec., On-Off Time Adjustments, DPDT, 10A, 120VAC, 8 Octal	PB581-ND	224.23	196.21	177.52	CRB-48-70030
	Recycle Time Delay Relay, 0.6 ~ 60 Sec., On-Off Time Adjustments, DPDT, 10A, 120VAC, 8 Octal	PB582-ND	224.23	196.21	177.52	CRB-48-70060
	Recycle Time Delay Relay, 1.8 ~ 180 Sec., On-Off Time Adjustments, DPDT, 10A, 120VAC, 8 Octal	PB583-ND	224.23	196.21	177.52	CRB-48-70180
–	Adjustable Voltage Sensor Relay, 80 ~ 140VAC, 90-138 Unom, 10A, 8 Octal	PB584-ND	155.11	135.72	122.80	CSA-38-70010

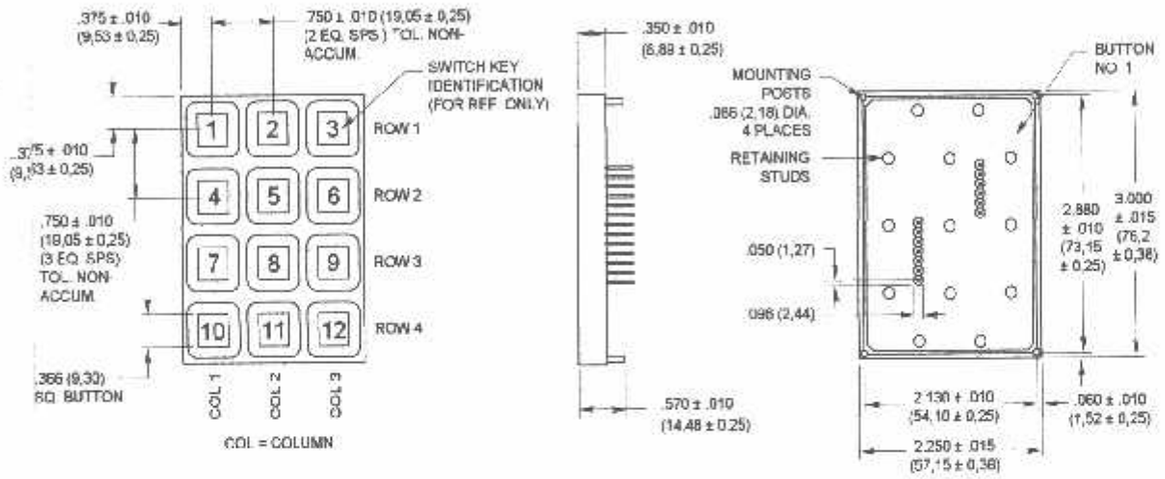
SERIES 84
Unsealed, .750" Centers



FEATURES
- 3/4" Button Centers
- Post Mounted
- Mounts by Tinerman Nut or Heat Upset Post
- Snap-Dome Contact Provides Positive Feedback

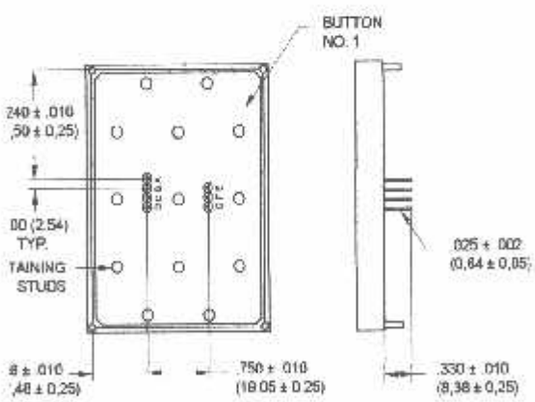
DIMENSIONS In inches (and millimeters)

3x4 Keyboard

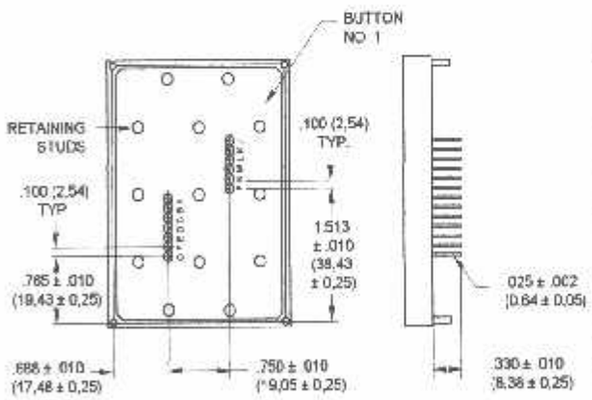


ermination In inches (and millimeters)

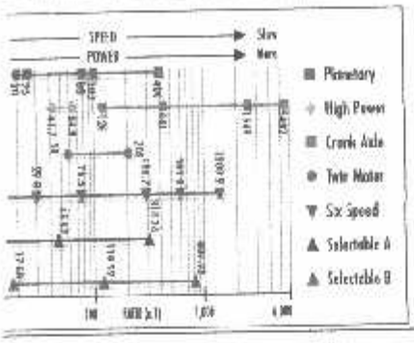
Matrix Output



Single Pole/Common Bus

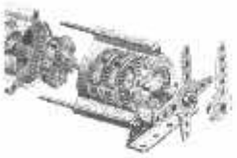


ar Boxes



Scavenge no longer! From low speed to high, we have gear kits for every need. Each features solid molded parts, metal shafts, plus lever arms and plenty of supporting hardware pieces. Drive any of these gear boxes via computer with our Mini Dual H-Bridge Driver Kit and Serial Motor Interface kit (page 41).

Power their small DC motors with from 3 to 4.5 Volts. Actual speed and torque depends on the voltage applied. Reverse the power to change direction. Use them for drive systems, sensor positers, manipulators, grippers and other miniature actuators.



New Low Price!

Planetary Gear Box Kit

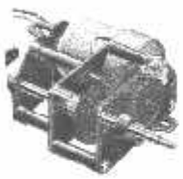
Assemble it for one of eight ratios: 4, 5, 16, 20, 25, 80, 100, or 400 to 1. Our most versatile gear box covering the broadest range. 35 mm wide, up to 80 mm long.

#3-225 $27.95

Speed and Torque outputs (approximate), at 3 Volts

Gear Ratio:	4:1	5:1	16:1	20:1	25:1	80:1	100:1	400:1
Speed RPM:	2625	2100	656	525	420	131	105	26.25
Torque g-cm:	60	75	240	300	375	1200	1500	6000

The included RC-260 motor runs at 3.0 Volts (4.5 V max)
Stall torque: 15 gcm
No-load speed: 10,500 rpm
Current: 1.0A
Maximum ratio: 160,000:1 (by combining two of these kits)



High Power Gear Box Kit

A strong, high torque gear kit. Build for one of two ratios: 41.7 or 64.8 to 1. Easily connected to wheels, cams, grippers, etc. Ideal for drive systems needing speed and strength. Size: 60 x 28 x 41 mm. 80 mm long shaft.

#3-219 $19.95

Speed and Torque outputs (approximate), at 3 Volts

Gear Ratio:	41.7:1	64.8:1
Speed RPM:	250	160
Torque g-cm:	670	1340

The included RS-260 motor runs at 3.0 Volts (4.5 V max)
Stall torque: 15 gcm
No-load speed: 10,500 rpm
Current: 1.0A
Maximum ratio: 65:1

Crank Axle Gear Box Kit

A wide ranging gear box. Build 1 of 4 ratios: 126, 441, 1543 or 5402:1. Size: 72 x 24 x 34 mm. 100 mm long shaft and slip clutch gear to protect motor from over strain.

#3-727 $15.95

Speed and Torque outputs (approximate), at 3 Volts

Gear Ratio:	126:1	441:1	1543:1	5402:1
Speed RPM:	105	30	8.5	2.5
Torque g-cm:	585	1483	499*	2020*

*limit of slip clutch
The included FA-130 motor runs at 3.0 Volts (4.5 V max)
Stall torque: 4.6 gcm
No-load speed: 13,230 rpm
Current: 0.5 A
Maximum ratio: 1543:1

Twin Motor Gearbox Kit

Two DC motors & gears in a compact unit. Same as in the Bulldozer (page 23). Provides full fwd-rev-left-right action! Build with 2 of two different ratios: fast 58:1 or strong 203:1. Size: 75 x 50 x 23 mm. Shafts: 3 mm hex, 105 mm long. Add your own wheel, hubs or tracks.

#3-709 $19.95

Speed and Torque outputs (approximate), at 3 Volts

Gear Ratio:	58:1	203:1
Speed RPM:	230	65
Torque g-cm:	269	941

The included FA-130 motors run at 3.0 Volts (4.5 V max)
Stall torque: 4.4 gcm
No-load speed: 11,230 rpm
Current: 0.5 A (each)
Maximum ratio: 203:1

Six Speed Gear Box Kit

A combination gear box with a wide range. Build 1 of 6 ratios: 11.6, 23.8, 76.5, 196.7, 505.9 or 1300.9 to 1. At 3 Volts, speed varies from 870 RPM (11.6:1) to 7.8 RPM (1300.9:1). Includes slip clutch gear. Size: 45 x 27 x 58 mm. 80 mm long shaft. **#3-260 $19.95**

Speed and Torque outputs (approximate), at 3 Volts

Gear Ratio:	11.6:1	23.8:1	76.5:1	196.7:1	505.9:1	1300.9:1
Speed RPM:	870	338	132	51.3	19.9	7.8
Torque g-cm:	161	415	1038	2600	2336*	2336*

*limited by slip clutch
The included RE-260 motor runs at 3.0 Volts (4.5 V max)
Stall torque: 15 gcm
No-load speed: 10,500 rpm
Current: 1.0A
Maximum ratio: 1300.9:1

Selectable Gear Box Kit

A switchable gear box. Assemble it with one of two different gear ratio groups: 6.8, 45.97 and 310.74 to 1, or 17.68, 119.52 and 807.93 to 1 then quickly switch between the three settings to choose speed, power, or some of each. Ideal for multi-speed machines. **#3-196 $19.95**

Speed and Torque outputs (approximate), at 3 Volts

Gear Ratio:	6.8:1	45.97:1	310.74:1	17.68:1	119.5:1	807.9:1
Speed RPM:	1028	152	22.5	395.5	58.8	8.7
Torque g-cm	40.6	275.8	1864	106	717	4843

The included motor runs at 3.0 Volts
Stall torque: 6 gcm
No-load speed: 6992 RPM
Current: 3.7A
Maximum ratio: 807.9:1

Order this document by LM339/D

MOTOROLA

Quad Single Supply Comparators

LM339, LM339A, LM239, LM239A, LM2901, M2901V, MC3302

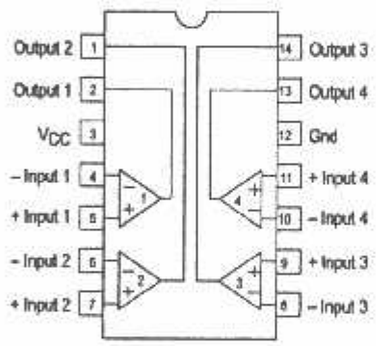
These comparators are designed for use in level detection, low–level sensing and memory applications in consumer automotive and industrial electronic applications.

- Single or Split Supply Operation
- Low Input Bias Current: 25 nA (Typ)
- Low Input Offset Current: ±5.0 nA (Typ)
- Low Input Offset Voltage: ±1.0 mV (Typ) LM139A Series
- Input Common Mode Voltage Range to Gnd
- Low Output Saturation Voltage: 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible
- ESD Clamps on the Inputs Increase Reliability without Affecting Device Operation

N, P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



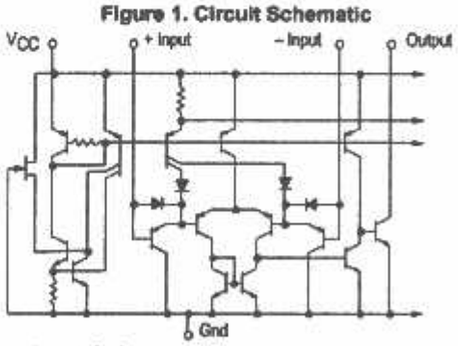
(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage LM239, A/LM339A/LM2901, V MC3302	V_{CC}	 +36 or ±18 +30 or ±15	Vdc
Input Differential Voltage Range LM239, A/LM339A/LM2901, V MC3302	V_{IDR}	 36 30	Vdc
Input Common Mode Voltage Range	V_{ICMR}	–0.3 to V_{CC}	Vdc
Output Short Circuit to Ground (Note 1)	I_{SC}	Continuous	
Power Dissipation @ T_A = 25°C Plastic Package Derate above 25°C	P_D	 1.0 8.0	 W mW/°C
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range LM239, A MC3302 LM2901 LM2901V LM339, A	T_A	 –25 to +85 –40 to +85 –40 to +105 –40 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: 1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}. Output short circuits to V_{CC} can cause excessive heating and eventual destruction.

Figure 1. Circuit Schematic



NOTE: Diagram shown is for 1 comparator.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM239D,AD LM239N,AN	T_A = 25° to +85°C	SO–14 Plastic DIP
LM339D, AD LM339N, AN	T_A = 0° to +70°C	SO–14 Plastic DIP
LM2901D LM2901N	T_A = –40° to +105°C	SO–14 Plastic DIP
LM2901VD LM2901VN	T_A = –40° to +125°C	SO–14 Plastic DIP
MC3302P	T_A = –40° to +85°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = +25°C, unless otherwise noted)

Characteristic	Symbol	LM239A/339A			LM239/339			LM2901/2901V			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	–	±1.0	±2.0	–	±2.0	±5.0	–	±2.0	±7.0	–	±3.0	±20	mVdc
Input Bias Current (Notes 4, 5) (Output in Analog Range)	I_{IB}	–	25	250	–	25	250	–	25	250	–	25	500	nA
Input Offset Current (Note 4)	I_{IO}	–	±5.0	±50	–	±5.0	±50	–	±5.0	±50	–	±3.0	±100	nA
Input Common Mode Voltage Range	V_{ICMR}	0	–	V_{CC} −1.5	0	–	V_{CC} −1.5	0	–	V_{CC} −1.5	0	–	V_{CC} −1.5	V
Supply Current R_L = ∞ (For All Comparators) R_L = ∞, V_{CC} = 30 Vdc	I_{CC}	 – –	 0.8 1.0	 2.0 2.5	 – –	 0.8 1.0	 2.0 2.5	 – –	 0.8 1.0	 2.0 2.5	 – –	 0.8 1.0	 2.0 2.5	mA
Voltage Gain R_L ≥ 15 kΩ, V_{CC} = 15 Vdc	A_{VOL}	50	200	–	50	200	–	25	100	–	25	100	–	V/mV
Large Signal Response Time V_I = TTL Logic Swing, V_{ref} = 1.4 Vdc, V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	–	–	300	–	–	300	–	–	300	–	–	300	–	ns
Response Time (Note 6) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	–	–	1.3	–	–	1.3	–	–	1.3	–	–	1.3	–	µs
Output Sink Current V_I (–) ≥ +1.0 Vdc, V_I(+) = 0, V_O ≤ 1.5 Vdc	I_{Sink}	6.0	16	–	6.0	16	–	6.0	16	–	6.0	16	–	mA
Saturation Voltage V_I(–) ≥ +1.0 Vdc, V_I(+) = 0, I_{sink} ≤ 4.0 mA	V_{sat}	–	130	400	–	130	400	–	130	400	–	130	500	mV
Output Leakage Current V_I(+) ≥ +1.0 Vdc, V_I(–) = 0, V_O = +5.0 Vdc	I_{OL}	–	0.1	–	–	0.1	–	–	0.1	–	–	0.1	–	nA

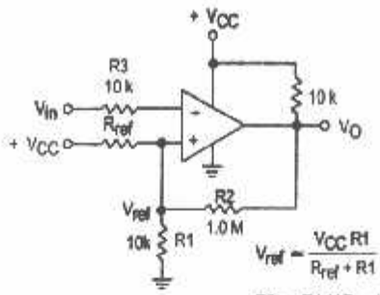
PERFORMANCE CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = T_{low} to T_{high} [Note 3])

Characteristic	Symbol	LM239A/339A			LM239/339			LM2901/2901V			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	–	–	±4.0	–	–	±9.0	–	–	±15	–	–	±40	mVdc
Input Bias Current (Notes 4, 5) (Output in Analog Range)	I_{IB}	–	–	400	–	–	400	–	–	500	–	–	1000	nA
Input Offset Current (Note 4)	I_{IO}	–	–	±150	–	–	±150	–	–	±200	–	–	±300	nA
Input Common Mode Voltage Range	V_{ICMR}	0	–	V_{CC} −2.0	0	–	V_{CC} −2.0	0	–	V_{CC} −2.0	0	–	V_{CC} −2.0	V
Saturation Voltage V_I(–) ≥ +1.0 Vdc, V_I(+) = 0, I_{sink} ≤ 4.0 mA	V_{sat}	–	–	700	–	–	700	–	–	700	–	–	700	mV
Output Leakage Current V_I(+) ≥ +1.0 Vdc, V_I(–) = 0, V_O = 30 Vdc	I_{OL}	–	–	1.0	–	–	1.0	–	–	1.0	–	–	1.0	µA
Differential Input Voltage All V_I ≥ 0 Vdc	V_{ID}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	Vdc

NOTES: 3. (LM239/239A) T_{low} = –25°C, T_{high} = +85°
(LM339/339A) T_{low} = 0°C, T_{high} = +70°C
(MC3302) T_{low} = –40°C, T_{high} = +85°C
(LM2901) T_{low} = –40°C, T_{high} = +105°
(LM2901V) T_{low} = –40°C, T_{high} = +125°C

4. At the output switch point, V_O = 1.4 Vdc, R_S ≤ 100 Ω 5.0 Vdc ≤ V_{CC} ≤ 30 Vdc, with the inputs over the full common mode range (0 Vdc to V_{CC} –1.5 Vdc).
5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

Figure 2. Inverting Comparator with Hystersis



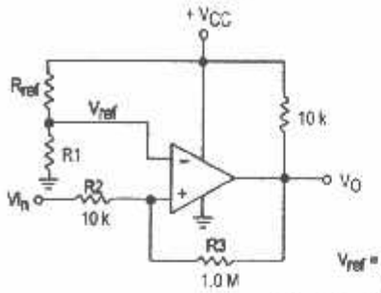
$$V_{ref} = \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R3 = R1 \,//\, R_{ref} \,//\, R2$$

$$V_H = \frac{R1 \,//\, R_{ref}}{R1 \,//\, R_{ref} + R2}\,[V_{O(max)} - V_{O(min)}]$$

$$R2 \gg Rref \,//\, R1$$

Figure 3. Noninverting Comparator with Hysteresis



$$V_{ref} = \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R2 = R1 \,//\, R_{ref}$$

Amount of Hysteresis V_H

$$V_H = \frac{R2}{R2 + R3}\,[V_{O(max)} - V_{O(min)}]$$

Typical Characteristics

(V_{CC} = 15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

Figure 4. Normalized Input Offset Voltage

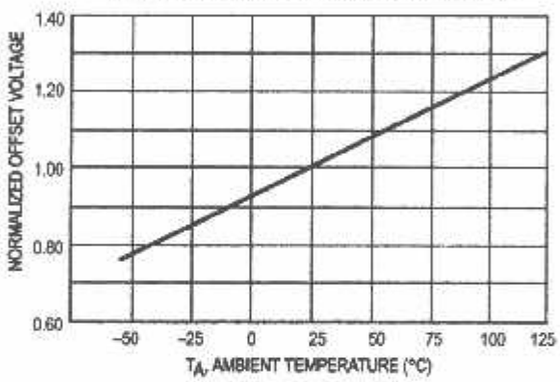


Figure 5. Input Bias Current

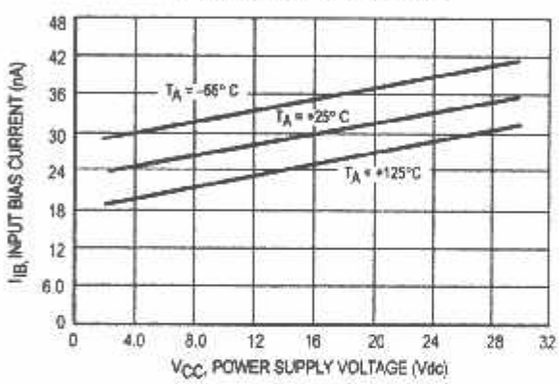


Figure 6. Output Sink Current versus Output Saturation Voltage

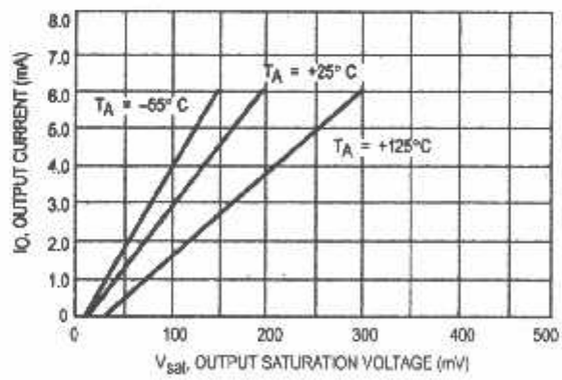
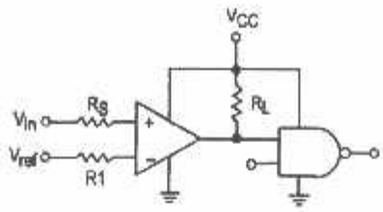


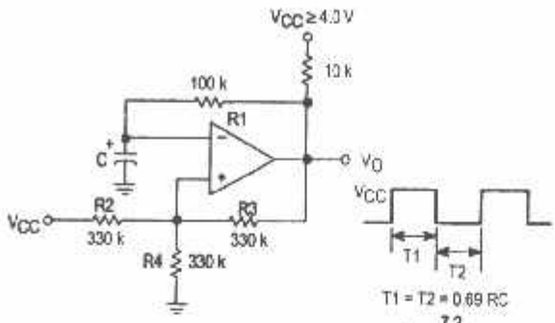
Figure 7. Driving Logic



RS = Source Resistance
R1 = RS

Logic	Device	VCC (V)	RL kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5.0	10

Figure 8. Squarewave Oscillator



$T1 = T2 = 0.69\ RC$

$f \approx \frac{7.2}{C(\mu F)}$

R2 = R3 = R4

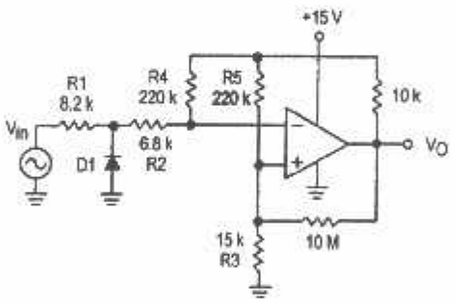
R1 ≈ R2 // R3 // R4

APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (< 10 mV) is also recommended. It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator's inputs. Voltages more negative than −300 mV should not be used.

Figure 9. Zero Crossing Detector (Single Supply)



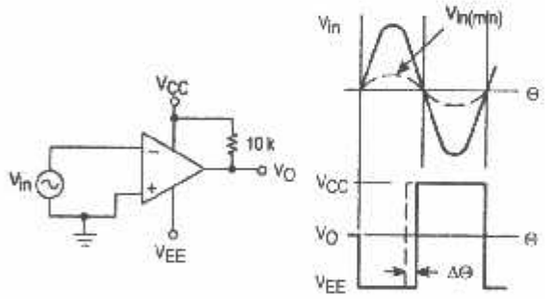
D1 prevents input from going negative by more than 0.6 V.

R1 = R2 = R3

$R3 \leq \frac{R5}{10}$ for small error in zero crossing

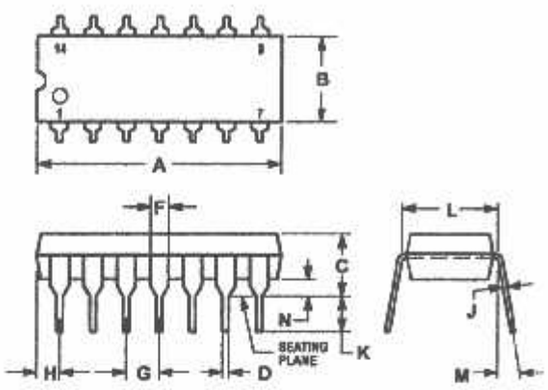
Figure 10. Zero Crossing Detector (Split Supplies)

$V_{in(min)}$ = 0.4 V peak for 1% phase distortion (Δθ).



OUTLINE DIMENSIONS

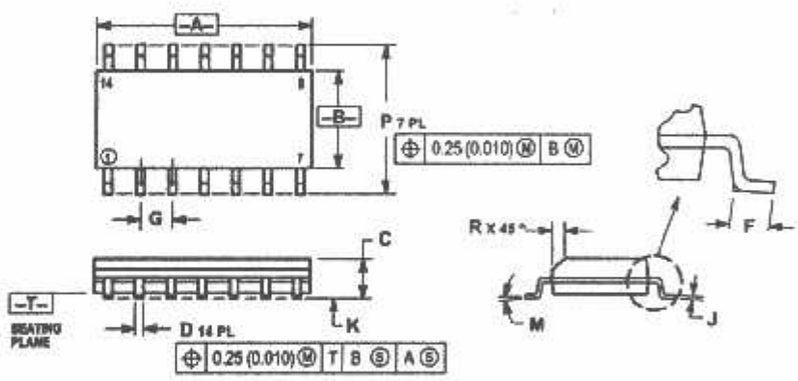
N, P SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE L



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
(SO–14)
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

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