

SKRIPSI

PERENCANAAN DAN PEMBUATAN PROGRAMMABLE SWITCHING POWER SUPPLY 0-15 VOLT, ARUS MAKSIMAL 2 AMPERE DENGAN MENGGUNAKAN MIKROKONTROLER AT89S8252



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**JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG**

SEPTEMBER 2007

LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN PROGRAMMABLE SWITCHING POWER SUPPLY 0-15 VOLT, ARUS MAKSIMAL 2 AMPERE DENGAN MENGGUNAKAN MIKROKONTROLER AT89S8252

SKRIPSI

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2007



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3.	Tulis ulang tentang pengujian alat : a. Pengujian minimum sistem b. Pengujian switching power supply c. Analisa error	
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Perbaikan meliputi:

No.	Materi perbaikan	Paraf Penguji II
1.	Metode penelitian	
2.	Teori mosfet/awitching power supply	
3.	Kesimpulan	
4.	Analisa pengujian alat	

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ABSTRAK

PERENCANAAN DAN PEMBUATAN PROGRAMMABLE SWITCHING POWER SUPPLY 0-15 VOLT, ARUS MAKSIMAL 2 AMPERE DENGAN MENGGUNAKAN MIKROKONTROLER AT89S8252

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Kata Kunci : Switching power supply, Mikrokontroler AT89S8252, LCD

Alat ini bertujuan sebagai sebuah catu daya jenis switching yang dapat di program untuk mendapatkan besaran tegangan yang diinginkan dengan cepat, stabil, dan presisi.

Dengan menggunakan metode pengolah lebar pulsa (PWM) yang dibangkitkan oleh mikrokontroler AT89S8252 sebagai pengolah data, penjaga kestabilan serta pengolah keputusan didapatkan lebar pulsa yang bervariasi.

Sehingga output dapat diatur sesuai keinginan kita yang dapat beroperasi pada frekuensi tinggi antara 1-100 KHz dengan pengaturan tegangan yang baik dan bernilai error kecil $\pm 1.29 \%$.

KATA PENGANTAR

Puji syukur kehadiran Allah SWT atas rahmat, hidayah, kasih sayang dan karunia – Nya sehingga Skripsi yang berjudul **“PERENCANAAN DAN PEMBUATAN PROGRAMMABLE SWITCHING POWER SUPPLY 0-15 VOLT, ARUS MAKSIMAL 2 AMPERE DENGAN MENGGUNAKAN MIKROKONTROLER AT89S8252”** ini dapat terselesaikan walau masih banyak kurang sempurna pada alat ini. Tidak lupa Shalawat serta Salam semoga tetap terlimpahkan kepada pemimpin besar kita dan sekaligus ulama besar kita adalah junjungan Nabi Besar Muhammad SAW beserta keluarga dan para sahabat – sahabatnya. Amien.

Penulisan Skripsi ini tidak akan terselesaikan dengan baik tanpa bantuan, bimbingan, saran, kritik dan doa dari berbagai pihak. Oleh karena itu penulis menyampaikan rasa terima kasih yang sedalam – dalamnya kepada :

1. Bapak Prof. Dr. Eng Ir. Abraham Lomi, MSEE selaku Rektor Institut Teknologi Nasional Malang.
2. Bapak Ir. Mochtar Asroni, MSME. Selaku Dekan Fakultas Teknologi Industri Institut Teknologi Nasional Malang.
3. Bapak Ir. F. Yudi Limpraptono, MT Selaku Ketua Jurusan Teknik Elektro S 1 Institut Teknologi Nasional Malang.
4. Bapak Ir. Widodo Pudji Mulyanto, MT selaku dosen pembimbing pertama.
5. Bapak I Komang Somawirata, ST, MT selaku dosen Pembimbing kedua.

6. Teman-teman semua yang telah banyak membantu dalam menyelesaikan laporan skripsi ini.

Meskipun telah dikaji ulang dan dikerjakan dengan sungguh – sungguh namun penulis menyadari bahwa Skripsi ini masih jauh dari sempurna, karena keterbatasan pengetahuan dan keterampilan yang penulis miliki, sehingga segala kritik dan saran penulis terima untuk dijadikan pedoman didalam menyusun laporan berikutnya yang lebih sempurna.

Akhir kata semoga Skripsi ini dapat memberikan manfaat bagi seluruh masyarakat ilmiah pada khususnya dan pembaca pada umumnya.

Malang, Agustus 2007

Penyusun

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BAB I

PENDAHULUAN

1.1. LATAR BELAKANG

Catu daya jenis *switching* ditandai dengan adanya penggunaan piranti semikonduktor yang berfungsi untuk *men-switch* (mensaklar) aliran arus di dalam catu. Mempunyai regulasi yang baik karena menggunakan *close loop*, ukurannya kecil dan kemampuannya untuk dapat beroperasi pada tegangan yang masuk yang lebih besar. Sebagai tambahan, karena semakin murah harga semi konduktor berdaya tinggi dan rangkaian terpadu maka catu daya jenis *switching* ini mempunyai banyak keuntungan dalam segi ekonomis.

Catu daya elektronik (atau catu daya yang digunakan dalam rangkaian elektronik) seringkali berarti sebagai pengubah (*altering*), pengendalian (*controlling*) atau pengaturan (*regulating*) daya listrik. Pengaturan cukup padat artinya, termasuk penyearah gelombang (*rectify*), mengubah AC ke DC (*invert*), menghaluskan (*regulasi*), atau mengubah tingkat tegangan atau arus, sedangkan catu daya jenis *switching* melibatkan proses membangkitkan pengaturan dan penyaringan oleh piranti *switching*.

1.2. TUJUAN

Adapun tujuan atau sasaran yang ingin dicapai dari skripsi ini, adalah sebagai berikut:

1. Merencanakan dan membuat sebuah catu daya jenis *switching* yang dapat di program untuk mendapatkan besaran tegangan yang diinginkan dengan cepat, stabil, presisi regulasi yang tinggi, lebih ringan dan berharga lebih murah dan output dapat diatur sesuai dengan keinginan kita..
2. Mendalami pemakaian peralatan pengolah modulasi lebar pulsa (PWM), khususnya yang dibangkitkan oleh mikrokontroler (Digital PWM) untuk mendapatkan lebar pulsa yang bervariasi.
3. Mendalami pemanfaatan mikrokontroler khususnya AT89S8252 sebagai pengolah data, penjaga kestabilan serta pengolah keputusan.

1.3. PERMASALAHAN

Bagaimana mendesain rangkaian *inverter* harus disesuaikan dengan jenis inti transformator frekuensi tinggi yang ada dipasaran, dan apabila yang diinginkan secara khusus, kita dapat mendesain gulungannya sendiri.

Kelemahan dari analog adalah pengolah lebar pulsa secara analog sangat sulit diterapkan untuk tegangan yang bervariasi, karena pada suatu tegangan tertentu, OP AMP didalam PWM (*Pulse Width Modulation*) analog menjadi kritis dan interferensi gelombang dari *switching* itu sendiri dapat merusak bentuk gelombang yang asli. Dalam hal ini penulis menggunakan mikrokontroler sebagai pengendali lebar pulsa agar tegangan yang dihasilkan dapat bervariasi.

1.4. BATASAN MASALAH

- * Tegangan keluaran dari alat yang direncanakan hanya dari 0 - 15 Volt
- * Frekuensi kerja antara 1 – 100 Khz
- * Arus maksimum 2 Amper
- * Tegangan jala – jala 220 – 230 Volt
- * Pengaturan tegangan menggunakan PWM (Pulse Width Modulation)
- * Trafo yang dipakai adalah trafo dengan inti ferit, unit ini tidak dapat dibebani 2 Amper karena kondisi trafo.

1.5. METODOLOGI

1. Studi Literatur.
2. Perencanaan berdasarkan studi literatur dan komponen yang ada dipasaran.
3. Pembuatan dan pengujian.

1.6. URAIAN SINGKAT

Skripsi ini membahas tentang perencanaan dan pembuatan *programmable switching power supply* dengan kemampuan output tegangan antara 0 sampai 15 Volt dan arus tidak lebih dari 2 Ampere, disamping itu dibahas beberapa piranti penunjang seperti ADC, desain filter, cara mendapatkan lebar pulsa variabel, sistem pengontrol kestabilan yang digunakan dalam pembuatan alat ini.

Bab pertama merupakan pendahuluan yang berisikan latar belakang, tujuan dan permasalahan yang mendasari pembuatan skripsi ini.

Bab kedua membahas apa yang dimaksud dengan sistem peregulasian atau pengaturan catu daya *switching*, cara mendapatkan lebar pulsa variabel, mikrokontroler AT89S8252 serta piranti penunjangnya dalam pembuatan skripsi ini.

Perancangan perangkat keras dan perangkat lunak dibahas pada bab tiga. Pada perancangan perangkat keras akan dijelaskan masalah-masalah dalam desain perancangan suatu *switching power supply*, hubungan antara mikrokontroler AT89S8252 dan peralatan pendukungnya. Pada perancangan perangkat lunak akan dijelaskan mengenai langkah-langkah pembuatan program minimum sistem AT89S8252.

Bab empat merupakan bab pengujian alat, pengumpulan data hasil pengujian dan analisa data. Sedangkan pada bab lima merupakan bab terakhir buku ini yang berisi kesimpulan dari seluruh hasil sebelumnya.

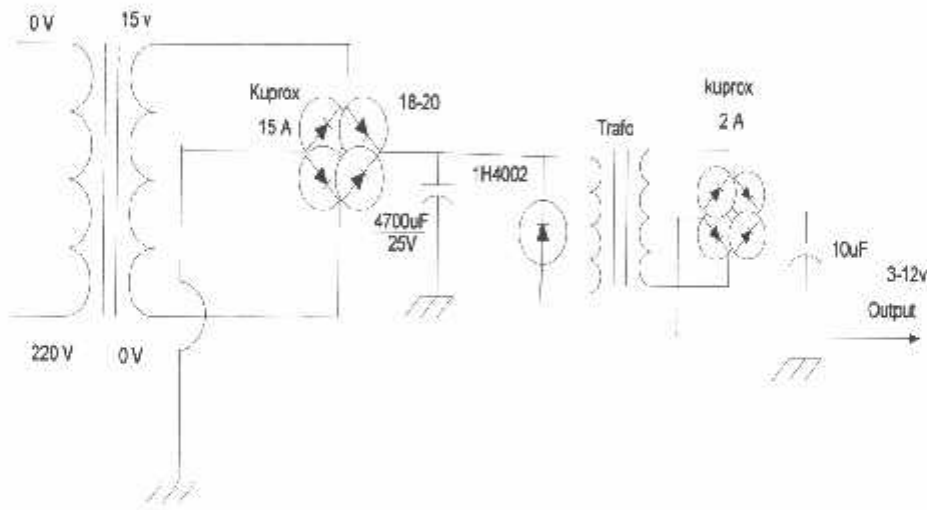
Lampiran dalam buku ini, khususnya data sheet, harus dianggap sebagai satu kesatuan yang utuh dengan bab-bab yang lain, mengingat hal-hal yang tercantum dalam data sheet sudah dianggap umum dan tidak memerlukan pembahasan lebih lanjut.

BAB II.

DASAR TEORI

2.1. RANGKAIAN DASAR DARI SWITCHING REGULATOR

Rangkaian *switching* ditandai dengan adanya piranti *switch* yang mengadakan transfer energi dari input ke output rangkaian. Secara garis besar rangkaian ini dapat digambarkan sebagai berikut:



GAMBAR 2.1.
RANGKAIAN DASAR SWITCHING REGULATOR

2.2. KONFIGURASI RANGKAIAN PENGONTROL

Ada banyak konfigurasi rangkaian pengontrol pada mode operasi dan piranti *switching* yang digunakan dalam catu daya jenis *switching*. Memang banyak sekali pendekatan yang dapat digunakan untuk memenuhi kebutuhan yang sama itu. Seluruh metode ini pada dasarnya adalah terdiri dari keadaan konduktif “On” dan “Off”. Cara-cara ini dapat diperinci sebagai berikut :

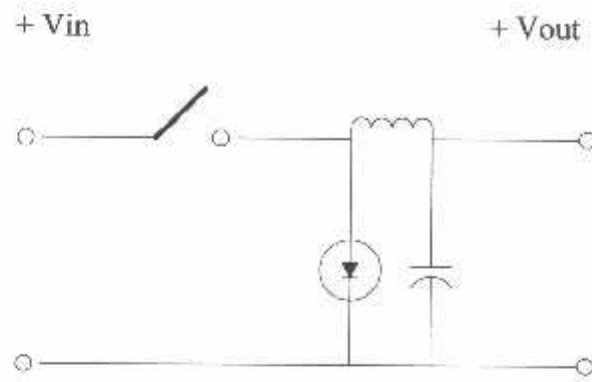
1. Variasi kedua frekuensi dan waktunya yang dapat secara random atau waktu “Off” yang konstan.
2. Frekuensi konstan, dengan waktu “On” yang variabel.
3. Waktu “On” konstan (atau lebar pulsa) dengan frekuensi variabel.

Disini penulis menggunakan konfigurasi yang kedua yaitu frekuensi konstan dan waktu “On” yang variabel.

2.3. JENIS-JENIS KONVERTER

2.3.1. Jenis Konverter Tidak Terisolasi

A. *Buck* adalah salah satu jenis konverter step down tanpa isolasi. Tegangan outputnya selalu lebih kecil atau sama dengan tegangan inputnya. Rangkaian *Buck* memutuskan tegangan yang masuk dan menghasilkan sebuah lebar pulsa gelombang persegi yang variabel. Pada mode ini tegangan output = tegangan input $\times$ duty cycle.



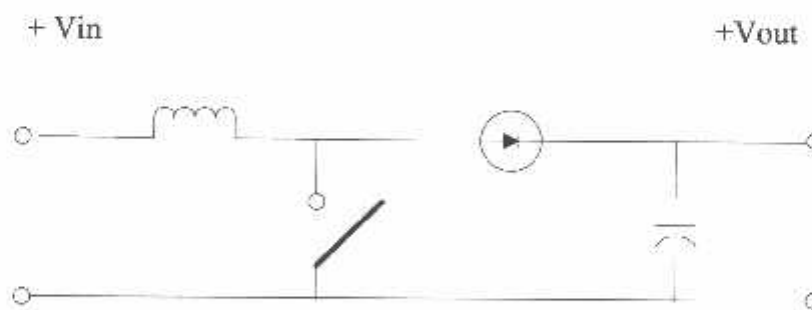
BUCK (STEP DOWN)

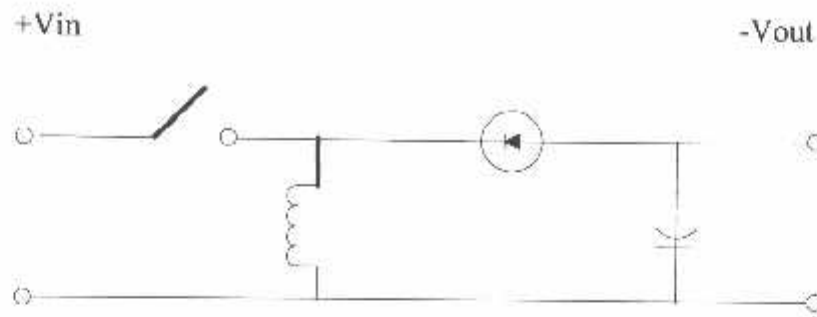
$$V_{Out} < V_{in}$$

GAMBAR 2.2.

KONVERTER TYPE BUCK

- B. Konverter dari jenis yang lainnya adalah jenis *Boost*. Konverter ini lebih halus dibandingkan dengan yang pertama dan converter ini dapat menaikkan atau menurunkan tegangan output





BOOST (STEP UP)

$$V_{out} > V_{in}$$

a.

BOOST VARIATION

STEP UP OR DOWN

b.

GAMBAR 2.3.

KONVERTER TYPE BOOST

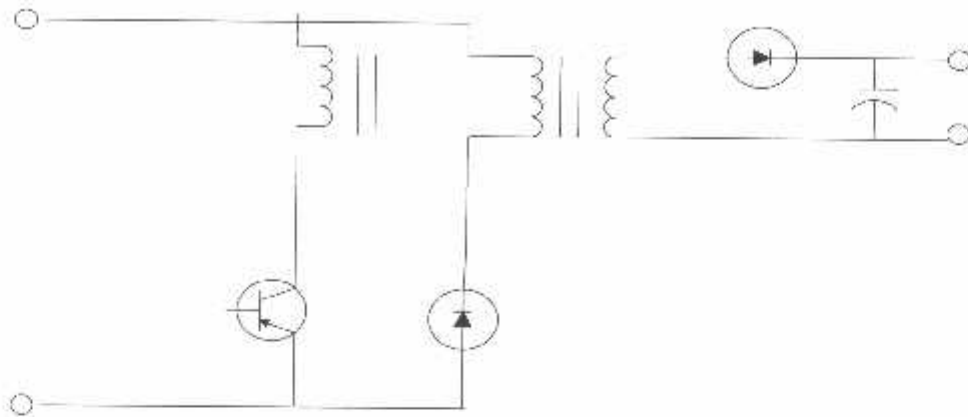
2.3.2. Jenis Konverter Terisolasi

A. *Fly back* merupakan konverter terisolasi dimana ia mempunyai dua sisi kumparan yaitu sisi primer dan sekunder. Sisi primer menyimpan energi dan kemudian menginduksikan energi itu pada sisi sekunder untuk selanjutnya disearahkan dan difilter.

Suatu lilitan *Clamp* adakalanya (tidak mutlak) diperlukan pada mode ini untuk mengembalikan energi reaktansi bocor ke jala-jala dengan baik.

Keunggulan jenis ini terdapat pada harga yang murah karena tidak memerlukan induktor “*Choke*”, tetapi disisi lain kelemahan rangkaian ini terdapat

pada *ripple factor* yang lebih besar dibandingkan dengan jenis yang akan kita bicarakan.



FLYBACK CLAMP WINDING OPTIONAL

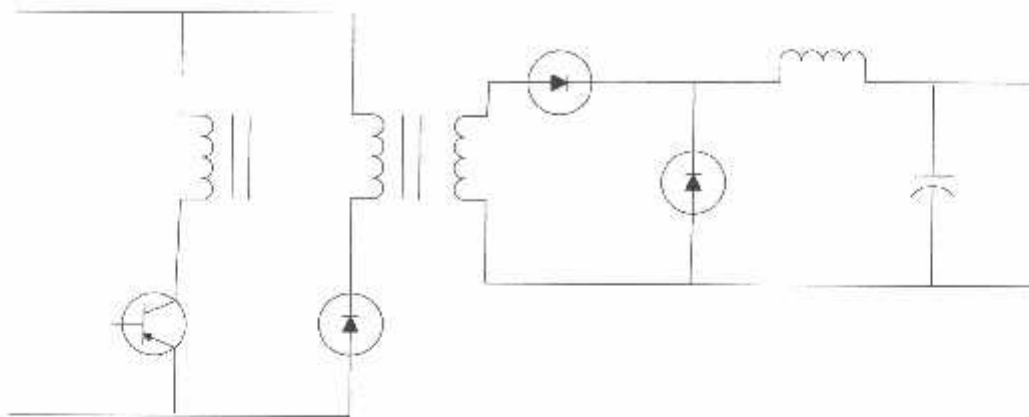
GAMBAR 2.4.

KONVERTER TYPE FLYBACK

B. *Forward* adalah jenis catu daya yang mutlak memerlukan lilitan *Clamp*. Mode ini lahir dari pengembangan jenis *Buck* dengan bentuk trafo yang komplek.

Jenis ini kebal terhadap gangguan kejenuhan inti trafo karena adanya lilitan *Clamp* sebagai kompensasi.

FORWARD

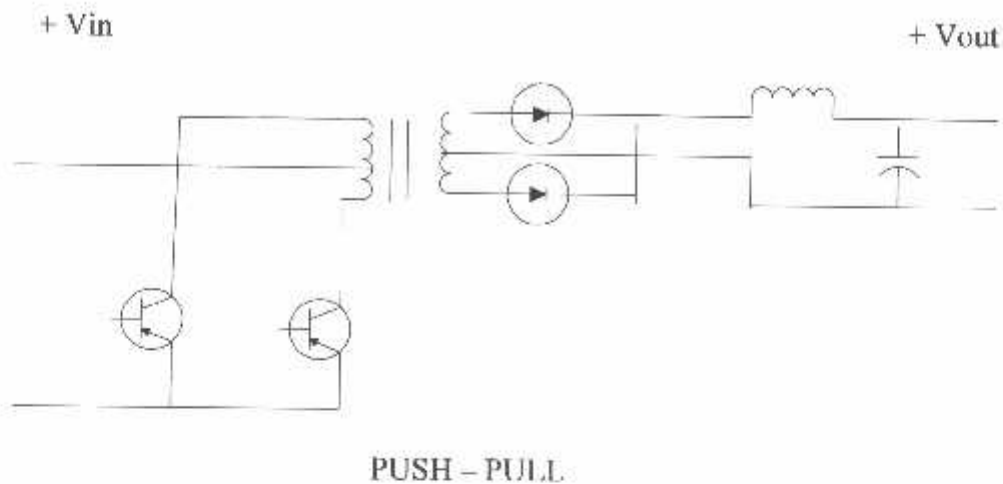


CLAMP WINDING IS NECESSARY

GAMBAR 2.5.

KONVERTER TYPE FORWARD

C. *Push-pull* adalah merupakan konverter tertua yang pernah dipakai, type ini sangat mudah diaplikasikan dari tegangan 12 volt DC sampai 120 volt DC input. Saturasi inti trafo pada tegangan input kecil sangat minimal, tetapi jika dipakai input DC yang besar maka saturasi inti trafo akan menjadi masalah yang sulit ditanggulangi.



PUSH – PULL

GAMBAR 2.6.

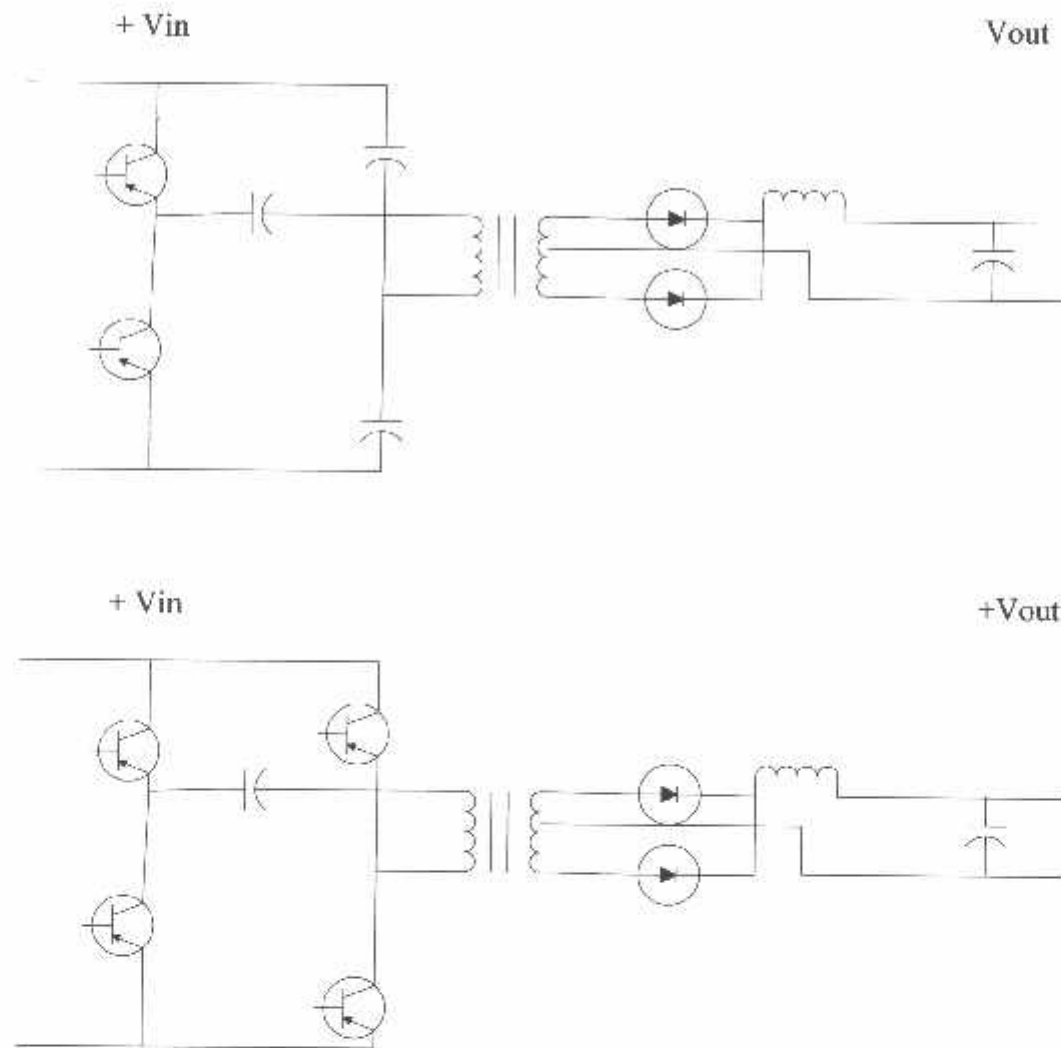
KONVERTER TYPE PUSH – PULL

D. Half and Full Bridge

Rangkaian paling populer yang sering dipakai untuk daya besar adalah dari type *half bridge*, karena :

1. Transistor tidak pernah terbeban lebih dari tegangan puncak jala-jala setengah energi jala-jala yang dipakai.
2. Saturasi inti trafo mudah dikoreksi dengan meletakkan kapasitor kopling yang kecil ($2,0 \mu F \leq C \leq 5,0$).

Sedangkan *full bridge* menyalurkan energi pada jalur primer secara penuh, sehingga output trafo hampir selalu mengeluarkan daya dua kali lipat dibandingkan dengan *half bridge* (dengan menggunakan type transistor yang sama).



HALF BRIDGE

a.

FULL BRIDGE

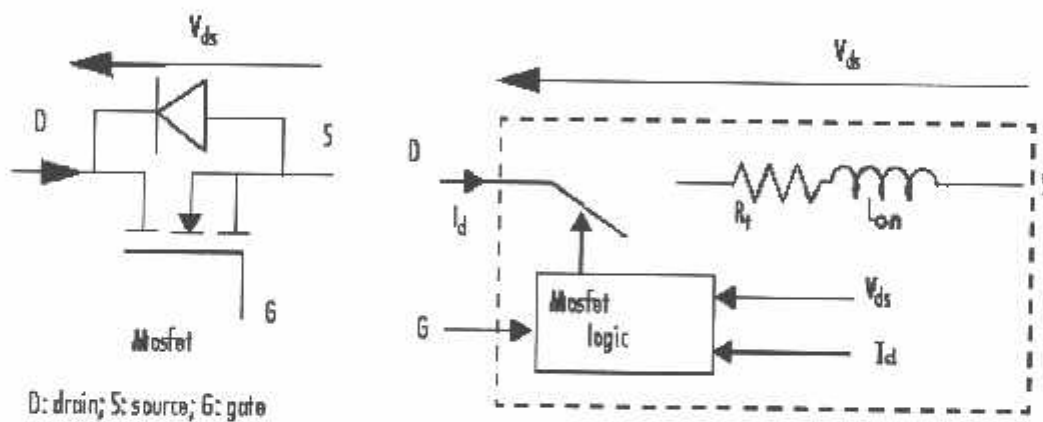
b.

GAMBAR 2.7.

KONVERTER TYPE HALF BRIDGE DAN FULL BRIDGE

2.4. MOSFET

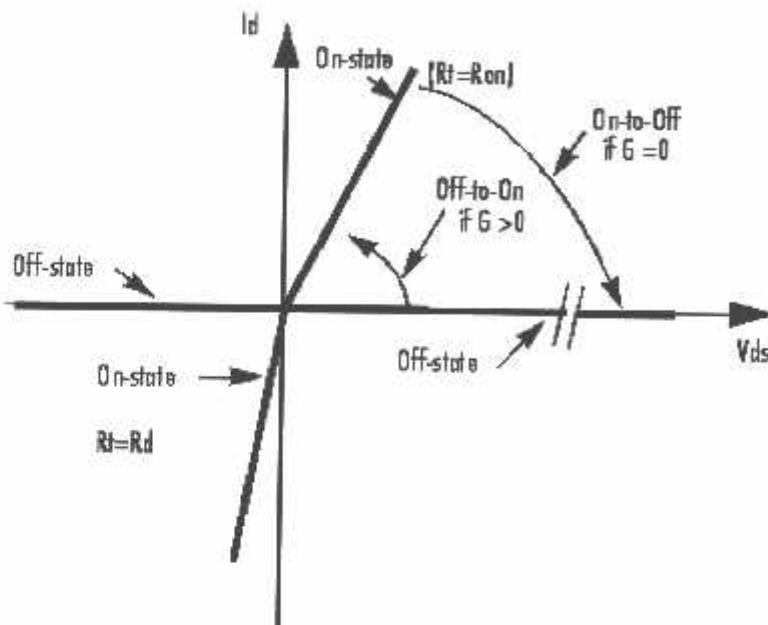
Metal-Oxide-Semiconductor-Field-Effect-Transistor (Mosfet) Blok adalah suatu semi konduktor yang dapat dikontrol oleh gerbang sinyal ($G > 0$) jika mendapat current I_d yang positif ($I_d > 0$). Mosfet Blok dihubungkan secara paralel dengan suatu dioda internal yang menyala ketika Mosfet Blok dibiaskan reverse ($V_{ds} < 0$). Model disimulasikan sebagai kombinasi rangkaian suatu variabel resistor (R_t) dan induktor (L_{on}) secara seri dengan switch control sebagai logical signal ($G > 0$ Atau $G = 0$).



GAMBAR 2.8.

SIMBOL MOSFET

Mosfet Blok menyala ketika voltase drain-source adalah positif dan sinyal positif diterapkan di masukan gerbang ($G > 0$).



GAMBAR 2.9.
PARAMETER MOSFET

Dengan arus positif yang mengalir melalui alat, Mosfet Blok mati (turns off) ketika masukan gerbang menjadi nol. Jika current I_d negatif (I_d yang mengalir di dioda internal) dan sinyal gerbang adalah nol ($G = 0$), Mosfet Blok mati ketika current I_d menjadi nol ($I_d = 0$).

- Catatan bahwa resistansi on-state R_t tergantung pada arah arus searah :

- $R_t = R_{on}$ jika $I_d > 0$, dimana R_{on} mendapatkan nilai tertentu pada bias forward resistansi konduksi Mosfet Blok
- $R_t = R_d$ jika $I_d < 0$, dimana R_d mendapatkan resistansi dioda internal.

Mosfet Blok juga berisi suatu rangkaian R_s - C_s snubber sirkuit, yang biasanya dihubungkan paralel dengan Mosfet Blok. Kamu dapat menetapkan snubber untuk memberi hambatan ($C_s = \text{Inf}$) atau kapasitif ($R_s = 0$). Jika kamu menetapkan baik $R_s = \text{Inf}$ maupun $C_s = 0$, snubber dihapus dan hilang pada icon Mosfet.

Arus Awal I_c yang mengalir Mosfet Blok pada umumnya dimulai dari nol, sehingga simulasi dimulai dengan pemblokkan Mosfet. Bagaimanapun, harus ditetapkan suatu Nilai I_c yang sesuai dengan sirkuit. Dengan demikian semua state linier harus di-set. Initializing semua state suatu konverter power-electronic adalah suatu pertanyaan kompleks. Oleh karena itu, pilihan ini hanya bermanfaat pada sirkuit sederhana.

- Kotak Parameter Mosfet

Block Parameters: Mosfet

Mosfet (mask)
 Simulates a MOSFET with internal diode, in parallel with a series R_s - C_s snubber circuit. In on-state MOSFET has internal resistance (R_{on} if $I_{ds} > 0$, R_{diode} if $I_{ds} < 0$) and inductance (L_{on} - required by model, cannot be set to zero). In off-state MOSFET impedance is infinite.

1st input (d) : Electrical drain connection
 2nd input (g) : Simulink gate signal (on when non zero)
 1st output (s) : Electrical source connection
 2nd output (m) : Simulink measurement output [$I_{ds}(A)$ $V_{ds}(V)$]

Parameters

MOSFET resistance R_{on} (Ohms) :
 0.001

MOSFET inductance L_{on} (H) :
 10e-6

Internal diode resistance R_d (Ohms) :
 .001

Initial current I_c (A) :
 0

Snubber resistance R_s (Ohms) :
 10

Snubber capacitance C_s (F) :
 0.01e-6

OK Cancel Help Apply

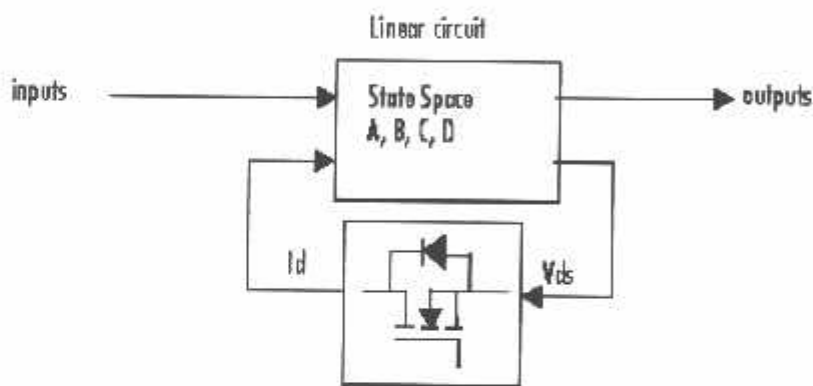
- Masukan Dan Keluaran

Keluaran dan masukan pertama Mosfet dikoneksikan ke drain (d) dan sumber (s). Masukan yang kedua (g) adalah suatu sinyal Simulink logis yang diaplikasikan pada gerbang. Keluaran yang kedua adalah suatu Simulink Garis vektor Pengukuran [I_d , V_{ds}] yang mengembalikan Voltase Dan Arus Mosfet.

- Asumsi Dan Pembatasan

Mosfet blok mengimplementasikan suatu model macro Alat Mosfet yang riil. Model macro ini tidak mempertimbangkan baik ilmu alat ukur maupun proses alam yang kompleks [1].

Di dalam Penyajian Simulink, Mosfet diperagakan sebagai elemen nonlinear yang menghubungkan dengan sirkuit linier seperti di bawah ini.



GAMBAR 2.10.

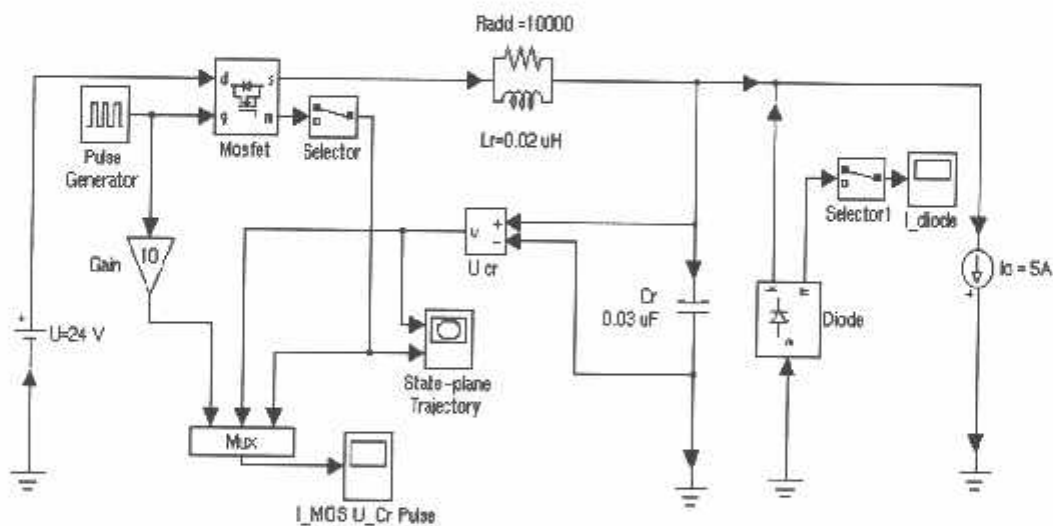
SIMULINK MOSFET

Untuk menghindari suatu pengulangan secara aljabar, Mosfet Induktansi Lon tidak bisa di-set nol. Masing-Masing Mosfet menambahkan suatu state ekstra ke model sirkuit elektrik. Sejak Mosfet diperagakan sebagai sumber arus, Mosfet tidak bisa dihubungkan secara seri dengan suatu Inductor, suatu sumber arus, atau suatu sirkuit terbuka, kecuali jika digunakan suatu sirkuit snubber.

Kita harus menggunakan suatu integrator algoritma untuk menirukan sirkuit yang berisi mosfets. *ode23tb* dan *ode15s* pada umumnya memberikan keunggulan kecepatan simulasi.

- Contoh

Contoh berikut menggambarkan penggunaan Blok Mosfet dalam Zero-Current-Quasi-Resonant Switch Konverter. Maka suatu konverter, yang sekarang yang diproduksi oleh Lr-Cr sirkuit resonan mengalir didalam alat tersebut, yang menyebabkan Turn on dan Off saat arus nol [1]. Frekuensi Switchnya adalah 2 MHZ dan lebar pulsa adalah 72 derajat tingkat (duty cycle: 20%). Contoh ini tersedia di *psbmosconv.mdl* file

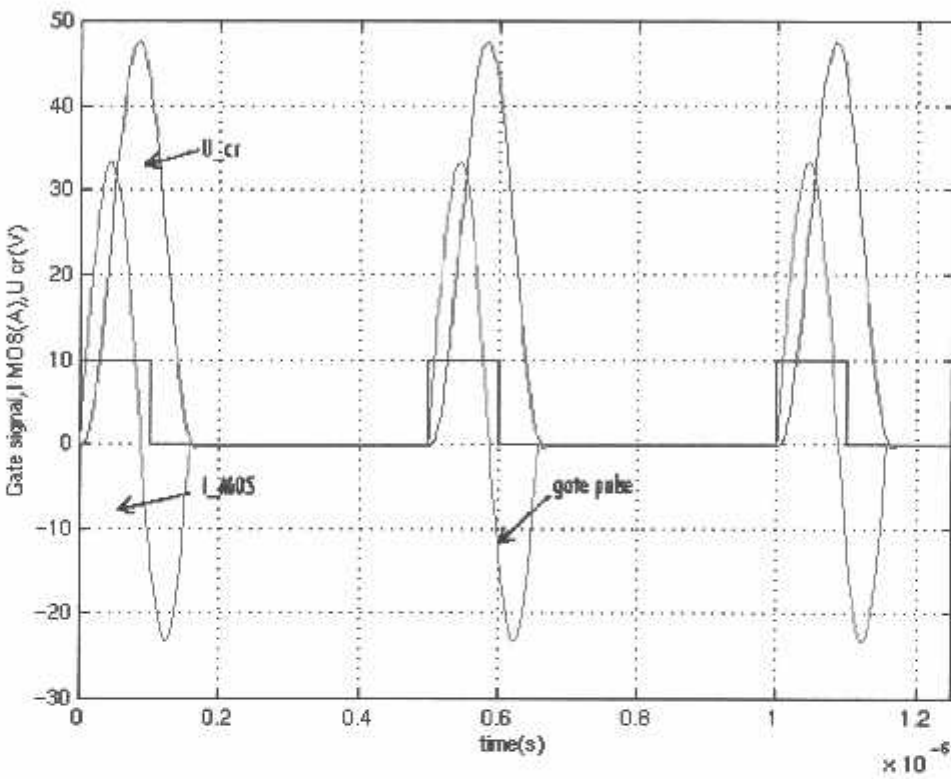


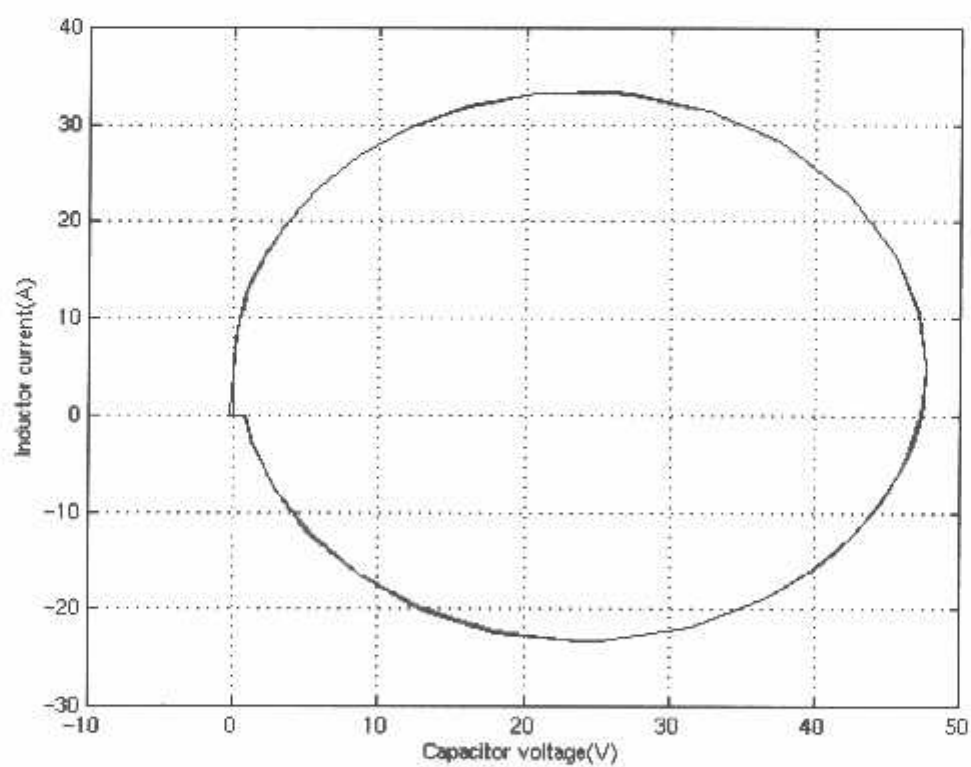
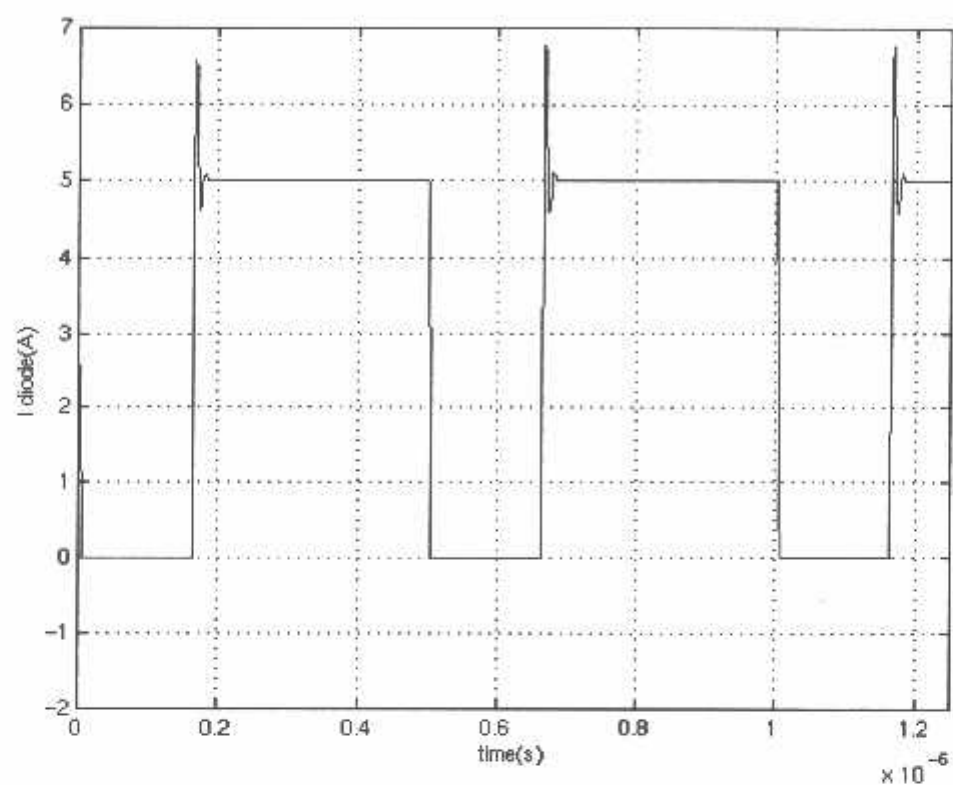
GAMBAR 2.11.

RANGKAIAN MOSFET

Zero-Current-Quasi-Resonant Konverter

Jalankan simulasi dan amati voltase kapasitor tersebut, mosfet arus, gerbang sinyal pulsa, arus dioda, dan state-plane trajectory (arus induktor vs voltase kapasitor).





GAMBAR 2.12.
SINYAL, GRAFIK MOSFET

2.5. Mikrokontroller AT89S8252

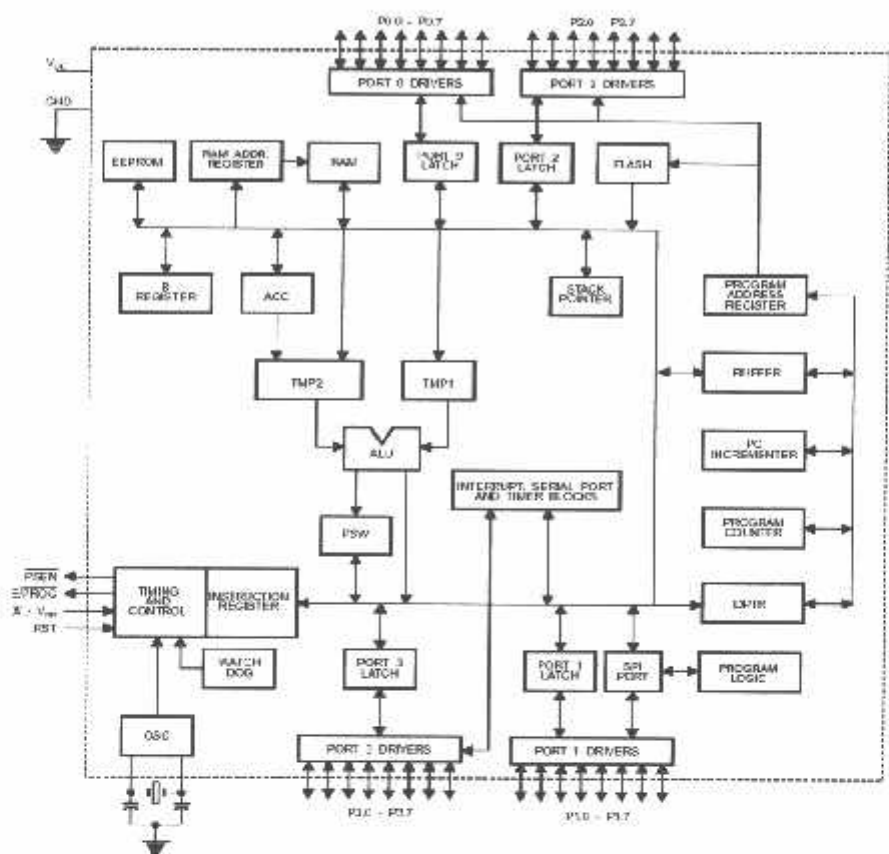
Mikrokontroller AT89S8252 adalah mikrokontroller ATMEL yang kompatibel, memerlukan daya yang rendah, memiliki performa tinggi dan merupakan mikrokontroller 8 bit yang dilengkapi 2 Kbyte EEPROM (*Electrical Erasable and Programmable Read Only Memory*) dan 256 byte RAM *internal*. Program memori yang dapat diprogram ulang dalam sistem atau menggunakan programmer non volatile memori konvensional.

2.5.1. Arsitektur mikrokontroller AT89S8252

Arsitektur mikrokontroller AT89S8252 adalah sebagai berikut:

- Termasuk dalam keluarga MCS 51
- Membutuhkan supply tegangan yang relatif kecil (4V-6V)
- 8 Kbyte *flash memory*
- 2 Kbyte EEPROM
- 256 byte *internal memory*
- 3 x 16 bit *timer/counter*
- 32 pin I/O
- 9 Buah sumber *interrupt*
- 2 buah data pointer
- 1 serial port full duplex

Diagram Blok AT89S8252



Gambar 2.12.
Diagram Blok Mikrokontroler AT89S8252

2.5.2. Konfigurasi Pin Pada Mikrokontroller AT89S8252

Konfigurasi kaki-kaki mikrokontroller AT89S8252 terdiri dari 40 pin, seperti terlihat pada gambar 2.2 sebagai berikut:



Gambar 2.13.
Konfigurasi Pin Mikrokontroller AT89S8252

Fungsi dari tiap-tiap pin adalah sebagai berikut:

- 1. VCC (supply tegangan)
- 2. GND (*Ground*)
- 3. Port 0

Merupakan port *input/output* dua arah dan dikonfigurasikan sebagai *multiplex* dua bus alamat rendah (A0-A7) dan data selama pengaksesan program memori dan data memori *internal*

4. Port 1

Merupakan port *input/output* dua arah dengan *internal pull-up*Port 2

Merupakan port *input/output* dua arah dengan *internal pull-up* mengeluarkan *address* tinggi selama pengambilan program *memory external*.

5. Port 3

Merupakan port *input/output* dua arah dengan *internal pull-up*

Port 3 memiliki fungsi khusus, yaitu:

- RXD (P3.0) : port *input* serial
- TXD (P3.1) : port *output* serial
- INT0 (P3.2) : *interrupt 0 external*
- INT1 (P3.3) : *interrupt 1 external*
- T0 (P3.4) : *input external timer 0*
- T1 (P3.5) : *input external timer 1*
- /WR (P3.6) : strobe tulis *memory data external*
- /RD (P3.7) : strobe baca *memory data external*

6. RST

Input reset

7. ALE / PROG

Pulsa *output* ALE digunakan untuk proses "*latching*" byte *address* rendah (A0-A7) selama pengaksesan ke memori *external*. Pin ini juga untuk memasukan pulsa program selama pemrograman.

8. PSEN

Merupakan strobe baca ke program memori *external*.

9. EA / VPP

Jika EA diberikan logika rendah (*ground*), maka mikrokontroller akan mengakses program dari memori *external* dan jika diberi logika tinggi (dihubungkan VCC), maka akan mengakses program dari memori *internal*.

10. XTAL1 DAN XTAL2

Pin ini dihubungkan dengan kristal bila menggunakan osilator *internal*. XTAL1 merupakan masukan ke rangkaian osilator *internal* sedangkan XTAL2 keluaran dari rangkaian osilator *internal*.

2.5.3. SFR Tambahan Pada Atmel AT89S8252

Selain memiliki SFR(*Special Function Register*) seperti halnya pada MCS-51, mikrokontroler ATMEL AT89S8252 memiliki tambahan SFR. Hal ini tak lain adalah karena adanya fitur tambahan pada mikrokontroler ATMEL AT89S8252.

SFR tambahan ini meliputi: T2CON(Timer 2 Register dengan alamat 0C8H), T2MOD(Timer 2 Mode dengan alamat 0C9H), WMCON(Watchdog and Memory Control Register dengan alamat 96H), SPCR(SPI Control Register dengan alamat D5H), SPSR(SPI Status Register dengan alamat AAH), SPDR(SPI Data Register dengan alamat 86H).

2.5.4. Data Memory (EEPROM) dan RAM

Berbeda dengan mikrokontroler standar MCS-51, mikrokontroler ATMEL AT89S8252 juga dilengkapi dengan data memori yang berupa EEPROM (*Electrically Erasable Programmable Read Only Memory*). EEPROM yang ditanamkan ini besarnya 2 Kbyte (2K) dan dipakai untuk penyimpanan data.

EEPROM ini diakses dengan mengeset bit EEMEN pada register WMCON pada alamat 96H. Alamat EEPROM ini adalah 000H sampai 7FFH. Instruksi *movx* digunakan untuk mengakses EEPROM *internal* ini. Namun jika ingin mengakses data memori luar (diluar mikrokontroler ATMEL AT89S8252) dengan menggunakan instruksi *movx* ini maka bit EEMEN harus dibuat "0".

Bit EEMWE pada register WMCON harus diset ke 1 sebelum sembarang lokasi pada EEPROM dapat ditulis. Program pengguna harus mereset bit EEMWE ke "0" jika proses penulisan ke EEPROM tidak diperlukan lagi. Proses penulisan pada EEPROM dapat dilihat dengan membaca bit RDY/BSY pada SFR WMCON. Jika bit ini berlogika rendah maka penulisan EEPROM sedang berlangsung, jika bit ini berlogika tinggi maka penulisan sudah selesai dan penulisan lain dapat dimulai lagi. Sedangkan RAM yang ada pada mikrokontroler ATMEL AT89S8252 adalah berkapasitas 256 *byte*. Penjelasan mengenai RAM ini adalah sama dengan RAM yang ada pada mikrokontroler standar MCS-51.

2.5.5. Programable Watchdog Timer (WDT)

Pada mikrokontroler ATMEL AT89S8252 juga dilengkapi oleh *watchdog Timer*. *Watchdog Timer* ini menggunakan detak tersendiri. Untuk mengatur rentang waktu (periode) pada WDT ini maka terdapat bit prescaler yang dapat mengatur rentang waktu yang dibutuhkan.

Bit prascaler ini adalah bit PS0, PS1 dan PS2 pada register WMCON. Periode waktu pada WDT ini berkisar dari 16 mili detik sampai 2048 mili detik. Karena bit prescalernya ada 3, maka akan ada 8 buah kemungkinan yaitu:

Tabel 2.1
Pemilihan Periode Waktu WDT

PS2	PS1	PS0	Periode
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

WDT dilumpuhkan oleh Power on Reset (POR) dan selama Power Down. WDT diaktifkan dengan menseting bit WDTEN pada SFR WMCON (alamat

96H). Jika perhitungan waktu WDI telah selesai tanpa ada reset atau dilumpuhkan, maka suatu pulsa reset internal akan dihasilkan untuk mereset CPU.

2.5.6. Timer 2

Pada mikrokontroler Atmel AT89S8252 terdapat tambahan *Timer 2*. *Timer* yang lain adalah *timer 0* dan *timer 1*. Hal yang perlu diperhatikan adalah *Timer/Counter* dapat digunakan sebagai generator *baudrate* untuk serial *port*. Pada standart MS-51 biasanya yang digunakan adalah *timer 1* sebagai penghasil *baudrate*. Pada mikrokontroler Atmel AT89S8252 selain menggunakan *timer 1* sebagai *baudrate* (untuk menjaga kompatibilitas dengan MCS-51) juga dapat menggunakan *Timer 2* sebagai penghasil *baudrate* untuk serial *port*. *Timer 2* ini merupakan *Timer/Counter* yang berukuran 16 bit yang dapat beroperasi sebagai timer atau dapat beroperasi sebagai penghitung kejadian dengan detak dari luar. Untuk mengatur fungsi ini dilakukan dengan mengatur bit C/T2 pada SFR T2CON. Terlihat bahwa jika bit ini tinggi maka akan terpilih fungsi *counter*, tapi jika bit ini rendah maka akan terpilih fungsi *Timer 2*.

Timer 2 ini memiliki 3 mode operasi yaitu: *capture*, *auto reload (up dan down counting)* dan *baud rate generator*. Untuk memilih mode ini dilakukan dengan mengatur bit pada SFR T2CON.

Timer 2 ini terdiri dari 2 buah *timer 8 bit register* yaitu TH2 dan TL2 dinaikkan tiap siklus mesin. Karena siklus mesin terdiri dari 1 *periode* osilasi, maka *count rate* menjadi 1/12 dari frekuensi osilator.

Pada fungsi *counter*, *register* dinaikkan berdasarkan tanggapan adanya transisi tinggi ke rendah pada pena yang bersesuaian (dalam hal ini pin T2 atau Pi.0). pada fungsi ini, masukan luar akan disampling selama S5P2 dari tiap siklus mesin. Jika hasil sampling menunjukkan logika tinggi pada selama satu siklus dan logika rendah pada siklus selanjutnya maka akan terdeteksi transisi tinggi ke rendah dan akibatnya perhitungan akan dinaikkan. Nilai perhitungan yang baru akan muncul pada register selama S3P1 dari siklus setelah transisi tinggi ke rendah terdeteksi.

Tabel 2.2
Tabel Mode Operasi Timer 2

RCLK+TCLK	CP/RL2	TR2	MODE
0	0	1	16 bit auto reload
0	1	1	16 bit capture
1	X	1	Baud rate generator
X	X	0	Off

2.6. ADC (ANALOG TO DECIMAL CONVERTER)

Data yang diambil dari output tegangan keluaran berbentuk analog, karena mikrokontroler hanya mengolah data digital maka tegangan tersebut harus dikonversikan kedalam bentuk digital dengan menggunakan ADC.

Dalam tugas akhir ini digunakan ADC tipe 0804 buatan NATIONAL SEMICONDUCTOR, dengan resolusi 8 bit.

IC ini memiliki suatu input sebagai input analog dan 8 bit output berupa digital, dengan kombinasi $2^8 = 256$ langkah pengaturan. Jika tegangan referensi yang kita set berada pada tegangan 5,12 volt atau $\frac{V_{ref}}{2} = 2,56$, maka step per tegangan yang dihasilkan adalah $\frac{5,12}{12} = 0,426$

Hal ini dimaksud agar jika tegangan maksimal yang masuk adalah 12 volt dan setelah melalui pembagi tegangan dengan ratio 0,426 maka dihasilkan tegangan 5,12 yang sesuai dengan tegangan referensi max, hal ini menyatakan bahwa step ADC sudah berada pada tingkat terakhir dalam konversi penuh.

Misalnya tegangan regulator yang keluar adalah 5 Volt maka setelah melalui pembagi tegangan, tegangan yang keluar adalah $5 \times 0,426 = 2,1333$ sebagai input ADC, atau konversi ADC berada pada tingkat

$$\text{ke } \frac{256}{2,1333} = 120,001875 \text{ (antara 120-121).}$$

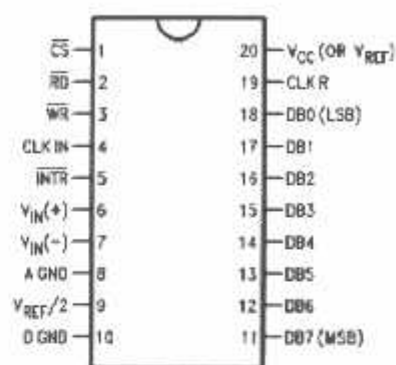
Pada IC ini telah terdapat rangkaian internal oscilator untuk mengaktifkan rangkaian konversinya.

Frekuensi osilator ditentukan oleh rangkaian external R dan C, pada rangkaian yang direncanakan frekuensi osilator adalah :

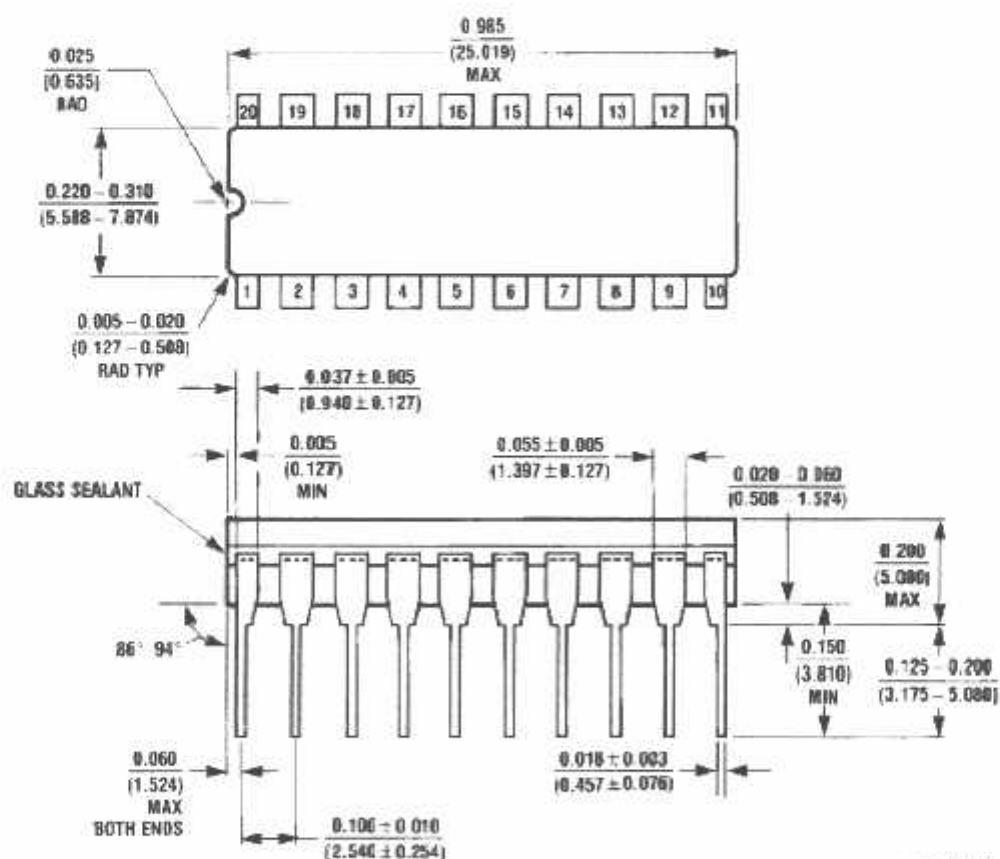
$$f = \frac{1}{1,1 \times R \times C}$$

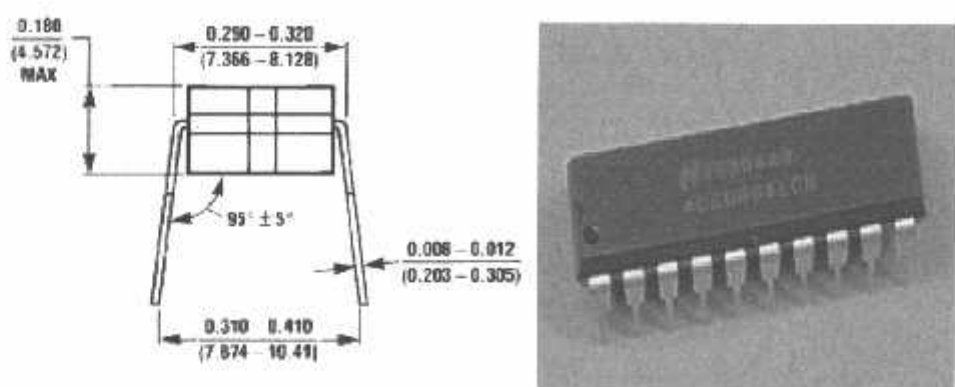
$$f = \frac{1}{1,1 \times 10^4 \times 150 \times 10^{-12}} = 600 \text{ Khz}$$

Frekuensi kerja rangkaian *switching* dengan maksud agar setiap besaran tegangan yang akan dibandingkan dapat diambil contohnya dengan cepat.



GAMBAR 2.14.
KONFIGURASI PIN ADC 0804





GAMBAR 2.16.
ADC 0804

2.7. LCD

Liquid Crystal Display atau LCD merupakan komponen optoelektronik yaitu komponen yang bekerja atau dipengaruhi oleh sinar (optolistrik), komponen pembangkit cahaya (*light emitting*) dan komponen-komponen yang akan mengubah sinar. LCD terbuat dari bahan kristal cair yang merupakan suatu komponen organik dan mempunyai sifat optik seperti benda padat meskipun bahan tetap cair.

Sel kristal cair terdiri dari selapis bahan kristal cair yang diapit antara dua kaca tipis yang transparan. Antara dua lembar kaca tersebut diberi bahan kristal cair (*liquid crystal*) yang tembus cahaya. Permukaan luar dari masing-masing keping kaca mempunyai lapisan penghantar tembus cahaya seperti oksida timah (*tin oxide*) atau oksida indium (*indium oxide*). Sel mempunyai ketebalan sekitar 1×10^{-5} meter dan diisi dengan kristal cair.

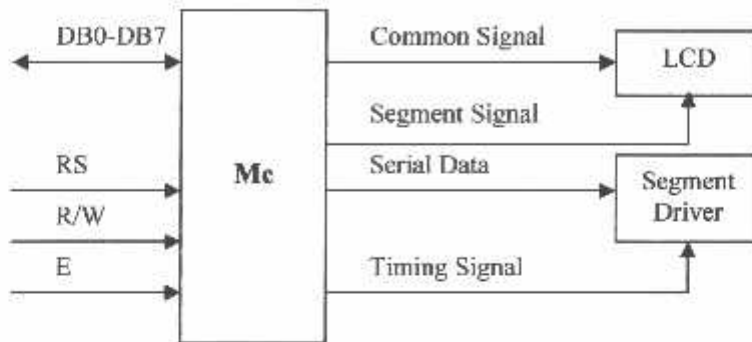
Karena sel-sel kristal cair merefleksikan cahaya dan bukan membangkitkan cahaya maka konsumsi daya yang dibutuhkan relatif rendah.

Energi yang dipergunakan hanya untuk mengaktifkan kristal cair. Pada dasarnya LCD bekerja pada tegangan rendah (3 – 15 Vrms), frekuensi rendah (25 – 60 Hz) sinyal AC dan memakai arus listrik yang sangat kecil (25 - 300 μ A). LCD seringkali ditata sebagai tampilan *seven segment* untuk menampilkan angka tetapi juga memiliki keistimewaan lain, yaitu kemampuan untuk menampilkan karakter dan berbagai macam simbol.

Salah satu jenis LCD diantaranya adalah LCD M1632, suatu jenis piranti dengan konsumsi daya yang rendah, disusun dari dot matrik dan dikontrol oleh ROM atau RAM generator karakter dan RAM data display. Pengontrolan utamanya adalah pada ROM generator dan display data RAM yang menghasilkan kode ASCII jika padanya diberikan *input* ASCII. Untuk dapat difungsikan dengan baik maka perlu diperhatikan proses analisis yang telah ditentukan oleh pabrik pembuatnya. Timing penganalisan sangat dipertimbangkan, karena jika meleset sampai ordo *milisecon* maka dapat dipastikan LCD tidak dapat berfungsi.

LCD Display Module M1632 buatan Seiko Instrument Inc. ini terdiri dari dua bagian, yang pertama merupakan panel LCD sebagai media penampil informasi dalam bentuk huruf/angka dua baris, masing-masing baris bisa menampung 16 huruf/angka. Bagian kedua merupakan sebuah sistem yang dibentuk dengan mikrokontroler yang ditempelkan dibalik pada panel LCD, berfungsi mengatur tampilan informasi serta berfungsi mengatur komunikasi M1632 dengan mikrokontroler yang memakai tampilan LCD itu. Dengan demikian pemakaian M1632 menjadi sederhana, sistem lain yang M1632 cukup

mengirimkan kode-kode ASCII dari informasi yang ditampilkan seperti layaknya memakai sebuah printer.



Gambar 2.16.

Blok Diagram LCD

Adapun karakteristik dari LCD M1632 antara lain :

- Dengan 16 karakter – 2 baris dalam bentuk dotmatrik 5x7 dan cursor
- *Duty ratio* 1/16
- Memiliki ROM pembangkitan karakter untuk 192 jenis karakter
- RAM untuk data display sebanyak 80x8 *bit*
- Dapat dirangkai dengan MPU 8 *bit*/4 *bit*
- RAM data display dan RAM pembangkit karakter dapat dibaca oleh MPU
- Memiliki fungsi instruksi antara lain *display on/off*, *Cursor on/off*, *display* karakter *blink*, *cursor shift* dan *display shift*
- Memiliki rangkaian osilator sendiri
- Catu tegangan tunggal yaitu $\pm 5\text{ V}$
- Memiliki rangkaian *reset* otomatis pada catu daya yang dihidupkan
- Temperatur operasi $0^{\circ} - 50^{\circ}$

LCD memiliki 16 pin, masing-masing memiliki fungsi sebagai berikut :

Tabel 2.3. Fungsi Tiap Pin LCD

No. Pin	Simbol	Level	Fungsi	
1	V _{SS}	-	Power Supply	0 V (GND)
2	V _{CC}	-		5 V ± 10%
3	V _{BE}	-		For LCD Drive
4	RS	H/L	Sinyal seleksi <i>register</i> H ; Data <i>Input</i> [<i>register data</i> (<i>write/read</i>)] L ; Instruction <i>Input</i> [<i>register instruksi</i> (<i>write</i>), <i>busy flag</i> dan <i>address counter</i> (<i>read</i>)]	
5	R/W	H/L	H ; <i>Read</i> L ; <i>Write</i>	
6	E	H	<i>Enable</i> Signal [sinyal penanda mulai operasi, aktif saat operasi <i>write</i> atau <i>read</i>]	
7	DB0	H/L	4 <i>bit</i> bus data <i>lower</i> 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L	4 <i>bit</i> bus data <i>upper</i> 2 arah, dapat dibaca atau ditulis terhadap mikrokontroler, DB7 juga sebagai <i>busy flag</i>	
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+BL	-	Back Light Supply	4 - 4,2 V 50 - 200 mA
16	V-BL	-		0 V (GND)

2.7.1. Instruksi Operasi

Tabel 2.4. Instruksi Pada LCD

Instruksi	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0						
Display Clear	0	0	0	0	0	0	0	0	0	1						
Cursor Home	0	0	0	0	0	0	0	0	1	*						
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S						
Display On/Off	0	0	0	0	0	0	1	D	C	B						
Cursor Display Shift	0	0	0	0	0	1	S/C	R/L	*	*						
Function Set	0	0	0	0	1	DL	1	*	*	*						
CG RAM Address Set	0	0	0	1	A _{CG}											
DD RAM Address Set	0	0	1	A _{DD}												
BF/Address Read	0	1	BF	AC												
Data Write to CG RAM	1	0	Write Data													
Data Read from CG RAM	1	1	Read Data													

*Invalid Bit

A_{CG} ; CG RAM Address dan A_{DD}

Pada LCD juga terdapat instruksi – instruksi sebagai berikut :

1. *Display clear*

Membersihkan tampilan yang ada pada LCD serta menyimpan, sedangkan kursor kembali ke posisi semula.

2. *Cursor home*

Hanya membersihkan tampilan dan kursor kembali ke semula.

3. *Empty Mode Set* : layar beraksi sebagai tampilan tulis.

S : 1/0 = menggeser layar.

1/0 : 1 = kursor bergerak ke kanan dan layar bergerak ke kiri.

1/0 : 0 = kursor bergerak ke kiri dan layar bergerak ke kanan

4. *Display On/Off Control.*

D : 1 – layar *on*

D : 0 = layar *off*

C : 1 = kursor *on*

C : 0 = kursor *off*

B : 1 = kursor berkedip-kedip

B : 0 = kursor tidak berkedip – kedip

5. *Cursor Display Shift*

S/C : 1 = LCD diidentifikasi sebagai layar

S/C : 0 = LCD diidentifikasi sebagai kursor

R/L : 1 = menggeser satu spasi ke kanan

R/L : 0 = menggeser satu spasi ke kiri

6. *Fuction Set*

DL : 1 = panjang data LCD pada 8 *bit*

DL : 0 = panjang data LCD pada 4 *bit*

Bit upper ditransfer terlebih dahulu kemudian diikuti dengan 4 *bit lower*.

N : 1/0 = LCD menggunakan 2 atau 1 baris karakter

P : 1/0 = LCD menggunakan 5 x 10 dot matrik

7. CG RAM *address set* : menulis alamat RAM ke karakter

8. DD RAM *address set* : menulis alamat RAM ke tampilan

9. BF/*address set* : BF = 1/0, LCD dalam keadaan sibuk atau tidak sibuk.

10. Data write to CG RAM or DD RAM : membaca *byte* dari alamat terakhir RAM yang dipilih.

2.7.2. Operasi Dasar

- *Register*

Kontrol dari LCD memiliki 2 buah *register* 8 *bit* yaitu *register* instruksi (IR) dan *register* data (DR). IR memiliki instruksi seperti display, *clear*, cursor shift dan display data (DD RAM) serta karakter (CG RAM). DR menyimpan data untuk ditulis ke DD RAM ataupun membaca data dari DD RAM dan CG RAM. Ketika data ditulis ke DD RAM atau CG RAM maka DR secara otomatis menulis data ke DD RAM atau CG RAM. Ketika data pada CG RAM atau DD RAM akan dibaca maka alamat data ditulis pada IR. Sedangkan data akan dimasukkan melalui DR sehingga dapat dibaca oleh mikrokontroler.

Tabel 2.5. Pemilihan Register Pada LCD

RS	RW	Operasi
0	0	Seleksi IR, IR <i>Write Display Clear</i>
0	1	<i>Busy Flag (DB7), @ Counter (DB0-DB7) Read</i>
1	0	Seleksi DR, DR <i>Write</i>
1	1	Seleksi DR, DR <i>Read</i>

- *Busy Flag*

Busy Flag menunjukkan bahwa modul siap untuk menerima instruksi selanjutnya sebagaimana terlihat pada tabel diatas. *Register* seleksi sinyal akan melalui DB7 jika RS=0 dan R/W=1. Jika bernilai 1 maka sedang melakukan kerja *internal* dan instruksi tidak akan dapat diterima, oleh karena itu status dari *flag* harus diperiksa sebelum melaksanakan instruksi selanjutnya.

- *Address Counter (AC)*

AC menunjukkan lokasi memori dalam modul LCD. Pemilihan lokasi alamat lewat Ac diberikan lewat *register* instruksi (IR) ketika data pada A, maka AC secara otomatis menaikkan atau menurunkan alamat tergantung dari *Entry Mode Set*.

- *Display Data RAM*

Pada LCD, masing-masing *line* memiliki *range* alamat tersendiri. Alamat itu diekspresikan dengan bilangan hexadesimal. Untuk *line 1 range* alamat berkisar antara 40_H-4F_H.

- Character Generator ROM (CG ROM)

CG ROM memiliki tipe dot matrik 5x7, dimana pada LCD telah tersedian ROM sebagai pembangkit karakter dalam kode ASCII.

- Character Generator RAM (CG RAM)

CG RAM dipakai untuk pembuatan karakter tersendiri melalui program.

Adapun bentuk fisik dari LCD M1632 adalah pada gambar berikut :

2.7.3. Sinyal *Interface* M1632

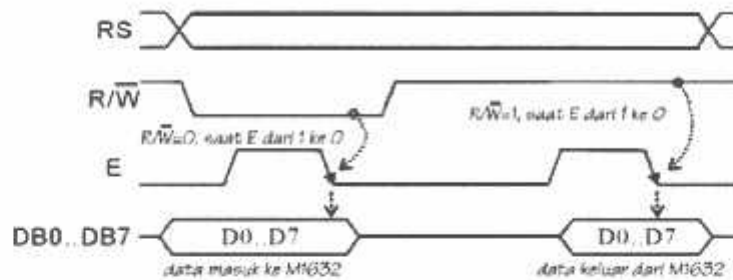
Untuk berhubungan dengan mikrokontroler pemakai, M1632 dilengkapi dengan 8 jalur data (DB0 - DB7) yang dipakai untuk menyalurkan kode ASCII maupun perintah pengatur kerjanya M1632. Selain itu dilengkapi pula dengan E, R/W dan RS seperti layaknya komponen yang kompatibel dengan mikroprosesor.

Kombinasi lainnya E dan $\overline{R/W}$ merupakan sinyal standar pada komponen buatan Motorola. Sebaliknya sinyal-sinyal dari MCS51 merupakan sinyal khas Intel dengan kombinasi sinyal WR dan RD.

RS, singkatan dari *Register Select*, dipakai untuk membedakan jenis data yang dikirim ke M1632, kalau RS=0 data yang dikirim adalah perintah untuk mengatur kerja M1632, sebaliknya kalau RS=1 data yang dikirim adalah kode ASCII yang ditampilkan.

Demikian pula saat pengambilan data, saat RS=0 data yang diambil dari M1632 merupakan data status yang mewakili aktivitas M1632, dan saat RS=1 maka data yang diambil merupakan kode ASCII dari data yang ditampilkan.

Proses mengirim/mengambil data ke/dari M1632 bisa dijabarkan sebagai berikut :



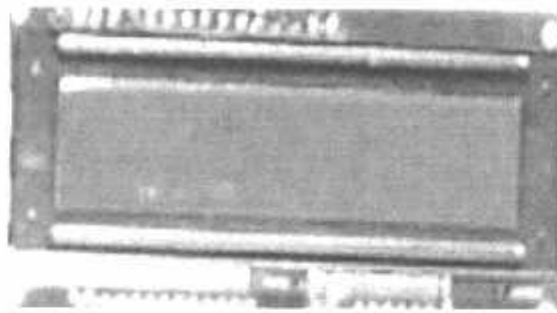
Gambar 2.17.

Mengirim/Mengambil Data Ke/Dari M1632

1. RS harus dipersiapkan dulu, untuk menentukan jenis data seperti yang telah dibicarakan di atas.
2. $\overline{R/W}$ di-nol-kan untuk menandakan akan diadakan pengiriman data ke M1632. Data yang akan dikirim disiapkan di DB0..DB7, sesaat kemudian sinyal E di-satu-kan dan di-nol-kan kembali. Sinyal E merupakan sinyal sinkronisasi, saat E berubah dari 1 menjadi 0 data di DB0 .. DB7 diterima oleh M1632.

Untuk mengambil data dari M1632 sinyal $\overline{R/W}$ di-satu-kan, menyusul sinyal E di-satu-kan. Pada suatu E menjadi 1, M1632 akan meletakkan datanya di DB0 .. DB7, data ini harus diambil sebelum sinyal E di-nol-kan kembali.

Liquid crystal display yang digunakan adalah *Display Module M1632*.



Gambar 2.18.

Liquid Crystal Display

2.8. Papan Tombol (*keypad*)

Keypad sering digunakan sebagai media masukan dalam berbagai aplikasi elektronik. Seperti yang sudah dijelaskan pada sub bab sebelumnya bahwa *keypad* ini bekerja dengan metode matrik dimana keluaran yang dihasilkan merupakan kombinasi dari baris dan kolom dari tombol yang ditekan.

Pada bagian belakang dari *keypad* 4x4 terdapat delapan buah pin yang berfungsi sebagai keluaran dari *keypad* tersebut. Delapan buah pin ini terdiri dari 4 buah pin yang menunjukkan kolom dari tombol yang ditekan dan 4 buah pin terhubung ke *resistor pull up* menunjukkan baris dari tombol yang ditekan.

Masalah-masalah yang sering timbul dengan digunakannya *keypad* jenis ini adalah dengan adanya bouncing. Dengan adanya bouncing maka tombol yang ditekan sekali. Akan terdeteksi berulang kali. *Bouncing* ini dapat diatasi dalam pemrograman dengan memberikan jeda waktu atau delay beberapa saat sebelum

data benar-benar dimasukkan ke dalam mikrokontroler untuk diolah. Tujuan pemberian jeda waktu ini untuk memberi kesempatan agar benar-benar terjadi kontak antar ujung baris dan kolom dari tombol yang ditekan dengan resistor pull up.

Prosedur untuk pembacaan *keypad* dilakukan dengan teknik compare atau membandingkan data. Data yang dimasukkan melalui *keypad* dibandingkan dengan data yang tersimpan di dalam mikrokontroler. Apabila ada yang sesuai maka mikrokontroler akan melakukan instruksi sesuai dengan data yang dimasukkan dari *keypad*. Data yang sah, yang akan diolah oleh mikrokontroler adalah data yang diambil setelah diadakan pemanggilan sub program *delay* untuk mengatasi bouncing. Data tersebut kemudian dibandingkan dengan data yang ada di mikrokontroler dan apabila ada yang sesuai maka mikrokontroler akan memproses data tersebut. Apabila data pada akumulator tidak ada yang sesuai dengan data pada mikrokontroler maka akan diulang kembali proses pemasukan data dari *port 1* ke akumulator.

BAB III.

PERANCANGAN DAN PEMBUATAN

3.1. PENDAHULUAN

Untuk membuat dan merencanakan sebuah *power supply jenis switching*, kita harus menentukan sistim dan metoda apa yang akan kita pakai pada rangkaian inverternya.

Dalam skripsi ini digunakan metoda *flyback* untuk rangkaian *inverter*, karena kesederhanaan rangkaian (tanpa filter output dan lilitan clamp) namun dapat diandalkan dan konfigurasi pengaturan (sebagai penjaga kestabilan) dipakai type PULSE WIDTH MODULATION dimana lebar pulsa yang kita atur, sedangkan frekuensi tetap dipertahankan.

Rangkaian minimum sistem disini digunakan sebagai otak kendali pengaturan lebar pulsa (PWM) agar diperoleh kestabilan tegangan yang tinggi, input keypad, lcd tegangan, dan elemen memori dari contoh tegangan yang dapat dipanggil setiap waktu dengan cepat.

Rangkaian rectifier dan filter untuk meratakan dan memperkecil kerut-kerut tegangan agar diperoleh tegangan output yang diharapkan mendekati tegangan DC murni.

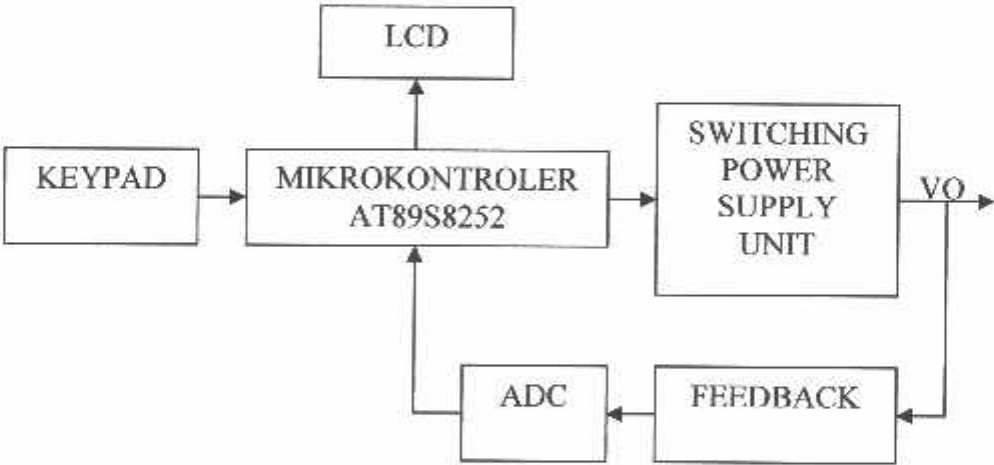
Output dapat beroperasi pada frekuensi tinggi dibutuhkan komponen-komponen pilihan terutama pada masalah trafo *switching*. Inti trafo ini dibuat dari bahan ferit yang didesain khusus dimana bahan tersebut memiliki sifat remanensi yang dapat dengan cepat dipulihkan atau dengan kata lain sifat inti trafo sewaktu

diimbaskan dan berubah menjadi magnet harus secepat mungkin bisa dihilangkan karena sentakan pulsa switching yang berikutnya sudah harus bebas dari sisa-sisa magnet yang sebelumnya.

Transistor-transistor pada output stage dan semi konduktor penunjang lainnya juga dipilih dari jenis high speed.

3.2. Blok Diagram

Blok diagram dari “: Perencanaan dan pembuatan *Programmable switching Power supply* 0 – 15 volt, arus maksimal 2 Ampere dengan menggunakan mikrokontroler AT89S8252 “ ditunjukkan dalam gambar berikut:



GAMBAR 3.1.
BLOK DIAGRAM

Keterangan dari blok diagram alat:

1. KEYPAD 4 x 4

Digunakan untuk memberikan inputan yang nantinya akan diproses lebih lanjut.

2. SWITCHING POWER SUPPLY UNIT

Merupakan rangkaian utama dari keseluruhan rangkaian yang ada. Rangkaian ini berfungsi sebagai penyuplai daya yang bekerja dengan metode *switching power supply*.

3. FEEDBACK

Digunakan sebagai umpan balik tegangan yang didapat dari tegangan output (VO) power supply.

4. ADC (analog to digital converter)

Digunakan sebagai pengkonversi tegangan analog ke digital yang diumpankan rangkaian *feedback*.

3.3. Prinsip Kerja Rangkaian

Untuk variasi tegangan sesuai dengan yang diminta oleh keypad. Untuk variasi tegangan, VO akan disample oleh rangkaian feedback dan dikonversikan didalam ADC, kemudian dibandingkan didalam mikrokontroler. Jika output dari rangkaian masih dibawah tegangan yang diminta, maka mikrokontroler akan menambah lebar pulsa dan dibandingkan terus menerus, sampai pada saat diperoleh tegangan yang sangat dekat dengan tegangan yang diminta.

Output dari mikrokontroler ini mengeluarkan pulsa yang akan mengontrol base dari rangkaian *switching Power Supply* dengan durasi transfer energi didalam power supply diubah ke posisi yang sesuai dengan tegangan yang diminta.

3.4. RANGKAIAN DASAR CATU DAYA JENIS SWITCHING

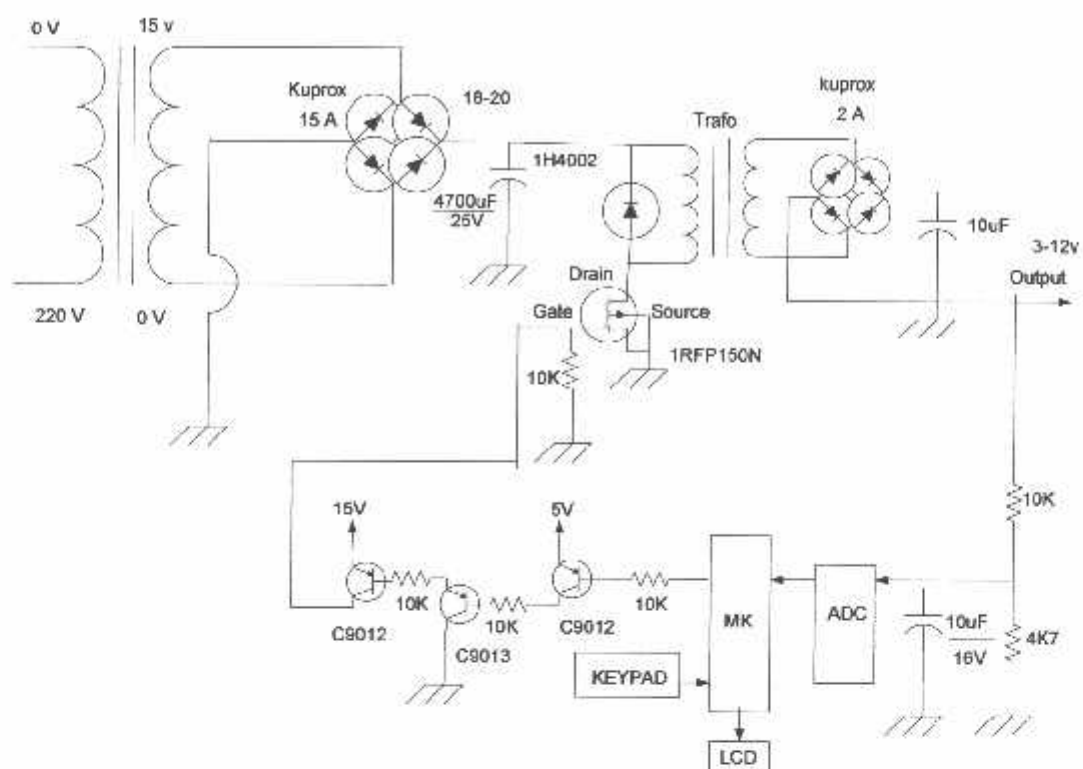
Rangkaian dasar terdiri dari empat blok yang terbagi atas :

1. Penyearah input dan filter input.

Tegangan diambil langsung dari jala-jala secara langsung dengan maksud agar menghindari pemakaian trafo frekuensi rendah (50 Hz). Tegangan yang masuk difilter kemudian disaraskan secara gelombang penuh.

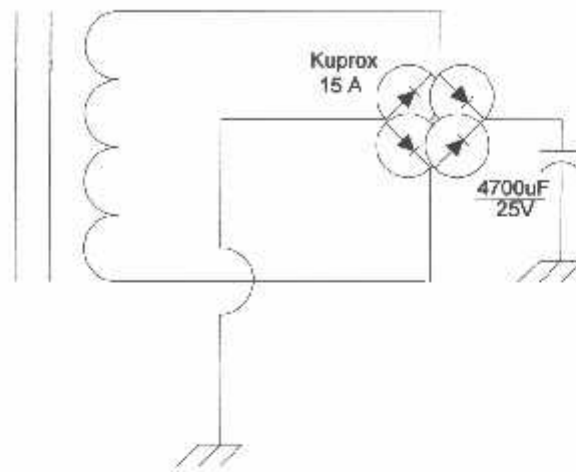
2. High frekuensi Inverter.

Tegangan DC yang telah disaraskan kemudian diumpan pada Inverter yang dikendalikan oleh rangkaian kontrol PWM sehingga transfer energinya sesuai dengan kebutuhan yang diminta.

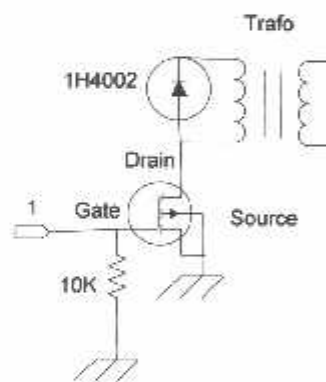


GAMBAR 3.2.

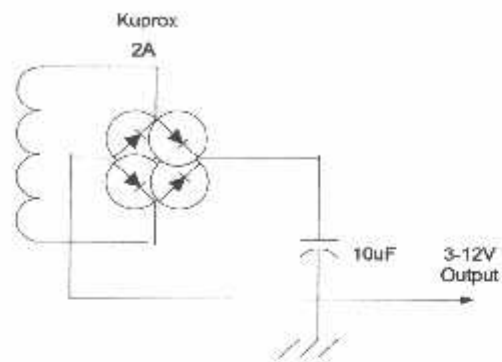
RANGKAIAN DASAR CATU DAYA JENIS SWITCHING



GAMBAR 3.3.
RANGKAIAN RECTIFIER & FILTER.



GAMBAR 3.4.
RANGKAIAN HIGH FREKUENSI INVERTER.



GAMBAR 3.5.
RANGKAIAN PENYEARAH

3. Penyearah output dan filter output.

Keluaran sisi sekunder dari Trafo konverter frekwensi tinggi ini kemudian disearahkan dan difilter untuk mendapatkan level DC yang baik.

4. Kontrol Unit.

Mikrokontroler sebagai otak dari sistem

3.5. CARA MENDAPATKAN LEBAR PULSA VARIABEL

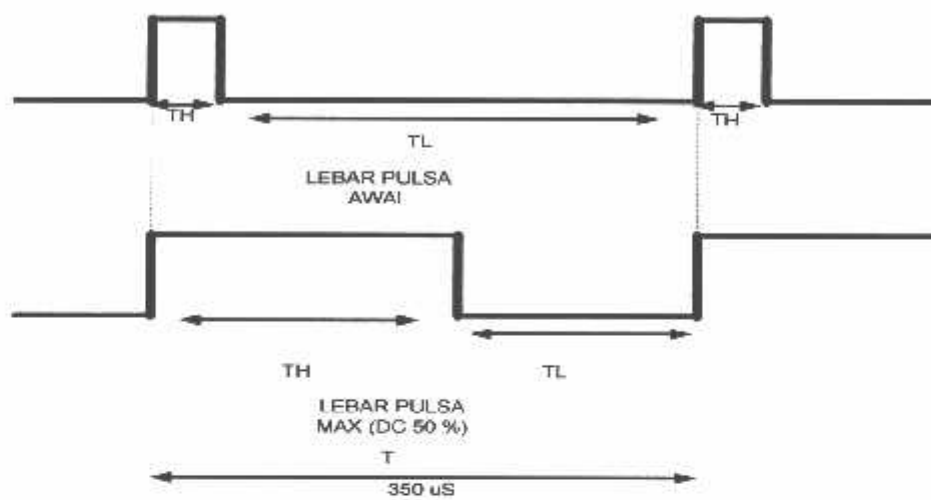
Diatas telah disinggung cara kerja dari rangkaian kontrol yang dapat mengendalikan lebar pulsa variabel secara analog, tetapi dalam tugas akhir ini pembangkit lebar pulsa dilakukan bukan oleh komponen analog melainkan dibangkitkan oleh minimum sistem.

Hal ini dilakukan dengan alasan :

1. Tidak perlu lagi membuat tegangan referensi dan osilator, karena output dari “PWM digital” sudah berlevel digital dan siap untuk mengatur waktu konduksi transistor *switching* menjadi dua keadaan.
2. Frekuensi kerja dari minimum sistem jauh lebih tinggi dari pada frekuensi kerja rangkaian *switching*, sehingga pelepasan pulsa *switch* dapat diatur dengan cepat.
3. Untuk membias transistor *switching* disini hanya dibutuhkan dua kejadian saja yaitu sifat saturasi (short) dan cut off (open) atau sebagai saklar. Dua level ini adalah identik dengan level kerja rangkaian digital. Proses pembangkitan pulsa *switch* pertama-tama yang dikeluarkan PWM adalah pulsa yang paling sempit, kemudian dimasukkan ke rangkaian konverter untuk diubah menjadi suatu level tegangan. Karena pulsa yang sempit ini menghasilkan periode “on” transistor yang sangat singkat, sehingga transfer daya pada trafo juga sedikit dan tegangan yang dihasilkan juga sangat kecil, pada saat itu juga ADC disiapkan untuk mendeteksi output dari regulator.

Output ADC setelah mengkonversi tegangan yang diterima sudah berupa level digital yang proporsional dengan besaran tegangan dan langsung diumpan pada mikrokontroler dan didalam mikrokontroler terjadi proses perbandingan dengan tegangan set yang diminta.

Jika pada suatu saat output *switching* kita bebani dengan beban yang lebih besar (tetapi tidak lebih besar dari kemampuan *switching*nya), maka tegangannya pasti turun. Gejala ini dapat dirasakan oleh mikrokontroler segera ia memerintahkan untuk menambah lebar pulsa sehingga kestabilan tetap terjaga.

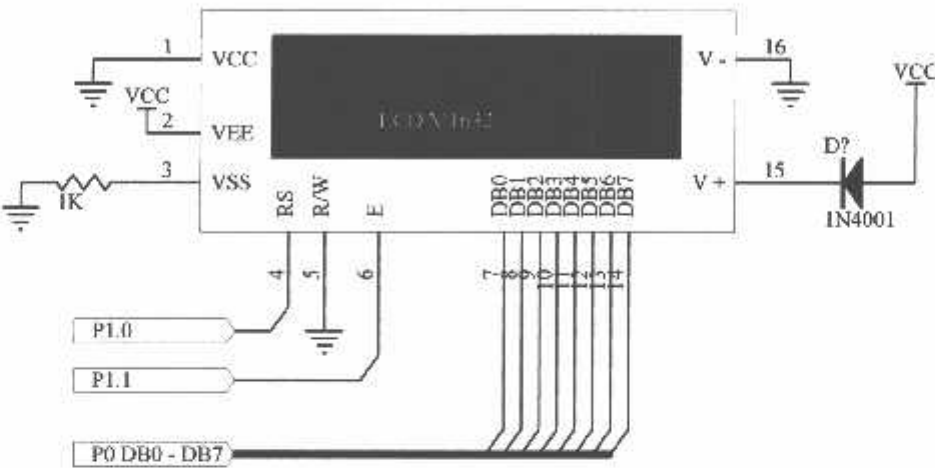


$$\text{Duty cycle } D = \frac{On}{T_{On} + t_{Off}} * 100 \%$$

GAMBAR 3.5.
LEBAR PULSA VARIABEL

3.6. LCD

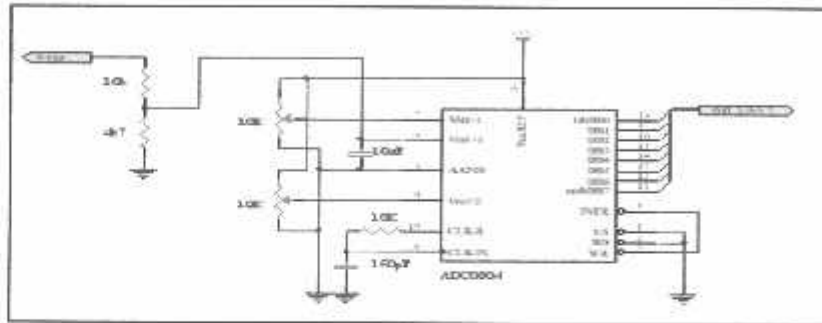
Liquid crystal Display yang digunakan adalah Display Module M1632.



GAMBAR 3.6.
RANGKAIAN LIQUID CRYSTAL DISPLAY

3.7. ADC

ADC yang digunakan adalah ADC 0804.

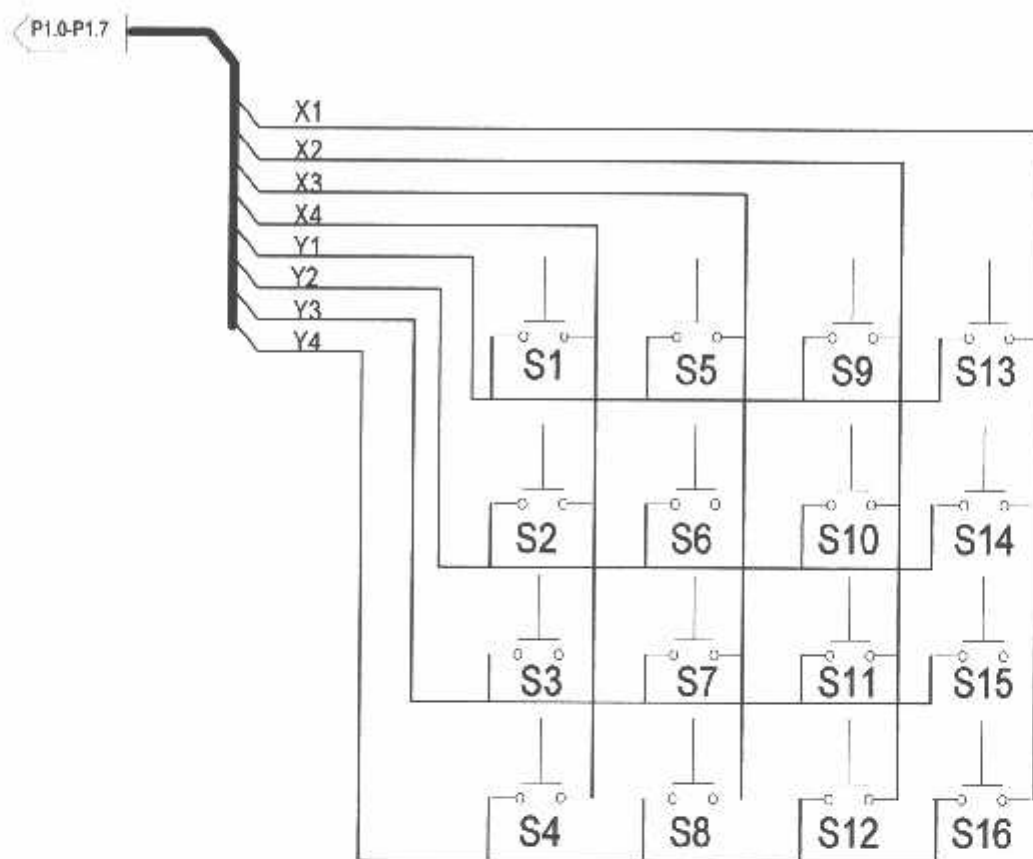


GAMBAR 3.7.
RANGKAIAN ADC 0804

3.8. Keypad

Keypad yang digunakan sebagai media masukan dalam berbagai aplikasi elektronik. Seperti yang sudah dijelaskan pada sub bab sebelumnya bahwa *keypad* ini bekerja dengan metode matrik dimana keluaran yang dihasilkan merupakan kombinasi dari baris dan kolom dari tombol yang ditekan.

Pada bagian belakang dari *keypad* 4x4 terdapat delapan buah pin yang berfungsi sebagai keluaran dari *keypad* tersebut. Delapan buah pin ini terdiri dari 4 buah pin yang menunjukkan kolom dari tombol yang ditekan dan 4 buah pin terhubung ke *resistor pull up* menunjukkan baris dari tombol yang ditekan.



GAMBAR 3.8.
RANGKAIAN KEYPAD

3.9. PERENCANAAN PERANGKAT LUNAK

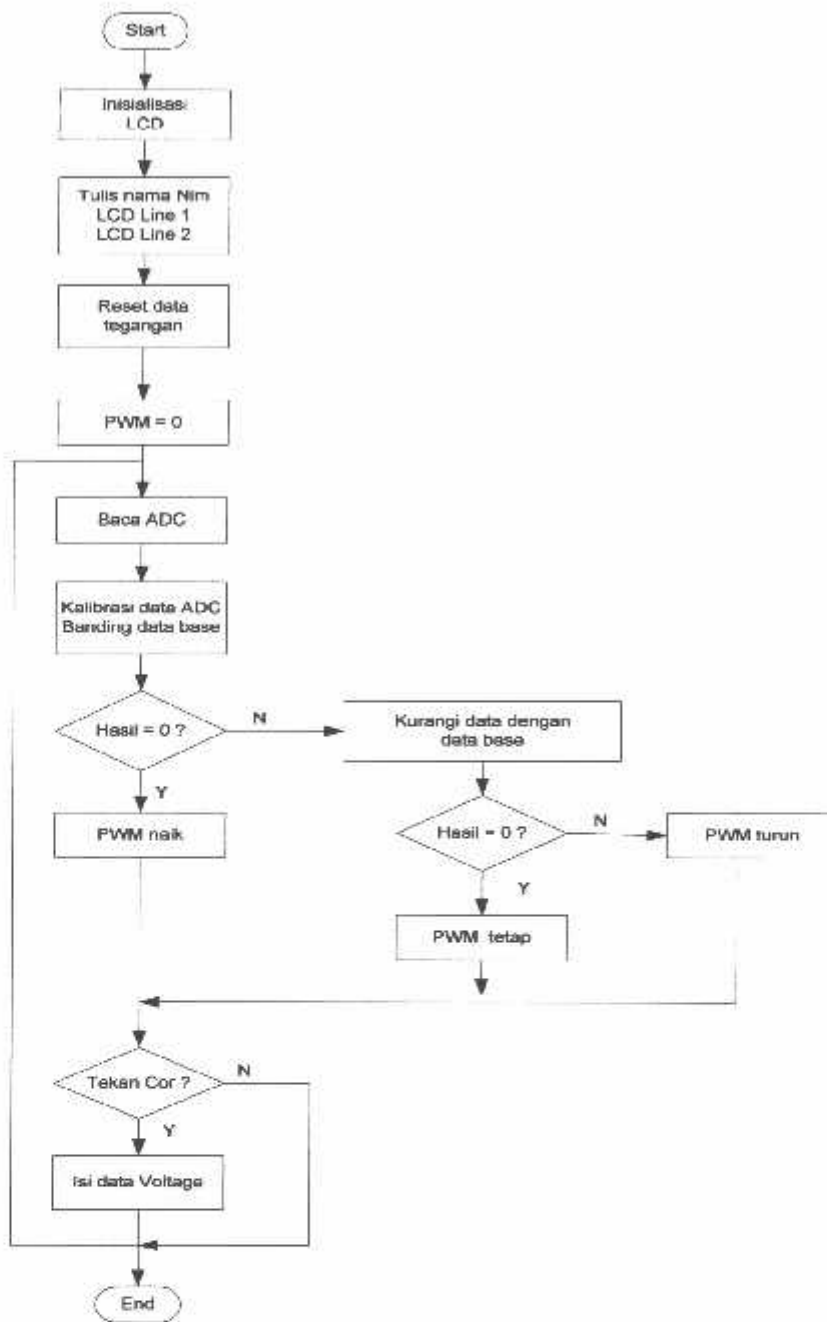
Perangkat lunak didalam pembuatan programmable switching power supply ini digunakan untuk mengendalikan seluruh kerja dari peralatan ini.

Perangkat lunak dibuat dalam bentuk naskah yang kemudian dikompile kedalam bahasa assembly 89S8252 yang dapat dimengerti oleh minimum sistem 89S8252.

Perangkat lunak yang bekerja pada minimum sistem 89S8252 secara garis besar dapat dibagi menjadi 2 bagian, yaitu :

- Program konversi keypad.
- Program pembuat, pembanding lebar pulsa.

Keseluruhan perangkat lunak pada minimum sistem ini menggunakan sistem polling yaitu keseluruhan instruksi itu dilakukan selama satu instruksi dijalankan, ini dimungkinkan karena keseluruhan sistem pada peralatan tersebut tidak membutuhkan kerja yang bersamaan, karena peralatan sendiri bersifat menunggu dan secara singkat dapat dikatakan bahwa peralatan ini tidak membutuhkan kecepatan kerja pada tombol operasinya (keypad).



GAMBAR 3.9.
DIAGRAM ALIR MINIMUM SISTEM

CARA KERJA

- Ketika Pertama kali dinyalakan, mikrokontroler tidak memberikan pulsa kepada driver (PWM), maka tidak ada tegangan yang keluar dari trafo switching.
- Ketika user memberikan data Voltage yang diinginkan maka mikrokontroler akan membandingkan data dari ADC (yang berasal dari trafo) dengan data base (data voltage ke ADC = $\frac{5V}{255} = 0,02 \text{ V/data}$). Jika data dari ADC lebih kecil dari data Voltage yang diinginkan maka mikrokontroler akan menaikkan data PWM, kemudian cek ulang dari membaca ADC & membandingkannya lagi ketika data dari ADC $\geq$ maka mikrokonroler akan menjaga data pada PWM pada nilai tersebut atau menurunkannya.

BAB IV

PENGUJIAN ALAT

4.1. PENGUJIAN SWITCHING POWER SUPPLY

Pengujian *switching power supply* yang memanfaatkan lebar pulsa variabel dari minimum sistem 89S8252 dilakukan dengan :

- * Percobaan awal modul switching.

Dengan menggunakan simulasi lebar pulsa variabel yang dibangkitkan oleh FUNCTION GENERATOR yaitu frekuensi yang bisa diatur dalam mode output gelombang persegi (square) yang diumpan pada basis transistor switching

Jika sudah didapatkan harga tegangan output yang tergantung dari variasi frekuensi (sama dengan variasi periode), berarti rangkaian tersebut sudah siap digabungkan dengan minimum sistem.

4.2. PENGUJIAN MINIMUM SISTEM

Pengujian dalam sistem ini dilakukan untuk mengetahui apakah rangkaian minimum sistem dan perangkat lunak yang disisikan ke dalam EPROM sudah bekerja dengan benar. Pengujian juga dilakukan dengan mengoperasikan peralatan melalui tombol operasi (keypad). Oleh karena itu pengujian minimum sistem ini dapat dilakukan dengan melihat hasil yang diperoleh seperti led pada 7 matrix, lebar pulsa yang keluar pada kaki output sesuai dengan program.

4.3. PENGUJIAN GABUNGAN

1). Melihat lebar pulsa awal yang dibangkitkan oleh rangkaian mikrokontroler.

Tegangan output diamati oleh bermacam-macam seting sambil melihat perubahan lebar pulsayng nampak pada layar osciloscop, kemudian output dibebani, juga sambil melihat ouput lebar pulsa tersebut pada outout kaki mikro.

2). Pengujian besaran arus input switching, tegangan input, tegangan output, arus output, ripple output (pada beban 330 Ω resistor $\frac{1}{2}$ W karbon murni) kemudian ditabelkan.

4.4. Hasil Pengujian

TABEL 4.1.
HASIL PENGUJIAN

V Set	V Out	Error (%)
0,5	0,54	8
1	1,02	2
1,5	1,55	3,33333333
2	2,06	3
2,5	2,52	0,8
3	3,03	1
3,5	3,56	1,71428571
4	4,01	0,25
4,5	4,52	0,44444444
5	5,15	3
5,5	5,52	0,36363636
6	6,02	0,33333333
6,5	6,51	0,15384615
7	7,02	0,28571429
7,5	7,54	0,53333333
8	8,03	0,375
8,5	8,57	0,82352941
9	9,05	0,55555556
9,5	9,54	0,42105263
10	10,11	1,1
10,5	10,58	0,76190476
11	11,04	0,36363636
11,5	11,54	0,34782609
12	12,22	1,83333333
12,5	12,62	0,96
13	13,23	1,76923077
13,5	13,51	0,07407407
14	14,25	1,78571429
14,5	14,6	0,68965517
15	15,25	1,66666667

38,7391061

4.5 Analisa Data

$$\text{Error (\%)} = \frac{\text{SelisihTegangan}}{V_{\text{Set}}} * 100 \%$$

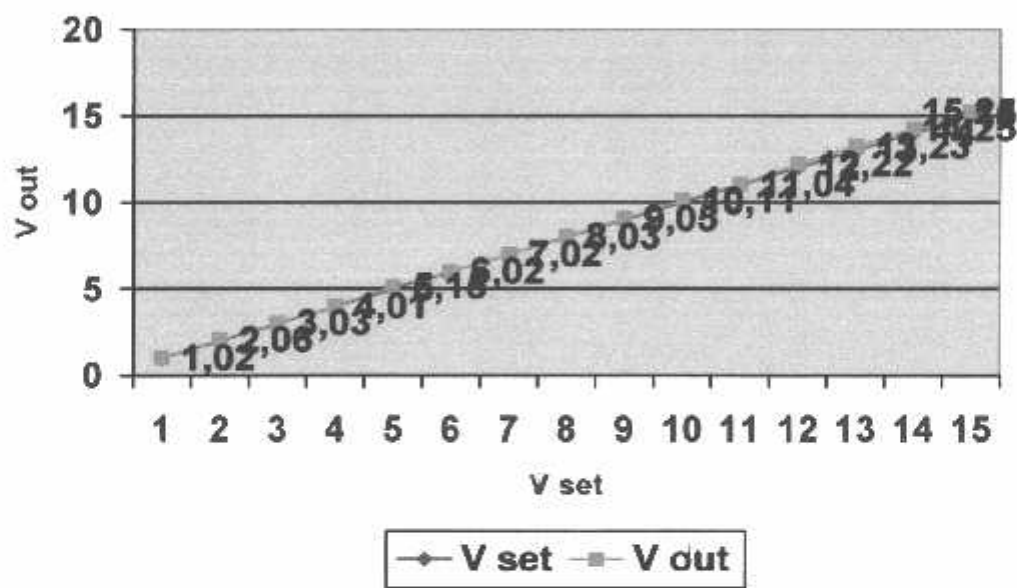
$$\text{Error Rata-Rata (\%)} = \frac{\sum \text{Error}}{\sum \text{Data}}$$

$$= \frac{38,73}{30}$$

$$=1,29 \%$$

4.6. Gambar Grafik

Di bawah ini tegangan output dan tegangan set dibuat grafik hasilnya akan membentuk garis linier.



Gambar 4.1.
Grafik V_o dan V_{set}

BAB V

PENUTUP

5.1. KESIMPULAN

1. Programmable switching power supply adalah suatu peralatan penunjang setiap kegiatan elektronika yang sangat penting apalagi jika dipakai pada keadaan yang sangat cepat tanpa perlu lagi mengeset tegangan yang hendak diminta.
2. Penggunaan lebar pulsa variabel (PWM) yang dibangkitkan atau dikontrol oleh mikrokontroler ternyata dapat memberikan hasil regulasi/pengaturan tegangan yang baik.
3. Trafo switching yang tersedia dipasaran hanya memiliki kemampuan 2 Ampere.
4. Output dapat diatur sesuai dengan keinginan kita yang dapat beroperasi pada frekuensi tinggi antara 1-100 KHz dengan pengaturan tegangan yang baik dan bernilai error 1,29 %.

5.2. SARAN

1. Melihat kemungkinan arus yang timbul tidak sesuai yang diharapkan maka sebaiknya desain dan karakter trafo juga perlu diperhitungkan.
2. Untuk daya switching ratusan watt (misalnya computer) harus diberi extra fan untuk menghindari.

DAFTAR PUSTAKA

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2. Wasito S, "Vademekum Elektronika Edisi Kedua" PT. Gramedia Pustaka Utama, Jakarta, 2006
3. Fu Keung, "High Frequency Transformer For Switching Mode Power Supplies" B. Eng and M. Phill, School Of Microelectronic Engineering Faculty Of Engineering an Information Technology Griffith University, Brisbane Australia, March 2004.
4. WWW.Atmel.Com
5. WWW.National.Com

LAMPIRAN

```

org 0h
;
Puls      Bit P2.0
Rest      Bit P2.6
Erb1      Bit P2.7
Stts      Bit 20h.0
Dfrk      Equ 30h          ; data frekwensi
Dkp0      Equ 31h          ; data masukan keypad 0
Dkp1      Equ 32h          ; data masukan keypad 1
Dkp2      Equ 33h          ; data masukan keypad 2
Dvin      Equ 34h          ; data volt input
Dvot      Equ 35h          ; data volt output
Dbf0      Equ 36h          ; data buffer 0
Dbf1      Equ 37h          ; data buffer 1
Hurf      Equ 40h
Dly0      Equ 41h
Dly1      Equ 42h
Dly2      Equ 43h
;
init:      acall  lcd_in
           clr    Stts
           mov    Dfrk,#50
;
mulai:      mov    DPTR,#nama
           acall  line1
           mov    Hurf,#16
           acall  tulis
           acall  line2
           mov    Hurf,#16
           acall  tulis
           acall  delay1
           mov    DPTR,#univ
           acall  line1
           mov    Hurf,#16
           acall  tulis
           acall  line2
           mov    Hurf,#16
           acall  tulis
           acall  delay1
           sjmp   mulai
;
seting:     mov    DPTR,#mskvl1
           acall  line1
           mov    Hurf,#16
           acall  tulis
           acall  line2
           mov    Hurf,#16
           acall  tulis
           mov    P0,#0C5h
           acall  w_ins
           mov    DPTR,#angka
           acall  tg_tkn
           mov    Lkp0,R0
           mov    A,R0
           acall  wr_chr
           acall  tg_lps

```

```

        acall    tg_tkn
        mov     Dkp1,R0
        mov     A,R0
        acall    wr_chr
        acall    tg_lps
        mov     P0,'#.'
        acall    w_chr
        acall    tg_tkn
        mov     Dkp2,R0
        mov     A,R0
        acall    wr_chr
        acall    tg_lps
        mov     DPTR,#dtabnr
        acall    line1
        mov     Hurf,#16
        acall    tulis
bole00: acall    senkpd
        cjne    R0,#11,bole01
        mov     SP,#07h
        ljmp    mulai
bole01: cjne    R0,#12,bole00
        mov     DPTR,#vltout
        acall    line1
        mov     Hurf,#16
        acall    tulis
        mov     A,Dkp0
        mov     B,#100
        mul     AB
        mov     Dbf0,A
        mov     A,Dkp1
        mov     B,#10
        mul     AB
        mov     B,Dkp2
        add     A,B
        mov     B,Dbf0
        add     A,B
        mov     Dvin,A
        acall    tg_lps
        seth    Stts
        mov     Dfrk,#50          ; set awal frek
        mov     DPTR,#lookup
/
output: mov     A,P3
        movc    A,@A+DPTR
        mov     Dvot,A
        mov     B,Dvin
        div     AB
outpt0: cjne    A,#0,outpt1
        dec     Dfrk
        sjmp    outpt4
outpt1: clr     C
        mov     A,Dvot
        mov     B,Dvin
        subb    A,B
outpt2: cjne    A,#C,outpt3
        sjmp    outpt4

```

```

outpt3: inc      Dfrk
outpt4: acall    delays
;
bole02: acall    scnkpdc
        cjne     R0,#11,output
        clr      Stts
        mov      SP,#07h
        ljmp     mulai
;
dt_adc: mov      DPTR,#bcaadc
        acall    line1
        mov      Hurf,#16
        acall    tulis
        mov      DPTR,#dtaadc
        acall    line2
        mov      Hurf,#12
        acall    tulis
        mov      DPTR,#angka
        acall    bc_adc
        mov      A,R1
        acall    wr_chr
        mov      A,R2
        acall    wr_chr
        mov      A,R3
        acall    wr_chr
        mov      A,#10
        acall    wr_chr
        acall    tg_lps
        acall    delays
bole03: acall    scnkpdc
        cjne     R0,#11,dt_adc
        mov      SP,#07h
        ljmp     mulai
;
bc_adc: mov      A,P3
cacah:  mov      B,#100
        div      AB
        mov      R1,A
        mov      A,B
        mov      B,#10
        div      AB
        mov      R2,A
        mov      R3,B
hps0:   cjne     R1,#0,hps1
        mov      R1,#10
tps1:   cjne     R2,#0,hps2
        cjne     R1,#10,hps2
        mov      R2,#10
hps2:   ret
;
line1:  mov      PC,#80h
        acall    w_ins
        ret
;
line2:  mov      PC,#0C0h
        acall    w_ins

```

```

        ret
;
tulis:  clr      A
        movc     A,@A+DPTR
        mov      P0,A
        acall    w_chr
        inc      DPTR
        djnz     Hurf,tulis
        ret
;
wr_chr: movc     A,@A+DPTR
        mov      P0,A
        acall    w_chr
        ret
;
w_ins:  clr      Enbl
        clr      Rest
        setb     Enbl
        clr      Enbl
        acall    jeda
        ret
;
w_chr:  clr      Enbl
        setb     Rest
        setb     Enbl
        clr      Enbl
        acall    jeda
        ret
;
lcd_in: acall    delays
        mov      PC,#C1h          ; Display Clear
        acall    w_ins
        mov      PC,#38h          ; Function Set
        acall    w_ins
        mov      P0,#0Dh          ; Display On, Cursor, Blink
        acall    w_ins
        mov      P0,#06h          ; Entry Mode
        acall    w_ins
        mov      P0,#02h          ; Cursor Home
        acall    w_ins
        acall    delays
        ret
;
senkpd: mov      R0,#10
        icall    jeda
coll:   mov      P1,#11111110b
        mov      A,P1
clb1:   cjne     A,#11101110b,clb2
        mov      R0,#1
clb2:   cjne     A,#11011110b,clb3
        mov      R0,#2
clb3:   cjne     A,#10111110b,clb4
        mov      R0,#3
clb4:   cjne     A,#01111110b,col2
        mov      R0,#13
;

```

```

col2:  mov    P1,#11111101b
       mov    A,P1
c2b1:  cjne   A,#11101101b,c2b2
       mov    R0,#4
c2b2:  cjne   A,#11011101b,c2b3
       mov    R0,#5
c2b3:  cjne   A,#10111101b,c2b4
       mov    R0,#6
c2b4:  cjne   A,#01111101b,col3
       mov    R0,#14
;
col3:  mov    P1,#11111011b
       mov    A,P1
c3b1:  cjne   A,#11101011b,c3b2
       mov    R0,#7
c3b2:  cjne   A,#11011011b,c3b3
       mov    R0,#8
c3b3:  cjne   A,#10111011b,c3b4
       mov    R0,#9
c3b4:  cjne   A,#01111011b,col4
       mov    R0,#15
;
col4:  mov    P1,#11110111b
       mov    A,P1
c4b1:  cjne   A,#11100111b,c4b2
       mov    R0,#11
c4b2:  cjne   A,#11010111b,c4b3
       mov    R0,#0
c4b3:  cjne   A,#10110111b,c4b4
       mov    R0,#12
c4b4:  cjne   A,#01110111b,back
       mov    R0,#16
back:  ret
;
tg_tkn: lcall  senkpd
tg_tk0: cjne   R0,#16,tg_tk1
       ljmp   tg_tkn
tg_tk1: cjne   R0,#15,tg_tk2
       ljmp   tg_tkn
tg_tk2: cjne   R0,#14,tg_tk3
       ljmp   tg_tkn
tg_tk3: cjne   R0,#13,tg_tk4
       ljmp   tg_tkn
tg_tk4: cjne   R0,#12,tg_tk5
       ljmp   tg_tkn
tg_tk5: cjne   R0,#11,tg_tk6
       ljmp   mulai
tg_tk6: cjne   R0,#10,tg_tk7
       ljmp   tg_tkn
tg_tk7: ret
;
tg_lps: lcall  senkpd
       cjne   R0,#10,tg_lps
       ret
;
jeda:  jnb     Stts,pison

```

```

        clr        Puls
pison:  mov        Dly0,Dfrk
        djnz       Dly0,$
        setb       Puls
        mov        Dly0,Dfrk
        djnz       Dly0,$
        ret

;
delays: acall      senkpd
        cjne       R0,#13,dlys0
        ljmp       seting
dlys0:  cjne       R0,#14,dlys1
        ljmp       dt_adc
dlys1:  djnz       Dly1,delays
        ret

;
delay1: mov        Dly2,#20
dly1:   acall      delays
        djnz       Dly2,dly1
        ret

;
nama:   DB         '  Ismail Jufri  '
        DB         '  NIM: 0017204  '
univ:   DB         '  Teknik Elektro '
        DB         '  ITN Malang    '
mskvit: DB         '  Setting Volt   '
        DB         '  00.0 V       '
dtadnr: DB         '  Data Benar ?   '
vitout: DB         '>>  OUTPUT  <<'
kosong: DB         '                '
bcaadc: DB         '  Baca ADC       '
dtaadc: DB         '  Data ADC :     '
angka: DB         '0123456789      '
lookup: DB         000,001,001,002,002,003,004,004,005,005
        ; 00
        DB         006,007,007,008,008,009,010,010,011,011
        ; 10
        DB         012,013,013,014,014,015,016,016,017,017
        ; 20
        DB         018,019,019,020,020,021,022,022,023,023
        ; 30
        DB         024,025,025,026,026,027,028,028,029,029
        ; 40
        DB         030,031,031,032,032,033,034,034,035,035
        ; 50
        DB         036,037,037,038,038,039,040,040,041,041
        ; 60
        DB         042,043,043,044,044,045,046,046,047,047
        ; 70
        DB         048,049,049,050,050,051,052,052,053,053
        ; 80
        DB         054,055,055,056,056,057,058,058,059,059
        ; 90
        DB         060,061,061,062,062,063,064,064,065,065
        ; 100

```



100%

At Peak = 0.00000

1.000

1.000

Curve 1
100%

Curve 2
100%

Curve 3
100%

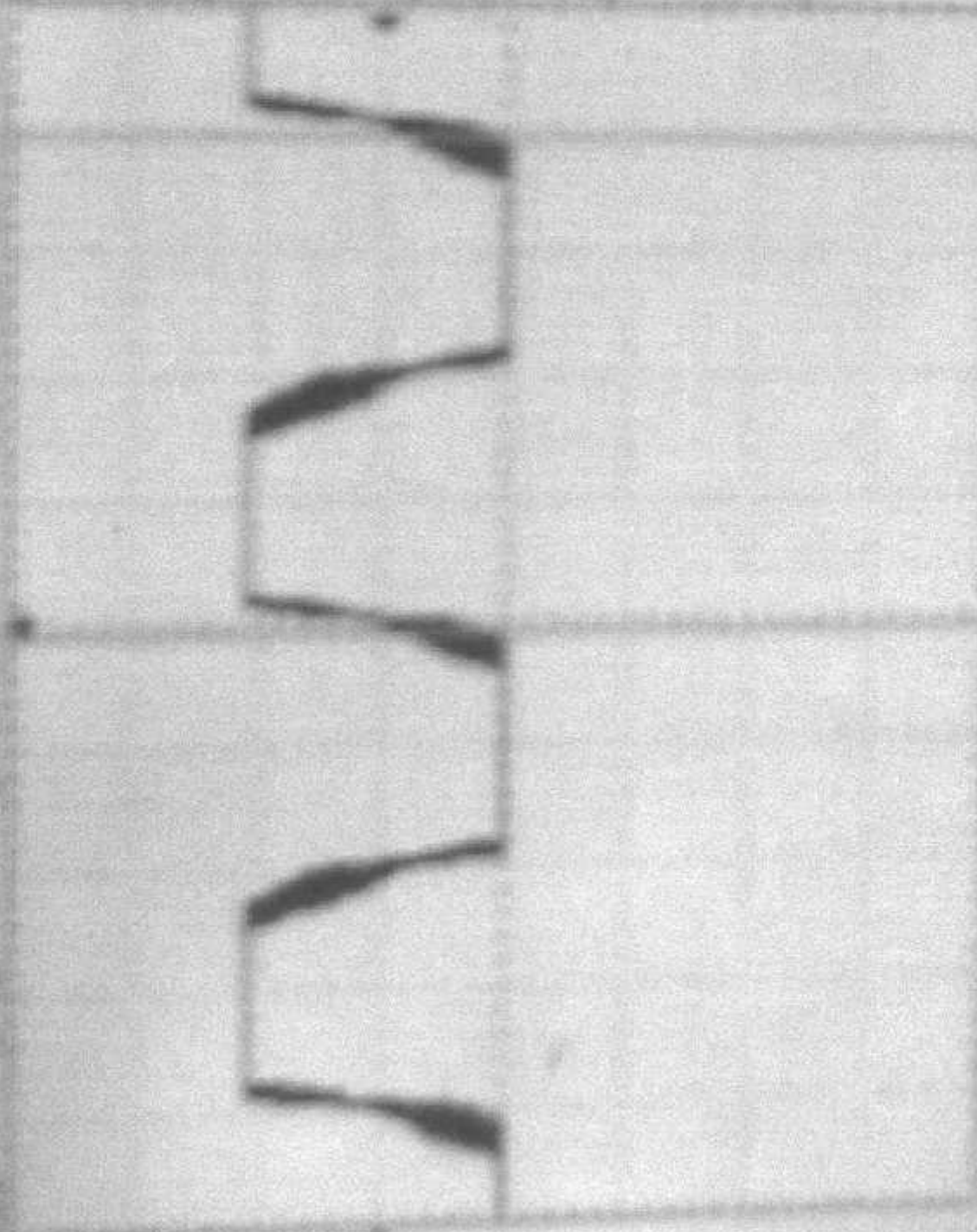
Curve 4
100%

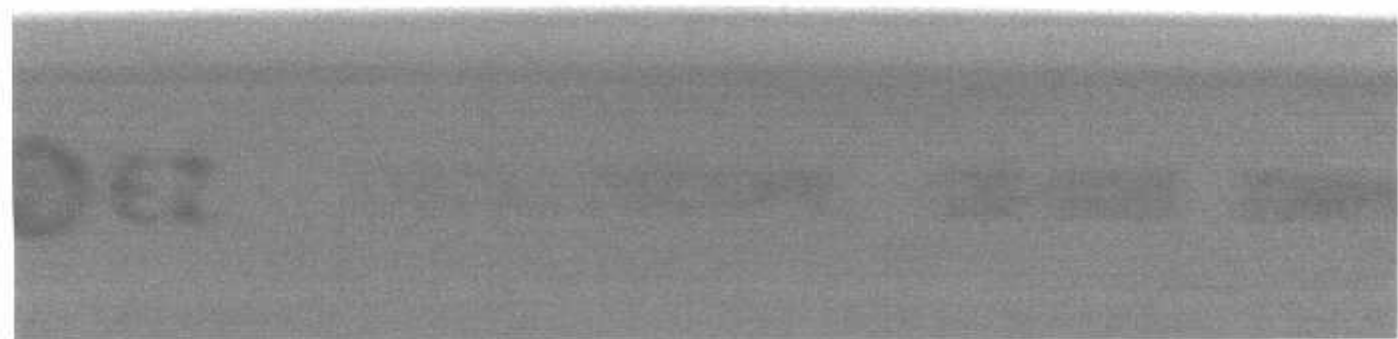
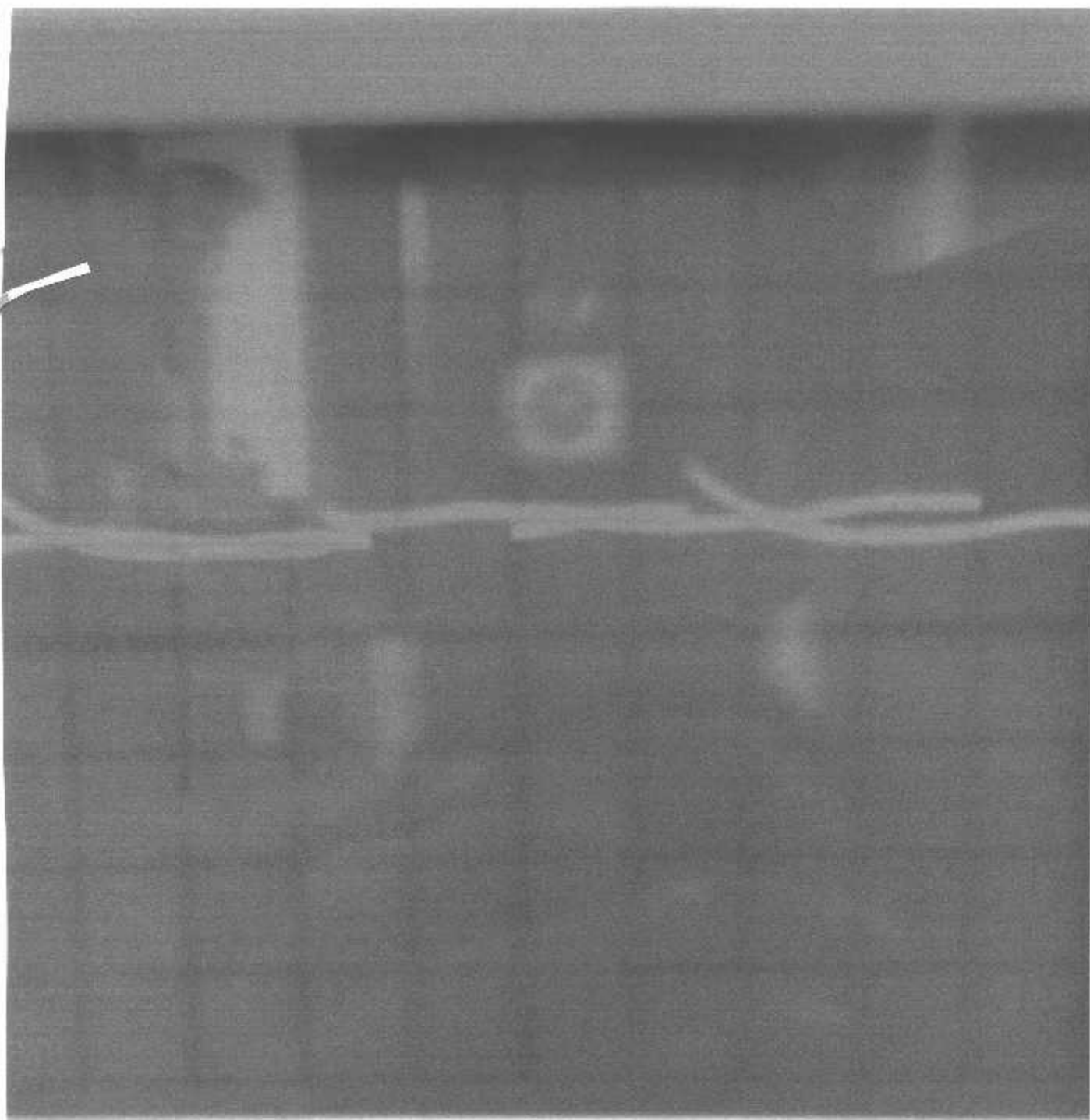
Curve 5
100%

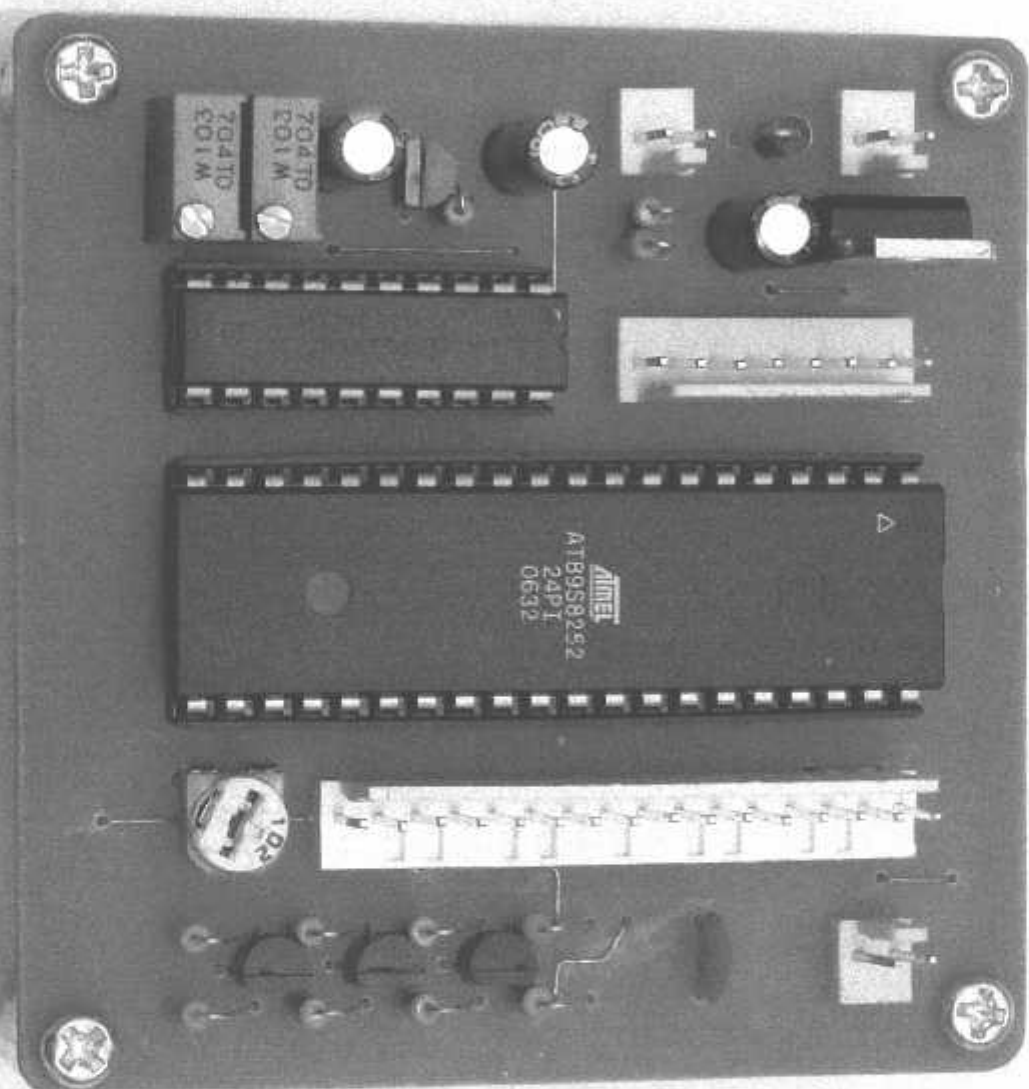
CH 1 / 100%

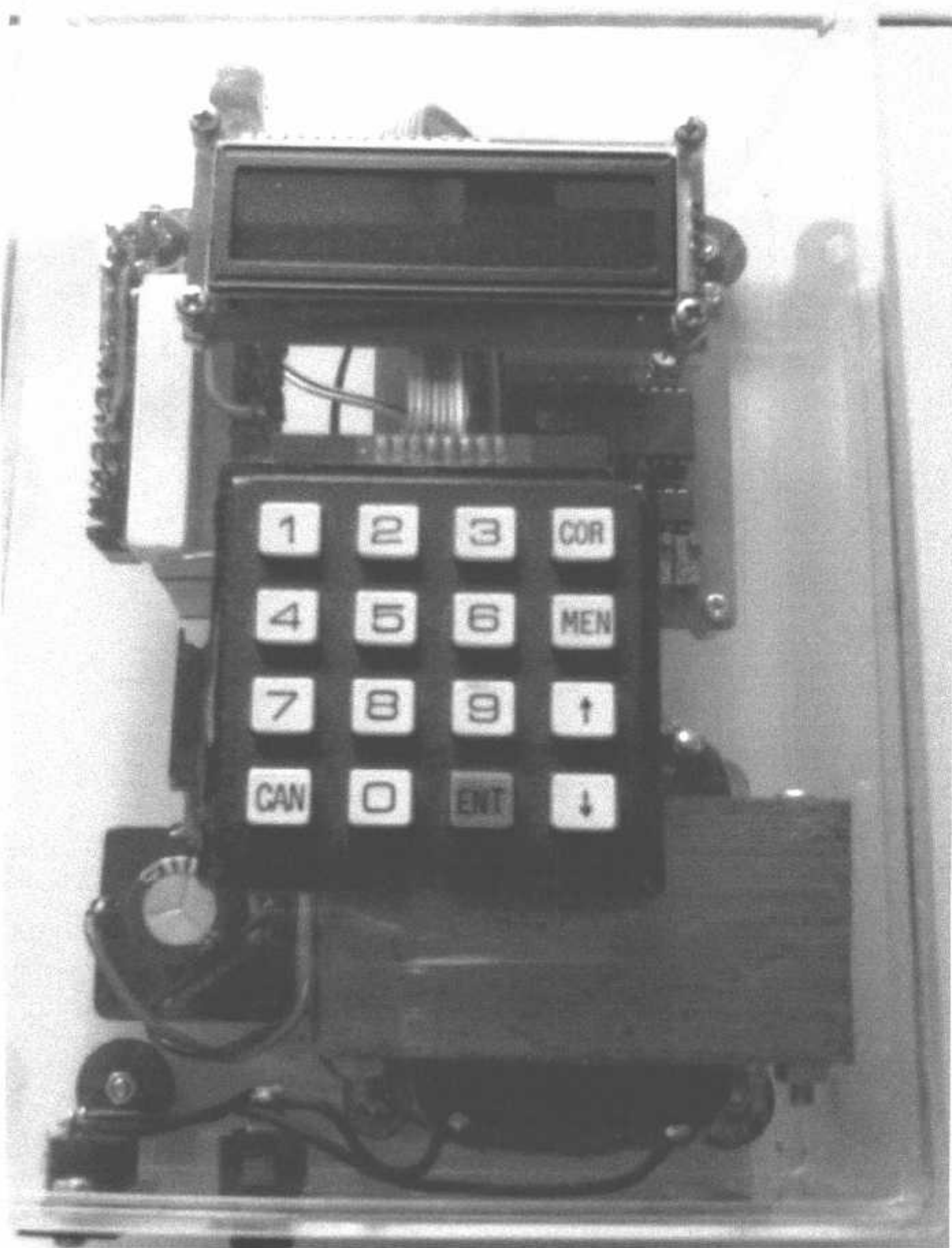
CH 2 / 100%

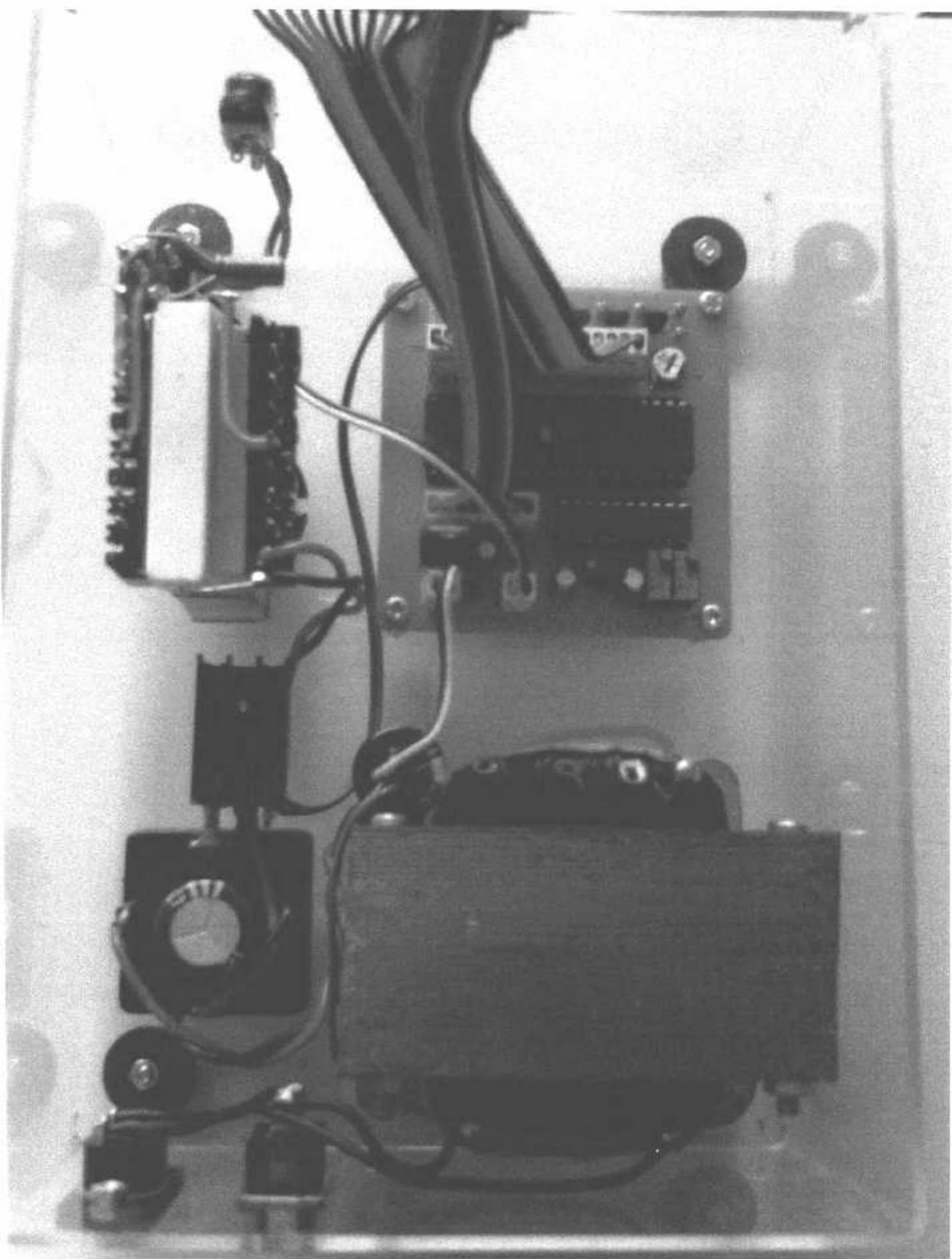
CH 3 / 100%



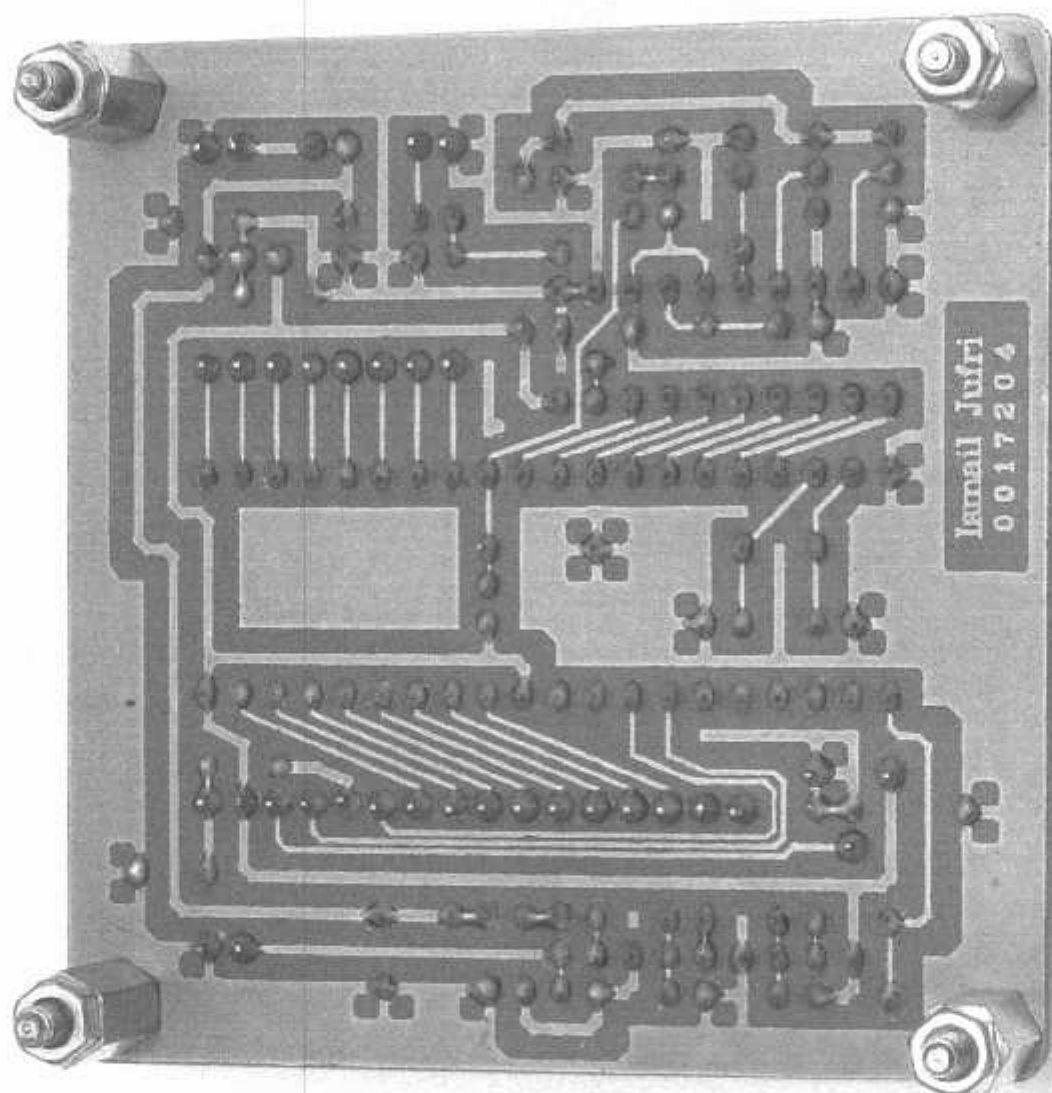


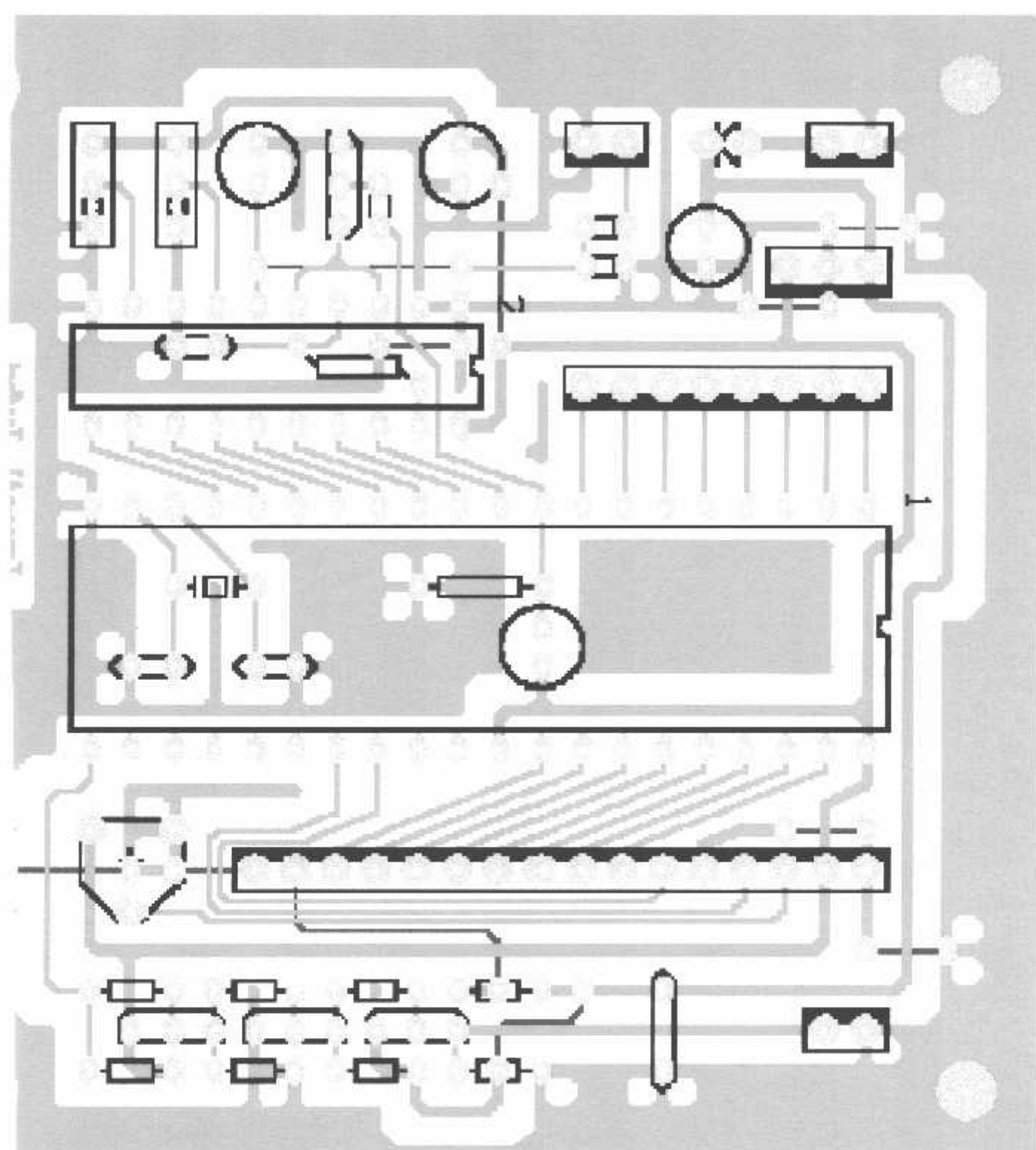












SWITCH-MODE PERSEDIAAN TENAGA

Elektronika tenaga berhadapan dengan empat format konversi tenaga.

1. ac-dc konversi
2. ac-ac konversi,
3. dc-ac konversi dan
4. dc-dc konversi.

DC-DC konverter dikenal lebih awal, ketika SCRS telah digunakan. Sekarang ini, IGBTs dan MOSFETs adalah alat menggunakan untuk dc-dc konversi dan sirkuit ini dapat digolongkan seperti sirkuit persediaan tenaga gaya tombol. Singkatan atau singkatan untuk persediaan tenaga gaya tombol adalah SMPS.

Suatu gaya tombol menggerakkan sirkuit persediaan adalah serbaguna. dapat digunakan untuk:

1. Langkah menurunkan suatu dc voltase masukan tak diatur untuk menghasilkan suatu dc voltase keluaran diatur menggunakan suatu sirkuit mengenal sebagai Konverter Saran atau Step-Down SMPS,
2. Melangkah atas suatu dc voltase masukan tak diatur untuk menghasilkan suatu dc voltase keluaran diatur menggunakan suatu sirkuit yang dikenal sebagai Naikkan tegangan Konverter atau Meningkatkan SMPS,
3. Melangkah atas atau turun suatu dc voltase masukan tak diatur untuk menghasilkan suatu dc voltase keluaran diatur,
4. Membalikkan masukan dc voltase menggunakan pada umumnya suatu sirkuit seperti Cuk Konverter,
5. Menghasilkan berbagai dc keluaran menggunakan suatu sirkuit seperti melenting kembali konverter.

Suatu persediaan tenaga gaya tombol adalah suatu sirkuit digunakan sekarang ini dan digunakan adalah suatu sistem seperti suatu komputer, penerima televisi, penuntut baterai dan lain lain Switch frekwensi pada umumnya di atas 20 kHz, sedemikian sehingga suara gaduh yang diproduksi oleh itu adalah di atas audio mencakup. Ini juga digunakan untuk menyediakan suatu variabel dc voltase ke perlengkapan suatu dc motor di dalam suatu variabel mempercepat pengarah. Itu digunakan adalah suatu frekuensi tinggi sirkuit faktor unity-power.

Pendahuluan

Suatu konverter saran atau step-down tenaga gaya tombol persediaan dapat juga disebut suatu pengatur gaya tombol. Kebenaran suatu pengatur gaya tombol adalah dalam kaitan dengan nya secara wajar efisiensi tinggi dan ukuran ringkas dan suatu pengatur gaya tombol digunakan sebagai pengganti suatu pengatur tegangan linier pada keluaran yang tinggi, sebab pengatur tegangan linier adalah tidak efisien. Karena alat tenaga menggunakan pengatur linier harus mengurangi suatu jumlah cukup besar tenaga, mereka harus cukup didinginkan, dengan kerja pemasangan pada atas heatsinks dan panas ditransfer dari heatsinks kepada udara sekitar baik oleh ilian alam maupun oleh forced-air yang mendingin. Heatsinks dan ketetapan untuk mendingin buatan pengatur yang besar sekali ukurannya dan besar. Di dalam aplikasi di mana ukuran dan efisiensi adalah pengatur tegangan linier kritis tidak bisa digunakan.

Suatu pengatur gaya tombol mengalahkan kelemahan dari pengatur linier. Tenaga yang diswitch Persediaan jadilah lebih efisien dan mereka cenderung untuk mempunyai suatu efisiensi 80% atau lebih. Mereka dapat dibungkus adalah suatu pecahan ukuran dari pengatur linier. Tidak sama dengan pengatur linier, tenaga yang diswitch persediaan dapat memperbesar atau turun voltase masukan.

Konverter Saran diperkenalkan di halaman ini yang menggunakan pendekatan yang evolusiner. Mari kita mempertimbangkan sirkuit di gambar 1, berisi kutub tunggal double-throw tombol.

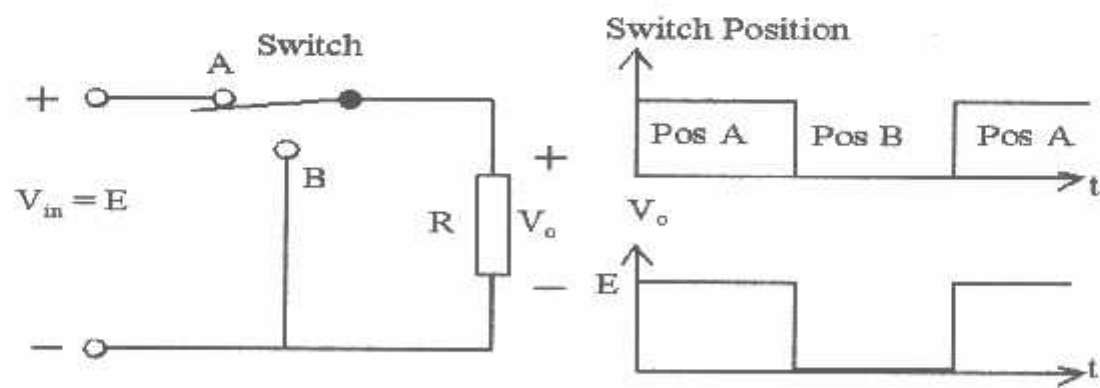


Fig. 1: A resistor with a single pole double-throw switch

Karena sirkuit gambar 1, voltase keluaran yang sama voltase masukan ketika tombol adalah di dalam posisi Adalah suatu dan adalah nol ketika tombol adalah di dalam posisi B. Dengan bermacam-macam jangka waktu di mana tombol adalah di dalam posisi Adalah suatu dan B, dapat dilihat bahwa rata-rata voltase keluaran dapat bervariasi, tetapi voltase keluaran bukanlah dc murni. Voltase Keluaran berisi suatu tegangan rata-rata dengan suatu square-voltage melapiskan pada atas itu, seperti ditunjukkan gambar 2.. Pada umumnya hasil yang diinginkan adalah suatu dc voltase tanpa isi riak nyata dan sirkuit di dalam gambar. 1 diharapkan untuk dimodifikasi.

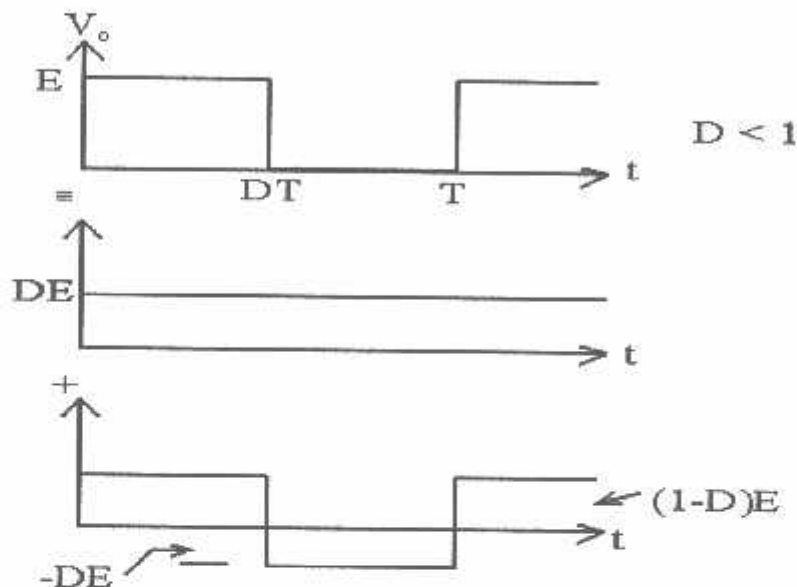


Fig. 2: Output Waveform Decomposed

Sirkuit di dalam gambar. 1 kaleng dimodifikasi seperti ditunjukkan gambar. 3 dengan menambahkan suatu induktor secara urut dengan resistor beban. Suatu induktor mengurangi riak yang melintas saat itu dan keluaran voltase akan berisi lebih sedikit isi riak karena yang sekarang melalui resistor beban adalah sama sebagai induktor itu nya. Ketika tombol adalah di dalam posisi A, yang sekarang melalui induktor meningkat dan energi menyimpan induktor meningkat. Ketika tombol adalah di dalam posisi B, induktor bertindak sebagai suatu sumber dan memelihara yang sekarang melalui resistor beban. Selama periode ini, energi menyimpan pengurangan induktor dan sekarang jatuh. Adalah penting untuk catat bahwa ada kepemimpinan berlanjut melalui beban untuk sirkuit ini. Jika waktunya tetap dalam kaitan dengan induktor dan resistor beban secara relatif besar dibandingkan dengan periode itu di mana tombol

adalah di dalam posisi Adalah suatu atau B, kemudian kenaikan dari sekarang melalui induktor jadilah lebih atau lebih sedikit linier, seperti ditunjukkan gambar. 3.

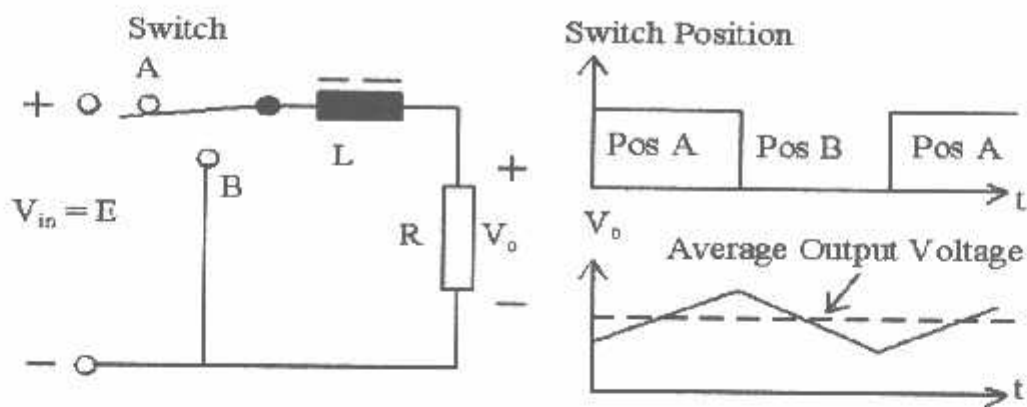


Fig. 3: Effect of Inductor

Langkah yang berikutnya di dalam pengembangan yang evolusiner konverter saran adalah untuk menambahkan suatu kapasitor ke seberang resistor beban dan sirkuit ini ditunjukkan gambar 4. Suatu kapasitor mengurangi isi riak itu di dalam voltase ke seberang itu, sedangkan suatu induktor memperlancar melintas yang sekarang itu. Tindakan LC saringan yang dikombinasikan mengurangi riak itu di dalam keluaran bagi suatu tingkatan sangat rendah.

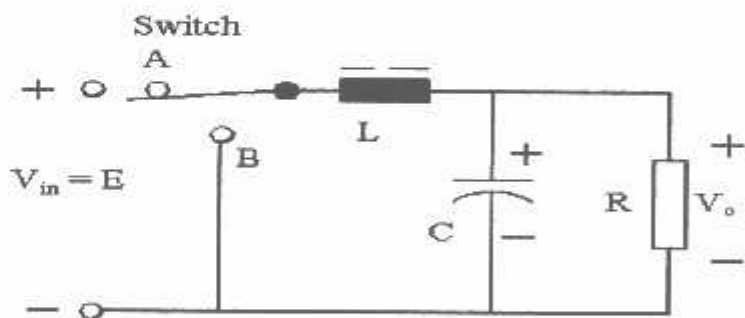


Fig. 4: Circuit with an LC Filter

Sirkuit pada gambar. 4 berisi suatu double-throw tombol berkutub tunggal. Ini merupakan suatu bentuk wujud sulit untuk merealisir menggunakan alat semi penghantar tenaga. Pada sisi lain, suatu pemahaman sirkuit di dalam gambar. 4 antara bagi suatu bentuk wujud sederhana dan dapat dicapai. Ketika tombol adalah di dalam posisi A, yang sekarang melalui induktor dan itu berkurang ketika tombol adalah di dalam posisi B. Itu adalah mungkin untuk mempunyai suatu tombol semi penghantar tenaga untuk sesuai dengan tombol

itu di dalam posisi A. Ketika tombol adalah di dalam posisi B, arus induktor meluncur bebas melalui dan karenanya suatu dioda dapat digunakan untuk meluncur bebas operasi. Kemudian hanya semi penghantar tenaga tombol perlu untuk dikendalikan, dan dalam praktek, suatu pulse-width pengaturan IC digunakan. Sirkuit yang hasil ditunjukkan gambar. 5.

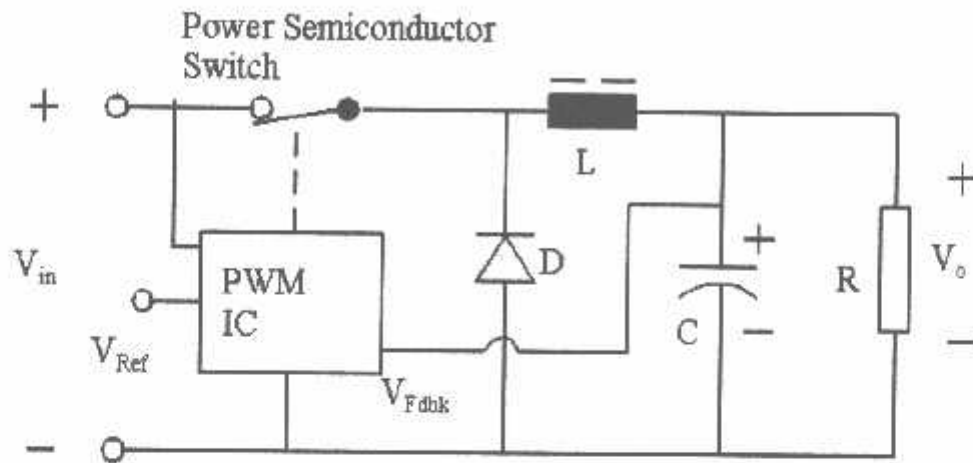


Fig. 5: Step Down Switch Mode Power Supply

Biasanya manapun dasar menswitch persediaan tenaga terdiri dari lima komponen baku:

- Suatu pulse-width yang mengatur pengontrol,
- Suatu tombol transistor,
- Suatu induktor,
- Suatu kapasitor dan
- Suatu dioda.

Kendali oleh pulse-width modulasi, pada umumnya yang diakibatkan oleh suatu IC, adalah yang penting bagi mengatur keluaran itu. Tombol Transistor adalah jantungnya persediaan yang diswitch dan itu mengendalikan tenaga itu menyediakan kepada beban. Tenaga MOSFETS jadilah lebih digunakan dibanding BJTS pada keluaran tenaga 50 W. Transistor pilih untuk digunakan di menswitch tenaga persediaan harus mempunyai kuasa menswitch kali dan harus bisa withstand voltase yang diproduksi oleh induktor.

Suatu induktor digunakan suatu saringan untuk mengurangi riak itu di dalam sekarang. Pengurangan ini terjadi sebab sekarang melalui induktor tidak bisa berubah tiba-tiba. Ketika yang sekarang melalui suatu induktor cenderung

untuk jatuh, induktor cenderung untuk memelihara yang sekarang dengan bertindak sebagai suatu sumber. Induktor menggunakan menswitch persediaan pada umumnya luka pada atas toroidal inti, sering dibuat dari ferrite atau inti besi dengan ruang terbuka dibagi-bagikan untuk memperkecil kerugian inti pada frekwensi tinggi.

Kebanyakan dari persediaan yang diswitch memerlukan suatu beban minimum, dalam rangka memastikan bahwa induktor itu membawa sekarang selalu. Jika yang sekarang mengalir sepanjang induktor itu tidaklah berlanjut.

Konverter Saran atau SMPS dapat dikendalikan jalan dua arah, dikenal sebagai:

1. Constant-Frequency Operasi Atau Pulse-Width Modulasi mengendalikan
2. Variable-Frequency Operasi atau kendali oleh modulasi frekuensi

Dengan pulse-width modulasi mengendalikan, peraturan voltase keluaran dicapai dengan bermacam-macam siklus tugas itu tombol, memelihara frekwensi operasi tetap. Siklus Tugas mengacu pada perbandingan periode di mana semipenghantar tenaga disimpan untuk kepada periode siklus. Pada umumnya mengendalikan dengan berdenyut modulasi lebar adalah lebih disukai metoda operasi frekwensi tetap memimpin ke arah optimisasi LC saringan dan isi riak di dalam voltase keluaran dapat dikendalikan di dalam batas yang di-set. Pada sisi lain, jika beban pada konverter di bawah suatu tingkatan tertentu, regulasi tegangan keluaran menjadi suatu masalah dan dalam yang sedemikian suatu kasus, kendali oleh modulasi freknensi diharapkan untuk lebih disukai.

Jika suatu mikrokontroller digunakan sebagai ganti suatu PWM spesifik IC, itu adalah mungkin ke tombol dari satu gaya mengendalikan kepada lain tergantung pada kondisi-kondisi beban itu.

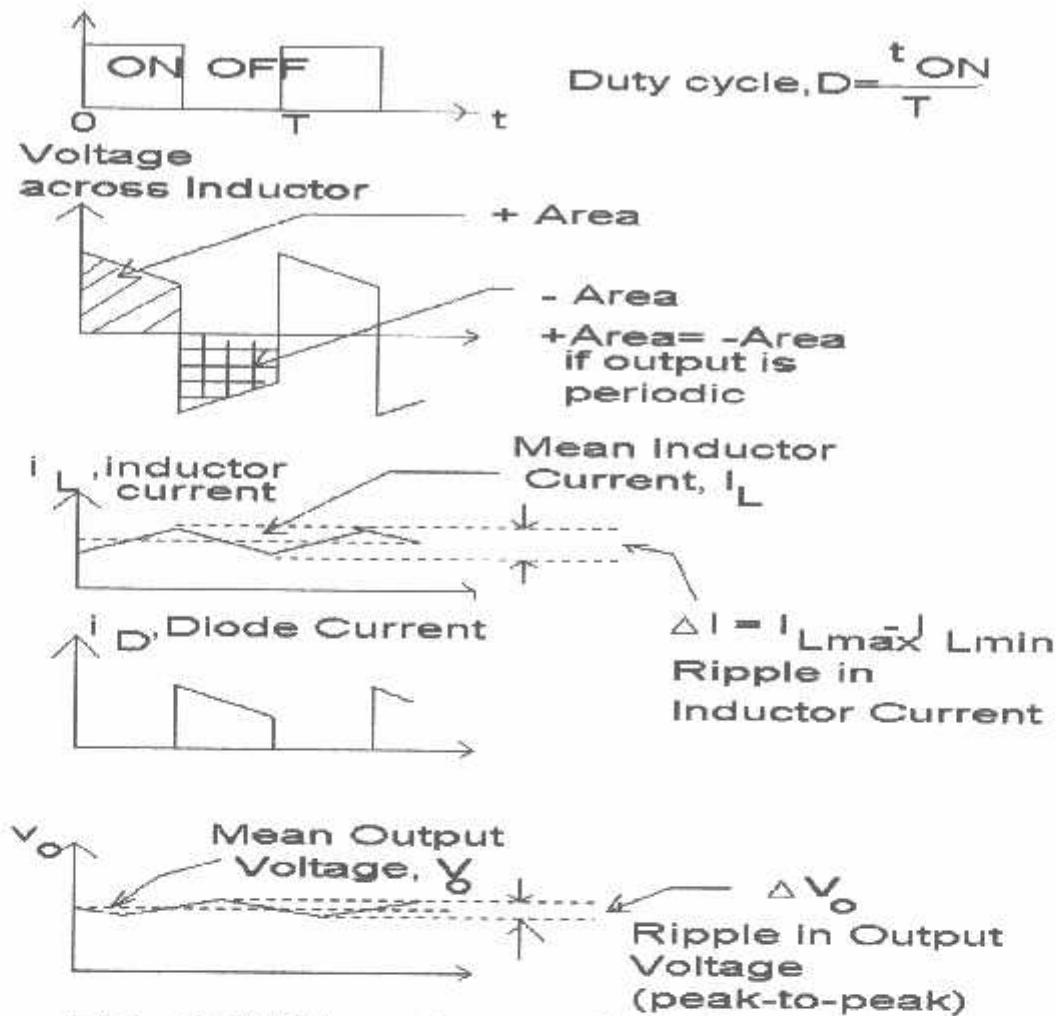


Fig. 10: Waveforms for step-down Switch-Mode Regulator

Pada [atas] evaluasi,

$$(E - V_{o,avg})DT - V_{o,avg}(1 - D).T = 0$$

$$\text{That is, } V_{o,avg} = D.E \quad (10)$$

Perubahan di dalam arus induktor ketika tombol adalah Pada atas kaleng ditentukan sebagai berikut. yang dibiarkan Perubahan di dalam arus induktor bukan, seperti ditunjukkan gambar. 10. Di dalam ini menggambarkan, perubahan di dalam keluaran voltase telah dilebih-lebihkan demi kejelasan. Ketika tombol TERPASANG, voltase ke seberang induktor dapat dinyatakan seperti:

$$v_L(t) = L \frac{di_L}{dt} = E - v_o \quad (11)$$

Ketika voltase keluaran tinggal mantap pada $V_{o,Avg}$, arus induktor secara linier sepanjang pada periode tombol itu. Kemudian

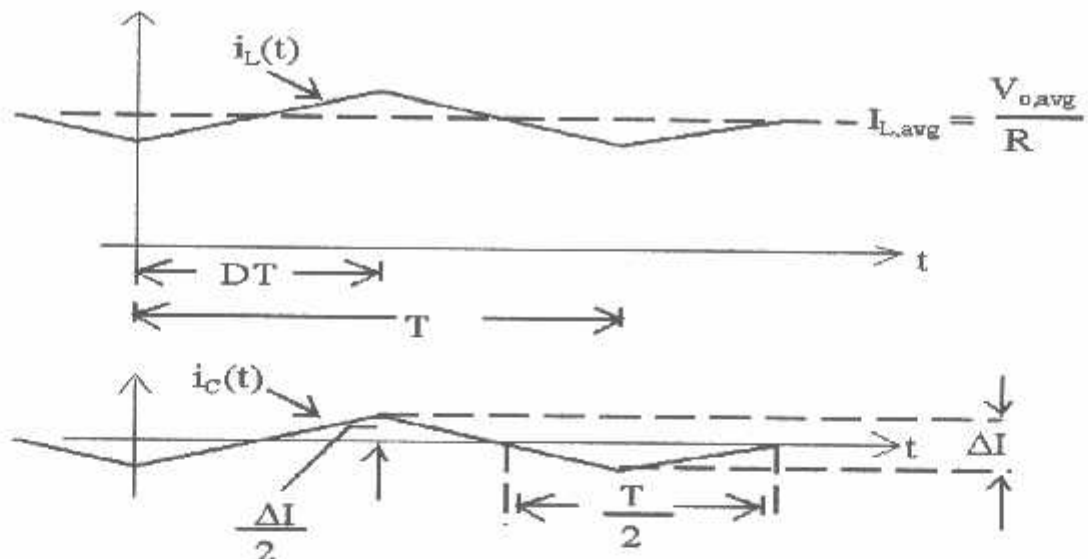


Fig.11: Capacitor Current

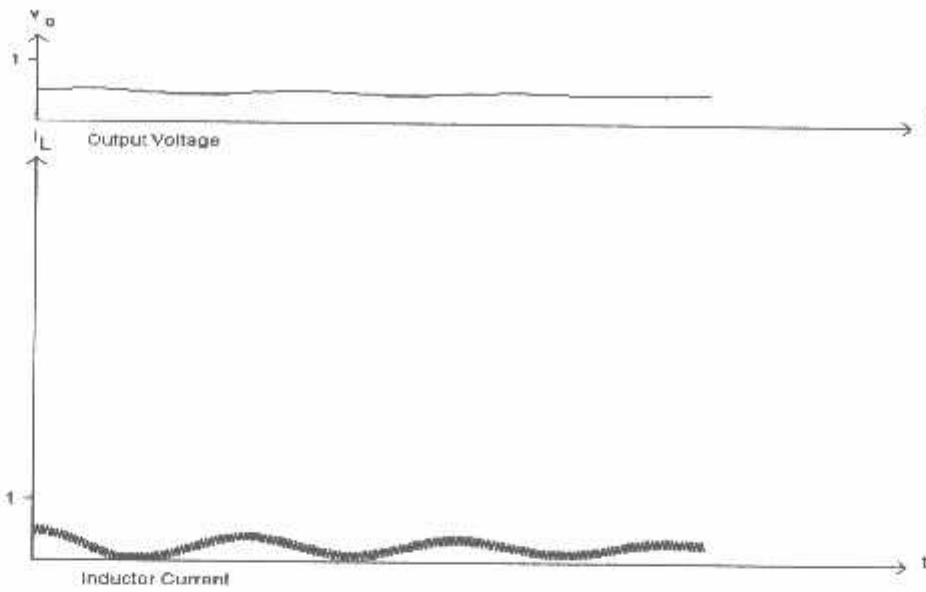
Sepanjang ON-PERIOD, arus induktor naik dari $(V_{o,Avg}/R - I/2)$ untuk $(V_{o,Avg}/R + I/2)$. Itu adalah,

$$i_L(0) = i_L(T) = \frac{V_{o,avg}}{R} - \frac{\Delta I}{2}, \quad i_L(DT) = \frac{V_{o,avg}}{R} + \frac{\Delta I}{2} \quad (13)$$

DISCONTINUOUS OPERASI

Ketika resistor beban menjadi tinggi, sirkuit konverter akan beroperasi itu discontinuous gaya. Arus Induktor jatuh pada nol ketika tombol bersikap terbuka dan tinggal pada nol hingga tombol menjadi pada yang siklus yang berikutnya itu. Gaya seperti itu adalah gaya operasi yang diinginkan ketika frekwensi variabel operasi dipekerjakan untuk pengendalian tegangan. Apalagi, discontinuous operasi menaruh lebih sedikit tekanan pada atas dioda dan sirkuit beroperasi dengan baik. Aspek ini akan jadi diterangkan kemudian.

Efek pembalasan beban pada arus induktor ditunjukkan gambar. 17. Dengan bahwa kepemimpinan adalah berlanjut, rata-rata arus beban adalah $V_{o,Avg}/R$. Seperti pembalasan beban meningkat, rata-rata pengurangan arus beban, tetapi pada sisi lain, perubahan di dalam arus induktor sebagai digambarkan oleh persamaan (12) tinggal tetap. Seperti ditandai oleh persamaan (13), sisa arus induktor di dalam cakupan menetapkan di bawah.



Buahan. 16: Efek Beban Langkah Ber;Ubahlah: Pengurangan di (dalam) Beban

$$\left. \begin{aligned} \left(\frac{V_{o,avg}}{R} - \frac{\Delta I}{2} \right) \leq I_L \leq \left(\frac{V_{o,avg}}{R} + \frac{\Delta I}{2} \right) \text{ if } \left(\frac{V_{o,avg}}{R} \right) \geq \left(\frac{\Delta I}{2} \right) \\ 0 \leq I_L \leq \left(\frac{V_{o,avg}}{R} + \frac{\Delta I}{2} \right) \text{ if } \left(\frac{V_{o,avg}}{R} \right) < \left(\frac{\Delta I}{2} \right) \end{aligned} \right\} \quad (21)$$

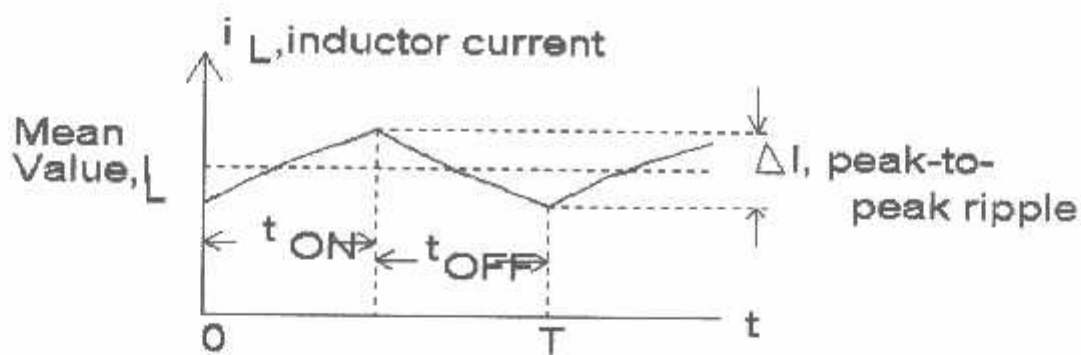
Ketika arus induktor adalah berlanjut, nilai $V_{o,Avg}$ adalah seperti digambarkan oleh persamaan (10) dan tidak demikian jika kepemimpinan adalah discontinuous. Setelah menggantikan dari persamaan (12), kita mendapatkan bahwa

$$\left. \begin{aligned} V_{o,avg} \left(\frac{1}{R} - \frac{(1-D)}{2fL} \right) \leq I_L \leq V_{o,avg} \left(\frac{1}{R} + \frac{(1-D)}{2fL} \right), \text{ if } V_{o,avg} \left(\frac{1}{R} - \frac{(1-D)}{2fL} \right) \geq 0 \\ 0 \leq I_L \leq V_{o,avg} \left(\frac{1}{R} + \frac{(1-D)}{2fL} \right) \text{ if } V_{o,avg} \left(\frac{1}{R} - \frac{(1-D)}{2fL} \right) < 0 \end{aligned} \right\} \quad (22)$$

Karenanya suatu pembalasan kritis, kata RC dapat digambarkan itu membuat sirkuit beroperasi pada batas dari kepemimpinan berlanjut, suatu situasi menggambarkan gambar 17. Ketika pembalasan beban lebih tinggi dibanding kepemimpinan di dalam induktor adalah discontinuous dan itu adalah berlanjut jika pembalasan beban kurang dari RC.

Itu dapat dilihat dari penyamaan bahwa di batas dari berlanjut dan discontinuous kepemimpinan,

$$R_C = \frac{2 \times D \times E}{\Delta I} = \frac{2 f L}{1 - D} \quad (23)$$



(a) Under Full-Load Conditions

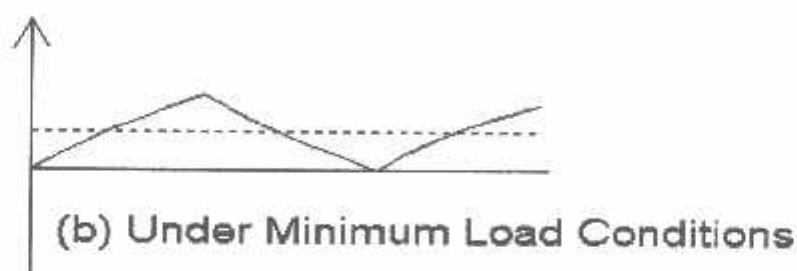


Fig. 17: Inductor current: Boundary of Discontinuous conduction

Discontinuous operasi digambarkan gambar 18. Di dalam gambar. 18, tugas beredar untuk tombol dikenalkan ke D1, dan tugas beredar untuk dioda dikenalkan ke D2. Ini berarti bahwa pada setiap siklus, tombol melakukan untuk sementara waktu interval sepadan dengan $D1T$ dan dioda melakukan untuk sementara waktu interval sepadan dengan $D2T$, di mana T adalah periode siklus. Itu dapat dilihat itu untuk discontinuous kepemimpinan

$$(D_1 + D_2) < 1 \quad (24)$$

Di batas dari berlanjut dan discontinuous kepemimpinan, $(D1 + D2) = 1$. Dengan bahwa discontinuous, tidak ada sekarang di dalam induktor untuk sementara waktu interval sepadan dengan $(1 - D1 - D2)T$.

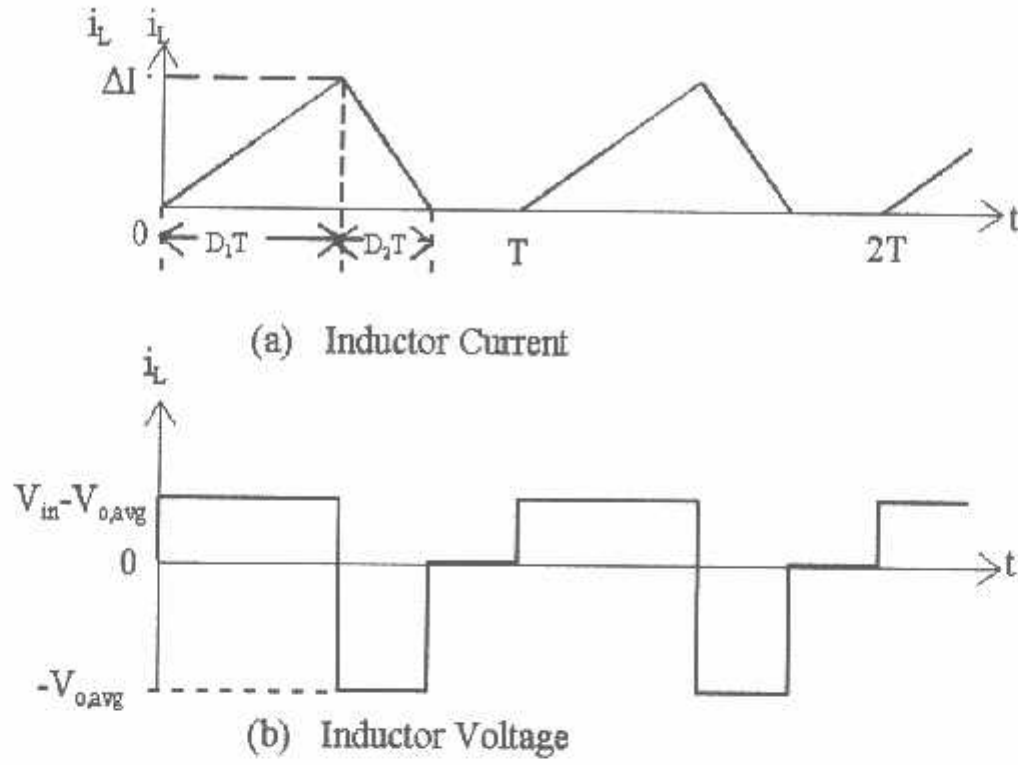


Fig. 18: Buck Converter: Discontinuous Conduction

Rata-Rata arus beban adalah rata-rata arus induktor di dalam gambar. 18. Dari gambar. 18,

$$\Delta I = \frac{(V_{in} - V_{o,avg})D_1}{fL} = \frac{V_{o,avg}D_2}{fL} \quad (24)$$

$$I_{o,avg} = \frac{V_{o,avg}}{R} = \frac{\Delta I}{2} \times (D_1 + D_2) \quad (25)$$

Menggantikan dari persamaan (24), kita mendapatkan bahwa

$$\frac{V_{o,avg}}{R} = \frac{V_{o,avg}D_2}{2fL} \times (D_1 + D_2)$$

$$\text{That is, } (D_2)^2 + D_1D_2 = \frac{2fL}{R} \quad (26)$$

Pemecahan untuk D2,

$$D_2 = -\frac{D_1}{2} + \sqrt{\frac{(D_1)^2}{4} + \frac{2fL}{R}} \quad (27)$$

Ketika $R > RC$, D_2 dapat diperoleh dari persamaan (27), mengira bahwa D_1 , f dan L dikenal. Karena rata-rata voltase induktor di atas suatu siklus adalah nol, kita memperoleh dari gambar yang,

$$(V_{in} - V_{o,avg}) \times D_1 = V_{o,avg} \times D_2 \quad (28)$$

Kemudian

$$V_{o,avg} = \frac{D_1 \times V_{in}}{D_1 + D_2} \quad (29)$$

Menggantikan untuk D_2 dari persamaan (27),

$$V_{o,avg} = \frac{D_1 \times V_{in}}{\frac{D_1}{2} + \sqrt{\frac{(D_1)^2}{4} + \frac{2fL}{R}}} = \frac{2D_1V_{in}}{D_1 + \sqrt{(D_1)^2 + \frac{8fL}{R}}} \quad (30)$$

Applet Yang kedua menunjukkan bagaimana D_2 Dan $V_{o,Avg}$ bertukar-tukar ketika $R > RC$.

APPLET PERTAMA

Applet yang kedua menerima tiga parameter, yang yakni menswitch frekwensi, induktor menghargai dan siklus tugas dan merencanakan siklus tugas itu dioda dan voltase keluaran sebagai fungsi pembalasan beban yang bermacam-macam dari RC untuk ($11 RC$).

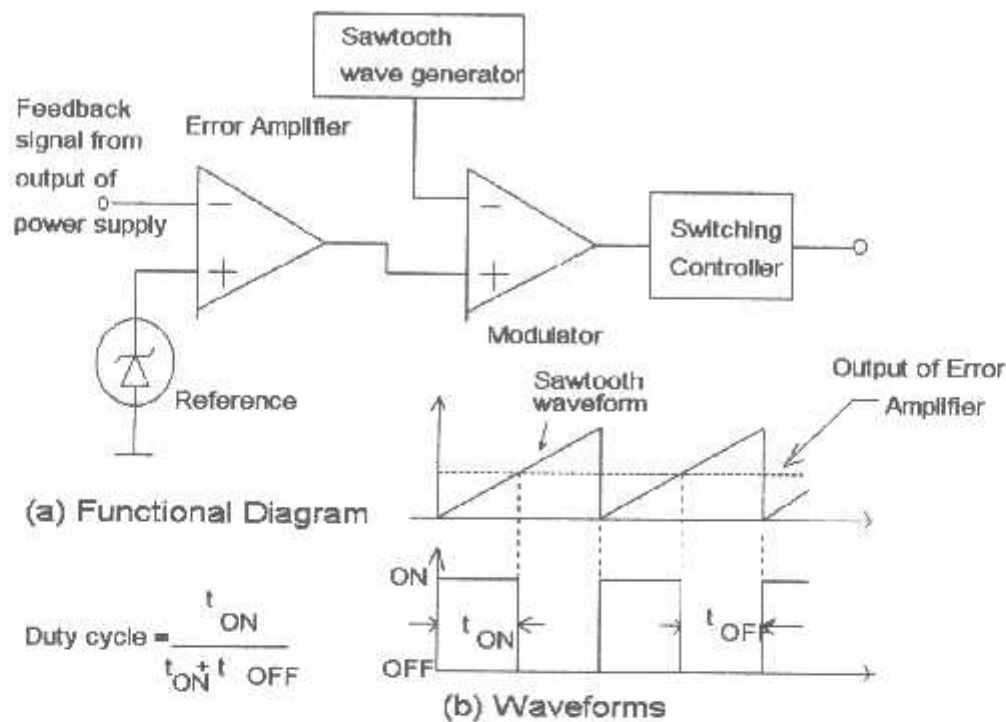


Fig. 19: Pulse-width Modulator

Pulse-Width Modulator mengendalikan tombol semipenghantar itu dan adalah suatu kompleks bagian dari suatu pengatur diswitch. Sekarang ini, pengatur yang diswitch menggunakan suatu pulse-width sirkuit integrator modulator. Prinsip kendali oleh pulse-width modulasi digambarkan gambar. 19. Diagram fungsional yang disederhanakan suatu pulse-width modulator khas ditunjukkan Fig. 19A, sedangkan bentuk gelombang di gambar. 19B menjelaskan operasi itu.

Pulse-Width Sirkuit Modulator terdiri dari suatu saw-tooth generator, suatu amplifier kesalahan, dan suatu pembanding. Frekwensi saw-tooth kaleng generator yang pada umumnya disimpan memilih nilai-nilai sesuai dari suatu RC jaringan. Amplifier Kesalahan bandingkan voltase acuan dan isyarat umpan balik. Isyarat Umpan balik diperoleh penggunaan adalah suatu jaringan pembagi tegangan ke seberang keluaran itu SMPS sirkuit. Sebagai contoh, biarkan isyarat umpan balik itu jadilah V_f dan voltase acuan jadilah V_{ref} . Kemudian

$$V_f = \beta V_o \quad (31)$$

$$\therefore V_f = V_{ref}, V_o = \frac{V_{ref}}{\beta} \quad (32)$$

Keluaran amplifier kesalahan dibandingkan dengan saw-tooth bentuk gelombang itu dan ketika voltase ini adalah lebih besar dari keluaran sawtooth generator, keluaran pembanding akan pada logika '1'. Ketika keluaran pembanding ada di logika '1', tombol di dalam SMPS sirkit dapat bertahan itu PADA ATAS status. Ketika pembanding ada di logika '0', tombol di dalam SMPS sirkit dapat bertahan itu MULAI menyatakan.

CLOSED-LOOP MENGENDALIKAN

Dalam rangka mengatur voltase keluaran itu, suatu pengontrol diperlukan untuk dirancang. Karena ini bermaksud, rangkaian tenaga yang yang pertama diwakili oleh suatu perpindahan berfungsi.

Yang pasif bagian dari rangkaian tenaga ditunjukkan gambar.20. Karena DC keluaran SMPS digambarkan oleh persamaan (10), masukan yang efektif kepada sirkit yang pasif di dalam gambar. 20 kaleng dinyatakan untuk menjadi E.D(S), sedangkan D(S) adalah Laplace Penjelmaan keluaran amplifier kesalahan menunjukkan gambar. 19. Di dalam prosedur desain menguraikan di bawah, D(S) mempertimbangkan keluaran pengontrol, bermacam-macam antar[a] 0 dan 1.

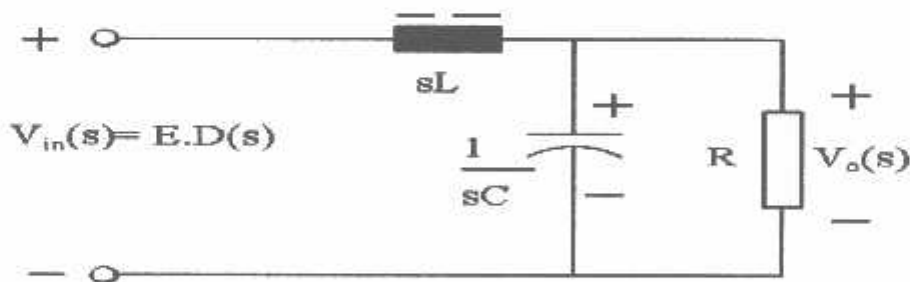


Fig. 20: Buck Converter: Passive Part

Karena sirkit di dalam gambar. 20,

$$\frac{V_o(s)}{V_{in}(s)} = \frac{1/(LC)}{s^2 + \frac{s}{RC} + \frac{1}{LC}} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (33)$$

di mana :

$$w_n = \frac{1}{\sqrt{LC}}, \text{ and } \xi = \frac{1}{2R} \sqrt{\frac{L}{C}} \quad (34)$$

Diagram blok SMPS dengan suatu pengontrol PI (22:7) ditunjukkan Buah ara. 21. Fungsi Perpindahan blok yang berbeda di dalam gambar. 21 sebagai berikut:

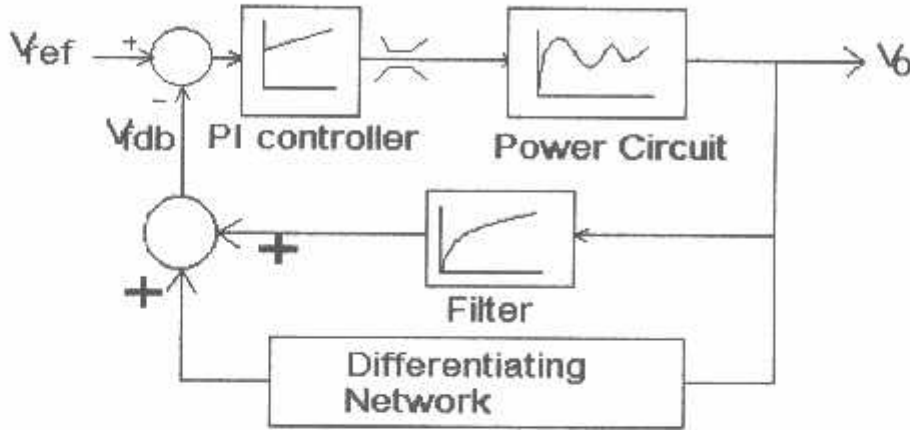


Fig. 21: Block Diagram with a PI controller

PI (22:7) pengontrol mempunyai dua masukan, isyarat acuan V_{ref} yang sesuai dengan voltase keluaran yang diinginkan dan isyarat umpan balik V_{fdb} . Isyarat Kesalahan, perbedaan, e , antar[a] V_{ref} Dan V_{fdb} diberi makan kepada pengontrol PI (22:7) dan keluaran pengontrol PI (22:7) adalah $D(s)$, isyarat yang menetapkan siklus tugas itu. Kemudian

$$\frac{D(s)}{E(s)} = \frac{1 + sKT}{sT} \quad (35)$$

Di dalam persamaan (35), K adalah keuntungan yang sebanding dan T adalah itu mengintegrasikan tetapan-waktu. Keluaran pengontrol PI (22:7) bervariasi antara 0 dan 1 dan mempunyai dua batas, seseorang sesuai dengan siklus tugas yang paling rendah dan lain sesuai dengan siklus tugas yang paling tinggi.

Fungsi Perpindahan rangkaian tenaga diperoleh sebagai berikut. Karena keluaran bervariasi secara linier dengan siklus tugas, penyamaan (33) kaleng diperkenalkan sebagai berikut:

$$\frac{V_o(s)}{D(s)} = \frac{V_m(s)/(LC)}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \quad (36)$$

Karena merancang sistem yang pengulangan tertutup, kutub dalam kaitan dengan sumber dapat diabaikan. Karena rangkaian tenaga sangat banyak umpan balik derivative under-damped diperlukan untuk operasi stabil. Sirkuit Pembedaan menyediakan isyarat umpan balik itu. Untuk simulasi, isyarat yang derivative diperoleh didasarkan pada arus kapasitor itu. Voltase Umpan balik yang derivative adalah mulai jadilah $kd \cdot i_C$, di mana i_C diharapkan untuk menjadi saban unit menghargai.

Applet yang ketiga yang diperkenalkan di bawah mengijinkan pemakai itu untuk mendisain suatu pengontrol PI (22:7) pantas. Parameter untuk di-set adalah: menswitch frekwensi di dalam kHz, keuntungan pengontrol PI (22:7), nya mengintegrasikan tetapan-waktu, induktans, kapasitansi, pembalasan beban, waktunya tetap untuk saringan di dalam alur umpan balik dan koefisien yang derivative.

APPLET KETIGA

Pengaturan Umpan balik menggunakan untuk simulasi yang nyata berisi untaian tambahan. Itu adalah diperlukan untuk membatasi arus induktor itu karena dilihat dari tanggapan yang pengulangan terbuka bahwa arus induktor dapat beberapa kali sekarang yang dinilai, di mana arus beban yang dinilai adalah beban maksimum yang sekarang yang nominal itu SMPS. Ini merupakan suatu parameter yang dapat yang ditetapkan dalam program.. Di dalam program ini, batas yang sekarang ditetapkan pada 1.5 kali arus beban yang dinilai, dan ketika arus induktor melebihi yang sekarang membatasi, yang sekarang lebih dari batas yang sekarang diperbesar dan ditambahkan kepada isyarat umpan balik. Sebagai tambahan, suatu isyarat umpan balik derivative, yang diperoleh menggunakan arus kapasitor itu, ditambahkan kepada isyarat umpan balik. Umpan balik derivative meningkatkan membasahi sistem dan tanpa itu, sistem adalah oscillatory kendati suatu pengontrol PI (22:7) dirancang dengan baik. Sedang merancang pengontrol PI (22:7) itu yang menggunakan applet yang ketiga, menswitch sirkit digantikan oleh suatu penguat linear dan perkiraan ini adalah yang penting bagi perancangan pengontrol PI (22:7). Tetapi pada

kenyataannya, square-wave voltase masuk kepada rangkaian tenaga membuat sistem [itu] untuk oscillatory [karena;sejak] rangkaian tenaga dengan berat under-damped. Pengaturan Umpan balik digunakan ditunjukkan Buah ara. 22.

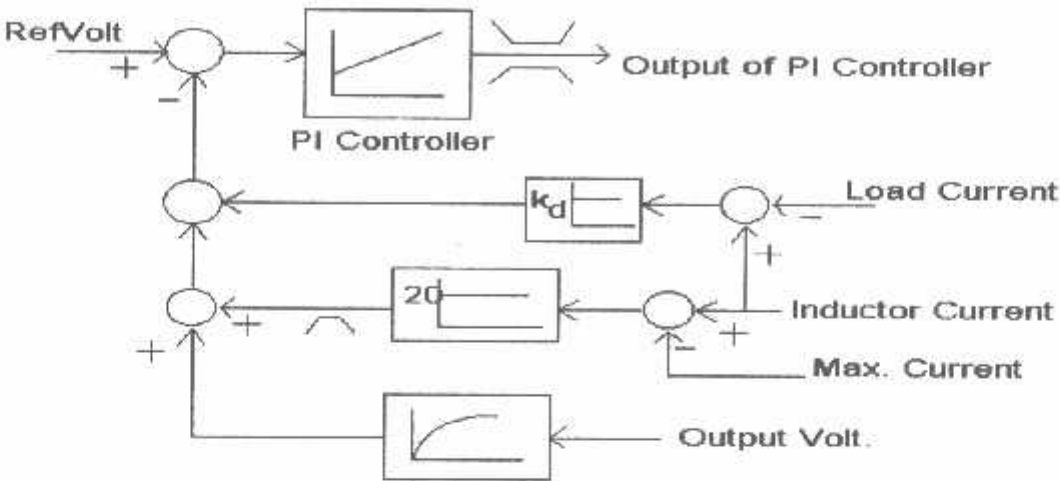


Fig. 22: Feedback arrangement

APPLET KE LIMA

IMPLEMENTASI YANG MENGGUNAKAN Suatu PENGALI

Implementasi yang menggunakan suatu pengali adalah suatu pilihan menarik karena rencana ini dapat [menyampaikan/kirim] hampir menginginkan voltase keluaran kendati fluktuasi di (dalam) voltase sumber. Rencana untuk digunakan ditunjukkan gambar. 23.

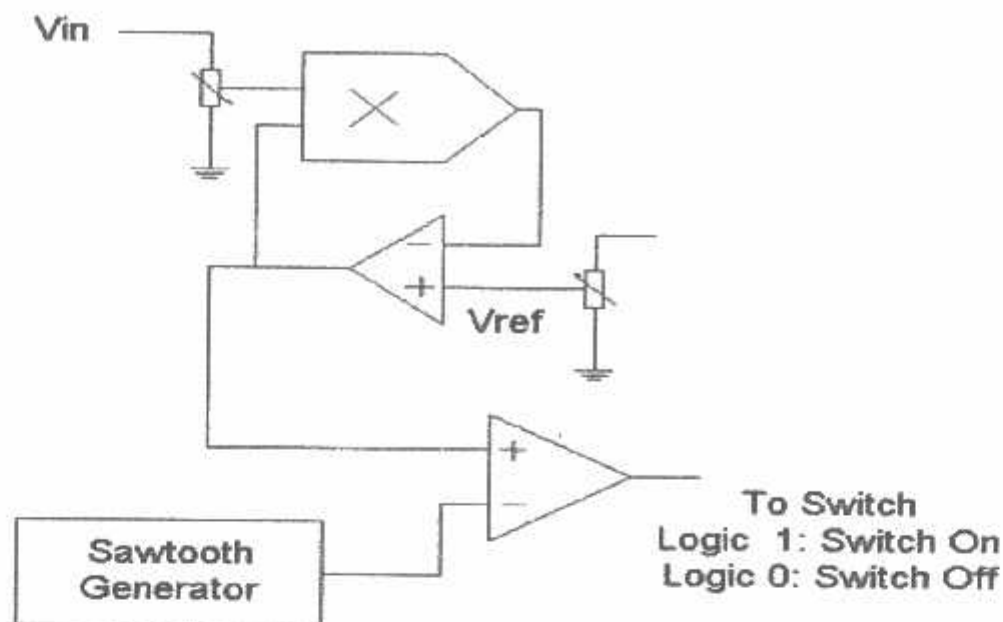


Fig. 23: Implementation using a multiplier

Masukan kepada pengali adalah voltase sumber atau suatu [part;bagian] daripadanya dan keluaran opamp di (dalam) pengulangan/jerat umpan balik. Karena keluaran pengali perlu Vref sama Perwakilan voltase keluaran yang diinginkan, keluaran opamp mencerminkan tugas itu beredar. Isyarat ini dapat dibandingkan dengan keluaran suatu sawtooth generator dan suatu denyut nadi untuk menyalakan tombol itu dapat diperoleh. Jika Vref dapat dimodifikasi untuk meliputi efek meneteskan ke dalam tombol itu, keluaran SMPS dapat sama nilai yang di-set itu. Applet yang keenam menirukan itu SMPS yang dikendalikan cara ini.

RINGKASAN

Halaman ini telah uraikan operasi suatu gaya tombol step-down menggerakkan sirkit persediaan. Karena uraian di dalam halaman ini, itu telah mengira bahwa komponen itu menggunakan rangkaian tenaga adalah ideal, sedangkan mereka bukanlah ideal

Power ON

Listrik 220 masuk ke trafo , sekunder dipilih tegangan AC 15 V, tegangan tersebut disearahkan menjadi DC 15 V, dipilih juga tegangan AC 12 V pada lilitan sekunder dan disearahkan menjadi DC 12 V untuk supply control.

Ketika diinginkan tegangan output tertentu , nilai tegangan diset pada keypad, setelah data benar dan kemudian ditekan enter maka control akan mengeluarkan sinyal dengan frekuensi 1 Khz , kemudian arus akan mengalir dari kuprox (Penyearah 15 V) ke trafo switching. Tegangan yang keluar dari sekunder trafo switching disearahkan menggunakan kuprox 2 A dan kemudian dikeluarkan sebagai tegangan output.

ADC membaca tegangan yang dihasilkan dari sekunder trafo switching yang sudah disearahkan dan kemudian diubah menjadi data digital dan diberikan kepada mikrokontroler. Mikrokontroler membaca data tersebut dan membandingkannya dengan data base tegangan. Misalnya Data = 50 tegangan 5 Volt.

Jika data ADC yang dibaca kurang dari data base tegangan, maka mikrokontroler akan menaikkan frekuensi menjadi 6,6 Khz kemudian dibaca kembali sampai dengan data ADC yang dibaca sama dengan data base tegangan.

Jika data ADC yang dibaca lebih dari data base tegangan maka mikrokontroler akan menurunkan frekuensi tersebut sampai dengan data ADC yang dibaca sama dengan data base tegangan.

PWM (Pulse Width Modulation) adalah : Memodulasi atau merekayasa waktu On dan Off , Perbandingan waktu On dan Off dikonversi ke dalam satuan persen

$$\begin{aligned}\text{misalnya On 30 dan 70 Off maka PWM} &= 30 \% = \frac{30}{30 + 70} \times 100 \% \\ &= 30 \%\end{aligned}$$

Pengujian minimum system :

Pengujian dalam sistem ini dilakukan untuk mengetahui apakah rangkaian minimum sistem dan perangkat lunak yang diisikan dalam EPROM sudah bekerja dengan benar. Pengujian juga dilakukan dengan mengoperasikan peralatan melalui tombol operasi (keypad). Oleh karena itu pengujian minimum system ini dapat dilakukan dengan melihat hasil yang diperoleh seperti lcd pada 7 matrix, lebar pulsa yang keluar pada kaki output sesuai dengan program.

Pengujian Switching Power Supply :

- 1). Melihat lebar pulsa awal yang dibangkitkan oleh rangkaian mikrokontroler.

Tegangan output diamati oleh bermacam-macam seting sambil melihat perubahan lebar pulsa yang tampak pada layar osciloscop, kemudian output dibebani, juga sambil melihat output kaki mikro.

- 2). Pengujian besaran arus input switching, tegangan input, tegangan output, arus output, ripple output (pada beban 330 Ω resistor ½ W karbon murni) kemudian ditabelkan.
-

HASIL PENGUJIAN

V Set	V Out	Error (%)
0,5	0,54	8
1	1,02	2
1,5	1,55	3,33333333
2	2,06	3
2,5	2,52	0,8
3	3,03	1
3,5	3,56	1,71428571
4	4,01	0,25
4,5	4,52	0,44444444
5	5,15	3
5,5	5,52	0,36363636
6	6,02	0,33333333
6,5	6,51	0,15384615
7	7,02	0,28571429
7,5	7,54	0,53333333
8	8,03	0,375
8,5	8,57	0,82352941
9	9,05	0,55555556
9,5	9,54	0,42105263
10	10,11	1,1
10,5	10,58	0,76190476
11	11,04	0,36363636
11,5	11,54	0,34782609
12	12,22	1,83333333
12,5	12,62	0,96
13	13,23	1,76923077
13,5	13,51	0,07407407
14	14,25	1,78571429
14,5	14,6	0,68965517
15	15,25	1,66666667
	Jumlah error	38,7391061

Analisa error :

$$\text{Error (\%)} = \frac{\text{Selisih tegangan}}{V_{\text{Set}}} * 100 \%$$

$$\text{Error Rata-Rata (\%)} = \frac{\sum \text{Error}}{\sum \text{Data}}$$

$$= \frac{38,73}{30}$$

$$= 1,29 \%$$

DAFTAR RIWAYAT HIDUP

DATA PRIBADI

- Nama Lengkap : Moh. Zulkarnain
- Nama Panggilan : Nanang
- Tempat / Tanggal Lahir : Sumenep / 11-04-1978
- Jenis Kelamin : Laki - Laki
- Kewarganegaraan : Indonesia
- Agama : Islam
- Status : Belum menikah
- Alamat Rumah : Jl. Meranggal Gg. 1 No. 6 Kepanjin
Sumenep
- Telepon : 081803875987

PENDIDIKAN FORMAL

- 2000 – 2007 : Teknik Elektronika S-1 ITN Malang
- 1995 – 1997 : SMU Negeri 1 Sumenep
- 1992 – 1994 : SLTP Negeri 1 Sumenep
- 1986 – 1991 : SD Negeri Pangarangan 1 Sumenep

Dengan ini saya menyatakan bahwa keterangan yang saya berikan diatas adalah benar. Bilamana ternyata terdapat ketidakbenaran, maka saya bertanggung jawab penuh atas akibatnya.

Saya yang bersangkutan,



(Moh. Zulkarnain)

DAFTAR RIWAYAT HIDUP

DATA PRIBADI

- Nama Lengkap : Yudi Setiawan
- Nama Panggilan : Yudi
- Tempat / Tanggal Lahir : Malang / 13- 03 - 1973
- Jenis Kelamin : Laki - Laki
- Kewarganegaraan : Indonesia
- Agama : Islam
- Status : menikah

PENDIDIKAN FORMAL

- 1992 – 1996 : Jurusan Informatika S -1 Stiki Malang
- 1989 – 1991 : SMU St. Albertus
- 1986 – 1988 : SLTP Negeri 2 Malang
- 1980 – 1985 : SD Santa Maria
- 1978 – 1979 : TK Hang tuah

Dengan ini saya menyatakan bahwa keterangan yang saya berikan diatas adalah benar. Bilamana ternyata terdapat ketidakbenaran, maka saya bertanggung jawab penuh atas akibatnya.

Saya yang bersangkutan,



(Yudi Setiawan)

1. Metode penelitian :

Dalam skripsi ini digunakan metoda *flyback* untuk rangkaian *inverter*, karena kesederhanaan rangkaian (tanpa filter output dan lilitan clamp) namun dapat diandalkan dan konfigurasi pengaturan (sebagai penjaga kestabilan) dipakai type PULSE WIDTH MODULATION dimana lebar pulsa yang kita atur, sedangkan frekuensi tetap dipertahankan.

Rangkaian minimum sistem disini digunakan sebagai otak kendali pengaturan lebar pulsa (PWM) agar diperoleh kestabilan tegangan yang tinggi, input keypad, lcd tegangan, dan elemen memori dari contoh tegangan yang dapat dipanggil setiap waktu dengan cepat.

Rangkaian rectifier dan filter untuk meratakan dan memperkecil kerut-kerut tegangan agar diperoleh tegangan output yang diharapkan mendekati tegangan DC murni.

Output dapat beroperasi pada frekuensi tinggi dibutuhkan komponen-komponen pilihan terutama pada masalah trafo *switching*. Inti trafo ini dibuat dari bahan ferit yang didesain khusus dimana bahan tersebut memiliki sifat remanensi yang dapat dengan cepat dipulihkan atau dengan kata lain sifat inti trafo sewaktu diimbis dan berubah menjadi magnet harus secepat mungkin bisa dihilangkan karena sentakan pulsa *switching* yang berikutnya sudah harus bebas dari sisa-sisa magnet yang sebelumnya.

CARA MENDAPATKAN LEBAR PULSA VARIABEL

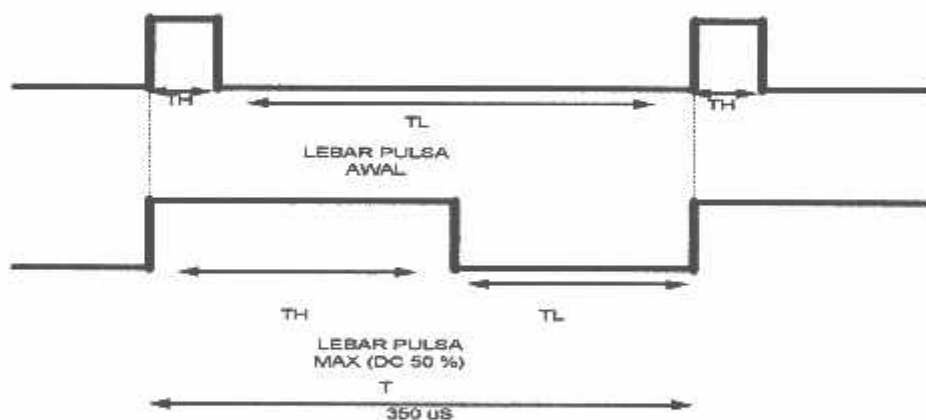
Diatas telah disinggung cara kerja dari rangkaian kontrol yang dapat mengendalikan lebar pulsa variabel secara analog, tetapi dalam tugas akhir ini pembangkit lebar pulsa dilakukan bukan oleh komponen analog melainkan dibangkitkan oleh minimum sistem.

Hal ini dilakukan dengan alasan :

1. Tidak perlu lagi membuat tegangan referensi dan osilator, karena output dari “PWM digital” sudah berlevel digital dan siap untuk mengatur waktu konduksi transistor *switching* menjadi dua keadaan.
 2. Frekuensi kerja dari minimum sistem jauh lebih tinggi dari pada frekuensi kerja rangkaian *switching*, sehingga pelepasan pulsa *switch* dapat diatur dengan cepat.
 3. Untuk membias transistor *switching* disini hanya dibutuhkan dua kejadian saja yaitu sifat saturasi (short) dan cut off (open) atau sebagai saklar. Dua level ini adalah identik dengan level kerja rangkaian digital. Proses pembangkitan pulsa *switch* pertama-tama yang dikeluarkan PWM adalah pulsa yang paling sempit, kemudian dimasukkan ke rangkaian konverter untuk diubah menjadi suatu level tegangan. Karena pulsa yang sempit ini menghasilkan periode “on” transistor yang sangat singkat, sehingga transfer daya pada trafo juga sedikit dan tegangan yang dihasilkan juga sangat kecil, pada saat itu juga ADC disiapkan untuk mendeteksi output dari regulator.
-

Output ADC setelah mengkonversi tegangan yang diterima sudah berupa level digital yang proporsional dengan besaran tegangan dan langsung diumpun pada mikrokontroler dan didalam mikrokontroler terjadi proses perbandingan dengan tegangan set yang diminta.

Jika pada suatu saat output *switching* kita bebani dengan beban yang lebih besar (tetapi tidak lebih besar dari kemampuan *switching*nya), maka tegangannya pasti turun. Gejala ini dapat dirasakan oleh mikrokontroler segera ia memerintahkan untuk menambah lebar pulsa sehingga kestabilan tetap terjaga.

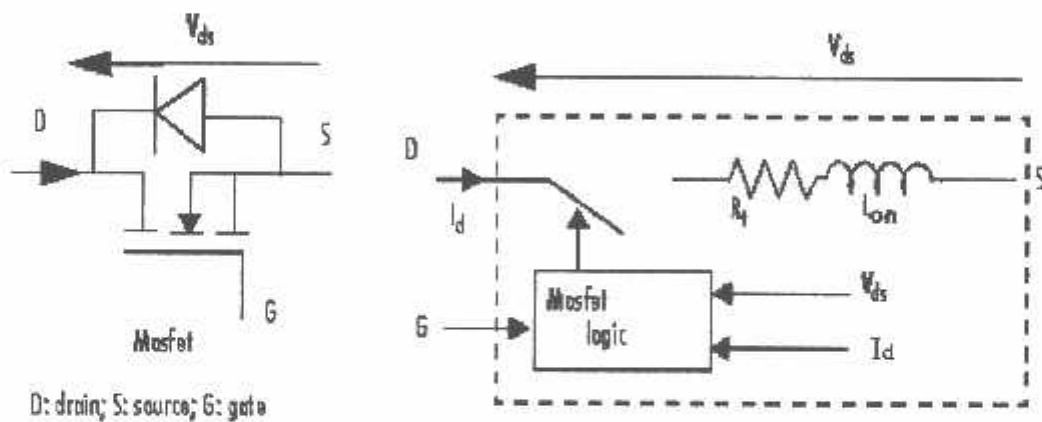


$$\text{Duty cycle } D = \frac{On}{T_{On} + t_{Off}}$$

GAMBAR
LEBAR PULSA VARIABEL

2. Teori mosfet / switching regulator :

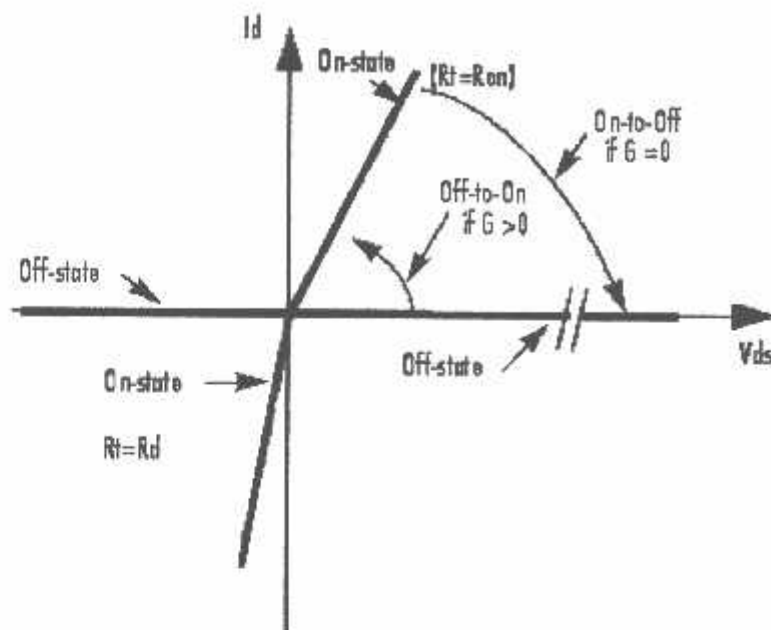
Metal-Oxide-Semiconductor-Field-Effect-Transistor (Mosfet) Blok adalah suatu semi konduktor yang dapat dikontrol oleh gerbang sinyal ($G > 0$) jika mendapat current I_d yang positif ($I_d > 0$). Mosfet Blok dihubungkan secara paralel dengan suatu dioda internal yang menyala ketika Mosfet Blok dibiaskan reverse ($V_{ds} < 0$). Model disimulasikan sebagai kombinasi rangkaian suatu variabel resistor (R_t) dan induktor (L_{on}) secara seri dengan switch control sebagai logical signal ($G > 0$ Atau $G = 0$).



GAMBAR

SIMBOL MOSFET

Mosfet Blok menyala ketika voltase drain-source adalah positif dan sinyal positif diterapkan di masukan gerbang ($G > 0$).



GAMBAR
PARAMETER MOSFET

Dengan arus positif yang mengalir melalui alat, Mosfet Blok mati (turns off) ketika masukan gerbang menjadi nol. Jika current I_d negatif (I_d yang mengalir di dioda internal) dan sinyal gerbang adalah nol ($G = 0$), Mosfet Blok mati ketika current I_d menjadi nol ($I_d = 0$).

- Catatan bahwa resistansi on-state R_t tergantung pada arah arus searah :

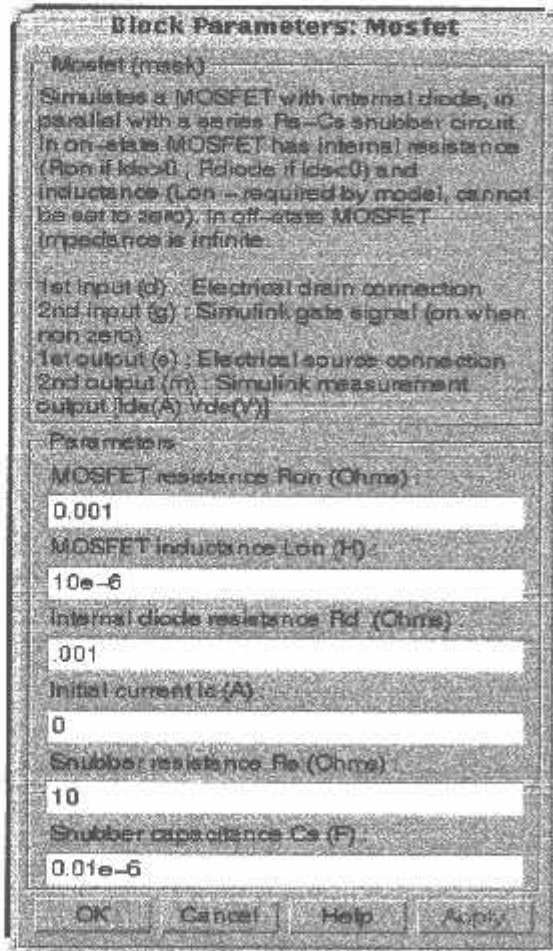
- $R_t = R_{on}$ jika $I_d > 0$, dimana R_{on} mendapatkan nilai tertentu pada bias forward resistansi konduksi Mosfet Blok
- $R_t = R_d$ jika $I_d < 0$, dimana R_d mendapatkan resistansi dioda internal.

Mosfet Blok juga berisi suatu rangkaian R_s - C_s snubber sirkit, yang biasanya dihubungkan paralel dengan Mosfet Blok. Kamu dapat menetapkan snubber untuk memberi hambatan ($C_s = \text{Inf}$) atau kapasitif

($R_s=0$). Jika kamu menetapkan baik $R_s=Inf$ maupun $C_s=0$, snubber dihapus dan hilang pada icon Mosfet.

Arus Awal I_c yang mengalir Mosfet Blok pada umumnya dimulai dari nol, sehingga simulasi dimulai dengan pemblokkan Mosfet. Bagaimanapun, harus ditetapkan suatu Nilai I_c yang sesuai dengan sirkuit. Dengan demikian semua state linier harus di-set. Initializing semua state suatu konverter power-electronic adalah suatu pertanyaan kompleks. Oleh karena itu, pilihan ini hanya bermanfaat pada sirkuit sederhana.

- Kotak Parameter Mosfet



Block Parameters: Mosfet

Mosfet (mask)
Simulates a MOSFET with internal diode, in parallel with a series R_s - C_s snubber circuit. In on-state MOSFET has internal resistance (R_{on} if $k > 0$, R_{diode} if $k < 0$) and inductance (L_{on} - required by model, cannot be set to zero). In off-state MOSFET impedance is infinite.

1st input (d): Electrical drain connection
2nd input (g): Simulink gate signal (on when non zero)
1st output (s): Electrical source connection
2nd output (m): Simulink measurement output $I_{ds}(A)$ $V_{ds}(V)$

Parameters

MOSFET resistance R_{on} (Ohms):
0.001

MOSFET inductance L_{on} (H):
10e-6

Internal diode resistance R_d (Ohms):
0.001

Initial current I_c (A):
0

Snubber resistance R_s (Ohms):
10

Snubber capacitance C_s (F):
0.01e-6

OK Cancel Help Apply

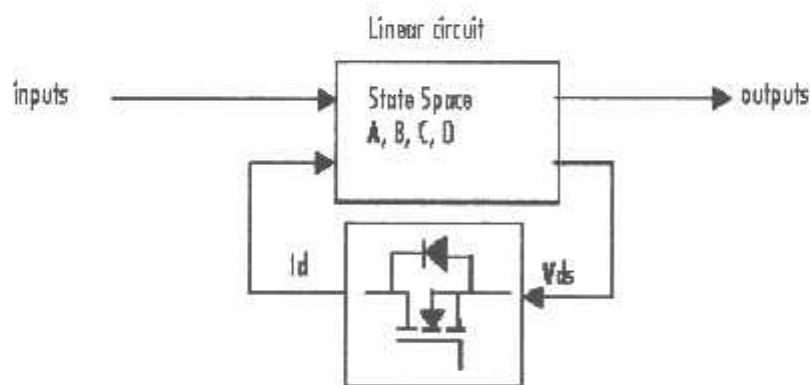
- Masukan Dan Keluaran

Keluaran dan masukan pertama Mosfet dikoneksikan ke drain (d) dan sumber (s). Masukan yang kedua (g) adalah suatu sinyal Simulink logis yang diaplikasikan pada gerbang. Keluaran yang kedua adalah suatu Simulink Garis vektor Pengukuran [I_d , V_{ds}] yang mengembalikan Voltase Dan Arus Mosfet.

- Asumsi Dan Pembatasan

Mosfet blok mengimplementasikan suatu model macro Alat Mosfet yang riil. Model macro ini tidak mempertimbangkan baik ilmu alat ukur maupun proses alam yang kompleks [1].

Di dalam Penyajian Simulink, Mosfet diperagakan sebagai elemen nonlinear yang menghubungkan dengan sirkuit linier seperti di bawah ini.



GAMBAR
SIMULINK MOSFET

Untuk menghindari suatu pengulangan secara aljabar, Mosfet Induktansi Lon tidak bisa di-set nol. Masing-Masing Mosfet menambahkan suatu state ekstra ke model sirkuit elektrik. Sejak Mosfet diperagakan sebagai sumber arus, Mosfet tidak bisa dihubungkan secara seri dengan suatu Inductor, suatu sumber arus, atau suatu sirkuit terbuka, kecuali jika digunakan suatu sirkuit snubber.

3. Kesimpulan :

1. Programmable switching power supply adalah suatu peralatan penunjang setiap kegiatan elektronika yang sangat penting apalagi jika dipakai pada keadaan yang sangat cepat tanpa perlu lagi mengeset tegangan yang hendak diminta.
 2. Penggunaan lebar pulsa variabel (PWM) yang dibangkitkan atau dikontrol oleh mikrokontroler ternyata dapat memberikan hasil regulasi/pengaturan tegangan yang baik.
 3. Trafo switching yang dipasang pada sistem ini memiliki kemampuan 2 Ampere.
 4. Output dapat diatur sesuai dengan keinginan kita yang dapat beroperasi pada frekuensi tinggi antara 1-100 Khz dan bernilai error 1,29 %.
-

4. Analisa pengujian Alat :

TABEL 4.1.
HASIL PENGUJIAN

V Set	V Out	Error (%)
0,5	0,54	8
1	1,02	2
1,5	1,55	3,33333333
2	2,06	3
2,5	2,52	0,8
3	3,03	1
3,5	3,56	1,71428571
4	4,01	0,25
4,5	4,52	0,44444444
5	5,15	3
5,5	5,52	0,36363636
6	6,02	0,33333333
6,5	6,51	0,15384615
7	7,02	0,28571429
7,5	7,54	0,53333333
8	8,03	0,375
8,5	8,57	0,82352941
9	9,05	0,55555556
9,5	9,54	0,42105263
10	10,11	1,1
10,5	10,58	0,76190476
11	11,04	0,36363636
11,5	11,54	0,34782609
12	12,22	1,83333333
12,5	12,62	0,96
13	13,23	1,76923077
13,5	13,51	0,07407407
14	14,25	1,78571429
14,5	14,6	0,68965517
15	15,25	1,66666667
Jumlah error		38,7391061

4.1. Analisa Data

$$\text{Error (\%)} = \frac{\text{Selisih tegangan}}{V_{\text{Set}}} * 100 \%$$

$$\text{Error Rata-Rata (\%)} = \frac{\sum \text{Error}}{\sum \text{Data}}$$

$$= \frac{38,73}{30}$$

$$= 1,29 \%$$

MC78XX/LM78XX/MC78XXA

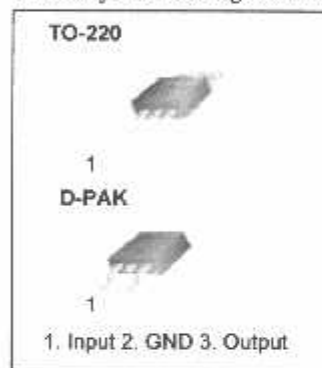
3-Terminal 1A Positive Voltage Regulator

Features

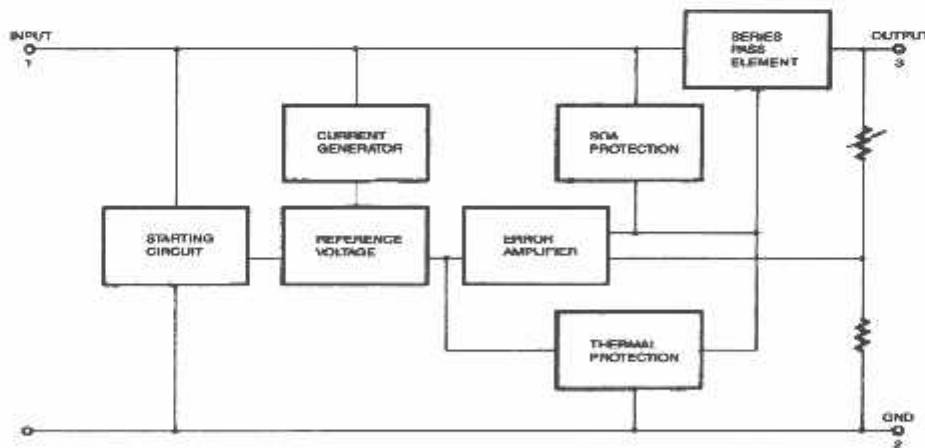
- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

Description

The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



Internal Block Diagram



Rev. 1.0.1

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage (for $V_O = 5V$ to $18V$) (for $V_O = 24V$)	V_I	35	V
	V_{I1}	40	V
Thermal Resistance Junction-Cases (TO-220)	$R_{\theta JC}$	5	$^{\circ}C/W$
Thermal Resistance Junction-Air (TO-220)	$R_{\theta JA}$	65	$^{\circ}C/W$
Operating Temperature Range	T_{OPR}	0 ~ +125	$^{\circ}C$
Storage Temperature Range	T_{STG}	-65 ~ +150	$^{\circ}C$

Electrical Characteristics (MC7805/LM7805)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	MC7805/LM7805			Unit	
			Min.	Typ.	Max.		
Output Voltage	VO	TJ =+25 °C	4.8	5.0	5.2	V	
		5.0mA ≤ IO ≤ 1.0A, PO ≤ 15W VI = 7V to 20V	4.75	5.0	5.25		
Line Regulation (Note1)	Regline	TJ=+25 °C	VO = 7V to 25V	-	4.0	100	mV
			VI = 8V to 12V	-	1.6	50	
Load Regulation (Note1)	Regload	TJ=+25 °C	IO = 5.0mA to 1.5A	-	9	100	mV
			IO =250mA to 750mA	-	4	50	
Quiescent Current	IQ	TJ =+25 °C	-	5.0	8.0	mA	
Quiescent Current Change	ΔIQ	IO = 5mA to 1.0A	-	0.03	0.5	mA	
		VI= 7V to 25V	-	0.3	1.3		
Output Voltage Drift	ΔVO/ΔT	IO= 5mA	-	-0.8	-	mV/ °C	
Output Noise Voltage	VN	f= 10Hz to 100KHz, TA=+25 °C	-	42	-	μV/VO	
Ripple Rejection	RR	f= 120Hz VO = 8V to 18V	62	73	-	dB	
Dropout Voltage	VDrop	IO = 1A, TJ =+25 °C	-	2	-	V	
Output Resistance	ro	f = 1KHz	-	15	-	mΩ	
Short Circuit Current	ISC	VI = 35V, TA =+25 °C	-	230	-	mA	
Peak Current	IPK	TJ =+25 °C	-	2.2	-	A	

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7806)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =11V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7806			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25 °C		5.75	6.0	6.25	V
		5.0mA ≤ I _O ≤ 1.0A, P _O ≤ 15W V _I = 8.0V to 21V		5.7	6.0	6.3	
Line Regulation (Note1)	Reg _{line}	T _J =+25 °C	V _I = 8V to 25V	-	5	120	mV
			V _I = 9V to 13V	-	1.5	60	
Load Regulation (Note1)	Reg _{load}	T _J =+25 °C	I _O =5mA to 1.5A	-	9	120	mV
			I _O =250mA to750A	-	3	60	
Quescent Current	I _Q	T _J =+25 °C		-	5.0	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1A		-	-	0.5	mA
		V _I = 8V to 25V		-	-	1.3	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	45	-	μV/V _O
Ripple Rejection	RR	f = 120Hz V _I = 9V to 19V		59	75	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	19	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C		-	250	-	mA
Peak Current	I _{PK}	T _J =+25 °C		-	2.2	-	A

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7808)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =14V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7808			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25 °C		7.7	8.0	8.3	V
		5.0mA ≤ I _O ≤ 1.0A, P _O ≤ 15W V _I = 10.5V to 23V		7.6	8.0	8.4	
Line Regulation (Note1)	Reg _{line}	T _J =+25 °C	V _I = 10.5V to 25V	-	5.0	160	mV
			V _I = 11.5V to 17V	-	2.0	80	
Load Regulation (Note1)	Reg _{load}	T _J =+25 °C	I _O = 5.0mA to 1.5A	-	10	160	mV
			I _O = 250mA to 750mA	-	5.0	80	
Quiescent Current	I _Q	T _J =+25 °C		-	5.0	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		-	0.05	0.5	mA
		V _I = 10.5A to 25V		-	0.5	1.0	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-0.8	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	52	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, V _I = 11.5V to 21.5V		56	73	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C		-	230	-	mA
Peak Current	I _{PK}	T _J =+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7809)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =15V, C_I= 0.33μF, C_O= 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7809			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25°C		8.65	9	9.35	V
		5.0mA ≤ I _O ≤1.0A, P _O ≤15W V _I = 11.5V to 24V		8.6	9	9.4	
Line Regulation (Note1)	Regline	T _J =+25°C	V _I = 11.5V to 25V	-	6	180	mV
			V _I = 12V to 17V	-	2	90	
Load Regulation (Note1)	Regload	T _J =+25°C	I _O = 5mA to 1.5A	-	12	180	mV
			I _O = 250mA to 750mA	-	4	90	
Quiescent Current	I _Q	T _J =+25°C		-	5.0	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		-	-	0.5	mA
		V _I = 11.5V to 26V		-	-	1.3	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-1	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	58	-	μV/V _O
Ripple Rejection	RR	f = 120Hz V _I = 13V to 23V		56	71	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25°C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25°C		-	250	-	mA
Peak Current	I _{PK}	T _J = +25°C		-	2.2	-	A

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7810)

(Refer to test circuit ,0°C< T_J < 125°C, I_O = 500mA, V_I =16V, C_I= 0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7810			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25 °C		9.6	10	10.4	V
		5.0mA ≤ I _O ≤1.0A, P _O ≤15W V _I = 12.5V to 25V		9.5	10	10.5	
Line Regulation (Note1)	Regline	T _J =+25°C	V _I = 12.5V to 25V	-	10	200	mV
			V _I = 13V to 25V	-	3	100	
Load Regulation (Note1)	Regload	T _J =+25°C	I _O = 5mA to 1.5A	-	12	200	mV
			I _O = 250mA to 750mA	-	4	400	
Quiescent Current	I _Q	T _J =+25°C		-	5.1	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		-	-	0.5	mA
		V _I = 12.5V to 29V		-	-	1.0	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-1	-	mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	58	-	μV/V _O
Ripple Rejection	RR	f = 120Hz V _I = 13V to 23V		56	71	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C		-	250	-	mA
Peak Current	I _{PK}	T _J =+25 °C		-	2.2	-	A

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7812)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =19V, C_I= 0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7812			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25 °C		11.5	12	12.5	V
		5.0mA ≤ I _O ≤1.0A, P _O ≤15W V _I = 14.5V to 27V		11.4	12	12.6	
Line Regulation (Note1)	Regline	T _J =+25 °C	V _I = 14.5V to 30V	-	10	240	mV
			V _I = 16V to 22V	-	3.0	120	
Load Regulation (Note1)	Regload	T _J =+25 °C	I _O = 5mA to 1.5A	-	11	240	mV
			I _O = 250mA to 750mA	-	5.0	120	
Quiescent Current	I _Q	T _J =+25 °C		-	5.1	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		-	0.1	0.5	mA
		V _I = 14.5V to 30V		-	0.5	1.0	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-1	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	76	-	μV/V _O
Ripple Rejection	RR	f = 120Hz V _I = 15V to 25V		55	71	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	18	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C		-	230	-	mA
Peak Current	I _{PK}	T _J = +25 °C		-	2.2	-	A

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7815)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =23V, C_I= 0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7815			Unit
				Min.	Typ.	Max.	
Output Voltage	VO	TJ =+25 °C		14.4	15	15.6	V
		5.0mA ≤ IO ≤ 1.0A, PO ≤ 15W VI = 17.5V to 30V		14.25	15	15.75	
Line Regulation (Note1)	Regline	TJ =+25 °C	VI = 17.5V to 30V	-	11	300	mV
			VI = 20V to 26V	-	3	150	
Load Regulation (Note1)	Regload	TJ =+25 °C	IO = 5mA to 1.5A	-	12	300	mV
			IO = 250mA to 750mA	-	4	150	
Quiescent Current	IQ	TJ =+25 °C		-	5.2	8.0	mA
Quiescent Current Change	ΔIQ	IO = 5mA to 1.0A		-	-	0.5	mA
		VI = 17.5V to 30V		-	-	1.0	
Output Voltage Drift	ΔVO/ΔT	IO = 5mA		-	-1	-	mV/°C
Output Noise Voltage	VN	f = 10Hz to 100KHz, TA =+25 °C		-	90	-	μV/VO
Ripple Rejection	RR	f = 120Hz VI = 18.5V to 28.5V		54	70	-	dB
Dropout Voltage	VDrop	IO = 1A, TJ =+25 °C		-	2	-	V
Output Resistance	ro	f = 1KHz		-	19	-	mΩ
Short Circuit Current	ISC	VI = 35V, TA =+25 °C		-	250	-	mA
Peak Current	IPK	TJ =+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7818)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =27V, C_I= 0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7818			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25 °C		17.3	18	18.7	V
		5.0mA ≤ I _O ≤1.0A, P _O ≤15W V _I = 21V to 33V		17.1	18	18.9	
Line Regulation (Note1)	Regline	T _J =+25 °C	V _I = 21V to 33V	-	15	360	mV
			V _I = 24V to 30V	-	5	180	
Load Regulation (Note1)	Regload	T _J =+25 °C	I _O = 5mA to 1.5A	-	15	360	mV
			I _O = 250mA to 750mA	-	5.0	180	
Quiescent Current	I _Q	T _J =+25 °C		-	5.2	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		-	-	0.5	mA
		V _I = 21V to 33V		-	-	1	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-1	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	110	-	μV/V _O
Ripple Rejection	RR	f = 120Hz V _I = 22V to 32V		53	69	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	22	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C		-	250	-	mA
Peak Current	I _{PK}	T _J =+25 °C		-	2.2	-	A

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7824)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =33V, C_I= 0.33μF, C_O=0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions		MC7824			Unit
				Min.	Typ.	Max.	
Output Voltage	V _O	T _J =+25 °C		23	24	25	V
		5.0mA ≤ I _O ≤ 1.0A, P _O ≤ 15W V _I = 27V to 38V		22.8	24	25.25	
Line Regulation (Note1)	Regline	T _J =+25 °C	V _I = 27V to 38V	-	17	480	mV
			V _I = 30V to 36V	-	6	240	
Load Regulation (Note1)	Regload	T _J =+25 °C	I _O = 5mA to 1.5A	-	15	480	mV
			I _O = 250mA to 750mA	-	5.0	240	
Quiescent Current	I _Q	T _J =+25 °C		-	5.2	8.0	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1.0A		-	0.1	0.5	mA
		V _I = 27V to 38V		-	0.5	1	
Output Voltage Drift	ΔV _O /ΔT	I _O = 5mA		-	-1.5	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz, T _A =+25 °C		-	60	-	μV/V _O
Ripple Rejection	RR	f = 120Hz V _I = 28V to 38V		50	67	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J =+25 °C		-	2	-	V
Output Resistance	r _O	f = 1KHz		-	28	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A =+25 °C		-	230	-	mA
Peak Current	I _{PK}	T _J =+25 °C		-	2.2	-	A

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7805A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 10V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	4.9	5	5.1	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 7.5V to 20V	4.8	5	5.2	
Line Regulation (Note1)	Regline	V _I = 7.5V to 25V I _O = 500mA	-	5	50	mV
		V _I = 8V to 12V	-	3	50	
		T _J = +25 °C	-	5	50	
				1.5	25	
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.5A	-	9	100	mV
		I _O = 5mA to 1A	-	9	100	
		I _O = 250mA to 750mA	-	4	50	
			-			
Quiescent Current	I _Q	T _J = +25 °C	-	5.0	6	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1A	-	-	0.5	mA
		V _I = 8 V to 25V, I _O = 500mA	-	-	0.8	
		V _I = 7.5V to 20V, T _J = +25 °C	-	-	0.8	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-0.8	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 8V to 18V	-	68	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2	-	V
Output Resistance	r _O	f = 1KHz	-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

Note:
1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7806A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 11V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	5.58	6	6.12	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 8.6V to 21V	5.76	6	6.24	
Line Regulation (Note1)	Regline	V _I = 8.6V to 25V I _O = 500mA	-	5	60	mV
		V _I = 9V to 13V	-	3	60	
		T _J = +25 °C	V _I = 8.3V to 21V	5	60	
			V _I = 9V to 13V	1.5	30	
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.5A	-	9	100	mV
		I _O = 5mA to 1A	-	4	100	
		I _O = 250mA to 750mA	-	5.0	50	
Quiescent Current	I _Q	T _J = +25 °C	-	4.3	6	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1A	-	-	0.5	mA
		V _I = 9V to 25V, I _O = 500mA	-	-	0.8	
		V _I = 8.5V to 21V, T _J = +25 °C	-	-	0.8	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-0.8	-	mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 9V to 19V	-	65	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2	-	V
Output Resistance	r _O	f = 1KHz	-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

Note:
1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7808A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 14V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	7.84	8	8.16	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 10.6V to 23V	7.7	8	8.3	
Line Regulation (Note1)	Regline	V _I = 10.6V to 25V I _O = 500mA	-	6	80	mV
		V _I = 11V to 17V	-	3	80	
		T _J = +25 °C	V _I = 10.4V to 23V	-	6	80
			V _I = 11V to 17V	-	2	40
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.5A	-	12	100	mV
		I _O = 5mA to 1A	-	12	100	
		I _O = 250mA to 750mA	-	5	50	
Quiescent Current	I _Q	T _J = +25 °C	-	5.0	6	mA
Quiescent Current Change	ΔI _Q	I _O = 5mA to 1A	-	-	0.5	mA
		V _I = 11V to 25V, I _O = 500mA	-	-	0.8	
		V _I = 10.6V to 23V, T _J = +25 °C	-	-	0.8	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-0.8	-	mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 11.5V to 21.5V	-	62	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2	-	V
Output Resistance	r _O	f = 1KHz	-	18	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

Note:
1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7809A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 15V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	8.82	9.0	9.18	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 11.2V to 24V	8.65	9.0	9.35	
Line Regulation (Note1)	Regline	V _I = 11.7V to 25V I _O = 500mA	-	6	90	mV
		V _I = 12.5V to 19V	-	4	45	
		T _J = +25 °C	V _I = 11.5V to 24V	6	90	
			V _I = 12.5V to 19V	2	45	
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.0A	-	12	100	mV
		I _O = 5mA to 1.0A	-	12	100	
		I _O = 250mA to 750mA	-	5	50	
Quiescent Current	I _Q	T _J = +25 °C	-	5.0	6.0	mA
Quiescent Current Change	ΔI _Q	V _I = 11.7V to 25V, T _J = +25 °C	-	-	0.8	mA
		V _I = 12V to 25V, I _O = 500mA	-	-	0.8	
		I _O = 5mA to 1.0A	-	-	0.5	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-1.0	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 12V to 22V	-	62	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2.0	-	V
Output Resistance	r _O	f = 1KHz	-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

Note:
1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7810A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 16V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	9.8	10	10.2	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 12.8V to 25V	9.6	10	10.4	
Line Regulation (Note1)	Regline	V _I = 12.8V to 26V I _O = 500mA	-	8	100	mV
		V _I = 13V to 20V	-	4	50	
		T _J = +25 °C	-	8	100	
				3	50	
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.5A	-	12	100	mV
		I _O = 5mA to 1.0A	-	12	100	
		I _O = 250mA to 750mA	-	5	50	
			-			
Quiescent Current	I _Q	T _J = +25 °C	-	5.0	6.0	mA
Quiescent Current Change	ΔI _Q	V _I = 13V to 26V, T _J = +25 °C	-	-	0.5	mA
		V _I = 12.8V to 25V, I _O = 500mA	-	-	0.8	
		I _O = 5mA to 1.0A	-	-	0.5	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-1.0	-	mV/ °C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 14V to 24V	-	62	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2.0	-	V
Output Resistance	r _O	f = 1KHz	-	17	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

Note:
1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7812A)

(Refer to the test circuits, 0°C < T_J < 125°C, I_O = 1A, V_I = 19V, C_I = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	11.75	12	12.25	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 14.8V to 27V	11.5	12	12.5	
Line Regulation (Note1)	Regline	V _I = 14.8V to 30V I _O = 500mA	-	10	120	mV
		V _I = 16V to 22V	-	4	120	
		T _J = +25 °C	V _I = 14.5V to 27V	10	120	
			V _I = 16V to 22V	3	60	
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.5A	-	12	100	mV
		I _O = 5mA to 1.0A	-	12	100	
		I _O = 250mA to 750mA	-	5	50	
Quiescent Current	I _Q	T _J = +25 °C	-	5.1	6.0	mA
Quiescent Current Change	ΔI _Q	V _I = 15V to 30V, T _J = +25 °C	-		0.8	mA
		V _I = 14V to 27V, I _O = 500mA	-		0.8	
		I _O = 5mA to 1.0A	-		0.5	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-1.0	-	mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 14V to 24V	-	60	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2.0	-	V
Output Resistance	r _O	f = 1KHz	-	18	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

Note:
1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7815A)

(Refer to the test circuits. $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $I_O = 1\text{A}$, $V_I = 23\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	14.7	15	15.3	V
		$I_O = 5\text{mA to } 1\text{A}$, $P_O \leq 15\text{W}$ $V_I = 17.7\text{V to } 30\text{V}$	14.4	15	15.6	
Line Regulation (Note1)	Regline	$V_I = 17.9\text{V to } 30\text{V}$ $I_O = 500\text{mA}$	-	10	150	mV
		$V_I = 20\text{V to } 26\text{V}$	-	5	150	
		$T_J = +25^{\circ}\text{C}$	$V_I = 17.5\text{V to } 30\text{V}$	-	11	150
			$V_I = 20\text{V to } 26\text{V}$	-	3	75
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$ $I_O = 5\text{mA to } 1.5\text{A}$	-	12	100	mV
		$I_O = 5\text{mA to } 1.0\text{A}$	-	12	100	
		$I_O = 250\text{mA to } 750\text{mA}$	-	5	50	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.2	6.0	mA
Quiescent Current Change	ΔI_Q	$V_I = 17.5\text{V to } 30\text{V}$, $T_J = +25^{\circ}\text{C}$	-	-	0.8	mA
		$V_I = 17.5\text{V to } 30\text{V}$, $I_O = 500\text{mA}$	-	-	0.8	
		$I_O = 5\text{mA to } 1.0\text{A}$	-	-	0.5	
Output Voltage Drift	$\Delta V/\Delta T$	$I_O = 5\text{mA}$	-	-1.0	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{KHz}$ $T_A = +25^{\circ}\text{C}$	-	10	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 18.5\text{V to } 28.5\text{V}$	-	58	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2.0	-	V
Output Resistance	r_O	$f = 1\text{KHz}$	-	19	-	m Ω
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7818A)

(Refer to the test circuits. 0°C < T_J < 125°C, I_O = 1A, V_I = 27V, C_P = 0.33μF, C_O = 0.1μF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V _O	T _J = +25 °C	17.64	18	18.36	V
		I _O = 5mA to 1A, P _O ≤ 15W V _I = 21V to 33V	17.3	18	18.7	
Line Regulation (Note1)	Regline	V _I = 21V to 33V I _O = 500mA	-	15	180	mV
		V _I = 21V to 33V	-	5	180	
		T _J = +25 °C	V _I = 20.6V to 33V	-	15	180
			V _I = 24V to 30V	-	5	90
Load Regulation (Note1)	Regload	T _J = +25 °C I _O = 5mA to 1.5A	-	15	100	mV
		I _O = 5mA to 1.0A	-	15	100	
		I _O = 250mA to 750mA	-	7	50	
Quiescent Current	I _Q	T _J = +25 °C	-	5.2	6.0	mA
Quiescent Current Change	ΔI _Q	V _I = 21V to 33V, T _J = +25 °C	-	-	0.8	mA
		V _I = 21V to 33V, I _O = 500mA	-	-	0.8	
		I _O = 5mA to 1.0A	-	-	0.5	
Output Voltage Drift	ΔV/ΔT	I _O = 5mA	-	-1.0	-	mV/°C
Output Noise Voltage	V _N	f = 10Hz to 100KHz T _A = +25 °C	-	10	-	μV/V _O
Ripple Rejection	RR	f = 120Hz, I _O = 500mA V _I = 22V to 32V	-	57	-	dB
Dropout Voltage	V _{Drop}	I _O = 1A, T _J = +25 °C	-	2.0	-	V
Output Resistance	r _O	f = 1KHz	-	19	-	mΩ
Short Circuit Current	I _{SC}	V _I = 35V, T _A = +25 °C	-	250	-	mA
Peak Current	I _{PK}	T _J = +25 °C	-	2.2	-	A

Note:
1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Electrical Characteristics (MC7824A)

(Refer to the test circuits. $0^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $I_O = 1\text{A}$, $V_I = 33\text{V}$, $C_I = 0.33\mu\text{F}$, $C_O = 0.1\mu\text{F}$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_O	$T_J = +25^{\circ}\text{C}$	23.5	24	24.5	V
		$I_O = 5\text{mA to } 1\text{A}$, $P_O \leq 15\text{W}$ $V_I = 27.3\text{V to } 38\text{V}$	23	24	25	
Line Regulation (Note1)	Regline	$V_I = 27\text{V to } 38\text{V}$ $I_O = 500\text{mA}$	-	18	240	mV
		$V_I = 21\text{V to } 33\text{V}$	-	6	240	
		$T_J = +25^{\circ}\text{C}$	$V_I = 26.7\text{V to } 38\text{V}$	-	18	240
			$V_I = 30\text{V to } 36\text{V}$	-	6	120
Load Regulation (Note1)	Regload	$T_J = +25^{\circ}\text{C}$ $I_O = 5\text{mA to } 1.5\text{A}$	-	15	100	mV
		$I_O = 5\text{mA to } 1.0\text{A}$	-	15	100	
		$I_O = 250\text{mA to } 750\text{mA}$	-	7	50	
Quiescent Current	I_Q	$T_J = +25^{\circ}\text{C}$	-	5.2	6.0	mA
Quiescent Current Change	ΔI_Q	$V_I = 27.3\text{V to } 38\text{V}$, $T_J = +25^{\circ}\text{C}$	-	-	0.8	mA
		$V_I = 27.3\text{V to } 38\text{V}$, $I_O = 500\text{mA}$	-	-	0.8	
		$I_O = 5\text{mA to } 1.0\text{A}$	-	-	0.5	
Output Voltage Drift	$\Delta V/\Delta T$	$I_O = 5\text{mA}$	-	-1.5	-	mV/ $^{\circ}\text{C}$
Output Noise Voltage	V_N	$f = 10\text{Hz to } 100\text{KHz}$ $T_A = 25^{\circ}\text{C}$	-	10	-	$\mu\text{V}/V_O$
Ripple Rejection	RR	$f = 120\text{Hz}$, $I_O = 500\text{mA}$ $V_I = 28\text{V to } 38\text{V}$	-	54	-	dB
Dropout Voltage	V_{Drop}	$I_O = 1\text{A}$, $T_J = +25^{\circ}\text{C}$	-	2.0	-	V
Output Resistance	r_O	$f = 1\text{KHz}$	-	20	-	$\text{m}\Omega$
Short Circuit Current	I_{SC}	$V_I = 35\text{V}$, $T_A = +25^{\circ}\text{C}$	-	250	-	mA
Peak Current	I_{PK}	$T_J = +25^{\circ}\text{C}$	-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Typical Performance Characteristics

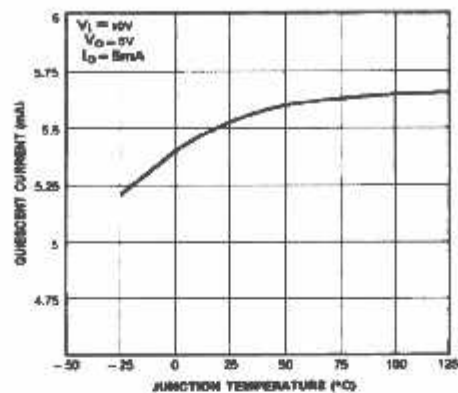


Figure 1. Quiescent Current

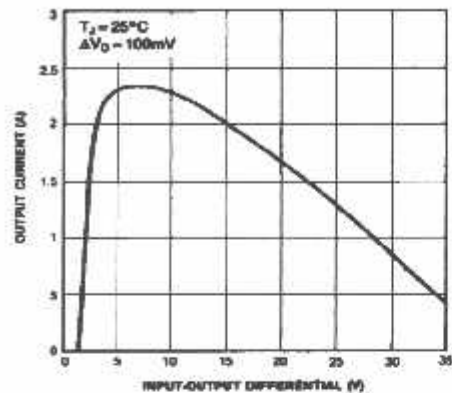


Figure 2. Peak Output Current

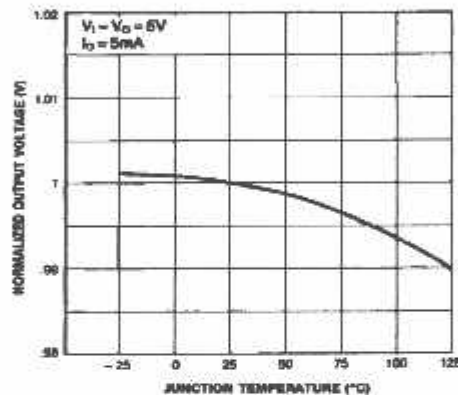


Figure 3. Output Voltage

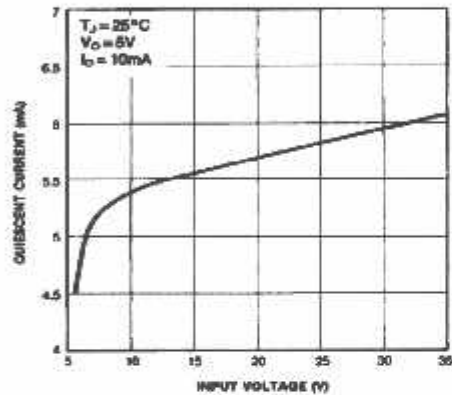


Figure 4. Quiescent Current

Typical Applications

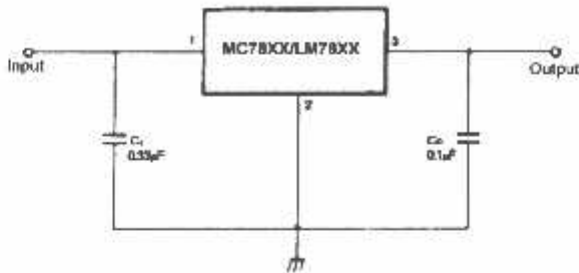


Figure 5. DC Parameters

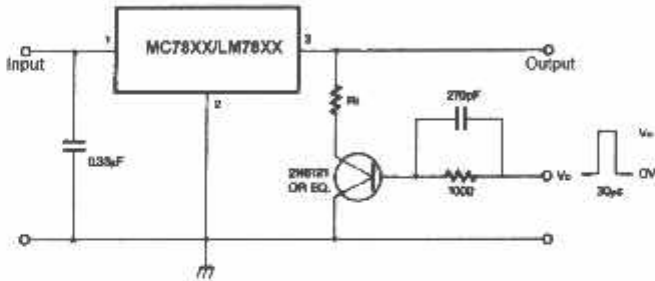


Figure 6. Load Regulation

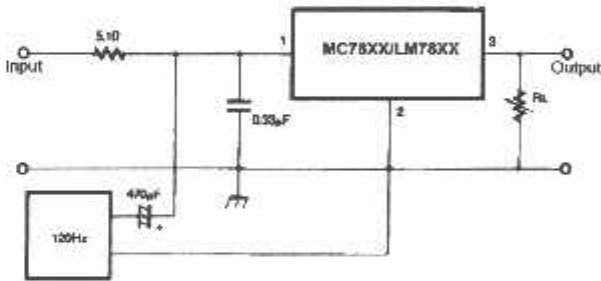


Figure 7. Ripple Rejection

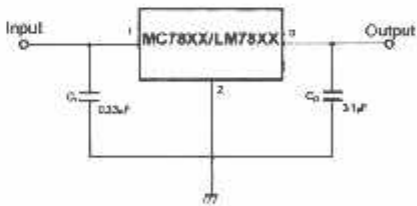


Figure 8. Fixed Output Regulator

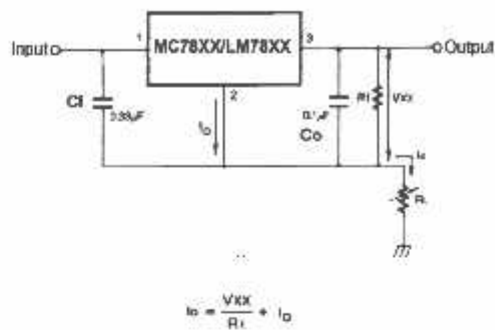
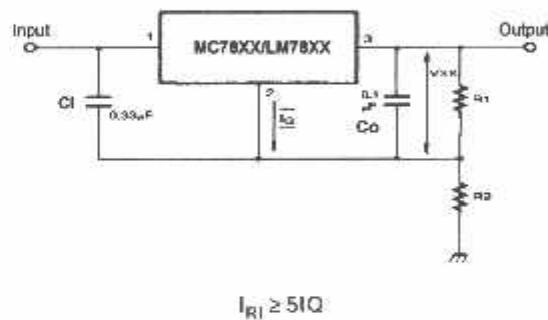


Figure 9. Constant Current Regulator

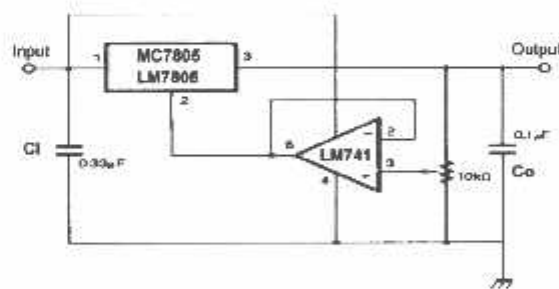
Notes:

- (1) To specify an output voltage, substitute voltage value for "XX." A common ground is required between the input and the Output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.
- (2) C1 is required if regulator is located an appreciable distance from power Supply filter.
- (3) C0 improves stability and transient response.



$$V_O = V_{XX}(1+R_2/R_1)+I_0R_2$$

Figure 10. Circuit for Increasing Output Voltage



$$V_O = V_{XX}(1+R_2/R_1)+I_0R_2$$

Figure 11. Adjustable Output Regulator (7 to 30V)

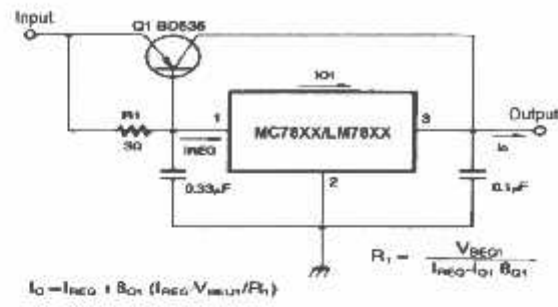


Figure 12. High Current Voltage Regulator

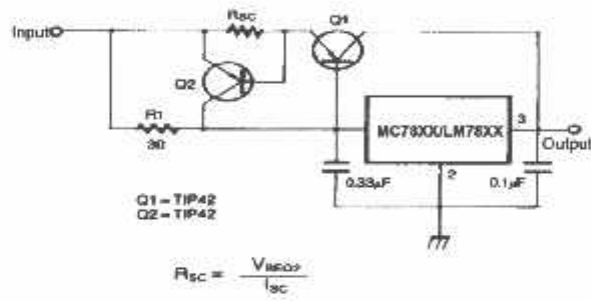


Figure 13. High Output Current with Short Circuit Protection

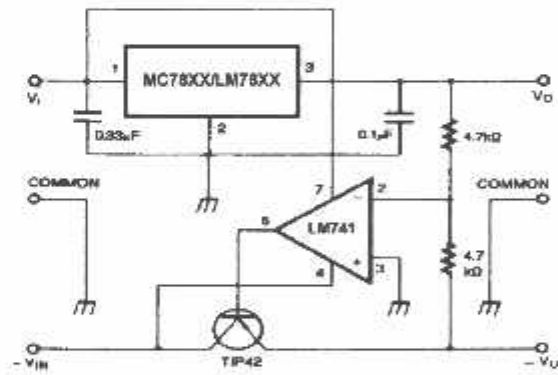


Figure 14. Tracking Voltage Regulator

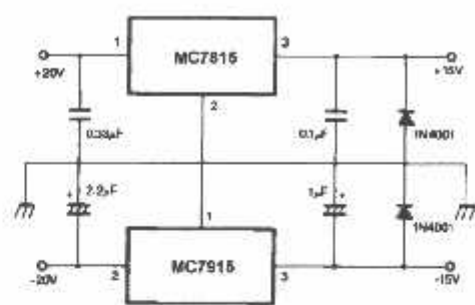


Figure 15. Split Power Supply (±15V-1A)

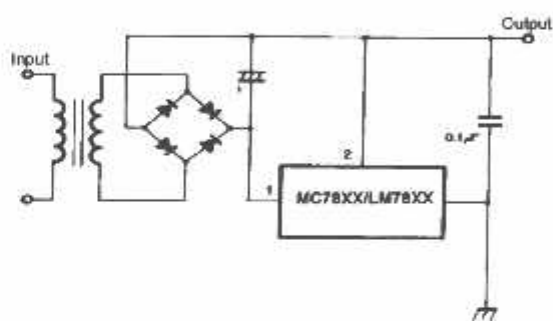


Figure 16. Negative Output Voltage Circuit

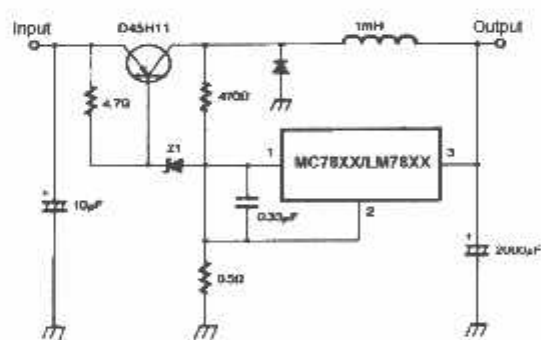


Figure 17. Switching Regulator

Ordering Information

Product Number	Output Voltage Tolerance	Package	Operating Temperature
LM7805CT	±4%	TO-220	0 ~ + 125°C

Product Number	Output Voltage Tolerance	Package	Operating Temperature
MC7805CT	+4%	TO-220	0 ~ + 125°C
MC7806CT			
MC7808CT			
MC7809CT			
MC7810CT			
MC7812CT			
MC7815CT			
MC7818CT			
MC7824CT			
MC7805CDT		D-PAK	
MC7806CDT			
MC7808CDT			
MC7809CDT			
MC7810CDT			
MC7812CDT	±2%	TO-220	
MC7805ACT			
MC7806ACT			
MC7808ACT			
MC7809ACT			
MC7810ACT			
MC7812ACT			
MC7815ACT			
MC7818ACT			
MC7824ACT			

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit μ P Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS808DA derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

- Compatible with 8080 μ P derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"

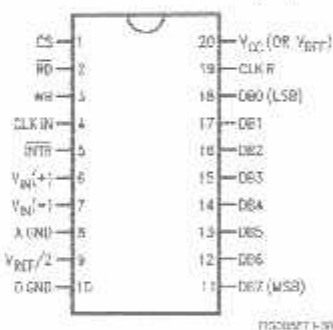
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DD} , 2.5 V_{DD} , or analog span adjusted voltage reference

Key Specifications

- Resolution 8 bits
- Total error $\pm 1/4$ LSB, $\pm 1/2$ LSB and ± 1 LSB
- Conversion time 100 μ s

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages



See Ordering Information

Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	-40°C TO +85°C
ERROR	$\pm 1/4$ Bit Adjusted			ADC0801LCN
	$\pm 1/2$ Bit Unadjusted	ADC0802LCWM		ADC0802LCN
	$\pm 1/4$ Bit Adjusted			ADC0803LCN
	± 1 Bit Unadjusted	ADC0804LCWM	ADC0804LCN	ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B—Small Outline	N20A	Molded DIP

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AD08000001

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ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit μ P Compatible A/D Converters

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	-0.3V to +18V
All Other Input and Outputs	-0.3V to ($V_{CC}+0.3V$)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C

Infrared (15 seconds)	220°C
Storage Temperature Range	-65°C to +150°C
Package Dissipation at $T_A=25^\circ\text{C}$	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0804LCJ	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
ADC0801/02/03/05LCN	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
ADC0804LCN	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
ADC0802/04LCWM	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for $V_{CC}=5 V_{DC}$, $T_{MIN} \leq T_A \leq T_{MAX}$ and $f_{CLK}=640 \text{ kHz}$ unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			$\pm 1/4$	LSB
DC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2=2.500 V_{DC}$			$\pm 1/2$	LSB
DC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			$\pm 1/2$	LSB
DC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2=2.500 V_{DC}$			± 1	LSB
DC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$ -No Connection			± 1	LSB
$R_{IF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05	2.5	8.0		k Ω
	ADC0804 (Note 9)	0.75	1.1		k Ω
Analog Input Voltage Range	(Note 4) $V(+)$ or $V(-)$	Gnd-0.05		$V_{CC}+0.05$	V_{DC}
Common-Mode Error	Over Analog Input Voltage Range		$\pm 1/16$	$\pm 1/8$	LSB
Power Supply Sensitivity	$V_{CC}=5 V_{DC} \pm 10\%$ Over Allowed $V_{IN}(-)$ and $V_{IN}(+)$ Voltage Range (Note 4)		$\pm 1/16$	$\pm 1/8$	LSB

AC Electrical Characteristics

The following specifications apply for $V_{CC}=5 V_{DC}$ and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Conversion Time	$f_{CLK}=640 \text{ kHz}$ (Note 6)	103		114	μs
	Conversion Time	(Notes 5, 6)	66		73	$1/f_{CLK}$
	Clock Frequency	$V_{CC}=5V$, (Note 5)	100	640	1460	kHz
	Clock Duty Cycle		40		60	%
	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}=0 V_{DC}$, $f_{CLK}=640 \text{ kHz}$	8770		9708	conv/s
t_{SL}	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}=0 V_{DC}$ (Note 7)	100			ns
	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L=100 \text{ pF}$		135	200	ns
t_{OH}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$C_L=10 \text{ pF}$, $R_L=10k$ (See TRI-STATE Test Circuits)		125	200	ns
t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
	Input Capacitance of Logic Control Inputs			5	7.5	pF

AC Electrical Characteristics (Continued)

The following specifications apply for $V_{DD}=5\text{ V}_{DD}$ and $T_{MIN}\leq T_A\leq T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
$V_{IN}(1)$	Logical "1" Input Voltage (Except Pin 4 CLK IN)	$V_{CC}=5.25\text{ V}_{DD}$	2.0		15	V_{IK}
$V_{IN}(0)$	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V_{CC}=4.75\text{ V}_{DD}$			0.8	V_{DC}
$I_{IN}(1)$	Logical "1" Input Current (All Inputs)	$V_{IN}=5\text{ V}_{DD}$		0.005	1	μA_{DC}
$I_{IN}(0)$	Logical "0" Input Current (All Inputs)	$V_{IN}=0\text{ V}_{DD}$	-1	-0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_{+}	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DD}
V_{-}	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DD}
V_H	CLK IN (Pin 4) Hysteresis (V_{+})-(V ₋)		0.6	1.3	2.0	V_{DD}
$V_{OUT}(0)$	Logical "0" CLK R Output Voltage	$I_O=360\text{ }\mu A$ $V_{CC}=4.75\text{ V}_{DD}$			0.4	V_{DD}
$V_{OUT}(1)$	Logical "1" CLK R Output Voltage	$I_O=-360\text{ }\mu A$ $V_{CC}=4.75\text{ V}_{DD}$	2.4			V_{DD}
DATA OUTPUTS AND INTR						
$V_{OUT}(0)$	Logical "0" Output Voltage Data Outputs INTR Output	$I_{OUT}=1.6\text{ mA}$, $V_{CC}=4.75\text{ V}_{DD}$ $I_{OUT}=1.0\text{ mA}$, $V_{CC}=4.75\text{ V}_{DD}$			0.4 0.4	V_{DD} V_{DD}
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O=-360\text{ }\mu A$, $V_{CC}=4.75\text{ V}_{DD}$	2.4			V_{DD}
$V_{OUT}(1)$	Logical "1" Output Voltage	$I_O=-10\text{ }\mu A$, $V_{CC}=4.75\text{ V}_{DD}$	4.5			V_{DD}
I_{RXD}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT}=0\text{ V}_{DD}$ $V_{OUT}=5\text{ V}_{DD}$	-3		3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, $T_A=25^\circ C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{DD} , $T_A=25^\circ C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current)	$f_{CLK}=640\text{ kHz}$, $V_{REF}/2=NC$, $T_A=25^\circ C$ and $\overline{CS}=5V$				
	ADC0801/02/03/04/LCJ/05			1.1	1.8	mA
	ADC0804/LCN/LCWM			1.9	2.5	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DD} .

Note 4: For $V_{IN}(1)\geq V_{IN}(1)$ the digital output code will be 0000000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DD} to 5 V_{DD} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DD} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at $f_{CLK}=640\text{ kHz}$. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see Figure 4 and section 2.0.

AC Electrical Characteristics (Continued)

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

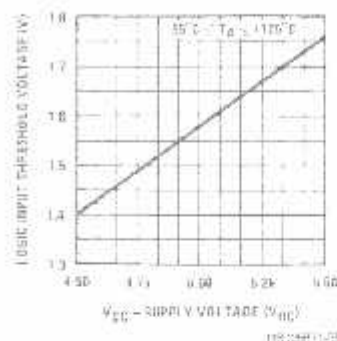
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and Figure 7.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804(C), each resistor is typically 16 k Ω . In all versions of the ADC0804 except the ADC0804(C), each resistor is typically 2.2 k Ω .

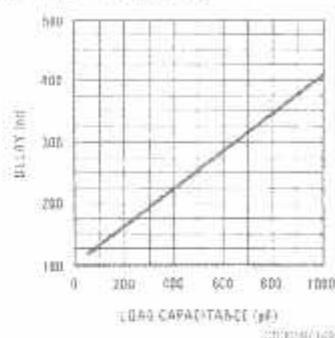
Note 10: Human body model, 100 pF discharged through a 1.5 k Ω resistor

Typical Performance Characteristics

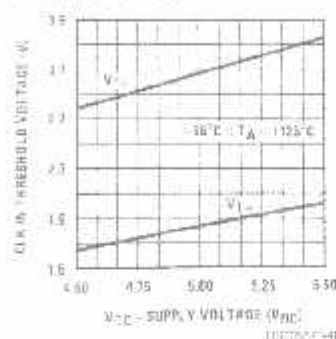
Logic Input Threshold Voltage vs. Supply Voltage



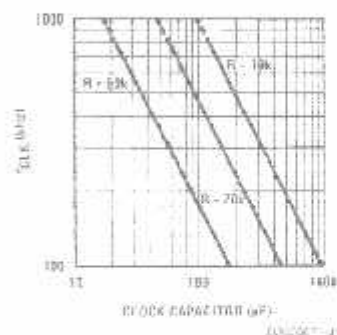
Delay From Falling Edge of RD to Output Data Valid vs. Load Capacitance



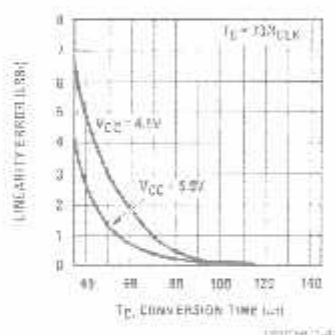
CLK IN Schmitt Trip Levels vs. Supply Voltage



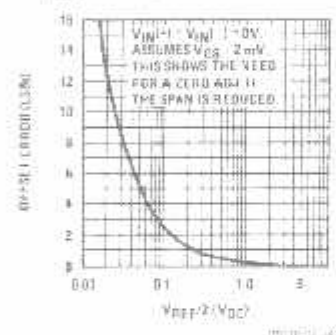
CLK vs. Clock Capacitor



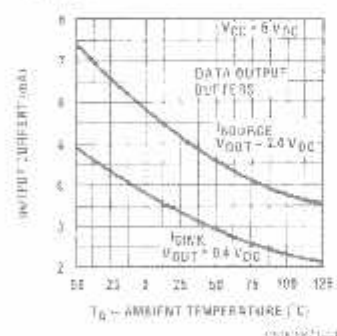
Full-Scale Error vs Conversion Time



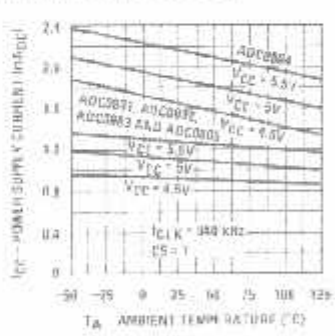
Effect of Unadjusted Offset Error vs. V_REF/2 Voltage



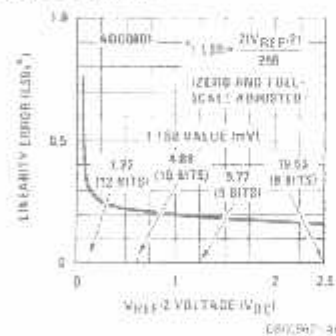
Output Current vs Temperature



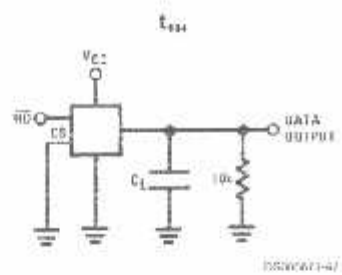
Power Supply Current vs Temperature (Note 8)



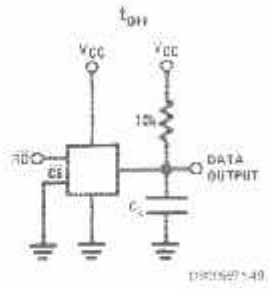
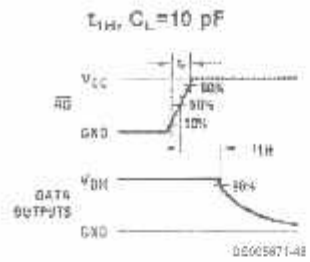
Linearity Error at Low V_REF/2 Voltages



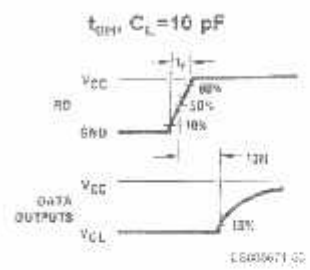
TRI-STATE Test Circuits and Waveforms



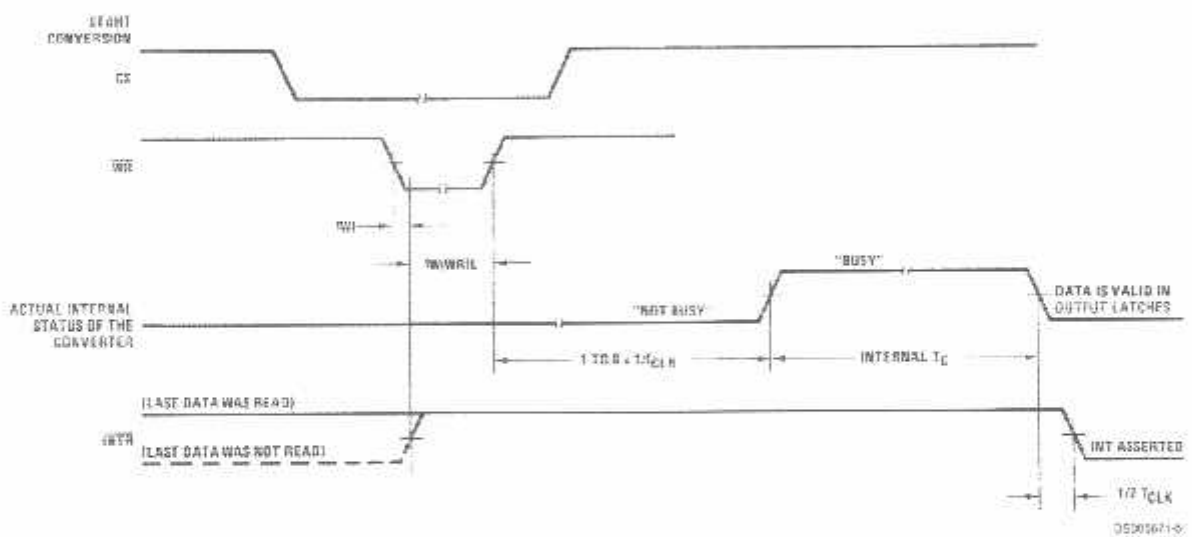
$t_1 = 20 \text{ ns}$



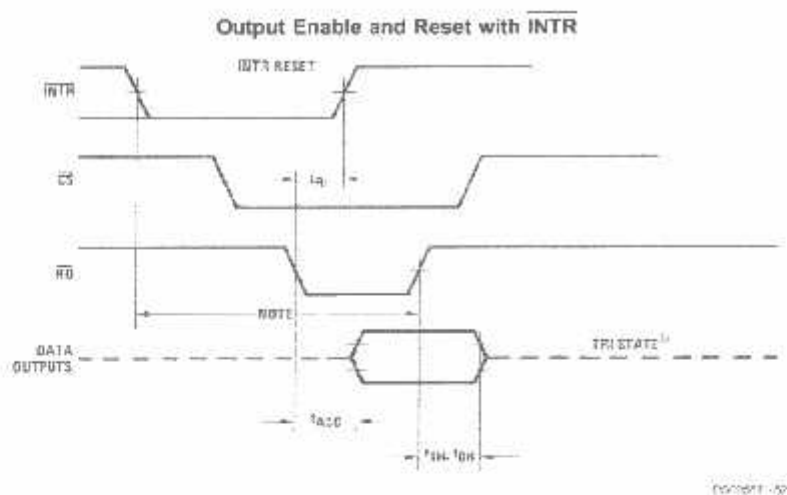
$t_0 = 20 \text{ ns}$



Timing Diagrams (All timing is measured from the 50% voltage points)

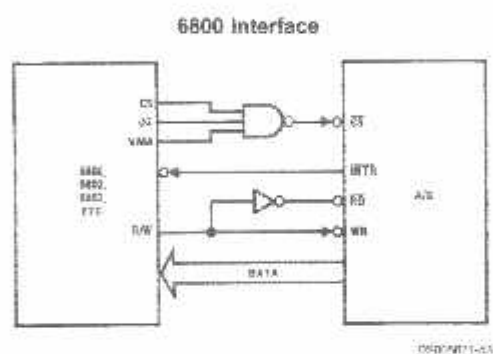


Timing Diagrams (All timing is measured from the 50% voltage points) (Continued)



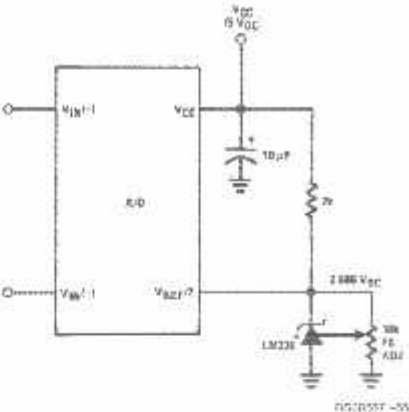
Note: Read strobe must occur 3 clock periods ($3/t_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{\text{INTR}}$.

Typical Applications



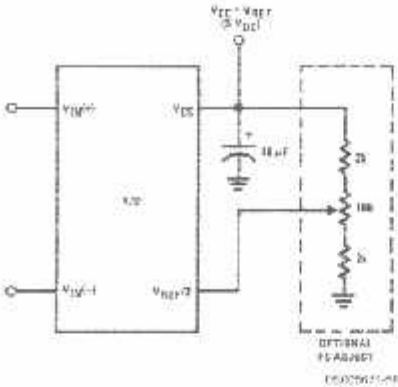
Typical Applications (Continued)

Absolute with a 2.500V Reference

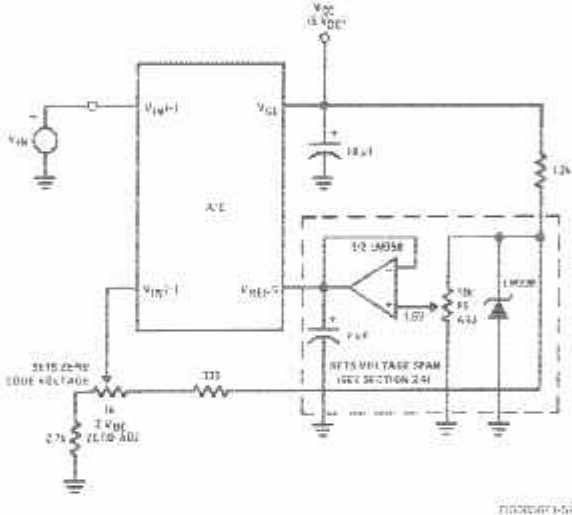


*For low power, see also LM385-2.5

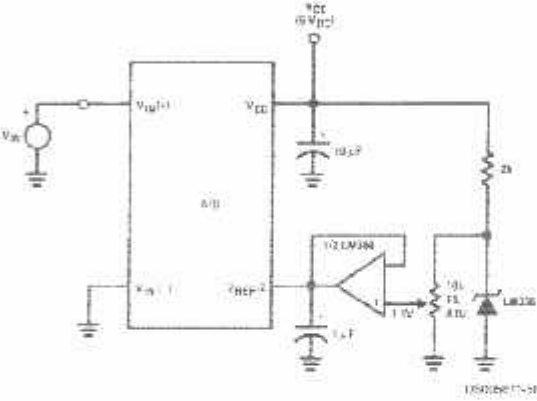
Absolute with a 5V Reference



Zero-Shift and Span Adjust: $2V < V_{IN} < 5V$



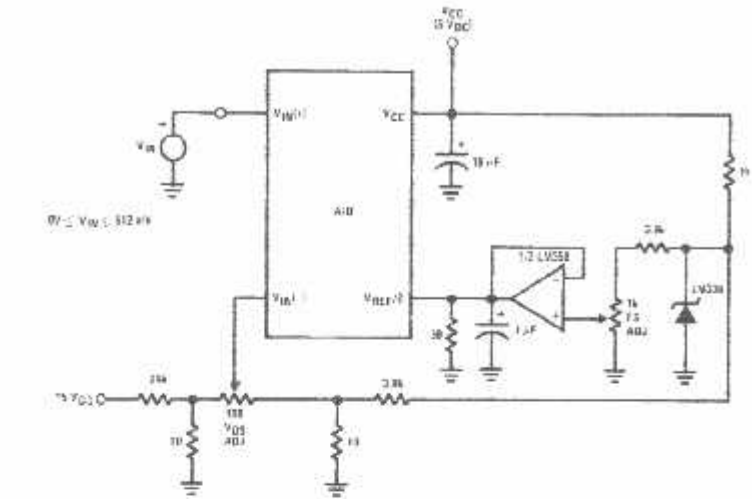
Span Adjust: $0V \leq V_{IN} \leq 3V$



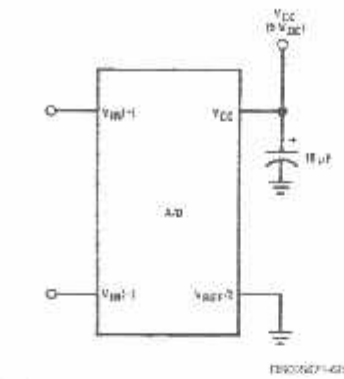
Typical Applications (Continued)

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805

Directly Converting a Low-Level Signal

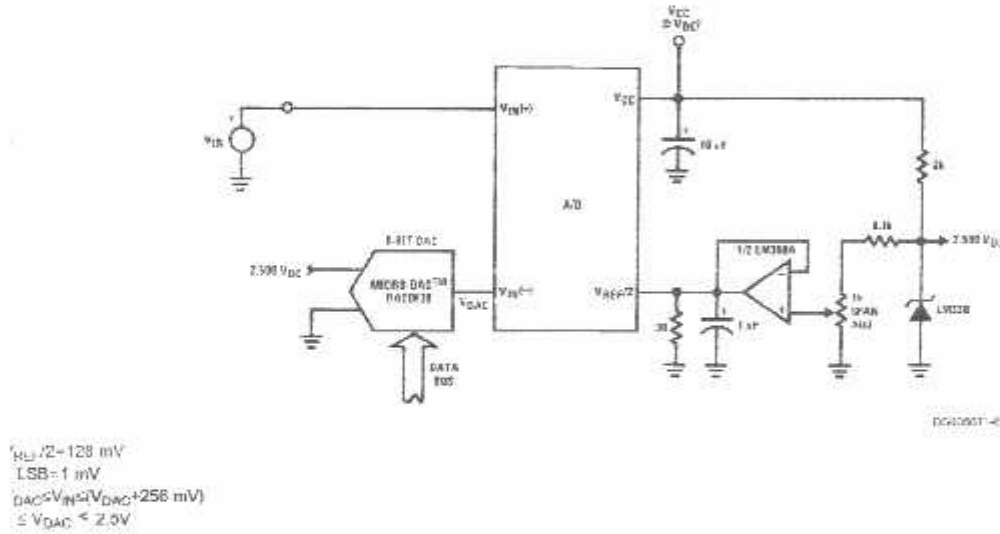


A μ P Interfaced Comparator



For:
V_{IN}(+) > V_{IN}(-)
Output = FF_{HEX}
For:
V_{IN}(+) < V_{IN}(-)
Output = 00_{HEX}

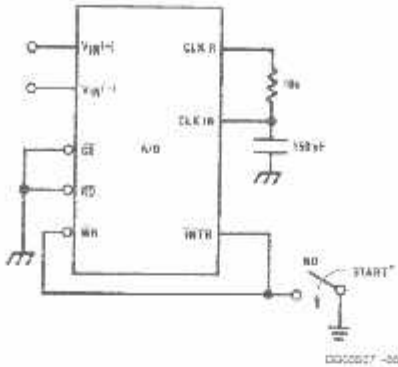
1 mV Resolution with μ P Controlled Range



Typical Applications (Continued)

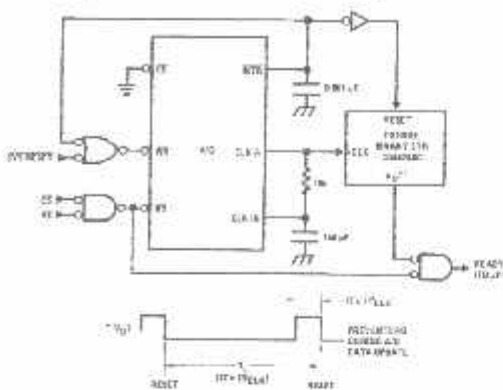
ADC0801/ADC0802/ADC0803/ADC0804/ADC0805

Self-Clocking in Free-Running Mode



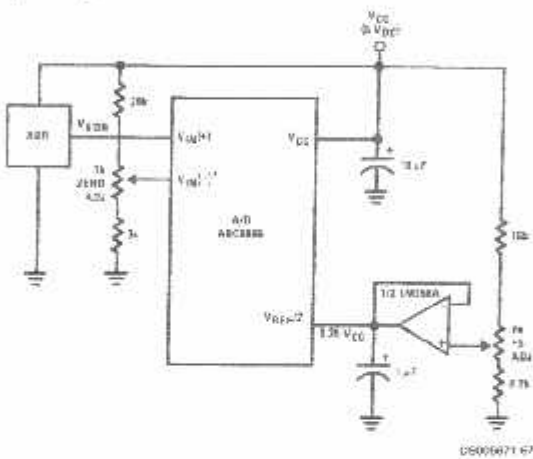
*After power-up, a momentary grounding of the WR input is needed to guarantee operation.

μ P Interface for Free-Running A/D



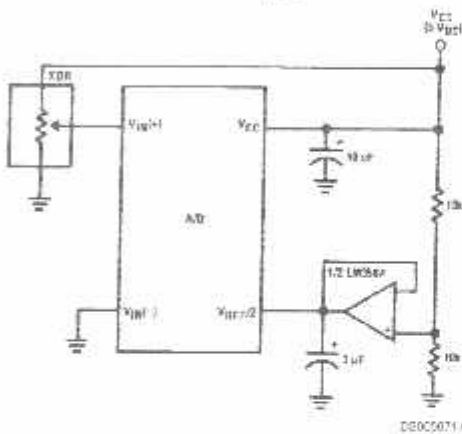
DS000671-65

Operating with "Automotive" Ratiometric Transducers



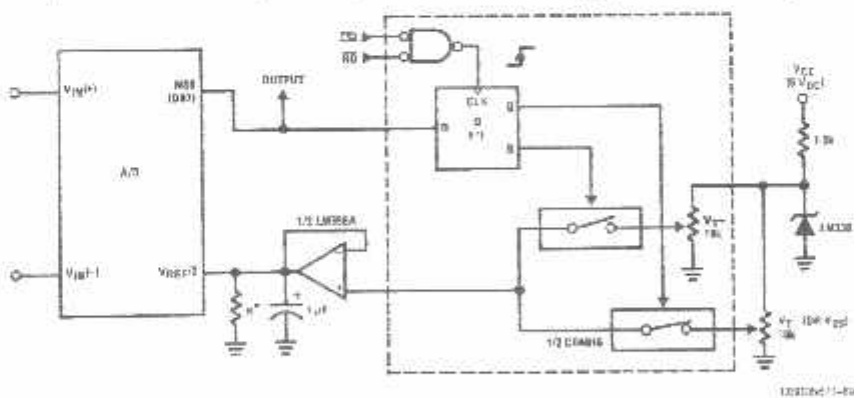
* $V_{REF-} = 0.15 V_{CC}$
15% of V_{CC} $V_{XDR} \leq 85\%$ of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



DS000671-65

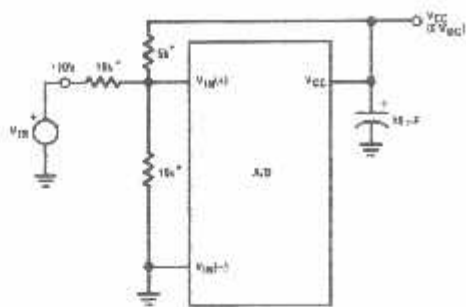
μ P Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)



as Figure 5 to select R value
 $R = 1$ for $V_{IN(+)} > V_{IN(-)} + (V_{REF}/2)$
all circuitry within the dotted area if
hysteresis is not needed

Typical Applications (Continued)

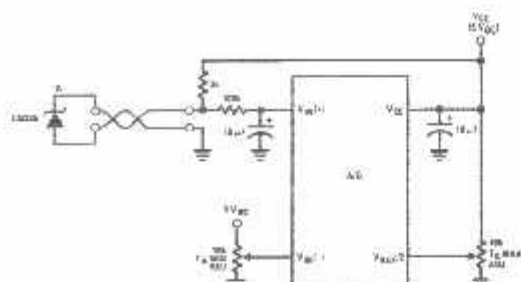
Handling $\pm 10\text{V}$ Analog Inputs



DS000671-70

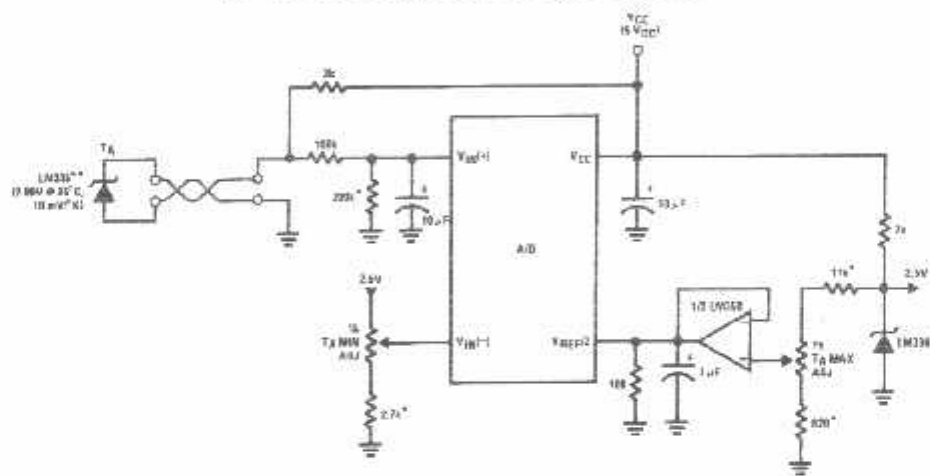
*Beckman Instruments #684-3 R10K resistor array

Low-Cost, μP Interfaced, Temperature-to-Digital Converter



DS000671-70

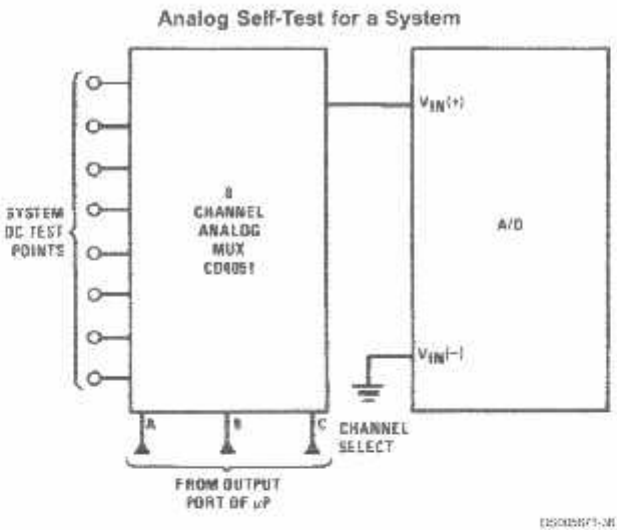
μP Interfaced Temperature-to-Digital Converter



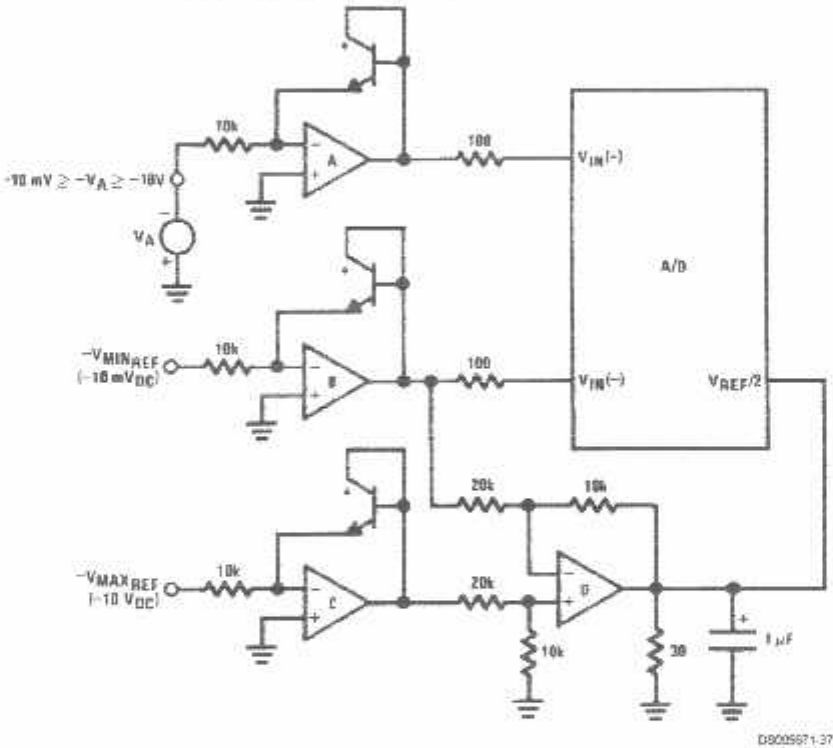
DS000671-70

*Circuit values shown are for $T_C \approx T_{AD} = 128^\circ\text{C}$
***Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

Typical Applications (Continued)



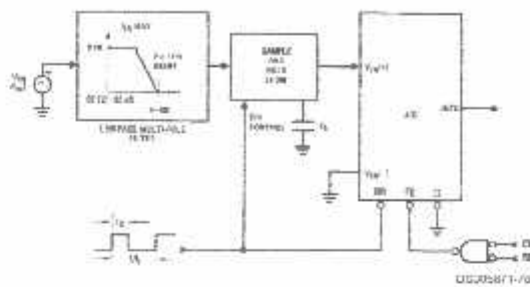
A Low-Cost, 3-Decade Logarithmic Converter



*LM389 transistors
A, B, C, D = LM324A quad op amp

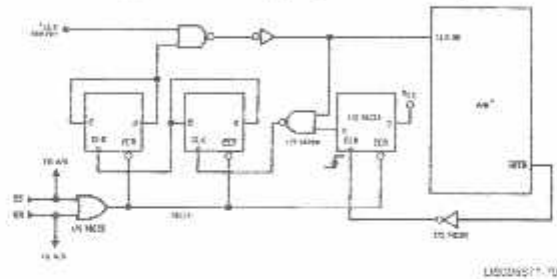
Typical Applications (Continued)

Sampling an AC Input Signal



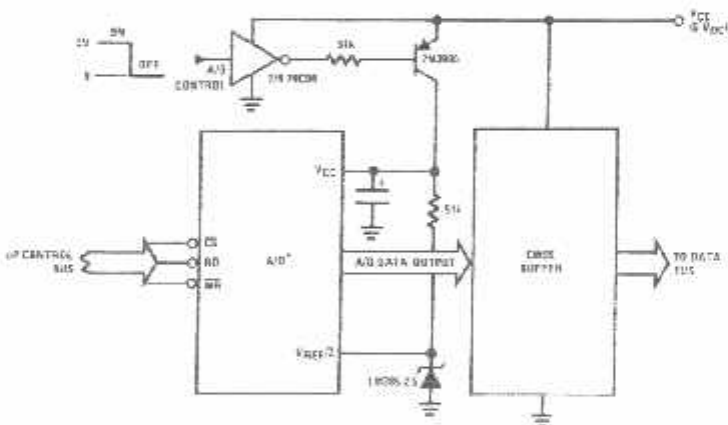
Note 11: Oversample whenever possible [keep $f_s > 2(f_i + 60)$] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.
Note 12: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ~30 seconds.)

Power Savings by A/D and VREF Shutdown



*Use ADC0801, 02, 03 or 05 for lowest power consumption.
Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.
Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in Figure 1. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as

D-1, D, and D+1. For the perfect A/D, not only will center-value (A-1, A, A+1, ...) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located $\pm 1/2$ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend

Functional Description (Continued)

± 1 LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Figure 2 shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct digital codes and the adjacent risers are guaranteed to be closer to the center-value points than $\pm 1/4$ LSB. In other words, if we apply an analog input equal to the center-value $\pm 1/4$ LSB, we guarantee that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than $1/2$ LSB.

The error curve of Figure 3 shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of Figure 1 is $+1/2$ LSB because the digital code appeared $1/2$ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt up-side steps are always 1 LSB in magnitude.

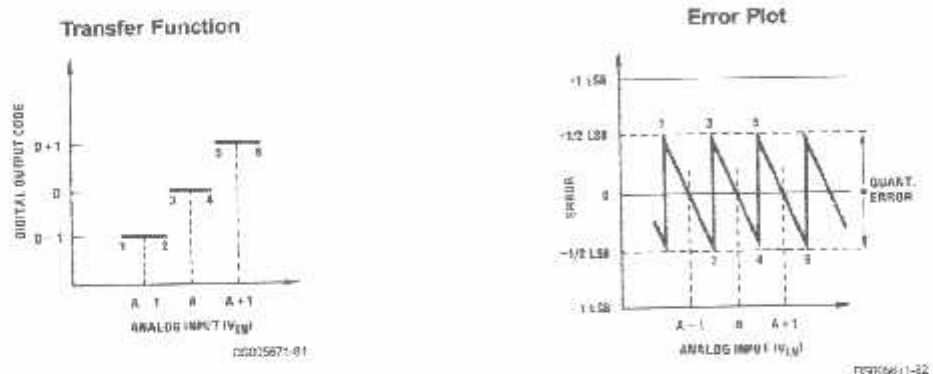


FIGURE 1. Clarifying the Error Specs of an A/D Converter
Accuracy = ± 0 LSB: A Perfect A/D

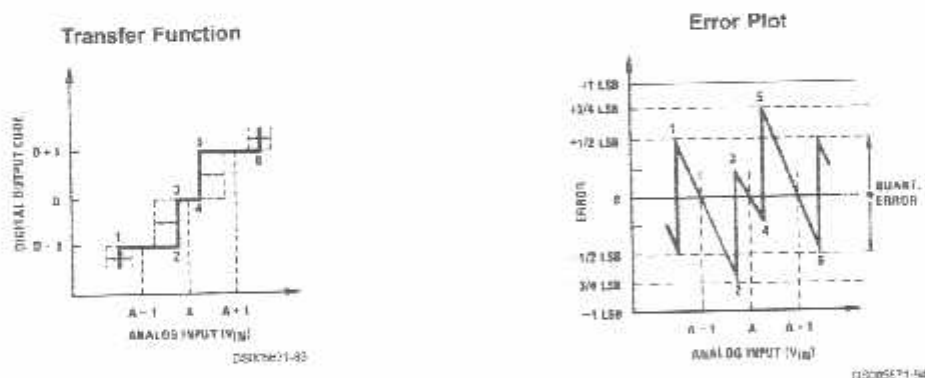


FIGURE 2. Clarifying the Error Specs of an A/D Converter
Accuracy = $\pm 1/4$ LSB

Functional Description (Continued)

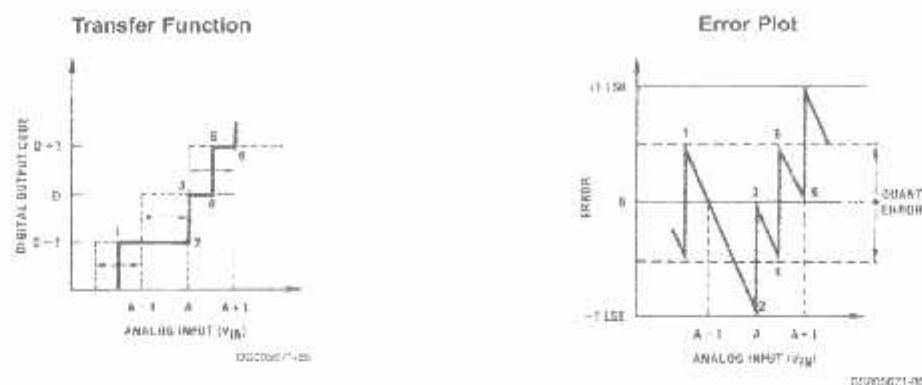


FIGURE 3. Clarifying the Error Specs of an A/D Converter
Accuracy = $\pm \frac{1}{2}$ LSB

2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage $[V_{IN}(+) - V_{IN}(-)]$ to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS} = 0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.

A functional diagram of the A/D converter is shown in Figure 4. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt ($\overline{INTR}$) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

Functional Description (Continued)

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is $4\frac{1}{2}$ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_{\theta}(\text{MAX}) = (V_P) (2\pi f_{\text{cm}}) \left(\frac{4.5}{f_{\text{CLK}}} \right)$$

where:

ΔV_{θ} is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to $\frac{1}{4}$ LSB (~ 5 mV) when operating with a 60 Hz common-mode frequency, f_{cm} , and using a 640 kHz A/D clock, f_{CLK} , would allow a peak value of the common-mode voltage, V_P , which is given by:

$$V_P = \frac{[\Delta V_{\theta}(\text{MAX})] (f_{\text{CLK}})}{(2\pi f_{\text{cm}}) (4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3}) (640 \times 10^3)}{(6.28) (60) (4.5)}$$

which gives

$$V_P = 1.9\text{V}$$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

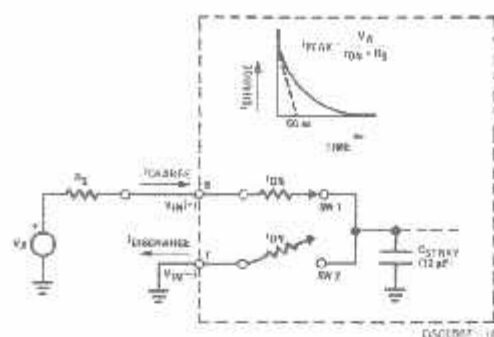
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in Figure 5.



$$f_{\text{CLK}} \text{ of } 8\text{W } 1 \text{ and } 8\text{W } 2 = 5 \text{ kHz}$$

$$\tau = f_{\text{CLK}} C_{\text{IN}} = 5 \text{ kHz} \times 12 \text{ pF} = 60 \text{ ns}$$

FIGURE 5. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not* cause errors as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of $V_{CC} + 50$ mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μ A. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin for high resistance sources ($> 1 \text{ k}\Omega$)*. If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor ($\leq 1 \text{ k}\Omega$) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, ($\leq 1 \text{ k}\Omega$), a 0.1 μ F bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long

Functional Description (Continued)

re. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

3.4 Noise

ie leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both rise and undesired digital clock coupling to these inputs in cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

4 Reference Voltage

4.1 Span Adjust

or maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC} , 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 6.

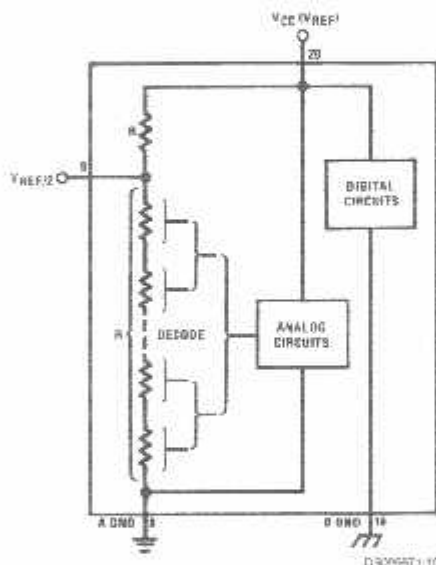


FIGURE 6. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either $1/2$ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

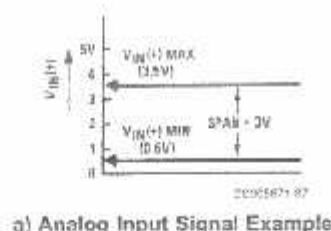
An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC} , instead of 0V to 5 V_{DC} , the span would be 3V as shown in Figure 7. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to $1/2$ of the 3V span or 1.5 V_{DC} . The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

2.4.2 Reference Accuracy Requirements

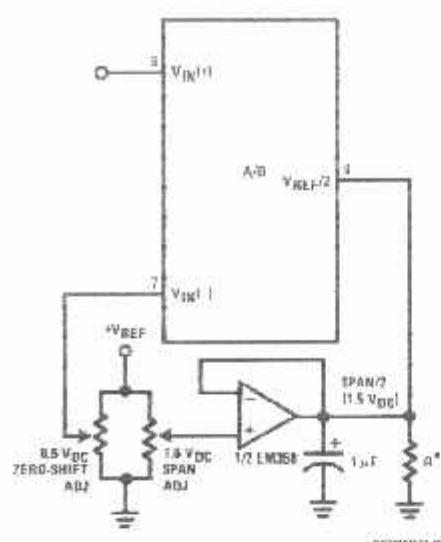
The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ± 10 mV V_{DC} will cause conversion errors of ± 1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even lighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM3366 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$. Other temperature range parts are also available.

Functional Description (Continued)



a) Analog Input Signal Example



*Add if $V_{REF}/2 \leq 1 V_{DC}$ with LM358 to draw 3 mA to ground.

b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 3.5V (Digital Out=FF_{HEX})

FIGURE 7. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal $\frac{1}{2}$ LSB value ($\frac{1}{2}$ LSB = 9.8 mV for $V_{REF}/2=2.500 V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is $\frac{1}{2}$ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus $\frac{1}{2}$ LSB (where the LSB is calculated for the desired analog span, $1 \text{ LSB} = \text{analog span}/256$) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+) \text{ fs adj} = V_{MAX} - 1.5 \left[\frac{(V_{MAX} - V_{MIN})}{256} \right]$$

where:

V_{MAX} = The high end of the analog input range and

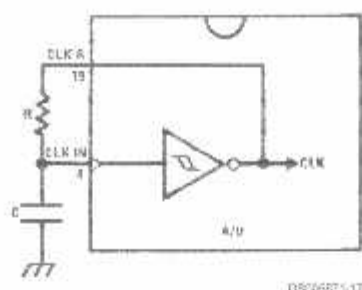
V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 8.

Functional Description (Continued)



$$R > \frac{1}{1.1 RC}$$

$$\geq 10 \text{ k}\Omega$$

FIGURE 8. Self-Clocking the A/D

any capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL driver).

Restart During a Conversion

When the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The INTR output simply remains at the "1" level.

Continuous Conversions

In operation in the free-running mode an initializing pulse would be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ output is tied to the INTR output. This $\overline{WR}$ and INTR mode would be momentarily forced to logic low following a power-up cycle to guarantee operation.

Driving the Data Bus

A MOS A/D, like MOS microprocessors and memories, require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in tri-state (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to solve this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available which to establish proper logic levels on the bus and before higher capacitive loads can be driven (see typical characteristics curves).

Higher CPU clock frequencies time can be extended for reads (and/or writes) by inserting wait states (8080) or clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external drivers must be used. These can be tri-state buffers

(low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μ F or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of 1/4 LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 9.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120 - 1/4 LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table 1 shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in Table 1, the nominal value of the digital display (when $V_{REF}/2 = 2.560V$) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC} . These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

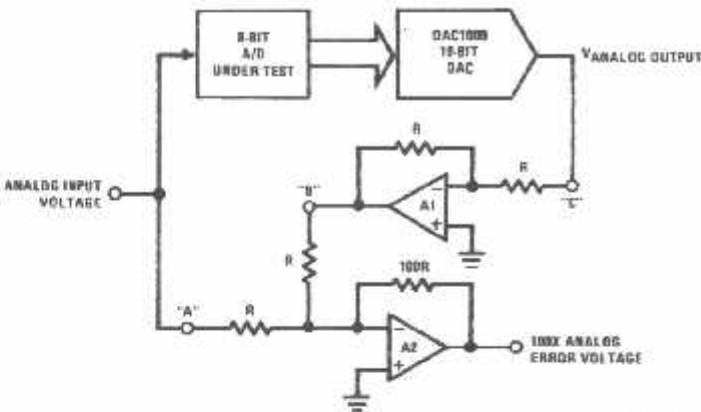


FIGURE 10. A/D Tester with Analog Error Output

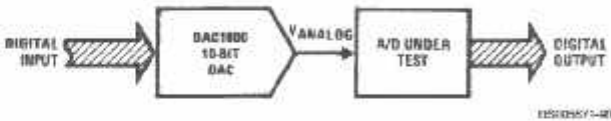


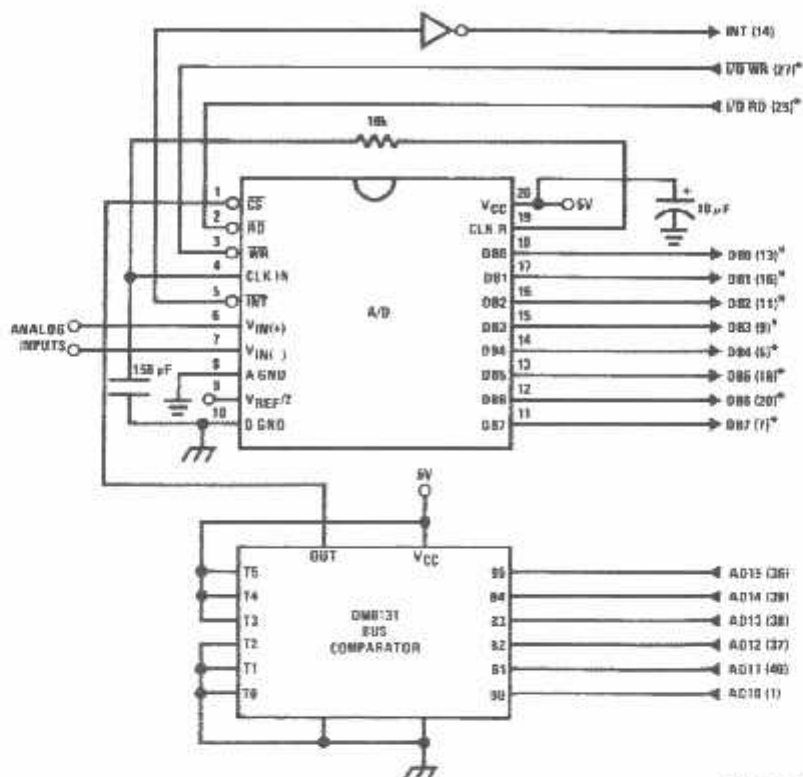
FIGURE 11. Basic "Digital" A/D Tester

TABLE 1. DECODING THE DIGITAL OUTPUT LEDs

BINARY	FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2=2.560 V_{DC}$	
	MS GROUP	LS GROUP	VMS GROUP (Note 15)	VLS GROUP (Note 15)
1 1 1 1	15/16	15/256	4.800	0.300
1 1 1 0	7/8	7/128	4.480	0.280
1 1 0 1	13/16	13/256	4.160	0.260
1 1 0 0	3/4	3/64	3.840	0.240
1 0 1 1	11/16	11/256	3.520	0.220
1 0 1 0	5/8	5/128	3.200	0.200
1 0 0 1	9/16	9/256	2.880	0.180
1 0 0 0	1/2	1/32	2.560	0.160
0 1 1 1	7/16	7/256	2.240	0.140
0 1 1 0	3/8	3/128	1.920	0.120
0 1 0 1	5/16	2/256	1.600	0.100
0 1 0 0	1/4	1/64	1.280	0.080
0 0 1 1	3/16	3/256	0.960	0.060
0 0 1 0	1/8	1/128	0.640	0.040
0 0 0 1	1/16	1/256	0.320	0.020
0 0 0 0			0	0

15: Display Output = VMS Group + VLS Group

Functional Description (Continued)



US000617-20

Note 16: *Pin numbers for the DP8228 system controller, others are INS8060A.

Note 17: Pin 23 of the INS8228 must be tied to -12V through a 1 k Ω resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 12. ADC0801 INS8080A CPU Interface

Functional Description (Continued)

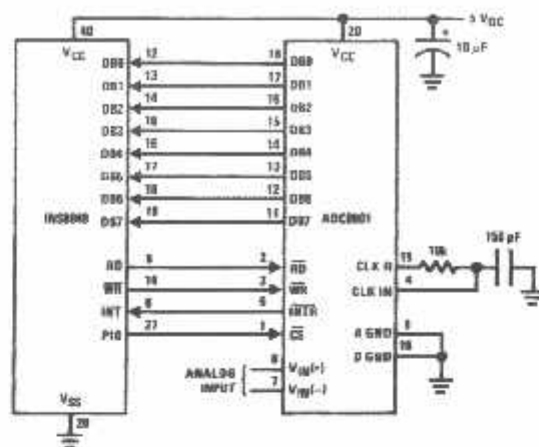


FIGURE 13. INS8048 Interface

SAMPLE PROGRAM FOR Figure 13 INS8048 INTERFACE

04 10	JMP	10H	: Program starts at addr 10
	ORG	3H	
04 50	JMP	50H	: Interrupt jump vector
	ORG	10H	: Main program
99 FE	ANL	P1, #0FEH	: Chip select
81	MOVX	A, @R1	: Read in the 1st data
			: to reset the intr
89 01	START:	ORL	P1, #1
B8 20		MOV	R0, #20H
B9 FF		MOV	R1, #0FFH
BA 10		MOV	R2, #10H
23 FF	AGAIN:	MOV	A, #0FFH
99 FE		ANL	P1, #0FEH
91		MOVX	@R1, A
05		EN	I
96 21	LOOP:	JNZ	LOOP
EA 1B		DJNZ	R2, AGAIN
00		NOP	
00		NOP	
		ORG	50H
81	INDATA:	MOVX	A, @R1
A0		MOV	@R0, A
18		INC	R0
89 01		ORL	P1, #1
27		CLR	A
93		RETR	

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4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General RD and WR strobes are provided and separate memory request, MREQ, and I/O request, IORQ, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the RD and WR strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 14.

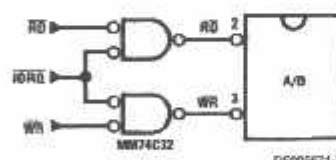


FIGURE 14. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to

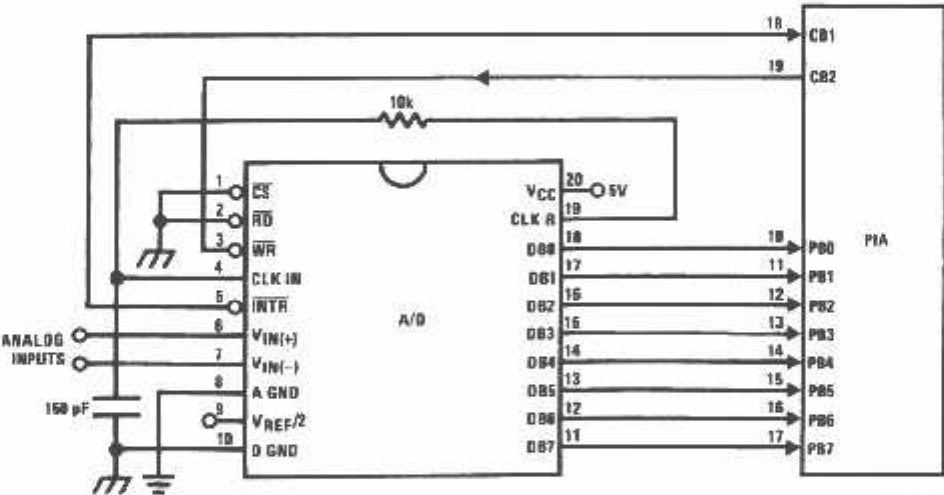
Functional Description (Continued)

SAMPLE PROGRAM FOR Figure 15 ADC0801-MC6800 CPU INTERFACE

```
0010    DF 36          DATAIN    STX      TEMP2      ; Save contents of X
0012    CE 00 2C          LDX      #002C      ; Upon  $\overline{IRQ}$  low CPU
0018    FF FF F8          STX      $FFF8      ; jumps to 002C
001B    B7 50 00          STAA     $5000      ; Start ADC0801
001C    0E              CLI              ;
001D    3E              CONVRT    WAI              ; Wait for interrupt
001F    DE 34          LDX      TEMP1
0022    8C 02 0F          CPX      #020F      ; Is final data stored?
0027    27 14          BEQ      ENDP
0028    B7 50 00          STAA     $5000      ; Restarts ADC0801
002A    08              INX
002B    DF 34          STX      TEMP1
002C    20 F0          BRA      CONVRT
002E    DE 34          INTRPT    LDX      TEMP1
0031    B6 50 00          LDAA     $5000      ; Read data
0033    A7 0D          STAA     X              ; Store it at X
0034    3B              RTI
0036    02 00          TEMP1    FDB     $0200      ; Starting address for
                                ; data storage
0038    00 00          TEMP2    FDB     $0000
003B    CE 02 00          ENDP    LDX      #0200      ; Reinitialize TEMP1
003D    DF 34          STX      TEMP1
003F    DE 36          LDX      TEMP2
                                RTS              ; Return from subroutine
                                ; To user's program
```

DS000671-A1

Note 22: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.



DS000671-25

FIGURE 16. ADC0801-MC6820 PIA Interface

unctional Description (Continued)

SAMPLE PROGRAM FOR Figure 16 ADC0801—MC6820 PIA INTERFACE

```

0010      CE 00 38      DATAIN      LDX      #$0038      ; Upon  $\overline{\text{IRQ}}$  low CPU
0013      FF FF F8      STX          $FFF8      ; jumps to 0038
0016      B6 80 06      LDAA         PIAORB      ; Clear possible  $\overline{\text{IRQ}}$  flags
0019      4F            CLRA
001A      B7 80 07      STAA         PIACRB
001D      B7 80 06      STAA         PIAORB      ; Set Port B as input
0020      DE            CLI
0021      C6 34          LDAB         #$34
0023      B6 3D          LDAA         #$3D
0025      F7 80 07      CONVRT      STAB         PIACRB      ; Starts ADC0801
0028      B7 80 07      STAA         PIACRB
002B      3E            WAI            ; Wait for interrupt
002C      DE 40          LDX          TEMP1
002E      BC 02 0F      CPX          #$020F      ; Is final data stored?
0031      27 0F          BEQ          ENDP
0033      08            INX
0034      DF 40          STX          TEMP1
0036      20 ED          BRA          CONVRT
0038      DE 40          INTERPT     LDX          TEMP1
003A      B6 80 06      LDAA         PIAORB      ; Read data in
003D      A7 00          STAA         X          ; Store it at X
003F      3B            RTI
0040      02 00          TEMP1       FDB         $0200      ; Starting address for
                                ; data storage
0042      CE 02 00      ENDP         LDX          #$0200      ; Reinitialize TEMP1
0045      DF 40          STX          TEMP1
0047      39            RTS            ; Return from Subroutine
                                PIAORB      EQU          $8006      ; To user's program
                                PIACRB      EQU          $8007

```

D80066T1 A2

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the 68000 CPU. This scheme can easily be extended to allow interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter; its output drives the other A/Ds.

The converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{\text{CS}}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the

CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)

SAMPLE PROGRAM FOR Figure 17 INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#002A	; Upon IRQ LOW CPU
0016	FF FF F8		STX	\$FFFF	; Jumps to 002A
0018	B7 50 00		STAA	\$5000	; Starts all A/D's
001E	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

DS005671-A3

SAMPLE PROGRAM FOR Figure 17 INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	\$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	\$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	\$0000	

DS005671-A4

Figure 25: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. Figure 18 is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 μ V for 1/4 LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN(+)} - V_{IN(-)}]}_{\text{SIGNAL}} \underbrace{\left(1 + \frac{2R_2}{R_1}\right)}_{\text{GAIN}} + \underbrace{(V_{OS2} - V_{OS1} - V_{OS3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R_2}{R_1}\right)}_{\text{GAIN}}$$

where I_X is the current through resistor R_X . All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

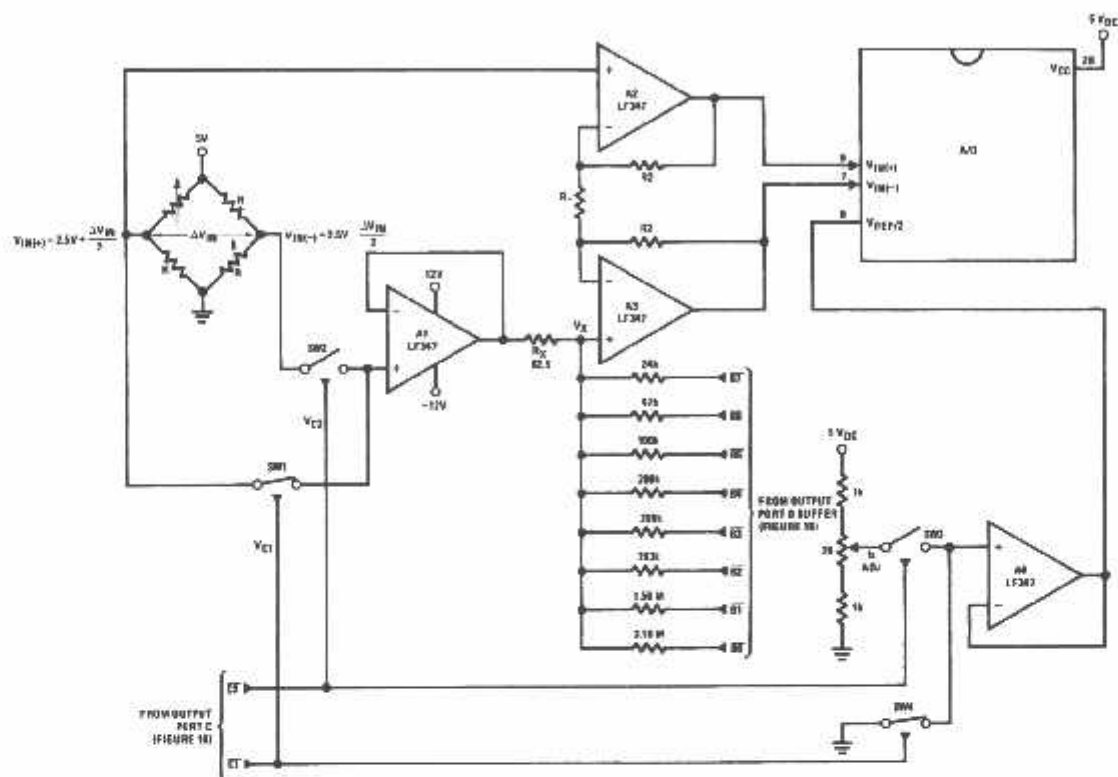
The INS8080A uses the 3 I/O ports of an INS8255 Programmable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in Figure 19. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_x increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on

Functional Description (Continued)

any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ± 12 mV with a resolution of $50 \mu\text{V}$, which will null the offset error term to $\frac{1}{4}$ LSB of full-scale for

the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



Note 26: $R2 = 49.5 R1$

Note 27: Switches are LMC1334 CMOS analog switches.

Note 28: The 9 resistors used in the auto-zero section can be $\pm 5\%$ tolerance.

FIGURE 18. Gain of 100 Differential Transducer Preamp

D3005671-01

unctional Description (Continued)

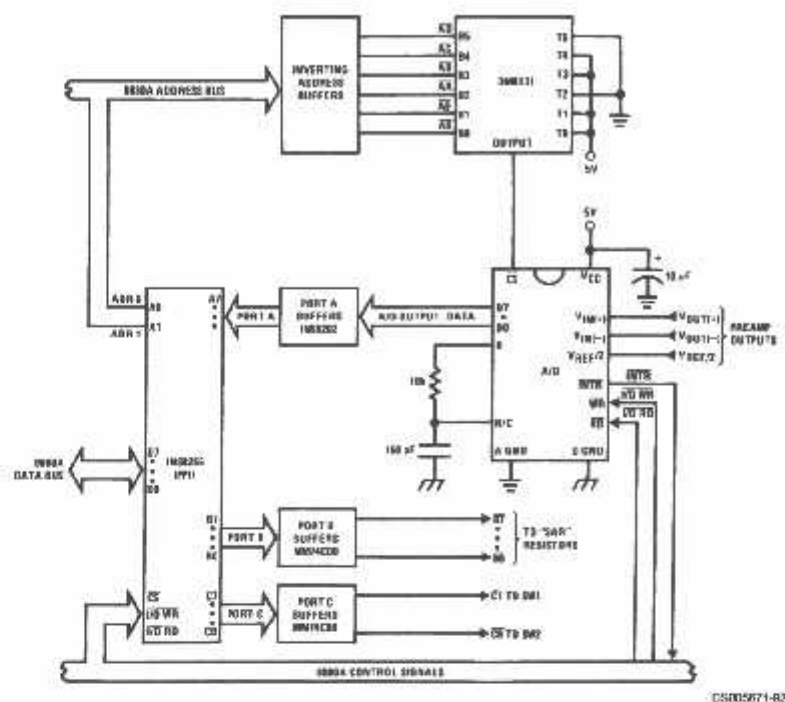


FIGURE 19. Microprocessor Interface Circuitry for Differential Preamp

flow chart for the zeroing subroutine is shown in Figure 20. must be noted that the ADC0801 series will output an all iro code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. so, a logic inversion exists as all of the I/O ports are iffered with inverting gates.

sically, if the data read is zero, the differential output ltag is negative, so a bit in Port B is cleared to pull V_x ore negative which will make the output more positive for e next conversion. If the data read is not zero, the output ltag is positive so a bit in Port B is set to make V_x more sltve and the output more negative. This continues for 8 proximations and the differential output eventually conges to within 5 mV of zero.

e actual program is given in Figure 21. All addresses used e compatible with the BLC 80/10 microcomputer system. particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

Multiple A/D Converters in a Z-80 Interrupt even Mode

data acquisition systems where more than one A/D con- ter (or other peripheral device) will be interrupting pro- m execution of a microprocessor, there is obviously a

need for the CPU to determine which device requires serv- ing. Figure 22 and the accompanying software is a method of determining which of 7 ADC0801 converters has com- pleted a conversion (INTR asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INTR is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the INTR outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

Functional Description (Continued)

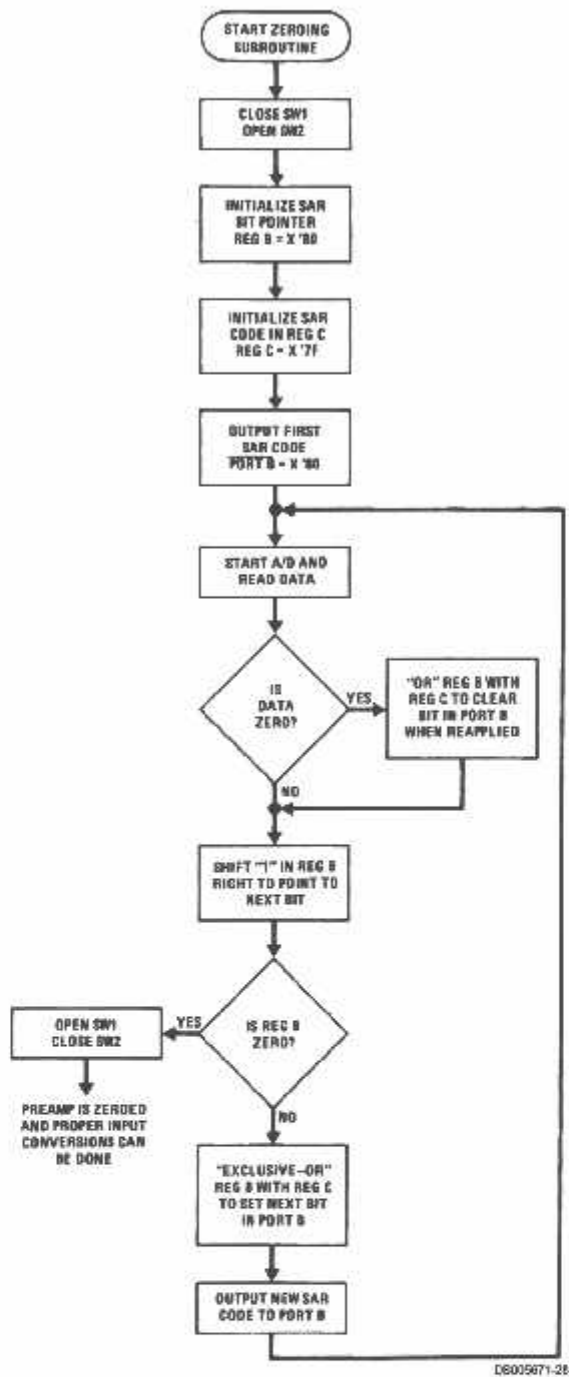


FIGURE 20. Flow Chart for Auto-Zero Routine

unctional Description (Continued)

3D00	3E90	MVI 90		
3D02	D3E7	Out Control Port		; Program PPI
3D04	2601	MVI H 01	Auto-Zero Subroutine	
3D06	7C	MOV A,H		
3D07	D3E6	OUT C		; Close SW1 open SW2
3D09	0680	MVI B 80		; Initialize SAR bit pointer
3D0B	3E7F	MVI A 7F		; Initialize SAR code
3D0D	4F	MOV C,A	Return	
3D0E	D3E5	OUT B		; Port B = SAR code
3D10	31AA3D	LXI SP 3DAA	Start	; Dimension stack pointer
3D13	D3E4	OUT A		; Start A/D
3D15	FB	IE		
3D16	00	NOF	Loop	; Loop until $\overline{\text{INT}}$ asserted
3D17	C3163D	JMP Loop		
3D1A	7A	MOV A,D	Auto-Zero	
3D1B	C600	ADI 00		
3D1D	CA2D3D	JZ Set C		; Test A/D output data for zero
3D20	78	MOV A,B	Shift B	
3D21	F600	ORI 00		; Clear carry
3D23	1F	RAR		; Shift "1" in B right one place
3D24	FE00	CPI 00		; Is B zero? If yes last
3D26	CA373D	JZ Done		; approximation has been made
3D29	47	MOV B,A		
3D2A	C3333D	JMP New C		
3D2D	79	MOV A,C	Set C	
3D2E	B0	ORA B		; Set bit in C that is in same
3D2F	4F	MOV C,A		; position as "1" in B
3D30	C3203D	JMP Shift B		
3D33	A9	XRA C	New C	; Clear bit in C that is in
3D34	C30D3D	JMP Return		; same position as "1" in B
3D37	47	MOV B,A	Done	; then output new SAR code.
3D38	7C	MOV A,H		; Open SW1, close SW2 then
3D39	EB03	XRI 03		; proceed with program. Presamp
3D3B	D3E6	OUT C		; is now zeroed.
3D3D	*		Normal	
	*			
	*			
	Program for processing proper data values			
3C3D	DBE4	IN A	Read A/D Subroutine	; Read A/D data
3C3F	EEFF	XRI FF		; Invert data
3C41	57	MOV D,A		
3C42	78	MOV A,B		; Is B Reg = 0? If not stay
3C43	E6FF	ANI FF		; in auto zero subroutine
3C45	C21A3D	JNZ Auto-Zero		
3C48	C33D3D	JMP Normal		

05005671-05

Note 29: All numerical values are hexadecimal representations.

FIGURE 21. Software for Auto-Zeroed Differential A/D

3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

- The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.
- The peripherals of concern are mapped into I/O space with the following port assignments:

Functional Description (Continued)

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3

HEX PORT ADDRESS	PERIPHERAL
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

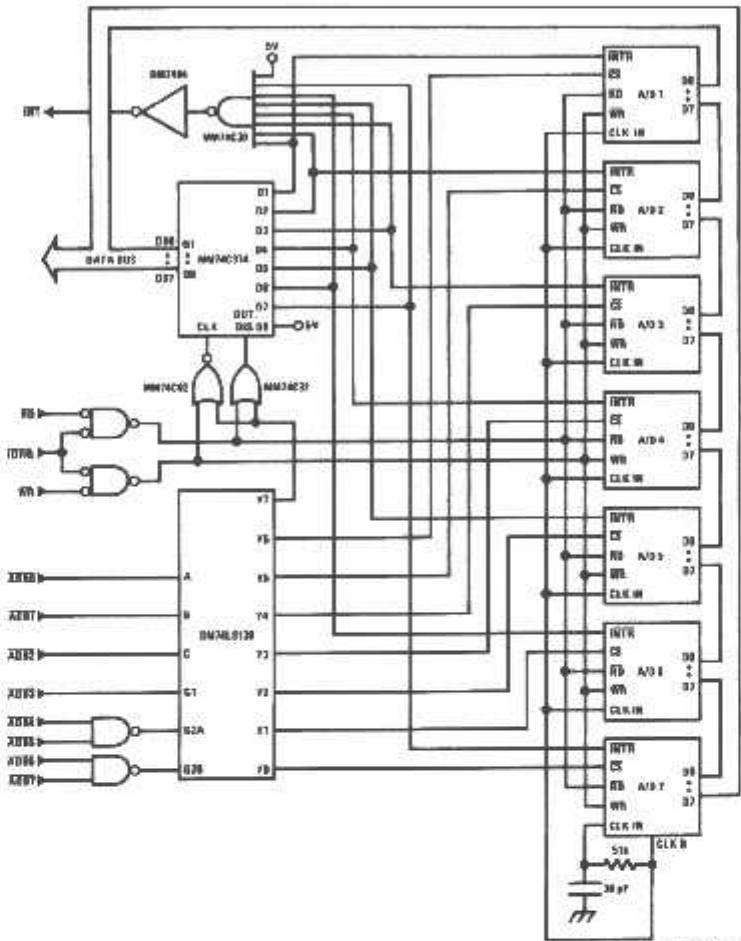


FIGURE 22. Multiple A/Ds with Z-80 Type Microprocessor

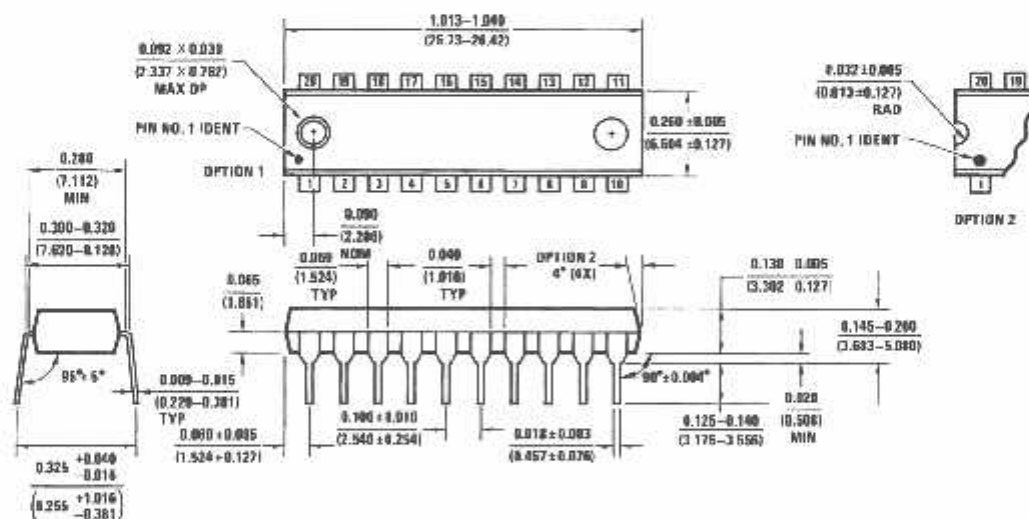
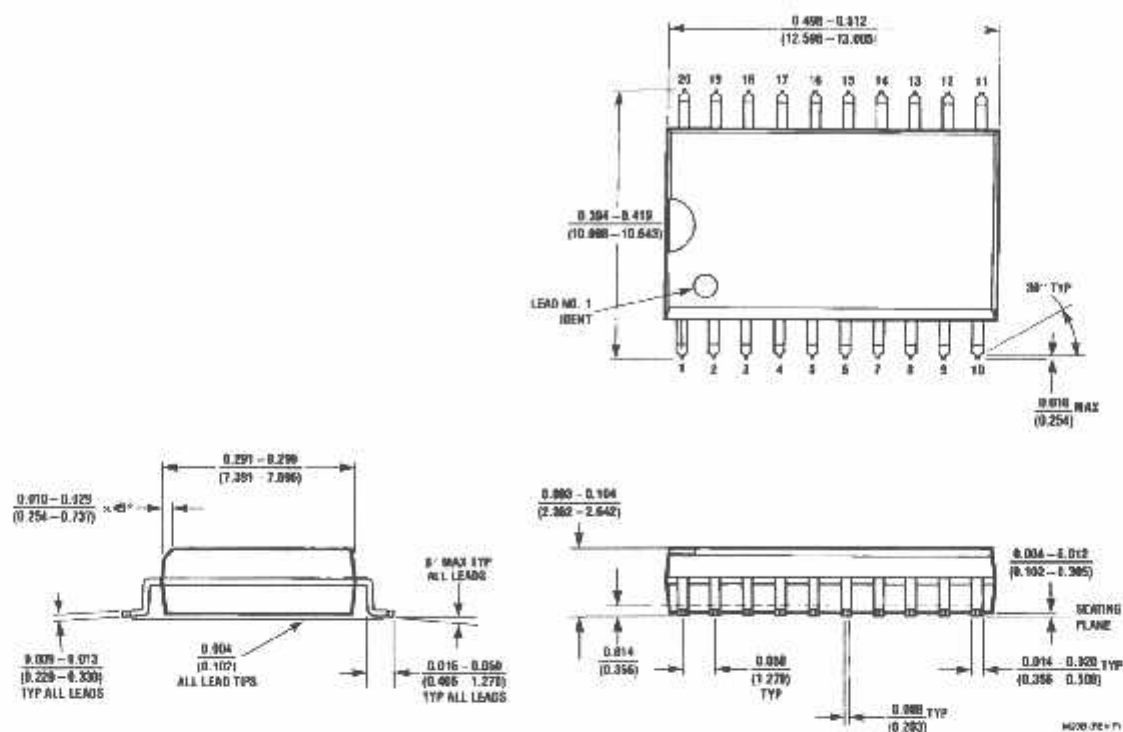
Functional Description (Continued)

INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE	SOURCE STATEMENT	COMMENT
0038	E5	PUSH HL	; Save contents of all registers affected by
0039	C5	PUSH BC	; this subroutine.
003A	F5	PUSH AF	; Assumed INT mode 1 earlier set.
003B	21 00 3E	LD (HL), X3E00	; Initialize memory pointer where data will be stored.
003E	0E 01	LD C, X01	; C register will be port ADDR of A/D converters.
0040	D3 00	OUT X00, A	; Load peripheral status word into 8-bit latch.
0042	DB 00	IN A, X00	; Load status word into accumulator.
0044	47	LD B, A	; Save the status word.
0045	79	TEST LD A, C	; Test to see if the status of all A/D's have
0046	FE 08	CP, X08	; been checked. If so, exit Subroutine
0048	CA 60 00	JPZ, DONE	
004B	7B	LD A, B	; Test a single bit in status word by looking for
004C	1F	RRA	; a "1" to be rotated into the CARRY (an INT
004D	47	LD B, A	; is loaded as a "1"). If CARRY is set then load
004E	DA 55 00	JPC, LOAD	; contents of A/D at port ADDR in C register.
0051	0C	INC C	; If CARRY is not set, increment C register to point
0052	C3 45 00	JP, TEST	; to next A/D, then test next bit in status word.
0055	ED 78	LOAD IN A, (C)	; Read data from interrupting A/D and invert
0057	EE FF	XOR FF	; the data.
0059	77	LD (HL), A	; Store the data
005A	2C	INC L	
005B	71	LD (HL), C	; Store A/D identifier (A/D port ADDR).
005C	2C	INC L	
005D	C3 51 00	JP, NEXT	; Test next bit in status word.
0060	F1	DONE POP AF	; Re-establish all registers as they were
0061	C1	POP BC	; before the interrupt.
0062	E1	POP HL	
0063	C9	RET	; Return to original program

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Physical Dimensions inches (millimeters) unless otherwise noted



Notes

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Features

- Compatible with MCS[®]51 Products
- 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
 - SPI Serial Interface for Program Downloading
 - Endurance: 1,000 Write/Erase Cycles
- 1K Bytes EEPROM
 - Endurance: 100,000 Write/Erase Cycles
- 5 to 6V Operating Range
- Typical Static Operation: 0 Hz to 24 MHz
- Two-level Program Memory Lock
- 6 x 8-bit Internal RAM
- Programmable I/O Lines
- Three 16-bit Timer/Counters
- Six Interrupt Sources
- Programmable UART Serial Channel
- I²C Serial Interface
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down
- Programmable Watchdog Timer
- Two Data Pointers
- Power-off Flag

Description

AT89S8252 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of downloadable Flash programmable and erasable read-only memory and 2K bytes of EEPROM. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip downloadable Flash allows the program memory to be programmed In-System through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with downloadable program memory on a monolithic chip, the Atmel AT89S8252 is a powerful microcontroller, which provides a highly-flexible and cost-effective solution to many embedded control applications.

AT89S8252 provides the following standard features: 8K bytes of downloadable program memory, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt structure, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, AT89S8252 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

The downloadable Flash can be changed a single byte at a time and is accessible through the SPI serial interface. Holding RESET active forces the SPI bus into a serial programming interface and allows the program memory to be written to or read from as long as lock bits have been activated.



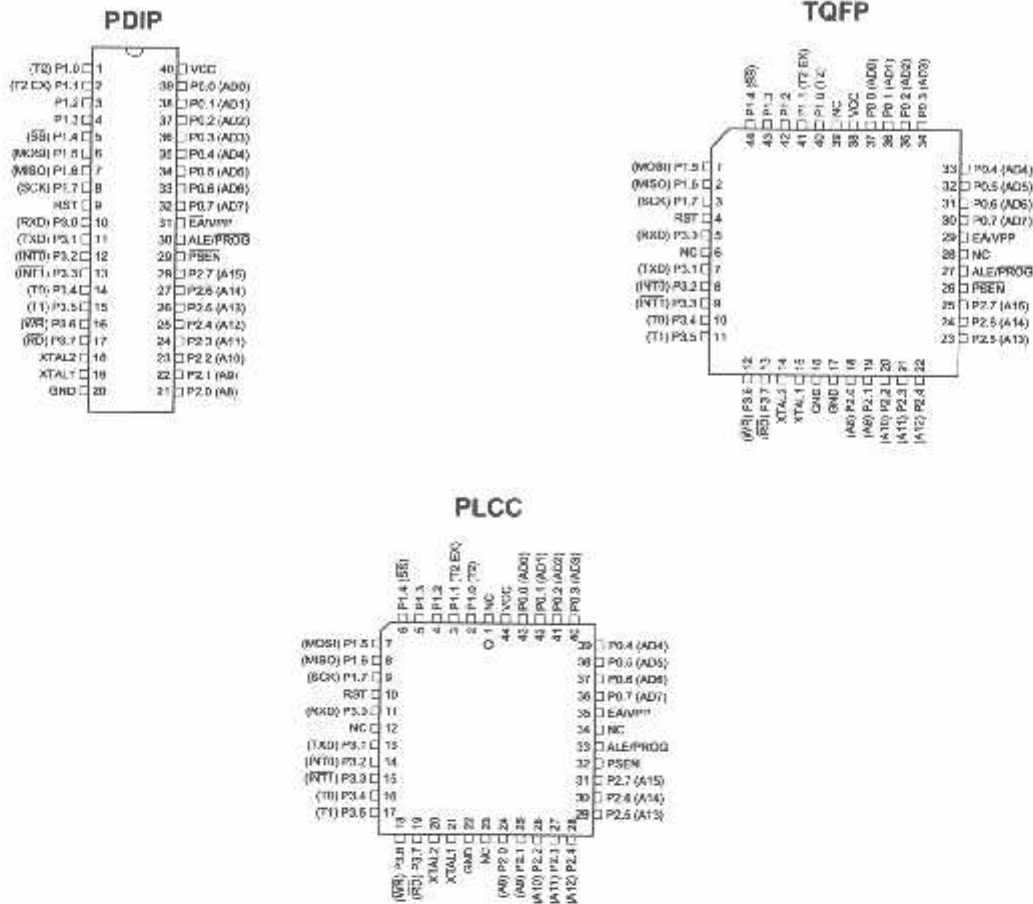
8-bit Microcontroller with 8K Bytes Flash

AT89S8252

0401F-MICRO-11/03



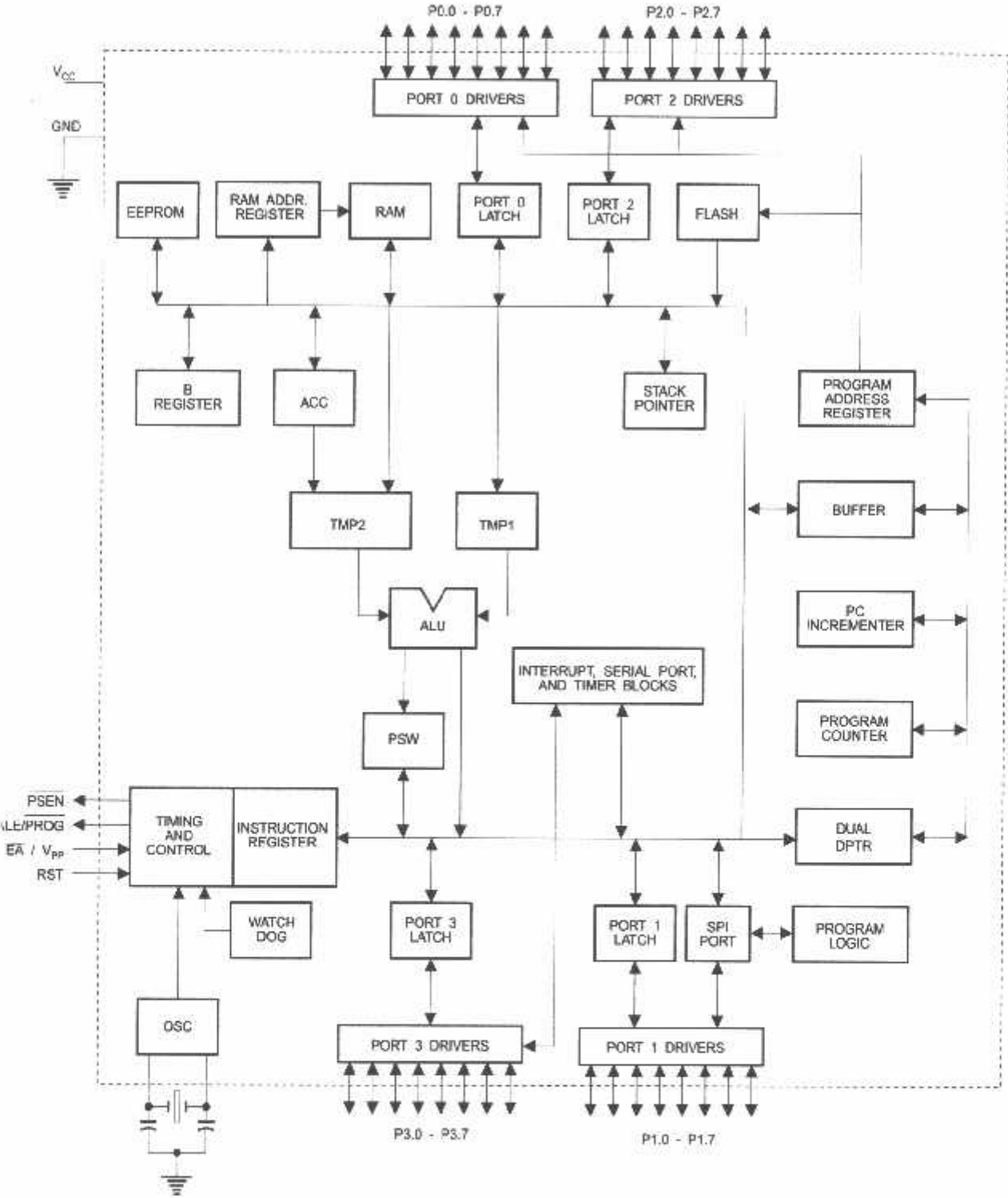
Configurations



Description

- Supply voltage.
- Ground.
- Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.
- Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.
- Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.
- Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

ck Diagram



Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

/PROG

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{\text{N}}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

/PP

External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

L1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

L2

Output from the inverting oscillator amplifier.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Table 1. AT89S8252 SFR Map and Reset Values

0FH								0FFH
0EH	B 00000000							0F7H
0DH								0EFH
0CH	ACC 00000000							0E7H
0BH								0DFH
0AH	PSW 00000000					SPCR 000001XX		0D7H
09H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CFH
08H								0C7H
07H	IP XX000000							0BFH
06H	P3 11111111							0B7H
05H	IE CX000000		SPSR 00XXXXXX					0AFH
04H	P2 11111111							0A7H
03H	SCON 00000000	SBUF XXXXXXXX						9FH
02H	P1 11111111						WMCON 00000010	97H
01H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		8FH
00H	P0 11111111	SP 0000011*	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	87H
							PCON 00000000	

2. T2CON – Timer/Counter 2 Control Register

ON Address = 0C8H

Reset Value = 0000 0000B

addressable

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
7	6	5	4	3	2	1	0

bit	Function
	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
.K	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
.K	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
1	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
2	Timer or counter select for Timer 2. C/T2 = 0 for timer function. C/T2 = 1 for external event counter (falling edge triggered).
RL2	Capture/Reload select. CP/RL2 = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/RL2 = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.



Watchdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in Figure 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

3. WMCON—Watchdog and Memory Control Register

CON Address = 96H

Reset Value = 0000 0010B

PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
7	6	5	4	3	2	1	0

Bit	Function
PS2, PS1, PS0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EEMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EEMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
DPS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1.
WDTRST / BSY	Watchdog Timer Reset and EEPROM Ready/Busy Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/BSY flag in a Read-Only mode during EEPROM write. RDY/BSY = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/BSY bit equals "0" and is automatically reset to "1" when programming is completed.
WDTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

4. SPCR – SPI Control Register

SFR Address = D5H				Reset Value = 0000 01XXB			
SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
7	6	5	4	3	2	1	0
Symbol	Function						
IE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts, SPIE = 0 disables SPI interrupts.						
	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.						
ID	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.						
TR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.						
IL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.						
IA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.						
IO :1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, F_{osc} , is as follows: SPR1 SPR0 SCK = F_{osc} divided by 0 0 4 0 1 16 1 0 64 1 1 128						



5. SPSR – SPI Status Register

SR Address = AAH

Reset Value = 00XX XXXXB

SPIF	WCOL	–	–	–	–	–	–
7	6	5	4	3	2	1	0

Bit	Function
7	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then reading/writing the SPI data register.
6	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

6. SPDR – SPI Data Register

SR Address = 86H

Reset Value = unchanged

SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
7	6	5	4	3	2	1	0

7. Memory – EEPROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/BSY bit (read-only) in SFR WMCON. RDY/BSY = 0 means

programming is still in progress and $\overline{RDY/BSY} = 1$ means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

programmable
Watchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent internal oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at $V_{CC} = 5V$) are within $\pm 30\%$ of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			Period (nominal)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the Atmel web site (<http://www.atmel.com>). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/T2 in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected.

Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

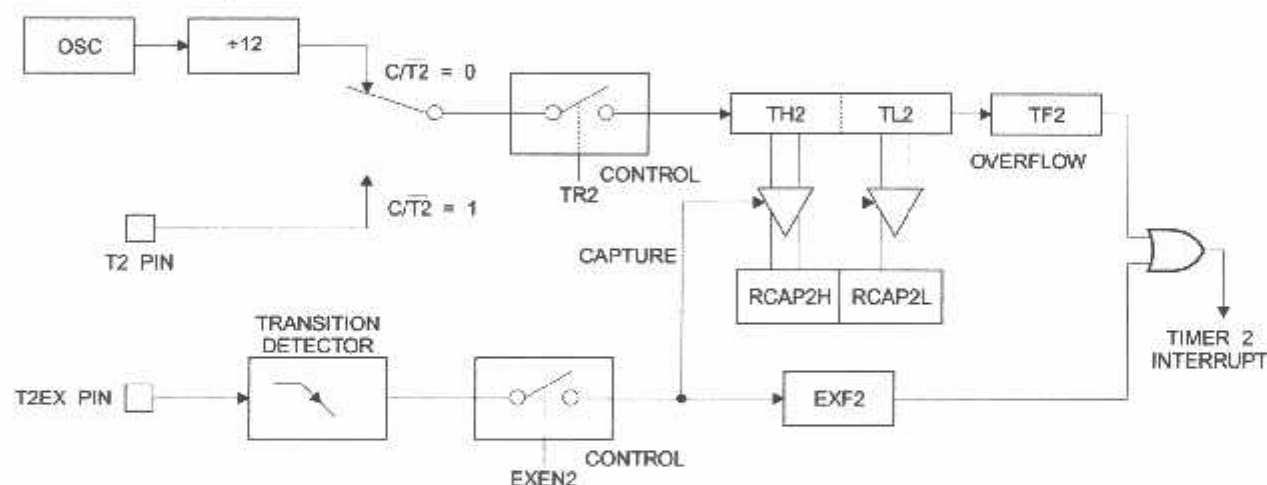
Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Figure 1. Timer 2 in Capture Mode



o-reload (Up or Down
nter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

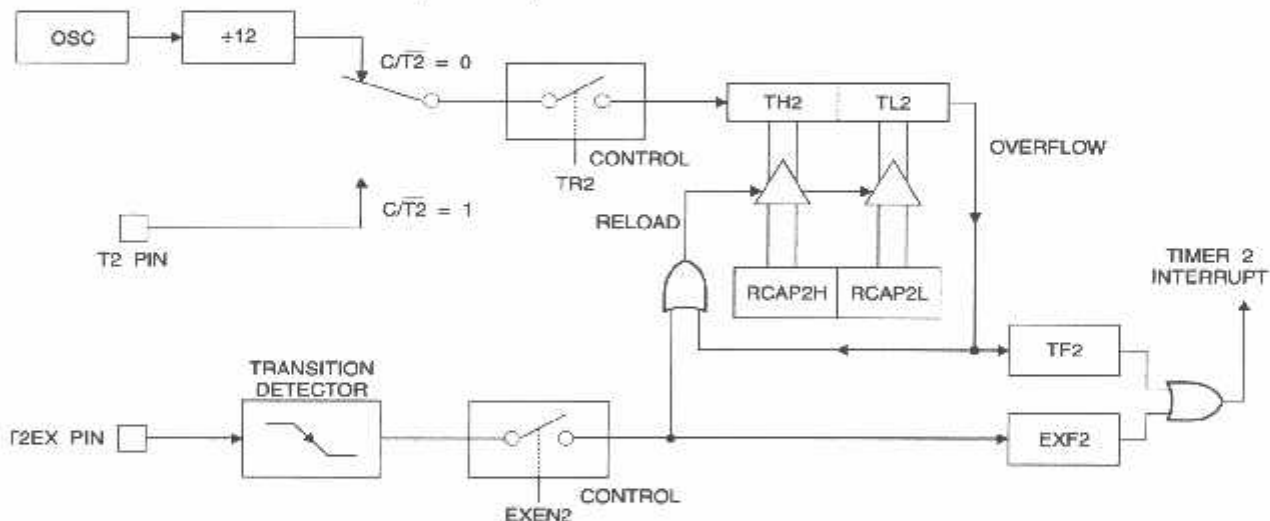
Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes **Timer 2** count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

re 2. Timer 2 in Auto Reload Mode (DCEN = 0)



9. T2MOD – Timer 2 Mode Control Register

OD Address = 0C9H

Reset Value = XXXX XX00B

Bit Addressable

–	–	–	–	–	–	T2OE	DCEN
7	6	5	4	3	2	1	0

Symbol	Function
–	Not implemented, reserved for future use.
OE	Timer 2 Output Enable bit.
EN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

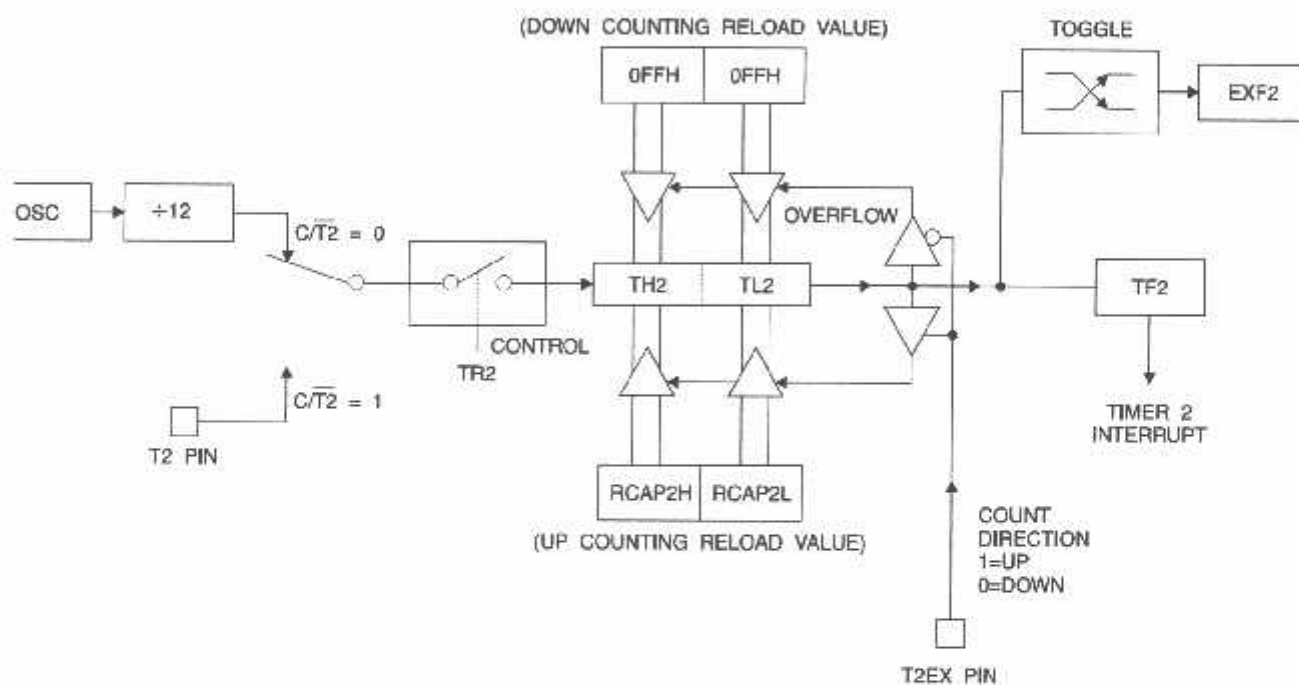
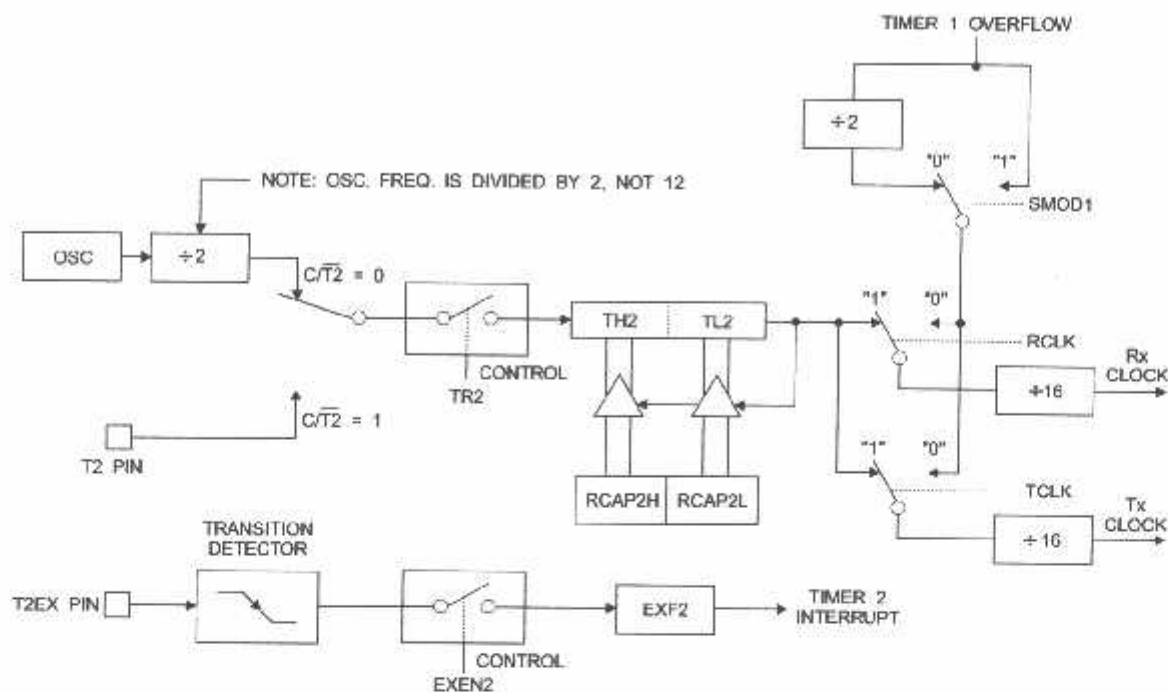


Figure 4. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($CP/T2 = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (RCAP2H, RCAP2L)]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.



Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

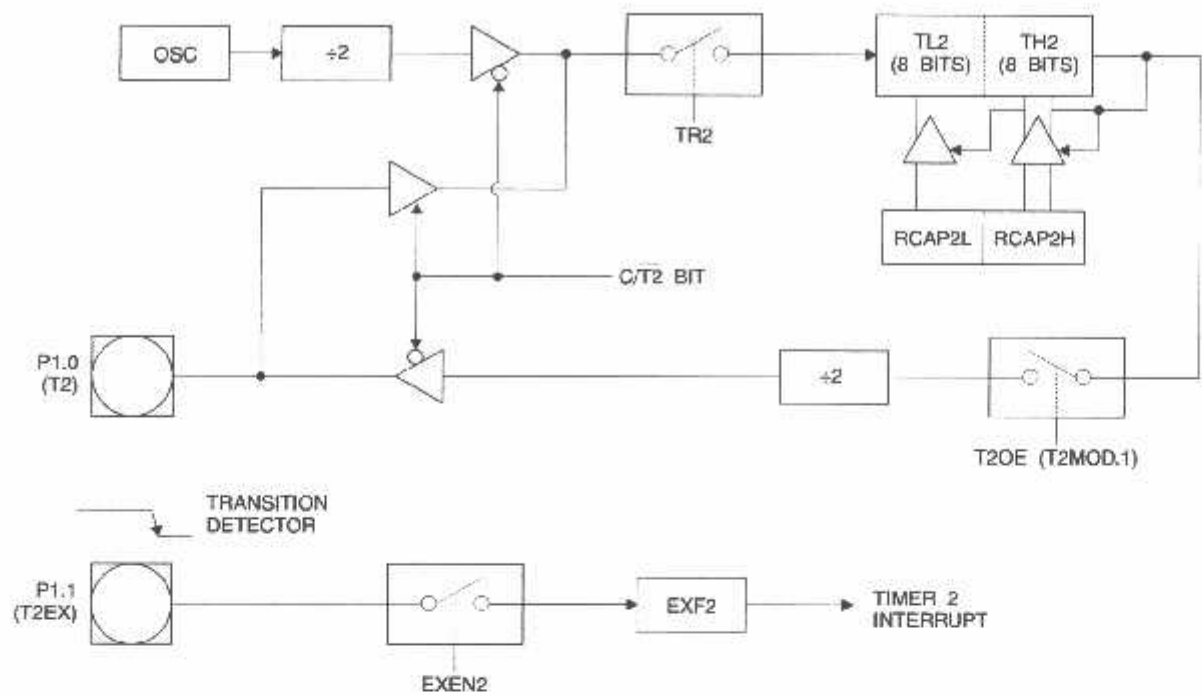
To configure the Timer/Counter 2 as a clock generator, bit C/T2 (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

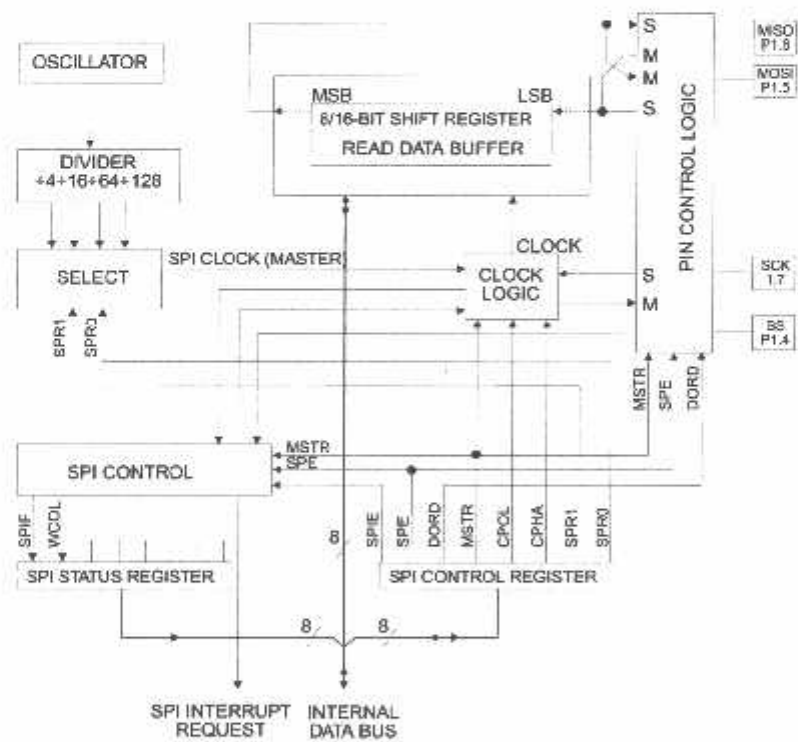
$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

re 5. Timer 2 In Clock-out Mode



re 6. SPI Block Diagram



The UART in the AT89S8252 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the Atmel web site (<http://www.atmel.com>). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5 MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

The Slave Select input, $\overline{SS}/P1.4$, is set low to select an individual SPI device as a slave. When $\overline{SS}/P1.4$ is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

Figure 7. SPI Master-slave Interconnection

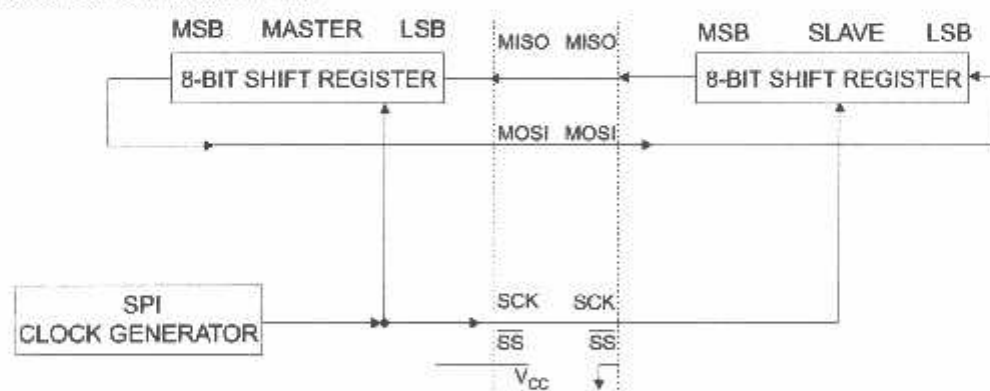
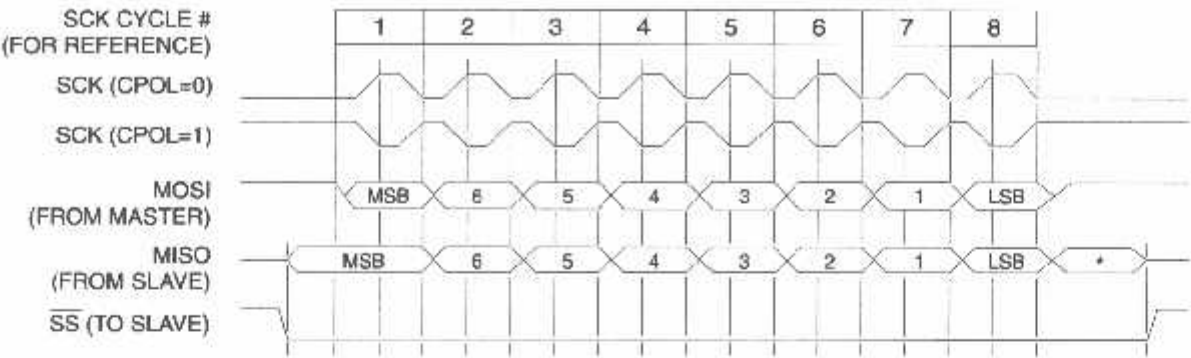
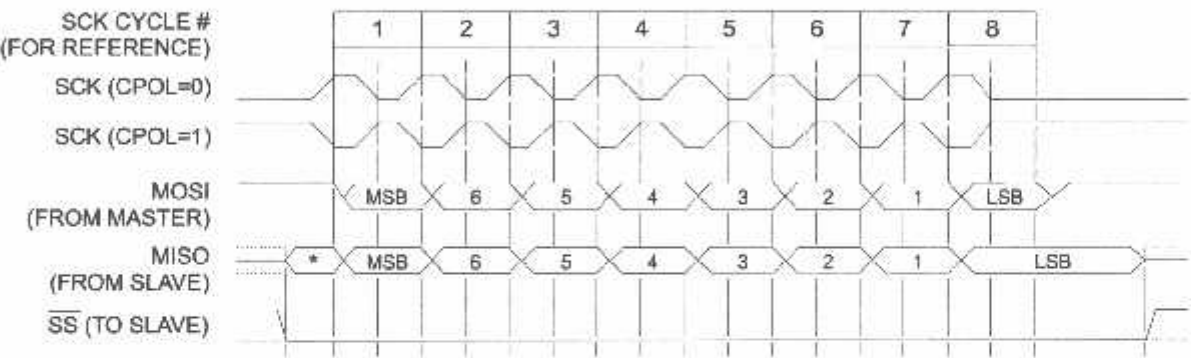


Figure 8. SPI transfer Format with CPHA = 0



*Not defined but normally MSB of character just received

Figure 9. SPI Transfer Format with CPHA = 1



*Not defined but normally LSB of previously transmitted character.

Interrupts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

10. Interrupt Enable (IE) Register

B)(LSB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0
----	---	-----	----	-----	-----	-----	-----

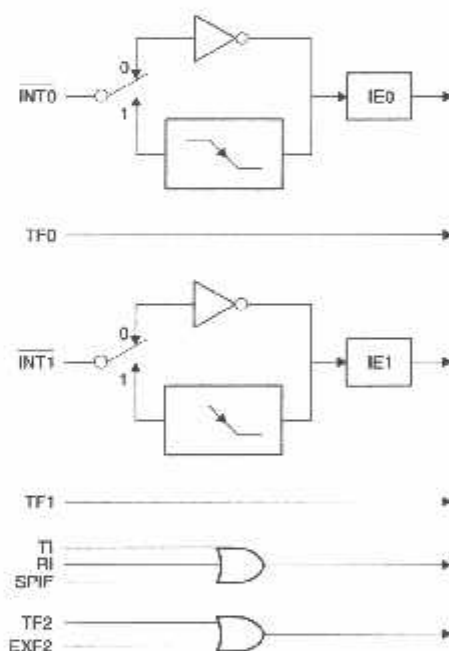
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

Software should never write 1s to unimplemented bits, because they may be used in future AT89 products.

10. Interrupt Sources



10. Interrupt Enable (IE) Register

B)(LSB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0
----	---	-----	----	-----	-----	-----	-----

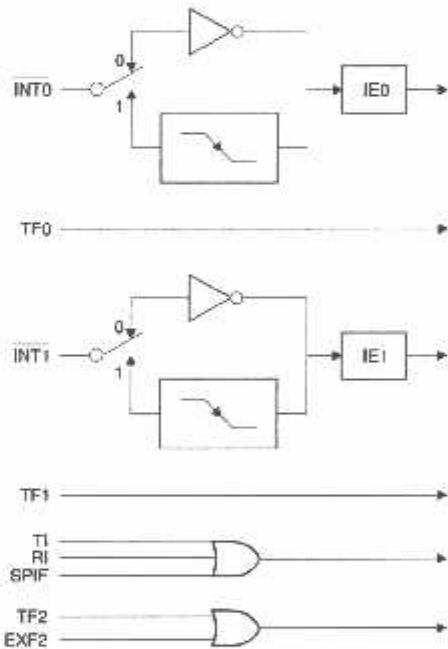
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ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

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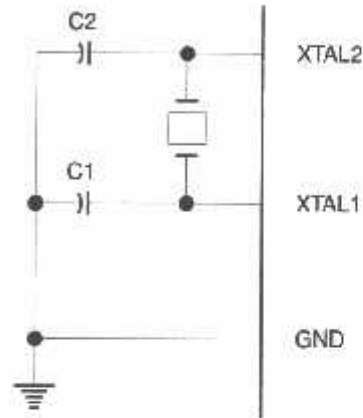
re 10. Interrupt Sources



Oscillator Characteristics

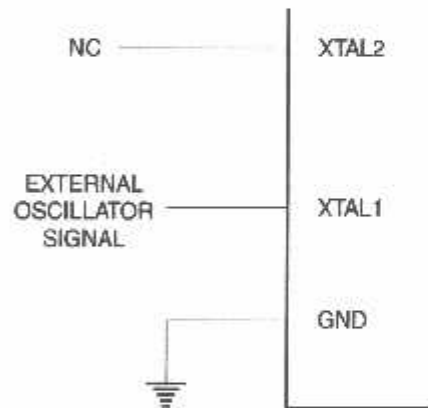
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF $\pm$ 10 pF for Crystals
 = 40 pF $\pm$ 10 pF for Ceramic Resonators

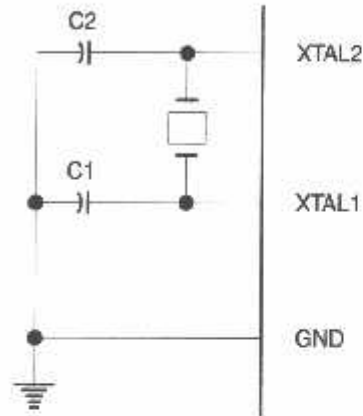
Figure 12. External Clock Drive Configuration



Oscillator Characteristics

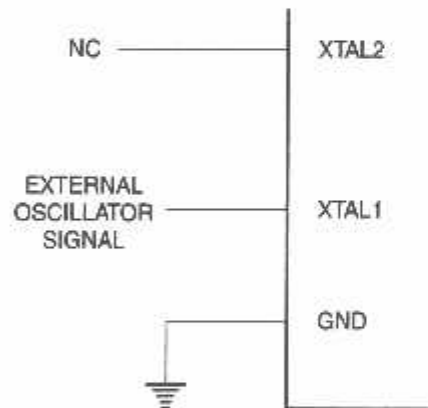
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Figure 11. Oscillator Connections



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 = 40 pF $\pm$ 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration





Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Power-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, the external interrupt must be enabled as level sensitive before entering power-down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the EA pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of EA must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Program Memory Lock Bit Protection Modes⁽¹⁾⁽²⁾

Program Lock Bits			Protection Type
LB1	LB2	LB3	
U	U	U	No internal memory lock feature.
P	U	U	MOVX instructions executed from external program memory are disabled from fetching code bytes from internal memory. EA is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
P	P	P	Same as Mode 3, but external execution is also disabled.

- 1. U = Unprogrammed
- 2. P = Programmed

AT89S8252



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Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

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P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
P	P	P	Same as Mode 3, but external execution is also disabled.

- 1. U = Unprogrammed
- 2. P = Programmed

AT89S8252

Programming the Flash and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-voltage (12-V V_{PP}) Parallel programming mode and a Low-voltage (5-V V_{CC}) Serial programming mode. The serial programming mode provides a convenient way to reprogram the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm: To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:
Apply power between V_{CC} and GND pins.
Set RST pin to "H".
Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{PSEN}$ pin to "L"
ALE pin to "H"
 $\overline{EA}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.
Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/ $\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:
Set XTAL1 to "L".
Set RST and $\overline{EA}$ pins to "L".
Turn V_{CC} power off.



In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Data Polling: The AT89S8252 features $\overline{\text{DATA}}$ Polling to indicate the end of a byte write cycle. During a byte write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{\text{DATA}}$ Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/BSY output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate BUSY. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse: A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

- (030H) = 1EH indicates manufactured by Atmel
- (031H) = 72H indicates 89S8252

programming interface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.



In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

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Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

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In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

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Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

AT89S8252

0401F-MICRO-11/03

Serial Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC} . The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Sequence

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
 Apply power between VCC and GND pins.
 Set RST pin to "H".
 If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.
6. Power-off sequence (if needed):
 Set XTAL1 to "L" (if a crystal is not used).
 Set RST to "L".
 Turn V_{CC} power off.



Serial Programming
Instruction

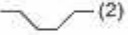
The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

Instruction Set

Instruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Chip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
Read Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Write Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
Read Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Write Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Write Lock Bits	1010 1100	LB3 LB2 LB1 x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

- Notes:
- 1. DATA polling is used to indicate the end of a byte write cycle which typically takes less than 2.5 ms at 5V.
 - 2. "aaaaa" = high order address.
 - 3. "x" = don't care.

Flash and EEPROM Parallel Programming Modes

Mode	RST	PSEN	ALE/PROG	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
Normal Prog. Modes	H	h ⁽¹⁾	h ⁽¹⁾	x						
Chip Erase	H	L	 (2)	12V	H	L	L	L	X	X
Flash (10K bytes) Memory	H	L		12V	L	H	H	H	DIN	ADDR
EEPROM (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
EEPROM Lock Bits:	H	L		12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
EEPROM Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
EEPROM Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
EEPROM Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Flash Prog. Enable	H	L	 (2)	12V	L	H	L	H	P0.0 = 0	X
Flash Prog. Disable	H	L	 (2)	12V	L	H	L	H	P0.0 = 1	X
EEPROM Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

- Notes:
- 1. "h" = weakly pulled "High" internally.
 - 2. Chip Erase and Serial Programming Fuse require a 10 ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
 - 3. P3.4 is pulled Low during programming to indicate $\overline{RDY/BSY}$.
 - 4. "X" = don't care



Figure 13. Programming the Flash/EEPROM Memory

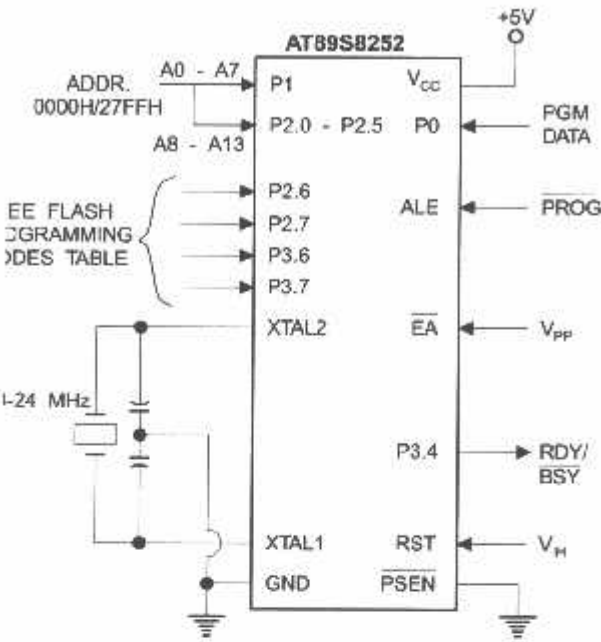


Figure 15. Flash/EEPROM Serial Downloading

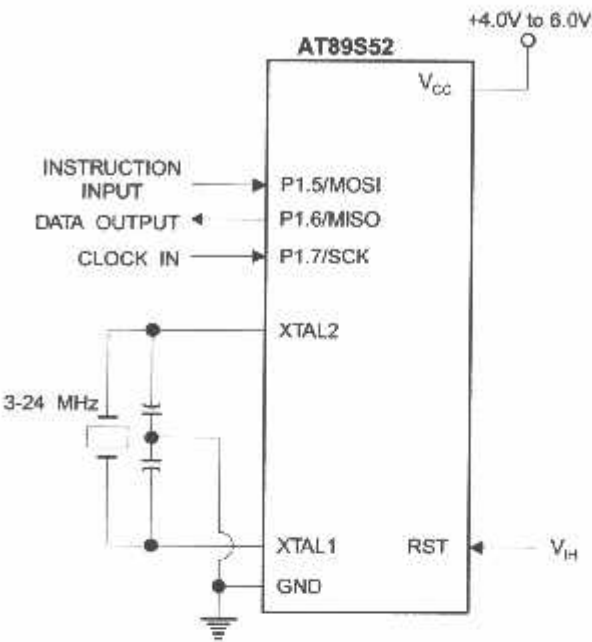
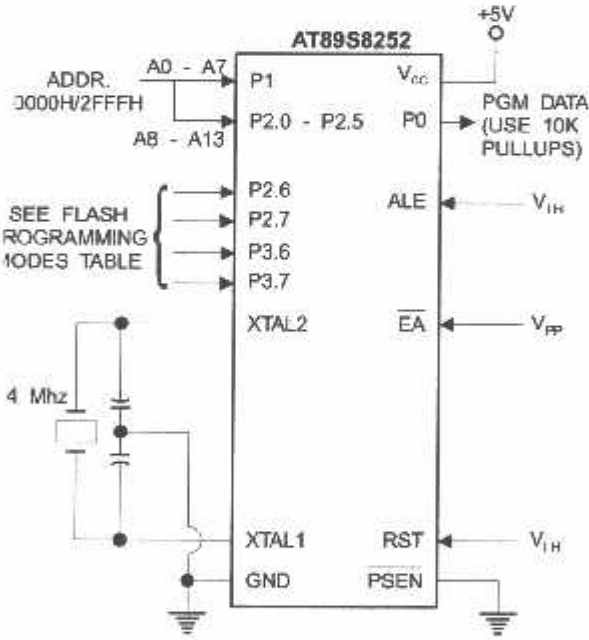


Figure 14. Verifying the Flash/EEPROM Memory

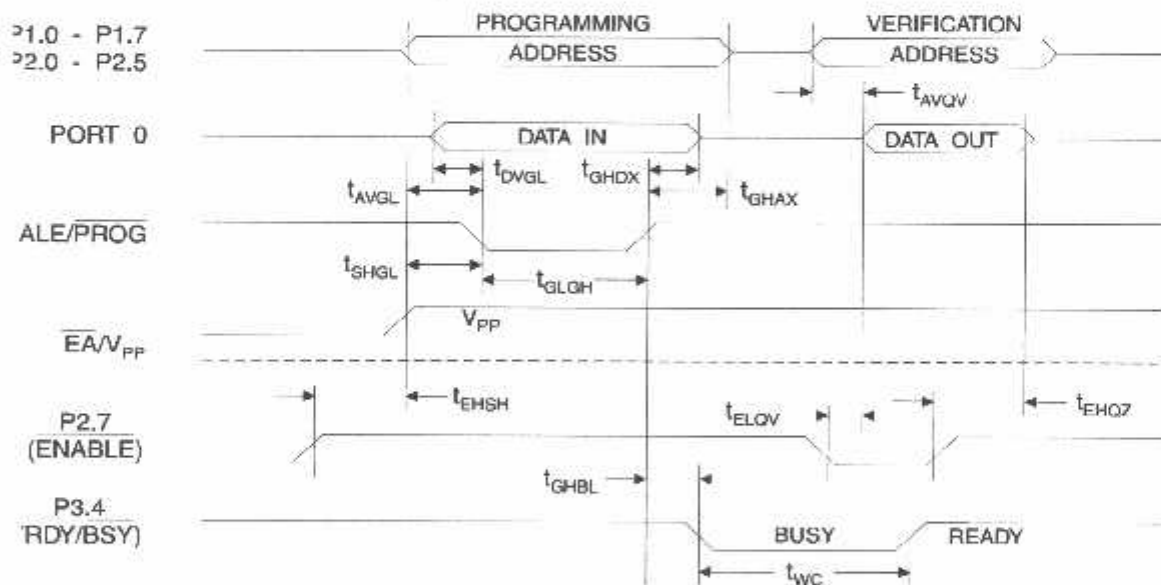


sh Programming and Verification Characteristics – Parallel Mode

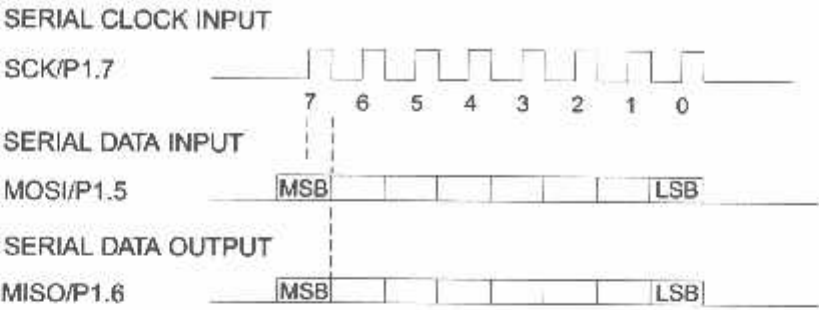
0°C to 70°C, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Min	Max	Units
	Programming Enable Voltage	11.5	12.5	V
	Programming Enable Current		1.0	mA
f_{CL}	Oscillator Frequency	3	24	MHz
t_{CL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{CX}	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{DX}	Data Hold after $\overline{PROG}$	$48t_{C_CL}$		
t_{EH}	P2.7 (ENABLE) High to V_{PP}	$48t_{CLCL}$		
t_{EL}	V_{PP} Setup to $\overline{PROG}$ Low	10		μs
t_{EH}	$\overline{PROG}$ Width	1	110	μs
t_{EV}	Address to Data Valid		$48t_{CLCL}$	
t_{DV}	ENABLE Low to Data Valid		$48t_{CLCL}$	
t_{ZF}	Data Float after ENABLE	0	$48t_{CLCL}$	
t_{HL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	μs
	Byte Write Cycle Time		2.0	ms

sh/EEPROM Programming and Verification Waveforms – Parallel Mode



Serial Downloading Waveforms



Serial Programming Characteristics

Figure 16. Serial Programming Timing

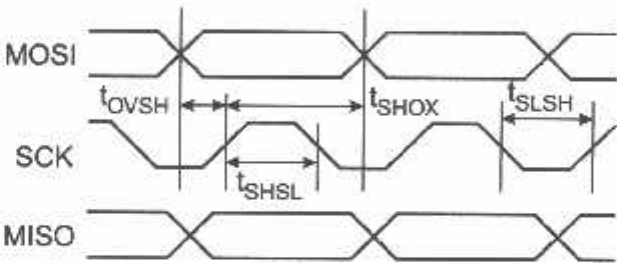


Table 11. Serial Programming Characteristics, $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 4.0 - 6.0\text{V}$ (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{CL}	Oscillator Frequency	0		24	MHz
T	Oscillator Period	41.6			ns
t_{H}	SCK Pulse Width High	$24 t_{CLCL}$			ns
t_{L}	SCK Pulse Width Low	$24 t_{CLCL}$			ns
t_{SU}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{H}	MOSI Hold after SCK High	$2 t_{CLCL}$			ns

Absolute Maximum Ratings*

Storage Temperature.....	-55°C to +125°C
Package Temperature	-65°C to +150°C
Power Dissipation on Any Pin Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
Output Current.....	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

Values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V _{CC} - 0.1	V
	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V _{CC} - 0.3	V
	Input High-voltage	(Except XTAL1, RST)	0.2 V _{CC} + 0.9	V _{CC} + 0.5	V
	Input High-voltage (XTAL1, RST)		0.7 V _{CC}	V _{CC} + 0.5	V
	Output Low-voltage ⁽¹⁾ (Ports 1,2,3)	I _{OL} = 1.6 mA		0.5	V
	Output Low-voltage ⁽¹⁾ (Port 0, ALE, $\overline{PSEN}$)	I _{OL} = 3.2 mA		0.5	V
	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I _{OH} = -60 μA, V _{CC} = 5V ± 10%	2.4		V
		I _{OH} = -25 μA	0.75 V _{CC}		V
		I _{OH} = -10 μA	0.9 V _{CC}		V
	Output High-voltage (Port 0 in External Bus Mode)	I _{OH} = -800 μA, V _{CC} = 5V ± 10%	2.4		V
		I _{OH} = -300 μA	0.75 V _{CC}		V
		I _{OH} = -80 μA	0.9 V _{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V _{IN} = 0.45V		-50	μA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V _{IN} = 2V, V _{CC} = 5V ± 10%		-850	μA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V _{IN} < V _{CC}		±10	μA
T	Reset Pull-down Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T _A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode ⁽²⁾	V _{CC} = 6V		100	μA
		V _{CC} = 3V		40	μA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA; Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V



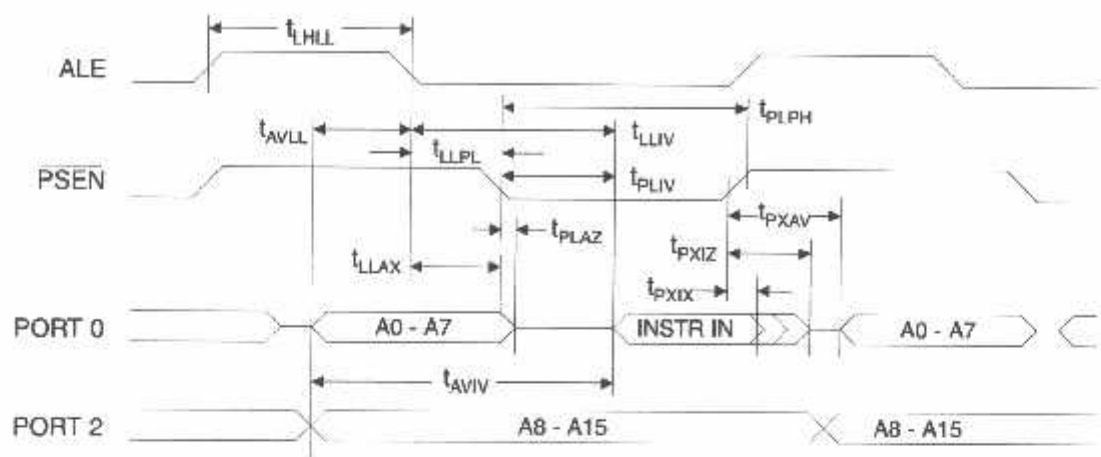
Characteristics

For operating conditions, load capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; load capacitance for all other pins = 80 pF.

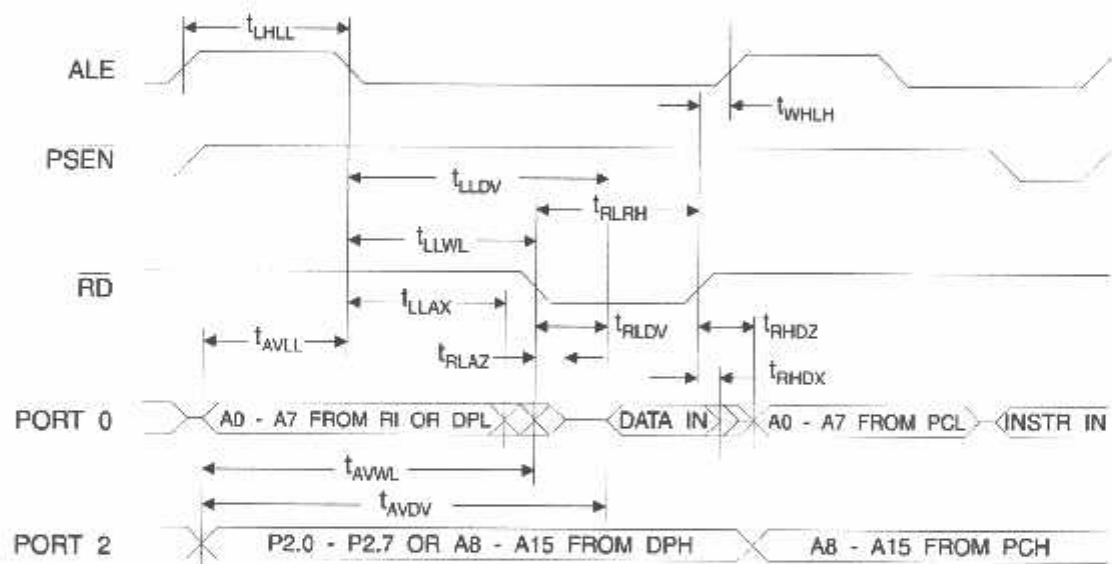
Internal Program and Data Memory Characteristics

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
f _{CL}	Oscillator Frequency	0	24	MHz
t _W	ALE Pulse Width	2t _{CL} - 40		ns
t ₁	Address Valid to ALE Low	t _{CL} - 13		ns
t ₂	Address Hold after ALE Low	t _{CL} - 20		ns
t ₃	ALE Low to Valid Instruction In		4t _{CL} - 65	ns
t ₄	ALE Low to PSEN Low	t _{CL} - 13		ns
t ₅	PSEN Pulse Width	3t _{CL} - 20		ns
t ₆	PSEN Low to Valid Instruction In		3t _{CL} - 45	ns
t ₇	Input Instruction Hold after PSEN	0		ns
t ₈	Input Instruction Float after PSEN		t _{CL} - 10	ns
t ₉	PSEN to Address Valid	t _{CL} - 8		ns
t ₁₀	Address to Valid Instruction In		5t _{CL} - 55	ns
t ₁₁	PSEN Low to Address Float		10	ns
t ₁₂	RD Pulse Width	6t _{CL} - 100		ns
t ₁₃	WR Pulse Width	6t _{CL} - 100		ns
t ₁₄	RD Low to Valid Data In		5t _{CL} - 90	ns
t ₁₅	Data Hold after RD	0		ns
t ₁₆	Data Float after RD		2t _{CL} - 28	ns
t ₁₇	ALE Low to Valid Data In		8t _{CL} - 150	ns
t ₁₈	Address to Valid Data In		9t _{CL} - 165	ns
t ₁₉	ALE Low to RD or WR Low	3t _{CL} - 50	3t _{CL} + 50	ns
t ₂₀	Address to RD or WR Low	4t _{CL} - 75		ns
t ₂₁	Data Valid to WR Transition	t _{CL} - 20		ns
t ₂₂	Data Valid to WR High	7t _{CL} - 120		ns
t ₂₃	Data Hold after WR	t _{CL} - 20		ns
t ₂₄	RD Low to Address Float		0	ns
t ₂₅	RD or WR High to ALE High	t _{CL} - 20	t _{CL} + 25	ns

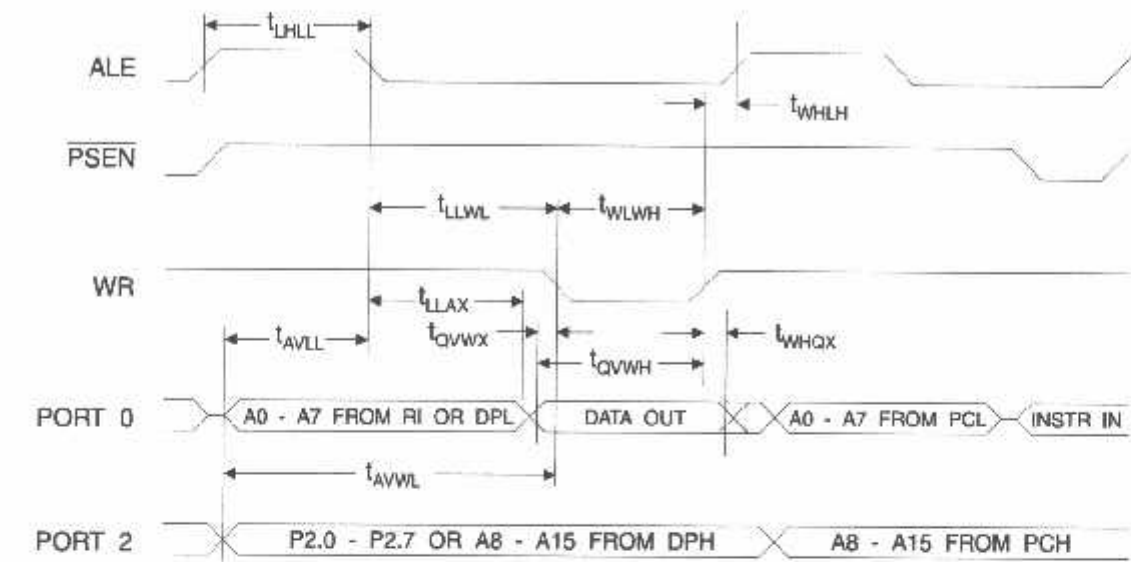
ernal Program Memory Read Cycle



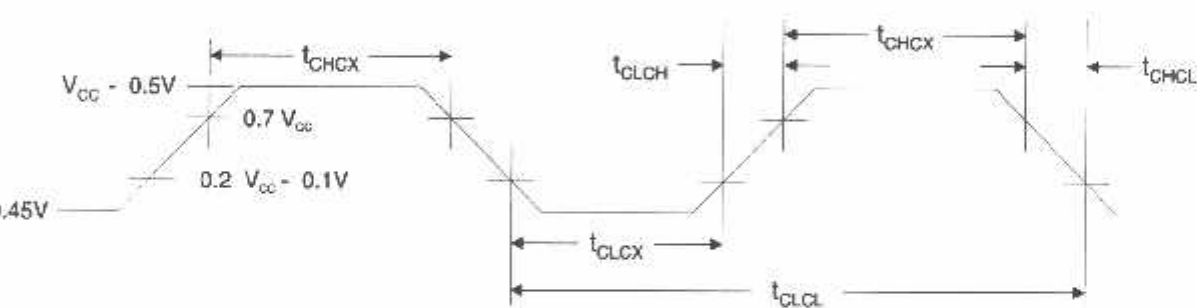
ernal Data Memory Read Cycle



Internal Data Memory Write Cycle



Internal Clock Drive Waveforms



Internal Clock Drive

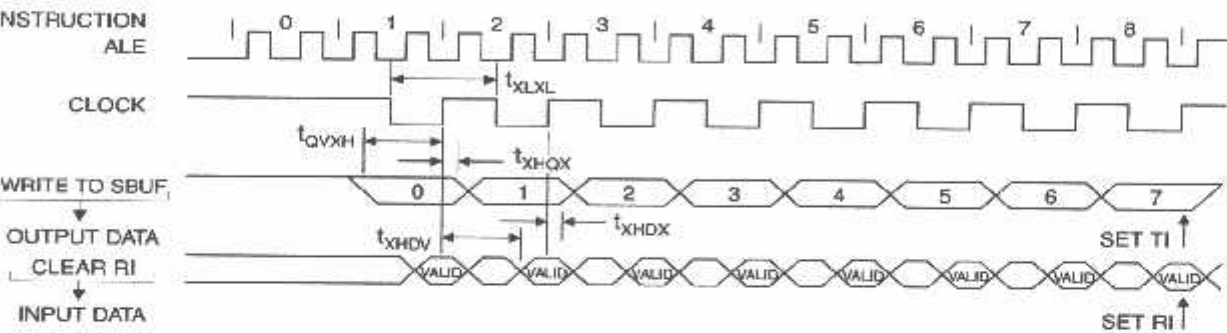
Symbol	Parameter	$V_{CC} = 4.0V \text{ to } 6.0V$		Units
		Min	Max	
f_{CL}	Oscillator Frequency	0	24	MHz
	Clock Period	41.6		ns
	High Time	15		ns
	Low Time	15		ns
	Rise Time		20	ns
	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

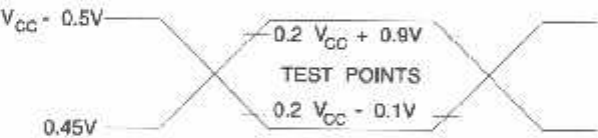
values in this table are valid for $V_{CC} = 4.0V$ to $6V$ and Load Capacitance = 80 pF .

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
	Serial Port Clock Cycle Time	$12t_{CLCL}$		μs
t_{DHS}	Output Data Setup to Clock Rising Edge	$10t_{CLCL} - 133$		ns
t_{DHO}	Output Data Hold after Clock Rising Edge	$2t_{CLCL} - 117$		ns
t_{DIO}	Input Data Hold after Clock Rising Edge	0		ns
t_{DVI}	Clock Rising Edge to Input Data Valid		$10t_{CLCL} - 133$	ns

Shift Register Mode Timing Waveforms

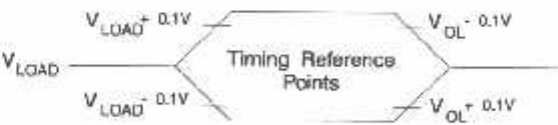


Testing Input/Output Waveforms⁽¹⁾



- 1. AC Inputs during testing are driven at $V_{CC} - 0.5V$ for a logic 1 and $0.45V$ for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

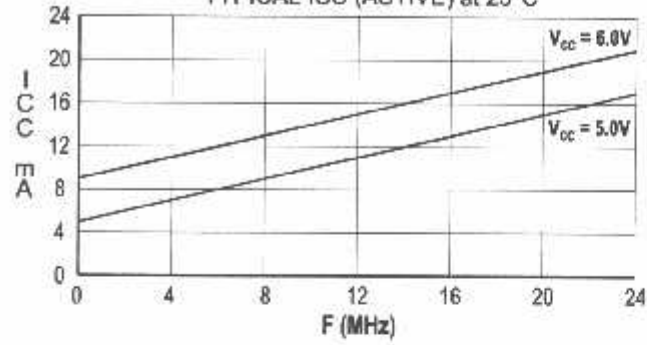
Load Waveforms⁽¹⁾



- 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

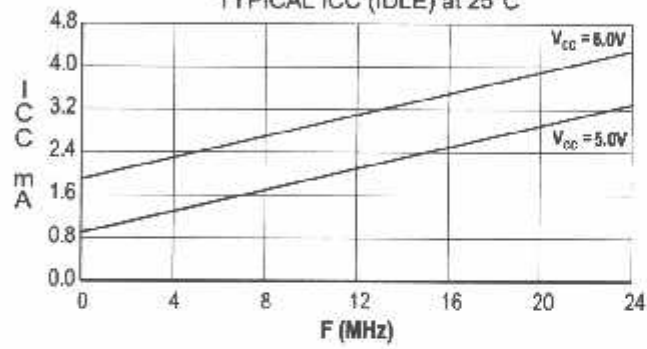
AT89S8252

TYPICAL I_{CC} (ACTIVE) at 25°C



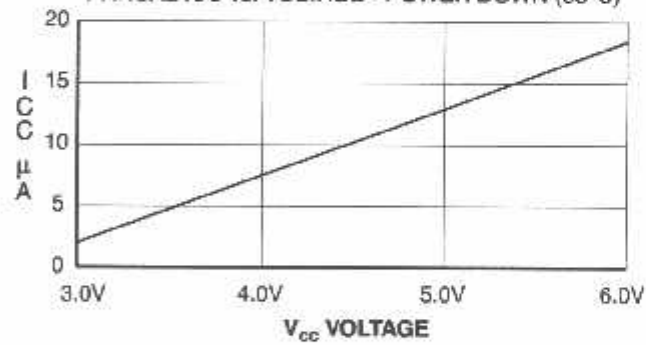
AT89S8252

TYPICAL I_{CC} (IDLE) at 25°C



AT89S8252

TYPICAL I_{CC} vs. VOLTAGE - POWER DOWN (85°C)



- Notes:
1. XTAL1 tied to GND for I_{CC} (power-down)
 2. Lock bits programmed

Ordering Information

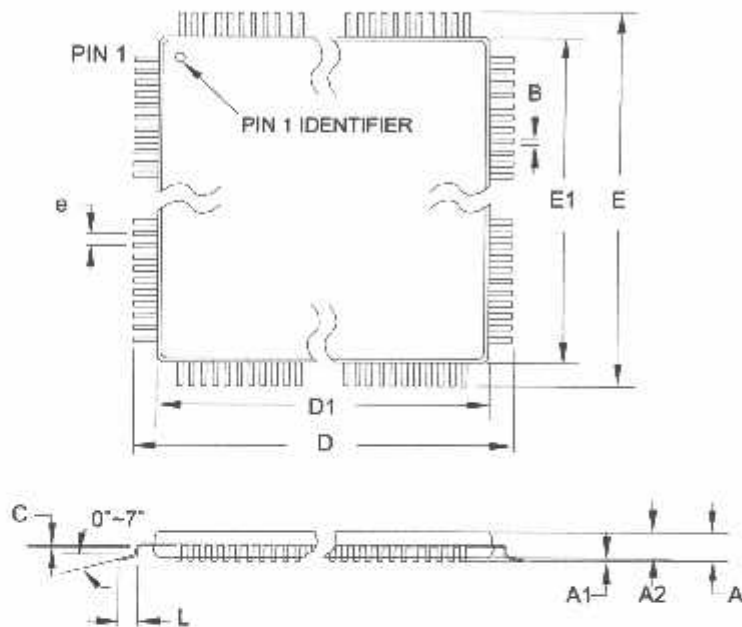
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 6.0V	AT89S8252-24AC AT89S8252-24JC AT89S8252-24PC	44A 44J 40P6	Commercial (0° C to 70° C)
	4.0V to 6.0V	AT89S8252-24AI AT89S8252-24JI AT89S8252-24PI	44A 44J 40P6	Industrial (-40° C to 85° C)

Package Type	
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)



Packaging Information

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

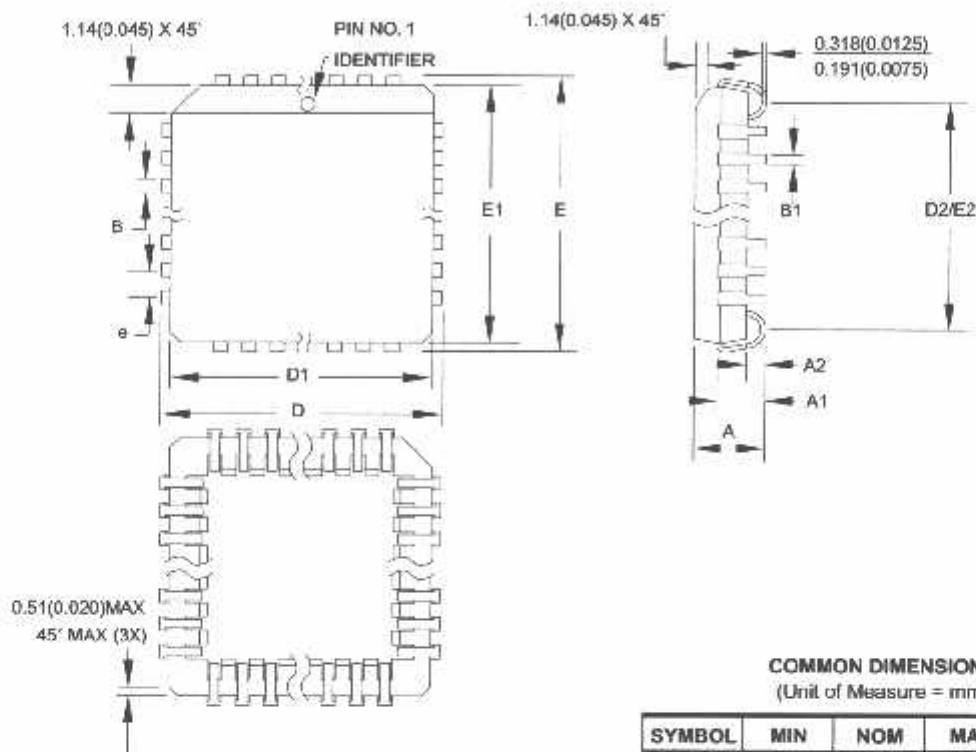
- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

2325 Orchard Parkway San Jose, CA 95131	TITLE 44A, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	DRAWING NO. 44A	REV. B

AT89S8252

– PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

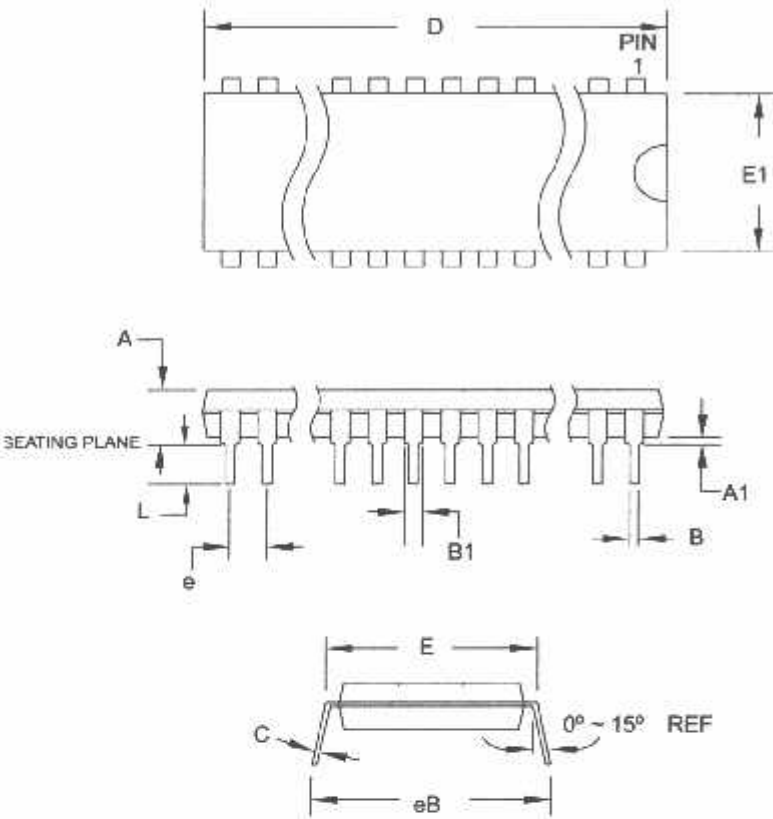
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

- Notes:
- 1. This package conforms to JEDEC reference MS-018, Variation AC.
 - 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 - 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

 2325 Orchard Parkway San Jose, CA 95131	TITLE 44J , 44-lead, Plastic J-leaded Chip Carrier (PLCC)	DRAWING NO.	REV.
		44J	B

6 – PDIP



- Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
 2. Dimensions D and E1 do not include mold Flash or Protrusion.
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	4.826	
A1	0.381	—	—	
D	52.070	—	52.578	Note 2
E	15.240	—	15.875	
E1	13.462	—	13.970	Note 2
B	0.356	—	0.559	
B1	1.041	—	1.651	
L	3.048	—	3.556	
C	0.203	—	0.381	
eB	15.494	—	17.526	
e	2.540 TYP			

09/28/01

	2325 Orchard Parkway San Jose, CA 95131	TITLE 40P6, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	DRAWING NO.	REV.
			40P6	B



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