Table 4. SPCR—SPI Control Register

SPCR Address = D5H — Reset Value = 0000 01XXB

Bit	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
	7	6	5	4	3	2	1	0

Symbol	Function
SPIE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
CPOL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
CPHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
SPR0 SPR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{osc.}$, is as follows: SPR1 SPR0 SCK = $F_{osc.}$ divided by 0 0 4 0 1 16 1 0 64 1 1 128

Table 5. SPSR—SPI Status Register

SPSR Address = AAH — Reset Value = 00XX XXXXB

Bit	SPIF	WCOL	—	—	—	—	—	—
	7	6	5	4	3	2	1	0

Symbol	Function
SPIF	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then accessing the SPI data register.
WCOL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

LEMBAR PERSETUJUAN

PERENCANAAN DAN PEMBUATAN
BUILDING AUTOMATION SYSTEM PADA KOMPLEKS
PERKANTORAN BERBASIS MIKROKONTROLLER AT89S8252
DAN DIANTARMUKAKAN KE PERSONAL COMPUTER (PC)

SKRIPSI

Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektronika Strata Satu (S-1)

Disusun Oleh :

DONI BUDI PRASETYO
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PERENCANAAN DAN PEMBUATAN BUILDING AUTOMATION SYSTEM PADA KOMPLEKS PERKANTORAN BERBASIS MIKROKONTROLLER AT89S8252 DAN DIANTARMUKAKAN KE PERSONAL KOMPUTER (PC)

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ABSTRAKSI

PERENCANAAN DAN PEMBUATAN BUILDING AUTOMATION SYSTEM PADA KOMPLEKS PERKANTORAN BERBASIS MIKROKONTROLLER AT89S8252 DAN DIANTARMUKAKAN KE PERSONAL COMPUTER (PC)

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Kata Kunci: Building Automation System, Personal Computer, AT89S8252.

Karena adanya perkembangan teknologi yang sangat pesat dan melihat kebutuhan manusia yang semakin meningkat, maka banyak alat yang dapat ditunjukan kepada konsumen guna mempermudah, mempercepat, dan memperingan dalam menyelesaikan suatu pekerjaan. Faktor inilah yang mendorong kami untuk mengangkat judul skripsi: **"Perencanaan Dan Pembuatan Building Automation System Pada Kompleks Perkantoran Berbasis Mikrokontroller AT89S8252 Dan Diantarmukakan Ke Personal Computer (PC)".**

Pada dasarnya sistem ini adalah sebuah sistem pengendali perangkat-perangkat yang berada didalam sebuah bangunan atau kompleks perkantoran yang dapat dikontrol dan dimonitor oleh sebuah Personal Computer (PC).

Sistem ini menggunakan komunikasi data serial dengan teknologi RS-485 yang memiliki keunggulan lebih tahan terhadap gangguan-gangguan dari luar, selain itu juga memiliki jarak jangkauan komunikasi data yang lebih jauh.

Setelah sistem/alat ini terwujud kami berharap semoga dapat bermanfaat bagi kita semua.

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BAB I

PENDAHULUAN

1.1. Latar Belakang

Kita semua tentunya mengetahui bahwa ilmu pengetahuan dan teknologi pada masa sekarang ini sangat berkembang pesat dan telah menampakkan keunggulannya, terutama dalam bidang elektronika yang hampir mendominasi segala hal mulai dari lingkup yang paling besar sampai dengan yang paling terkecil. Penemuan teknologi baru tidak lepas dari penemuan-penemuan elemen lama yang dikembangkan menjadi teknologi baru. Dengan melihat kebutuhan manusia yang semakin meningkat, sehingga banyak alat yang dapat ditunjukan kepada konsumen guna mempermudah, mempercepat, dan memperingan dalam menyelesaikan suatu pekerjaan.

Faktor inilah yang mendorong kami untuk mengangkat judul skripsi: **"Perencanaan Dan Pembuatan Building Automation System Pada Kompleks Perkantoran Berbasis Mikrokontroller AT89S8252 Dan Diantarmukakan Ke Personal Computer (PC)"**, yaitu suatu sistem/alat yang dapat mengontrol perangkat-perangkat yang berada di dalam ruang-ruang perkantoran melalui sebuah Personal Computer (PC).

Setelah sistem/alat ini terwujud kami berharap semoga dapat bermanfaat bagi kita semua untuk mempermudah, mempercepat, dan memperingan dalam menyelesaikan suatu pekerjaan.

1.2. Rumusan Masalah

Dari latar belakang yang telah dikemukakan diatas, maka rumusan masalah yang kami hadapi adalah :

1. Bagaimana kita dapat membuat sistem/alat yang bisa mengontrol perangkat-perangkat yang berada di dalam ruang-ruang perkantoran melalui satu tempat atau sebuah ruang kontrol.
2. Bagaimana merencanakan dan membuat perangkat keras (hardware) dari sistem ini.
3. Bagaimana merencanakan dan membuat perangkat lunak (software) yang berfungsi untuk mengendalikan sistem ini.

1.3. Tujuan

Dari permasalahan yang ada, maka tujuan perencanaan dan pembuatan sistem ini adalah :

1. Dapat merencanakan dan membuat sebuah Building Automation System Pada Kompleks Perkantoran Berbasis Mikrokontroller AT89S8252 Dan Diantarmukakan Ke Personal Computer (PC).
2. Dapat membuat sistem/alat yang dapat mempermudah, mempercepat, dan memperingan dalam menyelesaikan suatu pekerjaan.

1.4. Batasan Masalah

Agar permasalahan yang dibahas tidak meluas maka perlunya pembatasan permasalahan. Adapun batasan masalah yang meliputi :

1. Sebagai pusat kontrol menggunakan Personal Computer (PC).
2. Sistem/alat ini menggunakan mikrokontroller AT89S8252.
3. Sistem yang digunakan hanya dibatasi untuk 2 unit.
4. Sistem dibatasi hanya untuk mengontrol penguncian pintu, pengontrol lampu ruang dan lampu otomatis, serta pengaktifan sistem keamanan.

1.5. Metodologi Penulisan

Adapun metodologi penulisan yang digunakan dalam menyusun analisa skripsi ini adalah:

1. Studi literatur.
2. Perencanaan dan pembuatan alat.

   Merencanakan alat yang telah dirancang baik software maupun hardware.
3. Pengujian alat.

   Peralatan yang telah dibuat kemudian diuji apakah telah sesuai dengan yang direncanakan.
4. Penyusunan laporan

1.6. Sistematika Penulisan

Penulisan skripsi ini terbagi dalam lima bab dengan sistematika sebagai berikut :

BAB I PENDAHULUAN

Berisi latar belakang permasalahan, rumusan masalah, tujuan, batasan masalah, metodologi penulisan, dan sistematika penulisan.

BAB II TEORI PENUNJANG

Membahas teori-teori dasar penunjang perancangan dan pembuatan alat ini.

BAB III PERANCANGAN DAN PEMBUATAN ALAT

Membahas tentang teori dasar rangkaian yang akan digunakan.

BAB IV PENGUJIAN ALAT

Mencakup pembahasan tentang proses pengujian alat yang terdiri dari peralatan yang digunakan, langkah kerja dan analisa hasil pengujian .

BAB V PENUTUP

Berisi kesimpulan dari pembahasan pada bab-bab sebelumnya dan kemungkinan pengembangan alat.

BAB II

LANDASAN TEORI

Bab ini akan menguraikan tentang dasar-dasar teori yang dapat menunjang dalam perencanaan dan pembuatan alat. Uraian teori dalam bab ini meliputi: IC AT89S8252, RS-485/RS-422, RS-232, transistor, *operational amplifier* (op-amp), *relay*, *limit switch*, LDR, LED infra merah & photodioda, solenoid.

2.1. Mikrokontroller AT89S8252

Mikrokontroller AT89S8252 adalah mikrokontroller ATMEL yang kompatibel, memerlukan daya yang rendah, memiliki performa tinggi dan merupakan mikrokontroller 8 bit yang dilengkapi 2 Kbyte EEPROM (*Electrical Eraseble and Programmable Read Only Memory*) dan 256 byte RAM *internal*. Program memori yang dapat diprogram ulang dalam sistem atau menggunakan programmer non folatile memori konvensional.

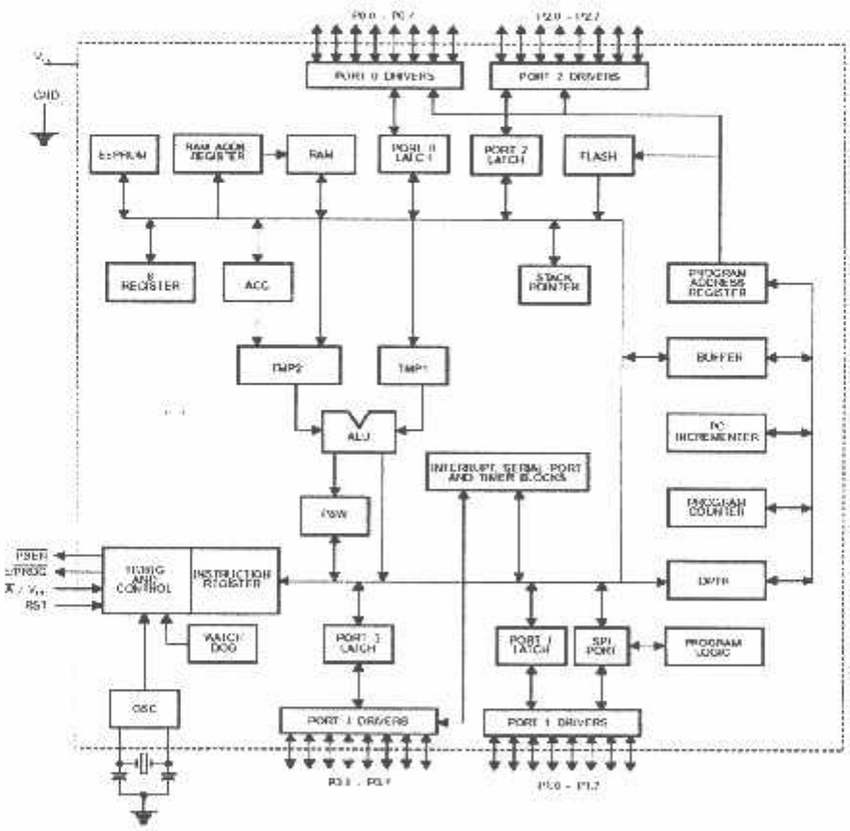
2.1.1. Arsitektur mikrokontroller AT89S8252

Arsitektur mikrokontroller AT89S8252 adalah sebagai berikut:

- Termasuk dalam keluarga MCS 51
- Membutuhkan supply tegangan yang relatif kecil (4V-6V)
- 8 Kbyte *flash memory*

- 2 Kbyte EEPROM
- 256 byte *internal memory*
- 3 x 16 bit *timer/counter*
- 32 pin I/O
- 9 Buah sumber *interupt*
- 2 buah data pointer
- 1 serial port full duplex

2.1.2. Diagram Blok AT89S8252

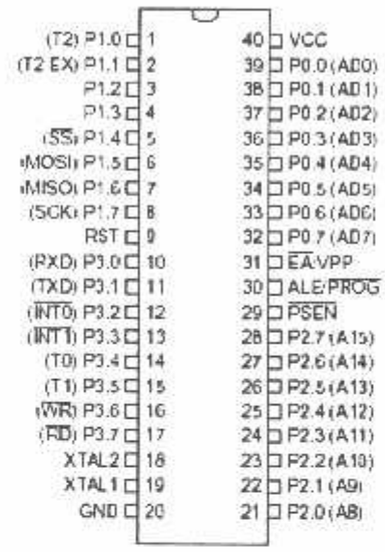


Gambar 2.1

Diagram Blok Mikrokontroller AT89S8252 [7]

2.1.3. Konfigurasi Pin Pada Mikrokontroller AT89S8252

Konfigurasi kaki-kaki mikrokontroller AT89S8252 terdiri dari 40 pin, seperti terlihat pada gambar 2.2 sebagai berikut:



Gambar 2.2

Konfigurasi Pin Mikrokontroller AT89S8252 [7]

Fungsi dari tiap-tiap pin adalah sebagai berikut:

1. VCC (supply tegangan)
2. GND (*Ground*)
3. Port 0

   Merupakan port *input/output* dua arah dan dikonfigurasikan sebagai *multiplex* dua bus alamat rendah (A0-A7) dan data selama pengaksesan program memori dan data memori *internal*
4. Port 1

   Merupakan port *input/output* dua arah dengan *internal pull-up*

5. Port 2

   Merupakan port *input/output* dua arah dengan *internal pull-up* mengeluarkan *address* tinggi selama pengambilan program *memory external*.

6. Port 3

   Merupakan port *input/output* dua arah dengan *internal pull-up*

   Port 3 memiliki fungsi khusus, yaitu:

   - RXD (P3.0) : port *input* serial
   - TXD (P3.1) : port *output* serial
   - INT0 (P3.2) : *interrupt 0 external*
   - INT1 (P3.3) : *interrupt 1 external*
   - T0 (P3.4) : *input external timer* 0
   - T1 (P3.5) : *input external timer* 1
   - /WR (P3.6) : strobe tulis *memory data external*
   - /RD (P3.7) : strobe baca *memory data external*

7. RST

   Input reset

8. ALE / PROG

   Pulsa *output* ALE digunakan untuk proses *"latching"* byte *address* rendah (A0-A7) selama pengaksesan ke memori *external*. Pin ini juga untuk memasukan pulsa program selama pemrograman.

9. PSEN

   Merupakan strobe baca ke program memori *external*.

10. EA / VPP

Jika EA diberikan logika rendah (*ground*), maka mikrokontroller akan mengakses program dari memori *external* dan jika diberi logika tinggi (dihubungkan VCC), maka akan mengakses program dari memori *internal.*

11. XTAL1 DAN XTAL 2

Pin ini dihubungkan dengan kristal bila menggunakan osilator *internal.* XTAL1 merupakan masukan ke rangkaian osilator *internal* sedangkan XTAL2 keluaran dari rangkaian osilator *internal.*

2.1.4. SFR Tambahan Pada Atmel AT89S8252

Selain memiliki SFR(*Special Function Register*) seperti halnya pada MCS-51, mikrokontroler ATMEL AT89S8252 memiliki tambahan SFR. Hal ini tak lain adalah karena adanya fitur tambahan pada mikrokontroler ATMEL AT89S8252.

SFR tambahan ini meliputi: T2CON(Timer 2 Register dangan alamat 0C8H), T2MOD(*Timer 2 Mode* dengan alamaat 0C9H), WMCON(*Watchdog and Memory Control Register* dengan alamat 96H), SPCR(*SPI Control Register* dengan alamat D5H), SPSR(*SPI Status Refister* dengan alamat AAH), SPDR(SPI Data Register dengan alamat 86H).

2.1.5. Data Memory (EEPROM) dan RAM

Berbeda dengan mokrokontroler standart MCS-51, mikrokontroler ATMEL AT89S8252 juga dilengkapi dengan data memori yang berupa EEPROM (*Electrically Erasable Programmable Read Only Memory*). EEPROM yang ditanamkan ini besarnya 2 Kbyte (2K) dan dipakai untuk penyimpanan data.

EEPROM ini diakses dengan mengeset bit EEMEN pada registerWMCON pada alamat 96H. Alamat EEPROM ini adalah 000H sampai 7FFH. Instruksi movx digunakan untuk mengakses EEPROM *internal* ini. Namun jika ingin mengakses data memori luar (diluar mikrokontroler ATMEL AT89S8252) dengan menggunakan instruksi movx ini maka bit EEMEN harus dibuat"0".

Bit EEMWE pada register WMCON harus diset ke 1 sebelum sembarang lokasi padaEEPROM dapat ditulisi. Program pengguna harus mereset bit EEMWE ke "0" jika proses penulisan ke EEPROM tidak diperlukan lagi. Proses penulisan pada EEPROM dapat dilihatdengan membaca bt RDY/BSY pada SFR WMCON. Jika bit ini berlogika rendah maka penulisan EEPROM sedang berlangsung, jika bit ini berlogika tinggi maka penulisan sudah selesai dan penulisan lain dapat dimulai lagi. Sedangkan RAM yang ada pada mikrokontroler ATMEL AT89S8252 adalah berkapasitas 256 *byte*. Penjelasan mengenai RAM ini adalah sama dengan RAM yang ada pada mikrokontroler standart MCS-51.

2.1.6. Programable Watchdog Timer (WDT)

Pada mikrokontroler ATMEL AT89S8252 juga dilkengkapi oleh *watchdog Timer*. *Watchdog Timer* ini menggunakan detak tersendiri. Untuk

mengatur rentang waktu (perioda) pada WDT ini maka terdapat bit prescaler yang dapat mengatur rentang waktu yang dibutuhkan.

Bit prascaler ini adalah bit PS0, PS1dan PS2 pada register WMCON. Perioda waktu pada WDT ini berkisar dari 16 mili detik sampai 2048 mili detik. Karena bit prescalernya ada 3, maka akan ada 8 buah kemungkinan yaitu:

Tabel 2.1
Pemilihan Perioda Waktu WDT [7]

PS2	PS1	PS0	Perioda
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

WDT dilumpuhkan oleh Power on Reset (POR) dan selama Power Down. WDT diaktifkan dengan menseting bit WDTEN pada SFR WMCON (alamat 96H). Jjika perhitungan waktu WDT telah selesai tanpa ada reset atau dilumpuhkan, maka suatu pulsa reset internal akan dihasilkan untuk mereset CPU.

2.1.7. Timer 2

Pada mikrokontroler Atmel AT89S8252 terdapat tambahan *Timer* 2. *Timer* yang lain adalah *timer* 0 dan *timer* 1. Hal yang perlu diperhatikan adalah *Timer/Counter* dapat digunakan sebagai generator *baudrate* untuk serial *port*. Pada standart MS-51 biasanya yang digunakan adalah *timer* 1 sebagai penghasil *baudrate*. Pada mikrokontroler Atmel AT89S8252 selain menggunakan *timer* 1 sebagai *baudrate* (untuk menjaga kompabilitas dengan MCS-51) juga dapat menggunakan *Timer* 2 sebagai penghasil *baudrate* untuk serial *port*. *Timer* 2 ini merupakan Timer/Counter yang berukuran 16 bit yang dapat beroperasi sebagai timer atau dapat beroperasi sebagai penghitung kejadian dengan detak dari luar. Untuk mengatur fungsi ini dilakukan dengan mengatur bit C/T2 pada SFR T2CON. Terlihat bahwa jika bit ini tinggi maka akan terpilih fungsai *counter*, tapi jika bit ini rendah maka akan terpilih fungsi *Timer* 2.

Timer 2 ini memiliki 3 mode operasi yaitu: *capture, auto reload (up dan down counting)* dan *baud rate* generator. Untuk memilih mode ini dilakukan dengan mengatur bit pada SFR T2CON.

Timer 2 ini terdiri dari 2 buah *timer* 8 bit *register* yaitu TH2 dan TL2 dinaikkan tiap siklus mesin. Karena siklus mesin terdiri dari 1 *periode* osilasi, maka *count rate* menjadi 1/12 dari frekuensi osilator.

Pada fungsi *counter, register* dinaikkan berdasarkan tanggapan adanya transisi tinggi ke rendah pada pena yang bersesuaian (dalam hal ini pin T2 atau Pi.0). pada fungsi ini, masukan luar akan disampling selama S5P2 dari tiap siklus mesin. Jika hasil sampling menunjukkan logika tinggi pada selama satu siklus dan

logika rendah pada siklus selanjutnya maka akan terdeteksi transisi tinggi ke rendah dan akibatnya perhitungan akan dinaikkan. Nilai perhitungan yang baru akan muncul pada register selama S3P1 dari siklus setelah transisi tinggi ke rendah terdeteksi.

Tabel 2.2

Tabel Mode Operasi Timer 2 [7]

RCLK+TCLK	CP/RL2	TR2	MODE
0	0	1	16 bit auto reload
0	1	1	16 bit capture
1	X	1	Baud rate generator
X	X	0	Off

2.2. Konsep Transmisi Data

Transmisi data didefinisikan sebagai pengiriman/pertukaran data (digital) antara dua peralatan atau lebih dengan menggunakan sistem transmisi elektronik. Sebagai contohnya adalah komputer dengan peralatan lainnya (peripheral).

Istilah data berarti informasi digital dengan sederetan bilangan biner, atau bit (*binary digit*). Setiap bit hanya bernilai nol dan satu, dan sekumpulan bit disebut juga sebagai kata biner. *Byte* adalah sebutan untuk kata biner yang terdiri dari 8 bit. Bit paling kanan dari suatu kata biner disebut dengan *Least Significant Bit* (LSB), sedangkan bit paling kiri disebut dengan *Most Significant Bit* (MSB).

Terdapat dua cara transmisi data, yaitu transmisi data parallel dan transmisi data serial.

a. Transmisi Data Parallel

Pada transmisi data parallel, data ditransfer sekaligus dalam satu waktu menggunakan saluran transmisi sebanyak bit data yang dikirimkan.

b. Transmisi Data Serial

Pada transmisi data serial, data ditransfer satu bit pada satu waktu melalui satu jalur transmisi tunggal.

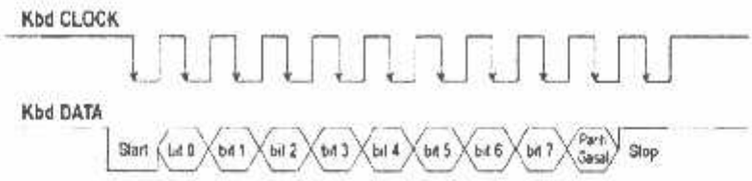
2.2.1. Metode Transfer Data Serial Berdasarkan Pewaktuan

Ada dua cara untuk mentransfer data serial berdasarkan pewaktuan, yaitu transmisi *sinkron* dan transmisi *asinkron*.

a. Transmisi *Sinkron*

Transmisi data *sinkron* biasanya digunakan pada pengiriman blok data yang besar. Blok data dikirimkan secara kontinyu tanpa adanya pembatas/interval waktu, dengan kecepatan yang konstan dan tidak memiliki *start bit* dan *stop bit*.

Pewaktuan diberikan dengan dua cara, yaitu menggunakan *sync character* dan *sinyal clock*. *Sync character* dikirimkan pada awal blok data. *Sync character* terdiri dari bit-bit khusus yang akan digunakan sisi penerima untuk menyesuaikan dengan sisi pengirim. Sedangkan sinyal *clock* digunakan untuk mengirimkan informasi pewaktuan data yang sedang dikirimkan.



Gambar 2.3
Data Serial *Sinkron* [11]

Sisi pengirim dapat mengirim informasi ini pada jalur yang terpisah dari data, atau menggabungkannya dengan data yang dikirimkannya.

b. Transmisi *Asinkron*

Pada transmisi data *asinkron* tiap karakter data terdiri atas 5, 6, 7, atau 8 data dengan penambahan bit yang disisipkan pada kedua ujung karakter data yaitu *start bit* dan *stop bit*. Gambar 2.4 menunjukan format bit yang digunakan untuk mengirimkan data serial *asinkron*.

Gambar 2.4
Data Serial *Asinkron* [11]

Start bit digunakan untuk memberitahukan penerima agar siap menerima data. Penerima akan mengetahui *start bit* bila ada perubahan logika 1 ke 0 pada pengiriman satu karakter data. Setelah bit itu karakter akan mengikuti *start bit*. Setelah bit terakhir dari karakter dikirim, *stop bit* akan diketahui ketika saluran berlogika 1 sekurang-kurangnya satu atau dua siklus waktu. Oleh karena itu transmisi asinkron dikenal juga dengan nama *start stop transmission*.

2.2.2. Tipe Transmisi Data Serial Berdasarkan Jalur Komunikasi

Berdasarkan jalur komunikasinya, transmisi data serial terbagi menjadi 3 tipe, yaitu:

a. Komunikasi *Simpleks*

Komunikasi *simplex* adalah komunikasi satu arah. Pengirim dan penerima tugasnya hanya satu saja, mengirim atau menerima saja. Sebagai contohnya adalah siaran radio komersial.

Gambar 2.5
Sistem Komunikasi *Simplex* [11]

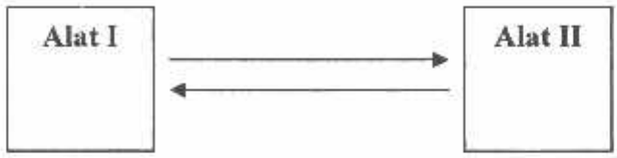
b. Komunikasi *Half Duplex*

Transfer data pada komunikasi ini dilakukan dua arah, tetapi data yang dikirimkan hanya satu arah pada satu waktu. Sebagai contohnya adalah pada penggunaan radio komunikasi *Handy Talky* (HT).

Gambar 2.6
Sistem Komunikasi *Half Duplex*[11]

c. Komunikasi *Full Duplex*

Merupakan komunikasi dua arah, masing-masing peralatan dapat mengirim dan menerima data dalam satu waktu yang bersamaan. Sebagai contoh penggunaan dalam metode ini adalah pada pesawat telepon.



Gambar 2.7
Sistem Komunikasi *Full Duplex* [11]

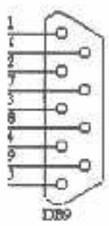
2.3. Interface RS 232

Interface merupakan suatu piranti yang dapat menghubungkan satu peralatan ke peralatan yang lain sehingga peralatan tersebut dapat saling berkomunikasi. Sedangkan cara/proses untuk menghubungkan dua sistem yang berbeda agar dapat bekerjasama disebut *interfacing*.

2.3.1. Konfigurasi Pin

Jika suatu komputer dihubungkan dengan komputer lain atau suatu peripheral lain, maka bisa dilakukan komunikasi data. Sebuah komputer dapat bertukar informasi melalui *interface port I/O* serial yang disebut *interface* RS-232. RS-232 merupakan *interface* antara peralatan terminal data dan peralatan komunikasi data dengan menggunakan data biner serial sebagai data yang

ditransmisikan. Salah satu konektor yang biasa digunakan untuk komunikasi serial ini adalah konektor DB-9.



Gambar 2.8
Konektor DB-9 [2]

Pada dasarnya semua pin memiliki fungsi, tetapi untuk keperluan RS-232 ini hanya beberapa saja yang penting.

Fungsi yang ada untuk konektor DB-9 adalah sebagaimana tampak dalam tabel 2.3 berikut:

Tabel 2.3
Konfigurasi Pin DB-9 [2]

Fungsi Pin RS-232	**PIN**
Data Carrier Detect (DCD)	1
Received Data (Rxd)	2
Transmited Data (Txd)	3
Data Terminal Ready (DTR)	4
Signal Ground (GND)	5
Data Set Ready (DSR)	6
Request To Send (RTS)	7
Clear To Send (CTS)	8
Ring Indicator (RI)	9

Fungsi tiap-tiap pin pada RS 232:

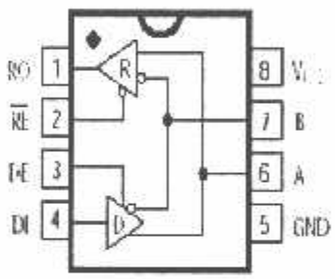
- DCD adalah *protective ground* yang merupakan ground dan digunakan sebagai pelindung dari *electrical shock* yang berlawanan.
- RxD adalah jalur masukkan data ke komputer.
- TxD adalah jalur keluaran data dari komputer
- RTS, merupakan sebuah jalur keluaran dimana sebuah sinyal akan dikirimkan pada alat yang dihubungkan dengan maksud meminta kiriman sinyal bahwa alat tersebut siap menerima data.
- CTS, merupakan jalur masukan sinyal dari alat yang dihubungkan, bahwa alat telah siap menerima data.
- DTR, merupakan sebuah jalur keluaran yang memberi tanda bahwa alat yang terhubung siap mengirimkan data.
- DSR, merupakan jalur masukan dari sinyal yang dikirimkan oleh alat yang terhubung bahwa alat tersebut siap menerima data.
- GND merupakan sinyal referensi untuk sEmua data, kontrol, dan pewaktuan.

2.4. Interface RS-485/RS-422 Tranceiver

Standart RS-485 ditetapkan oleh *Electronic Industry Association dan Telecomunication Industry Association* pada tahun 1983. Penggerak komunikasi RS-485/RS-422 adalah pembantu komunikasi serial seperti halnya RS-232 yang sudah umum dipakai dalam transfer data serial sekarang ini. Tetapi dibandingkan

dengan RS-232, RS485/RS-422 memiliki beberapa keunggulan, diantaranya : memiliki kecepatan maksimum yang lebih tinggi, memiliki jarak jangkauan yang lebih panjang (4000 feet), lebih tahan terhadap gangguan yang berasal dari luar seperti: tegangan listrik dan medan magnet.

RS-485/RS-422 menangani transmisi data dengan satu saluran bersama dan bekerja dengan metode *half duplex*. Dalam setiap IC terdapat satu unit pengirim (D = *driver*) dan satu unit penerima (R = *receiver*).



Gambar 2.9
RS-485/RS-422 [9]

pin 1 (RO) merupakan pin keluaran data, pin 2 (RE) berfungsi untuk mangaktifkan unit penerima data, pin 3 (DE) berfungsi untuk mengaktifkan unit pengirim data, (DI) merupakan pin masukan data, dan pin 6 dan pin 7 merupakan jalur yang akan dihubungkan ke kabel saluran.

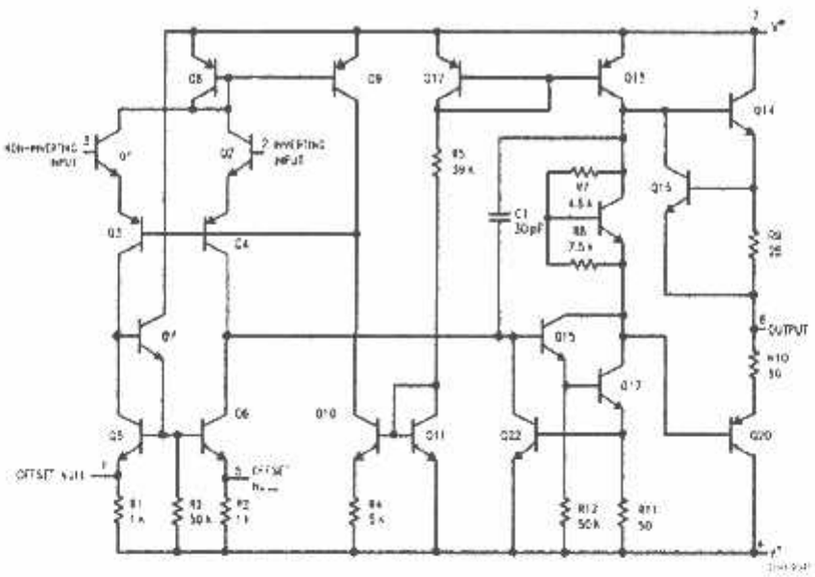
2.5. Operasional Amplifier (Op-Amp)

2.5.1. Sekilas Tentang Op-Amp

Operasional amplifier (Op-Amp) adalah penguat *gain* tinggi yang dirancang untuk melaksanakan tugas-tugas matematis seperti penjumlahan,

pengurangan, perkalian, dan pembagian. Pada saat ini op-amp rangkaian terpadu linier dapat bekerja dengan tegangan yang rendah dan dengan hasil yang tidak kalah baiknya dengan pendahulunya. Dengan harga yang relatif murah dan mudah diganti-ganti serta sifatnya yang dapat di andalkan, maka tidak heran kalau setiap tahunya berjuta-juta op-amp di gunakan. Dari kelebihan yang dimiliki op-amp telah memperluas penggunaan op-amp sampai jauh melampui kegunaannya saat pertama dirancang. Beberapa penggunaan op-amp adalah di bidang pengendalian proses, komunikasi, komputer, sumberdaya dan isyarat, sistem peraga dan sistem pengukuran atau sistem pengujian.

Pada op-amp mempunyai lima terminal dasar yang terbagi dalam dua untuk catu daya, dua untuk isyarat masukan, dan satu untuk keluarannya. Bagian dalam dari op-amp itu sendiri rumit, gambar skematik dari op-amp dapat di lihat dalam gambar 2.10. untuk dapat menggunakan op-amp tidak perlu mengetahui hal apapun tentang cara kerja bagian dalam dari op-amp, karena op-amp telah dirancang sedemikian rupa sehingga komponen luarlah yang akan menentukan kegunaan dari dari op-amp.

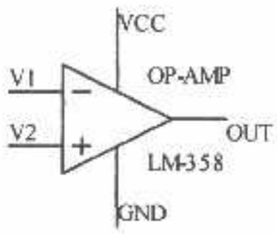


Gambar 2.10
Skematik Op-Amp [11]

2.5.2. Op-Amp Sebagai Pembanding Tegangan (Komparator)

Pembanding tegangan akan membandingkan tegangan masukan satu dengan tegangan masukan yang lain. Gambar 2.11 menunjukan rangkaian pembanding tegangan sederhana. Dalam konfigurasi yang paling sederhana modus lup terbuka , adanya sedikit perbedaan tegangan diantara kedua masukkan akan mengayunkan op-amp ke keadaan saturasi. Arah keluaran saturasi ditentukan oleh polaritas sinyal masukkan.

Bila tegangan masukkan membalik lebih positif dibandingkan tegangan masukkan tak membalik, maka keluaran akan berayun menuju ke saturasi negatif ($-V_{sat}$). Sebaliknya, bila tegangan masukkan membalik lebih negatif dibandingkan tegangan masukkan tak membalik, maka keluaran akan berayun menuju ke saturasi positif ($+V_{sat}$).



Gambar 2.11

Rangkaian Pembanding Tegangan [3]

2.6. LED Infra Merah & Photodioda

Dalam aplikasi, led infra merah digunakan bersama dengan photodioda dimana led sebagai pemancar (Tx) dan photodioda sebagai penerima (Rx) atau sensornya. Rangkaian sensor ini biasanya dioperasikan dalam uji kondisi dua keadaan, yaitu ada atau tidak adanya cahaya infra merah. Pada prinsipnya photodioda adalah mengkombinasikan kemampuan untuk mendeteksi jumlah cahaya yang masuk padanya dan menghasilkan penguatan berupa tegangan.

Adapun konstruksi dari sebuah photodioda hampir sama dengan transistor BJT biasa, kecuali bagian atasnya terdapat sebuah jendela/lensa, seperti terlihat pada gambar 2.12 dibawah ini:

Gambar 2.12

Simbol LED Infra Merah Dan Photo Dioda [6]

Timbulnya *photon* menggerakkan sepasang *hole electron* dalam pertemuan kolektor-basis. Tegangan *reverse* bias antara kolektor-basis akan menarik *hole* yang diinduksikan ke basis dan kolektor area. *Forward* bias dari basis emitor akan menyebabkan *hole-hole* mengalir dari basis ke emitor seperti juga elektron mengalir dari emitor ke basis

Pada titik ini transistor biasa akan mengambil alih yaitu dengan emitor *infected electron* bagian basis yang sempit dan ditarik kearah kolektor yang lebih positif. Aliran elektron menuju sumber cahaya yang diinduksikan oleh sepasang *hole electron* menyokong arus basis dan apabila transistor dihubungkan dalam konfigurasi *common emitor*, arus cahaya yang diinduksikan dikalikan dengan Hfe dari transistor dan akan muncul arus kolektor.

Makin tinggi intensitas cahaya yang mengenai photodioda maka tahanan photodioda akan makin rendah, sehingga menyebabkan tegangan output menjadi kecil. Sedangkan bila sinar dari led infra merah sebagai sumber cahaya tidak mengenai photodioda, maka keluaran akan sama dengan tegangan input (VCC).

2.7. LDR *(Light Dependent Resistor)*

Gambar 2.13
Bentuk LDR [6]

LDR adalah salah satu jenis komponen *tranducer* yang dapat mendeteksi intensitas cahaya. Komponen ini merupakan sebuah tahanan yang nilainya bergantung pada banyaknya cahaya yang diterima. LDR mempunyai nilai tahanan yang berbanding terbalik dengan jumlah cahaya yang diterimanya. Semakin banyak cahaya yang diterima, maka semakin kecil nilai tahanannya, begitu pula sebaliknya semakin kecil cahaya yang diterima, maka akan semakin besar nilai tahanannya.

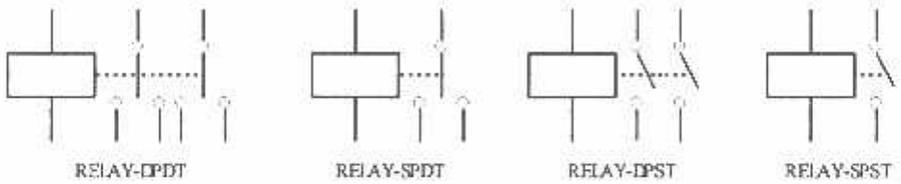
2.8. Relay

Relay adalah komponen elektrik yang umumnya digunakan untuk menghidupkan rangkaian kontrol dan peralatan elektrik lainnya yang menarik arus relatif kecil. Namun dapat mengontrol tegangan dan arus yang lebih besar dengan menggunakan efek penguatan *(amplifiying effect)*. *Amplifiying effect* didapat dengan cara memanfaatkan tegangan kecil (5-24 volt) untuk mengoperasikan koil dari relay. Kemudian koil tersebut digunakan untuk mensaklar (*switching*) tegangan yang lebih besar. Aliran arus yang digunakan untuk mengatur koil *relay* terpisah dari arus listrik yang dikontrol oleh kontak-kontak pada relay tersebut.

Berbagai jenis *relay* dipergunakan untuk berbagai jenis kebutuhan sehari-hari. Misalnya untuk keperluan mengatur peralatan rumah tangga, kelistrikan kendaraan bermotor, kerja mesin-mesin pada industri dan masih banyak yang lainnya. Ada empat jenis *relay* yang biasa digunakan, yaitu:

- DPDT (*Double Pole, Double Throw*)
- SPDT (*Single Pole, Double Throw*)
- DPST (*Double pole, Single Throw*)
- SPST (*Single Pole, Single Throw*)

Simbol relay ditunjukkan pada gambar 2.14



Gambar 2.14
Simbol Jenis-jenis *Relay* [12]

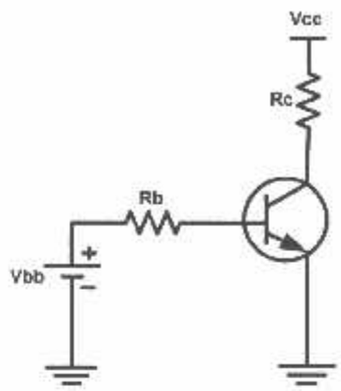
Pada dasarnya *relay* dapat dikatakan sebagai kuda beban elektrik (*electrical workhorses*) yang mengontrol suatu rangkaian elektrik dengan cara membuka dan menutup kontak pada rangkaian lain (rangkaian internal). Apabila kontak relay *normally open* (NO), maka kontak tersebut akan terbuka bila *relay* tidak dialiri arus listrik. Sebaliknya pada titik kontak *relay* yang tergolong *normally close* (NC) akan tertutup bila *relay* tidak daialiri arus listrik.

2.9. Solenoid

Solenoid adalah alat yang digunakan untuk mengubah sinyal/arus listrik menjadi gerakan mekanis linier. Solenoid terdiri dari kumparan /lilitan dengan inti besi yang dapat bergerak. Prinsip kerja solenoid adalah jika solenoid tidak diberi tegangan maka tidak akan timbul medan magnet pada kumparan, sehingga inti besi tidak akan bergerak. Sedangkan bila solenoid dialiri tegangan maka akan timbul medan magnet pada kumparan, sehingga inti besi akan bergerak masuk kedalam rumah solenoid.

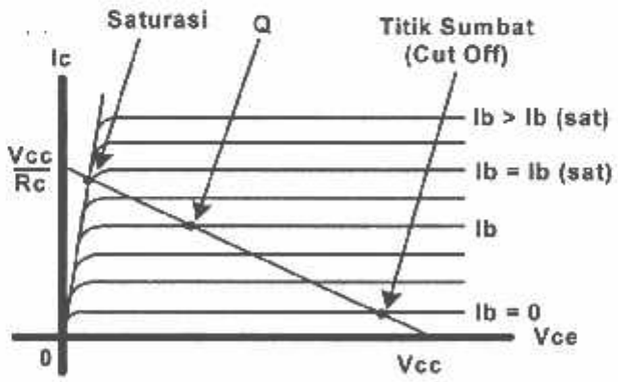
2.10. Transistor Sebagai Saklar

Transistor merupakan sebuah komponen semikonduktor yang banyak digunakan pada berbagai rangkaian elektronik baik sebagai penguat, saklar, dan lain-lain. Asas kerja dari transistor adalah akan ada arus yang mengalir diantara terminal kolektor – emitor (I_C) hanya apabila ada arus yang mengalir diantara terminal basis – emitor (I_B). Jadi transistor harus dioperasikan pada daerah linier agar diperoleh sinyal keluaran yang tidak cacat *(distorsi)*. Untuk dapat mengoperasikan secara tepat maka pengertian tentang titik kerja transistor sangatlah penting dan harus pahami dan dimengerti dengan benar.



Gambar 2.15
Rangkaian *Switching* Transistor [6]

Garis beban akan memotong sekelompok kurva arus basis constant I_B dengan I_B tertentu (yang diatur rangkaian bias), garis beban akan memotong kurva I_B tersebut dititik Q yang disebut titik kerja transistor. Titik kerja ini menjadi kondisi awal dari pengoperasian transistor kelak dimana transistor tersebut mempunyai tiga daerah kerja yaitu aktif (*active*), jenuh (*saturation*), dan tersumbat (*cut-off*).



Gambar 2.16
Karakteristik I_C-V_{CE} Transistor Bipolar [6]

Pada gambar diatas dapat dilihat, titik dimana garis beban memotong kurva I_B= 0 disebut sebagai titik sumbat (*cut-off*). Pada titik ini arus kolektor(I_C) sangat kecil (hanya arus bocor) sehingga dapat diabaikan, disini transistor kehilangan kerja normalnya. Disini dapat dikatakan bahwa tegangan kolektor-emitor sama dengan ujung dari garis beban tersebut.

$$V_{CE(cut\text{-}off)} \cong V_{CC}$$

Perpotongan garis beban dengan kurva $I_B = I_{B(sat)}$ disebut titik jenuh (*saturation*). Pada titik ini arus kolektor maksimum atau dapat dikatakan bahwa arus kolektor sama dengan ujung dari garis beban.

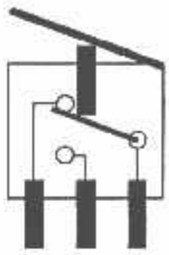
$$I_{C(sat)} \cong \frac{V_{CC}}{R_C}$$

Jika arus basis I_B lebih kecil dari $I_{B(sat)}$ maka transistor akan beroperasi pada daerah aktif, yaitu titik kerjanya terletak disepanjang garis beban.

Jadi disimpulkan bahwa transistor bipolar bekerja sebagi suatu sumber arus (penguat) dimana saja sepanjang garis beban, kecuali titik jenuh (*saturation*) atau titik sumbat (*cut-off*) dimana transistor tidak lagi bekerja sebagai sumber arus (penguat) melainkan sebagi saklar (*switching*)

2.11. Limit Switch

Limit switch merupakan peralatan pemutus dan penghubung sumber tegangan listrik untuk rangkaian kontak yang berfungsi sebagai saklar tekan yang bekerja karena adanya sentuhan, tekanan, atau gesekan. *Limit switch* mempunyai kontak *Normally Open* (NO) dan *Normally Close* (NC)



Gambar 2.17

Bentuk *Limit Switch* [6]

Biasanya *limit switch* ini digunakan atau ditempatkan sesuai dengan kebutuhan atau keadaan benda yang bersangkutan, dan harus memperhitungkan benda agar dapat menyentuh dari tuas *limit switch.*

Limit switch terdiri dari pengungkit dan roda penjulang yang memiliki bagian mekanik yang akan tersentuh oleh benda. Kemudian bagian ini menggerakkan pengungkit dan diteruskan pada suatu kontak. Karena adnya gerakan ini, maka kontak pada limit *switch* akan bekerja.

BAB III

PERANCANGAN DAN PEMBUATAN ALAT

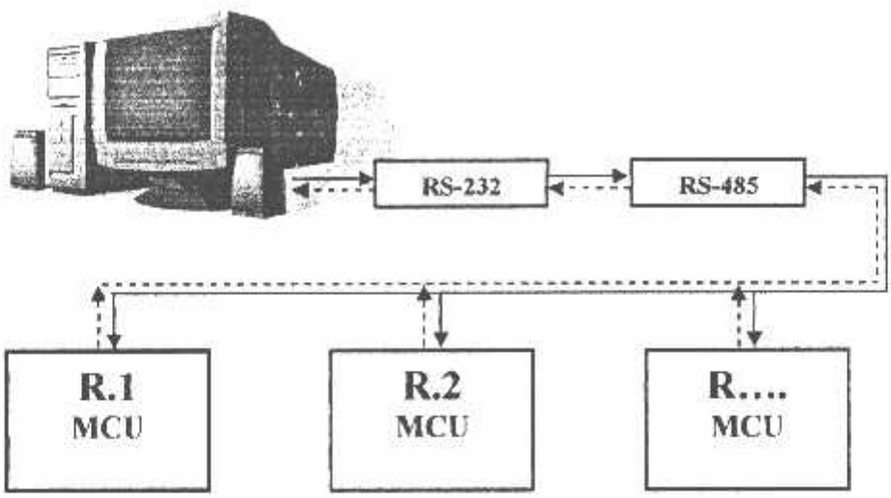
Pada bab ini akan dijelaskan mengenai perancangan dan pembuatan alat, khususnya dalam hal memilih komponen-komponen elektronika yang akan digunakan, membuat rangkaian dan merencanakan sebuah program dengan menggunakan bahasa yang sesuai.

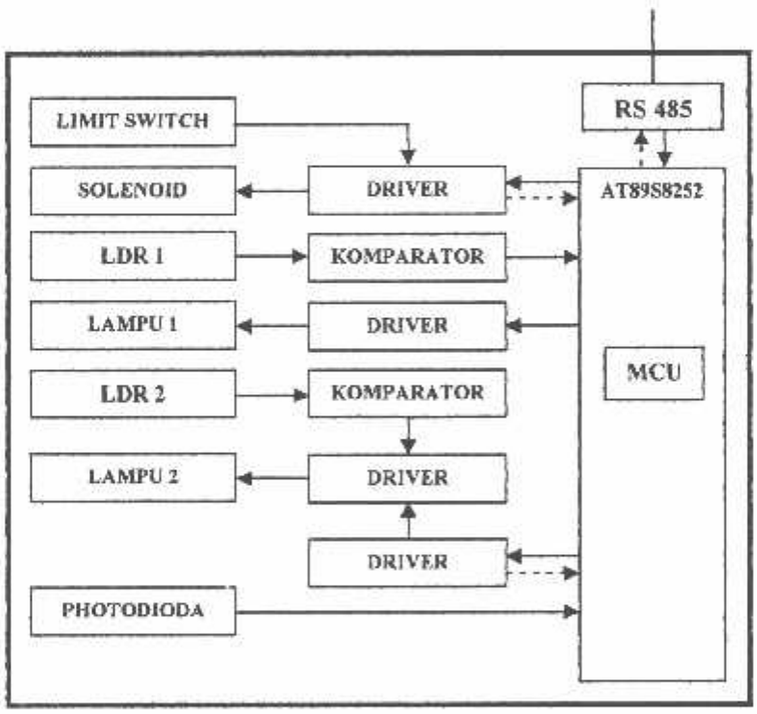
Secara garis besar perancangan dan pembuatan alat ini dapat dikelompokkan manjadi dua bagian:

1. Perancangan dan pembuatan perangkat keras *(hardware)*
2. Perancangan dan pembuatan perangkat lunak *(software)*

Perancangan dan pembuatan perangkat keras meliputi pembuatan diagram blok sistem secara keseluruhan, yang terdiri dari rangkaian input, rangkaian kontrol, dan rangkaian *output*. Sedangkan untuk perancangan dan pembuatan perangkat lunak meliputi pembuatan diagram alir perangkat lunak dan pembuatan yang akan disertakan pada lembar lampiran. Perangkat lunak ini adalah berupa program atau perintah yang digunakan untuk menjalankan IC mikrokontroller yang akan difungsikan sebagai unit kontrol sistem dari perangkat keras secara keseluruhan, sehingga sistem dapat berjalan seperti yang diharapkan.

Diagram blok sistem akan ditunjukkan pada gambar 3.1 berikut ini:





Gambar 3.1

Diagram Blok Sistem

Fungsi dari masing-masing blok dapat dijelaskan sebagai berikut:

1. Personal Computer (PC)

   Pada perancangan ini komputer berfungsi sebagai pusat kendali dan pusat monitor (*display*) dari sistem.

2. MCU *(Microcontroller Unit)*

   Pada perancangan ini MCU *(Microcontroller Unit)* berfungsi sebagai pusat pengolah data dari komputer yang kemudian digunakan untuk menjalankan perangkat-perangkat pendukung yang lain.

3. RS 232

   Pada perancangan ini RS-232 berfungsi sebagai media komunikasi antarmuka antara komputer dan perangkat MCU (*Microcontroller Unit*).

4. RS-485

   Pada perancangan ini RS-485 berfungsi sebagai pendukung RS-232, yang memiliki kelebihan dapat mengirimkan data serial dengan jarak jangkau yang jauh dan lebih tahan terhadap gangguan dari luar.

5. Solenoid

   Pada perancangan ini solenoid berfungsi sebagai alat pengunci pintu ruangan.

6. Limit Switch

   Pada perancangan ini *limit switch* berfungsi sebagai sensor yang mendeteksi posisi pintu ruangan apakah dalam keadaan terbuka atau tertutup.

7. LDR *(Lighting Dependent Resistant)*

   Pada perancangan ini LDR *(Lighting Dependent Resistant)* berfungsi sebagai sensor cahaya pada rangkaian pemberi status kaedaan lampu dan pada rangkaian lampu otomatis.

8. LED Infra Merah dan Photodioda

   Pada perancangan, rangkaian ini berfungsi sebagai sensor alarm pada sistem keamanan didalam ruangan.

9. Rangkaian Driver

   Karena arus dari mikrokontroller relatif kecil, maka diperlukan sebuah rangkaian *driver* untuk menggerakkan *relay* yang berfungsi sebagai saklar.

10. Rangkaian Komparator

    Pada perancangan, rangkaian ini berfungsi sebagai pengubah sinyal analog menjadi sinyal logika sebagai masukkan ke mikrokontroller dengan cara membandingkan antara tegangan *input* dari LDR dengan tegangan referensi.

11. Rangkaian Lampu 1 dan Lampu 2

    Pada perancangan ini rangkaian lampu 1 berfungsi untuk mengendalikan lampu dalam ruangan, sedangkan rangkaian lampu 2 berfungsi sebagai rangkaian lampu otomatis.

Prinsip kerja dari sistem:

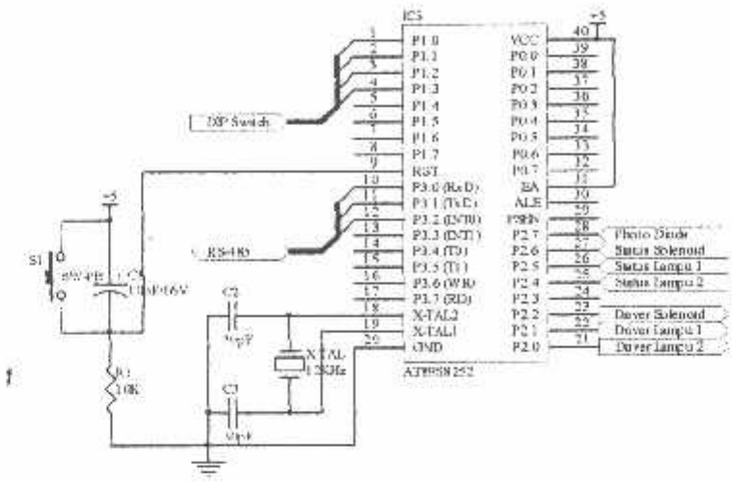
Pada dasarnya sistem ini adalah sistem pengendali perangkat-perangkat yang berada didalam sebuah bangunan atau kompleks perkantoran yang dapat dikontrol dan dipantau melalui sebuah *Personal Computer* (PC). Komputer akan mengirimkan perintah-perintah yang berupa data dengan cara meng-klik *icon* yang terdapat pada layar komputer, kemudian data akan dikirimkan ke MCU *(Microcontroller Unit)* yang terdapat disetiap ruangan kantor. Data akan diolah oleh MCU yang kemudian digunakan untuk menggerakkan perangkat-perangkat

yang berada didalam ruangan. Disetiap perangkat terdapat rangkaian sensor yang berfungsi sebagai pemberi informasi status dari kerja perangkat. Informasi status tersebut digunakan sebagai masukkan bagi mikrokontroller yang kemudian dikirimkan kembali ke komputer, dan ditampilkan melalui layar monitor.

3.1. Perancangan Dan Pembuatan Perangkat Keras *(Hardware)*

3.1.1. Perancangan Minimum Sistem Mikrokontroller AT89S8252

Rangkaian minimum sistem mikrokontroller AT89S8252 merupakan rangkaian utama pada perancangan alat ini. Rangkaian ini merupakan pengolah dari data-data biner yang akan dikirimkan oleh komputer yang kemudian digunakan untuk menjalankan perangkat-perangkat yang pendukung yang lain. Agar dapat melakukan prosesnya, maka mikrokontroller harus didukung oleh beberapa komponen tambahan, yaitu rangkaian rangkaian *clock* dan rangkaian reset. Selain itu juga harus ditentukan penggunaan port-portnya dan penggunaan sinyal-sinyal yang digunakan untuk mendukung proses yang dilakukan.



Gambar 3.2

Rangkaian Minimum Sistem Mikrokontroller AT89S8252

Pin X1 dan X2 dihubungkan dengan kristal 12 MHz yang didukung dengan dua kapasitor C1 dan C2 yang nilainya 30 pF. Apabila terjadi beda potensial pada kedua kapasitor tersebut kristal akan berisolasi dan menghasilkan pulsa yang berfungsi sebagai *clock* dari mikrokontroller tersebut.

Pin reset dihubungkan dengan saklar yang digunakan untuk mereset sistem mikrokontroller. Karena pin reset ini aktif pada logika tinggi, maka diperlukan sebuah tahanan sebesar 10 KΩ yang dihubungkan dengan ground untuk memastikan pin reset berlogika rendah pada saat sistem tidak bekerja. Kapasitor C1 dengan nilai 10 µF/16V berfungsi untuk meredam adanya pelentingan tegangan akibat dari penekanan saklar reset.

Pin (P1.0 – P1.3) dihubungkan dengan rangkaian DIP *switch* 4 bit yang berfungsi untuk menentukan *register* atau alamat MCU *(Microcontroller Unit)* yang akan diaktifkan.

Pin (P3.0 – P3.2) dihubungkan dengan rangkaian RS-485 yang merupakan media *interface* dari sistem ini.

Pin (P2.7) dihubungkan dengan photodiode yang berfungsi sebagai penerima dari LED infra merah yang merupakan sistem sensor keamanan ruangan.

Pin (P2.6) dihubungkan dengan sebuah *relay* DPDT yang digunakan untuk mengaktifkan solenoid, sehingga mikrokontroller dapat mengenali kondisi dari solenoid.

Pin (P2.5) dihubungkan dengan rangkaian sensor lampu, sehingga mikrokontroller dapat mengenali kondisi dari lampu.

Pin (P2.4) dihubungkan dengan sebuah *relay* DPDT yang digunakan untuk mengaktifkan sistem lampu otomatis, sehingga mikrokontroller dapat mengenali kondisi sistem tersebut.

Pin (P2.2) dihubungkan dengan sebuah *relay* yang digunakan untuk mengaktifkan solenoid.

Pin (P2.1) dihubungkan dengan sebuah *relay* yang merupakan saklar untuk menghidupkan lampu dalam ruangan.

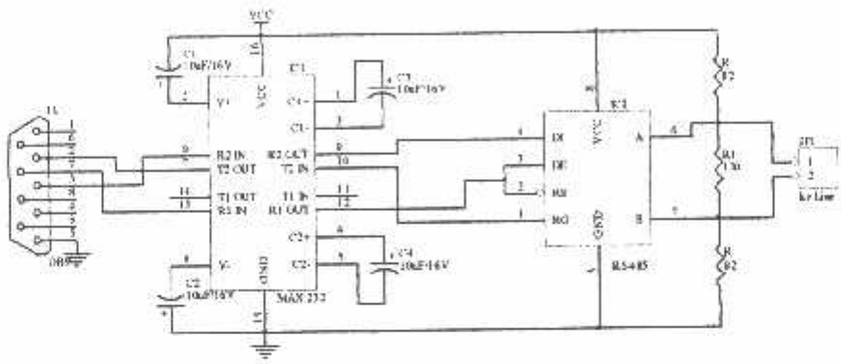
Pin (P2.0) dihubungkan dengan sebuah *relay* yang merupakan saklar untuk mengaktifkan sistem lampu otomatis.

3.1.2. Perancangan RS-485

Untuk dapat berkomunikasi dengan jarak jauh antara mikrokontroller dan komputer, maka dibutuhkan sistem komunikasi data yang dikenal dengan RS-485.

3.1.3. Perancangan RS-232 to RS-485

Pada perancangan sistem ini, selain menggunakan sistem komunikasi RS-485, kita harus tetap menggunakan RS-232. Hal ini dikarenakan adanya perbedaan antara level tegangan dari komputer (level RS-232) dan level tegangan pada IC mikrokontroller (level TTL).

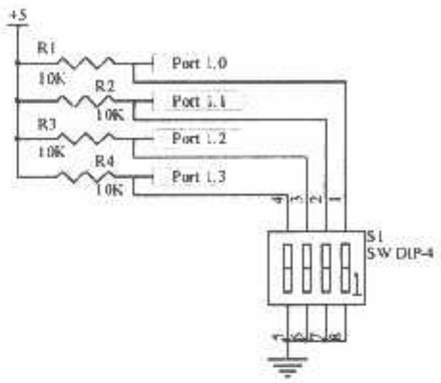


Gambar 3.4
Rangkaian RS-232 to RS485

Rangkaian ini berfungsi sebagai pengubah level tegangan RS-232 dari port serial komputer menjadi level tegangan TTL yang terdapat pada tegangan kerja IC mikrokontroller ataupun sebaliknya.

3.1.4. Perancangan Rangkaian DIP Switch

Pada perancangan ini, rangkaian DIP *switch* digunakan untuk menentukan *register* dari MCU (*Microcontroller Unit*) yang akan diaktifkan dan dikontrol oleh komputer. Rangkaian ini terdiri dari sebuah DIP *switch* 4 bit dan 4 buah tahanan.



Gambar 3.5

Rangkaian DIP *Switch*

Pada rangkaian ini DIP *switch* diberi resistor yang terhubung dengan V_{CC}, maka dua kondisi terhubung dan terputus pada DIP *switch* akan diubah menjadi sinyal *logic* yang akan menjadi masukan bagi mikrokontroller. Dalam rangkaian ini mikrokontroller mendapat tegangan 5V dengan arus sebesar 500 uA, dengan perhitungan maka akan didapat nilai tahanan sebagai berikut:

$$R = \frac{V}{I}$$

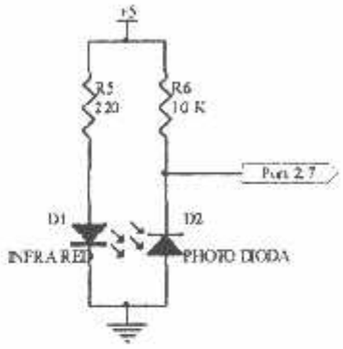
$$= \frac{5}{500.10^{-6}}$$

$$= 10\ K\Omega$$

3.1.5. Perancangan Rangkaian Infra Merah Dan Photodioda

Rangkaian infra merah dan photodioda pada perancangan ini berfungsi sebagai unit keamanan bila ada seseorang yang masuk ruangan tanpa seijin petugas keamanan sedangkan ruangan pada posisi terkunci dan sistem alarm telah

diaktifkan. Rangkaian ini menggunakan komponen LED infra merah dan photodioda yang dihubungkan secara seri dengan resistor.



Gambar 3.6

Rangkaian Infra Merah Dan Photo Dioda

Untuk mendapatkan nilai resistor (R_1) agar infra merah dapat aktif maka dilakukan perhitungan sebagai berikut:

Diketahui: $I_{IR} = 20$ mA

$V_{IR} = 1{,}2$ V

Maka:

$$R_1 = \frac{V_{CC} - V_{IR}}{I_{IR}}$$

$$= \frac{5 - 1{,}2}{20.10^{-3}}$$

$$= 190\ \Omega$$

Sedangkan untuk menentukan nilai resistor dari photodioda (R_2), dapat dilakukan perhitungan sebagai berikut:

Diketahui: I_{PD} = 0,5 mA

Maka:

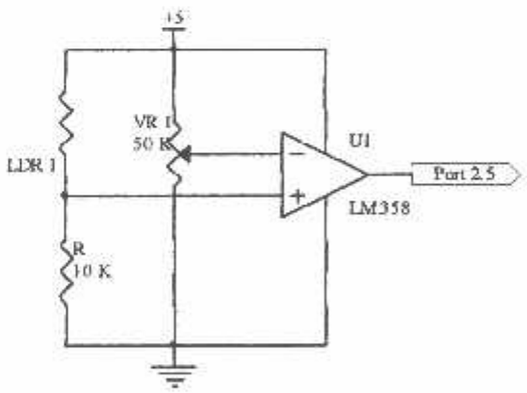
$$R_2 = \frac{V_{CC}}{I_{PD}}$$

$$= \frac{5}{0.5.10^{-3}}$$

$$= 10\ K\Omega$$

3.1.6. Perancangan Rangkaian Sensor Lampu 1

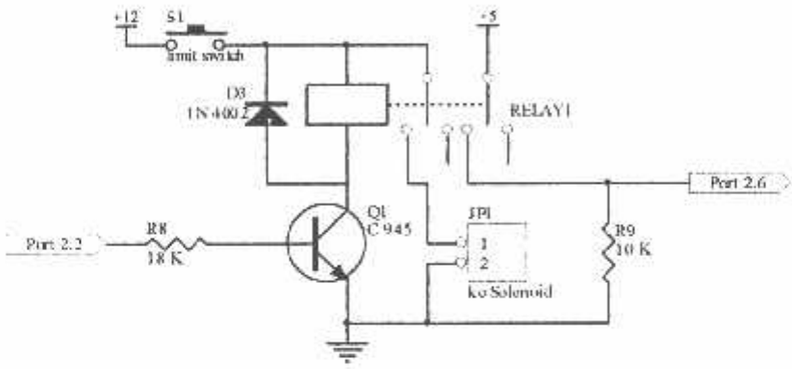
Pada perancangan ini, rangkaian berfungsi sebagai pemberi status dari lampu didalam ruangan sebagai masukkan untuk mikrokontroller apakah lampu dalam keadaan hidup atau mati. Rangkaian ini terdiri dari sebuah LDR yang berfungsi sebagai sensor, sebuah op-amp tipe LM 358 yang berfungsi sebagai komparator, sebuah resistor dengan nilai 10 K sebagai pembagi tegangan, dan sebuah resistor variable yang berfungsi sebagai setting dari rangkaian ini.



Gambar 3.7
Rangkaian Sensor Lampu

3.1.7. Perancangan Driver Relay Solenoid

Solenoid pada perancangan ini berfungsi sebagai pengunci pintu ruangan yang memerlukan tegangan catu sebesar 12V. Untuk mengaktifkannya digunakan sebuah *relay* DPDT yang berfungsi sebagai saklar sekaligus pemberi status dari kerja solenoid.



Gambar 3.8
Rangkaian Driver Selenoid

Relay tersebut digerakkan dengan sebuah driver yang terbentuk dari sebuah transistor sebagai *switch*, sebuah dioda sebagai pengaman transistor dari arus balik, dan sebuah tahanan (R_b). Agar transistor dapat bekerja dengan baik maka dibutuhkan nilai tahanan (R_b) yang sesuai. Dengan perhitungan maka akan didapat nilai tahanan (R_B) sebagai berikut:

Diketahui: $V_{CC} = 12V$

$V_{BE} = 0,65$

$V_{OH} = 2,4\ V$

$H_{FE} = 250$

$R_{relay} = 400\ \Omega$

Maka:

$$I_{relay} = \frac{V_{CC}}{R_{relay}}$$

$$= \frac{12}{400}$$

$$= 30 \text{ mA}$$

$$I_{relay} = I_C$$

$$I_B = \frac{I_C}{H_{FE}}$$

$$= \frac{30mA}{250}$$

$$= 0{,}12 \text{ mA}$$

$$R_B = \frac{V_{OH} - V_{BE}}{I_B}$$

$$= \frac{2{,}4 - 0{,}65}{0{,}12mA}$$

$$= 14{,}583 \text{ K}\Omega$$

Karena tahanan dengan nilai 14,583 KΩ tidak ada dipasaran, maka diganti tahanan dengan nilai 18 KΩ.

Untuk pemberi status ke mikrokontroller, salah satu kontak dari *relay* dihubungkan dengan sebuah tahanan yang tersambung ke *ground*. Sehingga pada saat kontak pertama bekerja untuk mengaktifkan rangkaian lampu otomatis, maka kontak yang lain akan ikut bekerja dan menghasilkan kondisi *logic* untuk masukan mikrokontroller. Dalam rangkaian ini mikrokontroller mendapat

tegangan 5V dengan arus sebesar 500 uA, dengan perhitungan maka akan didapat nilai tahanan sebagai berikut:

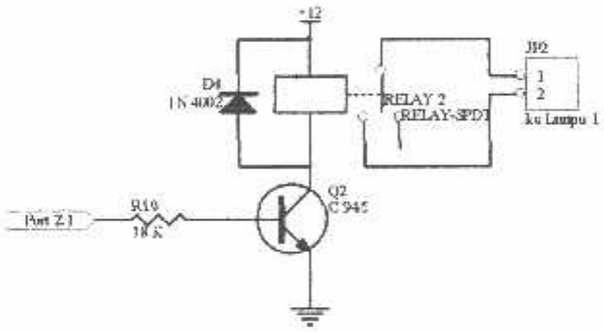
$$R = \frac{V}{I}$$

$$= \frac{5}{500.10^{-6}}$$

$$= 10\ K\Omega$$

3.1.8. Rangkaian Driver Lampu 1 (Lampu Ruangan)

Pada perancangan ini, rangkaian driver lampu 1 berfungsi untuk mengaktif dan menonaktifkan lampu dalam ruangan.



Gambar 3.9
Rangkaian Driver Lampu1

Rangkaian ini terdiri dari sebuah driver dan sebuah *relay* sebagai saklar. Driver dibentuk dari sebuah transistor sebagai *switch*, sebuah dioda sebagai pengaman transistor dari arus balik, dan sebuah tahanan (R_b). Agar transistor dapat bekerja dengan baik maka dibutuhkan nilai tahanan (R_b) yang sesuai. Dengan perhitungan maka akan didapat nilai tahanan (R_B) sebagai berikut:

Diketahui: $V_{CC} = 12V$

$V_{BE} = 0,65$

$V_{OH} = 2,4\ V$

$H_{FE} = 250$

$R_{relay} = 400\ \Omega$

Maka:

$$I_{relay} = \frac{V_{CC}}{R_{relay}}$$

$$= \frac{12}{400}$$

$$= 30\ mA$$

$$I_{relay} = I_C$$

$$I_B = \frac{I_C}{H_{FE}}$$

$$= \frac{30mA}{250}$$

$$= 0,12\ mA$$

$$R_B = \frac{V_{OH} - V_{BE}}{I_B}$$

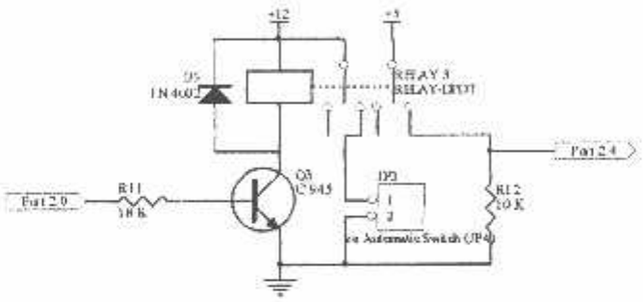
$$= \frac{2,4 - 0,65}{0,12mA}$$

$$= 14,583\ K\Omega$$

Karena tahanan dengan nilai 14,583 KΩ tidak ada dipasaran, maka diganti tahanan dengan nilai 18 KΩ.

3.1.9. Perancangan Driver Lampu 2 (Lampu Otomatis)

Pada perancangan ini, rangkaian driver lampu 2 berfungsi untuk mengaktif dan menonaktifkan rangkaian lampu otomatis. Untuk mengaktifkannya digunakan sebuah *relay* DPDT yang berfungsi sebagai saklar sekaligus pemberi status dari kerja rangkaian lampu otomatis.



Gambar 3.10

Rangkaian Driver Lampu 2

Rangkaian ini terdiri dari sebuah driver dan sebuah *relay*. Driver dibentuk dari sebuah transistor sebagai *switch*, sebuah dioda sebagai pengaman transistor dari arus balik, dan sebuah tahanan (R_b). Agar transistor dapat bekerja dengan baik maka dibutuhkan nilai tahanan (R_b) yang sesuai. Dengan perhitungan maka akan didapat nilai tahanan (R_D) sebagai berikut:

Diketahui: $V_{CC} = 12V$

$V_{BE} = 0{,}65$

$V_{OH} = 2{,}4\ V$

$H_{FE} = 250$

$R_{relay} = 400\ \Omega$

Maka:

$$I_{relay} = \frac{V_{CC}}{R_{relay}}$$

$$= \frac{12}{400}$$

$$= 30 \text{ mA}$$

$$I_{relay} = I_C$$

$$I_B = \frac{I_C}{H_{FE}}$$

$$= \frac{30mA}{250}$$

$$= 0{,}12 \text{ mA}$$

$$R_B = \frac{V_{OH} - V_{BE}}{I_B}$$

$$= \frac{2{,}4 - 0{,}65}{0{,}12mA}$$

$$= 14{,}583 \text{ K}\Omega$$

Karena tahanan dengan nilai 14,583 KΩ tidak ada dipasaran, maka diganti tahanan dengan nilai 18 KΩ.

Untuk pemberi status ke mikrokontroller, salah satu kontak dari *relay* dihubungkan dengan sebuah tahanan yang tersambung ke *ground*. Sehingga pada saat kontak pertama bekerja untuk mengaktifkan rangkaian lampu otomatis, maka kontak yang lain akan ikut bekerja dan menghasilkan kondisi *logic* untuk masukkan mikrokontroller. Dalam rangkaian ini mikrokontroller mendapat

tegangan 5V dengan arus sebesar 500 uA, dengan perhitungan maka akan didapat nilai tahanan sebagai berikut:

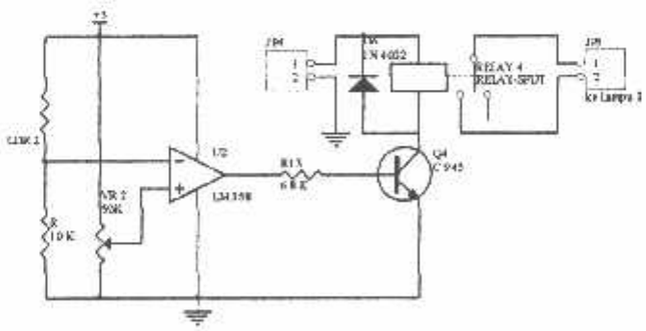
$$R = \frac{V}{I}$$

$$\therefore = \frac{5}{500.10^{-6}}$$

$$= 10\ K\Omega$$

3.1.10. Perancangan Rangkaian Lampu Otomatis

Pada perancangan, rangkaian ini berfungsi sebagai saklar otomatis dari lampu. Rangkaian ini akan mengatur hidup matinya lampu secara otomatis berdasarkan intensitas cahaya dilingkungan sekitarnya tanpa harus selalu dikontrol melalui PC. Rangkaian ini terdiri dari LDR yang berfungsi sebagai sensor, sebuah op-amp tipe LM 358 yang berfungsi sebagai komparator, sebuah resistor dengan nilai 10 K sebagai pembagi tegangan, sebuah resistor variable yang berfungsi sebagai setting dari rangkaian ini, dan sebuah driver yang akan menggerakan *relay* yang berfungsi sebagai saklar lampu.



Gambar 3.11
Rangkaian Lampu Otomatis

Rangkaian driver diatas dibentuk dari sebuah transistor yang berfungsi sebagai *switch*, sebuah dioda sebagai pengaman transistor dari arus balik, dan sebuah tahanan (R_b). Agar transistor dapat bekerja dengan baik maka dibutuhkan nilai tahanan (R_b) yang sesuai. Dengan perhitungan maka akan didapat nilai tahanan (R_B) sebagai berikut:

Diketahui: $V_{CC} = 12V$

$V_{BE} = 0{,}65$

$V_{OH} = 2{,}4\ V$

$H_{FE} = 250$

$R_{relay} = 400\ \Omega$

Maka:

$$I_{relay} = \frac{V_{CC}}{R_{relay}}$$

$$= \frac{12}{400}$$

$$= 30\ mA$$

$$I_{relay} = I_C$$

$$I_B = \frac{I_C}{H_{FE}}$$

$$= \frac{30mA}{250}$$

$$= 0{,}12\ mA$$

$$R_B = \frac{V_{OH} - V_{BE}}{I_B}$$

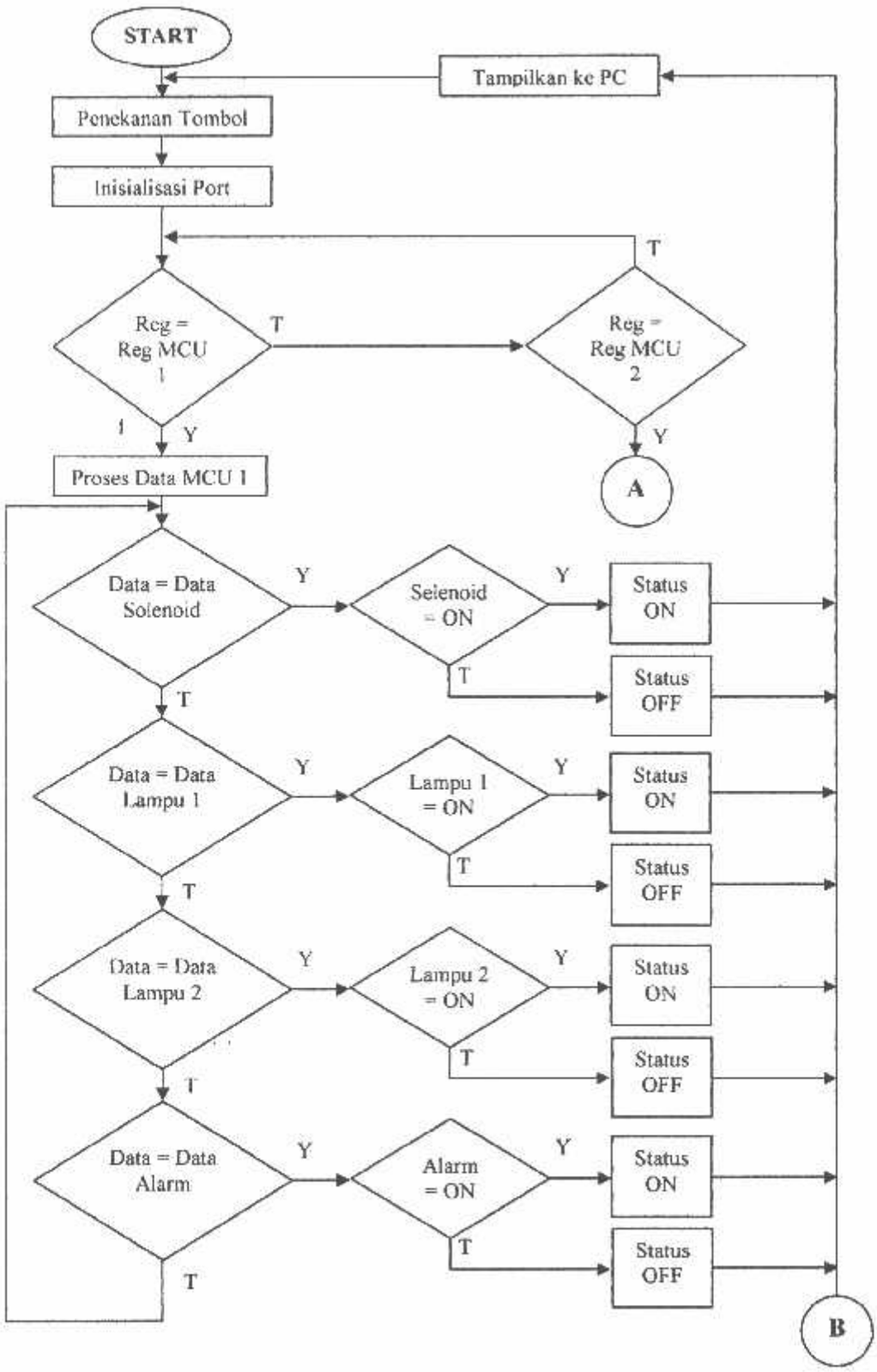
$$= \frac{2,4 - 0,65}{0,12mA}$$

$$= 14,583\ K\Omega$$

Karena tahanan dengan nilai 14,583 KΩ tidak ada dipasaran, maka diganti tahanan dengan nilai 18 KΩ.

3.2. Perancangan Dan Pembuatan Perangkat Lunak (*Software*).

Untuk pemakaian mikrokontroller dalam suatu sistem perlu direncanakan sebuah perangkat lunak yang dapat mengatur sistem tersebut. Perangkat lunak disini merupakan susunan perintah-perintah atau program didalam memori yang akan dilaksanakan oleh sistem tersebut. Perancangan perangkat lunak didasarkan atas perancangan perangkat keras yang telah dibuat sebelumnya. Perangkat lunak dari alat tersebut terdapat pada bagian lampiran dengan perencanaan diagram alir seperti yang terdapat pada gambar 3.12 sebagai berikut:


START
Tampilkan ke PC
Penekanan Tombol
Inisialisasi Port
Reg = Reg MCU 1
T
Reg = Reg MCU 2
T
Y
Y
Proses Data MCU 1
A
Data = Data Solenoid
Y
Selenoid = ON
Y
Status ON
T
Status OFF
T
Data = Data Lampu 1
Y
Lampu 1 = ON
Y
Status ON
T
Status OFF
T
Data = Data Lampu 2
Y
Lampu 2 = ON
Y
Status ON
T
Status OFF
T
Data = Data Alarm
Y
Alarm = ON
Y
Status ON
T
Status OFF
T
B

BAB IV

PENGUJIAN ALAT

Untuk mengetahui keberhasilan dari perencanaan dan pembuatan alat ini maka, diperlukan pengujian terhadap alat tersebut. Dalam rangka pengujian diuraikan sejumlah pengukuran dan penghitungan melalui percobaan yang dilakukan untuk mengetahui sistem kerja dari alat secara keseluruhan.

Pengujian alat dilakukan per-bagian agar mudah dalam menganalisis hasil perancangan dan pengujian. Pengujian alat dilakukan setelah pembuatan alat hasil rancangan selesai.

Secara umum dapat disimpulkan tujuan dari pengujian alat ini yaitu :

1. Mengetahui prinsip kerja dari masing-masing blok rangkaian.
2. Mempermudah pendataan spesifikasi alat.
3. Memudahkan perawatan dan perbaikan jika suatu saat terjadi kerusakan.

Bagian-bagian yang diuji adalah :

1. Pengujian Rangkaian Komunikasi Serial
2. Pengujian Rangkaian Infra Merah dan Phototransistor.
3. Pengujian Rangkaian Driver Relay.
4. Pengujian Rangkaian Sensor Lampu.
5. Pengujian Keseluruhan Sistem.

4.1. Pengujian Rangkaian Komunikasi Serial

Tujuan:

- Untuk mengetahui apakah komunikasi serial antara mikrokontroler dan PC dapat berjalan.

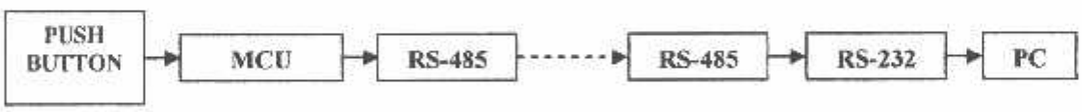
Peralatan Yang Digunakan:

- Power supply 5 volt.
- Mikrokontroler.
- PC.
- 8 LED.
- 8 Push Button.

Langkah-Langkah Pengujian:

1. Pengujian komunikasi serial dari mikrokontroler ke PC.

- Membuat rangkaian seperti pada gambar dibawah ini:



Gambar 4.1
Blok Pengujian Komunikasi Serial Dari Mikrokontroler Ke PC

- Membuat program pada mikrokontroler yang bisa mengambil data pada P2 mikrokontroler dan mengirimkan secara serial ke PC.
- Membuat program pada PC agar dapat membaca data yang dikirimkan melalui port serial oleh mikrokontroler.

2. Pengujian komunikasi serial dari PC ke mikrokontroler.

- Membuat rangkaian seperti pada gambar dibawah ini:

Gambar 4.2
Blok Pengujian Komunikasi Serial Dari PC Ke Mikrokontroler

- Membuat program pada PC agar dapat mengirimkan data melalui port serial ke mikrokontroler.
- Membuat program pada mikrokontroler yang bisa mengambil data dari RXD dan mengirimkam pada P2.

Hasil Pengujian:

- Pengujian Komunikasi Serial Dari Mikrokontroller ke PC

Gambar 4.3
Tampilan Komunikasi Serial dari Mikrokontroler ke PC

Tabel 4.1
Hasil Pengujian Komunikasi Serial Dari Mikrokontroler Ke PC

DATA INPUT PADA P2								TAMPILAN PADA PC
PB1	PB2	PB3	PB4	PB5	PB6	PB7	PB8	
1	1	1	1	0	0	0	0	11110000
0	0	0	0	0	0	0	0	00000000
1	1	1	1	1	1	1	1	11111111
0	0	0	0	1	1	1	1	00001111
1	1	1	0	1	1	1	0	11101110
0	1	1	0	0	1	1	0	01100110
1	0	1	0	1	0	1	0	10101010
1	1	1	0	1	1	1	0	11100111

- Pengujian Komunikasi Serial Dari PC ke Mikrokontroller

Gambar 4.4
Tampilan Komunikasi Serial dari PC ke Mikrokontroler

Tabel 4.2
Hasil Pengujian Komunikasi serial dari PC ke Mikrokontroler

DATA INPUT PC	LED 1	LED 2	LED 3	LED 4	LED 5	LED 6	LED 7	LED 8
10001000	1	0	0	0	1	0	0	0
01010101	0	1	0	1	0	1	0	1
00110011	0	0	1	1	0	0	1	1
11001100	1	1	0	0	1	1	0	0
10101010	1	0	1	0	1	0	1	0
10011001	1	0	0	1	1	0	0	1
01110111	0	1	1	1	0	1	1	1
00010001	0	0	0	1	0	0	0	1

Analisa Pengujian

Data yang dikirimkan oleh mikrokontroler dapat diterima dengan baik oleh PC, begitu juga sebaliknya. Ini berarti komunikasi serial antara mikrokontroler dan PC berjalan lancar.

4.2. Pengujian Rangkaian Infra Merah dan Phototransistor.

Tujuan:

- Untuk mengetahui apakah rangkaian ini dapat bekerja.
- Untuk mengetahui tegangan output dari rangkaian ini.

Peralatan Yang Digunakan:

- Rangkaian Infra Merah dan Phototransistor.
- Power Supply 5 volt.

- Multimeter.

Langkah-Langkah Pengujian:

1. Memberikan sumber tegangan (Vcc) 5 volt pada rangkaian.
2. Mengukur tegangan output pada rangkaian tersebut.

Tabel 4.3

Hasil Pengujian Rangkaian Infra Merah & Phototansistor

Posisi Infra Merah	Tegangan (Volt)	Logika
Tak Terhalang	0.08	0
Terhalang	4.89	1

Analisa Pengujian:

Rangkaian ini akan memberikan logika 0 pada saat LED infra merah tak terhalang dan logika 1 pada saat LED infra merah terhalang, yang kemudian akan menjadi inputan untuk rangkaian Microcontroller.

4.3. Pengujian Rangkaian Driver Relay.

Tujuan:

- Untuk mengetahui apakah rangkaian ini dapat bekerja.

Peralatan Yang Digunakan:

- Rangkaian Driver Relay.
- Power Supply 12 volt.

Langkah-Langkah Pengujian:

1. Memberikan sumber tegangan 12 volt pada relay.
2. Memberi tegangan input yang merupakan output dari Microcontroller.

Tabel 4.4

Hasil Pengujian Rangkaian Driver Relay

Vin (Volt)	Logika	Relay
0	0	OFF
4.85	1	ON

4.4. Pengujian Rangkaian Sensor Lampu.

Tujuan:

- Untuk mengetahui apakah rangkaian ini dapat bekerja.

Peralatan Yang Digunakan:

- Rangkaian Sensor Lampu.
- Power Supply 12 volt dan 5 volt.
- Multimeter.

Langkah-Langkah Pengujian:

1. Memberikan sumber tegangan (Vcc) 5 volt pada rangkaian.
2. Memberikan sumber tegangan (Vcc) 12 volt pada relay.
3. Memberikan kemungkinan gelap terang pada LDR yang merupakan sensor dari rangkaian ini.

4. Mengeset resistor variable dengan menyesuaikan antara intensitas cahaya lingkungan sekitarnya dengan saat penyaklaran.
5. Mengukur tegangan output pada rangkaian tersebut.

Tabel 4.5

Hasil Pengujian Rangkaian Sensor Lampu

Sensor Lampu 1 (Lampu Ruang)		
Intensitas Cahaya	**Vout (Volt)**	**Logika**
Gelap	0.09	0
Terang	3.69	1
Sensor Lampu 2 (Lampu Otomatis)		
Intensitas Cahaya	**Vout (Volt)**	**Logika**
Gelap	3.69	1
Terang	0.09	0

Analisa Pengujian:

- **Pada Sensor Lampu 1 (Lampu Ruang).**

Apabila lampu ruangan telah menyala atau keadaan ruang terang, maka rangkaian sensor ini akan memberikan logika 1 atau sebaliknya, dan logika ini akan menjadi inputan bagi Microcontroller. Sehingga microcontroller dapat mendeteksi apakah lampu ruangan tersebut dalam keadaan menyala atau padam, yang kemudian dikirim ke PC sebagai pusat control.

Pada Sensor Lampu 2 (Lampu Otomatis).

Apabila keadaan sekitarnya gelap maka rangkaian sensor ini akan memberikan logika 1 atau sebaliknya, dan logika ini akan menjadi inputan bagi driver relay. Driver relay akan menggerakkan relay yang merupakan saklar dari sumber tegangan jala-jala bagi lampu. Sehingga apabila keadaan sekitarnya gelap, maka lampu secara otomatis akan menyala, begitu juga untuk sebaliknya.

4.5. Pengujian Keseluruhan Sistem

Tujuan:

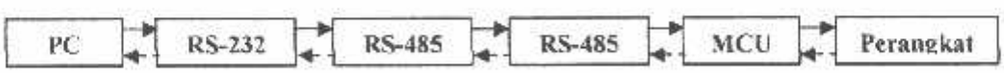
- Untuk mengetahui apakah sistem dapat bekerja seperti yang diharapkan.

Peralatan Yang Digunakan:

- Power supply 12 volt dan 5 volt.
- Seluruh Perangkat Yang Akan Dikontrol.
- MCU *(Microcontroller Unit)*
- PC.

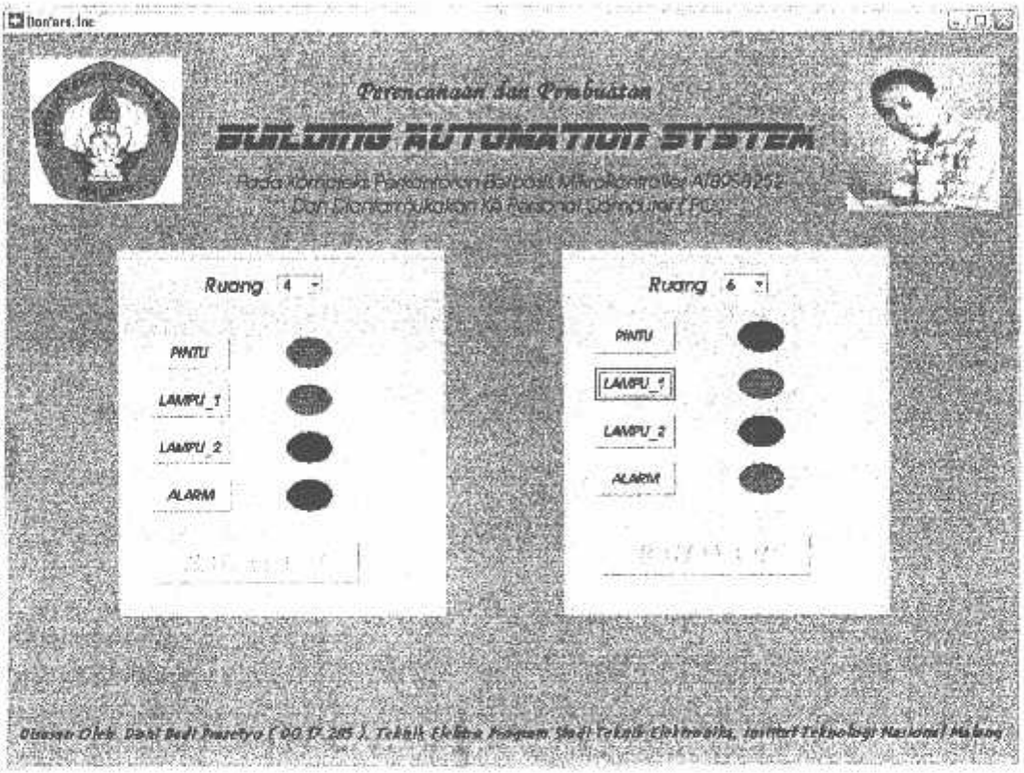
Langkah-Langkah Pengujian:

1. Menyusun sistem seperti pada diagram blok dibawah ini.



Gambar 4.5
Susunan Diagram Blok Sistem

2. Memberikan sumber tegangan pada semua sirkuit.
3. Memberikan perintah-perintah ke perangkat dengan cara meng-*click* icon panel pada layar monitor komputer.



Gambar 4.6
Tampilan Keseluruhan Sistem

Tabel 4.6.

Tabel Hasil Pengujian Keseluruhan Sistem

NO	PANEL	LAMPU KONTROL	KONDISI PERANGKAT
1.	PINTU	Hitam	Terbuka
		Merah	Terkunci
2.	LAMPU 1	Hitam	Padam
		Merah	Menyala
3.	LAMPU 2	Hitam	Padam
		Merah	Menyala
4.	ALARM	Hitam	Aktif
		Merah	Tidak Aktif
5.	TANDA BAHAYA	Tidak Berkedip	Tidak Mendeteksi Sesuatu
		Berkedip	Mendeteksi Sesuatu

Analisa Pengujian:

Terjadi perubahan warna lampu kontrol pada layar monitor sebagai status bahwa perangkat yang diberi perintah bekerja dengan baik, seperti pada tabel 4.6.

BAB V

PENUTUP

5.1. Kesimpulan

Dari pengamatan sampai pengujian alat, dapat diambil kesimpulan sebagai berikut :

1. Pada pengujian alat ini, jarak antara komputer dan MCU terjauh sekitar 20 meter, dan komunikasi data masih dapat dilakukan dengan baik
2. Sistem ini menggunakan komunikasi data serial dengan metode *Half Duplex*, sehingga terdapat tenggang waktu antara pengiriman perintah dan penerimaan status dari MCU *(Microcontroler Unit)* oleh komputer sekitar 65 ms.
3. Pada pengujian keseluruhan, sistem berjalan dengan sempurna yang meliputi: penguncian pintu, menghidup/mematikan lampu secara otomatis dan manual, serta mengaktikfan alarm untuk sistem keamanan.
4. Lampu otomatis bekerja berdasarkan intensitas cahaya lingkungan sekitarnya. Bila dalam keadaan gelap maka lampu akan menyala, sedangkan bila dalam keadaan terang lampu akan padam.

5.2. Saran

1. Jika ingin melakukan pengembangan pada alat ini, sebaiknya dilakukan pengembangan pada banyaknya jumlah perangkat dan jumlah ruangan yang akan dikontrol.
2. Untuk mendapatkan sistem komunikasi data yang sempurna, sebaiknya menggunakan komponen dan jenis kabel line yang berkualitas.

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INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

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NIM	:	00.17.285
Jurusan	:	TEKNIK ELEKTRO S-1
Konsentrasi	:	TEKNIK ELEKTRONIKA
Judul Skripsi	:	

PERENCANAAN DAN PEMBUATAN BUILDING AUTOMATION SYSTEM PADA KOMPLEKS PERKANTORAN BERBASIS MIKROKONTROLLER AT89S8252 DAN DIANTARMUKAKAN KE PERSONAL KOMPUTER (PC)

Tanggal Pengajuan Skripsi	:	9 Juni 2005
Selesai Penulisan Skripsi	:	14 Maret 2006
Dosen Pembimbing	:	Ir.F.Yudi Limpraptono, MT.
Telah Dievaluasi Dengan Nilai	:	90

Diperiksa dan Disetujui:

Ketua Jurusan
Teknik Elektro S-1

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Dosen Pembimbing

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INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

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NIM	:	00.17.285
Jurusan	:	TEKNIK ELEKTRO S-1
Konsentrasi	:	TEKNIK ELEKTRONIKA
Judul	:	

PERENCANAAN DAN PEMBUATAN BUILDING AUTOMATION SYSTEM PADA KOMPLEKS PERKANTORAN BERBASIS MIKROKONTROLLER AT89S8252 DAN DIANTARMUKAKAN KE PERSONAL KOMPUTER (PC)

No.	Uraian	Paraf
	• Sensor Infra Merah Untuk Luar Gedung. • Analisa Pengujian Seluruh Sistem. • Kesimpulan.	

Disetujui:

Penguji I

(**Ir.Usman Djuanda, MM**)
NIP.P. 070610501350

Penguji II

(**Mohammad Ashar, ST, MT**)

Mengetahui,
Dosen Pembimbing

(**Ir.F.Yudi Limpraptono, MT**)
NIP.Y. 1039500274

INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGURA-GURA 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Doni Budi Prasetyo
Nim : 0017285
Masa Bimbingan : 22-Jul-2005 s/d 22-Jan-2006
Judul Skripsi : Perencanaan dan pembuatan Building Automotion sistem pada kompleks perkantoran berbasis mikrokontroller AT89S8252 dan antarmukakan ke Personal Computer (PC)

NO	Tanggal	Uraian	Paraf Pembimbing
1.	7/9 2005	Bab I s/d IV	
2.	9/9 2005	Revisi Bab I s/d IV	
3.	7/2 2006	Demo alat	
4.		Melalui Seminar	
5.		Bab IV & V	
6.	4/3 2006	Bab I — V	
7.			
8.			
9.			
10.			

Malang, 2005
Dosen Pembimbing

Ir. F. Yudi Limpraptono, MT

Form. S-4a

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA :
N I M :
Perbaikan meliputi :

SARAN

perlu juga Sirine / Bel bila terjadi :
1. Pencurian, melalui atap
2. Kebocoran dengan sensor asap
3. Ada benda bergerak berpindah atau gangguan benda padat di dalam

Malang, 18 - 03 - 2006

([illegible])

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

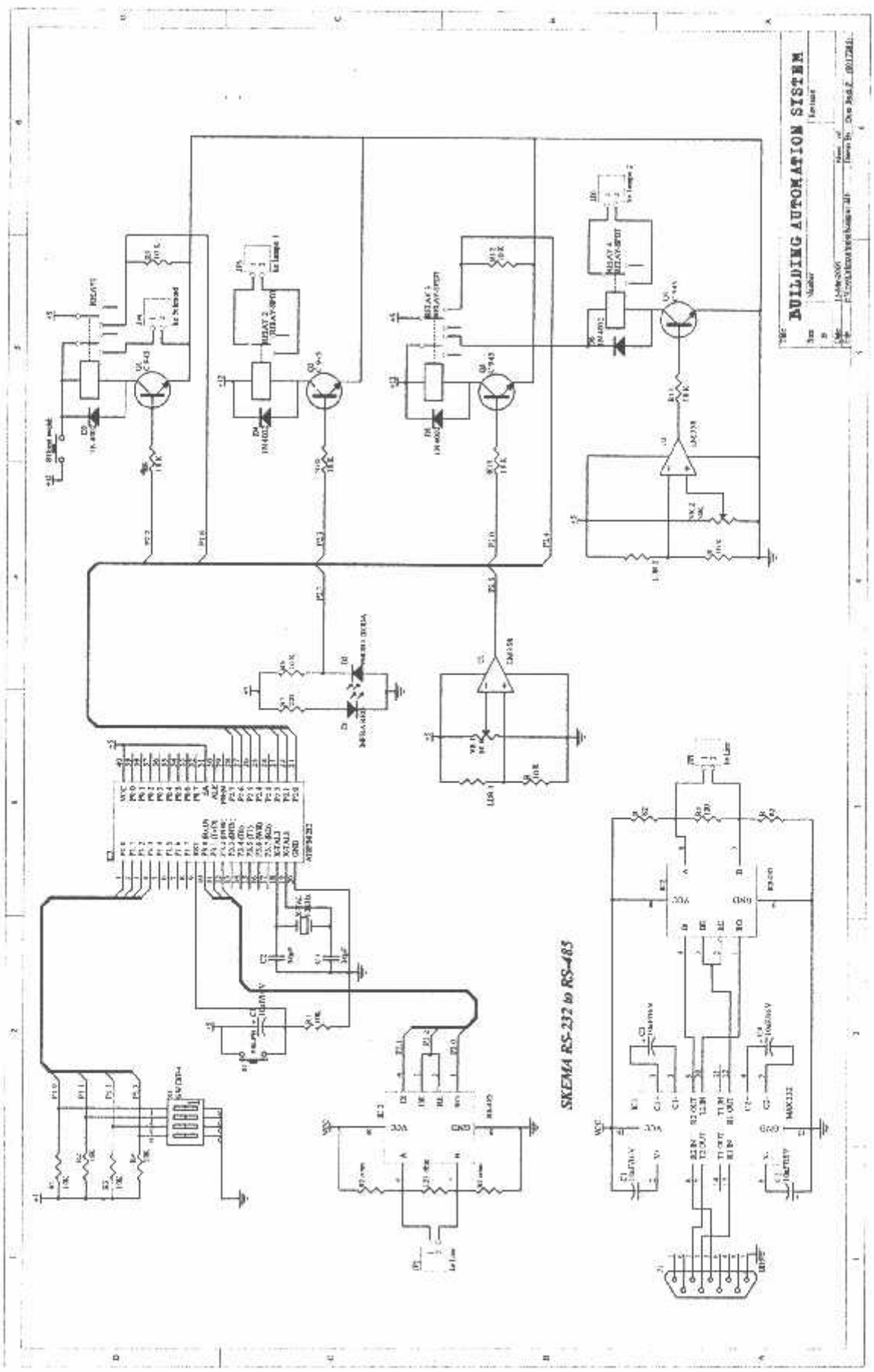
NAMA :
N I M :
Perbaikan meliputi :

- Sensor Inframerah u/ Luar Gedung.
- Analisa pengujian sistem system
- Kesimpulan

Malang,

(M. ASHAR)

LAMPIRAN


BUILDING AUTOMATION SYSTEM
SKEMA RS-232 to RS-485

(LISTING PROGRAM MICROCONTROLLER)

```
        org     0h
        sjmp    start
;
        org     23h
        clr     ES
        jnb     RI,$
        clr     RI
        mov     A,sbuf
        setb    ES
        reti
;
        Rly0    Bit  P2.0
        Rly1    Bit  P2.1
        Rly2    Bit  P2.2
        Slpl    Bit  P2.4
        Ldr0    Bit  P2.5
        Ssld    Bit  P2.6
        Ldr1    Bit  P2.7
        Krm0    Bit  P3.2
        Eemn    Equ 00001000b
        Eemw    Equ 00010000b
        Wtdg    Equ 00000010b
        Wmcn    Equ  96h
        Dly0    Equ  30h
        Dly1    Equ  31h
;
start:  acall   ser_in
        acall   amb_dt
```

```
        clr     Rly0
        clr     Rly1
        clr     Rly2
;
ckup0:  cjne    R1,#1,ckup1
        setb    Rly2
ckup1:  cjne    R2,#1,ckup2
        setb    Rly1
ckup2:  cjne    R3,#1,ckup3
        setb    Rly0
ckup3:  sjmp    cek0
;
cek0:   acall   tngdt
        cjne    R6,#08h,cek1
        cjne    R1,#0,snf1
        mov     R1,#1
        orl     Wmcn,#Eemn
        orl     Wmcn,#Eemw
        mov     DPH,#00h
        mov     DPL,#00h
        mov     A,#01h
        movx    @DPTR,A
        acall   wt_wr
        xrl     Wmcn,#Eemw
        xrl     Wmcn,#Eemn
cks00:  jnb     Ssld,cks01
        mov     A,R0
        anl     A,#0F7h
        orl     A,#80h
        acall   ser_sd
```

```
cks01: jb    Ssld,cks02
       mov   A,R0
       orl   A,#88h
       acall ser_sd
cks02: setb  Rly2
       sjmp  cek1
snf1:  cjne  R1,#1,cek1
       mov   R1,#0
       orl   Wmcn,#Eemn
       orl   Wmcn,#Eemw
       mov   DPH,#00h
       mov   DPL,#00h
       mov   A,#00h
       movx  @DPTR,A
       acall wt_wr
       xrl   Wmcn,#Eemw
       xrl   Wmcn,#Eemn
cks03: jnb   Ssld,cks04
       mov   A,R0
       anl   A,#0F7h
       orl   A,#80h
       acall ser_sd
cks04: jb    Ssld,cks05
       mov   A,R0
       orl   A,#88h
       acall ser_sd
cks05: clr   Rly2
       sjmp  cek1
;
cek1:  cjne  R6,#09h,cek2
```

```
        cjne    R2,#0,snf2
        mov     R2,#1
        orl     Wmcn,#Eemn
        orl     Wmcn,#Eemw
        mov     DPH,#00h
        mov     DPL,#01h
        mov     A,#01h
        movx    @DPTR,A
        acall   wt_wr
        xrl     Wmcn,#Eemw
        xrl     Wmcn,#Eemn
cks06:  jnb     Ldr0,cks07
        mov     A,R0
        anl     A,#0F7h
        orl     A,#80h
        acall   ser_sd
cks07:  jb      Ldr0,cks08
        mov     A,R0
        orl     A,#88h
        acall   ser_sd
cks08:  setb    Rly1
        sjmp    cek2
snf2:   cjne    R2,#1,cek2
        mov     R2,#0
        orl     Wmcn,#Eemn
        orl     Wmcn,#Eemw
        mov     DPH,#00h
        mov     DPL,#01h
        mov     A,#00h
        movx    @DPTR,A
```

```
        acall   wt_wr
        xrl     Wmcn,#Eemw
        xrl     Wmcn,#Eemn
cks09:  jnb     Ldr0,cks10
        mov     A,R0
        anl     A,#0F7h
        orl     A,#80h
        acall   ser_sd
cks10:  jb      Ldr0,cks11
        mov     A,R0
        orl     A,#88h
        acall   ser_sd
cks11:  clr     Rly1
        sjmp    cek2
;
cek2:   cjne    R6,#0Ah,cek3
        cjne    R3,#0,snf3
        mov     R3,#1
        orl     Wmcn,#Eemn
        orl     Wmcn,#Eemw
        mov     DPH,#00h
        mov     DPL,#02h
        mov     A,#01h
        movx    @DPTR,A
        acall   wt_wr
        xrl     Wmcn,#Eemw
        xrl     Wmcn,#Eemn
cks12:  jnb     Slpl,cks13
        mov     A,R0
        anl     A,#0F7h
```

```
        orl     A,#80h
        acall   ser_sd
cks13:  jb      Slpl,cks14
        mov     A,R0
        orl     A,#88h
        acall   ser_sd
cks14:  setb    Rly0
        sjmp    cek3
snf3:   cjne    R3,#1,cek3
        mov     R3,#0
        orl     Wmcn,#Eemn
        orl     Wmcn,#Eemw
        mov     DPH,#00h
        mov     DPL,#02h
        mov     A,#00h
        movx    @DPTR,A
        acall   wt_wr
        xrl     Wmcn,#Eemw
        xrl     Wmcn,#Eemn
cks15:  jnb     Slpl,cks16
        mov     A,R0
        anl     A,#0F7h
        orl     A,#80h
        acall   ser_sd
cks16:  jb      Slpl,cks17
        mov     A,R0
        orl     A,#88h
        acall   ser_sd
cks17:  clr     Rly0
        sjmp    cek3
```

```
;
cek3:   cjne    R6,#0Bh,cek4
        cjne    R4,#0,snf4
        mov     R4,#1
        orl     Wmcn,#Eemn
        orl     Wmcn,#Eemw
        mov     DPH,#00h
        mov     DPL,#03h
        mov     A,#01h
        movx    @DPTR,A
        acall   wt_wr
        xrl     Wmcn,#Eemw
        xrl     Wmcn,#Eemn
        mov     A,R0
        orl     A,#88h
        acall   ser_sd
        sjmp    cek4
snf4:   cjne    R4,#1,cek4
        mov     R4,#0
        orl     Wmcn,#Eemn
        orl     Wmcn,#Eemw
        mov     DPH,#00h
        mov     DPL,#03h
        mov     A,#00h
        movx    @DPTR,A
        acall   wt_wr
        xrl     Wmcn,#Eemw
        xrl     Wmcn,#Eemn
        mov     A,R0
        anl     A,#0F7h
```

```
        orl     A,#80h
        acall   ser_sd
        mov     R7,#0
        sjmp    cek4
;
cek4:   ljmp    cek0
;
ngdt:   mov     A,#0FFh
ckdt:   cjne    A,#0FFh,ccdt
ckal0:  cjne    R7,#0,ckal1
        cjne    R4,#1,ckal2
        jnb     Ldr1,ckal2
        mov     R7,#1
ckal1:  acall   delay
        mov     A,R0
        orl     A,#8Fh
        acall   ser_sd
        acall   delay
        acall   delay
        acall   delay
        acall   delay
        acall   delay
ckal2:  sjmp    ckdt
ccdt:   mov     R0,A
        mov     B,#16
        div     AB
        mov     R5,A
        mov     R6,B
;
bc_dip: acall   delay
```

```
        mov   A,P1
        anl   A,#15
        mov   B,R5
        subb  A,B
        cjne  A,#0,tngdt
        ret
;
ser_sd: setb  Krm0
        acall delay
        clr   ES
        mov   sbuf,A
        jnb   ti,$
        clr   ti
        setb  ES
        clr   Krm0
        ret
;
ser_in: acall delay
        setb  EA
        mov   TMOD,#20h
        mov   TH1,#0F3H
        setb  TR1
        mov   SCON,#50h
        setb  ES
        clr   Krm0
        mov   R7,#0
        ret
;
amb_dt: orl   Wmcn,#Eemn
        mov   DPH,#00h
```

```
        mov   DPL,#00h
        movx  A,@DPTR
        mov   R1,A
        mov   DPH,#00h
        mov   DPL,#01h
        movx  A,@DPTR
        mov   R2,A
        mov   DPH,#00h
        mov   DPL,#02h
        movx  A,@DPTR
        mov   R3,A
        mov   DPH,#00h
        mov   DPL,#03h
        movx  A,@DPTR
        mov   R4,A
        xrl   Wmcn,#Eemn
;
ck_dt0: cjne  R1,#0FFh,ck_dt1
        mov   R1,#00h
ck_dt1: cjne  R2,#0FFh,ck_dt2
        mov   R2,#00h
ck_dt2: cjne  R3,#0FFh,ck_dt3
        mov   R3,#00h
ck_dt3: cjne  R4,#0FFh,ck_dt4
        mov   R4,#00h
ck_dt4: ret
;
wt_wr:  mov   A,Wmcn
        anl   A,#Wtdg
        jz    wt_wr
```

```
        ret
;
delay : mov   Dly0,#255
delay1: mov   Dly1,#255
delay2: djnz  Dly1,Delay2
        djnz  Dly0,Delay1
        ret
;
        end
```

(LISTING PROGRAM DELPHI)

```
unit Unit1;

interface

uses
  Windows, Messages, SysUtils, Variants, Classes, Graphics, Controls, Forms,
  Dialogs, ExtCtrls, OleCtrls, MSCommLib_TLB, StdCtrls, jpeg;

type
  TForm1 = class(TForm)
    Label1: TLabel;
    Label2: TLabel;
    Label3: TLabel;
    Label4: TLabel;
    Label5: TLabel;
    Image1: TImage;
    Image2: TImage;
    GroupBox1: TGroupBox;
    Shape1: TShape;
    Label6: TLabel;
    Button1: TButton;
    Button2: TButton;
    Button3: TButton;
    Button4: TButton;
    ComboBox1: TComboBox;
    GroupBox2: TGroupBox;
    Button5: TButton;
    Button6: TButton;
    Button7: TButton;
    Button8: TButton;
```

```
    MSComm1: TMSComm;
    Timer1: TTimer;
    ComboBox2: TComboBox;
    Label7: TLabel;
    Shape2: TShape;
    Shape3: TShape;
    Shape4: TShape;
    Shape5: TShape;
    Shape6: TShape;
    Shape7: TShape;
    Shape8: TShape;
    Button9: TButton;
    Button10: TButton;
    procedure Button1Click(Sender: TObject);
    procedure Timer1Timer(Sender: TObject);
    procedure FormShow(Sender: TObject);
    procedure ComboBox1Change(Sender: TObject);
    procedure ComboBox2Change(Sender: TObject);
    procedure Button2Click(Sender: TObject);
    procedure Button3Click(Sender: TObject);
    procedure Button4Click(Sender: TObject);
    procedure Button5Click(Sender: TObject);
    procedure Button6Click(Sender: TObject);
    procedure Button7Click(Sender: TObject);
    procedure Button8Click(Sender: TObject);
    procedure BufferInput;
  private
    { Private declarations }
  public
      buffer,buffer1:string;
      bufferOut:byte;
      z:string;
```

```
    Button:byte;
    settime:boolean;
  { Public declarations }
 end;

var
 Form1: TForm1;

implementation

{$R *.dfm}

procedure TForm1.Button1Click(Sender: TObject);
Var
    i:byte;
    z:string;
begin
 for i:=0 to 7 do
 begin
    z:=inttostr(i);
    if combobox1.Text=z then
    begin
        mscomm1.Output:=chr($08+($10*i));
        bufferOut:=$08-($10*i);
        button:=0;
    end;
 end;
end;

procedure TForm1.Timer1Timer(Sender: TObject);
{var
 tempR:byte;
```

```
 a: char;}
begin
 if settime=true then
 begin
  bufferinput;
 end;
 { buffer:=mscomm1.Input;
  if not(buffer='') then
   a:= buffer[1];
 if buffer = chr(bufferout or $88)then
 begin
     case  button of
     0: shape1.Brush.Color:=clred;
     1: shape2.Brush.Color:=clred;
     2: shape3.Brush.Color:=clred;
     3: shape4.Brush.Color:=clred;
     4: shape5.Brush.Color:=clred;
     5: shape6.Brush.Color:=clred;
     6: shape7.Brush.Color:=clred;
     7: shape8.Brush.Color:=clred;
     end;
 end;
 if buffer= chr((bufferout and $F7) or $80)then
 begin
     case  button of
     0: shape1.Brush.Color:=clblack;
     1: shape2.Brush.Color:=clblack;
     2: shape3.Brush.Color:=clblack;
     3: shape4.Brush.Color:=clblack;
     4: shape5.Brush.Color:=clblack;
     5: shape6.Brush.Color:=clblack;
     6: shape7.Brush.Color:=clblack;
```

```
      7: shape8.Brush.Color:=clblack;
      end;
  end;
  if buffer= chr(bufferout or $8F)then
  begin

      tempR:=(ord(A) div $10)-8;
      if strtoint(combobox1.Text) = tempR then
      begin
        button9.Enabled:=true;
        sleep(100);
        button9.Enabled:=false;
      end;
      if strtoint(combobox2.Text) = tempR then
      begin
        button10.Enabled:=true;
        sleep(100);
        button10.Enabled:=false;
      end;
  end; }

end;


procedure TForm1.FormShow(Sender: TObject);
var
      i:byte;
begin
      mscomm1.settings:= '2400,n,8,1';
      mscomm1.PortOpen:=true;
      shape1.Brush.Color:=clblack;
      shape2.Brush.Color:=clblack;
```

```
    shape3.Brush.Color:=clblack;
    shape4.Brush.Color:=clblack;
    shape5.Brush.Color:=clblack;
    shape6.Brush.Color:=clblack;
    shape7.Brush.Color:=clblack;
    shape8.Brush.Color:=clblack;
    settime:=true;
    for i:=0 to 7 do
    begin
        z:=inttostr(i);
        if i<>1 then
            combobox1.AddItem(z,combobox1);
        if i>0 then
            combobox2.AddItem(z,combobox2);
    end;
    combobox1.ItemIndex:=0;
    combobox2.ItemIndex:=0;
end;

procedure TForm1.ComboBox1Change(Sender: TObject);
var
    i:byte;
    p:string;
begin
    p:=combobox2.Text;
    combobox2.Clear;
    for i:=0 to 7 do
    begin
    z:=inttostr(i);
    if not(combobox1.Text =z) then
        combobox2.AddItem(z,combobox2);
    end;
```

```
    i:=0;
    repeat
        combobox2.ItemIndex:=i;
        inc(i);
    until combobox2.Text=p;

end;

procedure TForm1.ComboBox2Change(Sender: TObject);

var
    i:byte;
    p:string;
begin
    p:=combobox1.Text;
    combobox1.Clear;
    for i:=0 to 7 do
    begin
    z:=inttostr(i);
    if  not(combobox2.Text  =z) then
        combobox1.AddItem(z,combobox1);
    end;
    i:=0;
    repeat
        combobox1.ItemIndex:=i;
        inc(i);
    until combobox1.Text=p;
end;

procedure TForm1.Button2Click(Sender: TObject);

Var
```

```
    i:byte;
    z:string;
begin
 for i:=0 to 7 do
 begin
    z:=inttostr(i);
    if combobox1.Text=z then
    begin
        mscomm1.Output:=chr($09+($10*i));
        bufferOut:=$09+($10*i);
        button:=1;
    end;
 end;
end;

procedure TForm1.Button3Click(Sender: TObject);

Var
    i:byte;
    z:string;
begin
 for i:=0 to 7 do
 begin
    z:=inttostr(i);
    if combobox1.Text=z then
    begin
        mscomm1.Output:=chr($0A+($10*i));
        bufferOut:=$0A+($10*i);
        button:=2;
    end;
 end;
end;
```

```
procedure TForm1.Button4Click(Sender: TObject);
Var
    i:byte;
    z:string;
begin
 for i:=0 to 7 do
 begin
    z:=inttostr(i);
    if combobox1.Text=z then
    begin
        mscomm1.Output:=chr($0B+($10*i));
        bufferOut:=$0B+($10*i);
        button:=3;
        button9.Enabled :=false;
    end;
 end;
end;


procedure TForm1.Button5Click(Sender: TObject);
Var
    i:byte;
    z:string;
begin
 for i:=0 to 7 do
 begin
    z:=inttostr(i);
    if combobox2.Text=z then
    begin
        mscomm1.Output:=chr($08+($10*i));
```

```
            bufferOut:=$08+($10*i);
            button:=4;
        end;
  end;
end;


procedure TForm1.Button6Click(Sender: TObject);
Var
      i:byte;
      z:string;
begin
  for i:=0 to 7 do
  begin
      z:=inttostr(i);
      if combobox2.Text=z then
      begin
            mscomm1.Output:=chr($09+($10*i));
            bufferOut:=$09+($10*i);
            button:=5;
      end;
  end;
end;

            '

procedure TForm1.Button7Click(Sender: TObject);
Var
      i:byte;
      z:string;
begin
  for i:=0 to 7 do
  begin
```

```
    z:=inttostr(i);
    if combobox2.Text=z then
    begin
        mscomm1.Output:=chr($0A+($10*i));
        bufferOut:=$0A+($10*i);
        button:=6;
    end;
  end;
end;

procedure TForm1.Button8Click(Sender: TObject);
Var
    i:byte;
    z:string;
begin
  for i:=0 to 7 do
  begin
    z:=inttostr(i);
    if combobox2.Text=z then
    begin
        mscomm1.Output:=chr($0B+($10*i));
        bufferOut:=$0B+($10*i);
        button:=7;
        button10.Enabled:=false;
    end;
  end;
end;

procedure TForm1.BufferInput;
var
  tempR:byte;
```

```
 a: char;
begin
  buffer:=mscomm1.Input;
 if not(buffer='') then
    a:= buffer[1];
 if buffer = chr(bufferout or $88)then
 begin
      case  button of
      0: shape1.Brush.Color:=clred;
      1: shape2.Brush.Color:=clred;
      2: shape3.Brush.Color:=clred;
      3: shape4.Brush.Color:=clred;
      4: shape5.Brush.Color:=clred;
      5: shape6.Brush.Color:=clred;
      6: shape7.Brush.Color:=clred;
      7: shape8.Brush.Color:=clred;
      end;
 end;
 if buffer= chr((bufferout and $F7) or $80)then
 begin
      case  button of
      0: shape1.Brush.Color:=clblack;
      1: shape2.Brush.Color:=clblack;
      2: shape3.Brush.Color:=clblack;
      3: shape4.Brush.Color:=clblack;
      4: shape5.Brush.Color:=clblack;
      5: shape6.Brush.Color:=clblack;
      6: shape7.Brush.Color:=clblack;
      7: shape8.Brush.Color:=clblack;
      end;
 end;
 if buffer= chr(bufferout or $8F)then
```

```
begin

    tempR:=(ord(A) div $10)-8;
    if strtoint(combobox1.Text) = tempR then
    begin
      button9.Enabled:=true;
      sleep(100);
      button9.Enabled:=false;
    end;
    if strtoint(combobox2.Text) = tempR then
    begin
      button10.Enabled:=true;
      sleep(100);
      button10.Enabled:=false;
    end;
 end;

end;


end.
```

Features

- Compatible with MCS-51™ Products
- 8K Bytes of In-System Reprogrammable Downloadable Flash Memory
  - SPI Serial Interface for Program Downloading
  - Endurance: 1,000 Write/Erase Cycles
- 2K Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- 4.0V to 6V Operating Range
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Nine Interrupt Sources
- Programmable UART Serial Channel
- SPI Serial Interface
- Low Power Idle and Power Down Modes
- Interrupt Recovery From Power Down
- Programmable Watchdog Timer
- Dual Data Pointer
- Power Off Flag

Description

The AT89S8252 is a low-power, high-performance CMOS 8-bit microcomputer with 8K bytes of Downloadable Flash programmable and erasable read only memory and 2K bytes of EEPROM. The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard 80C51 instruction set and pinout. The on-chip Downloadable Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Downloadable Flash on a monolithic chip, the Atmel AT89S8252 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

The AT89S8252 provides the following standard features: 8K bytes of Downloadable Flash, 2K bytes of EEPROM, 256 bytes of RAM, 32 I/O lines, programmable watchdog timer, two Data Pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S8252 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

The Downloadable Flash can be changed a single byte at a time and is accessible through the SPI serial interface. Holding RESET active forces the SPI bus into a serial programming interface and allows the program memory to be written to or read from unless Lock Bit 2 has been activated.

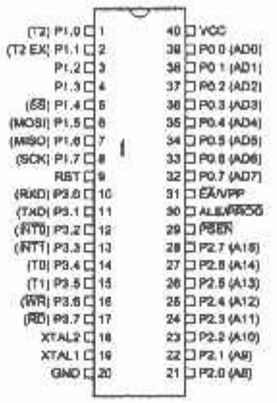
8-Bit Microcontroller with 8K Bytes Flash

AT89S8252

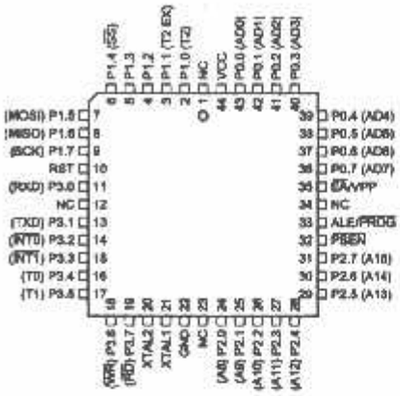
0401D-A-12/97

Pin Configurations

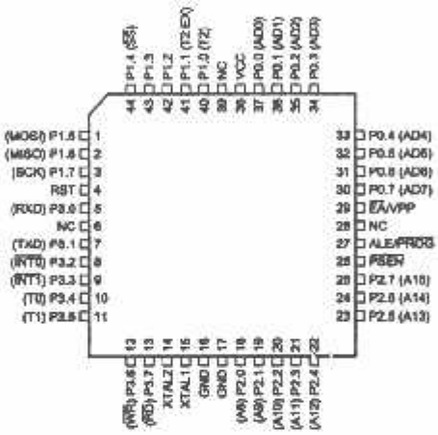
PDIP



PLCC



PQFP/TQFP



Pin Description

V_{CC}
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

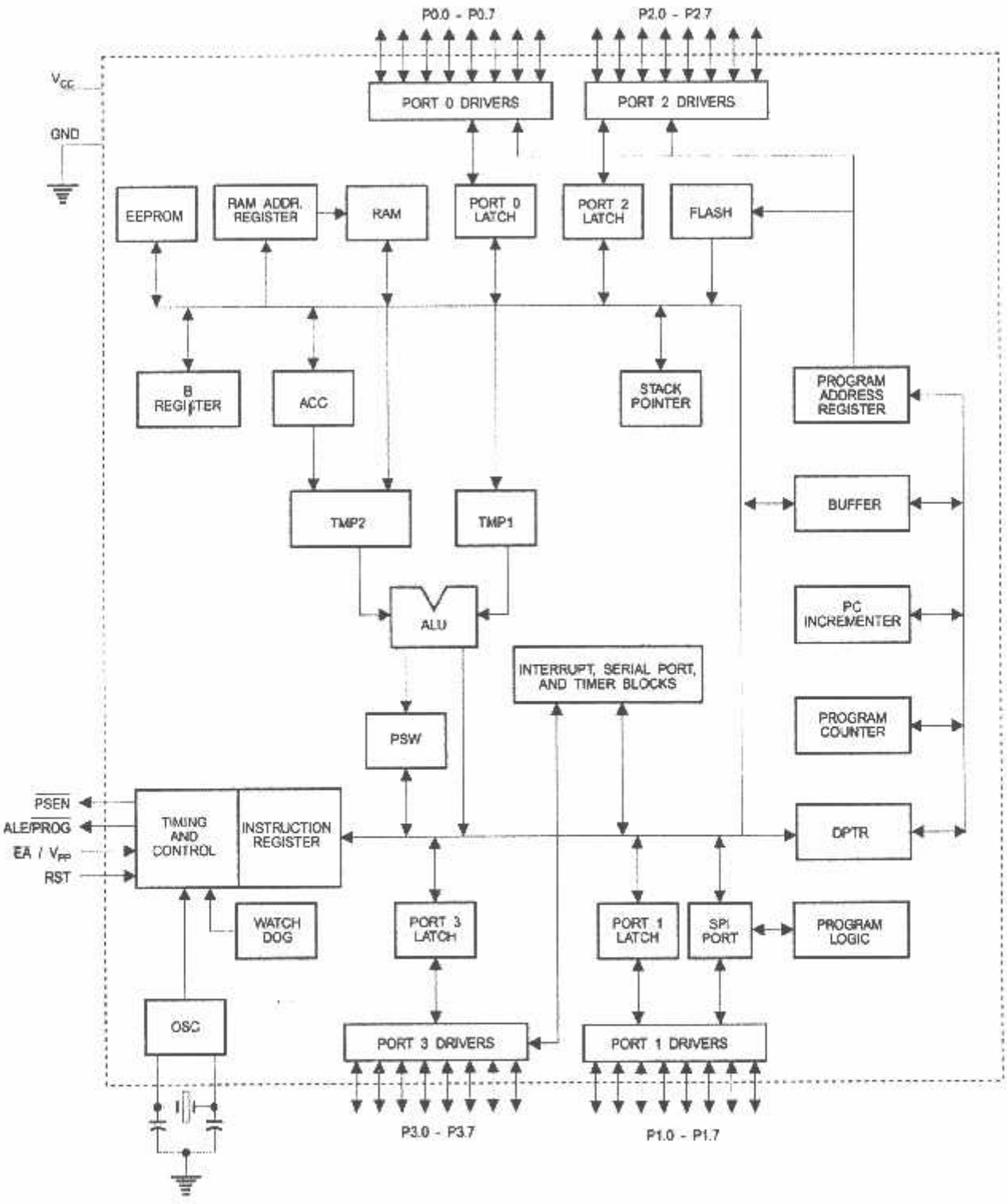
Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Block Diagram



Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8 bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/V_{PP}

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

XTAL1
Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2
Output from the inverting oscillator amplifier.

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

Table 1. AT89S8252 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 000001XX			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000		SPSR 00XXXXXX						0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						WMCON 00000010		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000	87H

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16 bit capture mode or 16-bit auto-reload mode.

Watchdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in Table 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The DPS bit selects one of two DPTR registers available.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 2. T2CON—Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16 bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

Table 3. WMCON—Watchdog and Memory Control Register

WMCON Address = 96H — Reset Value = 0000 0010B

Bit	7	6	5	4	3	2	1	0
	PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN

Symbol	Function
PS2 PS1 PS0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EEMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EEMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
DPS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
WDTRST RDY/$\overline{BSY}$	Watchdog Timer Reset and EEPROM Ready/$\overline{Busy}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{BSY}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{BSY}$ bit equals "0" and is automatically reset to "1" when programming is completed.
WDTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

Table 6. SPDR—SPI Data Register

SPDR Address = 86H — Reset Value = unchanged

Bit	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
	7	6	5	4	3	2	1	0

Data Memory—EEPROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. RDY/$\overline{BSY}$ = 0 means programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power Down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			Period (nominal)
PS2	PS1	PS0	
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-45, section titled, "Timer/Counters."

Timer 2

Timer 2 is a 16 bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-Reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

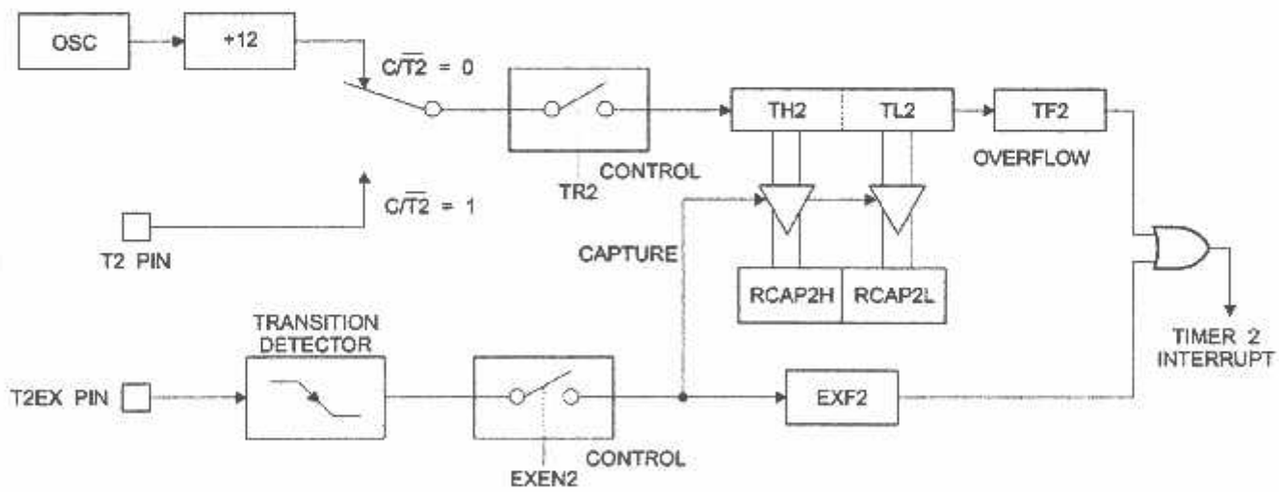
In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16 bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Auto-Reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16 bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to

Figure 1. Timer 2 in Capture Mode



0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16 bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16 bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16 bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 2. Timer 2 in Auto Reload Mode (DCEN = 0)

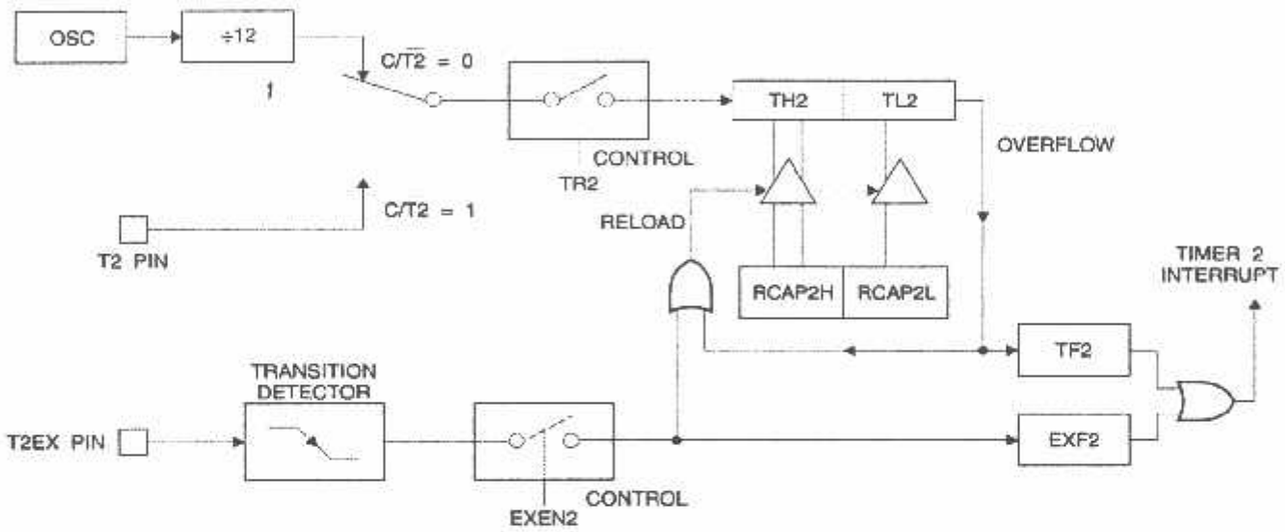


Table 9. T2MOD—Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

	—	—	—	—	—	—	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

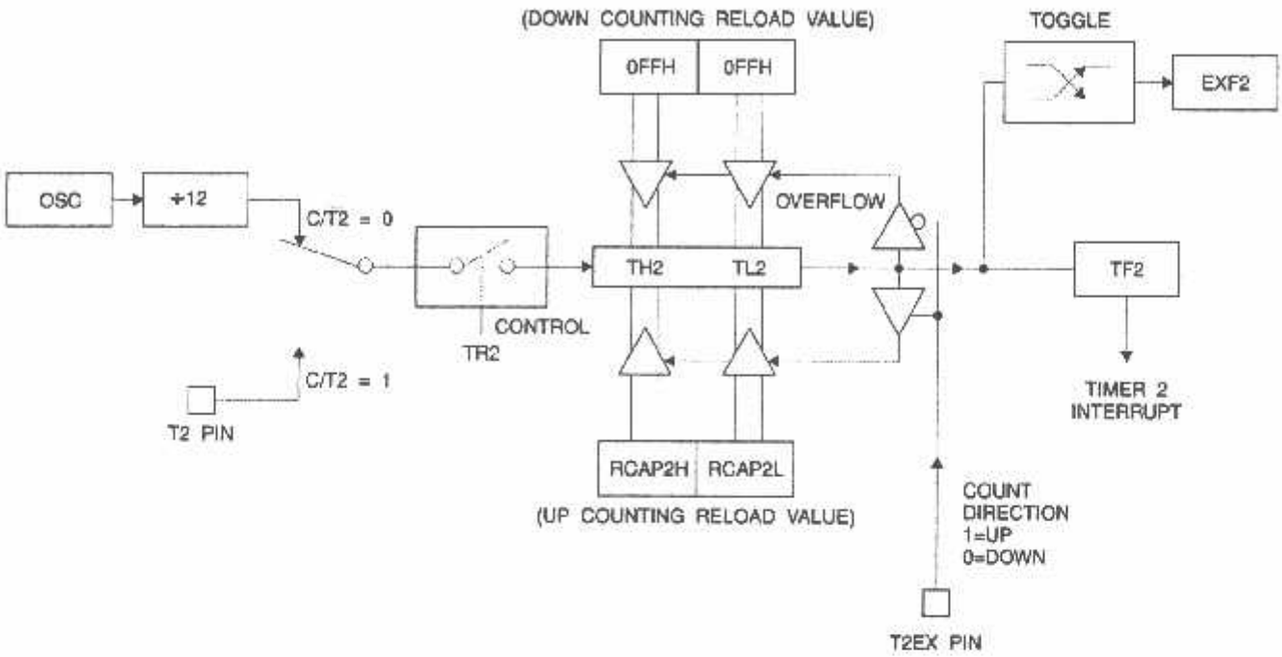
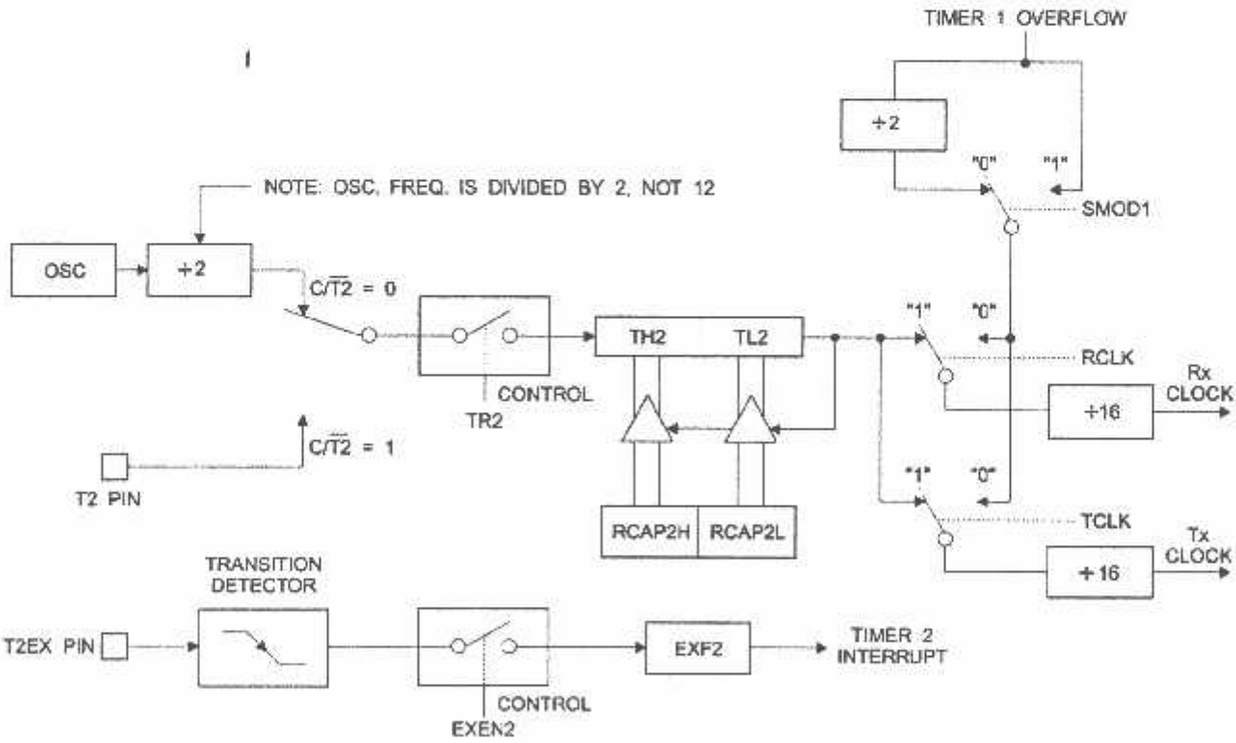


Figure 4. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16 bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

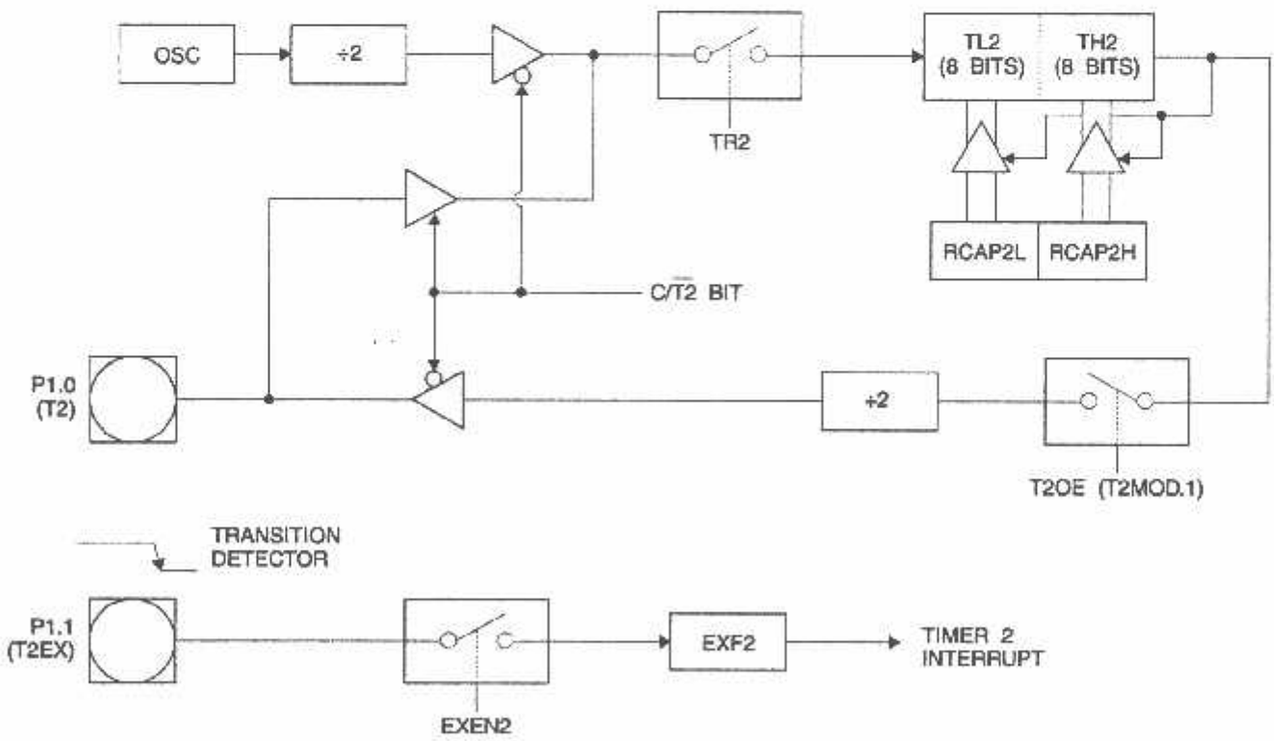
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16 bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Figure 5. Timer 2 in Clock-Out Mode



Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit $C/\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

UART

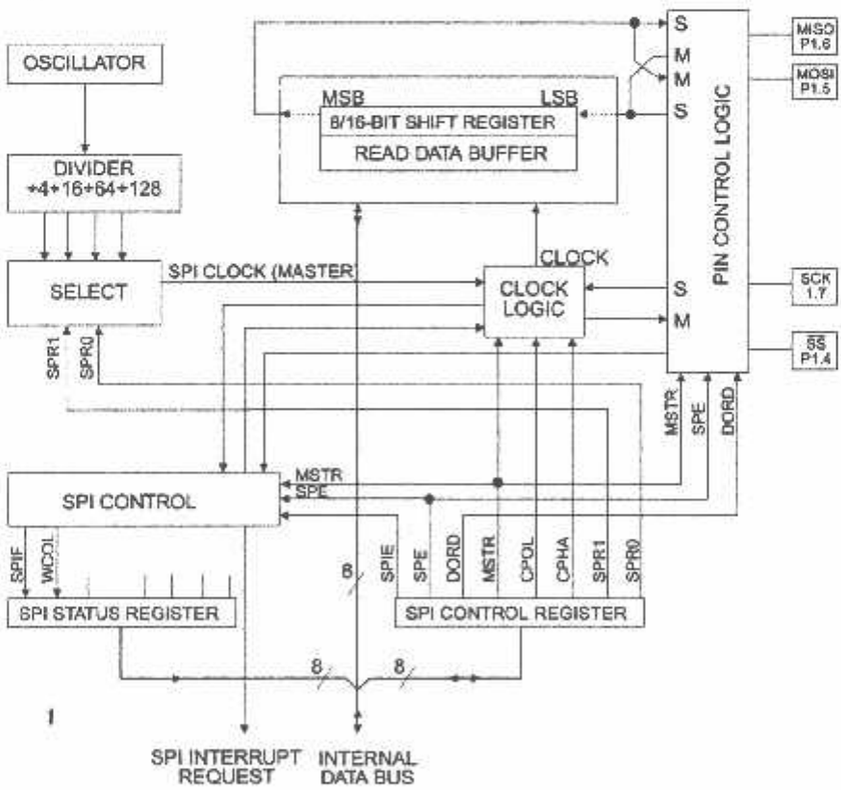
The UART in the AT89S8252 operates the same way as the UART in the AT89C51, AT89C52 and AT89C55. For further information, see the October 1995 Microcontroller Data Book, page 2-49, section titled, "Serial Interface."

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5-MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

Figure 6. SPI Block Diagram



The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figures 8 and 9.

Figure 7. SPI Master-Slave Interconnection

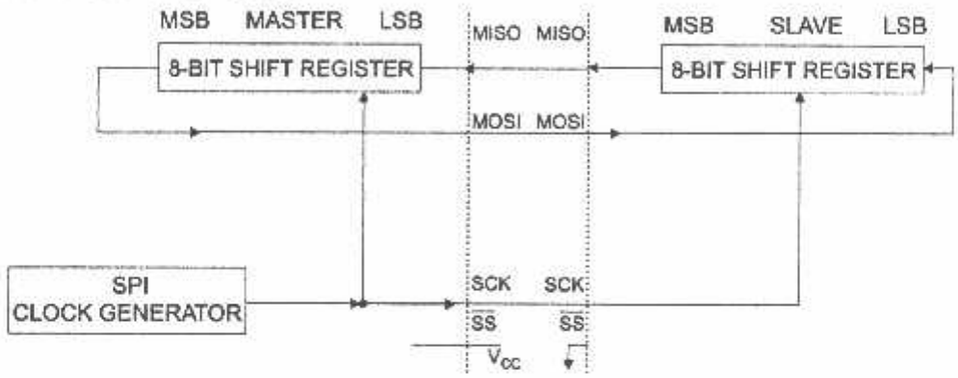
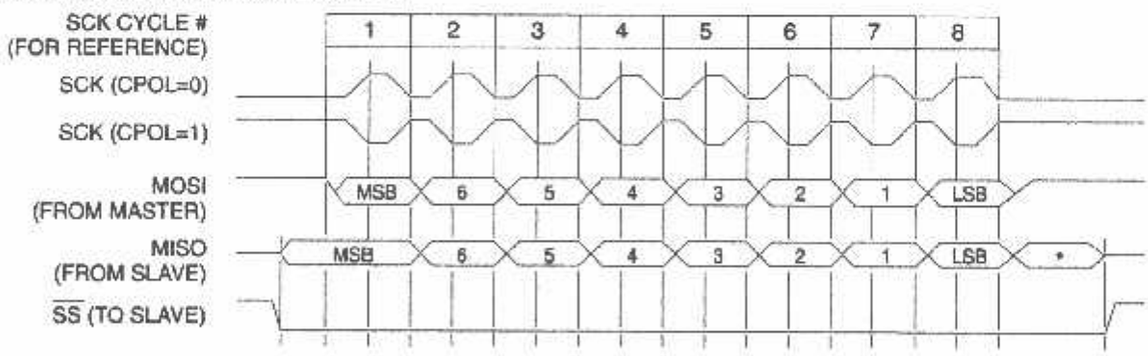
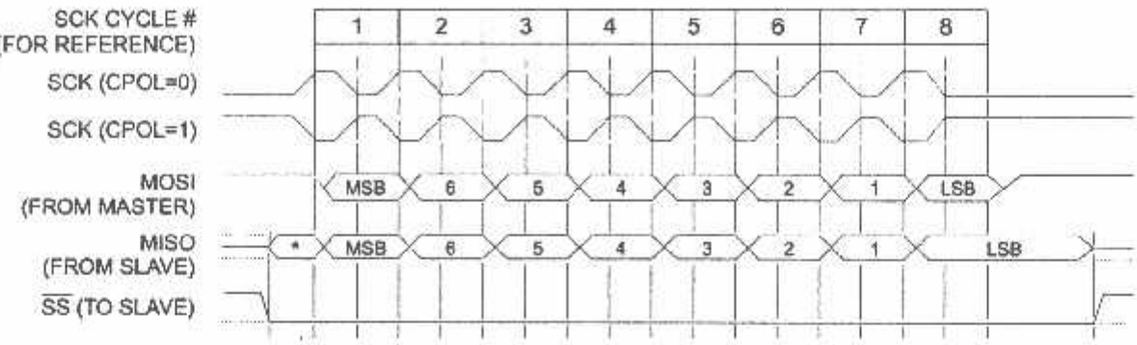


Figure 8. SPI transfer Format with CPHA = 0



*Not defined but normally MSB of character just received

Figure 9. SPI Transfer Format with CPHA = 1



*Not defined but normally LSB of previously transmitted character

Interrupts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 10. Interrupt Enable (IE) Register

(MSB) (LSB)

EA	—	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.

Figure 10. Interrupt Sources

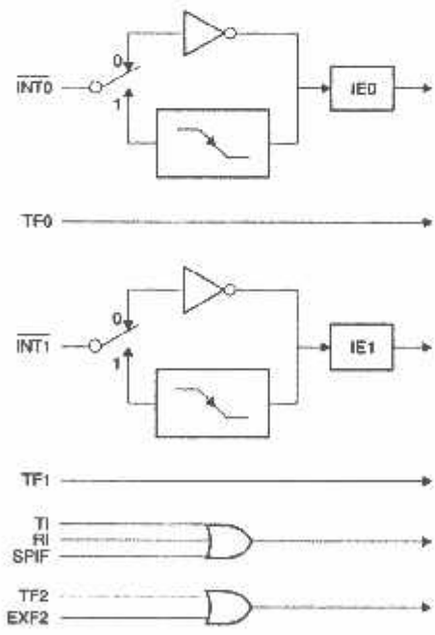


Figure 11. Oscillator Connections

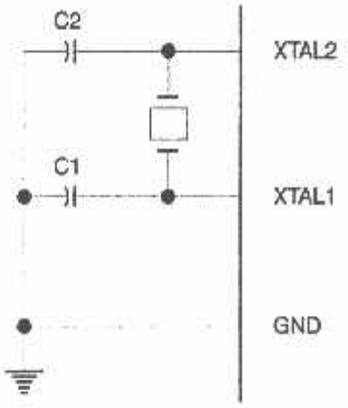
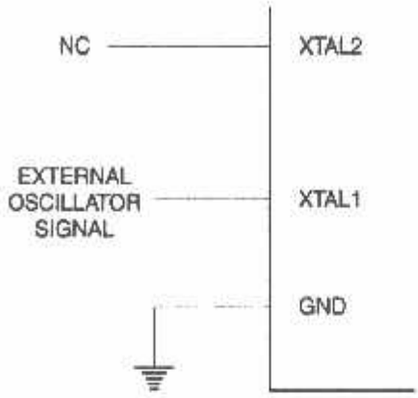


Figure 12. External Clock Drive Configuration



Note: Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power Down Mode

In the power down mode, the oscillator is stopped and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. Exit from power down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power down via an interrupt, the external interrupt must be enabled as level sensitive before entering power down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

Lock Bit Protection Modes[1][2]

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

Notes: 1. U = Unprogrammed
2. P = Programmed

Programming the Flash and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-Voltage (12V) Parallel programming mode and a Low-Voltage (5V) Serial programming mode. The serial programming mode provides a convenient way to download the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm

To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between V_{CC} and GND pins.
   Set RST pin to "H".
   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{PSEN}$ pin to "L"
   ALE pin to "H"
   $\overline{EA}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.
   Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.

8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:

   Set XTAL1 to "L".

   Set RST and $\overline{EA}$ pins to "L".

   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

$\overline{DATA}$ Polling

The AT89S8252 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$

The progress of byte programming in the parallel programming mode can also be monitored by the RDY/$\overline{BSY}$ output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate $\overline{BUSY}$. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify

If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase

Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse

A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

Programming Interface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Serial Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Algorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between V_{CC} and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

Serial Programming Instruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

Instruction Set

Instruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Chip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
Read Code Memory	aaaa a001 !	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Write Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
Read Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Write Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Write Lock Bits	1010 1100	LB1 LB2 LB3 x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

Notes: 1. $\overline{DATA}$ polling is used to indicate the end of a write cycle which typically takes less than 2.5 ms at 5V.

2. "aaaaa" = high order address.

3. "x" = don't care.

Flash and EEPROM Parallel Programming Modes

Mode	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
Serial Prog. Modes	H	h(1)	h(1)	x						
Chip Erase	H	L	⌐‾⌐ (2)	12V	H	L	L	L	X	X
Write (10K bytes) Memory	H	L	⌐‾⌐	12V	L	H	H	H	DIN	ADDR
Read (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
Write Lock Bits:	H	L	⌐‾⌐	12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
Read Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
Read Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
Read Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Serial Prog. Enable	H	L	⌐‾⌐ (2)	12V	L	H	L	H	P0.0 = 0	X
Serial Prog. Disable	H	L	⌐‾⌐ (2)	12V	L	H	L	H	P0.0 = 1	X
Read Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

Notes:
1. "h" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10-ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{BSY}$.
4. "X" = don't care

Figure 14. Programming the Flash/EEPROM Memory

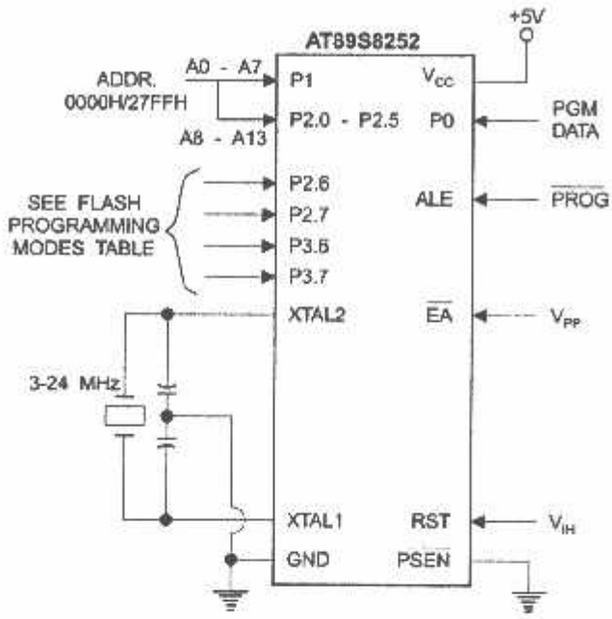


Figure 15. Flash/EEPROM Serial Downloading

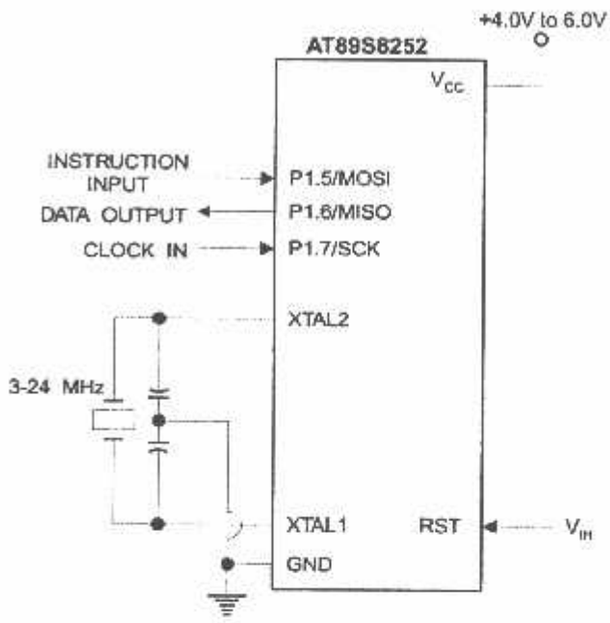
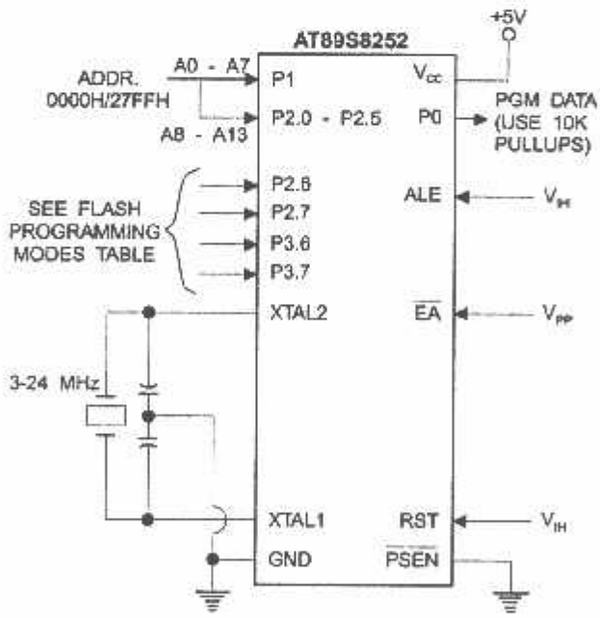


Figure 16. Verifying the Flash/EEPROM Memory

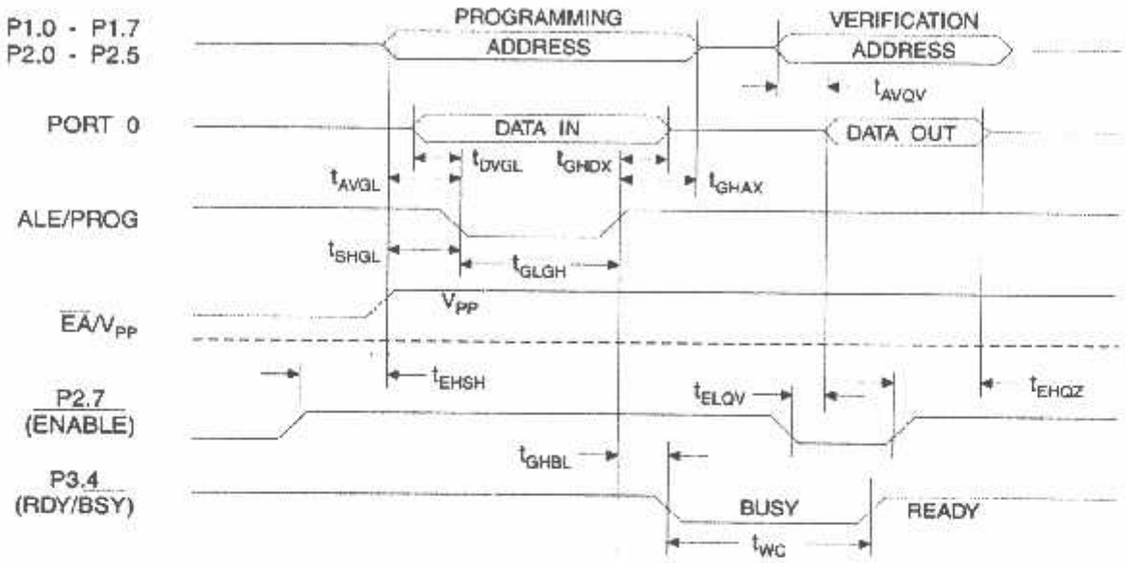


Flash Programming and Verification Characteristics-Parallel Mode

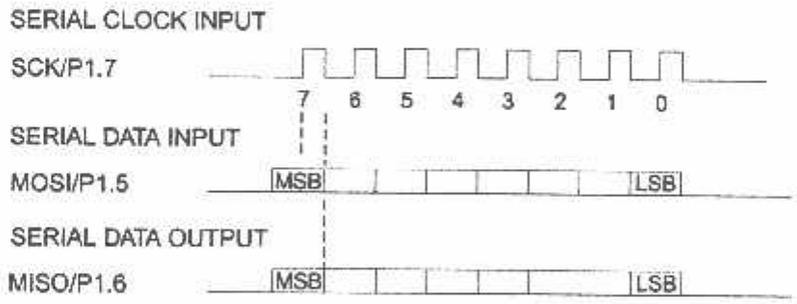
T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Flash/EEPROM Programming and Verification Waveforms - Parallel Mode



Serial Downloading Waveforms



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage (1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
V_{OL1}	Output Low Voltage (1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power Down Mode (2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power Down is 2V

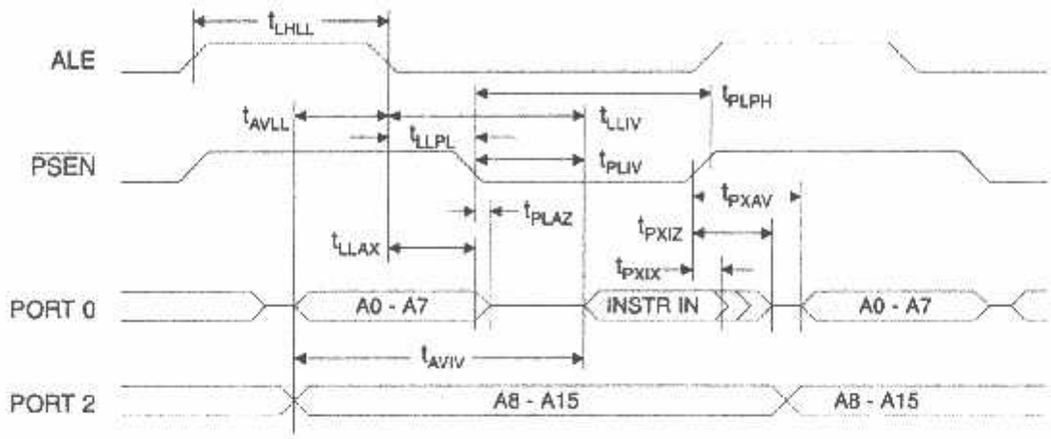
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

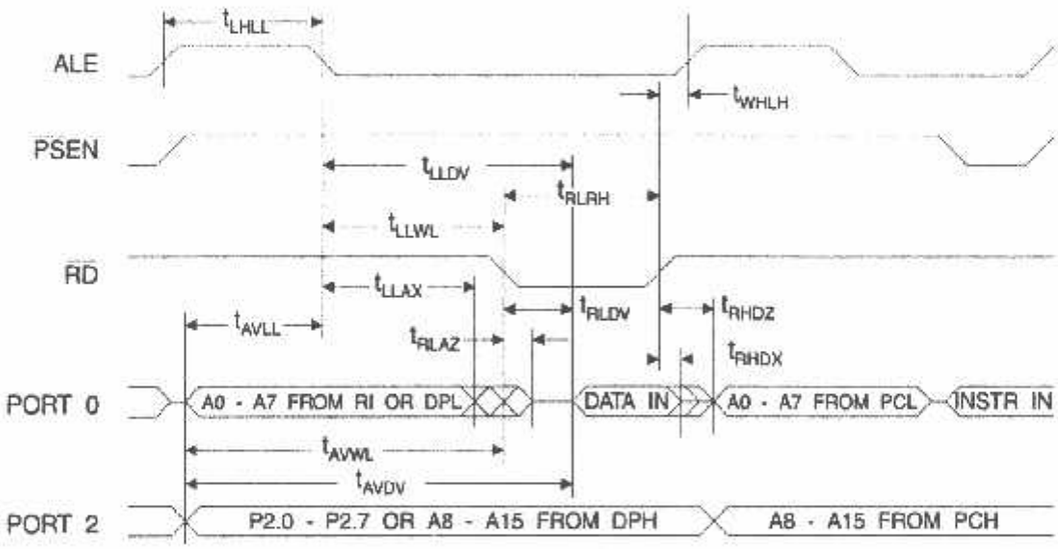
External Program and Data Memory Characteristics

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{LHLL}	ALE Pulse Width	$2t_{CLCL}$ - 40		ns
t_{AVLL}	Address Valid to ALE Low	t_{CLCL} - 13		ns
t_{LLAX}	Address Hold After ALE Low	t_{CLCL} - 20		ns
t_{LLIV}	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		t_{CLCL} - 10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
t_{AVIV}	Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		$2t_{CLCL}$ - 28	ns
t_{LLDV}	ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
t_{AVDV}	Address to Valid Data In		$9t_{CLCL}$ - 165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
t_{WHQX}	Data Hold After $\overline{WR}$	t_{CLCL} - 20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

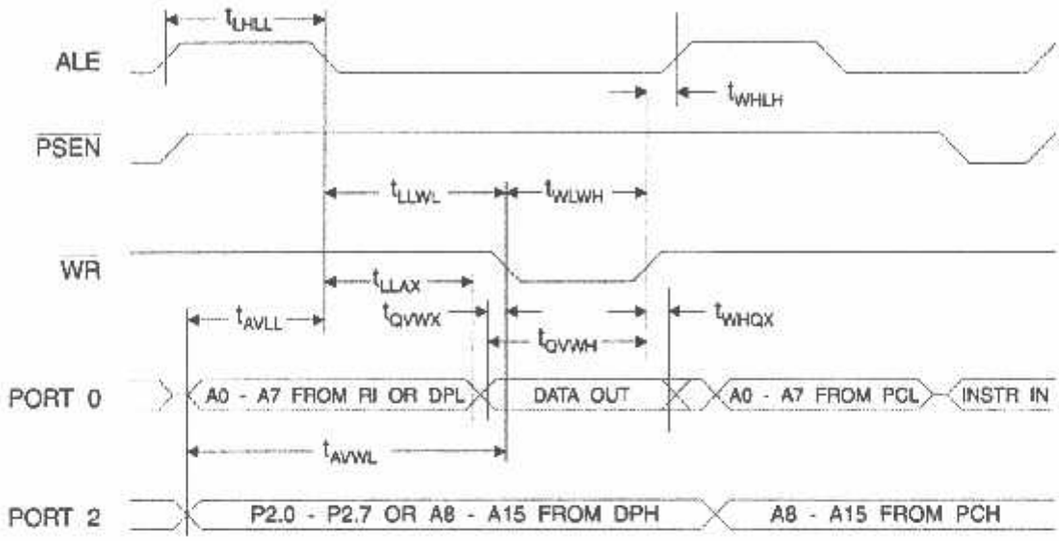
External Program Memory Read Cycle



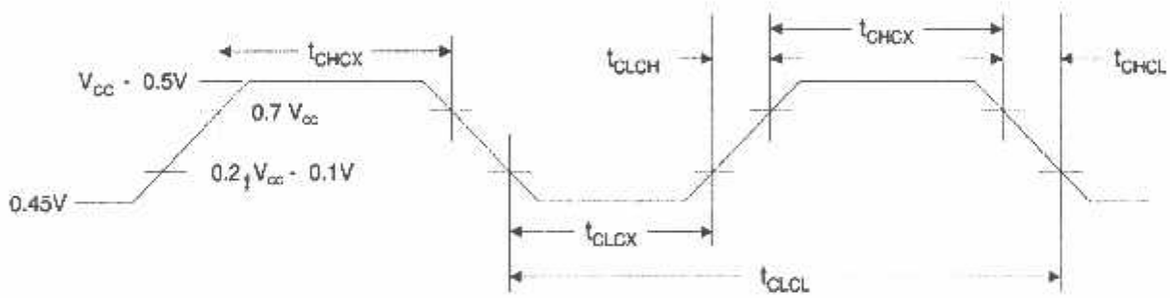
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

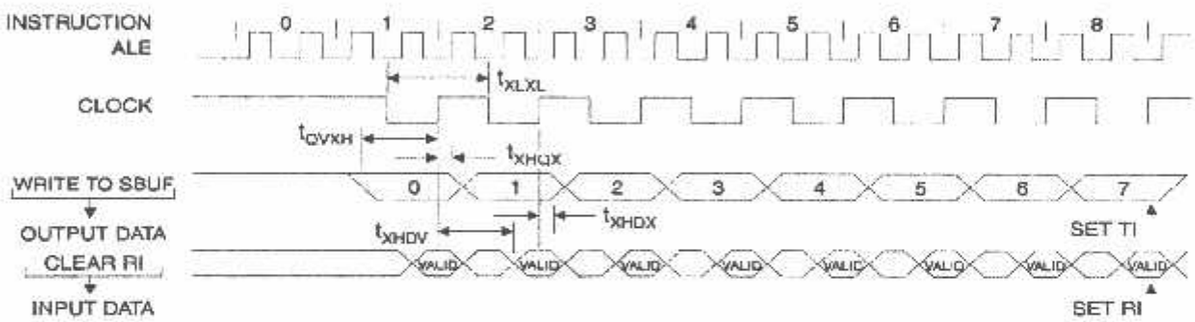
Symbol	Parameter	V_{CC} = 4.0V to 6.0V		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

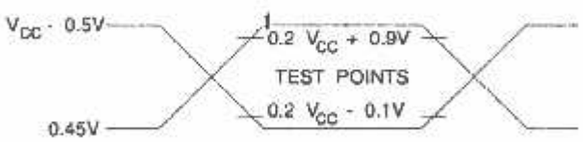
The values in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	$2t_{CLCL}$ - 117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

Shift Register Mode Timing Waveforms

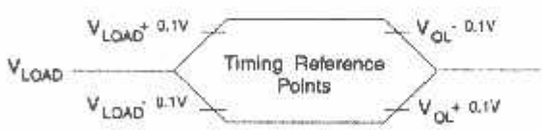


AC Testing Input/Output Waveforms[1]



Notes: 1. AC inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

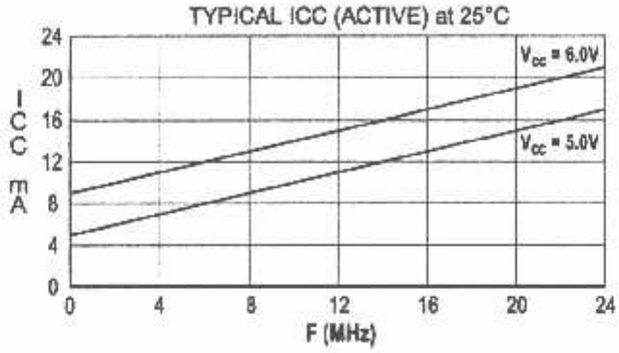
Float Waveforms[1]



Notes: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

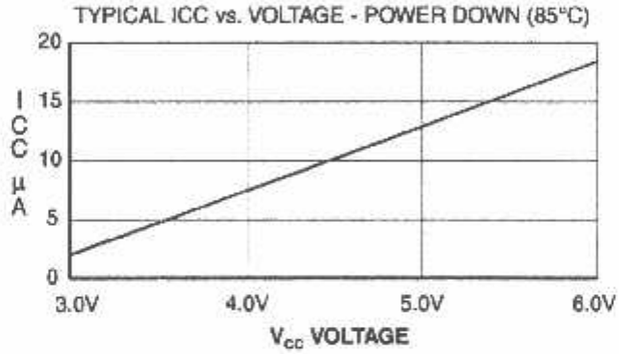
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



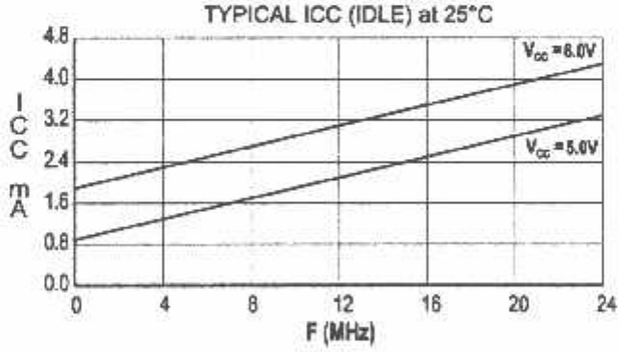
AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



AT89S8252

TYPICAL ICC (IDLE) at 25°C



Notes: 1. XTAL1 tied to GND for Icc (power down)
2. Lock bits programmed

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
16	4.0V to 6.0V	AT89S8252-16AA AT89S8252-16JA AT89S8252-16PA AT89S8252-16QA	44A 44J 40P6 44Q	Automotive (-40°C to 105°C)
24	4.0V to 6.0V	AT89S8252-24AC AT89S8252-24JC AT89S8252-24PC AT89S8252-24QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
	4.0V to 6.0V	AT89S8252-24AI AT89S8252-24JI AT89S8252-24PI AT89S8252-24QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S8252-33AC AT89S8252-33JC AT89S8252-33PC AT89S8252-33QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)

= Preliminary Information

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

HARRIS SEMICONDUCTOR

ICL232

+5V Powered Dual RS-232 Transmitter/Receiver

December 1993

Features

- Meets All RS-232C Specifications
- Requires Only Single +5V Power Supply
- Onboard Voltage Doubler/Inverter
- Low Power Consumption
- 2 Drivers
  - ±9V Output Swing for +5V Input
  - 300Ω Power-off Source Impedance
  - Output Current Limiting
  - TTL/CMOS Compatible
  - 30V/µs Maximum Slew Rate
- 2 Receivers
  - ±30V Input Voltage Range
  - 3kΩ to 7kΩ Input Impedance
  - 0.5V Hysteresis to Improve Noise Rejection
- All Critical Parameters are Guaranteed Over the Entire Commercial, Industrial and Military Temperature Ranges

Applications

- Any System Requiring RS-232 Communications Port
  - Computer - Portable and Mainframe
  - Peripheral - Printers and Terminals
  - Portable Instrumentation
  - Modems
  - Dataloggers

Description

The ICL232 is a dual RS-232 transmitter/receiver interface circuit that meets all EIA RS-232C specifications. It requires a single +5V power supply, and features two onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply.

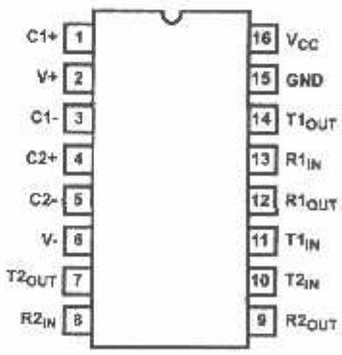
The drivers feature true TTL/CMOS input compatibility, slew-rate-limited output, and 300Ω power-off source impedance. The receivers can handle up to +30V, and have a 3kΩ to 7kΩ input impedance. The receivers also have hysteresis to improve noise rejection.

Ordering Information

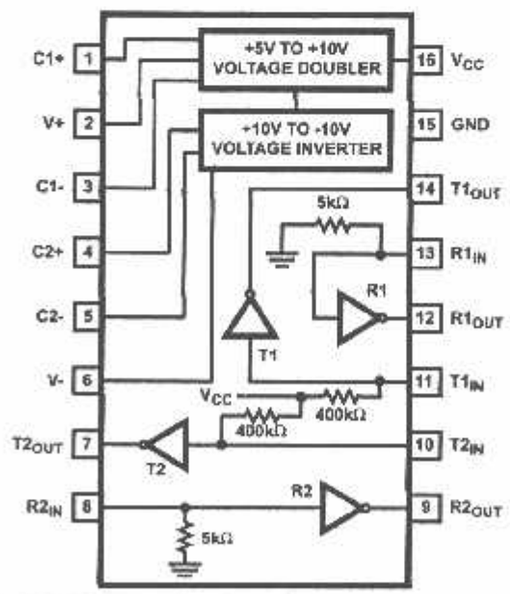
PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL232CPE	0°C to +70°C	16 Lead Plastic DIP
ICL232CJE	0°C to +70°C	16 Lead Ceramic DIP
ICL232CBE	0°C to +70°C	16 Lead SOIC (W)
ICL232IPE	-40°C to +85°C	16 Lead Plastic DIP
ICL232IJE	-40°C to +85°C	16 Lead Ceramic DIP
ICL232IBE	-40°C to +85°C	16 Lead SOIC (W)
ICL232MJE	-55°C to + 125°C	16 Lead Ceramic DIP

Pinouts

ICL232
(PDIP, CDIP, SOIC)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3020.2

Absolute Maximum Ratings

V_{CC} to Ground . . . . . (GND -0.3V) <V_{CC} < 6V
V- to Ground . . . . . (V_{CC} -0.3V) <V+ < 12V
V- to Ground . . . . . -12V < V- < (GND +0.3V)
Input Voltages
  $T1_{IN}$, $T2_{IN}$ . . . . . (V- -0.3V) < V_{IN} < (V+ +0.3V)
  $R1_{IN}$, $R2_{IN}$ . . . . . ±30V
Output Voltages
  $T1_{OUT}$, $T2_{OUT}$ . . . . . (V- -0.3V) < V_{TXOUT} < (V+ +0.3V)
  $R1_{OUT}$, $R2_{OUT}$ . . . . . (GND -0.3V) < V_{RXOUT} < (V_{CC} +0.3V)
Short Circuit Duration
  $T1_{OUT}$, $T2_{OUT}$ . . . . . Continuous
  $R1_{OUT}$, $R2_{OUT}$ . . . . . Continuous
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	80°C/W	24°C/W
Plastic DIP Package	100°C/W	-
SOIC Package	100°C/W	-

Maximum Power Dissipation 250mW
Operating Temperature Range
  ICL232C . . . . . 0°C to +70°C
  ICL232I . . . . . -40°C to +85°C
  ICL232M . . . . . -55°C to +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions: V_{CC} = +5V ±10%, T_A = Operating Temperature Range. Test Circuit as in Figure 8 Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Transmitter Output Voltage Swing, T_{OUT}	$T1_{OUT}$ and $T2_{OUT}$ loaded with 3kΩ to Ground	±5	±9	±10	V
Power Supply Current, I_{CC}	Outputs Unloaded, T_A = +25°C	-	5	10	mA
T_{IN}, Input Logic Low, V_{IL}		-	-	0.8	V
T_{IN}, Input Logic High, V_{IH}		2.0	-	-	V
Logic Pullup Current, I_P	$T1_{IN}$, $T2_{IN}$ = 0V	-	15	200	µA
RS-232 Input Voltage Range, V_{IN}		-30	-	+30	V
Receiver Input Impedance, R_{IN}	V_{IN} = ±3V	3.0	5.0	7.0	kΩ
Receiver Input Low Threshold, V_{IN} (H-L)	V_{CC} = 5.0V, T_A = +25°C	0.8	1.2	-	V
Receiver Input High Threshold, V_{IN} (L-H)	V_{CC} = 5.0V, T_A = +25°C	-	1.7	2.4	V
Receiver Input Hysteresis, V_{HYST}		0.2	0.5	1.0	V
TTL/CMOS Receiver Output Voltage Low, V_{OL}	I_{OUT} = 3.2mA	-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, V_{OH}	I_{OUT} = -1.0mA	3.5	4.6	-	V
Propagation Delay, t_{PD}	RS-232 to TTL	-	0.5	-	µs
Instantaneous Slew Rate, SR	C_L = 10pF, R_L = 3kΩ, T_A = +25°C (Notes 1, 2)	-	-	30	V/µs
Transition Region Slew Rate, SR_T	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or -3V to +3V	-	3	-	V/µs
Output Resistance, R_{OUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V	300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	$T1_{OUT}$ or $T2_{OUT}$ shorted to GND	-	±10	-	mA

NOTES:

1. Guaranteed by design.
2. See Figure 4 for definition.

Typical Performance Curves

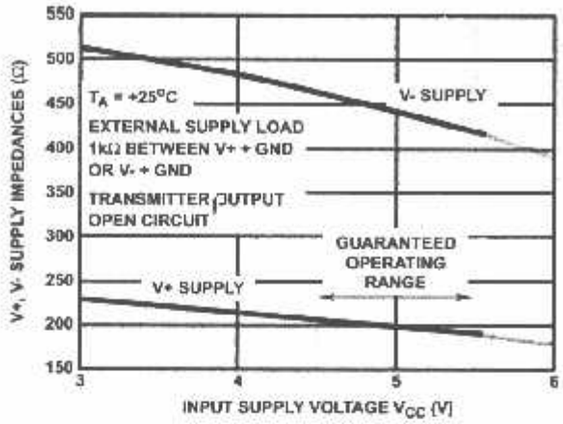


FIGURE 1. V+, V- OUTPUT IMPEDANCES vs V_{CC}

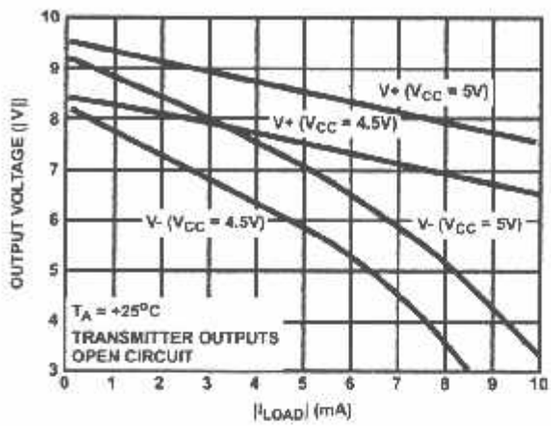


FIGURE 2. V+, V- OUTPUT VOLTAGES vs LOAD CURRENT

Pin Descriptions

PLASTIC DIP, CERAMIC DIP	SOIC	PIN NAME	DESCRIPTION
1	1	C1+	External capacitor "+" for internal voltage doubler.
2	2	V+	Internally generated +10V (typical) supply.
3	3	C1-	External capacitor "-" for internal voltage doubler.
4	4	C2+	External capacitor "+" internal voltage inverter.
5	5	C2-	External capacitor "-" internal voltage inverter.
6	6	V-	Internally generated -10V (typical) supply.
7	7	$T2_{OUT}$	RS-232 Transmitter 2 output ±10V (typical).
8	8	$R2_{IN}$	RS-232 Receiver 2 input, with internal 5K pulldown resistor to GND.
9	9	R2out	Receiver 2 TTL/CMOS output.
10	10	$T2_{IN}$	Transmitter 2 TTL/CMOS input, with internal 400K pullup resistor to V_{CC}.
11	11	$T1_{IN}$	Transmitter 1 TTL/CMOS input, with internal 400K pullup resistor to V_{CC}.
12	12	$R1_{OUT}$	Receiver 1 TTL/CMOS output.
13	13	$R1_{IN}$	RS-232 Receiver 1 input, with internal 5K pulldown resistor to GND.
14	14	$T1_{OUT}$	RS-232 Transmitter 1 output ±10V (typical).
15	15	GND	Supply Ground.
16	16	VCC	Positive Power Supply +5V ±10%

Detailed Description

The ICL232 is a dual RS-232 transmitter/receiver powered by a single +5V power supply which meets all EIA RS232C specifications and features low power consumption. The functional diagram illustrates the major elements of the ICL232. The circuit is divided into three sections: a voltage doubler/inverter, dual transmitters, and dual receivers.

Voltage Converter

An equivalent circuit of the dual charge pump is illustrated in Figure 3.

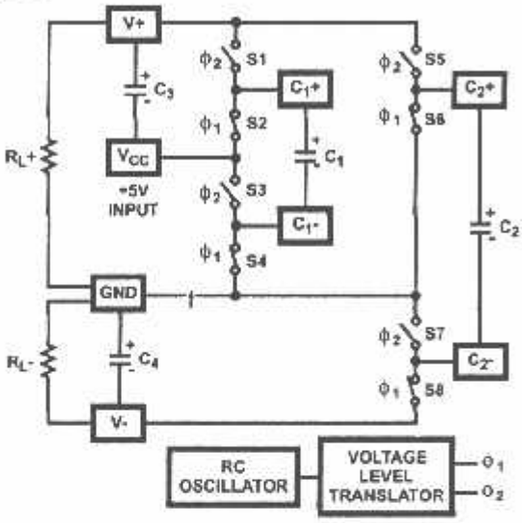
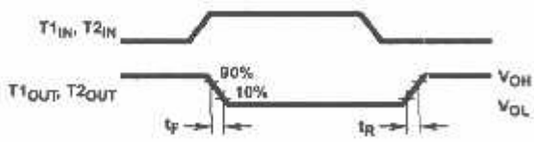


FIGURE 3. DUAL CHARGE PUMP

The voltage quadrupler contains two charge pumps which use two phases of an internally generated clock to generate +10V and -10V. The nominal clock frequency is 16kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C2 equal to twice V_{CC}. At the same time, C3 is also charged to $2V_{CC}$, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The voltage converter accepts input voltages up to 5.5V. The output impedance of the doubler (V+) is approximately 200Ω, and the output impedance of the inverter (V-) is approximately 450Ω. Typical graphs are presented which show the voltage converters output vs input voltage and output voltages vs load characteristics. The test circuit (Figure 8) uses 1µF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, and increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.



$$\text{Instantaneous Slew Rate (SR)} = \frac{(0.8)\,(V_{OH} - V_{OL})}{t_R} \text{ or } \frac{(0.8)\,(V_{OL} - V_{OH})}{t_F}$$

FIGURE 4. SLEW RATE DEFINITION

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ -0.6V). Each transmitter input has an internal 400kΩ pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specification of ±5V minimum with the worst case conditions of: both transmitters driving 3kΩ minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/µs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with ±2V applied to the outputs and V_{CC} = 0V.

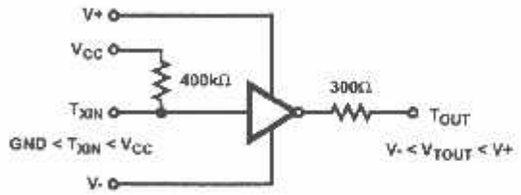


FIGURE 5. TRANSMITTER

Receivers

The receiver inputs accept up to ±30V while presenting the required 3kΩ to 7kΩ input impedance even it the power is off (V_{CC} = 0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specification. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis to improve noise rejection.

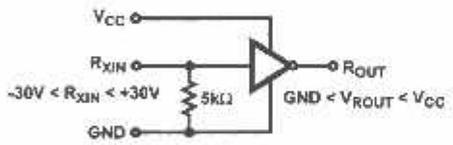
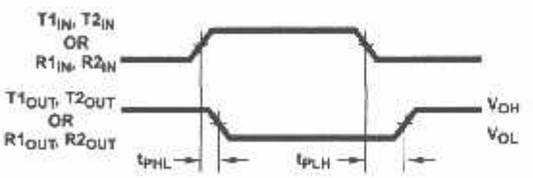


FIGURE 6. RECEIVER



$$\text{Average Propagation Delay} = \frac{t_{PHL} + t_{PLH}}{2}$$

FIGURE 7. PROPAGATION DELAY DEFINITION

Test Circuits

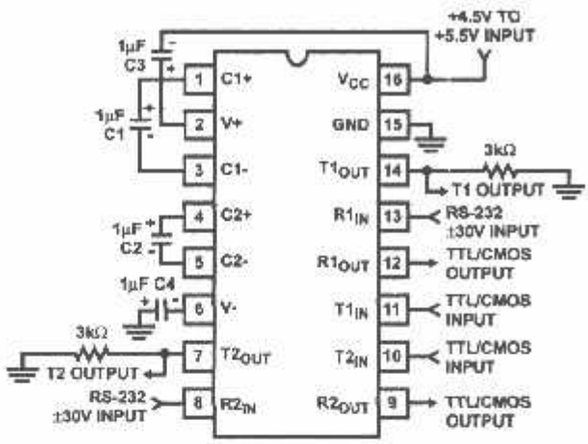


FIGURE 8. GENERAL TEST CIRCUIT

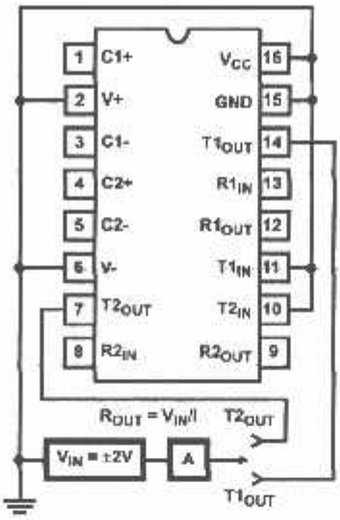


FIGURE 9. POWER-OFF SOURCE RESISTANCE CONFIGURATION

Applications

The ICL232 may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 10. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

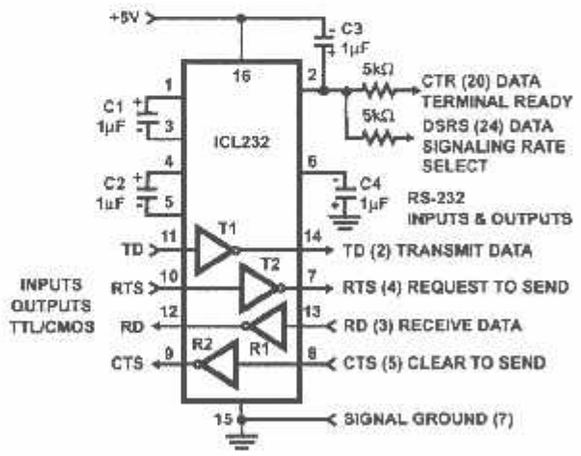


FIGURE 10. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

In applications requiring four RS-232 inputs and outputs (Figure 11), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

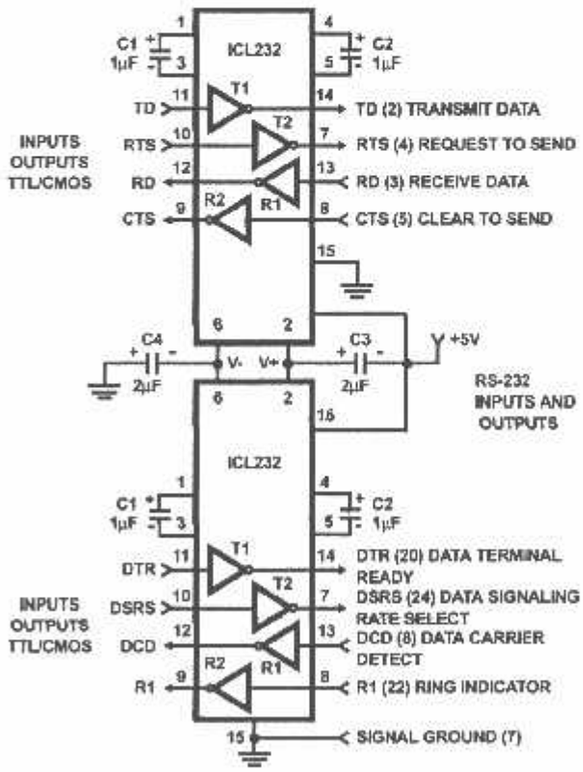


FIGURE 11. COMBINING TWO ICL232s FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

National Semiconductor

February 1996

DS75176B/DS75176BT
Multipoint RS-485/RS-422 Transceivers

General Description

The DS75176B is a high speed differential TRI-STATE® bus/line transceiver designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission. In addition, it is compatible with RS-422.

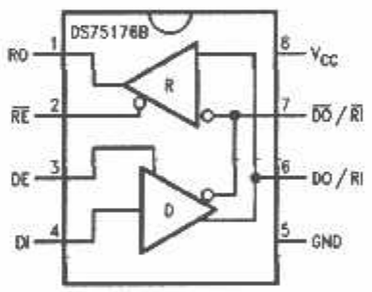
The driver and receiver outputs feature TRI-STATE capability, for the driver outputs over the entire common mode range of +12V to −7V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state.

DC specifications are guaranteed over the 0 to 70°C temperature and 4.75V to 5.25V supply voltage range.

Features

- Meets EIA standard RS485 for multipoint bus transmission and is compatible with RS-422.
- Small Outline (SO) Package option available for minimum board space.
- 22 ns driver propagation delays.
- Single +5V supply.
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus.
- Thermal shutdown protection.
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down.
- Pin out compatible with DS3695/A and SN75176A/B.
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus.
- 70 mV typical receiver hysteresis.

Connection and Logic Diagram



TL/F/8759–1

Top View

Order Number DS75176BN, DS75176BTN, DS75176BM or DS75176BTM
See NS Package Number N08E or M08A

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Control Input Voltages	7V
Driver Input Voltage	7V
Driver Output Voltages	+15V/ −10V
Receiver Input Voltages (DS75176B)	+15V/ −10V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @25°C	
for M Package	675 mW (Note 5)
for N Package	900 mW (Note 4)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Voltage at Any Bus Terminal (Separate or Common Mode)	−7	+12	V
Operating Free Air Temperature T_A			
DS75176B	0	+70	°C
DS75176BT	−40	+85	°C
Differential Input Voltage, VID (Note 6)	−12	+12	V

Electrical Characteristics (Notes 2 and 3)

0°C ≤ T_A ≤ 70°C, 4.75V < V_{CC} < 5.25V unless otherwise specified

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage (Unloaded)		I_O = 0				5	V
V_{OD2}	Differential Driver Output Voltage (with Load)		*(Figure 1)*	R = 50Ω; (RS-422) (Note 7)	2			V
				R = 27Ω; (RS-485)	1.5			V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage For Complementary Output States		*(Figure 1)*	R = 27Ω			0.2	V
V_{OC}	Driver Common Mode Output Voltage						3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage For Complementary Output States						0.2	V
V_{IH}	Input High Voltage	DI, DE, $\overline{RE}$, E			2			V
V_{IL}	Input Low Voltage						0.8	
V_{CL}	Input Clamp Voltage			I_{IN} = −18 mA			−1.5	
I_{IL}	Input Low Current			V_{IL} = 0.4V			−200	μA
I_{IH}	Input High Current			V_{IH} = 2.4V			20	μA
I_{IN}	Input Current	DO/RI, DO/RI	V_{CC} = 0V or 5.25V, DE = 0V	V_{IN} = 12V			+1.0	mA
				V_{IN} = −7V			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver		−7V ≤ V_{CM} ≤ +12V		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis		V_{CM} = 0V			70		mV
V_{OH}	Receiver Output High Voltage		I_{OH} = −400 μA		2.7			V
V_{OL}	Output Low Voltage	RO	I_{OL} = 16 mA (Note 7)				0.5	V
I_{OZR}	OFF-State (High Impedance) Output Current at Receiver		V_{CC} = Max, 0.4V ≤ V_O ≤ 2.4V				+20	μA
R_{IN}	Receiver Input Resistance		−7V ≤ V_{CM} ≤ +12V		12			kΩ
I_{CC}	Supply Current		No Load (Note 7)	Driver Outputs Enabled			55	mA
				Driver Outputs Disabled			35	mA

Electrical Characteristics (Notes 2 and 3)

$0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OSD}	Driver Short-Circuit Output Current	$V_O = -7V$ (Note 7)			−250	mA
		$V_O = +12V$ (Note 7)			+250	mA
I_{OSR}	Receiver Short-Circuit Output Current	$V_O = 0V$	−15		−85	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 4: Derate linearly at 5.56 mW/°C to 650 mW at 70°C.

Note 5: Derate linearly @ 6.11 mW/°C to 400 mW at 70°C.

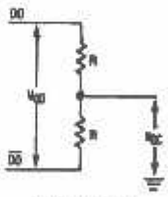
Note 6: Differential - Input/Output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

Note 7: All worst case parameters for which note 7 is applied, must be increased by 10% for DS75176BT. The other parameters remain valid for $-40°C < T_A < +85°C$.

Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$

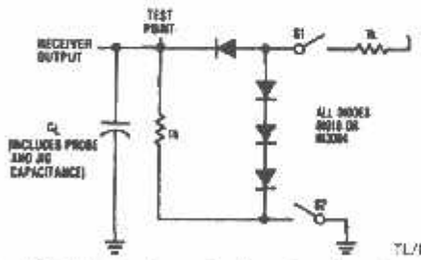
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Driver Input to Output	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF		12	22	ns
t_{PHL}	Driver Input to Output			17	22	ns
t_r	Driver Rise Time	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF *(Figures 3 and 5)*			18	ns
t_f	Driver Fall Time				18	ns
t_{ZH}	Driver Enable to Output High	$C_L = 100$ pF *(Figures 4 and 6)* S1 Open		29	100	ns
t_{ZL}	Driver Enable to Output Low	$C_L = 100$ pF *(Figures 4 and 6)* S2 Open		31	60	ns
t_{LZ}	Driver Disable Time from Low	$C_L = 15$ pF *(Figures 4 and 6)* S2 Open		13	30	ns
t_{HZ}	Driver Disable Time from High	$C_L = 15$ pF *(Figures 4 and 6)* S1 Open		19	200	ns
t_{PLH}	Receiver Input to Output	$C_L = 15$ pF *(Figures 2 and 7)* S1 and S2 Closed		30	37	ns
t_{PHL}	Receiver Input to Output			32	37	ns
t_{ZL}	Receiver Enable to Output Low	$C_L = 15$ pF *(Figures 2 and 8)* S2 Open		15	20	ns
t_{ZH}	Receiver Enable to Output High	$C_L = 15$ pF *(Figures 2 and 8)* S1 Open		11	20	ns
t_{LZ}	Receiver Disable from Low	$C_L = 15$ pF *(Figures 2 and 8)* S2 Open		28	32	ns
t_{HZ}	Receiver Disable from High	$C_L = 15$ pF *(Figures 2 and 8)* S1 Open		13	35	ns

AC Test Circuits



TL/F/8759–2

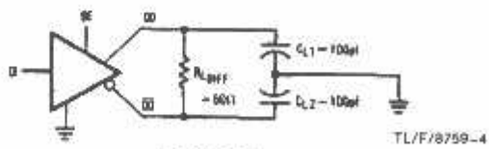
FIGURE 1



TL/F/8759–3

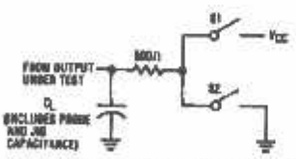
Note: S1 and S2 of load circuit are closed except as otherwise mentioned.

FIGURE 2



TL/F/8759–4

FIGURE 3

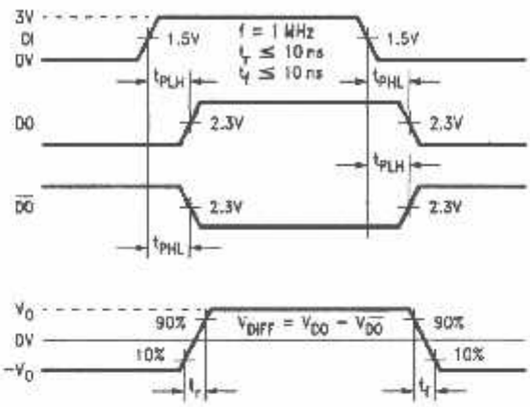


TL/F/8759–5

Note: Unless otherwise specified the switches are closed.

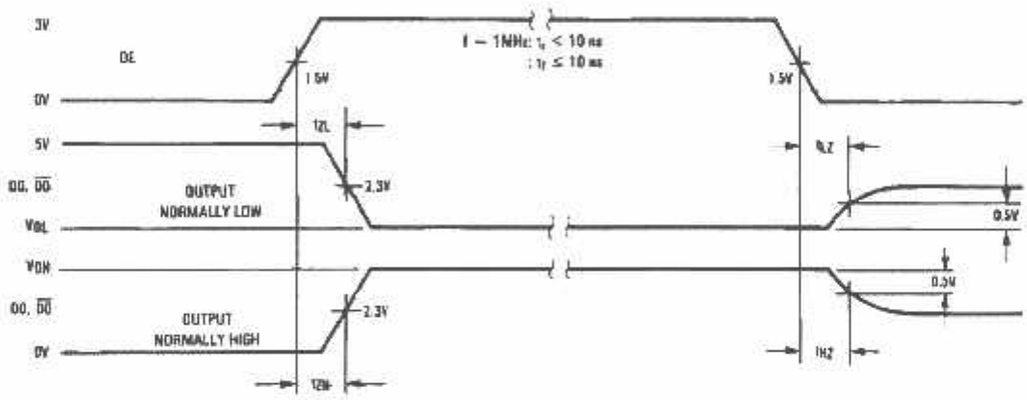
FIGURE 4

Switching Time Waveforms



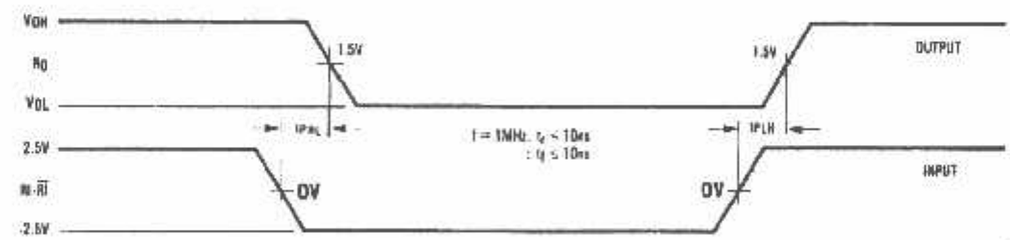
TL/F/8759–6

FIGURE 5. Driver Propagation Delays and Transition Times



TL/F/8759–7

FIGURE 6. Driver Enable and Disable Times

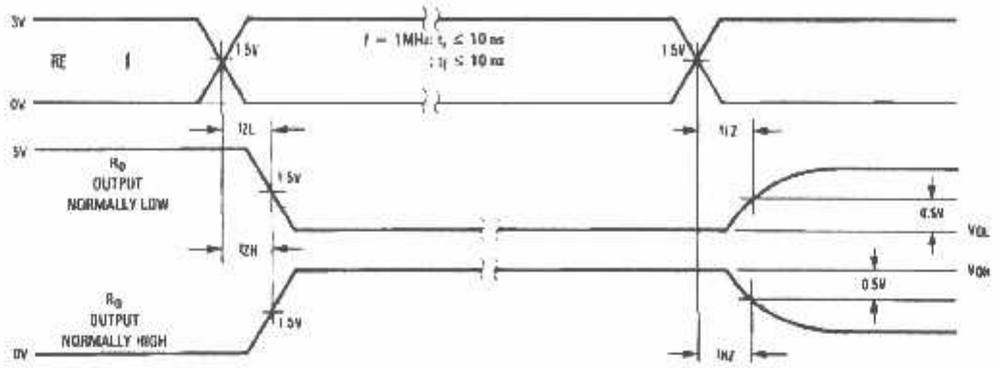


TL/F/8759–8

Note: Differential input voltage may may be realized by grounding $\overline{RI}$ and pulsing RI between +2.5V and −2.5V

FIGURE 7. Receiver Propagation Delays

Switching Time Waveforms (Continued)



TL/F/8759–9

FIGURE 8. Receiver Enable and Disable Times

Function Tables

DS75176B Transmitting

Inputs			Line Condition	Outputs	
$\overline{RE}$	DE	DI		$\overline{DO}$	DO
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

DS75176B Receiving

Inputs			Outputs
$\overline{RE}$	DE	RI-$\overline{RI}$	RO
0	0	≥ +0.2V	1
0	0	≤ −0.2V	0
0	0	Inputs Open**	1
1	0	X	Z

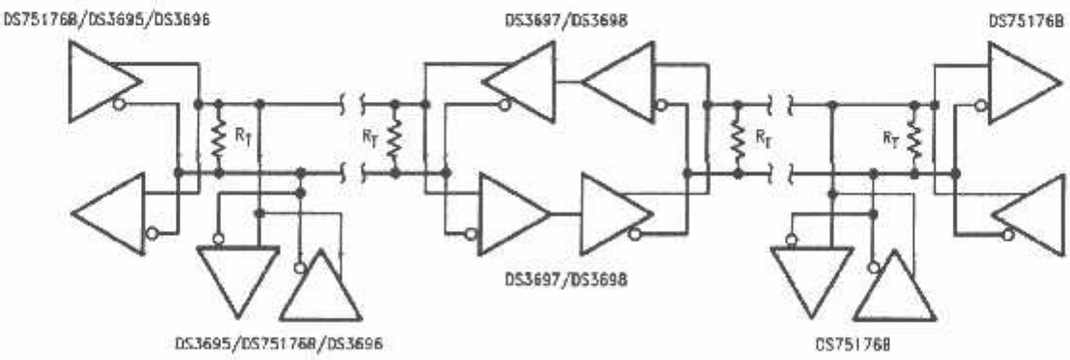
X — Don't care condition

Z — High impedance state

Fault — Improper line conditions causing excessive power dissipation in the driver, such as shorts or bus contention situations

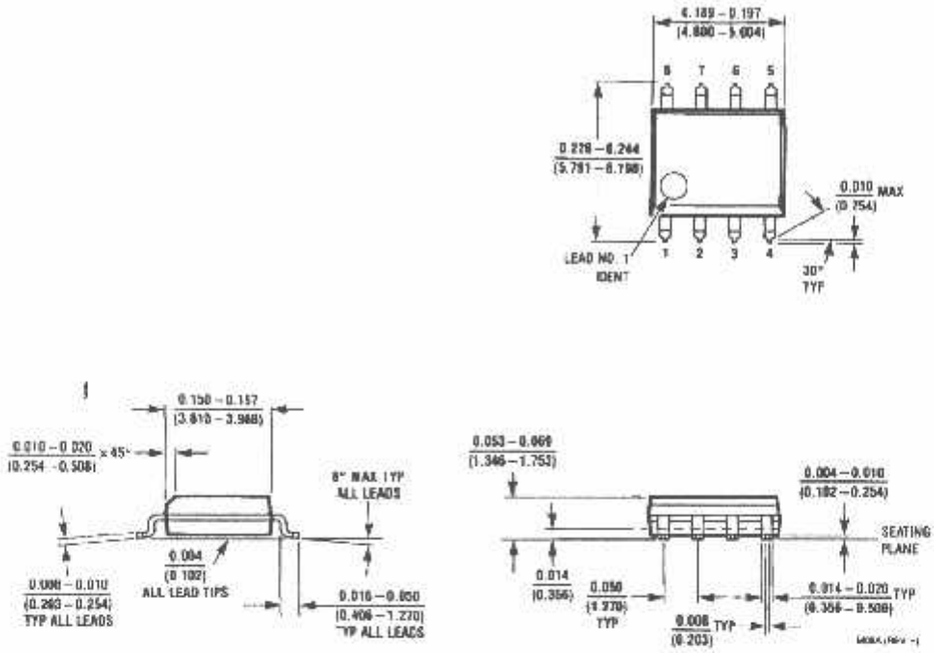
**This is a fail safe condition

Typical Application



TL/F/8759–11

Physical Dimensions inches (millimeters)



Small Outline Package (M)
Order Number DS75176BM or DS75176BTM
NS Package Number M08A

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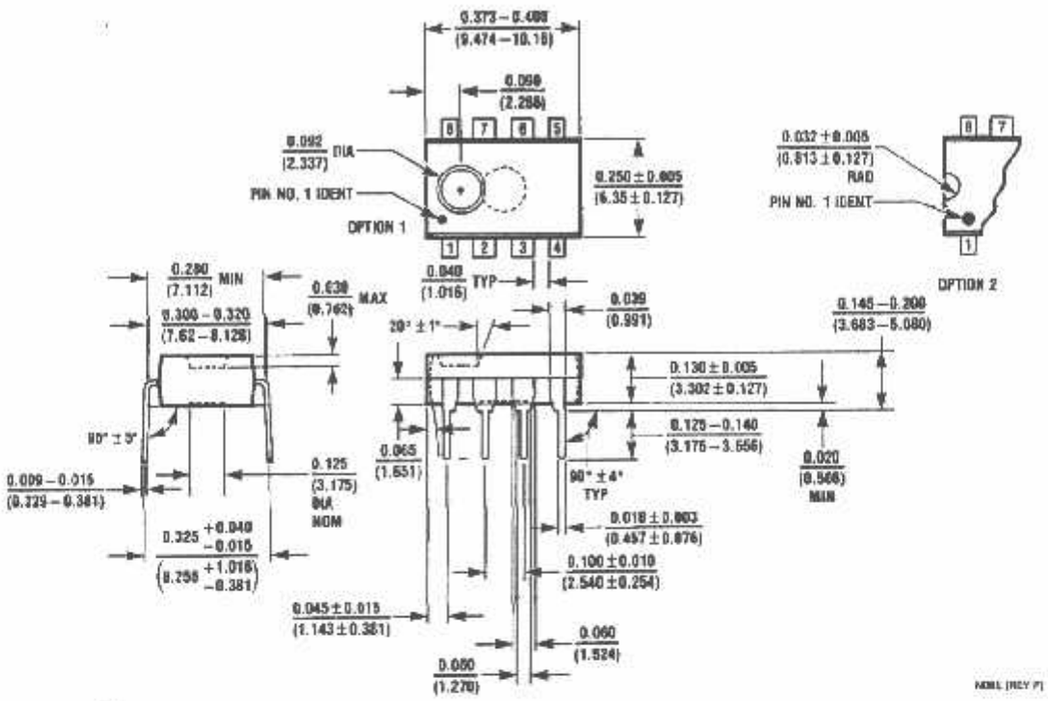
Physical Dimensions inches (millimeters) (Continued)

Lit. # 103669



Molded Dual-In-Line Package (N)
Order Number DS75176BN or DS75176BTN
NS Package Number N08E

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National Semiconductor

December 1994

LM158/LM258/LM358/LM2904
Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

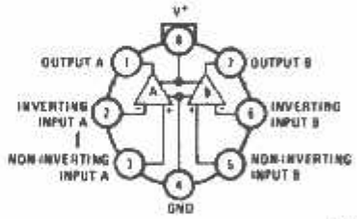
- Two internally compensated op amps in a single package
- Eliminates need for dual supplies
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply 3V to 32V
  - or dual supplies ±1.5V to ±16V
- Very low supply current drain (500 μA)—essentially independent of supply voltage
- Low input offset voltage 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V+ − 1.5V

Connection Diagrams (Top Views)

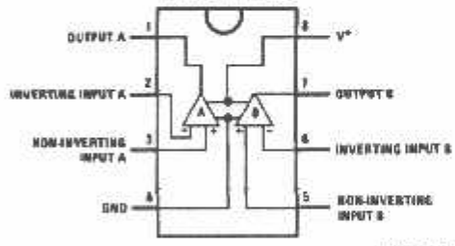
Metal Can Package



TL/H/7787–1

Order Number LM158AH, LM158AH/883*, LM158H, LM158H/883*, LM258H or LM358H
See NS Package Number H08C

DIP/SO Package



TL/H/7787–2

Order Number LM158J, LM158J/883*, LM158AJ or LM158AJ/883*
See NS Package Number J08A
Order Number LM358M, LM358AM or LM2904M
See NS Package Number M08A
Order Number LM358AN, LM358N or LM2904N
See NS Package Number N08E

*LM158 is available per SMD #5962-8771001
LM158A is available per SMD #5962-8771002

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 1)		
Molded DIP	830 mW	830 mW
Metal Can	550 mW	
Small Outline Package (M)	530 mW	530 mW
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15V$ and $T_A = 25°C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3V$) (Note 3)	50 mA	50 mA

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Operating Temperature Range		
LM358	0°C to +70°C	−40°C to +85°C
LM258	−25°C to +85°C	
LM158	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature, DIP (Soldering, 10 seconds)	260°C	260°C
Lead Temperature, Metal Can (Soldering, 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics $V^+ = +5.0V$, unless otherwise stated

Parameter	Conditions	LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 5), $T_A = 25°C$		1	2		2	3		2	5		2	7		2	7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$, $V_{CM} = 0V$, (Note 6)		20	50		45	100		45	150		45	250		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		2	10		5	30		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range	$V^+ = 30V$, (Note 7) (LM2904, $V^+ = 26V$), $T_A = 25°C$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps $V^+ = 30V$ (LM2904 $V^+ = 26V$) $V^+ = 5V$		1 0.5	2 1.2		1 0.5	2 1.2		1 0.5	2 1.2		1 0.5	2 1.2		1 0.5	2 1.2	mA mA

Electrical Characteristics (Continued) $V^+ = +5.0V$, Note 4, unless otherwise stated

Parameter		Conditions	LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		$V^+ = 15V$, $T_A = 25°C$, $R_L \geq 2 k\Omega$, (For $V_O = 1V$ to 11V)	50	100		25	100		50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio		$T_A = 25°C$, $V_{CM} = 0V$ to $V^+ - 1.5V$	70	85		65	85		70	85		65	85		50	70		dB
Power Supply Rejection Ratio		$V^+ = 5V$ to 30V (LM2904, $V^+ = 5V$ to 26V), $T_A = 25°C$	65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling		$f = 1$ kHz to 20 kHz, $T_A = 25°C$ (Input Referred), (Note 8)		−120			−120			−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		mA
	Sink	$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $T_A = 25°C$, $V_O = 2V$	10	20		10	20		10	20		10	20		10	20		mA
		$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $T_A = 25°C$, $V_O = 200$ mV, $V^+ = 15V$	12	50		12	50		12	50		12	50		12	50		µA
Short Circuit to Ground		$T_A = 25°C$, (Note 2), $V^+ = 15V$		40	60		40	60		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 5)			4			5			7			9			10	mV
Input Offset Voltage Drift		$R_S = 0\Omega$		7	15		7	20		7			7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			30			75			100			150		45	200	nA
Input Offset Current Drift		$R_S = 0\Omega$		10	200		10	300		10			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	200		40	300		40	500		40	500	nA

Electrical Characteristics (Continued) $V^+ = +5.0V$, Note 4, unless otherwise stated

Parameter		Conditions		LM158A			LM358A			LM158/LM258			LM358			LM2904			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Common-Mode Voltage Range		$V^+ = 30$ V, (Note 7) (LM2904, $V^+ = 26V$)		0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V
Large Signal Voltage Gain		$V^+ = +15V$ ($V_O = 1V$ to 11V) $R_L \geq 2 k\Omega$		25			15			25			15			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = +30V$ (LM2904, $V^+ = 26V$)	$R_L = 2 k\Omega$	26			26			26			26			22			V
			$R_L = 10 k\Omega$	27	28		27	28		27	28		27	28		23	24		V
	V_{OL}	$V^+ = 5V$, $R_L = 10 k\Omega$			5	20		5	20		5	20		5	20		5	100	mV
Output Current	Source	$V_{IN}^+ = +1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$		10	20		10	20		10	20		10	20		10	20		mA
	Sink	$V_{IN}^- = +1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 2V$		10	15		5	8		5	8		5	8		5	8		mA

Note 1: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 120°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$ for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM358/LM358A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2904 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O = 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$) at 25°C. For LM2904, V^+ from 5V to 26V.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2904), independent of the magnitude of V^+.

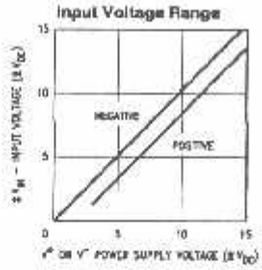
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

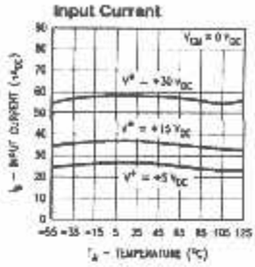
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

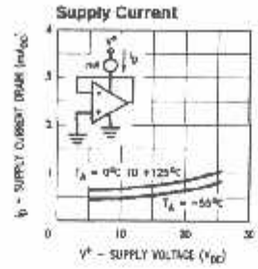
Input Voltage Range



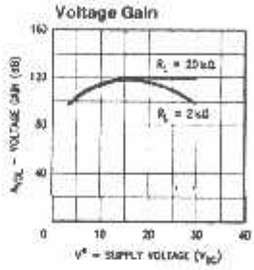
Input Current



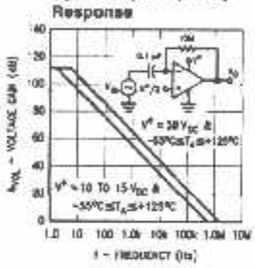
Supply Current



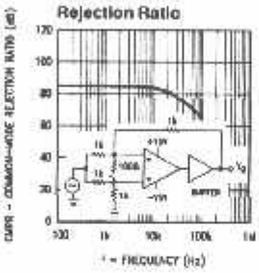
Voltage Gain



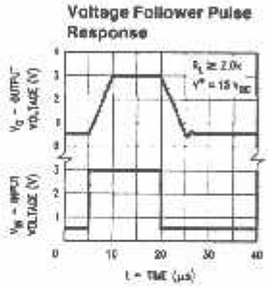
Open Loop Frequency Response



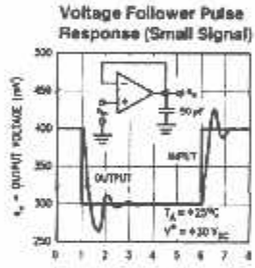
Common-Mode Rejection Ratio



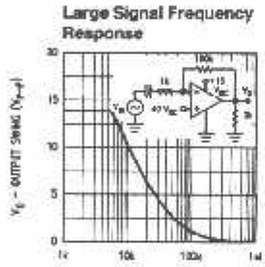
Voltage Follower Pulse Response



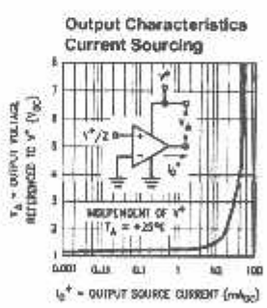
Voltage Follower Pulse Response (Small Signal)



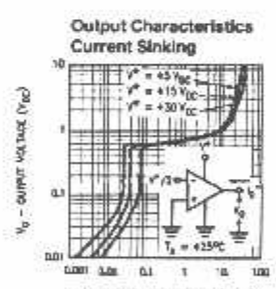
Large Signal Frequency Response



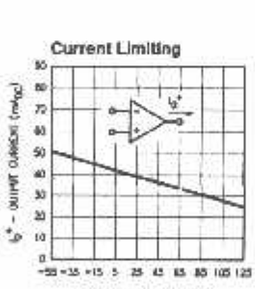
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



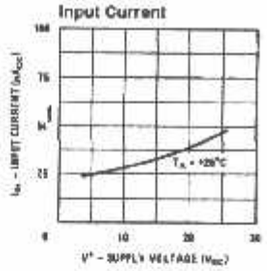
Current Limiting



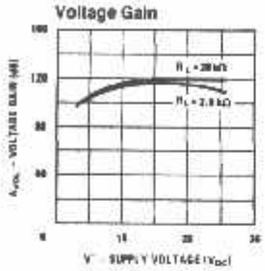
TL/H/7787–4

Typical Performance Characteristics (Continued) (LM2902 only)

Input Current



Voltage Gain



TL/H/7787–5

Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accomodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accomodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

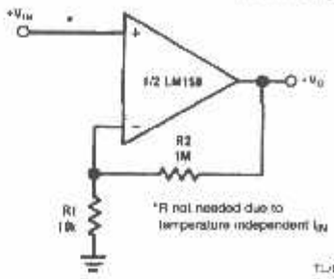
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

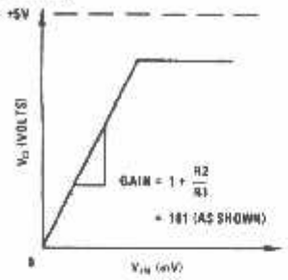
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^- = 5.0\ V_{DC}$)

Non-Inverting DC Gain (0V Input = 0V Output)

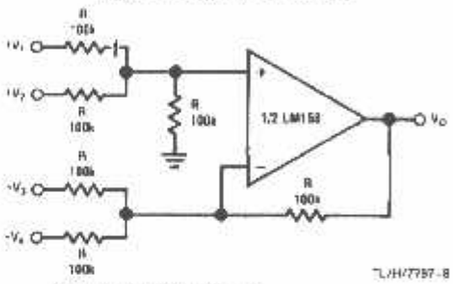


TL/H/7787–6



TL/H/7787–7

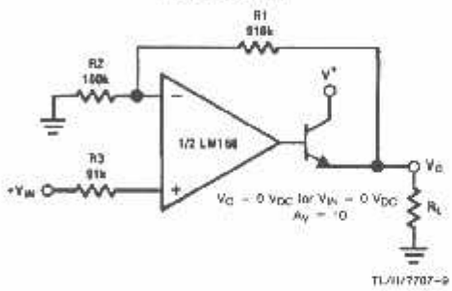
DC Summing Amplifier
(V_{IN}'S ≥ 0 V_{DC} and V_O ≥ 0 V_{DC})



TL/H/7787–8

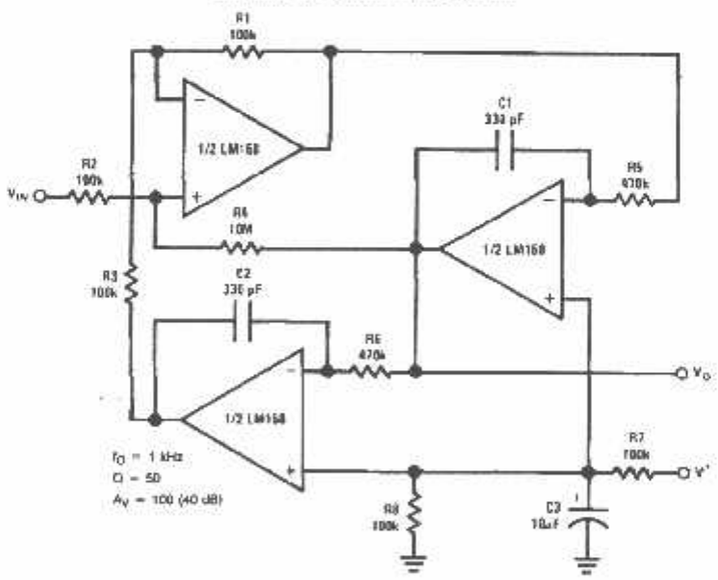
Where $V_O = V_1 + V_2 + V_3 + V_4$
$(V_1 + V_2) > (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Power Amplifier



TL/H/7787–9

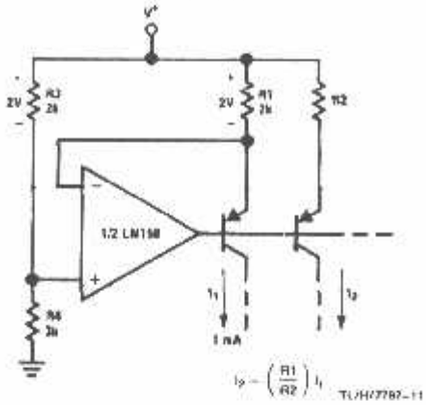
"Bi-QUAD" RC Active Bandpass Filter



TL/H/7787–10

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

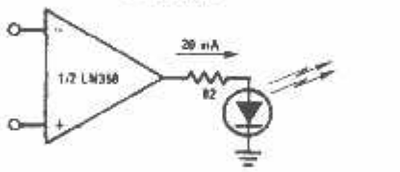
Fixed Current Sources



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

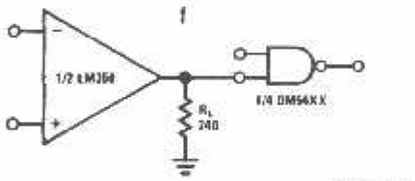
TL/H/7787–11

LED Driver



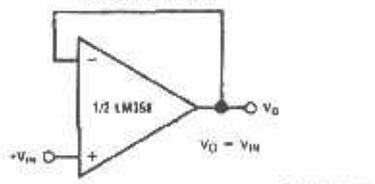
TL/H/7787–13

Driving TTL



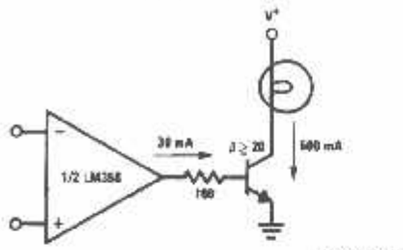
TL/H/7787–15

Voltage Follower



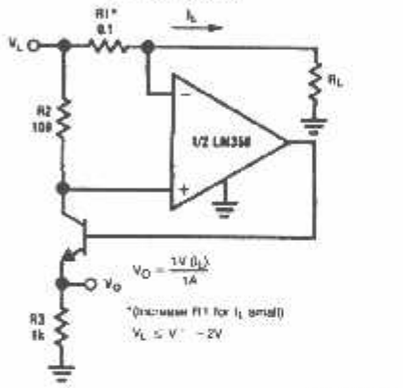
TL/H/7787–17

Lamp Driver



TL/H/7787–12

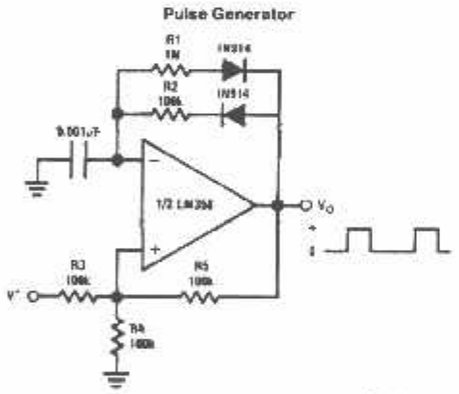
Current Monitor



$$V_O = \frac{1V\ (I_L)}{1A}$$

TL/H/7787–14

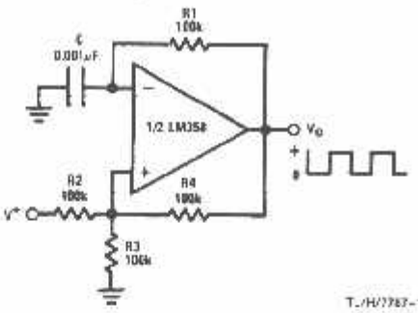
Pulse Generator



TL/H/7787–16

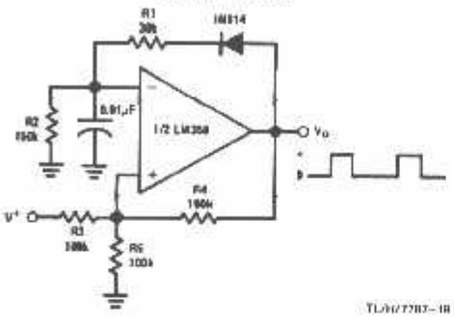
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Squarewave Oscillator



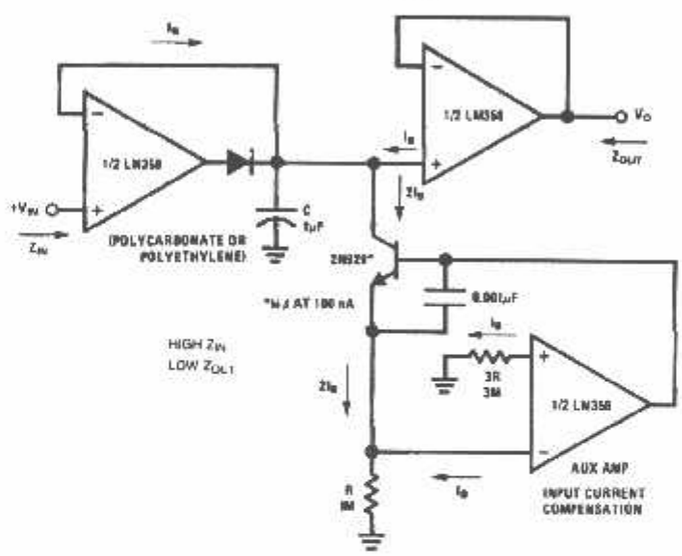
TL/H/7787–18

Pulse Generator



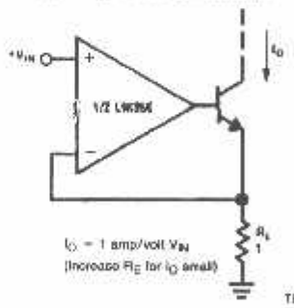
TL/H/7787–19

Low Drift Peak Detector



TL/H/7787–20

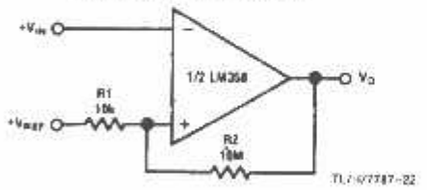
High Compliance Current Sink



I_O = 1 amp/volt V_{IN}
(Increase R_E for I_O small)

TL/H/7787–21

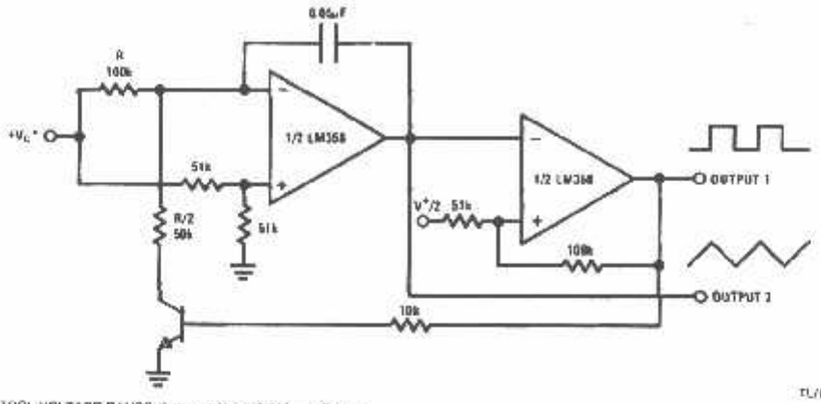
Comparator with Hysteresis



TL/H/7787–22

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

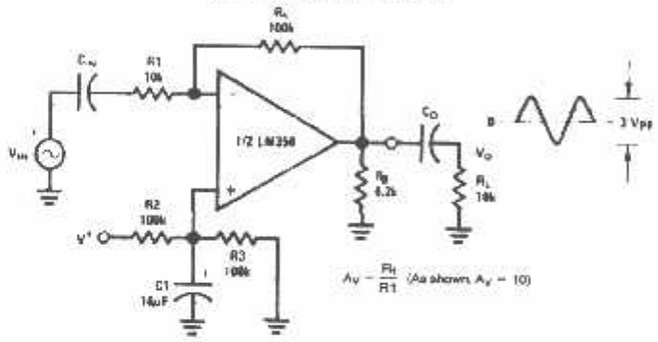
Voltage Controlled Oscillator (VCO)



TL/H/7787–23

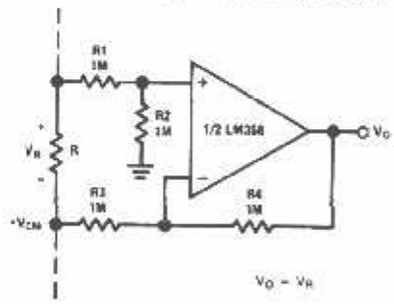
*WIDE CONTROL VOLTAGE RANGE: $0\ V_{DC} \leq V_C \leq 2\ (V^+ - 1.5V)_{DC}$

AC Coupled Inverting Amplifier



TL/H/7787–24

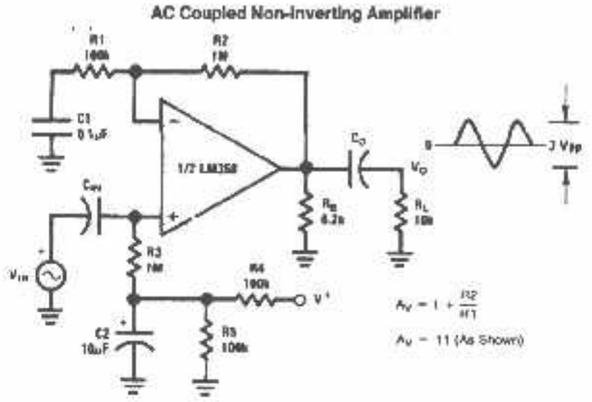
Ground Referencing a Differential Input Signal



TL/H/7787–25

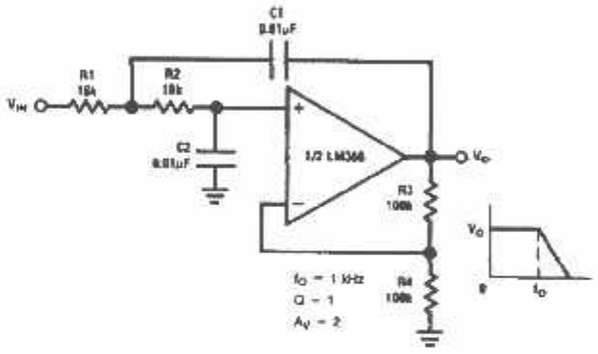
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

AC Coupled Non-Inverting Amplifier



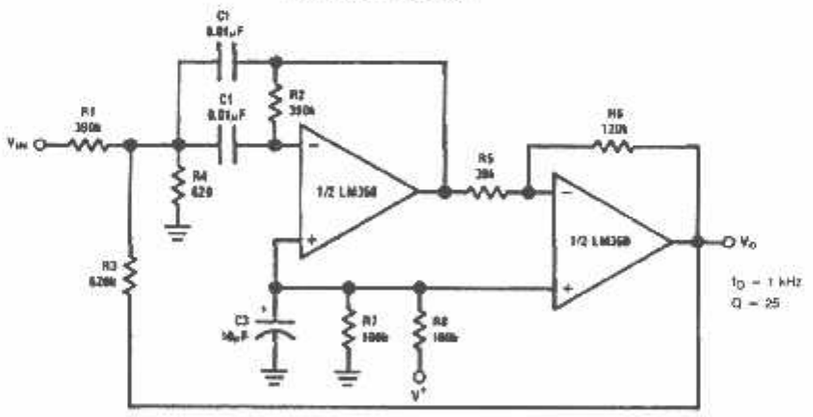
TL/H/7787–26

DC Coupled Low-Pass RC Active Filter



TL/H/7787–27

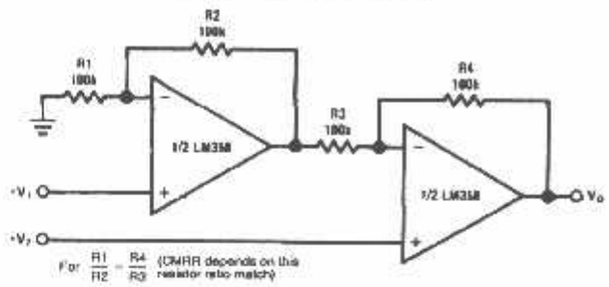
Bandpass Active Filter



TL/H/7787–28

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

High Input Z, DC Differential Amplifier



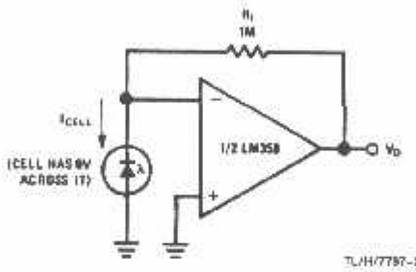
For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

TL/H/7787–29

$$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$$

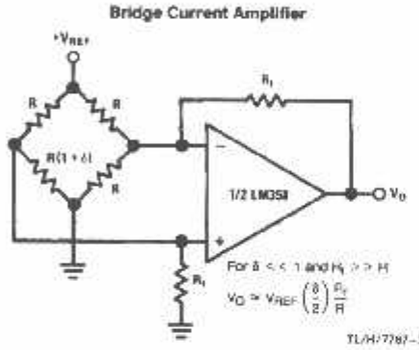
As Shown $V_O = 2(V_2 - V_1)$

Photo Voltaic-Cell Amplifier



TL/H/7787–30

Bridge Current Amplifier

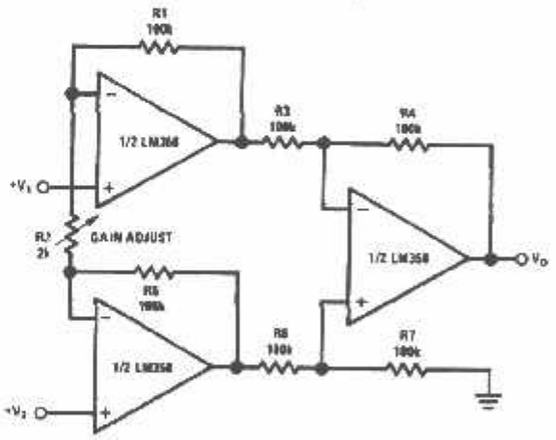


For $\delta << 1$ and $R_1 >> R$

$$V_O \approx V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

TL/H/7787–33

High Input Z Adjustable-Gain DC Instrumentation Amplifier



TL/H/7787–31

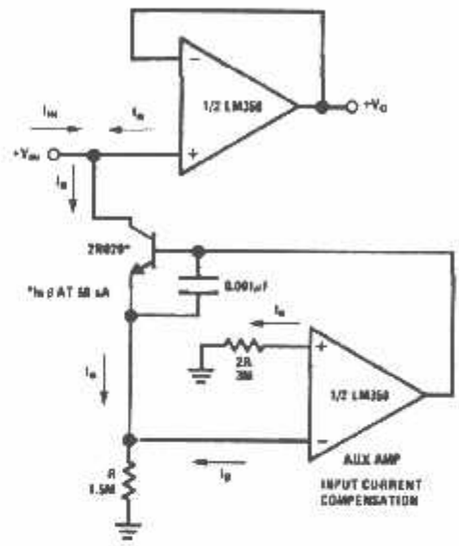
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101(V_2 - V_1)$

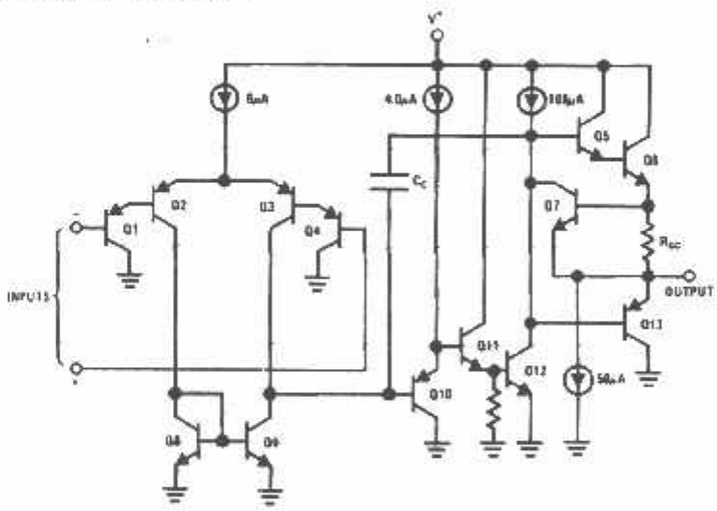
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



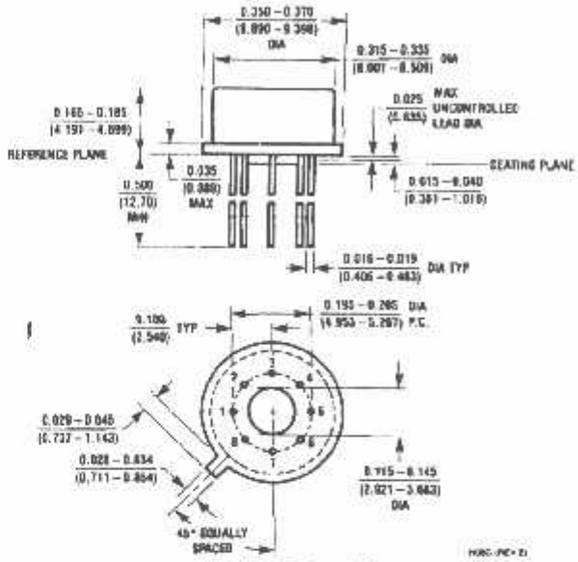
TL/H/7787–32

Schematic Diagram (Each Amplifier)



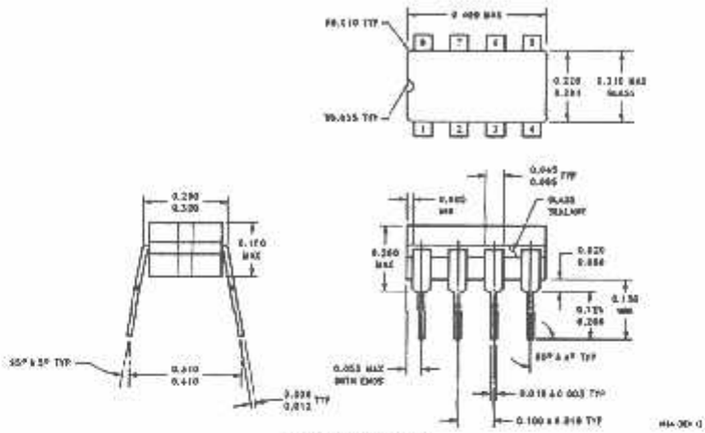
TL/H/7787–3

Physical Dimensions inches (millimeters)

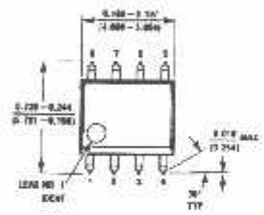


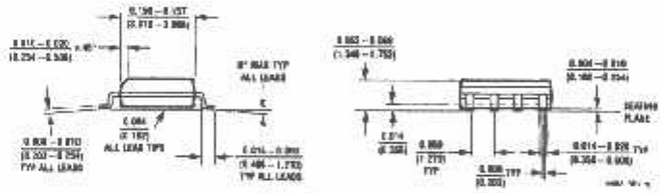
Metal Can Package (H)
Order Number LM158AH, LM158AH/883, LM158H, LM158H/883, LM258H or LM358H
NS Package Number H08C

Physical Dimensions inches (millimeters) (Continued)



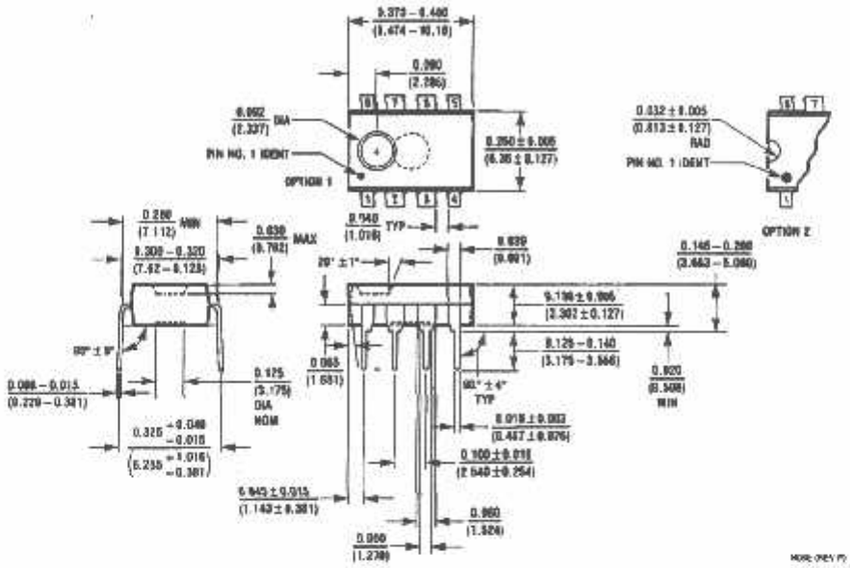
Cerdip Package (J)
Order Number LM158J, LM158J/883, LM158AJ or LM158AJ/883
NS Package Number J08A





S.O. Package (M)
Order Number LM358M, LM358AM or LM2904M
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dip Package (N)
Order Number LM358AN, LM358N or LM2904N
NS Package Number N08E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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