

SKRIPSI

PERANCANGAN DAN PEMBUATAN SISTEM ANTRIAN NASABAH BANK BERBASIS PERSONAL COMPUTER MENGUNAKAN RS-485



Disusun Oleh :
AGUS ADI WIRAWAN
95.17.008



JURUSAN TEKNIK ELEKTRO S -1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
SEPTEMBER 2008

LEMBAR PERSETUJUAN



PERANCANGAN DAN PEMBUATAN SISTEM ANTRIAN NASABAH BANK BERBASIS PERSONAL COMPUTER MENGGUNAKAN RS-485

SKRIPSI

*Disusun dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh
Gelar Sarjana Teknik Elektro Strata Satu (S-1)*

Disusun Oleh :

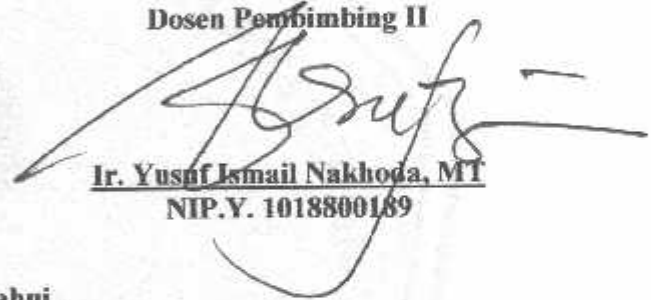
AGUS ADI WIRAWAN
95.17.008

Diperiksa dan Disetujui

Dosen Pembimbing I


Ir. F. Yudi Limpraptono, MT
NIP.Y. 1039500274

Dosen Pembimbing II


Ir. Yusuf Ismail Nakhoda, MT
NIP.Y. 1018800189

Mengetahui,



Ketua Jurusan Teknik Elektro S-1


Ir. F. YUDI LIMPRAPTONO, MT
NIP.Y. 1039500274

**JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG
SEPTEMBER 2008**



INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

**BERITA ACARA UJIAN SKRIPSI
FAKULTAS TEKNOLOGI INDUSTRI**

NAMA : AGUS ADI WIRAWAN
NIM : 95.17.008
JURUSAN : TEKNIK ELEKTRO S-1
KONSENTRASI : TEKNIK ELEKTRONIKA
JUDUL SKRIPSI : PERANCANGAN DAN PEMBUATAN
SISTEM ANTRIAN NASABAH BANK BERBASIS
PERSONAL COMPUTER MENGGUNAKAN RS-485

Dipertahankan dihadapan Tim Penguji Skripsi Jenjang Strata Satu pada :

Hari : Selasa
Tanggal : 23 September 2008
Dengan Nilai : 83,05 (A) *Ref*

Panitia Ujian Skripsi



Ketua

Ir. Mochtar Asroni, MSME
NIP.Y.1018100036

Sekretaris

Ir. F. Yudi Limpraptono, MT
NIP.Y.1039500274

Anggota Penguji

Penguji I

I Komang Somawirata, ST. MT
NIP.Y. 1030100361

Penguji II

Irmalia Suryani Faradisa, ST. MT
NIP.Y. 1030100365



INSTITUT TEKNOLOGI NASIONAL MALANG
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI TEKNIK ELEKTRONIKA

LEMBAR PERBAIKAN SKRIPSI

Dalam pelaksanaan Ujian Skripsi Jenjang Strata Satu Jurusan Teknik Elektro Konsentrasi Teknik Elektronika perlu adanya perbaikan untuk mahasiswa :

NAMA : AGUS ADI WIRAWAN
NIM : 95.17.008
JURUSAN : TEKNIK ELEKTRO S-1
KONSENTRASI : TEKNIK ELEKTRONIKA
JUDUL SKRIPSI : PERANCANGAN DAN PEMBUATAN
SISTEM ANTRIAN NASABAH BANK BERBASIS
PERSONAL COMPUTER MENGGUNAKAN RS-485

No	Tanggal	Uraian	Paraf
1	23 September 2008	Jelaskan maksud gambar foto oscilloscope.	

Diperiksa dan Disetujui,

Dosen Penguji I

I Komang Somawirata, ST. MT
NIP.Y. 1030100361

Dosen Penguji II

Irmalia Suryani Faradisa, ST. MT
NIP. Y. 1030100365

Mengetahui,

Dosen Pembimbing I

Ir. F. Yudi Limpraptono, MT
NIP.Y 1039500274

Dosen Pembimbing II

Ir. Yusuf Ismail Nakhoda, MT
NIP.Y. 1018800189

ABSTRAKSI

PERANCANGAN DAN PEMBUATAN SISTEM ANTRIAN NASABAH BANK BERBASIS PERSONAL COMPUTER MENGGUNAKAN RS-485

Agus Adi Wirawan
95.17.008

Jurusan Teknik Elektro S1 – Institut Teknologi Nasional Malang
Jln. Raya Karanglo Km 2 Malang

Dosen Pembimbing : **Ir. F. Yudi Limpraptono, MT**
Ir. Yusuf Ismail Nakhoda, MT

Kata Kunci : Sistem Antrian, RS-485, AT89S51, Personal Computer.

Dalam dunia perbankan yang sangat sensitif terhadap tingkat keamanan dan kenyamanan pelayanan terhadap nasabahnya, maka diperlukan suatu teknologi yang sebaik mungkin yang dapat menjamin kenyamanan nasabah dalam melakukan setiap transaksi. Dalam melakukan transaksi tersebut, terkadang para nasabah harus rela antri dengan cara berdiri yang terkadang bisa saja antrian itu berlangsung lama hingga berjam-jam. Hal ini tentu saja sangat merepotkan dan melelahkan bagi para nasabah. Oleh karenanya diperlukan sistem antrian yang lebih baik untuk para nasabah agar para nasabah lebih nyaman dalam melakukan setiap aktivitas transaksinya. Nasabah hanya perlu mendengarkan informasi lewat suara atau melihatnya pada layar monitor. Dalam sistem ini antrian akan diatur secara otomatis menggunakan Personal Computer dan Mikrokontroler AT89S51 serta menggunakan komunikasi RS-485.

KATA PENGANTAR

Segala Puji dihadapan Ida Sang Hyang Widhi Wasa atas waranugraha-Nya sehingga penyusun dapat menyelesaikan skripsi yang berjudul "Perancangan Dan Pembuatan Sistem Antrian Nasabah Bank Berbasis Personal Computer Menggunakan RS-485" ini dengan lancar. Adapun skripsi ini merupakan prasyarat yang harus dipenuhi untuk mencapai gelar Sarjana Teknik di Institut Teknologi Nasional Malang. Keberhasilan penyelesaian skripsi ini tidak lepas dari dukungan serta bantuan dari berbagai pihak, sehingga untuk itu penyusun juga mengucapkan terima kasih yang sebesar-besarnya kepada pihak-pihak yang telah banyak membantu dalam penyusunan skripsi ini :

1. Bapak Prof. Dr. Eng. Ir. Abraham Lomi, MSEF selaku Rektor Institut Teknologi Nasional Malang.
 2. Bapak Ir. Mochtar Asroni, MSME selaku Dekan Fakultas Teknologi Industri Institut Teknologi Nasional Malang.
 3. Bapak Ir. F. Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro / Elektronika S-1 Institut Teknologi Nasional Malang.
 4. Bapak Ir. F. Yudi Limpraptono, MT selaku Dosen Pembimbing Utama yang telah berupaya memberikan bimbingan, pengarahan dan saran-saran hingga terselesainya skripsi ini.
 5. Bapak Ir. Yusuf Ismail Nakhoda, MT selaku Dosen Pembimbing Pendamping yang telah berupaya memberikan bimbingan, pengarahan dan saran-saran hingga terselesainya skripsi ini.
-

6. Kedua Orang Tua dan Saudara penulis yang telah banyak memberikan dukungan moril.
7. Siti Harfiah atas semua doa dan dukungannya.
8. Rekan-rekan yang telah banyak membantu dalam penyusunan skripsi ini yang tidak dapat penulis sebutkan satu – persatu.

Dengan segala keterbatasan kemampuan dan pengetahuan, kami menyadari bahwa dalam skripsi ini masih terdapat banyak sekali kekurangan. Oleh karena itu segala saran dan kritik yang membangun dari semua pihak sangat kami harapkan guna penyempurnaan skripsi ini di kemudian hari.

Akhirnya dengan segala kerendahan hati penyusun berharap semoga skripsi ini dapat bermanfaat bagi kita semua.

Malang, September 2008

Penyusun

DAFTAR ISI

HALAMAN JUDUL	i
LEMBAR PERSETUJUAN	ii
BERITA ACARA SKRIPSI	iii
LEMBAR PERBAIKAN SKRIPSI	iv
ABSTRAKSI.....	v
KATA PENGANTAR.....	vi
DAFTAR ISI	viii
DAFTAR GAMBAR.....	xii
DAFTAR TABEL.....	xiv
BAB I: PENDAHULUAN	
1.1. Latar Belakang	1
1.2. Rumusan Masalah	2
1.3. Tujuan.....	2
1.4. Batasan masalah	3
1.5. Metodologi Penulisan	3
1.6. Sistematika Pembahasan	4
BAB II: DASAR TEORI	
2.1. Mikrokontroler	5
2.1.1. Arsitektur Mikrokontroler AT89S51	6
2.1.2. Diagram Blok Mikrokontroler AT89S51	7
2.1.3. Konfigurasi Pena-pena Mikrokontroler AT89S51	8

2.1.4. Organisasi Memori AT89S51	10
2.1.5. Special Function Register.....	12
2.1.6. Pewaktuan CPU.....	14
2.1.7. Port Serial AT89S51	15
2.1.7.1.Mode Operasi Port Serial	15
2.1.7.2.Register Kontrol Port Serial	17
2.2. Konsep Komunikasi Data.....	19
2.2.1. Mode Transmisi Berdasarkan Jalur Komunikasi	20
2.2.2. Mode Transmisi Paralel Dan Serial	20
2.2.3. Mode Transmisi Data Serial Berdasarkan Pewaktuan	22
2.2.4. Protokol	23
2.3. Komunikasi Serial RS-232.....	24
2.3.1. Karakteristik Sinyal RS-232.....	24
2.3.2. Konektor Dan Jenis Sinyal RS-232.....	26
2.3.3. RS-232 Level Konverter	26
2.4. Komunikasi Serial RS-485.....	27
2.4.1. RS-485.	28
2.4.2. IC SN75176B	31
2.4.3. Komunikasi Multi-drop (Multi-point Communication).....	32

BAB III: PERANCANAAN DAN PEMBUATAN PERALATAN

3.1. Perancangan Perangkat Keras	35
3.1.1. Perancangan Minimum Sistem AT89S51	38
3.1.1.1. Rangkaian Clock	39

3.1.1.2. Rangkaian Reset.....	.40
3.1.2. Perancangan Penggunaan Port-port AT89S51.....	.41
3.1.3. Rangkaian Interface RS-485	.43
3.1.3.1. Perancangan Topologi Jaringan Standar RS-485	.43
3.1.3.2. Rangkaian Interface RS-485 Dengan Komputer.....	.45
3.1.3.3. Rangkaian Interface RS-485 Dengan Port Serial.....	.48
3.2. Perancangan Perangkat Lunak	.49
3.2.1. Software Mikrokontroler	.49
3.2.2. Software Personal Computer	.52

BAB IV: PENGUJIAN ALAT

4.1. Pengujian Interface RS-232 Pada Titik Komputer	.55
4.1.1. Tujuan Pengujian	.55
4.1.2. Peralatan Yang Digunakan	.55
4.1.3. Prosedur Pengujian	.55
4.1.4. Hasil Pengujian	.57
4.2. Pengujian Interface RS-232	.58
4.2.1. Tujuan Pengujian	.58
4.2.2. Peralatan Yang Digunakan.....	.58
4.2.3. Prosedur Pengujian.....	.59
4.2.4. Hasil Pengujian	.60
4.3. Pengujian Penerimaan dan Pengiriman Data	.62
4.3.1. Tujuan Pengujian	.62
4.3.2. Peralatan Yang Digunakan.....	.62

4.3.3. Prosedur Pengujian.....	.62
4.3.4. Hasil Pengujian	.63
4.4. Pengujian Keseluruhan Sistem.....	.66
4.4.1. Tujuan Pengujian	.66
4.4.2. Peralatan Yang Digunakan.....	.66
4.4.3. Prosedur Pengujian.....	.67
4.4.4. Hasil Pengujian	.67

BAB V: PENUTUP

5.1 Kesimpulan.....	.70
5.2 Saran.....	.71

DAFTAR PUSTAKA

LAMPIRAN

DAFTAR GAMBAR

GAMBAR 2.1	Blok Diagram AT89S51	.7
GAMBAR 2.2	Konfigurasi Pena-Pena AT89S51	.8
GAMBAR 2.3	Struktur Memori AT89S51	.11
GAMBAR 2.4	Hubungan Oscilator	.14
GAMBAR 2.5	Susunan Bit Dalam SCON	.17
GAMBAR 2.6	Elemen Komunikasi Data	.19
GAMBAR 2.7	Transmisi Data Paralel	.21
GAMBAR 2.8	Transmisi Data Serial	.21
GAMBAR 2.9	Transmisi Asinkron	.23
GAMBAR 2.10	Level Tegangan RS-232	.25
GAMBAR 2.11	Konfigurasi Pin RS-232 (Female)	.26
GAMBAR 2.12	Konverter TTL – RS-232	.27
GAMBAR 2.13	RS-485	.29
GAMBAR 2.14	Level Tegangan Driver RS-485	.30
GAMBAR 2.15	IC SN75176B	.32
GAMBAR 2.16	Topologi Jaringan Multi-drop RS-485	.33
GAMBAR 3.1	Blok Diagram Sistem	.36
GAMBAR 3.2	Rangkaian Clock	.39
GAMBAR 3.3	Rangkaian Reset	.40
GAMBAR 3.4	Perancangan Pemakaian Port-Port AT89S51	.42
GAMBAR 3.5	Perencanaan Topologi Jaringan RS-485	.44

GAMBAR 3.6 Rangkaian Interface RS-485 Dengan Komputer	.46
GAMBAR 3.7 Rangkaian Interface RS-485 Dengan Port Serial AT89S51	.48
GAMBAR 3.8 Flowchart Program Mikrokontroler.....	.51
GAMBAR 3.9 Flowchart Program PC Secara Umum.....	.53
GAMBAR 3.10 Flowchart Pengolahan Data Pada Customer Service.....	.54
GAMBAR 4.1 Rangkaian Pengujian Di Titik Komputer	.56
GAMBAR 4.2 Tampilan Oscilloskop.....	.57
GAMBAR 4.3 Ilustrasi Pengukuran	.58
GAMBAR 4.4 Rangkaian Pengujian Output MAX 232.....	.59
GAMBAR 4.5 Tampilan Oscilloskop.....	.60
GAMBAR 4.6 Ilustrasi Pengukuran	.61
GAMBAR 4.7 Blok Diagram Pengujian Penerimaan Dan Pengiriman Data.....	.62
GAMBAR 4.8 Tampilan Oscilloskop.....	.63
GAMBAR 4.9 Ilustrasi Pengukuran	.64
GAMBAR 4.10 Tampilan Oscilloskop.....	.65
GAMBAR 4.11 Ilustrasi Pengukuran	.66
GAMBAR 4.12 Blok Diagram Pengujian Keseluruhan Sistem	.67
GAMBAR 4.13 Tampilan Awal Program.....	.68
GAMBAR 4.14 Tampilan Antrian Pada Layar Monitor.....	.68
GAMBAR 4.15 Tampilan Antrian Saat CS 1 kondisi "break".....	.69

DAFTAR TABEL

TABEL 2.1	Deskripsi Pena AT89S51	8
TABEL 2.2	Alamat Ruang SFR.....	12
TABEL 2.3	Penentuan Mode Kerja Port Serial	18
TABEL 2.4	Perbandingan RS-232 Dan RS-485	28

BAB I

PENDAHULUAN

1.1. Latar Belakang

Perkembangan teknologi dewasa ini telah semakin pesat dan maju. Teknologi menjadi suatu media penerapan yang membantu manusia dalam hampir seluruh aspek kehidupannya. Berbagai perangkat dan fasilitas kehidupan manusia telah diciptakan, mulai dari yang sederhana hingga sampai ke hal – hal yang kompleks. Dan hingga kini manusia terus menerus tiada hentinya mengembangkan ilmu pengetahuan dan teknologi untuk menemukan dan menciptakan segala sesuatu yang pada dasarnya akan memberikan kemudahan, efektifitas, penghematan, keunggulan kerja dan manfaat yang besar bagi kehidupan manusia di segala bidang.

Salah satu perkembangan teknologi khususnya teknologi bidang elektronika adalah teknologi komputer, yang berkembang pesat dalam segi hardware maupun software. Teknologi komputer ini sudah umum diterapkan dalam segala bidang, misalnya pada bank – bank dalam aplikasi perbankan.

Dalam dunia perbankan yang sangat sensitif terhadap tingkat keamanan dan kenyamanan pelayanan terhadap nasabahnya, maka diperlukan suatu teknologi yang sebaik mungkin yang dapat menjamin kenyamanan nasabahnya dalam melakukan setiap transaksi. Dalam melakukan transaksi tersebut, terkadang para nasabah harus rela antri dengan cara berdiri yang terkadang bisa saja antrian itu berlangsung lama hingga berjam - jam. Hal ini tentu saja sangat merepotkan dan

melelahkan bagi para nasabah. Oleh karenanya diperlukan sistem antrian yang lebih baik untuk para nasabah agar para nasabah lebih nyaman dalam melakukan setiap aktivitas transaksinya. Menyikapi hal tersebut, maka perlu direncanakan dan dibuat suatu sistem antrian yang lebih baik dalam memberikan kenyamanan pelayanan bagi para nasabah.

Dalam sistem ini, ditekankan kasus antrian yang terjadi pada bagian layanan (customer service), dimana nasabah tidak perlu harus berdiri mengantri di depan loket karena antrian akan diatur otomatis oleh sistem sehingga nasabah hanya perlu melihat tampilan nomer urut antriannya di layar monitor dan atau mendengarkan informasi suara dari speaker/pengeras suara yang tersedia.

1.2. Rumusan Masalah

Dari uraian latar belakang diatas, maka dapat dibuat rumusan masalahnya, yaitu : bagaimana merencanakan dan membuat sistem antrian untuk para nasabah bank, baik berupa hardware maupun software, dimana sistem akan dikendalikan oleh Personal Computer bersama – sama dengan Mikrokontroler AT89S51, saling berkomunikasi menggunakan saluran RS-485.

1.3. Tujuan

Adapun tujuan perencanaan dan pembuatan sistem dalam skripsi ini seperti uraian diatas adalah:

1. Mempelajari implementasi sistem Mikrokontroler khususnya AT89S51 yang didalamnya melibatkan unit – unit push button dan LED.
-

2. Merancang suatu perangkat komunikasi untuk saluran RS-485 agar dapat digunakan oleh Personal Computer dan Mikrokontroler AT89S51 untuk saling berkomunikasi, membentuk sistem antrian secara keseluruhan.

1.4. Batasan Masalah

Agar pembahasan dalam skripsi ini dapat memenuhi sasaran yang diinginkan, maka diperlukan batasan – batasan dalam pengkajiannya. Adapun batasan masalah dalam skripsi ini adalah :

1. Menggunakan Mikrokontroler AT89S51 sebagai pengkap kerja sistem yang menggunakan saluran RS-485, dimana keseluruhan sistem dikendalikan oleh Personal Computer.
2. Studi kasus yang terjadi hanya untuk bagian customer service.
3. Simulasi yang digunakan dalam analisa perancangan RS-485 dibatasi hanya dua titik/node.

1.5. Metodologi Penulisan

Metode yang digunakan dalam penulisan skripsi ini adalah :

1. Studi Pustaka

Memperoleh data dengan cara mempelajari secara sistematis buku – buku ataupun literatur yang berhubungan dengan sistem untuk tujuan perancangan alat.

2. Studi Lapangan
-

Memperoleh data dengan cara praktek langsung dalam pembuatan alat berdasarkan rancangan yang ada serta melakukan pengolahan data dengan jalan membuat analisa dari hasil pengujian yang ada.

1.6. Sistematika Pembahasan

Agar sistematis dan dapat mencapai pemahaman yang tepat, maka skripsi ini disusun dalam beberapa bab, yaitu :

BAB I Pendahuluan

Meliputi Latar belakang, Rumusan masalah, Tujuan, Batasan masalah, Metodologi penulisan, dan Sistematika pembahasan.

BAB II Landasan Teori

Meliputi teori penunjang yang dijadikan dasar – dasar dalam perancangan dan pembuatan alat.

BAB III Perencanaan Dan Pembuatan Alat

Meliputi berbagai hal yang berkenaan dengan perancangan perangkat keras maupun perangkat lunak.

BAB IV Pengujian Dan Analisa Data

Menerangkan hasil pengujian dan analisa pada alat yang telah dibuat

BAB V Penutup

Meliputi kesimpulan dan saran yang didapat selama perancangan dan pembuatan alat.

DAFTAR PUSTAKA

LAMPIRAN

BAB II

LANDASAN TEORI

Landasan teori sangat membantu untuk dapat memahami suatu sistem. Disamping itu dapat juga dijadikan sebagai bahan acuan didalam merencanakan suatu sistem. Dengan pertimbangan hal-hal tersebut, maka landasan teori merupakan bagian yang harus dipahami untuk pembahasan selanjutnya.

2.1. Mikrokontroler

Sistem minimum mikroprosesor umumnya terdiri dari beberapa bagian seperti CPU, ROM, RAM dan I/O. Penggabungan keseluruhan komponen-komponen tersebut dalam satu *chip* menyebabkan dimensi serta daya yang dibutuhkan oleh sistem menjadi lebih kecil. Komponen baru ini kemudian disebut *single chip microcomputer*.

Aplikasi *single chip microcomputer* dibatasi oleh kapasitas program yang mampu dilaksanakannya, sehingga secara umum setiap aplikasinya bercirikan sebagai berikut :

- Perhitungan matematis yang sederhana
- Program aplikasi yang kecil
- Aplikasi biasanya berorientasi pada sistem kontrol.

Berdasarkan ciri-ciri tersebut maka *single chip microcomputer* juga sering disebut *microcontroller*.

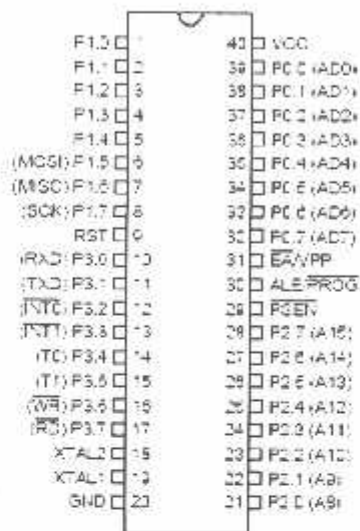
2.1.1. Arsitektur Mikrokontroler AT89S51

Mikrokontroler AT89S51 adalah sebuah mikrokomputer CMOS 8 bit berkinerja tinggi dengan *supply* tegangan yang rendah dan merupakan salah satu keluarga MCS-51 yang memiliki 4 kbyte Flash PEROM. Mikrokontroler ini banyak dipakai untuk keperluan kontrol, komunikasi, industri dan lain-lain. Mikrokontroler AT89S51 ini mempunyai beberapa keistimewaan antara lain :

- Termasuk keluarga MCS-51
 - 8 bit CMOS mikrokomputer berkinerja tinggi
 - 128 byte data memori (RAM) pada *chip (internal)*.
 - 4K byte *Reprogrammable Flash Memory*
 - 2 buah *timer/counter* 16 bit
 - 32 Programmable I/O
 - *Fully Static Operation* : 0 Hz – 33 MHz
 - *Oscillator* dan *clock* internal (*on-chip*).
 - Data serial dua arah (*Full duplex UART*)
 - *Mode* untuk *Low Power* dan *Power Down*
-

2.1.3. Konfigurasi Pena – pena Mikrokontroler AT89S51

Mikrokontroler AT89S51 dengan 40 pin, memiliki pena – pena seperti yang terlihat pada gambar 2.2 berikut :



Gambar 2.2 Konfigurasi Pena-pena AT89S51^[1]

• Fungsi dari pena atau kaki-kaki tersebut adalah sebagai berikut :

Tabel 2.1 Deskripsi Pena AT89S51^[3]

Nomor Pin	Nama Pin	Alternatif	Keterangan
20	GND		Ground
40	VCC		Power Supply
32...39	P0.7...P0.0	AD7...AD0 & A7...A0	Port 0 dapat berfungsi sebagai I/O biasa, menerima <i>low order multiplex address/data</i> ataupun menerima kode byte pada saat <i>Flash Programming</i>. Pada fungsi sebagai I/O biasa port ini dapat memberikan output sink ke 8 buah TTL input atau dapat diubah sebagai input dengan memberikan logika 1 pada port tersebut. Pada fungsi sebagai <i>low order multiplex address/data</i> port ini akan mempunyai internal pull-up.

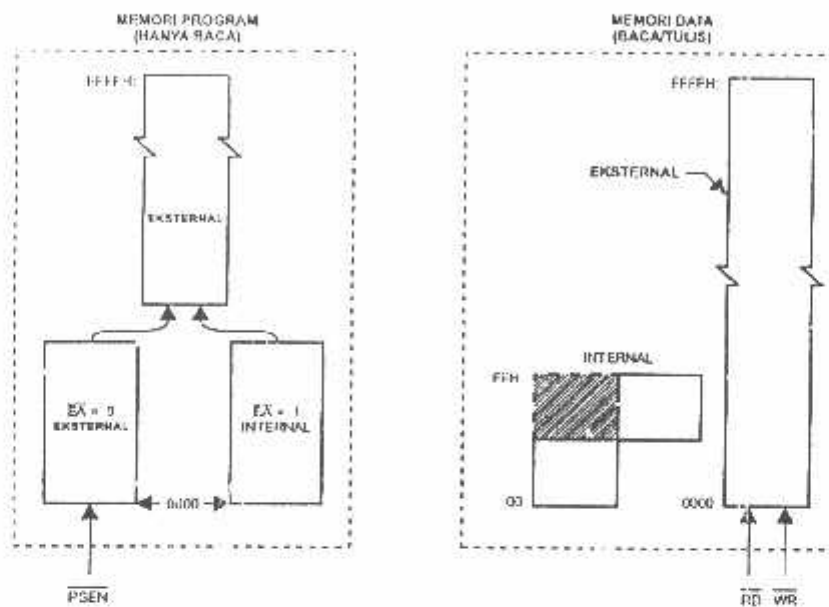
			Pada saat flash programming diperlukan external pull-up terutama pada saat verifikasi program.
1...8	P1.0...P1.7		Port 1 berfungsi sebagai I/O biasa atau menerima low order address byte selama pada saat Flash programming. Fasilitas khusus dari port 1 ini adalah adanya <i>In-System Programming</i>, yaitu port 1.5 sebagai MOSI, port 1.6 sebagai MISO, port 1.7 sebagai SCK. Port ini mempunyai internal pull-up dan berfungsi sebagai input dengan memberikan logika 1. Sebagai output port ini dapat memberikan output sink ke 4 buah input TTL.
21...28	P2.0...P2.7	A8...A15	Port 2 berfungsi sebagai I/O biasa atau high order address, pada saat mengakses memori secara 16-bit (<u>MOVX@DPTR</u>). Pada saat mengakses memori secara 8-bit (<u>MOV@Rn</u>), port ini akan mengeluarkan isi dari <i>P2 Special Function Register</i>. Port ini mempunyai internal pull-up dan berfungsi sebagai input dengan memberikan logika 1. Sebagai output, port ini dapat memberikan output sink ke 4 buah input TTL.
10...17	Port 3		Sebagai I/O biasa Port 3 mempunyai sifat yang sama dengan Port 1 maupun Port 2. Sedangkan sebagai fungsi spesial port - port ini mempunyai keterangan sebagai berikut :
10	P3.0	RXD	Port Serial Input
11	P3.1	TXD	Port Serial Output
12	P3.2	INT0	Port External Interrupt 0
13	P3.3	INT1	Port External Interrupt 1
14	P3.4	T0	Port External Timer 0 input
15	P3.5	T1	Port External Timer 1 input
16	P3.6	WR	External Data Memory Write Strobe
17	P3.7	RD	External Data Memory Read Strobe
9	RST		Reset akan aktif dengan memberikan input high selama 2 cycle
30	ALE	PROG	Pin ini dapat berfungsi sebagai Address Latch Enable(ALE) yang me-latch low byte address pada saat mengakses memori eksternal. Sedangkan pada saat Flash

			programming(PROG) akan berfungsi sebagai pulsa input. Pada operasi normal ALE akan mengeluarkan sinyal clock sebesar 1/16 frekwensi oscillator kecuali pada saat mengakses memori eksternal. Sinyal clock pada pin ini dapat pula didisable dengan men-set bit 0 dari Special Function Register di alamat 8EH. ALE hanya akan aktif pada saat mengakses memori eksternal (MOVX & MOVC).
29	PSEN		Pin ini berfungsi pada saat mengeksekusi program yang terletak pada memori eksternal. PSEN akan aktif dua kali setiap cycle.
31	EA	VP	Pada kondisi low, pin ini berfungsi sebagai EA yaitu mikrokontroler akan menjalankan program yang ada pada memori eksternal setelah sistem di-reset. Jika berkondisi high, pin ini berfungsi untuk menjalankan program yang ada pada memori internal. Pada saat Flash programming pin ini akan mendapat tegangan 12 volt.
19	XTAL1		<i>Input Oscillator</i>
18	XTAL2		<i>Output Oscillator</i>

2.1.4. Organisasi Memori AT89S51

Struktur memori pada mikrokontroler AT89S51 dapat dibagi menjadi dua bagian yaitu memori program dan memori data. Pembagian tersebut didasarkan atas fungsinya. Memori program digunakan untuk menyimpan instruksi-instruksi yang akan dijalankan oleh mikrokontroler, sedangkan memori data digunakan sebagai tempat penyimpanan data yang sedang diolah mikrokontroler. Program mikrokontroler disimpan dalam memori program berupa ROM. Mikrokontroler AT89S51 dilengkapi dengan ROM internal

namun untuk program – program yang lebih besar biasanya digunakan ROM eksternal yang terpisah dari mikrokontroler.



Gambar 2.3 Struktur Memori AT89S51^[2]

Mikrokontroler AT89S51 memiliki ruang alamat memori data dan program yang terpisah seperti ditunjukkan pada gambar 2.3, dimana dimungkinkan mengakses memori eksternal hingga 64 Kbyte. Memori program hanya bisa dibaca saja. *Strobe* (tanda) untuk akses program memori eksternal melalui sinyal $\overline{\text{PSEN}}$ atau *Program Store Enable*. CPU akan memberikan sinyal baca dan tulis, $\overline{\text{RD}}$ dan $\overline{\text{WR}}$, selama pengaksesan memori.

2.1.5. Special Function Register AT89S51

Register Fungsi Khusus (*Special Function Register*) terletak dalam RAM internal pada lokasi 80H hingga FFH, dimana register ini mencakup port – port, pewaktu (timer), kontrol periferan dan lain – lain. Alamat – alamat SFR ditunjukkan pada tabel 2.2.

Tabel 2.2 Alamat Ruang SFR^[3]

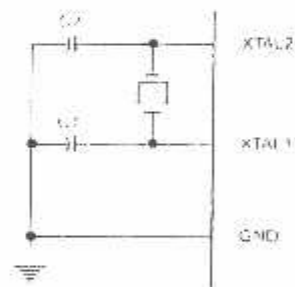
Simbol	Nama Register	Alamat
Acc	Accumulator	E0 _H
B	Register B	F0 _H
PSW	Program Status Word	D0 _H
SP	Stack Pointer	81 _H
DPL	Low bytes	82 _H
DPH	High bytes	83 _H
P0	Port 0	80 _H
P1	Port 1	90 _H
P2	Port 2	A0 _H
P3	Port 3	B0 _H
IP	Interrupt Priority Control	D8 _H
IE	Interrupt Enable Control	A8 _H
TMOD	Timer/Counter Mode Control	89 _H
TCN	Timer/Counter Control	88 _H
TH0	Timer/Counter 0 high byte	8C _H
TL0	Timer/Counter 0 low byte	8A _H
TH1	Timer/Counter 1 high byte	8D _H
TL1	Timer/Counter 1 low byte	8B _H
SCON	Serial Control	98 _H
SBUF	Serial Data Buffer	99 _H
PCON	Power Control	87 _H

Beberapa macam register fungsi khusus yang sering digunakan, dijelaskan sebagai berikut :

- *Accumulator (ACC)* digunakan sebagai register untuk penyimpanan data sementara, dalam program instruksinya mengacu sebagai register A.
 - *Register B* digunakan selama operasi perkalian dan pembagian.
 - *Program Status Word (PSW)* berisi bit – bit status yang berkaitan dengan kondisi CPU saat itu. Status yang tersimpan dalam PSW meliputi : *carry bit*, *the auxiliary carry* (untuk operasi BCD), dua *bit* pemilih bank register, *overflow flag*, sebuah bit paritas, dan dua flag status yang bisa didefinisikan sendiri (*user-defineable*).
 - *Stack Pointer (SP)* adalah register 8 bit yang digunakan dalam proses simpan dan ambil dari/ke *stack*. Walau *stack* bisa menempati lokasi di mana saja dalam RAM, register SP akan selalu diinisialisasi ke alamat 07H setelah adanya reset, hal ini menyebabkan *stack* berawal di lokasi 08H.
 - *Data Pointer (DPTR)* terdiri dari dua register, yaitu byte tinggi (*Data Pointer High*, DPH) dan byte rendah (*Data Pointer Low*, DPL), bersama – sama membentuk register yang mampu menyimpan alamat 16-bit.
 - Port 0, Port 1, Port 2, Port 3 merupakan register yang digunakan untuk menyimpan data yang akan dibaca atau ditulis dari/ke port.
-

- *Serial Data Buffer (SBUF)* sebenarnya terdiri dari dua register yang terpisah, register penyangga pengirim (*transmit buffer*) dan penyangga penerima (*receive buffer*). Pada saat data disalin ke SBUF, maka data sesungguhnya dikirim ke penyangga pengirim dan sekaligus mengawali transmisi data serial. Sedangkan pada saat data disalin dari SBUF, maka sebenarnya data tersebut berasal dari penyangga penerima.
- *Control Register* : Register – register IP, IE, TMOD, TCON, T2CON, T2MOD, SCON dan PCON berisi bit – bit kontrol dan status untuk sistem interupsi, Pencacah/Pewaktu dan Port Serial.

2.1.6. Pewaktuan CPU



C1, C2 = 30 pF $\pm$ 10 pF for Crystals
= 40 pF $\pm$ 10 pF for Ceramic Resonators

Gambar 2.4 Hubungan Osilator^[1]

Mikrokontroler AT89S51 memiliki osilator internal (*on chip oscillator*) yang dapat digunakan sebagai sumber detak (*clock*) bagi CPU. Untuk menggunakan osilator *internal* diperlukan sebuah kristal antara pena

XTAL. 1 dan XTAL. 2 dan menyambungkan kapasitornya ke *ground* seperti pada gambar 2.4. Dapat digunakan kristal dengan frekuensi antara 4 sampai 24 MHz, sedangkan untuk kapasitor dapat digunakan $30 \text{ pF} \pm 10 \text{ pF}$ untuk kristal dan $40 \text{ pF} \pm 10 \text{ pF}$ untuk keramik.

2.1.7. Port Serial AT89S51

Mikrokontroler AT89S51 dilengkapi dengan port serial yang dapat memungkinkan untuk komunikasi data serial secara *full duplex* yang berarti port serial dapat mengirim dan menerima data secara bersamaan. Selain itu juga memiliki penyangga penerima, artinya port serial mulai bisa menerima byte yang kedua sebelum byte yang pertama dibaca oleh register penerima (jika sampai byte yang kedua selesai diterima sedangkan byte pertama belum juga dibaca, maka salah satu byte akan hilang). Port serial terdapat dalam kelompok pin/pena port 3, yaitu port 3.0 sebagai port masukan serial (RxD) dan port 3.1 sebagai port keluaran serial (TxD). Penerimaan dan pengiriman data port serial melalui register SBUF. Penulisan ke SBUF berarti mengisi register pengiriman ke SBUF sedangkan pembacaan dari SBUF berarti membaca register penerimaan SBUF yang memang terpisah secara fisik (secara perangkat lunak namanya menjadi satu yaitu SBUF).

2.1.7.1.Mode Operasi Port serial

Port serial pada AT89S51 bisa digunakan dalam 4 mode kerja yang berbeda. Dari 4 mode tersebut, 1 mode diantaranya bekerja secara sinkron dan 3 lainnya bekerja secara asinkron. Keempat mode kerja itu adalah mode 0, mode 1, mode 2, dan mode 3.

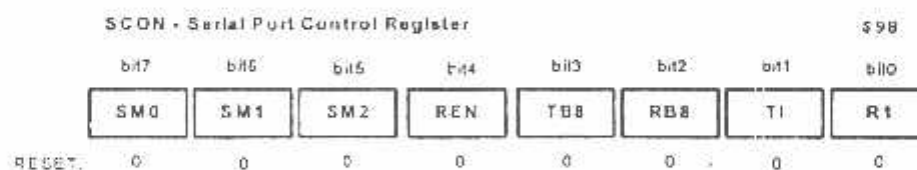
- **Mode 0 (*shift register 8 bit*) :** Mode ini bekerja secara sinkron, data serial dikirim dan diterima melalui kaki P3.0 (Rx/D), sedangkan kaki P3.1 (Tx/D) dipakai untuk menyalurkan detak pendorong data serial yang dibangkitkan AT89S51. Data dikirim/diterima 8 bit sekaligus, dimulai dari bit yang bobotnya paling kecil atau LSB (bit 0) dan diakhiri dengan bit yang bobotnya paling besar atau MSB (bit 7). Kecepatan pengiriman data (*baudrate*) adalah 1/12 frekuensi kristal yang digunakan.
 - **Mode 1 (UART 8-bit dengan *Baud Rate* Dapat Diatur) :** Pada mode ini tetap yaitu, data dikirim melalui kaki P3.1 (Tx/D) dan diterima melalui kaki P3.0 (Rx/D), secara asinkron (juga mode 2 dan 3). Pada Mode 1 data dikirim/diterima 10 bit sekaligus, diawali dengan 1 bit *start*, disusul dengan 8 bit data yang dimulai dari bit yang bobotnya paling kecil (bit 0), diakhiri dengan 1 bit *stop*. Pada AT89S51 yang berfungsi sebagai penerima bit *stop* adalah RB8 dalam register SCON. Kecepatan pengiriman data (*baud rate*) bisa diatur sesuai dengan keperluan. Mode inilah (mode 2 dan 3) yang umum dikenal sebagai UART (*Universal Asynchronous Receiver/Transmitter*).
 - **Mode 2 (UART 9-bit dengan *Baud Rate* Permanen) :** Data dikirim/diterima 11 bit sekaligus, diawali dengan 1 bit *start*, disusul 8 bit data yang dimulai dari bit yang bobotnya paling kecil (bit 0), kemudian bit ke 9 yang bisa diatur lebih lanjut, diakhiri
-

dengan 1 bit *stop*. Pada AT89S51 yang berfungsi sebagai pengirim, bit 9 tersebut berasal dari bit TB8 dalam register SCON. Pada AT89S51 yang berfungsi sebagai penerima, bit 9 ditampung pada bit RB8 dalam register SCON, sedangkan bit *stop* diabaikan tidak ditampung. Kecepatan pengiriman data (*baud rate*) bisa dipilih antara 1/32 atau 1/64 frekuensi kristal yang digunakan.

- **Mode 3** : mode ini sama dengan mode 2, hanya saja kecepatan pengiriman data (*baud rate*) bisa diatur sesuai dengan keperluan, seperti halnya Mode 1.

2.1.7.2. Register Kontrol Port Serial

Register kontrol dan status untuk port serial berada dalam register SCON, seperti yang ditunjukkan dalam gambar 2.5. Register ini mengandung bit-bit pemilihan mode kerja port serial, bit data ke-9 pengiriman dan penerimaan (TB8 dan RB8) serta bit-bit interupsi port serial (TI dan RI).



Gambar 2.5 Susunan Bit dalam SCON^[2]

Keterangan :

- Bit SM0 dan SM1 (bit 7 dan 6 pada register SCON) dipakai untuk menentukan mode kerja port serial. Setelah reset kedua bit ini bernilai '0' dan penentuan mode kerja port serial mengikuti tabel 2.3.

Tabel 2.3 Penentuan Mode Kerja Port Serial^[2]

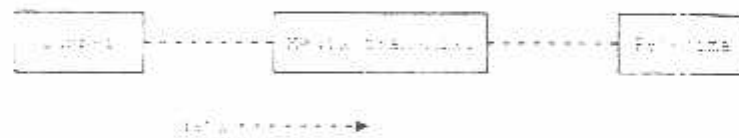
SM0	SM1	Mode	Keterangan	Baud Rate
0	0	0	Register geser	Tetap ($f_{osc}/12$)
0	1	1	UART 8-bit	Bisa diubah-ubah (dengan timer)
1	0	2	UART 9-bit	Tetap ($f_{osc}/64$ atau $f_{osc}/32$)
1	1	3	UART 9-bit	Bisa diubah-ubah (dengan timer)

- Bit REN (bit 4) dipakai untuk mengaktifkan kemampuan port serial untuk menerima data. Pada mode 0 kaki RxD (P3.0) dipakai untuk mengirim data serial dan juga untuk menerima data serial. Sifat ini terbawa pula pada saat port serial bekerja pada mode 1, 2, dan 3, meskipun pada mode – mode tersebut kaki RxD hanya dipakai untuk menerima data, agar kaki RxD dapat dipakai untuk menerima data, terlebih dahulu harus dibuat REN = '1'. Setelah reset bit REN bernilai '0'.
- Pada mode 2 dan mode 3, port serial bekerja dengan 9 bit data (dari 11 bit, 1 bit untuk bit start dan 1 bit untuk bit stop), SBUF yang kapasitasnya 8 bit tidak cukup untuk keperluan ini. Bit kesembilan yang akan dikirim terlebih dulu diletakkan di TB8 (bit

3), sedangkan bit RB8 (bit 2) merupakan bit yang dipakai untuk menampung bit ke-sembilan yang diterima port serial.

2.2. Konsep Komunikasi Data

Istilah komunikasi data (*data communication*) mengandung arti pengiriman data (data yang menggunakan komputer) yang dilakukan menggunakan sistem transmisi elektronik. Untuk mengkomunikasikan data dari satu tempat ke tempat yang lain, tiga elemen sistem harus tersedia, yaitu sumber data (*source*), media transmisi (*transmission media*) yang membawa data yang dikirimkan dari sumber data ke elemen ketiga yaitu penerima (*receiver*). Bila salah satu elemen tidak ada, maka komunikasi tidak akan dapat dilakukan, seperti yang terlihat pada gambar 2.6.



Gambar 2.6 Elemen Komunikasi Data^[4]

Sedangkan transmisi data (*data transmission*) merupakan proses pengiriman data dari sumber ke penerima data. Untuk mengetahui tentang transmisi data lebih lengkap maka perlu diketahui beberapa hal yang berhubungan dengan proses ini, antara lain : mode transmisi dan protokol.

2.2.1. Mode transmisi Berdasarkan Jalur Komunikasi

Berdasarkan jalur komunikasinya, transmisi data terbagi menjadi 3 yaitu :

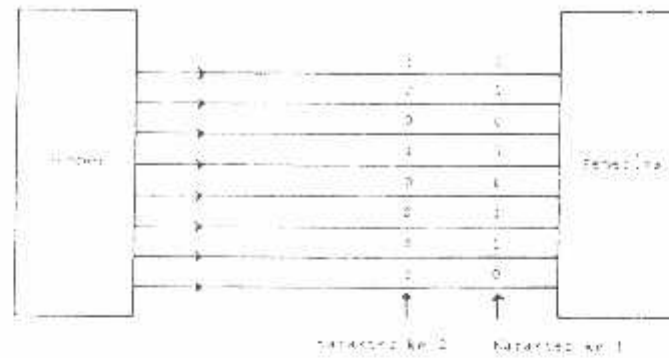
- a. **Simplex** : komunikasi yang hanya dapat membawa informasi data dalam satu arah saja, tidak bisa bolak – balik. Contohnya siaran radio atau televisi.
- b. **Half Duplex** : komunikasi dimana informasi data mengalir dalam dua arah secara bergantian (satu arah dalam suatu saat tertentu), yaitu bila satu mengirim, yang lain sebagai penerima dan sebaliknya, tidak bisa serentak. Contohnya Radio CB *walkie-talkie*.
- c. **Full-duplex** : komunikasi dimana informasi data dapat mengalir dalam dua arah serentak (dapat mengirim dan menerima data pada saat yang bersamaan. Contohnya komunikasi lewat telepon.

2.2.2. Mode Transmisi Paralel Dan Serial.

Berdasarkan caranya, mode transmisi dibagi menjadi 2 yaitu mode secara Paralel (*parallel transmission*) dan Serial (*serial transmission*)

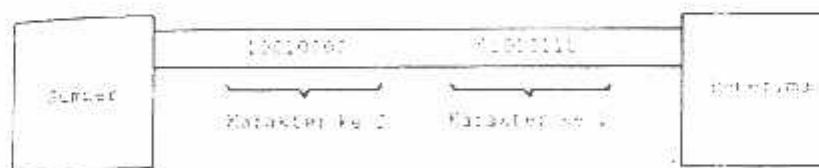
a. Transmisi Data Paralel.

Pada mode transmisi paralel, semua bit dari karakter yang diwakili oleh suatu kode, ditransmisikan secara serentak satu karakter setiap saat, seperti gambar 2.7.

Gambar 2.7 Transmisi Data Paralel^[4]

b. Transmisi Data Serial.

Transmisi secara seri merupakan mode transmisi yang umum dipergunakan. Pada mode ini, masing – masing bit dari suatu karakter dikirimkan secara ber-urutan, yaitu bit per bit, satu diikuti oleh bit berikutnya. Penerima kemudian merakit kembali arus bit-bit yang datang ke dalam bentuk karakter, seperti yang terlihat pada gambar 2.8.

Gambar 2.8 Transmisi Data Serial^[4]

Transmisi data serial dapat berbentuk *synchronous transmission* atau *asynchronous transmission*.

2.2.3. Mode Transmisi Data Serial Berdasarkan Pewaktuannya.

Berdasarkan pewaktuannya, transmisi data secara seri terbagi atas transmisi sinkron (*synchronous transmission*) dan transmisi asinkron (*asynchronous transmission*).

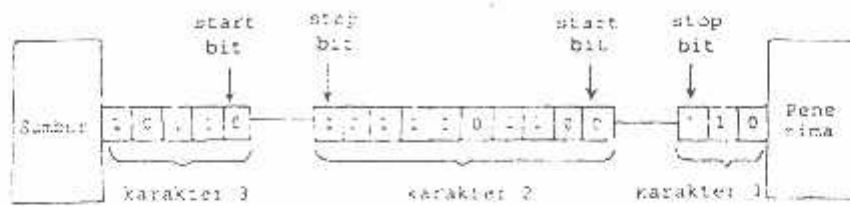
a. Sinkron.

Transmisi sinkron, yaitu waktu pengiriman bit-bit di sumber pengirim (*source*) harus sinkron (sesuai) dengan waktu penerimaan bit-bit yang diterima oleh penerima (*receiver*), kapan sumber pengirim (*source*) harus meletakkan bit-bit yang akan dikirim ke *channel* transmisi dan kapan penerima (*receiver*) harus mengetahui waktu yang tepat untuk mengambil bit-bit yang dikirim tersebut.

b. Asinkron.

Transmisi Asinkron, merupakan transmisi dari data yang ditransmisikan satu karakter tiap waktu yang tertentu. Pengirim dapat mentransmisikan karakter – karakter pada interval waktu yang berbeda, atau dengan kata lain tidak harus dalam waktu yang sinkron antara pengiriman satu karakter dengan karakter berikutnya. Tiap – tiap karakter yang ditransmisikan sebagai satu kesatuan yang berdiri sendiri dan penerima harus dapat mengenal masing – masing karakter tersebut. Untuk mengatasi hal ini, maka masing – masing karakter diawali dengan suatu bit-bit tambahan, yaitu *start bit* atau *start pulse* yang berupa nilai bit 0 dan *stop bit* atau *stop pulse* yang berupa nilai

bit 1 diletakkan pada akhir dari masing – masing karakter, seperti ditunjukkan pada gambar 2.9.



Gambar 2.9 Transmisi Asinkron^[4]

2.2.4. Protokol

Protokol adalah kumpulan dari aturan – aturan yang berhubungan dengan komunikasi data antara alat-alat komunikasi supaya komunikasi data dapat dilakukan dengan benar. Jabatan tangan merupakan contoh dari *protocol* antara dua manusia yang akan berkomunikasi. Di dalam istilah komputer, jabatan tangan (*handshaking*) menunjukkan suatu *protocol* dari komunikasi data bila dua alat dihubungkan satu dengan yang lainnya untuk menentukan bahwa keduanya telah kompatibel.

Supaya kompatibel, maka pada transmisi data, antara lain keduanya harus mempunyai *transfer rate* (tingkat pengiriman) yang sama, format datanya harus sama, tipe transmisinya harus sama dan mode transmisinya juga harus sama. Jika semua kondisi tersebut telah kompatibel, maka dapat dilakukan komunikasi data dengan benar. Protokol umumnya berupa suatu perangkat lunak (*software*) yang mengatur komunikasi data tersebut.

2.3. Komunikasi Serial RS-232

Interface merupakan suatu piranti yang dapat menghubungkan satu peralatan ke peralatan yang lain sehingga peralatan tersebut dapat saling berkomunikasi. Sedangkan cara/proses untuk menghubungkan dua sistem yang berbeda agar dapat bekerjasama disebut interfacing.

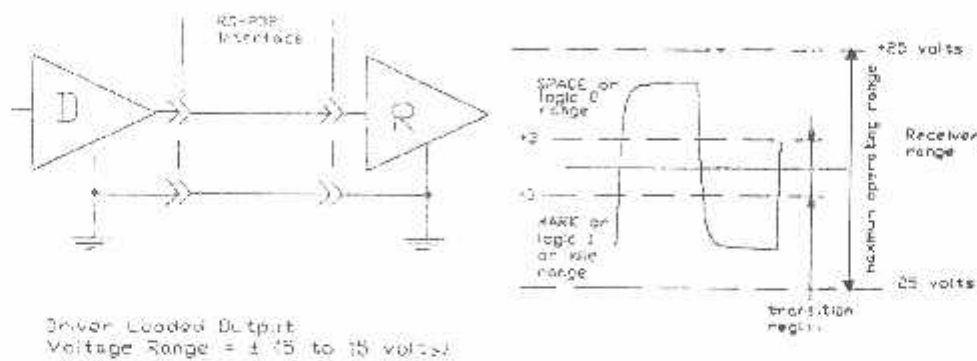
RS-232 merupakan salah satu jenis interface dalam proses transfer data antar peralatan komputer dalam bentuk serial. RS-232 merupakan kependekan dari Recommended Standard Number 232. Standar RS232 ditetapkan oleh Electronic Industry Association dan Telecommunication Industry Association pada tahun 1962. Nama lengkapnya adalah *EIA/TIA-232 Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange*.

Ada 3 hal pokok yang diatur oleh standar RS-232, antara lain : 1) bentuk sinyal dan level tegangan yang dipakai, 2) penentuan jenis sinyal dan konektor yang dipakai, serta susunan sinyal pada kaki – kaki di konektor dan 3) penentuan tata cara pertukaran informasi antara komputer dan alat – alat pelengkapinya.

2.3.1. Karakteristik Sinyal RS-232

Karakteristik ini meliputi bentuk sinyal dan level tegangan sinyal. Level tegangan yang umum digunakan dalam dunia digital dibuat atas dasar tegangan catu daya +5 Volt, tegangan input kurang dari 0,8 volt dianggap sebagai level tegangan '0' atau *space* dan tegangan input lebih dari 2.0 volt dianggap sebagai level tegangan '1' atau *mark*. Level tegangan ini sering disebut sebagai level tegangan TTL.

RS-232 dibuat jauh sebelum IC TTL populer, sehingga level tegangan yang ditentukan untuknya jauh berbeda dengan level tegangan TTL. Dalam standar RS-232, tegangan input antara +3 sampai +15 Volt dianggap sebagai level tegangan '0' dan tegangan input antara -3 sampai -15 Volt dianggap sebagai level tegangan '1', seperti yang terlihat pada gambar 2.10.



Gambar 2.10 Level Tegangan RS-232^[5]

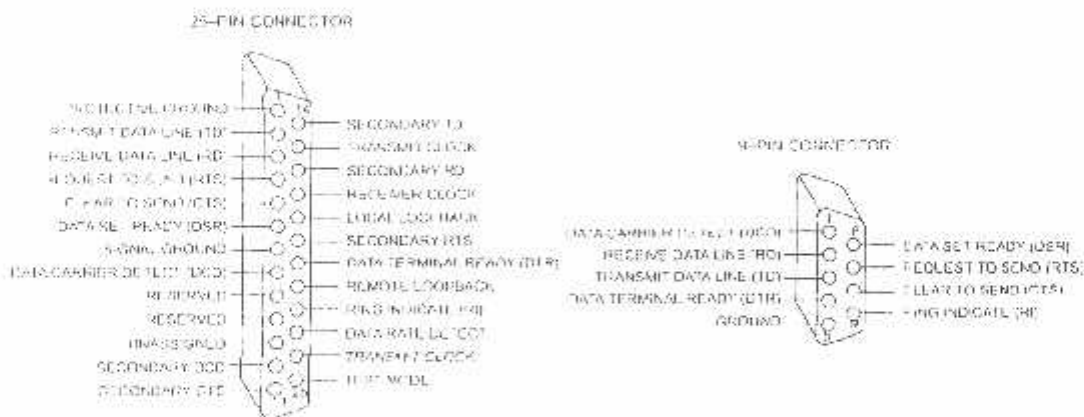
Daerah tegangan antara -3 Volt hingga +3 Volt adalah level invalid artinya daerah yang tidak memiliki level logika, sehingga daerah tersebut harus dihindari. Suatu saluran data RS-232 yang memberi keadaan ini berarti ada kesalahan. Demikian pula saluran daerah lebih negatif dari -15 volt dan daerah lebih positif dari +15 Volt merupakan daerah level invalid.

Impedansi saluran dibatasi antara 3 Kilo-Ohm sampai 7 Kilo-Ohm, serta ditentukan kecepatan transmisi tidak boleh lebih dari 20 KiloBit/detik. Dalam standar RS-232 yang pertama ditentukan pula panjang kabel tidak boleh lebih dari 15 Meter (50 feet), tapi ketentuan ini di telah di revisi pada standar RS-232 versi 'D'. Dalam ketentuan baru ini tidak lagi ditentukan

panjang kabel maksimum, tapi ditentukan nilai kapasitansi dari kabel tidak boleh lebih besar dari 2500 pF, sehingga dengan menggunakan kabel kualitas baik, bisa dicapai jarak lebih dari 50 feet.

2.3.2. Konektor Dan Jenis Sinyal RS-232

Standar RS-232 menentukan pula jenis – jenis sinyal yang dipakai mengatur pertukaran informasi, semuanya terdapat 24 jenis sinyal tetapi yang umum dipakai hanyalah 9 jenis sinyal. Konektor yang dipakai pun ditentukan dalam standar RS-232, untuk sinyal lengkap dipakai konektor DB25 (25 pin), sedangkan konektor DB9 hanya dipakai untuk 9 sinyal yang umum dipakai seperti yang ditunjukkan pada gambar 2.11.

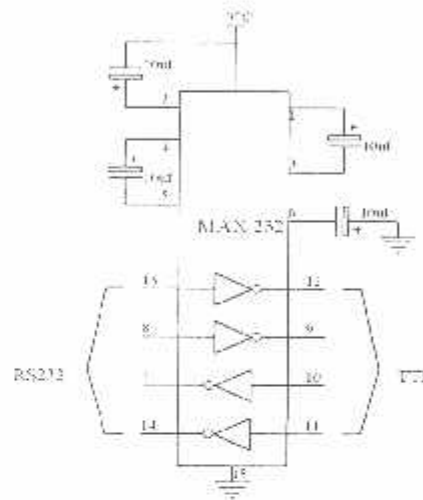


Gambar 2.11 Konfigurasi Pin RS-232 (Female)^[6]

2.3.3. RS-232 Level Converter

IC digital, termasuk mikrokontroler, umumnya memakai level tegangan TTL yang berbeda dengan level tegangan RS-232. Dengan

demikian dalam membentuk saluran RS-232 diperlukan pengubahan level tegangan timbal balik antara RS-232 – TTL. Dalam perancangan ini digunakan IC MAX232 yang didalamnya berisikan 2 line driver dan 2 line receiver serta terdapat pengubah sumber tegangan DC, sehingga meskipun catu daya untuk IC MAX232 hanya +5 volt, tetapi sanggup melayani level tegangan RS232 yang berkisar antara -12 volt sampai +12 volt.



Gambar 2.12 Konverter TTL – RS-232^[6]

2.4. Komunikasi Serial RS-485

Ditinjau dari standar elektronik, dewasa ini dikenal dua macam saluran data, yang pertama adalah transmisi saluran tunggal (*single-ended/unbalanced data transmission*) yang dipakai oleh RS-232, dan saluran data yang kedua adalah saluran ganda (*differential-balanced data transmission*) yang dipakai oleh RS-485.

2.4.1. RS-485

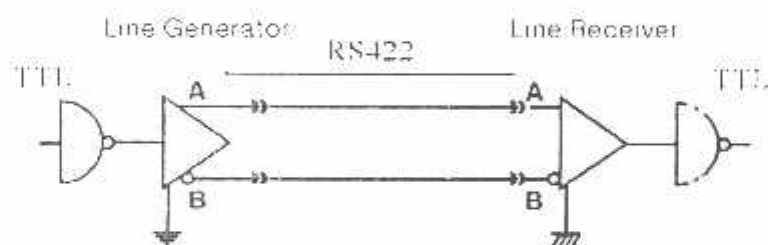
Standar RS-485 ditetapkan oleh *Electronic Industry Association* dan *Telecommunication Industry Association* pada tahun 1983. Nama lengkapnya adalah *EIA/TIA-485 Standard for Electrical Characteristics of Generators and Receivers for use in a Balanced Digital Multipoint System*. Standar RS-485 hanya membicarakan tentang karakteristik sinyal elektrik pada sistem, tidak menyebutkan tentang protokol. Jadi standar RS-485 dikatakan belum lengkap, tidak seperti halnya dengan standar RS-232 yang mencakup ketentuan tentang karakteristik sinyal, macam-macam sinyal dan konektor yang dipakai, serta konfigurasi sinyal pada kaki-kaki di konektor dan juga penentuan tata cara pertukaran informasi (protokol) antara komputer dan alat-alat pelengkap, sehingga dalam merancang suatu sistem yang berdasar pada komunikasi RS-485, baik tata cara komunikasi ataupun kecepatan transmisinya akan berbeda – beda tergantung seorang perancang.

Pada tabel 2.4, ditunjukkan ringkasan perbedaan antara RS-232 dan RS-485.

Tabel 2.4 Perbandingan RS-232 dan RS-485^[6]

	RS-232	RS-485
<i>Differential</i>	Tidak	Ya
Jumlah <i>driver</i> maksimum	1	32
Jumlah <i>receiver</i> maksimum	1	32
Jenis komunikasi data	Half Duplex Full Duplex	Half Duplex
Topologi jaringan	Point to point	Multipoint
Jarak maksimum (standar)	15 m	1200 m
Transfer rate maksimal pada 15 m	20 KBps	55 MBps

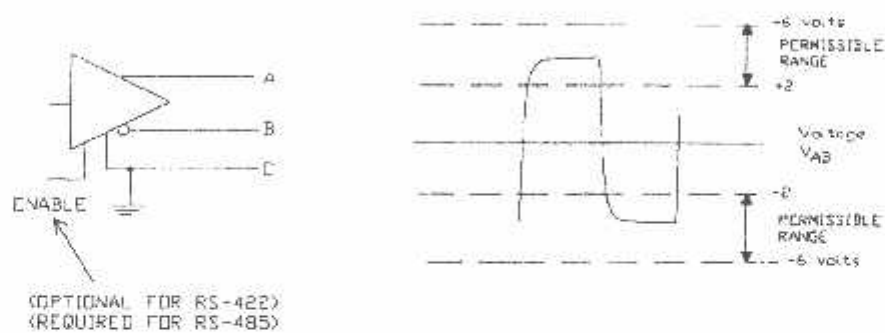
RS-485 menggunakan pensinyalan secara differential seperti yang ditunjukkan pada gambar 2.13. Jika ada gangguan listrik yang menimpa saluran transmisi, maka induksi tegangan yang diterima kedua utas kabel saluran dari gangguan akan sama besarnya. Karena Line Receiver membandingkan selisih tegangan antara dua utas kabel, maka induksi tegangan yang sama besarnya tersebut tidak pernah dirasakan oleh input Line Receiver, sehingga tidak akan berpengaruh pada outputnya. Untuk meningkatkan kekebalan terhadap gangguan, dalam saluran ganda sering dipakai dua utas kabel yang dililit menjadi satu (twist-pair cable).



Gambar 2.13 RS-485^[7]

Dengan cara ini, maka saluran ini dapat digunakan dalam jarak yang jauh dan kekebalan noise yang lebih baik dibandingkan dengan RS-232. RS-485 ini dapat dipakai untuk saluran sejauh 4000 feet atau sekitar 1200 meter dengan kecepatan transfer data hingga 35 Megabit/detik (Mbps). Kecepatan hingga 35 Mbps pada saluran sejauh 10 meter dan 100 kbit/detik pada jarak 1200 meter.

Pada gambar 2.14, ditunjukkan mengenai simbol skematik dan tegangan dari driver pada RS-485. Informasi logika akan ditafsirkan dari beda tegangan antara 2 utas kabel saluran. Tegangan pada kedua utas kabel saluran selalu berbeda, saat satu kabel bertegangan tinggi maka kabel yang lain akan bertegangan lebih rendah, demikian pula sebaliknya. Rangkaian penerima sinyal (receiver) akan membandingkan tegangan kedua kabel saluran sehingga level logika pada bagian output akan ditentukan oleh kabel mana yang lebih positif.



Gambar 2.14 Level Tegangan Driver RS-485^[5]

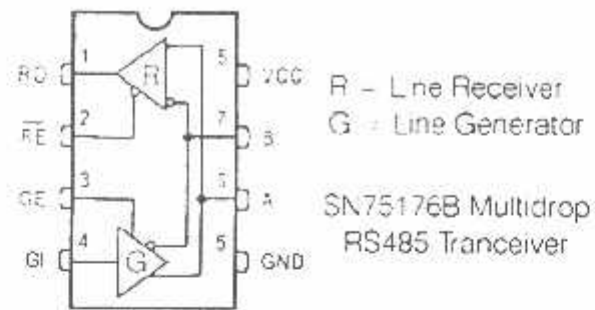
Driver menghasilkan tegangan berkisar antara 2 hingga 6 volt melalui output terminal A dan B, dan juga memiliki sinyal ground C. Meskipun sinyal ground ini berfungsi penting, tetapi receiver tidak menggunakannya untuk mendeteksi keadaan logika dalam saluran. Driver juga memiliki input sinyal yang disebut “Enable” sinyal. Tujuan dari sinyal ini adalah untuk menghubungkan keadaan driver tersebut kepada terminal outputnya, A dan B.

Jika “Enable” sinyal adalah OFF, maka driver dianggap terputus dari saluran transmisi.

Receiver pada RS-485, harus mendeteksi perbedaan tegangan sebesar 200 mV pada kedua line. Jika line A memiliki tegangan paling sedikit 200 mV lebih besar dari line B maka output receiver memiliki logika “high”. Jika line B bertegangan paling sedikit 200 mV lebih besar dari line A maka output memiliki logika “low”. Output tidak akan terdefinisikan jika perbedaan antara kedua line kurang dari 200 mV.

2.4.2. IC SN75176B

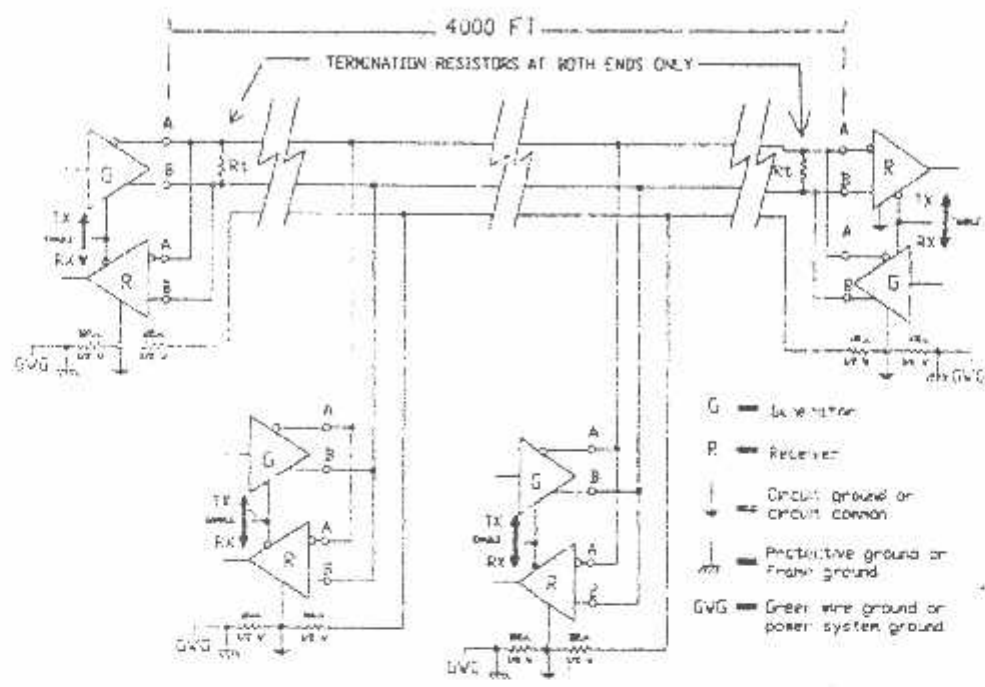
Texas Instrument membuat IC yang dirancang khusus untuk memenuhi ketentuan RS-485, IC tersebut dinamakan sebagai SN75176B Multipoint RS485 Transceiver. IC ini yang sangat terkenal dan banyak pabrik IC lainnya memproduksi IC sejenis dengan seri nomor yang sama. Di dalam SN75176B terdapat sebuah Line Generator dan sebuah Line Receiver yang dirangkai seperti terlihat dalam Gambar 2.15. Output dari Line Generator bisa di-ambang-kan (high impedance state) dengan memberi ‘0’ pada input GE, kemampuan ini dimaksudkan untuk menunjang keperluan dalam membentuk rangkaian saluran komunikasi multi-drop dimana hanya boleh ada satu Line Generator yang aktif pada suatu waktu, jadi tidak boleh ada dua atau lebih Line Generator yang aktif pada saat yang bersamaan.



Gambar 2.15 IC SN75176^[8]

2.4.3. Komunikasi Multi-drop (multi-drop/multi-point communication)

Dalam prakteknya, saluran ganda tidak dipakai untuk transmisi yang memerlukan banyak saluran, mengingat RS-485 memakai kabel yang jauh lebih banyak sehingga mahal. Untuk penghematan kabel, saluran ganda dipakai untuk saluran half-duplex, yakni saluran dua arah secara bergantian yang hanya menggunakan satu pasang kabel, dimana bisa dipakai untuk menghubungkan banyak Line Generator dan banyak Line Receiver menjadi satu (hanya satu unit driver/transmitter yang mengirimkan data dalam suatu waktu). Sistem ini disebut sebagai komunikasi multi-drop (multi-drop/multi-point communication).



Gambar 2.16 Topologi Jaringan Multi-drop RS-485^[5]

Berdasarkan topologi tersebut, pada saluran bisa dipasangkan sebanyak-banyaknya 32 chip SN75176B Multi-drop RS485 Transceiver, kaki A (kaki nomor 6) dari masing-masing IC harus dihubungkan pada seutas kabel pembentuk saluran yang sama, dan kaki B (kaki nomor 7) dihubungkan ke kabel yang lain.

Karena saluran dipakai bersama oleh banyak transceiver, agar output Line Generator dari masing-masing transceiver tidak berbenturan, dalam rangkaian saluran komunikasi multidrop ditentukan semua output Line Generator harus dalam keadaan non-aktif ($GE=0$, mengambang – high impedance state), kecuali Line Generator dari transceiver yang berfungsi sebagai induk (Master) yang boleh aktif ($GE=1$).

Saat beroperasi Master secara bergiliran akan menghubungi Slave, setelah itu Master me-nonaktif-kan Line Generatornya, Slave yang terpanggil akan meng-aktif-kan Line Generatornya dan mengirimkan informasi ke saluran, setelah itu Slave tersebut me-nonaktif-kan kembali Line Generatornya dan kembali Master meng-aktifkan generator untuk menghubungi Slave yang lain.

Dengan demikian Master berfungsi untuk mengendalikan saluran, dan komunikasi yang terjadi di saluran adalah komunikasi half-duplex, yakni komunikasi dua arah secara bergantian.

Meskipun kerja dari Line Receiver tidak memerlukan ground, tapi untuk menjamin agar pertukaran sinyal antara transceiver bisa terjadi dengan baik, biasanya disamping sepasang kabel sinyal, pada saluran multidrop ditambah lagi seutas kabel ground.

BAB III

PERANCANGAN DAN PEMBUATAN PERALATAN

Dalam bab ini akan dibahas mengenai perancangan dan pembuatan peralatan pada sistem antrian nasabah bank yang menggunakan mikrokontroler AT89S51 dengan komputer sebagai server.

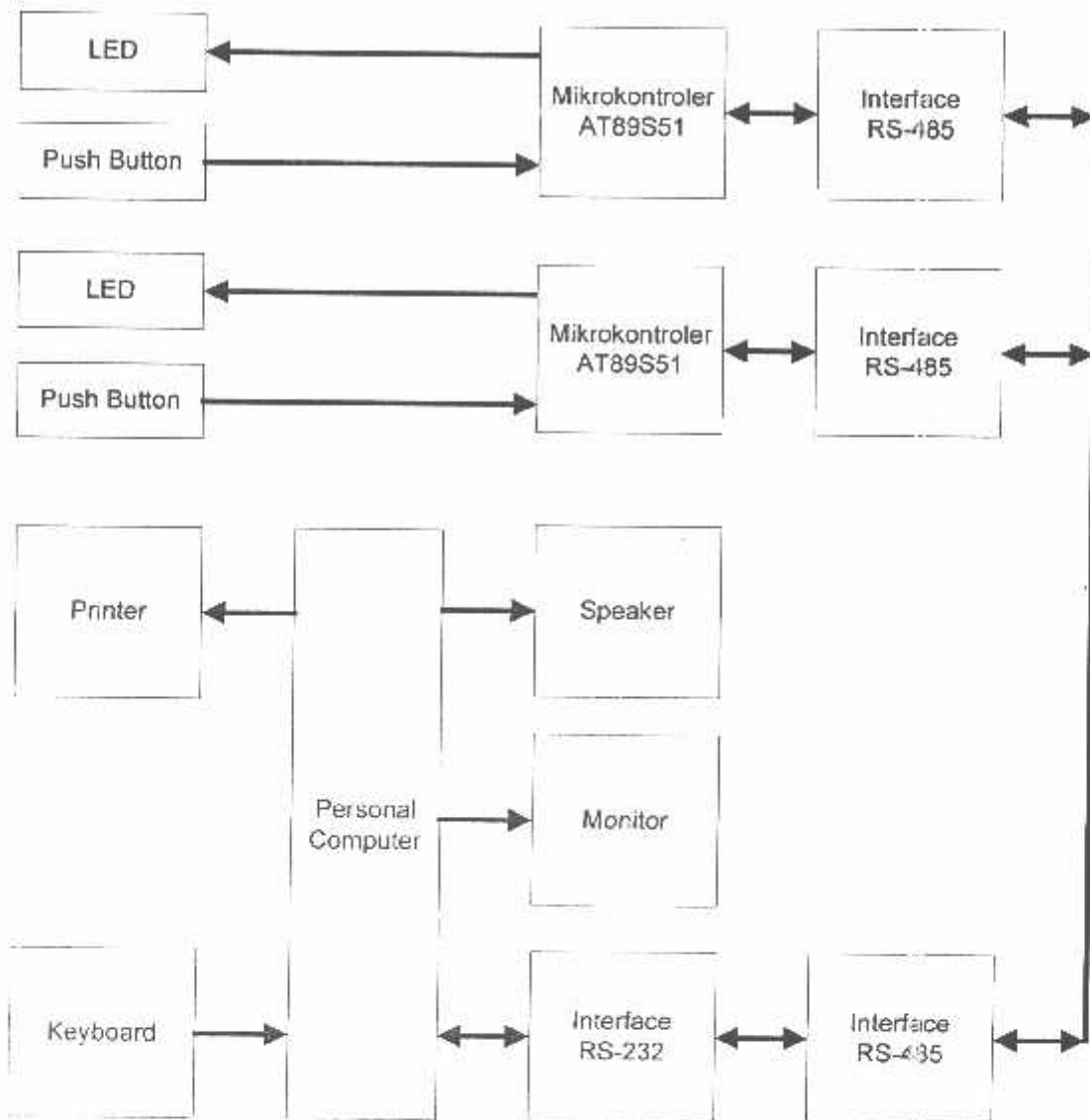
Pembahasan yang dilakukan dibagi menjadi 2 bagian besar, yaitu :

- Perancangan dan pembuatan perangkat keras (*Hardware*)
- Perancangan dan pembuatan perangkat lunak (*Software*)

Perancangan perangkat keras meliputi seluruh komponen yang digunakan pada sistem ini, sedangkan pada perancangan perangkat lunak meliputi *flowchart* dari *software* secara umum. Kedua perangkat tersebut dalam kerjanya akan saling menunjang satu sama lain.

3.1. Perancangan Perangkat Keras

Secara umum blok diagram Sistem Antrian Nasabah Bank Berbasis Personal Computer Menggunakan RS-485 adalah sebagai berikut:



Gambar 3.1 Blok Diagram Sistem

Fungsi dari masing-masing blok adalah sebagai berikut:

1. Tombol Push-button

Berfungsi untuk memberi input seting kepada mikrokontroler dengan menekan tombol-tombol sesuai prosedur.

2. LED

Berfungsi untuk memberikan status/kondisi dari tombol push-button.

3. Keyboard

Berfungsi sebagai inputan dari nasabah ke komputer.

4. Printer

Berfungsi untuk mencetak nomor urut antrian.

5. Monitor

Berfungsi sebagai output sistem secara visual kepada para nasabah.

6. Speaker

Berfungsi sebagai output sistem secara audio kepada para nasabah.

7. Personal Computer

Berfungsi sebagai master yang akan mengolah data dari sistem secara keseluruhan.

8. Interface RS-232

Sebagai rangkaian untuk mengkonversi tegangan TTL menjadi tegangan RS-232 ataupun sebaliknya.

9. Interface RS-485

Sebagai saluran untuk mentransmisikan data antara komputer dan mikrokontroler.

10. Mikrokontroler AT89S51

Berfungsi sebagai slave yang akan mengolah inputan tombol operasional dari operator, dan mentransmisikan data ke Personal Computer.

Prinsip Kerja Blok Diagram Sistem :

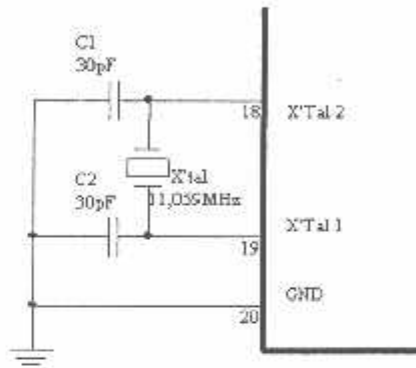
Pengendalian sistem dimulai dari tahap pensetingan sampai dengan komunikasi data. Akuisisi data dilakukan pertama – tama pada server/komputer melalui keyboard, dimana user menekan tombol pada keyboard sesuai prosedur. Selanjutnya data akan diolah didalam komputer, lalu komputer akan mentransmisikannya melalui saluran transmisi RS-485 sesuai perintah yang diberikan pada *software*. Data tersebut dicetak oleh unit printer serta akan ditampilkan secara audio visual melalui layar televisi dan speaker yang tersedia. Proses selanjutnya mikrokontroler akan menunggu data yang di-input-kan oleh operator melalui tombol push-button. Setelah data tersebut dibaca oleh mikrokontroler, didefinisikan, dan disimpan dalam register-register yang terdapat dalam mikrokontroler, kemudian mikrokontroler akan menunggu perintah dari komputer untuk mengirimkan data tersebut. Jika sudah ada perintah dari komputer untuk mentransmisikan data, maka mikrokontroler akan segera mengirimkan data tersebut melalui saluran RS-485 itu juga.

3.1.1. Perancangan Minimum Sistem AT89S51

Penggunaan mikrokontroler AT89S51 harus didukung oleh beberapa rangkaian penunjang agar dapat melakukan fungsinya. Rangkaian penunjang tersebut diantaranya adalah rangkaian *clock* dan rangkaian reset. Selain itu juga harus ditentukan penggunaan port-portnya untuk rangkaian pendukung yang lain yaitu untuk *led* dan *push-button*.

3.1.1.1. Rangkaian Clock

Pada mikrokontroler AT89S51 terdapat *internal clock generator* yang berfungsi sebagai sumber *clock*, tapi masih memerlukan rangkaian tambahan untuk membangkitkan *clock* yang diinginkan.



Gambar 3.2 Rangkaian Clock

Rangkaian tambahan ini terdiri atas 2 buah kapasitor dan sebuah kristal yang terangkai sedemikian rupa dan kemudian dihubungkan dengan port yang khusus tersedia pada mikrokontroler.

Dalam perancangan rangkaian ini menggunakan :

- 2 Kapasitor 30pF. Penentuan besarnya kapasitansi disesuaikan dengan spesifikasi pada data sheet.
- Kristal 11,0592 MHz.

Dengan demikian perhitungannya dapat dilihat sebagai berikut :

$$f = 11,0592 \text{ MHz}$$

$$T = \frac{1}{f}$$

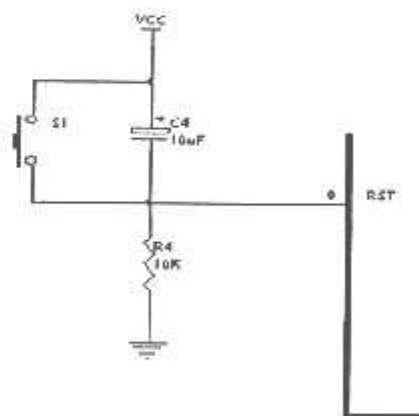
$$T = \frac{1}{11,0592 \times 10^6}$$

karena 1 siklus mesin = 12T, maka :

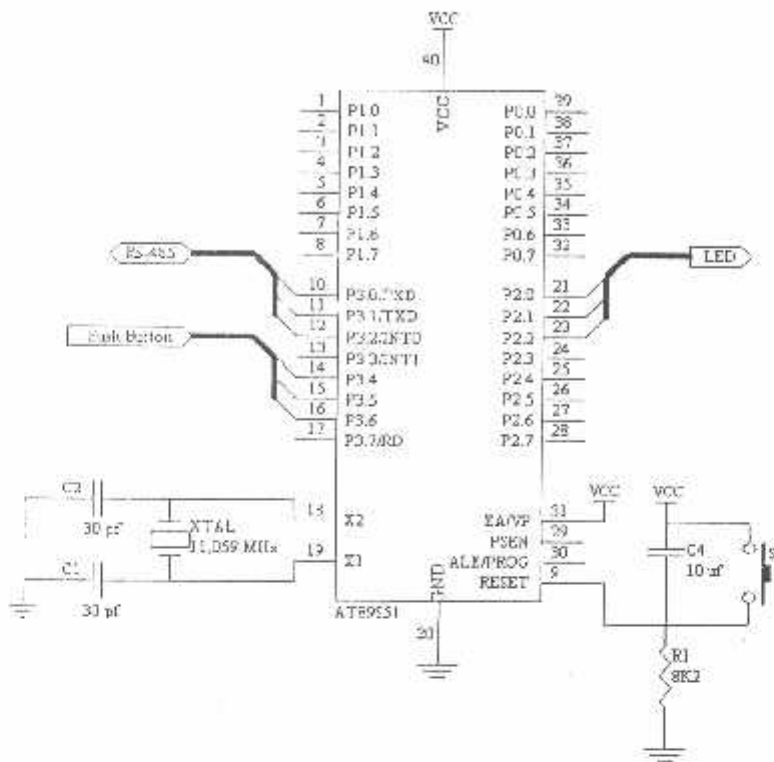
$$1 \text{ siklus mesin} = 12 \times \frac{1}{11,0592 \times 10^6} = 1,085 \mu\text{s} \approx 1 \mu\text{s}$$

3.1.1.2. Rangkaian Reset

Reset pada mikrokontroler merupakan masukan aktif *high* '1'. Pulsa transisi dari rendah '0' ke tinggi '1' selama 2 siklus mesin akan *reset* mikrokontroler menuju alamat 0000H. Pin *reset* dihubungkan dengan rangkaian *power-on reset* seperti pada gambar berikut :



Gambar 3.3 Rangkaian Reset



Gambar 3.4 Perancangan Pemakaian Port-port AT89S51

Keterangan :

1. Port 2.0 s/d port 2.3 digunakan untuk led sebagai ouput dari mikrokontroler.
2. Port 3.0 s/d port 3.2 dihubungkan ke saluran transmisi RS-485.
3. Port 3.4 s/d port 3.6 digunakan oleh push button sebagai inputan ke mikrokontroler.
4. Pin 9 dihubungkan dengan rangkaian *reset*.
5. Pin 18 dan 19 dihubungkan ke rangkaian *clock*.
6. Pin 40 dihubungkan dengan tegangan DC $\pm 5V$.
7. Pin 20 digunakan sebagai *ground* Mikrokontroler.

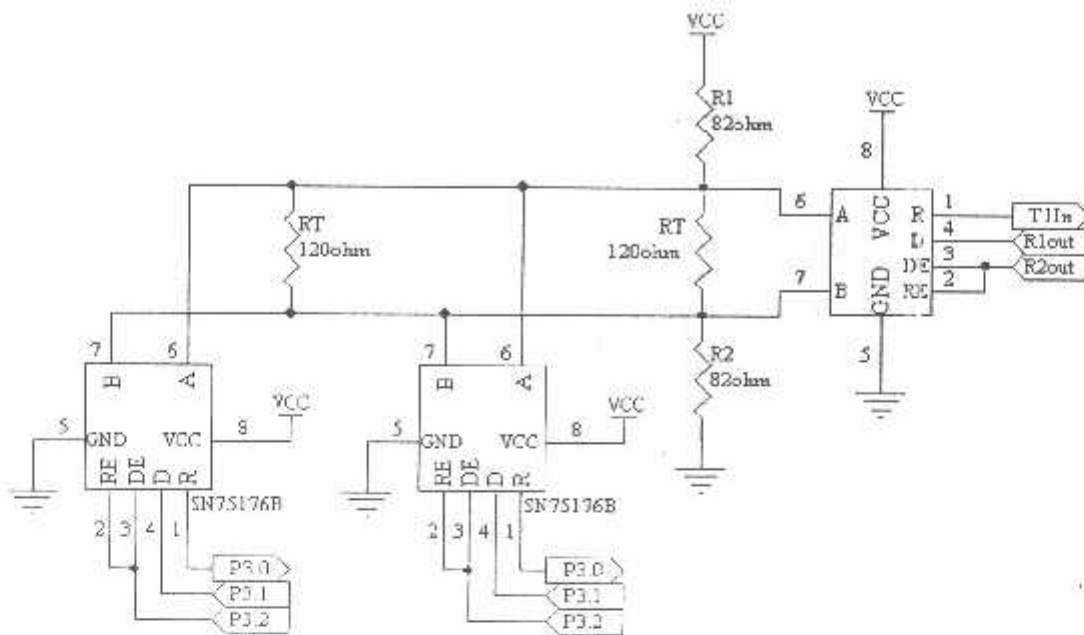
3.1.3. Rangkaian Interface RS-485

Saluran transmisi standar RS-485 merupakan media komunikasi data yang mempunyai jangkauan hingga mencapai jarak 4000 kaki (1200m) dan merupakan jaringan *multipoint* yang dapat memiliki lebih dari satu *driver* dan atau *receiver* didalamnya.

Pada rancangan rangkaian ini terdapat tiga buah node/titik, yaitu titik komputer sebagai *master* dan dua buah titik lainnya yaitu mikrokontroler, berfungsi sebagai *slave*. Pada titik mikrokontroler, port komunikasi serialnya bekerja pada level tegangan TTL, sehingga dapat langsung dihubungkan dengan port masukan dan keluran dari IC SN75176B yang berfungsi sebagai *driver* dan *receiver* dalam komunikasi RS-485. Sedangkan pada titik komputer, port komunikasi serial yang digunakannya bekerja pada level tegangan RS-232 sehingga memerlukan pengubahan level tegangan ke level tegangan TTL menggunakan IC MAX232, sebelum dihubungkan dengan port masukan dan keluaran dari IC SN75176B.

3.1.3.1. Perancangan Topologi Jaringan Standar RS-485

Topologi jaringan *multipoint* RS-485 yang direncanakan ditunjukkan pada gambar 3.5.



Gambar 3.5 Perencanaan Topologi Jaringan RS-485

Pada rangkaian terdapat 3 buah IC SN75176B yang berfungsi sebagai RS-485 *Transceiver*, kaki A (kaki nomor 6) dari masing-masing IC harus dihubungkan pada seutas kabel pembentuk saluran yang sama, dan kaki B (kaki nomor 7) dihubungkan ke kabel yang lain.

Karena saluran dipakai bersama oleh banyak transceiver, agar output *driver* dari masing-masing transceiver tidak berbenturan, dalam rangkaian saluran jaringan ditentukan bahwa semua output *driver* harus dalam keadaan non-aktif ($DE=0$), kecuali *driver* dari transceiver yang berfungsi sebagai induk (*Master*) yang boleh aktif ($DE=1$).

Pada saat beroperasi, *master* (komputer) secara bergilir menghubungi *slave* (mikrokontroler), setelah itu *master* me-nonaktif-kan *driver*-nya, *slave* yang terpanggil akan meng-aktif-kan *driver*-nya dan

mengirimkan informasi ke jaringan, setelah itu *slave* tersebut menonaktifkan kembali *driver*-nya dan kembali *master* mengaktifkan *driver*-nya untuk mengirimkan data.

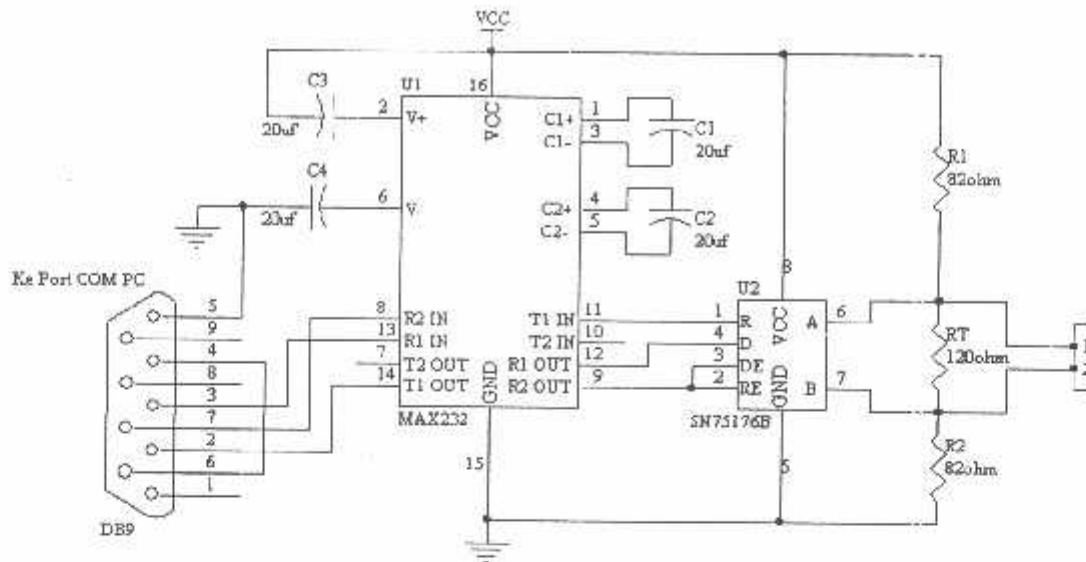
Dengan demikian *master* berfungsi untuk mengendalikan jaringan, dan komunikasi yang terjadi pada saluran adalah komunikasi *half-duplex*, yaitu komunikasi dua arah secara bergantian.

Pada saat pergantian aktivitas *driver* antara *master* dan *slave*, bisa terjadi satu saat secara bersamaan semua *driver* tidak aktif, akibatnya saluran menjadi mengambang dan keadaan logika dari saluran tidak menentu. Untuk mencegah terjadinya hal tersebut, pada saluran ditambahkan 2 buah resistor yang masing-masing bernilai 82 Ohm, resistor yang terhubung ke A dihubungkan ke +5 Volt dan resistor yang terhubung ke B dihubungkan ke *ground*, sehingga apabila semua *driver* tidak aktif bisa dipastikan saluran dalam keadaan '1'.

3.1.3.2. Rangkaian Interface RS-485 Dengan Port Serial Komputer

Rangkaian *interface* RS-485 dengan port serial komputer ditunjukkan dalam gambar 3.6 berikut ini :





Gambar 3.6 Rangkaian Interface RS-485 dengan Port Serial Komputer

Interface saluran RS-485 di titik komputer dilakukan terlebih dahulu dengan mengkonversi level tegangan TTL ke level tegangan RS-232, ini disebabkan karena port serial komputer tidak bekerja pada level tegangan TTL, melainkan level tegangan RS-232. Oleh karena itu diperlukan komponen tambahan yang berfungsi untuk mengubah level tegangan TTL menjadi level tegangan RS-232, begitu juga sebaliknya. Komponen yang digunakan adalah IC MAX232, MAX232 memiliki sepasang terminal masukan dan keluaran yang bekerja pada level tegangan TTL, yang berhubungan langsung dengan sepasang terminal masukan dan keluaran yang bekerja pada level tegangan RS-232.

Sebagai saluran penerimaan data, keluaran TTL (R) IC SN75176B dihubungkan ke masukan TTL ($T1_{in}$) dari IC MAX232 lalu kemudian keluaran RS-232-nya ($T1_{out}$) dihubungkan ke terminal RxD (pin 2) dari

port serial komputer. Sedangkan sebagai saluran pengiriman data dari komputer, terminal TxD (pin 3) dari port serial komputer dihubungkan ke masukan RS-232 ($R1_{in}$) dari MAX232 lalu kemudian keluaran TTL-nya ($R1_{out}$) dihubungkan ke masukan TTL (D) dari SN75176B.

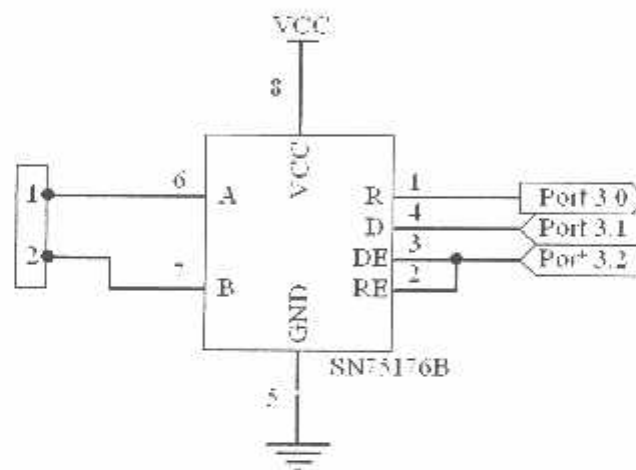
Dalam melakukan pengiriman maupun penerimaan data, komputer harus memberikan sinyal kontrol ke IC SN75176B. Untuk tujuan tersebut digunakan terminal RTS (pin7) dari port serial sebagai jalur sinyal kontrol. Terminal RTS ini dihubungkan dengan masukan RS-232 dari MAX232CPE, yaitu pin $R2_{in}$. Keluaran TTL-nya adalah $R2_{out}$ yang langsung dihubungkan dengan masukan TTL sinyal kontrol *driver* (DE) dan *receiver* (RE), sedangkan level logika sinyal kontrol ini diatur oleh program komputer. Sebelum komputer melakukan pengiriman data, program komputer harus membuat terminal RTS berlogika '1' (-3V s/d -15V) sehingga keluaran TTL pada $R1_{out}$ berlogika 1 untuk mengaktifkan *driver* saluran RS-485. Setelah pengiriman data selesai, program komputer sesegera mungkin membuat terminal RTS berlogika '0' (+3V s/d +15V) sehingga keluaran TTL $R1_{out}$ mengaktifkan *receiver* saluran sekaligus menonaktifkan *driver* saluran. Hal ini bertujuan untuk menghindari kemungkinan adanya lebih dari satu *driver* saluran yang aktif dalam satu jaringan yang dapat menyebabkan terganggunya saluran transmisi data.

Pada setiap rangkaian *interface* saluran transmisi RS-485 dalam jaringan disisipkan sebuah resistor terminasi (RT) yang besar

resistansinya disesuaikan dengan *datasheet* yaitu sebesar 120Ω . Resistor ini digunakan untuk menyesuaikan nilai impedansi karakteristik dari kabel jaringan yang digunakan. Dalam jaringan yang direncanakan ini, komputer akan bertindak menjadi *master*.

3.1.3.3. Rangkaian Interface RS-485 Dengan Port Serial AT89S51

Rangkaian *interface* mikrokontroler AT89S51 ke saluran transmisi RS-485 ditunjukkan dalam gambar 3.7.



Gambar 3.7 Rangkaian Interface RS-485 Dengan Port Serial AT89S51

Terminal A dan B dari SN75176B terhubung langsung ke saluran transmisi dua jalur. Keluaran TTL *receiver* (R) terhubung langsung ke terminal RxD mikrokontroler (port 3.0), sedangkan masukan TTL *driver* (D) terhubung langsung ke terminal TxD mikrokontroler pada port 3.1.

Kedua sinyal kontrol dari mikrokontroler bagi SN75176B, yaitu DE (*driver enable*) dan RE (*receiver enable*), dikeluarkan melalui port

3.2. Program mikrokontroler harus membuat port 3.2 berlogika tinggi untuk mengaktifkan *driver* sebelum mentransmisikan data, kemudian membuat port P3.2 berlogika rendah segera setelah pengiriman data selesai yang sekaligus mengaktifkan *receiver* sebelum menerima data yang ditransmisikan dari komputer. Dalam jaringan yang direncanakan ini, mikrokontroler bertindak menjadi *slave*.

3.2. Perancangan Perangkat Lunak

Perangkat lunak (*software*) yang direncanakan terdiri atas dua bagian, yaitu *software* untuk aplikasi pada komputer sebagai *master* dan *software* aplikasi mikrokontroler sebagai *slave*.

3.2.1. *Software* Mikrokontroler

Software mikrokontroler bertujuan untuk mengatur *input* dan *output*. Pekerjaan yang diatur oleh mikrokontroler adalah membaca inputan dari tombol operasional (*push-button*), menampilkan status led, serta mengatur transmisi data antara mikrokontroler dengan komputer.

Dalam jaringan yang direncanakan, mikrokontroler berfungsi sebagai *slave* sehingga apabila ada data yang akan dikirimkan, mikrokontroler harus dibuat menunggu panggilan dari komputer yang berposisi sebagai *master* sebelum mentransmisikan data. Setelah menerima panggilan untuk mengirimkan data, barulah mikrokontroler dapat mengirimkan data tersebut dan kemudian menunggu data balasan dari komputer.

Dalam proses komunikasi data antara mikrokontroler dengan komputer, terlebih dahulu ditentukan *baud rate* yang digunakan. Besarnya *baud rate* tergantung pada besarnya nilai *crystal* dan nilai TH1. Timer yang digunakan adalah Timer1 dalam mode 2 (*8bit-auto reload*). Jika besarnya *baud rate* yang dikehendaki adalah 1200bps, maka sesuai dengan persamaan dibawah, nilai dari TH1 dapat dicari dengan rumus :

$$TH1 = 256 - \left(\frac{2^{SMOD} \times F_{osc}}{384 \times BaudRate} \right)$$

Sehingga nilai TH1 :

$$TH1 = 256 - \left(\frac{2^0 \times 11,0592 \times 10^6}{384 \times 1200} \right)$$

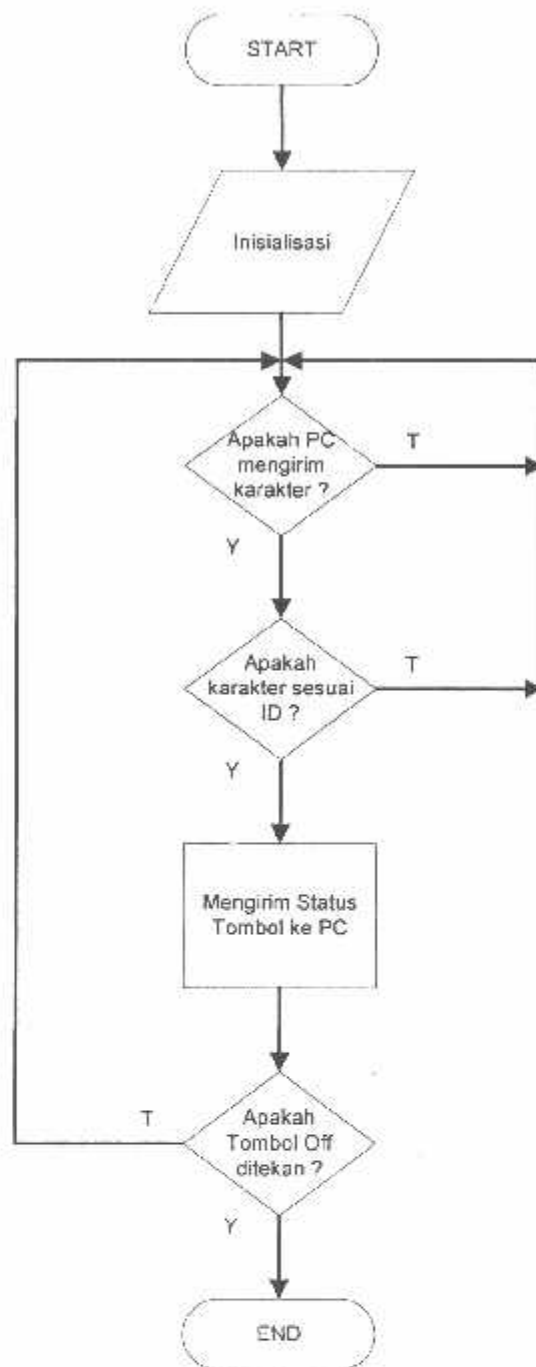
$$TH1 = 256 - \left(\frac{11,0592 \times 10^6}{460800} \right)$$

$$TH1 = 256 - 24$$

$$TH1 = 232d$$

$$TH1 = E8h$$

Flowchart dari program pada mikrokontroler ditunjukkan pada gambar berikut ini:



Gambar 3.8 Flowchart Program Mikrokontroler

3.2.2. *Software Personal Computer*

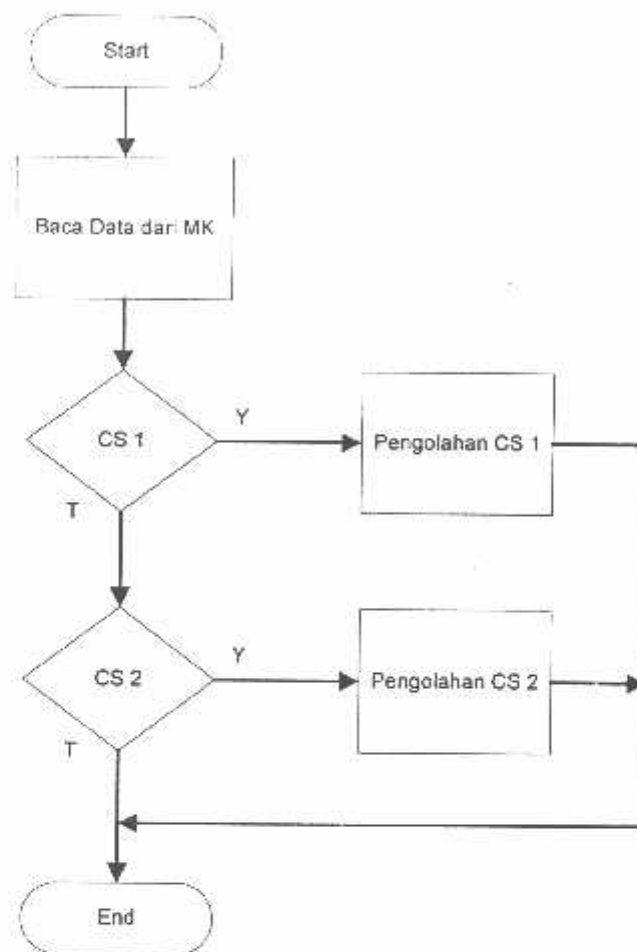
Pada dasarnya program komputer bertujuan untuk mengorganisir komunikasi yang terjadi antara komputer sebagai pengolah data dengan mikrokontroler, sehingga untuk merancang perangkat lunak dalam program komputer ditentukan terlebih dahulu aturan-aturan yang digunakan untuk mengatur jalannya komunikasi antara komputer dan mikrokontroler.

Pada program ini, komputer akan difungsikan untuk menerima data dari mikrokontroler dan juga dari keyboard, mengolah data tersebut, serta mengirimkan data yang diperlukan kepada mikrokontroler. Program dirancang sedemikian rupa sehingga apabila ada nasabah yang melakukan antrian dengan menekan tombol keyboard, maka nomor urut akan langsung dicetak, dan secara otomatis nasabah tersebut telah masuk dalam daftar antrian.

Prinsip kerja dari program ini adalah komputer yang diposisikan sebagai *master* secara bergilir akan memanggil alamat dari *client/slave* dan menunggu apakah ada data yang dikirim dari *client*. Jika ada data, komputer akan segera merespon dengan mengirimkan data yang dibutuhkan ke alamat *client* tersebut. dan jika tidak ada data, maka komputer akan terus menerus melakukan pemanggilan ke alamat *client* secara bergiliran.

Untuk program dalam perancangan ini dibuat dengan menggunakan *Borland Delphi 7.0* yang merupakan *software* pemrograman yang berorientasi pada objek (*object oriented programming*).

Flowchart pengiriman serta penerimaan data ke dan dari Personal Computer ditunjukkan pada gambar dibawah ini :



Gambar 3.9 Flowchart Program PC secara umum



Gambar 3.10 Flowchart Pengolahan Data Pada Customer Service

BAB IV

PENGUJIAN ALAT

Dalam bab ini dibahas tentang pengujian dan pengukuran dari peralatan yang dibuat. Secara umum pengujian ini bertujuan untuk mengetahui apakah alat yang telah direalisasikan dapat bekerja sesuai dengan perancangan atau tidak.

4.1. Pengujian Interface RS-232 Pada Titik Komputer

4.1.1. Tujuan Pengujian

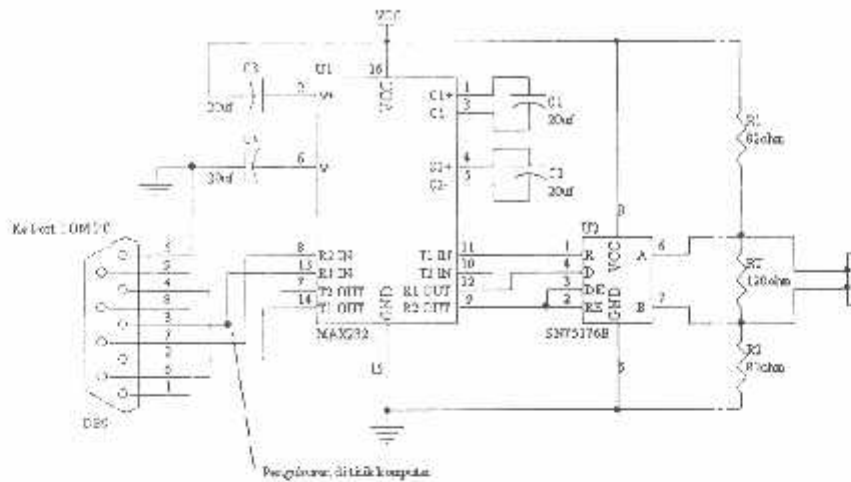
Pengujian ini bertujuan untuk mengetahui karakteristik dari tegangan RS-232.

4.1.2. Peralatan Yang Digunakan

1. Minimum sistem AT89S51
2. Rangkaian *Interface* RS-232
3. Komputer
4. Catu daya +5V
5. Multimeter
6. Osiloskop

4.1.3. Prosedur Pengujian

1. Menyusun semua peralatan yang dibutuhkan sesuai dengan gambar dibawah ini :



Gambar 4.1 Rangkaian Pengujian di titik komputer

2. Menjalankan *listing* program yang dibutuhkan :

```

procedure TForm1.Button5Click(Sender: TObject);
begin
  ComPort1.FlowControl.ControlRTS:=rtsDisable;
  sleep(5);
  Pengulang := 1;
  Repeat
    ComPort1.WriteStr('a');
    Application.ProcessMessages;
  until Pengulang = 2;
  sleep(100);
  ComPort1.ClearBuffer(true,true);
  ComPort1.FlowControl.ControlRTS:=rtsEnable;

end;

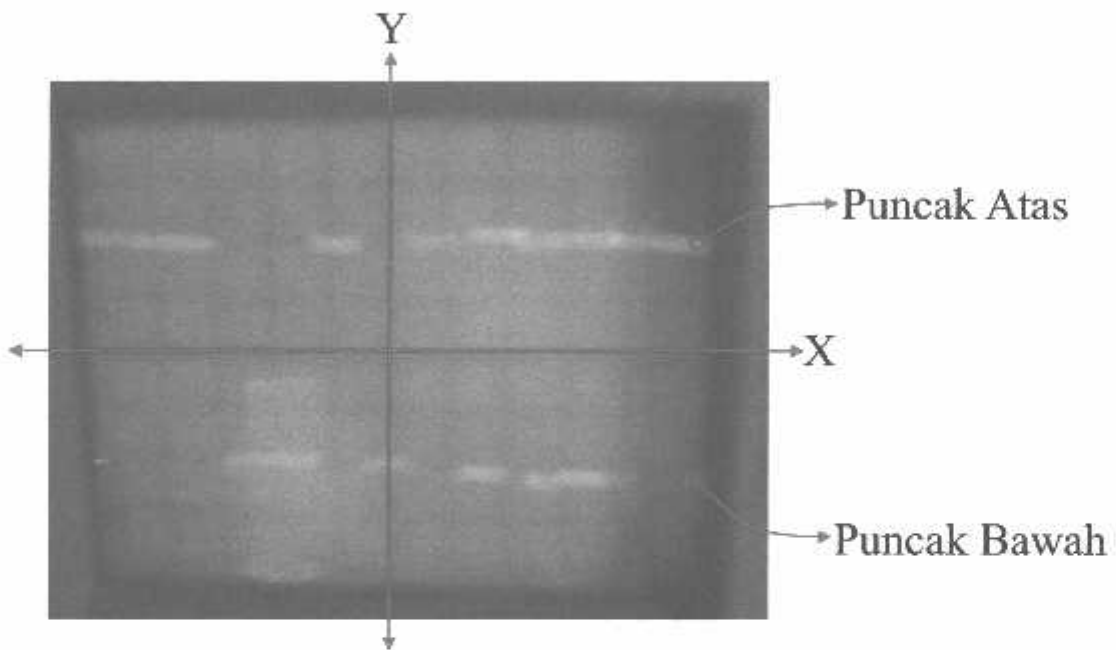
procedure TForm1.E7Click(Sender: TObject);
begin
  Pengulang := 2 ;
  Application.Terminate ;
end;

```

3. Menguji rangkaian dan mengukur besar tegangan input maupun output yang muncul pada titik komputer dengan melihat pada osiloskop.

4.1.4. Hasil Pengujian

Dari hasil pengujian yang terlihat pada osiloskop seperti gambar 4.2, didapatkan :



Gambar 4.2 Tampilan Osiloskop Untuk Level Tegangan RS-232

Dari gambar di atas :

Volt/div = 5 Volt

Time/div = 1 ms

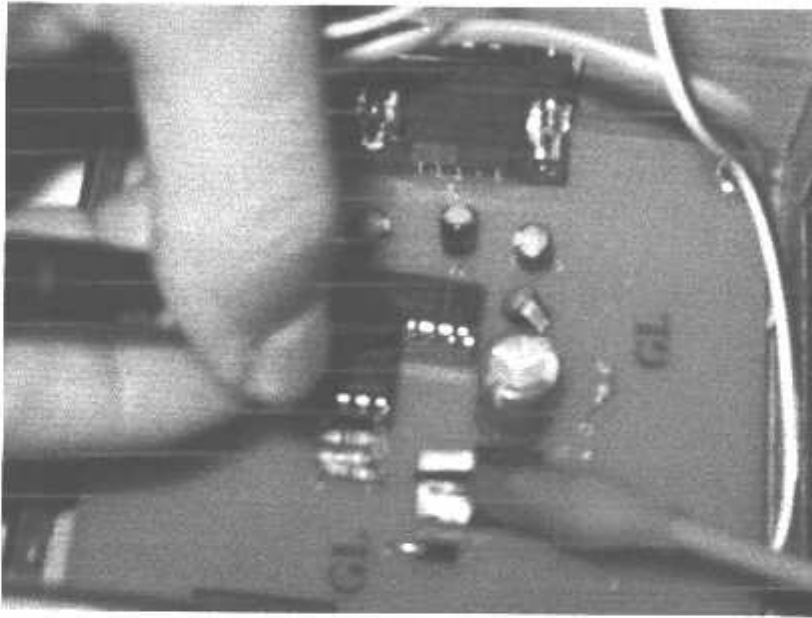
Tinggi = 4 kotak

Maka ;

Tegangan puncak $V_{pp} = 4 \times 5 = 20 \text{ V}$, atau

Batas atas = 10 V dan Batas bawah = 10 V.

Sehingga dapat disimpulkan bahwa tegangan di titik komputer adalah berkisar ± 10 V, yang sesuai dengan karakteristik level tegangan dari RS-232.



Gambar 4.3 Ilustrasi Pengukuran

4.2. Pengujian Interface RS-232

4.2.1. Tujuan Pengujian

Pengujian ini bertujuan untuk mengetahui karakteristik dari konverter tegangan RS-232 yang didalamnya terdapat IC MAX232.

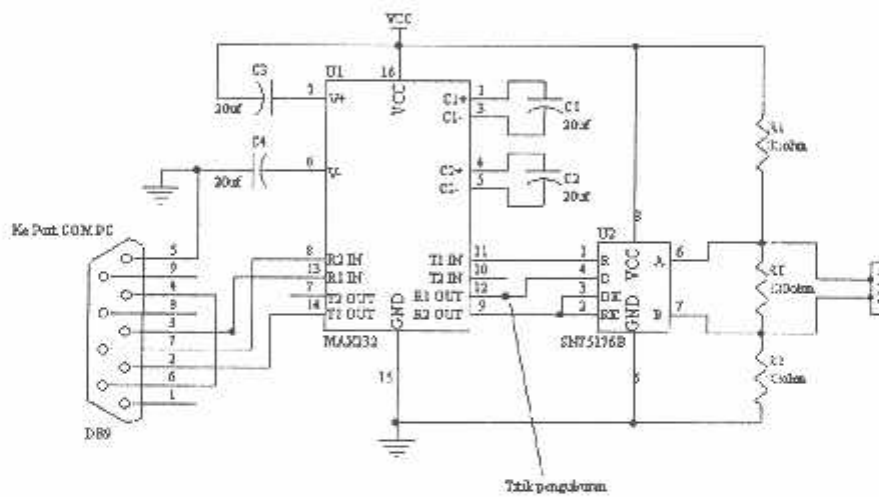
4.2.2. Peralatan Yang Digunakan

1. Minimum sistem AT89S51
2. Rangkaian *Interface* RS-232

3. Komputer
4. Catu daya +5V
5. Multimeter
6. Osiloskop

4.2.3. Prosedur Pengujian

4. Menyusun semua peralatan yang dibutuhkan sesuai dengan gambar dibawah ini :



Gambar 4.4 Rangkaian Pengujian Output MAX232

5. Menjalankan *listing* program yang dibutuhkan :

```

procedure TForm1.Button5Click(Sender: TObject);
begin
  ComPort1.FlowControl.ControlRTS:=rtsDisable;
  sleep(5);
  Pengulang :=1;
  Repeat
  ComPort1.WriteStr('a');
  Application.ProcessMessages;
  until Pengulang = 2;
  sleep(100);
  ComPort1.ClearBuffer(true,true);

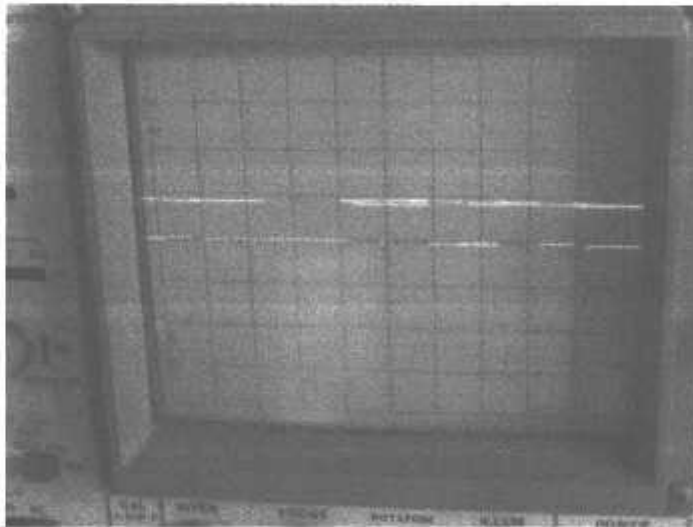
```

```
ComPort1.FlowControl.ControlRTS:=rtsEnable;  
end;  
  
procedure TForm1.E7Click(Sender: TObject);  
begin  
    Pengulang := 2 ;  
    Application.Terminate ;  
end;
```

6. Menguji rangkaian dan mengukur besar tegangan input maupun output yang muncul pada titik komputer dengan melihat pada osiloskop.

4.2.4. Hasil Pengujian

Dari hasil pengujian yang terlihat pada osiloskop seperti gambar 4.5, didapatkan :



Gambar 4.5 Tampilan Osiloskop

Volt/div = 5 Volt

Time/div = 1 ms

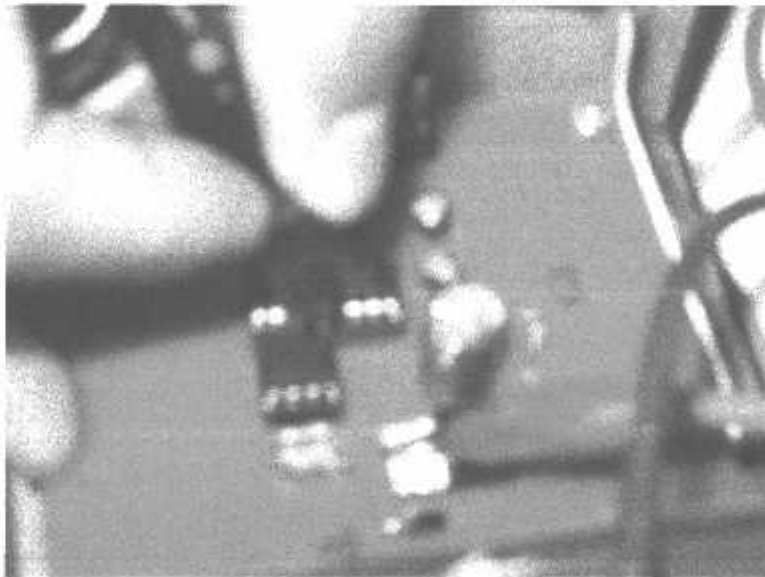
Tinggi = 1 kotak

Maka ;

Tegangan puncak $V_{pp} = 1 \times 5 = 5 \text{ V}$, atau

Batas atas = 5 V dan Batas bawah = 0 V.

Sehingga dapat disimpulkan bahwa tegangan di titik komputer adalah berkisar +5 V, yang sesuai dengan karakteristik level tegangan TTL.



Gambar 4.6 Ilustrasi Pengukuran

4.3. Pengujian Penerimaan dan Pengiriman Data

4.3.1. Tujuan Pengujian

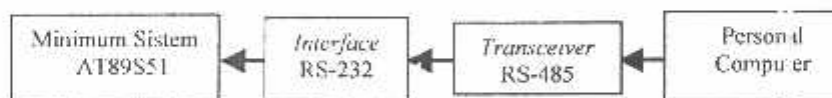
Pengujian ini bertujuan untuk mengetahui apakah komunikasi data yang terjadi antara mikrokontroler dan komputer melalui jaringan RS-485 dapat berjalan dengan baik atau tidak.

4.3.2. Peralatan Yang Digunakan

1. Minimum sistem AT89S51
2. Rangkaian *Interface* RS-232
3. *Transceiver* RS485 (SN75176B)
4. Komputer
5. Catu daya +5V
6. Multimeter
7. Osiloskop

4.3.3. Prosedur Pengujian

1. Menyusun semua peralatan yang dibutuhkan sesuai dengan gambar dibawah ini :



Gambar 4.7 Blok Diagram Pengujian Penerimaan dan Pengiriman Data

2. Menjalankan *listing* program yang dibutuhkan :

```

procedure TForm1.Button5Click(Sender: TObject);
begin
  ComPort1.FlowControl.ControlRTS:=rtsDisable;
  sleep(5);
end;
  
```

```

Pengulang :=1;
Repeat
ComPort1.WriteString('a');
Application.ProcessMessages;
until Pengulang = 2;
sleep(100);
ComPort1.ClearBuffer(true,true);
ComPort1.FlowControl.ControlRTS:=rtsEnable;

end;

procedure TForm1.E7Click(Sender: TObject);
begin
    Pengulang := 2 ;
    Application.Terminate ;
end;

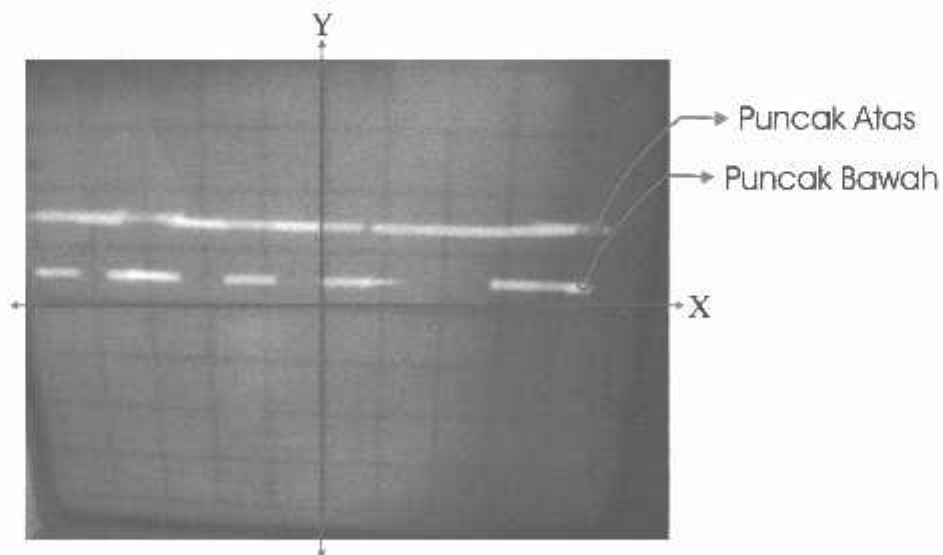
```

3. Menguji proses pengiriman data dan mengukur besar tegangan input maupun output yang muncul pada osiloskop.

4.3.4. Hasil Pengujian

Dari hasil pengujian yang terlihat pada osiloskop seperti gambar 4.8 dan gambar 4.10, didapatkan :

➤ Pada Jalur A :



Gambar 4.8 Tampilan Osiloskop Untuk Jalur A

Volt/div = 2 Volt

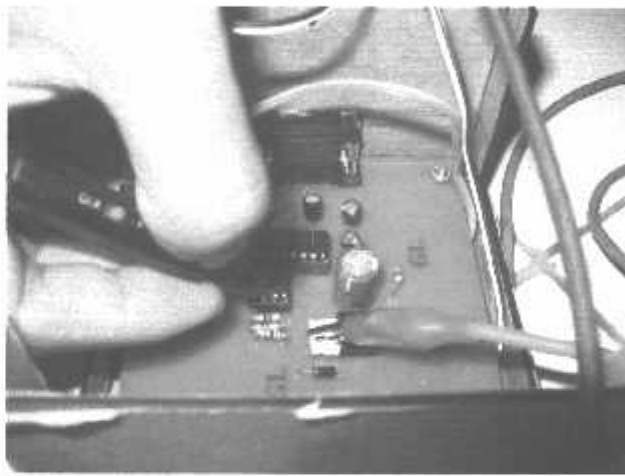
Time/div = 1 ms

Tinggi = 1,5 kotak

Maka ;

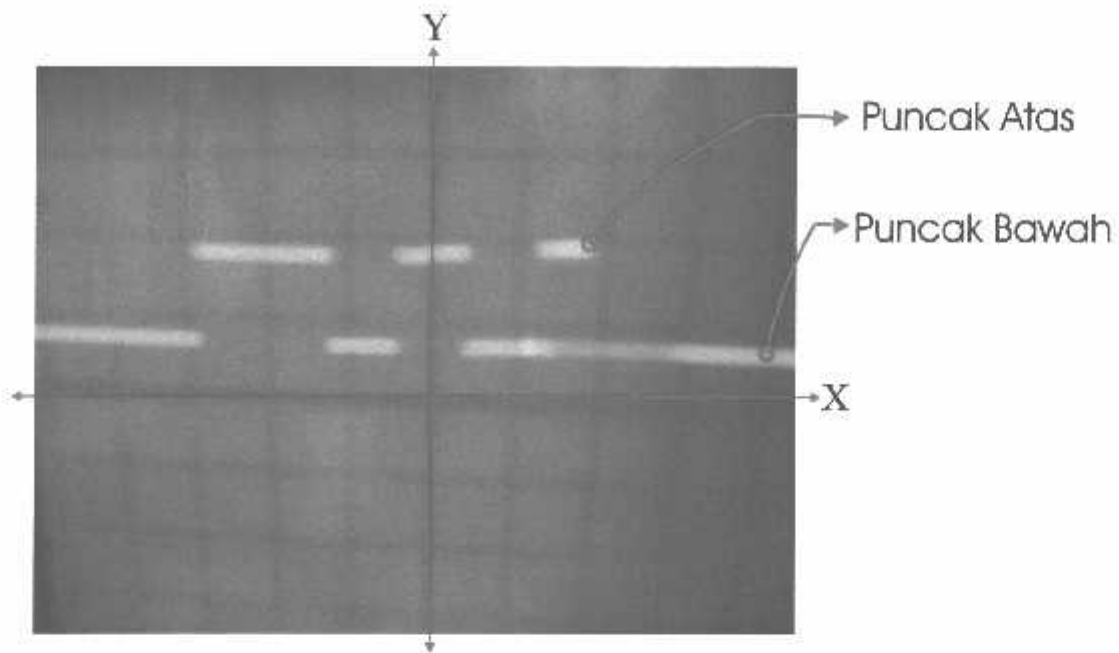
Tegangan puncak $V_{ppA} = 1,5 \times 2 = 3 \text{ V}$, atau

Batas atas = 3 V dan Batas bawah = 0 V



Gambar 4.9 Ilustrasi Pengukuran

➤ Pada Jalur B :



Gambar 4.10 Tampilan Osiloskop Untuk Jalur B

Dari gambar di atas :

Volt/div = 2 Volt

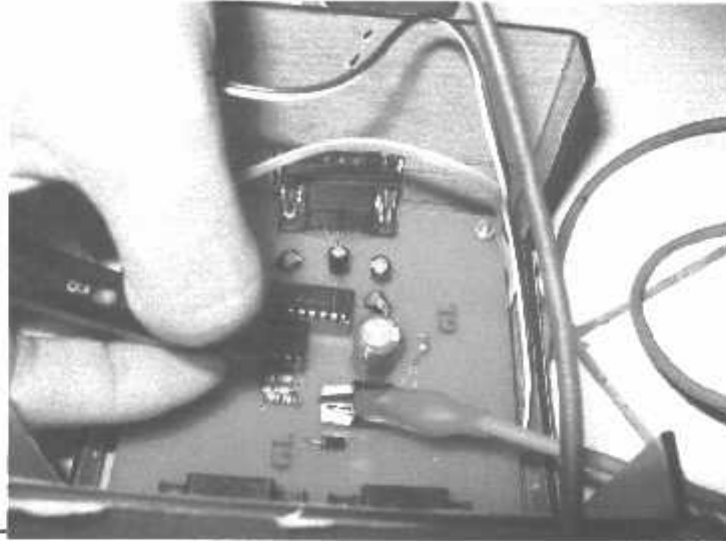
Time/div = 1 ms

Tinggi = 2 kotak

Maka ;

Tegangan puncak $V_{ppB} = 2 \times 2 = 4 \text{ V}$, atau

Batas atas = 4 V dan Batas bawah = 0 V



Gambar 4.11 Ilustrasi Pengukuran

Jadi selisih tegangan antara titik A dan B pada jalur RS-485 adalah sebesar 1 volt ($V_{ppA} - V_{ppB}$), yang berarti melampaui selisih tegangan minimum dari ketentuan RS-485 yang sebesar 200 mV.

4.4. Pengujian Keseluruhan Sistem

4.4.1. Tujuan Pengujian

Pengujian ini bertujuan untuk mengetahui apakah keseluruhan sistem yang direncanakan dapat bekerja dengan baik atau tidak.

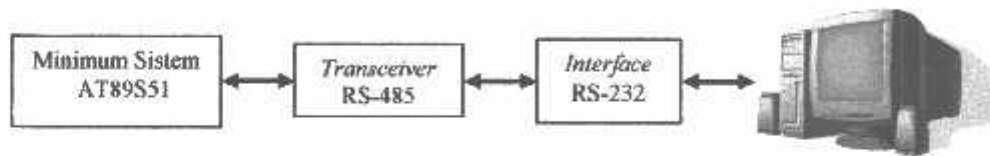
4.4.2. Peralatan Yang Digunakan

1. Minimum sistem AT89S51
2. Komputer
3. Keyboard

4. OPrinter
5. Speaker

4.4.3. Prosedur Pengujian

1. Menyusun semua peralatan yang dibutuhkan sesuai dengan gambar dibawah ini :

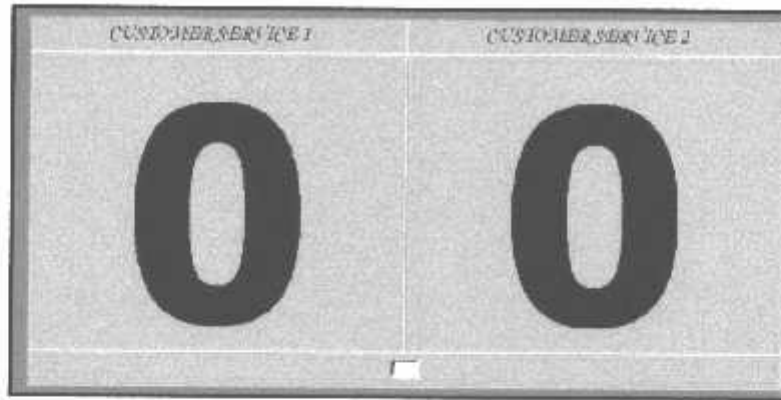


Gambar 4.12 Blok Diagram Pengujian Keseluruhan Sistem

2. Menjalankan program yang telah dibuat pada komputer.
3. Menguji hasil tampilan dari sistem secara keseluruhan.

4.4.4. Hasil Pengujian

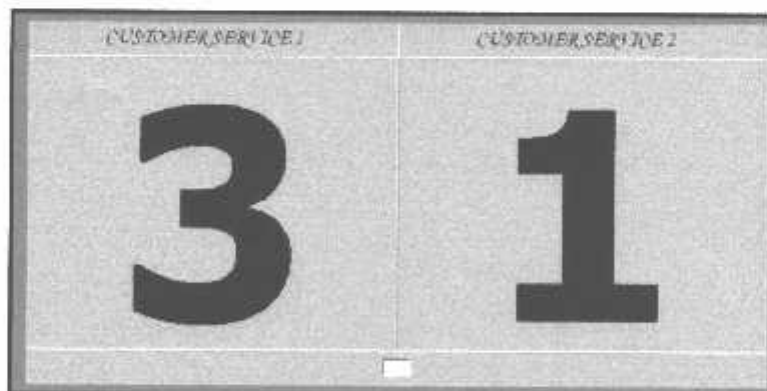
1. Menjalankan program yang telah dibuat pada komputer dan hasilnya terlihat seperti pada gambar 4.13



Gambar 4.13 Tampilan awal program

2. Menekan tombol *enter* untuk mulai memasukkan daftar antrian.
3. Unit *printer* langsung mencetak nomor urut antrian untuk nasabah.
4. Operator mulai memasukkan data melalui penekanan tombol *next*.

Selanjutnya antrian dimulai dan informasi terdengar pada speaker serta terlihat pada layar monitor, seperti yang terdapat pada gambar 4.14



Gambar 4.14 Tampilan Antrian Pada Layar Monitor

5. Jika pada saat antrian berlangsung, status salah satu operator tidak aktif atau tidak sedang melayani nasabah (melalui penekanan tombol *break*), misalnya status "CS 1" tidak aktif maka tampilan sistem akan terlihat seperti pada gambar 4.15



Gambar 4.15 Tampilan Sistem Saat Customer Service 1 kondisi "break"

BAB V

PENUTUP

5.1. Kesimpulan

Dari hasil perancangan dan pengujian alat yang telah dilakukan maka dapat ditarik kesimpulan sebagai berikut :

1. Pada saat pencetakan melalui unit printer, cara kerja sistem tidak terpengaruh, dalam arti sistem antrian berjalan lancar meskipun saat itu terjadi proses pencetakan nomor antrian.
2. Pada saat pemasukan data melalui tombol push-button oleh operator, tampilan LED sebagai status/penanda kondisi operator dapat dikatakan kurang efektif karena tidak secara terus menerus menunjukkan status dari tombol push-button.
3. Untuk keluaran audio terjadi tumpang tindih, ini disebabkan sistem hanya mampu mengolah satu perintah pengolahan suara dari satu client/slave pada saat yang sama.
4. Pengujian hubungan komunikasi serial pada mikrokontroler AT89S51 dan Personal Computer menunjukkan bahwa pengiriman dan penerimaan data telah berjalan dengan baik.
5. Sistem telah mampu memberikan tampilan antrian secara audio melalui speaker dan tampilan visual pada layar monitor kepada para nasabah.
6. Dari hasil pengujian membuktikan bahwa secara umum sistem dapat bekerja dengan baik serta dapat dioperasikan dan diaplikasikan secara

langsung, walaupun dalam pengujian terdapat hal – hal yang masih perlu mendapat perhatian lebih lanjut.

5.2. Saran – saran.

Dari hasil perencanaan dan pembuatan skripsi ini, perlu kiranya diberikan saran-saran guna kesempurnaan penyusunan skripsi selanjutnya. Adapun saran tersebut adalah sebagai berikut :

1. Sistem ini dapat dikembangkan lebih lanjut dengan saran untuk menambah spesifikasi hardwarenya.
 2. Memperbaiki pengolahan audio/suara dari sistem agar misalnya informasi yang berasal dari satu operator tidak akan tumpang tindih dengan operator yang lain, maksudnya hendaknya sistem suara dari masing – masing operator dapat berjalan secara terpisah.
 3. Untuk lebih mempermudah operator/customer service, dapat menggunakan seven segmen atau LCD untuk memperjelas status/kondisi tombol push-button.
 4. Untuk program utama pada PC, karena berjalan pada lingkungan sistem operasi microsoft windows yang multitasking, mungkin bisa diusahakan agar window dari program utama dari sistem tetap aktif.
 5. Sebelum dilakukan perencanaan dan pembuatan alat, sangatlah penting untuk melakukan kajian awal dengan tujuan untuk persiapan yang lebih dini sehingga nantinya tidak akan menimbulkan kendala-kendala yang bisa menghambat proses penyusunan skripsi selanjutnya.
-

Daftar Pustaka

- [1] Eko Putra, Agfianto, *"Belajar Mikrokontroler AT89C51/52/55 Teori dan Aplikasi"*, Penerbit Gava Media, Yogyakarta, 2002
 - [2] Andi Nalwan, Paulus, *"Panduan Praktis Teknik Antarmuka dan Pemrograman Mikrokontroler AT89C51"*, edisi kedua, Penerbit Elex Media Komputindo, Jakarta, 2003
 - [3] H.M, Jogyanto, *"Pengenaln Komputer"*, Penerbit ANDI, Yogyakarta
 - [4] <http://www.atmel.com>, *"Datasheet AT89S51"*
 - [5] <http://www.bb-elec.com>, *"rs422 485 app note"*
 - [6] *"Application Report: 422 and 485 Standards overview and System Configurations"*, Texas Instruments, June 2002
 - [7] *"Designing RS-485 Circuits"*, <http://www.circuitcellar.com>, Issue 107 Juni 1999
 - [8] <http://www.national.com>
 - [9] <http://www.epanorama.net>
-

LAMPIRAN



FORMULIR BIMBINGAN SKRIPSI

ia : Agus Adi Wirawan
: 95.17.008
a Bimbingan : 26 Juni 2008 - 26 Desember 2008
l Skripsi : Perancangan dan Pembuatan Sistem Antrian Nasabah Bank
Berbasis Personal Computer Menggunakan RS-485

Tanggal	Uraian	Paraf Bimbingan
23/8/2008	Bab I & II (Kursi)	
2/2008 19	Bab III	
	Demmo	
9/2008 19	Seminar hasil	
20/2008 19	Bab IV & V	
20/2008 19	Revisi	

Malang,
Dosen Pembimbing I

Ir. F. Yudi Limpraptono, MT
Nip.Y. 103 9500 274

Forma S-4b



FORMULIR BIMBINGAN SKRIPSI

a : Agus Adi Wirawan
: 95.17.008
Bimbingan : 26 Juni 2008 – 26 Desember 2008
Skripsi : **Perancangan dan Pembuatan Sistem Antrian Nasabah Bank Berbasis Personal Computer Menggunakan RS-485**

Tanggal	Uraian	Paraf Bimbingan
22/8/2008	Bab I (Revisi latar belakang)	
25/8/2008	Bab II (Revisi penulisan pustaka)	
27/8/2008	Bab II (Revisi dasar teori)	
30/8/2008	Bab III (Revisi penulisan)	
1/9/2008	Bab IV (Revisi)	
3/9/2008	Demo	
5/9/2008	Seminar Hasil	
15/9/2008	Bab IV dan Bab V	
20/9/2008	ACC Ujian skripsi	

Malang,
Dosen Pembimbing II

Ir. Yusuf Ismail Nakhoda, MT
Nip.Y. 101 8800 189

Form S-4b

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentrasi T. Energi Listrik / T. Elektronika / T. Infokom, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA

ABUS ADI W

NIM

95.17.008

Perbaikan meliputi

① jelaskan kembali gbr foto Casodascope!

Malang, 23-09-2008


(Rumay S. S. S. S.)

5

- e with MCS[®]-51 Products
- f In-System Programmable (ISP) Flash Memory
- ance: 1000 Write/Erase Cycles
- V Operating Range
- c Operation: 0 Hz to 33 MHz
- al Program Memory Lock
- t Internal RAM
- mmable I/O Lines
- t Timer/Counters
- upt Sources
- x UART Serial Channel
- r Idle and Power-down Modes
- Recovery from Power-down Mode
- j Timer
- Pointer
- Flag
- ramming Time
- SP Programming (Byte and Page Mode)

tion

51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K System Programmable Flash memory. The device is manufactured using high-density nonvolatile memory technology and is compatible with the industrial 80C51 instruction set and pinout. The on-chip Flash allows the program to be reprogrammed in-system or by a conventional nonvolatile memory programmer combining a versatile 8-bit CPU with In-System Programmable Flash on a single chip, the Atmel AT89S51 is a powerful microcontroller which provides a reliable and cost-effective solution to many embedded control applications.

51 provides the following standard features: 4K bytes of Flash, 128 bytes of internal RAM, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-level interrupt architecture, a full duplex serial port, on-chip oscillator, and more. In addition, the AT89S51 is designed with static logic for operation over a wide frequency range and supports two software selectable power saving modes. The Idle mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents by disabling the oscillator, disabling all other chip functions until the next external hardware reset.



8-bit Microcontroller with 4K Bytes In-System Programmable Flash

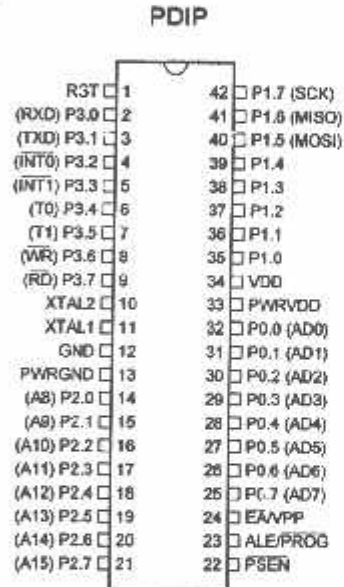
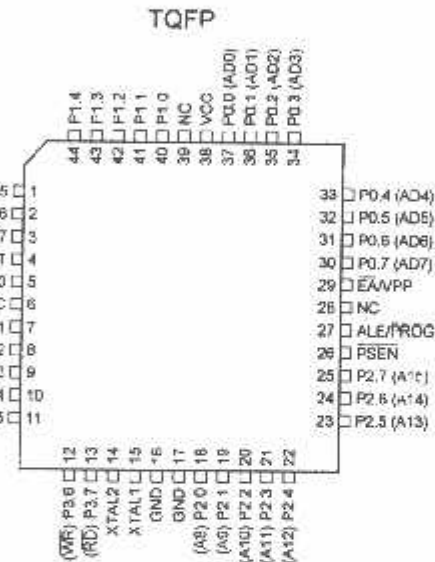
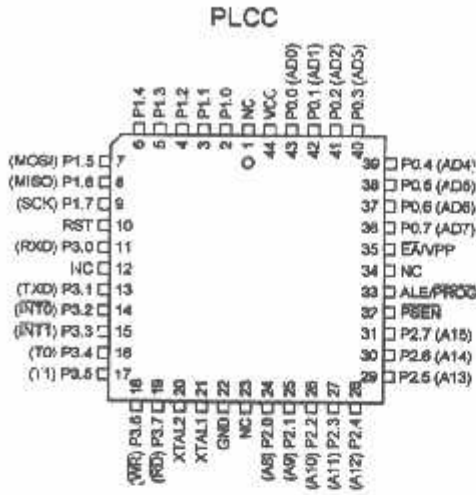
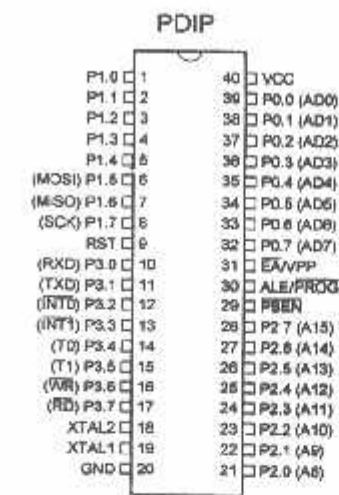
AT89S51

2487B-MICRO-12/03

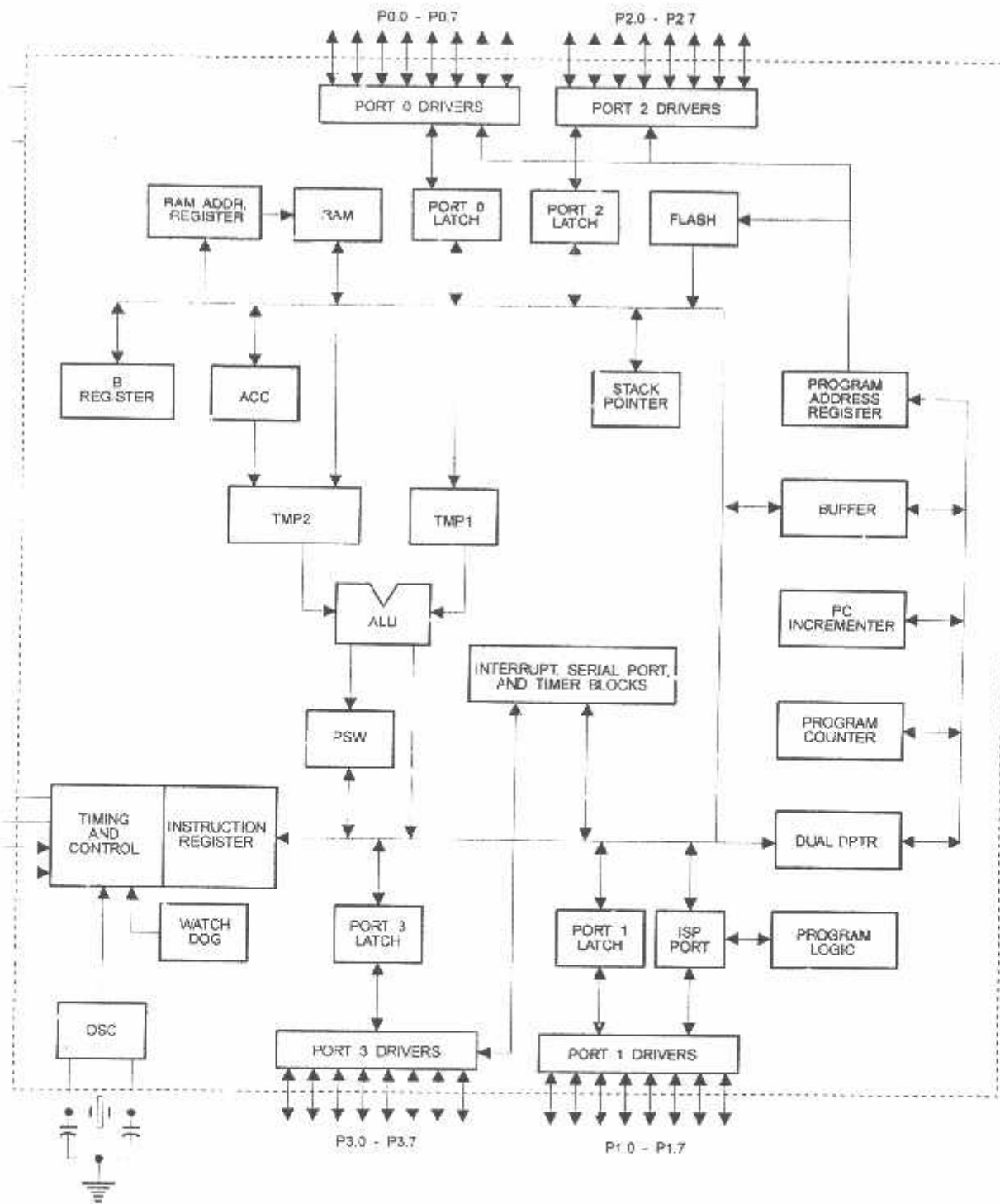




figurations



Diagram





cription

Supply voltage (all packages except 42-PDIP).

Ground (all packages except 42-PDIP; for 42-PDIP GND connects only the logic core and the embedded program memory).

Supply voltage for the 42-PDIP which connects only the logic core and the embedded program memory.

Supply voltage for the 42-PDIP which connects only the I/O Pad Drivers. The application board MUST connect both VDD and PWRVDD to the board supply voltage.

Ground for the 42-PDIP which connects only the I/O Pad Drivers. PWRGND and GND are weakly connected through the common silicon substrate, but not through any metal link. The application board MUST connect both GND and PWRGND to the board ground.

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Reset Input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

IG

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

Program Store Enable ($\overline{\text{PSEN}}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

Output from the inverting oscillator amplifier



A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

AT89S51 SFR Map and Reset Values

								0FFH
B								0F7H
00000000								0EFH
								0E7H
ACC								0DFH
00000000								0D7H
								0CFH
PSW								0C7H
00000000								0BFH
								0B7H
IP								0AFH
00000000								0A7H
P3								9FH
11111111								97H
IE								8FH
00000000								87H
P2		AUXR1				WDTRST		
11111111		XXXXXXXX0				XXXXXXXX		
SCON	SBUF							
00000000	XXXXXXXX							
P1								
11111111								
TCON	TMOD	TL0	TL1	TH0	TH1	AUXR		
00000000	00000000	00000000	00000000	00000000	00000000	XX00XX0		
P0	SP	DP0L	DP0H	DP1L	DP1H		PCON	
11111111	00000111	00000000	00000000	00000000	00000000		0XX0000	

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Table 2. AUXR: Auxiliary Register

AUXR			Address = 8EH			Reset Value = XXX00XX0B		
Not Bit Addressable								
	-	-	-	WDIDLE	DISRTO	-	-	DISALE
Bit	7	6	5	4	3	2	1	0

- Reserved for future expansion

DISALE Disable/Enable ALE

DISALE Operating Mode

0 ALE is emitted at a constant rate of 1/6 the oscillator frequency

1 ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset-out

DISRTO

0 Reset pin is driven High after WDT times out

1 Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE

0 WDT continues to count in IDLE mode

1 WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should ALWAYS initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.





Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and reset under software control and is not affected by reset.

Table 3. AUXR1: Auxiliary Register 1

AUXR1		Address = A2H						Reset Value = XXXXXXX0B
Not Bit Addressable								
	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0
– Reserved for future expansion								
DPS	Data Pointer Register Select							
DPS								
0	Selects DPTR Registers DP0L, DP0H							
1	Selects DPTR Registers DP1L, DP1H							

Memory Organization: MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Memory: If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory. On the AT89S51, if $\overline{EA}$ is connected to V_{CC} , program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Memory: The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

WDT: The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

WDT: To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

ring
own

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, refer to the Atmel Web site (<http://www.atmel.com>). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture", then "Documentation", and "Other Documents". Open the Adobe® Acrobat® file "AT89 Series Hardware Description".

and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, refer to the Atmel Web site (<http://www.atmel.com>). From the home page, select "Products", then "Microcontrollers", then "8051-Architecture", then "Documentation", and "Other Documents". Open the Adobe Acrobat file "AT89 Series Hardware Description".

ts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 4 shows that bit positions IE.6 and IE.5 are unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.



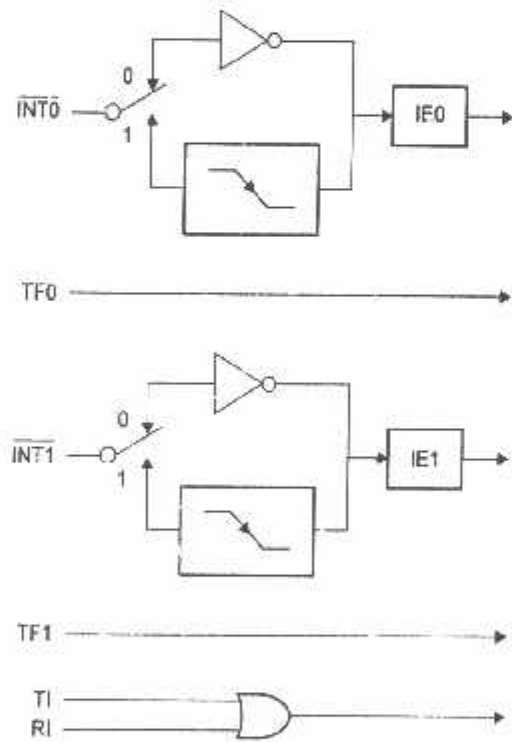
Table 4. Interrupt Enable (iE) Register

(MSB)				(LSB)			
EA	-	-	ES	ET1	EX1	ET0	EX0
Enable Bit = 1 enables the interrupt.							
Enable Bit = 0 disables the interrupt.							

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
-	IE.6	Reserved
-	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit

User software should never write 1s to reserved bits, because they may be used in future AT89 products.

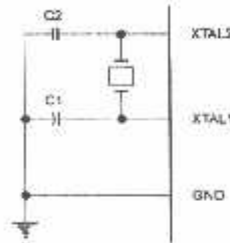
Figure 1. Interrupt Sources



Characteristics

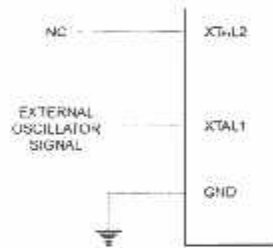
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 3. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 2. Oscillator Connections



Note: C1, C2 = 30 pF $\pm$ 10 pF for Crystals
= 40 pF $\pm$ 10 pF for Ceramic Resonators

Figure 3. External Clock Drive Configuration



Idle

In Idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt (INT0 or INT1). Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.



Table 5. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

n
/ Lock

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 6. Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features
2	P	U	U	MOV instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

iming
h –
Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash Programming Modes table (Table 7) and Figures 4 and 5. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/ $\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 μ s. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89S51 features Data Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

AT89S51

Ready/Busy: The progress of byte programming can also be monitored by the $\overline{\text{RDY/BSY}}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{\text{BUSY}}$. P3.0 is pulled high again when programming is done to indicate $\overline{\text{READY}}$.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
 (100H) = 51H indicates AT89S51
 (200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing $\text{ALE}/\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

programming
 in —
 code

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC} . The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

programming
 1

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
 Apply power between VCC and GND pins.
 Set RST pin to "H".
 If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.



Power-off sequence (if needed):
Set XTAL1 to "L" (if a crystal is not used).
Set RST to "L".
Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 8.

ming
on Set

nmimg
e –
Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer worldwide support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

ash Programming Modes

	V _{CC}	RST	PSEN	ALE/ PROG	EA/ V _{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.3-0	P1.7-0
												Address	
ata	5V	H	L		12V	L	H	H	H	H	D _{IN}	A11-8	A7-0
ata	5V	H	L	H	H	L	L	L	H	H	D _{OUT}	A11-8	A7-0
t1	5V	H	L		12V	H	H	H	H	H	X	X	X
t2	5V	H	L		12V	H	H	H	L	L	X	X	X
t3	5V	H	L		12V	H	L	H	H	L	X	X	X
ts	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
	5V	H	L		12V	H	L	H	L	L	X	X	X
)	5V	H	L	H	H	L	L	L	L	L	1EH	0000	00H
D	5V	H	L	H	H	L	L	L	L	L	51H	0001	00H
D	5V	H	L	H	H	L	L	L	L	L	06H	0010	00H

ach PROG pulse is 200 ns - 500 ns for Chip Erase.
ach PROG pulse is 200 ns - 500 ns for Write Code Data.
ach PROG pulse is 200 ns - 500 ns for Write Lock Bits.
DY/BSY signal is output on P3.0 during programming.
= don't care.

Figure 4. Programming the Flash Memory (Parallel Mode)

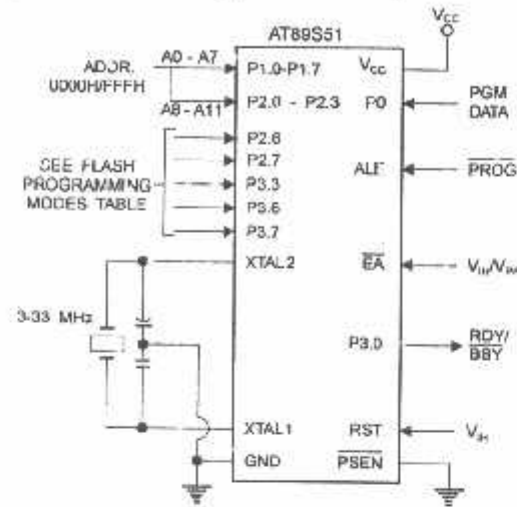
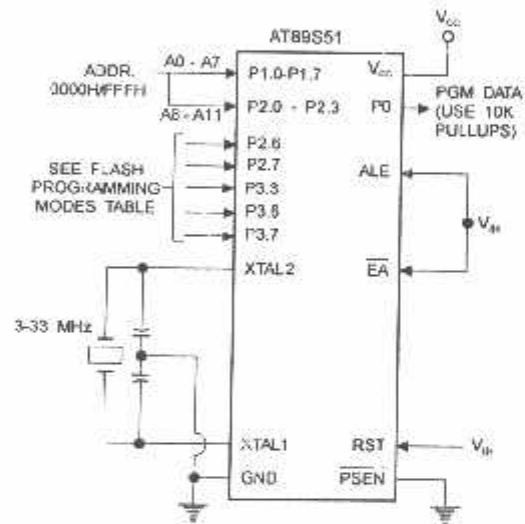


Figure 5. Verifying the Flash Memory (Parallel Mode)



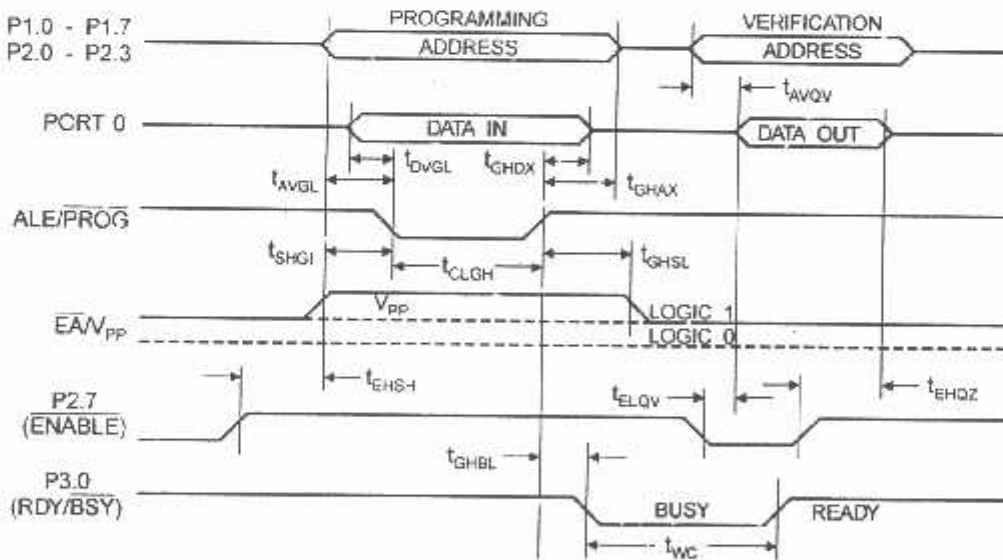


Programming and Verification Characteristics (Parallel Mode)

30°C, $V_{CC} = 4.5$ to $5.5V$

Parameter	Min	Max	Units
Programming Supply Voltage	11.5	12.5	V
Programming Supply Current		10	mA
V_{CC} Supply Current		30	mA
Oscillator Frequency	3	33	MHz
Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
P2.7 (ENABLE) High to V_{PP}	$48t_{CLCL}$		
V_{PP} Setup to $\overline{PROG}$ Low	10		μs
V_{PP} Hold After $\overline{PROG}$	10		μs
$\overline{PROG}$ Width	0.2	1	μs
Address to Data Valid		$48t_{CLCL}$	
ENABLE Low to Data Valid		$48t_{CLCL}$	
Data Float After ENABLE	0	$48t_{CLCL}$	
$\overline{PROG}$ High to BUSY Low		1.0	μs
Byte Write Cycle Time		50	μs

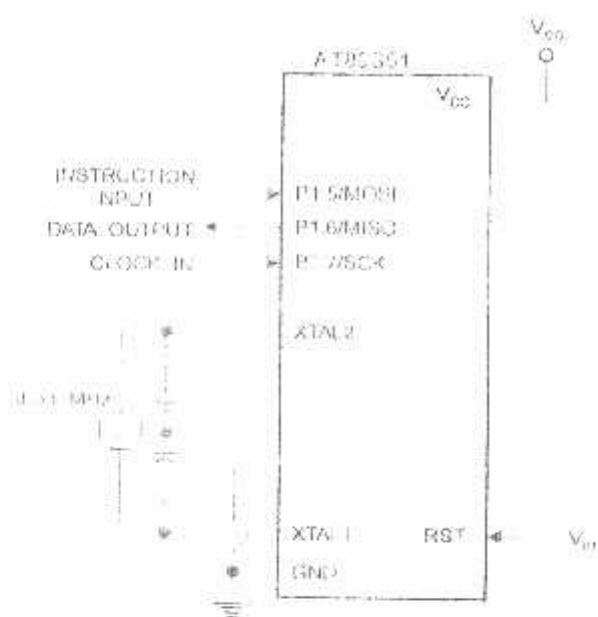
Flash Programming and Verification Waveforms – Parallel Mode



AT89S51

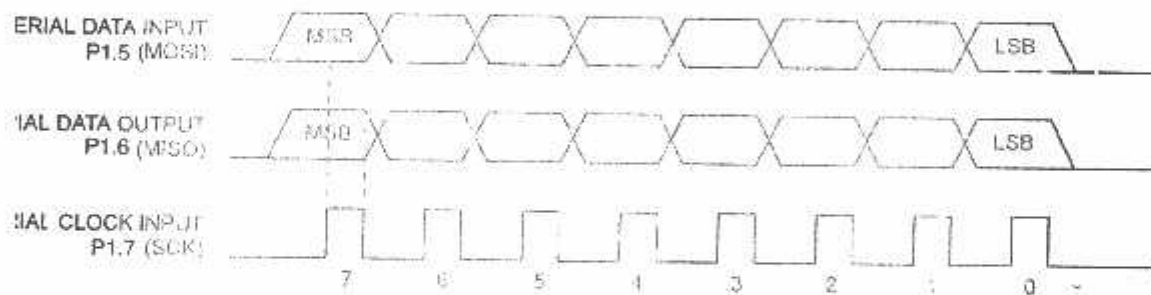
2487B-MICRO-12/03

Flash Memory Serial Downloading



Programming and Verification Waveforms – Serial Mode

Serial Programming Waveforms



Serial Programming Instruction Set

Instruction Format					
	Byte 1	Byte 2	Byte 3	Byte 4	Operation
Enable	1010 1100	0101 0011	XXXX XXXX	XXXX XXXX 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
	1010 1100	100x XXXX	XXXX XXXX	XXXX XXXX	Chip Erase Flash memory array
Program Memory (Read)	0010 0000	XXXX XXXX	XXXX XXXX	XXXX XXXX	Read data from Program memory in the byte mode
Program Memory (Write)	0100 0000	XXXX XXXX	XXXX XXXX	XXXX XXXX	Write data to Program memory in the byte mode
Lock Bits ⁽¹⁾	1010 1100	1110 0000	XXXX XXXX	XXXX XXXX	Write Lock bits. See Note (1).
Lock Bits	0010 0100	XXXX XXXX	XXXX XXXX	XXXX XXXX	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Signature Bytes	0010 1000	XXXX XXXX	XXXX XXXX	Signature Byte	Read Signature Byte
Program Memory (Read) - Page Mode	0011 0000	XXXX XXXX	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Program Memory (Write) - Page Mode	0101 0000	XXXX XXXX	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

B1 = 0, B2 = 0 — Mode 1, no lock protection
 B1 = 0, B2 = 1 — Mode 2, lock bit 1 activated
 B1 = 1, B2 = 0 — Mode 3, lock bit 2 activated
 B1 = 1, B2 = 1 — Mode 4, lock bit 3 activated

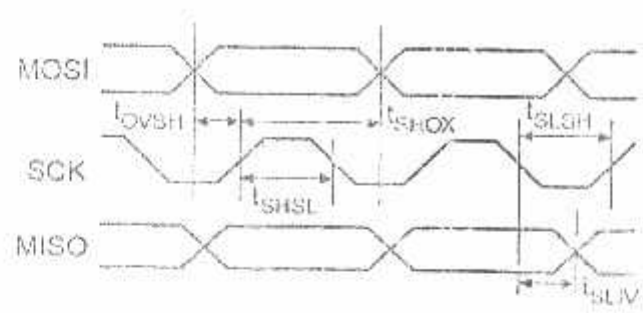
Each of the lock bit modes need to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

Programming Characteristics

Serial Programming Timing



Serial Programming Characteristics, $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 4.0 - 5.5\text{V}$ (Unless Otherwise Noted)

Parameter	Min	Typ	Max	Units
Oscillator Frequency	3		33	MHz
Oscillator Period	30			ns
SCK Pulse Width High	$8 t_{CLCL}$			ns
SCK Pulse Width Low	$8 t_{CLCL}$			ns
MOSI Setup to SCK High	t_{CLCL}			ns
MOSI Hold after SCK High	$2 t_{CLCL}$			ns
SCK Low to MISO Valid	10	16	32	ns
Chip Erase Instruction Cycle Time			500	ms
Serial Byte Write Cycle Time			$64 t_{CLCL} + 400$	μs



Maximum Ratings*

Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Any Pin Voltage to Ground.....	-1.0V to +7.0V
Operating Voltage.....	5.5V
Current.....	15.0 mA

***NOTICE:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

Values shown in this table are valid for $T_A = -40^{\circ}\text{C}$ to 85°C and $V_{CC} = 4.0\text{V}$ to 5.5V , unless otherwise noted.

Parameter	Condition	Min	Max	Units
Input Low Voltage	(Except EA)	-0.5	$0.2 V_{CC} - 0.1$	V
Input Low Voltage (EA)		-0.5	$0.2 V_{CC} - 0.3$	V
Input High Voltage	(Except XTAL1, RST)	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V
Input High Voltage	(XTAL1, RST)	$0.7 V_{CC}$	$V_{CC} + 0.5$	V
Output Low Voltage ⁽¹⁾ (Ports 1,2,3)	$I_{OL} = 1.6 \text{ mA}$		0.45	V
Output Low Voltage ⁽¹⁾ (Port 0, ALE, PSEN)	$I_{OL} = 3.2 \text{ mA}$		0.45	V
Output High Voltage (Ports 1,2,3, ALE, PSEN)	$I_{OH} = -60 \mu\text{A}$, $V_{CC} = 5\text{V} \pm 10\%$	2.4		V
	$I_{OH} = -25 \mu\text{A}$	$0.75 V_{CC}$		V
	$I_{OH} = -10 \mu\text{A}$	$0.9 V_{CC}$		V
	$I_{OH} = -800 \mu\text{A}$, $V_{CC} = 5\text{V} \pm 10\%$	2.4		V
Output High Voltage (Port 0 in External Bus Mode)	$I_{OH} = -300 \mu\text{A}$	$0.75 V_{CC}$		V
	$I_{OH} = -60 \mu\text{A}$	$0.9 V_{CC}$		V
Logical 0 Input Current (Ports 1,2,3)	$V_{IH} = 0.45\text{V}$		-50	μA
Logical 1 to 0 Transition Current (Ports 1,2,3)	$V_{IH} = 2\text{V}$, $V_{CC} = 5\text{V} \pm 10\%$		-650	μA
Input Leakage Current (Port 0, EA)	$0.45 < V_{IH} < V_{CC}$		± 10	μA
Reset Pulldown Resistor		50	300	$\text{K}\Omega$
Pin Capacitance	Test Freq. = 1 MHz, $T_A = 25^{\circ}\text{C}$		10	pF
Power Supply Current	Active Mode, 12 MHz		25	mA
	Idle Mode, 12 MHz		6.5	mA
Power-down Mode ⁽²⁾	$V_{CC} = 5.5\text{V}$		50	μA

Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA

Maximum I_{OL} per 8-bit port:

Port 0: 26 mA Ports 1, 2, 3: 15 mA

Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

Minimum V_{CC} for Power-down is 2V.

Characteristics

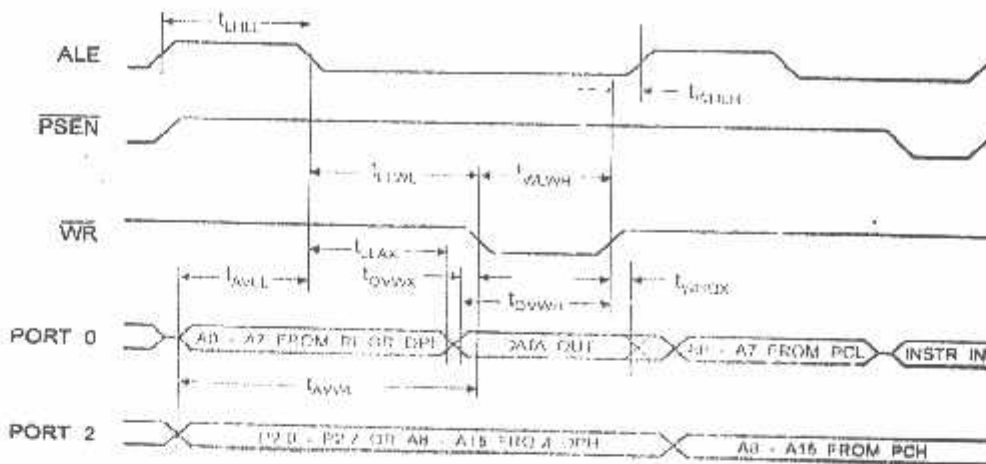
Operating conditions, load capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; load capacitance for all other ports = 50 pF.

1 Program and Data Memory Characteristics

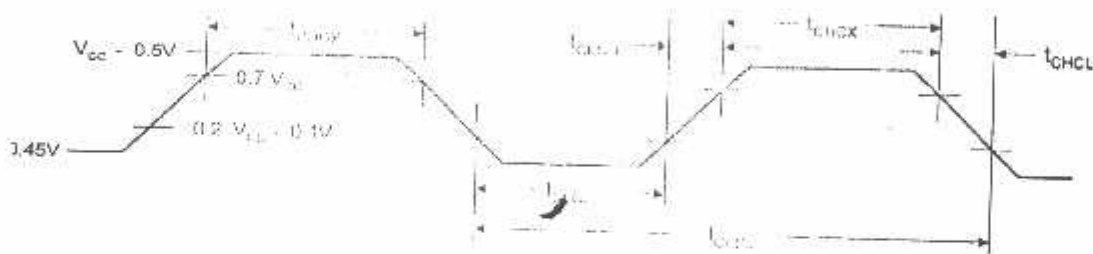
Parameter	12 MHz Oscillator		Variable Oscillator		Units
	Min	Max	Min	Max	
Oscillator Frequency			0	33	MHz
ALE Pulse Width	127		$2t_{CLCL}-40$		ns
Address Valid to ALE Low	43		$t_{CLCL}-25$		ns
Address Hold After ALE Low	48		$t_{CLCL}-25$		ns
ALE Low to Valid Instruction In		233		$4t_{CLCL}-65$	ns
ALE Low to PSEN Low	43		$t_{CLCL}-25$		ns
PSEN Pulse Width	205		$3t_{CLCL}-45$		ns
PSEN Low to Valid Instruction In		145		$3t_{CLCL}-60$	ns
Input Instruction Hold After PSEN	0		0		ns
Input Instruction Float After PSEN		59		$t_{CLCL}-25$	ns
PSEN to Address Valid	75		$t_{CLCL}-3$		ns
Address to Valid Instruction In		312		$5t_{CLCL}-80$	ns
PSEN Low to Address Float		10		10	ns
RD Pulse Width	400		$8t_{CLCL}-100$		ns
WR Pulse Width	400		$8t_{CLCL}-100$		ns
RD Low to Valid Data In		252		$5t_{CLCL}-90$	ns
Data Hold After RD	0		0		ns
Data Float After RD		97		$2t_{CLCL}-28$	ns
ALE Low to Valid Data In		517		$8t_{CLCL}-150$	ns
Address to Valid Data In		585		$9t_{CLCL}-165$	ns
ALE Low to RD or WR Low	203	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
Address to RD or WR Low	203		$4t_{CLCL}-75$		ns
Data Valid to WR Transition	23		$t_{CLCL}-30$		ns
Data Valid to WR High	423		$7t_{CLCL}-130$		ns
Data Hold After WR	33		$t_{CLCL}-25$		ns
RD Low to Address Float		0		0	ns
RD or WR High to ALE High	43	123	$t_{CLCL}-25$	$t_{CLCL}+25$	ns

[illegible]

Data Memory Write Cycle



Clock Drive Waveforms



Clock Drive

Parameter	Min	Max	Units
Oscillator Frequency	0	33	MHz
Clock Period	30		ns
High Time	12		ns
Low Time	12		ns
Rise Time		5	ns
Fall Time		5	ns

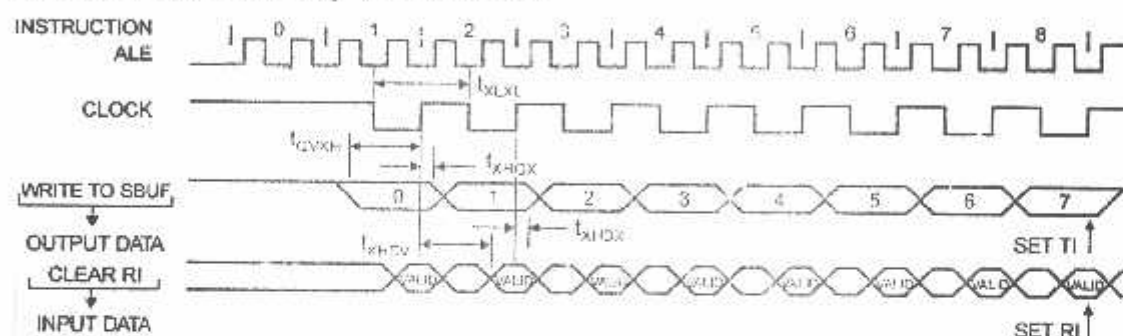


Port Timing: Shift Register Mode Test Conditions

Conditions in this table are valid for $V_{CC} = 4.0V$ to $5.5V$ and Load Capacitance = 80 pF .

Parameter	12 MHz Clock		Variable Oscillator		Units
	Min	Max	Min	Max	
Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		μs
Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}-133$		ns
Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}-80$		ns
Input Data Hold After Clock Rising Edge	0		0		ns
Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}-133$	ns

Shift Register Mode Timing Waveforms



Input/Output Waveforms⁽¹⁾



⁽¹⁾ AC Inputs during testing are driven at $V_{CC} = 0.5V$ for a logic 1 and $0.45V$ for a logic 0. Timing measurements are made at $V_{IH\min}$ for a logic 1 and $V_{IL\max}$ for a logic 0.

Waveforms⁽¹⁾



⁽¹⁾ For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

g Information

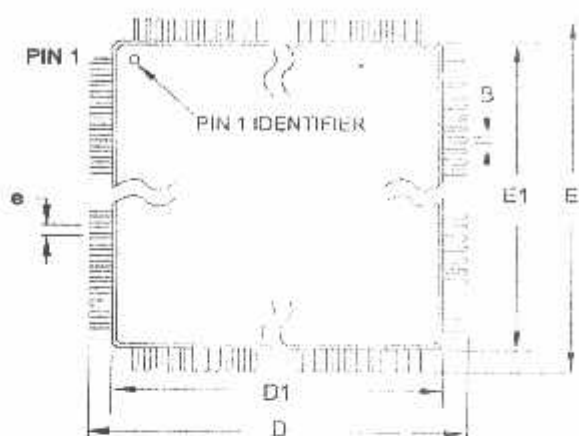
Power Supply	Ordering Code	Package	Operation Range
4.0V to 5.5V	AT89S51-24AC	44P	Commercial (0° C to 70° C)
	AT89S51-24JC	44J	
	AT89S51-24PC	40P6	
	AT89S51-24SC	42PS6	
	AT89S51-24AI	44A	Industrial (-40° C to 85° C)
	AT89S51-24JI	44J	
	AT89S51-24PI	40P6	
	AT89S51-24SI	42PS6	
4.5V to 5.5V	AT89S51-33AC	44A	Commercial (0° C to 70° C)
	AT89S51-33JC	44J	
	AT89S51-33PC	40P6	
	AT89S51-33SC	42PS6	

Package Type	
44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)	
44-lead, Plastic J-leaded Chip Carrier (PLCC)	
40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)	
42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)	



ing Information

FP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.95	1.00	1.05	
C	11.75	12.00	12.25	
D1	9.80	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	—	0.45	
C	0.09	—	0.20	
L	0.45	—	0.75	
e	0.80 TYP			

1. This package conforms to JEDEC reference MS-010, Variation FCB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

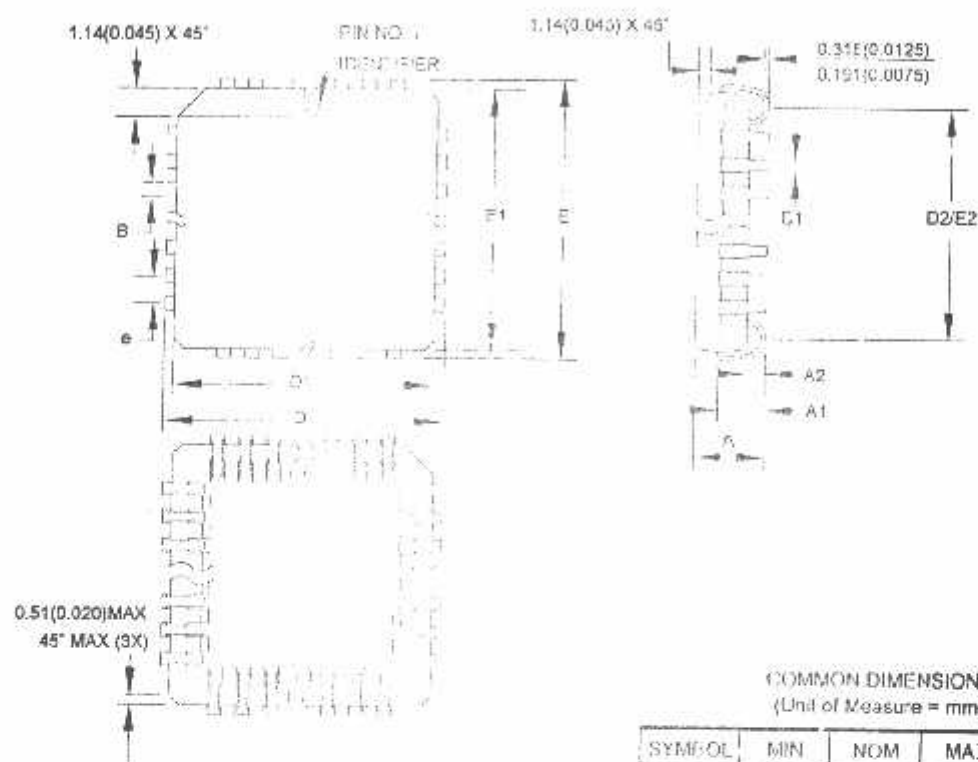
10/5/2001

3325 Orchard Parkway San Jose, CA 95131	TITLE 44A, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	DRAWING NO.	REV.
		44A	B

AT89S51

2487B-MICRO-12/03

PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.181	—	4.572	
A1	2.280	—	3.048	
A2	0.505	—	—	
D	17.389	—	17.653	
D1	16.510	—	16.662	Note 2
E	17.389	—	17.663	
E1	16.510	—	16.662	Note 2
D2/E2	14.963	—	16.002	
B	0.663	—	0.813	
B1	0.330	—	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AG.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.10" (2.54 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parking line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

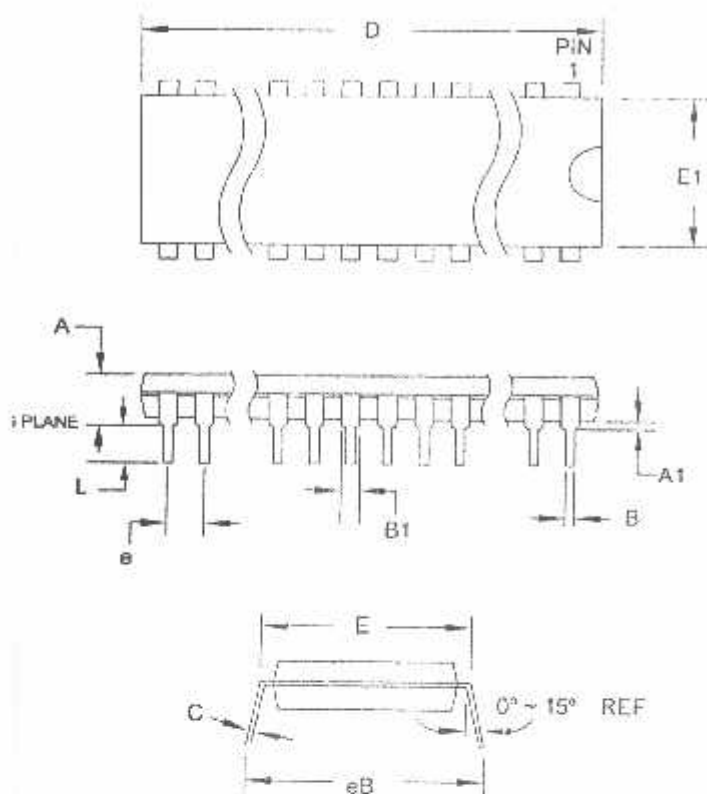
2325 Orchard Parkway
San Jose, CA 95131

TITLE
44J, 44-Pin, Plastic J-Leaded Chip Carrier (PLCC)

DRAWING NO.
44J

REV.
B

DIP



1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	4.826	
A1	0.381	—	—	
D	52.070	—	52.578	Note 2
E	15.240	—	16.875	
E1	13.462	—	13.970	Note 2
B	0.356	—	0.559	
B1	1.041	—	1.651	
L	3.048	—	3.556	
C	0.203	—	0.381	
eB	15.494	—	17.526	
P	2.540 TYP			

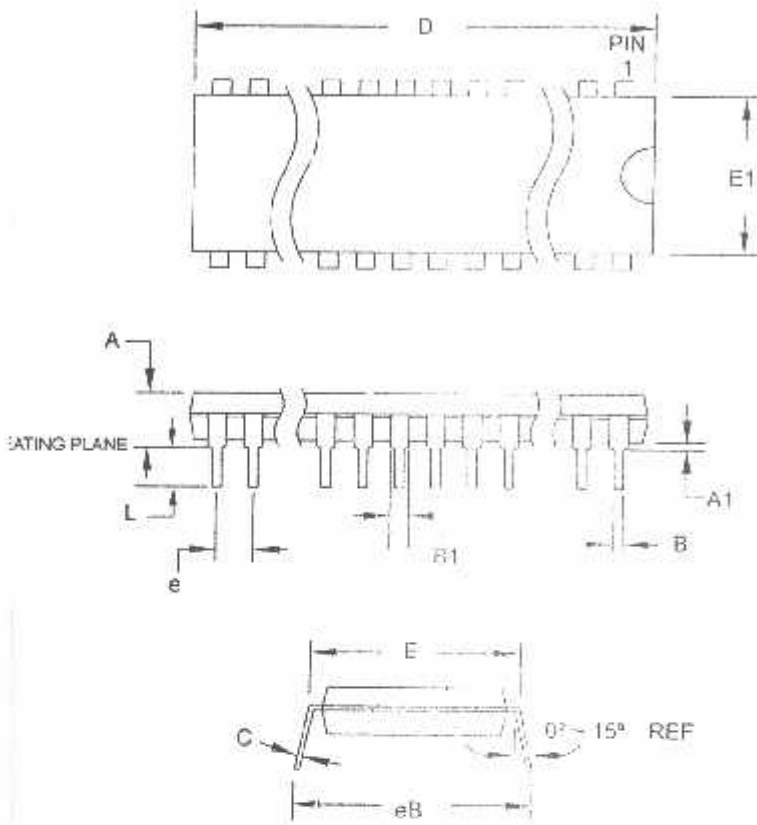
09/20/01

325 Orchard Parkway San Jose, CA 95131	TITLE 40P6, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	DRAWING NO. 40P6	REV. B
---	---	---------------------	-----------

AT89S51

2487B-MICRO-12/03

6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	4.83	
A1	0.51	—	—	
D	36.70	—	36.96	Note 2
E	15.24	—	15.88	
E1	13.46	—	13.97	Note 2
H	0.33	—	0.56	
B1	0.75	—	1.27	
L	3.05	—	3.43	
C	0.20	—	0.30	
e	—	—	18.55	
e	1.78 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-011, Variation A.
 2. Dimensions D and E1 do not include mold flash or protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/6/03

2325 Orchard Parkway San Jose, CA 95131	TITLE 42PS6, 42-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	DRAWING NO.	REV.
		42PS6	A



Atmel Corporation

25 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel SARL
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Suisse
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

China
Room 1219
Inachem Golden Plaza
Mody Road Tsinghua
District Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
Tonetsu Shinkawa Bldg.
4-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantre
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Roussel Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Kel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
39521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard terms and conditions. The Company assumes no responsibility for any errors or omissions which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and makes no commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use in life support devices or systems.

© Atmel Corporation 2003. All rights reserved. Atmel® and combinations thereof are the registered trademarks of Atmel Corporation or its subsidiaries. MCS® is a registered trademark of Intel Corporation. Adobe® and Acrobat® are the registered trademarks of Adobe Systems Inc. All other names and product names may be the trademarks of others.



Printed on recycled paper.

2487B-MICRO-12/03

RS-422 and RS-485 Application Note



International Headquarters

B&B Electronics Mfg. Co. Inc.
707 Dayton Road -- P.O. Box 1040 -- Ottawa IL 61350 USA
Phone (815) 433-5100 -- General Fax (815) 433-5105

Home Page: www.bb-elect.com

Customer Service e-mail: sales@bb-elect.com -- Fax (815) 433-5109

Technical Support e-mail: support@bb-elect.com -- Fax (815) 433-5104

European Headquarters

B&B Electronics Ltd.

Westlink Commercial Park, Oranmore, Co. Galway, Ireland
Phone (353) 91 792444 -- Fax (353) 91 792445

Home Page: www.bb-europe.com

Sales e-mail: sales@bb-europe.com

Technical Support e-mail: support@bb-europe.com

© Copyright B&B Electronics -- Revised June 2006

INTRODUCTION	1
DATA TRANSMISSION SIGNALS.....	1
Unbalanced Line Drivers.....	1
Balanced Line Drivers.....	1
Balanced Line Receivers.....	3
EIA STANDARD RS-422 DATA TRANSMISSION	3
EIA STANDARD RS-485 DATA TRANSMISSION	6
TRISTATE CONTROL OF AN RS-485 DEVICE USING RTS.....	9
SEND DATA CONTROL OF AN RS-485 DEVICE.....	11
CHAPTER 2: SYSTEM CONFIGURATION	13
NETWORK TOPOLOGIES.....	13
TWO WIRE OR FOUR WIRE SYSTEMS.....	13
TERMINATION.....	16
BIASING AN RS-485 NETWORK.....	17
EXTENDING THE SPECIFICATION.....	19
CHAPTER 3: SELECTING RS-422 AND RS-485 CABLING	20
NUMBER OF CONDUCTORS	20
SHIELDING.....	20
CABLE CHARACTERISTICS	20
CHAPTER 4: TRANSIENT PROTECTION OF RS-422 AND RS-485 SYSTEMS.....	25
WHAT DOES A SURGE LOOK LIKE?	25
Surge Specifications.....	25
Common Mode vs. Differential Mode.....	25
GROUND ≠ GROUND	26
TRANSIENT PROTECTION USING ISOLATION	27
Isolation Theory.....	27
Isolation Devices.....	28
TRANSIENT PROTECTION USING SHUNTING	28
Shunting Theory.....	28
Connecting Signal Grounds.....	29
Shunting Devices.....	29
COMBINING ISOLATION AND SHUNTING	29
SPECIAL CONSIDERATION FOR FAULT CONDITIONS.....	31
CHOOSING THE RIGHT PROTECTION FOR YOUR SYSTEM.....	31

RS-422 SYSTEMS.....	32
RS-485 DRIVER CONTROL.....	33
RS-485 RECEIVER CONTROL.....	34
MASTER-SLAVE SYSTEMS	34
Four Wire Master-Slave Systems.....	34
Two Wire Master-Slave Systems.....	34
MULTI-MASTER RS-485 SYSTEMS.....	35
SYSTEMS WITH PORT POWERED CONVERTERS.....	35
CHAPTER 6: SELECTING RS-485 DEVICES	36
CHAPTER 7: SOURCES OF FURTHER INFORMATION	37
APPENDIX A: EIA SPECIFICATION SUMMARY	38
APPENDIX B: EIA STANDARD RS-423 DATA TRANSMISSION.....	40

The purpose of this application note is to describe the main elements of an RS-422 and RS-485 system. This application note attempts to cover enough technical details so that the system designer will have considered all the important aspects in his data system design. Since both RS-422 and RS-485 are data transmission systems that use balanced differential signals, it is appropriate to discuss both systems in the same application note. Throughout this application note the generic terms of RS-422 and RS-485 will be used to represent the EIA/TIA-422 and EIA/TIA-485 Standards.

Data Transmission Signals

Unbalanced Line Drivers

Each signal that transmits in an RS-232 unbalanced data transmission system appears on the interface connector as a voltage with reference to a signal ground. For example, the transmitted data (TD) from a DTE device appears on pin 2 with respect to pin 7 (signal ground) on a DB-25 connector. This voltage will be negative if the line is idle and alternate between that negative level and a positive level when data is sent with a magnitude of ± 5 to ± 15 volts. The RS-232 receiver typically operates within the voltage range of +3 to +12 and -3 to -12 volts as shown in Figure 1.1.

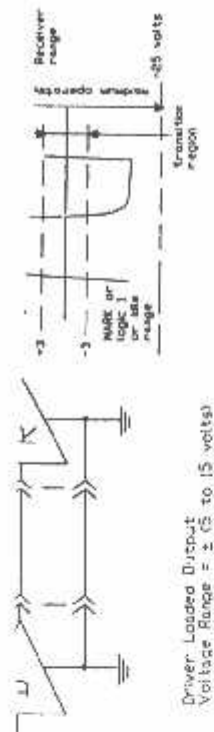
Balanced Line Drivers

In a balanced differential system the voltage produced by the driver appears across a pair of signal lines that transmit only one signal. Figure 1.2 shows a schematic symbol for a balanced line driver and the voltages that exist. A balanced line driver will produce a voltage from 2 to 6 volts across its A and B output terminals and will have a signal ground (C) connection. Although proper connection to the signal ground is important, it isn't used by a balanced line receiver in determining the logic state of the data line. A balanced line driver can also have an input signal called an "Enable" signal. The purpose of this signal is to connect the driver to its output terminals, A and B. If the "Enable" signal is OFF, one can consider the driver as disconnected from the transmission line. An RS-422 driver must have the "Enable" control signal. An RS-422 driver may have this signal, but it is not always required. The disconnected or "disabled" condition of the line driver usually is referred to as the "tristate" condition of the driver.

¹ The term "tristate" comes from the fact that there is a third output state of an RS-485 driver, in addition to the output states of "1" and "0."

RS-422/485 Application Note

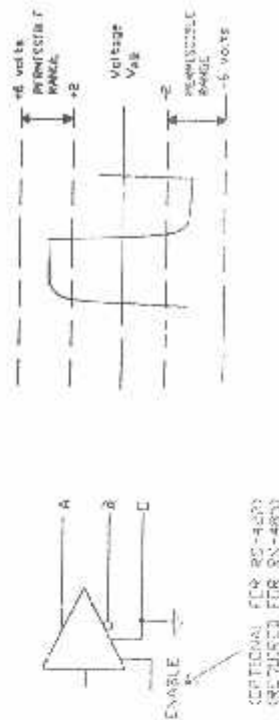
© Copyright B&B Electronics - Revised 2506
B&B Electronics Mfg Co - 707 Dayton Rd - PO Box 1040 - Ottawa IL 61350 - Ph 815-433-5100 - Fax 815-433-5104
B&B Electronics Ltd - Westlink Comm. Pk - Oramore, Galway, Ireland - Ph 353-91-792444 - Fax 353-91-792445



Driver Loaded Output
Voltage Range = ± 5 to ± 15 volts

RS-232 Interface Circuit

Figure 1.1



SECTIONAL FOR RS-422/485
(REPLACES FOR RS-485)

BALANCED DIFFERENTIAL OUTPUT
LINE DRIVER

Figure 1.2

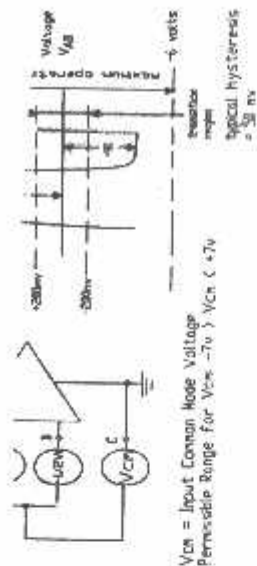
transmission line across two signal input lines, A and B. It will also have a signal ground (C) that is necessary in making the proper interface connection. Figure 1.3 is a schematic symbol for a balanced differential line receiver. Figure 1.3 also shows the voltages that are important to the balanced line receiver. If the differential input voltage V_{AB} is greater than +200 mV the receiver will have a specific logic state on its output terminal. If the input voltage is reversed to less than -200 mV the receiver will create the opposite logic state on its output terminal. The input voltages that a balanced line receiver must sense are shown in Figure 1.3. The 200 mV to 6 V range is required to allow for attenuation on the transmission line.

EIA Standard RS-422 Data Transmission

The EIA Standard RS-422-A entitled "Electrical Characteristics of Balanced Voltage Digital Interface Circuits" defines the characteristics of RS-422 interface circuits. Figure 1.4 is a typical RS-422 four-wire interface. Notice that five conductors are used. Each generator or driver can drive up to ten (10) receivers. The two signaling states of the line are defined as follows:

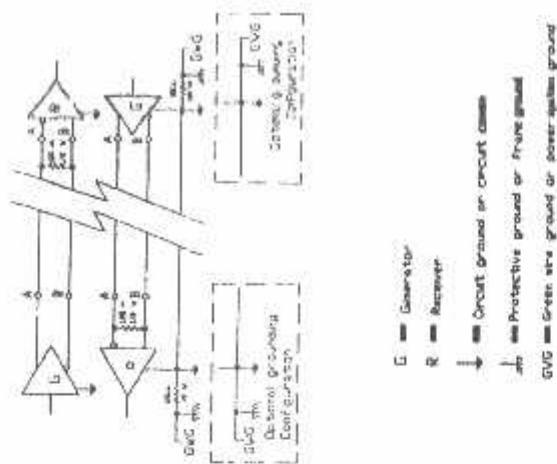
- When the "A" terminal of the driver is negative with respect to the "B" terminal, the line is in a binary 1 (MARK or OFF) state.
- When the "A" terminal of the driver is positive with respect to the "B" terminal, the line is in a binary 0 (SPACE or ON) state.

Figure 1.5 shows the condition of the voltage of the balanced line for an RS-232 to RS-422 converter when the line is in the "idle" condition or OFF state. It also shows the relationship of the "A" and "B" terminals of an RS-422 system and the "+" and "-" terminal markings used on many types of equipment. The "A" terminal is equivalent to the "+" designation, and the "B" terminal equivalent to the "-" designation. The same relationship shown in Figure 1.5 also applies for RS-485 systems. RS-422 can withstand a common mode voltage (V_{cm}) of ± 7 volts. Common mode voltage is defined as the mean voltage of A and B terminals with respect to signal ground.



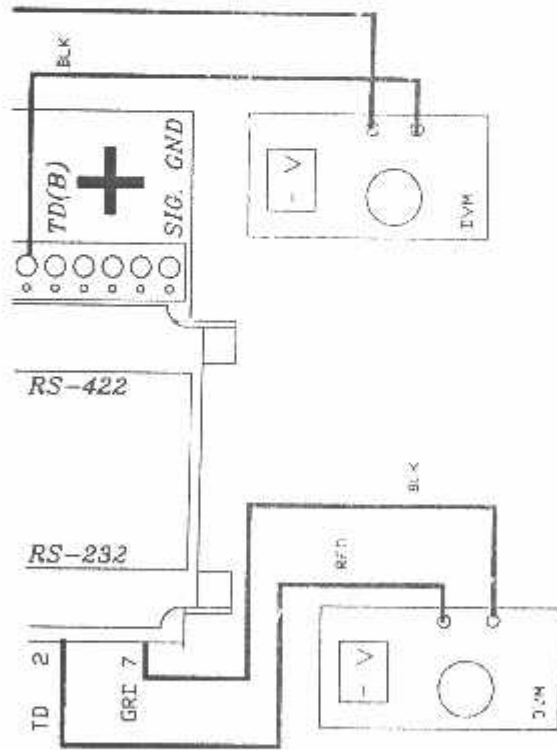
BALANCED DIFFERENTIAL INPUT
LINE RECEIVER

Figure 1.3



Typical RS-422 Four Wire Network

Figure 1.4



NOTE: UNDER "IDLE" CONDITIONS IT IS POSSIBLE TO DETERMINE WHICH TERMINAL IS "A" AND WHICH IS "B"

RELATIONSHIP BETWEEN EIA STANDARD "A" AND "B" TERMINALS ON AN RS-422 OR RS-485 DEVICE AND "A" AND "B" IDENTIFICATION CONVENTION

Figure 1.5

The RS-485 Standard permits a balanced transmission line to be shared in a party line or multidrop mode. As many as 32 driver/receiver pairs can share a multidrop network. Many characteristics of the drivers and receivers are the same as RS-422. The range of the common mode voltage V_{cm} that the driver and receiver can tolerate is expanded to +12 to -7 volts. Since the driver can be disconnected or tristated from the line, it must withstand this common mode voltage range while in the tristate condition. Some RS-422 drivers, even, with tristate capability, will not withstand the full V_{cm} voltage range of +12 to -7 volts.

Figure 1.6 shows a typical two-wire multidrop network. Note that the transmission line is terminated on both ends of the line but not at drop points in the middle of the line. Termination should only be used with high data rates and long wiring runs. A detailed discussion of termination can be found in Chapter 2 of this application note. The signal ground line is also recommended in an RS-485 system to keep the common mode voltage that the receiver must accept within the -7 to +12 volt range. Further discussion of grounding can be found in Chapter 3 of this application note.

TYPICAL RS-485 TWO WIRE MULTIDROP NETWORK

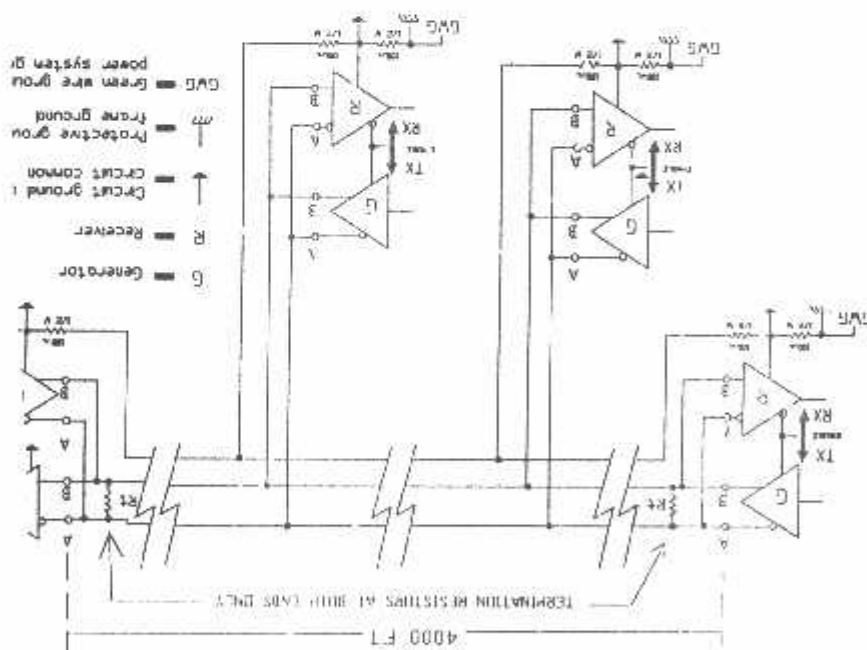


Figure 1.6

TYPICAL RS-485 FOUR WIRE MULTIDROP NETWORK

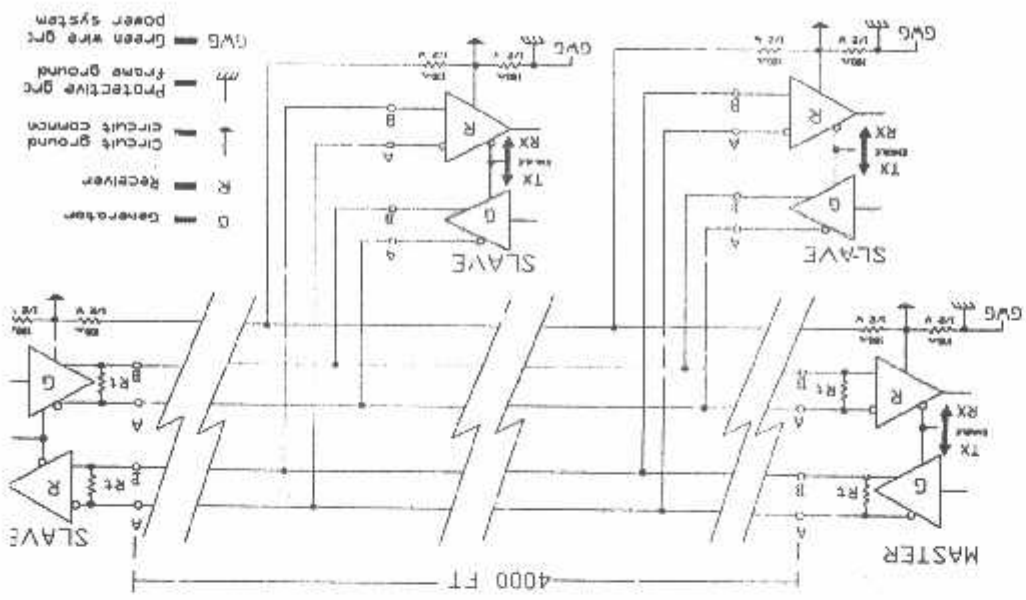


Figure 1.7

connected so that the master node communicates to all slave nodes. The network is nodes communicate only with the master node. This network has some advantages with equipment with mixed protocol communications. Since the slave nodes never listen to another slave response to the master, a slave node cannot reply incorrectly to another slave node.

Tristate Control of an RS-485 Device using RTS

As discussed previously, an RS-485 system must have a driver that can be disconnected from the transmission line when a particular node is not transmitting. In an RS-232 to RS-485 converter or an RS-485 serial card, this may be implemented using the RTS control signal from an asynchronous serial port to enable the RS-485 driver. The RTS line is connected to the RS-485 driver enable such that setting the RTS line to a high (logic 1) state enables the RS-485 driver. Setting the RTS line low (logic 0) puts the driver into the tristate condition. This in effect disconnects the driver from the bus, allowing other nodes to transmit over the same wire pair. Figure 1.8 shows a timing diagram for a typical RS-232 to RS-485 converter. The waveforms show what happens if the VRTS waveform is narrower than the data VSD. This is not the normal situation, but is shown here to illustrate the loss of a portion of the data waveform. When RTS control is used, it is important to be certain that RTS is set high before data is sent. Also, the RTS line must then be set low after the last data bit is sent. This timing is done by the software used to control the serial port and not by the converter.

When an RS-485 network is connected in a two-wire multidrop party line mode, the receiver at each node will be connected to the line (see Figure 1.6). The receiver can often be configured to receive an echo of its own data transmission. This is desirable in some systems, and troublesome in others. Be sure to check the data sheet for your converter to determine how the receiver "enable" function is connected.

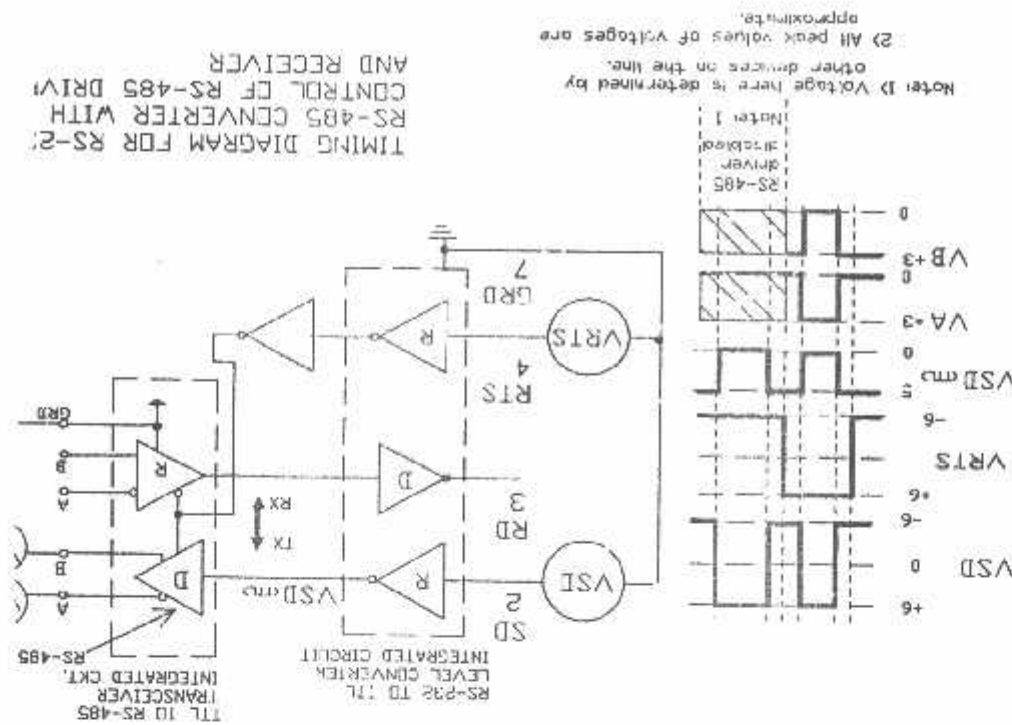


Figure 1.8

enable the RS-485 driver. Figure 1.9 is a timing diagram of the important signals used to control a converter of this type. It is important to note that the transmit data line is "disabled" at a fixed interval after the last bit, typically one character length. If this interval is too long, you can miss parts of each character being sent. If this time is too long, your system may try to turn the data line around from transmit to receive before the node (with the Send Data converter) is ready to receive data. If the latter is the case, you will miss portions (or complete characters) at the beginning of a response.

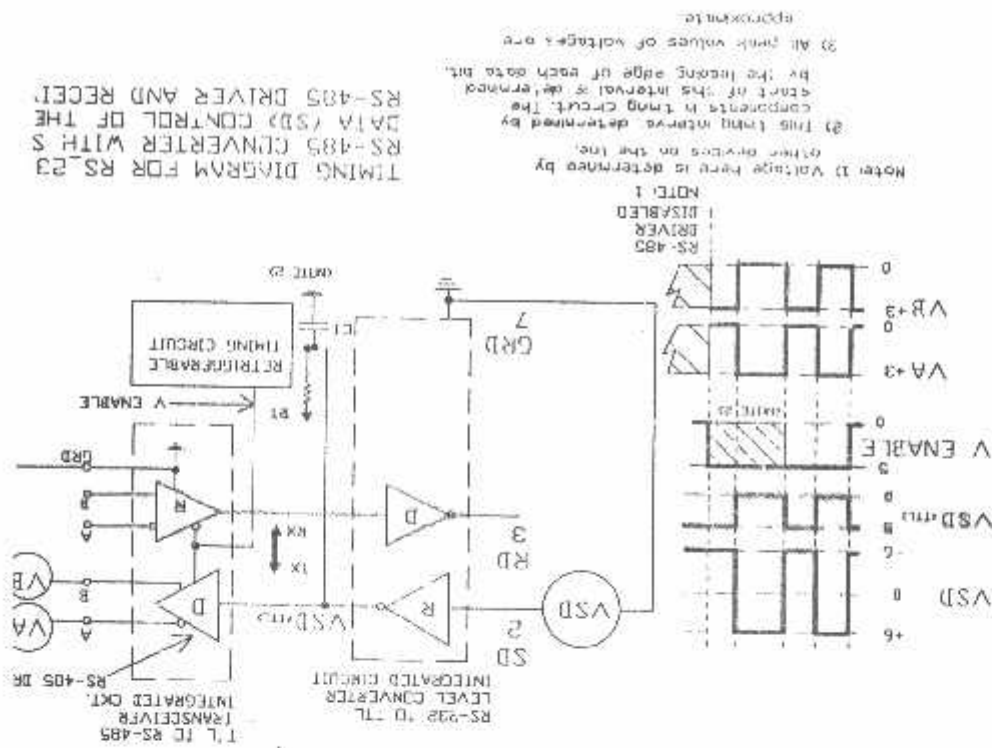


Figure 1.9

RS-422/485 Application Note

© Copyright B&B Electronics - Revised 2506
B&B Electronics Mfg Co - 707 Dayton Rd - PO Box 1040 - Ottawa IL 61350 - Ph 815-433-5100 - Fax 815-433-5104
B&B Electronics Ltd - Westlink Comm Pk - Oranmore, Galway, Ireland - Ph 353-91-792444 - Fax 353-91-792445

11

12

RS-422/485 Application Note

© Copyright B&B Electronics - Revised 2506
B&B Electronics Mfg Co - 707 Dayton Rd - PO Box 1040 - Ottawa IL 61350 - Ph 815-433-5100 - Fax 815-433-5104
B&B Electronics Ltd - Westlink Comm Pk - Oranmore, Galway, Ireland - Ph 353-91-792444 - Fax 353-91-792445

Network configuration isn't defined in the RS-422 or RS-485 specification. In most cases the designer can use a configuration that best fits the physical requirements of the system.

Two Wire or Four Wire Systems

RS-422 systems require a dedicated pair of wires for each signal, a transmit pair, a receive pair and an additional pair for each handshake control signal used (if required). The tristate capabilities of RS-485 allow a single pair of wires to share transmit and receive signals for half-duplex communications. This "two wire" configuration (note that an additional ground conductor should be used) reduces cabling cost. RS-485 devices may be internally or externally configured for two wire systems. Internally configured RS-485 devices simply provide A and B connections (sometimes labeled "-" and "+").

Devices configured for four wire communications bring out A and B connections for both the transmit and the receive pairs. The user can connect the transmit lines to the receive lines to create a two wire configuration. The latter type device provides the system designer with the most configuration flexibility. Note that the signal ground line should also be connected in the system. This connection is necessary to keep the V_{cm} common mode voltage at the receiver within a safe range. The interface circuit may operate without the signal ground connection, but may sacrifice reliability and noise immunity. Figures 2.1 and 2.2 illustrate connections of two and four wire systems.

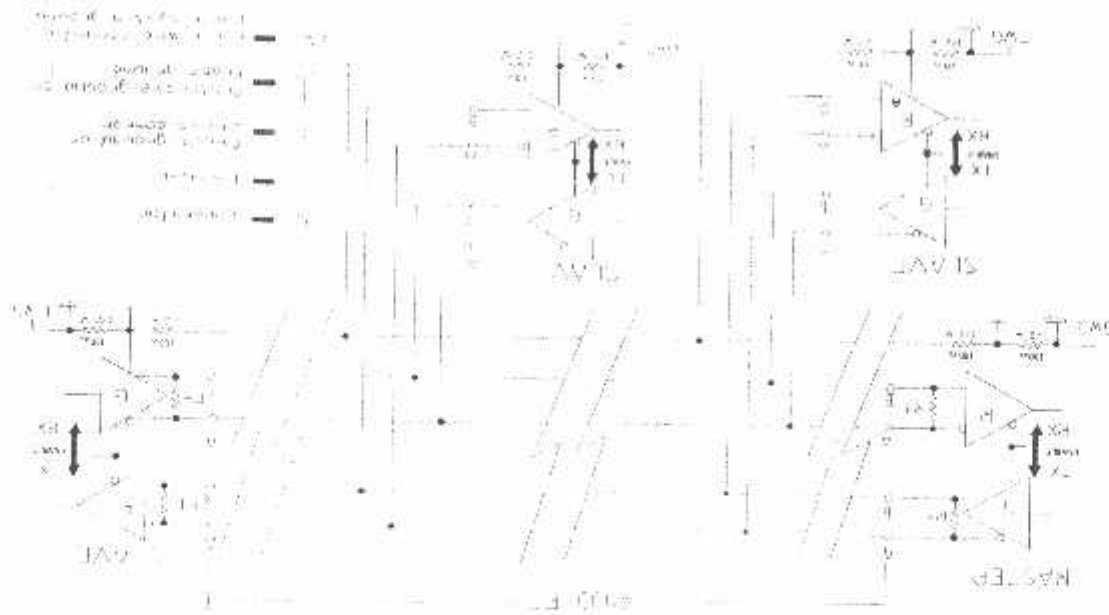


Figure 2.1 Typical RS-485 Four Wire Multidrop Configuration

Termination is used to prevent reflections on the transmission line being used. When impedance are mismatched, the transmitted signal is not completely absorbed by the load and a portion is reflected back into the transmission line. If the source, transmission line and load impedance are equal these reflections are eliminated. There are disadvantages of termination as well. Termination increases load on the drivers, increases installation complexity, changes biasing requirements and makes system modification more difficult.

The decision whether or not to use termination should be based on the cable length and data rate used by the system. A good rule of thumb is if the propagation delay of the data line is much less than one bit width, termination is not needed. This rule makes the assumption that reflections will damp out in several trips up and down the data line. Since the receiving UART will sample the data in the middle of the bit, it is important that the signal level be solid at that point. For example, in a system with 2000 feet of data line the propagation delay can be calculated by multiplying the cable length by the propagation velocity of the cable. This value, typically 66 to 75% of the speed of light (c), is specified by the cable manufacturer.

For our example, a round trip covers 4000 feet of cable. Using a propagation velocity of $0.66 \times c$, one round trip is completed in approximately 6.16 μs . If we assume the reflections will damp out in three "round trips" up and down the cable length, the signal will stabilize 18.5 μs after the leading edge of a bit. At 9600 baud one bit is 104 μs wide. Since the reflections are damped out much before the center of the bit, termination is not required.

There are several methods of terminating data lines. The method recommended by B&B Electronics is parallel termination. A resistor is added in parallel with the receiver's "A" and "B" lines in order to match the data line characteristic impedance specified by the cable manufacturer (120 Ω is a common value). This value describes the intrinsic impedance of the transmission line and is not a function of the line length. A terminating resistor of less than 90 Ω should not be used. Termination resistors should be placed only at the extreme ends of the data line, and no more than two terminations should be placed in any system that does not use repeaters. This type of termination clearly adds heavy DC loading to a system and may overload port powered RS-232 to RS-485 converters. Another type of termination, AC coupled termination, adds a small capacitor in series with the termination resistor to eliminate the DC loading effect. Although this method eliminates DC loading, capacitor selection is highly dependent on the system properties. System designers interested in AC

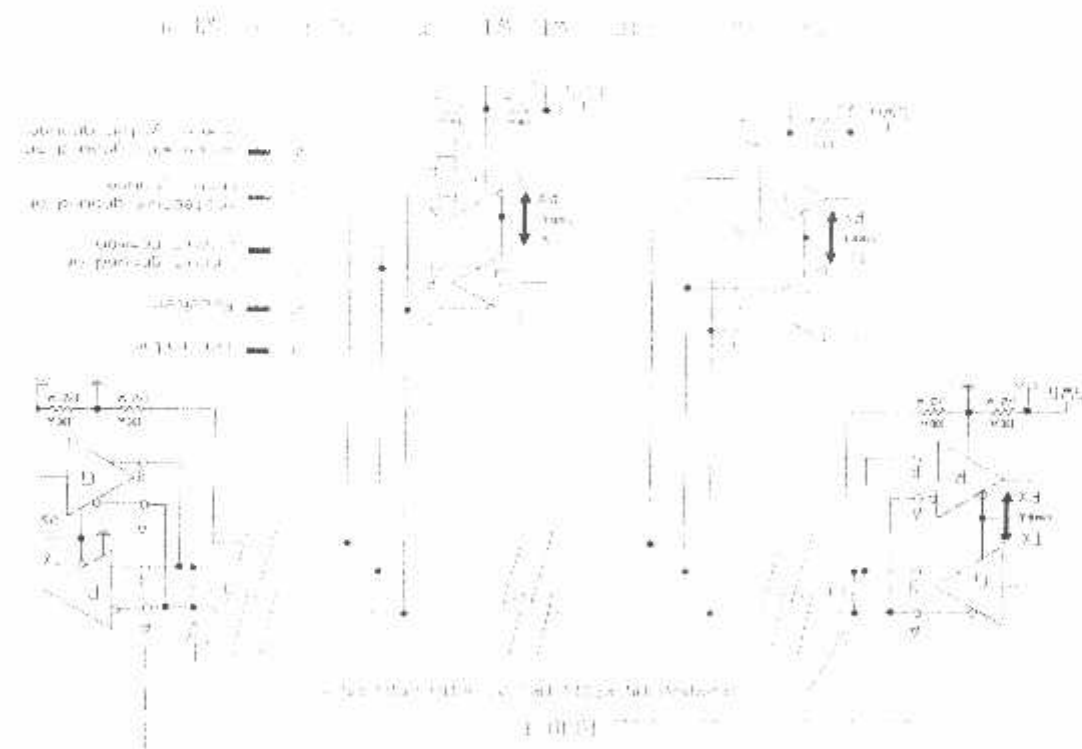


Figure 2.2 Typical RS-485 Two Wire Multidrop Network



Figure 2.3 Parallel and AC Termination

Biasing an RS-485 Network

When an RS-485 network is in an idle state, all nodes are in listen (receive) mode. Under this condition there are no active drivers on the network. All drivers are tristated. Without anything driving the network, the state of the line is unknown. If the voltage level at the receiver's A and B inputs is less than ± 200 mV the logic level at the output of the receivers will be the value of the last bit received. In order to maintain the proper idle voltage state, bias resistors must be applied to force the data lines to the idle condition. Bias resistors are nothing more than a pullup resistor on the data A line (typically to 5 volts) and a pulldown (to ground) on the data B line. Figure 2.4 illustrates the placement of bias resistors on a transceiver in a two-wire configuration. Note that in an RS-485 four-wire configuration, the bias resistors should be placed on the receiver lines. The value of the bias resistors is dependent on termination and number of nodes in the system. The goal is to generate enough DC bias current in the network to maintain a minimum of 200 mV between the B and A data line. Consider the following two examples of bias resistor calculation.

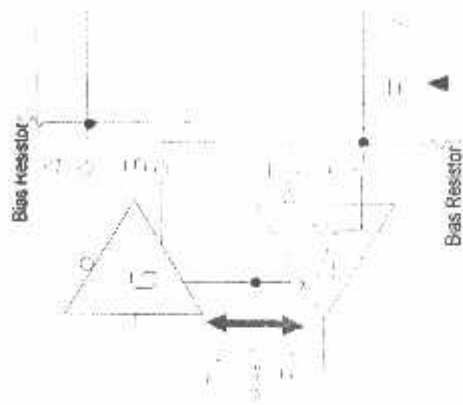


Figure 2.4 Transceiver with Bias Resistors

Example 1. 10 node, RS-485 network with two 120 Ω termination resistors

Each RS-485 node has a load impedance of 12K Ω . 10 nodes in parallel give a load of 1200 Ω . Additionally, the two 120 Ω termination resistors result in another 60 Ω load, for a total load of 57 Ω . Clearly the termination resistors are responsible for a majority of the loading. In order to maintain at least 200mV between the B and A line, we need a bias current of 3.5 mA to flow through the load. To create this bias from a 5V supply a total series resistance of 1428 Ω or less is required. Subtract the 57 Ω that is already a part of the load, and we are left with 1371 Ω . Placing half of this value as a pullup to 5V and half as a pulldown to ground gives a maximum bias resistor value of 685 Ω for each of the two biasing resistors.

² Refer to Chapter 7 for information on National Semiconductors Application Notes.

RS-422/485 Application Note

© Copyright B&B Electronics - Revised 2508
B&B Electronics Mfg Co - 707 Dayton Rd - PO Box 1040 - Ottawa IL 61350 - Ph 815-433-5100 - Fax 815-433-5104
B&B Electronics Ltd - Wexlink Comm. Pl - Oremore, Galway, Ireland - Ph 353-91-792444 - Fax 353-91-792445

CAUTION: Selection of RS-422 and RS-485 cable is critical. Attention to a few details in the selection process can prevent the costly prospect of re-pulling thousands of feet of cable.

Number of Conductors

The signal ground conductor is often overlooked when ordering cable. An extra twisted pair must be specified to have enough conductors to run a signal ground. A two-wire system then requires two twisted pair, and a four-wire system requires three twisted pair.

Shielding

It is often hard to quantify if shielded cable is required in an application or not. Since the added cost of shielded cable is usually minimal it is worth installing the first time.

Cable Characteristics

When choosing a transmission line for RS-422 or RS-485, it is necessary to examine the required distance of the cable and the data rate of the system. The Appendix to EIA RS-422-A Standard presents an empirical curve that relates Cable Length to Data Rate for 24 AWG twisted-pair telephone cable that has a shunt capacitance of 16 pF/ft. and is terminated in 100 ohms (see Figure 3.1). This curve is based on signal quality requirements of:

- Signal rise and fall time equal to, or less than, one-half unit interval at the applicable modulation rate.
- The maximum voltage loss between driver and load of 6 dB.

Each RS-485 node has a load impedance of 12K Ω . 32 nodes in parallel give a total load of 375 Ω . In order to maintain at least 200 mV across 375 Ω we need a current of 0.53 mA. To generate this current from a 5V supply requires a total resistance of 9375 Ω maximum. Since 375 Ω of this total is in the receiver load, our bias resistors must add to 9K Ω or less. Notice that very little bias current is required in systems without termination.

Bias resistors can be placed anywhere in the network or can be split among multiple nodes. The parallel combination of all bias resistors in a system must be equal to or less than the calculated biasing requirements. B&B Electronics uses 4.7K Ω bias resistors in all RS-485 products. This value is adequate for most systems without termination. The system designer should always calculate the biasing requirements of the network. Symptoms of under biasing range from decreased noise immunity to complete data failure. Over biasing has less effect on a system, the primary result is increased load on the drivers. Systems using port powered RS-232 to RS-485 converters can be sensitive to over biasing.

Extending the Specification

Some systems require longer distances or higher numbers of nodes than supported by RS-422 or RS-485. Repeaters are commonly used to overcome these barriers. An RS-485 repeater such as B&B Electronics' 485OP can be placed in a system to divide the load into multiple segments. Each "refreshed" signal is capable of driving another 4000 feet of cable and an additional 31 RS-485 loads.

Another method of increasing the number of RS-485 nodes is to use low load type RS-485 receivers. These receivers use a higher input impedance to reduce the load on the RS-485 drivers to increase the total number of nodes. There are currently half and quarter load integrated circuit receivers available, extending the total allowable number of nodes to 64 and 128.

IEEE 1151-1151 step upwards protecting an RS-422 or RS-485 system from transients is understanding the nature of the energy we are guarding against. Transient energy may come from several sources, most typically environmental conditions or induced by switching heavy inductive loads.

What does a surge look like?

Surge Specifications

While transients may not always conform to industry specifications, both the Institute of Electrical and Electronics Engineers (IEEE) and the International Electrotechnical Commission (IEC) have developed transient models for use in evaluating electrical and electronic equipment for immunity to surges. These models can offer some insight into the types of energy that must be controlled to prevent system damage.

Both IEC 1000-4-5: 1995 "Surge Immunity Test" and IEEE C62.41-1-1991 "IEEE Recommended Practice on Surge Voltages in Low-Voltage AC Power Circuits" define a "1.2/50µs - 8/20µs combination wave" surge which has a 1.2 µs voltage rise time with a 50 µs decay across an open circuit. The specified current waveform has an 8 µs rise time with a 20 µs decay into a short circuit. Open circuit voltages levels from 1 to 6 kV are commonly used in both the positive and negative polarities, although, under some circumstances, voltages as high as 20 kV may be applied. Figures 4.1 and 4.2 illustrate the combination wave characteristics. In addition, IEEE C62.41 also specifies a 100 kHz "ring wave" test. The ring wave has a 0.5 µs rise time and a decaying oscillation at 100 kHz with source impedance of 12Ω as shown in Figure 4.3. Typical amplitudes for the 100 kHz ring wave also range from 1 - 6 kV.

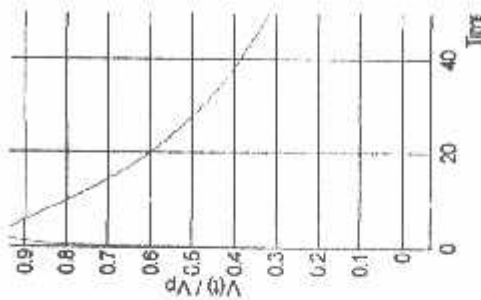


Figure 4.1 Combination Wave Voltage Waveform

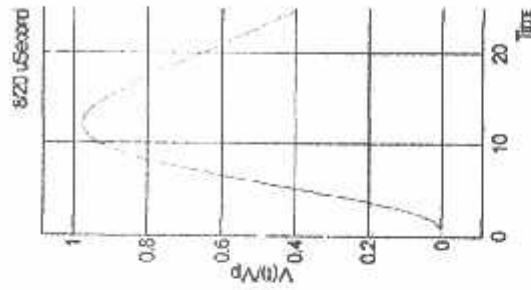


Figure 4.2 Combination Wave Current Waveform

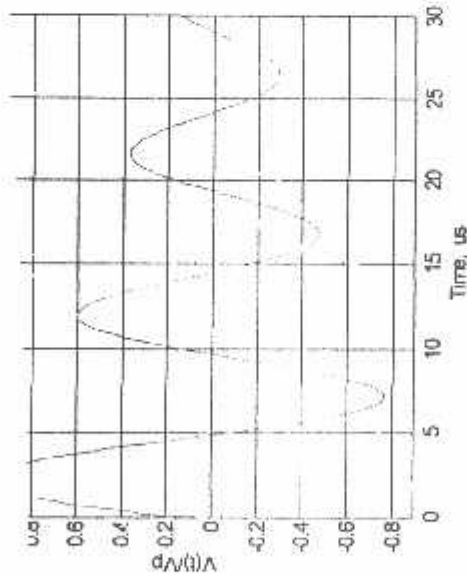


Figure 4.3 100 kHz Ring Wave

Common Mode vs. Differential Mode

Identifying the type of surges that may threaten a system is an important part of selecting the appropriate levels and methods of transient protection. Since each of the conductors in a data cable travels through the same physical space, it is reasonable to expect transients caused by environmental or current switching to be "common mode" that is, present on all data and ground conductors within the data cable. In some installations, there may be another source of unwanted energy to consider. If there are high voltage cables running anywhere near the data cables, the potential for a fault condition exists as a result of insulation failures or inadvertent contact by an installer. This type of surge could contact any number of conductors in the data cable, presenting a "differential" surge to the data equipment. Although the voltages and currents associated with this type surge are much lower than the types of surges modeled by ANSI or IEC, they have a particularly destructive quality of their own. Instead of dissipating within several milliseconds, they can exist in a steady state condition on the data network.

Realizing that transient energy can be high frequency in nature leads to some disturbing observations. At frequencies of this magnitude, it is difficult to make a low impedance electrical connection between two points due to the inductance of the path between them. Whether that path is several feet of cable or thousands of feet of earth between grounding systems, during a transient event there can be hundreds or thousands of volts potential between different "grounds". We can no longer assume that two points connected by a wire will be at the same voltage potential. To the system designer this means that although RS-422/485 uses 5V differential signaling, a remote node may see the 5V signal superimposed on a transient of hundreds or thousands of volts with respect to that nodes local ground. It is more intuitive to refer to what is commonly called "signal ground" as a "signal reference".

How do we connect system nodes knowing that these large potential differences between grounds may exist? The first step towards successful protection is to assure that each device in the system is referenced to only one ground, eliminating the path through the device for surge currents searching for a return. There are two approaches to creating this idyllic ground state. The first approach is to isolate the data ground from the host device ground, this is typically done with transformers or optical isolators as shown in Figure 4.4. The second approach is to tie each of the grounds on a device together (typically power ground and data ground) with a low impedance connection as shown in Figure 4.5. These two techniques lead us to the two basic methods of transient protection.

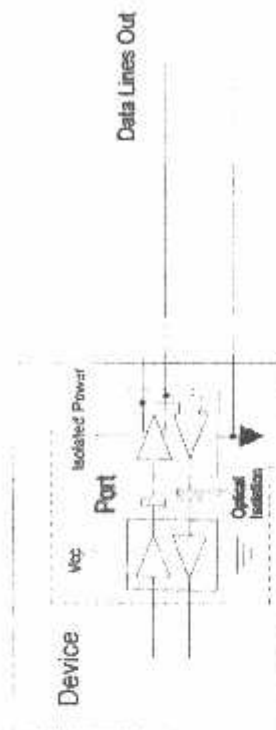
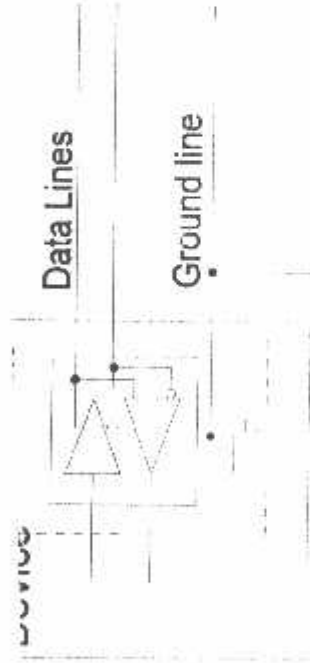


Figure 4.4 Isolated RS-485 Device



Local Chassis Ground Connection
Figure 4.5 RS-485 Device with Signal Ground
Connected to Chassis Ground

Transient Protection using Isolation

Isolation Theory

The most universal approach to protecting against transients is to galvanically isolate the data port from the host device circuitry. This method separates the signal reference from any fixed ground. Optical isolators, transformers and fiber optics are all methods commonly used in many types of data networks to isolate I/O circuitry from its host device. In RS-422 and RS-485 applications, optical isolators are most common. An optical isolator is an integrated circuit that converts the electrical signal to light and back, eliminating electrical continuity. With an isolated port, the entire isolated circuitry floats to the level of the transient without disrupting data communications. As long as the floating level of the circuitry does not exceed the breakdown rating of the isolators (typically 1000 - 2500 volts) the port will not be damaged. This type of protection does not attempt to absorb or shunt excess energy so it is not sensitive to the length of the transient. Even continuous potential differences will not harm isolated devices. It is important to note that isolators work on common mode transients; they cannot protect against large voltage differences between conductors of a data cable such as those caused by short circuits between data and power circuits.

Optical isolation can be implemented in a number of ways. If a conversion from RS-232 to RS-422 or RS-485 is being made, optically isolated converters are available. Optically isolated ISA bus serial cards can replace existing ports in PC systems. For systems with existing RS-422 or RS-485 ports, an optically isolated repeater can be installed. Examples of each of these type devices can be found in the B&B Electronics Data Communications catalog.

Transient Protection using Shunting

Shunting Theory

Creating one common ground at the host device provides a safe place to divert surge energy as well as a voltage reference to attach surge suppression devices to. Shunting harmful currents to ground before they reach the data port is the job of components such as TVS (often referred to by the trade name Transorb), MOV or gas discharge tubes. These devices all work by "clamping" at a set voltage, once the clamp voltage has been exceeded, the devices provide a low impedance connection between terminals.

Since this type of device diverts a large amount of energy, it cannot tolerate very long duration or continuous transients. Shunting devices are most often installed from each data line to the local earth ground, and should be selected to begin conducting current at a voltage as close as possible above the systems normal communications levels. For RS-422 and RS-485 systems, the voltage rating selected is typically 6 - 8 volts. These devices typically add some capacitive load to the data lines. This should be considered when designing a system and can be compensated for by derating the total line length to compensate for the added load. Several hundred feet is usually adequate.

To apply these type products correctly they should be installed as close to the port to be protected as possible, and the user must provide an extremely low impedance connection to the local earth ground of the unit being protected. This ground connection is crucial to proper operation of the shunting device. The ground connection should be made with heavy gauge wire and kept as short as possible. If the cable must be longer than one meter, copper strap or braided cable intended for grounding purposes must be used for the protection device to be effective. In addition to the high frequency nature of transients, there can be an enormous amount of current present. Several thousand amps typically result from applications of the combination wave test in the ANSI and IEC specification.

be considered. During transient events a high voltage potential may exist between the remote grounds. Only the impedance in the wire connecting the grounds limits the current that results from this voltage potential. The RS-422 and RS-485 specification both recommend using 100 ohm resistors in series with the signal ground path in order to limit ground currents. Figure 4.6 illustrates the ground connection recommended in the specification.



Figure 4.6 Signal Ground Connection between two nodes with 100 ohm resistor

Shunting Devices

There are two types of shunting devices to choose from. The least expensive type is single stage, which usually consists of a single TVS device on each line. Three stage devices are also available. The first stage of a three-stage device is a gas discharge tube, which can handle extremely high currents, but has a high threshold voltage and is too slow to protect solid state circuits. The second stage is a small series impedance which limits current and creates a voltage drop between the first and third stage. The final stage is a TVS device that is fast enough to protect solid state devices and brings the clamping voltage down to a safe level for data circuits.

Combining Isolation and Shunting

Installing a combination of both types of protection can offer the highest reliability in a system. Figures 4.7 and 4.8 illustrate two means of implementing this level of protection.

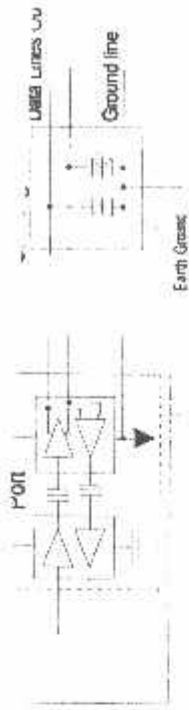


Figure 4.7 Isolated node with shunt protection to earth ground

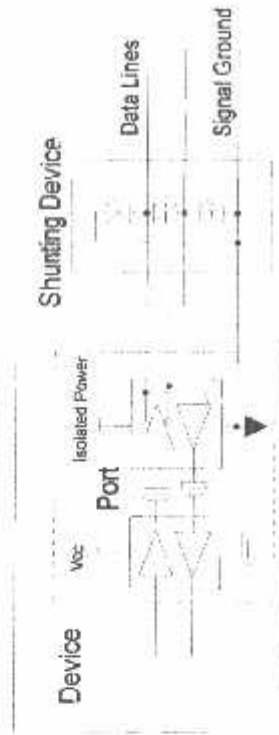


Figure 4.8 Isolated port with ungrounded shunt protection

The method shown in Figure 4.7 is recommended, in this case isolation protects the circuit from any voltage drops in the earth ground connection. The shunt devices will prevent a surge from exceeding the breakdown voltage of the isolators as well as handling any differential surges on the cable. Figure 4.8 illustrates a method recommended for cases where there is no way to make an earth ground connection. Here, the shunt device's function is to protect the port from differential surges, a differential surge will be balanced between conductors by the shunting device, converted to common mode. The isolation provides protection from the common mode transient remaining.

require an extra measure of protection. In these cases its recommended to add a fuse type device in addition to shunting type suppression, as shown in Figure 4.9. When a short circuit occurs, the shunt suppression will begin conducting, but shunting by itself cannot withstand the steady state currents of this type of surge. A small enough fuse value should be chosen so that the fuse will open before the shunt device is damaged. A typical fuse value is 125 mA.



Figure 4.9 Fused port protection

Choosing the right protection for your system

While it is hard to predict what type and level of isolation is correct for a system, an educated guess should be made based on the electrical environment, physical conditions and cost of failures in downtime and repair costs. Systems connected between two power sources, such as building to building, office to factory floor, or any system covering long distances should require some level of transient protection. Table 4.1 is a comparison of transient protection techniques.

Optical Isolation	Shunting
Requires no ground reference	Must have low impedance ground path
Adds no loading to data lines	Presents additional capacitive loading to data lines
Higher complexity	Lower complexity, uses passive components
Effective on common mode transients	Effective on both common and differential mode transients
Not dependent on installation quality	Can be improperly installed by user
Requires an external power source	No power required
Not affected by long term or continuous transients	Subject to damage by long duration transients

INTRODUCTION

RS-422 and RS-485 are hardware specifications. Software protocol is not discussed in either specification. It is up to the system designer to define a protocol suitable for their system. This chapter will not attempt to define a protocol standard, but will explain some of the issues that should be considered by the system designer, whether writing or purchasing software.

RS-422 Systems

RS-422 system software differs little from the familiar point-to-point RS-232 communication systems. RS-422 is often used to simply extend the distance between nodes over the capabilities of RS-232. RS-422 can also be used as the master node in a four-wire master-slave network described later in this chapter. When selecting or writing software for RS-422 systems the designer should be aware of the signals being used by the hardware in the system. Many RS-422 systems do not implement the hardware handshake lines often found in RS-232 systems due to the cost of running additional conductors over long distances.

RS-485 Driver Control

The principle difference between RS-422 and RS-485 is that the RS-485 driver can be put into a high impedance, tristate mode, which allows other drivers to transmit over the same pair of wires. There are two methods of tristating an RS-485 driver. The first method is to use a control line, often the RTS handshake line, to enable and disable the driver. This requires that the host software raise the RTS line before beginning a transmission to enable the driver, then lower the RTS line after the completion of the transmission. Since only a single RS-485 driver can be enabled on a network at one time it is important that the driver is disabled as quickly as possible after transmission to avoid two drivers trying to control the lines simultaneously, a condition called line contention. Under some operating systems it can be difficult to lower RTS in a timely manner and this method of driver control should be avoided altogether.

The second method of RS-485 driver control we refer to as Automatic Send Data Control. This type of control involves special circuitry that senses when data is being transmitted and automatically enables the driver as well as disabling the driver within one character length of the end of transmission. This is the preferred method of driver control since it reduces software overhead and the number of potential pitfalls for the programmer.

RS-422/485 Application Note

© Copyright B&B Electronics - Revised 2508
B&B Electronics Mfg Co - 707 Dayton Rd - PO Box 1040 - Ottawa IL 61330 - Ph 815-433-5100 - Fax 815-433-5104
B&B Electronics Ltd - Wexlink Comm. Plc - Oranmore, Galway, Ireland - Ph 353-91-792444 - Fax 353-91-792445

LOOPBACK RECEIVER CONTROL

The RS-485 receiver also has an enable signal. Since RS-485 systems using a two-wire configuration connect the driver to receiver in a loopback fashion, this feature is often used to disable the receiver during transmission to prevent the echo of local data. Another approach is to leave the RS-485 receiver enabled and monitor the loopback data for errors which would indicate that line contention has occurred. Although a good loopback signal does not guarantee data integrity it does offer a degree of error detection.

Master-Slave Systems

A master-slave type system has one node that issues commands to each of the "slave" nodes and processes responses. Slave nodes will not typically transmit data without a request from the master node, and do not communicate with each other. Each slave must have a unique address so that it can be addressed independent of other nodes. These type systems can be configured as two-wire or four-wire. Four-wire systems often use an RS-422 master (the driver is always enabled) and RS-485 slaves to reduce system complexity.

Four Wire Master-Slave Systems

This configuration reduces software complexity at the host since the driver and receiver are always enabled, at the expense of installing two extra conductors in the system. The Master node simply prefixes commands with the appropriate address of the slave. There is no data echo or turn around delays to consider. Since each of the slave transmitters share the same pair of wires, care must be taken that the master never requests data from multiple nodes simultaneously or data collisions will result.

Two Wire Master-Slave Systems

Two wire configurations add a small amount of complexity to the system. The RS-485 driver must be tristated when not in use to allow other nodes to use the shared pair of wires. The time delay between the end of a transmission and the tristate condition becomes a very important parameter in this type system. If a slave attempts to reply before the master has tristated the line, a collision will occur and data will be lost. The system designer must know the response time or turn around delay of each of the slave nodes and assure that the master will tristate its driver within that amount of time. B&B Electronics' Automatic Send Data control circuits tristate the driver within one character length of the end of a transmission.

RS-422/485 Application Note

© Copyright B&B Electronics - Revised 2508
B&B Electronics Mfg Co - 707 Dayton Rd - PO Box 1040 - Ottawa IL 61330 - Ph 815-433-5100 - Fax 815-433-5104
B&B Electronics Ltd - Wexlink Comm. Plc - Oranmore, Galway, Ireland - Ph 353-91-792444 - Fax 353-91-792445

EIA Standards and Publications can be purchased from:

GLOBAL ENGINEERING DOCUMENTS

7730 Carondelet Avenue
Clayton, MO 63105
Phone: (800) 854-7179
FAX: (314) 726-6418

GLOBAL ENGINEERING DOCUMENTS

15 Inverness Way East
Englewood, CO 80112
Phone: (800) 854-7179
FAX: (303) 397-2740

Global Engineering Documents web site can be found at <http://global.lhs.com>.

Related data interface standards are:

- EIA-232-E Interface between data terminal equipment and data circuit-terminating equipment employing serial binary data interchange (ANSI/EIA-232-D)
- EIA-422-A Electrical characteristics of balanced voltage digital interface circuits
- EIA-423-A Electrical characteristics of unbalanced voltage digital interface circuits
- EIA-485 Standard for electrical characteristics of generators and receivers for use in balanced digital multipoint systems
- EIA-449 General purpose 37-position and 9-position interface for data terminal equipment and data circuit-terminating equipment
- EIA-530 High speed 25-position interface for data terminal equipment and data circuit-terminating equipment
- EIA/TIA-562 Electrical characteristics for an unbalanced digital interface

Manufacturers of integrated circuit data transceivers often offer practical application information for RS-422 and RS-485 systems.

National Semiconductor's Interface Data Book includes a number of excellent applications notes. These notes are also available online at <http://www.national.com/>. A search engine is provided to search the text of the available application notes. Entering "422" or "485" as search criteria to get a current list of related application notes.

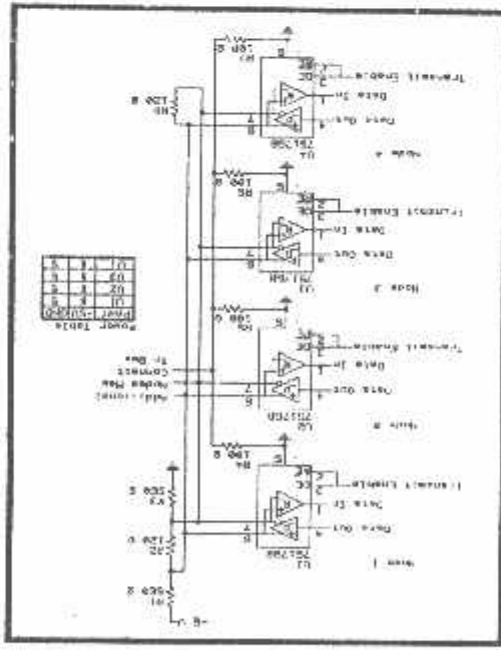
RS-422/485 Application Note

© Copyright B&B Electronics - Revised 2506
B&B Electronics Mfg Co - 707 Dayton Rd - PO Box 1040 - Ottawa IL 61350 - Ph 815-433-5100 - Fax 815-433-5104
B&B Electronics Ltd - Westlink Comm. Plc - Oranmore, Galway, Ireland - Ph 353-91-792444 - Fax 353-91-792445

EIA RS-422 Specification Summary				
Parameter	Conditions	Min	Max	Units
Driver Output Voltage Open Circuit			10	V
Driver Output Voltage Loaded	$R_T = 100 \Omega$	2	-10	V
Driver Output Resistance	A to B	-2		V
Driver Output Short-Circuit Current	Per output to common		100	mA
Driver Output Rise Time	$R_T = 100 \Omega$		± 150	nA
Driver Common Mode Voltage	$R_T = 100 \Omega$		10	% of Bit Width
Receiver Sensitivity	$V_{cm} \leq \pm 7$		± 3	V
Receiver Common-Mode Voltage Range		-7	± 200	mV
Receiver Input Resistance Differential Receiver	Operational: Withstand:	4000	± 10	Ω
			± 12	V

EIA RS-485 Specification Summary				
Parameter	Conditions	Min	Max	Units
Driver Output Voltage Open Circuit		1.5	6	V
Driver Output Voltage Loaded	$R_{LOAD} = 54 \Omega$	-1.5	-6	V
Driver Output Short-Circuit Current	Per output to +12V or -7V	1.5	5	V
Driver Output Rise Time	$R_{LOAD} = 54 \Omega$ $C_{LOAD} = 50 \text{ pF}$	-1.5	-5	V
Driver Common Mode Voltage	$R_{LOAD} = 54 \Omega$		± 250	nA
Receiver Sensitivity	$-7 \leq V_{cm} \leq +12$	-1	3	% of Bit Width
Receiver Common-Mode Voltage Range		-7	± 200	mV
Receiver Input Resistance		12K	112	V
				Ω

Figure 1—This general-purpose RS-485 network can have up to 32 nodes. Biasing resistors ensure that there are no false start bits when no drivers are enabled.



to any asynchronous serial port. Many network circuits also require a port bit to control each transceiver's driver-enable input. Ports designed for RS-232 communications can use the RTS output. If that's not available, any spare output bit will do.

Most serial-communications tools, including Visual Basic's MSComm, support RS-485 communications with RTS control in software. The COMMDRV serial-port drivers from WICS have automatic RTS control built-in.

The main reason why RS-485 links can extend so far is their use of balanced, or differential, signals. Two wires (usually a twisted pair) carry the signal voltage and its inverse. The receiver detects the difference between the two. Because most noise that couples into the wires is common to both wires, it cancels out.

In contrast, interfaces like RS-232 use unbalanced, or single-ended, signals. The receiver detects the voltage difference between a signal voltage and a common ground.

The ground wire tends to be noisy because it carries the return currents for all of the signals in the interface, along with whatever other noise has entered the wire from other sources.

And noise on the ground wire can cause the receiver to misread transmitted logic levels.

The datasheets for interface chips label the noninverted RS-485 line as line A and the inverted line as line B. An RS-485 receiver must see a voltage difference of just 200 mV between A and B. If A is at least 200 mV greater than B, the receiver's output is a logic high. If B is at least 200 mV greater than A, the output is a logic low. For differences less than 200 mV, the output is

undefined.

At the driver, the voltage difference must be at least 1.5 V, so the interface tolerates a fair amount of non-common-mode noise and attenuation.

Vendors for RS-485 transceivers include Linear Technology, Maxim, National Semiconductor, and Texas Instruments. These companies are also excellent sources for application notes containing circuit examples and explanations of the theory behind them.

RS-485 is designed to be wired in a daisy-chain or bus topology. Any stubs that connect a node to the line should be as short as possible. Most links use twisted pairs because of their ability to cancel magnetically and electro-

magnetically coupled noise.

GENERAL-PURPOSE LINK

Figure 1 shows a general-purpose RS-485 network. Each node has a Texas Instruments SN75176B transceiver that interfaces between RS-485 and TTL logic levels.

The chip has a two-wire RS-485 interface, a TTL driver input and receiver output, and TTL enable inputs for the driver and receiver. Similar chips include Linear Technology's LTC485, Maxim's MAX485, and National Semiconductor's DS3695.

The circuit has two 120-ohm terminating resistors connected in parallel at or just beyond the final node at each

end of the link. One end of the line also has two 560-ohm biasing resistors. The terminations reduce voltage reflections that can cause the receiver to misread logic levels. The reflected voltages as output switches and the line settles from its initial current to its final current. The termination eliminates reflections by matching the initial and final currents equal to the line's characteristic impedance. The value varies with the wires' diameters, the space between them, and the insulation. For digital signals (which consist mainly of frequencies greater than 100 kHz), the characteristic impedance is mostly resistive; the inductive and capacitive components are small. A typical value for 24-AWG twisted pair is 120 ohms.

The final current is a function of the line termination, the receiver's input impedance, and the line's series impedance. In a typical RS-485 line without a termination, the initial current is greater than the final current because the characteristic impedance is less than the receivers' combined input impedance.

On a line without a termination, the first reflection occurs when the initial current reaches the receiver. The receiver's input can absorb only a fraction of the current. The rest reflects back to the driver. As the current reverses direction, its magnetic field collapses and induces a voltage on the line. As a result, the receiver initially sees a greater voltage than what was transmitted.

When the reflected voltage reaches the driver, which has a lower impedance than the line, the driver absorbs some of the reflection and bounces the rest back to the receiver. This reflection is of opposite polarity to the first reflection and causes the receiver to see a reduced voltage. The reflection bounce back and forth like this for a few rounds before they die out and the line settles to its final current.

If the line terminates with a resistor equal to the line's characteristic impedance, there are no reflections. When the initial current reaches the termination, it is absorbed and the line settles to its final current.

The circuit has two 120-ohm terminating resistors connected in parallel at or just beyond the final node at each

When the receiver is disabled, the receiver's output is high impedance. If the output doesn't connect to a pull-up with an internal pulldown, adding a pull-up here ensures that the node doesn't see false start bits when its receiver is disabled. To comply with the specification, all of the nodes must share a common ground connection. This ground may

A general guideline is to read the signal before the reflections die out long system. On a short line, rather than distributed, behaves as a lumped, short, which means it the line is electrically component. This option is feasible if by not using terminating and biasing you can save power and components. For some shorter and slower links, impedance of 375 Ω to ground or V_{+} 32-unit loads have a combined parallel the number of receivers. The maximumers' input impedances and varies with the parallel combination of the receiver, without terminations, the load is ing, attenuation, etc.).

Adding terminations increases a link's power consumption. With two parallel 120 Ω terminations and a differential output of 1.5 V, the current through the combined terminations is 25 mA (disregarding the effects of biasing, attenuation, etc.). Without terminations, the load is the parallel combination of the receiver's input impedances and varies with the number of receivers. The maximum 32-unit loads have a combined parallel impedance of 375 Ω to ground or V_{+} . For some shorter and slower links, you can save power and components by not using terminating and biasing component. This option is feasible if the signal lines short together.

SIMPLIFIED LOW-POWER LINK

The RS-485 specification recommends connecting a 100- Ω resistor of at least 0.5 W in series between each node's signal ground and the network's ground wire, as Figure 1 shows. This way, if the ground potentials of two nodes vary, the resistors limit the current in the ground wire.

The ground wire provides a path for the current that results from small imbalances in the balanced line. If the A and B outputs balance exactly with equal, opposite currents, the two currents in the ground wire cancel each other out and the wire carries no current at all. In real life, components don't balance perfectly; one driver will be a little stronger and one receiver will have a slightly larger input impedance.

Without a common ground, the circuit may work, but the energy from and may dissipate as electromagnetic radiation.

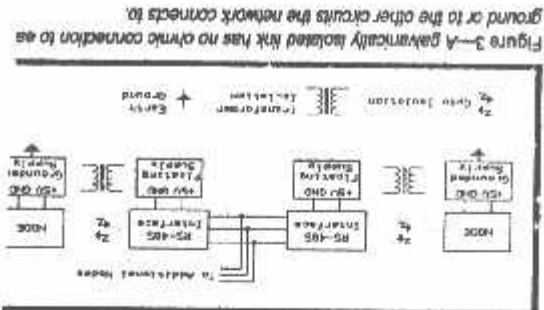
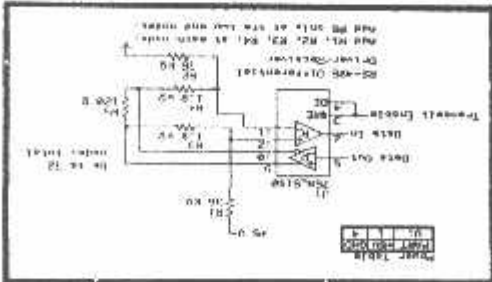
The RS-485 specification recom-

With no termination and when no drivers are enabled, the biasing resistors hold line A more positive than line B. When you add two 120- Ω terminations, the difference between A and B shrinks to a few millivolts, much less than the required 200 mV. The solution is to add smaller resistors in parallel with the internal biasing so that a greater proportion of the series voltage drops across the termination.

The biasing resistors hold the line in a known state when no drivers are enabled. Most RS-485 transceivers have internal biasing circuits, but adding a termination defeats their ability to bias the line. A typical internal circuit is a 100-k Ω pullup from line A to V_{+} and a 100-k Ω pulldown from line B to ground.

expecting—a load equal to the line's characteristic impedance. The entire transmitted voltage drops across the load. In a network with two parallel terminations, the drivers drive two lines with each ending at a termination.

Figure 2—The biasing resistors in this network hold the receiver's inputs in an idle state when no drivers are enabled, or if the node disconnects from the network, or if the signal lines are shorted.



The previous circuits ensured the line was in a predictable state with idle or open. The circuit in Figure 2 also protects the network as much as possible if the signal lines are shorted instead of a single pair of biasing resistors for the entire line. The circuit has four biasing resistors at each node. The circuit uses Texas Instruments 75ALS180B transceivers, which have full-duplex RS-485 inputs and output enable the receiver to have its own series biasing resistors. The two RS-485 lines connect just beyond the biasing lines connect just beyond the biasing

The rise time is specified in the driver's datasheet. The slowest cl I've found is Maxim's MAX3080. a minimum rise time of 667 ns. V cables of up to 100', the rise time greater than four times the one-way delay (4×150 ns), so the line behaves as a short line and doesn't need terminating or biasing. Another advantage is that the internal biasing pulls id lines to nearly V_{+} and ground, so y get greater noise immunity.

The downside to using this chip is that the slow rise time means that rated for use only at 115,200 bps or l greater than four times the signals travel from the driver to the receiver amount of time needed for a signal path for the current that results from small imbalances in the balanced line. If the A and B outputs balance exactly with equal, opposite currents, the two currents in the ground wire cancel each other out and the wire carries no current at all. In real life, components don't balance perfectly; one driver will be a little stronger and one receiver will have a slightly larger input impedance.

Without a common ground, the circuit may work, but the energy from and may dissipate as electromagnetic radiation.

The RS-485 specification recom-

tion with the 36-k Ω biasing resistors hold input A more positive than B. (Of course, the node can't communicate with the network if the line is open or shorted, but at least it remains in an idle state with no false start bits) until the problem is fixed. Another way to accomplish the same thing is to use transceivers with built-in fail-safe protection for open and short circuits. Chips that have this feature take varying approaches. Linear Technologies' LTC1482 has a carrier-detect function that brings the receiver's output high when the differential input voltage is too small to be a valid logic level. The chip has a carrier-detect output that indicates when the line is in an invalid state. National Semiconductor's DS36276 has internal circuits that bring the receiver's output high if the line is shorted or open. Maxim's MAX3080-89 series provide short-circuit biasing by redefining the threshold for logic 0. Instead of specifying all differential inputs of less than 200 mV as undefined, those chips define a differential voltage of -50 mV or greater as a logic 0. Voltages equal to or more negative than -200 mV remain defined as logic 1. The only undefined region is from -50 to -200 mV. With these definitions a shorted line (which results in a differential input of 0 V) is a logic 0, which results in a high output at the receiver. The entire RS-485 network has to share a ground, but the network can be galvanically isolated from other circuits the network connects to as well as from earth ground. All RS-485 components must be able to operate with common-mode voltages between -7 V and +12 V. Some components have higher ratings. The common-mode voltage at the receiver equals half the sum of the two signal voltages, referred to the receiver's signal ground. The voltage varies with the difference in signal voltages, the difference in ground potentials between the driver and receiver, and noise on the line. Where the ground connection is long, isolating the ground can ensure that the components don't exceed their ratings. Isolation also protects the cir-

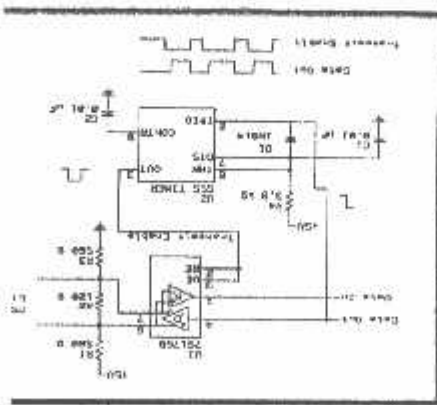
ISOLATED LINK

One of challenges in designing an RS-485 link is controlling the driver-cable lines. Because all of the nodes share a data path, only one driver can be enabled at a time. Before transmitting, a driver must be sure that the previous driver has been disabled. Many RS-485 networks use a command/response protocol; one node sends commands and the node being addressed returns a response. The UART in the node being addressed detects the final stop bit in the middle of the bit width, or slightly sooner or later if the sender's clock doesn't match exactly. A very fast node may be ready to send a reply within a few microseconds after detecting the stop bit. To prevent the need for a delay before responding, the sending node's driver should be disabled as soon as possible after the leading edge of its final stop bit. In most systems, the transmitting driver is enabled on the leading edge of the start bit and remains enabled for as long as possible after the final stop bit. In the delays between transmissions, biasing holds the line in an idle state. There are various ways that the transmitting node can determine when a transmission has finished and it is safe to disable the driver. The node may read back what it sent, or it may

AUTO-SWITCHING LINK

Complete isolation requires isolating the power supplies and the network's signals. The power supplies typically use transformer isolation, whereas the signals use optoisolators (see Figure 3). A one-chip way to achieve isolation is to use Maxim's MAX1480, which contains its own transformer-isolated supply and optoisolated signal path.

Figure 4—This circuit's automatic driver-enable ensures that the previous driver is disabled by the time the next node begins to transmit. The driver-enable line follows the data with a short delay before disabling the driver. Biasing circuitry holds the line in the correct state when the driver is disabled.



use a hardware or software timer to estimate the time needed to transmit. Figure 4 shows a completely automatic way to control the enable line the driver is disabled as quickly as possible, soon after the leading edge of the stop bit. With this circuit, the program code doesn't have to toggle signal to enable and disable the driver and a transmitting driver doesn't need to allow extra time to be sure that the previous driver has been disabled. Unlike other methods of automatic control, there are no jumpers to set. A particular bit rate. I learned of this method when I saw it in R.F. Smith IRSPC24 Isolated RS-485 board. Instead of keeping the transmitter enabled for the entire transmission, the circuit in Figure 4 enables the driver on the leading edge of the start bit or any logic low at the driver's input. It also disables the driver -40 μ s after the leading edge of the stop bit or any logic high at the driver's input. When the driver is disabled, biasing resistors ensure the receiver's output is a logic high. The delay is generated by a 555 timer configured as a monostable (one shot). The enable inputs of the driver and receiver are tied together so the receiver is disabled when the driver transmits. The timer's output controls the transceiver's enable inputs. A falling edge at Data Out indicates a start bit and triggers the timer. The timer's output goes high, enabling the driver line A. Diode feedback to the Trig input holds the timer's output high for as long as Trig remains low. When Data Out goes high, the RS-485 line switches, bringing line A more positive than line B. The same logic

©Circuit Cellar Inc., the Computer Applications Journal
 Reprinted by permission. For subscription information
 call (860) 875-2199 or subscribe @circuitcellar.com

SOURCES

RS-485 transceivers

Linear Technology
 (408) 432-1900
 Fax: (408) 434-0507
 www.linear-tech.com
 Maxxim Integrated Products
 (408) 737-7600

REFERENCE

high also causes the timer to begin timing out. About 40 μ s after the rising edge, the timer's output goes low, disabling the driver.

The delay ensures that the driver's RS-485 output switches without delay, while the driver is enabled. When the driver is disabled, the biasing components continue to hold A more positive than B.

Similarly, any falling edges in the transmitted data enable the driver and any rising edges disable the driver after the delay. On the final stop bit, the driver is disabled no later than 40 μ s after the stop bit's leading edge.

At rates of 9600 bps or less, the bit width is greater than 100 μ s, which means the driver is disabled at around the middle of the bit width. At faster bit rates, the driver will still be disabled no more than 40 μ s after the stop bit's leading edge. For networks needing very fast response time at faster bit rates, decrease R4 for a shorter delay.

A downside is that the final voltage for logic zeros is the biasing voltage, which is usually less than the differential voltage when the driver is enabled. But because the biasing voltage needs to be great enough to prevent errors from noise on an idle line, it should do the job for active logic states as well.

Jan Axelsson has been involved with computers and electronics for over 20 years. Her books include *Serial Port Complete*, *Parallel Port Complete*, and *The Microcontroller Idea Book*. You may reach her at jan@vr.com or on the web at www.jvr.com.

J. Axelsson, *Serial Port Complete: Programming and Circuits for RS-232 and RS-485 Links and Networks*, Lakeview Research, Madison, WI, 1998.

RS-485 interface with automatic enable control

R.E. Smith
 (513) 874-4796
 Fax: (513) 874-1236
 www.rs485.com

COMM-DRV serial-port drivers (with RS-485 support)

WCS
 (800) 963-4832
 (281) 360-4232
 Fax: (281) 360-3231
 www.wcsnet.com

USB-to-RS-485 converter

Inside Out Networks
 (512) 301-7080
 Fax: (512) 301-7060
 www.ionetworks.com

TIA/EIA-485-A

www.tia.com
 Fax: (972) 995-4360
 (972) 995-2011
 (800) 477-8924, x4500
 Texas Instruments, Inc.

www.national.com
 Fax: (408) 739-9803

(408) 721-5000
 (800) 272-9959
 National Semiconductor

www.maxim-ic.com
 Fax: (408) 737-7194

Global Engineering Documents
 (800) 854-7179
 (303) 397-7956
 Fax: (303) 397-2740
 www.global.tls.com/sitemap.html

B&B Electronics Manufacturing Co.
 (615) 433-5100
 Fax: (815) 434-7094
 www.bb-elec.com

75176B/DS75176BT**tipoint RS-485/RS-422 Transceivers****eral Description**

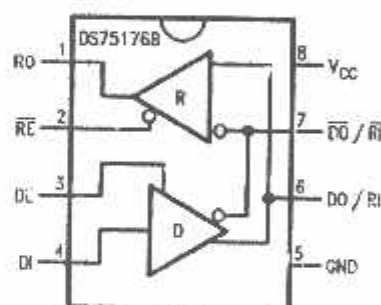
DS75176B is a high speed differential TRI-STATE® transceiver designed to meet the requirements of standard RS485 with extended common mode range ($-7V$ to $+12V$), for multipoint data transmission. In addition, it is compatible with RS-422.

Driver and receiver outputs feature TRI-STATE capability over the entire common mode range of $+12V$ to $-7V$. Bus contention or fault situations cause excessive power dissipation within the device, which is limited by a thermal shutdown circuit, which forces the outputs into the high impedance state.

Specifications are guaranteed over the 0 to $70^{\circ}C$ temperature range and $4.75V$ to $5.25V$ supply voltage range.

Features

- Meets EIA standard RS485 for multipoint bus transmission and is compatible with RS-422.
- Small Outline (SO) Package option available for minimum board space.
- 22 ns driver propagation delays.
- Single $+5V$ supply.
- $-7V$ to $+12V$ bus common mode range permits $\pm 7V$ ground difference between devices on the bus.
- Thermal shutdown protection.
- High Impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down.
- Pin out compatible with DS3695/A and SN75176A/B.
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus.
- 70 mV typical receiver hysteresis.

ection and Logic Diagram

Top View

TL/F/8758-1

Order Number DS75176BN, DS75176BTN, DS75176BM or DS75176BTM
See NS Package Number N08E or M08A

bsolute Maximum Ratings (Note 1)

ary/Aerospace specified devices are required, contact the National Semiconductor Sales /Distributors for availability and specifications.

Supply Voltage, V _{CC}	7V
Differential Input Voltages	7V
Input Voltage	7V
Output Voltages	+15V/ -10V
Differential Input Voltages (DS75176B)	+15V/ -10V
Differential Output Voltage	5.5V
Quiescent Power Dissipation @25°C	
M Package	675 mW (Note 5)
N Package	300 mW (Note 4)

Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V _{CC}	4.75	5.25	V
Voltage at Any Bus Terminal (Separate or Common Mode)	-7	+12	V
Operating Free Air Temperature T _A			
DS75176B	0	+70	°C
DS75176BT	-40	+85	°C
Differential Input Voltage, VID (Note 6)	-12	+12	V

Electrical Characteristics (Notes 2 and 3)

≤ T_A ≤ 70°C, 4.75V < V_{CC} < 5.25V unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Differential Driver Output Voltage (Unloaded)	I _O = 0			5	V
Differential Driver Output Voltage (with Load)	(Figure 1) R = 50Ω; (RS-422) (Note 7) R = 27Ω; (RS-485)	2 1.5			V
Change in Magnitude of Driver Differential Output Voltage For Complementary Output States	(Figure 1) R = 27Ω			0.2	V
Driver Common Mode Output Voltage				3.0	V
Change in Magnitude of Driver Common Mode Output Voltage For Complementary Output States				0.2	V
Input High Voltage	DI, DE, RE, E	2			V
Input Low Voltage				0.8	
Input Clamp Voltage				-1.5	
Input Low Current				-200	μA
Input High Current				20	μA
Input Current	DO/RI, DO/Ri	V _{CC} = 0V or 5.25V DE = 0V	V _{IN} = 12V V _{IN} = -7V	+1.0 -0.8	mA
Differential Input Threshold Voltage for Receiver	-7V ≤ V _{CM} ≤ +12V	-0.2		+0.2	V
Receiver Input Hysteresis	V _{CM} = 0V		70		mV
Receiver Output High Voltage	I _{OH} = -400 μA	2.7			V
Output Low Voltage	RO I _{OL} = 16 mA (Note 7)			0.5	V
FF-State (High Impedance) Output Current at Receiver	V _{CC} = Max 0.4V < V _O ≤ 2.4V			±20	μA
Receiver Input Resistance	-7V ≤ V _{CM} ≤ +12V	12			kΩ
Supply Current	No Load (Note 7)				
	Driver Outputs Enabled			55	mA
	Driver Outputs Disabled			35	mA

Electrical Characteristics (Notes 2 and 3)

T_A ≤ 70°C, 4.75V < V_{CC} < 5.25V unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Driver Short-Circuit Output Current	V _O = -7V (Note 7)			-250	mA
	V _O = +12V (Note 7)			+250	mA
Receiver Short-Circuit Output Current	V _O = 0V	-15		-85	mA

"Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

All typicals are given for V_{CC} = 5V and T_A = 25°C.

Dissipate linearly at 5.56 mW/°C to 650 mW at 70°C.

Dissipate linearly at 6.11 mW/°C to 400 mW at 70°C.

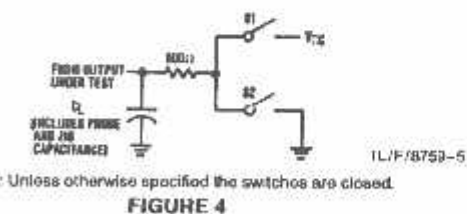
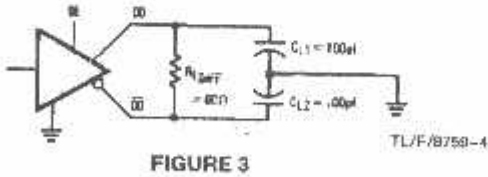
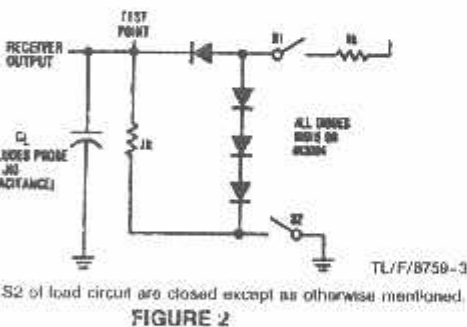
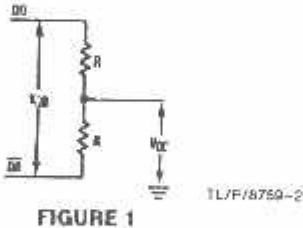
Differential - Input/Output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

7: All worst case parameters for which note 7 is applied, must be increased by 10% for DS75178ET. The other parameters remain valid for -40°C < T_A < +85°C.

Timing Characteristics V_{CC} = 5.0V, T_A = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Driver Input to Output	R _{LDIFF} = 60Ω C _{L1} = C _{L2} = 100 pF		12	22	ns
Driver Input to Output			17	22	ns
Driver Rise Time	R _{LDIFF} = 60Ω C _{L1} = C _{L2} = 100 pF (Figures 3 and 5)			18	ns
Driver Fall Time				18	ns
Driver Enable to Output High	C _L = 100 pF (Figures 4 and 6) S1 Open		29	100	ns
Driver Enable to Output Low	C _L = 100 pF (Figures 4 and 6) S2 Open		31	60	ns
Driver Disable Time from Low	C _L = 15 pF (Figures 4 and 6) S2 Open		13	30	ns
Driver Disable Time from High	C _L = 15 pF (Figures 4 and 6) S1 Open		19	200	ns
Receiver Input to Output	C _L = 15 pF (Figures 2 and 7) S1 and S2 Closed		30	37	ns
Receiver Input to Output			32	37	ns
Receiver Enable to Output Low	C _L = 15 pF (Figures 2 and 8) S2 Open		15	20	ns
Receiver Enable to Output High	C _L = 15 pF (Figures 2 and 8) S1 Open		11	20	ns
Receiver Disable from Low	C _L = 15 pF (Figures 2 and 8) S2 Open		28	32	ns
Receiver Disable from High	C _L = 15 pF (Figures 2 and 8) S1 Open		13	35	ns

Test Circuits



Timing Time Waveforms (Continued)

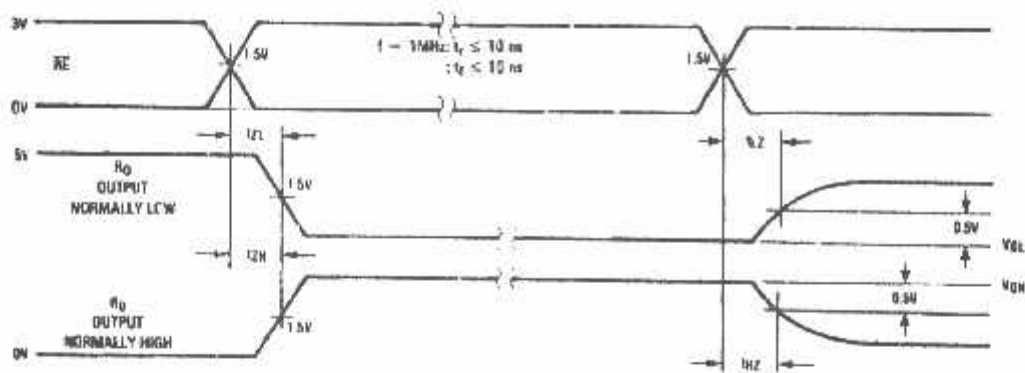


FIGURE 8. Receiver Enable and Disable Times

TL/F/8759-9

Function Tables

DS75176B Transmitting					
Inputs			Line Condition	Outputs	
RE	DE	DI		DO	DO
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

DS75176B Receiving			
Inputs			Outputs
RE	DE	RI-RI	
0	0	$\geq +0.2V$	1
0	0	$\leq -0.2V$	0
0	0	Inputs Open**	1
1	0	X	Z

*Not care condition

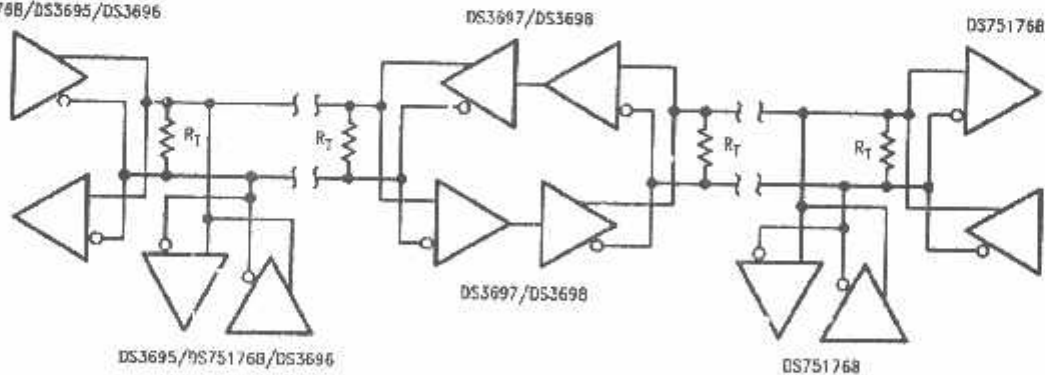
**High impedance state

Improper line conditions causing excessive power dissipation in the driver, such as shorts or bus contention situations

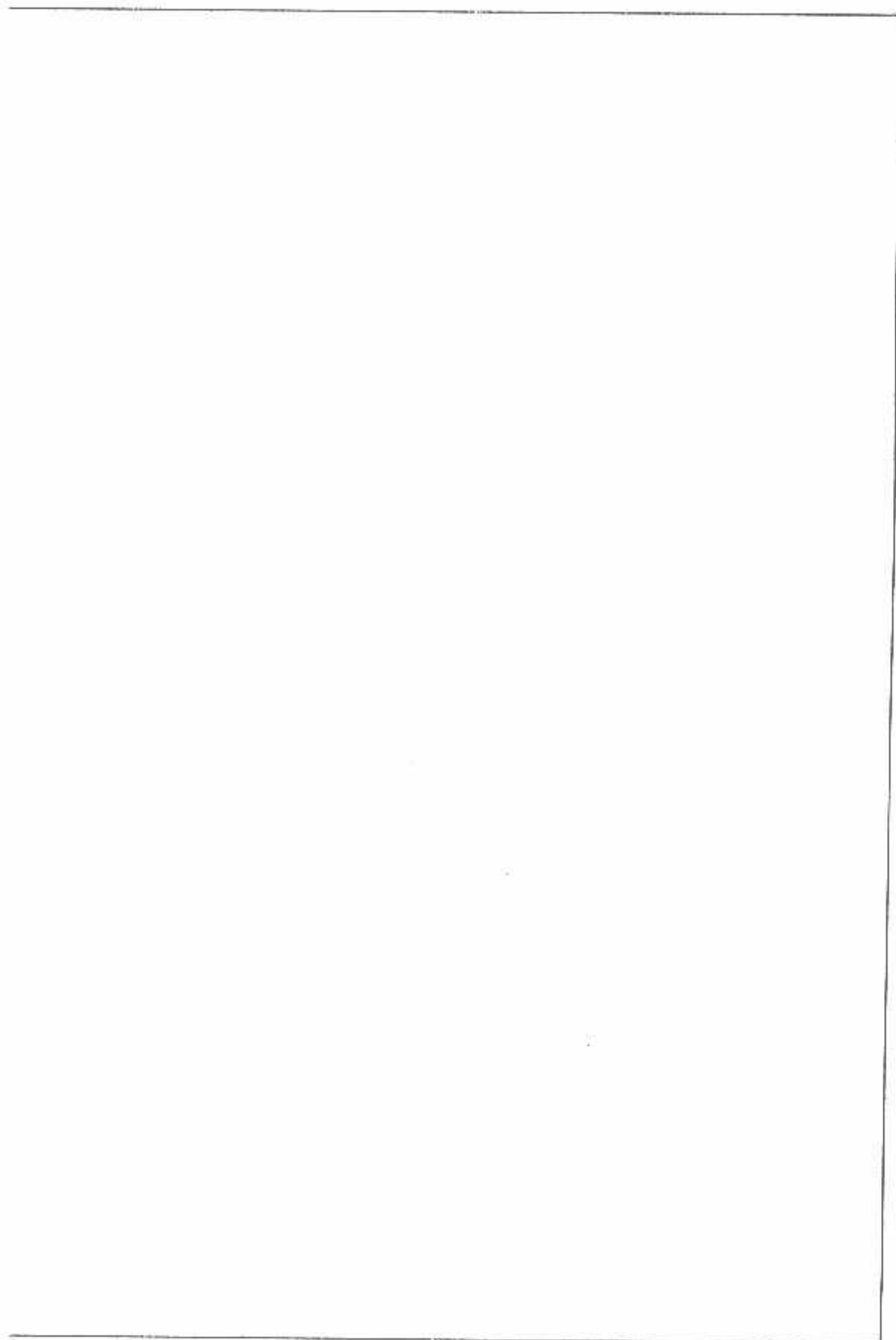
***A fail safe condition

Typical Application

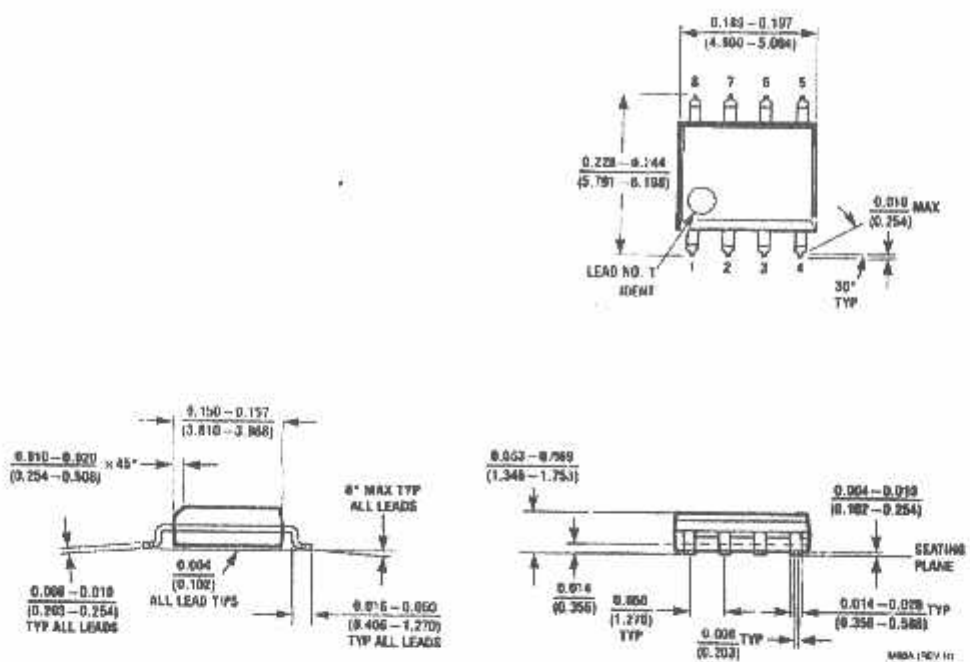
DS75176B/DS3695/DS3696



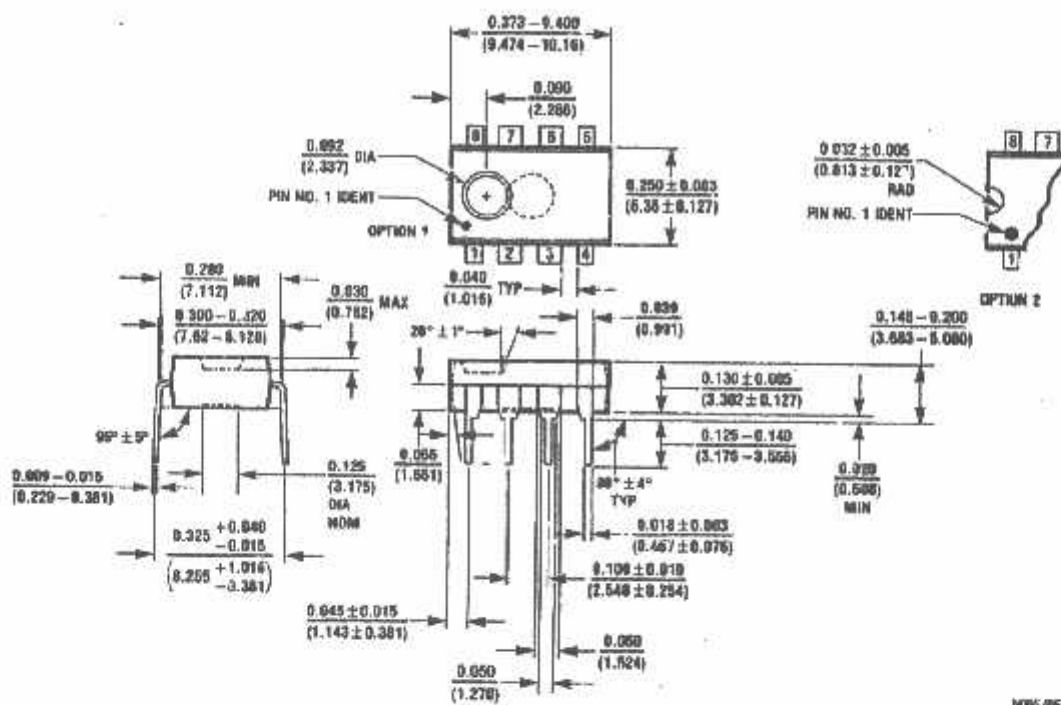
TL/F/8759-11



ical Dimensions inches (millimeters)



Small Outline Package (M)
Order Number DS75176BM or DS75176BTM
NS Package Number M08A



Molded Dual-In-Line Package (N)
Order Number DS75176BN or DS75176BTN
NS Package Number N08E

IFE SUPPORT POLICY

ATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT
VICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL
MICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation 1111 West Bardin Road Arlington, TX 76017 Tel: 1 (800) 272-8959 Fax: 1 (800) 773-7018 //www.national.com	National Semiconductor Europe Fax: +49 (0) 180-530 85 88 Email: europa.support@nsm.com Tel: +49 (0) 180-530 85 85 Dutch: Tel: +49 (0) 180-532 78 32 English: Tel: +49 (0) 180-532 93 58 Française: Tel: +49 (0) 180-534 16 80 Italiano:	National Semiconductor Hong Kong Ltd. 19th Floor, Straight Block, Ocean Centre, 6 Canton Rd., Kowloon, Hong Kong Tel: (852) 2737-6600 Fax: (852) 2735-8660	National Semiconductor Japan Ltd. Tel: 81-4-43-299-2306 Fax: 81-4-43-299-2409
---	---	--	--

MAXIM

±15kV ESD-Protected, +5V RS-232 Transceivers

General Description

The MAX202E-MAX213E, MAX232E/MAX241E line drivers/receivers are designed for RS-232 and V.28 communications in harsh environments. Each transmitter output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. The various combinations of features are outlined in the *Selection Guide*. The drivers and receivers for all ten devices meet all EIA/TIA-232C and CCITT V.28 specifications at data rates up to 120kbps, when loaded in accordance with the EIA/TIA-232C specification.

The MAX211E/MAX213E/MAX241E are available in 28-pin SO packages, as well as a 28-pin SSOP that uses 60% less board space. The MAX202E/MAX232E come in 16-pin narrow SO, wide SO, and DIP packages. The MAX203E comes in a 20-pin DIP/SO package, and needs no external charge-pump capacitors. The MAX205E comes in a 24-pin wide DIP package, and also eliminates external charge-pump capacitors. The MAX206E/MAX207E/MAX208E come in 24-pin SO, SSOP, and narrow DIP packages. The MAX232E/MAX241E operate with four 1µF capacitors, while the MAX202E/MAX206E/MAX207E/MAX208E/MAX211E/MAX213E operate with four 0.1µF capacitors, further reducing cost and board space.

Applications

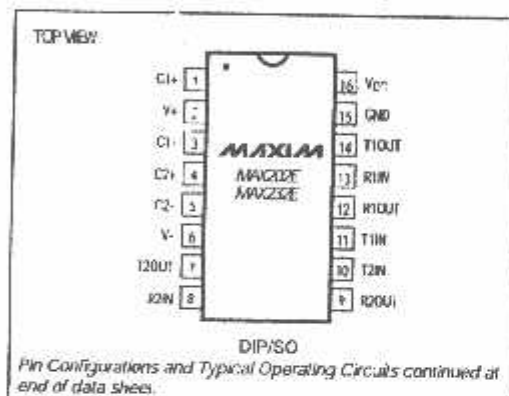
Notebook, Subnotebook, and Palmtop Computers
Battery-Powered Equipment
Hand-Held Equipment

Ordering information appears at end of data sheet.

Features

- ESD Protection for RS-232 I/O Pins:
±15kV—Human Body Model
±8kV—IEC1000-4-2, Contact Discharge
±15kV—IEC1000-4-2, Air-Gap Discharge
- Latchup Free (unlike bipolar equivalents)
- Guaranteed 120kbps Data Rate—LapLink™ Compatible
- Guaranteed 3V/µs Min Stew Rate
- Operate from a Single +5V Power Supply

Pin Configurations



Selection Guide

PART	No. of RS-232 DRIVERS	No. of RS-232 RECEIVERS	RECEIVERS ACTIVE IN SHUTDOWN	No. of EXTERNAL CAPACITORS	LOW-POWER SHUTDOWN	TTL THREE-STATE
MAX202E	2	2	0	4 (0.1µF)	No	No
MAX203E	2	2	0	None	No	No
MAX205E	5	5	0	None	Yes	Yes
MAX206E	4	3	0	4 (0.1µF)	Yes	Yes
MAX207E	5	3	0	4 (0.1µF)	No	No
MAX208E	4	4	0	4 (0.1µF)	No	No
MAX211E	4	5	0	4 (0.1µF)	Yes	Yes
MAX213E	4	5	2	4 (0.1µF)	Yes	Yes
MAX232E	2	2	0	4 (1µF)	No	No
MAX241E	4	5	0	4 (1µF)	Yes	Yes

LapLink is a registered trademark of Traveling Software, Inc.

MAXIM

Maxim Integrated Products 1

For free samples & the latest literature: <http://www.maxim-integrated.com>, or phone 1-800-998-8800

MAX202E-MAX213E, MAX232E/MAX241E

±15kV ESD-Protected, +5V RS-232 Transceivers

ABSOLUTE MAXIMUM RATINGS

V _{CC}	-0.3V to +6V
V ₊	(V _{CC} - 0.3V) to +14V
V ₋	-14V to -0.3V
Input Voltages	
T _{IN}	-0.3V to (V ₊ + 0.3V)
R _{IN}	±30Ω
Output Voltages	
T _{OUT}	(V ₋ - 0.3V) to (V ₊ + 0.3V)
R _{OUT}	-0.3V to (V _{CC} + 0.3V)
Short-Circuit Duration, T _{OUT}	
Continuous Power Dissipation (T _A = +70°C)	Continuous
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)	.842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C)	.696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C)	.762mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C)	.889mW

20-Pin SO (derate 10.00mW/°C above +70°C)	.800mW
24-Pin Narrow Plastic DIP (derate 13.33mW/°C above +70°C)	1.07W
24-Pin Wide Plastic DIP (derate 14.29mW/°C above +70°C)	1.14W
24-Pin SO (derate 11.76mW/°C above +70°C)	.941mW
24-Pin SSOP (derate 8.00mW/°C above +70°C)	.640mW
28-Pin SO (derate 12.50mW/°C above +70°C)	.1W
28-Pin SSOP (derate 9.52mW/°C above +70°C)	.762mW
Operating Temperature Ranges	
MAX2 _{EC}	0°C to +70°C
MAX2 _{EE}	-40°C to +85°C
Storage Temperature Range	
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = -5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; V_{CC} = +5V ±5% for MAX205E/206E/207E; C1-C4 = 0.1μF for MAX202E/206E/207E/208E/211E/213E; C1-C4 = 1μF for MAX232E/241E; T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
V _{CC} Supply Current	I _{CC}	No load, T _A = +25°C	MAX202E/203E		8	15	mA
			MAX205E-208E		11	20	
			MAX211E/213E		14	20	
			MAX232E		5	10	
			MAX241E		7	15	
Shutdown Supply Current		I _A = -25°C, Figure 1	MAX205E/206E		1	10	μA
			MAX211E/241E		1	10	
			MAX213E		15	50	
LOGIC							
Input Pull-Up Current		T _{IN} = 0V (MAX205E-208E/211E/213E/241E)		15	200		μA
Input Leakage Current		T _{IN} = 0V to V _{CC} (MAX202E/203E/232E)			±10		μA
Input Threshold Low	V _{IL}	T _{IN} , EN, SHDN (MAX213E) or EN, SHDN (MAX205E-208E/211E/241E)			0.8		V
Input Threshold High	V _{IH}	T _{IN}		2.0			V
		EN, SHDN (MAX213E) or EN, SHDN (MAX205E-208E/211E/241E)		2.4			
Output Voltage Low	V _{OL}	R _{OUT} ; I _{OUT} = 3.2mA (MAX202E/203E/232E) or I _{OUT} = 1.6mA (MAX205E/208E/211E/213E/241E)			0.4		V
Output Voltage High	V _{OH}	R _{OUT} ; I _{OUT} = -1.0mA		3.5 V _{CC} - 0.4			V
Output Leakage Current		EN = V _{CC} , EN = 0V, 0V ≤ R _{OUT} ≤ V _{CC} , MAX205E-208E/211E/213E/241E outputs disabled		±0.05	±10		μA

±15kV ESD-Protected, +5V RS-232 Transceivers

ELECTRICAL CHARACTERISTICS (continued)

(VCC = +5V ±10% for MAX202E/206E/208E/211E/213E/232E/241E; VCC = +5V ±5% for MAX203E/205E/207E; C1-C4 = 0.1µF for MAX202E/206E/207E/208E/211E/213E; C1-C4 = 1µF for MAX232E/241E; TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

MAX202E-MAX213E, MAX232E/MAX241E

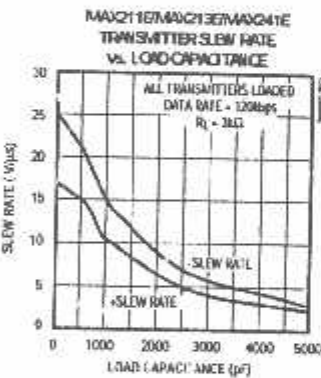
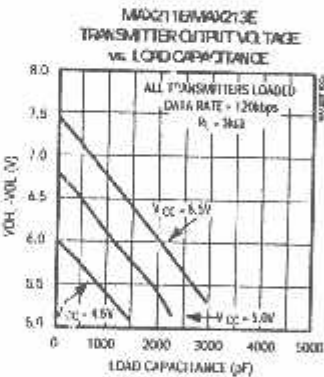
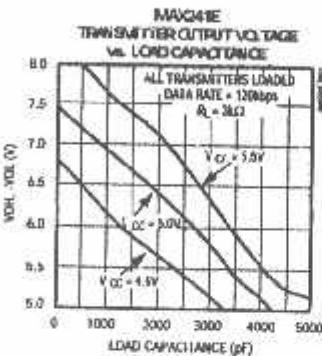
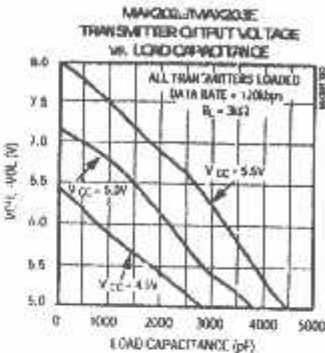
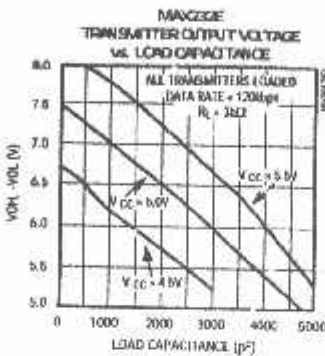
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EIA/TIA-232E RECEIVER INPUTS						
Input Voltage Range			-30		30	V
Input Threshold Low		TA = -25°C, VCC = 5V	All parts, normal operation	0.8	1.2	V
			MAX213E: SHDN = 0V, EN = VCC	0.6	1.5	
Input Threshold High		TA = +25°C, VCC = 5V	All parts, normal operation	1.7	2.4	V
			MAX213E (R4, R5), SDN = 0V, EN = VCC	1.5	2.4	
Input Hysteresis		VCC = 5V, no hysteresis in shutdown	0.2	0.5	1.0	V
Input Resistance		TA = +25°C, VCC = 5V	3	5	7	kΩ
EIA/TIA-232E TRANSMITTER OUTPUTS						
Output Voltage Swing		All drivers loaded with 3kΩ to ground (Note 1)	±5	±9		V
Output Resistance		VCC = V+ = V- = 0V, VOUT = ±2V	300			Ω
Output Short-Circuit Current				±10	±60	mA
TIMING CHARACTERISTICS						
Maximum Data Rate		RL = 3kΩ to 7kΩ, CL = 50pf to 1000pf, one transmitter switching	120			Mbps
Receiver Propagation Delay	tPHLW, tPHLW	CL = 150pf	All parts, normal operation	0.5	10	µs
			MAX213E (R4, R5), SDN = 0V, EN = VCC	4	40	
Receiver Output Enable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2		600		ns
Receiver Output Disable Time		MAX205E/206E/211E/213E/241E normal operation, Figure 2		200		ns
Transmitter Propagation Delay	tPLHT, tPHLT	RL = 3kΩ, CL = 2500pf, all transmitters loaded		2		µs
Transition-Region Slew Rate		TA = +25°C, VCC = 5V, RL = 3kΩ to 7kΩ, CL = 50pf to 1000pF, measured from -3V to +3V or +3V to -3V, Figure 3	3	6	30	V/µs
ESD PERFORMANCE: TRANSMITTER OUTPUTS, RECEIVER INPUTS						
ESD Protection Voltage		Human Body Model		±15		kV
		IEC1000-4-2, Contact Discharge		±8		
		IEC1000-4-2, Air-Gap Discharge		±15		

Note 1: MAX211EE_ tested with VCC = +5V ±5%.

±15kV ESD-Protected, +5V RS-232 Transceivers

Typical Operating Characteristics

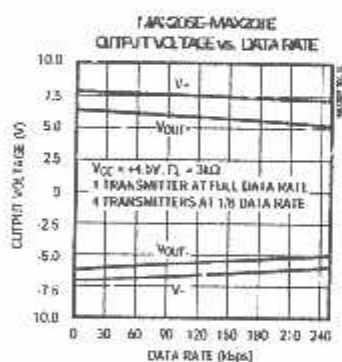
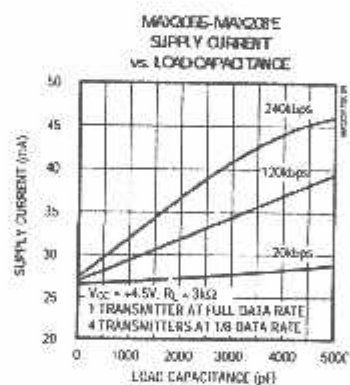
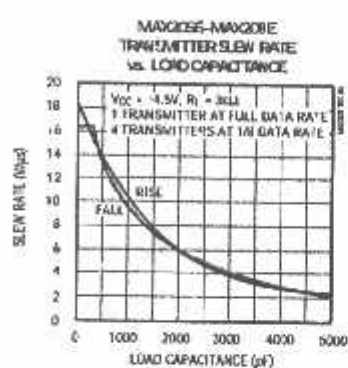
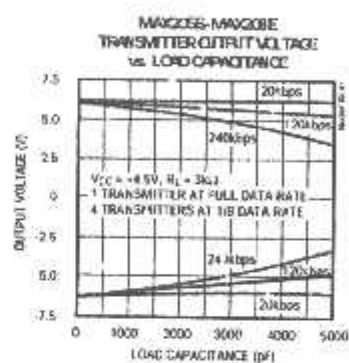
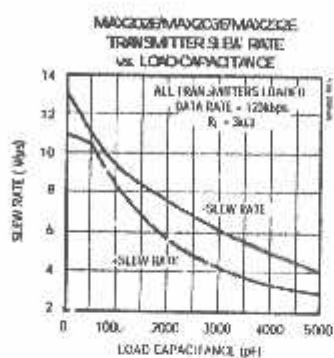
(Typical Operating Circuits, V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)



$\pm 15\text{kV}$ ESD-Protected, $+5\text{V}$ RS-232 Transceivers

Typical Operating Characteristics (continued)

(Typical Operating Circuits, $V_{CC} = +5\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



MAX202E-MAX213E, MAX232E/MAX241E

±15kV ESD-Protected, +5V RS-232 Transceivers

Pin Descriptions

MAX202E/MAX232E

PIN		NAME	FUNCTION
DIP/SO	LCC		
1, 3	2, 4	C1+, C1-	Terminals for positive charge-pump capacitor
2	3	V+	-2V _{CC} voltage generated by the charge pump
4, 5	5, 7	C2+, C2-	Terminals for negative charge-pump capacitor
6	8	V-	-2V _{CC} voltage generated by the charge pump
7, 14	9, 13	T_OUT	RS-232 Driver Outputs
8, 13	10, 17	R_IN	RS-232 Receiver Outputs
9, 12	12, 15	R_OUT	RS-232 Receiver Outputs
10, 11	13, 14	T_IN	RS-232 Driver Inputs
15	19	GND	Ground
16	20	V _{CC}	+4.5V to +5.5V Supply-Voltage Input
—	1, 6, 11, 16	N.C.	No Connect—not internally connected.

MAX203E

PIN		NAME	FUNCTION
DIP	SO		
1, 2	1, 2	T_IN	RS-232 Driver Inputs
3, 20	3, 20	R_OUT	RS-232 Receiver Outputs
4, 19	4, 19	R_IN	RS-232 Receiver Inputs
5, 18	5, 18	T_OUT	RS-232 Transmitter Outputs
6, 9	6, 9	GND	Ground
7	7	V _{CC}	+4.5V to +5.5V Supply-Voltage Input
8	13	C1+	Make no connection to this pin.
10, 16	11, 16	C2-	Connect pins together.
12, 17	10, 17	V	-2V _{CC} voltage generated by the charge pump. Connect pins together.
13	14	C1-	Make no connection to this pin.
14	8	V-	+2V _{CC} voltage generated by the charge pump
11, 15	12, 15	C2+	Connect pins together.

MAX205E

PIN	NAME	FUNCTION
1-4, 19	T_OUT	RS-232 Driver Outputs
5, 10, 13, 18, 24	R_IN	RS-232 Receiver Inputs
6, 9, 14, 17, 23	R_OUT	TTLCMOS Receiver Outputs. All receivers are inactive in shutdown.
7, 8, 15, 16, 22	T_IN	TTLCMOS Driver Inputs. Internal pull-ups to V _{CC} .
11	GND	Ground
12	V _{CC}	+4.75V to +5.25V Supply Voltage
20	EN	Receiver Enable—active low
21	SHDN	Shutdown Control—active high

±15kV ESD-Protected, +5V RS-232 Transceivers

Pin Descriptions (continued)

MAX206E

PIN	NAME	FUNCTION
1, 2, 3, 24	T_OUT	RS-232 Driver Outputs
4, 16, 23	R_IN	RS-232 Receiver Inputs
5, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
6, 7, 18, 19	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V _{CC} .
8	GND	Ground
9	V _{CC}	+4.5V to +5.5V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	+2V _{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V-	-2V _{CC} generated by the charge pump
20	EN	Receiver Enable—active low
21	SHDN	Shutdown Control—active high

MAX207E

PIN	NAME	FUNCTION
1, 2, 3, 20, 24	T_OUT	RS-232 Driver Outputs
4, 16, 23	R_IN	RS-232 Receiver Inputs
5, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
6, 7, 18, 19, 21	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V _{CC} .
8	GND	Ground
9	V _{CC}	+4.75V to +5.25V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	+2V _{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V-	-2V _{CC} generated by the charge pump

MAX208E

PIN	NAME	FUNCTION
1, 2, 20, 24	T_OUT	RS-232 Driver Outputs
3, 7, 16, 23	R_IN	RS-232 Receiver Inputs
4, 6, 17, 22	R_OUT	TTL/CMOS Receiver Outputs. All receivers are inactive in shutdown.
5, 18, 19, 21	T_IN	TTL/CMOS Driver Inputs. Internal pull-ups to V _{CC} .
8	GND	Ground
9	V _{CC}	+4.5V to +5.5V Supply Voltage
10, 12	C1+, C1-	Terminals for positive charge-pump capacitor
11	V+	+2V _{CC} generated by the charge pump
13, 14	C2+, C2-	Terminals for negative charge-pump capacitor
15	V-	-2V _{CC} generated by the charge pump

MAX202E-MAX213E, MAX232E/MAX241E

±15kV ESD-Protected, +5V RS-232 Transceivers

Pin Descriptions (continued)

MAX211E/MAX213E/MAX241E

PIN	NAME	FUNCTION
1, 2, 3, 28	Y_OUT	RS-232 Driver Outputs
4, 9, 18, 23, 27	R_IN	RS-232 Receiver Inputs
5, 8, 19, 22, 26	R_OUT	TL/CMOS Receiver Outputs. For the MAX213E, receivers R4 and R5 are active in shutdown mode when EN = 1. For the MAX211E and MAX241E, all receivers are inactive in shutdown.
6, 7, 20, 21	T_IN	TL/CMOS Driver Inputs. Only the MAX211E, MAX213E, and MAX241E have internal pull-ups to V _{CC} .
10	GND	Ground
11	V _{CC}	+4.5V to +5.5V Supply Voltage
12, 14	C1+, C1-	Terminals for positive charge-pump capacitor
13	V+	+2V _{CC} voltage generated by the charge pump
15, 16	C2+, C2-	Terminals for negative charge-pump capacitor
17	V-	-2V _{CC} voltage generated by the charge pump
24	EN	Receiver Enable—active low (MAX211E, MAX241E)
	EN	Receiver Enable—active high (MAX213E)
25	SHDN	Shutdown Control—active high (MAX211E, MAX241E)
	SHDN	Shutdown Control—active low (MAX213E)

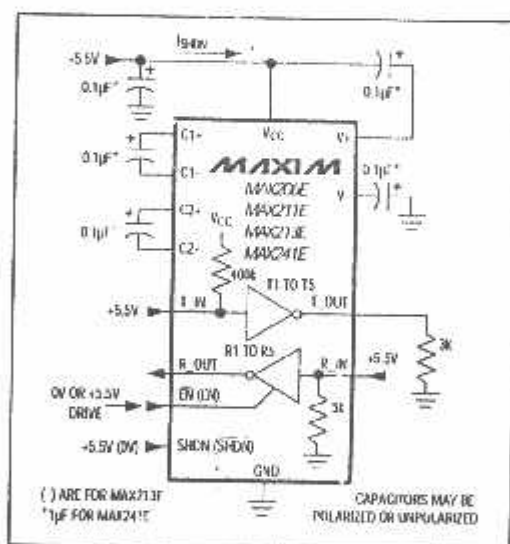


Figure 1. Shutdown-Current Test Circuit (MAX206E, MAX211E/MAX213E/MAX247E)

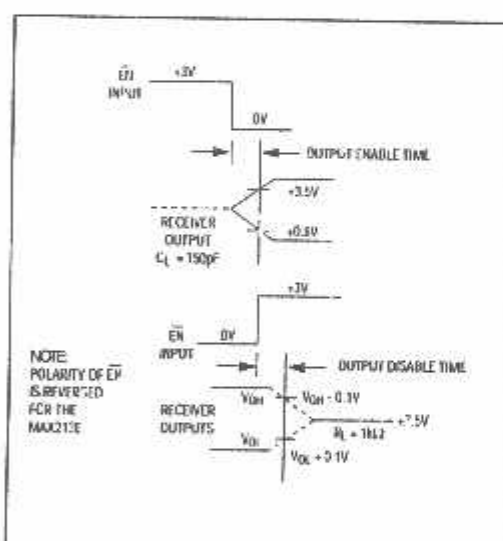


Figure 2. Receiver Output Enable and Disable Timing (MAX275E/MAX276E/MAX277E/MAX278E/MAX279E)

±15kV ESD-Protected, +5V RS-232 Transceivers

MAX202E-MAX213E, MAX232E/MAX241E

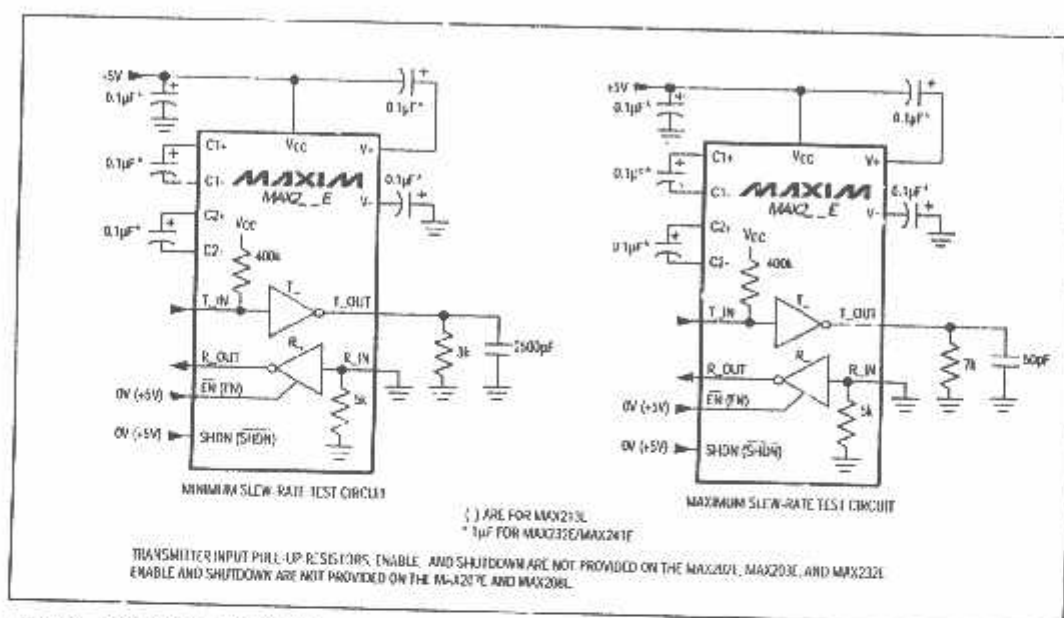


Figure 3. Transition Slow-Rate Circuit

Detailed Description

The MAX202E-MAX213E, MAX232E/MAX241E consist of three sections: charge-pump voltage converters, drivers (transmitters), and receivers. These E versions provide extra protection against ESD. They survive ±15kV discharges to the RS-232 inputs and outputs, tested using the Human Body Model. When tested according to IEC1000-4-2, they survive ±8kV contact discharges and ±15kV air-gap discharges. The rugged E versions are intended for use in harsh environments or applications where the RS-232 connection is frequently changed (such as notebook computers). The standard (non-"E") MAX202, MAX203, MAX205-MAX208, MAX211, MAX213, MAX232, and MAX241 are recommended for applications where cost is critical.

+5V to ±10V Dual Charge-Pump Voltage Converter

The +5V to ±10V conversion is performed by dual charge-pump voltage converters (Figure 4). The first charge-pump converter uses capacitor C1 to double the +5V into +10V, storing the +10V on the output filter capacitor, C3. The second uses C2 to invert the +10V

into -10V, storing the -10V on the V- output filter capacitor, C4.

In shutdown mode, V+ is internally connected to VCC by a 1kΩ pull-down resistor, and V- is internally connected to ground by a 1kΩ pull-up resistor.

RS-232 Drivers

With VCC = 5V, the typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver. The output swing is guaranteed to meet EIA/TIA-232E and V.28 specifications that call for ±5V minimum output levels under worst-case conditions. These include a 3kΩ load, minimum VCC, and maximum operating temperature. The open-circuit output voltage swings from (V+ - 0.6V) to V-.

Input thresholds are CMOS/TTL compatible. The unused drivers' inputs on the MAX205E-MAX208E, MAX211E, MAX213E, and MAX241E can be left unconnected because 400kΩ pull-up resistors to VCC are included on-chip. Since all drivers invert, the pull-up resistors force the unused drivers' outputs low. The MAX202E, MAX203E, and MAX232E do not have pull-up resistors on the transmitter inputs.

±15kV ESD-Protected, +5V RS-232 Transceivers

When in low-power shutdown mode, the MAX205E/MAX206E/MAX211E/MAX213E/MAX241E driver outputs are turned off and draw only leakage currents—even if they are back-driven with voltages between 0V and 12V. Below -0.5V in shutdown, the transmitter output is diode-clamped to ground with a 1kΩ series impedance.

RS-232 Receivers

The receivers convert the RS-232 signals to CMOS-logic output levels. The guaranteed 0.8V and 2.4V receiver input thresholds are significantly tighter than the ±3V thresholds required by the EIA/TIA-232E specification. This allows the receiver inputs to respond to TTL/CMOS-logic levels, as well as RS-232 levels.

The guaranteed 0.8V input low threshold ensures that receivers shorted to ground have a logic 1 output. The 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

Receiver inputs have approximately 0.5V hysteresis. This provides clean output transitions, even with slow rise/fall-time signals with moderate amounts of noise and ringing.

In shutdown, the MAX213E's R4 and R5 receivers have no hysteresis.

Shutdown and Enable Control (MAX205E/MAX206E/MAX211E/ MAX213E/MAX241E)

In shutdown mode, the charge pumps are turned off, V+ is pulled down to VCC, V- is pulled to ground, and the transmitter outputs are disabled. This reduces supply current typically to 1μA (15μA for the MAX213E). The time required to exit shutdown is under 1ms, as shown in Figure 5.

Receivers

All MAX213E receivers, except R4 and R5, are put into a high-impedance state in shutdown mode (see Tables 1a and 1b). The MAX213E's R4 and R5 receivers still function in shutdown mode. These two awake-in-shutdown receivers can monitor external activity while maintaining minimal power consumption.

The enable control is used to put the receiver outputs into a high-impedance state, to allow wire-OR connection of two EIA/TIA-232E ports (or ports of different types) at the UART. It has no effect on the RS-232 drivers or the charge pumps.

Note: The enable control pin is active low for the MAX211E/MAX241E (EN), but is active high for the MAX213E (EN). The shutdown control pin is active high for the MAX205E/MAX206E/MAX211E/MAX241E (SHDN), but is active low for the MAX213E (SHDN).

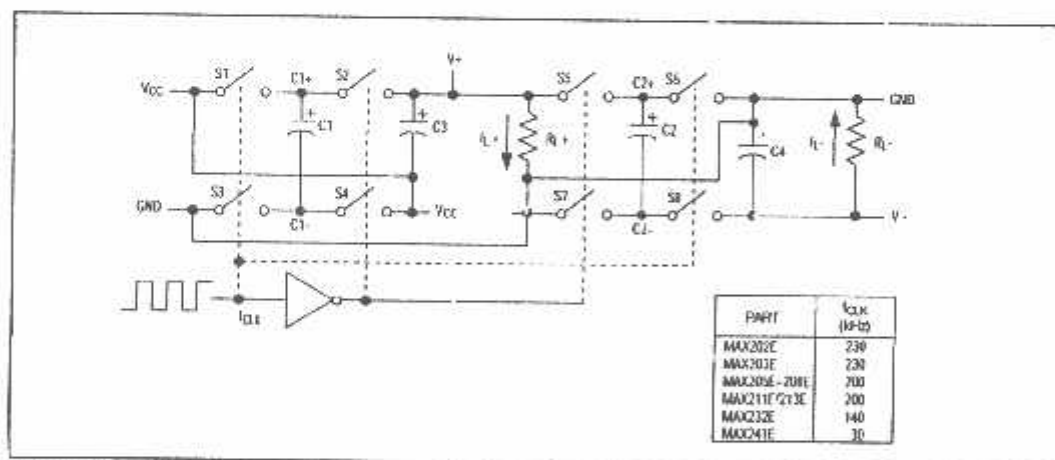


Figure 4. Charge-Pump Diagram

±15kV ESD-Protected, +5V RS-232 Transceivers

The MAX213E's receiver propagation delay is typically 0.5µs in normal operation. In shutdown mode, propagation delay increases to 4µs for both rising and falling transitions. The MAX213E's receiver inputs have approximately 0.5V hysteresis, except in shutdown, when receivers R4 and R5 have no hysteresis.

When entering shutdown with receivers active, R4 and R5 are not valid until 80µs after SHDN[†] is driven low. When coming out of shutdown, all receiver outputs are invalid until the charge pumps reach nominal voltage levels (less than 2ms when using 0.1µF capacitors).

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's E versions keep working without latchup, whereas competing RS-232 products can latch and must be powered down to remove latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to the following limits:

- 1) ±15kV using the Human Body Model
- 2) ±8kV using the contact-discharge method specified in IEC1000-4-2
- 3) ±15kV using IEC1000-4-2's air-gap method.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 6a shows the Human Body Model, and Figure 6b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

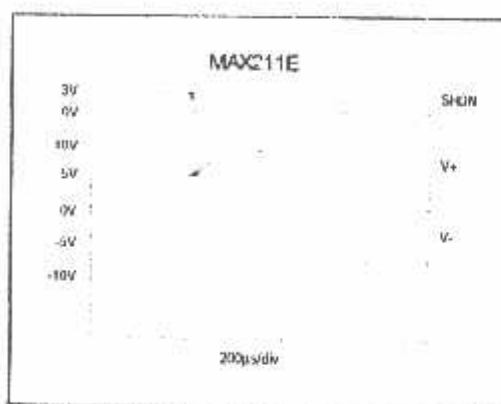


Figure 5. MAX211E V+ and V- when Exiting Shutdown (0.1µF capacitors)

Table 1a. MAX205E/MAX206E/MAX211E/MAX241E Control Pin Configurations

SHDN	EN	OPERATION STATUS	Tx	Rx
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All High-Z
1	X	Shutdown	All High-Z	All High-Z

X = Don't Care

Table 1b. MAX213E Control Pin Configurations

SHDN	EN	OPERATION STATUS	Tx 1-4	Rx	
				1-3	4, 5
0	0	Shutdown	All High-Z	High-Z	High-Z
0	1	Shutdown	All High-Z	High-Z	Active [†]
1	0	Normal Operation	All Active	High-Z	High-Z
1	1	Normal Operation	All Active	Active	Active

[†]Active = active with reduced performance

MAX202E-MAX213E, MAX232E/MAX241E

±15kV ESD-Protected, +5V RS-232 Transceivers

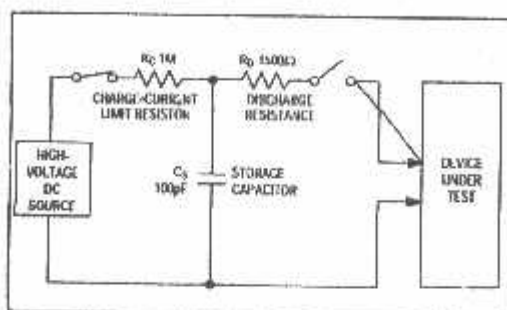


Figure 6a. Human Body ESD Test Model

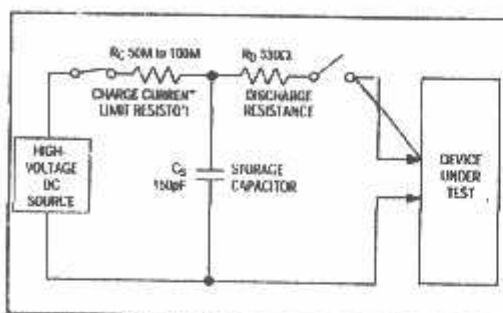


Figure 7a. IEC1000-4-2 ESD Test Model

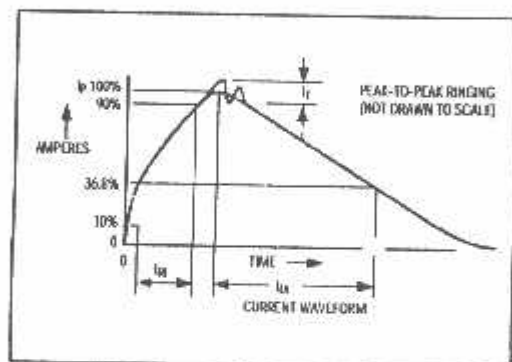


Figure 6b. Human Body Model Current Waveform

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The MAX202E/MAX203E-MAX213E, MAX232E/MAX241E help you design equipment that meets level 4 (the highest level) of IEC1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2, because series resistance is lower in the IEC1000-4-2 model. Hence, the ESD withstand voltage measured to IEC1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7b shows the current waveform for the 8kV IEC1000-4-2 level-four ESD contact-discharge test.

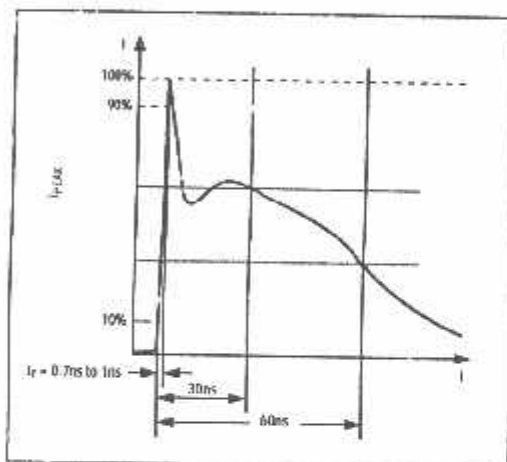


Figure 7b. IEC1000-4-2 ESD Generator Current Waveform

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just RS-232 inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

±15kV ESD-Protected, +5V RS-232 Transceivers

Applications Information

Capacitor Selection

The capacitor type used for C1-C4 is not critical for proper operation. The MAX202E, MAX206-MAX208E, MAX211E, and MAX213E require 0.1µF capacitors, and the MAX232E and MAX241E require 1µF capacitors, although in all cases capacitors up to 10µF can be used without harm. Ceramic, aluminum-electrolytic, or tantalum capacitors are suggested for the 1µF capacitors, and ceramic dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2x) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Use larger capacitors (up to 10µF) to reduce the output impedance at V+ and V-. This can be useful when "stealing" power from V+ or from V-. The MAX203E and MAX205E have internal charge-pump capacitors.

Bypass VCC to ground with at least 0.1µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple VCC to ground with a

capacitor the same size as (or larger than) the charge-pump capacitors (C1-C4).

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce both driver output swing and noise margins. Increasing the value of the charge-pump capacitors (up to 10µF) helps maintain performance when power is drawn from V+ or V-.

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple receivers.

Driver Outputs when Exiting Shutdown

The driver outputs display no ringing or undesirable transients as they come out of shutdown.

High Data Rates

These transceivers maintain the RS-232 ±5.0V minimum driver output voltages at data rates of over 120kbps. For data rates above 120kbps, refer to the Transmitter Output Voltage vs. Load Capacitance graphs in the *Typical Operating Characteristics*. Communication at these high rates is easier if the capacitive loads on the transmitters are small; i.e., short cables are best.

Table 2. Summary of EIA/TIA-232E, V.28 Specifications

PARAMETER		CONDITIONS	EIA/TIA-232E, V.28 SPECIFICATIONS
Driver Output Voltage	0 Level	3kΩ to 7kΩ load	+5V to +15V
	1 Level	3kΩ to 7kΩ load	-5V to -15V
Driver Output Level, Max		No load	±25V
Data Rate		3kΩ ≤ R _L ≤ 7kΩ, C _L ≤ 2500pF	Up to 20kbps
Receiver Input Voltage	0 Level		+3V to +15V
	1 Level		-3V to -15V
Receiver Input Level			±25V
Instantaneous Slew Rate, Max		3kΩ ≤ R _L ≤ 7kΩ, C _L ≤ 2500pF	30V/µs
Driver Output Short-Circuit Current, Max			100mA
Transition Rate on Driver Output		V.28	1ms or 3% of the period
		EIA/TIA-232E	4% of the period
Driver Output Resistance		-2V < V _{OUT} < +2V	300Ω

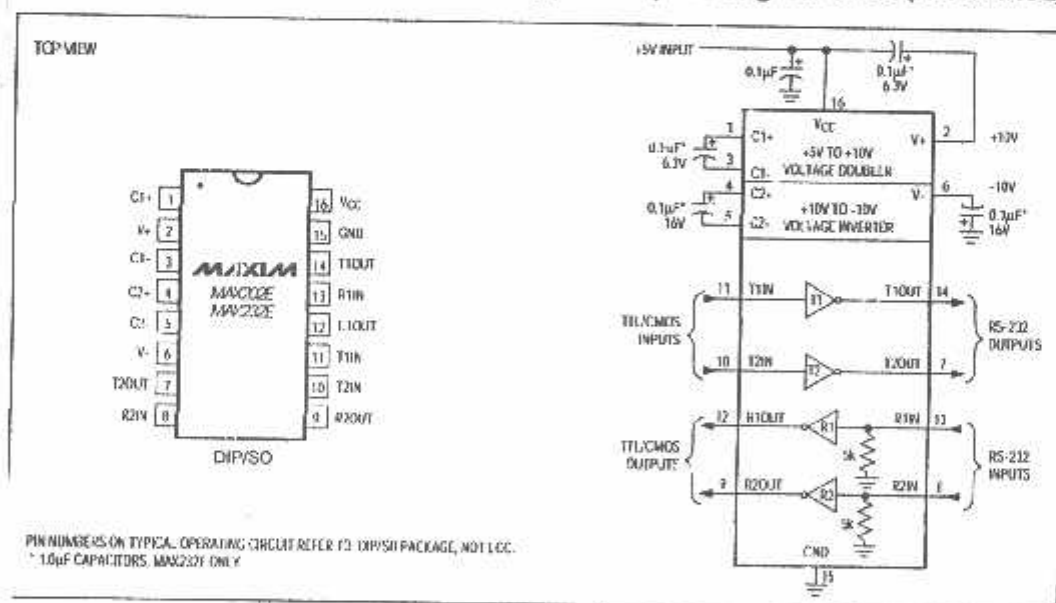
MAX202E-MAX213E, MAX232E/MAX241E

±15kV ESD-Protected, +5V RS-232 Transceivers

Table 3. DB9 Cable Connections
Commonly Used for EIA-232E and
V.24 Asynchronous Interfaces

PIN	CONNECTION	
1	Received Line Signal Detector (sometimes called Carrier Detect, DCD)	Handshake from DCE
2	Receive Data (RD)	Data from DCE
3	Transmit Data (TD)	Data from DTE
4	Data Terminal Ready	Handshake from DTE
5	Signal Ground	Reference point for signals
6	Data Set Ready (DSR)	Handshake from DCE
7	Request to Send (RTS)	Handshake from DTE
8	Clear to Send (CTS)	Handshake from DCE
9	Ring Indicator	Handshake from DCE

Pin Configurations and Typical Operating Circuits (continued)



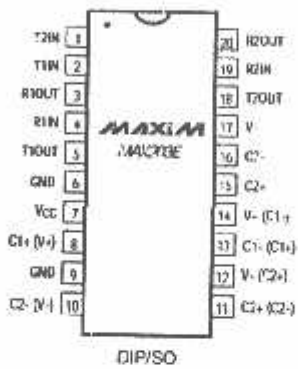
MAXIM

±15kV ESD-Protected, +5V RS-232 Transceivers

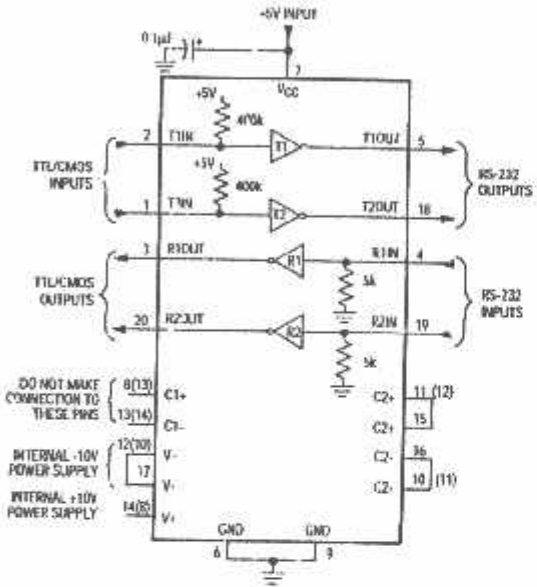
Pin Configurations and Typical Operating Circuits (continued)

MAX202E-MAX213E, MAX232E/MAX241E

TOP VIEW



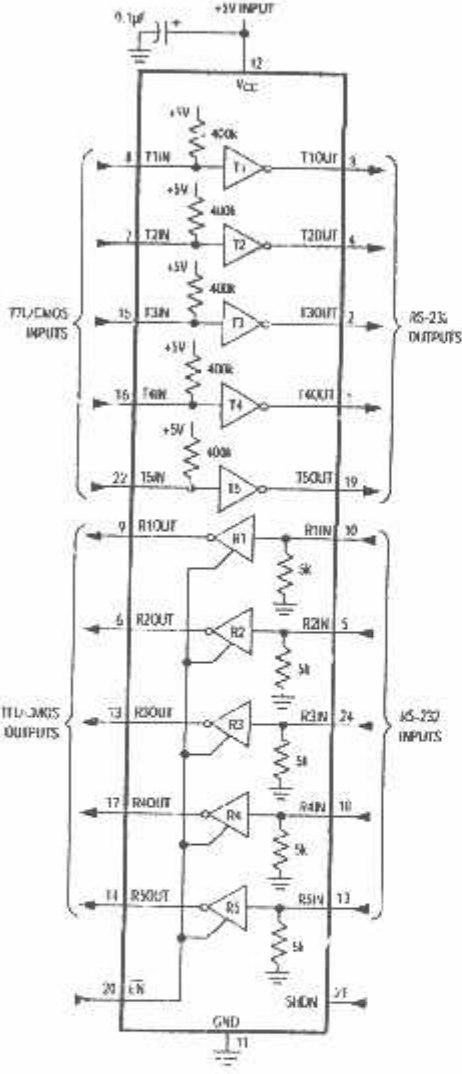
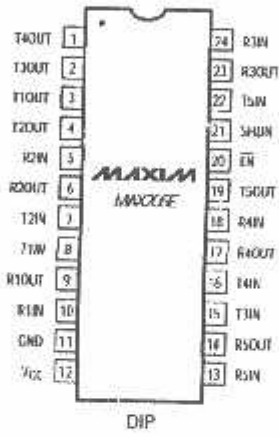
PIN NUMBERS IN () ARE FOR SO PACKAGE.



$\pm 15\text{kV}$ ESD-Protected, $+5\text{V}$ RS-232 Transceivers

Pin Configurations and Typical Operating Circuits (continued)

TC1-VB4

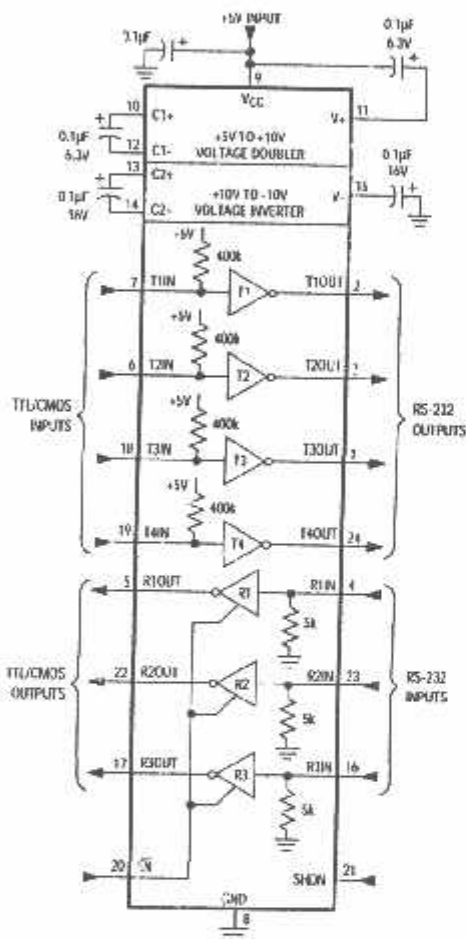
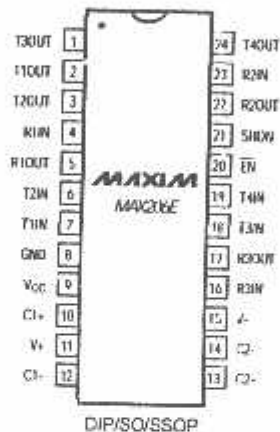


±15kV ESD-Protected, +5V RS-232 Transceivers

Pin Configurations and Typical Operating Circuits (continued)

MAX202E-MAX213E, MAX232E/MAX241E

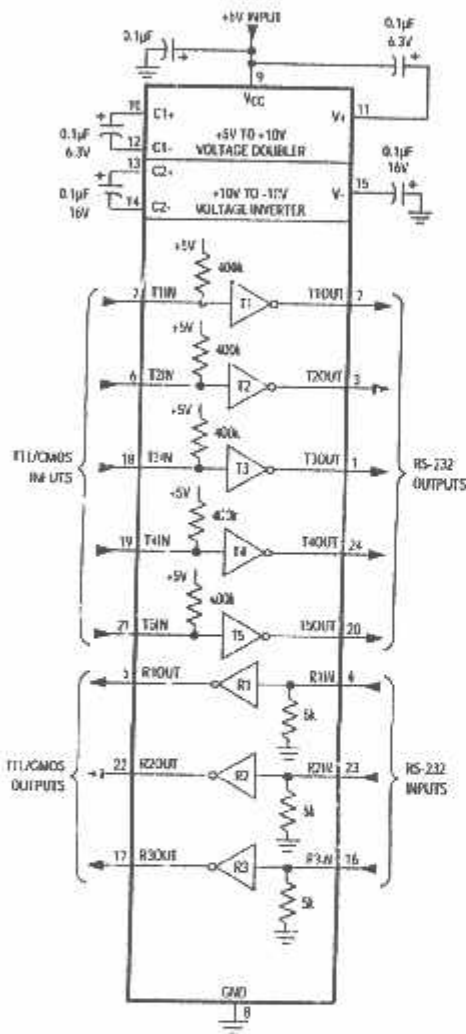
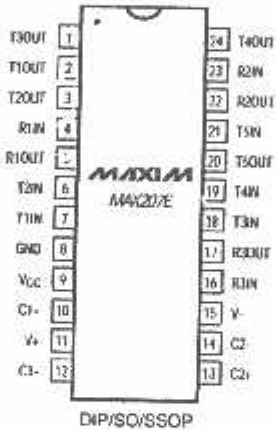
TOP VIEW



±15kV ESD-Protected, +5V RS-232 Transceivers

Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW

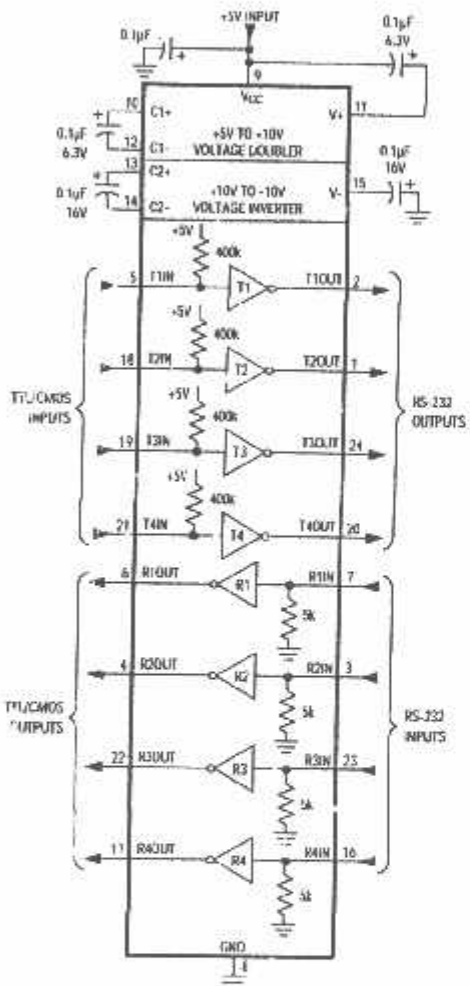
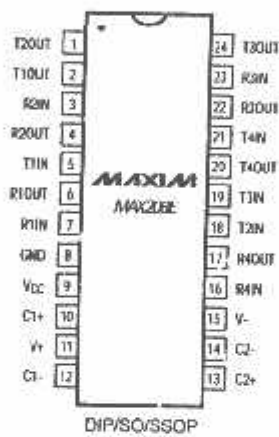


±15kV ESD-Protected, +5V RS-232 Transceivers

Pin Configurations and Typical Operating Circuits (continued)

MAX202E-MAX213E, MAX232E/MAX241E

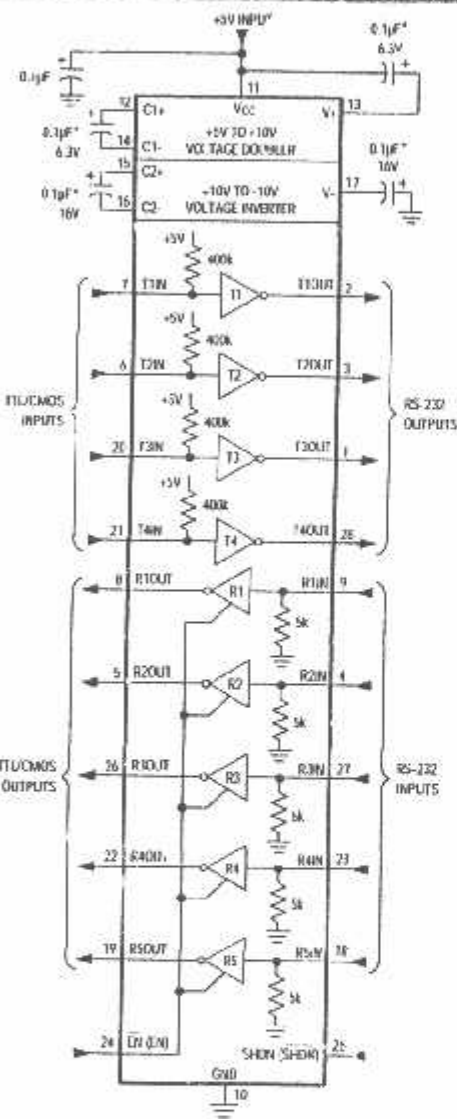
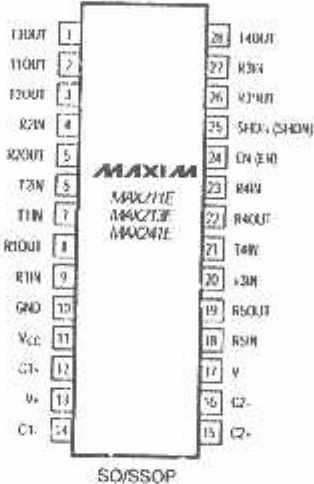
TOP VIEW



$\pm 15\text{kV}$ ESD-Protected, +5V RS-232 Transceivers

Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



(1) .01uF FOR MAX232C ONLY
(2) .01uF CAPACITORS, MAX232C ONLY

±15kV ESD-Protected, +5V RS-232 Transceivers

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX202ECPE	0°C to +70°C	16 Plastic DIP
MAX202ECSE	0°C to +70°C	16 Narrow SO
MAX202ECWE	0°C to +70°C	16 Wide SO
MAX202EC/D	0°C to +70°C	Dice*
MAX202EEPE	-40°C to +85°C	16 Plastic DIP
MAX202EESE	-40°C to +85°C	16 Narrow SO
MAX202EEWE	-40°C to +85°C	16 Wide SO
MAX203ECPP	0°C to +70°C	20 Plastic DIP
MAX203ECV/P	0°C to +70°C	20 SO
MAX203EEPP	-40°C to +85°C	20 Plastic DIP
MAX203EEWP	-40°C to +85°C	20 SO
MAX206ECPG	0°C to +70°C	24 Wide Plastic DIP
MAX206EEPG	-40°C to +85°C	24 Wide Plastic DIP
MAX206ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX206ECWG	0°C to +70°C	24 SO
MAX206ECAG	0°C to +70°C	24 SSOP
MAX206EENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX206EEWG	-40°C to +85°C	24 SO
MAX206EEAG	-40°C to +85°C	24 SSOP
MAX207ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX207ECWG	0°C to +70°C	24 SO
MAX207ECAG	0°C to +70°C	24 SSOP
MAX207EENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX207EEWG	-40°C to +85°C	24 SO
MAX207EEAG	-40°C to +85°C	24 SSOP

PART	TEMP. RANGE	PIN-PACKAGE
MAX208ECNG	0°C to +70°C	24 Narrow Plastic DIP
MAX208ECWG	0°C to +70°C	24 SO
MAX208ECAG	0°C to +70°C	24 SSOP
MAX208EENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX208EEWG	-40°C to +85°C	24 SO
MAX208EEAG	-40°C to +85°C	24 SSOP
MAX211ECWI	0°C to +70°C	28 SO
MAX211ECAI	0°C to +70°C	28 SSOP
MAX211EEWI	-40°C to +85°C	28 SO
MAX211EEAI	-40°C to +85°C	28 SSOP
MAX213ECWI	0°C to +70°C	28 SO
MAX213ECAI	0°C to +70°C	28 SSOP
MAX213EEWI	-40°C to +85°C	28 SO
MAX213EEAI	-40°C to +85°C	28 SSOP
MAX232ECPE	0°C to +70°C	16 Plastic DIP
MAX232ECSE	0°C to +70°C	16 Narrow SO
MAX232ECWE	0°C to +70°C	16 Wide SO
MAX232EC/D	0°C to +70°C	Dice*
MAX232EEPE	-40°C to +85°C	16 Plastic DIP
MAX232EESE	-40°C to +85°C	16 Narrow SO
MAX232EEWE	-40°C to +85°C	16 Wide SO
MAX241ECWI	0°C to +70°C	28 SO
MAX241ECAI	0°C to +70°C	28 SSOP
MAX241EEWI	-40°C to +85°C	28 SO
MAX241EEAI	-40°C to +85°C	28 SSOP

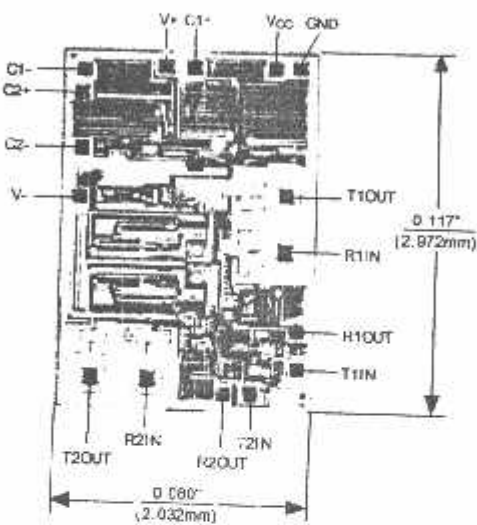
*Dice are specified at T_A = +25°C.

MAX202E-MAX213E, MAX232E/MAX241E

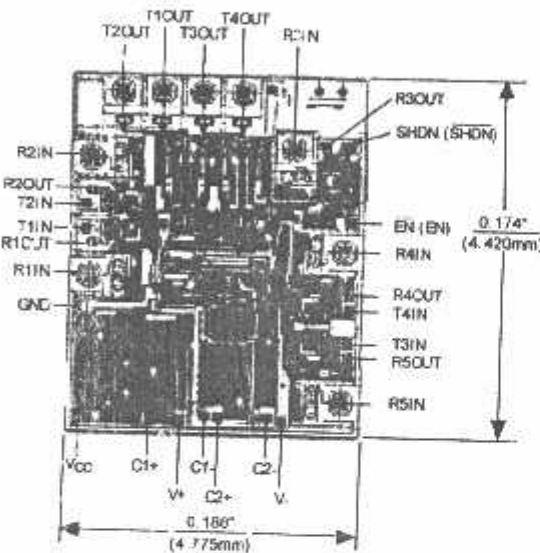
±15kV ESD-Protected, +5V RS-232 Transceivers

Chip Topographies

MAX202E/MAX232E



MAX211E/MAX213E/MAX241E



() ARE FOR MAX213E ONLY

TRANSISTOR COUNT: 123
SUBSTRATE CONNECTED TO GND

TRANSISTOR COUNT: 542
SUBSTRATE CONNECTED TO GND

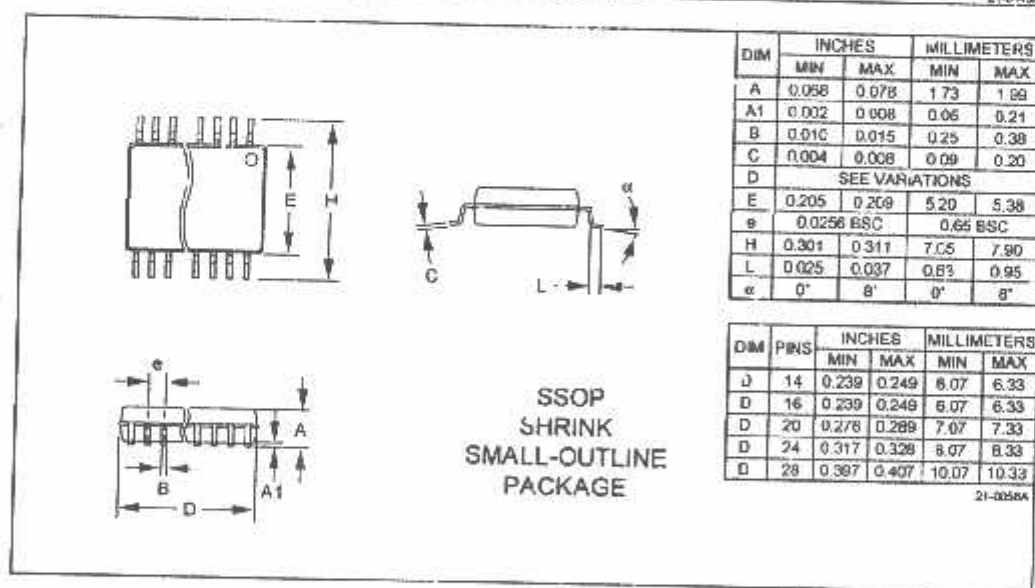
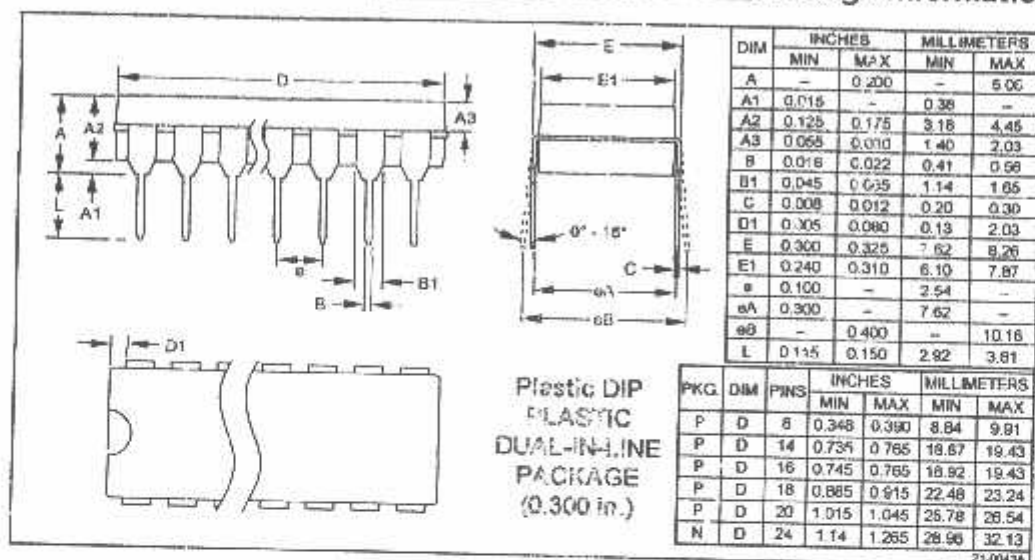
Chip Information

MAX205E/MAX206E/MAX207E/MAX208E
TRANSISTOR COUNT: 328
SUBSTRATE CONNECTED TO GND

±15kV ESD-Protected, +5V RS-232 Transceivers

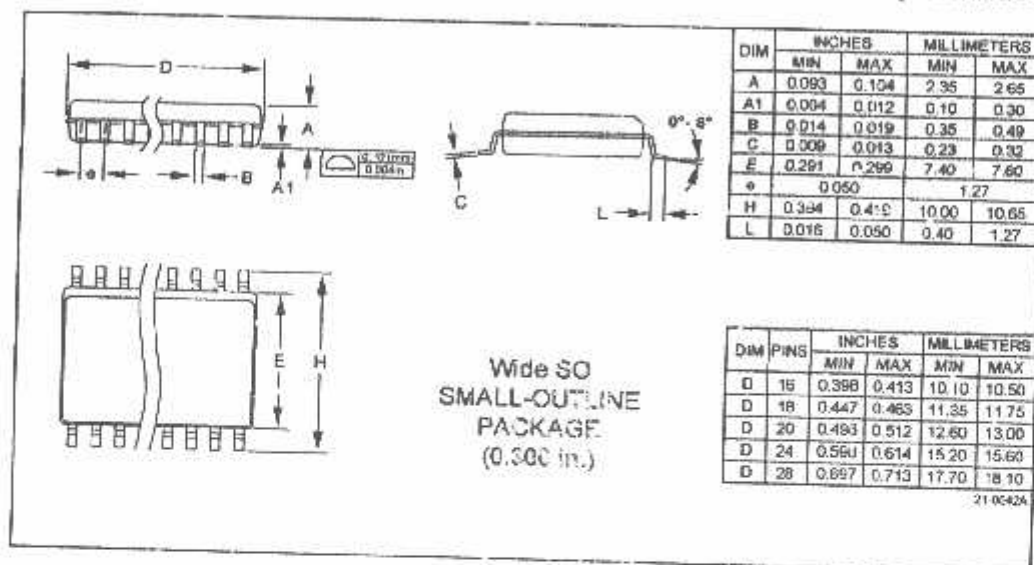
Package Information

MAX202E-MAX213E, MAX232E/MAX241E



±15kV ESD-Protected, +5V RS-232 Transceivers

Package Information (continued)



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 (408) 737-7600
1996 Maxim Integrated Products Printed USA MAXIM is a registered trademark of Maxim Integrated Products.

