SKRIPSI

PERANCANGAN DAN PEMBUATAN *AUTOMATIC WARNING OIL SYSTEM* DAN KECEPATAN PUTARAN MESIN PADA SEPEDA MOTOR BERBASIS MIKROKONTROLLER AT89S8252

Disusun Oleh :

AGUS HARDIYANTO

NIM : 01.17.067

KONSENTRASI TEKNIK ELEKTRONIKA

JURUSAN TEKNIK ELEKTRO S-1

FAKULTAS TEKNOLOGI INDUSTRI

INSTITUT TEKNOLOGI NASIONAL MALANG

2006

LEMBAR PERSETUJUAN

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INSTITUT TEKNOLOGI NASIONAL MALANG
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Judul Skripsi : **PERANCANGAN DAN PEMBUATAN AUTOMATIC WARNING OIL SYSTEM DAN KECEPATAN PUTARAN MESIN PADA SEPEDA MOTOR BERBASIS MIKROKONTROLLER AT 89S8252**

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KATA PENGANTAR

Dengan memanjatkan puji syukur , Alhamdulillah atas Rahmat dan hidayahnya schingga dapat menyelesaikan Tugas akhir ini dengan judul " Perancangan Dan Pembuatan Automatik Warning oil System Dan Kecepatan Putaran Mesin Pada Sepeda Motor Berbasis Mikrokontroller AT89S8252". Tugas akhir ini merupakan persyaratan kelulusan Studi di Jurusan Teknik Elektronika ITN Malang dan untuk mencapai gelar Sarjana Teknik.

Keberhasilan penyelesaian laporan tugas akhir ini tidak lepas dari dukungan dan bantuan dari berbagai pihak. Untukitu penyusun mengucapkan terimakasih yang sebesar besarnya kepada :

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Penyusun telah berusaha semaksimal mungkin dan menyadari sepenuhnya akan keterbatasan pengetahuan dalam menyelesaikan laporan ini.

Harapan penyusun semoga laporan ini berguna bagi ilmu pengetahuan dan pembaca.

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BAB I

PENDAHULUAN

1.1 Latar Belakang

Seiring perkembangan zaman, manusia semakin dituntut untuk melakukan segala sesuatu bukan hanya secara cepat, tetapi juga harus tepat. Untuk itu manusia senantiasa mencari akal guna mempermudah pekerjaannya sehari-hari.

Berkaitan dengan hal tersebut, manusia juga cenderung disibukan dengan pekerjaan yang menumpuk. Biasanya orang yang mempunyai sepeda motor sering lupa untuk mengecek apakah oli mesin sudah diganti atau belum dan kejadian ini yang sering banyak terjadi di masyarakat pada umumnya. Padahal kita semua tahu bahwa apabila kita terlambat mengganti oli akan berdampak pada kerusakan sepeda motor itu sendiri.

Dan hingga saat ini belum ada salah satu pabrikan sepeda motor yang memberikan suatu alat peringatan pengganti oli secara otomatis. Maka dari itu kami akan merancang suatu alat peringatan pengganti oli mesin yang dinamai *automatic warning oil.*

Dari permasalahan tersebut, dengan sedikitnya pengembangan dibidang tersebut, kami merasa masih ada peluang untuk teknologi yang lebih tepat guna dari rancangan kami tersebut. Sehingga kami dalam pengerjaan Tugas Skripsi ini mencoba mengaktualisasikan suatu rancangan tersebut sehingga bermanfaat bagi masyarakat.

1.2 Rumusan Masalah

Pembuatan alat ini meliputi perencanaan hardware dan software. Hardware meliputi Sensor Infra merah, keypad, Liquid Crystal Display (LCD), Information Storage Device ISD,. Sedangkan software yang digunakan meliputi pemrograman mikrokontroller

Permasalahan yang timbul adalah:

- Bagaimana mendesain dan membuat suatu sistem menggunakan Mikrokontroller AT89S8252.
- Bagaimana merancang sistem berbasis mikrokontroler AT89S8252 untuk diaplikasikan pada sistem waktu penggantian oli mesin dan menghitung kecepatan putaran mesin yang menggunakan ISD.

1.3 Batasan Masalah

Berdasarkan permasalahan yang telah dirumuskan sebelumnya, maka pada perancagan dan pembuatan alat tersebut diberi batasan permasalahan, yaitu :

- Perencanaan dan perealisasian sistem mikrokontroller AT89S8252
- Pembuatan software yang dibutuhkan pada mikrokontroller
- Membahas *system warning oil* hanya untuk roda dua (dua tak)
- Yang ditampilkan jarak yang ditempuh dan putaran mesin permenit
- Tidak membahas catu daya (accu).
- Alat ini hanya *prototype*.
- Tidak membahas kebocoran oli.

1.4 Tujuan

Tujuan dari penulisan tugas akhir Perencanaan dan Pembuatan Alat sistem pengingat penggantian oli mesin dan menghitung kecepatan putaran mesin pada sepeda motor Berbasis Microkontroller adalah :

1. Memberi kemudahan dalam mengingat waktu penggantian oli mesin dalam waktu yang telah ditentukan oleh pemakai kendaranya sesuai dengan keunggulan oli mesin yang digunakannya

2. Mengetahui jumlah putaran (Rpm) pada mesin sehingga pemakai kendaraan dapat membandingkan kapan harus menambahkan perseleng (gigik mesin) yang sesuai secara manual.

1.5 Metodologi

Metodologi penulisan tugas akhir ini adalah sebagai berikut :

- Studi literature, yaitu melakukan pencarian informasi dan data-data dari referensi-referensi yang berhubungan dengan alat seperti Microcontroller, ISD
- Perancangan *hardware* dan *software*, yaitu melakukan kegiatan pembuatan program, rangkaian per-blok hingga pembuatan PCB rangkaian keseluruhan sampai melakukan perakitan komponen.
- Pengujian dan analisa, pada bagian ini melakukan uji coba *hardware* dan *sofiware*, kemudian melakukan analisa berdasarkan hasil pengujian yang dilakukan.

1.6 Sistematika Penulisan

Untuk mempermudah dan memperjelas pembuatan laporan akhir ini, maka penulisan disusun secara sistematis sebagai berikut :

BAB I : Pendahuluan

Meliputi latar belakang, rumusan masalah, tujuan, , metodologi, dan sistematika penulisan

BAB II : Teori Dasar

Meliputi uraian mengenai teori-teori yang mendukung perencanaan dan pembuatan alat

BAB III : Perencanaan dan Pembuatan Alat

Meliputi penjelasan blok diagram serta perencanaan dan pembuatan hardware dan software.

BAB IV : Pembahasan

Meliputi prinsip kerja, pengujian, dan spesifikasi alat

BAB V : Penutup

Meliputi kesimpulan dan saran

BAB II

TEORI PENUNJANG

Landasan teori ini sangat membantu untuk dapat memahami suatu sistem. Disamping itu dapat juga dijadikan sebagai bahan acuan didalam merencanakan suatu sistem. Dengan pertimbangan hal-hal tersebut maka landasan teori merupakan bagian yang harus dipahami untuk pembahasan selanjutnya.

2.1 Mikrokontroler AT89S8252

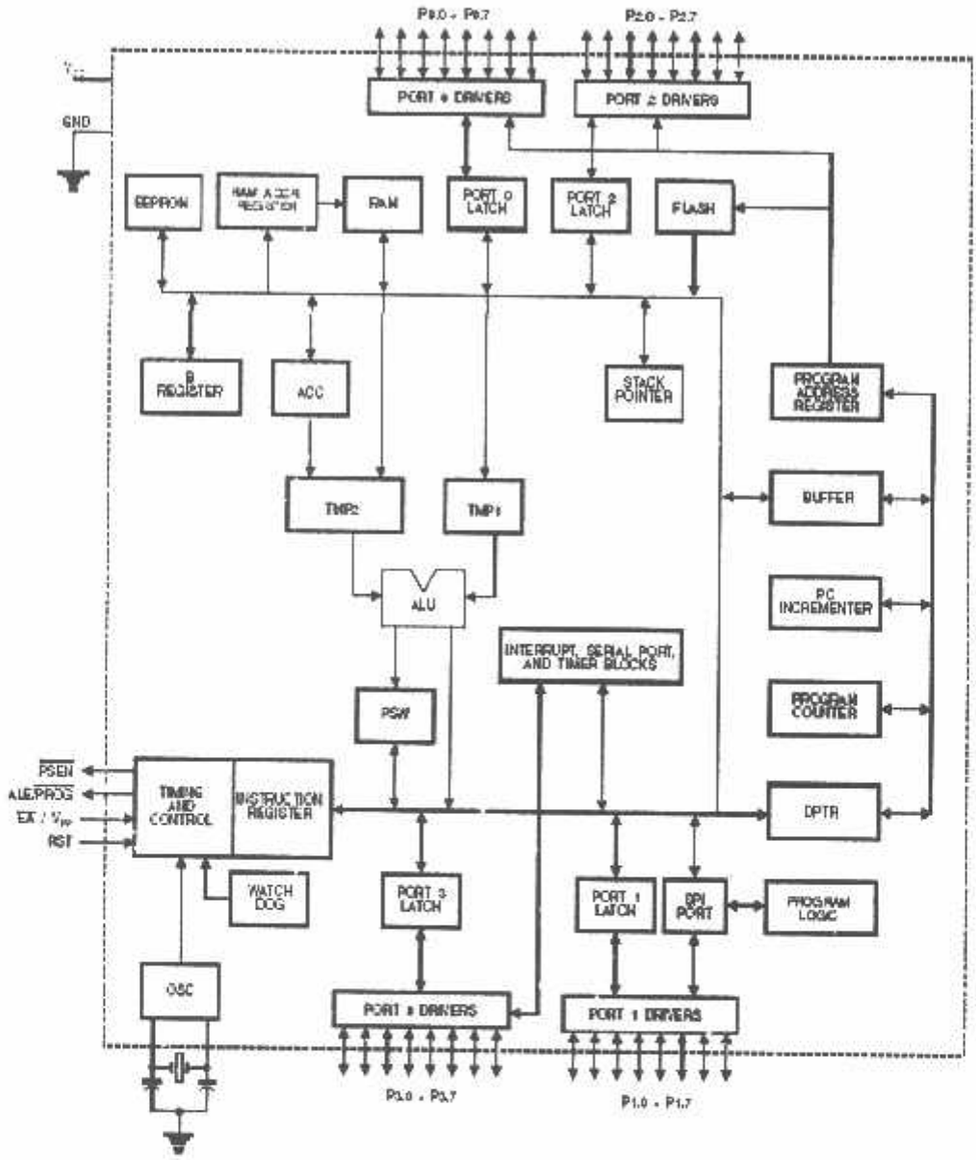
Mikrokontroler AT89S8252 merupakan mikrokontroler 8 bit kompatibel dengan Standar industri MCS-51™ baik atas segi pemrograman maupun kaki tiap pin. Mikrokontroler AT89S8252 menpunyai 8 *Kbyte (Flash Programmable and Read Only Memori*) pada dasarnya mikrokontroler adalah terdiri atas mikroprosesor, *timer*, dan *counter*, perangkat I/O dan internal memori. Mikrokontroler termasuk perangkat yang sudah didesain dalam *chip* tunggal.

Pada dasarnya mikrokontroler mempunyai fungsi yang sama dengan mikroprosesor yaitu untuk mengontrol suatu kerja system. Selain itu mikrokontroler juga dikemas dalam satu *chip* (*single chip*). Didalam mikrokontroler juga terdapat CPU, ALU, PC, SP, dan register seperti dalam mikroprosesor, tetapi juga ditambah dengan perangkat-perangkat lain seperti ROM, RAM, PIO, SIO, *counter* dan sebuah rangkaian *clock*. Mikroprosesor didesain dengan intruksi-intruksi lebih luas dan 8 bit instruksi yang digunakan membaca data instruksi dari internal memori ke ALU. Sebagai suatu system control mikrokontroler bila dibandingkan dengan *mikroprosesor* memiliki kemampuan dan segi ekonomis yang bisa diandalkan karena dalam

mikrokontroler sudah terdapat RAM dan ROM. Sedangkan mikroprosesor didalamnya tidak terdapat keduanya. Terlihat bahwa mikrokontroler Atmel AT89S8252 memilki banyak fitur yang menguntungkan. Dipakainya Downloadable flash memori memungkinkan mikrokontroler ini bekerja sendiri tanpa diperlukan tambahan *chip* lainya. Sementara *Flash* memorinya mampu diprogram hingga seribu kali. Hal lain yang menguntungkan adalah system pemrograman menjadi lebih sederhana dan tidak memerlukan rangkaian yang rumit seperti rangkaian untuk memprogram produk Atmel lainya. Secara umum konfigurasi yang dimiliki mikrokontroler AT89S8252 adalah sebagai berikut :

- Sebuah CPU 8 bit dengan menggunakan teknologi dari Atmel.
- 8K byte Downloadable Flash Memori.
- 2K byte EEPROM
- Sebuah *port* serial dengan control *full duplex* UART (Universal Asynchronous Receiver Transmiter.
- 256 byte RAM internal.
- 32 I/O yang dapat dipakai semua.
- 3 buah Timer/Counter 16 bit .
- SPI Serial Interface.
- Programmable Watchdog Timer .
- Dual Data Pointer.
- Frekuensi kerja 0 sampai 24 MHz
- Tegangan operasi 2,7 Volt sampai 6Volt.
- Kemampuan melaksanakan operasi perkalian, pembagian, dan operasi *Bolean* (bit)

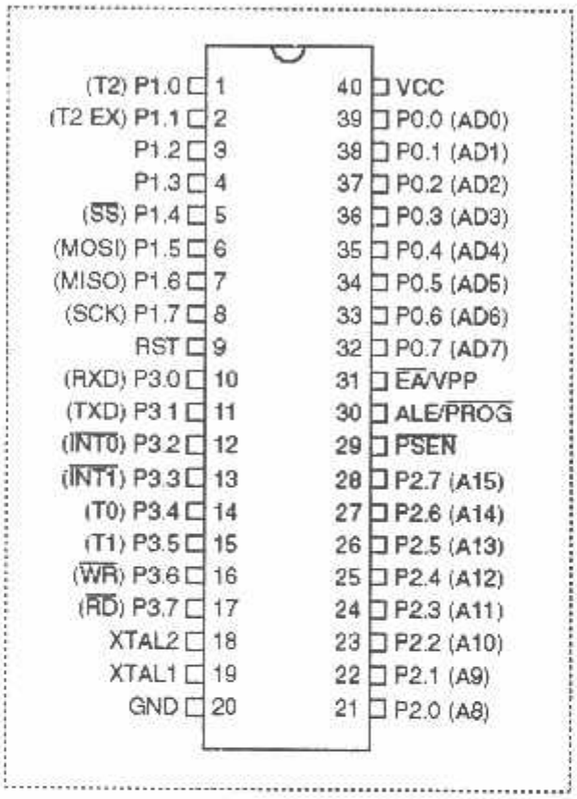
Sedangkan untuk blok diagram AT89S8252 diperlihatkan dalam gambar 2-1



Gambar 2-1 Blok Diagram AT89S8252 [1]

2.1.1. Penjelasan Fungsi Pin AT89S8252

Mikrktroler AT89S8252 mempunyai 40 pin seperti yang ditunjukkan dalam gambar 2-2 Fungsi-fungsi pin dijelaskan sebagai berikut :



Gambar 2-2 Susunan Pin AT89S8252 [1]

- Pin 1 sampai 8

  Port 1 yang terdiri atas pin 1 sampai 8 merupakan saluran masukan/keluaran dua arah.

- Pin 9

  RST merupakan saluran dua masukan untuk m*ereset* mikrokontroler dengan cara memberi masukan logika tinggi.

- Pin 10 sampai 17

  Port 3 yang terdiri atas pin 10 sampai pin 17 merupakan saluran masukan/keluaran dua arah dan mempunyai fungsi khusus seperti yang terlihat dalam tabel 2-1

- Pin 18 dan 19

  $XTAL_1$ dan $XTAL_2$ merupakan saluran untuk mengatur pewktuan system. Untuk pewaktuan dapat menggunakan pewaktuan internal maupun eksternal .

- Pin 20

  Vss merupakan hubungan ke *ground* dari rangkaian.

- Pin 21 sampai 28

  Port 2 yang terdiri atas pin 21 sampai 28 merupakan saluran masukan/keluaran dua arah. *Port* ini mengeluarkan 8 bit bagian alamat tinggi (A8-A15) selama pengambilan instruksi dari memori program eksternal dan pengambilan data memori eksternal yang menggunakan mode pengalamatan 16 bit.

- Pin 29

  PSEN (*Program Store Enable*) merupakan sinyal baca untuk mengaktifkan memori program eksternal.

- Pin 30

  ALE/PROG (*Address Latch Enable*) merupakan pulsa yang berfungsi untuk menahan alamat rendah (A0-A7) dalam *port* 0, selama proses baca/tulis memori eksternal. Frekuensi ALE adalah 1/6 kali frekuensi osilator, dan digunakan sebagai pewaktu. Pin ini juga berfungsi sebagai

saluran program selama dilakukan pemrograman jika menggunakan memori program eksternal.

- Pin 31

  EA/VPP (*External Access Enable*) untuk mengatur penggunaan memori program eksternal dan internal. Pin ini harus dihubungkan dengan *ground* bila menggunakan memori program eksternal dan dihubungkan dengan VPP sebesar 12 Volt jika menggunakan memori program eksternal.

- Pin 32 sampai 39

  Port 0 yang terdiri atas pin 32 sampai 39 merupakan saluran masukan/keluaran. *Port* 0 merupakan saluran alamat rendah (A0-A7) yang dimultipleks dengan saluran *bus* data (D0-D7).

- Pin 40

  Vcc merupakan saluran masukan untuk catu daya positif sebesar 5 Volt DC dengan toleransi kurang lebih 10 %.

2.1.2. Masukan dan Keluaran

Untuk saluran dan keluaran terdapat 4 buah *port* yang masing-masing 8 bit. Saluran ini bersifat dua arah (*bidirectional*) yang berarti dapat difungsikan sebagai masukan atau keluaran, serta dapat dialamati per bit. *Port* 3 selain digunakan sebagai *port* masukan dan keluaran juga dapat digunakan sebagai fungsi pengganti sebagaimana yang terdapat dalam tabel 2-1. Sedangkan AT89S8252 memiliki fitur tambahan yang terdapat pada *port 1* seperti pada tabel 2-2.

Tabel 2-1 Fungsi Pengganti *Port 3* [1]

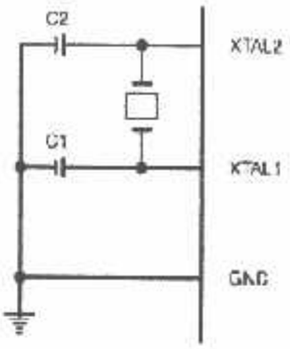
Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Tabel 2-2 Fungsi khusus pada *port 1* AT89S8252 [1]

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

2.1.3. Osilator

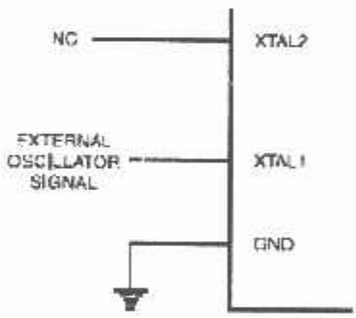
Jantung dari AT89S8252 adalah rangkaian yang membangkitkan pulsa clock yang mesinkronkan semua operasi internal. Mikrokontroler AT89S8252 memiliki osilator internal (*on chip oscillator*) yang dapat digunakan sebagai sumber pewaktu (*clock*) bagi CPU. Untuk menggunakan internal diperlukan sebuah kristal atau resonator keramik antara pin XTAL1 dan pin XTAL2 dan sebuah kapasitor ke *ground*. Konfigurasinya dapat dilihat pada gambar berikut.



Gambar 2-3 Konfigurasi Osilator Menggunakan Kristal [1]

Nilai C1 dan C2 adalah 10 pF – 30 pF bila menggunakan kristal, dan bernilai 10 pF – 40 pF bila menggunakan resonator keramik.

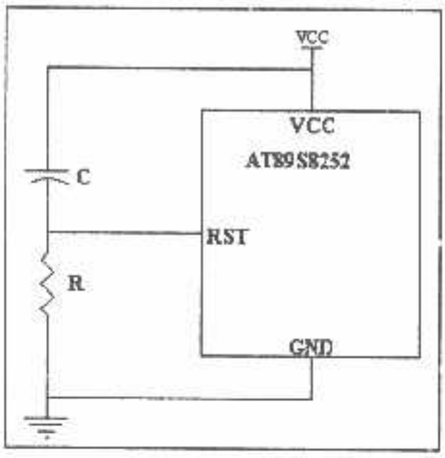
Untuk penggunaan dengan external clock, XTAL2 harus dibiarkan dalam kondisi tidak terhubung. Konfigurasinya dapat dilihat pada gambar berikut ini :



Gambar 2-4 Konfigurasi Osilator Menggunakan External Oscilator Signal [1]

2.1.4. Reset

Rangkaian *power on reset* diperlukan untuk me*reset* mikrokontroler secara otomatis setiap catu daya *on*. Gambar 2-5 menunjukkan rangkaian *power on reset*. Ketika catu daya diaktifkan, rangkaian *reset* menahan logika tinggi pin RST dengan jangka waktu yang ditentukan oleh besarnya pengisian muatan C.



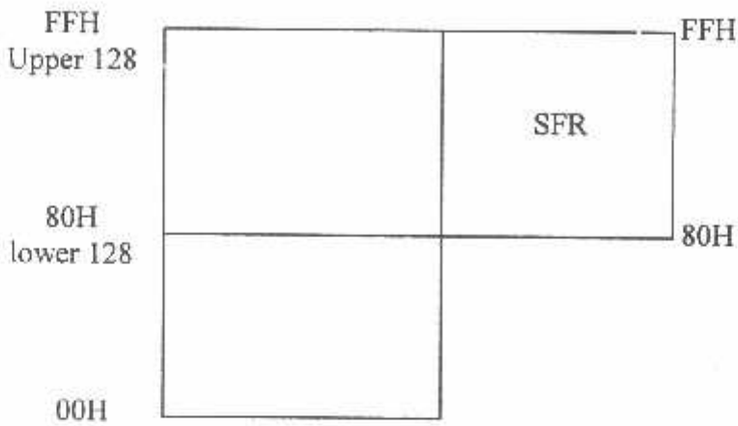
Gambar 2-5 Rangkaian Power On Reset [1]

2.1.5. Data Memori (EEPROM) Dan RAM

Berbeda dengan mikrokontroler standard MCS-51, mikrokontroler Atmel AT89S8252 juga dilengkapi dengan data memori yang berupa EEPROM (*Electrically Erasable Programmable Read Only Memory*). EEPROM yang dimaksud ini besarnya 2 *klo byte* (2K) dan dipakai untuk penyimpanan data.

EEPROM *on-chip* ini diakses dengan mengeset bit EEMEN pada register WMCON pada alamat 96H. Alamat EEPROM ini adalah 000H sampai 7FFH. Intruksi move digunakan untuk mengakses EEPROM internal ini. Bit EEMWE pada register WMCON harus diset ke-1 sebelum seberang lokasi pada EEPROM dapat ditulisi. Program pengguna harus *mereset* bit EEMWE ke '0'jika proses penulisan ke EEPROM tidak diperlukan lagi. Proses penulisan kc EEPROM dapat dilihat dengan membaca bit RDY/BSY pada SFR WMCON. Jika bit ini berlogika rendah maka berarti penulisan EEPROM sedang berlangsung, jika bit ini berlogika tinggi berarti penulisan sudah selesai dan penulisan lain dapat dimulai lagi.

Sedangkan RAM yang ada pada mikrokontroler AT89S8252 adalah berkapasitas 256 *byte* dan kompatibel dengan RAM yang ada pada mikrokontroler standard MCS-51.



Gambar 2-6. Memori Data internal (RAM) [2]

Pada *lower* 128 lokasi memori dibagi menjadi 3 bagian :

1. Register bank 0 – 3

   Lokasi bank register dimulai dari alamat 00H – 1 H yang terdiri dari 32 *bytes*. Register bank ini terdiri dari 4 buah register 8 bit yang dapat dipilih melalui pengaturan *program status word* register.

2. Bit *Addressing*

   Terdiri dari 16 *bytes* yang dimulai dari 20H – 2FH. Masing-masing dari 128 bit lokasi ini dapat dialamati secara langsung yaitu dari 00H sampai 7FH.

3. *Scratch Pad Area*

   Lokasi dari alamat 30H – 7FH atau sebanyak 80 *bytes* yang dapat digunakan sebagai alamat bagi RAM.

2.1.6. Special Function Register (SFR)

Special Function Register merupakan register dengan tugas khusus. SFR pada mikrokontroler AT89S8252 kompatibel dengan mikrokontroler keluarga MCS-51 dan memiliki alamat 80H - FFH sehingga terdapat 128 lokasi alamat untuk SFR. Namun demikian pada mikrokontroler ini tidak berarti memiliki SFR sebanyak 128 buah. Berikut ini adalah gambar letak dari lokasi alamat SFR.

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000					SPCR 00001XX			0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 00000000		SPSR 00XXXXXX						0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111						WMCON 00000010		97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DPOL 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 00X10000	87H

Gambar 2-7. AT89S8252 SFR Map dan Reset Value [1]

Selain itu mikrokontroler AT89S8252 memiliki tambahan SFR . Hal ini tak lain adalah karena terdapatnya tambahan fitur pada mikrokontroler ini. SFR tambahan ini meliputi : T2CON (Timer 2 Register dengan alamat 0C8H), T2MOD (Timer 2 Mode dengan alamat 0C9H), WMCON (*Watcdog and Memory*

Control Register dengan alamat 96H), SPCR (SPI *Control* Register dengan alamat D5H), SPSR (SPI Status Register dengan alamat AAH), SPDR (SPI Data Register dengan alamat 86H).

- SFR untuk Timer 2

  Mikrokontroler AT89S8252 terdapat tambahan sebuah Timer/Counter yang diberi nama timer 2 (sehingga AT89S8252 memiliki 3 Timer /Counter yaitu Timer/Counter 0, Timer/Counter 1, Timer/Counter 2). Pada Timer/Counter 2 ini dikendalikan oleh *Special Function* Register yang bernama T2CON (Timer 2 Control), T2MOD (Timer @ MODE) dan sepasang register RCAP2H, RCAP2L merupakan register *capture/reload* untuk Timer 2 dalam 16 bit *capture mode/auto reload mode.*

- SFR untuk *Watchdog* Memori.

  Untuk menggunakan *Watchdog* timer atau memori, maka dapat dilakukan dengan mengatur SFR yang bernama WMCON dengan alamat 96H.

- SFR pengontrol SPI

  Berbeda dengan mikrokontroler MCS-51, AT89S8252 memiliki fasilitas SPI (*Serial Perpheral Interface*). Fasilitas ini memungkinkan transfer data kecepatan tinggi secara sinkron antara mikrokontroler dengan peripheral atau antar mikrokontroler AT89S8252. Fitur ini meliputi :

  a. Full Duplek, 3 kawat dengan transfer data secara sinkron .
  b. Operasi Master atau Slave.
  c. Frekuensi maksimum 6 MHz.
  d. 4 bit rate terprogram.

2.1.7. Timer dan Counter

Dalam mikrokontroler AT89S8252 terdapat tiga buah pewaktu/pencacah (timer/counter 16) 16 bit yang dapat diatur melalui perangkat lunak, yaitu pewaktu / pencacah 0 dan pewaktu / pencacah 1. Timer/counter ini diatur oleh *special function* register yaitu Timer/Counter *Control* (TCON alamat 88H), dan Timer/Counter Mode *Control* (TMOD alamat 89H). Selain itu nilai byte bawah dan byte atas dari Timer/Counter disimpan dalam register TL dan TH.

Jika difungsikan sebagai Timer, maka akan menggunakan system clock sebagai sumber masukan pulsanya. Jika sebagai Counter (pencacah), maka akan menggunakan pulsa dari luar (eksternal) sebagai masukan pulsanya. Pada Port 3 terdapat fungsi khusus yaitu TO (masukan luar untuk Timer/Counter 0) dan T1 (masukan luar untuk Timer/Counter 1). Pemilihan mode Timer/Counter dikontrol oleh register TMOD. Dengan memberikan nilai tertentu pada register TMOD dapat dipilih mode operasi untuk Timer/Counter 0 dan Timer/Counter 1 seperti terlihat dalam Tabel 2-3.

Tabel 2-3 Mode Operasi Timer/Counter 0 dan 1 [2]

M2	M1	Mode	Keterangan
0	0	0	13 bit Timer
0	1	1	16 bit Timer
1	0	2	8 bit auto-reload
1	1	3	Split Mode

Pada mikrokontroler AT89S8252 terdapat tambahan Timer 2. Timer yang lain adalah Timer 0 dan Timer 1. Timer 2 ini merupakan Timer/Counter 16 bit dan memiliki 3 mode operasi yaitu *capture, auto reload* (*up down counting*) dan baud rate generator. Untuk memilih mode ini dilakukan dengan mengatur bit pada SFR T2CON (Timer 2 Control Register). Timer 2 ini terdiri dari 2 buah timer 8 bit register yaitu TH2 dan TL2. pada fungsi Timer, register TL2 dinaikkan (increment) tiap siklus mesin. Karena siklus mesin terdiri dari 12 periode osilasi, maka count rate menjadi 1/12 dari frekuensi osilator. Sedangkan pada fungsi Counter, register dinaikkan berdasarkan tanggapan adanya transisi tinggi ke rendah pada pena yang bersesuaian (dalam hal ini pin T2 atau P1.0). Tabel berikut menunjukkan mode operasi yang dapat dijalankan pada timer 2.

Tabel 2-4 Mode Operasi Timer 2 [1]

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

RCLK = Receive clock enable. Jika diset menyebabkan serial port menggunakan pulsa overflow Timer 2 sebagai detak penerimaan pada serial port. Jika RCLK = 0 Timer 1 yang digunakan.

TCLK = Transmit clok enable. Jika diset menyebabkan serial port menggunakan pulsa overflow Timer 2 sebagai detak pengiriman. Jika TCLK = 0 pulsa overflow timer 1 yang digunakan.

CP/RL2 = Pemilihan capture/Reload. Jika diset maka proses capture yang terjadi sedangkan jika bit ini diclear maka proses reload.

TR2 = Bit untuk mengatur start/stop untuk timer 2 jika TR2 = 1 Timer akan aktif.

2.1.8. Idle Mode

Saat *Idle Mode* mikrokontroler tidak melakukan apa-apa. Tetapi peralatan lain yang terhubung tetap aktif. Kondisi ini dapat dihentikan dengan sebuah *interrupt* atau dengan me-*reset* system.

2.1.9. Sistem Interupt

Mikrokontroler AT89S8252 mempunyai 6 buah sumber interrupt yang dapat membangkitkan permintaan interrupt, yaitu INTO, INT1, T0, T1, T2 dan port serial.

Saat terjadinya interrupt, mikrokontroler secara otomatis akan menuju ke *sub rutin* pada alamat tersebut. Setelah interrupt service selesai dikerjakan, mikrokontroler akan mengerjakan program semula. Dua sumber interrupt *external* adalah INTO dan INT1, dimana kedua interupsi eksternal akan aktif atau aktif transisi tergantung isi dari IT0 dan IT1 pada register TCON. Interupsi T0, T1, T2 aktif pada saat timer yang sesuai mengalami *roll over*, interupsi serial dibangkitkan dengan melakukan operasi OR pada R1 dan T1. Tiap-tiap sumber interupsi dapat *enable* atau *disable* secara otomatis.

Tingkat prioritas semua sumber interupsi dapat diprogram sendiri-sendiri dengan set atau *clear bit* pada SFRS IP (*interrupt Priority*).

Tabel 2-5 Alamat Sumber Interupsi [1]

(MSB=LSB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

2.2 ISD (Information Storage Device) 1400

Peralatan penyimpanan informasi suara, ISD seri 1400 menpunyai kualitas bagus, dengan durasi penyimpanan dari 16 sampai 20 detik. Peralatan CMOS yang ada didalamnya adalah *chip oscilator, mocrophone preamplifier, automatic gain control, antilisiang filter, smouthing filter, speaker amplifier*. Pada pengembangannya, ISD 1400 adalah kompatibel dengan mikrokontroler, mengijinkan penyimpanan dan pengalamatan yang komplek. Perekaman disimpan dalam suatu *chip* yang tidak mudah berubah dalam *cell* memori.

Sinyal suara dan audio disimpan secara langsung ke memori pada tempat naturalnya dengan kualitas suara yang bagus. Untuk karakteristiknya adalah sebagai berikut:

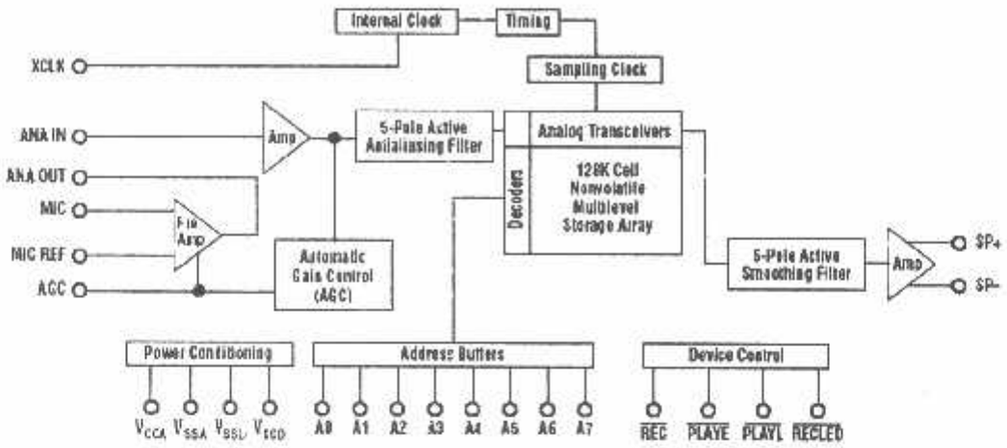
- *Chip* tunggal yang mudah digunakan untuk merekam atau memainkan suara.

- Durasi perekaman 14 dan 20 detik.
- Suara yang direproduksi menpunyai kualitas yang bagus dan alami.
- Bisa dioperasikan secara manual dengan *switch* atau dengan mircokontroler.
- Bisa dipasang bertingkat untuk durasi waktu yang lama.
- Arus pada saat *standby* = 1 µA.
- Tidak perlu power untuk tetap menyimpan data dalam IC, sehingga tidak perlu baterai cadangan.
- Data dapat tahan hingga 100 tahun.
- 100.000 kali rekam.
- *Power supply* +5 Volt.

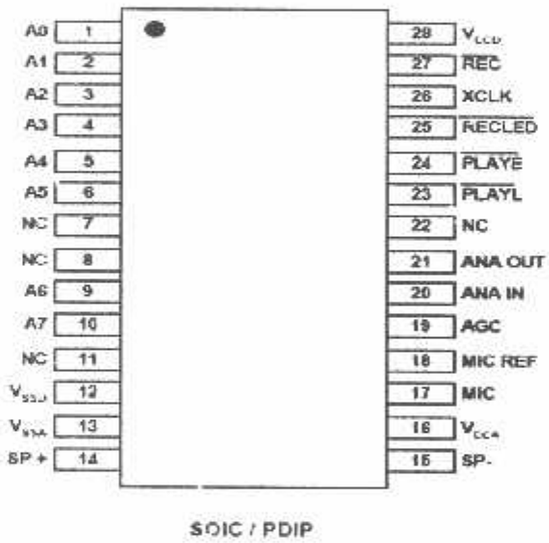
Tabel 2.6. Seri ISD 1400 [3]

Tipe	Waktu (detik)	Sample rate (KHz)	Filter band pass (Hz)
ISD 1416	16	8.0	3300
ISD 1420	20	6.4	2600

Dengan melihat tabel diatas, maka dapat diketahui bahwa IC penyimpan suara ISD seri 1420 ini adalah merupakan jenis EEPROM (*Electrically Erasable Programable* ROM). EEPROM adalah jenis ROM yang dapat diprogram, dihapus dan diprogram ulang secara elektrik. IC ISD 1420 ini dapat melakukan perekaman suara atau pesan dengan jangka waktu durasi maksimum 20 detik. dengan sample rate 6.4 Khz.



Gambar 2-8. Diagram blok ISD1400 [3]



Gambar 2-9. Susunan Kaki ISD 1400 [3]

Keterangan pin ISD 1400 :

1. Microphone Input (Mic)

   Input microphone akan mentransfer sinyal yang akan masuk ke amplifier yang berada di dalam IC rangkaian *AGC* mengontrol penguatan antara -15

7. Voltage Input (V_{CCA},V_{CCD})

   Merupakan kaki untuk memasukkan tegangan +5 Volt pada IC.

8. Ground Input (V_{SSA},V_{SSD})

   Input untuk kaki *ground* pada IC.

9. Speaker *Output* (SP+ dan SP-)

   Pin ini digunakan untuk mengeluarkan suara yang telah direkam ke speaker atau ke *device* lainnya. Output ini menpunyai impendasi sebesar 16 Ohm.

10. Optimal *Eksternal Clock* (XCLK)

    Digunakan untuk menenbahkan kristal clock bila dibutuhkan pewaktuan yang lebih besar dan presisi. Bila input ini tidak digunakan, harus dihubungkan dengan *ground.*

11. PLAYL (playback, level-activated)

    Ketika sinyal input ini berpindah dari *high* ke *low*; maka PLAYL akan berjalan. *Playback* akan berjalan sampai input ini tertekan *high*, tanda akhir dari pesan tercapai atau ruang memori sudah habis. ISD akan kembali ke mode *stanby* setelah *playback* ini terhenti.

12. PLAYE (playback, edge-activated)

    Ketika sinyal akan berpindah menuju *low* (*low – going – transition*) terdeteksi di *input* ini, maka PLAYE akan berjalan. *Playback* berjalan sampai tanda akhir dari pesan tercapai atau akhir dari ruang memori tercapai. Setelah menyelesaikan *playback*, ISD secara otomatis akan kembali ke mode *stanby*, menakan PLAYE ke *high* pada waktu *playback* akan berhenti bila mencapai ahkir dari pesan atau ruang memori habis.

13. REC (Record Input)

Input sinyal akan aktif dalam keadaan *low*. ISD 1420 akan merekam bila REC dalm keadaan *low*, dan sinyal ini harus terus dalam keadaan *low* bila ingin terus merekam. Jika input REC ini tertekan *low* dalam keadaan kita masih memutar ulang (*playback*), maka *playback* akan berhenti dan ISD akan merekam. Dalam perancangan dan pembuatan alat ini, harga kapasitor ditentukan sama dengan yang terdapat dalam data sheet ISD 1420.

14. RECLED (Record Led)

Output dari RECLED akan *low* selama perekaman, maka output ini biasanya digunakan untuk menjalankan sebuah LED yan berguna untuk mengetahui bahwa sedang terjadi proses perekaman. RECLED ini akan *low* sebentar ketika tanda akhir dari pesan tercapai pada saat *playback*.

2.2.1. Cara perekaman / pengisian suara

Langkah langkah yang dilakukan untuk memulai perekaman yang mengeset alamat / durasi waktu yang dibutuhkan untuk perekaman. Pada saat memulai perekaman sinyal REC LOW maka dengan demikian secara otomatis pin ANA – IN bekerja. Pada saat inilah dimasukan suara yang akan direkam melalui microphone. Jika ruang sudah terisi penuh maka sinyal REC harus dikembalikan keposisi HIGH. Tanda ahkir dari pesan (end – off – message merker) akan otomatis terekam sesudah itu. Tanda ini berguna untuk memutuskan *playback* secara otomatis bila rekaman sudah habis. ISD 1420 akan langsung ke stanby bila REC dalam keadaan high.

2.3 Liquid Crystal Display (LCD)

2.3.1 Konfigurasi LCD

Liquid Crystal Display adalah modul tampilan berkonsumsi daya yang relatif rendah dan terdapat sebuah kontroller CMOS didalamnya. Kontroler tersebut sebagai pembangkit karakter dari ROM/RAM dan display data RAM. Semua fungsi tampilan dikontrol oleh suatu intruksi dan modul LCD dapat dengan mudah untuk diinterfacekan dengan mikroprossor/mikrokontroller. Input yang diperlukan untuk mengendalikan modul ini berupa bus data yang termultipleks dengan bus alamat dan 3 bit sinyal kontrol. Pengendali dot matrik LCD dilakukan secara internal pada modul LCD sendiri.

LCD merupakan suatu bentuk kristal cair yang akan beremulsi apabila dikenakan tegangan padanya. Tampilannya ini berupa dot matrik 5 x LCD sehingga jenis huruf yang dapat ditampilkan akan lebih banyak dan lebih baik resolusinya jika dibandingkan dengan 7 segment.

Gambar 2-10 Deskripsi pin pada LCD Tipe M1632

(Sumber : LCD Manual Book `-

LCD tipe M1632 memiliki ciri-ciri sebagai berikut :

- LCD ini terdiri dari 32 karakter dengan 2 baris masing-masing 16 karakter dengan display dot matrik 5 x 7
- Karakter generator Rom dengan 192 tipe karakter
- Karakter generator RAM dengan 8 tipe karakter

- 80 x 8 display data RAM
- Dapat diinterfacekan ke MPU 8 atau 4
- Dilengkapi fungsi tambahan : *display clear, cursor hpme, display ON/OFF, cursor ON/OFF, display character blink, cursor shift, dan display shift.*
- Internal Data
- Internal Otomatis, reset pada saat power ON
- +5 volt PSU Tunggal

Tabel 2-6 Konfigurasi Pin-pin LCD

NO	SYMBOL	LEVEL	FUNCTION
1	Vss	-	0 Ground
2	Vcc	-	5 V + 10%
3	Vee	-	LCD Drive
4	RS	H/L	H : Data Input
			L : Intruksi Input
5	R/W	H/L	H : Read L : Write
6	E	H/L	Enable Signal
7-14	DB0-DB7	H/L	Data Bus
15	Light LCD	-	Menyalakan lampu LCD max 200 mA
16	Light LCD	-	Ground

(Sumber : LCD Manual Book)

2.3.2 Interuksi Operasi Dasar

2.3.2.1 Register

Kontroller dari LCD mempunyai dua buah register 8 bit yaitu register intruksi (IR) dan register data (RD). IR menyimpan intruksi seperti *display clear, cursor shift* dan *display data* (DD RAM) serta *character generator* (CG RAM). DR menyimpan data untuk ditulis di DD RAM atau CG RAM atau membaca data dari DD RAM atau CG RAM. Ketika data ditulis ke DD RAM atau CG RAM maka DR akan secara otomatis menulis data ke DD RAM atau CG RAM dan data pada DD RAM atau CG RAM hendak dibaca maka alamat data ditulis pada IR sedangkan data alamat dimasukkan melalui DR dan mikroprosesor membaca data dari DR.

Tabel 2-7 Tabel Register Seleksi

RS	R/W	OPERASI
0	0	Seleksi IR, IR Write Display Clear
0	0	Busy Flag (DB7) @counter (DB0-DB7) Read
1	0	Seleksi DR, DR Write
1	1	Seleksi DR, DR Read

(Sumber : LCD Manual Book)

2.3.2.2 Busy Flag

Busy Flag menunjukkan bahwa modul siap untuk menerima instruksi selanjutnya. Sebagaimana yang terlihat pada table register seleksi sinyal akan melalui DB7. Jika RS = 0 dan R/W = 1. Jika bernilai 1 maka modul sedang melakukan kerja internal dan intruksi tidak dapat diterima. Sehingga status dari flag ini harus diperiksa sebelum melaksanakan intruksi selanjutnya.

2.3.2.3 Address Counter

AC menunjukkan lokasi memori dalam modul LCD. Pemilihan lokasi alamat itu diberikan lewat registerintruksi (IR). Ketika data ada pada A, maka AC secara otomatis menaikkan atau menurunkan alamat tergantung dari *Entry Mode Set*.

2.3.2.4 Display Data RAM (DD RAM)

Pada LCD masing-masing line mempunyai range alamat tersendiri. Alamat ini diekspresikan dengan bilangan *Hexadecimal*. Untuk itu 1 range alamat berkisar 00H-0FH sedangkan untuk line 2 range alamat berkisar antara 40H-4FH.

2.3.2.5 Character Generator ROM (CG ROM)

CG ROM mempunyai tipe dot matrik 5 x 7 dan data pada LCD telah tersedia ROM sebagai pembangkit Character dalam kode ASCII.

2.3.2.6 Character Generator RAM (CG RAM)

CG RAM digunakan untuk pembuatan karakter tersendiri melalui program.

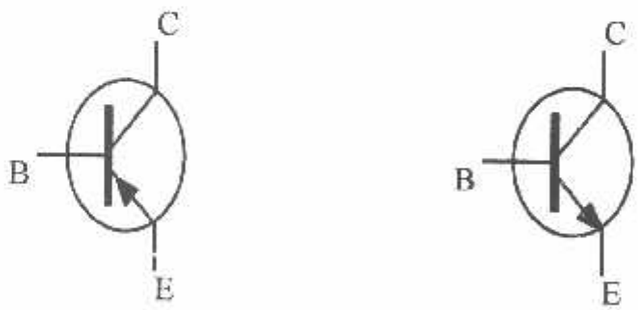
Tabel 2-8 Fungsi Terminal Pada LCD

Nama Signal	Jml Term	I/O	Tujuan	Fungsi
DB0-DB3	4	I/O	MPU	Sebagai lalu lintas data dan intruksi ke atau dari MPU Low Byte
DB4-DB7	4	I/O	MPU	Sebagai lalu lintas data atau intruksi 2 arah upper byte. DB7 sebagai busy flag
E	1	I	MPU	Sinyal Start (read/write)
R/W	1	I	MPU	Seleksi Sinyal 0 = write 1 = read
RS	1	I	MPU	Seleksi Register
VLS	1	-	PS	0 = intruksi reg (wr) Busy flag addr counter (rd) 1 = data reg (wr dan rd)
7	1	-	PS	Mengatur Tampilan LCD
Vss	1	-	PS	+5 volt

(Sumber : LCD Manual Data Book)

2.4 Transistor

Transistor adalah suatu komponen aktif yang dibuat dari bahan semikonduktor. Apabila kita mendoping semikonduktor untuk mendapatkan kristal NPN atau PNP, maka kristal seperti ini disebut Transistor *Junction*. Daerah tipe N mempunyai banyak sekali elektron pita konduksi dan daerah tipe P mempunyai banyak *hole*. Jadi transistor *junction* mempunyai dua macam pembawa muatan yaitu elektron bebas pada daerah N dan *hole* pada daerah P. Oleh karena itu transistor junction disebut juga transistor dua kutub (*bipolar*). Transistor bipolar ada dua macam yaitu transistor jenis NPN dan PNP. Adapun simbol dari kedua transistor seperti pada gambar 2.12 berikut ini :

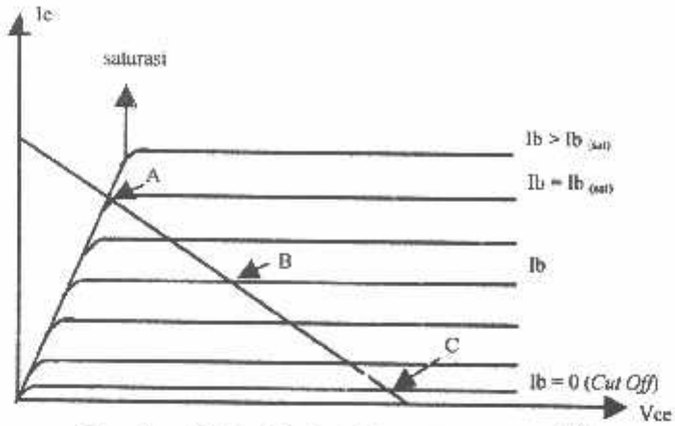


Transistor PNP *Transistor NPN*

Gambar 2-13. Simbol Transistor Bipolar [6]

Daerah kerja dari transistor terbagi menjadi tiga yaitu : daerah kerja *cut off*, daerah kerja saturasi dan daerah kerja aktif.

Untuk lebih jelasnya mengenai daerah kerja Transistor dapat dilihat pada gambar 2.13. dibawah ini :



Gambar 2-14. Garis Beban Transistor [6]

A = Penjenuhan (saturasi)

B = Titik Kerja

C = Titik Sumbat (*Cut Off*)

Untuk garis beban diperoleh dengan persamaan :

$$V_{CC} = I_C \cdot R_C + V_{CE}$$

Saat *cut off* $I_B = 0$, schingga :

$$I_C = \beta_{dc} \cdot I_B$$

$$I_B = \frac{Vcc - Vbe}{Rb}$$

$$V_{CE\,(cut\,off)} = V_{CC} \text{ (pada titik A)}$$

Saat saturasi, maka $I_B = I_{B\,(sat)}$, schingga :

$$I_{C\,(sat)} = \frac{Vcc}{Rc} \text{ (titik B)}$$

Jika arus basis lebih besar atau sama dengan I_B saturasi, titik kerja Q berada dalam ujung atas dari garis beban, maka transistor seperti sebuah saklar tertutup. Sebaliknya, jika arus basis nol, transistor bekerja dalam ujung bawah dari garis beban, dan transistor seperti sebagai saklar terbuka .

Daerah Kerja Transistor

Berdasarkan pada teori di atas maka dapat dilihat bahwa transistor mempunyai 3 daerah yaitu : Basis, Kolektor dan Emitor. Pada transistor NPN mempunyai dua junction , yaitu *junction* antara Emitor dan Basis serta *junction* antara Basis dan Kolektor. Oleh karena itu, transistor bersifat seperti dua buah dioda. Sedangkan pada transistor PNP adalah kebalikan dari transistor NPN khususnya untuk karakteristik arus dan tegangannya.

2.5 Light Emitting Dioda (LED)

Sesuai dengan namanya LED digunakan untuk menghasilkan emisi. Emisi tergantung dari bahan yang menyusunnya misalnya untuk LED berbahan Galium Arsenid (GaAs) mempunyai panjang gelombang 940 nm sedangkan untuk berbahan Galium Alumunium Arsenid (GaAlAs) dengan panjang gelombang 880 nm sehingga lebih efisien dan meningkatkankepekaan sistem dibanding dengan GaAs.

LED biasanya digunakan dalam rangkaian dengan daya keluaran sebesar 2 sampai 7 mV . Dengan arus maksimum 100 mA serta tegangan rata-rata pada LED 1,1 Volt. Dengan penurunan rumusnya adalah:

$$I = \frac{Vs - Vied}{Rs} \quad \text{.....} \quad 2.30$$

Gambar 2-15 Simbol Infra –merah

2.6 Fotodioda

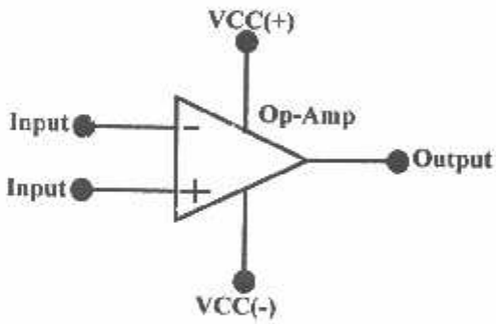
Fotodioda adalah piranti detector peka cahaya yang tersusun dari sambungan semikonduktor *pn* yang bekerja pada arus balik . Fotodioda merupakan salah satu fotodetektor , yaitu optoelektronika yang dapat mengubah cahaya datang menjadi besaran listrik.

Pada fotodioda terdapat sebuah jendela yang memungkinkan cahaya untuk masuk melalui pembungkus dan mengenai persambungan *pn* , maka jumlah elektron – elektro valensi semakin besar yang berarti jumlah pembawa minoritas menjadi bertambah banyak yang mengakibatkan semakin besar arus baliknya.

Gambar 2-16. Fotodioda

2.7 Penguat Operasional (Operational Amplifier)

Penguat operasional adalah chip yang umumnya digunakan untuk penguatan sinyal dan nilai penguatannya dapat dikontrol melalui penggunaan resistor dan komponen lainnya. Umumnya op-amp terdiri dari dua input dan satu output. Pemakaian penguat operasional digunakan untuk menperkuat sinyal dari transducer (sensor) tanpa menpengaruhi ketelitian sensor, sebab impendasi inputnya sangat tinggi sehingga dapat dianggap tidak menyerap arus pada masukannya. Mutu penguatan itu tergantung dari dari mutu Op-Amp yang digunakan. Selain itu ketepatan penguatan Op-Amp dipengaruhi ketepatan dan mutu komponen pendukung yang digunakan.



Gambar 2-11. Rangkaian Dasar Op-Amp [5]

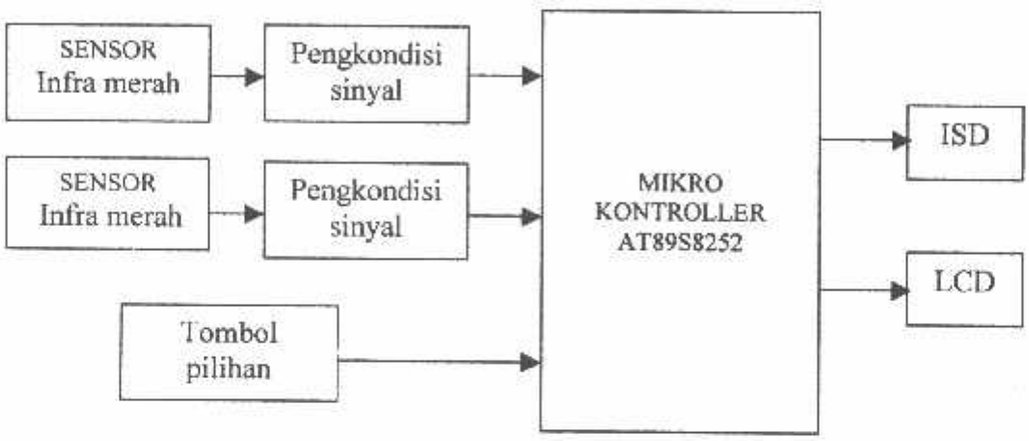
Pada gambar 2.11. diatas menunjukkan bahwa Op-Amp menpunyai input yang berfungsi sebagai masukan pembalik (*inverting*) dan masukan tak membalik (*non inverting*).

BAB III

PERENCANAAN DAN PEMBUATAN ALAT

3.1. Pendahuluan

Bagian ini menjelaskan tentang perencanaan dan pembuatan alat warning oil dan putaran mesin (rpm) berbasis mikrokontoller AT89S8252



Gambar 3-1 Blok Diagram Rangkaian

Sestem ini secara umum dapat dibagi menjadi dua bagian besar yaitu bagian mengukur jarak tempuh dan menghitung jumlah putaran mesin (rpm).

Dari gambar blok diagram di atas dapat dijelaskan fungsi dari masing–masing blok, antara lain :

- Mikrokontroller AT89S8252

  Berfungsi sebagai pengendali keseluruhan sistem.

  Mikrokontroller akan memproses input yang telah diberikan dan mengendalikanoutput.

- ISD

  Berfungsi sebagai perekam dan memutar kembali suatu pesan pendek kedalam Chip.

- Optocoupler

  Sebagai pendeteksi pulsa-pulsa yang dihasilkan oleh putaran mesin.

- Keypad

  Sebagai masukan data, untuk mengatur menu dan data pada MCU

- LCD

  Sebagai tampilan dari RPM putaran mesin pada coil.

- Sensor Putaran

  Sensor putaran yang dipakai adalah infra merah sebagai pemancar dan fhoto dioda sebagai penerimanya.

Prinsip kerjanya :

Pertama-tama menyalakan / mengaktifkan mesin sepeda motor maka dengan begitu koil akan ikut berputar. Kemudian perputaran koil tersebut akan dideteksi oleh sensor putaran yang akan mendeteksi putaran rpm / mesin kemudian sensor akan mengirim pulsa ke mikrokontroler dan oleh mikrokontroler akan diolah kemudian akan dikirim ke LCD untuk menampilkan angka yang dideteksi.

Kemudian proses kedua sensor autocopler akan mendeteksi jarak yang ditempuh sesuai dengan inputan dari kypet , berapa jarak yang ditentukan untuk penggantian oli sesuai dengan mutu dari oli. Lalu sinyal dari sensor tersebut akan dikirim ke mikrokontroler dan oleh mikrokontroler diteruskan ke lampu indikator dan ISD sebagai peringatan kepada pengendara sepeda motor.

Reset digunakan apabila oli mesin telah diganti, maka dengan menekan tombol reset secara otomatis agar yang tampil pada rpm akan kembali ke 0 lagi dan siap untuk digunakan lagi.

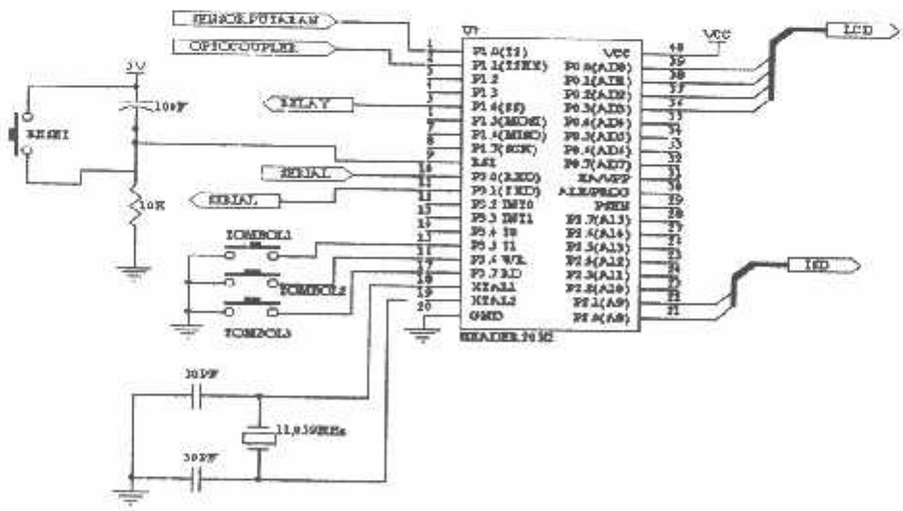
3.2 Perencanaan Perangkat Keras

Bagian ini menguraikan perencanaan perangkat keras yang meliputi perencanaan :

1. Sistem Mikrokontroller AT89S8252
2. Antarmuka Mikrokontroller ke keypad
3. Antarmuka Mikrokontroller ke modul LCD

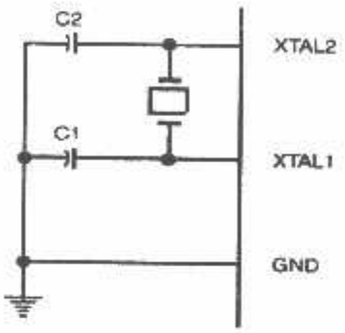
3.2.1 Sistem Mikrokontroller AT89S8252

Gambar 3-2 menunjukkan rangkaian mikrokontroller AT89S8252 yang akan diantarmukakan ke keypad, modul kartu debet, modul LCD dan transceiver saluran transmisi RS-485. Pada masing-masing blok memiliki rangkaian yang sama, hanya pada blok dapur tidak dipasang modul kartu debet.



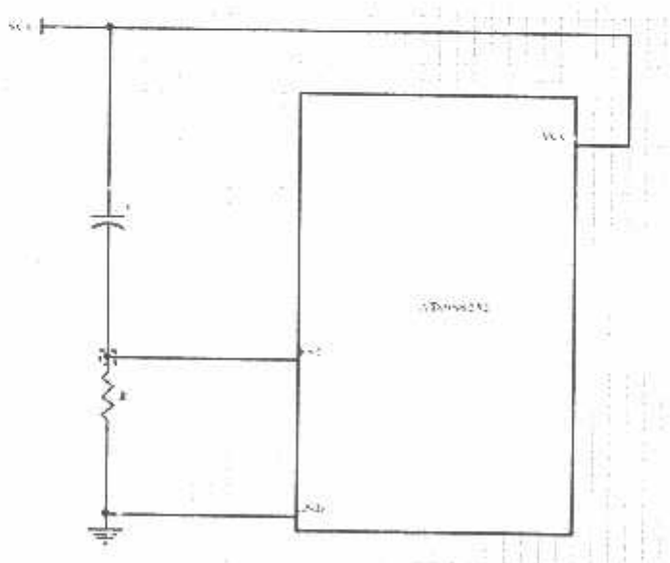
Gambar 3-2 Rangkaian Mikrokontroller AT89S8252

Rangkaian yang mendukung mikrokontroller ada dua, yaitu rangkaian clock dan rangkaian reset. Kristal dengan frekuensi 11,0592 Mhz serta dua buah kapasitor 30pF (sesuai dengan datasheet AT89S8252) digunakan untuk menggerakkan osilator internal



Gambar 3-3 Rangkaian Pewaktuan dengan Osilator Internal

Untuk mereset mikrokontroller, pin RST harus diberi logika tinggi selama sekurangnya dua siklus mesin (24 periode osilator). Untuk membangkitkan sinyal reset pada saat awal catu daya yang dihidupkan, suatu reset otomatis dapat dilakukan dengan menghubungkan pin RST ke rangkaian *Power-On Reset.* Rangkaian *Power-On Reset* ditunjukkan dalam gambar 3-4.



Gambar 3-4 Rangkaian Power-On Reset

Pemberian catu daya pada mikrokontroller tanpa suatu sinyal reset dapat menyebabkan CPU memulai eksekusi intstruksinya dari lokasi yang tak tentu. Ini disebabkan karena Program Counter tidak terinisialisasi. Dengan adanya rangkaian reset, pin RST akan ditahan dalam kondisi logika tinggi selama selang beberapa saat tergantung nilai kapasitor dan resistor yang mempengaruhi jangka waktu pengosongan muatan kapasitor. Jangka waktu pengosongan muatan C yang masih dalam level logika 1 dapat dihitung dengan persamaan berikut.

Dalam sistem mikrokontroller ini direncanakan penggunaaan port yang tersedia sebagai :

1.Port 1.0 s/d Port 1.3 sebagai jalur data untuk LCD.

2.Port 1.4 sebagai relay.

3.Port 2.0 s/d port 2.7 sebagai jalur data untuk keypad.

4.Port 3.0 sebagai jalur data RS-232

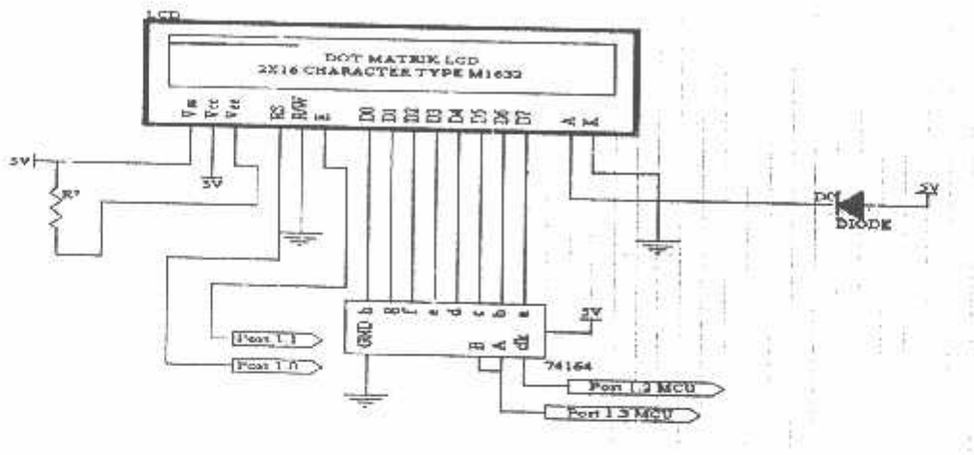
Port 3.1 sebagai jalur data RS-

3.2.2 Rangkaian Antarmuka Modul LCD (*Liquid Cyrstal Display*)

Sebagai unit keluaran system mikrokontroller, port 1 digunakan sebagai jalur data bagi penampil LCD. Dalam aplikasi ini tidak dilakukan operasi pembacaan dari register intruksi internal ataupun register data internal modul LCD, Oleh karena itu jalur kontrol R/W dihubungkan langsung ke ground sehingga mode operasi yang dilakukan selalu operasi penulisan ke register instruksi maupun register data internal modul LCD.

Rangkain antarmuka LCD ditunjukkan dalam gambar 3-6. Dengan mengubah nilai V_{EE} menggunakan potensiometer P1 akan diperoleh tingkat

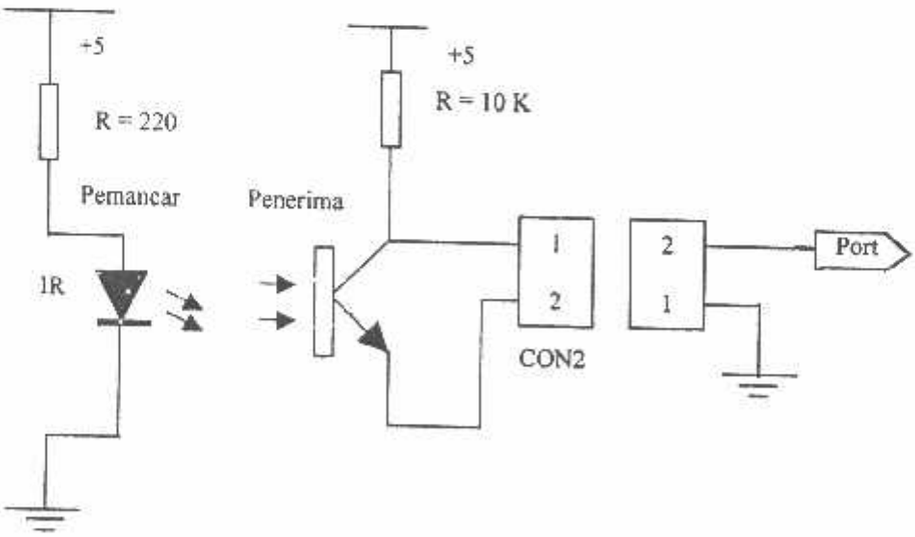
kecerahan yang berbeda pada tampilan LCD. Dioda D1 dipasang antara V_{cc} dan terminal BL+ untuk mencatu lampu latar tampilan LCD pada tegangan 4,3V. Bila LCD yang digunakan tanpa backlight, dioda tidak perlu dipasangkan



Gambar 3-5Rangkaian Antarmuka Modul LCD

3.2.3. Sensor Infra Merah

Untuk mengaktifkan Kapan kontrol akan bekerja adalah dengan menggunakan sensor infra merah sebagai pemancar dan Fhoto dioda sebagai penerimanya.



Gambar 3-6 Rangkaian Sensor Infra Merah

Dari gambar rangkaian infra merahdi atas, saat pemancar infra merah high memerlukan arus (I_{IR}) sebagai 20mA dan tegangan (V_{iR}) sebesar 1,2 volt sehingga dapat dihitung besarnya R_1 sebagai berikut :

$$R_1 = \frac{Vcc - V_{IR}}{I_{IR}}$$

$$= \frac{5 - 1,2}{20 \times 10^{-3}}$$

$$= 190 \text{ Ohm}$$

Dikarenakan sulit untuk mencari nilai resistor 190 ohm, maka dipilih harga resistor 220 ohm yang tersedia dipasaran.

Dan untuk nilai dari R_2 :

$$IC = 0,5.10^{-3} \text{ mA}$$

$$V_{CE\ SAT} = 0,1$$

$$- Vcc + Ic \,.\, Rc + V_{CE\ SAT} = 0$$

$$5 + 0,5.10^{-3} \,.\, Rc + 0,1 = 0$$

$$0,5\text{mA} \,.\, Rc = 5,1$$

$$Rc = \frac{5,1}{0,5}$$

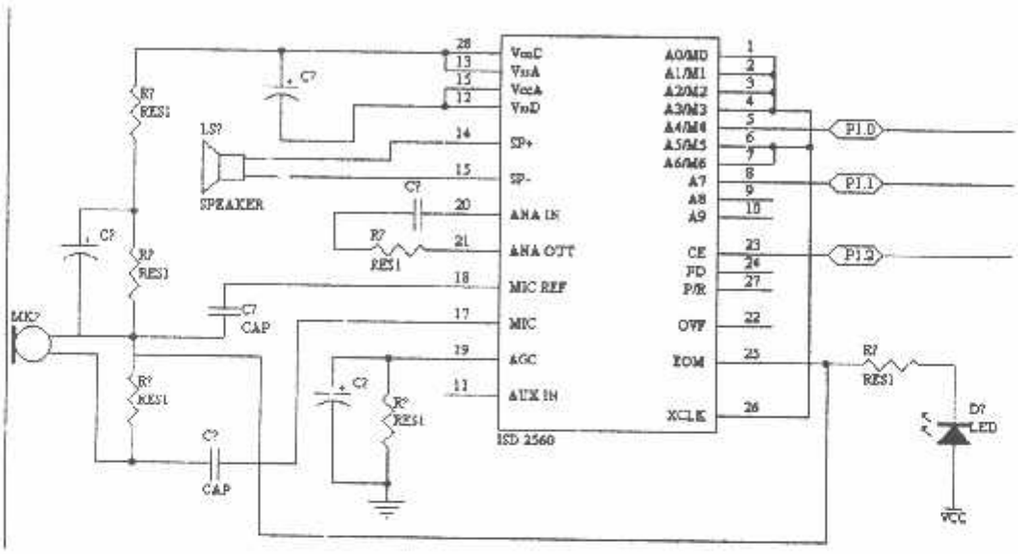
$$Rc = 10,2 \text{ K}$$

Dikarenakan sulit untuk mencari nilai resistor 10,2K, maka untuk R2 dipilih harga resistor 10K yang tersedia dipasaran.

3.2.4. IC Voice/Perekam ISD 1420P

Peralatan penyimpan informasi suara, ISD 1420P mempunyai kualitas yang

bagus, dengan durasi penyimpanan 60 detik Rangkaian alat dapat dilihat pada Gambar 3.4 di bawah ini:



Gambar 3-7 Rangkaian ISD 1420P

Peralatan CMOS yang ada didalamnya adalah *chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smouthing filter,* dan *speaker amplifier.* ISD 1420P adalah kompatibel dengan mikrokontroler. Alamat dan jalur kendali dapat di hubungkan dengan mikrokontroler, sehingga mengijinkan penyimpanan dan pengalamatan yang komplek. Perekaman disimpan dalam suatu *chip* yang tidak mudah berubah dalam *cell* memori. Sinyal suara audio disimpan secara langsung ke memori pada tempat naturalnya dengan kualitas suara yang bagus.

Dengan memanggil alamat-alamat data yang diinginkan maka terbetuk kalimat-kalimat dari penggalan-penggalan kata-kata yang sudah dialamati.

3.2.5 Perhitungan Pengkalibrasian (Jarak Tempuh)

Setiap motor memiliki ukuran roda yang berbeda-beda sesuai dengan jenis kendaraan .Disini saya memakai motor dua tak dimana diameter rodanya 53cm sehingga kita dapat mengetahui banyaknya putaran roda dalam jarak yang ditempuh

Diameter = 53cm

Keliling = 3,14 . 53 = 166,42 cm

Sehingga roda dalam satu putaran menempuh jarak 166,42cm atau 1,6642m

Sehingga dalam 3 putaran menempuh jarak

1,6642 . 3 = 4,9926 m dibulatkan menjadi 5 m

Dari perhitungan diatas maka kita peroleh untuk menghitung jumlah putaran dalam perhitungan penggantian oli dapat dihitung

- Untuk jarak tempuh 1500 km

  Jumlah putaran = (1500 km / 5). 3 = (1500.000 m /5). 3
  = 300.000 . 3 = 900.000putaran

- Untuk jarak tempuh 2000 km

  Jumlah putaran = (2000 km / 5). 3 = (2000.000m / 5). 3

  = 400.000 . 3 = 1200.000putaran

- Untuk jarak tempuh 2500 km

  Jumlah putaran = (2500 km / 5). 3 = (2500.000m / 5). 3

  = 500.000 . 3 = 1500.000putaran

Dari perhitungan diatas dalam pembuatan alat saya mengugunakan sekala 1 : 100.000

Sehingga dalam 3 putaran menempuh jarak 500 000m

Maka yang di peroleh dalam jarak tempuh 1500km

Jumlah putaran = (1500 km / 500km). 3 = (1500.000 m /500.000). 3
= 3 . 3 = 9putaran

Untuk jarak tempuh 2000 km

Jumlah putaran = (2000 km / 500km). 3 = (2000.000m / 500.000). 3

= 4 . 3 = 12putaran

Untuk jarak tempuh 2500 km

Jumlah putaran = (2500 km / 500km). 3 = (2500.000m / 500.000). 3

= 5 . 3 = 15putaran

Sehingga nilai erornya

- Untuk jarak 1500km

Jarak sebenarnya= 900.000 . 1,6642 = 1497780 m = 1497,78 km

Nilai eror = (1500.000 – 1497.780) . 100% / 1500.000

= 2220 . 100% / 1500.000 = 0,148 %

- Untuk jarak 2000km

Jarak sebenarnya = 1200.000 . 1,6642 = 1997.040m = 1997,04 km

Nilai eror = (2000.000 – 1997.040) . 100% / 2000.000

= 2960 . 100 % / 2000.000 = 0,148 %

- Untuk jarak 2500km

Jarak sebenarnya = 1500.000 . 1,6642 = 2496.300m = 2496,3km

Nilai eror = (2500.000 – 2496.300) . 100 % / 2500.000

= 3700 . 100 % / 2500.000 = 0,148

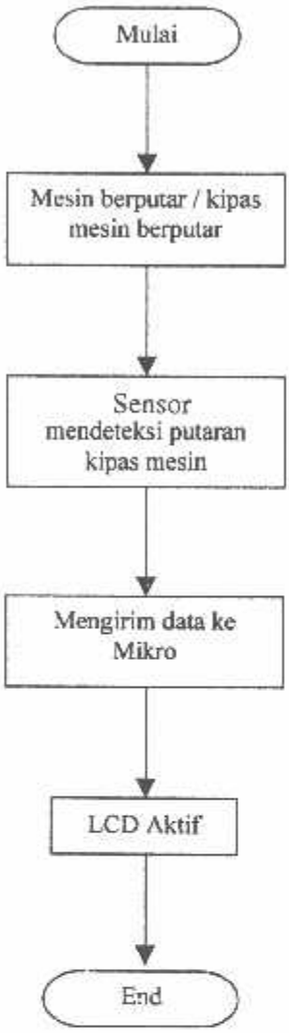
3.3 Perencanaan Perangkat Lunak / Software

Untuk pemakaian mikrokontroller di dalam suatu sistem, perlu direncanakan perangkat lunak mikrokontroler yang dapat mengatur system tersebut. Perangkat lunak disini adalah susunan perintah-perintah (program) di dalam memori yang harus dilaksanakan adalah mikrokontroler. Di dalam suatu mikrokontroler memori merupakan suatu fasilitas utama karena disinilah disimpan perintah-perintah yang harus dijalankan. Memori disini dapat dibedakan menurut fungsuinya menjadi memori program dan memori data.Mak perlu dibuat sebuah program yang mengendalikan setiap proses yang akan dilakukan oleh mikrokontroller . Metode yang digunakan dalam pembuatan perangkat lunak ini didasarkan pada studi Literatur dari buku-buku dan Literatur mikrokontroller Atmel 89S8252. Program (software) ditulis dengan sembarang pengolah kata (teks) dan disimpan dengan H51 atau ASM. Pembuatan perangkat lunak menggunakan teknik pengolahan dengan bahasa pemrograman *Assembly* dengan menggunakan konsep-konsep pemrograman yang efesien, selanjutnya dievaluasi dan di-download kedalam EPROM mikrokontroller 89S8252 menggunakan experimeter 89S8252.

Perencanaan perangkat lunak (software) didasarkan perencanaan perangkat keras yang telah dibuat sebelumnya, untuk mendapatkan system kerja yang diharapkan.

Gambar 3 – 9 Flowchart Putaran Mesin

(Rpm)



Gambar 3 – 9 Flowchart Putaran Mesin

(Rpm)

BAB IV

PENGUJIAN ALAT

Dalam bab ini akan dibahas tentang pengujian alat yang telah dibuat berdasarkan perencanaan dan pembuatan. Maksud dan tujuan pengujian alat ini adalah untuk mengetahui apakah alat yang telah direncanakan dan dibuat dapat bekerja dengan baik juga untuk mengetahui kerja dari masing-masing blok, sehingga dapat diketahui kepresisian kerja dari alat yang telah direncanakan secara umum , dari pengujian tersebut adalah sebagai berikut

1. Mengetahui proses kerja dari masing-masing rangkaian
2. Memudahkan spesifikasi alat
3. Memudahkan perawatan dan perbaikan apabilah sewaktu-waktu terjadi kerusakan

4.1. Pengujian Sensor Infra merah

- **Tujuan**

  Mengetahui tegangan pada sensor infra merah saat phototransistornya terkana dan tidak terkena sinar led.

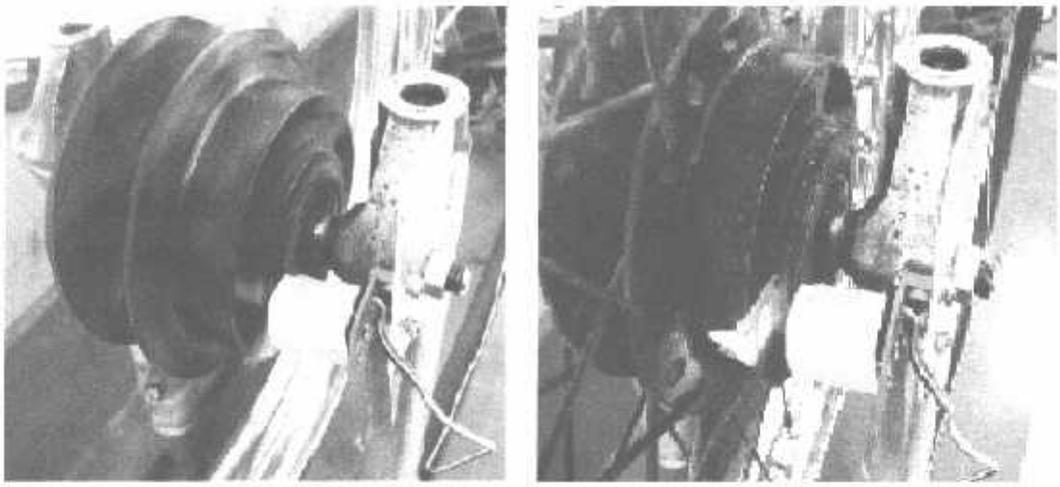
- **Alat dan Bahan**

  1. AVO meter digital
  2. Rangkaian sensor infra merah

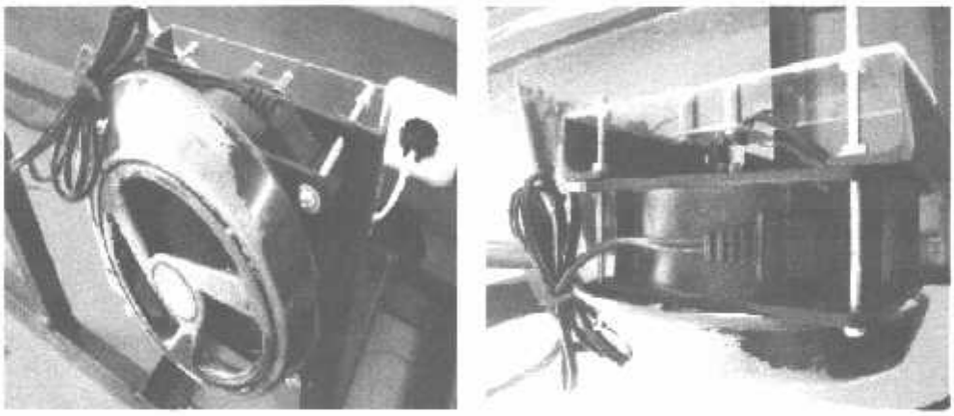
- **Langkah pengujian dan pengukuran**

  1. Mengaktifkan semua peralatan yang dibutuhkan.
  2. Mengukur tegangan sensor infra merah pada saat photo transistor terkena cahaya led.

3. Mengukur tegangan sensor infra merah pada saat photo transistor tidak terkena sinar led.



Gambar 4-1 sensor infra merah ditempatkan pada roda yang dipakai untuk jarak tempuh (*warning oil system*)



Gambar 4-2 sensor infra merah ditempatkan pada kipas mesin dipakai untuk menghitung banyaknya putaran mesin per menit (rpm)

- **Hasil Pengukuran**

  Hasil pengukuran pada sensor infra merah yang dipakai untuk jarak tempuh (*warning oil system*)

  Tegangan pada pemancar : 1,89 Volt

  Tegangan pada saat tidak terhalang : 5,04 Volt

  Tegangan pada saat terhalang : 0,131 Volt

Gambar 4-3 Pengukuran Tegangan

(saat sensor terhalang)

Gambar 4-4 Pengukuran Tegangan

(saat sensor tidak terhalang)

Hasil pengukuran pada sensor infra merah yang dipakai untuk menghitung banyaknya putaran mesin per menit (rpm)

Tegangan pada pemancar : 1,89 Volt

Tegangan pada saat tidak terhalang : 4,87 Volt

Tegangan pada saat terhalang : 3,6 Volt

Gambar 4-5 Pengukuran Tegangan

(saat sensor terhalang)

Gambar 4-6 Pengukuran Tegangan

(saat sensor tidak terhalang)

- **Analisa Hasil**

  Tegangan pada led sebagai pemancar sinar ataupun pada phototransistor dipengaruhi ketidak idealan komponen yang menyebabkan tegangan pada pemancar tidak bisa sesuai dengan perancangan alat. Walaupun tegangan pada phototransistor saat terkena sinar led tidak sebesar 5 volt ataupun pada saat tidak terkena sinar tidak bisa mencapai 0 volt, tetapi hal ini tidak mempengaruhi data pembacaan logika pada sensor infra merah. Pada saat tegangan bernilai 4,45 volt dan 4,67 volt, logika sensor inframerah adalah 1 dan berlogika 0 saat tegangan 3,24 volt dan 3,26 volt

4.2. Pengujian Penguat Sinyal

- **Tujuan**

  Untuk mengetahui besarnya penguat sinyal yang dikuatkan oleh rangkaian penguat sinyal

- **Peralatan yang digunakan**

  1. Power supply
  2. Rangkaian penguat sinyal
  3. AVO meter digital
  4. Kabel jepit buaya

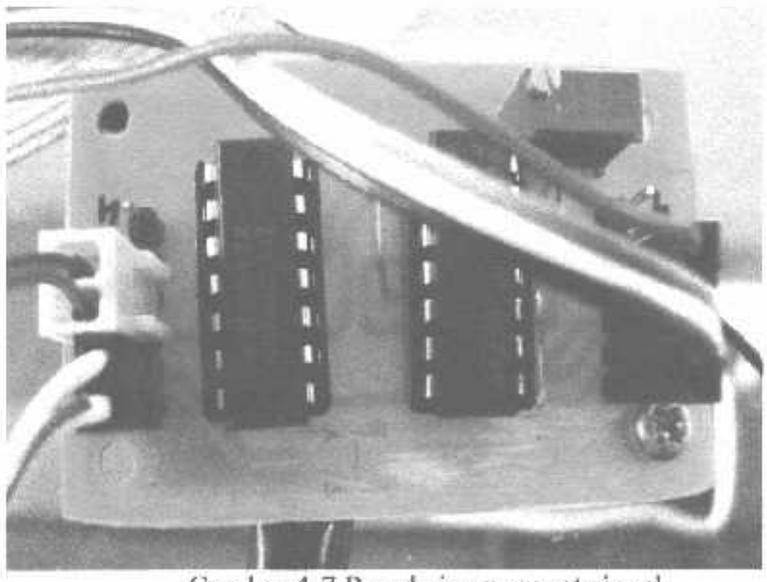
- **Hasil Pengujian**

Tabel 4-1 Hasil pengujian pada penguat sinyal untuk pengukuran jarak tempuh (*Warning oil system*)

Tegangan Input	Tegangan Output
3,24	0
4,45	5

Tabel 4-2 Hasil pengujian pada penguat sinyal untuk putaran mesin (rpm)

Tegangan Input	Tegangan Output
3,26	0
4,67	5



Gambar 4-7 Rangkaian penguat sinyal

- **Analisa Hasil**

  Dapat dilihat dari tabel diatas dari hasil pengukuran penguat yang dilakukan oleh rangkaian penghuat sinyal ini adalah dikisaran kurang dari empat adalah nol dan lebih dari empat adalah lima

4.3. Pengujian IC penyimpan Suara (ISD 1420P)

- **Tujuan**

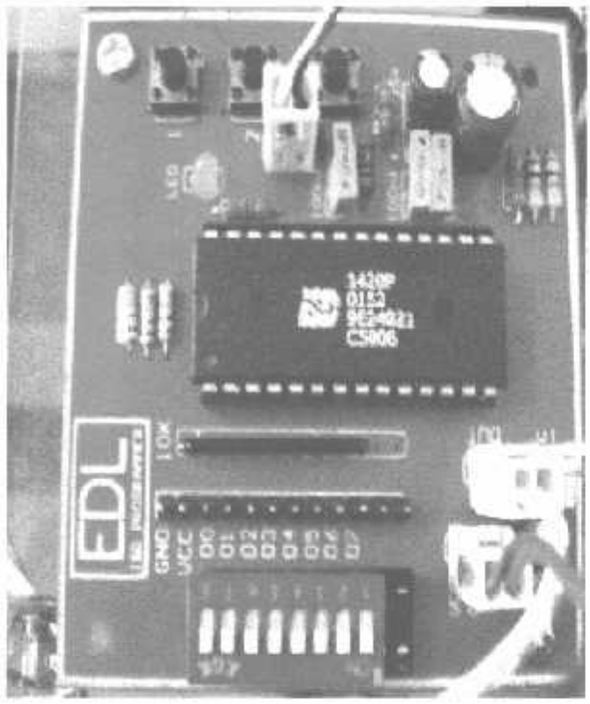
  Tujuan dari pengujian IC ini adalah untuk mengetahui apakah ISD 1420P bisa melakukan perekaman suara dengan baik ataukah tidak.

- **Langkah Pengujian**

  Lamanya perekama akan menentukan banyaknya alamat yang dipakai oleh ISD 1420P, semakin lama perekamannya maka alamat yang dipakai semakin banyak. Jika ISD 1420P dipakai untuk merekam suara lebih dari satu maka lamanya perekaman tidak boleh melebihi atau masuk pada alamat suara berikutnya ,karena suara yang telah direkam akan tergeser pada alamat berikutnya dan otomatis suara yang telah direkam akan terputus.

Tabel 4-3 Pemilihan alamat untuk merekam kata-kata

Alamat	Kata yang direkam
00000000 (0II)	Waktu penggantian oli



Gambar 4-8 Rangkaian ISD 1420P

- **Hasil Pengujian ISD 1420P**

  Dari hasil pengujian diperoleh hasil perekaman suara melalui sebuah speker apabila suara yang direkam dari mic condensor, berarti ISD telah bekerja dengan baik.

4.4. Pengujian Rangkaian Tampilan LCD

- **Tujuan**

  Untuk mengetahui kemampuan rangkaian tampilan yang sudah dibuat apakah dapat mendukung system yang direncanakan untuk menampilkan data pada LCD

- **Peralatan yang dibutuhkan untuk pengukuran**

  1. Tacho Meter

- **Hasil Pengukuran**

Hasil pengukuran dari Tacho meter digital dengan Tampilan LCD sebagai berikut:

HasilPengukuran (Rpm)	Tampilan LCD (Rpm)
2235	2230
1994	1990
1516	1510
1450	1441
1336	1330
1091	1090
912	910
761	760

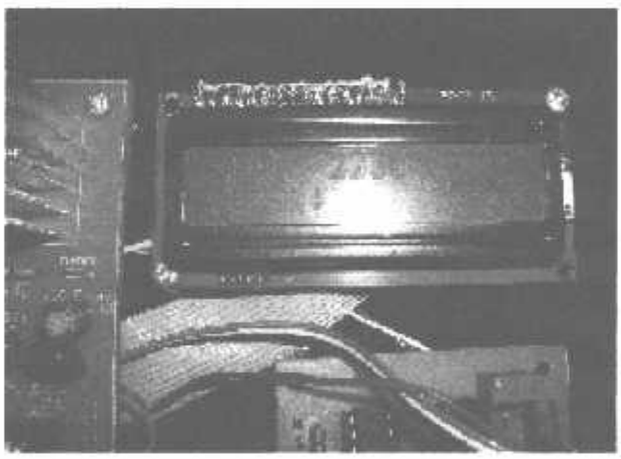
Sehingga kita peroleh nilai eror dari keseluruhan didapat:

Eror = (0,224 + 0,201 + 0,624 + 0,451 + 0,091+ 0,21 + 0,131) % / 8

= 1,932 / 8

= 0,2415 %

Gambar 4-9 Mengukur putaran Mesin (kipas mesin)



Gambar 4-10 Nilai yang ditampilkan LCD

- **Hasil dan Analisa**

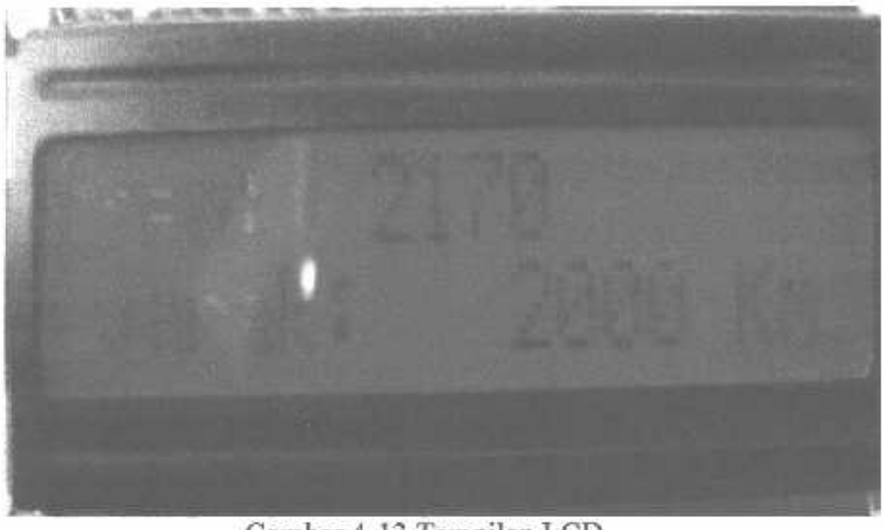
  Dari hasil pengujian dapat dilihat bahwa rangkaian tampilan dapat bekerja dengan baik

Gambar 4-11 Tampilan LCD

dengan tiga pilihan jarak tempuh untuk penggantian oli

Gambar 4-12 Tampilan LCD

Dengan jarak tempuh 1500 Km untuk penggantian oli



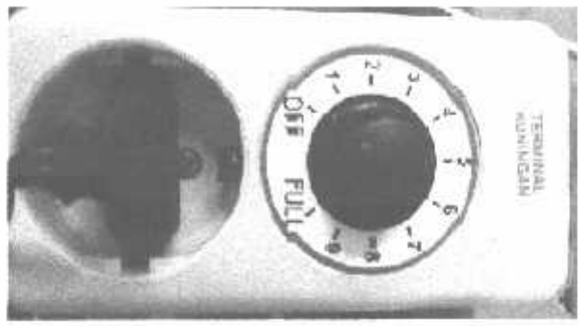
Gambar 4-13 Tampilan LCD

Dengan jarak tempuh 2000 Km untuk penggantian oli

Gambar 4-14 Tampilan LCD

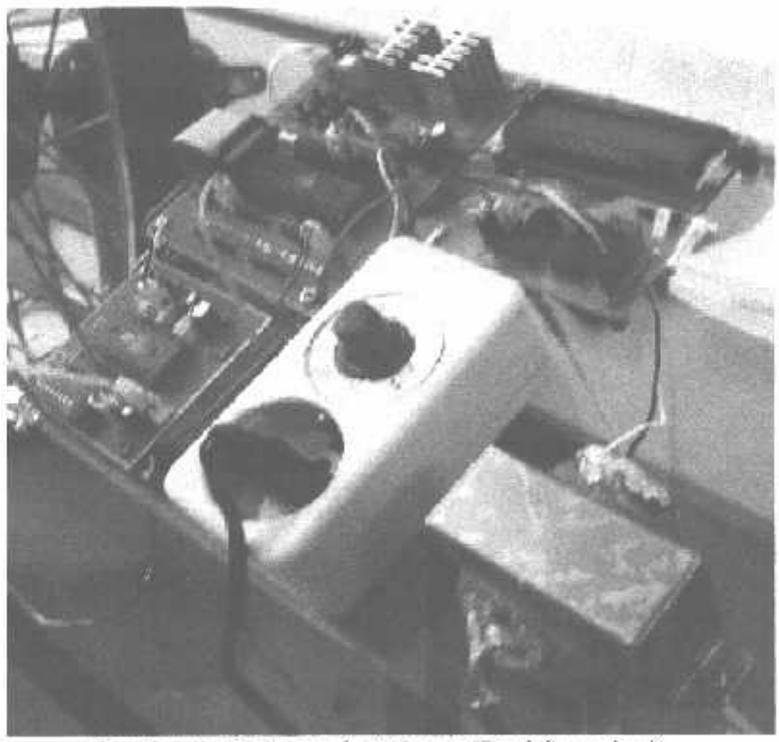
Dengan jarak tempuh 2500 Km untuk penggantian oli

4.5. Gambar Alat Serta Alat Pendukungnya

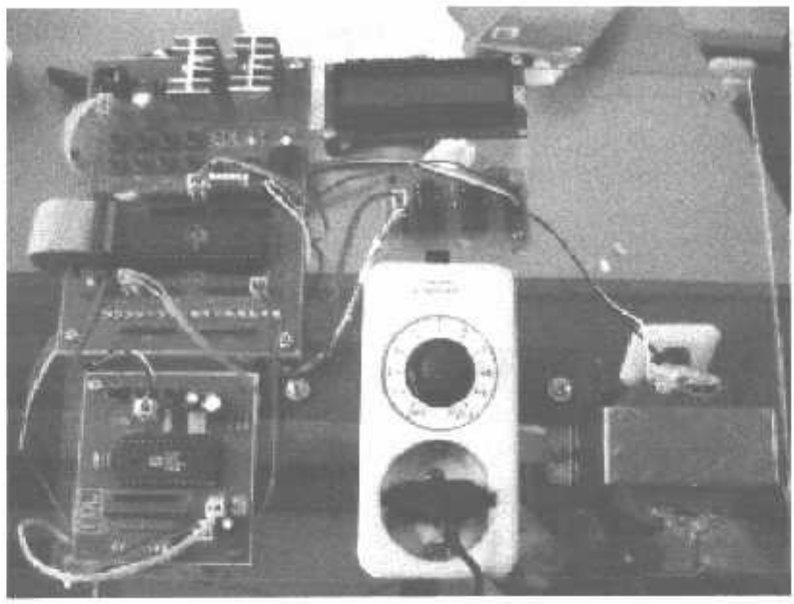


Gambar 4-15 Power Kontrol

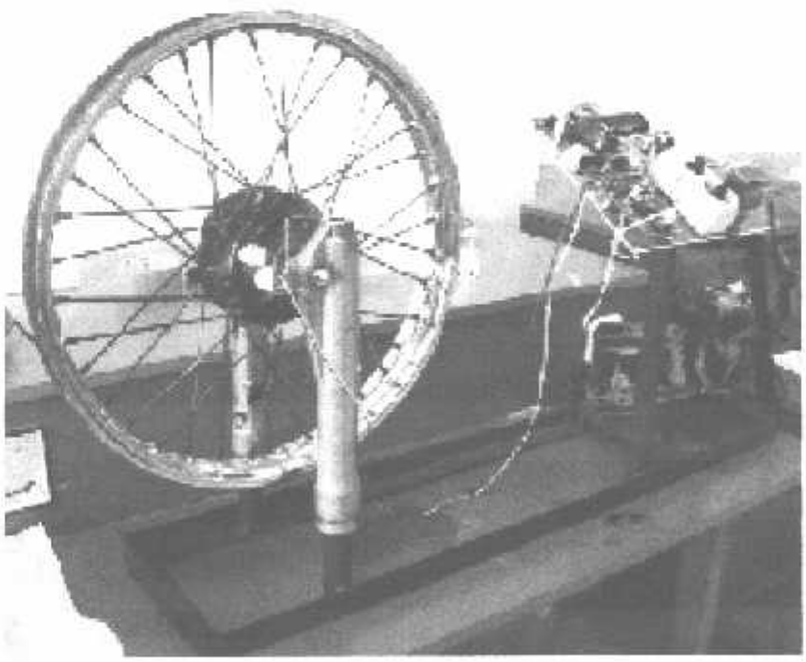
Sebagai pengatur kecepatan Mesin (kipas mesin)



Gambar 4-16 Perangkat Keras (Dari Samping)



Gambar 4-17 Perangkat Keras (Dari Depan)



Gambar4-18 Alat Keseluruhan

Spesifikasi :

1. Ukuran alat dengan panjang $\pm$ 1 meter.
2. Dengan lebar alat $\pm$ 21,5 cm.
3. Dengan tinggi alat $\pm$ 58 cm.
4. Memakai tegangan sebesar 5 Volt, dengan tampilan LCD 162A dan rekaman suara sebagai peringatan (ISD 1420P).
5. Dengan tiga tombol pilihan sebagai pilihan untuk jarak tempuh penggantian oli.
   - Pilihan 1 dengan jarak tempuh 1500 Km untuk penggantian oli.
   - Pilihan 2 dengan jarak tempuh 2000 Km untuk penggantian oli.
   - Pilihan 3 dengan jarak tempuh 2500 Km untuk penggantian oli.
6. Setelah penggantian oli tekan tombol *restart* terlebih dahulu, setelah itu baru memilih tombol pilihan sesuai keinginannya serta disesuaikan dengan kondisi dan mutu oli yang akan dipakainya.
7. Dalam tampilan LCD disertai dengan putaran mesin (RPM).
8. Suara peringatan akan berbunyi saat mencapai jarak yang ditempuh (jarak tempuh yang dipilih).

BAB V

KESIMPULAN DAN SARAN

5.1. Kesimpulan

Dari hasil perancangan dan pembuatan *automatic warning oil system dan* kecepatan putaran mesin pada sepeda motor berbasis mikrokontroller AT89S8252, maka dapat disimpulkan sebagai berikut :

- Rangkaian Liquit Crystal Display (LCD) digunakan untuk menampilkan perhitungan putaran mesin (rpm) waktu mesin hidup dan jarak tempuh waktu kendaraan mulai start.
- Hasil pengujian menunjukkan bahwa alat mampu bekerja dengan baik yaitu dengan menampilkan jarak tempuh kendaraan dan jumlah putaran mesin (rpm).
- Nilai jarak tempuh dengan jarak sesunggunya memiliki nilai selisi 0,148 % dan untuk jumlah putaran mesi (rpm) yang ditampilkan oleh LCD dengan pengukuran memiliki selisih 0,2415 %
- Bahwa suara yang tersimpan dalam ISD dapat dikeluarkan setelah suara diisi terlebih dahulu dengan modul ISD.
- Suara keluaran dari speker yang dihasilkan sesuai dengan keinginan , sehingga diharapkan bisa menjadi pengingat kepada pemakai kendaraan.

5.2 Saran

- Saat penggantian oli kita bisa memeriksa tingkat kekentalan oli dimana tingkat kekentalan oli diatas jauh dari ukuran standatnya oli yang baru.
- Dilihat dari warna oli yang jelek warnanya sangat hitam apalagi mengandung gram besi harus segera menggantinya karena dapatmengakibatkan kerusakan pada silinder mesin dan bagian lainnya.
- Oli yang baik harus memiliki daya kepekatan yang bagus terutama dalam suhu yang tinggi , bila dalam suhu 100 ^{0}C kondisi oli harus memiliki daya kepekatan yang hampir sama dengan kondisi biasa . Dari kondisi suhu yang panas kita bisa mengetahui adanya unsur-unsur lain atau oli palsu karena dalam keadaan panas oli tersebut kekentalannya akan cepat berubah tidak sesuai dengan kondisi semula.
- Dalam rancang bangun suatu peralatan hendaknya direncanakan secara matang dengan memperhatikan keterbatasan ,ketrampilan dan pengalaman yang dimiliki serta peranan dan prasarana yang dibutuhkan.
- Sebaiknya pada sensor diberi kotak pelindung agar tidak terkena sinar matahari karena mempengaruhi pada sensitifitas sensornya.
- Dalam pengoperasian alat hendaknya diperhatikan cara pengoperasian yang benar karena akan memberikan hasil yang maksimal sesuai dengan yang diharapkan.

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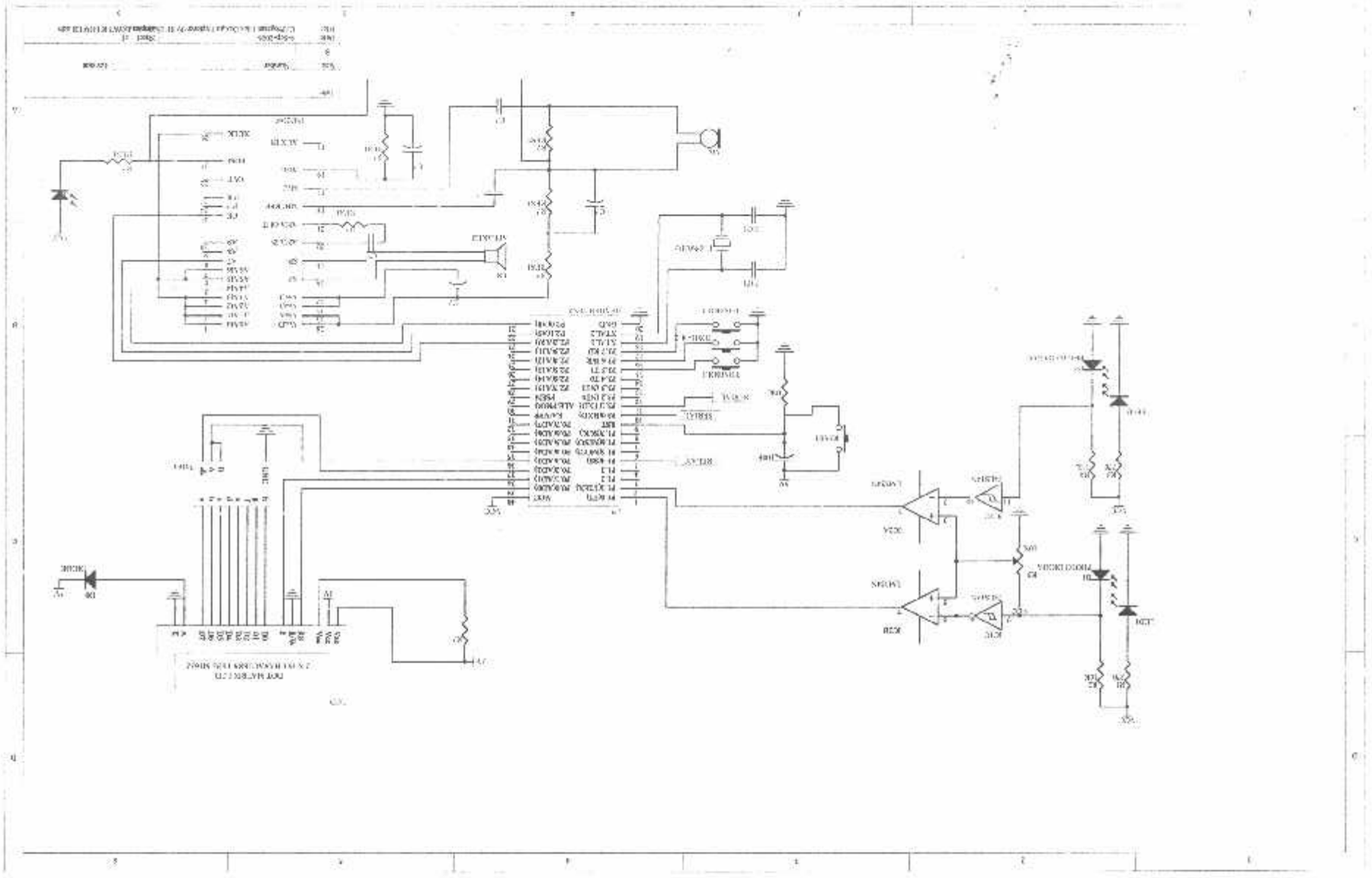
LAMPIRAN



INSTITUT TEKNOLOGI NASIONAL MALANG
JL. Bendungan Sigura-gura No.2
Malang

LEMBAR BIMBINGAN SKRIPSI

1. Nama : AGUS HARDIYANTO
2. Nim : 01.17.067
3. Jurusan : Teknik Elektro (S-1)
4. Konsentrasi : Teknik Elektronika
5. Judul Skripsi : **PERANCANGAN DAN PEMBUATAN AUTOMATIC WARNING OIL SYSTEM DAN KECEPATAN PUTARAN MESIN PADA SEPEDA MOTOR BERBASIS MIKROKONTROLLER AT 89S8252**
6. Tanggal Pengajuan Skripsi : 27 Juli 2006
7. Selesai Menulis Skripsi : 2 Oktober 2006
8. Dosen Pembimbing : Ir. Eko Nurcahyo
9. Telah Dievaluasi Dengan Nilai : 80

Mengetahui Ketua Jurusan Teknik Elektro S-1	Diperiksa dan disetujui Dosen Pembimbing
Ir. F. Yudi Limpraptono, MT. NIP. Y. 1039500274	Ir. Eko Nurcahyo NIP. Y. 1028700172

JL. Bendungan Sigura-gura No. 2
MALANG

FORMULIR BIMBINGAN SEKRIPSI

Nama : AGUS HARDIYANTO
Nim : 0117067
Masa Bimbingan : 27 Juli 2006 s/d 27 Januari 2007
Judul Sekripsi : **Perancangan Dan Pembuatan Automatic *Warning Oil Sytem* dan Kecepatan Putaran Mesin Pada Sepeda Motor Berbasis Mikrokontroler AT89S8252**

NO	Tanggal	Uraian	Paraf Pembibing
1	4-08-06	BAB I. perbaiki latar belakang masalah.	
2	6-08-06	Acc BAB I,	
3	18-08-06	Acc BAB II, tambahkan teori	
4	23-08-06	BAB II, perbaiki teori.	
5	28-08-06	Acc BAB III.	
6	31-08-06	BAB IV, foto alat	
7	02-09-06	Acc BAB IV & BAB V	
8	07-09-06	Acc maju Seminar hasil	
9			
10			

Malang, - - 2007
Dosen Pembibing

Ir.Eko Nurcahyo

From S-4

INSTITUT TEKNOLOGI NASIONAL MALANG
JL. Bendungan Sigura-gura No.2
Malang

FORMULIR PERBAIKAN SKRIPSI

Dari hasil ujian skripsi jenjang strata satu (S-1) Jurusan Teknik Elektro konsentrasi Elektronika yang diselenggarakan pada :

1. Nama Mahasiswa : AGUS HARDIYANTO
2. Nim : 01.17.067
3. Jurusan : Teknik Elektro S-1
4. Konsentrasi : Teknik Elektronika
5. Judul Skripsi : **PERANCANGAN DAN PEMBUATAN AUTOMATIC WARNING OIL SYSTEM DAN KECEPATAN PUTARAN MESIN PADA SEPEDA MOTOR BERBASIS MIKROKONTROLLER AT 89S8252**

Perbaikan Meliputi

NO	Materi Perbaikan	Keterangan
1	LED Infra Merah !	
2	Kekentalan	
3	Warna yang telah mengandung gram besi	
4	Suhu lamanya beroperasi dan unsur ^{2} lain oli di pertamina / di toko-toko	
5	Spesifikasi infra yang dipakai	

Disetujui

Penguji I

Ir. Usman Djuanda, MM
NIP. 1018700143

Penguji II

Sotyohadi, ST. MSC

Mengetahui
Dosen Pembimbing

Ir. Eko Nurcahyo
NIP. Y. 1028700172

```
org 00h

sensor_rpm      bit     P3.1
sensor_jarak    bit     P3.0
data_rpm        equ     20h
data_jarak      equ     22h

        mov     data_jarak,#0
mulai:
        mov     TMOD,#01h
        mov     data_rpm,#0

rpm:
        mov     r0,#20
time1:
        mov     th0,#03ch
        mov     tl0,#0b0h
        setb    tr0
ulang:
        jnb     sensor_rpm,counter_up_rpm
loop:   jnb     sensor_jarak,counter_up_jarak
        jnb     tf0,ulang
        clr     tr0
        clr     tf0


        djnz    r0,time1
        mov     p0,data_rpm
        mov     p2,data_jarak

        jmp     mulai
; data rpm disimpan di data_rpm
counter_up_rpm:
        jnb     sensor_rpm,$
        inc     data_rpm
        jmp     ulang

counter_up_jarak:
        jnb     sensor_jarak,$
        inc     data_jarak

        jmp     loop



end
```

```
org 00h
awal:
sensor_rpm      bit     P3.1
sensor_jarak    bit     P3.0
rs              bit     p2.6
cs              bit     p2.7
eoc             bit     p2.1
play            bit     p2.0
data_lcd        equ     p0
data_rpm        equ     20h
data_jarak      equ     22h
        setb    eoc
        setb    play
        mov     TMOD,#01h
        mov     data_jarak,#0
        call    inisial_3
        mov     dptr,#pilihan
        call    x5
        mov     dptr,#pilihan2
        call    x6
tombol1: jb     p3.7,tombol2
         sjmp   mulai
tombol2: jb     p3.6,tombol3
         sjmp   mulai2
tombol3: jb     p3.5,tombol1
         sjmp   mulai3

;-------------------------------------------------
mulai:  mov     data_rpm,#0
        mov     r0,#20
time1:  mov     th0,#03ch
        mov     tl0,#0b0h
        setb    tr0
ulang:  jnb     sensor_rpm,counter_up_rpm
loop:   jnb     sensor_jarak,counter_up_jarak
        jnb     tf0,ulang
        clr     tr0
        clr     tf0
        djnz    r0,time1
        call    bandingkan_rpm
        mov     a,data_jarak
        call    bandingkan_jarak
        jmp     mulai
counter_up_rpm:
        jnb     sensor_rpm,$
        inc     data_rpm
        jmp     ulang
counter_up_jarak:
        jnb     sensor_jarak,$
        inc     data_jarak
        call    bandingkan_jarak
        jmp     loop
;-------------------------------------------------
mulai2: mov     data_rpm,#0
        mov     r0,#20
time2:  mov     th0,#03ch
        mov     tl0,#0b0h
        setb    tr0
ulang2: jnb     sensor_rpm,counter_up_rpm2
loop2:  jnb     sensor_jarak,counter_up_jarak2
        jnb     tf0,ulang2
        clr     tr0
        clr     tf0
        djnz    r0,time2
        call    bandingkan_rpm
        mov     a,data_jarak
        call    bandingkan_jarak2
```

```
        jmp     mulai2
counter_up_rpm2:
        jnb     sensor_rpm,$
        inc     data_rpm
        jmp     ulang2
counter_up_jarak2:
        jnb     sensor_jarak,$
        inc     data_jarak
        call    bandingkan_jarak2
        jmp     loop2
;-------------------------------------------------------
mulai3: mov     data_rpm,#0
        mov     r0,#20
time3:  mov     th0,#03ch
        mov     tl0,#0b0h
        setb    tr0
ulang3: jnb     sensor_rpm,counter_up_rpm3
loop3:  jnb     sensor_jarak,counter_up_jarak3
        jnb     tf0,ulang3
        clr     tr0
        clr     tf0
        djnz    r0,time3
        call    bandingkan_rpm
        mov     a,data_jarak
        call    bandingkan_jarak3
        jmp     mulai3
counter_up_rpm3:
        jnb     sensor_rpm,$
        inc     data_rpm
        jmp     ulang3
counter_up_jarak3:
        jnb     sensor_jarak,$
        inc     data_jarak
        call    bandingkan_jarak3
        jmp     loop3


;=====================================
;perbandigan rpm
;=====================================
bandingkan_rpm: call    inisial

        mov     a,data_rpm
rpm1:   cjne    a,#2ah,rpm2
        call    lcd_1
        sjmp    rpm2
rpm2:   cjne    a,#29h,rpm3
        call    lcd_2
        jmp     rpm3
rpm3:   cjne    a,#28h,rpm4
        call    lcd_3
        sjmp    rpm4
rpm4:   cjne    a,#27h,rpm5
        call    lcd_4
        sjmp    rpm5
rpm5:   cjne    a,#26h,rpm6
        call    lcd_5
        sjmp    rpm6
rpm6:   cjne    a,#25h,rpm7
        call    lcd_6
        sjmp    rpm7
rpm7:   cjne    a,#24h,rpm8
        call    lcd_7
        jmp     rpm8
rpm8:   cjne    a,#23h,rpm9
        call    lcd_8
```

```
        sjmp    rpm9
rpm9:   cjne    a,#22h,rpm10
        call    lcd_9
        sjmp    rpm10
rpm10:  cjne    a,#21h,rpm11
        call    lcd_10
        sjmp    rpm11
rpm11:  cjne    a,#20h,rpm12
        call    lcd_11
        sjmp    rpm12
rpm12:  cjne    a,#1fh,rpm13
        call    lcd_12
        jmp     rpm13
rpm13:  cjne    a,#1eh,rpm14
        call    lcd_13
        sjmp    rpm14
rpm14:  cjne    a,#1dh,rpm15
        call    lcd_14
        sjmp    rpm15
rpm15:  cjne    a,#1ch,rpm16
        call    lcd_15
        sjmp    rpm16
rpm16:  cjne    a,#1bh,rpm17
        call    lcd_16
        sjmp    rpm17
rpm17:  cjne    a,#1ah,rpm18
        call    lcd_17
        jmp     rpm18
rpm18:  cjne    a,#19h,rpm19
        call    lcd_18
        sjmp    rpm19
rpm19:  cjne    a,#18h,rpm20
        call    lcd_19
        sjmp    rpm20
rpm20:  cjne    a,#17h,rpm21
        call    lcd_20
        sjmp    rpm21
rpm21:  cjne    a,#16h,rpm22
        call    lcd_21
        sjmp    rpm22
rpm22:  cjne    a,#15h,rpm23
        call    lcd_22
        jmp     rpm23
rpm23:  cjne    a,#14h,rpm24
        call    lcd_23
        sjmp    rpm24
rpm24:  cjne    a,#13h,rpm25
        call    lcd_24
        sjmp    rpm25
rpm25:  cjne    a,#12h,rpm26
        call    lcd_25
        sjmp    rpm26
rpm26:  cjne    a,#11h,rpm27
        call    lcd_26
        sjmp    rpm27
rpm27:  cjne    a,#10h,rpm28
        call    lcd_27
        jmp     rpm28
rpm28:  cjne    a,#0ah,rpm29
        call    lcd_27
        sjmp    rpm29
rpm29:  cjne    a,#0fh,rpm30
        call    lcd_28
        sjmp    rpm30
rpm30:  cjne    a,#0eh,rpm31
        call    lcd_29
        sjmp    rpm31
```

```
rpm31:  cjne    a,#0dh,rpm32
        call    lcd_30
        sjmp    rpm32
rpm32:  cjne    a,#0ch,rpm33
        call    lcd_31
        jmp     rpm33
rpm33:  cjne    a,#0bh,rpm34
        call    lcd_32
        sjmp    rpm34
rpm34:  cjne    a,#0ah,rpm35
        call    lcd_33
        sjmp    rpm35
rpm35:  cjne    a,#09h,rpm36
        call    lcd_34
        sjmp    rpm36
rpm36:  cjne    a,#08h,rpm37
        call    lcd_35
        sjmp    rpm37
rpm37:  cjne    a,#07h,rpm38
        call    lcd_36
        jmp     rpm38
rpm38:  cjne    a,#06h,rpm39
        call    lcd_37
        sjmp    rpm39
rpm39:  cjne    a,#05h,rpm40
        call    lcd_38
        sjmp    rpm40
rpm40:  cjne    a,#04h,rpm41
        call    lcd_39
        sjmp    rpm41
rpm41:  cjne    a,#03h,rpm42
        call    lcd_40
        sjmp    rpm42
rpm42:  cjne    a,#02h,rpm43
        call    lcd_41
        sjmp    rpm43
rpm43:  cjne    a,#01h,rpm44
        call    lcd_42
        sjmp    rpm44
rpm44:  cjne    a,#00h,rpm45
        call    lcd_43
        sjmp    rpm45
rpm45:  ret

;=========================================
;penulisan LCD rpm
;=========================================
lcd_1:  ;call   inisial
        mov     dptr,#tulis_rpm_1
        call    x2
        ret
lcd_2:  ;call   inisial
        mov     dptr,#tulis_rpm_2
        call    x2
        ret
lcd_3:  ;call   inisial
        mov     dptr,#tulis_rpm_3
        call    x2
        ret
lcd_4:  ;call   inisial
        mov     dptr,#tulis_rpm_4
        call    x2
        ret
lcd_5:  ;call   inisial
        mov     dptr,#tulis_rpm_5
        call    x2
        ret
```

```
lcd_6:  ;call   inisial
        mov     dptr,#tulis_rpm_6
        call    x2
        ret
lcd_7:  ;call   inisial
        mov     dptr,#tulis_rpm_7
        call    x2
        ret
lcd_8:  ;call   inisial
        mov     dptr,#tulis_rpm_8
        call    x2
        ret
lcd_9:  ;call   inisial
        mov     dptr,#tulis_rpm_9
        call    x2
        ret
lcd_10: ;call   inisial
        mov     dptr,#tulis_rpm_10
        call    x2
        ret
lcd_11: ;call   inisial
        mov     dptr,#tulis_rpm_11
        call    x2
        ret
lcd_12: ;call   inisial
        mov     dptr,#tulis_rpm_12
        call    x2
        ret
lcd_13: ;call   inisial
        mov     dptr,#tulis_rpm_13
        call    x2
        ret
lcd_14: ;call   inisial
        mov     dptr,#tulis_rpm_14
        call    x2
        ret
lcd_15: ;call   inisial
        mov     dptr,#tulis_rpm_15
        call    x2
        ret
lcd_16: ;call   inisial
        mov     dptr,#tulis_rpm_16
        call    x2
        ret
lcd_17: ;call   inisial
        mov     dptr,#tulis_rpm_17
        call    x2
        ret
lcd_18: ;call   inisial
        mov     dptr,#tulis_rpm_18
        call    x2
        ret
lcd_19: ;call   inisial
        mov     dptr,#tulis_rpm_19
        call    x2
        ret
lcd_20: ;call   inisial
        mov     dptr,#tulis_rpm_20
        call    x2
        ret
lcd_21: ;call   inisial
        mov     dptr,#tulis_rpm_21
        call    x2
        ret
lcd_22: ;call   inisial
        mov     dptr,#tulis_rpm_22
        call    x2
```

```
        ret
lcd_23: ;call   inisial
        mov     dptr,#tulis_rpm_23
        call    x2
        ret
lcd_24: ;call   inisial
        mov     dptr,#tulis_rpm_24
        call    x2
        ret
lcd_25: ;call   inisial
        mov     dptr,#tulis_rpm_25
        call    x2
        ret
lcd_26: ;call   inisial
        mov     dptr,#tulis_rpm_26
        call    x2
        ret
lcd_27: ;call   inisial
        mov     dptr,#tulis_rpm_27
        call    x2
        ret
lcd_28: ;call   inisial
        mov     dptr,#tulis_rpm_28
        call    x2
        ret
lcd_29: ;call   inisial
        mov     dptr,#tulis_rpm_29
        call    x2
        ret
lcd_30: ;call   inisial
        mov     dptr,#tulis_rpm_30
        call    x2
        ret
lcd_31: ;call   inisial
        mov     dptr,#tulis_rpm_31
        call    x2
        ret
lcd_32: ;call   inisial
        mov     dptr,#tulis_rpm_32
        call    x2
        ret
lcd_33: ;call   inisial
        mov     dptr,#tulis_rpm_33
        call    x2
        ret
lcd_34: ;call   inisial
        mov     dptr,#tulis_rpm_34
        call    x2
        ret
lcd_35: ;call   inisial
        mov     dptr,#tulis_rpm_35
        call    x2
        ret
lcd_36: ;call   inisial
        mov     dptr,#tulis_rpm_36
        call    x2
        ret
lcd_37: ;call   inisial
        mov     dptr,#tulis_rpm_37
        call    x2
        ret
lcd_38: ;call   inisial
        mov     dptr,#tulis_rpm_38
        call    x2
        ret
lcd_39: ;call   inisial
        mov     dptr,#tulis_rpm_39
```

```
        call    x2
        ret
lcd_40: ;call   inisial
        mov     dptr,#tulis_rpm_40
        call    x2
        ret
lcd_41: ;call   inisial
        mov     dptr,#tulis_rpm_41
        call    x2
        ret
lcd_42: ;call   inisial
        mov     dptr,#tulis_rpm_42
        call    x2
        ret
lcd_43: ;call   inisial
        mov     dptr,#tulis_rpm_43
        call    x2
        ret
;=======================================
;perbandigan jarak
;=======================================
bandingkan_jarak: call inisial_2
        mov     a,data_jarak
jarak1: cjne    a,#0,jarak2
        call    lcd_jarak_1
        sjmp    jarak2
jarak2: cjne    a,#1,jarak3
        call    lcd_jarak_2
        sjmp    jarak3
jarak3: cjne    a,#2,jarak4
        call    lcd_jarak_3
        sjmp    jarak4
jarak4: cjne    a,#3,jarak5
        call    lcd_jarak_4
        clr     play
        jb      eoc,$
        jb      p3.4,$
        call    delay
        call    delay
        call    delay
        ljmp    awal

jarak5: ret
;-----------------------------------------
bandingkan_jarak2: call inisial_2
        mov     a,data_jarak
jarak6: cjne    a,#0,jarak8
        call    lcd_jarak_1
        sjmp    jarak8
jarak8: cjne    a,#1,jarak10
        call    lcd_jarak_2
        sjmp    jarak10
jarak10: cjne   a,#2,jarak11
        call    lcd_jarak_3
        sjmp    jarak11
jarak11:cjne    a,#3,jarak12
        call    lcd_jarak_4
        sjmp    jarak12
jarak12:cjne    a,#4,jarak13
        call    lcd_jarak_5
        clr     play
        jb      eoc,$
        jb      p3.4,$
        call    delay
        call    delay
        call    delay
        ljmp    awal
```

```
jarak13: ret
;---------------------------------------
bandingkan_jarak3: call inisial_2
        mov     a,data_jarak
jarak16:cjne    a,#0,jarak17
        call    lcd_jarak_1
        sjmp    jarak17
jarak17:cjne    a,#1,jarak18
        call    lcd_jarak_2
        sjmp    jarak18
jarak18:cjne    a,#2,jarak19
        call    lcd_jarak_3
        sjmp    jarak19
jarak19:cjne    a,#3,jarak20
        call    lcd_jarak_4
        sjmp    jarak20
jarak20:cjne    a,#4,jarak21
        call    lcd_jarak_5
        sjmp    jarak21
jarak21:cjne    a,#5,jarak22
        call    lcd_jarak_6
        clr     play
        jb      eoc,$
        jb      p3.4,$
        call    delay
        call    delay
        call    delay
        ljmp    awal
jarak22: ret


;=======================================
;penulisan LCD jarak
;=======================================
lcd_jarak_1:    ;call   inisial_2
                mov     dptr,#tulis_jarak_1
                call    x3
                ret
lcd_jarak_2:    ;call   inisial_2
                mov     dptr,#tulis_jarak_2
                call    x3
                ret
lcd_jarak_3:    ;call   inisial_2
                mov     dptr,#tulis_jarak_3
                call    x3
                ret
lcd_jarak_4:    ;call   inisial_2
                mov     dptr,#tulis_jarak_4
                call    x3
                ret
lcd_jarak_5:    ;call   inisial_2
                mov     dptr,#tulis_jarak_5
                call    x3
                ret
lcd_jarak_6:    ;call   inisial_2
                mov     dptr,#tulis_jarak_6
                call    x3
                ret
;=======================================
;inisial lcd semua
;=======================================
x1:     clr     a
        movc    a,@a+dptr
        inc     dptr
        call    tulis
        djnz    r3,x1
        ret
```

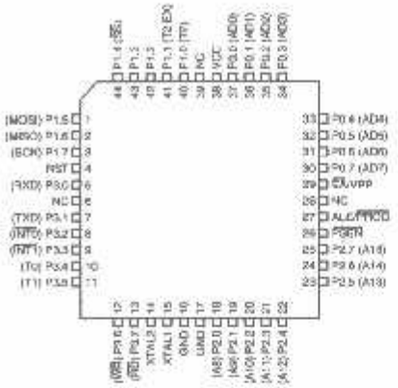
```
x2:     mov     r3,#10
        mov     a,#80h
        call    instruksi
        call    x1
        ret
x3:     mov     r4,#16
        mov     a,#0c0h
        call    instruksi
        call    x4
        ret
x4:     clr     a
        movc    a,@a+dptr
        inc     dptr
        call    tulis
        djnz    r4,x4
        ret

x5:     mov     r4,#16
        mov     a,#80h
        call    instruksi
        call    x4
        ret
x6:     mov     r4,#16
        mov     a,#0c0h
        call    instruksi
        call    x4
        ret

inisial: mov    a,#3fh
         call   instruksi
         mov    a,#00001100b
         call   instruksi
         mov    a,#01h
         call   instruksi
         ret
inisial_2: mov  a,#3fh
           call instruksi
           mov  a,#00001100b
           call instruksi
           ;mov 18h,#01h
           ;call        instruksi
           ret
inisial_3: mov  a,#3fh
           call instruksi
           mov  a,#0dh
           call instruksi
           mov  a,#01h
           call instruksi
           ret
instruksi:
        clr     rs
        setb    cs
        mov     data_lcd,a
        clr     cs
        setb    cs
        call    delay
        ret
Tulis:
        setb    rs
        setb    cs
        mov     data_lcd,a
        clr     cs
        setb    cs
        call    delay
        ret
;====================================
;delay
```

```
;=====================================
delay:  mov     r1,#45
delay1: mov     r2,#10
        djnz    r2,$
        djnz    r1,delay1
        ret
;=======================================
;data base rpm
;=======================================
tulis_rpm_1: db 'rpm:  2530'
tulis_rpm_2: db 'rpm:  2470'
tulis_rpm_3: db 'rpm:  2410'
tulis_rpm_4: db 'rpm:  2350'
tulis_rpm_5: db 'rpm:  2290'
tulis_rpm_6: db 'rpm:  2230'
tulis_rpm_7: db 'rpm:  2170'
tulis_rpm_8: db 'rpm;  2110'
tulis_rpm_9: db 'rpm:  2050'
tulis_rpm_10: db 'rpm:  1990'
tulis_rpm_11: db 'rpm:  1930'
tulis_rpm_12: db 'rpm:  1870'
tulis_rpm_13: db 'rpm:  1810'
tulis_rpm_14: db 'rpm:  1750'
tulis_rpm_15: db 'rpm:  1690'
tulis_rpm_16: db 'rpm:  1630'
tulis_rpm_17: db 'rpm:  1570'
tulis_rpm_18: db 'rpm:  1510'
tulis_rpm_19: db 'rpm:  1450'
tulis_rpm_20: db 'rpm:  1390'
tulis_rpm_21: db 'rpm:  1330'
tulis_rpm_22: db 'rpm:  1270'
tulis_rpm_23: db 'rpm:  1210'
tulis_rpm_24: db 'rpm:  1150'
tulis_rpm_25: db 'rpm:  1090'
tulis_rpm_26: db 'rpm:  1030'
tulis_rpm_27: db 'rpm:  0970'
tulis_rpm_28: db 'rpm:  0910'
tulis_rpm_29: db 'rpm:  0850'
tulis_rpm_30: db 'rpm:  0790'
tulis_rpm_31: db 'rpm:  0730'
tulis_rpm_32: db 'rpm:  0670'
tulis_rpm_33: db 'rpm:  0610'
tulis_rpm_34: db 'rpm:  0550'
tulis_rpm_35: db 'rpm:  0490'
tulis_rpm_36: db 'rpm:  0430'
tulis_rpm_37: db 'rpm:  0370'
tulis_rpm_38: db 'rpm:  0310'
tulis_rpm_39: db 'rpm:  0250'
tulis_rpm_40: db 'rpm:  0190'
tulis_rpm_41: db 'rpm:  0130'
tulis_rpm_42: db 'rpm:  0070'
tulis_rpm_43: db 'rpm:  0010'
tulis_rpm_44: db 'rpm:  0300'

;=======================================
;data base rpm
;=======================================
tulis_jarak_1: db 'jarak:     0 Km'
tulis_jarak_2: db 'jarak:   500 Km'
tulis_jarak_3: db 'jarak:  1000 Km'
tulis_jarak_4: db 'jarak:  1500 Km'
tulis_jarak_5: db 'jarak:  2000 Km'
tulis_jarak_6: db 'jarak:  2500 Km'

pilihan:        db '1=1500K  2=2000K'
pilihan2:       db '    3=2500K     '
end
```

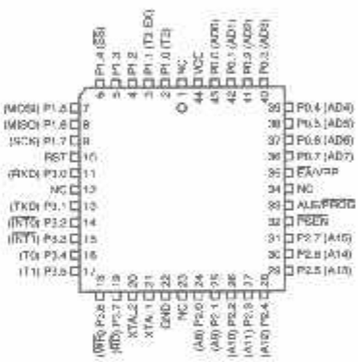
n Configurations

PDIP

TQFP



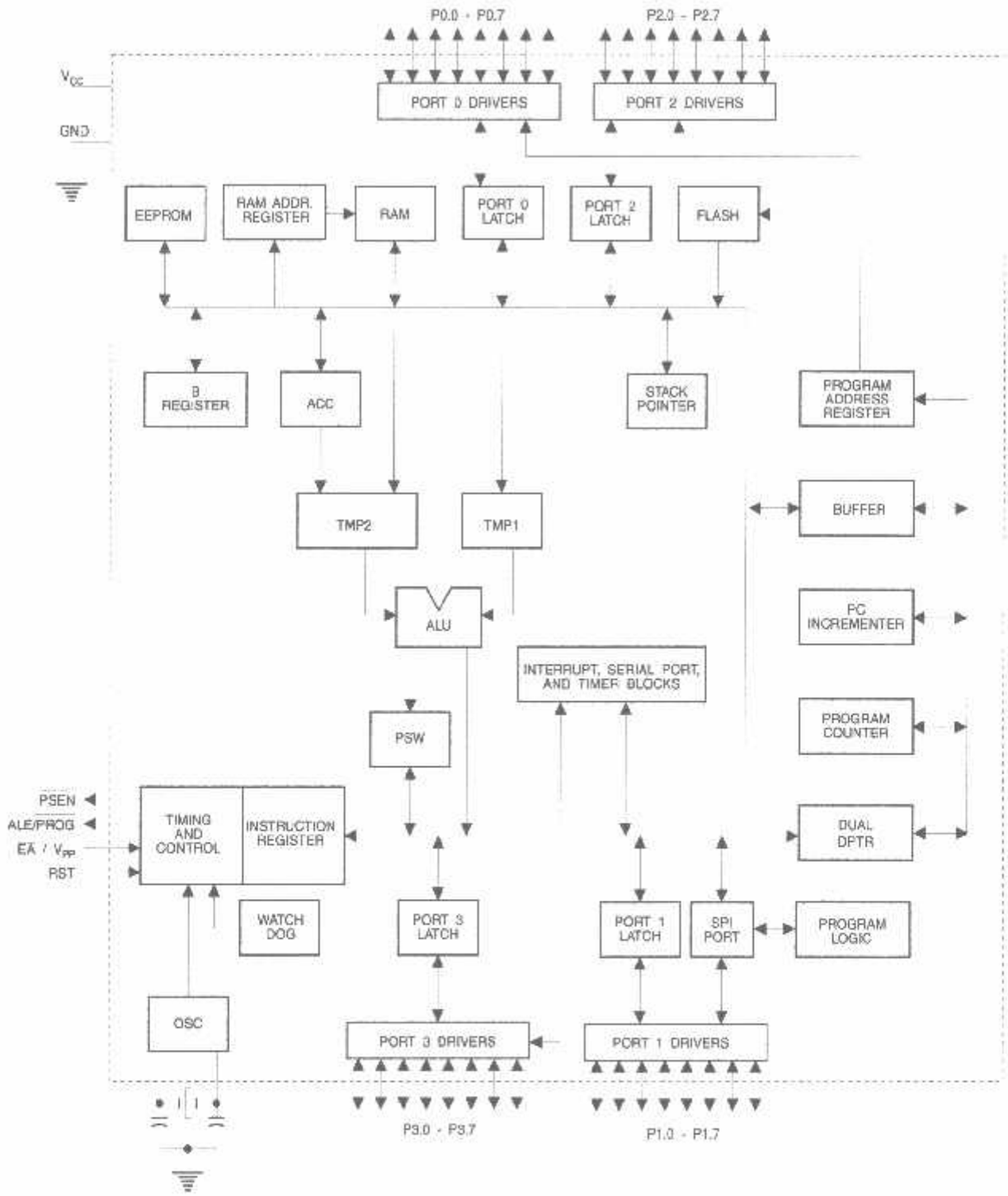
PLCC



in Description

CC	Supply voltage.
ND	Ground.
ort 0	Port 0 is an 8-bit open drain bi-didirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs. Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.
ort 1	Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

lock Diagram



Some Port 1 pins provide additional functions. P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively.

Furthermore, P1.4, P1.5, P1.6, and P1.7 can be configured as the SPI slave port select, data input/output and shift clock input/output pins as shown in the following table.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.4	$\overline{SS}$ (Slave port select input)
P1.5	MOSI (Master data output, slave data input pin for SPI channel)
P1.6	MISO (Master data input, slave data output pin for SPI channel)
P1.7	SCK (Master clock output, slave clock input pin for SPI channel)

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S8252, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

IST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{SEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89S8252 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{A}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{pp}) during Flash programming when 12-volt programming is selected.

TAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

TAL2

Output from the inverting oscillator amplifier.

pecial Function :egisters

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 9) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

able 1. AT89S8252 SFR Map and Reset Values

0F8H								0FFH
0F0H	B 00000000							0F7H
0E8H								0EFH
0E0H	ACC 00000000							0E7H
0D8H								0DF H
0D0H	PSW 00000000					SPCR 000001XX		0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000		0CF H
0C0H								0C7H
0B8H	IP XX000000							0BFH
0B0H	P3 11111111							0B7H
0A8H	IE 0X000000		SPSR 0XXXXXXX					0AFH
0A0H	P2 11111111							0A7H
98H	SCON 00000000	SBUF XXXXXXXX						9FH
90H	P1 11111111						WMCON 00000010	97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000	SPDR XXXXXXXX	PCON 0XXX0000 87H

ıble 2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled. EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflows to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

atchdog and Memory Control Register The WMCON register contains control bits for the Watchdog Timer (shown in ıble 3). The EEMEN and EEMWE bits are used to select the 2K bytes on-chip EEPROM, and to enable byte-write. The ?S bit selects one of two DPTR registers available.

ıble 3. WMCON—Watchdog and Memory Control Register

'MCON Address = 96H — Reset Value = 0000 0010B

Bit	PS2	PS1	PS0	EEMWE	EEMEN	DPS	WDTRST	WDTEN
	7	6	5	4	3	2	1	0

Symbol	Function
PS2 PS1 PS0	Prescaler Bits for the Watchdog Timer. When all three bits are set to "0", the watchdog timer has a nominal period of 16 ms. When all three bits are set to "1", the nominal period is 2048 ms.
EEMWE	EEPROM Data Memory Write Enable Bit. Set this bit to "1" before initiating byte write to on-chip EEPROM with the MOVX instruction. User software should set this bit to "0" after EEPROM write is completed.
EEMEN	Internal EEPROM Access Enable. When EEMEN = 1, the MOVX instruction with DPTR will access on-chip EEPROM instead of external data memory. When EEMEN = 0, MOVX with DPTR accesses external data memory.
DPS	Data Pointer Register Select. DPS = 0 selects the first bank of Data Pointer Register, DP0, and DPS = 1 selects the second bank, DP1
WDTRST RDY/$\overline{BSY}$	Watchdog Timer Reset and EEPROM Ready/$\overline{Busy}$ Flag. Each time this bit is set to "1" by user software, a pulse is generated to reset the watchdog timer. The WDTRST bit is then automatically reset to "0" in the next instruction cycle. The WDTRST bit is Write-Only. This bit also serves as the RDY/$\overline{BSY}$ flag in a Read-Only mode during EEPROM write. RDY/$\overline{BSY}$ = 1 means that the EEPROM is ready to be programmed. While programming operations are being executed, the RDY/$\overline{BSY}$ bit equals "0" and is automatically reset to "1" when programming is completed.
WDTEN	Watchdog Timer Enable Bit. WDTEN = 1 enables the watchdog timer and WDTEN = 0 disables the watchdog timer.

SPI Registers Control and status bits for the Serial Peripheral Interface are contained in registers SPCR (shown in Table 4) and SPSR (shown in Table 5). The SPI data bits are contained in the SPDR register. Writing the SPI data register during serial data transfer sets the Write Collision bit, WCOL, in the SPSR register. The SPDR is double buffered for writing and the values in SPDR are not changed by Reset.

Interrupt Registers The global interrupt enable bit and the individual interrupt enable bits are in the IE register. In addition, the individual interrupt enable bit for the SPI is in the SPCR register. Two priorities can be set for each of the six interrupt sources in the IP register.

Dual Data Pointer Registers To facilitate accessing both internal EEPROM and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR WMCON selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag The Power Off Flag (POF) is located at bit_4 (PCON.4) in the PCON SFR. PCF is set to "1" during power up. It can be set and reset under software control and is not affected by RESET.

Table 4. SPCR – SPI Control Register

SPCR Address = D5H — Reset Value = 0000 01XXB

Bit	7	6	5	4	3	2	1	0
	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

Symbol	Function
SPIE	SPI Interrupt Enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI Enable. SPI = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPI = 0 disables the SPI channel.
DORD	Data Order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/Slave Select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects Slave SPI mode.
CPOL	Clock Polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI Clock Phase and Polarity Control.
CPHA	Clock Phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI Clock Phase and Polarity Control.
SPR0 SPR1	SPI Clock Rate Select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, F_{osc}, is as follows: SPR1 SPR0 SCK = F_{osc} divided by 0 0 4 0 1 16 1 0 64 1 1 128

ible 5. SPSR – SPI Status Register

SPSR Address = AAH — Reset Value = 00XX XXXXB

	SPIF	WCOL	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIF	SPI Interrupt Flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register with SPIF and WCOL bits set, and then reading/writing the SPI data register.
WCOL	Write Collision Flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register with SPIF and WCOL set, and then accessing the SPI data register.

able 6. SPDR – SPI Data Register

SPDR Address = 86H — Reset Value = unchanged

	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Bit	7	6	5	4	3	2	1	0

)ata Memory – :EPROM and RAM

The AT89S8252 implements 2K bytes of on-chip EEPROM for data storage and 256 bytes of RAM. The upper 128 bytes of RAM occupy a parallel space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

The on-chip EEPROM data memory is selected by setting the EEMEN bit in the WMCON register at SFR address location 96H. The EEPROM address range is from 000H to 7FFH. The MOVX instructions are used to access the EEPROM. To access off-chip data memory with the MOVX instructions, the EEMEN bit needs to be set to "0".

The EEMWE bit in the WMCON register needs to be set to "1" before any byte location in the EEPROM can be written. User software should reset EEMWE bit to "0" if no further EEPROM write is required. EEPROM write cycles in the serial programming mode are self-timed and typically take 2.5 ms. The progress of EEPROM write can be monitored by reading the RDY/$\overline{BSY}$ bit (read-only) in SFR WMCON. RDY/$\overline{BSY}$ = 0 means

programming is still in progress and RDY/$\overline{BSY}$ = 1 means EEPROM write cycle is completed and another write cycle can be initiated.

In addition, during EEPROM programming, an attempted read from the EEPROM will fetch the byte being written with the MSB complemented. Once the write cycle is completed, true data are valid at all bit locations.

rogrammable Vatchdog Timer

The programmable Watchdog Timer (WDT) operates from an independent internal oscillator. The prescaler bits, PS0, PS1 and PS2 in SFR WMCON are used to set the period of the Watchdog Timer from 16 ms to 2048 ms. The available timer periods are shown in the following table and the actual timer periods (at V_{CC} = 5V) are within ±30% of the nominal.

The WDT is disabled by Power-on Reset and during Power-down. It is enabled by setting the WDTEN bit in SFR WMCON (address = 96H). The WDT is reset by setting the WDTRST bit in WMCON. When the WDT times out without being reset or disabled, an internal RST pulse is generated to reset the CPU.

Table 7. Watchdog Timer Period Selection

WDT Prescaler Bits			
PS2	PS1	PS0	Period (nominal)
0	0	0	16 ms
0	0	1	32 ms
0	1	0	64 ms
0	1	1	128 ms
1	0	0	256 ms
1	0	1	512 ms
1	1	0	1024 ms
1	1	1	2048 ms

imer 0 and 1

Timer 0 and Timer 1 in the AT89S8252 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 8.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected.

Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

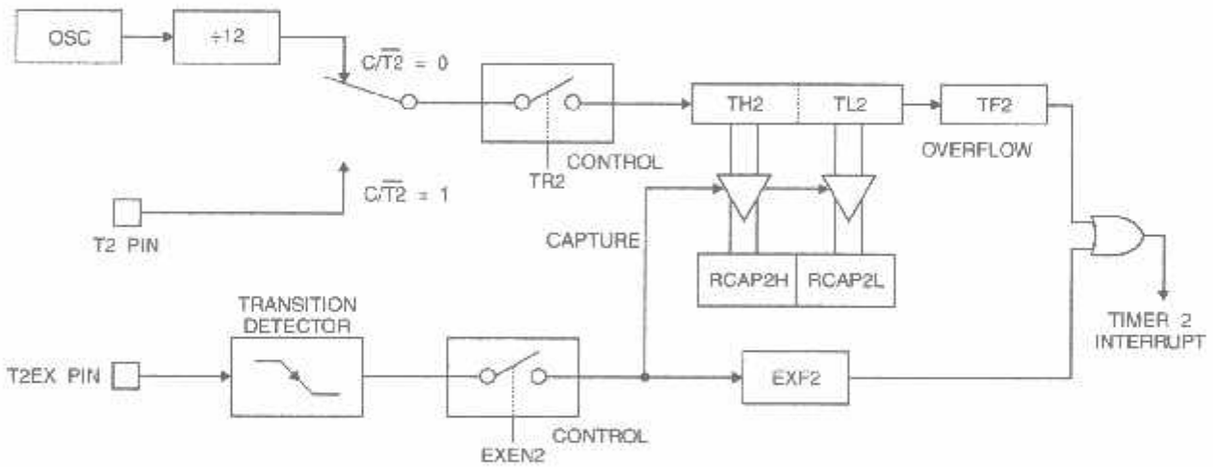
Table 8. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a I-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Figure 1. Timer 2 in Capture Mode



.uto-reload (Up or Down :ounter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 9). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in RCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered e ther by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 2. Timer 2 in Auto Reload Mode (DCEN = 0)

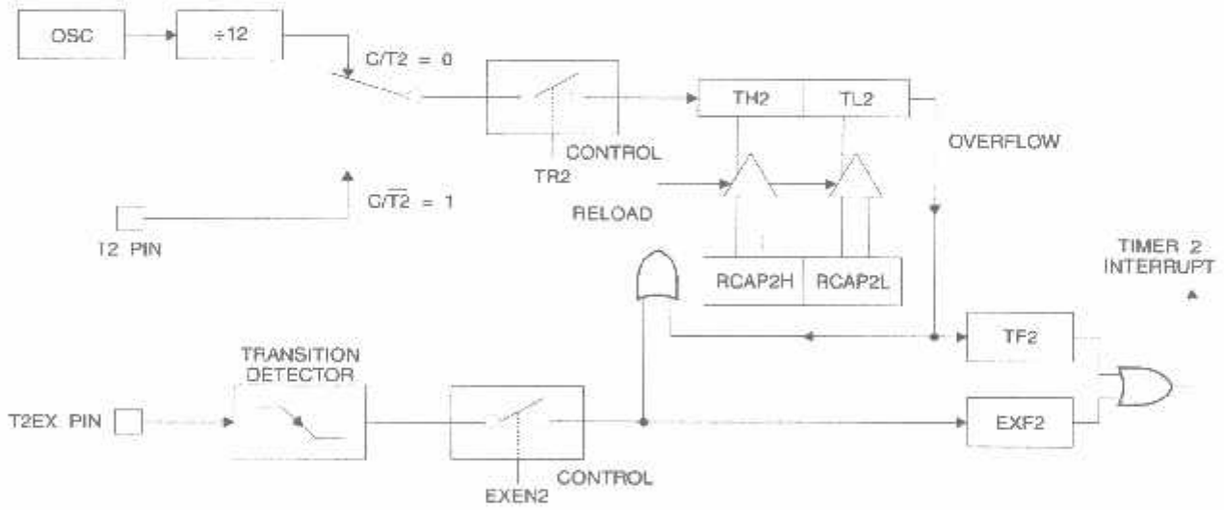


Table 9. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

	–	–	–	–	–	–	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
–	Not implemented, reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

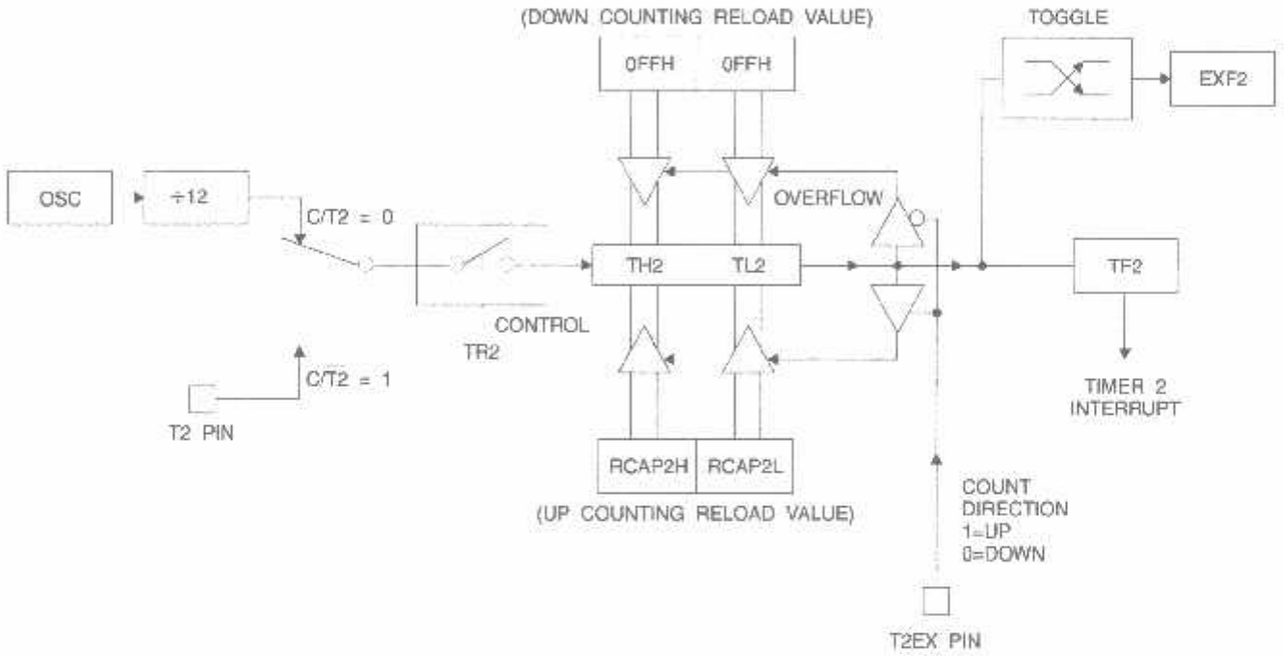
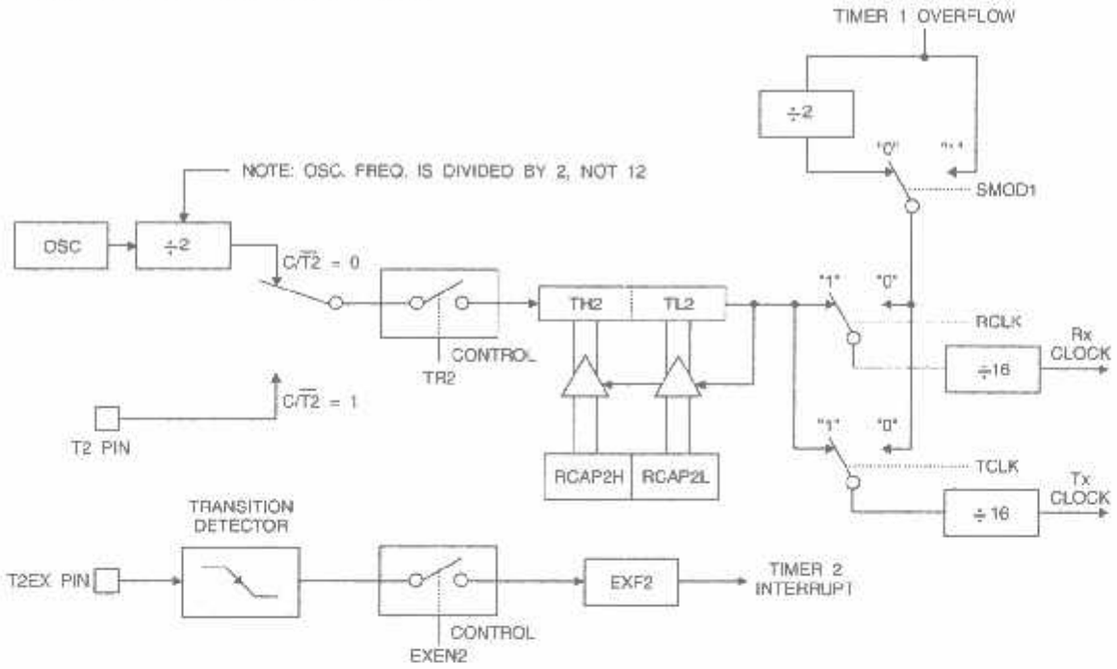


Figure 4. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

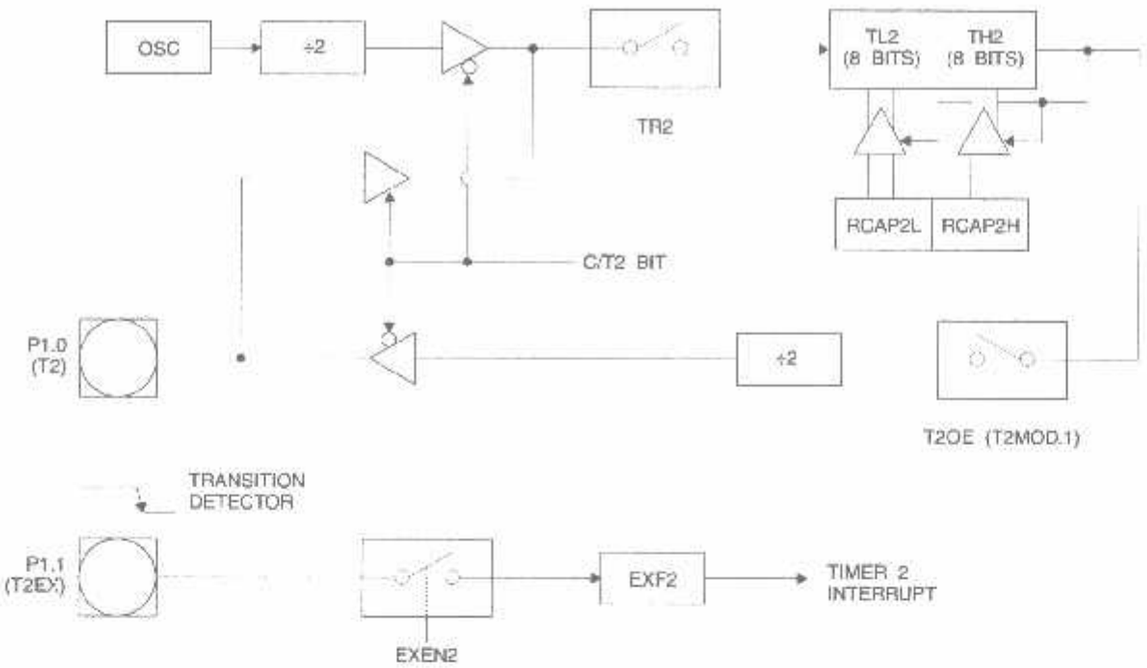
To configure the Timer/Counter 2 as a clock generator, bit $C/\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

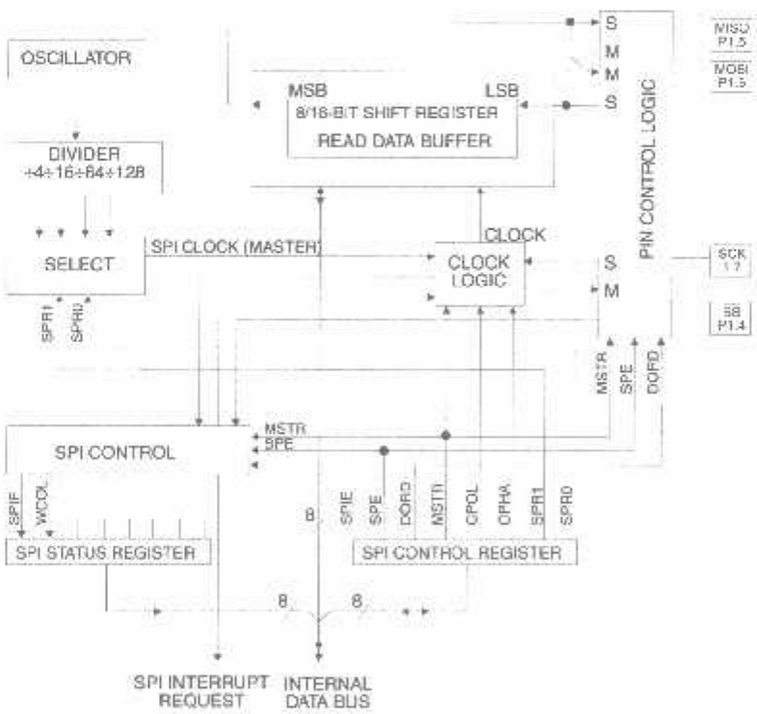
$$\text{Clock Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 rollovers will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

igure 5. Timer 2 in Clock-out Mode



igure 6. SPI Block Diagram



UART

The UART in the AT89S8252 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, refer to the Atmel web site (http://www.atmel.com). From the home page, select "Products", then "Microcontrollers, then "8051-Architecture". Click on "Documentation", then on "Other Documents". Open the document "AT89 Series Hardware Description".

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89S8252 and peripheral devices or between several AT89S8252 devices. The AT89S8252 SPI features include the following:

- Full-Duplex, 3-Wire Synchronous Data Transfer
- Master or Slave Operation
- 1.5 MHz Bit Frequency (max.)
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wakeup from Idle Mode (Slave Mode Only)

The interconnection between master and slave CPUs with SPI is shown in the following figure. The SCK pin is the clock output in the master mode but is the clock input in the slave mode. Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested.

The Slave Select input, $\overline{SS}$/P1.4, is set low to select an individual SPI device as a slave. When $\overline{SS}$/P1.4 is set high, the SPI port is deactivated and the MOSI/P1.5 pin can be used as an input.

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 8 and Figure 9.

Figure 7. SPI Master-slave Interconnection

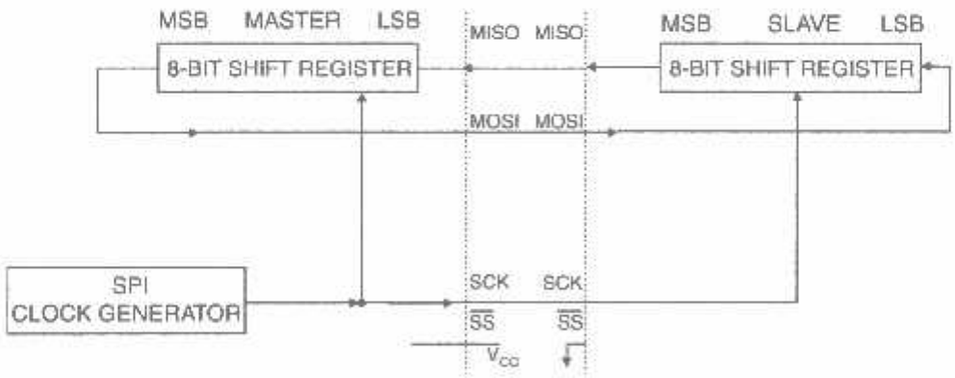
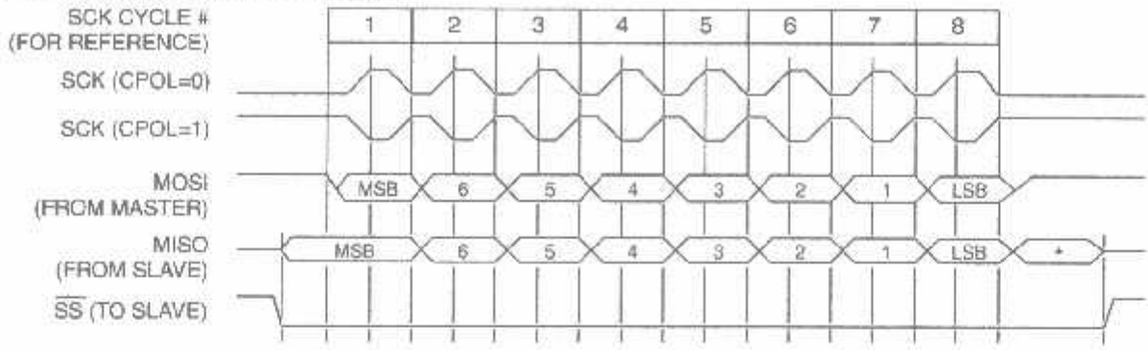
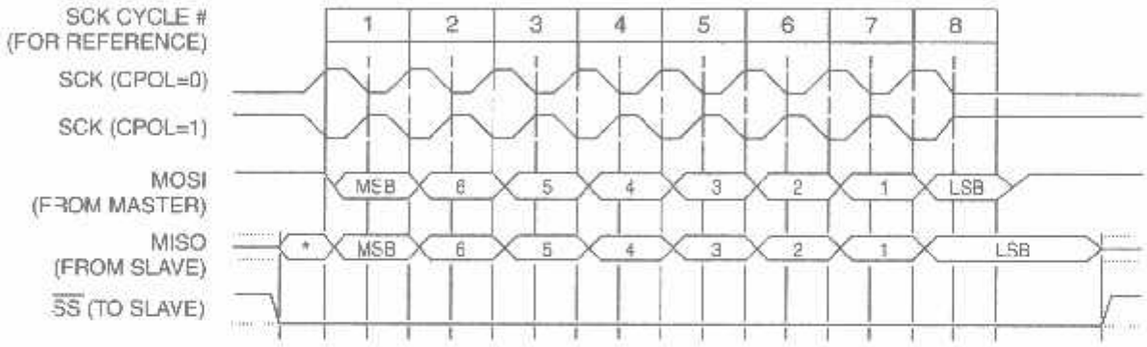


Figure 8. SPI transfer Format with CPHA = 0



Note: *Not defined but normally MSB of character just received

Figure 9. SPI Transfer Format with CPHA = 1



Note: *Not defined but normally LSB of previously transmitted character.

Interrupts

The AT89S8252 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

able 10. Interrupt Enable (IE) Register

(MSB)(LSB)

EA	–	ET2	ES	ET1	EX1	ET0	EX0

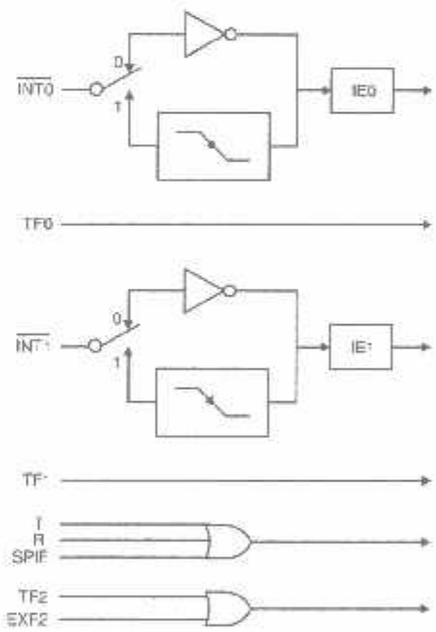
Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	SPI and UART interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.

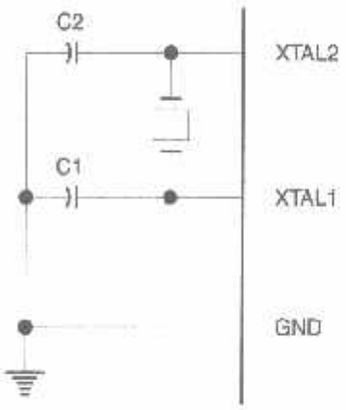
igure 10. Interrupt Sources



Oscillator Characteristics

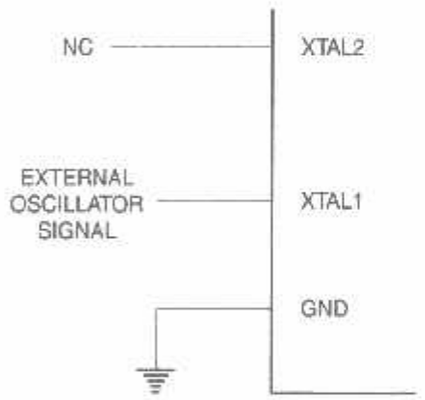
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration



ıle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

²ower-down Mode

In the power-down mode, the oscillator is stopped and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. Exit from power-down can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

To exit power-down via an interrupt, the external interrupt must be enabled as level sensitive before entering power-down. The interrupt service routine starts at 16 ms (nominal) after the enabled interrupt pin is activated.

²rogram Memory .ock Bits

The AT89S8252 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Once programmed, the lock bits can only be unprogrammed with the Chip Erase operations in either the parallel or serial modes.

.ock Bit Protection Modes[1][2]

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No internal memory lock feature.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset and further programming of the Flash memory (parallel or serial mode) is disabled.
3	P	P	U	Same as Mode 2, but parallel or serial verify are also disabled.
4	P	P	P	Same as Mode 3, but external execution is also disabled.

lotes: 1. U = Unprogrammed
2. P = Programmed

'rogramming the 'lash and EEPROM

Atmel's AT89S8252 Flash Microcontroller offers 8K bytes of in-system reprogrammable Flash Code memory and 2K bytes of EEPROM Data memory.

The AT89S8252 is normally shipped with the on-chip Flash Code and EEPROM Data memory arrays in the erased state (i.e. contents = FFH) and ready to be programmed. This device supports a High-voltage (12-V V_{PP}) Parallel programming mode and a Low-voltage (5-V V_{CC}) Serial programming mode. The serial programming mode provides a convenient way to reprogram the AT89S8252 inside the user's system. The parallel programming mode is compatible with conventional third party Flash or EPROM programmers.

The Code and Data memory arrays are mapped via separate address spaces in the serial programming mode. In the parallel programming mode, the two arrays occupy one contiguous address space: 0000H to 1FFFH for the Code array and 2000H to 27FFH for the Data array.

The Code and Data memory arrays on the AT89S8252 are programmed byte-by-byte in either programming mode. An auto-erase cycle is provided with the self-timed programming operation in the serial programming mode. There is no need to perform the Chip Erase operation to reprogram any memory location in the serial programming mode unless any of the lock bits have been programmed.

In the parallel programming mode, there is no auto-erase cycle. To reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Parallel Programming Algorithm: To program and verify the AT89S8252 in the parallel programming mode, the following sequence is recommended:

1. Power-up sequence:
   Apply power between V_{CC} and GND pins.
   Set RST pin to "H".
   Apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Set $\overline{PSEN}$ pin to "L"
   ALE pin to "H"
   $\overline{EA}$ pin to "H" and all other pins to "H".
3. Apply the appropriate combination of "H" or "L" logic levels to pins P2.6, P2.7, P3.6, P3.7 to select one of the programming operations shown in the Flash Programming Modes table.
4. Apply the desired byte address to pins P1.0 to P1.7 and P2.0 to P2.5.
   Apply data to pins P0.0 to P0.7 for Write Code operation.
5. Raise $\overline{EA}/V_{PP}$ to 12V to enable Flash programming, erase or verification.
6. Pulse ALE/$\overline{PROG}$ once to program a byte in the Code memory array, the Data memory array or the lock bits. The byte-write cycle is self-timed and typically takes 1.5 ms.
7. To verify the byte just programmed, bring pin P2.7 to "L" and read the programmed data at pins P0.0 to P0.7.
8. Repeat steps 3 through 7 changing the address and data for the entire 2K or 8K bytes array or until the end of the object file is reached.
9. Power-off sequence:
   Set XTAL1 to "L".
   Set RST and $\overline{EA}$ pins to "L".
   Turn V_{CC} power off.

In the parallel programming mode, there is no auto-erase cycle and to reprogram any non-blank byte, the user needs to use the Chip Erase operation first to erase both arrays.

Data Polling: The AT89S8252 features DATA Polling to indicate the end of a byte write cycle. During a byte write cycle in the parallel or serial programming mode, an attempted read of the last byte written will result in the complement of the written datum on P0.7 (parallel mode), and on the MSB of the serial output byte on MISO (serial mode). Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. DATA Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming in the parallel programming mode can also be monitored by the RDY/BSY output signal. Pin P3.4 is pulled Low after ALE goes High during programming to indicate BUSY. P3.4 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed Code or Data byte can be read back via the address and data lines for verification. The state of the lock bits can also be verified directly in the parallel programming mode. In the serial programming mode, the state of the lock bits can only be verified indirectly by observing that the lock bit features are enabled.

Chip Erase: Both Flash and EEPROM arrays are erased electrically at the same time. In the parallel programming mode, chip erase is initiated by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The Code and Data arrays are written with all "1"s in the Chip Erase operation.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 16 ms.

During chip erase, a serial read from any address location will return 00H at the data outputs.

Serial Programming Fuse: A programmable fuse is available to disable Serial Programming if the user needs maximum system security. The Serial Programming Fuse can only be programmed or erased in the Parallel Programming Mode.

The AT89S8252 is shipped with the Serial Programming Mode enabled.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

(030H) = 1EH indicates manufactured by Atmel
(031H) = 72H indicates 89S8252

Programming Interface

Every code byte in the Flash and EEPROM arrays can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most worldwide major programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Serial Downloading

Both the Code and Data memory arrays can be programmed using the serial SPI bus while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

An auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction unless any of the lock bits have been programmed. The Chip Erase operation turns the content of every memory location in both the Code and Data arrays into FFH.

The Code and Data memory arrays have separate address spaces:

0000H to 1FFFH for Code memory and 000H to 7FFH for Data memory.

Either an external system clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/40 of the crystal frequency. With a 24 MHz oscillator clock, the maximum SCK frequency is 600 kHz.

Serial Programming Algorithm

To program and verify the AT89S8252 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 24 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 40.
3. The Code or Data array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The selected memory location is first automatically erased before new data is written. The write cycle is self-timed and typically takes less than 2.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal operation.
6. Power-off sequence (if needed):

   Set XTAL1 to "L" (if a crystal is not used).

   Set RST to "L".

   Turn V_{CC} power off.

erial Programming
ıstruction

The Instruction Set for Serial Programming follows a 3-byte protocol and is shown in the following table:

ıstruction Set

Instruction	Input Format			Operation
	Byte 1	Byte 2	Byte 3	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	Enable serial programming interface after RST goes high.
Chip Erase	1010 1100	xxxx x100	xxxx xxxx	Chip erase both 8K & 2K memory arrays.
Read Code Memory	aaaa a001	low addr	xxxx xxxx	Read data from Code memory array at the selected address. The 5 MSBs of the first byte are the high order address bits. The low order address bits are in the second byte. Data are available at pin MISO during the third byte.
Write Code Memory	aaaa a010	low addr	data in	Write data to Code memory location at selected address. The address bits are the 5 MSBs of the first byte together with the second byte.
Read Data Memory	00aa a101	low addr	xxxx xxxx	Read data from Data memory array at selected address. Data are available at pin MISO during the third byte.
Write Data Memory	00aa a110	low addr	data in	Write data to Data memory location at selected address.
Write Lock Bits	1010 1100	LB1 LB2 LB3 x x111	xxxx xxxx	Write lock bits. Set LB1, LB2 or LB3 = "0" to program lock bits.

lotes:
1. DATA polling is used to indicate the end of a byte write cycle which typically takes less than 2.5 ms at 5V.
2. "aaaaa" = high order address.
3. "x" = don't care.

Flash and EEPROM Parallel Programming Modes

Mode	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7	Data I/O P0.7:0	Address P2.5:0 P1.7:0
Serial Prog. Modes	H	H[1]	H[1]	x						
Chip Erase	H	L	⌐‾⌐ (2)	12V	H	L	L	L	X	X
Write (10K bytes) Memory	H	L	⌐‾⌐	12V	L	H	H	H	DIN	ADDR
Read (10K bytes) Memory	H	L	H	12V	L	L	H	H	DOUT	ADDR
Write Lock Bits:	H	L	⌐‾⌐	12V	H	L	H	L	DIN	X
Bit - 1									P0.7 = 0	X
Bit - 2									P0.6 = 0	X
Bit - 3									P0.5 = 0	X
Read Lock Bits:	H	L	H	12V	H	H	L	L	DOUT	X
Bit - 1									@P0.2	X
Bit - 2									@P0.1	X
Bit - 3									@P0.0	X
Read Atmel Code	H	L	H	12V	L	L	L	L	DOUT	30H
Read Device Code	H	L	H	12V	L	L	L	L	DOUT	31H
Serial Prog. Enable	H	L	⌐‾⌐ (2)	12V	L	H	L	H	P0.0 = 0	X
Serial Prog. Disable	H	L	⌐‾⌐ (2)	12V	L	H	L	H	P0.0 = 1	X
Read Serial Prog. Fuse	H	L	H	12V	H	H	L	H	@P0.0	X

Notes: 1. "H" = weakly pulled "High" internally.
2. Chip Erase and Serial Programming Fuse require a 10 ms $\overline{PROG}$ pulse. Chip Erase needs to be performed first before reprogramming any byte with a content other than FFH.
3. P3.4 is pulled Low during programming to indicate RDY/$\overline{BSY}$.
4. "X" = don't care

Figure 13. Programming the Flash/EEPROM Memory

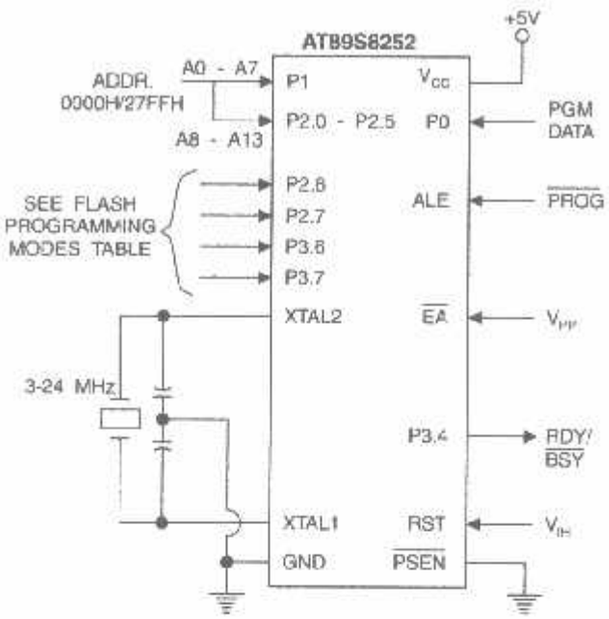


Figure 14. Verifying the Flash/EEPROM Memory

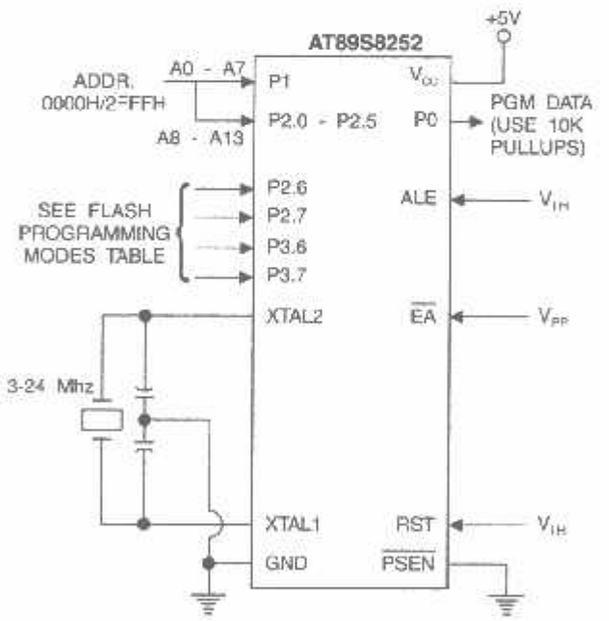
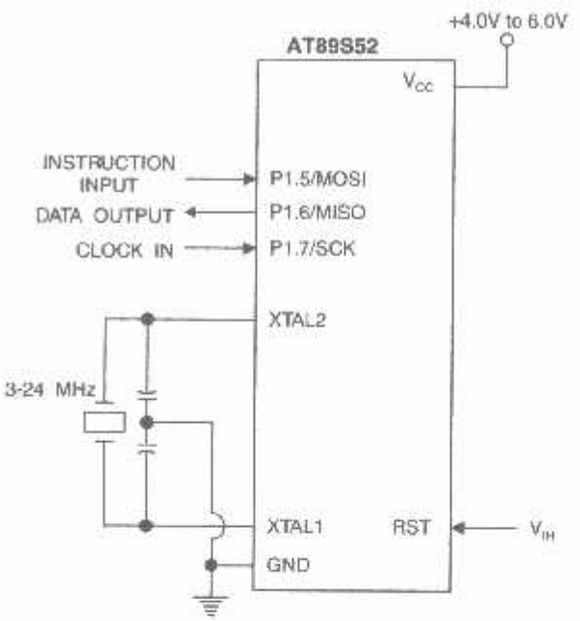


Figure 15. Flash/EEPROM Serial Downloading

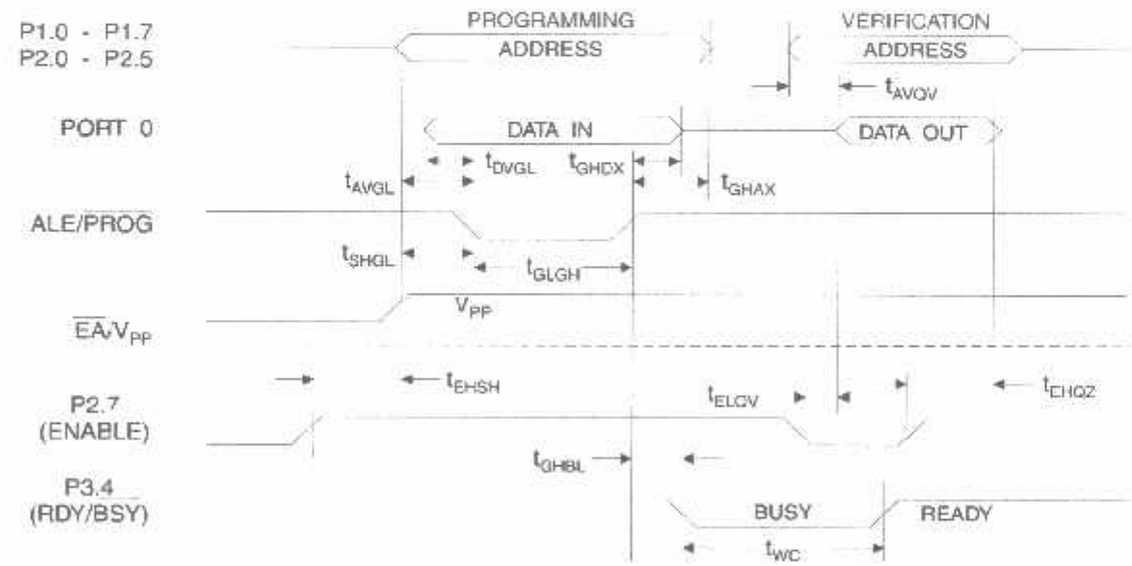


Flash Programming and Verification Characteristics – Parallel Mode

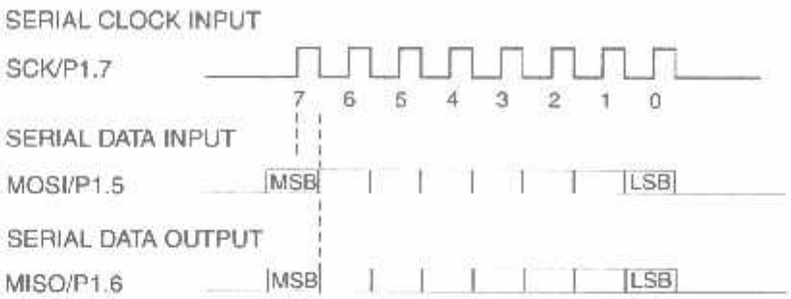
T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Flash/EEPROM Programming and Verification Waveforms – Parallel Mode

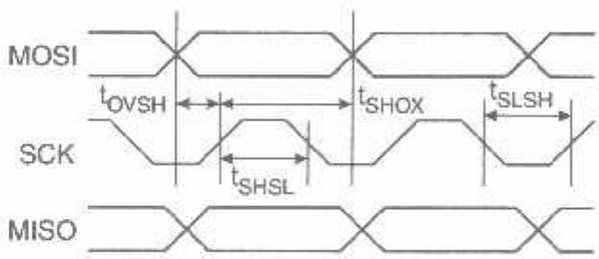


ierial Downloading Waveforms



erial Programming Characteristics

igure 16. Serial Programming Timing



able 11. Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 4.0 - 6.0V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0		24	MHz
t_{CLCL}	Oscillator Period	41.6			ns
t_{SHSL}	SCK Pulse Width High	24 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	24 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage [1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.5	V
V_{OL1}	Output Low-voltage [1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.5	V
V_{OH}	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode [2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA; Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V

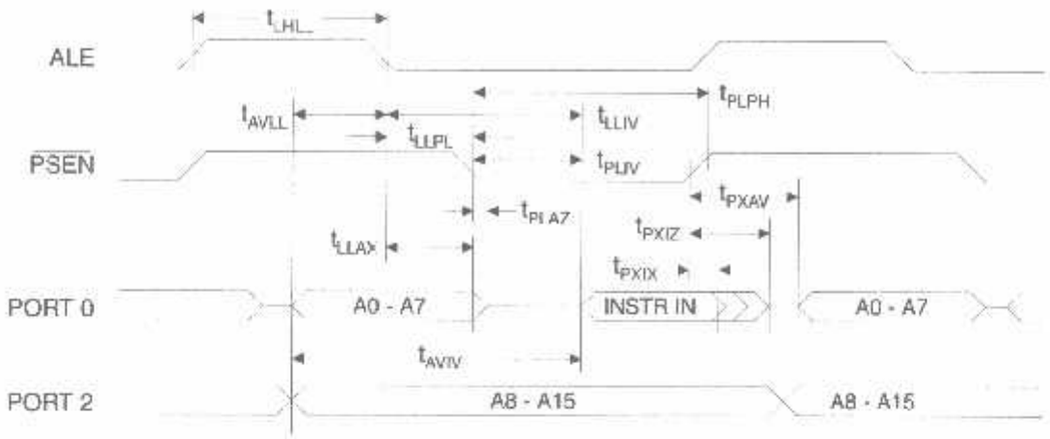
\C Characteristics

nder operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other .utputs = 8C pF.

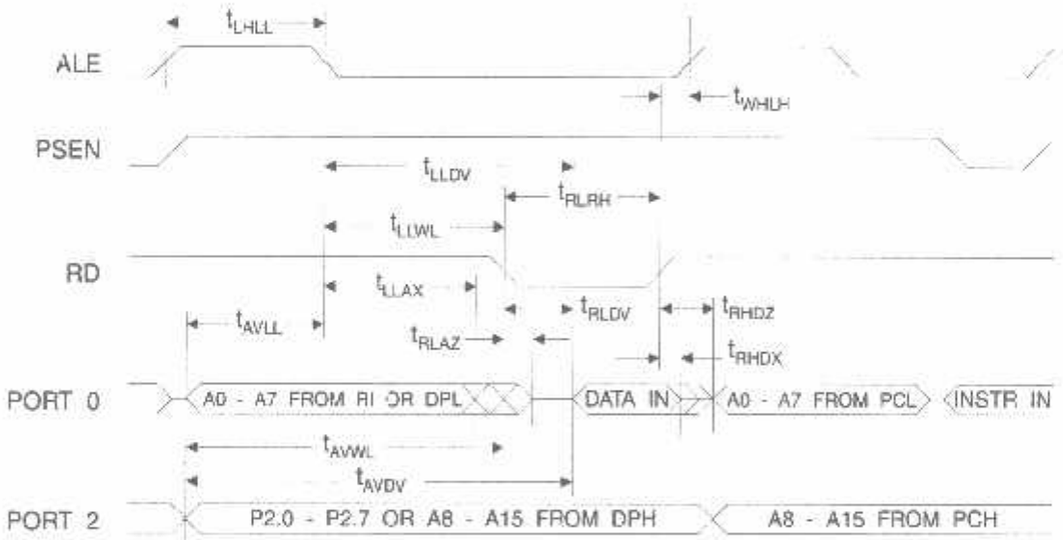
xternal Program and Data Memory Characteristics

Symbol	Parameter	Variable Oscillator		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{LHLL}	ALE Pulse Width	$2t_{CLCL}$ - 40		ns
t_{AVLL}	Address Valid to ALE Low	t_{CLCL} - 13		ns
t_{LLAX}	Address Hold after ALE Low	t_{CLCL} - 20		ns
t_{LLIV}	ALE Low to Valid Instruction In		$4t_{CLCL}$ - 65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	t_{CLCL} - 13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	$3t_{CLCL}$ - 20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		$3t_{CLCL}$ - 45	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	0		ns
t_{PXIZ}	Input Instruction Float after PSEN		t_{CLCL} - 10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	t_{CLCL} - 8		ns
t_{AVIV}	Address to Valid Instruction In		$5t_{CLCL}$ - 55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	$6t_{CLCL}$ - 100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		$5t_{CLCL}$ - 90	ns
t_{RHDX}	Data Hold after $\overline{RD}$	0		ns
t_{RHDZ}	Data Float after $\overline{RD}$		$2t_{CLCL}$ - 28	ns
t_{LLDV}	ALE Low to Valid Data In		$8t_{CLCL}$ - 150	ns
t_{AVDV}	Address to Valid Data In		$9t_{CLCL}$ - 165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3t_{CLCL}$ - 50	$3t_{CLCL}$ + 50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	$4t_{CLCL}$ - 75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	t_{CLCL} - 20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	$7t_{CLCL}$ - 120		ns
t_{WHQX}	Data Hold after $\overline{WR}$	t_{CLCL} - 20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL} - 20	t_{CLCL} + 25	ns

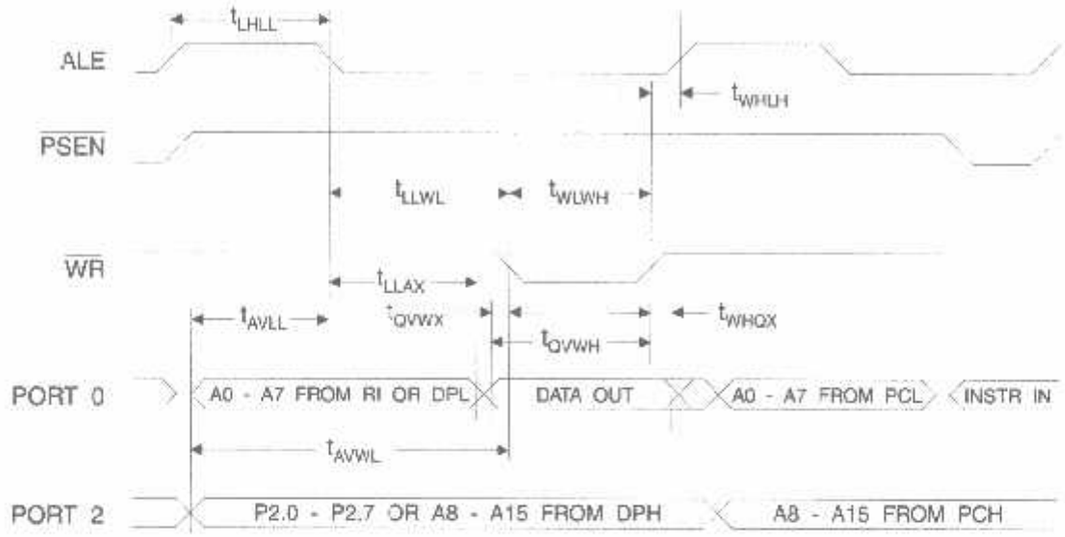
External Program Memory Read Cycle



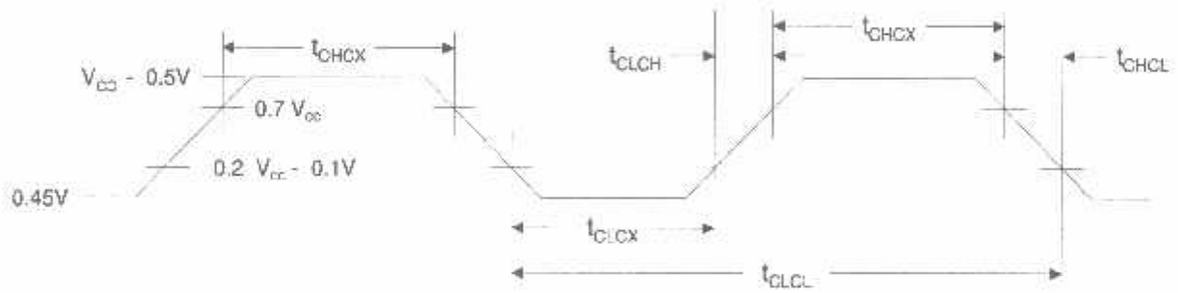
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

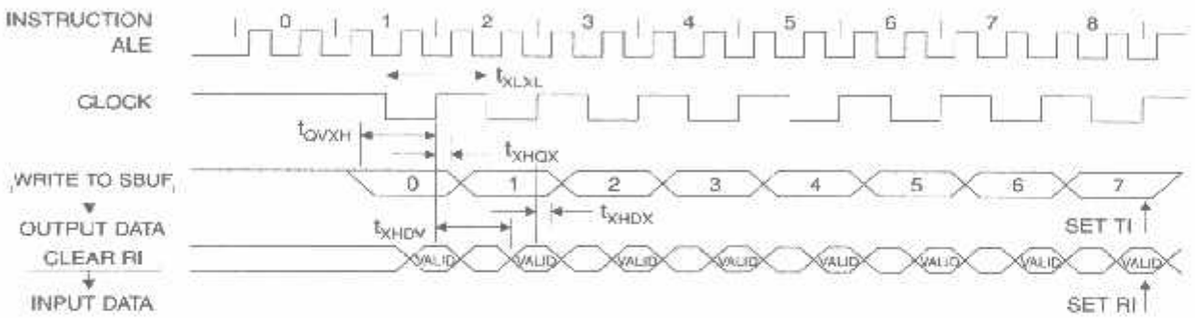
Symbol	Parameter	V_{CC} = 4.0V to 6.0V		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

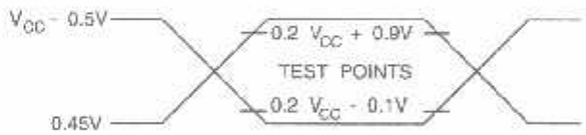
The values in this table are valid for V_{CC} = 4.0V to 6V and Load Capacitance = 80 pF.

Symbol	Parameter	Variable Oscillator Min	Variable Oscillator Max	Units
t_{XLXL}	Serial Port Clock Cycle Time	$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	$10t_{CLCL}$ - 133		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	$2t_{CLCL}$ - 117		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		$10t_{CLCL}$ - 133	ns

Shift Register Mode Timing Waveforms



AC Testing Input/Output Waveforms[1]



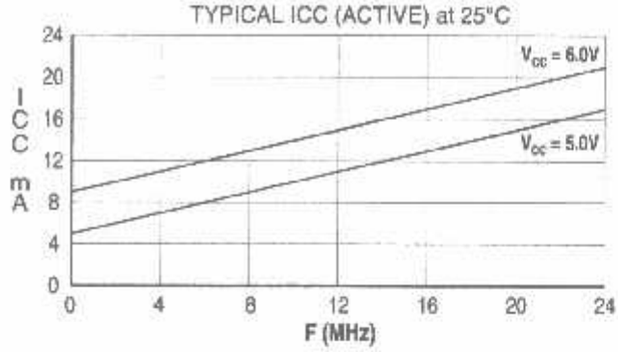
Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]

Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

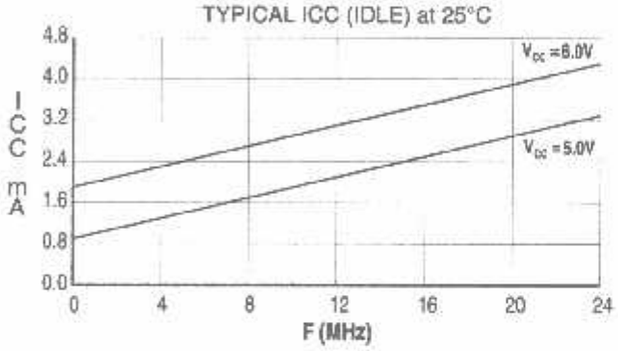
AT89S8252

TYPICAL ICC (ACTIVE) at 25°C



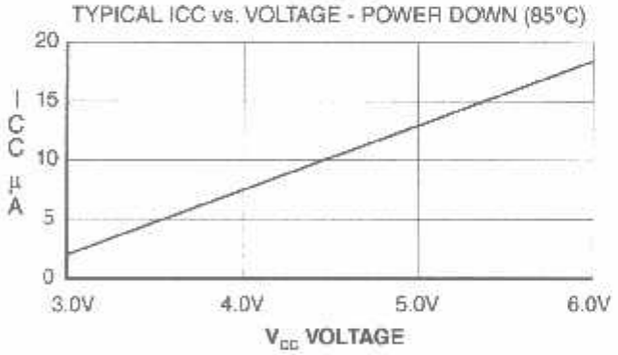
AT89S8252

TYPICAL ICC (IDLE) at 25°C



AT89S8252

TYPICAL ICC vs. VOLTAGE - POWER DOWN (85°C)



Notes: 1. XTAL1 tied to GND for Icc (power-down)
2. Lock bits programmed

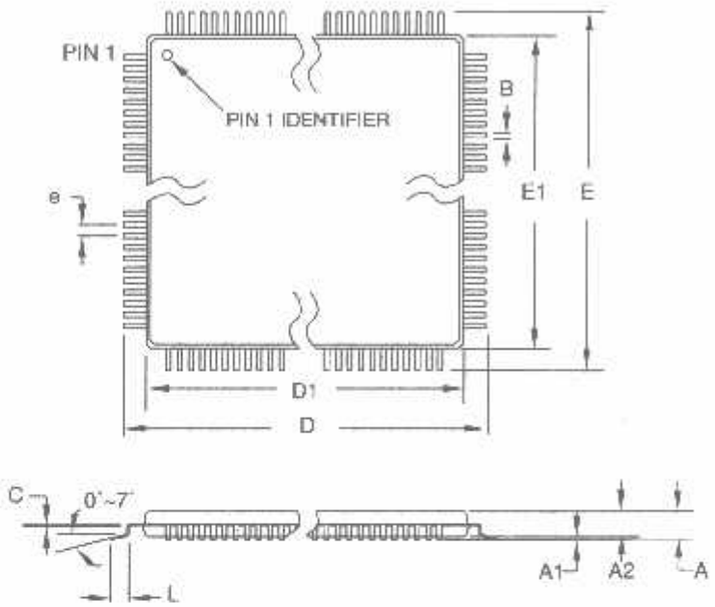
Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 6.0V	AT89S8252-24AC	44A	Commercial (0°C to 70°C)
		AT89S8252-24JC	44J	
		AT89S8252-24PC	40P6	
	4.0V to 6.0V	AT89S8252-24AI	44A	Industrial (-40°C to 85°C)
		AT89S8252-24JI	44J	
		AT89S8252-24PI	40P6	

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Packaging Information

44A – TQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

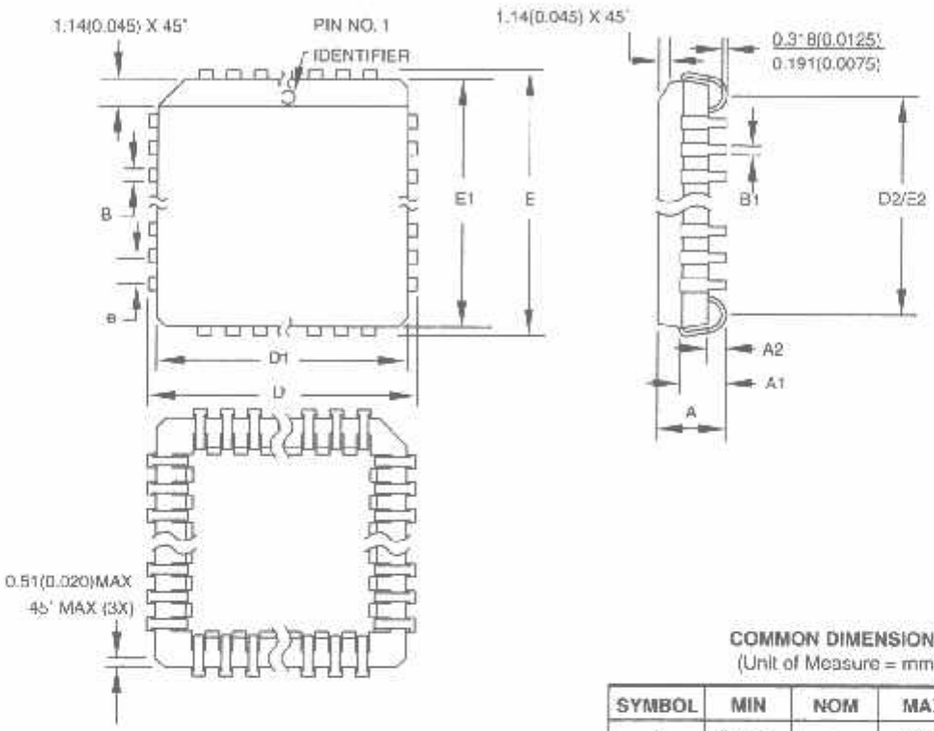
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A**, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

4J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

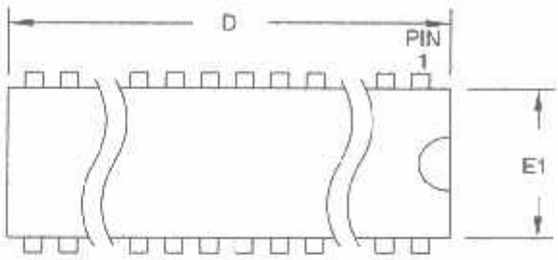
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

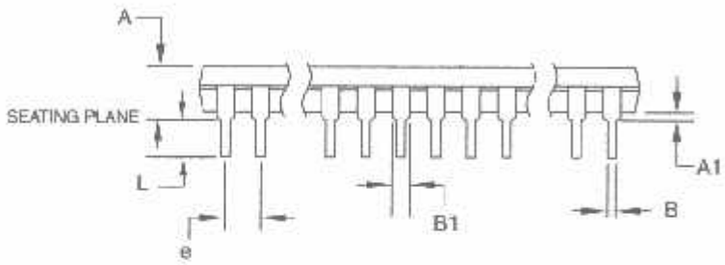
Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

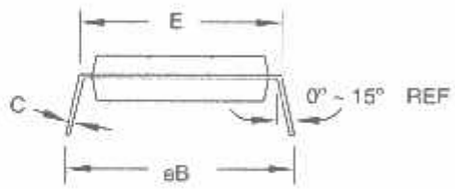
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

0P6 – PDIP







COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

2325 Orchard Parkway San Jose, CA 95131	**TITLE** **40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	**DRAWING NO.** 40P6	**REV.** B

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Winbond Electronics Corp.

ISD1400 SERIES

SINGLE-CHIP

VOICE RECORD/PLAYBACK DEVICES

16- AND 20-SECOND DURATION

Publication Release Date: June 21, 2005
Revision 1.2

Winbond Electronics Corp.

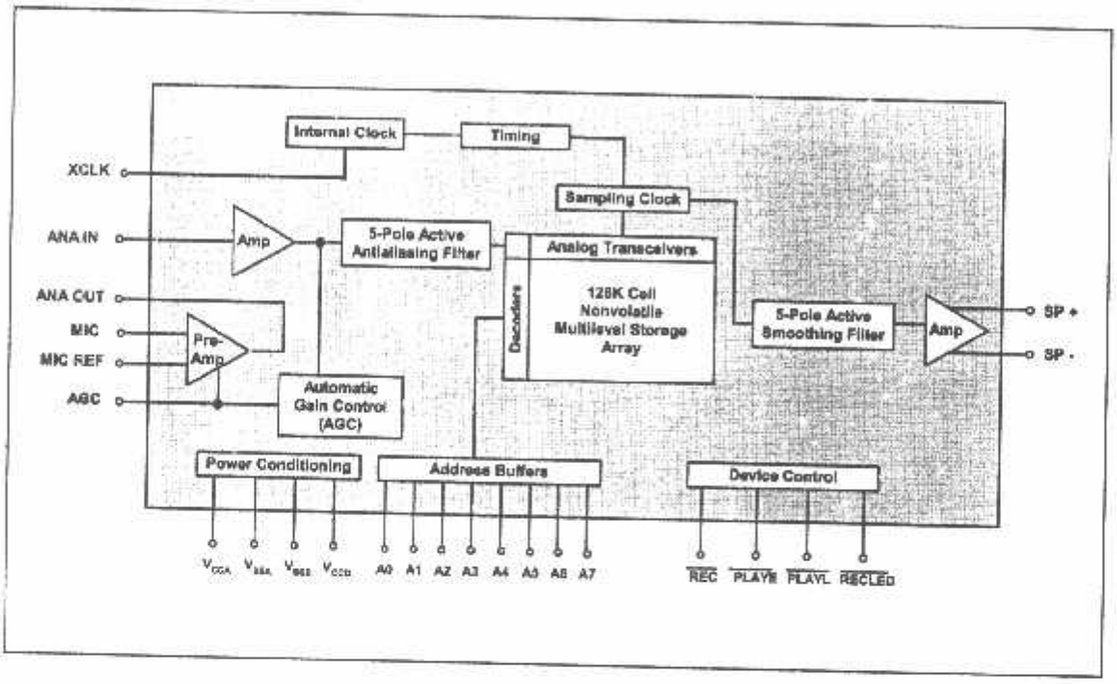
1. GENERAL DESCRIPTION

Winbond's ISD1400 ChipCorder® series provide high-quality, single-chip, Record/Playback solutions to short-duration messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, anti-aliasing filter, smoothing filter, and speaker amplifier. A minimum Record/Playback subsystem can be configured with a microphone, a speaker, several passive components, two push buttons and a power source. Recordings are stored into on-chip non-volatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through Winbond's patented Multi-Level Storage (MLS) technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

2. FEATURES

- Single +5 volt power supply
- Duration: 14 and 20 seconds.
- Easy-to-use single-chip, voice record/playback solution
- High-quality, natural voice/audio reproduction
- Manual switch or microcontroller compatible Playback can be edge- or level-activated
- Directly cascadable for longer durations
- Automatic power-down (push-button mode)
    - Standby current 1 µA (typical)
- Zero-power message storage
    - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip oscillator
- Programmer support for play-only applications
- Available in die, PDIP and SOIC
- Temperature:
    - Commercial - Packaged unit : 0°C to 70°C, Die : 0°C to 50°C
    - Industrial - Packaged unit : -40°C to 85°C

3. BLOCK DIAGRAM



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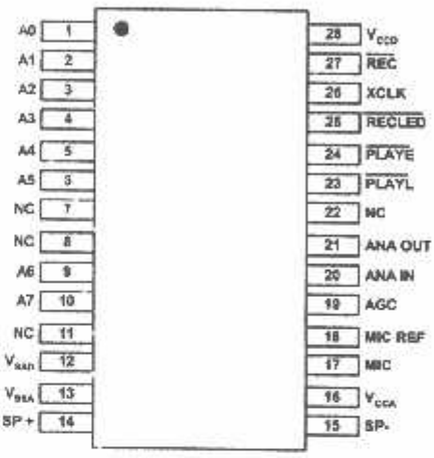
5. PIN CONFIGURATION



SOIC / PDIP

Note: NC means must be No connect

6. PIN DESCRIPTION

PIN NAME	PIN NO	FUNCTION
A0-A7	1-6, 9, 10	**Address Inputs:** The address inputs have two functions, depending on the level of the two Most Significant Bits (MSB) of the address. If either or both of the two MSBs are LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of $\overline{\text{PLAYE}}$, $\overline{\text{PLAYL}}$, or $\overline{\text{REC}}$. If both A6 & A7 are HIGH, then the device is in special operational modes. Please refer to operational modes section for details.
NC	7, 8, 11, 22	**NC:** No Connect
V_{SSD}, V_{SSA}	12, 13	**Ground:** Similar to V_{CCA} and V_{CCD}, the analog and digital circuits internal to the ISD1400 series use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.
SP+, SP-	14, 15	**Speaker Outputs:** The SP+ and SP- pins provide direct drive for loudspeakers with impedances as low as 16 Ω. A single output may be used, but, for direct-drive loudspeakers, the two opposite-polarity outputs provide an improvement in output power of up to four times over a single-ended connection. Forthermore, when SP+ and SP- are used, a speakercoupling capacitor is not required. A single-ended connection will require an AC-coupling capacitor between the SP pin and the speaker. The speaker outputs are in a high-impedance state during a record cycle, and held at V_{SSA} during power down.
V_{CCA}, V_{CCD}	16, 28	**Supply Voltage:** Analog and digital circuits internal to the ISD1400 series use separate power buses to minimize noise on the chip. These voltage buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the power supply he decoupled as close to the package as possible.
MIC	17	**Microphone:** The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the ISD1400 series passband. See Winbond's Application Information for additional information on low-frequency cutoff calculation.

PIN NAME	PIN NO	FUNCTION
MIC REF	18	**Microphone Reference:** The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected to a differential microphone.
AGC	19	**Automatic Gain Control (AGC):** The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of sound, from whispers to loud sounds, to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C6 on the schematic of section 11, Figure 5) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R5) and an external capacitor (C6) connected in parallel between the AGC pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases.
ANA IN	20	**Analog Input:** The analog input pin transfers its signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.
ANA OUT	21	**Analog Output:** This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.
$\overline{\text{PLAYL}}$ [2]	23	**Playback, Level-Activated:** When this input signal is held LOW, a playback cycle is initiated, and playback continues until $\overline{\text{PLAYL}}$ is pulled HIGH, or an EOM marker is detected. The device automatically powers down and enters into standby mode upon completion of a playback cycle.
$\overline{\text{PLAYE}}$ [2]	24	**Playback, Edge-Activated:** When a LOW-going transition is input to this pin, a playback cycle begins. Taking $\overline{\text{PLAYE}}$ HIGH during a playback cycle will not terminate the current cycle. Playback continues until an EOM is encountered. Upon completion of a playback cycle, the device automatically powers down and enters into standby mode.

PIN NAME	PIN NO	FUNCTION
$\overline{\text{RECLED}}$	25	**Record LED**: The $\overline{\text{RECLED}}$ output is LOW during a record cycle. It can be used to drive an LED to indicate a record cycle is in progress. In addition, $\overline{\text{RECLED}}$ pulses LOW momentarily when an end-of-message is encountered in a playback operation.
XCLK	26	**External Clock**: The input has an internal pull-down device. The ISD1400 is configured at the factory with an internal sampling clock frequency that guarantees its minimum nominal record/playback time. For instance, an ISD1420 operating within specification will be observed to always have a minimum of 20 seconds of recording time. The sampling frequency is then maintained to a variation of ±2.25 percent over the commercial temperature and operating voltage ranges, while still maintaining the minimum specified recording duration. This will result in some devices having a few percent more than nominal recording time. The internal clock has a ±5 percent tolerance over the industrial temperature and voltage range. A regulated power supply is recommended for industrial temperature parts. If greater precision is required, the device can be clocked through the XCLK pin as follows: **EXTERNAL CLOCK SAMPLE RATES** Part Number / Sample Rate / Required Clock ISD1416 / 8.0 kHz / 1024 kHz ISD1420 / 6.4 kHz / 819.2 kHz These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. **If the XCLK is not used, this input must be connected to ground.**

PIN NAME	PIN NO	FUNCTION
$\overline{\text{REC}}$	27	**Record Input:** The $\overline{\text{REC}}$ input is an active-LOW record signal. The device records whenever $\overline{\text{REC}}$ is LOW. This signal must remain LOW for the duration of the recording. $\overline{\text{REC}}$ takes precedence over either playback ($\overline{\text{PLAYE}}$ or $\overline{\text{PLAYL}}$) signal. If $\overline{\text{REC}}$ is pulled LOW during a playback cycle, the playback immediately ceases and recording begins. A record cycle is completed when $\overline{\text{REC}}$ is pulled HIGH or the memory space is filled. And end-of-message marker (EOM) is internally recorded, enabling a subsequent playback cycle to terminate appropriately. The device automatically powers down to standby mode when $\overline{\text{REC}}$ goes HIGH.

Notes:

[1] The $\overline{\text{REC}}$ signal is debounced for 50 ms on the rising edge to prevent a false retriggering from a push-button switch.

[2] During playback, if either $\overline{\text{PLAYE}}$ or $\overline{\text{PLAYL}}$ is held LOW during EOM or OVF, the device will still enter into standby mode and the internal oscillator and timing generator will stop. However, the rising edge of $\overline{\text{PLAYE}}$ and $\overline{\text{PLAYL}}$ are not debounced and any subsequent falling edge (particularly switch bounce) present on the input pins will initiate another playback.

7. FUNCTIONAL DESCRIPTION

7.1. DETAILED DESCRIPTION

Speech/Sound Quality

The Winbond's ISD1400 series offer 6.4 and 8.0 kHz sampling frequencies, allowing the user a choice of speech quality options. The speech samples are stored directly into on-chip non-volatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solidstate digital solutions.

Duration

To meet end system requirements, the ISD1400 series offer single-chip solutions at 16 and 20 seconds.

TABLE 1: ISD1400 SERIES SUMMARY

Part Number	Duration (Seconds)	Input Sample Rate (kHz)	Typical Filter Pass Band* (kHz)
ISD1416	16	8.0	3.3
ISD1420	20	6.4	2.6

* 3dB roll-off-point

EEPROM Storage

One of the benefits of Winbond's ChipCorder® technology is the use of on-chip non-volatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

Basic Operation

The ISD1400 ChipCorder® series are controlled by a single control signal, $\overline{\text{REC}}$, $\overline{\text{PLAYE}}$ (edge-activated playback) or $\overline{\text{PLAYL}}$ (level-activated playback). The ISD1400 parts are configured for simplicity of design in a single/multiple-message application. Using the address lines will allow multiple message applications.

Automatic Power-Down Mode

At the end of a playback or record cycle, the ISD1400 series automatically return to a low-power standby mode, consuming typically 0.5 µA. After a playback cycle, the device powers down automatically at the end of the message. After a record cycle, the device powers down immediately after $\overline{\text{REC}}$ is pulled to HIGH.

Addressing

In addition to providing single message application, the ISD1400 series provide a full addressing capability.

The ISD1400 series have 160 distinct addressable segments, providing the below resolutions. See Application Information for ISD1400 address tables.

TABLE 2: DEVICE PLAYBACK/RECORD DURATIONS

Part Number	Minimum Duration (Seconds)
ISD1416	100 ms
ISD1420	125 ms

7.2. OPERATIONAL MODES

The ISD1400 series have several built-in operational modes providing maximum functionality with a minimal additional components. The operational modes use the address pins, but are mapped to outside the normal address range. When the two Most Significant Bits (MSBs), A6 and A7, are HIGH, the remaining address signals are interpreted as mode bits and not as address bits. Therefore, operational modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using operational modes. Firstly, all operations begin initially at address 0, which is the beginning address. Later operations can begin at other address locations, depending on the operational mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback but not from playback to record when A4 is HIGH in Operational Mode.

Secondly, an Operational Mode is executed when any of the control inputs, $\overline{\text{PLAYE}}$, $\overline{\text{PLAYL}}$ or $\overline{\text{REC}}$, goes LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going control input signal, at which point the current address/mode levels are sampled and executed.

7.2.1. Operational Modes Description

The Operational Modes can be used in conjunction with a microcontroller, or they can be hardwired to provice the desired system operation.

A0 – Message Cueing

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each LOW pulse causes the internal address pointer to skip to the next message. This mode is used for playback only and typically used with the A4 Operational Mode.

A1 – Delete $\overline{\text{EOM}}$ Markers

The A1 Operational Mode allows recording messages sequentially and playback as a single message with only one $\overline{\text{EOM}}$ set at the end of the final message.

A2 – Unused

A3 – Message Looping

The A3 Operational Mode allows repeating playback a message continuously from the beginning of the memory. A message can completely fill the ISD1400 device and will loop from beginning to end. Pulsing $\overline{\text{PLAYE}}$ will start the playback and pulsing $\overline{\text{PLAYL}}$ will end the playback.

A4 – Consecutive Addressing

During normal operation, the address pointer will reset when a message is played through to an $\overline{\text{EOM}}$ marker. The A4 Operational Mode inhibits the address pointer reset, allowing messages to be recorded or played back consecutively. When the device is in a static state; i.e., not recording or playback, momentarily taking this pin LOW will reset the address counter to zero.

A5 – Unsued

TABLE 3: OPERATIONAL MODES

Mode	Function	Typical Use	Jointly Compatible [1]
A0	Message cueing	Fast-forward through messages	A4
A1	Delete $\overline{\text{EOM}}$ markers	Position $\overline{\text{EOM}}$ marker at the end of the last message	A3, A4
A2	Unused		
A3	Looping	Continuous playback from Address 0	A1
A4	Consecutive addressing	Record/playback multiple consecutive messages	A0, A1
A5	Unused		

[1] Additional Operational Modes can be used simultaneously with the given mode.

8. TIMING DIAGRAMS

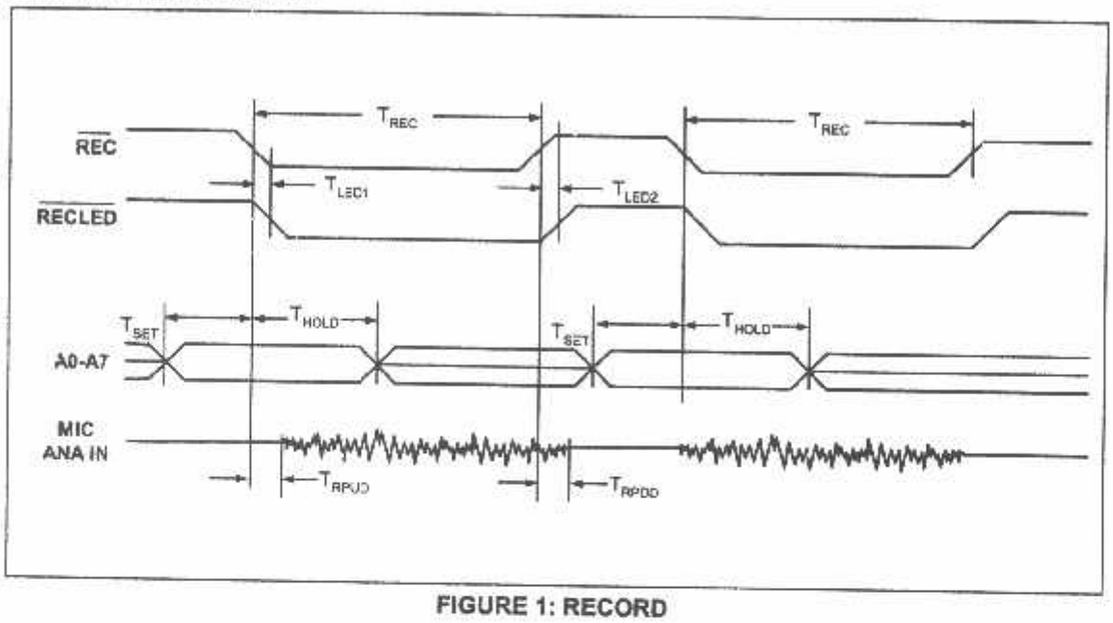


FIGURE 1: RECORD

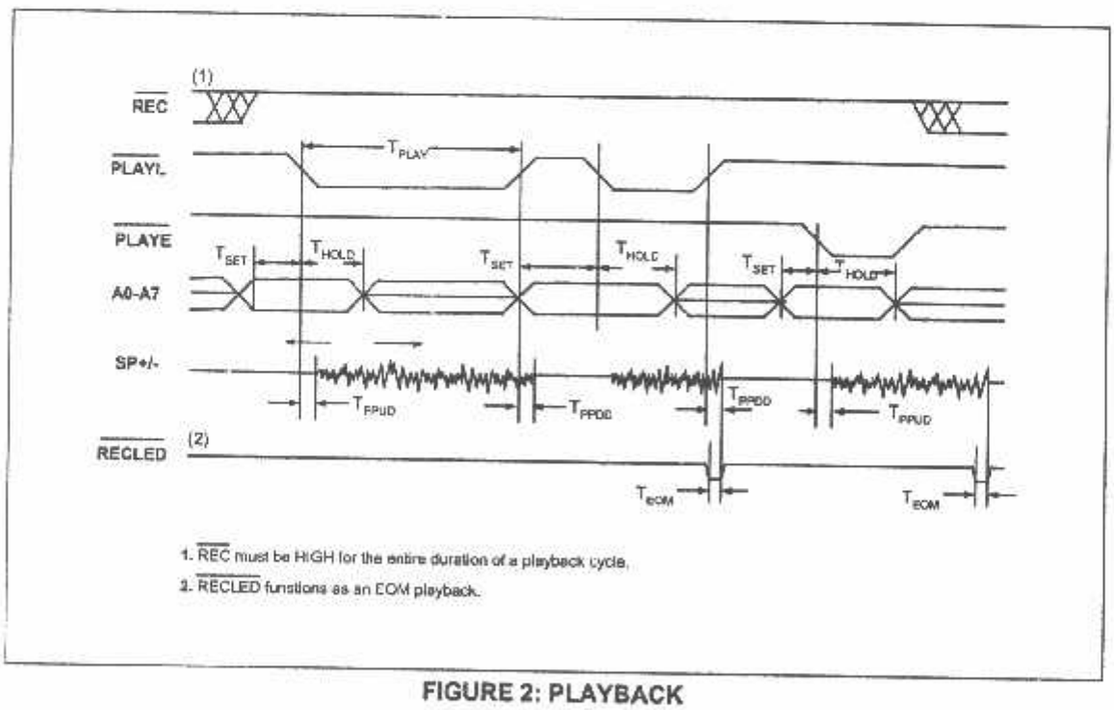


FIGURE 2: PLAYBACK

9. ABSOLUTE MAXIMUM RATINGS[2]

TABLE 4: ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)

CONDITIONS	VALUES
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3V) to (V_{CC} + 0.3V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} – 1.0V) to (V_{CC} + 1.0V)
Lead temperature (Soldering – 10sec)	300°C
V_{CC} – V_{SS}	-0.3V to +7.0V

TABLE 5: ABSOLUTE MAXIMUM RATINGS (DIE)

CONDITIONS	VALUES
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pad	(V_{SS} – 0.3V) to (V_{CC} + 0.3V)
Voltage applied to any pad (Input current limited to ±20mA)	(V_{SS} – 1.0V) to (V_{CC} + 1.0V)
Lead Temperature (soldering 10 seconds)	330° C
V_{CC} – V_{SS}	-0.3V to +7.0V

[2] Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability and performance. Functional operation is not implied at these conditions.

9.1 OPERATING CONDITIONS

TABLE 6: OPERATING CONDITIONS (PACKAGED PARTS)

CONDITIONS	VALUES
Commercial operating temperature range (Case temperature)	0°C to +70°C
Industrial operating temperature (Case temperature)	-40°C to +85°C
Supply voltage (V_{CC}) [1]	+4.5V to +5.5V
Ground voltage (V_{SS}) [2]	0V

TABLE 7: OPERATING CONDITIONS (DIE)

CONDITIONS	VALUES
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC}) [1]	+4.5V to +6.5V
Ground voltage (V_{SS}) [2]	0V

[1] $V_{CC} = V_{CCA} = V_{CCD}$

[2] $V_{SS} = V_{SSA} = V_{SSD}$

10. ELECTRICAL CHARACTERISTICS

10.1. PARAMETERS FOR PACKAGED PARTS

TABLE 8: DC PARAMETERS

PARAMETERS	SYMBOLS	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.4			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -1.6 mA
V_{CC} Current (Operating)	I_{CC}		15	30	mA	V_{CC} = 5.5V[3], R_{EXT} = ∞
V_{CC} Current (Standby)	I_{SB}		0.5	10	µA	[3] [4]
Input Leakage Current	I_{IL}			±1	µA	
Input Current HIGH w/Pull Down	I_{ILPD}			130	µA	Force V_{CC} [5]
Output Load Impedance	R_{EXT}	16			Ω	Speaker Load
Preamp IN Input Resistance	R_{MIC}	4	9	17	KΩ	Pins 17, 18
ANA IN Input Resistance	$R_{ANA\ IN}$	2.5	3	5	KΩ	
Preamp Gain 1	A_{PRE1}	20	23	26	dB	AGC = 0.0V
Preamp Gain 2	A_{PRE2}		-45	-15	dB	AGC = 2.5V
ANA IN to SP+/- Gain	A_{ARP}	20	22	25	dB	
AGC Output Resistance	R_{AGC}	2.5	5	9.5	KΩ	
Preamp Out Source	I_{PREH}		-2		mA	@ V_{OUT} = 1.0V
Preamp In Sink	I_{PREL}		0.5		mA	@ V_{OUT} = 2.0V

[1] Typical values @ T_A = 25° and 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electronical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} connected together.

[4] $\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be at V_{CCD}.

[5] XCLK pin.

TABLE 9: AC PARAMETERS

CHARACTERISTICS	SYMBOLS	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Sampling Frequency	F_S			8.0		
ISD1416				6.4	kHz	[5]
ISD1420					kHz	[5]
Filter Pass Band	F_{CF}					
ISD1416			3.3		kHz	3 dB Roll-Off Point[3][6]
ISD1420			2.6		kHz	3 dB Roll-Off Point[3][6]
Record Duration	T_{REC}					
ISD1416		16			sec	
ISD1420		20			sec	
Playback Duration	T_{PLAY}					
ISD1416		16			sec	[5]
ISD1420		20			sec	[5]
$\overline{\text{RECLED}}$ ON Delay	T_{LED1}		5		msec	
$\overline{\text{RECLED}}$ OFF Delay	T_{LED2}	30	38.9	95	msec	
ISD1416		40	48.6	110	msec	
ISD1420						
Address Setup Time	T_{SET}	300			nsec	
Address Hold Time	T_{HOLD}	0			nsec	
Record Power-Up Delay	T_{RPUD}					
ISD1416			26		msec	
ISD1420			32		msec	
Record Power-Down Delay	T_{RPDD}					
ISD1416			26		msec	
ISD1420			32		msec	
Play Power-Up Delay	T_{PPUD}					
ISD1416			26		msec	
ISD1420			32		msec	
Play Power-Down Delay	T_{PPDD}		6.5			
ISD1416			8.1		msec	
ISD1420					msec	

CHARACTERISTICS	SYMBOLS	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
EOM Pulse Width	T_{EOM}					
SD1416			12.5		msec	
SD1420			15.625		msec	
Total Harmonic Distortion	THD		1	3	%	@ 1 kHz
Speaker Output Power	P_{OUT}		12.2		mW	R_{EXT} = 16 Ω
Voltage Across Speaker Pins	V_{OUT}		1.25	2.5	V p-p	R_{EXT} = 600 Ω
MIC Input Voltage	V_{IN1}			20	mV	Peak-to-Peak[5]
ANA IN Input Voltage	V_{IN2}			50	mV	Peak-to-Peak

Notes:

[1] Typical values @ T_A = 25° and 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electronical testing or characterization. Not all specifications are 100 percent tested.

[3] Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions)

[4] With 5.1 K Ω series resistor at ANA IN.

[5] Sampling Frequency and playback duration can vary as much as ±2.25 percent over the commercial temperature and voltage rangs. It may vary as much as ±5 percent over the industrial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions)

[6] Filter specification applies to the anti-aliasing filter and the smoothing filter. Typical Parameter Variation with Voltage and Temperature. This parameter is not checked during production testing and may vary due to process variations and other factors. Therefore, the customer should not rely upon this value for testing purposes.

10.1.1. Typical Parameter Variation with Voltage and Temperature

Chart 1: Record Mode Operating Current (I_{CC})

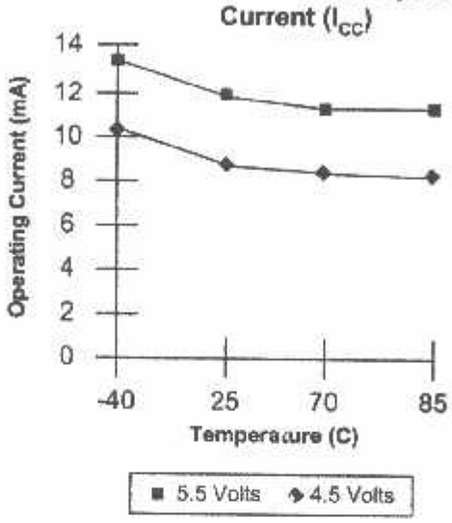


Chart 3: Standby Current (I_{SB})

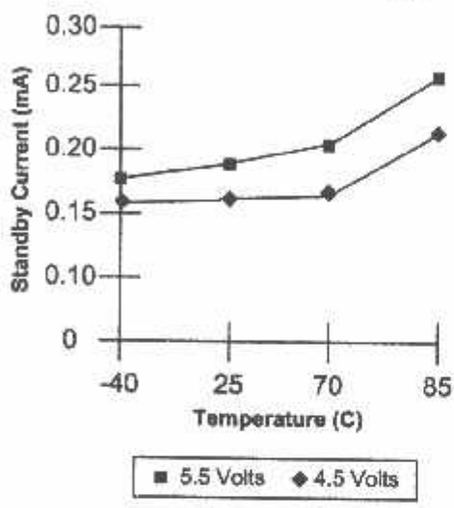


Chart 2: Total Harmonic Distortion

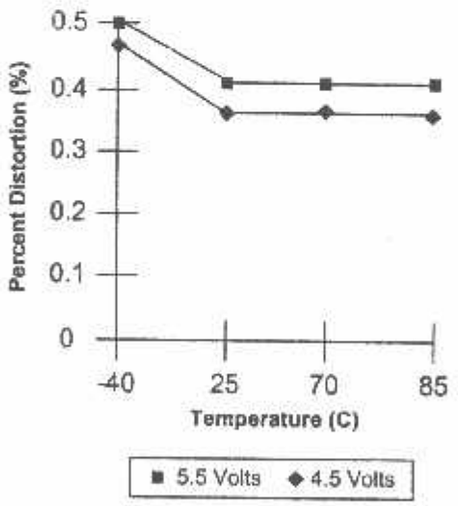
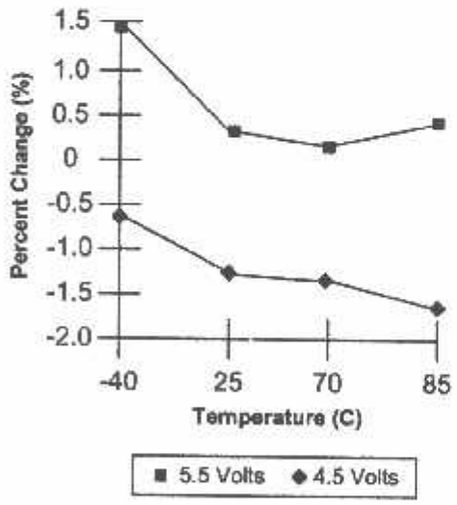


Chart 4: Oscillator Stability



10.2. PARAMETERS FOR DIE

TABLE 10: DC PARAMETERS

PARAMETERS	SYMBOLS	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.4			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -1.6 mA
V_{CC} Current (Operating)	I_{CC}		15	30	mA	V_{CC} = 5.5V[3], R_{EXT} = ∞
V_{CC} Current (Standby)	I_{SB}		0.5	10	µA	[3] [4]
Input Leakage Current	I_{IL}			±1	µA	
Input Current HIGH w/Pull Down	I_{ILPD}			130	µA	Force V_{CC} [5]
Output Load Impedance	R_{EXT}	16			Ω	Speaker Load
Preamp IN Input Resistance	R_{MIC}	4	9	17	KΩ	Pads 17,18
ANA IN Input Resistance	$R_{ANA\ IN}$	2.5	3	5	KΩ	
Preamp Gain 1	A_{PRE1}	20	23	26	dB	AGC = 0.0V
Preamp Gain 2	A_{PRE2}		-45	-15	dB	AGC = 2.5V
ANA IN to SP+/- Gain	A_{ARP}	20	22	25	dB	
AGC Output Resistance	R_{AGC}	2.5	5	9.5	KΩ	
Preamp Out Source	I_{PREH}		-2		mA	@ V_{OUT} = 1.0V
Preamp In Sink	I_{PREL}		0.5		mA	@ V_{OUT} = 2.0V

[1] Typical values @ T_A = 25° and 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electronical testing or characterization. Not all specifications are 100 percent tested.

[3] V_{CCA} and V_{CCD} connected together.

[4] $\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be at V_{CCD}.

[5] XCLK pin.

TABLE 11: AC PARAMETERS

CHARACTERISTICS	SYMBOLS	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Sampling Frequency	F_S					
ISD1416			8.0		kHz	[5]
ISD1420			6.4		kHz	[5]
Filter Pass Band	F_{CF}					
ISD1416			3.3		kHz	3 dB Roll-Off Point[3][6]
ISD1420			2.6		kHz	3 dB Roll-Off Point[3][6]
Record Duration	T_{REC}					
ISD1416		16			sec	
ISD1420		20			sec	
Playback Duration	T_{PLAY}					
ISD1416		16			sec	
ISD1420		20			sec	
$\overline{\text{RECLED}}$ ON Delay	T_{LED1}		5		msec	
$\overline{\text{RECLED}}$ OFF Delay	T_{LED2}					
ISD1416		30	38.9	95	msec	
ISD1420		40	48.6	110	msec	
Address Setup Time	T_{SET}	300			nsec	
Address Hold Time	T_{HOLD}	0			nsec	
Power-Up Delay	T_{RPUD}					
ISD1416			26		msec	
ISD1420			32		msec	
PD Pulse Width (Record)	T_{RPUD}					
ISD1416			26		msec	
ISD1420			32		msec	
PD Pulse Width (Play)	T_{PPUD}					
ISD1416			6.5		msec	
ISD1420			8.1		msec	
Play Power-Down Delay	T_{PPDD}					
ISD1416			6.5		msec	
ISD1420			8.1		msec	

CHARACTERISTICS	SYMBOLS	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
$\overline{EOM}$ Pulse Width ISD1416 ISD1420	T_{EOM}		 12.5 15.625		 msec msec	
Total Harmonic Distortion	THD		1	3	%	@ 1 kHz
Speaker Output Power	P_{OUT}		12.2		mW	R_{EXT} = 16 Ω[4]
Voltage Across Speaker Pins	V_{OUT}		1.25	2.5	V p-p	R_{EXT} = 600 Ω
MIC Input Voltage	V_{IN1}			20	mV	Peak-to-Peak[4]
ANA IN Input Voltage	V_{IN2}			50	mV	Peak-to-Peak

Notes:

[1] Typical values @ T_A = 25° and 5.0V.

[2] All Min/Max limits are guaranteed by Winbond via electronical testing or characterization. Not all specifications are 100 percent tested.

[3] Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions)

[4] With 5.1 K Ω series resistor at ANA IN.

[5] Sampling Frequency and playback duration can vary as much as ±2.25 percent over the commercial temperature and voltage rangs. It may vary as much as ±5 percent over the industrial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions)

[6] Filter specification applies to the anti-aliasing filter and the smoothing filter. Typical Parameter Variation with Voltage and Temperature. This parameter is not checked during production testing and may vary due to process variations and other factors. Therefore, the customer should not rely upon this value for testing purposes.

10.2.1. Typical Parameter Variation with Voltage and Temperature

Chart 5: Record Mode Operating Current (I_{CC})

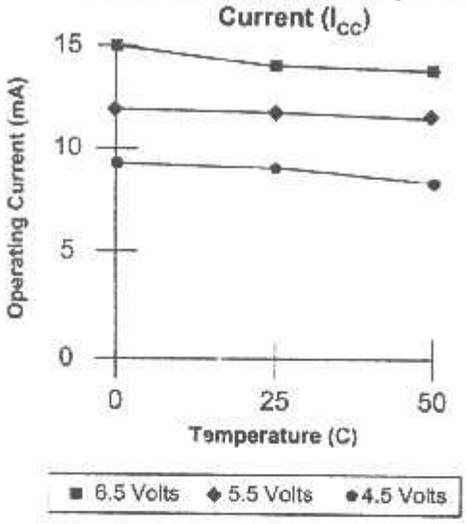


Chart 7: Standby Current (I_{SB})

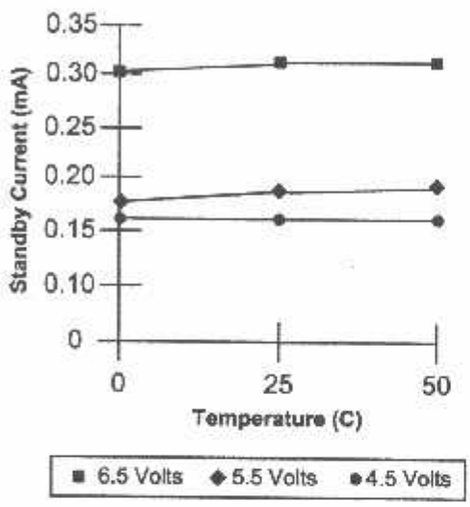


Chart 6: Total Harmonic Distortion

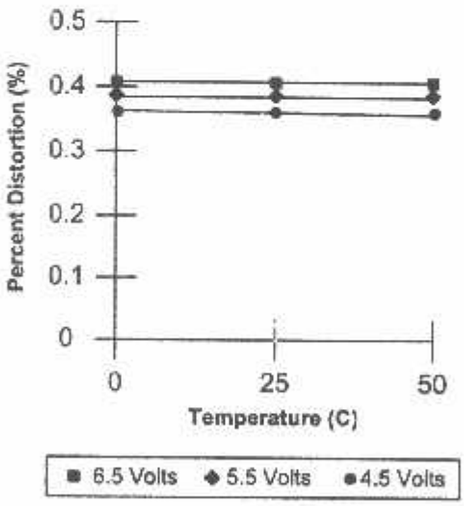
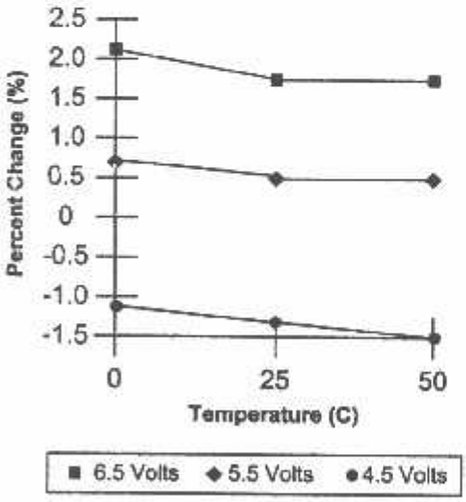


Chart 8: Oscillator Stability



11. TYPICAL APPLICATION CIRCUIT

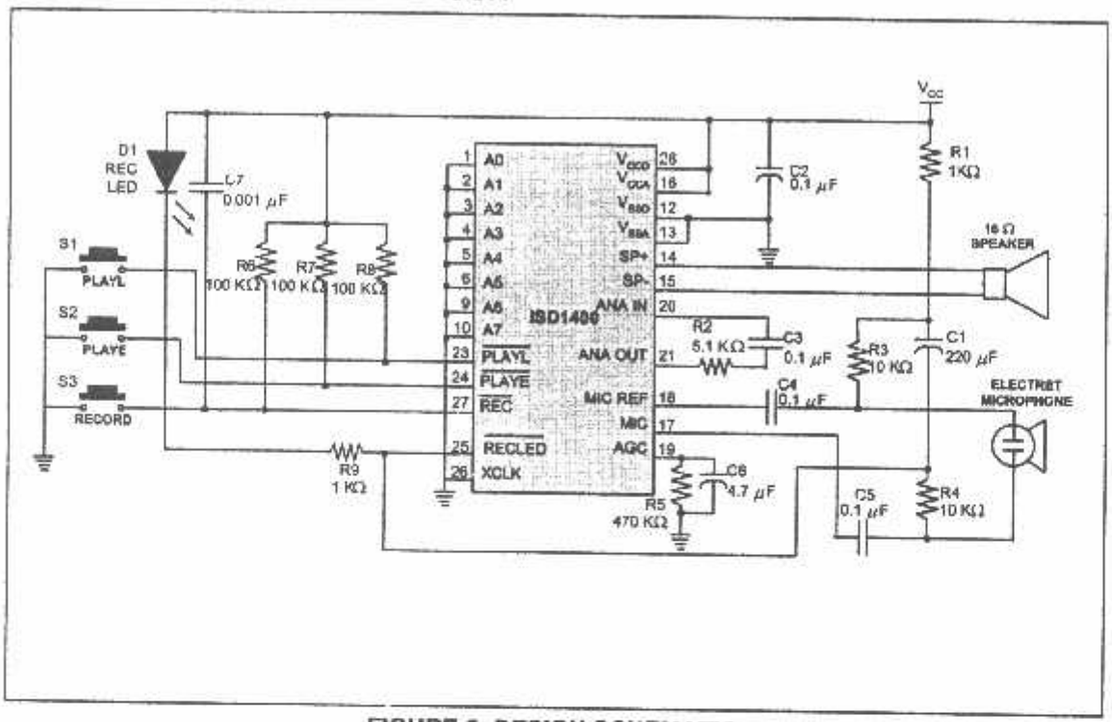


FIGURE 5: DESIGN SCHEMATIC

Functional Description Example

The following operating examples demonstrate the functionality of the ISD1400 series.

1. Record a message:

   Pulling the $\overline{REC}$ signal LOW initiates a record cycle from current location. When $\overline{REC}$ is held LOW, the recording continues. Until the memory array is filled up or when $\overline{REC}$ is pulled HIGH, recording ceases. An EOM marker is written at the end of message. Then the device will automatically power down.

2. Edge-activated playback:

   Pulling the $\overline{PLAYE}$ signal LOW initiates a playback cycle from the beginning of the message until the entire message is played. The rising edge of $\overline{PLAYE}$ has no effect on operation. When the EOM marker is encountered, the device automatically powers down. A subsequent falling edge on $\overline{PLAYE}$ initiates a new playback operation from the beginning of the message.

3. Level-activated playback:

   Holding the $\overline{PLAYL}$ signal LOW initiates a playback cycle from the beginning of the message, until $\overline{PLAYL}$ is pulled HIGH or when the EOM marker is encountered, playback operation stops and the device automatically powers down.

4. Record (interrupting playback).

   The $\overline{REC}$ signal takes precedence over playback operation. Holding $\overline{REC}$ LOW initiates a new record operation from current location, regardless of any current operation in progress.

5 $\overline{RECLED}$ operation.

   During record, the $\overline{RECLED}$ output pin provides an active-LOW signal, which can be used to drive an LED as a "record- n-progress" indicator. It returns to a HIGH state when the $\overline{REC}$ pin is pulled HIGH or when the recording is completed due to the memory being filled. However, during playback, this pin also pulses LOW to indicate an EOM at the end of a message.

Applications Note

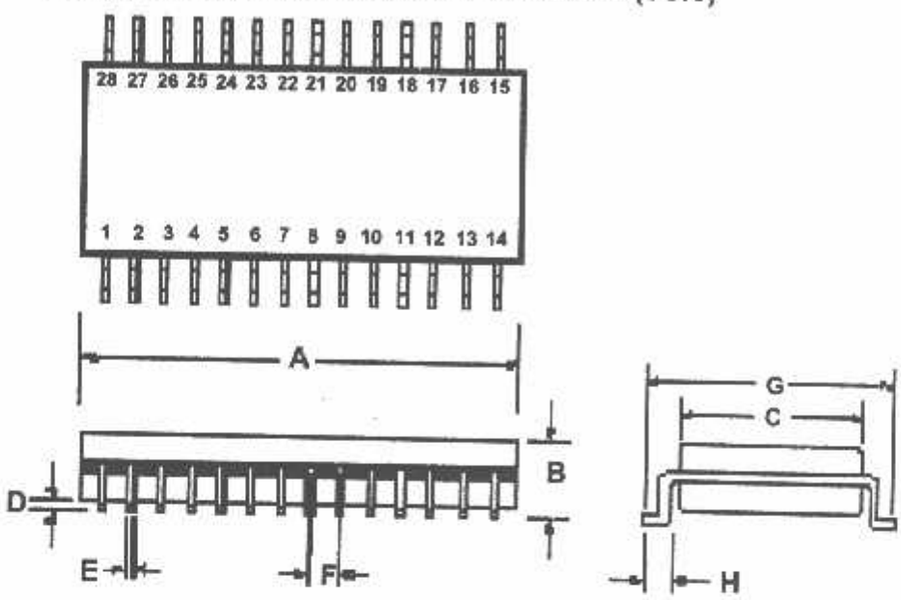
Some users may experience an unexpected recording taking place when their circuit is powered up, or the batteries are changed and V_{CC} rises faster than $\overline{REC}$. This undesired recording prevents playback of the previously recordec message. A spurious End Of Message (EOM) marker appears at the very beginning of the memory, preventing access to the original message, and nothing is played.

To prevent this occurrence, place a capacitor (approx. 0.001 µF) between the control pin ($\overline{REC}$) and V_{CC}. This pulls the control pin voltage up with V_{CC} as it rises. Once the voltage is HIGH, the pull-up device will keep the pin HIGH until intentionally pulled LOW, preventing the false EOM marker.

Since this anomaly depends on factors such as the capacitance of the user's printed circuit board, not all circuit designs will exhibit the spurious marker. However, it is recommended that the capacitor is included for design reliability. A more detailed explanation and resolution of this occurrence is described in Application Information.

12. PACKAGE DRAWING AND DIMENSIONS

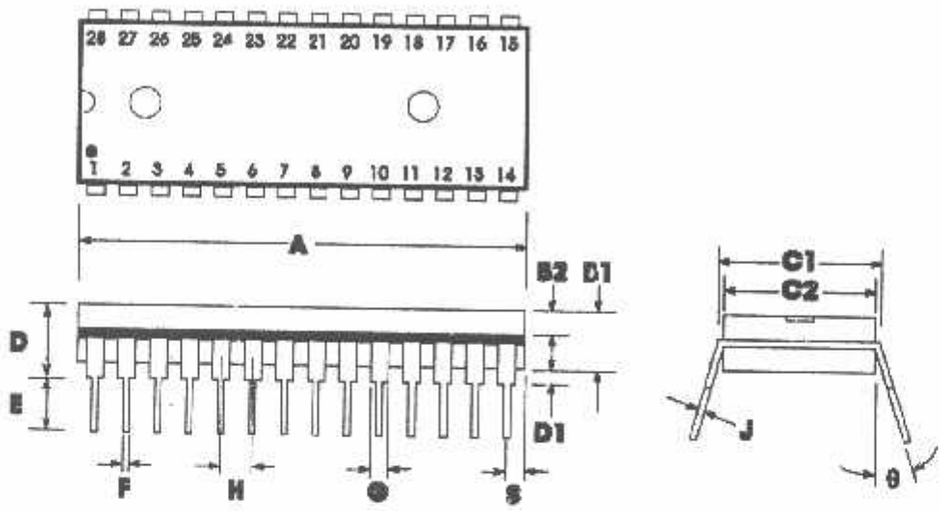
12.1. 28-LEAD 300 MIL PLASTIC SMALL OUTLINE IC (SOIC)



	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

Note: Lead coplanarity to be with n 0.004 inches.

12.2. 28-LEAD 600 MIL PLASTIC DUAL INLINE PACKAGE (PDIP)

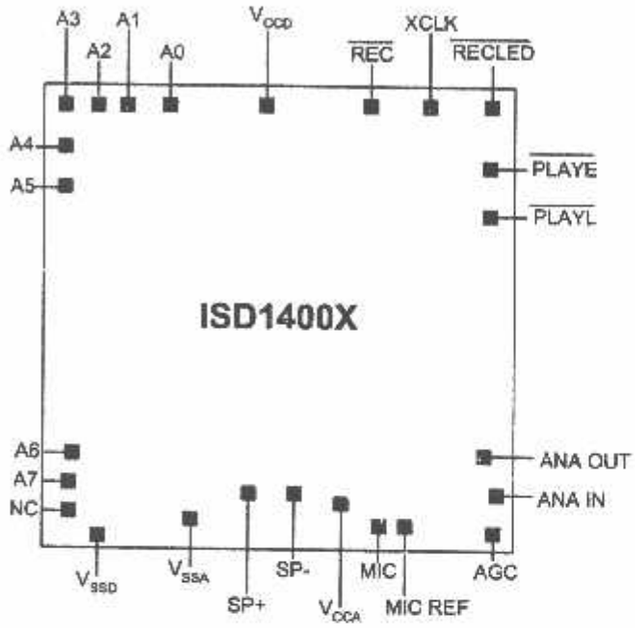


	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.62
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

12.3. Die Physical Layout [1]

ISD1400x

- Die Dimensions
  X: 172.2 ± 1 mils
  Y: 168.5 ± 1 mils
- Die Thickness[2]
  17.5 ± 1 mils
- Pad Opening
  100 x 112 microns
  3.9 x 4.4 mils



Notes:

[1] The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.

[2] Die thickness is subject to change, please contact Winbond factory for status and availability.

Winbond Electronics Corp.

ISD1400 SERIES PAD DESIGNATIONS

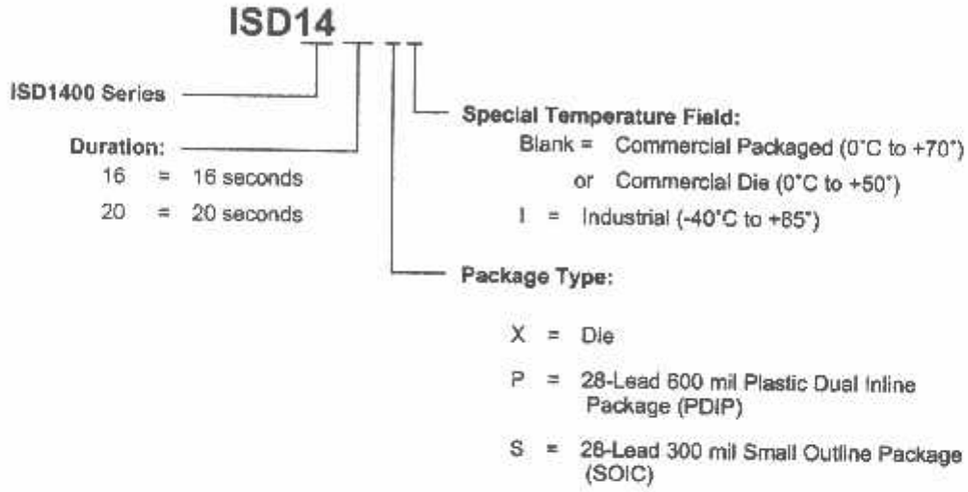
(with respect to die center)

Pad	Pad Name	X Axis (µm)	Y Axis (µm)
A0	Address 0	-1332.5	1973.8
A1	Address 1	-1628.9	1973.8
A2	Address 2	-1808.9	1973.8
A3	Address 3	-2014.1	1910.2
A4	Address 4	-2014.1	1722.6
A5	Address 5	-2014.1	1519.8
A6	Address 6	-2014.1	-1214.6
A7	Address 7	-2014.1	-1399.8
NC	No Connect	-2014.1	-1745.4
V_{SSD}	Digital Ground	-1894.1	-1971.8
V_{SSA}	Analog Ground	-358.1	-1971.8
SP+	Speaker Output +	-17.7	-1896.6
SP-	Speaker Output -	411.9	-1896.6
V_{CCA}	Analog Power Supply	779.5	-1936.2
MIC	Microphone Input	991.5	-1973.8
MIC REF	Microphone Reference	1168.7	-1973.8
AGC	Automatic Gain Control	1977.9	-1910.6
ANA IN	Analog Input	2005.1	-1580.2
ANA OUT	Analog Output	1990.7	-1379.0
$\overline{\text{PLAYL}}$	Level-Activated Playback	2013.9	1608.6
$\overline{\text{PLAYE}}$	Edge-Activated Playback	2013.9	1777.0
$\overline{\text{RECLED}}$	Record LED Output	2011.9	1971.8
XCLK	External Clock	1580.7	1973.8
$\overline{\text{REC}}$	Record	752.3	1973.8
V_{CCD}	Digital Power Supply	-48.5	1929.4

Note: Die dimensions and pad positions may be subjected to change. Please contact Winbond Sales Offices or Representatives to verify current or future specifications.

13. ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD1400 Series devices, please refer to the following valid part numbers.

Die / Package	16-Second		20-Second	
	Product P/N	Ordering P/N	Product P/N	Ordering P/N
Die	ISD1416X C5006	I1416X5006	ISD1420X C5006	I1420X5006
PDIP	ISD1416P C5006	I1416P5006	ISD1420P C5006	I1420P5006
	ISD1416PI C5006	I1416PI5006	ISD1420PI C5006	I1420PI5006
SOIC	ISD1416S C5006	I1416S5006	ISD1420S C5006	I1420S5006
	ISD1416SI C5006	I1416SI5006	ISD1420SI C5006	I1420SI5006

For the latest product information, access Winbond's worldwide website at
http://www.winbond-usa.com

14. VERSION HISTORY

VERSION	DATE	DESCRIPTION
0	Before 2004	Initial issue.
1.0	March 2004	Reformat the document. Revise footnote for Filter Passband in Tables 1, 9 & 11. Revise Functional Description Example section. Revise die picture. Revise ordering information.
1.1	Apr 2005	Revise the disclaim section.
1.2	Jun 2005	Revise the part number for I1420 device in Ordering section.

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Information contained in this ISD® ChipCorder® datasheet supersedes all data for the ISD ChipCorder products published by ISD® prior to August, 1998.

This datasheet and any future addendum to this datasheet is(are) the complete and controlling ISD® ChipCorder® product specifications. In the event any inconsistencies exist between the information in this and other product documentation, or in the event that other product documentation contains information in addition to the information in this, the information contained herein supersedes and governs such other information in its entirety. This datasheet is subject to change without notice.

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FAX: 852-27552064

INTRODUCTION

KS0070B is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology. It is capable of displaying 1 or 2 lines with the 5×7 format or 1 line with the 5×10 dots format.

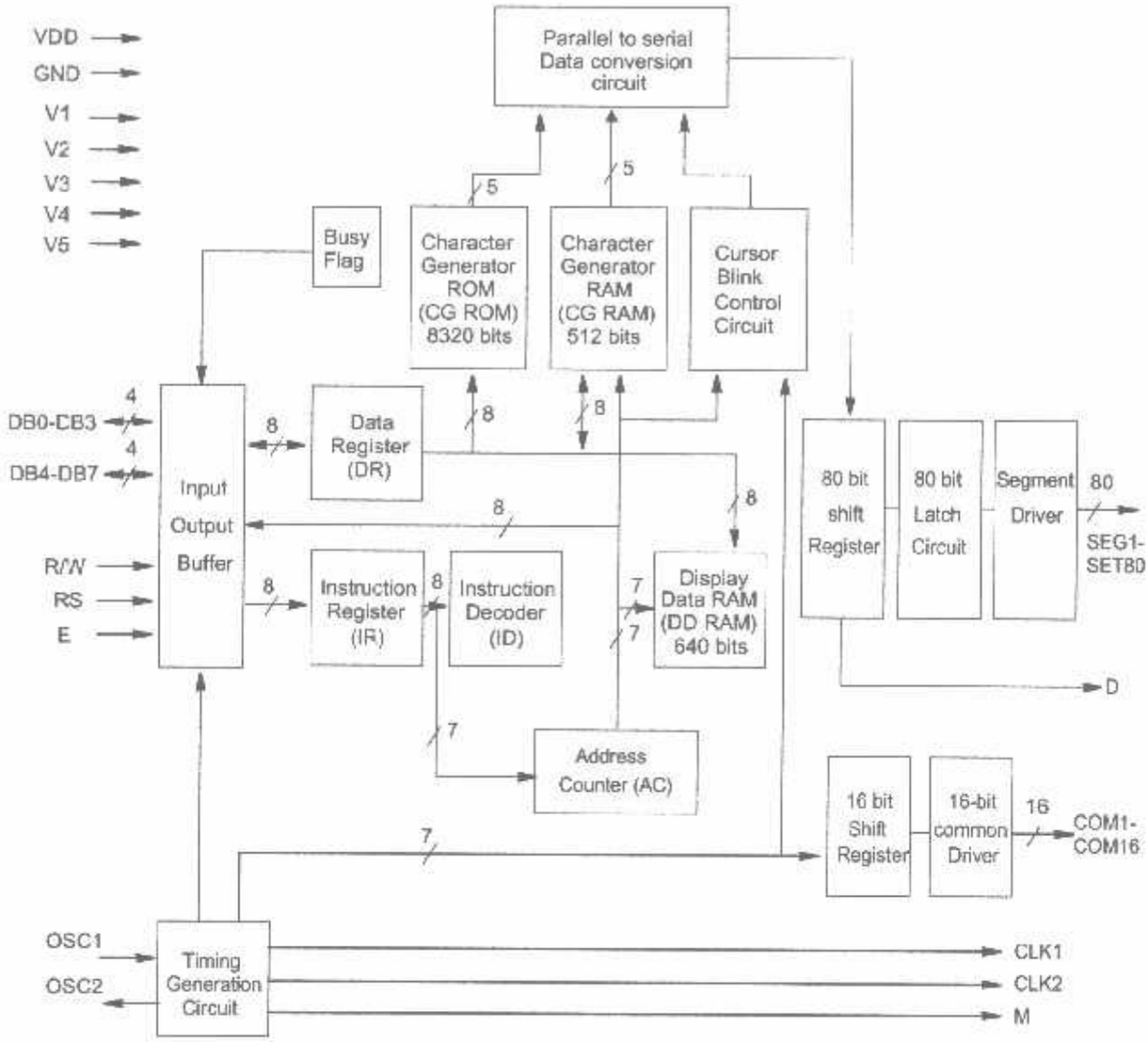
FUNCTIONS

- Character type dot matrix LCD driver & controller
- Internal driver: 16 common and 80 segment signal output
- Easy interface with 4-bit or 8-bit MPU
- Display character pattern: 5×7 dots format (192 kinds) & 5×10 dots format (32 kinds)
- The special character pattern is directly programmable by the character generator RAM.
- A customer character pattern is programmable by mask option.
- It can drive a maximum of 80 characters by using the KS0065B or KS0063B externally.
- Varicus instruction functions
- Built-in automatic power on reset
- Driving method is A-type (Line inversion)

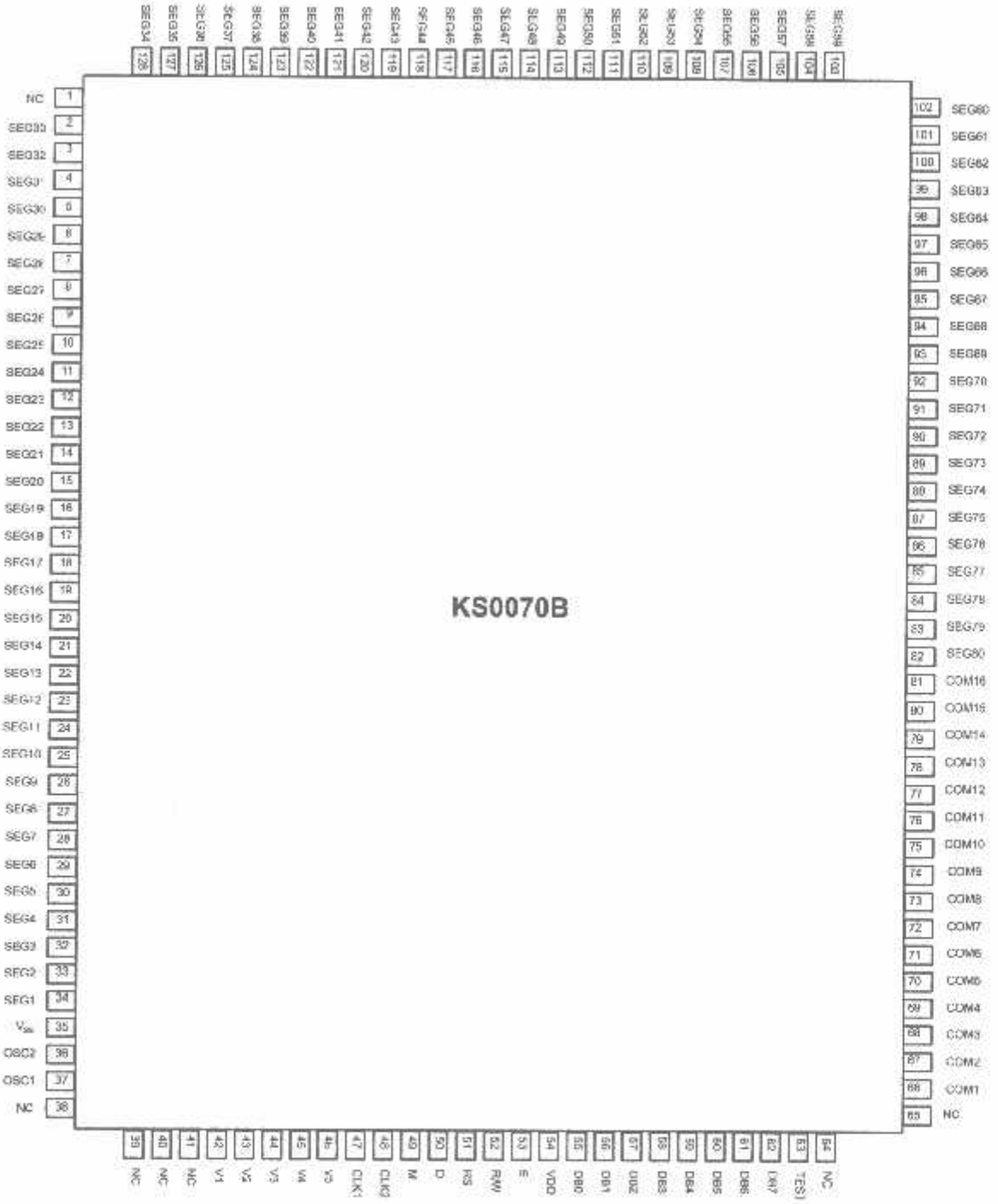
FEATURES

- Internal Memory
  - Character Generator ROM (CGROM): 8,320 bits (192 characters × 5 × 7 dots) & (32 characters x 5 × 10 dots)
  - Character Generator RAM (CGRAM): 64 × 8 bits (8 characters × 5 × 7 dots)
  - Display Data RAM (DDRAM): 80 × 8 bits (80 characters max.)
- Low power operation
  - Power supply voltage range: 2.7 to 5.5 V (VDD)
  - LCD Drive voltage range: 3.0 to 10.0 V (VDD to V5)
- Supply voltage for display: 0 to −5 V (V5)
- Programmable duty cycle: 1/8, 1/11, 1/16
- Interral oscillator with an external resistor
- Bare chip or bumped chip available

BLOCK DIAGRAM

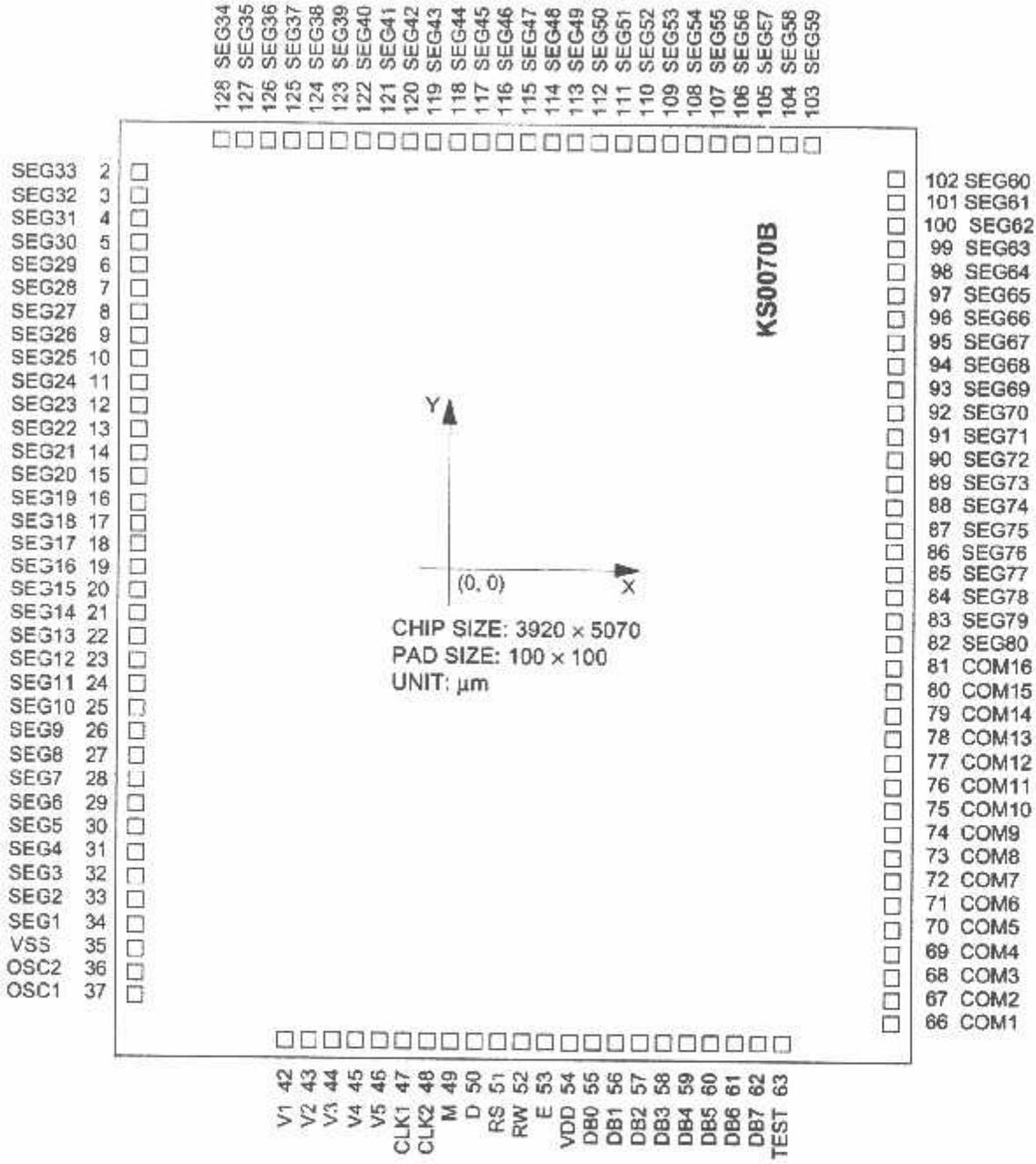


PIN CONFIGURATION

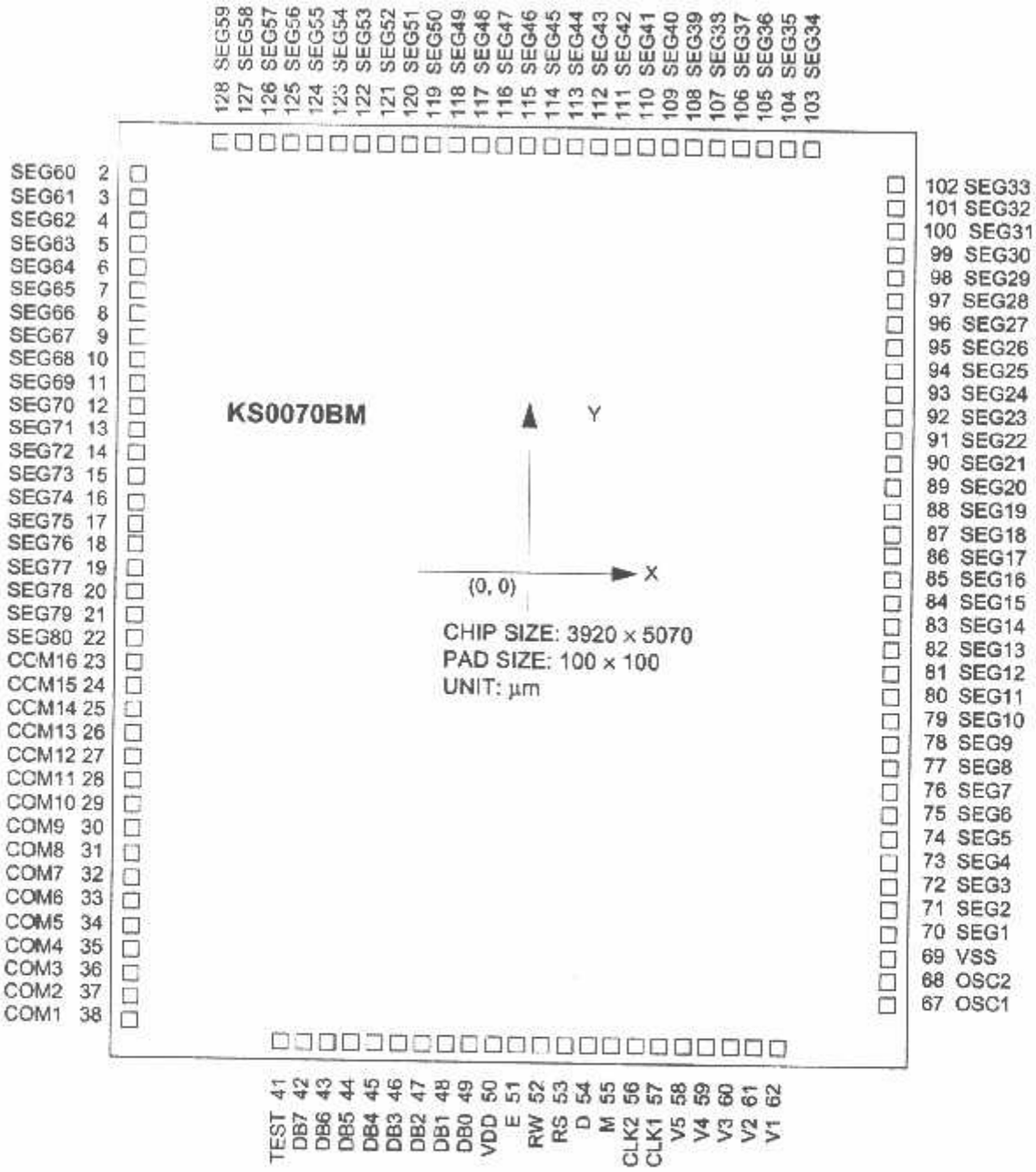


PAD CONFIGURATION

I) NORMAL TYPE PAD CONFIGURATION



2) MIRROR TYPE PAD CONFIGURATION



PAD COORDINATE

1) NORMAL TYPE PAD COORDINATE

PAD NO.	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE		PAD NO	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y			X	Y
1	NC	-	-	24	SEG11	-1794	-581	47	CLK1	-530	-2369	70	COM5	1794	-1831
2	SEG33	-1794	2169	25	SEG10	-1794	-706	48	CLK2	-405	-2369	71	COM6	1794	-1706
3	SEG32	-1794	2044	26	SEG9	-1794	-831	49	M	-280	-2369	72	COM7	1794	-1581
4	SEG31	-1794	1919	27	SEG8	-1794	-956	50	D	-155	-2369	73	COM8	1794	-1456
5	SEG30	-1794	1794	28	SEG7	-1794	-1081	51	RS	-30	-2369	74	COM9	1794	-1331
6	SEG29	-1794	1669	29	SEG6	-1794	-1206	52	RW	95	-2369	75	COM10	1794	-1206
7	SEG28	-1794	1544	30	SEG5	-1794	-1331	53	E	220	-2369	76	COM11	1794	-1081
8	SEG27	-1794	1419	31	SEG4	-1794	-1456	54	VDD	345	-2369	77	COM12	1794	-956
9	SEG26	-1794	1294	32	SEG3	-1794	-1581	55	DB0	470	-2369	78	COM13	1794	-831
10	SEG25	-1794	1169	33	SEG2	-1794	-1706	56	DB1	595	-2369	79	COM14	1794	-706
11	SEG24	-1794	1044	34	SEG1	-1794	-1831	57	DB2	720	-2369	80	COM15	1794	-581
12	SEG23	-1794	919	35	VSS	-1794	-1956	58	DB3	845	-2369	81	COM16	1794	-456
13	SEG22	-1794	794	36	OSC2	-1794	-2106	59	DB4	970	-2369	82	SEG80	1794	-331
14	SEG21	-1794	669	37	OSC1	-1794	-2231	60	DB5	1095	-2369	83	SEG79	1794	-206
15	SEG20	-1794	544	38	NC	-	-	61	DB6	1220	-2369	84	SEG78	1794	-81
16	SEG19	-1794	419	39	NC	-	-	62	DB7	1345	-2369	85	SEG77	1794	44
17	SEG18	-1794	294	40	NC	-	-	63	TEST	1470	-2369	86	SEG76	1794	169
18	SEG17	-1794	169	41	NC	-	-	64	NC	-	-	87	SEG75	1794	294
19	SEG16	-1794	44	42	V1	-1155	-2369	65	NC	-	-	88	SEG74	1794	419
20	SEG15	-1794	-81	43	V2	-1030	-2369	66	COM1	1794	-2331	89	SEG73	1794	544
21	SEG14	-1794	-206	44	V3	-905	-2369	67	COM2	1794	-2206	90	SEG72	1794	669
22	SEG13	-1794	-331	45	V4	-780	-2369	68	COM3	1794	-2081	91	SEG71	1794	794
23	SEG12	-1794	-456	46	V5	-655	-2369	69	COM4	1794	-1956	92	SEG70	1794	919

NORMAL TYPE PAD COORDINATE (CONTINUED)

PAD NO.	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y			X-	Y-
93	SEG69	1794	1044	102	SEG60	1794	2169	111	SEG51	563	2369	120	SEG42	-562	2369
94	SEG68	1794	1169	103	SEG59	1563	2369	112	SEG50	438	2369	121	SEG41	-687	2369
95	SEG67	1794	1294	104	SEG58	1438	2369	113	SEG49	313	2369	122	SEG40	-812	2319
96	SEG66	1794	1419	105	SEG57	1313	2369	114	SEG48	188	2369	123	SEG39	-937	2369
97	SEG65	1794	1544	106	SEG56	1188	2369	115	SEG47	63	2369	124	SEG38	-1062	2369
98	SEG64	1794	1669	107	SEG55	1063	2369	116	SEG46	-62	2369	125	SEG37	-1187	2369
99	SEG63	1794	1794	108	SEG54	938	2369	117	SEG45	-187	2369	127	SEG36	-1312	2369
100	SEG62	1794	1919	109	SEG53	813	2369	118	SEG44	-312	2369	127	SEG35	-1437	2369
101	SEG61	1794	2044	110	SEG52	688	2369	119	SEG43	-437	2369	128	SEG34	-1562	2369

2) MIRROR TYPE PAD COORDINATE

PAD NO.	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE		PAD NO	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y			X	Y
1	NC	-	-	24	COM15	-1794	-581	47	DB2	-720	-2369	70	SEG1	1794	-1831
2	SEG60	-1794	2169	25	COM14	-1794	-706	48	DB1	-595	-2369	71	SEG2	1794	-1706
3	SEG61	-1794	2044	26	COM13	-1794	-831	49	DB0	-470	-2369	72	SEG3	1794	-1581
4	SEG62	-1794	1919	27	COM12	-1794	-956	50	VDD	-345	-2369	73	SEG4	1794	-1456
5	SEG63	-1794	1794	28	COM11	-1794	-1081	51	E	-220	-2369	74	SEG5	1794	-1331
6	SEG64	-1794	1669	29	COM10	-1794	-1206	52	RW	-95	-2369	75	SEG6	1794	-1206
7	SEG65	-1794	1544	30	COM9	-1794	-1331	53	RS	30	-2369	76	SEG7	1794	-1081
8	SEG66	-1794	1419	31	COM8	-1794	-1456	54	D	155	-2369	77	SEG8	1794	-956
9	SEG67	-1794	1294	32	COM7	-1794	-1581	55	M	280	-2369	78	SEG9	1794	-831
10	SEG68	-1794	1169	33	COM6	-1794	-1706	56	CLK2	405	-2369	79	SEG10	1794	-706
11	SEG69	-1794	1044	34	COM5	-1794	-1831	57	CLK1	530	-2369	80	SEG11	1794	-581
12	SEG70	-1794	919	35	COM4	-1794	-1956	58	V5	655	-2369	81	SEG12	1794	-456
13	SEG71	-1794	794	36	COM3	-1794	-2081	59	V4	780	-2369	82	SEG13	1794	-331
14	SEG72	-1794	669	37	COM2	-1794	-2206	60	V3	905	-2369	83	SEG14	1794	-206
15	SEG73	-1794	544	38	COM1	-1794	-2331	61	V2	1030	-2369	84	SEG15	1794	-81
16	SEG74	-1794	419	39	NC	-	-	62	V1	1155	-2369	85	SEG16	1794	44
17	SEG75	-1794	294	40	NC	-	-	63	NC	-	-	86	SEG17	1794	169
18	SEG76	-1794	169	41	TEST	-1470	-2369	64	NC	-	-	87	SEG18	1794	294
19	SEG77	-1794	44	42	DB7	-1345	-2369	65	NC	-	-	88	SEG19	1794	419
20	SEG78	-1794	-81	43	DB6	-1220	-2369	66	NC	-	-	89	SEG20	1794	544
21	SEG79	-1794	-206	44	DB5	-1095	-2369	67	OSC1	1794	-2231	90	SEG21	1794	669
22	SEG80	-1794	-331	45	DB4	-970	-2369	68	OSC2	1794	-2106	91	SEG22	1794	794
23	COM16	-1794	-456	46	DB3	-845	-2369	69	VSS	1794	-1956	92	SEG23	1794	919

MIRROR TYPE PAD COORDINATE (CONTINUED)

PAD NO.	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE		PAD NO.	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y			X	Y
93	SEG24	1794	1044	102	SEG33	1794	2169	111	SEG42	562	2369	120	SEG51	-563	2369
94	SEG25	1794	1169	103	SEG34	1562	2369	112	SEG43	437	2369	121	SEG52	-688	2369
95	SEG26	1794	1294	104	SEG35	1437	2369	113	SEG44	312	2369	122	SEG53	-813	2369
96	SEG27	1794	1419	105	SEG36	1312	2369	114	SEG45	187	2369	123	SEG54	-938	2369
97	SEG28	1794	1544	106	SEG37	1187	2369	115	SEG46	62	2369	124	SEG55	-1063	2369
98	SEG29	1794	1669	107	SEG38	1062	2369	116	SEG47	-63	2369	125	SEG56	-1188	2369
99	SEG30	1794	1794	108	SEG39	937	2369	117	SEG48	-188	2369	127	SEG57	-1313	2369
100	SEG31	1794	1919	109	SEG40	812	2369	118	SEG49	-313	2369	127	SEG58	-1438	2369
101	SEG32	1794	2044	110	SEG41	687	2369	119	SEG50	-438	2369	128	SEG59	-1563	2369

PAD DESCRIPTION

Pad No. (Normal/Mirror)	Input/ Output	Name	Description	Interface
VDD (54/50)	-	Power supply	For logical circuit (+3 V, + 5 V)	Power Supply
VSS(35, 69)			0 V (GND)	
V1 ~ V5 (42~46/62~58)			Bias voltage level for LCD driving.	
SEG1 ~ SEG80 (34~2, 128~82/ 70~128, 2~22)	Output	Segment output	Segment signal output for LCD drive.	LCD
COM1 ~ COM16 (66~81/38~23)	Output	Common output	Common signal output for LCD drive.	LCD
OSC1,OSC2 (37,36/67,68)	Input (OSC1)/ Output (OSC2)	Oscillator	When using internal oscillator, connect external Rf resistor. If external clock is used, connect it to OSC1.	External resistor/ oscillator (OSC1)
CLK1,CLK2 (47,48/57,56)	Output	Extension driver Latch (CLK1)/Shift (CLK2) clock	Each outputs extension driver latch clock and extension driver shift clock.	Extension driver
M (49/55)	Output	Alternated signal for LCD driver output	Outputs the alternating signal to convert LCD driver waveform to AC.	Extension driver
D (50/54)	Output	Display data interface	Output extension driver data (the 41st dot's data)	Extension driver
RS (51/53)	Input	Register select	Used as register selection input. When RS = "1", Data register is selected. When RS = "0", Instruction register is selected.	MPU
RW (52/52)	Input	Read/Write	Used as read/write selection input. When RW = "1", read operation. When RW = "0", write operation.	MPU
E (53/51)	Input	Read/Write enable	Used as read. Write enable signal.	MPU
DB0~DB3 (55~58/49~46)	Input / Output	Data bus 0~7	When 8-bit bus mode, used as low order bidirectional data bus. During 4-bit bus mode open these pins.	MPU
DB4~DB7 (59~62/45~42)			When 8-bit bus mode, used as high order bidirectional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 used for Busy Flag output.	MPU
TEST (63/41)	Input	Test Pin	This pin must be fixed to VDD or open.	–

FUNCTION DESCRIPTION

System Interface

This chip has both kinds of interface type with MPU: 4-bit bus and 8-bit bus.
4-bit bus and 8-bit bus are selected by the DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is the data register (DR), and the other is the instruction register (IR).

The data register (DR) is used as a temporary data storage place for being written into or read from DDRAM/CGRAM. Target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.
After MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register (IR) is used only to store instruction codes transferred from MPU. MPU cannot use it to read instruction data.

To select a register, use RS input pin in 4-bit/8-bit bus mode.

Table 1. Various Kinds of Operations According to RS and R/W bits.

RS	R/W	Operation
0	0	Instruction Write operation (MPU writes Instruction code into IR)
0	1	Read Busy flag (DB7) and address counter (DB0 ~ DB6)
1	0	Data Write operation (MPU writes data into DR)
1	1	Data Read operation (MPU reads data from DR)

Busy Flag (BF)

When BF = "1", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = "0" and R/W = "1"
(Read Instruction Operation), through DB7 port.
Before executing the next instruction, be sure that BF is not "1".

Address Counter (AC)

The Address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.
After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = "0" and R/W = "1", AC can be read through ports DB0~DB6.

Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters).
DDRAM address is set in the address counter (AC) as a hexadecimal number. (Refer to Fig-1.)

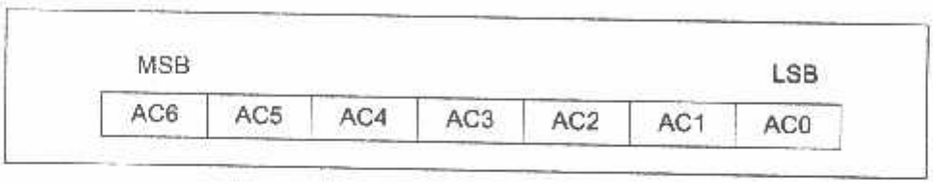


Fig-1. DDRAM Address

1) 1-line display

In the case of a 1-line display, the address range of DDRAM is 00H ~ 4FH.
An Extension driver will be used. Fig-2 shows the example when a 40-segment extension driver is added.

2) 2-line display

In the case of a 2-line display, the address range of DDRAM is 00H ~27H and 40H ~ 67H.
An Extension driver will be used. Fig-3 shows the example when a 40 segment extension driver is added.

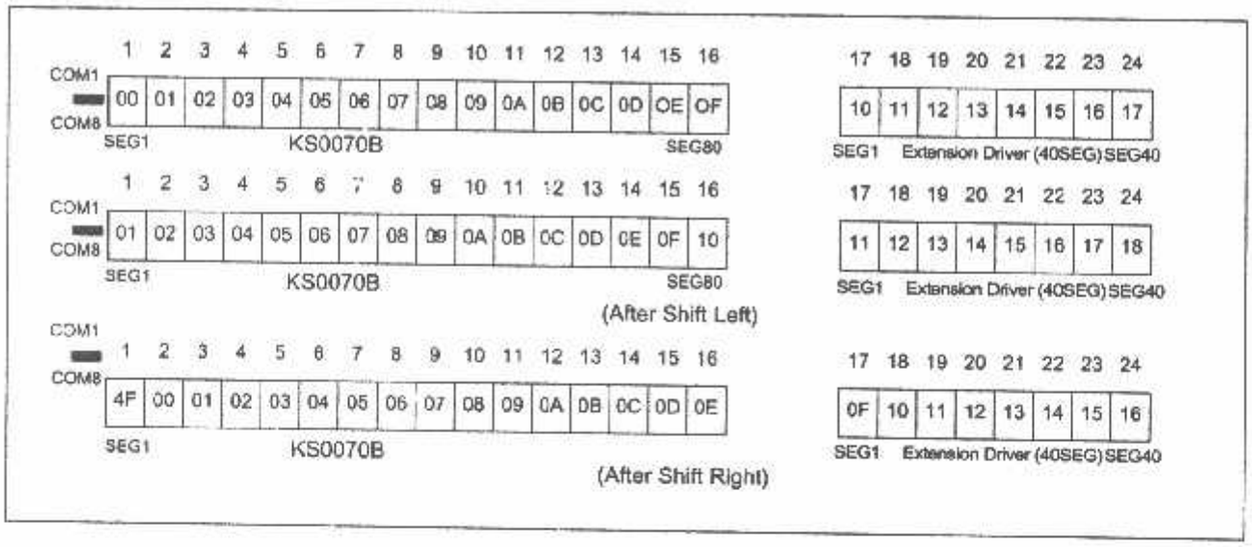


Fig-2. 1-line × 24ch. Display With 40 SEG. Extension Driver.

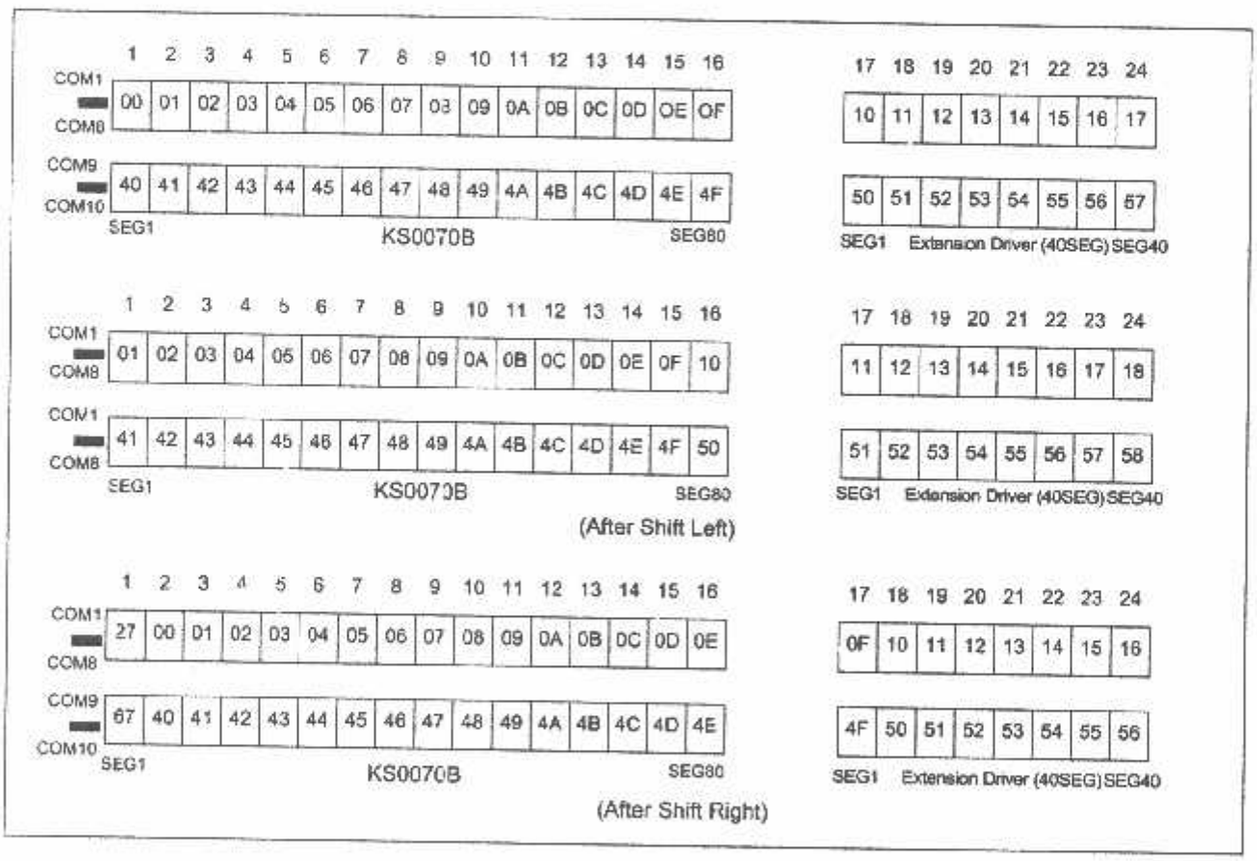


Fig-3. 2-line × 24ch. Display With 40 SEG. Extension Driver.

CGROM (Character Generator ROM)

CGROM has a 5 × 7-dot 192 character pattern, and a 5 × 10-dot 32 character pattern (Refer to Table 2).

CGRAM (Character Generator RAM)

CGRAM has up to 5 × 8-dot 8 characters. By writing font data to CGRAM, user defined characters can be used (Refer to Table 3).

Timing Generation Circuit

Timing generation circuit generates clock signals for the internal operations.

LCD Driver Circuit

LCD Driver circuit has 16 common and 80 segment signals for LCD driving.
Data from CGRAM/CGROM is transferred to an 80-bit segment latch serially, and then stored to an 80-bit shift latch. When each com is selected by a 16-bit common register, segment data is also output through the segment driver from an 80-bit segment latch.
In the case of a 1-line display mode, COM1 ~ COM8 have 1/8 duty or COM1 ~ COM11 have a 1/11 duty. In a 2-line display mode, COM1 ~ COM16 have a 1/16 duty ratio.

Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF at cursor position.

Table 2. CGROM Character Code Table

Table 3. Relationship Between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)								CGRAM Address						CGRAM Data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	×	0	0	0	0	0	0	0	0	0	×	×	×	0	1	1	1	0	pattern 1
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	
0	0	0	0	×	1	1	1	1	1	1	0	0	0	×	×	×	1	0	0	0	1	pattern 8
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

* "×": dont care

INSTRUCTION DESCRIPTION

Outline

To overcome the speed difference between the internal clock of KS0070B and the MPU clock, KS0070B performs internal operations by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table 5).
Instruction can be divided largely into four kinds:
(1) KS0070B function set instructions (set display methods, set data length, etc.)
(2) address set instructions to internal RAM
(3) data transfer instructions with internal RAM
(4) others .

The address of the internal RAM is automatically increased or decreased by 1.

* NOTE: During internal operation, Busy Flag (DB7) is read "1". Busy Flag check must be preceded by the next instruction.
When you make an MPU program with checking the Busy Flag (DB7), it must be necessary 1/2 Fosc for executing the next instruction by falling E signal after the Busy Flag (DB7) goes to "0".

Contents

1) Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM addresses, and set the DDRAM addresses to "00H" in the AC (address counter). Return cursor to original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

2) Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	×

Return Home is the cursor return home instruction.
Set DDRAM address to "00H" in the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

3) Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.
I/D : Increment / decrement of DDRAM address (cursor or blink)
When I/D = "1", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "0", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when reading from or writing to CGRAM.

SH: Shift of entire display
When DDRAM is in read (CGRAM read/write) operation or SH = "0", shift of entire display is not performed.
If SH = "1" and in DDRAM write operation, shift of entire display is performed according to I/D value
(I/D = "1": shift left, I/D = "0": shift right).

4) Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1-bit register.
D : Display ON/OFF control bit
When D = "1", entire display is turned on.
When D = "0", display is turned off, but display data remains in DDRAM.

C : Cursor ON/OFF control bit
When C = "1", cursor is turned on.
When C = "0", cursor disappears in current display, but I/D register retains its data.

B : Cursor Blink ON/OFF control bit
When B = "1", cursor blink is on, which performs alternately between all the "1" data and display characters at the cursor position.
When B = "0", blink is off.

5) Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	×	×

Without writing or reading the display data, shift right/left cursor position or display.
This instruction is used to correct or search display data.(Refer to Table 4)
During 2-line mode display, cursor moves to the 2nd line after the 40st digit of the 1st line.
Note that display shift is performed simultaneously in all the lines.
When displayed data is shifted repeatedly, each line shifts individually.
When display shift is performed, the contents of the address counter are not changed.

Table 4. Shift Patterns According to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	×	×

DL : Interface data length control bit
When DL = "1", it means 8-bit bus mode with MPU.
When DL = "0", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data in two parts.

N : Display line number control bit
When N = "0", it means 1-line display mode.
When N = "1", 2-line display mode is set.

F : Display font type control bit
When F = "0", 5 × 7 dots format display mode
When F = "1", 5 × 10 dots format display mode.

7) Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

8) Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When in 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".
In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0070B is in internal operation or not. If the resultant BF is "1", it means the internal operation is in progress and you have to wait until BF is Low. Then the next instruction can be performed. In this instruction you can also read the value of the address counter.

0) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction DDRAM address set, and CGRAM address set. RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

1) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that is read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. In the case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction; It also transfers RAM data to the output data register. After read operation the address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

In the case of RAM write operation, after this AC is increased/decreased by 1 like read operation. At this time, AC indicates the next address position, but you can read only the previous data by the read instruction.

ıble 5. Instruction Table

Instruction	Instruction Code										Description	Execution Time (fosc = 270 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC.	1.53 ms
Return Home	0	0	0	0	0	0	0	0	1	×	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted.	1.53 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display .	39 µs
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	39 µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	×	×	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39 µs
Function Set	0	0	0	0	1	DL	N	F	×	×	Set interface data length (DL : 4-bit/8-bit), numbers of display line (N : 1-line/ 2-line, Display font type (F:0 ...)	39 µs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 µs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 µs
Read Busy flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 µs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43 µs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43 µs

NOTE : When you make an MPU program with checking the Busy Flag (DB7), it must be necessary 1/2Fosc for executing the next instruction by falling E signal after the Busy Flag (DB7) goes to "0".

TERFACE WITH MPU

Interface with 8-bit MPU

hen interfacing data length are 8-bit, transfer is performed all at once through 8 ports, from DB0 to DB7.
n Example of the timing sequence is shown below.

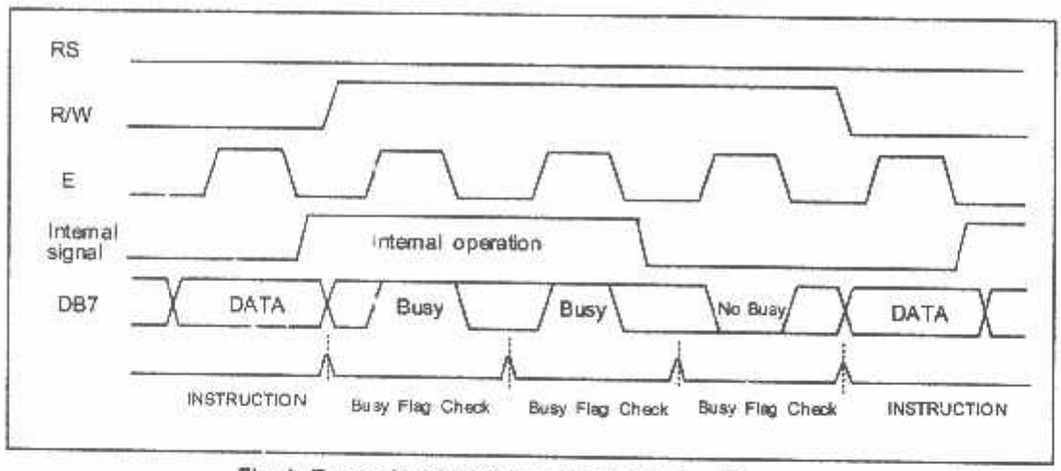


Fig-4. Example of 8-bit Bus Mode Timing Diagram

) Interface with 4-bit MPU

/hen interfacing data length are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus.
t first, higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then the lower 4-bit
n case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed in two parts. Busy
lag outputs "1" after the second transfer are ended.
xample of timing sequence is shown below.

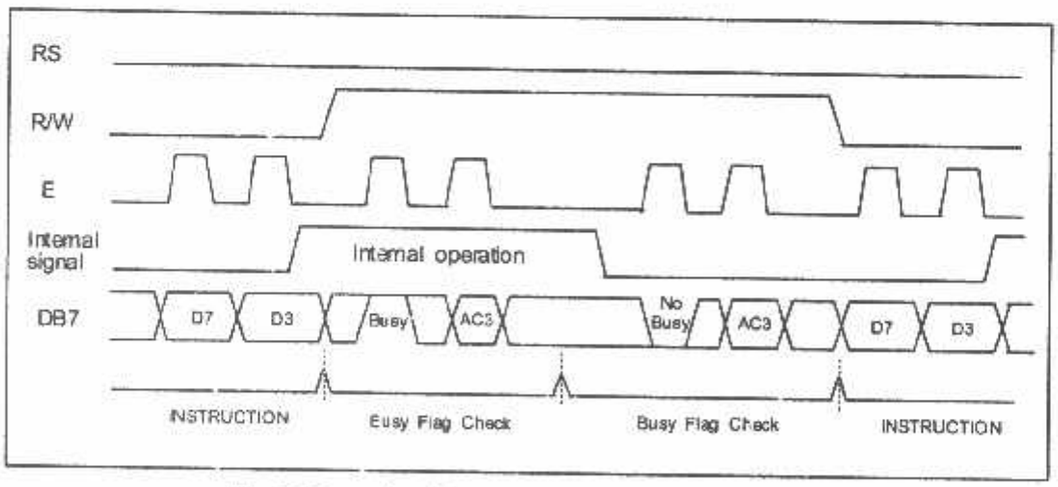
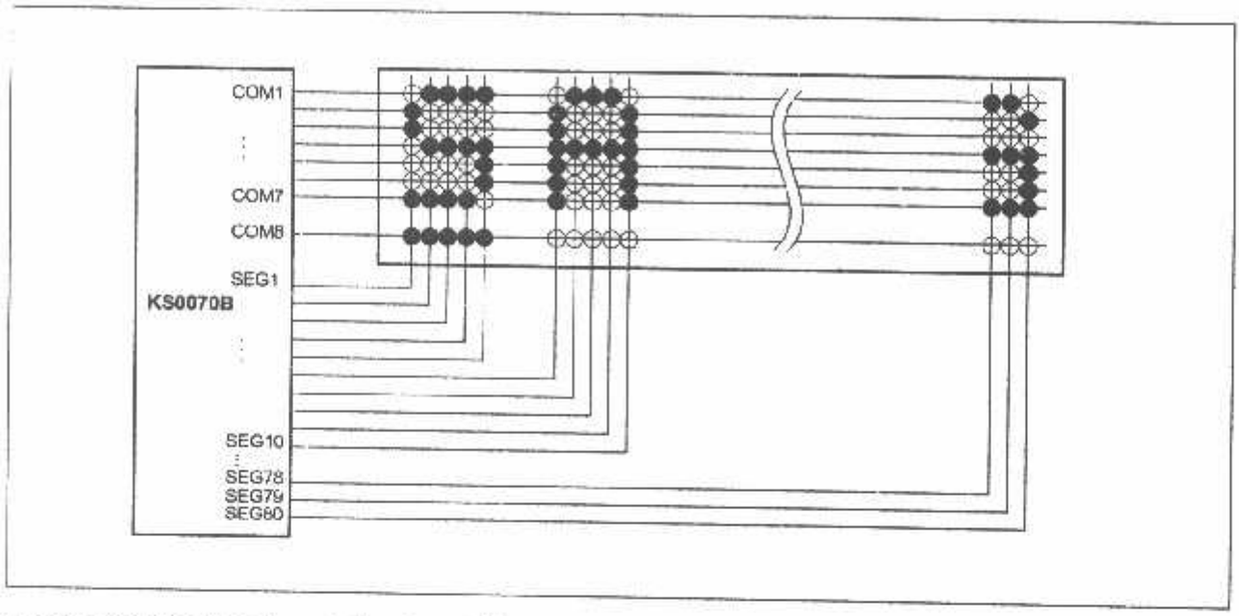


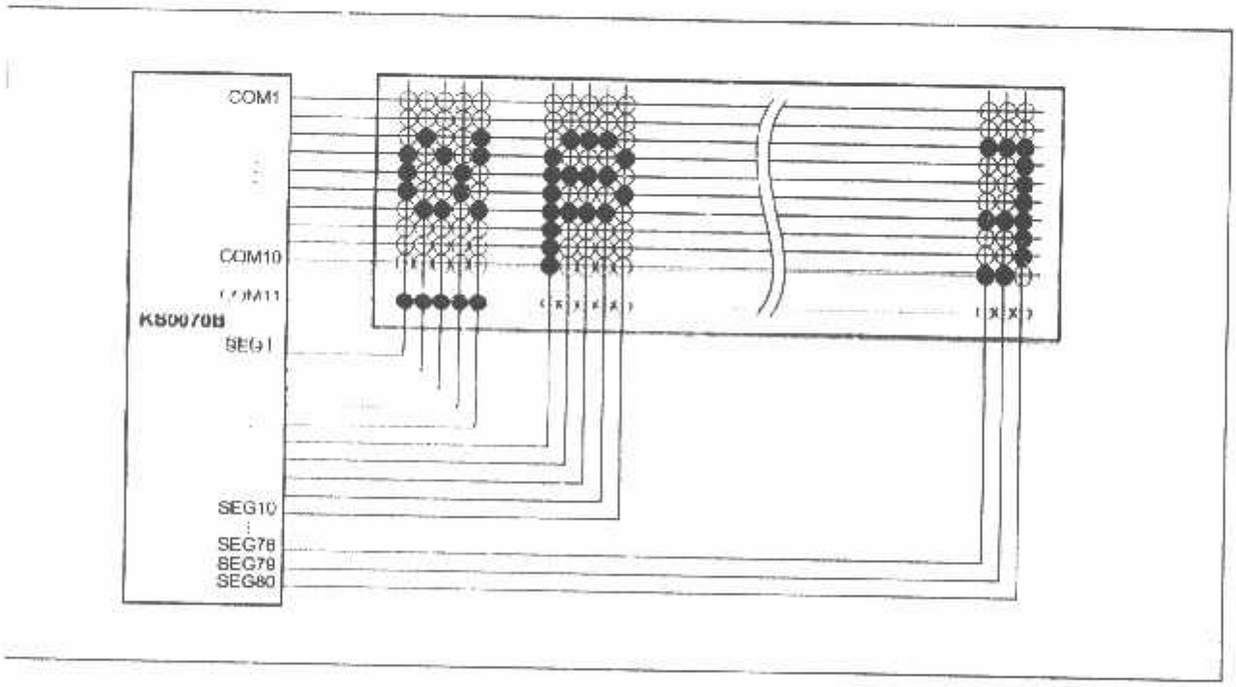
Fig-5. Example of 4-bit Bus Mode Timing Diagram

PPLICATION INFORMATION ACCORDING TO LCD PANEL

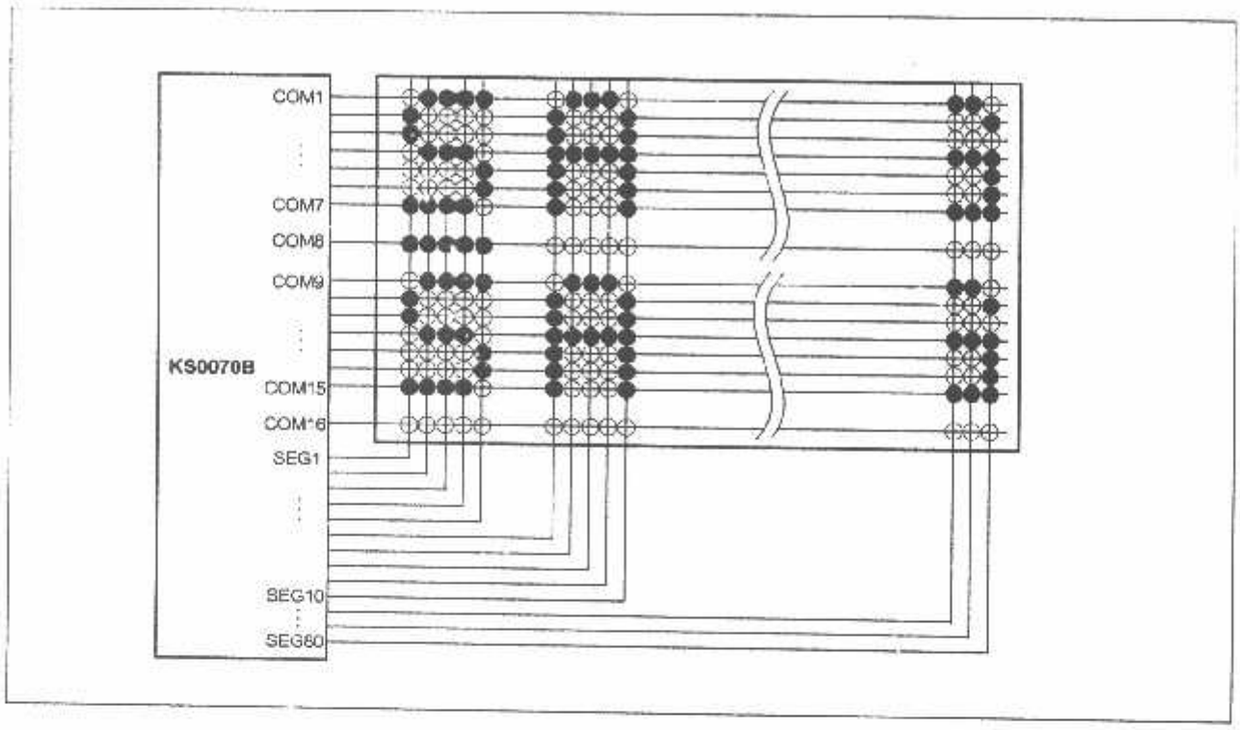
I LCD Panel: 16 characters × 1-line format (5 × 7 dots + 1 cursor line 1/4 bias, 1/8 duty)



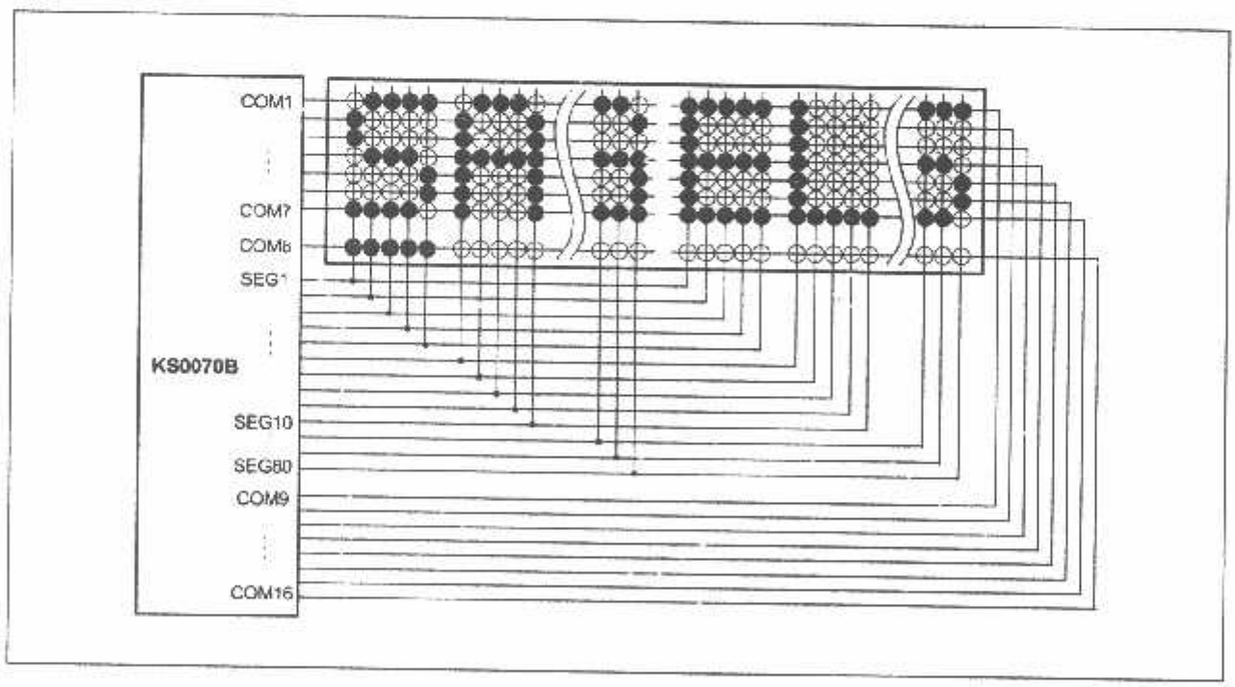
) LCD Panel: 16 characters × 1-line format (5 × 10 dots + 1 cursor line 1/4 bias, 1/11 duty)



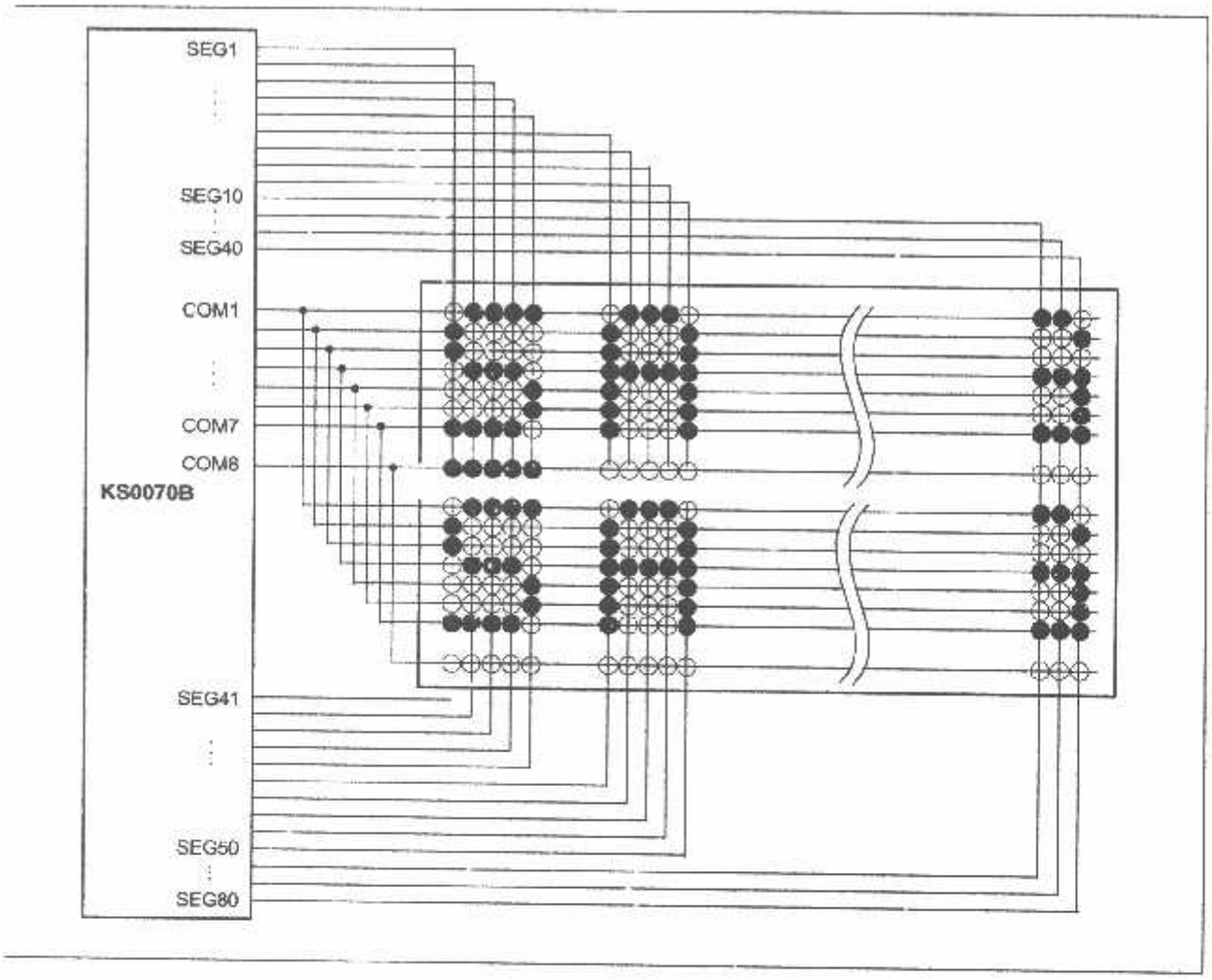
) LCD Panel : 16 character × 2-line format: (5 × 7 dots + 1 cursor line 1/5 bias, 1/16 duty)



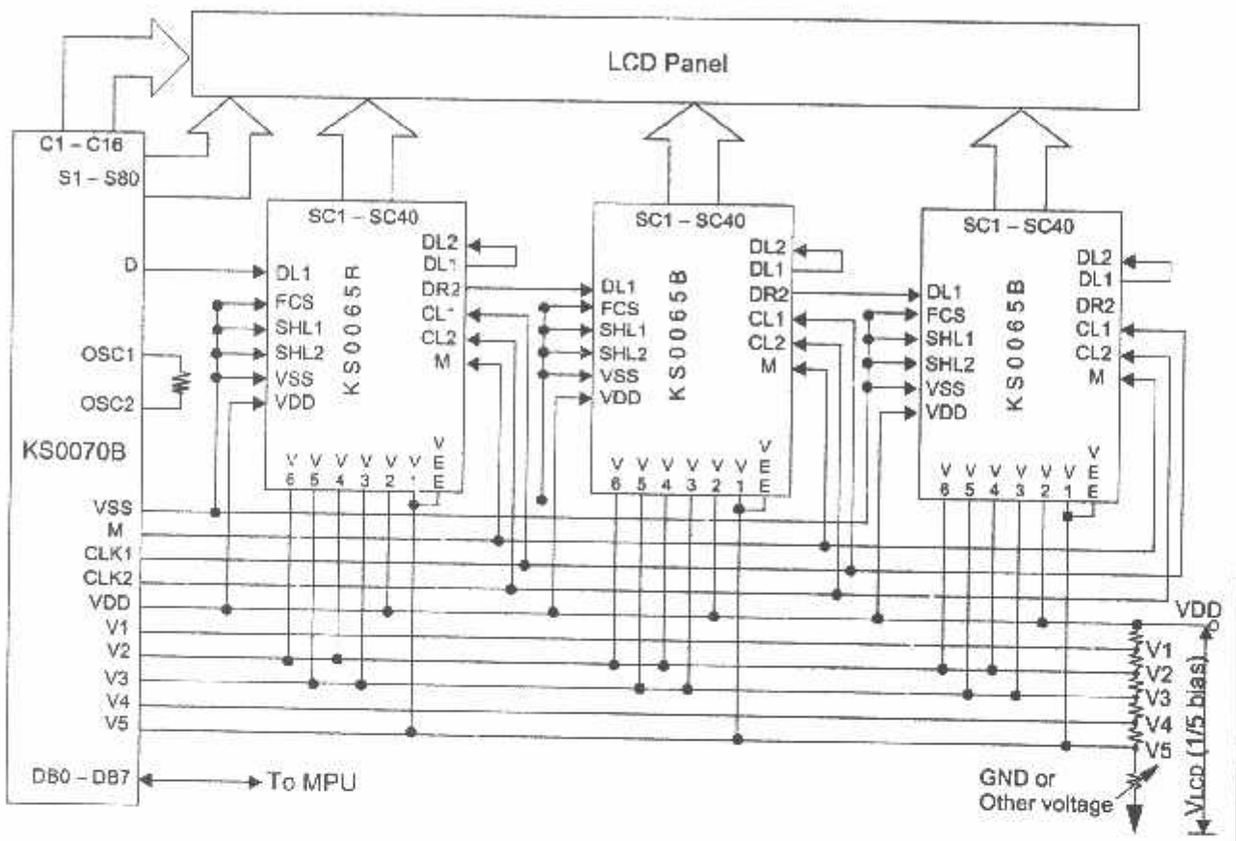
I) LCD Panel : 32 character × 1-line format: (5 × 7 dots + 1 cursor line 1/5 bias, 1/16 duty)



• LCD Panel : 8 character x 2-line format: (5 x 7 dots + 1 cursor line 1/4 bias, 1/8 duty)



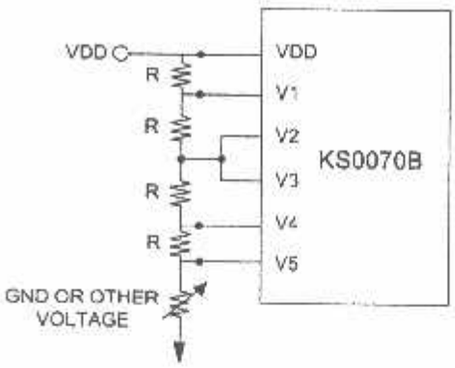
APPLICATION CIRCUIT



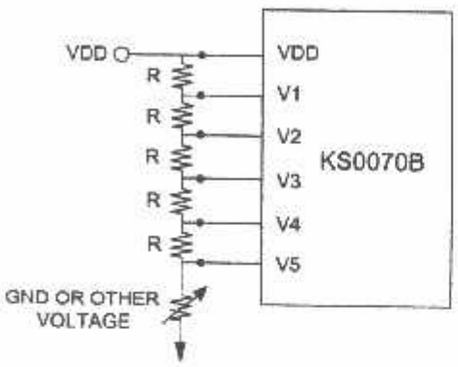
* When KS0065B is externally connected to the KS0070B, you can increase the number of display digits up to 80 characters

BIAS VOLTAGE DIVIDE CIRCUIT

1) 1/4 bias, 1/8 OR 1/11 duty



2) 1/5 bias, 1/16 OR 1/11 duty



INITIALIZING

When the power is turned on, KS0070B is initialized automatically by the power on reset circuit.
During the initialization, the following instructions are executed, and BF(Busy Flag) is kept "1"(busy state) to the end of initialization.

1) Display Clear instruction
   Write "20H" to all DDRAM
2) Set Functions instruction
   DL = 1 : 8-bit bus mode
   N = 0 : 1-line display mode
   F = 0 : 5×7 font type
3) Control Display ON/OFF instruction
   D = 0 : Display OFF
   C = 0 : Cursor OFF
   B = 0 : Blink OFF
4) Set Entry Mode instruction
   I/D = 1 : Increment by 1
   SH = 0 : No entire display shift

INTRODUCTION

KS0070B is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology. It is capable of displaying 1 or 2 lines with the 5×7 format or 1 line with the 5×10 dots format.

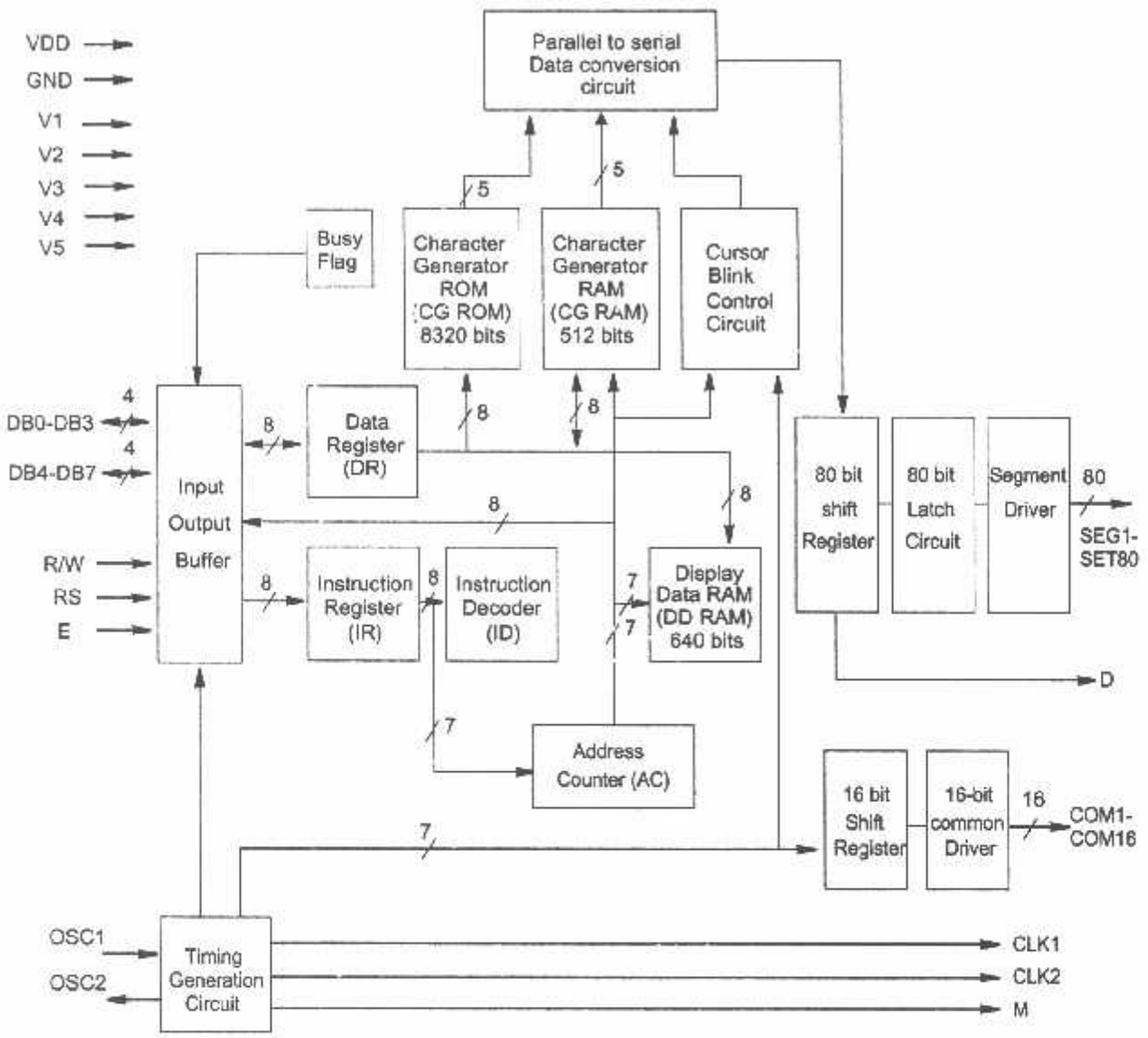
FUNCTIONS

- Character type dot matrix LCD driver & controller
- Internal driver: 16 common and 80 segment signal output
- Easy interface with 4-bit or 8-bit MPU
- Display character pattern: 5×7 dots format (192 kinds) & 5×10 dots format (32 kinds)
- The special character pattern is directly programmable by the character generator RAM.
- A customer character pattern is programmable by mask option.
- It can drive a maximum of 80 characters by using the KS0065B or KS0063B externally.
- Various instruction functions
- Built-in automatic power on reset
- Driving method is A-type (Line inversion)

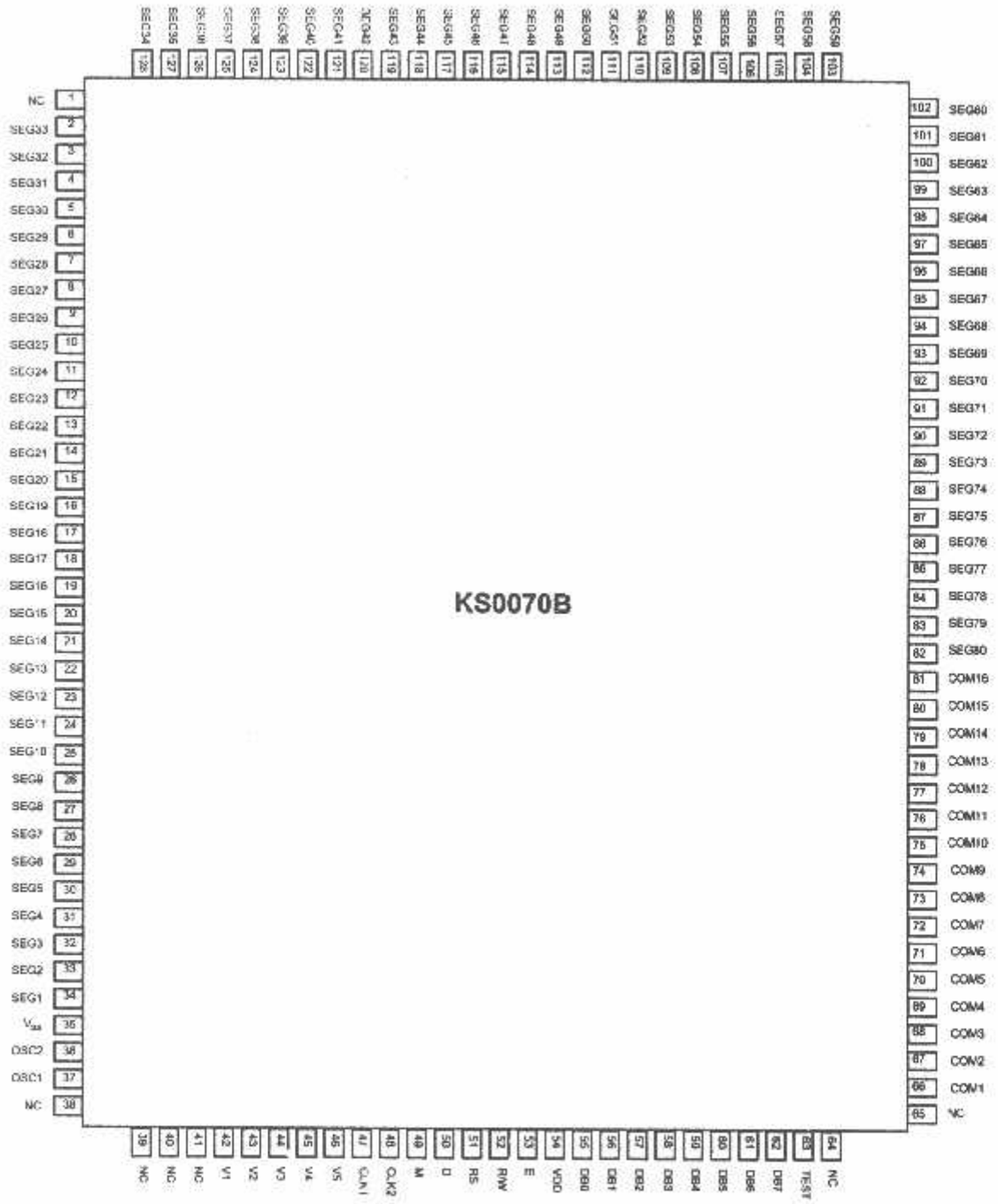
FEATURES

- Internal Memory
  - Character Generator ROM (CGROM): 8,320 bits (192 characters × 5 × 7 dots) & (32 characters x 5 × 10 dots)
  - Character Generator RAM (CGRAM): 64 × 8 bits (8 characters × 5 × 7 dots)
  - Display Data RAM (DDRAM): 80 × 8 bits (80 characters max.)
- Low power operation
  - Power supply voltage range: 2.7 to 5.5 V (VDD)
  - LCD Drive voltage range: 3.0 to 10.0 V (VDD to V5)
- Supply voltage for display: 0 to –5 V (V5)
- Programmable duty cycle: 1/8, 1/11, 1/16
- Internal oscillator with an external resistor
- Bare chip or bumped chip available

BLOCK DIAGRAM



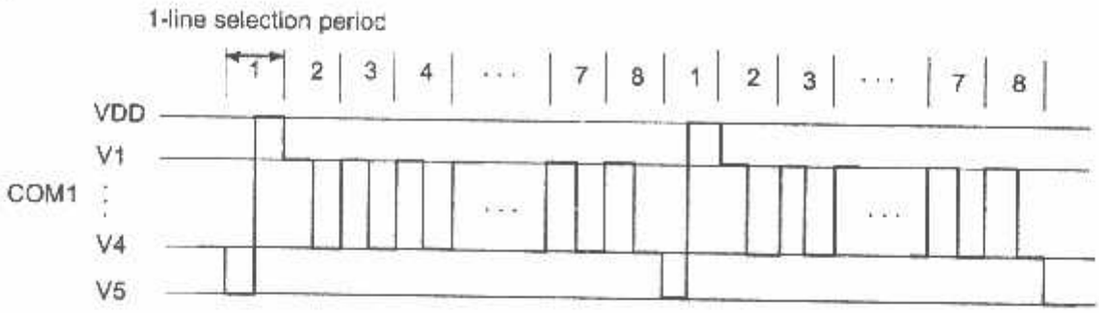
PIN CONFIGURATION



FRAME FREQUENCY

) 1/8 duty cycle

.) A-type Waveform

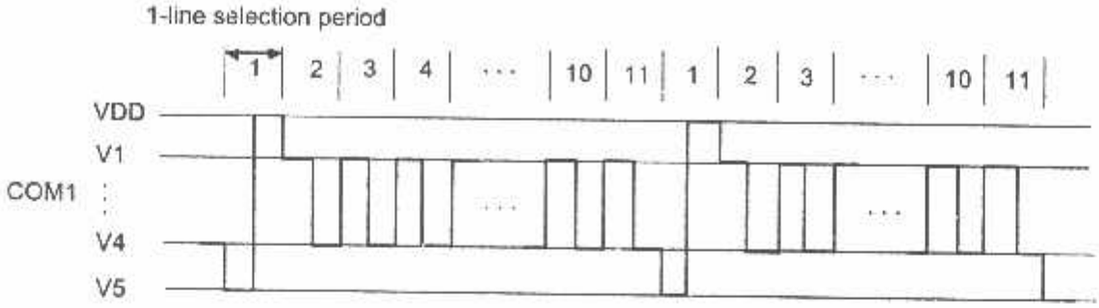


Item	Clock / Frequency
Line selection period	400 clocks
Frame frequency	84.4 Hz

* fosc=270 kHz (1 clock = 3.7 μs)

) 1/11 duty cycle

.) A-type Waveform

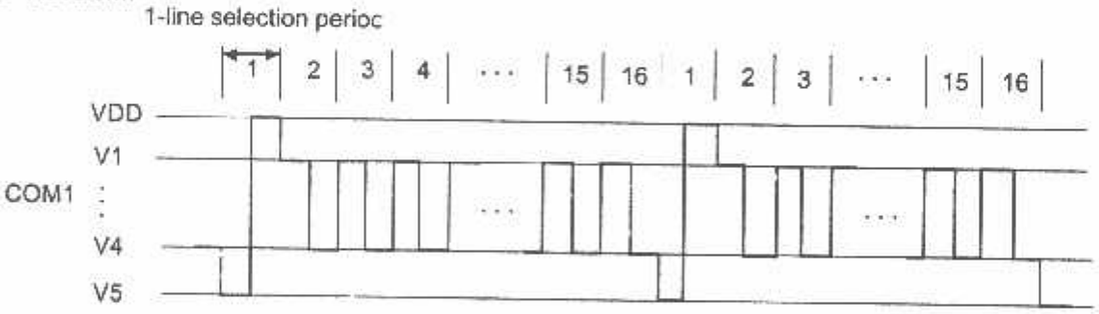


Item	Clock / Frequency
Line selection period	400 clocks
Frame frequency	61.4 Hz

* fosc=270 kHz (1 clock = 3.7 μs)

·) 1/16 duty cycle

·) A-type Waveform

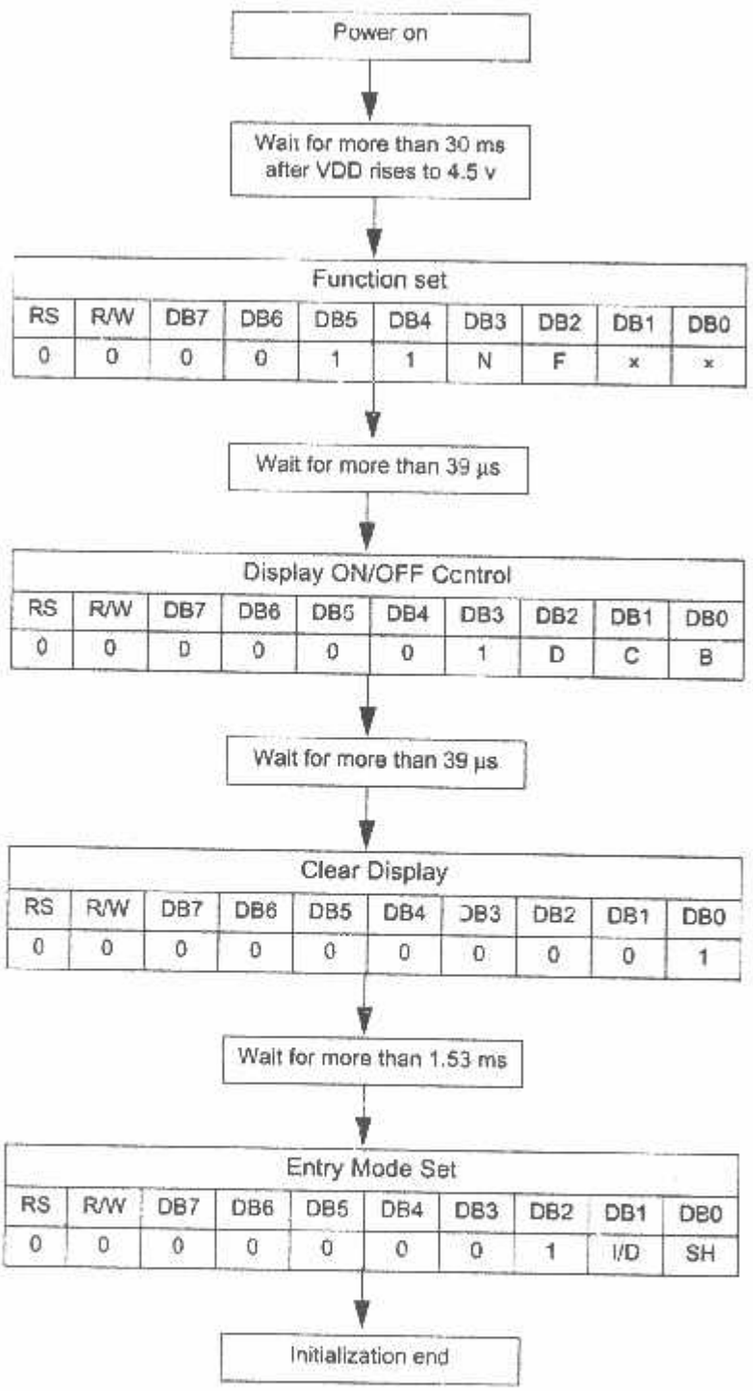


Item	Clock / Frequency
Line selection period	200 clocks
Frame frequency	84.4 Hz

* fosc=270 kHz (1 clock = 3.7 μs)

NITIALIZING BY INSTRUCTION

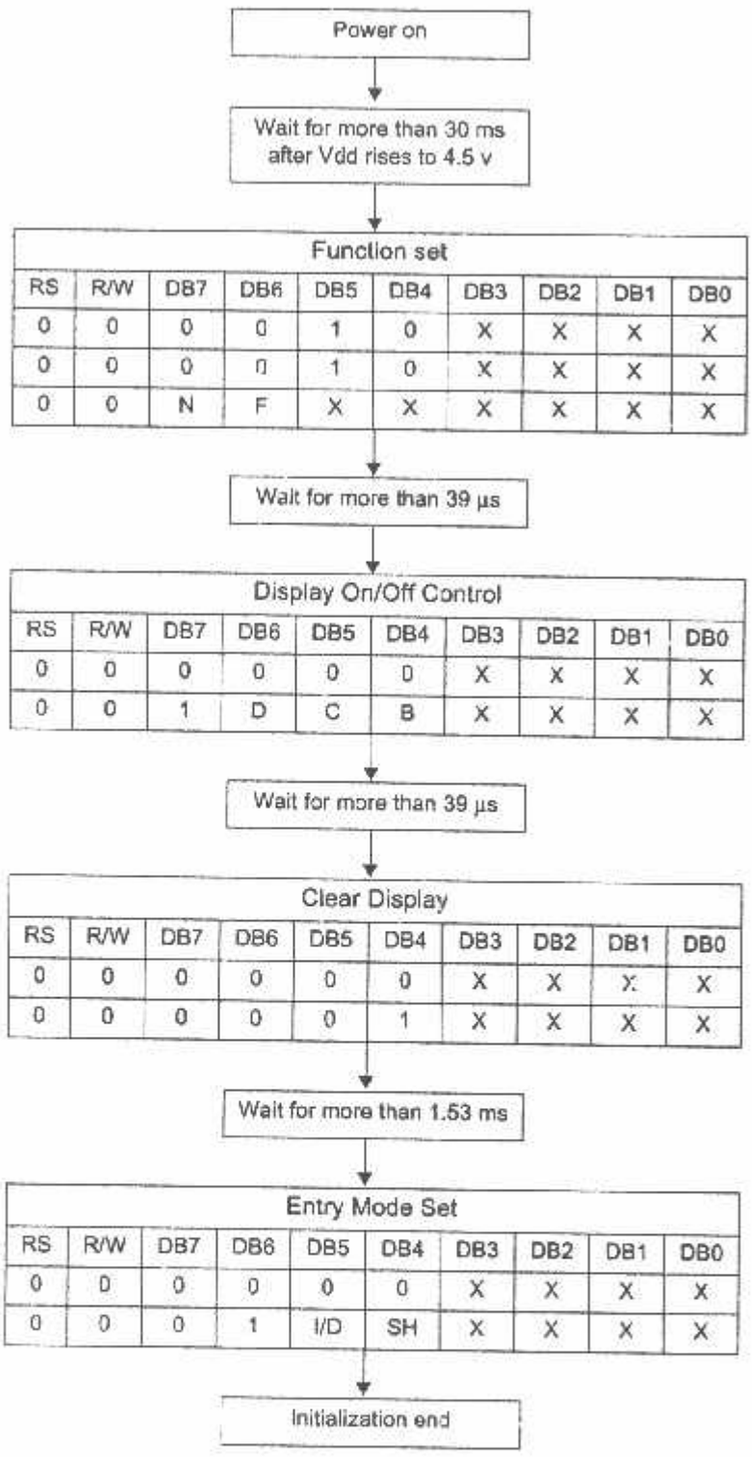
) 8-bit interface mode



Condition: fosc=270 kHz

N	0	1-line mode
	1	2-line mode
F	0	5 × 7 dots
	1	5 × 10 dots
D	0	display off
	1	display on
C	0	cursor off
	1	cursor on
B	0	blink off
	1	blink on
I/D	0	decrement mode
	1	increment mode
SH	0	entire shift off
	1	entire shift on

) 4-bit interface mode



Condition: fosc=270 kHz

Function set									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	X	X	X	X
0	0	0	0	1	0	X	X	X	X
0	0	N	F	X	X	X	X	X	X

N	0	1-line mode
	1	2-line mode

F	0	5 × 7 Dots
	1	5 × 10 Dots

Display On/Off Control									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	1	D	C	B	X	X	X	X

D	0	display off
	1	display on

C	0	cursor off
	1	cursor on

B	0	blink off
	1	blink on

Clear Display									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	1	X	X	X	X

Entry Mode Set									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	1	I/D	SH	X	X	X	X

I/D	0	decrement mode
	1	increment mode

SH	0	entire shift off
	1	entire shift on

EXAMPLE OF INSTRUCTION AND DISPLAY CORRESPONDENCE

1. Power supply on: Initialized by the internal power on reset circuit*

LCD DISPLAY

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

2. Function Set: 8-bit, 2-line, 5×7 dot

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	X	X

3. Display ON/OFF Control: Display/Cursor on/Blink off

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	1	1	0

4. Entry Mode Set: Increment

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	0

5. Write Data to DDRAM: Write S

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

S_

6. *Write Data to DDRAM: Write A

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	0	1

SA_

7. Write Data to DDRAM: Write M

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	0	1

SAM_

8. Write Data to DDRAM: Write S

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

SAMS_

9. Write Data to DDRAM: Write U

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	1	0	1

SAMSU_

10. Write Data to DDRAM: Write N

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	1	0

SAMSUN_

11. Write Data to DDRAM: Write G

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	1	1

SAMSUNG_

12. Set DDRAM Address: 40H

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	0	0	0	0

SAMSUNG
_

13. Write Data to DDRAM: Write K

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	0	1	1

SAMSUNG
K_

14. Write Data to DDRAM: Write S

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

SAMSUNG
KS_

15. Write Data to DDRAM: Write 0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	0	0

SAMSUNG
KS0_

16. Write Data to DDRAM: Write 0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	0	0

SAMSUNG
KS00_

17. Write Data to DDRAM: Write 7

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	1	1	1

SAMSUNG
KS007_

18. Write Data to DDRAM: Write 2

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	1	0

SAMSUNG
KS0072_

19. Cursor or Display Shift: Cursor shift left

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	0	X	X

SAMSUNG
KS0072

20. Write Data to DDRAM: Write 0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	0	0

SAMSUNG
KS0070_

21. Entry Mode Set: Entire Display shift Enable

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	1

SAMSUNG
KS0070_

22. Write Data to DDRAM: Write B

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	1	0

AMSUNG
S0070B_

23. Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	×

SAMSUNG
KS0070B

24. Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

IAXIMUM ABSOLUTE RATE

laximum Absolute Power Ratings

Item	Symbol	Unit	Value
Power supply voltage(1)	V_{DD}	V	-0.3 to + 7.0
Power supply voltage(2)	V_{LCD}	V	VDD -15.0 to V_{DD} + 0.3
Input voltage	V_{IN}	V	-0.3 to V_{DD} + 0.3

* NOTE: Voltage greater than above may damage the circuit (VDD ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5)

emperature Characteristics

Item	Symbol	Unit	Value
Operating temperature	Topr	°C	-30 to + 85
Storage temperature	Tstg	°C	-55 to + 125

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 4.5V to 5.5V, Ta = -30 to +85 °C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	V_{IDD}	-	4.5	-	5.5	V
Supply Current	I_{DD1}	ceramic resonator fosc = 250 kHz		0.7	1.0	mA
	I_{DD2}	Resistor oscillation external clock operation fosc = 270 kHz	-	0.4	0.6	
Input Voltage (1) (except OSC1)	V_{IH1}	-	2.2	-	V_{DD}	V
	V_{IL1}	-	-0.3	-	0.6	
Input Voltage (2) (OSC1)	V_{IH2}	-	V_{DD}-1.0	-	V_{DD}	V
	V_{IL2}	-	-0.2	-	1.0	
Output Voltage (1) (DB0 to DB7)	V_{OH1}	I_{OH} = -0.205 mA	2.4	-	-	V
	V_{OL1}	I_{OL} = 1.2 µA	-	-	0.4	
Output Voltage (2) (except DB0 to DB7)	V_{OH2}	I_O = -40 µA	0.9V_{DD}	-	-	V
	V_{OL2}	I_O = 40 µA	-	-	0.1V_{DD}	
Voltage Drop	Vd_{COM}	I_O = ± 0.1 mA	-	-	1	V
	Vd_{SEG}		-	-	1	
Input Leakage Current	I_{IL}	V_{IN} = 0 V to V_{DD}	-1	-	1	µA
Low Input Current	I_{IN}	V_{IN} = 0 V, V_{DD} = 5 V (PULL UP)	-50	-125	-250	
Internal Clock (external Rf)	f_{IC}	Rf = 91 kΩ ± 2% (V_{DD} = 5 V)	190	270	350	kHz
External Clock	f_{EC}	-	150	250	350	kHz
	duty		45	50	55	%
	tr, tf		-	-	0.2	µs
LCD Driving Voltage	V_{LCD}	V_{DD}-V_5 (1/5, 1/4 Bias)	4.6	-	10.0	V

(V_{DD} = 2.7 to 4.5V, Ta = -30 + 85°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	-	2.7	-	4.5	V
Supply Current	I_{DD1}	ceramic resonator fosc = 250 kHz	-	0.3	0.5	mA
	I_{DD2}	Resistor oscillation external clock operation fosc = 270 kHz	-	0.17	0.3	
Input Voltage (1) (except OSC1)	V_{IH1}	-	0.7V_{DD}	-	V_{DD}	V
	V_{IL1}	-	-0.3	-	0.4	
Input Voltage (2) (OSC1)	V_{IH2}	-	0.7V_{DD}	-	V_{DD}	V
	V_{IL2}	-		-	0.2V_{DD}	
Output Voltage (1) (DB0 to DB7)	V_{OH1}	I_{OH} = -0.1 mA	2.0	-	-	V
	V_{OL1}	I_{OL} = 0.1 mA	-	-	0.4	
Output Voltage (2) (except DB0 to DB7)	V_{OH2}	I_O = -40 µA	0.8V_{DD}	-	-	V
	V_{OL2}	I_O = 40 µA	-	-	0.2V_{DD}	
Voltage Drop	Vd_{COM}	I_O = ± 0.1 mA	-	-	1	V
	Vd_{SEG}		-	-	1.5	
Input Leakage Current	I_{IL}	V_{IN} = 0 V to V_{DD}	-1	-	1	µA
Low Input Current	I_{IN}	V_{IN} = 0 V, V_{DD} = 3 V (PULL UP)	-10	-50	-120	
Internal Clock (external Rf)	f_{IC}	Rf = 75 kΩ ± 2% (V_{DD} = 3 V)	190	250	350	kHz
External Clock	f_{EC}	-	125	270	350	kHz
	duty		45	50	55	%
	tr, tf		-	-	0.2	µs
* LCD Driving Voltage	V_{LCD}	V_{DD}-V_5 (1/5, 1/4 Bias)	3.0	-	10.0	V

LCD Driving Voltage (next page)

LCD Driving Voltage

POWER	DUTY	1/8, 1/11 DUTY	1/16 DUTY
	BIAS	1/4 BIAS	1/5 BIAS
V_{DD}		V_{DD}	V_{DD}
V1		$V_{DD} - V_{LCD}/4$	$V_{DD} - V_{LCD}/5$
V2		$V_{DD} - V_{LCD}/2$	$V_{DD} - 2V_{LCD}/5$
V3		$V_{DD} - V_{LCD}/2$	$V_{DD} - 3V_{LCD}/5$
V4		$V_{DD} - 3V_{LCD}/4$	$V_{DD} - 4V_{LCD}/5$
V5		$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$

AC Characteristics

(V_{DD} = 4.5 to 5.5 V, Ta = -30 to +85°C)

Mode	Item	Symbol	Min	Typ	Max	Unit
Write Mode (Refer to Fig-6)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	tr,tf	-	-	25	
	E Pulse Width (High, Low)	tw	220	-	-	
	R/W and RS Setup Time	tsu1	40	-	-	
	R/W and RS Ho d Time	th1	10	-	-	
	Data Setup Time	tsu2	60	-	-	
	Data Hold Time	th2	10	-	-	
Read Mode (Refer to Fig-7)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	tr,tf	-	-	25	
	E Pulse Width (High, Low)	tw	220	-	-	
	R/W and RS Setup Time	tsu	40	-	-	
	R/W and RS Hold Time	th	10	-	-	
	Data Output Delay Time	t_D	-	-	120	
	Data Hold Time	t_{DH}	20	-	-	

(V_{DD} = 2.7 to 4.5 V, Ta = -30 to +85°C)

Mode	Item	Symbol	Min	Typ	Max	Unit
Write Mode (Refer to Fig-6)	E Cycle Time	tc	1400	-	-	ns
	E Rise / Fall Time	tr,tf	-	-	25	
	E Pulse Width (High, Low)	tw	400	-	-	
	R/W and RS Setup Time	tsu1	60	-	-	
	R/W and RS Hold Time	th1	20	-	-	
	Data Setup Time	tsu2	140	-	-	
	Data Hold Time	th2	10	-	-	
Read Mode (Refer to Fig-7)	E Cycle Time	tc	1400	-	-	ns
	E Rise / Fall Time	tr,tf	-	-	25	
	E Pulse Width (High, Low)	tw	400	-	-	
	R/W and RS Setup Time	tsu	60	-	-	
	R/W and RS Hold Time	th	20	-	-	
	Data Output Delay Time	t_D	-	-	360	
	Data Hold Tim.e	t_{DH}	5	-	-	

(V_{DD} = 2.7 to 5.5 V, Ta = -30 to +85°C)

Mode	Item	Symbol	Min	Type	Max	Unit
Interface Mode with Extension Driver (Refer to Fig-8)	Clock Pulse Width (High, Low)	tw	800	-	-	ns
	Clock Rise / Fall Time	tr,tf	-	-	100	
	Clock Setup Time	t_{SU1}	500	-	-	
	Data Setup Time	t_{SU2}	300	-	-	
	Data Hold Time	t_{DH}	300	-	-	
	M Delay Time	t_{Dw}	-1000	-	1000	

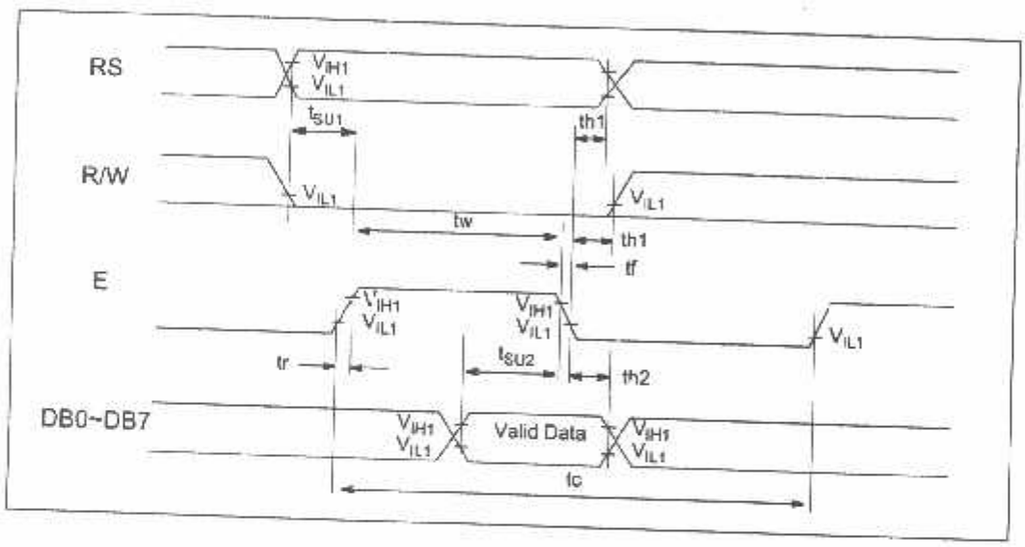


Fig-6. Write Mode Timing Diagram

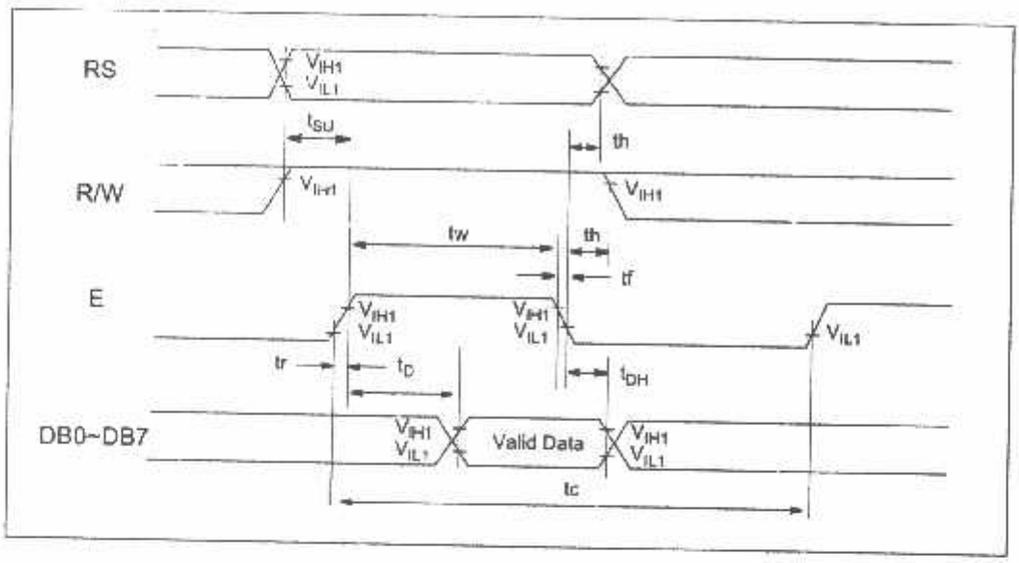


Fig-7. Read Mode Timing Diagram

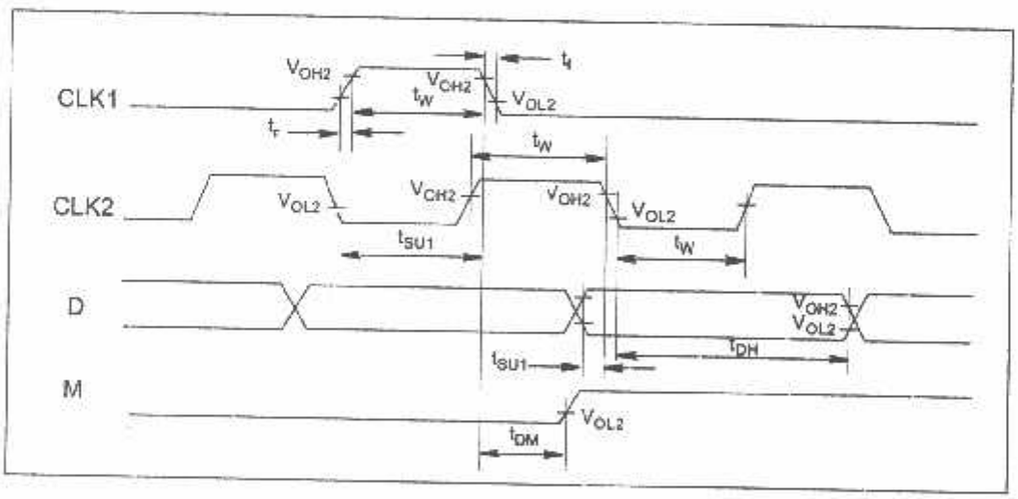


Fig-8. Interface Mode with Extension Driver Timing Diagram