INSTITUT TEKNOLOGI NASIONAL MALANG

FAKULTAS TEKNOLOGI INDUSTRI

JURUSAN TEKNIK ELEKTRO S-1

KOSENTRASI TEKNIK ELEKTRONIKA

SKRIPSI

Diajukan untuk memenuhi sebagaian persyaratan

memperoleh gelar sarjana teknik

SKRIPSI

PERENCANAAN DAN PEMBUATAN ALAT PENGUKUR KEKUATAN BENANG DIGITAL DENGAN TAMPILAN PADA LCD BERBASIS MIKROKONTROLER AT89S52

Disusun Oleh :

HERVIEN DWI ANINDITA

01.17.077

MARET 2006

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PERENCANAAN DAN PEMBUATAN ALAT PENGUKUR KEKUATAN BENANG DIGITAL DENGAN TAMPILAN PADA LCD BERBASIS MIKROKONTROLER AT89S52

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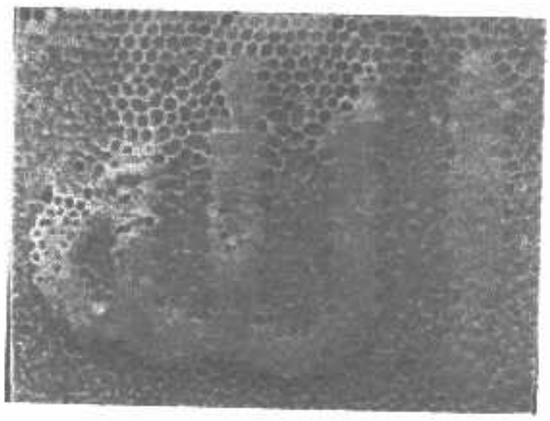
بسم الله الرحمن الرحيم

"Dengan Menyebut Nama Allah yang Maha Pengasih Lagi Maha Penyayang"



"Allah mengangkat orang-orang yang beriman dan orang-orang yang berilmu pengetahuan beberapa derajat". (Qs. Al-Mujadallah:11)

Pertama-tama ku ucapkan terima kasih sebesar-besarnya kepada Allah S.W.T. Tuhan semesta alam atas rahmat dan hidayahnya yang difimpahkan kepada hambahmu ini yang penuh dengan dosa. Serta shalawat dan salam selalu tercurah untuk nabi Muhammad S.A.W.

Skripsi ini kuuuuuuuu Persembahkan For :
My Family : Papa & Mama Atas Kasih sayang dan doa yang tak Pernah berhenti terima kasih atas investasinya, My sister "cepat lulus & jangan malas terapi biar bisa cepat jalan". My brother " Jangan mancing aja ingat ama keluarga nanti tambah item"

My best friends : terima kasih atas semangat yang diberikan maaf aku ndak bisa memenuhi janjiku (LULUS bareng Jesss) and maaf juga aku ndak bisa seperti dulu tolong ngertiin aku Keadaan yang membuat aku begini.

Dosen pembimbing Skripsiku : Pak Usman + Pak Ibrahim
Terima kasih atas perhatian dan kemudahan-kemudahan yang diberikan dalam proses bimbingan moriil and spiritual.Bu Mimien selaku dosen wali, Pak Yudi selaku Ketua jurusan, Pak Sidik selaku pembimbing PKN terima kasih atas

ABSTRAKSI

PERANCANGAN DAN PEMBUATAN ALAT PENGUKUR KEKUATAN BENANG DIGITAL DENGAN TAMPILAN PADA LCD BERBASIS MIKROKONTROLLER AT89S52

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Kata Kunci : *Pengukur Kekuatan Benang, Strain Gage, Mikrokontroller AT89S52*

Dalam skripsi ini dibahas suatu perencanaan dan pembuatan alat pengukur kekuatan benang dengan menggunakan teknologi mikrokontroller dari keluarga ATMEL AT89S52. Dengan menggunakan teknologi ini diharapkan dapat membuat suatu alat yang menghasilkan nilai yang akurat dan yang lebih baik dari yang sudah ada.

Perencanaan blok diagram alat yang direncanakan ini meliputi sensor strain gage, Op-Amp, ADC, limit switch, display / LCD, driver motor, motor DC dan mekanik alat. Sensor strain gage berfungsi sebagai sensor gaya dari tarikan, motor DC berfungsi sebagai penarik benang hingga putus,Op-Amp berfungsi sebagai penguat. ADC berfungsi sebagai pengubah sinyal analog menjadi senyal digital, display / LCD berfungsi sebagai penampil data hasil pengukuran, driver motor berfungsi sebagai driver motor untuk menggerakkan motor DC.

Cara kerja dari alat ini adalah dalam hal ini menggunakan strain gage yang dipakai sebagai sensor, Motor akan mundur apabila tombol start dalam kondisi aktif. Sehingga strain gage akan mengalami perubahan resistansi yang dihubungkan dengan menggunakan rangkaian jembatan wheatstone sinyal yang dihasilkan sangat kecil sehingga membutuhkan penguatan sebesar 687.76 kali. Apabila limit switch 1 dalam kondisi aktif maka ADC yang berfungsi untuk mengubah sinyal analog menjadi sinyal digital akan bekerja memilih data yang terbesar kemudian mikrokontroler akan mengelolah data dari ADC kemudian ditampilkan ke dalam LCD. Apabila motor menyentuh limit switch 2 maka motor akan maju hingga menyentuh limit switch 3 hingga motor akan berhenti ke kondisi awal.

KATA PENGANTAR

Dengan mengucapkan puji syukur kehadirat Tuhan Yang Maha Esa Penulis dapat menyelesaikan skripsi ini karena berkat rahmat-Nyalah Penulis dapat menyusun skripsi ini yang menjadi salah satu syarat akademik dalam menyelesaikan studi untuk menempuh gelar Sarjana S-1 di Fakultas Teknologi Industri Jurusan Teknik Elektro di Institut Teknologi Nasional Malang.

Skripsi ini disusun berdasarkan hasil-hasil percobaan beserta teori dasar dan beberapa jawaban pertanyaan dari permasalahan yang ada sehinga Penulis sekaligus Penyusun dapat menambah wawasan dan tidak hanya menguasai teori saja namun juga memahami pengetahuan tersebut secara teknis.

Tersusunnya skripsi ini karena adanya dorongan, masukan, juga fasilitas dari pihak-pihak yang berhubungan dengan pelaksanaan dan penyusunan skripsi ini. Oleh karena itu penulis mengucapkan terima kasih yang sebesar-besarnya kepada :

1. Dr. Ir. Abraham Lomi, MSEE selaku Rektor Institut Teknologi Nasional Malang
2. Ir. F. Yudi Limpraptono, MT selaku Ketua Jurusan Teknik Elektro Institut Teknologi Nasional Malang
3. Ir. Usman Djuanda, MM selaku Dosen Pembimbing I
4. M.Ibrahim Ashari, ST selaku Dosen Pembimbing II

5. Rekan-rekan yang telah banyak membantu dalam pelaksanaan dan penyusunan skripsi ini.

Namun Penulis sadar bahwa isi dari skripsi ini masih jauh dari sempurna. Oleh sebab itu kritik dan saran yang membangun sangat Penulis harapkan guna dalam perbaikan pada periode mendatang serta sebagai kelanjutan studi Penulis nantinya.

Penyusun berharap semoga skripsi ini dapat bermanfaat bagi Penyusun sendiri juga pembaca sekalian.

Malang, Maret 2006

Penulis

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BAB I

PENDAHULUAN

1.1. LATAR BELAKANG

Perkembangan ilmu pengetahuan dan teknologi pada era globalisasi saat ini mengalami kemajuan yang sangat pesat salah satunya terlihat pada bidang elektronika dimana telah banyak melahirkan peralatan elektronik. Dewasa ini tuntutan akan kebutuhan manusia semakin kompleks memunculkan inovasi baru di bidang elektronika yang digunakan untuk mempermudah segala kegiatan manusia.

Ada berbagai macam alat ukur yang dirancang manusia sampai saat ini baik yang bekerja secara mekanik, semi elektronik sampai yang berbasis pada mikrokontroler. Seperti alat pengukur kekuatan benang digital yang digunakan secara luas dan banyak beredar dipasaran dengan memakai berbagai jenis tranduser dengan harga yang relatif mahal. Maka pembuatan suatu alat pengukur kekuatan benang yang berkualitas dengan menggunakan sistem digital dengan harga relatif murah serta menghasilkan pengukuran yang presisi (ketelitian) serta memiliki akurasi (ketepatan) dalam mengukur kekuatan suatu benang mendapatkan nilai yang lebih pasti.

Pengetahuan tentang evaluasi bahan-bahan tekstil mempunyai peranan yang sangat penting dalam dunia industri maupun perdagangan tekstil. Banyak keputusan-keputusan yang penting baik dalam proses produksi tekstil maupun dalam perdagangan harus didasarkan atas pengetahuan evaluasi bahan tekstil yang bersangkutan diantaranya masalah kekuatan tarik dari bahan tersebut.

1.2. RUMUSAN MASALAH

Untuk membuat alat pengukur kekuatan benang dengan menggunakan sistem digital agar diperoleh hasil pengukuran yang presisi dan akurasi serta mudah dalam pembacaannya dengan biaya yang cukup murah, maka dapat diambil rumusan masalah dititik beratkan pada :

1. Bagaimana perancangan dan pembuatan alat.
2. Bagaimana penggunaan sistem mikrokontroler berbasis AT89S52 sebagai pengendali utama.
3. Bagaimana cara kerja alat tersebut.

1.3. BATASAN MASALAH

Agar yang dibahas tidak meluas maka perlu adanya pembatasan permasalahan. Adapun batasan masalah sebagai berikut :

1. Sistem mikrokontroler yang diaplikasikan dengan menggunakan IC AT89S52 sebagai unit kontrol utama dengan LCD sebagai tampilan.
2. Kekuatan benang yang akan diukur harus dibawah batas yang ditentukan dalam hal ini 1,3 Kg/helai.
3. Menggunakan penguat AD 521 sebagai penguat tegangan DC.
4. ADC 0804 sebagai pengubah sinyal analog ke sinyal digital.
5. Alat ini menggunakan motor DC sebagai penarik yang dikendalikan oleh mikrokontroler.
6. Tidak membahas catu daya.

1.4. TUJUAN MASALAH

Berdasarkan latar belakang diatas, maka tujuan dari perencanaan dan pembuatan alat ini sebagai berikut:

1. Mempelajari aplikasi sistem mikrokontroler dengan menggunakan AT89S52.
2. Mengaplikasikan sistem mikrokontroler AT89S52 pada alat ini dengan tampilan LCD.
3. Memberikan kemudahan dalam mengukur kekuatan benang yang pasti.

1.5. METODOLOGI PERENCANAAN

Adapun langkah-langkah yang diambil untuk menyelesaikan perancangan alat pembawa barang otomatis yaitu sebagai berikut :

1. Mempelajari sistem mikrokontroler AT89S52 dan komponen pendukung serta mencari literatur.
2. Merancang dan membuat desain alat, meliputi perancangan hardware dan software.
3. Pengujian terhadap peralatan serta analisa data hasil pemantauan peralatan.
4. Mengambil kesimpulan atas hasil untuk kerja alat.
5. Menyusun laporan.

1.6. SISTEMATIKA PERENCANAAN

Sistematika penulisan dan gambaran secukupnya yang terdapat dalam setiap bab sebagai berikut:

BAB I : PENDAHULUAN

Membahas tentang latar belakang, rumusan masalah, tujuan, batasan masalah, metodologi perencanaan, sistematika penulisan.

BAB II : DASAR TEORI

Membahas teori beserta pustaka yang relevansi dan menunjang perancangan dan pembuatan rangkaian yang digunakan.

BAB III : PERENCANAAN DAN PEMBUATAN ALAT

Membahas perencanaan dan pembuatan alat pengukur kekuatan tarik benang.

BAB IV : PENGUJIAN ALAT

Membahas tentang pengujian-pengujian terhadap sistem yang telah dibuat.

BAB V : PENUTUP

Merupakan bagian-bagian penutup yang berisi kesimpulan dan saran yang bermanfaat bagi pengembangan lebih lanjut.

BAB II

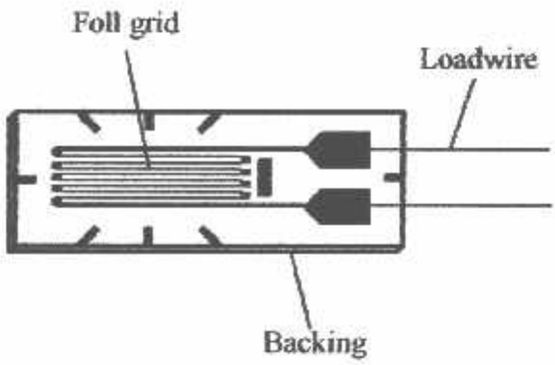
LANDASAN TEORI

Landasan teori sangat membantu untuk dapat memahami suatu sistem. Disamping itu dapat juga dijadikan acuan didalam merencanakan suatu sistem. Dengan pertimbangan hal-hal tersebut, maka landasan teori merupakan bagian yang harus dipahami untuk pembahasan selanjutnya.

Pada bab ini akan diuraikan mengenai penggunaan teknologi mikrokontroler AT89S52 beserta piranti penunjang lainya. Dimana teknologi AT89S52 sendiri merupakan pengembangan teknologi mikroprosesor dan mikrokontroler sebelumnya. Disini akan diuraikan mengenai segala aspek komponen perangkat keras yang akan dibuat.

2.1. Strain Gage

Strain gage adalah tranduser pasif yang merubah suatu pergeseran mekanis menjadi perubahan tahanan. Strain gage merupakan sebuah alat yang dapat disatukan keberbagai bahan untuk mengukur tegangan yang diberikan kepadanya. Strain gage metalik (logam) tersebut berubah terhadap panjang jika bahan tempat gage disatukan mengalami tarikan atau tekanan. Perubahan tahanan ini sebanding dengan regangan yang diberikan dan diukur dengan sebuah rangkaian jembatan wheatstone.



Gambar 2-1. Strain gage[12]

Karakteristik dari sensitivitas strain gage disebut faktor gage (GF) yang memenuhi syarat sebagai berikut :

$$GF = \frac{\Delta R/R}{\Delta L/L} \qquad (2\text{-}1)$$

Dimana :

GF = Faktor gage

R = Tahanan gage nominal

ΔR = perubahan tahanan gage

L = Panjang nominal bahan percobaan

ΔL = Perubahan panjang bahan percobaan

Perubahan tahanan ΔR pada sebuah konduktor yang panjangnya L, dinyatakan dengan persamaan sebagai berikut :

$$R = \rho \frac{L}{A} \qquad (2\text{-}2)$$

$$R = \frac{\rho \times L}{(\pi/4)d^2} \qquad (2\text{-}3)$$

Dimana :

R = Tahanan

ρ = Tahanan spesifik dari konduktor

L = Panjang konduktor

A = Luas penampang

d = Diameter konduktor

Tarikan (tension) terhadap konduktor menyebabkan pertambahan panjang ΔL dan pengurangan secara bersamaan pada diameter Δd. Maka persamaan (2-3) menjadi :

$$Rs = \rho \frac{(L + \Delta L)}{\left(\pi/4\right)(d - \Delta d)^2} \tag{2-4}$$

$$Rs = \rho \frac{L\left(1 + \Delta L/L\right)}{\left(\pi/4\right)d^2\left(1 - 2\Delta d/d\right)} \tag{2-5}$$

Persamaan (2-5) disederhanakan dengan menggunakan bilangan poisson (μ) yang didefinisikan sebagai perbandingan regangan dalam arah lateral terhadap regangan dalam arah aksial, yang dapat dinyatakan dengan persamaan sebagai berikut :

$$\mu = \frac{\Delta d/d}{\Delta L/L} \tag{2-6}$$

Subsitusi persamaan (2-6) kepersamaan (2-5) menjadi :

$$Rs = \rho \frac{L}{\left(\pi/4\right)d^2}\left(\frac{L + \Delta L/L}{1 - 2\mu\,\Delta L/L}\right) \tag{2-7}$$

Selanjutnya faktor gage dapat dinyatakan dalam persamaan sebagai berikut :

$$GF = \frac{\Delta R/R}{\Delta L/L} = 1 + 2\mu \qquad (2\text{-}8)$$

Bilangan poisson untuk logam umumnya berkisar antara 0,25 sampai 0,35. Dalam penggunaan strain gage diinginkan sensitivitas yang besar, faktor gage yang besar berarti pula perubahan tahanan yang relatif besar, maksudnya kemudahan dalam melakukan suatu tarikan atau tahanan yang kecil.

2.2. Penguat Instrumentasi

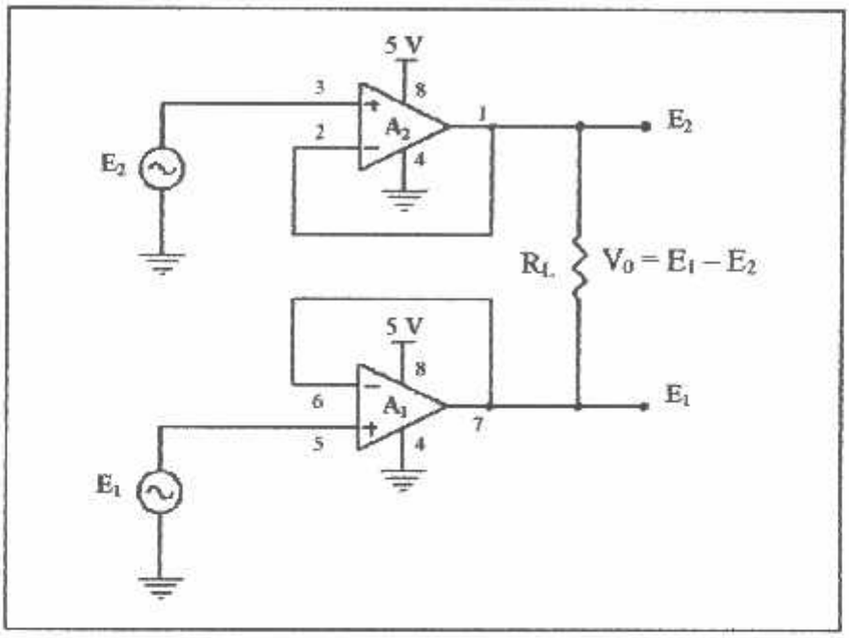
Penguat instrumentasi adalah suatu penguat loop tertutup dengan masukkan differensial, impedansi masukannya sangat tinggi sehingga dapat dianggap tidak menyerap arus pada masukkanya dan penguatannya dapat diatur.

Penguat instrumentasi dapat dibuat dengan menggunakan Op-Amp dan tahanan yang membuat rangkaiannya sangat stabil dan berguna bilamana ketelitian merupakan hal yang sangat penting.

2.2.1. Penguat Diferensial Tersangga

Penguat diferensial dasar mempunyai kekurangan dalam hal resistansi masukannya kecil sehingga perbandingan tahanannya harus disesuaikan dengan cermat akan tetapi resistansi tersebut dapat dihilangkan dengan menyangga atau mengisolasi masukan-masukannya. Hal ini menggunakan dua Op-Amp sebagai diferensial tersangga. Keluaran dari Op-Amp A_1 terhadap ground adalah E_1, dan keluaran dari Op-Amp A_2 terhadap ground adalah E_2. tegangan keluaran diferensial V_0 yang ditimbulkan melintasi tahanan R_L. Bila E_1 lebih besar dari E_2 menentukan harga V_0.

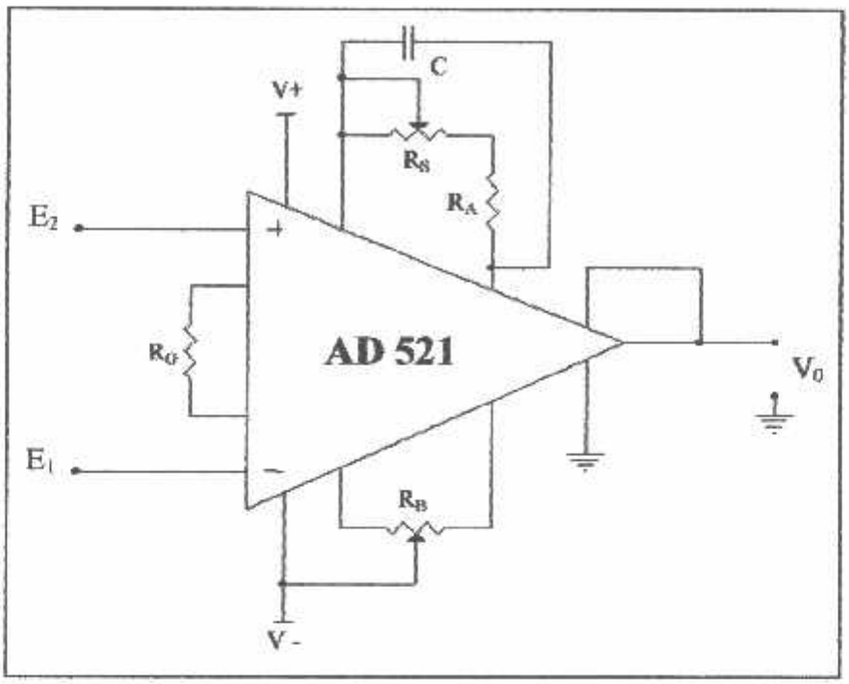
$$V_0 = E_1 - E_2 \qquad (2\text{-}9)$$



Gambar 2-2. Masukan diferensial tersangga ke penguat keluaran diferensial[2]

2.2.2. Penguat Diferensial Dasar

Rangkaian penguat diferensial dasar terdapat dua masukan E_1 dan E_2 yang dihubungkan ke terminal Op-Amp. R_S dan R_A digunakan sebagai resistor variabel untuk R_S berfungsi sebagai pengatur besarnya gain sehingga dapat diatur sesuai dengan keinginan sedangkan R_A berfungsi untuk menyetel tegangan ofset sehingga nilai $V_0 = 0$ V. Penguat diferensial dasar ditunjukkan pada gambar berikut :



Gambar 2-3. Penguat diferensial dasar

Dari gambar diatas didapat

$$\text{Gain} = \frac{R_S + R_A}{R_G} \tag{2-10}$$

V_0 pada penguat diferensial dasar adalah

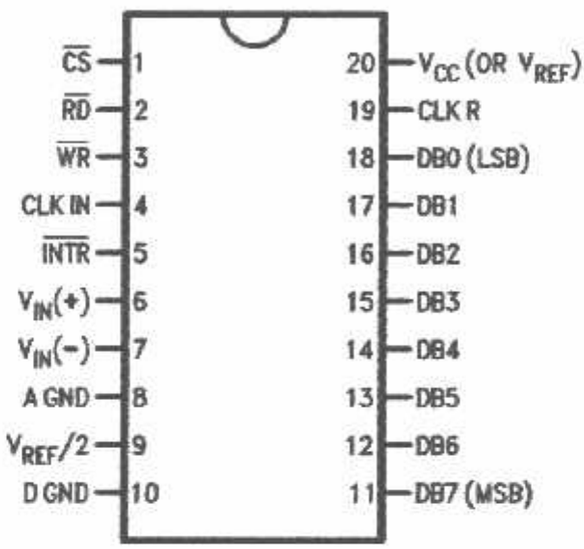
$$V_0 = \frac{Gain}{E_1 - E_2} \tag{2-11}$$

2.3. Analog to Digital Converter

2.3.1. Successive Approximation register (SAR)

Proses konversi besaran analog menjadi besaran digital merupakan proses penting dalam sistem akuisisi data. Proses konversi ini dilakukan oleh sebuah perangkat yang dinamakan *Analog to Digital Converter* atau ADC.

Pemilihan komponen sesuai dengan kebutuhan karena masing-masing jenis ADC memiliki resolusi, akurasi, stabilisasi kecepatan konversi dan harga yang berbeda-beda, dalam hal ini menggunakan ADC 0804 buatan National Semi conductor, dimana ADC memiliki sistem konversi secara pendekatan berturut-turut atau *successive approximation.*



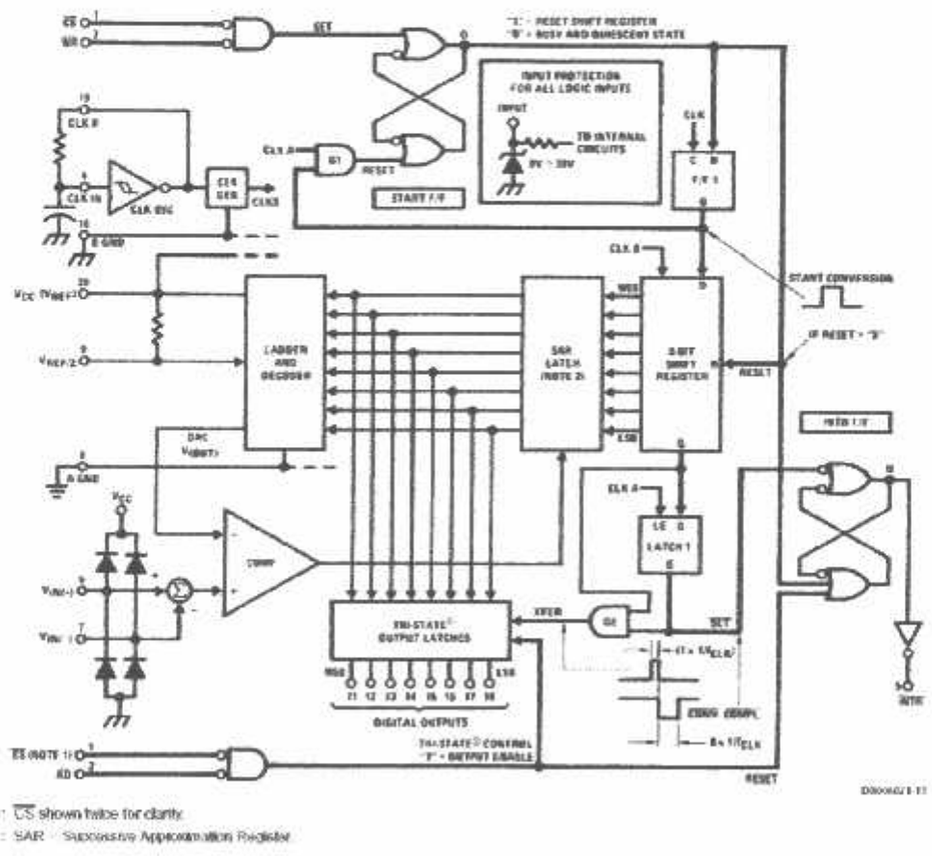
Gambar 2-4. Konfigurasi pin ADC 0804[3]

ADC 0804 memiliki kelebihan antara lain, mudah untuk interfacing dengan komputer, serta kecepatan konversi yang cukup tinggi dan memungkinkan untuk resolusi tinggi (8-bit). Pada ADC ini konversi dilakukan dengan cara membandingkan input yang tidak diketahui dengan sebuah tegangan referensi yang dibangkitkan oleh sebuah DAC. Input dari DAC berasal dari output digital SAR. Pembandingan dilakukan bit per bit, mulai dari bit yang terbesar sampai bit yang terkecil. Setelah SAR direset dengan output awal '1000 0000', output DAC dibandingkan dengan tegangan input analog lewat komparator. Bilamana input

lebih besar dari MSB tersebut, bit ini akan bernilai '1' dan bit berikutnya dites. Bila input kurang dari MSB, bit tersebut akan bernilai '0', bit kedua tidak dapat membuat output DAC lebih besar dari input analog, bit ini akan diset '1'. Dan bit ketiga dites. Bila pemberian '1' pada bit kedua membuat output DAC kali ini lebih besar dari input analog maka bit ini akan bernilai '0', proses ini berlangsung terus-menerus sampai LSB atau sampai pada pendekatan terakhir.

2.3.2. Pengoperasian ADC 0804

ADC 0804 memiliki satu line input analog dengan tegan referensi + 5 volt. Data digital 8 bit maksimal (Dmax) adalah 1111 1111 dalam biner atau FF dalam hexadesimal atau 255 dalam desimal.



CS shown twice for clarity.
SAR = Successive Approximation Register

Gambar 2-5. Diagram Blok ADC[3]

Besarnya resolusi dapat dihitung dengan menggunakan rumus :

$$\text{Resolusi (R)} = \frac{\text{Vref}}{2^n - 1} \qquad (2\text{-}12)$$

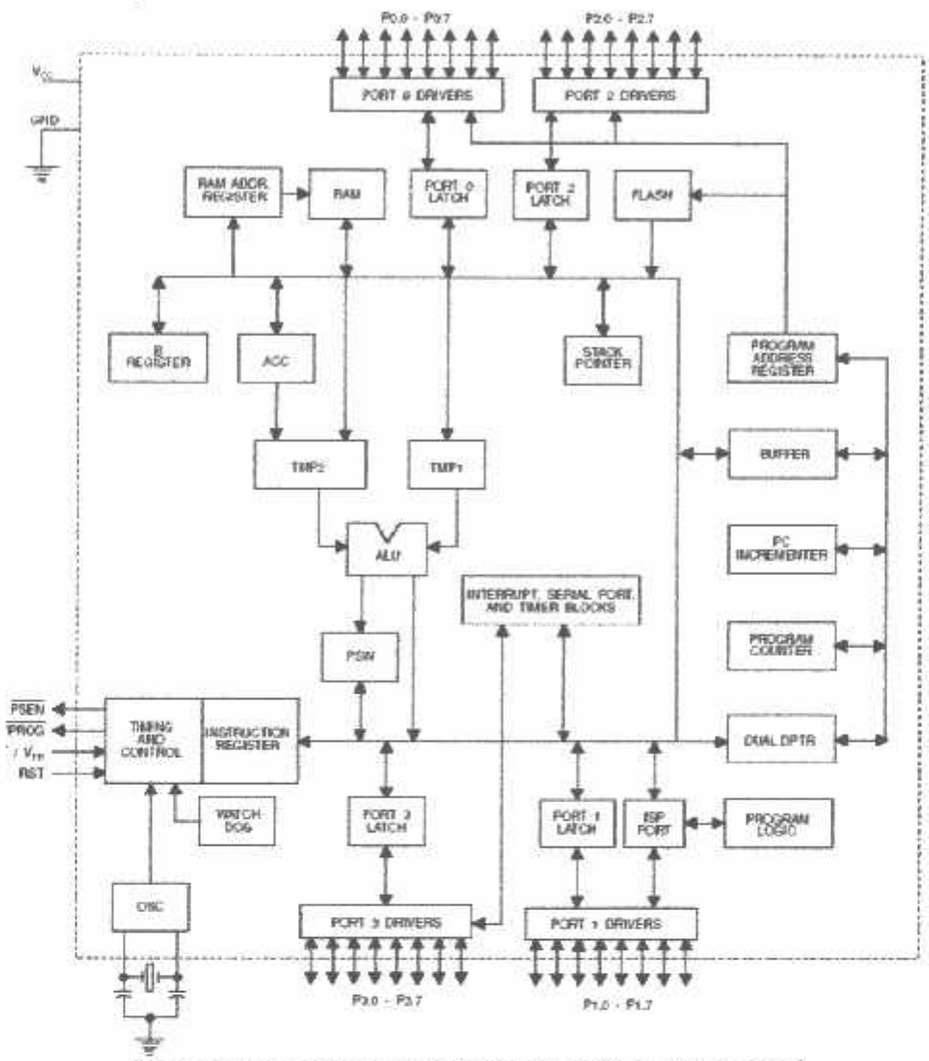
Dimana : n = jumlah bit

2.4. Mikrokontroler AT89S52

2.4.1. Fitur mikrokontroler AT89S52

Mikrokontroler AT89S52 merupakan salah satu keluarga MCS-51 keluaran Atmel yang mempunyai 40 kaki, 32 kaki diantaranya digunakan sebagai port paralel. Satu port paralel terdiri dari 8 kaki dengan demikian 32 kaki membentuk 4 buah port paralel, yang masing-masing dikenal dengan port 0, port 1, port 2, port 3. Jenis mikrokontroler ini pada prinsipnya dapat digunakan untuk mengolah data per bit ataupun data 8 bit secara bersamaan.

Sebuah mikrokontroler dapat bekerja bila dalam mikrokontroler tersebut terdapat sebuah program yang berisi instruksi-instruksi yang akan digunakan untuk menjalankan sistem mikrokontroler tersebut. Pada prinsipnya program pada mikrokontroler dijalankan secara bertahap, jadi dalam program itu sendiri terdapat beberapa set instruksi dan tiap instruksi itu dijalankan secara bertahap atau berurutan.

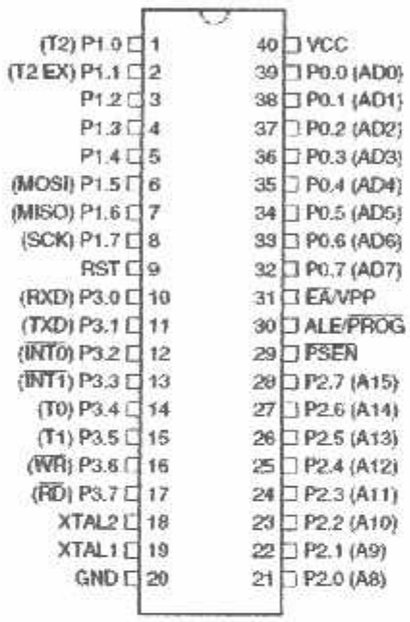


Gambar 2-6. Diagram Blok mikrokontroler AT89S52[4]

Beberapa spesifikasi yang dimiliki oleh mikrokontroler AT89S52 adalah sebagai berikut :

- Kompatibel dengan semua produk MCS-51
- 8K byte ISP *flash memory*
- 3 level program memori *lock*
- 256 byte RAM *internal*
- Jalur I/0 dua arah 32 buah
- 3 buah *timer/counter* 16-bit

- *Programmable* UART (serial port)
- *Programmable watchdog timer*
- *Dual data pointer*
- Frekuensi kerja 0 sampai 33 MHz
- Teganan operasi 4,0 Volt sampai 5,5Volt



Gambar 2-7. Mikrokontroler Atmel AT89S52[4]

Semua pin pada mikrokontroler Atmel AT89S52 adalah sama dengan mikrokontroler MCS-51. Penjelasan untuk masing-masing pin dari mikrokontroler adalah sebagai berikut :

- **VCC** digunakan sebagai catu daya
- **Gnd** digunakan sebagai ground
- **Port 0** (P0) merupakan port paralel 8-bit dua arah dan memiliki alamat 80H. Posisi *low significant* bit (LSB) terletak pada pin 39 dan *most significant* (MSB) terletak pada pin 32.

- **Port 1** (P1) merupakan port paralel 8-bit dua arah dan memiliki alamat 90H. Posisi LSB terletak pada pin 1 dan LSB terletak pada pin 8. Penyangga keluaran port 1 mampu memberikan menyerap arus empat masukan TTL (sekitar 1,6 mA). Port ini mempunyai beberapa fungsi khusus ditunjukkan pada tabel dibawah ini :

Tabel 2-1. Fungsi khusus port 1 pada AT89S52

Pin-pin pada port 1	Fungsi pengganti
P1.0	T2 (masukan luar untuk timer/counter 2)
P1.1	T2 EX (timer/counter 2 capture/ reload triger dan control arah)
P1.2	-
P1.3	-
P1.4	-
P1.5	MOSI (Master Data Output, Slave Data Input untuk kanal SPI)
P1.6	MISO (Master Data Input, Slave Data Output untuk kanal SPI)
P1.7	SCK (Master clock output, Slave clock input untuk kanal SPI)

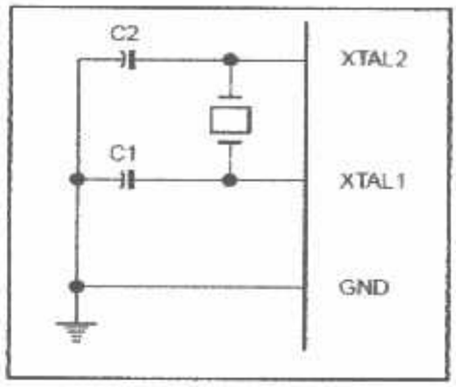
- **Port 2** (P2) merupakan port paralel 8-bit dua arah dan memiliki alamat A0H. Posisi *low significant* bit (LSB) terletak pada pin 21 dan *most significant* (MSB) terletak pada pin 28. Penyangga keluaran port 2 mampu memberikan menyerap arus empat masukan TTL (sekitar 1,6 mA).
- **Port 3** (P3) merupakan port paralel 8-bit dua arah dan memiliki alamat B0H. Posisi LSB terletak pada pin 10 dan LSB terletak pada pin 17.

Penyangga keluaran port 3 mampu memberikan menyerap arus empat masukan TTL (sekitar 1,6 mA). Port ini mempunyai beberapa fungsi khusus ditunjukkan pada tabel dibawah ini :

Tabel 2-2. Fungsi khusus port 3 pada AT89S52

Pin-pin pada port 3	Fungsi pengganti
P3.0	RXD (port input serial)
P3.1	TXD (port output serial)
P3.2	INT0 (interrupt eksternal 0)
P3.3	INT1 (interrupt eksternal 1)
P3.4	T0 (input eksternal timer 0)
P3.5	T1 (input eksternal timer 1)
P3.6	WR (perintah write pada memori eksternal)
P3.7	RD (perintah read pada memori eksternal)

- **RST** (reset) pada kondisi high akan aktif selama dua siklus.
- **ALE/PROG** atau *Adreess Latch Enable* menghasilkan pulsa-pulsa untuk mengancing byte rendah (*low byte*) alamat selama pengaksesan memori eksternal.
- **EA/Vpp** atau *External Access Enable* pada kondisi low maka mikrokontroler menjalankan instruksi-instruksi yang ada pada memori internal.
- **XTAL 1** sebagai masukan dari rangkaian osilator.
- **XTAL 2** sebagai keluaran dari rangkaian osilator.

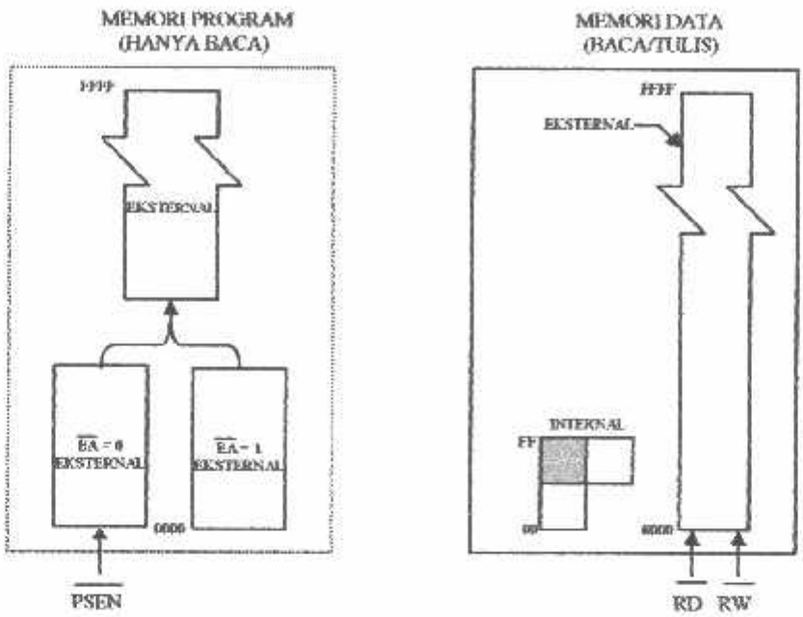


Gambar 2-8. Rangkaian osilator[4]

2.4.2. Organisasi memori

Mikrokontroler AT89S52 mengimplementasikan ruang memori yang terpisah antara program dan data. Kapasitas memori internal 8 Kb, tetapi keduanya dapat diperluas dengan memori *eksternal* sampai 64 Kb memori program dan 64 Kb memori data. Memori *eksternal* ini dapat diaktifkan dengan sinyal PSEN, sedangkan pin EA dinolkan ke ground, maka akan menghasilkan sinyal *Write* (WR) dan *read* (RD).

Namun AT89S52 telah memiliki ROM *internal* sebanyak 8 Kb yang dipakai sebagai memori program serta RAM *internal* sebanyak 256 byte yang digunakan sebagai memori data. Penunjukkan alamat kedua memori ini dihasilkan melalui register *Data Pointer* (DPTR).



Gambar 2-9. Struktur memori program dan data[8]

2.4.3. Special Function register (SFR)

Special Function Register atau SFR adalah register-register yang mempunyai fungsi khusus, di antaranya ada yang digunakan untuk mengatur input output data dari mikrokontroler. Misalnya register P0, P1, P2, dan P3 digunakan sebagai register untuk menampung data input/output. Selain itu juga digunakan untuk mengatur dan memantau kondisi UART, yaitu pada register SCON. Register yang mengatur kerja *timer* adalah TCON.

2.4.3.1. Accumulator

Accumulator menempati lokasi E0H merupakan register yang berfungsi menyimpan data sementara dalam program. Register accumulator ini sering digunakan dalam proses operasi aritmatika, logika, pengambilan dan penerimaan data.

2.4.3.2. Register B

Register B menempati lokasi F0H digunakan untuk operasi perkalian dan pembagian untuk instruksi lain dapat diperlakukan sebagai register *scratch pad* (Papan coret-coret).

2.4.3.3. Register Port

Register ini terdapat 4 buah yaitu register P0, P1, P2, dan P3 masing-masing menempati lokasi 80H, 90H, A0H, dan B0H digunakan sebagai sarana input/output untuk menyimpan data dari atau ke masing-masing port 0, port 1, port 2, dan port 3.

2.4.3.4. Register Timer

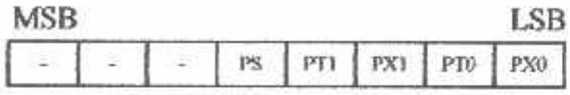
Mikrokontroler AT89S52 mempunyai tiga buah 16-bit timer , yaitu timer 0, timer 1, dan timer 2. Timer 0 dibentuk oleh register TH0 dan TL0 di lokasi 8CH dan 8AH. Timer 1 dibentuk oleh register TH1 dan TL1 di lokasi 8DH dan 8BH. Timer 2 dibentuk oleh register TH2 dan TL2 di lokasi CDH dan CCH. Perilaku dari register TH0, TH1, TH2, TL0, TL1, dan TL2 diatur oleh register TMOD dan register TCON.

2.4.3.5. Register Control

Ada beberapa register yang berisi bit-bit kontrol dan status untuk sistem interupsi, pencacah atau pewaktu, dan port serial antara lain :

- Register IP (*Interrupt Priority*) digunakan untuk mengatur prioritas dari masing-masing interupsi. Tingkat prioritas semua sumber *interupt* dapat diprogram sendiri-sendiri dengan *set* atau *clear* bit pada (*Interupt Priority*). Jika dua permintaan interupsi dengan tingkat prioritas yang

berbeda diterima secara bersamaan, permintaan interupsi dengan prioritas tertinggi yang akan dilayani. Jika permintaan interupsi dengan prioritas yang sama diterima bersamaan, akan dilakukan polling untuk menentukan mana yang akan dilayani. Bit-bit pada IP adalah sebagai berikut:



Priority bit = 1 menandakan prioritas tinggi (*high priority*)

Priority bit = 0 menandakan prioritas rendah (*low priority*)

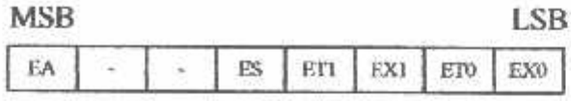
Gambar 2-10. Register IP pada mikrokontroler AT89S52[8]

Tabel 2-3. Register IP pada mikrokontroler AT89S52

Simbol	Posisi	Fungsi
-	IP.7	Cadangan
-	IP.6	Cadangan
-	IP.5	Cadangan
PS	IP.4	Bit interupsi port serial
PT1	IP.3	Bit interupsi timer 1 overflow
PX1	IP.2	Bit interupsi eksternal 1
PT0	IP.1	Bit interupsi timer 0 overflow
PX0	IP.0	Bit interupsi eksternal 0

- Register IE (*Interrupt Enable*) digunakan untuk mengaktifkan atau menonaktifkan sarana interupsi. IE.0 sampai IE.6 mengatur masing-masing sumber interupsi, sedangkan IE.7 mengatur interupsi secara keseluruan. Jika IE.7 bernilai 0 maka sistem interupsi akan non aktif atau keadaan dari IE.0 sampai IE.6 tidak diperhatikan. Masing-masing sumber interupsi dapat diaktifkan dan dimatiakan secara individual atau me-nol-kan bit-bit IE (*interrupt Enable*) dalam SFR. Register IE ini juga mengandung sebuah bit untuk aktivasi interupsi secara global, yang dapat

digunakan untuk mengaktifkan dan mematikan interupsi secara keseluruan.



Jika isinya = 1 artinya bit aktif (*enable*)

Jika isinya = 0 artinya bit pasif (*disable*)

Gambar 2-11. Register IE pada mikrokontroler AT89S52[8]

Tabel 2-4. Register IE pada mikrokontroler AT89S52

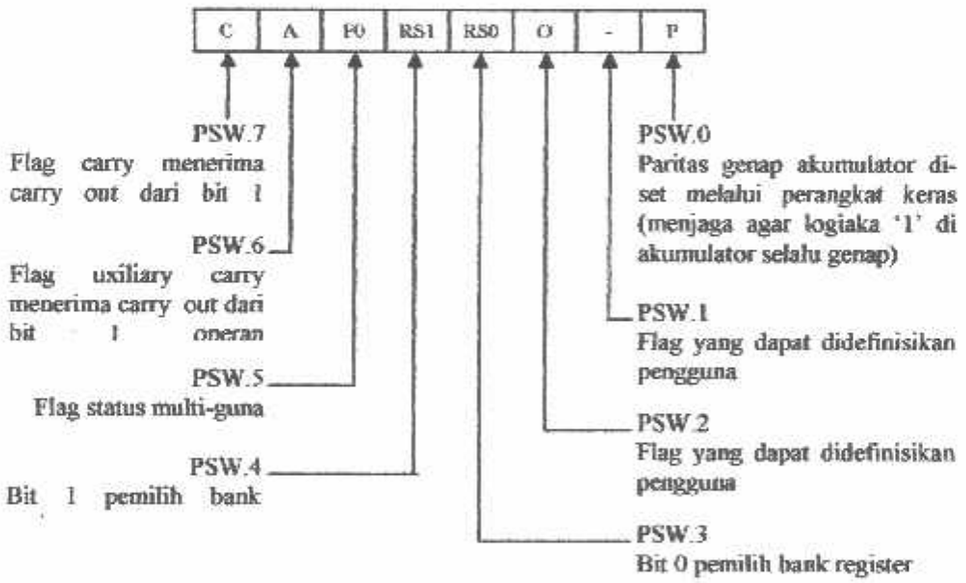
Simbol	Posisi	Fungsi
EA	IE.7	Untuk menghidupkan (IE=1)dan mematikan (IE=0)
-	IE.6	Cadangan
-	IE.5	Cadangan
ES	IE.4	Bit interupsi port serial
ET1	IE.3	Bit interupsi timer 1 overflow
EX1	IE.2	Bit interupsi eksternal 1
ET0	IE.1	Bit interupsi timer 0 overflow
EX0	IE.0	Bit interupsi eksternal 0

- Register TMOD (*Timer Mode*) digunakan untuk mengatur mode kerja timer. Dengan mengatur mode kerja timer untuk diatur menjadi timer 16-bit, timer13-bit, atau timer 8-bit. Selain itu register ini juga dapat mengatur agar proses pencacah timer dapat dikendalikan malalui sinyal dari luar mikrokontroler.
- Register TCON (*Timer Control*) digunakan untuk memulai atau menghentikan proses pencacah timer, mengatur sinyal interupsi dari INT0 atau INT1.

- Register SCON (*Serial Control*) digunakan untuk mangatur perilaku dari UART yang diantaranya memantau proses pengiriman dan penerimaan data seri.
- Register PCON (*Power Control*) digunakan untuk mengatur pemakaian daya pada IC.

2.4.3.6. Program Status Word

Register *Program Status Word* (PSW) menempati lokasi D0H ini berisi informasi status program yang mana masing-masing bit menunjukkan kondisi *Central Processing Unit* (CPU) setelah operasi dijalankan. Terdiri atas beberapa bit sebagai berikut:



Gambar 2-12. Register PSW dalam mikrokontroler AT89S52[8]

2.4.3.7. Stack Pointer

Register *Stack Pointer* (SP) menempati lokasi 81H merupakan register 8-bit yang terletak pada alamat 81H yang mempunyai fungsi untuk menyimpan data pada saat terjadi interrupt.

2.4.3.8. Data Pointer

Register *Data Pointer* (DPTR) merupakan register 16-bit atau sebagai dua register 8-bit yang terpisah yaitu data pointer high byte (DPH) dan data pointer low byte (DPL) yang masing-masing menempati lokasi 83H dan 82H.

2.4.3.9. Serial Data Buffer

Serial Data Buffer (SBUF) terletak pada lokasi 99H yang dibagi menjadi dua register terpisah, yaitu penyangga pengirim atau *transmit buffer* dan penerima atau *receive buffer*. Pada saat data disalin ke SBUF, maka data sesunggunya dikirim ke penyangga pengirim dan sekaligus mengawali transmisi data serial. Sedangkan pada saat data disalin dari SBUF, maka sebenarnya data tersebut berasal dari penyangga penerima.

2.4.4. Mode Pengalamatan

Data atau operan bisa berada ditempat yang berbeda sehingga dikenal beberapa cara untuk mengakses data tersebut yang dinamakan sebagai mode pengalamatan (*addressing mode*).

1. Pengalamatan langsung (*Direct Addressing*)

Dalam pengalamatan langsung, operan-operan ditentukan berdasarkan alamat 8-bit dalam suatu instruksi. Hanya RAM data internal dan SFR yang bisa diakses secara langsung.

2. Pengalamatan tak langsung (*Indirect Addressing*)

Dalam pengalamatan tak langsung, instruksi menentukan suatu register yang digunakan untuk menyimpan alamat operan. Baik RAM internal maupun eksternal dapat diakses secara tak langsung.

Register alamat untuk alamat-alamat 8-bit bisa menggunakan *stack pointer* atau R0 atau R1 dari bank register yang dipilih. Sedangkan untuk alamat 16-bit hanya bisa menggunakan register pointer 16-bit atau DPTR.

3. Instruksi-instruksi register

Bank-bank register yang masing-masing R0 hingga R7 atau 8 register dapat diakses melalui instruksi yang OP-kodenya mengandung 3-bit spesifikasi register (000 untuk R0, 001 untuk R1 hingga 111 untuk R7). Pengaksesan register dengan cara demikian bisa menghemat penggunaan kode instruksi, karena tidak memerlukan sebuah byte untuk alamat. Saat instruksi tersebut dijalankan satu dari delapan register pada bank yang terpilih yang diakses.

4. Instruksi-instruksi register khusus

Beberapa instruksi hanya dikhususkan untuk suatu register tertentu. Misalnya suatu instruksi yang hanya bekerja pada akumulator saja, sehingga tidak memerlukan alamat byte untuk menunjuk ke akumulator tersebut. Dalam hal ini op-kodenya sendiri telah mengandung penunjuk ke register yang benar. Instruksi yang mengacu akumulator sebagai A akan dikodekan dengan op-kode spesifik akumulator.

5. Konstata langsung (*Immediate Constants*)

Nilai dari suatu konstanta dapat segera menyatu dengan op-kode dalam memori program. Misalnya instruksi : MOV A,#100, yang akan menyimpan konstanta 100 (desimal) ke dalam akumulator. Bilangan yang sama tersebut bisa juga dituliskan dengan format heksa sebagai 64H.

6. Pengalamatan terindeks (*Indexed Addressing*)

Memori program hanya dapat diakses melalui pengalamatan terindeks. Mode pengalamatan ini ditunjukan untuk membaca tabel (look-up tables) yang tersimpan dalam memori program. Sebuah register dasar 16-bit menunjuk ke awal atau dasar tabel dan akumulator di-set dengan angka indek tabel yang akan diakses. Alamat dari entri tabel dalam memori program dibentuk dengan menjumlahkan data akumulator dengan penunjuk awal tabel.

Type lain dari pengalamatan terindeks digunakan dalam interuksi-interuksi "lompat bersyarat". Dalam hal ini alamat tujuan dari interuksi lompat (*jump*) dihitung sebagai jumlah penunjuk dasar (*base pointer*) dengan data akumulator.

2.4.5. Set instruksi

Secara keseluruan MCS51 mempunyai 255 macam instruksi, yang dibentuk dengan mengkombinasikan dan operan. Instruksi tersebut dikelompokkan menjadi berikut :

1. Kelompok penyalin data

Instruksi dasar untuk kelompok ini adalah MOV, singkatan dari move yang artinya memindahkan, meskipun demikian lebih tepat dikatakan instruksi ini mempunyai arti menyalin data. Misalnya, instruksi-instruksi berikut ini :

```
MOV  A, 20H      ; salin isi lokasi memori 20H ke akumulator A
MOV  A, @R1      ; salin isi lokasi yang ditunjuk R1 ke A
MOV  A, P1       ; salin isi latch port 1 ke A
MOV  P3, A       ; salin isi A ke latch port 3
```

Untuk pemakaian pada memori program , instruksi ini ditulis menjadi MOVC, hanya ada 2 jenis instruksi yang menggunakanya yaitu :

```
MOVC  A, @A+DPTR      ; DPTR sebagai register tak langsung
MOVC  A, @ A+PC       ; PC sebagai register tak langsung
```

Selain itu masih dikenal pula instruksi MOVX yang digunakan untuk mengakses memori data eksternal. Hanya ada 6 macam instruksi yang memakai MOVX, antara lain :

```
MOVX  A,@DPTR      ; salin data eksternal pada lokasi DPTR ke A
MOVX  A,@R0        ; salin data eksternal pada lokasi R0 ke A
MOVX  A,@R1        ; salin data eksternal pada lokasi R1 ke A
MOVX  @DPTR, A     ; salin data eksternal dari A ke lokasi DPTR
MOVX  @R0, A       ; salin data eksternal dari A ke lokasi R0
MOVX  @R1,A        ; salin data eksternal dari A ke lokasi R1
```

2. Kelompok instruksi aritmatik

Instruksi-instruksi dalam aritmatik ini selalu melibatkan akumulator, hanya beberapa yang juga melibatkan register lainya. Instruksi yang termasuk dalam kelompok ini, antara lain :

A. Instruksi ADD dan ADDC

Isi akumulator A ditambahkan dengan suatu bilangan (1 byte), maka hasil penjumlahannya akan ditampung kembali dalam akumulator. Dalam operasi ini bit *Carry* berfungsi sebagai penampung limpahan hasil penjumlahan. Jika hasil penjumlahan tersebut melimpah maka bit *Carry* akan bernilai '1' jika tidak *Carry* akan selalu bernilai '0'.

B. Instruksi SUBB

Isi akumulator dikurangi dengan bilangan (1 byte) besertadengan nilai bit *Carry*, hasil pengurangan akan ditampung kembali dalam akumulator.

Dalam hal ini bit *Carry* juga berfungsi sebagai penampung limpahan dari hasil pengurangan. Jika hasil pengurangan tersebut melimpah maka bit *Carry* akan bernilai '1' jika tidak akan bernilai '0'.

C. Instruksi DA A

Instruksi DA A (*Decimal Adjust*) dipakai setelah instruksi ADD, ADDC atau SUBB, digunakan untuk merubah nilai biner8-bit yang tersimpan dalam akumulator menjadi 2 digit bilangan dalam format BCD (*Binary Code Decimal*).

D. Instruksi MUL AB

Bilangan biner 8-bit dalam akumulator A dikalikan dengan bilangan biner 8-bit dalam register B. Hasil perkalian berupa bilangan biner 16-bit, 8-bit bilangan biner yang bagian atas (*high byte*) disimpan di register B. Sedangkan 8-bit lainya (*low byte*) disimpan di akumulator A.

E. Instruksi DIV AB

Bilangan biner 8-bit dalam akumulator A dibagi dengan bilangan biner 8-bit dalam register B. Hasil perkalian berupa bilangan biner 16-bit, 8-bit bilangan biner yang bagian atas (*high byte*) disimpan di register B. Sedangkan 8-bit lainya (*low byte*) disimpan di akumulator A.

F. Instruksi DEC dan INC

Interuksi DEC digunakan untuk menurunkan satu nilai (1 byte). Jika nilai awal adalah 00H, maka setelah dilaksanakan instruksi ini hasilnya adalah FFh. Tidak ada flag yang terpengaruh. Sedangkan instruksi INC digunakan untuk menaikkn nilai (1 byte). Jika nilai awalnya adalah FFH maka setelah dilaksanakan instruksi ini menjadi 00H.

G. Instruksi INC DPTR

Instruksi penaikkan (*increment*) yang bekerja pada data 16-bit yaitu DPTR. Yaitu menaikkan penunjuk data sebesar 1. suatu limpahan dari byte rendah (*low order*) dari DPTR atau DPL akan menaikkan byte tinggi (*high order*) yaitu yang tersimpan dalam DPH sebesar 1.

3. Kelompok instruksi logika

Kelompok instruksi ini dipakai untuk melakukan operasi logika, yaitu operasi AND (*instruksi* ANL), operasi OR (Instrukai ORL),operasi exlusive OR (instruksi XRL), operasi clear (instruksi CLR), instruksi negasi atau komplemen (instruksi CPL), operasi pergeseran kanan atau kiri (instruksi RR, RRC, RL dan RLC) serta operasi pertukaran data (instruksi SWAP).

2.5. Relay

Relay adalah komponen elektronika yang umumnya digunakan untuk menghidupkan rangkaian kontrol dan peralatan listrik lainnya yang memerlukan arus relatif kecil, namun demikian relay dapat mengontrol tegangan dan arus yang lebih besar dengan menggunakan efek penguatan. Efek penguatan ini didapat dengan dengan memanfaatkan tegangan kecil (5 - 24 Volt) untuk mengoperasikan koil dari relay, kemudian relay tersebut digunakan untuk mengubah-ubah posisi kontak. Kontak pada relay dapat digunakan untuk mensaklar (switching) tegangan yang lebih besar. Sebuah relay terdiri dari satu kumparan dan inti, yang mana bila dialiri arus listrik, kumparan tersebut akan menjadi magnet dan menutup atau membuka kontak – kontak.

Pada dasarnya relay dapat dikatakan sebagai kontak beban elektrik yang mengontrol suatu rangkaian elektrik dengan cara membuka dan menutup kontak

pada rangkaian lain. Apabila kontak relay adalah *Normaly Open* (NO), maka akan terbuka bila relay tidak dialiri arus listrik. Sebaliknya, pada titik kontak relay yang tergolong *Normaly Close* (NC) akan tertutup bila relay tidak dialiri arus listrik. Pada kedua kondisi tersebut kontak–kontak pada relay akan berubah keadaannya apabila relay dialirai arus listrik.

Ada beberapa jenis susunan kontak relay, dimana semuanya terisolasi terhadap arus listrik yang ada didalam kumparan. Jenis susunan kontak sebagai berikut:

1. *Normaly open* (normal terbuka)

   Yaitu kontak – kontak tertutup pada saat kumparan relay dialiri arus listrik.

2. *Normaly Close* (normal tertutup)

   Yaitu kontak – kontak terbuka pada saat kumparan relay dialiri arus listrik.

Adapun karakteristik dari sebuah relay adalah sebagai berikut :

- Tegangan operasi, yaitu tegangan koil minimum yang diperlukan oleh koil untuk dapat mengaktifkan kontak saklar relay dari posisi normal ke posisi operasi.
- Tegangan lepas, yaitu tegangan koil minimum yang diperlukan oleh koil untuk dapat mengaktifkan kontak saklar dari posisi operasi ke posisi normal.
- Tegangan maksimum yaitu, tegangan maksimum yang diperlukan koil untuk dapat bekerja tanpa merusak koil itu sendiri.
- Tegangan normal, adalah tegangan kerja nominal sehingga koil dapat bekerja secara normal.

Prinsip kerja dari sebuah relay adalah apabila lilitan terisolasi dari sebuah relay diberikan tegangan maka pada relay tersebut akan timbul induksi, dengan

adanya induksi ini maka besi (inti) yang diselubungi oleh lilitan akan berubah sifatnya menjadi magnet yang bersifat sementara, karena besi (inti) tersebut bersifat magnet maka akan dapat menarik besi lain yang berfungsi sebagi kontak sehingga relay menjadi aktif. Jika tegangan pada relay dihilangkan, maka besi (inti) akan kembali seperti sifat semula sehingga relay akan menjadi tidak aktif.

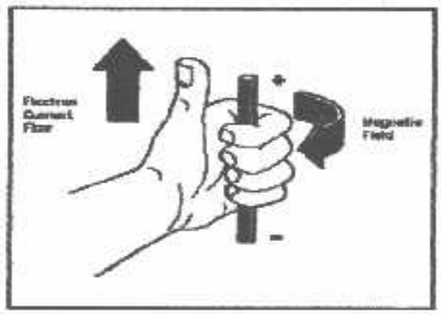
2.6. Motor arus searah

Motor arus searah (DC) adalah motor yang berfungsi untuk mengubah energi listrik menjadi energi mekanik yang berupa putaran pada rotor. Berdasarkan karakteristiknya motor DC ini mempunyai daerah pengaturan putaran yang lebih luas bila dibandingkan dengan motor AC, sehingga sampai sekarang motor DC masih banyak digunakan pada industri-industri seperti pabrik kertas, tekstil dan pabrik yang membutuhkan pengaturan motor.

2.6.1. Prinsip kerja motor arus searah

Prinsip dasar dari motor arus searah adalah kalau sebuah kawat berarus diletakkan antara kutub magnet (U-S), maka pada kawat tersebut akan bekerja suatu gaya yang akan menggerakkan kawat tersebut. Arah gerak dari kawat tersebut dapat ditentukan dengan " Kaidah Tangan Kiri " yang berbunyi sebagai berikut : " Apabila tangan kiri dibiarkan terbuka dan diletakkan diantara kutub utara dan kutub selatan, sehingga garis-garis gaya yang keluar dari kutub utara menembus telapak tangan kiri dan arus di dalam kawat mengalir searah dengan keempat jari, maka kawat tersebut akan mendapat gaya yang jatuhnya sesuai dengan ibu jari ". Ada tiga pokok dari kerja motor DC, antara lain :

1. Adanya garis gaya medan magnet (fluks) antara kutub-kutub yang berada di stator.
2. menempatkan kawat penghantar yang dialiri arus listrik pada jangkar yang berada dalam medan magnet.
3. Pada kawat penghantar timbul gaya yang menghasilkan torsi.



Gambar 2-13. Kaidah tangan kiri[1]

Arah dari garis gaya medan magnet (fluks) yang dihasilkan kutub, arah dari arus yang mengalir dan arah gaya adalah saling tegak lurus satu sama lain dengan kaidah tangan kiri. Jika panjang kumparan L dialiri arus listrik sebesar I dan terletak diantara kutub magnet utara dan selatan dengan kerapatan fluks sebesar B, maka kumparan rotor tersebut mendapat gaya sebesar :

$$F = B \cdot I \cdot L \qquad (2\text{-}13)$$

Dimana :

F = Gaya lorent

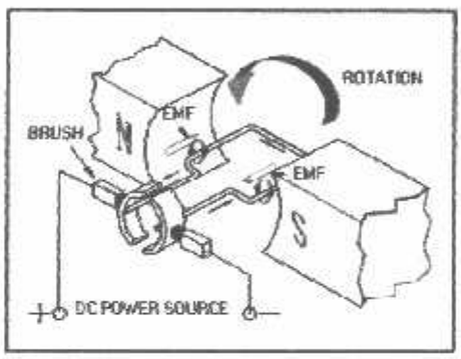
B = Kerapatan fluks magnet

I = Arus listrik

L = Panjang sisi kumparan rotor

2.6.2. Kontruksi motor DC

Motor DC mempunyai dua bagian utama yaitu stator dan rotor. Stator adalah bagian dari motor yang diam atau statis dan bagian ini terdiri dari badan (body) motor yang memiliki lempeng-lempeng magnet yang melekat pada badannya, untuk motor kecil lempeng-lempeng itu dari magnet permanen dan untuk motor besar, lempeng-lempeng itu berupa elektromagnetik dan terbuat dari bahan magnetik derajat tinggi. Kumparan yang dililitkan pada lempeng-lempeng magnet ini disebut kumparan medan.



Gambar 2-14. Kontruksi dasar motor DC[1]

Sedangkan motor adalah bagian dari motor yang bergerak atau dinamik dan bagian ini terdiri dari jangkar yang intinya terbuat dari lempeng-lempeng yang ditarik, susunan lempeng-lempeng tersebut memberikan celah-celah konduktor dan kumparan jangkar dimasukkan pada celah-celah tersebut. Ujung dari tiap kumparan dihubungkan pada satu segment komutator dan setiap segmen merupakan pertemuan antara dua ujung kumparan yang terhubung ke segmen.

2.6.3. Jenis-jenis motor arus searah

Motor arus searah dibedakan atas :

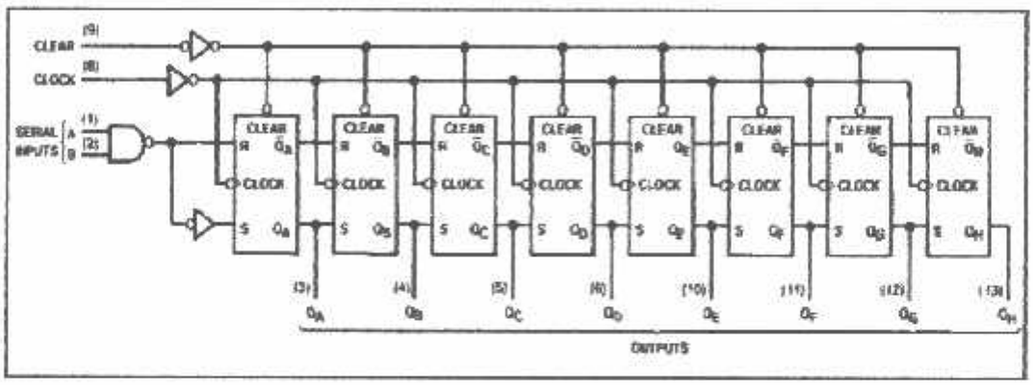
1. Berdasarkan atas sumber arus penguat magnetnya motor DC, yaitu :

- Motor DC dengan penguatan terpisah, bila sumber arus penguatan magnetnya diperoleh dari luar motor DC.
- Motor DC dengan penguatan sendiri, bila sumber arus penguatan magnetnya diperoleh dari dalam motor DC itu sendiri.

2. Berdasarkan hubungan lilitan penguat magnet terhadap lilitan jangkar, motor DC dibagi menjadi :
   - Motor DC shunt.
   - Motor DC seri.
   - Motor DC kompon, motor ini dibedakan menjadi dua, yaitu :
     a. Motor kompon pendek.
     b. Motor kompon panjang.

2.7. Register geser 8-bit 74LS164

Register adalah memori sementara yang digunakan untuk mengelolah data register geser (*shift register*) merupakan memori sementara yang dapat dipindahkan dengan jalan menggeser dari bit rendah ke bit tinggi atau sebaliknya. Dalam perancangan ini menggunakan register geser dengan masukan seri dan keluaran paralel 8-bit dengan type IC 74LS164.



Gambar 2-15. Diagram Blok IC 74LS164[7]

Prinsip dasar kerja dari register geser 74LS164 merupakan register kiri 8-bit adalah bila 1-bit data dimasukkan ke inputan bersama dengan naiknya pulsa clock maka 1-bit akan disimpan dan dikeluarkan oleh flip-flop RS yang pertama (QA), sedangkan keadaan keluaran yang lain (QB – QH) seperti keadaan semula dan apabila diinputkan lagi 1-bit ke dua bersama dengan clock, maka bit yang ada di Qa akan digeser ke QB. Sedangkan isi QA adalah bit yang baru diinputkan tersebut, dan itu akan berlaku terus menerus selama masukan diberi data bersama dengan pulsa clock untuk menghapus setiap register yaitu dengan memberikan sinyal low pada clear.

Tabel 2-5. Tabel kebenaran IC 74LS164[7]

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

2.8. LCD (*Liquid Crystal Display*)

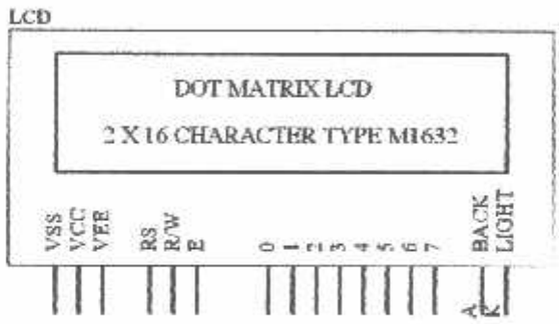
Untuk menampilkan hasil pengukuran yang telah diproses oleh mikrokontroler, maka dibutuhkan suatu perangkat yang dapat dipergunakan sebagai alat penampil data, sehingga pengguna dapat mengetahui data hasil pengukuran.

LCD adalah modul tampilan yang mempunyai konsumsi daya yang relatif rendah dan terdapat kontroler CMOS didalamnya. Kontroler tersebut sebagai pembangkit dari ROM/RAM dan display data RAM. Semua fungsi tampilan dikontrol oleh suatu instruksi dan modul LCD dapat dengan mudah diinterface dengan unit mikroprosesor maupun mikrokontroler. Masukan yang diperlukan untuk mengendalikan modul ini berupa bus data dari sinyal kontrol.

Dalam hal ini digunakan LCD type M1632 yang memiliki tampilan sebanyak 16 kolom dan 2 baris buatan seiko instrument dengan karakteristik sebagai berikut :

- Duty cycle 1/6.
- 16 x 2 karakter dengan 5 x 7 dot matriks.
- RAM generator karakter dengan 8 tipe karakter (untuk program write).

- Rangkaian oscillator terpadu.
- Memiliki ROM pembangkit karakter 192 jenis karakter.
- Maksimum display data RAM 80 x 8.
- Dapat diinterface 4-bit dan 8-bit.
- Catu daya tunggal + 5 volt.
- Otomatis reset saat power dinyalakan.
- Mampu bekerja pada temperature 0°C sampai 50°C



Gambar 2-16. LCD M1632

LCD ini mempunyai 16 pin yang dihubungkan dengan perangkat keras prosessor penunjang. Adapun fungsi dari masing-masing pin, ditunjukkan dalam tabel berikut ini :

Tabel 2-6. Fungsi pin LCD M1632

Nama	Pin	I/O	Fungsi
Vss	1	Power supply	Ground terminal.
VCC	2	Power supply	Tegangan + 5 Volt
VEE	3	Power supply	Tegangan supply yang digunakan untuk mengatur fokus dari layar LCD
RS	4	Input	Register selection signal 0 = Instruction register (write) Busy flag and address counter (read) 1 = Data register (write and read)
R/W	5	Input	Signal control untuk opcrasi read/write 0 = write 1 = read
E	6	Input	Operational start signal yaitu signal yang akan melatch data bus
DB0 – DB7	7 – 14	I/O	8-bit data bus yang digunakan menampilkan data dari MPU. DB7 juga sebagai digunakan sebagai *busy flag.*

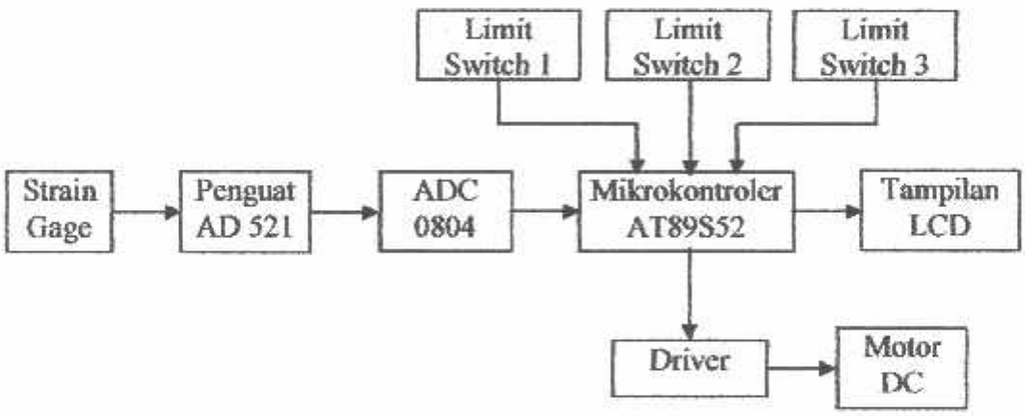
BAB III

PERENCANAAN DAN PEMBUATAN ALAT

3.1. Pendahuluan

Untuk merancang dan membuat alat ukur ini perlu dipahami terlebih dahulu diagram blok sistem, perhitungan-perhitungan dan merancang *software* dan *hardware*. Secara garis besar, perancangan terdiri dari dua bagian yaitu perancangan *Hardware* dan perancangan *Software*.

Untuk menggambarkan keseluruan unit dan hubungan tiap unit yang menyusun alat pengukur kekuatan benang dengan tampilan LCD berbasis mikrokontroler AT89S52, maka dapat dilihat pada blok diagram sebagai berikut:



Gambar 3-1. Diagram Blok Rangkaian

Prinsip kerja :

Dalam hal ini menggunakan strain gage yang dipakai sebagai sensor, Motor akan mundur apabila tombol start dalam kondisi aktif. Sehingga strain gage akan mengalami perubahan resistansi yang dihubungkan dengan menggunakan

rangkaian jembatan wheatstone sinyal yang dihasilkan sangat kecil sehingga membutuhkan penguatan sebesar 687,76 kali. Apabila limit switch 1 dalam kondisi aktif maka ADC yang berfungsi untuk mengubah sinyal analog menjadi sinyal digital akan bekerja memilih data yang terbesar kemudian mikrokontroler akan mengelolah data dari ADC kemudian ditampilkan ke dalam LCD. Apabila motor menyentuh limit switch 2 maka motor akan maju hingga menyentuh limit switch 3 hingga motor akan berhenti ke kondisi awal.

3.2. Perancangan Hardware

3.2.1. Strain gage

Dalam perancangan dam pembuatan alat pengukur kekuatan benang ini, strain gage disatukan dengan lempengan baja dengan ukuran :

Tebal = 1 mm

Lebar = 2,5 cm

Panjang = 15 cm

Modulus elastisitas baja : 20.10^{10} N/m^2

Dari data strain gage yang dipakai, diketahui :

R = 120 Ω

E = 5 V

GF = 2,1

ΔR = 0,7 Ω

Untuk mengatisipasi adanya beban lebih (*over load*) dan bengkok permanen maka kemampuan maksimal peralatan. Dari faktor pengukur diperoleh :

$$GF = \frac{\Delta R / R}{\Delta L / L}$$

$$2,1 = \frac{0,7/120}{\Delta L/L}$$

$$2,1 = \frac{5,8.\ 10^{-3}}{\Delta L/L}$$

$$\Delta L/L = \frac{5,8.\ 10^{-3}}{2,1}$$

$$\Delta L/L = 2,78.\ 10^{-3} \text{ per meter}$$

S(Tegangan) $= \Delta L/L$ x Modulus Elastisitas

$$= 2,78.10^{-3} \times 20.10^{10}$$

S (Tegangan) $= 556.10^{6}\ N/m^2$

$$S = \frac{6FD}{WT^2}$$

$$F = \frac{SWT^2}{6D}$$

$$= \frac{556.10^{6} \times 2,5.10^{-2} \times (1.10^{-3})^2}{6 \times 15.10^{-2}}$$

$$= \frac{1390}{90}$$

$$= 15,4 \text{ Newton}$$

F = 1,57 Kg

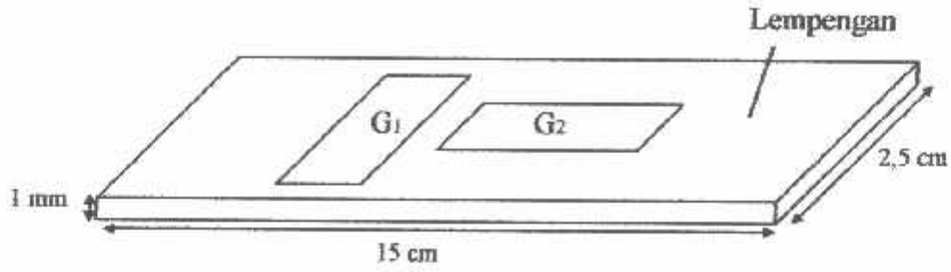
(1 Kg = 9,8068 Newton)

Dimana :

W = Lebar lempengan baja

D = Panjang lempengan baja

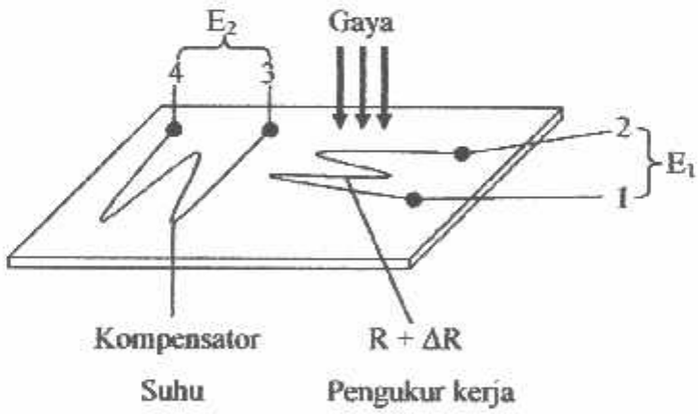
T = Tebal lempengan baja



Gambar 3-2. Pemasangan Strain Gage Pada Lempengan Baja

Beban seberat 1,57 Kg adalah beban terberat yang dapat diterima oleh strain gage. Dalam perencanaan alat ini beban maksimum dibatasi sampai 1,3 kg , agar tidak terjadi pembengkokan permanen pada lempengan strain gage.

Dalam rangkaian sensor gaya ini digunakan 2 buah strain gage. Strain gage 1 adalah strain gage aktif sedangkan strain gage 2 adalah dummy gage yang berfungsi sebagai kompensator suhu. Kompensator suhu dipasang dengan sumbu tegak lurus terhadap sumbu tegak lurus terhadap sumbu tegak dari strain gage aktif.

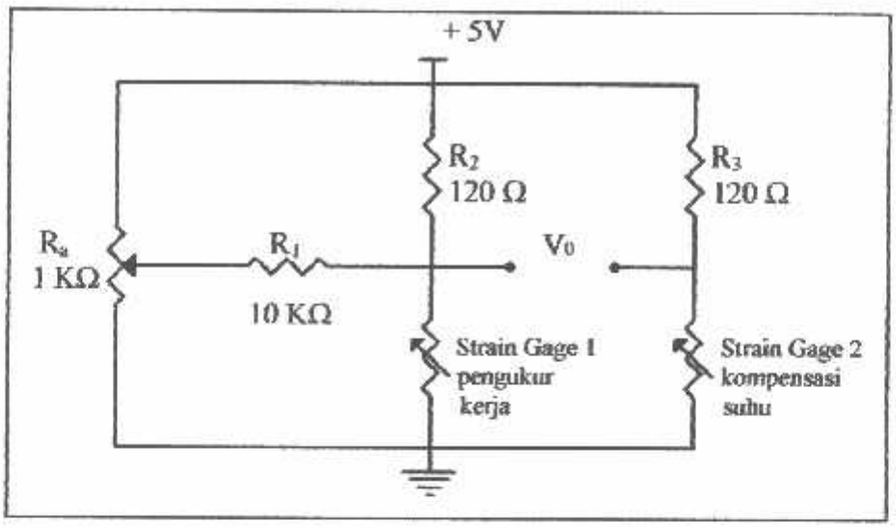


Gambar 3-3. Pemasangan Strain Gage Aktif dan Dummy Gage

Dimana :

G_2 = Kompensator suhu

G_1 = R + ΔR (Pengukur kerja)



Gambar 3-4. Rangkaian Jembatan Wheatstone

Untuk mengetahui besarnya tegangan output dari rangkaian tersebut, maka dapat dihitung dengan cara sebagai berikut :

$$V_0 = \left[\frac{G_1}{(G_1 + R_1)} - \frac{G_2}{(G_2 + R_2)}\right].Vin$$

$$= \left[\frac{G_1.R_2 - G_2.R_1}{(G_1 + R_1)(G_2 + R_2)}\right].Vin$$

$$= \left[\frac{120.120 - 120.120}{(120 + 120)(120 + 120)}\right].5 \text{ Volt}$$

$V_0 = 0$ volt

Pada saat ada beban, RG = R + ΔR, maka untuk beban maksimum yang dapat terukur harga ΔR = 0,7 Ω sehingga tegangan pada titik V_0 pada saat beban maksimal adalah :

$$V_0 = \left[\frac{G_1.R_2 - G_2.R_1}{(G_1 + R_1)(G_2 + R_2)}\right].Vin$$

$$= \left[\frac{120{,}7x120 - 120x120}{(120{,}7 + 120)(120 + 120)}\right]. 5 \text{ Volt}$$

$$V_0 = 7{,}27 \text{ mV}$$

Dari hasil perhitungan diatas, maka diketahui bahwa pada saat tidak ada beban $V_0 = 0$ V, sedangkan pada saat beban maksimal $V_0 = 7{,}27$ mV.

3.2.2. Penguat Instrumentasi

Penguat instrumentasi diperlukan untuk memperkuat output dari rangkaian sensor gaya yang merupakan besaran analog yang sangat kecil sehingga sesuai dengan level tegangan ADC sehingga dapat dikonversikan oleh ADC 0804.

Penguat instrumentasi yang digunakan dalam perencanaan ini menggunakan IC penguat operasional AD 521 dan TLC 272 yang digunakan sebagai diferensial tersangga tengangan gain yang tetap.

Output dari rangkaian sensor gaya berkisar antara 0 – 8,31 mV, sedangkan untuk ADC tegangan referensi yang digunakan adalah 0 - 5 V.

Diketahui :

$V_1 = E_1 - E_2$

$= 5$ V (Perencanaan)

$V_0 = 7{,}27.10^{-3}$ V

Dimana :

$R_4 = 100\ \Omega$

$R_5 = 10\ K\Omega$

Maka besarnya penguatan yang diperoleh :

$$\text{Gain} = \frac{V_i}{V_o}$$

$$= \frac{5}{7{,}27.10^{-3}}$$

$$= 687{,}76 \text{ Kali}$$

Sehingga dapat diperoleh nilai R_b yang dibutuhkan sebesar :

$$\text{Gain} = \frac{R_b + R_5}{R_4}$$

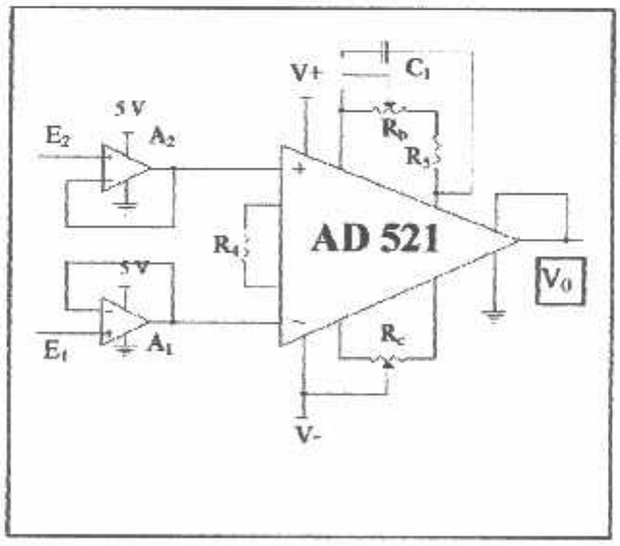
$$687{,}76 = \frac{R_b + 10.10^3}{100}$$

$$68776 = R_b + 10.10^3$$

$$R_b = 68776 - 10.10^3$$

$$R_b = 58776\ \Omega$$

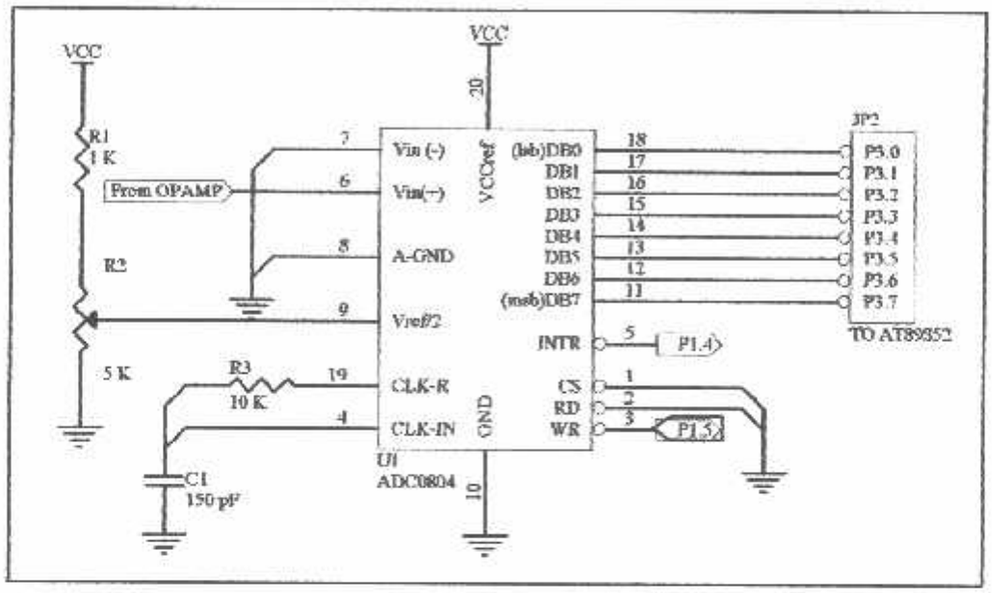
Dipilih $R_b > 58{,}776\ K\Omega$ misalnya $R_b = 100\ K\Omega$



Gambar 3-5. Rangkaian Penguat Instrumentasi

3.2.3. Rangkaian ADC

Untuk rangkaian pengubah besaran analog menjadi besaran digital digunakan IC 0804 yang mempunyai satu inputan analog dengan tegangan referensi + 5 volt, data digital 8 bit maksimal adalah 11111111 dalam biner atau FF dalam hexadecimal atau 255 dalam decimal.



Gambar 3-6. Rangkaian Interfacing ADC 0804

Pada gambar diatas terlihat bahwa pada pin RD dan CS langsung diaktifkan dengan menghubungkan kedua pin tersebut ke ground. Hal ini guna memungkinkan terselenggaranya pembacaan data dari bus data ADC (DB0 – DB7) ke port 1. pin 6 adalah masukan dari keluaran dari sensor yang dikuatkan, sinyal WR dan INTR masing-masing dihubungkan dengan P1.5 dan P1.4.

Pada pin 4 dan pin 19 dipasang rangkaian RC sebagai pembangkit osilasi ke rangkaian generator clock internal ADC. Frekuensi clock yang masuk pada ADC yang dihitung sebagai berikut :

$$f_{clk} = \frac{1}{(1,1.R.C)}$$

dimana :

f_{clk} = Frekuensi

R = Tahanan = 10 KΩ

C = Kapasitor = 150 pF

Maka :

$$f_{clk} = \frac{1}{(1{,}1.10\,K\Omega.150\,pF)}$$

$$= 606\ KHz$$

Dengan frekuensi clock sebesar 606 KHz, maka waktu yang diperlukan internal ADC adalah

$$T_{clk} = \frac{1}{f_{clk}}$$

$$= \frac{1}{606.10^3}$$

$$= 1{,}65\ \mu s$$

Besarnya resolusi dapat dihitung dengan menggunakan rumus :

$$\text{Resolusi (R)} = \frac{Vref}{2^n - 1}$$

Dimana : n = jumlah bit

Diketahui : Vref = 5 volt

n = 8 bit

maka besarnya resolusi :

$$R = \frac{5}{255}$$

$$= 19{,}6\ mv$$

$\approx 0{,}02$ volt

Data output dari ADC

Jika diketahui

Vin $= 0.04$ volt

$$\text{Output ADC} = \frac{0{,}04 \text{ volt}}{0{,}02 \text{ volt}}$$

$= 2$ (bilangan desimal)

$= 00000010$ (bilangan biner)

$= 2\text{ H}$ (bilangan hexadesimal)

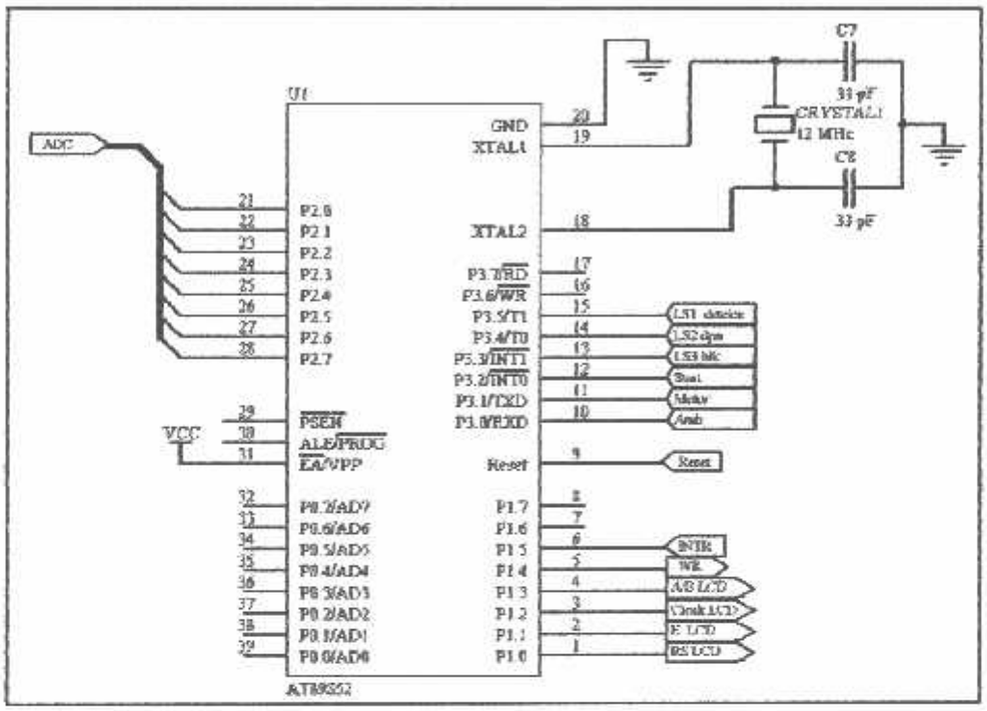
3.2.4. Rangkaian mikrokontroler AT89S52

Mikrokontroler berfungsi sebagai pusat pengendali dari seluruh sistem melalui software yang dimasukkan kedalamnya. Pada perancangan ini digunakan IC AT89S52 dalam bentuk single chip artinya tidak menggunakan tambahan EPROM eksternal. Alasan menggunakan mikrokontroler ini adalah mendapatkan suatu rangkaian yang praktis dimana mikrokontroler ini memiliki keunggulan antara lain :

- Kompatible dengan mikrokontroler MCS-51
- 8K byte *downloadable flash memory*
- 3 level program *memori lock*
- 256 byte RAM *internal*
- 3 buah *timer/counter* 16-bit
- *Programmable* UART (serial port)
- *Programmable watchdog timer*

- *Dual data pointer*
- Frekuensi kerja 0 sampai 33 MHz
- Teganan operasi 4,0 Volt sampai 5,5Volt

Berikut ini gambar perancangan rangkaian pengendali utama :



Gambar 3-7. Rangkaian Mikrokontroler AT89S52

Mikrokontroler AT89S52 memiliki 4 buah port, adapun port-port yang digunakan dalam perancangan ini adalah sebagai berikut :

- P1.0 - P1.3 digunakan sebagai keluaran ke LCD M1632
- P1.5 - P1.6 digunakan sebagai jalur pengontrol dari dan ke ADC0804
- Reset digunakan sebagai mereset sistem
- P2.0 - P2.7 digunakan sebagai jalur komunikasi data dari ADC0804
- P3.0 – P3.7 dihubungkan ke 8 saklar dengan konfigurasi *aktif low*
- $XTAL_1$ untuk osilator pada mikrokontroler AT89S52
- $XTAL_2$ untuk osilator pada mikrokontroler AT89S52

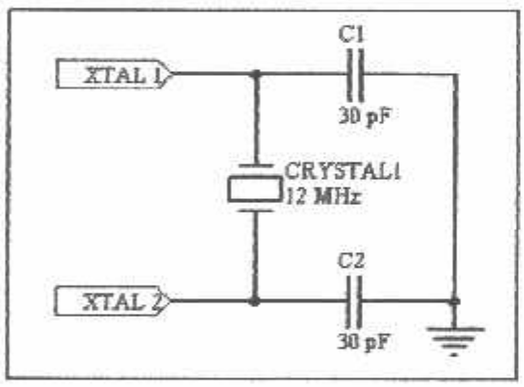
- EA/VPP dihubungkan ke VCC
- VCC dihubungkan ke VCC +5 volt
- GND dihubungkan ke Ground

Agar dalam mengakses program yang tersimpan dalam EPROM internal, maka pin 31 harus diberi logika 1 dalam hal ini dihubungkan dengan VCC 5 volt.

3.2.4.1. Rangkaian Osilator

Rangkaian osilator digunakan sebagai sumber clock dengan menggunakan 2 buah kapasitor dan sebuah kristal dengan ketentuan sebagai berikut :

- C_1 dan C_2 = 20 pF – 40 pF jika menggunakan kristal
- C_1 dan C_2 = 30 pF – 50 pF jika menggunakan menggunakan resonator keramik.

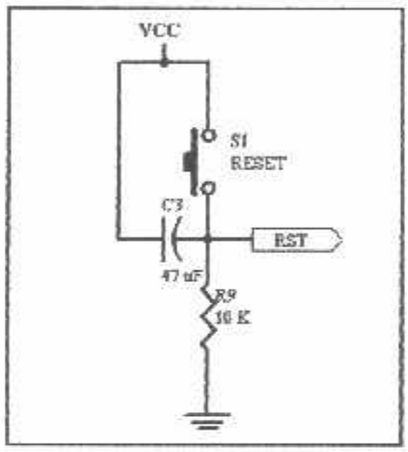


Gambar 3-8. Rangkaian Osilator

Dalam pembuatan alat ini meggunakan kristal sebagai sumber clock, dengan C1 dan C2 sebesar 33 pF. Kristal dihubungkan diantara kaki-kaki $XTAL_1$ dan $XTAL_2$ pada mikrokontroler dan kapasitornya dihubungkan ke ground. Kristal yang digunakan sebesar 12 MHz.

3.2.4.2. Rangkaian reset

Pin 9 pada mikrokontroler dihubungkan dengan saklar yang digunakan untuk mereset system mikrokontroler. Karena pin reset ini aktif berlogika tinggi maka diperlukan resistor yang bernilai 10 KΩ yang dihubungkan dengan ground untuk memastikan reset berlogika rendah saat ini bekerja. Dengan menggunakan kapasitor bernilai 47 µF.

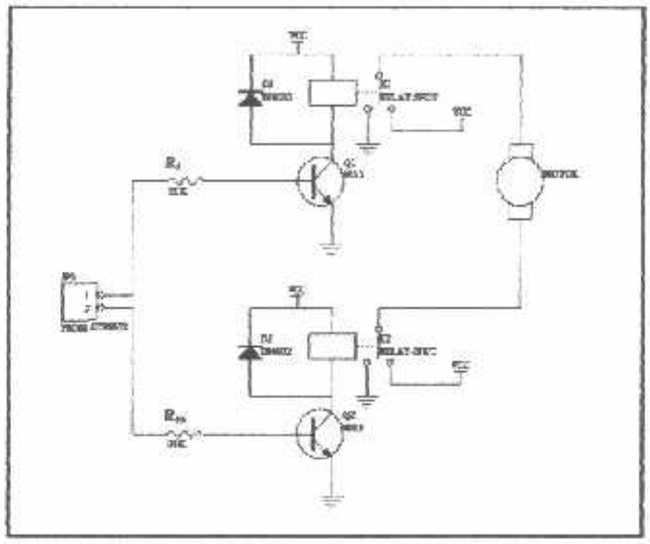


Gambar 3-9. Rangkaian Reset

3.2.5. Rangkaian penggerak motor DC

Pada perancangan ini digunakan satu buah motor DC yang digunakan untuk menarik hingga putus benang yang akan diukur. Rangkaian penggerak motor DC ini menggunakan satu buah relay dan satu buah transistor. Relay yang digunakan memiliki kontak dua jalur yaitu NO (*normaly open*) dan NC (*normaly Close*).

Kontak NC adalah awal ketika relay dalam kondisi OFF. Transistor yang digunakan 9013 yang berfungsi sebagai saklar untuk mengaktifkan relay. Pada perencanaan ini, relay yang digunakan 12 volt tegangan DC.



Gambar 3-10. Rangkaian Penggerak Motor DC

Besarnya arus Ib yang mengalir pada Q_1 sebesar :

Diketahui : $VBE_{(sat)}$ = 1,2 Volt

Vcc = 12 Volt

V_{in} = 5 Volt

Ib(sat) = 50 mA

R(relay) = 400 Ω

Maka,

$$Ic = \frac{V_{(relay)}}{R_{(relay)}}$$

$$= \frac{12V}{400}$$

$$= 30\ mA$$

Arus basis Ib pada transistor Q_1 adalah :

$$Ib = \frac{Vin - VBE_{(sat)}}{Rb}$$

$$= \frac{5-1,2}{10.10^3}$$

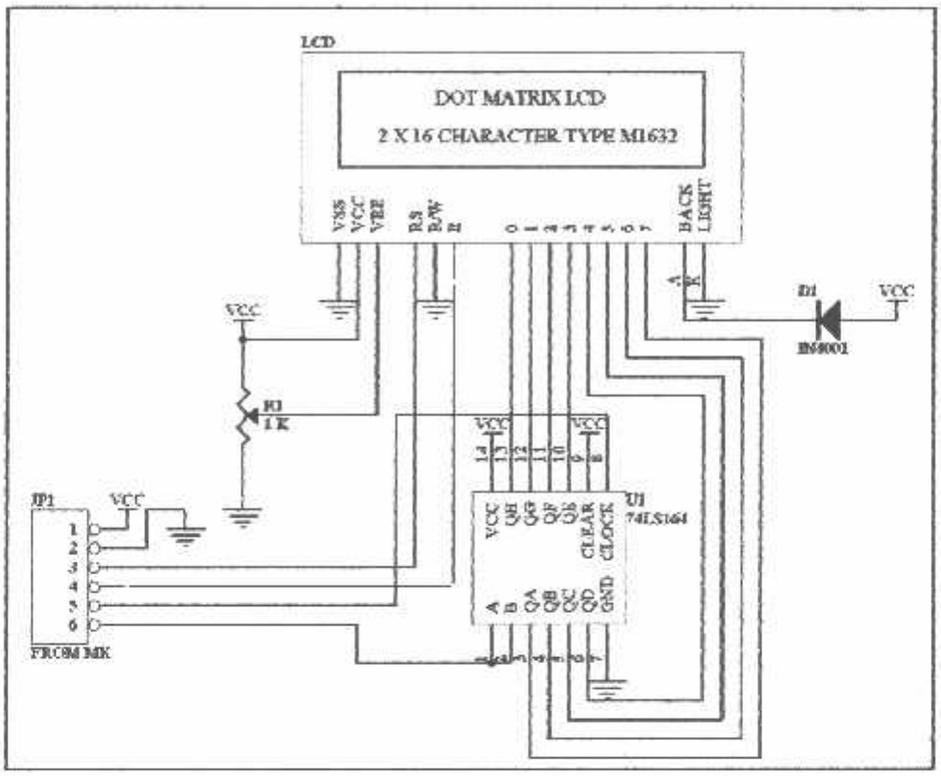
$$= \frac{3,8}{10.10^3}$$

$$= 0,38 \text{ mA}$$

Dari perhitungan diatas didapat bahwa $Ib > Ib_{(sat)}$, maka arus Ib akan membuat transistor dalam keadaan saturasi

3.2.6. Rangkaian unit tampilan (LCD)

Dalam sistem ini direncanakan menggunakan sebuah layar penampil yang berupa *Liquit Cristal Display* (LCD). Piranti yang digunakan untuk mendukung pengoperasian sistem agar dapat dioperasikan secara interaktif adalah penampil. Tipe penampil kristal cair yang digunakan adalah TM 1632 yang mempunyai 2 baris tampilan dan masing-masing terdiri atas 16 karakter tiap barisnya. Penampil kristal cair tipe TM 1632 ini dilengkapi pula dengan back light berwarna hijau. Dalam hal ini menggunakan register geser 8-bit 74LS164 yang merupakan memori sementara yang dijalankan dengan menggeser dari bit rendah ke bit tinggi atau sebaliknya.



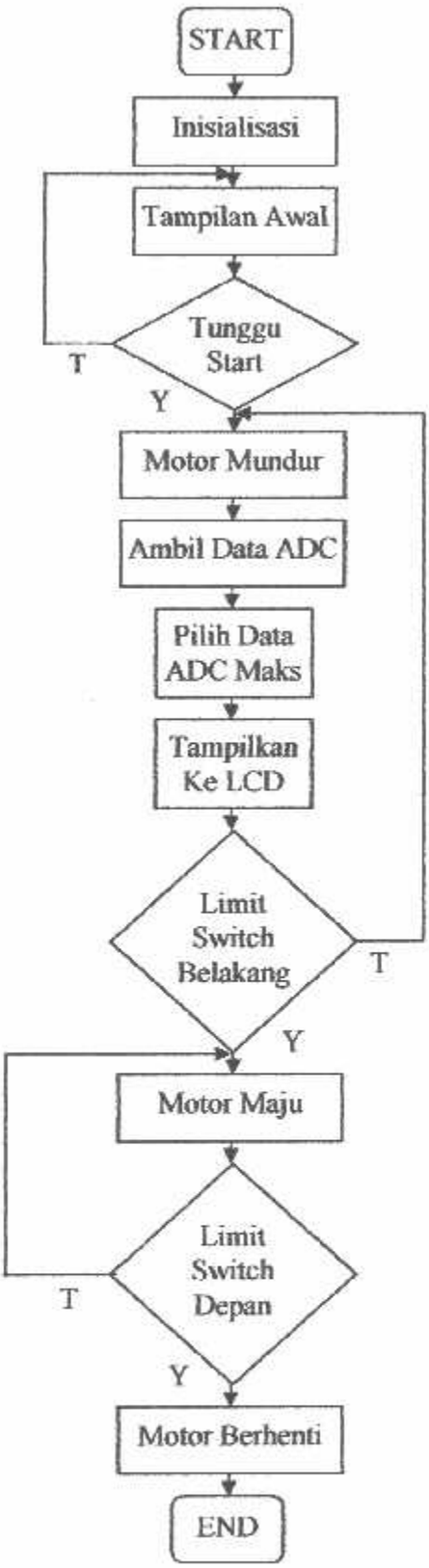
Gambar 3-11. Rangkaian Interfacing LCD

Alamat rangkaian penampil kristal cair adalah A000 h - A001 h. Penyemat Vcc dihubungkan pada potensio 1 KΩ, yang berfungsi sebagai mengatur kecerahan *back light*. R/W dihubungkan ke catu daya 5 volt sehingga mode penampil kristal cair hanya mempunyai dua mode pilihan register yaitu bila diberi logika rendah menggunakan register perintah dan bila diberi logika tinggi akan menggunakan register data.

3.3. Perancangan Software

Diagram flowchart program utama yang disusun dengan menggunakan bahasa assembler suatu program yang dapat menerjemahkan bahasa assembly ke pogram bahasa mesin yang mengandung kode-kode biner yang merupakan instruksi-instruksi yang mudah dipahami oleh prosesor seperti pada gambar 3-12 dapat dijelaskan sebagai berikut :

1. Start.
2. Tampilan Awal.
3. Banang dipasang pada tempat yang telah disediakan kemudian menunggu perintah Start.
4. Memulai proses pertama motor akan berjalan mundur hingga benang putus.
5. Mengambil data dari ADC.
6. Memilih data maksimal yang dihasilkan ADC.
7. Kemudian Menampilkan pada LCD.
8. Apabila motor menyentuh limit switch belakang maka motor akan kembali maju ke tempat semula hingga menyentuh limit switch depan hingga berhenti.
9. Selasai



Gambar 3-12. Diagram flowchart

BAB IV

PENGUKURAN DAN PENGUJIAN ALAT

Untuk mendapatkan hasil yang maksimum setelah perencanaan dan pembuatan alat ini, maka langkah berikutnya yaitu suatu pengujian. Hal ini bertujuan untuk mengetahui apakah alat yang telah dibuat tersebut sudah dapat bekerja sesuai dengan yang diharapkan dan sesuai dengan teorinya dan mempunyai nilai selisih kesalahan yang sangat kecil. Pengujian dilakukan secara bertahap, adapun rangkaian atau alat yang diuji adalah sebagai berikut :

- Rangkaian strain gage
- Rangkaian penguat instrumentasi
- Rangkaian ADC 0804
- Rangkaian LCD M1632
- Rangkaian penggerak motor

$$\text{Selisih kesalahan (\%)} = \frac{\left| \text{(Hasil Pendulum - Hasil Strain gage)} \right|}{\text{Hasil Pendulum}} x\,100\,\%$$

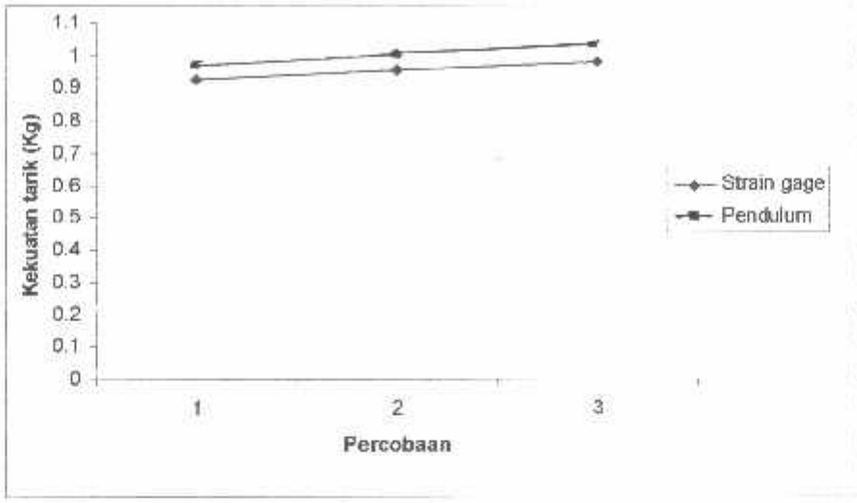
Tabel 4-1. Lincaritas kekuatan tarik benang

Percobaan	Jenis Benang	Kekuatan Benang (Kg)		Selisih kesalahan (%)
		Strain Gage	Pendulum	
1	Benang Obras (Rayon)	0.96	0.92	4.10
2	Benang Jahit (polyester)	1	0.95	4.82
3	Benang Sulam	1.02	0.98	5.52

$$\text{Selisih kesalahan rata-rata} = \frac{\sum \text{Selisih kesalahan}}{3}\ \%$$

$$= \frac{14.44}{3} \%$$

$$= 4.81\%$$



Grafik 4-1. Linearitas kekuatan tarik benang

4.1. Pengujian strain gage

4.1.1. Tujuan

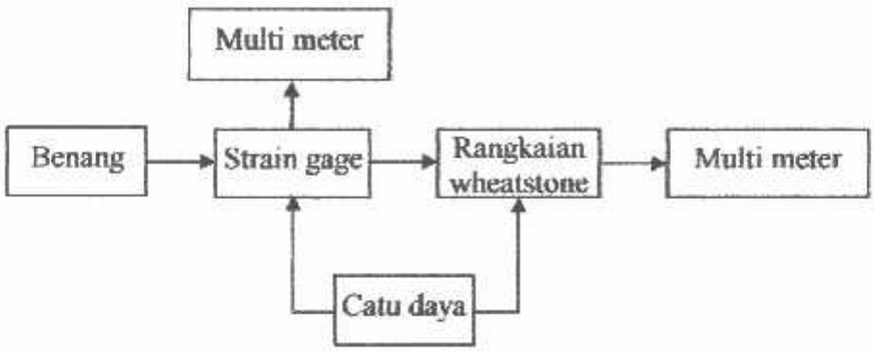
Adapun tujuan dari pengujian rangkaian strain gege adalah dengan cara membandingkan setiap perhitungan perubahan dari gaya yang diberikan pada strain gage yang dihubungkan dengan menggunakan rangkaian jembatan wheatstone dengan pengukuran yang dilakukan dari perubahan gaya yang dihasilkan.

4.1.2. Alat-alat yang digunakan

- Strain gage
- Rangkaian jembatan wheatstone
- Multimeter digital
- Catu daya

4.1.3. Prosedur pengujian

1. Memasang urutan peralatan seperti pada diagram blok dibawah ini :



Gambar 4-1. Diagram blok pengukuran strain gage

2. Melakukan pengukuran pada keluaran strain gage untuk mendapatkan nilai G_1 tanpa menggunakan beban.
3. Menarik benang dengan menggunakan motor DC hingga putus.
4. Melakukan pengukuran pada keluaran strain gage untuk mendapatkan nilai G_1 dengan menggunakan beban.
5. Melakukan perhitungan nilai ΔR.

4.1.4. Hasil pengujian

Dari hasil pengujian maka didapatkan data sebagai seperti yang terlihat pada tabel berikut ini :

ΔR = G_1 dengan beban – G_1 tanpa beban

$$V_{out1} = \left[\frac{G_1.R_2 - G_2.R_2}{(G_1 + R_1)(G_2.R_2)} \right]$$

Tabel 4-2. Pengukuran strain gage

Percobaan	G_1 tanpa beban (Ω)	G_1 dengan beban (Ω)	ΔR (Ω)
1	120	120.49	0.49
2	120	120.66	0.66
3	120	120.49	0.49
4	120	120.44	0.44
5	120	120.44	0.44
6	120	120.49	0.49
7	120	120.41	0.41
8	120	120.49	0.49
9	120	120.66	0.66
10	120	120.66	0.66
11	120	120.61	0.61
12	120	120.66	0.66
13	120	120.59	0.59
14	120	120.44	0.44
15	120	120.49	0.49
16	120	120.52	0.52
17	120	120.41	0.41
18	120	120.47	0.47
19	120	120.66	0.66
20	120	120.54	0.54
21	120	120.59	0.59
22	120	120.56	0.56
23	120	120.54	0.54
24	120	120.46	0.46
25	120	120.49	0.49

Tabel 4-3. Pengukuran nilai selisih kesalahan pada strain gage

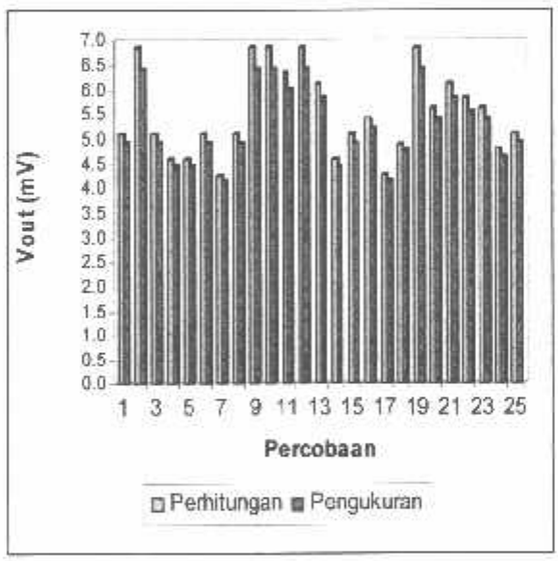
Percobaan	Output Strain Gage (mV)		Selisih kesalahan (%)
	Perhitungan	Pengukuran	
1	5.09	4.92	3.41
2	6.86	6.42	6.30
3	5.09	4.92	3.41
4	4.57	4.44	3.06
5	4.57	4.44	3.06
6	5.09	4.92	3.41
7	4.26	4.15	2.66
8	5.09	4.92	3.41
9	6.86	6.42	6.30
10	6.86	6.42	6.30
11	6.34	6.00	5.30

12	6.86	6.42	6.30
13	6.13	5.83	4.99
14	4.57	4.44	3.06
15	5.09	4.92	3.41
16	5.40	5.22	3.38
17	4.26	4.15	2.66
18	4.89	4.76	2.69
19	6.86	6.42	6.30
20	5.61	5.40	3.87
21	6.13	5.83	4.99
22	5.82	5.53	5.06
23	5.61	5.40	3.87
24	4.78	4.62	3.40
25	5.09	4.92	3.41

$$\text{Selisih kesalahan rata-rata} = \frac{\sum \text{Selisih kesalahan}}{25} \%$$

$$= \frac{104.044}{25} \%$$

$$= 4.162 \%$$



Grafik 4-2. Pengukuran strain gage

4.1.5. Analisa

Dari data yang diperoleh tersebut dapat diketahui respon tegangan terhadap gaya, bahwa setiap kenaikkan gaya akan diikuti oleh kenaikkan

tegangan. Dan hasil pengujian ini menunjukkan bahwa alat dapat bekerja sesuai dengan yang direncanakan.

4.2. Pengujian penguat instrumentasi

4.2.1. Tujuan

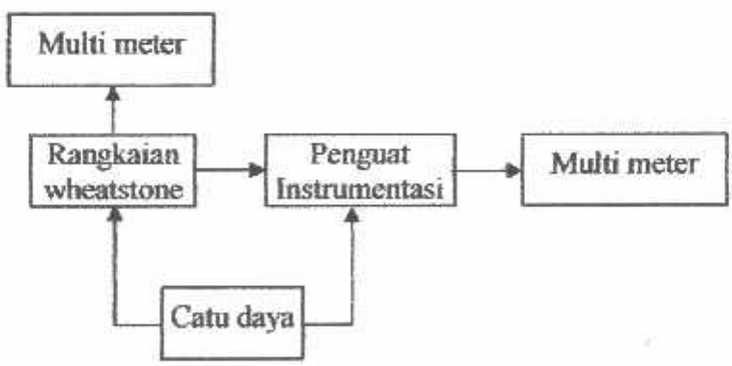
Adapun tujuan dari pengujian rangkaian penguat instrumentasi adalah memperkuat output dari rangkaian sensor gaya dengan menggunakan rangkaian jembatan wheatstone yang merupakan sinyal analog sangat kecil, sehingga Membutuhkan penguatan agar tegangan sesuai dengan tegangan referensi ADC sehingga dapat dikonversikan oleh ADC 0804 menjadi sinyal digital.

4.2.2. Alat-alat yang digunakan

- Rangkaian jembatan wheastone
- Rangkaian penguat instrumentasi
- Multimeter digital
- Catu daya

4.2.3. Prosedur pengujian

1. Memasang urutan peralatan seperti pada digram blok dibawah ini :



Gambar 4-2. Diagram blok pengukuran penguat instrumentasi

2. Menarik benang dengan menggunakan motor DC hingga putus.
3. Melakukan pengukuran pada keluaran rangkaian jembatan wheatstone.
4. Melakukan pengukuran tegangan keluaran yang melalui rangkaian penguat instrumentasi.

4.2.4. Hasil pengujian

Dari hasil pengujian maka didapatkan data sebagai seperti yang terlihat pada tabel berikut ini :

$V_{out\,2} = V_{out\,1} \times \text{Gain}$

$\text{Gain} = 687{,}76 \text{ kali}$

$$\text{Selisih kesalahan (\%)} = \frac{|\,(\text{Hasil Perhitungan} - \text{Hasil Pengukuran})\,|}{\text{Hasil Perhitungan}} \times 100\,\%$$

Tabel 4-4. Pengukuran penguat instrumentasi

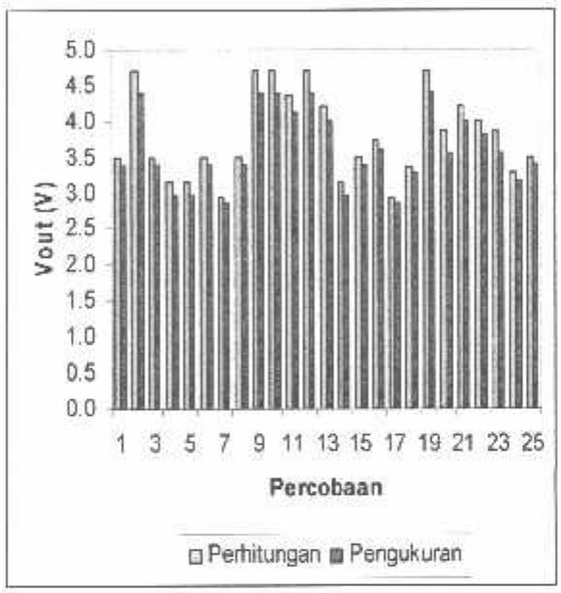
Percobaan	Output penguat instrumentasi (V)		Selisih kesalahan (%)
	Perhitungan	Pengukuran	
1	3.50	3.38	3.66
2	4.72	4.39	6.90
3	3.50	3.38	3.66
4	3.15	2.95	6.24
5	3.15	2.95	6.24
6	3.50	3.38	3.66
7	2.93	2.84	3.01
8	3.50	3.38	3.66
9	4.72	4.39	6.90
10	4.72	4.39	6.90
11	4.36	4.13	5.30
12	4.72	4.39	6.90
13	4.22	4.01	4.99
14	3.15	2.95	6.24
15	3.50	3.38	3.66
16	3.72	3.59	3.40
17	2.93	2.84	3.01
18	3.36	3.27	2.70
19	4.72	4.39	6.90
20	3.86	3.55	8.03

21	4.22	4.01	4.99
22	4.00	3.80	5.06
23	3.86	3.55	8.03
24	3.29	3.18	3.41
25	3.50	3.38	3.66

$$\text{Selisih kesalahan rata-rata} = \frac{\sum \text{Selisih kesalahan}}{25} \%$$

$$= \frac{127.140}{25} \%$$

$$= 5.086 \%$$



Grafik 4-3. Pengukuran penguat instrumentasi

4.2.5. Analisa

Dari data yang diperoleh tersebut dapat diketahui hasil dari perhitungan dan hasil dari pengukuran tidak berbeda jauh schingga dapt mengurangi keakuratan dalam melakukan suatu pengukuran. Dan hasil pengujian ini menunjukkan bahwa alat dapat bekerja sesuai dengan yang direncanakan.

Tabel 4-3. Hasil pengujian benang

Percobaan	Kekuatan Tarik Benang (Kg)
1	0,96
2	1,00
3	0,96
4	0,96
5	0,96
6	0,96
7	0,92
8	0,96
9	1,00
10	1,00
11	0,99
12	1,00
13	0,99
14	0,96
15	0,96
16	0,98
17	0,96
18	0,96
19	1,00
20	0,98
21	0,98
22	0,98
23	0,98
24	0,96
25	0,96

$$\text{Kekuatan tarik benang rata-rata} = \frac{\sum \text{Kekuatan tarik benang}}{25} \text{ Kg}$$

$$= \frac{24,32}{25} \text{ Kg}$$

$$= 0,973 \text{ Kg}$$

4.3. Pengujian ADC 0804

4.3.1. Tujuan

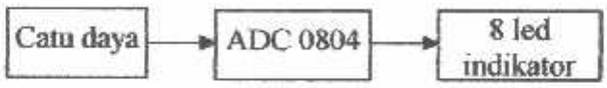
Adapun tujuan dari pengujian rangkaian ini untuk mengetahui kondisi keluaran ADC yaitu perubahan dari besaran analog menjadi besaran digital

4.3.2. Alat-alat yang digunakan

- 8 led indikator
- Rangkaian ADC 0804
- Catu daya

4.3.3. Prosedur pengujian

1. Memasang urutan peralatan seperti pada digram blok dibawah ini :



Gambar 4-3. Diagram blok pengukuran ADC 0804

2. Memberikan masukan pada ADC berupa catu daya dari 0 volt sampai 5 volt.
3. Apabila keluaran biner led ini dikonversikan sesuai dengan nilai masukan analog maka rangkaian berfungsi.

4.3.4. Hasil pengujian

Dari hasil pengujian maka didapatkan data sebagai seperti yang terlihat pada tabel berikut ini :

Tabel 4-6. Pengukuran ADC 0804

Vin (mV)	D7	D6	D5	D4	D3	D2	D1	D0
5	1	1	1	1	1	0	1	0
4,5	1	1	1	0	0	0	0	1
4	1	1	0	0	1	0	0	0
3,5	1	0	1	0	1	1	1	1
3	1	0	0	1	0	1	1	0
2,5	0	1	1	1	1	1	0	1
2	0	1	1	0	0	1	0	0
1,5	0	1	0	0	1	0	1	1
1	0	0	1	1	0	0	1	0
0,5	0	0	0	1	1	0	0	1
0	0	0	0	0	0	0	0	0

4.3.5. Analisa

Dari data yang diperoleh tersebut dapat diketahui bahwa keluaran ADC 0804 yang berupa data biner 8 bit sesuai dengan data analog masukan.

4.4. Pengujian LCD

4.4.1. Tujuan

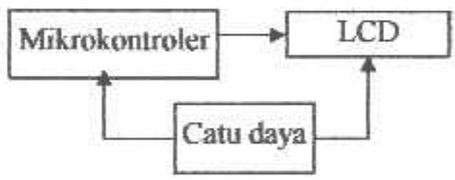
Adapun tujuan dari pengujian rangkaian ini untuk mengetahui kondisi keluaran LCD yaitu sebagai tampilan hasil pengukuran kekuatan benang.

4.4.2. Alat-alat yang digunakan

- LCD
- Rangkaian mikrokontroler AT 89S52
- Catu daya

4.4.3. Prosedur pengujian

1. Memasang urutan peralatan seperti pada digram blok dibawah ini :

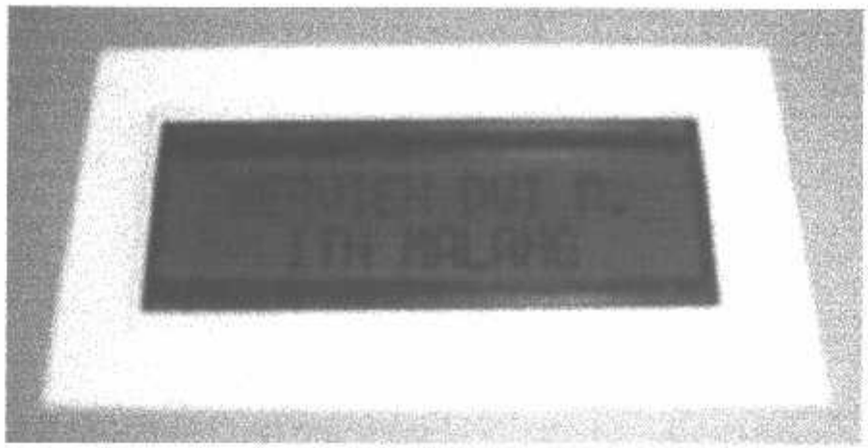


Gambar 4-4. Diagram blok pengukuran LCD

2. Memberikan masukan pada LCD berupa catu daya dari 0 volt sampai 5 volt.
3. Apabila lampu menyala dan terdapat karakter maka rangkaian berfungsi.

4.4.4. Hasil pengujian

Dari hasil pengujian maka didapatkan data sebagai seperti yang terlihat pada gambar berikut ini :



Gambar 4-5. Hasil pengujian LCD

4.5. Pengujian rangkaian penggerak motor DC

4.5.1. Tujuan

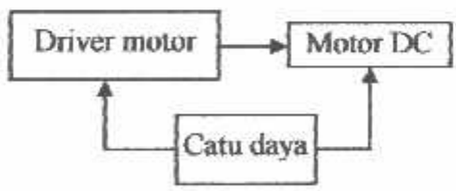
Tujuan dari pengujian rangkaian ini adalah untuk menentukan konfigurasi bit pengaturan arah putaran motor.

4.5.2. Alat – alat yang digunakan

- Motor DC
- Rangkaian driver motor
- Catu daya

4.5.3. Prosedur pengujian

1. Memasang urutan peralatan seperti pada digram blok dibawah ini :



Gambar 4-6 Diagram blok pengukuran motor DC

2. Memberikan masukan pada driver motor berupa catu daya 5 Volt.

3. Memberikan masukan pada motor DC berupa catu daya 18 Volt.

4. Apabila motor dapat berjalan maka rangkaian dapat bekerja dengan baik.

4.5.4. Hasil pengujian

Dari hasil pengujian maka didapatkan data sebagai seperti yang terlihat pada tabel berikut ini :

Tabel 4-7. pengujian motor DC

P3.1	P3.2	Kondisi motor
0	0	Diam
0	1	Diam
1	0	Mundur
1	1	Maju

4.5.5. Analisa

Dari tabel diatas dapat diketahui bahwa untuk menghasilkan gerakan atau arah putaran motor dapat dilakukan dengan memberikan masukan berupa logika 1 atau 0 pada output P3.1 dan P3.2 mikrokontroler AT 89S52.

BAB V

PENUTUP

5.1. Kesimpulan

Dari pengamatan dan analisa selama proses perencanaan hardware dan software serta pengujian alat dapat diambil kesimpulan sebagai berikut :

1. Dengan bertambahnya beban tegangan output pada rangkaian jembata wheatstone kenaikkan sebesar 0 – 7,27 mV.
2. Alat dapat bekerja secara linier dengan bertambahnya gaya yang diberikan maka kekuatan tarik per helai akan semakin besar pula.
3. Dari hasil pengukuran penguatan pada rangkaian instrumentasi didapat penguatan sebesar 687,76 kali.
4. Dari sensor gaya dapat diambil kesimpulan bahwa Selisih kesalahan rata-rata sebasar 4,162 %.
5. Dari rangkaian penguat instrumentasi dapat diambil kesimpulan bahwa Selisih kesalahan rata-rata sebasar 5,086 %.

5.2. Saran

Beberapa saran yang dapat penulis kepada pihak-pihak yang berniat mengembangkan alat ini antara lain :

1. Dalam pembuatan alat seperti ini hendaknya menggunakan komponen yang berkualitas tinggi agar mendapat hasil yang akurat dan mengurangi nilai error.
2. Sistem yang dirancang ini merupakan konsep dasar pengukuran berat dengan batas pengukuran 1,3 Kg/helai untuk pengembangan lebih lanjut diharapkan beban maksimal melebihi berat maksimal yang sudah ada.

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LAMPIRAN I
SPESIFIKASI ALAT

Gambar 4-7. Foto alat keseluruan

Spesifikasi alat

1. Alat ini menggunakan tranduser strain gage yang diaplikasikan dalam sebuah rangkaian jembatan wheatstone sebagai sensor gaya.
2. Menggunakan mikrokontroler AT89S52 sebagai pengendali utama rangkaian secara otomatis sehingga dapat bekerja dengan baik sesuai dengan yang direncanakan.
3. Menggunakan motor DC sebagai penarik benang hingga putus.
4. Menggunakan LCD dengan jumlah karakter 16 X 2 untuk unit tampilan dari hasil pengukuran.

LAMPIRAN 2
DATA HASIL PENGUJIAN LINIERITAS

Jenis benang : Benang Obras (Rayon)

Percobaan	Kekuatan Tarik (Kg)	
	Strain Gage	Pendulum
1	0.98	0.92
2	0.98	0.9
3	0.96	0.96
4	0.98	0.96
5	0.94	0.9
6	0.98	0.94
7	0.96	0.92
8	0.96	0.94
9	0.96	0.92
10	0.94	0.9
Rata-Rata	**0.964**	**0.926**

Jenis benang : Benang Jahit (Polyster)

Percobaan	Kekuatan Tarik (Kg)	
	Strain Gage	Pendulum
1	0.96	0.94
2	0.94	0.9
3	0.98	0.94
4	0.98	0.96
5	1	0.98
6	0.98	0.94
7	0.98	0.96
8	1	0.94
9	1.2	1
10	0.98	0.98
Rata-Rata	1	**0.954**

Jenis benang : Benang Sulam

Percobaan	Kekuatan Tarik (Kg)	
	Strain Gage	Pendulum
1	1	0.98
2	1.2	1
3	0.98	0.98

4	1	0.94
5	0.98	0.96
6	0.98	0.98
7	1	1
8	0.98	0.96
9	1	0.98
10	1.2	1
Rata-Rata	**1.032**	**0.978**

LAMPIRAN 3
LISTING PROGRAM

```
0001    dispelear   equ   00000001b
0038    funeset     equ   00111000b
0006    entrmod     equ   00000110b
000C    dispon      equ   00001100b
000E    cusor       equ   00001110b
000D    blink       equ   00001101b

0090    RS          equ   p1.0
0091    E           equ   p1.1
0092    con_lcd     equ   p1.2
0093    data_lcd    equ   p1.3
0094    eoc         equ   p1.4
0095    wr_adc      equ   p1.5

00B0    arah        equ   p3.0
00B1    motor       equ   p3.1      ; high
00B2    saklar      equ   p3.2      ; low
00B3    lstarik     equ   p3.3      ; low
00B4    lsdorong    equ   p3.4      ; low
00B5    lsawal      equ   p3.5      ; low

0030    buffer      equ   30h
0031    buffer1     equ   31h
0032    simpan1     equ   32h
0033    simpan2     equ   33h

0000    org   0h
```

;---

; **Program utama**

;---

```
0000            mulai:
0000 D2B2           setb saklar
0002 D2B3           setb lstarik
0004 D2B4           setb lsdorong
0006 C2B1           clr motor
0008 120153         lcall initlcd
000B 7D01           movR5,#1
000D 9001C4         mov dptr,#har1
0010 1200F6         lcall cetak1
```

```
0013 7D01          mov R5,#1
0015 9001D6        mov dptr,#har2
0018 1200F1        lcall cetak2
001B 753300        mov simpan2,#0
001E 20B2FD        awal:  jb saklar,$
024 853330         mov buffer,simpan2
0027 120074        lcall tampil
002A C2B0          clr arah
002C 120173        lcall dly100ms
002F D2B1          setb motor

0031          ambil:
0031 30B329        jnb lstarik,ambil1
0034 30B5FA        jnb lsawal,ambil
0037 1200B5        lcall ambiladc
003A 941E          subb a,#30
003C 4016          jc ambil0
003E 75F005        mov b,#5
0041 A4            mul ab
0042 E532          mov a,simpan1
0044 9533          subb a,simpan2
0046 400C          jc ambil0
0048 853230        mov buffer,simpan1
004B 853233        mov simpan2,simpan1
004E 120074        lcall tampil
0051 020031        jmp ambil

0054          ambil0:
0054 853330        mov buffer,simpan2
0057 120074        lcall tampil
005A 020031        jmp ambil

005D          ambil1:
005D 753300        mov simpan2,#0
0060 C2B1          clr motor
0062 120173        lcall dly100ms
0065 D2B0          setb arah
0067 120173        lcall dly100ms
006A D2B1          setb motor
006C 20B4FD        jb lsdorong,$
006F C2B1          clr motor
0071 02001E        jmp awal
```

```
;-------------------------------------------------------------------------
;                              sub program
;-------------------------------------------------------------------------

0074 7D01          tampil: mov r5,#1
0076 9001A8        mov dptr,#h1
0079 1200F6        lcall cetak1
007C 9001BA        mov dptr,#h2
007F 1200F1        lcall cetak2
0082 E530          mov a,buffer
0084 75F064        mov b,#100
0087 84            div ab
0088 85F031        mov buffer1,b
008B 4430          orl a,#30h
008D 12010D        lcall dataout
0090 742C          mov a,#','
0092 12010D        lcall dataout
0095 E531          mov a,buffer1
0097 75F00A        mov b,#10
009A 84            div ab
009B 85F031        mov buffer1,b
009E 4430          orl a,#30h
00A0 12010D        lcall dataout
00A3 E531          mov a,buffer1
00A5 4430          orl a,#30h
00A7 12010D        lcall dataout
00AA 744B          mov a,#'K'
00AC 12010D        lcall dataout
00AF 7467          mov a,#'g'
00B1 12010D        lcall dataout
00B4 22            ret

00B5           ambiladc:
00B5 D295          setb wr_adc
00B7 00            nop
00B8 00            nop
00B9 00            nop
00BA 00            nop
00BB 00            nop
00BC C295          clr wr_adc
00BE 00            nop
00BF 00            nop
00C0 00            nop
00C1 00            nop
00C2 00            nop
```

```
00C3 00          nop
00C4 D295        setb wr_adc
00C6          waiteoc1:
00C6 3094FD      jnb eoc,waiteoc1
00C9 D294        setb eoc
00CB E5A0        mov a,p2
00CD F532        mov simpan1,a
00CF 22          ret

00D0 120153   hapus: lcall  initLCD
00D3 7D01        mov r5,#1
00D5 900184      mov dptr,#hapus1
00D8 1200F6      lcall cetak1
00DB 7D01        mov r5,#1
00DD 900196      mov dptr,#hapus2
00E0 1200F1      lcall cetak2
00E3 22          ret

;-------------------------------------------------------------------------
;                              Routine LCD
;-------------------------------------------------------------------------

00E4          baris2:
00E4 ED          mov a,r5
00E5 24C0        add a,#0c0h ;11000000b
00E7 8003        sjmp posisisub

00E9          baris1:
00E9 ED          mov a,r5
00EA 2480        add a,#80h; 10000000b

00EC          posisisub:
00EC 14          dec  a
00ED 120105      lcall controlout
00F0 22          ret

00F1          cetak2:
00F1 1200E4      lcall baris2
00F4 8003        sjmp life

00F6          cetak1:
00F6 1200E9      lcall baris1

00F9          life:
00F9 8004        sjmp outstring
```

```
00FB            loop:
00FB 12010D         lcall dataout
00FE A3             inc dptr

00FF            outstring:
00FF E4             clr a
0100 93             movc a,@a+dptr
0101 B424F7         cjne a,#'$',loop
0104 22             ret

0105            controlout:
0105 C083           push dph
0107 C082           push dpl
0109 C290           clr rs
010B 8006           sjmp out

010D            dataout:
010D C083           push dph
010F C082           push dpl
0111 D290           setb rs

0113            out:
0113 D291           setb e
0115 120123         lcall geser
0118 7EFA           mov r6,#250
011A DEFE           djnz r6,$
011C D082           pop dpl
011E D083           pop dph
0120 C291           clr e
0122 22             ret

0123            geser:
0123 C292           clr con_lcd
0125 75F008         mov   b,#8

0128            a1:
0128 13             rrc a
0129 9293           mov data_lcd,c
012B 00             nop
012C 00             nop
012D 00             nop
012E 00             nop
012F D292           setb con_lcd
0131 00             nop
0132 00             nop
```

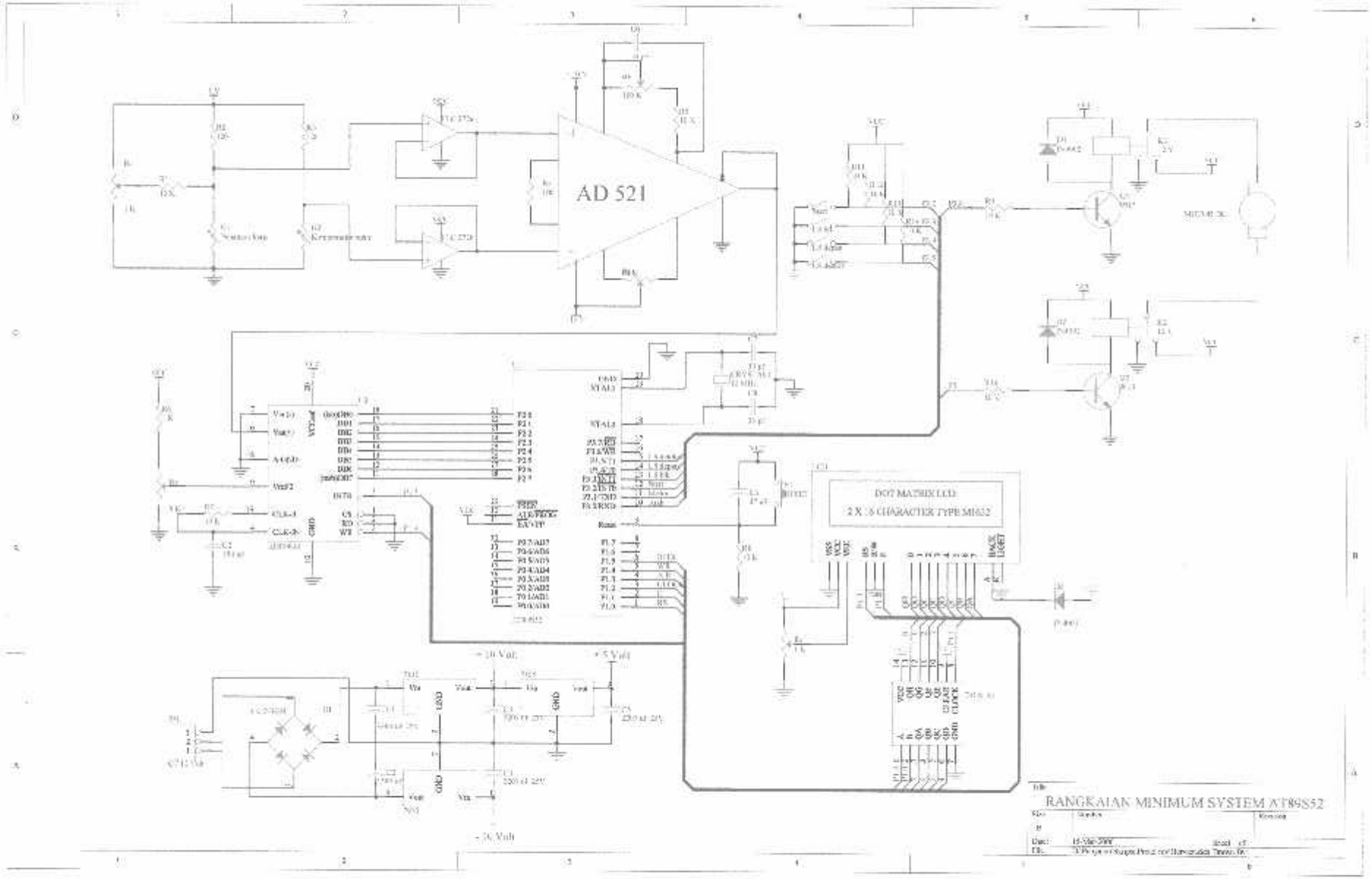
```
0133 00          nop
0134 00          nop
0135 C292        clr con_lcd
0137 D5F0EE      djnz b,a1
013A 22          ret

013B             dele:
013B 7E00            mov r6,#00h

013D             dlylcdlp:
013D 7F00            mov r7,#00h
013F DFFE            djnz r7,$
0141 DEFA            djnz r6,dlylcdlp
0143 22              ret

0144             ldelay:
0144             ldelay2:
0144 7B00            mov r3,#00h

0146             ldelay1:
0149 DBFB            djnz r3,ldelay1
014B DAF7            djnz r2, ldelay2
014D 22              ret

014E             tdelay:
014E 7F00            mov r7,#00h
0150 DFFE            djnz r7,$
0152 22              ret

0153             initlcd:
0153 7401            mov  a,#dispclear
0155 120105          lcall controlout
0158 12013B          lcall dele
015B 7438            mov a,#funcset
015D 120105          lcall controlout
0160 740C            mov a,#dispon
0162 120105          lcall controlout
0165 7406            mov a,#entrmod
0167 120105          lcall controlout
016A 22              ret
```

;---

; **Rutin delay**

;---

```
016B            dly1000mS:
016B 7A0A           mov    r2,#10

016D            UlDel:
016D 120173         lcall  dly100mS
0170 DAFB           djnz   r2,UlDel
0172 22             ret

0173            dly100mS:
0173 7EC8           mov r6,#200
0175 02017D         ljmp   waktu

0178            dly10mS:
0178 7E14           mov  r6,#20
017A 02017D         ljmp    waktu

017D            waktu:
017D 7FF7           mov    r7,#247
017F DFFE           djnz   r7,$
0181 DEFA           djnz   r6,Waktu
0183 22             ret
;=============================================================

0184            hapus1:
0184 20202020       db '            $'
0188 20202020
018C 20202020
0190 20202020
0194 2024

0196            hapus2:
0196 20202020       db '            $'
019A 20202020
019E 20202020
01A2 20202020
01A6 2024

01A8            h1:
01A8 4E696C61       db 'Nilai satuannya  $'
01AC 69207361
01B0 7475616E
01B4 6E796120
01B8 2024
```


AD 521
DOT MATRIX LCD
2 X 16 CHARACTER TYPE M1632
RANGKAIAN MINIMUM SYSTEM AT89S52

PT. (PERSERO) INDUSTRI SANDANG NUSANTARA
UNIT LAWANG
Alamat : Jl. Indrokilo No. 1 Telp. (0341) 426165, 426254 Fax (0341) 426220 Telex 31073 Lawang 65215 - Malang
Kantor Pusat : Jl. Wolter Monginsidi No. 88K Kebayoran Baru Telp. (021) 7252623, 7252624 Fax. (021) 7221553 Jakarta 12170 - Indonesia

SURAT KETERANGAN

Nomor : 029 / 7 – II / 2006

Sesuai surat ijin Praktek Kerja Lapangan dari PT. Industri Sandang Nusantara (Persero) Unit Patal Lawang No. : 027 / 7 – G / 2006 tanggal 14 Maret 2006 perihal Survey (Penelitian), maka dengan ini menerangkan bahwa :

N A M A	: HERVIN DWI ANINDITA
NIM	: 01.17.077
PERGURUAN TINGGI	: ITN MALANG.
PROGRAM STUDY	: TEKNIK ELEKTRO.
JENJANG PENDIDIKAN	: S – 1

Telah melaksanakan Survey (Peneletihan) selama 2 (dua) hari mulai tanggal 20 & 21 Maret 2006.

Demikian Surat Keterangan ini dibuat untuk dapat dipergunakan sebagaimana mestinya

Lawang, 21 Maret 2006
General Manager,
Ub.

PT. INDUSTRI SANDANG NUSANTARA (PERSERO) PATAL LAWANG

ARY SUPRIYATNO
Manager Keuangan & Umum.

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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO

Formulir Perbaikan Ujian Skripsi

Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA : Hervian Dwi Ananda
N I M : 0917077
Perbaikan meliputi :

1) Bukti pengujian di Lab Tesnik dilampirkan

Malang,

(_____)

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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO
JL.Raya Karanglo Km 2
MALANG

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Dalam pelaksanaan Ujian Skripsi Jenjang Strata 1 Jurusan Teknik Elektro Konsentrasi Teknik Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

Nama	: HERVIEN DWI ANINDITA
Nim	: 01.17.077
Masa Bimbingan	: 10-september-2005 s/d 13-maret-2006
Judul Skripsi	: PERANCANGAN DAN PEMBUATAN ALAT PENGUKUR KEKUATAN BENANG DIGITAL DENGAN TAMPILAN PADA LCD BERBASIS MIKROKONTROLER AT89S52

No	Tanggal	Uraian	Paraf
1	18-03-2006	Bukti pengujian di laboratorium tekstil	

Mengetahui

Dosen Pembimbing I

(Ir. Usman Djuanda, MM)
NIP.P 07 061 05 01350

Dosen Pembimbing II

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Dosen Penguji I

(Ir. F. Yudi Limpraptono, MT)
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INSTITUT TEKNOLOGI NASIONAL
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JURUSAN TEKNIK ELEKTRO

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Dalam pelaksanaan Ujian Skripsi Janjang Strata 1 Jurusan Teknik Elektro Konsentasi T. Energi Listrik / T. Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

NAMA :
N I M :
Perbaikan meliputi :

- Data pengujian u/ berbagai jenis benang !!!
- Algoritma Mulai Data Kekuatan benang ke ATK !
- Kesimpulan

Malang,

(M. ASHAR)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO
JL.Raya Karanglo Km 2
MALANG

FORMULIR PERBAIKAN UJIAN SKRIPSI

Dalam pelaksanaan Ujian Skripsi Jenjang Strata 1 Jurusan Teknik Elektro Konsentrasi Teknik Elektronika, maka perlu adanya perbaikan skripsi untuk mahasiswa :

Nama	: HERVIEN DWI ANINDITA
Nim	: 01.17.077
Masa Bimbingan	: 10-september-2005 s/d 13-maret-2006
Judul Skripsi	: PERANCANGAN DAN PEMBUATAN ALAT PENGUKUR KEKUATAN BENANG DIGITAL DENGAN TAMPILAN PADA LCD BERBASIS MIKROKONTROLER AT89S52

No	Tanggal	Uraian	Paraf
1	18-03-2006	• Data pengujian untuk berbagai jenis benang • Algoritma maks data kekuatan benang ke ADC • Kesimpulan	

Mengetahui

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(M. Ashar, ST, MT)

INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO
JL.Raya Karanglo Km 2
MALANG

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Nim	: 01.17.077
Jurusan	: Teknik Elektro
Kosentrasi	: Teknik Elektronika S-1
Masa Bimbingan	: 10-september-2005 s/d 13-maret-2006
Judul Skripsi	: PERANCANGAN DAN PEMBUATAN ALAT PENGUKUR KEKUATAN BENANG DIGITAL DENGAN TAMPILAN PADA LCD BERBASIS MIKROKONTROLER AT89S52
Pembimbing	: 1. Ir. Usman Djuanda, MM 2. M. Ibrahim Ashari, ST
Telah Dievaluasi	: 95/95

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MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Hervien Dwi Anindita
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Judul Skripsi : Pembuatan dan perancangan alat pengukur kekuatan benang digital dengan tampilan pada LCD berbasis Mikrokonteroller AT89S52

NO	Tanggal	Uraian	Paraf Pembimbing
1.	10 okt '05	Acc Bab I	
2.	12 okt '05	Acc Bab II	
3	16 okt '05	Revisi Bab III	
4.	17 okt '05	Acc Bab III	
5.	6 jan '06	Acc Bab IV	
6.	10 feb '06	Acc Bab V	
7.	10 feb '06	Makalah Seminar	
8.			
9.			
10.			

Malang, 28 - 3 - 2006
Dosen Pembimbing

Ir. Usman Djuanda, MM

Form. S-4a

INSTITUT TEKNOLOGI NASIONAL
JL. BENDUNGAN SIGURA-GURA 2
MALANG

FORMULIR BIMBINGAN SKRIPSI

Nama : Hervien Dwi Anindita
Nim : 0117077
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Judul Skripsi : Pembuatan dan perancangan alat pengukur kekuatan benang digital dengan tampilan pada LCD berbasis Mikrokonteroller AT89S52

NO	Tanggal	Uraian	Paraf Pembimbing
1.	10 Okt 05	acc bab I	
2.	11 Okt '05	acc bab II	
3.	13 Okt '05	acc bab III	
4.	2 Jan '06	acc bab IV	
5.	10 Feb '06	acc bab V	
6.	10 Feb '06.	makalah Seminar	
7.			
8.			
9.			
10.			

Malang, 10 Feb 2006
Dosen Pembimbing

M. Ibrahim Ashari, ST

Form. S-4a


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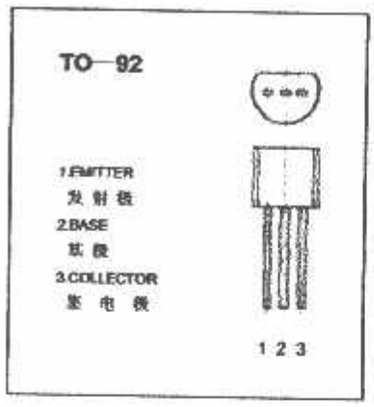
ITN
MALANG

9013

NPN SILICON TRANSISTOR



FEATURES
特　　征

Power dissipation　（最大耗散功率）

P_{CM} : 0.625 W (Tamb=25℃)

Collector current　（最大集电极电流）

I_{CM} : 0.5 A

Collector-base voltage　（集电极—基极击穿电压）

$V_{(BR)CBO}$: 45 V

ELECTRICAL CHARACTERISTICS (Tamb=25℃ unless otherwise specified)
电　　特　　性　　（环境温度　　除　非　另　有　规　定）

Parameter 参　数	Symbol 符　号	Test conditions 测　试　条　件	MIN 最小值	TYP 典型值	MAX 最大值	UNIT 单位
Collector-base breakdown voltage 集电极--基极击穿电压	$V(BR)_{CBO}$	Ic= 100 μ A, I_E=0	45			V
Collector-emitter breakdown voltage 集电极--发射极击穿电压	$V(BR)_{CEO}$	Ic= 0.1 mA, I_B=0	25			V
Emitter-base breakdown voltage 发射极--基极击穿电压	$V(BR)_{EBO}$	I_E= 100 μ A, I_C=0	5			V
Collector cut-off current 集电极--基极截止电流	I_{CBO}	V_{CB}= 40 V I_E=0			0.1	μ A
Collector cut-off current 集电极--发射极截止电流	I_{CEO}	V_{CE}= 20 V I_B=0			0.1	μ A
Emitter cut-off current 发射极--基极截止电流	I_{EBO}	V_{EB}= 5 V, I_C=0			0.1	μ A
DC current gain(note) 直流电流增益	$H_{FE(1)}$	V_{CE}= 1 V, I_C= 50 mA	64		300	
	$H_{FE(2)}$	V_{CE}= 1V, I_C =500 mA	40			
Collector-emitter saturation voltage 集电极--发射极饱和压降	V_{CE}(sat)	I_C= 500 mA, I_B=50 mA			0.6	V
Base-emitter saturation voltage 基极--发射极饱和压降	V_{BE}(sat)	I_C= 500mA, I_B= 50 mA			1.2	V
Base-emitter voltage 基极--发射极正向电压	V_{BE}	I_E=100mA			1.4	V
Transition frequency 特　征　频　率	f_T	V_{CE}= 6 V, I_C= 20 mA f =30MHz	160			MHz

CLASSIFICATION OF $H_{FE(1)}$　（分类）

Rank 档次	D	E	F	G	H	I
Range 范围	64-91	78-112	96-135	112-166	144-220	190-300

Wing Shing Computer Components Co., (H.K.)Ltd.
Homepage: http://www.wingshing.com
Tel:(852)2341 9276 Fax:(852)2797 8153
E-mail: wsccltd@hkstar.com

ANALOG DEVICES

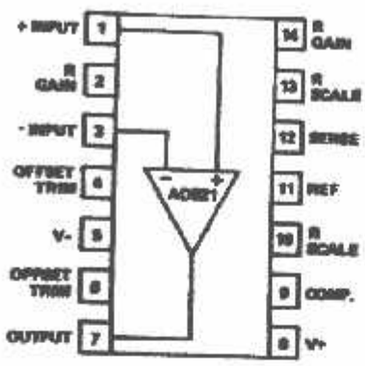
Integrated Circuit Precision Instrumentation Amplifier

AD521

FEATURES

- Programmable Gains from 0.1 to 1000
- Differential Inputs
- High CMRR: 110dB min
- Low Drift: 2μV/°C max (L)
- Complete Input Protection, Power ON and Power OFF
- Functionally Complete with the Addition of Two Resistors
- Internally Compensated
- Gain Bandwidth Product: 40MHz
- Output Current Limited: 25mA
- Very Low Noise: 0.5μV p-p, 0.1Hz to 10Hz, RTI @ G = 1000
- Chips are Available

PIN CONFIGURATION



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PRODUCT DESCRIPTION

The AD521 is a second generation, low cost, monolithic IC instrumentation amplifier developed by Analog Devices. As a true instrumentation amplifier, the AD521 is a gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521 IC instrumentation amplifier should not be confused with an operational amplifier, although several manufacturers (including Analog Devices) offer op amps which can be used as building blocks in variable gain instrumentation amplifier circuits. Op amps are general-purpose components which, when used with precision-matched external resistors, can perform the instrumentation amplifier function.

An instrumentation amplifier is a precision differential voltage gain device optimized for operation in a real world environment, and is intended to be used wherever acquisition of a useful signal is difficult. It is characterized by high input impedance, balanced differential inputs, low bias currents and high CMR.

As a complete instrumentation amplifier, the AD521 requires only two resistors to set its gain to any value between 0.1 and 1000. The ratio matching of these resistors does not affect the high CMRR (up to 120dB) or the high input impedance ($3 \times 10^9\ \Omega$) of the AD521. Furthermore, unlike most operational amplifier-based instrumentation amplifiers, the inputs are protected against overvoltages up to ±15 volts beyond the supplies.

The AD521 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "J" grade, the low drift "K" grade, and the lower drift, higher linearity "L" grade are specified from 0 to +70°C. The "S" grade guarantees performance to specification over the extended temperature range: -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 has low guaranteed input offset voltage drift (2μV/°C for L grade) and low noise for precision, high gain applications.
3. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
4. The AD521 is fully protected for input levels up to 15V beyond the supply voltages and 30V differential at the inputs.
5. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
6. Offset nulling can be achieved with an optional trim pot.
7. The AD521 offers superior dynamic performance with a gain-bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5μs to 0.1% of a 10V step.

AD521 —SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

MODEL	AD521JD	AD521KD	AD521LD	AD521SD (ABSOLUTE MAXIMUM)
GAIN				
Range (Per Specified Operation, Note 1)	1 to 1000	"	"	"
Equation	$G = R_S/R_G$ V/V	"	"	"
Error from Equation	(±0.25—0.004G)%	"	"	"
Nonlinearity (Note 2)				
1≤G≤1000	0.2% max	"	0.1% max	"
Gain Temperature Coefficient	±(3 +0.05G)ppm/°C	"	"	0.15 +0.4G)ppm/°C
OUTPUT CHARACTERISTICS				
Rated Output	±10V, ±10mA min	"	"	"
Output at Maximum Operating Temperature	±10V @ 5mA min	"	"	"
Impedance	0.1Ω	"	"	"
DYNAMIC RESPONSE				
Small Signal Bandwidth (±3dB)				
G = 1	>25MHz	"	"	"
G = 10	800kHz	"	"	"
G = 100	200kHz	"	"	"
G = 1000	40kHz	"	"	"
Small Signal, ±1.0% Flatness				
G = 1	75kHz	"	"	"
G = 10	20kHz	"	"	"
G = 100	2kHz	"	"	"
G = 1000	4kHz	"	"	"
Full Peak Response (Note 3)	100kHz	"	"	"
Slew Rate, 1≤G≤1000	10V/μs	"	"	"
Settling Time (any 20V step to within 10mV of Final Value)				
G = 1	7μs	"	"	"
G = 10	5μs	"	"	"
G = 100	10μs	"	"	"
G = 1000	15μs	"	"	"
Differential Overload Recovery (±10V input to within 10mV of Final Value) (Note 4)				
G = 1000	50μs	"	"	"
Common Mode Step Recovery (10V Input to within 10mV of Final Value) (Note 5)				
G = 1000	10μs	"	"	"
VOLTAGE OFFSET (may be nulled)				
Input Offset Voltage (V_{OS_I})	3mV max (2mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.5mV typ)	**
vs. Temperature	15μV/°C max (7μV/°C typ)	5μV/°C max (1.5μV/°C typ)	3μV/°C max	**
vs. Supply	3μV/%	"	"	"
Output Offset Voltage (V_{OS_O})	400mV max (200mV typ)	200mV max (30mV typ)	100mV max	**
vs. Temperature	400μV/°C max (250μV/°C typ)	150μV/°C max (50μV/°C typ)	75μV/°C max	**
vs. Supply (Note 6)	$0.005V_{OS_O}$/%	"	"	"
INPUT CURRENTS				
Input Bias Current (either input)	60nA max	40nA max	**	**
vs. Temperature	1nA/°C max	500pA/°C max	**	**
vs. Supply	2%/V	"	"	"
Input Offset Current	20nA max	10nA max	**	**
vs. Temperature	250pA/°C max	125pA/°C max	**	**
INPUT				
Differential Input Impedance (Note 7)	3×10^8 Ω‖3.0pF	"	"	"
Common Mode Input Impedance (Note 8)	6×10^{10} Ω‖3.0pF	"	"	"
Input Voltage Range for Specified Performance (with respect to ground)	±10V	"	"	"
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	"	"	"
Voltage at either input (Note 9)	V_S ±15V	"	"	"
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance				
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	**	**
G = 10	90dB min (94dB typ)	94dB min (100dB typ)	**	**
G = 100	100dB min (104dB typ)	104dB min (114dB typ)	**	**
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	**	**
NOISE				
Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10)	$\sqrt{(0.5G)^2 + (12)^2}$ μV	"	"	"
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (80)^2}$ μV	"	"	"
Input Current, rms, 10Hz to 10kHz	15pA (rms)	"	"	"
REFERENCE TERMINAL				
Bias Current	5μA	"	"	"
Input Resistance	100kΩ	"	"	"
Voltage Range	±10V	"	"	"
Gain to Output	1	"	"	"
POWER SUPPLY				
Operating Voltage Range	±5V to ±18V	"	"	"
Quiescent Supply Current	5mA max	"	"	"
TEMPERATURE RANGE				
Specified Performance	0 to +70°C	"	"	-55°C to +125°C
Operating	-25°C to +85°C	"	"	-55°C to +125°C
Storage	-65°C to +150°C	"	"	"

*Specifications same as AD521JD.
**Specifications same as AD521KD.
Specifications subject to change without notice.

NOTES:

1. Gains below 1 and above 1000 are obtained by simply adjusting the gain setting resistors. (Input voltage should be restricted to ±10V for gains equal to or less than 1.)

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output range of ±9 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.3%.

3. Full Peak Response is the frequency below which a typical amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10μs pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10μs pulse at a 1kHz rate. (When a common mode signal greater than V_S −0.5V is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)

6. Output Offset Voltage versus Power Supply includes a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when V_S = 0) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 2 of 3 separate 10 second periods with the test circuit of Figure 8.

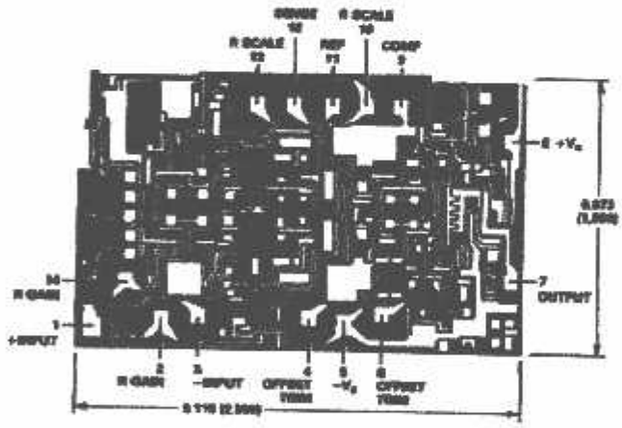
ORDERING GUIDE

Model	Temperature Range	Description	Package Option[1]
AD521JD	0°C to +70°C	14-Pin Ceramic DIP	D-14
AD521KD	0°C to +70°C	14-Pin Ceramic DIP	D-14
AD521LD	0°C to +70°C	14-Pin Ceramic DIP	D-14
AD521SD	−55°C to +125°C	14-Pin Ceramic DIP	D-14
AD521SD/883B[2]	−55°C to +125°C	14-Pin Ceramic DIP	D-14
AD521J Chips	0°C to +70°C	Die	
AD521K Chips	0°C to +70°C	Die	
AD521S Chips	−55°C to +125°C	Die	

NOTES
[1]For outline information see Package Information section.
[2]Standard military drawing available.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



DESIGN PRINCIPLE

Figure 1 is a simplified schematic of the AD521. A differential input voltage, V_{IN}, appears across R_G causing an imbalance in the currents through Q_1 and Q_2, $\Delta I = V_{IN}/R_G$. That imbalance is forced to flow in R_S because the collector currents of Q_3 and Q_4 are constrained to be equal by their biasing (current mirror). These conditions can only be satisfied if the differential voltage across R_S (and hence the output voltage of the AD521) is equal to $\Delta I \times R_S$. The feedback amplifier, A_{FB} performs that function. Therefore, $V_{OUT} = \frac{V_{IN}}{R_G} \times R_S$ or $\frac{V_{OUT}}{V_{IN}} = \frac{R_S}{R_G}$

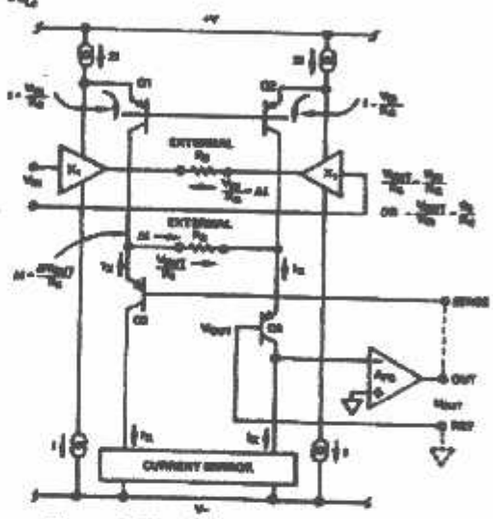


Figure 1. Simplified AD521 Schematic

APPLICATION NOTES FOR THE AD521

These notes ensure the AD521 will achieve the high level of performance necessary for many diversified IA applications.

1. Gains below 1 are realized by adjusting the gain setting resistors as shown in Figure 2 (the resistor, R_S between pins 10 and 13 should remain 100kΩ ±15%, see application note 3). For best results, the input voltage should be restricted to ±10V even though the gain may be less than 1. See Figure 6 for gains above 1000.

2. Provide a return path to ground for input bias currents. The AD521 is an instrumentation amplifier, not an isolation amplifier. When using a thermocouple or other "floating" source, this return path may be provided directly to ground or indirectly through a resistor to ground from pins 1 and/or 3, as shown in Figure 3. If the return path is not provided, bias currents will cause the output to saturate. The value of the resistor may be determined by dividing the maximum allowable common mode voltage for the application by the bias current of the instrumentation amplifier.

3. The resistors between pins 10 and 13, (R_{SCALE}) must equal 100kΩ ±15% (Figure 2). If R_{SCALE} is too low (below 85kΩ) the output swing of the AD521 is reduced. At values below 80kΩ and above 120kΩ the stability of the AD521 may be impaired.

4. Do not exceed the allowable input signal range. The linearity of the AD521 decreases if the inputs are driven within 5 volts of the supply rails, particularly when the device is used at a gain less than 1. To avoid this possibility, attenuate the input signal through a resistive divider network and use the AD521 as a buffer, as shown in Figure 4. The resistor R/2 matches the impedance seen by both AD521 inputs so that the voltage offset caused by bias currents will be minimized.

5. Use the compensation pin (pin 9) and the applicable compensation circuit when the amplifier is required to drive a capacitive load. It is worth mentioning that coaxial cables can "invisibly" provide such capacitance since many popular coaxial cables display capacitance in the vicinity of 30pF per foot.

This compensation (bandwidth control) feature permits the user to fit the response of the AD521 to the particular application as illustrated by Figure 5. In cases of extremely high load capacitance the compensation circuit may be changed as follows:

1. Reduce 680Ω to 24Ω
2. Reduce 330Ω to 7.5Ω
3. Increase 1000pF to 0.1μF
4. Set C_X to 1000pF if no compensation was originally used. Otherwise, do not alter the original value.

This allows stable operation for load capacitances up to 3000pF, but limits the slew rate to approximately 0.16V/μs.

6. Signals having frequency components above the Instrumentation Amplifier's output amplifier closed-loop bandwidth will be transmitted from V– to the output with little or no attenuation. Therefore, it is advisable to decouple the V– supply line to the output common or to pin 11.[1]

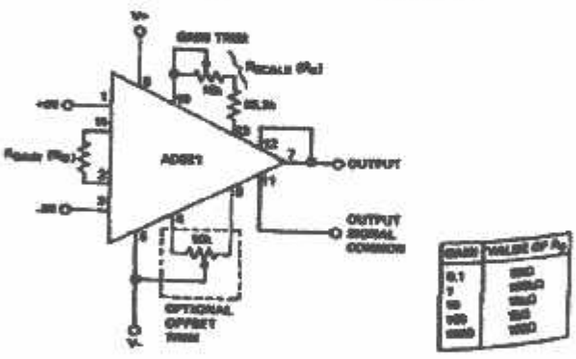
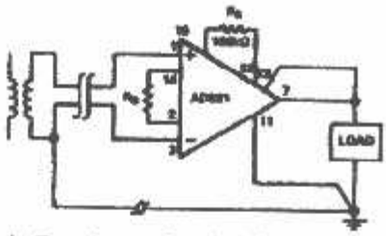
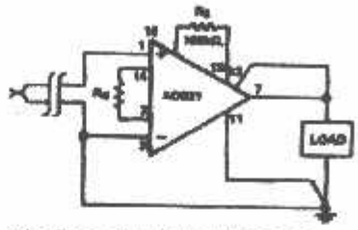


Figure 2. Operating Connections for AD521

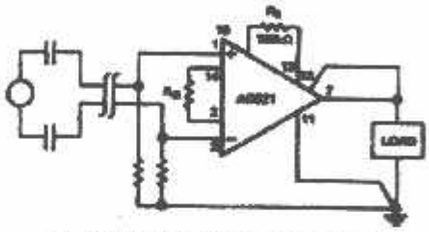
[1] For further details, refer to "An I.C. User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A. Paul Brokaw. This application note is available from Analog Devices without charge upon request.



a). Transformer Coupled, Direct Return

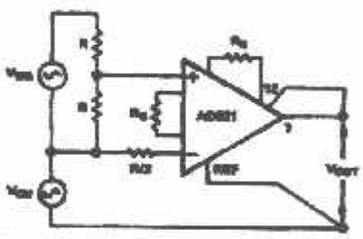


b). Thermocouple, Direct Return



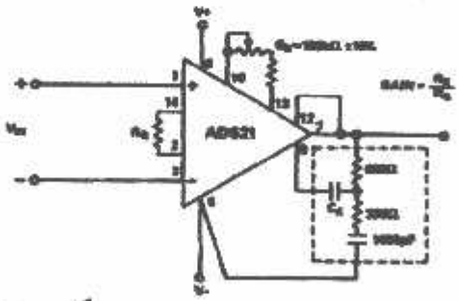
c). AC Coupled, Indirect Return

Figure 3. Ground Returns for "Floating" Transducers



1. INCREASE R_G TO PICK UP GAIN LOST BY R DIVIDER NETWORK
2. INPUT SIGNAL MUST BE REDUCED IN PROPORTION TO POWER SUPPLY VOLTAGE LEVEL

Figure 4. Operating Conditions for $V_{IN}=V_S=10V$



$C_X = \frac{1}{100\pi f_c}$ when f_c is the desired bandwidth.

(f_c in kHz, C_X in μF)

Figure 5. Optional Compensation Circuit

INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output with any gain or circuit configuration. An op amp with 1mV of input offset voltage, for example, would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain can be classified as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the *total* output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or: 30mV + 100(-0.7mV) = -40mV.

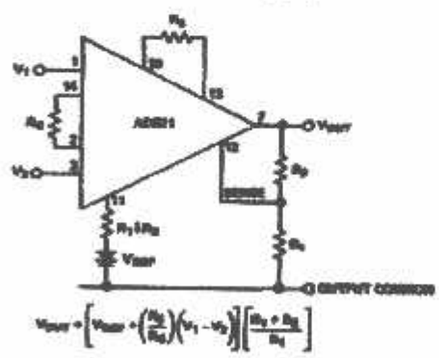
By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error *referred to the input* (R.T.I.) or *output* (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain x input error) + output error

The offset trim adjustment (pins 4 and 6, Figure 2) is associated primarily with the output offset. At any gain it can be used to introduce an output offset equal and opposite to the input offset voltage multiplied by the gain. As a result, the total output offset can be reduced to zero.

As shown in Figure 6, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio, R_G/R_C). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by R_1 and R_2. This gain factor is $1 + R_2/R_1$.



$$V_{OUT} = \left[V_{REF} + \left(\frac{R_2}{R_1}\right)(V_1 - V_2)\right]\left[\frac{R_3 + R_4}{R_4}\right]$$

Figure 6. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing R1 and R2 will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

Where offset errors are critical, a resistor equal to the parallel combination of R_1 and R_2 should be placed between pin 11 and V_{REF}. This minimizes the offset errors resulting from the input current flowing in R_1 and R_2 at the sense terminal. Note that gain changes introduced by changing the R_1/R_2 attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired, V_{REF} can be placed in series with pin 11. This offset is then multiplied by the gain factor $1 + R_2/R_1$ as shown in the equation of Figure 6.

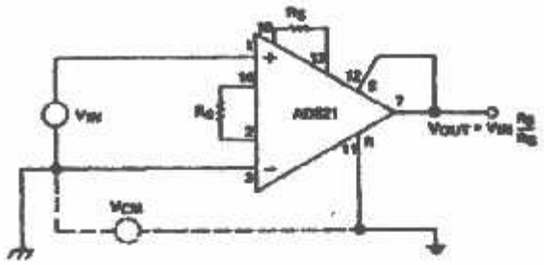


Figure 7. Ground loop elimination. The reference input, Pin 11, allows remote referencing of ground potential. Differences in ground potentials are attenuated by the high CMRR of the AD521.

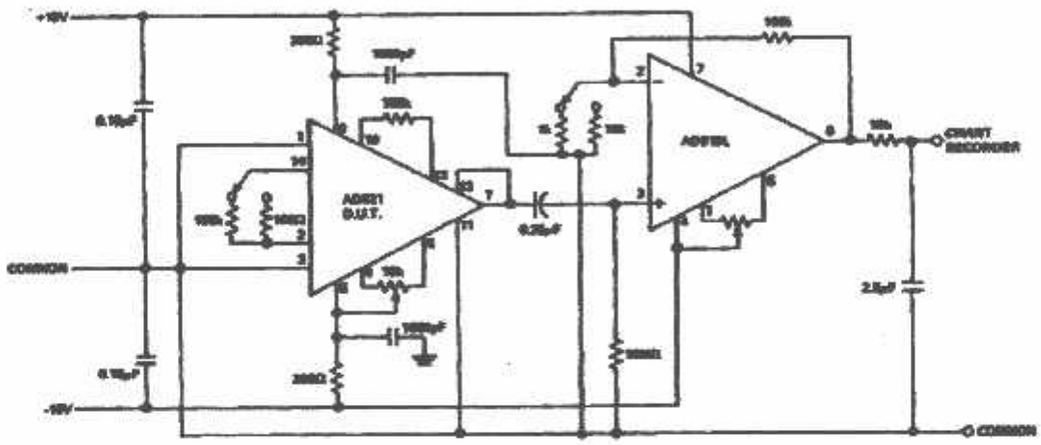


Figure 8. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.

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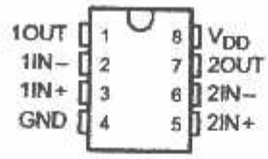
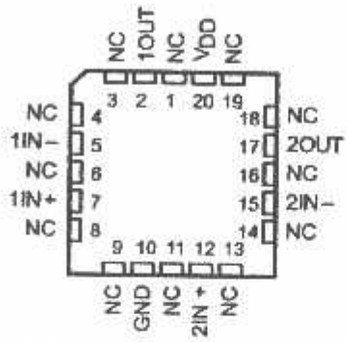
- **Trimmed Offset Voltage:**
  TLC277 . . . 500 μV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  0°C to 70°C . . . 3 V to 16 V
  –40°C to 85°C . . . 4 V to 16 V
  –55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Low Noise . . . Typically 25 nV/√Hz at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-in Latch-Up Immunity**

D, JG, P, OR PW PACKAGE
(TOP VIEW)

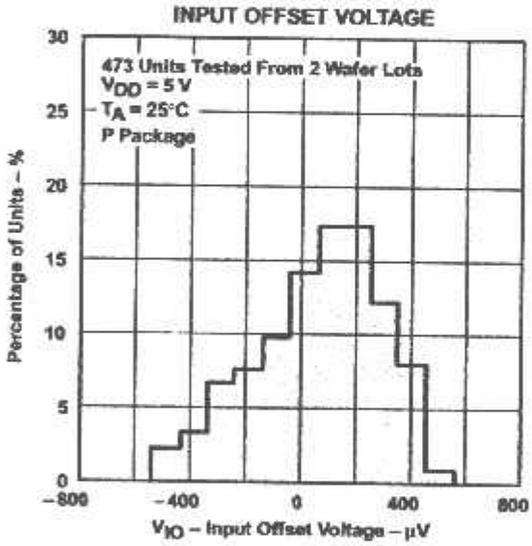


FK PACKAGE
(TOP VIEW)



NC – No internal connection

DISTRIBUTION OF TLC277
INPUT OFFSET VOLTAGE



description

The TLC272 and TLC277 precision dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general-purpose BiFET devices.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC272 (10 mV) to the high-precision TLC277 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

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AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	500 µV	TLC277CD	—	—	TLC277CP	—	—
	2 mV	TLC272BCD	—	—	TLC272BCP	—	—
	5 mV	TLC272ACD	—	—	TLC272ACP	—	—
	10mV	TLC272CD	—	—	TLC272CP	TLC272CPW	TLC272Y
–40°C to 85°C	500 µV	TLC277ID	—	—	TLC277IP	—	—
	2 mV	TLC272BID	—	—	TLC272BIP	—	—
	5 mV	TLC272AID	—	—	TLC272AIP	—	—
	10 mV	TLC272ID	—	—	TLC272IP	—	—
–55°C to 125°C	500 µV	TLC277MD	TLC277MFK	TLC277MJG	TLC277MP	—	—
	10 mV	TLC272MD	TLC272MFK	TLC272MJG	TLC272MP	—	—

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC277CDR).

description (continued)

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

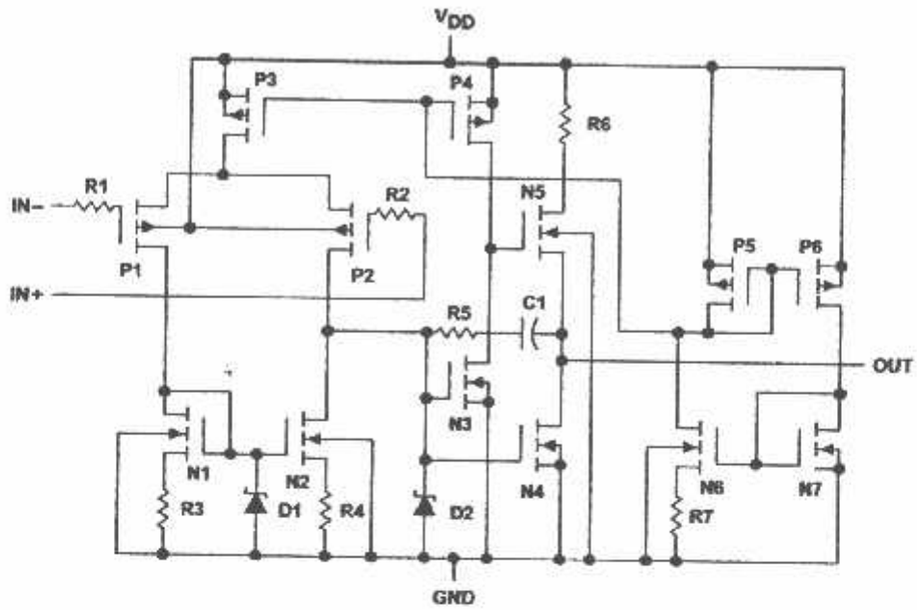
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

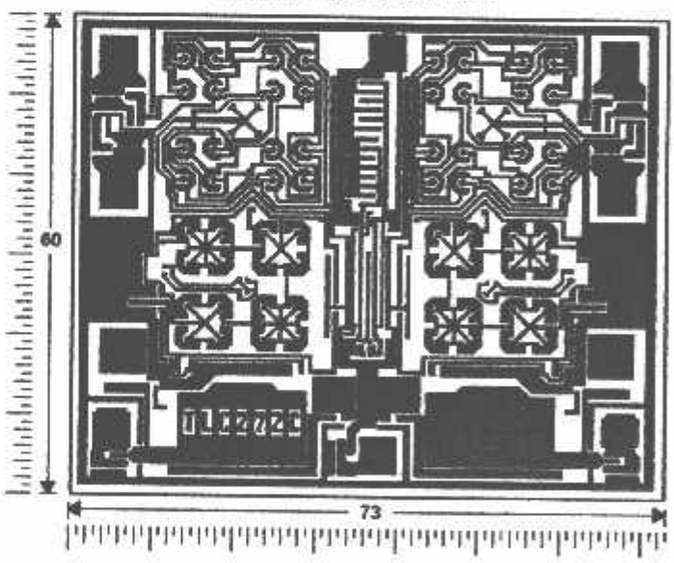
equivalent schematic (each amplifier)

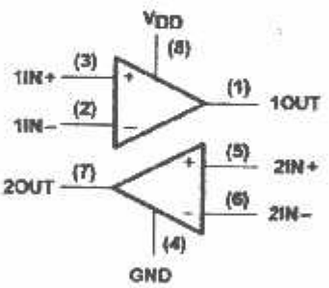


TLC272Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC272C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_{jmax} = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 18 V
Differential input voltage, V_{ID} (see Note 2) ..... $\pm V_{DD}$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
output current, I_O (each output) ..... ±30 mA
Total current into V_{DD} ..... 45 mA
Total current out of GND ..... 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A
PW	525 mW	4.2 mW/°C	336 mW	N/A	N/A

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		3	16	4	16	4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	−0.2	3.5	−0.2	3.5	0	3.5	V
	V_{DD} = 10 V	−0.2	8.5	−0.2	8.5	0	8.5	
Operating free-air temperature, T_A		0	70	−40	85	−55	125	°C

TEXAS INSTRUMENTS
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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC272AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC272BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		230	2000	μV
					Full range			3000	
		TLC277C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		200	500	
					Full range			1500	
α_{VIO}	Temperature coefficient of input offset voltage				25°C to 70°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					0°C	3	3.8		
					70°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					0°C	4	27		
					70°C	4	20		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	80		dB
					0°C	60	84		
					70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		
					70°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 5 V,	25°C		1.4	3.2	mA
					0°C		1.6	3.6	
					70°C		1.2	2.6	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC272AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC272BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		290	2000	μV
					Full range			3000	
		TLC277C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		250	800	
					Full range			1900	
α_{VIO}	Temperature coefficient of input offset voltage				25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					0°C	7.8	8.5		
					70°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	38		V/mV
					0°C	7.5	42		
					70°C	7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	85		dB
					0°C	60	88		
					70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		
					70°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 5 V,	25°C		1.9	4	mA
					0°C		2.3	4.4	
					70°C		1.6	3.4	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC272AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			7	
		TLC272BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		230	2000	μV
					Full range			3500	
		TLC277I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		200	500	
					Full range			2000	
α_{VIO}	Temperature coefficient of input offset voltage				25°C to 85°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					85°C		24	15	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					85°C		200	35	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					−40°C	3	3.8		
					85°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					−40°C	3.5	32		
					85°C	3.5	19		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	80		dB
					−40°C	60	81		
					85°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−40°C	60	92		
					85°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		1.4	3.2	mA
					−40°C		1.9	4.4	
					85°C		1.1	2.4	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V, R_S = 50 Ω	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC272AI	V_O = 1.4 V, R_S = 50 Ω	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			7	
		TLC272BI	V_O = 1.4 V, R_S = 50 Ω	V_{IC} = 0, R_L = 10 kΩ	25°C		290	2000	μV
					Full range			3500	
		TLC277I	V_O = 1.4 V, R_S = 50 Ω	V_{IC} = 0, R_L = 10 kΩ	25°C		250	800	
					Full range			2900	
α_{VIO}	Temperature coefficient of input offset voltage				25°C to 85°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					−40°C	7.8	8.5		
					85°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					−40°C	7	46		
					85°C	7	31		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	85		dB
					−40°C	60	87		
					85°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−40°C	60	92		
					85°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		1.4	4	mA
					−40°C		2.8	5	
					85°C		1.5	3.2	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC272M, TLC277M			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC277M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		200	500	μV
					Full range			3750	
α_{VIO}	Temperature coefficient of input offset voltage				25°C to 125°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V	V_{IC} = 2.5 V	25°C		0.1		pA
					125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V	V_{IC} = 2.5 V	25°C		0.6		pA
					125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 4	−0.3 to 4.2		V
					Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					−55°C	3	3.8		
					125°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V	R_L = 10 kΩ	25°C	5	23		V/mV
					−55°C	3.5	35		
					125°C	3.5	16		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	80		dB
					−55°C	60	81		
					125°C	60	84		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−55°C	60	90		
					125°C	60	97		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		1.4	3.2	mA
					−55°C		2	5	
					125°C		1	2.2	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC272M, TLC277M			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272M	V_O = 1.4 V, R_S = 50 Ω	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC277M	V_O = 1.4 V, R_S = 50 Ω	V_{IC} = 0, R_L = 10 kΩ	25°C		250	800	μV
					Full range			4300	
α_{VIO}	Temperature coefficient of input offset voltage				25°C to 125°C		2.2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					−55°C	7.8	8.5		
					125°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					−55°C	7	50		
					125°C	7	27		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	85		dB
					−55°C	60	87		
					125°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−55°C	60	90		
					125°C	60	97		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		1.9	4	mA
					−55°C		3	6	
					125°C		1.3	2.8	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC272Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, R_S = 50 Ω	V_{IC} = 0, R_L = 10 kΩ		1.1	10	mV
α_{VIO}	Temperature coefficient of input offset voltage				1.8		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 2.5 V,	V_{IC} = 2.5 V		0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 2.5 V,	V_{IC} = 2.5 V		0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	R_L = 10 kΩ	3.2	3.8		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV,	I_{OL} = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V to 2 V	R_L = 10 kΩ	5	23		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V,	V_O = 1.4 V	65	95		dB
I_{DD}	Supply current (two amplifiers)	V_O = 2.5 V, No load	V_{IC} = 2.5 V,		1.4	3.2	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics, V_{DD} = 10 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC272Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, R_S = 50 Ω	V_{IC} = 0, R_L = 10 kΩ		1.1	10	mV
α_{VIO}	Temperature coefficient of input offset voltage				1.8		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 5 V,	V_{IC} = 5 V		0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 5 V,	V_{IC} = 5 V		0.7		pA
V_{ICR}	Common-mode input voltage range (see Note 5)			−0.2 to 9	−0.3 to 9.2		V
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	R_L = 10 kΩ	8	8.5		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV,	I_{OL} = 0		0	50	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 6 V,	R_L = 10 kΩ	10	36		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min		65	85		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V,	V_O = 1.4 V	65	95		dB
I_{DD}	Supply current (two amplifiers)	V_O = 5 V, No load	V_{IC} = 5 V,		1.9	4	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			V_{IPP} = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				0°C		47°		
				70°C		43°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			V_{IPP} = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				0°C		50°		
				70°C		46°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−40°C		4.5		
				85°C		2.8		
			V_{IPP} = 2.5 V	25°C		2.9		
				−40°C		3.5		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−40°C		380		
				85°C		250		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−40°C		2.6		
				85°C		1.2		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−40°C		49°		
				85°C		43°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−40°C		6.8		
				85°C		4		
			V_{IPP} = 5.5 V	25°C		4.6		
				−40°C		5.8		
				85°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−40°C		260		
				85°C		130		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−40°C		3.1		
				85°C		1.7		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−40°C		52°		
				85°C		46°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLC272M, TLC277M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.8		V/μs
				−55°C		4.7		
				125°C		2.3		
			V_{IPP} = 2.5 V	25°C		2.9		
				−55°C		3.7		
				125°C		2		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−55°C		400		
				125°C		230		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−55°C		2.9		
				125°C		1.1		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−55°C		49°		
				125°C		41°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	TLC272M, TLC277M			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−55°C		7.1		
				125°C		3.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				−55°C		6.1		
				125°C		2.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−55°C		280		
				125°C		110		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−55°C		3.4		
				125°C		1.6		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−55°C		52°		
				125°C		44°		

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			TLC272Y			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, See Figure 1	C_L = 20 pF,	V_{IPP} = 1 V		3.6		V/μs
				V_{IPP} = 2.5 V		2.9		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω,	See Figure 2		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, See Figure 1	C_L = 20 pF,	R_L = 10 kΩ,		320		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF,	See Figure 3		1.7		MHz
ϕ_m	Phase margin	V_I = 10 mV, See Figure 3	f = B_1,	C_L = 20 pF,		46°		

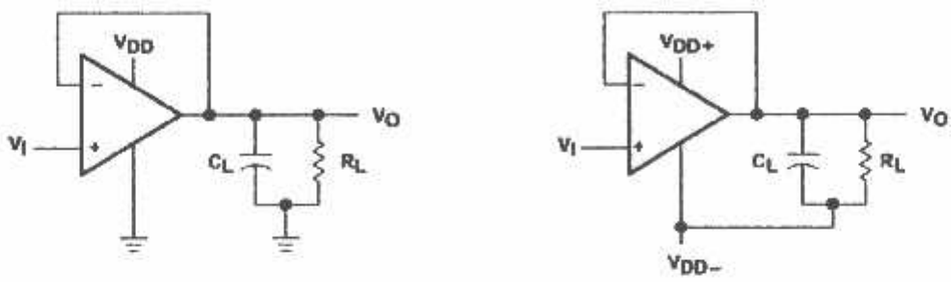
operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			TLC272Y			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, See Figure 1	C_L = 20 pF,	V_{IPP} = 1 V		5.3		V/μs
				V_{IPP} = 5.5 V		4.6		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω,	See Figure 2		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, See Figure 1	C_L = 20 pF,	R_L = 10 kΩ,		200		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV,	C_L = 20 pF,	See Figure 3		2.2		MHz
ϕ_m	Phase margin	V_I = 10 mV, See Figure 3	f = B_1,	C_L = 20 pF,		49°		

PARAMETER MEASUREMENT INFORMATION

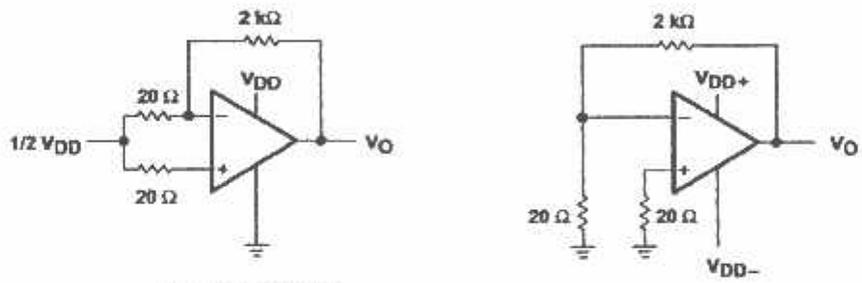
single-supply versus split-supply test circuits

Because the TLC272 and TLC277 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



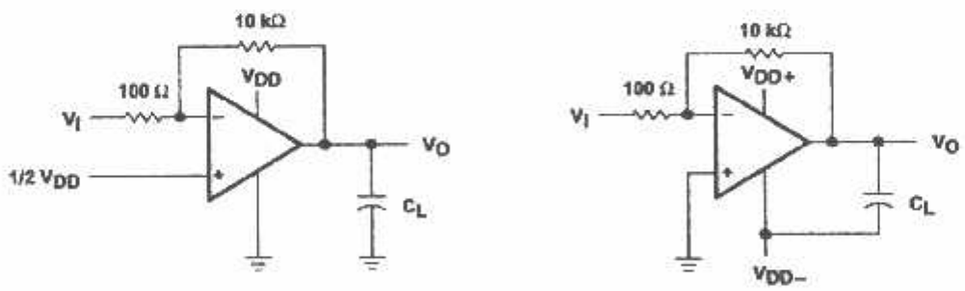
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 1. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 2. Noise-Test Circuit



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 3. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC272 and TLC277 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

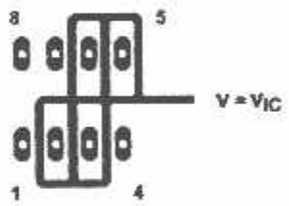


Figure 4. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6, 7
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	8, 9
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I_{IB}	Input bias current	vs Free-air temperature	22
I_{IO}	Input offset current	vs Free-air temperature	22
V_{IC}	Common-mode input voltage	vs Supply voltage	23
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	29
B_1	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	34 35 36
V_n	Equivalent input noise voltage	vs Frequency	37
	Phase shift	vs Frequency	32, 33

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC272
INPUT OFFSET VOLTAGE

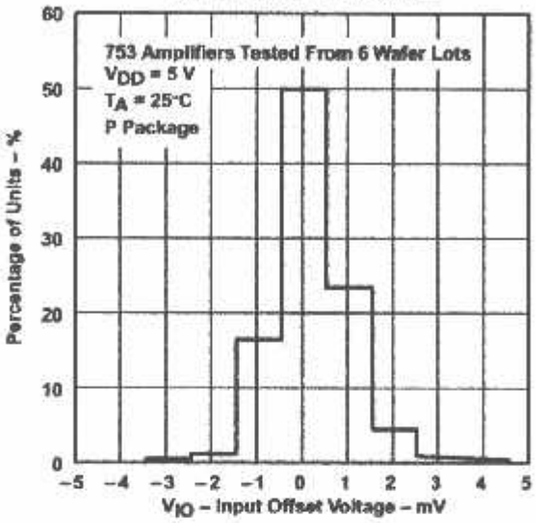


Figure 6

DISTRIBUTION OF TLC272
INPUT OFFSET VOLTAGE

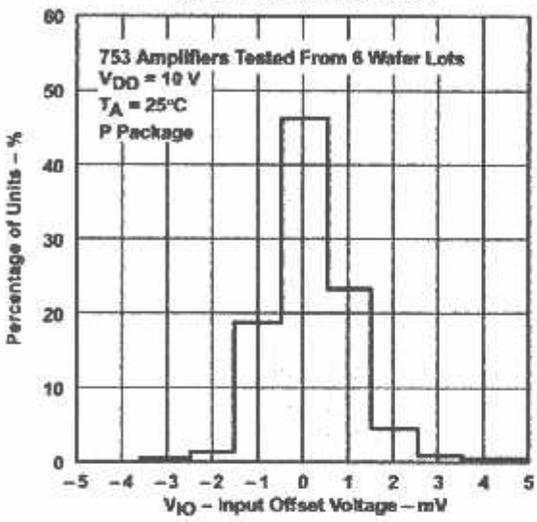


Figure 7

DISTRIBUTION OF TLC272 AND TLC277
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

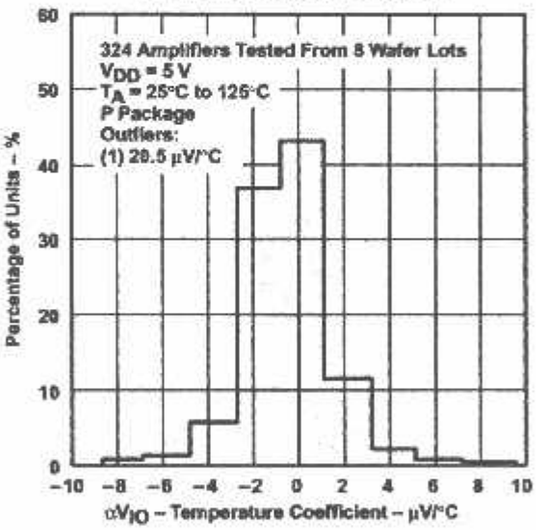


Figure 8

DISTRIBUTION OF TLC272 AND TLC277
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

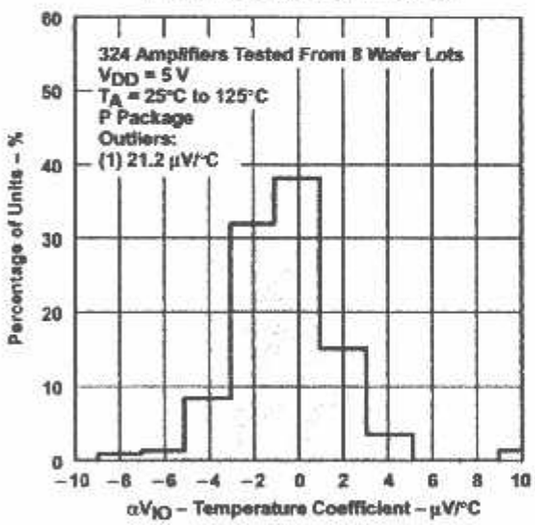
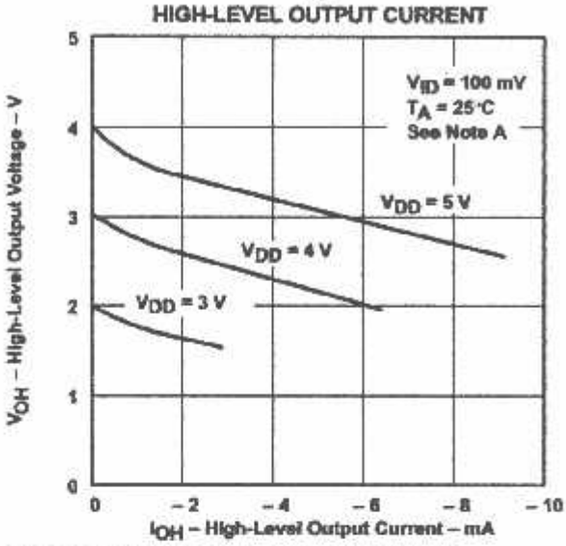


Figure 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT



NOTE A: The 3-V curve only applies to the C version.

Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

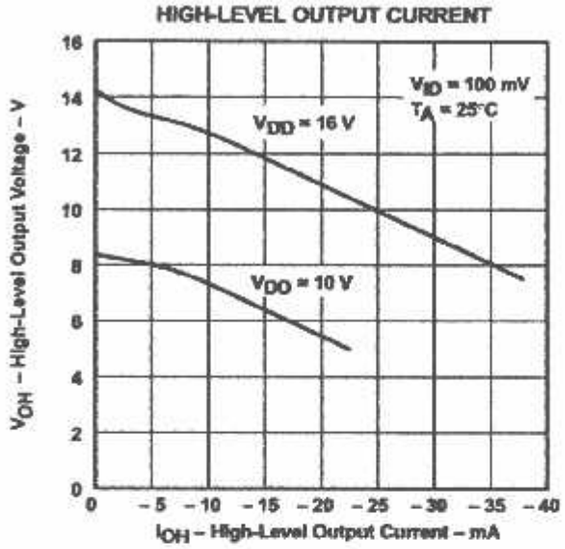


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

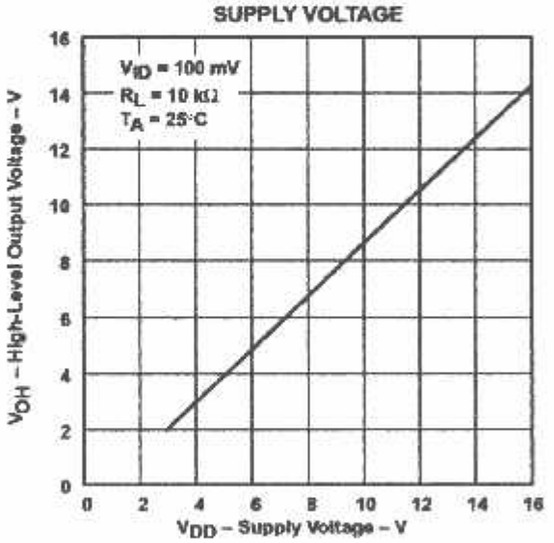


Figure 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

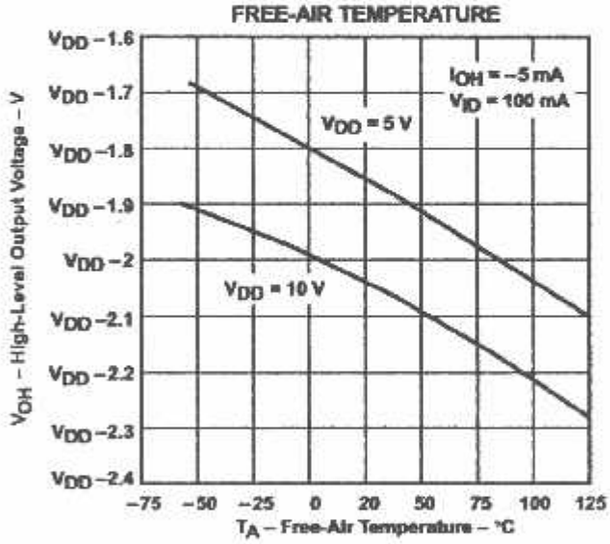


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

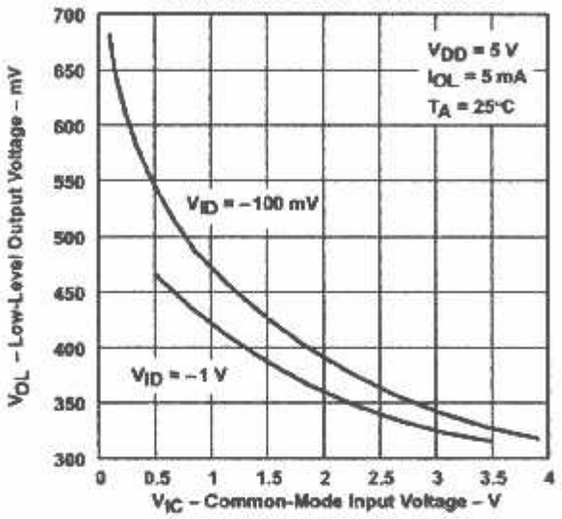


Figure 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

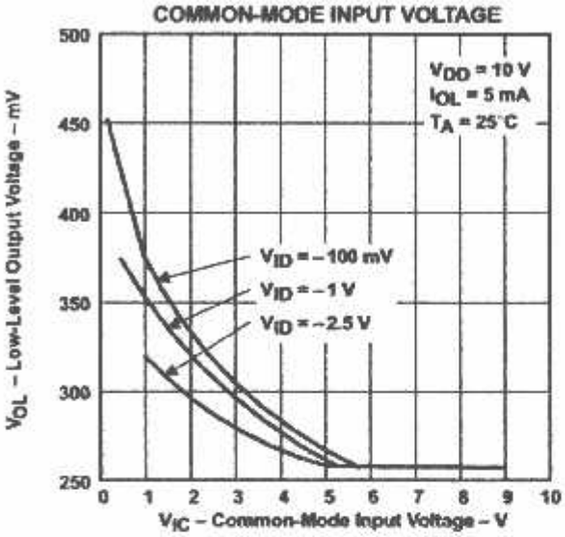


Figure 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

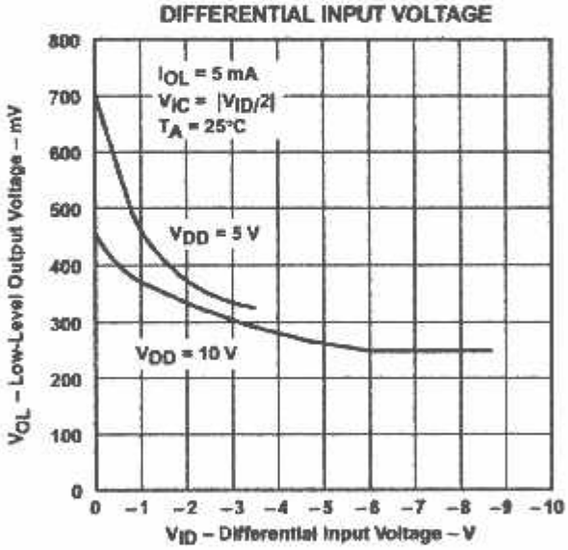


Figure 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

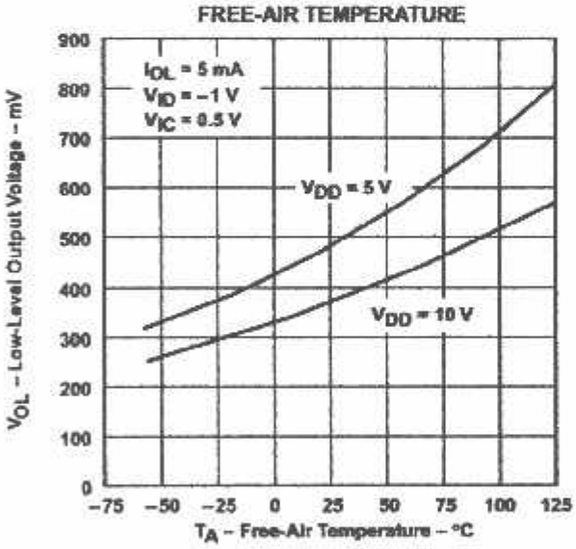
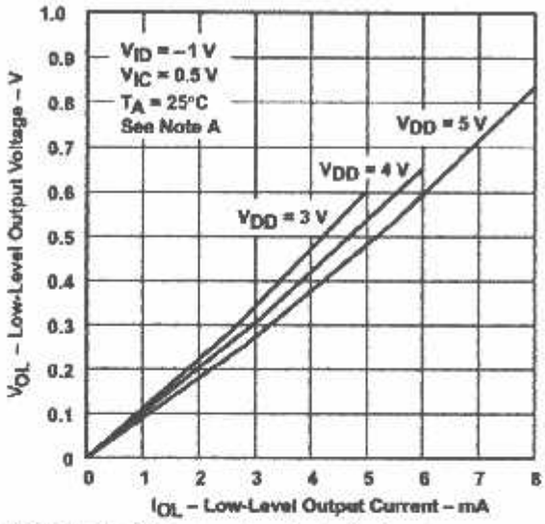


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT



NOTE A: The 3-V curve only applies to the C version.

Figure 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

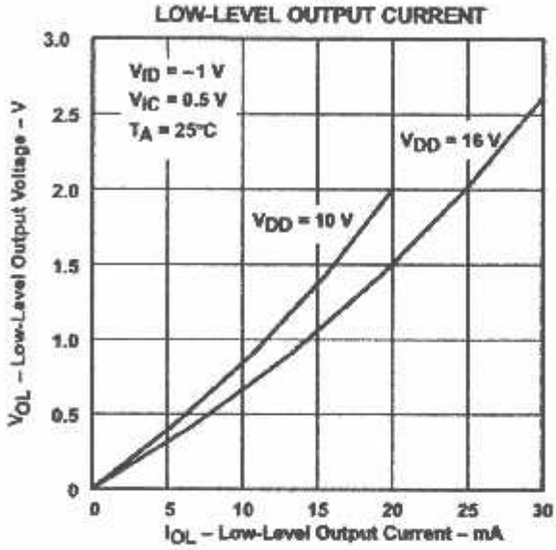


Figure 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

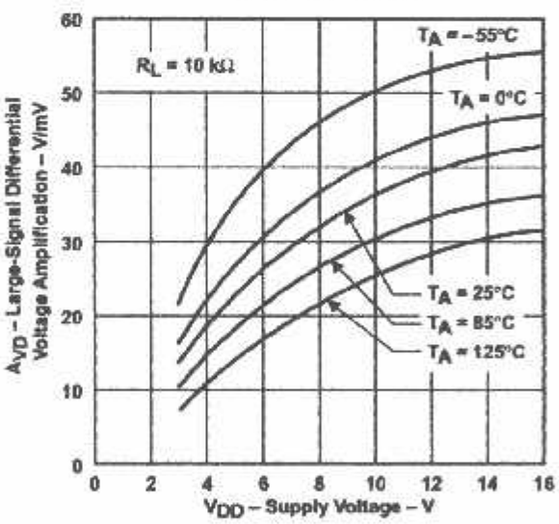


Figure 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

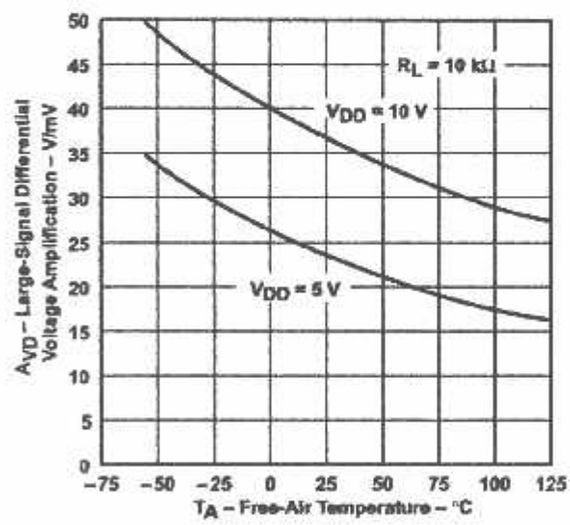
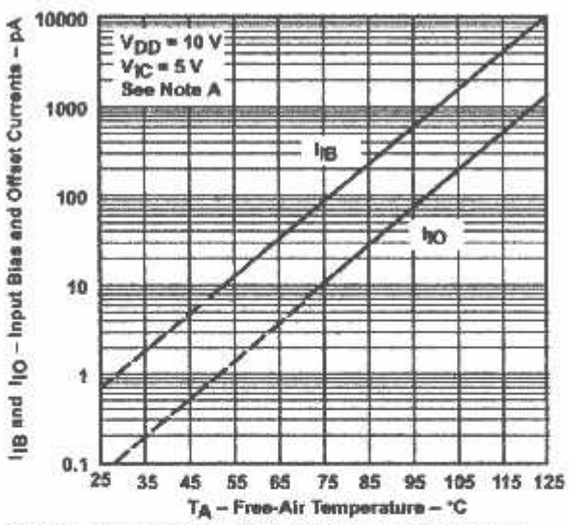


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

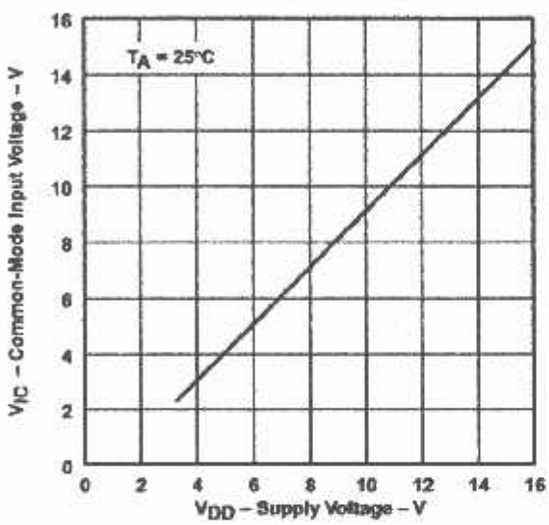


Figure 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

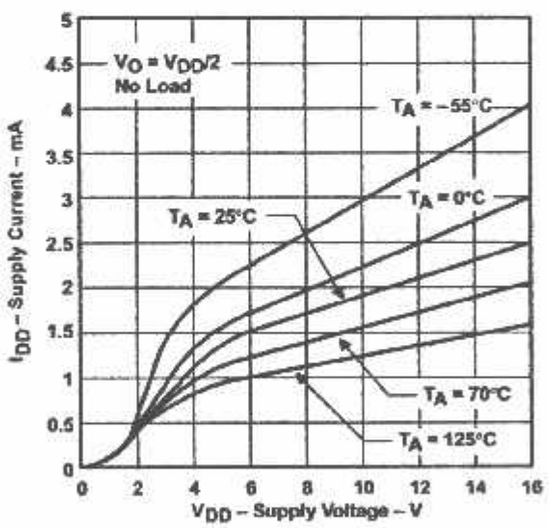


Figure 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

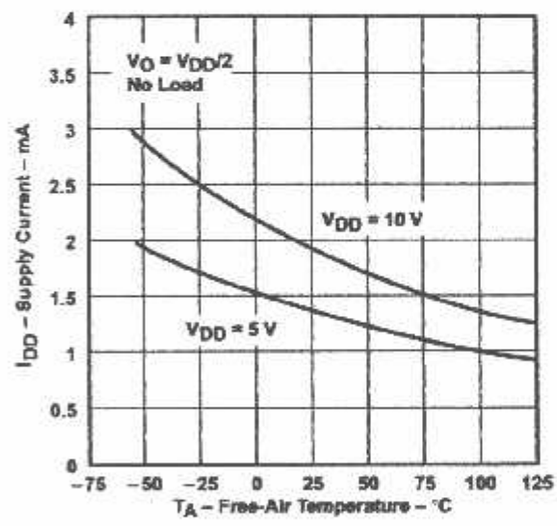


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

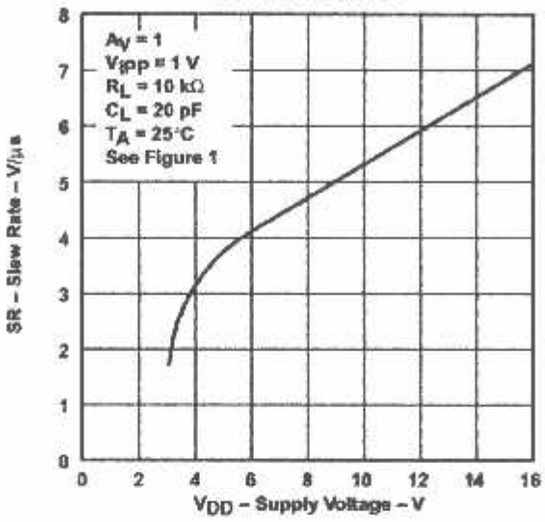


Figure 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

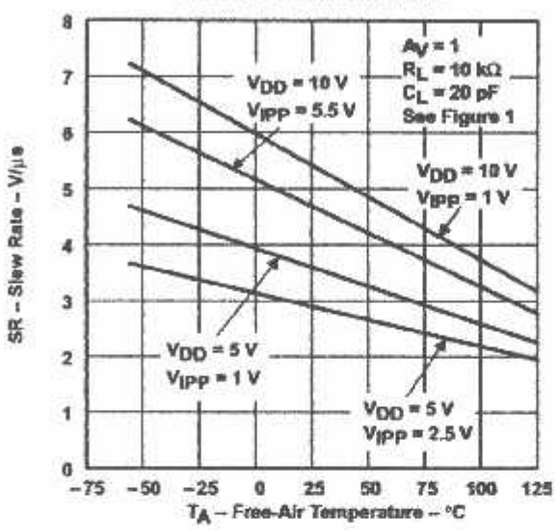


Figure 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

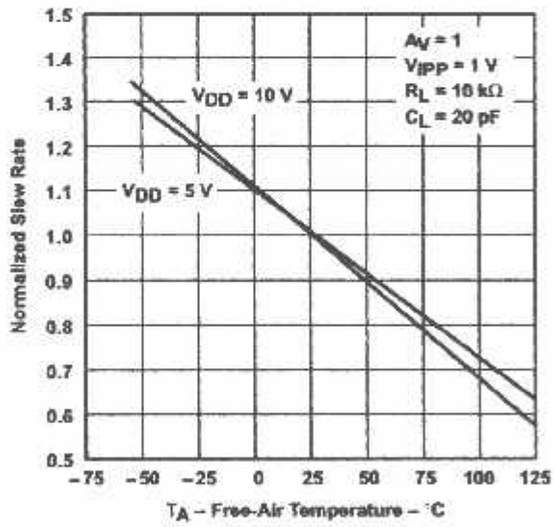


Figure 28

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

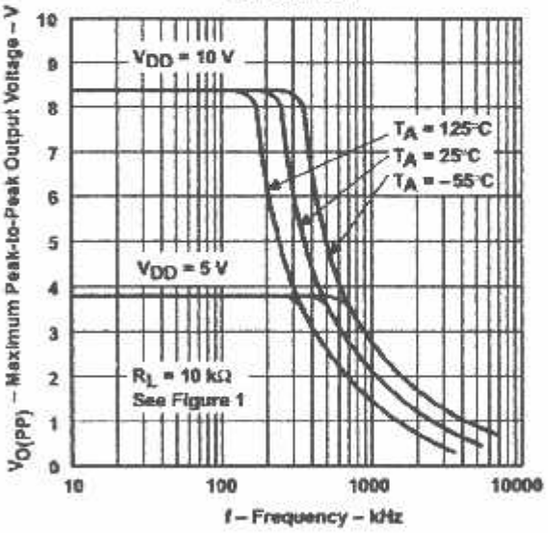


Figure 29

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

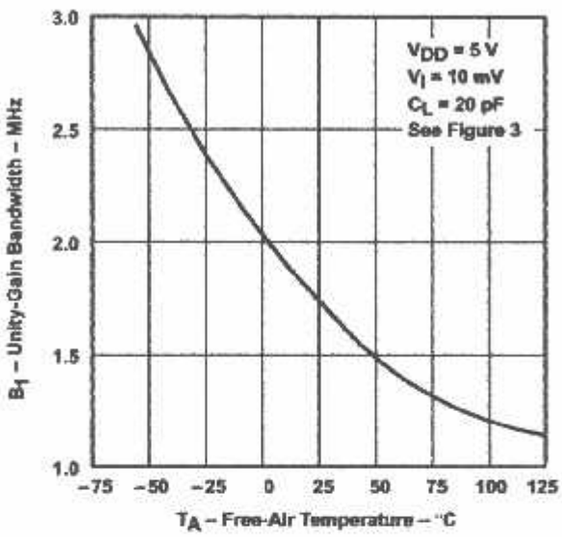


Figure 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

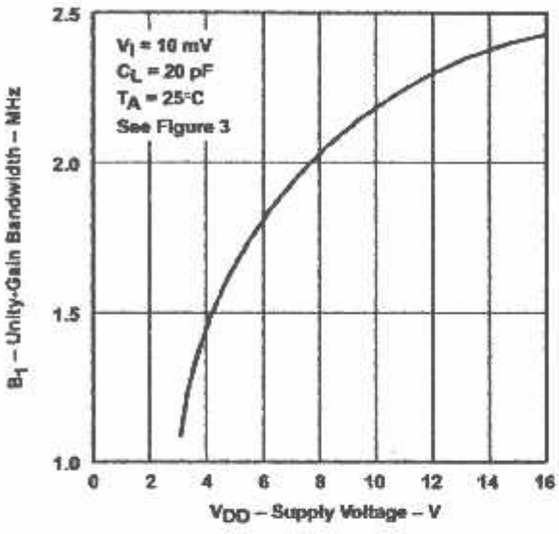


Figure 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

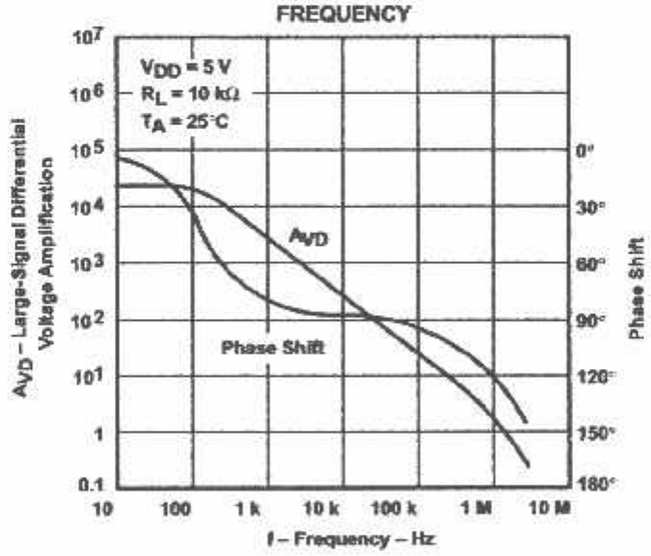


Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

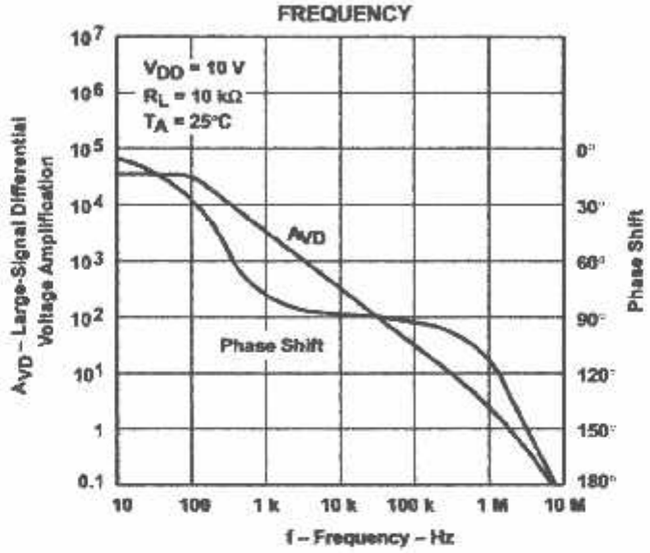


Figure 33

PHASE MARGIN vs SUPPLY VOLTAGE

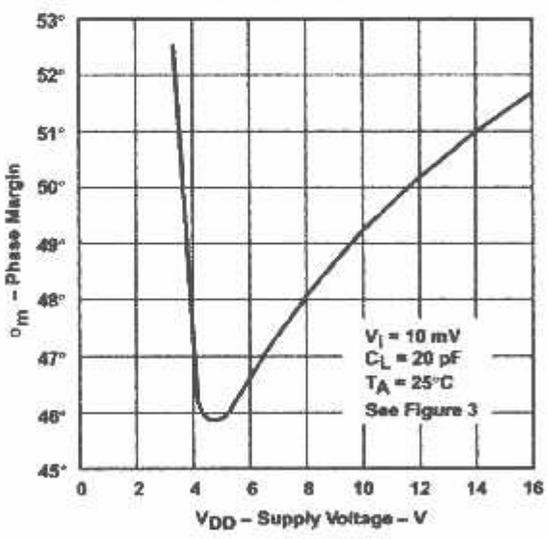


Figure 34

PHASE MARGIN vs FREE-AIR TEMPERATURE

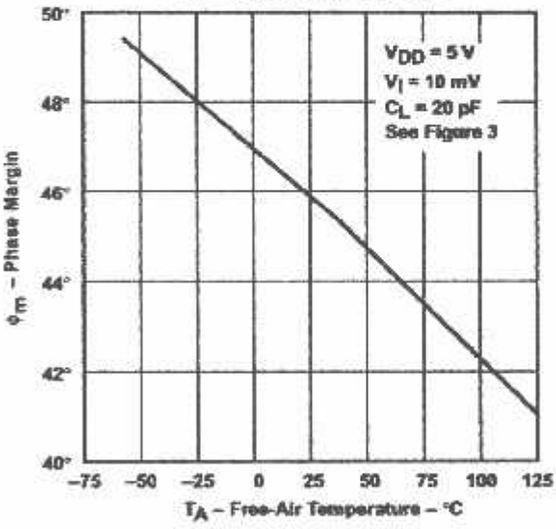


Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
CAPACITIVE LOAD

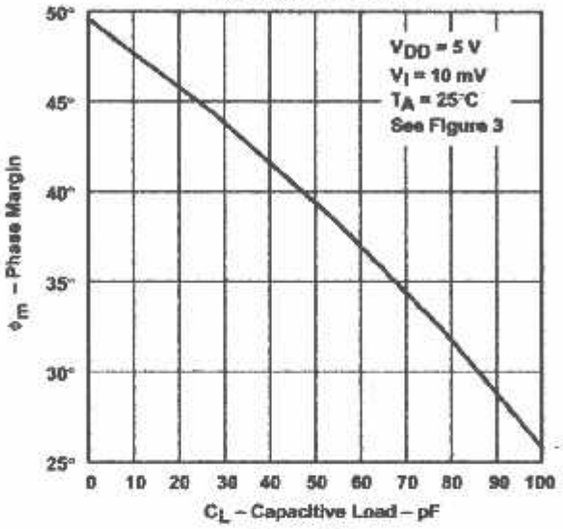


Figure 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

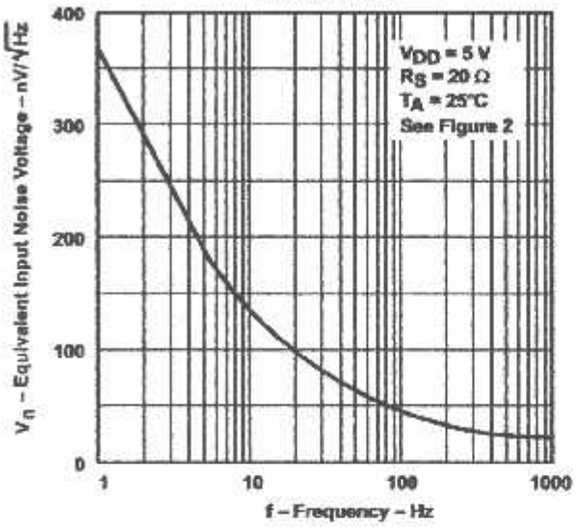


Figure 37

APPLICATION INFORMATION

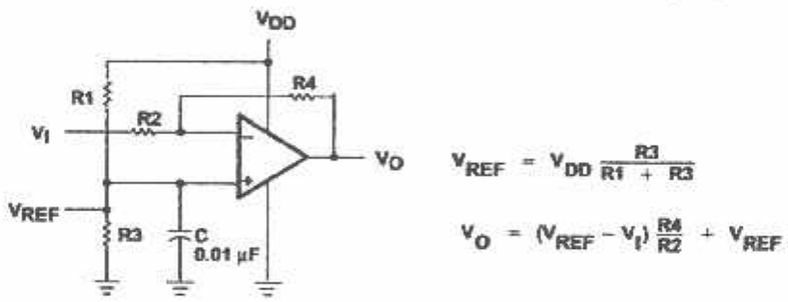
single-supply operation

While the TLC272 and TLC277 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC272 and TLC277 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC272 and TLC277 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

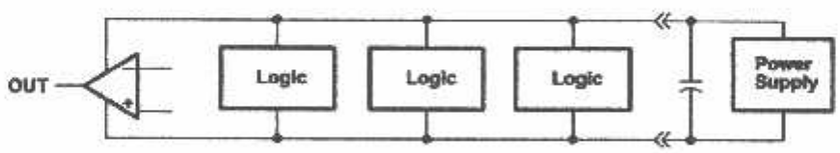
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



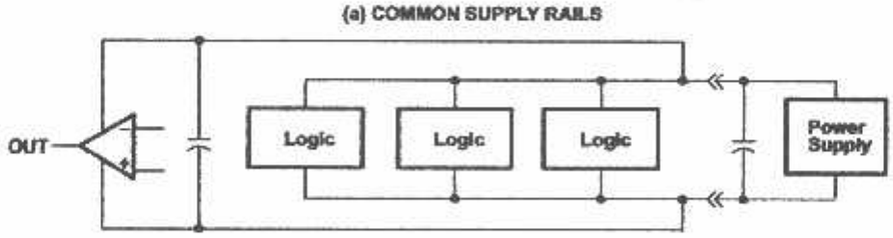
$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

$$V_O = (V_{REF} - V_I) \frac{R4}{R2} + V_{REF}$$

Figure 38. Inverting Amplifier With Voltage Reference



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 39. Common vs Separate Supply Rails

APPLICATION INFORMATION

input characteristics

The TLC272 and TLC277 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.5 V at all other temperatures.

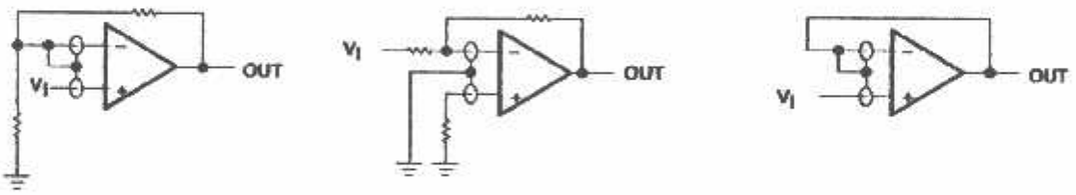
The use of the polysilicon-gate process and the careful input circuit design gives the TLC272 and TLC277 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC272 and TLC277 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC272 and TLC277 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 40. Guard-Ring Schemes

output characteristics

The output stage of the TLC272 and TLC277 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC272 and TLC277 are measured using a 20-pF load. The devices can drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.

APPLICATION INFORMATION

output characteristics (continued)

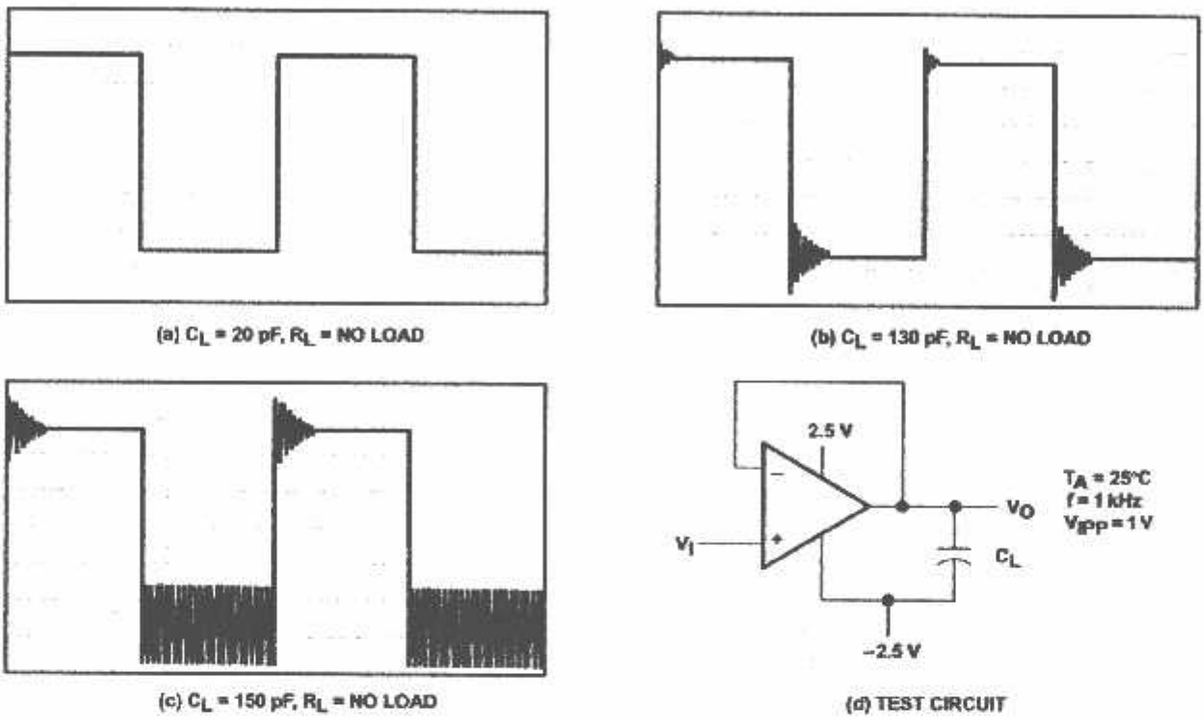
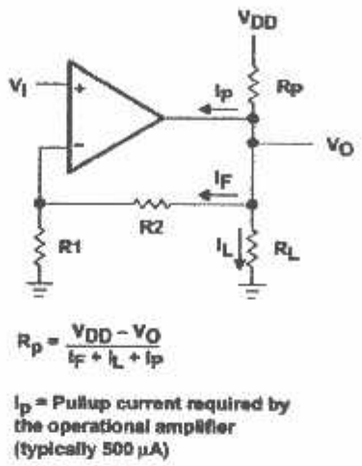


Figure 41. Effect of Capacitive Loads and Test Circuit

Although the TLC272 and TLC277 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

APPLICATION INFORMATION

output characteristics (continued)



$$R_p = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_p = Pullup current required by the operational amplifier (typically 500 µA)

Figure 42. Resistive Pullup to Increase V_{OH}

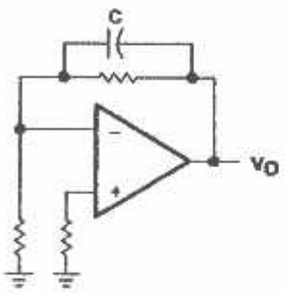


Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits almost always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

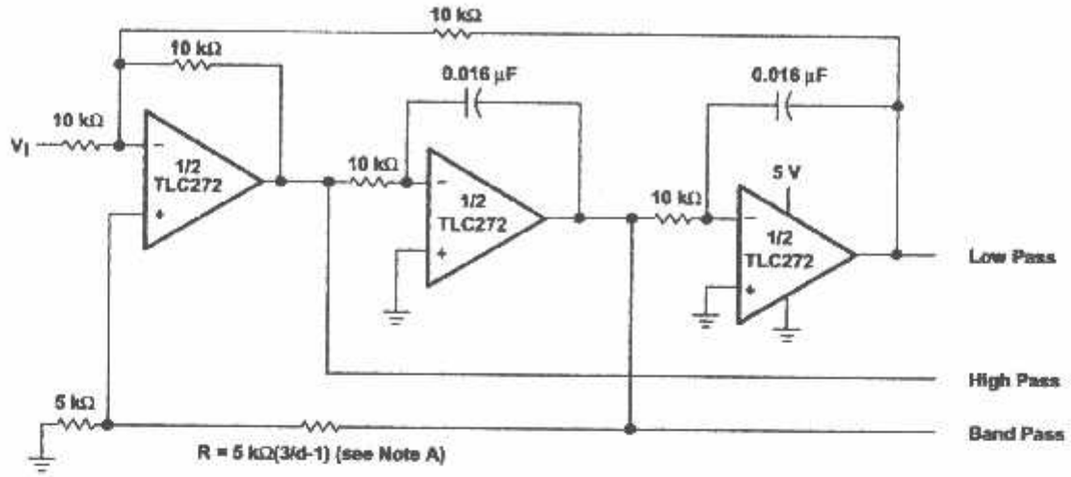
The TLC272 and TLC277 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC272 and TLC277 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

APPLICATION INFORMATION



NOTE A: d = damping factor, 1/Q

Figure 44. State-Variable Filter

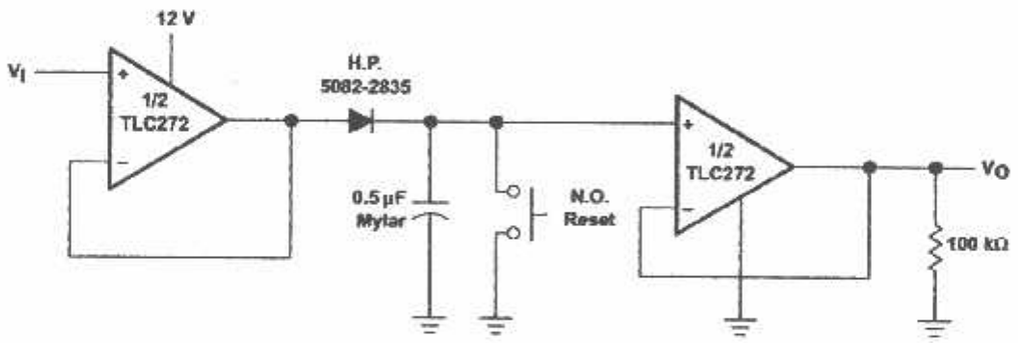
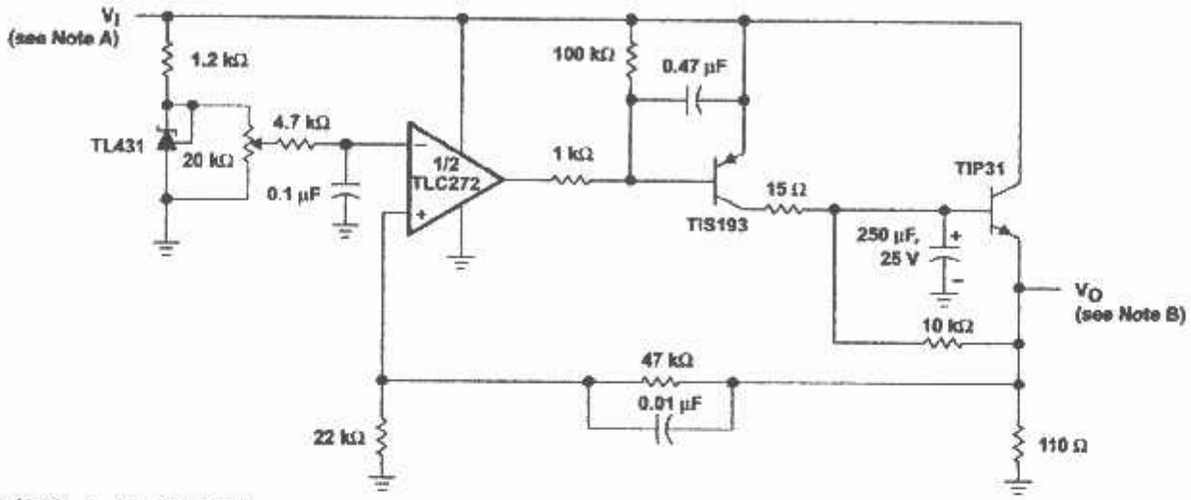


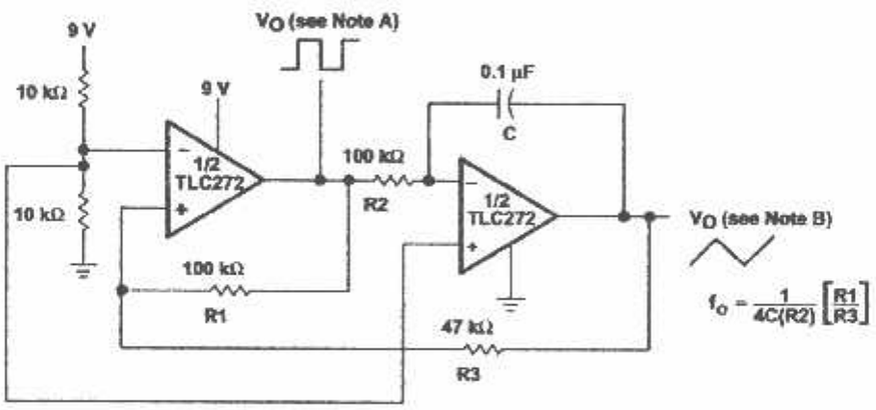
Figure 45. Positive-Peak Detector

APPLICATION INFORMATION



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2 V, 0 to 1 A

Figure 46. Logic-Array Power Supply



NOTES: A. $V_{O(PP)}$ = 8 V
B. $V_{O(PP)}$ = 4 V

Figure 47. Single-Supply Function Generator

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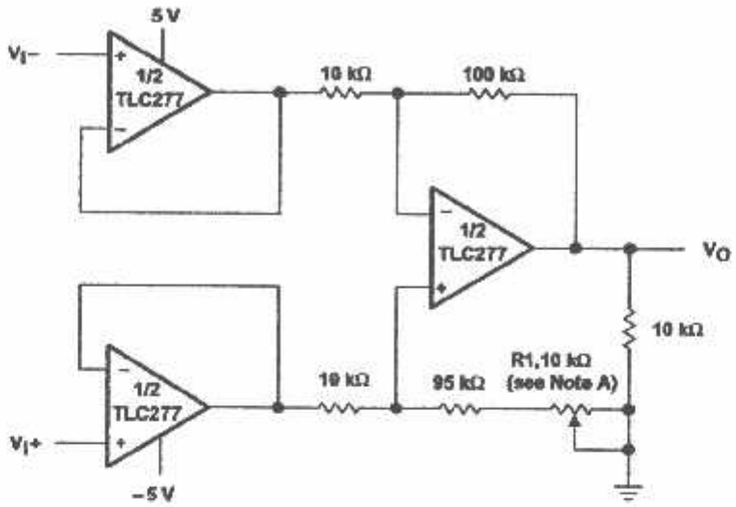
APPLICATION INFORMATION



NOTE B: CMRR adjustment must be noninductive.

Figure 48. Low-Power Instrumentation Amplifier

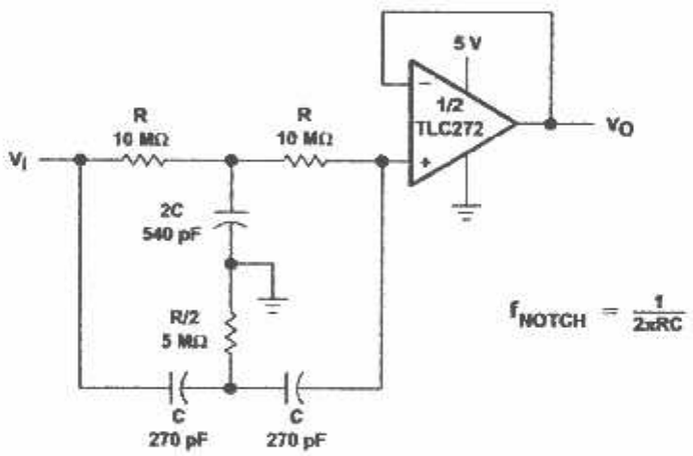


Figure 49. Single-Supply Twin-T Notch Filter

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National Semiconductor

November 1999

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

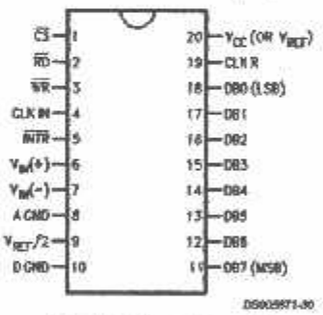
- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution 8 bits
- Total error ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time 100 µs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages



DS005671-30

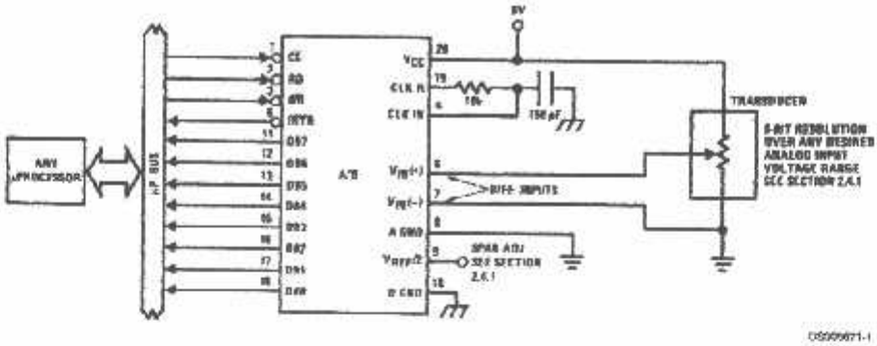
See Ordering Information

Ordering Information

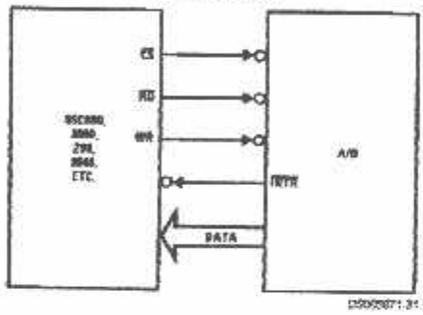
TEMP RANGE		0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted	ADC0802LCWM	ADC0804LCN	ADC0801LCN
	±½ Bit Unadjusted			ADC0802LCN
	±½ Bit Adjusted			ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM		ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B—Small Outline	N20A—Molded DIP	

Z-80® is a registered trademark of Zilog Corp.

Typical Applications



8080 Interface



Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2$=2.500 V_{DC} (No Adjustments)	$V_{REF}/2$=No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0804LCJ	−40°C≤T_A≤+85°C
ADC0801/02/03/05LCN	−40°C≤T_A≤+85°C
ADC0804LCN	0°C≤T_A≤+70°C
ADC0802/04LCWM	0°C≤T_A≤+70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	V_{REF}/2-No Connection			±1	LSB
V_{REF}/2 Input Resistance (Pin 9)	ADC0801/02/03/05	2.5	8.0		kΩ
	ADC0804 (Note 9)	0.75	1.1		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±1/16	±¼	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Notes 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency	V_{CC}=5V, (Note 5)	100	640	1460	kHz
	Clock Duty Cycle		40		60	%
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ =0 V_{DC}, f_{CLK}=640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ =0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS (Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately)						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN}=0 V_{DC}	-1	-0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis (V_T+)-(V_T-)		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O=360 µA V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O=-360 µA V_{CC}=4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT}=1.6 mA, V_{CC}=4.75 V_{DC} I_{OUT}=1.0 mA, V_{CC}=4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=-360 µA, V_{CC}=4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=-10 µA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0 V_{DC} V_{OUT}=5 V_{DC}	-3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A=25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A=25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCWM	f_{CLK}=640 kHz, $V_{REF}/2$=NC, T_A=25°C and $\overline{CS}$ =5V		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct--especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 4* and section 2.0.

AC Electrical Characteristics (Continued)

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

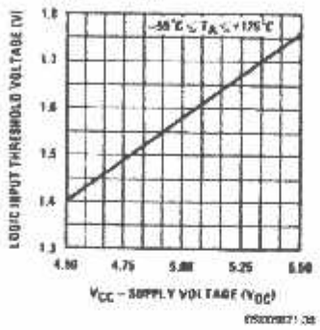
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 7*.

Note 9: The $V_{REF}/2$ pin is the center point of a two-resistor divider connected from V_{CC} to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

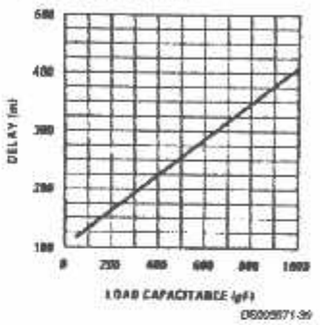
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

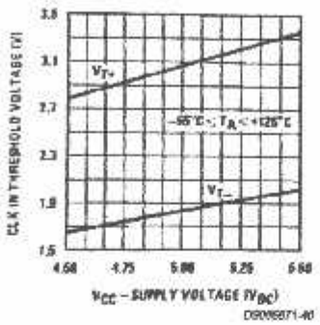
Logic Input Threshold Voltage vs. Supply Voltage



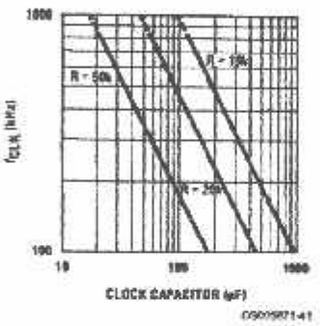
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



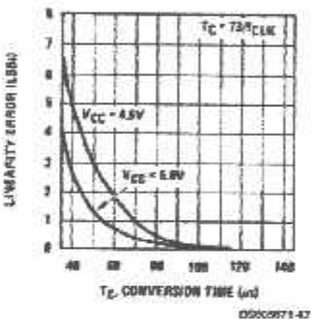
CLK IN Schmitt Trip Levels vs. Supply Voltage



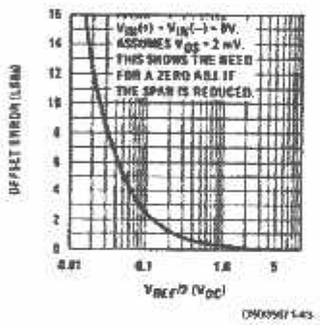
f_{CLK} vs. Clock Capacitor



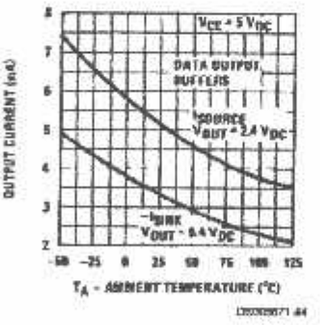
Full-Scale Error vs Conversion Time



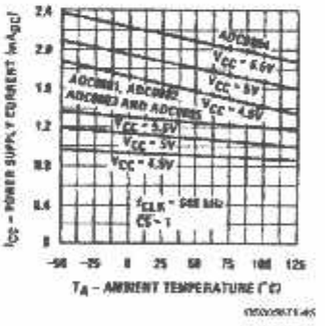
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



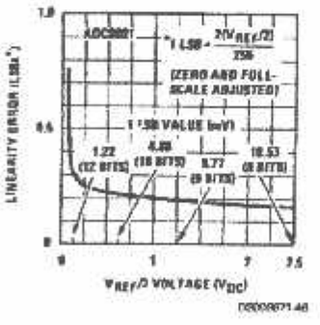
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)

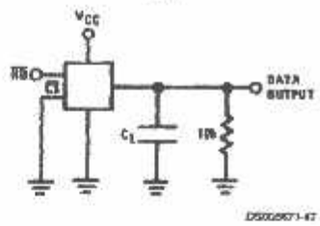


Linearity Error at Low $V_{REF}/2$ Voltages

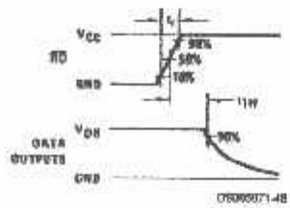


TRI-STATE Test Circuits and Waveforms

t_{1H}

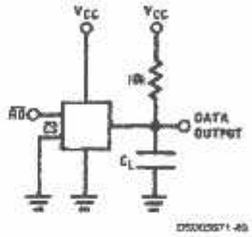


t_{1H}, C_L=10 pF

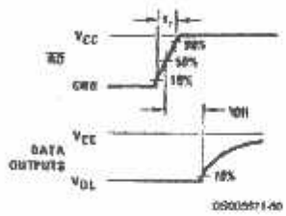


t_r=20 ns

t_{0H}

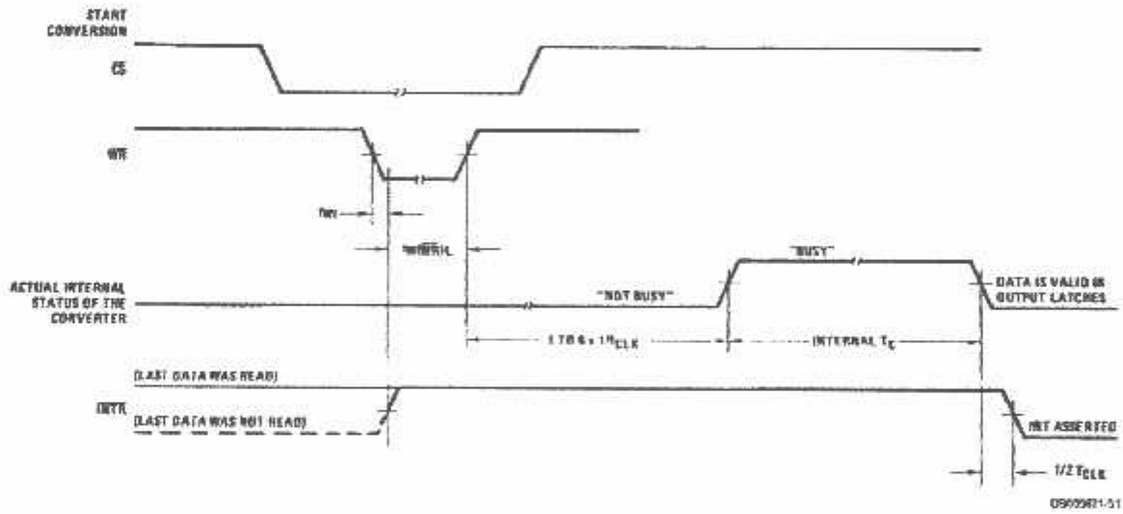


t_{0H}, C_L=10 pF



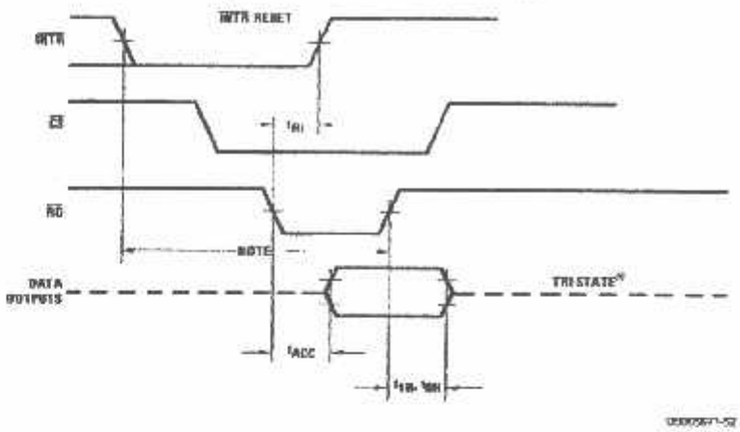
t_r=20 ns

Timing Diagrams (All timing is measured from the 50% voltage points)



Timing Diagrams (All timing is measured from the 50% voltage points) (Continued)

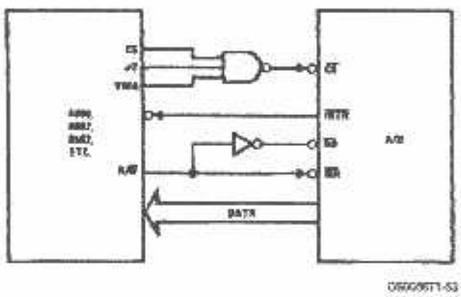
Output Enable and Reset with $\overline{INTR}$



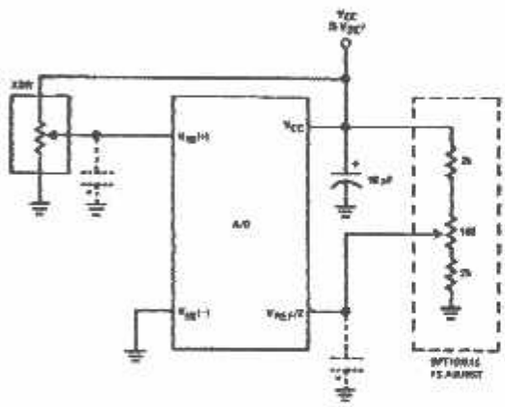
Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

Typical Applications

6800 Interface



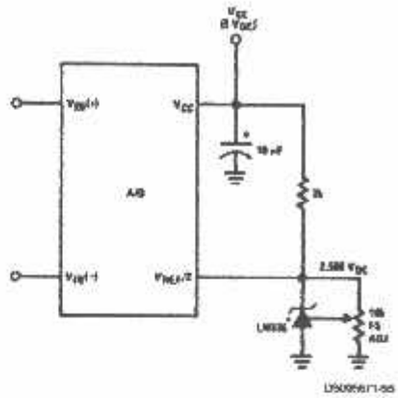
Ratiometeric with Full-Scale Adjust



Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

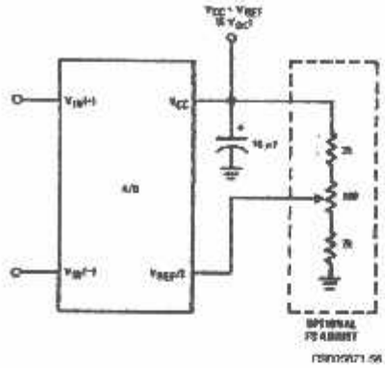
Typical Applications (Continued)

Absolute with a 2.500V Reference

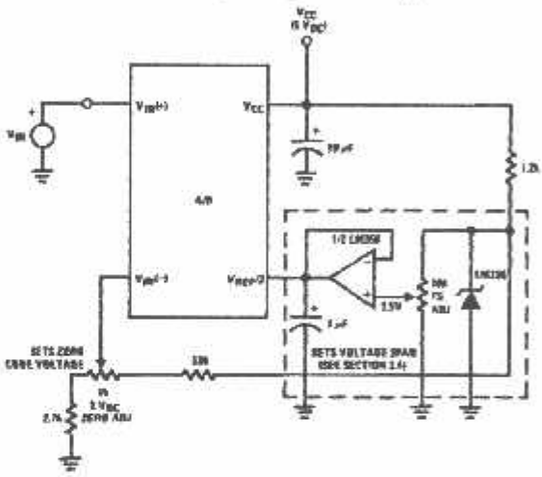


*For low power, see also LM385–2.5

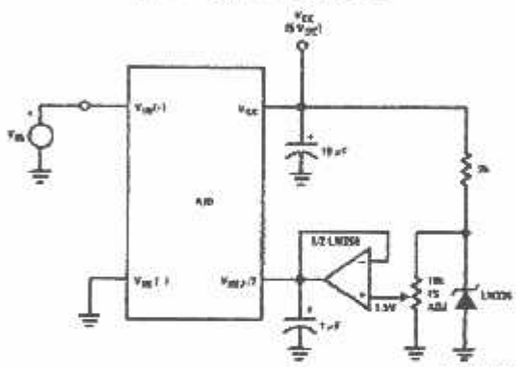
Absolute with a 5V Reference



Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V

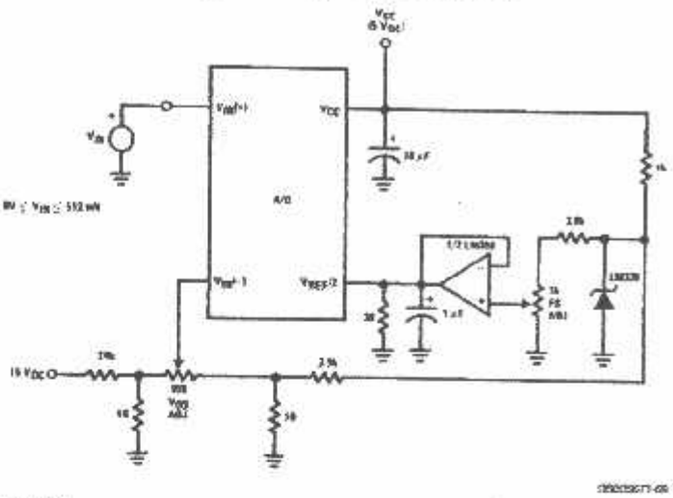


Span Adjust: 0V ≤ V_{IN} ≤ 3V



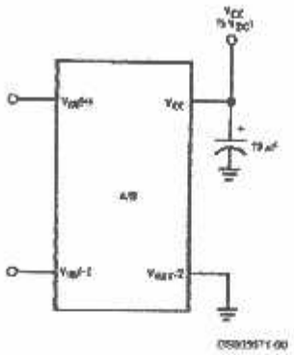
Typical Applications (Continued)

Directly Converting a Low-Level Signal



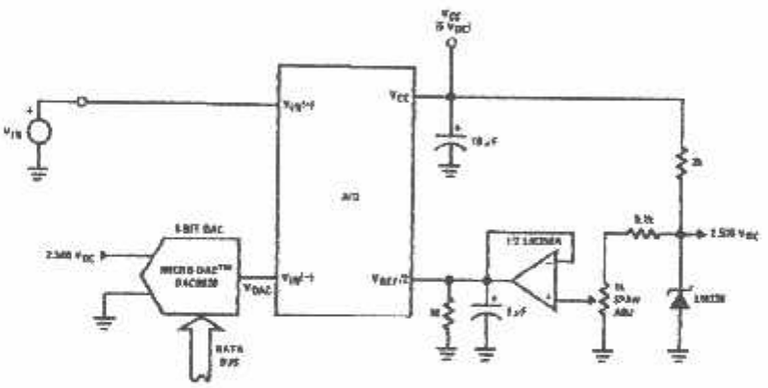
$V_{REF}/2 = 256$ mV

A µP Interfaced Comparator



For:
$V_{IN}(+) > V_{IN}(-)$
Output = FF_{HEX}
For:
$V_{IN}(+) < V_{IN}(-)$
Output = 00_{HEX}

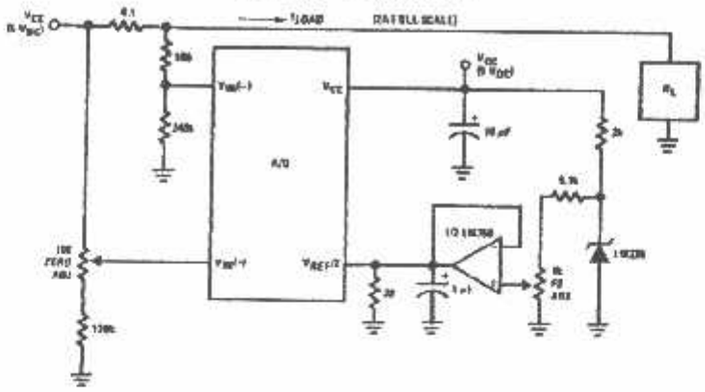
1 mV Resolution with µP Controlled Range



$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC} + 256\ mV)$
$0 \leq V_{DAC} < 2.5V$

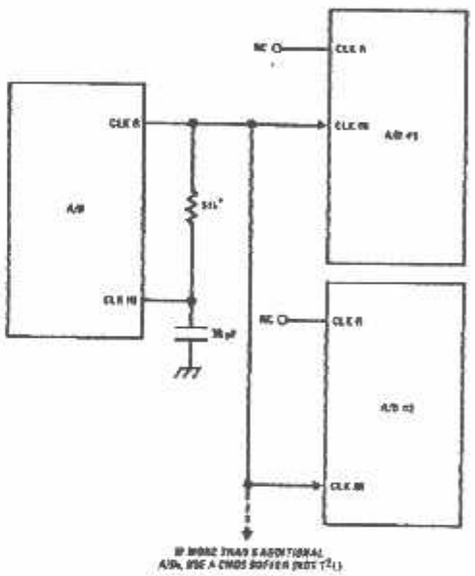
Typical Applications (Continued)

Digitizing a Current Flow



DS009871-62

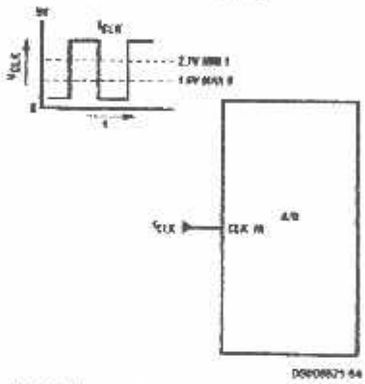
Self-Clocking Multiple A/Ds



DS009871-63

* Use a large R value to reduce loading at CLK R output.

External Clocking

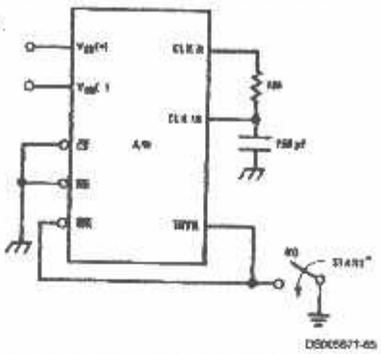


100 kHz≤f_{CLK}≤1460 kHz

DS009871-64

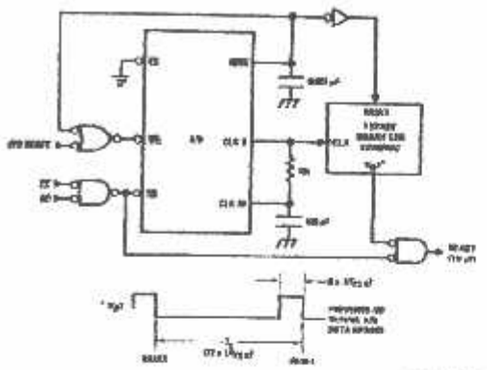
Typical Applications (Continued)

Self-Clocking in Free-Running Mode

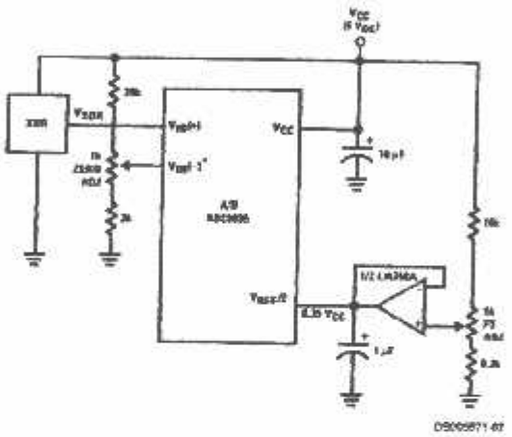


*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

µP Interface for Free-Running A/D

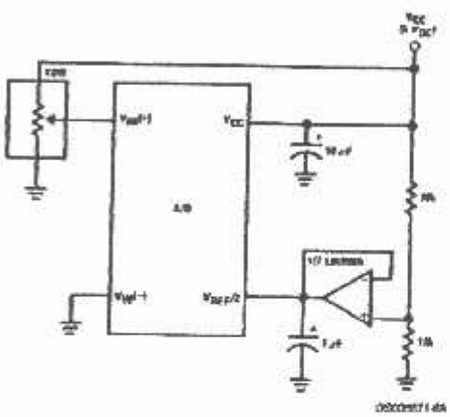


Operating with "Automotive" Ratiometric Transducers

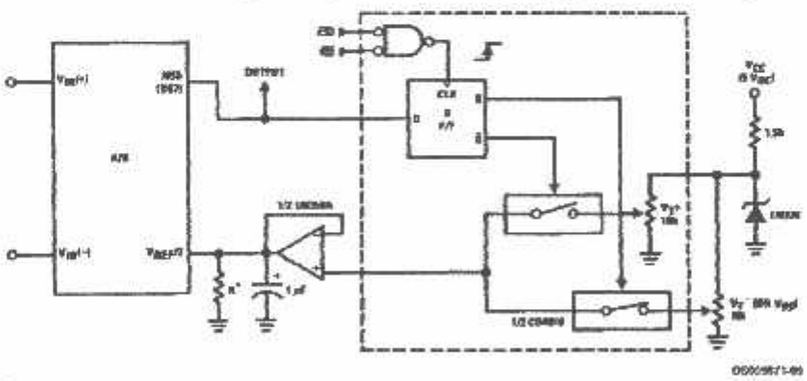


*$V_{IN}(-)=0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



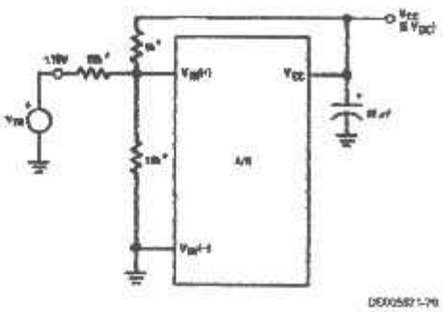
µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)



*See *Figure 6* to select R value
DB7="1" for $V_{IN}(+) \geq V_{IN}(-)+(V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

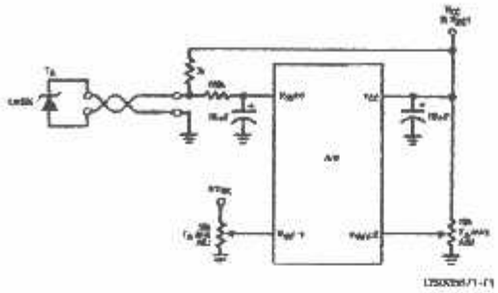
Typical Applications (Continued)

Handling ±10V Analog Inputs

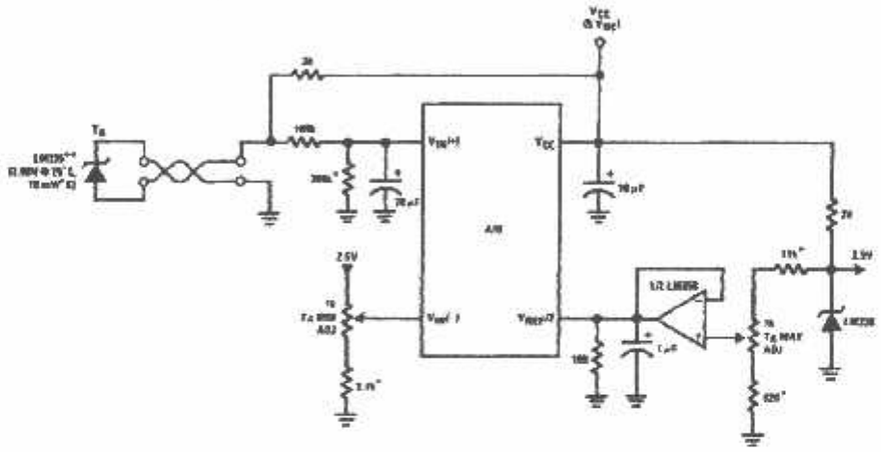


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, µP Interfaced, Temperature-to-Digital Converter



µP Interfaced Temperature-to-Digital Converter

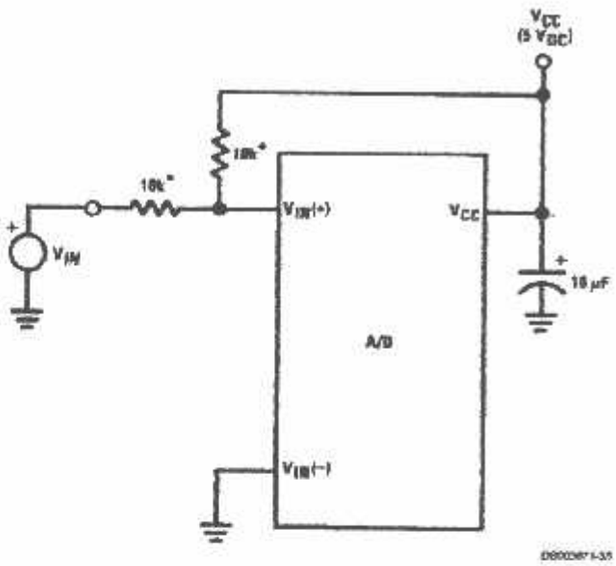


*Circuit values shown are for $0°C \leq T_A \leq +128°C$

**Can calibrate each sensor to allow easy replacement; then A/D can be calibrated with a pre-set input voltage.

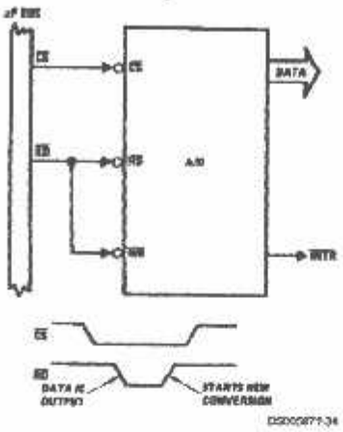
Typical Applications (Continued)

Handling ±5V Analog Inputs

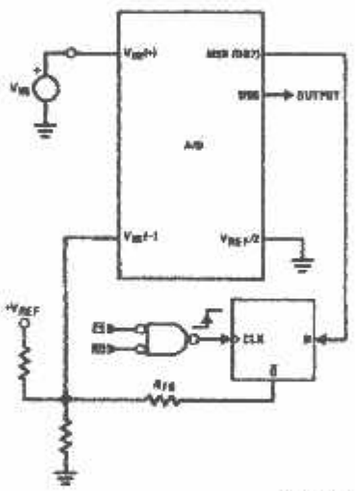


*Beckman Instruments 694-3-R10K resistor array

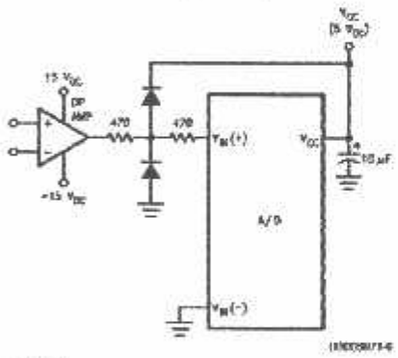
Read-Only Interface



µP Interfaced Comparator with Hysteresis



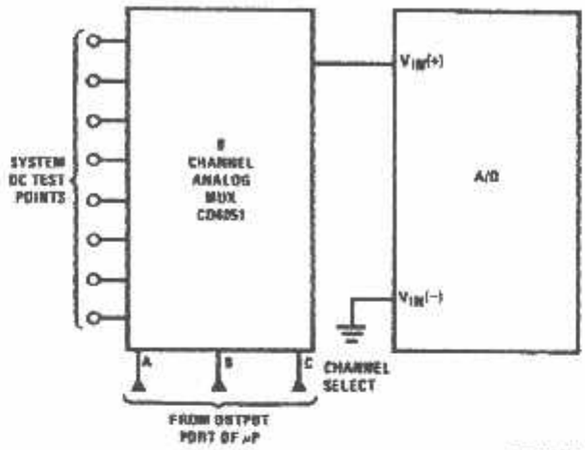
Protecting the Input



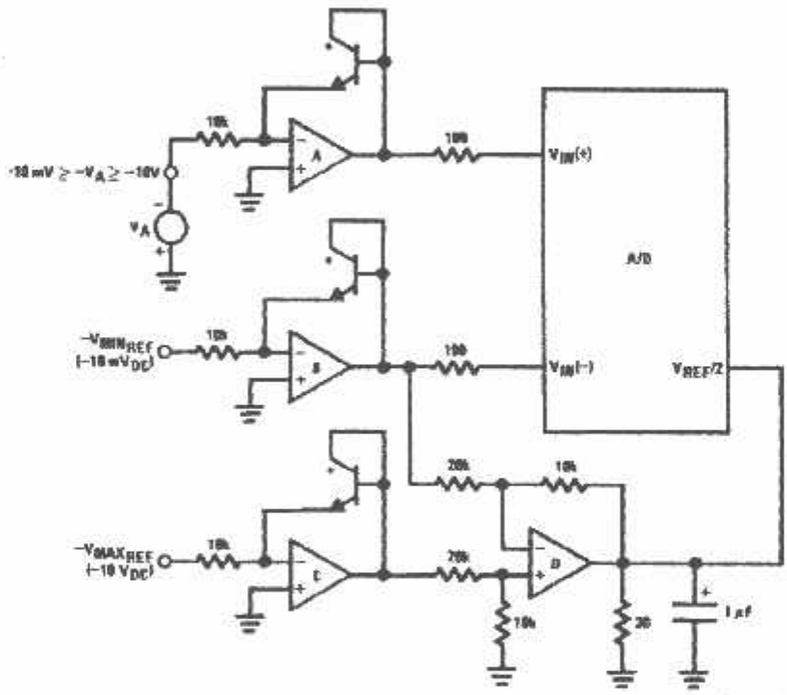
Diodes are 1N914

Typical Applications (Continued)

Analog Self-Test for a System



A Low-Cost, 3-Decade Logarithmic Converter

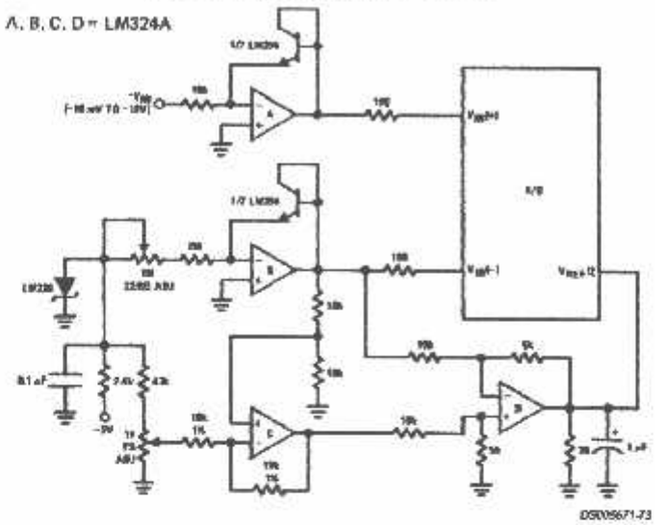


*LM389 transistors
A, B, C, D = LM324A quad op amp

Typical Applications (Continued)

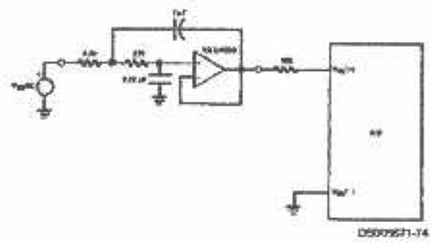
3-Decade Logarithmic A/D Converter

A, B, C, D = LM324A



DS005671-73

Noise Filtering the Analog Input



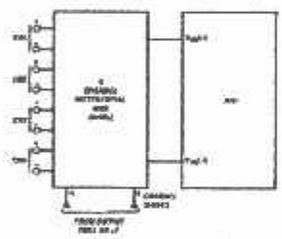
DS005671-74

f_C = 20 Hz.

Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter

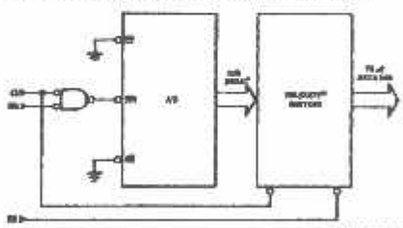
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs



DS005671-75

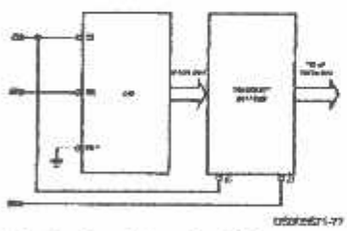
Output Buffers with A/D Data Enabled



DS005671-76

*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

Increasing Bus Drive and/or Reducing Time on Bus

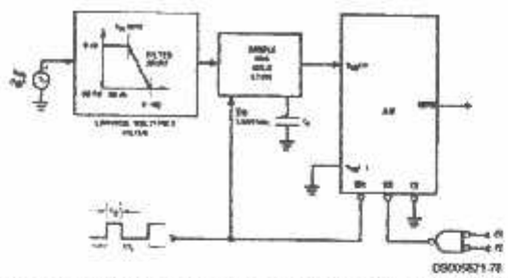


DS005671-77

*Allows output data to set-up at falling edge of $\overline{CS}$

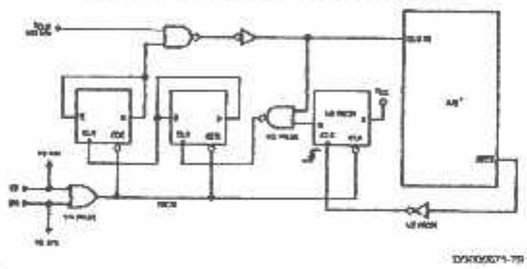
Typical Applications (Continued)

Sampling an AC Input Signal



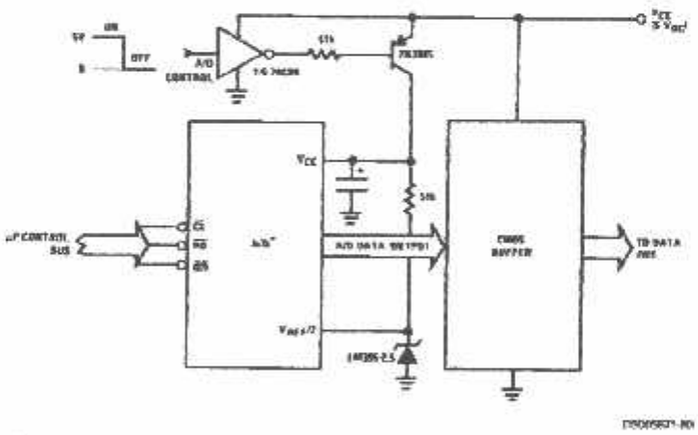
Note 11: Oversample whenever possible (keep $f_s > 2(f_{-60})$) to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.
Note 12: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



*Use ADC0801, 02, 03 or 05 for lowest power consumption.
Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.
Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend

Functional Description (Continued)

±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Figure 2 shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 3* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.

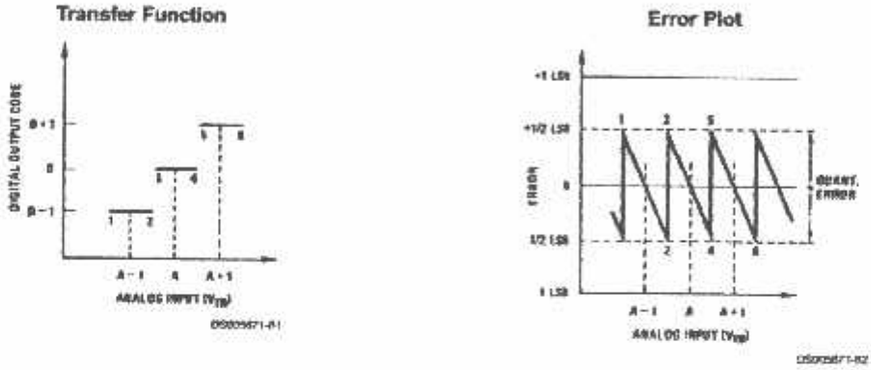


FIGURE 1. Clarifying the Error Specs of an A/D Converter Accuracy=±0 LSB: A Perfect A/D

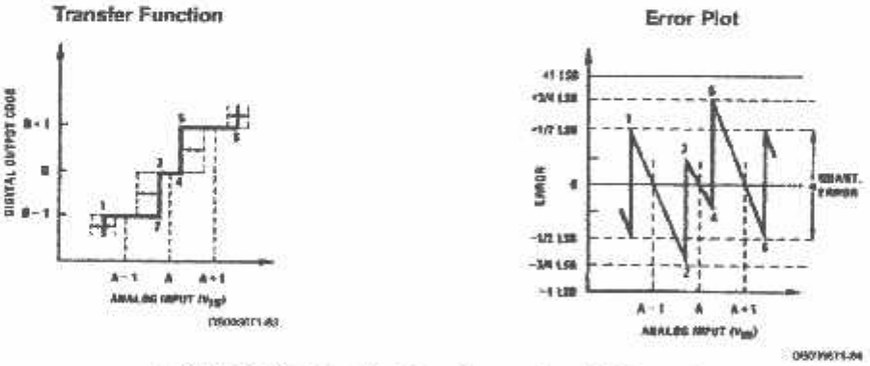


FIGURE 2. Clarifying the Error Specs of an A/D Converter Accuracy=±¼ LSB

Functional Description (Continued)

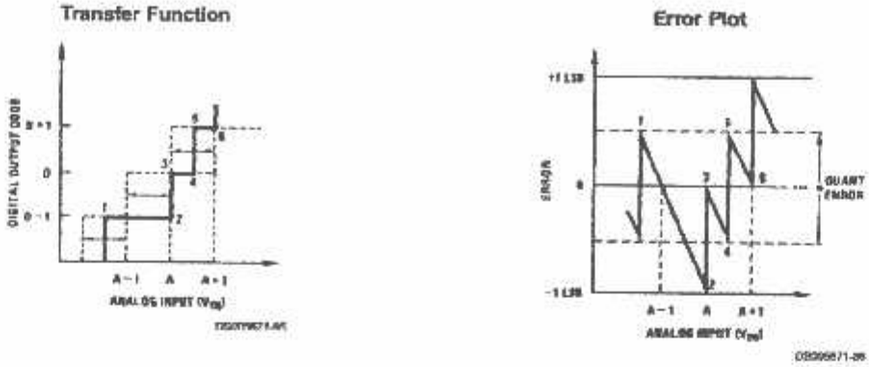


FIGURE 3. Clarifying the Error Specs of an A/D Converter
Accuracy=±½ LSB

2.0 FUNCTIONAL DESCRIPTION

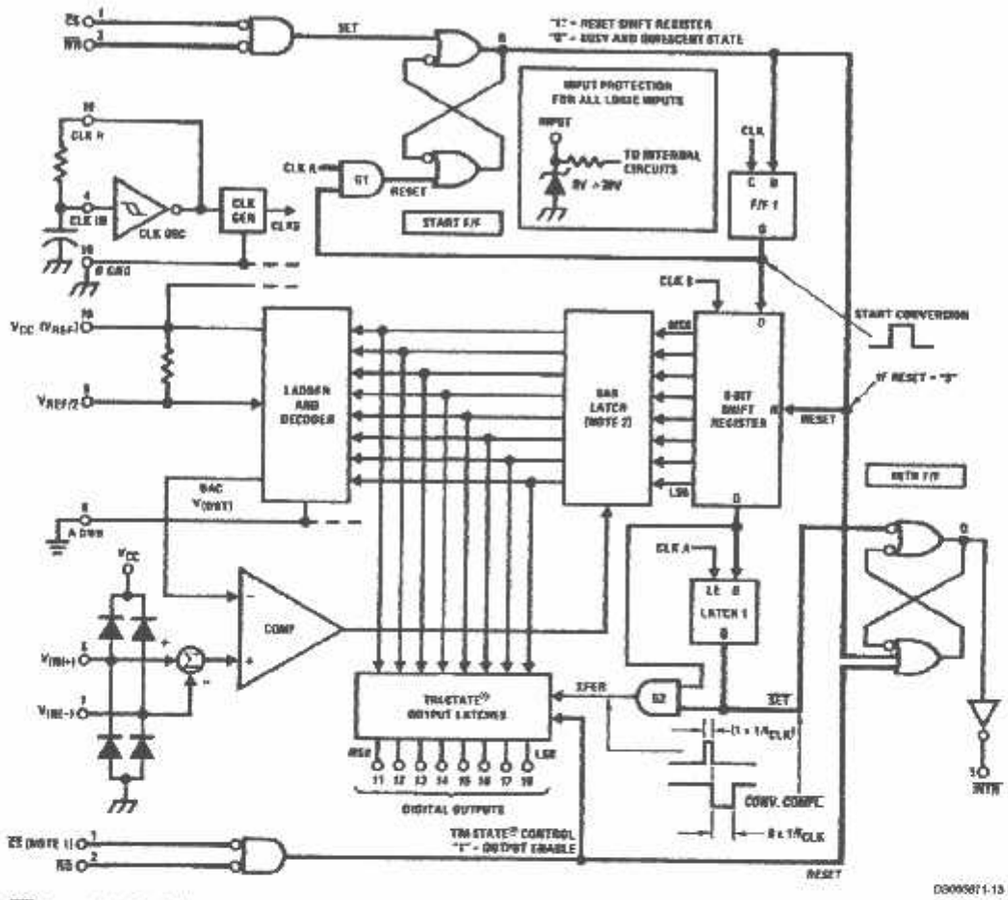
The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage $[V_{IN}(+) - V_{IN}(-)]$ to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ =0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 4*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

Functional Description (Continued)



D0005871-13

Note 13: $\overline{CS}$ shown twice for clarity.

Note 14: SAR = Successive Approximation Register.

FIGURE 4. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

Functional Description (Continued)

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right)$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)}$$

which gives

V_P=1.9V.

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

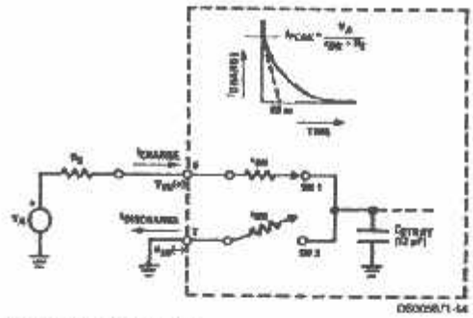
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3 1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 5*.



r_{ON} of SW 1 and SW 2 = 5 kΩ

$\tau = r_{ON} C_{STRAY} = 5\ k\Omega \times 12\ pF = 60\ ns$

FIGURE 5. Analog Input Impedance

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

Fault Mode

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of V_{CC}+50 mV, large input currents can flow through a parasitic diode to the V_{CC} pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the V_{CC} pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the V_{CC} voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 µA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 µF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long

Functional Description (Continued)

wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

2.3.4 Noise

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 6*.

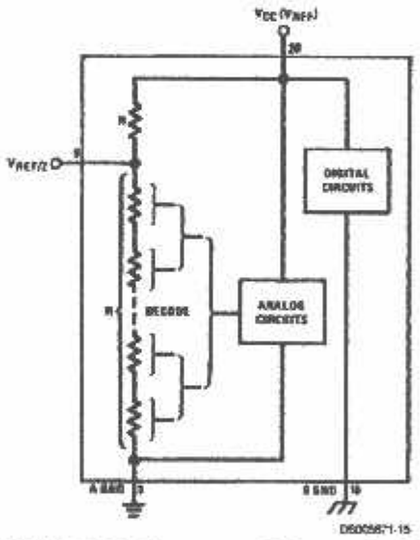


FIGURE 6. The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the V_{CC} supply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

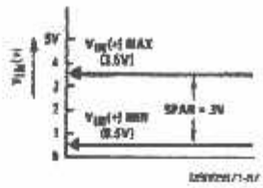
An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 7*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

2.4.2 Reference Accuracy Requirements

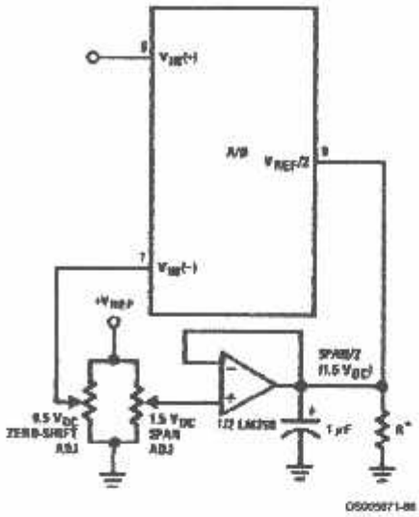
The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0^{\circ}C \leq T_A \leq +70^{\circ}C$. Other temperature range parts are also available.

Functional Description (Continued)



a) Analog Input Signal Example



*Add if $V_{REF}/2 \leq 1\ V_{DC}$ with LM358 to draw 3 mA to ground.

b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 3.5V (Digital Out=FF_{HEX})

FIGURE 7. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V_{IN} (−) input and applying a small magnitude positive voltage to the V_{IN} (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2$=2.500 V_{DC}).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB=analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\text{ fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX}=The high end of the analog input range

and

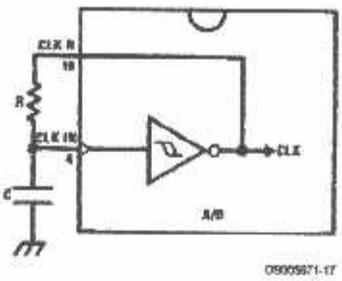
V_{MIN}=the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 8*.

Functional Description (Continued)



$$f_{CLK} \cong \frac{1}{1.1\ RC}$$

$R \cong 10\ k\Omega$

FIGURE 8. Self-Clocking the A/D

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 µF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 9*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120–1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). *Table 1* shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in *Table 1*, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

Functional Description (Continued)

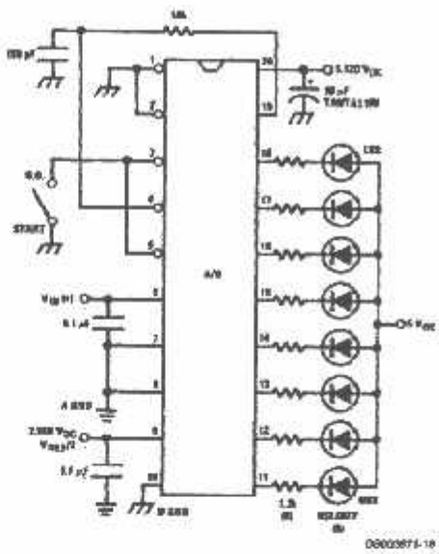


FIGURE 9. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A–C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 11*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 12*.

Functional Description (Continued)

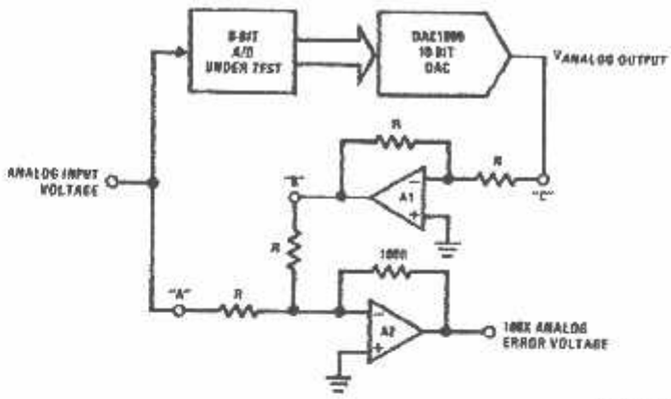


FIGURE 10. A/D Tester with Analog Error Output

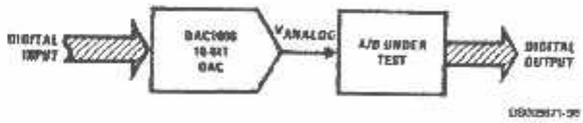


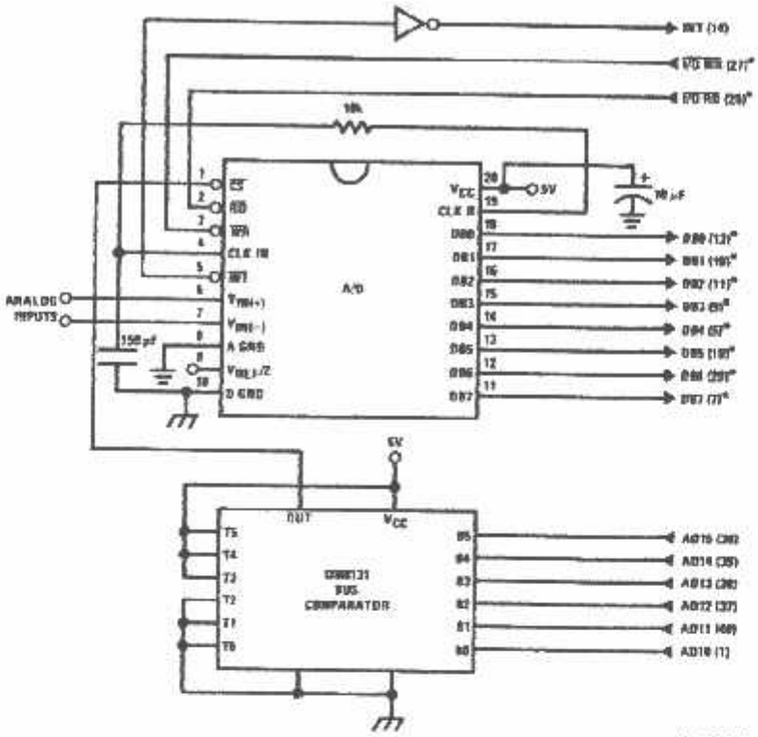
FIGURE 11. Basic "Digital" A/D Tester

TABLE 1. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY	FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2=2.560\ V_{DC}$	
		MS GROUP	LS GROUP	VMS GROUP (Note 15)	VLS GROUP (Note 15)
F	1 1 1 1	15/16	15/256	4.800	0.300
E	1 1 1 0	7/8	7/128	4.480	0.280
D	1 1 0 1	13/16	13/256	4.160	0.260
C	1 1 0 0	3/4	3/64	3.840	0.240
B	1 0 1 1	11/16	11/256	3.520	0.220
A	1 0 1 0	5/8	5/128	3.200	0.200
9	1 0 0 1	9/16	9/256	2.880	0.180
8	1 0 0 0	1/2	1/32	2.560	0.160
7	0 1 1 1	7/16	7/256	2.240	0.140
6	0 1 1 0	3/8	3/128	1.920	0.120
5	0 1 0 1	5/16	2/256	1.600	0.100
4	0 1 0 0	1/4	1/64	1.280	0.080
3	0 0 1 1	3/16	3/256	0.960	0.060
2	0 0 1 0	1/8	1/128	0.640	0.040
1	0 0 0 1	1/16	1/256	0.320	0.020
0	0 0 0 0			0	0

Note 15. Display Output=VMS Group + VLS Group

Functional Description (Continued)



Note 16: *Pin numbers for the DP8228 system controller, others are INS8080A.

Note 17: Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 12. ADC0801_INS8080A CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 12* ADC0801–INS8080A CPU INTERFACE

```
0038    C3 00 03    RST 7:      JMP     LD DATA
  •       •           •
  •       •           •
0100    21 00 02    START:      LXI H 0200H         ;HL pair will point to
                                                    ;data storage locations
0103    31 00 04    RETURN:     LXI SP 0400H        ;Initialize stack pointer (Note 1)
0106    7D                      MOV A, L            ;Test # of bytes entered
0107    FE 0F                   CPI 0F H            ;If # = 16. JMP to
0109    CA 13 01                JZ CONT             ;user program
010C    D3 E0                   OUT E0 H            ;Start A/D
010E    FB                      EI                  ;Enable interrupt
010F    00          LOOP:       NOP                 ;Loop until end of
0110    C3 0F 01                JMP LOOP            ;conversion
0113      •         CONT:         •
  •       •           •           •
  •       •           •           •
  •       •           •           •
  •       •           •           •
  •       •           •           •
  •       •           •           •
0300    DB E0       LD DATA:    IN E0 H             ;Load data into accumulator
0302    77                      MOV M, A            ;Store data
0303    23                      INX H               ;Increment storage pointer
0304    C3 03 01                JMP RETURN
```

05005871-69

Note 18: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 19: All address used were arbitrarily chosen.

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 12* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 13*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

Functional Description (Continued)

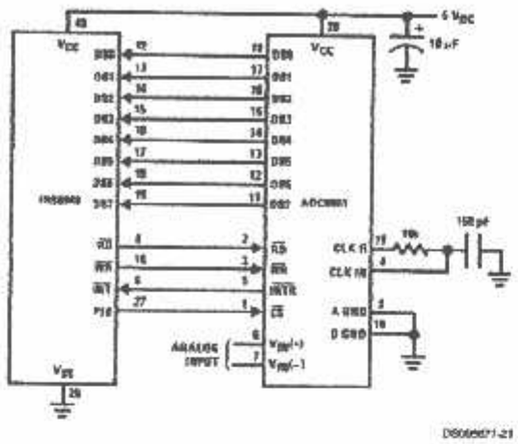


FIGURE 13. INS8048 Interface

SAMPLE PROGRAM FOR *Figure 13* INS8048 INTERFACE

```
04 10                    JMP     10H          ;Program starts at addr 10
                         ORG     3H
04 50                    JMP     50H          ;Interrupt jump vector
                         ORG     10H          ;Main program
99 FE                    ANL     P1, #0FEH    ;Chip select
81                       MOVX    A, @R1       ;Read in the 1st data
                                              ;to reset the intr
89 01          START:    ORL     P1, #1       ;Set port pin high
B8 20                    MOV     R0, #20H     ;Data address
B9 FF                    MOV     R1, #0FFH    ;Dummy address
BA 10                    MOV     R2, #10H     ;Counter for 16 bytes
23 FF          AGAIN:    MOV     A, #0FFH     ;Set ACC for intr loop
99 FE                    ANL     P1, #0FEH    ;Send CS (bit 0 of P1)
91                       MOVX    @R1, A       ;Send WR out
05                       EN      I            ;Enable interrupt
96 21          LOOP:     JNZ     LOOP         ;Wait for interrupt
EA 1B                    DJNZ    R2, AGAIN    ;If 16 bytes are read
00                       NOP                  ;go to user's program
00                       NOP
                         ORG     50H
81             INDATA:   MOVX    A, @R1       ;Input data, CS still low
A0                       MOV     @R0, A       ;Store in memory
18                       INC     R0           ;Increment storage counter
89 01                    ORL     P1, #1       ;Reset CS signal
27                       CLR     A            ;Clear ACC to get out of
93                       RETR                 ;the interrupt loop
```

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 14*.

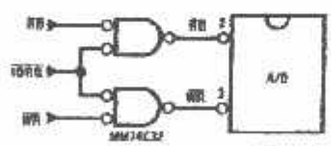


FIGURE 14. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to

Functional Description (Continued)

A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived form the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 15* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 16* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

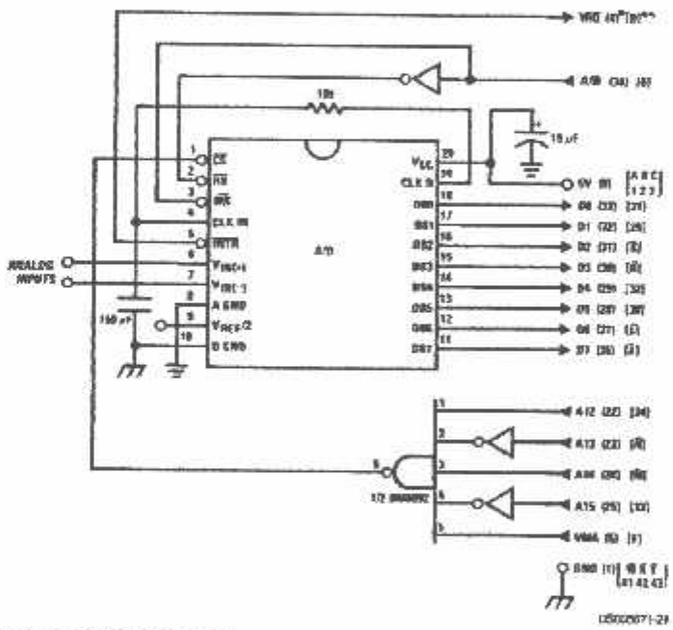
A sample interface program equivalent to the previous one is shown below *Figure 16*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 17*.



Note 20: Numbers in parentheses refer to MC6800 CPU pin out.

Note 21: Number or letters in brackets refer to standard M6800 system common bus code.

FIGURE 15. ADC0801-MC6800 CPU Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 15* ADC0801-MC6800 CPU INTERFACE

```
0010  DF 36     DATAIN  STX   TEMP2    ; Save contents of X
0012  CE 00 2C          LDX   #$002C   ; Upon IRQ low CPU
0015  FF FF F8          STX   $FFF8    ; jumps to 002C
0018  B7 50 00          STAA  $5000    ; Start ADC0801
001B  0E                CLI
001C  3E        CONVRT  WAI            ; Wait for interrupt
001D  DE 34             LDX   TEMP1
001F  8C 02 DF          CPX   #$02DF   ; Is final data stored?
0022  27 14             BEQ   ENDP
0024  B7 50 00          STAA  $5000    ; Restarts ADC0801
0027  08                INX
0028  DF 34             STX   TEMP1
002A  20 F0             BRA   CONVRT
002C  DE 34     INTRPT  LDX   TEMP1
002E  B6 50 00          LDAA  $5000    ; Read data
0031  A7 00             STAA  X        ; Store it at X
0033  3B                RTI
0034  02 00     TEMP1   FDB   $0200    ; Starting address for
                                       ; data storage
0036  00 00     TEMP2   FDB   $0000
0038  CE 02 00  ENDP    LDX   #$0200   ; Reinitialize TEMP1
003B  DF 34             STX   TEMP1
003D  DE 36             LDX   TEMP2
003F  39                RTS            ; Return from subroutine
                                       ; To user's program
```

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Note 22: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

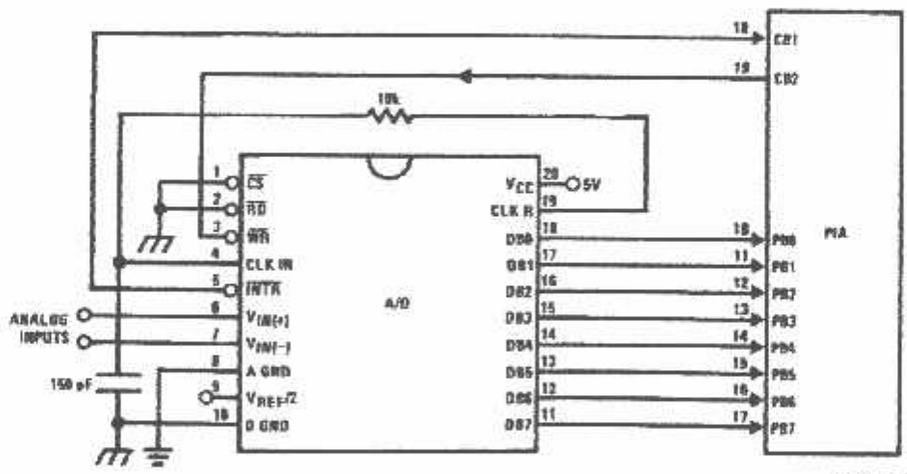

FIGURE 16. ADC0801–MC6820 PIA Interface

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 16* ADC0801–MC6820 PIA INTERFACE

```
0010  CE 00 38      DATAIN   LDX   #$0038    ; Upon IRQ low CPU
0013  FF FF F8               STX   $FFF8     ; jumps to 0038
0016  B6 80 06               LDAA  PIAORB    ; Clear possible IRQ flags
0019  4F                     CLRA
001A  B7 80 07               STAA  PIACRB
001D  B7 80 06               STAA  PIAORB    ; Set Port B as input
0020  0E                     CLI
0021  C6 34                  LDAB  #$34
0023  86 3D                  LDAA  #$3D
0025  F7 80 07      CONVRT   STAB  PIACRB    ; Starts ADC0801
0028  B7 80 07               STAA  PIACRB
002B  3E                     WAI             ; Wait for interrupt
002C  DE 40                  LDX   TEMP1
002E  8C 02 0F               CPX   #$020F    ; Is final data stored?
0031  27 0F                  BEQ   ENDP
0033  08                     INX
0034  DF 40                  STX   TEMP1
0036  20 ED                  BRA   CONVRT
0038  DE 40         INTRPT   LDX   TEMP1
003A  B6 80 06               LDAA  PIAORB    ; Read data in
003D  A7 00                  STAA  X         ; Store it at X
003F  3B                     RTI
0040  02 00          TEMP1   FDB   $0200     ; Starting address for
                                             ; data storage
0042  CE 02 00       ENDP    LDX   #$0200    ; Reinitialize TEMP1
0045  DF 40                  STX   TEMP1
0047  39                    RTS             ; Return from subroutine
                     PIAORB  EQU   $8006     ; To user's program
                     PIACRB  EQU   $8007
```

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The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

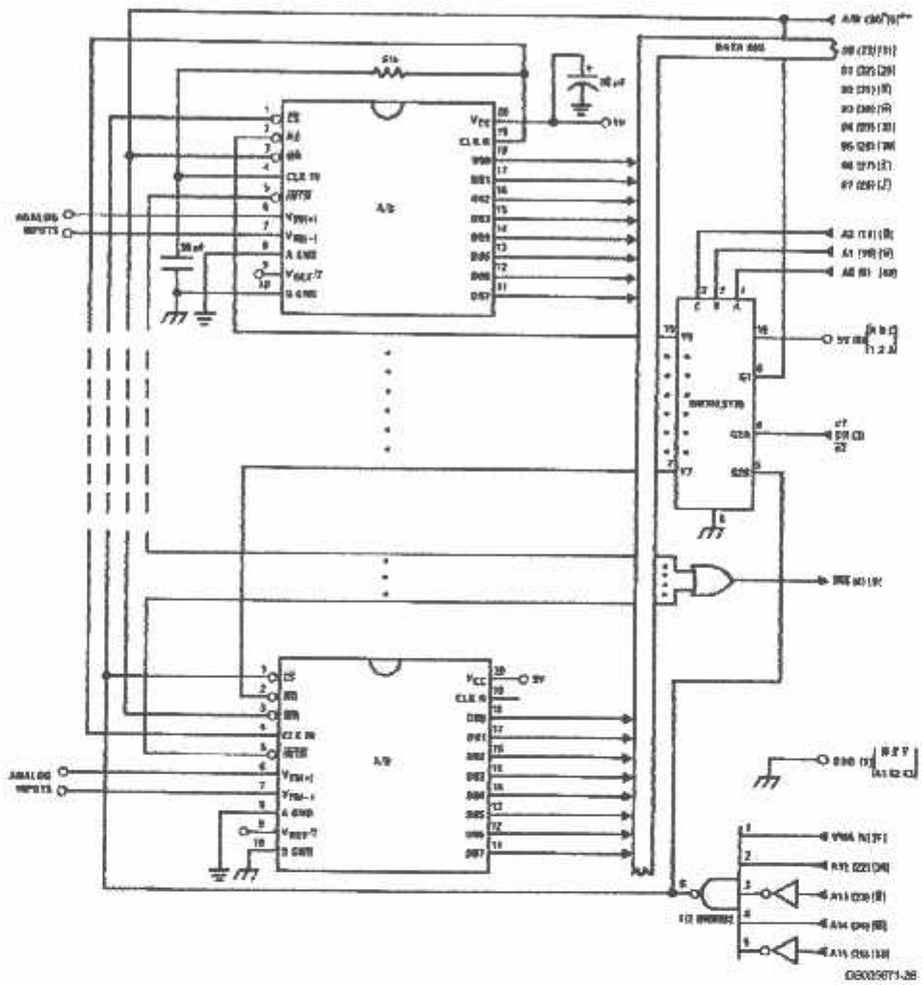
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

Functional Description (Continued)



Note 23: Numbers in parentheses refer to MC6800 CPU pin out.

Note 24: Numbers or letters in brackets refer to standard M6800 system common bus code.

FIGURE 17. Interfacing Multiple A/Ds in an MC6800 System

Functional Description (Continued)

SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0010	DF 44	DATAIN	STX	TEMP	; Save Contents of X
0012	CE 00 2A		LDX	#$002A	; Upon $\overline{IRQ}$ LOW CPU
0015	FF FF F8		STX	$FFF8	; Jumps to 002A
0018	B7 50 00		STAA	$5000	; Starts all A/D's
001B	0E		CLI		
001C	3E		WAI		; Wait for interrupt
001D	CE 50 00		LDX	#$5000	
0020	DF 40		STX	INDEX1	; Reset both INDEX
0022	CE 02 00		LDX	#$0200	; 1 and 2 to starting
0025	DF 42		STX	INDEX2	; addresses
0027	DE 44		LDX	TEMP	
0029	39		RTS		; Return from subroutine
002A	DE 40	INTRPT	LDX	INDEX1	; INDEX1 → X
002C	A6 00		LDAA	X	; Read data in from A/D at X
002E	08		INX		; Increment X by one
002F	DF 40		STX	INDEX1	; X → INDEX1
0031	DE 42		LDX	INDEX2	; INDEX2 → X

SAMPLE PROGRAM FOR *Figure 17* INTERFACING MULTIPLE A/D's IN AN MC6800 SYSTEM

ADDRESS	HEX CODE		MNEMONICS		COMMENTS
0033	A7 00		STAA	X	; Store data at X
0035	8C 02 07		CPX	#$0207	; Have all A/D's been read?
0038	27 05		BEQ	RETURN	; Yes: branch to RETURN
003A	08		INX		; No: increment X by one
003B	DF 42		STX	INDEX2	; X → INDEX2
003D	20 EB		BRA	INTRPT	; Branch to 002A
003F	3B	RETURN	RTI		
0040	50 00	INDEX1	FDB	$5000	; Starting address for A/D
0042	02 00	INDEX2	FDB	$0200	; Starting address for data storage
0044	00 00	TEMP	FDB	$0000	

Note 25: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 18* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 µV for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

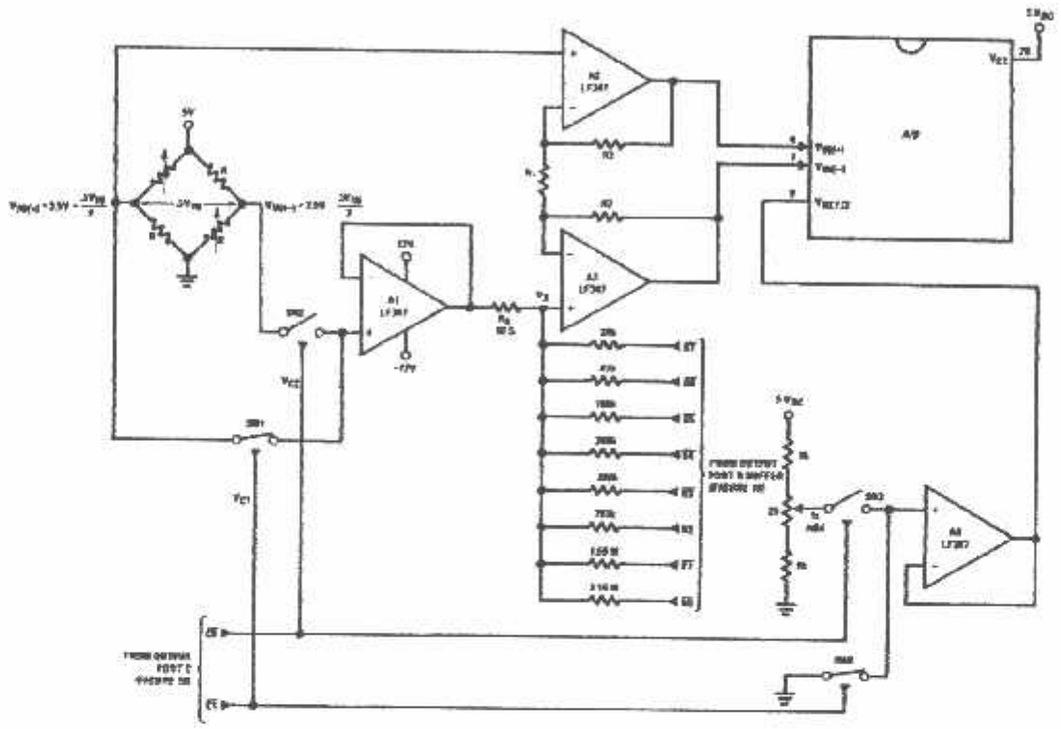
where I_X is the current through resistor R_X. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 19*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at V_x increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on

Functional Description (Continued)

any output of Port B will source current into node V_X thus raising the voltage at V_X and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node V_X and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, V_X can move ±12 mV with a resolution of 50 µV, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



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Note 26: R2 = 49.5 R1

Note 27: Switches are LMC13334 CMOS analog switches.

Note 28: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 18. Gain of 100 Differential Transducer Preamp

Functional Description (Continued)

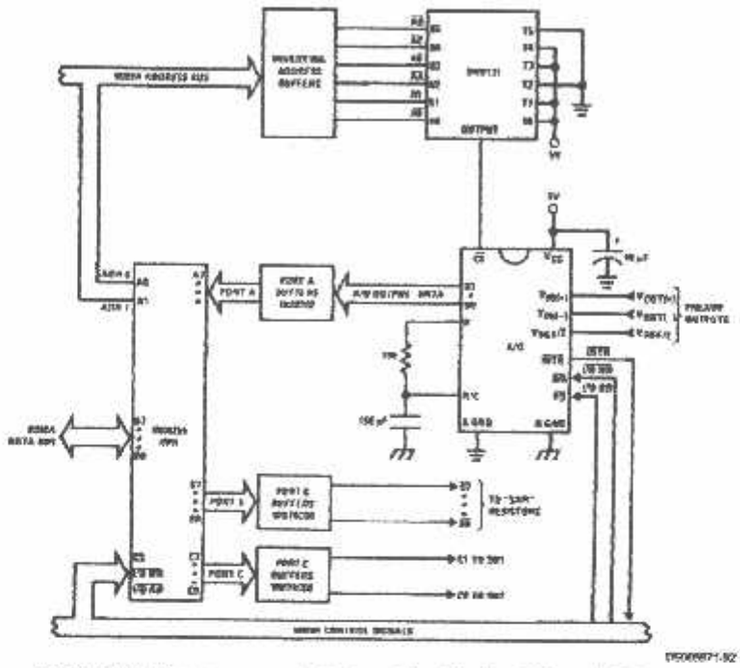

FIGURE 19. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in *Figure 20*. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull V_X more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make V_X more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 21*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 22* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion (INTR asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

Functional Description (Continued)

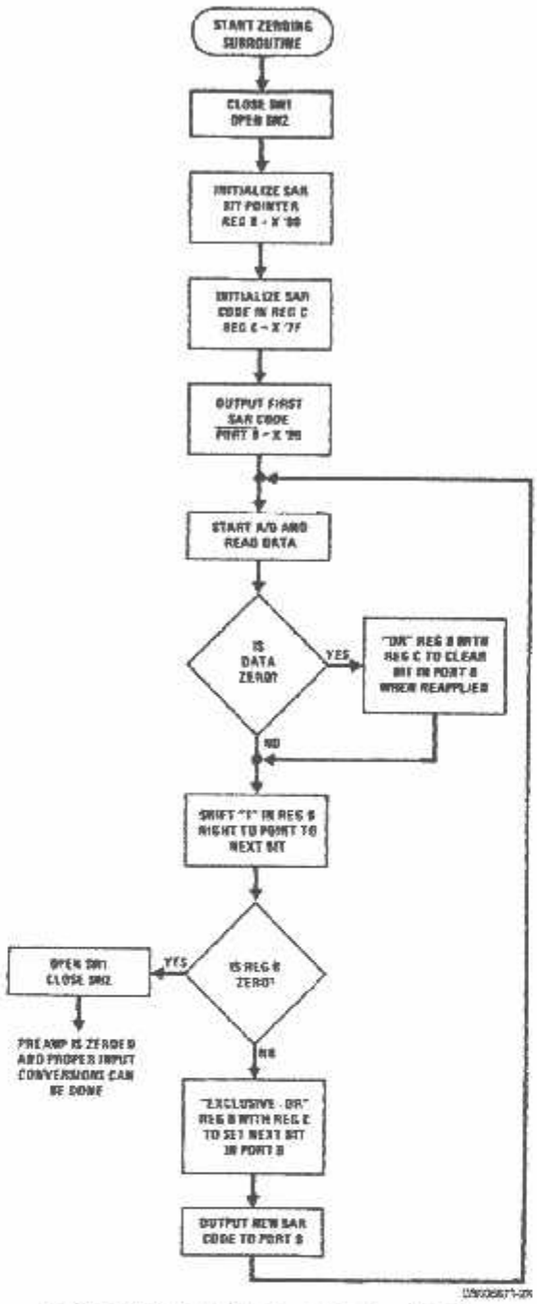

FIGURE 20. Flow Chart for Auto-Zero Routine

Functional Description (Continued)

```
3D00  3E90    MVI 90
3D02  D3E7    Out Control Port          ;Program PPI
3D04  2601    MVI H 01      Auto-Zero Subroutine
3D06  7C      MOV A,H
3D07  D3E6    OUT C                    ;Close SW1 open SW2
3D09  0680    MVI B 80                 ;Initialize SAR bit pointer
3D0B  3E7F    MVI A 7F                 ;Initialize SAR code
3D0D  4F      MOV C,A       Return
3D0E  D3E5    OUT B                    ;Port B = SAR code
3D10  31AA3D  LXI SP 3DAA   Start      ;Dimension stack pointer
3D13  D3E4    OUT A                    ;Start A/D
3D15  FB      IE
3D16  00      NOP           Loop       ;Loop until INT asserted
3D17  C3163D  JMP Loop
3D1A  7A      MOV A,D       Auto-Zero
3D1B  C600    ADI 00
3D1D  CA2D3D  JZ Set C                 ;Test A/D output data for zero
3D20  78      MOV A,B       Shift B
3D21  F600    ORI 00                   ;Clear carry
3D23  1F      RAR                      ;Shift "1" in B right one place
3D24  FE00    CPI 00                   ;Is B zero? If yes last
3D26  CA373D  JZ Done                  ;approximation has been made
3D29  47      MOV B,A
3D2A  C3333D  JMP New C
3D2D  79      MOV A,C       Set C
3D2E  B0      ORA B                    ;Set bit in C that is in same
3D2F  4F      MOV C,A                  ;position as "1" in B
3D30  C3203D  JMP Shift B
3D33  A9      XRA C         New C      ;Clear bit in C that is in
3D34  C30D3D  JMP Return               ;Same position as "1" in B
3D37  47      MOV B,A       Done       ;then output new SAR code.
3D38  7C      MOV A,H                  ;Open SW1, close SW2 then
3D39  EE03    XRI 03                   ;proceed with program. Preamp
3D3B  D3E6    OUT C                    ;is now zeroed.
3D3D          •             Normal
              •
              •
              Program for processing
              proper data values
3C3D  DBE4    IN A          Read A/D Subroutine   ;Read A/D data
3C3F  EEFF    XRI FF                   ;Invert data
3C41  57      MOV D,A
3C42  78      MOV A,B                  ;Is B Reg = 0? If not stay
3C43  E6FF    ANI FF                   ;in auto zero subroutine
3C45  C21A3D  JNZ Auto-Zero
3C48  C33D3D  JMP Normal
```

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Note 29: All numerical values are hexadecimal representations.

FIGURE 21. Software for Auto-Zeroed Differential A/D

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

- It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.
- The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.
- A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.
- The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.
- The peripherals of concern are mapped into I/O space with the following port assignments:

Functional Description (Continued)

HEX PORT ADDRESS	PERIPHERAL
00	MM74C374 8-bit flip-flop
01	A/D 1
02	A/D 2
03	A/D 3
04	A/D 4
05	A/D 5
06	A/D 6
07	A/D 7

This port address also serves as the A/D identifying word in the program.

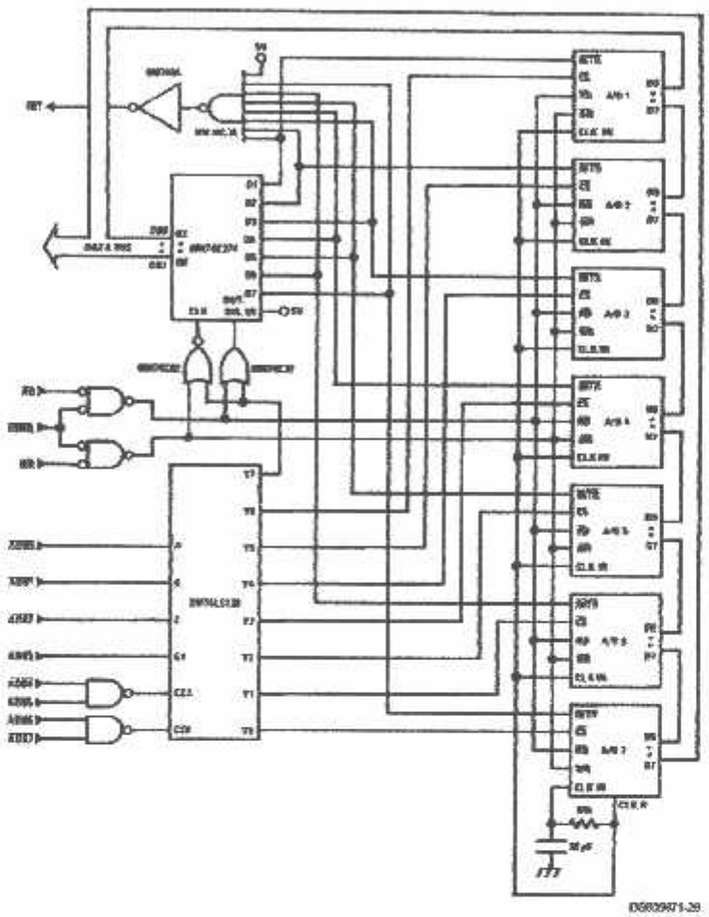


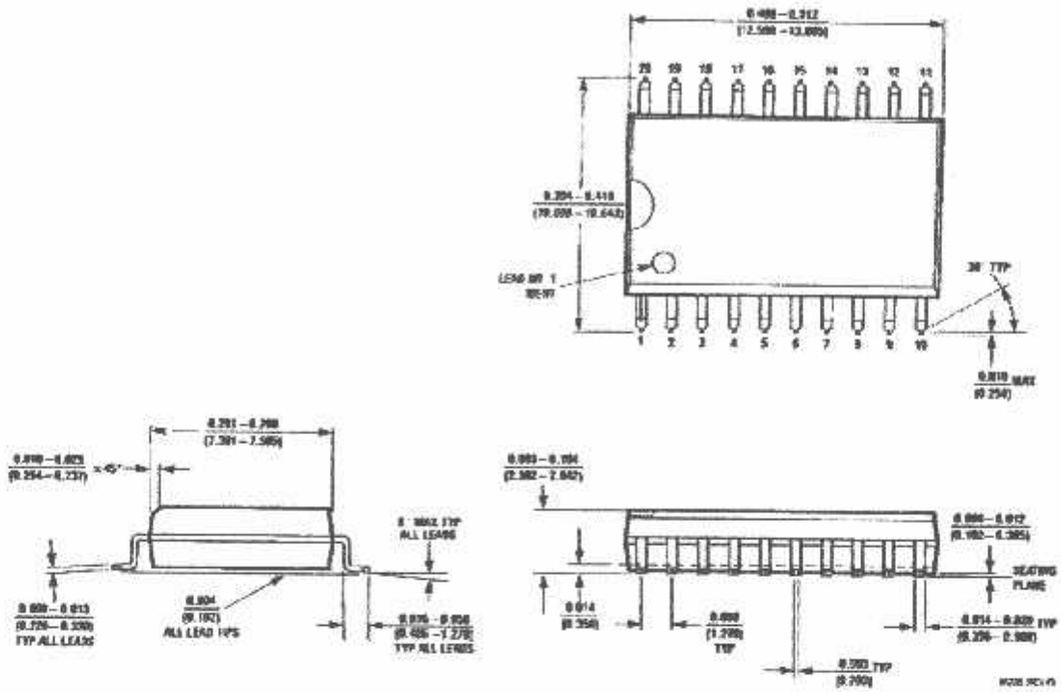
FIGURE 22. Multiple A/Ds with Z-80 Type Microprocessor

Functional Description (Continued)

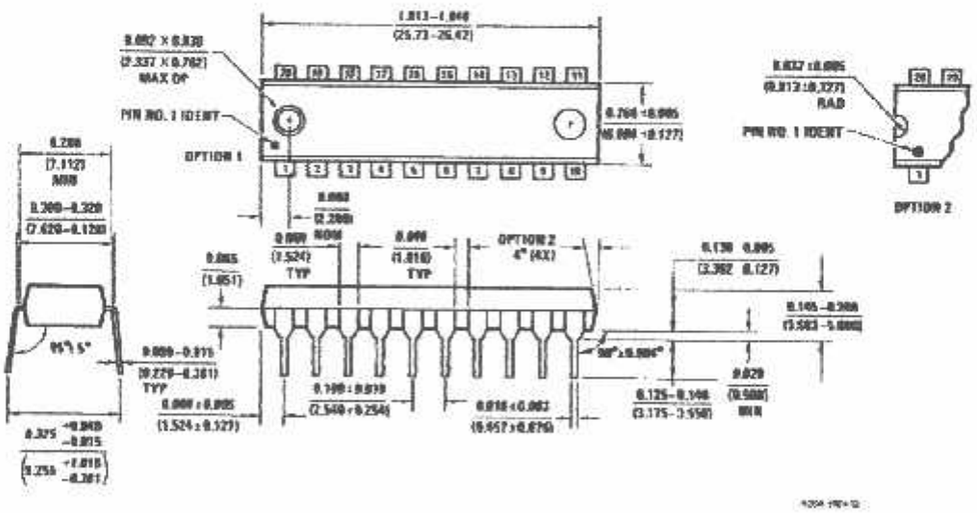
INTERRUPT SERVICING SUBROUTINE

LOC	OBJ CODE		SOURCE STATEMENT	COMMENT
0038	E5		PUSH HL	;Save contents of all registers affected by
0039	C5		PUSH BC	;this subroutine.
003A	F5		PUSH AF	;Assumed INT mode 1 earlier set.
003B	21 00 3E		LD (HL),X3E00	;Initialize memory pointer where data will be stored.
003E	0E 01		LD C, X01	;C register will be port ADDR of A/D converters.
0040	D300		OUT X00, A	;Load peripheral status word into 8-bit latch.
0042	DB00		IN A, X00	;Load status word into accumulator.
0044	47		LD B,A	;Save the status word.
0045	79	TEST	LD A,C	;Test to see if the status of all A/D's have
0046	FE 08		CP, X08	;been checked. If so, exit subroutine
0048	CA 60 00		JPZ, DONE	
004B	78		LD A,B	;Test a single bit in status word by looking for
004C	1F		RRA	;a "1" to be rotated into the CARRY (an $\overline{INT}$
004D	47		LD B,A	;is loaded as a "1"). If CARRY is set then load
004E	DA 5500		JPC, LOAD	;contents of A/D at port ADDR in C register.
0051	0C	NEXT	INC C	;If CARRY is not set, increment C register to point
0052	C3 4600		JP,TEST	;to next A/D, then test next bit in status word.
0055	ED 78	LOAD	IN A, (C)	;Read data from interrupting A/D and invert
0057	EE FF		XOR FF	;the data.
0059	77		LD (HL),A	;Store the data
005A	2C		INC L	
005B	71		LD (HL),C	;Store A/D identifier (A/D port ADDR).
005C	2C		INC L	
005D	C3 51 00		JP,NEXT	;Test next bit in status word.
0060	F1	DONE	POP AF	;Re-establish all registers as they were
0061	C1		POP BC	;before the interrupt.
0062	E1		POP HL	
0063	C9		RET	;Return to original program

Physical Dimensions inches (millimeters) unless otherwise noted



SO Package (M)
Order Number ADC0802LCWM or ADC0804LCWM
NS Package Number M20B



Molded Dual-In-Line Package (N)
Order Number ADC0801LCN, ADC0802LCN,
ADC0803LCN, ADC0804LCN or ADC0805LCN
NS Package Number N20A

Notes

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Features

- Compatible with MCS®-51 Products
- 8K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)
- Green (Pb/Halide-free) Packaging Option

8-bit Microcontroller with 8K Bytes In-System Programmable Flash

AT89S52

1. Description

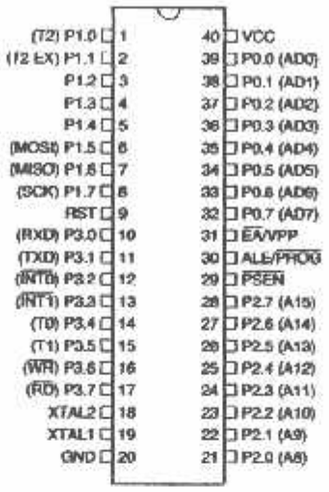
The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

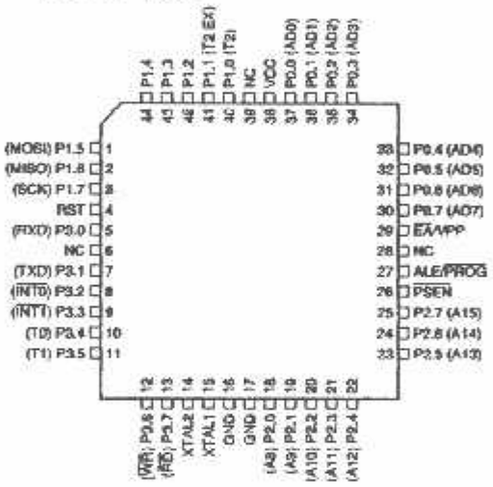
1919C–MICRO–3/05

2. Pin Configurations

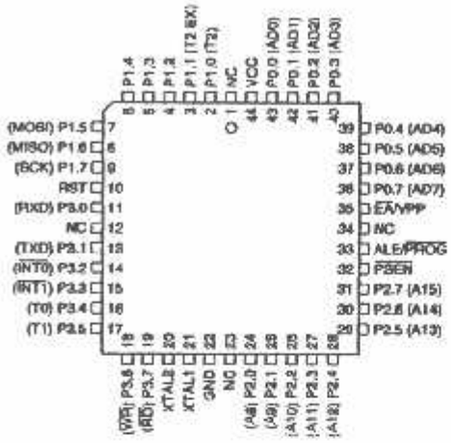
2.1 40-lead PDIP



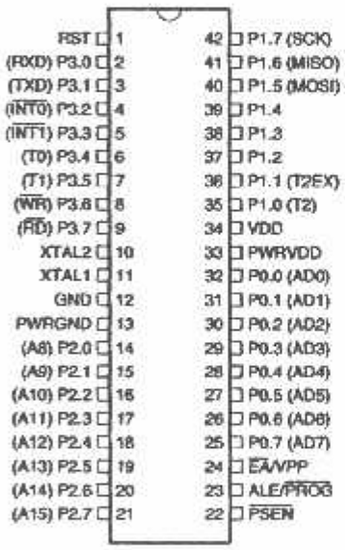
2.2 44-lead TQFP



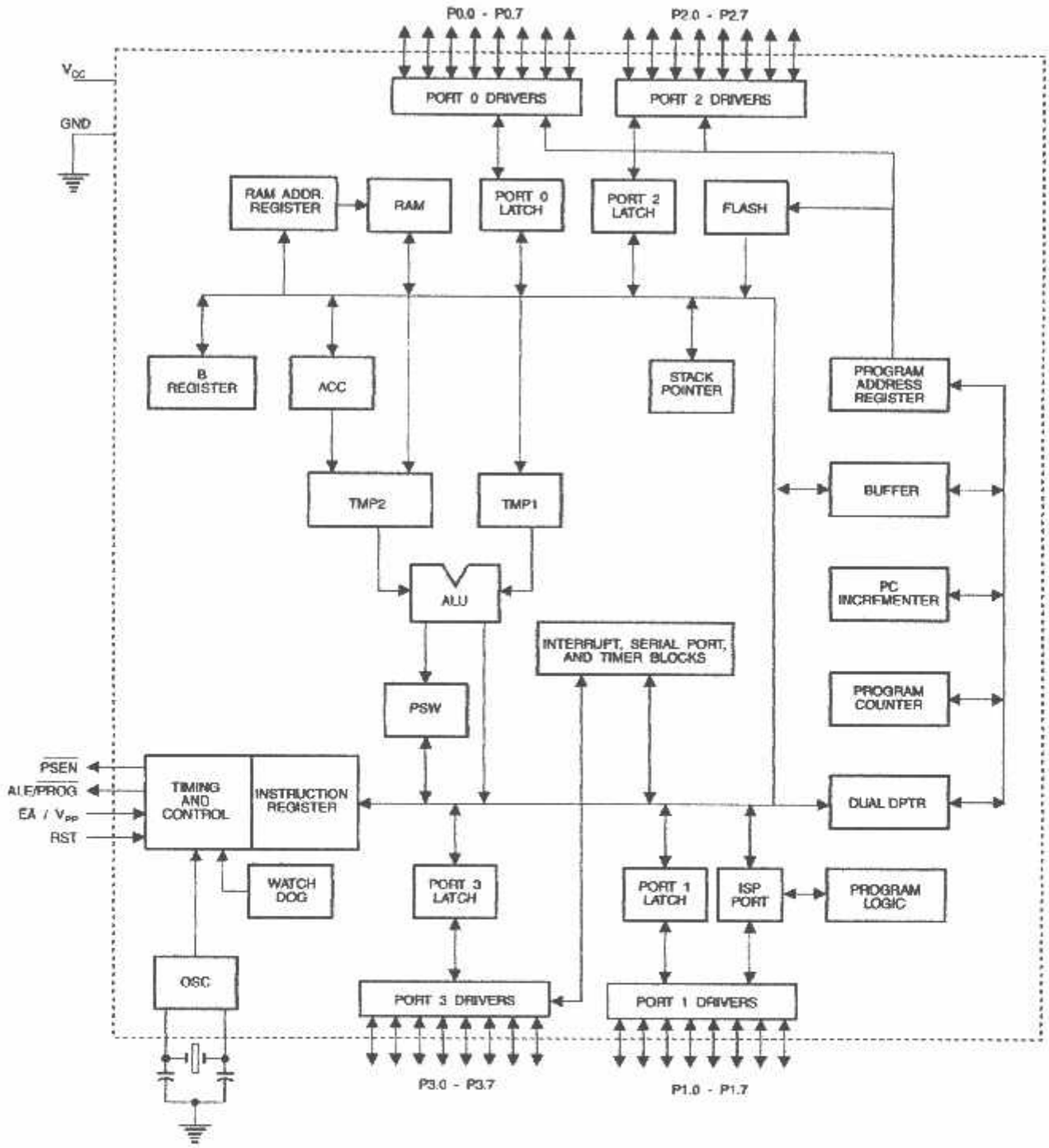
2.3 44-lead PLCC



2.4 42-lead PDIP



3. Block Diagram



4. Pin Description

4.1 VCC

Supply voltage.

4.2 GND

Ground.

4.3 Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification.**

4.4 Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

4.5 Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

4.6 Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

4.7 RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives high for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

4.8 ALE/$\overline{PROG}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

4.9 $\overline{\text{PSEN}}$

Program Store Enable ($\overline{\text{PSEN}}$) is the read strobe to external program memory.

When the AT89S52 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

4.10 $\overline{\text{EA}}$/VPP

External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

4.11 XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

4.12 XTAL2

Output from the inverting oscillator amplifier.

5. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 5-2) and T2MOD (shown in Table 10-2) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 5-1. AT89S52 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

Table 5-2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 5-3. AUXR: Auxiliary Register

AUXR — Address = 8EH — Reset Value = XXX00XX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	WDIDLE	DISRTO	–	–	DISALE

– Reserved for future expansion

DISALE Disable/Enable ALE

DISALE	Operating Mode
0	ALE is emitted at a constant rate of 1/6 the oscillator frequency
1	ALE is active only during a MOVX or MOVC instruction

DISRTO Disable/Enable Reset out

DISRTO	
0	Reset pin is driven High after WDT times out
1	Reset pin is input only

WDIDLE Disable/Enable WDT in IDLE mode

WDIDLE	
0	WDT continues to count in IDLE mode
1	WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 5-4. AUXR1: Auxiliary Register 1

AUXR1 — Address = A2H — Reset Value = XXXXXXX0B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	DPS

– Reserved for future expansion

DPS Data Pointer Register Select

DPS	
0	Selects DPTR Registers DP0L, DP0H
1	Selects DPTR Registers DP1L, DP1H

6. Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

6.1 Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S52, if $\overline{EA}$ is connected to V_{CC}, program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are to external memory.

6.2 Data Memory

The AT89S52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

7. Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

7.1 Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When

WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

7.2 WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S52 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S52 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

8. UART

The UART in the AT89S52 operates the same way as the UART in the AT89C51 and AT89C52. For further information on the UART operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

9. Timer 0 and 1

Timer 0 and Timer 1 in the AT89S52 operate the same way as Timer 0 and Timer 1 in the AT89C51 and AT89C52. For further information on the timers' operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

10. Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 5-2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 10-1. Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Table 10-1. Timer 2 Operating Modes

RCLK +TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

10.1 Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 10-1.

10.2 Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 10-2). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 10-1. Timer in Capture Mode

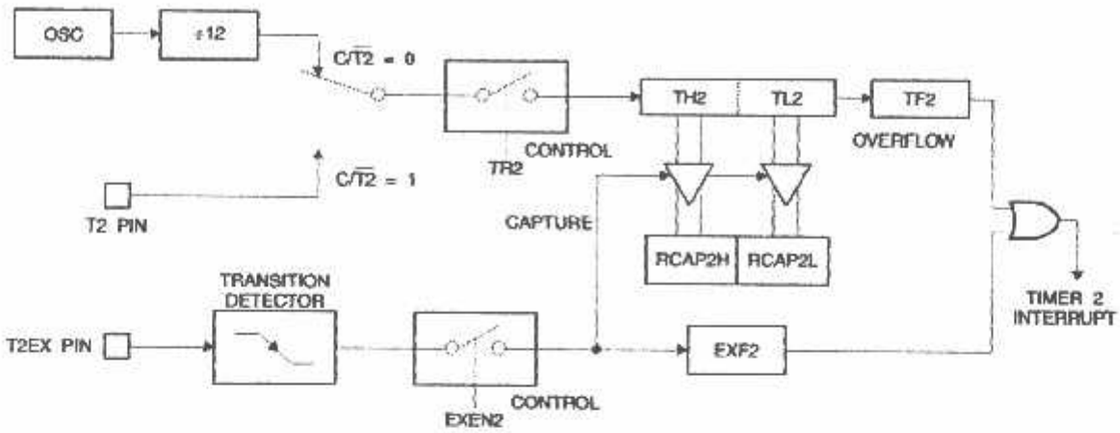


Table 10-2. T2MOD – Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

Bit	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	T2OE	DCEN

Symbol	Function
–	Not implemented, reserved for future
T2OE	Timer 2 Output Enable bit
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter

Figure 10-2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in Timer in Capture ModeRCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 10-2. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 10-2. Timer 2 Auto Reload Mode (DCEN = 0)

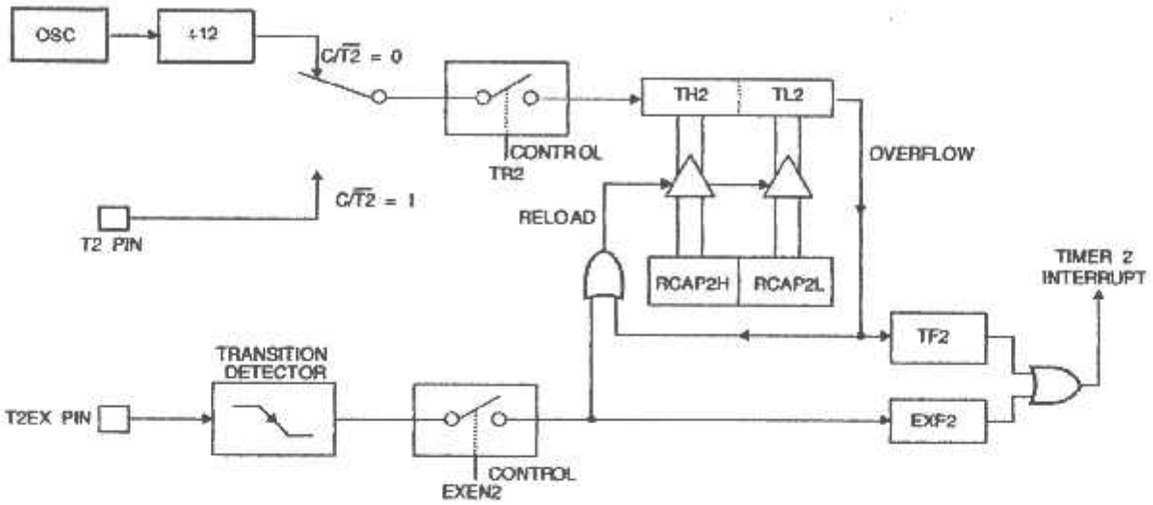
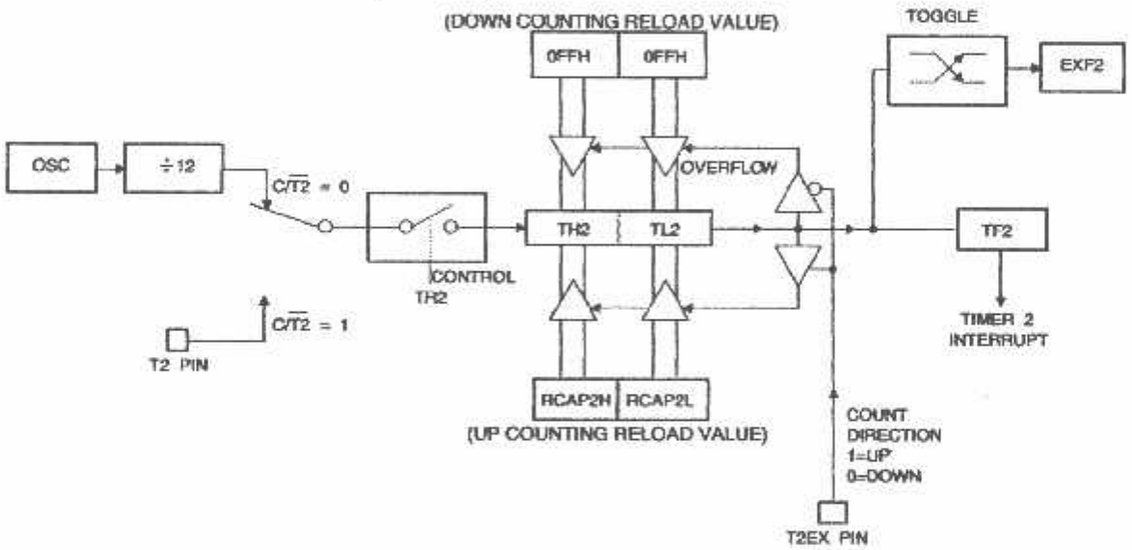


Figure 10-3. Timer 2 Auto Reload Mode (DCEN = 1)



11. Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 5-2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 11-1.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation ($C/\overline{T2} = 0$). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

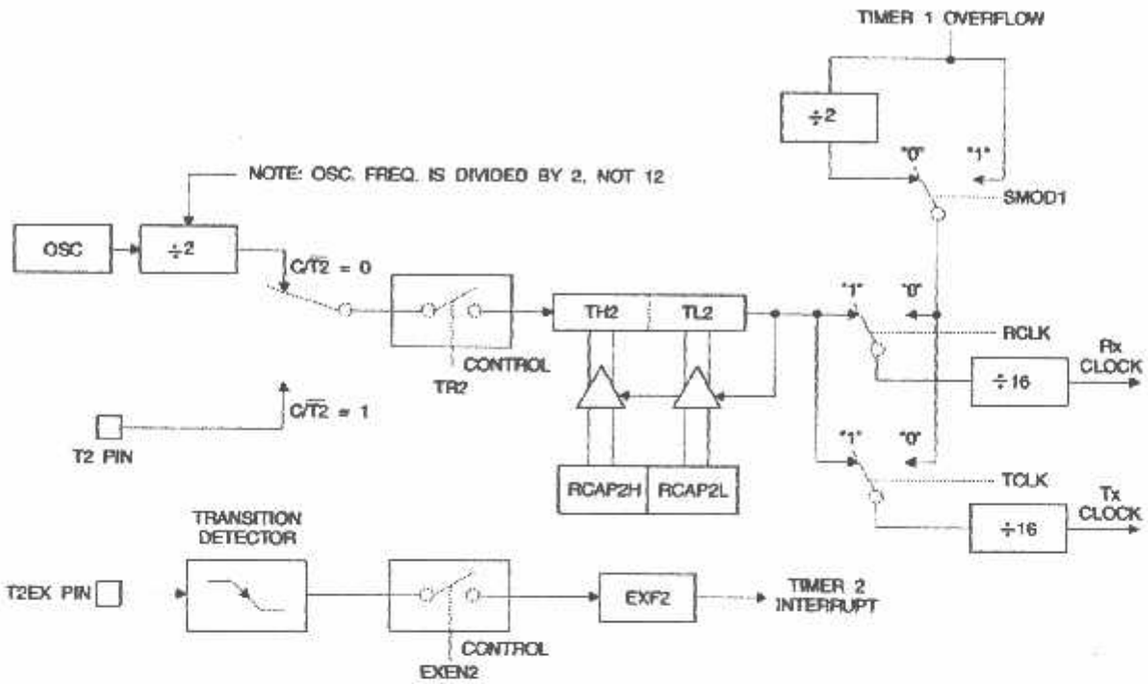
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - \text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 11-1. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus, when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Figure 11-1. Timer 2 in Baud Rate Generator Mode



12. Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 12-1. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz (for a 16-MHz operating frequency).

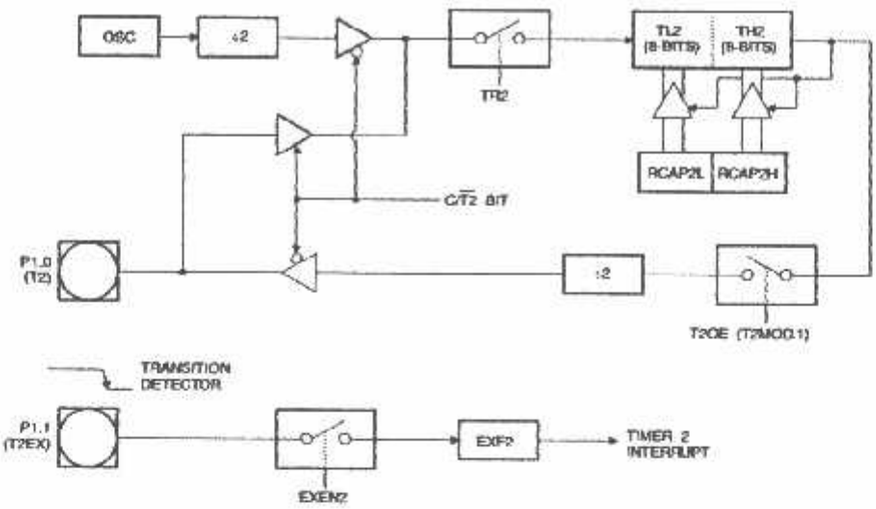
To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536-(\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Figure 12-1. *Timer 2 in Clock-Out Mode*



13. Interrupts

The AT89S52 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 13-1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 13-1 shows that bit position IE.6 is unimplemented. User software should not write a 1 to this bit position, since it may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 13-1. Interrupt Enable (IE) Register

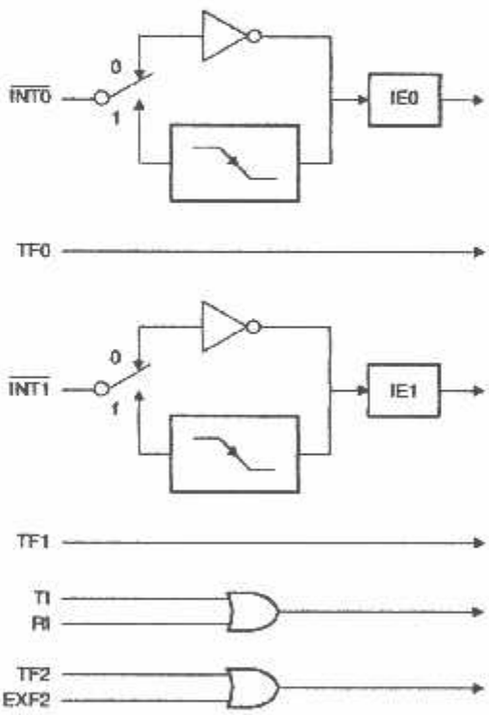
(MSB)							(LSB)
EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to reserved bits, because they may be used in future AT89 products.		

Figure 13-1. Interrupt Sources



14. Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 16-1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 16-2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

15. Idle Mode

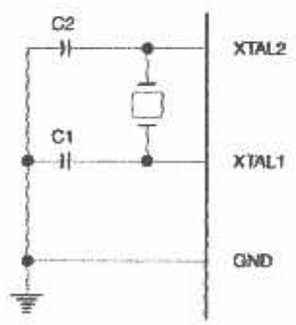
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

16. Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 16-1. Oscillator Connections



Note: 1. C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 16-2. External Clock Drive Configuration

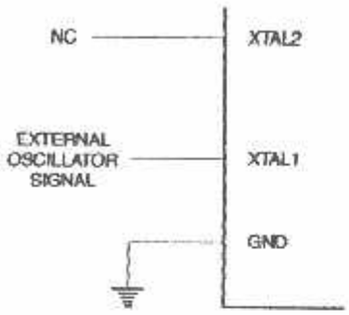


Table 16-1. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

17. Program Memory Lock Bits

The AT89S52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in Table 17-1.

Table 17-1. Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

18. Programming the Flash – Parallel Mode

The AT89S52 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S52 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S52, the address, data, and control signals should be set up according to the "Flash Programming Modes" (Table 22-1) and Figure 22-1 and Figure 22-2. To program the AT89S52, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89S52 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. **The status of the individual lock bits can be verified directly by reading them back.**

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 52H indicates AT89S52
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

19. Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

20. Serial Programming Algorithm

To program and verify the AT89S52 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   a. Apply power between VCC and GND pins.
   b. Set RST pin to "H".

If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

1. Set XTAL1 to "L" (if a crystal is not used).
2. Set RST to "L".
3. Turn V_{CC} power off.

Data Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

21. Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 24-1.

22. Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Table 22-1. Flash Programming Modes

Mode	V_{CC}	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	P0.7-0 Data	P2.4-0	P1.7-0
												Address	
Write Code Data	5V	H	L	(2)	12V	L	H	H	H	H	D_{IN}	A12-8	A7-0
Read Code Data	5V	H	L	H	H	L	L	L	H	H	D_{OUT}	A12-8	A7-0
Write Lock Bit 1	5V	H	L	(3)	12V	H	H	H	H	H	X	X	X
Write Lock Bit 2	5V	H	L	(3)	12V	H	H	H	L	L	X	X	X
Write Lock Bit 3	5V	H	L	(3)	12V	H	L	H	H	L	X	X	X
Read Lock Bits 1, 2, 3	5V	H	L	H	H	H	H	L	H	L	P0.2, P0.3, P0.4	X	X
Chip Erase	5V	H	L	(1)	12V	H	L	H	L	L	X	X	X
Read Atmel ID	5V	H	L	H	H	L	L	L	L	L	1EH	X 0000	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	52H	X 0001	00H
Read Device ID	5V	H	L	H	H	L	L	L	L	L	06H	X 0010	00H

Notes:
1. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{PROG}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{BSY}$ signal is output on P3.0 during programming.
5. X = don't care.

Figure 22-1. Programming the Flash Memory (Parallel Mode)

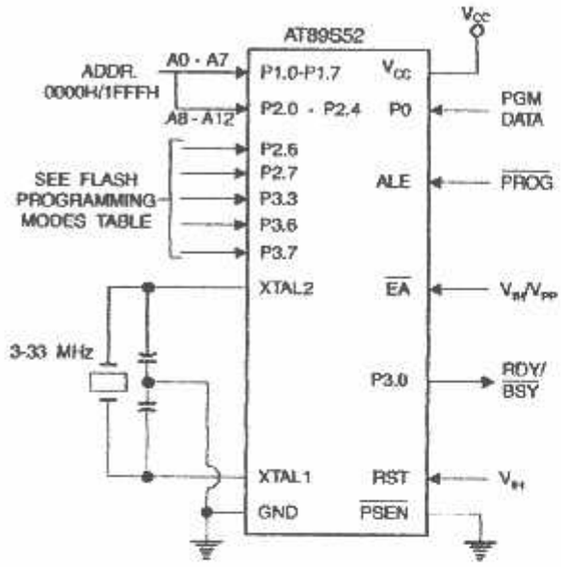
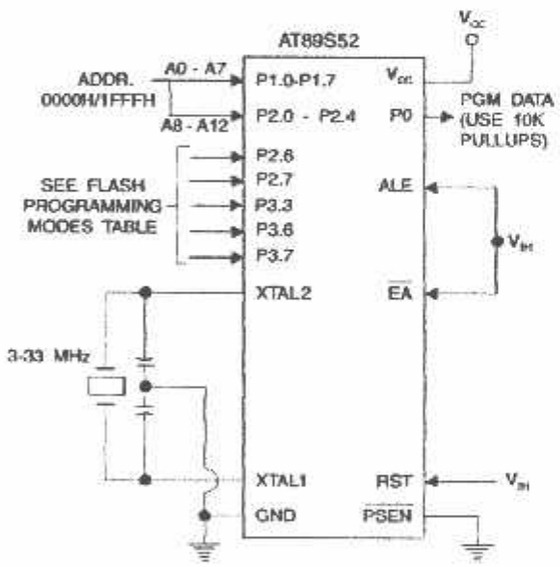


Figure 22-2. Verifying the Flash Memory (Parallel Mode)



23. Flash Programming and Verification Characteristics (Parallel Mode)

T_A = 20°C to 30°C, V_{CC} = 4.5 to 5.5V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	11.5	12.5	V
I_{PP}	Programming Supply Current		10	mA
I_{CC}	V_{CC} Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	3	33	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
t_{GHAX}	Address Hold After $\overline{PROG}$	48 t_{CLCL}		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	48 t_{CLCL}		
t_{GHDX}	Data Hold After $\overline{PROG}$	48 t_{CLCL}		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48 t_{CLCL}		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	0.2	1	µs
t_{AVQV}	Address to Data Valid		48 t_{CLCL}	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		48 t_{CLCL}	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	48 t_{CLCL}	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		50	µs

Figure 23-1. Flash Programming and Verification Waveforms – Parallel Mode

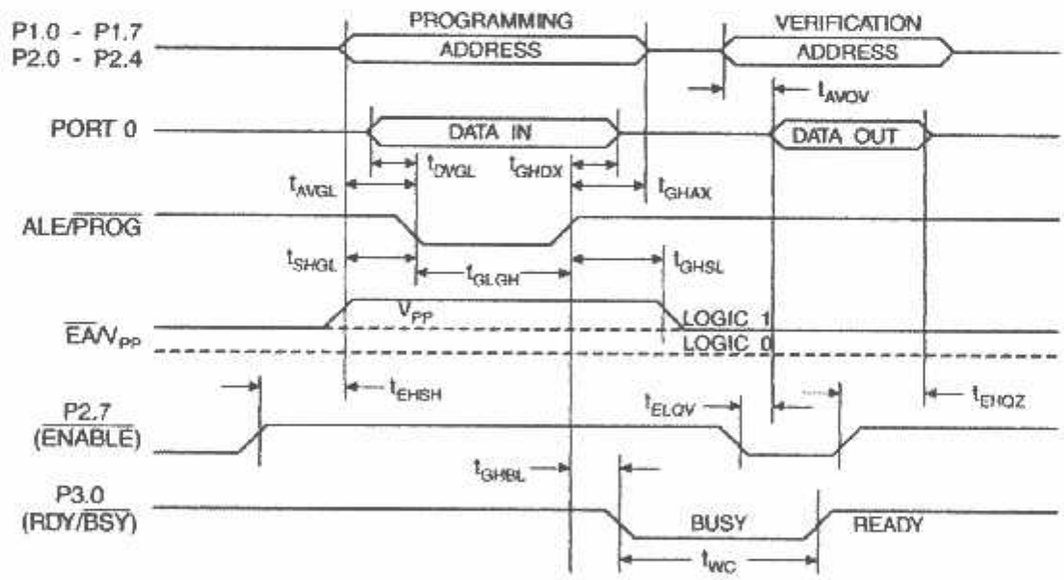
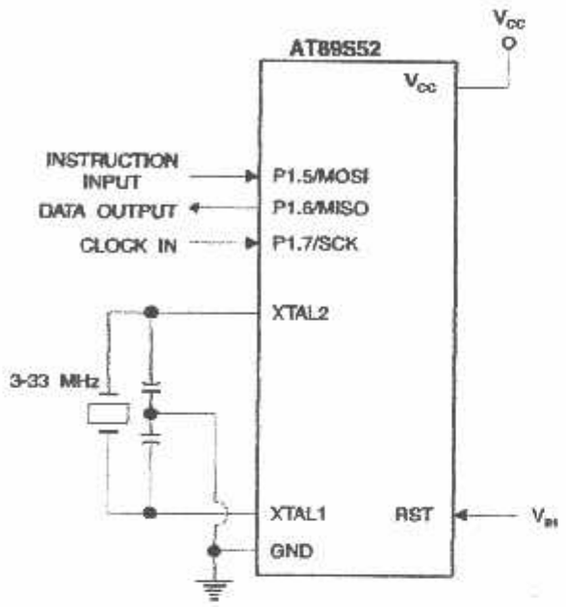


Figure 23-2. Flash Memory Serial Downloading



24. Flash Programming and Verification Waveforms – Serial Mode

Figure 24-1. Serial Programming Waveforms

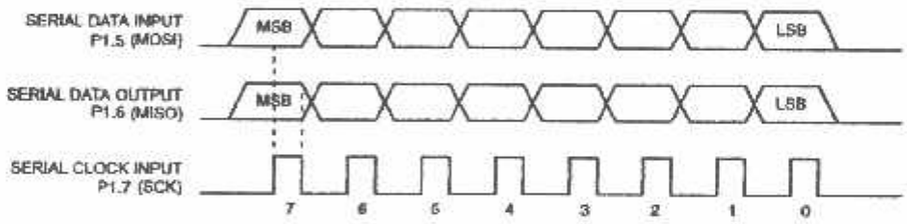


Table 24-1. Serial Programming Instruction Set

Instruction	Instruction Format				
	Byte 1	**Byte 2**	**Byte 3**	**Byte 4**	**Operation**
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	xxx A12 A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	Write data to Program memory in the byte mode
Write Lock Bits[1]	1010 1100	1110 00 B1 B2	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
Read Lock Bits	0010 0100	xxxx xxxx	xxxx xxxx	xxx LB3 LB2 LB1 xx	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Read Signature Bytes	0010 1000	xxx A12 A11 A10 A9 A8	A7 xxx xxx0	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	xxx A12 A11 A10 A9 A8	Byte 0	Byte 1... Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Note: 1. B1 = 0, B2 = 0 ---> Mode 1, no lock protection
B1 = 0, B2 = 1 ---> Mode 2, lock bit 1 activated
B1 = 1, B2 = 0 ---> Mode 3, lock bit 2 activated
B1 = 1, B2 = 1 ---> Mode 4, lock bit 3 activated

} Each of the lock bit modes needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

25. Serial Programming Characteristics

Figure 25-1. Serial Programming Timing

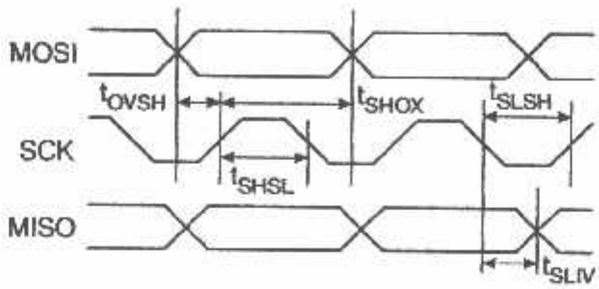


Table 25-1. Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 4.0 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	3		33	MHz
t_{CLCL}	Oscillator Period	30			ns
t_{SHSL}	SCK Pulse Width High	8 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	8 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t_{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t_{SWC}	Serial Byte Write Cycle Time			64 t_{CLCL} + 400	µs

26. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

27. DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 4.0V to 5.5V, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-300	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power-down Mode[2]	V_{CC} = 5.5V		50	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:
   Port 0: 26 mA Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

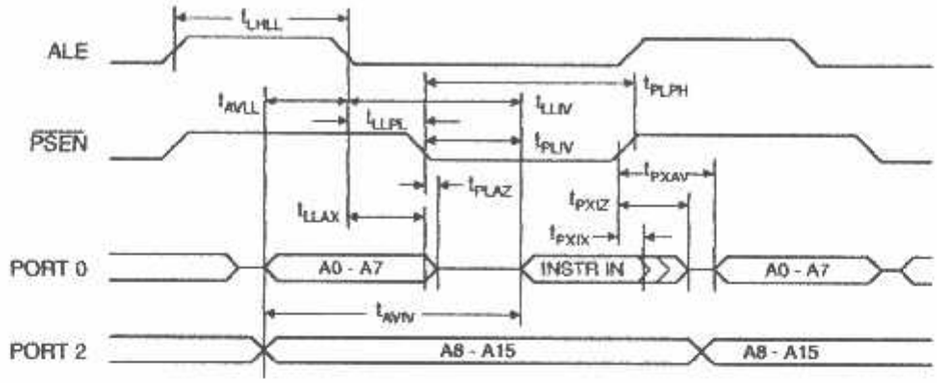
28. AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

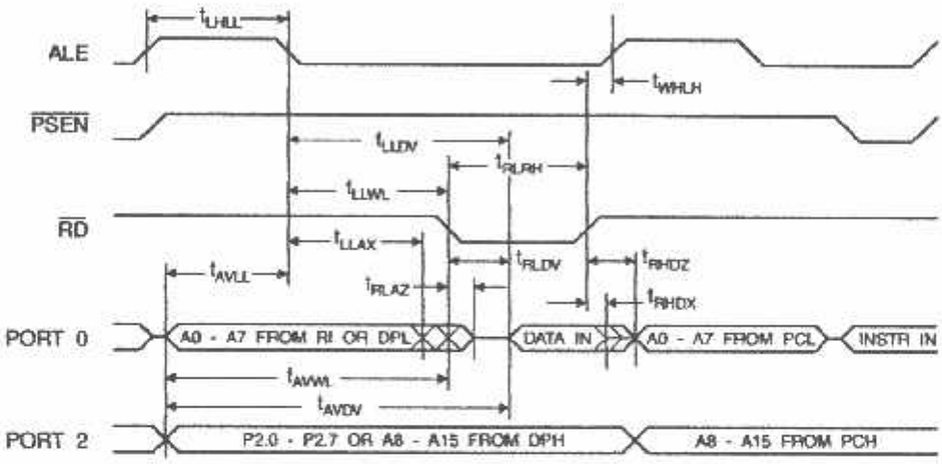
28.1 External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	33	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-25		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-25		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-25		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-60	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-80	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-30		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-130		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-25		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-25	t_{CLCL}+25	ns

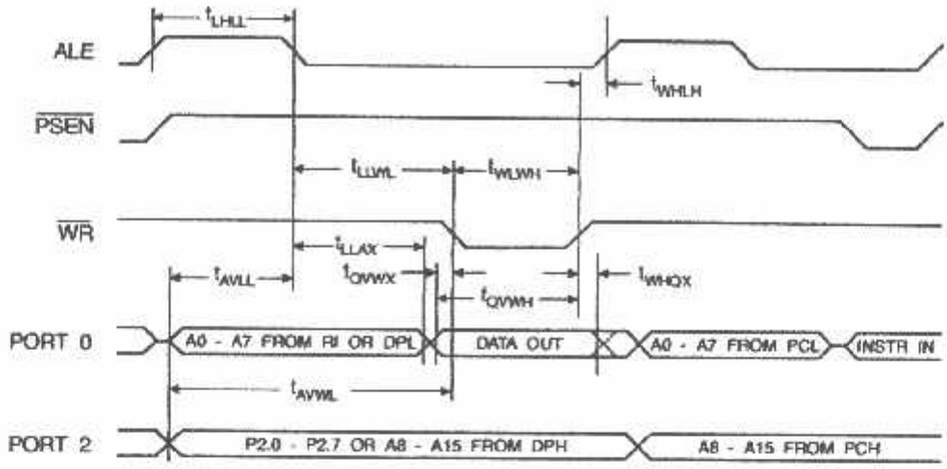
29. External Program Memory Read Cycle



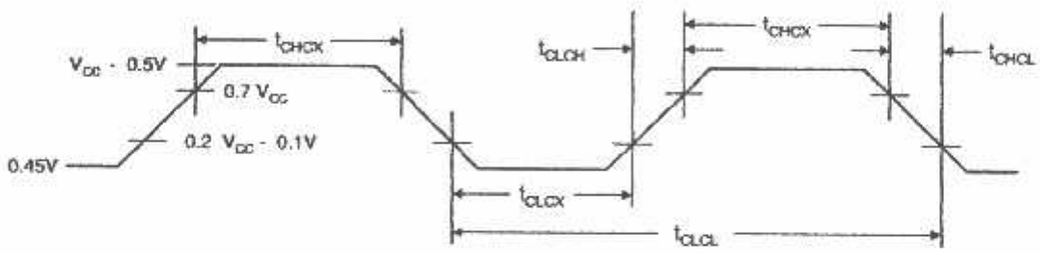
30. External Data Memory Read Cycle



31. External Data Memory Write Cycle



32. External Clock Drive Waveforms



33. External Clock Drive

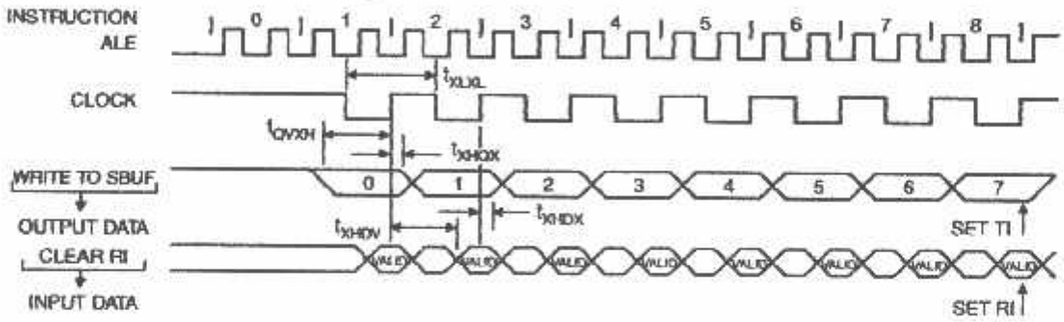
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	33	MHz
t_{CLCL}	Clock Period	30		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

34. Serial Port Timing: Shift Register Mode Test Conditions

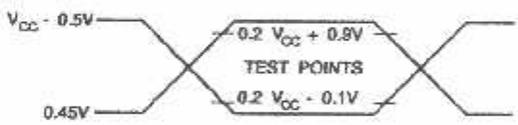
The values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		12 t_{CLCL}		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		10 t_{CLCL}-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		2 t_{CLCL}-80		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		10 t_{CLCL}-133	ns

35. Shift Register Mode Timing Waveforms



36. AC Testing Input/Output Waveforms(1)



Note: 1. AC inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

37. Float Waveforms(1)

Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

38. Ordering Information

38.1 Standard Package

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S52-24AC AT89S52-24JC AT89S52-24PC AT89S52-24SC	44A 44J 40P6 42PS6	Commercial (0°C to 70°C)
		AT89S52-24AI AT89S52-24JI AT89S52-24PI AT89S52-24SI	44A 44J 40P6 42PS6	Industrial (-40°C to 85°C)
33	4.5V to 5.5V	AT89S52-33AC AT89S52-33JC AT89S52-33PC AT89S52-33SC	44A 44J 40P6 42PS6	Commercial (0°C to 70°C)

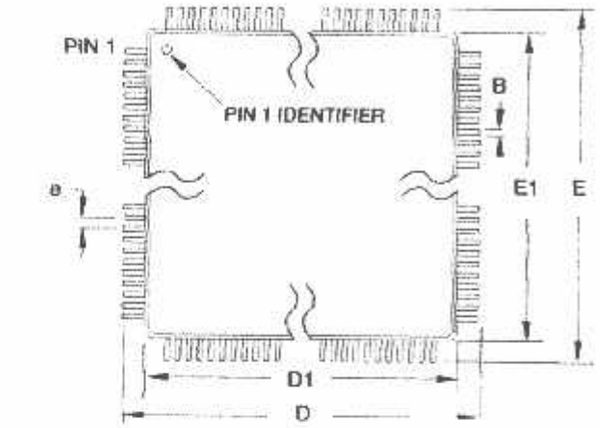
38.2 Green Package Option (Pb/Halide-free)

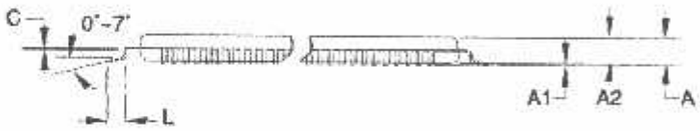
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	4.0V to 5.5V	AT89S52-24AU AT89S52-24JU AT89S52-24PU	44A 44J 40P6	Industrial (-40°C to 85°C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
42PS6	42-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)

39. Packaging Information

39.1 44A – TQFP





COMMON DIMENSIONS
(Unit of Measure = mm)

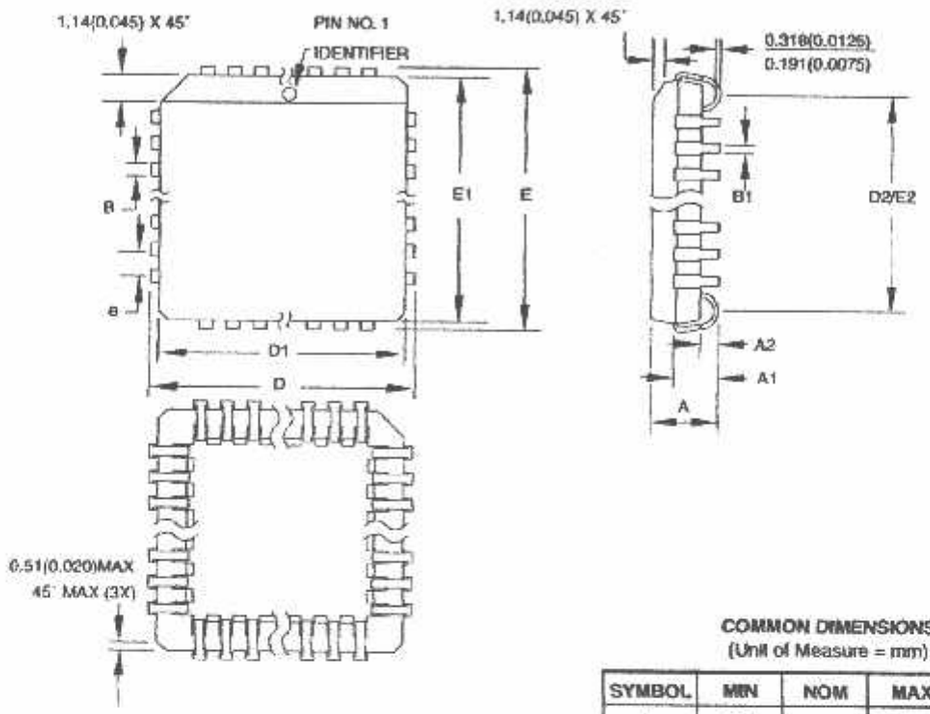
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	44A, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

39.2 44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

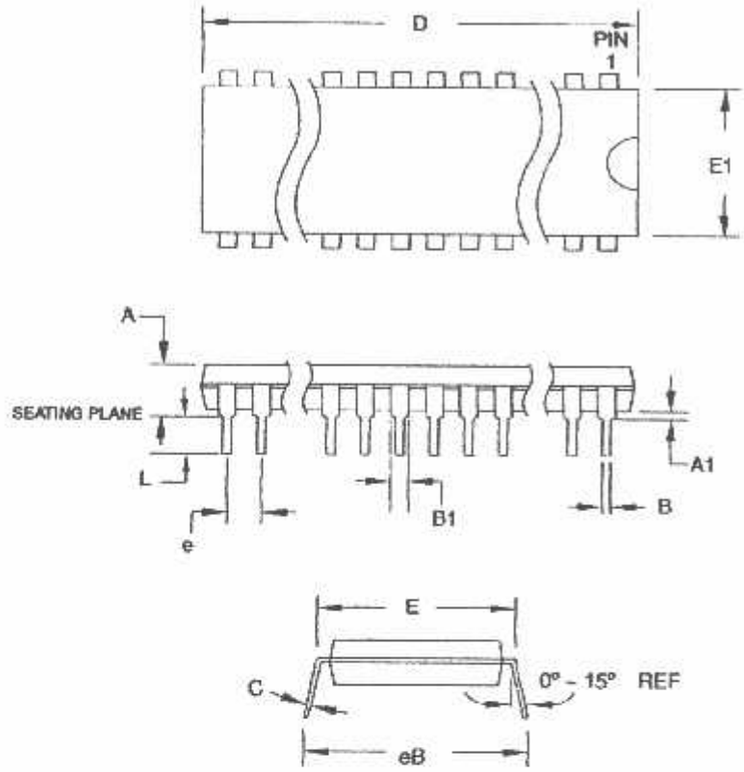
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

39.3 40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

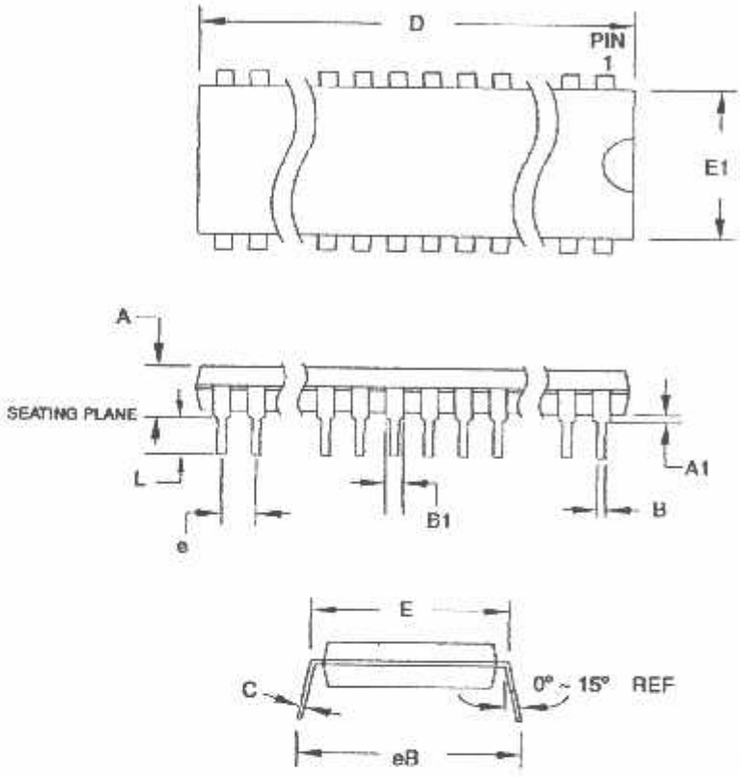
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

39.4 42PS6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.83	
A1	0.51	–	–	
D	36.70	–	36.96	Note 2
E	15.24	–	15.88	
E1	13.46	–	13.97	Note 2
B	0.38	–	0.56	
B1	0.76	–	1.27	
L	3.05	–	3.43	
C	0.20	–	0.30	
eB	–	–	18.55	
e	1.78 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/6/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**42PS6**, 42-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	42PS6	A

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National Semiconductor

June 1989

54LS164/DM54LS164/DM74LS164
8-Bit Serial In/Parallel Out Shift Registers

General Description

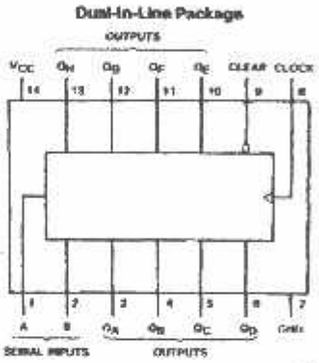
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 80 mW
- Alternate Military/Aerospace device (54LS164) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6368–1

Order Number 54LS164DMQB, 54LS164FMQB, 54LS164LMQB, DM54LS164J, DM54LS164W, DM74LS164M or DM74LS164N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

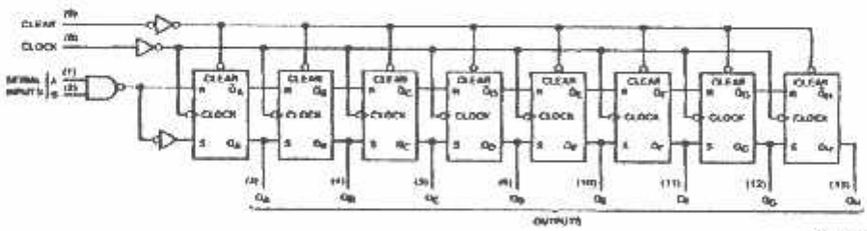
X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagram



TL/F/6368–2

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" tables will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		DM54LS164			DM74LS164			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
t_W	Pulse Width (Note 4)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 4)		17			17			ns
t_H	Data Hold Time (Note 4)		5			5			ns
t_{REL}	Clear Release Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			16	27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

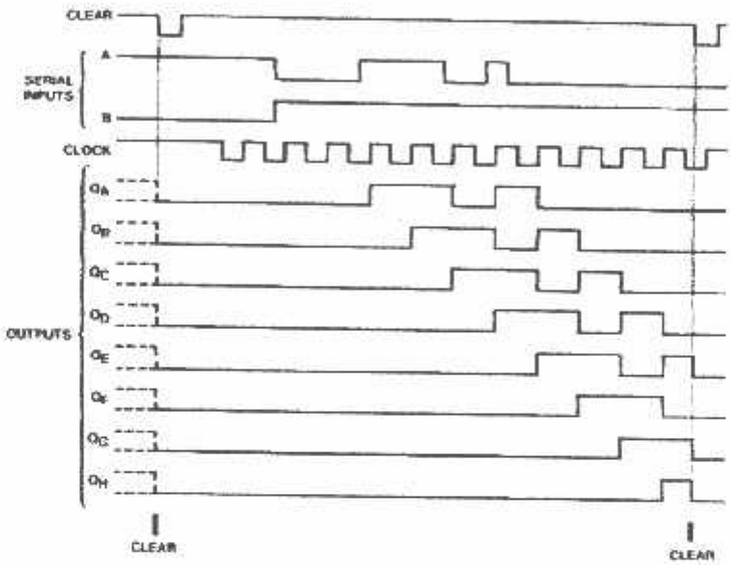
Note 3: I_{CC} is measured with all outputs open, the SERIAL input grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

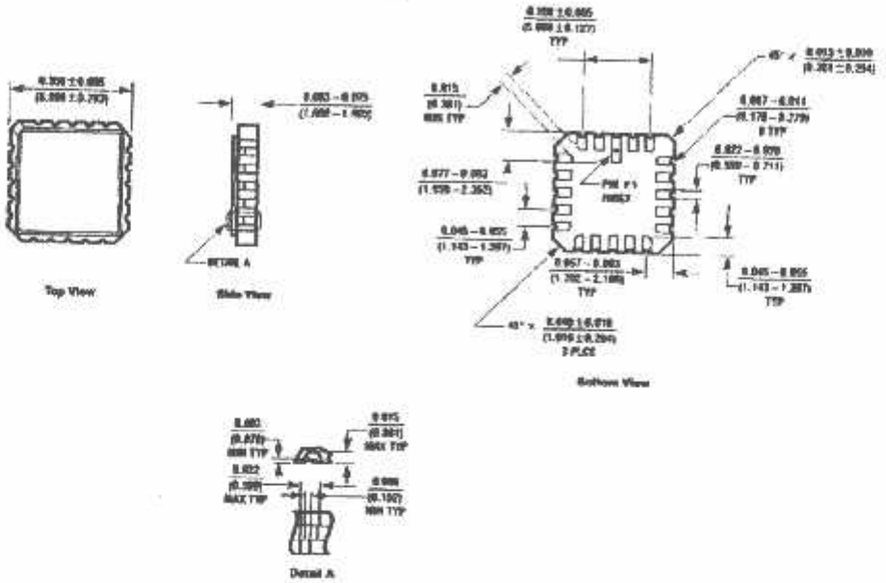
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25				MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		32		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		36		45	ns

Timing Diagram

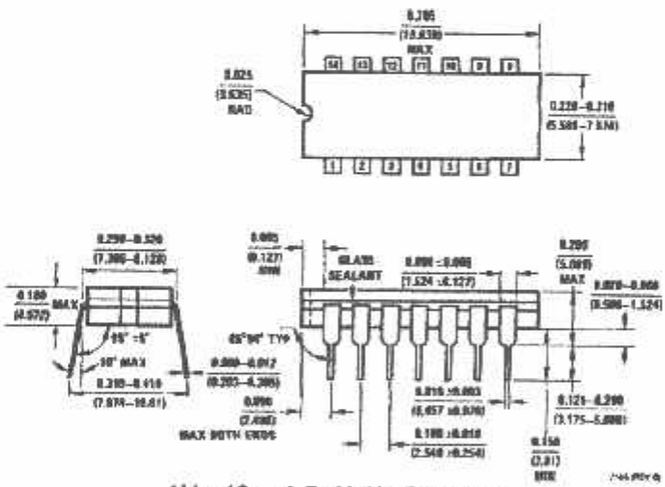


TL/F/6088–3

Physical Dimensions inches (millimeters)

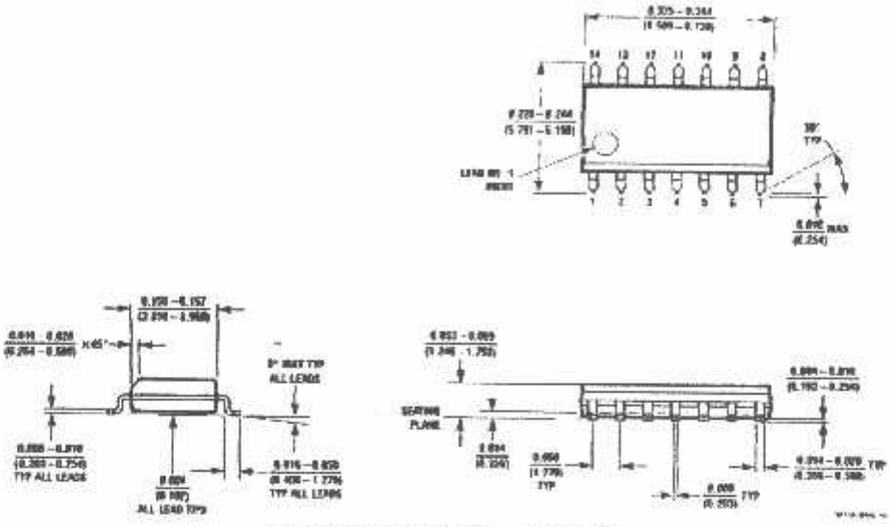


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS164LMQB
NS Package Number E20A

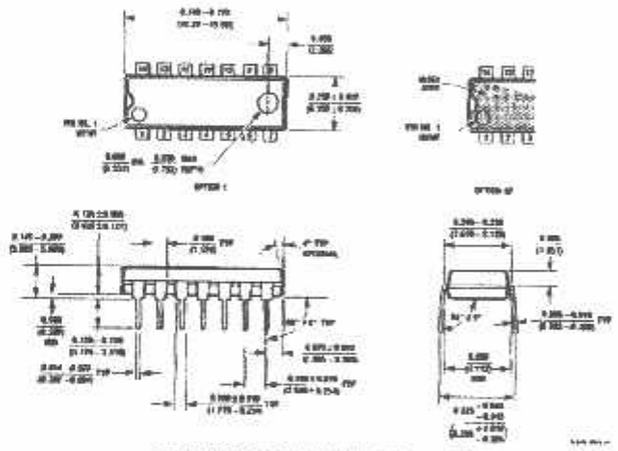


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS164DMQB or DM54LS164J
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)

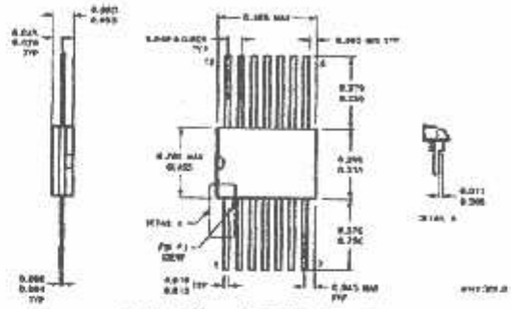


14-Lead Small Outline Molded Package (M)
Order Number DM74LS164M
NS Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS164N
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS164FMQB or DM54LS164W
NS Package Number W14B

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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