PERENCANAAN DAN PEMBUATAN ALAT UNTUK MENAMPILKAN KARAKTERISTIK KURVA TRACER TRANSISTOR BIPOLAR BERBASIS MIKROKONTROLLER AT89C51

SKRIPSI

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JURUSAN TEKNIK ELEKTRO
KONSENTRASI TEKNIK ELEKTRONIKA
FAKULTAS TEKNOLOGI INDUSTRI
INSTITUT TEKNOLOGI NASIONAL MALANG

2009

LEMBAR PERSETUJUAN

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SKRIPSI

Disusun Dan Diajukan Sebagai Salah Satu Syarat Untuk Memperoleh Gelar Sarjana Teknik Elektronika Strata Satu (S-1)

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2009

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Pada Hari : Sabtu
Tanggal : 3 Oktober 2009
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ABSTRAKSI

PERENCANAAN DAN PEMBUATAN ALAT UNTUK MENAMPILKAN KURVA KARAKTERISTIK TRANSISTOR BIPOLAR BERBASIS MIKROKONTROLLER AT89C51

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Transistor adalah salah satu komponen semikonduktor yang banyak digunakan pada berbagai rangkaian elektronika. Transistor dapat berfungsi sebagai saklar, penguat (arus maupun tegangan) dan dengan elektronika digital dapat dibangun gerbang logika. Agar transistor dapat beroperasi secara tepat maka maka transistor harus di operasikan di daerah linier agar diperoleh sinyal keluaran yang tidak cacat.

Dengan alat ini kita akan dapat menampilkan kurva karakteristik dari transistor, yang di khususkan pada transistor jenis NPN. Dalam alat ini yang berfungsi sebagai control utama adalah µC AT89C51.

Ketika alat diaktifkan µC akan menset tegangan kemudian dirubah melalui DAC untuk mengaktifkan rangkaian transistor. Selanjutnya nilai – nilai yang dihasilkan rangkaian transistor dimasukkan ke ADC untuk dibaca µC, selanjutnya nilai- nilai itu akan ditampilkan di computer berupa grafik.

Dengan alat ini kita akan mampu menampilkan grafik dari transistor sehingga dapat mempelajari karakteristik dan mengetahui daerah titik kerjanya

Kata kunci: Transistor, Saklar, AT 89C51

KATA PENGANTAR

Segala puji dan syukur kami panjatkan kehadirat Allah SWT atas limpahan rahmat dan hidayah-Nya sehingga penulis dapat menyelesaikan laporan skripsi ini dengan judul, ***Perencanan dan Pembuatan Alat Untuk Menampilkan Karakteristik Kurva Tracer Transistor Bipolar Berbasis Mikrokontroller AT89C51.***

Skripsi ini merupakan salah satu syarat yang harus ditempuh dalam menyelesaikan program studi (S-1) Jurusan Teknik Elektro Konsentrasi Elektronika di Institut Teknologi Nasional Malang. Dalam penyusunan skripsi ini penulis tidak lepas dari bantuan dari berbagai banyak pihak, oleh karena itu pada kesempatan ini penulis ingin mengucapkan banyak terima kasih kepada:

1. Allah SWT atas segala berkah dan kemudahan yang telah diberikan dalam penyelesaian skripsi ini.
2. Bapak Dr Ir Abraham Lomi, MSEE selaku rektor ITN Malang.
3. Bapak Ir. Sidik Nurtjahjono, MT selaku dekan FTI ITN Malang.
4. Bapak Ir. F Yudi Limpraptono, MT selaku ketua jurusan Teknik Elektro S-1
5. Bapak Ir.Yusuf Ismail Nahkoda, MT selaku sekretaris jurusan Teknik Elektro S-1
6. Bapak Ir. F Yudi Limpraptono, MT selaku dosen pembimbing atas bantuan, arahan dan bimbingan dalam penyusunan skripsi ini.
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Buat Ayahanda alm, tiada kata yang paling indah yang dapat aku ucapkan. Terima kasih engkau telah berikan semua tenaga dan pikiran untuk anakmu hingga akhir hayat. Terima kasih ayah engkau telah mengantarkan aku, meski hanya sampai dipintu gerbang perjuangan.

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Buat yang belum disebut

Thank's A lot

Skripsi ini aku persembahkan untuk:

Ayah alm & ibu, Lin, Rizal serta nenekku Alm.

Dan juga almamaterku

Teknik Elektronika S-1 Institut Teknologi Nasional Malang

DAFTAR ISI

DAFTAR GAMBAR

BAB I

PENDAHULUAN

1.1 Latar Belakang

Dunia elektronika dari hari ke hari semakin menunjukkan kemajuan yang pesat seiring kemajuan ilmu dan teknologi. Peralatan elektronika menjadi piranti yang sangat banyak digunakan diberbagai bidang, dan piranti yang sudah ada akan terus berkembang agar memiliki kemampuan yang lebih baik dan lebih kompleks aplikasinya. Dengan semakin kompleksnya sebuah piranti maka akan semakin rumit instrumennya

Transistor adalah salah satu komponen semikonduktor yang banyak digunakan pada berbegai rangkaian elektronika. Transistor dapat befungsi sebagai saklar, penguat (arus maupun tegangan) dan dengan elektronika digital dapat dibangun gerbang logika.

Agar transistor dapat beroperasi secara tepat maka transistor harus dioperasikan didaerah linier agar diperoleh sinyal keluaran yang tidak cacat. Maka dengan mempelajari karakteristik dari transistor akan diketahui daerah titik kerjanya

1.2 Rumusan masalah

Dengan memperhatikan latar belakang dari usulan skripsi ini didapatkan rumusan masalah sebagai berikut :

- Bagaimana merencanakan dan membuat minimum sistem mikrokontroler AT89C51
- Bagaimana membuat rangkaian DAC agar besaran yang dimasukkan bisa mengaktifkan transistor
- Bagaimana membuat rangkaian transistor
- Bagaimana membuat rangkaian ADC agar besaran yang dikelurkan transistor dapat dibaca oleh mikrokontroller
- Bagaimana membuat perangkat lunak atau software yang berfungsi untuk mengendalikan alat yang direncanakan

1.3 Tujuan Perencanaan

Dari rumusan masalah di atas maka tujuan ini adalah untuk merencanakan dan membuat alat untuk menampilkan karakterisik kurva tracer transistor bipolar.

1.4 Batasan Masalah

Agar pemasalahan dalam tugas akhir ini tidak berkambang karena keterbatasan pengatehuan, waktu, dan biaya maka pembahasan dibatasi pada :

a. Minimum system yang dirancang menggunakan Chip AT89C51 sebagai unit kontrol utama.
b. Pembahasan hanya ditekankan pada kurva karakteristik
c. Transistor yang digunakan adalah jenis NPN


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BAB II

LANDASAN TEORI

Pada bab II akan diberikan peembahasan mengenai teori yang menunjang penyelesaian skripsi ini. Pembahasan terebut mengenai mikrokontroler AT89C51 dan komponen penunjang lainnya yang meliputi transistor Bipolar, DAC, ADC, buffer, penghubung data, dan program visual basic.

2.1. Mikrokontroler AT89C51

Perbedaan antara mikroprosesor dan mikrokontroler adalah

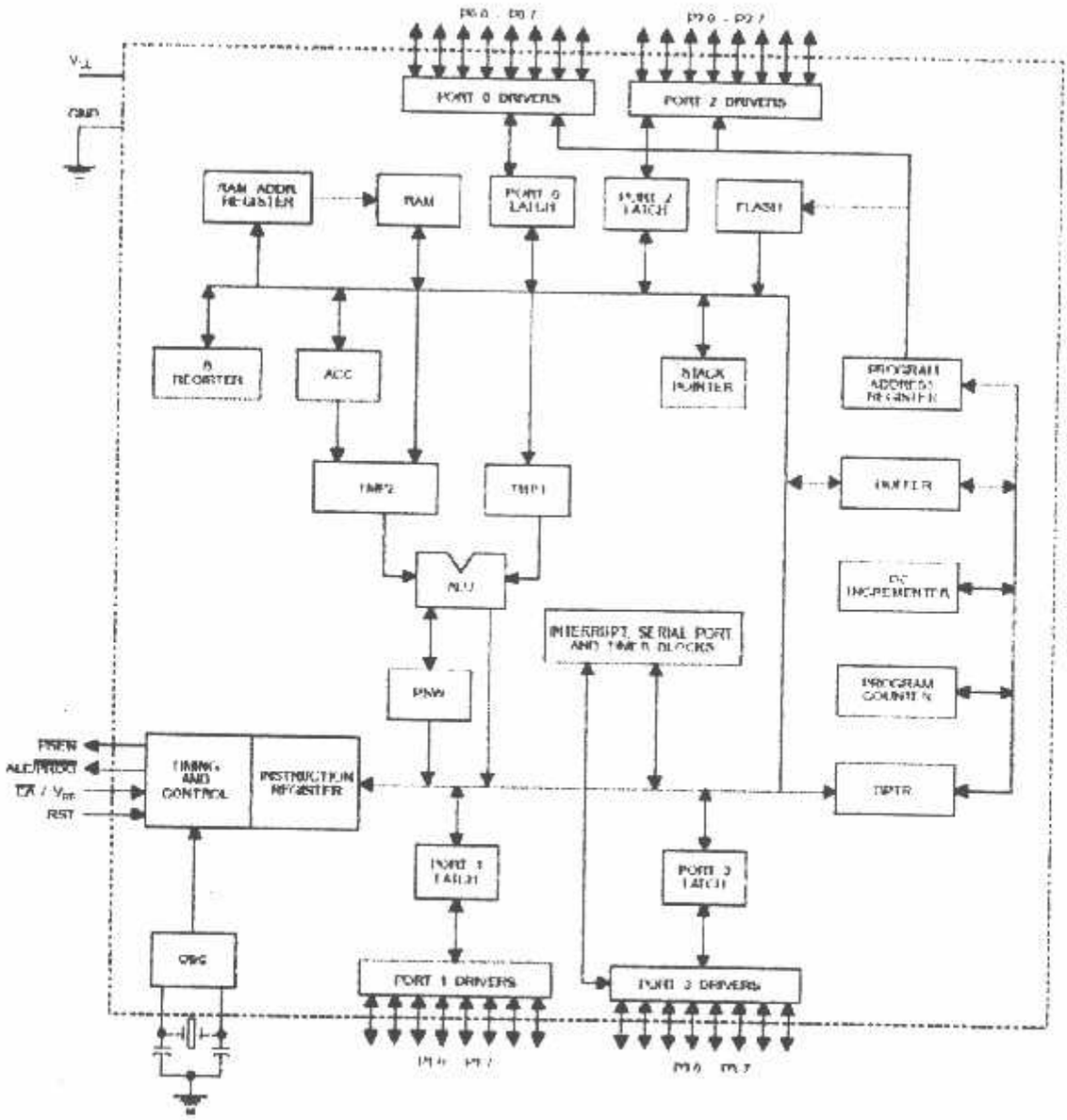
Mikroprosesor: adalah bagian dari CPU dari sebuah computer, tanpa memori tanpa I/ O dan Peripheral. Contoh 8088 dan 80x86. Untuk dapat bekerja membutuhkan perangkat pendukung berupa RAM, ROM, dan I/O

Mikrokontroler atau yang kita kenal dengan *Single Chip* mengkombinasikan CPU dengan memori dan I/O. Dengan demikian suatu mikrokontroler tidak membutuhkan tambahan RAM, ROM dan I/O.

Mikrokontroler AT89C51 adalah Mikrokontroler ATMEL yang kompatibel penuh dengan mikrokontroler keluarga MCS-51, membutuhkan daya rendah, memiliki performance yang tinggi dan merupakan mikrokomputer 8-bit yang dilengkapi 4Kbyte EEPROM (Electrical Eresable and Programable Read Only Memory) dan 128 X 8-bit internal RAM. Program memori yang dapat deprogram ulan dalam system atau menggunakan programmer Nonvolatile memory konvensional. Dalam system mikrokontroler terdapat dua hal yang

mendasar yaitu perangkat lunak dan perangkat keras yang keduanya saling terkait dan mendukung.

2.1.1. Perangkat Keras Mikrokontroler AT89C51



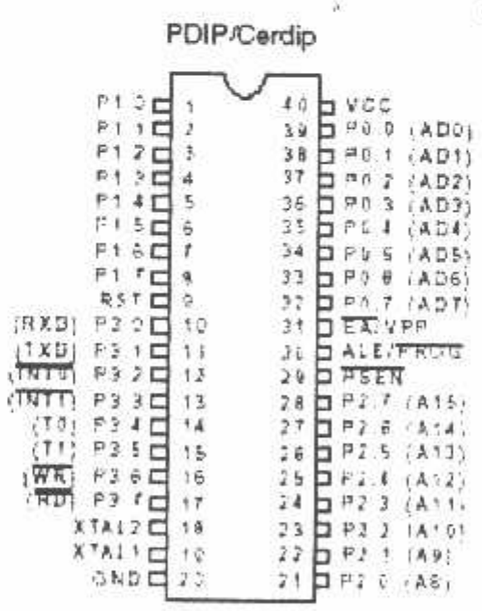
Gambar 2.-1 Blok Diagram Mikrokontroler AT89C51(5)

Secara umum mikrokontroler AT89C51 memiliki fitur:

- CPU 8-bit
- Memiliki 4 Kb flash memory. Flash dapat ditulis / dihapus 1000 kali
- Memiliki internal RAM 128 byte
- Memiliki I/O sebanyak 32 line
- 2 Timer/Counter 16-bit
- Menangani 6 sumber interupsi
- 3 level program memori lock
- Memiliki serial port, untuk komunikasi serial

2.1.2. Konfigurasi Pin Mikrokontroler AT89C51

Mikrokontroler AT89C51 memiliki 40 pin yang diperlihatkan pada gambar berikut:



Gambar 2-2 Konfigurasi Pin AT89C51(5)

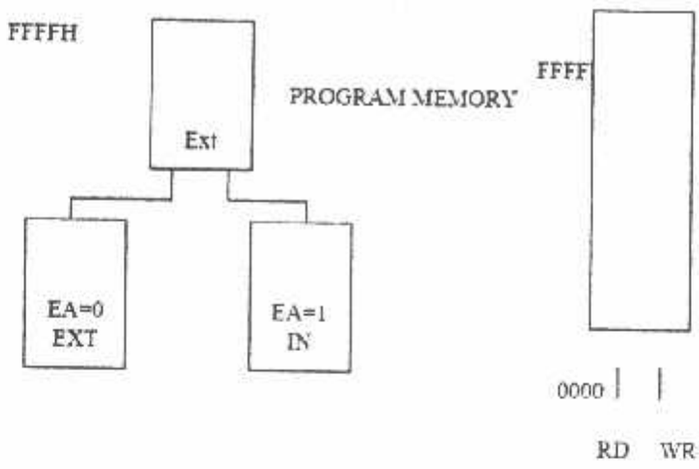
Penjelasan masing-masing pin adalah sebagai berikut:

1. port 1 sampai 8 (Port 1) merupakan port input/output 8 bit dua arah yang dapat digunakan untuk berbagai keperluan (general Purpose)
2. Port 9 RESET, merupakan pin yang berfungsi mereset MCU AT89C51 ke keadaan awal. Port ini dihubungkan ke power on reset
3. Port 10 sampai 17 (port 3) adalah port input/output 8 bit dua arah. Port 3 juga memiliki fungsi pengganti sebagai:
   - Port 10 port komunikasi input serial RXD
   - Port 11 port komunikasi output serial TXD
   - Port 12 saluran interupsi eksternal 0 (aktif rendah) INT0
   - Port 13 saluran interupsi eksternal 1 (aktif rendah) INT1
   - Port 14 input timer 0 T0
   - Port 15 input timer 1 T1
   - Port16 berfungsi sebagai sinyal kendali tulis, saat prosesor akan menulis data ke memori I/O luar WR
   - Port 17 berfungsi sebagai sinyal kendali tulis, saat prosesor akan membaca data ke memori I/O luar RD
4. Port 18 (XTAL 1) adalah port masukan ke rangkaian osilator internal. Sebuah osilator kristal atau sumber osilator luar dapat digunakan.
5. Port 19 (Xtal 2) adalah port keluaran ke rangkaian osilator internal. Port ini dipakai bila menggunakan osilator kristal
6. Port 20 (Ground) dihubungkan ke Vss atau Ground

7. Port 21 sampai 28 (Port 2) adalah port pararel 2 (P2) selebar 8 bit dua arah. Port 2 ini digunakan sebagai pengalamat bila dilakukan pengaksesan memori eksternal
8. Port 29 adalah port PSEN (Program Store Enable) yang merupakan sinyal pengontrol yang membolehkan program memory eksternal masuk ke dalam bus selama proses pemberian/pengambilan instruksi (fetching)
9. Port 30 adalah port ALE (Addres Latch Enable) yang digunakan untuk menahan alamat memori eksternal selama proses pelaksanaan instruksi
10. Port 31 (EA). Bila port ini diberi logika tinggi (H) mikrokontroler akan melaksanakan instruksi dari ROM/EPROM. Ketika isi program counter kurang dari 4096. Bila diberi logika rendah (L), mikrokontroler akan melaksanakan seluruh instruksi dari program emori program luar.
11. Port 32 sampai 39 (Port 0) merupakan port pararel 8 bit open drain dua arah. Bila digunakan untuk mengakses memori luar, port ini akan memultipleks alamat memori dengan data.
12. Port 40 (Vcc) dihubungkan dengan ke Vcc + 5 volt

2.1.3. Organisasi Memori

Mikrokontroler MCS 51 memiliki pembagian ruang alamat untuk program dan data. Memori program hanya dapat dibaca tidak dapat ditulisi. Sedang memory data dapat ditulisi Program yang berukuran lebih dari kapasitas EEPROM (4 Kbite untuk 8951, dan 8 Kbit untuk 8952) disimpan di EEPROM eksternal. Sinyal yang membolehkan pembacaan dari memori program eksternal adalah dari pin PSEN (Program Store Enable)



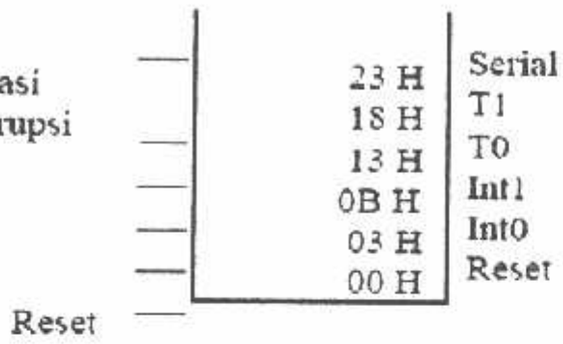
Gambar 2-3 Struktur Memori Mikrokontroler 8951[5]

Mikrokontroler AT89C51 memiliki 5 buah ruang alamat,yaitu

1. Ruang alamat kode (code addresss space) sebanyak 4k, yang seluruhnya merupakan ruang alamat kode eksternal (off chip)
2. Ruang alamat data internal yang dapat dialamati secara langsung, yang terdiri atas:
   - RAM sebanyak 128 byte
   - Hardware register sebanyak 128 byte
3. Ruang alamat data internal yang dialamati secara tidak langung sebanyak 128 byte, seluruhnya diakses dengan pengalamatan tidak langsung.
4. Ruang alamat data eksternal 64K bytc yang dapat ditambahkan oleh pemakai.
5. Ruang alamat bit. Dapat diakses dengan pengalamatan langsung.

2.1.3.1. Memori Program

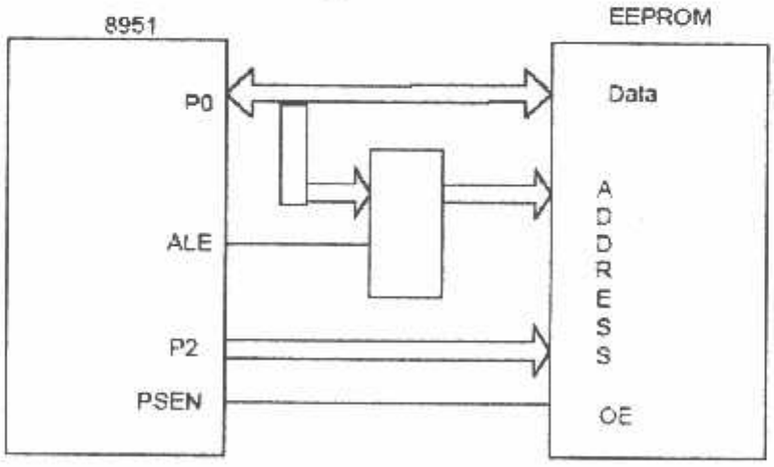
Gambar dibawah memperlihatkan bagian bawah dari memori program. Setelah reset CPU memulai eksekusi dari lokasi 0000H



Gambar 2-4 Memori Program(5)

Setiap interupsi mempunyai lokasi tetap dalam memori program. Interupsi menyebabkan CPU melompat lokasi yang ada diatas yang merupakan alamat-alamat lokasi interupsi. Terdapat sub rutin yang harus dilaksanakan.

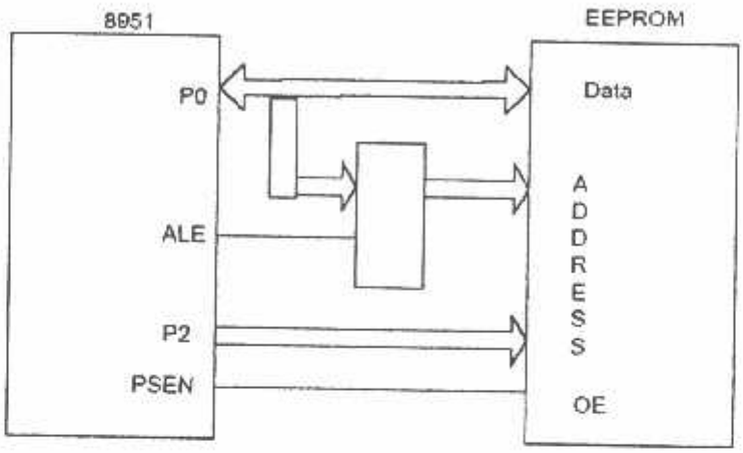
kita dapat menambahkan EEPROM eksternal bila dirasa ukuran program lebih dari 4 Kbyte. Tampak pada blok diagram dibawah ini :



Gambar 2-5 EEPROM Eksternal(5)

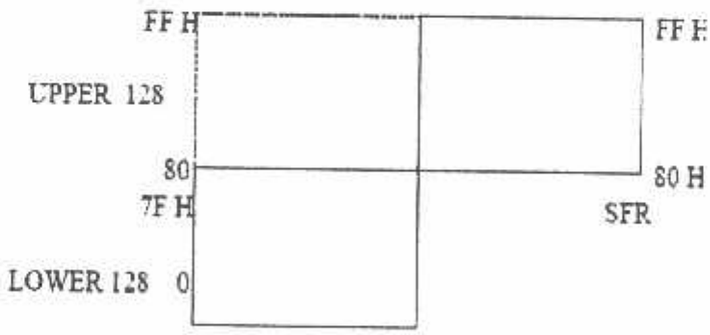
2.1.3.2. Memori Data

Gambar dibawah memperlihatkan hubungan mikrokontroler untuk mengkases RAM Eksternal. Untuk melakukan pembacaan dan penulisan, mikrokontroler akan mengirimkan RD atau WR.



Gambar 2-6 Menggabungkan Mikrokontroler dengan RAM Eksternal(5)

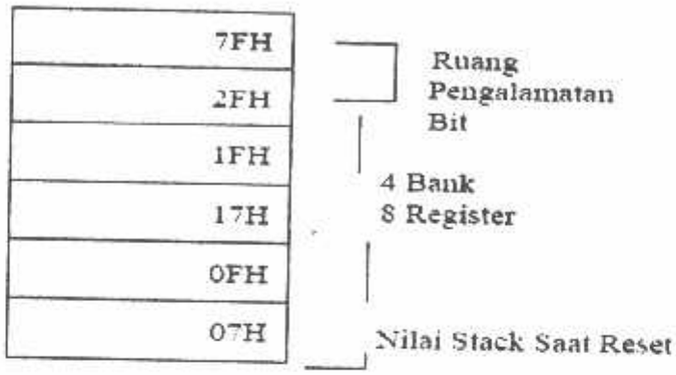
Memori data internal dipetakan seperti pada gambar 2-7. Ruang memorinya dibagi menjadi tiga blok, yaitu sebagai Lower 128, upper 128 dan ruang SFR



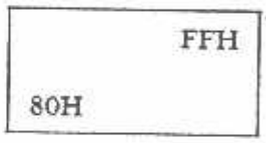
(Special Function Register)

Gambar 2-7 Memori data Intenal(5)

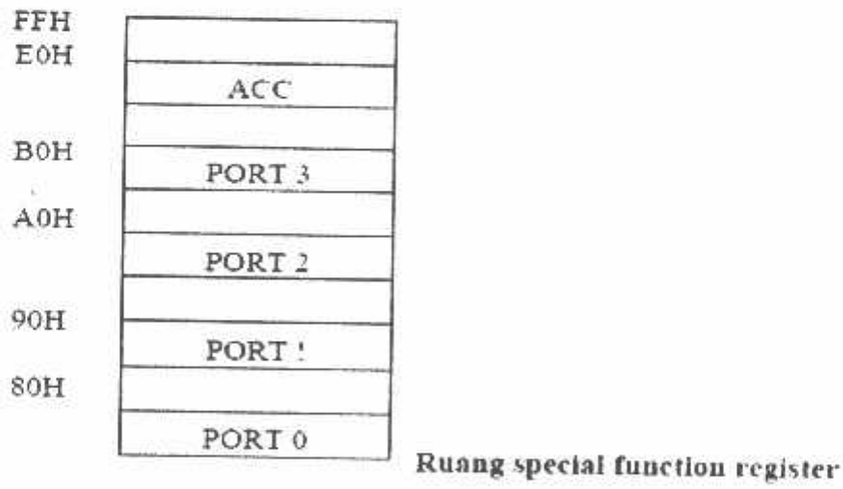
Bagian Bawah dari 128 Byte RAM dipetakan seperti telihat pada gambar 2-8. Tiga puluh byte paling bawah dikelompokkan dalam 4 bank (8 Register) yaitu R0 sampai R7. Dua bit dalam psw memilih register bank yang digunakan.



Bagian Bawah 128 Byte RAM Internal



bagian atas 128 byte RAM Internal



Gambar 2-8 Organisasi Memori(5)

2.1.4. Register – Register di Mikrokontroler AT89C51

Register di Mikrokontroler dapat diklasifikasikan berdasar penggunaan sebagai berikut:

Tabel 2-1 register-register mikrokontroller AT 89C51[5]

Klasifikasi Register	Nama Register	Nama	Alamat	fungsi
Register Untuk Aritmatika dan Logik (8 Byte)	A	Accumulator	E0H	
	B		F0H	
Register I/O (8 Byte)	P0	Port 0	80H	
	P1	Port 1	90H	
	P2	Port 2	A0H	
	P3	Port 3	B0H	
	SBUF	Serial Buffer	98H	
Register Control (8 Byte)	IP	Interupt Priority Control	B8H	
	IE	Interupt Enable Control	A8H	
	TMOD	Timer/Counter Mode Control	89H	
	TCON	Timer/Counter Control	88H	
	TH0	Timer/Counter 0 High Byte	8CH	
	TL0	Timer/Counter 0 Low Byte	8AH	
	TH1	Timer/Counter 1 High Byte	8DH	
	TL1	Timer/Counter 0 Low Byte	8BH	
	PCON	Power Control	87H	
Register Bantu (8 Byte)	R0..R7		00H..07H	
	R0'..R7'		08H..0FH	
	R0''..R7''		10H..17H	
	R0'''..R7'''		18H..1FH	
Register 16 Bit	DPTR		82H..83H	
Register Pointer	SP		81H	

2.1.5. Interupsi

Ada 2 jenis interupsi dalam mikrokontroler 8951 yaitu :

1. Interupsi yang tak dapat dihalangi oleh perangkat lunak(Non maskable Interrupt) misalnya reset
2. Interupsi yang dapat dihalangi perangkat lunak (maskable interrupt) contoh interupsi jenis ini adalah INT 0dan IT 1 serta timer/Counter 0, Timer/Counter 1 dan interupsi serial (internal)

Alamat layanan rutin interupsi dari setiap sumber interupsi diperlihatkan pada table dibawah ini:

Tabel 2-2 Alamat Interupsi[5]

Nama	Lokasi	Alat Interupsi
Reset	00 H	Power on reset
$\overline{\text{Int 0}}$	03H	INT 0
Timer 0	0BH	Timer 0
$\overline{\text{Int 1}}$	13 H	INT 1
Timer 1	1 BH	Timer 1
Sint	23 H	Port I/O serial

Mikrokontroler AT89C51 menyediakan 5 sumber interupsi: 2 interupsi eksternal, 2 interupsi timer, dan satu interupsi port serial.. Register yang mengontrol interupsi yaitu IE(Interrupt enable) dan IP (Interupt priority)

2.1.5.1.Interupsi enable

Tabel 2-3 Interupsi Enable[5]

MSB							LSB
EA	-	-	ES	ETI	EXI	ET0	EX0

Simbol	**Posisi**	**Fungsi**
EA	IE.7	Melumpuhkan semua interupsi. Jika EA = 0 tidak ada interupsi yang akan dilayani. Jika EA = 1 setiap sumber interupsi dapat dijalankan atau dilumpuhkan secara individual
-	IE.6	Kosong

2.2. Transistor

Transistor adalah komponen semikonduktor yang dapat dipakai sebagai penguat, sebagai sirkuit pemutus dan penyambung (switching), stabilisasi tegangan, modulasi sinyal atau sebagai fungsi lainnya. Transistor dapat berfungsi semacam kran listrik, dimana berdasarkan arus inputnya (BJT) atau tegangan inputnya (FET), memungkinkan pengaliran listrik yang sangat akurat dari sirkuit sumber listriknya.

Pada umumnya, transistor memiliki 3 terminal. Tegangan atau arus yang dipasang di satu terminalnya mengatur arus yang lebih besar yang melalui 2 terminal lainnya. Transistor adalah komponen yang sangat penting dalam dunia elektronik modern. Dalam rangkaian analog, transistor digunakan dalam amplifier (penguat). Rangkaian analog melingkupi pengeras suara, sumber listrik stabil, dan penguat sinyal radio. Dalam rangkaian-rangkaian digital, transistor digunakan sebagai saklar berkecepatan tinggi. Beberapa transistor juga dapat dirangkai sedemikian rupa schingga berfungsi sebagai logic gate, memori, dan komponen-komponen lainnya.

2.2.1. Cara Kerja Transistor

Dari banyak tipe-tipe transistor modern, pada awalnya ada dua tipe dasar transistor, bipolar junction transistor (BJT atau transistor bipolar) dan field-effect transistor (FET), yang masing-masing bekerja secara berbeda.

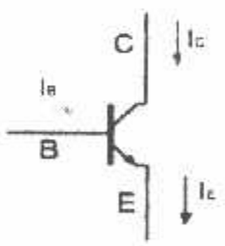
Transistor bipolar dinamakan demikian karena kanal konduksi utamanyamenggunakan dua polaritas pembawa muatan: elektron dan lubang, untuk membawa arus listrik. Dalam BJT, arus listrik utama harus melewati satu

daerah/lapisan pembatas dinamakan depletion zone, dan ketebalan lapisan ini dapat diatur dengan kecepatan tinggi dengan tujuan untuk mengatur aliran arus utama tersebut.

FET (juga dinamakan transistor unipolar) hanya menggunakan satu jenis pembawa muatan (elektron atau hole, tergantung dari tipe FET). Dalam FET, arus listrik utama mengalir dalam satu kanal konduksi sempit dengan depletion zone di kedua sisinya (dibandingkan dengan transistor bipolar dimana daerah Basis memotong arah arus listrik utama). Dan ketebalan dari daerah perbatasan ini dapat dirubah dengan perubahan tegangan yang diberikan, untuk mengubah ketebalan kanal konduksi tersebut. Lihat artikel untuk masing-masing tipe untuk penjelasan yang lebih lanjut.

2.2.2. BJT

BJT (Bipolar Junction Transistor) adalah salah satu dari dua jenis transistor. Cara kerja BJT dapat dibayangkan sebagai dua dioda yang terminal positif atau negatifnya berdempet, sehingga ada tiga terminal. Ketiga terminal tersebut adalah emiter (E), kolektor (C), danbasis (B).



Gambar 2 – 9 Transistor Bipolar NPN[3]

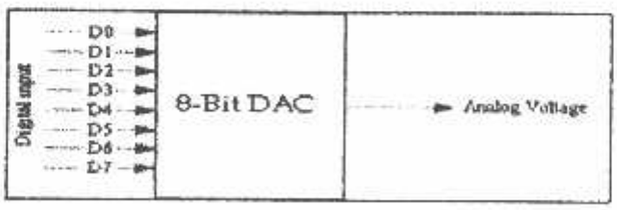
Perubahan arus listrik dalam jumlah kecil pada terminal basis dapat menghasilkan perubahan arus listrik dalam jumlah besar pada terminal kolektor. Prinsip inilah yang mendasari penggunaan transistor sebagai penguat elektronik. Rasio antara arus pada koletor dengan arus pada basis biasanya dilambangkan dengan β atau hFE. β biasanya berkisar sekitar 100 untuk transistor-transisor BJT

2.3. DAC

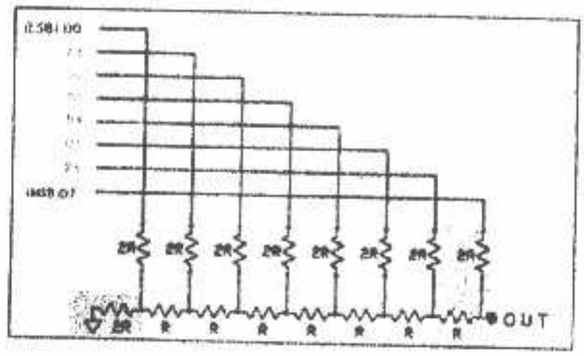
DAC adalah perangkat untuk mengkonversi sinyal masukan dalam bentuk digital menjadi sinyal keluaran dalam bentuk analog (tegangan). Tegangan keluaran yang dihasilkan DAC sebanding dengan nilai digital yang masuk ke dalam DAC.

2.3.1. R/2R sebagai DAC

Sesuai namanya DAC berfungsi untuk mengubah data digital (00110011) menjadi analog 0-5 V. sekarang kita akan membuat 8 bit DAC maksudnya range yang bisa ditangani antara 0 (0000 0000) sampai 255 (1111 1111) yang akan mengasilkan nilai tegangan output 0-5 Volt. sehingga setiap 1 bit bernilai 5/255=0.019 v. sehingga saat input diberi data 129 (1000 0001) pada tegangan output keluar 129 x 0.019=2.451 V



Gambar 2-10 Contoh Aplikasi DAC(10)



Gambar 2-11 Prinsip Kerja R2R(10)

Rangakaian ini sebenarnya merupakan prinsip kerja IC DAC. Digital input masuk melalui D0-D7. R/2R menggunakan 2 macam resistor yang nilainya merupakan 2 x resistor satunya (lihat gambar). contoh 10K dengan 20 K atau 470K dengan 1 M (tidak harus sama persis yang penting tidak terlalu jauh perbedaannya).

DAC R/2R memiliki kelebihan-kelebihan antara lain:

- Tegangan output analog yang dapat diatur antara 5V sampai 34V sesuai yang diinginkan
- Arus output yang lebih besar daripada IC DAC yang lain.
- Menambah atau mengurangi jumlah bit dapat dilakukan dengan mudah tinggal menambah/mengurangi cabang dari resistor

2.4. ADC (ANALOG TO DIGITAL CONVERTER)

ADC digunakan sebagai rangkaian yang mengubah sinyal analog menjadi sinyal digital. Dengan menggunakan ADC, kita dapat mengamati sinyal-sinyal dari perubahan-perubahan sinyal analog seperti perubahan temperature,

kepekatan asap, tekanan udara, kecepatan angin, berat benda, kadar asam (pH), dan lain-lain yang semuanya dapat diamati melalui sensornya masing-masing. Hal yang paling penting dalam suatu rangkaian ADC adalah resolusi, yaitu besaran analog terkecil yang masih dapat dikonversi menjadi satuan digital.

Resolusi (r) = ((1 / (2 pangkat n)) * Vref

Dimana : n banyaknya bit ADC; Vref = tegangan referensi yang digunakan

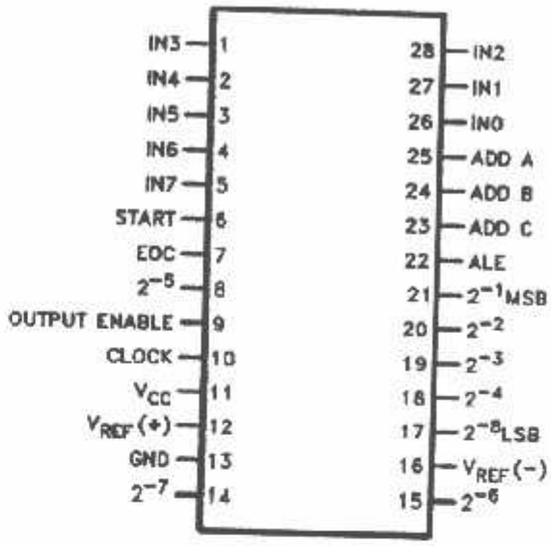
2.4.1. ADC 0808

ADC 0808 merupakan konverter A/D 8 bit yang dapat mengkonversi data input sebanyak 8 sinyal, sehingga dapat menerima 8 buah tranduser yang berbeda untuk setiap chipnya. Jika pada ADC 0808 ini diberikan tegangan referensi +5V maka resolusinya adalah 20 mV (untuk menghitungnya, gunakan rumus diatas).

Dalam menggunakan ADC 0808 ini pada sistem, hal penting yang perlu diperhatikan adalah pengaktifan/pengkonversian ADC yang harus selalu dilakukan ketika data dari sensor akan dibaca oleh mikroprosesor. Adapun langkah-langkah pengkonversian pada ADC 0808 ini adalah :

1. Aktifkan ADC.
2. RD dan WR diberi logic 1, dimana WR dan RD merupakan keluaran dari PortC0 dan PortC1 yang telah dikombinasikan pada gerbang NOR (Anda dapat melihat rangkaiannya di data book ADC 0808 pada perancangan hasil penulis yang telah di download).
3. WR diberi logic 0 kemudian diberi logic 1
4. RD diberi logic 0

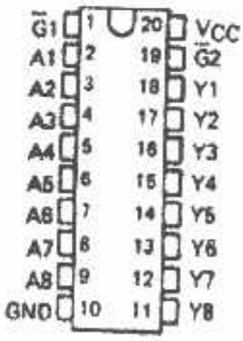
5. Maka pada langkah ini terjadi konversi besaran analog ke digital



Gambar 2-12 Konfigurasi Pin ADC 0808 (6)

2.5. Buffer

Rangkaian buffer disini berfungsi untuk menguatkan sinyal clock dan sinkronisasi agar cukup kuat untuk ditransmisikan. Rangkaian buffer harus memiliki impedansi keluaran yang cukup rendah dan Arus keluaran juga harus cukup besar. Output buffer selain untuk pulsa dan sinyal sinkronisasi dapat juga digunakan sebagai sumber catu.



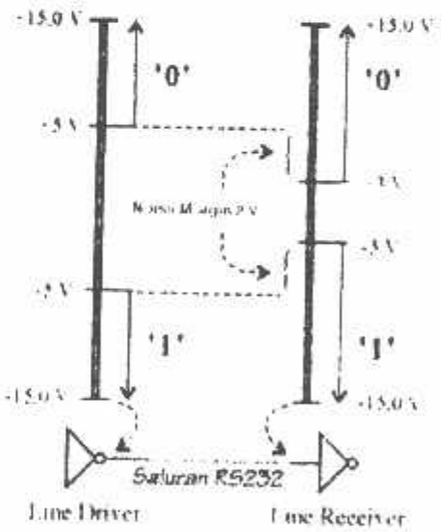
Gambar 2-13 IC 74LS541 (6)

Ada 3 hal pokok yang diatur standard RS232, antara lain adalah :

1. Bentuk sinyal dan level tegangan yang dipakai
2. Penentuan jenis sinyal dan konektor yang dipakai, serta susunan sinyal pada kaki-kaki di konektor
3. Penentuan tata cara pertukaran informasi antara komputer dan alat-alat pelengkapnya.

2.6.1. Karakteristik sinyal RS232

Karakteristik sinyal yang diatur meliputi level tegangan sinyal, kecuraman perubahan tegangan (slew rate) dari level tegangan '0' menjadi '1' dan sebaliknya, serta impedansi dari saluran yang dipakai. RS232 dibuat pada tahun 1962, jauh sebelum IC TTL populer, maka level tegangan yang ditentukan untuk RS232 tidak ada hubungannya dengan level tegangan TTL, bahkan jauh berbeda!



Gambar 2 – 15 Level Teganagn RS32[8]

- Dalam standard RS232, tegangan antara +3 sampai +15 Volt pada input Line Receiver dianggap sebagai level tegangan '0', dan tegangan antara –3 sampai –15 Volt dianggap sebagai level tegangan '1'.
- Agar output Line Driver bisa dihubungkan dengan baik, tegangan output Line Driver berkisar antara +5 sampai +15 Volt untuk menyatakan level tegangan '0', dan berkisar antara –5 sampai –15 Volt untuk menyatakan level tegangan '1'

Beda tegangan sebesar 2 Volt ini disebut sebagai ***noise margin*** dari RS232.

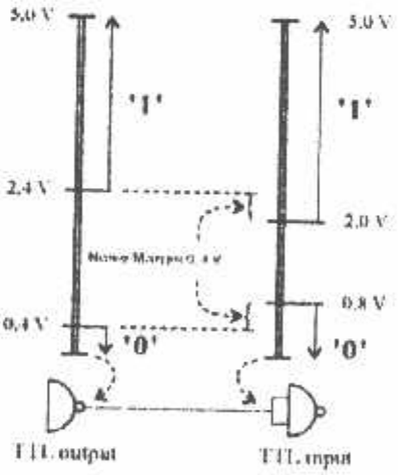
Untuk mengurangi kemungkinan terjadinya gangguan 'cross talk' antara kabel saluran sinyal RS232, kecuraman perubahan tegangan sinyal dibatasi tidak boleh lebih dari 30 Volt/mikro-detik. (Makin besar kecuraman sinyal, makin besar pula kemungkinan terjadi 'cross talk'). Di samping itu ditentukan pula kecepatan transmisi data seri tidak boleh lebih besar dari 20 KiloBit/Detik. Impedansi saluran dibatasi antara 3 Kilo-Ohm sampai 7 Kilo-Ohm. dalam standard RS232 yang pertama ditentukan pula panjang kabel tidak boleh lebih dari 15 Meter (50 feet), tapi ketentuan ini sudah di-revisi pada standard RS232 versi 'D'. Dalam ketentuan baru tidak lagi ditentukan panjang kabel maksimum, tapi ditentukan nilai kapasitan dari kabel tidak boleh lebih besar dari 2500 pF, sehingga dengan menggunakan kabel kwalitas baik bisa dicapai jarak yang lebih dari 50 feet.

2.6.2. Menghubungkan TTL ke RS232

IC digital, termasuk mikrokontroler, umumnya bekerja pada level tegangan TTL, yang dibuat atas dasar tegangan catu daya +5 Volt.

- Rangkaian input TTL menganggap tegangan kurang dari 0,8 Volt sebagai level tegangan '0' dan tegangan lebih dari 2.0 Volt dianggap sebagai level tegangan '1'. Level tegangan ini sering dikatakan sebagai level tegangan TTL.
- Untuk menjamin output bisa diumpankan ke input dengan baik, tegangan output TTL saat level '0' dijamin lebih rendah dari 0,4 Volt, atau 0,4 lebih rendah dari tegangan yang dituntut oleh input TTL. Sedangkan tegangan output TTL pada saat level '1' dijamin lebih tinggi dari 2,4 Volt, atau 0,4 Volt lebih tinggi dari tegangan yang dituntut oleh input TTL.

Beda tegangan sebesar 0,4 Volt ini disebut sebagai ***noise margin*** dari TTL.



Gambar 2 – 16 Level Tegangan TTL[8]

2.7. Visual Basic

Visual Basic adalah salah satu development tools untuk membangun aplikasi dalam bidang windows. Visual basic merupakan bahasa pemrograman tingkat tinggi yang merupakan pengembangan dari bahasa BASIC versi DOS. Dalam pengembangan aplikasi, visual basic menggunakan pendekatan visual untuk merancang user interface dalam bentuk form, sedangkan untuk coding menggunakan bahasa basic yang cenderung mudah untuk dipelajari. Pada pemrograman visual, pengembangan aplikasi dimulai dengan pembentukan user interface dengan mengatur form sesuai dengan yang diinginkan, kemudian mengatur properti dari objek – objek yang digunakan pada user interface. Setelah tampilan form sudah sesuai dengan yang diinginkan dan properti sudah diatur, saatnya melakukan penulisan kode program untuk menangani kejadian – kejadian (event).

Sebelum kita melangkah lebih jauh, kita harus melihat beberpa keterbatasan dalam VB. Karena VB tidak dapat mengakses hardware secara langsung dalam sistem operasi Windows, maka semua permintaan pengaksesan hardware harus melalui windows. Mungkin kita dapat menggunakan windows API untuk melakukan ini, tetapi susah untuk menemukan fungsi yang disediakan oleh windows API untuk melaksanakan tugas tersebut. Oleh karena itu maka dibutuhkan sebuah program eksternal untuk melakukan pengaksesan hardware secara langsung yang biasa disebut DLL (Dynamic Link Library).

BAB III

PERANCANGAN DAN PEMBUATAN ALAT

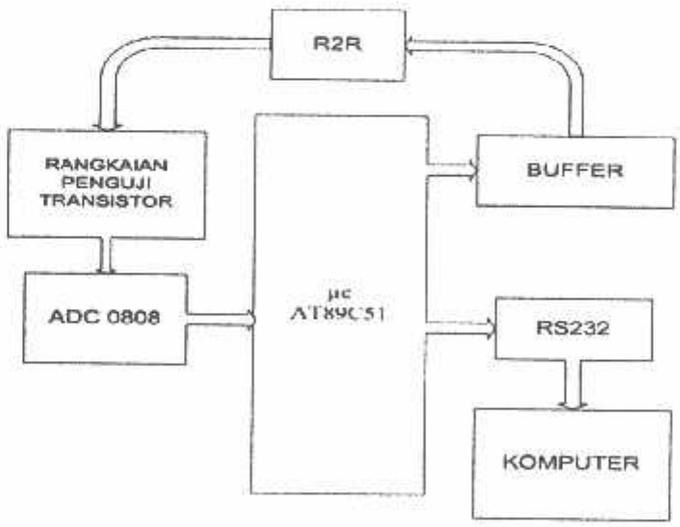
Perencanaan dan pembuatan alat untu menampilkan karakteristik kurva tracer ransistor bipolar tmenggunakan mikrokontroller AT89C51, dimaksudkan untuk lebih memahami karakteristik dari sebuah transistor.

Parameter yang digunakan untuk mewujudkan sistem agar dapat bekerja dengan baik yaitu:

1. Menggunakan Mikrokontroller AT89C51 sebagai pengontrol yang diprogram untuk mengontrol alat sesuai yang kita inginkan.
2. Menggunakan program visual basic sebagai program pendukung untuk menampilkan kurva pada computer

3.1. Blok Diagram Rangkaian

Blok rangkaian dari alat ini ditunjukkan dalam gambar berikut ini:



Gambar 3-1. Diagram Blok Alat

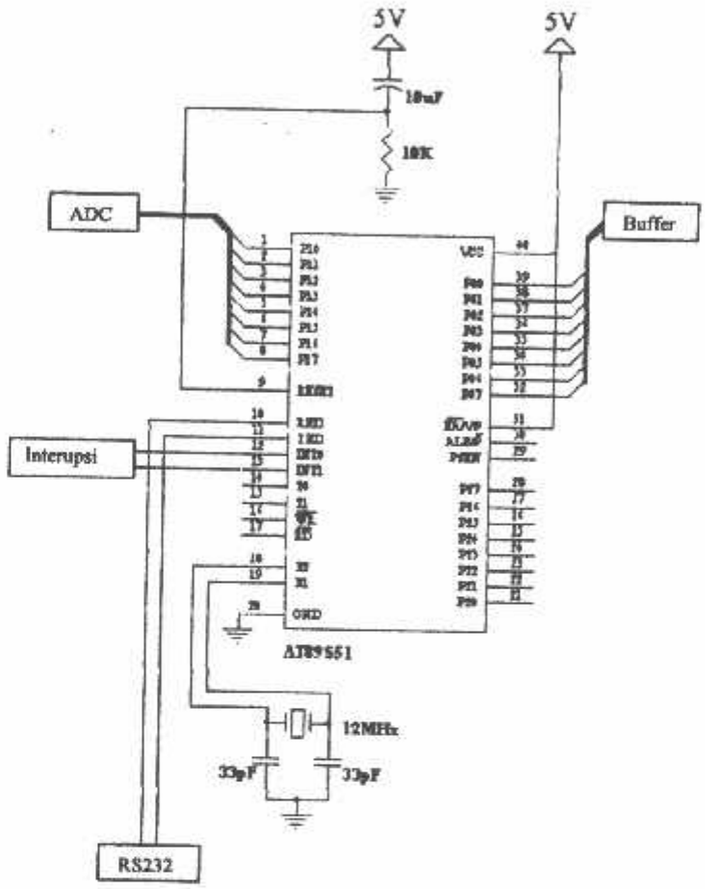
Fungsi dari masing – masing blok diagram adalah sebagai berikut :

1. Mikrokontroller berfungsi sebagai pengendali kesceluruhan system. Mikrokontroller akan memproses input yang telah diberikan dan mengendalikan output yang diinginkan.
2. Buffer berfungsi sebagai penyangga atau penguat tegangan yang dikeluarkan mikrokotroler agar mampu mengaktifkan rangkaian transistor
3. DAC berfungsi untuk merubah nilai tegangan dari besaran digital menjadi analog untuk mengaktifkan rangkaian transistor.
4. Rangkaian transistor berfungsi untuk mengaktifkan transistor sehingga transistor dapat bekerja
5. ADC berfungsi untuk merubah besaran besaran analog yang dikeluarkan rangkaian transistor menjadi besaran digital agar bisa dibaca mikrokontroler.
6. RS232 sebagai penghubung antara alat dengan komputer.
7. PC berfungsi untuk menampilkan kurva kerakteristik

Berdasarkan diagram blok diatas, maka prinsip kerja dari alat tersebut dapat dijelaskan sebagai berikut:

AT89C51 sebagai pengontrol utama, yang mengatur seluruh system. saat diinputkan sebuah nilai, dalam hal ini adalah nilai tahanan maka nilai ini akan diproses oleh mikrokontroller kemudian dibuffer dan dirubah nilainya menjadi analog. Nilai – nilai ini akan masuk kerangkaian transistor sehingga mempengaruhi nilai tegangan dan arusnya. Selanjutnya nilai – nilai ini akan dirubah menjadi digital dan dimasukkan kemikrokontroller. Nilai – nilai yang

- Pin 29 – 30 / Port (ALE/PROG dan PSEN) Tidak digunakan karena pada pembuatan alat ini tidak menggunakan atau mengakses *memory external*
- Pin 31 & Pin 40 (Vcc) dihubungkan dengan tegangan supply +5Volt
- Pin 32 – 39 / Port (0.0 – 0.7) Digunakan sebagai output keluaran



Gambar 3 - 2
Minimum Sistem Mikrokontroler AT89C51(1)

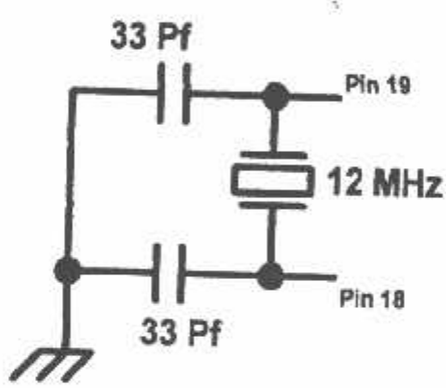
3.2.1.1. Rangkaian Clock Minimum System

Kecepatan proses pengolahan data pada mikrokontroller ditentukan oleh clock (pewaktu) yang dikendalikan oleh mikrokontroller tersebut. Pada

mikrokontroller AT89C51 terdapat internal clock. Internal clock generator berfungsi sebagai sumber clock, tapi masih memerlukan rangkaian tambahan untuk membangkitkan clock yang diperlukan. Rangkaian clock ini terdiri dari dua buah kapasitor dan sebuah kristal yang dirangkai sedemikian rupa dan kemudian dihubungkan dengan Pin 18 dan 19 pada AT 89C51.

Dalam perancangan rangkaian ini menggunakan.

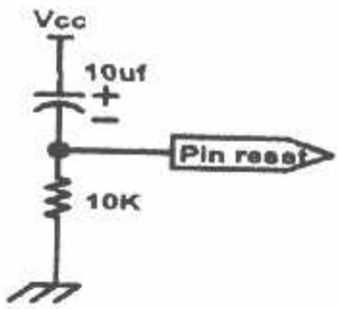
1. C= 33 pF.Penentuan besarnya kapasitansi disesuaikan dengan spesifikasi pada data sheet AT 89C51.
2. Kristal 12 MHZ (berdasarkan data sheet AT89C51) adapun gambar rangkaian clock tampak seperti pada gambar 3-3.



Gambar 3-3 Rangkaian Clock Miinimum Sistem(1)

3.2.3. Rangkaian Reset

Reset pada Mikrokontroller merupakan masukkan aktif High '1' Pulsa transisi dari rendah '0' ketinggi '1' akan mereset Mikrokontroller menuju alamat 0000H. Pin reset dihubungkan dengan rangkaian power on reset seperti pada gambar 3-4.



Gambar 3-4. Rangkaian Power On Reset (1)

Rangkaian reset bertujuan agar mikrokontroller dapat menjalankan proses dari awal. Rangkaian reset untuk mikrokontoller dirancang agar mempunyai kemampuan power on reset, yaitu reset yang terjadi pada saat system dinyalakan untuk pertama kalinya. Reset juga dapat dilakukan secara manual dengan menekan tombol reset yang berupa switch push button.

Rangkaian Reset terbentuk oleh komponen R dan C yang sudah baku (ditetapkan oleh perusahaan pembuat IC AT 89C51). Nilai R yang dipakai adalah 10 Kohm dan C =10 μF.

Sedangkan untuk mencari frekuensi dari reset tersebut dengan menggunakan rumus sebagai berikut :

$$Fo = \frac{1}{1{,}1R.C}$$

Sehingga dengan komponen resistor dengan nilai 10 Kohm serta kapasitor dengan nilai 10 μF akan dihasilkan frekuensi.

$$fo = \frac{1}{1{,}1.RC}$$

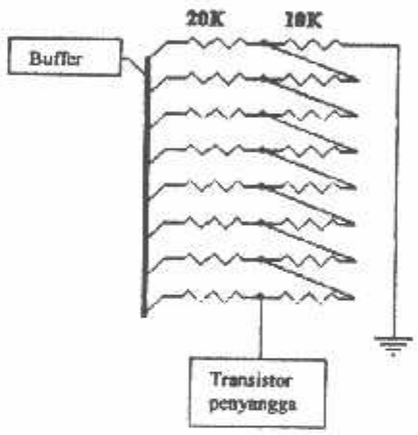
$$= \frac{1}{1{,}1.10^{1}.10^{-6}}$$

$$fo = 9{,}09Hz$$

Karena konverter digital ke analog ini banyak macamnya, maka pada umumnya dipakai cara konversi dengan rangkaian resistor berbobot (binary weighted resistor) dimana posisi dari bit digital yang akan diberikan akan menghasilkan besar arus tegangan yang sesuai bobot biner pada data digital. Didalam penerapannya, cara pemakaian harga tahanan yang bervariasi akan menimbulkan kesulitan dalam memilih harga tahanan yang sesuai, sehingga dipakai rangkaian tangga tahanan R-2R yang lebih sederhana.

Tahanan keluaran Vout dapat dihitung dengan rumus berikut;

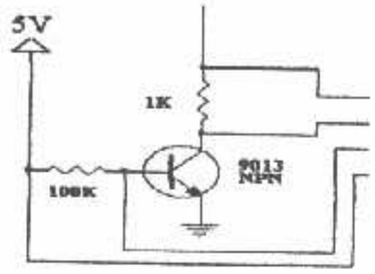
$$\text{Vout} = - \quad \frac{Rf}{R} Vref\left(\frac{D_0}{2^n} + \frac{D_1}{2^{n-1}} + \frac{D_2}{2^{n-2}}\right) - \left(\frac{D_{(n-2)}}{2^2} + \frac{D_{(n-1)}}{2^1}\right)$$



Gambar 3 – 6 Rangkaian DAC R-2R (Digital Analog Converter)(3)

3.2.4. Perancangan Rangkaian Transistor

Dalam perancangan alat ini rangkaian transistor merupakan rangkaian vital, karena pada rangkaian inilah yang menentukan bahwa grafik yang ditampikan benar atau tidak. Dalam rangkaian ini transistor yang digunakan adalah tipe NPN 9013.



Gambar 3-7 Rangkaian Transistor (4)

Dari gambar diatas dapat dijelaskan Vcc diberi tegangan variable sampai tegangan maksimal yang dapat dikeluarkan DAC. Vbb diberikan tegangan tetap yaitu sebesar 5Volt dan dengan merubah besarnya tahanan Rb. Penggantian besarnya tahanan Rb bertujuan untuk melihat perubahan grafik karena transistor sangat berpengaruh terhadap perubahan nilai arus.

3.2.4.1. Daerah Aktif

Daerah kerja transistor yang normal adalah pada daerah aktif, dimana arus I_C konstans terhadap berapapun nilai V_{CE}. Dari kurva ini diperlihatkan bahwa arus I_C hanya tergantung dari besar arus I_B. Daerah kerja ini biasa juga disebut daerah linear (*linear region*).

Jika hukum Kirchhoff mengenai tegangan dan arus diterapkan pada loop kolektor (rangkaian CE), maka dapat diperoleh hubungan :

$$V_{CE} = V_{CC} - I_C R_C \quad \text{..... (6)}$$

Dapat dihitung dissipasi daya transistor adalah :

$$P_D = V_{CE} I_C \quad \text{..... (7)}$$

Rumus ini mengatakan jumlah dissipasi daya transistor adalah tegangan kolektor-emitor dikali jumlah arus yang melewatinya. Dissipasi daya ini

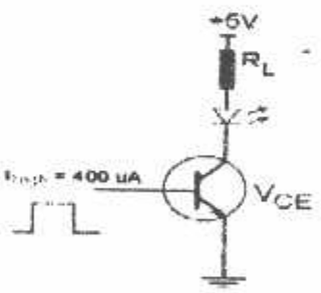
berupa panas yang menyebabkan naiknya temperatur transistor. Umumnya untuk transistor power sangat perlu untuk mengetahui spesifikasi $P_D$max. Spesifikasi ini menunjukkan temperatur kerja maksimum yang diperbolehkan agar transistor masih bekerja normal. Sebab jika transistor bekerja melebihi kapasitas daya $P_D$max, maka transistor dapat rusak atau terbakar.

3.2.4.2. Daerah Saturasi

Daerah saturasi adalah mulai dari V_{CE} = 0 volt sampai kira-kira 0.7 volt (transistor silikon), yaitu akibat dari efek dioda kolektor-base yang mana tegangan V_{CE} belum mencukupi untuk dapat menyebabkan aliran elektron.

3.2.4.3. Daerah Cut-Off

Jika kemudian tegangan V_{CC} dinaikkan perlahan-lahan, sampai tegangan VCE tertentu tiba-tiba arus IC mulai konstan. Pada saat perubahan ini, daerah kerja transistor berada pada daerah cut-off yaitu dari keadaan saturasi (OFF) lalu menjadi aktif (ON). Perubahan ini dipakai pada system digital yang hanya mengenal angka biner 1 dan 0 yang tidak lain dapat direpresentasikan oleh status transistor OFF dan ON.



Gambar 3 – 8 *Rangkaian driver LED*[3]

Misalkan pada rangkaian driver LED di atas, transistor yang digunakan adalah transistor dengan □ = 50. Penyalaan LED diatur oleh sebuah gerbang logika (*logic gate)* dengan arus *output high* = 400 uA dan diketahui tegangan forward LED, V_{LED} = 2.4 volt. Lalu pertanyaannya adalah, berapakah seharusnya resistansi R_L yang dipakai.

$I_C = \square I_B = 50 \times 400\ uA = 20\ mA$

Arus sebesar ini cukup untuk menyalakan LED pada saat transistor *cut-off.* Tegangan V_{CE} pada saat *cut-off* idealnya = 0, dan aproksimasi ini sudah cukup untuk rangkaian ini.

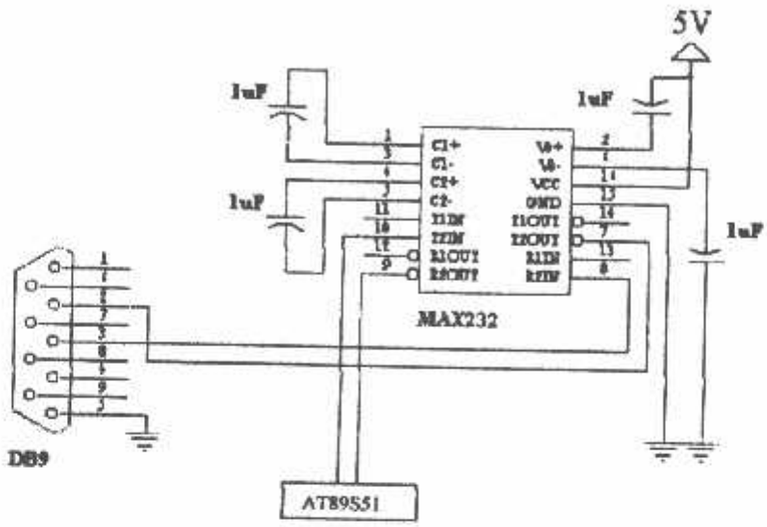
$R_L = (V_{CC} - V_{LED} - V_{CE}) / I_C$
$= (5 - 2.4 - 0)V / 20\ mA$
$= 2.6V / 20\ mA$
$= 130\ Ohm$

3.2.4.4. Daerah Breakdown

Dari kurva kolektor, terlihat jika tegangan V_{CE} lebih dari 40V, arus I_C menanjak naik dengan cepat. Transistor pada daerah ini disebut berada pada daerah breakdown. Seharusnya transistor tidak boleh bekerja pada daerah ini, karena akan dapat merusak transistor tersebut. Untuk berbagai jenis transistor nilai tegangan $V_{CE}max$ yang diperbolehkan sebelum breakdown bervariasi. $V_{CE}max$ pada databook transistor selalu dicantumkan juga.

3.2.6. Perancangan Rangkaian Serial RS232

Rangkaian serial RS232 ini berfungsi untuk komunikasi data antara alat dan komputer sehingga bisa saling mengirim dan menerima data



Gambar 3 – 10 Rangkaian RS-232 (8)

Untuk mengirim data dari mikrokontroller ke komputer ialah menggunakan system duplex. Baud rate yang digunakan ialah 9600bps atau dapat dipakai yang lain asal sinkron baik komputer maupun mikrokontroller. Pada konektor serial ini yang dipakai hanya 3 pin saja yaitu TX, RX dan Ground.

Rangkaian converter Max232 digunakan untuk mengubah level tegangan TTL menjadi level tegangan RS-232 maupun sebaliknya.IC Max232 memiliki charge pump yang akan membangkitkan tegangan +10Volt & -10Volt dari sumber +5Volt tunggal.

Penggunaan pin pada perancangan rangkaian IC Max232

- pin 7 pada Max232 dihubungkan ke konektor DB9 pada pin 2 (TX) untuk mengirimkan data dari mikrokontroller ke komputer.

- Pin 8 pada Max232 dihubungkan ke konektor DB9 pada pin 3 (RX) untuk menerima data dari komputer ke mikrokontroller.
- Pin 9 pada Max232 dihubungkan ke port 3.0 (RXD) mikrokontroller yang digunakan sebagai modem untuk menerima data dari komputer.
- Pin 10 pada Max232 dihubungkan ke port 3.1 (TXD) mikrokontroller untuk mengirim data ke komputer
- Pin 16 pada Max232 dihubungkan dengan tegangan supply +5Volt (Vcc)
- Pin 15 pada Max232 dihubungkan dengan ground (GND)

3.3. Perancangan Perangkat Lunak

Dalam menunjang kerja sistem secara keseluruhan diperlukan suatu perangkat lunak (*software*). *Software* yang digunakan untuk AT89C51 disini menggunakan bahasa *assembler* keluarga MCS51. Program yang ditulis dengan bahasa assembly terdiri dari *label: kode mnemonic* dan lain sebagainya yang pada umumnya dinamakan sebagai program sumber (*source code*) yang belum bisa diterima oleh prosesor untuk dijalankan sebagai program, tetapi harus dijalankan dulu menjadi bahasa mesin dalam bentuk *kode biner*.

- Penulisan program dengan menggunakan teks editor dan disimpan dengan ekstensi *Asm*.
- Meng-compile program yang telah ditulis dengan menggunakan Compiler MCS52 sehingga didapatkan file dengan ekstensi *Hex*.
- Mengubah file berekstensi *Hex* menjafi file berekstensi *Bin*.
- Men-download file berekstensi Bin ke dalam EPROM Mikrokontroler AT89C51.

BAB IV

PENGUJIAN ALAT

Untuk mengetahui keberhasilan dari alat yang dirancang apakah dapat bekerja sesuai dengan yang diharapkan, maka diperlukan pengujian terhadap alat tersebut. Pada pengujian ini dilakukan sejumlah percobaan untuk mengetahui sistem kerja alat secara keseluruhan.

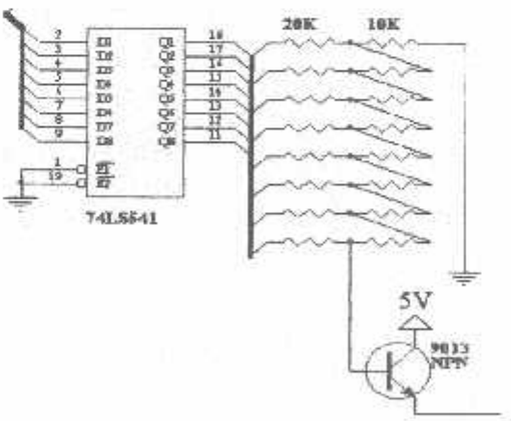
4.1 Pengujian Rangkaian DAC R2R

4.1.1 Tujuan Pengujian

Untuk mengetahui apakah rangkaian DAC yang telah dibuat dapat bekerja sesuai dengan yang diharapkan dan untuk mengetahui sinyal keluaran yang dihasilkan.

4.1.2 Langkah – Langkah Pengujian

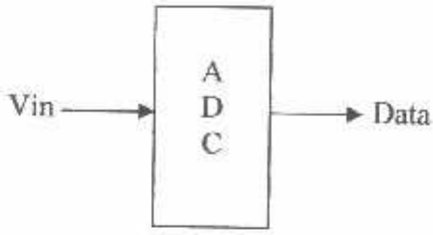
1. Menyusun rangkaian DAC R2R
2. Menghubungkan kutub positif multimeter pada output DAC dan kutub negatif ke ground
3. Mengamati perubahan nilai tegangan



Gambar 4 – 1 Rangkaian pengujian DAC

1 Volt

3. mengamati perubahan nilai untuk tiap – tiap masukan



Gambar 4 – 2 Rangkaian pengujian ADC

4.2.3 Hasil dan Analisa

Setelah melakukan pengujian terhadap rangkaian ADC (analog to digital converter) maka hasil yang diperoleh adalah seperti yang ditunjukkan pada tabel 4-2 sebagai berikut:

Vin (Volt)	Data (Des)	Data (Hex)
0	0	00
1	51	33
2	103	67
3	155	9B
4	208	D0
5	255	FF

Tabel 4 – 2 Data keluaran DAC

4.2.4. Analisa Data

Dari data hasil pengujian dapat diketahui bahwa resolusi tegangan adalah $\frac{5}{255} = 0{,}0196$ Volt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BAB V

Kesimpulan dan Saran

5.1. Kesimpulan

Dari hasil perencanaan dan pembuatan alat dapat diambil kesimpulan yaitu:

1. Minimum sistem mikrokontroller AT89C51 mampu menerima, mengolah dan mengeluarkan data dengan benar sesuai algoritma program
2. Untuk mendapatkan hasil konversi yang bagus pada rangkaian ADC hendaknya memperhatikan Vref, karena Vref berpengaruh pada resolusi konversimya.
3. Titik kerja merupakan pertemuan Ic terhadap Vce pada garis beban
4. Posisi titik kerja ditentukan oleh nilai Vce
5. Ada 3 jenis keadaan transistor bipolar yang ditentukan oleh titik kerja
   - Aktif (menghantar)
   - Saturasi (jenuh)
   - Cut off (tersumbat)

5.2.Saran

Adapun saran dari penulis agar tercapai efisiensi dan perkembangan alat ini antara lain:

1. Agar nilainya akurat maka yang paling utama perlu diperhatikan adalah rangkaian ADC dan DAC

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FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI T. ELEKTRONIKA

LEMBAR BIMBINGAN SKRIPSI

Nama	: Denny Tri Prayogo
Nim	: 9917255
Jurusan	: T. Elektro S-1
Konsentrasi	: T Elektronika
Judul	: Perencanaan dan Pembuatan Alat Untuk Menampilkan Karakteristik Kurva Tracer Transistor Bipolar Berbasis Mikrokontroller AT89C51
Tanggal Pengajuan Skripsi	: 15 Januari 2009
Selesai Pengajuan Skripsi	: 19 Juli 2009
Dosen Pembimbing	: Ir. F Yudi Limpraptono, MT
Dievaluasi Dengan Nilai	:85 (A)

Mengetahui,
Ketua Jurusan T. Elektro S-1

(Ir. F. Yudi Limpraptono, MT)
NIP.Y. 1039500274

Diperiksa dan Disetujui,
Dosen Pembimbing

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INSTITUT TEKNOLOGI NASIONAL
FAKULTAS TEKNOLOGI INDUSTRI
JURUSAN TEKNIK ELEKTRO S-1
KONSENTRASI T. ELEKTRONIKA

FORMULIR PERBAIKAN SKRIPSI

Nama : Denny Tri Prayogo
Nim : 9917255
Masa Bimbingan : 19 Januari 2009 – 19 Juli 2009
Judul : Perencanaan dan Pembuatan Alat Untuk Menampilkan Karakteristik Kurva Tracer Transistor Bipolar Berbasis Mikrokontroller AT89C51

No	Tanggal	Materi Perbaikan	Paraf
1		- Perbaiki Abstrak	
2		- Perbaiki batasan masalah	
3		- Perbaiki identitas gambar & table	
4		- Perbaiki blok diagram	
5		- Perbaiki gambar lengkap pada lampiran	

Disetujui
Penguji 1

(Ir. Eko Nurcahyo, MT)
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Mengetahui
Dosen Pembimbing

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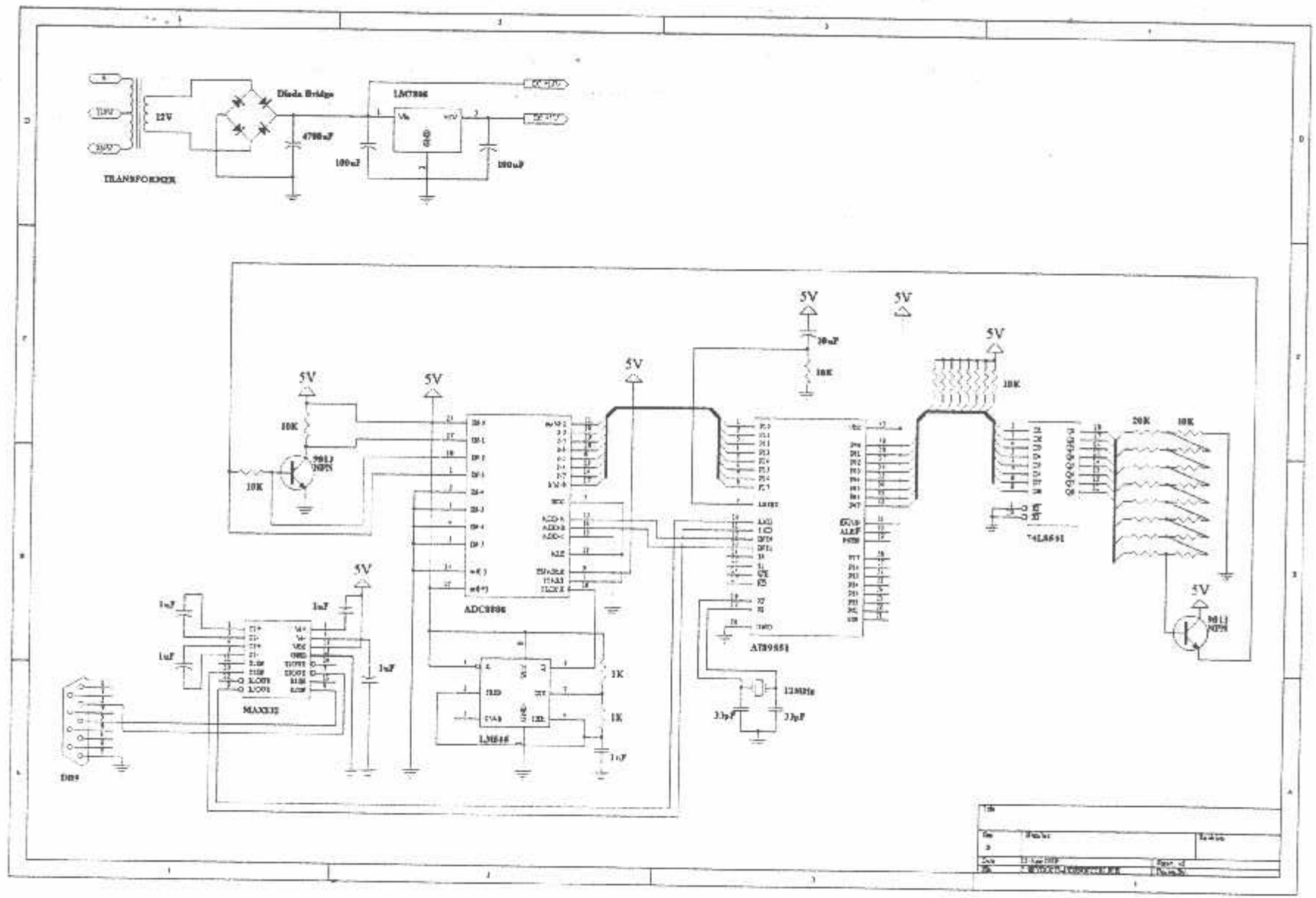
LAMPIRAN


TRANSFORMER
12V
Diode Bridge
LM7806
4700uF
100uF
100uF
5V
10K
9013
NPN
ADC0804
MAX232
DB9
1uF
1K
33pF
12MHz
AT89S51
74LS573
20K

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (5-volt) program enable signal. The low-voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third-party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	V_{PP} = 12V	V_{PP} = 5V
Top-side Mark	AT89C51	AT89C51
	xxxx	xxxx-5
	yyww	yyww
Signature	(030H) = 1EH	(030H) = 1EH
	(031H) = 51H	(031H) = 51H
	(032H) = FFH	(032H) = 05H

The AT89C51 code memory array can be programmed byte-by-byte in either programming mode. To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase mode.

Programming Algorithm: Before programming the AT89C51, the address, data, and control signals should be set up according to the Flash programming mode table and Figure 3 and Figure 4. To program the AT89C51, the following sequence is recommended.

1. With the desired memory location on the address lines...
2. ...apply the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}$/V_{PP} to the programming voltage (high-voltage mode).
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1's". The chip erase operation must be executed before the code memory can be reprogrammed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

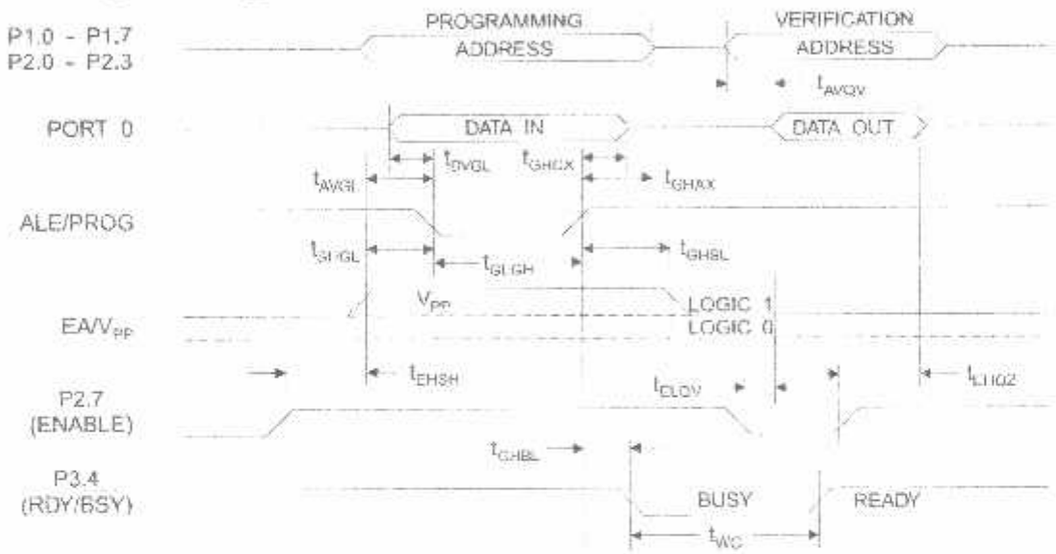
(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates AT89C51
(032H) = 05H indicates 12V programming
(032H) = 85H indicates 5V programming

Programming Interface

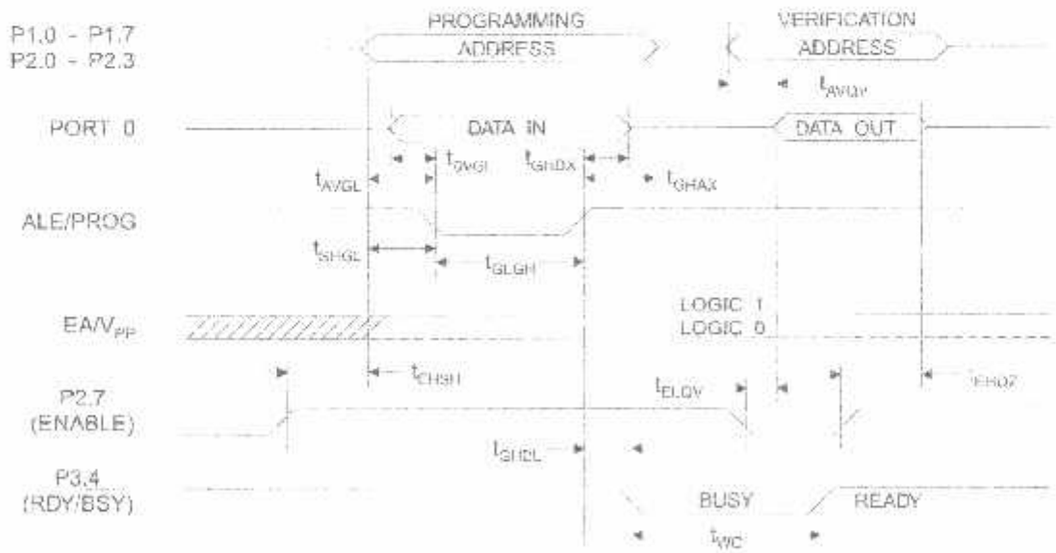
Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming and Verification Waveforms - High-voltage Mode (V_{PP} = 12V)



Flash Programming and Verification Waveforms - Low-voltage Mode (V_{PP} = 5V)



Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}[1]	Programming Enable Voltage	11.5	12.5	V
I_{PP}[1]	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to PROG Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold after PROG	$48t_{CLCL}$		
t_{DVGL}	Data Setup to PROG Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold after PROG	$48t_{CLCL}$		
t_{EHSH}	P2.7 (ENABLE) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to PROG Low	10		µs
t_{GHSL}[1]	V_{PP} Hold after PROG	10		µs
t_{GLGH}	PROG Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	ENABLE Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float after ENABLE	0	$48t_{CLCL}$	
t_{GHBL}	PROG High to BUSY Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except EA)	-0.5	$0.2V_{CC}$ - 0.1	V
V_{IL1}	Input Low-voltage (EA)		-0.5	$0.2V_{CC}$ - 0.3	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	$0.2V_{CC}$ + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	$0.7V_{CC}$	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low-voltage[1] (Port 0, ALE, PSEN)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High-voltage (Ports 1,2,3, ALE, PSEN)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	$0.75V_{CC}$		V
		I_{OH} = -10 µA	$0.9V_{CC}$		V
V_{OH1}	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	$0.75V_{CC}$		V
		I_{OH} = -80 µA	$0.9V_{CC}$		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, EA)	$0.45 < V_{IN} < V_{CC}$		±10	µA
R_{RST}	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power-down Mode[2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

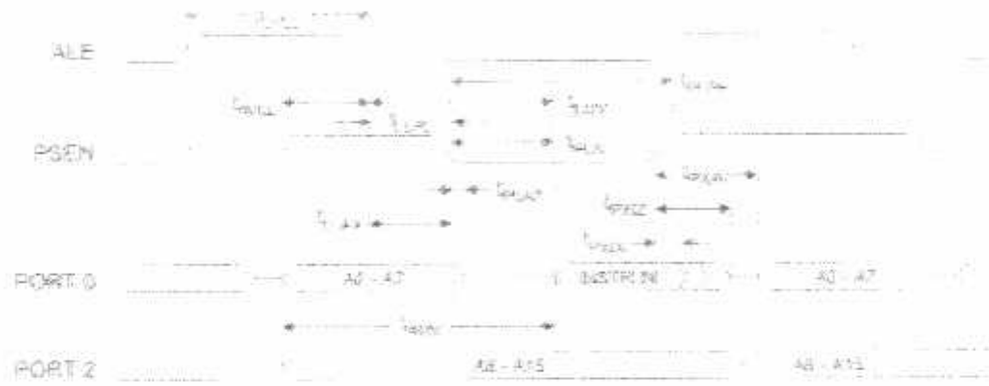
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.

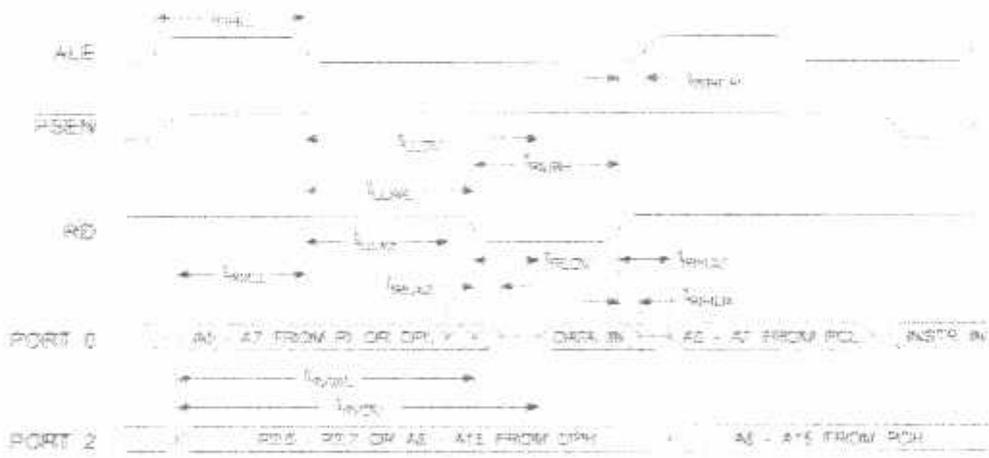
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-13		ns
t_{LLAX}	Address Hold after ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	PSEN Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float after $\overline{PSEN}$		59		t_{CLCL}-10	ns
t_{PXAV}	PSEN to Address Valid	75		t_{CLCL}-5		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	RD Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float after $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold after $\overline{WR}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	13	133	t_{CLCL}-20	t_{CLCL}+25	ns

External Program Memory Read Cycle



External Data Memory Read Cycle



Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ±20%	AT89C51-12AC AT89C51-12JC AT89C51-12PC AT89C51-12QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
		AT89C51-12AI AT89C51-12JI AT89C51-12PI AT89C51-12QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
16	5V ±20%	AT89C51-16AC AT89C51-16JC AT89C51-16PC AT89C51-16QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
		AT89C51-16AI AT89C51-16JI AT89C51-16PI AT89C51-16QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
20	5V ±20%	AT89C51-20AC AT89C51-20JC AT89C51-20PC AT89C51-20QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
		AT89C51-20AI AT89C51-20JI AT89C51-20PI AT89C51-20QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
24	5V ±20%	AT89C51-24AC AT89C51-24JC AT89C51-24PC AT89C51-24QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
		AT89C51-24AI AT89C51-24JI AT89C51-24PI AT89C51-24QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44-lead, Plastic Gull Wing Quad Flatpack (PQFP)

July 2005

National Semiconductor

LM555
Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

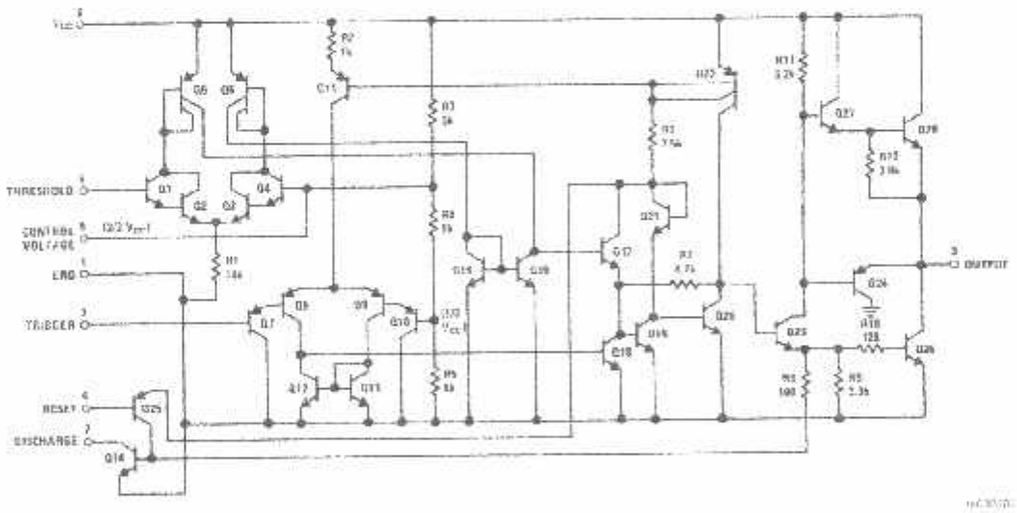
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

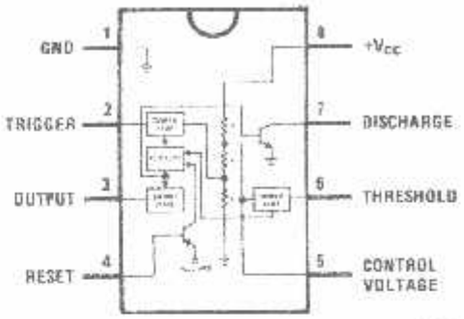
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Connection Diagram

Dual-In-Line, Small Outline
and Molded Mini Small Outline Packages



Top View

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Packages	
(SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

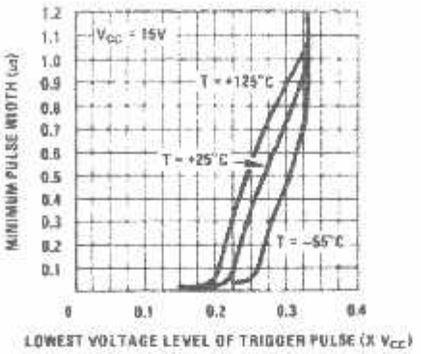
Electrical Characteristics (Notes 1, 2)

(T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

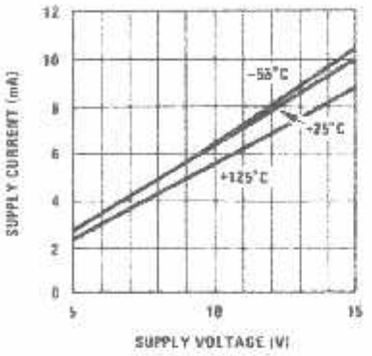
Parameter	Conditions	Limits LM555C			Units
		Min	Typ	Max	
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞ (Low State) (Note 4)		3 10	5 15	mA
Timing Error, Monostable					
Initial Accuracy			1		%
Drift with Temperature	R_A = 1k to 100kΩ, C = 0.1µF, (Note 5)		50		ppm/°C
Accuracy over Temperature			1.5		%
Drift with Supply			0.1		%/V
Timing Error, Astable					
Initial Accuracy			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100kΩ, C = 0.1µF, (Note 5)		150		ppm/°C
Accuracy over Temperature			3.0		%
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V		5		V
	V_{CC} = 5V		1.67		V
Trigger Current			0.5	0.9	µA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V	9	10	11	V
	V_{CC} = 5V	2.6	3.33	4	
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat (Note 7)					
Output Low	V_{CC} = 15V, I_7 = 15mA		180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5mA		80	200	mV

Typical Performance Characteristics

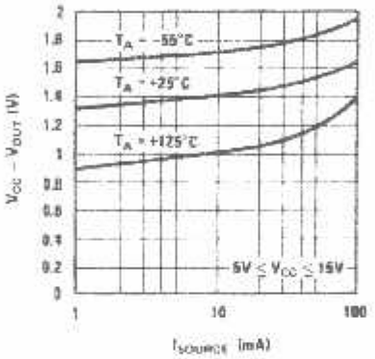
Minimum Pulse Width Required for Triggering



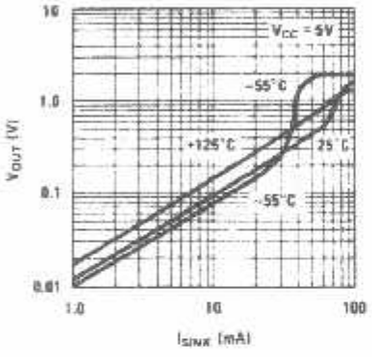
Supply Current vs. Supply Voltage



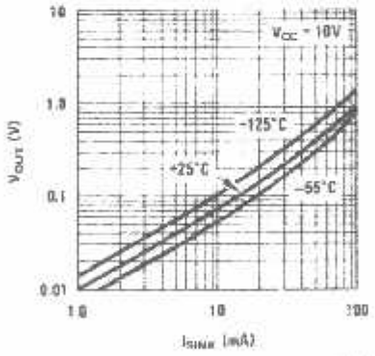
High Output Voltage vs. Output Source Current



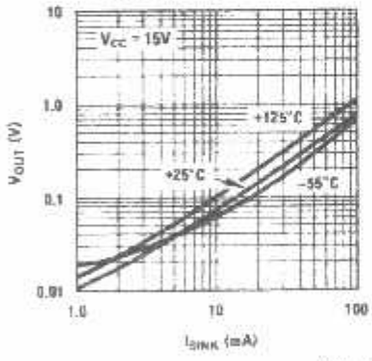
Low Output Voltage vs. Output Sink Current



Low Output Voltage vs. Output Sink Current

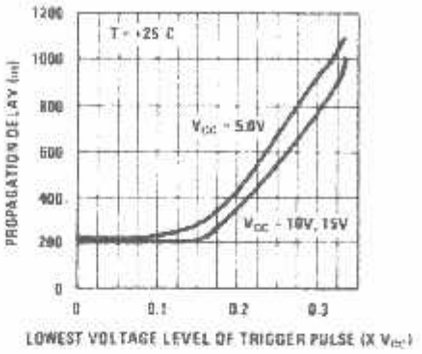


Low Output Voltage vs. Output Sink Current

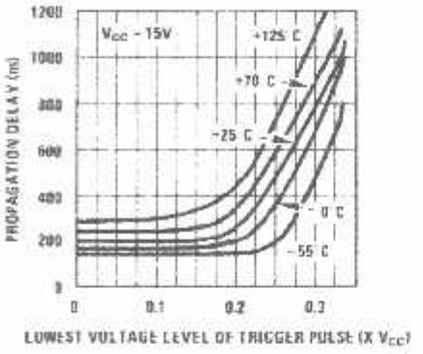


Typical Performance Characteristics (Continued)

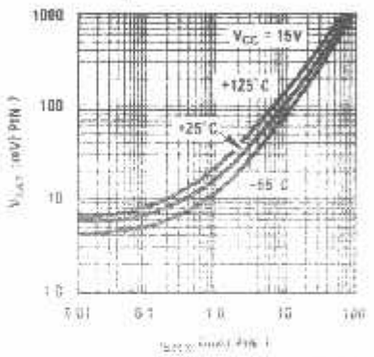
Output Propagation Delay vs.
Voltage Level of Trigger Pulse



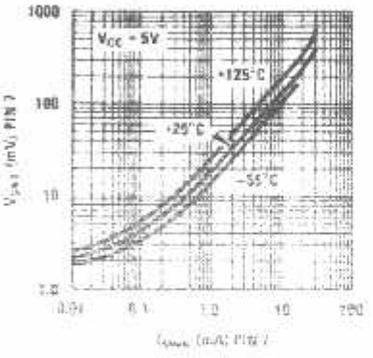
Output Propagation Delay vs.
Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7)
Voltage vs. Sink Current



Discharge Transistor (Pin 7)
Voltage vs. Sink Current



Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

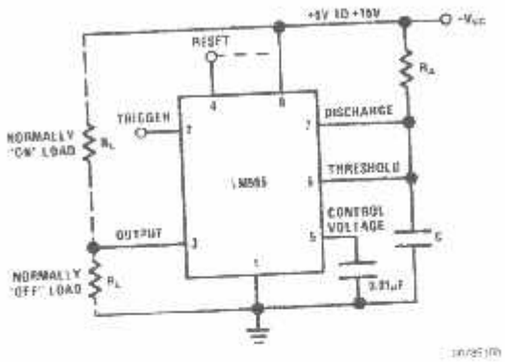
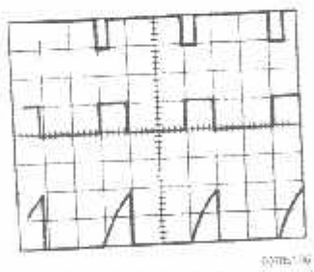


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A\ C$, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



V_{CC} = 5V
TIME = 0.1 ms/DIV
R_A = 9.1kΩ
C = 0.01μF

Top Trace: Input 5V/Div
Middle Trace: Output 5V/Div
Bottom Trace: Capacitor Voltage 2V/Div

FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

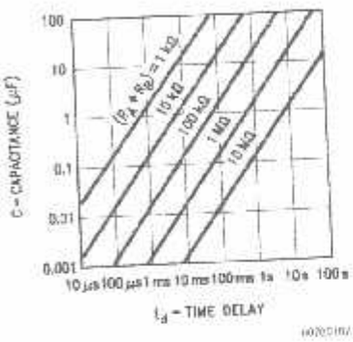


FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

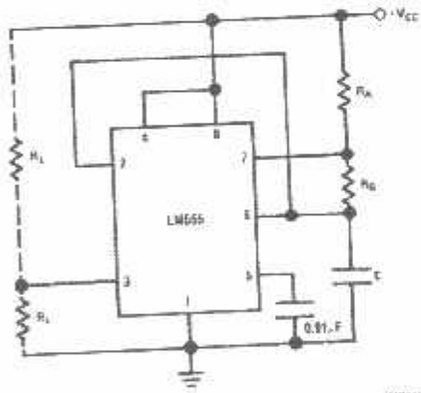
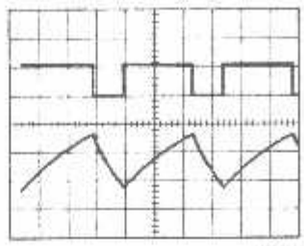


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



V_{CC} = 5V
TIME = 20μs/DIV.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01μF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

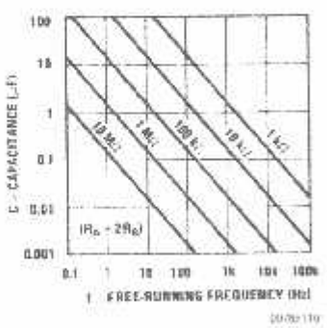
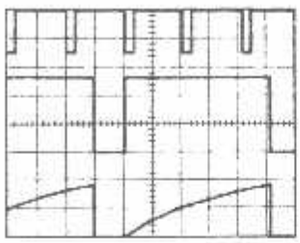


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



V_{CC} = 5V
TIME = 20μs/DIV.
R_A = 9.1kΩ
C = 0.01μF

Top Trace: Input 5V/Div.
Middle Trace: Output 2V/Div.
Bottom Trace: Capacitor 2V/Div.

FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

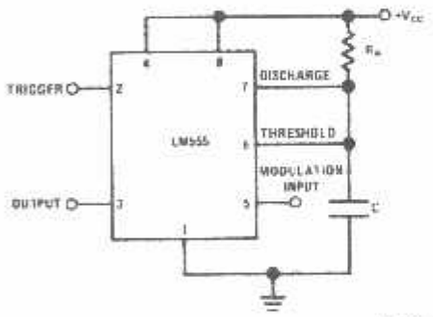
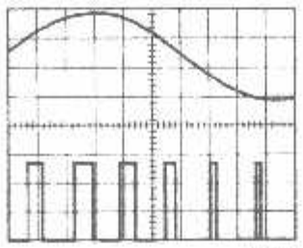


FIGURE 8. Pulse Width Modulator

Applications Information (Continued)



V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1kΩ
C = 0.01µF

FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

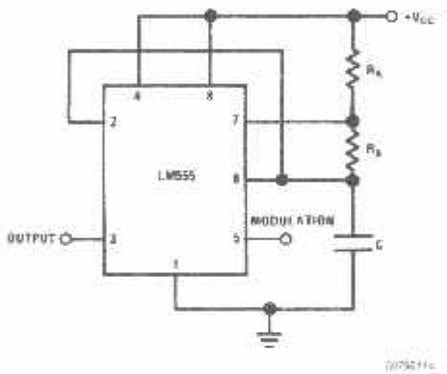
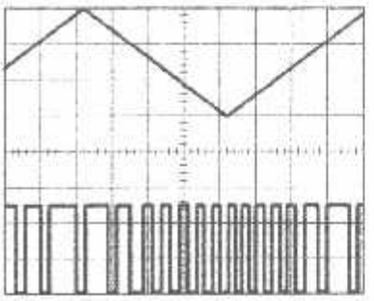


FIGURE 10. Pulse Position Modulator



V_{CC} = 5V Top Trace: Modulation Input 1V/Div.
TIME = 0.1 ms/DIV Bottom Trace: Output 2V/DIV
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.

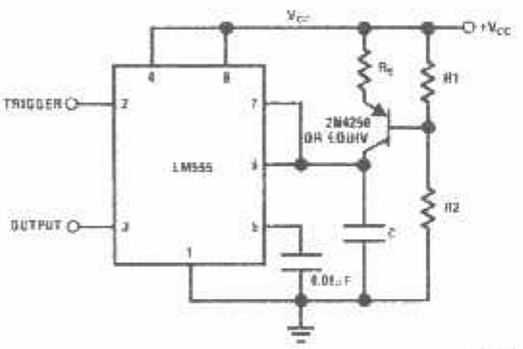


FIGURE 12.

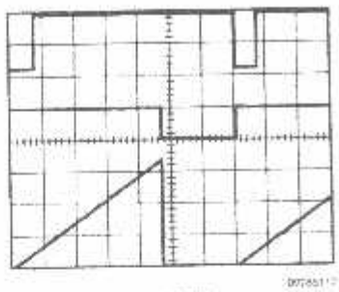
Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)}$$

$V_{BE} = 0.6V$

$V_{EE} = 0.6V$

Applications information (Continued)



V_{CC} = 5V — Top Trace: Input 3V/Div
TIME = 20μs/Div. — Middle Trace: Output 5V/Div.
R_1 = 47kΩ — Bottom Trace: Capacitor Voltage 1V/Div
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 μF

FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is t_2 =

$$\left[(R_A\ R_B)/(R_A + R_B)\right] C\ ln\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$

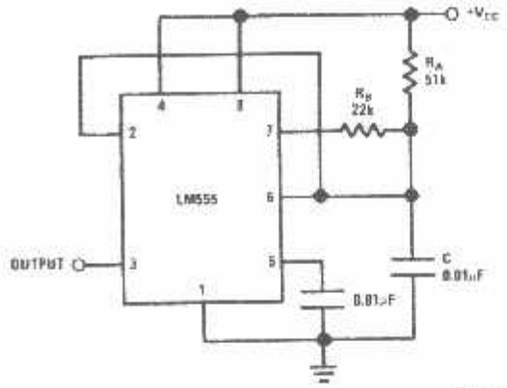


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

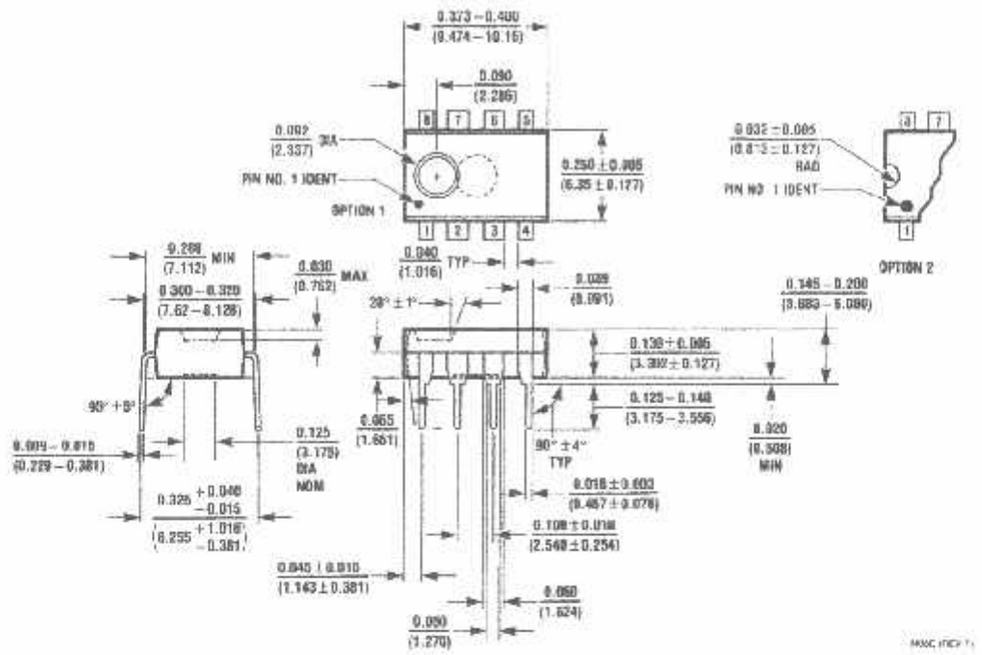
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.

Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

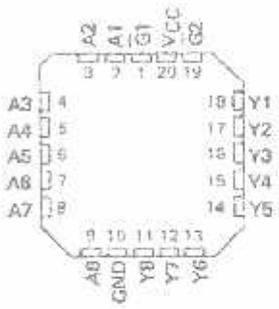


Molded Dual-In-Line Package (N)
NS Package Number N08E

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins
- Data Flow-thru Pinout (All Inputs on Opposite Side from Outputs)

SN54LS540, SN54LS541 . . . J OR W PACKAGE
SN74LS540, SN74LS541 . . . DW OR N PACKAGE
(TOP VIEW)

SN54LS540, SN54LS541 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular SN54LS240/SN74LS240 series and, at the same time, offer a pinout having the inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

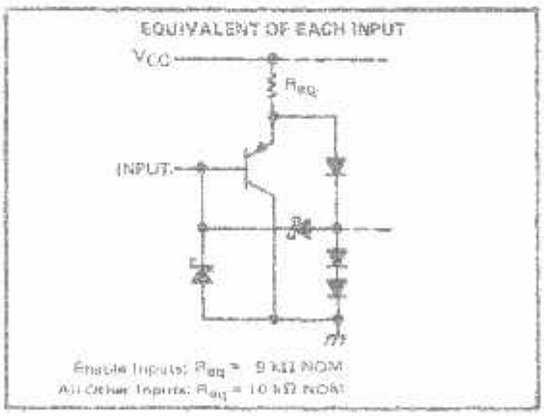
The 'LS540 offers inverting data and the 'LS541 offers true data at the outputs.

The SN54LS540 and SN54LS541 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS540 and SN74LS541 are characterized for operation from 0°C to 70°C.

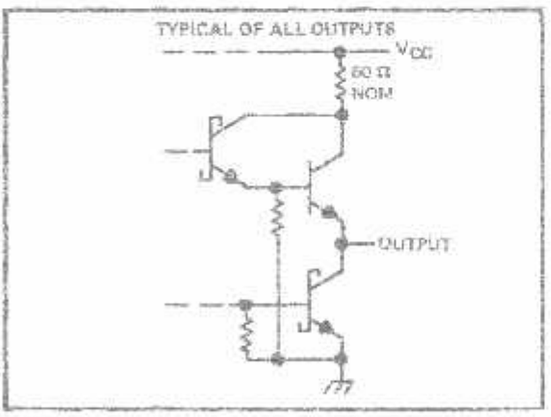
TYPE	RATED I_{OL} (SINK CURRENT)	RATED I_{OH} (SOURCE CURRENT)	TYPICAL POWER DISSIPATION (ENABLED) 'LS540	'LS541
SN54LS'	12 mA	−12 mA	92.5 mW	120 mW
SN74LS'	24 mA	−15 mA	92.5 mW	120 mW

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

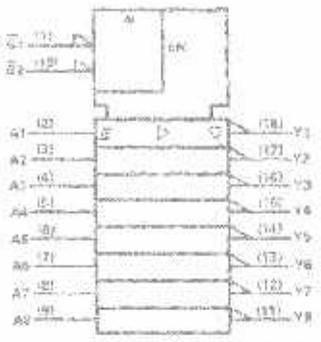


TYPICAL OF ALL OUTPUTS

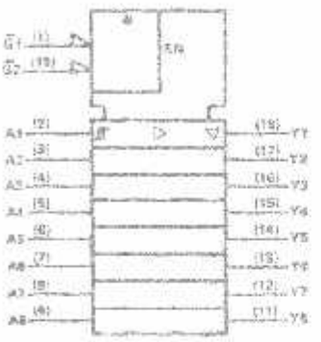


logic symbols†

'LS540



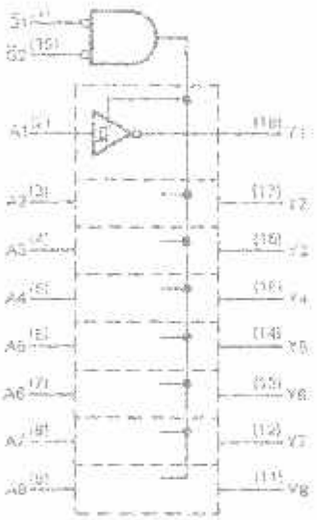
'LS541



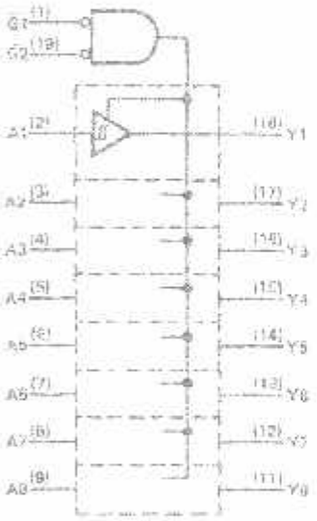
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

'LS540



'LS541



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS540, SN54LS541 . . . . . −55°C to 125°C
SN74LS540, SN74LS541 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −3 mA		2.4	3.4		2.4	3.4		V
		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.5 V, I_{OH} = MAX		2			2			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current, any input	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.2			−0.2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Outputs high	'LS540		13	25		13	25	mA
			'LS541		18	32		18	32	
		Outputs low	'LS540		24	45		24	45	
			'LS541		30	52		30	52	
		All outputs disabled	'LS540		30	52		30	52	
			'LS541		32	55		32	55	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

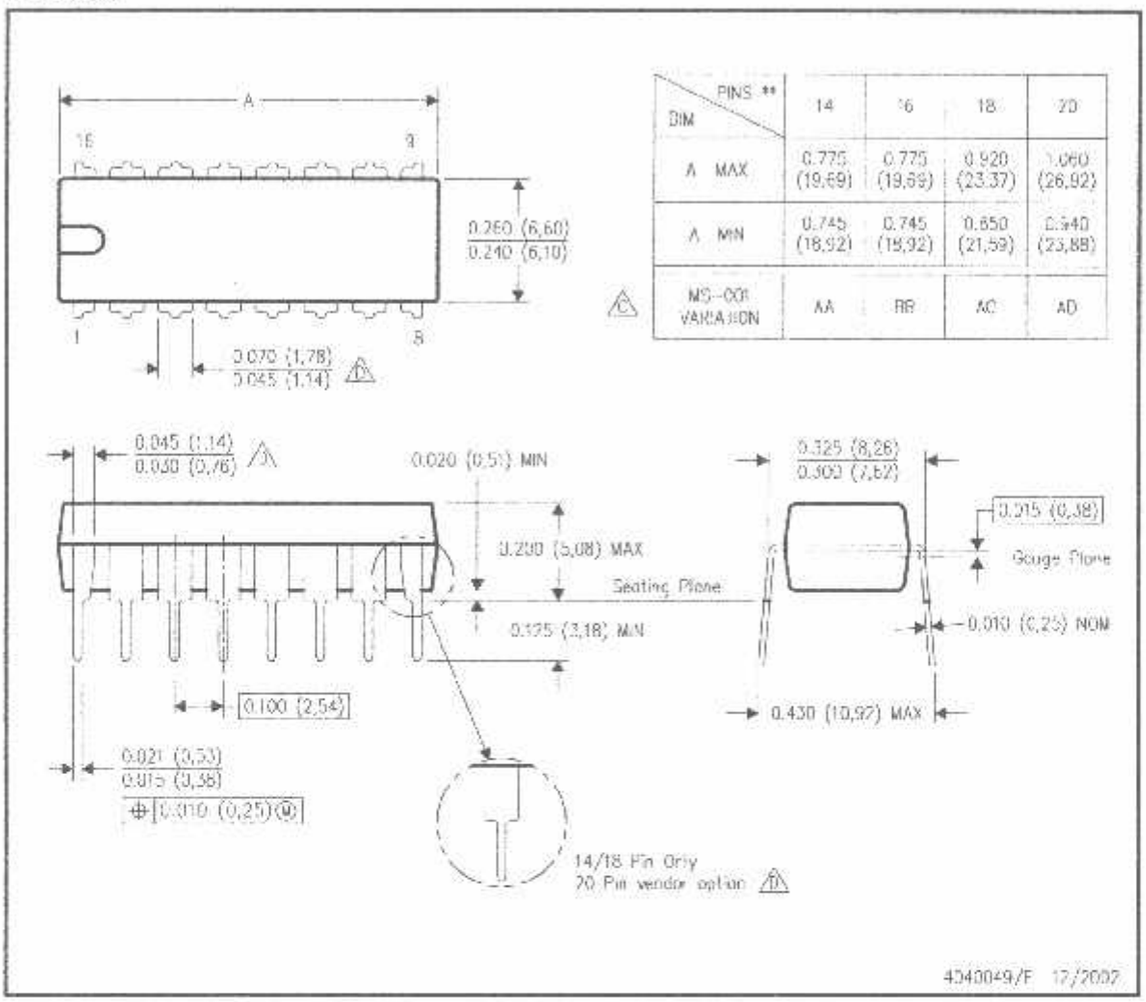
PARAMETER		TEST CONDITIONS	'LS540			'LS541			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, R_L = 667 Ω, See Note 2		9	15		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	15		10	15	ns
t_{PZL}	Output enable time to low level			25	39		28	39	ns
t_{PZH}	Output enable time to high level			15	25		20	32	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, R_L = 667 Ω, See Note 2		10	18		10	18	ns
t_{PHZ}	Output disable time from high level			15	25		18	29	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

N (R–PDIP–T**)

16 PINS SHOWN

PLASTIC DUAL–IN–LINE PACKAGE



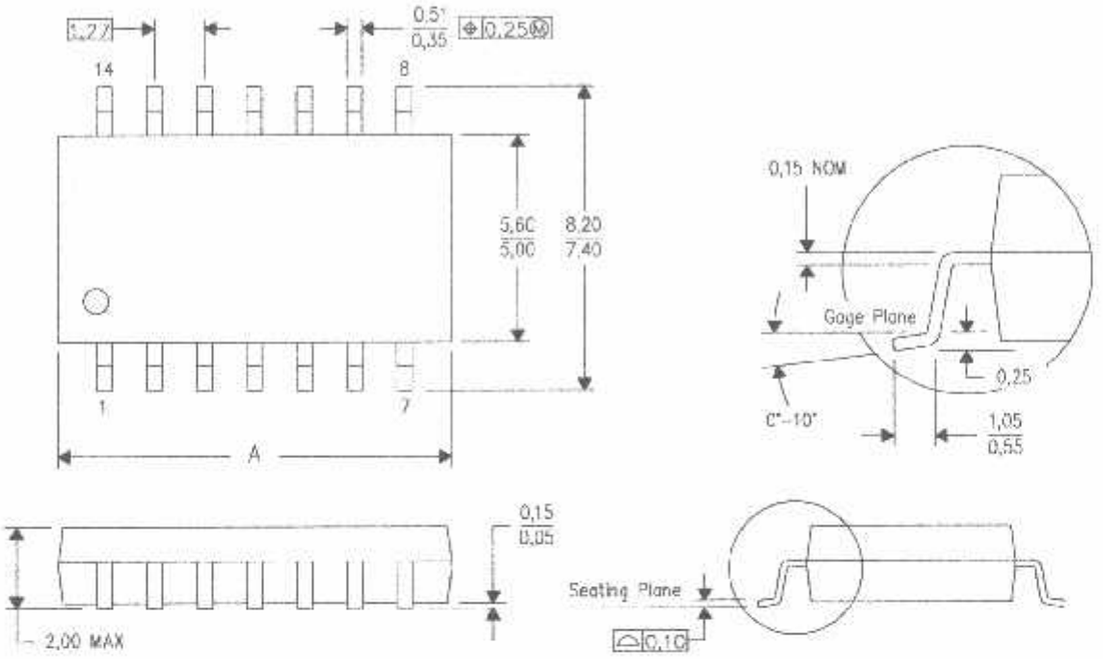
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NS (R-PDSO-G)** — **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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National Semiconductor

July 8, 2009

ADC0808/ADC0809

8-Bit µP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

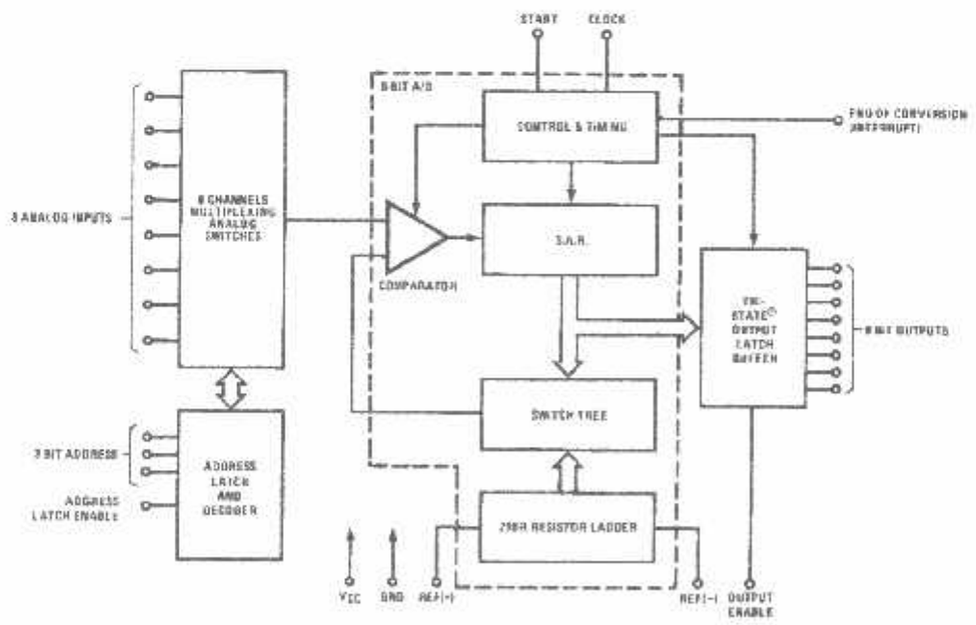
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to V_{CC} input range
- Outputs meet TTL voltage level specifications
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

Resolution	8 Bits
Total Unadjusted Error	±½ LSB and ±1 LSB
Single Supply	5 V_{DC}
Low Power	15 mW
Conversion Time	100 µs

Block Diagram



See Ordering Information

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN}=15V			1.0	µA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN}=0	-1.0			µA
I_{CC}	Supply Current	f_{CLK}=640 kHz		0.3	3.0	mA
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V I_{OUT} = -360µA I_{OUT} = -10µA	 **2.4** **4.5**			 V V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O=1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O=1.2 mA			0.45	V
I_{OUT}	TRI-STATE Output Current	V_O=5V V_O=0	 -3		3	µA µA

Electrical Characteristics – Timing Specifications

Timing Specifications V_{CC}=$V_{REF(+)}$=5V, $V_{REF(-)}$=GND, t_r=t_f=20 ns and T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{STCLK}	Start Time Delay from Clock	(*Figure 5*)	300		900	ns
t_{WS}	Minimum Start Pulse Width	(*Figure 5*)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(*Figure 5*)		100	200	ns
t_S	Minimum Address Set-Up Time	(*Figure 5*)		25	50	ns
t_H	Minimum Address Hold Time	(*Figure 5*)		25	50	ns
t_D	Analog MUX Delay Time From ALE	R_S=0Ω (*Figure 5*)		1	2.5	µs
t_{1H}, t_{H0}	OE Control to Q Logic State	C_L=50 pF, R_L=10k (*Figure 8*)		125	250	ns
t_{0H}, t_{H0}	OE Control to Hi-Z	C_L=10 pF, R_L=10k (*Figure 8*)		125	250	ns
t_C	Conversion Time	f_c=640 kHz, (*Figure 5*) (Note 7)	90	100	116	µs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(*Figure 5*)	0		8 + 2 µS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A Zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper-stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (*Figure 5*). See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description

MULTIPLEXER

The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. *Table 1* shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1. Analog Channel Selection

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (*Figure 1*) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion start pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

Timing Diagram

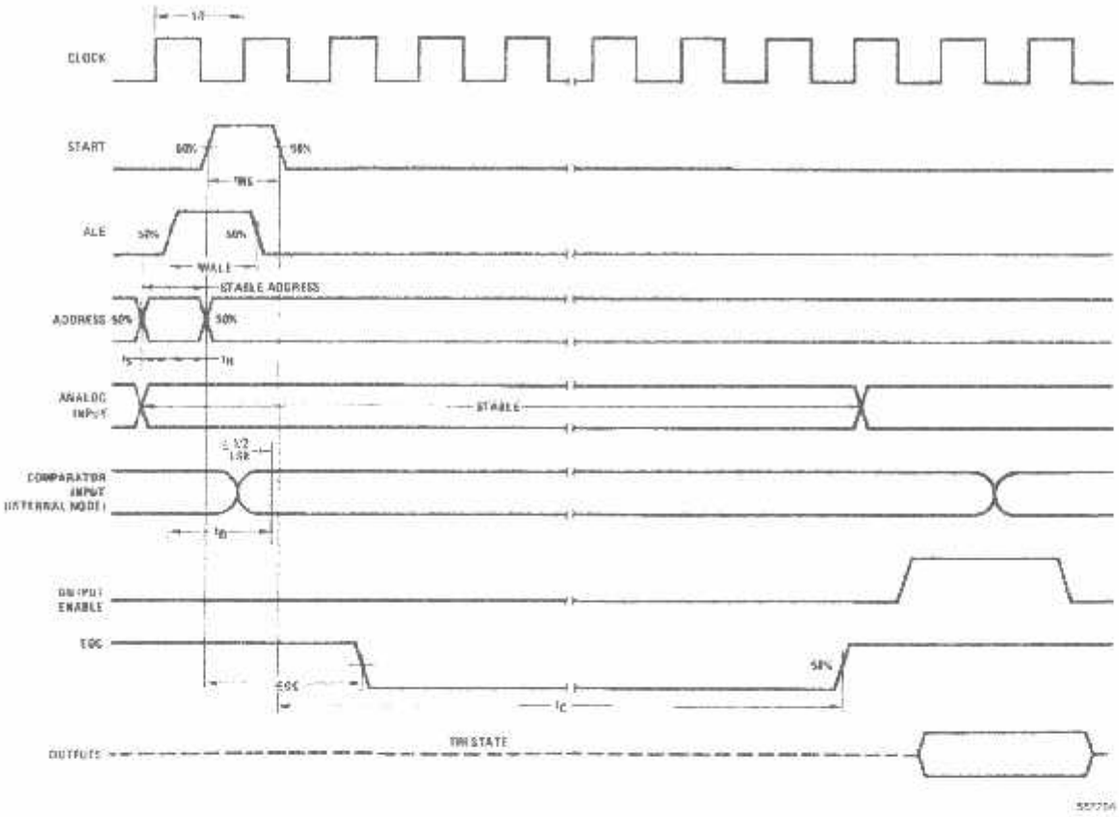


FIGURE 5.

TRI-STATE Test Circuits and Timing Diagrams

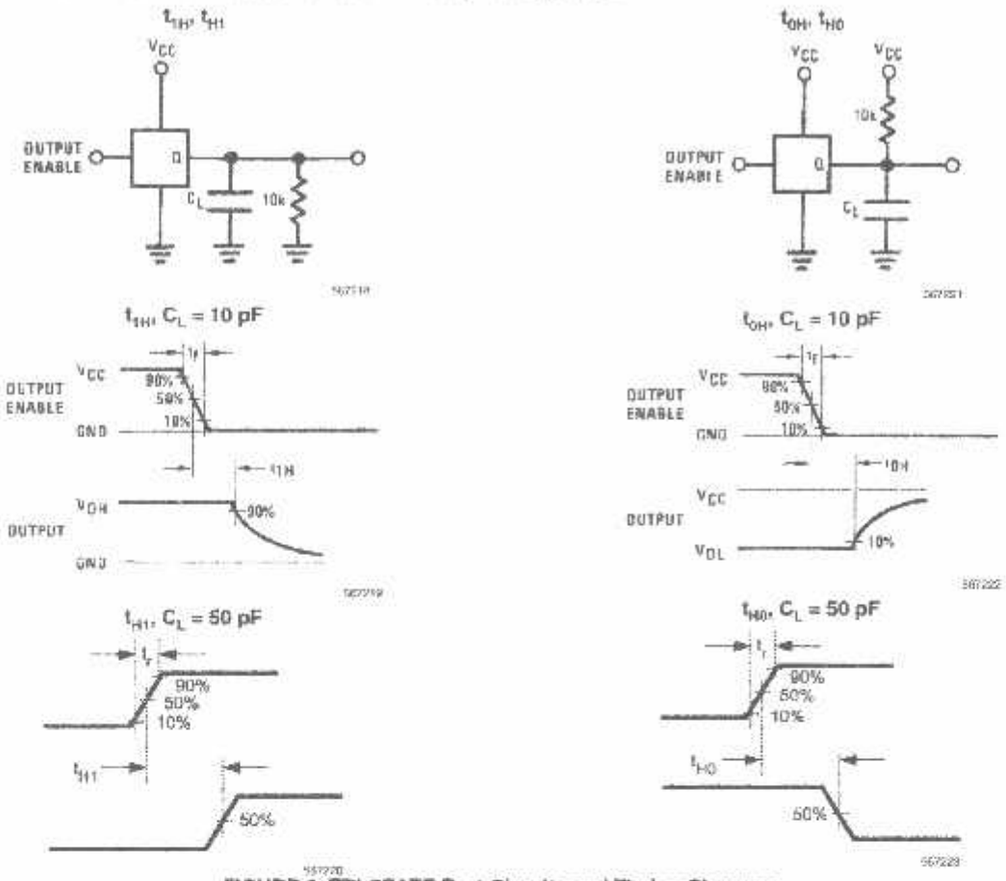


FIGURE 8. TRI-STATE Test Circuits and Timing Diagrams

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{MAX} - D_{MIN}} \qquad (1)$$

V_{IN}= Input voltage into the ADC0808

V_{fs}= Full-scale voltage

V_Z= Zero voltage

D_X= Data point being measured

D_{MAX}= Maximum data limit

D_{MIN}= Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs. (*Figure 9*).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if V_{CC}=V_{REF}=5.12V, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

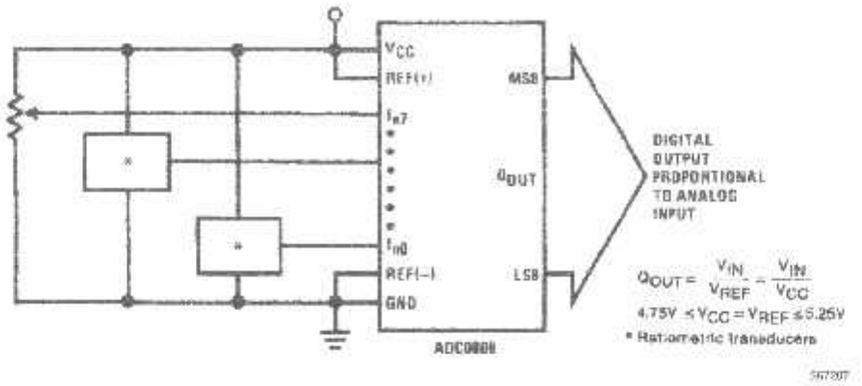
2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected info 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(-), should not be more negative than ground. The center of the ladder volt-

age must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.



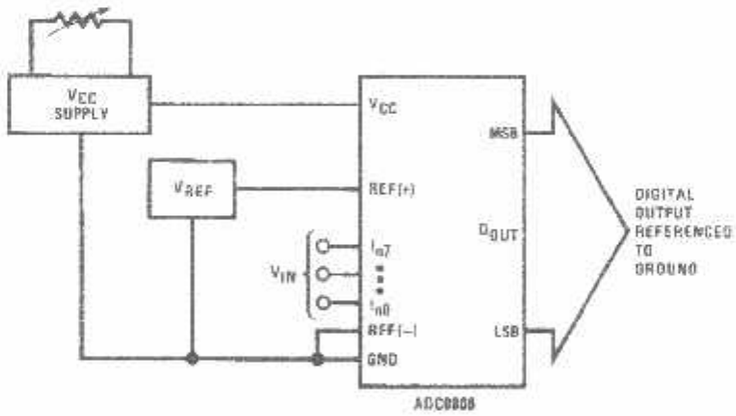
$$D_{OUT} = \frac{V_{IN}}{V_{REF}} = \frac{V_{IN}}{V_{CC}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 9. Ratiometric Conversion System

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 µF output capacitor.

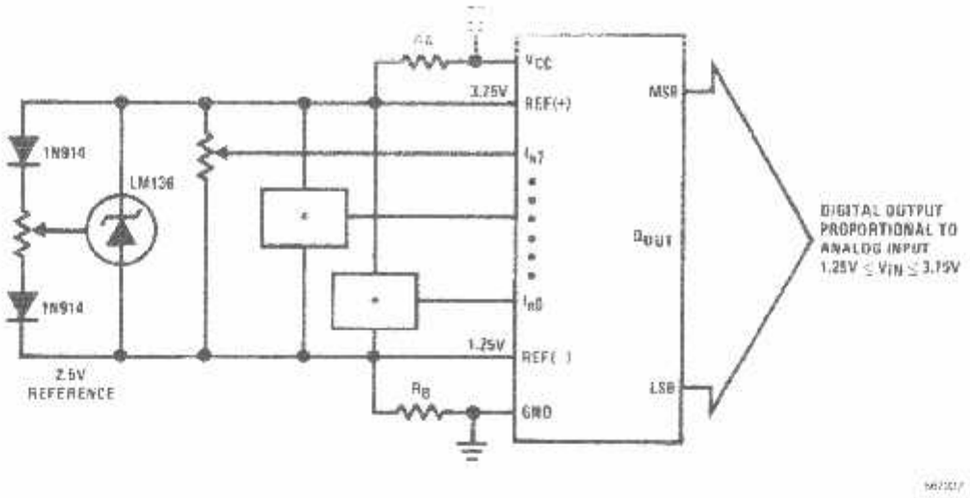
The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.



$$D_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply



$R_A=R_B$

*Ratiometric transducers

FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N+1 is given by:

$$V_{IN}=\left\{(V_{REF(+)}-V_{REF(-)})\left[\frac{N}{256}+\frac{1}{512}\right]\pm V_{TUE}\right\}+V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN}\left\{(V_{REF(+)}-V_{REF(-)})\left[\frac{N}{256}\right]+V_{TUE}\right\}+V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N=\frac{V_{IN}-V_{REF(-)}}{V_{REF(+)}-V_{REF(-)}}\times 256\pm\text{Absolute Accuracy} \quad (4)$$

Where: V_{IN}=Voltage at comparator input

$V_{REF(+)}$=Voltage at Ref(+)

$V_{REF(-)}$=Voltage at Ref(−)

V_{TUE}=Total unadjusted error voltage (typically $V_{REF(+)}$÷512)

4.0 ANALOG COMPARATOR INPUTS

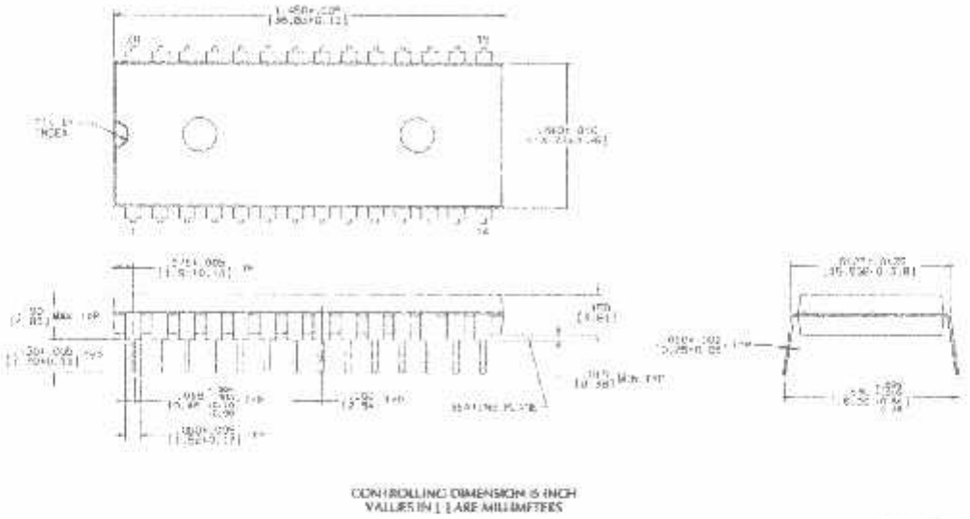
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

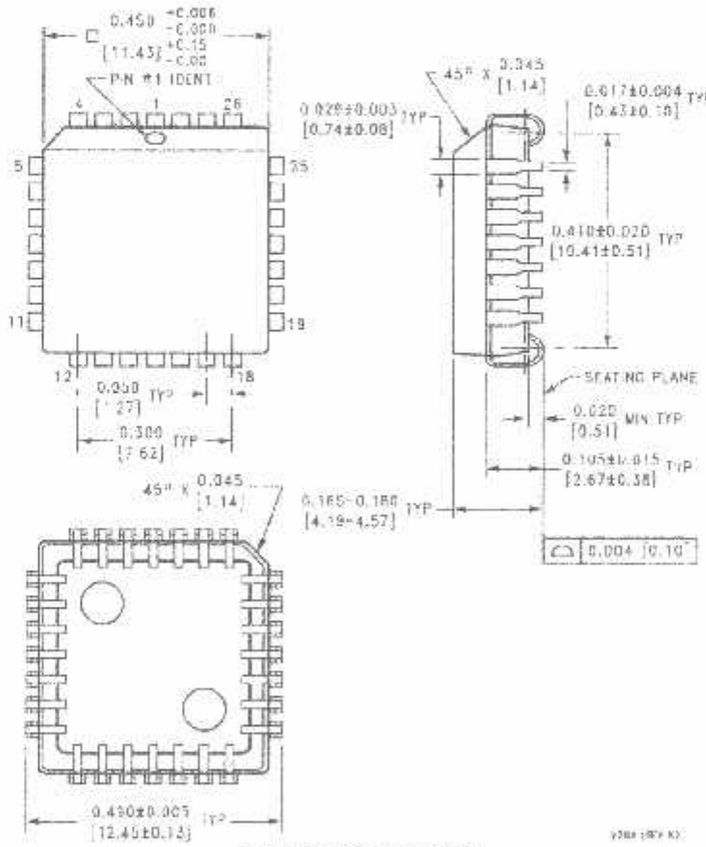
Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NA28E (Rev B)

Molded Dual-In-Line Package (N)
Order Number ADC0808CCN or ADC0809CCN
NS Package Number NA28E



Molded Chip Carrier (V)
Order Number ADC0808CCV or ADC0809CCV
NS Package Number V28A

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

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Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
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Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
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LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
Wireless (PLL/VCO)	www.national.com/wireless	PowerWise® Design University	www.national.com/training

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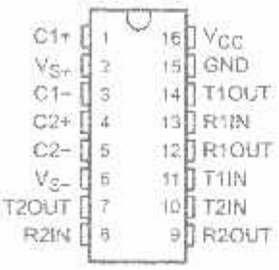
SLLS047L – FEBRUARY 1989 – REVISED MARCH 2004

- Meets or Exceeds TIA/EIA-232-F and ITU Recommendation V.28
- Operates From a Single 5-V Power Supply With 1.0-μF Charge-Pump Capacitors
- Operates Up To 120 kbit/s
- Two Drivers and Two Receivers
- ±30-V Input Levels
- Low Supply Current . . . 8 mA Typical
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
- Upgrade With Improved ESD (15-kV HBM) and 0.1-μF Charge-Pump Capacitors is Available With the MAX202
- Applications
  - TIA/EIA-232-F, Battery-Powered Systems, Terminals, Modems, and Computers

MAX232 . . . D, DW, N, OR NS PACKAGE
MAX232I . . . D, DW, OR N PACKAGE
(TOP VIEW)



description/ordering information

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	MAX232N	MAX232N
	SOIC (D)	Tube of 40	MAX232D	MAX232
		Reel of 2500	MAX232DR	
	SOIC (DW)	Tube of 40	MAX232DW	MAX232
		Reel of 2000	MAX232DWR	
	SOP (NS)	Reel of 2000	MAX232NSR	MAX232
−40°C to 85°C	PDIP (N)	Tube of 25	MAX232IN	MAX232IN
	SOIC (D)	Tube of 40	MAX232ID	MAX232I
		Reel of 2500	MAX232IDR	
	SOIC (DW)	Tube of 40	MAX232IDW	MAX232I
		Reel of 2000	MAX232IDWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

EACH DRIVER

INPUT TIN	OUTPUT TOUT
L	H
H	L

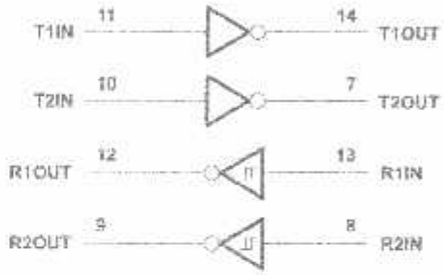
H = high level, L = low level

EACH RECEIVER

INPUT RIN	OUTPUT ROUT
L	H
H	L

H = high level, L = low level

logic diagram (positive logic)



DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 4)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT, T2OUT	R_L = 3 kΩ to GND		5	7		V
V_{OL}	Low-level output voltage‡	T1OUT, T2OUT	R_L = 3 kΩ to GND			−7	−5	V
r_o	Output resistance	T1OUT, T2OUT	V_{S+} = V_{S-} = 0,	V_O = ±2 V	300			Ω
I_{OS}§	Short-circuit output current	T1OUT, T2OUT	V_{CC} = 5.5 V,	V_O = 0		±10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN	V_I = 0				200	µA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
§ Not more than one output should be shorted at a time.
NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ, See Figure 2			30	V/µs
SR(t)	Driver transition region slew rate	See Figure 3		3		V/µs
	Data rate	One TOUT switching		120		kbit/s

NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 4)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R1OUT, R2OUT	I_{OH} = −1 mA		3.5			V
V_{OL}	Low-level output voltage‡	R1OUT, R2OUT	I_{OL} = 3.2 mA				0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V,	T_A = 25°C		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V,	T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	R1IN, R2IN	V_{CC} = 5 V		0.2	0.5	1	V
r_i	Receiver input resistance	R1IN, R2IN	V_{CC} = 5,	T_A = 25°C	3	5	7	kΩ

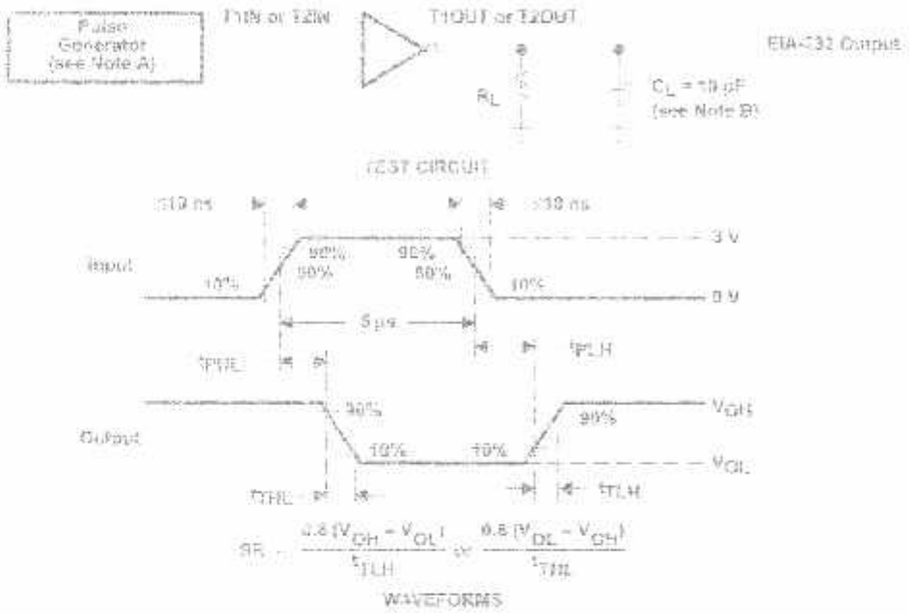
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 4 and Figure 1)

PARAMETER		TYP	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	500	ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	500	ns

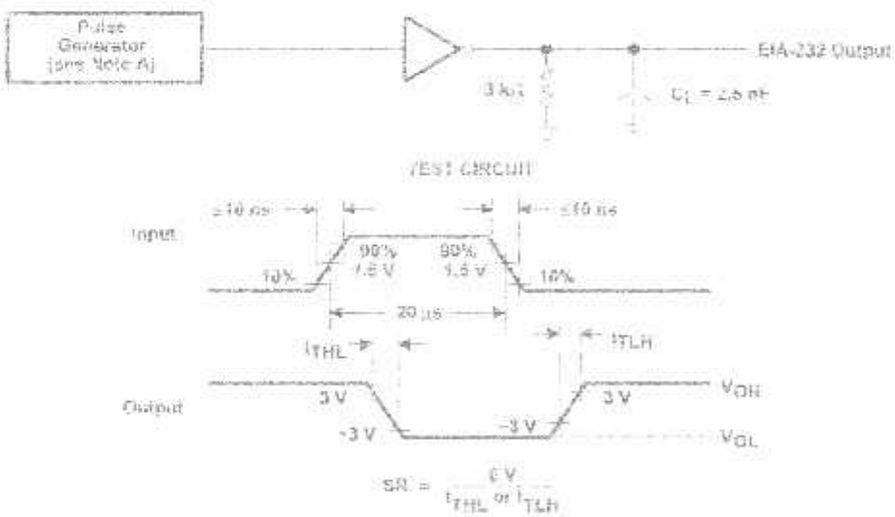
NOTE 4: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

Figure 2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5-µs Input)

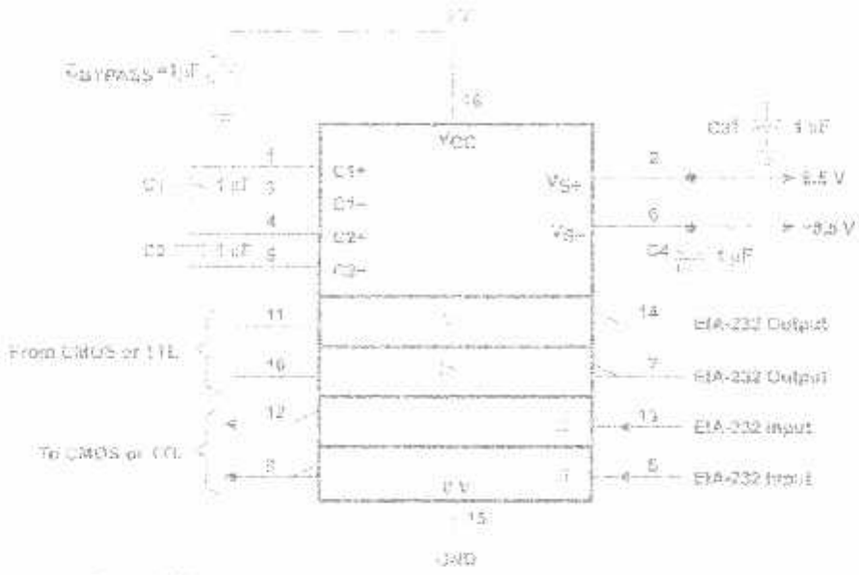


NOTE A: The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

Figure 3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20-µs Input)

SLLS047L – FEBRUARY 1989 – REVISED MARCH 2004

APPLICATION INFORMATION



†C2 can be connected to VCC in some applications.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1-µF capacitors shown, the MAX232I can operate with 0.1-µF capacitors.

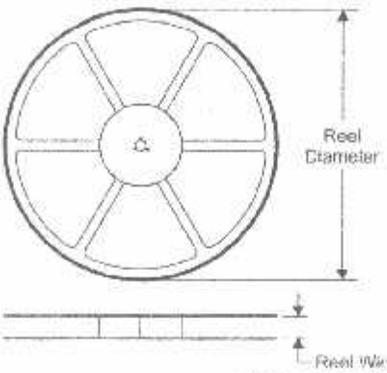
Figure 4. Typical Operating Circuit

PACKAGING INFORMATION

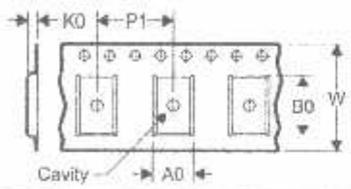
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MAX232D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX232IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

TAPE AND REEL INFORMATION

REEL DIMENSIONS

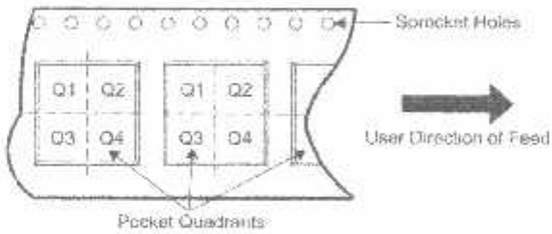


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



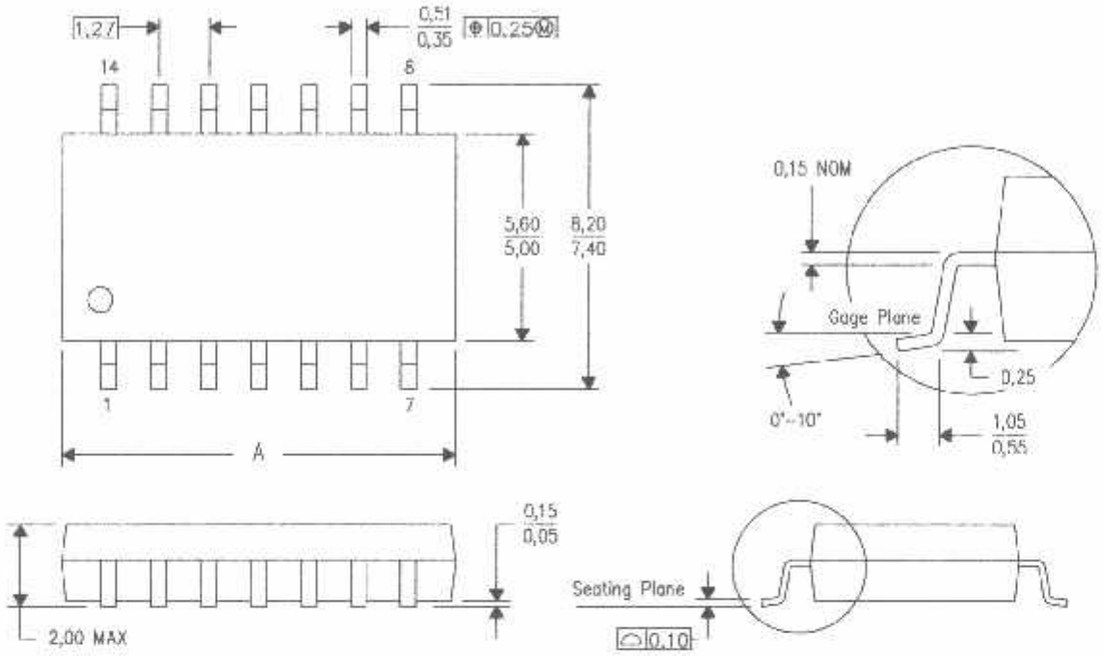
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MAX232IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MAX232NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

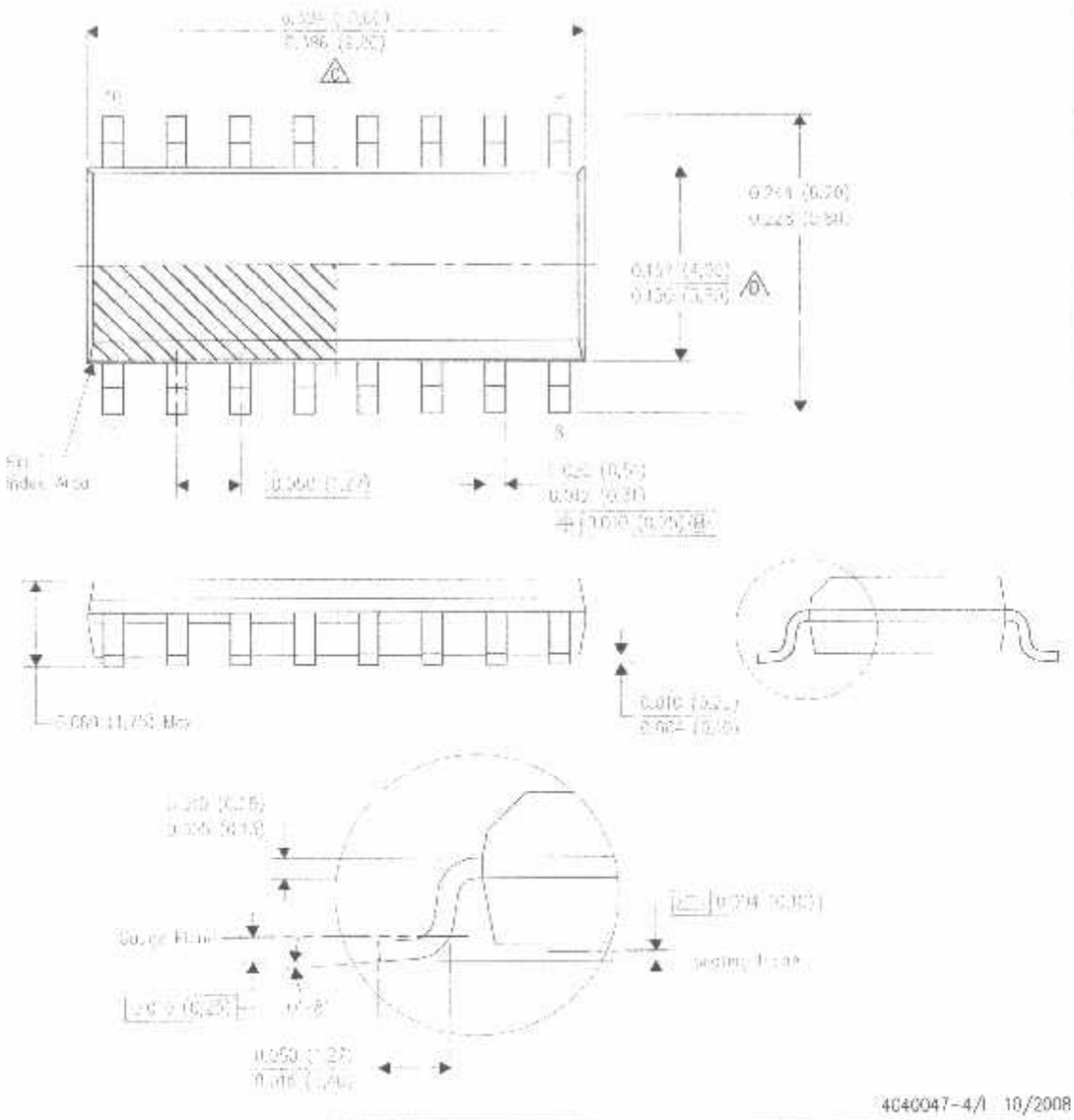


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

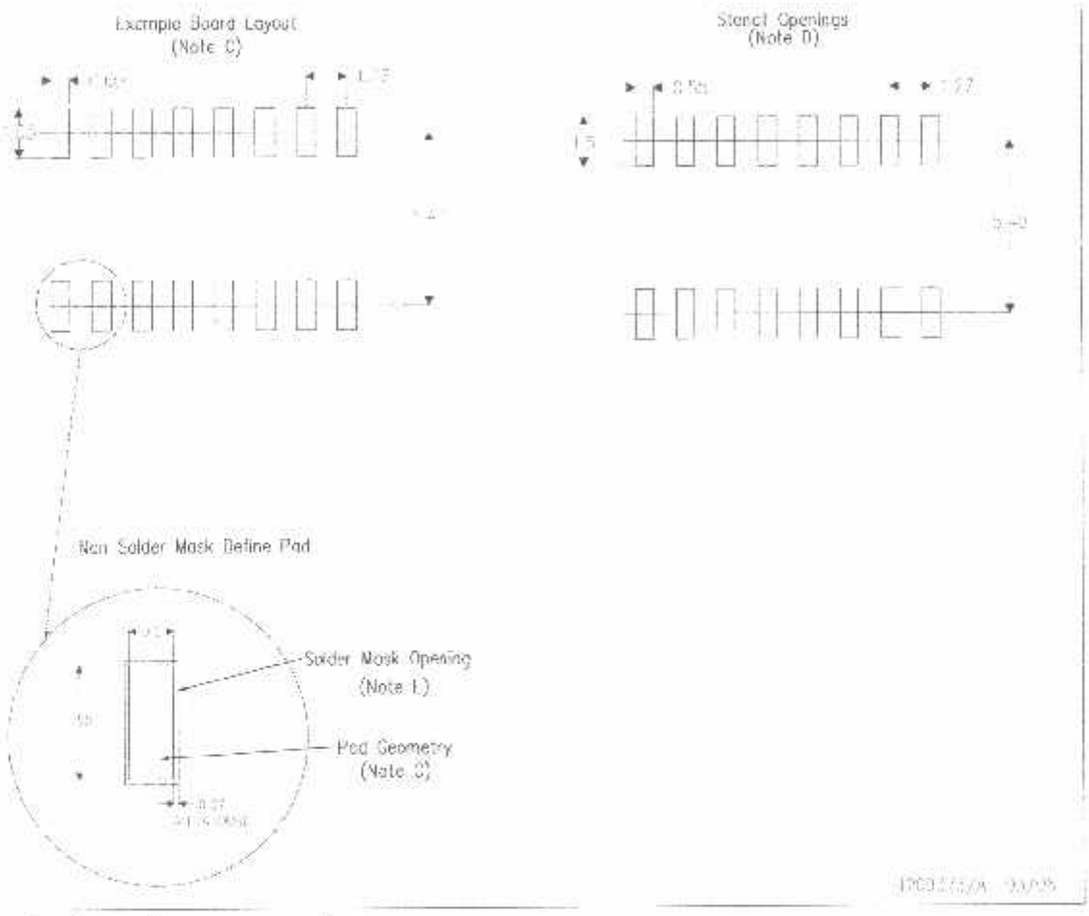
D (R-PDSO-G16) PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/I 10/2008

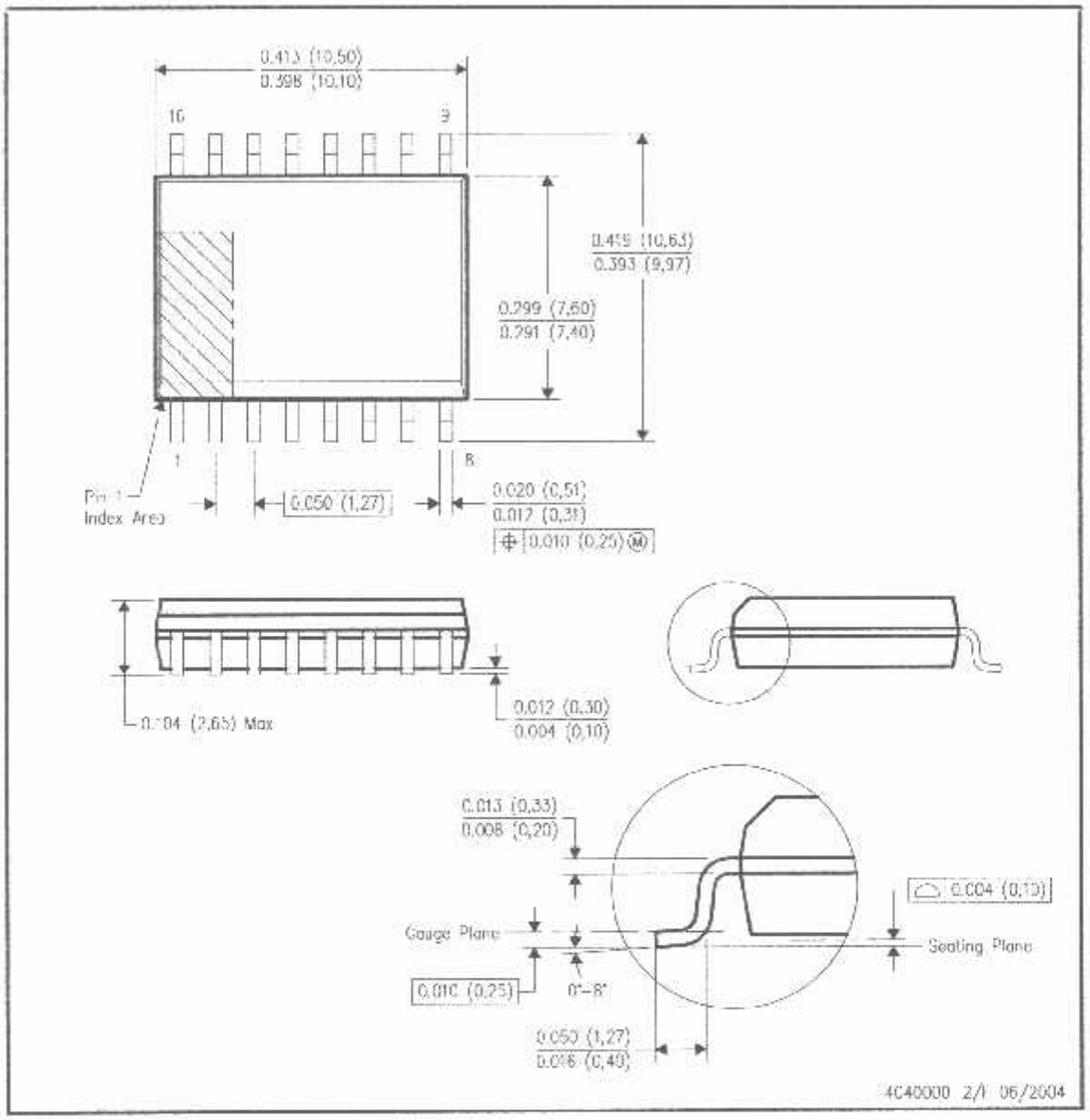
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
△ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
△ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
D. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE

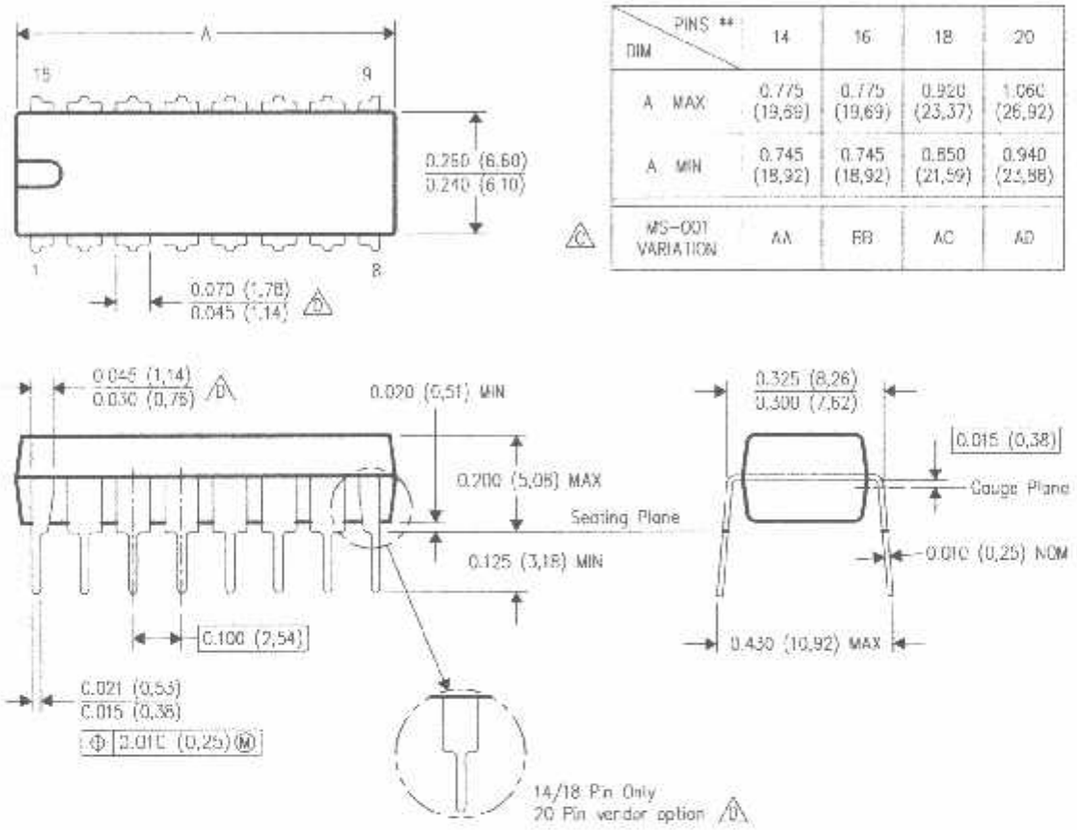


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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